TEXAS INSTRUMENTS

Programmable Logic

Data Book

Data Book

Programmable Logic

1990

1990

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The Programmable Logic Data Book

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INTRODUCTION

In this data book, Texas Instruments (TI) presents technical information on TI's broad line of programmable logic devices (PLDs), including the high-speed 5-ns PAL® circuits and high-density, low-power, Erasable Programmable Logic Devices (EPLDs). More than 40 PLD functions in industry standard architectures are available from Texas Instruments. For high-performance applications, TI also offers several high-speed programmable state machine devices. Where low power and reprogrammability are key considerations, TI offers its family of EPLDs. This data book includes specifications on existing and future products including:

- High-performance, low-power IMPACT™ and IMPACT-X™ 20- and 24-pin standard PAL® circuits including TI's new 5-ns device
- TI's high-speed 6-ns programmable address decoder, TIBPAD18N8-6
- Flexible, '22V10-architecture macrocell PAL® ICs including TI's enhanced version, the TIBPAL22VP10
- Fast, 50-MHz programmable state machines, including enhanced versions of the '82S105B/167B and TI's complex TIBPLS506
- The TIBPSG507, programmable sequence generator with internal 6-bit counter and 50-MHz performance
- Higher speed versions of the industry standard EPLD architectures including the 20-ns EP630.

Texas Instruments high-speed programmable bipolar devices utilize TI's advanced IMPACT™ and new IMPACT-X™ technologies. IMPACT-X™ uses trench isolation and polysilicon emitters to increase performance and reduce power dissipation compared to traditional processes. For EPLDs, TI utilizes its 1.0 micron high-voltage EPIC™ CMOS technology to combine the benefits of low power and higher speed.

This volume contains design and specification data for 183 device types. Package dimensions are given in the Mechanical Data section in metric measurement (and parenthetically in inches). In some cases, package dimensions are included in the actual data sheet.

Several programmable logic application reports have been incorporated into this book to aid in the design of TI PLDs. User notes also explain considerations for programming and testing of PLDs in a manufacturing environment.

Complete technical data for any Texas Instrument semiconductor product is available from your nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at 1-800-232-3200.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART 1 — GENERAL CONCEPTS AND CLASSIFICATIONS OF CIRCUIT COMPLEXITY

Chip-Enable Input

A control input that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in reduced-power standby mode.
NOTE: See "chip-select input."

Chip-Select Input

A gating input that when inactive prevents input or output of data to or from an integrated circuit.
NOTE: See "chip-select input."

Field-Programmable Logic Array (FPLA)

A user-programmable integrated circuit whose basic logic structure consists of a programmable AND array and whose outputs feed a programmable OR array.

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration (LSI)

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context, a major sybsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Medium-Scale Integration (MSI)

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Memory Cell

The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Memory Integrated Circuit

An integrated circuit consisting of memory cells and usually including associated circuits such as those for address selection, amplifiers, etc.

Output-Enable Input

A gating input that when active permits the integrated circuit to output data and when inactive causes the integrated circuit output(s) to be at a high impedance (off).

Output-Enable Input

A gating input that when active permits the integrated circuit to output data and when inactive causes the integrated circuit output(s) to be at a high impedance (off).

Programmable Array Logic (PAL®)

A user-programmable integrated circuit which utilizes proven fuse link technology to implement logic functions. Implements sum of products logic by using a programmable AND array whose outputs feed a fixed OR array.

Read/Write Memory

A memory in which each cell may be selected by applying appropriate electronic input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electronic input signals.

Small-Scale Integration (SSI)

Integrated circuits of less complexity than medium-scale integration (MSI)

Typical (TYP)

A calculated value representative of the specified parameter at nominal operating conditions (V_{CC} = 5 V, T_A = 25°C), based on the measured value of devices processed, to emulate the process distribution.

Very-Large-Scale Integration (VLSI)

A concept whereby a complete system function is fabricated as a single microcircuit. In this context, a system, whether digital or linear, is considered to be one that contains 3000 or more gates or circuitry of similar complexity.

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PART 2 — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} (I_O) **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

*Current out of a terminal is given as a negative value.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IK} **Input clamp voltage**
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

t_a **Access time**
The time interval between the application of a specific input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}).

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets.

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
	=	value/level is reentered
X	=	irrelevant (any input, including transitions)
Z	=	off (high impedance) state of a 3-state output
a ... h	=	the level of steady-state inputs A through H respectively
Q_0	=	the level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
	=	one high-level pulse
	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

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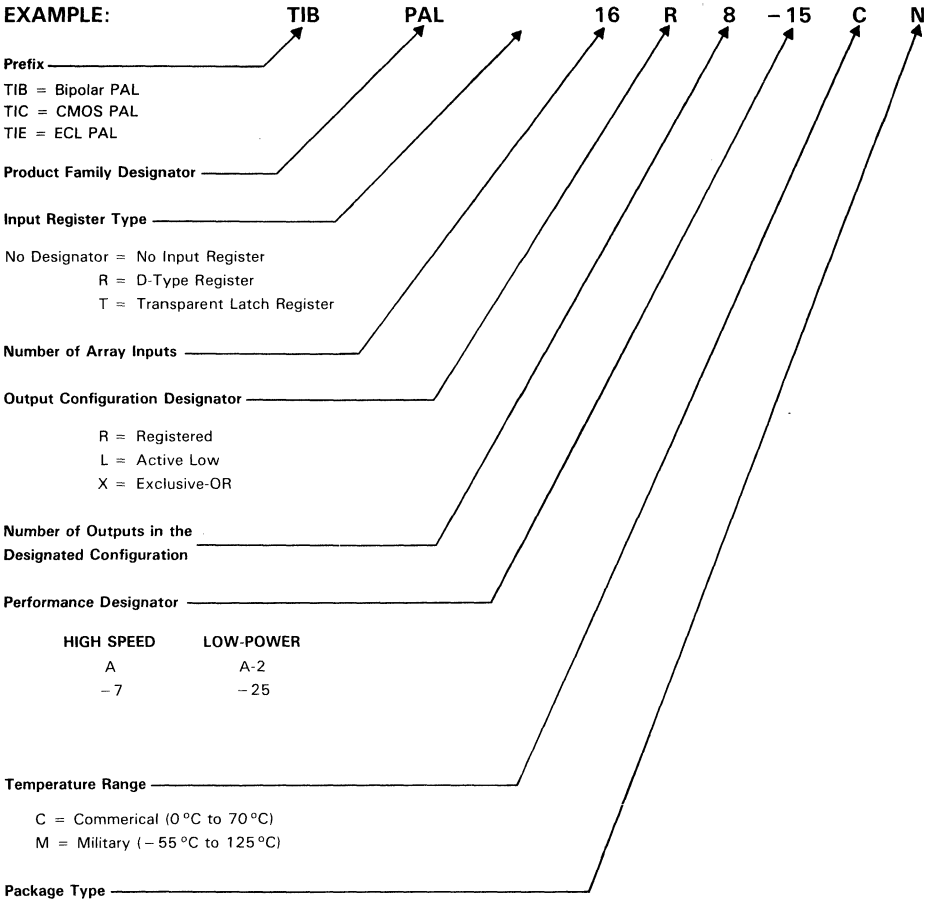
PAL® NUMBERING SYSTEM AND ORDERING INSTRUCTIONS

Factory orders for leadership PAL® circuits described in this catalog should include a nine-part type number as explained in the example below. Exclude the prefix when ordering standard PALs.



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ADDRESSES FOR PAL® AND FPLA PROGRAMMING AND SOFTWARE MANUFACTURERS†

adams-macDonald enterprises, Inc.
800 Airport Road
Monterey, CA 93940
(408) 373-3607

ADVIN SYSTEMS INC.
1050-L East Duane Ave.
Sunnyvale, CA 94086
(408) 984-8600

ANVIL SOFTWARE
427-3 Amherst St.
Suite 341
Nassua, NH 03063
(617) 641-3861

Bytek Corporation
508 Northwest 77th St.
Boca Raton, FL 33487
(407) 994-3520

BP MICROSYSTEMS
10681 Haddington,
Suite #190
Houston, TX 77043
(713) 461-9430

DATA I/O (*ABEL Design Software*)
10525 Willows Road, N.E.
Redmond, WA 98073-9746
(800) 247-5700

INLAB INC. (*proLogic Design Software*)
2150-1 West 6th Ave.
Broomfield, CO 80020
(303) 460-0103
(800) 237-6759

LOGICAL DEVICES INC. (*CUPL Design Software*)
1201 N.W. 65th Place
Ft. Lauderdale, FL 33309
(305) 974-0967
(800) 331-7766

MINC Incorporated (*PLDesigner Software*)
1575 York Road
Colorado Springs, CO 80918
(719) 590-1155

Microprоss
Parc d'acivité des Prés
5, rue Denis Papin
59650 VILLENEUVE D'ASCQ;
FRANCE
(20) 47.90.40

STAG MICRO SYSTEMS
1600 Wyatt Drive
Santa Clara, CA 95054
(800) 227-8836

System-General Corp.
3Fl., No. 6, Lane 4,
Tun Hwa N. Rd.,
P.O. Box: 53-591
Taipei, Taiwan, R.O.C.
886-2-9173005
886-2-9111283 FAX

System-General America
510 South Paric Victoria
Malpitas, CA 93035
(408) 263-6667
(408) 262-9220 FAX

†Texas Instruments does not endorse or warrant the suppliers referenced. Presently, Texas Instruments has certified DATA I/O, Sunrise, Structured Design and Digital Media. Other programmers are now in the certification process. For a current list of certified programmers, please contact your local TI sales representative.

Design and programming assistance is offered by Texas Instruments IMPACT™ Design and Service Centers. The centers are equipped with the latest in software and hardware tools for design, debugging, prototyping, and production on a local basis. Supported by a professional engineering staff, the centers provide complete code development, device programming, symbolization, functional and DC parametric testing.

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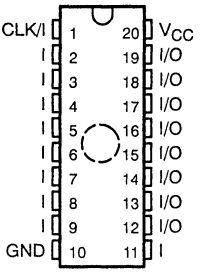
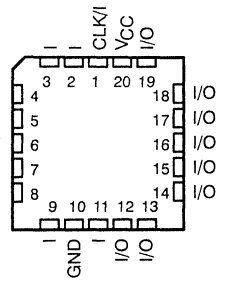
- Programmable Replacement for Conventional TTL, 74HC, and 20-Pin PAL® Family
- UV-Light-Erasable Cell Technology Provides:
  - — Reconfigurable Logic
  - — Reprogrammable Cells
  - — Full Factory Testing for 100% Programming Yields
- High-Voltage EPIC™ Process Allows for Higher Performance as follows:

  Maximum t_{pd}: – 25M . . . 25 ns
  –20I . . . 20 ns
  –15C . . . 15 ns
- User-Programmable Output Logic Macrocells Provide Flexibility in Output Types with:
  - — Selectable for Registered or Combinational Operation
  - — Output Polarity Control
  - — Independently User Programmable Feedback Path
- Programmable Design-Security Bit Prevents Copying of Logic Stored in Device
- Advanced Software Support Featuring Schematic Capture, Interactive Netlist, Boolean Equations, and State-Machine Design Entry
- Package Options Include:
  - — 20-pin Ceramic Dual-In-Line (J) — UV-erasable
  - — 20-pin Plastic Dual-In-Line (N) — One-Time Programmable
  - — 20-pin Plastic Chip Carrier (FN) — One-Time Programmable

J OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

PRODUCT PREVIEW

description

general

The EP330 features advanced-CMOS speed and very low power. It combines the High-Voltage Enhanced-Processed Implanted CMOS (HVEPIC™) process with ultraviolet-light-erasable technology. Each output has an Output-Logic-Macrocell (OLM) configuration that allows user definition of the output type. This EPLD provides a reliable low-power substitute for numerous high-performance TTL PALs.

AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PACKAGE TYPE		
		CERAMIC DUAL-IN-LINE (J)	PLASTIC DUAL-IN-LINE (N)	PLASTIC CHIP CARRIER (FN)
–55°C to 125°C	25 ns	EP330-25MJB	N/A	N/A
–40°C to 85°C	20 ns	EP330-20IJ	EP330-20IN	EP330-20IFN
0°C to 70°C	15 ns	EP330-15CJ	EP330-15CN	EP330-15CFN

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description (continued)

The EP330 can accommodate up to 18 inputs and up to eight outputs. The 20-pin 300-mil package contains eight macrocells each using a programmable AND/fixed-OR structure. This AND-OR structure yields eight product terms for the logic function as well as an individual term for Output Enable.

The EP330 output-logic macrocell allows the user to configure output and feedback paths for combinational or registered operation either active high or active low. With a t_{pd} of 15 ns, the EP330 may be configured as a low-power substitute for popular PAL devices such as the PAL16XXB series or the PAL16XX-15 series.

The CMOS EPROM technology makes it possible for the EP330 to operate at an active power-consumption level that is less than 75% of equivalent bipolar devices without sacrificing speed performance. This technology also facilitates 100% generic testability as well as UV-light erasability. As a result, designs and design modification can be quickly effected with a given EP330 without the need for post-programming testing.

Programming the EP330 is accomplished with the use of the TI EPLD development system, which supports four different design entry methods. When the design has been entered, the A+PLUS software (which is the heart of the development system) performs automatic translation into logical equations, performs complete Boolean minimization, and fits the design directly into an EP330. The device can then be programmed to achieve customized working silicon within minutes at the designer's desk.

The EP330M is characterized for operation over the full military temperature range of −55°C to 125°C. The EP330I is characterized for operation from −40°C to 85°C. The EP330C is characterized for operation from 0°C to 70°C.

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functional description

Externally, the EP330 provides ten dedicated inputs (one of which may be used as a synchronous clock input) and eight I/O pins that may be configured for input, output, or bidirectional operation.

The logic diagram shows the complete EP330, while Figure 1 shows the basic EP330 macrocell. The internal architecture is organized with the familiar sum of products (AND-OR) structure. Inputs to the programmable AND array (shown running vertically in Figure 1) come from two sources: first, the true and complement of the ten dedicated input pins and second, the true and complement of the eight feedback signals, each one originating from an I/O architecture-control block. The 36-input AND array encompasses a total of 72 product terms distributed equally among the eight macrocells. Each product term (shown running horizontally in the logic diagram) represents a 36-input AND gate.

As shown in the logic diagram, the outputs of eight product terms are ORed together, then the output of the OR gate is sent as an input to an exclusive-OR gate. The purpose of this exclusive-OR gate is to allow the user to specify the polarity of the output signal by using the invert-select EPROM cell (active high if the EPROM cell is programmed and active low if it is not programmed).

The exclusive-OR output then feeds the I/O architecture control block. The control block configures the output for registered or combinational operation. In the registered configuration, the output is registered via a positive edge-triggered D-type flip-flop. In this condition, the feedback signal going to the array is also registered and comes directly from the output of the D-type flip-flop. In the combinational configuration, the output is nonregistered and the feedback signal comes directly from the I/O pin. In the erased state, the EP330 contains the same architectural characteristics as the PAL16L8.

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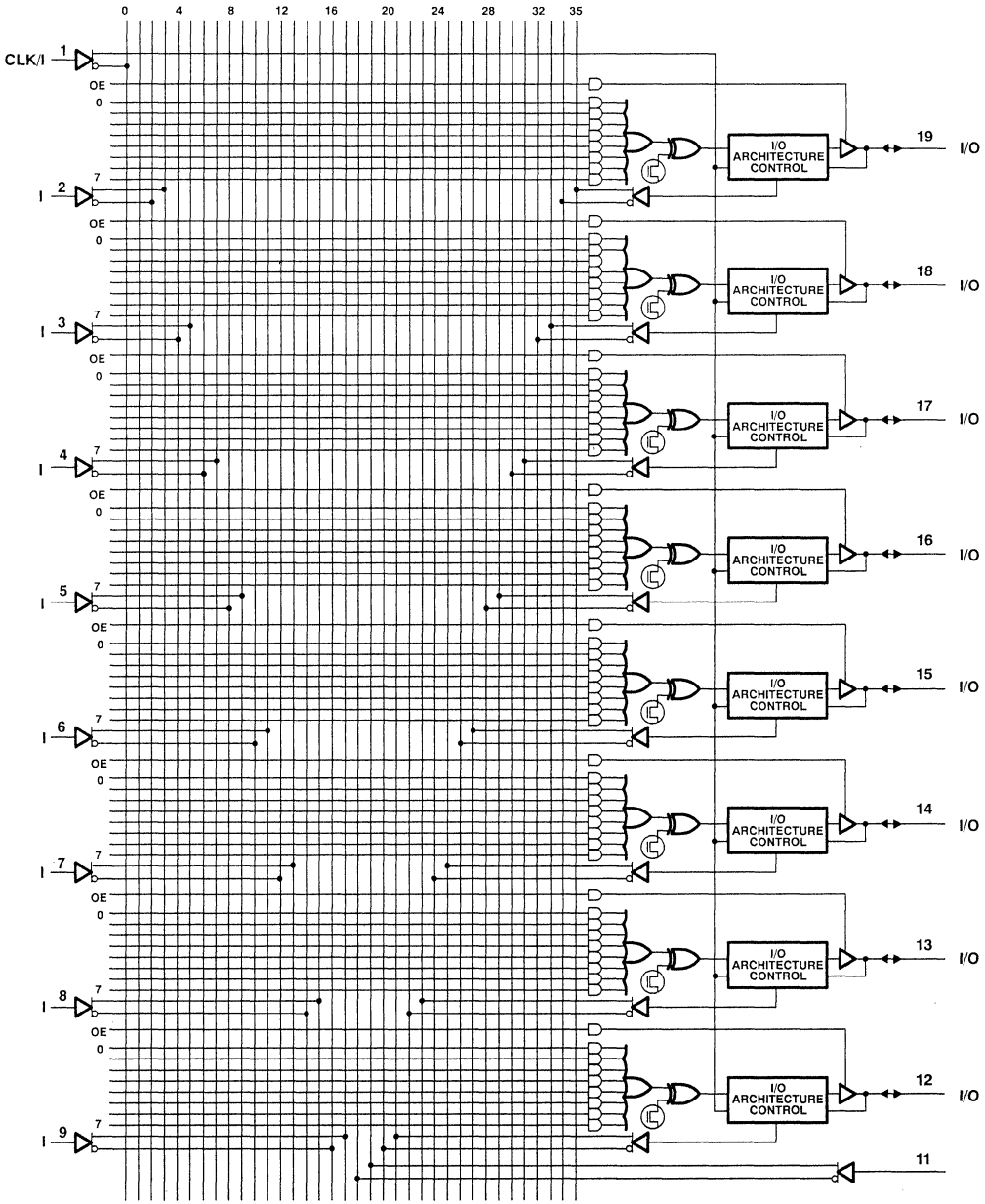
logic diagram (positive logic)



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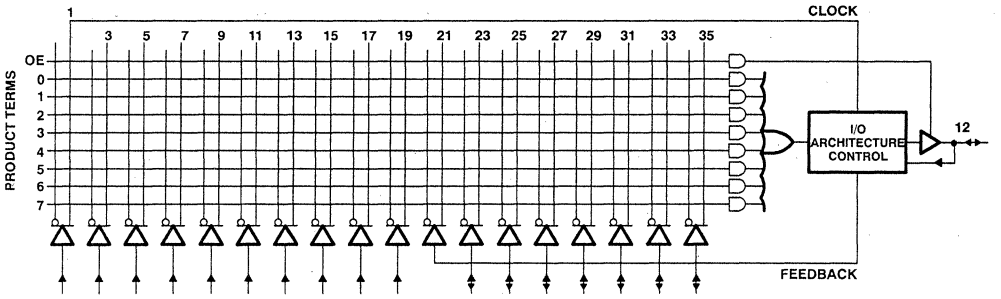

NOTES: A. This diagram shows one of the eight macrocells within the EP330.
B. The double-arrow lines (⇕) show I/O feedback from a macrocell.

FIGURE 1. LOGIC ARRAY MACROCELL

output-enable product term

The output enable (OE) product term determines whether an output signal is allowed to propagate to the output pin. If the output of the OE product term is low, then the output buffer becomes a high-impedance node, thus inhibiting the output signal from reaching the output pin. For combinational configurations, this OE product term can be used to allow for true bidirectional operation.

The EP330 contains eight separate OE product terms, one per I/O pin. If it is desired that all outputs be enabled or disabled simultaneously, use an identically programmed product term at each of the outputs. If different outputs are to be enabled under different conditions, different OE product terms for each specific output may be defined.

I/O architecture

Figure 2 shows the different output configurations that can be chosen for any of the eight I/O pins on the EP330. Because of the individuality of each I/O architecture control block, both registered and combinational output can be chosen on a given EP330 device.

In the combinational configuration, either active-high or active-low output polarity can be chosen. Pin feedback or no feedback is also optional. In the registered configuration, the user has control over output polarity and may choose to use the internal feedback path or no feedback. Any I/O pin can be configured as a dedicated input by choosing no output and no feedback from the array. In the erased state, the I/O architecture is configured for a combinational active-low output with pin feedback.

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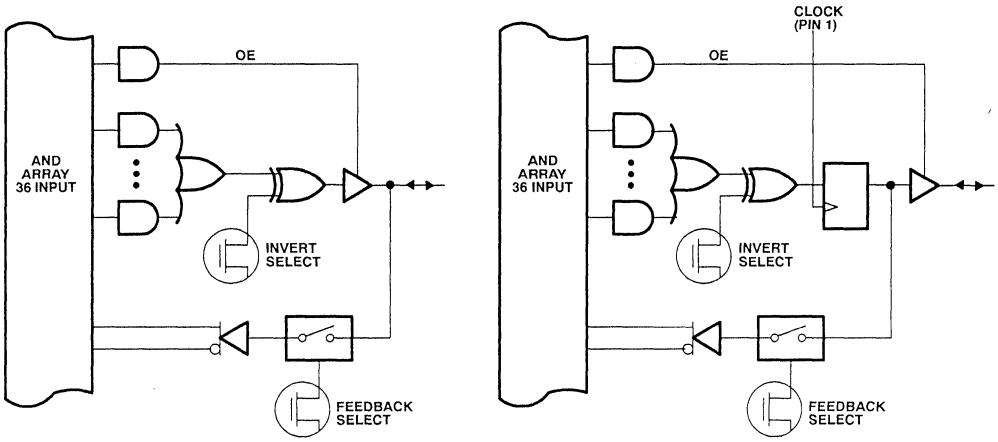

OUTPUT/POLARITY	FEEDBACK
Combinational/High	Pin, None
Combinational/Low	Pin, None
None	Pin

(a) Combinational Configuration

OUTPUT/POLARITY	FEEDBACK
D Register/High	D Register, None
D Register/Low	D Register, None
None	D Register

(b) Registered Configration

FIGURE 2. I/O CONFIGURATIONS

PAL compatibility

Figures 2(a) and 2(b) show how an EP330 can be configured as a drop-in replacement for two commonly used members of the 20-pin PAL family: the PAL16L8 and the PAL16R8. When configured in these manners, the EP330 is both a functional replacement, as well as a pin-to-pin replacement, for the PAL16L8 and PAL16R8.

Tables 1 and 2 provide additional information concerning the EP330 as a replacement for the 20-pin PAL family of devices.

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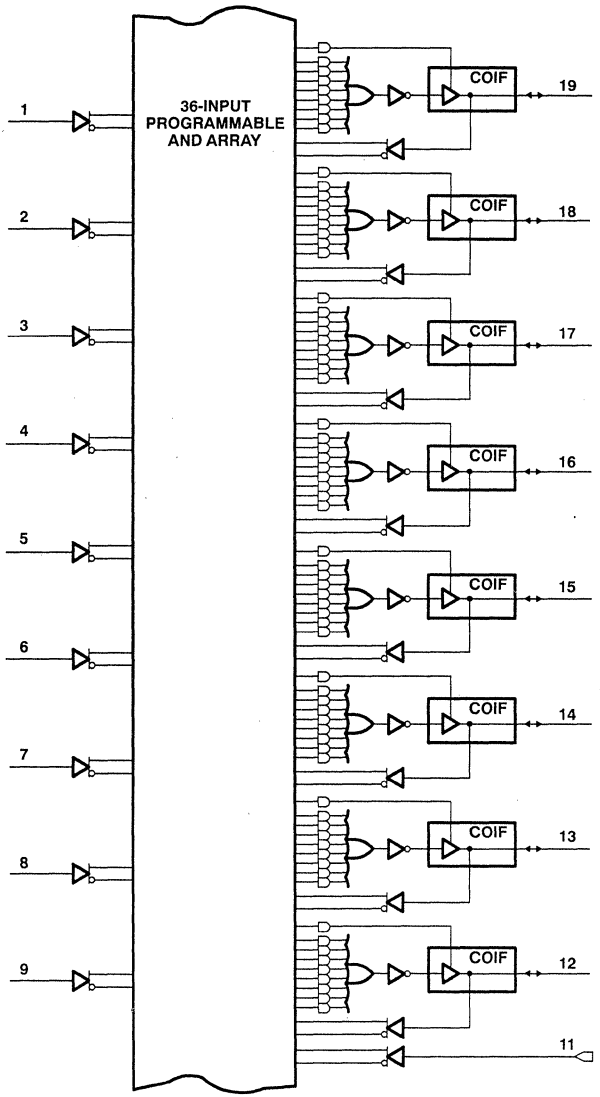
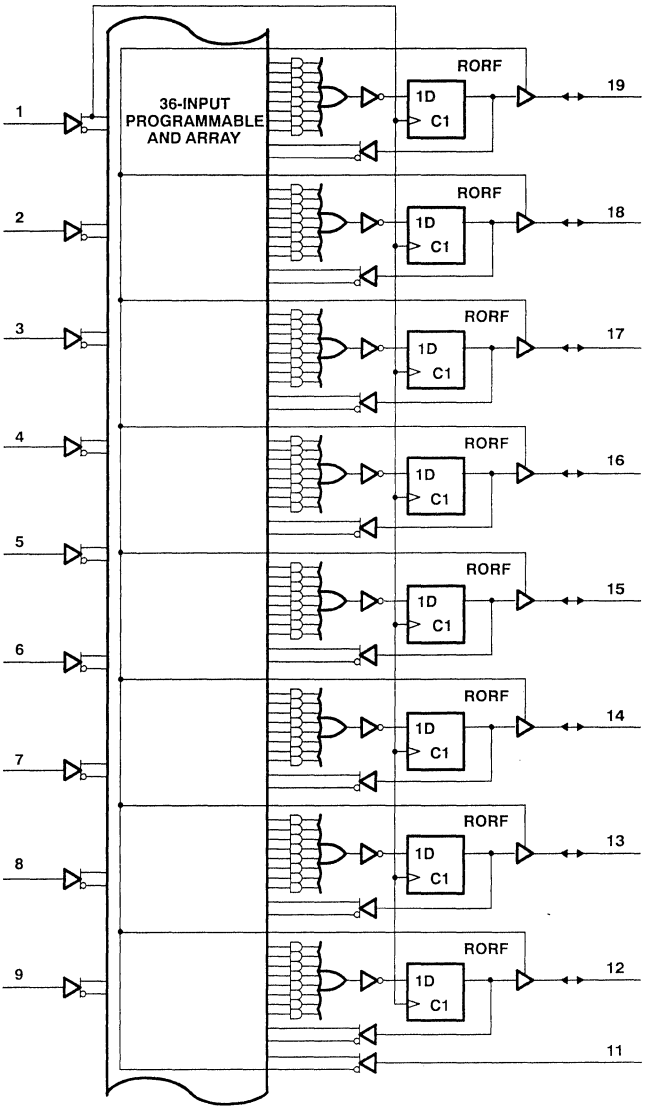


- "Invert Select" EPROM cell is in the erased state providing active-low outputs.
- "Combinational Mode" is chosen providing Combinational Output with Input (Pin) Feedback (COIF).
- 8-product-term OR gate compared to 7-product-term OR gate on PAL16L8.
- Pin feedback to the array at 12 through 19 is not available in PAL16L8.

FIGURE 3. EP330 CONFIGURATION FOR REPLACING A PAL16L8



- "Invert Select" EPROM cell is in the erased state providing active-low outputs.
- "Registered Mode" is chosen providing Registered Output with Registered Feedback (RORF).
- Complement of pin 11 is used as common OE term for all eight output pins.

FIGURE 4. EP330 CONFIGURATION FOR REPLACING A PAL16R8

PRODUCT PREVIEW

PRODUCT PREVIEW

TABLE 1. CONFIGURATIONS FOR 20-PIN PAL REPLACEMENT

PAL PART NUMBER	EP330 PIN NUMBER	EP330 MACROCELL NUMBER	I/O CONFIGURATION MODE	OUTPUT/ POLARITY	FEEDBACK
10H8	12-19	1-8	Combinational	Comb/High	None
10L8	12-19	1-8	Combinational	Comb/Low	None
12H6	12	8	Combinational	None	Pin
	13-18	2-7	Combinational	Comb/High	None
	19	1	Combinational	None	Pin
12L6	12	8	Combinational	None	Pin
	13-18	2-7	Combinational	Comb/Low	None
	19	1	Combinational	None	Pin
14H4	12-13	7-8	Combinational	None	Pin
	14-17	3-6	Combinational	Comb/High	None
	18-19	1-2	Combinational	None	Pin
14L4	12-13	7-8	Combinational	None	Pin
	14-17	3-6	Combinational	Comb/Low	None
	18-19	1-2	Combinational	None	Pin
16C1	12-14	6-8	Combinational	None	Pin
	15	5	Combinational	Comb/Low	None
	16	4	Combinational	Comb/High	None
	17-19	1-3	Combinational	None	Pin
16H2	12-14	6-8	Combinational	None	Pin
	15-16	4-5	Combinational	Comb/High	None
	17-19	1-3	Combinational	None	Pin
16L2	12-14	6-8	Combinational	None	Pin
	15-16	4-5	Combinational	Comb/Low	None
	17-19	1-3	Combinational	None	Pin
16H8	12	8	Combinational	Comb/High/Z	None
&	13-18	2-7	Combinational	Comb/High/Z	Comb
16HD8	19	1	Combinational	Comb/High/Z	None
16L8	12	8	Combinational	Comb/Low/Z	None
&	13-18	2-7	Combinational	Comb/Low/Z	Comb
16LD8	19	1	Combinational	Comb/Low/Z	None
16R4	12-13	7-8	Combinational	Comb/Low/Z	Comb
	14-17	3-6	Registered	Reg/Low/Z	Reg
	18-19	1-2	Combinational	Comb/Low/Z	Comb
16R6	12	8	Combinational	Comb/Low/Z	Comb
	13-18	2-7	Registered	Reg/Low/Z	Reg
	19	1	Combinational	Comb/Low/Z	Comb
16R8	12-19	1-8	Registered	Reg/Low/Z	Reg
16P8	12	8	Combinational	Comb/Option/Z	None
	13-18	2-7	Combinational	Comb/Option/Z	Comb
	19	1	Combinational	Comb/Option/Z	None
16RP4	12-13	7-8	Combinational	Comb/Option/Z	Comb
	14-17	3-6	Registered	Reg/Option/Z	Reg
	18-19	1-2	Combinational	Comb/Option/Z	Comb
16RP6	12	8	Combinational	Comb/Option/Z	Comb
	13-18	2-7	Registered	Re/Option/Z	Reg
	19	1	Combinational	Comb/Option/Z	Comb
16RP8	12-19	1-8	Registered	Reg/Option/Z	Reg

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TABLE 2. DEVICE SPECIFICATIONS†

SYMBOL	PARAMETER	HIGH-SPEED EPLD	HIGH-SPEED PAL SERIES 16XXB/–15	
		EP330	PAL16L8B/–15	PAL16R8B/–15
I_{CC}	Supply current active f = 1 MHz	45 mA	180 mA	180 mA
t_{pd}	Input to nonregistered output	15 ns	15 ns	N/A
t_{CO1}	Clock to output delay	12 ns	12 ns	12 ns
t_{su}	Input setup time	12 ns	15 ns	15 ns
f_{max}	Max frequency	42 MHz	37 MHz	37 MHz

† Over commercial temperature range

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... –0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \leq 20$ ns) ..... –2 V to 7 V
Programming supply voltage range, V_{PP} ..... –0.3 V to 13.5 V
Instantaneous programming supply voltage range, V_{PP} ($t \leq 20$ ns) ..... –2 V to 13.5 V
Input voltage range, V_I ..... –0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \leq 20$ ns) ..... –2 V to 7 V
V_{CC} or GND current range ..... –175 mA to 175 mA
Operating free-air temperature, T_A ..... –65°C to 135°C
Storage temperature range ..... –65°C to 150°C

NOTE 1: All voltage values are with respect to GND terminal.

recommended operating conditions

		EP330-25M		EP330-20I		EP330-15C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.75	5.25	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_{IH}	High-level input voltage	2	V_{CC}+0.3	2	V_{CC}+0.3	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
t_w	Pulse duration, CLK high or low	14		12		10		ns
t_{su}	Setup time, input	20		16		12		ns
t_h	Hold time, input	0		0		0		ns
t_r	Rise time, input	3		3		3		ns
t_f	Fall time, input	3		3		3		ns
T_A	Operating free-air temperature	–55	125	–40	85	0	70	°C

NOTE 2: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	EP330-25M		EP330-20I		EP330-15C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −8 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 24 mA		0.5		0.5		0.5	V
I_I	Input current	V_I = V_{CC}max or GND		±10		±10		±10	µA
I_{OZ}	Off-state output current	V_{CC} = MAX, V_O = V_{CC} or GND		±10		±10		±10	µA
I_{CC}	Supply current	f = 1 MHz, No load, Programmed as an 8-bit counter		70		70		45	mA
C_i	Input capacitance	V_{CC} = 5 V, V_I = 2 V, f = 1 MHz		10		10		10	pF
C_o	Output capacitance			10		10		10	pF
C_{clk}	Clock capacitance			10		10		10	pF
C_{pp}	Programming input capacitance (pin 11)			20		20		20	pF

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER‡		TEST CONDITIONS†	EP330-25M		EP330-20I		EP330-15C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	C_L = 35 pF, See Note 3	22		30		42		MHz
t_{pd}	Input to nonregistered output delay			25		20		15	ns
t_{co}	Clock input to registered output delay			24		18		12	ns
t_{PZX}	Output enable time	See Note 4		20		20		15	ns
t_{PXZ}	Output disable time			20		20		15	ns
t_{cnt}	Minimum clock period (internal)			24		20		15	ns
f_{cnt}	Maximum frequency without feedback, ($1/t_{cnt}$)		42		50		66.6		MHz

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 3. The f_{max} values shown represent the highest frequency of operation without feedback in the pipeline condition.
4. This is for an output voltage change of 500 mV.

PARAMETER MEASUREMENT INFORMATION

functional testing

The EP330 is functionally tested through complete testing of each programmable EPROM bit and all internal logic elements, thus ensuring 100% programming yield. The erasable nature of the EP330 allows test program patterns to be used and then erased.

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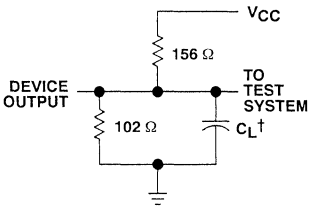
PARAMETER MEASUREMENT INFORMATION



† Includes capacitance. Equivalent loads may be used for testing.

FIGURE 5. DYNAMIC TEST CIRCUIT

design security

The EP330 contains a programmable design-security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. Therefore, a very high level of design control is achieved since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the cells in the device.

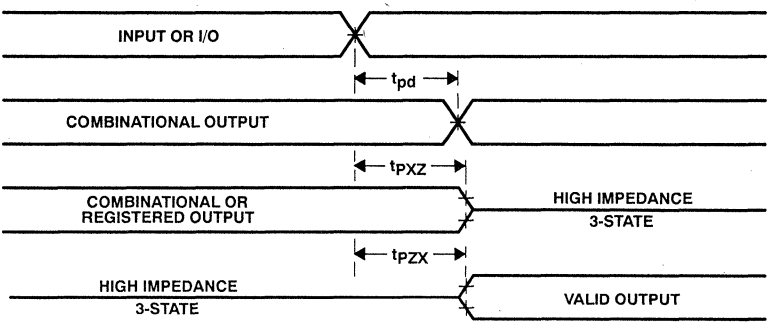
latchup

The EP330 input, I/O, and clock pins have been carefully designed to resist the latchup that is inherent in CMOS structures. The EP330 pins will not latch up for input voltages between –1 V and V_{CC} + 1 V with currents up to 250 mA. During transitions, the inputs may undershoot to –2 V for periods of less than 20 ns.

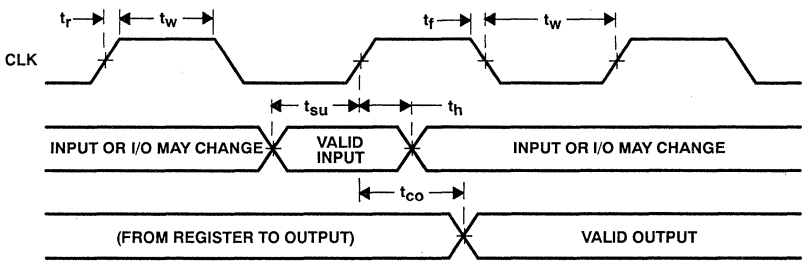
Although the programming pin (pin 11) is designed to resist latchup to the 13.5-V limit, during positive-current latch-up testing, the verify mode (pin 1) and program mode (pin 11) can be inadvertently entered into, causing current flow in the pins. This should not be construed as latchup.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



(a) Combinational Mode



(b) Synchronous Clock Mode

NOTES: A. Rise time (t_r) and fall time (t_f) < 3 ns.
B. t_w is measured at 0.3 V and 2.7 V. All other timing is measured at 1.5 V.
C. Input voltage levels at 0 V and 3 V.
D. Timing measurements are made from 2 V for a high level and 0.8 V for a low level to the 1.5 V level on the outputs.

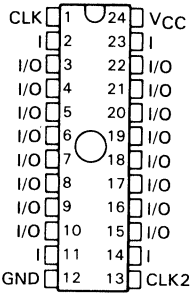
FIGURE 6. VOLTAGE WAVEFORMS

EP610
HIGH-PERFORMANCE 16-MACROCELL ERASABLE PROGRAMMABLE LOGIC DEVICE (EPLD)

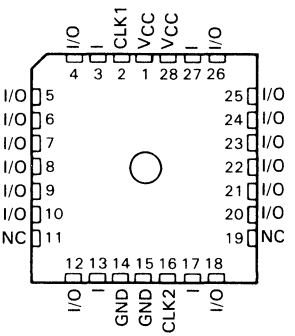
D3177, OCTOBER 1988 – AUGUST 1989

- High-Density (Over 600 Gates) Replacement for TTL and 74HC
- Virtually Zero Standby Power . . . Typ 20 µA
- High Speed:
  Propagation Delay Time . . . 25 ns
- Asynchronous Clocking of All Registers or Banked Register Operation from 2 Synchronous Clocks
- Sixteen Macrocells with Configurable I/O Architecture Allowing for Up to 20 Inputs and 16 Outputs
- Each Output Macrocell User-Programmable for D, T, SR, or JK Flip-Flops with Individual Clear Control or Combinational Operation
- UV-Light-Erasable Cell Technology Allows for:
  – Reconfigurable Logic
  – Reprogrammable Cells
  – Full Factory Testing for 100% Programming Yields
- Programmable Design Security Bit Prevents Copying of Logic Stored in Device
- Advanced Software Support Featuring Schematic Capture, Interactive Netlist, Boolean Equations, and State Machine Design Entry
- Package Options Include Plastic [for One-Time-Programmable (OTP) Devices] and Ceramic Dual-In-Line Packages and Chip Carriers

DUAL-IN-LINE PACKAGE
(TOP VIEW)



CHIP-CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PACKAGE TYPE			
		CERAMIC DUAL-IN-LINE PACKAGE (CDIP)	CERAMIC CHIP CARRIER (CLCC)	PLASTIC† DUAL-IN-LINE PACKAGE (PDIP)	PLASTIC† CHIP CARRIER (PLCC)
0°C – 70°C	25 ns	EP610DC-25	EP610JC-25	EP610PC-25	EP610LC-25
	30 ns	EP610DC-30	EP610JC-30	EP610PC-30	EP610LC-30
	35 ns	EP610DC-35	EP610JC-35	EP610PC-35	EP610LC-35
–40°C – 85°C	40 ns	EP610DI-40	EP610JI-40	EP610PI-40	EP610LI-40

†This package is for one-time-programmable (OTP) devices.

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description

general

The Texas Instruments EP610 Erasable Programmable Logic Device is capable of implementing over 600 equivalent gates of SSI and MSI logic functions all in plastic and ceramic space-saving 24-pin, 300-mil dual-in-line (DIP) packages and 28-pin chip-carrier packages. It uses the familiar sum-of-products logic, providing a programmable AND with a fixed OR structure. The device accommodates both combinational and sequential (registered) logic functions with up to 20 inputs and 16 outputs. The EP610 has a user programmable output logic macrocell that allows each output to be configured as a combinational or registered output and feedback signals active high or active low.

A unique feature of the EP610 is the ability to program D, T, SR, or JK flip-flop operation individually for each output without sacrificing product terms. In addition, each register can be individually clocked from any of the input or feedback paths available in the AND array. These features allow a variety of logic functions to be simultaneously implemented.

The CMOS EPROM technology reduces the power consumption to less than 20% of equivalent bipolar devices without sacrificing speed performance. Erasable EPROM bits allow for enhanced factory testing. Design changes can be easily implemented by erasing the device with ultraviolet (UV) light.

Programming the EP610 is accomplished by using the TI EPLD Development System, which supports four different design entry methods. When the design has been entered, the software performs automatic translation into logical equations, Boolean minimization, and design fitting directly into an EPLD.

functional

The EP610 is an Erasable Programmable Logic Device (EPLD) that uses a CMOS EPROM technology to implement logic designs in a programmable AND logic array. The device contains a revolutionary programmable I/O architecture that provides advanced functional capability for user programmable logic.

Externally, the EP610 provides 4 dedicated data inputs and 16 I/O pins, which may be configured for input, output, or bidirectional operation. Figure 1 shows the EP610 basic logic array macrocell. The internal architecture is organized with familiar sum-of-products (AND-OR) structure. Inputs to the programmable AND array come from true and complement signals from the 4 dedicated data inputs and the 16 I/O architecture-control blocks. The 40-input AND array encompasses 160 product terms, which are distributed among 16 available macrocells. Each EP610 product term represents a 40-input AND gate.

Each macrocell contains 10 product terms, 8 of which are dedicated for logic implementation. One product term is used for clear control of the macrocell internal register. The remaining product terms are used for output enable/asynchronous clock implementation.

There is an EPROM connection at the intersection point of each input signal and each product term. In the erased state, all connections are made. This means both the true and complement forms of all inputs are connected to each product term. Connections are opened during the programming process. Therefore, any product term may be connected to the true or complement form of any array input signal.

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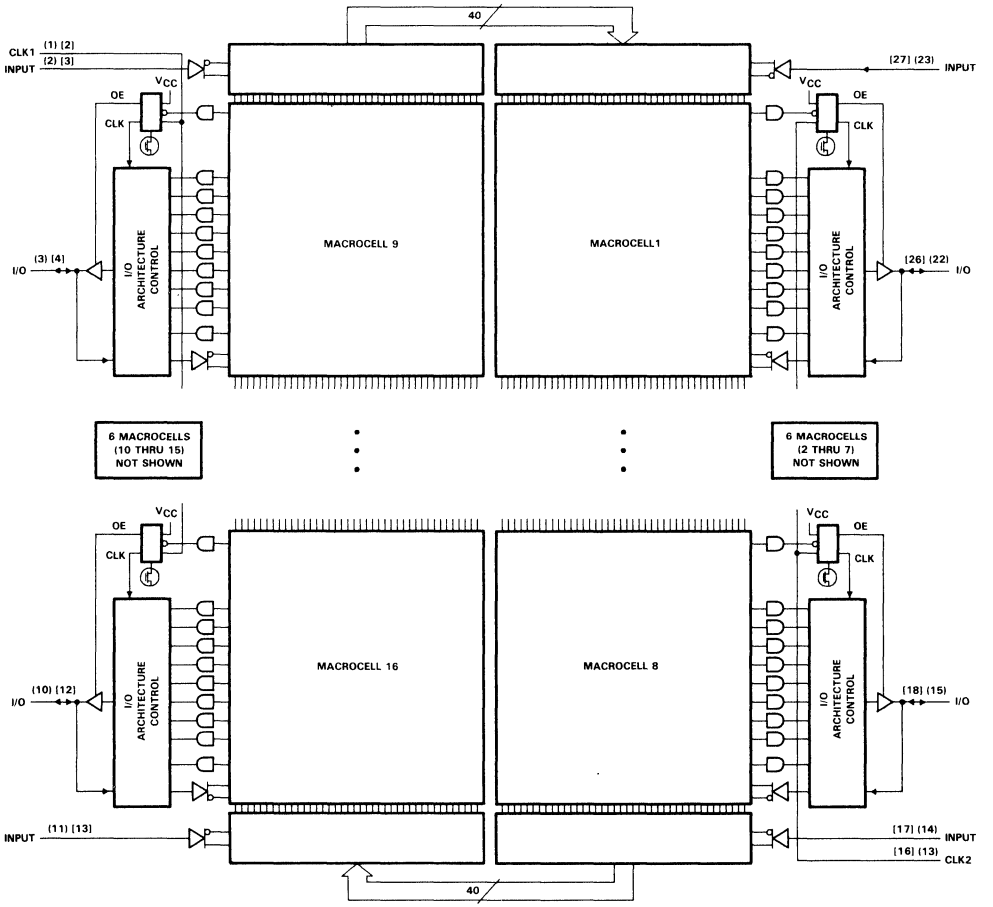
functional block diagram



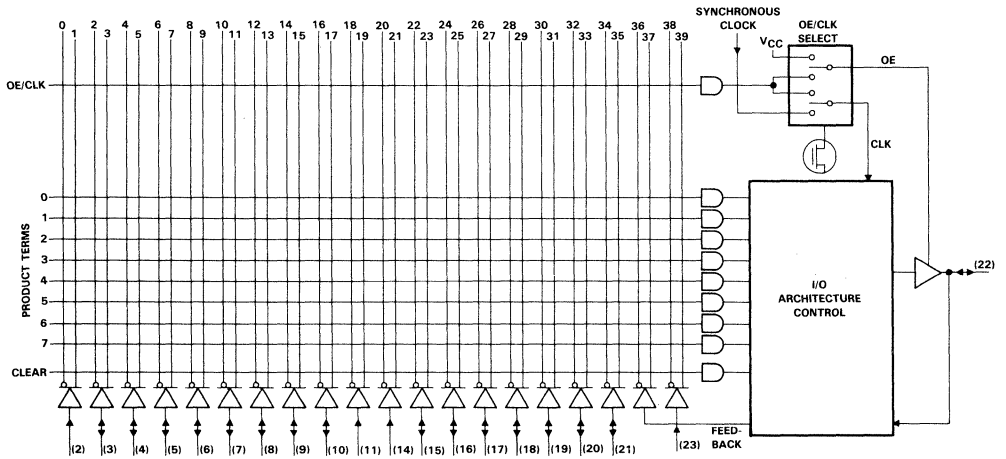
Pin numbers in ( ) are for DIP packages; pin numbers in [ ] are for chip-carrier packages.

When both the true and complement forms of any signal are left intact, a logical false state results on the output of the AND gate. If both the true and complement connections are open, then a logical "don't care" applies for that input. If all inputs for the product term are programmed open, then a logical true state results on the output of the AND gate.

Two dedicated clock inputs provide synchronous clock signals to the EP610 internal registers. Each of the clock signals controls a bank of 8 registers. CLK1 controls registers associated with macrocells 9-16, and CLK2 controls registers associated with macrocells 1-8. The EP610 advanced I/O architecture allows the number of synchronous registers to be user defined, from one to sixteen. Both dedicated clock inputs are positive-edge triggered.

I/O architecture

The EP610 input/output architecture provides each macrocell with over 50 possible I/O configurations. Each I/O can be configured for combinational or registered output, with programmable output polarity. Four different types of registers (D, T, JK, and SR) can be implemented into every I/O without any additional logic requirements. I/O feedback selection can also be programmed for registered or input (pin) feedback. Another benefit of the EP610 I/O architecture is its ability to individually clock each internal register from asynchronous clock signals.



Pin numbers are for dual-in-line packages.

FIGURE 1. LOGIC ARRAY MACROCELL (MACROCELL 1 ILLUSTRATED)

OE/CLK selection

Figure 2 shows the two modes of operation that are provided by the OE/CLK select multiplexer. The operation of this multiplexer is controlled by a single EPROM bit and may be individually configured for each EP610 I/O pin. In Mode 0, the 3-state output buffer is controlled by a single product term. If the output of the AND gate is true, the output buffer is enabled. If the output of the AND gate is false, the output buffer is in the high-impedance state. In this mode, the macrocell flip-flop may be clocked by its respective synchronous clock input. After erasure, the OE/CLK select multiplexer is configured in Mode 0.

In Mode 1, the output-enable buffer is always enabled. The macrocell flip-flop may now be triggered from an asynchronous clock signal generated by the OE/CLK multiplexable product term. This mode allows individual clocking of flip-flops from any available signal in the AND array. Because both true and complement signals reside in the AND array, the flip-flop may be configured for positive- or negative-edge-triggered operation. With the clock now controlled by a product term, gated clock structures are also possible.

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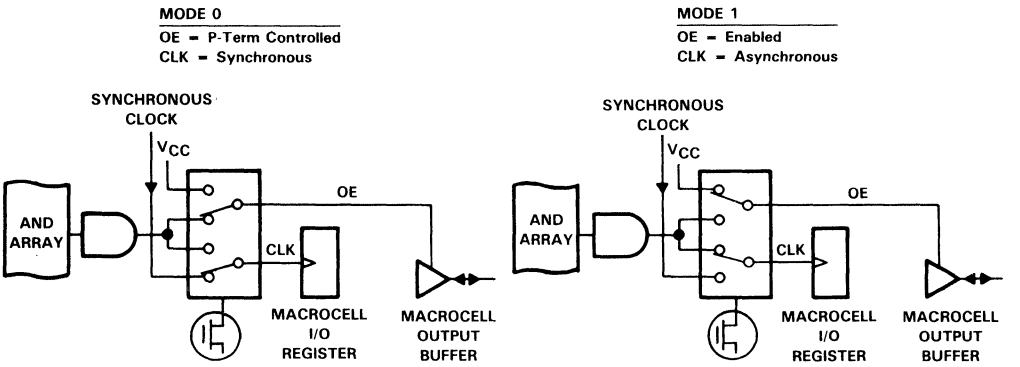


The register is clocked by the synchronous clock signal, which is common to 11 other Macrocells. The output is enabled by the logic from the product term.

The output is permanently enabled and the register is clocked via the product term. This allows for gated clocks that may be generated from elsewhere in the EP610.

FIGURE 2. OE/CLK SELECT MULTIPLEXER

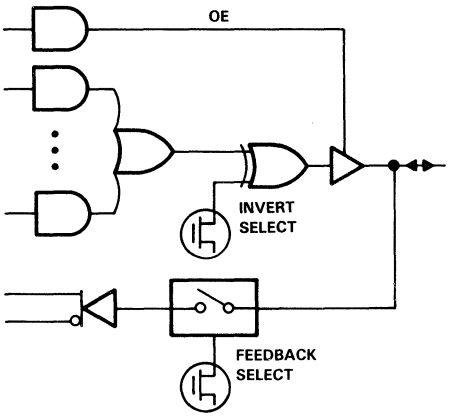
output/feedback selection

Figure 3 shows the EP610 basic output configurations. Along with combinational output, 4 register types are available. Each macrocell I/O may be independently configured. All registers have individual asynchronous clear control from a dedicated product term. When the product term is asserted, the macrocell register will immediately be loaded with a zero independently of the clock. On power-up, the EP610 performs the clear function automatically.

When the D or T register is selected, 8 product terms are ORed together and made available to the register input. The invert select EPROM bit determines output polarity. The feedback-select multiplexer enables register, I/O (pin), or no feedback to the AND array.

If the JK or SR registers are selected, the 8 product terms are shared between 2 OR gates. The allocation of product terms for each register input is optimized by the TI EPLD Development System. The invert select EPROM bit configures output polarity. The feedback-select multiplexer enables registered or no feedback to the AND array.

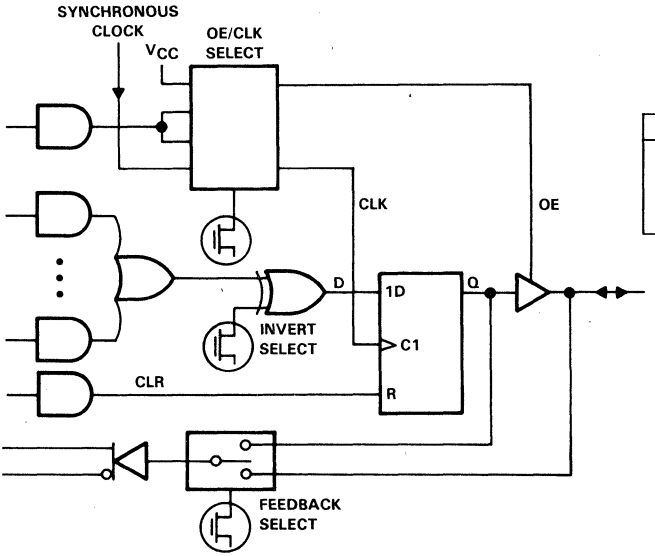
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback. No output is obtained by disabling the macrocell output buffer. In the erased state, each I/O is configured for combinational active-low output with input (pin) feedback.



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinational/high	Pin, None
Combinational/low	Pin, None
None	Pin

(a) COMBINATIONAL



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/high	JK Register, None
JK Register/low	JK Register, None
None	JK Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L or H	X	Q_0
H	X	X	L

(b) D-TYPE FLIP-FLOP

FIGURE 3. I/O CONFIGURATIONS

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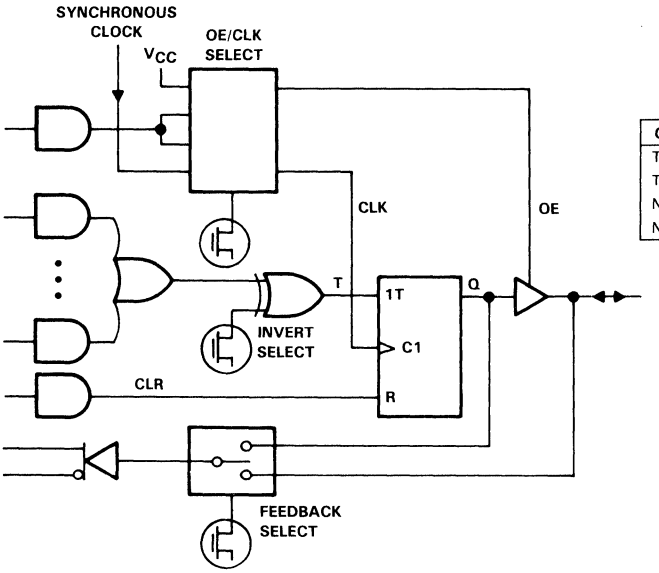


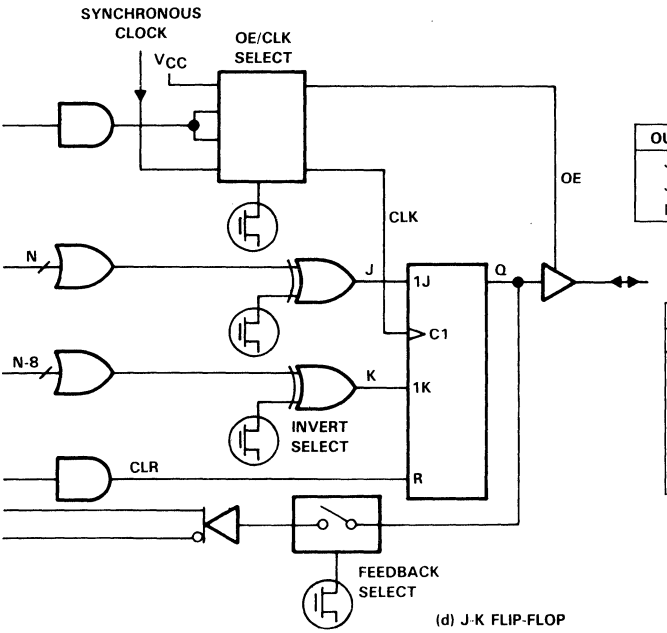
(c) TOGGLE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T Register/high	T Register, Pin, None
T Register/low	T Register, Pin, None
None	T Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	T	Q
L	↑	L	Q_0
L	↑	H	$\overline{Q}_0$
L	L or H	X	Q_0
H	X	X	L



(d) J-K FLIP-FLOP

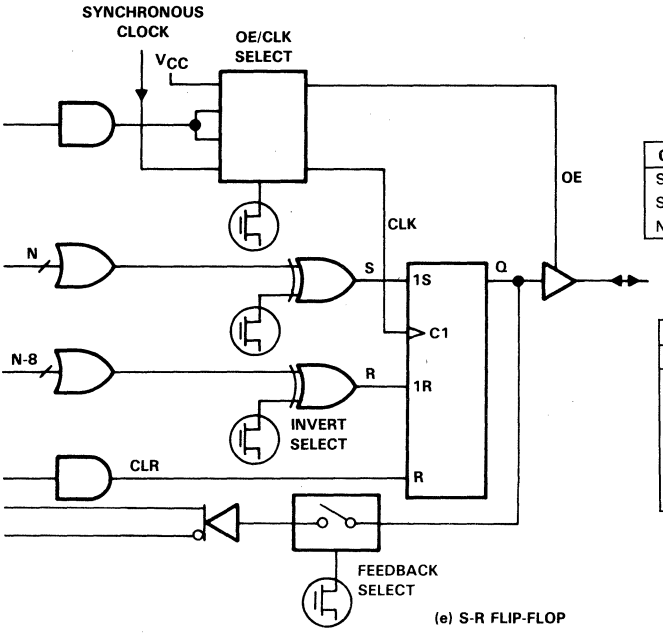
I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/high	JK Register, None
JK Register/low	JK Register, None
None	JK Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	J	K	Q
L	↑	L	L	Q_0
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	$\overline{Q}_0$
L	L or H	X	X	Q_0
H	X	X	X	L

FIGURE 3. I/O CONFIGURATIONS (CONTINUED)



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/high	SR Register, None
SR Register/low	SR Register, None
None	SR Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	S	R	Q
L	↑	L	L	Q_0
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	Undefined
L	L or H	X	X	Q_0
H	X	X	X	L

FIGURE 3. I/O CONFIGURATIONS (CONTINUED)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \leq 20$ ns) . . . . . −2 V to 7 V
Programming supply voltage range, V_{pp} . . . . . −0.3 V to 13.5 V
Instantaneous programming supply voltage range, V_{pp} ($t \leq 20$ ns) . . . . . −2 V to 13.5 V
Input voltage range, V_I . . . . . −0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \leq 20$ ns) . . . . . −2 V to 7 V
V_{CC} or GND current . . . . . −175 mA to 175 mA
Power dissipation at 25°C free-air temperature (see Note 2) . . . . . 1000 mW
Operating free-air temperature, T_A . . . . . −65°C to 135°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to GND terminal.
2. For operation above 25°C free-air temperature, derate to 120 mW at 135°C at the rate of 8.0 mW/°C.

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recommended operating conditions

PARAMETER			EP610I MIN	EP610I MAX	EP610C MIN	EP610C MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{IH}	High-level input voltage		2	$V_{CC}+0.3$	2	$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage (see Note 3)		−0.3	0.8	−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
t_r	Rise time	CLK input		100		250	ns
		Other inputs		250		500	
t_f	Fall time	CLK input		100		250	ns
		Other inputs		250		500	
T_A	Operating free-air temperature		−40	85	0	70	°C

Note 3: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

electrical charateristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		EP610I MIN	EP610I TYP†	EP610I MAX	EP610C MIN	EP610C TYP†	EP610C MAX	UNIT
V_{OH}	High-level output voltage	TTL	I_{OH} = −4 mA		2.4			2.4			V
		CMOS	I_{OH} = −2 mA		3.84			3.84			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA				0.45			0.45	V
I_I	Input current		$V_I = V_{CC}$ or GND				±10			±10	µA
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or GND				±10			±10	µA
I_{CC}	Supply current	Standby	$V_I = V_{CC}$ or GND, No load	See Note 4		0.02	0.15		0.02	0.1	mA
		Non-turbo		See Note 5		3	15		3	10	
		Turbo		See Note 5		32	75		32	60	
C_i	Input capacitance		V_I = 0, f = 1 MHz, T_A = 25°C				20			20	pF
C_o	Output capacitance		V_O = 0, f = 1 MHz, T_A = 25°C				20			20	pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz, T_A = 25°C				20			20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. When in the non-turbo mode, the device automatically goes into the standby mode approximately 100 ns after the last transition.
5. These parameters are measured with device programmed as a 16-bit counter and f = 1 MHz.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

combinational mode, turbo bit on

PARAMETER†		TEST CONDITIONS	EP610-25		EP610-30		EP610-35		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output	C_L = 35 pF		25		30		35	ns
t_{pd2}	I/O input to nonregistered output			27		32		37	ns
t_{PZX}	Input to output enable			25		30		35	ns
t_{PXZ}	Input to output disable	C_L = 5 pF, See Note 6		25		30		35	ns
t_{clr}	Asynchronous output clear time	C_L = 35 pF		27		32		37	ns
t_{io}	I/O input buffer delay			2		2		2	ns

combinational mode, turbo bit off

PARAMETER†		TEST CONDITIONS	EP610-25		EP610-30		EP610-35		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output	C_L = 35 pF		55		60		65	ns
t_{pd2}	I/O input to nonregistered output			57		62		67	ns
t_{PZX}	Input to output enable			55		60		65	ns
t_{PXZ}	Input to output disable	C_L = 5 pF, See Note 6		55		60		65	ns
t_{clr}	Asynchronous output clear time	C_L = 35 pF		57		62		67	ns
t_{io}	I/O input buffer delay			2		2		2	ns

synchronous clock mode

PARAMETER†		TEST CONDITIONS	EP610-25		EP610-30		EP610-35		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	See Note 7	47.6		41.7		37		MHz
t_{co1}	Clock to output delay time			15		17		20	ns
t_{cnt}	Minimum clock period (register feedback to register output)	See Note 5		25		30		35	ns
f_{cnt}	Maximum frequency with feedback	See Note 5	40		33.3		28.6		MHz

asynchronous clock mode

PARAMETER†			TEST CONDITIONS	EP610-25		EP610-30		EP610-35		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency		See Note 7	47.6		41.7		37		MHz
t_{aco1}	Clock to output delay time	Turbo bit on			27		32		37	ns
		Turbo bit off			57		62		67	
t_{acnt}	Minimum clock period (register feedback to register output)				25		30		35	ns
f_{acnt}	Maximum frequency with feedback			40		33.3		28.6		MHz

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 5. These parameters are measured with device programmed as a 16-bit counter and f = 1 MHz.
6. This is for an output voltage change of 500 mV.
7. The f_{max} values shown represent the highest frequency of operation without feedback.

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timing requirements over recommended ranges of supply voltage and free-air temperature

synchronous clock mode

PARAMETER†			TEST CONDITIONS	EP610-25		EP610-30		EP610-35		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Input setup time	Turbo bit on		21		24		27		ns
		Turbo bit off		51		54		57		
t_h	Input hold time			0		0		0		ns
t_{ch}	Clock high pulse duration			10		11		12		ns
t_{cl}	Clock low pulse duration			10		11		12		ns

asynchronous clock mode

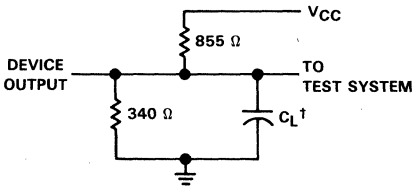
PARAMETER†			TEST CONDITIONS	EP610-25		EP610-30		EP610-35		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{asu}	Input setup time	Turbo bit on		8		8		8		ns
		Turbo bit off		38		38		38		
t_{ah}	Input hold time			12		12		12		ns
t_{ach}	Clock high pulse duration			10		11		12		ns
t_{acl}	Clock low pulse duration			10		11		12		ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

functional testing

The EP610 is functionally tested including complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield. As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP610 allows test program patterns to be used and then erased.

Figure 4 shows the test circuit and the conditions under which dynamic measurements are made. Because power supply transients can affect dynamic measurements, simultaneous transitions of multiple outputs should be avoided to ensure accurate measurement. The performance of threshold tests under dynamic conditions should not be attempted. Large-amplitude fast ground-current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground terminal and the test-system ground can create significant reductions in observable input noise immunity.



†Includes jig capacitance

FIGURE 4. DYNAMIC TEST CIRCUIT

design security

The EP610 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within the EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the device.

turbo bit

Some EPLDs contain a programmable option to control the automatic power-down feature that enables the low-standby-power mode of the device. This option is controlled by a turbo bit that can be set using the EPLD Development System. When the turbo bit is on, the low-standby-power mode is disabled. This renders the circuit less sensitive to V_{CC} noise transients created by the power-up/power-down cycle when operating in the low-power mode. The typical I_{CC} versus frequency data for both the turbo-bit-on mode and the turbo-bit-off (low-power) mode is shown in Figure 5. All dynamic parameters are tested with the turbo bit on. Figure 6 shows the relationship between the output drive currents and the corresponding output voltages.

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SUPPLY CURRENT
vs
MAXIMUM FREQUENCY

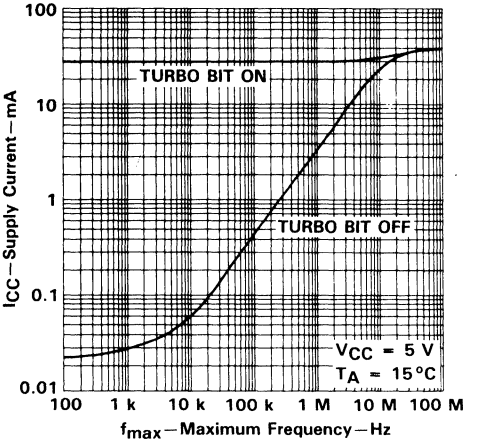


FIGURE 5

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

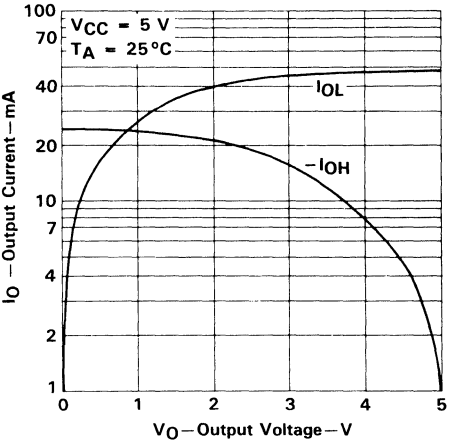
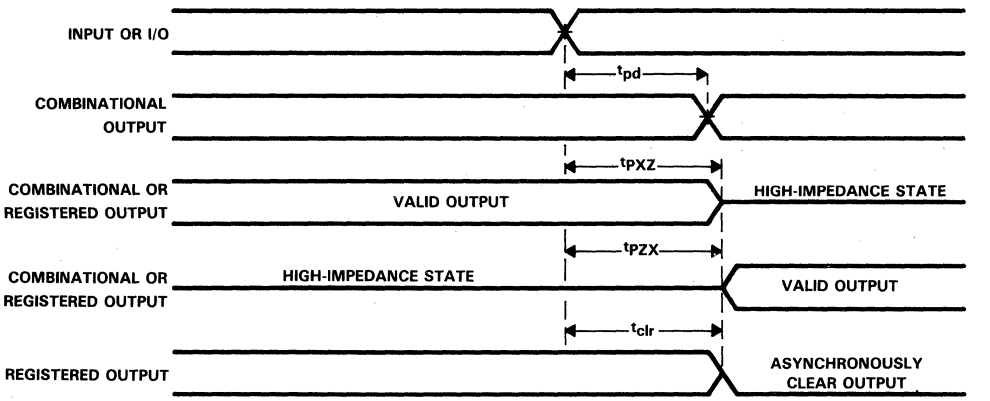
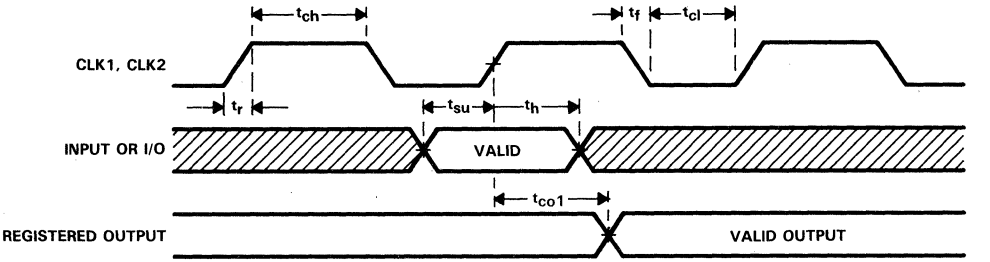


FIGURE 6

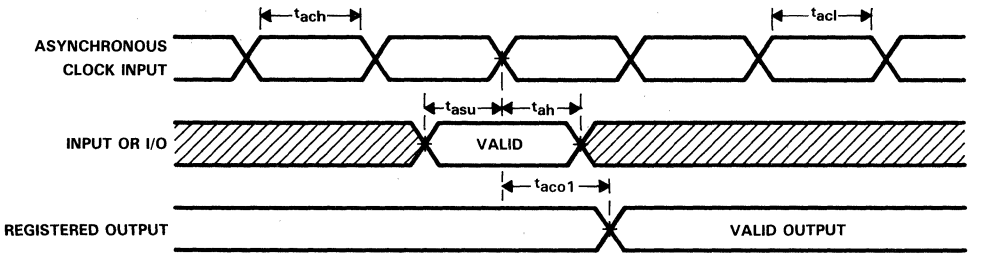
If the design requires low-power operation, the turbo bit should not be set. When operating in this mode, some dynamic parameters are subject to increases.



(a) COMBINATIONAL MODE



(b) SYNCHRONOUS CLOCK MODE



(c) ASYNCHRONOUS CLOCK MODE

FIGURE 7. SWITCHING WAVEFORMS

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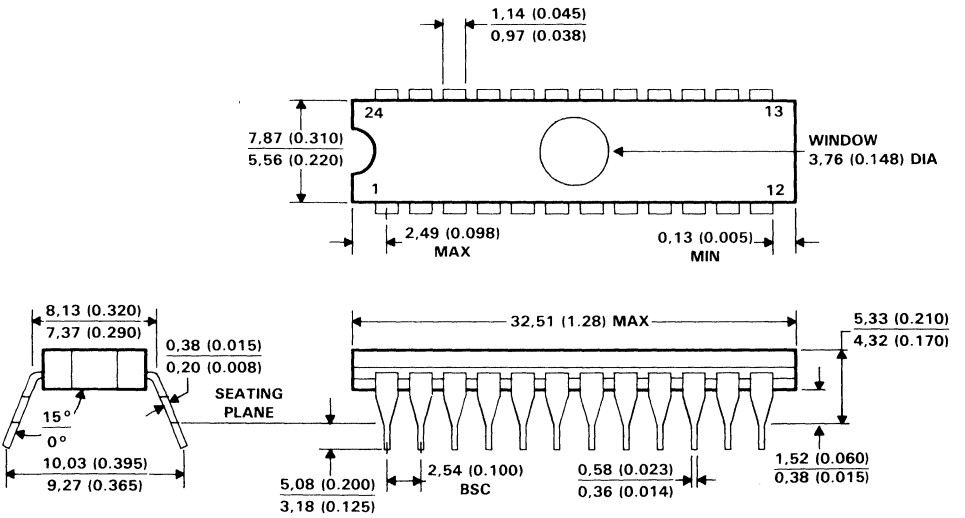
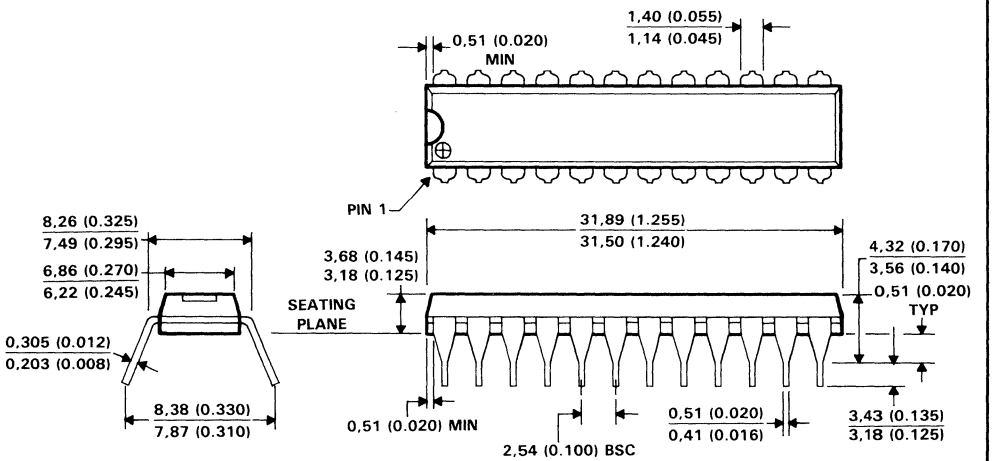
MECHANICAL DATA

24-PIN CERAMIC DIP (CDIP)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

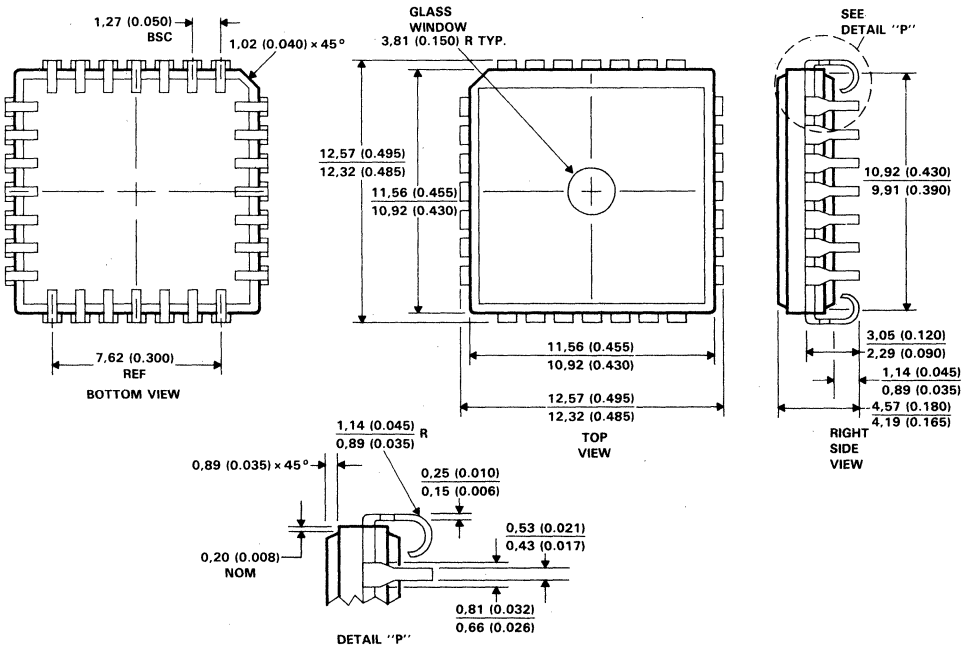
24-PIN DIP PLASTIC (PDIP)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

MECHANICAL DATA

28-PIN CERAMIC LEADED CHIP CARRIER (CLCC)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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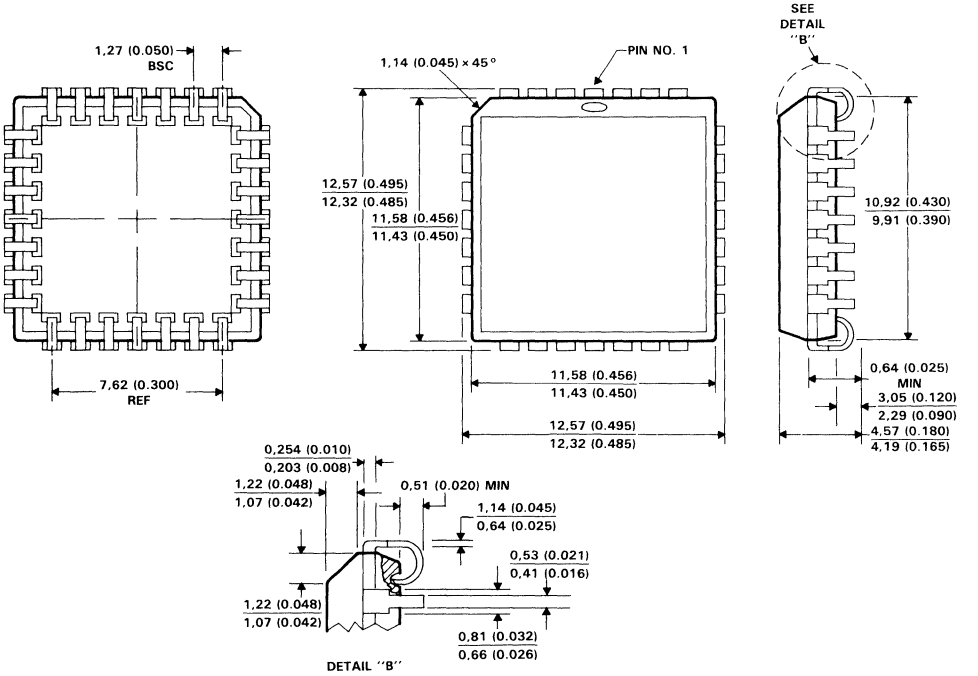
MECHANICAL DATA

28-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



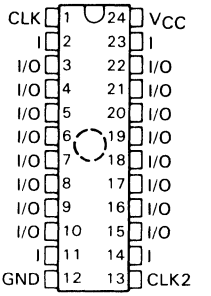
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

EP630
HIGH-PERFORMANCE 16-MACROCELL ERASABLE PROGRAMMABLE LOGIC DEVICE (EPLD)

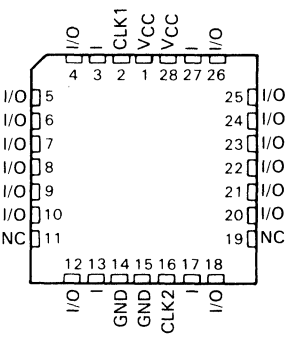
D3357, OCTOBER 1989

- High-Density (Over 600 Gates) Replacement for TTL and 74HC
- Low Operating Current:
  I_{CC} max . . . 100 mA
- High Speed:
  Propagation Delay Time . . . 20 ns
- Asynchronous Clocking of All Registers or Banked Register Operation from 2 Synchronous Clocks
- Sixteen Macrocells with Configurable I/O Architecture Allowing for up to 20 Inputs and 16 Outputs
- Each Output Macrocell User-Programmable for D, T, SR, or JK Flip-Flops with Individual Clear Control or Combinational Operation
- UV-Light-Erasable Cell Technology Allows for:
  - Reconfigurable Logic
  - Reprogrammable Cells
  - Full Factory Testing for 100% Programming Yields
- Programmable Design Security Bit Prevents Copying of Logic Stored in Device
- Advanced Software Support Featuring Schematic Capture, Interactive Netlist, Boolean Equations, and State Machine Design Entry
- Package Options Include Plastic [for One-Time-Programmable (OTP) Devices] and Ceramic Dual-In-Line Packages, Ceramic Quad Flat Packages, and Plastic Chip Carriers

JT OR NT PACKAGE
(TOP VIEW)



FZ OR FN PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PACKAGE TYPE			
		CERAMIC DUAL-IN-LINE (JT)	J-LEADED CERAMIC QUAD FLAT† (FZ)	PLASTIC† DUAL-IN-LINE (NT)	PLASTIC† CHIP CARRIER (FN)
0°C to 70°C	20	EP630-20CJT	EP630-20CFZ	EP630-20CNT	EP630-20CFN
−40°C to 85°C	25	EP630-25IJT	EP630-25IFZ	EP630-25INT	EP630-25IFN
−55°C to 125°C	25	EP630-25MJTB	EP630-25MFZB	N/A	N/A

† Contact factory for mechanical data on this package.

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TEXAS INSTRUMENTS
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description

general

The Texas Instruments EP630 Erasable Programmable Logic Device is capable of implementing over 600 equivalent gates of SSI and MSI logic functions all in plastic and ceramic space-saving 24-pin, 300-mil dual-in-line (DIP) packages and 28-pin chip-carrier packages. It uses the familiar sum-of-products logic, providing a programmable AND with a fixed OR structure. The device accommodates both combinational and sequential (registered) logic functions with up to 20 inputs and 16 outputs. The EP630 has a user programmable output logic macrocell that allows each output to be configured as a combinational or registered output and feedback signals active high or active low.

A unique feature of the EP630 is the ability to program D, T, SR, or JK flip-flop operation individually for each output without sacrificing product terms. In addition, each register can be individually clocked from any of the input or feedback paths available in the AND array. These features allow a variety of logic functions to be simultaneously implemented.

The CMOS EPROM technology reduces the power consumption to less than 55% of equivalent bipolar devices without sacrificing speed performance. Erasable EPROM bits allow for enhanced factory testing. Design changes can be easily implemented by erasing the device with ultraviolet (UV) light.

Programming the EP630 is accomplished by using the TI EPLD Development System, which supports four different design entry methods. When the design has been entered, the software performs automatic translation into logical equations, Boolean minimization, and design fitting directly into an EPLD.

functional

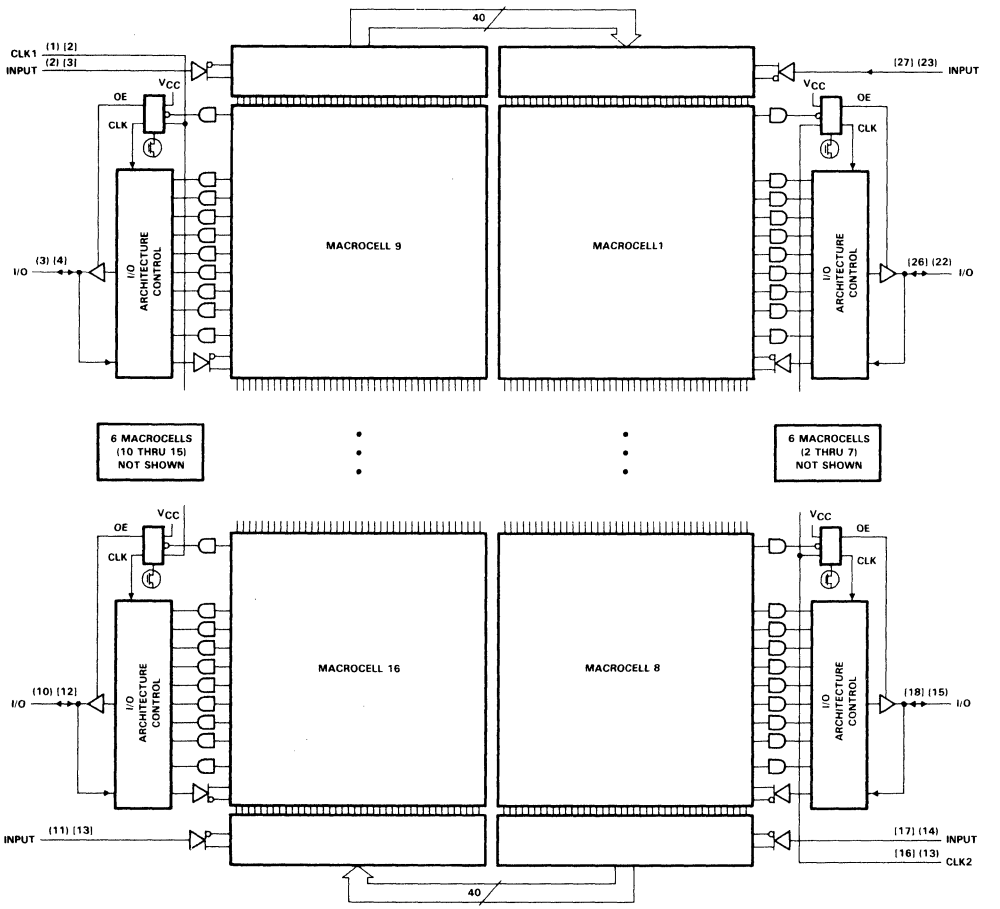
The EP630 is an Erasable Programmable Logic Device (EPLD) that uses a CMOS EPROM technology to implement logic designs in a programmable AND logic array. The device contains a revolutionary programmable I/O architecture that provides advanced functional capability for user programmable logic.

Externally, the EP630 provides 4 dedicated data inputs and 16 I/O pins, which may be configured for input, output, or bidirectional operation. Figure 1 shows the EP630 basic logic array macrocell. The internal architecture is organized with familiar sum-of-products (AND-OR) structure. Inputs to the programmable AND array come from true and complement signals from the 4 dedicated data inputs and the 16 I/O architecture-control blocks. The 40-input AND array encompasses 160 product terms, which are distributed among 16 available macrocells. Each EP630 product term represents a 40-input AND gate.

Each macrocell contains 10 product terms, 8 of which are dedicated for logic implementation. One product term is used for clear control of the macrocell internal register. The remaining product terms are used for output enable/asynchronous clock implementation.

There is an EPROM connection at the intersection point of each input signal and each product term. In the erased state, all connections are made. This means both the true and complement forms of all inputs are connected to each product term. Connections are opened during the programming process. Therefore, any product term may be connected to the true or complement form of any array input signal.

functional block diagram



Pin numbers in ( ) are for DIP packages; pin numbers in [ ] are for chip-carrier packages.

When both the true and complement forms of any signal are left intact, a logical false state results on the output of the AND gate. If both the true and complement connections are open, then a logical "don't care" applies for that input. If all inputs for the product term are programmed open, then a logical true state results on the output of the AND gate.

Two dedicated clock inputs provide synchronous clock signals to the EP630 internal registers. Each of the clock signals controls a bank of 8 registers. CLK1 controls registers associated with macrocells 9-16, and CLK2 controls registers associated with macrocells 1-8. The EP630 advanced I/O architecture allows the number of synchronous registers to be user defined, from one to sixteen. Both dedicated clock inputs are positive-edge-triggered.

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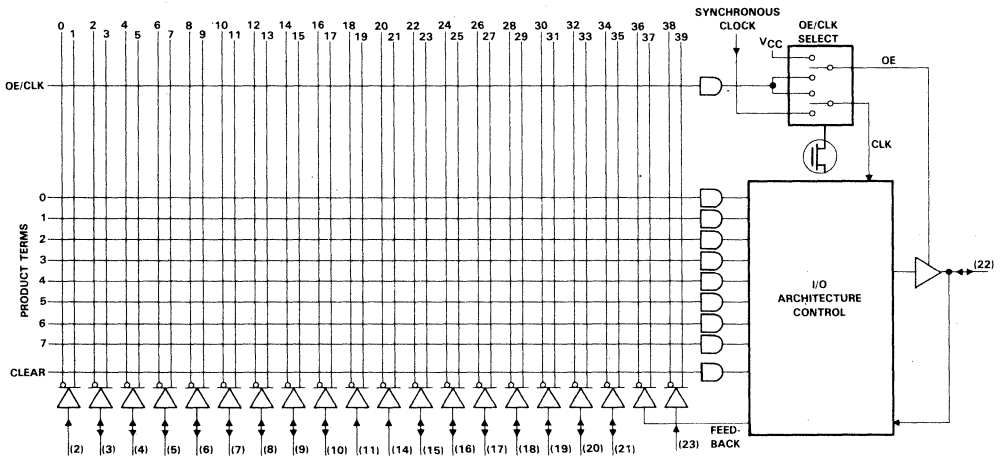
I/O architecture

The EP630 input/output architecture provides each macrocell with over 50 possible I/O configurations. Each I/O can be configured for combinational or registered output, with programmable output polarity. Four different types of registers (D, T, JK, and SR) can be implemented into every I/O without any additional logic requirements. I/O feedback selection can also be programmed for registered or input (pin) feedback. Another benefit of the EP630 I/O architecture is its ability to individually clock each internal register from asynchronous clock signals.



Pin numbers are for dual-in-line packages.

FIGURE 1. LOGIC ARRAY MACROCELL (MACROCELL 1 ILLUSTRATED)

OE/CLK selection

Figure 2 shows the two modes of operation that are provided by the OE/CLK select multiplexer. The operation of this multiplexer is controlled by a single EPROM bit and may be individually configured for each EP630 I/O pin. In Mode 0, the 3-state output buffer is controlled by a single product term. If the output of the AND gate is true, the output buffer is enabled. If the output of the AND gate is false, the output buffer is in the high-impedance state. In this mode, the macrocell flip-flop may be clocked by its respective synchronous clock input. After erasure, the OE/CLK select multiplexer is configured in Mode 0.

In Mode 1, the output-enable buffer is always enabled. The macrocell flip-flop may now be triggered from an asynchronous clock signal generated by the OE/CLK multiplexable product term. This mode allows individual clocking of flip-flops from any available signal in the AND array. Because both true and complement signals reside in the AND array, the flip-flop may be configured for positive- or negative-edge-triggered operation. With the clock now controlled by a product term, gated clock structures are also possible.

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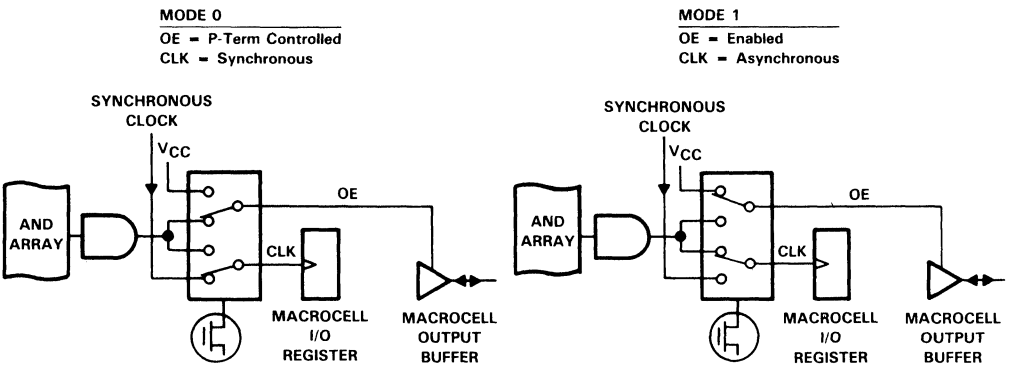


The register is clocked by the synchronous clock signal, which is common to 7 other Macrocells. The output is enabled by the logic from the product term.

The output is permanently enabled and the register is clocked via the product term. This allows for gated clocks that may be generated from elsewhere in the EP630.

FIGURE 2. OE/CLK SELECT MULTIPLEXER

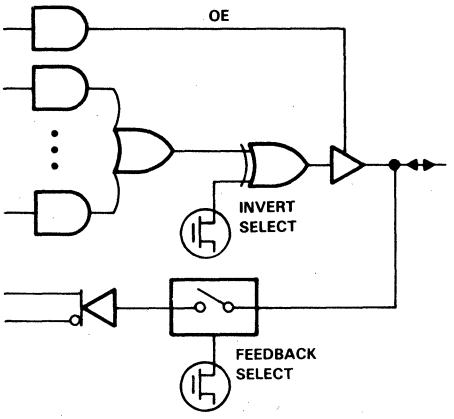
output/feedback selection

Figure 3 shows the EP630 basic output configurations. Along with combinational output, four register types are available. Each macrocell I/O may be independently configured. All registers have individual asynchronous clear control from a dedicated product term. When the product term is asserted, the macrocell register will immediately be loaded with a zero independently of the clock. On power-up, the EP630 performs the clear function automatically.

When the D or T register is selected, eight product terms are ORed together and made available to the register input. The invert select EPROM bit determines output polarity. The feedback-select multiplexer enables register, I/O (pin), or no feedback to the AND array.

If the JK or SR registers are selected, the eight product terms are shared between two OR gates. The allocation of product terms for each register input is optimized by the TI EPLD Development System. The invert select EPROM bit configures output polarity. The feedback-select multiplexer enables registered or no feedback to the AND array.

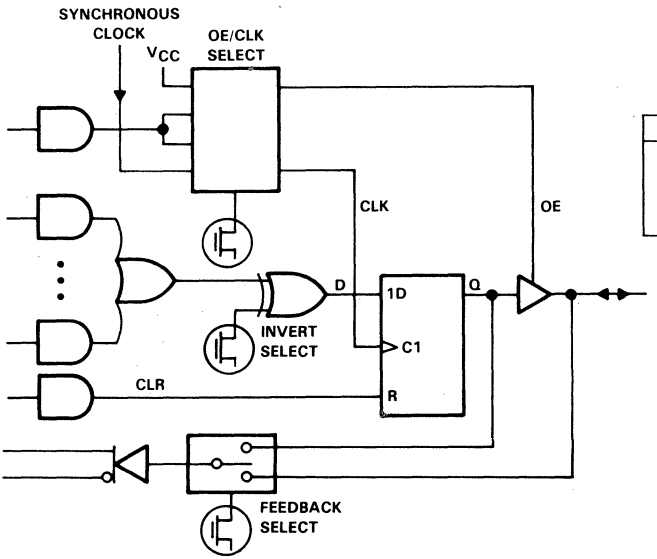
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback. No output is obtained by disabling the macrocell output buffer. In the erased state, each I/O is configured for combinational active-low output with input (pin) feedback.



(a) COMBINATIONAL

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinational/high	Pin, None
Combinational/low	Pin, None
None	Pin



(b) D-TYPE FLIP-FLOP

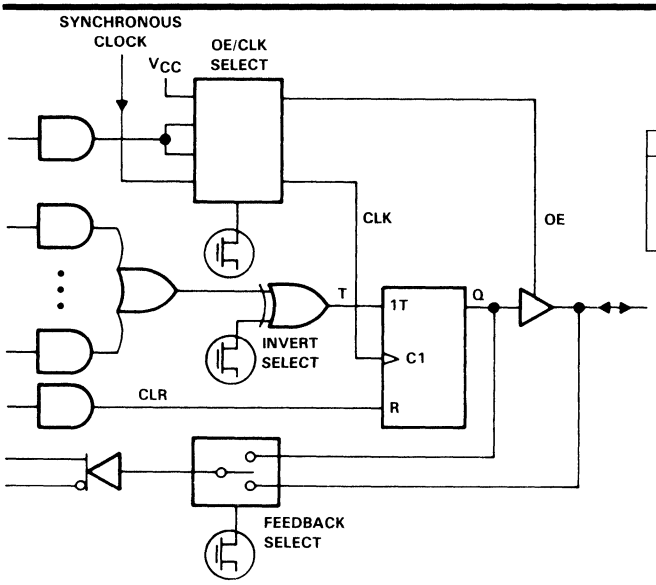
I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
D Register/high	D Register, Pin, None
D Register/low	D Register, Pin, None
None	D Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q_0
H	X	X	L

FIGURE 3. I/O CONFIGURATIONS



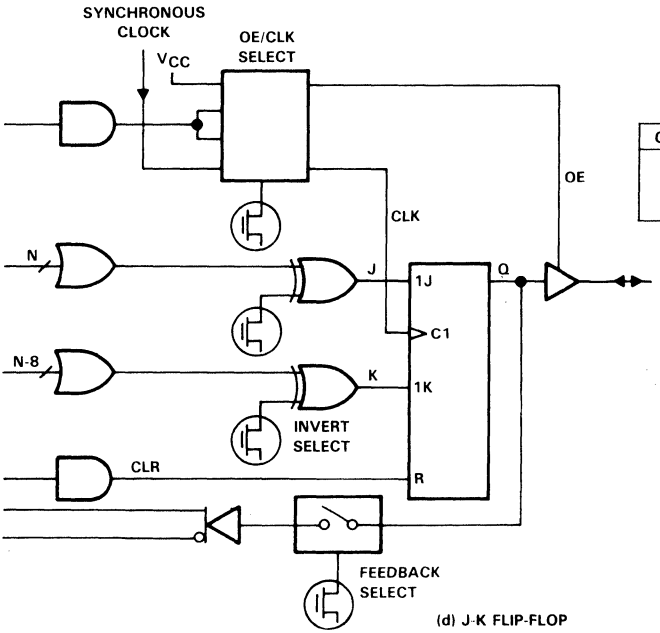
(c) TOGGLE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T Register/high	T Register, Pin, None
T Register/low	T Register, Pin, None
None	T Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	T	Q
L	↑	L	Q_0
L	↑	H	$\overline{Q}_0$
L	L	X	Q_0
H	X	X	L



(d) J-K FLIP-FLOP

I/O SELECTION

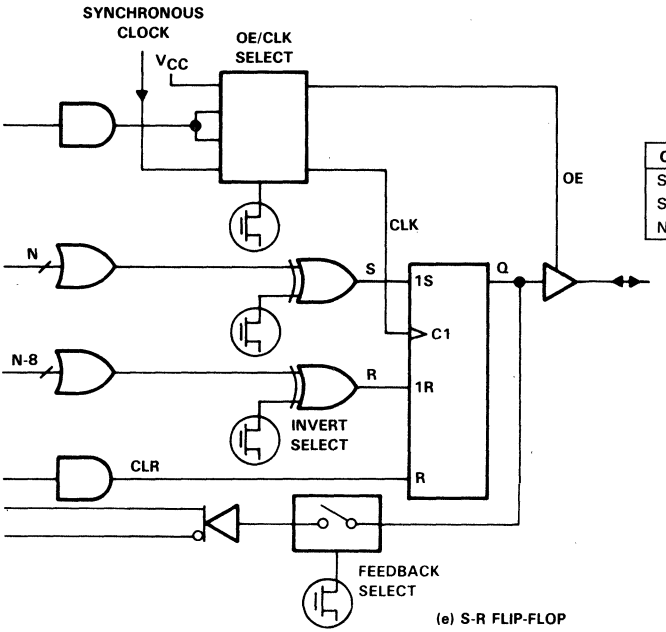
OUTPUT/POLARITY	FEEDBACK
JK Register/high	JK Register, None
JK Register/low	JK Register, None
None	JK Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	J	K	Q
L	↑	L	L	Q_0
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	$\overline{Q}_0$
L	L	X	X	Q_0
H	X	X	X	L

FIGURE 3. I/O CONFIGURATIONS (CONTINUED)

PRODUCT PREVIEW



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/high	SR Register, None
SR Register/low	SR Register, None
None	SR Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	S	R	Q
L	↑	L	L	Q_0
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	Undefined
L	L	X	X	Q_0
H	X	X	X	L

FIGURE 3. I/O CONFIGURATIONS (CONTINUED)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} (t ≤ 20 ns) . . . . . −2 V to 7 V
Programming supply voltage range, V_{PP} . . . . . −0.3 V to 13.5 V
Instantaneous programming supply voltage range, V_{PP} (t ≤ 20 ns) . . . . . −2 V to 13.5 V
Input voltage range, V_I . . . . . −0.3 V to 7 V
Instantaneous input voltage range, V_I (t ≤ 20 ns) . . . . . −2 V to 7 V
V_{CC} or GND current . . . . . −175 mA to 175 mA
Operating free-air temperature, T_A . . . . . −65°C to 135°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to GND terminal.

PRODUCT PREVIEW

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recommended operating conditions

PARAMETER			EP630-25M		EP630-25I		EP630-20C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	VCC	0	V_{CC}	V
V_{IH}	High-level input voltage		2	$V_{CC}+0.3$	2	$V_{CC}+0.3$	2	$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage (see Note 2)		−0.3	0.8	−0.3	0.8	−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
t_r	Rise time	CLK input		100		100		250	ns
		Other inputs		250		250		500	
t_f	Fall time	CLK input		100		100		250	ns
		Other inputs		250		250		500	
T_A	Operating free-air temperature		−55	125	−40	85	0	70	°C

Note 2: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical charateristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		EP6630-25M		EP630-20I		EP630-20C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	TTL	I_{OH} = −4 mA		2.4		2.4		2.4		V
		CMOS	I_{OH} = −2 mA		3.84		3.84		3.84		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.45		0.45		0.45	V
I_I	Input current		$V_I = V_{CC}$ or GND			±10		±10		±10	µA
I_{OZ}	Off-state output current		$V_O = V_{CC}$ or GND			±10		±10		±10	µA
I_{CC}	Supply current	Standby	$V_I = V_{CC}$ or GND, No load	See Note 3		150		150		150	µA
		Nonturbo		See Note 4		15		15		10	mA
		Turbo		See Note 4		150		150		100	
C_i	Input capacitance		V_I = 0, f = 1 MHz, T_A = 25°C			20		20		20	pF
C_o	Output capacitance		V_O = 0, f = 1 MHz, T_A = 25°C			20		20		20	pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz, T_A = 25°C			20		20		20	pF

NOTES: 3. When in nonturbo, the device automatically goes into the standby mode approximately 100 ns after the last transition.
4. These parameters are measured with the device programmed as a 16-bit counter and f = 1 MHz.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

combinational mode, turbo bit on

PARAMETER†		TEST CONDITIONS	EP630-25M		EP630-25I		EP630-20C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF		25		25		20	ns
t_{pd2}	I/O input to nonregistered output delay			27		27		22	ns
t_{PZX}	Output enable time			25		25		20	ns
t_{PXZ}	Output disable time	C_L = 5 pF, See Note 5		25		25		20	ns
t_{clr}	Asynchronous output clear time	C_L = 35 pF		30		30		25	ns
t_{io}	I/O input buffer delay			2		2		2	ns

combinational mode, turbo bit off

PARAMETER†		TEST CONDITIONS	EP630-25M		EP630-25I		EP630-20C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF		40		40		35	ns
t_{pd2}	I/O input to nonregistered output delay			42		42		37	ns
t_{PZX}	Output enable time			40		40		35	ns
t_{PXZ}	Output disable time	C_L = 5 pF, See Note 5		40		40		35	ns
t_{clr}	Asynchronous output clear time	C_L = 35 pF		45		45		40	ns
t_{io}	I/O input buffer delay			2		2		2	ns

synchronous clock mode

PARAMETER†		TEST CONDITIONS	EP630-25M		EP630-25I		EP630-20C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	See Note 6	50		50		55		MHz
t_{co1}	Clock to output delay time			18		18		15	ns
t_{cnt}	Minimum clock period (register feedback to register output)	See Note 4		25		25		20	ns
f_{cnt}	Maximum frequency with feedback	See Note 4	40		40		50		MHz

asynchronous clock mode

PARAMETER†			TEST CONDITIONS	EP630-25M		EP630-25I		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency		See Note 6	50						MHz
t_{aco1}	Clock to output delay time	Turbo bit on			30		30		25	ns
		Turbo bit off			45		45		40	
t_{acnt}	Minimum clock period (register feedback to register output)				25		25		20	ns
f_{acnt}	Maximum frequency with feedback			40		40		50		MHz

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 4. These parameters are measured with device programmed as a 16-bit counter and f = 1 MHz.
5. This is for an output voltage change of 500 mV.
6. The fmax values shown represent the highest frequency of operation without feedback.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and free-air temperature

synchronous clock mode

PARAMETER†			TEST CONDITIONS	EP630-25M		EP630-25I		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Input setup time	Turbo bit on		20		20		15		ns
		Turbo bit off		35		35		30		
t_h	Input hold time			0		0		0		ns
t_{ch}	Clock high pulse duration			10		10		9		ns
t_{cl}	Clock low pulse duration			10		10		9		ns

asynchronous clock mode

PARAMETER†			TEST CONDITIONS	EP630-25M		EP630-25I		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{asu}	Input setup time	Turbo bit on		10		10		8		ns
		Turbo bit off		25		25		23		
t_{ah}	Input hold time			15		15		12		ns
t_{ach}	Clock high pulse duration			10		10		9		ns
t_{acl}	Clock low pulse duration			10		10		9		ns

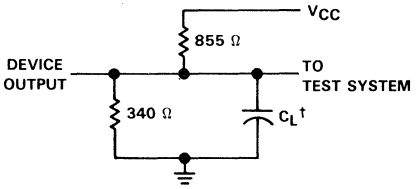
† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

PRODUCT PREVIEW

functional testing

The EP630 is functionally tested including complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield. As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP630 allows test program patterns to be used and then erased.

Figure 4 shows the test circuit and the conditions under which dynamic measurements are made. Because power supply transients can affect dynamic measurements, simultaneous transitions of multiple outputs should be avoided to ensure accurate measurement. The performance of threshold tests under dynamic conditions should not be attempted. Large-amplitude fast ground-current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground terminal and the test-system ground can create significant reductions in observable input noise immunity.



†Includes jig capacitance
Equivalent loads may be used for testing

FIGURE 4. DYNAMIC TEST CIRCUIT

design security

The EP630 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within the EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the device.

turbo bit

These EPLDs contain a programmable option to control the automatic power-down feature that enables the low-standby-power mode of the device. This option is controlled by a turbo bit that can be set using the EPLD Development System. When the turbo bit is on, the low-standby-power mode is disabled. This renders the circuit less sensitive to V_{CC} noise transients created by the power-up/power-down cycle when operating in the low-power mode. The typical I_{CC} versus frequency data for both the turbo-bit-on mode and the turbo-bit-off (low-power) mode is shown in Figure 5. All dynamic parameters are tested with the turbo bit on. Figure 6 shows the relationship between the output drive currents and the corresponding output voltages.

SUPPLY CURRENT
vs
MAXIMUM FREQUENCY

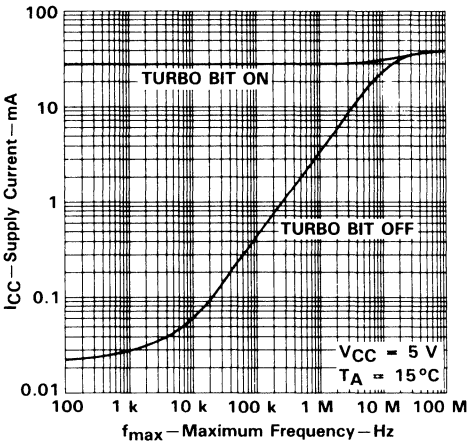


FIGURE 5

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

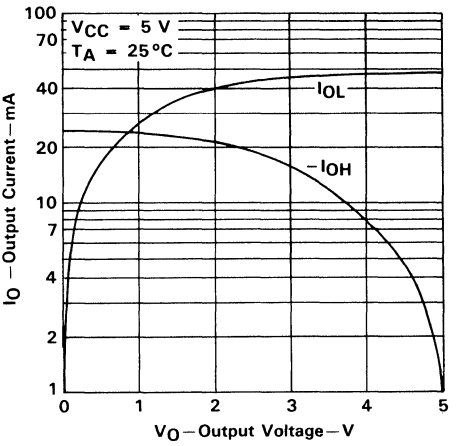
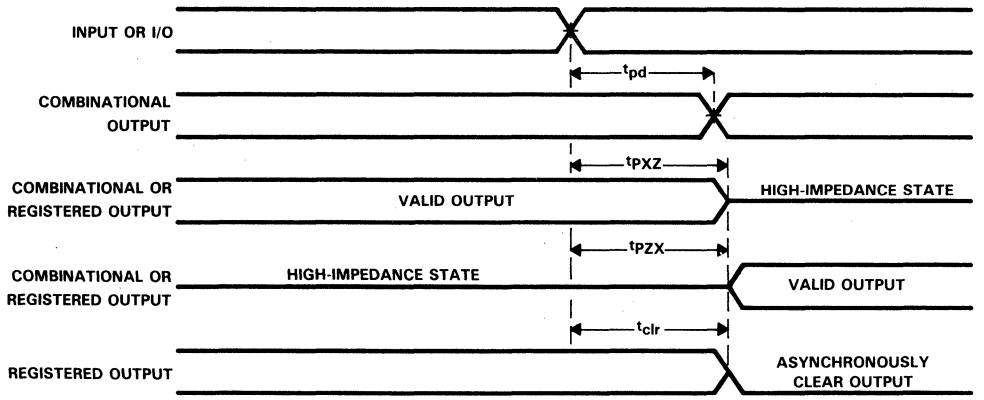


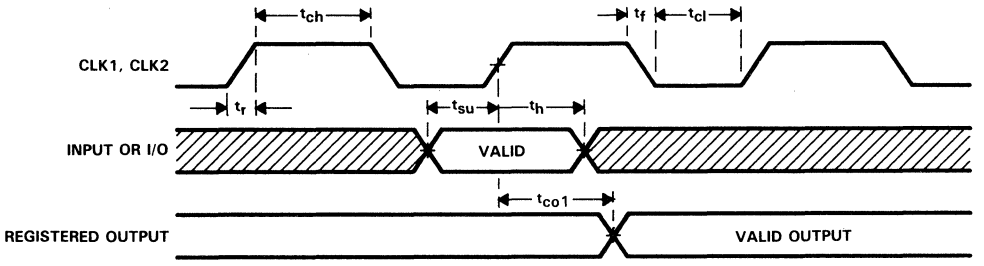
FIGURE 6

If the design requires low-power operation, the turbo bit should not be set. When operating in this mode, some dynamic parameters are subject to increases.

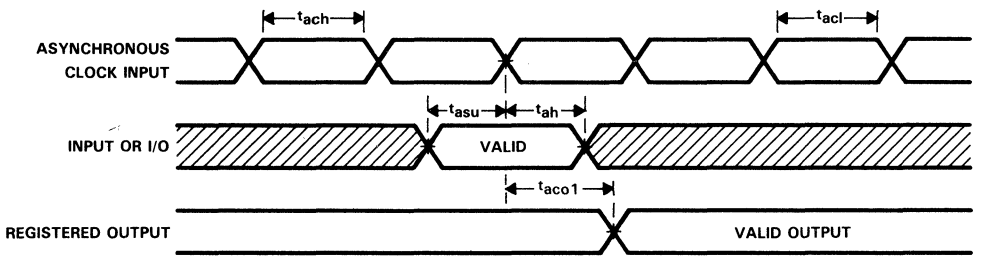
PRODUCT PREVIEW



(a) COMBINATIONAL MODE



(b) SYNCHRONOUS CLOCK MODE



(c) ASYNCHRONOUS CLOCK MODE

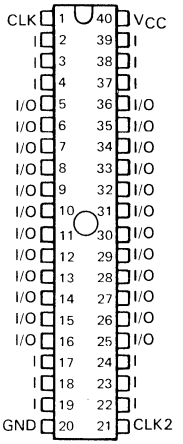
FIGURE 7. SWITCHING WAVEFORMS

EP910
HIGH-PERFORMANCE 24-MACROCELL ERASABLE PROGRAMMABLE LOGIC DEVICE (EPLD)

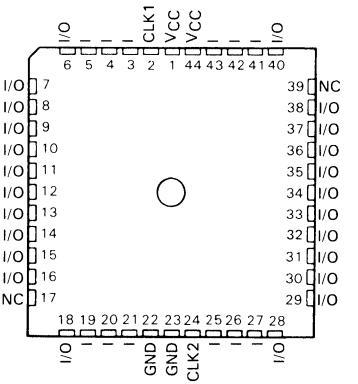
D3187, OCTOBER 1988 – REVISED AUGUST 1989

- High-Density (Over 900 Gates) Replacement for TTL and 74HC
- Virtually Zero Standby Power . . . Typ 20 μA
- High Speed:
  Propagation Delay Time . . . 30 ns
- Asynchronous Clocking of All Registers or Banked Register Operation from 2 Synchronous Clocks
- 24 Macrocells with Configurable I/O Architecture Allowing for Up to 36 Inputs and 24 Outputs
- Each Output Macrocell User-Programmable for D, T, SR, or JK Flip-Flops with Individual Clear Control or Combinational Operation
- UV-Light-Erasable Cell Technology Allows for:
  Reconfigurable Logic
  Reprogrammable Cells
  Full Factory Testing for 100% Programming Yields
- Programmable Design Security Bit Prevents Copying of Logic Stored in Device
- Advanced Software Support Featuring Schematic Capture, Interactive Netlist, Boolean Equations, and State Machine Design Entry
- Package Options Include Plastic [For One-Time-Programmable (OTP) Devices] and Ceramic Dual-In-Line Packages and J-Leaded Chip Carriers

DUAL-IN-LINE PACKAGE
(TOP VIEW)



CHIP-CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PACKAGE TYPE			
		CERAMIC DUAL-IN-LINE PACKAGE (CDIP)	CERAMIC CHIP CARRIER (CLCC)	PLASTIC† DUAL-IN-LINE PACKAGE (PDIP)	PLASTIC† CHIP CARRIER (PLCC)
0°C – 70°C	30 ns	EP910DC-30	EP910JC-30	EP910PC-30	EP910LC-30
	35 ns	EP910DC-35	EP910JC-35	EP910PC-35	EP910LC-35
	40 ns	EP910DC-40	EP910JC-40	EP910PC-40	EP910LC-40
−40°C – 85°C	45 ns	EP910DI-45	EP910JI-45	EP910PI-45	EP910LI-45

†This package is for One-Time-Programmable (OTP) devices.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description

general

The Texas Instruments EP910 Erasable Programmable Logic Device is capable of implementing over 900 equivalent gates of SSI and MSI logic functions accommodating up to 36 inputs and 24 outputs all in plastic and ceramic space-saving 40-pin, 600-mil dual-in-line (DIP) packages and 44-pin chip-carrier packages.

Each of the 24 macrocells contains a programmable-AND, fixed-OR PLA structure that yields 8 product terms for logic implementation and a single product term for output-enable and asynchronous-clear control functions. The architecture of the output logic macrocell allows the EP910 user to program output and feedback paths for both combinational or registered operation, active high or active low.

For increased flexibility, the EP910 also includes programmable registers. Each of the 24 internal registers may be programmed to be a D, T, SR, or JK flip-flop. In addition, each register may be clocked asynchronously on an individual basis or synchronously on a banked register basis.

In addition to density and flexibility, the performance characteristics allow the EP910 to be used in the widest possible range of applications. The CMOS EPROM technology reduces the power consumption to less than 20% of equivalent bipolar devices without sacrificing speed performance. Another advantage is 100% generic testing. The device can be erased with ultraviolet (UV) light. Design changes are no longer costly, nor is there a need for post-programming testing.

Programming the EP910 is accomplished by using the TI EPLD Development System, which supports four different design entry methods. When the design has been entered, the software performs automatic translation into logical equations, Boolean minimization, and design fitting directly into an EP910. The device may then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

functional

The EP910 is an Erasable Programmable Logic Device (EPLD) that uses a CMOS EPROM technology to implement logic designs in a programmable AND-logic array. The device also contains a revolutionary programmable I/O architecture that provides advanced functional capability for user programmable logic.

Externally, the EP910 provides 12 dedicated data inputs and 24 I/O pins, which may be configured for input, output, or bidirectional operation. Figure 1 shows the EP910 basic macrocell. The internal architecture is organized with the familiar sum-of-products (AND-OR) structure. Inputs to the programmable AND array come from the true and complement signal from 12 dedicated data inputs and 24 feedback signals originating from each of the 24 I/O architectural control blocks. The 72-input AND array encompasses 240 product terms, which are distributed among 24 available macrocells. Each EP910 product term represents a 72-input AND gate.

At the intersection point between each AND array input and each product term, there is an EPROM control cell. In the erased state, all connections are made. This means both the true and complement of all inputs are connected to each product term. Connections are opened during the programming process. Therefore, any product term may be connected to the true or complement form of any array input signal.

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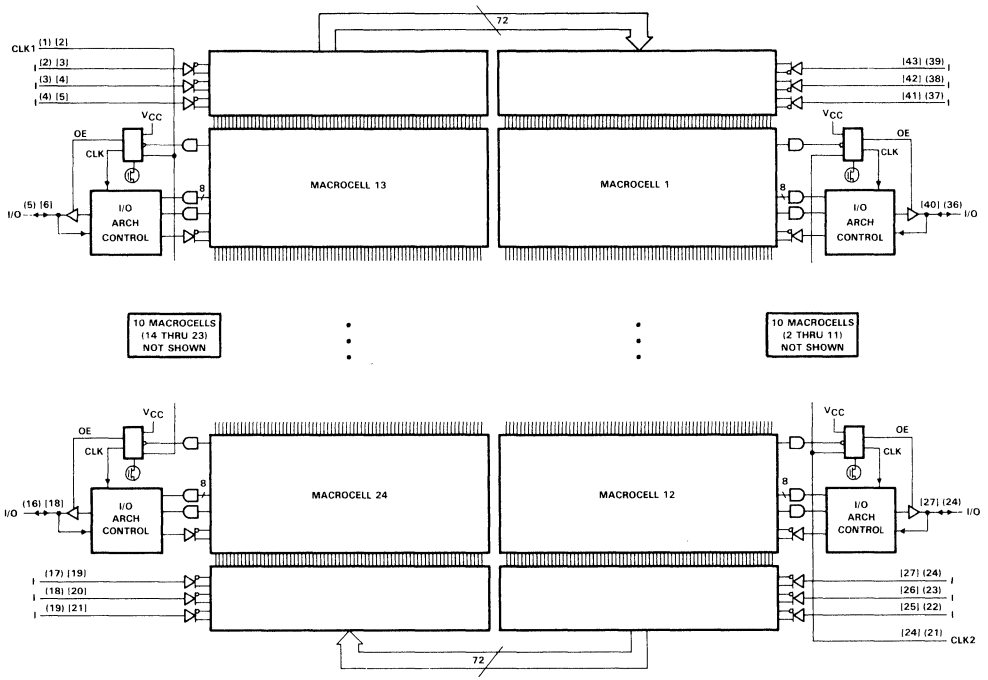
functional block diagram

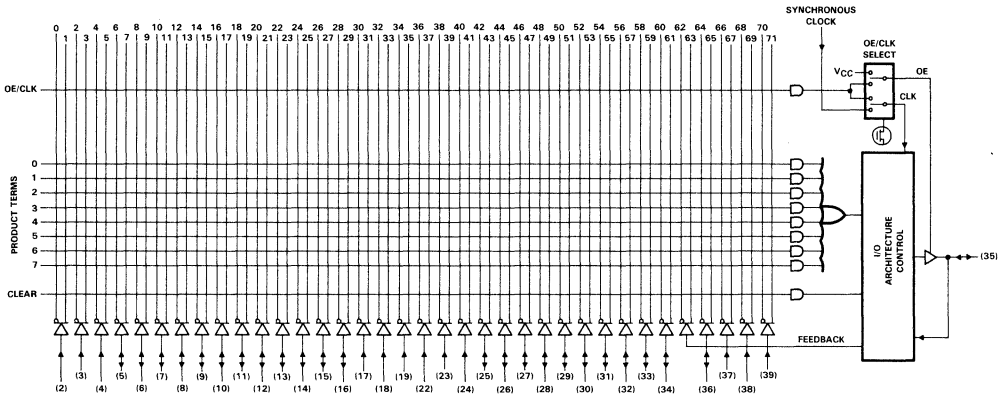


Pin numbers in parenthesis are for DIP packages. Pin numbers in brackets are for chip-carrier packages.

When both the true and complement of an array input signal are connected, a logical false results on the output of the AND gate. When both the true and complement forms of any array input signal are programmed open, then a logical "don't care" results for that input. If all 72 inputs for a given product term are programmed open, then a logical true state results on the output of the corresponding AND gate. Two dedicated clock inputs (not available in the AND array) provide the clock signals used for asynchronous clocking of the EP910 internal registers. Each of these clock signals is positive-edge triggered and has control over a bank of 12 registers. CLK1 controls registers associated with macrocells 13 through 24. CLK2 controls registers associated with macrocells 1 through 12. The EP910 advanced I/O architecture allows the number of synchronous registers to be user defined, from 1 to 24. Both dedicated clock inputs are positive-edge triggered.

I/O architecture

The EP910 input/output architecture provides each macrocell with over 50 possible I/O configurations. Each I/O can be configured for combinational or registered output, with programmable output polarity. Four different types of registers (D, T, JK, and SR) can be implemented into every I/O without any additional logic requirements. I/O feedback selection can also be programmed for registered or input (pin) feedback. Another benefit of the EP910 I/O architecture is its ability to individually clock each internal register from asynchronous clock signals.



Pin numbers shown are for dual-in-line packages.

FIGURE 1. LOGIC ARRAY MACROCELL (MACROCELL 1 ILLUSTRATED)

OE/CLK selection

Figure 2 shows the two modes of operation that are provided by the OE/CLK select multiplexer. The operation of this multiplexer is controlled by a single EPROM bit and may be individually configured for each of the EP910 I/O pins. In Mode 0, the 3-state output buffer is controlled by the OE/CLK product term. If the output of the AND gate is true, the output buffer is enabled. If the output of the AND gate is false, the output buffer is in the high-impedance state. In this mode, the macrocell flip-flop is clocked by its respective synchronous clock input signal (CLK1 or CLK2). After erasure, the OE/CLK select multiplexer is configured in Mode 0.

In Mode 1, the output-enable buffer is always enabled. The macrocell flip-flop may now be triggered from an asynchronous clock signal generated by the OE/CLK multiplexable product term. This mode allows individual clocking of flip-flops from any of the 72 available AND array input signals. Because both true and complement signals reside in the AND array, the flip-flop may be configured for positive- or negative-edge-triggered operation. With the clock now controlled by a product term, gated clock structures are also possible.

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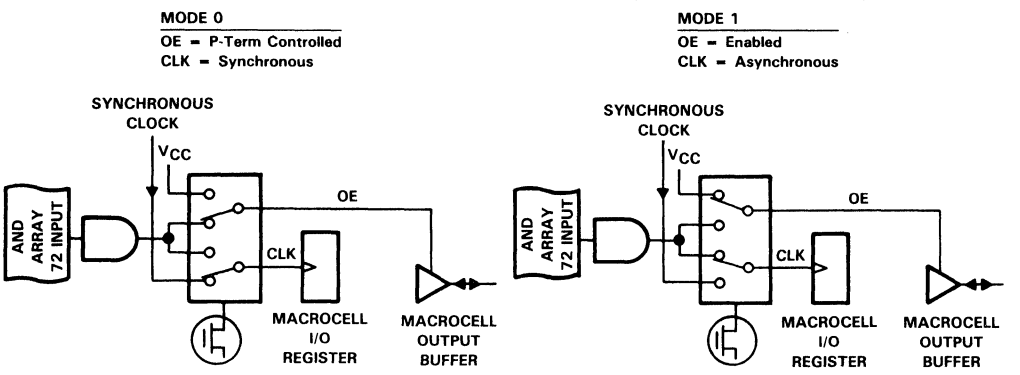


The register is clocked by the synchronous clock signal, which is common to 11 other Macrocells. The output is enabled by the logic from the product term.

The output is permanently enabled and the register is clocked via the product term. This allows for gated clocks that may be generated from elsewhere in the EP910.

FIGURE 2. OE/CLK SELECT MULTIPLEXER

output/feedback selection

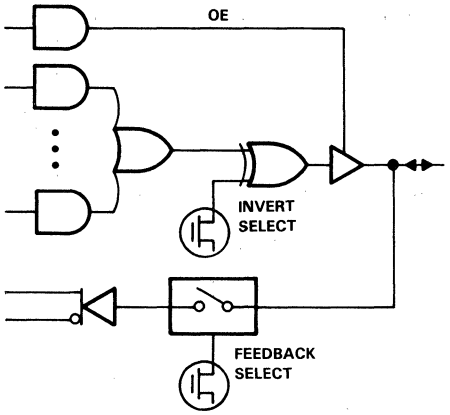
Figure 3 shows the EP910 basic output configurations. Along with combinational output, 4 register types are available. Each macrocell I/O may be independently configured. All registers have individual asynchronous-clear control from a dedicated product term. When the product term is asserted, the macrocell register will immediately be loaded with a zero independently of the clock. On power-up, the EP910 performs the clear function automatically.

In the combinational configuration, 8 product terms are ORed together to acquire the output signal. The invert-select EPROM bit controls output polarity and the output-enable buffer is product term controlled. The feedback-select multiplexer enables registered I/O (pin), feedback, or no feedback to the AND array.

When the D or T register is selected, 8 product terms are ORed together and made available to the register input. The invert select EPROM bit determines output polarity. The OE/CLK select multiplexer is used to configure the mode of operation to Mode 0 or Mode 1 (see Figure 2). The feedback-select multiplexer enables registered I/O (pin) or no feedback to the AND array.

If the JK or SR registers are selected, the 8 product terms are shared among two OR gates whose outputs feed the two primary register inputs. The allocation of product terms for each register input is optimized by the TI EPLD Development System. The invert select EPROM bit controls output polarity while the OE/CLK select multiplexer allows the mode of operation be Mode 0 or Mode 1. The feedback-select multiplexer enables registered I/O (pin) or no feedback to the AND array.

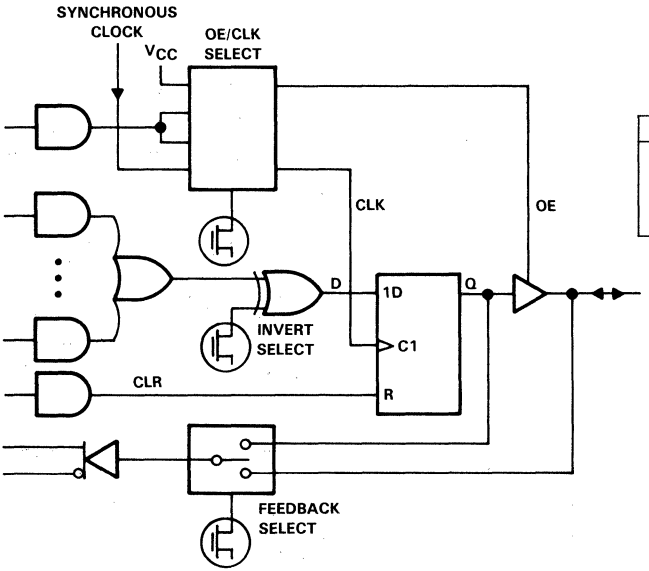
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback. No output is obtained by disabling the macrocell output buffer. In the erased state, I/O is configured for combinational active-low output with input (pin) feedback.



(a) COMBINATIONAL

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinational/high	Pin, None
Combinational/low	Pin, None
None	Pin



(b) D-TYPE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
D Register/high	D Register, Pin, None
D Register/low	D Register, Pin, None
None	D Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L or H	X	Q_0
H	X	X	L

FIGURE 3. I/O CONFIGURATIONS

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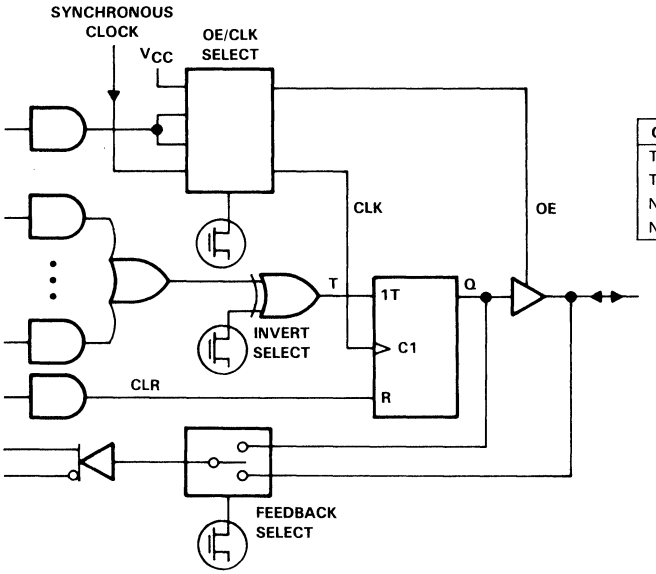


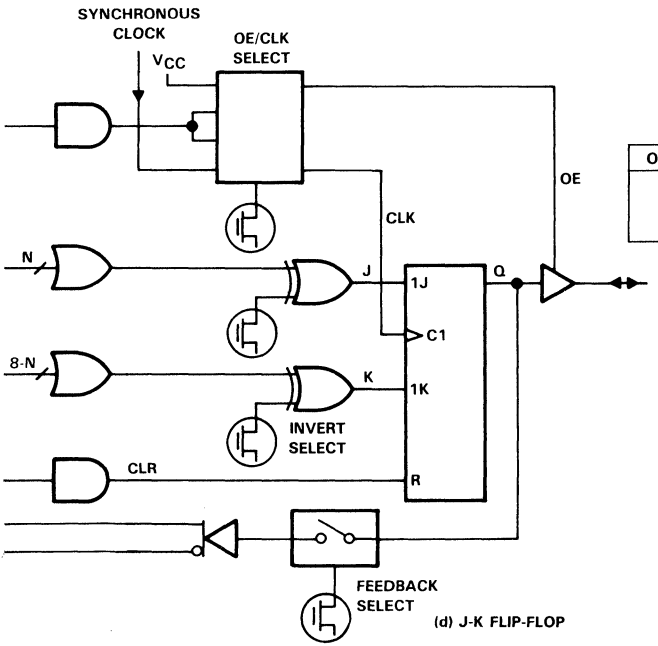
(c) TOGGLE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T Register/high	T Register, Pin, None
T Register/low	T Register, Pin, None
None	T Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	T	Q
L	↑	L	Q_0
L	↑	H	$\overline{Q}_0$
L	L or H	X	Q_0
H	X	X	L



(d) J-K FLIP-FLOP

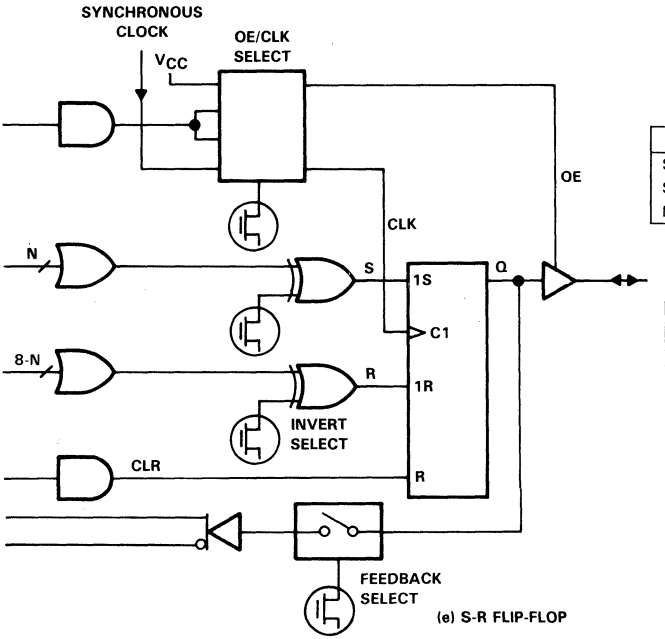
I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/high	JK Register, None
JK Register/low	JK Register, None
None	JK Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	J	K	Q
L	↑	L	L	Q_0
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	$\overline{Q}_0$
L	L or H	X	X	Q_0
H	X	X	X	L

FIGURE 3. I/O CONFIGURATIONS (CONTINUED)



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/high	SR Register, None
SR Register/low	SR Register, None
None	SR Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	S	R	Q
L	↑	L	L	Q_0
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	Undefined
L	L or H	X	X	Q_0
H	X	X	X	L

FIGURE 3. I/O CONFIGURATIONS (CONTINUED)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \leq 20$ ns) . . . . . −2 V to 7 V
Programming supply voltage range, V_{pp} . . . . . −0.3 V to 13.5 V
Instantaneous programming supply voltage range, V_{pp} ($t \leq 20$ ns) . . . . . −2 V to 13.5 V
Input voltage range, V_I . . . . . −0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \leq 20$ ns) . . . . . −2 V to 7 V
V_{CC} or GND current . . . . . −250 mA to 250 mA
Power dissipation at 25°C free-air temperature (see Note 2) . . . . . 1200 mW
Operating free-air temperature, T_A . . . . . −65°C to 135°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to GND terminal.
2. For operation above 25°C free-air temperature, derate to 144 mW at 135°C at the rate of 9.6 mW/°C.

recommended operating conditions

PARAMETER			EP910I		EP910C		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 3)		−0.3	0.8	−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
t_r	Rise time	CLK input		50		100	ns
		Other inputs		50		100	
t_f	Fall time	CLK input		50		100	ns
		Other inputs		50		100	
T_A	Operating free-air temperature		−40	85	0	70	°C

Note 3: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		EP910I			EP910C			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	TTL	I_{OH} = −4 mA		2.4			2.4			V
		CMOS	I_{OH} = −2 mA		3.84			3.84			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA				0.45			0.45	V
I_I	Input current		V_I = V_{CC} or GND				±10			±10	µA
I_{OZ}	Off-state output current		V_O = V_{CC} or GND				±10			±10	µA
I_{CC}	Supply current	Standby	V_I = V_{CC} or GND, No load	See Note 4		0.02	0.15		0.02	0.1	mA
		Non-turbo		See Note 5		6	30		6	20	
		Turbo		See Note 5		45	100		45	80	
C_i	Input capacitance		V_I = 0, f = 1 MHz, T_A = 25°C				20			20	pF
C_o	Output capacitance		V_O = 0, f = 1 MHz, T_A = 25°C				20			20	pF
C_{clk}‡	Clock capacitance		V_I = 0, f = 1 MHz, T_A = 25°C				20			20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ During programming, the clock capacitance of CLK2 is 60 pF maximum.
NOTES: 4. When in the non-turbo mode, the device automatically goes into the standby mode approximately 100 ns after the last transition.
5. These parameters are measured with device programmed as a 16-bit counter, and f = 1 MHz.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

combinational mode, turbo bit on

PARAMETER†		TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output	C_L = 35 pF		30		35		40	ns
t_{pd2}	I/O input to nonregistered output			33		38		43	ns
t_{PZX}	Input to output enable			30		35		40	ns
t_{PXZ}	Input to output disable	C_L = 5 pF, See Note 6		30		35		40	ns
t_{clr}	Asynchronous output clear time	C_L = 35 pF		33		38		43	ns
t_{io}	I/O input buffer delay			3		3		3	ns

combinational mode, turbo bit off

PARAMETER†		TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output	C_L = 35 pF		60		65		70	ns
t_{pd2}	I/O input to nonregistered output			63		68		73	ns
t_{PZX}	Input to output enable			60		65		70	ns
t_{PXZ}	Input to output disable	C_L = 5 pF, See Note 6		60		65		70	ns
t_{clr}	Asynchronous output clear time	C_L = 35 pF		63		68		73	ns
t_{io}	I/O input buffer delay			3		3		3	ns

synchronous clock mode

PARAMETER†		TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	See Note 7	41.7		37		32.3		MHz
t_{co1}	Clock to output delay time			18		21		24	ns
t_{cnt}	Minimum clock period (register feedback to register output)	See Note 5		30		35		40	ns
f_{cnt}	Maximum frequency with feedback	See Note 5	33.3		28.6		25		MHz

asynchronous clock mode

PARAMETER†			TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency		See Note 7	33.3		31.3		29.4		MHz
t_{aco1}	Clock to output delay time	Turbo bit on			33		38		43	ns
		Turbo bit off			63		68		73	
t_{acnt}	Minimum clock period (register feedback to register output)				30		35		40	ns
f_{cnt}	Maximum frequency with feedback			33.3		28.6		25		MHz

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 5. These parameters are measured with device programmed as a 16-bit counter, and f = 1 MHz.
6. This is for an output voltage change of 500 mV.
7. The f_{max} values shown represent the highest frequency of operation without feedback.

timing requirements over recommended ranges of supply voltage and free-air temperature

synchronous clock mode

PARAMETER†			TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Input setup time	Turbo bit on		24		27		31		ns
		Turbo bit off		54		57		61		
t_h	Input hold time			0		0		0		ns
t_{ch}	Clock high pulse duration			12		13		15		ns
t_{cl}	Clock low pulse duration			12		13		15		ns

asynchronous clock mode

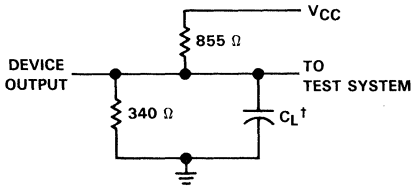
PARAMETER†			TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{asu}	Input setup time	Turbo bit on		10		10		10		ns
		Turbo bit off		40		40		40		
t_{ah}	Input hold time			15		15		15		ns
t_{ach}	Clock high pulse duration			15		16		17		ns
t_{acl}	Clock low pulse duration			15		16		17		ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

functional testing

The EP910 is functionally tested including complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield. As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP910 allows test program patterns to be used and then erased.

Figure 4 shows the dynamic test circuit and the conditions under which dynamic measurements are made. Because power supply transients can affect dynamic measurments, simultaneous transitions of multiple outputs should be avoided to ensure accurate measurement. The performance of threshold tests under dynamic conditions should not be attempted. Large-amplitude fast-ground-current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground terminal and the test-system ground can create significant reductions in observable input noise immunity.



†Includes jig capacitance

FIGURE 4. DYNAMIC TEST CIRCUIT

design security

The EP910 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within the EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the device.

turbo bit

Some EPLDs contain a programmable option to control the automatic power-down feature that enables the low-standby-power mode of the device. This option is controlled by a turbo bit that can be set using the TI EPLD Development System. When the turbo bit is on, the low-standby-power mode is disabled. This renders the circuit less sensitive to V_{CC} noise transients created by the power-up/power-down cycle when operating in the low-power mode. The typical I_{CC} versus frequency data for both the turbo-bit-on mode and the turbo-bit-off (low power) mode is shown in Figure 5. All dynamic parameters are tested with the turbo bit on. Figure 6 shows the relationship between the output drive currents and the corresponding output voltages.

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SUPPLY CURRENT
vs
MAXIMUM FREQUENCY

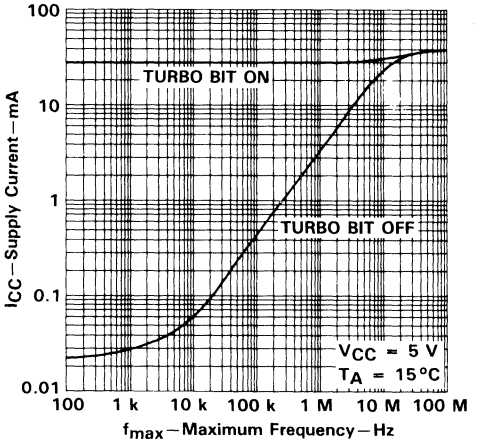


FIGURE 5

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

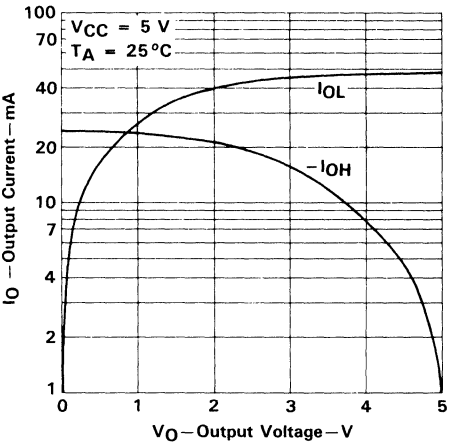
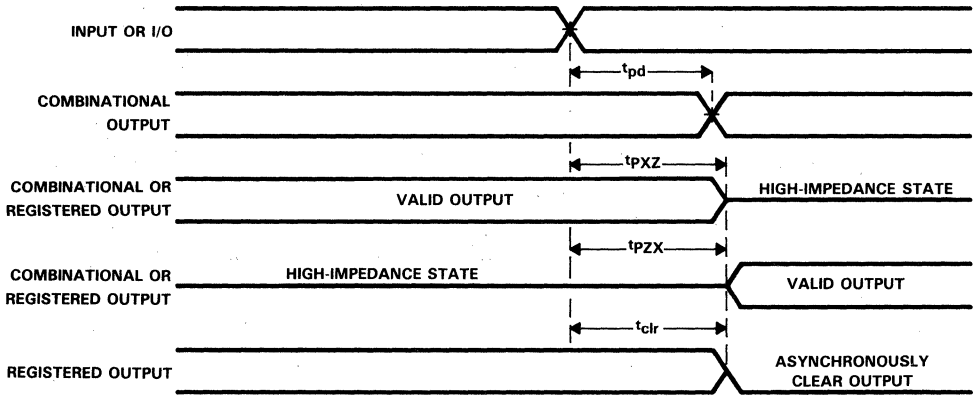
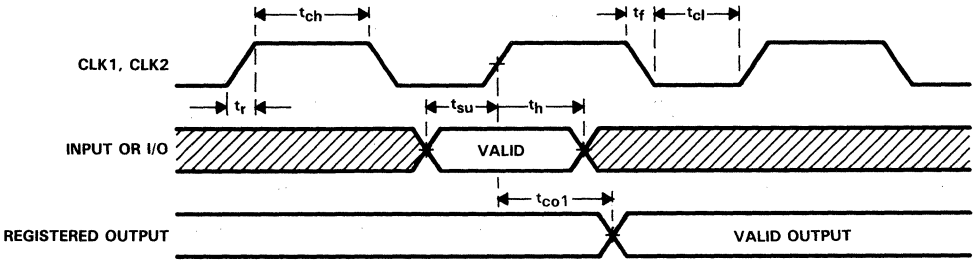


FIGURE 6

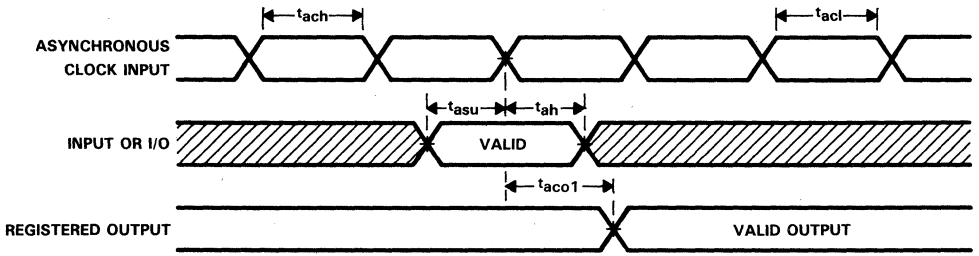
If the design requires low-power operation, the turbo bit should be (disabled) off. When operating in this mode, some dynamic parameters are subject to increases.



(a) COMBINATIONAL MODE



(b) SYNCHRONOUS CLOCK MODE



(c) ASYNCHRONOUS CLOCK MODE

FIGURE 7. SWITCHING WAVEFORMS

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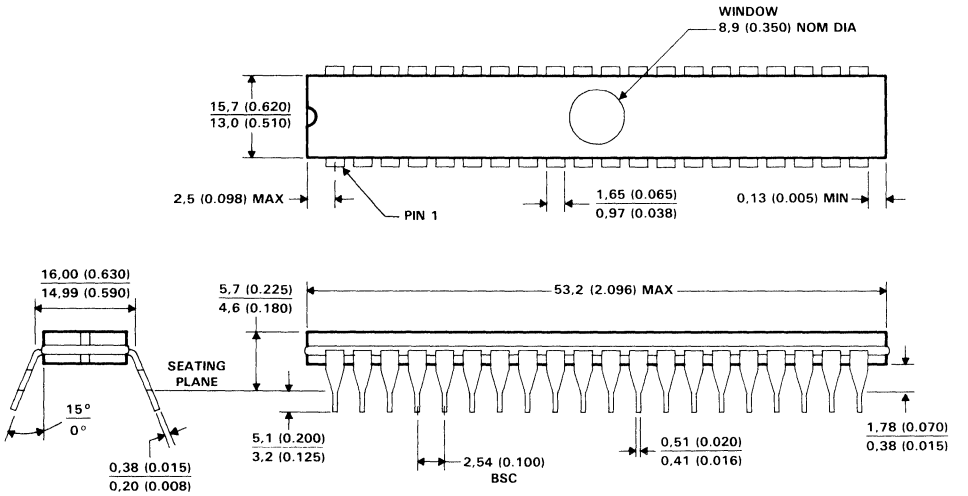
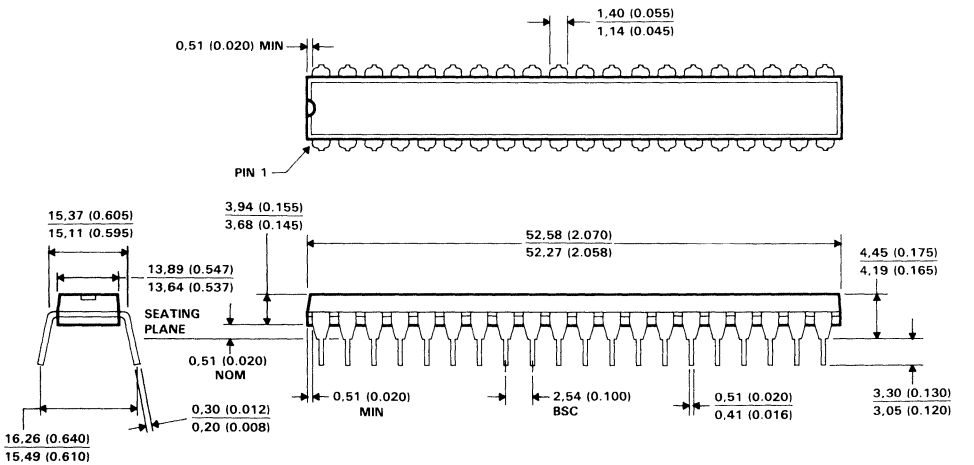
MECHANICAL DATA

40-PIN CERAMIC DIP (CDIP)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

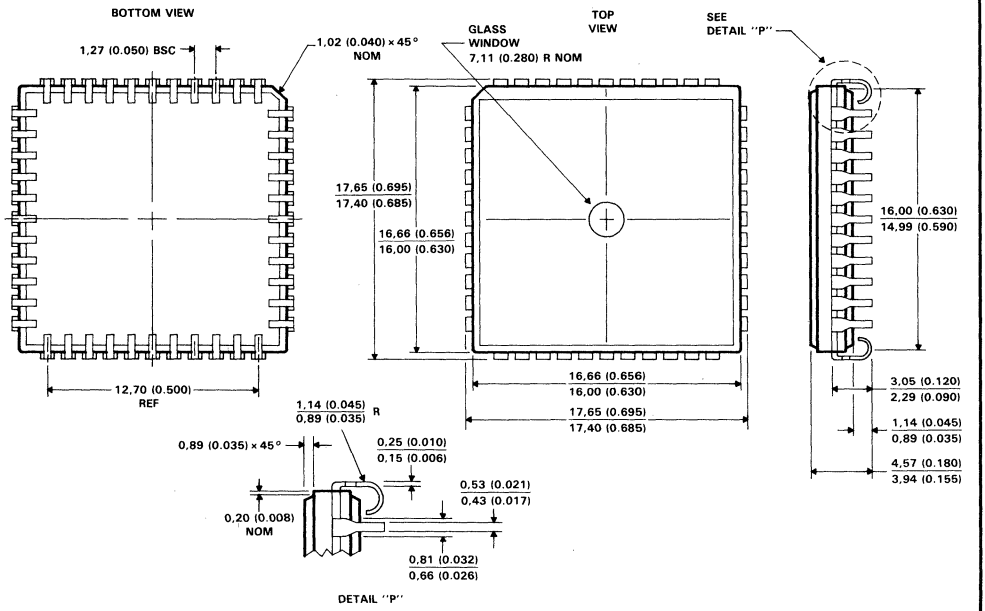
40-PIN PLASTIC DIP (PDIP)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

MECHANICAL DATA

44-PIN CERAMIC LEADED CHIP CARRIER (CLCC)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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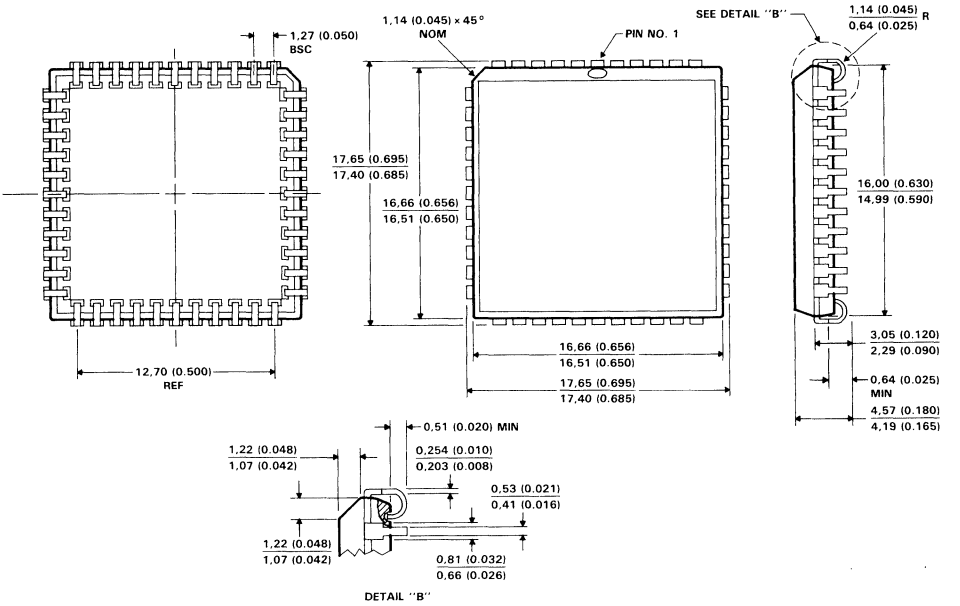
MECHANICAL DATA

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



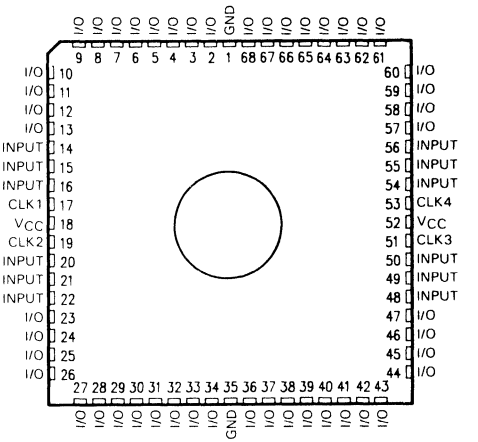
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

EP1810
HIGH-PERFORMANCE 48-MACROCELL ERASABLE PROGRAMMABLE LOGIC DEVICE (EPLD)

D3232, FEBRUARY 1989—REVISED AUGUST 1989

- **Erasable, User-Configurable LSI Circuit Capable of Implementing 2100 Equivalent Gates of Conventional and Custom Logic**
- **Speed Equivalent to 74LS TTL with 33-MHz Clock Rates**
- **Virtually Zero Standby Power . . . 35 μA Typ**
- **Active Power of 250 mW at 5 MHz**
- **Programmable Clock Option Allows Independent Clocking of All Registers**
- **Forty-eight Macrocells with Configurable I/O Architecture Allowing Up to 64 Inputs or 48 Outputs**
- **Accepts TTL SSI and MSI Based Macrofunction Design Inputs**
- **TTL/CMOS I/O Compatibility**
- **100% Generically Testable — Provides 100% Programming Yield**
- **CAD Support from the TI EPLD Development System Featuring Schematic Capture Design Entry with Extensive Primitive and Macrofunction Libraries**
- **Packaged in a 68-Pin J-Leaded, Ceramic (with Window) and Plastic (One-Time Programmable) Chip Carrier**

CHIP-CARRIER PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PACKAGE TYPE	
		CERAMIC CHIP CARRIER (CLCC)	PLASTIC CHIP CARRIER (PLCC)
0°C to 70°C	35 ns	EP1810JC-35	EP1810LC-35
	45 ns	EP1810JC-45	EP1810LC-45
−40°C to 85°C	45 ns	EP1810JI-45	EP1810LI-45

description

The EP1810 series of CMOS EPLDs from Texas Instruments offer LSI density, TTL equivalent speed performance and low power consumption. Each device is capable of implementing over 2100 equivalent gates of SSI, MSI and custom logic circuits. The EP1810 series is packaged as a 68-Pin J-Leaded Chip Carrier, and is available in ceramic (erasable) and plastic (one-time programmable) versions.

The EP1810 series is designed as an LSI replacement for traditional low-power Schottky TTL logic circuits. Its speed and density also make it suitable for high-performance complex functions such as dedicated peripheral controllers and intelligent support chips. Integrated-circuit count and power requirements can be reduced by several orders of magnitude allowing similar reduction in total size and cost of the system, with significantly enhanced reliability.

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The EP1810 architecture has been configured to facilitate design with conventional TTL SSI and MSI building blocks as well as simple, optimized gate and flip-flop elements. Schematic descriptions of these functions are stored in a library. The desired TTL logic functions are selected and interconnected "on-screen" with a low-cost personal-computer based workstation. The design processor within the TI EPLD Development System then automatically places the functions in appropriate locations within the EPLD's internal structure. Included in the Development System is EPLD programming hardware and software. The TI EPLD Development System is available for the personal computer.

The EP1810 uses a 1.2 μm CMOS EPROM technoloy employing EPROM transistors to configure logic connections. User defined logic functions are constructed by selectively programming EPROM cells within the device. The EPROM technology also allows 100% generic testing (all devices are 100% tested at the factory). The devices can be erased with ultraviolet light. Design changes are no longer costly or time consuming.

functional description

The EP1810 series of Erasable Programmable Logic Devices (EPLDs) use CMOS EPROM cells to configure logic functions within the device. The EP1810 architecture is 100% user configurable, allowing the device to accommodate a variety of independent logic functions. Externally, the EP1810 provides 16 dedicated data inputs, four of which may be used as system clock inputs. There are 48 I/O pins, which may be individually configured for input, output, or bidirectional data flow.

macrocells

Internally, the EP1810 architecture consists of a series of macrocells. All logic is implemented within these cells. Each macrocell, shown in Figure 1, contains three basic elements: a logic array, a selectable register element, and 3-state I/O buffer (see Figure 1). All combinational logic such as exclusive-OR, NAND, NOR, AND, OR and invert gates are implemented within the logic array. For register applications, each macrocell provides one of 4 possible flip-flop options: D,T,JK,SR. Each EP1810 macrocell is equivalent to over 40 2-input NAND gates.

The EP1810 is partitioned into four identical quadrants. Each quadrant contains 12 macrocells. Input signals into the macrocells come from the EP1810 internal bus structures. Macrocell outputs may drive the EP1810 external pins as well as the internal buses. Figure 2 illustrates a simple logic function that can be implemented within a single macrocell. Note that all combinational logic is implemented within the logic array, a JK flip-flop is selected, and the 3-state buffer is permanently enabled.

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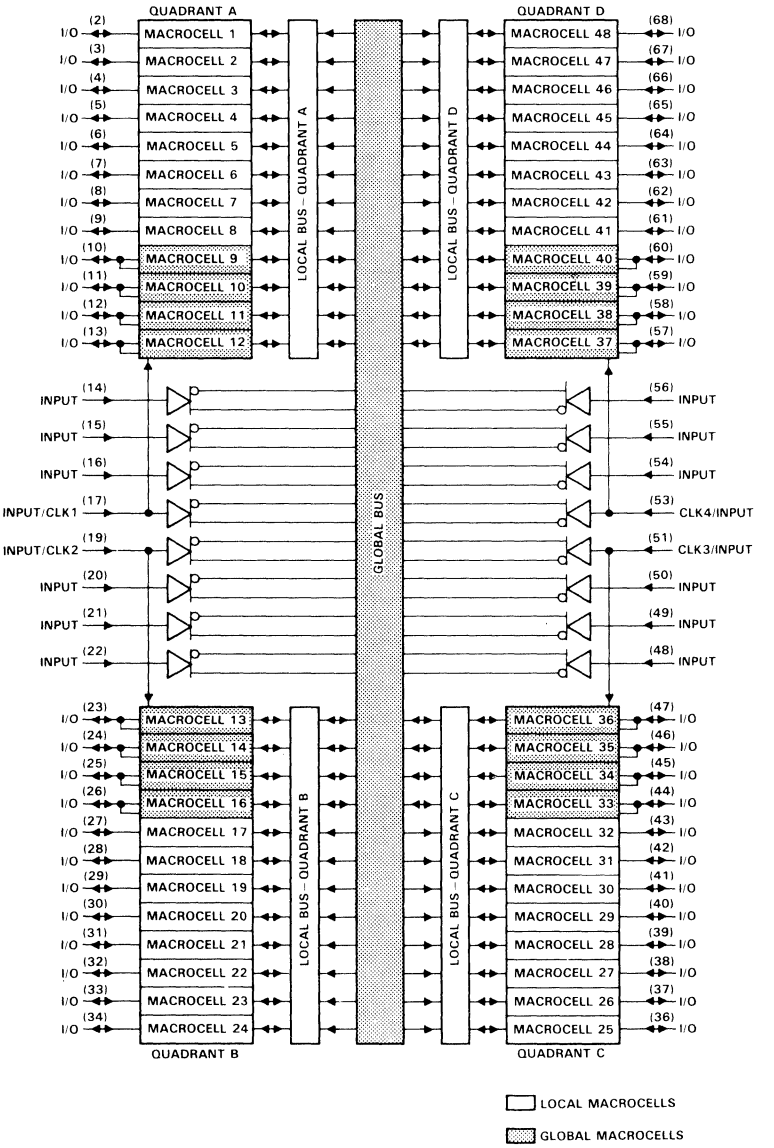
functional block diagram



Each EP1810 macrocell consists of 3 basic components (see Figure 1):

1. A logic array for gated logic.
2. A flip-flop for data storage (selectable options include D, T, JK, and SR). The flip-flop may be bypassed for purely combinational functions.
3. A 3-state I/O buffer to define input, output, or bidirectional data flow.

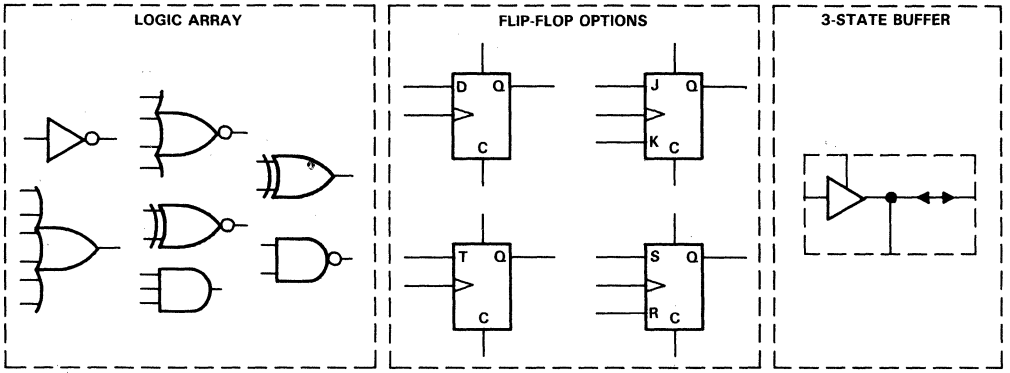


FIGURE 1. MACROCELL COMPONENTS

Typical logic functional implemented into a single macrocell. Each EP1810 macrocell can accommodate the equivalent of 40 gates.

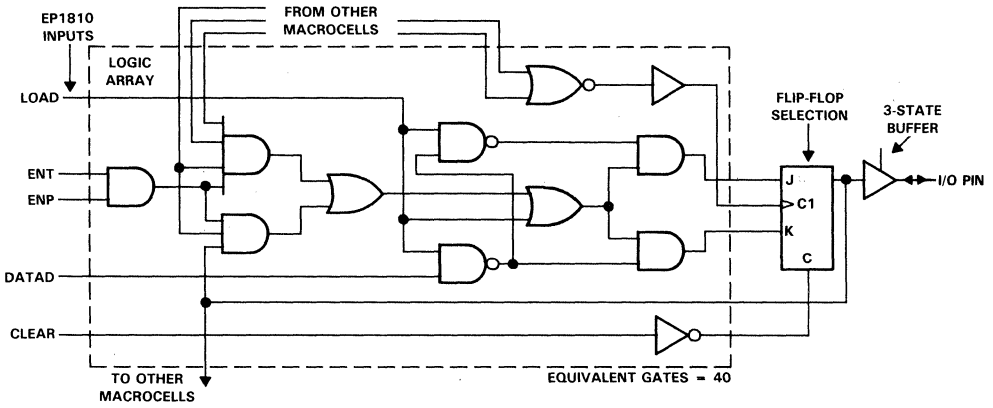


FIGURE 2. SAMPLE CIRCUIT

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The EP1810 macrocell architecture is shown in Figures 3 and 4. There are 32 macrocells called local macrocells. These macrocells offer a multiplexed feedback path (pin or internal) which drives the local bus of the respective quadrant.

There are another 16 macrocells known as the global macrocells (see Figure 4). These global macrocells have features that allow each macrocell to implement buried logic functions and, at the same time, serve as dedicated input pins. Thus, the EP1810 may have an additional 16 input pins giving a total of 32 inputs. The global macrocells have the same timing characteristics as the local macrocells.

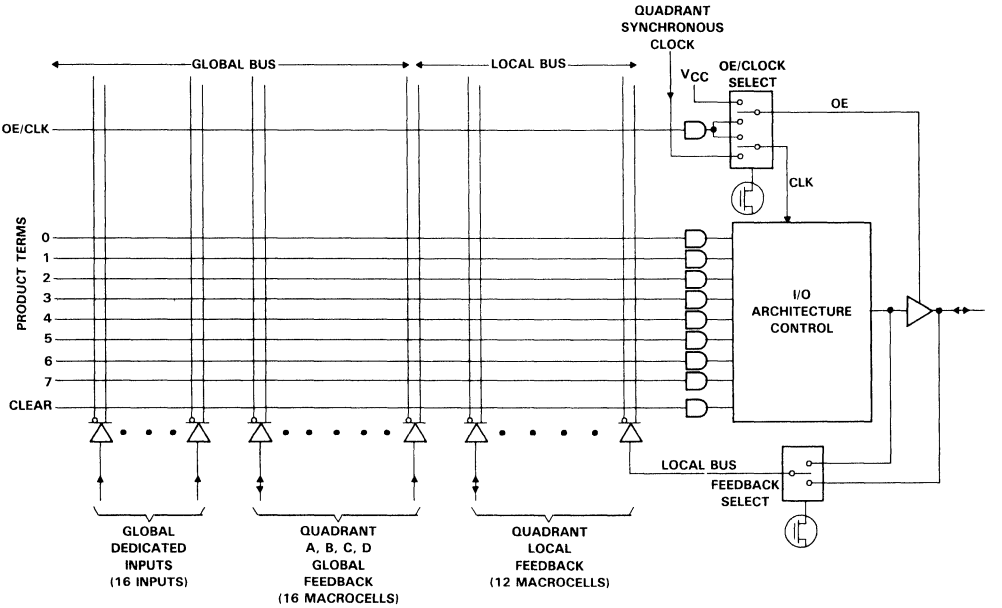

FIGURE 3. LOCAL MACROCELL LOGIC ARRAY

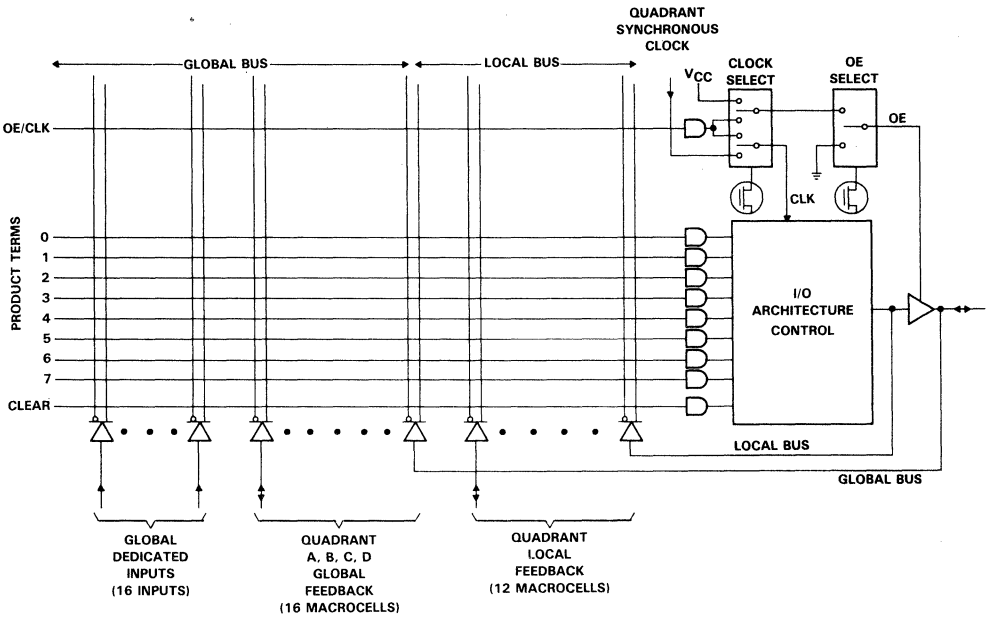

FIGURE 4. GLOBAL MACROCELL LOGIC ARRAY

clock options

Each of the EP1810 internal flip-flops may be clocked independently or in user defined groups. Any input or internal logic function may be used as a clock. These clock signals are activated by driving the flip-flop clock input with a clock buffer (CLKB) primitive. In this mode, the flip-flops can be configured for positive or negative edge triggered operation.

Four dedicated system clocks (CLK1-CLK4) also provide clock signals to the flip-flops. System clocks are connected directly from the EP1810 external pins. With this direct connection, system clocks give enhanced clock to output delay times than internally operated clock signals. There is one system clock per EP1810 quadrant. When using system clocks, the flip-flops are positive edge triggered (data transitions occur on the rising edge of the clock).

macrofunctions

The macrofunctions shown in Figure 5 allow the circuit designer to use popular TTL SSI and MSI building blocks. Many macrofunctions are standard TTL circuits such as counters, comparators, multiplexers, decoders, shift registers, etc. and are identified by their familiar TTL part numbers. Macrofunctions are constructed by combining one or more macrocells. These high-level function blocks may be combined with low-level gate and flip-flop elements to produce a complete logic design.

An automatic function built into the TI EPLD Development System ensures that the use of macrofunctions causes no loss of design efficiency. The development system analyzes the complete logic schematic and automatically removes unused gates and flip-flops from any macrofunction employed. This MacroMunching™ process allows the logic designer to employ macrofunctions without the problems of optimizing their use.

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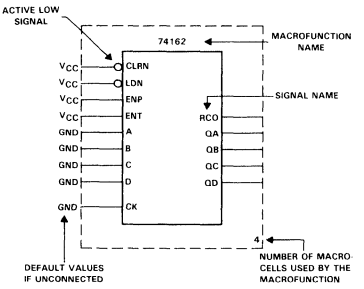
All inputs to macrofunctions are designed with intelligent-default input signal levels (V_{CC} or GND). Normally active high and low signals or unused inputs can simply be left unconnected, further improving productivity and reducing the burden placed on the designer.

Macrofunctions are TTL compatible SSI and MSI circuits giving the circuit designer a high-level approach to EPLD design. Macrofunctions include input default values to unconnected inputs and MacroMunching™ to unused outputs. The macrofunction library consists of over 100 components.



74162 FUNCTION TABLE

INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
⌐	X	L	X	X					L	L	L	L	L
⌐	L	H	X	X	d	c	b	a	d	c	b	a	L
⌐	H	H	X	L					HOLD COUNT				L
⌐	H	H	L	X					HOLD COUNT				L
⌐	H	H	H	H					COUNT UP				L
⌐	H	H	H	H					H	L	L	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d = level of steady state input at inputs A,B,C,D

FIGURE 5. MACROFUNCTION SYMBOL

design libraries

Texas Instruments provides both primitive and macrofunction libraries within the EPLD Development System. These libraries are used with the LogiCaps™ schematic capture design entry to specify the logic. Elements from both libraries may be used in the same design, allowing full utilization of the EP1810 resources.

primitive library

The primitive library consists of 80 low-level logic gates, flip-flop, and I/O symbols. See section on primitive library in the A+PLUS™ *reference guide*. Basic gates provided are AND, OR, NAND, NOR, Exclusive OR and NOR, and NOT functions. De-Morgan's inversion (bubble input) of each gate is included. These logic gates have a maximum of 12 inputs. Larger gates may be constructed by chaining primitives together. Flip-flops in the form of D,T,JK and SR types are supplied. Each flip-flop has asynchronous clear capability. To connect signals to external pins, input and 3-state I/O buffers are available. For the designer's convenience, compound primitives that combine register and I/O buffers, are also supplied.

macrofunction library

The development system macrofunction library encompasses over 100 high-level building blocks that can greatly increase design productivity. See the ADLIB™ and TTL macrofunctions manual that comes with the development system. The library contains the most commonly used TTL SSI and MSI functions. In addition, a number of more specialized macrofunctions have been added. These blocks perform logic functions in an optimum manner for EPLD implementation. They include counters implemented with toggle flip-flops, inhibit gates, combinational shift-registers/counters and a variety of useful logic structures not found in standard TTL devices.

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A+PLUS is a trademark of ALTERA Corporation.
ADLIB is a trademark of ALTERA Corporation.

starting a design

To get started on an EP1810 design the following sequence of preliminary steps is suggested. The equations given will help estimate how to build your system with EP1810s.

partitioning

Partition the complete system into functional blocks. Major functional blocks may be expressed in standard MSI TTL form for integration within the EP1810. Should the design require a multiple EPLD solution, the I/O connections which interface between the EPLDs should be minimized. The complete schematic should be structured as a set of subsystems such as counters, shift registers, comparators, etc., to allow easy design entry.

timing specifications

Knowledge of the base-clock frequency and critical-timing paths are necessary to make the correct choice of EPLDs. The EP1810 series can support circuits operating up to 33 MHz. Critical-timing paths are determined based upon input buffer, logic array, and output buffer delays. See switching characteristics. Smaller EPLDs, such as the EP910 or EP610, can be used for circuits that demand higher speed requirements on critical paths.

estimating a fit

To estimate the amount of logic that will fit into an EP1810, the number of input and output pins and the number of macrocells must be specified.

To estimate the number of macrocells, determine the number of buried flip-flops (flip-flops that do not drive output pins) and the number of macrocells used by macrofunctions. Since basic gates are implemented within the logic array, they usually do not require an entire macrocell. Therefore, they may be safely ignored in the estimation.

Each member of the macrofunction library has a maximum number of macrocells used to build the function. This number is shown in the lower right hand corner of the symbol. Refer to the ADLIB™ and TTL macrofunction manual to determine how many macrocells each macrofunction requires. Note that some macrofunctions have no macrocell specification. These functions use only a portion of the logic array, thus other logic could be added before the entire macrocell is used.

estimation formula

The estimation formula is as follows:

1. Determine the number of output pins = OP
2. Determine the number of input pins = IP (if less than 16 enter zero)
3. Determine the number of macrocells = BFF + MR where: BFF = buried flip-flops and MR = macrofunction requirements.

If OP + IP + BFF + MR < 48, the design will most likely fit into an EP1810. Complete the design using the TI EPLD Development System.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} (t ≤ 20 ns) . . . . . −2 V to 7 V
Programming supply voltage range, V_{PP} . . . . . −0.3 V to 13.5 V
Instantaneous programming supply voltage range, V_{PP} (t ≤ 20 ns) . . . . . −2 V to 13.5 V
Input voltage range, V_I . . . . . −0.3 V to 7 V
Instantaneous input voltage range, V_I (t ≤ 20 ns) . . . . . −2 V to 7 V
V_{CC} or GND current . . . . . −400 mA to 400 mA
Power dissipation at 25°C free-air temperature (see Note 2) . . . . . 2000 mW
Operating free-air temperature, T_A . . . . . −65°C to 135°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to GND terminal.
2. For operation above 25°C free-air temperature, derate to 240 mW at 135°C at the rate of 16 mW/°C.

recommended operating conditions

PARAMETER			EP1810I		EP1810C		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 3)		−0.3	0.8	−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
t_r	Rise time	CLK input		50		100	ns
		Other inputs		50		100	
t_f	Fall time	CLK input		50		100	ns
		Other inputs		50		100	
T_A	Operating free-air temperature		−40	85	0	70	°C

NOTE 3: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		EP1810I			EP1810C			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	TTL	I_{OH} = −4 mA		2.4			2.4			V
		CMOS	I_{OH} = −2 mA		3.84			3.84			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA				0.45			0.45	V
I_I	Input current		V_I = V_{CC} or GND				±10			±10	µA
I_{OZ}	Off-state output current		V_O = V_{CC} or GND				±10			±10	µA
I_{CC}	Supply current	Standby	V_I = V_{CC} or GND, No load	See Note 4		0.035	0.15		0.035	0.15	mA
		Non-turbo		See Note 5		10	40		10	30	
		Turbo		See Note 5		100	240		100	180	
C_i	Input capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C			20			20	pF
C_o	Output capacitance		V_O = 0, f = 1 MHz,	T_A = 25°C			20			20	pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C			25			25	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. When in the non-turbo mode, the device automatically goes into the standby mode approximately 100 ns after the last transition.
5. These parameters are measured with device programmed as four 12-bit counters and f = 1 MHz.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

turbo-bit on

PARAMETER†		TEST CONDITIONS	EP1810-35		EP1810-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd1(tot)}$	Input to nonregistered output delay	C_L = 35 pF		35		45	ns
$t_{pd2(tot)}$	I/O input to nonregistered output delay			40		50	ns
t_{in}	Input pad and buffer delay			7		7	ns
t_{io}	I/O input pad and buffer delay			5		5	ns
t_{lad}	Logic array delay			19		27	ns
t_{od}	Output buffer and pad delay	C_L = 35 pF		9		11	ns
t_{PZX}	Output buffer enable time			9		11	ns
t_{PXZ}	Output buffer disable time	C_L = 5 pF, See Note 6		9		11	ns

turbo-bit off

PARAMETER†		TEST CONDITIONS	EP1810-35		EP1810-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd1(tot)}$	Input to nonregistered output delay	C_L = 35 pF		65		75	ns
$t_{pd2(tot)}$	I/O input to nonregistered output delay			70		80	ns
t_{in}	Input pad and buffer delay			7		7	ns
t_{io}	I/O input pad and buffer delay			5		5	ns
t_{lad}	Logic array delay			49		57	ns
t_{od}	Output buffer and pad delay	C_L = 35 pF		9		11	ns
t_{PZX}	Output buffer enable time			9		11	ns
t_{PXZ}	Output buffer disable time	C_L = 5 pF, See Note 6		9		11	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTE 6: This capacitance is for an output voltage change of 500 mV.

synchronous/asynchronous clock mode, turbo-bit on

PARAMETER†		TEST CONDITIONS	EP1810-35		EP1810-45		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	See Note 7	40		33.3		MHz
t_{su}	Register set-up time		10		11		ns
t_h	Register hold time		15		18		ns
t_{ch}	Clock high pulse duration		12		15		ns
t_{cl}	Clock low pulse duration		12		15		ns
t_{ic}	Clock delay			19		27	ns
t_{ics}	System clock delay			4		8	ns
t_{fd}	Feedback delay			6		7	ns
t_{clr}	Register clear time nonregistered output			24		32	ns
t_{cnt}	Minimum clock period (register output feedback to register input-internal data)			35		45	ns
f_{cnt}	Maximum frequency with feedback	See Note 5	28.6		22.2		MHz

synchronous/asynchronous clock mode, turbo-bit off

PARAMETER†		TEST CONDITIONS	EP1810-35		EP1810-45		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	See Note 7	40		33.3		MHz
t_{su}	Register set-up time		10		11		ns
t_h	Register hold time		15		18		ns
t_{ch}	Clock high pulse duration		12		15		ns
t_{cl}	Clock low pulse duration		12		15		ns
t_{ic}	Clock delay			49		57	ns
t_{ics}	System clock delay			4		8	ns
t_{fd}	Feedback delay			−24		−23	ns
t_{clr}	Register clear time nonregistered output			54		62	ns
t_{cnt}	Minimum clock period (register output feedback to register input-internal data)			35		45	ns
f_{cnt}	Maximum frequency with feedback	See Note 5	28.6		22.2		MHz

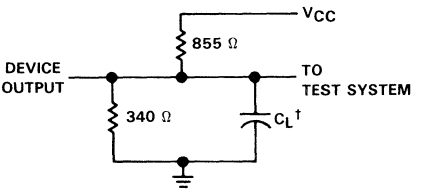
† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 5. f_{max} is measured with device programmed as four 12-bit counters.
7. The f_{max} values shown represent the highest frequency of operation without feedback.
8. The negative number shown for this specification is to compensate for the 30 ns that is being added to the t_{lad} parameter in the turbo-bit off mode. In the non-turbo mode, t_{fd} is not affected by the additional propagation delay because the logic array is already taken out of the non-turbo mode by the first transition into the array. See section on EPLD delay elements.

functional testing

The EP1810 is functionallly tested including complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield. As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP1810 allows test program patterns to be used and then erased.

Figure 6 shows the dynamic test circuit and the conditions under which dynamic measurements are made. Because power supply transients can affect dynamic measurements, simultaneous transitions of multiple outputs should be avoided to ensure accurate measurement. The performance of threshold tests under dynamic conditions should not be attempted. Large-amplitude fast-ground-current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground terminal and the test-system ground can create significant reductions in observable input noise immunity.



†Includes jig capacitance

FIGURE 6. DYNAMIC TEST CIRCUIT

design security

The EP1810 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within the EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the device.

turbo bit

Some EPLDs contain a programmable option to control the automatic power-down feature that enables the low-standby-power mode of the device. This option is controlled by a turbo bit that can be set using the TI EPLD Development System. When the turbo bit is on, the low-standby-power mode is disabled. This renders the circuit less sensitive to V_{CC} noise transients created by the power-up/power-down cycle when operating in the low-power mode. The typical I_{CC} versus frequency data for both the turbo-bit-on mode and the turbo-bit-off (low power) mode is shown in Figure 7. All dynamic parameters are tested with the turbo bit on. Figure 8 shows the relationship between the output drive currents and the corresponding output voltages.

Figures 7 and 8 show the I_{CC} vs f_{max}, and output current vs output voltage.

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SUPPLY CURRENT
vs
MAXIMUM FREQUENCY

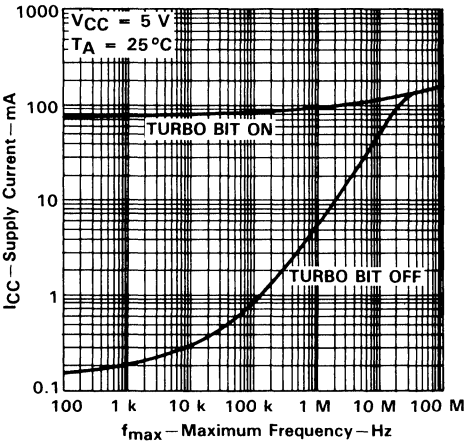


FIGURE 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

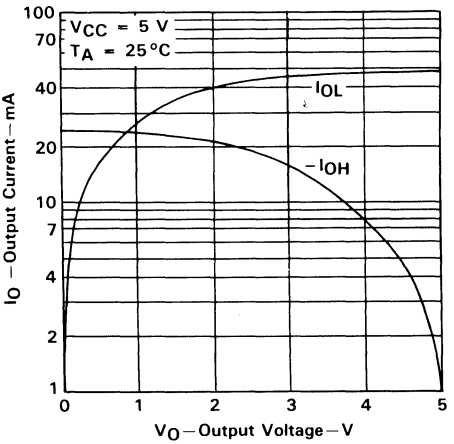
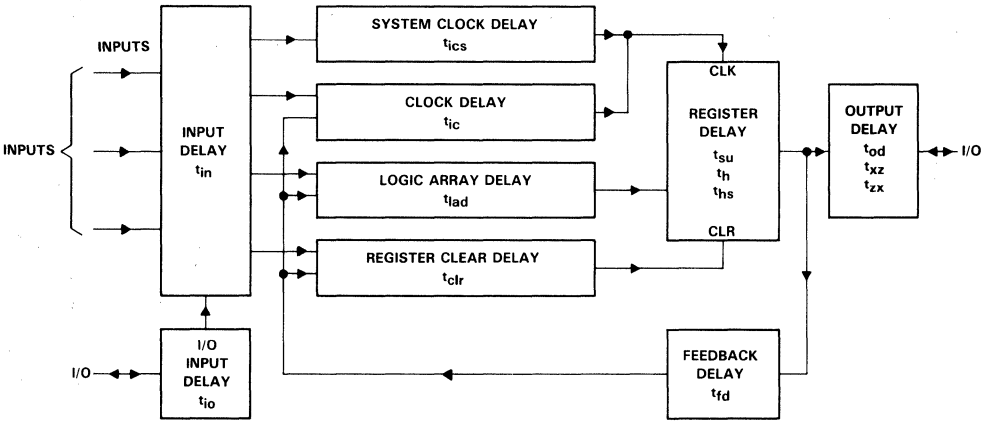


FIGURE 8

If the design requires low-power operation, the turbo bit should be off (disabled). When operating in this mode, some dynamic parameters are subject to increases.



NOTE: For combinatorial outputs, the delay between the logic array and the output buffer is zero. (i.e., $t_{su} = 0$ or $t_h = 0$)

FIGURE 9. EPLD MACROCELL DELAY PATHS MODEL

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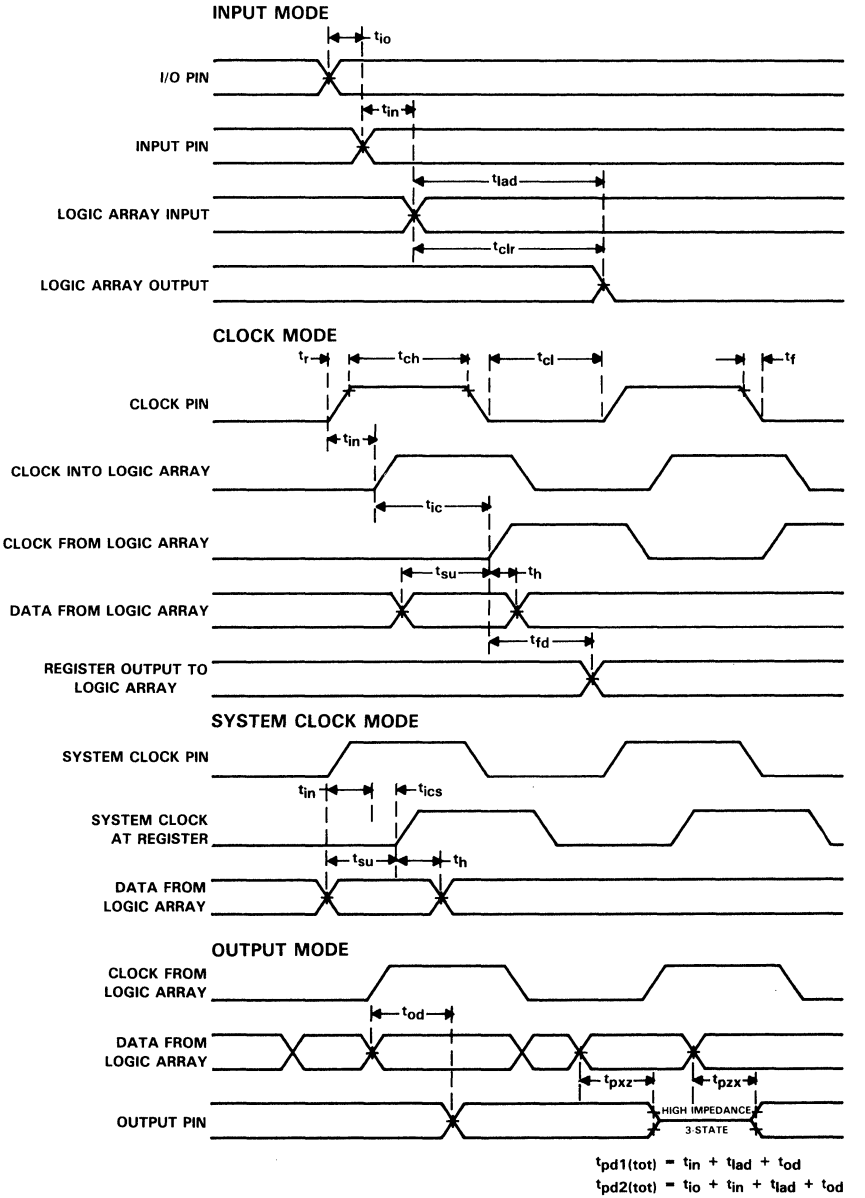

FIGURE 10. SWITCHING WAVEFORMS

understanding EPLD timing characteristics

introduction

One of the most important benefits of using an EPLD in any design is the integration of complex logic functions into single chip solutions in most cases. However, when the functional compatibility of a design has been determined, timing analysis should be completed to ensure AC parameter compatibility.

The purpose of this applications supplement is to discuss the timing delays which exist in the TI EPLDs. The focus here is on the inherent delay paths that exist in every EPLD and their relation to the data sheet switching specifications. This should aid designers in modelling and simulating their logic designs.

gate delays vs EPLD timing characteristics

Accurately modelling the timing characteristics requires an understanding of how a given application is implemented within the EPLD. Most designs targeted for EPLDs contain basic gates, and TTL macrofunctions, which are emulated by the EPLD general macrocell structure. The macrocell structure is an array of logic in an AND/OR configuration with a programmable inversion followed by an optional flip-flop and feedback, (See Figure 11).

When designing with EPLDs, the term "gate delay" is not a useful measure. Within the EPLD AND array are product terms. A product term is simply an n-input AND gate where n is the number of connections. Depending on the logic implemented, a single product term may represent one to several gate equivalents. Therefore, gate delays do not necessarily provide EPLD timing characteristics.

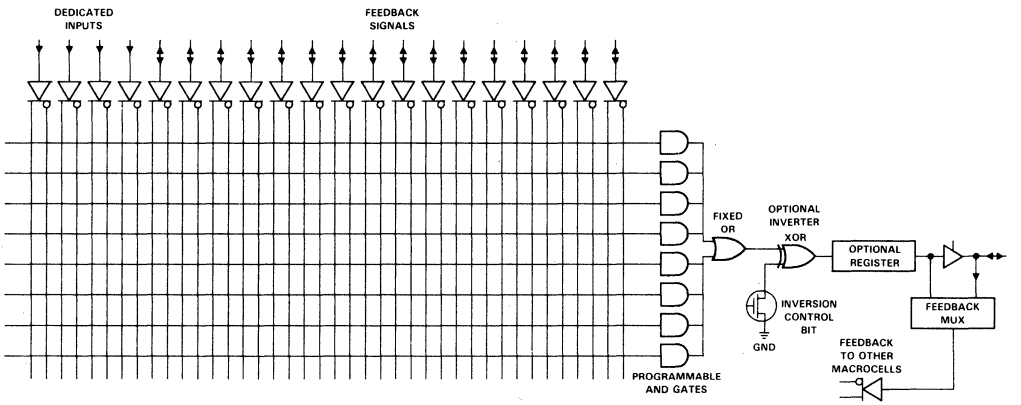

FIGURE 11. EPLD MACROCELL

AND/OR/INV structure

The AND portion consists of a column of AND gates, each of which has a very large number of possible inputs selected by EPROM bits. The EPROM bits serve as electrical switches. An erased bit passes the input into the AND gate (switch on), while a programmed bit cuts it off (switch off). All bits are initially erased.

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The number of possible inputs to an AND gate varies from 40 (EP610) to 88 (EP1810). In the EP610 and EP910 every dedicated input and its inversion and every macrocell feedback and its inversion are possible inputs to the AND gate. In the EP1810 which has local and global bussing, not all of the macrocell feedback is available at every AND gate. The reason larger devices such as the EP1810 do not have all feedbacks feeding the AND gates is to preserve the speed characteristics of the device.

Following the AND gates is a fixed 8 input OR function. This structure is called a fixed OR because the AND functions are hard wired into the OR gates, and cannot be redistributed if unused.

The OR gate feeds a programmable inverter (XOR). A dedicated EPROM bit either programs the inversion function on or off.

EPLD delay elements

The simplest solution to the architectural requirements is to model time through the logic array as a constant. This parameter is called t_{lad}. The rest of the elements in the timing model are similar to those found in conventional logic. There are input and output delay parameters (t_{in}, t_{io}, t_{od}); register parameters (t_{su}, t_h, t_{clr}, t_{hs}, t_{ics}, t_{ic}); and internal connection parameters (t_{fd}). A detailed diagram of an EPLD Macrocell Delay Paths Model is shown in Figure 9 with a description of the signals.

glossary – internal delay elements

t_{clr} - Asynchronous register clear time. This is the amount of time it takes for a low signal to appear at the output of a register after the transition at the logic array, including the time required to go through the logic array.

t_{fd} - Feedback delay. In registered applications, this is the delay from the output of the register to the input of the logic array. In combinational applications, it is the delay from the combinational feedback to the input of the logic array.

t_h - Register hold time. This is the internal hold time of the register inside a macrocell: measured from the register clock to the register data input.

t_{lad} - Logic array delay. This parameter incorporates all delay from an input or feedback through the AND/OR structure.

t_{ic} - Clock delay. This delay incorporates all the delay incurred between the output of an input pad or I/O pad and the clock input of a register including the time required to go through the logic array. This delay is differentiated from the system clock delay tics by the need to pass through a CLKB primitive, which specifies individual register clocking.

t_{ics} - System clock delay. This delay incorporates all delays incurred between the output of the input pad and the clock input of the registers for dedicated clock pins.

t_{in} - Input pad and buffer delay which direct the true and complement data input signals into the AND array.

t_{io} - I/O input pad delay. This delay applies to I/O pins committed as inputs.

t_{od} - Output buffer and pad delay. For registered applications, this incorporates the clock to output delay of the flip flop. In combinational applications, it incorporates delay from the output of the array to the output of the device.

t_{su} - Register setup time. This is the internal setup time of the register inside a macrocell - measured from the register data input until the register clock.

t_{xz} - Time to 3-state output delay. This delay incorporates the time between a high-to-low transition on the enable input of the 3-state buffer to assertion of a high impedance value at an output pin.

t_{zx} - 3-state to active output delay. This delay incorporates the time between a low-to-high transition on the enable input of the 3-state buffer to assertion of a high or low logic level at an output pin.

explaining the EPLD data sheet specifications

The data sheet for each TI EPLD references timing parameters which characterize the switching operating specifications. These parameters are measured values, derived from extensive device characterization and 100% device testing. Among the switching characteristics are the following: $t_{aco1(tot)}$, $t_{acnt(tot)}$, $t_{ah(tot)}$, $t_{asu(tot)}$, $t_{co1(tot)}$, $t_{clr(tot)}$, $t_{cnt(tot)}$, $t_{h(tot)}$, $t_{pd1(tot)}$, $t_{pd2(tot)}$, $t_{PXZ(tot)}$, $t_{PZX(tot)}$, $t_{su(tot)}$. These parameters, described below in detail, may be represented by the EPLD internal delay elements. (See Figure 12)

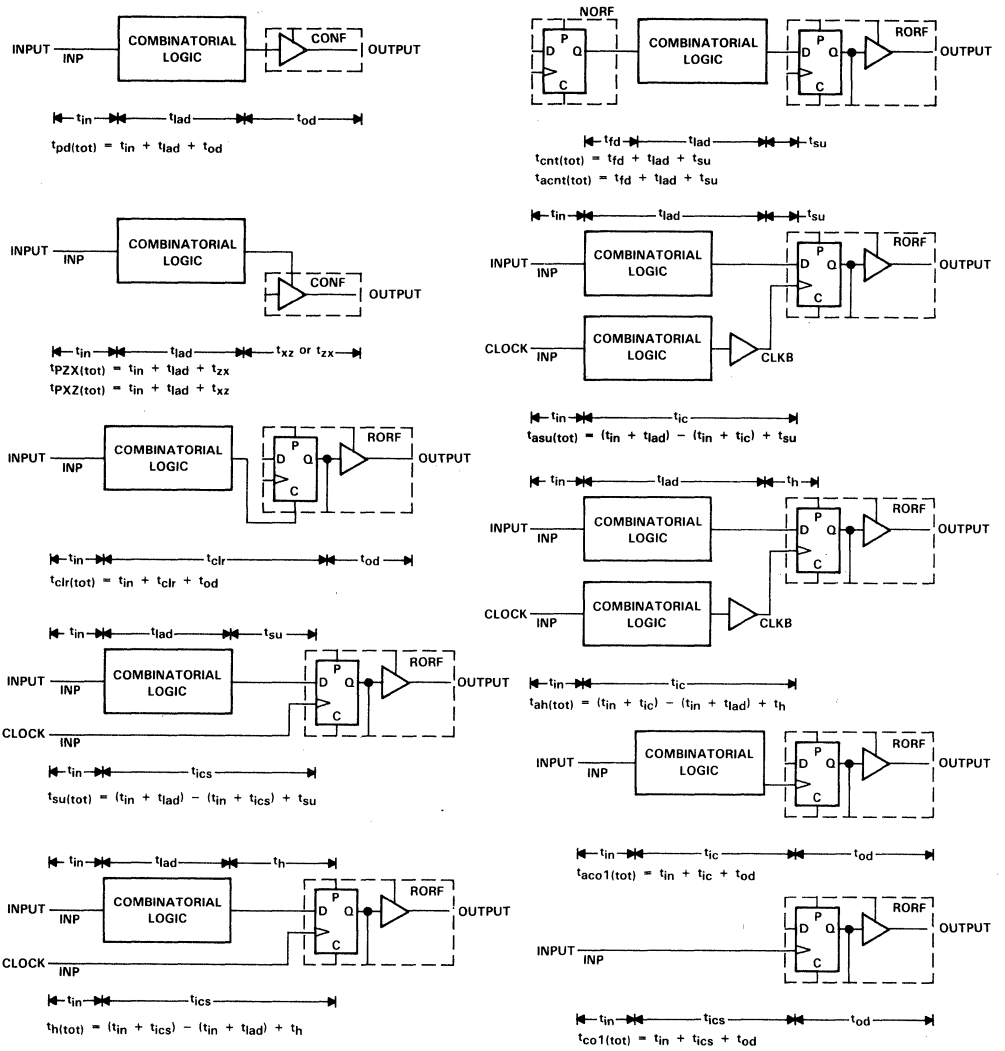

FIGURE 12. TI EPLD TIMING EQUATIONS

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glossary – external delay elements

$t_{aco1(tot)}$ - Defined as the asynchronous clock to output delay. It is the time required to obtain a valid output after a clock is asserted on an input pin. This delay is the sum of the input delay (t_{in}), the clock delay (t_{ic}), and the output delay (t_{od}).

$t_{acnt(tot)}$ - Defined as the asynchronous clocked counter period. It is the minimum period a counter can maintain when asynchronously clocked. This delay is the sum of the feedback delay (t_{fd}) and the logic array delay (t_{lad}), and the register setup time (t_{su}).

$t_{ah(tot)}$ - Defined as the asynchronous hold time. It is the amount of time required for data to be present after an asynchronous clock. This value is the difference between the sum of the input delay (t_{in}), the clock delay (t_{ic}), and the hold time (t_h) and the sum of the input delay (t_{in}) and logic array delay (t_{lad}).

$t_{asu(tot)}$ - Defined as asynchronous setup time. It is the time required for data to be present at the input to the register before an asynchronous clock. This value is the difference between the sum of the input delay (t_{in}), array delay (t_{lad}) and the register setup time (t_{su}) and the sum of the input delay (t_{in}) and the clock delay (t_{ic}).

$t_{co1(tot)}$ - Defined as system clock to output delay. It is the time required to obtain a valid output after the system clock is asserted on an input pin. This delay is the sum of the input delay (t_{in}), the system clock delay (t_{ics}), and the output delay (t_{od}).

$t_{clr(tot)}$ - Defined as delay required to clear register. It is the time required to change the output from high to low through a register clear measured from an input transition. This delay is the sum of input delay (t_{in}), register clear delay (t_{clr}), and the output delay (t_{od}).

$t_{cnt(tot)}$ - Defined as the system clock counter period. It is the minimum period a counter can maintain. This delay is the sum of the feedback delay (t_{fd}), the logic array delay (t_{lad}), and the internal register setup time (t_{su}).

$t_{h(tot)}$ - Defined as hold time for the register. It is the amount of time the data must be valid after the system clock. It is the difference between the sum of the internal input delay (t_{in}), the system clock (t_{ics}), and the system-clock hold time (t_{hs}) and the sum of the input delay (t_{in}) and logic array delay (t_{lad}).

$t_{pd1(tot)}$ - Propagation Delay; Defined as the delay from a dedicated input to a non-registered output. This is the time required for data to propagate through the logic array and appear at the EPLD external output pin. This delay is the sum of input delay (t_{in}), array delay (t_{lad}) and output delay (t_{od}).

$t_{pd2(tot)}$ - Propagation Delay; Defined as the delay from I/O pin to a nonregistered output. This is the time required for data from any external I/O input to propagate through any combinational logic and appear at the external output pin of an EPLD. This delay is the sum of the I/O delay (t_{io}), input delay (t_{in}), array delay (t_{lad}), and the output delay (t_{od}).

$t_{PXZ(tot)}$ - Defined as the time to enter into 3-state. It is the time required to change an external output from a valid high or low logic level to 3-state from an input transition. This delay is the sum of input delay (t_{in}), array delay (t_{lad}), and the time to activate the 3-state buffer (t_{xz}).

$t_{PZX(tot)}$ - Defined as the delay from high impedance to active output. It is the time required to change an external output from 3-state to a valid high or low logic level measured from an input transition. This delay is the sum of input delay (t_{in}), array delay (t_{lad}), and the time to de-activate the 3-state buffer (t_{zx}).

$t_{su(tot)}$ - Defined as set up time for the register. It is the time required for data to be present at the register before the system clock. This value is the difference between the sum of input delay (t_{in}), array delay (t_{lad}), and an internal register setup time (t_{su}) and the sum of the input delay (t_{in}) and the system clock delay (t_{ics}).

conclusion

To understand timing relationships in the EP1810 and all EPLDs, it is very important to break up the internal paths into meaningful microparameters that model portions of the EPLD architecture. Once internal paths are decomposed, it is then possible to obtain accurate timing information by summing the appropriate combinations of these microparameters. The EP1810 data sheet and relevant EPLD data sheets provide architectural information on which the parameters apply and how the primitives are implemented.The TI EPLD Development System provides minimized files that aid in the decomposition of designs. The combination of these elements and the knowledge of the architecture of each device allow characterization of any timing path within an EPLD.

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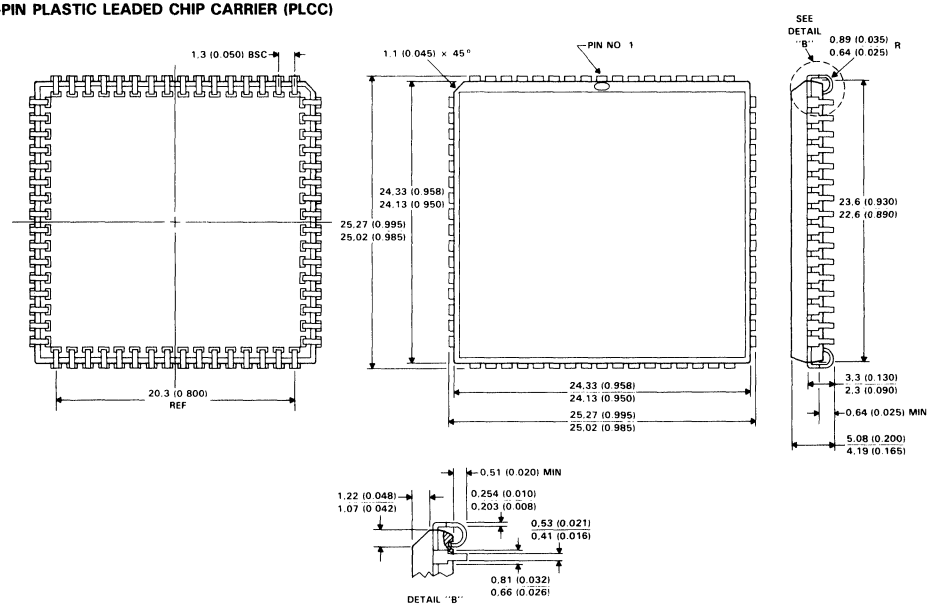
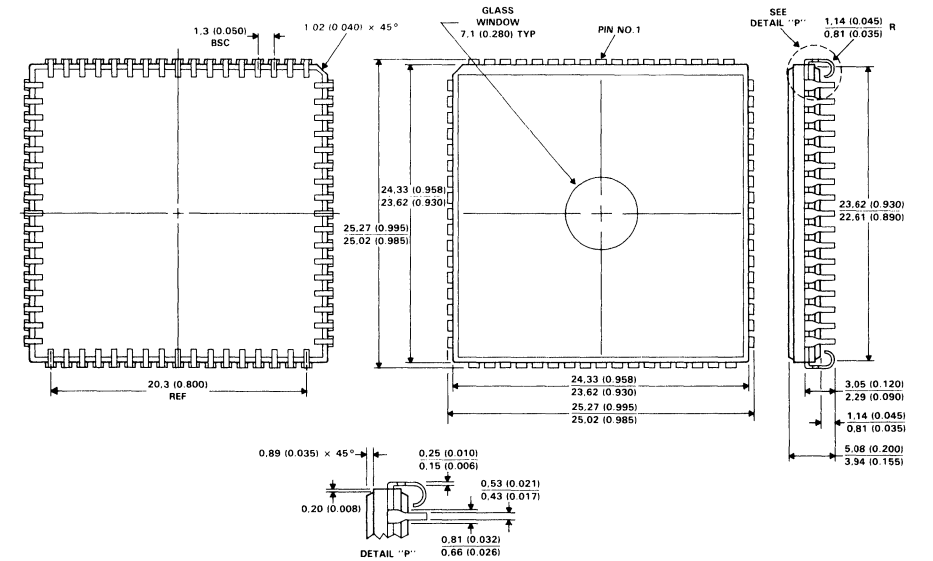
MECHANICAL DATA

68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



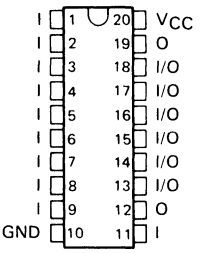
68-PIN CLCC CERAMIC



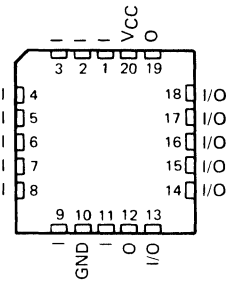
- **Choice of Operating Speeds**
  High Speed, A Devices . . . 25 MHz
  Half Power, A-2 Devices . . . 16 MHz
- **Choice of Input/Output Configuration**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allow for quick design of ''custom'' functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

The PAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PAL is a registered trademark of Monolithic Memories Inc.

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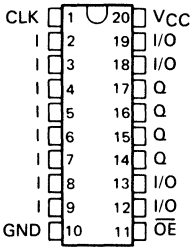
PAL16R4'
J OR W PACKAGE
(TOP VIEW)



PAL16R4'
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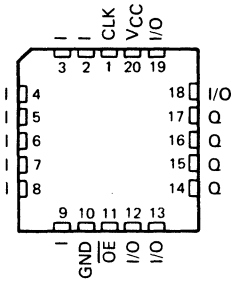
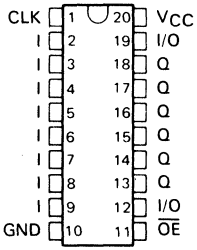
(TOP VIEW)



PAL16R6'
J OR W PACKAGE
(TOP VIEW)



PAL16R6'
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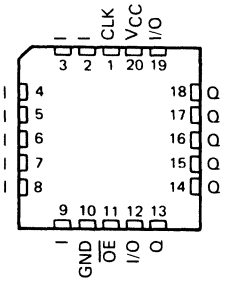
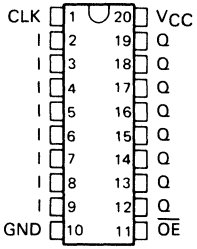
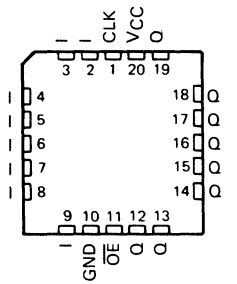
(TOP VIEW)



PAL16R8'
J OR W PACKAGE
(TOP VIEW)



PAL16R8'
FK PACKAGE
(TOP VIEW)



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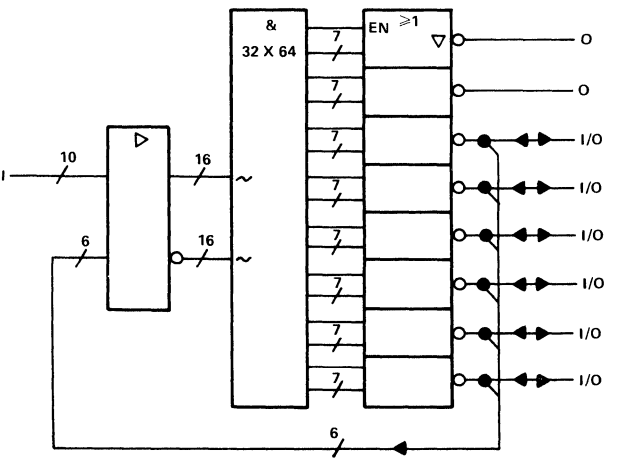
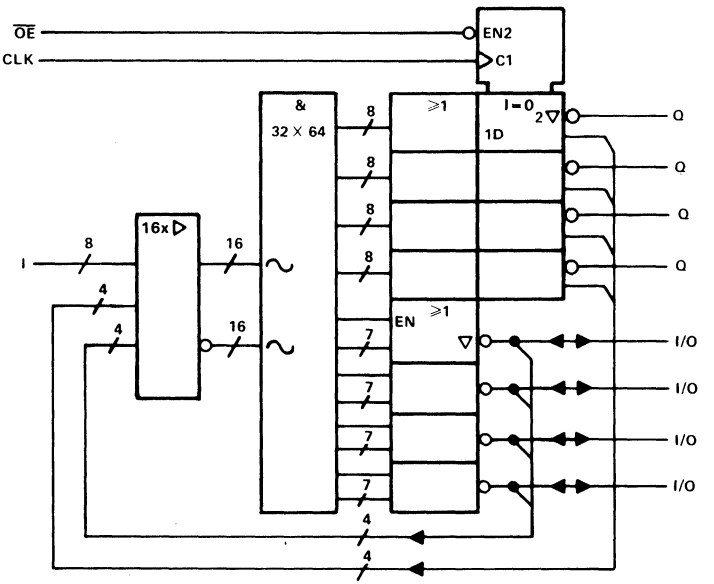
functional block diagrams (positive logic)

PAL16L8AM
PAL16L8A-2M



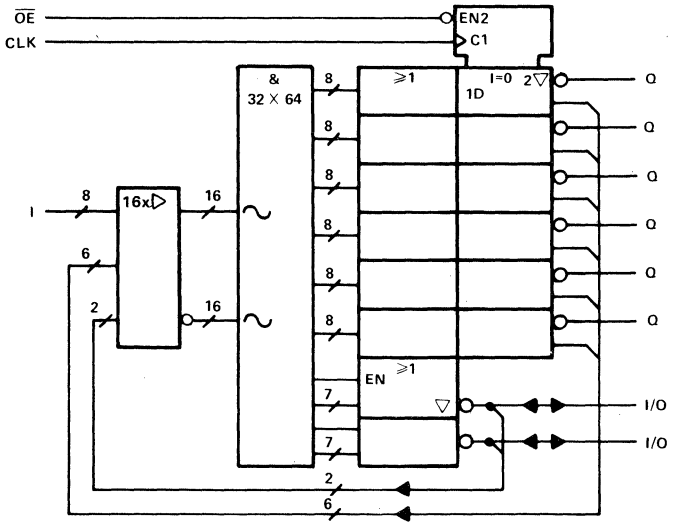
PAL16R4AM
PAL16R4A-2M



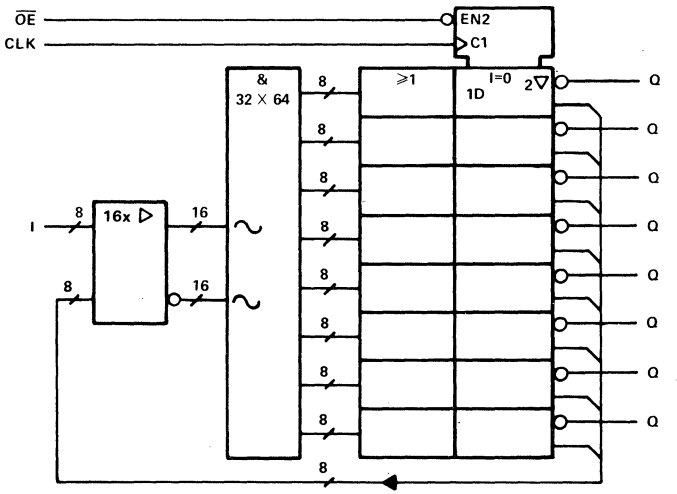
∼ denotes fused inputs

functional block diagrams (positive logic)

PAL16R6AM
PAL16R6A-2M



PAL16R8AM
PAL16R8A-2M



~ denotes fused inputs

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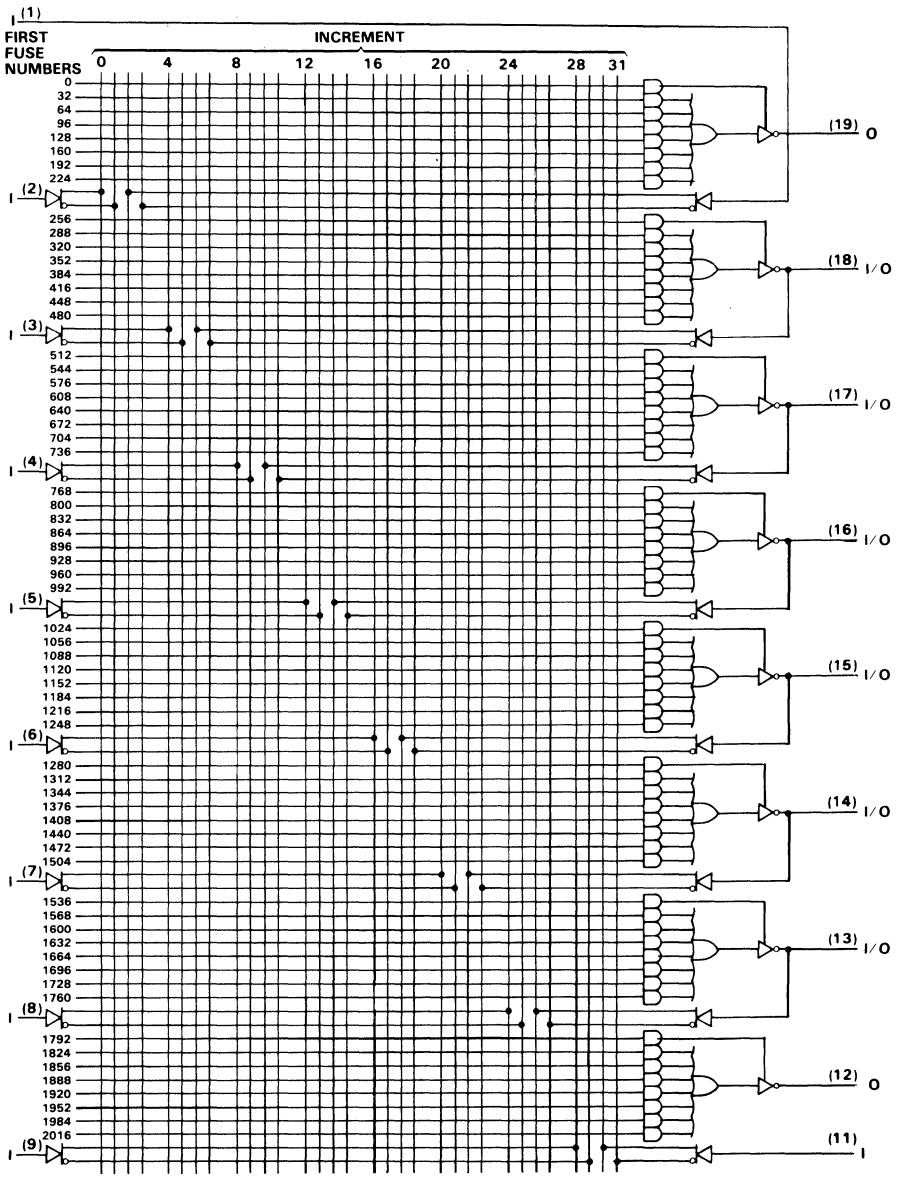
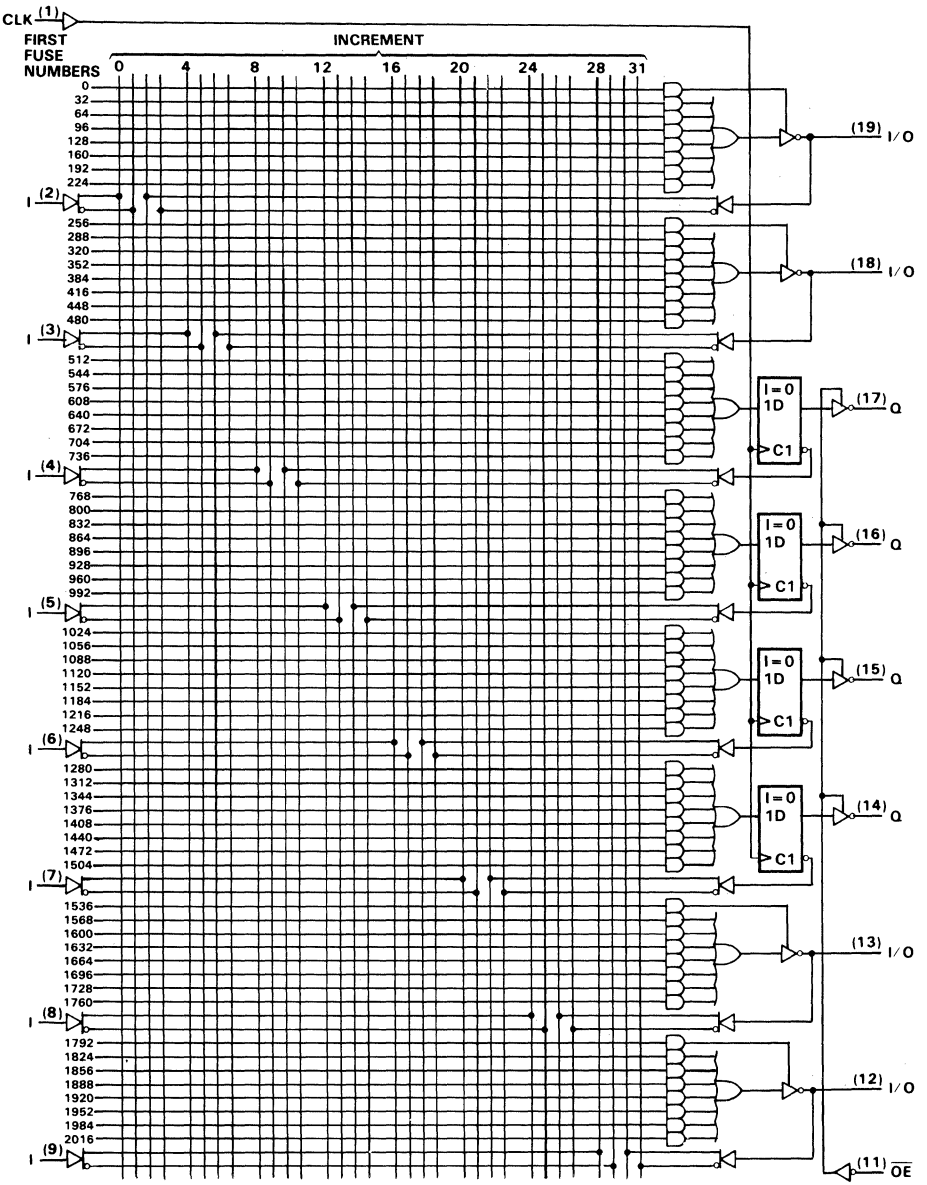


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

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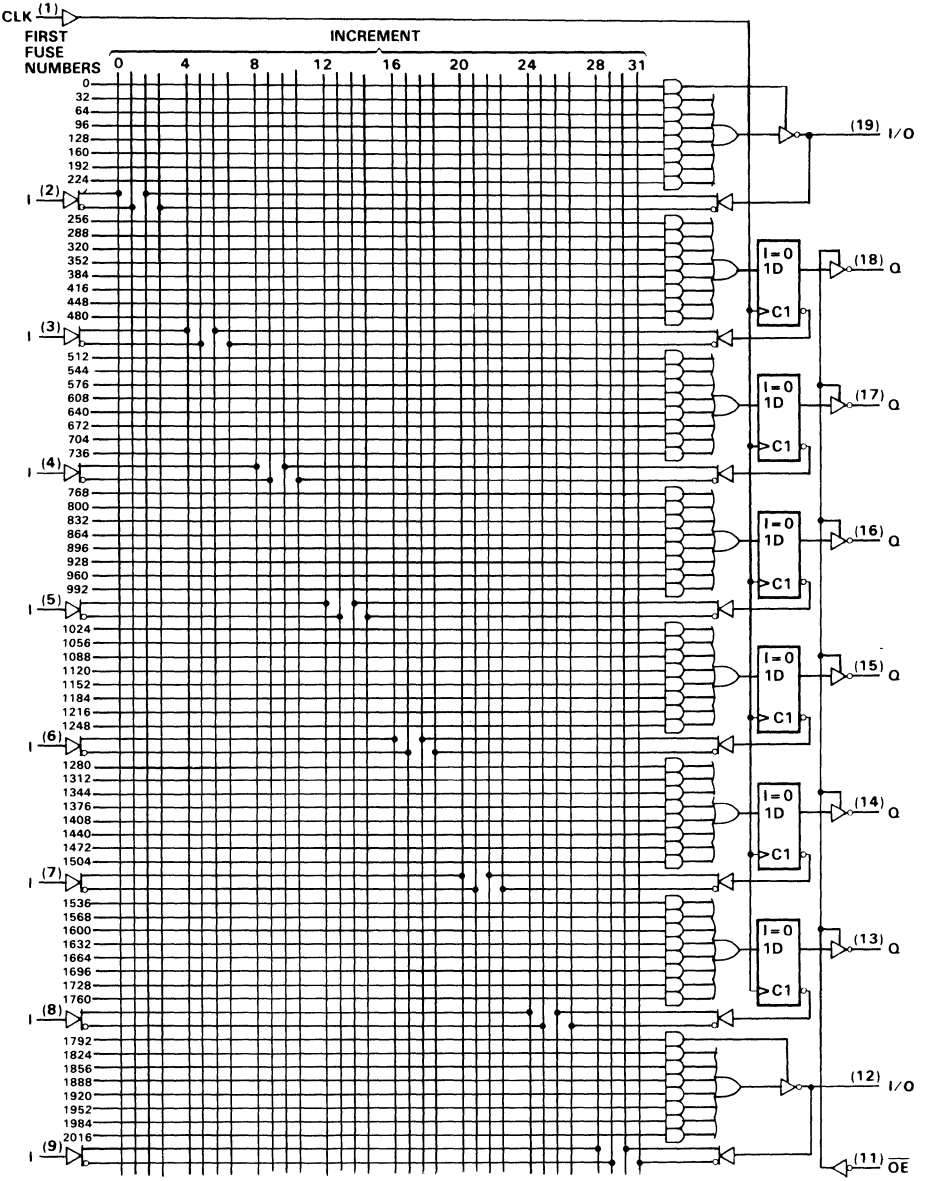
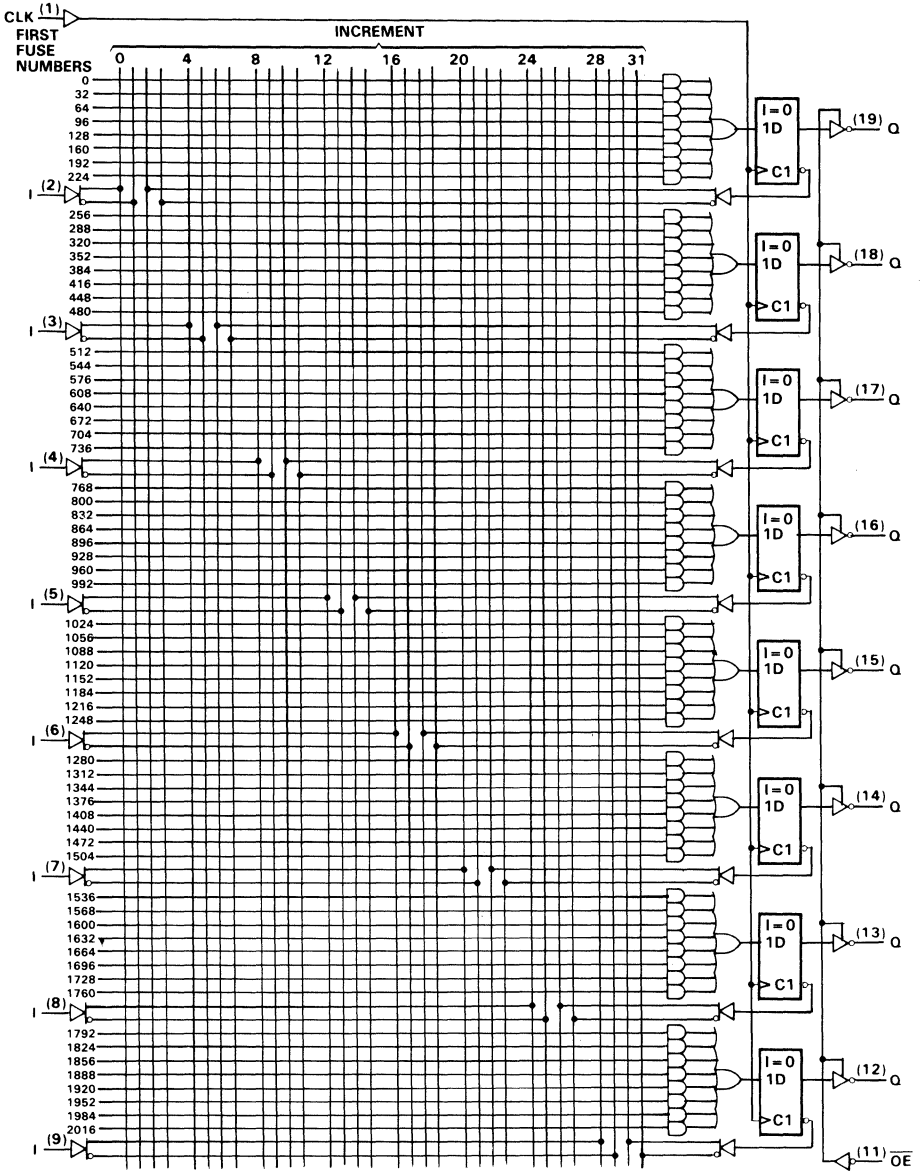


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{OE}$ input	2		5.5	V
		All others	2		5.5	
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
T_A	Operating free-air temperature		−55		125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V, I_{OL} = −12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
	I/O ports					−100	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V				0.2	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V, V_I = 2.7 V				100	μA
	All others					25	
I_{IL}		V_{CC} = 5.5 V, V_I = 0.4 V	$\overline{OE}$ input			−0.2	mA
			All others			−0.1	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0.5 V		−30		−250	mA
I_{CC}		V_{CC} = 5.5 V, V_I = 0 V, Outputs open			75	180	mA

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	25	MHz
t_w	Pulse duration (see Note 2)	Clock high	15		ns
		Clock low	20		
t_{su}	Setup time, input or feedback before CLK↑		25		ns
t_h	Hold time, input or feedback after CLK↑		0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}				25	45		MHz
t_{pd}	I, I/O,	O, I/O			15	30	ns
t_{pd}	CLK↑	Q	R1 = 390 Ω,		10	20	ns
t_{en}	$\overline{OE}$↓	Q	R2 = 750 Ω,		15	25	ns
t_{dis}	$\overline{OE}$↑	Q	See Figure 1		10	25	ns
t_{en}	I, I/O	O, I/O			14	30	ns
t_{dis}	I, I/O	O, I/O			13	30	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
	I/O ports					−100	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V				0.2	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V, V_I = 2.7 V				100	μA
	All others					25	
I_{IL}		V_{CC} = 5.5 V, V_I = 0.4 V	$\overline{OE}$ input			−0.2	mA
			All others			−0.1	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0.5 V		−30		−250	mA
I_{CC}		V_{CC} = 5.5 V, V_I = 0 V, Outputs open			75	90	mA

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	16	MHz
t_w	Pulse duration, (see Note 2)	Clock high	25		ns
		Clock low	25		
t_{su}	Setup time, input or feedback before CLK↑		35		ns
t_h	Hold time, input or feedback after CLK↑		0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}				16	25		MHz
t_{pd}	I, I/O,	O, I/O			25	40	ns
t_{pd}	CLK↑	Q	R1 = 390 Ω,		11	35	ns
t_{en}	$\overline{OE}$↓	Q	R2 = 750 Ω,		20	35	ns
t_{dis}	$\overline{OE}$↑	Q	See Figure 1		11	30	ns
t_{en}	I, I/O	O, I/O			25	40	ns
t_{dis}	I, I/O	O, I/O			25	35	ns

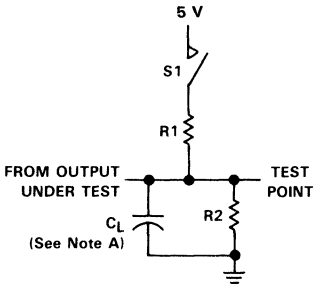
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

programming information

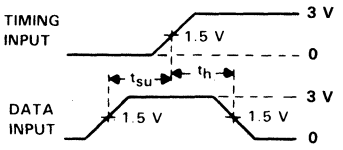
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

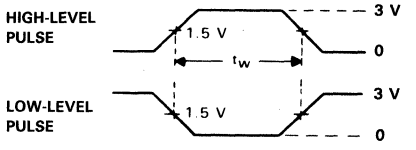
PARAMETER MEASUREMENT INFORMATION



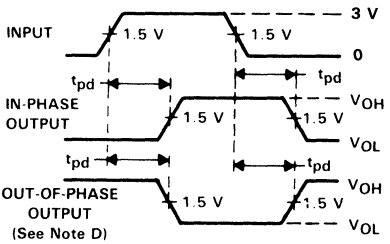
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



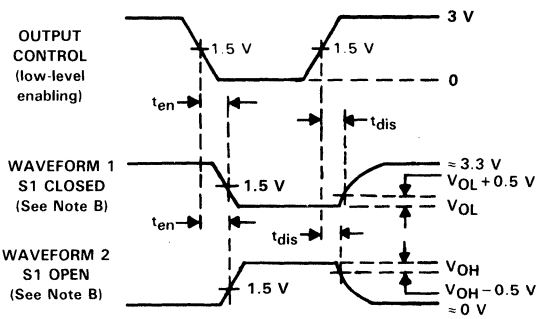
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 1

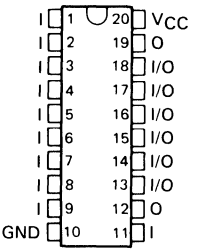
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TIBPAD16N8-7C
HIGH-PERFORMANCE PROGRAMMABLE ADDRESS DECODER

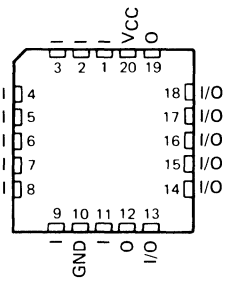
D3085, JANUARY 1988—REVISED AUGUST 1989

- **Very-High-Speed Address Decoder (Ideal for Use with High Speed Processors)**
- **I/O Propagation Delay: 7 ns Max**
- **Field Programmable on Standard PLD Programmers**
- **Fully TTL Compatible**
- **Security Fuse Prevents Unauthorized Duplication**
- **Dependable Texas Instruments Quality and Reliability**
- **Potential Applications**
  - **Address Decoders**
  - **Code Detectors**
  - **Peripheral Selectors**
  - **Fault Monitors**
  - **Machine State Decoders**

J OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TIBPAD16N8 is a very-high-speed Programmable Address Decoder featuring 7 ns maximum propagation delay, the highest speed in the TTL programmable logic family. The TIBPAD16N8 utilizes the IMPACT-X™ process and proven titanium-tungsten fuse technology to provide reliable, high performance substitutes for conventional TTL logic.

The TIBPAD16N8 contains 10 dedicated inputs and 8 outputs. Each output has two product terms, one of which is used to enable the inverting buffer associated with the respective output. Six of the outputs are I/O ports, the remaining two are dedicated outputs. Each of the six I/O ports can be individually programmed as an input or an output; this allows the device to be used for functions requiring up to 16 inputs and 2 outputs or 10 inputs and 8 outputs.

The TIBPAD16N8 is supplied with all six I/O ports in the input configuration (output buffers in the high-impedance state). If an I/O port is selected to be an output, it must be programmed accordingly. It is recommended that all unused outputs on this device remain in the three-state condition for better noise immunity.

The TIBPAD16N8-7C is characterized for operation from 0°C to 75°C.

IMPACT-X is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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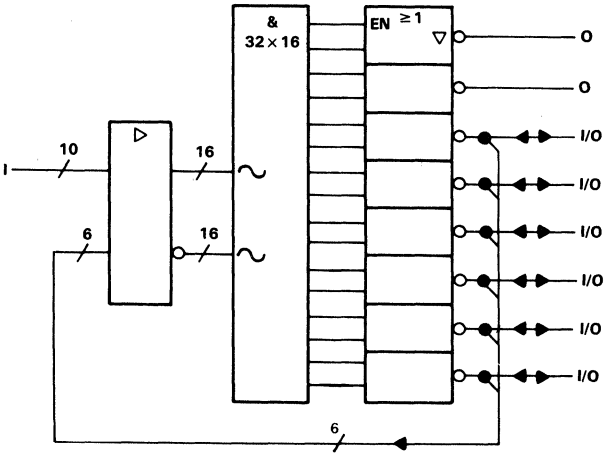
functional block diagram (positive logic)



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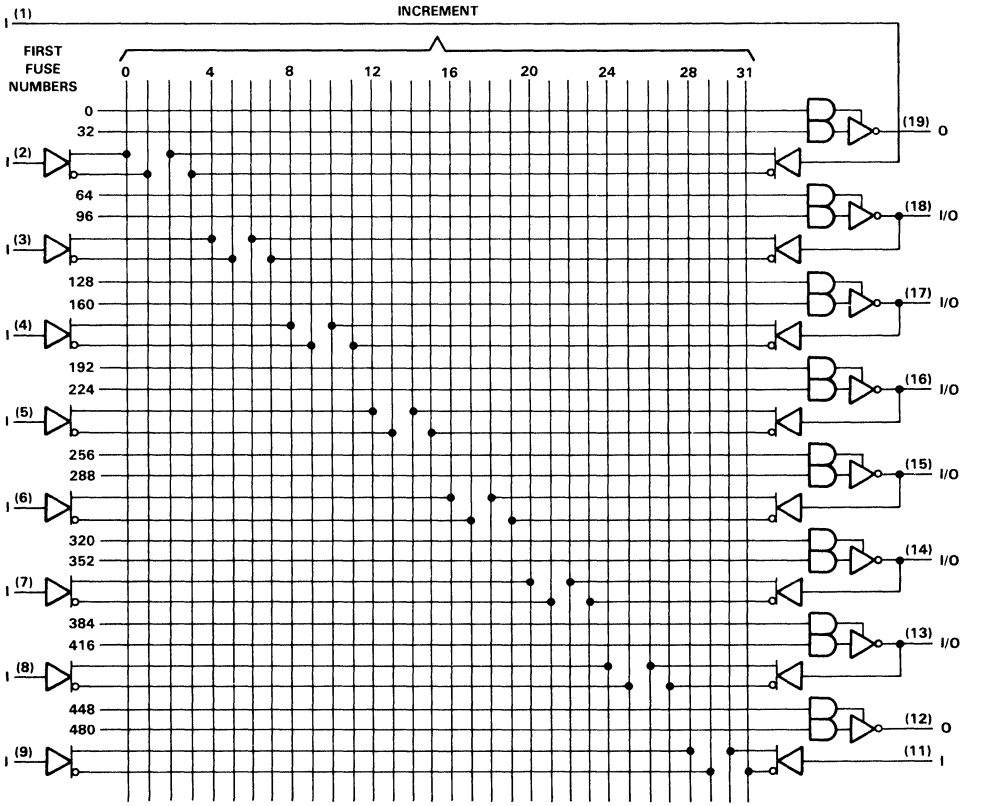
logic diagram (positive logic)



Fuse number = First Fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−3.2	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V, I_I = −18 mA			−1.5	V
V_{OH}	V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3		V
V_{OL}	V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_I	V_{CC} = 5.25 V, V_I = 5.5 V			0.2	mA
I_{OZH}‡	V_{CC} = 5.25 V, V_O = 2.7 V			0.1	mA
I_{OZL}‡	V_{CC} = 5.25 V, V_O = 0.4 V			−0.1	mA
I_{IH}‡	V_{CC} = 5.25 V, V_I = 2.7 V			25	μA
I_{IL}‡	V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
I_O§	V_{CC} = 5 V, V_O = 0.5 V	−30	−70	−130	mA
I_{CC}	V_{CC} = 5.25 V, V_I = 0, Outputs open		120	180	mA
C_I	V_I = 2 V		5		pF
C_o	V_O = 2 V		6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}.
§ This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics with two outputs switching (typical PAD mode) over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	I, I/O	O, I/O 2 outputs switching	R1 = 200 Ω, R2 = 390 Ω See Figure 1	2	5	7	ns
t_{en}	I, I/O	O, I/O		3	8	10	ns
t_{dis}	I, I/O	O, I/O		3	8	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C

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programming information

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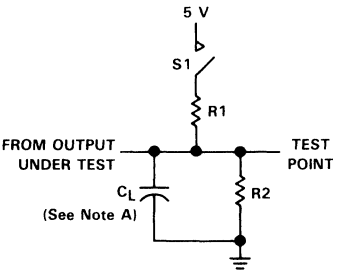
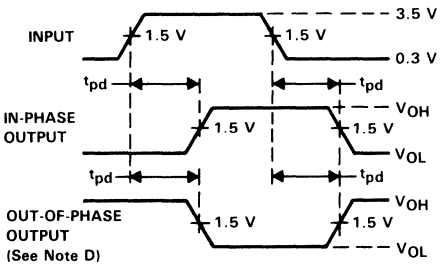
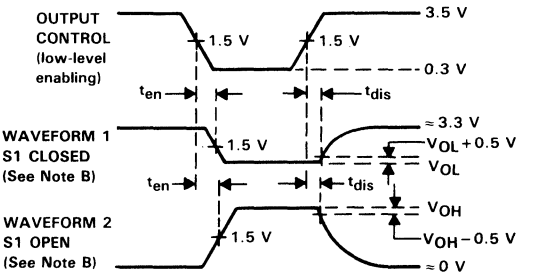
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

WORST CASE MULTIPLE OUTPUT SWITCHING CHARACTERISTICS

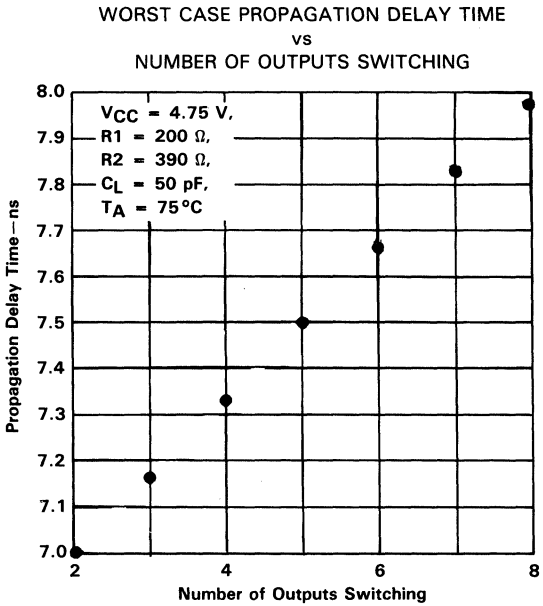


FIGURE 2

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

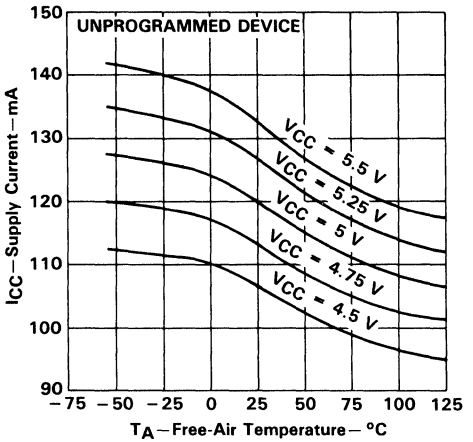


FIGURE 3

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

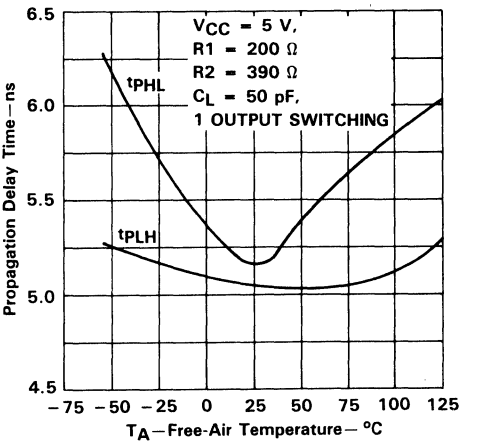


FIGURE 4

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

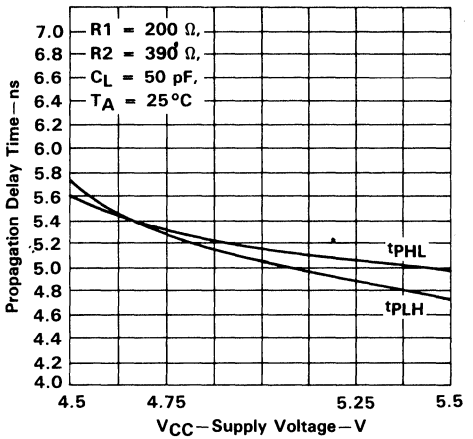


FIGURE 5

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

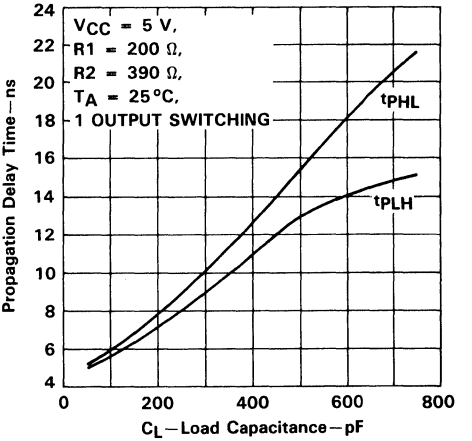


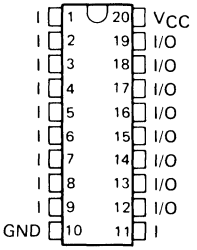
FIGURE 6

HIGH-PERFORMANCE PROGRAMMABLE ADDRESS DECODER/NAND ARRAY

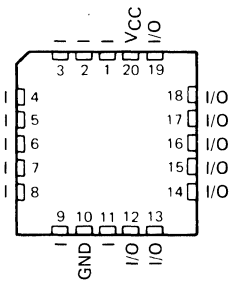
D3086, DECEMBER 1987 – REVISED AUGUST 1988

- **Very-High-Speed Address Decoder (Ideal for Use with High Speed Processors)**
- **I/O Propagation Delay: 6 ns Max**
- **Suitable for High Speed NAND-NAND Logic Implementation**
- **Field Programmable on Standard PLD Programmers**
- **Fully TTL Compatible**
- **Security Fuse Prevents Unauthorized Duplication**
- **Dependable Texas Instruments Quality and Reliability**
- **Potential Applications**
  - **Address Decoders**
  - **Random Logic (NAND-NAND)**
  - **Code Detectors**
  - **Peripheral Selectors**
  - **Fault Monitors**
  - **Machine State Decoders**

J OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TIBPAD18N8-6C is a very-high-speed Programmable Address Decoder featuring 6-ns maximum propagation delay, the highest speed in the TTL programmable logic family. The TIBPAD18N8 uses the IMPACT-X™ process and proven titanium-tungsten fuse technology to provide reliable, high-performance substitutes for conventional TTL logic.

The TIBPAD18N8-6C contains 10 dedicated inputs and 8 product terms, each followed by an inverting buffer. Each of the eight buffers can be individually programmed so that the corresponding pin can function either as an input or output, depending on the state of the fuse controlling the output buffer, as indicated by Table 1. This allows the device to be used for functions requiring up to 17 inputs and a single output or down to 10 inputs and 8 outputs.

A high-speed feedback path, which does not go through the output buffer, is provided to offer higher performance operation in designs where feedback is required. The architectural fuse on the internal multiplexer is used for the selection of this path (see Table 2). This makes the TIBPAD18N8-6C ideal for the implementation of a very fast NAND-NAND logic. The TIBPAD18N8 is supplied with all eight output buffers disabled thus establishing all programmable input/output lines as inputs. If an I/O line is selected to be an output it must be programmed accordingly.

The TIBPAD18N8-6C is characterized for operation from 0°C to 75°C.

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functional block diagram (positive logic)

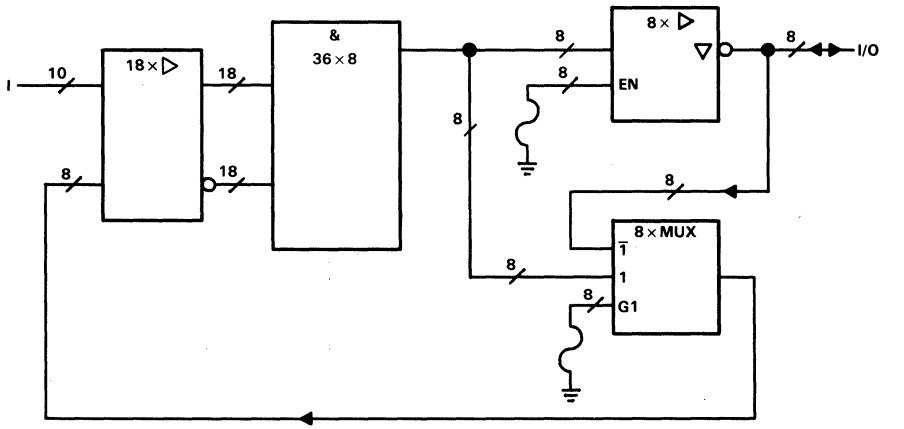

Table 1. Output Buffer Programming

ARCHITECTURAL FUSE	OPERATION
Intact	Input (Output Buffer in 3-State)
Blown	Output

Table 2. I/O Multiplexer Programming

ARCHITECTURAL FUSE	OPERATION
Intact	Output Buffer Feedback
Blown	Fast Feedback (pre-output buffer)

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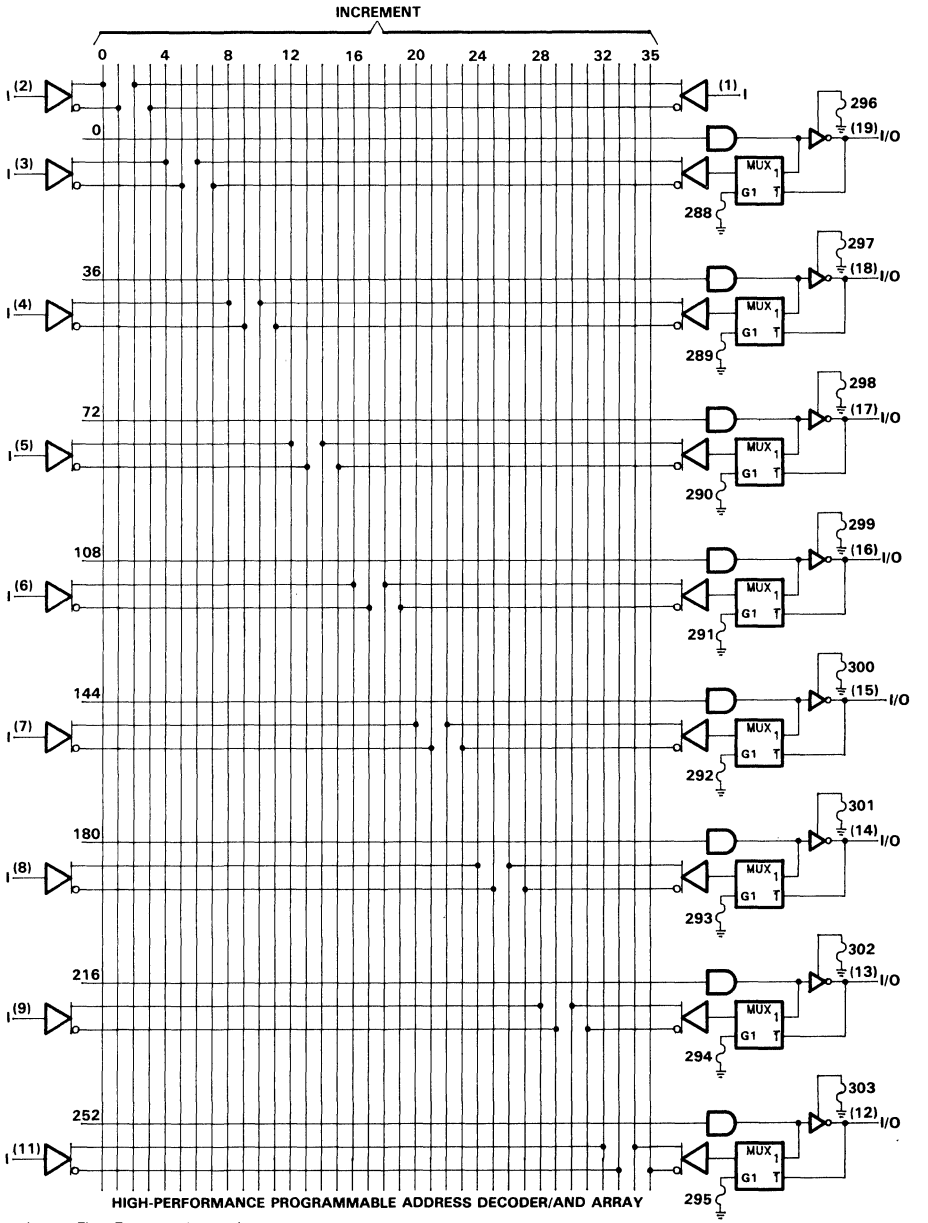
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

logic diagram (positive logic)



Fuse number = First Fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)	2			V
V_{IL}	Low-level input voltage (see Note 2)			0.8	V
I_{OH}	High-level output current			−3.2	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V, I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3		V
V_{OL}	V_{CC} = 4.75 V, I_{OL} = 24 mA		0.37	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
I_{OZL}‡	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.25 V, V_I = 5.5 V			20	μA
I_{IH}	V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
I_O§	V_{CC} = 5.25 V, V_O = 0.5 V	−30	−75	−130	mA
I_{CC}	V_{CC} = 5.25 V, V_I = 4.5 V		145	180	mA
C_i	V_I = 2 V		5		pF
C_o	V_O = 2 V		6		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	I (2 outputs switching)	O (no feedback)	R1 = 200 Ω, R2 = 390 Ω, C_L = 50 pF, See Figure 1	2	4.5	6	ns
		O (with 1 fast feedback path)		3.5	7	10	ns
		O (with 2 fast feedback paths)		5	9.5	14	ns
		O (with 3 fast feedback paths)		6.5	12	18	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worse case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}.
§ This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

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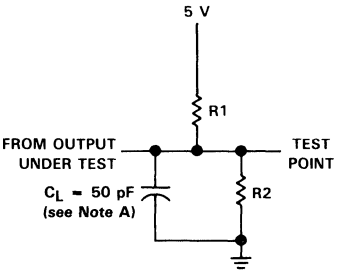
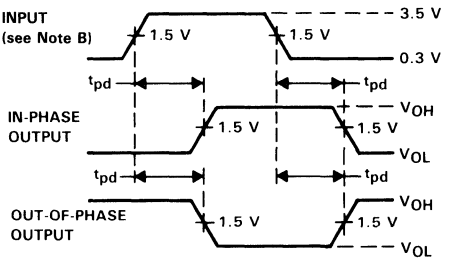
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.

FIGURE 1

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

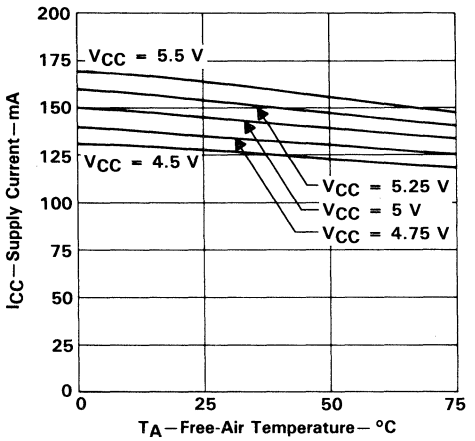


FIGURE 2

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

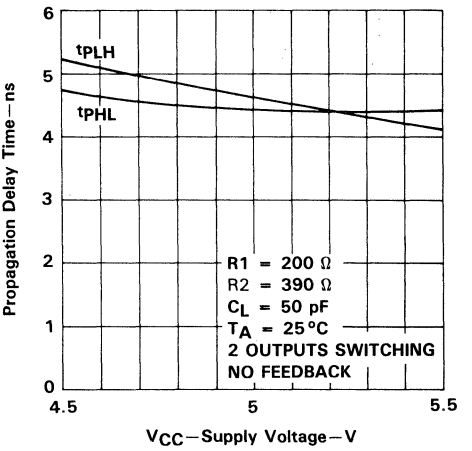


FIGURE 3

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

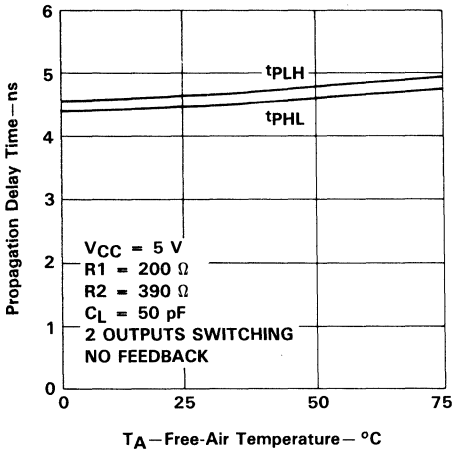


FIGURE 4

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

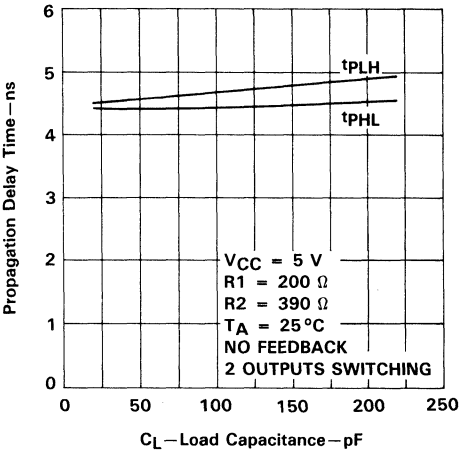


FIGURE 5

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TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
NUMBER OF FAST FEEDBACK PATHS

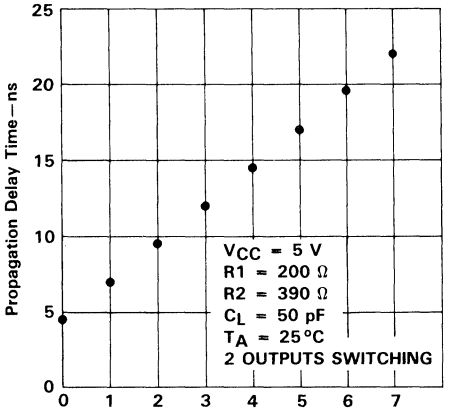


FIGURE 6

WORST-CASE PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

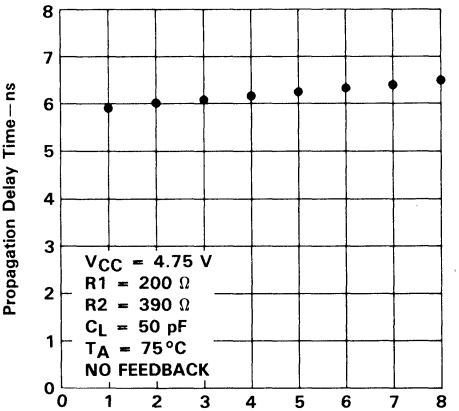


FIGURE 7

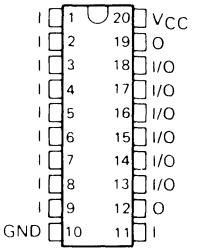
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

D3359, OCTOBER 1989

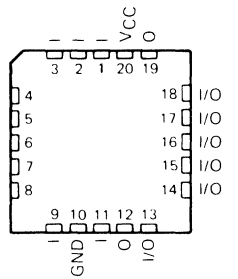
- **High-Performance Operation:**
  - f_{max} (no feedback)
    - TIBPAL16R'-7M Series . . . 100 MHz
    - TIBPAL16R'-5C Series . . . 125 MHz
  - f_{max} (internal feedback)
    - TIBPAL16R'-7M Series . . . 100 MHz
    - TIBPAL16R'-5C Series . . . 125 MHz
  - f_{max} (external feedback)
    - TIBPAL16R'-7M Series . . . 74 MHz
    - TIBPAL16R'-5C Series . . . 115 MHz
  - Propagation Delay
    - TIBPAL16L'-7M . . . 7 ns Max
    - TIBPAL16L'-5C . . . 5 ns Max
- **Functionally Equivalent, but Faster than Existing 20-Pin PALs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

PRODUCT PREVIEW

description

These Programmable Array Logic devices feature the highest speed yet achieved in a bipolar PAL circuit. This family of PALs is 100% functionally and pin-for-pin compatible with the industry standard 'PAL16L8, 'PAL16R4, 'PAL16R6, and 'PAL16R8. The Texas Instruments IMPACT-X™ (Enhanced Implanted Advanced Composed Technology) fabrication process has been employed to ensure this ultra-high-performance operation. This process combines the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL16' C series is characterized for operation from 0°C to 75°C.

IMPACT-X™ is a trademark of Texas Instruments Incorporated.
PAL® is a registered trademark of Monolithic Memories, Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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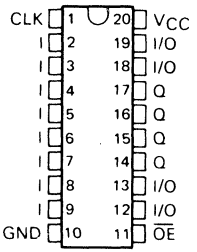
PRODUCT PREVIEW

TIBPAL16R4'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R4'
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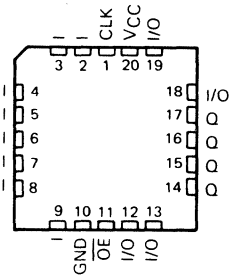
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL16R6'
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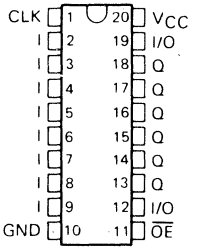
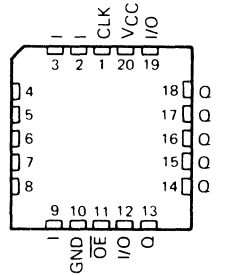
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL16R8'
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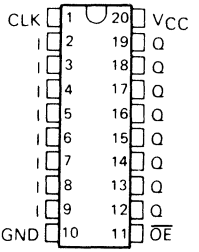
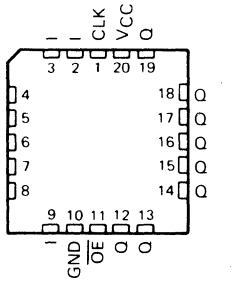
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)

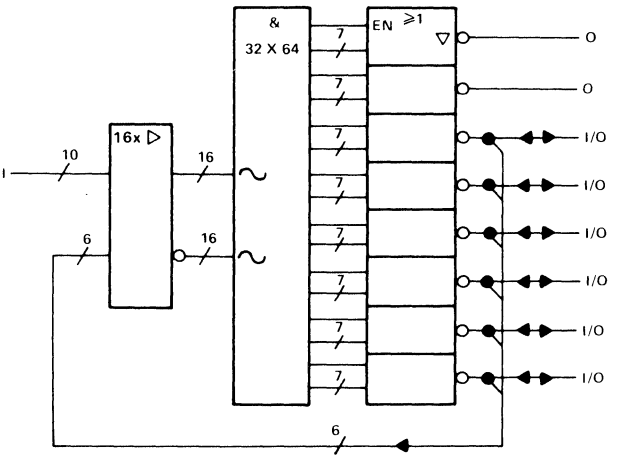


Pin assignments in operating mode

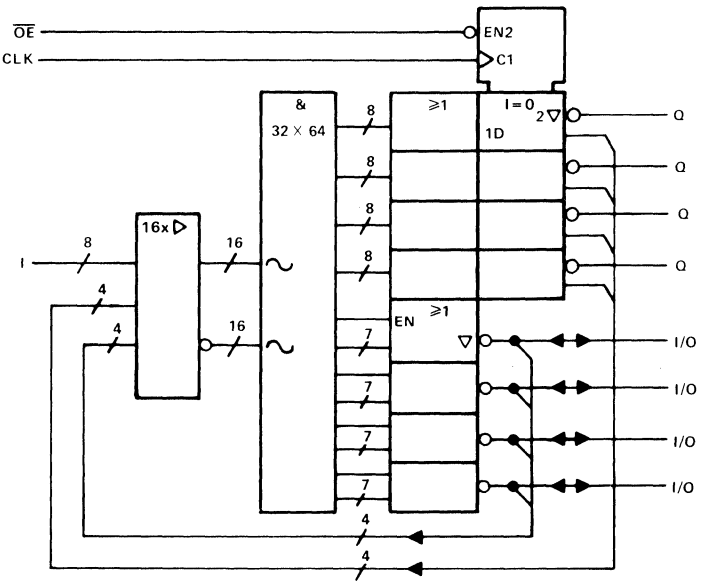
PRODUCT PREVIEW

functional block diagrams (positive logic)

'PAL16L8



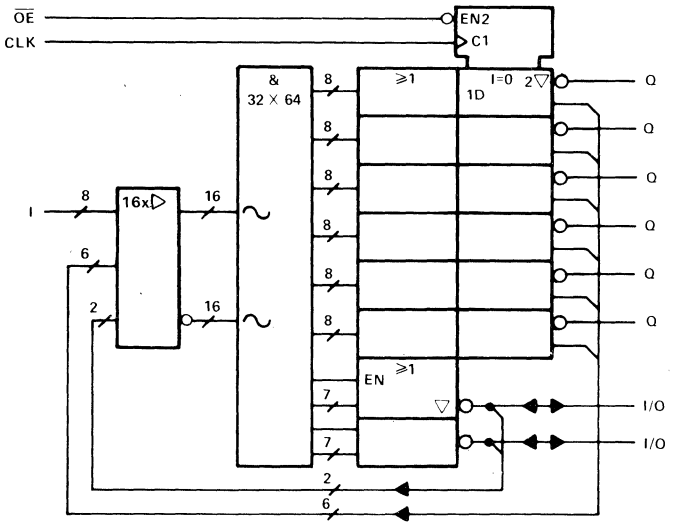
'PAL16R4



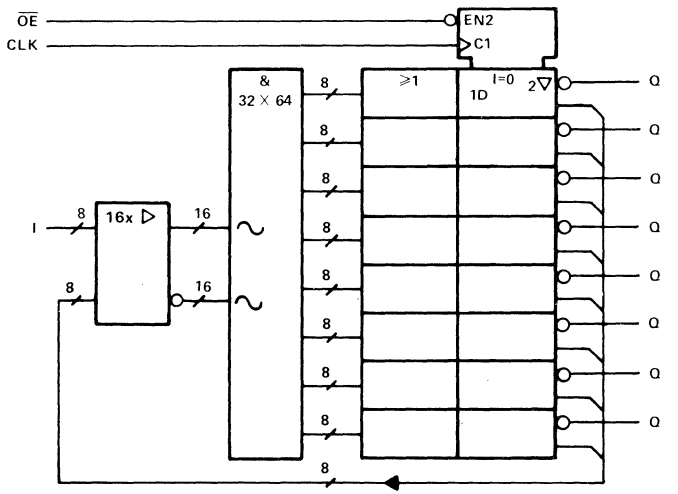
~ denotes fused inputs

functional block diagrams (positive logic)

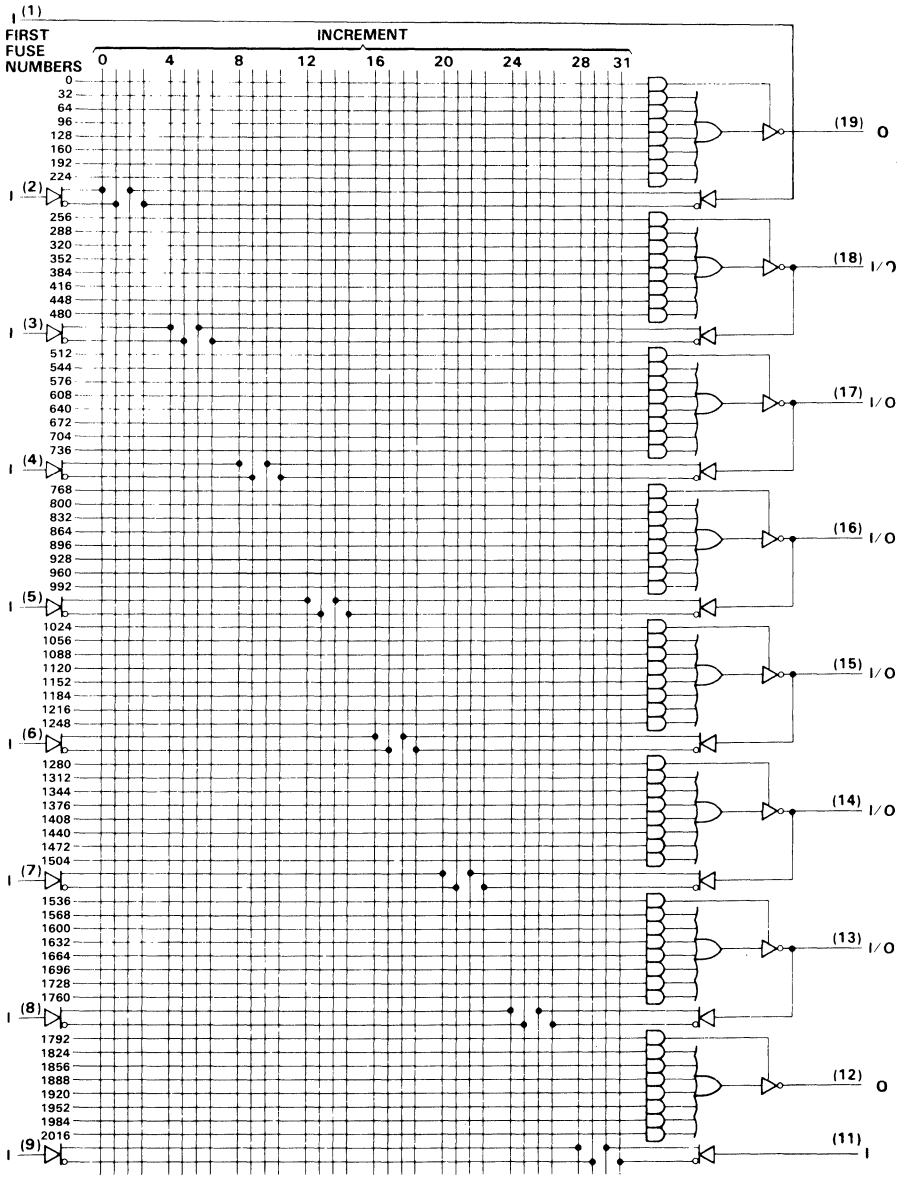
'PAL16R6



'PAL16R8

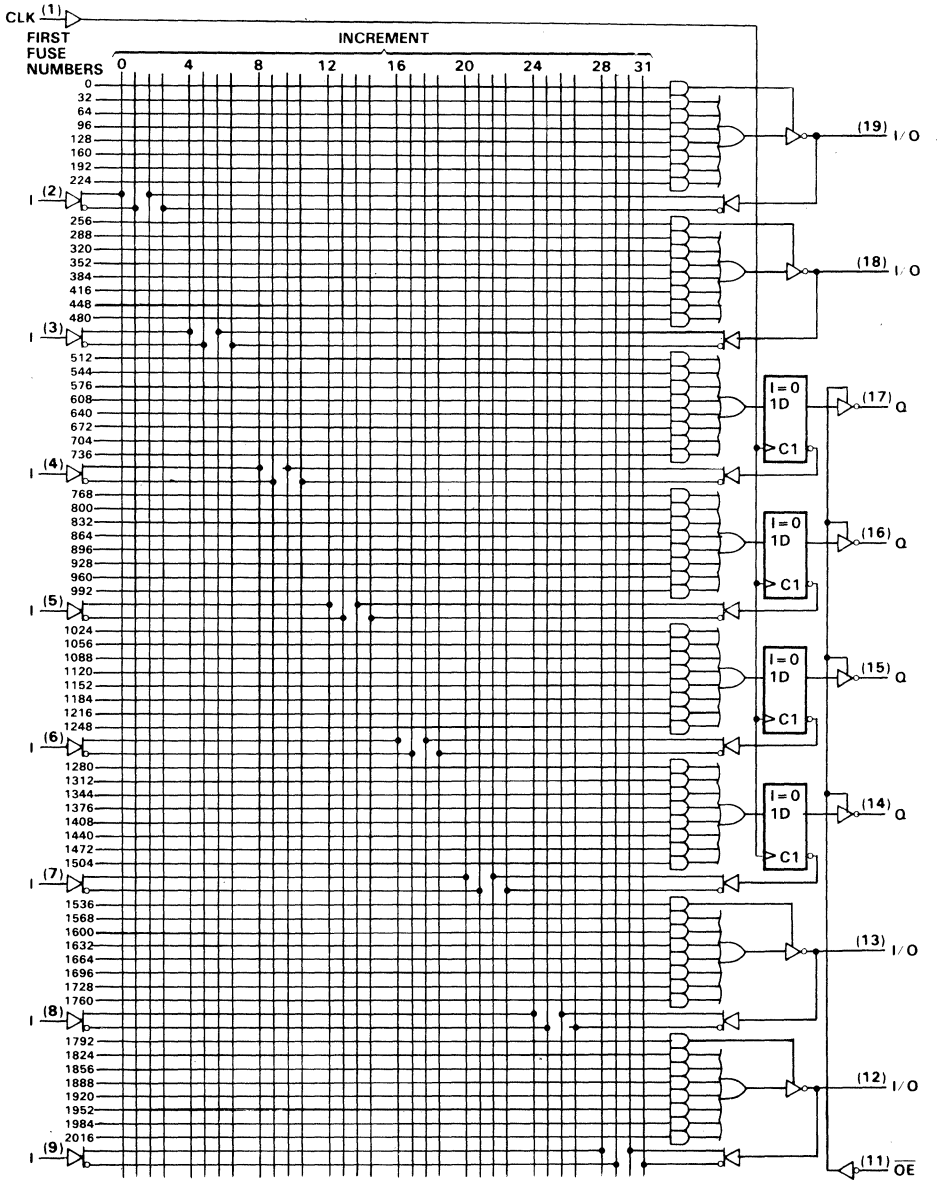


∼ denotes fused inputs

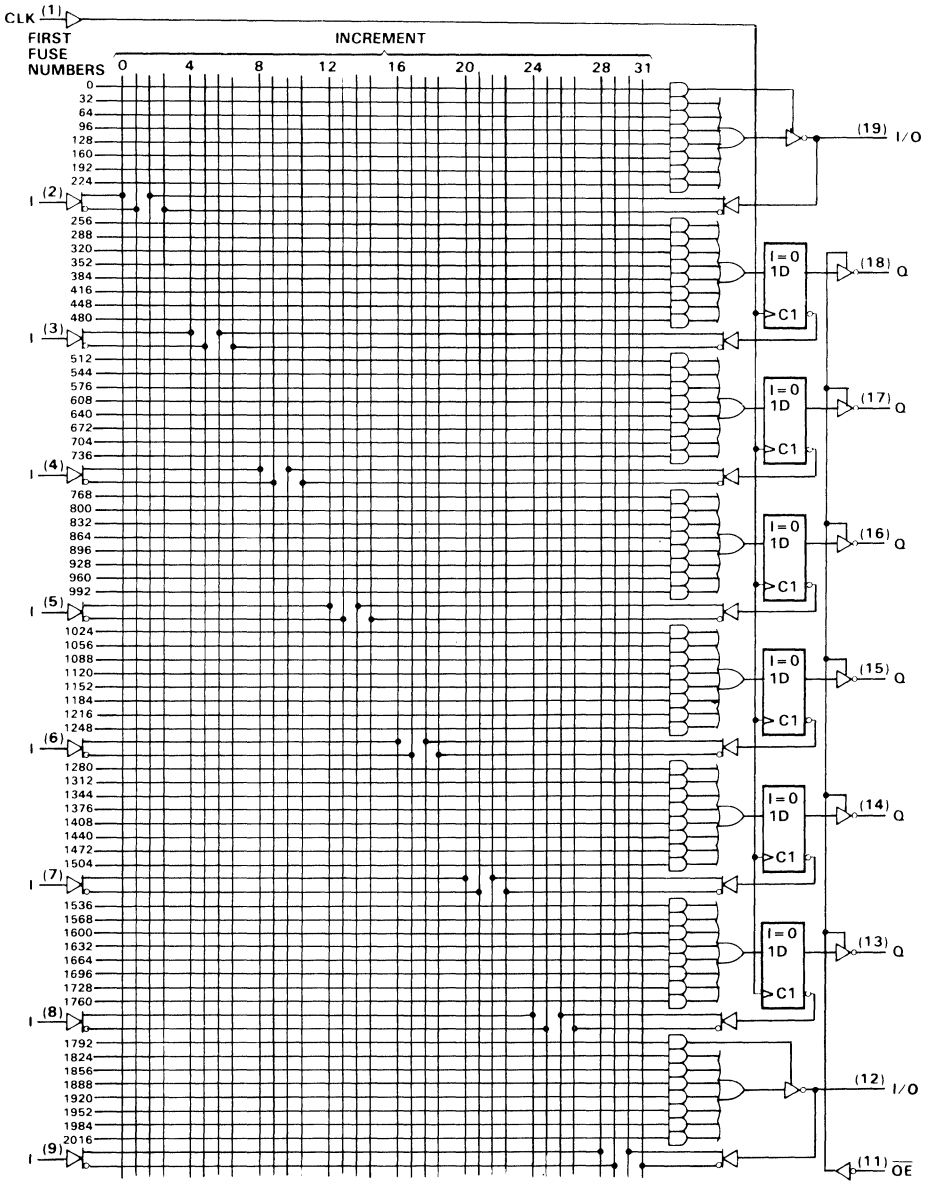


Fuse number = First Fuse number + Increment

PRODUCT PREVIEW

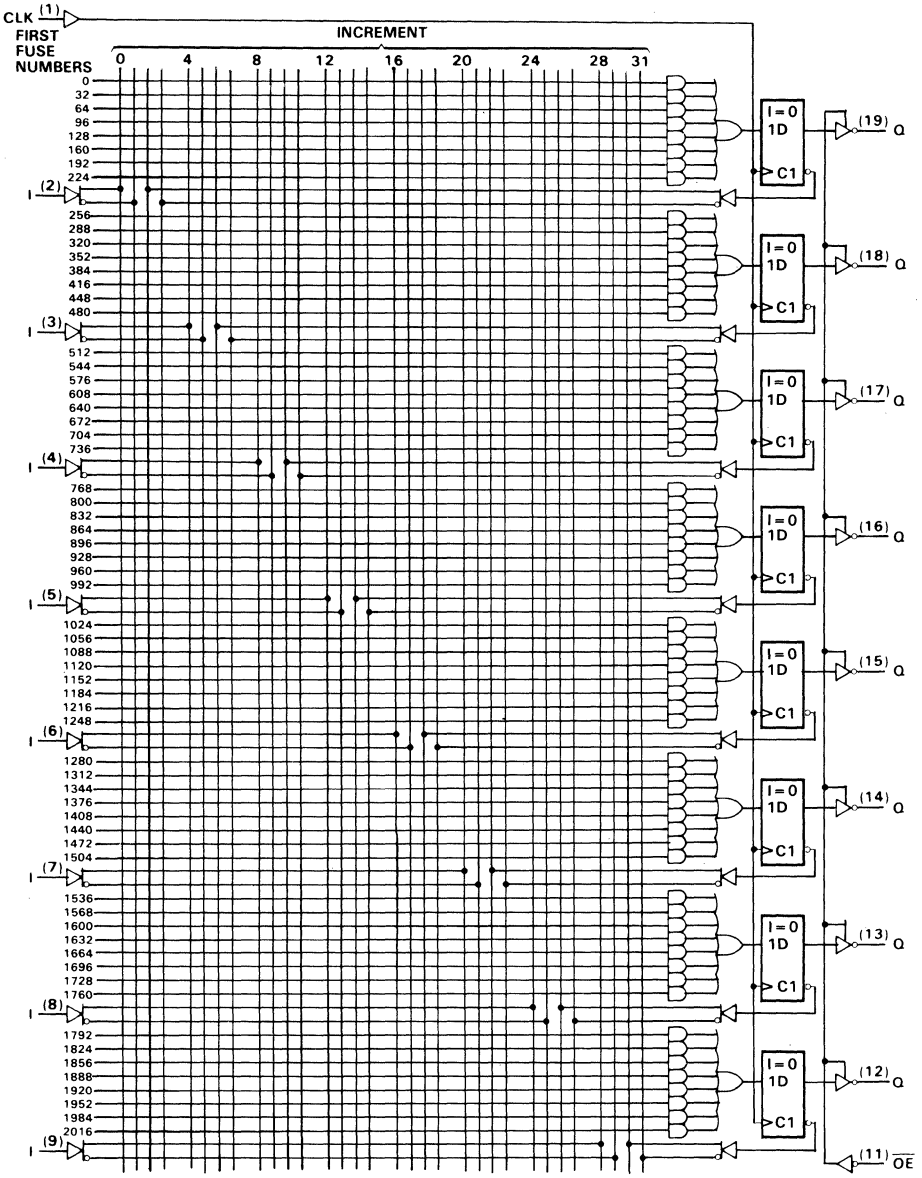


Fuse number = First Fuse number – Increment



Fuse number = First Fuse number + Increment

PRODUCT PREVIEW



Fuse number = First Fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		100	MHz
t_w	Pulse duration, clock (see Note 2)	High	6			ns
		Low	6			
t_{su}	Setup time, input or feedback before CLK↑		7			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.3	0.5	V
I_{OZH}‡	O, Q outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}‡	O, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				−20	μA
	I/O ports						−250	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	μA
	All others						25	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.08	−0.25	mA
I_{OS}§		V_{CC} = 5 V,	V_O = 0.5 V		−30	−70	−130	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs open,	T_A = 25°C and 125°C		120	180	mA
		V_I = 0 V,	$\overline{OE}$ = V_{IH}	T_A = −55°C				
C_i		f = 1 MHz,	V_I = 2 V					pF
C_o		f = 1 MHz,	V_O = 2 V					pF
C_{clk}		f = 1 MHz,	V_{CLK} = 2 V					pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.

PRODUCT PREVIEW

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted) (see Figure 5)

PARAMETER	FROM	TO	MIN	TYP†	MAX	UNIT
f_{max}‡	Without feedback		100			MHz
	With internal feedback (counter configuration)		100			
	With external feedback		74			
t_{pd}	I, I/O	O, I/O			7	ns
t_{pd}	CLK↑	Q			6	ns
t_{pd}§	CLK↑	Feedback input			3	ns
t_{en}	OE↓	Q			7.5	ns
t_{dis}	OE↑	Q			7.5	ns
t_{en}	I, I/O	O, I/O			8.5	ns
t_{dis}	I, I/O	O, I/O			8.5	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡See section on f_{max} specifications.
§This parameter applies to TIBPAL16R4′ and TIBPAL16R6′ only (see Figure 2 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration, clock (see Note 2)	High	4			ns
		Low	4			
t_{su}	Setup time, input or feedback before CLK↑		4			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA		−0.8	−1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.7 V			100	μA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V			−100	μA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			0.2	mA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.7 V			25	μA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V		−0.08	−0.25	mA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0.5 V	−30	−70	−130	mA
I_{CC}	V_{CC} = 5.25 V, Outputs open	V_I = 0 V,		120	180	mA
C_i	f = 1 MHz,	V_I = 2 V				pF
C_o	f = 1 MHz,	V_O = 2 V				pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V				pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.

PRODUCT PREVIEW

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted) (see Figure 6)

PARAMETER	FROM	TO	MIN	TYP†	MAX	UNIT
f_{max}‡	Without feedback		125			MHz
	With internal feedback (counter configuration)		125			
	With external feedback		115			
t_{pd}	I, I/O	O, I/O			5	ns
t_{pd}	CLK↑	Q			4	ns
t_{pd}§	CLK↑	Feedback input			3	ns
t_{en}	OE↓	Q			5.5	ns
t_{dis}	OE↑	Q			5.5	ns
t_{en}	I, I/O	O, I/O			6.5	ns
t_{dis}	I, I/O	O, I/O			6.5	ns
t_{skew}¶	Skew between registered outputs					ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡See section on f_{max} specifications.
§This parameter applies to TIBPAL16R4' and TIBPAL16R6' only (see Figure 2 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.
¶This parameter is the measurement of the difference between the fastest and slowest t_{pd} (CLK-to-Q) observed when multiple registered outputs are switching in the same direction.

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programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

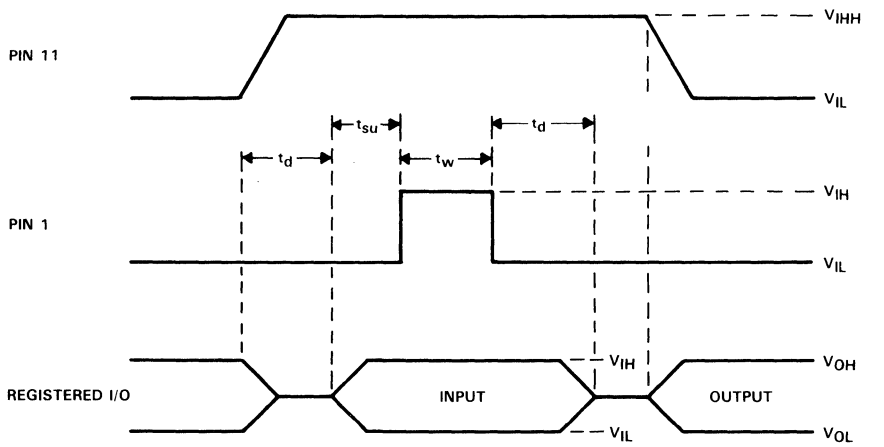
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 3)



NOTE 3: $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

PRODUCT PREVIEW

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 1

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su}+t_h$). However, the minimum f_{max} is determined by the minimum clock period ($t_w$high + $t_w$low).

Thus, f_{max} without feedback $= \dfrac{1}{(t_w \text{ high} + t_w \text{ low})}$ or $\dfrac{1}{(t_{su}+t_h)}$

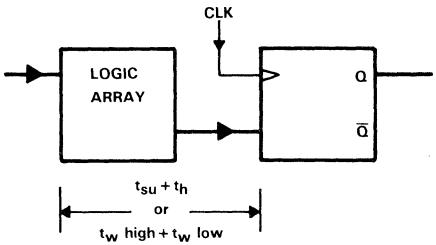


FIGURE 1. f_{max} WITHOUT FEEDBACK

f_{max} with internal feedback, see Figure 2

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus, f_{max} with internal feedback $= \dfrac{1}{(t_{su}+t_{pd} \text{ CLK-to-FB})}$

Where t_{pd} CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

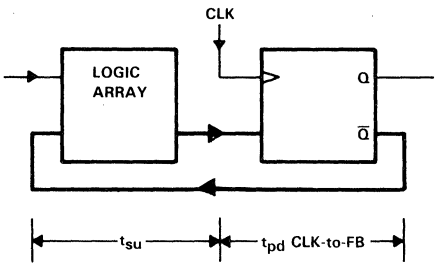


FIGURE 2. f_{max} WITH INTERNAL FEEDBACK

f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 3

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input and setup time for the external signals ($t_{su} + t_{pd}$ CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd} \text{ CLK-to-Q})}$.

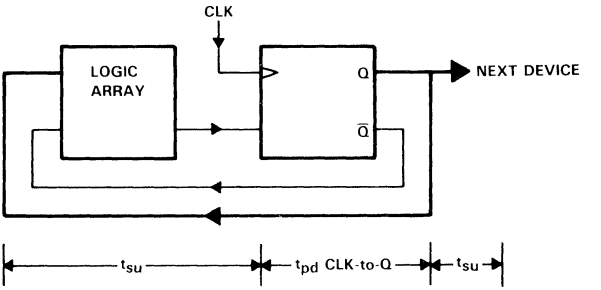


FIGURE 3. f_{max} WITH EXTERNAL FEEDBACK

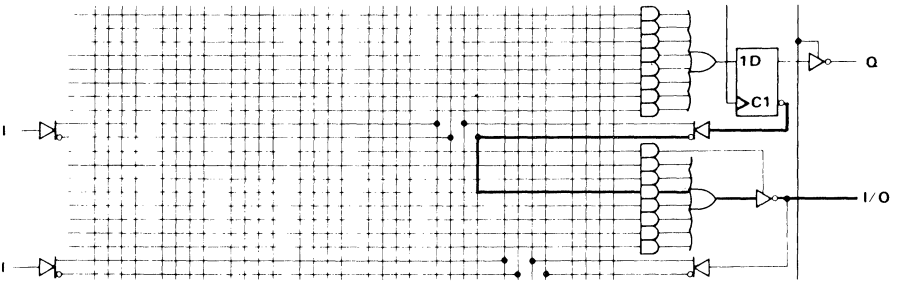
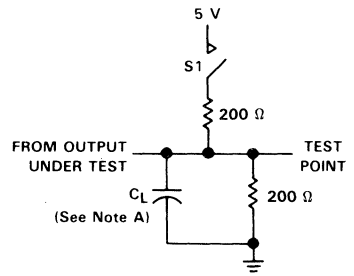
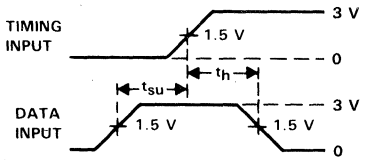


FIGURE 4. PROPAGATION DELAY FROM CLK↑ to I/O, THRU LOGIC ARRAY

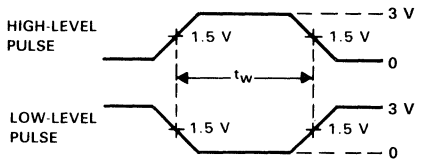
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

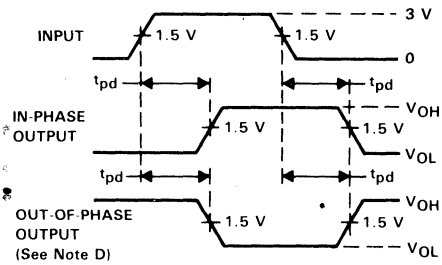




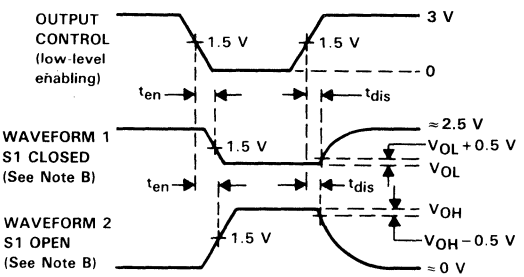
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}. 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and t_f = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 5

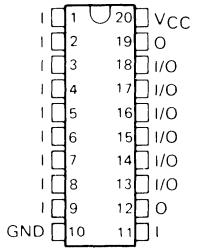
TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M
TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C
HIGH-PERFORMANCE *IMPACT-X™ PAL®* CIRCUITS

D3115, MAY 1988—REVISED OCTOBER 1989

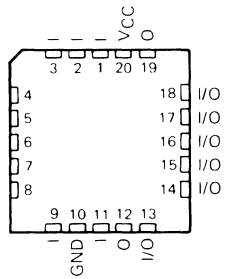
- High-Performance Operation:
  - f_{max} (no feedback)
    - TIBPAL16R'-7C Series . . . 100 MHz
    - TIBPAL16R'-10M Series . . . 62.5 MHz
  - f_{max} (internal feedback)
    - TIBPAL16R'-7C Series . . . 100 MHz
    - TIBPAL16R'-10M Series . . . 62.5 MHz
  - f_{max} (external feedback)
    - TIBPAL16R'-7C Series . . . 74 MHz
    - TIBPAL16R'-10M Series . . . 55.5 MHz
  - Propagation Delay
    - TIBPAL16L'-7C . . . 7 ns Max
    - TIBPAL16L'-10M . . . 10 ns Max
- Functionally Equivalent, but Faster than Existing 20-Pin PALs
- Preload Capability on Output Registers Simplifies Testing
- Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Security Fuse Prevents Duplication
- Dependable Texas Instruments Quality and Reliability

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom-functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL16' C series is characterized for operation from 0°C to 75°C.

IMPACT-X™ is a trademark of Texas Instruments Incorporated.
PAL® is a registered trademark of Monolithic Memories, Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

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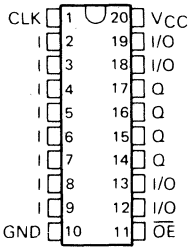
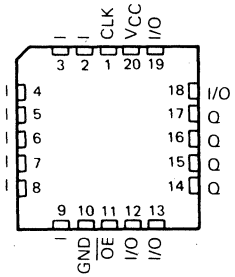
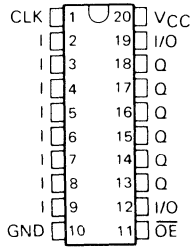
TIBPAL16R4'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



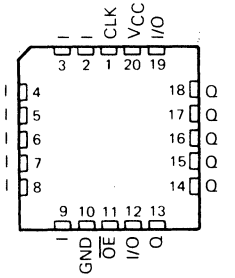
TIBPAL16R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



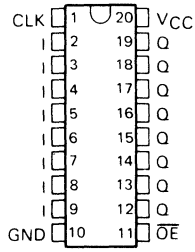
TIBPAL16R6'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



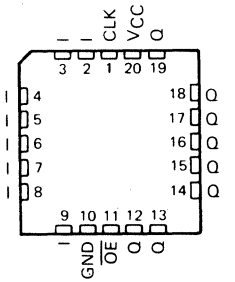
TIBPAL16R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

TEXAS INSTRUMENTS
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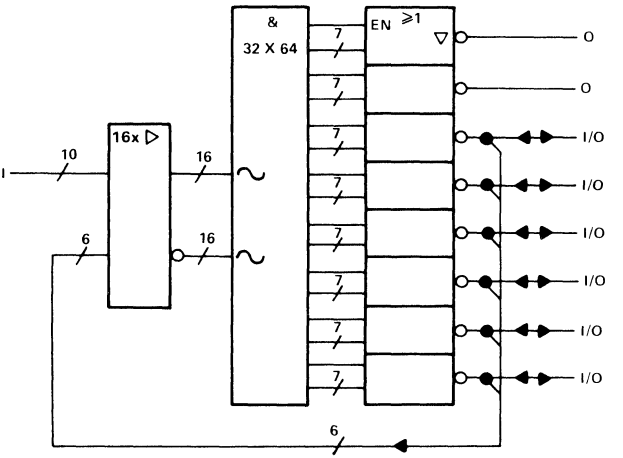
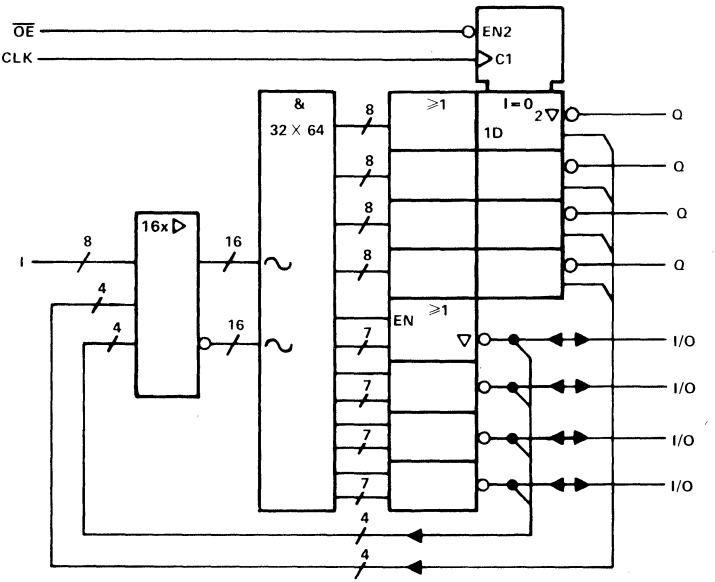
functional block diagrams (positive logic)

'PAL16L8



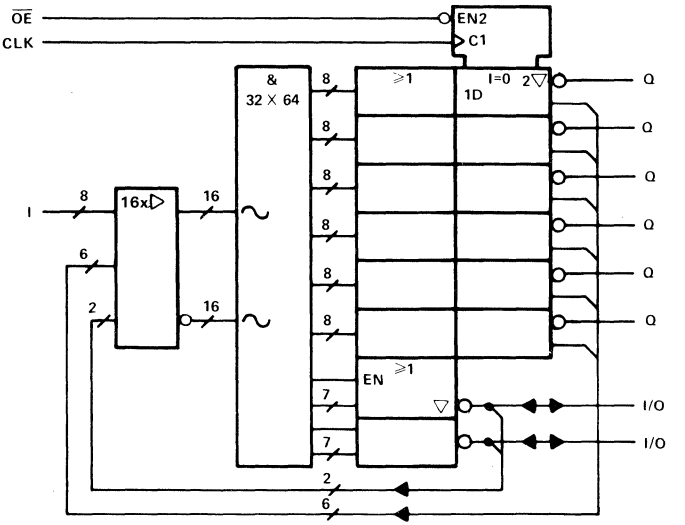
'PAL16R4



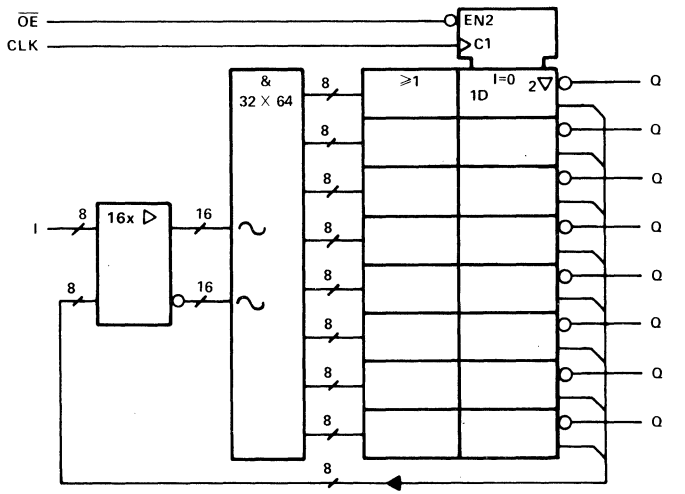
∼ denotes fused inputs

functional block diagrams (positive logic)

'PAL16R6



'PAL16R8



~ denotes fused inputs

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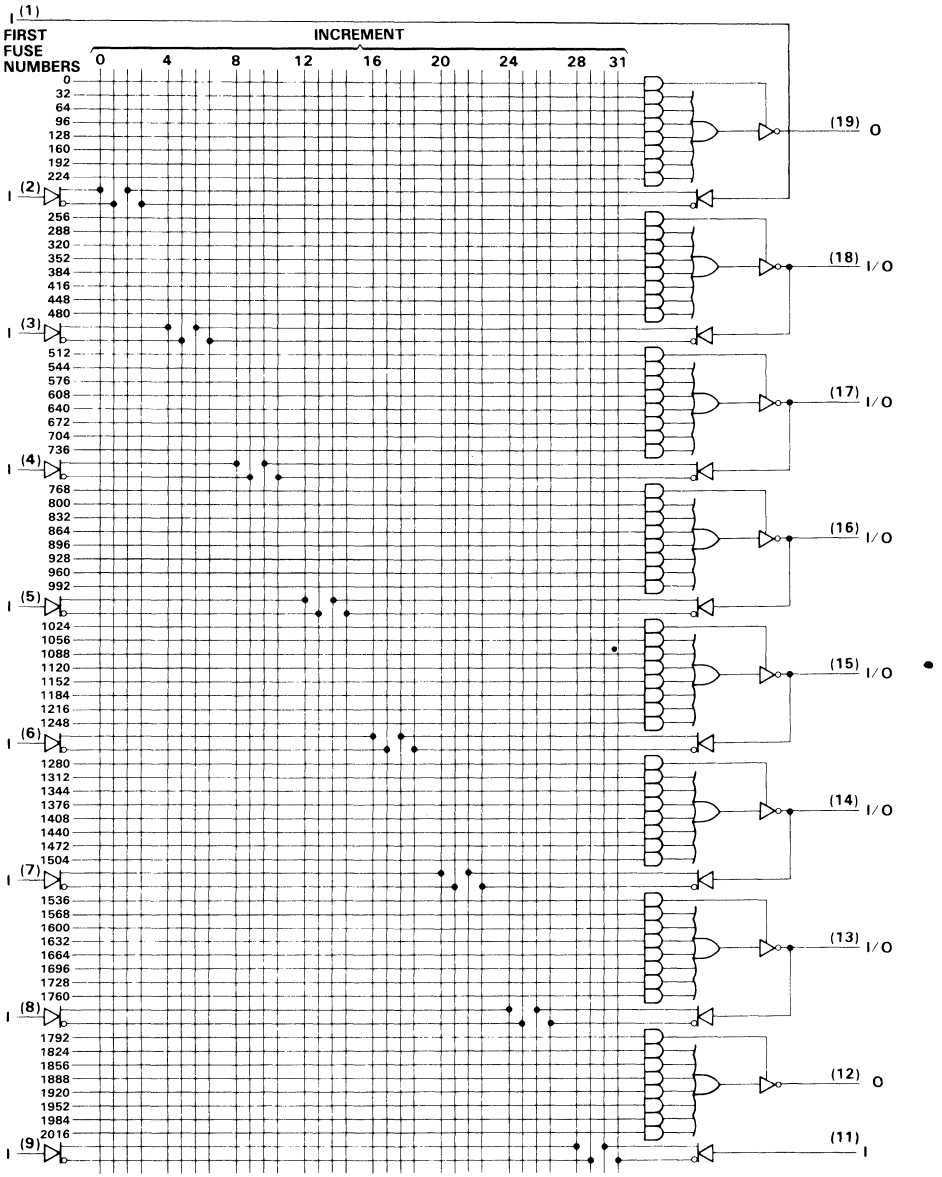
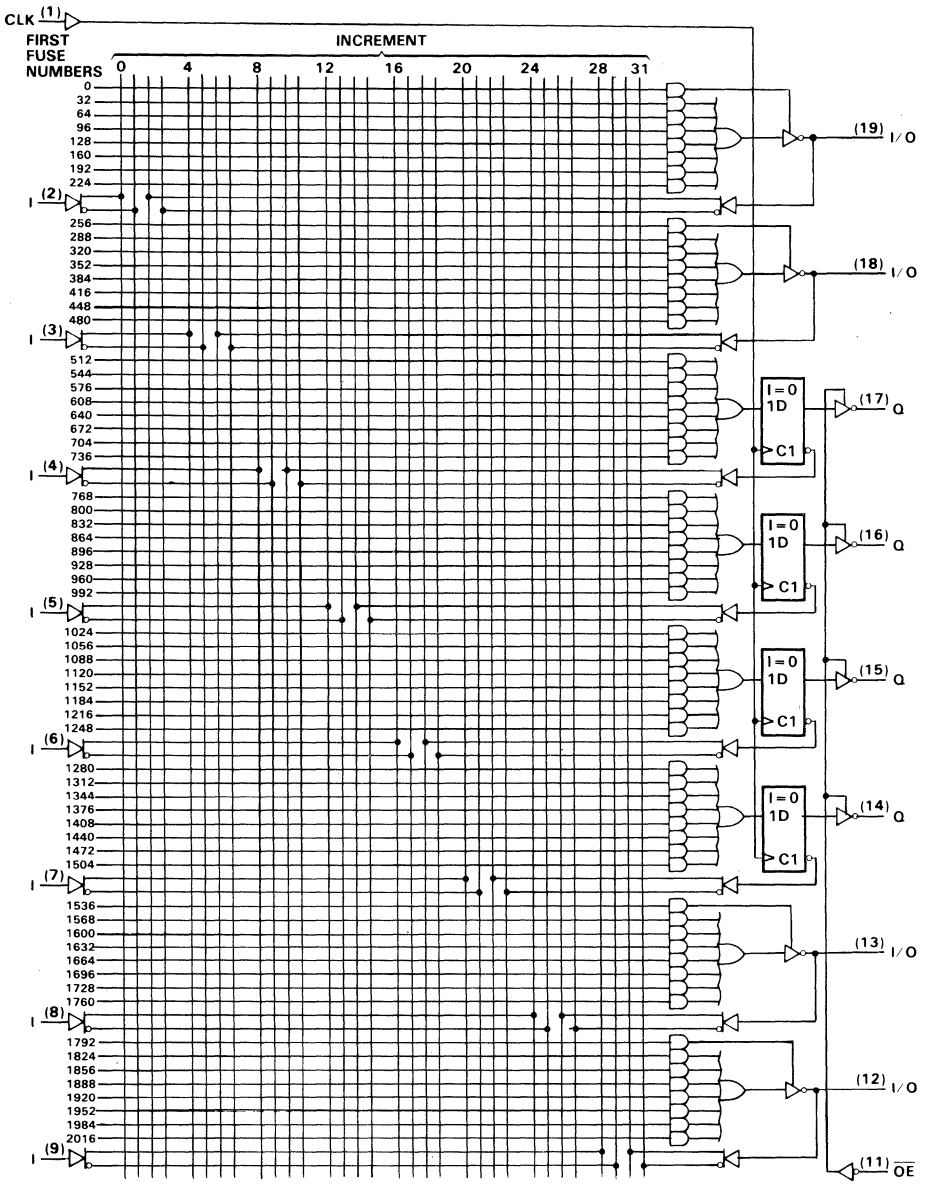


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

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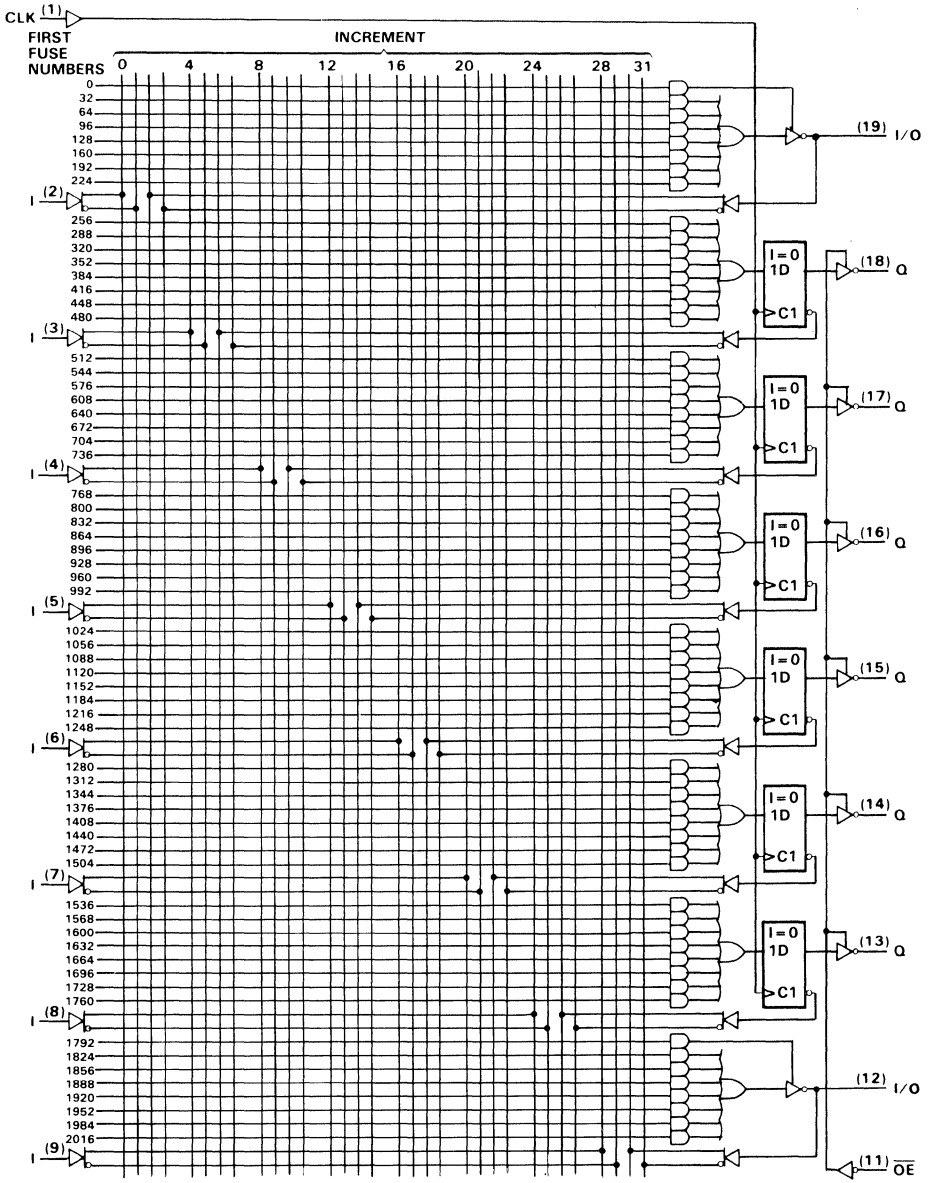
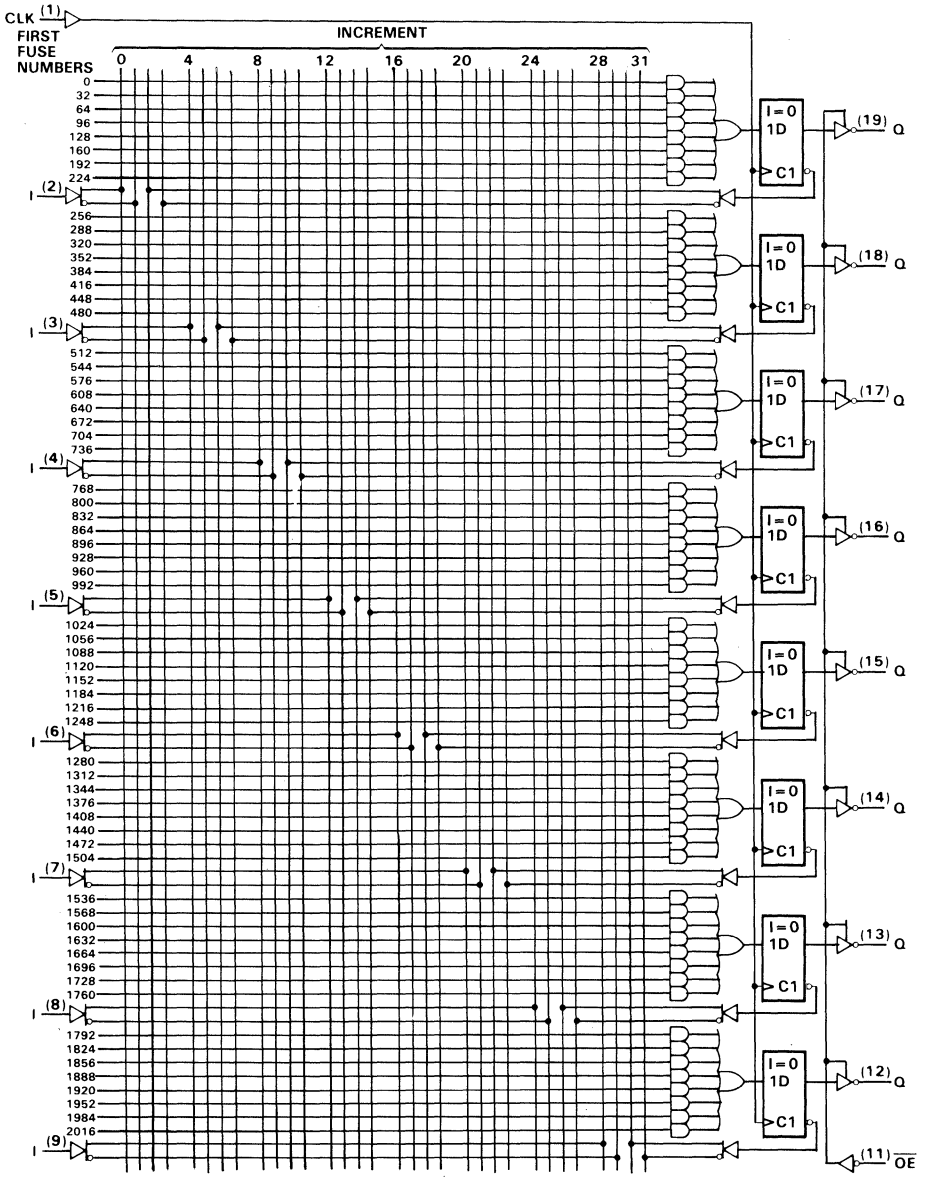


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		62.5	MHz
t_w	Pulse duration, clock (see Note2)	High	8			ns
		Low	8			
t_{su}	Setup time, input or feedback before CLK↑		10			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.3	0.5	V
I_{OZH}‡	O, Q outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}‡	O, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				−20	μA
	I/O ports						−250	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	μA
	All others						25	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.08	−0.25	mA
I_{OS}§		V_{CC} = 5 V,	V_O = 0.5 V		−30	−70	−130	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs open,	T_A = 25°C and 125°C		140	220	mA
		V_I = 0 V,	$\overline{OE}$ = V_{IH}	T_A = −55°C			250	
C_i		f = 1 MHz,	V_I = 2 V			5		pF
C_o		f = 1 MHz,	V_O = 2 V			6		pF
C_{clk}		f = 1 MHz,	V_{CLK} = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.

PRODUCT PREVIEW

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted) (see Figure 5)

PARAMETER	FROM	TO	MIN	TYP†	MAX	UNIT
f_{max}‡	Without feedback		62.5			MHz
	With internal feedback (counter configuration)		62.5			
	With external feedback		55.5			
t_{pd}	I, I/O	O, I/O	3	6	10	ns
t_{pd}	CLK↑	Q	2	4	8	ns
t_{pd}§	CLK↑	Feedback input			5	ns
t_{en}	OE↓	Q	2	4	10	ns
t_{dis}	OE↑	Q	2	4	10	ns
t_{en}	I, I/O	O, I/O	3	6	10	ns
t_{dis}	I, I/O	O, I/O	2	6	10	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡See section on f_{max} specifications.
§This parameter applies to TIBPAL16R4' and TIBPAL16R6' only (see Figure 2 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

PRODUCT PREVIEW

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		100	MHz
t_w	Pulse duration, clock (see Note 2)	High	5			ns
		Low	5			
t_{su}	Setup time, input or feedback before CLK↑		7			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA		−0.8	−1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.7 V			100	μA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V			−100	μA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			0.2	mA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.7 V			25	μA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V		−0.08	−0.25	mA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0.5 V	−30	−70	−130	mA
I_{CC}	V_{CC} = 5.25 V, V_I = 0 V	Outputs open,		160	210	mA
C_i	f = 1 MHz,	V_I = 2 V		5		pF
C_o	f = 1 MHz,	V_O = 2 V		6		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V		6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.

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switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted) (see Figure 6)

PARAMETER	FROM	TO		MIN	TYP†	MAX	UNIT
f_{max}‡	Without feedback			100			MHz
	With internal feedback (counter configuration)			100			
	With external feedback			74			
t_{pd}	I, I/O	O, I/O	1 or 2 outputs switching	3	5.5	7	ns
			8 outputs switching	3	6	7.5	
t_{pd}	CLK↑	Q		2	4	6.5	ns
t_{pd}§	CLK↑	Feedback input				3	ns
t_{en}	OE↓	Q		2	4	7.5	ns
t_{dis}	OE↑	Q		2	4	7.5	ns
t_{en}	I, I/O	O, I/O		3	6	9	ns
t_{dis}	I, I/O	O, I/O		2	6	9	ns
t_{skew}¶	Skew between registered outputs				0.5		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡See section on f_{max} specifications.
§This parameter applies to TIBPAL16R4′ and TIBPAL16R6′ only (see Figure 2 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.
¶This parameter is the measurement of the difference between the fastest and slowest t_{pd} (CLK-to-Q) observed when multiple registered outputs are switching in the same direction.

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programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

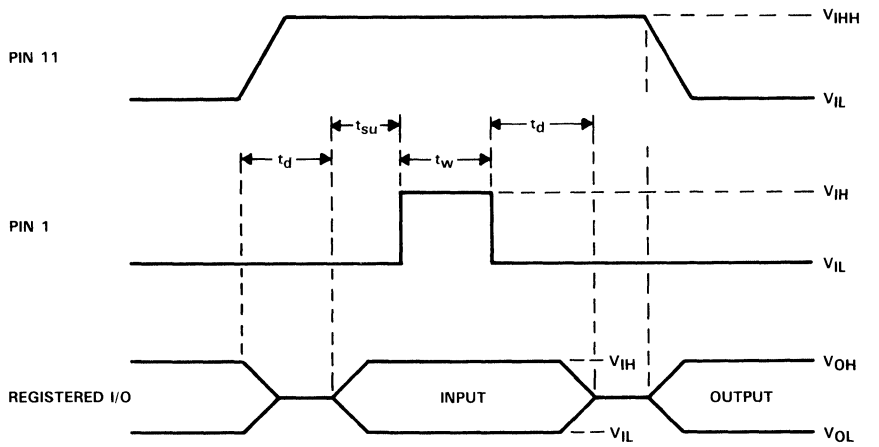
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 3)



NOTE 3: $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 1

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su} + t_h$). However, the minimum f_{max} is determined by the minimum clock period ($t_w$high + $t_w$low).

Thus, f_{max} without feedback $= \dfrac{1}{(t_w \text{ high} + t_w \text{ low})}$ or $\dfrac{1}{(t_{su} + t_h)}$.

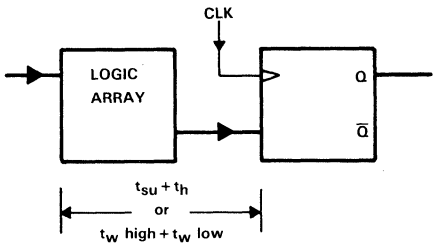


FIGURE 1. f_{max} WITHOUT FEEDBACK

f_{max} with internal feedback, see Figure 2

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus, f_{max} with internal feedback $= \dfrac{1}{(t_{su} + t_{pd} \text{ CLK-to-FB})}$.

Where t_{pd} CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

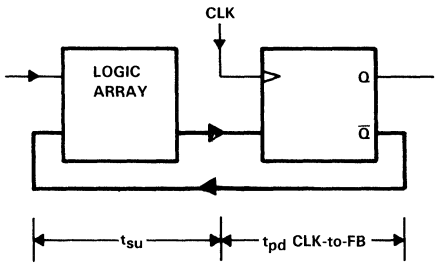


FIGURE 2. f_{max} WITH INTERNAL FEEDBACK

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f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 3

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input and setup time for the external signals ($t_{su} + t_{pd}$ CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd} \text{ CLK-to-Q})}$.

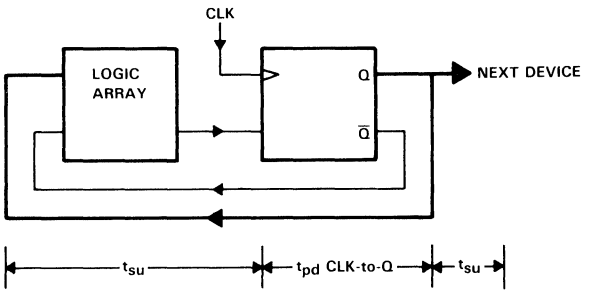


FIGURE 3. f_{max} WITH EXTERNAL FEEDBACK

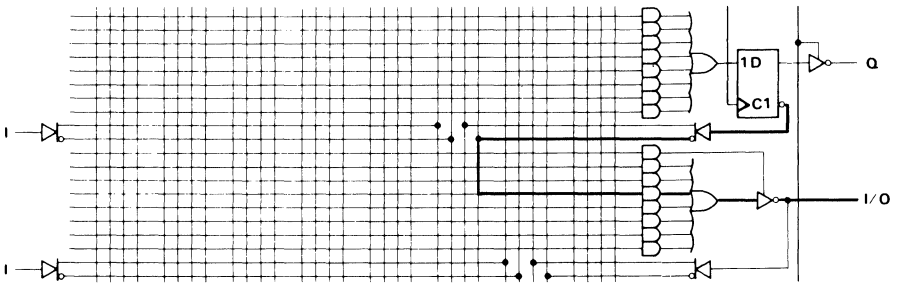
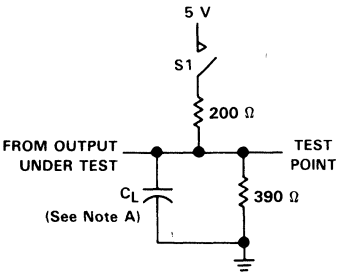
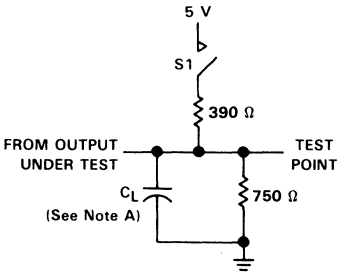


FIGURE 4. PROPAGATION DELAY FROM CLK↑ to I/O, THRU LOGIC ARRAY

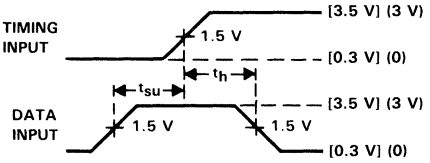
PARAMETER MEASUREMENT INFORMATION



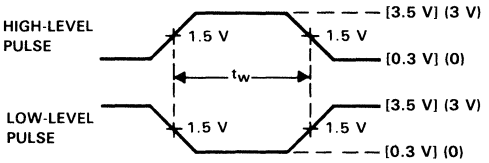
LOAD CIRCUIT FOR C SUFFIX DEVICES



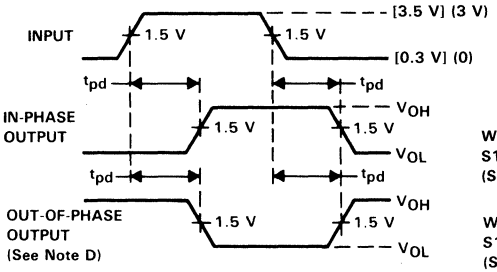
LOAD CIRCUIT FOR M SUFFIX DEVICES



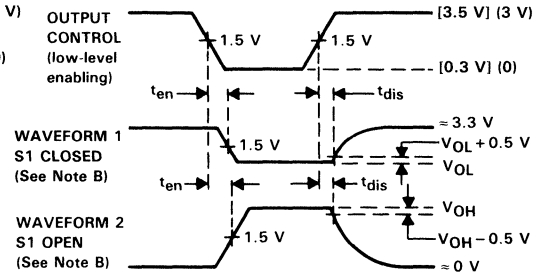
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}. 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and t_f = 2 ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in parentheses ( ). For C suffix, use the voltage levels indicated in brackets [ ].
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 5

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

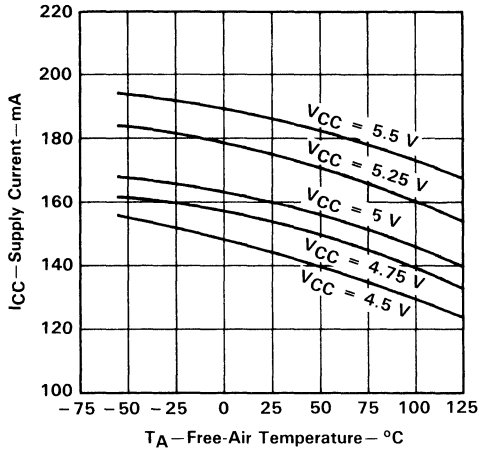

FIGURE 6

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

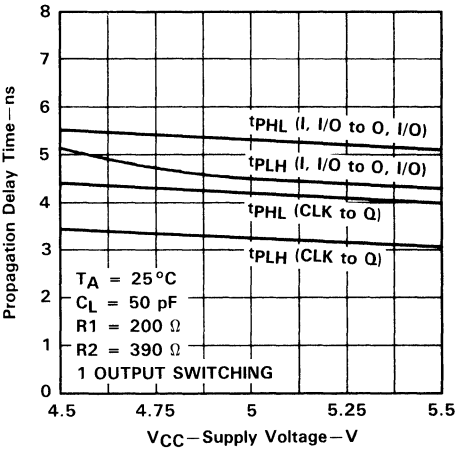

FIGURE 7

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

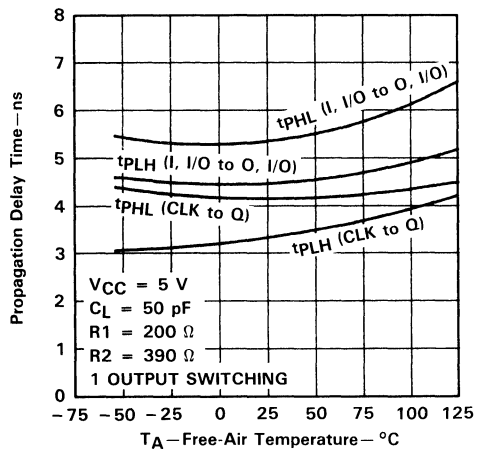

FIGURE 8

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

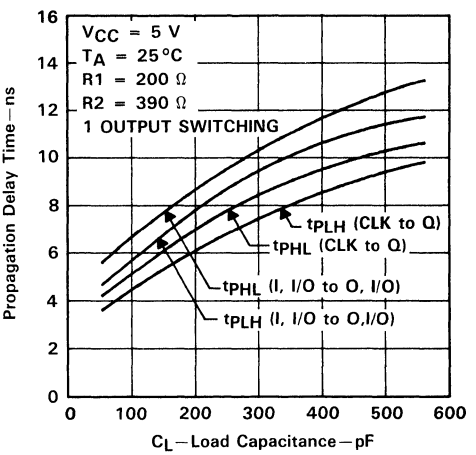

FIGURE 9

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
FREQUENCY
8-BIT COUNTER MODE

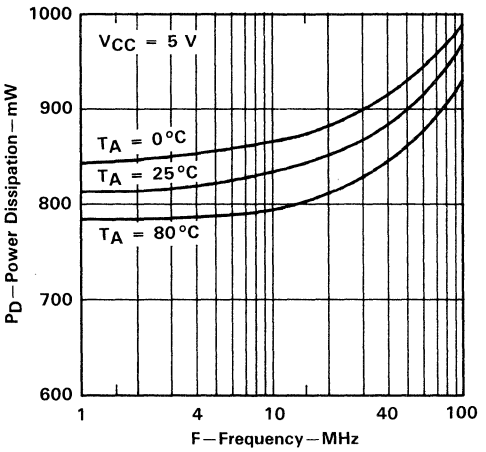

FIGURE 10

SKEW BETWEEN OUTPUTS†
vs
NUMBER OF OUTPUTS SWITCHING

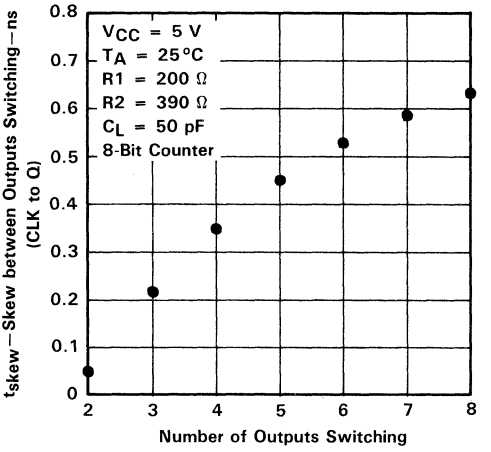

FIGURE 11

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

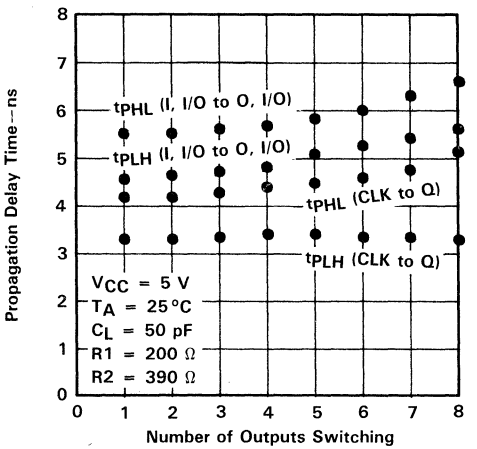

FIGURE 12

†Output switching in the same direction (t_{PLH} compared to t_{PLH}/t_{PHL} to t_{PHL})

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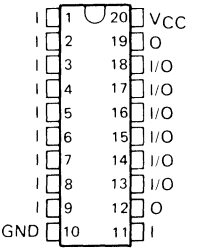
TIBPAL16L8-12M, TIBPAL16R4-12M, TIBPAL16R6-12M, TIBPAL16R8-12M
TIBPAL16L8-10C, TIBPAL16R4-10C, TIBPAL16R6-10C, TIBPAL16R8-10C
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

D3023, MAY 1987—REVISED NOVEMBER 1989

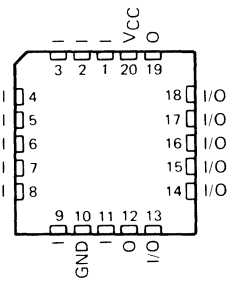
- **High-Performance Operation:**
  - **f_{max} (w/o feedback)**
    - **TIBPAL16R'-10C Series . . . 62.5 MHz**
    - **TIBPAL16R'-12M Series . . . 56 MHz**
  - **f_{max} (with feedback)**
    - **TIBPAL16R'-10C Series . . . 55.5 MHz**
    - **TIBPAL16R'-12M Series . . . 48 MHz**
  - **Propagation Delay**
    - **TIBPAL16L-10C . . . 10 ns Max**
    - **TIBPAL16L-12M . . . 12 ns Max**
- **Functionally Equivalent, but Faster than Existing 20-Pin PALs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom-functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL16' C series is characterized for operation from 0°C to 75°C.

IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Monolithic Memories, Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

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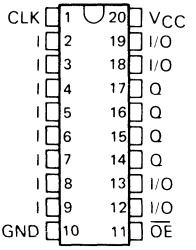
TIBPAL16R4'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



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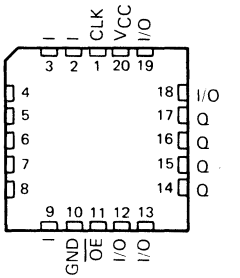
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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C SUFFIX . . . J OR N PACKAGE
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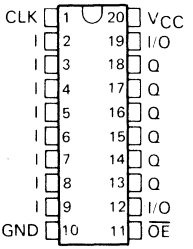

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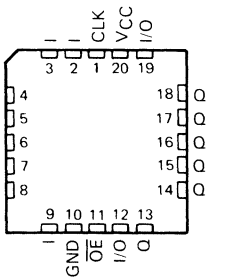

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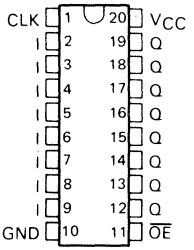
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



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C SUFFIX . . . FN PACKAGE
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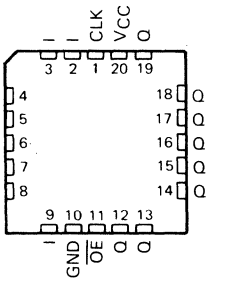

Pin assignments in operating mode

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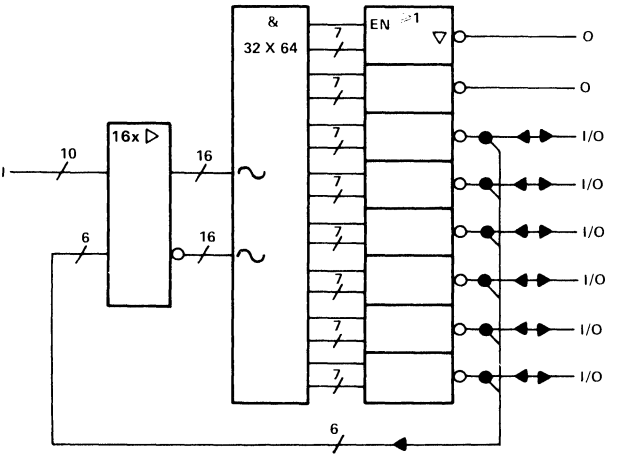
functional block diagrams (positive logic)

'PAL16L8



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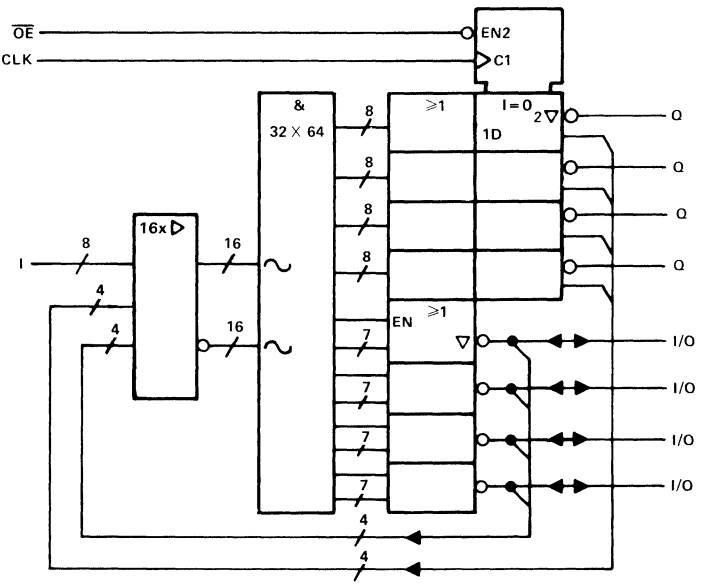
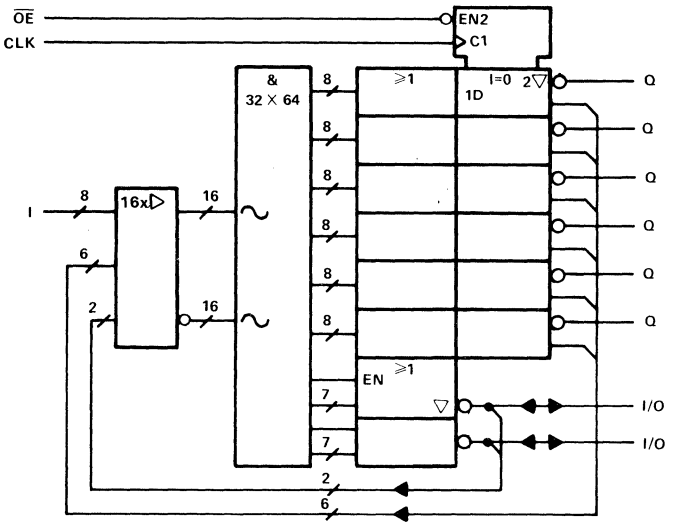


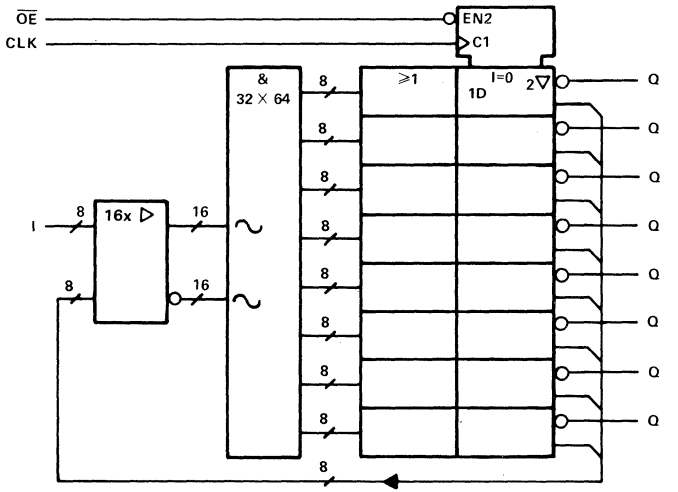
~ denotes fused inputs

functional block diagrams (positive logic)

'PAL16R6



'PAL16R8



∿ denotes fused inputs

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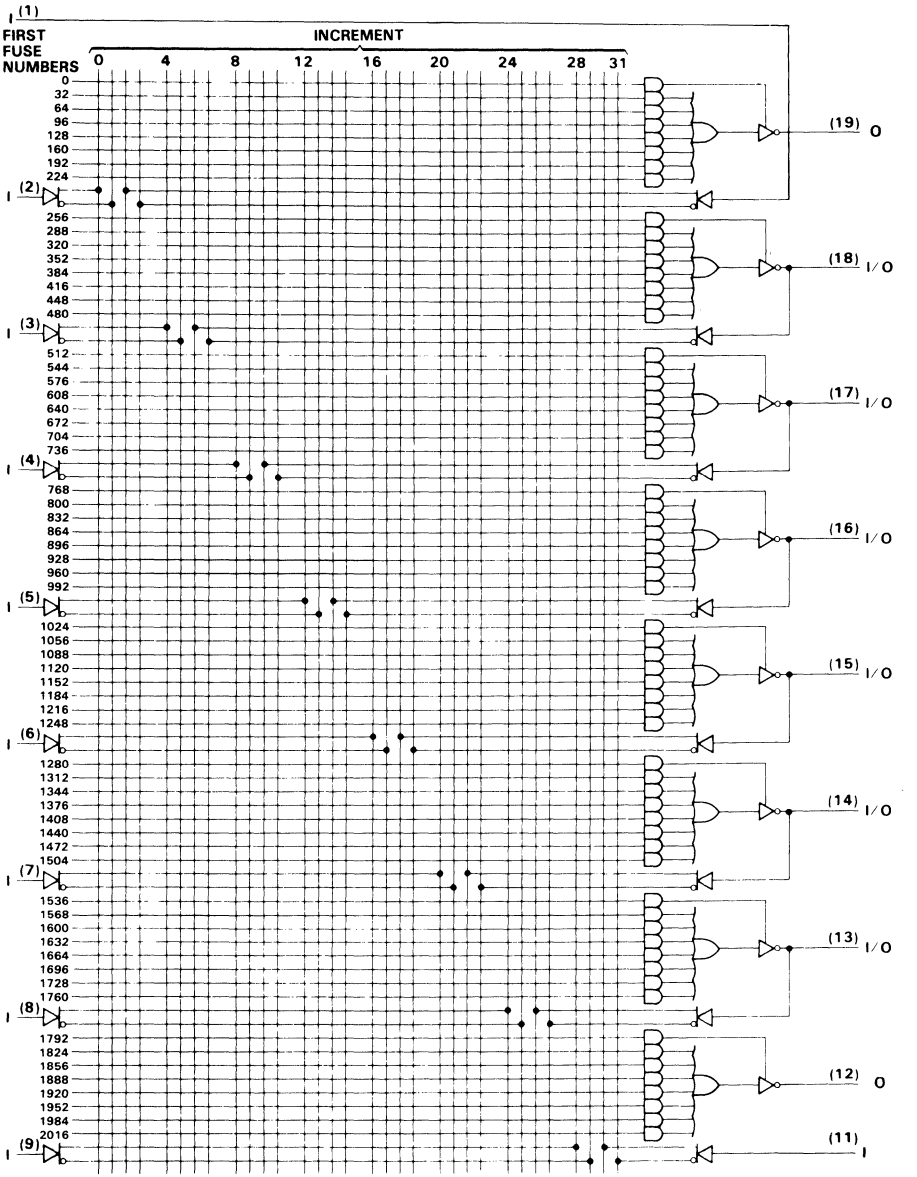
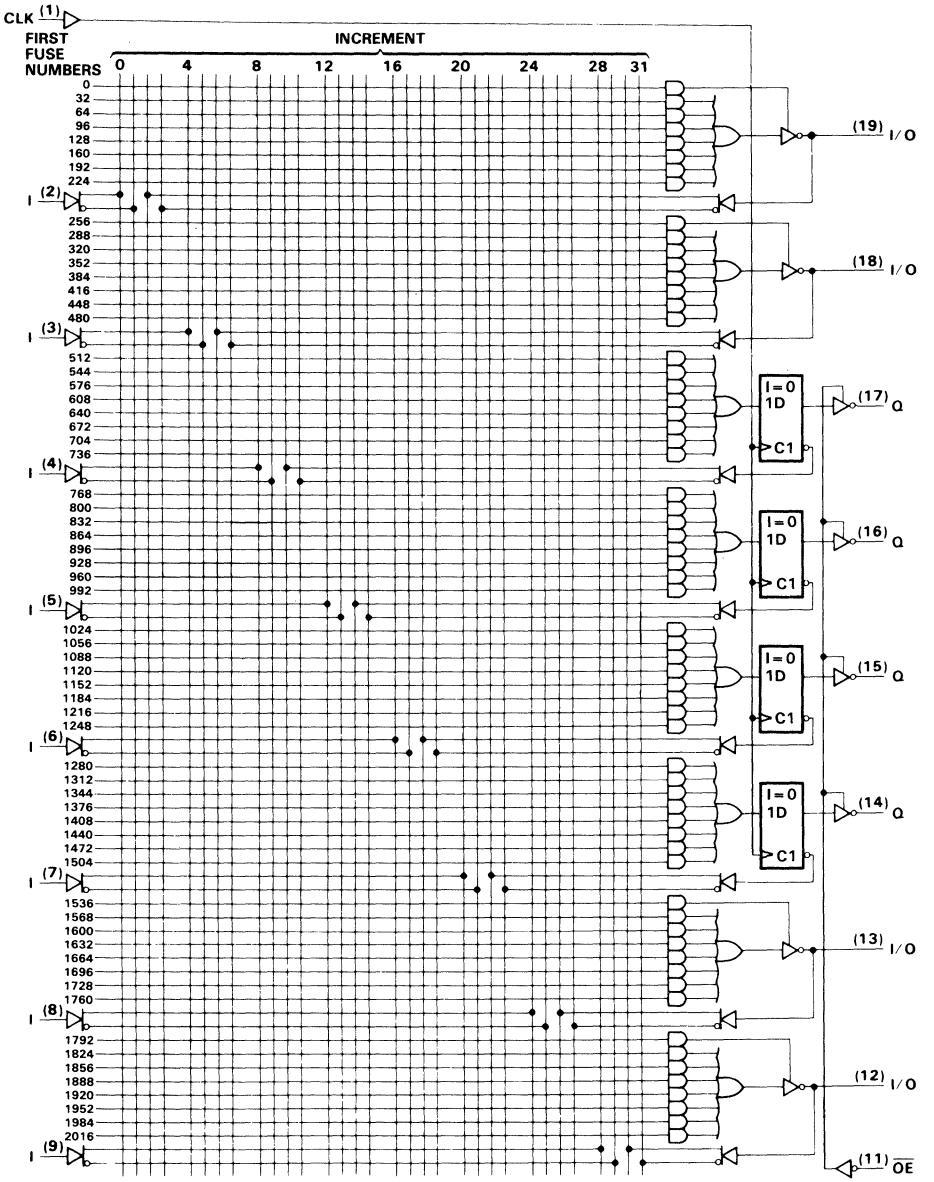


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

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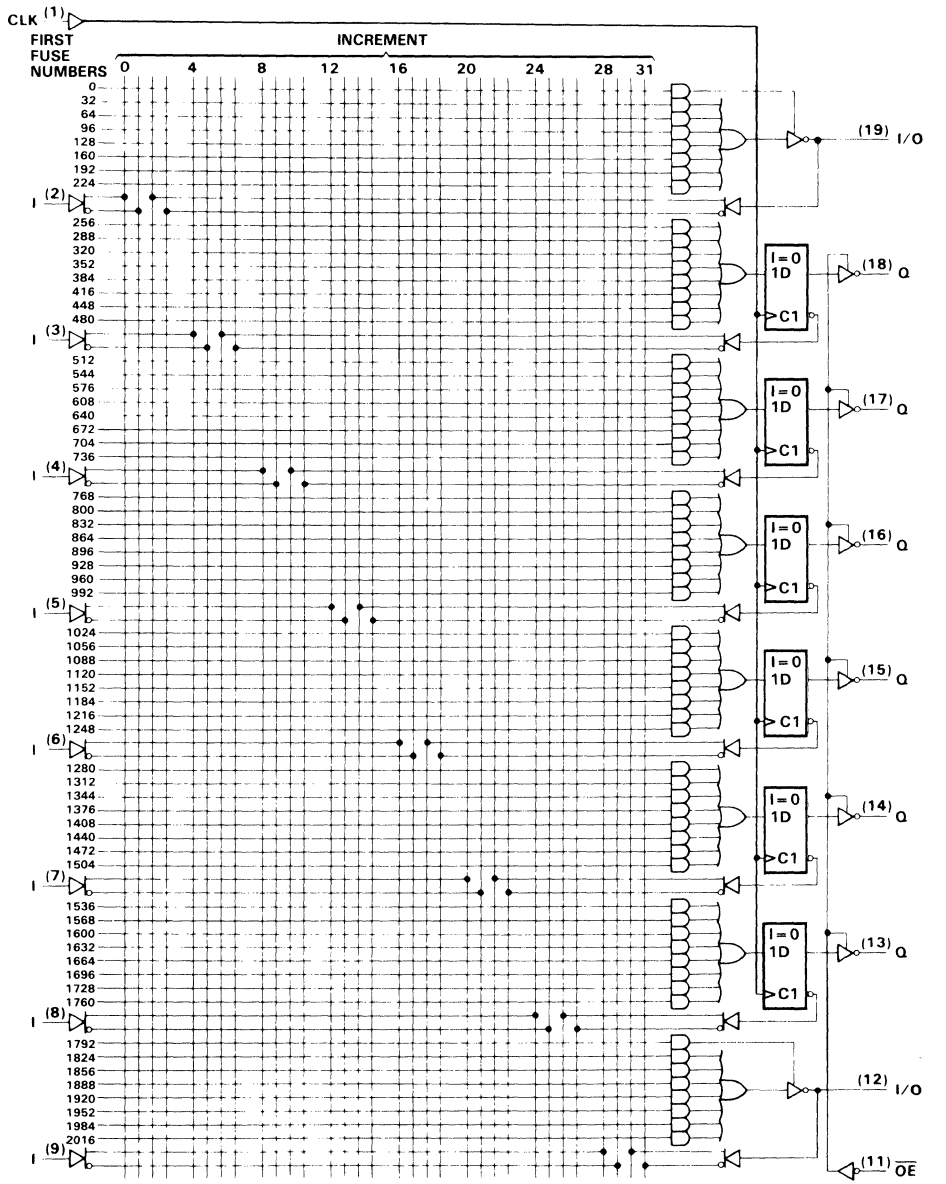
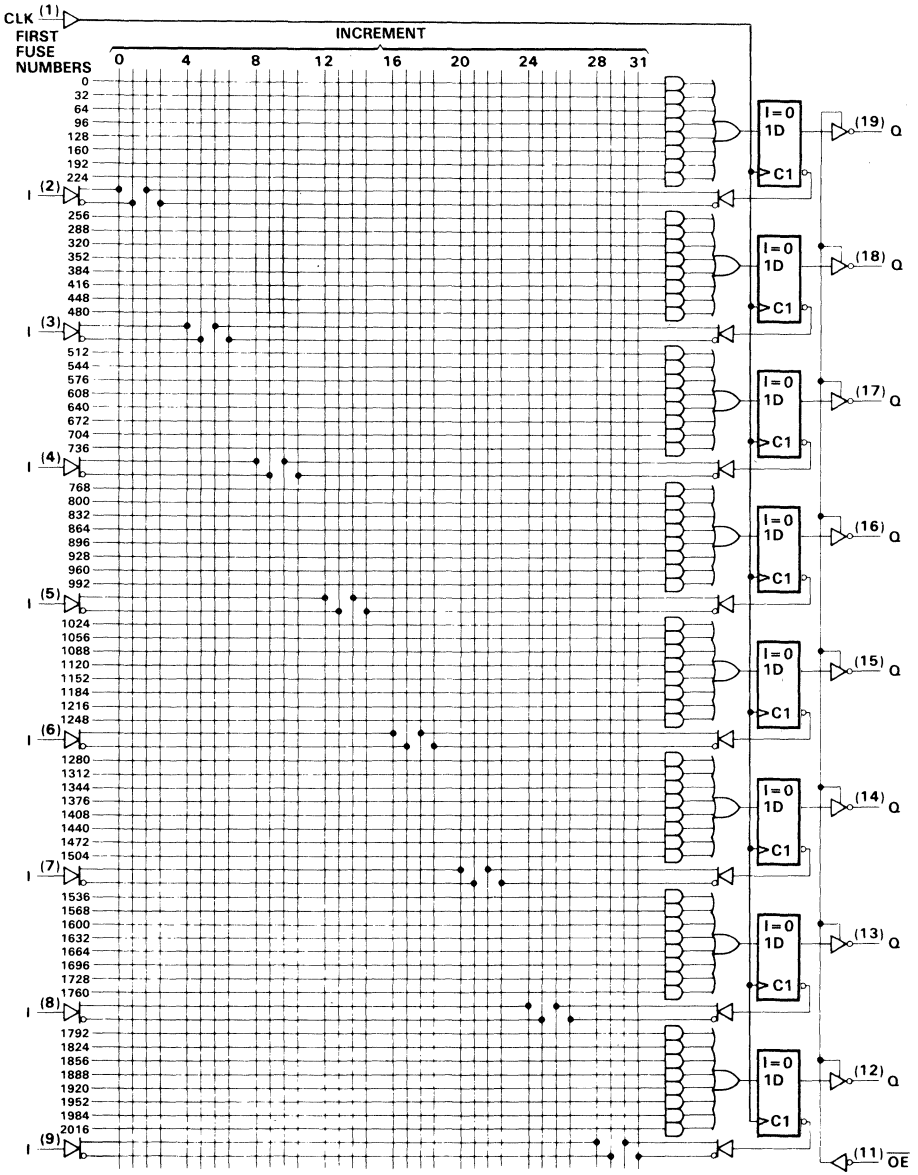


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		56	MHz
t_w	Pulse duration, clock (see Note 2)	High	9			ns
		Low	9			
t_{su}	Setup time, input or feedback before CLK↑		11			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−0.8	−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.4 V				100	μA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.4 V				−100	μA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
I_{IH}‡	V_{CC} = 5.5 V,	V_I = 2.4 V				25	μA
I_{IL}‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.08	−0.25	mA
I_{OS}§	V_{CC} = 5 V,	V_O = 0.5 V		−30	−70	−250	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = 0,	Outputs open		140	220	mA
C_{in}	f = 1 MHz,	V_I = 2 V			5		pF
C_{out}	f = 1 MHz,	V_O = 2 V			6		pF
$C_{i/o}$	f = 1 MHz,	$V_{i/o}$ = 2 V			7.5		pF
C_{CLK}	f = 1 MHz,	V_{CLK} = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}‡	With Feedback		$R1 = 390\ \Omega$, $R_2 = 750\ \Omega$, See Figure 1	48	80		MHz
	Without Feedback			56	85		
t_{pd}	I, I/O	O, I/O		3	7	12	ns
t_{pd}	CLK↑	Q		2	5	10	ns
t_{en}	OE↓	Q		1	4	10	ns
t_{dis}	OE↑	Q		1	4	10	ns
t_{en}	I, I/O	O, I/O		3	8	14	ns
t_{dis}	I, I/O	O, I/O		2	8	12	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ f_{max} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{max} (without feedback) $= \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		62.5	MHz
t_w	Pulse duration, clock (see Note 2)	High	8			ns
		Low	8			
t_{su}	Setup time, input or feedback before CLK↑		10			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA			−0.8	−1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.4 V				100	μA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V				−100	μA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				0.2	mA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.4 V				25	μA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.08	−0.25	mA
I_{OS}§	V_{CC} = 5 V,	V_O = 0		−30	−70	−130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open		140	180	mA
C_{in}	f = 1 MHz,	V_I = 2 V			5		pF
C_{out}	f = 1 MHz,	V_O = 2 V			6		pF
$C_{i/o}$	f = 1 MHz,	$V_{i/o}$ = 2 V			7.5		pF
C_{CLK}	f = 1 MHz,	V_{CLK} = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}‡	With Feedback		$R1 = 390\ \Omega$, $R_2 = 750\ \Omega$, See Figure 1	55.5	80		MHz
	Without Feedback			62.5	85		
t_{pd}	I, I/O	O, I/O		3	7	10	ns
t_{pd}	CLK↑	Q		2	5	8	ns
t_{en}	OE↓	Q		1	4	10	ns
t_{dis}	OE↑	Q		1	4	10	ns
t_{en}	I, I/O	O, I/O		3	8	10	ns
t_{dis}	I, I/O	O, I/O		3	8	10	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ f_{max} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{max} (without feedback) $= \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

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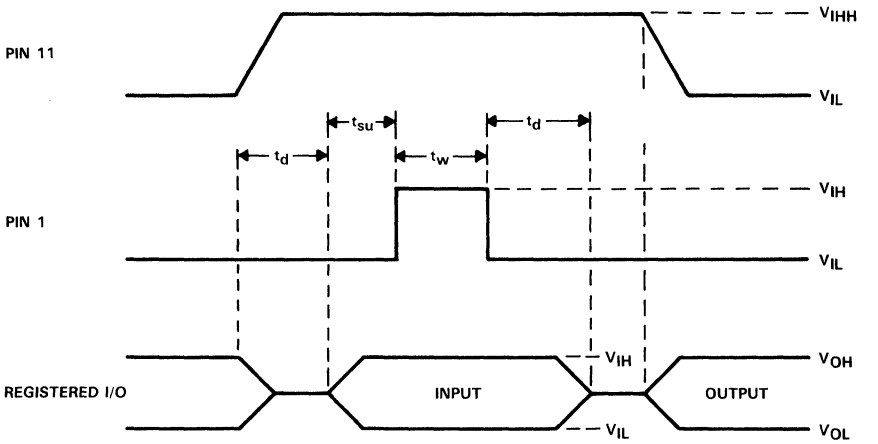
preload procedure for registered outputs (see Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

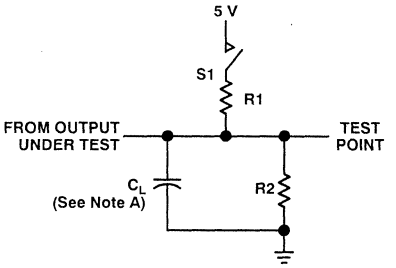
Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 3)

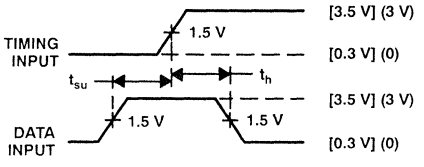


NOTE 3: $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

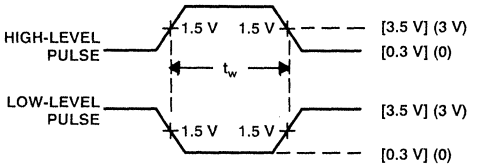
PARAMETER MEASUREMENT INFORMATION



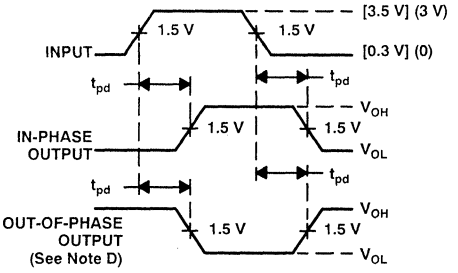
LOAD CIRCUIT FOR 3-STATE OUTPUTS



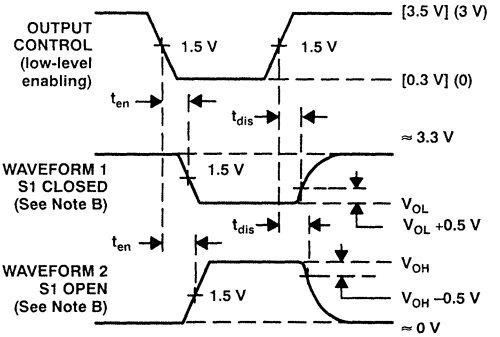
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For M suffix, use the voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be fused for testing.

FIGURE 1

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metastable characteristics for TIBPAL16R4-10C, TIBPAL16R6-10C, and TIBPAL16R8-10C

At some point in every system designer's career, he or she is faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically overcome by synchronizing one of the signals to the local clock through use of a flip-flop. However, this solution presents an awkward dilemna since the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop can influence overall system reliability.

Whenever the setup and hold times of a flip-flop are violated, its output response becomes uncertain and is said to be in the metastable state if the output hangs up in the region between V_{IL} and V_{IH}. This metastable condition lasts until the flip-flop falls into one of its two stable states, which takes longer than the specified maximum propagation delay time (CLK to Q max).

From a system engineering standpoint, a designer cannot use the specified data sheet maximum for propagation delay time when using the flip-flop as a data synchronizer — how long to wait after the specified data sheet maximum must be known before using the data in order to guarantee reliable system operation.

The circuit shown in Figure 2 can be used to evaluate MTBF (Mean Time Between Failure) and Δt for a selected flip-flop. Whenever the Q output of the DUT is between 0.8 V and 2 V, the comparators are in opposite states. When the Q output of the DUT is higher than 2 V or lower than 0.8 V, the comparators are at the same logic level. The outputs of the two comparators are sampled a selected time (Δt) after SCLK. The exclusive OR gate detects the occurrence of a failure and increments the failure counter.

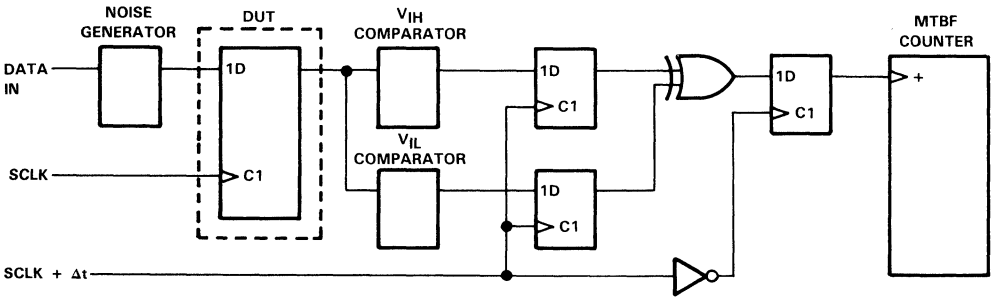
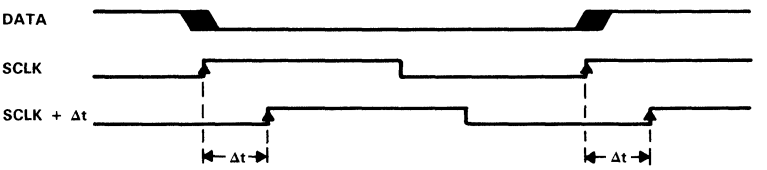


FIGURE 2. METASTABLE EVALUATION TEST CIRCUIT

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal is applied so that it always violates the setup and hold time. This condition is illustrated in the timing diagram in Figure 3. Any other relationship of SCLK to data will provide less chance for the device to enter into the metastable state.



$$MTBF = \frac{\text{TIME (SEC)}}{\#\ \text{FAILURES}}$$

t_{rec} = Δt − CLK TO Q (MAX)

FIGURE 3. TIMING DIAGRAM

By using the described test circuit, MTBF can be determined for several different values of Δt (see Figure 2). Plotting this information on semilog paper demonstrates the metastable characteristics of the selected flip-flop. Figure 4 shows the results for the TIBPAL16'-10 operating at 1 MHz.

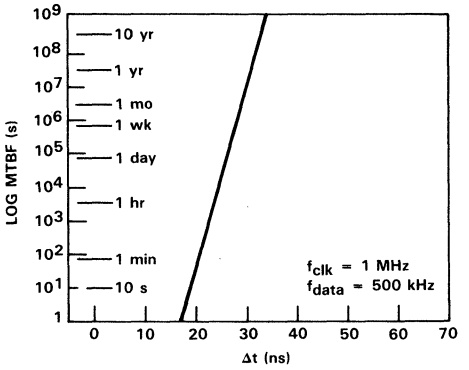


FIGURE 4. METASTABLE CHARACTERISTICS

From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies.

The metastable equation: $\frac{1}{MTBF} = f_{SCLK} \times f_{data} \times C1\ e^{(-C2 \times \Delta t)}$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data, these constants can be solved for: $C1 = 9.15 \times 10^{-7}$ and $C2 = 0.959$

Therefore

$$\frac{1}{MTBF} = f_{SCLK} \times f_{data} \times 9.159 \times 10^{-7}\ e^{(-0.959 \times \Delta t)}$$

definition of variables

DUT (Device Under Test): The DUT is a 10-ns registered PAL programmed with the equation Q := D.

MTBF (Mean Time Between Failures): The average time (s) between metastable occurrences that cause a violation of the device specifications.

f_{SCLK} (system clock frequency): Actual clock frequency for the DUT.

f_{data} (data frequency): Actual data frequency for a specified input to the DUT.

C1: Calculated constant that defines the magnitude of the curve.

C2: Calculated constant that defines the slope of the curve.

t_{rec} (metastability recovery time): Minimum time required to guarantee recovery from metastability, at a given MTBF failure rate. $t_{rec} = \Delta t - t_{pd}$ (CLK to Q, max)

Δt: The time difference (ns) from when the synchronizing flip-flop is clocked to when its output is sampled.

The test described above has shown the metastable characteristics of the TIBPAL16R4/R6/R8-10 series. For additional information on metastable characteristics of Texas Instruments logic circuits, please refer to TI Applications publication #SDAA004, "Metastable Characteristics, Design Considerations for ALS, AS, and LS Circuits."

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TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

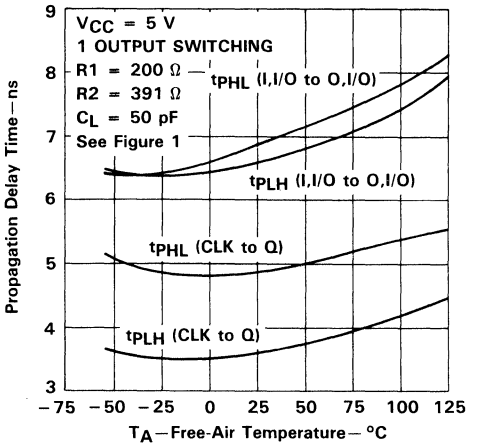

FIGURE 5

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

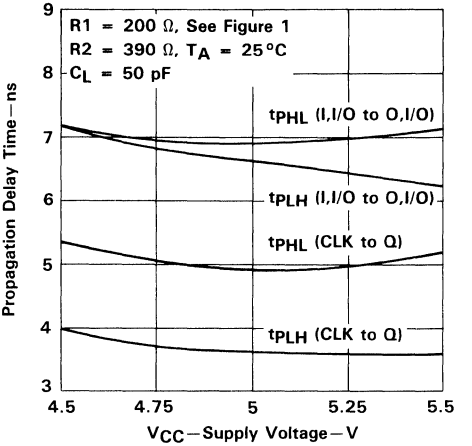

FIGURE 6

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

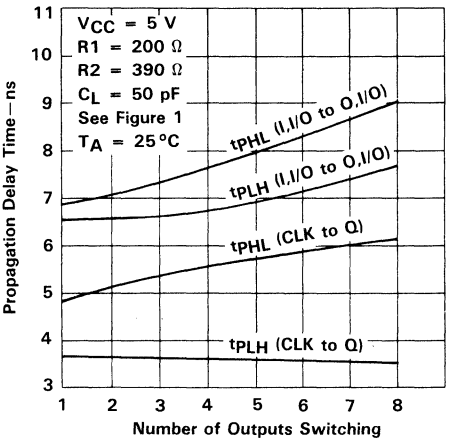

FIGURE 7

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

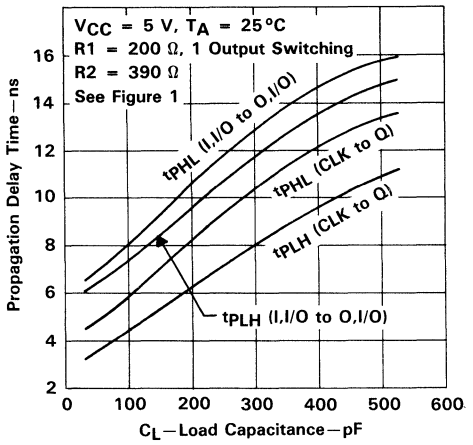

FIGURE 8

POWER DISSIPATION
vs
FREQUENCY
8-BIT COUNTER MODE

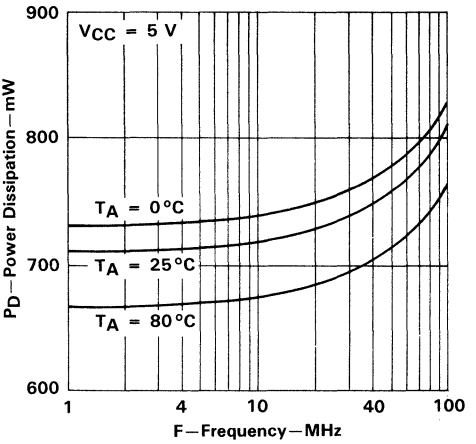

FIGURE 9

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

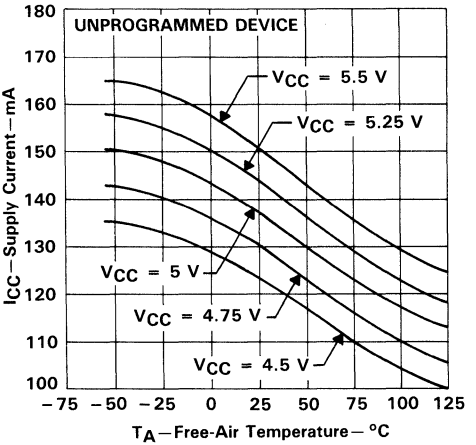

FIGURE 10

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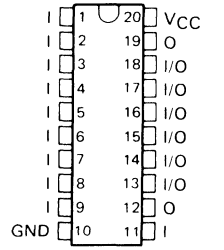
TIBPAL16L8-15M, TIBPAL16R4-15M, TIBPAL16R6-15M, TIBPAL16R8-15M
TIBPAL16L8-12C TIBPAL16R4-12C TIBPAL16R6-12C TIBPAL16R8-12C
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

D3338, JANUARY 1986—REVISED AUGUST 1989

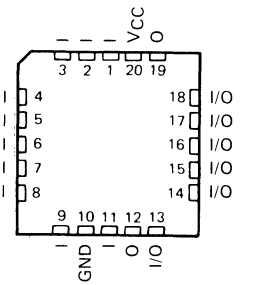
- **High-Performance Operation**
  Propagation Delay
  M Suffix . . . 15 ns Max
  C Suffix . . . 12 ns Max
- **Functionally Equivalent, but Faster than PAL16L8B, PAL16R4B, PAL16R6B, and PAL16R8B**
- **Power-Up Clear on Registered Devices (All Registered Outputs are Set High but Voltage Levels at the Output Pins Go Low)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The TIBPAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL16' C series is characterized for operation from 0°C to 75°C.

IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Monolithic Memories, Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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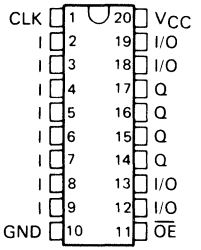
TIBPAL16R4'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX. . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R4'
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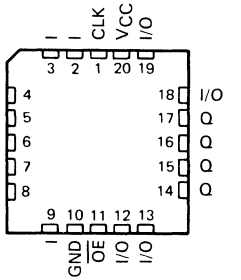
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL16R6'
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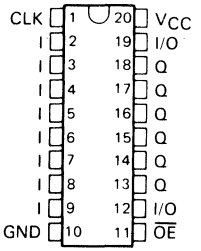
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R6'
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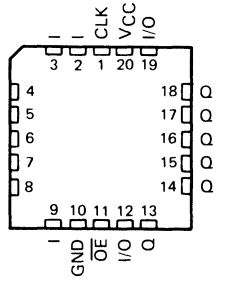
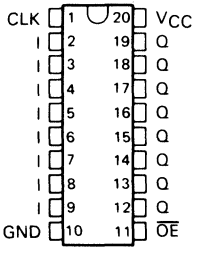
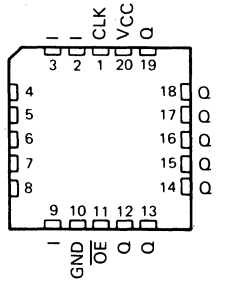
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX. . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

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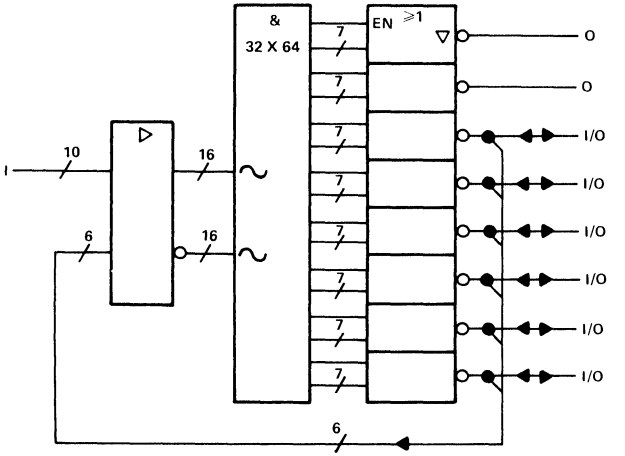
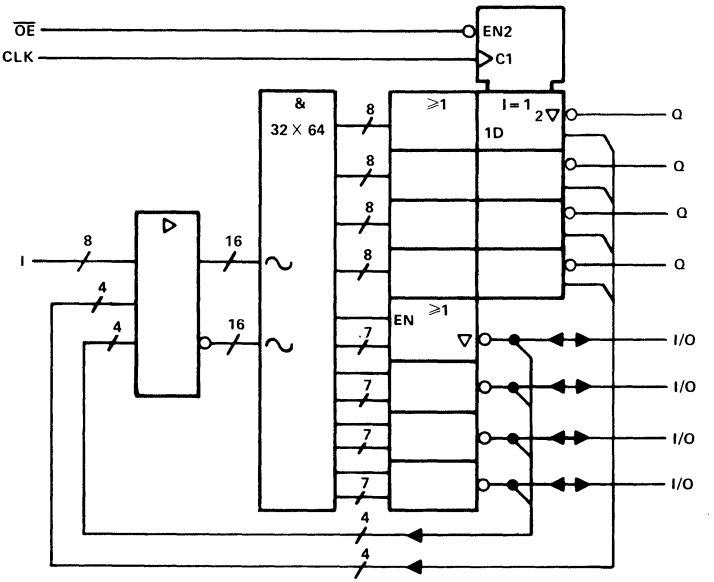
functional block diagrams (positive logic)

'PAL16L8



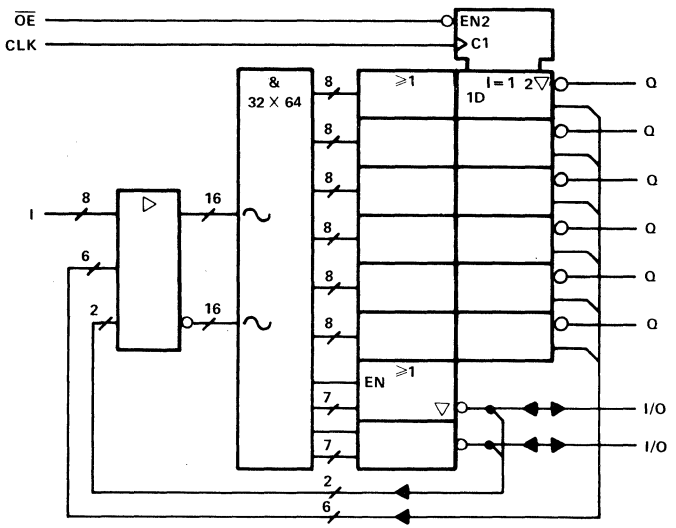
'PAL16R4



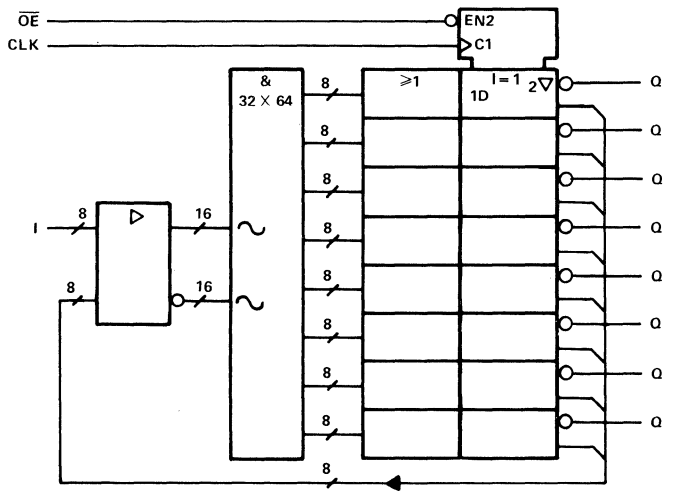
∼ denotes fused inputs

functional block diagrams (positive logic)

'PAL16R6



'PAL16R8



~ denotes fused inputs

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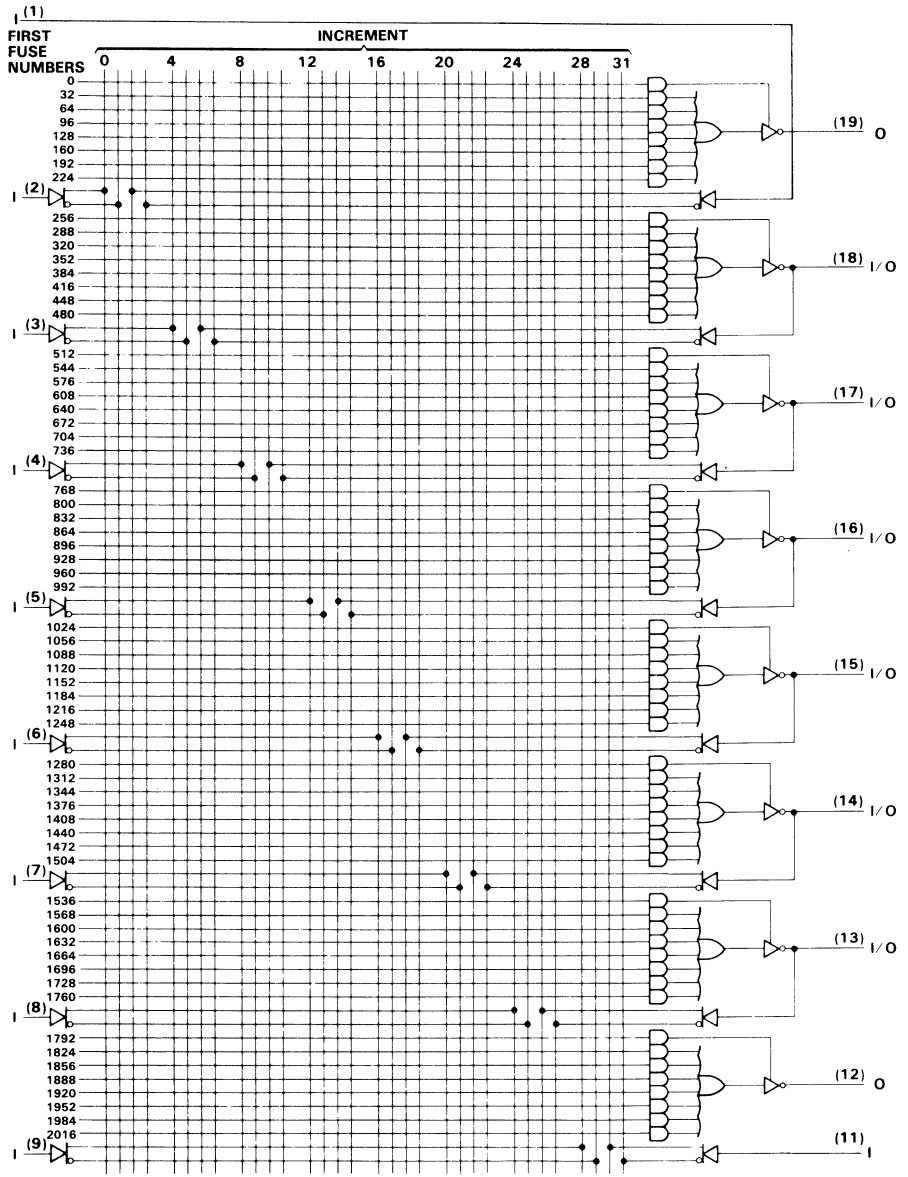
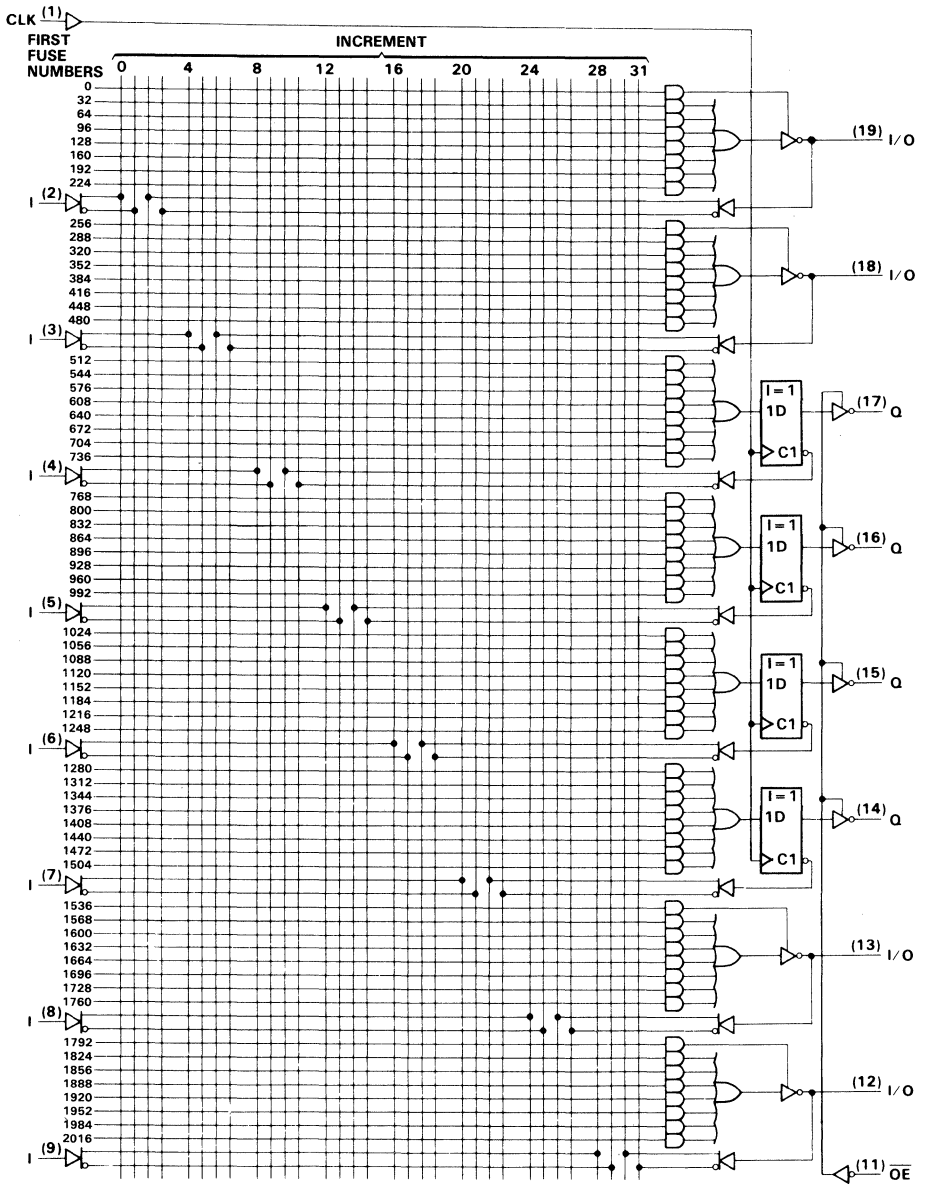


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

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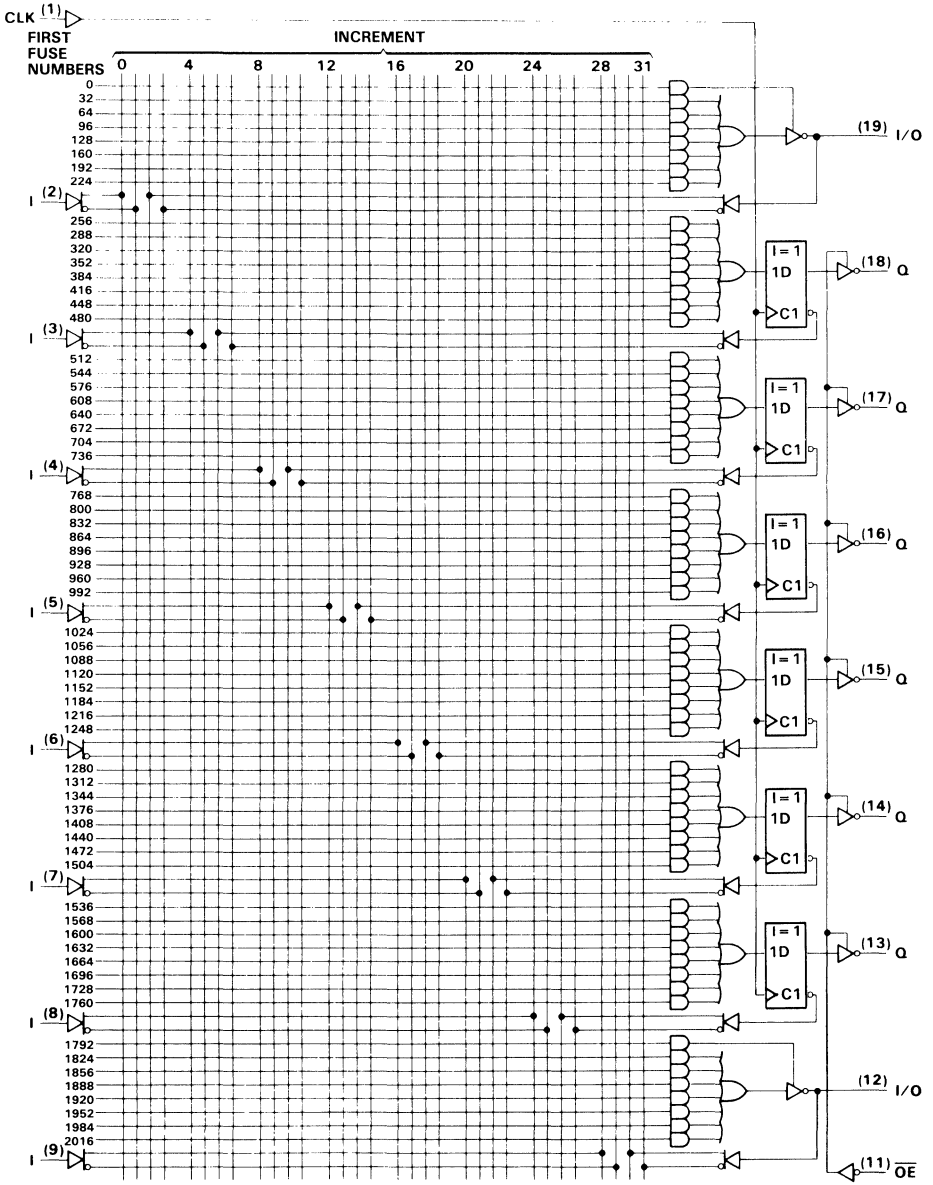
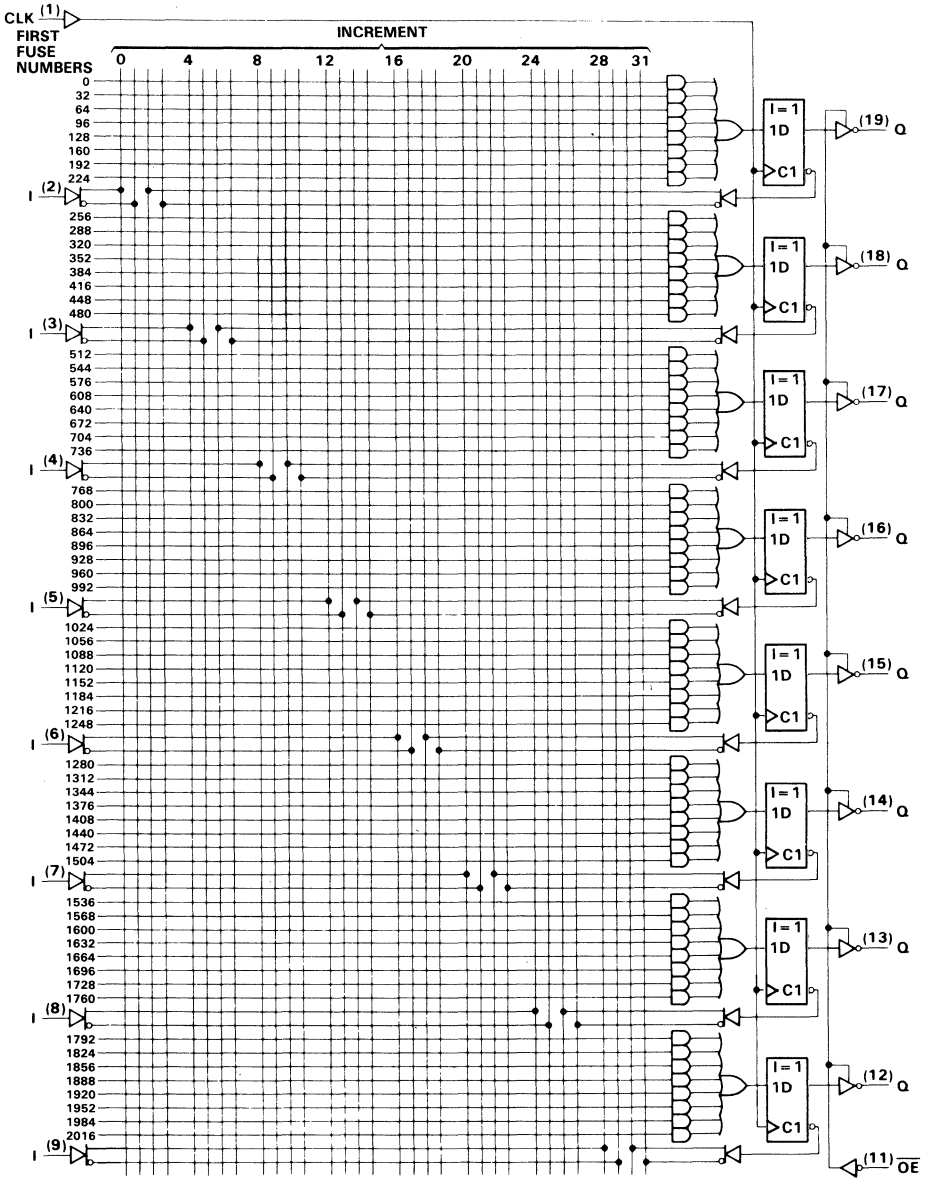


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions (see Note 2)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		50	MHz
t_w	Pulse duration, clock (see Note 2)	High	9			ns
		Low	10			
t_{su}	Setup time, input or feedback before CLK↑		15			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		−55		125	°C

NOTE 2: The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA		2.4	3.3		V
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
	I/O ports					−250	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V	Pin 1, 11			0.2	mA
			All others			0.1	
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V	Pin 1, 11			50	μA
			I/O ports			100	
			All others			20	
I_{IL}		V_{CC} = 5.5 V, V_I = 0.4 V	I/O ports			−0.25	mA
			All others			−0.2	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0.5 V		−30		−250	mA
I_{CC}		V_{CC} = 5.5 V, V_I = 0, Outputs open			170	220	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}‡				50			MHz
t_{pd}‡	I, I/O	O, I/O			8	15	ns
t_{pd}	CLK↑	Q	R1 = 390 Ω,		7	12	ns
t_{en}	OE↓	Q	R2 = 750 Ω,		8	12	ns
t_{dis}	OE↑	Q	See Figure 1		7	12	ns
t_{en}	I, I/O	O, I/O			8	15	ns
t_{dis}	I, I/O	O, I/O			8	15	ns

†All typical values are at V_{CC} = 5 V, T_A 25°C.
‡Maximum operating frequency and propagation delay are specified for the basic building block. When using feedback, limits must be calculated accordingly.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions (see Note 2)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		62	MHz
t_w	Pulse duration, clock (see Note 2)	High	7			ns
		Low	8			
t_{su}	Setup time, input or feedback before CLK↑		10			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0		75	°C

NOTE 2: The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA		2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA			0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = 5.25 V, V_O = 2.7 V				20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.25 V, V_O = 0.4 V				−20	μA
	I/O ports					−250	
I_I		V_{CC} = 5.25 V, V_I = 5.5 V	Pin 1, 11			0.1	mA
			All others			0.1	
I_{IH}		V_{CC} = 5.25 V, V_I = 2.7 V	Pin 1, 11			20	μA
			All others			20	
I_{IL}		V_{CC} = 5.25 V, V_I = 0.4 V				−0.2	mA
I_O‡		V_{CC} = 5.25 V, V_O = 0.5 V		−30		−125	mA
I_{CC}		V_{CC} = 5.25 V, V_I = 0, Outputs open			170	200	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}‡				62			MHz
t_{pd}‡	I, I/O	O, I/O			8	12	ns
t_{pd}	CLK↑	Q	R1 = 500 Ω,		7	10	ns
t_{en}	OE↓	Q	R2 = 500 Ω,		8	10	ns
t_{dis}	OE↑	Q	See Figure 1		7	10	ns
t_{en}	I, I/O	O, I/O			8	12	ns
t_{dis}	I, I/O	O, I/O			8	12	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Maximum operating frequency and propagation delay are specified for the basic building block. When using feedback, limits must be calculated accordingly.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 995-5666.

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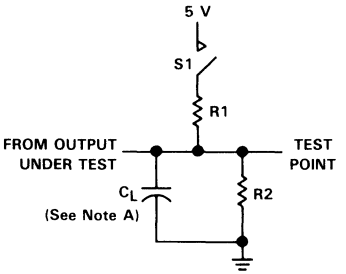
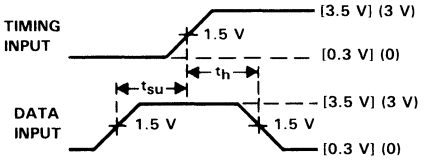
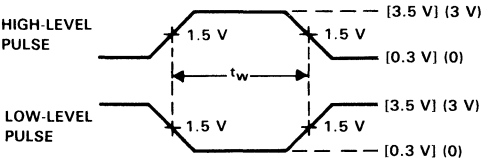
PARAMETER MEASUREMENT INFORMATION



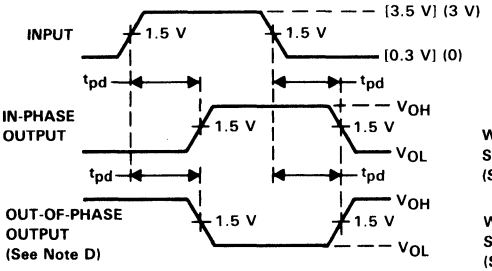
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



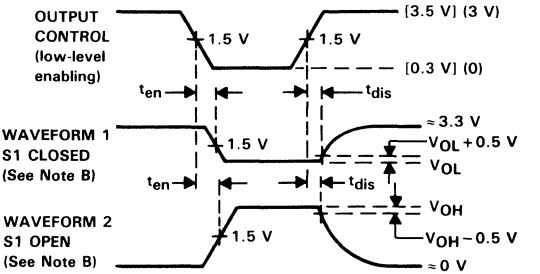
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For M suffix, use voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 1

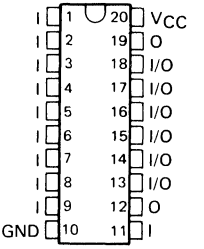
TIBPAL16L8-20M, TIBPAL16R4-20M, TIBPAL16R6-20M, TIBPAL16R8-20M
TIBPAL16L8-15C, TIBPAL16R4-15C, TIBPAL16R6-15C, TIBPAL16R8-15C
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

D3340, FEBRUARY 1984—REVISED AUGUST 1989

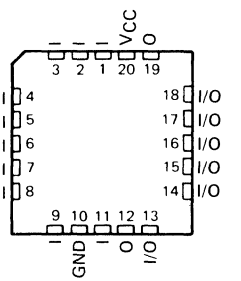
- **High-Performance Operation**
  - **Propagation Delay**
    - **M Suffix . . . 20 ns Max**
    - **C Suffix . . . 15 ns Max**
- **Functionally Equivalent, but Faster than PAL16L8A, PAL16R4A, PAL16R6A, and PAL16R8A**
- **Power-Up Clear on Registered Devices (All Registered Outputs are Set High but Voltage Levels at the Output Pins Go Low)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



description

These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The PAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The PAL16' C series is characterized for operation from 0°C to 70°C.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
IMPACT is a trademark of Texas Instruments Incorporated.

PAL is a registered trademark of Monolithic Memories Inc.

PRODUCTION DATA *documents contain information* **current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.**

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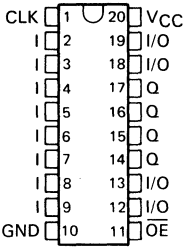
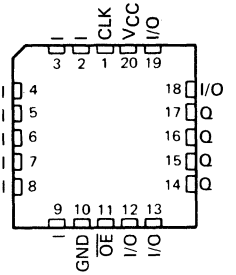
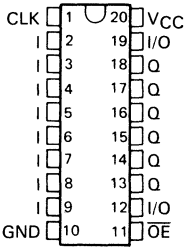
TIBPAL16R4'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



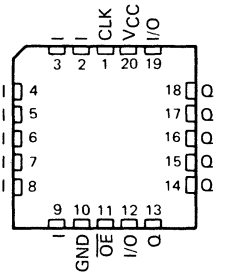
TIBPAL16R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



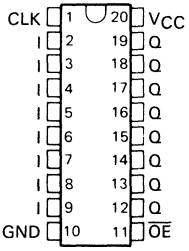
TIBPAL16R6'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



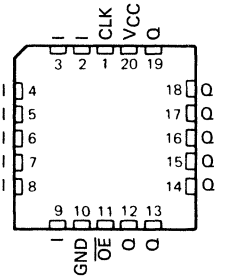
TIBPAL16R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



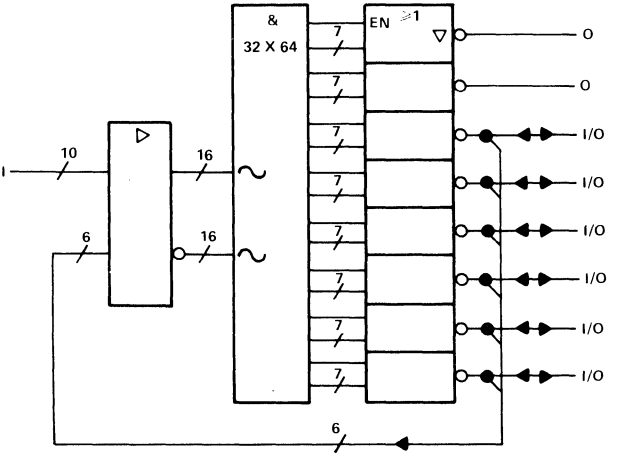
TIBPAL16R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

functional block diagrams (positive logic)

'PAL16L8



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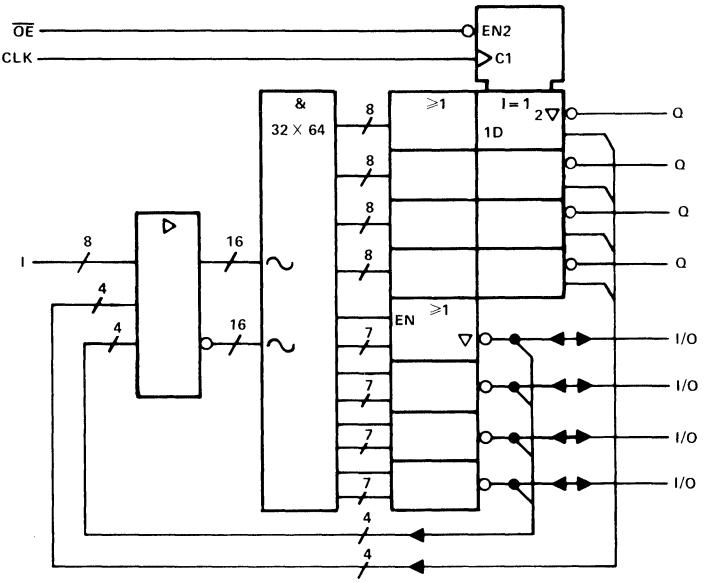
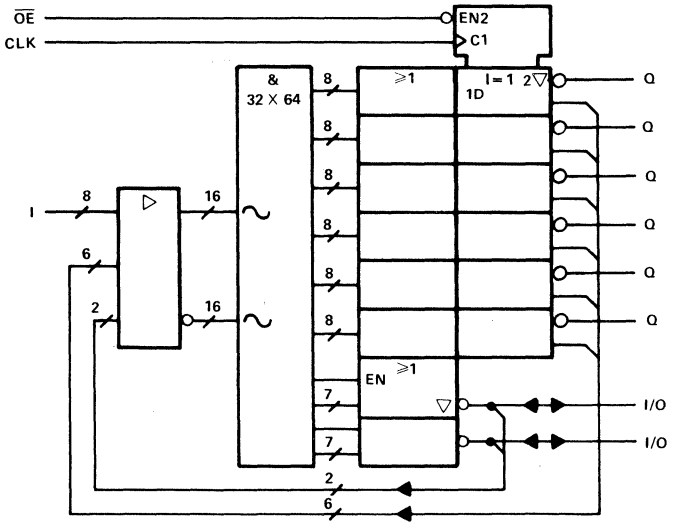


∼ denotes fused inputs

functional block diagrams (positive logic)

'PAL16R6



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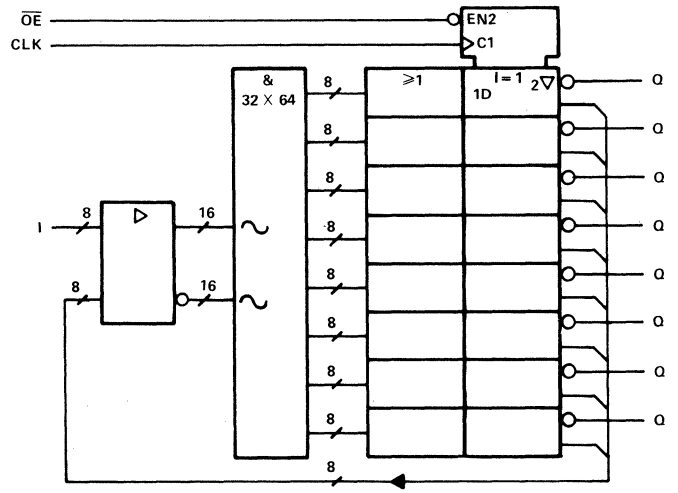

∼ denotes fused inputs

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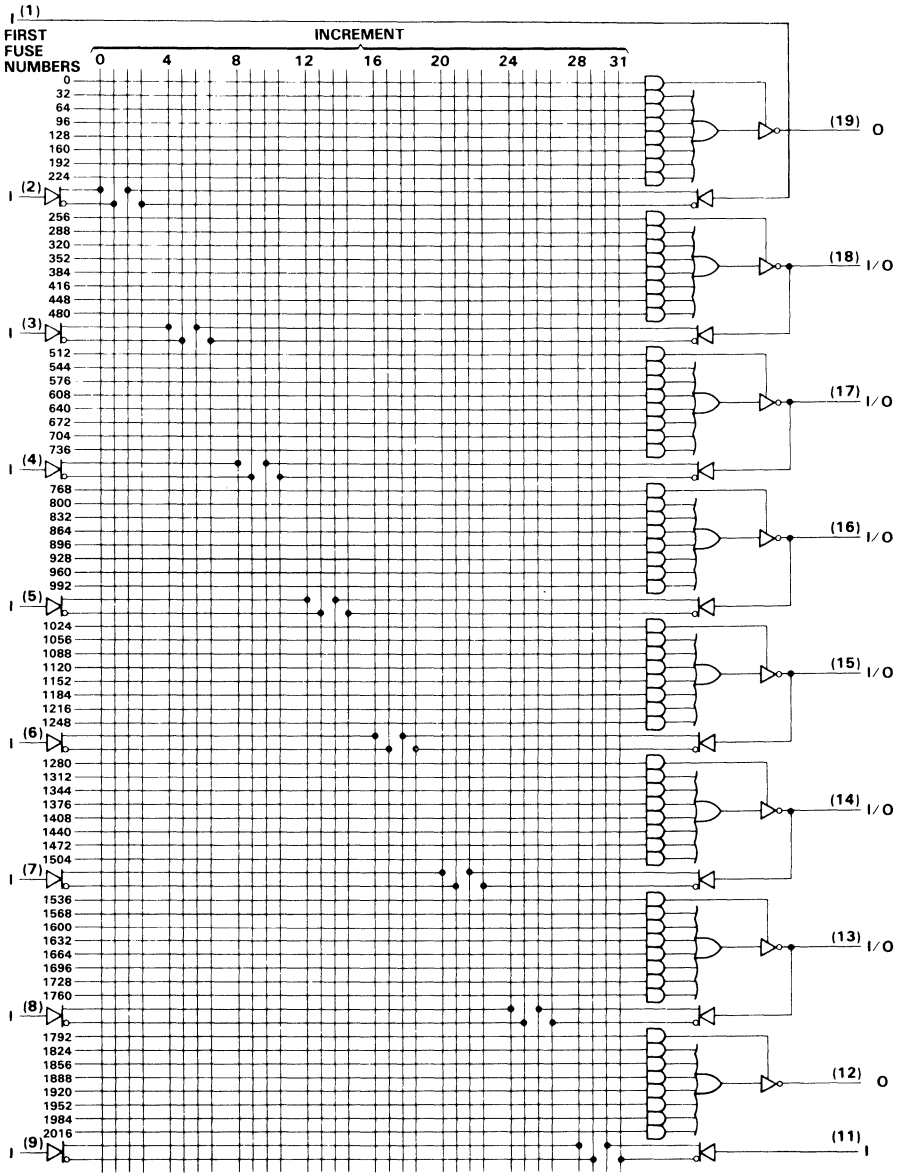
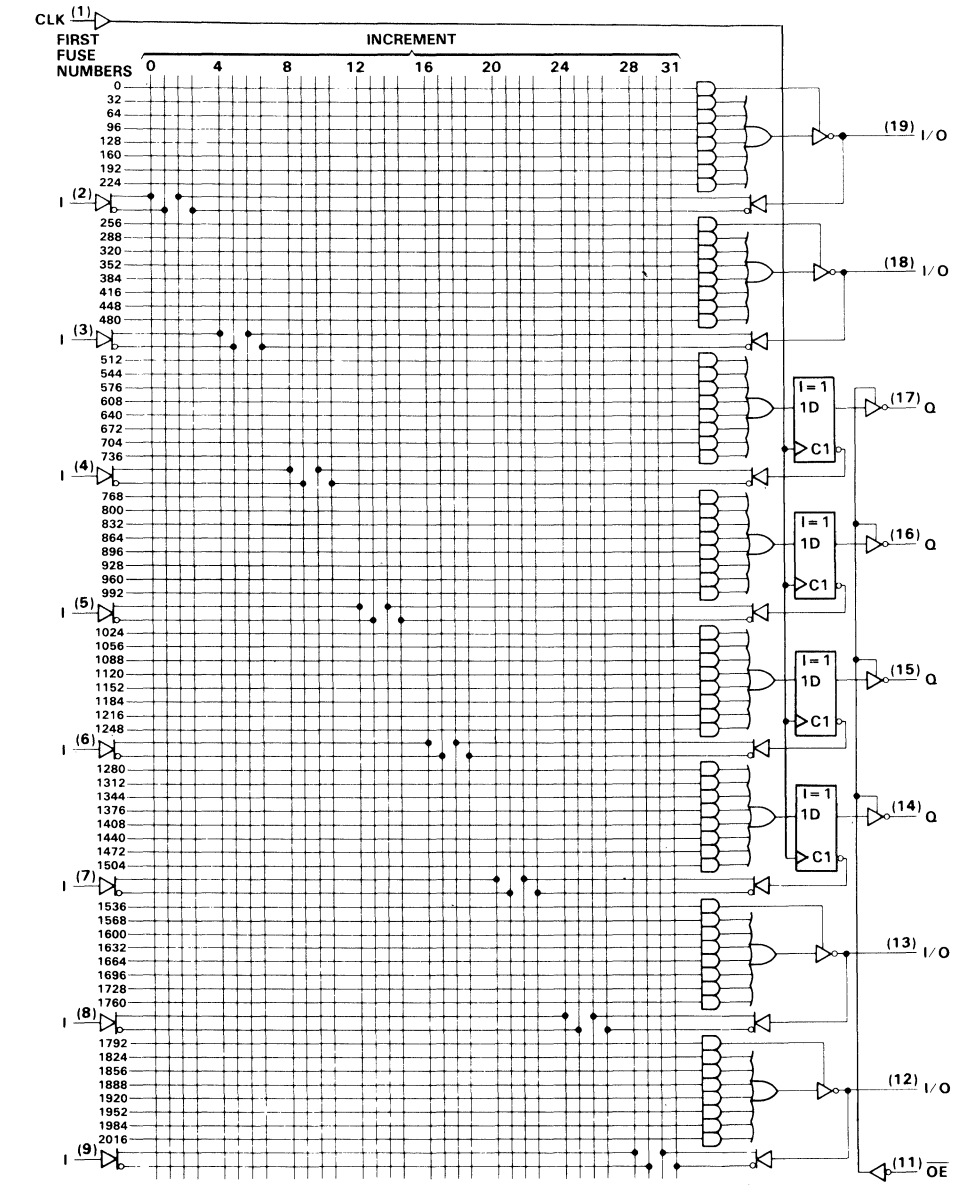


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

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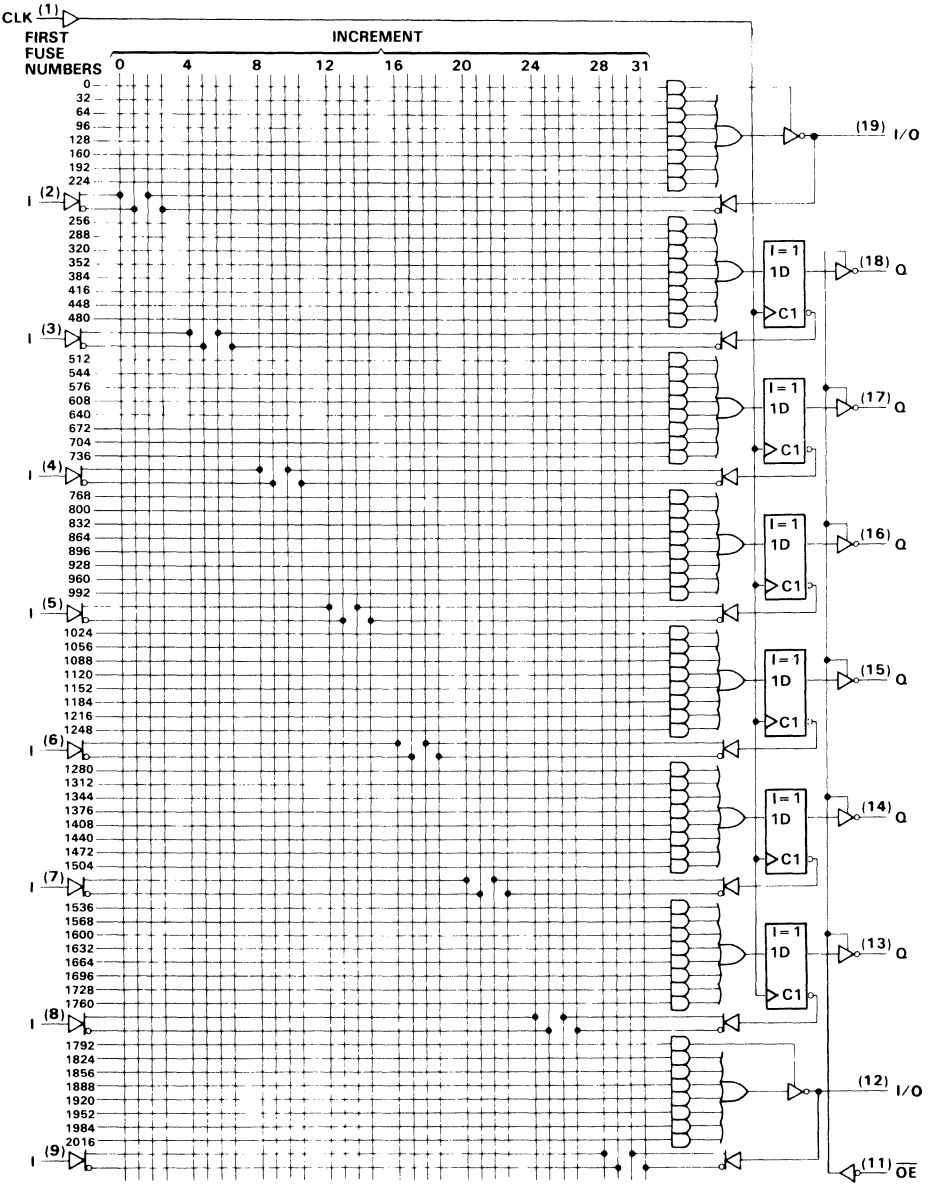
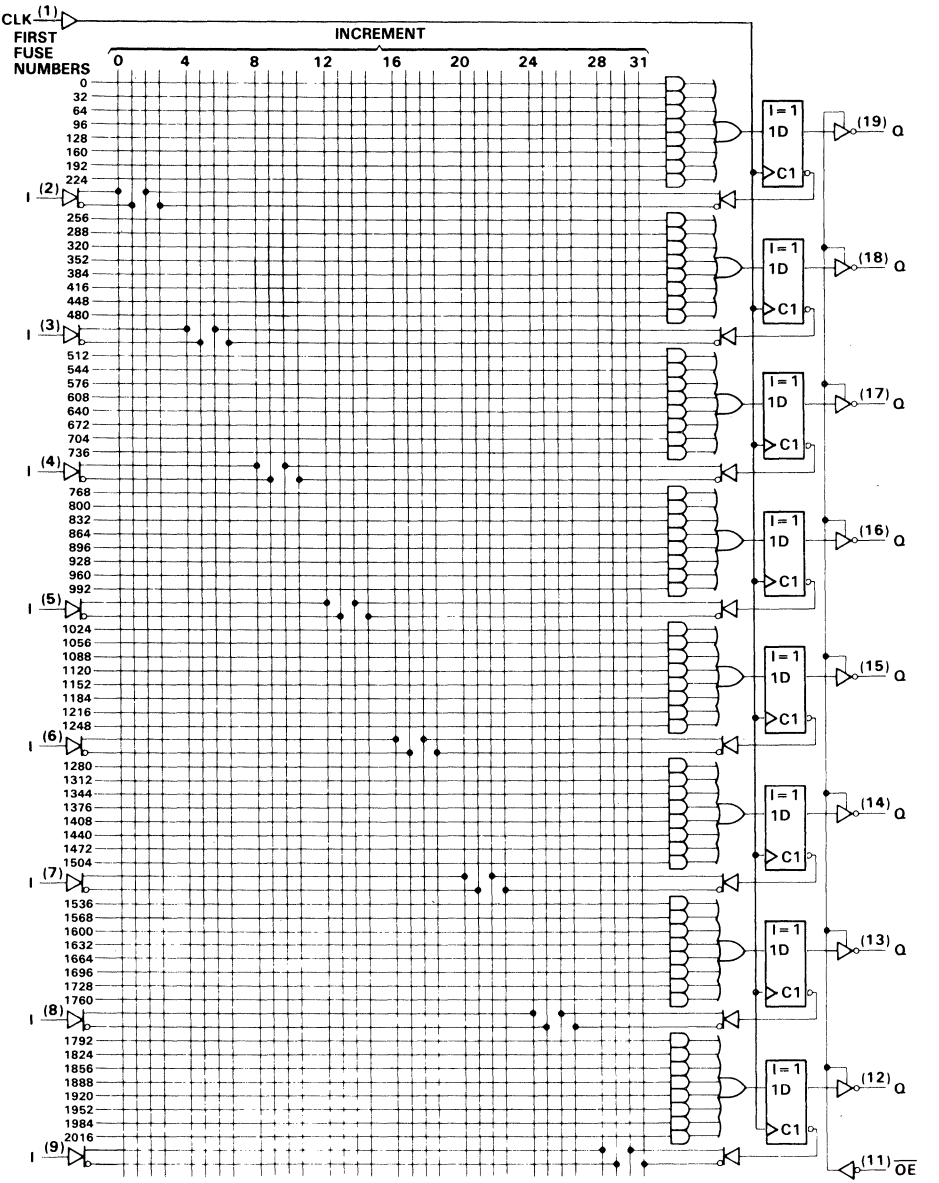


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		41.6	MHz
t_w	Pulse duration, clock (see Note 2)	High	10			ns
		Low	11			
t_{su}	Setup time, input or feedback before CLK↑		20			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		−55		125	°C

NOTE: 2. The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
	I/O ports					−250	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V	Pin 1, 11			0.2	mA
			All others			0.1	
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V	Pin 1, 11			50	μA
			I/O ports			100	
			All others			20	
I_{IL}		V_{CC} = 5.5 V, V_I = 0.4 V	I/O ports			−0.25	mA
			All others			−0.2	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0.5 V		−30		−250	mA
I_{CC}		V_{CC} = 5.5 V, V_I = 0, Outputs open			140	190	mA

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}			R1 = 390 Ω, R2 = 750 Ω, See Figure 1	41.6			MHz
t_{pd}	I, I/O	O, I/O			10	20	ns
t_{pd}	CLK↑	Q			8	15	ns
t_{en}	OE↓	Q			8	15	ns
t_{dis}	OE↑	Q			7	15	ns
t_{en}	I, I/O	O, I/O			10	20	ns
t_{dis}	I, I/O	O, I/O			10	20	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		50	MHz
t_w	Pulse duration, clock (see Note 2)	High	8			ns
		Low	9			
t_{su}	Setup time, input or feedback before CLK↑		15			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0		75	°C

NOTE 2: The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA		2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA			0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = 5.25 V, V_O = 2.7 V				20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.25 V, V_O = 0.4 V				−20	μA
	I/O ports					−250	
I_I		V_{CC} = 5.25 V, V_I = 5.5 V	Pin 1, 11			0.1	mA
			All others			0.1	
I_{IH}		V_{CC} = 5.25 V, V_I = 2.7 V	Pin 1, 11			20	μA
			All others			20	
I_{IL}		V_{CC} = 5.25 V, V_I = 0.4 V				−0.2	mA
I_O‡		V_{CC} = 5.25 V, V_O = 2.25 V		−30		−125	mA
I_{CC}		V_{CC} = 5.25 V, V_I = 0, Outputs open			140	180	mA

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}				50			MHz
t_{pd}	I, I/O	O, I/O			10	15	ns
t_{pd}	CLK↑	Q	R1 = 500 Ω,		8	12	ns
t_{en}	OE↓	Q	R2 = 500 Ω,		8	12	ns
t_{dis}	OE↑	Q	See Figure 1		7	10	ns
t_{en}	I, I/O	O, I/O			10	15	ns
t_{dis}	I, I/O	O, I/O			10	15	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 995-5666.

TEXAS INSTRUMENTS
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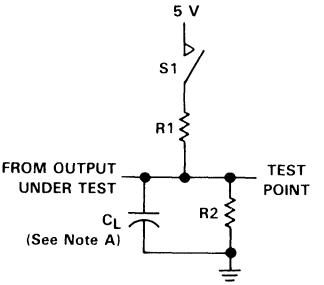
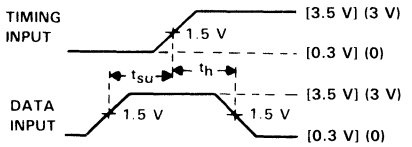
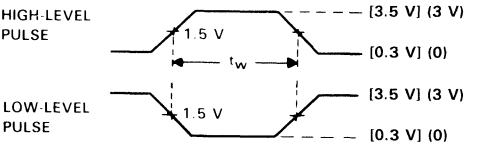
PARAMETER MEASUREMENT INFORMATION



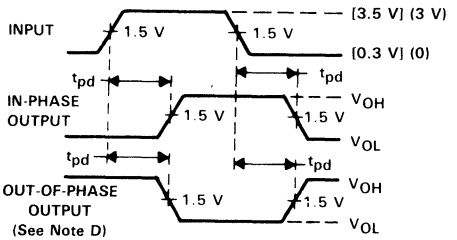
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



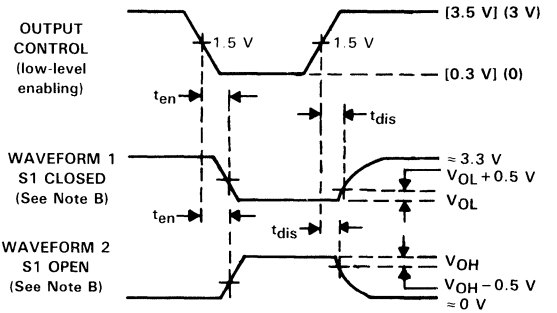
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For M suffix, use voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 1 MHz, t_r = t_f = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 1

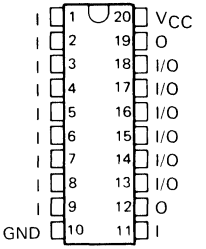
TIBPAL16L8-30M, TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
TIBPAL16L8-25C, TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

D3337, FEBRUARY 1984—REVISED AUGUST 1989

- **High-Performance Operation**
  - **Propagation Delay**
    - **M Suffix . . . 30 ns Max**
    - **C Suffix . . . 25 ns Max**
- **Functionally Equivalent, but Faster than PAL16L8A, PAL16R4A, PAL16R6A, and PAL16R8A**
- **Power-Up Clear on Registered Devices (All Registered Outputs are Set High but Voltage Levels at the Output Pins Go Low)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
M SUFFIX . . . J OR W PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
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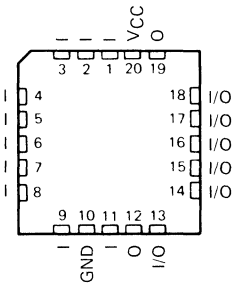
(TOP VIEW)



description

These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The PAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The PAL16' C series is characterized for operation from 0°C to 70°C.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
IMPACT is a trademark of Texas Instruments Incorporated.

PAL is a registered trademark of Monolithic Memories Incorporated

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TIBPAL16R4'
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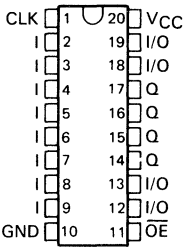
(TOP VIEW)



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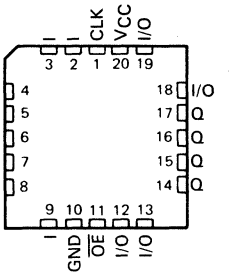

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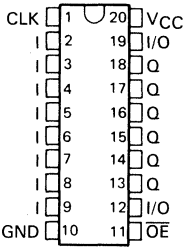

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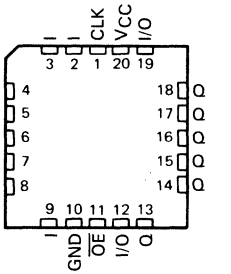

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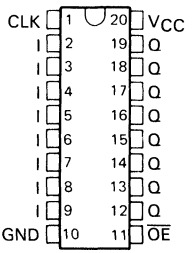

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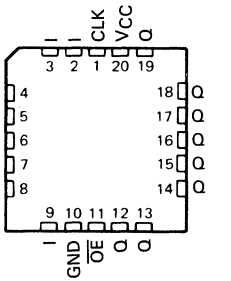

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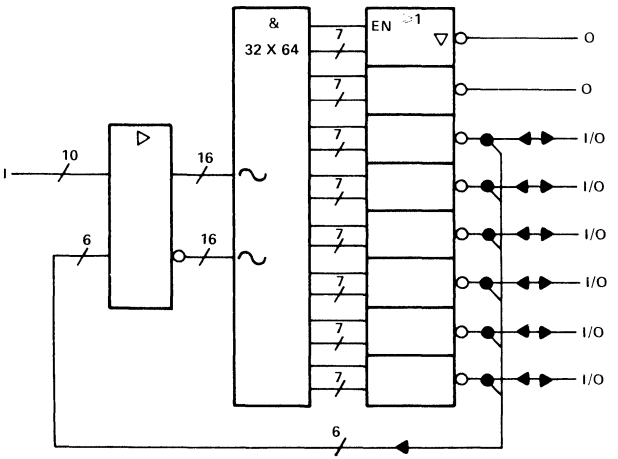
functional block diagrams (positive logic)

'PAL16L8



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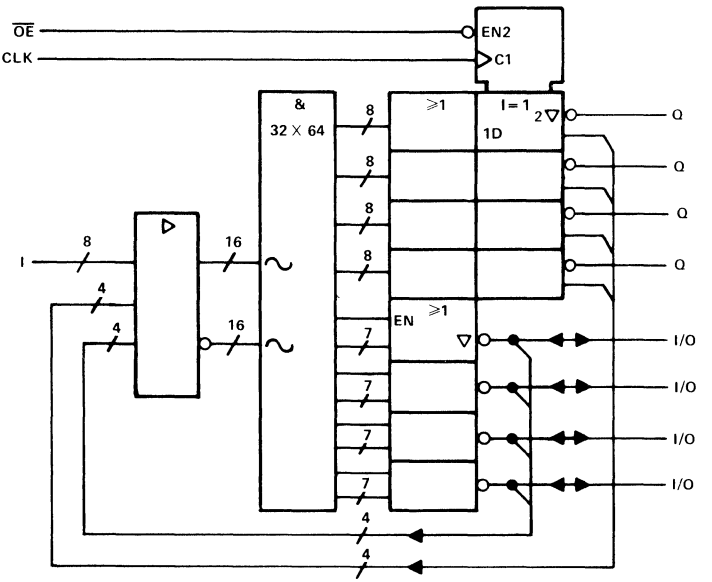
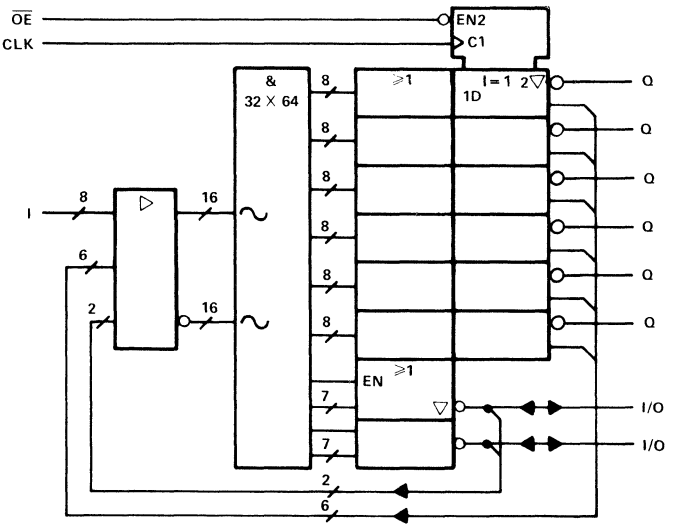


~ denotes fused inputs

functional block diagrams (positive logic)

'PAL16R6



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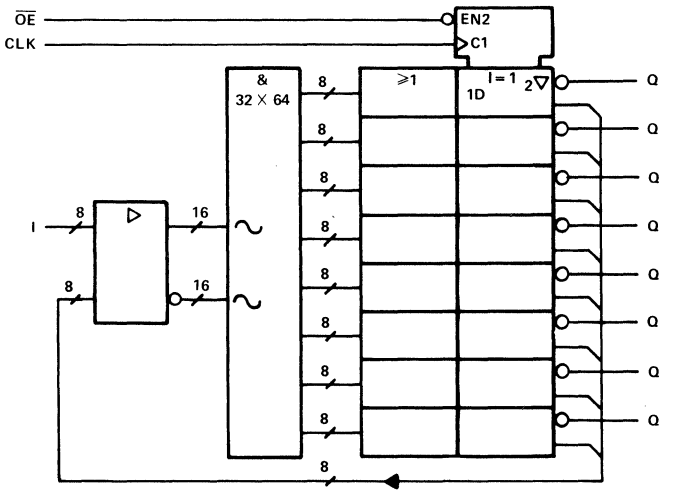

~ denotes fused inputs

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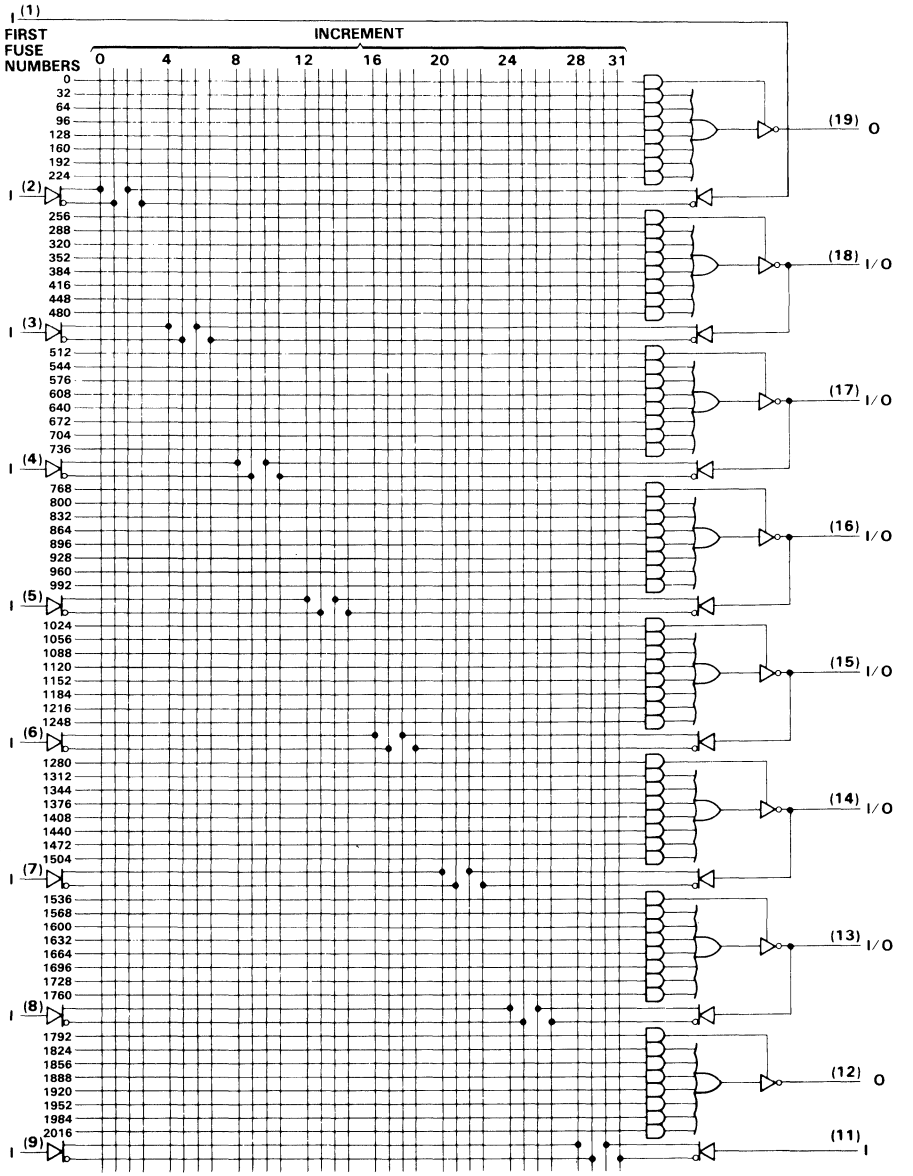
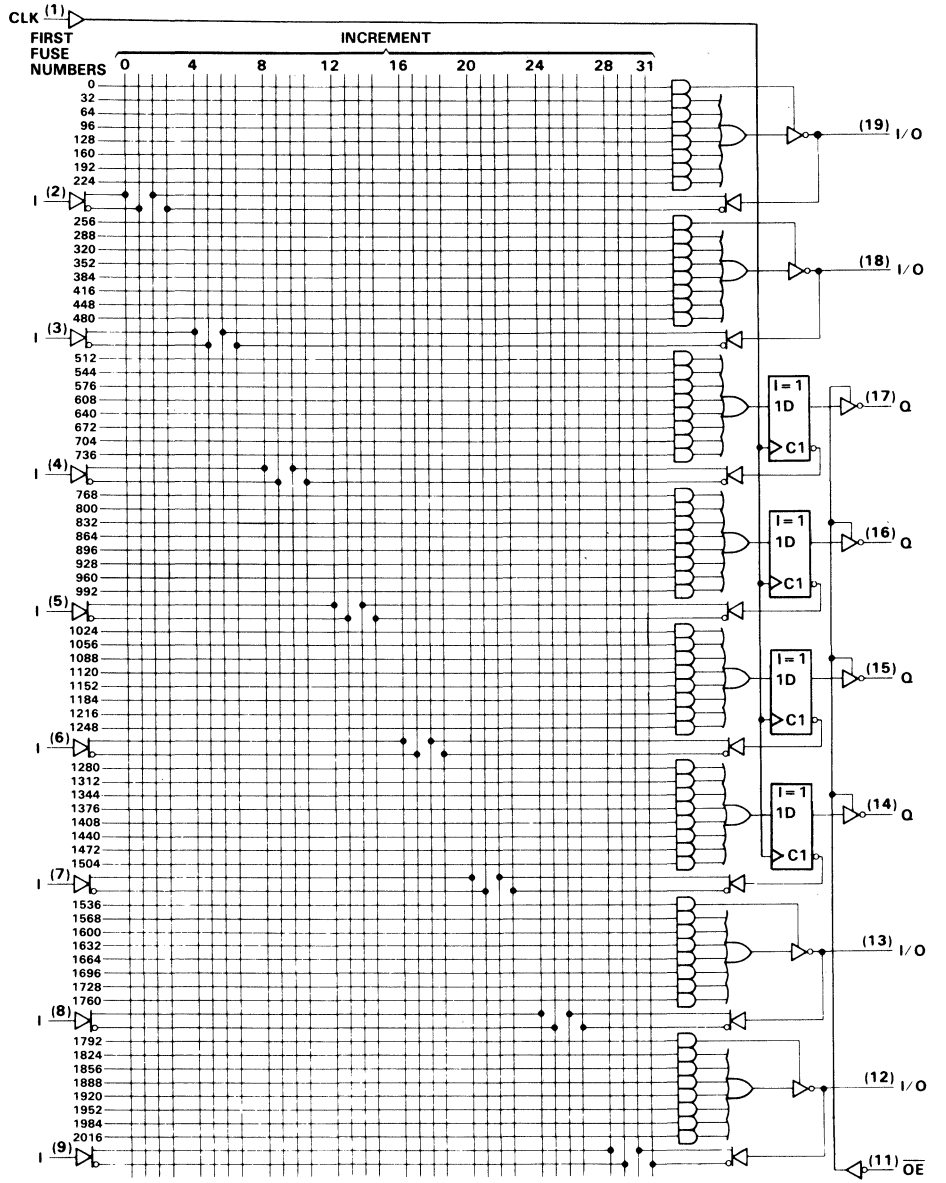


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

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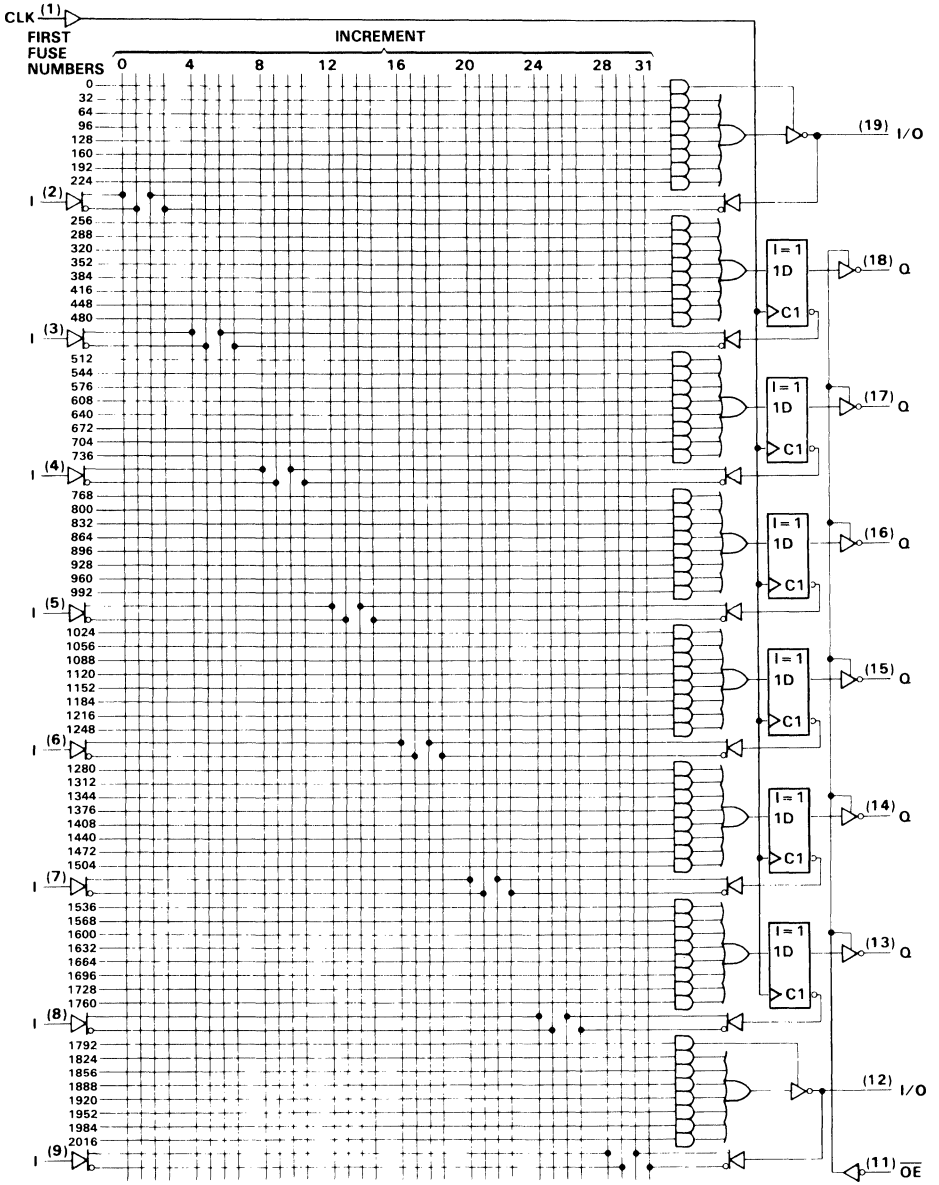
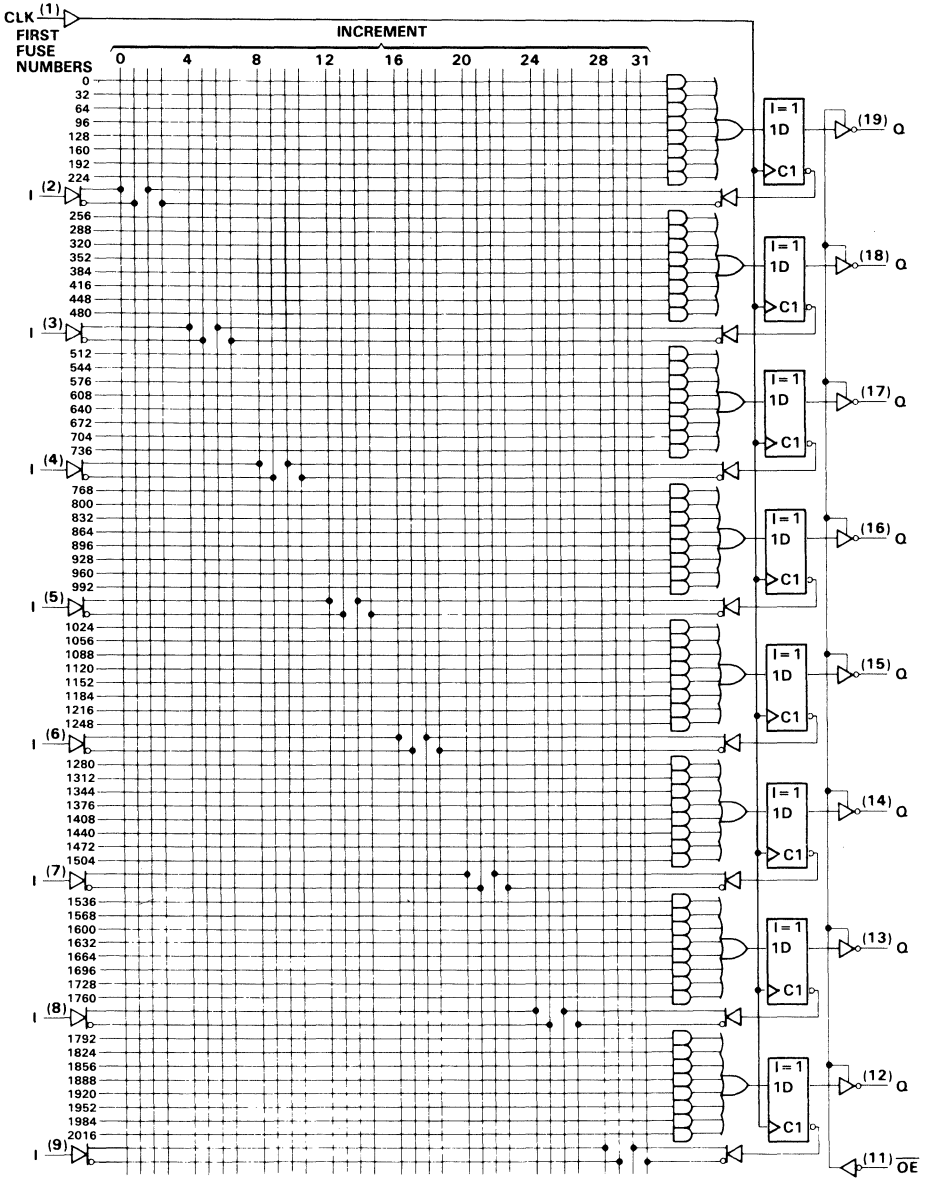


Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		25	MHz
t_w	Pulse duration, clock (see Note 2)	High	15			ns
		Low	20			
t_{su}	Setup time, input or feedback before CLK↑		25			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		−55		125	°C

NOTE 2: The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
	I/O ports					−250	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V	Pin 1, 11			0.2	mA
			All others			0.1	
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V	Pin 1, 11			50	μA
			I/O ports			100	
			All others			20	
I_{IL}		V_{CC} = 5.5 V, V_I = 0.4 V	I/O ports			−0.25	mA
			All others			−0.2	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0.5 V		−30		−250	mA
I_{CC}		V_{CC} = 5.5 V, V_I = 0, Outputs open			75	105	mA

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}				25			MHz
t_{pd}	I, I/O	O, I/O			15	30	ns
t_{pd}	CLK↑	Q	R1 = 390 Ω,		10	20	ns
t_{en}	OE↓	Q	R2 = 750 Ω,		15	25	ns
t_{dis}	OE↑	Q	See Figure 1		10	25	ns
t_{en}	I, I/O	O, I/O			14	30	ns
t_{dis}	I, I/O	O, I/O			13	30	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		30	MHz
t_w	Pulse duration, clock (see Note 2)	High	10			ns
		Low	15			
t_{su}	Setup time, input or feedback before CLK↑		20			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA		2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA			0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = 5.25 V, V_O = 2.7 V				20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.25 V, V_O = 0.4 V				−20	μA
	I/O ports					−250	
I_I		V_{CC} = 5.25 V, V_I = 5.5 V	Pin 1, 11			0.1	mA
			All others			0.1	
I_{IH}		V_{CC} = 5.25 V, V_I = 2.7 V	Pin 1, 11			20	μA
			All others			20	
I_{IL}		V_{CC} = 5.25 V, V_I = 0.4 V				−0.2	mA
I_O‡		V_{CC} = 5.25 V, V_O = 2.25 V		−30		−125	mA
I_{CC}		V_{CC} = 5.25 V, V_I = 0, Outputs open			75	100	mA

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}				30			MHz
t_{pd}	I, I/O	O, I/O			15	25	ns
t_{pd}	CLK↑	Q	R1 = 500 Ω,		10	15	ns
t_{en}	OE↓	Q	R2 = 500 Ω,		15	20	ns
t_{dis}	OE↑	Q	See Figure 1		10	20	ns
t_{en}	I, I/O	O, I/O			14	25	ns
t_{dis}	I, I/O	O, I/O			13	25	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 995-5666.

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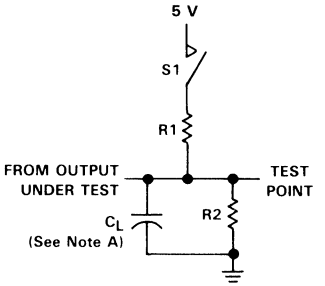
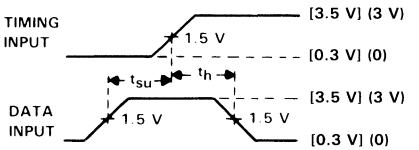
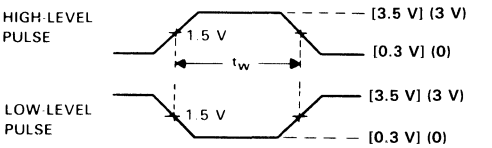
PARAMETER MEASUREMENT INFORMATION



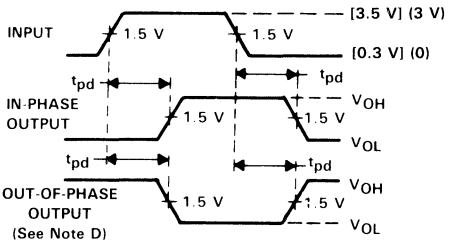
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



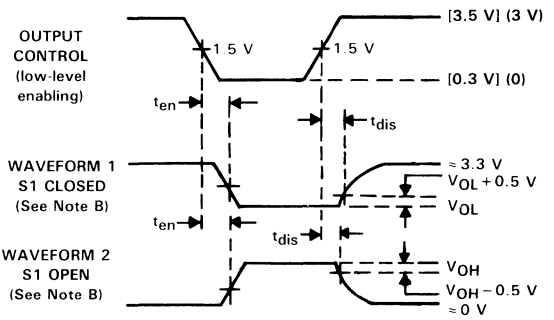
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

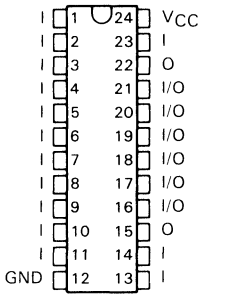
NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For M suffix, use voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 1

- **High-Performance Operation:**
  - f_{max} (no feedback)
    - TIBPAL20R'-5C Series . . . 125 MHz
    - TIBPAL20R'-7M Series . . . 100 MHz
  - f_{max} (internal feedback)
    - TIBPAL20R'-5C Series . . . 125 MHz
    - TIBPAL20R'-7M Series . . . 100 MHz
  - f_{max} (external feedback)
    - TIBPAL20R'-5C Series . . . 115 MHz
    - TIBPAL20R'-7M Series . . . 74 MHz
  - Propagation Delay
    - TIBPAL20R'-5C Series . . . 5 ns Max
    - TIBPAL20R'-7M Series . . . 7 ns Max
- **Functionally Equivalent, but Faster than, Existing 20-Pin PALs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8	14	2	0	6
'PAL20R4	12	0	4 (3-state buffers)	4
'PAL20R6	12	0	6 (3-state buffers)	2
'PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



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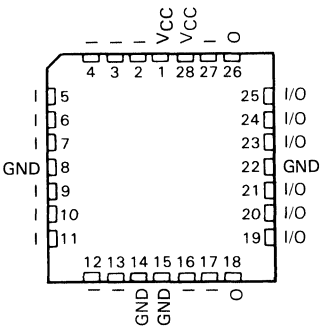
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board.

The TIBPAL20'M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL20'C series is characterized from 0°C to 75°C.

IMPACT-X is a trademark of Texas Instruments Incorporated
PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCT PREVIEW

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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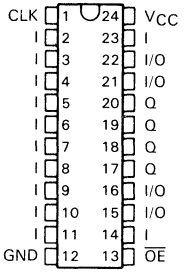
TIBPAL20R4'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R4'
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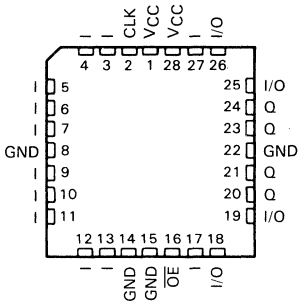
(TOP VIEW)



TIBPAL20R6'
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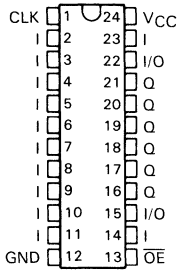
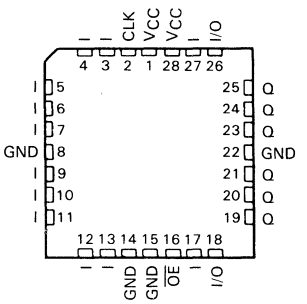
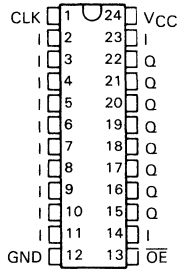
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



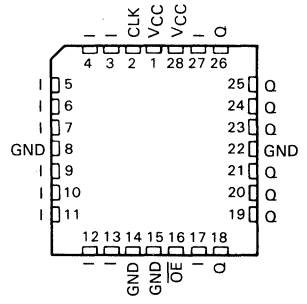
TIBPAL20R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)

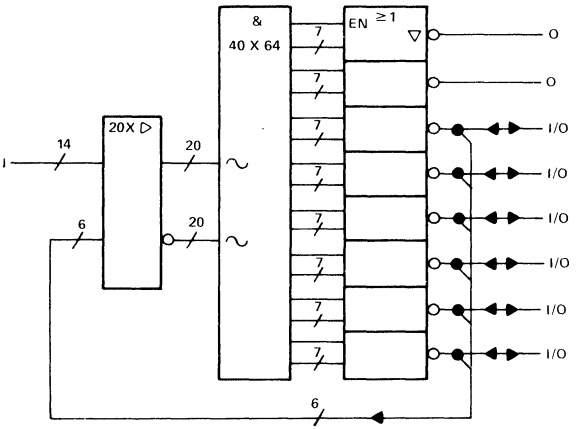


Pin assignments in operating mode

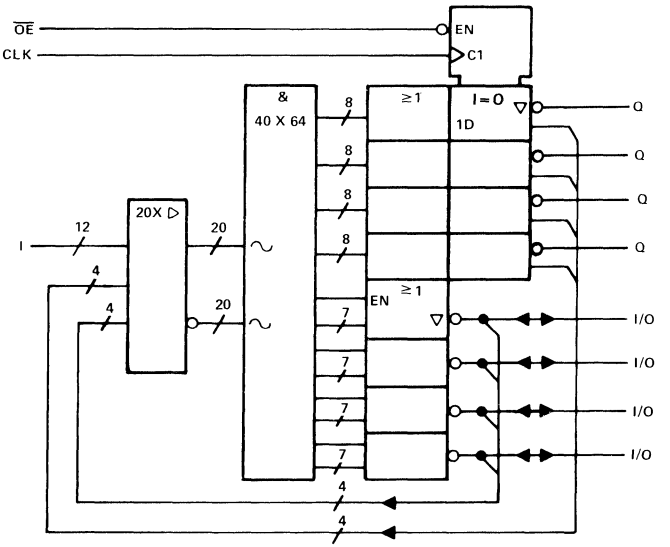
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

functional block diagrams (positive logic)

TIBPAL20L8'



TIBPAL20R4'



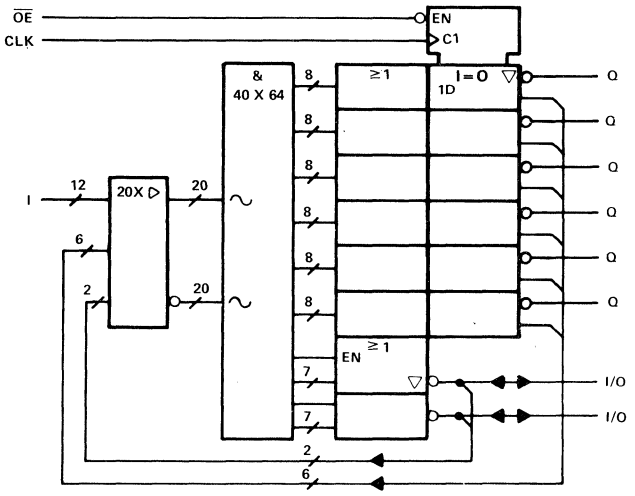
∼ denotes fused inputs

PRODUCT PREVIEW

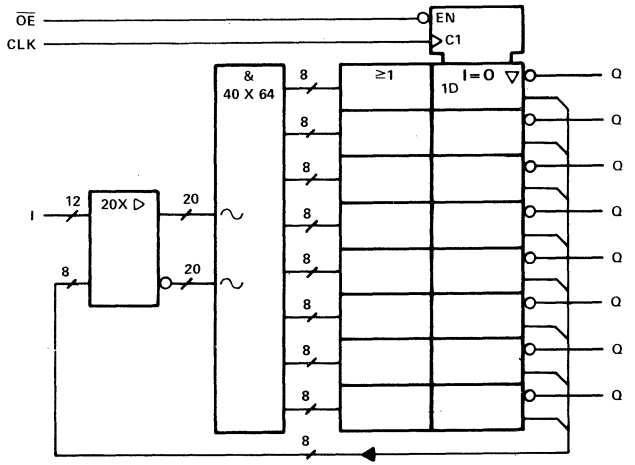
PRODUCT PREVIEW

functional block diagrams (positive logic)

TIBPAL20R6'



TIBPAL20R8'



∿ denotes fused inputs

TEXAS INSTRUMENTS
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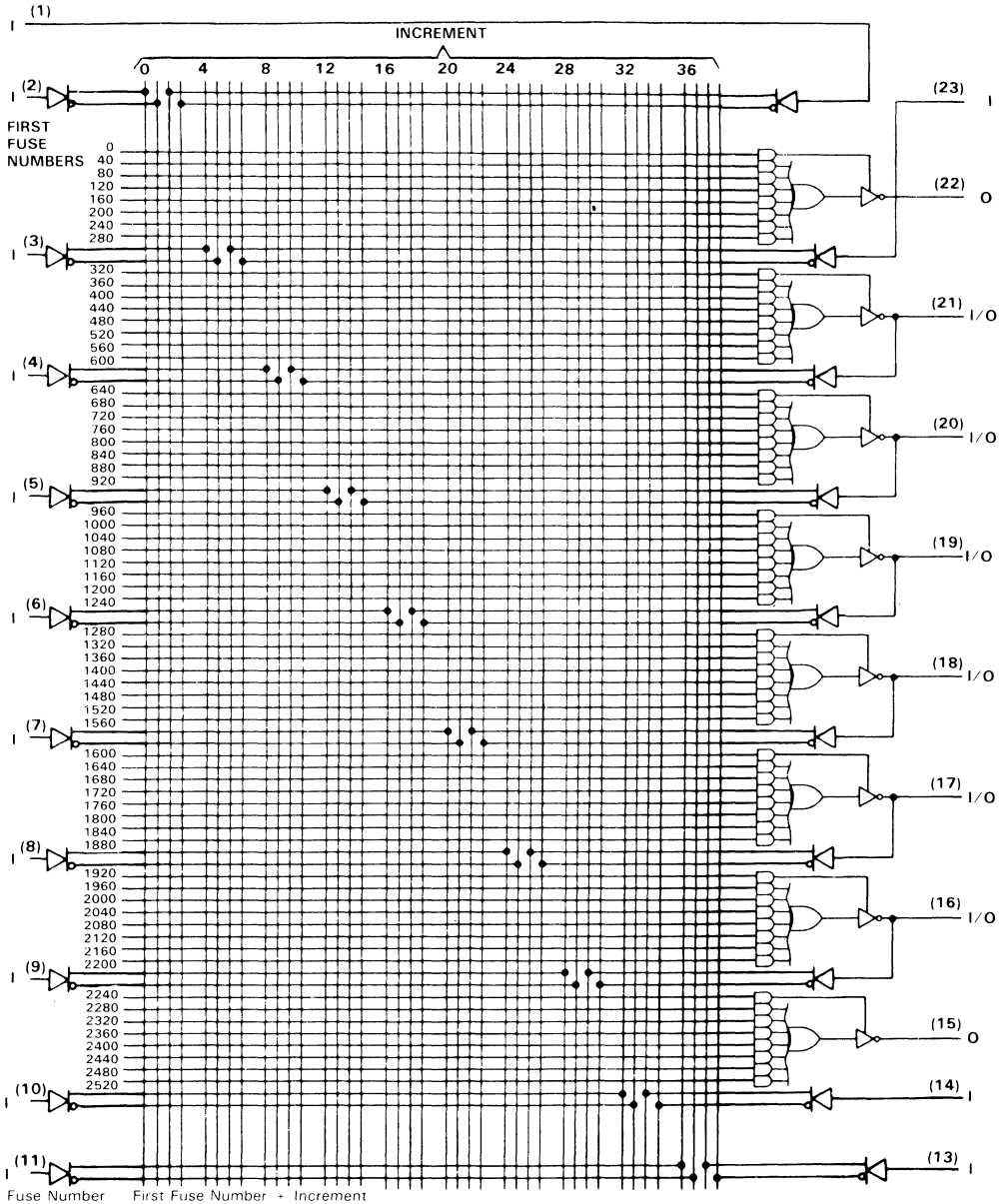
logic diagram (positive logic)



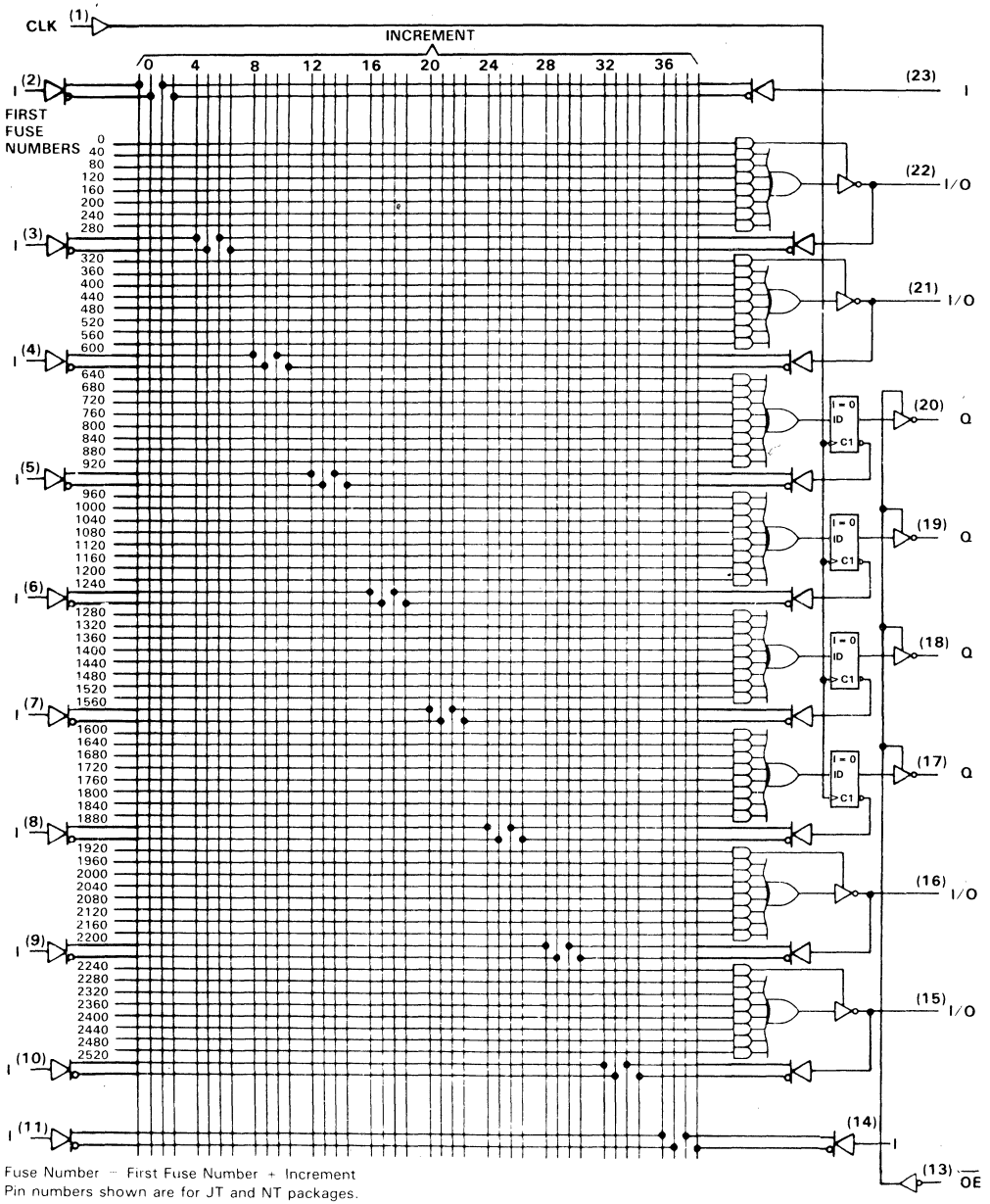
Fuse Number = First Fuse Number + Increment

Pin numbers shown are for JT and NT packages.

PRODUCT PREVIEW

PRODUCT PREVIEW

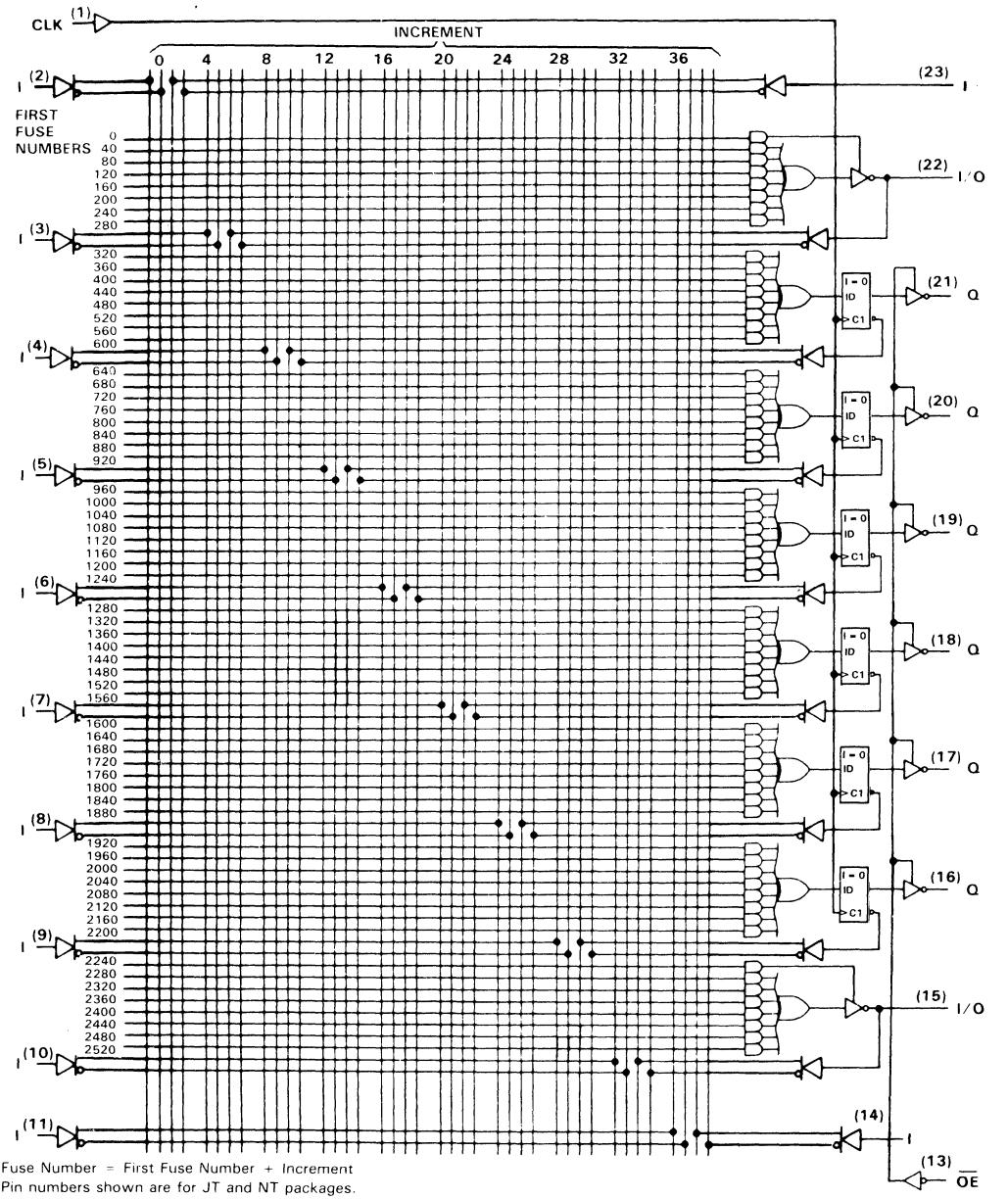
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram (positive logic)

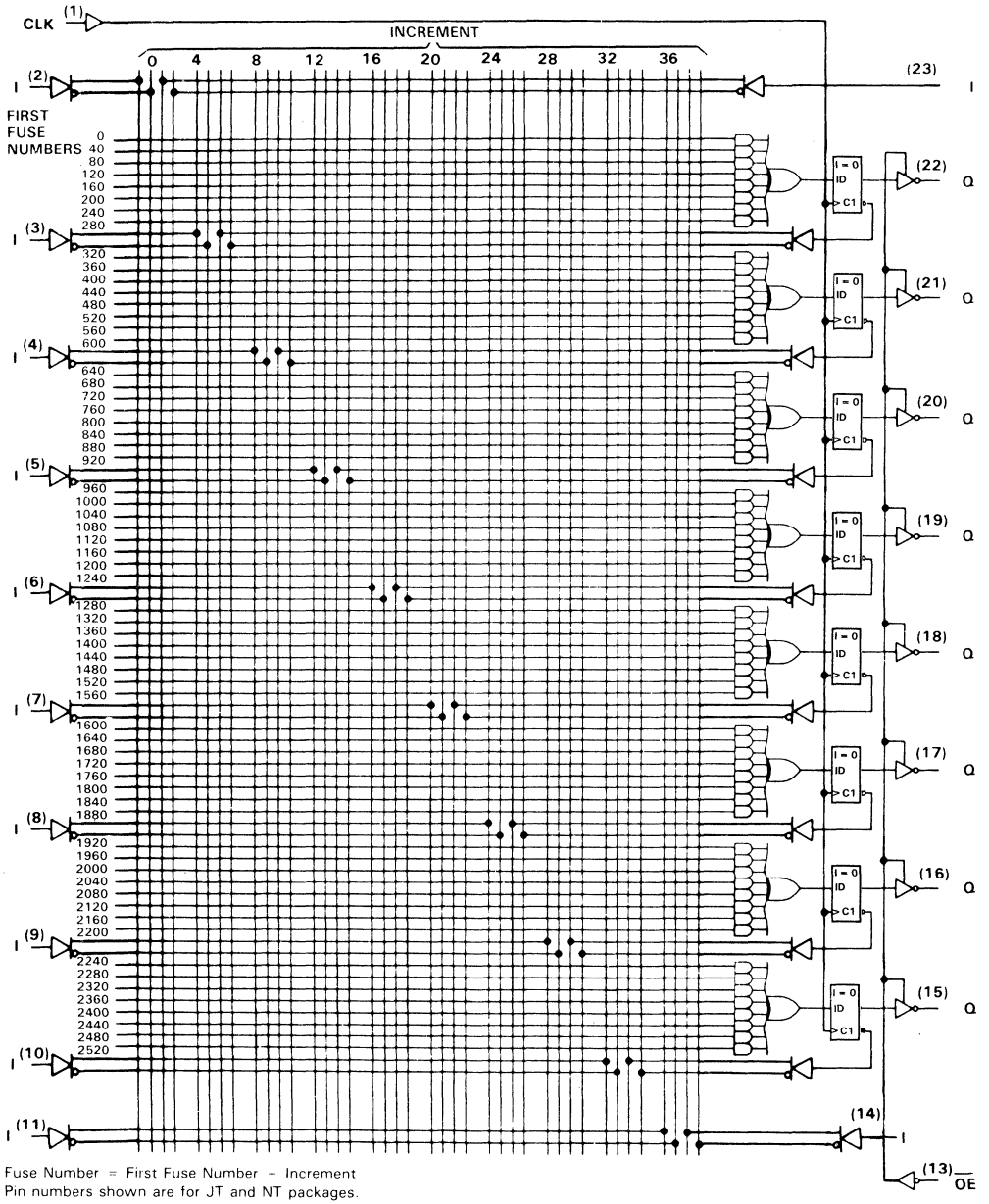


Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages.

PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		100	MHz
t_w	Pulse duration, clock	High	5			ns
		Low	5			ns
t_{su}	Setup time, input or feedback before CLK↑		7			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

PRODUCT PREVIEW

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.5	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			100	μA
I_{OZL}	O, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
	I/O ports					−0.25	mA
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V			100	μA
	All others					25	
I_{IL}	I/O ports	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	All others					−0.2	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V	−30	−70	−250	mA
I_{CC}		V_{CC} = 5.5 V, Outputs open,	V_I = 0, $\overline{OE}$ at V_{IH}			210	mA
C_i		f = 1 MHz,	V_I = 2 V				pF
C_o		f = 1 MHz,	V_O = 2 V				pF
C_{clk}		f = 1 MHz,	V_{CLK} = 2 V				pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed 1 second. Set V_O at 0.5 V to avoid test equipment ground degradation.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}§	without feedback		R1 = 200 Ω, R2 = 200 Ω, See Figure 1	100		MHz
	with internal feedback (counter configuration)			100		
	with external feedback			74		
t_{pd}	I, I/O	O, I/O				ns
t_{pd}	CLK	Q				ns
t_{en}	OE↓	Q				ns
t_{dis}	OE↑	Q				ns
t_{en}	I, I/O	O, I/O				ns
t_{dis}	I, I/O	O, I/O				ns

§ See f_{max} SPECIFICATIONS. f_{max} does not apply for TIBPAL20L8'.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration, clock	High	4			ns
		Low	4			ns
t_{su}	Setup time, input or feedback before CLK↑		4			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

PRODUCT PREVIEW

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4			V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
	I/O ports				100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
	I/O ports				−100	
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}‡		V_{CC} = 5.25 V, V_I = 2.7 V			25	μA
I_{IL}‡		V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0.5 V	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open, V_I = 0, $\overline{OE}$ at V_{IH}			210	mA
C_i		f = 1 MHz, V_I = 2 V				pF
C_o		f = 1 MHz, V_O = 2 V				pF
C_{clk}		f = 1 MHz, V_{CLK} = 2 V				pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed 1 second. Set V_O at 0.5 V to avoid test equipment ground degradation

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}§	without feedback		R1 = 200 Ω, R2 = 200 Ω, See Figure 1	125		MHz
	with internal feedback (counter configuration)			125		
	with external feedback			115		
t_{pd}	I, I/O	O, I/O			5	ns
t_{pd}	CLK↑	Q			4.5	ns
t_{pd}	CLK	Internal Feedback			3	ns
t_{en}	OE↓	Q			5.5	ns
t_{dis}	OE↑	Q			5.5	ns
t_{en}	I, I/O	O, I/O			6.5	ns
t_{dis}	I, I/O	O, I/O			6.5	ns
t_{skew}	Skew between registered outputs					ns

§ See f_{max} SPECIFICATIONS. f_{max} does not apply for TIBPAL20L8'.

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TEXAS INSTRUMENTS
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programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

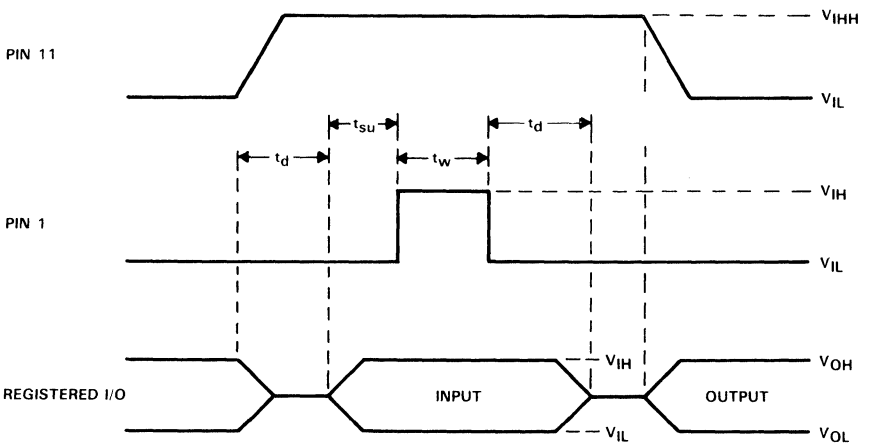
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 3)



NOTE 3: $t_d = t_{su} = t_w = 100$ ns to 1000 ns.
$V_{IHH} = 10.25$ V to 10.75 V.

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 1

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su} + t_h$). However, the minimum f_{max} is determined by the minimum clock period ($t_w$high + $t_w$low).

Thus, f_{max} without feedback $= \dfrac{1}{(t_w \text{ high} + t_w \text{ low})}$ or $\dfrac{1}{(t_{su} + t_h)}$.

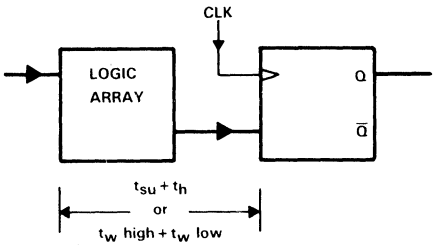


FIGURE 1. f_{max} WITHOUT FEEDBACK

f_{max} with internal feedback, see Figure 2

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus, f_{max} with internal feedback $= \dfrac{1}{(t_{su} + t_{pd} \text{ CLK-to-FB})}$.

Where t_{pd} CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

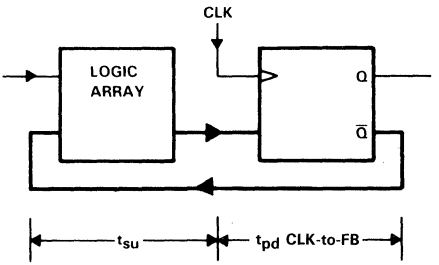


FIGURE 2. f_{max} WITH INTERNAL FEEDBACK

f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 3

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input and setup time for the external signals ($t_{su} + t_{pd}$ CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd} \text{ CLK-to-Q})}$.

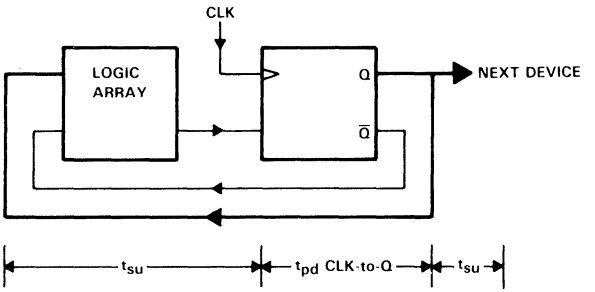


FIGURE 3. f_{max} WITH EXTERNAL FEEDBACK

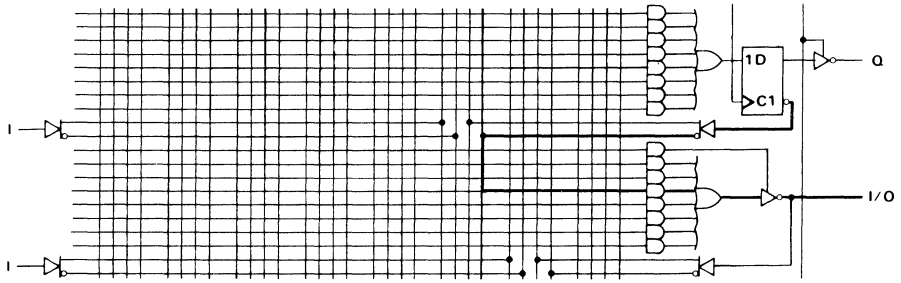
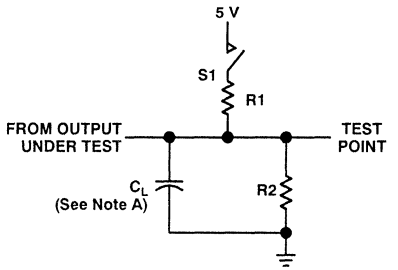


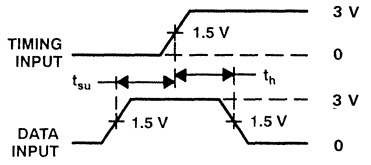
FIGURE 4. PROPAGATION DELAY FROM CLK↑ to I/O, THRU LOGIC ARRAY

PRODUCT PREVIEW

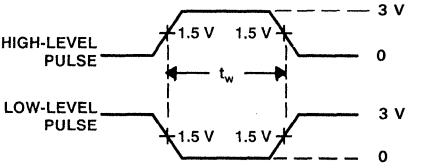
PARAMETER MEASUREMENT INFORMATION



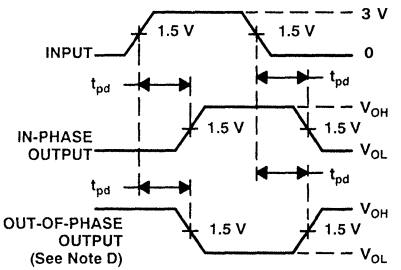
LOAD CIRCUIT FOR 3-STATE OUTPUTS



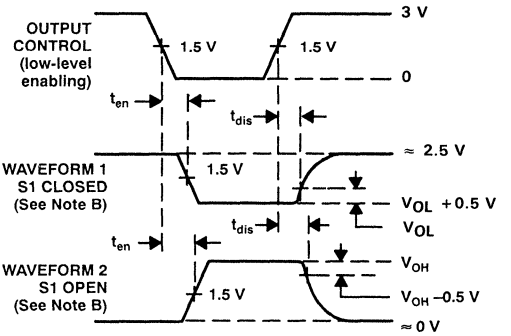
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 5

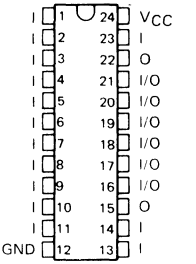
TIBPAL20L8-10M, TIBPAL20R4-10M, TIBPAL20R6-10M, TIBPAL20R8-10M
TIBPAL20L8-7C, TIBPAL20R4-7C, TIBPAL20R6-7C, TIBPAL20R8-7C
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

D3307, OCTOBER 1989

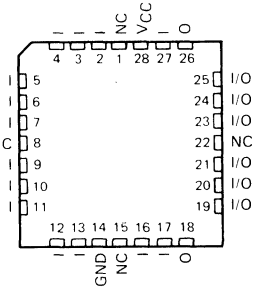
- **High-Performance Operation:**
  - f_{max} (no feedback)
    - TIBPAL20R'-7C Series . . . 100 MHz
    - TIBPAL20R'-10M Series . . . 62.5 MHz
  - f_{max} (internal feedback)
    - TIBPAL20R'-7C Series . . . 100 MHz
    - TIBPAL20R'-10M Series . . . 62.5 MHz
  - f_{max} (external feedback)
    - TIBPAL20R-7C Series . . . 74 MHz
    - TIBPAL20R'-10M Series . . . 55.5 MHz
  - Propagation Delay
    - TIBPAL20L'-7C . . . 7 ns Max
    - TIBPAL20L'-10M . . . 10 ns Max
- **Functionally Equivalent, but Faster than Existing 24-Pin PALs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8	14	2	0	6
'PAL20R4	12	0	4 (3-state buffers)	4
'PAL20R6	12	0	6 (3-state buffers)	2
'PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL20' C series is characterized for operation from 0°C to 75°C.

IMPACT-X™ is a trademark of Texas Instruments Incorporated.
PAL® is a registered trademark of Monolithic Memories, Inc.
† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

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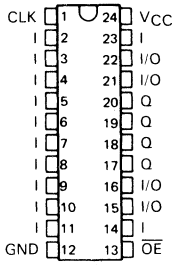
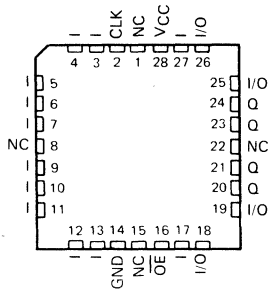
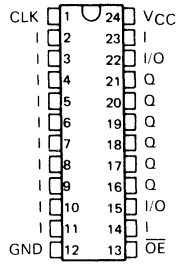
TIBPAL20R4'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



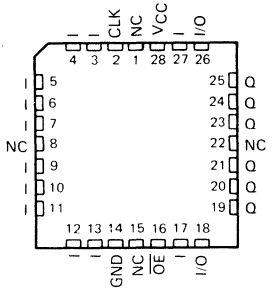
TIBPAL20R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



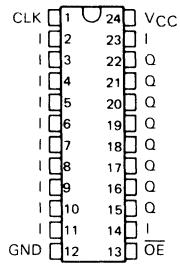
TIBPAL20R6'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



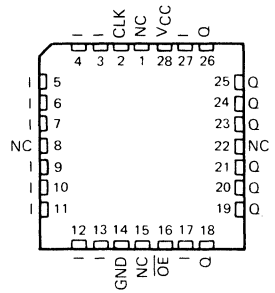
TIBPAL20R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

NC—No internal connection

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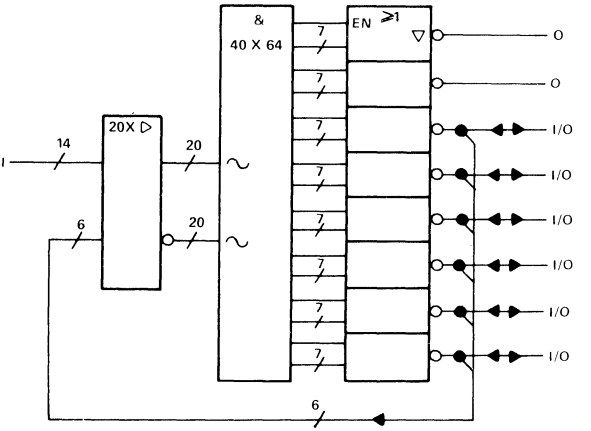
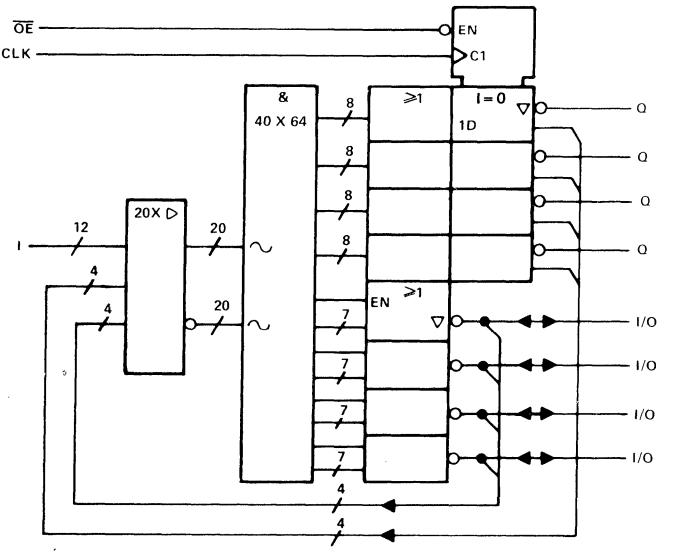
functional block diagrams (positive logic)

TIBPAL20L8'



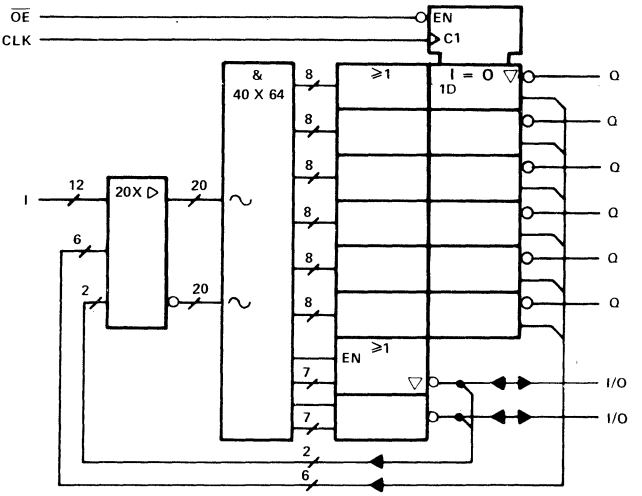
TIBPAL20R4'



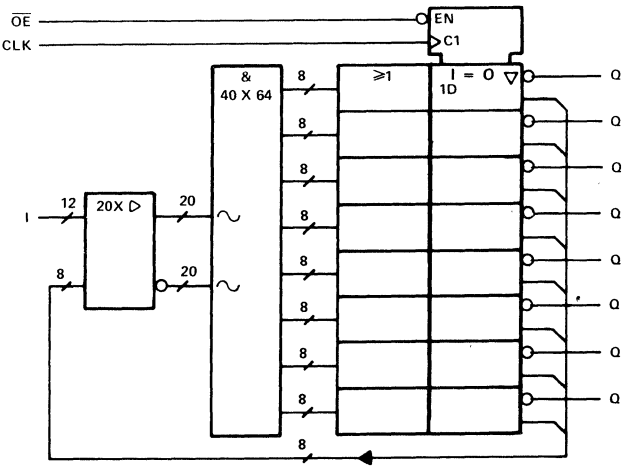
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'



TIBPAL20R8'



∿ denotes fused inputs

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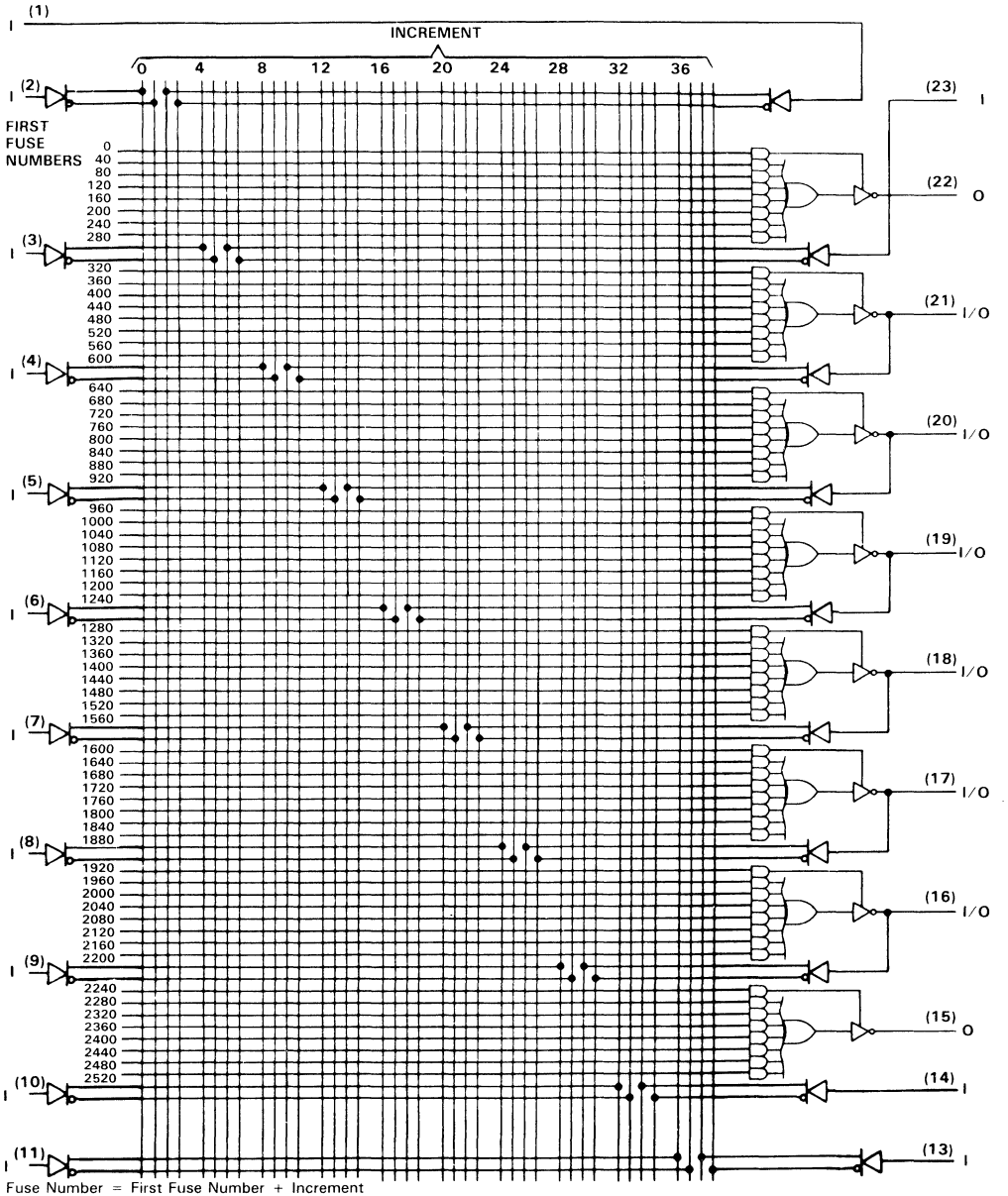
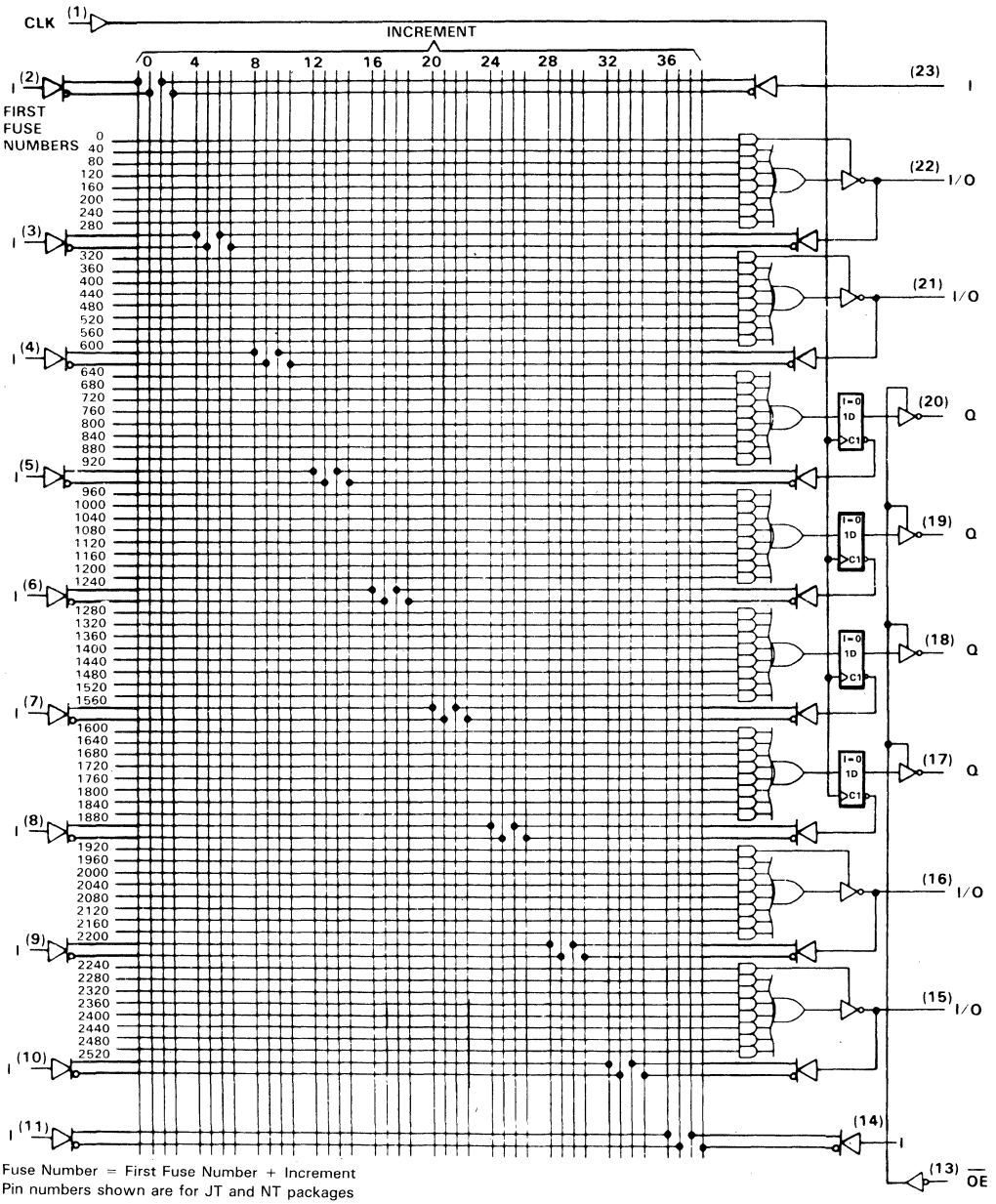
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages

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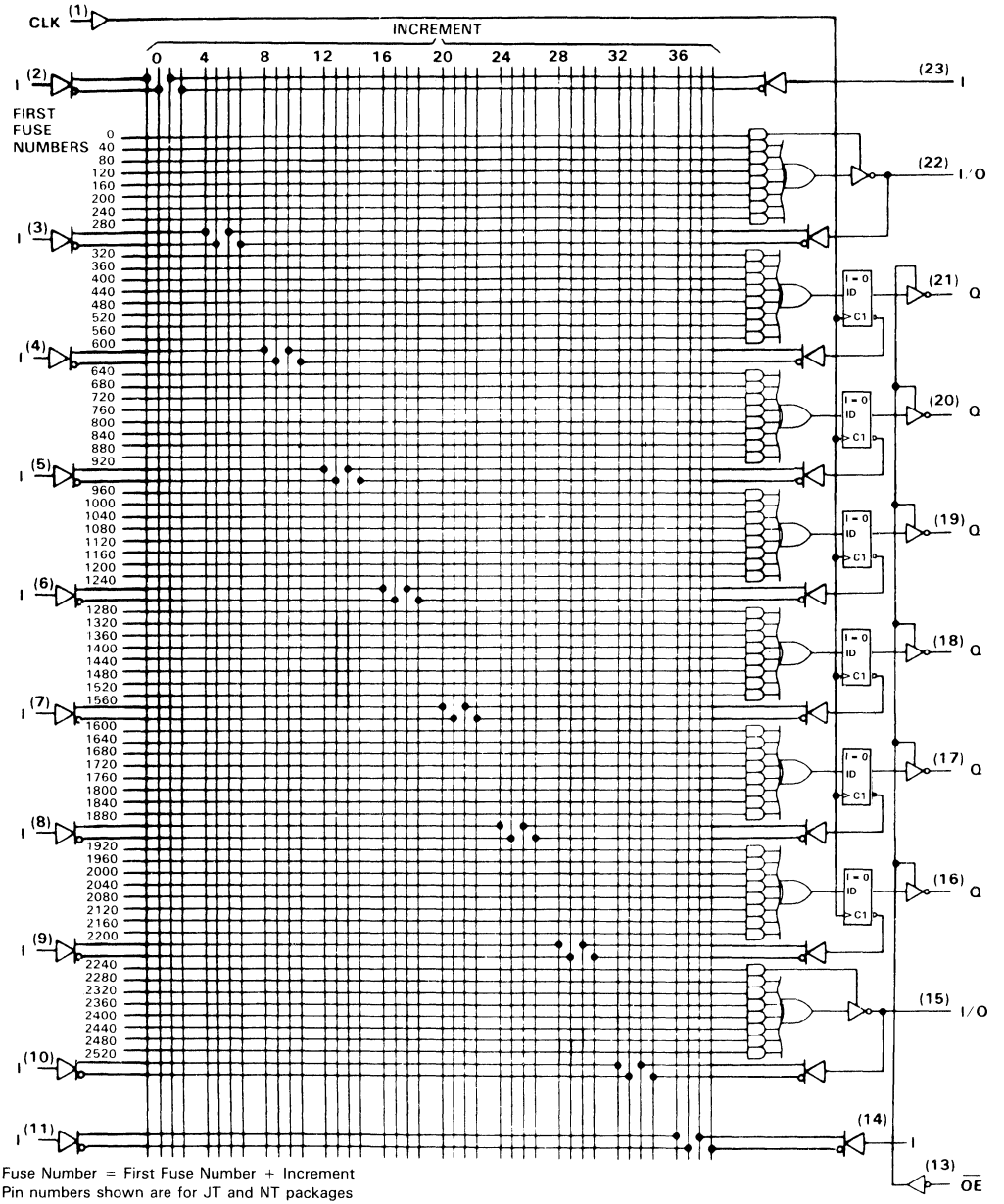
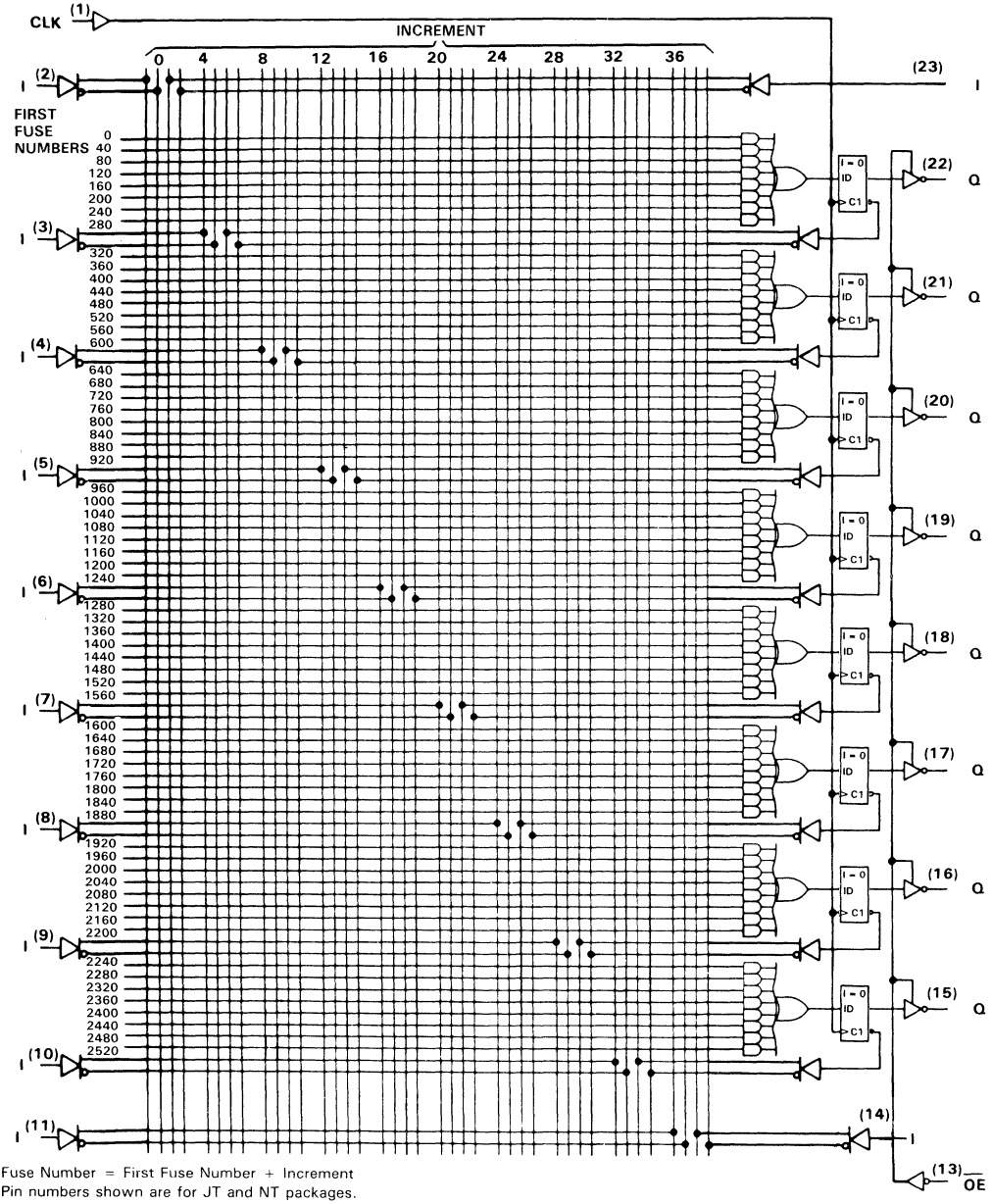
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		62.5	MHz
t_w	Pulse duration, clock (see Note 2)	High	8			ns
		Low	8			ns
t_{su}	Setup time, input or feedback before CLK↑		10			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.
NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.3	0.5	V
I_{OZH}‡	O, Q outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}‡	O, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				−20	μA
	I/O ports						−250	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	μA
	All others						25	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.08	−0.25	mA
I_{OS}§		V_{CC} = 5 V,	V_O = 0.5 V		−30	−70	−130	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs open	T_A = 25°C and 125°C		140	220	mA
		V_I = 0 V,	$\overline{OE}$ = V_{IH}	T_A = −55°C			250	
C_i		f = 1 MHz,	V_I = 2 V			5		pF
C_o		f = 1 MHz,	V_O = 2 V			6		pF
C_{clk}		f = 1 MHz,	V_{CLK} = 2 V			6		pF

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted) (see Figure 5)

PARAMETER	FROM	TO	MIN	TYP†	MAX	UNIT
f_{max}¶	Without feedback		62.5			MHz
	With internal feedback (counter configuration)		62.5			
	With external feedback		55.5			
t_{pd}	I, I/O	O, I/O	3	6	10	ns
t_{pd}	CLK↑	Q	2	4	8	ns
t_{pd}#	CLK↑	Feedback input			5	ns
t_{en}	OE↓	Q	2	4	10	ns
t_{dis}	OE↑	Q	2	4	10	ns
t_{en}	I, I/O	O, I/O	3	6	10	ns
t_{dis}	I, I/O	O, I/O	2	6	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.
¶ See section on f_{max} specifications.
# This parameter applies to TIBPAL20R4' and TIBPAL20R6' only (see Figure 2 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		100	MHz
t_w	Pulse duration, clock (see Note 2)	High	5			ns
		Low	5			ns
t_{su}	Setup time, input or feedback before CLK↑		7			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA		−0.8	−1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.7 V			100	μA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V			−100	μA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			0.2	mA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.7 V			25	μA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V		−0.08	−0.25	mA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0.5 V	−30	−70	−130	mA
I_{CC}	V_{CC} = 5.25 V, V_I = 0 V,	Outputs open		160	210	mA
C_i	f = 1 MHz,	V_I = 2 V		5		pF
C_o	f = 1 MHz,	V_O = 2 V		6		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V		6		pF

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted) (see Figure 6)

PARAMETER	FROM	TO		MIN	TYP†	MAX	UNIT
f_{max}¶	Without feedback			100			MHz
	With internal feedback (counter configuration)			100			
	With external feedback			74			
t_{pd}	I, I/O	O, I/O	1 or 2 outputs switching	3	5.5	7	ns
			8 outputs switching	3	6	7.5	
t_{pd}	CLK↑	Q		2	4	6.5	ns
t_{pd}#	CLK↑	Feedback input				3	ns
t_{en}	OE↓	Q		2	4	7.5	ns
t_{dis}	OE↑	Q		2	4	7.5	ns
t_{en}	I, I/O	O, I/O		3	6	9	ns
t_{dis}	I, I/O	O, I/O		2	6	9	ns
t_{skew}‖	Skew between registered outputs				0.5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.
¶ See section on f_{max} specifications.
# This parameter applies to TIBPAL20R4' and TIBPAL20R6' only (see Figure 2 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.
‖ This parameter is the measurement of the difference between the fastest and slowest t_{pd} (CLK-to-Q) observed when multiple registered outputs are switching in the same direction.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

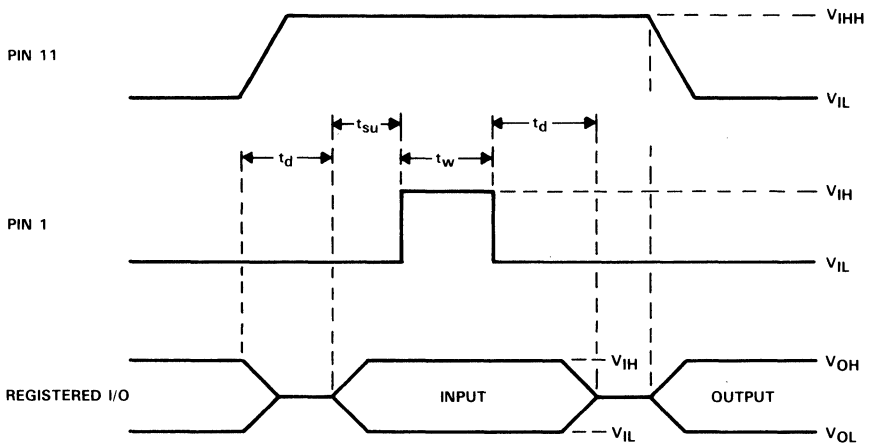
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 3)



NOTE 3: $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 1

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su}+t_h$). However, the minimum f_{max} is determined by the minimum clock period ($t_w$high + $t_w$low).

Thus, f_{max} without feedback $= \dfrac{1}{(t_w \text{ high} + t_w \text{ low})}$ or $\dfrac{1}{(t_{su}+t_h)}$.

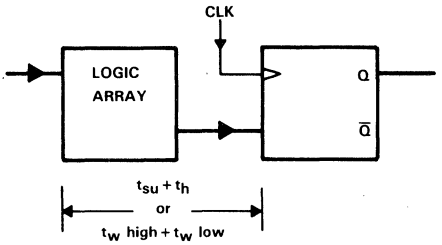


FIGURE 1. f_{max} WITHOUT FEEDBACK

f_{max} with internal feedback, see Figure 2

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus, f_{max} with internal feedback $= \dfrac{1}{(t_{su}+t_{pd} \text{ CLK-to-FB})}$.

Where t_{pd} CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

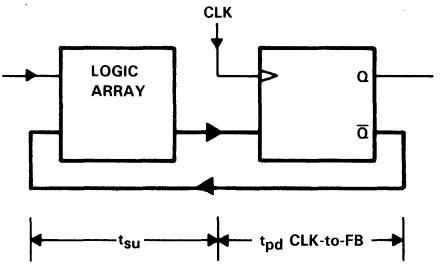


FIGURE 2. f_{max} WITH INTERNAL FEEDBACK

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f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 3

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input and setup time for the external signals ($t_{su} + t_{pd}$ CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd} \text{ CLK-to-Q})}$.

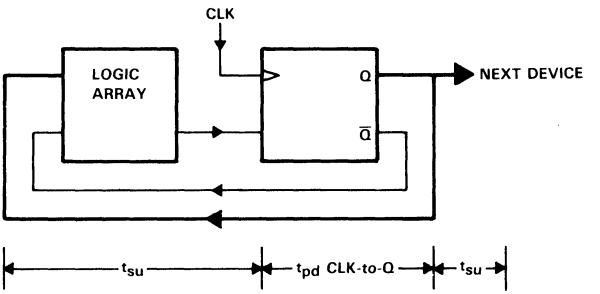


FIGURE 3. f_{max} WITH EXTERNAL FEEDBACK

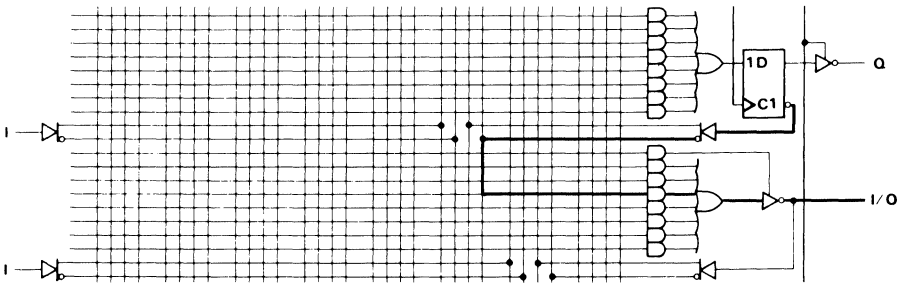
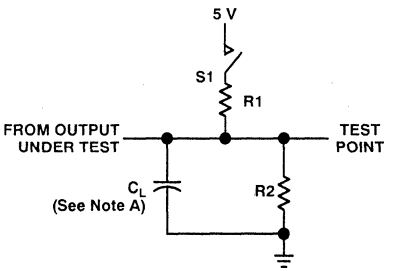
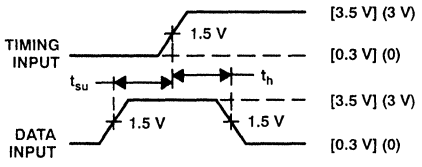


FIGURE 4. PROPAGATION DELAY FROM CLK↑ to I/O, THRU LOGIC ARRAY

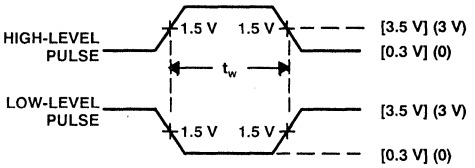
PARAMETER MEASUREMENT INFORMATION



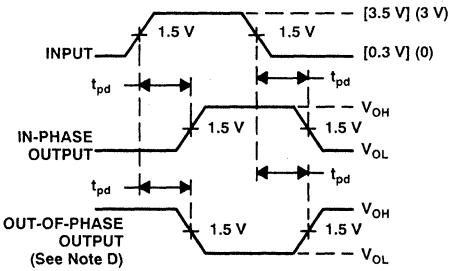
LOAD CIRCUIT FOR 3-STATE OUTPUTS



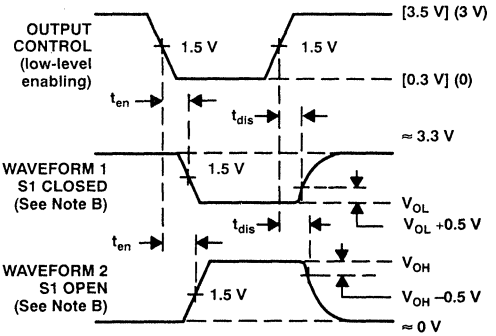
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For M suffix use the voltage levels indicated in parentheses. For C suffix, use the voltage levels indicated in brackets [ ].
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 5

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

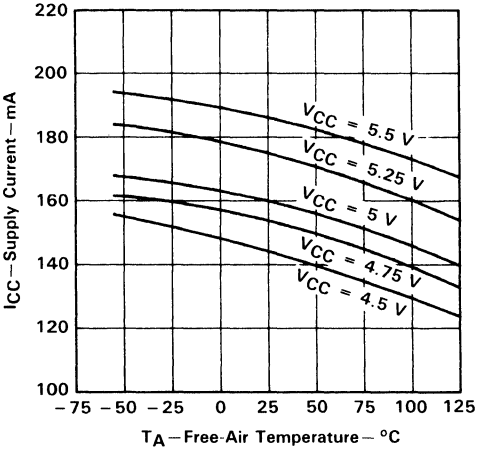

FIGURE 6

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

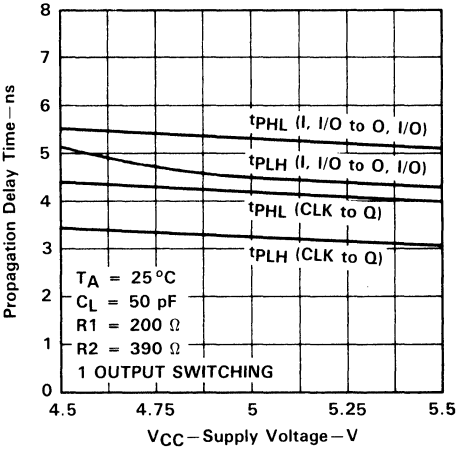

FIGURE 7

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

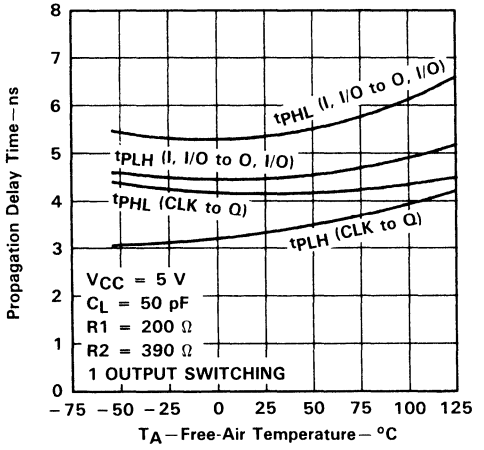

FIGURE 8

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

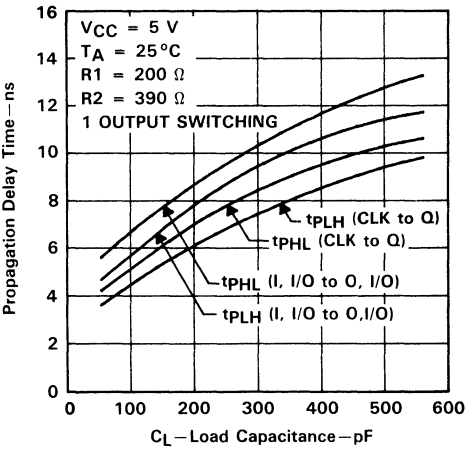

FIGURE 9

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
FREQUENCY
8-BIT COUNTER MODE

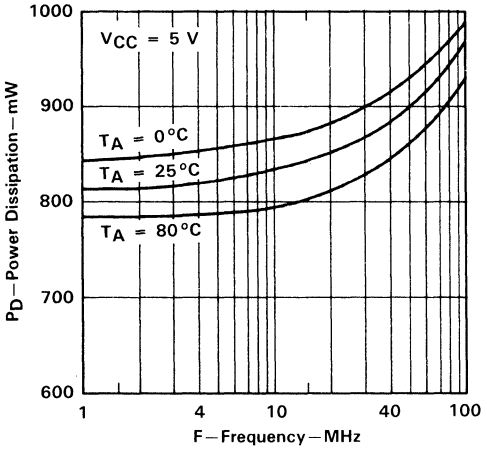

FIGURE 10

SKEW BETWEEN OUTPUTS†
vs
NUMBER OF OUTPUTS SWITCHING

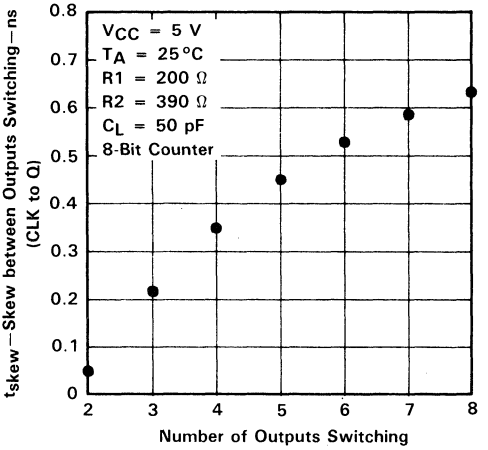

FIGURE 11

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

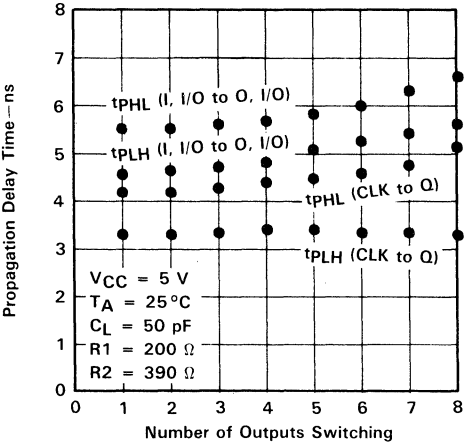

FIGURE 12

†Output switching in the same direction (t_{PLH} compared to t_{PLH}/t_{PHL} to t_{PHL})

TEXAS INSTRUMENTS
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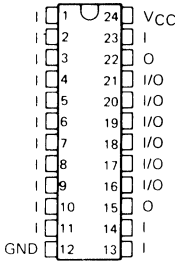
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

D3336, OCTOBER 1989

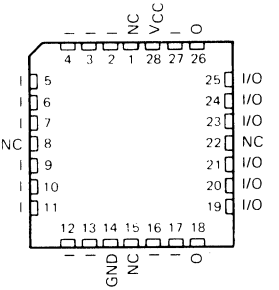
- High-Performance Operation:
  - f_{max} (w/o feedback)
    - TIBPAL20R'-10C Series . . . 71.4 MHz
    - TIBPAL20R'-12M Series . . . 62.5 MHz
  - f_{max} (internal feedback)
    - TIBPAL20R'-10C Series . . . 58.8 MHz
    - TIBPAL20R'-12M Series . . . 52.6 MHz
  - f_{max} (external feedback)
    - TIBPAL20R'-10C Series . . . 55.5 MHz
    - TIBPAL20R'-12M Series . . . 48 MHz
  - Propagation Delay
    - TIBPAL20L'-10C . . . 10 ns Max
    - TIBPAL20L'-12M . . . 12 ns Max
- Functionally Equivalent to, but Faster than, Existing 24-Pin PALs
- Preload Capability on Output Registers Simplifies Testing
- Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Security Fuse Prevents Duplication
- Dependable Texas Instruments Quality and Reliability

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8	14	2	0	6
'PAL20R4	12	0	4 (3-state buffers)	4
'PAL20R6	12	0	6 (3-state buffers)	2
'PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are also available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20'M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL20'C series is characterized from 0°C to 75°C.

IMPACT-X is a trademark of Texas Instruments Incorporated
PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

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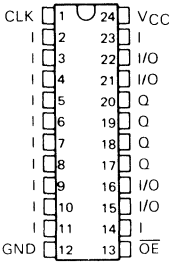
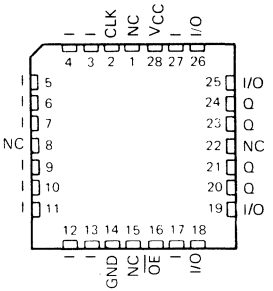
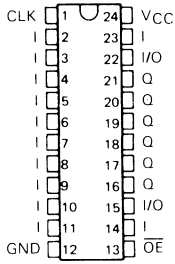
TIBPAL20R4'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



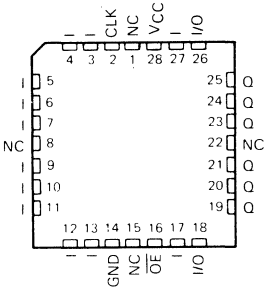
TIBPAL20R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



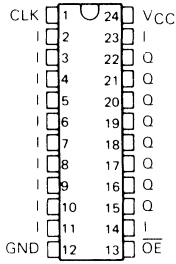
TIBPAL20R6'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



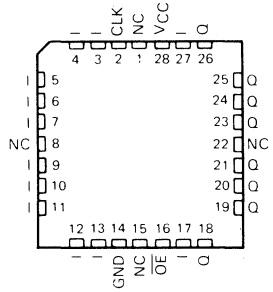
TIBPAL20R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

NC—No internal connection

TEXAS INSTRUMENTS
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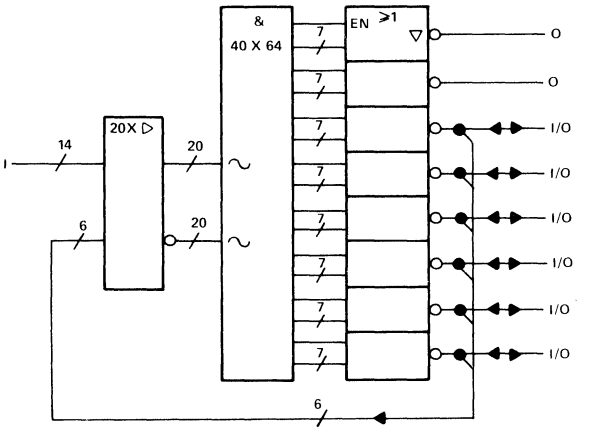
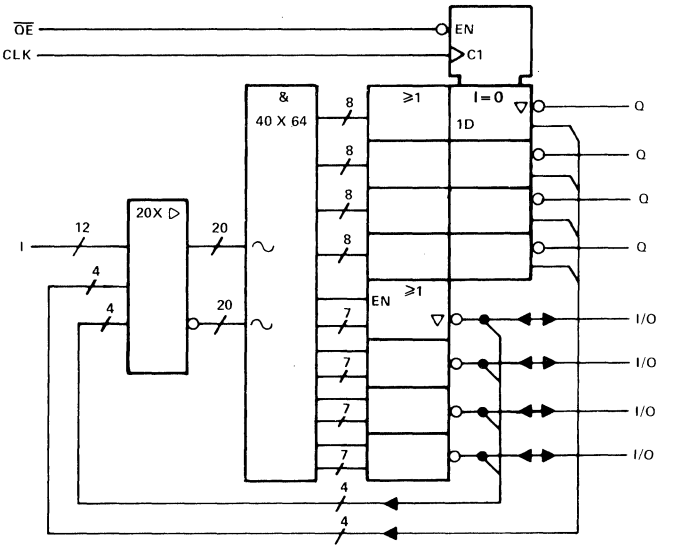
functional block diagrams (positive logic)

TIBPAL20L8'



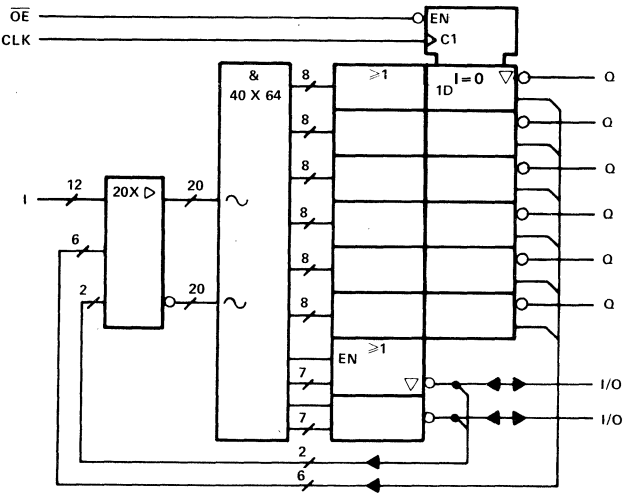
TIBPAL20R4'



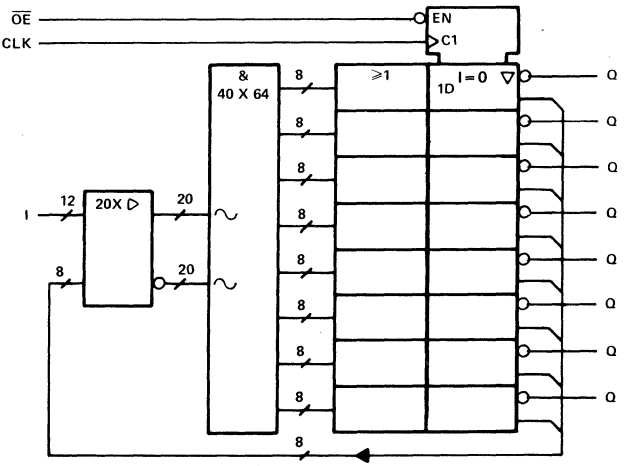
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'



TIBPAL20R8'



∿ denotes fused inputs

TEXAS INSTRUMENTS
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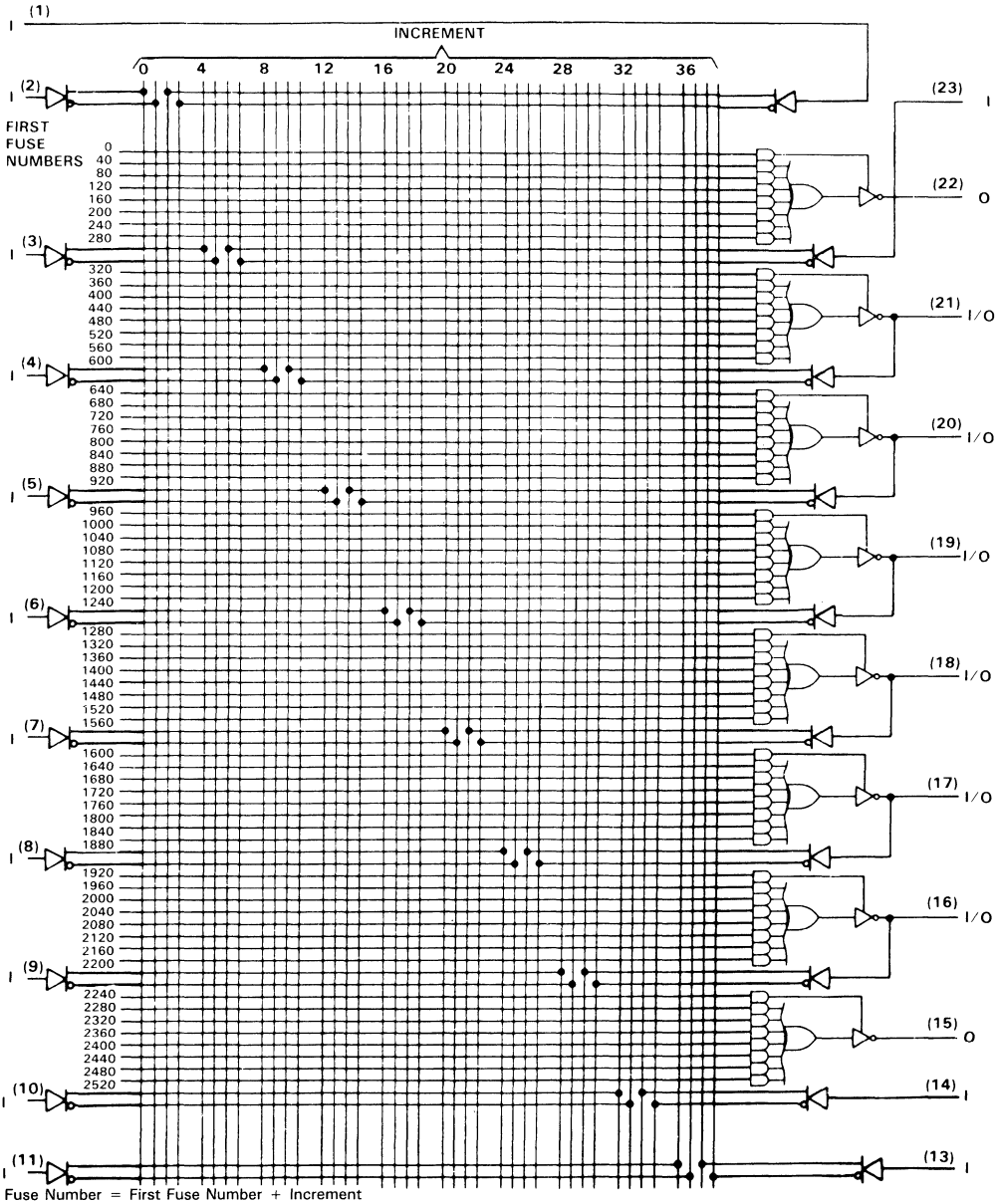
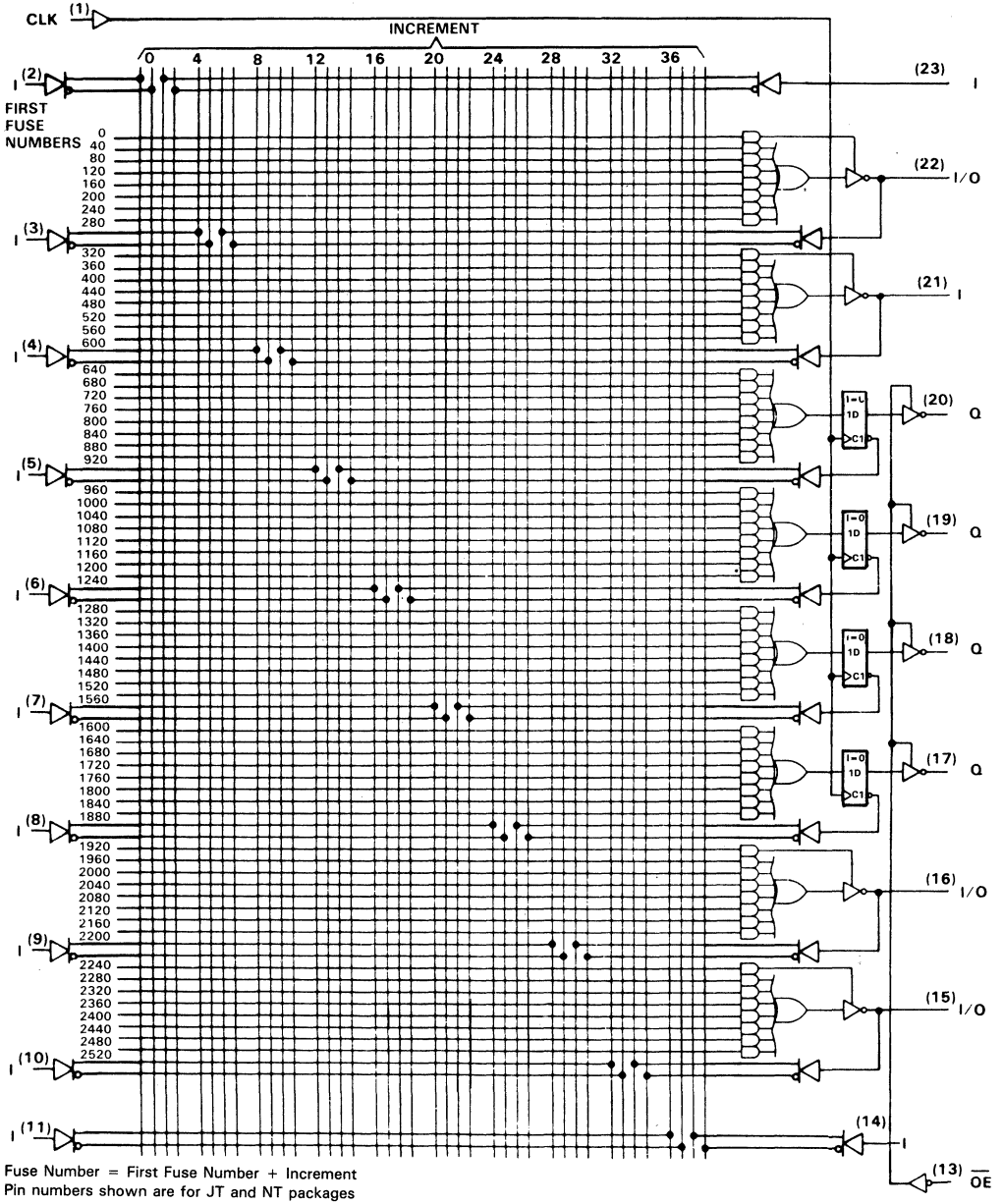
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages

TEXAS INSTRUMENTS
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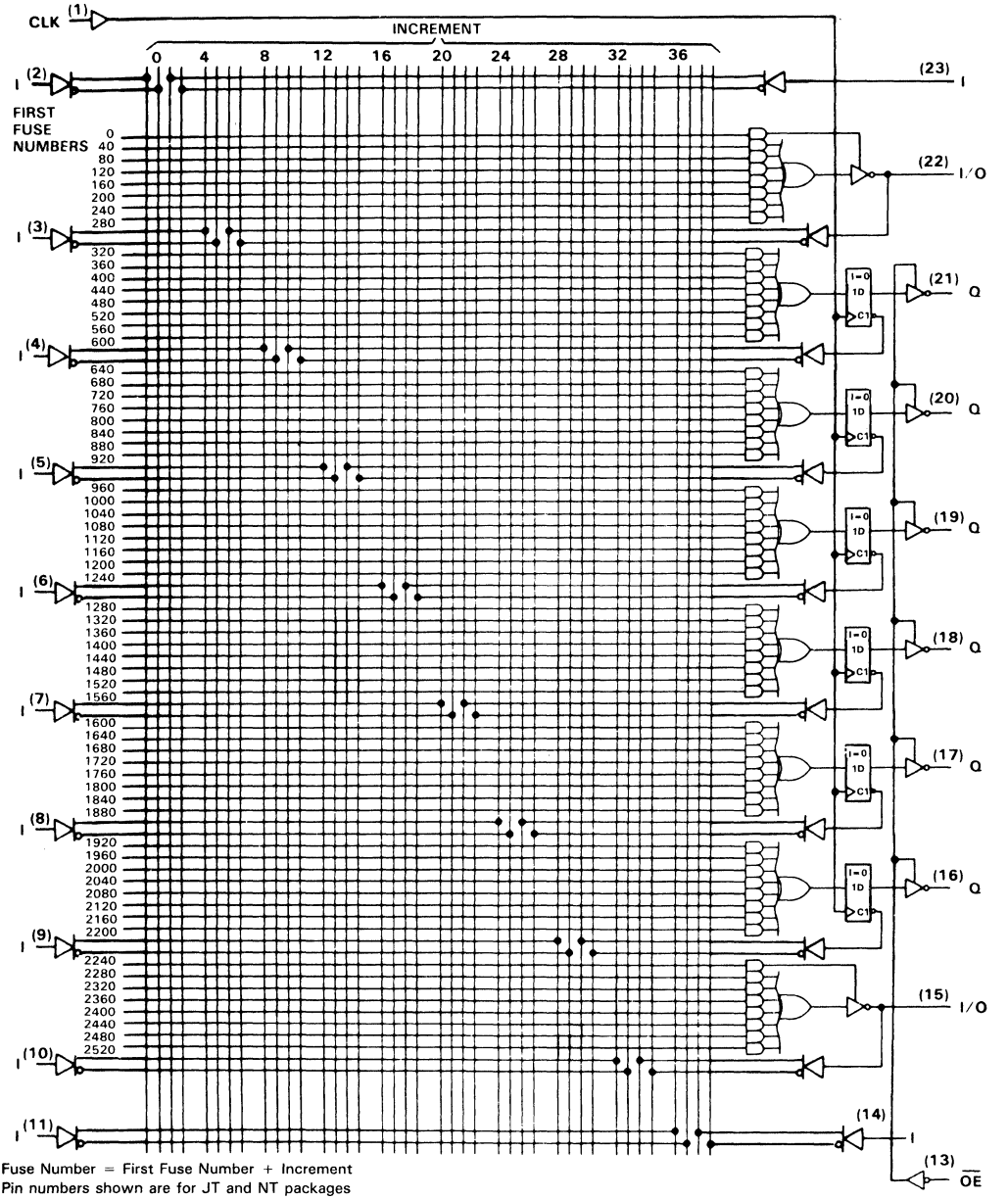
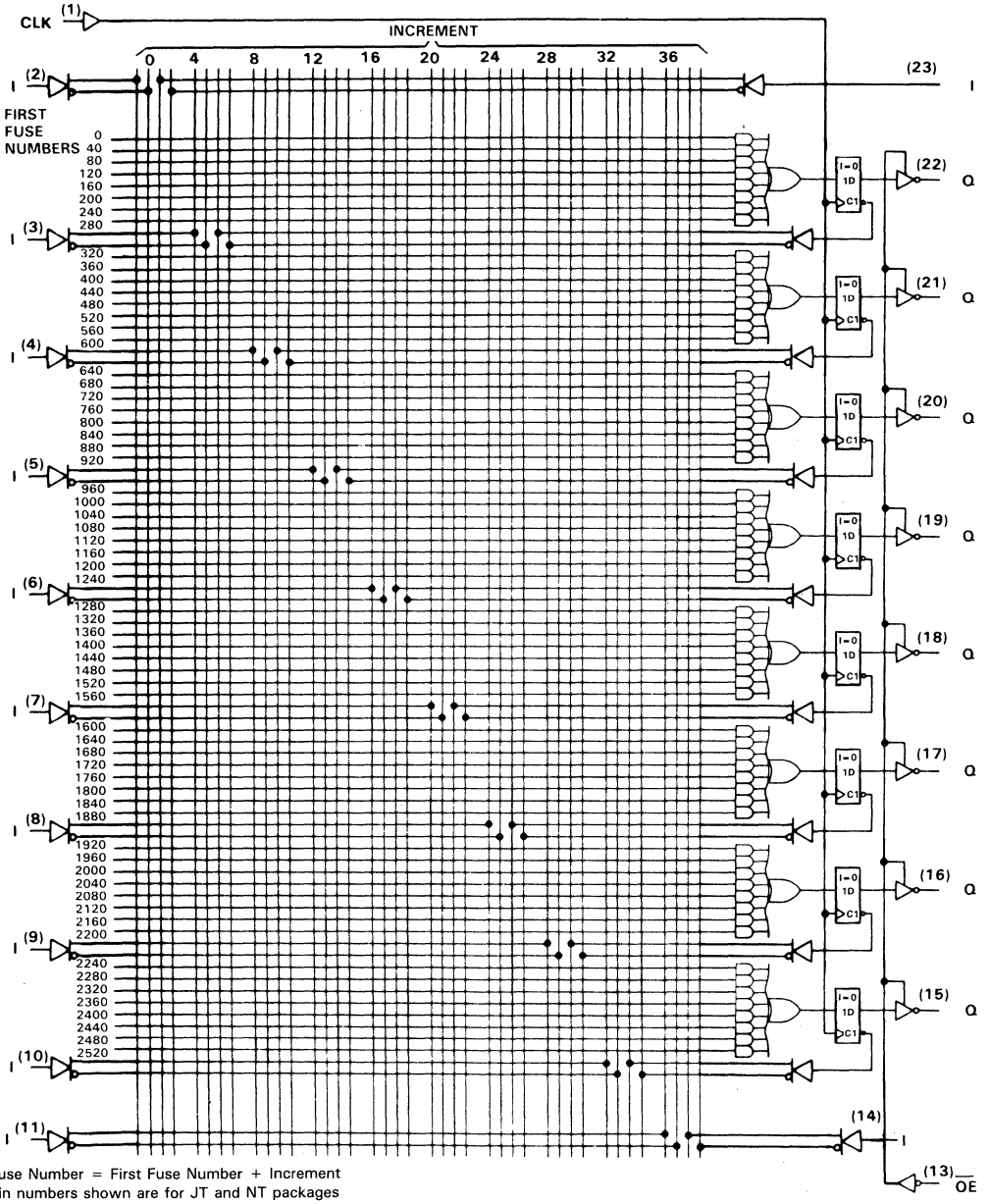
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		62.5	MHz
t_w	Pulse duration, clock	High	9			ns
		Low	9			ns
t_{su}	Setup time, input or feedback before CLK↑		12			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

PRODUCT PREVIEW

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.5	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			100	μA
I_{OZL}	O, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
	I/O ports					−0.25	mA
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V			100	μA
	All others					25	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.25	mA
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.5 V, Outputs open,	V_I = 0, $\overline{OE}$ at V_{IH}			210	mA
C_i		f = 1 MHz,	V_I = 2 V		7		pF
C_o		f = 1 MHz,	V_O = 2 V		8		pF
C_{clk}		f = 1 MHz,	V_{CLK} = 2 V		12		pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§	without feedback			62.5			MHz
	with internal feedback (counter configuration)			52.6			
	with external feedback			48			
t_{pd}	I, I/O	O, I/O	R = 390 Ω, R = 750 Ω, See Figure 1	3	8	12	ns
t_{pd}	CLK↑	Q		2	5	10	ns
t_{en}	$\overline{OE}$	Q		3	8	10	ns
t_{dis}	$\overline{OE}$↑	Q		2	8	10	ns
t_{en}	I, I/O	O, I/O		3	8	12	ns
t_{dis}	I, I/O	O, I/O		2	8	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed 1 second. Set V_O at 0.5 V to avoid test equipment ground degradation.
§ See f_{max} SPECIFICATIONS. f_{max} does not apply for TIBPAL20L8'.

PRODUCT PREVIEW

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		71.4	MHz
t_w	Pulse duration, clock	High	7			ns
		Low	7			ns
t_{su}	Setup time, input or feedback before CLK↑		10			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4			V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
	I/O ports				100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
	I/O ports				−100	
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.2	mA
I_{IH}‡		V_{CC} = 5.25 V, V_I = 2.7 V			25	μA
I_{IL}‡		V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0.5 V	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open, V_I = 0, $\overline{OE}$ at V_{IH}			210	mA
C_i		f = 1 MHz, V_I = 2 V		7		pF
C_o		f = 1 MHz, V_O = 2 V		8		pF
C_{clk}		f = 1 MHz, V_{CLK} = 2 V		12		pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}¶	without feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 1	71.4			MHz
	with internal feedback (counter configuration)			58.8			
	with external feedback			55.5			
t_{pd}	I, I/O	O, I/O		3	8	10	ns
t_{pd}	CLK↑	Q		2	5	8	ns
t_{pd}#	CLK↑	feedback				7	ns
t_{en}	$\overline{OE}$↓	Q		2	6	10	ns
t_{dis}	$\overline{OE}$↑	Q		2	6	10	ns
t_{en}	I, I/O	O, I/O		3	8	10	ns
t_{dis}	I, I/O	O, I/O		2	8	10	ns
t_{skew}	Skew between registered outputs				0.5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed 1 second.
¶ See f_{max} SPECIFICATIONS. f_{max} does not apply for TIBPAL20L8'.
# This parameter applies to TIBPAL20R4' and TIBPAL20R6' only (see Figure 2 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS
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programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

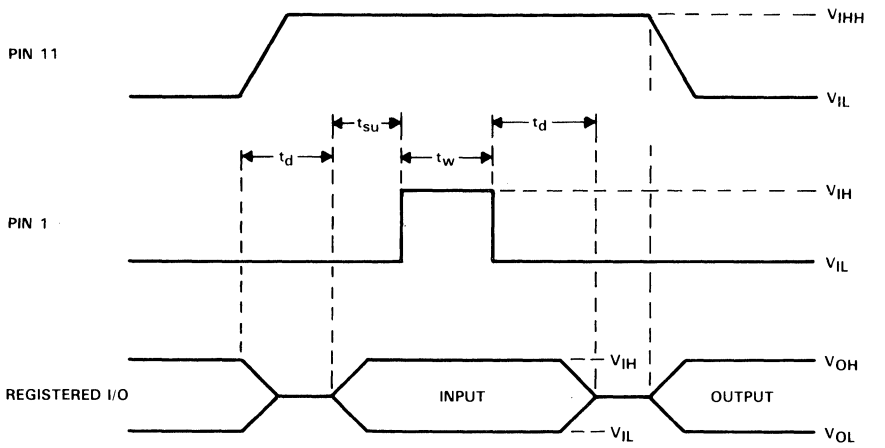
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 3)



NOTE 3: $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 1

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su} + t_h$). However, the minimum f_{max} is determined by the minimum clock period ($t_w$high + $t_w$low).

Thus, f_{max} without feedback $= \dfrac{1}{(t_w \text{ high} + t_w \text{ low})}$ or $\dfrac{1}{(t_{su} + t_h)}$.

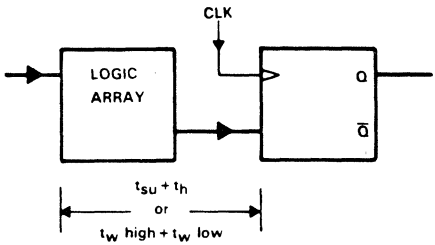


FIGURE 1. f_{max} WITHOUT FEEDBACK

f_{max} with internal feedback, see Figure 2

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus, f_{max} with internal feedback $= \dfrac{1}{(t_{su} + t_{pd} \text{ CLK-to-FB})}$.

Where t_{pd} CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

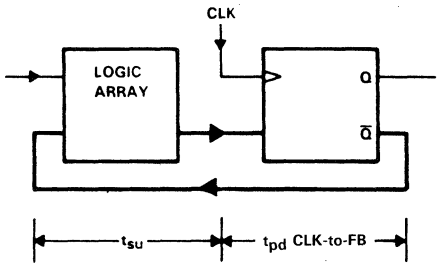


FIGURE 2. f_{max} WITH INTERNAL FEEDBACK

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f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 3

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input and setup time for the external signals ($t_{su} + t_{pd}$ CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd} \text{ CLK-to-Q})}$.

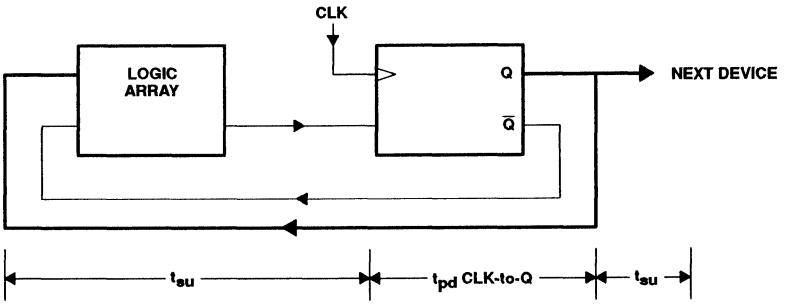


FIGURE 3. f_{max} WITH EXTERNAL FEEDBACK

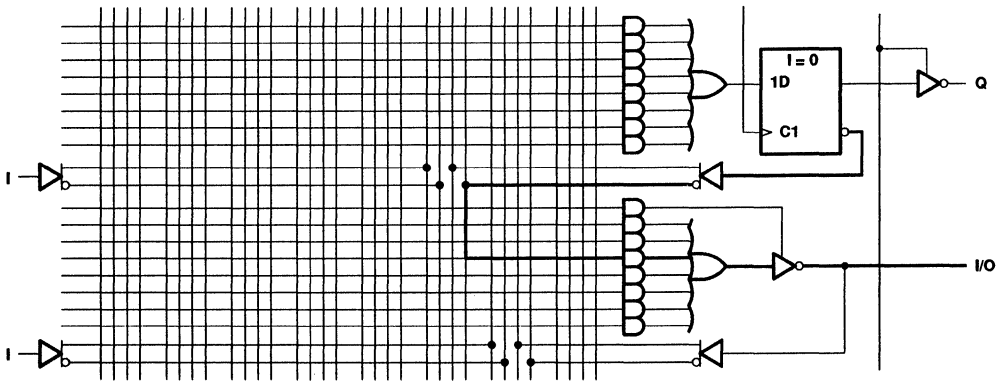
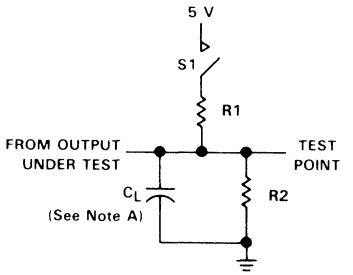
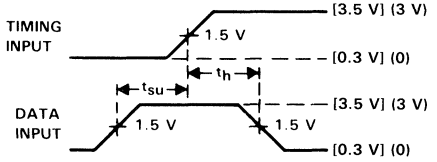


FIGURE 4. PROPAGATION DELAY FROM CLK↑ to I/O, THRU LOGIC ARRAY

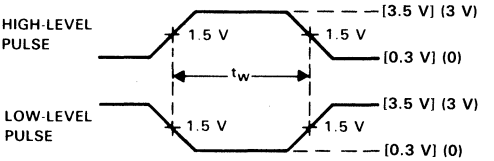
PARAMETER MEASUREMENT INFORMATION



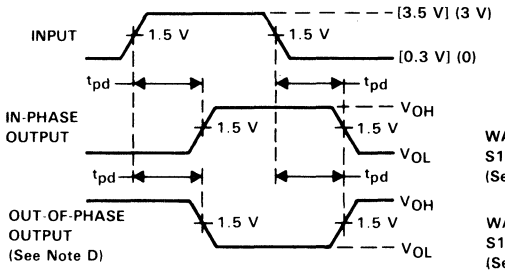
LOAD CIRCUIT FOR THREE-STATE DEVICES



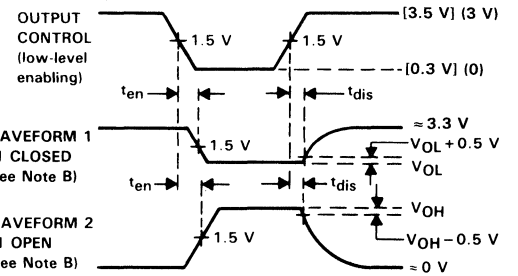
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in parentheses ( ). For C suffix, use the voltage levels indicated in brackets [ ].
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 5

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

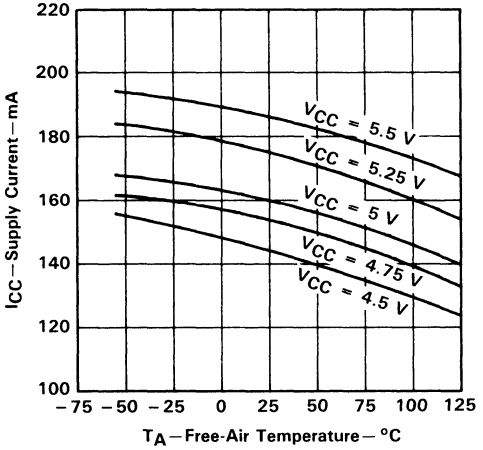

FIGURE 6

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

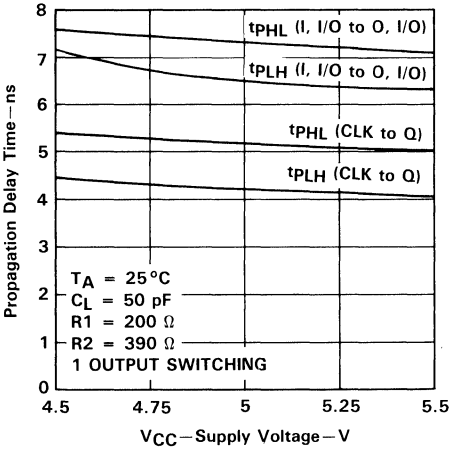

FIGURE 7

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

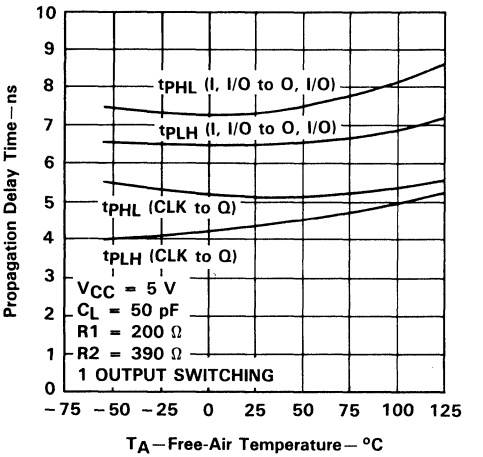

FIGURE 8

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

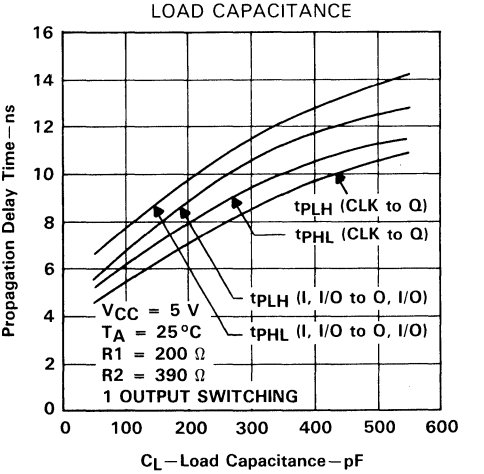

FIGURE 9

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
FREQUENCY
8-BIT COUNTER MODE

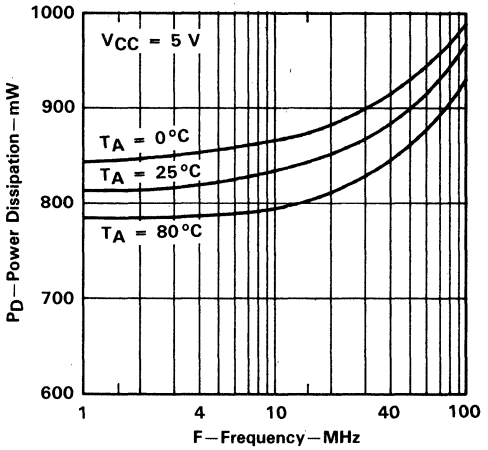

FIGURE 10

SKEW BETWEEN OUTPUTS†
vs
NUMBER OF OUTPUTS SWITCHING

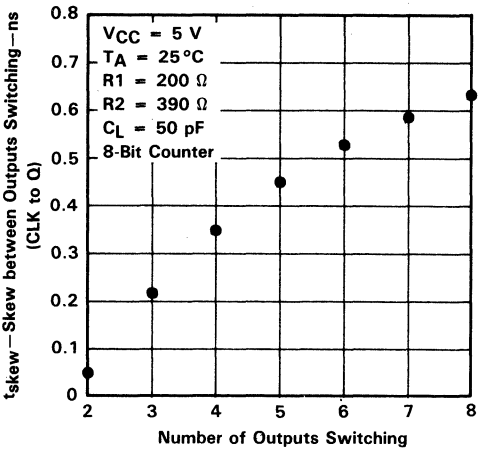

FIGURE 11

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

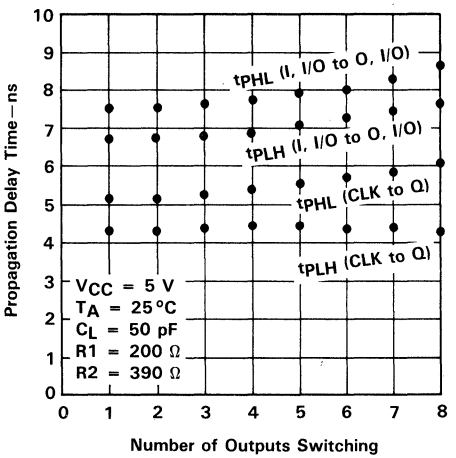

FIGURE 12

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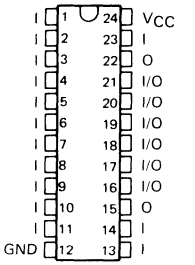
TIBPAL20L8-20M, TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M
TIBPAL20L8-15C, TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C
HIGH PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

D2920, JUNE 1986—REVISED AUGUST 1989

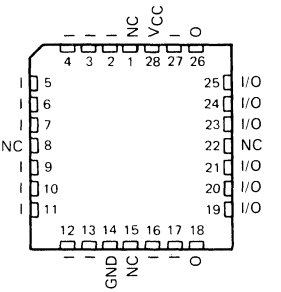
- **High Performance: f_{max} (w/o feedback)**
  TIBPAL20R' C series . . . 45 MHz
  TIBPAL20R' M series . . . 41.6 MHz
- **High Performance . . . 45 MHz Min**
- **Functionally Equivalent to, but Faster than, PAL20L8, PAL20R4, PAL20R6, PAL20R8**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Preload Capability on Output Registers Simplifies Testing**
- **Package Options Include Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Reduced I_{CC} of 180 mA Max**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8	14	2	0	6
'PAL20R4	12	0	4 (3-state buffers)	4
'PAL20R6	12	0	6 (3-state buffers)	2
'PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
M SUFFIX . . . JT OR W PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are also available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20'M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL20'C is characterized from 0°C to 75°C.

IMPACT is a trademark of Texas Instruments Incorporated
PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

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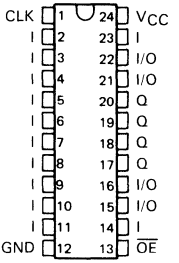
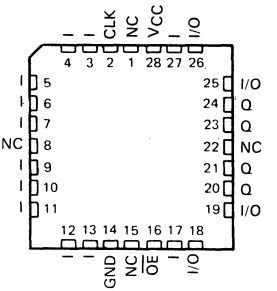
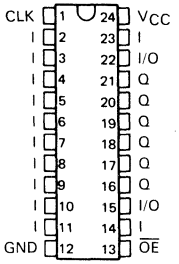
TIBPAL20R4'
M SUFFIX . . . JT OR W PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R6'
M SUFFIX . . . JT OR W PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R6'
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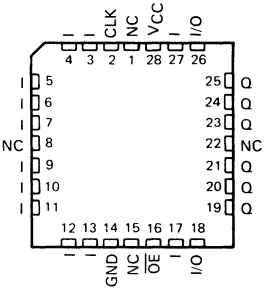
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R8'
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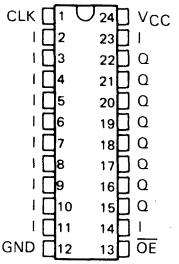
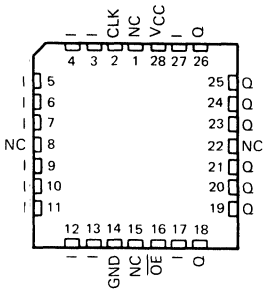
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

NC—No internal connection

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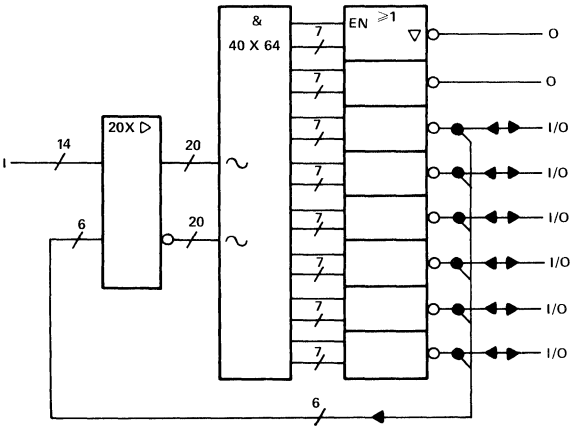
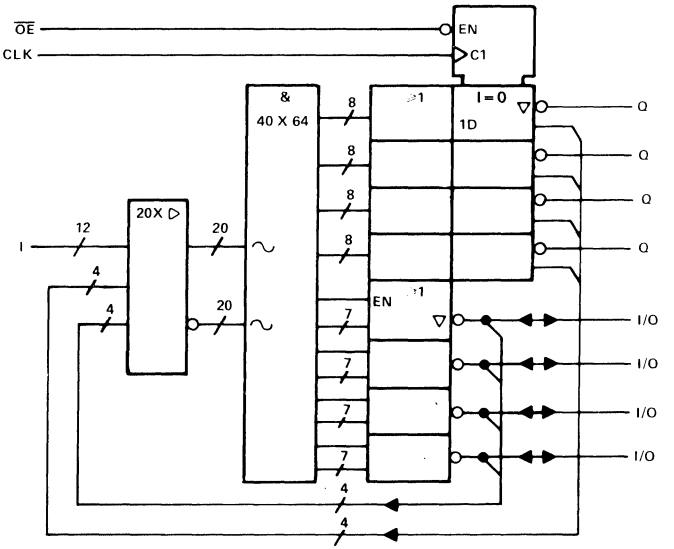
functional block diagrams (positive logic)

TIBPAL20L8'



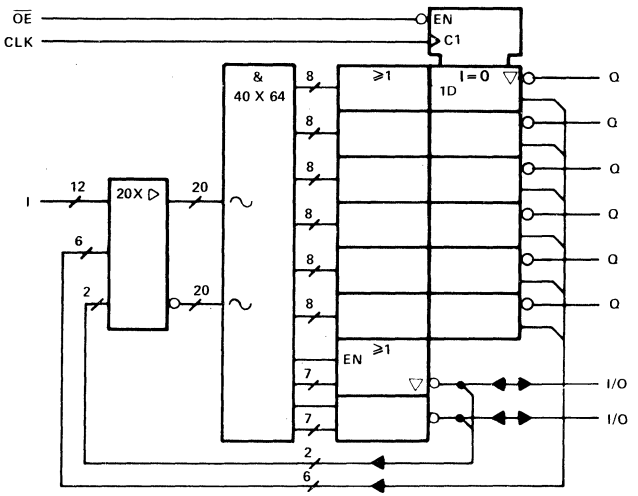
TIBPAL20R4'



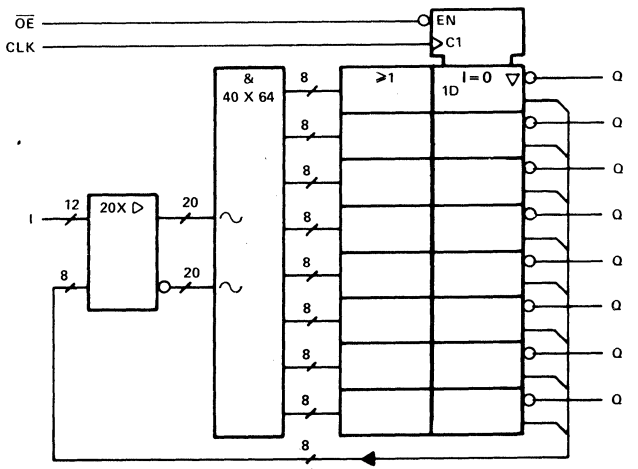
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'



TIBPAL20R8'



∿ denotes fused inputs

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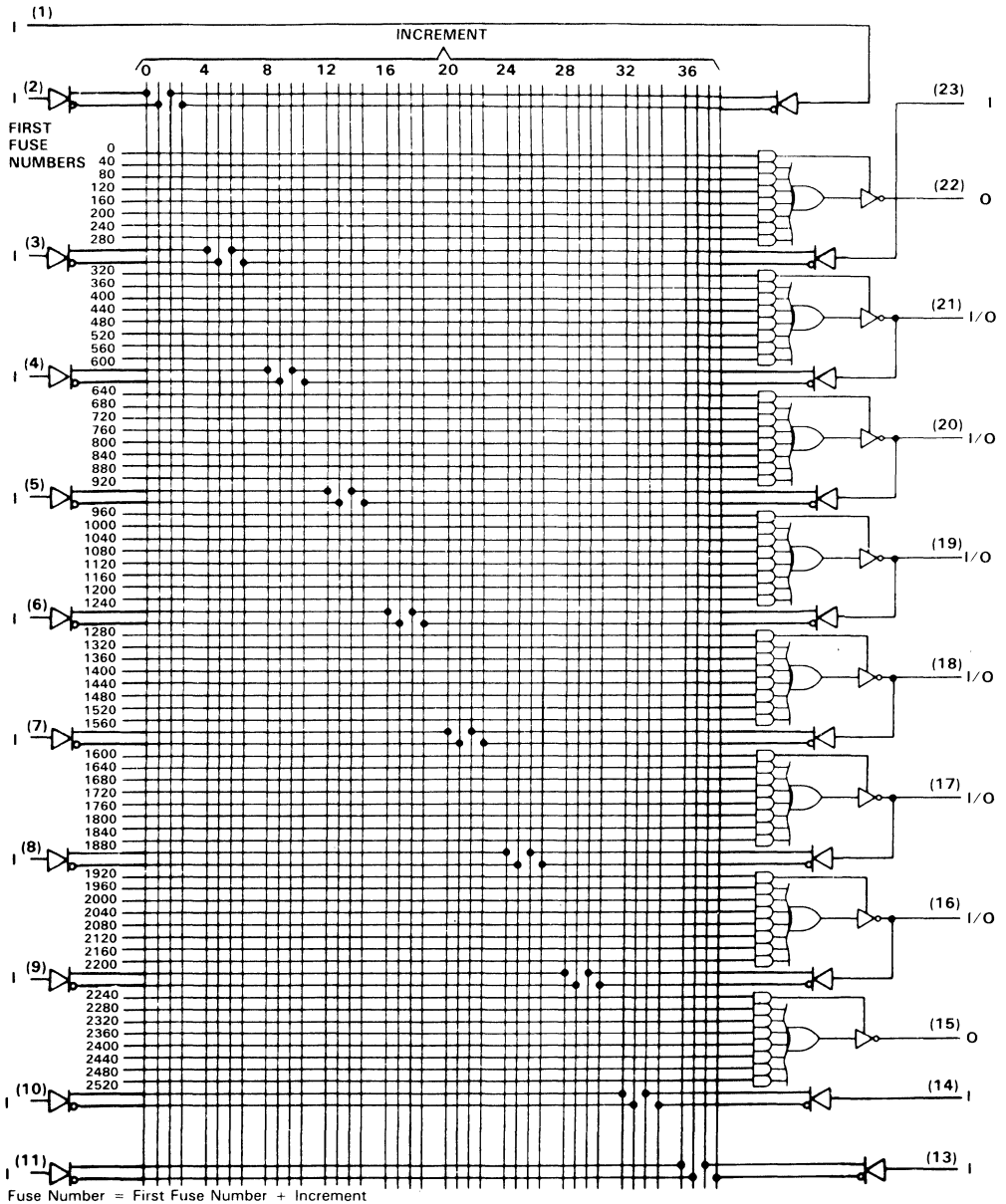
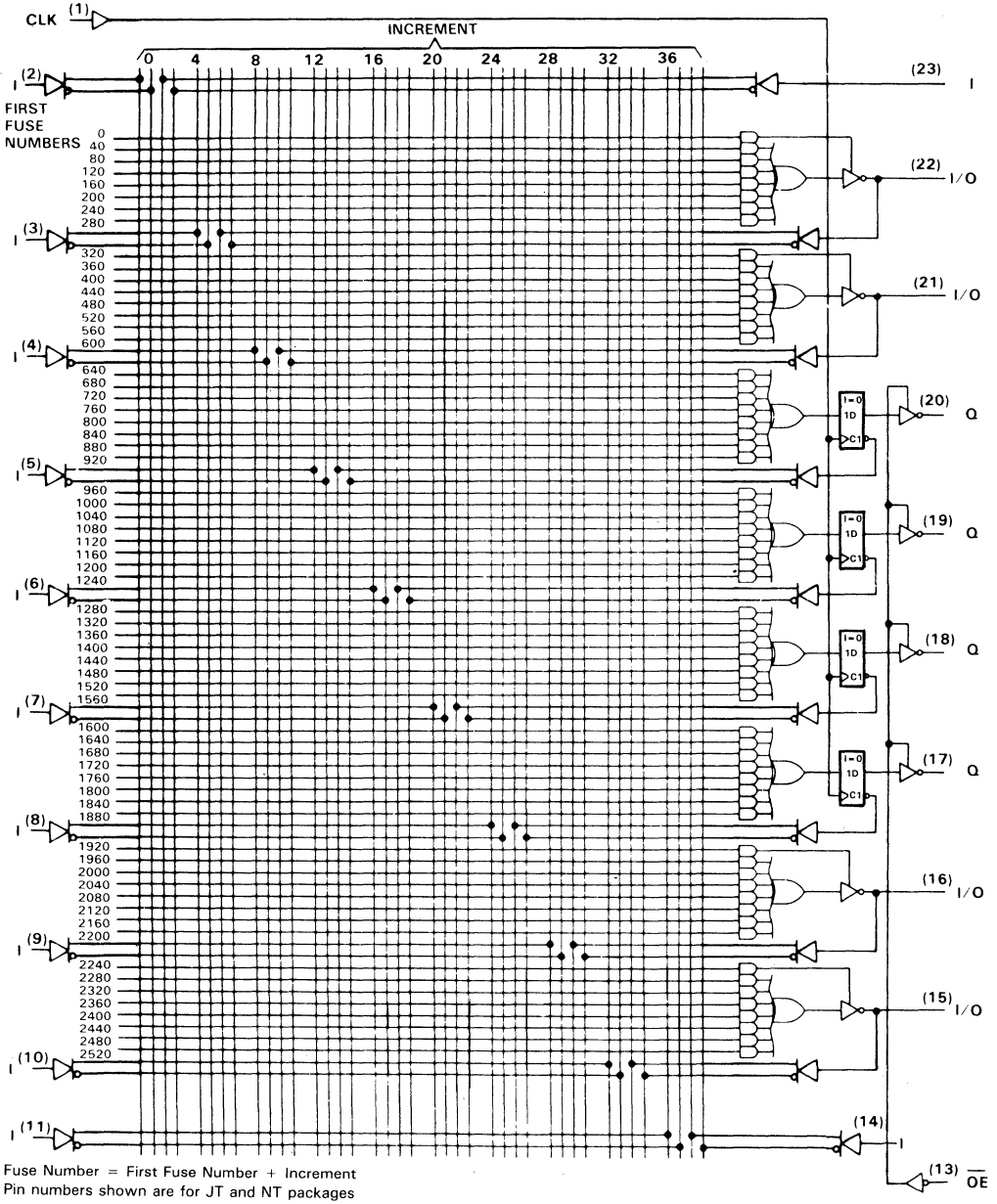
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages

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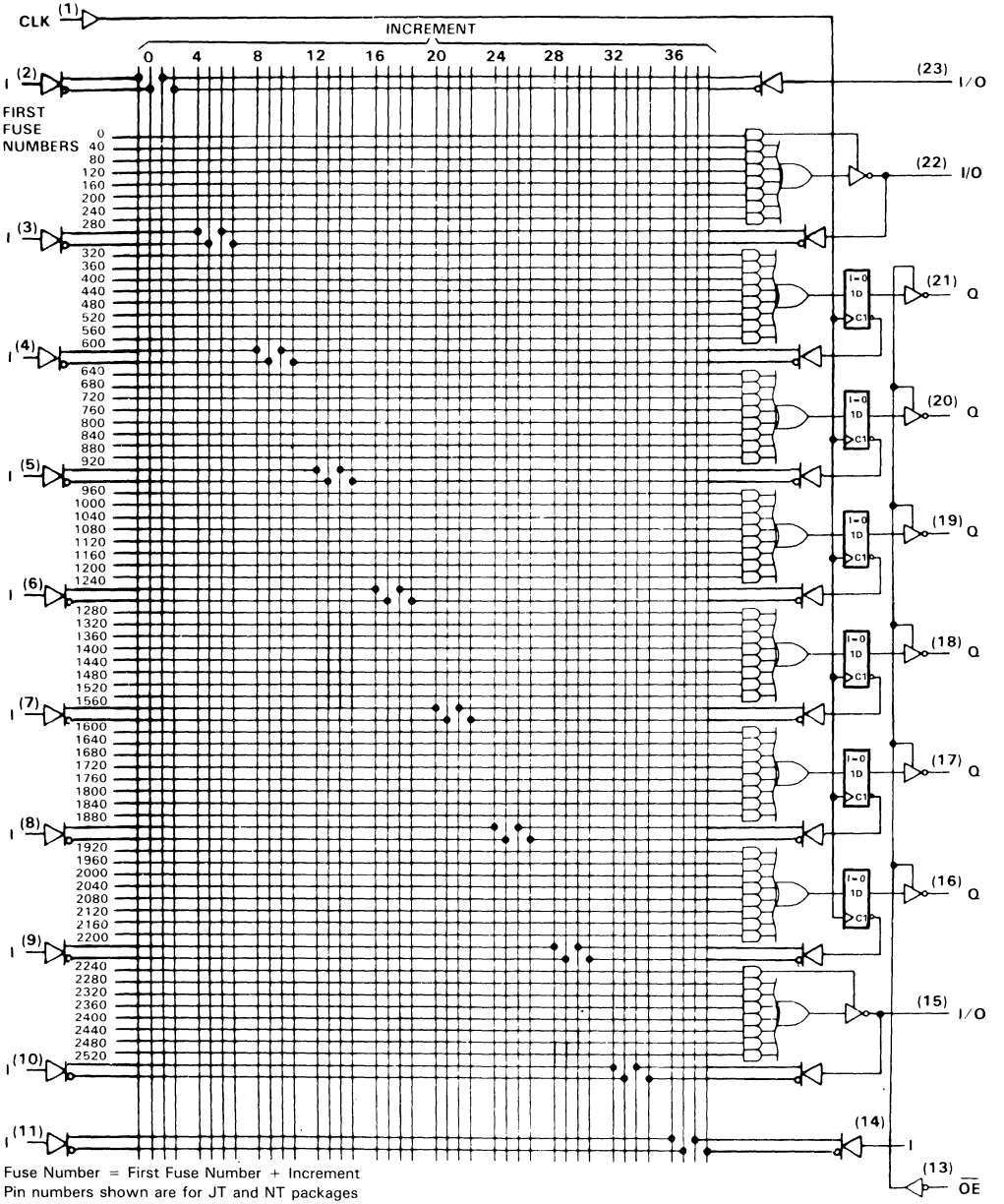
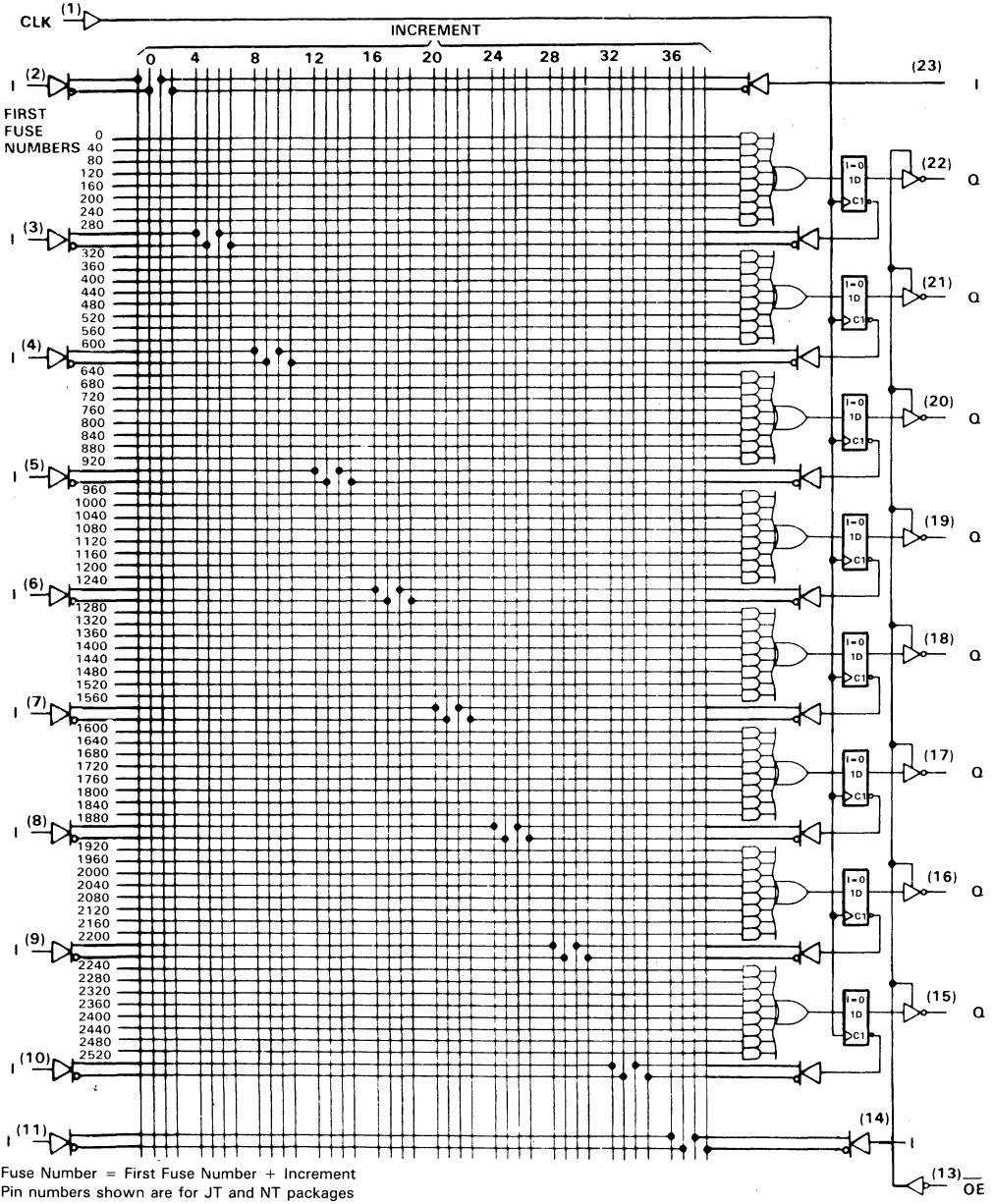
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JT and NT packages

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			−20M			−15C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		41.6	0		45	MHz
t_w	Pulse duration, clock	High	12			10			ns
		Low	12			12			ns
t_{su}	Setup time, input or feedback before CLK↑		20	10		15	10		ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA	2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA		0.25	0.5	V
I_{OZH}		V_{CC} = 5.5 V, V_O = 2.7 V			100	μA
I_{OZL}	O, Q outputs	V_{CC} = 5.5 V, V_O = 0.4 V			−20	μA
	I/O ports				−0.25	mA
I_I		V_{CC} = 5.5 V, V_I = 5.5 V			1	mA
I_{IH}‡	I/O ports	V_{CC} = 5.5 V, V_I = 2.7 V			100	μA
	All others				25	
I_{IL}‡		V_{CC} = 5.5 V, V_I = 0.4 V			−0.25	mA
I_{OS}§		V_{CC} = 5.5 V, V_O = 0.5 V	−30	−70	−250	mA
I_{CC}		V_{CC} = 5.5 V, V_I = 0, Outputs open, $\overline{OE}$ at V_{IH}		120	180	mA

† All typical values are V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}¶	with feedback		R_1 = 390 Ω, R2 = 750 Ω, See Figure 1	28.5	40		MHz
	without feedback			41.6	50		
t_{pd}	I, I/O	O, I/O			12	20	ns
t_{pd}	CLK↑	Q			8	15	ns
t_{en}	$\overline{OE}$	Q			10	20	ns
t_{dis}	$\overline{OE}$↑	Q			8	20	ns
t_{en}	I, I/O	O, I/O			12	25	ns
t_{dis}	I, I/O	O, I/O			12	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, f_{max} (without feedback) = $\frac{1}{t_w\text{ high} + t_w\text{ low}}$

f_{max} does not apply for TIBPAL20L8'

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electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4			V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
	I/O ports				100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
	I/O ports				−0.25	mA
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V, V_I = 2.7 V			25	μA
I_{IL}‡		V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0.5 V	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, V_I = 0, Outputs open, $\overline{OE}$ at V_{IH}		120	180	mA

† All typical values are V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}¶	with feedback		R_1 = 200 Ω, R2 = 390 Ω, See Figure 1	37	40		MHz
	without feedback			45	50		
t_{pd}	I, I/O	O, I/O			12	15	ns
t_{pd}	CLK↑	Q			8	12	ns
t_{en}	$\overline{OE}$	Q			10	15	ns
t_{dis}	$\overline{OE}$↑	Q			8	12	ns
t_{en}	I, I/O	O, I/O			12	18	ns
t_{dis}	I, I/O	O, I/O			12	15	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ f_{max} (with feedback) = $\dfrac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, f_{max} (without feedback) = $\dfrac{1}{t_w\text{ high} + t_w\text{ low}}$

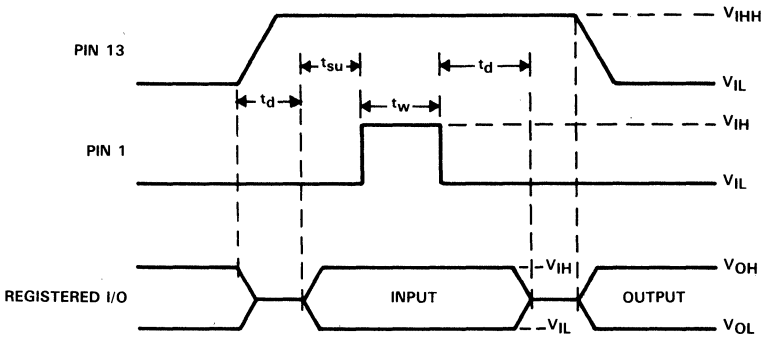
f_{max} does not apply for TIBPAL20L8'

preload procedure for registered outputs (see Note 2)

The output registers of the TIBPAL20R' can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Notes 2 and 3)



NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

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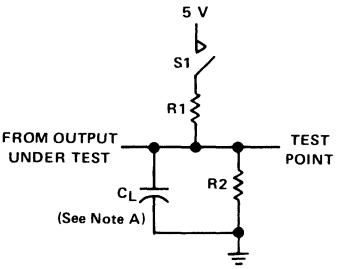
programming information

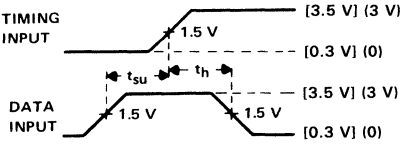
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

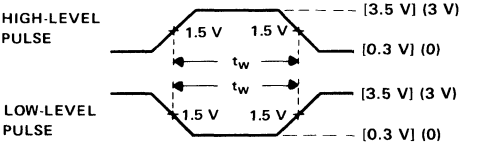
PARAMETER MEASUREMENT INFORMATION



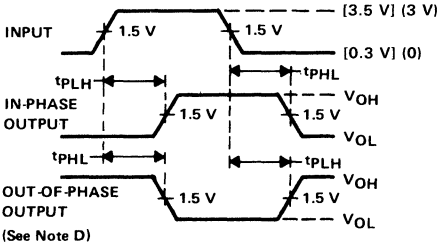
LOAD CIRCUIT FOR 3-STATE OUTPUTS



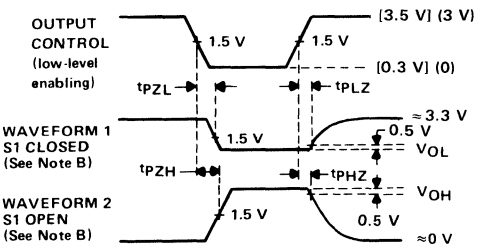
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For M suffix, use voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 1

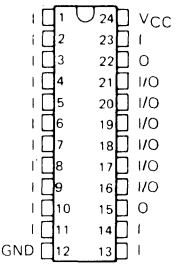
TIBPAL20L8-25C, TIBPAL20R4-25C, TIBPAL20R6-25C, TIBPAL20R8-25C
LOW-POWER HIGH PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

D2920, MAY 1987—REVISED AUGUST 1989

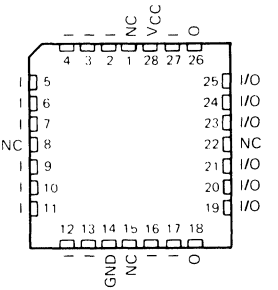
- **Low-Power, High Performance**
  Reduced I_{CC} of 105 mA Max
  f_{max}:
  Without Feedback . . . 33 MHz Min
  With Feedback . . . 25 MHz Min
  t_{pd} . . . 25 ns Max
- **Direct Replacement for PAL20L8A, PAL20R4A, PAL20R6A, and PAL20R8A with at Least 50% Reduction in Power**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Registered Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8	14	2	0	6
'PAL20R4	12	0	4 (3-state buffers)	4
'PAL20R6	12	0	6 (3-state buffers)	2
'PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are also available for further reduction in board space.

In many cases, these low-power devices are fast enough to be used where the high-speed or "A" devices are used. From an overall system level, this can amount to a significant reduction in power consumption, with no sacrifice in speed.

All of the output registers are set to a low level during power-up, but the voltage levels at the output pins stay high. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20'C series is characterized from 0°C to 75°C.

IMPACT is a trademark of Texas Instruments Incorporated
PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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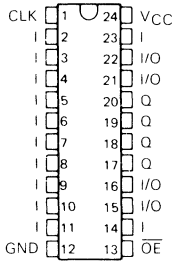
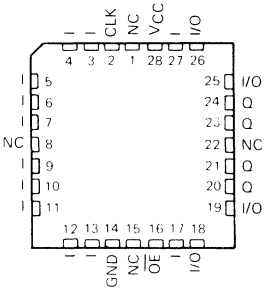
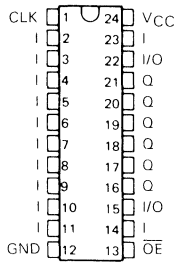
TIBPAL20R4'
JT OR NT PACKAGE
(TOP VIEW)



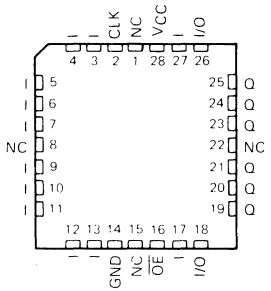
TIBPAL20R4'
FN PACKAGE
(TOP VIEW)



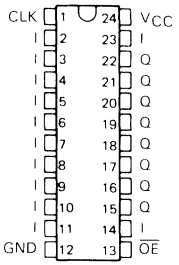
TIBPAL20R6'
JT OR NT PACKAGE
(TOP VIEW)



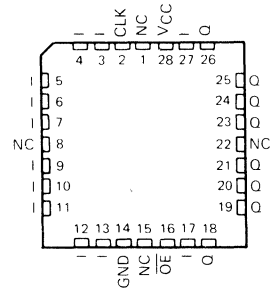
TIBPAL20R6'
FN PACKAGE
(TOP VIEW)



TIBPAL20R8'
JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R8'
FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

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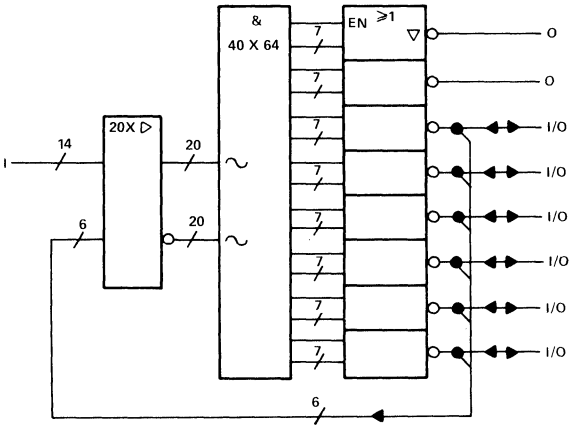
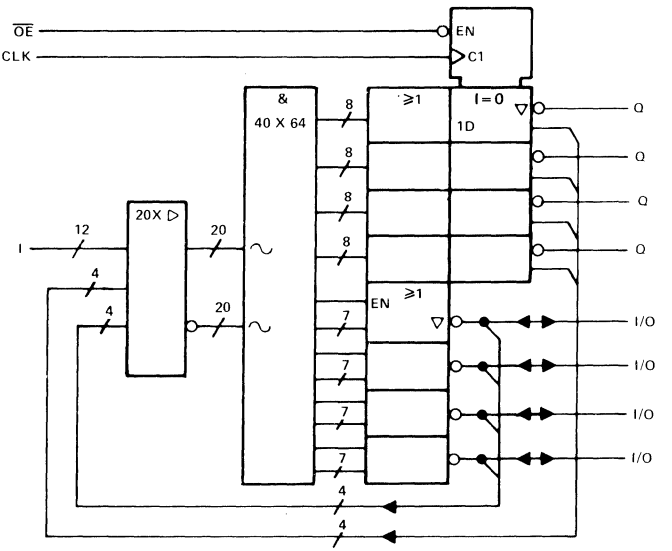
functional block diagrams (positive logic)

TIBPAL20L8'



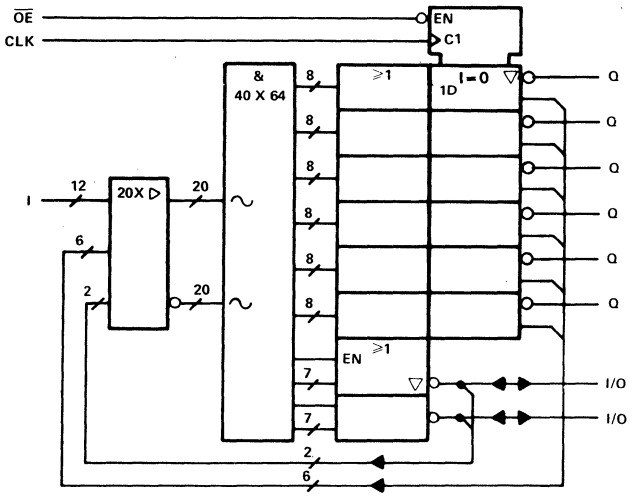
TIBPAL20R4'



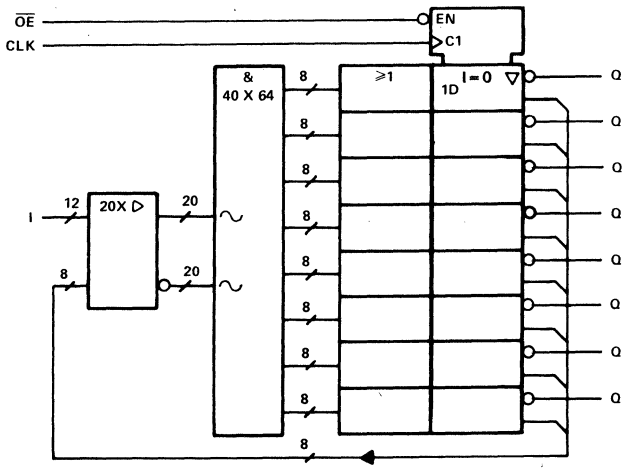
∼ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'



TIBPAL20R8'



∿ denotes fused inputs

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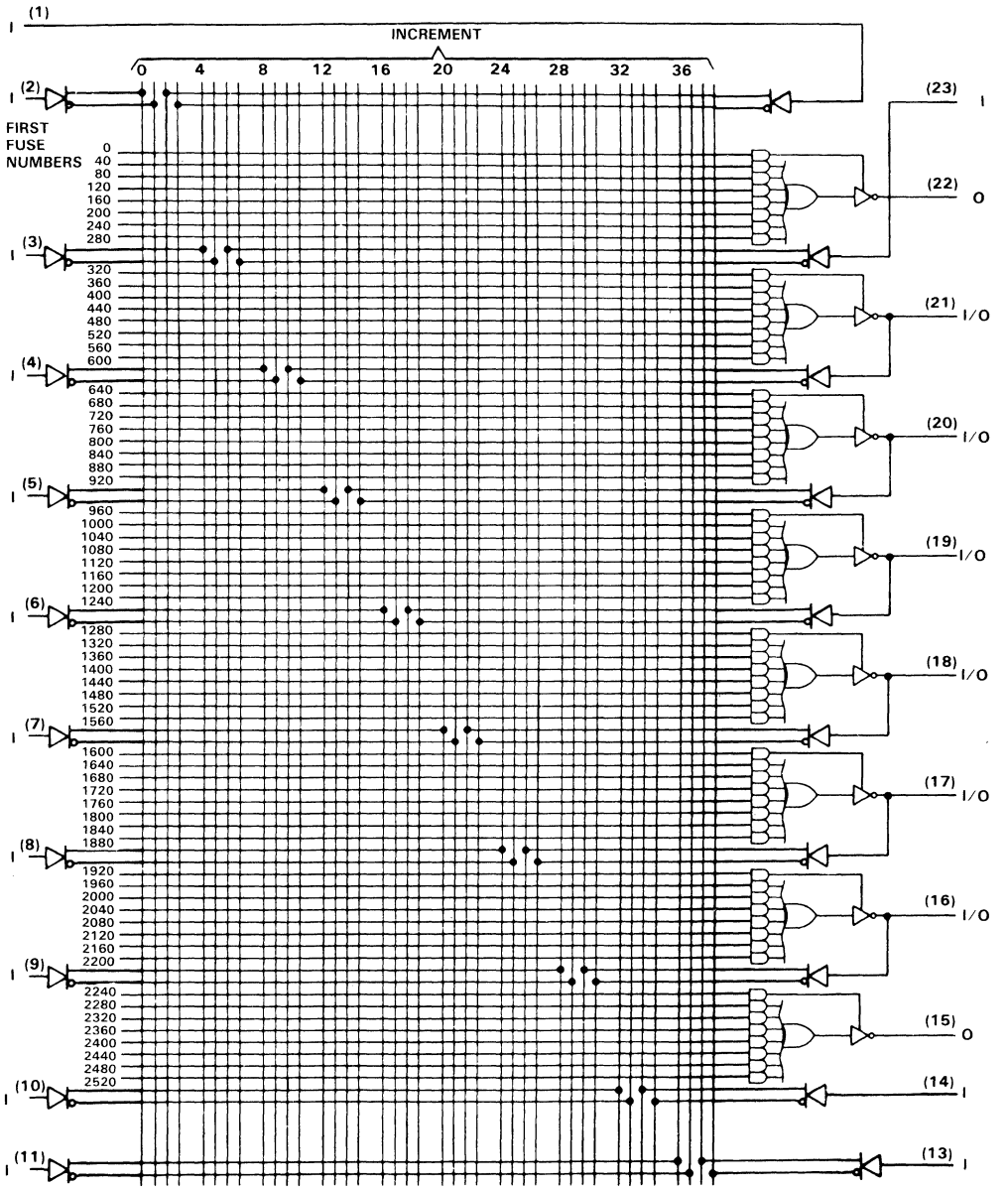
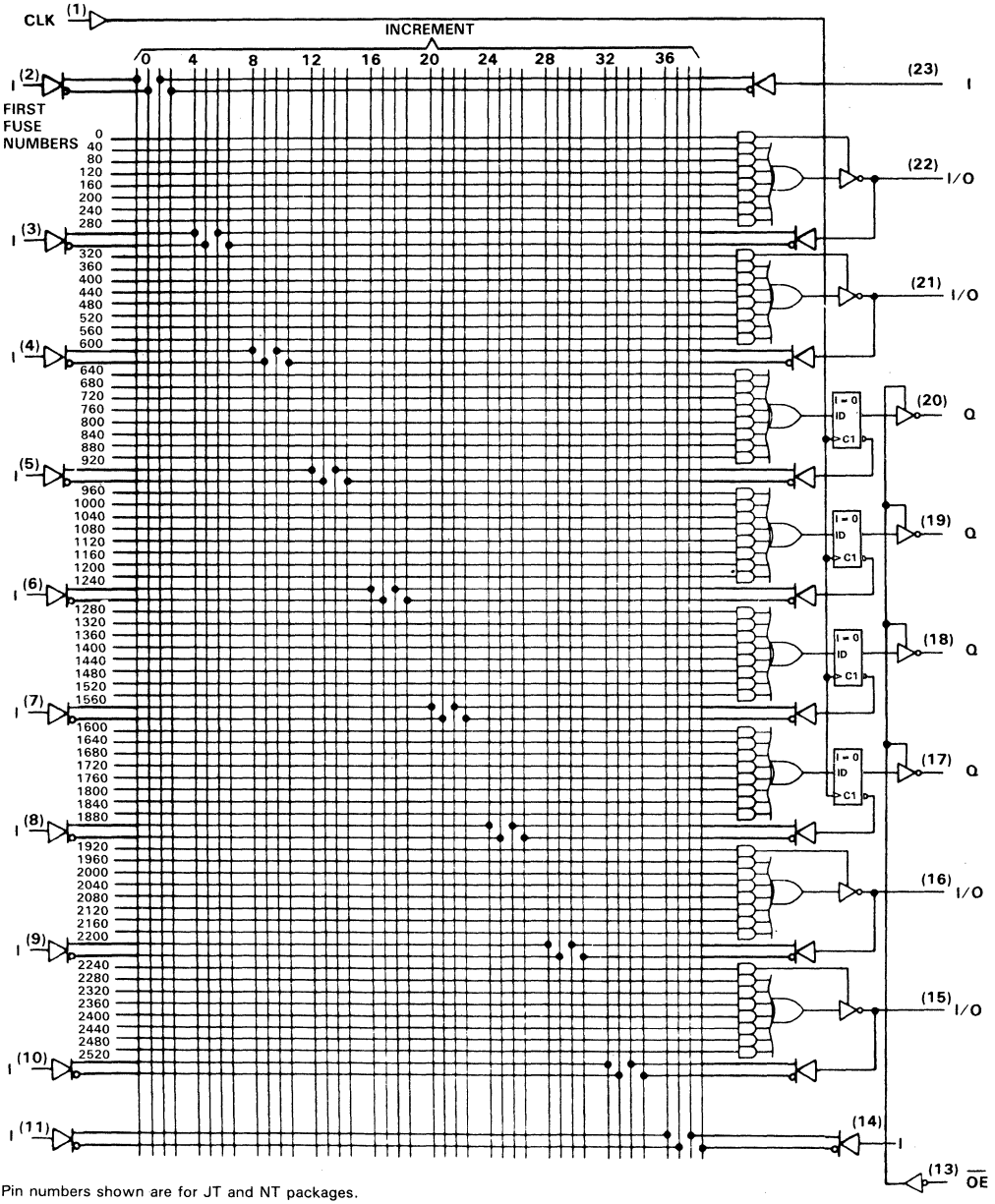
logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

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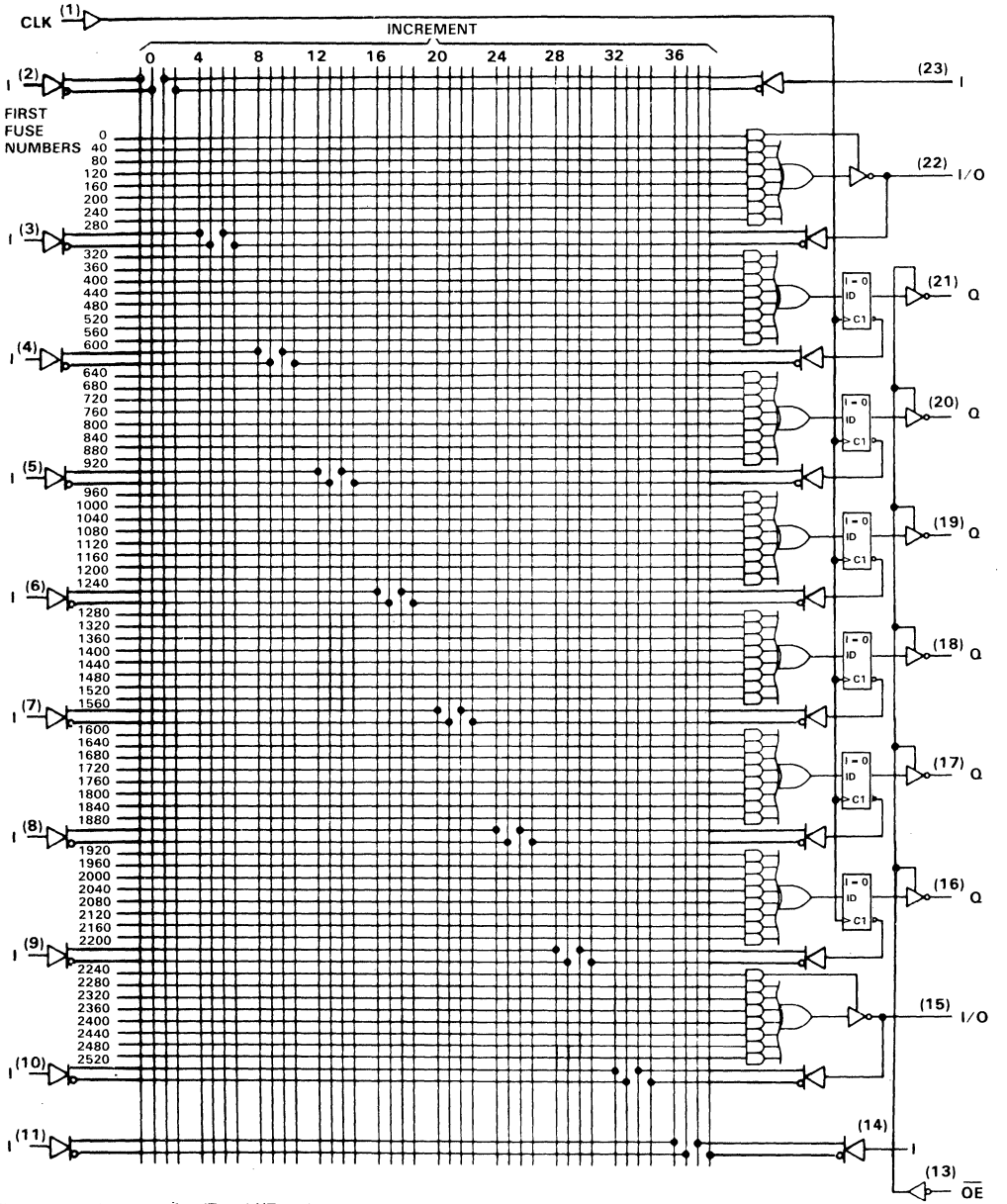
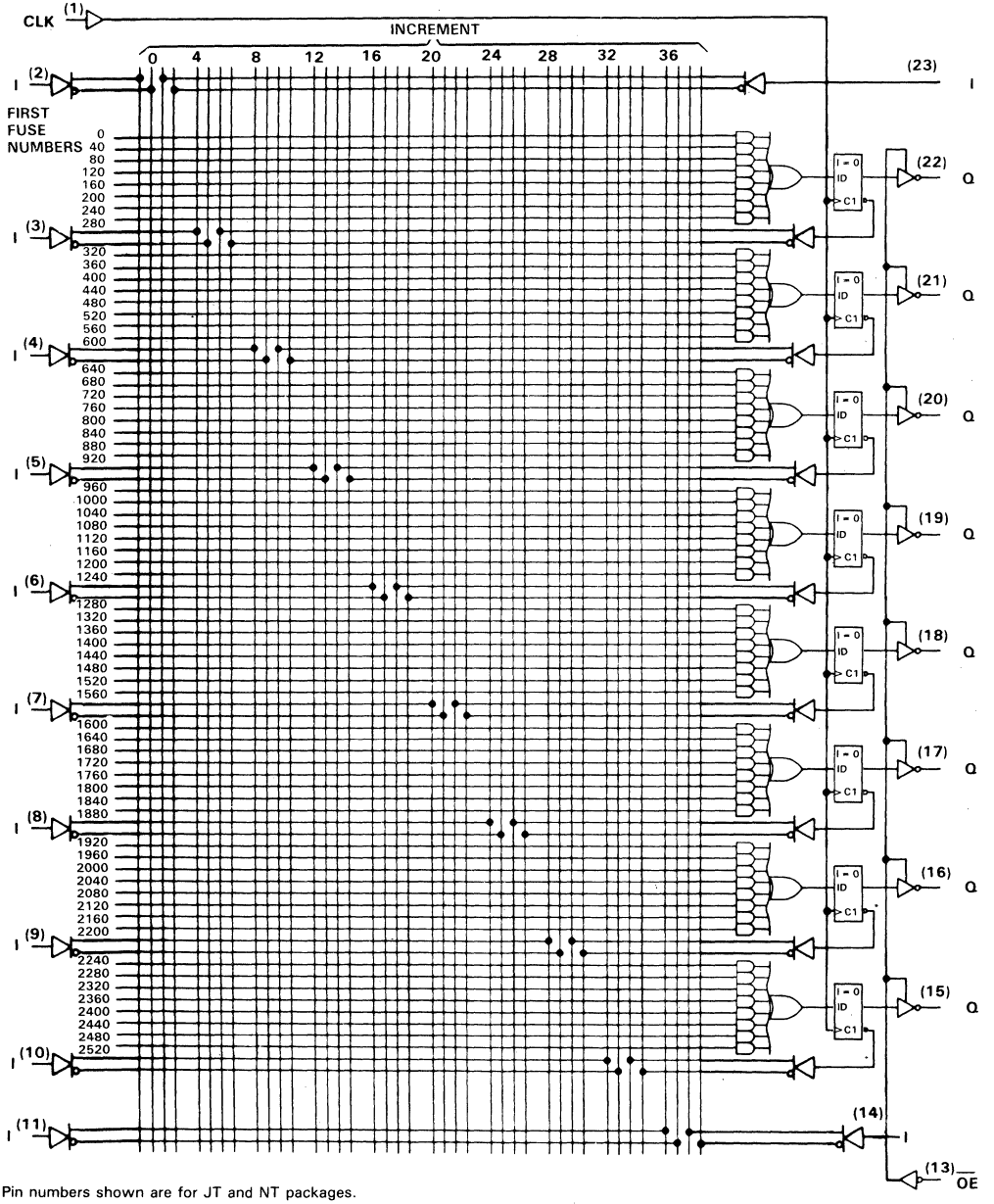
logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		33	MHz
t_w	Pulse duration, clock	High	15			ns
		Low	15			ns
t_{su}	Setup time, input or feedback before CLK↑		25			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0		75	°C

f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
	I/O ports				100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
	I/O ports				−0.25	mA
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
I_{IL}‡		V_{CC} = 5.25 V, V_I = 0.4 V			−0.2	mA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, V_I = 0, Outputs open, $\overline{OE}$ at V_{IH}		75	105	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed 1 second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}¶	with feedback		R_1 = 200 Ω, R2 = 390 Ω, C_L = 50 pF, See Figure 1	25	40		MHz
	without feedback			33	50		
t_{pd}	I, I/O	O, I/O		3	14	25	ns
t_{pd}	CLK↑	Q		2	10	15	ns
t_{en}	$\overline{OE}$	Q		2	8	15	ns
t_{dis}	$\overline{OE}$↑	Q		2	8	15	ns
t_{en}	I, I/O	O, I/O		3	15	25	ns
t_{dis}	I, I/O	O, I/O		3	15	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, f_{max} (without feedback) = $\frac{1}{t_w\text{ high} + t_w\text{ low}}$

f_{max} does not apply for TIBPAL20L8'

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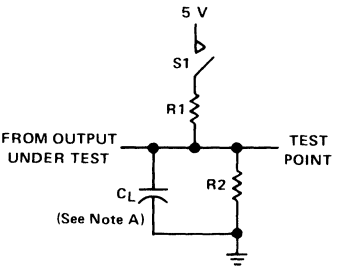
programming information

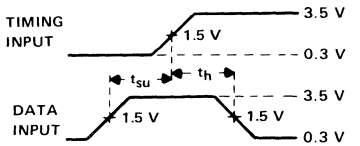
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

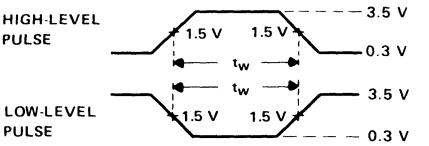
PARAMETER MEASUREMENT INFORMATION



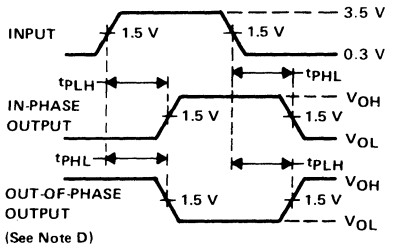
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



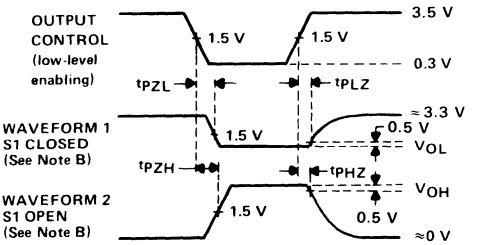
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

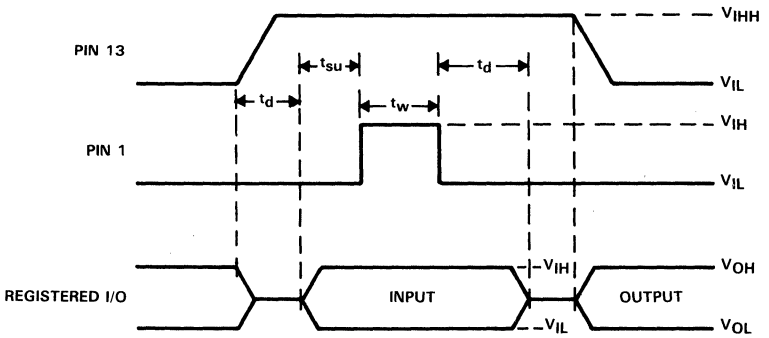
FIGURE 1

preload procedure for registered outputs (see Note 2)

The output registers of the TIBPAL20R' can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Notes 2 and 3)



NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

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TIBPAL20L8-15CNL, TIBPAL20R4-15CNL, TIBPAL20R6-15CNL, TIBPAL20R8-15CNL
TIBPAL20L8-25CNL, TIBPAL20R4-25CNL, TIBPAL20R6-25CNL, TIBPAL20R8-25CNL
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

D3095, JANUARY 1988—REVISED AUGUST 1989

- **High Performance: f_{max}(w/o feedback)**
  TIBPAL20R' -15 Series . . . 45 MHz
  TIBPAL20R' -25 Series . . . 33 MHz
- **-15CNL Devices are Direct Replacements for MMI PAL20L8BCNL, PAL20R4BCNL, PAL20R6BCNL, and PAL20R8BCNL**
- **-25CNL Devices are Direct Replacements for MMI PAL20L8B-2CNL, PAL20R4B-2CNL, PAL20R6B-2CNL, and PAL20R8B-2CNL**
- **Power-up Clear on Registered Devices (All Registered Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Preload Capability on Output Registers Simplifies Testing**

DEVICE	I INPUTS	3-STATE Q OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8	14	2	0	6
'PAL20R4	12	0	4 (3-state buffers)	4
'PAL20R6	12	0	6 (3-state buffers)	2
'PAL20R8	12	0	8 (3-state buffers)	0

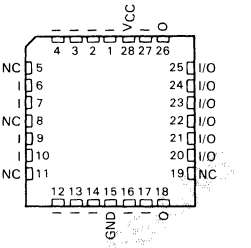
ordering information

Devices with the MMI chip-carrier pin-out shown here may be ordered by using the indicated part number with the NL suffix. Do not include the package suffix (FN).

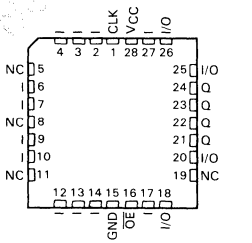
description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are also available for further reduction in board space.

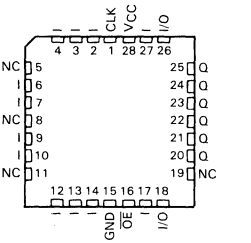
TIBPAL20L8' . . . FN PACKAGE
(TOP VIEW)



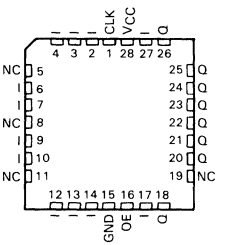
TIBPAL20R4' . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R6' . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R8' . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

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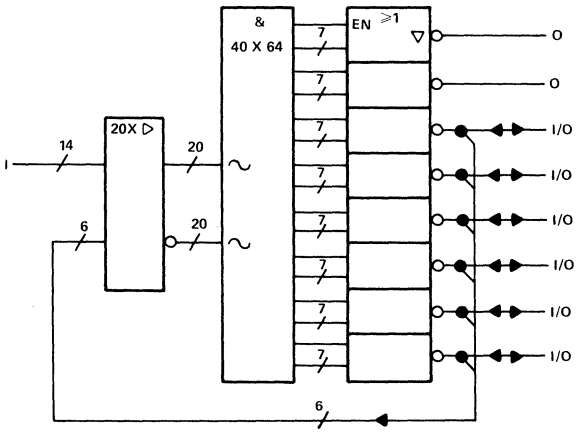
description (continued)

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

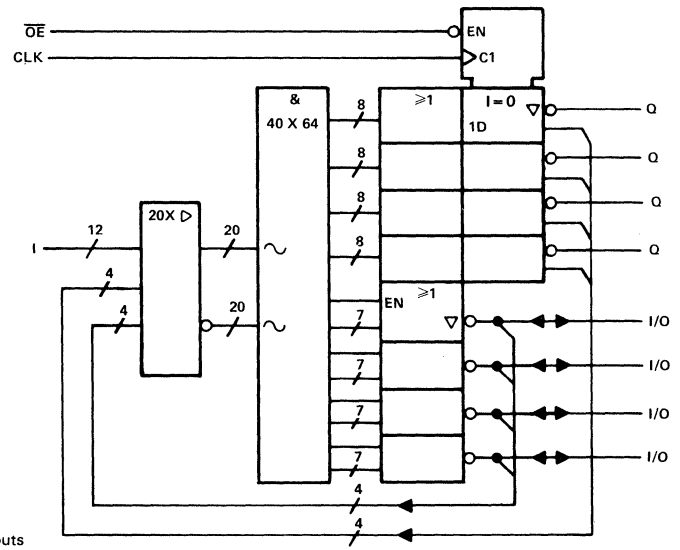
The TIBPAL20' CNL series is characterized from 0°C to 75°C.

functional block diagrams (positive logic)

TIBPAL20L8'



TIBPAL20R4'



~ denotes fused inputs

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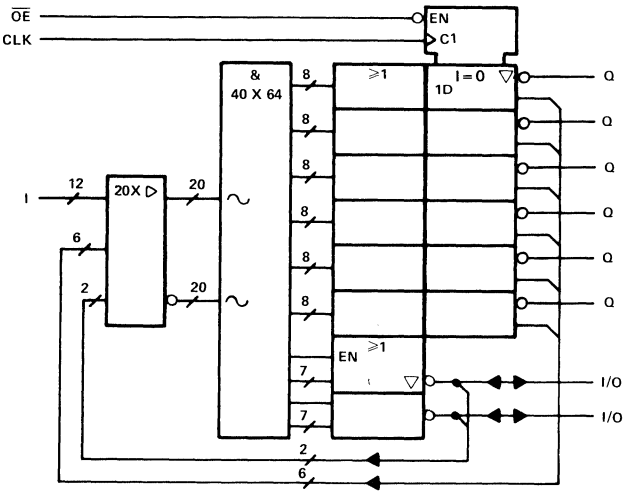
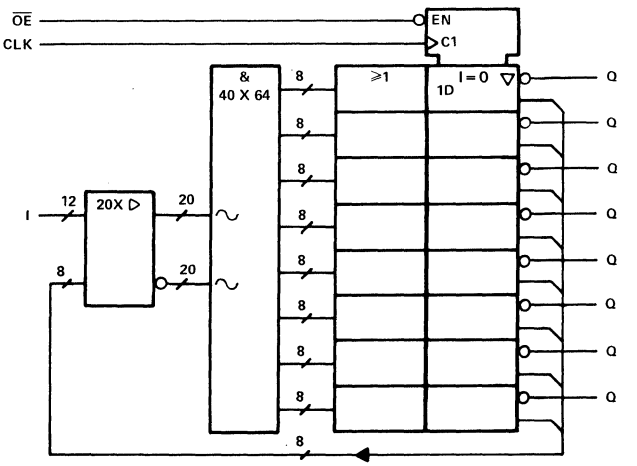
functional block diagrams (positive logic)

TIBPAL20R6'

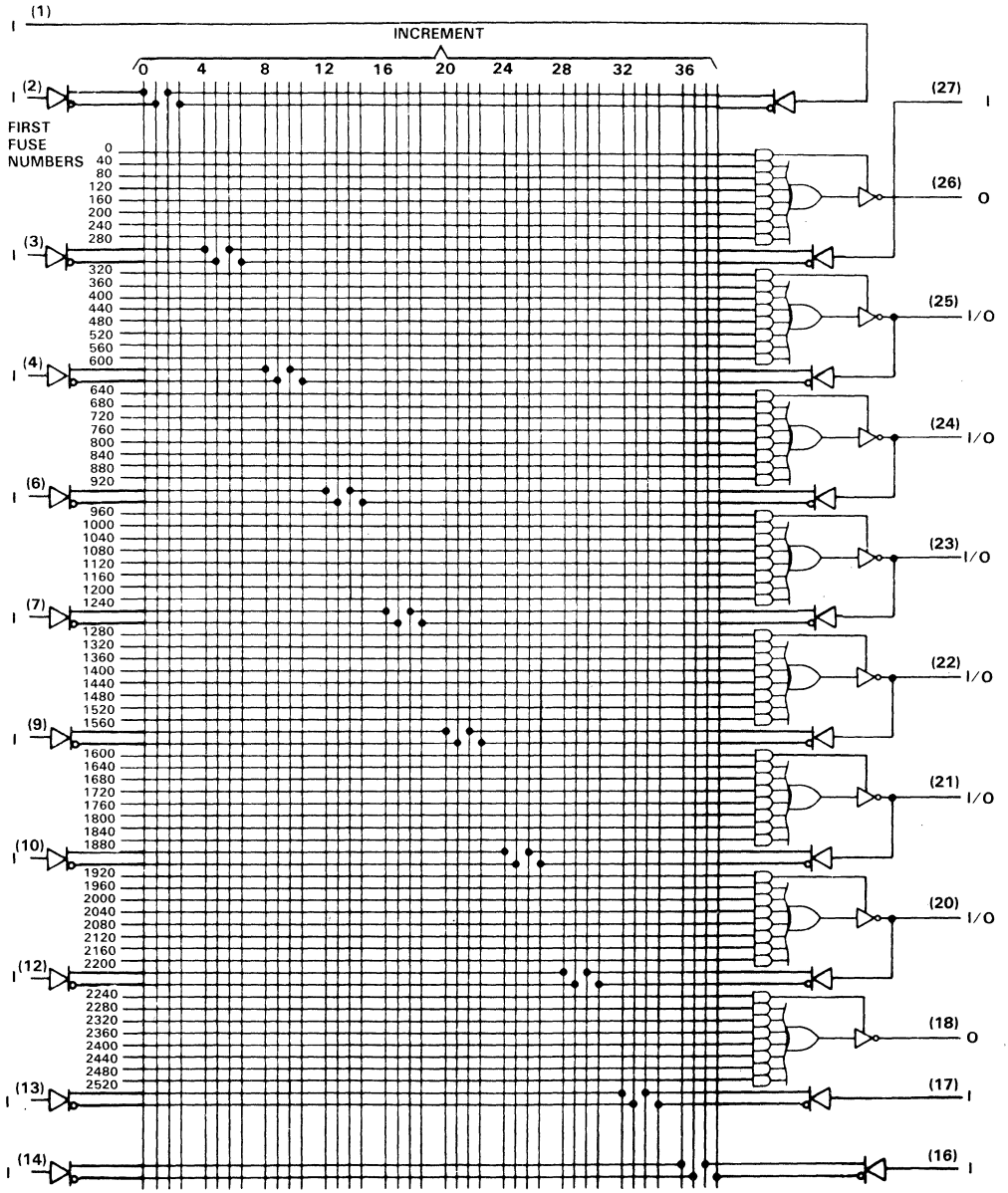


TIBPAL20R8'



∿ denotes fused inputs

logic diagram (positive logic)



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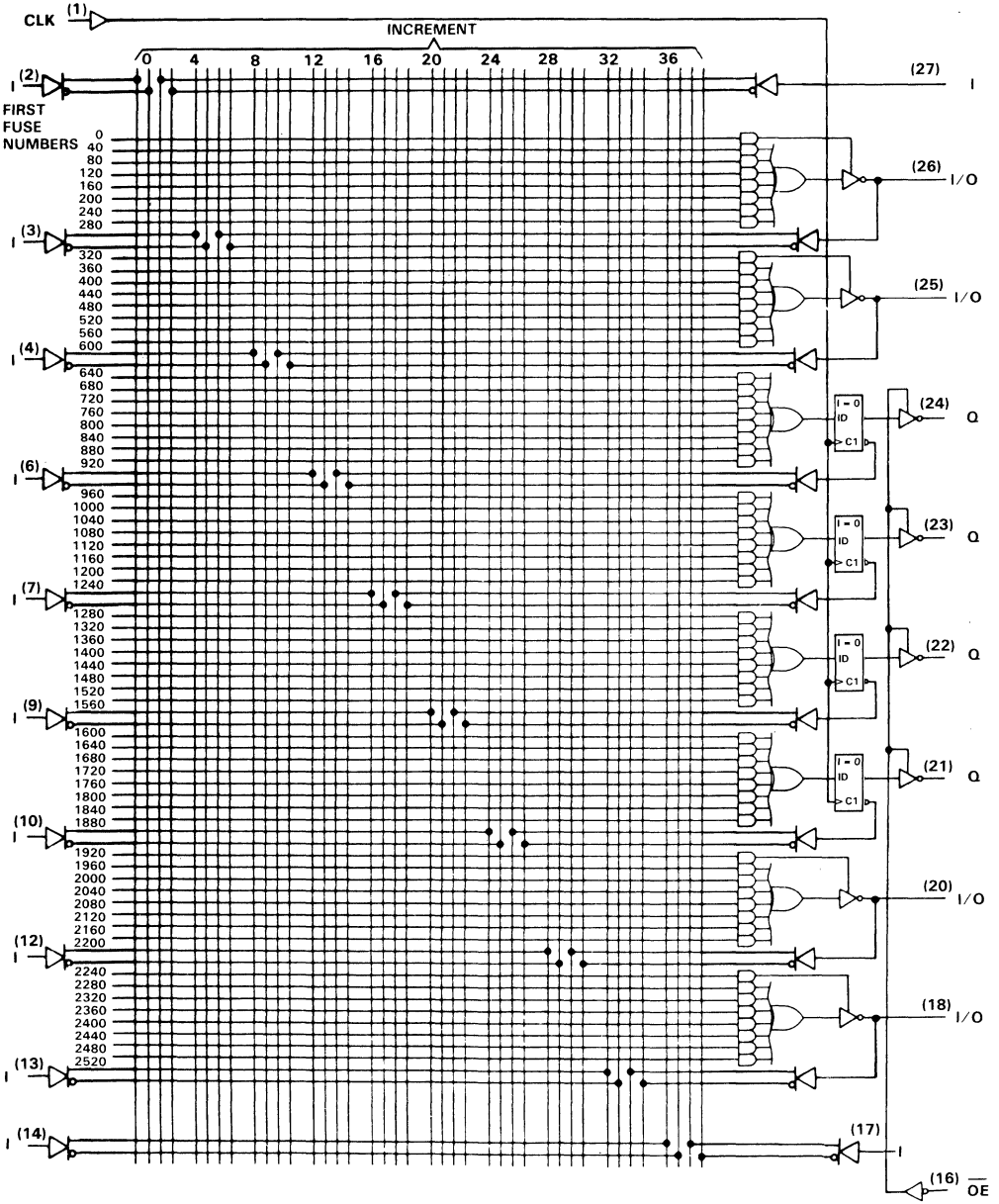
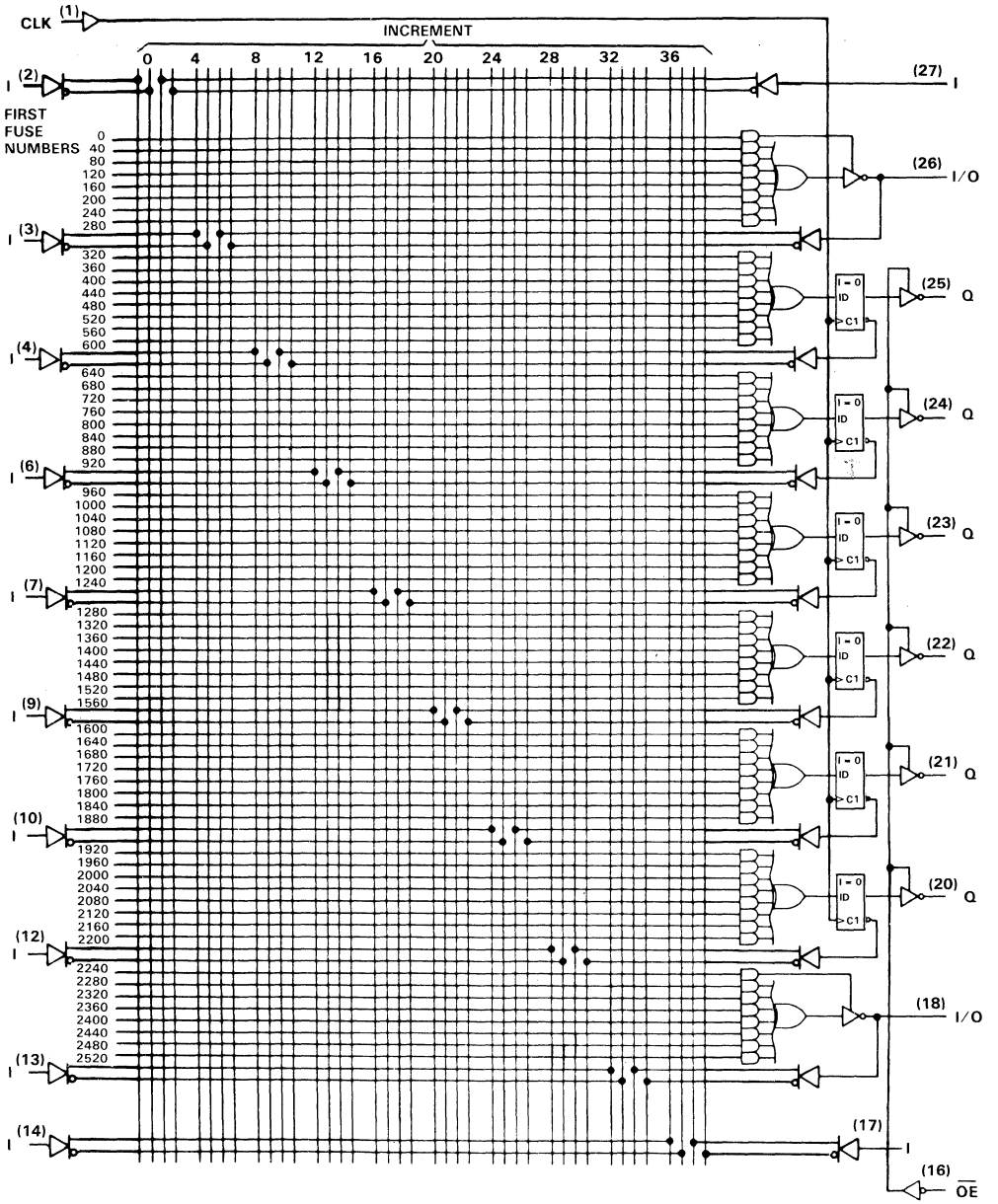
logic diagram (positive logic)



logic diagram (positive logic)



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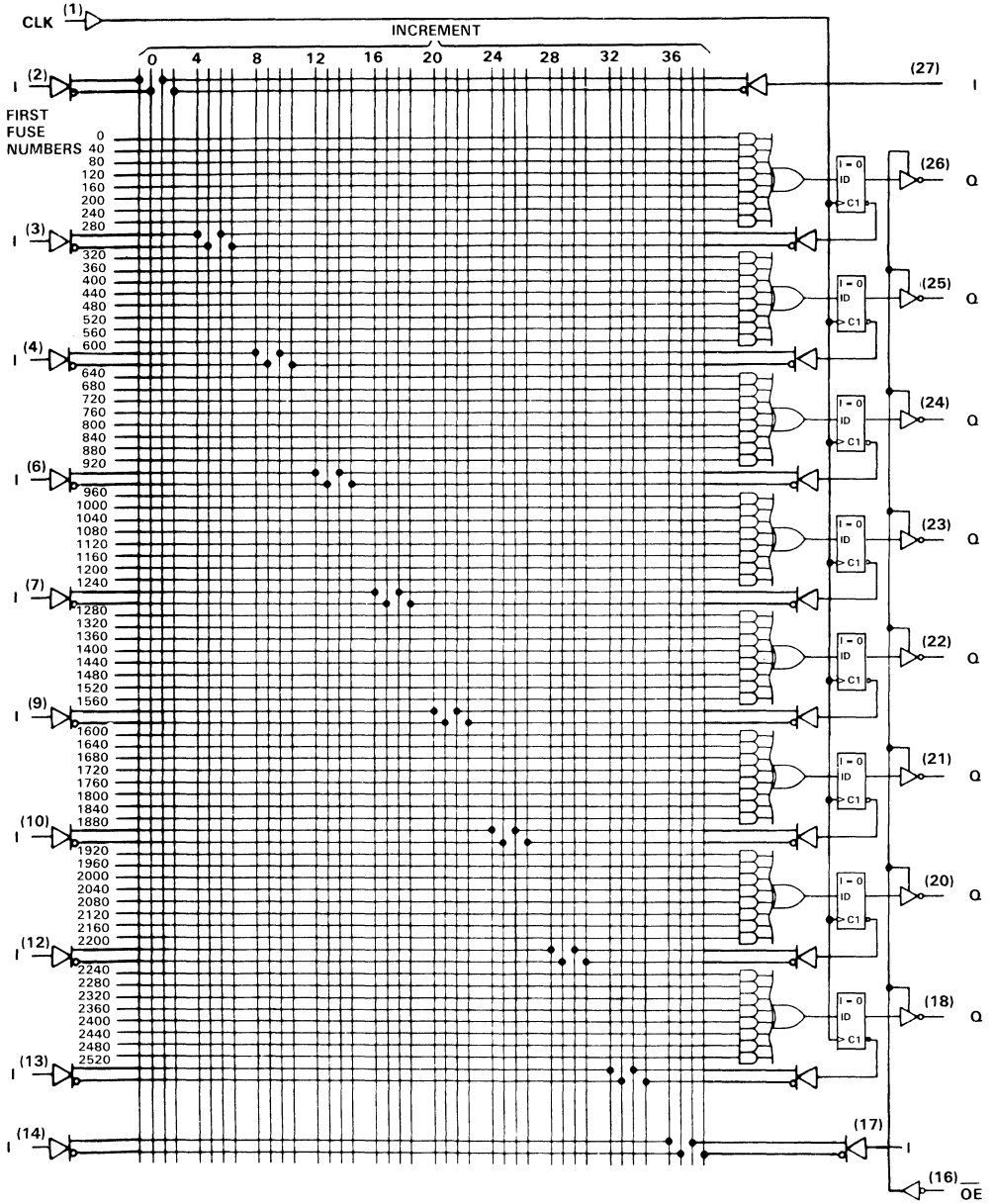
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disable output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			-25CNL			-15CNL			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−3.2			−3.2	mA
I_{OL}	Low-level output current				24			24	mA
f_{clock}	Clock frequency		0		33	0		45	MHz
t_w	Pulse duration, clock	High	15			10			ns
		Low	15			12			ns
t_{su}	Setup time, input or feedback before CLK↑		25			15	10		ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns
T_A	Operating free-air temperature		0		75	0		75	°C

†f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

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electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	-15CNL			UNIT
			MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4			V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
	I/O ports				100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
	I/O ports				−0.25	mA
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V, V_I = 2.7 V			25	μA
I_{IL}‡		V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, V_I = 0, Outputs open, $\overline{OE}$ at V_{IH}		120	180	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed 1 second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-15CNL			UNIT
				MIN	TYP†	MAX	
f_{max}¶	With feedback		R_1 = 200 Ω, R2 = 390 Ω, C_L = 50 pF, See Figure 1	37	40		MHz
	Without feedback			45	50		
t_{pd}	I, I/O	O, I/O			12	15	ns
t_{pd}	CLK↑	Q			8	12	ns
t_{en}	$\overline{OE}$	Q			10	15	ns
t_{dis}	$\overline{OE}$↑	Q			8	12	ns
t_{en}	I, I/O	O, I/O			12	18	ns
t_{dis}	I, I/O	O, I/O			12	15	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, f_{max} (without feedback) = $\frac{1}{t_w\text{ high} + t_w\text{ low}}$

f_{max} does not apply for TIBPAL20L8'

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	-25CNL			UNIT
			MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
	I/O ports				100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
	I/O ports				−0.25	mA
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
I_{IL}‡		V_{CC} = 5.25 V, V_I = 0.4 V			−0.2	mA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open, V_I = 0, $\overline{OE}$ at V_{IH}		75	105	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed 1 second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-25CNL			UNIT
				MIN	TYP†	MAX	
f_{max}¶	With feedback		R_1 = 200 Ω, R2 = 390 Ω, C_L = 50 pF, See Figure 1	25	40		MHz
	Without feedback			33	50		
t_{pd}	I, I/O	O, I/O		3	14	25	ns
t_{pd}	CLK↑	Q		2	10	15	ns
t_{en}	$\overline{OE}$	Q		2	8	15	ns
t_{dis}	$\overline{OE}$↑	Q		2	8	15	ns
t_{en}	I, I/O	O, I/O		3	15	25	ns
t_{dis}	I, I/O	O, I/O		3	15	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, f_{max} (without feedback) = $\frac{1}{t_w\text{ high} + t_w\text{ low}}$

f_{max} does not apply for TIBPAL20L8'.

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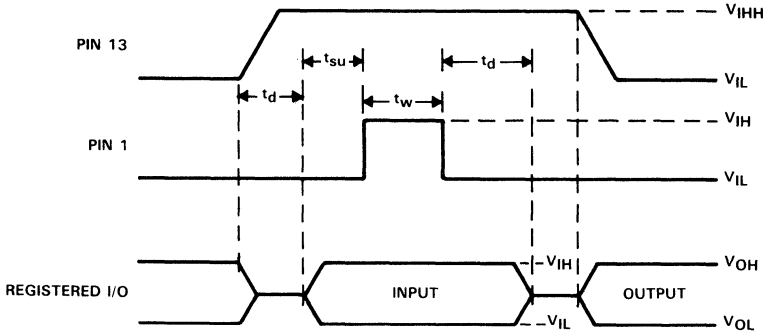
preload procedure for registered outputs (see Note 2)

The output registers of the TIBPAL20R' can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Notes 2 and 3)



NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

programming information

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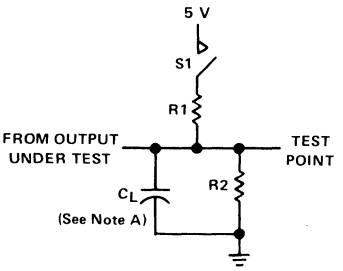
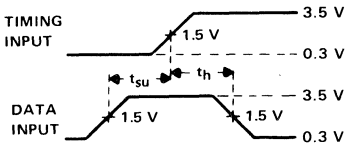
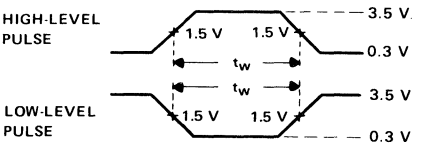
PARAMETER MEASUREMENT INFORMATION



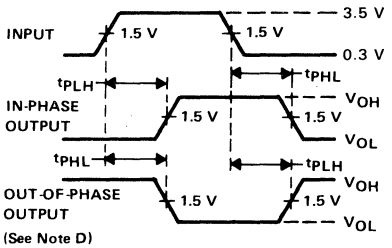
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



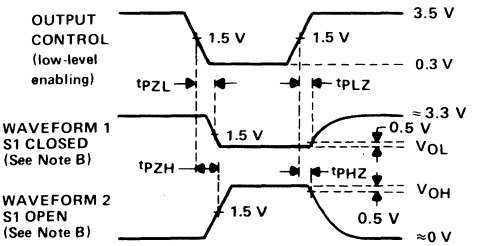
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = t_f = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

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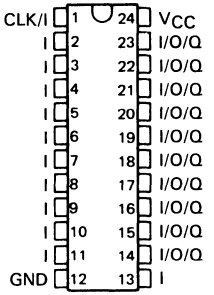
TIBPAL22V10AM, TIBPAL22V10C, TIBPAL22V10AC
HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC

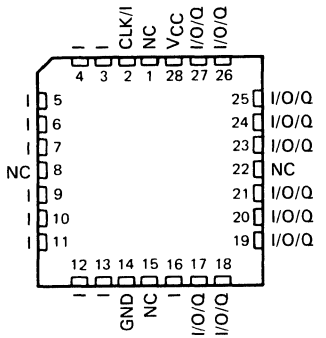
D2943, OCTOBER 1986—REVISED AUGUST 1989

- Second Generation PAL Architecture
- Choice of Operating Speeds
  - TIBPAL22V10AC . . . 25 ns Max
  - TIBPAL22V10AM . . . 30 ns Max
  - TIBPAL22V10C . . . 35 ns Max
- Increased Logic Power — Up to 22 Inputs and 10 Outputs
- Increased Product Terms — Average of 12 per Output
- Variable Product Term Distribution Allows More Complex Functions to be Implemented
- Each Output is User Programmable for Registered or Combinatorial Operation, Polarity, and Output Enable Control
- TTL-Level Preload for Improved Testability
- Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability
- Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses
- AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features
- Dependable Texas Instruments Quality and Reliability
- Package Options Include Plastic and Ceramic Dual-In-Line Packages and Chip Carriers
- Functionally Equivalent to AMDs AMPAL22V10 and AMPAL22V10A

M SUFFIX . . . JT PACKAGE
C SUFFIX . . . NT PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection
Pin assignments in operating mode

description

The TIBPAL22V10 and TIPPAL22V10A are programmable array logic devices featuring high speed and functional equivalency when compared to presently available devices. They are implemented with the familiar sum-of-products (AND-OR) logic structure featuring the new concept "Programmable Output Logic Macrocell". These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable high-performance substitutes for conventional TTL logic.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10 and TIBPAL22V10A offer quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power-up with their outputs high. Registered outputs selected as active-high power-up with their outputs low.

A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

The M suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The C suffix devices are characterized for operation from 0°C to 75°C.

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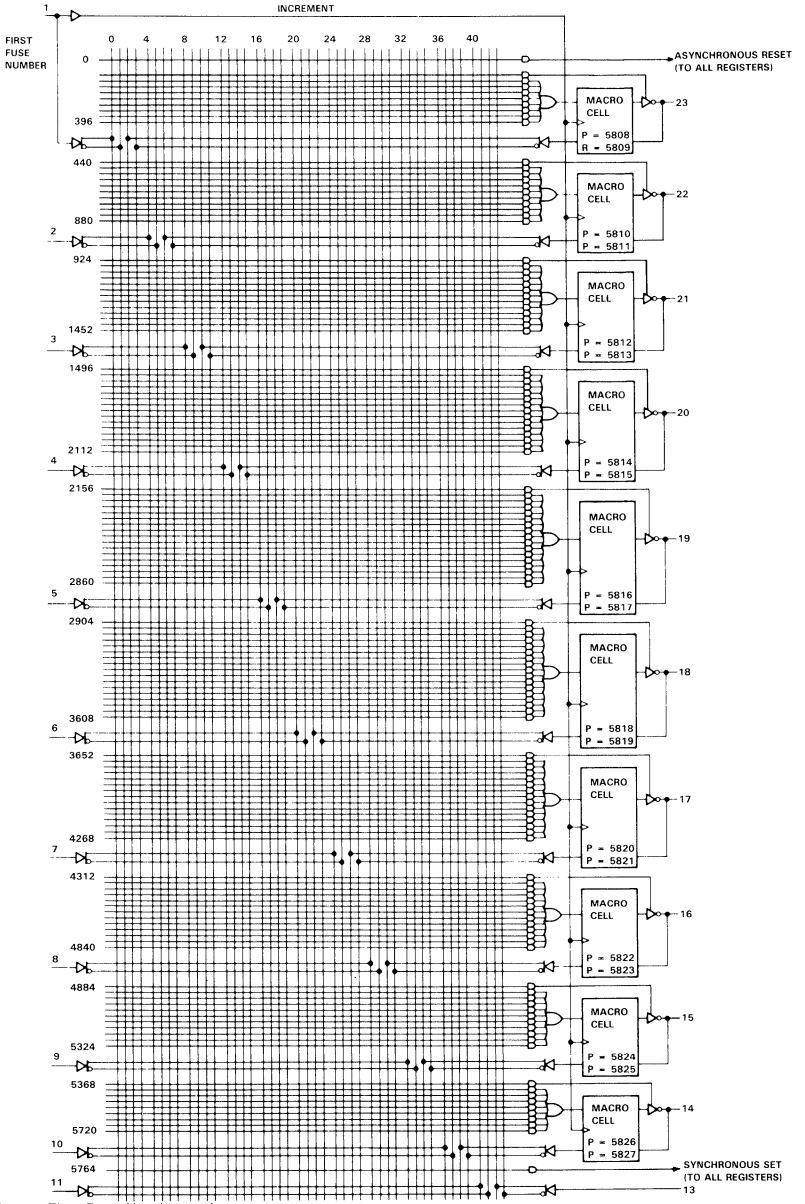
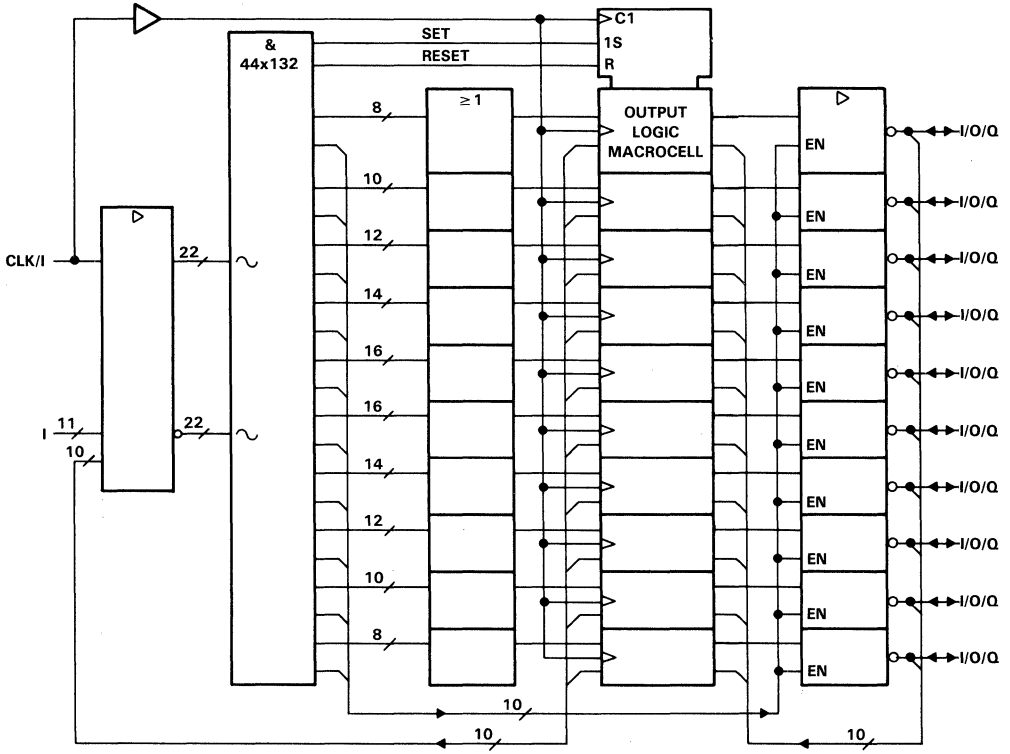
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

functional block diagram (positive logic)



∼ denotes fused inputs

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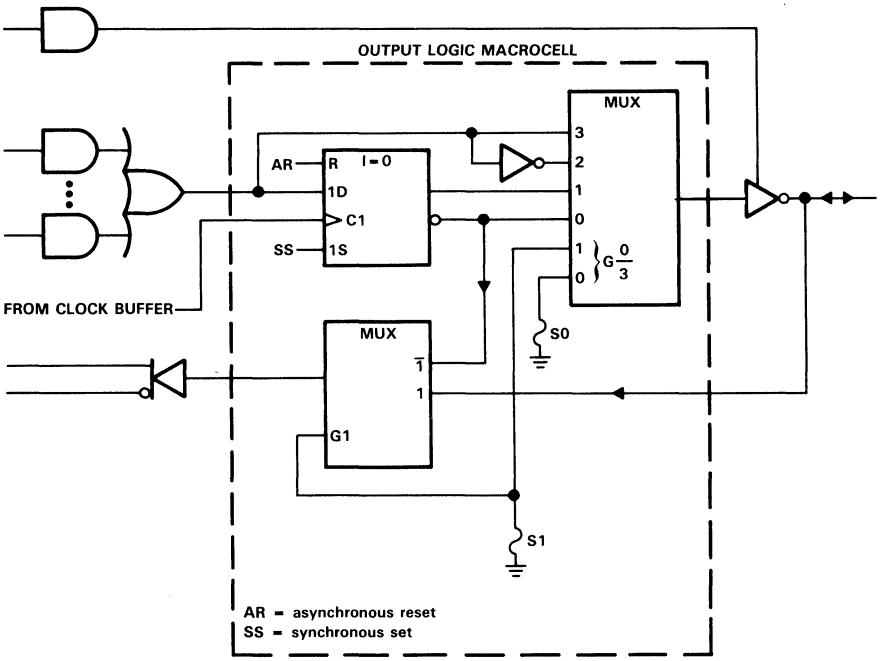
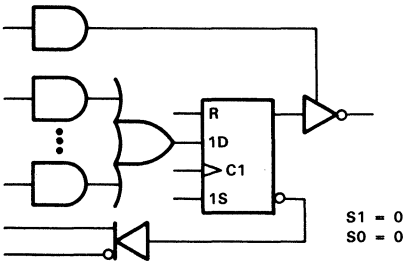
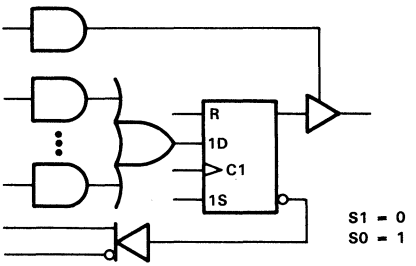
output logic macrocell diagram

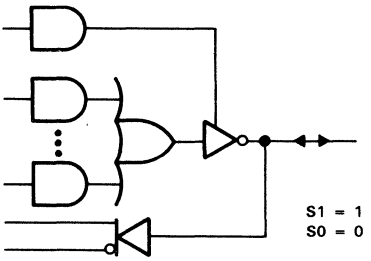




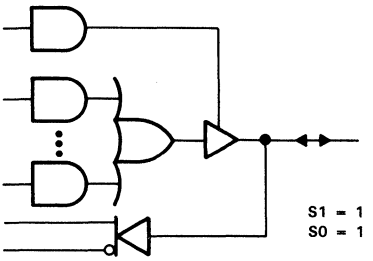
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse
S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

FIGURE 1. RESULTANT MACROCELL FEEDBACK AND OUTPUT LOGIC AFTER PROGRAMMING

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a pre-load cycle.

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recommended operating conditions

			TIBPAL22V10AM			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency†				22	MHz
t_w	Pulse duration	Clock high or low	20			ns
		Asynchronous Reset high or low	30			
t_{su}	Setup time before clock↑	Input	25			ns
		Feedback	25			
		Synchronous Set	25			
		Asynchronous Reset low (inactive)	30			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		−55		125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	TIBPAL22V10AM			UNIT
			MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA	2.4	3.5		V
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA		0.25	0.5	V
I_{OZH}		V_{CC} = 5.5 V, V_O = 2.7 V			0.1	mA
I_{OZL}	Any output	V_{CC} = 5.5 V, V_O = 0.4 V			−100	μA
	Any I/O				−250	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V			1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V			25	μA
I_{IL}		V_{CC} = 5.5 V, V_I = 0.4 V			−0.25	mA
I_{OS}§		V_{CC} = 5.5 V, V_O = 0.5 V	−30		−90	mA
I_{CC}		V_{CC} = 5.5 V, V_I = GND, Outputs open		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	TIBPAL22V10AM			UNIT
				MIN	TYP‡	MAX	
f_{max}†	With feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 2	22			MHz
t_{pd}	I, I/O	I/O			15	30	ns
t_{pd}	I, I/O (reset)	Q			15	35	ns
t_{pd}	Clock	Q			10	20	ns
t_{en}	I, I/O	Q			15	30	ns
t_{dis}	I, I/O	Q			15	30	ns

†f_{max} and f_{clock} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, f_{max} and f_{clock} without feedback can be calculated as f_{max} and $f_{clock}\text{ (without feedback)} = \dfrac{1}{t_w\text{ high} + t_w\text{ low}}$.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test problems caused by test equipment ground degradation.

recommended operating conditions

			TIBPAL22V10C			TIBPAL22V10AC			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−3.2			−3.2	mA
I_{OL}	Low-level output current				16			16	mA
f_{clock}	Clock frequency†				18			28.5	MHz
t_w	Pulse duration	Clock high or low	25			15			ns
		Asynchronous Reset high or low	35			25			
t_{su}	Setup time before clock↑	Input	30			20			ns
		Feedback	30			20			
		Synchronous Set	30			20			
		Asynchronous Reset low (inactive)	35			25			
t_h	Hold time, input, set, or feedback after clock↑		0			0			ns
T_A	Operating free-air temperature		0		75	0		75	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	TIBPAL22V10C			TIBPAL22V10AC			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3.5		2.4	3.5		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
I_{OZH}		V_{CC} = 5.25 V, V_O = 2.7 V			0.1			0.1	mA
I_{OZL}	Any output	V_{CC} = 5.25 V, V_O = 0.4 V			−100			−100	μA
	Any I/O				−250			−250	
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			1			1	mA
I_{IH}		V_{CC} = 5.25 V, V_I = 2.7 V			25			25	μA
I_{IL}		V_{CC} = 5.25 V, V_I = 0.4 V			−0.25			−0.25	mA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0.5 V	−30		−90	−30		−90	mA
I_{CC}		V_{CC} = 5.25 V, V_I = GND, Outputs open		120	180		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	TIBPAL22V10C			TIBPAL22V10AC			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}†	With feedback		R1 = 300 Ω, R2 = 390 Ω, See Figure 2	18			28.5			MHz
t_{pd}	I, I/O	I/O			15	35		15	25	ns
t_{pd}	I, I/O (reset)	Q			15	40		15	30	ns
t_{pd}	Clock	Q			10	25		10	15	ns
t_{en}	I, I/O	Q			15	35		15	25	ns
t_{dis}	I, I/O	Q			15	35		15	25	ns

†f_{max} and f_{clock} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{max} and f_{clock} without feedback can be calculated as f_{max} and

$f_{clock}\ (\text{without feedback}) = \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test problems caused by test equipment ground degradation.

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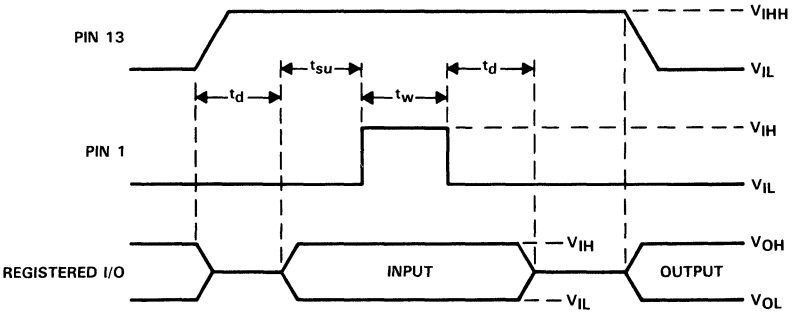
preload procedure for registered outputs (see Note 2)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Notes 2 and 3)

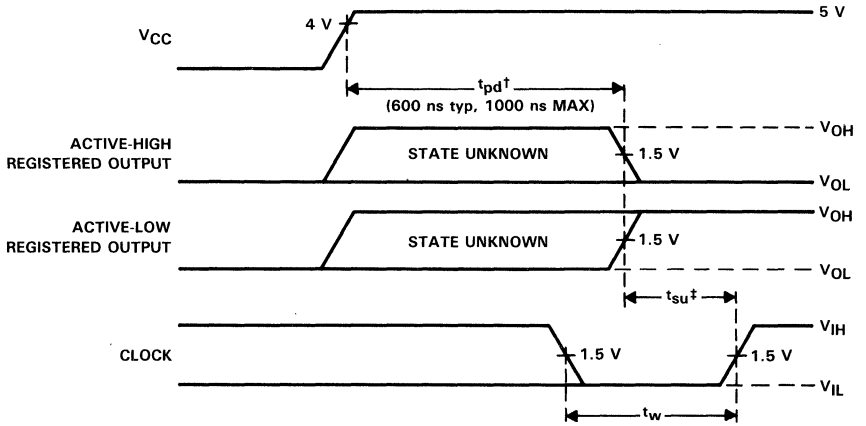


NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power-up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the V_{CC}'s rise be monotonic. Following power-up, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

power-up reset waveforms



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

TEXAS INSTRUMENTS
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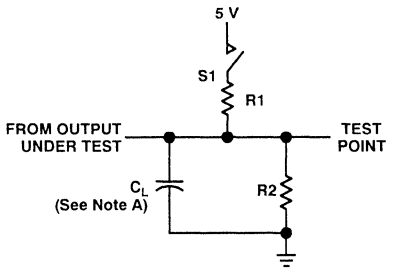
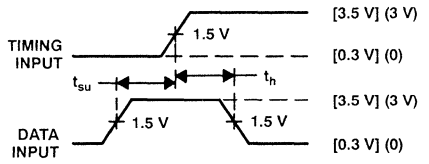
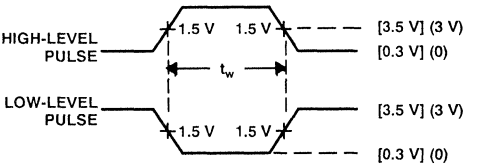
PARAMETER MEASUREMENT INFORMATION



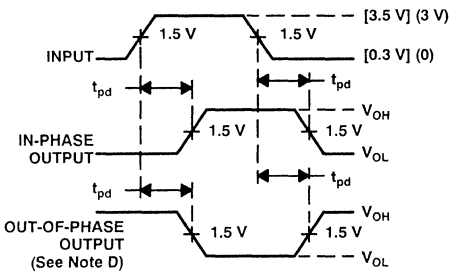
LOAD CIRCUIT FOR 3-STATE OUTPUTS



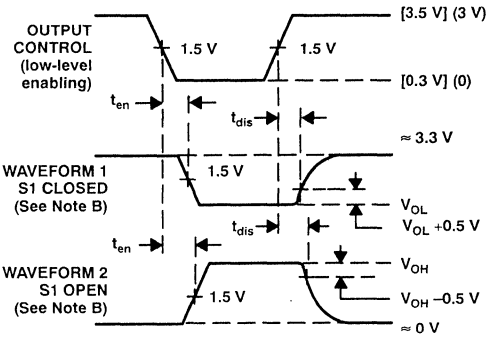
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For M suffix, use the voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be fused for testing.

FIGURE 2

TIBPAL22V10-20M, TIBPAL22V10-15C
HIGH-PERFORMANCE *IMPACT-X*™ PROGRAMMABLE ARRAY LOGIC

D3356, OCTOBER 1989

- Second-Generation PAL Architecture
- Choice of Operating Speeds
  - TIBPAL22V10-15C . . . 15 ns Max
  - TIBPAL22V10-20M . . . 20 ns Max
- Increased Logic Power — up to 22 Inputs and 10 Outputs
- Increased Product Terms — Average of 12 per Output
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- Each Output Is User Programmable for Registered or Combinatorial Operation, Polarity, and Output Enable Control
- Power-Up Clear on Registered Outputs
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- Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability
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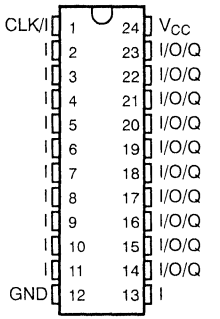
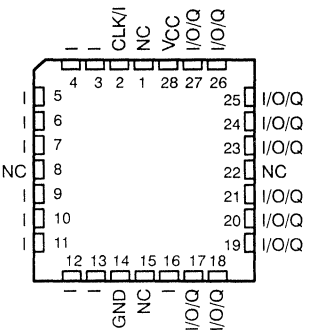
- AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features
- Dependable Texas Instruments Quality and Reliability
- Package Options Include Plastic and Ceramic Dual-In-Line Packages and Chip Carriers

M SUFFIX . . . JT PACKAGE
C SUFFIX . . . NT PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection
Pin assignments in operating mode

PRODUCT PREVIEW

description

The TIBPAL22V10-15C and TIBPAL22V10-20M are programmable array logic devices featuring high speed and functional equivalency when compared to presently available devices. They are implemented with the familiar sum-of-products (AND-OR) logic structure featuring the new concept "Programmable Output Logic Macrocell". These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

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description (continued)

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10' offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power-up with their outputs high. Registered outputs selected as active-high power-up with their outputs low.

A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

The M suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The C suffix devices are characterized for operation from 0°C to 75°C.

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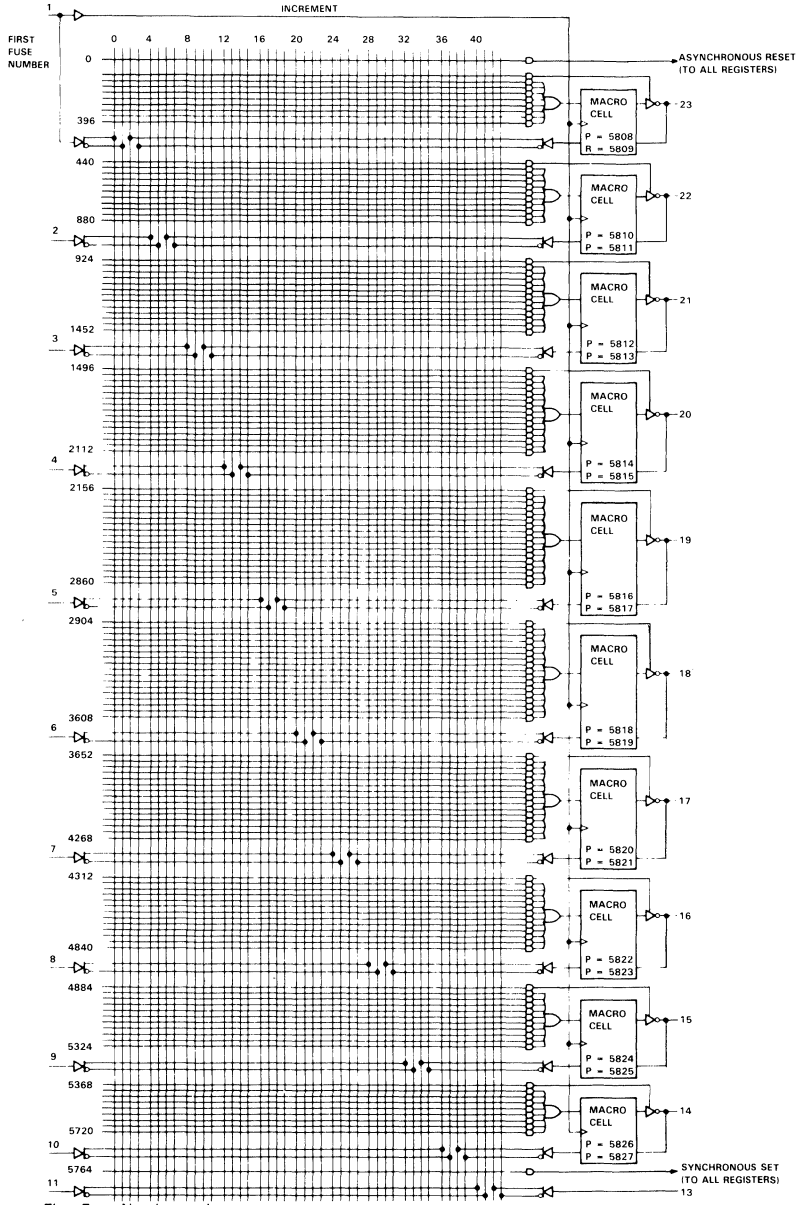
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment

Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

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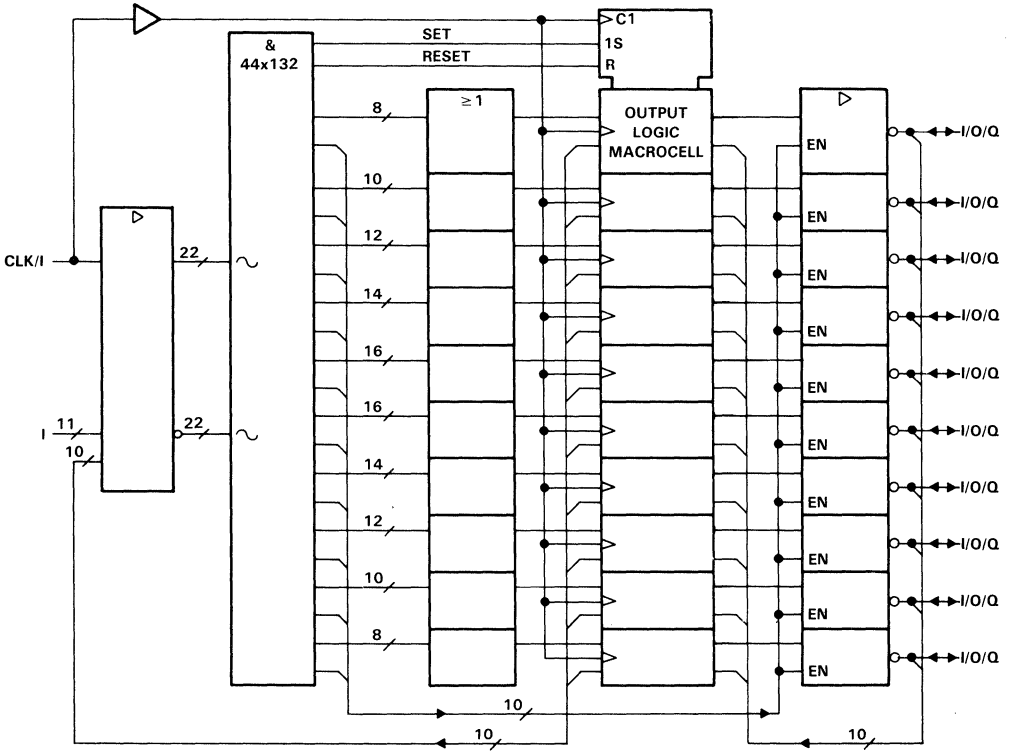
functional block diagram (positive logic)



~ denotes fused inputs

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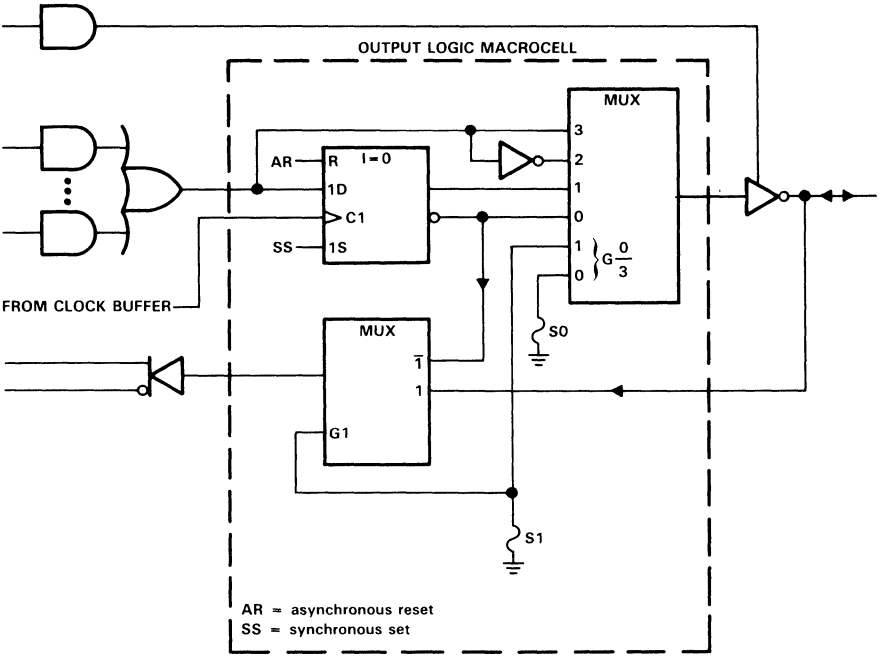
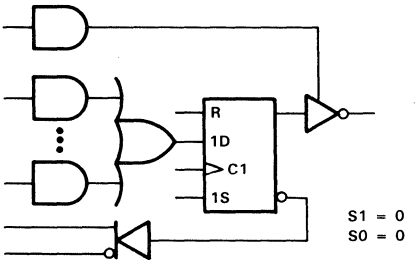
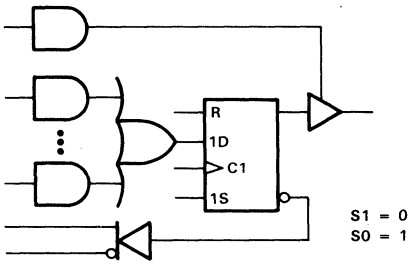
output logic macrocell diagram



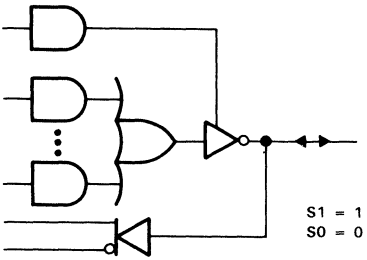
PRODUCT PREVIEW



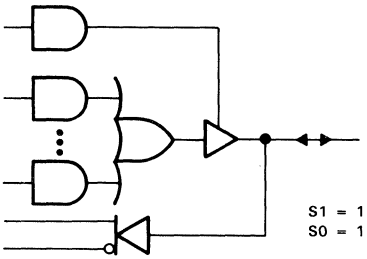
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse
S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

FIGURE 1. RESULTANT MACROCELL FEEDBACK AND OUTPUT LOGIC AFTER PROGRAMMING

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Voltage applied to diabled output (see Note 1) ..... 5.5 V
Operating free-air temperature range ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
t_w	Pulse duration	Clock high or low				ns
		Asynchronous Reset high or low				
t_{su}	Setup time before clock↑†	Input				ns
		Feedback				
		Synchronous Preset				
		Asynchronous Reset low (inactive)				
t_h	Hold time, input, set, or feedback after clock↑					ns
T_A	Operating free-air temperature		−55		125	°C

† The values for this parameter can only be obtained with a pulse repetition rate of 1 MHz.

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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.5		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.5	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V				0.1	mA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V				−0.1	mA
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V				25	μA
I_{IL}	CLK	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.15	mA
	All others						−0.1	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		−30		−90	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = GND,	Outputs open			180	mA
C_i		f = 1 MHz,	V_I = 2 V					pF
C_o		f = 1 MHz,	V_O = 2 V					pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}§	External feedback					MHz
t_{pd}	I, I/O	I/O	R1 = 390 Ω,			ns
t_{pd}	I, I/O (reset)	Q	R2 = 750 Ω,			ns
t_{pd}	Clock	Q	See Figure 2			ns
t_{en}	I, I/O	I/O, Q				ns
t_{dis}	I, I/O	I/O, Q				ns

§ f_{max} (with feedback) = $\dfrac{1}{t_{su} + t_{pd}\ (CLK\ to\ Q)}$.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high or low	10			ns
		Asynchronous Reset high or low	15			
t_{su}	Setup time before clock↑†	Input	13			ns
		Feedback	13			
		Synchronous Preset	13			
		Asynchronous Reset low (inactive)	15			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0		75	°C

† The values for this parameter can only be obtained with a pulse repetition rate of 1 MHz.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA		2.4	3.5		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.35	0.5	V
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.7 V				0.1	mA
		V_{CC} = 5.25 V,	V_O = 0.4 V				−0.1	mA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}		V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}	CLK	V_{CC} = 5.25 V,	V_I = 0.4 V				−0.15	mA
	All others						−0.1	
I_{OS}‡		V_{CC} = 5.25 V,	V_O = 0.5 V		−30		−90	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = GND,	Outputs open			180	mA
C_i		f = 1 MHz,	V_I = 2 V					pF
C_o		f = 1 MHz,	V_O = 2 V					pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

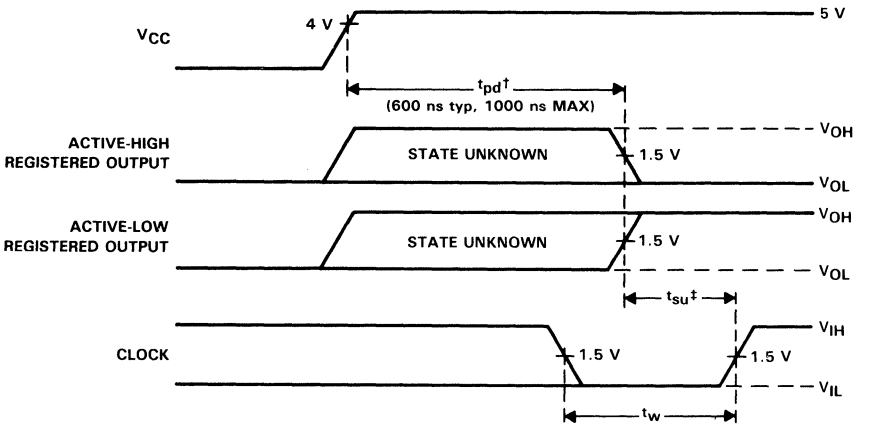
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}§	External feedback			40		MHz
t_{pd}	I, I/O	I/O			15	ns
t_{pd}	I, I/O (reset)	Q	R1 = 300 Ω,		20	ns
t_{pd}	Clock	Q	R2 = 390 Ω,		12	ns
t_{pd}	Clock	I/O	See Figure 2		22	ns
t_{en}	I, I/O	I/O, Q			15	ns
t_{dis}	I, I/O	I/O, Q			15	ns

§ f_{max} (with feedback) = $\dfrac{1}{t_{su} + t_{pd}\ (CLK\ to\ Q)}$.

power-up reset

Following power-up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

power-up reset waveforms



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

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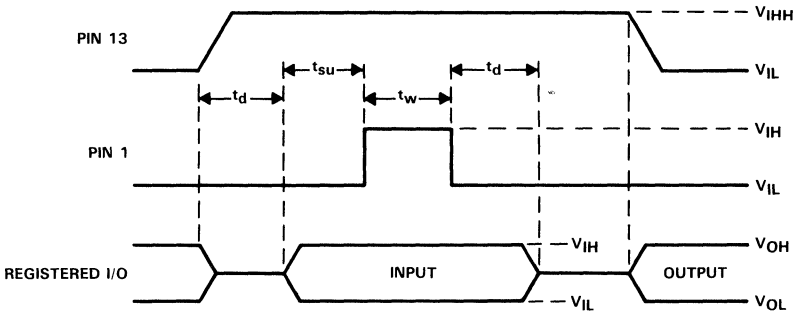
preload procedure for registered outputs (see Note 2)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to setup through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Notes 2 and 3)



NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

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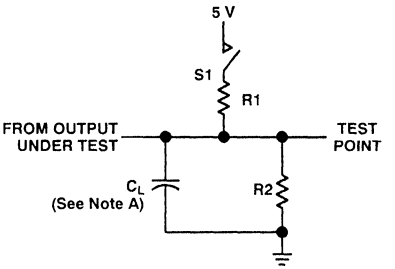
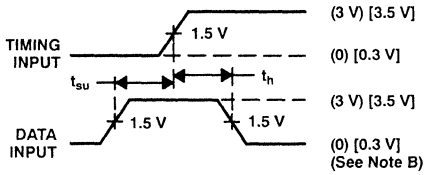
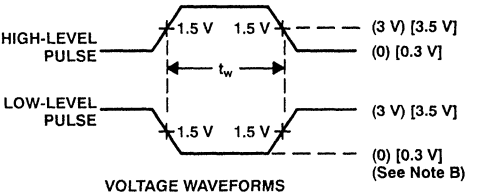
PARAMETER MEASUREMENT INFORMATION



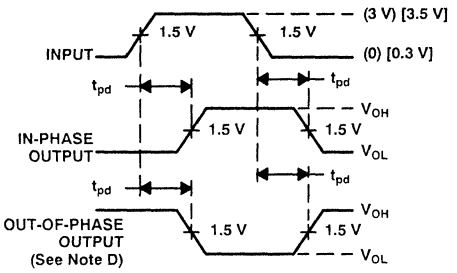
LOAD CIRCUIT FOR 3-STATE OUTPUTS



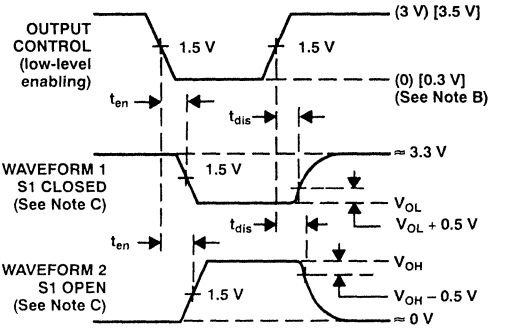
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: For M suffix, use the voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [ ] PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

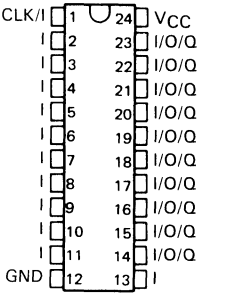
FIGURE 2

PRODUCT PREVIEW

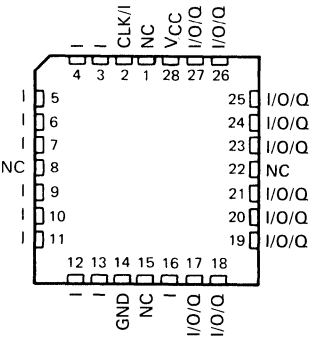
D2943, FEBRUARY 1987—REVISED OCTOBER 1989

- **Functionally Equivalent to the TIBPAL22V10/10A, with Additional Feedback Paths in the Output Logic Macrocell**
- **Choice of Operating Speeds:**
  TIBPAL22VP10-20C . . . 20 ns Max
  TIBPAL22VP10-25M . . . 25 ns Max
- **Variable Product Term Distribution Allows More Complex Functions to be Implemented**
- **Polarity of Each Output is Programmable**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Dependable Texas Instruments Quality and Reliability**
- **Package Options Include Plastic and Ceramic Dual-In-Line Packages and Chip Carriers**

M SUFFIX . . . JT PACKAGE
C SUFFIX . . . NT PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection
Pin assignments in operating mode

description

The TIBPAL22VP10 is equivalent to the TIBPAL22V10A but offers additional flexibility in the output structure. The improved output macrocell uses the registered outputs as inputs when in a high-impedance condition. This provides two additional output configurations for a total of six possible macrocell configurations all of which are shown in Figure 1.

The device contains up to twenty-two inputs and ten outputs. It defines and programs the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting. In addition, the data may be fed back into the array from either the register or the I/O port. The ten potential outputs are enabled through the use of individual product terms.

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

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Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

With features such as programmable output logic macrocells and variable product terms, the TIBPAL22VP10 offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power-up with their outputs high. Registered outputs selected as active-high power-up with their outputs low.

A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

The TIBPAL22VP10-25M is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL22VP10-20C is characterized for operation from 0°C to 75°C.

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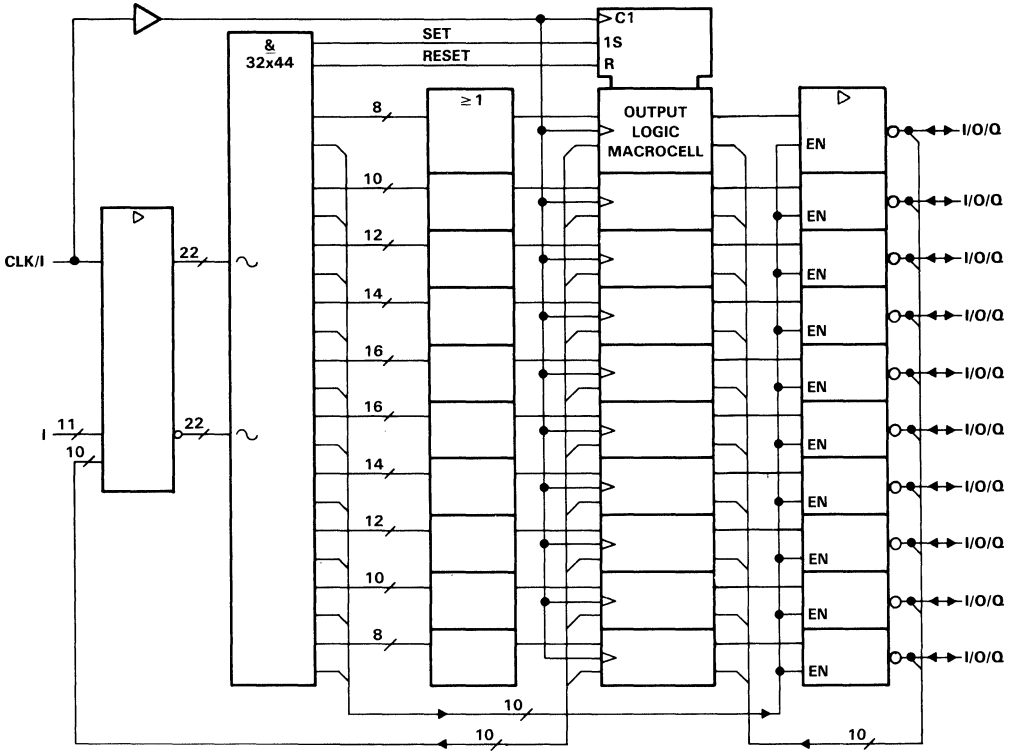
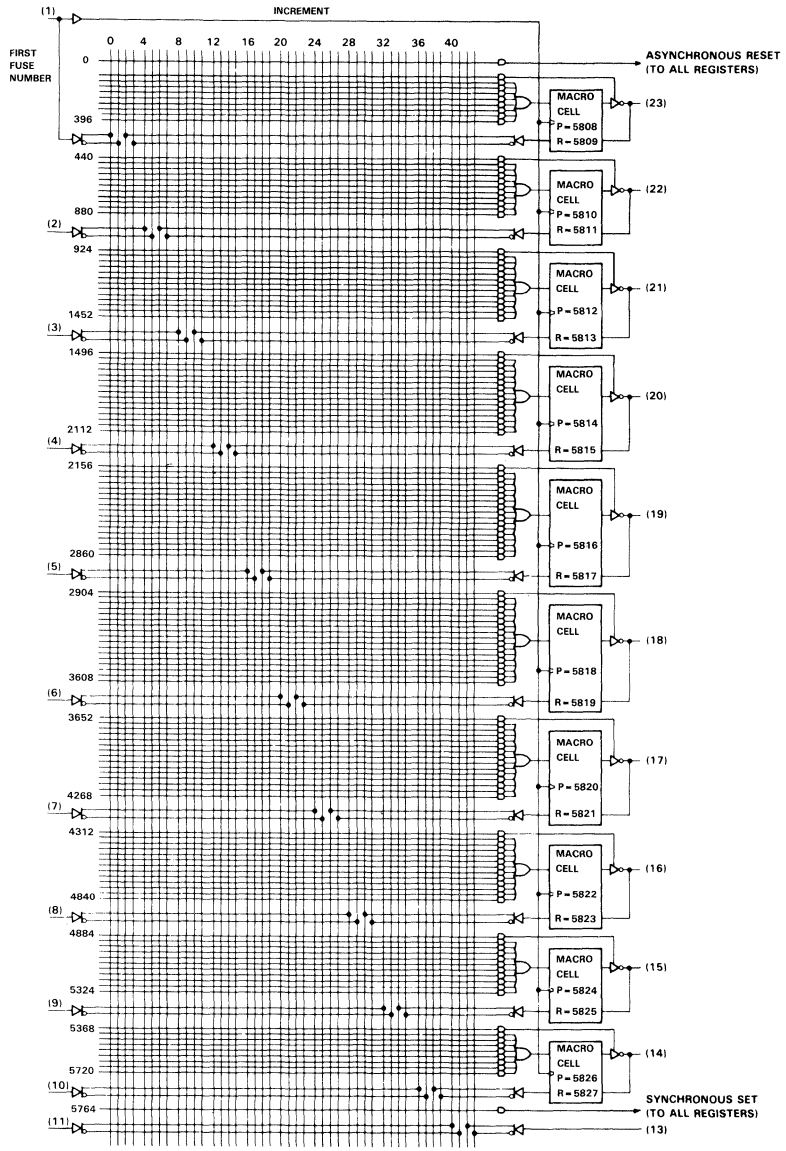
functional block diagram (positive logic)



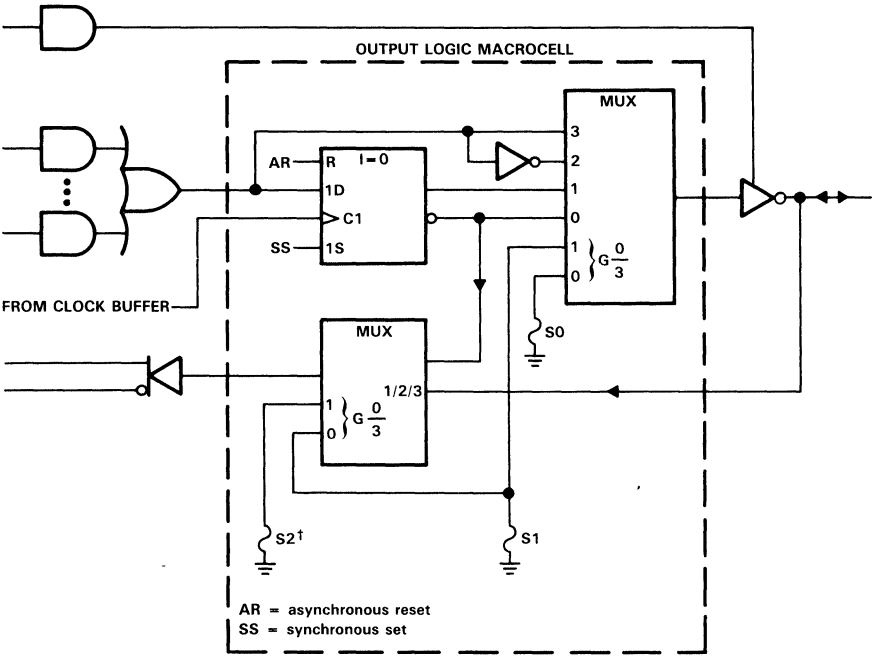
~ denotes fused inputs

logic diagram (positive logic)

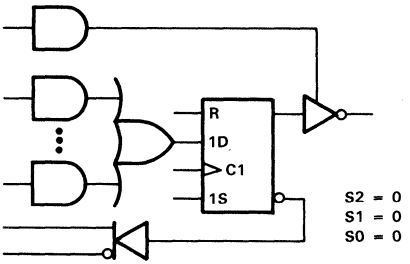


Fuse Number = First Fuse Number − Increment
Inside each MACROCELL, the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

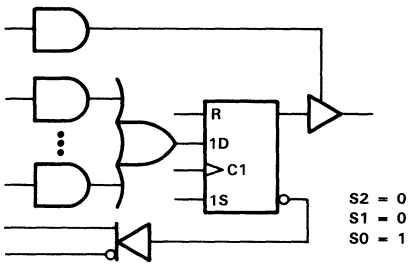
output logic macrocell diagram



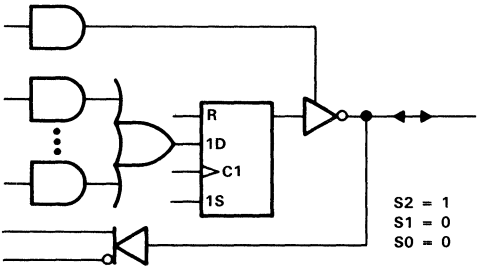
† This fuse is unique to the Texas Instruments TIBPAL22VP10A. It allows feedback from the I/O port using registered outputs as shown in the macrocell fusing logic function table.



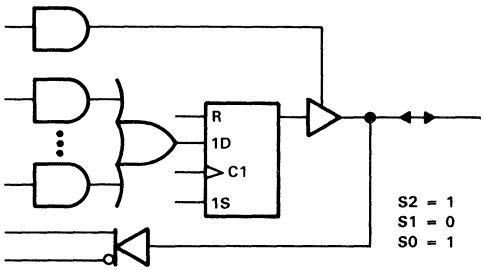
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



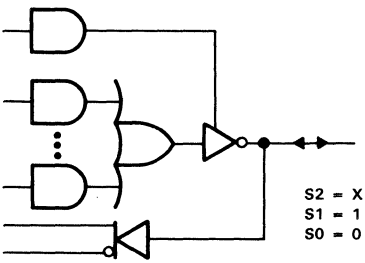
REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



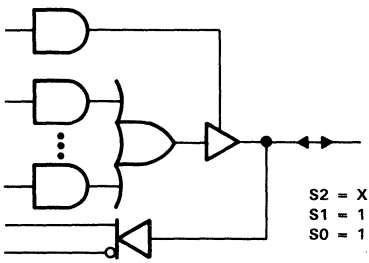
I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT†



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT†



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

† These configurations are unique to the TIBPAL22VP10 and provide added flexibility when comparing it to the TIBPAL22V10 or TIBPAL22V10A.

FIGURE 1. RESULTANT MACROCELL FEEDBACK AND OUTPUT LOGIC AFTER PROGRAMMING

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MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

PROGRAM-FUSE SELECT			FEEDBACK AND OUTPUT CONFIGURATION		
S2	S1	S0			
0	0	0	Register feedback	Registered	Active low
0	0	1	Register feedback	Registered	Active high
1	0	0	I/O feedback	Registered	Active low
1	0	1	I/O feedback	Registered	Active high
X	1	0	I/O feedback	Combinational	Active low
X	1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse, X = unblown or blown fuse
S2, S1, and S0 are select-function fuses as shown in the output logic macrocell diagram.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: TIBPAL22VP10-25M . . . . . −55°C to 125°C
TIBPAL22VP10-20C . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a pre-load cycle.

recommended operating conditions

			TIBPAL22VP10-25M			TIBPAL22VP10-20C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			16	mA
f_{clock}	Clock frequency†				25			37	MHz
t_w	Pulse duration	Clock high or low	20			10			ns
		Reset high	30			20			
t_{su}	Setup time before clock†	Input	25			15			ns
		Feedback	25			15			
		Preset	25			15			
		Reset low (inactive)	30			20			
t_h	Hold time, input, preset, or feedback after clock†		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

† f_{clock} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{clock} without feedback can be calculated as

f_{clock} (without feedback) $= \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.4	3.5		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.5	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			0.1	mA
I_{OZL}	Any output	V_{CC} = 5.5 V,	V_O = 0.4 V			−100	μA
	Any I/O					−250	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			25	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.25	mA
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V	−30		−90	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = GND, Outputs open		140	220	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§				25	50		MHz
t_{pd}	I, I/O	I/O	C_L = 50 pF,		12	25	ns
t_{pd}	I, I/O (reset)	Q	R1 = 390 Ω,		12	25	ns
t_{pd}	Clock	Q	R2 = 750 Ω,		8	15	ns
t_{en}	I, I/O	Q	See Figure 2		12	25	ns
t_{dis}	I, I/O	Q			12	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test problems caused by test equipment ground degradation.

§ f_{max} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, f_{max} without feedback can be calculated as

$$f_{max}\text{ (without feedback)} = \frac{1}{t_w\text{ high} + t_w\text{ low}}.$$

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4	3.5		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA		0.35	0.5	V
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.7 V			0.1	mA
I_{OZL}	Any output	V_{CC} = 5.25 V,	V_O = 0.4 V			−100	μA
	Any I/O					−250	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			1	mA
I_{IH}		V_{CC} = 5.25 V,	V_I = 2.7 V			25	μA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.4 V			−0.25	mA
I_{OS}‡		V_{CC} = 5.25 V,	V_O = 0.5 V	−30		−90	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = GND, Outputs open		140	210	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§				37	50		MHz
t_{pd}	I, I/O	I/O	C_L = 50 pF,		12	20	ns
t_{pd}	I, I/O (reset)	Q	R1 = 300 Ω,		12	20	ns
t_{pd}	Clock	Q	R2 = 390 Ω,		8	12	ns
t_{en}	I, I/O	Q	See Figure 2		12	20	ns
t_{dis}	I, I/O	Q			12	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test problems caused by test equipment ground degradation.

§ f_{max} (with feedback) = $\dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{max} without feedback can be calculated as

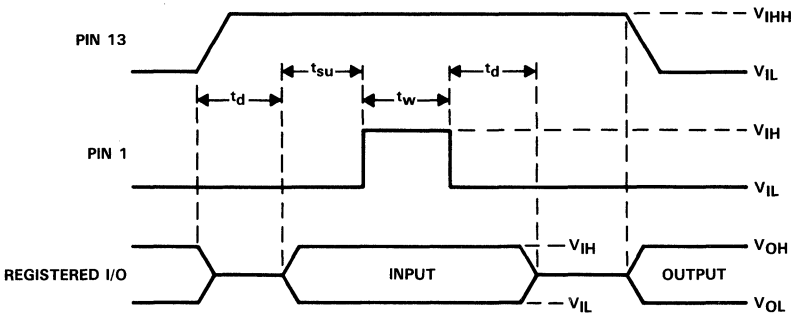
f_{max} (without feedback) = $\dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$.

preload procedure for registered outputs (see Note 2)

The output registers of the TIBPAL22VP10 can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Notes 2 and 3)



NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

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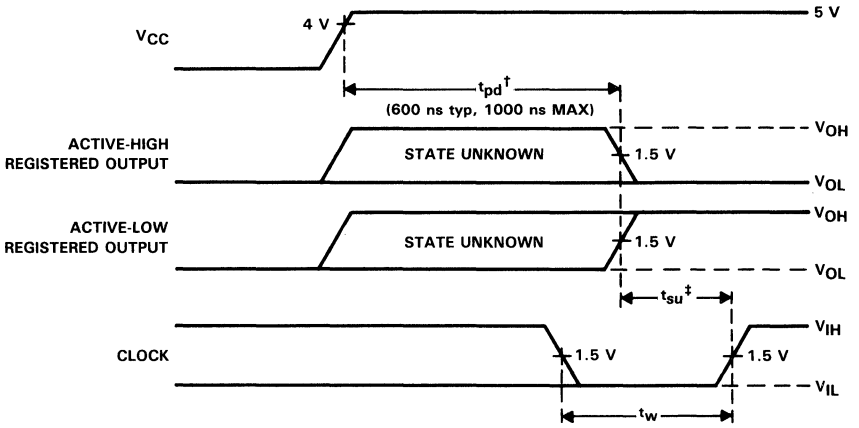
power-up reset

Following power-up, all registers of the TIBPAL22VP10 are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the V_{CC}'s rise be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

power-up reset waveforms



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

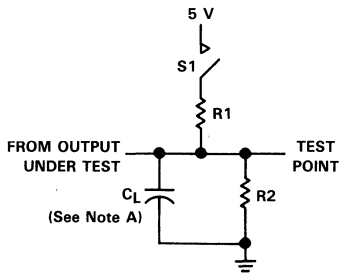
programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

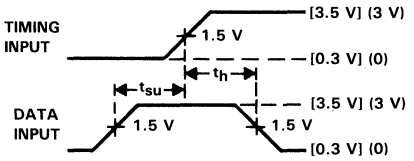
When the additional fuses are not being used, the TIBPAL22VP10 can be programmed using the TIBPAL22V10/10A programming alogrithm. The fuse configuration data can either be from a JEDEC file (format per JEDEC Standard No. 3-A) or a TIBPAL22V10/10A master.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 995-5666.

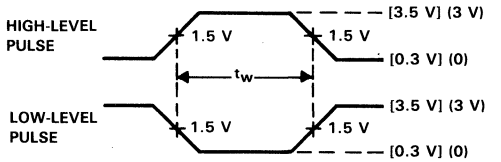
PARAMETER MEASUREMENT INFORMATION



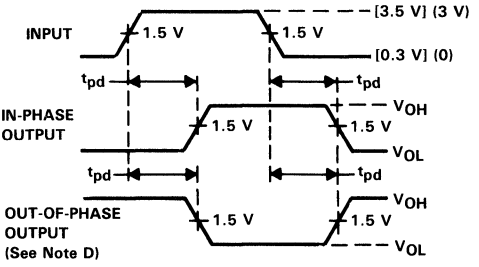
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



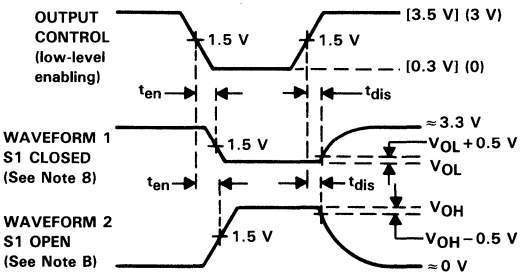
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For M suffix, use the voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 2

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TIBPALR19L8C, TIBPALR19R4C, TIBPALR19R6C, TIBPALR19R8C
HIGH-PERFORMANCE REGISTERED-INPUT *PAL*® CIRCUITS

D2709, DECEMBER 1982—REVISED AUGUST 1989

- High-Performance Operation . . . 30 MHz
- Preload Capability on Output Registers
- DIP Options Include Both 300-mil Plastic and 600-mil Ceramic
- Dependable Texas Instruments Quality and Reliability

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PALR19L8	11	2	2	0	6
'PALR19R4	11	0	0	4 (3-state buffers)	4
'PALR19R6	11	0	0	6 (3-state buffers)	2
'PALR19R8	11	0	0	8 (3-state buffers)	0

description

These programmable array logic devices feature high speed and functionality similar to the TIBPAL16L8, 16R4, 16R6, 16R8 series, but with the added advantage of D-type input registers. If any input register is not desired, it can be converted to an input buffer by simply programming the architectural fuse.

Combining Advanced Low-Power Schottky† technology, with proven titanium-tungsten fuses, these devices will provide reliable high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

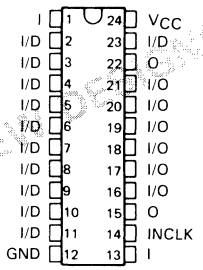
A C suffix designates commercial-temperature circuits that are characterized for operation from 0°C to 70°C.

INPUT REGISTER FUNCTION TABLE

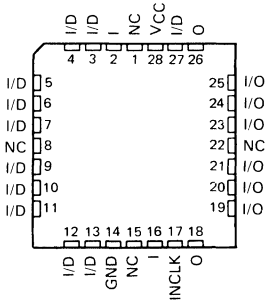
INPUT		OUTPUT OF
INCLK	D	INPUT REGISTER
↑	H	H
↑	L	L
L	X	Q_0

† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
PAL is a registered trademark of Monolithic Memories Inc.

TIBPALR19L8'
JW OR NT PACKAGE
(TOP VIEW)



TIBPALR19L8'
FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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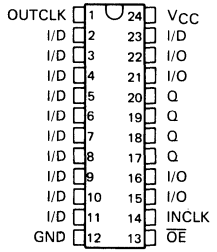
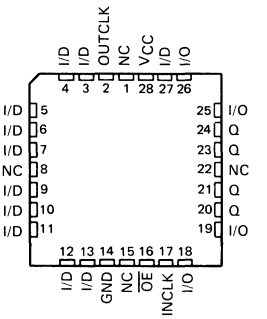
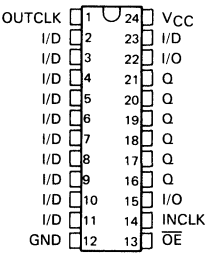
TIBPALR19R4'
JW OR NT PACKAGE
(TOP VIEW)



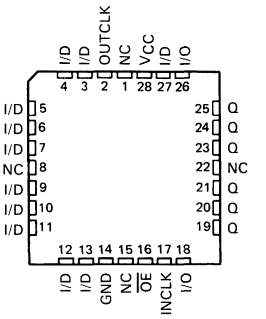
TIBPALR19R4'
FN PACKAGE
(TOP VIEW)



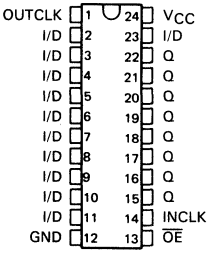
TIBPALR19R6'
JW OR NT PACKAGE
(TOP VIEW)



TIBPALR19R6'
FN PACKAGE
(TOP VIEW)

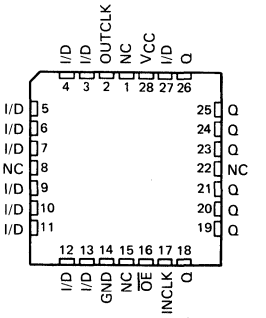


TIBPALR19R8'
JW OR NT PACKAGE
(TOP VIEW)



Pin assignments in operating mode

TIBPALR19R8'
FN PACKAGE
(TOP VIEW)



NC—No internal connection

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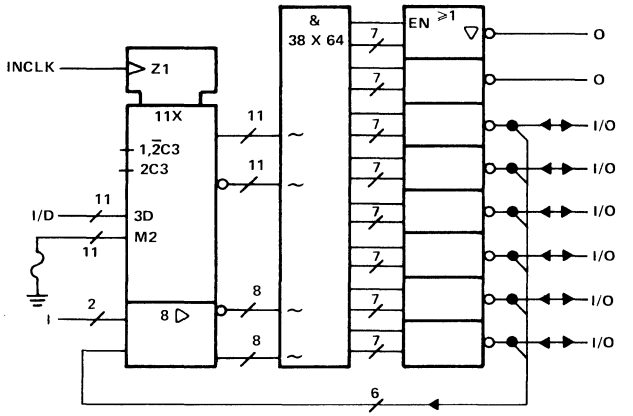
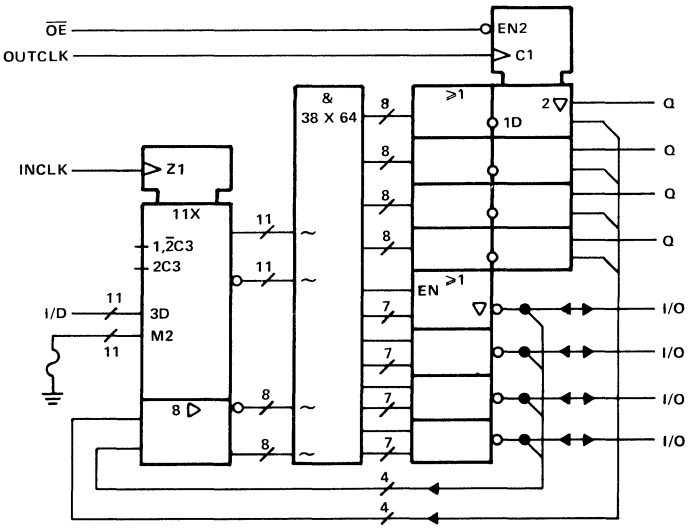
functional block diagrams (positive logic)

'PALR19L8

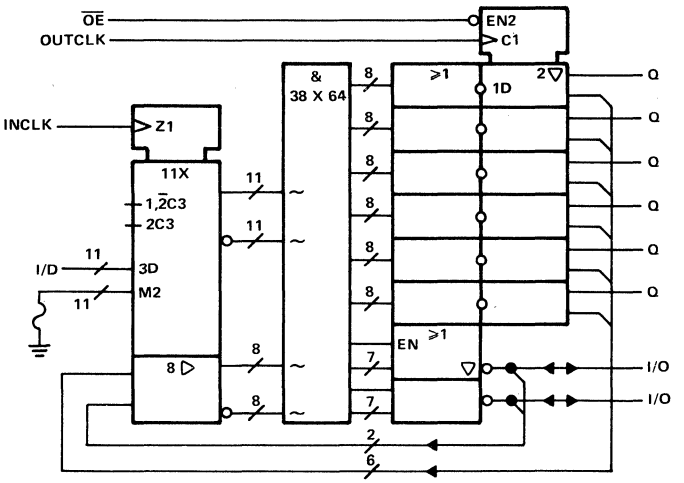


'PALR19R4

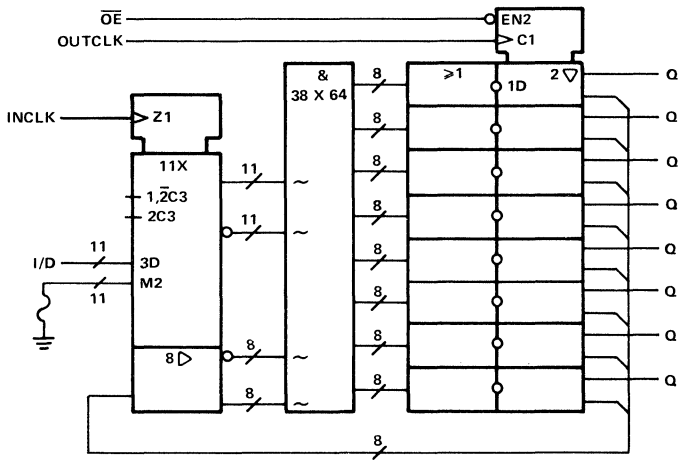


functional block diagrams (positive logic)

'PALR19R6



'PALR19R8



TEXAS INSTRUMENTS
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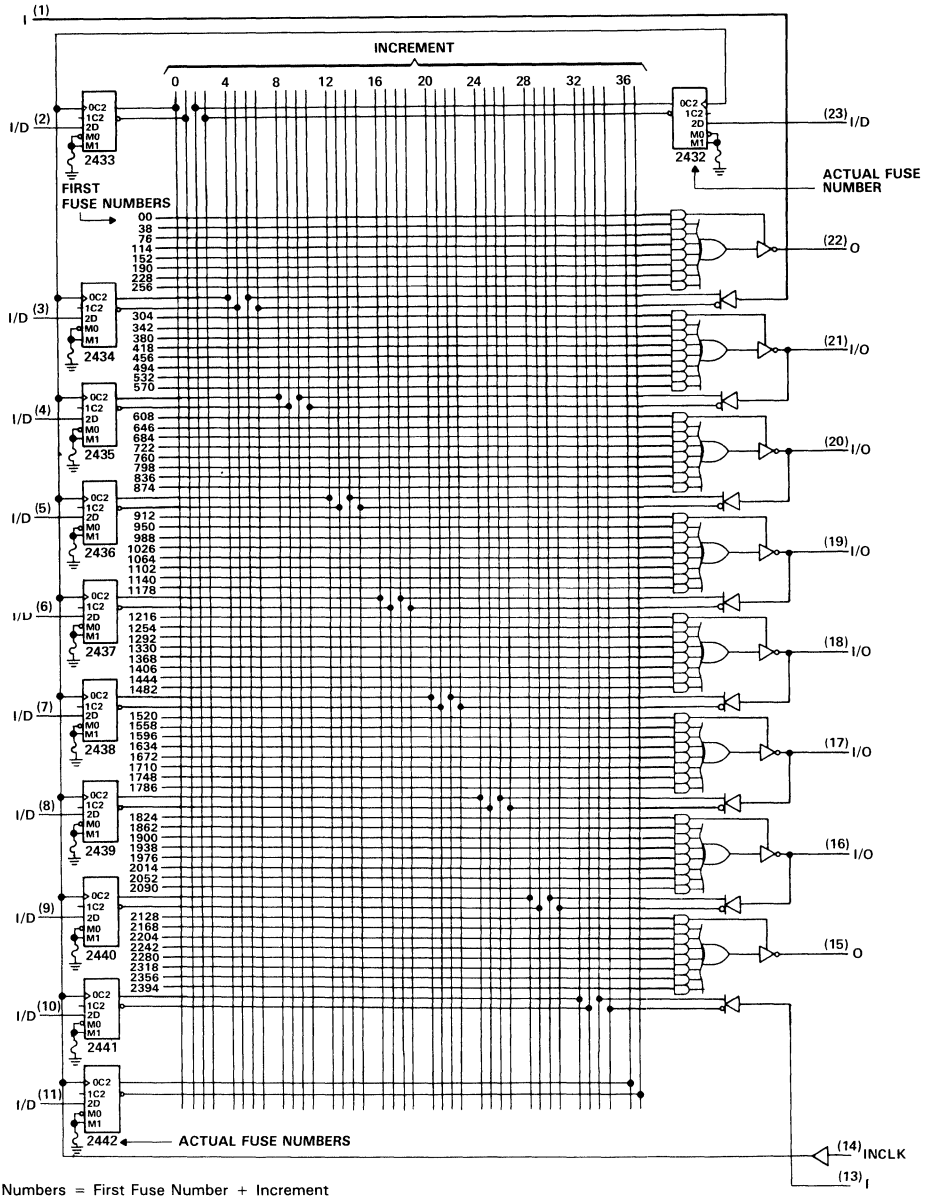
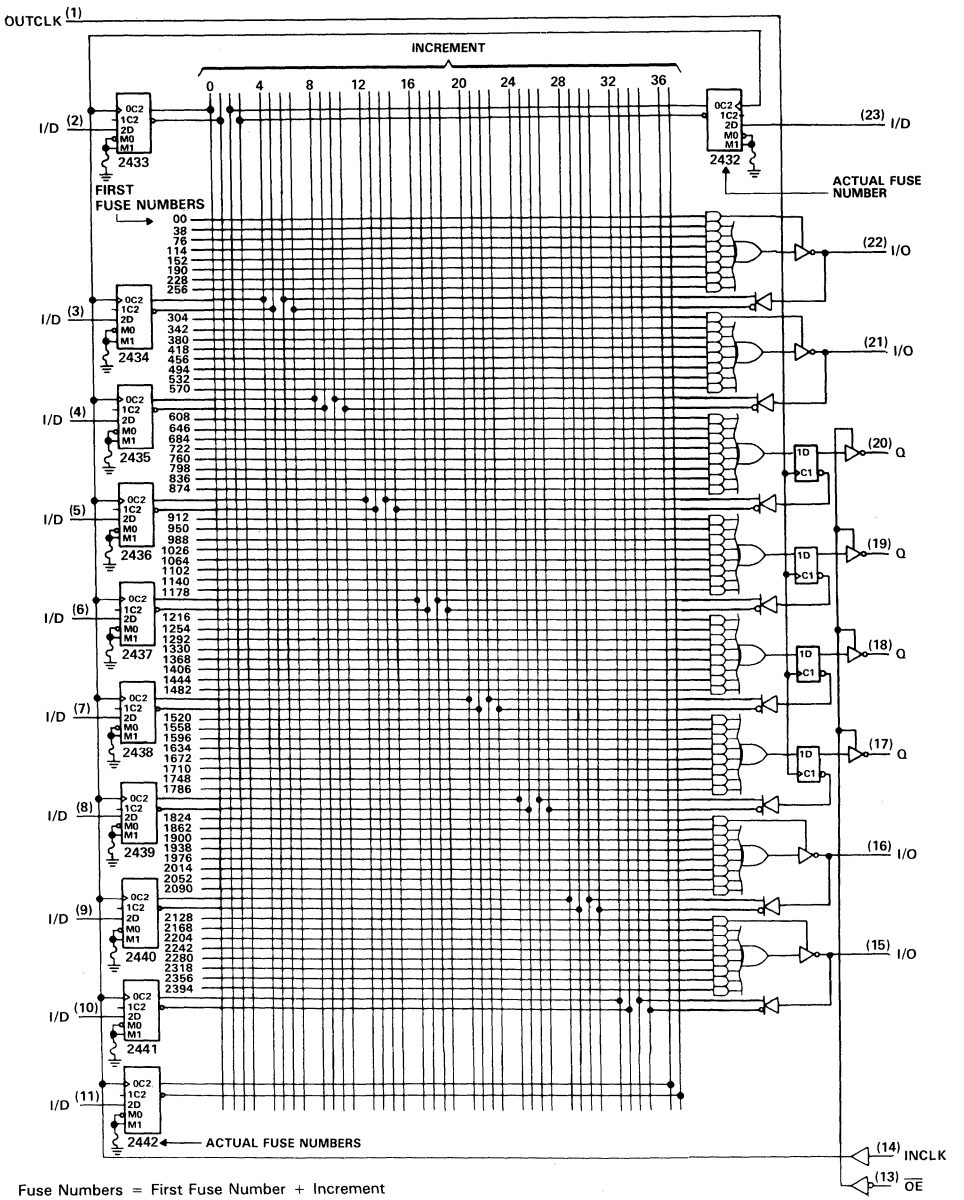
logic diagram (positive logic)



Fuse Numbers = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



Fuse Numbers = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

TEXAS INSTRUMENTS
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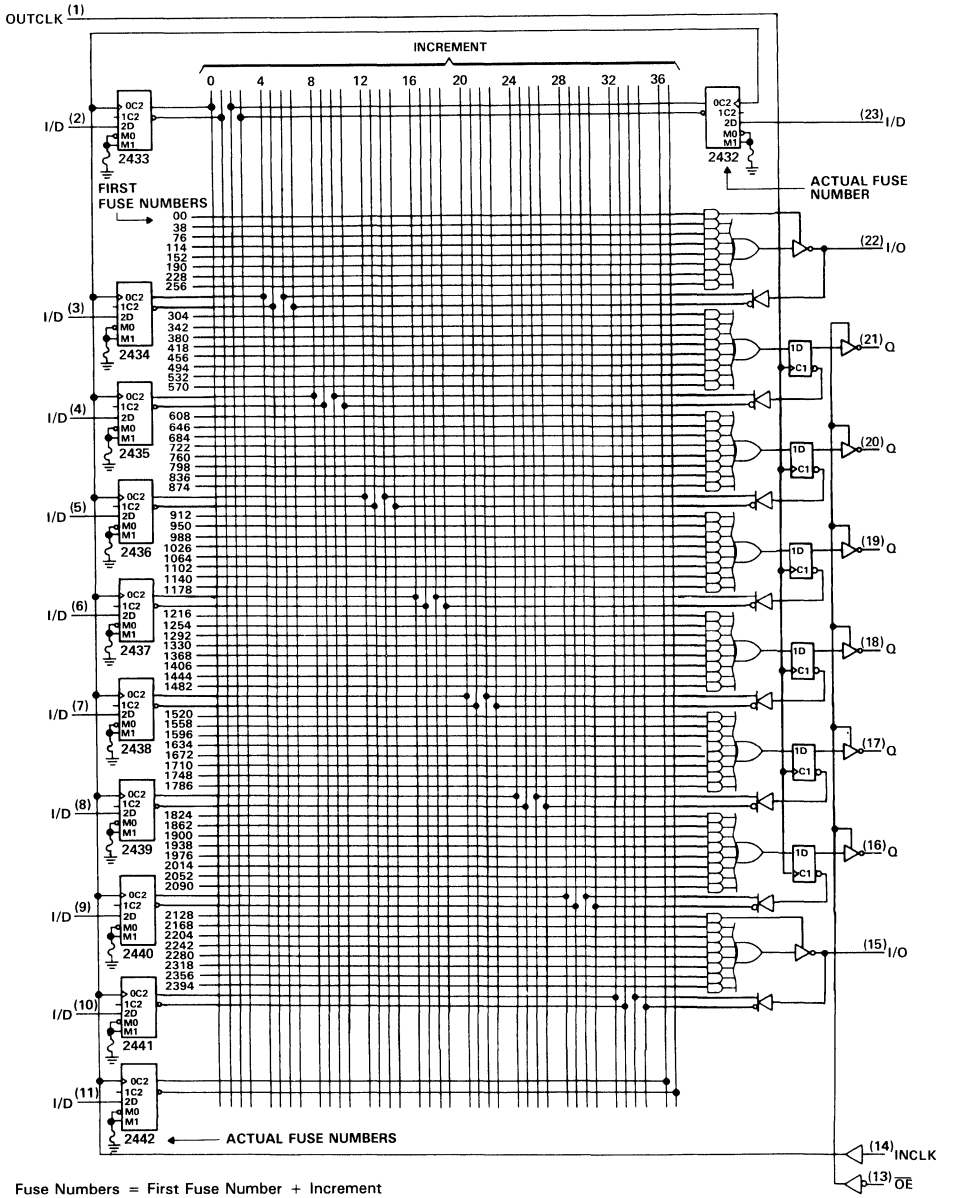
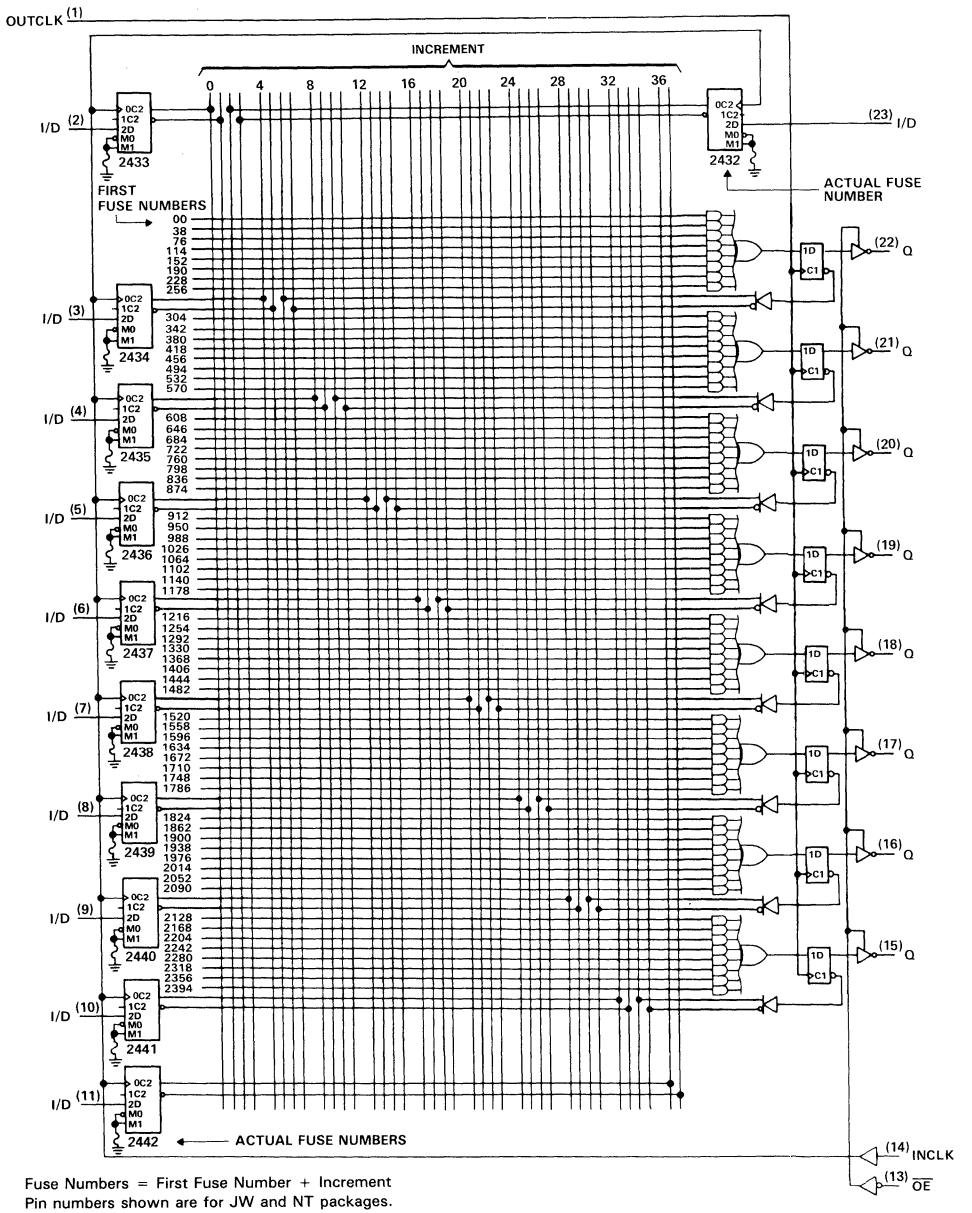
logic diagram (positive logic)



Fuse Numbers = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



Fuse Numbers = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency	INCLK	0		30	MHz
		OUTCLK	0		30	
t_w	Pulse duration, clock	INCLK high	15			ns
		INCLK low	15			
		OUTCLK high	15			
		OUTCLK low	15			
t_{su}	Setup time	Data before INCLK↑	10			ns
		Data before OUTCLK↑	25			
		INCLK↑ before OUTCLK↑ (See Note 2)	25			
t_h	Hold time	Data after INCLK↑	5			ns
		Data after OUTCLK↑	0			
T_A	Operating free-air temperature		0		70	°C

NOTE 2: This setup time ensures the output registers will see stable data from the input registers.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = 5.25 V,	V_{IH} = 2.7 V			20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.25 V,	V_{IH} = 0.4 V			−20	μA
	I/O ports					−250	
I_I	$\overline{OE}$ Input	V_{CC} = 5.25 V,	V_I = 5.5 V			0.2	mA
	I/D Inputs					0.1	
	All others					0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = 5.25 V,	V_I = 2.7 V			40	μA
	I/D Inputs					20	
	All others					20	
I_{IL}	$\overline{OE}$ Input	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.4	mA
	I/D Inputs					−0.6	
	All others					−0.2	
I_O‡		V_{CC} = 5.25 V,	V_O = 2.25 V	−30		−125	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open	V_I = 0 V,		150	210	mA

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
f_{max}	INCLK↑	I/O, O	R1 = 500 Ω, R2 = 500 Ω, C_L = 50 pF, See Figure 1	30			MHz
t_{pd}	I, I/O	I/O, O			15	25	ns
t_{pd}	I/D§	I/O, O			20	35	ns
t_{pd}	INCLK↑	I/O, O			20	35	ns
t_{pd}	OUTCLK↑	Q			10	20	ns
t_{en}	$\overline{OE}$↓	Q			10	20	ns
t_{en}	I, I/O	I/O, O			14	25	ns
t_{en}	I/D§	I/O, O			27	40	ns
t_{en}	INCLK↑	I/O, O			27	40	ns
t_{dis}	$\overline{OE}$↑	Q			11	20	ns
t_{dis}	I, I/O	I/O, O			12	25	ns
t_{dis}	I/D§	I/O, O			13	30	ns
t_{dis}	INCLK↑	I/O, O			13	25	ns

†All typical values are V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.
§Input configured as an input buffer.

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programming information

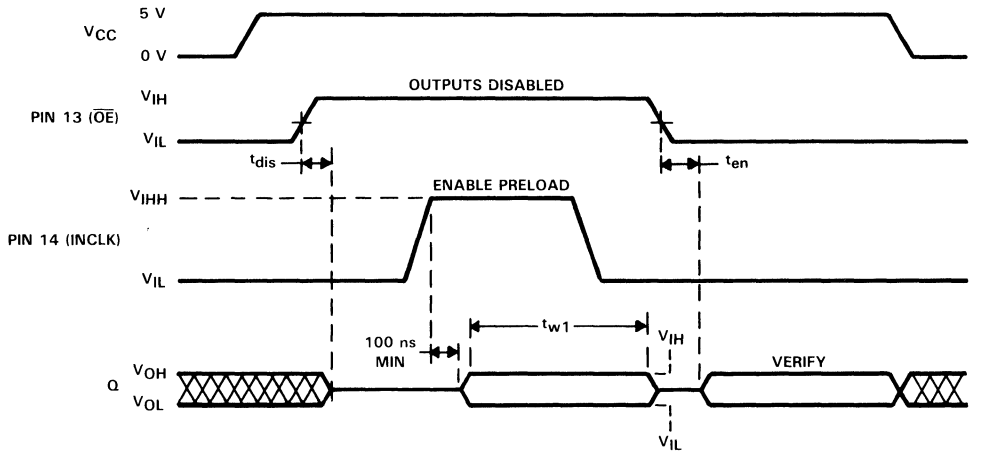
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

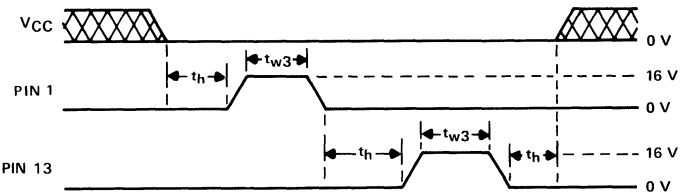
preload procedure for registered outputs (see Note 3)

Step 1 Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2 Pin 14 to V_{IHH}
Step 3 At Q outputs, apply V_{IL} to preload a low and V_{IH} to preload a high.
Step 4 Pin 14 to V_{IL}.
Step 5 Remove the voltages applied to the outputs.
Step 6 Pin 13 to V_{IL}
Step 7 Check the output states to verify preload.

preload waveforms (see Note 3)

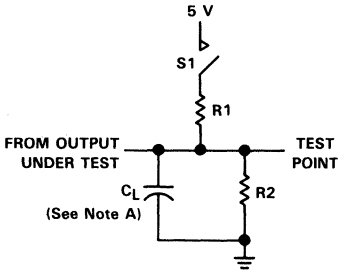


security fuse programming (see Note 3)

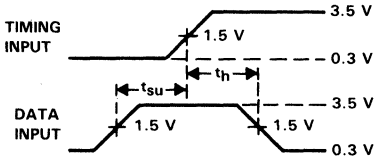


NOTE 3: Pin numbers shown are for JW and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

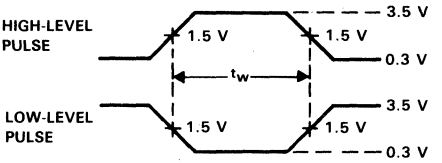
PARAMETER MEASUREMENT INFORMATION



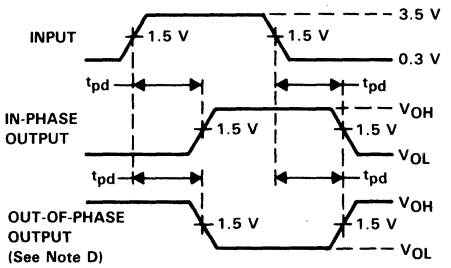
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



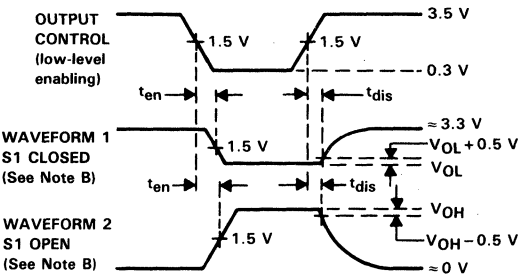
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

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TIBPALT19L8C, TIBPALT19R4C, TIBPALT19R6C, TIBPALT19R8C
HIGH-PERFORMANCE LATCHED-INPUT *PAL*® CIRCUITS

D2709, DECEMBER 1982—REVISED AUGUST 1989

- **High-Performance Operation . . . 30 MHz**
- **Preload Capability on Output Registers**
- **DIP Options Include Both 300-mil Plastic and 600-mil Ceramic**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PALT19L8	11	2	2	0	6
'PALT19R4	11	0	0	4 (3-state buffers)	4
'PALT19R6	11	0	0	6 (3-state buffers)	2
'PALT19R8	11	0	0	8 (3-state buffers)	0

description

These programmable array logic devices feature high speed and functionality similar to the TIBPAL16L8, 16R4, 16R6, 16R8 series, but with the added advantage of D-type transparent latches on the inputs. If any input register is not desired, it can be converted to an input buffer by simply programming the architectural fuse.

Combining Advanced Low-Power Schottky† technology, with proven titanium-tungsten fuses, these devices will provide reliable high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

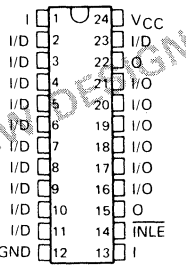
A C suffix designates commercial-temperature circuits that are characterized for operation from 0°C to 70°C.

INPUT LATCH FUNCTION TABLE

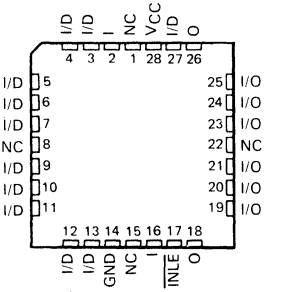
$\overline{INLE}$	D	LATCH OUTPUT
L	L	L
L	H	H
H	X	Q_0

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
PAL is a trademark of Monolithic Memories Inc.

TIBPALT19L8'
JW OR NT PACKAGE
(TOP VIEW)



TIBPALT19L8'
FN PACKAGE
(TOP VIEW)



NC No internal connection

Pin assignments in operating mode

NOT RECOMMENDED FOR NEW DESIGNS

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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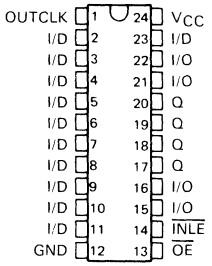
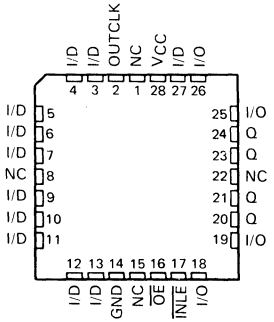
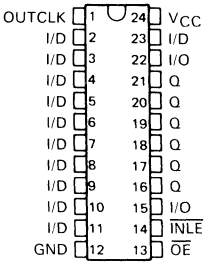
TIBPALT19R4'
JW OR NT PACKAGE
(TOP VIEW)



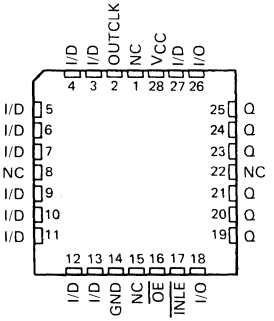
TIBPALT19R4'
FN PACKAGE
(TOP VIEW)



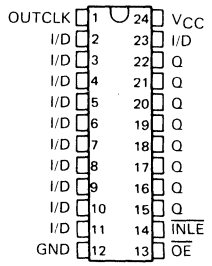
TIBPALT19R6'
JW OR NT PACKAGE
(TOP VIEW)



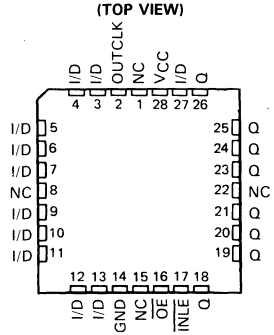
TIBPALT19R6'
FN PACKAGE
(TOP VIEW)



TIBPALT19R8'
JW OR NT PACKAGE
(TOP VIEW)



TIBPALT19R8'
FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

NC—No internal connection

TEXAS INSTRUMENTS
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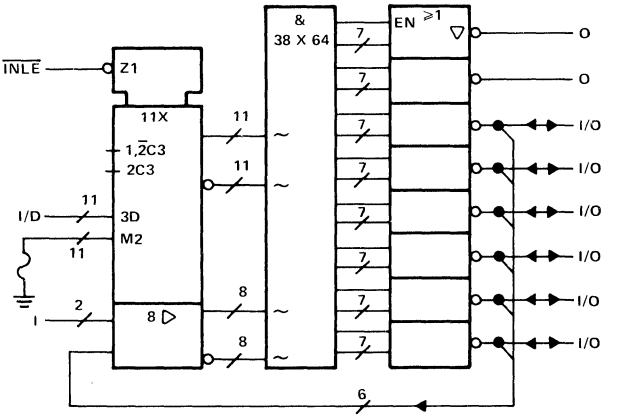
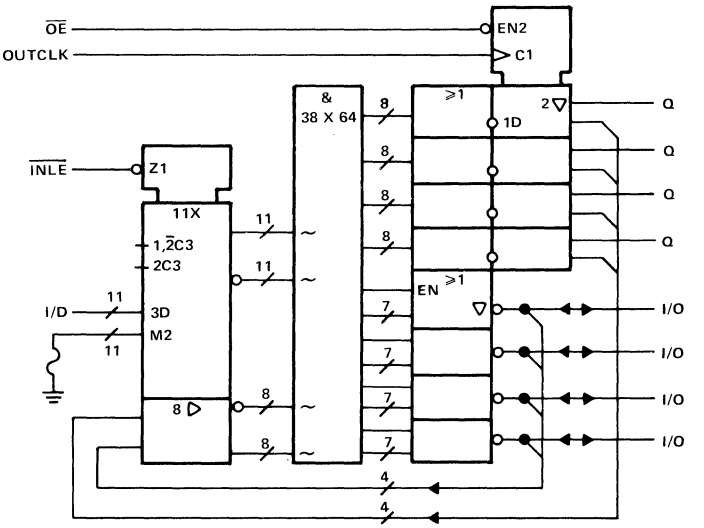
functional block diagrams (positive logic)

'PALT19L8

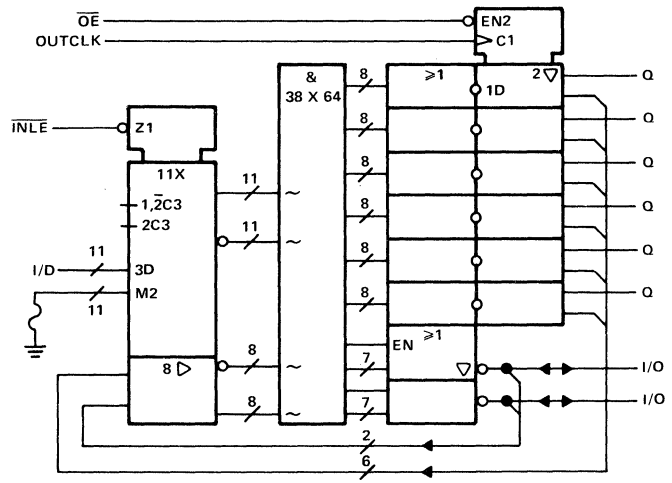


'PALT19R4

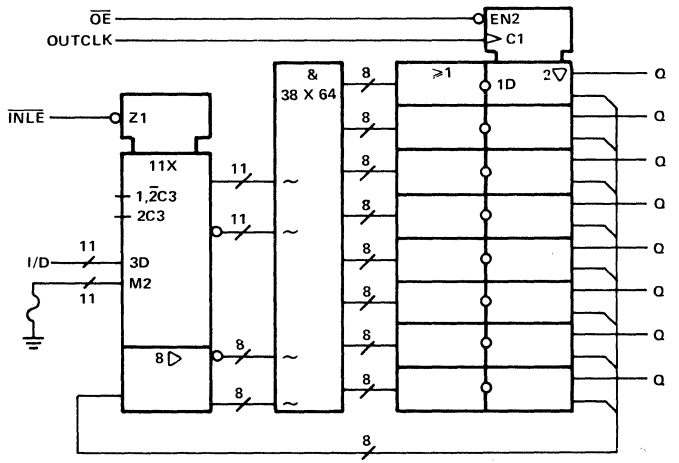


functional block diagrams (positive logic)

'PALT19R6



'PALT19R8



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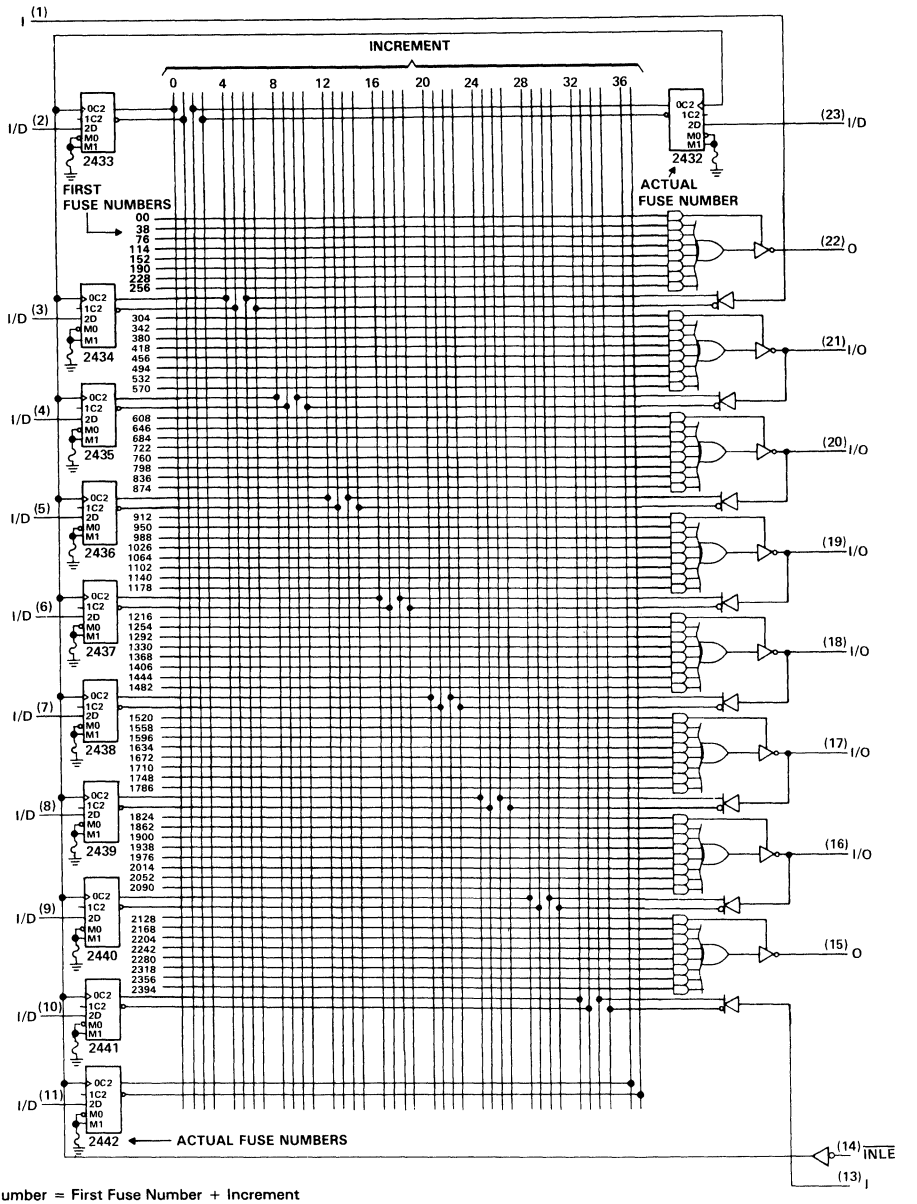
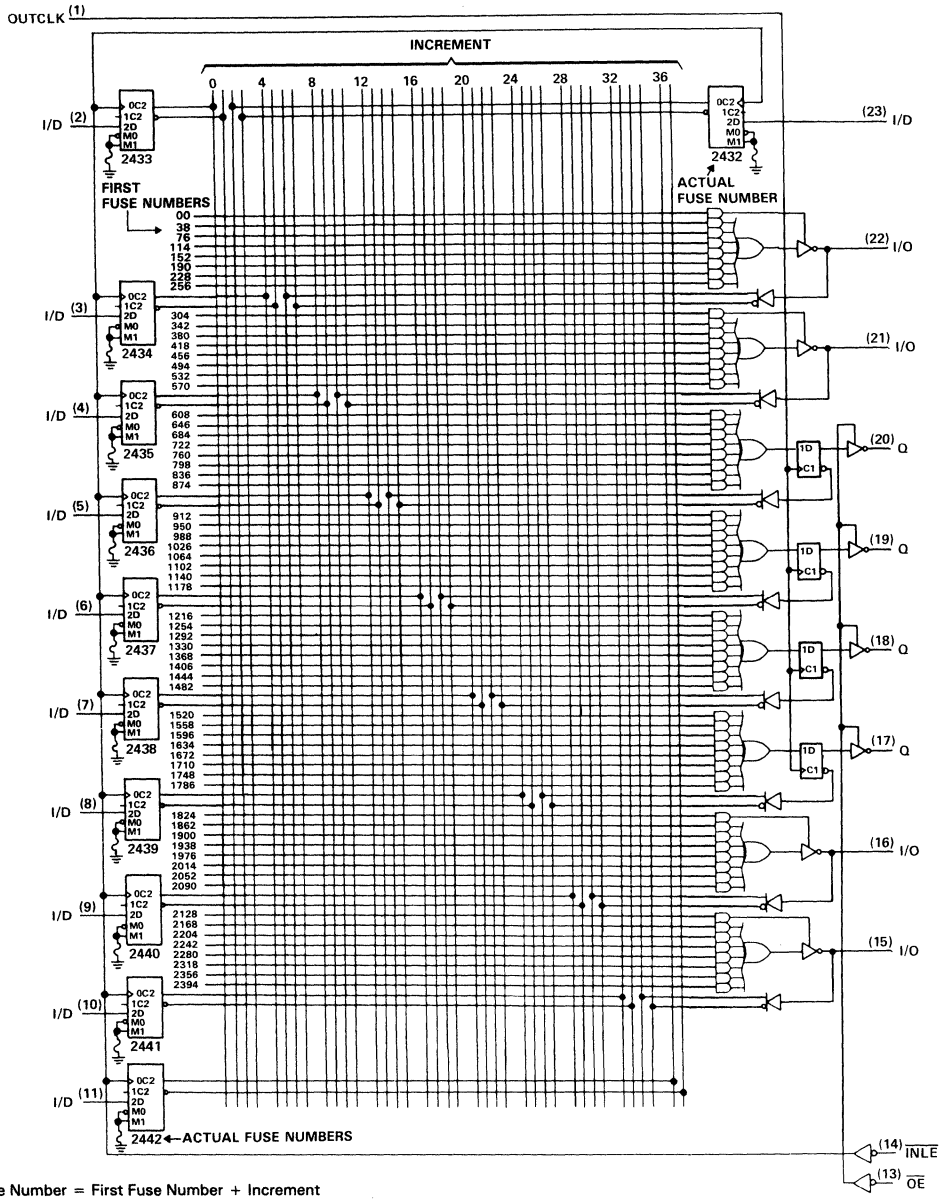
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

TEXAS INSTRUMENTS
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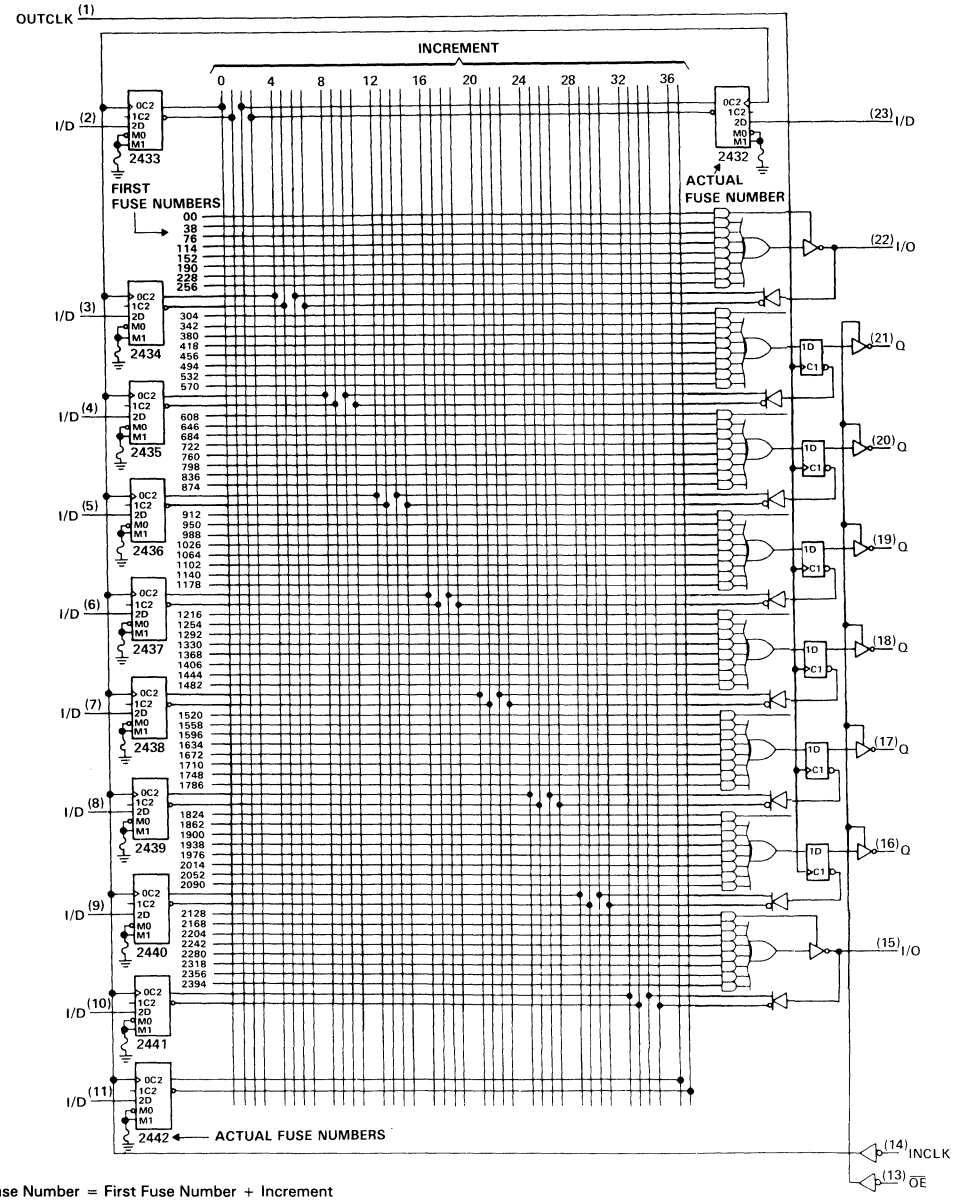
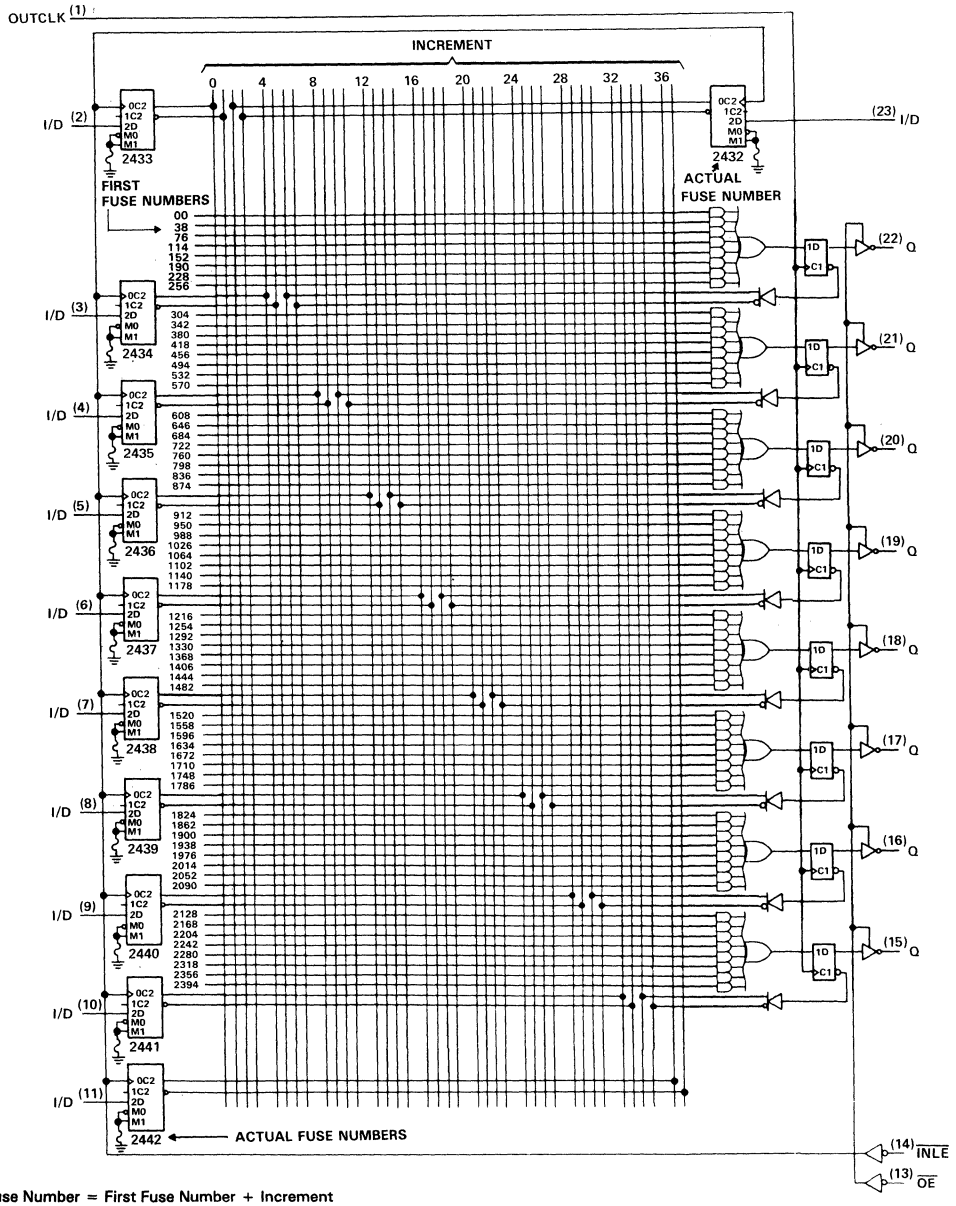
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency	OUTCLK	0		30	MHz
t_w	Pulse duration	$\overline{INLE}$ low	15			ns
		OUTCLK high	15			
		OUTCLK low	15			
t_{su}	Setup time	Data before $\overline{INLE}$ ↑	10			ns
		Data before OUTCLK↑	25			
		$\overline{INLE}$ low before OUTCLK↑ (See Note 2)	30			
t_h	Hold time	Data after $\overline{INLE}$ ↑	5			ns
		Data after OUTCLK↑	0			
T_A	Operating free-air temperature		0		70	°C

NOTE 2: This setup time ensures the output registers will see stable data from the input latches.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = 5.25 V,	V_{IH} = 2.7 V			20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.25 V,	V_{IH} = 0.4 V			−20	μA
	I/O ports					−250	
I_I	$\overline{OE}$ Input	V_{CC} = 5.25 V,	V_I = 5.5 V			0.2	mA
	All others					0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = 5.25 V,	V_I = 2.7 V			40	μA
	All others					20	
I_{IL}	$\overline{OE}$ Input	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.4	mA
	All others					−0.2	
I_O‡		V_{CC} = 5.25 V,	V_O = 2.25 V	−30		−125	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open	V_I = 0 V,		150	210	mA

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}	OUTCLK↑	Q	R1 = 500 Ω, R2 = 500 Ω, C_L = 50 pF, See Figure 1	30			MHz
t_{pd}	I, I/O	I/O, O			15	25	ns
t_{pd}	I/D§	I/O, O			25	40	ns
t_{pd}	$\overline{INLE}$↓	I/O, O			28	40	ns
t_{pd}	OUTCLK↑	Q			10	20	ns
t_{en}	$\overline{OE}$↓	Q			10	20	ns
t_{en}	I, I/O	I/O, O			14	25	ns
t_{en}	I/D§	I/O, O			30	40	ns
t_{en}	$\overline{INLE}$↓	I/O, O			30	40	ns
t_{dis}	$\overline{OE}$↑	Q			11	20	ns
t_{dis}	I, I/O	I/O, O			12	25	ns
t_{dis}	I/D§	I/O, O			14	25	ns
t_{dis}	$\overline{INLE}$↓	I/O, O			14	25	ns

† All typical values are V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.
§ Input configured as an input buffer or $\overline{INLE}$ low.

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programming information

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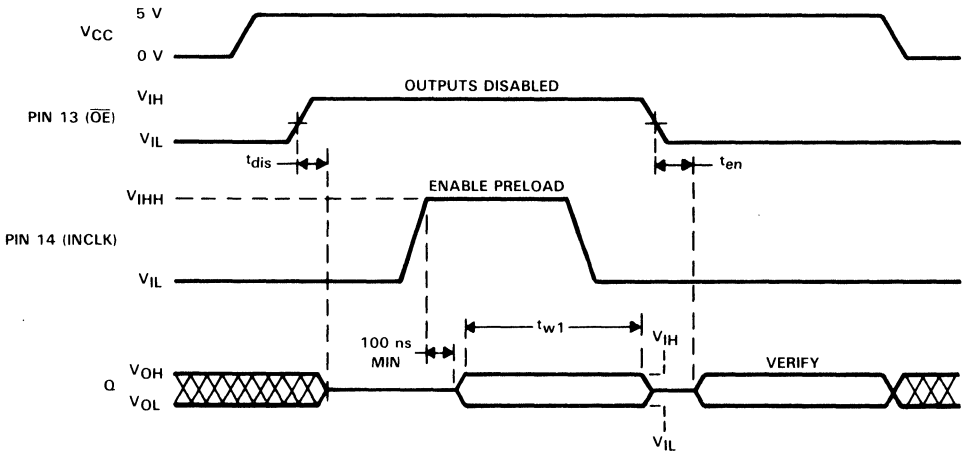
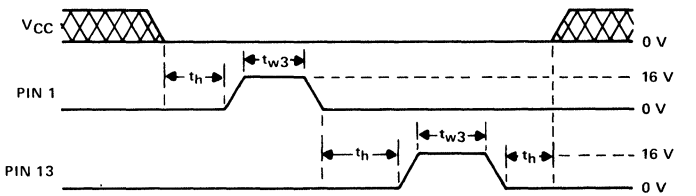
preload procedure for registered outputs (see Note 3)

Step 1 Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2 Pin 14 to V_{IHH}
Step 3 At Q outputs, apply V_{IL} to preload a low and V_{IH} to preload a high.
Step 4 Pin 14 to V_{IL}.
Step 5 Remove the voltages applied to the outputs.
Step 6 Pin 13 to V_{IL}
Step 7 Check the output states to verify preload.

preload waveforms (see Note 3)

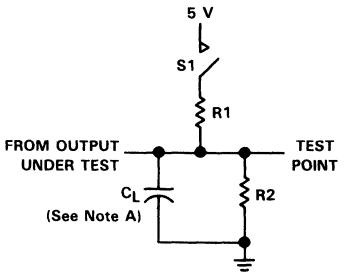


security fuse programming (see Note 3)

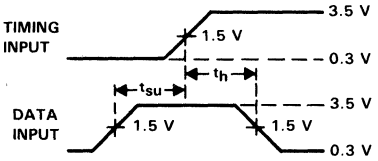


NOTE 3: Pin numbers shown are for JW and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

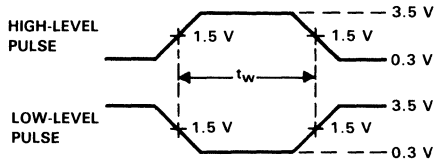
PARAMETER MEASUREMENT INFORMATION



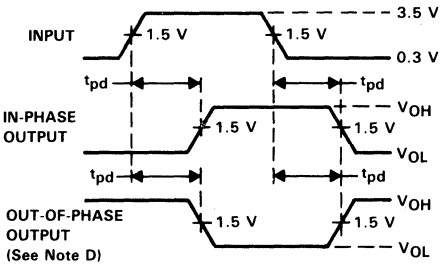
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



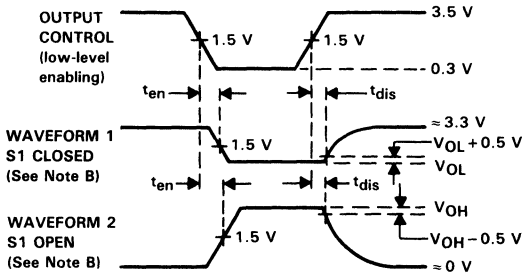
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

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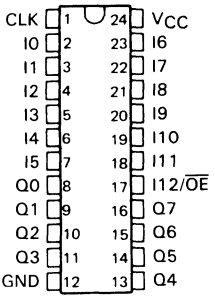
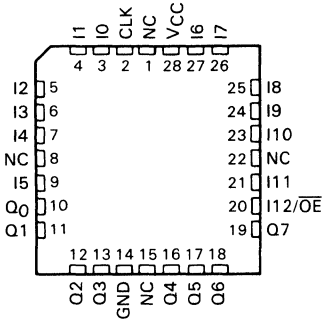
D3090, DECEMBER 1987—REVISED NOVEMBER 1989

- **50-MHz Max Clock Rate**
- **2 Transition Complement Array Terms**
- **16-Bit Internal State Registers**
- **8-Bit Output Registers**
- **Outputs Programmable for Registered or Combinational Operation**
- **Ideal for Waveform Generation and High-Performance State Machine Applications**
- **Programmable Output Enable**
- **Programmable Clock Polarity**

JT OR NT PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TIBPLS506 is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 97 product terms (AND terms) and 48 sum terms (OR terms). The product and sum terms are used to control the 16-bit internal state registers and the 8-bit output registers.

The outputs of the internal state registers (P0-P15) are fed back and combined with the 13 inputs (I0-I12) to form the AND array. In addition, two sum terms are complemented and fed back to the AND array, which allows any product terms to be summed, complemented, and used as inputs to the AND array.

The eight output cells can be individually programmed for registered or combinational operation. Nonregistered operation is selected by blowing the output multiplexer fuse. Registered output operation is selected by leaving the output multiplexer fuse intact.

Pin 17 can be programmed to function as an input and/or an output enable. Blowing the output enable fuse lets pin 17 function as an output enable but does not disconnect pin 17 from the input array. When the output enable fuse is intact, pin 17 functions only as an input with the outputs being permanently enabled.

The state and output registers are synchronously clocked by the fuse programmable clock input. The clock polarity fuse selects either postive- or negative-edge triggering. Negative-edge triggering is selected by blowing the clock polarity fuse. Leaving this fuse intact selects positive-edge triggering. After power-up, the device must be initialized to the desired state. When the output multiplexer fuse is left intact, registered operation is selected.

The TIBPLS506C is characterized for operation from 0°C to 75°C.

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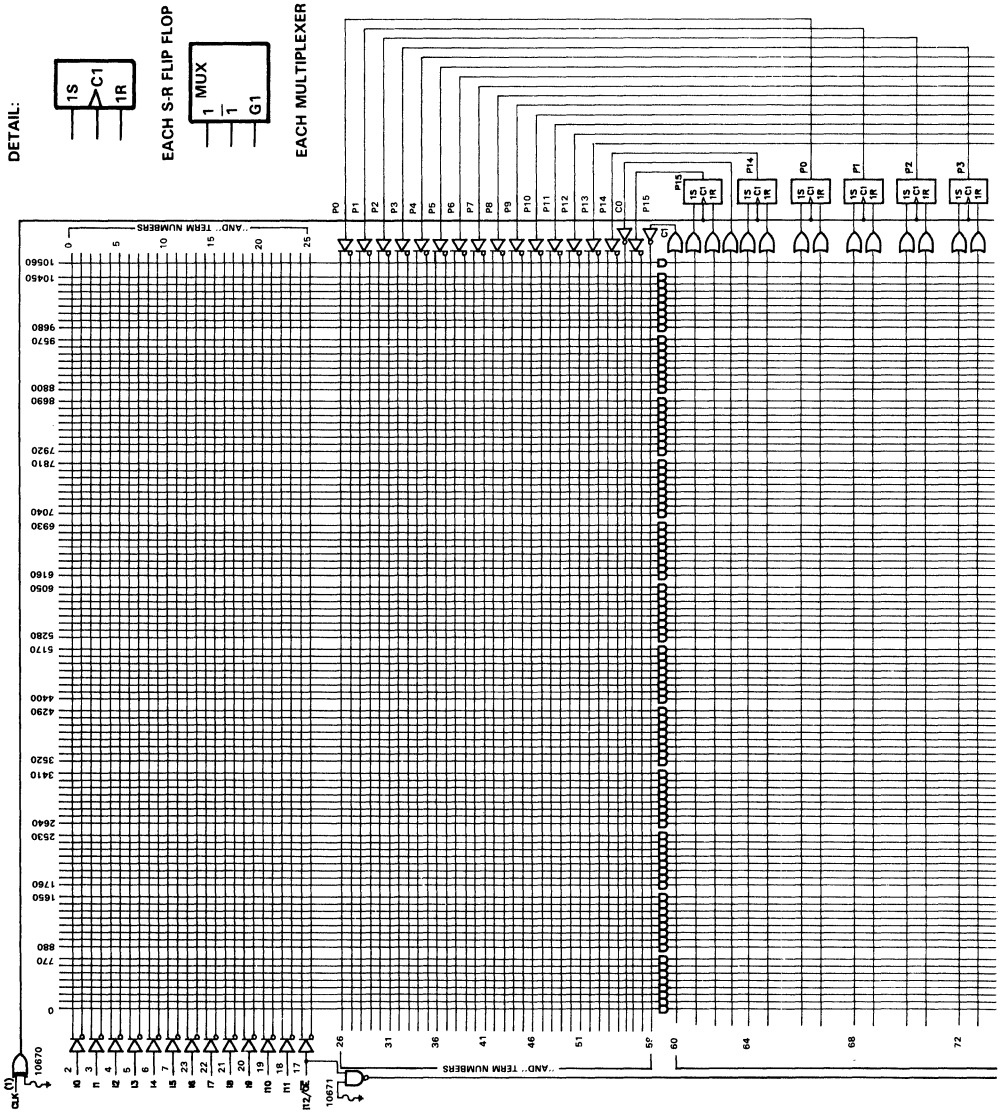
logic diagram (positive logic)



NOTES: A. All inputs to AND gates, exclusive-OR gates, and multiplexters with a blown link assume the logic-1 state.
B. All OR gate inputs with a blown link assume the logic-0 state.

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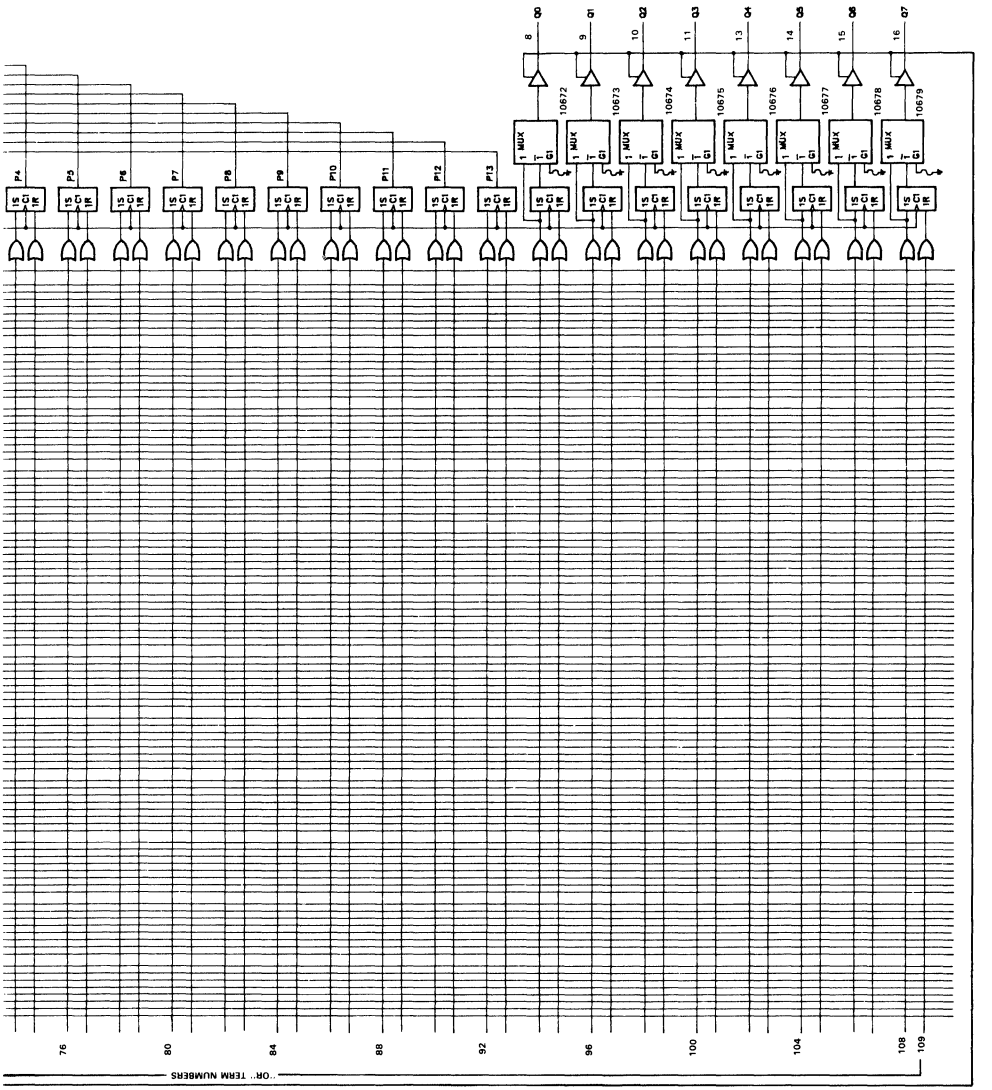
logic diagram (continued)

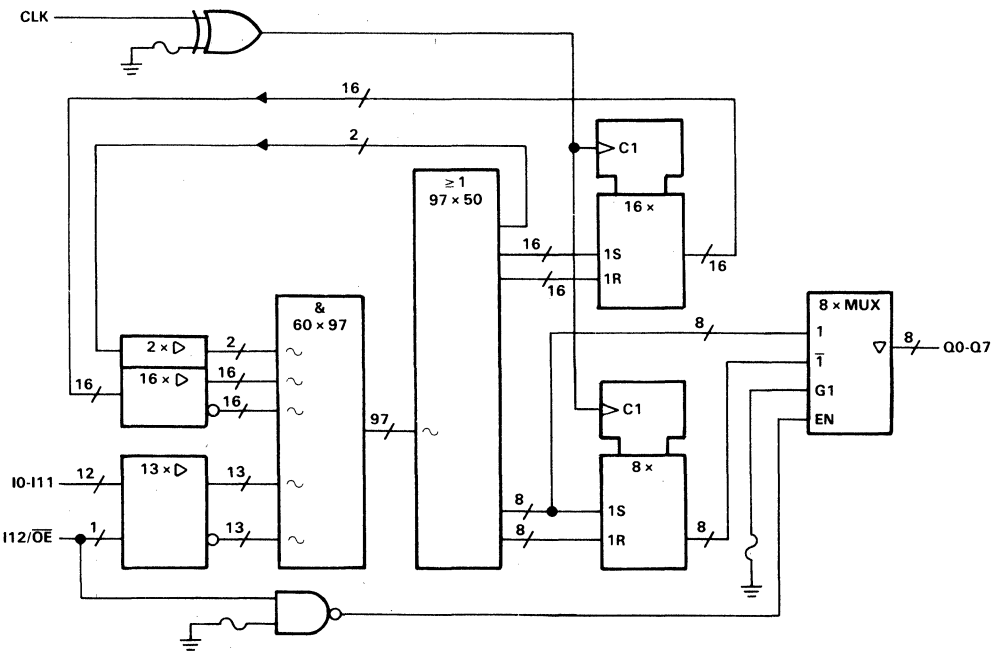


S-R FUNCTION TABLE (see Note 1)

CLK POLARITY FUSE	CLK	S	R	STATE REGISTER
INTACT	↑	L	L	Q_0
INTACT	↑	L	H	L
INTACT	↑	H	L	H
INTACT	↑	H	H	INDETERMINATE
BLOWN	↓	L	L	Q_0
BLOWN	↓	L	H	L
BLOWN	↓	H	L	H
BLOWN	↓	H	H	INDETERMINATE

NOTE 1: Q_0 is the state of the S-R registers before the active clock edge.

functional block diagram (positive logic)



∿ denotes fused inputs.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 2) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Voltage applied to disabled output (see Note 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 2: These ratings apply except when programming pins during a programming cycle or during diagnostic testing.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage, V_{CC} = 5.25 V		2		5.5	V
V_{IL}	Low-level input voltage, V_{CC} = 4.75 V				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high	6			ns
		Clock low	6			
t_{su}	Setup time before CLK† input or feedback to S-R inputs	Without C-array	15			ns
		With C-array	25			
t_h	Hold time after CLK	Input or feedback at S-R inputs	0			ns
T_A	Operating free-air temperature		0		75	°C

†The active edge of CLK is determined by the programmed state of CLK polarity fuse.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.75 V, I_{OH} = −3.2 mA		2.4	3		V
V_{OL}	V_{CC} = 4.75 V, I_{OL} = 16 mA			0.37	0.5	V
I_I	V_{CC} = 5.25 V, V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.25 V, V_I = 2.7 V				20	μA
I_{IL}	V_{CC} = 5.25 V, V_I = 0.4 V				−0.25	mA
I_O§	V_{CC} = 5.25 V, V_O = 0.5 V		−30		−130	mA
I_{OZH}	V_{CC} = 5.25 V, V_O = 2.7 V				20	μA
I_{OZL}	V_{CC} = 5.25 V, V_O = 0.4 V				−20	μA
I_{CC}	V_{CC} = 5.25 V, See Note 3,	Outputs open		156	210	mA
C_i	f = 1 MHz, V_I = 2 V			7		pF
C_o	f = 1 MHz, V_O = 2 V			11		pF
C_{clk}	f = 1 MHz, V_I = 2 V			14		pF

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 3: When the clock is programmed for negative-edge, then V_I = 4.75 V. When the clock is programmed for positive-edge, then V_I = 0.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}‡		Without C-array	R_1 = 300 Ω, R_2 = 390 Ω, See Figure 3	50	65		MHz
		With C-array		33	50		
t_{pd}§	CLK↑	Q (nonregistered)		8		27	ns
	CLK↓			9		28	
t_{pd}§	CLK↑	Q (registered)		3		10	ns
	CLK↓			4		11	
t_{pd}	I or Feedback	Q (nonregistered)		10		22	ns
t_{en}	OE↓	Q	C_L = 5 pF	2	6	10	ns
t_{dis}	OE↑	Q		2	6	10	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡f_{max}, with external feedback, can be calculated as $\frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$. f_{max} is independent of the internal programmed configuration and the number of product terms used.

§The active edge of CLK is determined by the programmed state of the CLK polarity fuse.

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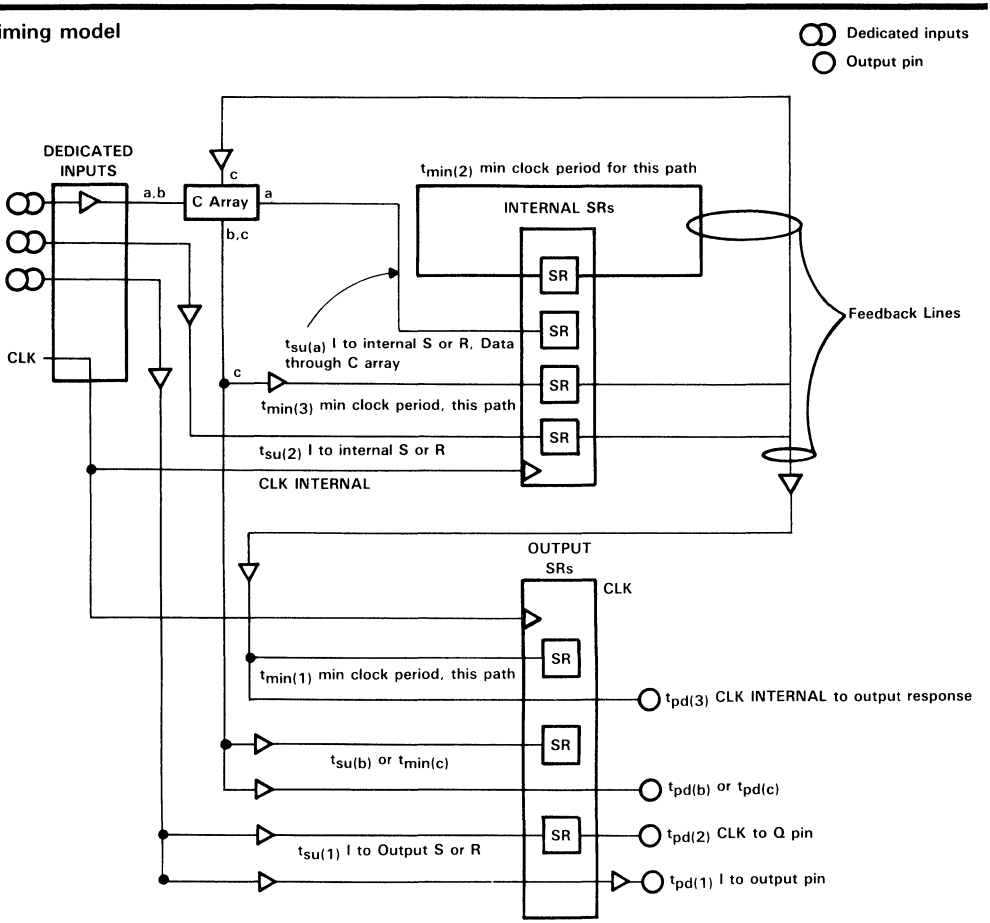
timing model



glossary—timing model

$t_{pd(1)}$ — Maximum time interval from the time a signal edge is received at any input pin to the time any logically affected combinational output pin delivers a response.

$t_{pd(2)}$* — Maximum time interval from a positive edge on the clock input pin to data delivery on the output pin corresponding to any output SR register.

$t_{pd(3)}$* — Maximum time interval from the positive edge on the clock input pin to the response on any logically affected combinationally configured output (at the pin), where data origin is any internal SR register.

$t_{pd(b)}$ — Maximum time interval from the time a signal edge is received at any input pin to the time any logically affected combinational output pin delivers a response, where data passes through a **C ARRAY** once before reaching the affected output.

$t_{pd(c)}$* — Maximum time interval from the positive edge on the clock input pin to the response on any logically affected combinationally configured output (at the pin), where data origin is any internal SR register and data passes once through a **C ARRAY** before reaching an affected output.

$t_{su(1)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the **active** clock edge on the clock input pin when data affects the S or R line of any output SR register.

$t_{su(2)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the **active** clock edge on the clock input pin when data affects the S or R line of any internal SR register.

$t_{su(a)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the **active** clock edge on the clock input pin when data passes once through a C ARRAY before reaching an affected S or R line on any internal SR register.

$t_{su(b)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the **active** clock edge on the clock input pin when data passes once through a C ARRAY before reaching an affected S or R line on any output SR register.

$t_{min(1)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accomodate when using feedback from any internal SR register or counter bit to feed the S or R line of any output SR register.

$t_{min(2)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accomodate when using feedback from any internal SR register to feed the S or R line of any internal SR register.

$t_{min(3)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accomodate when using feedback from any internal SR register to feed the S or R line of any internal SR register and data passes once through a C ARRAY before reaching an affected S or R line on any internal SR register.

$t_{min(c)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accomodate when using feedback from any internal SR register to feed the S or R line of any output SR register and data passes once through a C ARRAY before reaching an affected S or R line on any output SR register.

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PARAMETER VALUES FOR TIMING MODEL

$t_{pd(1)}$ = 22 ns	$t_{su(1)}$ = 15 ns	$t_{min(1)}$ = 20 ns
$t_{pd(2)}$* = 10 ns	$t_{su(2)}$ = 15 ns	$t_{min(2)}$ = 20 ns
$t_{pd(3)}$* = 27 ns	$t_{su(a)}$ = 25 ns	$t_{min(3)}$ = 25 ns
	$t_{su(b)}$ = 25 ns	$t_{min(c)}$ = 25 ns

INTERNAL NODE NUMBERS

Q0-Q7	RESET 25-32	P0-P15	SET 33-48
C0	65		RESET 49-64
C1	66		

diagnostics

A diagnostic mode is provided with these devices that allows the user to inspect the contents of the state registers. The step-by-step procedures required to use the diagnostics follow.

1. Disable all outputs by taking pin 17 ($\overline{OE}$) high (see Note 4).
2. Take pin 8 (Q0) double high to enable the diagnostics test sequence.
3. Apply appropriate levels of voltage to pins 11 (Q3), 13 (Q4), and 14 (Q5) to select the desired state register (see Table 1).

The voltage level monitored on pin 9 will indicate the state of the selected state register.

NOTE 4: If pin 17 is being used as an input to the array, then pin 7 (I5) must be taken double high before pin 17 is taken high.

diagnostics waveforms

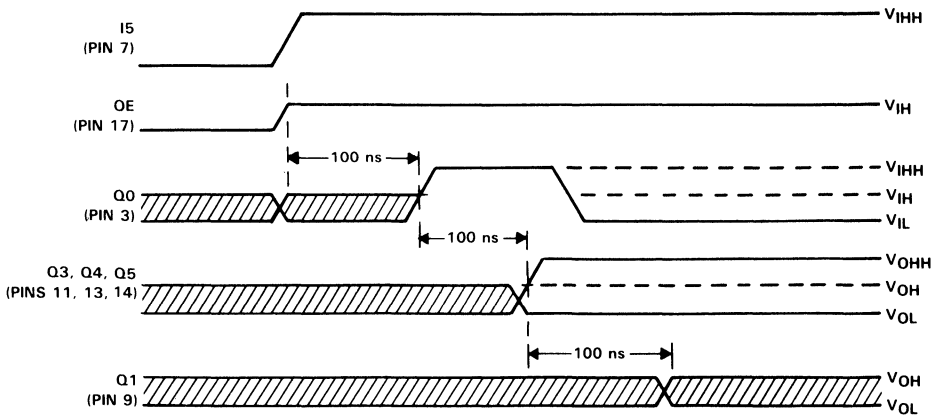

TABLE 1. ADDRESSING STATE REGISTERS DURING DIAGNOSTICS†

REGISTER BINARY ADDRESS			BURIED REGISTER
PIN 11	PIN 13	PIN 14	SELECTED
L	L	L	C1
L	L	H	P15
L	L	HH	C0
L	H	L	P14
L	H	H	P0
L	H	HH	P1
L	HH	L	P2
L	HH	H	P3
L	HH	HH	P4
H	L	L	P5
H	L	H	P6
H	L	HH	P7
H	H	L	P8
H	H	H	P9
H	H	HH	P10
H	HH	L	P11
H	HH	H	P12
H	HH	HH	P13

†V_{IHH} = 10.25 V min, 10.5 V nom, 10.75 V max

programming information

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Complete programming specifications, algorithms, and the latest information on firmware, software, and hardware updates are available upon request. Information on programmers that are capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI sales office, local authorized Texas Instruments distirbutor, or by calling Texas Instruments at (214) 997-5666.

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TYPICAL APPLICATIONS

f_{max}

When the TIBPLS506 is used with two or more devices linked to build a "multi-device" state machine (see Figure 1), the maximum operating frequency for this state machine is limited to the sum of t_{pd} CLK-Q (10 ns) of the first '506 and t_{su} (15 ns), of the second '506, for a clock period of 25 ns. This results in an f_{max} of 40 MHz (1/25 ns).

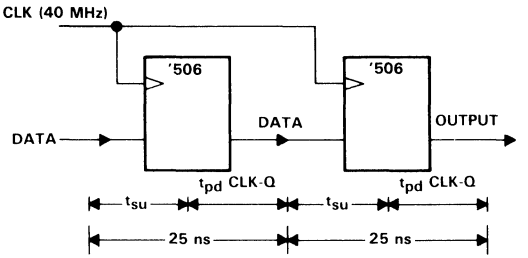
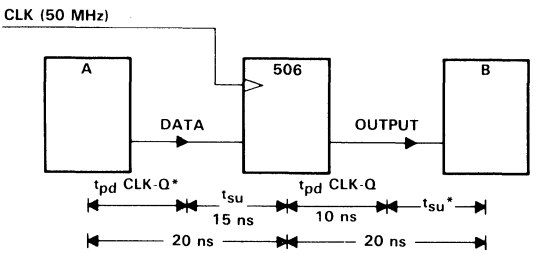


FIGURE 1

Figure 2 shows the '506 used in a system environment where it is operated at 50 MHz, the highest clock rate possible without compromising data integrity. At the input of the '506, the system clock period is limited to the sum of t_{pd} CLK-Q of device A and t_{su} of the '506. At the output of the '506, the system clock period is limited to the sum of t_{pd} CLK-Q of the '506 and t_{su} of device B.

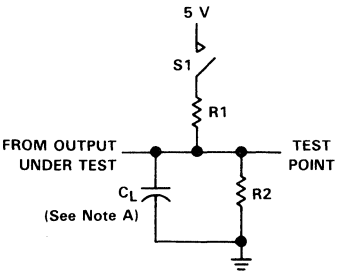
For this system to operate at 50 MHz, a system clock period of 20 ns must be met. Given that t_{su} for the '506 is 15 ns minimum, t_{pd} CLK-Q of device A cannot exceed 5 ns (15 ns + 5 ns = 20 ns). On the output side of the '506, t_{pd} CLK-Q of 10 ns must be allowed. In order to meet the system clock period of 20 ns, t_{su} for device B must not exceed 10 ns (10 ns + 10 ns) = 20 ns). Under these circumstances, a system frequency of 50 MHz (1/20 ns) can be realized.



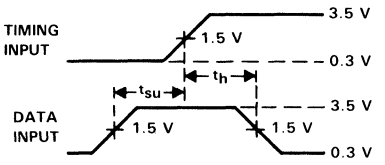
*External device parameters (t_{pd} CLK-Q of device A ≤ 5 ns, and t_{su} of device B ≤ 10 ns)

FIGURE 2

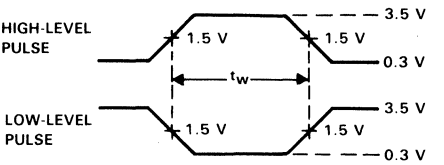
PARAMETER MEASUREMENT INFORMATION



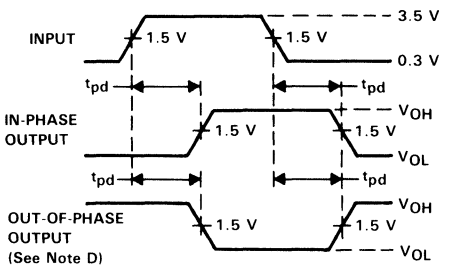
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



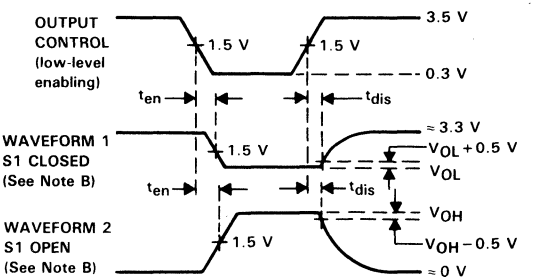
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 3

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

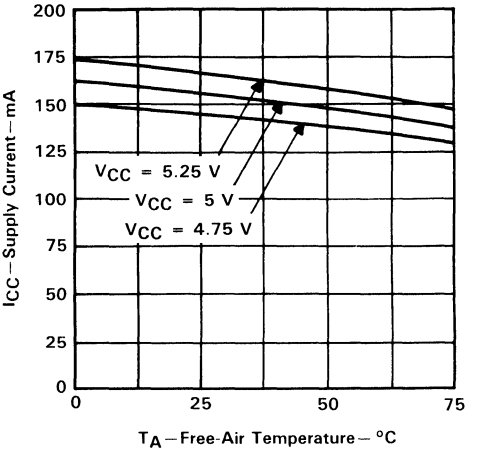

FIGURE 4

POWER DISSIPATION
vs
FREQUENCY

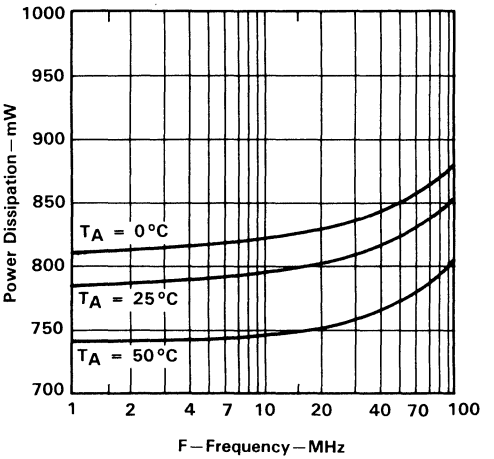

FIGURE 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

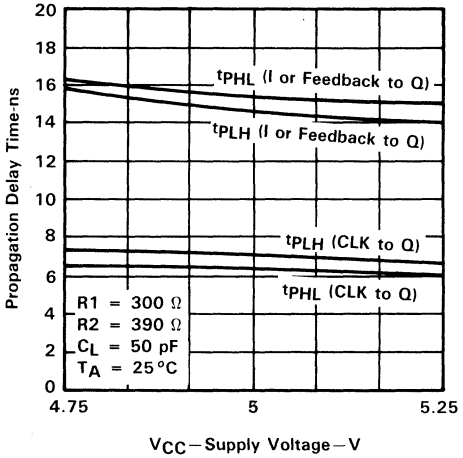

FIGURE 6

PROPAGATION DELAY
vs
LOAD CAPACITANCE

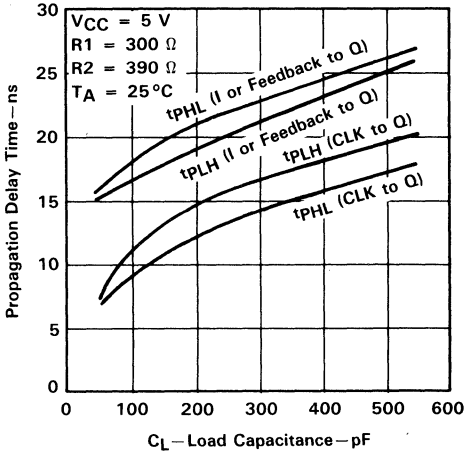

FIGURE 7

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

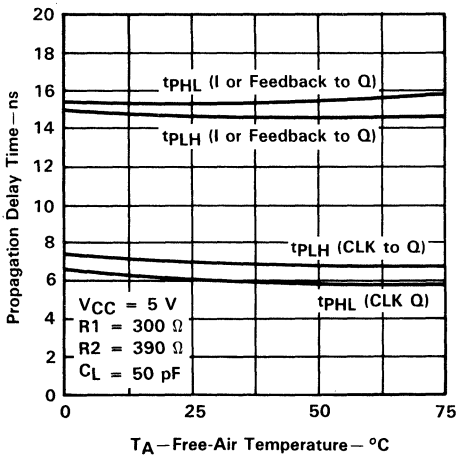

FIGURE 8

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

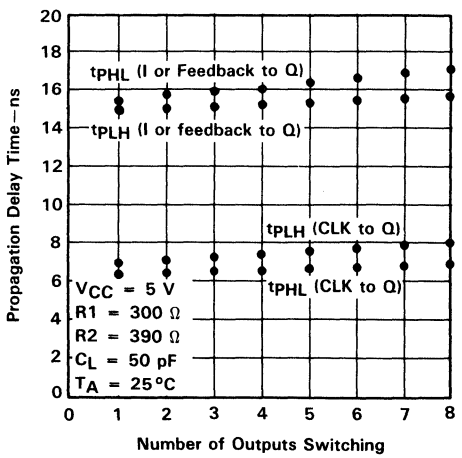

FIGURE 9

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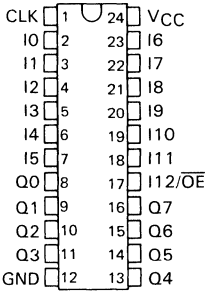
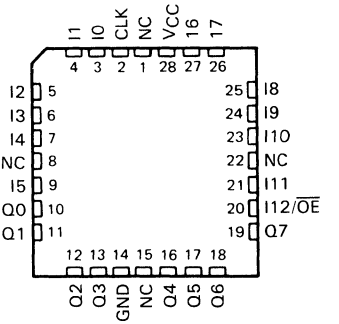
D3029, MAY 1987 – REVISED NOVEMBER 1989

- **58-MHz Max Clock Rate**
- **Ideal for Waveform Generation and High-Performance State Machine Applications**
- **6-Bit Internal Binary Counter**
- **8-Bit Internal State Register**
- **Programmable Clock Polarity**
- **Outputs Programmable for Registered or Combinatorial Operation**
- **6-Bit Counter Simplifies Logic Equation Development in State Machine Designs**
- **Programmable Output Enable**

M SUFFIX . . . , JT PACKAGE
C SUFFIX . . . . JT OR NT PACKAGE
(TOP VIEW)



M SUFFIX . . . . FK PACKAGE
C SUFFIX . . . . FK OR FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TIBPSG507 is a 13 × 80 × 8 Programmable Sequence Generator (PSG) that offers the system designer unprecedented flexibility in a high-performance field-programmable logic device. Applications such as waveform generators, state machines, dividers, timers, and simple logic reduction are all possible with a PSG. By utilizing the built-in binary counter, the PSG is capable of generating complex timing controllers. The binary counter also simplifies logic equation development in state machine and waveform generator applications.

The PSG507 contains 80 product (AND) terms, a 6-bit binary counter with control logic, eight S/R state holding registers, and eight outputs. The eight outputs can be individually programmed for either registered or combinatorial operation. The clock input is fuse programmable for either positive- or negative-edge operation.

The 6-bit binary counter is controlled by a synchronous-clear and a count/hold function. Each control function has a nonregistered and registered option. When either SCLR0 or SCLR1 is taken high, the counter resets to zero on the next active clock edge. When either $\overline{\text{CNT}}$/HLD0 or $\overline{\text{CNT}}$/HLD1 is taken high, the counter is held at the present count and is not allowed to advance on the active clock edge. The SCLR function overrides the $\overline{\text{CNT}}$/HLD feature when both lines are simultaneously high.

Clock polarity is programmable through the clock polarity fuse. Leaving this fuse intact selects positive-edge triggering. Negative-edge triggering is selected by blowing this fuse. Pin 17 functions as an input and/or an output enable. When the output enable fuse is intact, all outputs are always enabled allowing pin 17 to be used strictly as an input. Blowing the output enable fuse lets pin 17 function as an output enable and an input. In this mode, the outputs are enabled when pin 17 is low and are in a high-impedance state when pin 17 is high.

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description (continued)

The eight outputs can be individually programmed for combinational operation by blowing the output multiplexer fuse. When the output multiplexer fuse is left intact, registered operation is selected.

The M suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The C suffix devices are characterized for operation from 0°C to 75°C.

6-BIT COUNTER CONTROL FUNCTION TABLE (see Note 1)

$\overline{CNT}$/HLD1	$\overline{CNT}$/HLD0	SCLR1	SCLR0	OPERATION
L	L	L	L	counter active
X	X	X	H	synchronous clear
X	X	H	X	synchronous clear
X	H	L	L	hold counter
H	X	L	L	hold counter

NOTE 1: When all fuses are blown on a product line (AND), its output will be high. When all fuses are blown on a sum line (OR), its outputs will be low. All product and sum terms are low on devices with fuses intact.

S/R FUNCTION TABLE (see Note 2)

CLK POLARITY FUSE	CLK	S	R	STATE REGISTER
INTACT	↑	L	L	Q_0
INTACT	↑	L	H	L
INTACT	↑	H	L	H
INTACT	↑	H	H	INDET†
BLOWN	↓	L	L	Q_0
BLOWN	↓	L	H	L
BLOWN	↓	H	L	H
BLOWN	↓	H	H	INDET†

†Output state is indeterminate

NOTE 2: After power-up, the device must be initialized to its desired state. Q_0 is the state of the S/R register before the active clock edge.

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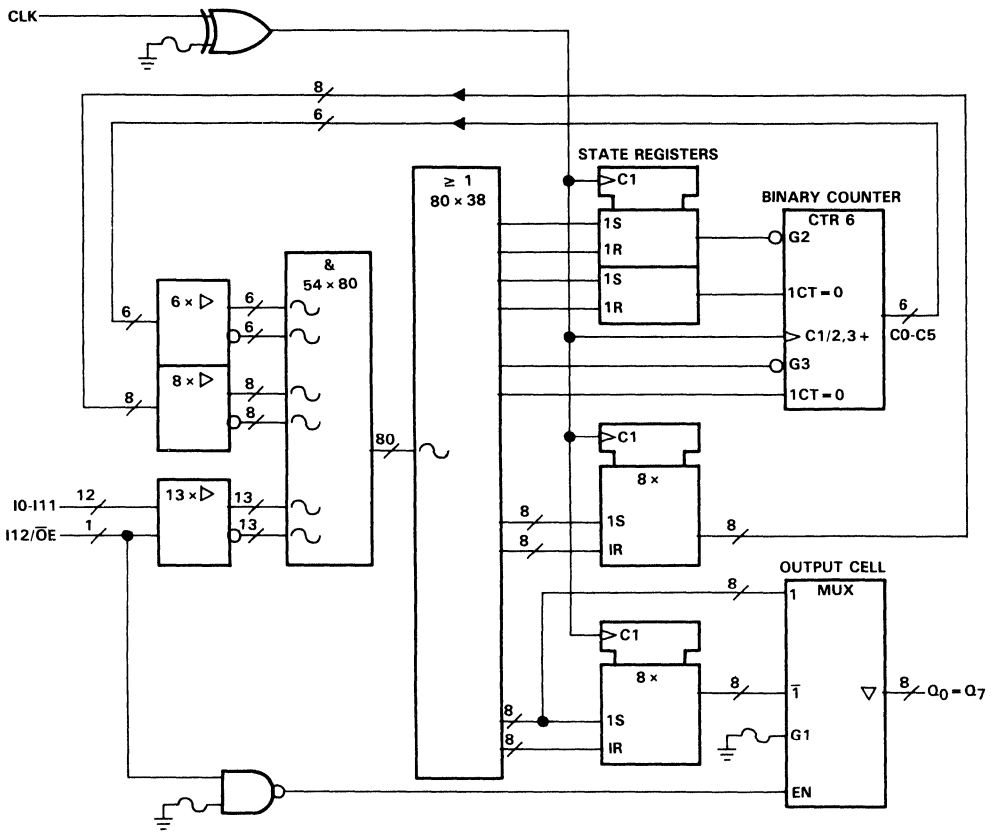
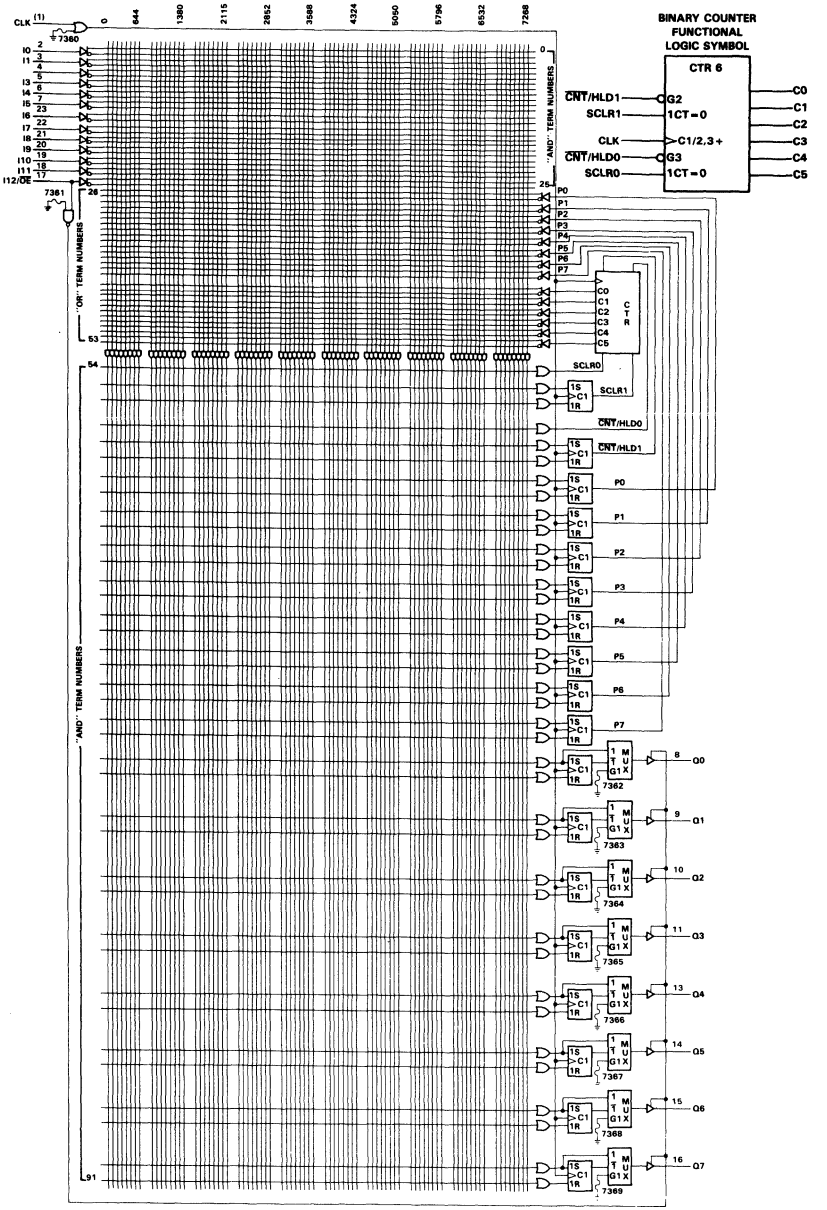
functional block diagram



∿ denotes fused inputs

logic diagram (positive logic)



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absolute maximum ratings

Supply voltage, V_{CC} (see Note 3) . . . . . 7 V
Input voltage, V_I (see Note 3) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 3) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 3: These ratings apply except for programming pins during a programming cycle or during the diagnostic mode.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				8	mA
t_w	Pulse duration	Clock high				ns
		Clock low				
t_{su}	Setup time before CLK active transition†	Input or feedback to S/R inputs				ns
		Input or feedback to SCLR0				
		Input or feedback to $\overline{CNT}$/HOLD0				
t_h	Hold time after CLK active transition†	Input or feedback at S/R inputs				ns
		Input or feedback at SCL0				
		Input or feedback at $\overline{CNT}$/HLD0				
T_A	Operating free-air temperature		−55		125	°C

†Internal setup and hold times, t_{su} feedback to SCLR1, feedback to $\overline{CNT}$/HLD1; t_h feedback at SCLR1 and feedback at $\overline{CNT}$/HLD1, are guaranteed by f_{max} specifications. The active transition of CLK is determined by the programmed state of the CLK polarity fuse.

PRODUCT PREVIEW

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V				−0.25	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 0.5 V		−30		−130	mA
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
I_{OZL}	I/O ports	V_{CC} = 5.5 V,	V_O = 0.4 V				−250	μA
	All others						−20	
I_{CC}		V_{CC} = 5.5 V,	See Note 4,	Outputs open		156	230	mA
C_i		f = 1 MHz,	V_I = 2 V			7		pF
C_o		f = 1 MHz,	V_O = 2 V			11		pF
C_{clk}		f = 1 MHz,	V_I = 2 V			14		pF

switching characteristics over recommended supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§	6-Bit counter with SCLR1 or $\overline{CNT}$/HLD1		R1 = 390 Ω, R2 = 750 Ω, See Figure 3				MHz
	6-Bit counter with SCLR0 or $\overline{CNT}$/HLD0						
	S/R registers						
t_{pd}¶	CLK↑	Q (nonregistered)#					ns
	CLK↓	Q (nonregistered)#					
	CLK↑	Q (registered)					
	CLK↓	Q (registered)					
	I or Feedback	Q (nonregistered)					
t_{en}	$\overline{OE}$↓	Q					ns
t_{dis}	$\overline{OE}$↑	Q					ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
§f_{max} is independent of the number of product terms used.
¶The active edge of CLK is determined by the programmed state of the CLK polarity fuse.
#t_{pd} CLK to Q (nonregistered) is the same for data clocked from the counter or state registers.
NOTE 4: When the clock is programmed for negative edge, then V_I = 4.5 V. When the clock is programmed for positive edge, then V_I = 0.

PRODUCT PREVIEW

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

absolute maximum ratings

Supply voltage, V_{CC} (see Note 3) . . . . . 7 V
Input voltage (see Note 3) . . . . . 5.5 V
Voltage applied to disabled output (see Note 3) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 3: These ratings apply except when programming pins during a programming cycle or during the diagnostic mode.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high	6			ns
		Clock low	6			
t_{su}	Setup time before CLK active transition†	Input or feedback to S/R inputs	12			ns
		Input or feedback to SCLR0	25			
		Input or feedback to $\overline{CNT}$/HOLD0	25			
t_h	Hold time after CLK active transition†	Input or feedback at S/R inputs	0			ns
		Input or feedback at SCL0	0			
		Input or feedback at $\overline{CNT}$/HLD0	0			
T_A	Operating free-air temperature		0		75	°C

†Internal setup and hold times, t_{su} feedback to SCLR1, feedback to $\overline{CNT}$/HLD1; t_h feedback at SCLR1 and feedback at $\overline{CNT}$/HLD1, are guaranteed by f_{max} specifications. The active transition of CLK is determined by the programmed state of the CLK polarity fuse.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.25	0.5	V
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V				20	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V				−0.25	mA
I_O‡	V_{CC} = 5.25 V,	V_O = 0.5 V		−30		−130	mA
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V				20	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V				−20	μA
I_{CC}	V_{CC} = 5.25 V,	See Note 4,	Outputs open		156	210	mA
C_i	f = 1 MHz,	V_I = 2 V			7		pF
C_o	f = 1 MHz,	V_O = 2 V			11		pF
C_{clk}	f = 1 MHz,	V_I = 2 V			14		pF

switching characteristics over recommended supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§	6-Bit counter with SCLR1 or $\overline{CNT}$/HLD1		R1 = 300 Ω, R2 = 390 Ω, See Figure 3	58	65		MHz
	6-Bit counter with SCLR0 or $\overline{CNT}$/HLD0			33	50		
	S/R registers			58	65		
t_{pd}¶	CLK↑	Q (nonregistered)#		8		27	ns
	CLK↓	Q (nonregistered)#		9		28	
	CLK↑	Q (registered)		3		10	
	CLK↓	Q (registered)		4		11	
	I or Feedback	Q (nonregistered)		10		22	
t_{en}	$\overline{OE}$↓	Q		2	6	10	ns
t_{dis}	$\overline{OE}$↑	Q		2	6	10	ns

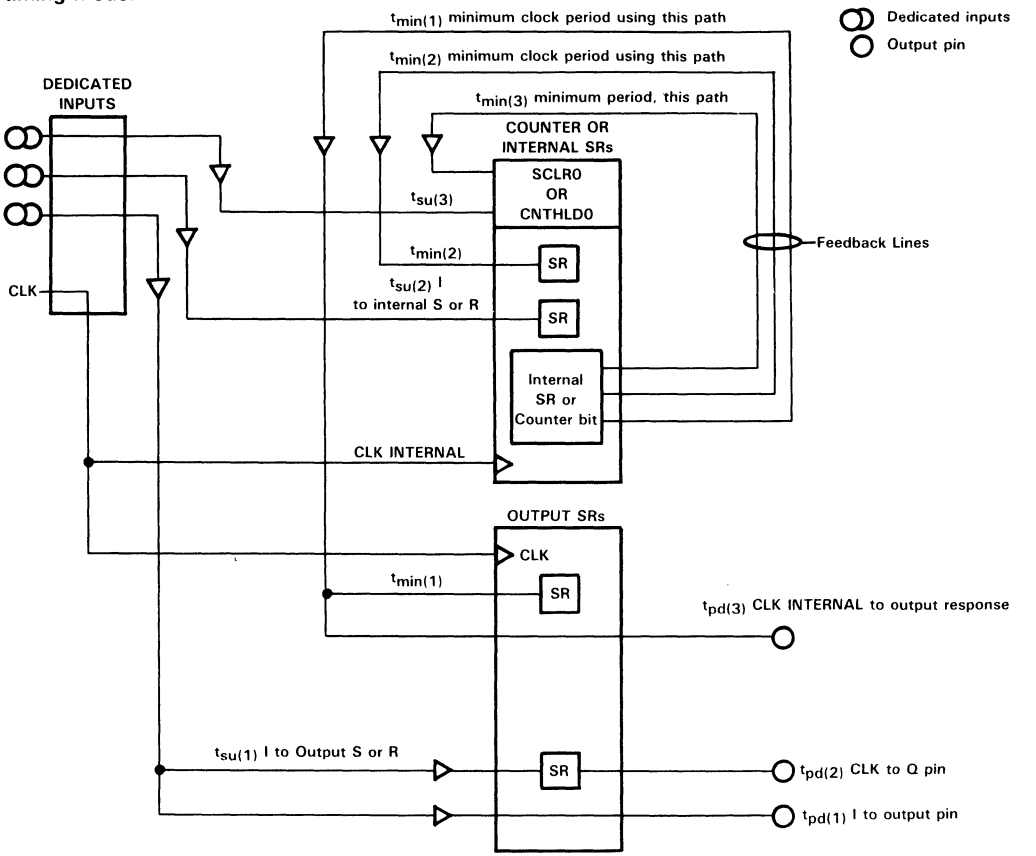
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Note more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§f_{max} is independent of the number of product terms used.
¶The active edge of CLK is determined by the programmed state of the CLK polarity fuse.
#t_{pd} CLK to Q (nonregistered) is the same for data clocked from the counter or state registers.
NOTE 4: When the clock is programmed for negative edge, then V_I = 4.5 V. When the clock is programmed for positive edge, then V_I = 0.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on firmware, software, and hardware updates are available upon request. Information on persons capable of programming Texas Instruments Programmable Logic is also available upon request from the nearest TI sales office or local authorized TI distributor; information may also be obtained by calling or writing Texas Instruments at (214) 997-5666, Texas Instruments, Post Office Box 655803, Dallas, Texas 75265.

timing model



glossary—timing model

$t_{pd(1)}$ — Maximum time Interval from the time a signal edge is received at any input pin to the time any logically affected combinational output pin delivers a response.

$t_{pd(2)}$* — Maximum time interval from a positive edge on the clock input pin to data delivery on the output pin corresponding to any output SR register.

$t_{pd(3)}$* — Maximum time interval from the positive edge on the clock input pin to the response on any logically affected combinationally configured output (at the pin), where data origin is any internal SR register or counter bit.

$t_{su(1)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the **active** clock edge on the clock input pin when data affects the S or R line of any output SR register.

$t_{su(2)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the **active** clock edge on the clock input pin when data affects the S or R line of any internal SR register.

$t_{su(3)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the **active** clock edge on the clock input pin **only when entering data on SCLR0 or CNT/HLD0 lines.**

$t_{min(1)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accomodate when using feedback from any internal SR register or counter bit to feed the S or R line of any output SR register.

$t_{min(2)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accomodate when using feedback from any internal SR register to feed the S or R line of any internal SR register.

$t_{min(3)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accomodate when using feedback from any internal SR register or counter bit to feed SCLR0 or CNT/HLD0.

PARAMETER VALUES FOR TIMING MODEL

$t_{pd(1)}$ = 22 ns	$t_{su(1)}$ = 12 ns	$t_{min(1)}$ = 17 ns
$t_{pd(2)}$* = 10 ns	$t_{su(2)}$ = 12 ns	$t_{min(2)}$ = 17 ns
$t_{pd(3)}$* = 27 ns	$t_{su(3)}$ = 25 ns	$t_{min(3)}$ = 25 ns

*add 1 ns when using negative clock edge as active

INTERNAL NODE NUMBERS

SCLR0	25	CNTHLD0	28	P0-P7	SET 31-38
SCLR1	SET 26	CNTHLD1	SET 29		RESET 39-46
	RESET 27		RESET 30	Q0-Q7	RESET 47-54
		C0-C5	55-60		

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PRINCIPLES OF OPERATION

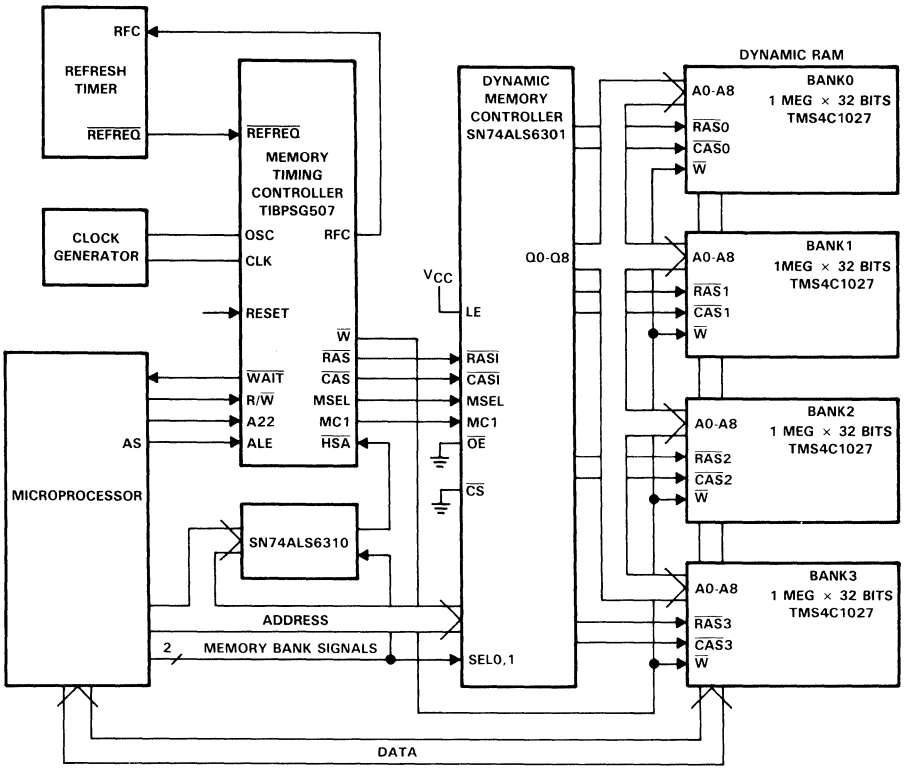
PSG design theory

Most state machine and waveform generator designs can be simplified with the PSG by referencing all or part of each sequence to a binary count. The internal state registers can then be used to keep track of which binary count sequence is in operation, to store input data and keep track of internally generated status bits, or as output registers when connected to a nonregistered output cell. State registers can also be used to expand the binary counter when a larger counter is needed.

Through the use of the binary counter, the number of product lines and state registers required for a design is usually reduced. In addition, the designer does not have to be concerned about generating wait states where the outputs are unaffected because these can be timed from the binary counter. For detailed information and examples using this design concept, see the "DESIGNER'S GUIDE TO THE PSG507" located in the applications report section of the *Programmable Logic Data Book*, 1990.

TYPICAL APPLICATION

The TIBPSG507 is used in this application to generate the required memory timing control signals ($\overline{RAS}$, $\overline{CAS}$, etc) for the memory timing controller.



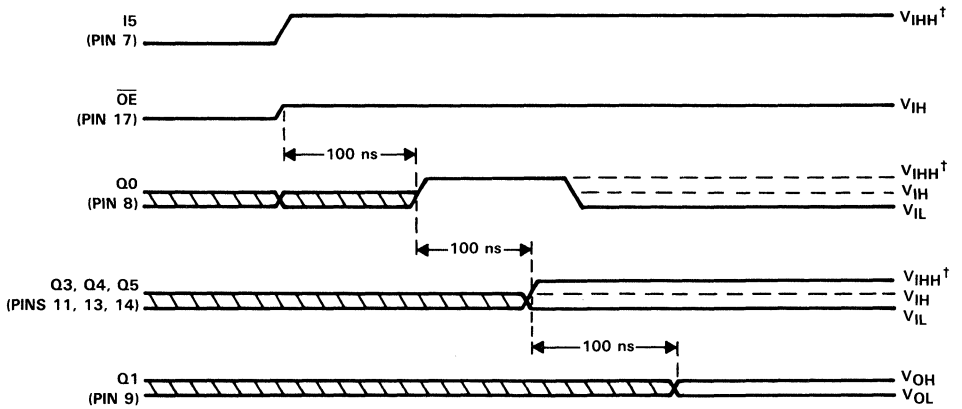
For detailed information, please see the "SYSTEMS SOLUTION FOR STATIC COLUME DECODE" Application Report.

diagnostics

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state registers. The following are the step-by-step procedures required for the diagnostics.

1. Disable all outputs by taking $\overline{OE}$ (pin 17) high. (Note: If pin 17 is being used as an input to the array, then pin I5 or pin 7 must be taken to double high first before pin 17 is taken high.)
2. Take Q0 (pin 8) double high to enable the diagnostics test sequence.
3. Apply appropriate levels of voltage to pins 11, 13 and 14 to select the desired state register, (see Table 1)
4. The voltage level monitored on pin 9 will indicate the state of the selected state register.

diagnostics waveforms



†V_{IHH} = 10.25 V min, 10.5 V nom, and 10.75 V max

TABLE 1. ADDRESSING STATE REGISTERS DURING DIAGNOSTICS

REGISTER BINARY ADDRESS			BURRIED REGISTER SELECTED
PIN 11	PIN 13	PIN 14	
L	L	L	SCLR0
L	L	H	SCLR1
L	L	HH	$\overline{CNT}$/HLD0
L	H	L	$\overline{CNT}$/HLD1
L	H	H	P0
L	H	HH	P1
L	HH	L	P2
L	HH	H	P3
L	HH	HH	P4
H	L	L	P5
H	L	H	P6
H	L	HH	P7
H	H	L	C0
H	H	H	C1
H	H	HH	C2
H	HH	L	C3
H	HH	H	C4
H	HH	HH	C5

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TYPICAL APPLICATIONS

f_{max}

When the TIBPSG507 is used with two or more devices linked to build a "multi-device" state machine (see Figure 1), the maximum operating frequency for this state machine is limited to the sum of t_{pd} CLK-Q (10 ns) of the first '507 and t_{su} (12 ns), of the second '507, for a clock period of 22 ns. This results in an f_{max} of 45 MHz (1/22 ns).

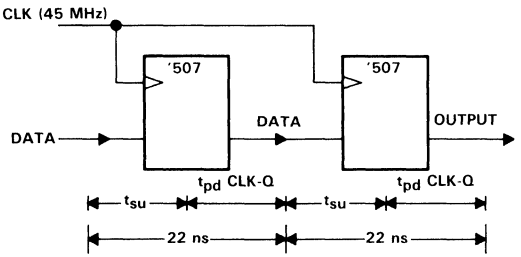
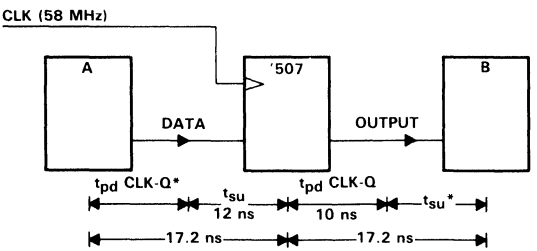


FIGURE 1

Figure 2 shows the TIBPSG507 used in a system environment where it is operated at 58 MHz, the highest clock rate possible without compromising data integrity. At the input of the '507, the system clock period is limited to the sum of t_{pd} CLK-Q of device A and t_{su} of the '507. At the output of the '507, the system clock period is limited to the sum of t_{pd} CLK-Q of the '507 and t_{su} of device B.

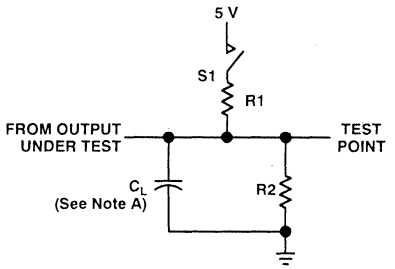
For this system to operate at 58 MHz, a system clock period of 17.2 ns must be met. Given that t_{su} for the '507 is 12 ns minimum, t_{pd} CLK-Q of device A cannot exceed 5.2 ns (12 ns + 5.2 ns = 17.2 ns). On the output side of the '507, t_{pd} CLK-Q of 10 ns must be allowed. In order to meet the system clock period of 17.2 ns, t_{su} for device B must not exceed 7.2 ns (10 ns + 7.2 ns) = 17.2 ns). Under these circumstances, a system frequency of 58 MHz (1/17.2 ns) can be realized.



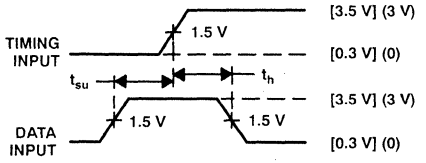
*External device parameters (t_{pd} CLK-Q of device A ≤ 5.2 ns, and t_{su} of device B ≤ 7.2 ns)

FIGURE 2

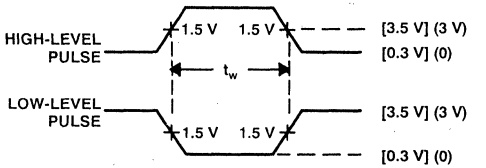
PARAMETER MEASUREMENT INFORMATION



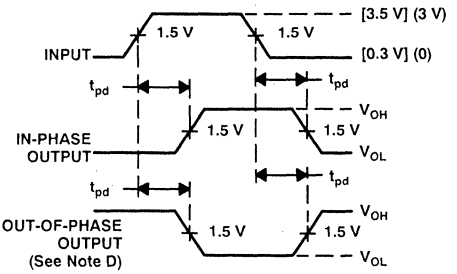
LOAD CIRCUIT FOR 3-STATE OUTPUTS



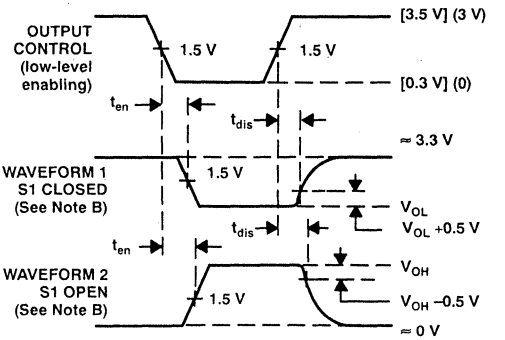
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For M suffix, use voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 3

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

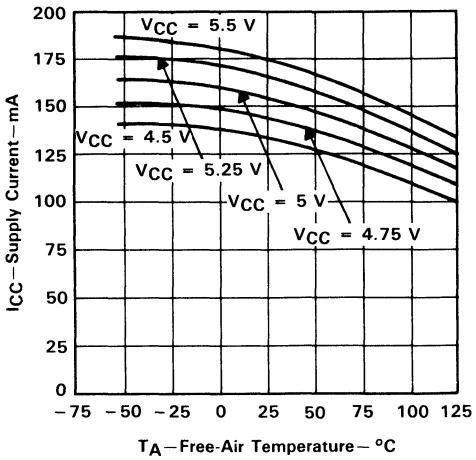

FIGURE 4

POWER DISSIPATION
vs
FREQUENCY

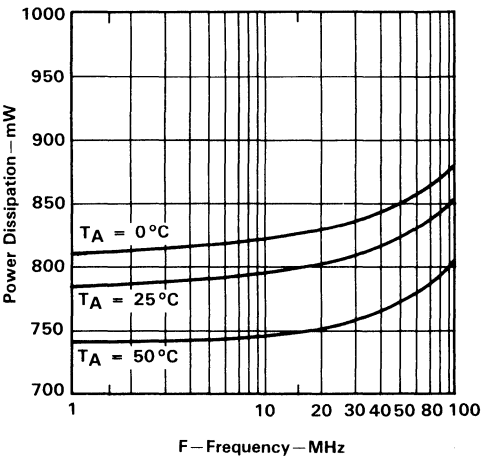

FIGURE 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

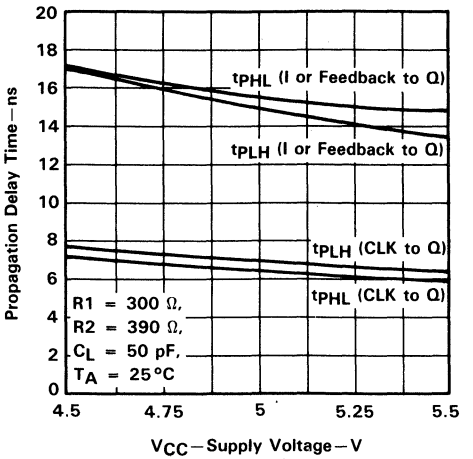

FIGURE 6

PROPAGATION DELAY
vs
LOAD CAPACITANCE

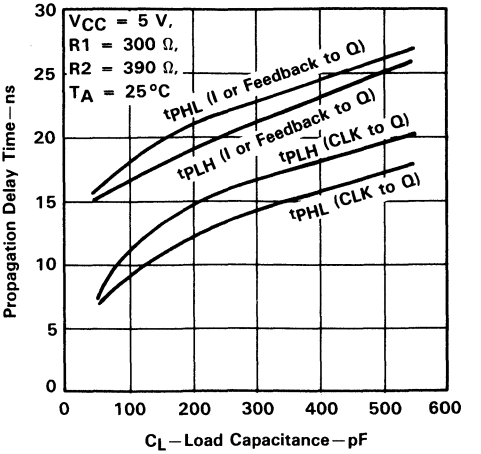

FIGURE 7

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

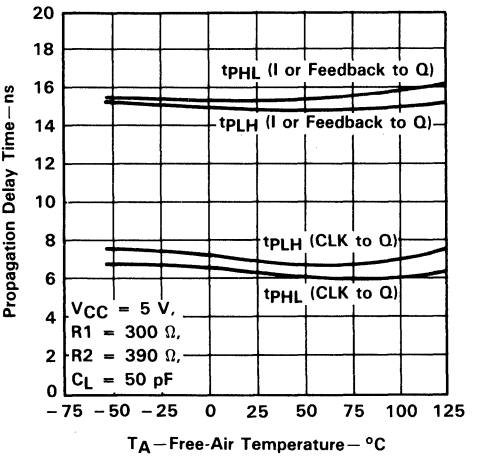

FIGURE 8

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

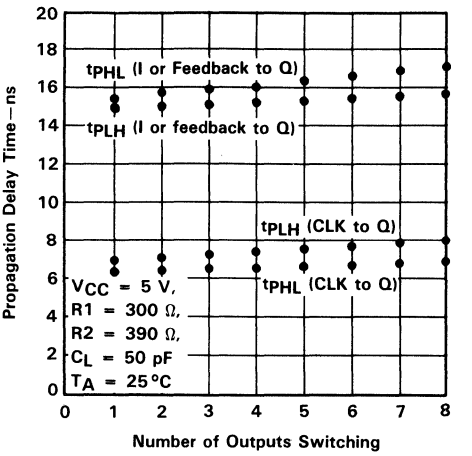

FIGURE 9

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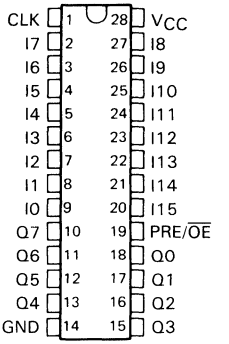
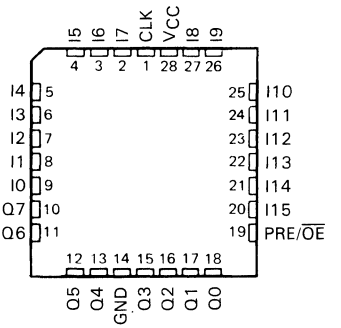
- 50-MHz Clock Rate
- Power-On Preset of All Flip-Flops
- 6-Bit Internal State Register with 8-Bit Output Register
- Power Dissipation . . . 600 mW Typical
- Programmable Asynchronous Preset or Output Control
- Functionally Equivalent to, but Faster than 82S105A†

M SUFFIX . . . J PACKAGE
C SUFFIX . . . N PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



description

The TIB82S105B is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 14 pairs of sum terms (OR terms). The product and sum terms are used to control the 6-bit internal state register and the 8-bit output register.

The outputs of the internal state register (P0—P5) are fed back and combined with the 16 inputs (I0—I15) to form the AND array. In addition a single sum term is complemented and fed back to the AND array, which allows any of the product terms to be summed, complemented, and used as an input to the AND array.

The state and output registers are positive-edge-triggered S/R flip-flops. These registers are unconditionally preset high on power-up. Pin 19 can be used to preset both registers or, by blowing the proper fuse, be converted to an output control function.

The TIB82S105BM is characterized for operation over the full military temperature range of −55°C to 125°C. The TIB82S105BC is characterized for operation from 0°C to 75°C.

† Power-up preset and asynchronous preset functions are not identical to 82S105A. See Recommended Operating Conditions.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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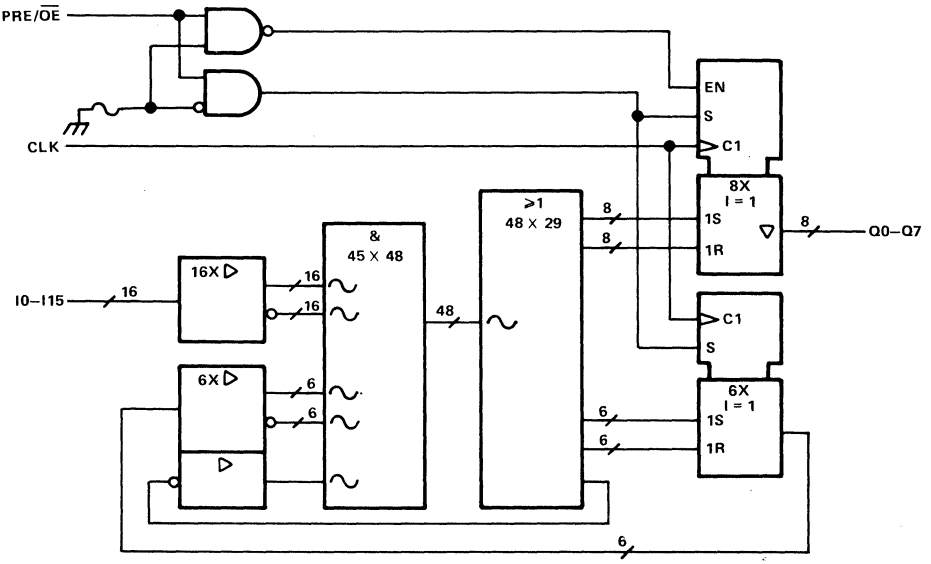
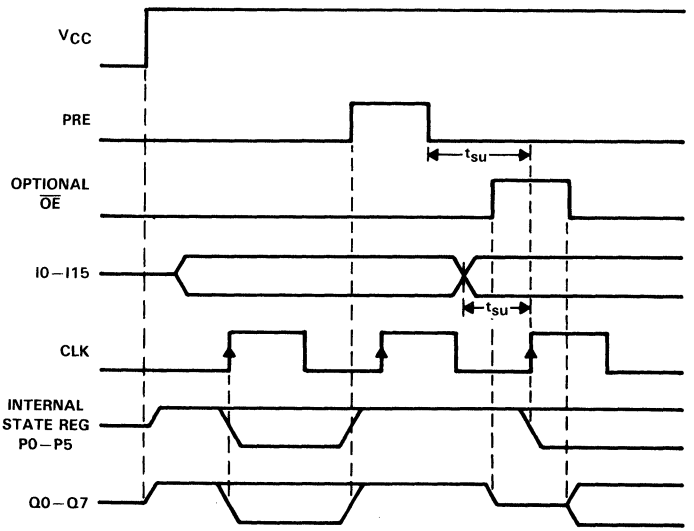
functional block diagram (positive logic)



~ denotes fused inputs.

timing diagram



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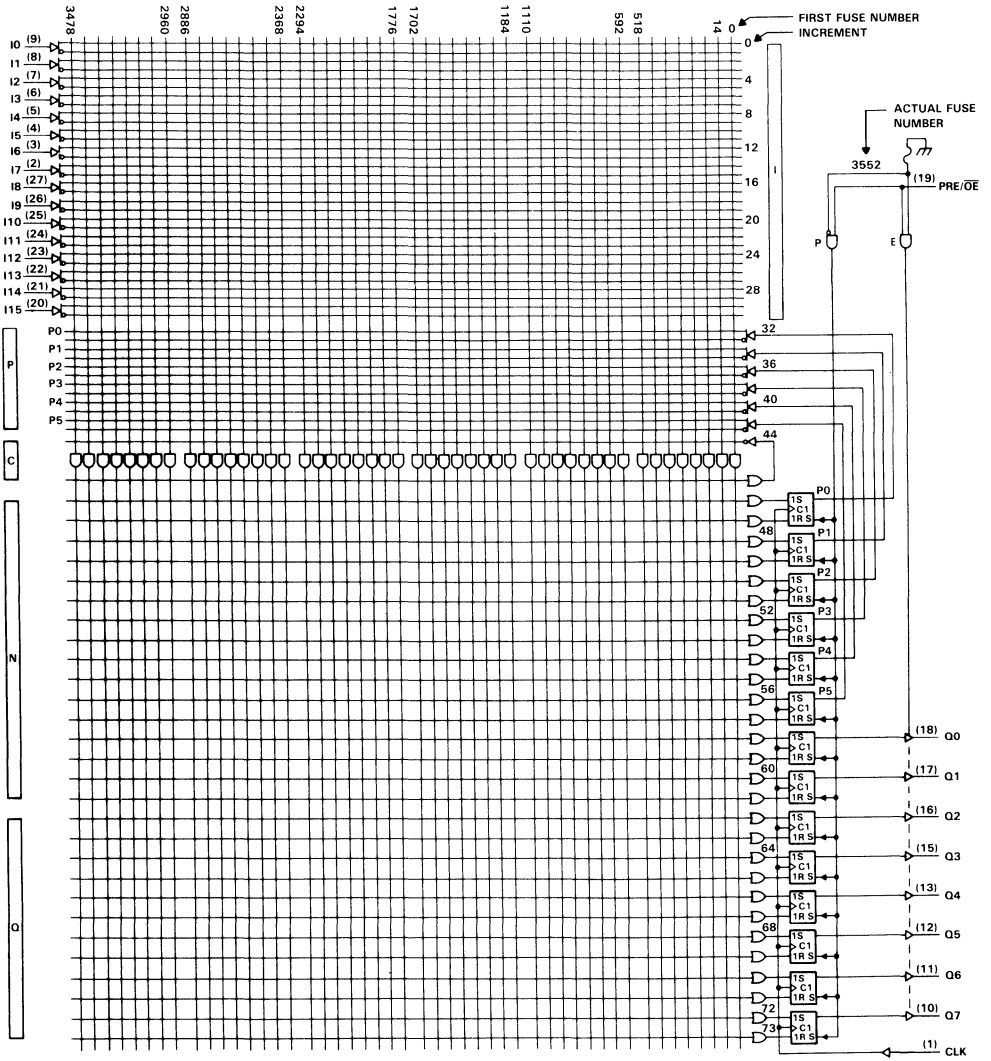
logic diagram (positive logic)



NOTES: 1. All AND gate inputs with a blown link float to a logic 1.
2. All OR gate inputs with a blown link float to a logic 0.
3. Fuse Numbers = First Fuse Number + Increment.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 7 V
Input voltage (see Note 4) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 4) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 4: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency†	1 thru 48 product terms without C-array‡	0		40	MHz
		1 thru 48 product terms with C-array	0		25	
t_w	Pulse duration	Clock high or low	12			ns
		Preset	18			
t_{su}	Setup time before CLK↑, 1 thru 48 product terms	Without C-array	25			ns
		With C-array	40			
t_{su}	Setup time, Preset low (inactive) before CLK↑§		10			ns
t_h	Hold time, input after CLK↑		0			ns
T_A	Operating free-air temperature		−55		125	°C

†The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.
‡The C-array is the single sum term that is complemented and fed back to the AND array.
§After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			25	μA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.25	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0.5 V	−30		−250	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_{CC}	V_{CC} = 5.5 V, PRE/$\overline{OE}$ input at GND,	V_I = 4.5 V, Outputs open		120	180	mA

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§	Without C array				40	70		MHz
	With C array				25	45		
t_{pd}		CLK↑	Q	R1 = 390 Ω,		8	20	ns
t_{pd}		PRE↑	Q	R2 = 750 Ω,		12	25	ns
t_{pd}		V_{CC}↑	Q	See Figure 3		0	10	ns
t_{en}		$\overline{OE}$↓	Q			10	25	ns
t_{dis}		$\overline{OE}$↑	Q			5	15	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 1 second. Set V_O at 0.5 V to avoid test equipment ground degradation.
§f_{max} is independent of the internal programmed configuration and the number of product terms used.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 7 V
Input voltage (see Note 4) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 4) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 4: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency†	1 thru 48 product terms without C-array‡	0		50	MHz
		1 thru 48 product terms with C-array	0		30	
t_w	Pulse duration	Clock high or low	10			ns
		Preset	15			
t_{su}	Setup time before CLK↑, 1 thru 48 product terms	Without C-array	15			ns
		With C-array	30			
t_{su}	Setup time, Preset low (inactive) before CLK↑§		8			ns
t_h	Hold time, input after CLK↑		0			ns
T_A	Operating free-air temperature		0		75	°C

†The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.
‡The C-array is the single sum term that is complemented and fed back to the AND array.
§After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4	3		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.37	0.5	V
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			25	μA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.25	mA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.25 V	−30		−112	mA
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V			−20	μA
I_{CC}	V_{CC} = 5.25 V, PRE/$\overline{OE}$ input at GND,	V_I = 4.7 V, Outputs open		120	180	mA

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§	Without C array				50	70		MHz
	With C array				30	45		
t_{pd}		CLK↑	Q	R1 = 500 Ω,		8	15	ns
t_{pd}		PRE↑	Q	R2 = 500 Ω,		12	20	ns
t_{pd}		V_{CC}↑	Q	See Figure 3		0	10	ns
t_{en}		$\overline{OE}$↓	Q			10	20	ns
t_{dis}		$\overline{OE}$↑	Q			5	10	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.
§f_{max} is independent of the internal programmed configuration and the number of product terms used.

programming information

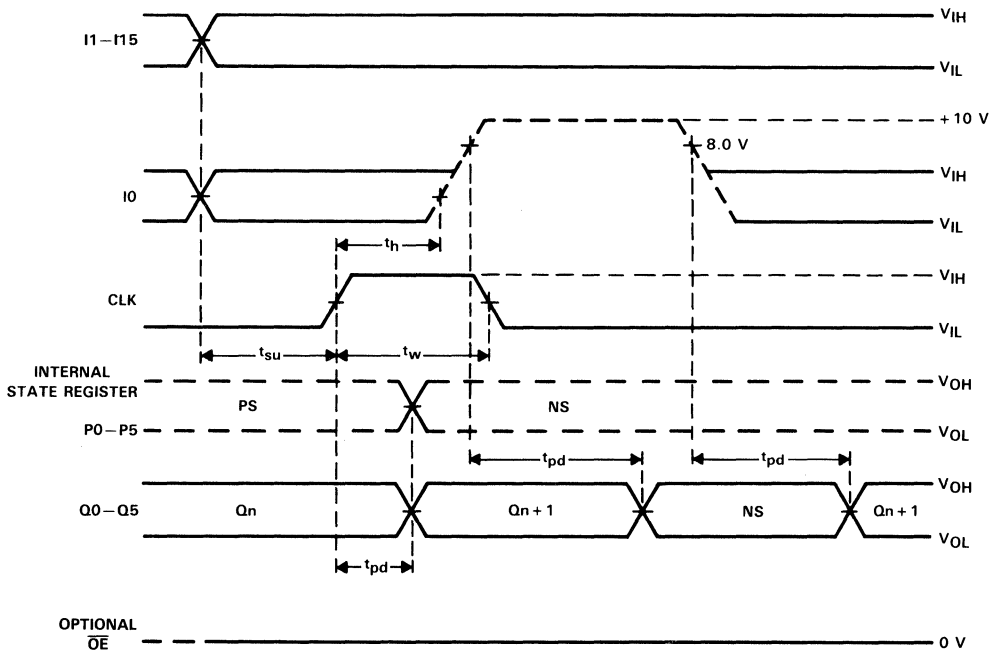
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

diagnostics

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state register. When I0 (pin 9) is held at 10 V, the state register bits P0—P5 will appear at the Q0—Q5 outputs and Q6—Q7 will be high. The contents of the output register will remain unchanged.

diagnostics waveforms



PS = Present state, NS = Next state

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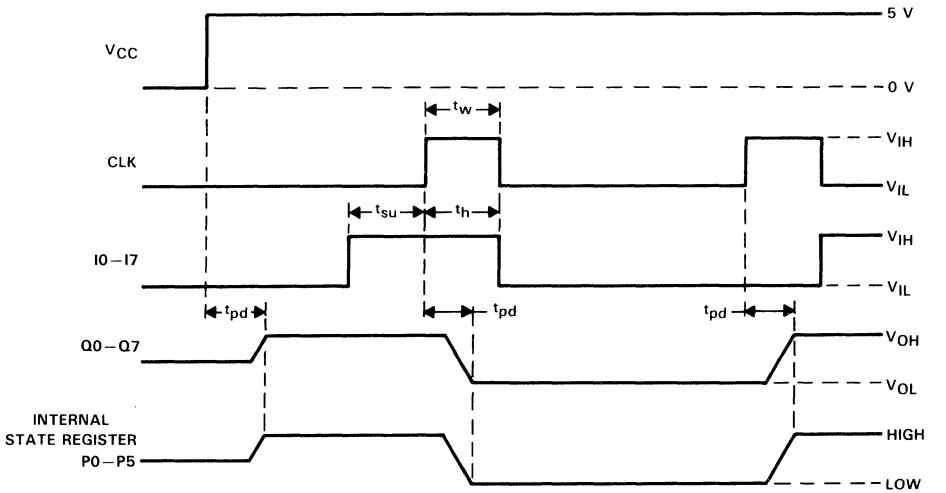
test array

A test array that consists of product lines 48 and 49 has been added to these devices to allow testing prior to programming. The test array is factory programmed as shown below. Testing is accomplished by connecting Q0—Q7 to I8—I15, PRE/$\overline{OE}$ to GND, and applying the proper input signals as shown in the timing diagram. Product lines 48 and 49 MUST be deleted during user programming to avoid interference with the programmed logic function.

TEST ARRAY PROGRAM

PRODUCT LINE	AND																								OPTION PRE/$\overline{OE}$	OR												H
	C	$\overline{C}$	INPUT (In)																PRESENT STATE (PS)						NEXT STATE (NS)						OUT (Qn)						
			1	1	1	1	1	1																														
			5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	X	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
49	—	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H

test array waveforms



TEST ARRAY DELETED

PRODUCT LINE	AND																								OPTION PRE/$\overline{OE}$	OR												H
	C	$\overline{C}$	INPUT (In)																PRESENT STATE (PS)						NEXT STATE (NS)						OUT (Qn)						
			1	1	1	1	1	1																														
			5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	—	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—
49	—	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—

X = Fuse intact, — = Fuse blown

TIB82S105B, 82S105A COMPARISON

The Texas Instruments TIB82S105B is a 16 × 48 × 8 Field-Programmable Logic Sequencer that is functionally equivalent to the Signetics 82S105A. However, the TIB82S105B is designed for a maximum speed of 50 MHz with the preset function being made conventional. As a result the TIB82S105B differs from the 82S105A in speed and in the preset recovery function.

The TIB82S105B is a high-speed version of the original 82S105A. The TIB82S105B features increased switching speeds with no increase in power. The maximum operating frequency is increased from 20 MHz to 50 MHz and does not decrease as more product terms are connected to each sum (OR) line. For instance, if all 48 product tems were connected to a sum line on the original 82S105A, the f_{max} would be about 15 MHz. The f_{max} for the TIB82S105B remains at 50 MHz regardless of the programmed configuration. In addition, the preset recovery sequence was changed to a conventional recovery sequence, providing quicker clock recovery times. This is explained in the following paragraph.

The TIB82S105B and the 82S105A are equipped with power-up preset and asynchronous preset functions. The power-up preset causes the registers to go high during power-up. The asynchronous preset inhibits clocking and causes the registers to go high whenever the preset pin is taken high. After a power-up preset occurs, the minimum setup time from power-up to the first clock pulse must be met in order to assure that clocking is not inhibited. In a similar manner after an asynchronous preset, the preset input must return low (inactive) for a given time, t_{su}, before clocking.

The Signetics 82S105A was designed in such a way that after both power-up preset and asynchronous preset it requires that a high-to-low clock transition occur before a clocking transition (low-to-high) will be recognized. This is shown in Figure 1. The Texas Instruments TIB82S105B does not require a high-to-low clock transition before clocking can be resumed, it only requires that the preset be inactive 8 ns (preset inactive-state setup time) before the clock rising edge. See Figure 2.

The TIB82S105B, with an f_{max} of 50 MHz, is ideal for systems in which the state machine must run several times faster than the system clock. It is recommended that the TIB82S105B be used in new designs. ***However, if the TIB82S105B is used to replace the 82S105A, then the customer must understand that clocking will begin with the first clock rising edge after preset.***

TABLE 3. SPEED DIFFERENCES

PARAMETER	82S105A SIGNETICS	TIB82S105B TI ONLY
f_{max}	20 MHz	50 MHz
t_{pd}, CLK to Q	20 ns	15 ns

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

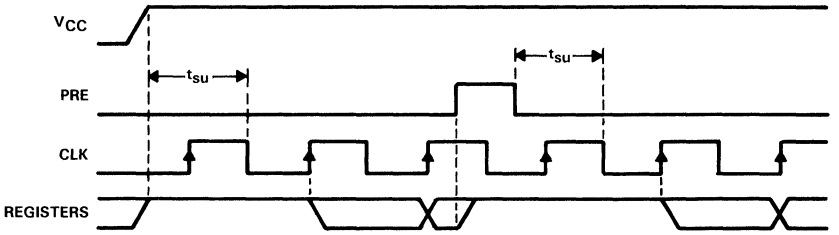


FIGURE 1. 82S105A PRESET RECOVERY OPERATION

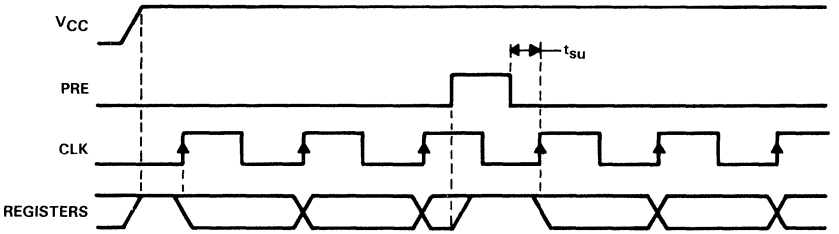
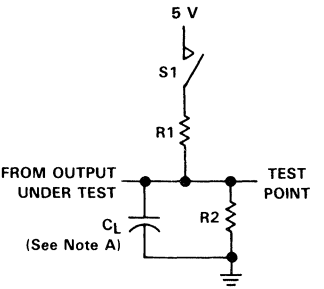
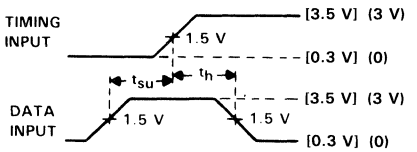


FIGURE 2. TIB82S105B PRESET RECOVERY OPERATION

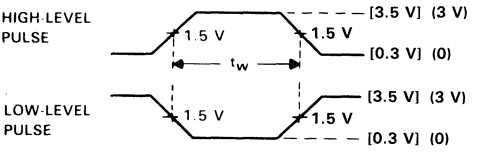
PARAMETER MEASUREMENT INFORMATION



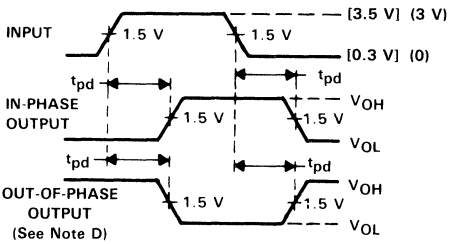
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



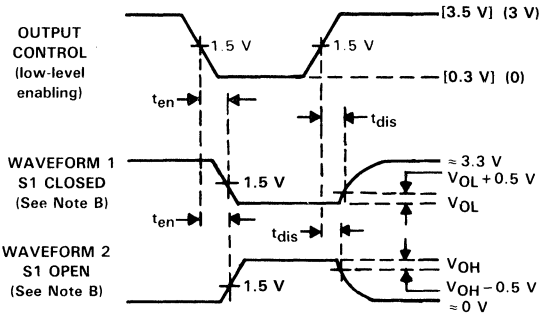
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

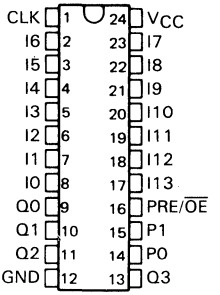
NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For M suffix, use the voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in [ ], PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 3

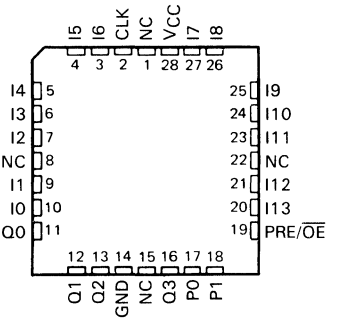
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **Programmable Asynchronous Preset or Output Control**
- **Power-On Preset of All Flip-Flops**
- **8-Bit Internal State Register with 4-Bit Output Register**
- **Power Dissipation . . . 600 mW Typical**
- **Functionally Equivalent to,† but Faster than 82S167A**

M SUFFIX . . . JT PACKAGE
C SUFFIX . . . NT PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TIB82S167B is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 12 pairs of sum terms (OR terms). The product and sum terms are used to control the 8-bit internal state register and the 4-bit output register.

The outputs of the internal state register (P0-P7) are fed back and combined with the 14 inputs (I0-I13) to form the AND array. In addition the first two bits of the internal state register (P0-P1) are brought off-chip to allow the output register to be extended to 6 bits if desired. A single sum term is complemented and fed back to the AND array, which allows any of the product terms to be summed, complemented, and used as inputs to the AND array.

The state and output registers are positive-edge-triggered S/R flip-flops. These registers are unconditionally preset high on power-up. PRE/$\overline{OE}$ can be used as PRE to preset both registers or, by blowing the proper fuse, be converted to an output control function, $\overline{OE}$.

The TIB82S167BM is characterized for operation over the full military temperature range of −55°C to 125°C. The TIB82S167BC is characterized for operation from 0°C to 75°C.

† Power up preset and asynchronous preset functions are not identical to 82S167A.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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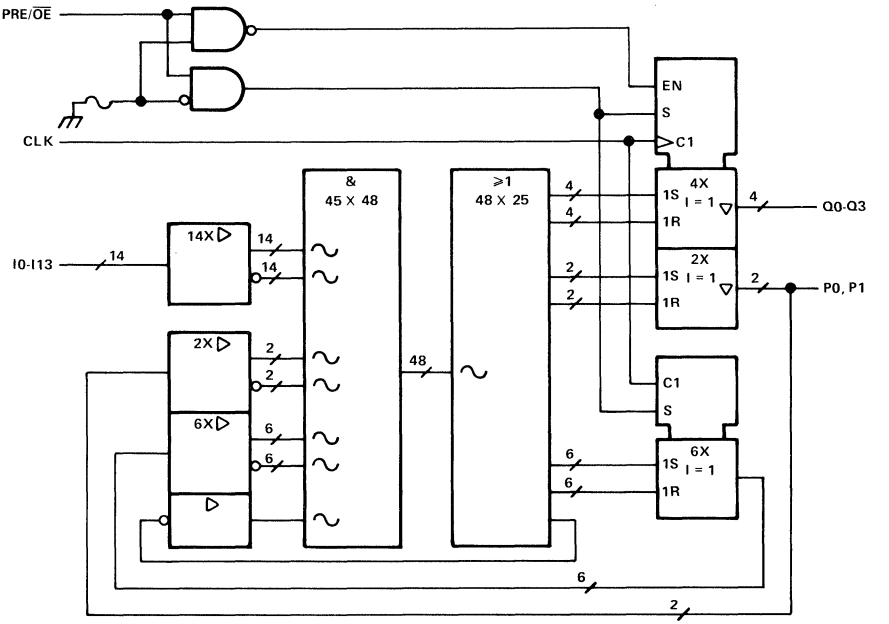
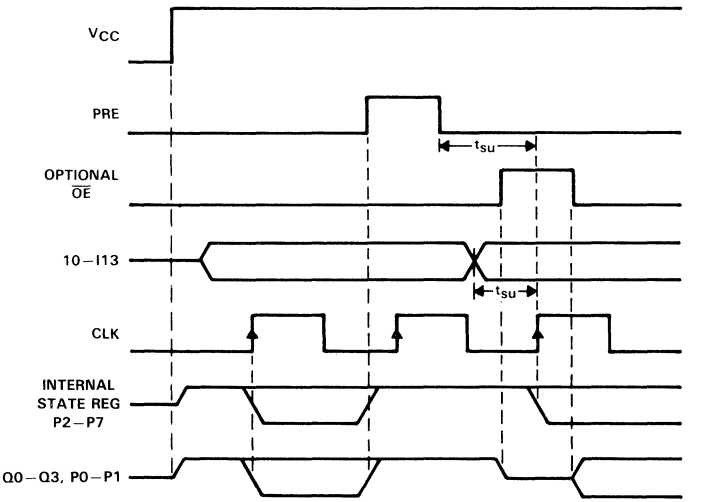
functional block diagram (positive logic)

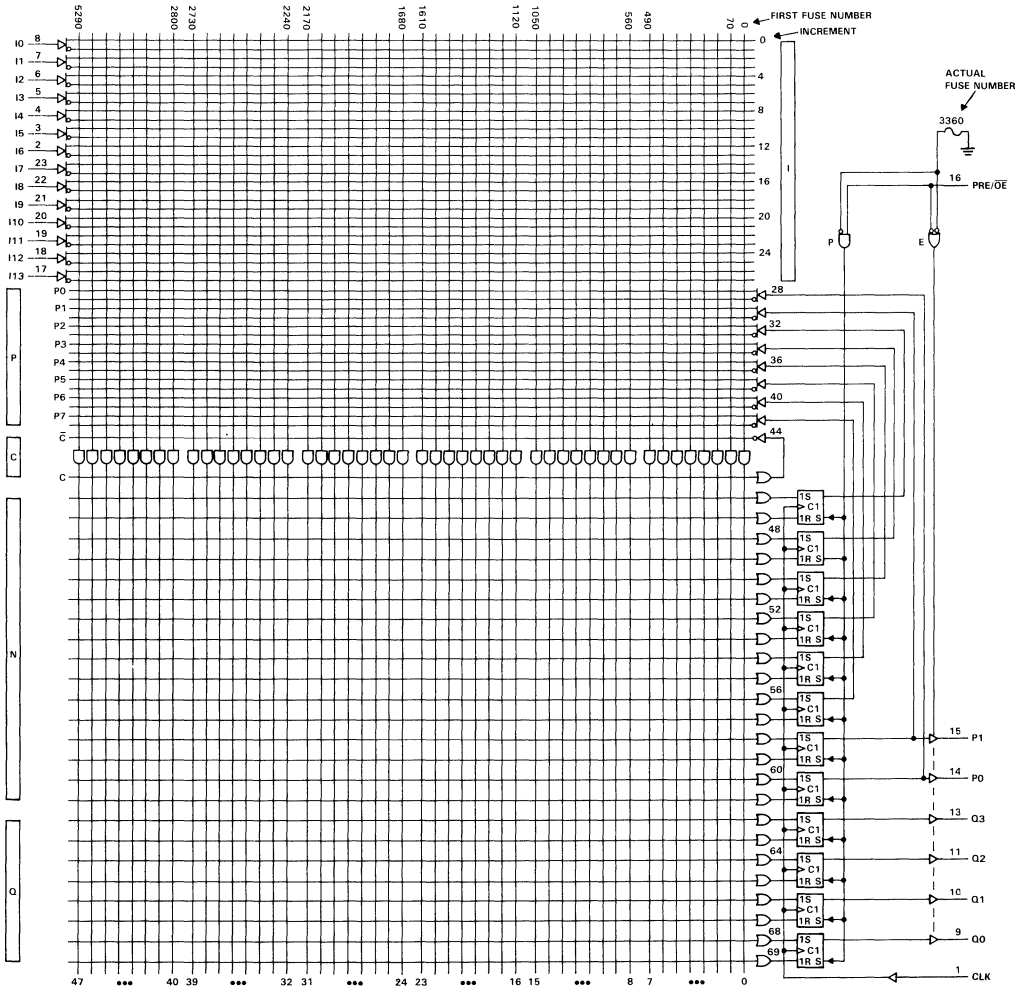


~ denotes fused inputs

timing diagram



logic diagram



NOTES: 1. All AND gate inputs with a blown link float to the high level.
2. All OR gate inputs with a blown link float to the low level.
3. Fuse Number = First Fuse Number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 3) . . . . . 7 V
Input voltage (see Note 3) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 3) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 3: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency†	1 thru 48 product terms without C-array‡	0		40	MHz
		1 thru 48 product terms with C-array	0		25	
t_w	Pulse duration	Clock high or low	12			ns
		Preset	18			
t_{su}	Setup time before CLK↑, 1 thru 48 product terms	Without C-array	25			ns
		With C-array	40			
t_{su}	Setup time, Preset low (inactive) before CLK↑§		10			ns
t_h	Hold time, input after CLK↑		0			ns
T_A	Operating free-air temperature		−55		125	°C

†The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.
‡The C-array is the single sum term that is complemented and fed back to the AND array.
§After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			25	μA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.25	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0.5 V	−30		−250	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_{CC}	V_{CC} = 5.5 V, PRE/$\overline{OE}$ input at GND,	V_I = 4.5 V, Outputs open		90	160	mA

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§	Without C array				40	70		MHz
	With C array				25	45		
t_{pd}		CLK↑	Q	R1 = 390 Ω,		10	20	ns
t_{pd}		PRE↑	Q	R2 = 750 Ω,		8	25	ns
t_{pd}¶		V_{CC}↑	Q	See Figure 3		0	15	ns
t_{en}		OE↓	Q			10	25	ns
t_{dis}		OE↑	Q			5	15	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.
§f_{max} is independent of the internal programmed configuration and the number of product terms used.
¶This parameter is guaranteed but not tested.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 3) . . . . . 7 V
Input voltage (see Note 3) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 3) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 3: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency†	1 thru 48 product terms without C-array‡	0		50	MHz
		1 thru 48 product terms with C-array	0		30	
t_w	Pulse duration	Clock high or low	10			ns
		Preset	15			
t_{su}	Setup time before CLK↑, 1 thru 48 product terms	Without C-array	15			ns
		With C-array	30			
t_{su}	Setup time, Preset low (inactive) before CLK↑§		8			ns
t_h	Hold time, input after CLK↑		0			ns
T_A	Operating free-air temperature		0		75	°C

†The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.
‡The C-array is the single sum term that is complemented and fed back to the AND array.
§After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4	3		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.37	0.5	V
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			25	μA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.25	mA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.25 V	−30		−112	mA
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V			−20	μA
I_{CC}	V_{CC} = 5.25 V, PRE/$\overline{OE}$ input at GND,	V_I = 4.5 V, Outputs open		90	160	mA

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§	Without C array				50	70		MHz
	With C array				30	45		
t_{pd}		CLK↑	Q	R1 = 500 Ω,		10	15	ns
t_{pd}		PRE↑	Q	R2 = 500 Ω,		8	20	ns
t_{pd}		V_{CC}↑	Q	See Figure 3		0	10	ns
t_{en}		OE↓	Q			10	20	ns
t_{dis}		OE↑	Q			5	10	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.
§f_{max} is independent of the internal programmed configuration and the number of product terms used.

programming information

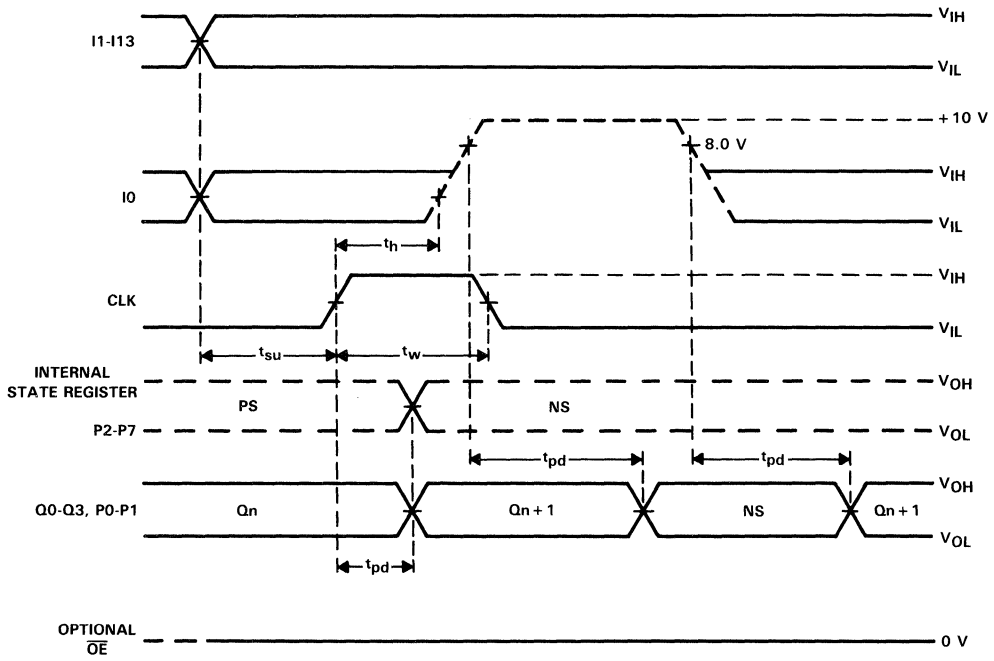
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

diagnostics

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state register. When I0 (pin 9) is held at 10 V, the state register bits P2-P7 will appear at the Q0-Q3 and P0-P1 outputs. The contents of the registers, Q0-Q3, and P0-P1 remain unchanged.

diagnostics waveforms



PS = Present State
NS = Next State

test array

A test array that consists of product lines 48 and 49 has been added to these devices to allow testing prior to programming. The test array is factory programmed as shown below. Testing is accomplished by connecting Q0-Q3 to I10-I13, PRE/$\overline{OE}$ to GND, and applying the proper input signals as shown in the timing diagram. Product lines 48 and 49 must be deleted during user programming to avoid interference with the programmed logic function.

test array program

| | | |

TIB82S167B, 82S167A COMPARISON

The Texas Instruments TIB82S167B is a 14 × 48 × 6 Field-Programmable Logic Sequencer that is functionally equivalent to the Signetics 82S167A. However, the TIB82S167B is designed for a maximum speed of 50 MHz with the preset function being made conventional. As a result the TIB82S167B differs from the 82S167A in speed and in the preset recovery function.

The TIB82S167B is a high-speed version of the original 82S167A. The TIB82S167B features increased switching speeds with no increase in power. The maximum operating frequency is increased from 20 MHz to 50 MHz and does not decrease as more product terms are connected to each sum (OR) line. For instance, if all 48 product tems were connected to a sum line on the original 82S167A, the f_{max} would be about 15 MHz. The f_{max} for the TIB82S167B remains at 50 MHz regardless of the programmed configuration. In addition, the preset recovery sequence was changed to a conventional recovery sequence, providing quicker clock recovery times. This is explained in the following paragraphs.

The TIB82S167B and the 82S167A are equipped with power-up preset and asynchronous preset functions. The power-up preset causes the registers to go high during power-up. The asynchronous preset inhibits clocking and causes the registers to go high whenever the preset pin is taken high. After a power-up preset occurs, the minimum setup time from power-up to the first clock pulse must be met in order to assure that clocking is not inhibited. In a similar manner after an asynchronous preset, the preset input must return low (inactive) for a given time, t_{su}, before clocking.

The Signetics 82S167A was designed in such a way that after both power-up preset and asynchronous preset it requires that a high-to-low clock transition occur before a clocking transition (low-to-high) will be recognized. This is shown in Figure 1. The Texas Instruments TIB82S167B does not require a high-to-low clock transition before clocking can be resumed, it only requires that the preset be inactive 8 ns (preset inactive-state setup time) before the clock rising edge. See Figure 2.

The TIB82S167B, with an f_{max} of 50 MHz, is ideal for systems in which the state machine must run several times faster than the system clock. It is recommended that the TIB82S167B be used in new designs. ***However, if the TIB82S167B is used to replace the 82S167A, then the customer must understand that clocking will begin with the first clock rising edge after preset.***

SPEED DIFFERENCES

PARAMETER	82S167A SIGNETICS	TIB82S167B TI ONLY
f_{max}	20 MHz	50 MHz
t_{pd}, CLK to Q	20 ns	15 ns

TEXAS INSTRUMENTS
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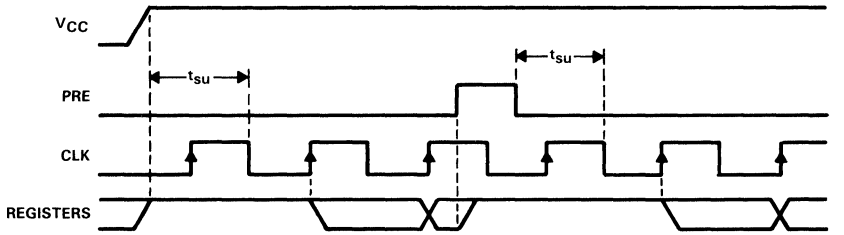


FIGURE 1. 82S167A PRESET RECOVERY OPERATION

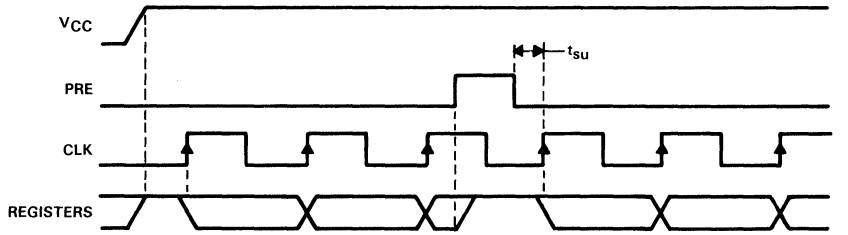
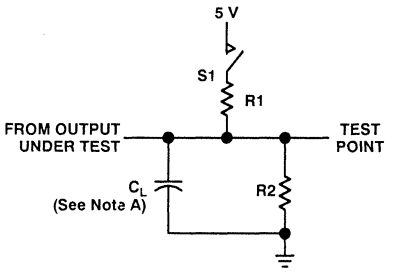
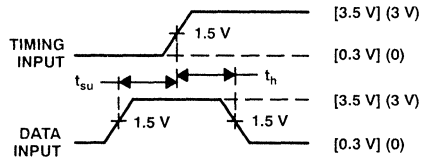


FIGURE 2. TIB82S167B PRESET RECOVERY OPERATION

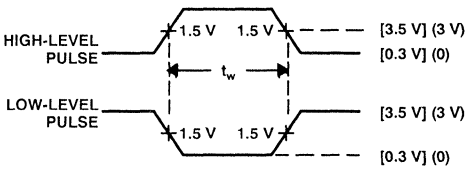
PARAMETER MEASUREMENT INFORMATION



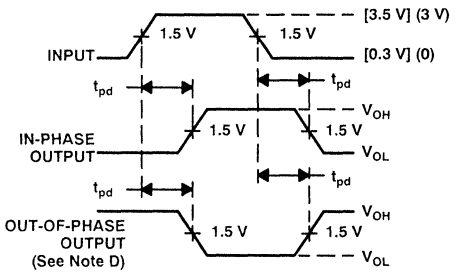
LOAD CIRCUIT FOR 3-STATE OUTPUTS



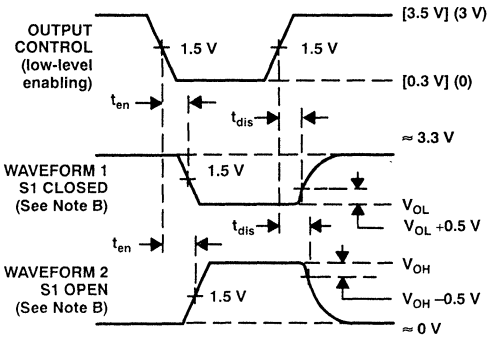
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For M suffix, use the voltage levels indicated in parentheses ( ), PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For C suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be fused for testing.

FIGURE 3

TEXAS INSTRUMENTS
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- **Standard 20-Pin PAL Family**
- **Virtually Zero Standby Power**
- **Propagation Delay . . . 55 ns Max**
- **TTL- and HC-Compatible Inputs and Outputs**
- **Preload Capability to Aid Testing**
- **Fully Tested for High Programming Yield Before Packaging**
- **Greater than 2000-V Input Protection for Electrostatic Discharge**
- **Devices in the 'J' Package Can Be Erased and Reprogrammed More Than Once**

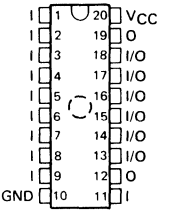
DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

description

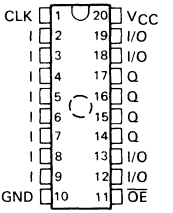
These PAL devices provide reliable, high-performance substitutes for conventional TTL and HCT logic. They are also compatible with HC logic over the V_{CC} range of 4.75 V to 5.25 V. Their easy programmability allows for quick design of "custom" functions and typically result in a more compact circuit board. Static power dissipation for these devices is negligible.

The output registers of these devices are D-type flip-flops that store data on the low-to-high transition of the clock input. The registered outputs may be disabled by taking $\overline{OE}$ high, whereas the nonregistered outputs may be disabled through the use of individual product terms. Unused inputs must always be connected to an appropriate logic level, preferably either V_{CC} or ground.

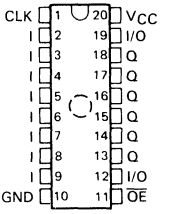
TICPAL16L8'
J OR N PACKAGE
(TOP VIEW)



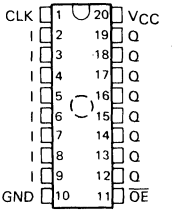
TICPAL16R4'
J OR N PACKAGE
(TOP VIEW)



TICPAL16R6'
J OR N PACKAGE
(TOP VIEW)



TICPAL16R8'
J OR N PACKAGE
(TOP VIEW)



The dotted circles represent windows found only in the J package.

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description (continued)

The programming cell consists of a floating-gate device like those used in EPROMs. All terms are initially connected. The unwanted terms are programmed out to provide the desired function. The output of a given AND gate is low if both the true and complement cells of a term are connected, and high if all related cells are programmed. Programming can be done manually but is usually achieved through the use of commercially available programming equipment.

This TICPAL16' series has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices, as exposure to ESD may result in a degradation of the device parametric performance.

The floating gate programmable cells allow these PALs to be fully programmed and tested before assembly to assure high field programming yield and functionality. They are then erased by ultraviolet light before packaging.

All devices in this series contain a security feature. Once the security cell is programmed, additional programming and verification cannot be performed. This prevents easy duplication of a design.

The TICPAL16'C series is characterized for operation from 0°C to 75°C.

erasure

The TICPAL16' (JL package) series can be erased after programming by exposure to ultraviolet light that has a wavelength of 253.7 nm (2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen $w \cdot s \cdot cm^{-2}$. The lamp should be located about 2.5 cm (1 inch) above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TICPAL16' series (JL package), the window should be covered with an opaque label.

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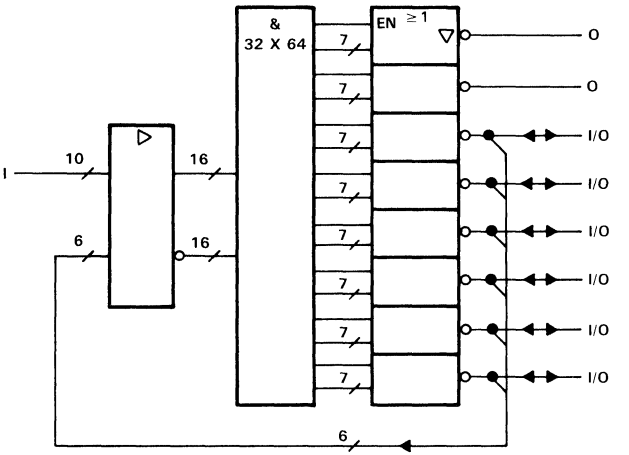
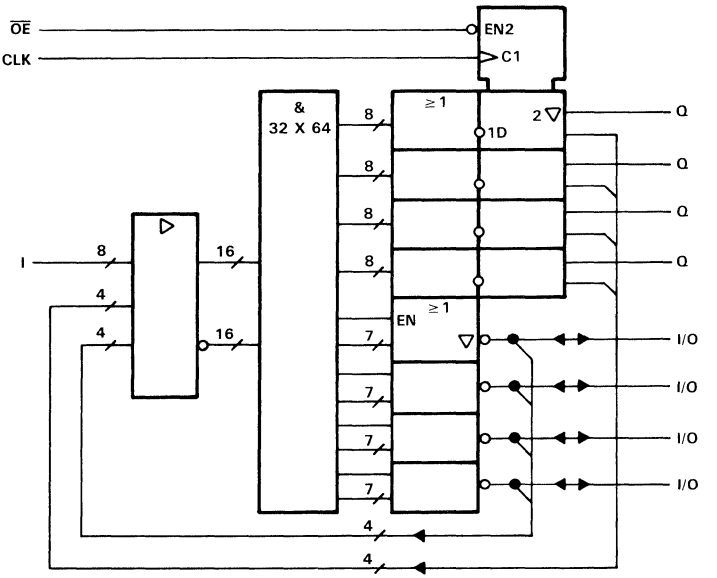
functional block diagrams (positive logic)

TICPAL16L8'

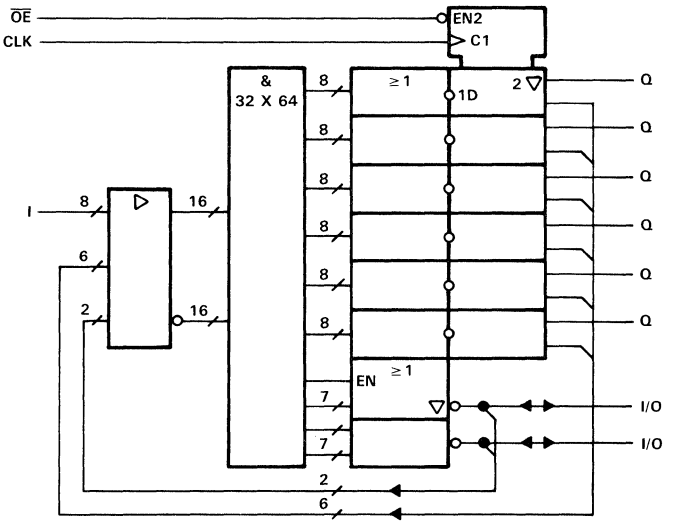


TICPAL16R4'

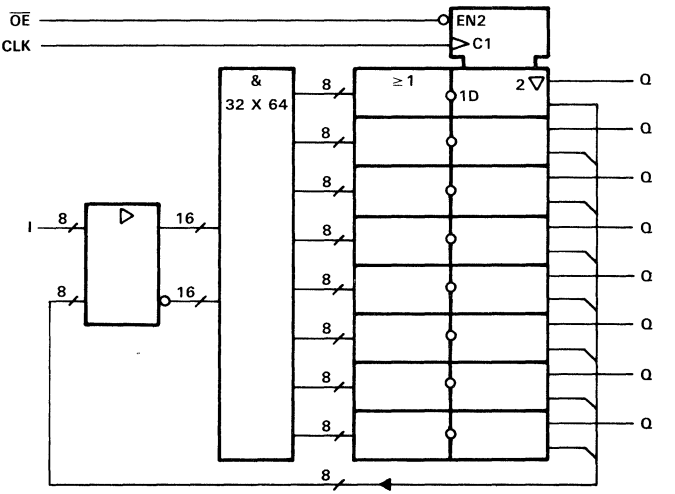


functional block diagrams (positive logic)

TICPAL16R6



TICPAL16R8



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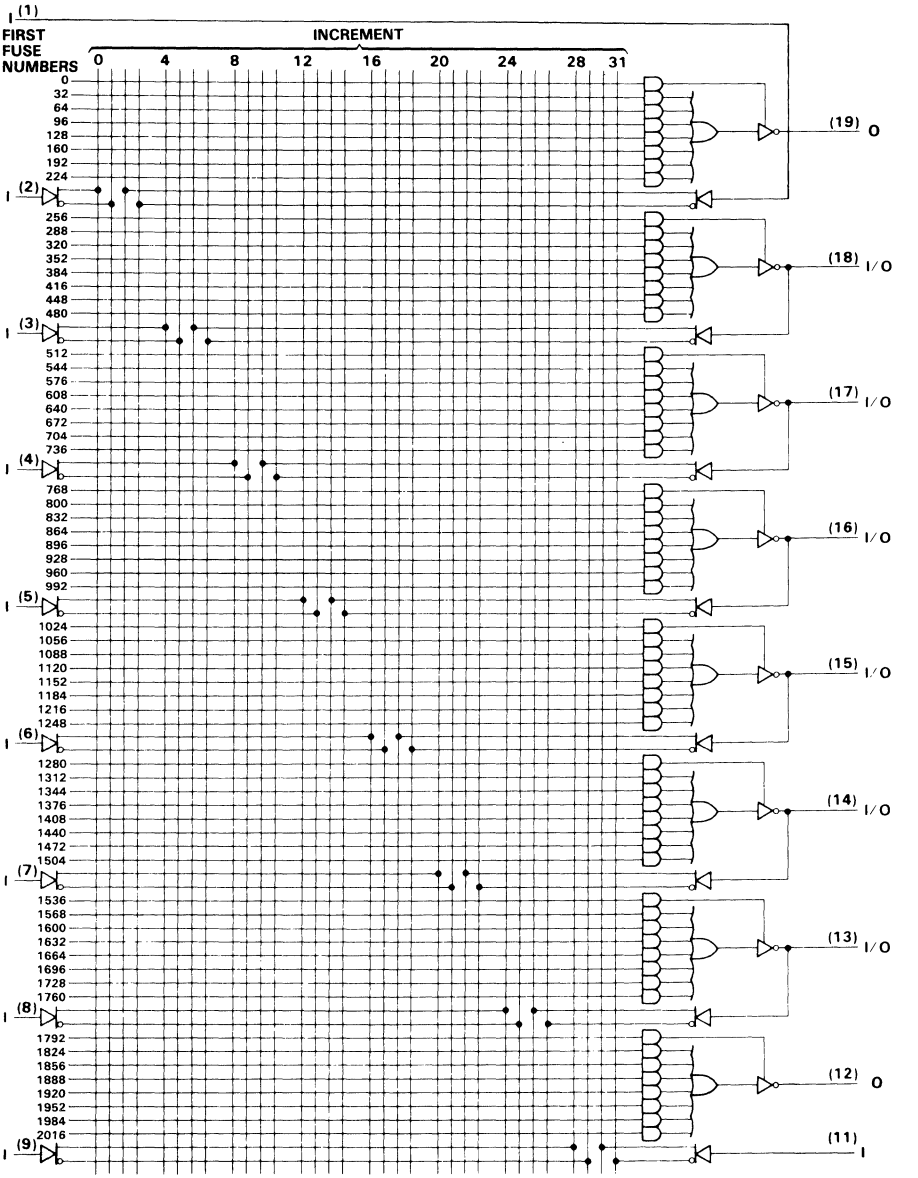
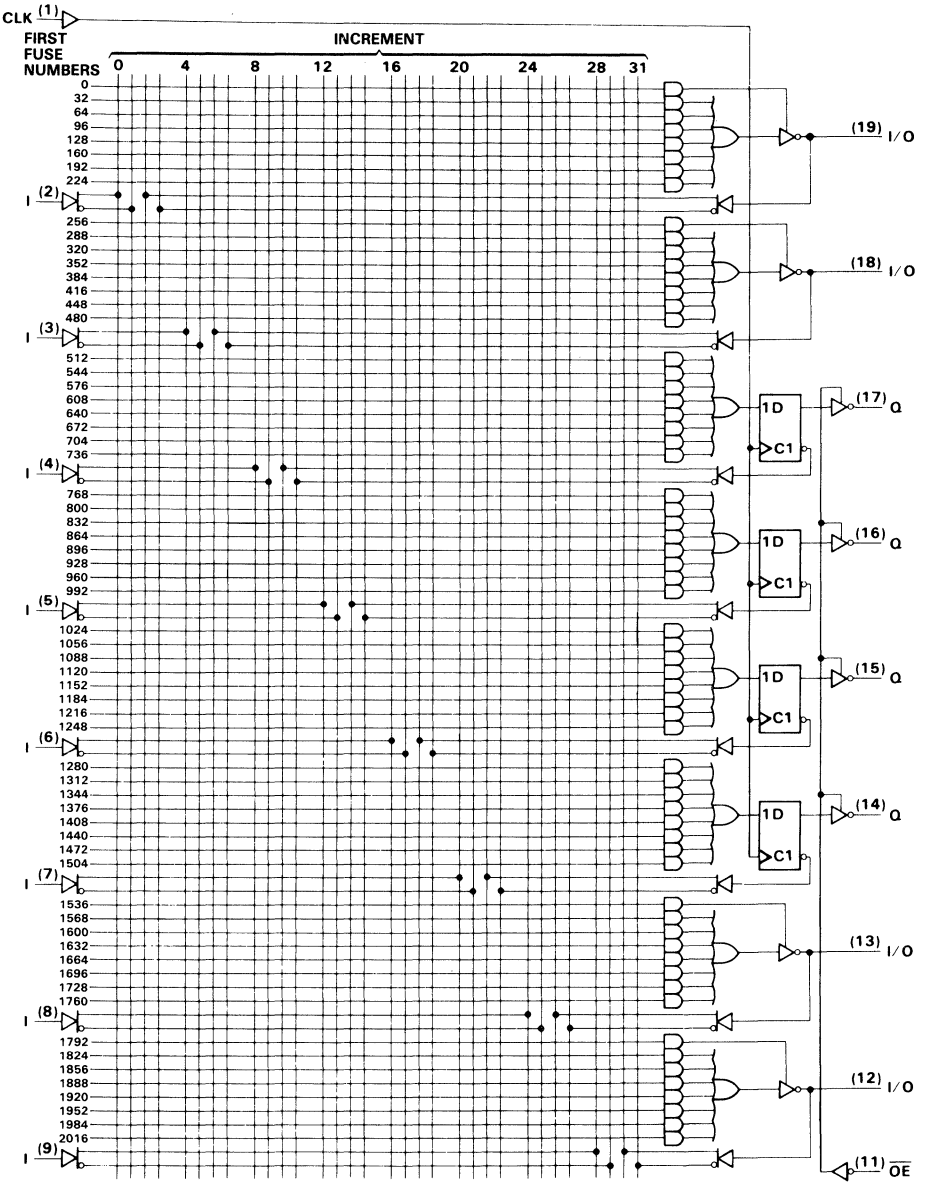
logic diagram (positive logic)



Fuse number = First Fuse number + Increment

logic diagram (positive logic)



Fuse number = First Fuse number + Increment

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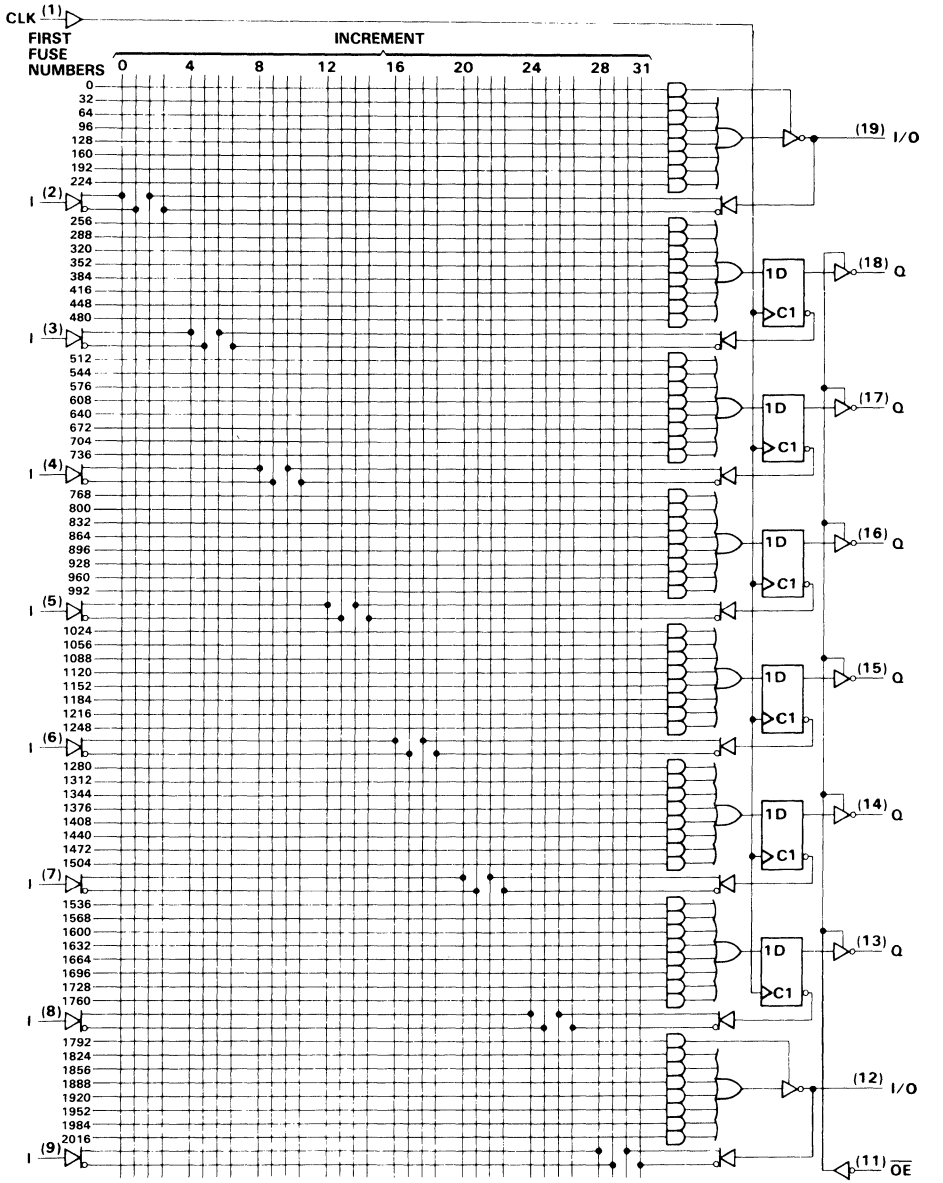
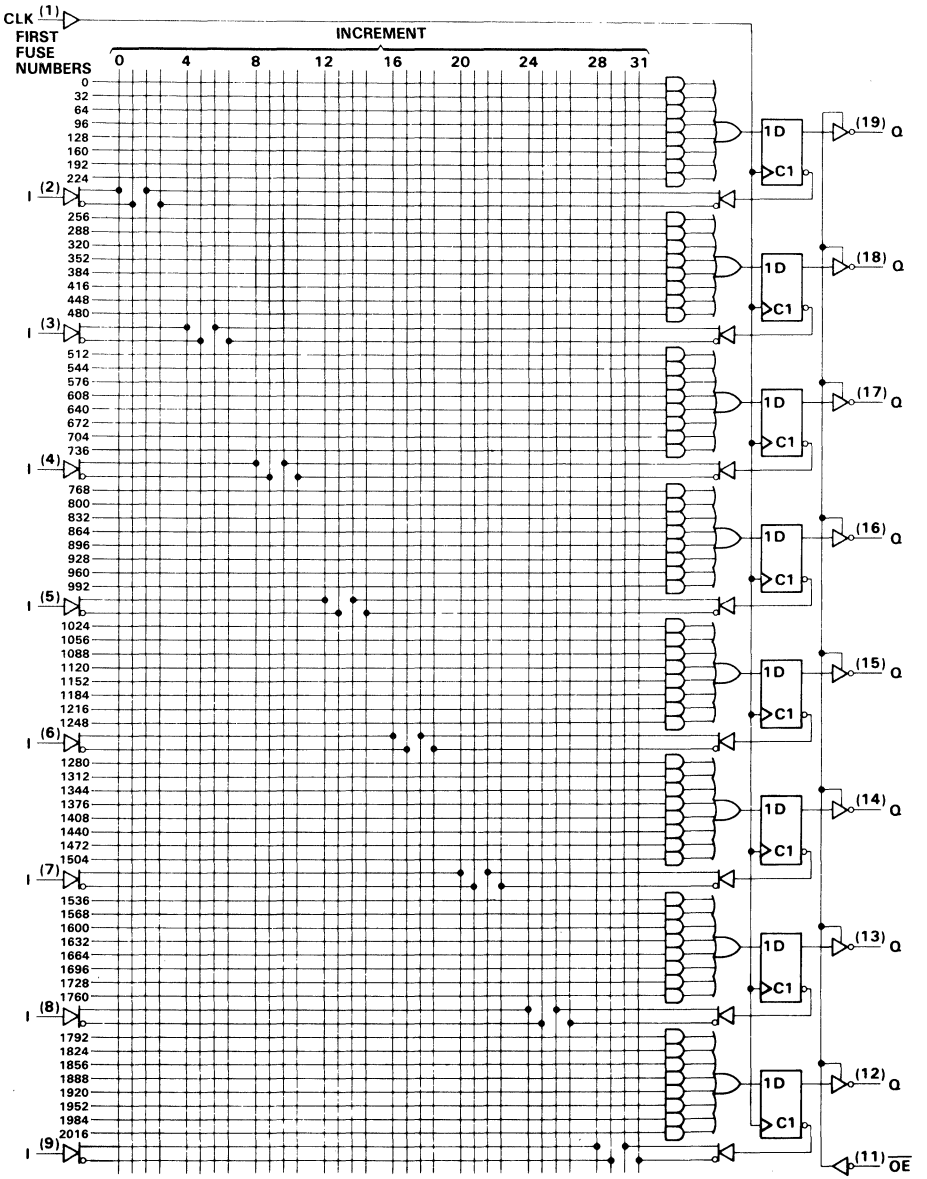
logic diagram (positive logic)



Fuse number = First Fuse number + Increment

logic diagram (positive logic)



Fuse number = First Fuse number + Increment

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I . . . . . −0.5 V to V_{CC} +0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} pin . . . . . 70 mA
Continuous current through GND pin . . . . . −200 mA
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds (J package) . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds (N package) . . . . . 260°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
t_w	Pulse duration	Clock high	20			ns
		Clock low	20			
t_{su}	Setup time, input or feedback before CLK↑		40			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature range		0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = 3.2 mA (for TTL)		4			V
	V_{CC} = 4.75 V,	I_{OH} = −4 mA (for CMOS)		3.86			
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA (for TTL)				0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 4 mA (for CMOS)				0.4	
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.4 V				10	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V				−10	μA
I_{IH}	V_{CC} = 5.25 V,	V_I = V_{CC}				10	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0				−10	μA
$I_{CC(standby)}$	V_{CC} = 5.25 V,	V_I = 0 or V_{CC},	I_O = 0			100	μA
$I_{CC(operating)}$ f	V_{CC} = 5.25 V, f = 1 MHz to 25 MHz	V_I = 0 to V_{CC},	I_O = 0,		2		mA MHz
‡ΔI_{CC}	V_{CC} 5.25 V, Other inputs at 0 V or V_{CC}	V_I = 0.5 V or 2.4 V,			1.4	3	mA
C_i	T_A = 25°C,	f = 1 MHz			6		pf

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) R1 = 200 Ω, R2 = 390 Ω, C_L = 50 pf

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}§		with feedback	16			MHz
		w/o feedback	25			
t_{pd}	I, I/O, or feedback	O or I/O		35	55	ns
t_{pd}	CLK↑	Q		15	22	ns
t_{en}	$\overline{OE}$↓	Q		15	25	ns
t_{dis}	$\overline{OE}$↑	Q		15	25	ns
t_{en}	I or I/O	Q or I/O		35	55	ns
t_{dis}	I or I/O	Q or I/O		35	55	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 or V_{CC}.

§$f_{max(\text{with feedback})} = \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$; $f_{max(\text{without feedback})} = \dfrac{1}{t_{su}}$

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preload procedure for registered outputs

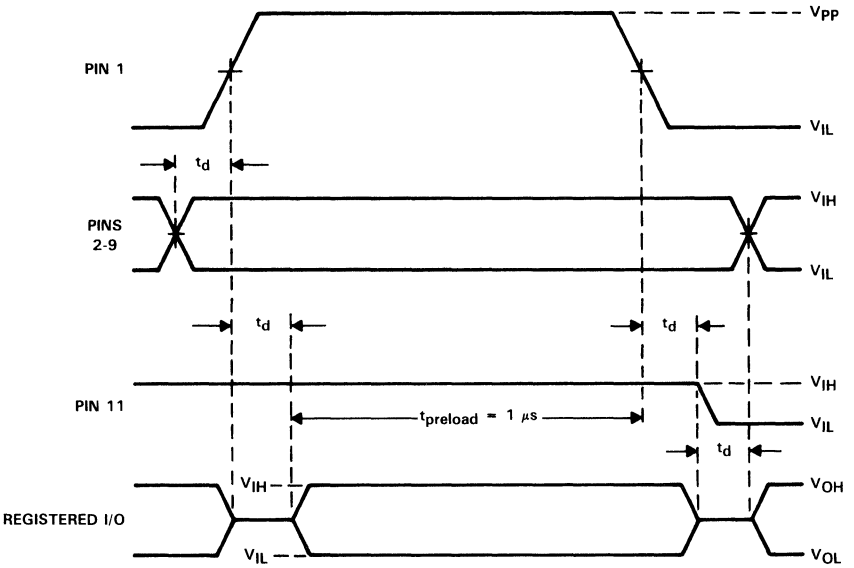
The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. All of the registers may be preloaded simultaneously by following the steps below.

Step 1. With V_{CC} at 5 V and Pin 11 at V_{IH}, raise Pin 1 to V_{IHH}.

Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.

Step 3. Lower Pin 1 to V_{IL}, then remove the output voltage. Preload can be verified by lowering Pin 11 to V_{IL} and observing the voltage level at the output pins.

preload waveforms

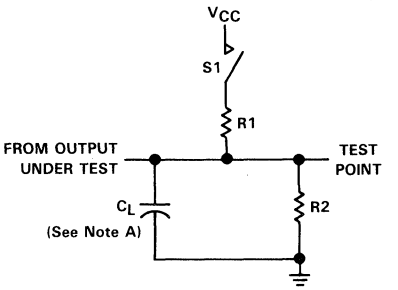


preload parameters, T_A = 25°C

	PARAMETER†	MIN	NOM	MAX	UNIT
V_{IHH}	Preload voltage on pin 1	12.5	13	13.5	V
I_{IHH}	Preload input current at pin 1	3.2	4	4.8	mA
$\Delta v/\Delta t$	Voltage ramping (V_{IHH})	50			V/µs
t_d	Setup and hold times	2			µs

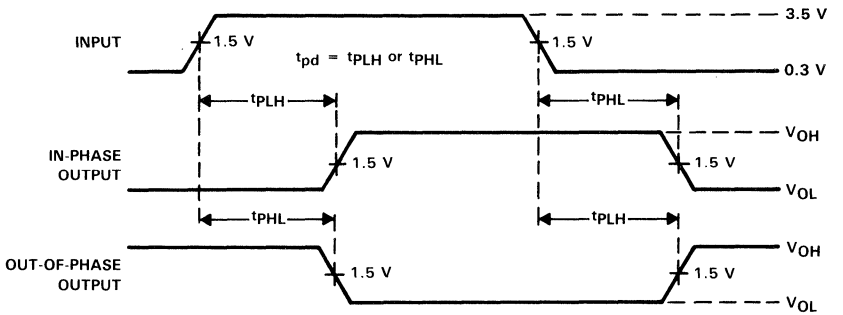
†Other test parameters and conditions are shown in recommended operating conditions and electrical characteristics tables.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L = includes probe and jig capacitance.
B. When measuring propagation times of 3-state outputs, S1 is closed.

FIGURE 1. LOAD CIRCUIT FOR THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS

NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns.

FIGURE 2. PROPAGATION DELAY TIMES, OUTPUT RISE AND FALL TIMES

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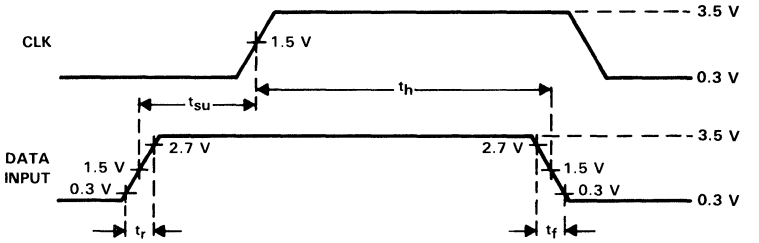
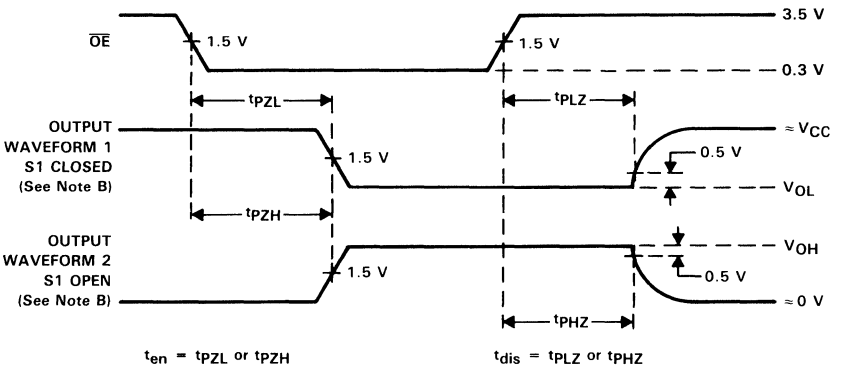
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE: Phase relationship between waveforms was chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = t_r = 6 ns, t_f = 6 ns.

FIGURE 3. SETUP AND HOLD TIMES, AND INPUT RISE AND FALL TIMES

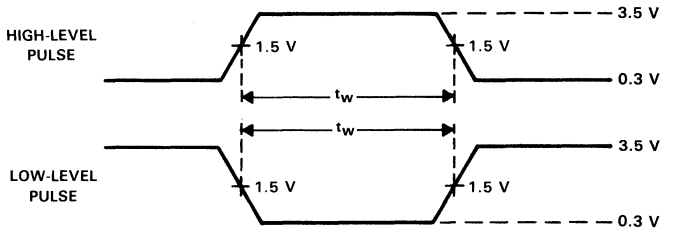


VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r = 6 ns.
B. For clock inputs, f_{max} is measured with input duty cycle = 50%.

FIGURE 5. PULSE DURATIONS

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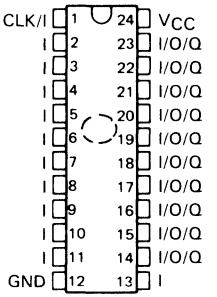
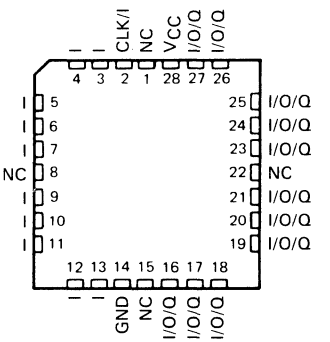
D3323, SEPTEMBER 1989—REVISED DECEMBER 1989

- 24-Pin Advanced CMOS PAL
- Virtually Zero Standby Power
- Propagation Delay Time
  - 25 ns . . . Turbo Mode
  - 35 ns . . . Zero-Power Mode
- Variable Product Term Distribution Allows More Complex Functions to Be Implemented
- Each Output Is User-Programmable for Registered or Combinatorial Operation, Polarity, and Output Enable Control
- Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability
- Preload Capability on All Registered Outputs Allows for Improved Device Testing
- UV Light Erasable Cell Technology Allows for:
  - Reconfigurable Logic
  - Reprogrammable Cells
  - Full Factory Testing for Guaranteed 100% Yields
- Programmable Design Security Bit Prevents Copying of Logic Stored in Device
- Package Options Include Plastic DIP and Chip Carrier [for One-Time-Programmable (OTP) Devices] and Ceramic Dual-In-Line Windowed Package

JT AND NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection
Pin assignments in operating mode

description

This CMOS PAL device features variable product terms, flexible outputs, and virtually zero standby power. It combines TI's EPIC ™ (Enhanced Processed Implanted CMOS) process with ultraviolet-light-erasable EPROM technology. Each output has an OLM (Output Logic Macrocell) configuration allowing for user definition of the output type. This PAL provides reliable, low-power substitutes for numerous high-performance TTL PALs with gate complexities between 300 and 800 gates.

The 'PAL22V10Z has 12 dedicated inputs and ten user-definable outputs. Individual outputs can be programmed as registered or combinational and inverting or noninverting as shown in the Output Logic Macrocell (OLM) diagram. These ten outputs are enabled through the use of individual product terms.

The variable product-term distribution on this device removes rigid limitation to a maximum of eight product terms per output. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. The variable allocation of product terms allows for far more complex functions to be implemented in this device than in previously available devices.

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description (continued)

With features such as the programmable OLMs and the variable product-term distribution, the TICPAL22V10Z offers quick design and development of custom LSI functions. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs can be implemented with this device.

Design complexity is enhanced by the addition of synchronous set and asynchronous reset product terms. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0 independently of the clock. The output logic level after set or reset will depend on the polarity selected during programming.

Output registers of this device can be preloaded to any desired state during testing, thus allowing for full logical verification during product testing.

The TICPAL22V10Z has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.6. However, care should be exercised in handling these devices, as exposure to ESD may result in a degradation of the device parametric performance.

The floating gate programmable cells allow these PAL devices to be fully programmed and tested before assembly to assure high field programming yield and functionality. They are then erased by ultraviolet light before packaging.

The TICPAL22V10Z-25C and TICPAL22V10Z-35C are characterized for operation from 0°C to 75°C.

design security

The 'PAL22V10Z contains a programmable design security cell. Programming this cell will disable the read verify and programming circuitry protecting the design from being copied. The security cell is usually programmed after the design is finalized and released to production. A secured device will verify as if every location in the device is programmed. Because programming is accomplished by storing an invisible charge instead of opening a metal link, the '22V10Z cannot be copied by visual inspection. Once a secured device is fully erased, it can be reprogrammed to any desired configuration.

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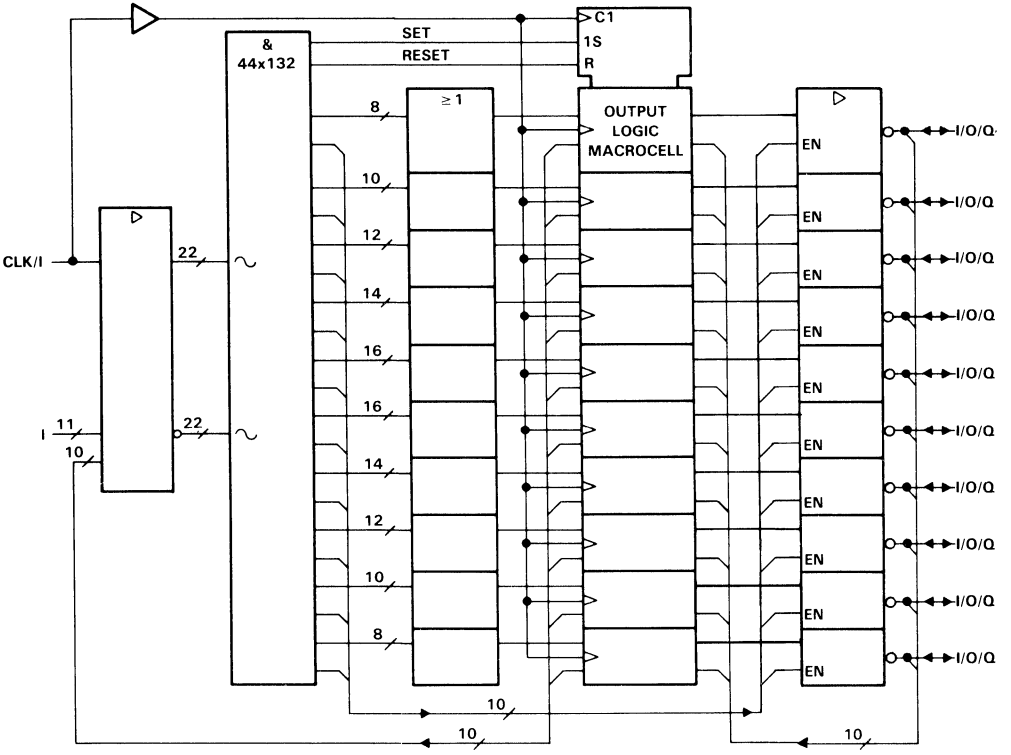
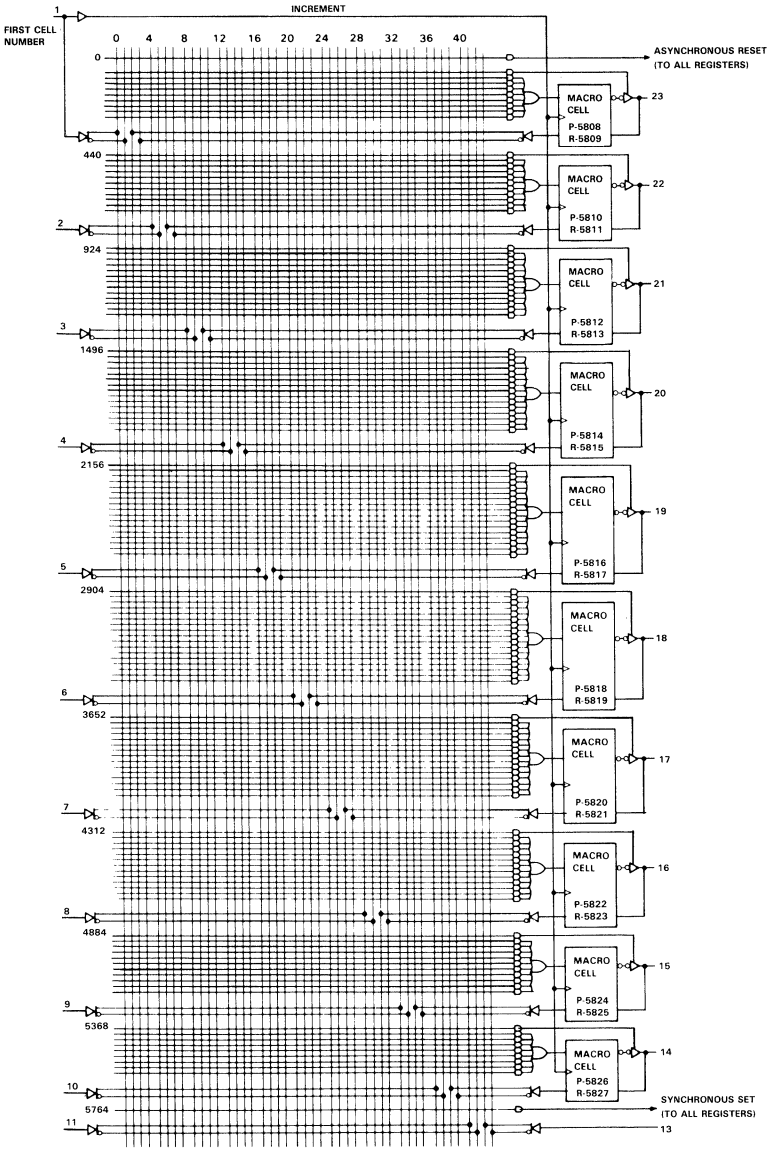
functional block diagram (positive logic)



~ denotes programmable cell inputs

logic diagram (positive logic)



Programmable Cell Number = First Cell Number + Increment

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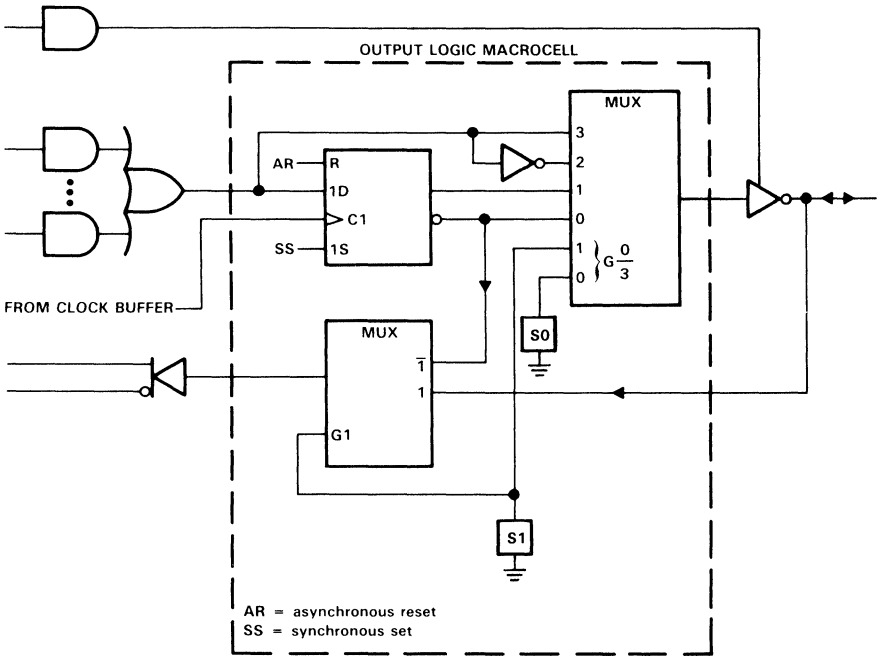
output logic macrocell (OLM) description

A great amount of architectural flexibility is provided by the user-configurable macrocell output options. The macrocell consists of a D-type flip-flop and two select multiplexers. The D-type flip-flop operates like a standard TTL D-type flip-flop. The input data is latched on the low-to-high transition of the clock input. The Q and $\overline{Q}$ outputs are made available to the output select multiplexer. The asynchronous reset and synchronous set controls are available in all flip-flops.

The select multiplexers are controlled by programmable cells. The combination of these programmable cells will determine which macrocell functions are implemented. It is this user control of the architectural structure that provides the generic flexibility of this device.

output logic macrocell diagram

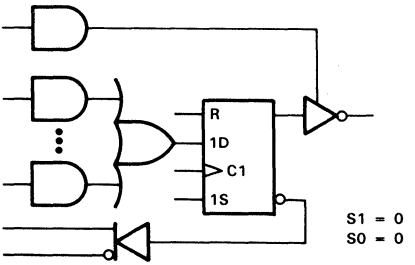


output logic macrocell options

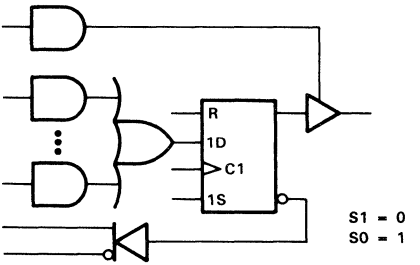
MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

CELL SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

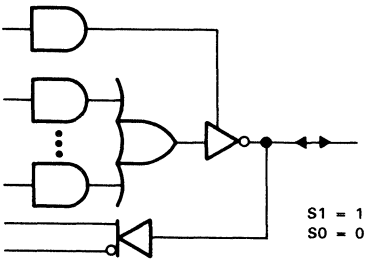
0 = erased cell 1 = programmed cell
S1 and S0 are select-function cells as shown in the output logic macrocell diagram.



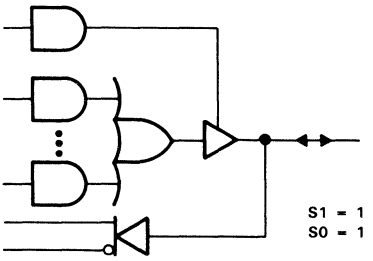
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 to V_{CC} + 0.5 V
Input diode current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output diode current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±40 mA
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: FN or NT package . . . . . 260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: JT package . . . . . 300°C
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1: This rating applies except during programming and preload cycles.

recommended operating conditions

			−25C			−35C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Driving TTL			−3.2			−3.2	mA
		Driving CMOS			−4			−4	
I_{OL}	Low-level output current	Driving TTL			16			16	mA
		Driving CMOS			4			4	
t_w	Pulse duration	CLK high	10			15			ns
		CLK low	10			15			ns
		Asynchronous reset	20			25			ns
t_{su}	Setup time, turbo mode	Input or feedback	17			25			ns
		Asynchronous reset inactive	20			30			
		Synchronous preset inactive	20			30			
t_{su}	Setup time, zero-power mode	Input or feedback	25			35			ns
		Asynchronous reset inactive	30			40			
		Synchronous preset inactive	30			40			
t_h	Hold time	Input or feedback	0			0			ns
T_A	Operating free-air temperature		0		75	0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		-25C			-35C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	V_{CC} = 4.75 V, I_{OH} = −3.2 mA for TTL		4	4.8		4	4.8		V
	V_{CC} = 4.75 V, I_{OH} = −4 mA for CMOS		3.86	4.7		3.86	4.7		V
V_{OL}	V_{CC} = 4.75 V, I_{OL} = 16 mA for TTL			0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V, I_{OL} = 4 mA for CMOS			0.07	0.4		0.07	0.4	V
I_{OZH}	V_{CC} = 5.25 V, V_O = 2.7 V			0.01	10		0.01	10	μA
I_{OZL}	V_{CC} = 5.25 V, V_O = 0.5 V			−0.01	−10		−0.01	−10	μA
I_{IH}	V_{CC} = 5.25 V, V_I = 5.25 V			0.01	10		0.01	10	μA
I_{IL}	V_{CC} = 5.25 V, V_I = 0.5 V			−0.01	−10		−0.01	−10	μA
I_O‡	V_{CC} = 5.25 V, V_O = 0.5 V		−30	−45	−90	−30	−45	−90	mA
I_{CC} (Zero-power mode)	V_{CC} = 5.25 V, Outputs open§	V_I = 0 or V_{CC},		10	100		10	100	μA
C_i	V_I = 2 V, f = 1 MHz	All inputs		6			6		pF
		All I/O pins		10			10		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	-25C			-35C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}¶	Without feedback			50	66		33	47		MHz
	With feedback			28.5	55		20	38		
t_{pd}	Turbo mode	I, I/O	O, I/O		16	25		22	35	ns
	Zero-power mode				21	35		28	45	
t_{pd}	Turbo mode	Asynchronous RESET	Q		18	30		24	40	ns
	Zero-power mode				23	40		31	50	
t_{pd}		CLK↑	Q		10	18		14	25	ns
t_{en}	Turbo mode	I, I/O	I, Q, I/O		15	25		21	35	ns
	Zero-power mode				20	35		27	45	
t_{dis}	Turbo mode	I, I/O	I, Q, I/O		15	25		21	35	ns
	Zero-power mode				17	35		25	45	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account.

§Disabled outputs are tied to GND or V_{CC}.

¶f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$; f_{max} (without feedback) = $\frac{1}{t_w\text{(hi)} + t_w\text{(low)}}$

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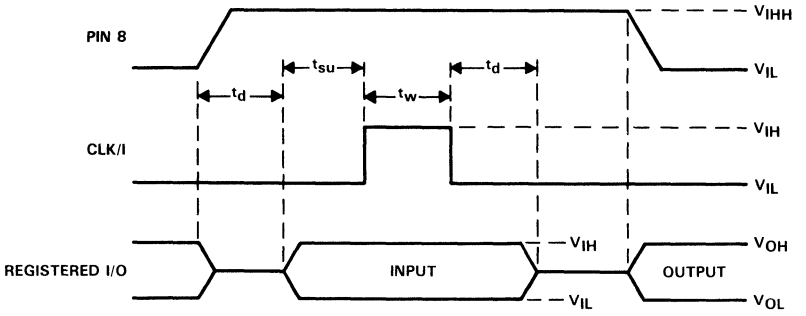
preload procedure for registered outputs

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below. The output level depends on the polarity selected during programming.

Step 1. With V_{CC} at 5 volts and pin 1 at V_{IL}, raise pin 8 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 8 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 2)



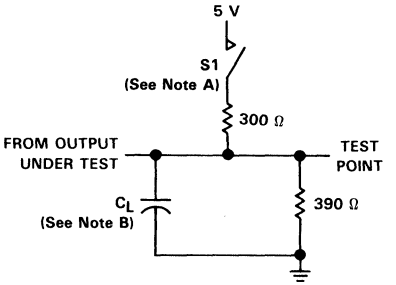
NOTE 2: $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

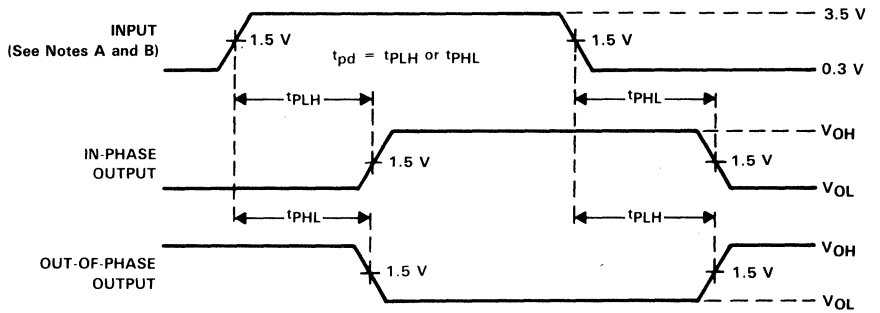
Complete programming specification, algorithms, and the lastest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} and 5 pF for t_{dis}.

FIGURE 1. LOAD CIRCUIT FOR THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS

NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = t_f = 2 ns.

FIGURE 2. PROPAGATION DELAY TIMES, OUTPUT RISE AND FALL TIMES

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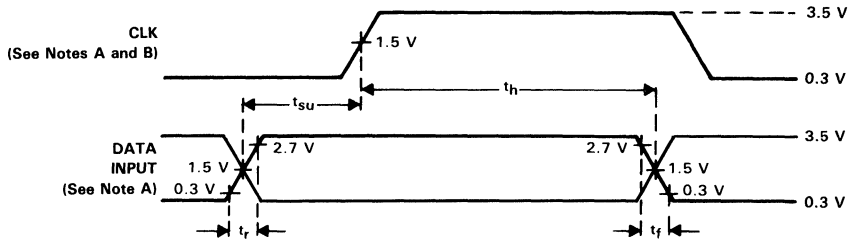
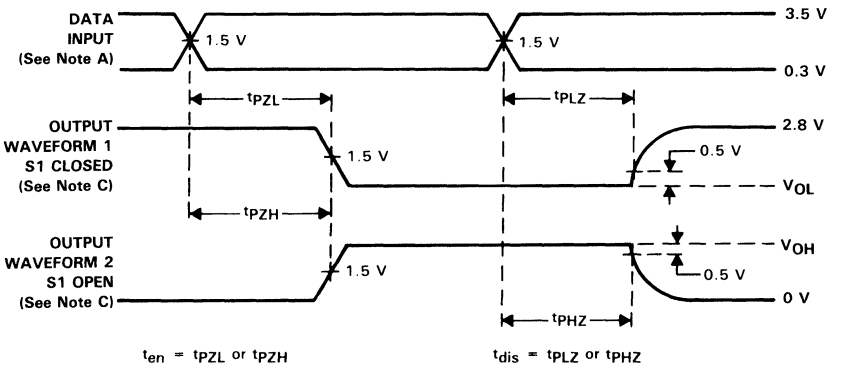
PARAMETER MEASUREMENT INFORMATION



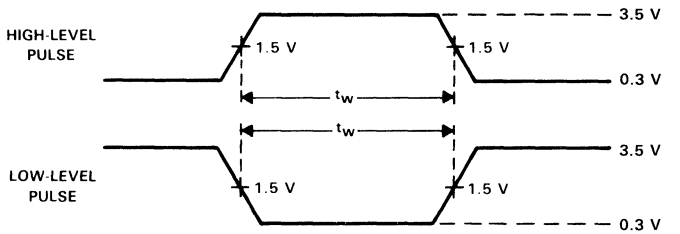
VOLTAGE WAVEFORMS

FIGURE 3. SETUP AND HOLD TIMES, AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS



VOLTAGE WAVEFORMS

FIGURE 5. PULSE DURATIONS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = t_f = 2 ns.
B. For clock inputs, f_{max} is measured with input duty cycle = 50%
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

special design features

True CMOS Outputs: Each TICPAL22V10Z output is designed with a P-channel pull-up transistor and an N-channel pull-down transistor, a true CMOS output with rail-to-rail output switching. This provides direct interface to CMOS logic, memory, or ASIC devices without the need for a pull-up resistor. The CMOS output has 16-mA drive capability, which makes the TICPAL22V10Z an ideal substitute for bipolar PALs. The electrical characteristics of this device show the output under both CMOS and TTL conditions.

Simultaneous Switching: High-performance CMOS devices often have output glitches on nonswitched outputs when a large number of outputs are switched simultaneously. This glitch is commonly referred to as "ground bounce" and is most noticeable on outputs held at V_{OL} (low-level output voltage). Ground bounce is caused by the voltage drop across the inductance in the package lead when current is switched ($dv \propto I \times di/dt$).

One solution is to restrict the number of outputs that can switch simultaneously. Another solution is to change the device pinout such that the ground is located on a low-inductance package pin. TI opted for a third option in order to maintain pinout compatibility and eliminate functional constraints. This option controls the output transistor turn-on characteristics and puts a limit on the instantaneous current available to the load, much like the I_{OS} resistor in a TTL circuit.

Wake-Up Features: The TICPAL22V10Z employs input signal transition detection techniques to power-up the device from the standby-power mode. The transition detector monitors all inputs, I/Os, and feedback paths. Whenever a transition is sensed, the detector activates the power-up mode. The device will remain in the power-up mode until the detector senses that the inputs and outputs have been static for about 40 ns; thereafter, the device returns to the standby mode.

Turbo Mode or Zero-Power Mode: When the turbo cell is programmed, the device will be set to the power-up mode. Therefore, the delay associated with its transition detection and power up will be eliminated. This is how the faster propagation delays and shorter setup times are obtained in the turbo mode. The turbo mode and the associated speed increase can be effectively simulated with the turbo cell erased, if a series of adjacent input, I/O, or feedback edges occur with an interval of about 25 ns or less between these adjacent edges. Under these conditions, the TICPAL22V10Z will never have the opportunity to power down due to the frequency of the adjacent edges.

Power Dissipation: Power dissipation of the TICPAL22V10Z is defined by three contributing factors, and the total power dissipation is the sum of all three.

Standby Power: The product of V_{CC} and the standby I_{CC}. The standby current is the reverse current through the diodes that are reversed biased. This current is very small, and for circuits that remain in static condition for a long time, this low amount of current can become a major performance advantage.

Dynamic Power: The product of V_{CC} and the dynamic current. This dynamic current flows through the device only when the transistors are switching from one logic level to the other. The total dynamic current for the TICPAL22V10Z is dependent upon the users' configuration of the PAL and the operating frequency. Output loading can be a source of additional power dissipation.

Interface Power: The product of I_{CC} (interface) and V_{CC}. The total interface power is dependent on the number of inputs at the TTL V_{OH} level. The interface power can be eliminated by the addition of a pull-up resistor.

Even though power dissipation is a function of the user's device configuration and the operating frequency, the TICPAL22V10Z is a lower powered solution than either the quarter-powered or half-powered bipolar devices. The virtually zero standby power feature makes the TICPAL22V10Z the device of choice for low-duty-cycle and battery-powered applications.

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programming and erasability

Programming of the TICPAL22V10Z is achieved through floating-gate avalanche injection techniques. The charge trapped on the floating gate remains after power has been removed, allowing for the nonvolatility of the programmed data. The charge can be removed by exposure to light with wavelengths of less than 400 nm (4000 Å). The recommended erasure wavelength is 253.7 nm (2537 Å), with erasure time of 60 to 90 minutes, using a light source with a power rating of 12000 $\mu W/cm^2$ placed within 2.5 cm (1 inch) of the device.

The TICPAL22V10 is designed for programming endurance of 1000 write/erase cycles with a data retention of ten years. To guarantee maximum data retention, the window on the device should be covered by an opaque label. The fluorescent light in a room can erase a unit in three years or, in the case of a direct sunlight, erasure can be complete in one week.

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

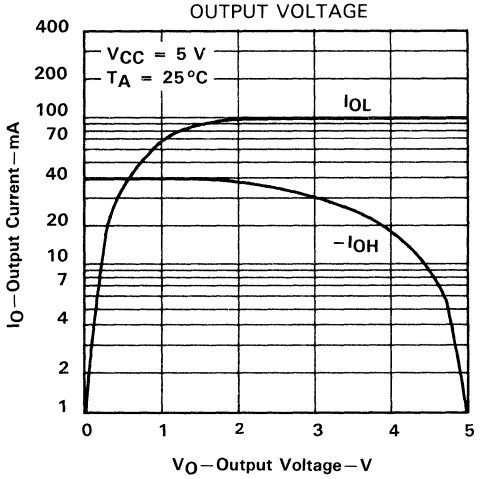

FIGURE 6

NORMALIZED SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE
(10-BIT COUNTER)

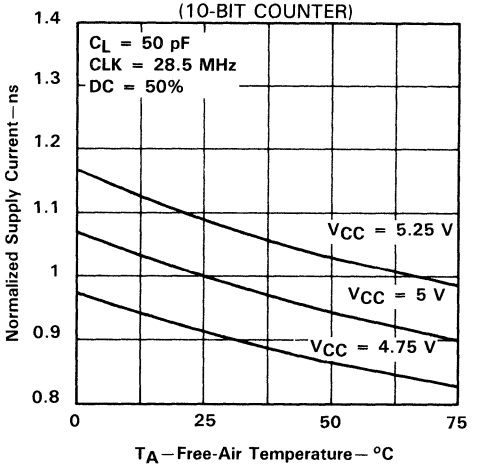

FIGURE 7

SUPPLY CURRENT
vs
CLOCK FREQUENCY
(10-BIT COUNTER)

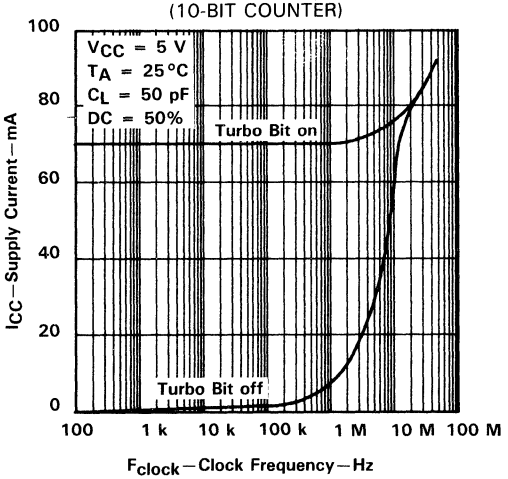

FIGURE 8

NORMALIZED PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

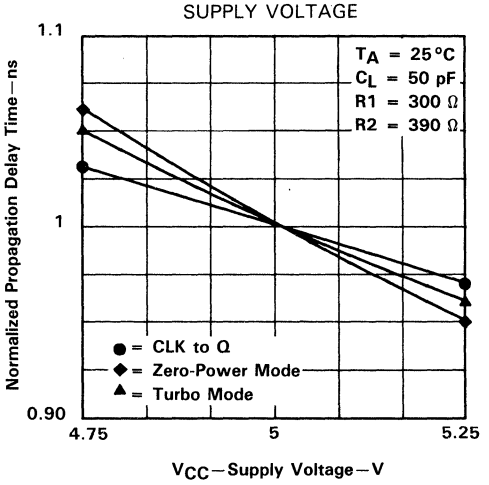

FIGURE 9

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NORMALIZED PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

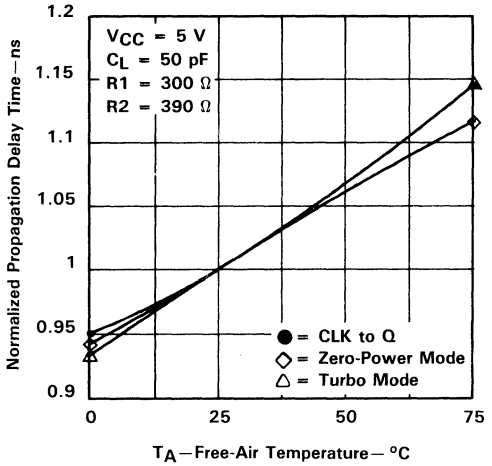


FIGURE 10

DELTA PROPAGATION TIME
vs
LOAD CAPACITANCE

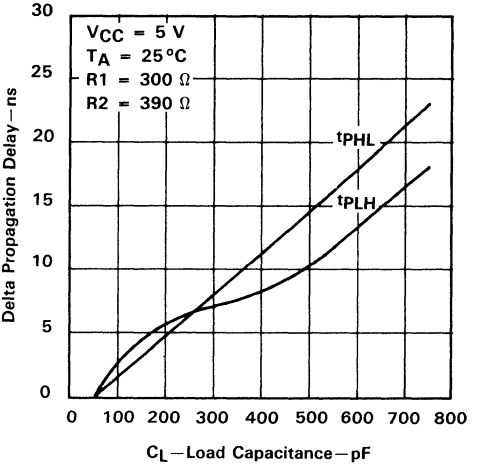


FIGURE 11

DELTA PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

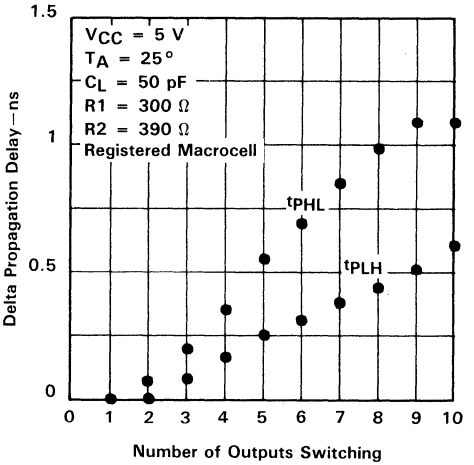


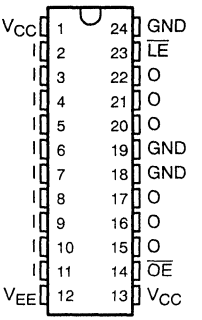
FIGURE 12

TIEPAL10H16ET6C
ECL-TO-TTL *IMPACT-X™ PAL®* TRANSLATOR CIRCUIT

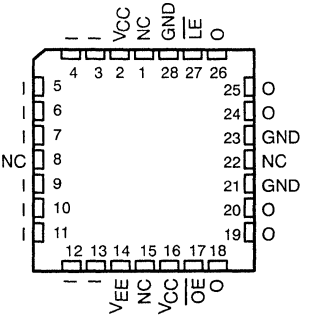
D3283, OCTOBER 1989

- **ECL 10KH Programmable Logic with ECL-to-TTL Translation**
- **ECL Control Inputs**
- **3-State TTL Outputs**
- **Reliable Titanium-Tungsten Fuses**
- **Package Options Include Both 300-mil Ceramic DIP and Plastic Chip Carrier**

JT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TIEPAL10H16ET6C combines the IMPACT-X™ (Advanced Implanted, Advanced Composed) technology with proven titanium-tungsten fuses to provide a reliable high-performance substitute for conventional ECL 10KH logic. Easy programmability allows for quick design of custom functions with increased logic density.

The TIEPAL10H16ET6C accepts ECL input levels and provides TTL output levels, making it ideal for interfacing ECL circuits with TTL circuits. It has latched outputs controlled by a Latch Enable ($\overline{LE}$) input at the ECL inputs. The 3-state outputs are enabled by an Output Enable ($\overline{OE}$) input from a single ECL input. The TTL outputs are designed for 24-mA low-level output current.

The TIEPAL10H16ET6C is provided with an output polarity fuse that, if blown, will allow an output to assume a logic high when the implemented equation is satisfied. However, when the output polarity fuse is intact and the implementation equation is satisfied, the output will assume a logic low.

PRODUCT PREVIEW

The TIEPAL10H16ET6C is equipped with a security fuse. When the security fuse is blown, additional programming and verification cannot be performed. This safeguards against easy duplication of a design.

The three GND pins must all be tied externally to an adequate ground plane for proper operation of this device.

The TIEPAL10H16ET6C is characterized for operation from 0°C to 75°C.

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IMPACT-X is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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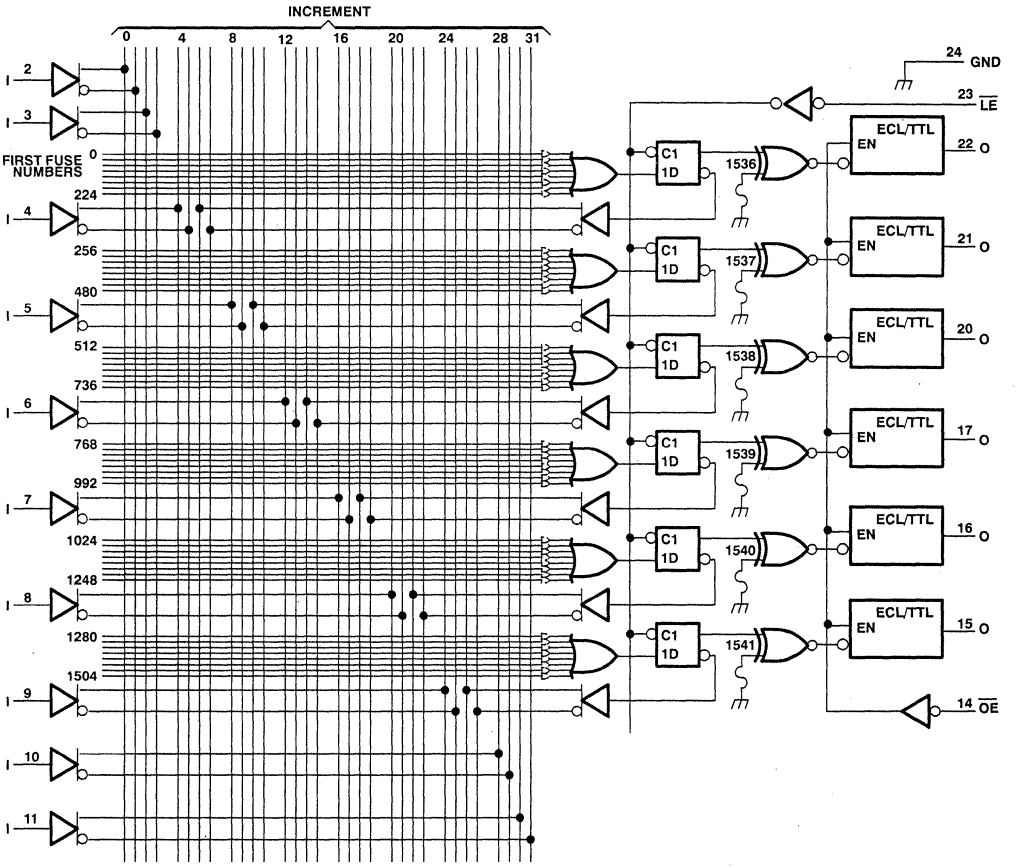
PRODUCT PREVIEW

logic diagram†



Fuse Number = First Fuse Number + Increment

† An exclusive-NOR input grounded through an intact polarity fuse is at an ECL high logic level.

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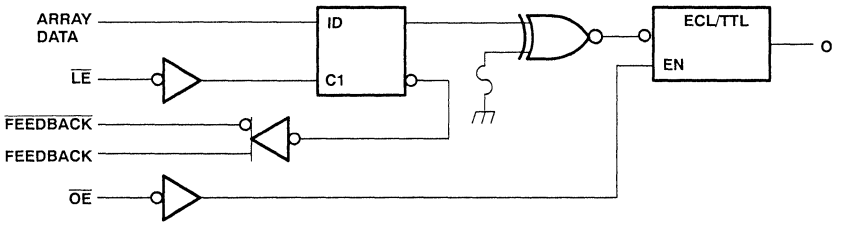
FUNCTION TABLE

INPUTS			OUTPUTS		
$\overline{OE}$	$\overline{LE}$	DATA	O†	$\overline{O}$‡	FEEDBACK
L	L	H	H	L	H
L	L	L	L	H	L
L	H	X	O_O	$\overline{O}_O$	O_O
H	H	X	Z	Z	O_O
H	L	H	Z	Z	H
H	L	L	Z	Z	L

X = Don't care
† = Polarity fuse blown
‡ = Polarity fuse intact



NOTE: An exclusive-NOR input grounded through an intact polarity fuse is at an ECL high logic level.

FIGURE 1. SIMPLIFIED LOGIC DIAGRAM (EACH OUTPUT)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

ECL supply voltage, V_{EE} (see Note 2) ..... −7 V to 0.5 V
TTL supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I ..... V_{EE} to 0.5 V
Operating free-air temperature range, T_A ..... 0°C to 75°C
Storage temperature range ..... −65°C to 150°C

NOTES: 1. These ratings apply except for programming pins during a programming cycle.
2. All voltage values are with respect to the GND pin.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
TTL supply voltage, V_{CC}		4.75	5	5.25	V
ECL supply voltage, V_{EE}		−4.94	−5.2	−5.46	V
High-level input voltage, V_{IH}	T_A = 0°C	−1.17		−0.84	V
	T_A = 25°C	−1.13		−0.81	
	T_A = 75°C	−1.07		−0.735	
Low-level input voltage, V_{IL}	T_A = 0°C	−1.95		−1.48	V
	T_A = 25°C	−1.95		−1.48	
	T_A = 75°C	−1.95		−1.45	
High-level output current, I_{OH}				−3.2	mA
Low-level output current, I_{OL}				24	mA
Pulse duration, $\overline{LE}$ high, t_w		3			ns
Setup time, data before $\overline{LE}\uparrow$, t_{su}		4			ns
Hold time, data after $\overline{LE}\uparrow$, t_h		0			ns

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	V_{CC} = 4.75 V,	$V_I = V_{IH}$min or V_{IL}max,	I_{OH} = −3.2 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	$V_I = V_{IH}$min or V_{IL}max,	I_{OL} = 24 mA		0.3	0.5	V
I_{IH}‡	V_{EE} = −5.46 V,	$V_I = V_{IH}$max				220	µA
I_{IL}‡	V_{EE} = −4.94 V,	$V_I = V_{IL}$min		0.5			µA
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V				20	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V				−20	µA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0		−30		−130	mA
I_{EE}	V_{EE} = −5.46 V					−220	mA
I_{CC} (Total)	V_{CC} = 5.25 V					20	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{en}	$\overline{OE}$	O	R1 = 200 Ω, R2 = 200 Ω, See Figure 1		4		ns
t_{dis}	$\overline{OE}$	O			5		ns
t_{pd}	$\overline{LE}\downarrow$	O			5		ns
t_{pd}	I or feedback	O			6		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Measure one input at a time with the other inputs open.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

¶ All inputs and outputs open.

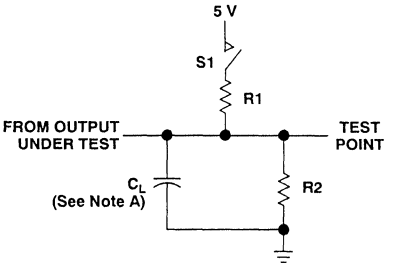
NOTES: 3. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.

4. This device has been designed to meet the dc and ac specifications after thermal equilibrium has been achieved. The device is in a test socket or mounted on a printed circuit board and transverse air flow of greater than 500 linear ft/min is maintained.

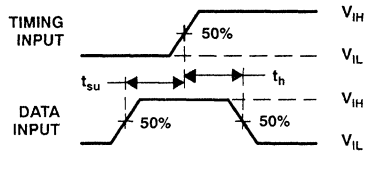
PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

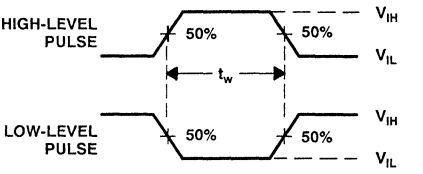
PARAMETER MEASUREMENT INFORMATION



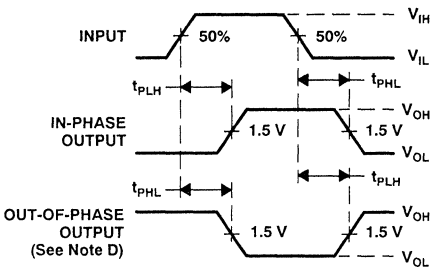
LOAD CIRCUIT FOR 3-STATE OUTPUTS



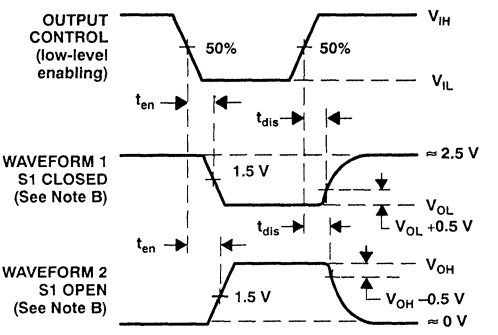
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 0.7$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 2. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

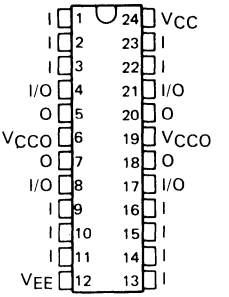
PRODUCT PREVIEW

TIEPAL10H16P8-3C
HIGH-PERFORMANCE *ExCL™PAL®* CIRCUIT

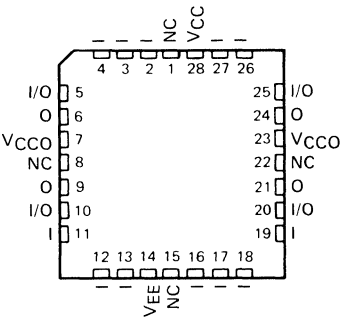
D3084, DECEMBER 1987—REVISED SEPTEMBER 1989

- **ECL 10KH PAL**
- **High-Performance Operation**
  Propagation Delay . . . 3 ns Max
- **Replacement for Conventional ECL Logic**
- **24-Pin, 300-Mil Package**
- **Reliable Titanium-Tungsten Fuses**

JT PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

This ECL PAL device combines the ExCL™ (Double Polysilicon Self-Aligned) process with the proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional ECL logic. Its easy programmability allows for quick design of "custom" functions and typically results in a more compact board. In addition, chip carriers are available for further reduction in board space.

The TIEPAL10H16P8-3 is provided with output polarity fuses. Each output remains active-high when the fuse is intact and is active-low when the fuse is blown.

The TIEPAL10H16P8-3 has 12 dedicated inputs, four standard outputs, and four I/O ports. It should be noted that with emitter-coupled outputs, a high level overrides a low level. Therefore, in order to use an I/O port as an input, the related output must be forced to a low level either through satisfying preprogrammed equations or permanently by programming.

The TIEPAL10H16P8-3 is equipped with a security fuse. Once the security fuse is blown, additional programming and verification cannot be performed. This prevents easy duplication of a design.

This device is characterized for operation from 0°C to 75°C; this temperature range is designated by a "C" suffix in the part number (TIEPAL10H16P8-3CJT).

PRODUCT PREVIEW

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PAL is a registered trademark of Monolithic Memories Inc.

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TEXAS INSTRUMENTS
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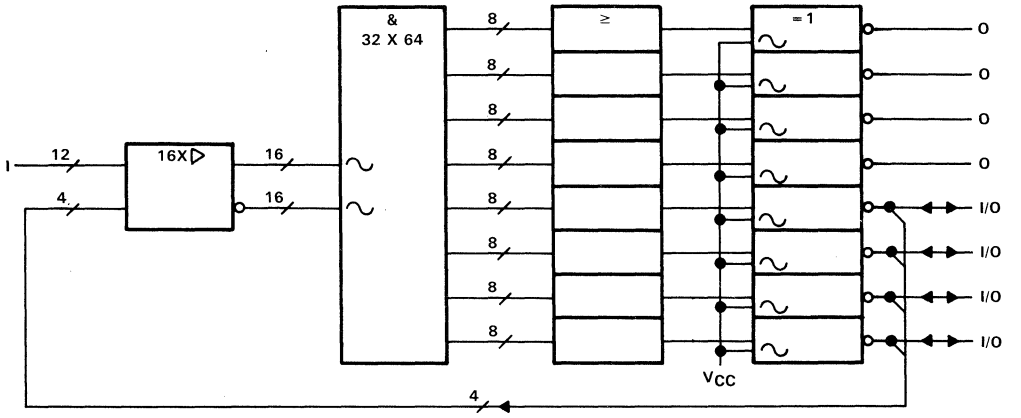
functional block diagram (positive logic)



PRODUCT PREVIEW

TEXAS INSTRUMENTS
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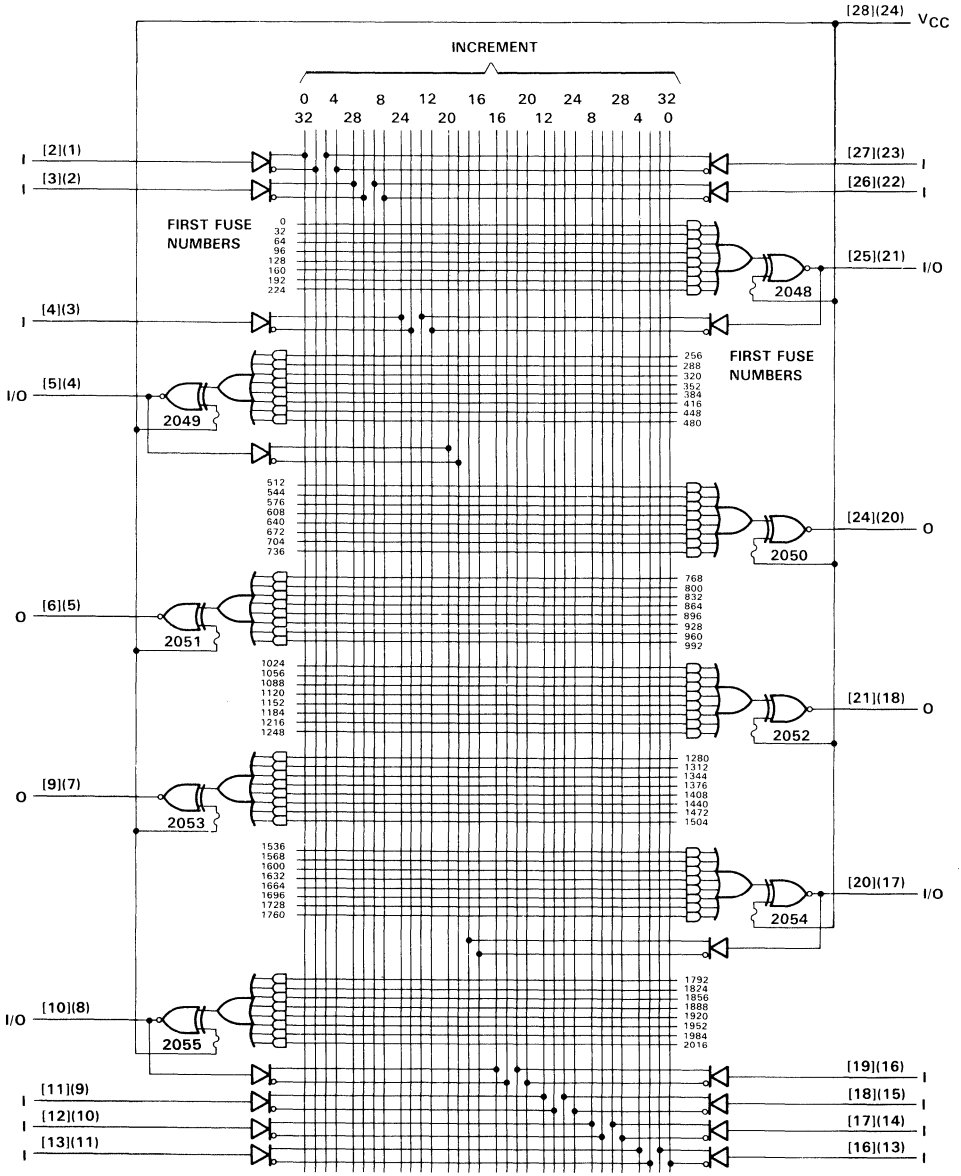
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment

NOTE: Pin numbers in [ ] are for the FK package; pin numbers in ( ) are for JT package.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Supply voltage, V_{EE} (see Note 2) . . . . . 0 V to −6.5 V
Input voltage, V_I (see Note 3) . . . . . 0 V to V_{EE}
Output current . . . . . −50 mA
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. These ratings apply except for programming pins during a programming cycle.
2. All voltage values are with respect to V_{CC} and V_{CCO}, i.e., these pins are all assumed to be at 0 volts.
3. V_I should never be more negative than V_{EE}.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{EE}	Supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	High-level input voltage	T_A = 0°C	−1.17		−0.84	V
		T_A = 25°C	−1.13		−0.81	
		T_A = 75°C	−1.07		−0.735	
V_{IL}	Low-level input voltage	T_A = 0°C	−1.95		−1.48	V
		T_A = 25°C	−1.95		−1.48	
		T_A = 75°C	−1.95		−1.45	
T_A	Operating free-air temperature		0		75	°C

NOTE 4: The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.

electrical characteristics over recommended supply voltage range at specified free-air temperature (see Notes 4 and 5)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	V_I = V_{IH}min or V_{IL}max	0°C	−1.02		−0.84	V
		25°C	−0.98	−0.895	−0.81	
		75°C	−0.92		−0.735	
V_{OL}	V_I = V_{IH}min or V_{IL}max	0°C	−1.95		−1.63	V
		25°C	−1.95		−1.63	
		75°C	−1.95	−1.79	−1.60	
I_{IH}	V_I = V_{IH}max	0°C			220	μA
		25°C			220	
		75°C			220	
I_{IL}	V_I = V_{IL}min	0°C	0.5			μA
		25°C	0.5			
		75°C	0.3			
I_{EE}	All inputs open	0°C to 75°C			−220	mA

NOTES: 4. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.
5. Each 10KH PAL has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	I, I/O, or feedback	O, I/O	See Figures 1 and 2	1		3	ns
t_r				0.7		1.5	ns
t_f				0.7		1.5	ns

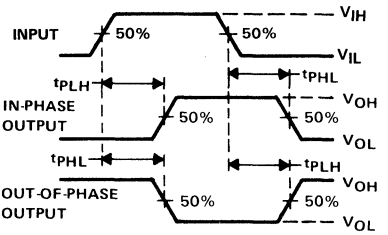
NOTE 5: Each 10KH PAL has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

PROGRAMMING INFORMATION

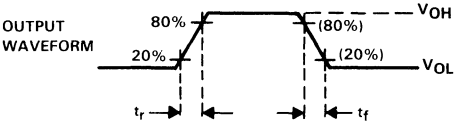
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



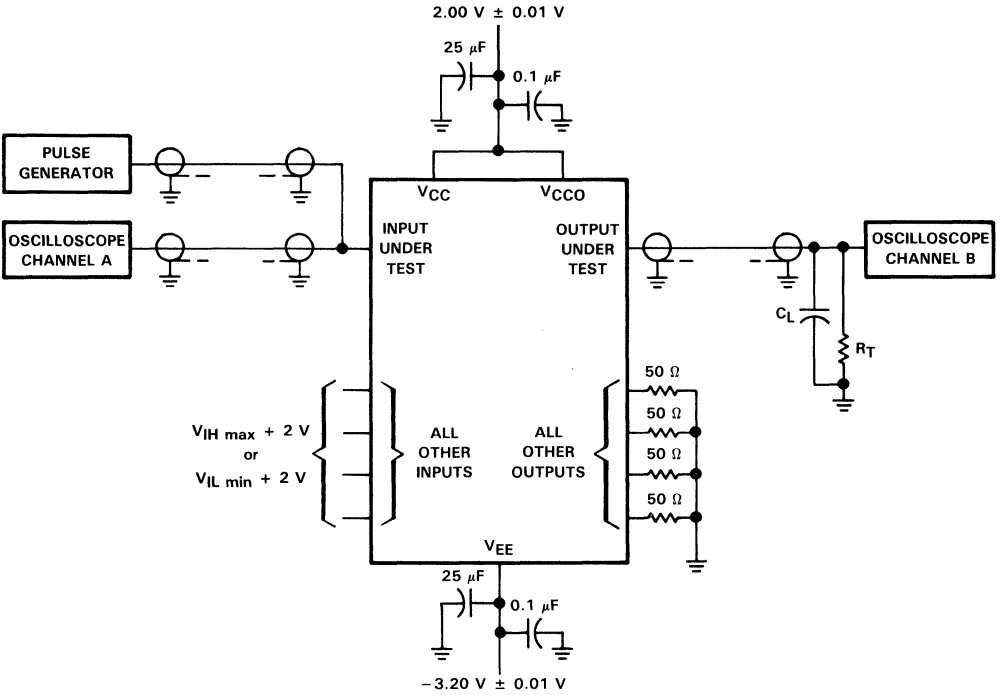
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
RISE TIME AND FALL TIME

FIGURE 1. VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The offset voltage generator has the following characteristics: Pulse amplitude = 800 mV P-P, PRR ≤ 1 MHz, t_w = 500 ns, $t_r = t_f$ = 1 ns.
B. R_T is a 50-Ω terminator internal to the oscilloscope.
C. $C_L \leq 3$ pF, includes fixture and stray capacitance.
D. Coax has 50-Ω impedance and the coax to oscilloscope channel A and to channel B must be of equal lengths.
E. All unused outputs are loaded with 50-Ω ± 1% resistors to ground.
F. All unused inputs should be connected to either high or low levels consistent with the logic function required.
G. All fixture wire lengths or unterminated stubs should not exceed 6 mm (1/4 inch).

FIGURE 2. LOAD CIRCUIT

PRODUCT PREVIEW

TEXAS INSTRUMENTS
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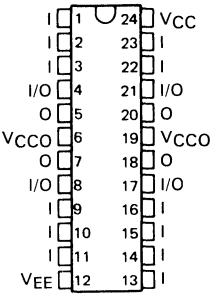
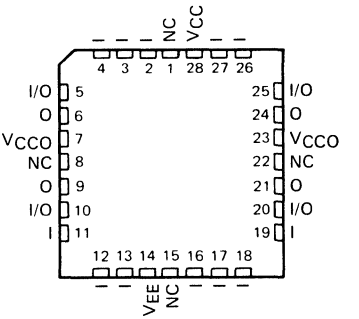
D2916, MAY 1987—REVISED SEPTEMBER 1989

- **ECL 10KH PAL**
- **High-Performance Operation**
  Propagation Delay . . . 6 ns Max
- **Replacement for Conventional ECL Logic**
- **24-Pin, 300-Mil Package**
- **Reliable Titanium-Tungsten Fuses**

TIEPAL10H16P8-6 . . . JT PACKAGE
(TOP VIEW)



TIEPAL10H16P8-6 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

This IMPACT™ ECL PAL device uses proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional ECL logic. Its easy programmability allows for quick design of "custom" functions and typically results in a more compact board. In addition, chip carriers are available for further reduction in board space.

The TIEPAL10H16P8-6 is provided with output polarity fuses. Each output remains active-high when the fuse is intact and is active-low when the fuse is blown.

The TIEPAL10H16P8-6 has 12 dedicated inputs, four standard outputs, and four I/O ports. It should be noted that with emitter-coupled outputs, a high level overrides a low level. Therefore, in order to use an I/O port as an input, the related output must be forced to a low level either through satisfying preprogrammed equations or permanently by programming.

The TIEPAL10H16P8-6 is equipped with a security fuse. Once the security fuse is blown, additional programming and verification cannot be performed. This prevents easy duplication of a design.

This device is characterized for operation from 0°C to 75°C; this temperature range is designated by a "C" suffix in the part number (TIEPAL10H16P8-6CJT).

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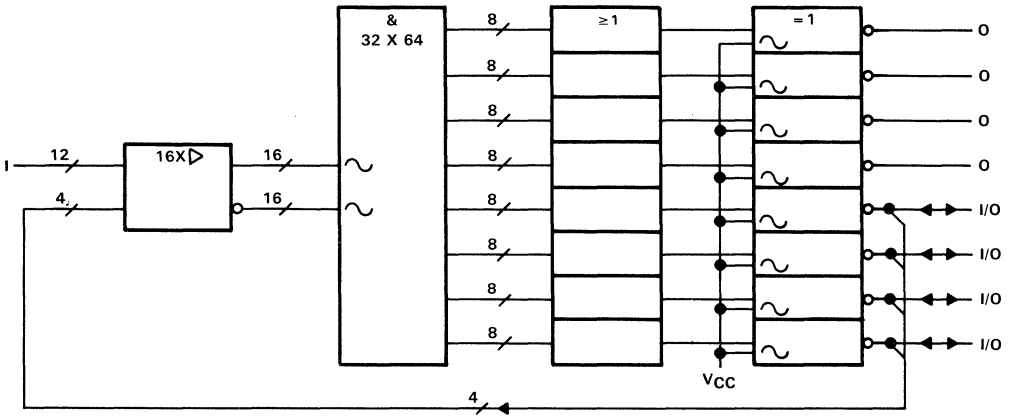
functional block diagram (positive logic)



TEXAS INSTRUMENTS
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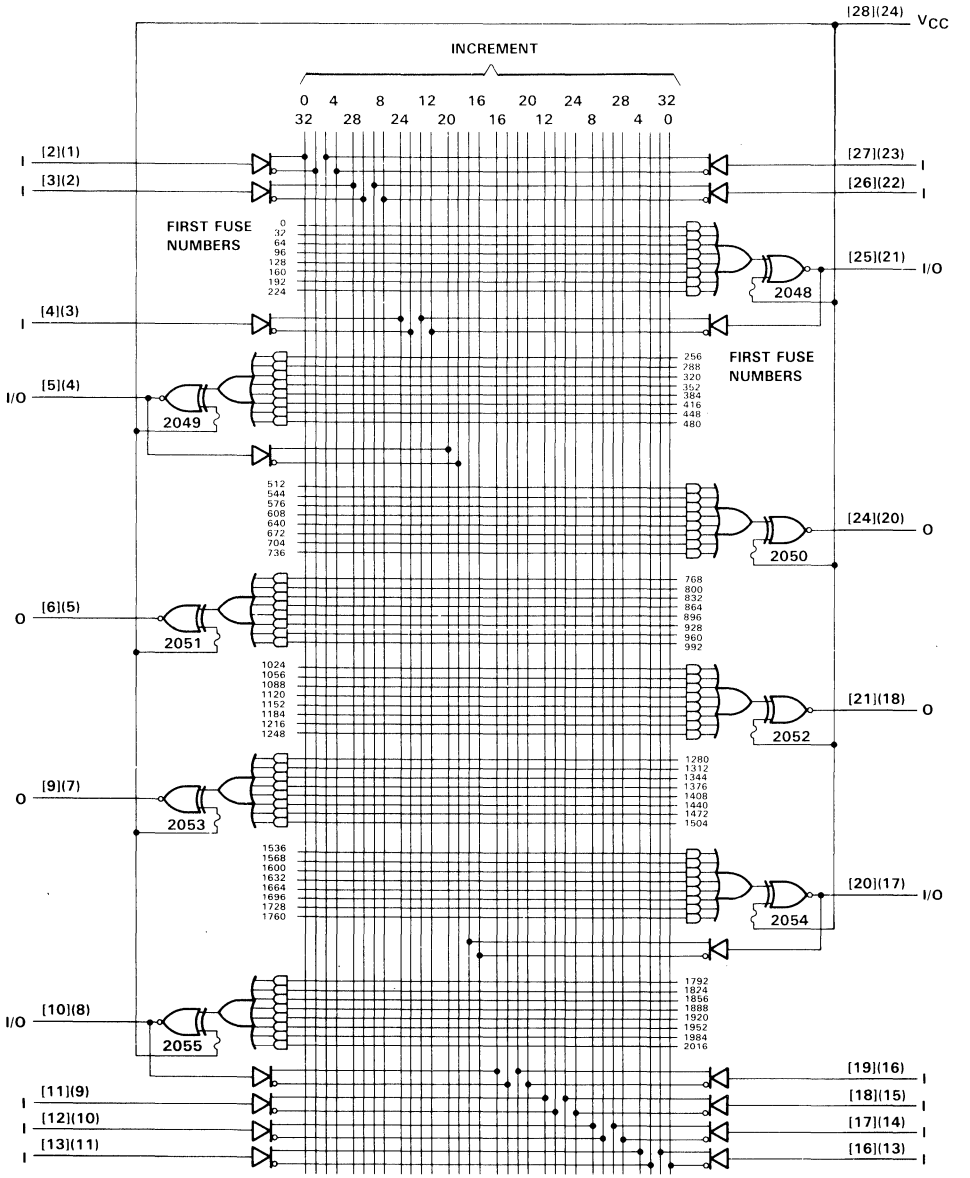
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment

NOTE: Pin numbers in [ ] are for the FK package; pin numbers in ( ) are for JT package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Supply voltage, V_{EE} (see Note 2) . . . . . 0 V to −6.5 V
Input voltage, V_I (see Notes 2 and 3) . . . . . 0 V to V_{EE}
Output current . . . . . −50 mA
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. These ratings apply except for programming pins during a programming cycle.
2. All voltage values are with respect to V_{CC} and V_{CCO}, i.e., these pins are all assumed to be at 0 volts.
3. V_I should never be more negative than V_{EE}.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{EE}	Supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	High-level input voltage	T_A = 0°C	−1.170		−0.840	V
		T_A = 25°C	−1.130		−0.810	
		T_A = 75°C	−1.070		−0.735	
V_{IL}	Low-level input voltage	T_A = 0°C	−1.950		−1.480	V
		T_A = 25°C	−1.950		−1.480	
		T_A = 75°C	−1.950		−1.450	
T_A	Operating free-air temperature		0		75	°C

NOTE 4: The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.

electrical characteristics over recommended supply voltage range at specified free-air temperature, V_{CC} = V_{CCO} = 0 (see Notes 4 and 5)

PARAMETER	TEST CONDITIONS	T_A	MIN	MAX	UNIT
V_{OH}	V_I = V_{IH}min or V_{IL}max	0°C	−1.020	−0.840	V
		25°C	−0.980	−0.810	
		75°C	−0.920	−0.735	
V_{OL}	V_I = V_{IH}min or V_{IL}max	0°C	−1.950	−1.630	V
		25°C	−1.950	−1.630	
		75°C	−1.950	−1.600	
I_{IH}	V_I = V_{IH}max	0°C		220	μA
		25°C		220	
		75°C		220	
I_{IL}	V_I = V_{IL}min	0°C	0.5		μA
		25°C	0.5		
		75°C	0.3		
I_{EE}	All inputs open	0°C to 75°C		−240	mA

NOTES: 4. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.
5. Each 10KH PAL® has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	I, I/O, or feedback	Q	See Figures 1 and 2	2	4	6	ns
t_r				0.7	1	2.2	ns
t_f				0.7	1	2.2	ns

NOTES: 4. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.

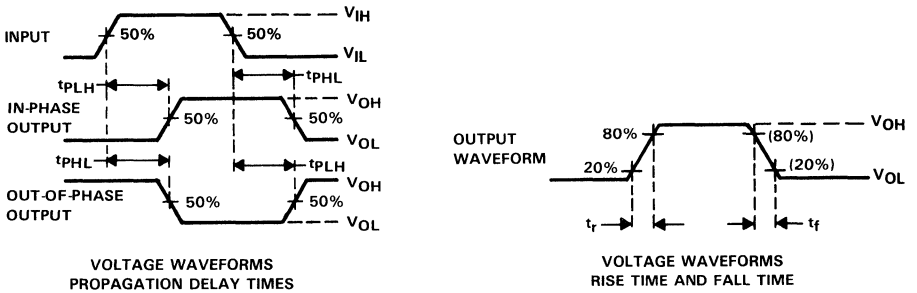
5. Each 10KH PAL® has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

PROGRAMMING INFORMATION

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 995-5666.

PARAMETER MEASUREMENT INFORMATION

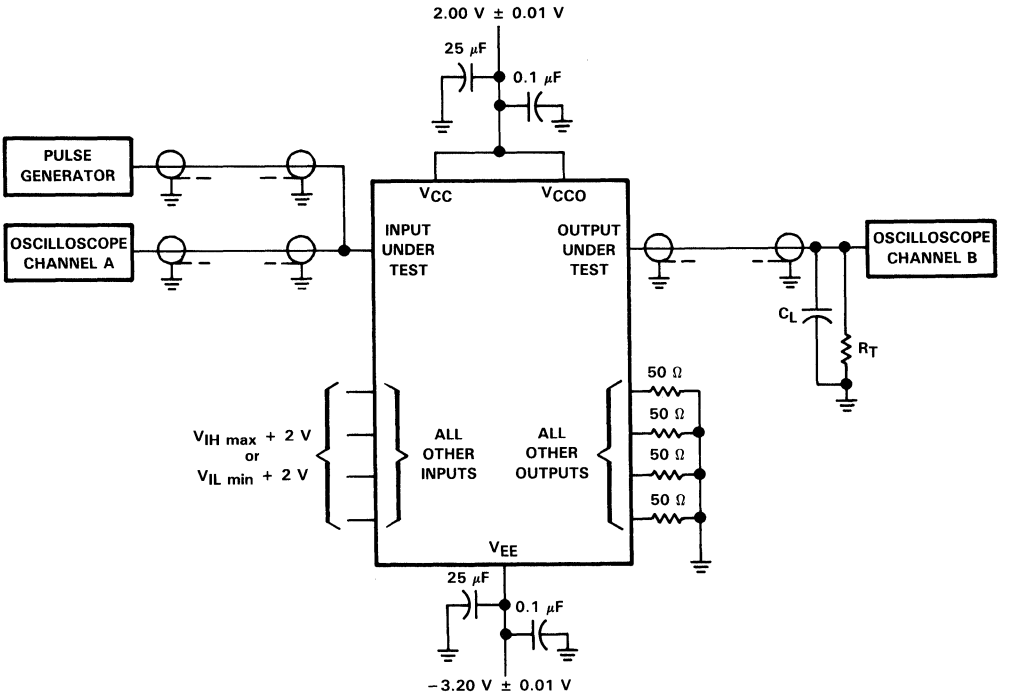


VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS RISE TIME AND FALL TIME

FIGURE 1. VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The offset voltage generator has the following characteristics: Pulse amplitude = 800 mV P-P, PRR ≤ 1 MHz, t_w = 500 ns, t_r = t_f = 1 ns.
B. R_T is a 50-Ω terminator internal to the oscilloscope.
C. C_L ≤ 3 pF, includes fixture and stray capacitance.
D. Coax has 50-Ω impedance and the coax to oscilloscope channel A and to channel B must be of equal lengths.
E. All unused outputs are loaded with 50-Ω ±1% resistors to ground.
F. All unused inputs should be connected to either high or low levels consistent with the logic function required.
G. All fixture wire lengths or unterminated stubs should not exceed 6 mm (1/4 inch).

FIGURE 2. LOAD CIRCUIT

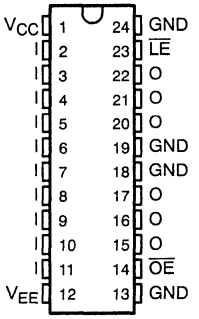
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TIEPAL10H16TE6C
TTL-TO-ECL *IMPACT-X™ PAL®* TRANSLATOR CIRCUIT

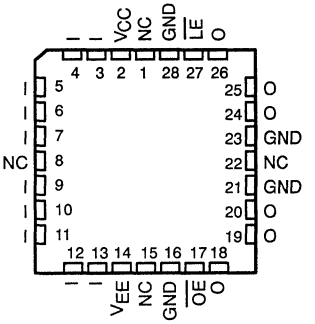
D3351, OCTOBER 1989

- **ECL 10H Programmable Logic with TTL-to-ECL Translation**
- **ECL Control Inputs**
- **3-State ECL Outputs**
- **IMPACT-X™ Process with Reliable Titanium-Tungsten Fuses**
- **Package Options Include Both 300-mil Ceramic DIP and Plastic Chip Carrier**

JT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TIEPAL10H16TE6C combines the IMPACT-X™ (Advanced Implanted, Advanced Composed Technology) process with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional ECL 10H logic. Easy programmability allows for quick design of custom functions with increased logic density.

The TIEPAL10H16TE6C accepts TTL input levels and provides ECL output levels, making it ideal for interfacing TTL with ECL circuits. It has latched outputs, which are controlled from an ECL Latch Enable input, $\overline{LE}$. The outputs are enabled from a single ECL input, $\overline{OE}$.

The TIEPAL10H16TE6C is provided with an output polarity fuse that, if blown, allows an output to assume a logic high when the implemented equation is satisfied. However, when the output polarity fuse is intact and the implemented equation is satisfied, the output will assume a logic low.

The TIEPAL10H16TE6C is equipped with a security fuse that, when blown, prevents additional programming and design verification. This safeguards against easy duplication of a design.

The four GND pins must all be tied externally to an adequate ground plane for proper operation of this device.

The TIEPAL10H16TE6C is characterized for operation from 0°C to 75°C.

PRODUCT PREVIEW

IMPACT-X is a trademark of Texas Instruments Incorporated
PAL is a registered trademark of Monolithic Memories Inc.

PRODUCT PREVIEW *documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.*

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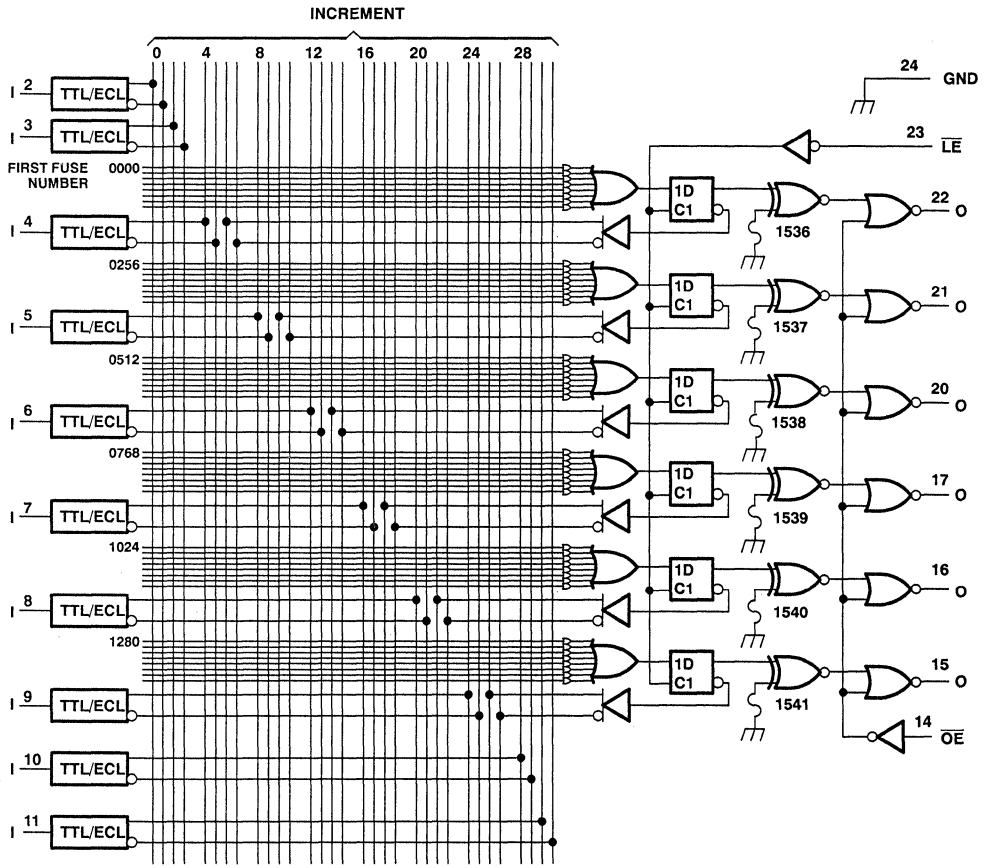
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for the JT package.
An exclusive-NOR input grounded through an intact polarity fuse is at an ECL high logic level.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FUNCTION TABLE

INPUTS			OUTPUTS		
$\overline{OE}$	$\overline{LE}$	ARRAY DATA	O†	$\overline{O}$‡	FEEDBACK
L	L	H	H	L	H
L	L	L	L	H	L
L	H	X	O_0	$\overline{O}_0$	O_0
H	H	X	L	L	O_0
H	L	H	L	L	H
H	L	L	L	L	L

X = Don't care
† = Polarity fuse blown
‡ = Polarity fuse intact

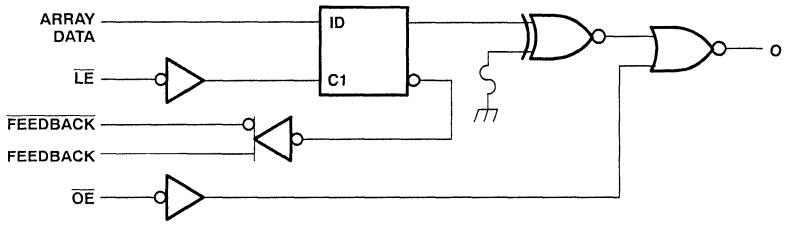


FIGURE 1. SIMPLIFIED LOGIC DIAGRAM (EACH OUTPUT)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

ECL supply voltage range, V_{EE} (see Note 2) ..... −7 V to 0.5 V
TTL supply voltage range, V_{CC} ..... −0.5 V to 7 V
ECL input voltage range ..... V_{EE} to 0.5 V
TTL input voltage ..... 5.5 V
Operating free-air temperature range, T_A ..... 0°C to 75°C
Storage temperature range ..... −65°C to 150°C

NOTES: 1. These ratings apply except for programming pins during a programming cycle.
2. All voltage values are with respect to the GND pins connected together.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
TTL supply voltage, V_{CC}		4.75	5	5.25	V
ECL supply voltage, V_{EE}		−4.95	−5.2	−5.46	V
TTL high-level input voltage, V_{IH}		2		5.5	V
ECL high-level input voltage, V_{IH} ($\overline{LE}$ and $\overline{OE}$ inputs)	T_A = 0°C	−1.17		−0.84	V
	T_A = 25°C	−1.13		−0.81	
	T_A = 75°C	−1.07		−0.735	
TTL low-level input voltage, V_{IL}				0.8	V
ECL low-level input voltage, V_{IL} ($\overline{LE}$ and $\overline{OE}$ inputs)	T_A = 0°C	−1.95		−1.48	V
	T_A = 25°C	−1.95		−1.48	
	T_A = 75°C	−1.95		−1.45	
Pulse duration, $\overline{LE}$ high, t_w		3			ns
Setup time, data before $\overline{LE}\uparrow$, t_{su}		4			ns
Hold time, data after $\overline{LE}\uparrow$, t_h		0			ns
Operating free-air temperature, T_A		0		75	°C

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	V_I = −18 mA			−1.5	V
V_{OH}		V_{EE} = −5.46 V,	V_I = V_{IL}max or V_{IH}min	T_A = 0°C	−1.02	−0.84	V
				T_A = 25°C	−0.98	−0.81	
				T_A = 75°C	−0.92	−0.735	
V_{OL}		V_{EE} = −5.46 V,	V_I = V_{IL}max or V_{IH}min	T_A = 0°C	−1.95	−1.63	V
				T_A = 25°C	−1.95	−1.63	
				T_A = 75°C	−1.95	−1.6	
I_{IH}†	I	V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
	$\overline{LE}$, $\overline{OE}$	V_{EE} = −5.46 V,	V_I = V_{IH}max			220	
I_{IL}†	I	V_{CC} = 5.25 V,	V_I = 0.4 V			−200	µA
	$\overline{LE}$, $\overline{OE}$	V_{EE} = −4.94 V,	V_I = V_{IL}min		0.5		
I_{CC} + I_{EE}‡		V_{CC} = 5.25 V	V_{EE} = −5.46 V			−220	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	$\overline{LE}\downarrow$	O	See Figures 2 and 3		5		ns
t_{pd}	I or Feedback	O			6		ns
t_{en}	$\overline{OE}$	O			4		ns
t_{dis}	$\overline{OE}$	O			5		ns

† For ECL inputs, measure one input at a time with the other inputs open.

‡ All inputs and outputs are open.

NOTES: 3. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.

4. Each device has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-Ω resistor to −2 V.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

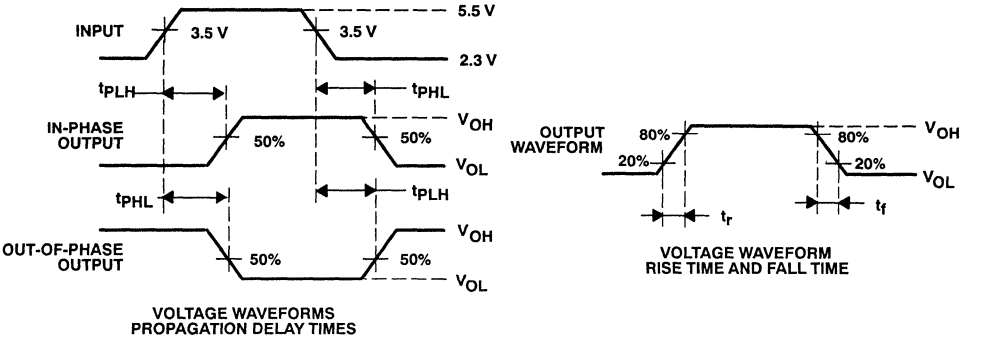
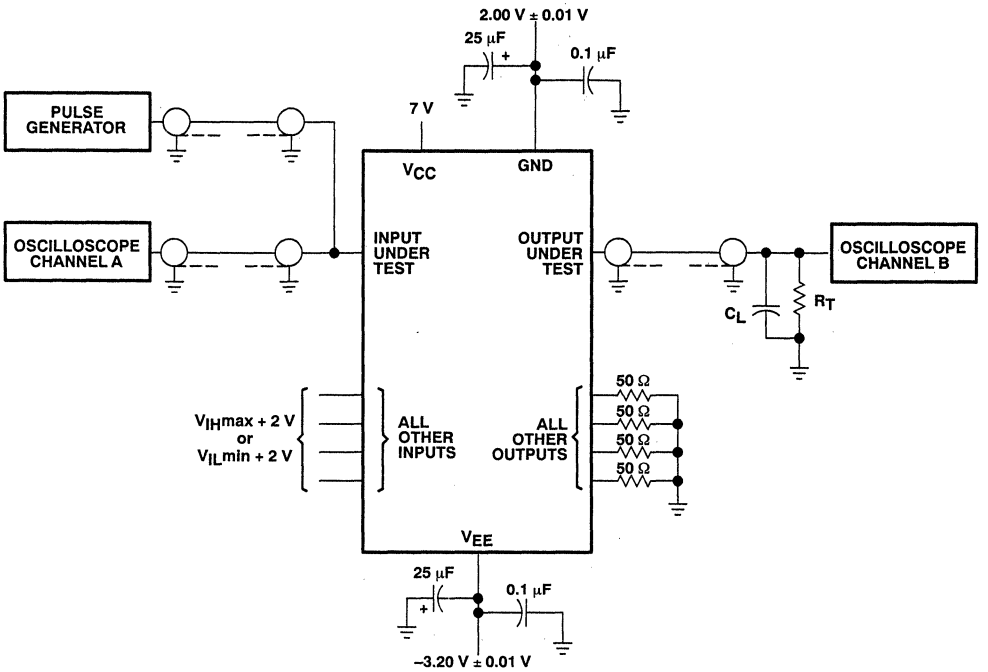


FIGURE 2. VOLTAGE WAVEFORMS

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The offset voltage generator has the following characteristics: Pulse amplitude = 800 mV P-P, PRR ≤ 1 MHz, t_w = 500 ns, $t_r = t_f$ = 1 ns.
B. R_T is a 50-Ω terminator internal to the oscilloscope.
C. C_L ≤ 3 pF, includes fixture and stray capacitance.
D. The coaxial cables have 50-Ω impedance and the cable lengths to oscilloscope channel A and to channel B must be equal.
E. All unused outputs are loaded with 50-Ω ± 1% resistors to ground.
F. All unused inputs should be connected to either high or low levels consistent with the logic function required.
G. All fixture wire lengths or unterminated stubs should not exceed 6 mm (1/4 inch).

FIGURE 3. TEST CIRCUIT

PRODUCT PREVIEW

TEXAS INSTRUMENTS
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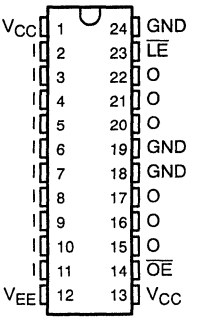
TIEPAL10016ET6C
ECL-TO-TTL *IMPACT-X™ PAL®* TRANSLATOR CIRCUIT

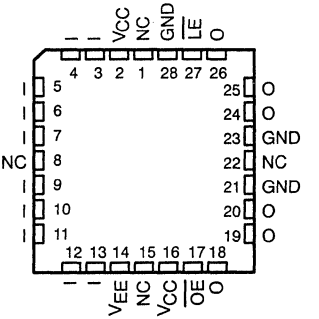
D3352, OCTOBER 1989

- **ECL 100K Programmable Logic with ECL-to-TTL Translation**
- **ECL Control Inputs**
- **3-State TTL Outputs**
- **IMPACT-X™ Process with Reliable Titanium-Tungsten Fuses**
- **Package Options Include Both 300-mil Ceramic DIP and Plastic Chip Carrier**

JT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TIEPAL10016ET6C combines the IMPACT-X™ (Advanced Implanted, Advanced Composed Technology) process with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional ECL 100K logic. Easy programmability allows for quick design of custom functions with increased logic density.

The TIEPAL10016ET6C accepts ECL input levels and provides TTL output levels, making it ideal for interfacing ECL with TTL circuits. It has latched outputs, which are controlled by an ECL Latch Enable input, $\overline{LE}$. The 3-state outputs are enabled input from a single ECL input, $\overline{OE}$. The TTL outputs are designed for 24-mA low-level output current.

The TIEPAL10016ET6C is provided with an output polarity fuse that, if blown, allows an output to assume a logic high when the implemented equation is satisfied. However, when the output polarity fuse is intact and the implementation equation is satisfied, the output will assume a logic low.

The TIEPAL10016ET6C is equipped with a security fuse that, when blown, prevents additional programming and design verification. This safeguards against easy duplication of a design.

The three GND pins must all be tied externally to an adequate ground plane for proper operation of this device.

The TIEPAL10016ET6C is characterized for operation from 0°C to 85°C.

PRODUCT PREVIEW

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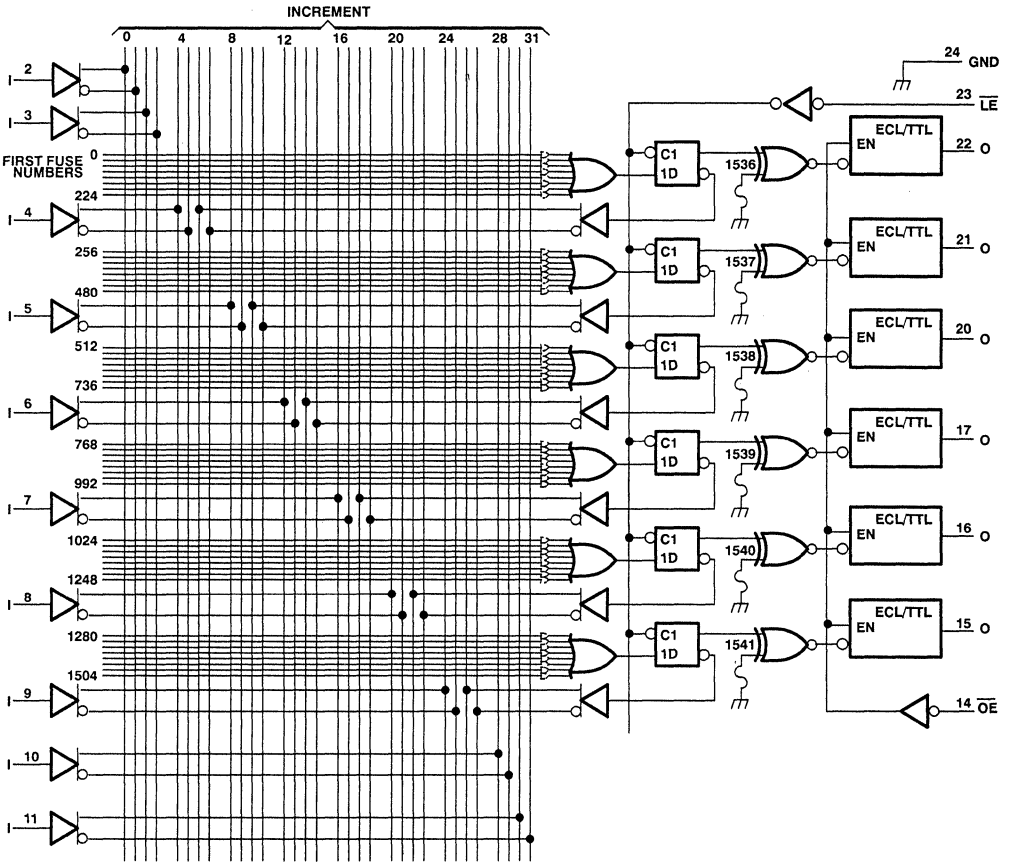
PRODUCT PREVIEW

logic diagram



Fuse Number = First Fuse Number + Increment
An exclusive-NOR input grounded through an intact polarity fuse is at an ECL logic-high level.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FUNCTION TABLE

INPUTS			OUTPUTS		
$\overline{OE}$	$\overline{LE}$	DATA IN	O†	O‡	FEEDBACK
L	L	H	H	L	H
L	L	L	L	H	L
L	H	X	O_0	$\overline{O}_0$	O_0
H	H	X	Z	Z	O_0
H	L	H	Z	Z	H
H	L	L	Z	Z	L

X = Don't care
† = Polarity fuse blown
‡ = Polarity fuse intact

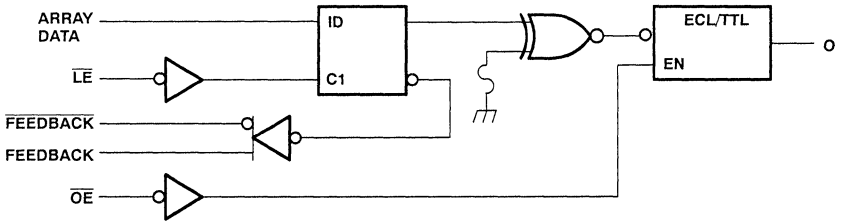


FIGURE 1. SIMPLIFIED LOGIC DIAGRAM (EACH OUTPUT)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

ECL supply voltage, V_{EE} ..... −7 V to 0.5 V
TTL supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage range ..... V_{EE} to 0.5 V
Operating free-air temperature range ..... 0°C to 85°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
TTL supply voltage, V_{CC}		4.5	5	5.5	V
ECL supply voltage, V_{EE}		−4.2	−4.5	−4.8	V
High-level input voltage, V_{IH}	V_{EE} = −4.2 V	−1.15		−0.88	V
	V_{EE} = −4.5 V	−1.165		−0.88	
	V_{EE} = −4.8 V	−1.165		−0.88	
Low-level input voltage, V_{IL}	V_{EE} = −4.2 V	−1.81		−1.475	V
	V_{EE} = −4.5 V	−1.81		−1.475	
	V_{EE} = −4.8 V	−1.81		−1.49	
High-level output current, I_{OH}				−3.2	mA
Low-level output current, I_{OL}				24	mA
Pulse duration, $\overline{LE}$ high, t_w		3			ns
Setup time, data before $\overline{LE}\uparrow$, t_{su}		4			ns
Hold time, data after $\overline{LE}\uparrow$, t_h		0			ns
Operating free-air temperature, T_A		0		85	°C

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			V_{EE}	MIN	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	$V_I = V_{IH}$min or V_{IL}max	I_{OH} = −2 mA	−4.2 V to −4.8 V	2.4		V
V_{OL}	V_{CC} = 4.5 V,	$V_I = V_{IH}$min or V_{IL}max	I_{OL} = 24 mA	−4.2 V to −4.8 V		0.5	V
I_{IH}†	$V_I = V_{IH}$max			−4.8 V		220	µA
I_{IL}†	$V_I = V_{IL}$min			−4.2 V	0.5		µA
I_{OZH}	V_{CC} = 5.5 V,	V_I = 2.7 V		−4.2 V to −4.8 V		20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−4.2 V to −4.8 V		−20	µA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0		−4.2 V to −4.8 V	−40	−100	mA
$I_{CC} + I_{EE}$	V_{CC} = 5.5 V,	Pins 1 and 13 are tied together		−4.8 V		−240	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	$\overline{LE}\downarrow$	O	R1 = 200 Ω, R2 = 200 Ω, See Figure 1		5		ns
t_{pd}	I or Feedback	O			6		ns
t_{en}	$\overline{OE}$	O			4		ns
t_{dis}	$\overline{OE}$	O			5		ns

† Measure one input at a time. Ensure that all other inputs are open.

‡ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 2. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.

3. Each device has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained.

TEXAS INSTRUMENTS
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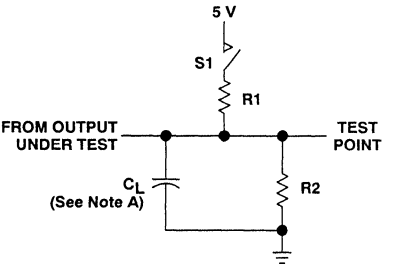
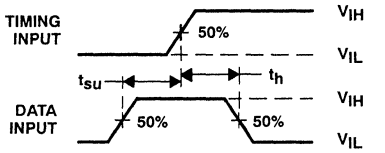
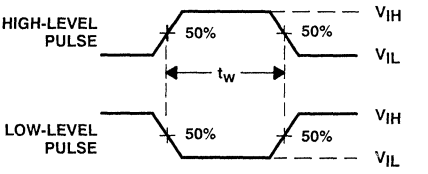
PARAMETER MEASUREMENT INFORMATION



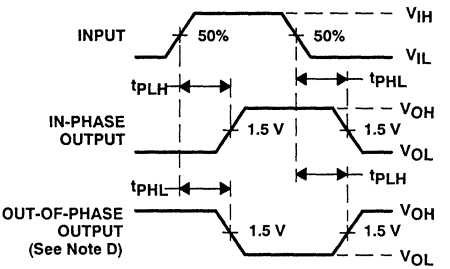
LOAD CIRCUIT FOR 3-STATE OUTPUTS



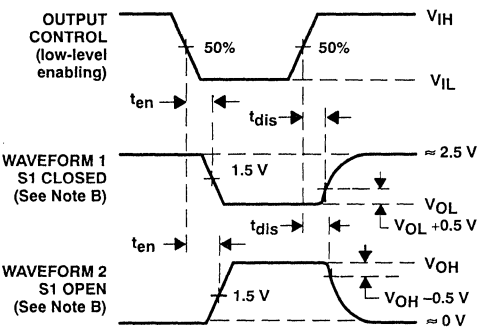
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 0.7$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

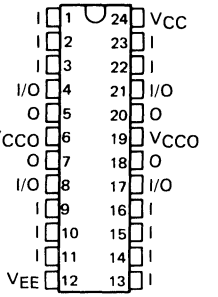
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PRODUCT PREVIEW

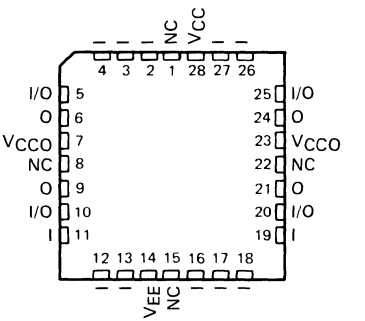
D3083, DECEMBER 1987—REVISED SEPTEMBER 1989

- **ECL 100K PAL**
- **High-Performance Operation**
  Propagation Delay . . . 3 ns Max
- **I_{EE} . . . −220 mA Max**
- **Replacement for 100K ECL Logic**
- **24-Pin, 300-Mil Package**
- **Reliable Titanium-Tungsten Fuses**

JT PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

This ECL PAL device combines the ExCL™ (Double Polysilicon Self-Aligned) process with the proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional ECL logic. Its easy programmability allows for quick design of "custom" functions with increased logic density. In addition, chip carriers are available for further reduction in board space.

The TIEPAL10016P8-3 is provided with output polarity fuses. Each output remains active-high when the fuse is intact and is active-low when the fuse is blown.

The TIEPAL10016P8-3 has 12 dedicated inputs, four standard outputs, and four I/O ports. It should be noted that with emitter-coupled outputs, a high level overrides a low level. Therefore, in order to use an I/O port as an input, the related output must be forced to a low level either through satisfying preprogrammed equations or permanently by programming.

The TIEPAL10016P8-3 is equipped with a security fuse. Once the security fuse is blown, additional programming and verification cannot be performed. This prevents easy duplication of a design.

This device is characterized for operation from 0°C to 85°C; this temperature range is designated by a "C" suffix in the part number (TIEPAL10016P8-3CJT).

PRODUCT PREVIEW

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PAL is a registered trademark of Monolithic Memories Inc.

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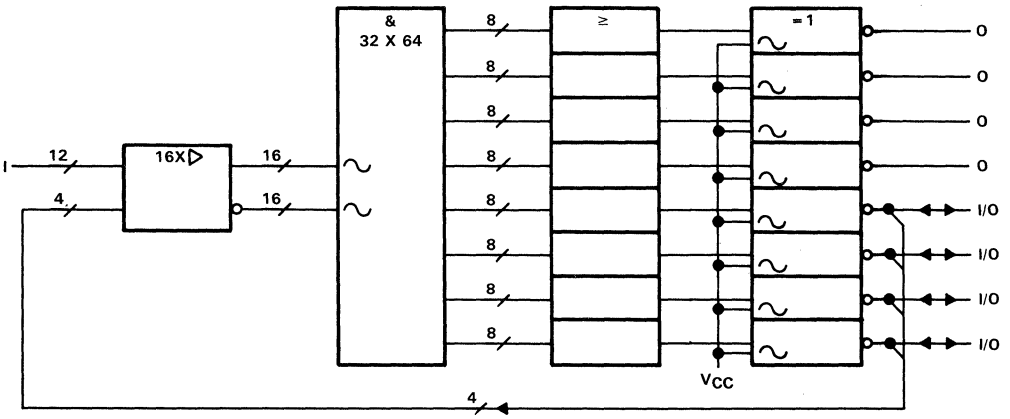
functional block diagram (positive logic)



PRODUCT PREVIEW

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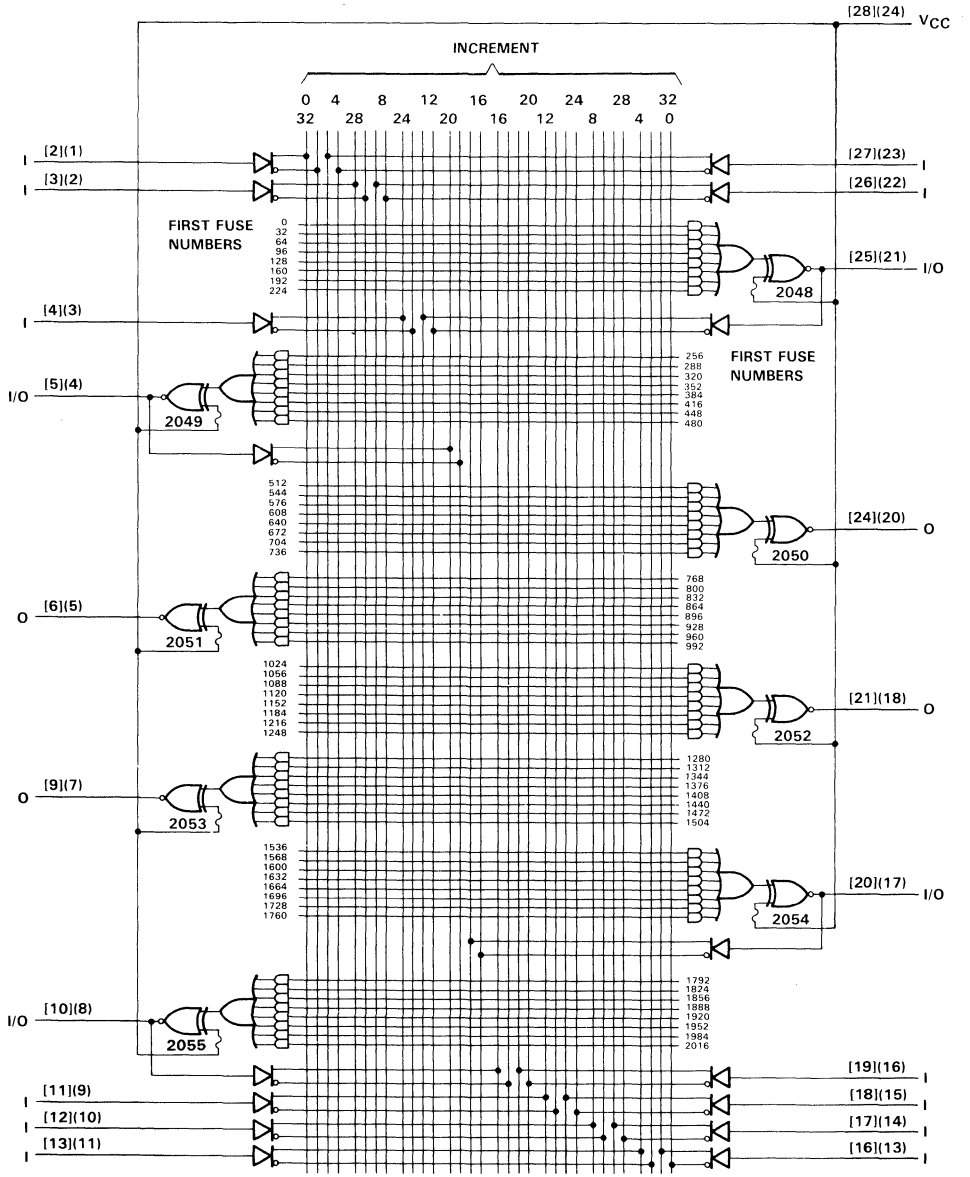
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
NOTE: Pin numbers in [ ] are for the FK package; pin numbers in ( ) are for JT package.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Supply voltage, V_{EE} (see Note 2) . . . . . 0 V to −6.5 V
Input voltage, V_I (see Note 3) . . . . . 0 V to V_{EE}
Output current . . . . . −50 mA
Operating free-air temperature range . . . . . 0°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. These ratings apply except for programming pins during a programming cycle.
2. All voltage values are with respect to V_{CC} and V_{CCO}, i.e., these pins are all assumed to be at 0 volts.
3. V_I should never be more negative than V_{EE}.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{EE}	Supply voltage		−4.2	−4.5	−4.8	V
V_{IH}	High-level input voltage	V_{EE} = −4.2 V	−1.15		−0.88	V
		V_{EE} = −4.5 V	−1.165		−0.88	
		V_{EE} = −4.8 V	−1.165		−0.88	
V_{IL}	Low-level input voltage	V_{EE} = −4.2 V	−1.81		−1.475	V
		V_{EE} = −4.5 V	−1.81		−1.475	
		V_{EE} = −4.8 V	−1.81		−1.49	
T_A	Operating free-air temperature		0		85	°C

electrical characteristics over recommended supply voltage range, T_A = 0°C to 85°C (unless otherwise noted) (see Notes 4 and 5)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	V_I = V_{IH}min or V_{IL}max	V_{EE} = −4.2 V	−1.03		−0.87	V
		V_{EE} = −4.5 V	−1.035	−0.955	−0.88	
		V_{EE} = −4.8 V	−1.045		−0.88	
V_{OL}	V_I = V_{IH}min or V_{IL}max	V_{EE} = −4.2 V	−1.81		−1.595	V
		V_{EE} = −4.5 V	−1.81	−1.700	−1.61	
		V_{EE} = −4.8 V	−1.81		−1.61	
I_{IH}	V_I = V_{IH}max				220	μA
I_{IL}	V_I = V_{IL}min		0.5			μA
I_{EE}	All inputs open				−220	mA

†Typical values are at V_{CC} = 4.5 V, T_A = 25°C.

NOTES: 4. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.
5. Each 100KH PAL has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	I, I/O, or feedback	O, I/O	See Figures 1 and 2	1	3	ns
t_r				0.7	1.5	ns
t_f				0.7	1.5	ns

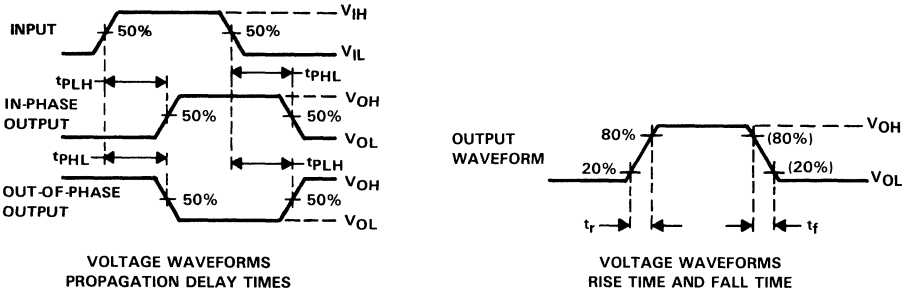
NOTE 5: Each 100KH PAL has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

PROGRAMMING INFORMATION

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

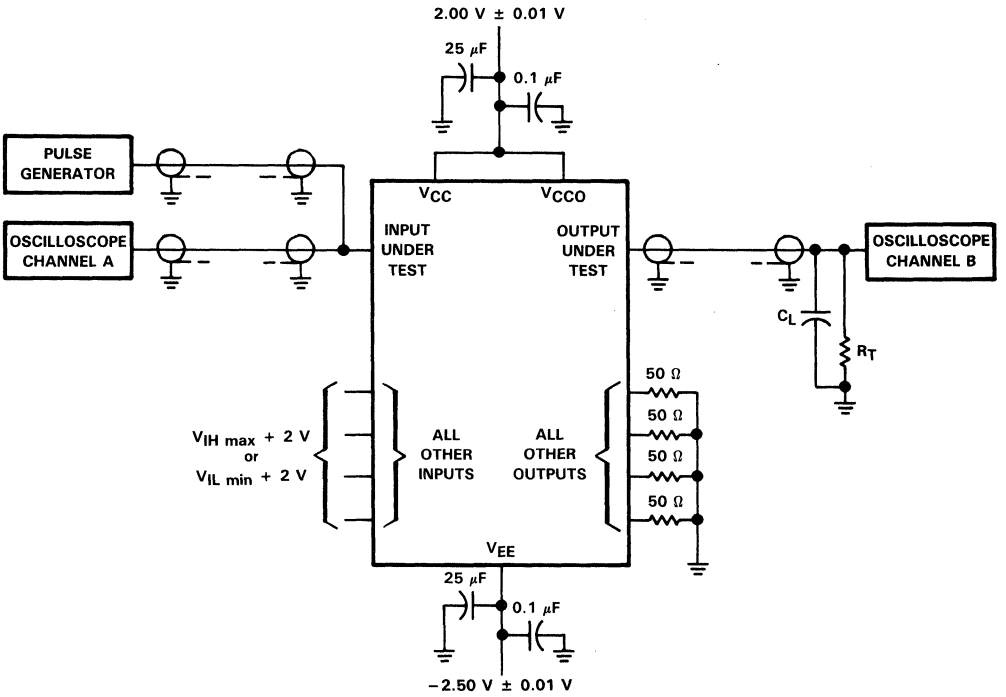


VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS RISE TIME AND FALL TIME

FIGURE 1. VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The offset voltage generator has the following characteristics: Pulse amplitude = 800 mV P-P, PRR ≤ 1 MHz, t_w = 500 ns, $t_r = t_f$ = 1 ns.
B. R_T is a 50-Ω terminator internal to the oscilloscope.
C. C_L ≤ 3 pF, includes fixture and stray capacitance.
D. Coax has 50-Ω impedance and the coax to oscilloscope channel A and to channel B must be of equal lengths.
E. All unused outputs are loaded with 50-Ω ± 1% resistors to ground.
F. All unused inputs should be connected to either high or low levels consistent with the logic function required.
G. All fixture wire lengths or unterminated stubs should not exceed 6 mm (1/4 inch).

FIGURE 2. LOAD CIRCUIT

PRODUCT PREVIEW

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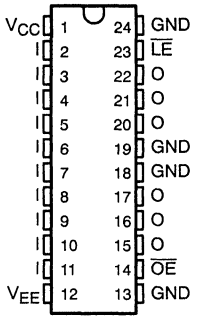
TIEPAL10016TE6C
TTL-TO-ECL *IMPACT-X™ PAL®* TRANSLATOR CIRCUIT

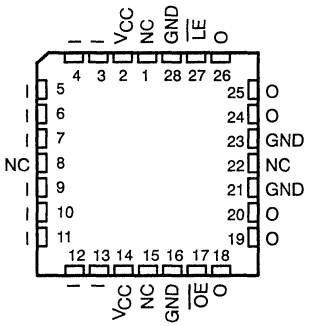
D3362, OCTOBER 1989

- **ECL Programmable Logic with TTL-to-ECL Translation**
- **ECL Control Inputs**
- **3-State ECL Outputs**
- **Impact-X™ Process with Reliable Titanium-Tungsten Fuses**
- **Package Options Include Both 300-mil Ceramic DIP and Plastic Chip Carrier**

JT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TIEPAL10016TE6C combines the IMPACT-X™ (Advanced Implanted, Advanced Composed Technology) process with proven titanium-tungsten fuses to provide reliable high-performance substitutes for conventional ECL 100K logic. Easy programmability allows for quick design of custom functions with increased logic density.

The TIEPAL10016TE6C accepts TTL input levels and provides ECL output levels, making it ideal for interfacing TTL with ECL circuits. It has latched outputs, which are controlled from an ECL Latch Enable input, $\overline{LE}$. The outputs are enabled from a single ECL input, $\overline{OE}$.

The TIEPAL10016TE6C is provided with an output polarity fuse that, if blown, will allow an output to assume a logic high when the implemented equation is satisfied. However, when the output polarity fuse is intact and the implemented equation is satisfied, the output will assume a logic low.

The TIEPAL10016TE6C is equipped with a security fuse that, when blown, prevents additional programming and design verification. This safeguards against easy duplication of a design.

The four GND pins must all be tied externally to an adequate ground plane for proper operation of this device.

The TIEPAL10016TE6C is characterized for operation from 0°C to 85°C.

PRODUCT PREVIEW

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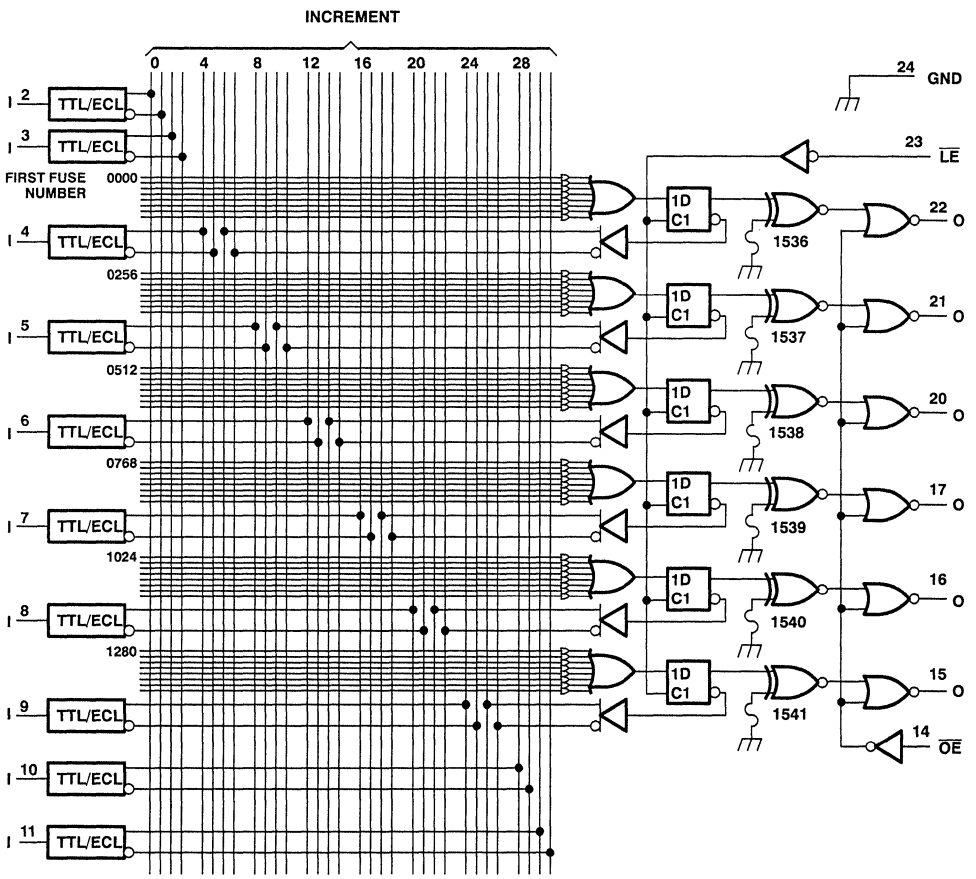
logic diagram



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for the JT package.
An exclusive-NOR input grounded through an intact polarity fuse is at an ECL high logic level.

PRODUCT PREVIEW

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FUNCTION TABLE

INPUTS			OUTPUTS		
$\overline{OE}$	$\overline{LE}$	ARRAY DATA	O†	$\overline{O}$‡	FEEDBACK
L	L	H	H	L	H
L	L	L	L	H	L
L	H	X	Q_0	$\overline{Q}_0$	Q_0
H	H	X	L	L	Q_0
H	L	H	L	L	H
H	L	L	L	L	L

X = Don't care
† = Polarity fuse blown
‡ = Polarity fuse intact

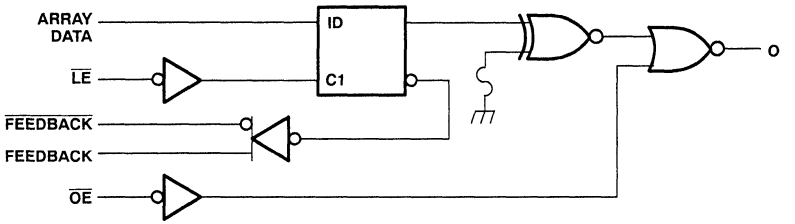

FIGURE 1. SIMPLIFIED LOGIC DIAGRAM (EACH OUTPUT)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

ECL supply voltage range, V_{EE} (see Note 2) ..... −8 V to 0.5 V
TTL supply voltage range, V_{CC} ..... −0.5 V to 7 V
ECL input voltage range ..... V_{EE} to 0.5 V
TTL input voltage ..... 5.5 V
Operating free-air temperature range, T_A ..... 0°C to 85°C
Storage temperature range ..... −65°C to 150°C

NOTES: 1. These ratings apply except for programming pins during a programming cycle.
2. All voltage values are with respect to the GND pins connected together.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
TTL supply voltage, V_{CC}		4.75	5	5.25	V
ECL supply voltage, V_{EE}		−4.2	−4.5	−4.8	V
TTL high-level input voltage, V_{IH}		2		5.5	V
ECL high-level input voltage, V_{IH} ($\overline{LE}$ and $\overline{OE}$ inputs)	V_{EE} = −4.2 V	−1.15		−0.88	V
	V_{EE} = −4.5 V	−1.165		−0.88	
	V_{EE} = −4.8 V	−1.165		−0.88	
TTL low-level input voltage, V_{IL}				0.8	V
ECL low-level input voltage, V_{IL} ($\overline{LE}$ and $\overline{OE}$ inputs)	V_{EE} = −4.2 V	−1.81		−1.475	V
	V_{EE} = −4.5 V	−1.81		−1.475	
	V_{EE} = −4.8 V	−1.81		−1.49	
Pulse duration, $\overline{LE}$ high, t_w		3			ns
Setup time, data before $\overline{LE}\uparrow$, t_{su}		4			ns
Hold time, data after $\overline{LE}\uparrow$, t_h		0			ns
Operating free-air temperature, T_A		0		85	°C

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	V_I = −18 mA			−1.5	V
V_{OH}		$V_I = V_{IL}$max or V_{IH}min		V_{EE} = −4.2 V	−1.03	−0.87	V
				V_{EE} = −4.5 V	−1.035	−0.88	
				V_{EE} = −4.8 V	−1.045	−0.88	
V_{OL}		$V_I = V_{IL}$max or V_{IH}min		V_{EE} = −4.2 V	−1.81	−1.595	V
				V_{EE} = −4.5 V	−1.81	−1.61	
				V_{EE} = −4.8 V	−1.81	−1.61	
I_{IH}†	I	V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
	$\overline{LE}$, $\overline{OE}$	$V_I = V_{IH}$max		V_{EE} = −4.2 V to −4.8 V		220	
I_{IL}†	I	V_{CC} = 5.25 V,	V_I = 0.4 V			−200	µA
	$\overline{LE}$, $\overline{OE}$	$V_I = V_{IL}$min		V_{EE} = −4.2 V to −4.8 V	0.5		
$I_{CC} + I_{EE}$‡		V_{CC} = 5.25 V		V_{EE} = −4.2 V to −4.8 V		−220	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	$\overline{LE}\downarrow$	O	See Figures 2 and 3		5		ns
t_{pd}	I or Feedback	O			6		ns
t_{en}	$\overline{OE}$	O			4		ns
t_{dis}	$\overline{OE}$	O			5		ns

† For ECL inputs, measure one input at a time with the other inputs open.

‡ All inputs and outputs are open.

NOTES: 3. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.

4. Each device has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-Ω resistor to −2 V.

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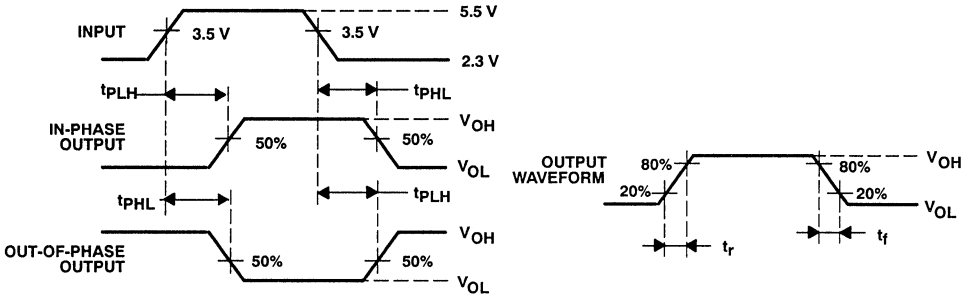
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

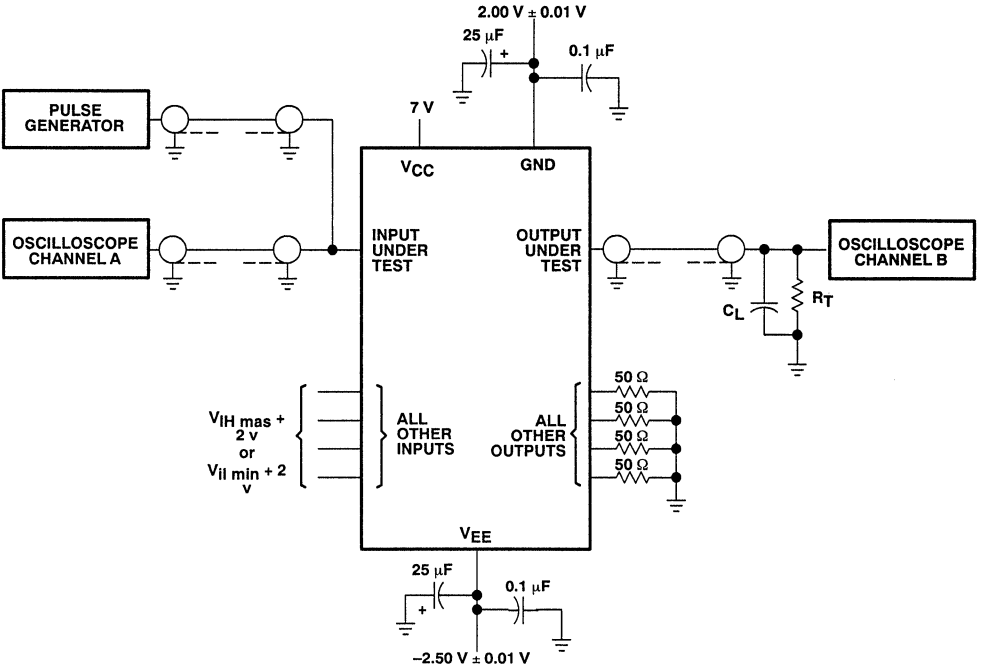
VOLTAGE WAVEFORM
RISE TIME AND FALL TIME

FIGURE 2. VOLTAGE WAVEFORMS

PRODUCT PREVIEW

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The offset voltage generator has the following characteristics: Pulse amplitude = 800 mV P-P, PRR ≤ 1 MHz, t_W = 500 ns, $t_r = t_f$ = 1 ns.
B. R_T is a 50-Ω terminator internal to the oscilloscope.
C. C_L ≤ 3 pF, includes fixture and stray capacitance.
D. Coax has 50-Ω impedance and the coax to oscilloscope channel A and to channel B must be of equal lengths.
E. All unused outputs are loaded with 50-Ω ± 1% resistors to ground.
F. All unused inputs should be connected to either high or low levels consistent with the logic function required.
G. All fixture wire lengths or unterminated stubs should not exceed 6 mm (1/4 inch).

FIGURE 3. TEST CIRCUIT

D2708, JUNE 1984—REVISED AUGUST 1989

- **Input-to-Output Propagation Delay . . . 10 ns Typical**
- **24-Pin, 300-mil Slim Line Packages**
- **Power Dissipation . . . 650 mW Typical**
- **Programmable Output Polarity**

description

The'FPLA839 (3-state outputs) and the 'FPLA840 (open-collector outputs) are TTL field-programmable logic arrays containing 32 product terms (AND terms) and six sum terms (OR terms). Each of the sum-of-products output functions can be programmed either high true or low true. The true condition of each output function is activated by the programmed logical minterms of 14 input variables. The outputs are controlled by two chip-enable pins to allow output inhibit and expansion of terms.

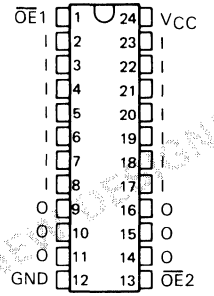
These devices provide high-speed data-path logic replacement where several conventional SSI functions can be designed into a single package.

The 'FPLA839C and 'FPLA840C are characterized for operation from 0°C to 70°C.

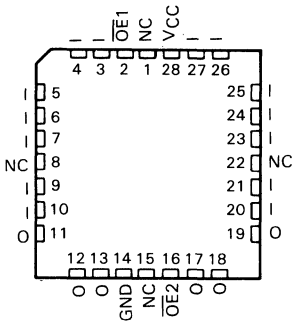
LOGIC FUNCTION

f(I) = P0 + P1 . . . P31 for polarity link intact
f(I) = $\overline{P0}$* $\overline{P1}$* . . . *$\overline{P31}$ for polarity link open
where P0 through P31 are product terms

JT OR NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode (pin 1 is less positive than V_{IHH})

NOT RECOMMENDED FOR NEW DESIGNS

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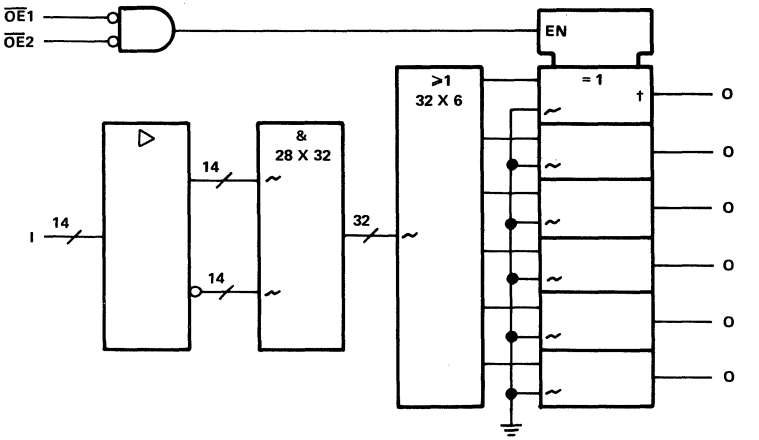
functional block diagram (positive logic)



~denotes fused inputs.
†FPLA839 has 3-state (▽) outputs; FPLA840 has open-collector (Ω) outputs.

absolute maximum ratings

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Off-state output voltage (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

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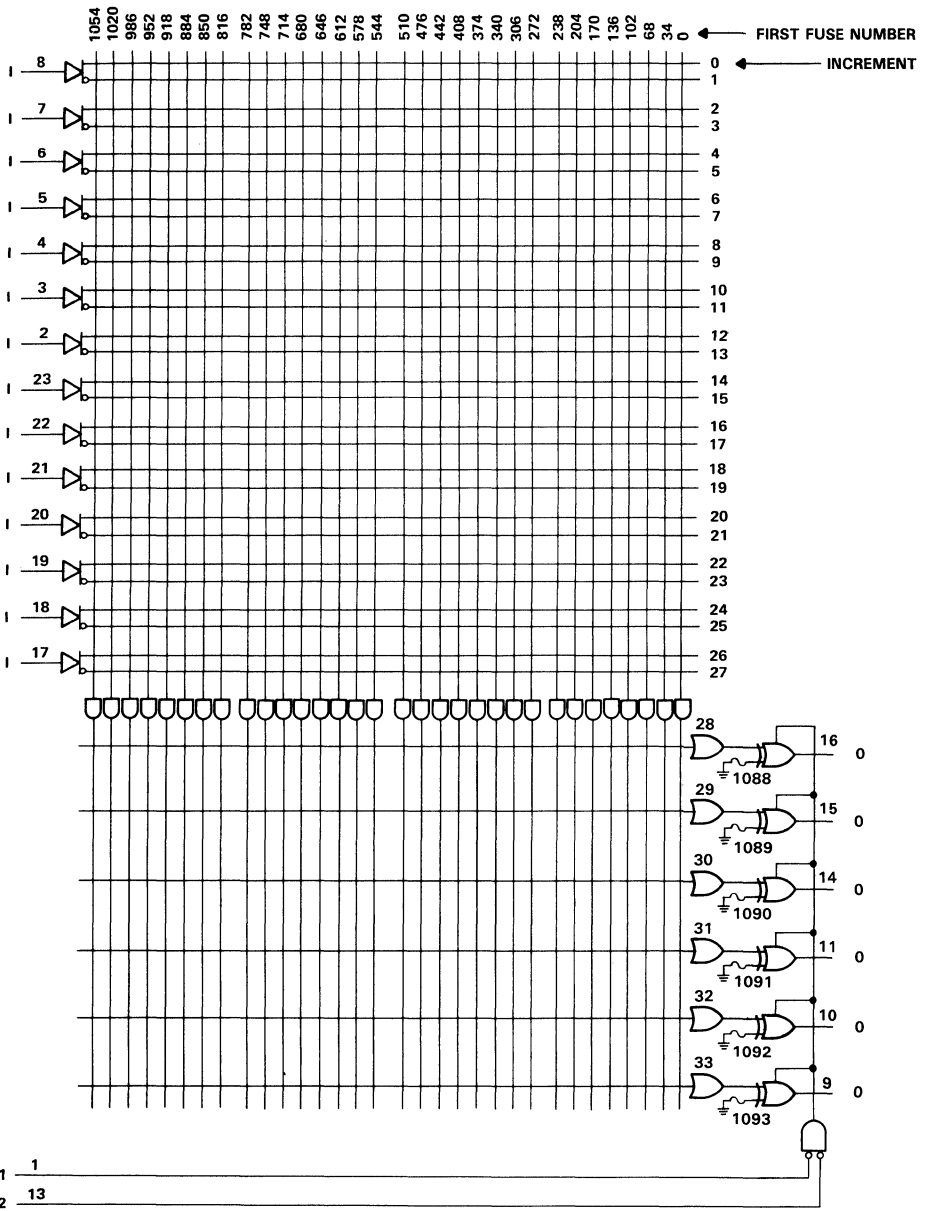
logic diagram



Fuse number = first fuse number + increment

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output voltage, V_{OH}	'FPLA840			5.5	V
High-level output current, I_{OH}	'FPLA839			−3.2	mA
Low-level output current, I_{OL}				24	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA			−1.5	V
I_{OH}	'FPLA840	V_{CC} = 4.75 V, V_{OH} = 5.5 V			0.1	mA
V_{OH}	'FPLA839	V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.37	0.5	V
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}		V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.25 V, V_I = 0.4 V			−0.5	mA
I_O‡		V_{CC} = 5.25 V, V_O = 2.25 V	−30		−112	mA
I_{OZH}		V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
I_{CC}		V_{CC} = 5.25 V, V_I = 0 V, $\overline{OE}$ inputs at V_{IH}		130	180	mA

'FPLA839 switching characteristics

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Input	Output	R1 = 500 Ω, R2 = 500 Ω, C_L = 50 pF, See Figure 1		10	20	ns
t_{en}	Pin 1 or Pin 13	Output			10	20	ns
t_{dis}					8	15	

'FPLA840 switching characteristics

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Input	Output	R1 = 500 Ω, R2 = 500 Ω, C_L = 50 pF, See Figure 1		10	25	ns
t_{en}	Pin 1 or Pin 13	Output			10	20	ns
t_{dis}					8	15	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.

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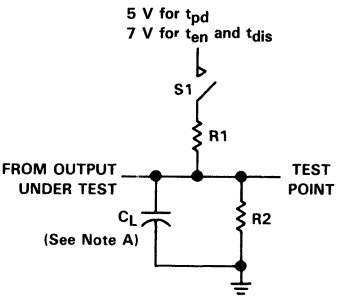
programming information

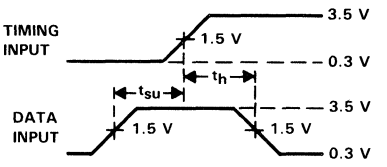
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

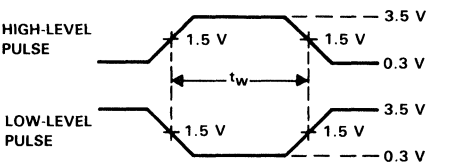
PARAMETER MEASUREMENT INFORMATION



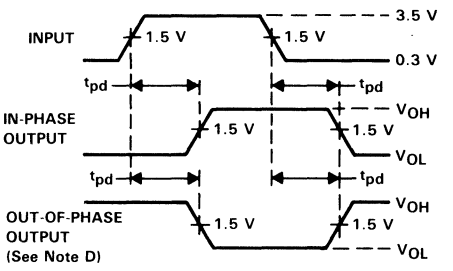
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



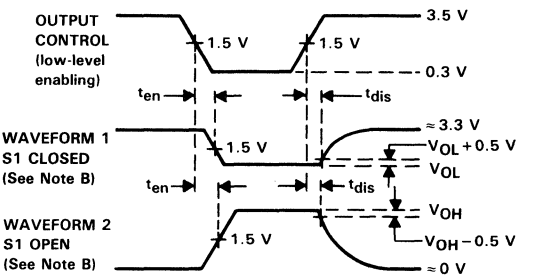
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

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Introduction to Designing with Programmable Logic

TEXAS
INSTRUMENTS

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PAL is a registered trademark of Monolithic Memories Incorporated.

Introduction

The purpose of this application report is to provide the first time user of programmable logic with a basic understanding of this powerful technology. The term Programmable Logic Device (PLD), refers to any device supplied with an uncommitted logic array, which the user programs to his own specific function.

Programmable Logic Advantages

Programmable logic devices (PLDs) offer many advantages to the system designer who presently is using several standard catalog SSI and MSI functions. Listed below are just a few of the benefits which are achievable when using programmable logic.

- Package Count Reduction: Several MSI/SSI functions can be replaced with one PLD. This reduces system power requirements.
- PC Board Area Reduced: Fewer devices consume less PC board space.
- Circuit Flexibility: Programmability allows for minor circuit changes without changing PC boards.
- Improved Reliability: With fewer PC interconnects, overall system reliability increases.
- Shorter Design Cycle: When compared with standard-cell or gate-array approaches, custom functions can be implemented much more quickly.
- Proprietary Design Protection (fuse protection): Circuit can be protected by blowing the security fuse.

The PLD will fill the gap between standard logic and large scale integration. The versatility of these devices provide a very powerful tool for the system designer.

Symbology for PLDs

In order to keep the PLDs easy to understand and use, a special convention has been adopted. Figure 1 is the representation for a 3-input AND gate. Note that only one line is shown as the input to the AND gate. This line is commonly referred to as the product line. The inputs are shown as vertical lines, and at the intersection of these lines are the programmable fuses. An X represents an intact fuse. This makes that input, part of the product term. No X represents a blown fuse. This means that input will not be part of the product term (in Figure 1, input B is not part of the product term). A dot at the intersection of any line represents a hard-wire connection.

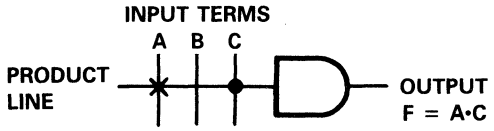


Figure 1. Basic Symbology

In Figure 2, we will extend the symbology to develop a simple 2-input programmable AND array feeding an OR gate. Notice that buffers have been added to the inputs, which provide both true and complement outputs to the product lines. The intersection of the input terms form a 4×3 programmable AND array. From the above symbology, we can see that the output of the OR gate is programmed to the following equation, $A\overline{B} + \overline{A}B$. Note that the bottom AND gate has an X marked inside the gate symbol. This means that all fuses are left intact, which results in that product line not having any effect on the sum term. In other words, the output of the AND gate will be a logic 0. **When all the fuses are blown on a product line, the output of the AND gate will always be a logic 1. This has the effect of locking up the output of the OR gate to a logic level 1.**

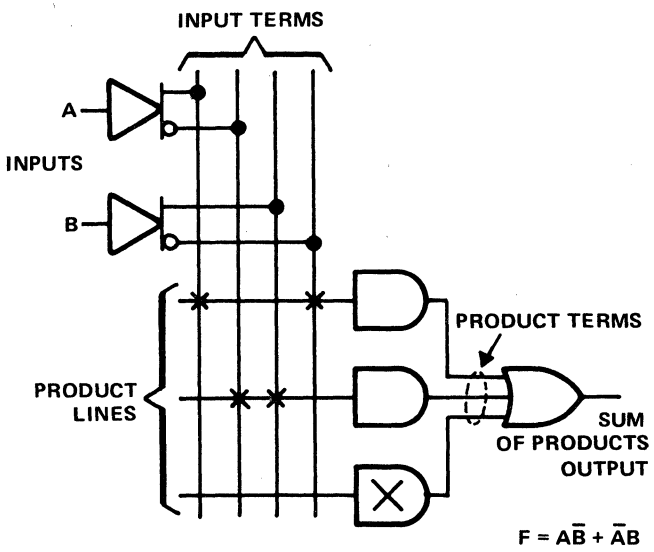


Figure 2. Basic Symbology Example

Family Architectures

The PROM was the first widely used programmable logic family. Its basic architecture is an input decoder configured from AND gates, combined with a programmable OR matrix on the outputs. As shown in Figure 3, this allows every output to be programmed

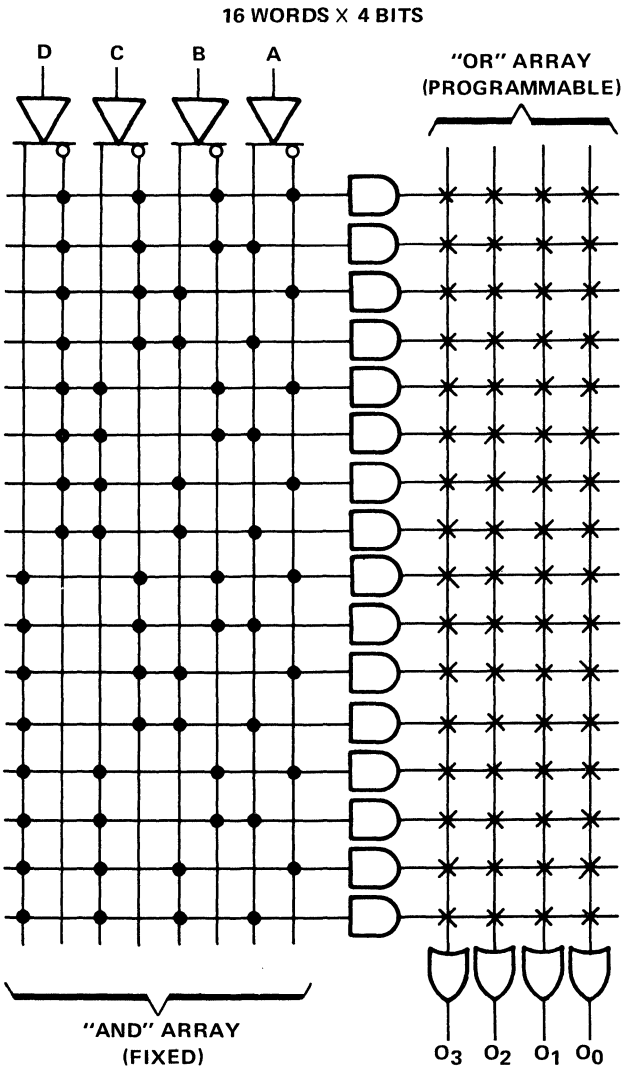


Figure 3. PROM Architecture

individually from every possible input combination. In this example, a PROM with 4 inputs has 2^4, or 16 possible input combinations. With the output word width being 4 bits, each of the 16×4 bit words can be programmed individually. Applications such as data storage tables, character generators, and code converters are just a few design examples which are ideally suited for the PROM. In general, any application which requires every input combination to be programmable is a good candidate for a PROM. However, PROMs have difficulty accomodating large numbers of input variables. Eventually, the size of the fuse matrix will become prohibitive because for each input variable added, the size of the fuse matrix doubles.

To overcome the limitation of a restricted number of inputs, the PAL utilizes a slightly different architecture as shown in Figure 4. The same AND-OR implementation is used as with PROMs, but now the input AND array is programmable instead of the output OR array. This has the effect of restricting the output OR array to a fixed number of input AND terms. The trade-off is that now, every output is not programmable from every input combination, but more inputs can be added without doubling the size of the fuse matrix. For example, if we were to expand the inputs on the PAL shown in Figure 4 to 10 and on the PROM in Figure 3 to 10, we would see that the fuse matrix required for the PAL would be 20×16 (320 fuses) vs 4×1024 (4096 fuses for the PROM). **It is important to realize that not every application requires every output to be programmable from every input combination. This is what makes the PAL a viable product family.**

The FPLA goes one step further in offering both a programmable AND array and a programmable OR array (Figure 5). This feature makes the FPLA the most versatile device of the three, but often impractical in most low complexity applications. For applications in which complex timing control is required, Texas Instruments offers several programmable state machines based on the FPLA architecture. Several of these devices incorporate internal state registers or on-chip binary counters to aid in generating complex timing sequences.

Another type of programmable logic device (PLD) is the erasable PLD. Based on the traditional PAL® architecture, these devices typically offer a higher level of flexibility in the input and output configuration, register selection, and clocking options. CMOS EPLDs provide a higher level of density over standard PLDs and have lower power dissipation characteristics than bipolar PLDs. All programmable logic approaches discussed have their own unique advantages and limitations. The best choice depends on the complexity of the function being implemented and the current cost of the devices themselves. It is important to realize that a circuit solution may exist for more than one of these logic families.

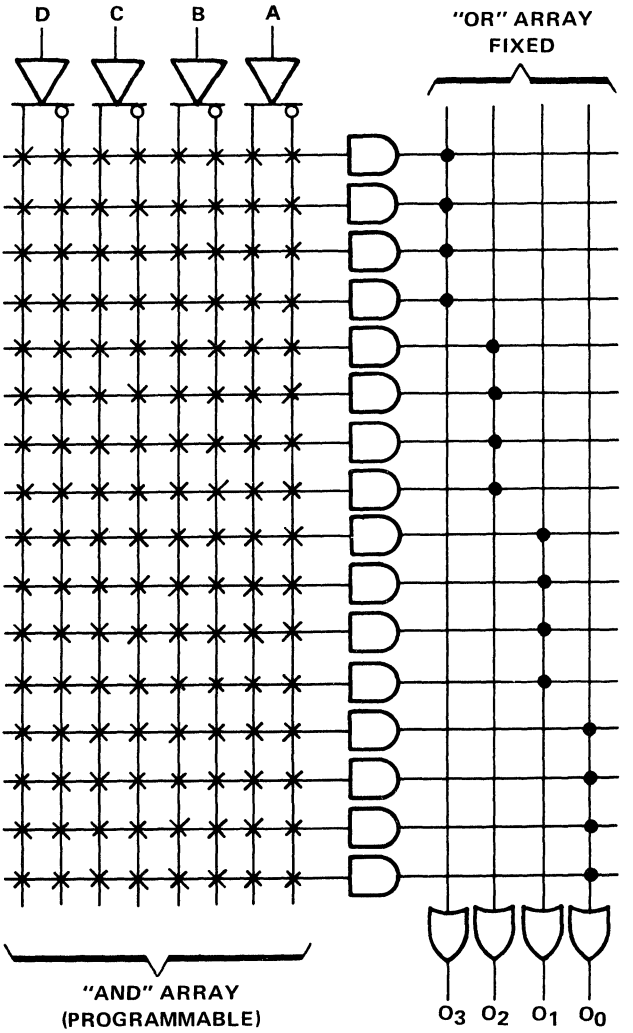


Figure 4. PAL® Architecture

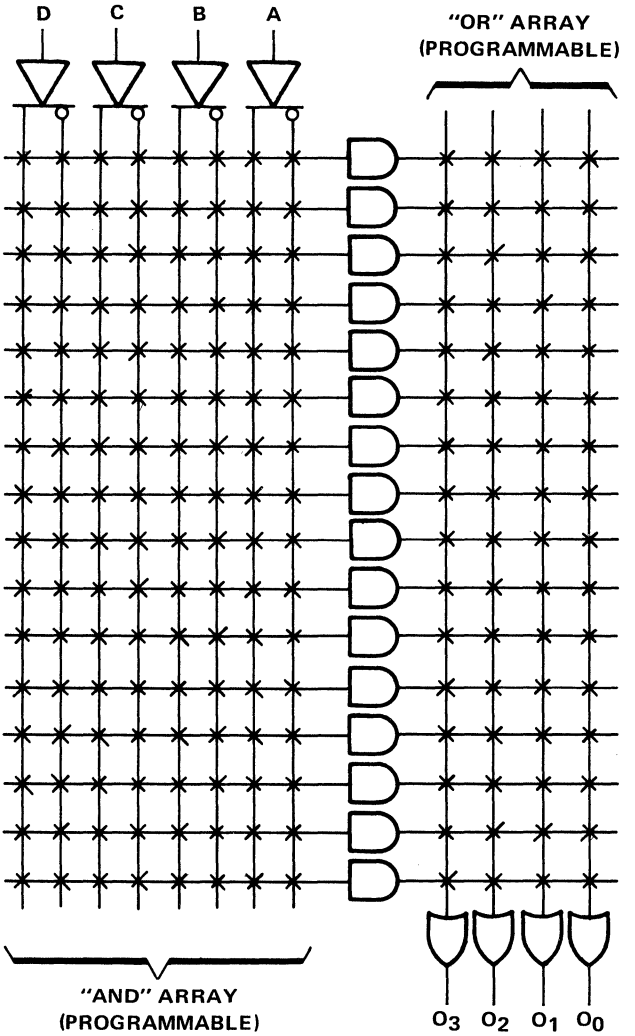


Figure 5. FPLA Architecture

PLD Options

Figure 6 shows the logic diagram of the popular TIBPAL16L8. Its basic architecture is the same as discussed in the previous section, but with the addition of some special circuit features. First, notice that the PAL has 10 simple inputs. In addition, 6 of the outputs operate as I/O ports. This allows feedback into the AND array. One AND gate in each product term controls each 3-state output. The architecture used in this PAL makes it very useful in generating all sorts of combinational logic.

Another important feature about the logic diagram and all other block diagrams supplied from individual datasheets are that there are no Xs marked at every fuse location. From the previous convention, we stated that everywhere there was an intact fuse, there was an X. However, in order to make the logic diagram useful when generating specific functions, it is supplied with no Xs. This allows the user to insert the Xs wherever an intact fuse is desired.

The basic concept of the TIBPAL16L8 can be expanded further to include D-type flip-flops on the outputs. An example of this is shown in Figure 7 with the TIBPAL16R8. This added feature allows the device to be configured as a counter, simple storage register, or similar clocked function.

Circuit variations which are available on other members of the TI PLD family are explained in the following paragraphs.

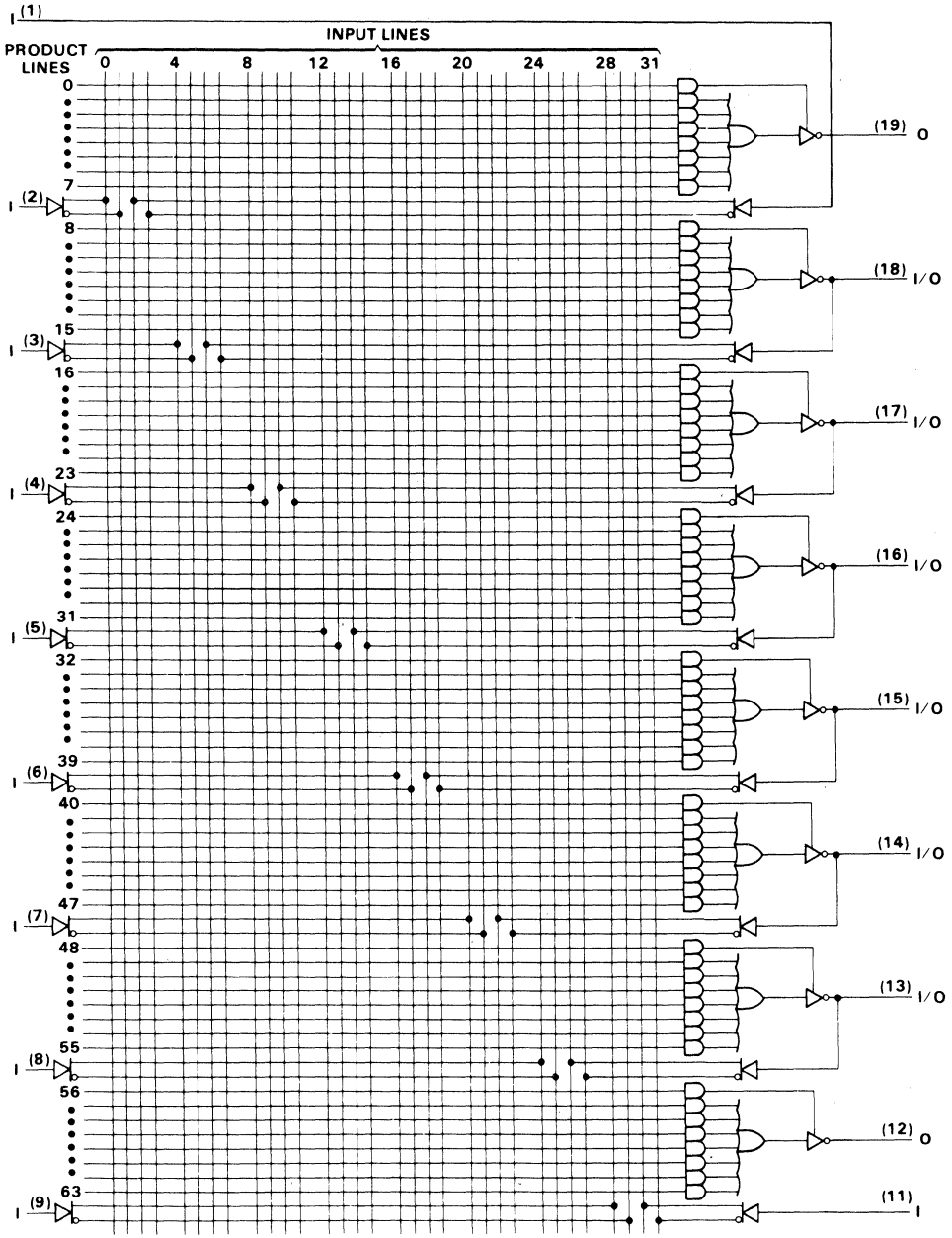


Figure 6. TIBPAL16L8 Logic Diagram

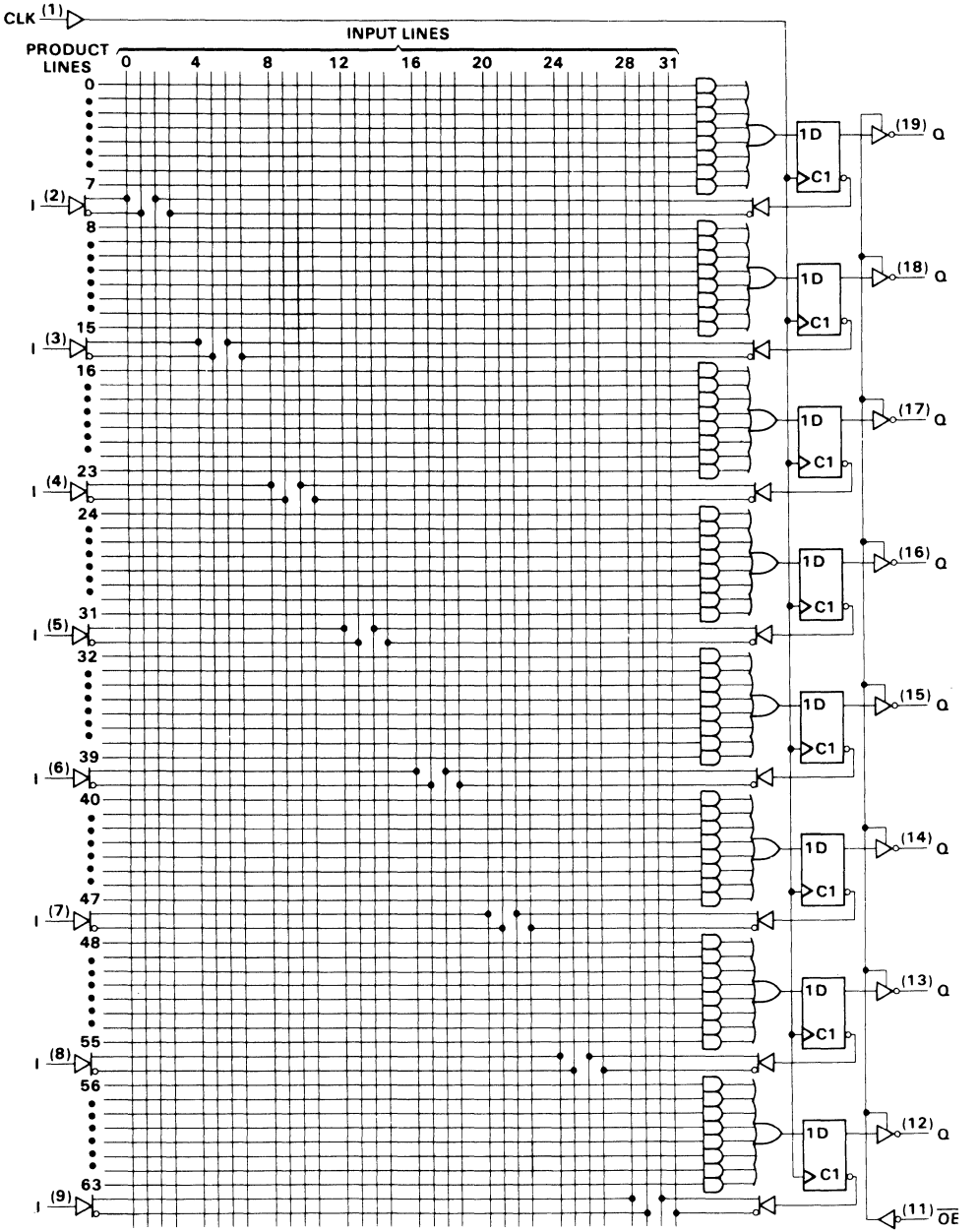


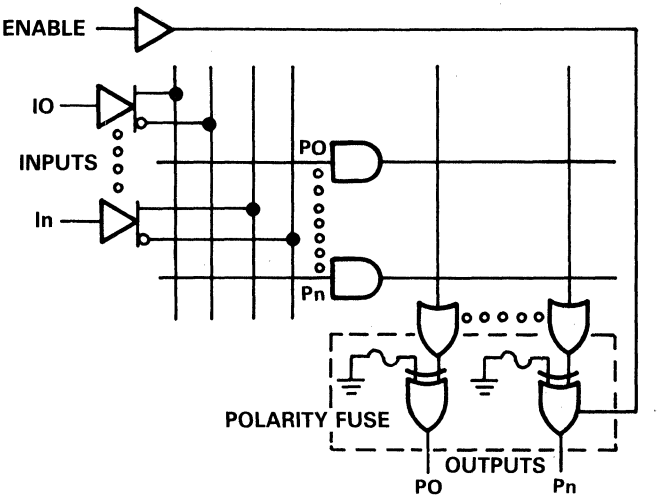
Figure 7. TIBPAL16R8 Logic Diagram

Output Macrocell

PLDs equipped with the output macrocell offer total output flexibility. Figures 8 and 9 show examples of these types of features as implemented in the TIBPAL22V10 device. Fuses S0 and S1 allow selection between registered or combinational outputs as well as output polarity. Figure 10 illustrates the user options.

The user options are as follows:

1. Clock Polarity Select. The clock signal can be inverted via a clock polarity select fuse. This allows the transition of the register outputs to be on either the positive or negative edge of the clock pulse.
2. Internal-State Registers. Several devices offer internal-state registers, which are often called buried registers. With the internal-state register, the output of the register is fed back into the AND array rather than to an output pin. This feature can be used for timing control sequences.
3. Variable Product Terms. Some PAL® device architectures vary the number of product terms associated with each output pin. This allows better utilization of the programmable array.



INTACT: OUTPUT = $\overline{P0} + \overline{P1} + \ldots + Pn$
BLOWN: OUTPUT = $\overline{P0} \cdot \overline{P1} \cdot \ldots \cdot \overline{Pn}$

Figure 8. Polarity Selection

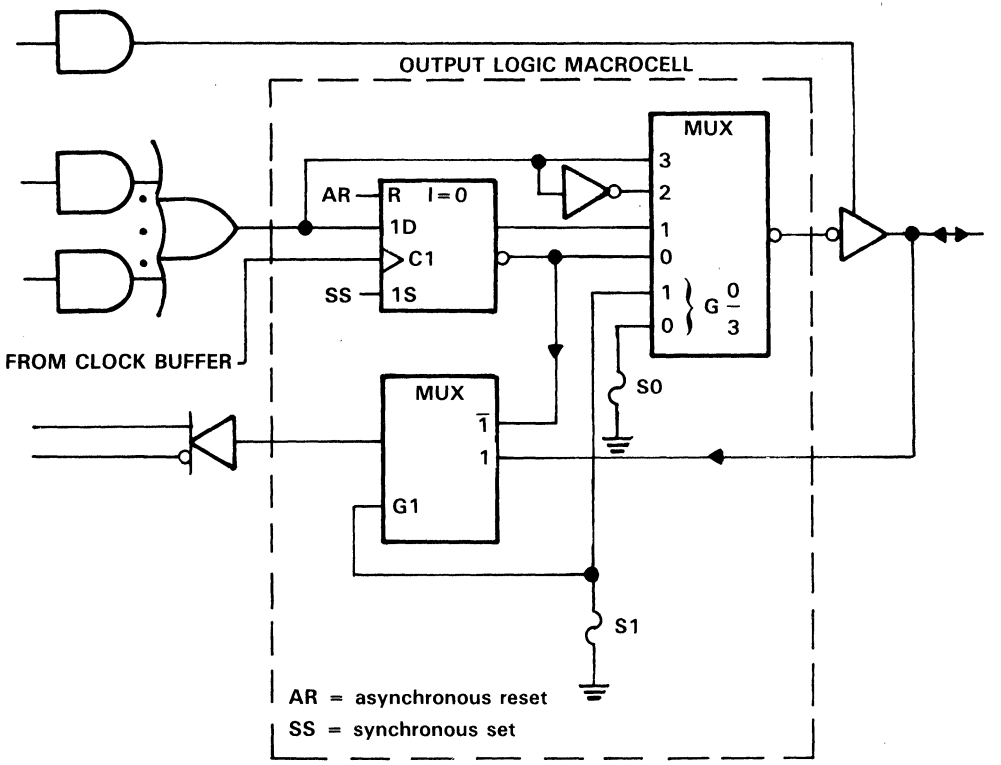
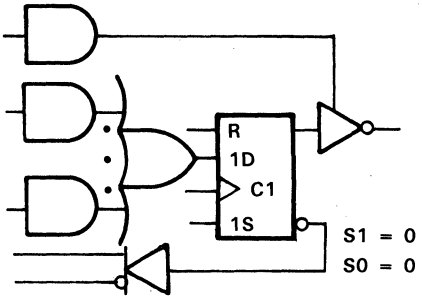
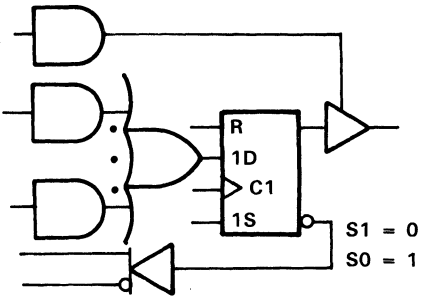


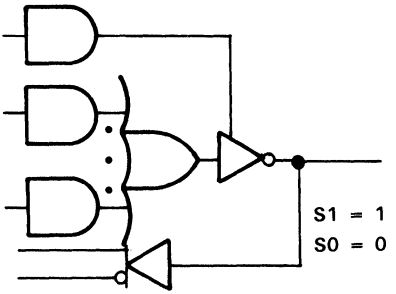
Figure 9. Output Macrocell Diagram



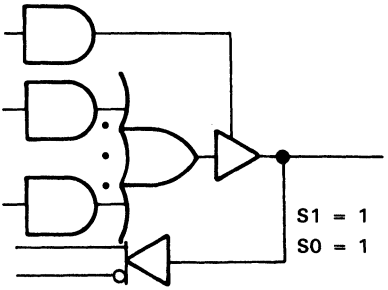
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse
S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Figure 10. Resultant Macrocell Feedback and Output Logic After Programming

Design Example

The easiest way to demonstrate the unique capabilities of the PLD is through a design example. Through this example, the reader will gain the basic understanding needed to apply a PLD in his own application. In some cases, this goal may only be to reduce existing logic, but the overall approach will be the same.

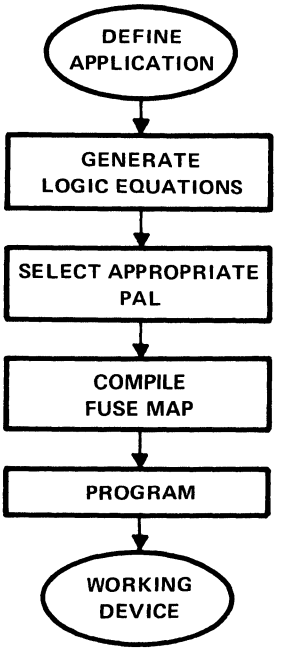


Figure 11. PLD Process Flow Diagram

Example Requirements

This example will generate a 4-bit binary counter which is fed by one of four clocks. There are two lines available for selecting the clocks, SEL1 and SEL0. Table 1 shows the required input for the selection of the clocks. In addition, it is desired that the counter be able to switch from binary to decade count. This feature is controlled by an input called BD. When BD is high, the counter will count in binary. When low, the counter will count in decade.

Table 1. Clock Selection

SEL1	SEL0	OUTPUT
0	0	CLKA
0	1	CLKB
1	0	CLKC
1	1	CLKD

Figure 12 shows this example is implemented using standard logic. As shown, three MSI functions are required. The 'LS162 is used to generate the 4-bit counter while the clock selection is handled by the 'LS253. The 'LS688 is an 8-bit comparator which is used for selecting either the binary or decade count. In this example, only five of the eight comparator inputs are used. Four are used for comparing the counter outputs, while the other is used for the BD input. The comparator is hard wired to go low whenever the BD input is low and the counter output is "9". The $\overline{P=Q}$ output is then fed back to the synchronous clear input on the 'LS162. This will reset the counter to zero whenever this condition occurs.

PLD Implementation

As stated before, the problem in programming a PAL is not in programming the fuses, but rather what fuses need to be programmed to generate a particular function. Fortunately, this problem has been greatly simplified by computer software. But before we examine these techniques, it is beneficial to explore the methods used in generating the logic equations. This will help develop an understanding and appreciation for these advanced software packages.

From digital logic theory, we know that almost any type of logic can be implemented in either AND-OR-INVERT or AND-NOR form. This is the basic concept used in the PLD. This allows classical techniques, such as Karnaugh Maps[1] to be used in generating specific logic functions. As with the separate component example (see Figure 12), it is easier to break it into separate functions. The first one that we will look at is the clock selector, but remember that the overall goal will be to reduce this design example into one PLD.

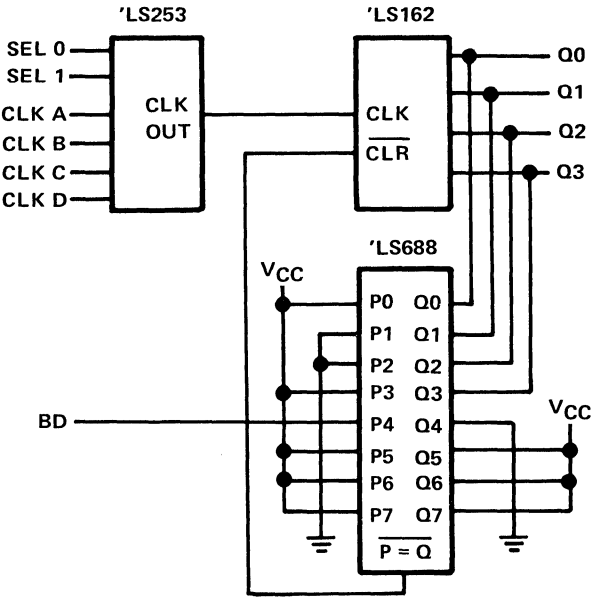


Figure 12. Counter Implementation with Standard Logic

PLD Selection

Before proceeding with the design for the clock selector, the first question which needs to be addressed is which PLD to use. As discussed earlier, there are several different types of output architectures. Looking at our example, we can see that four flip-flops with feedback will be required in the 4-bit counter, plus input clock and clear lines. In addition, seven inputs plus two simple outputs will be required in the clock selector and comparator. With this information in hand, we can see that the TIBPAL16R4 (Figure 13) will handle our application.

Clock Selector Details

The first step in determining the logic equation for the clock selector is to generate a function table with all the possible input combinations. This is shown in Table 2. From this table, the Karnaugh map can be generated and is shown in Figure 14. The minimized equation for CLKOUT comes directly from this.

Table 2. Function Table

SEL1	SEL0	CLKA	CLKB	CLKC	CLKD	CLKOUT	SEL1	SEL0	CLKA	CLKB	CLKC	CLKD	CLKOUT
0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	1	0	1	0	0	0	0	1	0
0	0	0	0	1	0	0	1	0	0	0	1	0	1
0	0	0	0	1	1	0	1	0	0	0	1	1	1
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	1	0	1	0	0	1	0	1	0
0	0	0	1	1	0	0	1	0	0	1	1	0	1
0	0	0	1	1	1	0	1	0	0	1	1	1	1
0	0	1	0	0	0	1	1	0	1	0	0	0	0
0	0	1	0	0	1	1	1	0	1	0	0	1	0
0	0	1	0	1	0	1	1	0	1	0	1	0	1
0	0	1	0	1	1	1	1	0	1	0	1	1	1
0	0	1	1	0	0	1	1	0	1	1	0	0	0
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0	0	1	1	1	0	1	1	0	1	1	1	0	1
0	0	1	1	1	1	1	1	0	1	1	1	1	1
0	1	0	0	0	0	0	1	1	0	0	0	0	0
0	1	0	0	0	1	0	1	1	0	0	0	1	1
0	1	0	0	1	0	0	1	1	0	0	1	0	0
0	1	0	0	1	1	0	1	1	0	0	1	1	1
0	1	0	1	0	0	1	1	1	0	1	0	0	0
0	1	0	1	0	1	1	1	1	0	1	0	1	1
0	1	0	1	1	0	1	1	1	0	1	1	0	0
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0	1	1	1	1	0	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1

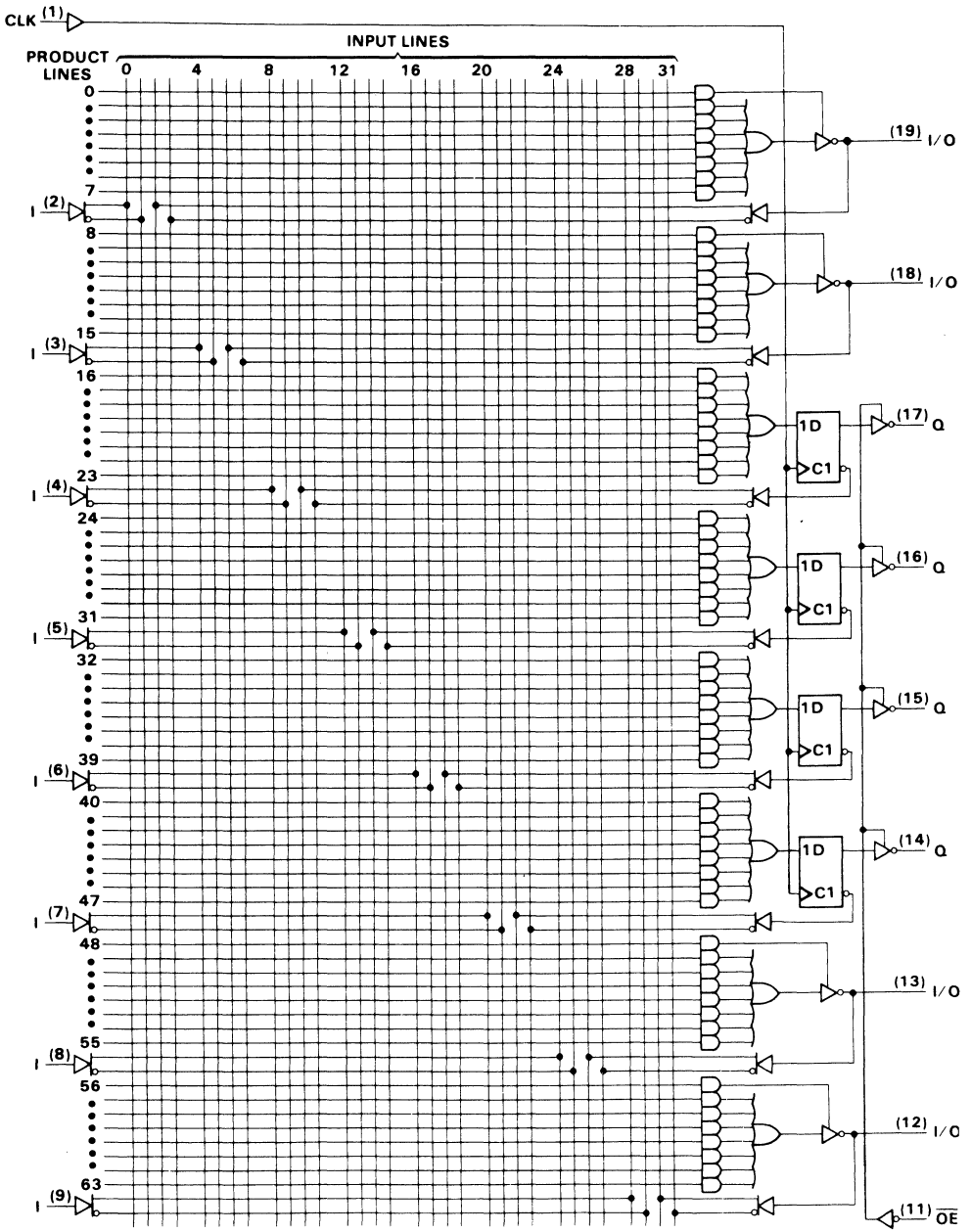
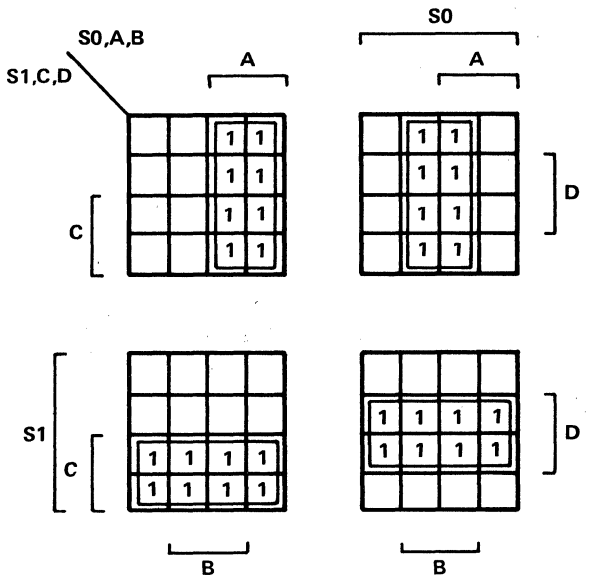


Figure 13. TIBPAL16R4 Logic Diagram

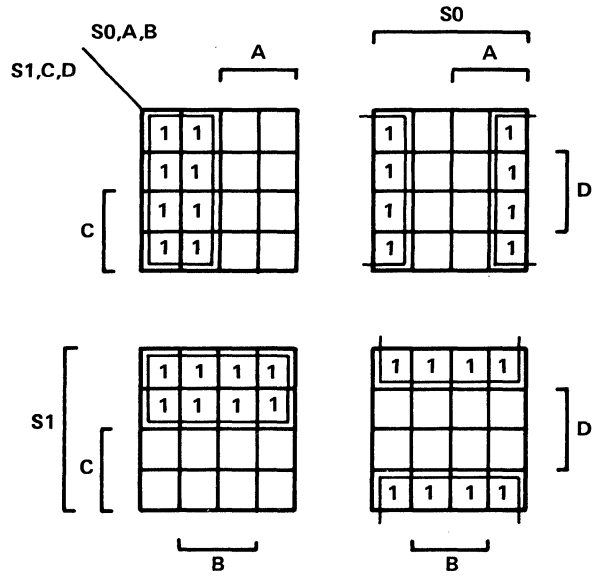
It is important to notice that the equation derived from the Karnaugh map is stated in AND-OR notation. The PLD that we have selected is implemented in AND-NOR logic. This means we either have to do DeMorgan's theorem on the equation or solve the inverse of the Karnaugh map. Figure 15 shows the inverse of the Karnaugh map and the resulting equation. This equation can be easily implemented in the TIBPAL16R4.



$$CLKOUT = \overline{S1}\,\overline{S0}A\overline{C}\overline{D} + \overline{S1}S0A\overline{B}\overline{C}\overline{D} + S1\overline{S0}A\overline{B}C\overline{D} + S1S0A\overline{B}\overline{C}D$$

$$CLKOUT = \overline{S1}\,\overline{S0}A + \overline{S1}S0B + S1\overline{S0}C + S1S0D$$

Figure 14. Karnaugh Map for CLKOUT



$$\overline{CLKOUT} = \overline{S1}\,\overline{S0}A\overline{B}\overline{C}\overline{D} + \overline{S1}S0\overline{A}\overline{B}\overline{C}\overline{D} + S1\overline{S0}\overline{A}\overline{B}C\overline{D} + S1S0\overline{A}\overline{B}\overline{C}D$$

$$\overline{CLKOUT} = \overline{S1}\,\overline{S0}\overline{A} + \overline{S1}S0\overline{B} + S1\overline{S0}\overline{C} + S1S0\overline{D}$$

Figure 15. Karnaugh Map for $\overline{CLKOUT}$

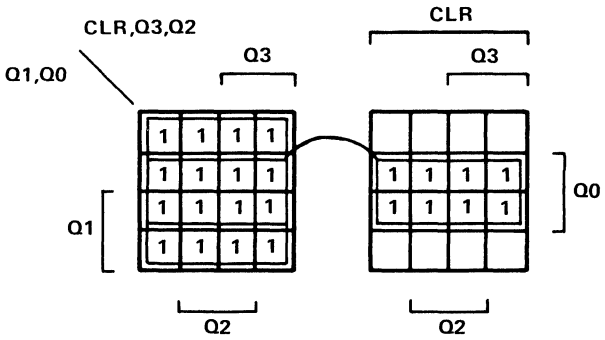
4-Bit Binary Counter Details

The same basic procedure used in determining the equations for the clock selector is used in determining the equations for the 4-bit counter. The only difference is that now we are dealing with a present state, next state situation. This means a D-type flip-flop will be required in actual circuit implementation. As before, the truth table is generated first and is shown in Table 3.

Table 3. Truth Table

	PRESENT STATE				NEXT STATE			
CLR	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	X	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	1	1
1	0	0	1	1	0	1	0	0
1	0	1	0	0	0	1	0	1
1	0	1	0	1	0	1	1	0
1	0	1	1	0	0	1	1	1
1	0	1	1	1	1	0	0	0
1	1	0	0	0	1	0	0	1
1	1	0	0	1	1	0	1	0
1	1	0	1	0	1	0	1	1
1	1	0	1	1	1	1	0	0
1	1	1	0	0	1	1	0	1
1	1	1	0	1	1	1	1	0
1	1	1	1	0	1	1	1	1
1	1	1	1	1	0	0	0	0

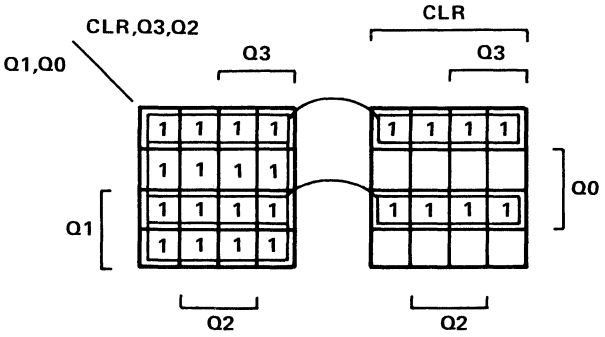
From the truth table, the equations for each output can be derived from the Karnaugh map. This is shown in Figure 16. Note that the inverse of the truth table is being solved so that the equation will come out in AND-NOR logic form.



$\overline{Q0} = \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}\overline{Q0} + CLR\,Q3\,Q2\,Q1\,Q0$

$\overline{Q0} = \overline{CLR} + Q0$

(a) Karnaugh Map for $\overline{Q0}$

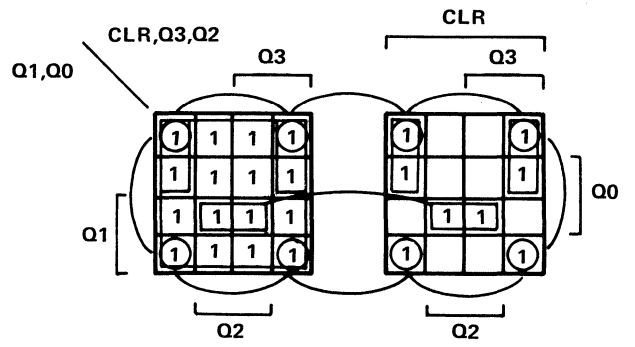


$\overline{Q1} = \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}\overline{Q0} + CLR\,Q3\,Q2\,\overline{Q1}\,\overline{Q0} + CLR\,Q3\,Q2\,Q1\,Q0$

$\overline{Q1} = \overline{CLR} + \overline{Q1}\,\overline{Q0} + Q1\,Q0$

(b) Karnaugh Map for $\overline{Q1}$

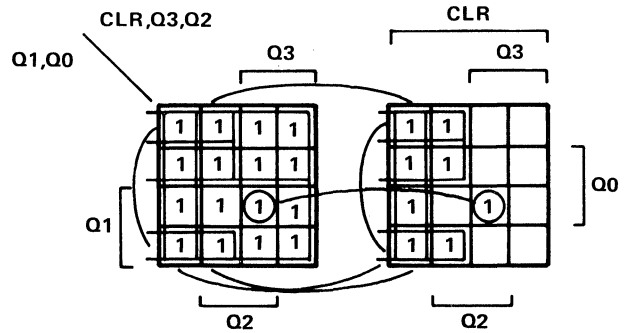
Figure 16. Karnaugh Maps



$\overline{Q2} = \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}\overline{Q0} + \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}Q0 + \overline{CLR}\overline{Q3}Q2Q1Q0 + \overline{CLR}\overline{Q3}Q2\overline{Q1}Q0$

$\overline{Q2} = \overline{CLR} + \overline{Q2}\overline{Q1} + Q2Q1Q0 + \overline{Q2}\overline{Q0}$

(c) Karnaugh Map for $\overline{Q2}$



$\overline{Q3} = \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}\overline{Q0} + \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}Q0 + \overline{CLR}\overline{Q3}\overline{Q2}Q1\overline{Q0} + \overline{CLR}\overline{Q3}Q2\overline{Q1}\overline{Q0}$

$\overline{Q3} = \overline{CLR} + \overline{Q3}\overline{Q2} + \overline{Q3}\overline{Q1} + \overline{Q3}\overline{Q0} + Q3Q2Q1Q0$

(d) Karnaugh Map for $\overline{Q3}$

Figure 16. Karnaugh Maps (Continued)

Binary/Decade Count Details

Recalling from the example requirements that the counter should count in decade whenever the BD input is low, we can again generate a truth table for this function (Table 4). Since the counter is already designed to count in binary, we can use this feature to simplify our design. What we desire is a circuit whose output goes low, whenever the BD input is equal to a logic level "0", and the counter output is equal to "9". This output can then be fed back to the CLR input of the counter so that it will reset whenever the BD input is low. Whenever the BD input is high, the output of the circuit should be a high since the counter will automatically count in binary. Notice that $\overline{Q}$ shown in the truth table is the function we desire.

Table 4. Truth Table

BD	Q3	Q2	Q1	Q0	Q	$\overline{Q}$	BD	Q3	Q2	Q1	Q0	Q	$\overline{Q}$
0	0	0	0	0	0	1	1	0	0	0	0	0	1
0	0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	0	0	1	1	0	0	1	0	0	1
0	0	0	1	1	0	1	1	0	0	1	1	0	1
0	0	1	0	0	0	1	1	0	1	0	0	0	1
0	0	1	0	1	0	1	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	1	0	0	1
0	0	1	1	1	0	1	1	0	1	1	1	0	1
0	1	0	0	0	0	1	1	1	0	0	0	0	1
0	1	0	0	1	0	1	1	1	0	0	1	0	1
0	1	0	1	0	0	1	1	1	0	1	0	0	1
0	1	0	1	1	0	1	1	1	0	1	1	0	1
0	1	1	0	0	0	1	1	1	1	0	0	0	1
0	1	1	0	1	0	1	1	1	1	0	1	0	1
0	1	1	1	0	0	1	1	1	1	1	0	0	1
0	1	1	1	1	0	1	1	1	1	1	1	0	1

In this particular example, a Karnaugh map is not required because the equation cannot be further simplified. The resulting equation is given below.

$$\overline{BD\ OUT} = \overline{BD}Q3\overline{Q2}\overline{Q1}Q0$$

Fuse Map Details

Now that the logic equations have been defined, the next step will be to specify which fuses need to be programmed. Before we do this however, we first need to label the input and output pins on the TIBPAL16R4. By using Figure 12 as a guide, we can make the following pin assignments in Figure 17.

PIN:

1	CLK	20	V_{CC}
2	SEL0	19	CLKOUT
3	SEL1	18	NC
4	CLKA	17	Q0
5	CLKB	16	Q1
6	CLKC	15	Q2
7	CLKD	14	Q3
8	CLR	13	NC
9	BD	12	BD OUT
10	GND	11	OE

With this information defined, we now need to insert the logic equations into the logic diagram as shown in Figure 17.

It is now probably obvious to the reader, that inserting the logic equations into the logic diagram is a tedious operation. Fortunately, several software programs are available to perform this task automatically. All that is required is telling the program which device has been selected and defining the input and output pins with their appropriate logic equations. The program will then generate a fuse map for the device selected. This information can then be down loaded into the selected device programmer.

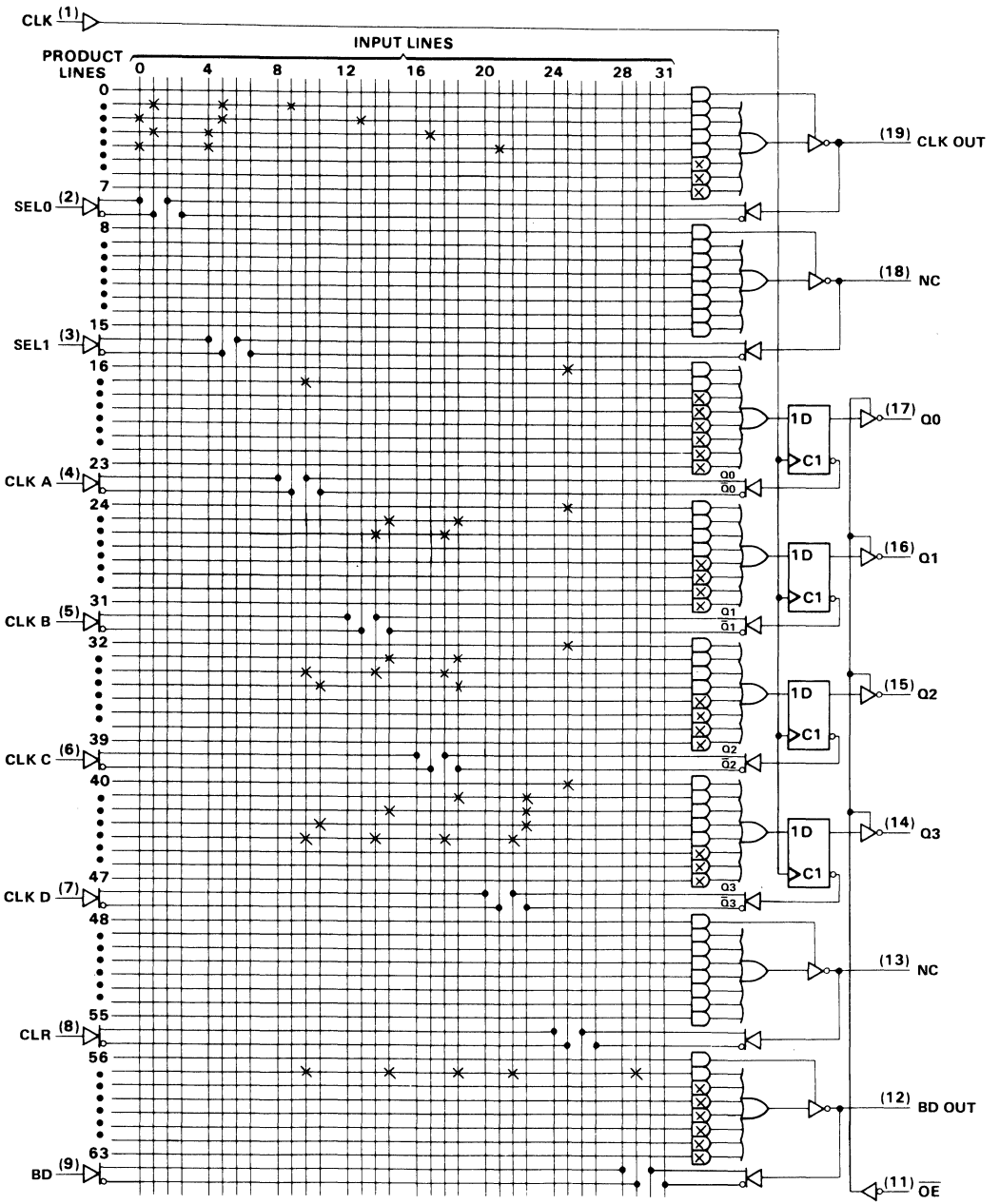


Figure 17. Programmed TIBPAL16R4

PLD Design Software

Software packages such as ABEL™, CUPL™, and proLogic™ not only generate the fuse map, but they also help in developing the logic equations. In most cases, they can generate the logic equations from simply providing the program with either a truth table or state diagram. In addition, they can test the logic equations against a set of test vectors. This helps to ensure the that designer gets the desired function.

Several software packages are described in further detail in this data book. The Programmable Logic Device Design Software Support section provides a detailed summary of the capabilities of several of these popular design tools.

As an example, we will approach our previous design utilizing DATA I/O's ABEL™ package. The purpose here is not to teach the reader how to use ABEL™, but rather to give them a basic overview of this powerful software package. Figure 18 shows the source file required by ABEL™. Note that the 4-bit counter has been described with a state diagram table. When the ABEL™ program is compiled, the logic equations will be generated from this. The equations for CLK OUT and BD OUT are given in their final form to demonstrate how ABEL™ will handle these. Also notice that test vectors are included for checking the logic equations. This is especially important when only the logic equations are given.

Figure 19 shows some of the output documentation generated by the program. Notice that the equations generated for the counter match the ones generated by the Karnaugh maps. A pinout for the device has also been generated and displayed. The fuse map for the device has not been shown; however, the standard JEDEC fuse map thus generated can be down loaded into the device programmer to program the selected PLD.

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proLogic is a trademark of Inlab Inc.

```
module BD_COUNT flag '-r2'
title '4-bit binary/decade counter


      IC1  device 'P16R4';

"  pin assignments and constant declarations
      CLK_IN,SEL0,SEL1,CLKA    pin  1,2,3,4;
      CLKB,CLKC,CLKD           pin  5,6,7;
      CLR,BD_IN,OE             pin  8,9,11;
      BD_OUT,CLK_OUT           pin  12,19;
      Q3,Q2,Q1,Q0              pin  14,15,16,17;
      CK, L, H, X, Z  =        .C. , 0 , 1 , .X. , .Z.;
      OUTPUT           =       [Q3,Q2,Q1,Q0];

"  counter states
      S0=^b0000;   S4=^b0100;   S8=^b1000;   S12=^b1100;
      S1=^b0001;   S5=^b0101;   S9=^b1001;   S13=^b1101;
      S2=^b0010;   S6=^b0110;  S10=^b1010;   S14=^b1110;
      S3=^b0011;   S7=^b0111;  S11=^b1011;   S15=^b1111;

equations
"  clock selector
      CLK_OUT = CLKA & !SEL0 & !SEL1 # CLKB & !SEL1 & SEL0
                # CLKC & SEL1 & !SEL0 # CLKD & SEL1 & SEL0;

"  count nine indicator for decade counting
      BD_OUT  = !(!BD_IN & Q3 & !Q2 & !Q1 & Q0);

state_diagram [Q3,Q2,Q1,Q0]
      State  S0:  IF CLR == 0 THEN S0 ELSE  S1;
      State  S1:  IF CLR == 0 THEN S0 ELSE  S2;
      State  S2:  IF CLR == 0 THEN S0 ELSE  S3;
      State  S3:  IF CLR == 0 THEN S0 ELSE  S4;
      State  S4:  IF CLR == 0 THEN S0 ELSE  S5;
      State  S5:  IF CLR == 0 THEN S0 ELSE  S6;
      State  S6:  IF CLR == 0 THEN S0 ELSE  S7;
      State  S7:  IF CLR == 0 THEN S0 ELSE  S8;
      State  S8:  IF CLR == 0 THEN S0 ELSE  S9;
      State  S9:  IF CLR == 0 THEN S0 ELSE S10;
      State S10:  IF CLR == 0 THEN S0 ELSE S11;
      State S11:  IF CLR == 0 THEN S0 ELSE S12;
      State S12:  IF CLR == 0 THEN S0 ELSE S13;
      State S13:  IF CLR == 0 THEN S0 ELSE S14;
      State S14:  IF CLR == 0 THEN S0 ELSE S15;
      State S15:  IF CLR == 0 THEN S0 ELSE  S0;

test_vectors   'clock selector'
     ([CLKA, CLKB, CLKC, CLKD, SEL1, SEL0] -> CLK_OUT)
      [ L  ,  X  ,  X  ,  X  ,  L,    L ] ->    L;
      [ H  ,  X  ,  X  ,  X  ,  L,    L ] ->    H;
      [ X  ,  L  ,  X  ,  X  ,  L,    H ] ->    L;
      [ X  ,  H  ,  X  ,  X  ,  L,    H ] ->    H;
      [ X  ,  X  ,  L  ,  X  ,  H,    L ] ->    L;
      [ X  ,  X  ,  H  ,  X  ,  H,    L ] ->    H;
      [ X  ,  X  ,  X  ,  L  ,  H,    H ] ->    L;
      [ X  ,  X  ,  X  ,  H  ,  H,    H ] ->    H;
```

Figure 18. Source File for ABEL

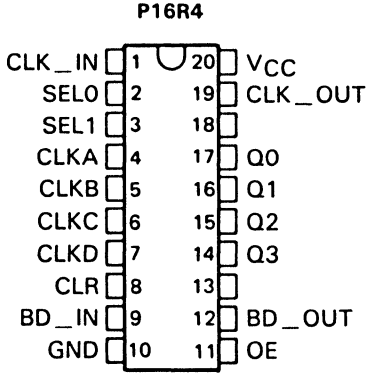
```
test_vectors    'counter'
      ([CLK_IN, OE, CLR, BD_IN] -> [OUTPUT, BD_OUT])
       [  CK,    L ,  L,     X  ] -> [  S0,   H ];
       [  CK,    L ,  H,     X  ] -> [  S1,   H ];
       [  CK,    L ,  H,     X  ] -> [  S2,   H ];
       [  CK,    L ,  H,     X  ] -> [  S3,   H ];
       [  CK,    L ,  H,     X  ] -> [  S4,   H ];
       [  CK,    L ,  H,     X  ] -> [  S5,   H ];
       [  CK,    L ,  H,     X  ] -> [  S6,   H ];
       [  CK,    L ,  H,     X  ] -> [  S7,   H ];
       [  CK,    L ,  H,     X  ] -> [  S8,   H ];
       [  CK,    L ,  H,     L  ] -> [  S9,   L ];
       [  CK,    L ,  H,     X  ] -> [ S10,   H ];
       [  CK,    L ,  H,     X  ] -> [ S11,   H ];
       [  CK,    L ,  H,     X  ] -> [ S12,   H ];
       [  CK,    L ,  H,     X  ] -> [ S13,   H ];
       [  CK,    L ,  H,     X  ] -> [ S14,   H ];
       [  CK,    L ,  H,     H  ] -> [ S15,   H ];
       [  CK,    I ,  H,     X  ] -> [  S0,   H ];
       [   X,    H ,  X,     X  ] -> [   Z ,  H ];
end BD_COUNT
```

Figure 18. Source File for ABEL (Continued)


```
ABEL(tm) Version  1.00  - Document Generator
4-bit binary/decade counter

Equations for Module BD_COUNT

Device IC1


     Reduced Equations:

       CLK_OUT = !((SEL1 & SEL0 & !CLKD
                  # (SEL1 & !SEL0 & !CLKC
                  # (!SEL1 & SEL0 & !CLKB
                  # !SEL1 & !SEL0 & !CLKA)));


       BD_OUT = !(Q3 & !Q2 & !Q1 & Q0 & !BD_IN);

       Q3 := !((Q3 & Q2 & Q1 & Q0
              # (!Q3 & !Q2
              # (!Q3 & !Q1
              # (!Q3 & !Q0
              # !CLR)))));


       Q2 := !((Q2 & Q1 & Q0 # (!Q2 & !Q1 # (!Q2 & !Q0 # !CLR))));

       Q1 := !((Q1 & Q0 # (!Q1 & !Q0 # !CLR)));

       Q0 := !((Q0 # !CLR));
```

Figure 19. ABEL Output Documentation

```
ABEL(tm) Version  1.00  - Document Generator
4-bit binary/decade counter

Chip diagram for Module BD_COUNT

Device IC1
```




```
end of module BD_COUNT
```

Figure 19. ABEL Output Documentation (Continued)

Reference

1. H. Troy Nagle, Jr., B.D. Carroll, and David Irwin, *An Introduction to Computer Logic*. New Jersey: Prentice-Hall, Inc., 1975.

Programmable Logic Device Design Software Support

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Programmable Logic Device Design Software Support

INTRODUCTION

There are a number of logic design software products available to the design engineer, intended to make logic design easier and less cumbersome. With these software products, complex designs can be described using Boolean equations, truth tables, state machine diagrams and schematic capture methods available on most CAD systems.

The ultimate function of these software products is to generate a JEDEC file of the original design to be programmed into the targeted Programmable Logic Device (PLD). However, most S/W vendors provide more than a JEDEC file as an output from the software. This section seeks to describe the attributes of a few of the popular logic design products. We recommend that the reader contact the specific manufactures to obtain the latest and most comprehensive information available.

ABEL™ – Advanced Boolean Expression Language by DATA I/O Corporation:

ABEL consists of a special-purpose, high-level language that is used to describe logic designs, and a language processor that converts logic descriptions to programmer load files – or JEDEC files. These files contain the information necessary to program and test programmable logic devices.

Features of ABEL design language:

- Universal syntax for all PLDs
- High-level, structered design language
- Flexible forms for logic description

  Boolean Equations
  Truth Tables
  State Diagrams

- Test Vectors for simulation and functional testing of programmed parts
- Time-Saving Macros and Directives

Some powerful features of the ABEL language processor:

- Syntax checking
- Verification that a design can be implemented with a chosen part
- Logic Reduction
- Design Simulation
- Automatic design documentation
- Creation of programmer load files in JEDEC format

Between the ABEL design language and the language processor it becomes rather easy to design and test logic functions to be implemented with a PLD. For example, a three-input AND function with the inputs Q, R, and S and an output P could be designed using a truth table like this:

```
truth_table "3-input AND gate"
 ([ Q, R, S ] -> P)

 [ 0, .X.,.X.] -> 0 ;

 [ X, .0.,.X.] -> 0 ;
 [ X, .X.,.0.] -> 0 ;

 [ 1, 1, 1 ] -> 1 ;
```

The ".X." in the table indicate "don't care" conditions, and the output P is set to 1 only when all three inputs equal 1. The output could also be specified in simple Boolean operators and achieve the same result. This is done here, where "&" is the logical AND operator:

```
P = Q & R & S;
```

More Boolean Operators

Operator	Example	Description
!	!A	NOT: ones complement
&	A & B	AND
#	A # B	OR
$	A $ B	XOR: exclusive OR
!$	A !$ B	XNOR:exclusive NOR

ABEL allows designs to be described in the best possible manner to suit the logic to be implemented or in a manner suitable to the logic designer. In most cases the same description can be used for many different devices simply by changing the device specified.

The logic design process using ABEL is shown in Figure 1. Beginning with the design concept, the designer creates the ABEL source file required by the language processor in order for it to generate the programmer load file. With the help of a text editor, the designer can create the source file which contains complete description of the logic design. The source file may also be created using DASH-ABEL to convert a DASH-generated schematic of a design

Logic Design Steps:

The source file is presented to the language processor which performs the several functions to produce a programmer load file (in JEDEC) format and all the required design documentation (see Figure 1.).

PARSE	checks the syntax of the source file and flags any errors.
TRANSFORM	converts the logic description to an intermediate form.
REDUCE	performs logic reduction.
FUSEMAP	creates the (JEDEC) programmer load file, which can then be downloaded to the logic programmer to program parts, or used to generate test vectors.
DOCUMENT	generates a listing of the source file, a drawing of the logic device pin assignments, and a listing of the programmer load file.

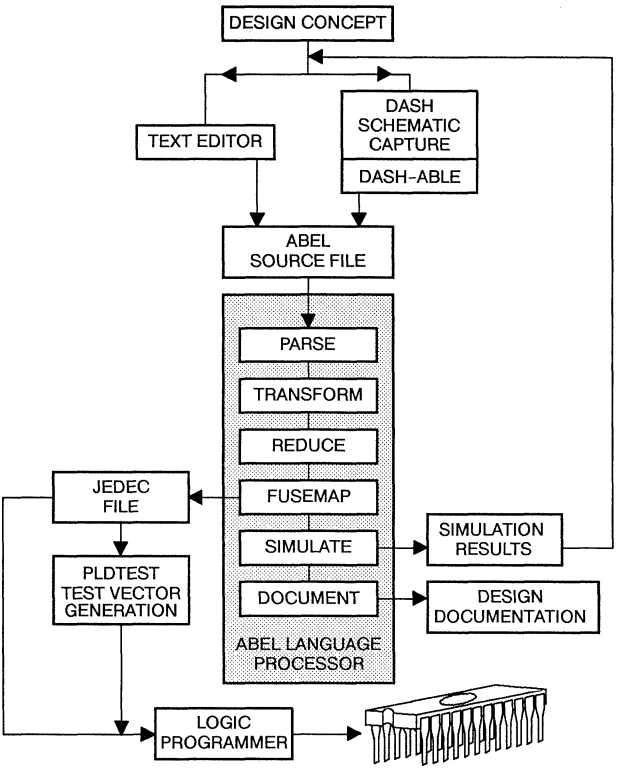


Figure 1. Logic Design Steps with ABEL

DESIGN EXAMPLES

The following two design examples highlight two design entry methods, Boolean equations and State Diagrams.

Three–State Sequencer

The following design is a simple sequencer that demonstrates the use of ABEL state diagrams. The design is implemented in a TIBPAL16R4–10 device (P16R4). There is no limit to the number of states that can be processed by ABEL, but the number of transitions and the path of the transitions is limited.

Figure 2. shows the sequencer design, with a bubble diagram showing the transitions and the desired outputs. The state machine starts in state A and remains in that state until the 'start' input becomes high. It then transitions from state A to state B, from state B to state C, and back to state A. It remains in state A until the 'start' input is high again. If the 'reset' input is high, the state machine returns to state A at the next clock cycle. If this reset to state A occurs during state B, an 'abort' synchronous output goes high, and remains high until the machine is again started.

During states B and C, asynchronous outputs 'in_B' and 'in_C' become high to indicate the current state. Activation of the 'hold' input will cause the machine to hold in state B or C until 'hold' is no longer high or 'reset' becomes high.

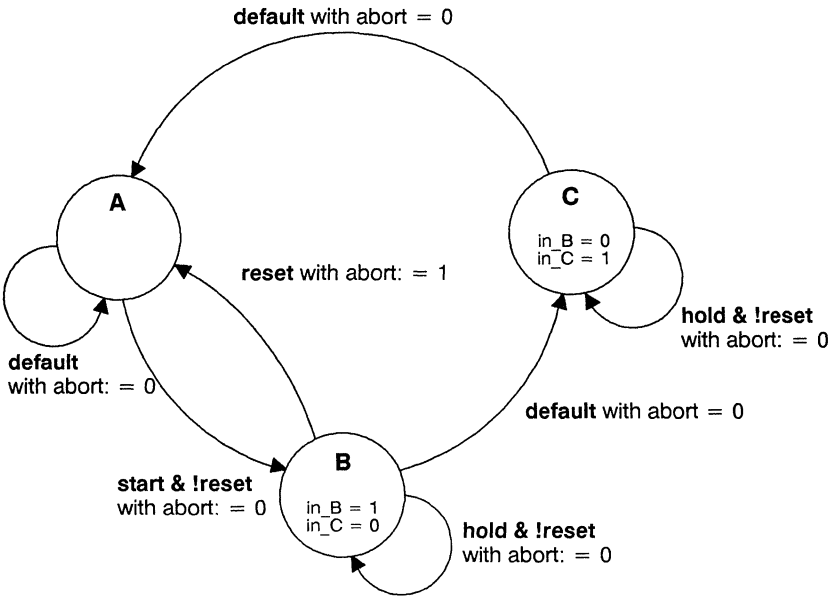


Figure 2. State Machine Bubble Diagram

Design Methodology

The sequencer is described by using a STATE_DIAGRAM section in the ABEL source file. The ABEL source file for the sequencer is shown in Figure 3. In this example, the design is given a title, the target device is specified, and pin declarations are made. The FLAG statement is used to select the level of reduction required. Constants are declared to simplify the state diagram notation. The two state registers are grouped into a set called 'sreg'. The three states A, B, and C are declared with appropriate values specified for each.

For larger state machines with more state bits, careful numbering of states can dramatically reduce the logic required to implement the design. Using constant declarations to specify state values saves time when later changes to these values are made.

The state diagram begins with the STATE_DIAGRAM statement that names the set of signals to be used for the state register. The set to be used is 'sreg'.

Within the STATE_DIAGRAM, IF-THEN-ELSE statements are used to indicate the transitions between states, and the input conditions that cause each transition. In addition, equations are written in each state that indicate the outputs required for each state or transition.

For example, state A reads:

```
State A:
  in_B = 0;
  in_C = 0;
  if (start & !reset) then B with abort := 0;
  else A with abort :=0;
```

This means that if the machine is in state A and 'start' is high, but 'reset' is low, then the machine will advance to state B, but in another input condition the machine will remain in sate A.

The equations for 'in_B' and 'in_C' indicate that those outputs should remain low while the machine is in state A, while the equations for 'abort', specified with the "with" keyword, indicate that 'abort' should go low if the machine transitions to state B, but should remain at its previous value if the machine stays in state A.

Test Vectors

The specification of the test vectors for this design is similar to those of any other synchronous designs. The first vector puts the machine into a known state (state A), and the following vectors exercise the functions of the machine. The A, B, and C constants are used in the vectors to indicate the value of the current state, thus improving the readability of the vectors.

```
title '8-bit barrel shifter
Gerrit Barrere    Data I/O Corp  Redmond WA   17 Oct 1987'

module sequence        flag '-r3'
title 'State machine example        D. B. Pellerin - Data I/O';

          d1          device      'p16r4';

          q1,q0                                pin        14,15;
          clock,enab,start,hold,reset          pin        1,11,4,2,3;
          abort                                pin        17;
          in_B,in_C                            pin        12,13;
          sreg                                    =       [q1,q0];

      "State Values...
          A = 0;                B = 1;                C = 2;

state_diagram sreg;
          State A:              " Hold in state A until start is active.
            in_B = 0;
            in_C = 0;
            IF (start & !reset) THEN B WITH abort := 0;
            ELSE A WITH abort := abort;

          State B:              " Advance to state C unless reset is active
            in_B = 1;           " or hold is active. Turn on abort indicator
            in_C = 0;           " if reset.
            IF (reset) THEN A WITH abort := 1;
            ELSE IF (hold) THEN B WITH abort := 0;
            ELSE C WITH abort := 0;

          State C:              " Go back to A unless hold is active
            in_B = 0;           " Reset overrides hold.
            in_C = 1;
            IF (hold & !reset) THEN C WITH abort := 0;
            ELSE A WITH abort := 0;
   [q0, q1] = !RESET
test_vectors([clock,enab,start,reset,hold]->[sreg,abort,in_B,in_C])
             [ .c. ,  0 ,  0  ,  0  ,  0 ]->[  A ,  0  ,  0 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  0 ]->[  A ,  0  ,  0 ,  0 ];
             [ .c. ,  0 ,  1  ,  0  ,  0 ]->[  B ,  0  ,  1 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  0 ]->[  C ,  0  ,  0 ,  1 ];

             [ .c. ,  0 ,  1  ,  0  ,  0 ]->[  A ,  0  ,  0 ,  0 ];
             [ .c. ,  0 ,  1  ,  0  ,  0 ]->[  B ,  0  ,  1 ,  0 ];
             [ .c. ,  0 ,  0  ,  1  ,  0 ]->[  A ,  1  ,  0 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  0 ]->[  A ,  1  ,  0 ,  0 ];

             [ .c. ,  0 ,  1  ,  0  ,  0 ]->[  B ,  0  ,  1 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  1 ]->[  B ,  0  ,  1 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  1 ]->[  B ,  0  ,  1 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  0 ]->[  C ,  0  ,  0 ,  1 ];
end
```

Figure 3. The ABEL Source File for Sequencer

8-Bit Barrel Shifter

This design example highlights the use of Boolean equations as design entry format using ABEL. It is an 8-bit barrel shifter that includes a shift amount selector, an output control, and a device enable. The target device for this design is the TIBPAL20R8-XX. This design is described by only one Boolean equation. Figure 4. shows a block diagram of the design.

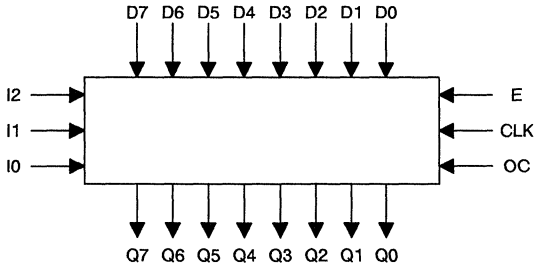


Figure 4. Block Diagram: 8-Bit Barrel Shifter

Design Specification

As shown in the block diagram above, the barrel shifter has 8 inputs (D0-D7), eight outputs (Q0-Q7), three select lines (I0-I2), a clock (CLK), an output control (OC), and an enable (E). On each clock pulse when E is high, the outputs show the inputs shifted by n bits to the right, where n is specified by the select lines. The bit shifted out of the barrel shifter on the right is shifted in on the left, actually performing a rotate. When E is low, the shifter outputs are then preset to 1.

The output control, when high, sets all outputs to high impedance, without affecting the shift. This means that if a shift is selected while the output control is high, the shift still occurs, but it is not seen at the outputs. If the OC is then set low, the shifted data will appear on the outputs.

Design Methodology

Figures 5. and 6. show a simplified block diagram and the source file listing of the design respectively. Pins have been assigned so that the shifter outputs can be associated with the registered outputs of the targeted PLD. The inputs, outputs, and select lines are then assigned to sets which simplify notation.

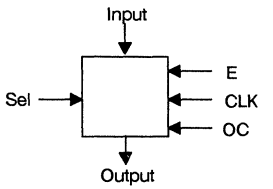


Figure 5. Simplified Block Diagram: 8-Bit Barrel Shifter

One Boolean equation is used to describe the entire function of the barrel shifter. The equation is expressed in the sum of products form and assigns a value to the output set. Each product in the equation corresponds to one of the possible shifts and defines the outputs for that shift.

Thus, the product term,

```
(Sel==0) & ![D7,D6,D5,D4,D3,D2,D1,D0]
```

defines that for a shift of 0, the inputs are transferred without a shift directly to the outputs. Similarly, the product term,

```
(Sel==5) & ![D4,D3,D2,D1,D0,D7,D6,D5]
```

defines that for a shift of 5, output Q7 gets the value of input D4, Q6 gets D3 and so on, corresponding to the correct shift of five places. Notice that the low-order input bits have been "wrapped around", shifted out of the right side and into the left side.

Sel can have only one value at a time, thus only one of the "Sel = =" relational statements can be true at a given time, and only one of the product terms contributes to the sum of products. The OR of all the product terms is ANDed with the enable E so that when E is low, all the outputs are preset to 1.

Both the output sets on the left side of the equation and the inputs on the right side of the equation are expressed as negative logic, which, in effect, gives active high logic. This is done to compensate for the 'PAL20R8's inverted outputs. The inverse of the inputs is available on the device.

```
module     barrel
title '8-bit barrel shifter
Gerrit Barrere    Data I/O Corp  Redmond WA   17 Oct 1987'

           P7095      device     'P20R8';

           D7,D6,D5,D4,D3,D2,D1,D0                    Pin 2,3,4,5,6,7,8,9;
           Q7,Q6,Q5,Q4,Q3,Q2,Q1,Q0                    Pin
15,16,17,18,19,20,21,22;
           Clk,OC,E,I2,I1,I0                Pin 1,13,23,10,11,14;

           Input                 = [D7,D6,D5,D4,D3,D2,D1,D0];
           Output                = [Q7,Q6,Q5,Q4,Q3,Q2,Q1,Q0];
           Sel                   = [I2,I1,I0];
           H,L,C,Z               = 1,0,.C.,.Z.;

equations

           !Output := E & (  (Sel == 0) & ![D7,D6,D5,D4,D3,D2,D1,D0]
                           # (Sel == 1) & ![D0,D7,D6,D5,D4,D3,D2,D1]
                           # (Sel == 2) & ![D1,D0,D7,D6,D5,D4,D3,D2]
                           # (Sel == 3) & ![D2,D1,D0,D7,D6,D5,D4,D3]
                           # (Sel == 4) & ![D3,D2,D1,D0,D7,D6,D5,D4]
                           # (Sel == 5) & ![D4,D3,D2,D1,D0,D7,D6,D5]
                           # (Sel == 6) & ![D5,D4,D3,D2,D1,D0,D7,D6]
                           # (Sel == 7) & ![D6,D5,D4,D3,D2,D1,D0,D7]) ;

test_vectors
           ([Clk,OC, E, Sel,   Input]    ->   Output)
            [ C,  L, H,  0, ^b10000000]  -> ^b10000000; " Shift 0
            [ C,  L, H,  1, ^b10000000]  -> ^b01000000; " Shift 1
            [ C,  L, H,  2, ^b10000000]  -> ^b00100000; " Shift 2
            [ C,  L, H,  3, ^b10000000]  -> ^b00010000; " Shift 3
            [ C,  L, H,  4, ^b10000000]  -> ^b00001000; " Shift 4
            [ C,  L, H,  5, ^b10000000]  -> ^b00000100; " Shift 5
            [ C,  L, H,  6, ^b10000000]  -> ^b00000010; " Shift 6
            [ C,  L, H,  7, ^b10000000]  -> ^b00000001; " Shift 7

            [ C,  L, H,  0, ^b01111111]  -> ^b01111111; " Shift 0
            [ C,  L, H,  1, ^b01111111]  -> ^b10111111; " Shift 1
            [ C,  L, H,  3, ^b01111111]  -> ^b11101111; " Shift 3
            [ C,  L, H,  7, ^b01111111]  -> ^b11111110; " Shift 7

            [ C,  L, H,  1, ^b00000001]  -> ^b10000000; " Shift 1/Wrap
            [ C,  L, H,  1, ^b11111110]  -> ^b01111111; " Shift 1/Wrap
            [ C,  L, L,  0, ^b00000000]  -> ^b11111111; " Preset
            [ C,  H, H,  0, ^b00000000]  ->      Z;     " Test High Z
end
```

Figure 6. ABEL Source File for the 8-Bit Barrel Shifter

OTHER PLD DESIGN SOFTWARE PRODUCTS

Below is a short list of some of the popular PLD design software products available to logic designers. They are all PC based and can be installed on your IBM PC™ or compatible.

CUPL™ - by Logical Devices Inc.

PLDesigner™ - by MINC Inc.

proLogic™ - by INLAB Inc.

CUPL

CUPL, like ABEL, is a universal Computer Aided Design (CAD) tool that supports PLDs. It has utility files that facilitate conversion of designs done in other design software environment to the CUPL design environment. CUPL also produces a standard programmer load file in JEDEC format, thus making it compatible with logic programmers that accept JEDEC files.

Features of CUPL design language:

- Flexible forms for design description

  Boolean Equations
  Truth Tables
  State Diagrams

- Expression substitutions or time saving Macros

  This involves the assignment of names to equations and having the software do the substitution any time the assigned name is encountered during the compile process

- Shorthand Features offered by CUPL

  List Notation; This nested directive [A4,A3,A2,A1,A0] can be represented as [A4..0]

  Bit Fields; A group of bits may be assigned to a name as in

  ```
  FIELD ADDR = [A4..0]
  ```

  Also available in CUPL are the use of

  Distributive property - where `A & (B # C)`

  is replaced with `A & B # A & C`

  DeMorgans Theorem - where `!(A & B)`
  is replaced with `!A # !B`

Some features of the CUPL language processor:

- CUPL provides design templates which allow designers to just "fill-in-the-blanks" when originating a design. Free form comments can also be used throughout the design.
- Error checking with detailed error messages directs designers to the source of problems during debugging.
- Logic Reduction Capabilities available on CUPL offers a choice of several minimization levels from just fitting a design into a target device to the absolute minimum.
- Design Simulation is accomplished using the CSIM feature.This feature allows designers to check the workability of their designs before a part is programmed. Functional simulation can be done at the programmer when test vectors are provided.

PLDesigner

The PLDesigner is a universal logic design synthesis tool for designing with PLDs. It features:

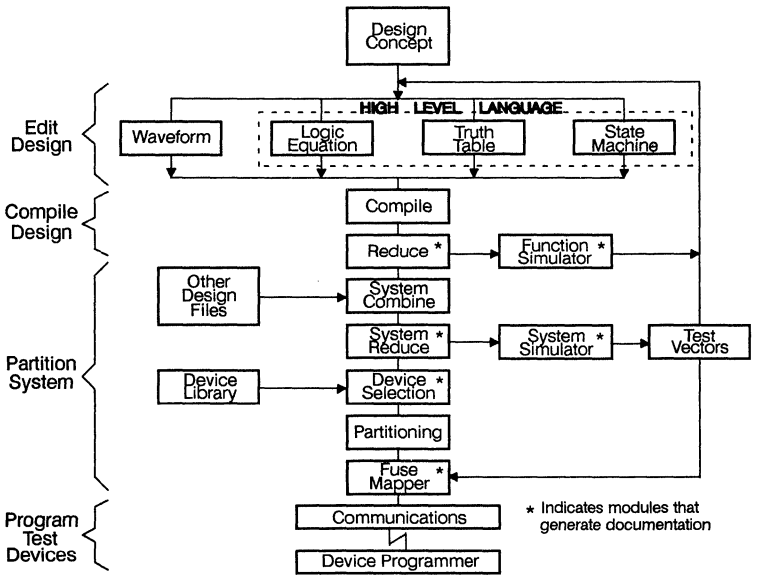
- A high-level behavioral language
- Algorithmic design entry for state machine designs
- Waveform design entry for glue logic
- Design simulation with automatic test vector generation
- Automatic device selection and design partitioning across multiple device architectures
- A device library of over 2,000 devices.

A fundamental difference between PLDesigner and other products is that the "design phase" is separate from the "device selection phase". You can complete a design before a device, or devices, are selected. This allows you to concentrate on design and simulation. No longer is it necessary to limit your design to a single device, or to select a device before starting the design.

System Requirements

PLDesigner runs on an IBM PC™ or compatible with an MS-DOS™ or PC-DOS™ operating system, version 2.0 or later. 640K RAM memory and a hard disk are recommended. A CGA, EGA, Hercules, or monochrome display may be used. A mouse and printer are optional.

Logic Design Steps with PLDesigner



proLogic

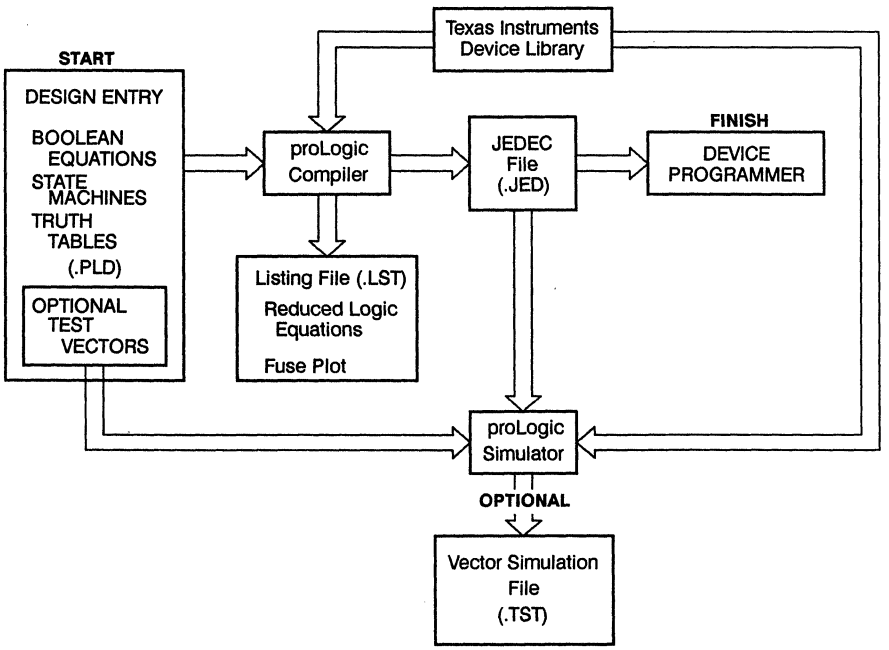
proLogic is a logic design software tool used to design and program Texas Instruments PLDs. This design software development package quickly converts your logic design to a programmer load file in the standard JEDEC format. proLogic has the flexibility to allow you to describe your logic design in any of the following formats:

- Boolean Equations
- Truth Table
- State Diagrams

It should be noted here that, not only can a design be entered in any of the above methods, you can design various sections of the design in any of the three formats shown above, and proLogic has the ability to unify the various sections and process them as one design.

The proLogic compiler is capable of performing functional simulation when test vectors are provided. The simulator uses the fuse list portion from the JEDEC file to create a functional device model. It can then execute the simulation vectors against this model. The results are automatically placed in a file for evaluation.

PLD design flow using proLogic design software:



Programming Texas Instruments Programmable Logic Devices

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Programming Texas Instruments Programmable Logic Devices

This report is intended to introduce the reader to the fuse technologies used in Texas Instruments PLDs, the measures taken by TI to provide devices with the highest possible programming yields, and the steps users can take to ensure good programmability.

HOW A FUSE IS PROGRAMMED

Programming Algorithm

Each programmable logic device family requires a unique algorithm for fuse programming and verification on commercial programming equipment. The algorithm is a combination of voltage and timing required for addressing and programming fuses in the user array.

The PLD's programming circuitry is enabled by pulsing one or more pins to a super voltage level (10.5 volts). Once the programming circuitry is enabled, inputs become addressing nodes for the input and product lines within the PLD. The actual fuse link is at the intersection of the input and product lines. Once the fuse is addressed, the fuse can be programmed by pulsing the output associated with the location of the fuse link. A fuse can be verified to be programmed by enabeling the programming circuitry, supplying the fuse address to the device's inputs, and reading the level of the device's output.

Bipolar Fuse Technology

Figure 1 shows a top and side view of a fuse in a bipolar PLD before it is programmed. Titanium-Tungsten (TiW) is used for the "fuse" or metal link programming element. The ideal thickness for this programming element is about 500 Angstroms. Titanium-Tungsten is also used as a barrier metal over contacts to prevent direct aluminum contact to silicon. To prevent aluminum diffusion during high temperature processing, the ideal thickness of the barrier metal is about 2000 Angstroms. TI's two-step link process allows both the barrier thickness and the fuse thickness to be at the ideal. The net result is a higher reliability and better programming yields.

When a device is programmed, the fuse location is selected. The fuse element at the selected location is then opened by the programmer passing a current through the Titanium-tungsten fuse element that violates the current density limit for the element. This current flow heats the fuse element to approximately 2,100 degees Celcius at which point the element is in a molten state. The metal migration which results from the heat of this out-of-limit current stress causes a gap in the fuse element.

As shown in Figure 2, the high temperature at the fuse element's gap causes two actions to occur. The fuse element's TiW material oxidizes so as to leave the metal on both sides of the gap non-conductive. Also, the heat associated with programming, causes the Silicon Dioxide (SiO_2) above the fusing element to flow into the gap. This proven fuse technology has eliminated the fears of fuse grow back as a failure mechanism in PLDs.

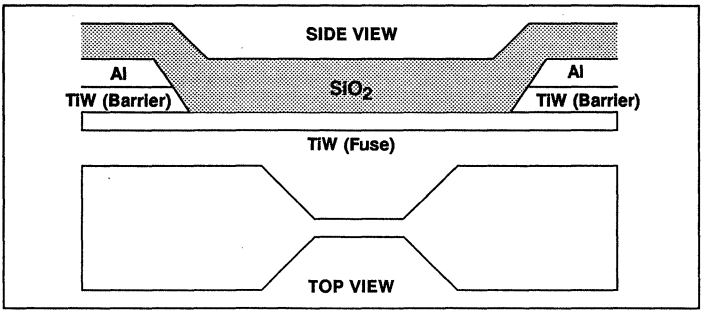

Figure 1. Before Programming

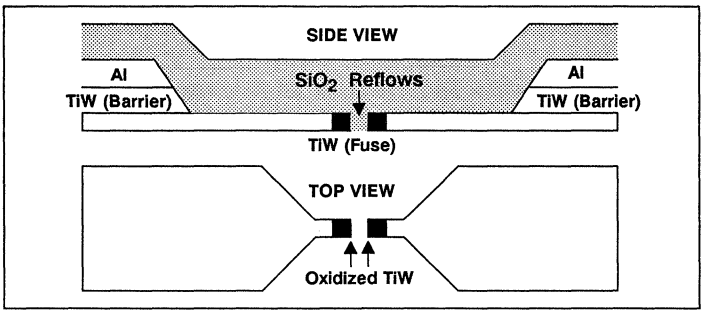

Figure 2. After Programming

EPLD Programming Technology

Texas Instruments CMOS PLDs employ a process technology similar to EPROM devices. When compared to the bipolar fusible link technology, the FAMOS (Floating-gate, Avalance-Injection MOS) transistor used by EPROMS replaces the fusible link. This permits the programmability function in the same way as the fuse.

The FAMOS transistor resembles an ordinary MOS transistor except for the addition of a floating gate buried in the insulator between the substrate and the ordinary select-gate electrode as shown in Figure 3. The programming of the FAMOS structure is performed by capacitively coupling the select gate in series with the floating gate. Hot electron injection onto the floating gate occurs by pulling the select gate to the programming voltage and the drain of the FAMOS transistor to the programming voltage minus several threshold drops. As shown in Figure 4, this serves to alter the threshold voltage of the select gate.

Once programmed, the FAMOS transistor retains the electron charge or data pattern, until exposed to an integrated dose of ultraviolet light with a wavelength of 2,537 ang-

stroms. This uv light will "erase" the charge by giving the electrons enough energy to scatter from the floating gate. This returns the threshold voltage of the select gate back to its original value or unprogrammed state. After erasure, the device is ready for reprogramming. The reprogrammablity feature of Erasable PLDs allows the devices to be used for many programming iterations which are often required in the user's design and prototyping stages.

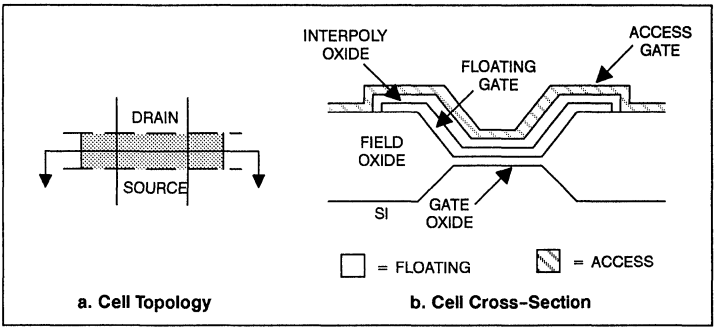

Figure 3. Views of an Floating Gate EPROM Cell

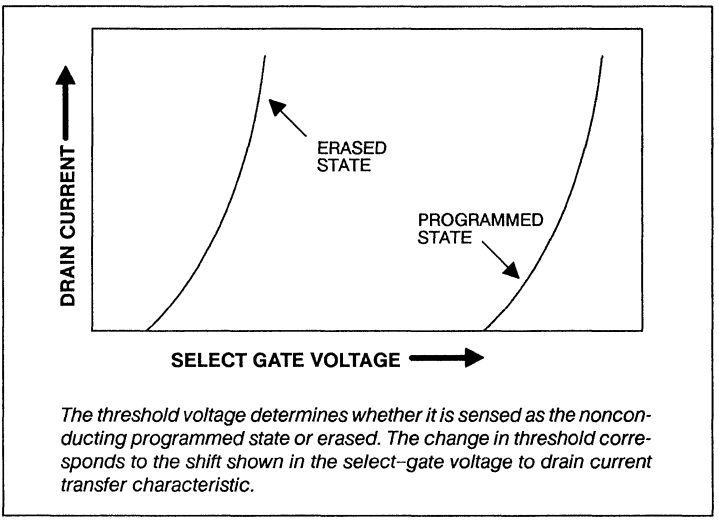

Figure 4. Drain Current vs Gate Voltage

PROGRAMMER APPROVAL

Programming Algorithm Specifications

In order to achieve satisfactory programming yields for PLDs, it is critical that device programmers adhere to the programming algorithm specifications as defined by Texas Instruments. Each specification contains detailed step-by-step programming procedures, input and product line addressing procedures, waveform diagrams, and minimum and maximum voltage and timing tables. Becuase of the complexity of the programming algorithms and the need to control and update the specifications, Texas Instruments maintains programming algorithms in a specificaiton system seperate from the PLD Data Book.

TI currently sends specifications and specification updates to most programmer and software manufacturers, and challenges each to work with TI to provide our mutual customer with approved programming support to guarantee them with the best possible programming yield.

Texas Instruments reserves the right to approve programming algorithms contained in commercial programming equipment, and recommends that customers only use approved programming support.

Approved programming support means that TI has evaluated the programming algorithm, has verified critical timing paths and voltage levels, and has performed yield analysis testing. Approvals are granted by device and are thoroughly documented.

These measures are taken to ensure that TI's customers receive the best possible programming yields when using TI PLDs.

Evaluation and Approval Methods

Programmers are evaluated by TI's programmable logic applications. The evaluation includes the following:

- Measure voltage levels for accuracy and repeatability
- Measure critical timing paths
- Evaluate system power supply and grounding
- Yield analysis

Templates and oscilliscope printouts are used to document all measurements and are maintained permanently on file. Approvals are granted by device or algorithm and documented by letter to the programmer manufacturer.

Approved Programmer Support

Approved programmer support is documented in the 'TI Programming Reference Guide', and on the TI PLD Bulletin Board (214)997-5665. To subscribe to the Programming Reference Guide, simply contact the TI PLD Hotline (214)997-5666 or your local TI field sales representative.

Texas Instruments recommends that customers use only approved programming support. Approved programming support ensures the user...

- The best possible programming yield is being achieved because the programming algorithms were evaluated and closely scrutinized.
- TI guarantees 100% programming yield if approved programmers are used, any fallout can be returned for full credit.
- TI applications engineers are available to interface with programmer manufacturers for you on any programming issues or concerns.

HELPFUL HINTS FOR GOOD PROGRAMMABILITY

1) Follow accepted standards for ESD protection – remember the additional handling requirements in customizing PLDs make them more susceptible to ESD damage.

   - Equipment, personnel and work surfaces should be grounded
   - Air ionization is recommended when handling static sensitive devices outside of protective containers.

2) Misaligned contactors and worn sockets can contribute to poor programming yield. Be aware of the manufacturers specification for number of insertions and be sure sockets are replaced frequently to ensure proper contact.

3) Ensure you are using the latest update. Most programmer manufacturers offer update and repair services to their users. The cost of the service is typically not much more than the cost of a single update and the manufacturer may update four or more times per year. TI recommends the user subscribe to this service.

   - Revisions could improve yield. TI continuously works with programmer manufacturers on yield improvement.
   - New devices may be supported.

4) Programming equipment should be calibrated. Calibration is typically included with the update and repair services previously discussed. TI recommends no less than two calibrations per year.

   - Highest possible yields
   - Avoid device damage

5) Verify the correct family pinout codes or device entry codes are being used. It is important to understand that different algorithms may be needed for different speed versions of the same function.

6) Use only TI evaluated and approved programming equipment to ensure the highest possible programming yield and quality level.

Test Considerations for PLDs

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PLD architecture establishes some unique characteristics. Because PLDs do not have the functional needs for address pins as found in a PROM, the array must be addressed for programming through the use of super voltages (10.5 volts). Since the programming and verification circuitry are not the same as the functional circuitry, verification of the array fuses does not ensure total functionality. For this reason, there are two customer yield points to be considered for a PLD, 1) programmability yield, and 2) functionality after programming. TI thoroughly tests PLDs in its factory; however, many users find the need to test after programming to achieve the highest quality levels.

The objective of this report is to provide the PLD user with an insight as to what kind of testing is performed at TI prior to shipment of programmable logic devices, and to assist you in the evaluation of your testing alternatives after programming.

DESIGNED-IN FACTORY TESTABILITY

Texas Instruments has designed testability into its bipolar PLDs through the addition of test input and test product lines. Utilizing the same circuitry as the main array fuses, a test pattern is programmed into the test array fuses which address and program at least one fuse in each input and product line. In addition to verification of the main fuse array, the test lines provide a further programmability checkpoint for each device. These same test lines enable TI to do functional, dc, and ac parametric testing on every packaged device.

Figures 1 and 2 are simplified diagrams of the test circuitry for the TIBPAL16XX series devices. Note that the test lines allow testing of actual input and output circuitry; therefore, all guaranteed specifications can be tested. AC testing through the test circuitry is closely correlated to worst case paths and should eliminate the need for ac testing at the customers incoming inspection.

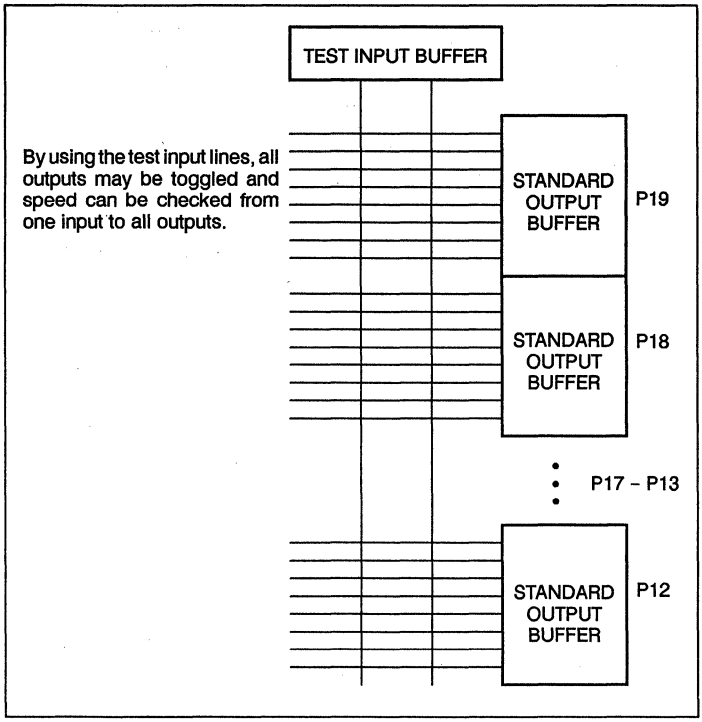

Figure 1. Additional Input Lines

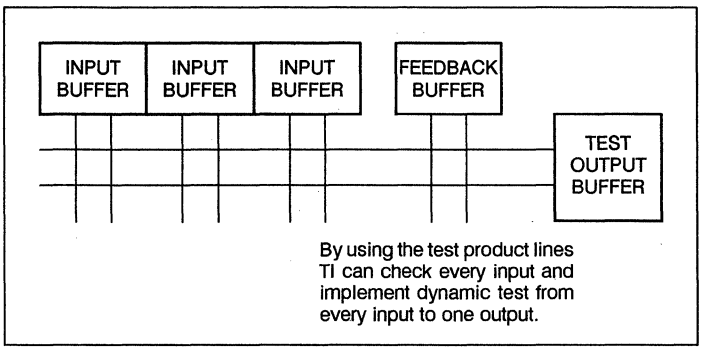

Figure 2. Additional Product Lines

USER TESTABILITY FEATURES

In addition to the designed-in testability features used in factory testing, features were also added to simplify user testability. Table 1 lists user testability features offered on TI programmable logic devices and associated software products available to assist the user with testing PLD's.

Register Pre-Load

This feature allows the user to pre-load the output registers to known states prior to applying data at inputs and/or I/O's and clocking.

Pre-load can be implemented by writing pre-load vectors in more popular logic compilers following logic equations or can be automatically generated by using automatic vector generation software. Most commercial programmers used for functional test support the use of pre-load vectors.

The real advantage of register pre-load is that it allows the user to fully test the more complex codes.

Power-Up Clear, Set or Reset

Power-up clear, set, or reset enables the user to know the state of the register at power-up. Again, this is a key feature for testability as it allows the user writing test vectors or the automatic vector generation software with a starting point for register intensive designs. Table 1 shows the power-up state of the register and resulting state at the output.

The user can also contribute to the testability of his design by utilizing other features of the PLD.

Unused Inputs / Product Lines

Unused inputs and product lines can be used to implement set, reset, clear, etc... functions to register intensive designs which are often hard to test. Often register designs have unused input pins, as well as product lines available for implementing these functions.

Enable on Combinational Outputs

Combinational outputs have one product line available for implementing the enable/disable function. The key advantage here can be seen during board testing where devices need to be isolated from each other. By disabling the output of the PLD, the user can force input conditions from the external source to the devices being driven by the PLD.

Table 1: User Testability Features

DEVICE FAMILY	SPEED DESIGNATOR	REGISTERED PRELOAD	REGISTERED OUTPUTS	POWER-UP AT REGISTER	POWER-UP AT OUTPUT	VECTOR GENERATION SOFTWARE SUPPORT: ANVIL ATG	(-- DATA I/O --) PLDTEST	PLDTEST+
TIBPAD16N8	-7	NA	0	NA	NA	-	1.3	1.0
TIBPAD18N8	-6	NA	0	NA	NA	-	-	-
TIBPAL16L8	-7/-10	NA	0	NA	NA	2.23	1.0	1.0
TIBPAL16R4	-7/-10	YES	4	L	H	2.23	1.0	1.0
TIBPAL16R6	-7/-10	YES	6	L	H	2.23	1.0	1.0
TIBPAL16R8	-7/-10	YES	8	L	H	2.23	1.0	1.0
TIBPAL16L8	-12/-15/-25	NA	0	NA	NA	2.23	1.0	1.0
TIBPAL16R4	-12/-15/-25	-	4	H	L	2.23	1.0	1.0
TIBPAL16R6	-12/-15/-25	-	6	H	L	2.23	1.0	1.0
TIBPAL16R8	-12/-15/-25	-	8	H	L	2.23	1.0	1.0
TIBPAL20L8	-7/-10	NA	0	NA	NA	2.23	1.0	1.0
TIBPAL20R4	-7/-10	YES	4	L	H	2.23	1.0	1.0
TIBPAL20R6	-7/-10	YES	6	L	H	2.23	1.0	1.0
TIBPAL20R8	-7/-10	YES	8	L	H	2.23	1.0	1.0
TIBPAL20L8	-15/-25	NA	0	NA	NA	2.23	1.0	1.0
TIBPAL20R4	-15/-25	YES	4	L	H	2.23	1.0	1.0
TIBPAL20R6	-15/-25	YES	6	L	H	2.23	1.0	1.0
TIBPAL20R8	-15/-25	YES	8	L	H	2.23	1.0	1.0
TIBPAL22V10	-/A	YES	10*	L	H/L	2.23	1.0	1.0
TIBPAL22V10	-15	YES	10*	L	H/L	2.23	1.0	1.0
TIBPAL22VP10	-20	YES	10*	L	H/L	2.23	-	-
TICPAL16L8	-35,-55	NA	0	NA	NA	2.23	1.0	1.0
TICPAL16R4	-35,-55	YES	4	NA	NA	2.23	1.0	1.0
TICPAL16R6	-35,-55	YES	6	NA	NA	2.23	1.0	1.0
TICPAL16R8	-35,-55	YES	8	NA	NA	2.23	1.0	1.0
TICPAL22V10Z	-25	YES	10*	-	-	2.23	1.0	1.0
TIEPAL10H16P8	-3,-6	NA	0	NA	NA	2.23	-	-
TIEPAL10016P8	-3,-6	NA	0	NA	NA	2.23	-	-
TIB82S105	B	-	8	H	H	2.23	-	-
TIB82S167	B	-	6	H	H	2.23	-	-
TIBPSG507	-	-	8*	L	H	2.23	-	-
TIBPLS506	-	-	8*	L	H	2.23	-	-
EP610	-25,-30,-35	-	16*	NA	NA	2.23	-	-
EP910	-30,-35,-40	-	24*	NA	NA	2.23	-	-
EP1810	-35,-45	-	48*	NA	NA	-	-	-

* = USER CONFIGURABLE
NA = NOT APPLICABLE
NOTE: ALL CMOS PLDS ARE ERASABLE FOR REPEATED PROGRAMMABILITY.

PLD TESTING OPTIONS

Fuse Verification / Checksum

Checksum testing verifies array fuses to be intact or blown. Each fuse location is assigned a value of 1, 2, 4, 8, 16, 32, 64, or 128. The checksum is the sum (in hexadecimal) of the values of positions with blown fuses. As previously discussed, checksum testing or fuse verification only tests for the state of the fuse and exercises programming circuitry only. Functional circuitry is not tested.

Structured Vector Testing

Structured vector testing, utilizing the software packages shown in Table 1 or generated manually at design conception, allow the user to apply structured test vectors (see Figure 3) to the device either on device programmers or testers. Figure 4 shows how to implement pre-load into your vector test.

Fault coverage of structured vectors is graded and documented so the user knows how much coverage he has for his design. A fault is simply a potential for device failures. Faults graded include logic faults as well as fuse faults.

Logic Faults - Check affected gates for S-A-0, or stuck low, and S-A-1, or stuck high. Figure 5 Illustrates logic faults. Fuse Faults - Check each fuse for intact or blown

Structured vectors are generic so they can be applied to all manufacturers PLDs of like function (e.g. 16L8, 22V10, etc...). Structured vector testing ensures the functionality of the design, and can be performed right on the device programmer. Structured vector testing should be considered the minimum amount of testing required prior to application.

Signature Analysis / Logic Fingerprint™ / Random Vector Test

Signature analysis or fingerprint testing is sometimes seen as an alternative to structured vector testing. The test applies a pre-determined or psuedo-random vector set to the inputs of a "known good" device and memorizes the output responses. Subsequent devices are tested against the master. Potential problems exist with this type of testing.

- Master device could be defective resulting in the acceptance of bad devices and/or rejection of good devices.
- Registered devices may never initialize
- Outputs may never be put in the correct states to ensure correct feedback (only structured vectors ensure correct feedback)
- Oscillating conditions not controlled (structured vectors can void oscillations)
- Different manufacturers use different power-up / pre-load conditions
- Percent of coverage is unknown

The best case could yield an adequate functional test while the worst case may test little or nothing. The problem is there is no way to determine which case you have as grading is not available.

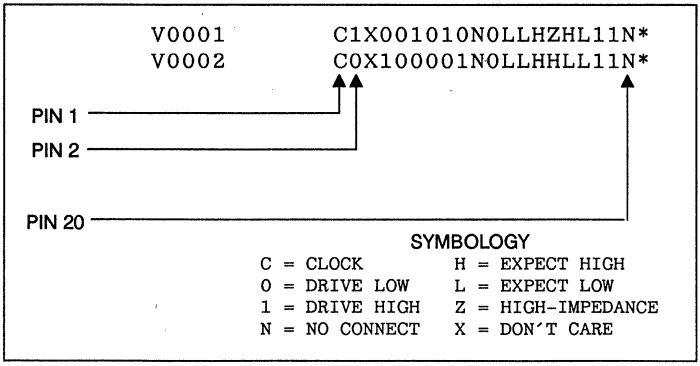

Figure 3. Test Vectors (Standard JEDEC Form)

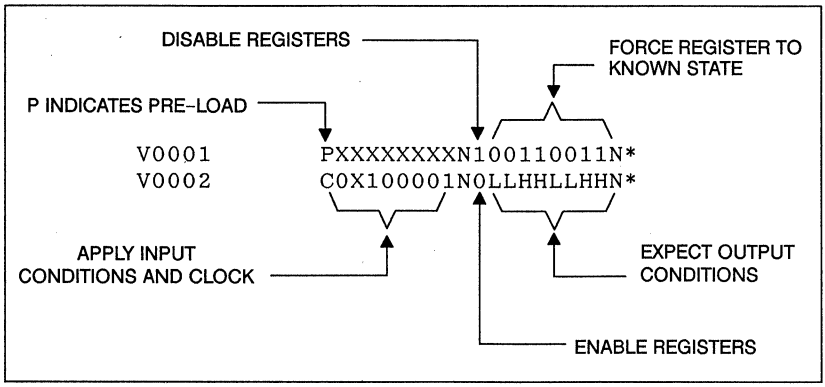

Figure 4. Pre-Load Implementation – '16R8

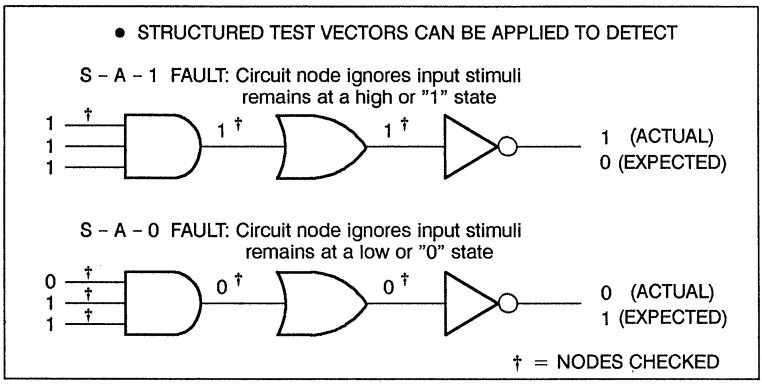

Figure 5. Fault Grading

DC Parametric Testing

DC parametric testing includes structured vector or functional testing as described previously plus the testing of critical current/voltage parameters to ensure they meet the specifications prescribed by the TI data book.

The testing of dc parametrics, such as input and I/O leakage currents, output high and low voltages under dc loading, power supply current, etc... will only improve the quality of the PLD going into the application by ensuring that devices which are functional were not damaged due to ESD (electrostatic discharge) or EOS (electrical overstress) during the customization process.

DC parametric testing can not presently be performed on device programmers and therefore requires the use of automatic test equipment (ATE). dc parametric testing coupled with structured vector testing should provide the user an "optimum" test with a "medium" investment.

AC Testing

AC testing ensures that the PLD meets all the speed requirements of the design. A good ac test measures propagation delay time through all possible paths and, when coupled with functional and dc parametric testing, provides the ultimate PLD test.

There are two types of ac testing to be considered: functional ac and measurement ac testing. Functional ac testing becomes a popular test method for PLDs. This method applies structured test vectors and sets strobes to ensure transistions occur with proper timing. Functional ac does a good job of simulating the actual design if structured vectors with good coverage are used.

In contrast, measurement ac testing tests and measures all speed parameters utilizing all possible input and output combinations. This type of testing is typically only available from the factory as it requires another level of vector grading and dedicated engineering resources.

AC testing usually requires a large investment by the user in not only hardware, but also in engineering time in the development of extensive test programs, bench to tester correlation, load boards, vector software, etc...

Texas Instruments performs extensive worst case code characterization prior to device release. Each device shipped from TI undergoes ac testing using the device's test rows and test columns. Many users find post programming ac test does not justify the payback in terms of a higher level of quality.

WHY TEST AFTER PROGRAMMING?

As previously discussed, verification of the fuse array following programming does not ensure total functionality; therefore, the user must determine what amount of testing is required after programming. The following concerns should be considered.

Programming

Programming exposes the device to super voltages (up to 10.75 volts) and currents high enough to overstress devices. TI PLDs are designed to withstand these conditions; however, all leakage current parameters should be tested to eliminate the risk of electrical overstress.

An uncalibrated programmer can expose devices to voltages/currents outside specified ranges.

Handling

In addition to programming, most users designate their custom function which was programmed into the PLD through labeling or marking. The added handling required to program and customize the PLD increases the chances for ESD (electro-static discharge) damage unless strict adherence to ESD protection procedures is observed.

Custom Function

TI goes to extreme measures to ensure device functionality and performance; however, each user design is a custom function and should be treated as such during final testing prior to application.

Test vs Rework

Figure 6 compares the impact of testing on board rework and, consequently, manufacturing cost. This illustration compares no testing vs. functional and dc parametric testing. Using conservative figures for rework cost, the data shows rework cost due to untested PLDs can exceed one dollar per PLD used. A similar analysis of the reader's application may show a cost savings which would result from testing after programming.

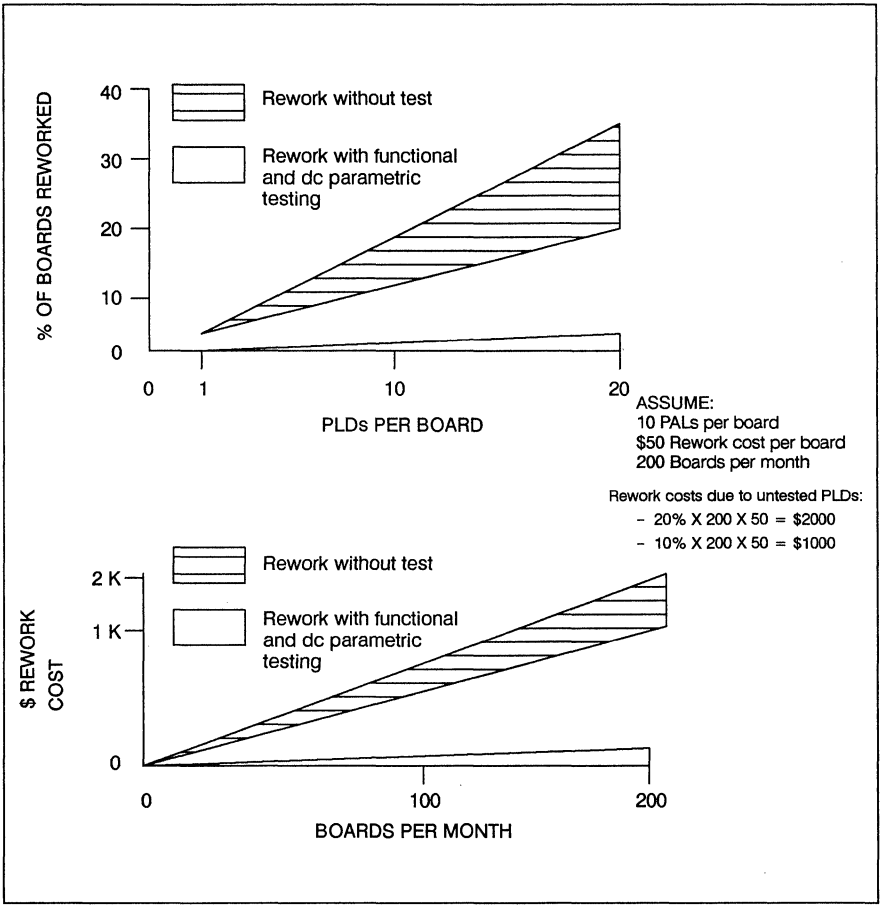

Figure 6. Test vs Rework

TI PROGRAMMING AND TEST SERVICES

What services are offered by your PLD manufacturer? Texas Instruments provides its customers with a three phase service program which provides for programmed and tested PLDs of the highest quality (see Figure 7) direct from the factory or through TI's authorized distributors.

Factory Programmed and Tested PLDs

TI has the capability to support run rates greater than 1000 parts per code per month with factory programmed and tested PLDs. TI generates structured test vectors and performs 100% functional, dc parametric, and ac testing on PLDs programmed to your custom logic function. Custom symbolization is also included in the factory programmed PLD flow, thereby delivering ship-to-stock and/or ship-to-WIP product.

Impact Design and Services Centers

Texas Instruments took the leadership role in the provision of program and test services to its customers by implementing the Impact Center approach in 1986. The Impact Centers offer the customer a local "quick turn" production resource with factory quality programming, marking, and testing on TI owned and maintained equipment. Strict adherence to TI's ESD protection guidelines is maintained. Production specifications remain under TI control and operations are continuously audited by TI.

Endorsed Program and Test Centers

An extension of the Impact Center philosophy, an endorsed center is a distributor funded program and test facility which meets or exceeds TI specifictions. Each center has the capability to program, mark, and test PLDs. Production flows are approved to guarantee the user receives devices of ship-to-stock quality. The centers are audited bi-annually to ensure compliance.

Tables 2 lists the TI Impact Centers. An updated listing for Endorsed Centers may be obtained through the TI PLD Bulletin Board (214) 997-5665, the TI PLD Hotline (214) 997-5666 or your local TI Sales Representative.

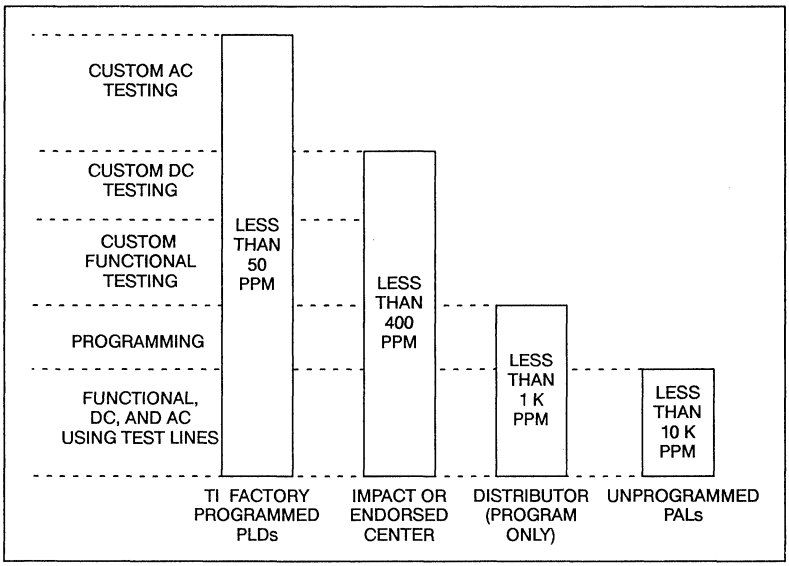

Figure 7. TI Programmable Logic Services

Table 2. TI Impact Design and Services Centers

NORTHERN CALIFORNIA	**BOSTON**
MARSHALL IMPACT CENTER	HALL-MARK IMPACT CENTER
336 LOS COCHES STREET	6 COOK STREET
MILPITAS, CA 95035	PINEHURST PARK
(408) 942-4600	BILLERICA, MA 01821
	(617)935-9777

A Designer's Guide to the TIBPSG507

Robert K. Breuninger and Loren E. Schiele
with Contributions by
Joshua K. Peprah

TEXAS INSTRUMENTS

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INTRODUCTION

The term PSG stands for Programmable Sequence Generator. The PSG is the newest member of the programmable logic family. It combines the powerful benefits of programmable array logic (PALs) with the specialized world of Field Programmable Logic Sequencers (FPLSs).

Applications such as waveform generators, state machines, timers, and simple logic reduction are all possible with a PSG. By utilizing the built-in binary counter, the PSG is capable of generating complex timing controllers. In short, the PSG offers the system designer an extremely powerful building block.

The purpose of this application report is to describe the functional operation of the PSG507 and demonstrate how it can be applied in real-world applications. Three design examples that highlight the features and flexibility of the PSG will be discussed.

FUNCTIONAL DESCRIPTION

Figure 1 shows the architecture of the PSG507. Major features include 13 inputs, eight programmable registered or nonregistered outputs, eight S/R state registers, and a 6-bit binary counter with control logic. The clock input is fuse-programmable for selection of positive or negative edge triggering.

The binary counter, state registers, and output cells are synchronously clocked by the fuse-programmable clock input. The clock polarity fuse selects either positive or negative edge triggering. Negative edge triggering is selected by blowing the clock polarity fuse. Leaving this fuse intact selects positive edge triggering.

Each output cell on the PSG can be configured for registered or nonregistered operation through the output multiplexer fuse. Nonregistered operation is selected by blowing the output multiplexer fuse. Leaving this fuse intact selects registered operation.

The PSG507 has 13 inputs, each providing a true and complement input to the AND array. Pin 17 functions as either an input and/or an output enable. Blowing the output enable fuse lets pin 17 function as an output enable but does not disconnect pin 17 from the input array. When the output enable fuse is intact, pin 17 functions only as an input with the outputs being permanently enabled.

The 6-bit binary counter is controlled by a synchronous clear and a count/hold function. Each control function has a nonregistered and registered option. When either SCLR0 or SCLR1 is taken active high, the counter resets to zero on the next active clock edge. When either $\overline{\text{CNT}}$/HLD0 or $\overline{\text{CNT}}$/HLD1 is taken active high, the counter is held at the present count and is not allowed to advance on each active clock edge. The SCLR feature overrides the $\overline{\text{CNT}}$/HLD feature when both functions are simultaneously active high. The functional benefit of both these features will be further clarified in the examples shown later in this appliction report.

The eight internal state registers feed back into the AND array. These registers can be used to store input data, to keep track of binary count sequences, or they can be used as output registers when connected to a nonregistered output cell. The state registers differ from the output registers in that they feed back into the input array. They can also be used to override an operating sequence such as demonstrated in the designer notes located at the end of this application report. By using extra state registers, the 6-bit counter can be expanded as shown in the second example. Other uses of the internal state registers will become apparent upon reading the examples shown.

THEORY OF OPERATION

The PSG architecture is capable of operating in many different modes. When comparing the operation of a PSG to a PAL, the outputs in both devices can be configured as an AND/OR function of the inputs. One major difference between a PSG and a PAL is that a programmable OR array is used in the PSG. This allows a selected number of AND terms to be connected to each output as compared to a fixed number of AND terms assigned to each output on a PAL. The programmable OR array is the more efficient in that it lets the user assign the exact number of AND terms to each output as required by the application.

Another major difference between the PAL architecture and that of a PSG is that the output cells on a PSG are not fed back into the input array. Typically, output feedback is used for building a counter or for holding state information. Since the architecture of the PSG already includes state registers and a binary counter, the requirement for output feedback is eliminated in most applications. This is a benefit to the user because valuable output cells and AND terms are not wasted when generating these functions.

When a Field Programmable Logic Sequencer is compared to a PSG, the most obvious difference is the addition of a binary counter. Most state machine designs can be simplified by referencing all or part of each sequence to a binary count. This technique is highlighted in the third example shown in this application note. A comparison will also reveal that the output cells on a PSG can be configured

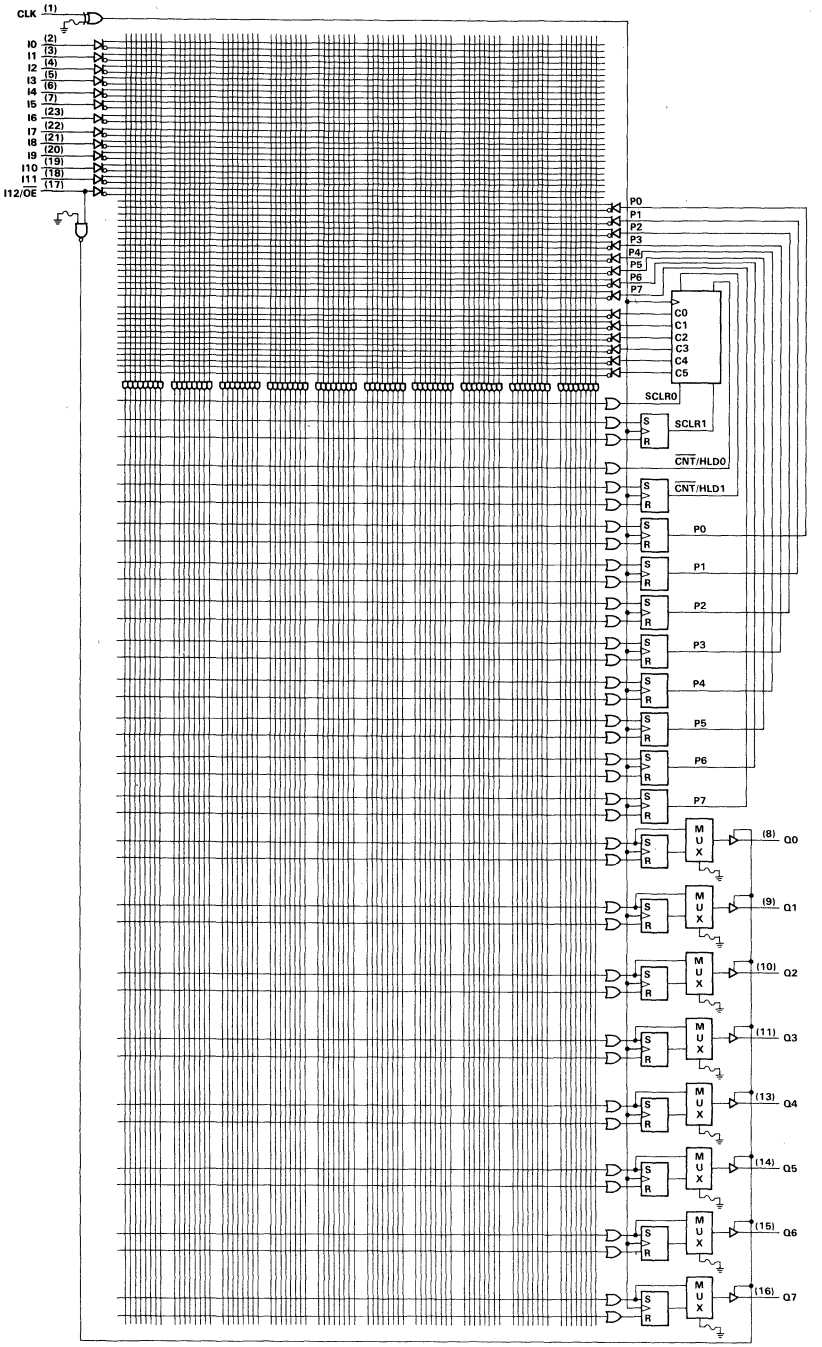


Figure 1. PSG507 Architecture

for nonregistered operation. This permits the outputs to be directly fed from the counter, AND/OR array, or state registers. Example 1 highlights this feature.

In short, the outputs of a PSG can be controlled by any or all of the following conditions:

- Present state of the inputs
- Present state of the binary counter
- Present state of the state holding registers

The key to understanding state machine design when using a PSG is to realize that different states can be assigned for each sequence. In other words, the assigned state determines which sequence is in operation. The length of each sequence is controlled by the SCLR function. Once the count sequence has been programmed to the desired length, each output can be easily decoded from the present state of the binary counter. The user will soon discover that complex state machines are easily developed when using this technique. This technique is demonstrated in Example 3.

Example 1: Waveform Generator

The first example demonstrates a design for a simple clock generator used for driving a microprocessor operating at 5 MHz (required duty cycle of 33.5% high, 66.5% low). In addition to the 5 MHz system clock (SYS CLK), a reference clock (REF CLK) operating at 15 MHz (50% duty cycle) and a peripheral clock (PCLK) operating at 2.5 MHz (50% duty cycle) are required for other timing controllers and peripherals throughout the system. Both clocks must be in close phase with the SYS CLK to guarantee synchronous operation within the system.

The above example demonstrates one of the many uses of the binary counter in the PSG. State registers are not used in this particular application, only the binary counter and three outputs. A 30 MHz clock, typically generated from a crystal, is used for driving the binary counter of the PSG. The three generated clock signals are decoded from the binary count. The unused inputs and outputs are still available for other sequential or combinational applications.

Figure 2 shows the timing diagram for the above application. For reference, a decimal count has been assigned to the master clock (PSG CLK) of the PSG. As shown in the timing diagram, at count 11 (1011_2) the sequence is repeated. By using the SCLR0 function, a logic equation can be defined to reset the counter at count 11. This concept is demonstrated in Figure 3.

With the binary counter programmed to clear at 11, it is a simple matter to decode the outputs from the binary count. With the REF CLK equal to the inverse of binary count zero (C0), REF CLK can be directly generated from the binary counter. A product term is required to connect C0 to the output cell. The output register is bypassed by blowing the output multiplexer fuse. Figure 4 shows how C0 can be connected.

SYS CLK and PCLK are decoded from the present state of the binary counter through the S/R outputs. Since the S/R register holds its present state until changed, product terms have to be used only during output transitions. For example, when the binary counter reaches one, a product term is used to reset the SYS CLK on the next clock transition. Below is a summary of the product terms required to control SYS CLK and PCLK. Note that the output transitions are set up in the previous clock cycle. Also note that only one product term is used regardless of how many output terms switch. This is demonstrated at count 5 and count 11. Figure 4 also shows how SYS CLK and PCLK are connected.

CNT 1:	Reset SYS CLK
CNT 5:	Set SYS CLK, reset PCLK
CNT 7:	Reset SYS CLK
CNT 11:	Set SYS CLK, set PCLK

This simple application demonstrates the basic concept of building a waveform generator using the PSG. This concept will be expanded further in Example 3 when a memory timing controller is developed. The basic rules for building a waveform generator are summarized below.

- Program the counter to reset to zero after the desired count length is reached.
- Generate the logic equations to control the outputs from the present state of the binary counter.

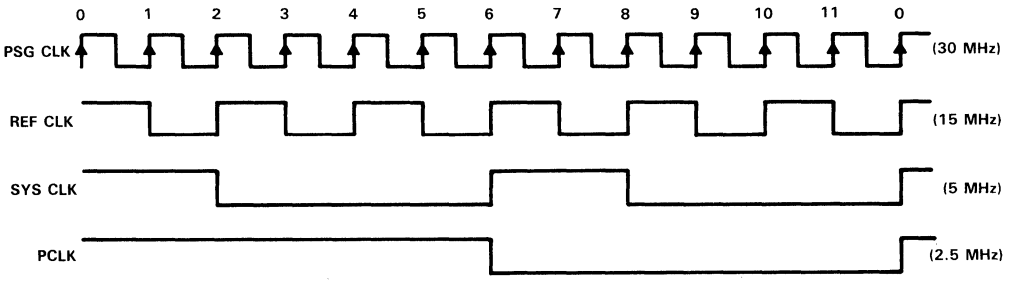


Figure 2. Clock Generator Timing Requirements (Example 1 — Waveform Generator)

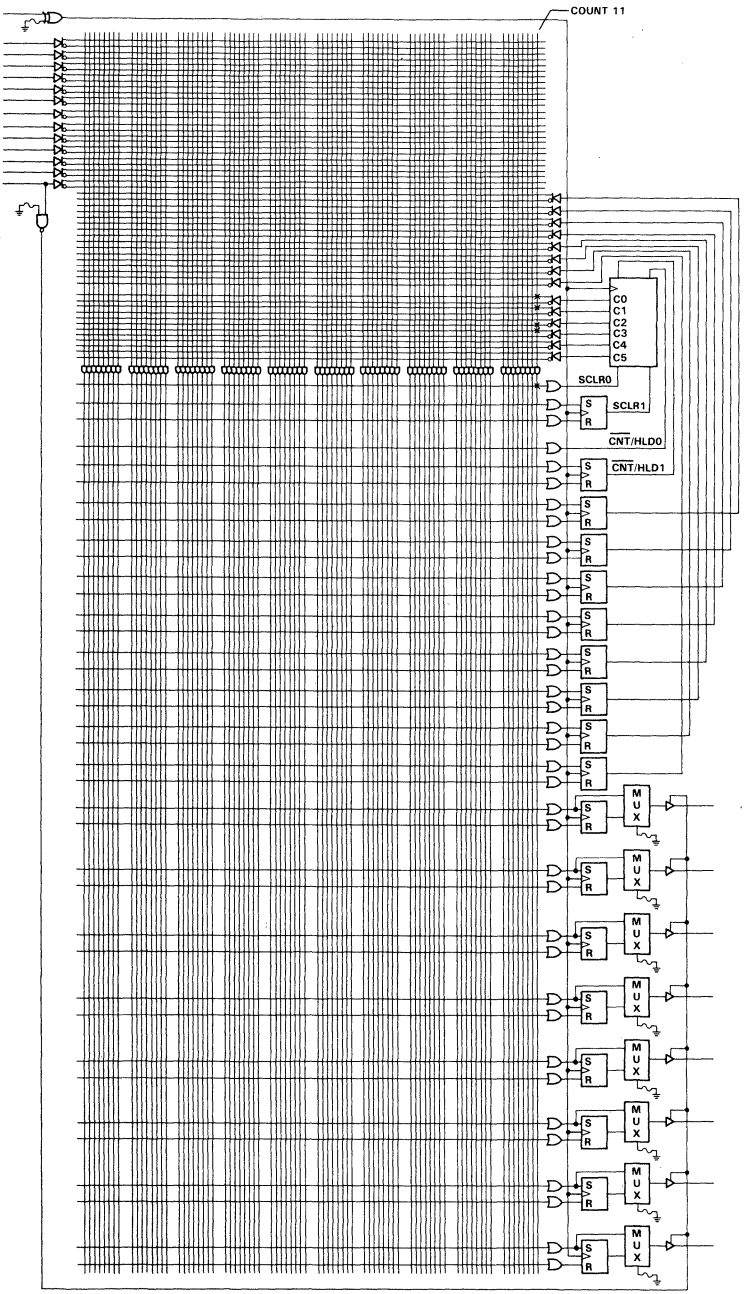


Figure 3. SCLR at COUNT 11
(Example 1 — Waveform Generator)

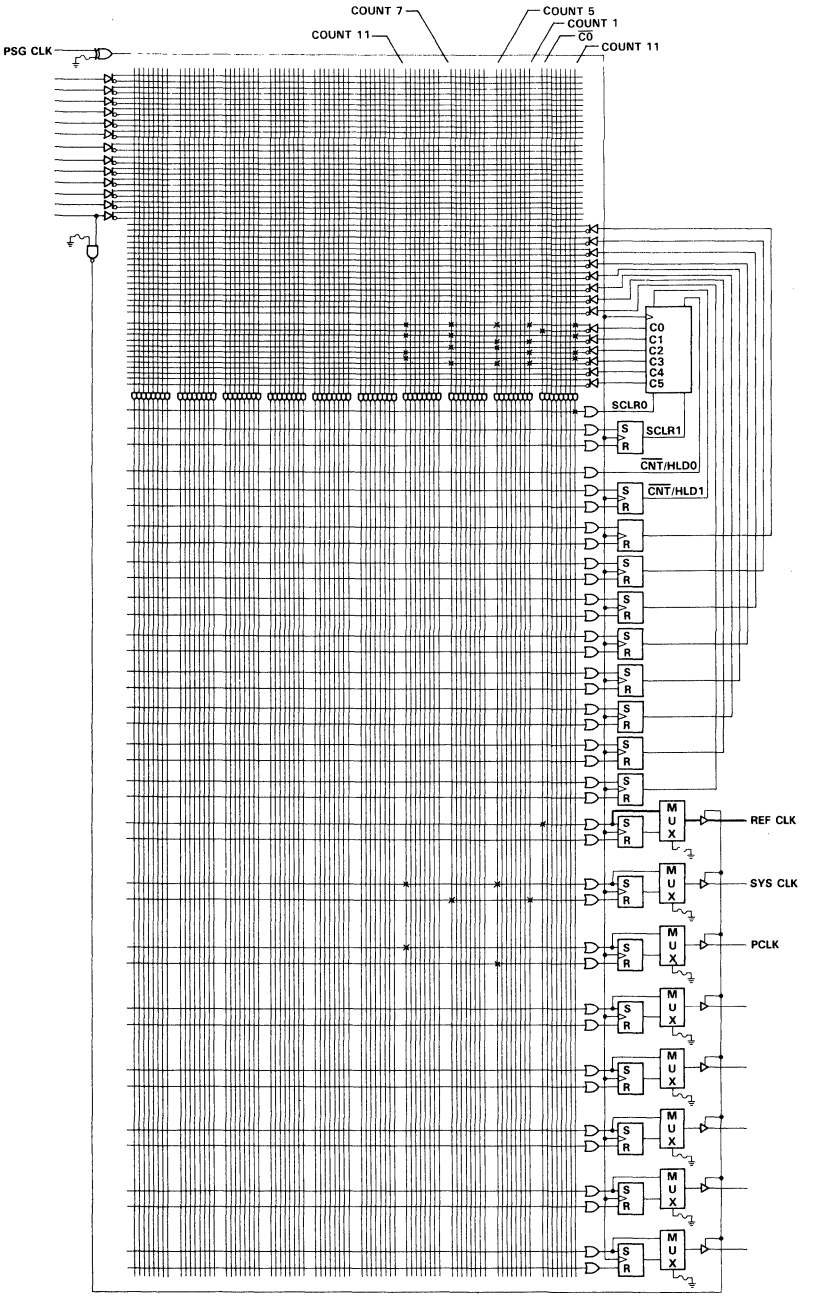


Figure 4. Waveform Generator (Example 1)

Example 2: Refresh Timer

The second example demonstrates a design for a refresh timer used for signaling to a memory controller that it should execute a refresh cycle. As required by the dynamic memory, every row (256 on TMS4256) must be addressed once every 4 ms. One method used to guarantee that this requirement is met is to refresh one row at least once every 15.6 μs. With a 5 MHz system clock, the timer should be set for a division rate of approximately 77 clock cycles. This condition will generate a refresh request every 15.4 μs.

The memory controller executes the refresh request ($\overline{\text{REFREQ}}$) immediately if it is not involved in an access cycle. If the memory controller is executing an access cycle, then the refresh request will not be honored until the access cycle is completed. A refresh complete input (RFC) is required on the refresh timer to acknowledge when the refresh cycle has been completed by the memory controller. It is important that the timer does not stop, even though a refresh complete signal has not been received. This guarantees the refresh requirement is not violated. This also assumes the memory controller will complete the refresh request sometime in the next 77 clock cycles.

Figure 5 shows the timing diagram for the above application. A decimal count has been assigned to the PSG's master clock (PSG CLK) for reference. The counter is held at zero until the reset input is taken inactive low. Once the counter reaches 76 (equal to 77 clock cycles) the $\overline{\text{REFREQ}}$ output is driven active (low). The $\overline{\text{REFREQ}}$ output returns inactive high on the first positive clock edge after RFC goes active high. RFC is the signal from the memory controller that tells the refresh timer when the refresh operation has been completed. The $\overline{\text{REFREQ}}$ output remains low until the RFC signal has been received.

In order to generate a refresh request every 77 clock cycles, a 7-bit counter is required. Since the internal counter of the PSG is 6 bits, one of the state holding registers is required to expand the counter to 7 bits. As shown in Figure 6, only two product terms are required to expand to 7 bits; one product term to set the register when the 6-bit counter reaches its full count (63), and one product term to reset the register after count 76. Since both the binary counter and the added register need to be reset after count 76, a single product line can be used for both. (For additional details on expanding the 6-bit counter of the PSG, see the designer notes at the end of this application report.)

Figure 7 shows the fuse map for the entire refresh timer. The refresh timer is initialized by taking the RESET input high. When RESET is taken high, a single product line is activated and all other product lines are disabled. On the next active clock edge, the binary counter and C6 are cleared and the $\overline{\text{REFREQ}}$ output is set high. The refresh timer will begin counting when RESET returns low. When the 7-bit counter reaches 76, a product line goes active (high) and on the next clock edge forces C6 and the 6-bit counter to zero. Note that the output register holding $\overline{\text{REFREQ}}$ is also reset to zero. The RFC input is connected to a product line which in turn is connected to the set input of the $\overline{\text{REFREQ}}$ output register. On the next active clock edge after RFC is taken high the $\overline{\text{REFREQ}}$ output will return high.

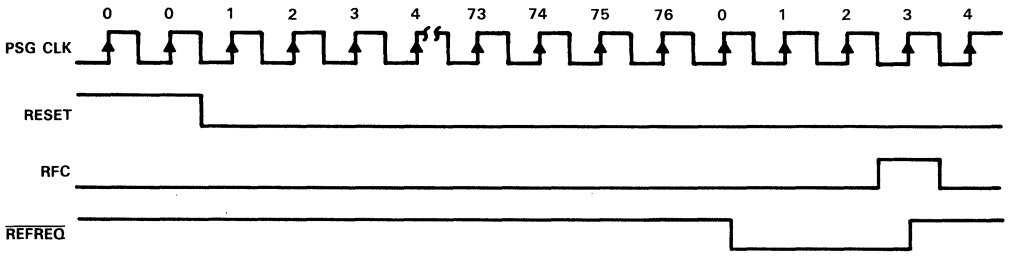


Figure 5. Refresh Timer Requirements (Example 2 — Refresh Timer)

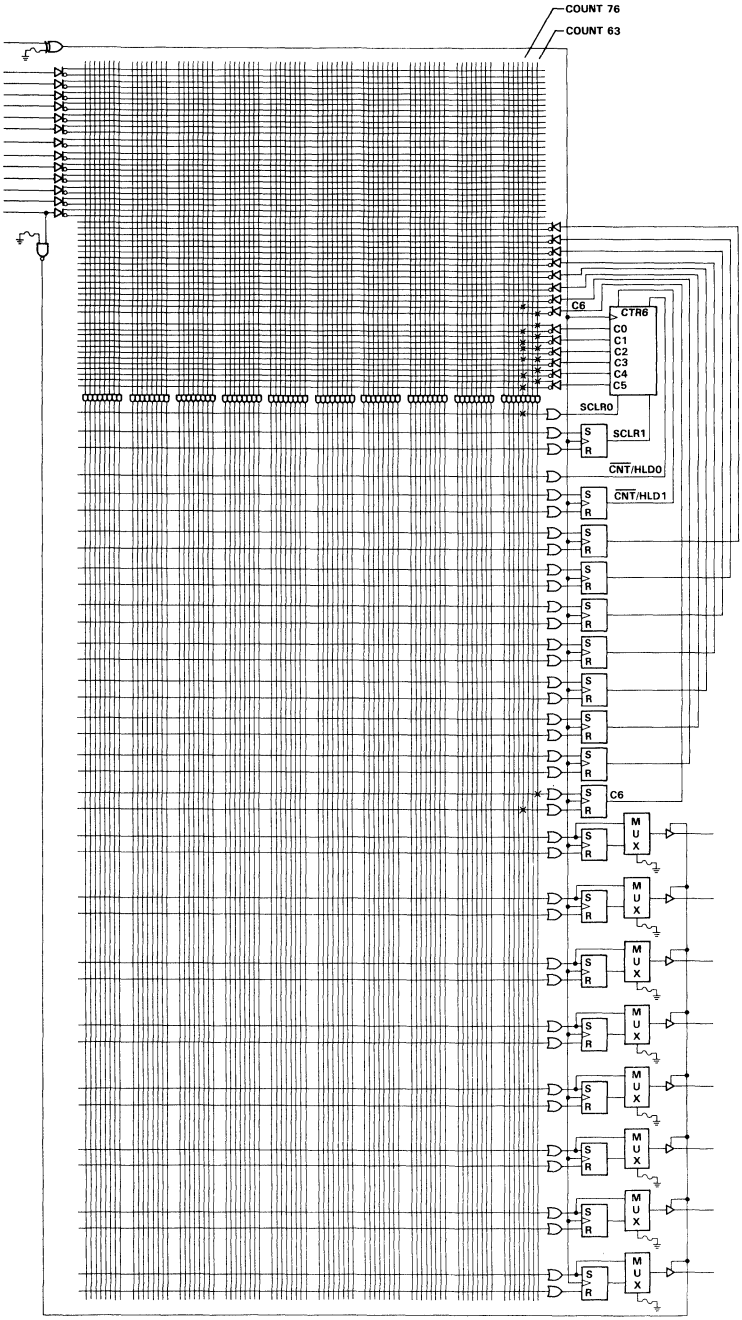


Figure 6. Expanding to 7-Bit Binary Counter (Example 2 — Refresh Timer)

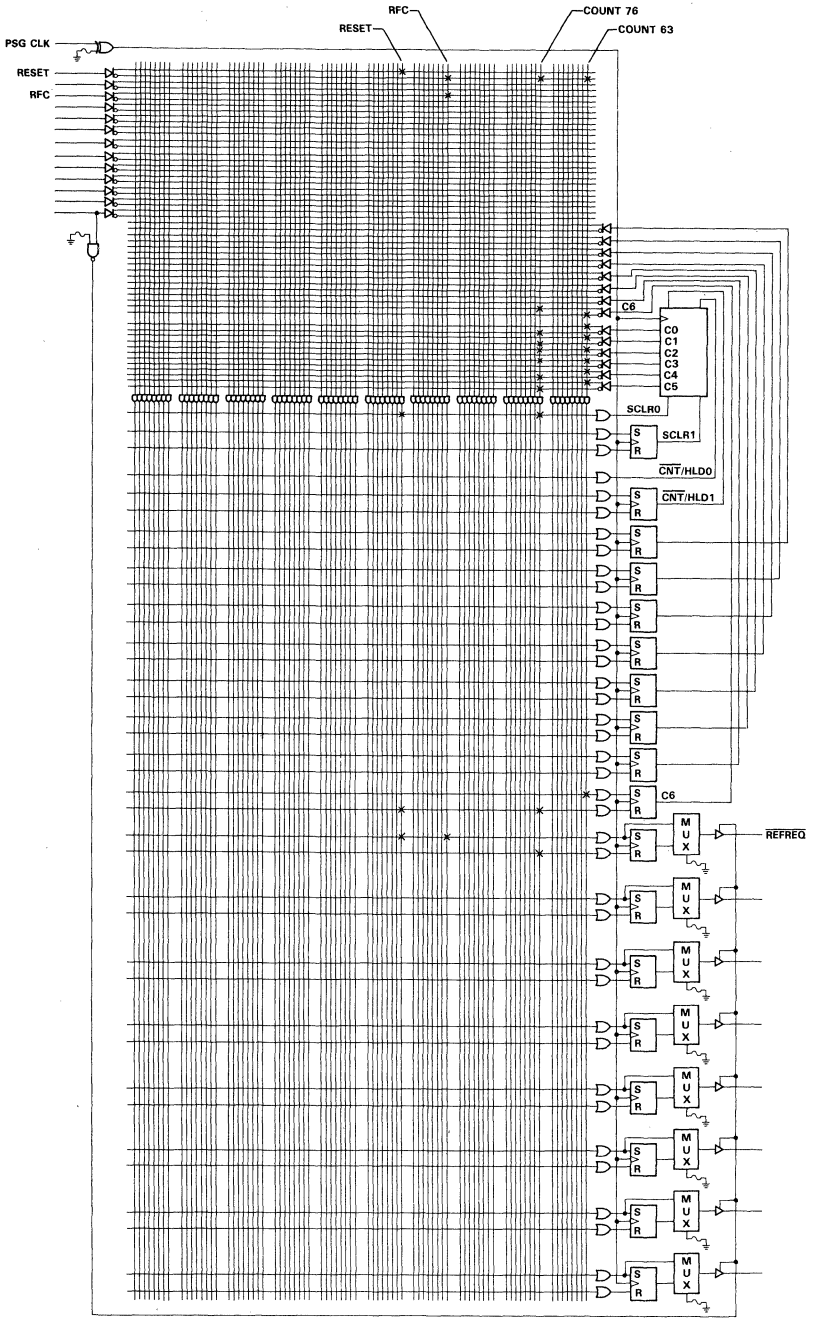


Figure 7. Refresh Timer
(Example 2)

Example 3: Dynamic Memory Timing Controller

The third and last example will demonstrate a state machine design using the PSG507. Figure 8 shows the circuit requirement for a memory timing controller used for interfacing an Intel 8086 to an 'ALS2967 dynamic memory controller. Note that the clock generator and refresh timer, developed in Examples 1 and 2, can be used in this circuit.

The dynamic memory timing controller generates the control signals ($\overline{RAS}$, $\overline{CAS}$, MSEL, etc.) needed for accessing and refreshing the dynamic memory. The memory timing controller must also be capable of arbitrating between refresh and access cycles. In other words, if a refresh request ($\overline{REFREQ}$) occurs while the timing controller is performing an access cycle, the controller must finish the access cycle before granting the refresh request. Likewise, if an access cycle is requested during a refresh cycle, the controller must hold the processor while completing the refresh cycle. After the refresh cycle has been completed, the access cycle can be performed.

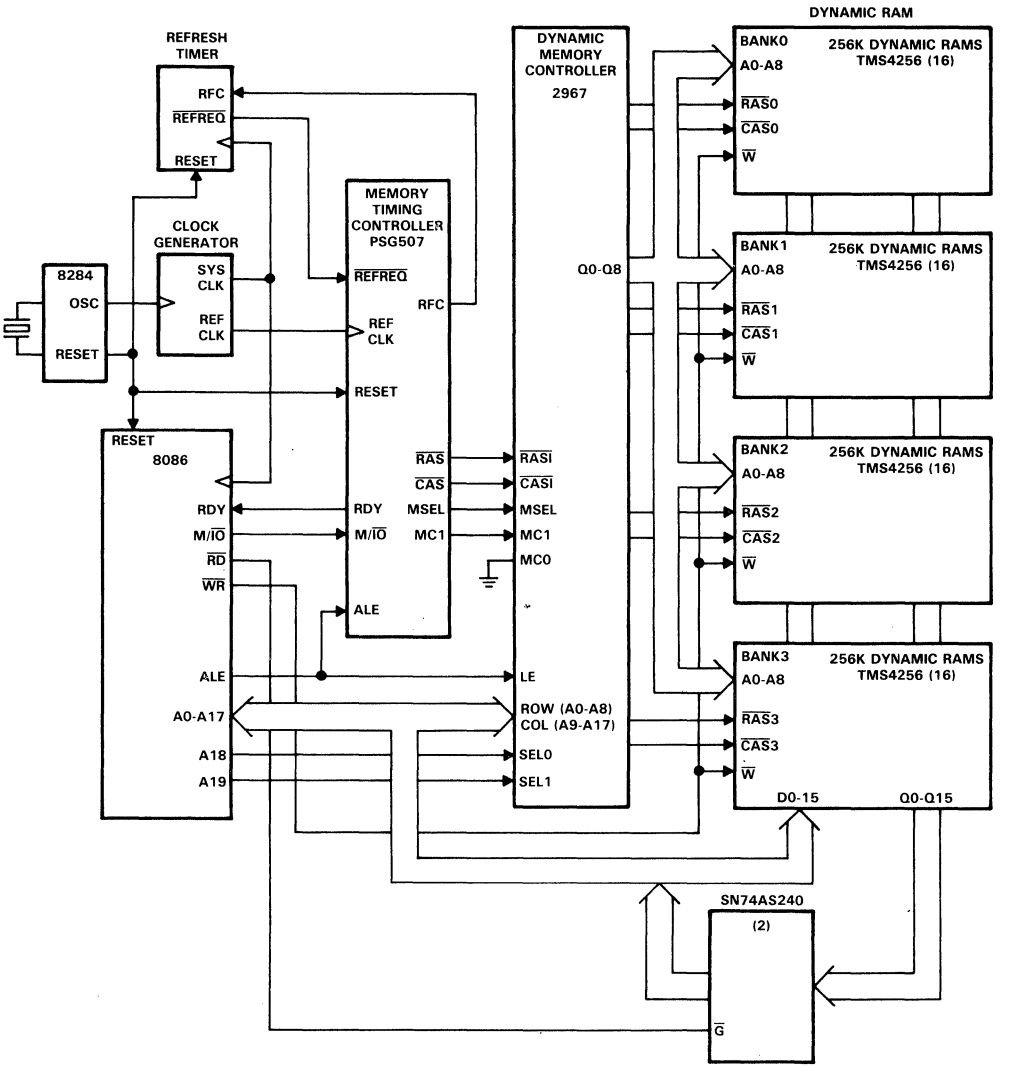


Figure 8. Memory Timing Controller (Example 3)

Figure 9 shows a detailed flow chart for the intended application. Note that two sequences are executed and three states are used. State 0 (ST0) provides an initalization and holding state, while state 1 (ST1) is assigned to the access sequence. The access sequence consists of 10 clock cycles as shown in Figure 10. State 2 (ST2) is assigned to the refresh/access grant sequence (Figure 11). This particular sequence takes 20 clock cycles, with a logical decision being made between count 9 and count 10. If at count 9 RDY is low, the counter will continue on and execute the access grant sequence. If RDY is high, the controller will clear the counter and return to state 0.

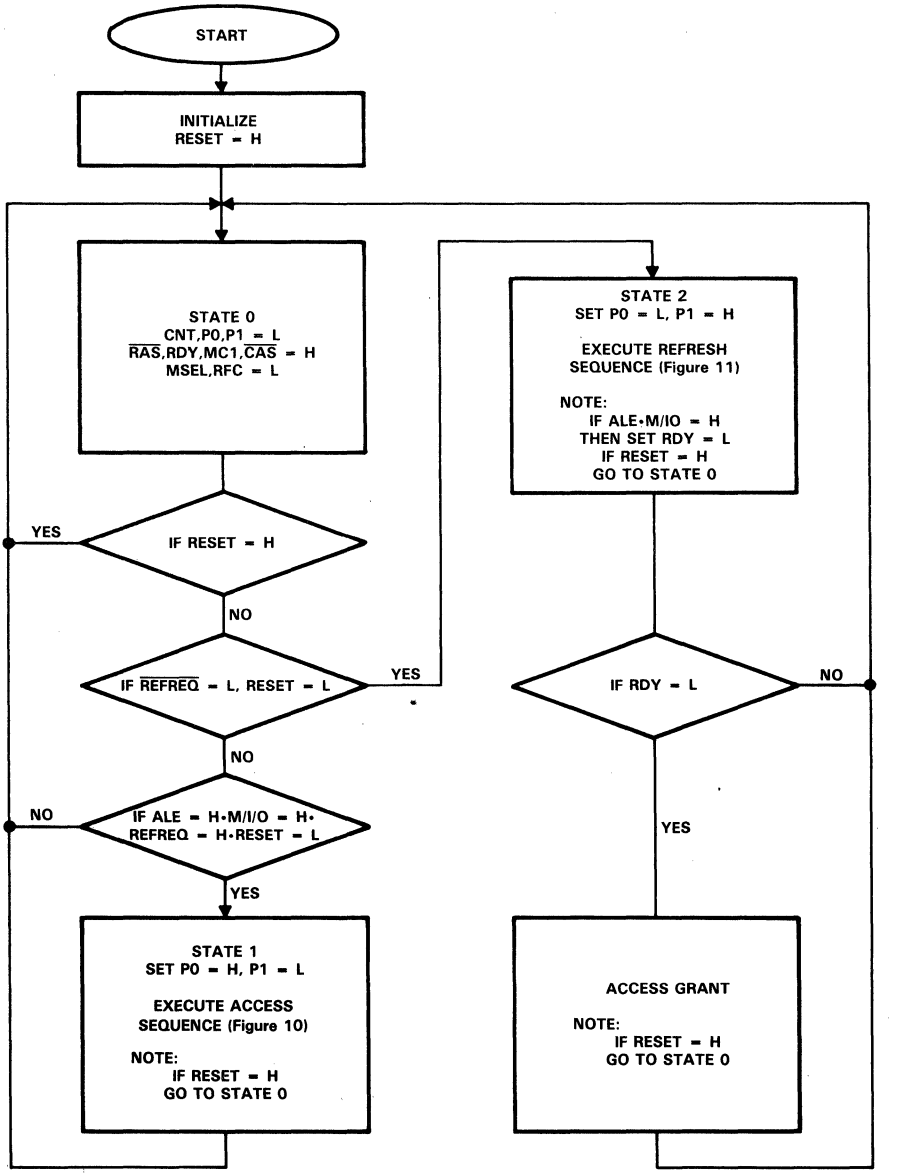


Figure 9. Flow Chart: Dynamic Memory Timing Controller

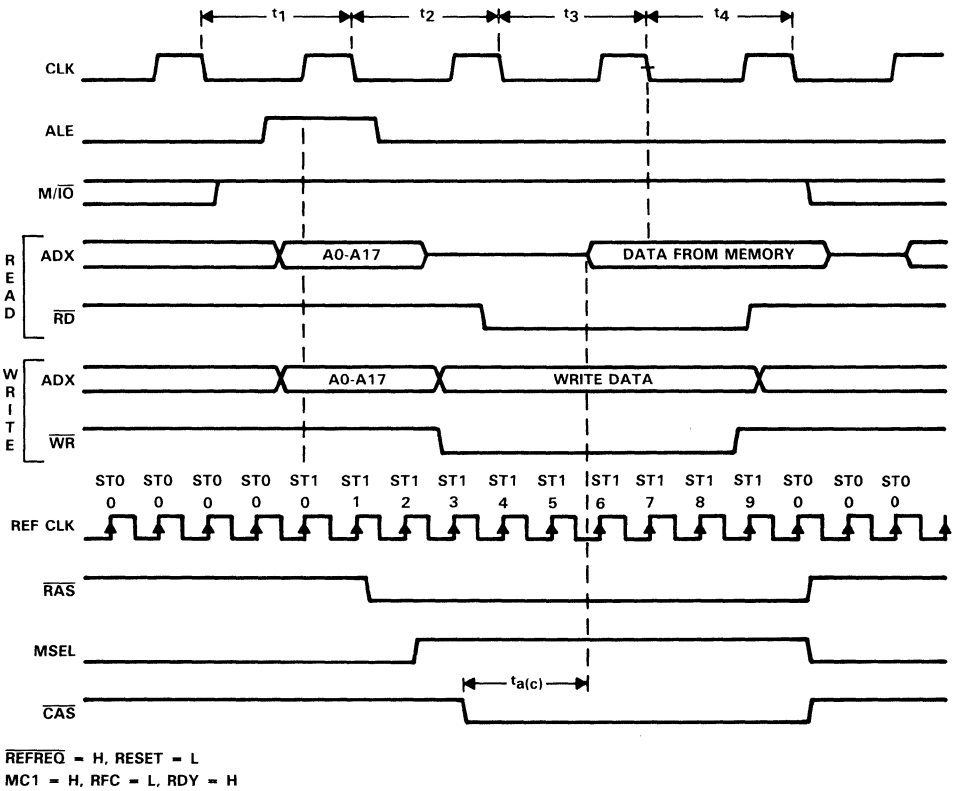


Figure 10. Access Cycle

Developing the logic equations for this application becomes a simple matter when referencing the sequences to a decimal count (Figures 10 and 11). It is important to realize that each sequence has been referenced to a state. This allows the same binary counter to be used for each sequence, even though each sequence is of a different length.

The first step in implementing the above application is to define the logic equations which will make the binary counter perform as described in the flow chart of Figure 9. As will become evident, these equations fall directly from the flow chart. After the counter has been made to perform as described, the outputs can be easily decoded from the binary count and the present state of the state holding registers.

Figure 12 shows a fuse map for step 1 as described above. Initalization is performed by taking the reset input high. When this condition occurs, all product lines except the reset product line are forced inactive. When the reset product line is active, the counter and state holding registers (P0 and P1) are reset to zero on the first active clock edge. The $\overline{CNT}$/HLD1 register is set high, which places the counter in the hold mode. The RDY, MC1, $\overline{RAS}$, and $\overline{CAS}$ outputs are driven high on the same active clock edge. Since the RDY output does not feed back to the AND array, a buried state register, BRDY, is used to monitor the RDY output and is also set high. MSEL and RFC are driven low.

Controlling the binary counter is a simple matter and normally takes only a couple of logic equations. For each sequence, a start and stop condition must be defined. In the case of ST1, when the condition RESET = L, ALE = H, M/$\overline{IO}$ = H, $\overline{REFREQ}$ = H, P0 = L, and P1 = L occurs, ST0 (P1 = L, P0 = L) changes to ST1 (P1 = L, P0 = H), and the $\overline{CNT}$/HLD1 register is driven low to let the counter advance on the next active clock edge. When the counter reaches nine, ST1 returns to ST0 and the counter is cleared and put back into the hold condition.

In the case of ST2, when the condition RESET = L, $\overline{REFREQ}$ = L, P0 = L, and P1 = L occurs, ST0 changes to ST2 (P1 = H, P0 = L) and the $\overline{CNT}$/HLD1 register is driven low to let the counter advance on the next active clock

edge. As shown in the flow chart, if M/IO and ALE go high while in state 2, RDY and BRDY will be reset low on the next active clock edge. When the counter reaches nine, if RDY (BRDY) is high the state registers are returned to ST0 and the counter is cleared and placed back into the hold condition. If RDY (BRDY) is low, the counter advances on until it reaches 19. ST2 then returns to ST0 with the counter being cleared and placed back into the hold condition.

With the binary counter programmed to execute the flow chart in Figure 9, it is now a simple matter of decoding the outputs to perform as required in Figures 10 and 11. This is the same technique used in Example 1, except now a state has been assigned to each sequence. Below is a summary of the switching requirements for both the access (ST1) and the refresh sequence (ST2).

Access Sequence		Refresh Sequence	
ST1 CNT 0:	Reset $\overline{RAS}$	ST2 CNT 0:	Reset MC1
ST1 CNT 1:	Set MSEL	ST2 CNT 1:	Set RFC, Reset $\overline{RAS}$
ST1 CNT 2:	Reset $\overline{CAS}$	ST2 CNT 5:	Reset RFC
ST1 CNT 9:	Set $\overline{RAS}$, Reset MSEL, Set $\overline{CAS}$	ST2 CNT 6:	Set $\overline{RAS}$
		ST2 CNT 7:	Set MC1
		ST2 CNT 10:	Reset $\overline{RAS}$
		ST2 CNT 11:	Set MSEL
		ST2 CNT 12:	Reset $\overline{CAS}$, Set RDY, Set BRDY
		ST2 CNT 19:	Set $\overline{RAS}$, Reset MSEL, Set $\overline{CAS}$

Note that the transition changes are set up in the previous clock cycle, just as in Example 1. Figure 13 shows a complete fuse map for the memory controller.

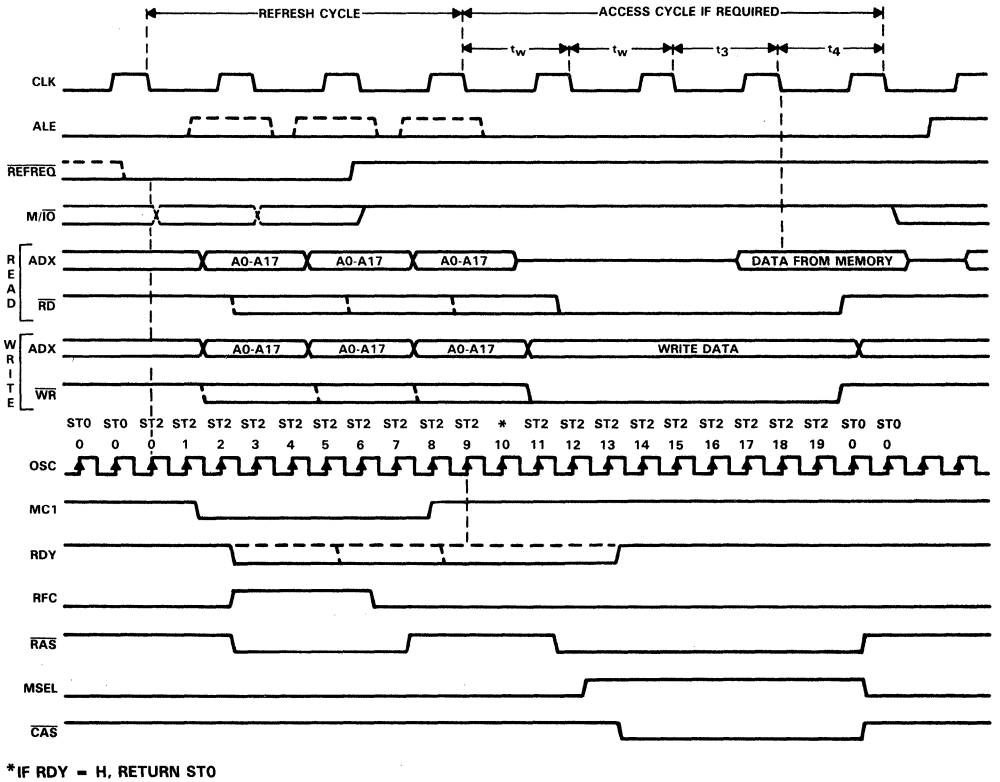


Figure 11. Refresh/Access Grant Cycle

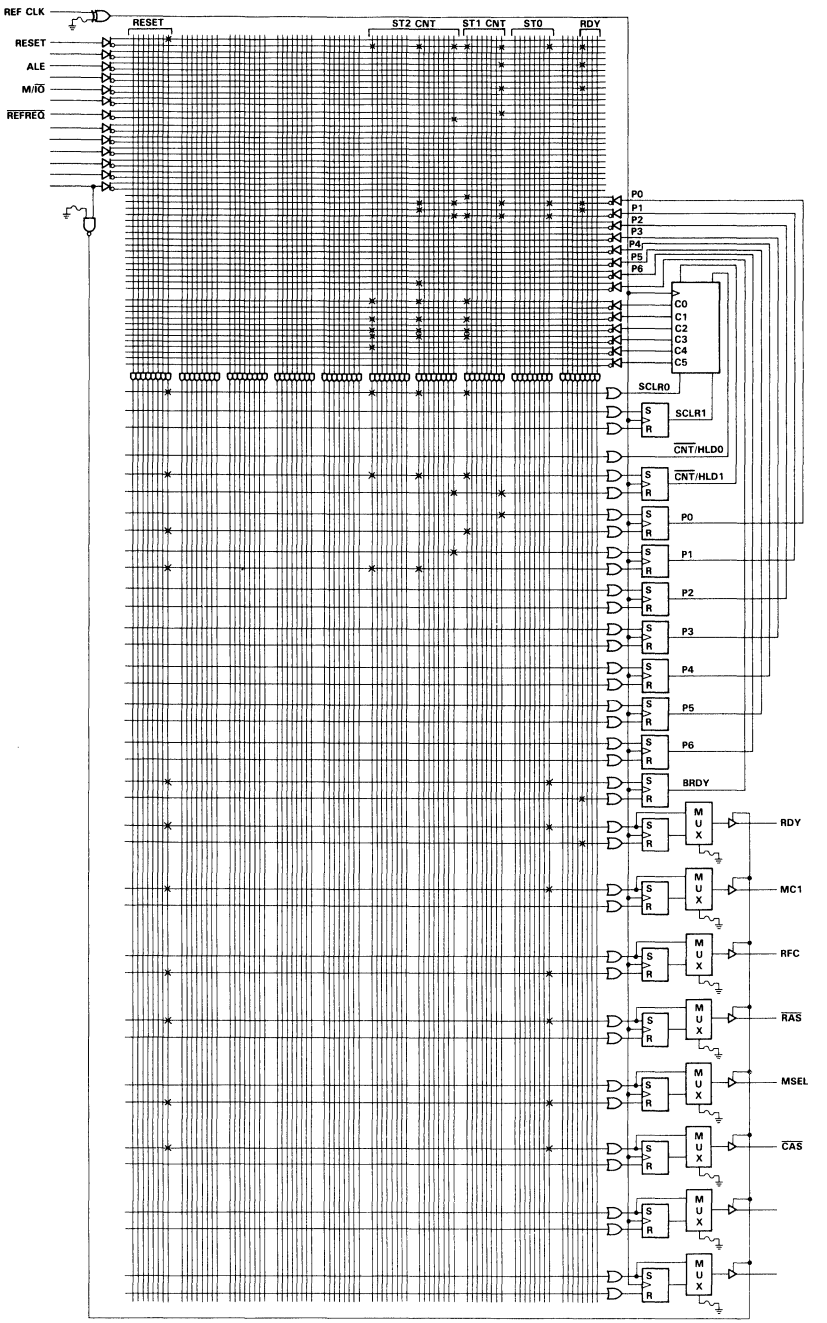


Figure 12. Counter Control Logic
(Example 3 — Dynamic Memory Timing Controller)

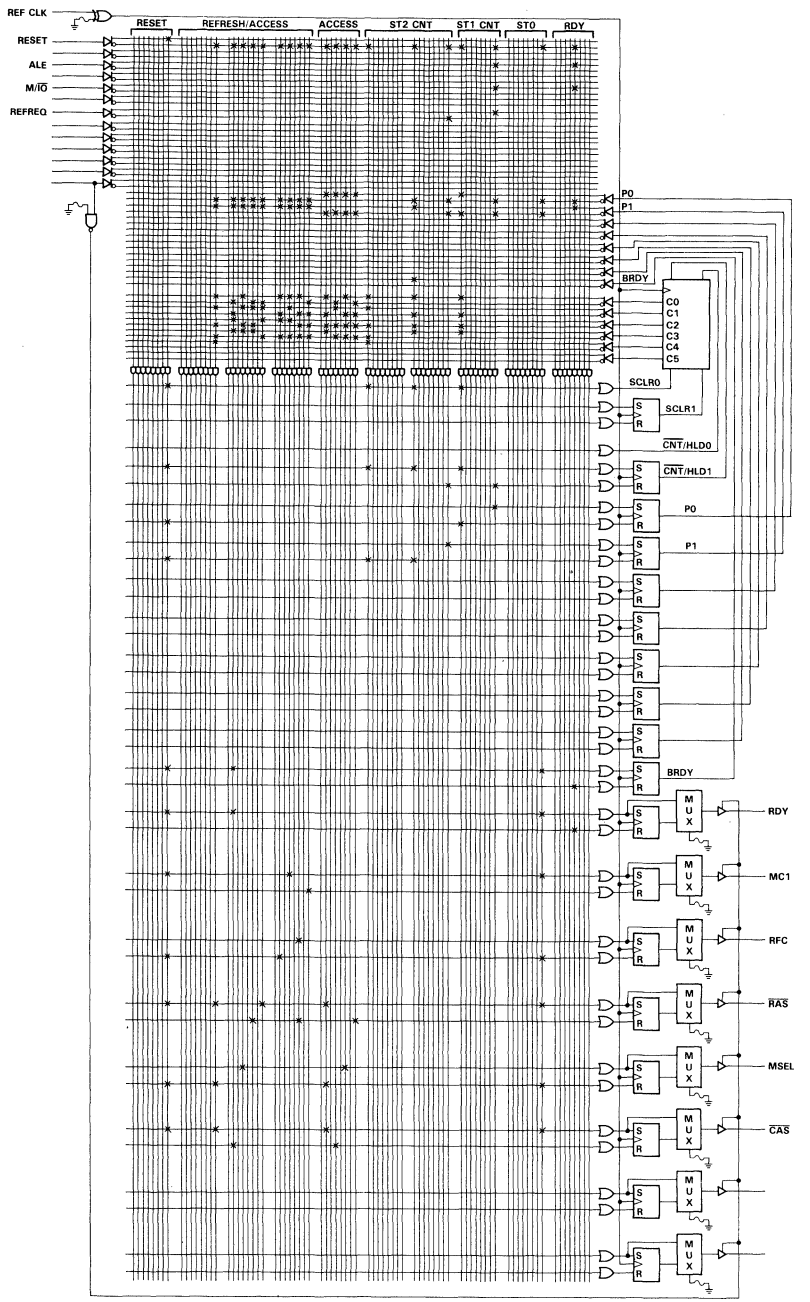


Figure 13. Memory Timing Controller (Example 3)

DESIGNER NOTES

Obtaining Maximum Counter Performance

As with any programmable logic device, there are usually several different methods for implementing any one application. In some cases, device performance is affected. On the PSG, maximum counter frequency is affected by how the designer controls the 6-bit counter.

For example, in the waveform generator example shown at the beginning of this application note, the counter was reset to zero after reaching count 11 by using the nonregistered SCLR0 function. By using the registered SCLR1 function, a higher operating frequency is obtainable.

This method requires an additional "AND" term as shown in Figure 14, but does provide maximum performance. Note that during the 10th clock cycle the set input on the SCLR1 register is high. On the next active clock edge, the counter advances to 11 and the SCLR1 register is set high. This causes the counter to be reset on the next active clock edge. At the same time, the SCLR1 register is reset low to allow the counter to advance past zero.

In effect, the setup time requirement for SCLR1 is performed in the previous clock cycle. When using the SCLR0 method, the setup time must be added to the f_{max} equation. This results in a lower f_{max}. The same tradeoffs apply with the $\overline{CNT}$/HLD function. The PSG507 data sheet specifies f_{max} for both methods.

Expanding the 6-Bit Counter

In Example 2, the six bit counter had to be expanded to 7 bits. This was accomplished by adding one of the state registers to the most significant bit of the counter. It should be noted that the synchronous clear and count hold functions must be controlled through the set and reset inputs of the added bits. The designer must be aware of certain limitations when trying to perform this function. Figure 15 shows three additional bits being added to the 6-bit counter. Note that every bit added requires two additional "AND" terms.

A problem can arise on certain counts when trying to generate a synchronous clear before reaching the full binary count (all outputs high). The designer must ensure that both S and R are not high simultaneously. For example, let's say we want the 9-bit counter to return to zero at count 383 (101111111_2). At count 383, the S/R register used for C7 is being told to set. Therefore, any reset command would result in both S and R being high simultaneously.

This problem, only seen on a few data words, can be solved by using another state register to control the counter reset. This method is similar to that used above to obtain maximum operating frequency. Figure 16 shows the 9-bit counter returning to zero after count 383. Notice that at count 382 the extra S/R register is being told to reset on the next active clock edge. At count 383 the six product lines controlling C6, C7, and C8 are disabled by the feedback from the extra register, in particular the S input on C7. At count 383, the 9-bit counter will return to zero and the extra register is set high.

An extra register may also be needed to achieve the count/hold function when using an expanded counter. During certain counts the added bits will change state, even though the 6-bit counter is programmed to hold. For example, let's say we want the 9-bit counter to hold at count 383. Even though the 6-bit counter can be held at 111111, C6 and C7 will advance on the next active clock edge. In order to hold C6 and C7 where they are, an extra register is used to disable the product lines responsible for the transition from count 383 to 384. Since the counter is on hold, the extra hold register can only be reset from an input pin or a state register(s) transition (not on the next count). In this example, an input pin is used to reset the extra register and the $\overline{CNT}$/HOLD register. When the CONTINUE input is taken low, the counter will continue to advance. The system must guarantee that the continue input will not be low during count 382 to avoid the indeterminant set = H, reset = H state. Figure 17 shows this 9-bit counter.

It is also important to note that when using extra registers a reset input may be necessary to set the extra registers high after powerup, since all S/R registers power-up clear. This requirement would not be necessary if the phase of the extra register was reversed. This is easily accomplished by using the inverted feedback from the extra register. However, it is good state machine design practice to include a reset input that forces all S/R registers to a known state.

Software Support

The PSG507 is supported by two software packages; CUPL, which was created by and is supported by Assisted Technologies, a division of Personal CAD Systems Incorporated, and ABEL, which was created by and is supported by FutureNet, a division of Data I/O Corporation. Each of these software packages can be used to reduce equations and to generate a fuse map necessary to program the PSG507. Appendices A and B show the ABEL and CUPL files for Examples 1, 2, and 3. In addition, a PSG507 template is shown for each software package. These templates provide software information that will make it easier for the designer to create the source files.

Test vectors are included with the ABEL and CUPL source files so software simulation can be performed on the computer. If the proper instruction is provided, the software will attach the test vectors to the end of the fuse map. This allows programming equipment to run a functional test on each device immediately after programming.

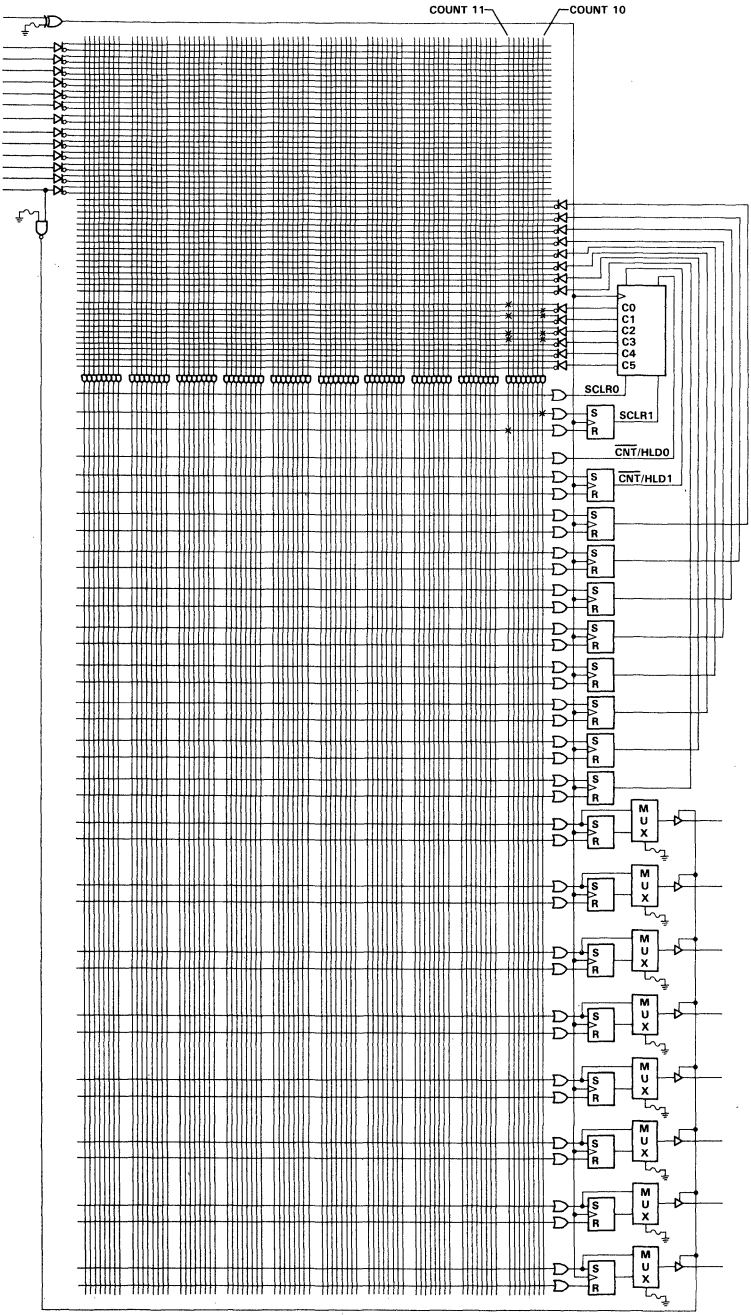


Figure 14. Registered $\overline{\text{SCLR}}$ Example (Designer Notes)

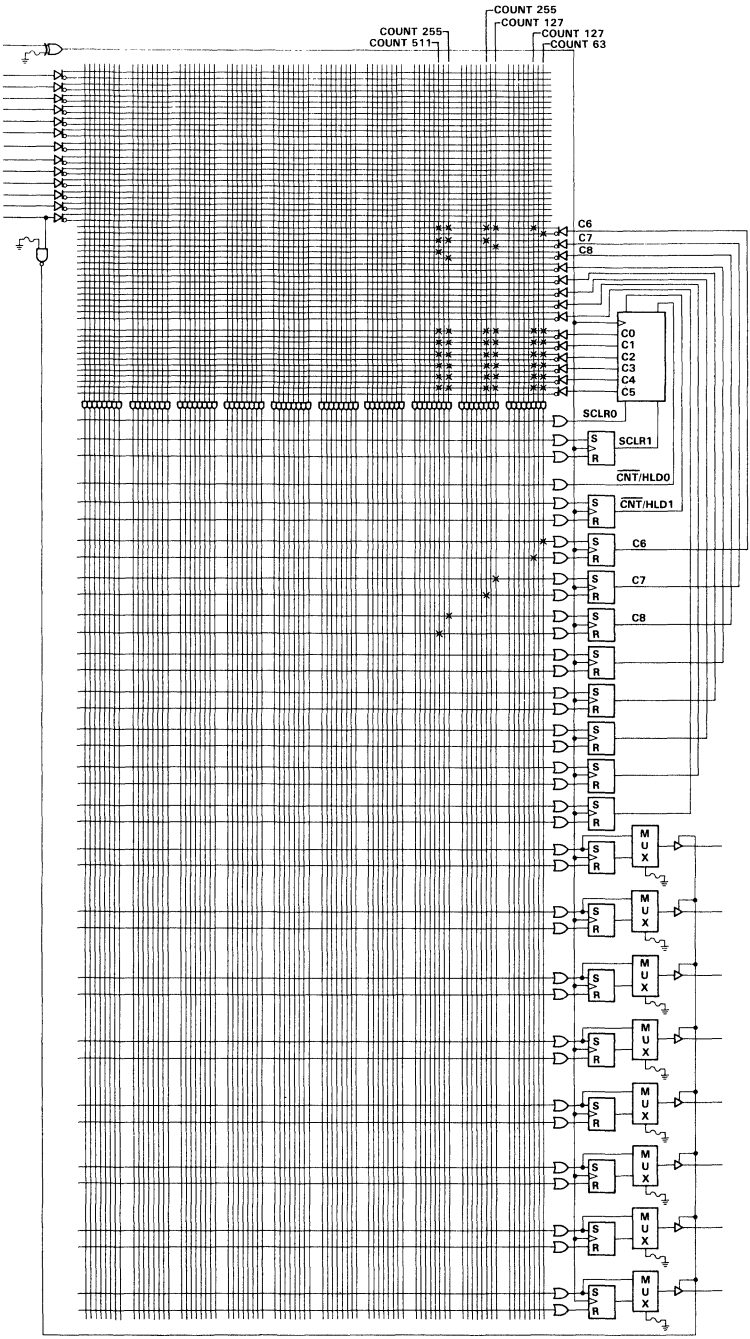


Figure 15. Expanding to 9-Bit Counter

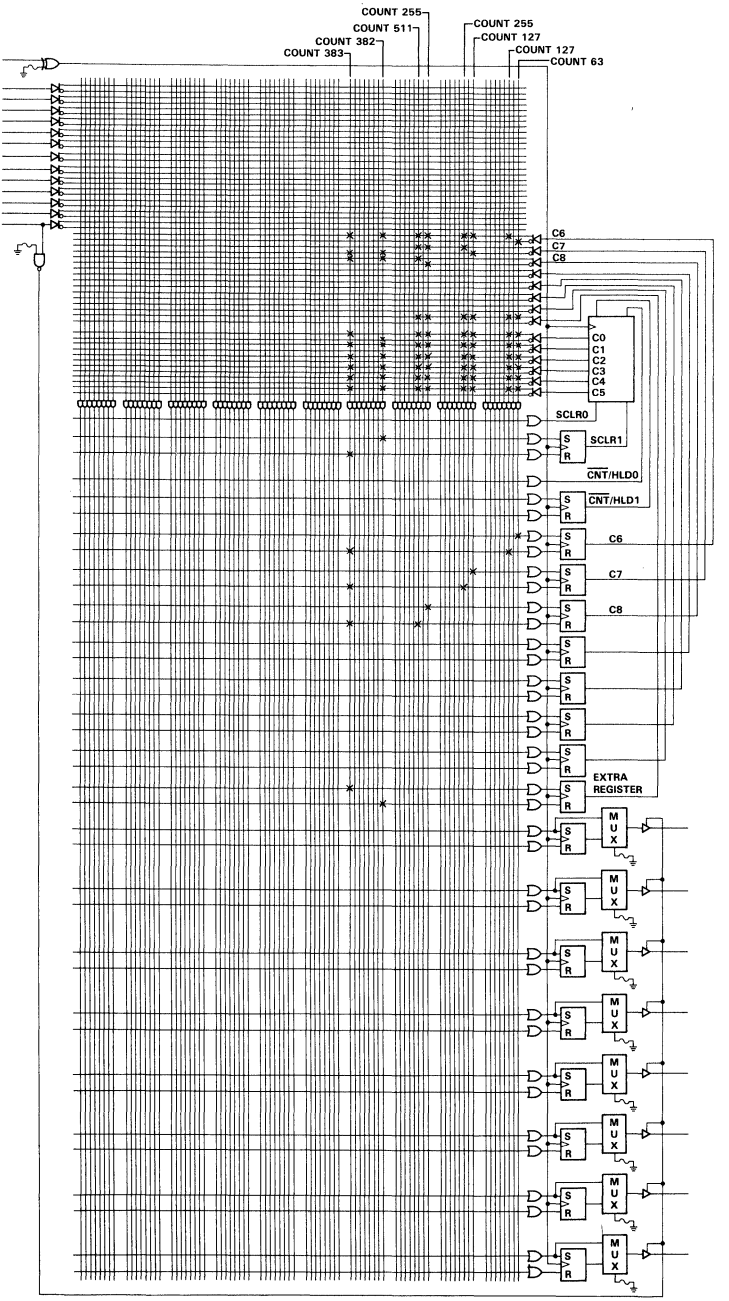


Figure 16. Resetting after Count 383 (Expanding the 6-Bit Counter)

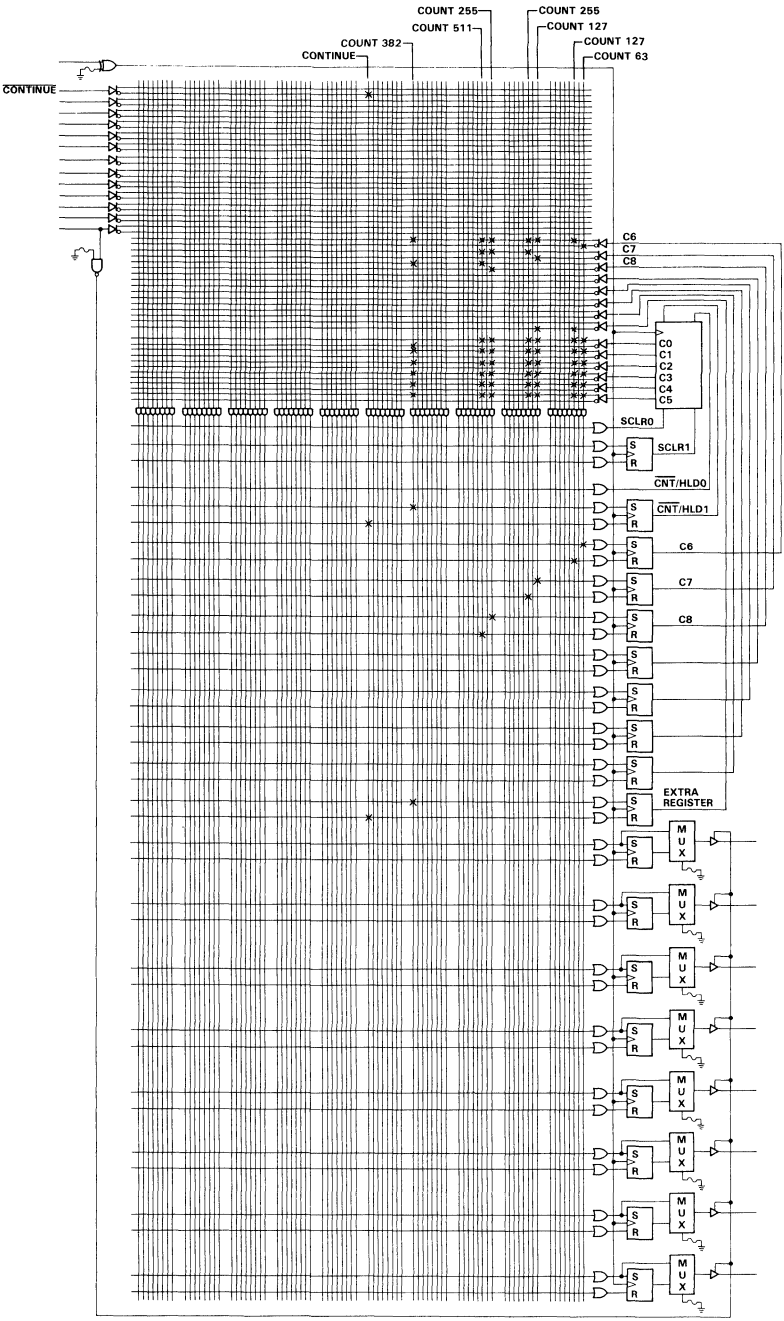


Figure 17. Holding the 9-Bit Counter at Count 383 (Expanding the 6-Bit Counter)

```
" " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " "
" ABEL (tm) TEMPLATE FOR THE TI PSG507                                                          "
"                                                                                              "
" This file provides the PSG507 designer quick access to the information                       "
" needed to write an ABEL source file. To use this file as a template, make                    "
" a copy and delete this box from your new file.                                               "
"                                                                                              "
" NODES: The PSG counter bits, counter control bits and state register bits                    "
"        are accessed through the use of nodes.  Any valid identifier can                      "
"        be used for node names.  The node numbers are specific and must be                    "
"        used as shown below. Nodes that will not be used do not have to be                    "
"        declared.                                                                             "
"                                                                                              "
" OUTPUT STRUCTURE:  The default output stucture is registered.  The output                    "
"                    type is determined by usage, i.e. Q0 := (COUNT==7);                       "
"                    will cause Q0 to remain registered and Q0 = (COUNT==7);                   "
"                    will cause Q0 to be combinatorial.  When an output is                     "
"                    used as nonregistered, ABEL will automatically program                    "
"                    the associated reset fuses as required in the PSG507                      "
"                    data sheet.  Unused  product  terms can  be  left                         "
"                    connected to either side of an output register.                           "
"                                                                                              "
" CLOCK POLARITY:  The default clock polarity is active on the rising edge.                    "
"                  The statement fuses [7360]=1; can be used to blow the                       "
"                  clock polarity fuse so that the clock will be active on                     "
"                  the falling edge (fuses [7360]=0; is the default). 7360                     "
"                  is the clock polarity fuse number.                                          "
"                                                                                              "
" OUTPUT ENABLE:  The output enable fuse is blown by using the equation                        "
"                 enable output = !en; where output is a defined output pin                    "
"                 or set of outputs and en is assigned to pin 17.  The                         "
"                 default  condition is permantly enabled with pin 17 an                       "
"                 input.  If desired the default condition can be specified                    "
"                 with enable output = en;  This fuse can also be blown by                     "
"                 the statement: fuses [7361]=1;                                               "
"                                                                                              "
" SET NOTATION:  Set notation is often used to represent control, buried                       "
"                state, and output registers. This is done to simplify                         "
"                equations.  The sets shown below (Q0_ = [Q0, Q0_r];) are                      "
"                in the form; New register name = [set input, reset input].                    "
"                Note that the ouput register pin name specifies the set                       "
"                input.                                                                        "
"                                                                                              "
"                The sets 'high' and 'low' (high=[1,0]; and low=[0,1];) can                    "
"                be used to set or reset the S/R registers.   Example:                         "
"                Q1_ := high & I0; will cause pin 9 to go high on the next                     "
"                clock edge if input pin 7 is high.                                            "
"                                                                                              "
" SIMULATION:    During simulation of a PSG507 design the ABEL 2.10a                           "
"                simulator will advance the counter on each clock depending                    "
"                on the state of the counter hold and clear functions.                         "
"                If counter bits are included on the output side of a test                     "
"                vector simulation errors will occur. Counter bits included                    "
"                on the input side of the test vectors are ignored.  The                       "
"                powerup condition (counter bits and all registers low) is                     "
"                recognized by the simulator.                                                  "
"                                                                                              "
"  ABEL is a trademark of Data I/O Corporation                                                 "
"                                                                                              "
" " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " " "
```

```
Module PSGFILE
title 'ABEL TEMPLATE FILE FOR THE TEXAS INSTRUMENTS PSG507'

        PSG device 'F507';

" Input pin assignments
CLK       pin   1;                          " comments
I0        pin   7;                          "
I1        pin   6;                          "
I2        pin   5;                          "
I3        pin   4;                          "
I4        pin   3;                          "
I5        pin   2;                          "
I6        pin  23;                          "
I7        pin  22;                          "
I8        pin  21;                          "
I9        pin  20;                          "
I10       pin  19;                          "
I11       pin  18;                          "
I12_OE    pin  17;                          "

" Output pin and node assignments
Q0        pin   8;  Q0_r    node 47;        " comments
Q1        pin   9;  Q1_r    node 48;        "
Q2        pin  10;  Q2_r    node 49;        "
Q3        pin  11;  Q3_r    node 50;        "
Q4        pin  13;  Q4_r    node 51;        "
Q5        pin  14;  Q5_r    node 52;        "
Q6        pin  15;  Q6_r    node 53;        "
Q7        pin  16;  Q7_r    node 54;        "

" Internal counter bits & control - node declarations
C0,C1,C2,C3,C4,C5  node 55,56,57,58,59,60;

SCLR0     node 25;                          " nonregistered counter clear con-
trol
SCLR1     node 26;  SCLR1_r    node 27;     " registered counter clear control
CNTHOLD0  node 28;                          " nonregistered count/hold control
CNTHOLD1  node 29;  CNTHOLD1_r node 30;     " registered count/hold control

" Buried state registers - node declarations
P0        node 31;  P0_r       node 39;     " buried state register
P1        node 32;  P1_r       node 40;     " buried state register
P2        node 33;  P2_r       node 41;     " buried state register
P3        node 34;  P3_r       node 42;     " buried state register
P4        node 35;  P4_r       node 43;     " buried state register
P5        node 36;  P5_r       node 44;     " buried state register
P6        node 37;  P6_r       node 45;     " buried state register
P7        node 38;  P7_r       node 46;     " buried state register

@page
```

```
Q0_ = [Q0, Q0_r];
Q1_ = [Q1, Q1_r];
Q2_ = [Q2, Q2_r];
Q3_ = [Q3, Q3_r];
Q4_ = [Q4, Q4_r];
Q5_ = [Q5, Q5_r];
Q6_ = [Q6, Q6_r];
Q7_ = [Q7, Q7_r];
SCLR1_     = [SCLR1, SCLR1_r];
CNTHOLD1_ = [CNTHOLD1, CNTHOLD1_r];

" Intermediate declarations for simplification
INPUTS     = [I12_OE,I11,I10,I9,I8,I7,I6,I5,I4,I3,I2,I1,I0];
OUTPUTS    = [Q7,Q6,Q5,Q4,Q3,Q2,Q1,Q0];
STATE_     = [P7,P6,P5,P4,P3,P2,P1,P0];
COUNT      = [C5,C4,C3,C2,C1,C0];
H,L,X,Z    = 1, 0, .X.,.Z.;
high       = [ 1,  0];
low        = [ 0,  1];
ck         = .C.;    " Use .K. for falling edge, .C. for rising edge clock.


" DEVICE FUNCTION can be specified using state diagrams, equations,
" and truth tables.


test_vectors ' optional header
([CLK, INPUTS ] -> [OUTPUTS, STATE_])
 [ ck,         ] -> [       ,       ];   "count xx
 [ ck,         ] -> [       ,       ];   "count xx
 [ ck,         ] -> [       ,       ];   "count xx
end PSGFILE
```

```
Module PSG_EX1
title 'ABEL EXAMPLE #1 (Waveform Generator) for the
PSG507 DESIGNERS GUIDE, Texas Instruments,  August 26, 1987'

        PSG1 device 'F507';

" Input pin assignments
PSG_CLK  pin   1;

" Output pin and node assignments
REF_CLK  pin   8;
SYS_CLK  pin   9;   SYS_CLK_r  node 48;
PCLK     pin  10;   PCLK_r     node 49;

REF_CLK IsType 'com';   " REF_CLK is combinational

" Internal counter bits & control - node declarations
C0     node 55;    C1    node 56;
C2     node 57;    C3    node 58;
SCLR0  node 25;

" Intermediate declarations for simplification
COUNT    = [C3,C2,C1,C0];
H,L,clk  = 1, 0, .C.;

equations
REF_CLK    = !C0;
SYS_CLK    := (COUNT==5) # (COUNT==11);  " High on cnt 5 and 11
SYS_CLK_r  := (COUNT==1) # (COUNT==7);   " Low on cnt 1 and 7
PCLK       := (COUNT==11);               " High on cnt 11
PCLK_r     := (COUNT==5);                " Low on cnt 5
SCLR0       = (COUNT==11);               " Counter cleared after cnt 11


" The PSG507 has powerup clear of counter and registers.  Six clocks
" are required after powerup for this design to initialize.  This
" design could be initialized after one clock by setting SYS_CLK and
" PCLK high at COUNT0. i.e. SYS_CLK := COUNT0 # COUNT5 # COUNT11; and
" PCLK := COUNT0 # COUNT11;
```

```
test_vectors
([PSG_CLK , COUNT] -> [REF_CLK, SYS_CLK, PCLK])
 [ clk    ,    0  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,    1  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,    2  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,    3  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,    4  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,    5  ] -> [   H   ,    H   ,  L  ];
 [ clk    ,    6  ] -> [   L   ,    H   ,  L  ];
 [ clk    ,    7  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,    8  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,    9  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,   10  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,   11  ] -> [   H   ,    H   ,  H  ];
 [ clk    ,    0  ] -> [   L   ,    H   ,  H  ];
 [ clk    ,    1  ] -> [   H   ,    L   ,  H  ];
 [ clk    ,    2  ] -> [   L   ,    L   ,  H  ];
 [ clk    ,    3  ] -> [   H   ,    L   ,  H  ];
 [ clk    ,    4  ] -> [   L   ,    L   ,  H  ];
 [ clk    ,    5  ] -> [   H   ,    H   ,  L  ];
 [ clk    ,    6  ] -> [   L   ,    H   ,  L  ];
 [ clk    ,    7  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,    8  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,    9  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,   10  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,   11  ] -> [   H   ,    H   ,  H  ];
 [ clk    ,    0  ] -> [   L   ,    H   ,  H  ];

end PSG_EX1
```

```
Module PSG_EX2
title 'ABEL EXAMPLE #2 (Refresh Timer) for the
PSG507 DESIGNERS GUIDE, Texas Instruments,  August 26, 1987'

        PSG2 device 'F507';

" Input pin assignments
PSG_CLK  pin   1;
RESET    pin   2;
RFC      pin   3;

" Output pin and node assignments
REFREQ   pin   8;  REFREQ_r node 47;

" Internal counter bits & control - node declarations
C0 node 55;  C1 node 56;  C2 node 57;
C3 node 58;  C4 node 59;  C5 node 60;
SCLR0  node 25;

" Buried register
C6 node 31; C6_r node 39; " 7th counter bit

" Intermediate declarations for simplification
COUNT      = [C6,C5,C4,C3,C2,C1,C0];
H,L,clk,X  = 1, 0, .C., .X.;

equations
REFREQ    := RFC # RESET;                      " set input
REFREQ_r  := (COUNT==76) & !RESET;             " reset input
C6        := (COUNT==63) & !RESET;             " set input
C6_r      := (COUNT==76) & !RESET # RESET;     " reset input
SCLR0      = (COUNT==76) & !RESET # RESET;     " synchronous nonregistered
clear


test_vectors              ([PSG_CLK,RESET,RFC] ->  REFREQ )
                           [  clk  ,  H  , X ] ->    H     ;   "CNT0
@REPEAT 76  {              [  clk  ,  L  , L ] ->    H     ; } "CNT1-76
                           [  clk  ,  L  , L ] ->    L     ;   "CNT0
@REPEAT 20  {              [  clk  ,  L  , L ] ->    L     ; } "CNT1-20
                           [  clk  ,  L  , H ] ->    H     ;   "CNT21
                           [  clk  ,  L  , L ] ->    H     ;   "CNT22
                           [  clk  ,  H  , X ] ->    H     ;   "CNT0


end PSG_EX2
```

```
Module PSG_EX3
title 'ABEL EXAMPLE #3 (Dynamic Memory Timing Controller)
for the PSG507 DESIGNERS GUIDE, Texas Instruments,  August 26, 1987'

        PSG3 device 'F507';

" Input pin assignments
OSC       pin   1;                        " OSCILLATOR
RESET     pin   2;                        " RESET - INITIALIZES WHEN HIGH
ALE       pin   3;                        " ADDRESS LATCH ENABLE
MIO       pin   4;                        " MEMORY I/O
REFREQ    pin   5;                        " REFRESH REQUEST

" Output pin and node assignments
RDY       pin   8;  RDY_r     node 47;    " READY
MC1       pin   9;  MC1_r     node 48;    " MODE CONTROL
RFC       pin  10;  RFC_r     node 49;    " REFRESH COMPLETE
RAS       pin  11;  RAS_r     node 50;    " ROW ADDRESS STROBE
MSEL      pin  13;  MSEL_r    node 51;    " MULTIPLEXER SELECT
CAS       pin  14;  CAS_r     node 52;    " COLUMN ADDRESS STROBE

" Internal counter bits & control, and state reg - node declarations
C0        node 55;  C1 node 56;  C2 node 57;
C3        node 58;  C4 node 59;
SCLR0     node 25;
CNTHOLD1 node 29;  CNTHOLD1_r node 30; " COUNT/HOLD CONTROL REGISTER
P0        node 31;  P0_r        node 39; " BURIED STATE REGISTER
P1        node 32;  P1_r        node 40; " BURIED STATE REGISTER
BRDY      node 33;  BRDY_r      node 41; " BURIED READY SIGNAL

" Set notation is used to represent control, buried state, and output
" registers. This is done to simplify the equations.  The following
" sets are in the form;  register name = [set input, reset input]. Note
" that the ouput register pin name specifies the set input.
RDY_      = [RDY, RDY_r];
MC1_      = [MC1, MC1_r];
RFC_      = [RFC, RFC_r];
RAS_      = [RAS, RAS_r];
MSEL_     = [MSEL, MSEL_r];
CAS_      = [CAS, CAS_r];
BRDY_     = [BRDY, BRDY_r];

" Intermediate declarations for simplification.
" The sets 'high' and 'low' are used to set or reset the S/R
" registers.  Example: MC1_ := high & RESET; will cause pin 9
" to go high on the next clock edge if input pin 2 is high.
high      = [ 1,  0];
low       = [ 0,  1];
COUNT     = [C4,C3,C2,C1,C0];
STATE_    = [P1,P0];            " STATE REGISTER SET DEFINED
H,L,clk,X = 1, 0, .C., .X.;
@page
```

```
equations
        enable MC1 = 1;  "outputs always enabled, pin 12 is only an input

" Initialization when RESET is high
        [ BRDY,RDY,MC1,RAS,CAS]     :=  RESET;
        [ P0_r,P1_r,MSEL_r,RFC_r]   :=  RESET;

" Counter controls defined
SCLR0 =          RESET
             # (STATE_==1) & (COUNT==9)
             # (STATE_==2) & (COUNT==9) & BRDY
             # (STATE_==2) & (COUNT==19);

CNTHOLD1    =   RESET
             # (STATE_==1) & (COUNT==9)
             # (STATE_==2) & (COUNT==9) & BRDY
             # (STATE_==2) & (COUNT==19);

CNTHOLD1_r =    (STATE_==0) & ALE & MIO & REFREQ & !RESET
             # (STATE_==0) & !REFREQ & !RESET;

" Execution of access and refresh sequènces
state_diagram STATE_                                    " NEXT
   State 0:          case                               " STATE
                       RESET==H                           : 0;
                       ALE & MIO & REFREQ & !RESET        : 1;
                      !REFREQ & !RESET                    : 2;
                       REFREQ & (!ALE # !MIO)             : 0;
                     endcase;
" ACCESS CYCLE
   State 1:          RAS_   := (COUNT==0) & low  & !RESET;
                     MSEL_  := (COUNT==1) & high & !RESET;
                     CAS_   := (COUNT==2) & low  & !RESET;
                     RAS_   := (COUNT==9) & high;
                     MSEL_  := (COUNT==9) & low;
                     CAS_   := (COUNT==9) & high;
                               if (COUNT==9) # RESET then 0 else 1;

" REFRESH CYCLE WITH ACCESS GRANT
   State 2:          RDY_   := low & ALE & MIO  & !RESET;
                     BRDY_  := low & ALE & MIO  & !RESET;
                     MC1_   := (COUNT==0) & low  & !RESET;
                     RFC_   := (COUNT==1) & high & !RESET;
                     RAS_   := (COUNT==1) & low  & !RESET;
                     MC1_   := (COUNT==3) & high;
                     RFC_   := (COUNT==5) & low;
                     RAS_   := (COUNT==6) & high;
                     RAS_   := (COUNT==10)& low  & !RESET;
                     RDY_   := (COUNT==11)& high;
                     BRDY_  := (COUNT==11)& high;
                     MSEL_  := (COUNT==11)& high & !RESET;
                     CAS_   := (COUNT==12)& low  & !RESET;
                     RAS_   := (COUNT==19)& high;
                     MSEL_  := (COUNT==19)& low;
                     CAS_   := (COUNT==19)& high;
                               if (COUNT==9)  & BRDY then 0 else 2;
                               if (COUNT==19)# RESET then 0 else 2;
@page
```

```
test_vectors ' ACCESS SEQUENCE '
([OSC,RESET,ALE,MIO,REFREQ,COUNT] -> [RDY,MC1,RFC,RAS,MSEL,CAS,STATE_])
 [clk,  H  , X , X ,  X   ,  X  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , L , H ,  H   ,  0  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , H , H ,  H   ,  0  ] -> [ H , H , L , H , L  , H ,  1   ];
 [clk,  L  , X , X ,  X   ,  0  ] -> [ H , H , L , L , L  , H ,  1   ];
 [clk,  L  , X , X ,  X   ,  1  ] -> [ H , H , L , L , H  , H ,  1   ];
 [clk,  L  , X , X ,  X   ,  2  ] -> [ H , H , L , L , H  , L ,  1   ];
@CONST cnt = 3; @REPEAT 6  {
 [clk,  L  , X , X ,  X   , cnt ] -> [ H , H , L , L , H  , L ,  1   ];
@CONST cnt = cnt + 1;}
 [clk,  L  , X , X ,  X   ,  9  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , L , L ,  H   ,  0  ] -> [ H , H , L , H , L  , H ,  0   ];

test_vectors ' REFRESH WITH ACCESS FOLLOWING'
([OSC,RESET,ALE,MIO,REFREQ,COUNT] -> [RDY,MC1,RFC,RAS,MSEL,CAS,STATE_])
 [clk,  H  , X , X ,  X   ,  X  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , X , X ,  L   ,  0  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  0  ] -> [ H , L , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  1  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  2  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  3  ] -> [ H , H , H , L , L  , H ,  2   ];
 [clk,  L  , H , H ,  X   ,  4  ] -> [ L , H , H , L , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   ,  5  ] -> [ L , H , L , L , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   ,  6  ] -> [ L , H , L , H , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   ,  7  ] -> [ L , H , L , H , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   ,  8  ] -> [ L , H , L , H , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   ,  9  ] -> [ L , H , L , H , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   , 10  ] -> [ L , H , L , L , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   , 11  ] -> [ H , H , L , L , H  , H ,  2   ];
 [clk,  L  , X , X ,  X   , 12  ] -> [ H , H , L , L , H  , L ,  2   ];
@CONST cnt =13; @REPEAT 6  {
 [clk,  L  , X , X ,  X   , cnt ] -> [ H , H , L , L , H  , L ,  2   ];
@CONST cnt = cnt + 1;}
 [clk,  L  , X , X ,  X   , 19  ] -> [ H , H , L , H , L  , H ,  0   ];

test_vectors ' REFRESH WITHOUT ACCESS FOLLOWING'
([OSC,RESET,ALE,MIO,REFREQ,COUNT] -> [RDY,MC1,RFC,RAS,MSEL,CAS,STATE_])
 [clk,  H  , X , X ,  X   ,  X  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , X , X ,  L   ,  0  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  0  ] -> [ H , L , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  1  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  2  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  3  ] -> [ H , H , H , L , L  , H ,  2   ];
 [clk,  L  , L , H ,  X   ,  4  ] -> [ H , H , H , L , L  , H ,  2   ];
 [clk,  L  , H , L ,  X   ,  5  ] -> [ H , H , L , L , L  , H ,  2   ];
 [clk,  L  , H , L ,  X   ,  6  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , H , L ,  X   ,  7  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , H , L ,  X   ,  8  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , H , L ,  X   ,  9  ] -> [ H , H , L , H , L  , H ,  0   ];
@page
```

```
test_vectors ' RESET DURING REFRESH '
([OSC,RESET,ALE,MIO,REFREQ,COUNT] -> [RDY,MC1,RFC,RAS,MSEL,CAS,STATE_])
 [clk,  H  , X , X ,  X   ,  X  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , X , X ,  L   ,  0  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  0  ] -> [ H , L , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  1  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  2  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  H  , X , X ,  X   ,  3  ] -> [ H , H , L , H , L  , H ,  0   ];

end PSG_EX3
```

```
/*****************************************************************************/
/* CUPL (tm) TEMPLATE FOR THE TI PSG507                                      */
/*                                                                           */
/* This file provides the PSG507 designer quick access to the information   */
/* needed to write a CUPL source file.  By copying this file and deleting    */
/* this box from the  new file a fill-in-the-blanks template will be left    */
/* for use in creating a source file.                                        */
/*                                                                           */
/* 6-BIT COUNTER:  The 6-bit counter is accessed through use of the PINNODE */
/*                 statement.  The pinnode statement is used to assign       */
/*                 variables to the internal node numbers.  i.e. pinnode     */
/*                 [33..38] = [C0..C5].CNT.  These variables can then        */
/*                 be used in the same manner as input pins.Using the        */
/*                 field statement, i.e. field COUNTER = [C0..C5].CNT;       */
/*                 allows an equation like Q0 = COUNTER'd'3 # COUNTER'd'7;    */
/*                 This  equation causes the nonregistered output Q0 to be   */
/*                 high only during counts 3 and 7.                          */
/*                                                                           */
/* COUNTER CONTROLS:  Clear and hold functions SCLR0, SCLR1, CNTHOLD0,       */
/*                    and CNTHOLD1 are specified using the PINNODE           */
/*                    statement. Any valid variable can be used as a node    */
/*                    name, i.e. pinnode [39..42] = [CLR0,CLR1,HLD0,HLD1];   */
/*                    These variables can then be used in the same manner    */
/*                    as an output pin.                                      */
/*                                                                           */
/* STATE  REGISTERS:  Buried registers are assigned using the NODE state-    */
/*                    ment, i.e. node  [P0..P7];.  The actual registers      */
/*                    used are chosen by software in the order specified.    */
/*                                                                           */
/* OUTPUT STRUCTURE: Each output can be defined as either registered or      */
/*                   nonregistered. The structure assignment is automatic    */
/*                   and is determined by usage.  Q0.s = COUNTER'd'77;       */
/*                   causes the Q0 output to remain registered while         */
/*                   Q0 = COUNTER'd'77; causes the Q0 output to be non-      */
/*                   registered.  When using nonregistered outputs CUPL      */
/*                   will automatically program the associated reset fuse    */
/*                   for each product term used as required in the PSG507    */
/*                   data sheet.                                             */
/*                                                                           */
/*****************************************************************************/
```

```
/*****************************************************************************/
/*                                                                           */
/*                                                                           */
/* CLOCK POLARITY:  The default clock polarity is active on the rising       */
/*                  edge.  The equation  OUTPUT.ckmux = !CLK; will cause     */
/*                  the clock to be active on the falling edge.  The         */
/*                  default can be specified by OUTPUT.ckmux = CLK;          */
/*                                                                           */
/* OUTPUT ENABLE:  The default condition is outputs always enabled. The      */
/*                 output enable fuse at pin 17 can be blown using the       */
/*                 .oe extention. If pin 17 = EN; the fuse will be blown     */
/*                 by the equation  OUTPUTS.oe = EN; where OUTPUTS is a      */
/*                 defined set of outputs. A single output can also be       */
/*                 used to blow the fuse, Q0.oe = EN;                        */
/*                                                                           */
/* SIMULATION:     During simulation of a PSG design the CUPL 2.15a          */
/*                 simulator will advance the counter on each clock          */
/*                 depending on the state of the counter hold and clear      */
/*                 functions. The powerup condition (counter bits and        */
/*                 all registers low) is recognized by the simulator.        */
/*                                                                           */
/*   CUPL is a trade mark of Personal CAD Systems, Inc.                      */
/*****************************************************************************/
```

```
NAME      XXXXX ;
PARTNO    XXXXX ;
DATE      XX/XX/XX ;
REV       XX ;
DESIGNER  XXXXX ;
COMPANY   XXXXX ;
ASSEMBLY  XXXXX ;
LOCATION  XXXXX ;

/*************************************************************************/
/*                                                                       */
/*                                                                       */
/*                                                                       */
/*************************************************************************/
/*  Allowable Target Device Types :  TEXAS INTSRUMENTS  PSG507           */
/*************************************************************************/

/**  Inputs  **/
pin  1          = CLK       ;          /* PSG's clock input             */
pin  2          =           ;          /*                               */
pin  3          =           ;          /*                               */
pin  4          =           ;          /*                               */
pin  5          =           ;          /*                               */
pin  6          =           ;          /*                               */
pin  7          =           ;          /*                               */
pin 17          =           ;          /* input and/or output enable    */
pin 18          =           ;          /*                               */
pin 19          =           ;          /*                               */
pin 20          =           ;          /*                               */
pin 21          =           ;          /*                               */
pin 22          =           ;          /*                               */
pin 23          =           ;          /*                               */

/**  Outputs  **/
pin  8          =           ;          /*                               */
pin  9          =           ;          /*                               */
pin 10          =           ;          /*                               */
pin 11          =           ;          /*                               */
pin 13          =           ;          /*                               */
pin 14          =           ;          /*                               */
pin 15          =           ;          /*                               */
pin 16          =           ;          /*                               */

/** Node Declarations **/
pinnode [33..38] = [C0..5]  ;          /* BUILT-IN 6-BIT COUNTER        */
pinnode 39       = SCLR0    ;          /* COUNTER CLEAR - non registered */
pinnode 40       = SCLR1    ;          /* COUNTER CLEAR - registered    */
pinnode 41       = CNTHOLD0 ;          /* COUNTER HOLD  - non registered */
pinnode 42       = CNTHOLD1 ;          /* COUNTER HOLD  - registered    */
node               [P0..P7] ;          /* BURIED STATE REGISTERS        */

/** Declarations and Intermediate Variable Definitions **/
field COUNTER    = [C5..0]  ;          /* 6-BIT COUNTER                 */

/** Logic Equations **/

/** End of File **/
```

```
Name      PSG_EX1;
Partnò    TI0001;
Date      08/26/87;
Rev       02;
Designer  Schiele/Woolhiser;
Company   Texas Instruments/Personnal CAD Systems;
Assembly  None;
Location  None;

/*************************************************************************/
/* Waveform Generator                                                    */
/*                                                                       */
/* This is the first example from "A Designer's Guide to the             */
/* PSG507", by R. Breuninger.  In this example a waveform generator      */
/* which generates three clocks, running at 15, 5, and 2.5MHz, is        */
/* implemented for the PSG507 using CUPL.  In this implementation        */
/* the built-in counter feature of the PSG507 is utilized to divide      */
/* a 30MHz master clock to generate the three output waveforms. The      */
/* built-in counter is accessed by defining the variable list            */
/* [C0..5] as PINNODE's and then using the list where ever the           */
/* counter values are needed. The synchronous clear function, SCLR0      */
/* is also accessed through use of the pinnode statement.                */
/*************************************************************************/
/*  Allowable Target Device Types :   TI PSG507                          */
/*************************************************************************/

/**  Inputs  **/

pin 1            =  PSG_CLK;      /* 30MHz MASTER CLOCK                 */

/**  Outputs  **/

pin 8            = REF_CLK;       /* 15MHz REFERENCE CLOCK              */
pin 9            = SYS_CLK;       /*  5MHz SYSTEM CLOCK                 */
pin 10           = PCLK;          /* 2.5MHz PERIPHERAL CLOCK            */

pinnode [33..36] = [C0..3];       /* BUILT-IN COUNTER                   */
pinnode 39       = SCLR0;         /* COUNTER SYNCHRONOUS CLEAR          */

/** Declarations and Intermediate Variable Definitions **/

field COUNTER    = [C3..0].CNT;

/**[SYS_CLK, PCLK, C0..3].CKMUX = !PSG_CLK;                            **/

/** Logic Equations **/

REF_CLK          = !C0.CNT;
SYS_CLK.r        = COUNTER:'d'1 # COUNTER:'d'7;
SYS_CLK.s        = COUNTER:'d'5 # COUNTER:'d'11;
PCLK.r           = COUNTER:'d'5;
PCLK.s           = COUNTER:'d'11;
SCLR0            = COUNTER:'d'11;

/* The PSG507 has powerup clear of counter and registers.  Six clocks  */
/* are required after powerup for this design to initialize.  This     */
/* design could be initialized after one clock by setting SYS_CLK and  */
/* PCLK high at COUNT 0. i.e. SYS_CLK.s = COUNTER:'d'0 # COUNTER:'d'5  */
/* # COUNTER:'d'11; and  PCLK.s = COUNTER:'d'0 # COUNTER:'d'11;        */

/** End of file **/
```

```
Name      PSG_EX1;
Partno    TI0001;
Date      08/26/87;
Rev       02;
Designer  Schiele/Woolhiser;
Company   Texas Instruments/Personnal CAD Systems;
Assembly  None;
Location  None;

/*************************************************************************/
/*                                                                       */
/* Waveform Generator                                                    */
/*                                                                       */
/* CUPL simulation file for Example 1 from  "A Designer's Guide to  */
/* the PSG507".                                                          */
/*************************************************************************/
/*  Allowable Target Device Types :   TI PSG507                          */
/*************************************************************************/

ORDER: PSG_CLK, %7,. REF_CLK, %9, SYS_CLK, %6, PCLK;

BASE: DECIMAL;

VECTORS:
$msg"  ";
$msg"  PSG_CLK  REF_CLK   SYS_CLK PCLK ";
$msg" ---------------------------------------- ";

         P        X        0     0
         0        H        H     H                    /* 0 */
         C        L        H     H                    /* 1 */
         C        H        L     H                    /* 2 */
         C        L        L     H                    /* 3 */
         C        H        L     H                    /* 4 */
         C        L        L     H                    /* 5 */
         C        H        H     L                    /* 6 */
         C        L        H     L                    /* 7 */
         C        H        L     L                    /* 8 */
         C        L        L     L                    /* 9 */
         C        H        L     L                    /* 10 */
         C        L        L     L                    /* 11 */
         C        H        H     H                    /* 0  */
```

```
Name      PSG_EX2;
Partno    TI0002;
Date      08/26/87;
Rev       02;
Designer  Schiele/Woolhiser;
Company   Texas Instruments/Personal CAD Systems;
Assembly  None;
Location  None;

/*************************************************************************/
/*                                                                       */
/* Refresh Timer                                                         */
/*                                                                       */
/* This is the second example from "A Designer's Guide to the PSG507", by */
/* R. Breuninger.  In this example a dynamic memory refresh timer, which  */
/* generates a refresh request every 15.4 uS, is implemented for the TI   */
/* PSG507 using CUPL.  In this implementation the built-in 6-bit counter  */
/* is extended by using one of the buried state registers as the 7th bit. */
/*                                                                       */
/*************************************************************************/
/*  Allowable Target Device Types :  TI PSG507                           */
/*************************************************************************/

/**  Inputs  **/
pin 1            = PSG_CLK;          /* 5MHz SYSTEM CLOCK               */
pin 2            = RESET;            /* SYNCHRONOUS RESET OR INITIALIZE */
pin 4            = RFC;              /* REFRESH COMPLETE                */

/**  Outputs  **/
pin 8            = REFREQ;           /* REFRESH REQUEST                 */

/** Node Declarations **/
pinnode [33..38] = [C0..5];          /* BUILT-IN 6-BIT COUNTER          */
pinnode 39       = SCLR0;            /* COUNTER CLEAR CONTROLS          */
node               C6;               /* EXTENSION TO 6-BIT COUNTER      */

/** Declarations and Intermediate Variable Definitions **/
field 6BIT       = [C0..5].CNT;      /* 6 BIT COUNTER                   */
field COUNTER    = [6BIT,C6];        /* FULL 7-BIT COUNTER              */

/** Logic Equations **/

REFREQ.s         = RFC # RESET;
REFREQ.r         = COUNTER:'d'76 & !RESET;

/* EXTEND BUILT-IN 6-BIT COUNTER BY ADDING A BURIED STATE REGISTER */

C6.s             =  COUNTER:'d'63 & !RESET;
C6.r             =  COUNTER:'d'76 #  RESET;

/* BUILT-IN COUNTER CONTROL */

SCLR0            = COUNTER:'d'76 # RESET;

/** End of file **/
```

```
Name      PSG_EX2;
Partno    TI0002;
Date      08/26/87;
Rev       02;
Designer  Schiele/Woolhiser;
Company   Texas Instruments/Personal CAD Systems;
Assembly  None;
Location  None;

/*****************************************************************************/
/* Refresh Timer                                                             */
/*                                                                           */
/* CUPL simulation file for example 2 from "A Designer's Guide to the        */
/* PSG507".  This simulation file uses the $REPEAT directive to generate     */
/* many of the test vectors in the counter sequence.                         */
/*****************************************************************************/
/*  Allowable Target Device Types :  TI PSG507                               */
/*****************************************************************************/

ORDER:  PSG_CLK,%6,RESET,%4,RFC,%4,C6,%5,REFREQ;

BASE: DECIMAL;

VECTORS:

$msg"  ";
$msg" NORMAL REFRESH CYCLE WITH REFRESH COMPLETE SIGNAL";
$msg"  ";
$msg"   -------INPUTS--------  -OUTPUT-";
$msg"   PSG_CLK RESET RFC  C6   REFREQ ";
$msg"   ------------------------------------"; /*COUNT*/
         C      1    X    L    H              /*  0  */
         C      0    X    L    H              /*  1  */
$repeat 74;
         C      0    X    *    *              /*2-75 */
$msg "end repeat";
         C      0    0    H    H              /* 76  */
         C      0    0    L    L              /*  0  */
         C      0    0    L    L              /*  1  */
         C      0    0    L    L              /*  2  */
         C      0    1    L    H              /*  3  */
         C      0    0    L    H              /*  4  */

$msg"  ";
$msg" CHECK RESET FUNCTION AFTER REFREQ=L ";
$msg"  ";
$msg"   -------INPUTS--------  -OUTPUT-";
$msg"   PSG_CLK RESET RFC  C6   REFREQ ";
$msg"   ------------------------------------"; /*COUNT*/
         C      1    X    L    H              /*  0  */
         C      0    X    L    H              /*  1  */
$repeat 74;
         C      0    X    *    *              /*2-75 */
$msg "end repeat";
         C      0    0    H    H              /* 76  */
         C      0    0    L    L              /*  0  */
$repeat 29;
         C      0    0    *    *              /*1-30 */
$msg "end repeat";
         C      0    0    L    L              /* 31  */
         C      1    0    L    H              /*  0  */
```

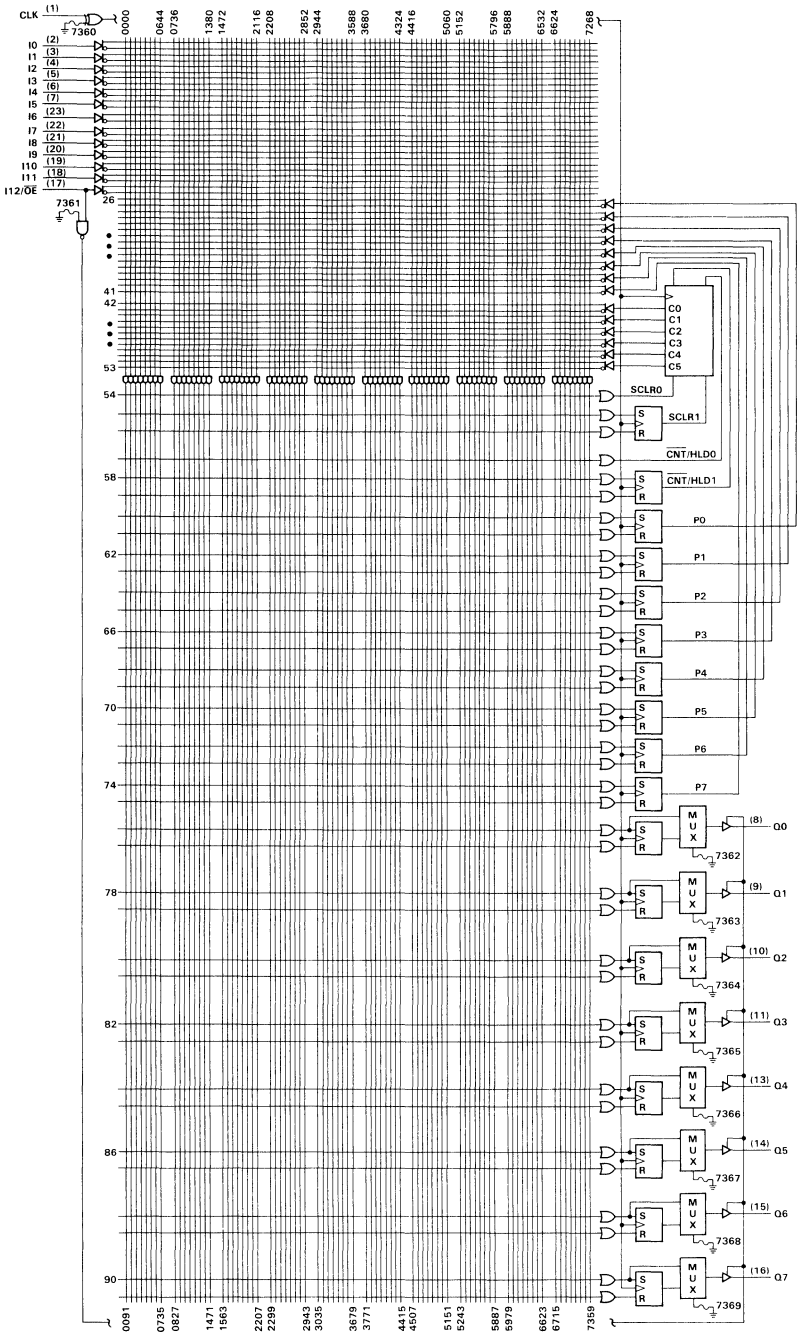
```
Name      PSG_EX3;
Partno    TI0003;
Date      08/26/87;
Rev       02;
Designer  Schiele/Woolhiser;
Company   Texas Instruments/Personnal CAD Systems;
Assembly  None;
Location  None;

/*****************************************************************************/
/*                                                                           */
/* Dynamic Memory Timing Controller                                          */
/*                                                                           */
/* This is the third example from "A Designer's Guide to the PSG507", by     */
/* R. Breuninger.  In this example a dynamic memory timing controller,       */
/* which generates the control signals (RDY, MC1, RFC, RAS, CAS, MSEL)       */
/* necessary for accessing and refreshing dynamic memory, is implemented     */
/* for the TI PSG507 using CUPL.                                             */
/*****************************************************************************/
/*  Allowable Target Device Types :  TI PSG507                               */
/*****************************************************************************/

/**  Inputs  **/
PIN 1            =  REF_CLK;              /* OSCILLATOR                    */
PIN 2            =  RESET;                /* RESET - INITIALIZE            */
PIN 3            =  ALE;                  /* ADDRESS LATCH ENABLE          */
PIN 4            =  MIO;                  /* MEMORY I/O                    */
PIN 5            =  REFREQ;               /* REFRESH REQUEST               */

/**  Outputs  **/
PIN 8            = RDY;                   /* READY                         */
PIN 9            = MC1;                   /* MODE CONTROL                  */
PIN 10           = RFC;                   /* REFRESH COMPLETE              */
PIN 11           = RAS;                   /* ROW ADDRESS STROBE            */
PIN 13           = MSEL;                  /* MULTIPLEXER SELECT            */
PIN 14           = CAS;                   /* COLUMN ADDRESS STROBE         */

/**  Node Declarations **/
pinnode [33..37] = [C0..4];               /* BUILT-IN COUNTER              */
pinnode 39       = SCLR0;                 /* COUNTER HOLD non-registered   */
pinnode 40       = SCLR1;                 /* COUNTER HOLD registered       */
pinnode 41       = CNTHOLD0;              /* COUNTER HOLD non-refistered   */
pinnode 42       = CNTHOLD1;              /* COUNTER HOLD registered       */
node               [P0..1];               /* BURIED STATE REGISTERS        */
node               BRDY;                  /* BURIED READY SIGNAL           */

/** Declarations and Intermediate Variable Definitions **/
field COUNTER    = [C0..4].CNT;
field STATE      = [P1..0];
$define ST0        'b'00
$define ST1        'b'01
$define ST2        'b'10
```

```
sequence STATE {
present ST0:
       /* INITIALIZE AND HOLD */
       if(RESET)                          next ST0;
       if(ALE & MIO & REFREQ & !RESET)    next ST1;
       if(!REFREQ & !RESET)               next ST2;
       default                            next ST0;

present ST1:
       /* ACCESS CYCLE */
       if(RESET)                          next ST0;
       if(COUNTER:'d'0)  & !RESET         next ST1 out !RAS;
       if(COUNTER:'d'1)  & !RESET         next ST1 out  MSEL;
       if(COUNTER:'d'2)  & !RESET         next ST1 out !CAS;
       if(COUNTER:'d'9)  & !RESET         next ST0 out [RAS,!MSEL,CAS];
       default                            next ST1;

present ST2:
       /* REFRESH/ACCESS GRANT CYCLE */
       if(RESET)                          next ST0;
       if(COUNTER:'d'0)  & !RESET         next ST2 out !MC1;
       if(COUNTER:'d'1)  & !RESET         next ST2 out [RFC,!RAS];
       if(COUNTER:'d'3)  & !RESET         next ST2 out  MC1;
       if(COUNTER:'d'5)  & !RESET         next ST2 out !RFC;
       if(COUNTER:'d'6)  & !RESET         next ST2 out  RAS;
       if(COUNTER:'d'9)  &  BRDY          next ST0;
       if(COUNTER:'d'10) & !RESET         next ST2 out !RAS;
       if(COUNTER:'d'11) & !RESET         next ST2 out [BRDY,MSEL];
       if(COUNTER:'d'12) & !RESET         next ST2 out [RDY,!CAS];
       if(COUNTER:'d'19)                  next ST0 out [RAS,!MSEL,CAS];
       default                            next ST2; }

append BRDY.r    = STATE:ST2 & ALE & MIO & !RESET;
append  RDY.r    = STATE:ST2 & ALE & MIO & !RESET;

/* BUILT-IN COUNTER CONTROL EQUATIONS, WRITTEN  */
/* OUTSIDE THE STATE MACHINE FOR CLARITY.       */
SCLR0            = RESET                        /* Clear counter on RESET */
                 # STATE:ST1 & COUNTER:'d'9     /* and transitions to ST0.*/
                 # STATE:ST2 & COUNTER:'d'9 & BRDY
                 # STATE:ST2 & COUNTER:'d'19;
CNTHOLD1.s       = RESET                        /* Set count hold while   */
                 # STATE:ST1 & COUNTER:'d'9     /* clearing the counter.  */
                 # STATE:ST2 & COUNTER:'d'9 & BRDY
                 # STATE:ST2 & COUNTER:'d'19;
CNTHOLD1.r       = STATE:ST0 & ALE & MIO
                            & REFREQ & !RESET  /* Reset count hold       */
                 # STATE:ST0 & !REFREQ & !RESET;/* on transition to ST1,2 */

APPEND BRDY.s  = RESET;  APPEND RAS.s  = RESET;  APPEND P1.r   = RESET;
APPEND RDY.s   = RESET;  APPEND CAS.s  = RESET;  APPEND MSEL.r = RESET;
APPEND MC1.s   = RESET;  APPEND P0.r   = RESET;  APPEND RFC.r  = RESET;

/** End of file **/
```

```
Name     PSG_EX3;
Partno   TI0003;
Date     08/26/87;
Rev      02;
Designer Schiele/Woolhiser;
Company  Texas Instruments/Personnal CAD Systems;
Assembly None;
Location None;

/*************************************************************************/
/*                                                                       */
/* Dynamic Memory Timing Controller                                      */
/*                                                                       */
/* CUPL simulation file for Example 3 from "A Designer's Guide to the    */
/* PSG507".                                                              */
/*************************************************************************/
/*  Allowable Target Device Types :  TI PSG507                           */
/*************************************************************************/

ORDER:  REF_CLK,%4,RESET,%4,ALE,%3,MIO,%4,REFREQ,%9,RDY,%3,
        MC1,%3,RFC,%3,RAS,%3,MSEL,%4,CAS,%3,STATE;

BASE: DECIMAL;

VECTORS:

$msg"     ";
$msg"     ";
$msg"ACCESS TIMING CYCLE ";
$msg"     ";
$msg"     ------------ INPUT -----     ------------ OUTPUT ----------- ";
$msg"     CLK RESET ALE MIO REFREQ     RDY MC1 RFC RAS MSEL CAS STATE  ";
$msg"     ------------------------------------------------------------ ";
/*RESET*/ C    1     X   X   X         H   H   L   H   L   H   "0"
          C    0     0   1   1         H   H   L   H   L   H   "0"
          C    0     1   1   1         H   H   L   H   L   H   "1"
          C    0     X   X   X         H   H   L   L   L   H   "1"
          C    0     X   X   X         H   H   L   L   H   H   "1"
          C    0     X   X   X         H   H   L   L   H   L   "1"
          C    0     X   X   X         H   H   L   L   H   L   "1"
          C    0     X   X   X         H   H   L   L   H   L   "1"
          C    0     X   X   X         H   H   L   L   H   L   "1"
          C    0     X   X   X         H   H   L   L   H   L   "1"
          C    0     X   X   X         H   H   L   L   H   L   "1"
          C    0     X   X   X         H   H   L   L   H   L   "1"
          C    0     X   X   X         H   H   L   H   L   H   "0"
          C    0     0   0   1         H   H   L   H   L   H   "0"

$msg"     ";
$msg"     ";
$msg"REFRESH WITH ACCESS FOLLOWING ";
$msg"     ";
$msg"     ------------ INPUT -----     ------------ OUTPUT ----------- ";
$msg"     CLK RESET ALE MIO REFREQ     RDY MC1 RFC RAS MSEL CAS STATE  ";
$msg"     ------------------------------------------------------------ ";
/*RESET*/ C    1     X   X   X         H   H   L   H   L   H   "0"
          C    0     X   X   0         H   H   L   H   L   H   "2"
          C    0     0   0   X         H   L   L   H   L   H   "2"
          C    0     0   0   X         H   L   H   L   L   H   "2"
          C    0     0   0   X         H   L   H   L   L   H   "2"
          C    0     0   0   X         H   H   H   L   L   H   "2"
```

```
            C    0    1    1    X         L    H    H    L    L    H    "2"
            C    0    X    X    X         L    H    L    L    L    H    "2"
            C    0    X    X    X         L    H    L    H    L    H    "2"
            C    0    X    X    X         L    H    L    H    L    H    "2"
            C    0    X    X    X         L    H    L    H    L    H    "2"
            C    0    X    X    X         L    H    L    H    L    H    "2"
            C    0    X    X    X         L    H    L    L    L    H    "2"
            C    0    X    X    X         L    H    L    L    H    H    "2"
            C    0    0    X    X         H    H    L    L    H    L    "2"
            C    0    0    X    X         H    H    L    L    H    L    "2"
            C    0    0    X    X         H    H    L    L    H    L    "2"
            C    0    0    X    X         H    H    L    L    H    L    "2"
            C    0    0    X    X         H    H    L    L    H    L    "2"
            C    0    0    X    X         H    H    L    L    H    L    "2"
            C    0    0    X    X         H    H    L    L    H    L    "2"
            C    0    0    X    X         H    H    L    H    L    H    "0"

$msg"      ";
$msg"      ";
$msg" REFRESH WITHOUT ACCESS FOLLOWING ";
$msg"      ";
$msg"      ------------ INPUT -----      ------------ OUTPUT ----------- ";
$msg"      CLK RESET ALE MIO REFREQ      RDY MC1 RFC RAS MSEL CAS STATE  ";
$msg"      ------------------------------------------------------------- ";
/*RESET*/  C    1    X    X    X         H    H    L    H    L    H    "0"
            C    0    X    X    0         H    H    L    H    L    H    "2"
            C    0    0    0    X         H    L    L    H    L    H    "2"
            C    0    0    0    X         H    L    H    L    L    H    "2"
            C    0    0    0    X         H    L    H    L    L    H    "2"
            C    0    0    0    X         H    H    H    L    L    H    "2"
            C    0    0    1    X         H    H    H    L    L    H    "2"
            C    0    1    0    X         H    H    L    L    L    H    "2"
            C    0    1    0    X         H    H    L    H    L    H    "2"
            C    0    1    0    X         H    H    L    H    L    H    "2"
            C    0    1    0    X         H    H    L    H    L    H    "2"
            C    0    1    0    X         H    H    L    H    L    H    "0"

$msg"      ";
$msg"      ";
$msg" RESET DURING REFRESH";
$msg"      ";
$msg"      ------------ INPUT -----      ------------ OUTPUT ----------- ";
$msg"      CLK RESET ALE MIO REFREQ      RDY MC1 RFC RAS MSEL CAS STATE  ";
$msg"      ------------------------------------------------------------- ";
/*RESET*/  C    1    X    X    X         H    H    L    H    L    H    "0"
            C    0    X    X    0         H    H    L    H    L    H    "2"
            C    0    0    0    X         H    L    L    H    L    H    "2"
            C    0    0    0    X         H    L    H    L    L    H    "2"
            C    0    0    0    X         H    L    H    L    L    H    "2"
            C    1    X    X    X         H    H    L    H    L    H    "0"
```

Appendix C. PSG507 Fuse Numbers



System Solutions for Static Column Decode

Robert K. Breuninger, Loren Schiele,
and Joshua K. Peprah

TEXAS
INSTRUMENTS

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INTRODUCTION

The new 32-bit microprocessors are capable of addressing 4G bytes of physical memory and typically feature clock frequencies greater than 16 Mhz. However, clock speed alone does not guarantee increased system performance; if the processor must wait for data, then memory bandwidth will be the limiting factor.

This situation exists between today's microprocessors and the access times of affordable DRAMs. One solution to optimizing system performance is to mix and match memory, using lower cost dynamic RAM in conjunction with fast, more expensive static RAM caches. However, this approach is only attractive to high end systems where cost and board space is a less significant factor.

Another approach to improving system performance is to utilize the new accessing modes available on certain 1 meg DRAMs, such as static column decode. This method does not improve system performance as much as caches, but it does involve less hardware, resulting in lower system cost. This approach can also be used in systems already using caches, further improving system performance.

This application note describes the theory of using static column decode and also describes how it might be implemented in a typical system. In addition, it highlights three new products from Texas Instruments. The SN74ALS6300 "Selectable Refresh Timer", the SN74ALS6310 "Static Column Access Detector", and the TIBPSG507 "Programmable Sequence Generator".

STATIC COLUMN DECODE

The TMS4C1027 is a 1,048,576-bit × 1 dynamic RAM featuring static column decode. Static column decode allows high-speed read and write operations by reducing the number of required signal setup, hold, and transition timings. This is achieved by first strobing the row and column addresses in the normal manner by taking $\overline{RAS}$ and $\overline{CAS}$ low. If $\overline{RAS}$ and $\overline{CAS}$ are kept low, new data can be accessed by simply changing the column addresses, assuming the new address is in the same row. If the new address is not in the same row, then a normal access cycle must be performed.

Figure 1 is a timing diagram taken from the TMS4C1027 datasheet showing static column decode mode read cycle timing.

If the assumption is made that the majority of memory references tend to be sequential, which is a similar assumption made when using caches, then it is logical to assume that a large percentage of memory accesses will be within the same row. The trick is how to implement a timing controller which will take full advantage of the static column mode of operation.

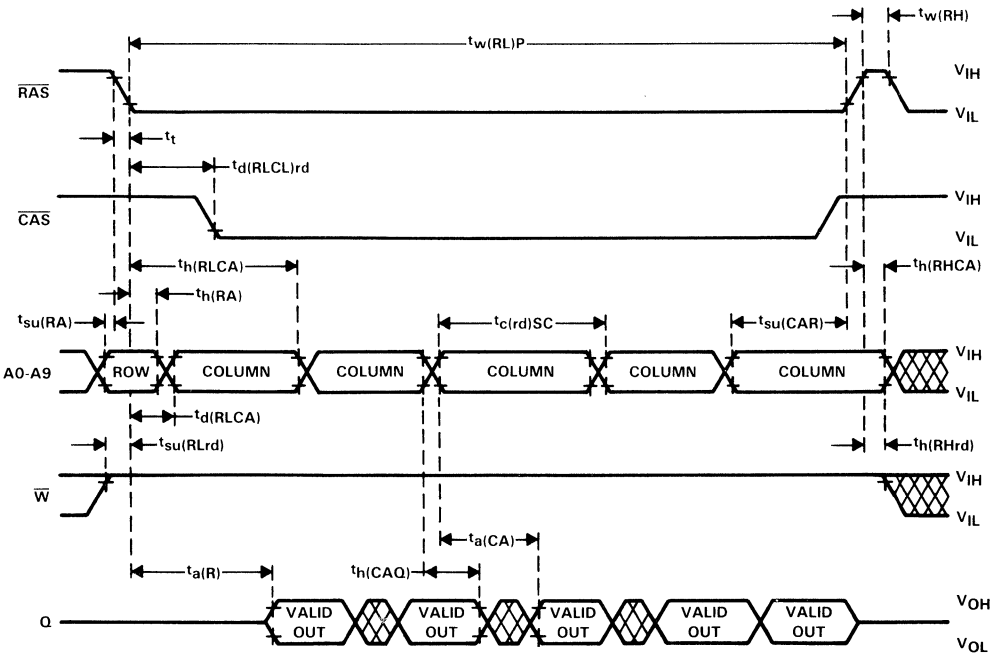

Figure 1. Static Column Decode Mode Read Cycle Timing

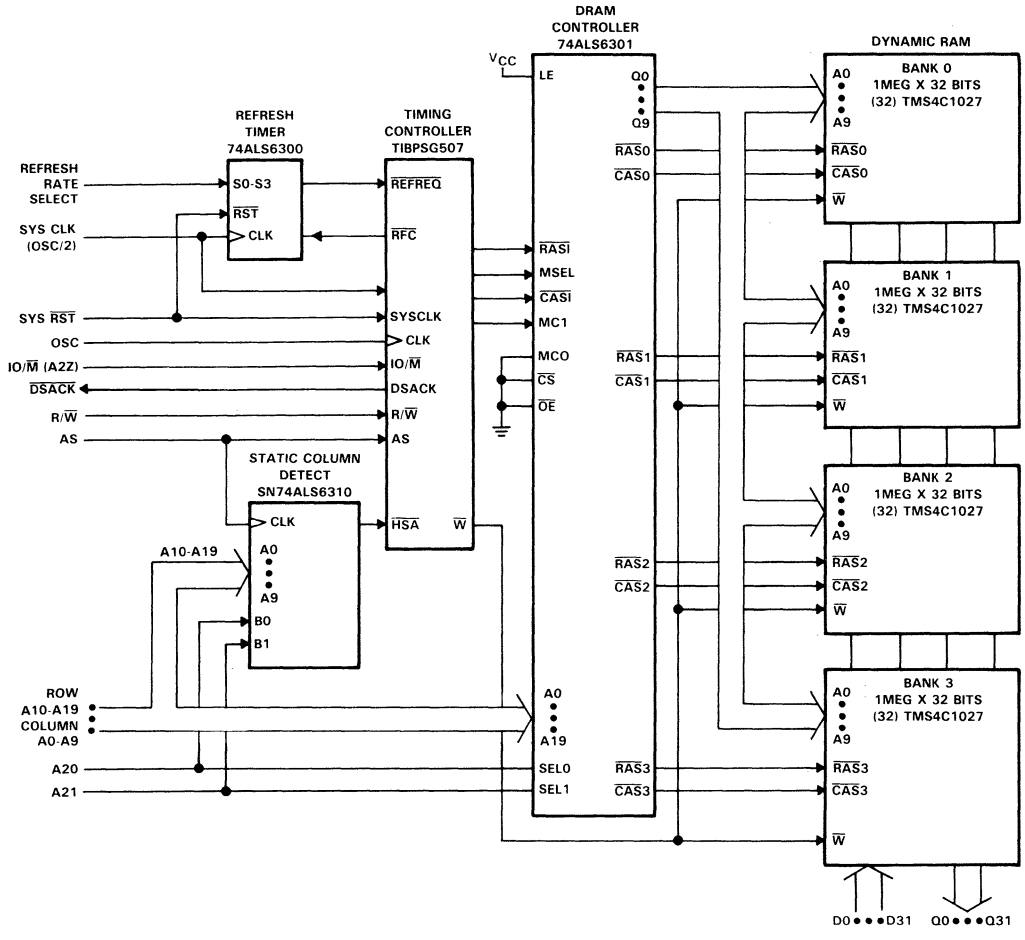

Figure 2. 68020 Static Column Memory Controller

TYPICAL MEMORY CONTROLLER

Figure 2 shows a block diagram of a memory system utilizing static column decode. The ALS6310 is a new circuit offered by Texas Instruments which detects if the present row being accessed is the same as last row accessed. This is the fundamental requirement for implementing static column decode. Note that the row addresses from the 68020 are used as the most significant bits (A10-A19) and the column addresses are used as the least significant bits (A0-A9). Figure 3 shows a block diagram of the ALS6310.

In circuit operation, when address strobe (AS) from the 68020 is taken low, the present row (A10-A19) and bank address (B0, B1) is clocked into the first register of the ALS6310. The previous bank and row address, stored in the first register, is clocked into the second register at the same time. The two addresses are then compared to see if they are equal. If they are equal, the high speed access output ($\overline{HSA}$) will be logically low. If not, $\overline{HSA}$ will be high.

The function of the PSG507 is to generate the required memory timing control signals ($\overline{RAS}$, $\overline{CAS}$, etc.) for the ALS6301 dynamic memory controller. The ALS6301 is responsible for multiplexing row and column addresses into DRAM. The ALS6301 is also capable of driving 4 banks of 1M-byte memory.

Supporting the PSG507 is the ALS6300 refresh timer. This device is responsible for generating a refresh request signal ($\overline{REFREQ}$) every 15.5 μs. The input select lines are hardwired to match the microprocessor clock frequency. The refresh complete input ($\overline{RFC}$), resets the $\overline{REFREQ}$ signal after the timing controller completes the refresh cycle.

TIMING CONTROLLER DETAILS

Figure 4 shows a typical flow chart for implementing static column decode. As stated before, the PSG507 is responsible for implementing the flow chart shown in Figure 4. A breakdown of this flow chart reveals 9 states (ST0-ST8), associated with 5 different sequences. States ST0, ST1, ST3, and ST4 are holding and transition states, leading into the various sequences. The five possible sequences are listed below.

ST2 Normal Access Sequence
ST5 Extended Access Sequence
ST6 High-Speed Access Sequence
ST7 Normal Refresh Sequence
ST8 Extended Refresh Sequence

Notice that the $\overline{HSA}$ signal from the ALS6310 decides if the timing controller will execute ST5, the Extended Access Sequence, or ST6, the High-Speed Access Sequence. A brief description of each sequence follows.

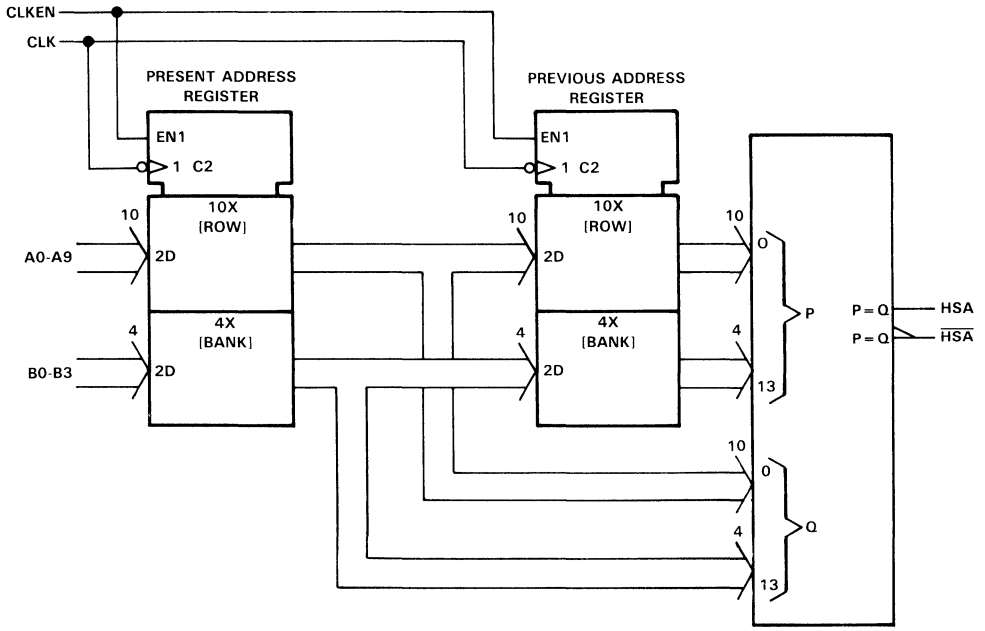

Figure 3. ALS6310 Static Column Page Mode Access Detector

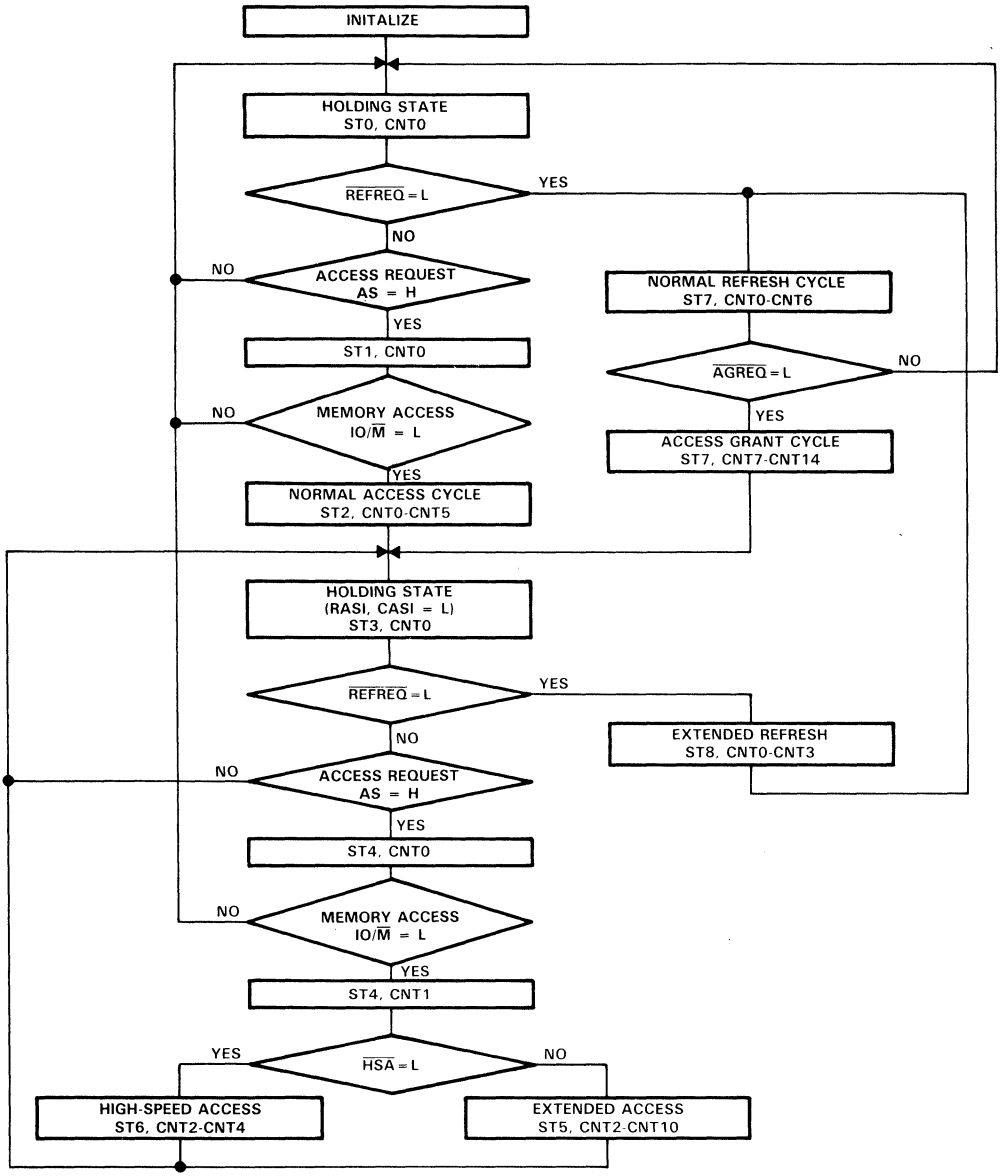

Figure 4. Timing Controller Flowchart

NORMAL ACCESS SEQUENCE

The normal access sequence is shown in Figure 5. This sequence begins by executing a normal $\overline{RAS}/\overline{CAS}$ cycle. Notice that a wait state of one clock cycle is needed to guarantee that data is valid for the 68020. This is the problem mentioned in the introduction; if all access cycles had to be performed in this manner, then the processor would face a wait state every access cycle. As will be shown later, this wait state can be eliminated if the next address is from the same row.

Notice also, at the end of this sequence, the $\overline{RAS}$ and $\overline{CAS}$ output signals are left active low. Here we are making the assumption that the next access cycle will be a high-speed access. We will not know if this assumption is true until the next address is presented by the 68020. At that time, the ALS6310 will signal the timing controller if it can execute a high-speed access.

HIGH-SPEED ACCESS SEQUENCE

For a high-speed access sequence to be executed, two conditions must be met. The $\overline{RAS}$ and $\overline{CAS}$ inputs must already be low, and secondly, the static column access detector must be indicating the present row is the same as the last row ($\overline{HSA}$ = L). The bank addresses must also be unchanged as detected by the ALS6310.

Figure 6 shows the timing diagram for the high-speed access sequence. Notice that no wait states are required. If the assumption is made that the majority of memory references are sequential, then this sequence will be the one typically used. In other words, this sequence is similar to accessing data from a static RAM, or just like taking data from cache.

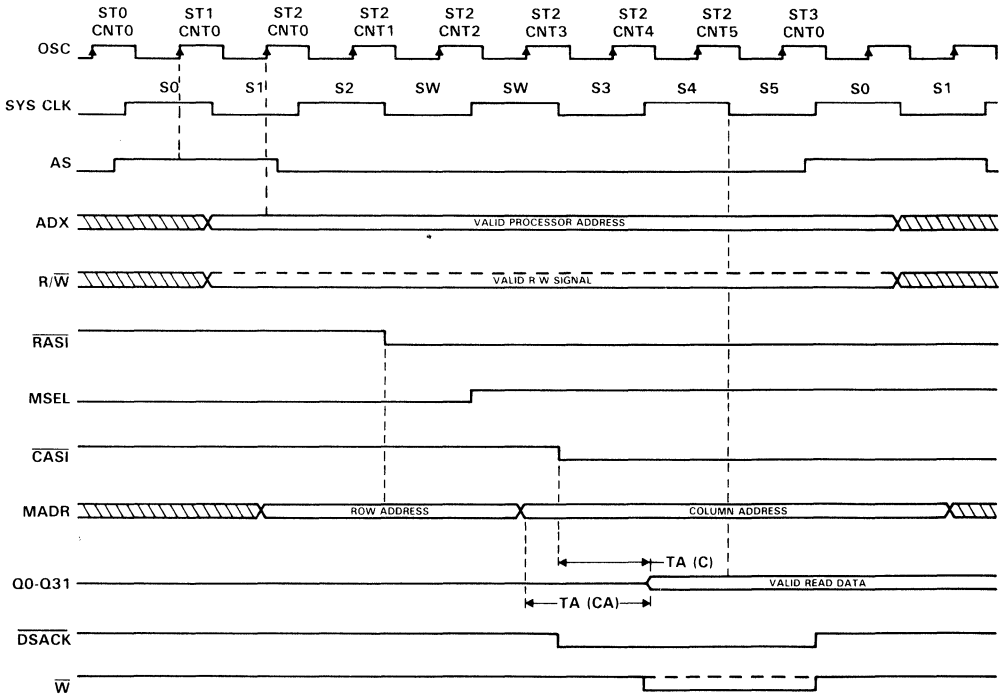

Figure 5. Normal Access Cycle

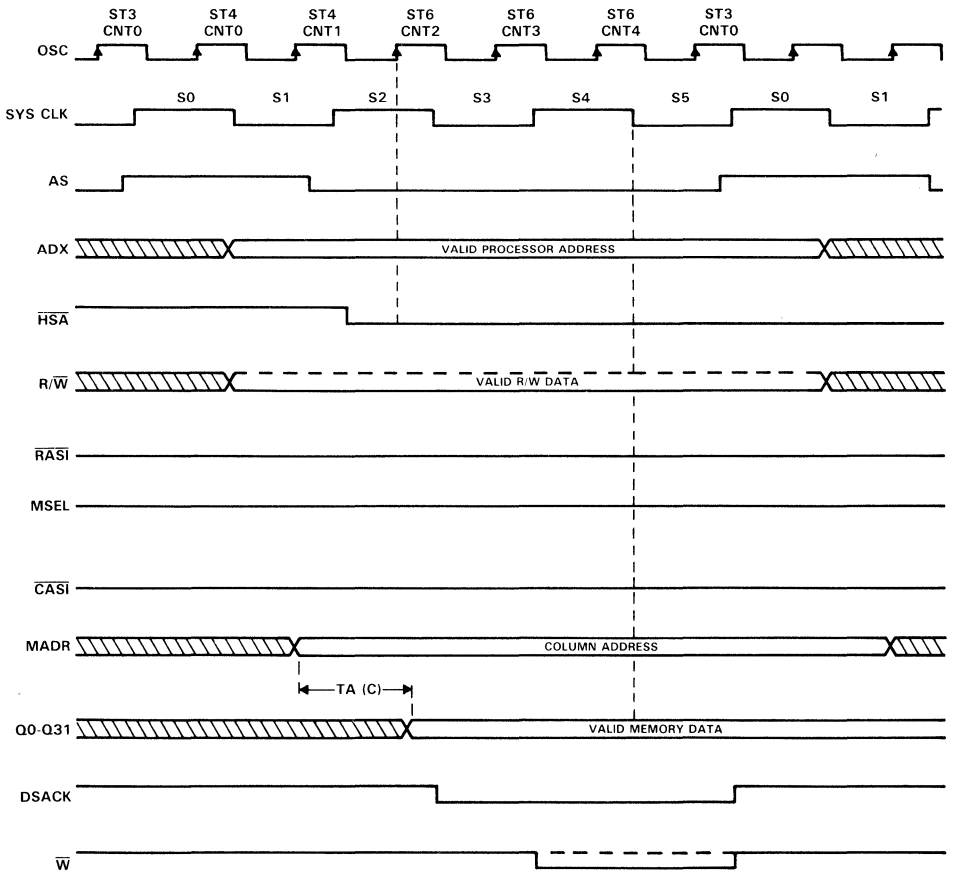

Figure 6. High-Speed Access Cycle

EXTENDED ACCESS SEQUENCE

The extended access sequence is executed if the ALS6310 detects a difference between the present, and last row addresses.. This cycle is called extended because $\overline{RAS}$ and $\overline{CAS}$ are presently low and both must be brought high to strobe in the new row and column addresses. The precharge time of the DRAM has to be met before taking $\overline{RAS}$ and $\overline{CAS}$ low. From the timing diagram in Figure 7, it can be seen that wait states of three clock cycles are generated when executing this timing sequence.

In systems where sequential data is not the general rule, it would be more efficient to execute only normal access sequences, since this generates fewer wait states. The system designer must understand what type of memory accesses will be used. For example, the designer may want only to enter the high-speed access portion of the flow chart when the system is performing DMA access cycles.

NORMAL/EXTENDED REFRESH SEQUENCES

Figures 8 and 9 show the timing diagrams for the normal and extended refresh sequences. The refresh sequence selected is a function of the present condition of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ and $\overline{CAS}$ are presently low, an extended refresh cycle is performed. If $\overline{RAS}$ and $\overline{CAS}$ are presently high, a normal refresh cycle is executed. At the end of each refresh sequence, the controller checks to see if an access request has been generated. If there has been an access request, the controller will perform an access grant sequence at the end of the refresh cycle before returning to normal process flow.

Referring back to Figure 1, there is a maximum time that $\overline{RAS}$ and $\overline{CAS}$ can be held low, $t_W(RL)P$. For the TMS4C1027, $t_W(RL)P$ must not exceed 100 μs. Since our refresh timer forces a refresh cycle every 15.5 μs, $t_W(RL)P$ cannot be violated. If the designer chooses to use a different refresh scheme, then $t_W(RL)P$ must be considered.

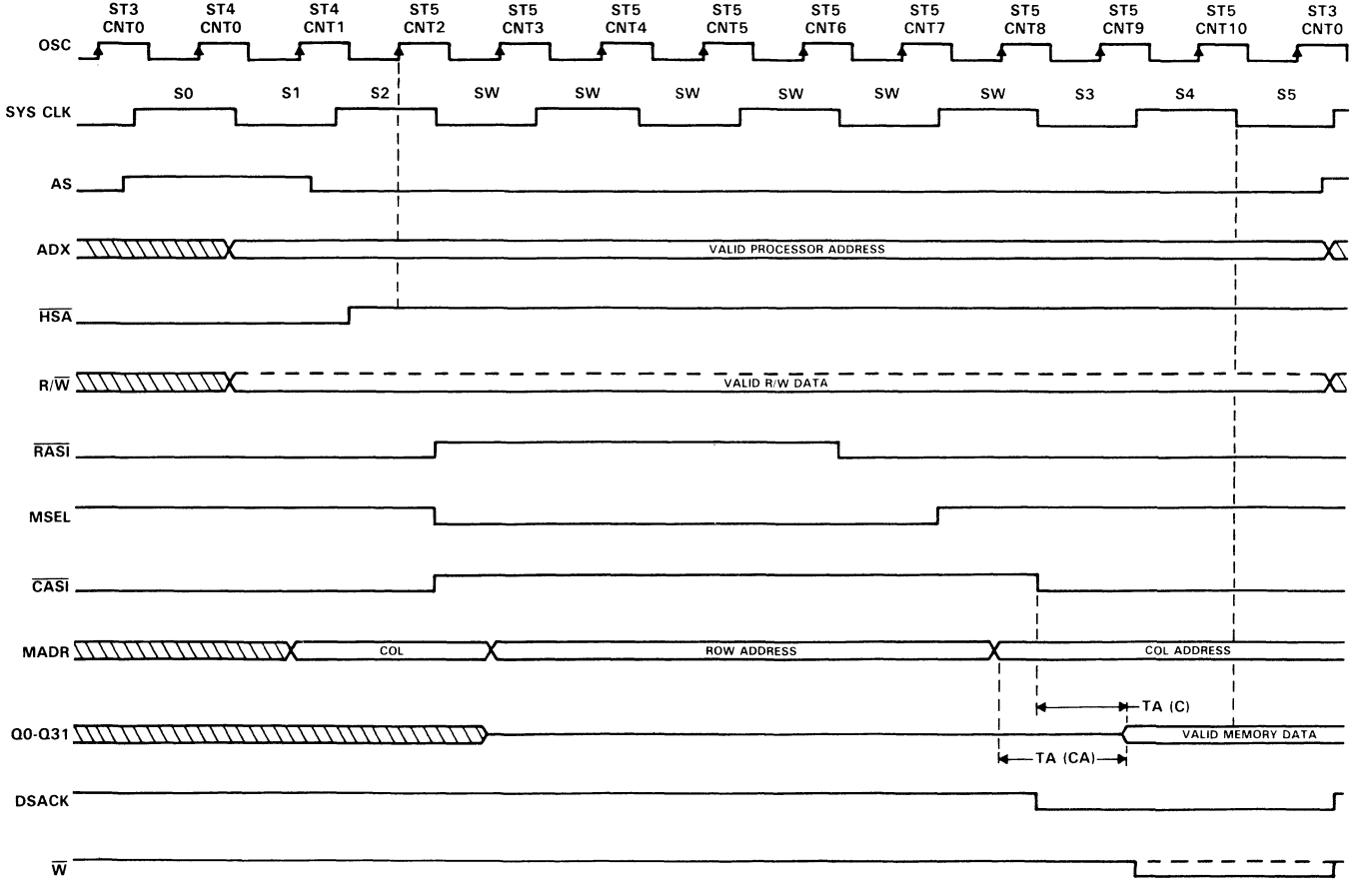

Figure 7. Extended Access Cycle

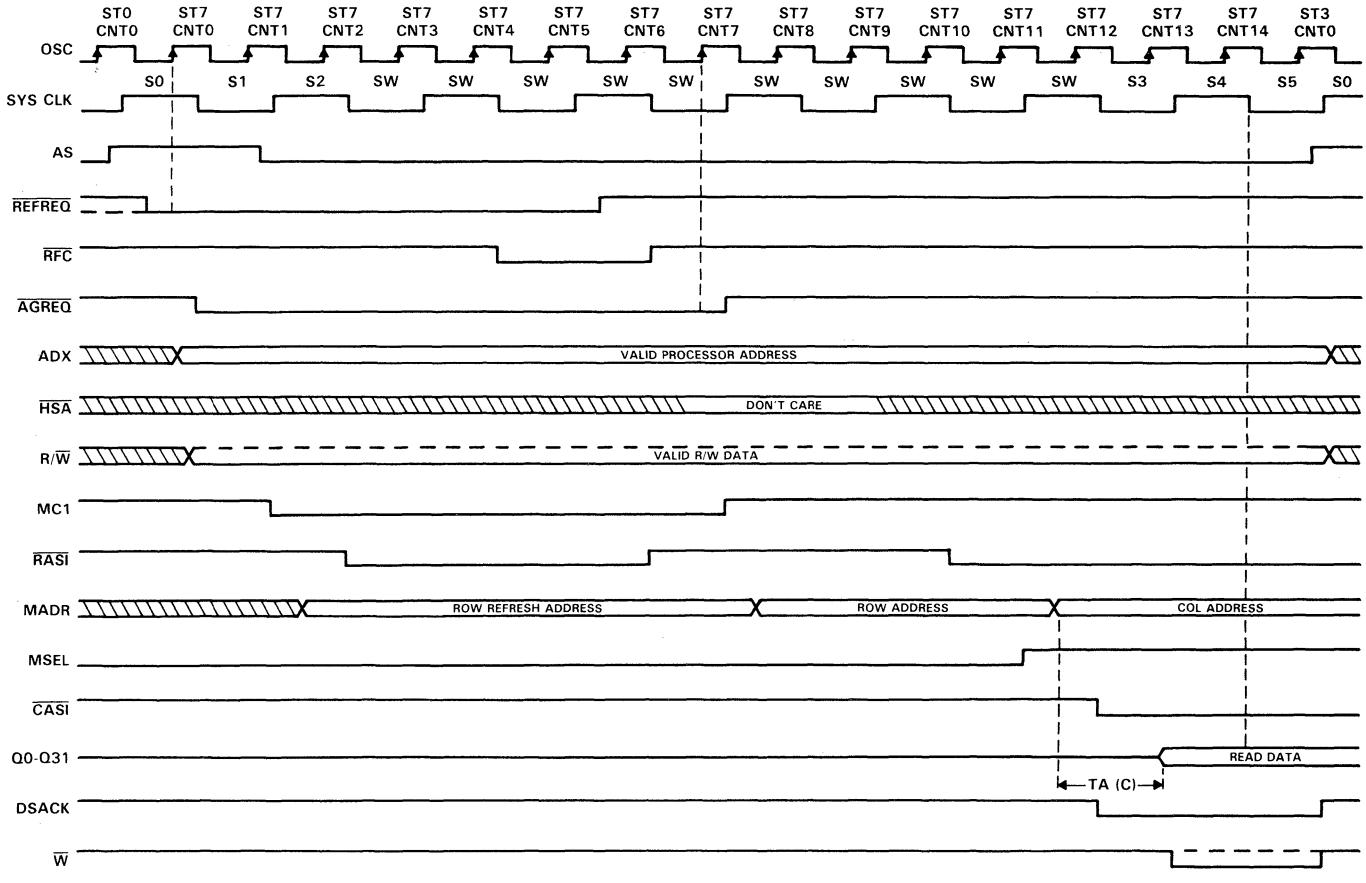

Figure 8. Normal Refresh/Access Grant Cycle

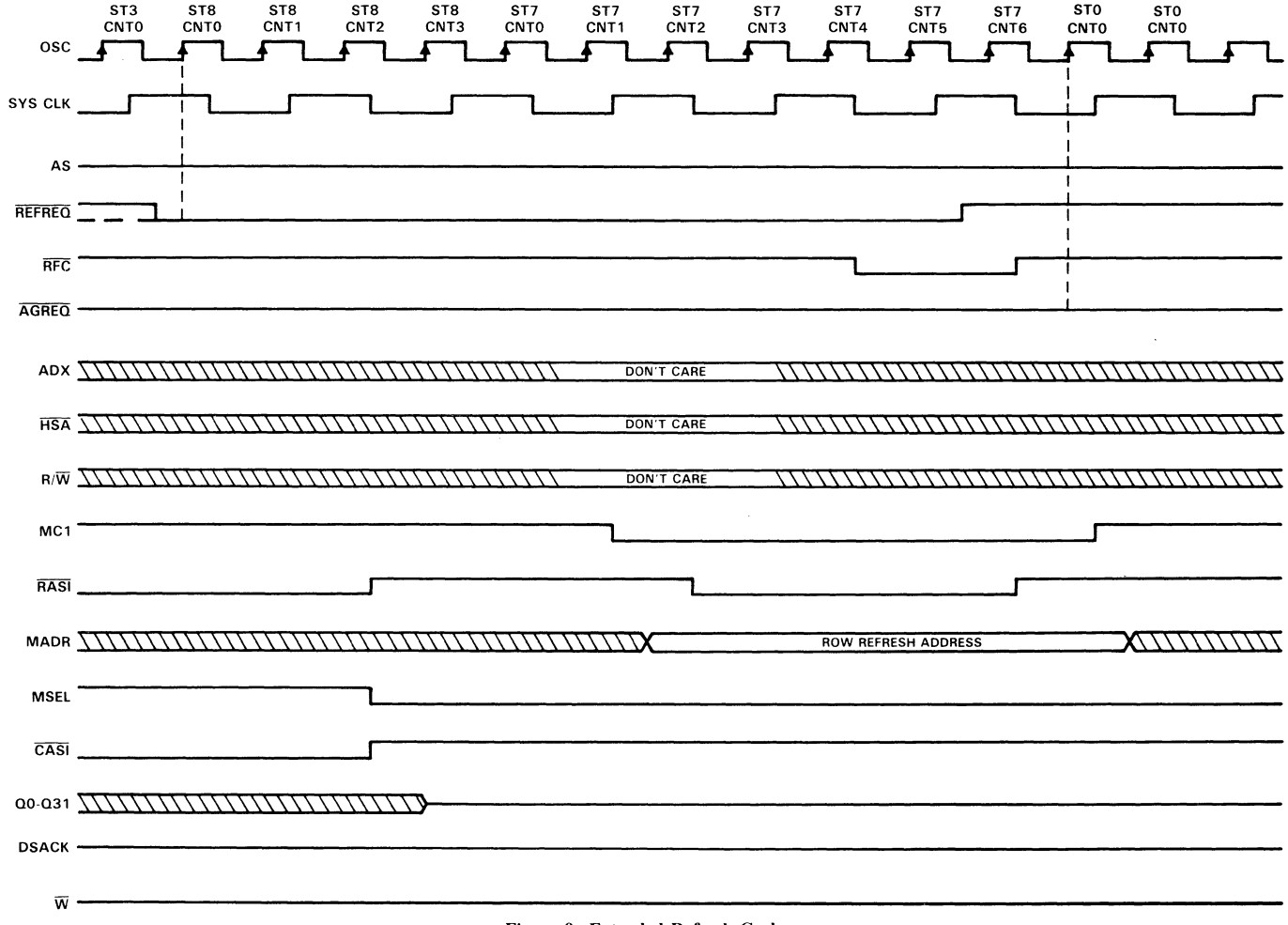

Figure 9. Extended Refresh Cycle

SOFTWARE SUPPORT

The PSG507 is supported by two software packages. CUPL which was created by and is supported by Assisted Technologies, a division of Personal CAD Systems Inc. and ABEL which was created by and is supported by FutureNet a division of Data I/O Corp. Both of these software packages have been used to reduce equations and to generate the fusemap necessary to program the PSG507. Appendices A and B show the ABEL™ and CUPL™ source files for the described static column memory timing controller are attached to assist the designer in programming the PSG507.

Since only 54% (43 out of 80) of the PG507's product terms were used in this design, it will be easy to modify or add to the sequences used to meet specific system requirements. For detailed information on designing with the PSG507 see "A Designer's Guide to the PSG507" application report.

SUMMARY

Static column decode offers the system designer a method for improving system performance in applications where the microprocessor can outperform conventional DRAM access times. By utilizing the ALS6310 "Static Column Access Detector", the ALS6300 "Refresh Timer", and the TIBPSG507 "Programmable Sequence Generator" a high performance memory timing controller can be easily developed to take full advantage of static column decode.

APPENDIX A

```
module SCDECODE
title  'ABEL EXAMPLE FOR THE STATIC COLUMN DECODER
               JOSH PEPRAH, TEXAS INSTRUMENTS, OCT 29, 1987'

      DECODE device 'F507';

" Input pin assignments
OSC           pin   1;                        " OSCILLATOR
RESET         pin   2;                        " SYSTEM RESET - WHEN LOW
A22           pin   3;                        " IO/MEMORY - MEMORY ACCESS
RW            pin   4;                        " READ / WRITE ENABLE
REFREQ        pin   5;                        " REFRESH REQUEST
AS            pin   6;                        " ADDR STROBE - ACCESS REQ
HSA           pin   7;                        " HIGH SPEED ACCESS
SYSCLK        pin  17;                        " SYSTEM CLOCK - (OSC/2)

" Output pin and node assignments
RFC           pin   8;  RFC_r    node 47;   " REFRESH COMPLETE
RASI          pin   9;  RASI_r   node 48;   " ROW ADDRESS STROBE
MSEL          pin  10;  MSEL_r   node 49;   " MULTIPLEXER SELECT
CASI          pin  11;  CASI_r   node 50;   " COLUMN ADDRESS STROBE
MC1           pin  13;  MC1_r    node 51;   " MODE CONTROL
W             pin  14;  W_r                 node 52;   " WRITE
DSACK         pin  15;  DSACK_r  node 53;   " DATA STROBE ACKNOWLEDGE


" Internal counter bits & control, and state reg - node declarations
C0,C1,C2,C3,C4,C5  node 55,56,57,58,59,60;
SCLR0         node 25;
CNTHOLD0 node 28;
CNTHOLD1 node 29;  CNTHOLD1_r node 30; " COUNT/HOLD CONTROL REGISTER

" Buried state registers - node declarations

P0     node 31;  P0_r      node 39;       " STATE REGISTER
P1     node 32;  P1_r      node 40;       " STATE REGISTER
P2     node 33;  P2_r      node 41;       " STATE REGISTER
P3     node 34;  P3_r      node 42;       " STATE REGISTER
AGREQ  node 35; AGREQ_r node 43;       " ACCESS GRANT REQUEST STATUS REGISTER

" Set notation is used to represent control, buried state, and output
" registers. This is done to simplify the equations.  The following
" sets are in the form;  register name_ = [set input, reset input]. Note
" that the ouput register pin name specifies the set input.

RFC_              = [RFC, RFC_r];
RASI_             = [RASI, RASI_r];
MSEL_             = [MSEL, MSEL_r];
CASI_             = [CASI, CASI_r];
MC1_              = [MC1, MC1_r];
W_                = [W, W_r];
DSACK_            = [DSACK, DSACK_r];
AGREQ_            = [AGREQ, AGREQ_r];
```

```
" Intermediate declarations for simplification.
" The sets 'high' and 'low' are used to set or reset the S/R
" registers.  Example: RASI_ := high & RESET; will cause pin 9
" to go high on the next clock edge if input pin 6 is high.

high            = [ 1,  0];
low             = [ 0,  1];
COUNT           = [C3,C2,C1,C0];
STATE_          = [P3,P2,P1,P0];              " STATE REGISTER SET DEFINED
H,L,clk,X   = 1, 0, .C., .X.;

equations

enable RFC  = 1;  "outputs always enabled, pin 17 is only an input

" Initialization when RESET is low
    [RASI,CASI,RFC,W,AGREQ,DSACK,MC1,SCLR0] := !RESET;
    [MSEL_r,P0_r,P1_r,P2_r,P3_r]            := !RESET;

" Counter controls defined

SCLR0           =  !RESET
                  # (STATE_==2) & (COUNT==5)
                  # (STATE_==4) & (COUNT==0) & A22
                  # (STATE_==5) & (COUNT==10)
                  # (STATE_==6) & (COUNT==4)
                  # (STATE_==7) & (COUNT==6) & (A22 # AGREQ)
                  # (STATE_==7) & (COUNT==14)
                  # (STATE_==8) & (COUNT==3);

CNTHOLD1   :=  !RESET
                  # (STATE_==2) & (COUNT==5)
                  # (STATE_==4) & (COUNT==0) & A22
                  # (STATE_==5) & (COUNT==10)
                  # (STATE_==6) & (COUNT==4)
                  # (STATE_==7) & (COUNT==6) & (A22 # AGREQ)
                  # (STATE_==7) & (COUNT==14)
                  # (STATE_==8) & (COUNT==3);

CNTHOLD1_r := (STATE_==0) & !REFREQ & RESET
                  # (STATE_==1) & !A22 & RESET
                  # (STATE_==3) & !REFREQ & RESET
                  # (STATE_==3) &  REFREQ &  AS & SYSCLK & RESET;

" Execution of access and refresh sequences
state_diagram STATE_
   State 0:                                                          " NEXT
                                  case                                " STATE
                                   !RESET                                      : 0;
                                    REFREQ & (!AS  # !SYSCLK)          : 0;
                                    REFREQ &  AS & SYSCLK & RESET      : 1;
                                   !REFREQ &  RESET                            : 7;
                                  endcase;
```

```
" NORMAL ACCESS CYCLE

   State 1:                                                    " NEXT
                                 case                          " STATE
                                   (COUNT==0) & !A22          : 2;
                                   (COUNT==0) &  A22          : 0;
                                 endcase;

   State 2:
                                 RASI_ := (COUNT==0)  & low  & RESET;
                                 MSEL_ := (COUNT==1)  & high;
                                 CASI_ := (COUNT==2)  & low  & RESET;
                                DSACK_ := (COUNT==2)  & low  & RESET;
                                   W_  := (COUNT==3)  & low  & RESET;
                                   W_  := (COUNT==5)  & high;
                                DSACK_ := (COUNT==5)  & high;
                               if (COUNT==5) then 3 else 2;

"HOLDING STATE
   State 3:                                                    " NEXT
                                 case                          " STATE
                               (!AS # !SYSCLK) & REFREQ & RESET      : 3;
                                 REFREQ &  AS & SYSCLK & RESET       : 4;
                                !REFREQ & RESET                                : 8;
                                 endcase;

   State 4:
                                CASI_  := (COUNT==0)  &  high &  A22;
                                RASI_  := (COUNT==0)  &  high &  A22;
                                MSEL_  := (COUNT==0)  &  low  &  A22;
                                RASI_  := (COUNT==1)  &  high &  HSA;
                                DSACK_ := (COUNT==1)  &  low  & !HSA;
                                MSEL_  := (COUNT==1)  &  low  &  HSA;
                                CASI_  := (COUNT==1)  &  high &  HSA;

                                                                          " NEXT
                                 case                          " STATE
                                   (COUNT==0) &  A22  & RESET        : 0;
                                   (COUNT==0) & !A22  & RESET        : 4;
                                   (COUNT==1) &  HSA  & RESET        : 5;
                                   (COUNT==1) & !HSA  & RESET        : 6;
                                 endcase;

"EXTENDED ACCESS CYCLE
   State 5:
                                 RASI_ := (COUNT==5)  & low & RESET;
                                 MSEL_ := (COUNT==6)  & high & RESET;
                                 CASI_ := (COUNT==7)  & low & RESET;
                                DSACK_ := (COUNT==7)  & low & RESET;
                                         W_ := (COUNT==8)  & low & RESET;
                                         W_ := (COUNT==10) & high;
                                DSACK_ := (COUNT==10) & high;
                                   if (COUNT==10) & RESET then 3 else 5;
```

```
"HIGH SPEED ACCESS
   State 6:
                                    W_ := (COUNT==2)  & low & RESET;
                                    W_ := (COUNT==4)  & high;
                                DSACK_ := (COUNT==4)  & high;
                                   if (COUNT==4) then 3 else 6;

"NORMAL REFRESH CYCLE
   State 7:
                                AGREQ_ := AS            & low  & RESET;
                                 MC1_ := (COUNT==0)  & low  & RESET;
                                RASI_ := (COUNT==1)  & low  & RESET;
                                 RFC_ := (COUNT==3)  & low  & RESET;
                                 RFC_ := (COUNT==5)  & high;
                                RASI_ := (COUNT==5)  & high;
                                 MC1_ := (COUNT==6)  & high;
                                RASI_ := (COUNT==9)  & low  & RESET;
                                MSEL_ := (COUNT==10) & high & RESET;
                                CASI_ := (COUNT==11) & low  & RESET;
                                DSACK_ := (COUNT==11) & low  & RESET;
                                    W_ := (COUNT==12) & low  & RESET;
                                    W_ := (COUNT==14) & high;
                                DSACK_ := (COUNT==14) & high;
                                if (COUNT==6) & (A22 # AGREQ) then 0 else 7;
                                if (COUNT==14) then 3 else 7;

"EXTENDED REFRESH CYCLE
   State 8:
                                 RASI_ := (COUNT==1)  & high;
                                 MSEL_ := (COUNT==1)  & low ;
                                 CASI_ := (COUNT==1)  & high;
                                 if (COUNT==3) then 7 else 8;


test_vectors  'NORMAL ACCESS CYCLE'

([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       L , X , X,  X            , X, X ,   X  ,  X  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0      ];
 [clk,       H , X , X,  H            , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0      ];
 [clk,       H , X , X,  H            , H, X ,   H  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  1      ];
 [clk,       H , L , X,  X            , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  2      ];
 [clk,       H , X , X,  X            , X, X ,   X  ,  0  ] -> [ H ,  L ,  L ,  H , H ,H,  H  ,  2      ];
 [clk,       H , X , X,  X            , X, X ,   X  ,  1  ] -> [ H ,  L ,  H ,  H , H ,H,  H  ,  2      ];
 [clk,       H , X , X,  X            , X, X ,   X  ,  2  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  2      ];
 [clk,       H , X , X,  X            , X, X ,   X  ,  3  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  2      ];
 [clk,       H , X , X,  X            , X, X ,   X  ,  4  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  2      ];
 [clk,       H , X , X,  X            , X, X ,   X  ,  5  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3      ];

test_vectors  'HOLDING STATE 4 WITH EXTENDED ACCESS REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , H , X,  H            , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4      ];
 [clk,       H , L , X,  X            , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4      ];
 [clk,       H , X , X,  X            , X, H ,   X  ,  1  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5      ];
```

```
test_vectors  'EXTENDED ACCESS'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , X , X,  X              , X, X ,   X  ,  2  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  3  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  4  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  5  ] -> [ H ,  L ,  L ,  H , H ,H,  H  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  6  ] -> [ H ,  L ,  H ,  H , H ,H,  H  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  7  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  8  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  9  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  5       ];
 [clk,       H , X , X,  X              , X, X ,   X  , 10  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3       ];

test_vectors  'HOLDING STATE 4 WITH HIGH SPEED ACCESS REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , H , X,  H              , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4       ];
 [clk,       H , L , X,  X              , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4       ];
 [clk,       H , L , X,  X              , X, L ,   X  ,  1  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  6       ];

test_vectors  'HIGH SPEED ACCESS'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , X , X,  X              , X, X ,   X  ,  2  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  6       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  3  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  6       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  4  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3       ];

test_vectors  'NON-MEMORY ACCESS FOLLOWED BY REFRESH REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , H , X,  H              , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4       ];
 [clk,       H , H , X,  X              , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0       ];
 [clk,       H , X , X,  H              , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0       ];
 [clk,       H , X , X,  H              , X, X ,   L  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0       ];
 [clk,       H , X , X,  L              , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7       ];

test_vectors  'NORMAL REFRESH CYCLE'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , X , X,  X              , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  X              , L, X ,   X  ,  1  ] -> [ H ,  L ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  X              , L, X ,   X  ,  2  ] -> [ H ,  L ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  X              , L, X ,   X  ,  3  ] -> [ L ,  L ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  X              , L, X ,   X  ,  4  ] -> [ L ,  L ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  H              , L, X ,   X  ,  5  ] -> [ H ,  H ,  L ,  H , L ,H,  H  ,  7       ];
 [clk,       H , X , X,  X              , L, X ,   X  ,  6  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0       ];
```

```
test_vectors  'NORMAL REFRESH CYCLE FOLLOWED BY ACCESS GRANT REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
[clk,  H , X , X,  L      , X, X ,   X  ,  0  ] -> [ H ,          H ,  L ,  H , H ,H,  H     ,  7   ];
[clk,  H , X , X,  X      , L, X ,   X  ,  0  ] -> [ H ,          H ,  L ,  H , L ,H,  H     ,  7   ];
[clk,  H , X , X,  X      , L, X ,   X  ,  1  ] -> [ H ,          L ,  L ,  H , L ,H,  H     ,  7   ];
[clk,  H , X , X,  X      , H, X ,   X  ,  2  ] -> [ H ,          L ,  L ,  H , L ,H,  H     ,  7   ];
[clk,  H , X , X,  X      , H, X ,   X  ,  3  ] -> [ L ,          L ,  L ,  H , L ,H,  H     ,  7   ];
[clk,  H , X , X,  X      , L, X ,   X  ,  4  ] -> [ L ,          L ,  L ,  H , L ,H,  H     ,  7   ];
[clk,  H , L , X,  H      , L, X ,   X  ,  5  ] -> [ H ,          H ,  L ,  H , L ,H,  H     ,  7   ];
[clk,  H , L , X,  X      , L, X ,   X  ,  6  ] -> [ H ,          H ,  L ,  H , H ,H,  H     ,  7   ];
[clk,  H , L , X,  X      , L, X ,   X  ,  7  ] -> [ H ,          H ,  L ,  H , H ,H,  H     ,  7   ];
[clk,  H , L , X,  X      , L, X ,   X  ,  8  ] -> [ H ,          H ,  L ,  H , H ,H,  H     ,  7   ];
[clk,  H , L , X,  X      , L, X ,   X  ,  9  ] -> [ H ,          L ,  L ,  H , H ,H,  H     ,  7   ];
[clk,  H , L , X,  X      , L, X ,   X  , 10  ] -> [ H ,          L ,  H ,  H , H ,H,  H     ,  7   ];
[clk,  H , L , X,  X      , L, X ,   X  , 11  ] -> [ H ,          L ,  H ,  L , H ,H,  L     ,  7   ];
[clk,  H , L , X,  X      , L, X ,   X  , 12  ] -> [ H ,          L ,  H ,  L , H ,L,  L     ,  7   ];
[clk,  H , L , X,  X      , L, X ,   X  , 13  ] -> [ H ,          L ,  H ,  L , H ,L,  L     ,  7   ];
[clk,  H , L , X,  X      , L, X ,   X  , 14  ] -> [ H ,          L ,  H ,  L , H ,H,  H     ,  3   ];

test_vectors  'HOLDING STATE 3 WITH EXTENDED REFRESH REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H  , X , X,  H            , X, X ,   L  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3   ];
 [clk,       H  , X , X,  H            , L, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3   ];
 [clk,       H  , X , X,  L            , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  8   ];

test_vectors  'EXTENDED REFRESH CYCLE'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H  , X , X,  X            , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  8   ];
 [clk,       H  , X , X,  X            , X, X ,   X  ,  1  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  8   ];
 [clk,       H  , X , X,  X            , X, X ,   X  ,  2  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  8   ];
 [clk,       H  , X , X,  X            , X, X ,   X  ,  3  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7   ];


end SCDECODE
```

APPENDIX B

```
NAME      SCDECODE;
PARTNO    TI0004;
DATE      05/07/87 ;
REV       01 ;
DESIGNER  Breuninger/Peprah;
COMPANY   Texas Instruments;
ASSEMBLY  None ;
LOCATION  Dallas;

/*****************************************************************************/
/*   Static Column Decode                                                    */
/*                                                                           */
/*                                                                           */
/*        This is an example of how the PSG507 can be used to generate the   */
/*   required memory timing control signals (RAS, CAS, MSEL etc) for static  */
/*   column decode implementation using the ALS6301, ALS6310 and the ALS630   */
/*   ALS6300, in a system environment.                                       */
/*                                                                           */
/*                                                                           */
/*****************************************************************************/
/*   Allowable Target Device Types :  TEXAS INTSRUMENTS  PSG507              */
/*****************************************************************************/

/**  Inputs  **/

pin  1          =  OSC      ;          /* Oscillator                        */
pin  2          =  RESET    ;          /* System Reset - when low           */
pin  3          =  A22      ;          /* IO/!M - Memory access             */
pin  4          =  RW       ;          /* Read / Write  Enable              */
pin  5          =  REFREQ   ;          /* Refresh Request                   */
pin  6          =  AS       ;          /* Addr Strobe - access request      */
pin  7          =  HSA      ;          /* High Speed Access                 */
pin 18          =  SYSCLK   ;          /* System Clock - (OSC/2)            */

/**  Outputs  **/

pin  8          =  RFC      ;          /* Refresh Complete                  */
pin  9          =  RAS1     ;          /* Row Address Strobe                */
pin 10          =  MSEL     ;          /* Multiplexer Select                */
pin 11          =  CAS1     ;          /* Column Address Strobe             */
pin 13          =  MC1_     ;          /* Mode Control                      */
pin 14          =  W        ;          /* Write                             */
pin 15          =  DSACK    ;          /* Data Strobe Acknowledge           */

/** Node Declarations **/
pinnode [33..38] = [C0..5]  ;          /* Built-in 6-Bit counter            */
pinnode 39       = SCLR0    ;          /* Counter Cclear- non registered    */
pinnode 41       = CNTHOLD0 ;          /* Counter Hold - non registered     */
pinnode 42       = CNTHOLD1 ;          /* Counter Hold - registered         */
node               [P3..0]  ;          /* Buried State Registers            */
node               AGREQ    ;          /* Access Grant Request              */
```

```
/** Declarations and Intermediate Variable Definition **/
field COUNT      = [C5..0]   ;
field STATE      = [P3..0]   ;
$define ST0        'b'0000
$define ST1        'b'0001
$define ST2        'b'0010
$define ST3        'b'0011
$define ST4        'b'0100
$define ST5        'b'0101
$define ST6        'b'0110
$define ST7        'b'0111
$define ST8        'b'1000

/* BUILT-IN COUNTER CONTROL EQUATIONS */

SCLR0        = !RESET                          /* Clear counter when RESET is low        */
             # ST2 & COUNT:'d'5                 /* and during transitions at the end      */
             # ST4 & COUNT:'d'0                 /* the indicated states and counts.       */
             # ST5 & COUNT:'d'10                /*                                        */
             # ST6 & COUNT:'d'4                 /*                                        */
             # ST7 & COUNT:'d'6 & (A22 & AGREQ) /*                                        */
             # ST7 & COUNT:'d'14                /*                                        */
             # ST8 & COUNT:'d'3;                /*                                        */

CNTHOLD1.s   = !RESET                          /* Set count hold while clearing          */
             # ST2 & COUNT:'d'5                 /* the counters accordingly.              */
             # ST4 & COUNT:'d'0                 /*                                        */
             # ST5 & COUNT:'d'10                /*                                        */
             # ST6 & COUNT:'d'4                 /*                                        */
             # ST7 & COUNT:'d'6 & (A22 & AGREQ) /*                                        */
             # ST7 & COUNT:'d'14                /*                                        */
             # ST8 & COUNT:'d'3;                /*                                        */

 CNTHOLD1.r  = ST0 & !REFREQ & RESET            /* Reset count hold on transition to ST7  */
             # ST1 & !A22 & RESET               /* Reset count hold on transition to ST2  */
             # ST3 & !REFREQ & RESET            /* Reset count hold on transition to ST8  */
             # ST3 &  REFREQ &  AS              /* Reset count hold on transition to ST4  */
                  & SYSCLK & RESET;

/** State Machine Equations **/
sequence STATE {
present ST0:
        if(REFREQ & (!AS  # !SYSCLK))       next ST0;
        if(REFREQ &  AS & SYSCLK & RESET)   next ST1;
        if(!REFREQ &  RESET)                next ST7;
        default                             next ST0;

present ST1:
        if(COUNT:'d'0 & !A22)               next ST2;
        if(COUNT:'d'0 &  A22)               next ST0;
        default                             next ST1;

present ST2:
        /* NORMAL ACCESS CYCLE */
        if(COUNT:'d'0) &  RESET             next ST2 out !RAS1;
        if(COUNT:'d'1)                      next ST2 out  MSEL;
        if(COUNT:'d'2) & RESET              next ST2 out [!CAS1,!DSACK];
        if(COUNT:'d'3) & RESET              next ST2 out !W;
        if(COUNT:'d'5)                      next ST3 out [W,DSACK];
        default                             next ST2;
```

```
present ST3:
        /* HOLDING STATE    */
        if(!AS # !SYSCLK) & REFREQ & RESET   next ST3;
        if(REFREQ &  AS & SYSCLK & RESET)    next ST4;
        if(!REFREQ & RESET)                  next ST8;
        default                              next ST3;

present ST4:
        if(COUNT:'d'0) & A22 & RESET         next ST0 out [RASI,!MSEL,CASI];
        if(COUNT:'d'0) & !A22 & RESET        next ST4;
        if(COUNT:'d'1) & HSA & RESET         next ST5 out [RASI,!MSEL,CASI];
        if(COUNT:'d'1) & !HSA & RESET        next ST6 out !DSACK;
        default                              next ST4;

present ST5:
        /* EXTENDED ACCESS CYCLE */
        if(COUNT:'d'5) & RESET               next ST5 out !RASI;
        if(COUNT:'d'6) & RESET               next ST5 out  MSEL;
        if(COUNT:'d'7) & RESET               next ST5 out [!CASI,!DSACK];
        if(COUNT:'d'8) & RESET               next ST5 out !W;
        if(COUNT:'d'10) & RESET              next ST3 out [W,DSACK];
        default                              next ST5;

present ST6:
         /* HIGH SPEED ACCESS    */
         if(COUNT:'d'2) & RESET              next ST6 out !W;
         if(COUNT:'d'4)                      next ST3 out [W,DSACK];
         default                             next ST6;

present ST7:
         /* NORMAL REFRESH CYCLE */
         if AS                               next ST7 out !AGREQ;
         if(COUNT:'d'0) & RESET              next ST7 out !MCI_;
         if(COUNT:'d'1) & RESET              next ST7 out !RASI;
         if(COUNT:'d'3) & RESET              next ST7 out !RFC;
         if(COUNT:'d'5)                      next ST7 out [RFC,RASI];
         if(COUNT:'d'6) & (A22 # AGREQ)      next ST0 out  MCI_;
         if(COUNT:'d'6) & !A22 & !AGREQ      next ST7 out  MCI_;
         if(COUNT:'d'9) & RESET              next ST7 out !RASI;
         if(COUNT:'d'10) & RESET             next ST7 out  MSEL;
         if(COUNT:'d'11) & RESET             next ST7 out [!CASI,!DSACK];
         if(COUNT:'d'12) & RESET             next ST7 out !W;
         if(COUNT:'d'14)                     next ST3 out [W,DSACK];
         default                             next ST7;

present ST8:
         /* EXTENDED REFRESH CYCLE   */
         if(COUNT:'d'1)                      next ST8 out [RASI,!MSEL,CASI];
         if(COUNT:'d'3)                      next ST7;
         default                             next ST8; }

APPEND RASI.s = !RESET; APPEND CASI.s  = !RESET; APPEND RFC.s   = !RESET;
APPEND W.s    = !RESET; APPEND AGREQ.s = !RESET; APPEND DSACK.s = !RESET;
APPEND MCI_.s = !RESET; APPEND SCLR0   = !RESET; APPEND MSEL.r  = !RESET;
APPEND P0_.r  = !RESET; APPEND P1_.r   = !RESET; APPEND P2_.r    = !RESET;
APPEND P3_.r  = !RESET;
```

```
NAME      SCDECODE;
PARTNO    T10004;
DATE      05/07/87 ;
REV       01 ;
DESIGNER  Breuninger/Peprah;
COMPANY   Texas Instruments;
ASSEMBLY  None ;
LOCATION  Dallas;

/*************************************************************************************************/
/* Static Column Decode                                                                          */
/*                                                                                               */
/*      CUPL simulation file for the Static Column Decode Application                            */
/*                                                                                               */
/*************************************************************************************************/
/*  Allowable Target Device Types :  TEXAS INTSRUMENTS  PSG507                                   */
/*************************************************************************************************/

ORDER:  OSC,%4,RESET,%4,A22,%3,RW,%3,REFREQ,%5,AS,%2,HSA,%5,SYSCLK,%3,COUNT,
        %2,RFC,%4,RAS1,%4,MSEL,%4,CAS1,%3,MC1_,%2,W,%3,DSACK,%4,STATE;

BASE: DECIMAL;

VECTORS:

$msg"   ";
$msg"   ";
$msg"NORMAL ACCESS CYCLE";
$msg"   ";
$msg"     ------------------ INPUT ------------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RAS1,MSEL,CAS1,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C    0    X   X   X     X  X     X    'X'    H    H    L    H   H   H    H    "0"
          C    1    X   X   1     0  X     X    '0'    H    H    L    H   H   H    H    "0"
          C    1    X   X   1     1  X     1    '0'    H    H    L    H   H   H    H    "1"
          C    1    0   X   X     X  X     X    '0'    H    H    L    H   H   H    H    "2"
          C    1    X   X   X     X  X     X    '0'    H    L    L    H   H   H    H    "2"
          C    1    X   X   X     X  X     X    '1'    H    L    H    H   H   H    H    "2"
          C    1    X   X   X     X  X     X    '2'    H    L    H    L   H   H    L    "2"
          C    1    X   X   X     X  X     X    '3'    H    L    H    L   H   L    L    "2"
          C    1    X   X   X     X  X     X    '4'    H    L    H    L   H   L    L    "2"
          C    1    X   X   X     X  X     X    '5'    H    L    H    L   H   H    H    "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 4 WITH EXTENDED ACCESS REQUEST";
$msg"   ";
$msg"     ------------------ INPUT -------------------  -------------- OUTPUT ------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RAS1,MSEL,CAS1,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C    1    1   X   1     1  X     1    '0'    H    L    H    L   H   H    H    "4"
          C    1    0   X   X     X  X     X    '0'    H    L    H    L   H   H    H    "4"
          C    1    X   X   X     X  1     X    '1'    H    H    L    H   H   H    H    "5"
```

```
$msg"   ";
$msg"   ";
$msg"EXTENDED ACCESS";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------ OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C    1    X   X   X     X  X     X    '2'    H    H    L    H   H  H    H    "5"
           C    1    X   X   X     X  X     X    '3'    H    H    L    H   H  H    H    "5"
           C    1    X   X   X     X  X     X    '4'    H    H    L    H   H  H    H    "5"
           C    1    X   X   X     X  X     X    '5'    H    L    L    H   H  H    H    "5"
           C    1    X   X   X     X  X     X    '6'    H    L    H    H   H  H    H    "5"
           C    1    X   X   X     X  X     X    '7'    H    L    H    L   H  H    L    "5"
           C    1    X   X   X     X  X     X    '8'    H    L    H    L   H  L    L    "5"
           C    1    X   X   X     X  X     X    '9'    H    L    H    L   H  L    L    "5"
           C    1    X   X   X     X  X     X   '10'    H    L    H    L   H  H    H    "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 4 WITH HIGH SPEED ACCESS REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------ OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C    1    1   X   1     1  X     1    '0'    H    L    H    L   H  H    H    "4"
           C    1    0   X   X     X  X     X    '0'    H    L    H    L   H  H    H    "4"
           C    1    0   X   X     X  0     X    '1'    H    L    H    L   H  H    L    "6"

$msg"   ";
$msg"   ";
$msg"HIGH SPEED ACCESS";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------ OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C    1    X   X   X     X  X     X    '2'    H    L    H    L   H  L    L    "6"
           C    1    X   X   X     X  X     X    '3'    H    L    H    L   H  L    L    "6"
           C    1    X   X   X     X  X     X    '4'    H    L    H    L   H  H    H    "3"

$msg"   ";
$msg"   ";
$msg"NON-MEMORY ACCESS FOLLOWED BY REFRESH REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------ OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C    1    1   X   1     1  X     1    '0'    H    L    H    L   H  H    H    "4"
           C    1    1   X   X     X  X     X    '0'    H    H    L    H   H  H    H    "0"
           C    1    X   X   1     0  X     X    '0'    H    H    L    H   H  H    H    "0"
           C    1    X   X   1     X  X     0    '0'    H    H    L    H   H  H    H    "0"
           C    1    X   X   0     X  X     X    '0'    H    H    L    H   H  H    H    "7"
```

```
$msg"   ";
$msg"   ";
$msg"NORMAL REFRESH CYCLE";
$msg"   ";
$msg"     ------------------ INPUT ------------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C    1    X   X   X     0  X     X    '0'    H    H    L    H   L  H   H    "7"
           C    1    X   X   X     0  X     X    '1'    H    L    L    H   L  H   H    "7"
           C    1    X   X   X     0  X     X    '2'    H    L    L    H   L  H   H    "7"
           C    1    X   X   X     0  X     X    '3'    L    L    L    H   L  H   H    "7"
           C    1    X   X   X     0  X     X    '4'    L    L    L    H   L  H   H    "7"
           C    1    X   X   1     0  X     X    '5'    H    H    L    H   L  H   H    "7"
           C    1    X   X   X     0  X     X    '6'    H    H    L    H   H  H   H    "0"

$msg"   ";
$msg"   ";
$msg"NORMAL REFRESH CYCLE FOLLOWED BY ACCESS GRANT REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C    1    X   X   0     X  X     X    '0'    H    H    L    H   H  H   H    "7"
           C    1    X   X   X     0  X     X    '0'    H    H    L    H   L  H   H    "7"
           C    1    X   X   X     0  X     X    '1'    H    L    L    H   L  H   H    "7"
           C    1    X   X   X     1  X     X    '2'    H    L    L    H   L  H   H    "7"
           C    1    X   X   X     1  X     X    '3'    L    L    L    H   L  H   H    "7"
           C    1    X   X   X     0  X     X    '4'    L    L    L    H   L  H   H    "7"
           C    1    0   X   X     0  X     X    '5'    H    H    L    H   L  H   H    "7"
           C    1    0   X   X     0  X     X    '6'    H    H    L    H   H  H   H    "7"
           C    1    0   X   X     0  X     X    '7'    H    H    L    H   H  H   H    "7"
           C    1    0   X   X     0  X     X    '8'    H    H    L    H   H  H   H    "7"
           C    1    0   X   X     0  X     X    '9'    H    L    L    H   H  H   H    "7"
           C    1    0   X   X     0  X     X   '10'    H    L    H    H   H  H   H    "7"
           C    1    0   X   X     0  X     X   '11'    H    L    H    L   H  H   L    "7"
           C    1    0   X   X     0  X     X   '12'    H    L    H    L   H  L   L    "7"
           C    1    0   X   X     0  X     X   '13'    H    L    H    L   H  L   L    "7"
           C    1    0   X   X     0  X     X   '14'    H    L    H    L   H  H   H    "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 3 WITH EXTENDED REFRESH REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C    1    X   X   1     X  X     0    '0'    H    L    H    L   H  H   H    "3"
           C    1    X   X   1     0  X     X    '0'    H    L    H    L   H  H   H    "3"
           C    1    X   X   0     X  X     X    '0'    H    L    H    L   H  H   H    "8"
```

```
$msg"   ";
$msg"   ";
$msg"EXTENDED REFRESH CYCLE";
$msg"   ";
$msg"     ----------------- INPUT -----------------  ------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------- ";
          C    1    X   X   X     X  X     X    '0'    H    L    H    L   H  H   H    "8"
          C    1    X   X   X     X  X     X    '1'    H    H    L    H   H  H   H    "8"
          C    1    X   X   X     X  X     X    '2'    H    H    L    H   H  H   H    "8"
          C    1    X   X   X     X  X     X    '3'    H    H    L    H   H  H   H    "7"
```

Programmable Frequency Divider

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Programmable Frequency Divider

A Single Chip Solution and A Multiple Chip Solution

INTRODUCTION

The purpose of this application report is to provide a comparison between the EP610 and the TIBPAL22V10 architecture capabilities and also illustrate some of the latest PLD (Programmable Logic Device) design tools offered by Texas Instruments. First, a brief description of the EP610 and 22V10 device architectures will be given followed by two unique implementation examples. The first with one EP610 and the second using two TIBPAL22V10 devices. Finally, a comparison will be made between the two designs.

DEVICE ARCHITECTURES

Although the EP610 and TIBPAL22V10 are both available in the same package types, the device architectures are considerably different. Both devices utilize a programmable "AND", fixed "OR" type of architecture common to all programmable logic devices. The EP610 has eight programmable "AND" terms, called Product Terms, per output while the '22V10 can utilize up to 16 product terms on some outputs. The main difference between the two devices which makes the EP610 better suited for this application is the number of registers available in each device. The EP610 has 16 registers available while the '22V10 has only 10, one per macrocell. A complete description of the device architectures and macrocell capabilities can be found in the device data sheets.

DESIGN METHODOLOGY

In the first example, design development will be accomplished using theTI EPLD Development System. The design will be entered in a schematic format using multiple, 4 bit frequency dividers and multiplexers for output control. The design will then be automatically fitted into an EP610 using the A+PLUS software.

The second example will illustrate how to implement the same application with TI's proLogic software. This example will consist of a 12 bit counter and the control logic which allows any one of the 12 counter bits to be routed to a single output thus creating a progammable frequency divider.

SOLUTION 1: Single Chip Frequency Divider Implemented Using EP610

Figure 1 shows the schematic which was entered using the TI EPLD Development System to implement the EP610 design. Three 4 bit frequency dividers were used to implement the 12 bit division. Notice that the divide by 16 bit output of each device was fed to the clock input of the next. By feeding these ouputs to each successive stage, a 2^1 to 2^{12} frequency divider can be implemented.

The next level is a multiplexing level which routes the appropriate divided output to the final output, FDIV. This task is accomplished using an 8 to 1 and a 4 to 1 multiplexer. Some extra control logic is also necessary to provide the final level of multiplexing to the output. The input signals A, B, C, and D are used to select the desired frequency division. The table below illustrates how the device will function:

INPUT A B C D	FREQUENCY DIVISION DIVIDE BY:
0 0 0 0	2^1
0 0 0 1	2^2
0 0 1 0	2^3
•	•
•	•
•	•
1 0 1 0	2^{11}
1 0 1 1	2^{12}

Finally, the design is compiled using the A+PLUS software and a standard JEDEC file is produced which can then be programmed into a single EP610.

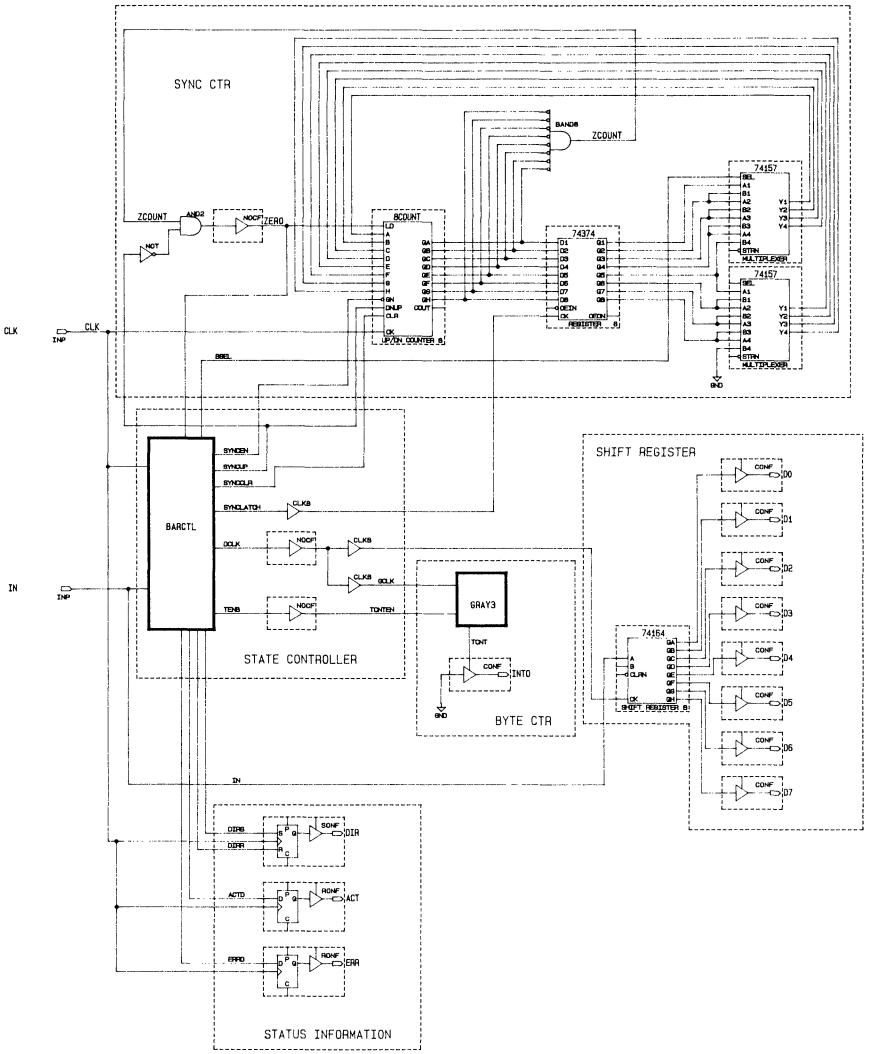

Figure 1. Logicaps Schematic Showing EP610 Solution

SOLUTION 2: Multiple Chip Frequency Divider Implemented Using Two TIBPAL22V10 Devices

In this next example two TIBPAL22V10 devices will be used to implement the frequency divider. Program Listings 1 and 2 show the proLogic codes developed for this application. The code shown in Listing 1 is for device A which provides the 10 lower bits of the 12 bit counter. First, the pin assignments are made which include a clock, clear, and 10 counter outputs. Next, the D input to each register is specified using Boolean equations followed by output enable and polarity configurations. Finally, test vectors are specified which allows the code to be simulated before actually programming a device.

The next proLogic code shown in Listing 2 is for the B device which provides the two most significant bits of the 12 bit counter as well as the mutliplexing control for the outputs. The clock input for the B device is driven by the Q9 output from the A device. It can be seen from the Boolean equations in Listing B that 12 product terms are needed to implement the FDIV output. Each of these "AND" terms is refered to as a Product Term. This is why the '22V10 was chosen for this application since as many as 16 product terms are available in this architecture where most PALs have a maximum of 8 per output.

Diagrams of both solution 1 and 2 along with device pin outs are shown in Figure 2. A complete copy of the proLogic software and manual explaining syntax, design entry methods, device support and simulation can be obtained from your local TI sales office or by calling the TI Programmable Logic applications hotline at (214) 997-5666.

Listing 1: Device A

```
title {  Device:          TIBPAL22V10
         Application:     12 Bit Programmable Frequency Divider: Device A
         Source:          Kyle Newman  Texas Instruments      9/89      }

include p22v10;              /* specify that target device is TIBPAL22V10 */

define  CLK = pin1 ;         /* define input pins */
define  CLR = pin2 ;

define  Q0 = pin14 ;         /* define output pins */
define  Q1 = pin15 ;
define  Q2 = pin16 ;
define  Q3 = pin17 ;
define  Q4 = pin18 ;
define  Q5 = pin19 ;
define  Q6 = pin20 ;
define  Q7 = pin23 ;
define  Q8 = pin22 ;
define  Q9 = pin21 ;

/* define equations to implement lower 10 bits of counter */

  Q0.d = !(Q0.q) & !CLR ;

  Q1.d = (!Q0.q & Q1.q | Q0.q & !Q1.q) & !CLR ;

  Q2.d = (!Q0.q & Q2.q | !Q1.q & Q2.q | Q0.q & Q1.q & !Q2.q) & !CLR ;

  Q3.d = (!Q0.q & Q3.q
        | !Q1.q & Q3.q
        | !Q2.q & Q3.q
        | Q0.q & Q1.q & Q2.q & !Q3.q) & !CLR ;

  Q4.d = (!Q0.q & Q4.q
        | !Q1.q & Q4.q
        | !Q2.q & Q4.q
        | !Q3.q & Q4.q
        | Q0.q & Q1.q & Q2.q & Q3.q & !Q4.q) & !CLR ;

  Q5.d = (!Q0.q & Q5.q
        | !Q1.q & Q5.q
        | !Q2.q & Q5.q
        | !Q3.q & Q5.q
        | !Q4.q & Q5.q
        | Q0.q & Q1.q & Q2.q & Q3.q & Q4.q & !Q5.q) & !CLR;

  Q6.d = (!Q0.q & Q6.q
        | !Q1.q & Q6.q
        | !Q2.q & Q6.q
        | !Q4.q & Q6.q
        | !Q3.q & Q6.q
        | !Q5.q & Q6.q
        | Q0.q & Q1.q & Q2.q & Q3.q & Q4.q & Q5.q & !Q6.q) & !CLR;


Q7.d = (!Q0.q & Q7.q
        | !Q1.q & Q7.q
        | !Q2.q & Q7.q
        | !Q3.q & Q7.q
```

```
        | !Q4.q & Q7.q
        | !Q5.q & Q7.q
        | !Q6.q & Q7.q
        | Q0.q & Q1.q & Q2.q & Q3.q & Q4.q & Q5.q & Q6.q & !Q7.q) & !CLR;

  Q8.d = (!Q0.q & Q8.q
        | !Q1.q & Q8.q
        | !Q2.q & Q8.q
        | !Q4.q & Q8.q
        | !Q3.q & Q8.q
        | !Q5.q & Q8.q
        | !Q6.q & Q8.q
        | !Q7.q & Q8.q
          | Q0.q & Q1.q & Q2.q & Q3.q & Q4.q & Q5.q & Q6.q & Q7.q & !Q8.q) &
!CLR;

 Q9.d = (!Q0.q & Q9.q
        | !Q1.q & Q9.q
        | !Q2.q & Q9.q
        | !Q3.q & Q9.q
        | !Q4.q & Q9.q
        | !Q5.q & Q9.q
        | !Q6.q & Q9.q
        | !Q7.q & Q9.q
        | !Q8.q & Q9.q
  | Q0.q & Q1.q & Q2.q & Q3.q & Q4.q & Q5.q & Q6.q & Q7.q & Q8.q & !Q9.q) &
!CLR;


 /*  permanently enable all counter outputs  */
 Q0.oe = 1;  Q1.oe = 1;  Q2.oe = 1;  Q3.oe = 1;  Q4.oe = 1;
 Q5.oe = 1;  Q6.oe = 1;  Q7.oe = 1;  Q8.oe = 1;  Q9.oe = 1;


 /*  define outputs as active high  */
 Q0 = q;  Q1 = q;  Q2 = q;  Q3 = q;  Q4 = q;
 Q5 = q;  Q6 = q;  Q7 = q;  Q8 = q;  Q9 = q;


 /*  define some test vectors to verify that counter is working properly  */
test_vectors { /* CLK   CLR         Q3     Q2     Q1     Q0    */
                pin1  pin2       pin17  pin16  pin15  pin14;
                C     1          L      L      L      L     ;   /* RESET */
                C     1          L      L      L      L     ;   /* RESET */
                C     0          L      L      L      H     ;   /*   1   */
                C     0          L      L      H      L     ;   /*   2   */
                C     0          L      L      H      H     ;   /*   3   */
                C     0          L      H      L      L     ;   /*   4   */
                C     0          L      H      L      H     ;   /*   5   */
                C     0          L      H      H      L     ;   /*   6   */
                C     0          L      H      H      H     ;   /*   7   */
                C     0          H      L      L      L     ;   /*   8   */
                C     0          H      L      L      H     ;   /*   9   */
                C     0          H      L      H      L     ;   /*   10  */
                C     0          H      L      H      H     ;   /*   11  */
                C     0          H      H      L      L     ;   /*   12  */
                C     0          H      H      L      H     ;   /*   13  */
                C     0          H      H      H      L     ;   /*   14  */
                C     0          H      H      H      H     ;   /*   15  */
                C     0          L      L      L      L     ;   /*   0   */
                C     1          L      L      L      L     ;   /* RESET */
```

Listing 2: Device B

```
title {  Device:          TIBPAL22V10

         Application:     12 Bit Programmable Frequency Divider:  Device B
                          2 MSB and Multiplexing Control
         Source:          Kyle Newman  Texas Instruments      9/89      }

include p22v10;           /* specify that target device is TIBPAL22V10 */

define  CLK = pin1 ;      /* clock input is from Q9 on device A        */
define  CLR = pin2 ;      /* clear goes to pin 2 on both devices       */

define  A = pin3 ;        /* select inputs for multiplexing outputs    */
define  B = pin4 ;        /*   Select Input         Q Output           */
define  C = pin5 ;        /*    ABCD = 0           divide by 2         */
define  D = pin6 ;        /*           1                    4         */
                          /*           2                    8 ..etc   */

define  Q0 = pin7  ;      /* define counter inputs from device A       */
define  Q1 = pin8  ;
define  Q2 = pin9  ;
define  Q3 = pin10 ;
define  Q4 = pin11 ;
define  Q5 = pin13 ;
define  Q6 = pin14 ;
define  Q7 = pin15 ;
define  Q8 = pin16 ;
define  Q9 = pin17 ;

define  Q10 = pin19 ;      /*  define 2 MSB of 12 bit counter  */
define  Q11 = pin20 ;

define  FDIV = pin18 ;       /*  divided output  */

 /*  define equations to implement 2 MSB of counter */

  Q10.d = !(Q10.q) & !CLR ;

  Q11.d = (!Q10.q & Q11.q | Q10.q & !Q11.q) & !CLR ;

 /*  define equations to control multiplexing of outputs  */

  FDIV  =  Q0   & !A & !B & !C & !D
        |  Q1   & !A & !B & !C &  D
        |  Q2   & !A & !B &  C & !D
        |  Q3   & !A & !B &  C &  D
        |  Q4   & !A &  B & !C & !D
        |  Q5   & !A &  B & !C &  D
        |  Q6   & !A &  B &  C & !D
        |  Q7   & !A &  B &  C &  D
        |  Q8   &  A & !B & !C & !D
        |  Q9   &  A & !B & !C &  D
        | Q10.q &  A & !B &  C & !D   /* ".q" was used on these terms        */
        | Q11.q &  A & !B &  C &  D;  /* because they are internal feedbacks */

 /*  permanently enable all outputs  */
  Q10.oe = 1;  Q11.oe = 1;  FDIV.oe = 1;

 /*  define outputs as active high  */
  Q10 = q;  Q11 = q;
```

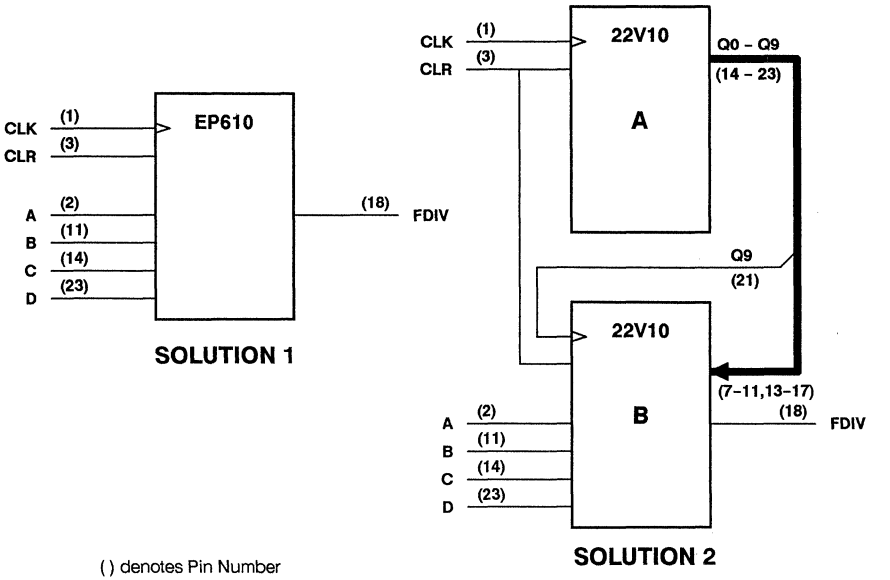

Figure 2. EP610 vs TIBPAL22V10 Solution

CONCLUSION

Following is a brief comparison of the two design implementations discussed in the applications note.

	SOLUTION 1	SOLUTION 2
DEVICE TYPE	**EP610**	**TIBPAL22V10**
PACKAGE	24 PIN DIP	24 PIN DIP
MAX I_{CC}	60 mA	180 mA
PROPAGATION DELAY	25 ns	20 ns - 25 ns
MAX CLOCK FREQUENCY	40 MHz	28.5 MHz
PRICE PER PACKAGE	1.7X	X
NUMBER OF DEVICES	1	2

From this comparison, it can be seen that the EP610 is a better solution for this application. Not all applications will yield these results between a EP610 and a 22V10. However in register intensive applications such as the frequency divider, an EP610 can offer considerable savings in power consumption and package count while providing enhanced performance at a comparable price.

EP1810 as a Bar Code Decoder

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FEATURES

- Description of a generic Barcode
- Description of a Bar Code Decoder EPLD
- State machine implements controller functions
- Functional simulation verifies design before commitment to silicon
- TTL MacroFunctions simplify and speed up the design task

EP1810 as a Bar Code Decoder

INTRODUCTION

The following Applications Brief describes a bar code decoder implemented in an EP1810. The EP1810 decodes a generic bar code, stores the decoded data byte, and alerts a microprocessor that data is ready. This Application Brief describes a generic bar code decoder, the various design methodologies used to implement the design and the functional simulation used to verify the design before programming devices. The final design is specified by a mix of design entry formats: state machine design entry is used to specify an internal controller, while schematic capture and TTL macrofunctions are used to define additional functions.

WHAT IS BAR CODE?

Bar code, a means of representing binary data or program information, has become popular due to its great flexibility and cost effectiveness. For many applications bar code yields superior results when compared to optical character recognition, particularly for success on a first time read. Bar code is suitable in many applications where magnetic stripe or other media would be impractical. Bar code has several variations; this Application Brief covers a common version with some advanced features.

PHYSICAL SPECIFICATIONS OF BAR CODE

Although many versions of bar code exist to support the variety of applications served, there is enough in common to treat a meaningful generic case (Figure 1). All bar codes have "zero", "one", and space characters; the "zero" and space character are the same width, while the "one" is twice that width. All bar codes have a header and a tail. The generic bar code has a header consisting of a zero-zero sequence, followed by a checksum byte. The tail is a one-zero sequence. Data follows the header and terminates with the tail. All bar codes have maximum limits on the number of data bytes.

One requirement for accurate bar code detection is that the reader, usually a light pen, scan the bar code at a relatively constant speed. For this reason bar codes are of modest width; its easier to move a light pen at reasonably constant speed over shorter distances than over longer ones. Before reading the bar code, the light pen is inactive or in a white region. As the light pen reaches the dark region of the header, the light pen output goes high. If the light pen's speed varies by too much, then the mis-read should be detected by verification against the checksum.

A generic barcode has "0", "1", and space characters. Bar code sequences consist of START and STOP bars, data and checksum bytes.

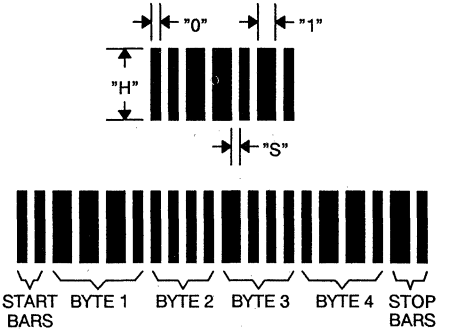


Figure 1. Sample Barcode

BAR CODE DECODER OVERVIEW

Figure 2 shows a bar code decoder implemented in an EP1810. The bar code data is fed into the EP1810 through the IN input. The data is used by the sync counter to determine the input data read rate, and by the state machine to decode incoming data, which is stored in a shift register. Once 8 bits of data have been shifted into the shift register, an open collector interrupt back to the microprocessor (INTO) goes low. Various status outputs (DIR, ACT, and ERR) indicate the current state of the bar code decoder.

The bar code decoder consists of 5 different modules: a sync counter, a controller state machine, a byte counter, a shift register, and a microprocessor interface.

Sync Counter

The bar code decoder uses the bar code header's leading single width dark region to measure the fundamental width of a "zero". When the light pen passes over the first dark region, the sync counter begins counting. The sync counter stops counting only when the light pen has completed reading the dark region (ie. when it reads the beginning of light region). The count value thus reflects the amount of time required to read the width of a space or "zero" bar. It takes twice the count value to read a "one" bar.

The count value is used to sample the bar code data. Since the light pen scanning speed will vary somewhat over the bar code label, the count value is only approximately correct at measuring width. For this reason it is best not to sample data on the edges of the light and dark regions, but rather in the center of these regions. The first sampling occurs in the middle of the space width following the leading dark region when the sync counter reaches half of its sync value. The counter is reset and subsequent samples occur when the sync counter reaches the full sync value.

A barcode decoder implemented in an EP1810 consists of Syn Counter, State Controller, Byte Counter, Status Outputs, and Shift Register sections.

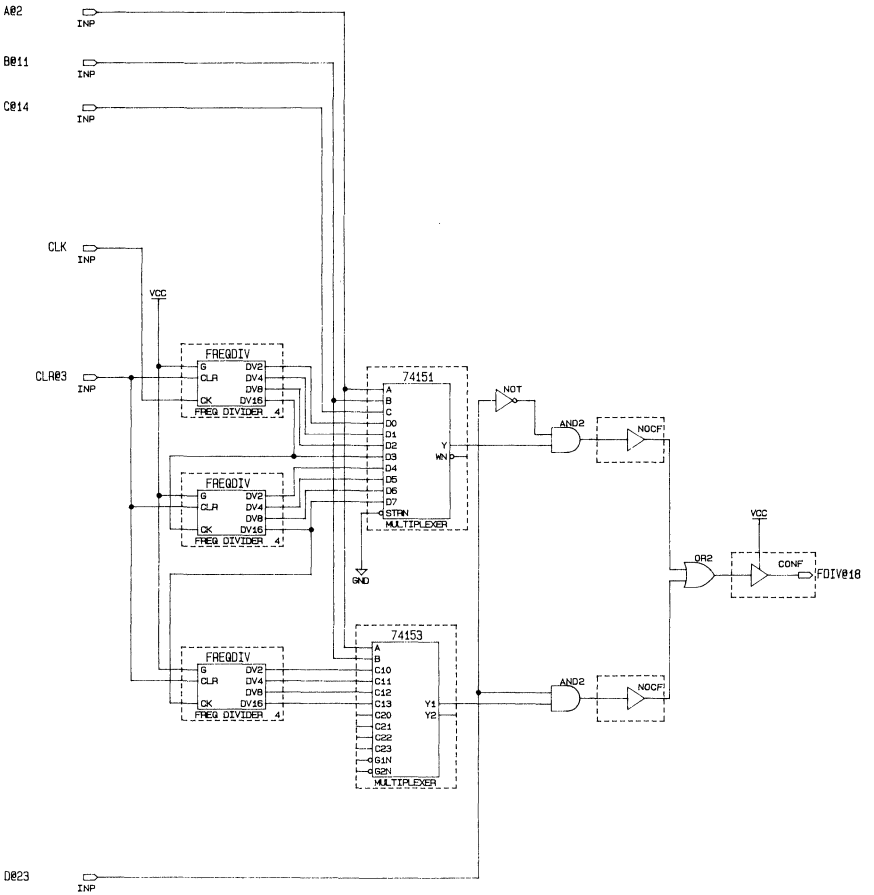


Figure 2. Bar Code Decoder Schematic

The values of the data samples correspond to the bar encoded data. If "dark-light" is read, then the light pen has passed over a single width dark region followed by a single width light region, indicating a "zero". If a "dark-dark-light" is read, then the light pen has passed over two adjacent dark regions followed by a light region, indicating a "one". If any other combinations starting with "dark" are read, or if two adjacent "light"s are read, then the code is invalid.

The sync counter is implemented by four Macro-Functions (8COUNT, 2 of 74157s, and the 74374) and terminal count circuitry comprised of logic and an NOCF primitive.

Byte counter specification

The byte counter counts the number of bits shifted in, and if they are a multiple of 8, alerts the microprocessor that a full byte is ready to be read. The byte counter is implemented using a Gray code sequence, a sequence which only has one bit change between any two count transitions, so that its outputs will be glitch-free; preventing spurious outputs from inadvertently interrupting the micro-processor. Figure 3 shows the byte counter implemented using the state machine format.

An 8 stage gray counter is implemented using the high level state machine format (SMF)

```
%GRAY3  3 BIT GRAY COUNTER%
PART: EP1810J
INPUTS:
OUTPUTS:
NETWORK:
EQUATIONS:
 TCNT = TCNTEN*/G2*/G1*/G0;

MACHINE: GRAY3
  CLOCK: GCLK
  STATES: [ G2 G1 G0 ]
   S0     [  0  0  0 ]
   S1     [  0  0  1 ]
   S2     [  0  1  1 ]
   S3     [  0  1  0 ]
   S4     [  1  1  0 ]
   S5     [  1  1  1 ]
   S6     [  1  0  1 ]
   S7     [  1  0  0 ]

S0:  S1   %STATES MAKES UNCONDITIONAL%
S1:  S2   %TRANSITION TO NEXT STATE  %
S2:  S3
S3:  S4
S4:  S5
S5:  S6
S6:  S7
S7:  S0

END$
```

Figure 3. Byte Counter State Machine File

The byte counter has an open collector output back to the microprocessor (INTO), fashioned by connecting the input of a 3-state driver to ground and selectively enabling the 3-state (TCNT).

Shift register specification

Input data is stored in a 74164 shift register. The shift register clock is fed from the state controller state machine to assure that data is latched at the appropriate time. The 74164 outputs should be buffered and connected to the microprocessor bus. The shift register is implemented by a 74164 macrofunction and CONF output primitive.

Bar Code Decoder Status Information

Special outputs allow external devices to determine the status of the bar code decoder. If active, the DIR signal indicates that the tail was read before the header. In this instance all data and checksum words would be reversed, and the microprocessor would have to make the compensating transformations. The ability to read bar codes backwards as well as forwards is a practical requirement, permitting bar codes to be read upside down as well as scanned from right to left.

The ACT signal indicated that a bar code is being scanned in. This is useful for a variety of error handling or initialization tasks: for example a microprocessor may poll on this signal and enter special routines dedicated to bar code reading.

The ERR signal indicates an illegal sequence of light and dark regions was encountered during the decoding process: perhaps the bar code is unreadable, or the scan rate was not uniform enough. The microprocessor may use ERR to dump illegal reads without computing and comparing a checksum against the checksum byte passed to the microprocessor by the bar code.

The status information is comprised of the open collector CONF output, and the SONF and RORF status flags.

State controller specification

The bar code decoding process requires intelligence to determine if a header is valid, and to convert the light and dark bar code regions to machine readable data. Beyond data conversion, the bar code decoder must coordinate activities of sync counter, shift register, byte counter, and status generation circuitry. The simplest means of achieving these aims is to create a centralized state controller state machine. Figure 4 shows the state diagram for the state controller, implemented using the high level state machine syntax shown in figure 5. The algorithm for Figure 4 is as follows:

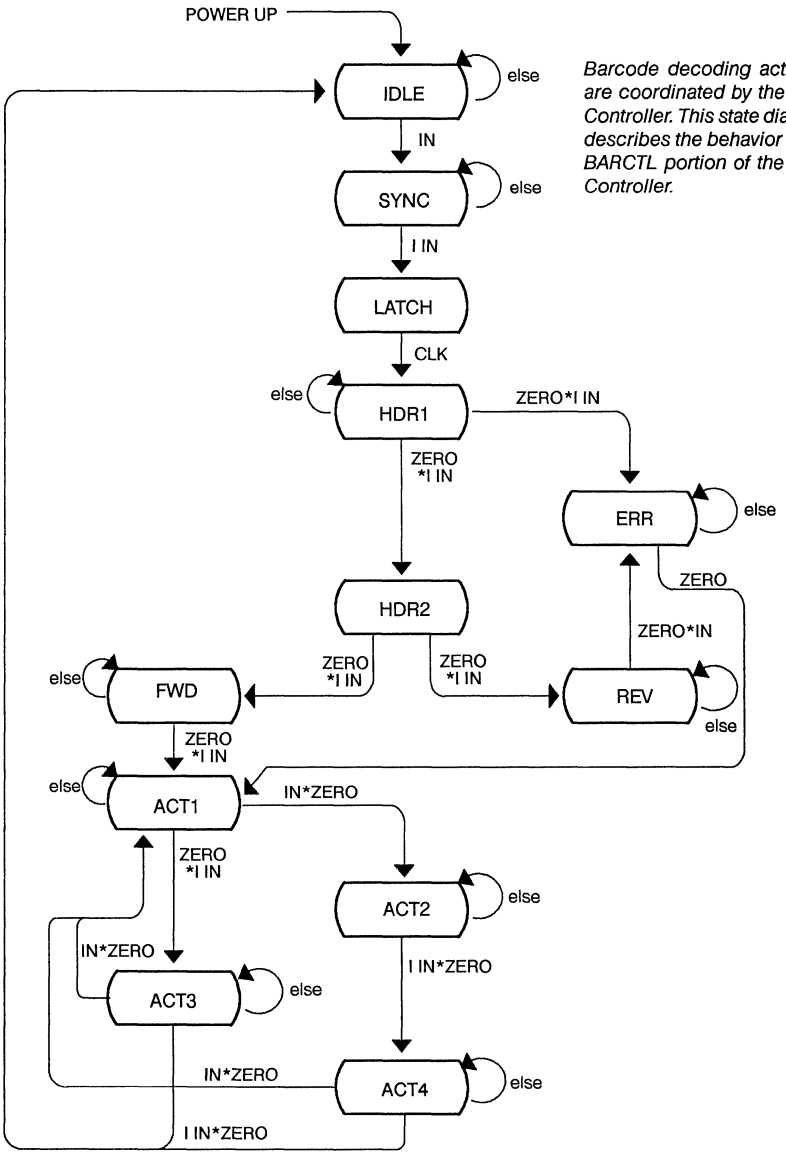
IDLE – the machine idles until a dark region is read by the input device (eg. light pen) at which time the sync counter is started.

SYNC – The sync counter counts up while in this state. The machine stays in this state until reading the first light region. The sync count corresponds to the width of the first dark bar.

LATCH – The machine latches the count value into a holding register. Hereafter the sync count will expire on every modulus of the latched count, and cause the reading of the input stream.

HDR1, HDR2, FWD, REV, ERR – The machine begins reading the rest of the header bits. Bear in mind that we get two different sequences depending if we read a 0–0 sequence or a 0–1 sequence. The 0–0 sequence is a forward read, while the 0–1 sequence is a backward read. If there are any improper reads we will go to ERR. Direction status is latched dependent on either state FWD or REV. At the end of this we begin the reading of data and checksum bytes into the shift register.

ACT1, ACT2, ACT3, ACT4 – These are the active reading states. The ACT1 – ACT3 loop indicates a "0" was read. The ACT1–ACT2–ACT4 loop corresponds to the reading of a "1". Reading is stopped when a long white space is read indicating the end of the bar code.



Barcode decoding activities are coordinated by the State Controller. This state diagram describes the behavior of the BARCTL portion of the State Controller.

Figure 4. Controller State Diagram

```
% Bar Code Controller %
PART: EP1800J
INPUTS:
OUTPUTS:
EQUATIONS:
NETWORK:
  DIRS = FWD;              DIRR = IDLE;
  ACTD = !IDLF;            ERRD = ERR * !IDLE;
  SYNCCLR = IDLK * /IN;    SYNCUP = SYNC;
  SYNCEN = IDLE;           SYNCLATCH = LATCH;
  DCLK = ACT2 + ACT3;      TENB = ACT2 + ACT3 + ACT4;
  BSEL = /LATCH;

MACHINE: BARCTL
  CLOCK: CLK
  STATES: [Q3 Q2 Q1 Q0]
    IDLE  [ 0  0  0  0]
    SYNC  [ 1  0  0  1]
    LATCH [ 0  1  1  1]
    HDR1  [ 1  0  1  1]
    HDR2  [ 1  1  1  1]
    FWD   [ 0  1  0  1]
    REV   [ 0  1  1  0]
    ACT1  [ 0  1  0  0]
    ACT2  [ 1  1  0  0]
    ACT3  [ 0  0  1  0]
    ACT4  [ 0  0  1  1]
    ERR   [ 1  1  1  0]

IDLE:
        IF IN THEN SYNC
SYNC:
        IF /IN THEN LATCH
LATCH:
        HDR1
HDR1:
    IF IN*ZERO THEN HDR2
    IF /IN * THEN ERR
HDR2:
        IF IN * ZERO THEN REV
        IF /IN * ZERO THEN FDW
FDW:
        IF ZERO THEN ACT1
REV:
        IF IN * ZERO THEN ERR
        IF /IN * ZERO THEN ACT1
ACT1:
        IF IN * ZERO THEN ACT2
        IF /IN * ZERO THEN ACT3
ACT2:
        IF IN * ZERO THEN ERR
        IF /IN * ZERO THEN ACT4
ACT3:
        IF IN * ZERO THEN ACT1
        IF /IN * ZERO THEN IDLE
ACT3:
        IF IN * ZERO THEN ACT1
        IF /IN * ZERO THEN IDLE
ERR:
        IF ZERO THEN ACT1
END$
```

Figure 5. Controller State Machine Described Using the State Machine Format

IMPLEMENTATION OF THE BAR CODE DECODER

Figure 2 shows a LogiCaps schematic of the Bar Code Decoder. The sync counter is implemented by four MacroFunctions (8Count, 2 of 74157s, and the 743474) and terminal count circuitry comprised of logic and an NOCF primitive. The byte counter is implemented in state machine format in a file named GRAY3.SMF (Fig 4). The shift register is implemented with MacroFunction 74164 and CONF output primitives. The microprocessor interface consists of a CONF configured as an open collector output and status flags implemented by SONF and RORF primitives. The State controller was implemented in a state machine file named BARCTL.SMF (Fig 5). The state machines are outlined on the schematic for documentation purposes only. The borders are not required for design processing.

DESIGN PROCESSING

Design input is contained in three separate files, of two different formats. LogiCaps generates the bar.adf file, whereas barctl.smf and gray3.smf are state machine files. Linking all the design information is done in the A+PLUS Design Processor (ADP) section of the A+PLUS development software. This is done by answering all the prompts as in Figure 6.

ADP automatically links the names between the various input files and create an output file bar.jed for device programming. Device utilization, given after processing, indicated that 38 of the 48 macrocells were used, 2 of the 7 inputs, and 36 percent of the available logic.

```
APLUS  ADP

FORMAT    : Adf
FILE NAME: bar barctl.smf gray3.smf
MIN       : yes
INV CTL   : no
LEF ANAL  : yes
```

Figure 6. Multiple Design Processing Prompts

SIMULATION VERIFIES OPERATION BEFORE PROGRAMMING A DEVICE

Simulation was run on the device to assure proper operation. In this instance a serial input stream corresponding to a valid bit stream is read by the design. It properly sequences through the states, latches the data, and interrupts a processor. The anticipated simulation data is shown in Figure 7. The controller state machine is verified by comparing the Q0-Q3 outputs, and the state table values in Figure 5.

The Simulator will be driven with a data input emulating the previous sequence. Design behavior is verified by monitoring for the correct response from the Functional Simulator.

Figure 7. Anticipated Simulation Data

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EPLD Development System Summary

Part Number: EP–APLUS

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EPLD Development System Summary

FEATURES:

- ❑ **Complete Design Solution for TI EPLDs**
  - **Development Software**
  - **Programming Hardware**
  - **Device Samples**
- ❑ **Supports Multiple Design Entry methods**
  - **Schematic Capture Entry**
  - **Netlist Entry**
  - **Boolean Equation Entry**
  - **State Machine Entry**
- ❑ **Device Fitter Optimizes Device Resources**
- ❑ **Support for User-Defined MacroFunctions**
- ❑ **Automatic Pin Assignments**

GENERAL DESCRIPTION:

The Texas Instruments (TI) Erasable Programmable Logic Device (EPLD) Development System is a consolidated Computer Assisted Engineering (CAE) tool that transforms a logic design into a programmed device. The development system supports a variety of input formats that can be used individually or combined together to meet the needs of a particular design task. The system includes design entry, design processing, functional simulation and device programming.

The A+PLUS™ software, which is at the heart of this system, includes a design processor which transforms the input format to optimized code used to program the targeted EPLD. The design processor implements logic minimization, automatic EPLD part selection, architecture optimizations and design fitting. The system also includes LogicMap™ software for device programming.

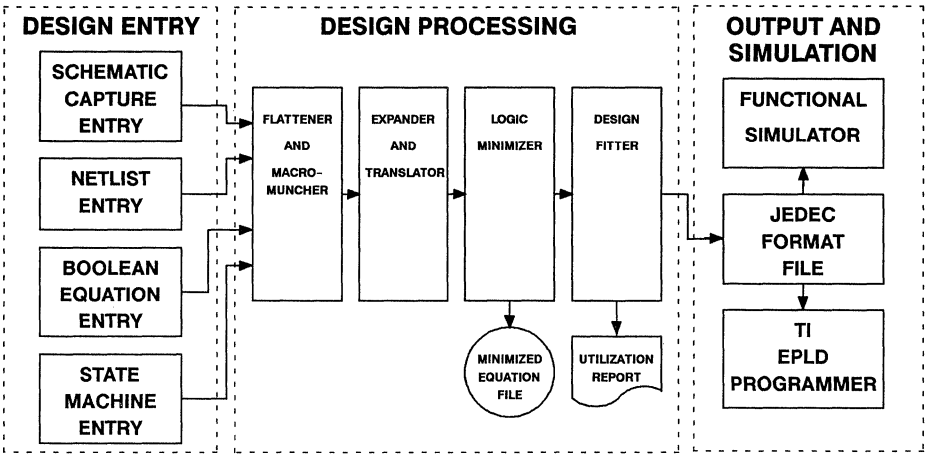


Figure 1. The TI EPLD Development System

FUNCTIONAL DESCRIPTION:

As can be seen in the detailed block diagram of the TI EPLD Development System, in Figure 2, the A+PLUS software accepts four different design entry formats: Schematic Capture, Netlist, Boolean Equations, or State Machine input. The designer is not restricted to just one design entry format but has the freedom to "mix and match" different formats to best meet the needs of the overall logic design.

The design entry format is converted to an A+PLUS Design File (ADF) which is the common entry format for the A+PLUS software. The ADF is then submitted to the A+PLUS Design Processor (ADP). The ADP is composed of a set of modules integrated together that produce an industry standard JEDEC code used to program the EPLD.

The ADP also produces documentation showing minimized logic and EPLD utilization. Once the JEDEC file is produced, the user may functionally simulate the design. Finally the user can program the chosen EPLD with the LogicMap programming software and the hardware provided with this system. TI qualified third party programmers can also be used for production volume programming.

Schematic Capture

Logic Designs may be entered from schematic drawings by using the LogiCaps™ or other schematic capture packages. Schematic capture design entry allows the user to quickly construct a wide range of logic circuits. Designs entered with this method use library primitives in the form of low level functions (input, basic gates, flip-flops, I/O primitives) to high level TTL MacroFunctions. LogiCaps is mouse driven and supports hard copy printouts and plots. As required the schematic representation is converted to an ADF file and processed by the A+PLUS Design Processor.

LogiCaps is a high performance schematic capture package that has been optimized for entering designs destined for TI EPLDs. It is the primary design entry platform for any member of the TI EPLD family. When used in conjunction with TTL and user defined MacroFunction libraries, LogiCaps becomes the essential tool for the design of high density EPLDs.

The TI design library is a collection of high level MSI building blocks which allow the LogiCaps user to enter designs in a "block manner". An initial primitive symbol library contains basic gates, flip-flops and I/O symbols as well as the most commonly used TTL SSI and MSI functions. Other design libraries include an extensive TTL 7400 series symbol library, and user-defined libraries. In addition each library also contains logic functions not available in standard TTL or CMOS devices. Examples include counters implemented with toggle flip-flops, combination up/down counter with left/right shift register, and inhibit gates.

Netlist Entry

The A+PLUS software directly supports netlist entry from third party schematic capture packages via the the A+PLUS Design File (ADF). Using a standard text editor, a netlist which describes the circuit is created by using a simple, high-level,design language.

The netlist may contain basic gates, I/O architectures, boolean equations, and TTL MacroFunction descriptions. In addition, user defined comments and white space may be freely used throughout the ADF file. The completed file is then submitted to the design processor. This entry method also permits circuit designers to utilize netlist outputs (e.g from workstations or other schematic capture packages) that have been translated into ADF format.

Boolean Equations

The A+PLUS Design Processor compiles Boolean equation designs that are written in a simple design language. The source for the design may be created with any convenient text editor. The language supports free-form entry of all syntactical elements. Boolean equations need not be entered in sum-of-products form since the design processor will expand equations automatically. The multi-pass design processor/compiler has the ability to support intermediate equations. This feature allows for significant reduction in the size of the Boolean equation source code and allows the designer to define the logic in the most natural conceptual manner.

State Machine

Designs that are easily represented with state diagrams may be entered via the state machine approach. This method uses a high level language featuring IF-THEN con-

structs, Case statements and truth tables. This design entry supports both Mealy and Moore state machines. Outputs of the state machine may be defined conditionally or unconditionally allowing flexible output structures that can be merged with other portions of the design. In addition, multiple state machines may be linked within the same design. Boolean equations can also be employed, thus offering the definition of high level intermediate logic expression. The software will also select the optimum flip-flops for the particular design.

DESIGN PROCESSING

The A+PLUS Design Processor (ADP) consists of a series of modules that translate design information from a variety of input sources into a JEDEC Standard File used to program the EPLD. This process is automatic and requires little or no assistance from the circuit designer.

Design Flattening

The design processor accepts design files from one or more of the design entry methods already described. Once the design has been submitted, the first function of the ADP is to "flatten" the design from high-level MacroFunctions to low level gate primitives. In order for designs to be flattened, information from the MacroFunction Behavioral Library is transferred to the design flattener, which in turn decomposes all MacroFunctions to their primitive gate equivalents.

MacroMunching™ And Default Modes

Once the design is flattened, the design processor analyzes the complete logic circuit and removes unused gates and flip-flops from any MacroFunction utilized. This "MacroMuncher" allows the logic designer to freely use the high-level building blocks from the MacroFunction Symbol Libraries without the headaches of optimizing their use.

When MacroFunctions with unconnected inputs are detected, the design processor assigns "intelligent" default values. In general, active-high inputs default to ground (GND) and active-low inputs default to the supply voltage (V_{CC}) when left unconnected. This default mode is activated simply by leaving unused inputs without connections, thus eliminating "busy work" and enhancing productivity.

Once the design has been flattened or "munched", and all default values have been assigned, a secondary design file, (SDF file) is produced for further processing.

Translation/Minimization

The Translator takes the SDF file and checks for logic completeness and consistency. For example, the Translator validates that no two logic function outputs are shorted and that all logic nodes have an origin. In the event that the designer has chosen an EPLD name of "AUTO", the Translator will automatically select the appropriate EPLD based on the logic requirements of the design.

Logic minimization of designs is provided by the Minimizer module. Minimization phases include Boolean minimization with a SALSA™ (Speedy A+PLUS Logic Simplifying Algorithm) that yields superior results to other heuristic reduction techniques. DeMorgan's theorem inversion can be applied automatically to equations. The processor contains algorithms based on artificial intelligence techniques to select can-

didate equations that will best be represented by a complemented AND/OR function. This feature significantly reduces product-term demands that can be generated by complex logic functions. For TI EPLDs with selectable flip-flop, the Minimizer checks which type of flip-flops yields a more efficient solution and converts architecture if necessary. The minimized logic can then be passed to the Analyzer module which converts the file into human-readable format allowing the designer to examine the minimized logic.

Design Fitting

The fully minimized design is now transferred to the Fitter. This fitting routine relies on algorithms based on artificial intelligence software techniques in order to fit the logic requirements of the design into the specified EPLD providing full pin assignments automatically.

The Fitter module matches the requests of the design with the resources of the EPLD. The Fitter process encompasses all EPLD architectural attributes such as variable product term distribution, programmable flip-flops, local and global busses and I/O requirements. If the designer specifies a pin assignment, the Fitter matches the request. If no pin assignments are made, the Fitter finds an optimized fit for the design. The Fitter produces a Utilization Report that shows which of the EPLD's resources were used up by the design and how. Finally, the Assembler module converts the fitted requests into an image for the part in a JEDEC Standard File.

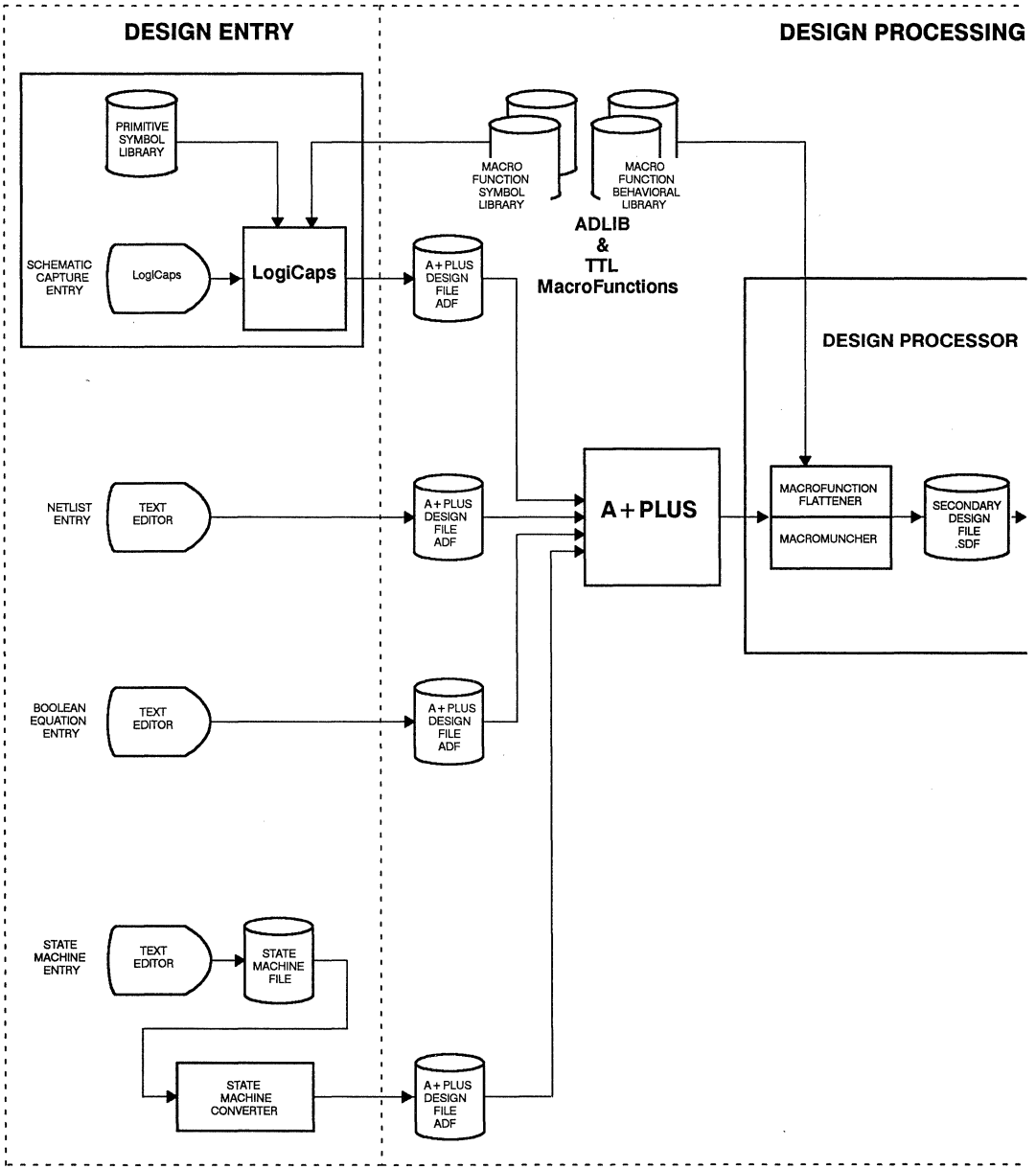
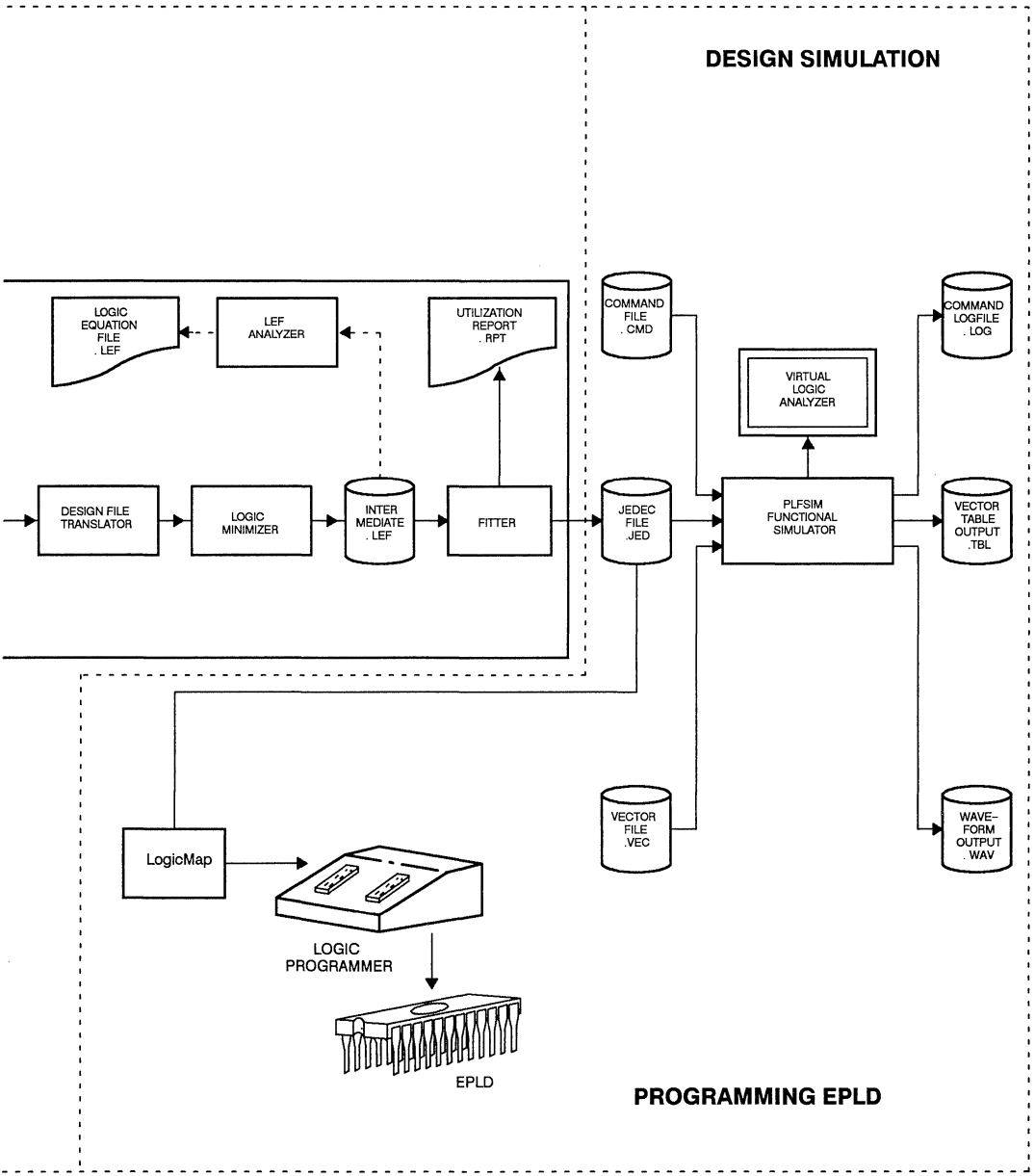


Figure 2. The TI EPLD Development System


DESIGN SIMULATION
LOGIC EQUATION FILE . LEF
LEF ANALYZER
UTILIZATION REPORT . RPT
COMMAND FILE . CMD
COMMAND LOGFILE . LOG
VIRTUAL LOGIC ANALYZER
DESIGN FILE TRANSLATOR
LOGIC MINIMIZER
INTER MEDIATE . LEF
FITTER
JEDEC FILE .JED
PLFSIM FUNCTIONAL SIMULATOR
VECTOR TABLE OUTPUT .TBL
VECTOR FILE .VEC
WAVE-FORM OUTPUT . WAV
LogicMap
LOGIC PROGRAMMER
EPLD
PROGRAMMING EPLD

Design Simulation

Once the design has been fitted to the specified EPLD and a JEDEC file has been produced, the A+PLUS functional simulator allows the designer to test the logical operation of the design. This software package requires the use of any general purpose text editor and is completely compatible with the A+PLUS Development System. As a result, users may now enter designs on the EPLD Development System, have them automatically fitted and optimized, then perform logic simulation without needing to commit a device to hardware.

A complete set of simulation commands allows the user to check critical logic within a design in a succinct and straightforward manner. Users can specify commands to occur at particular events such as during a given circuit condition or at an absolute simulation timestep. Nodes may be forced to a chosen logic state to verify proper circuit behavior from any initial condition. The input waveforms from the VECTOR file containing logic values that are to be applied to the inputs, can be superseded by another pattern at any point in time.

For debugging purposes simulation breakpoints can be set to halt execution when a specified event occurs. This "break" command provides designers the ability to detect illegal states. Once a break condition is met, a command sub-list is activated to provide status information or to enter into a separate procedure. For example, a breakpoint might signal an illegal state, display the current output waveform on the screen, enter a legal state and continue with the simulation.

Device Programming – With LogicMap II

LogicMap II is the interface software that programs EPLDs from JEDEC files created by the A+PLUS Design Processor. The program uses the A+PLUS Super Adaptive Programming algorithm (ASAP ™) which significantly reduces device programming times. LogicMap II fully calibrates the programming environment and checks out the programming hardware when initiated. In addition the program allows the designer to review the JEDEC object code generated by the Processor in a structured manner. The program is fully menu driven and provides views of the device object code through a series of hierarchical windows. This feature permits low-level observation and editing of the design, viewed from a perspective similar to that of the logic diagram of the device in the data sheet. Individual EPROM bits may be examined or changed if desired, however this mode of editing is not recommended.

Hardware – Logic Programmer

LogicMap software is used to drive the programming hardware comprised of a software-configured programming card that occupies a single slot in the computer. Programming signals are transmitted to an external programming unit via a 30 inch ribbon cable and connector. The programming unit contains zero-insertion-force sockets for easy device insertion. All programing waveforms and voltages are derived by the programming card so that no additional power sources are necessary. A programming indicator lamp on the programming unit is illuminated when the unit is active.

For ordering information about Texas Instruments EPLD Development System contact your TI field sales representative, local authorized distributor, or call the customer response center at 1-800-232-3200. For applications questions contact the Programmable Logic Applications Group at (214) 997-5666.

RECOMMENDED COMPUTER CONFIGURATION

- ❑ IBM™ XT™ or AT™ Personal Computer, or Compatible, with:
  - Either Monochrome, CGA, EGA with extended memory or Hercules
  - 640 K bytes of main memory (RAM)
  - 20 M Byte Hard Disk Drive and Floppy-Disk Drive
  - MS-DOS™ or PC-DOS™ versions 3.2 or later releases
  - Full-Card slot for programming Card
  - Serial 3-Button Mouse

DEVELOPMENT SYSTEM CONTENTS

- ❑ **TI Part Number:** EP-APLUS

- ❑ **Software:**
  - A+PLUS programs and support files
  - LogiCaps Schematic Capture Program
  - 7400 Series TTL MacroFunction Library
  - State Machine Entry Program
  - Functional Simulation Program

- ❑ **Documentation:**
  - A+PLUS Reference Manual and User Guide
  - LogiCaps Manual
  - MacroFunction Reference Manual
  - Functional Simulation User Guide
  - State Machine Entry User Guide

- ❑ **Software Warranty:**
  - 12 Month Extended Software Warranty and Update Service

- ❑ **Hardware:**
  - Software Controlled Programmer Interface Card
  - EPLD Master Programming Unit
  - EPLD Device Adapters

EP610 DIP adapter	(PLED600/610)
EP610 J-Lead adapter	(PLEJ600/610)
EP910 DIP adapter	(PLED900/910)
EP910 J-Lead adapter	(PLEJ900/910)
EP1810 J-Lead adapter	(PLEJ1800/1810)

- ❑ **EPLD Device Samples**

  EP610DC
  EP910DC
  EP1810JC

All contents are packaged in a box measuring 18.5 " X 15.5 " X 10.5 ".

EPLD Design Software Summary

Part Number: EP–APLUS–S/W

TEXAS
INSTRUMENTS

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EPLD Design Software Summary

As the software only package of the TI EPLD Development System, the EP-APLUS-S/W extends the TI EPLD Development System to additional satellite design stations without the expense of additional programming hardware. It also fills the needs of design engineers with third party programming hardware already installed.

Designs are entered and processed through the A+PLUS™ Design Processor. The resulting JEDEC file is then transferred to a development system that contains programming hardware or to a third party programmer where the design is physically mapped (programmed) into the device.

Features:

- ❑ Complete CAD software
  - Offers ease of designing with TI EPLDs
  - Consists of the following pieces:
  - LogiCaps® Schematic Capture Software
  - MacroFunction Library
  - A+PLUS, Assembly Software
- ❑ Software Designed to run on IBM-XT™ or AT™ compatible PC with following configuration
  - Monochrome, CGA, EGA with extended memory or Hercules Display
  - 640K bytes of system memory (RAM)
  - 20M bytes hard drive and floppy drive
  - MS-DOS™ or PC-DOS™ Versions 3.2 or later releases
  - Serial 3-Button Mouse

LogiCaps Schematic Capture Software

Contents:

LogiCaps Schematic Capture Diskettes
Printer/Plotter Interface
Standard Symbol Library
LogiCaps Manual

Features:

- ❑ Graphical Entry of Logic Schematics
- ❑ Easy Mouse, Key and Menu Commands
- ❑ Extensive on-line documentation
- ❑ Orthogonal Rubberbanding of lines
- ❑ Area Editing, Save and Load
- ❑ User definable functions (MACROs)
- ❑ Schematic plotting with HP7475,7580 and 7585 plotters
- ❑ Directly Interfaces with the A+PLUS software system
- ❑ Dual window display capability
- ❑ Multiple ZOOM levels
- ❑ Tag and Drag editing
- ❑ Draw schematics up to 90"x90"
- ❑ Standard Symbol Lbrary contains 30 MacroFunctions and over 80 MacroPrimitives

Description:

LogiCaps is a fast and powerful schematic entry tool for capturing designs destined for TI EPLDs. Schematic diagrams are drawn on the screen of a PC using a mouse; then, with a single command, a netlist file is generated ready for logic synthesis and eventual generation of a JEDEC file to be programmed into silicon. LogiCaps complements the A+PLUS software to form a complete interactive EPLD development system.

An engineer could start with a blank "sheet" on a PC, then in minutes transform a circuit idea into a working, user configured integrated circuit.

The most frequently used functions - drawing and connecting lines, moving and copying objects, and just getting around in the drawing - are done by simple mouse motion or pressing a mouse button. Functions used less often are executed by pressing a single key, while those functions rarely used or requiring more data are selected from a nested command menu system. No command requires more than three key presses to execute, unless a file name or some other text is needed.

MacroFunction Library

Contents:

TTL MacroFunction Lbrary Diskettes
ADLIB (A+PLUS Design Librarian) Diskettes
TTL MacroFunction User Manual
ADLIB manual

Features:

- ❑ 100+ Different MacroFunctions
- ❑ Allows High Level Design Entry
- ❑ User Definable Symbols and MacroFunctions with ADLIB
- ❑ Used with LogiCaps Schematic Entry
- ❑ MacroMunching of unused Gates

Description:

The MacroFunctions facilitate easy designing and incresed productivity. They are high level building blocks that allow the user to design at TTL level. This ability aids a first time user since the TTL functions will already be familiar. The experienced EPLD user will also benefit by being able to increase design productivity with the use of MSI function blocks.

Most MacroFunctions are commonly used 7400 series SSI and MSI TTL parts. A few particular ones have been developed specifically to suit logic designs with the TI EPLD architecture. These have been designed by EPLD design experts and contain inner logic behavior to maximize EPLD speed and utilization.

These MacroFunctions are very versatile and can be used together with user designed MacroFunctions and/or low level logic primitives depending on the logic needed. The inputs and outputs of the EPLD to be programmed are specified with A+PLUS I/O design primitives.

A+PLUS Assembly Software

Contents:

A+PLUS Diskettes
ADP, A+PLUS Design Processor, Diskettes
FSIM, Functional Simulator, Diskettes
SMV, State Machine Converter, Diskettes
Install Diskettes
A+PLUS Reference Guide
A+PLUS User Guide, includes
FSIM and SMV Manuals

Features: A+PLUS, PLSME (SMV)

The A+PLUS programs and support files make the following possible;

- ❑ Boolean Equation Entry and Netlist Entry of Logic Designs
- ❑ MacroFunction Design Capability
- ❑ Automatic Pin Assignment and part selection
- ❑ Interactive Netlist Design Entry
- ❑ Design Flattening & Logic Minimization for complete Optimization of EPLD designs

The SMV program is the means whereby programmable logic state machine designs are entered (PLSME - Programmable Logic State Machine Entry incorporates SMV) in addition the following benefits are possible;

- ❑ Multiple State Definition allowed in one file
- ❑ Standard Format Allows Design to be Merged with Other State Machines, Schematic Entry, Boolean Equations, or Netlist Entry within a Single EPLD
- ❑ Human readable format eases the maintenance of complex designs
- ❑ Truth Table Option allows the Specification of Random Logic From functional definition
- ❑ Truth Table Option allows the Specification of Random Logic From functional definition
- ❑ Sophisticated minimization algorithms in A+PLUS Perform automatic reduction to improve device utilization
- ❑ Outputs of State Machines can be either conditionally or unconditionally defined

Description - A+PLUS, PLSME (SMV)

The PLSME and the A+PLUS development software automatically transform high level state machine descriptions into device programming files. PLSME provides a state machine entry option in addition to the traditional entry methods (LogiCaps Schematic Capture, Boolean Equations) currently available to A+PLUS. Design information is entered using any standard text editor. It is then processed by the state machine converter to a standard A+PLUS Design File (ADF). This common intermediate format allows the linking of multiple state machines, schematic, Boolean, or netlist entered design files.

Features: FSIM

- ❑ Simulation of BUS Structures
- ❑ Interactive Debugging ability with Break, Force, Save and Restore Commands
- ❑ Functional Simulation for TI's Entire Family of EPLDs
- ❑ Easy Definition of Inputs using State Table, Vector Patterns or Predefined Patterns
- ❑ Output formats include state table or graphic waveforms for on-screen display or hard copy printout
- ❑ Ability to access buried nodes within the design
- ❑ Back-end integration with A+PLUS Environment using JEDEC File for Simulation

Description - FSIM

FSIM, the A+PLUS Functional Simulator, provides a convenient and easy-to- use tool for testing the logical operation of any EPLD design. This software require the use of any general purpose text editor and is completely compatible with the A+PLUS development system. Consequently users may now enter designs, have them automatically fitted and optimized, then perform logic simulation without needing to commit a device to hardware.

A complete set of simulation commands allows the user to check critical logic within a design in a succinct and straightfoward manner. Users can specify commands to occur at particular events, such as during a given circuit condition or at an absolute simulation timestep. Nodes may be forced to a chosen logic state to verify proper circuit behavior from any initial condition. The input waveforms from the VECTOR file can be superseded by another pattern at any point in time.

For debugging purposes simulation breakpoints can be set to halt execution when a specified event occurs. This "break" command provides designers with the ability to detect illegal states. Once a break condition is met a command sub-list is activated to provide status information or to enter into a separate procedure. For example, a breakpoint might signal an illegal state, display the current output waveform on the screen, enter a legal state and continue with the simulation.

Third–Party Software Tools

Available for Designs with EPLDs

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THIRD-PARTY SOFTWARE DEVELOPMENT TOOLS AVAILABLE FOR DESIGNS WITH EPLDs FROM TEXAS INSTRUMENTS

The third-party support tools listed below appear to meet the specifications published by their manufacturers. Texas Instruments does not accept any responsibility for the suitability or accuracy of these products for use with TI EPLDs. Similar TI products are listed for completeness.

Schematic Capture Software

VENDOR	PRODUCT	DEVICES SUPPORTED
Texas Instruments	LogiCaps™	**TI** – EP330, 610, 630, 910, and EP1810
		ALTERA – EP310, 320, 330, 512, 600, 610, 630, 900, 910, 1210, 1800, 1810, and EPB1400
DATA I/O ®–FutureNet®	DASH4™	EP310, 320, 600, 610, 900, 910, 1210, 1800, and EP1810
OrCAD	SDT III™	EP310, 320, 600, 610, 900, 910, 1210, 1800, and EP1810
View*logic*®	Altera ASIC Design Kit	EP310, 320, 600, 610, 900, 910, 1210, 1800, and EP1810
Mentor Graphics™	PLD Synthesis™	EP310, 320, 600, 610, 900, 910, 1210, 1800, and EP1810
MINC	PLDesigner™	EP310, 320, 600, 610, 900, 910, 1210, 1800, and EP1810

DATA I/O – FutureNet

DATA I/O – FutureNet's DASH 4.1 Schematic Capture package can be used to capture the circuit logic of a design. The output of this package is a standard PLD file.

Phone (800) 247-5700 – For more information

OrCAD Netlist Interface to A+PLUS:

OrCAD Systems, a manufacturer and vendor of schematic capture software, has developed a netlist interface to A+PLUS™ as part of their schematic capture software, the OrCAD/SDT™. The interface translates designs generated with OrCAD's SDT editor into a netlist format which is then translated into an ADF file to be processed by A+PLUS.

Support for TI's logic symbol and MacroFunction libraries is also available with this interface. Existing OrCAD customers with valid software warranty agreements, will receive the interface as part of a general product update. New OrCAD customers will receive the interface when they purchase the OrCAD/SDT package. It is an integral part of the package.

With this interface capability, designs done in the OrCAD/SDT schematic capture environment can now be processed by A+PLUS. For more information on availability of this interface, OrCAD/SDT upgrade and related issues, please contact;

Phone (503) 640-9488 - For more information

Viewlogic Altera ASIC Design Kit

Viewlogic has developed a product called *The Altera ASIC Design Kit* which supports the TI EPLD product family. The kit provides EPLD library primitives and macro's for schematic capture and functional simulation of TI EPLD Designs. An ADF netlist is produced and can be downloaded to the A+PLUS system for design processing and device programming.

Phone (800) 480-0881 - For more information

Mentor Graphics

Mentor Graphics' PLD Synthesis tool offers the capability of using their NETED™ Schematic Capture package to capture the TI EPLD Design. After capture you may specify the TI EPLD as the target device for programming. The software is fully integrated into the mentor Graphic Design enviorment.

Phone (503) 626-7000 - For more information

MINC Inc.

A number of Schematic Editors may be used to capture a TI EPLD Design for development using MINC's PLDesigner. OrCAD, Mentor, Intergraph, Teradyne, and Cadnetix editor's are all supported. Additional language and waveform entry options are included. MINC's software operates on Apollo, Sun, NEC9801, PC and PC-compatable platforms.

Phone (719) 590-1155 - For more information

ALTERNATIVE DESIGN SOFTWARE FOR TI EPLDs:

While it is highly recommended that EPLD designs be processed by the TI EPLD Development System, there are logic design software packages on the market that can process TI EPLD designs.

The following is a short list of alternative design software packages.

Software	Version	Devices Supported	Vendor
ABEL™	3.1	EP610, EP910, EP1810	DATA I/O
CUPL™	3.0	EP610, EP910, EP1810	LOGICAL DEVICES
PLDesigner	1.6	EP610, EP910, EP1810	MINC

TEST VECTOR GENERATION AND FAULT GRADING

The following software packages allow design simulation to be performed by generating test vectors to act as stimuli to the inputs of the design and compare subsequent output responses with expected respones according to the particular design. The programmer load file, in the JEDEC format, is the required input or source file for the generation of such vectors.

VENDOR	PRODUCT	REVISION	DEVICES SUPPORTED
Anvil	ATG™	2.23 and UP	EP310, 320, 600, 610, 900, 910, and EP1210
DATA I/O	PLDtest®	1.3 and UP	EP310, 320, 600, 610, 900, and EP910

BOARD LEVEL SIMULATION

EPLD models developed by Logic Automation Inc. (LAI), enable the designer to do board level simulation of the entire design, including the individual EPLDs. Such simulation tasks can only be accomplished using workstations as platforms. The various workstation platforms capable of simulating with LAI EPLD models are shown below.

VENDOR	PLATFORM	DEVICES SUPPORTED
Logic Automation	MENTOR - QuickSim™ DAISY - DLS2™ VALID - ValidSim™ GATEWAY - Verilog®	EP310, 320, 600, 610, 910, 1800, and 1810

General-Purpose EPLD Behavioral Simulation Models from Logic Automation Inc. (LAI):

Most designers have design verification requirements that involve simulation of a complete system. However existing EPLD design verification tools like PLFSIM (used with A+PLUS), can only simulate the logic integrated into the EPLD, and not the entire system design. Typically these overall system simulation requirements are met using tools available at the workstation level, such as simulation tools offered by Mentor, Daisy and Valid.

In order to accurately represent logic and timing information integrated into an EPLD, a model must be constructed in the appropriate simulation format. Logic Automation Inc., based in Portland, Oregon, has a contract with Texas Instruments to construct models of nearly every TI Programmable Logic Device, including the current line of EPLDs. LAI has been provided with specific architectural information for the EP610, EP910, and EP1810 general-purpose EPLDs which includes macrocell configuration and all ac timing parameters.

LAI has constructed behavioral simulation models, based on the detailed information supplied, for the Mentor, Valid, Daisy and Gateway simulators.

For more information on system simulation involving the TI EPLDs, please contact:

LAI, Applications Dept
19545 N.W. Von Neumann Drive
P.O. Box 310
Beaverton, Oregon 97075

Tel: (503) 690-6900

These are some of the Third-Parties who support TI EPLD Design Development in some way. While the TI A+PLUS System is recommended, this extensive additional support offers you, the designer, choices. These choices can make integration of TI EPLDs into your Design Environment easier. Call the TI Hot line or the local Third-Party vendor if you have questions regarding Third-Party support tools.

TI Hotline: Phone (214) 997-5666

TI Bulletin Board: Phone (214) 997-5665

General Information 1

Data Sheets 2

Application Reports 3

Development Systems 4

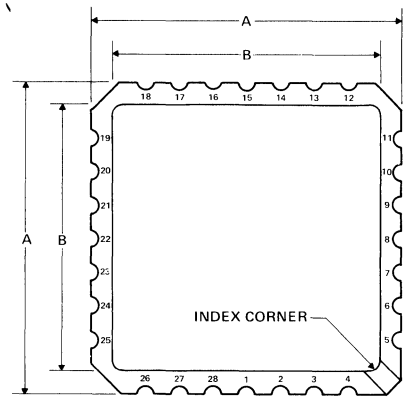
Mechanical Data 5

FK020 and FK028 ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

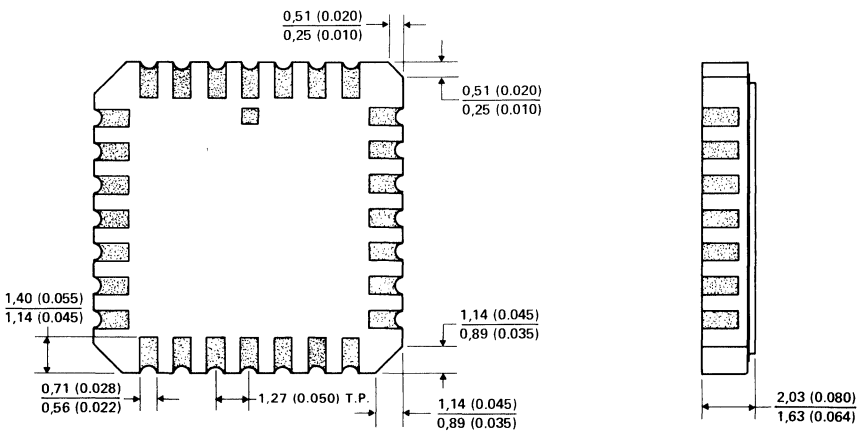
FK020 and FK028
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.

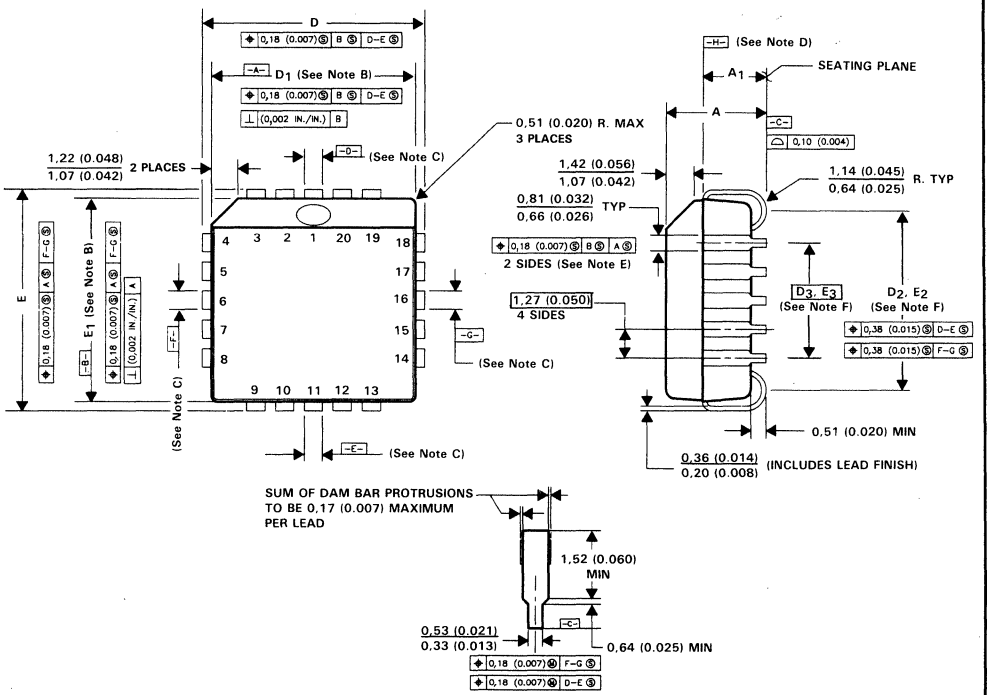


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

FN020, FN028, FN044, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN052, FN068, and FN084
(20-terminal package used for illlustration)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M–1982.

B. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (0.010) on any side.

C. Datums D–E and F–G for center leads are determined at datum –H–

D. Datum –H– is located at top of leads where they exit plastic body.

E. Location to datums –A– and –B– to be determined at datum –H–

F. Determined at seating plane –C–

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FN020, FN028, FN044, FN068, and FN084 plastic chip carrier packages (continued)

JEDEC OUTLINE	NO. OF PINS	A		A_1		D, E		D_1, E_1		D_2, E_2 (See Note F)		D_3, E_3 BASIC
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
MO-047AA	20	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,37 (0.290)	8,38 (0.330)	5,08 (0.200)
MO-047AB	28	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	9,91 (0.390)	10,92 (0.430)	7,62 (0.300)
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AD	52	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	19,94 (0.785)	20,19 (0.795)	19,05 (0.750)	19,20 (0.756)	17,53 (0.690)	18,54 (0.730)	15,24 (0.600)
MO-047AE	68	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

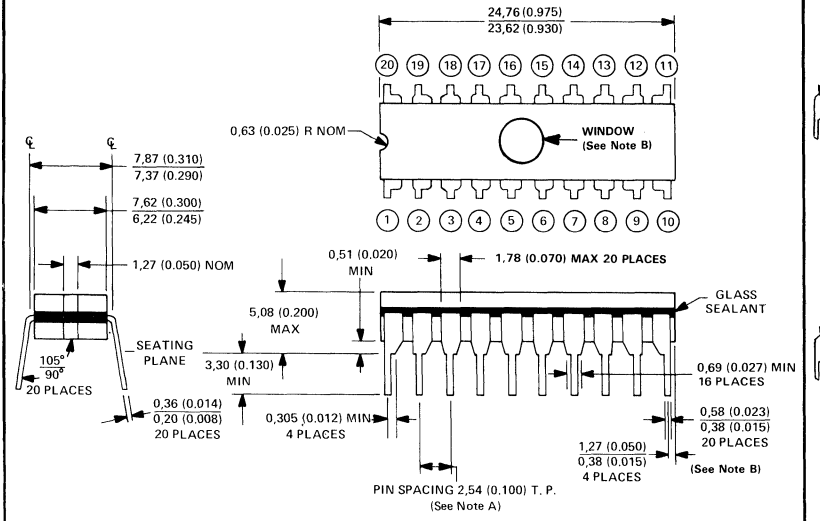
NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M–1982.

F. Determined at seating plane $\boxed{-C-}$

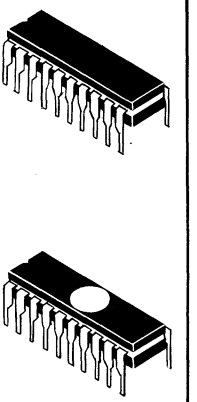
J020 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-coated leads require no additional cleaning or processing when used in soldered assembly.

J020



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

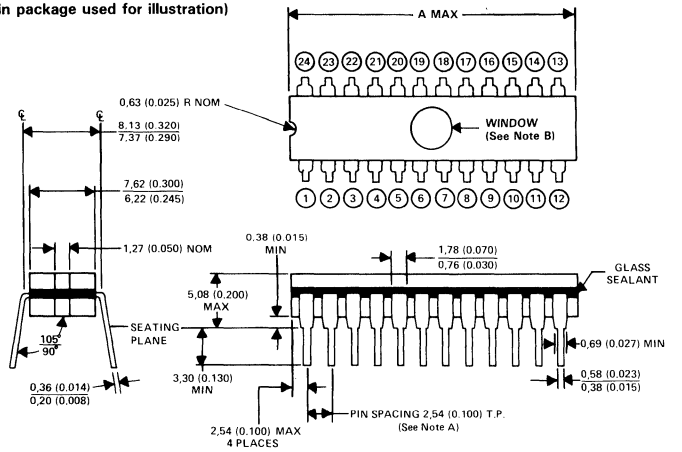


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. The window is present only on UV-eraseable products.

JT024 and JT028 ceramic dual-in-line packages

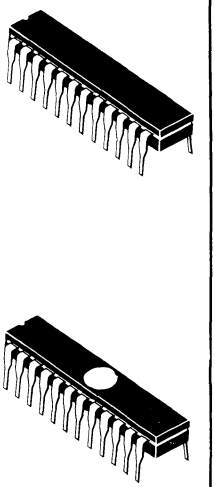
Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. These packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-coated leads require no additional cleaning or processing when used in soldered assembly.

JT024 and JT028
(24-Pin package used for illustration)



PINS / DIM	24	28
A (MAX)	32,51 (1.280)	37,95 (1.480)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

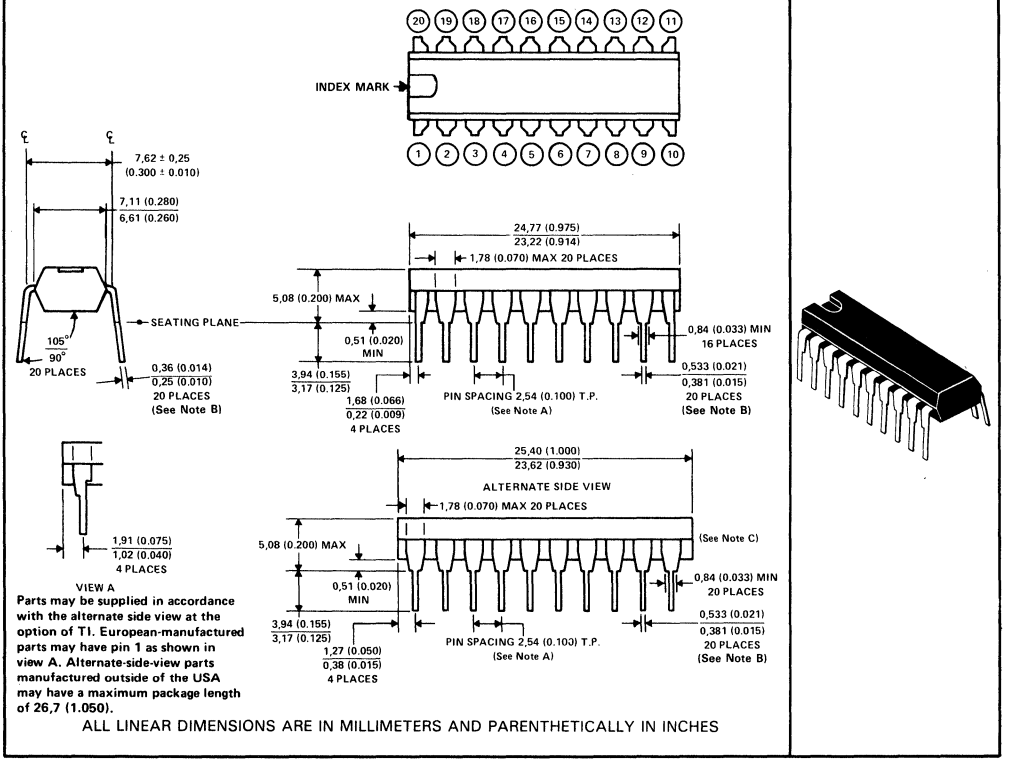


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. The window is present only on UV-eraseable products.

N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N020



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. When solder-coated leads are specified, coated area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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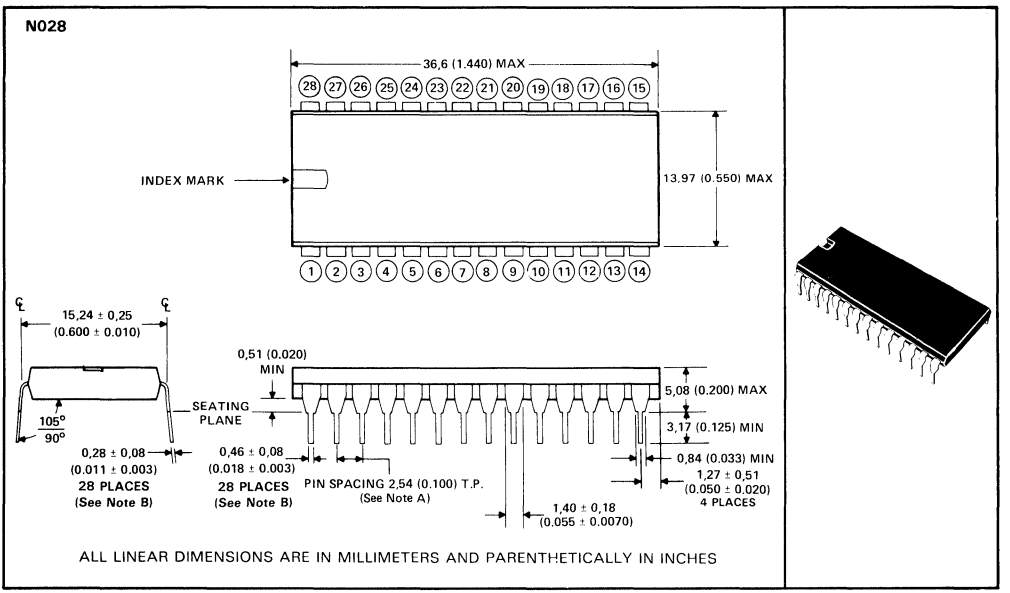
N028 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



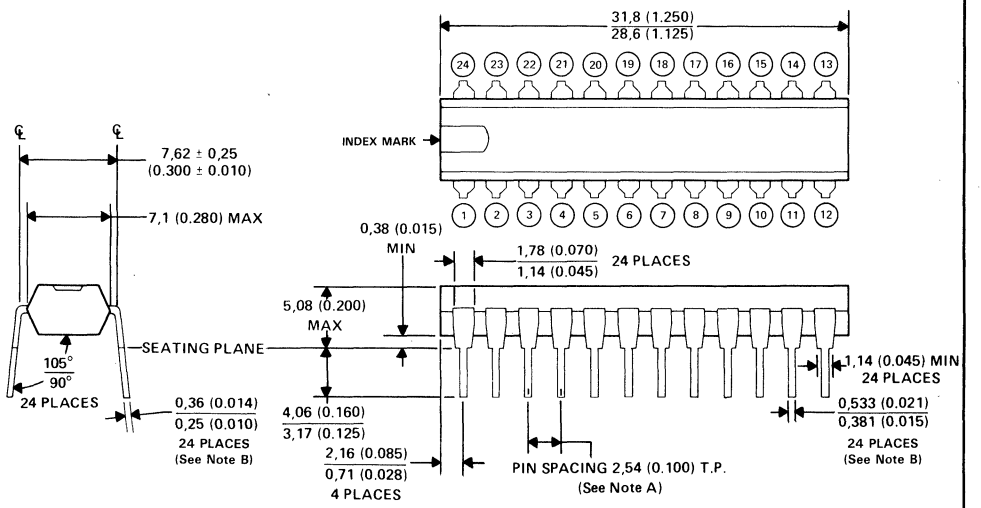
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. When solder-coated leads are specified, coated area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NT024 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

NT024



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. When solder-coated leads are specified, coated area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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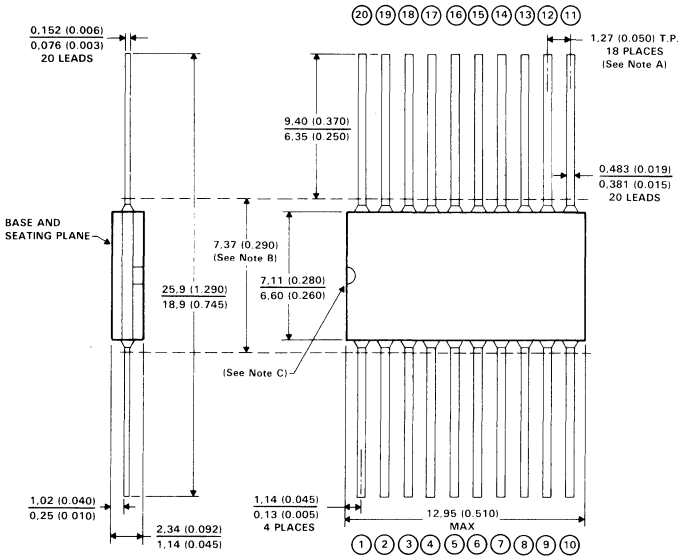
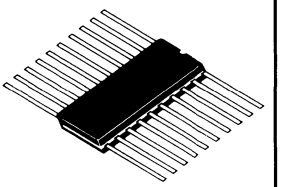
W020 ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

W020





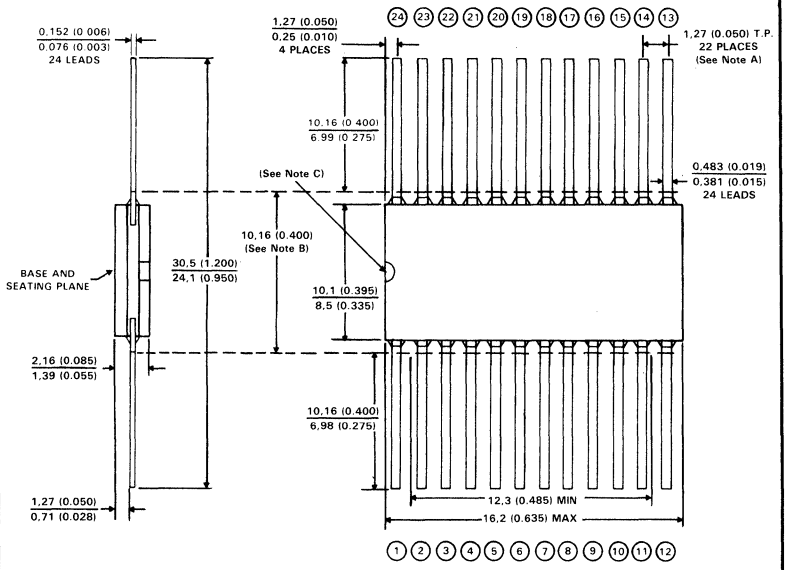
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

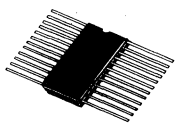
NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

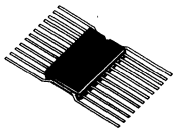
W024 ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

W024







Falls Within JEDEC MO-019AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

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NORTH CAROLINA: Charlotte: 8 Woodlawn Green, Woodlawn Rd., Charlotte, NC 28210, (704) 527-0933; **Raleigh:** 2809 Highwoods Blvd., Suite 100, Raleigh, NC 27625, (919) 876-2725.

OHIO: Beachwood: 23775 Commerce Park Rd., Beachwood, OH 44122, (216) 464-6100; **Beavercreek:** 4200 Colonel Glenn Hwy., Beavercreek, OH 45431, (513) 427-6200.

OREGON: Beaverton: 6700 SW 105th St., Suite 110, Beaverton, OR 97005, (503) 643-6758.

PENNSYLVANIA: Blue Bell: 670 Sentry Pkwy, Blue Bell, PA 19422, (215) 825-9500.

PUERTO RICO: Hato Rey: Mercantil Plaza Bldg., Suite 505, Hato Rey, PR 00918, (809) 753-8700.

TENNESSEE: Johnson City: Erwin Hwy, P.O. Drawer 1255, Johnson City, TN 37605 (615) 461-2192.

TEXAS: Austin: 12501 Research Blvd., Austin, TX 78759, (512) 250-7655; **Richardson:** 1001 E. Campbell Rd., Richardson, TX 75081, (214) 680-5082; **Houston:** 9100 Southwest Frwy., Suite 250, Houston, TX 77074, (713) 778-6592; **San Antonio:** 1000 Central Parkway South, San Antonio, TX 78232, (512) 496-1779.

UTAH: Murray: 5201 South Green St., Suite 200, Murray, UT 84123, (801) 266-8972.

WASHINGTON: Redmond: 5010 148th NE, Bldg B, Suite 107, Redmond, WA 98052, (206) 881-3080.

WISCONSIN: Brookfield: 450 N. Sunny Slope, Suite 150, Brookfield, WI 53005, (414) 782-2899.

CANADA: Nepean: 301 Moodie Drive, Mallorn Center, Nepean, Ontario, Canada, K2H9C4, (613) 726-1970. **Richmond Hill:** 280 Centre St. E., Richmond Hill L4C1B1, Ontario, Canada (416) 884-9181; **St. Laurent:** Ville St. Laurent Quebec, 9460 Trans Canada Hwy., St. Laurent, Quebec, Canada H4S1R7, (514) 336-1860.

ARGENTINA: Texas Instruments Argentina Viamonte 1119, 1053 Capital Federal, Buenos Aires, Argentina, 541/748-3699

AUSTRALIA (& NEW ZEALAND): Texas Instruments Australia Ltd.: 6-10 Talavera Rd., North Ryde (Sydney), New South Wales, Australia 2113, 2 + 887-1122; 5th Floor, 418 St. Kilda Road, Melbourne, Victoria, Australia 3004, 3 + 267-4677; 171 Philip Highway, Elizabeth, South Australia 5112, 8 + 255-2066.

AUSTRIA: Texas Instruments Ges.m.b.H.: Industriestrabe B/16, A-2345 Brunn/Gebirge, 2236-846210.

BELGIUM: Texas Instruments N.V. Belgium S.A.: 11, Avenue Jules Bondetlaan 11, 1140 Brussels, Belgium, (02) 242-3080.

BRAZIL: Texas Instruments Electronicos do Brasil Ltda.: Rua Paes Leme, 524-7 Andar Pinheiros, 05424 Sao Paulo, Brazil, 0815-6166.

DENMARK: Texas Instruments A/S, Mairelundvej 46E, 2730 Herlev, Denmark, 2 - 91 74 00.

FINLAND: Texas Instruments Finland OY: Ahertajantie 3, P.O. Box 81, ESP00, Finland, (90) 0-461-422.

FRANCE: Texas Instruments France: Paris Office, BP 67 8-10 Avenue Morane-Saulnier, 78141 Velizy-Villacoublay cedex (1) 30 70 1003.

GERMANY (Fed. Republic of Germany): Texas Instruments Deutschland GmbH: Haggertystrasse 1, 8050 Freising, 8161 + 80-4591; Kurfuerstendamm 195/196, 1000 Berlin 15, 30 + 882-7365; Ill, Hagen 43/Kibbelstrasse, 19, 4300 Essen, 201-24250; Kirchhorsterstrasse 2, 3000 Hannover 51, 511 + 648021; Maybachstrabe 11, 7302 Ostfildern 2-Nelingen, 711 + 34030.

TEXAS INSTRUMENTS

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