TEXAS INSTRUMENTS

ABT
Advanced BiCMOS Technology
A High-Performance Line of 5-V and 3.3-V Products

Data Book

1993

Advanced Bus-Interface and Management Logic

ABT
Advanced BiCMOS Technology Data Book

A High-Performance Line of 5-V and 3.3-V Products

TEXAS INSTRUMENTS

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INTRODUCTION

As the operating frequencies of microprocessors increase, the period of time allotted for memory access, arithmetic computation, or similar operations decreases. With this in mind, a new series of advanced bus-interface products, developed with the Texas Instruments submicron Advanced BiCMOS (ABT) process technology, assumes a prominent role as the key high-performance logic needed in today's workstation, personal and portable computer, and telecom systems. The goal of this family of products is to provide to system designers a bus-interface solution combining high-drive capability, lower power consumption, signal integrity, and propagation delays fast enough to appear transparent with respect to overall system performance. Fine-pitch package options simplify layout, reduce required board space, and decrease overall system costs. Novel circuit design techniques add value over competitive solutions.

Texas Instruments presents the 1993 ABT Advanced BiCMOS Technology Data Book. Included in this updated edition is the broadest line of advanced bus products in the industry. As new bus architectures and logic standards are being developed, Texas Instruments continues to lead the industry in producing advanced logic to support these emerging technologies. Products such as enhanced transceiver logic (ETL), Gunning transceiver logic (GTL), low-voltage JTAG, and LVT memory drivers have been added to illustrate this technology leadership. Data sheets have also been added to other sections to reflect new products under development. All of the devices contained in this data book incorporate the Texas Instruments high-performance EPIC-IIB™ submicron BiCMOS process.

The products described in this data book have been designed specifically to help system engineers meet the varied and stringent requirements of their end equipments. Products range from the simple and popular octal buffer/transceiver to the extremely complex 36-bit universal bus transceiver (UBT™). For midscale integration, a whole series of 16-bit Widebus™ products exist. Because board costs also affect system costs, it is desirable for chips to be housed in a variety of packaging options to save space. Each of the products in the data book are offered in a number of different surface-mount and fine-pitch package options such as the shrink small-outline package (SSOP) and the thin shrink small-outline package (TSSOP). Circuit design techniques built into the silicon such as mixed mode, power on demand, and bus hold offer enhanced parametrics and save having to discretely implement these enhancements.

Most of the products in the data book are available in production quantities. Please contact your local authorized distributor or Texas Instruments representative for details on any of these devices. Some of the devices in this data book are not yet available in production quantities; information on these devices is included as Product Previews. Texas Instruments is also evaluating many other devices for market introduction. Some of these are listed along with a description of their function in tables at the front of each section. Please contact the Advanced System Logic hotline at (214) 997-5202 to learn more about plans for these devices.

Finally, in addition to specific information on the products, the data book contains other useful sections including mechanical data, application notes, and characterization information.

We hope you agree that Texas Instruments has the most complete line of high-performance bus-interface logic in the industry. We hope that these products will meet your system and design needs.

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Contents

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i **Input capacitance**

The internal capacitance at an input of the device

C_o **Output capacitance**

The internal capacitance at an output of the device

C_{pd} **Power dissipation capacitance**

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} **Maximum clock frequency**

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**

The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} **Supply current change**

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}

I_{CEX} **Output high leakage current**

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_O = 5.5$ V.

$I_{I(hold)}$ **Input hold current**

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

I_{IH} **High-level input current**

The current into* an input when a high-level voltage is applied to that input

I_{IL} **Low-level input current**

The current into* an input when a low-level voltage is applied to that input

I_{off} **Input/output power-off leakage current**

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and $V_{CC} = 0$ V

I_{OH} **High-level output current**

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

*Current out of a terminal is given as a negative value.

I_{OZ} **Off-state (high-impedance-state) output current (of a 3-state output)**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output.

t_a **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_{dis} **Disable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them $t_{en} = t_{PHL}$.

t_h **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

t_{pd} **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to a high-impedance (off) state

t_{PLH} **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

t_{PLZ} **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to a high-impedance (off) state

t_{PZH} **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined low level.

t_{su} **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{IL} **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎴	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎴, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

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Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	L	L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

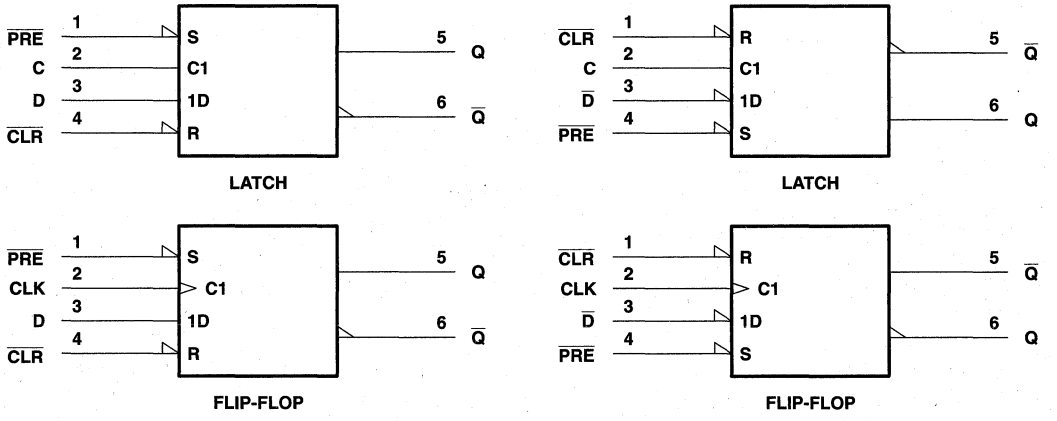
The function table functional tests do not reflect all possible combinations or sequential modes.

D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊾) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

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In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the ABT family. In general, the junction temperature for any device can be calculated using using the following equation.

$$T_J = R_{\theta JA} \times P_t + T_A$$

where:

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
P_t = total power dissipation of the device (see Section 15, package thermal considerations)
T_A = free-air temperature

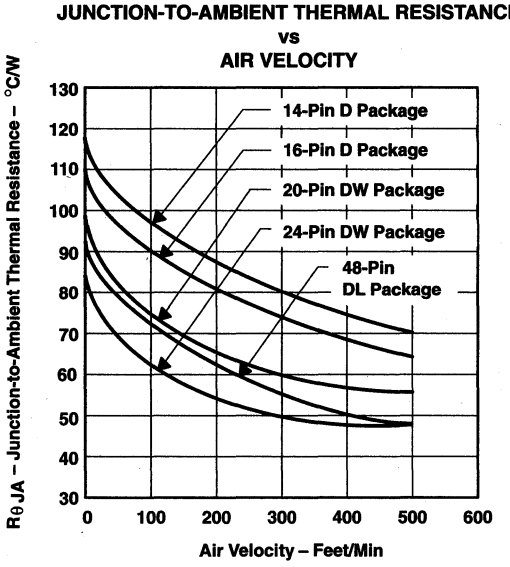


Figure 1

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

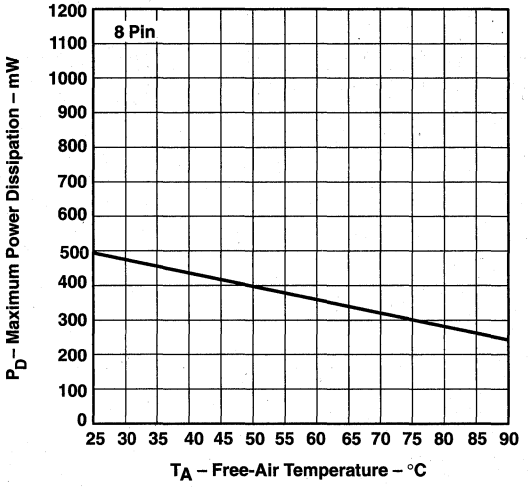


Figure 2

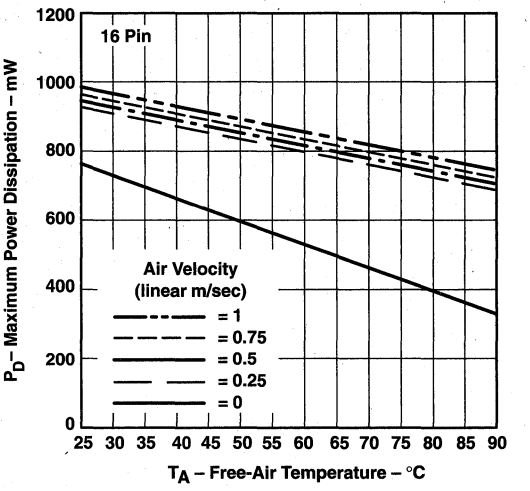


Figure 3

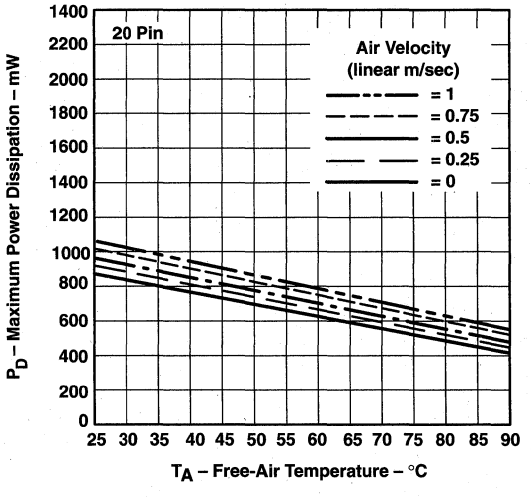


Figure 4

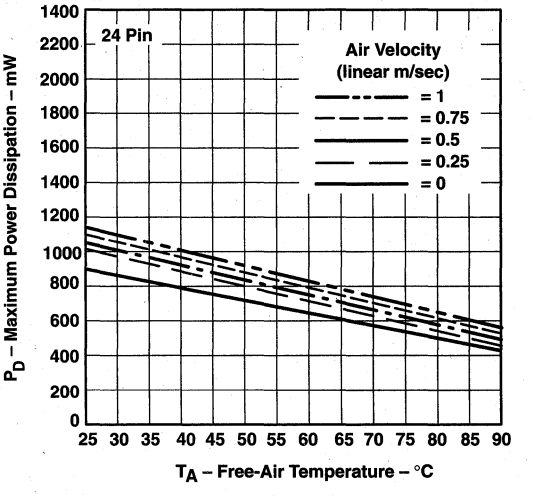


Figure 5

The following tables outline the logic functions Texas Instruments offers in a variety of technologies. The tables are organized by function type and list all available or planned options of that function. The technology columns identify the appropriate family and a particular data book where more information can be found. The applicable literature number, composed of either seven or eight alphanumeric characters, can be found at the lower right-hand corner on the back cover of each publication.

List of additional Advanced System Logic data books:

AC and ACT Devices	Advanced CMOS Logic Data Book	SCAD001C
ALS and AS Devices†	ALS/AS Logic Data Book	SDAD001B
BCT Devices†	BiCMOS Bus-Interface Logic Data Book	SCBD001B
F Devices†	F Logic (SN54/74F) Data Book	SDFD001A
FIFO Devices†	High-Performance FIFO Memories Data Book	SCAD003
HC and HCT Devices	High-Speed CMOS Logic Data Book	SCLD001C
LV, LVC, LVT, and ALVC Devices†	Low-Voltage Logic Data Book	SCBD003
SCOPE™ Devices	SCOPE™ Product Information	SSYV001
Std TTL, LS, and S Devices	TTL Logic Data Book	SDLD001A

† Updated data book planned for this technology.

Contents

Contents (continued)

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

GATES

Positive-NAND Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
8-Input		'30	✔	✔	✔								
		'11030						✔	✔				
13-Input		'133	✔			✔							
Dual 2-Input		'8003	✔										
Dual 4-Input		'20	✔	✔	✔	✔							
		'40	✔										
		'11020						✔	✔				
Triple 3-Input		'10	✔	✔	✔	✔							+
		'1010	✔										
		'11010						✔	✔				
Quad 2-Input		'00	✔	✔	✔	✔	✔					✔	+
		'11000						✔	✔				
		'37	✔										
	OC	'38	✔		✔								
		'132				✔							
		'11132						✔	✔				
		'1000		✔									
Hex 2-Input		'804	✔	✔									
Quad 2-Input	OC	'01	✔			✔							
		'03	✔			✔							

Positive-AND Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Quad 2-Input	OC	'09	✔			✔							
		'7001				✔							
Dual 4-Input		'21	✔	✔	✔	✔							
		'11021						✔	✔				
Triple 3-Input		'11	✔	✔	✔	✔							
		'11011						✔	✔				
Quad 2-Input		'08	✔	✔	✔	✔	✔					✔	+
		'1008		✔									
		'11008						✔	✔				
Hex 2-Input		'808		✔									

✔ Product available in technology indicated
+ New product planned in technology indicated

GATES (continued)

Positive-OR/NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Triple 3-Input		'4075				✔							
Quad 2-Input		'32	✔	✔	✔	✔	✔					✔	+
		'1032		✔									
		'11032						✔	✔				
		'7032				✔							
Hex 2-Input		'832	✔	✔		✔							
Dual 5-Input		'260			✔								
Triple 3-Input		'27	✔	✔	✔	✔							
		'11027						✔	✔				
Quad 2-Input		'02	✔	✔	✔	✔	✔					✔	+
	OC	'33	✔										
		'7002				✔							
		'11002						✔	✔				
Hex 2-Input		'805	✔	✔		✔							

OR/NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Quad 2-Input Exclusive-OR Gates With Totem-Pole Outputs		'86	✔	✔	✔	✔							+
		'11086						✔	✔				
Quad 2-Input Exclusive-OR Gates	OC	'136	✔										
Quad 2-Input Exclusive-NOR Gates	OD	'266				✔							
		'810	✔										
	OC	'811	✔										

AND-OR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual 2-Wide 2-Input, 3-Input		'51			✔						

✔ Product available in technology indicated
+ New product planned in technology indicated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

INVERTING/NONINVERTING BUFFERS

Hex Inverters/Noninverters

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Hex Inverters		'04	✔	✔	✔	✔	✔					✔	+
		'U04				✔						✔	+
		'11004						✔	✔				
	OC	'05	✔			✔							
		'14				✔						✔	+
		'11014						✔	✔				
		'1004	✔	✔									
		'1005	✔										
Hex Noninverters		'11034						✔	✔				
	OC	'35	✔										
		'1034	✔	✔									
	OC	'1035	✔										

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Buffers/Drivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Quad Buffers/Drivers	3S	'125			✔	✔	✔			✔	✔	✔		+	
		'126			✔	✔				✔	✔				
Noninverting Hex Buffers/Drivers	3S	'365				✔									
		'367				✔									
Inverting Hex Buffers/Drivers	3S	'368				✔									
Noninverting Octal Buffers/Drivers	3S	'241	✔	✔	✔	✔	✔			✔	✔				
		'11241						✔	✔						
		'25241									+				
		'244	✔	✔	✔	✔	✔			✔	✔		✔	+	
		'244A										✔			
		'11244						✔	✔						
		'1244	✔												
		'25244								✔	+				
		'541	✔		✔	✔	✔			✔	✔			+	
	OC	'757		✔						✔					
		'760	✔	✔						✔					
		'25760								+					
Inverting Octal Buffers/Drivers	3S	'240	✔	✔	✔	✔	✔			✔	✔	✔	✔	+	
		'11240						✔	✔						
		'1240	✔												
		'25240								✔					
		'466	✔												
		'540	✔			✔	✔			✔	✔			+	
	OC	'756	✔	✔						✔					
		'763	✔	✔											
Inverting and Noninverting Octal Buffers/Drivers	3S	'230		✔											
	OC	'762		✔											
Triple 4-Input OR/NOR Drivers		'11802							✔						
Noninverting 10-Bit Buffers/Drivers	3S	'827									✔				
		'11827						✔	✔						
		'29827	✔							✔					
Inverting 10-Bit Buffers/Drivers	3S	'828									+				
		'11828						✔	✔						
		'29828	✔							✔					
Noninverting 16-Bit Buffers/Drivers	3S	'16241							✔		✔				
		'16244						✔	✔		✔			+	+
		'16244A										✔			
		'16541							✔		✔				

✔ Product available in technology indicated
+ New product planned in technology indicated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

BUFFERS/DRIVERS AND BUS TRANSCEIVERS (continued)

Buffers/Drivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Inverting 16-Bit Buffers/Drivers	3S	'16240						✔	✔		✔			+	+
		'16540							✔		✔				
Noninverting 18-Bit Buffers/Drivers	3S	'16825							✔		✔				
Inverting 18-Bit Buffers/Drivers	3S	'16826									+				
Noninverting 20-Bit Buffers/Drivers	3S	'16827							✔		✔				+
Inverting 20-Bit Buffers/Drivers	3S	'16828									+				+
Octal Buffers/Drivers With Input Pullup Resistors		'746	✔												

Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY							
			AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting 18-Bit Universal Bus Transceivers (UBT™)	3S	'16500					+			+
		'16500B				✔				
Noninverting 18-Bit Universal Bus Transceivers (UBT™)	3S	'16501				✔	+		+	+
		'16600				✔				+
		'16601				✔				+
Noninverting 36-Bit Universal Bus Transceivers (UBT™)	3S	'32501				✔				
Noninverting 16-Bit Tri-Port Universal Bus Exchangers (UBE™)	3S	'32316				✔				
Noninverting 18-Bit Tri-Port Universal Bus Exchangers (UBE™)	3S	'32318				✔				
18-Bit Universal Bus Transceivers (UBT™) With Series Resistors on B Port	3S	'162500				+				
		'162501				+				
		'162600				+				
		'162601				✔				
SCOPE™ 18-Bit Universal Bus Transceivers (UBT™)	3S	'18502				✔	+			
SCOPE™ 20-Bit Universal Bus Transceivers (UBT™)	3S	'18504				✔	+			

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS (continued)

Bus Transceivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting Quad Transceivers	3S	'243	✔		✔										
Inverting Quad Transceivers	OC	'758	✔												
	3S	'242			✔										
Noninverting Octal Transceivers	3S	'245	✔	✔	✔	✔	✔			✔	✔	✔	✔	+	
		'1245	✔												
		'11245						✔	✔						
		'25245								✔	✔				
		'645	✔	✔		✔	✔								
		'1645	✔												
	OC	'621	✔		✔										
		'641	✔	✔											
	OC/3S	'639	✔	✔											
Inverting Octal Transceivers	3S	'620	✔							✔	✔				
		'623	✔	✔	✔	✔	✔			✔	✔				
		'11623							✔						
		'640	✔	✔		✔				✔	✔				
		'1640	✔												
		'11640							✔						
	OC	'642	✔												
		'25642								✔					
	OC/3S	'638	✔	✔											
Noninverting 9-Bit Transceivers	3S	'863									✔			+	
		'29863	✔							✔					
Inverting 9-Bit Transceivers	3S	'29864								✔					
Noninverting 10-Bit Transceivers	3S	'861									+				
		'29861								✔					
Inverting 10-Bit Transceivers	3S	'29862								✔					
Noninverting 16-Bit Transceivers	3S	'16245						✔	✔		✔	✔		+	+
		'16623						✔	✔		✔				
Inverting 16-Bit Transceivers	3S	'16640						✔	✔		✔				
		'16620						✔	✔		+				
Noninverting 18-Bit Transceivers	3S	'16863							✔		✔				
Inverting 18-Bit Transceivers	3S	'16864									+				

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS (continued)

Bus Transceivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting 20-Bit Transceivers	3S	'16861							✔		+				
Inverting 20-Bit Transceivers	3S	'16862									+				
Noninverting Octal Registered Transceivers	3S	'11470							✔						
		'543			✔					✔	✔	✔		+	
		'11543							✔						
		'646	✔	✔		✔	✔			✔	✔	✔		+	
		'646A									✔				
		'11646						✔	✔						
		'652	✔	✔		✔	✔			✔	✔	✔		+	
		'11652						✔	✔						
		'2952								✔	+	✔		+	
		'2952A									✔				
	OC/3S	'653	✔												
		'654	✔												
Inverting Octal Registered Transceivers	3S	'544								✔	+				
		'11544							✔						
		'648	✔	✔						✔	+				
		'11648							✔						
		'651	✔	✔						✔	✔				
		'2953								✔	+				
Noninverting 16-Bit Registered Transceivers	3S	'16470							✔		✔				
		'16543						✔	✔		✔	+		+	+
		'16646						✔	✔		✔	+		+	+
		'16652						✔	✔		✔	+		+	+
		'16952							✔		✔	+		+	+
Inverting 16-Bit Registered Transceivers	3S	'16471									+				
		'16544							✔		+				
		'16648							✔		+				
		'16651							✔		+				
		'16953									+				

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS (continued)

Bus Transceivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting 18-Bit Registered Transceivers	3S	'16472						✔							
		'16474							✔						
		'16500									✔	+		+	+
		'16501									✔	+		+	+
		'16600									✔				+
		'16601									✔				+
Inverting 18-Bit Registered Transceivers	3S	'16475							✔						
Noninverting 36-Bit Transceivers	3S	'32245									+				
Noninverting 36-Bit Registered Transceivers	3S	'32501									✔				
		'32543									✔				
8-/9-Bit Bus Transceivers With Parity Checkers/ Generators	3S	'657			✔					✔	+				
		'659					✔								
		'833									+				
		'834									+				
		'853									+				
		'854									+				
		'899								✔					
	3S/OC	'29833	✔							✔					
		'29834								✔					
		'29853	✔							✔					
		'29854	✔							✔					
Dual 8-/9-Bit Bus Transceivers With Parity Checkers/ Generators	3S	'16833							✔		✔				
		'16657							✔		✔				
		'16853									✔				
Universal Transceivers/Port Controllers	3S	'856		✔											
Noninverting 16-Bit Tri-Port Registered Bus Exchangers	3S	'32316									✔				
Noninverting 18-Bit Tri-Port Registered Bus Exchangers	3S	'32318									✔				

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS (continued)

MOS Memory Drivers/Transceivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Octal Transceivers With Series Resistors on Output	3S	'2623		✔							
Octal Buffers/Drivers With Series Resistors on Output	3S	'2240	✔							✔	✔
		'2241								✔	✔
		'2244								✔	✔
		'2541	✔								
Octal Transceivers With Series Resistors on B Port	3S	'2245								✔	+
Octal Latches With Series Resistors on Output	3S	'2574								+	
10-Bit Buffers/Drivers With Series Resistors	3S	'2827								✔	
		'2828								✔	
11-Bit Buffers/Drivers With Series Resistors	3S	'2410								✔	
		'2411								+	
		'5400									✔
		'5401									✔
12-Bit Buffers/Drivers With Series Resistors	3S	'5402									✔
		'5403									✔
16-Bit Buffers/Drivers With Series Resistors	3S	'162240									+
		'162244									✔
16-Bit Transceivers With Series Resistors	3S	'162245									+
18-Bit Universal Bus Transceivers (UBT™) With Series Resistors on B Port	3S	'162500									+
		'162501									+
		'162600									+
		'162601									✔
12-to-24 Multiplexed D-Type Latches With Series Resistors on B Port	3S	'162260									✔

✔ Product available in technology indicated
+ New product planned in technology indicated

TESTABILITY BUS-INTERFACE CIRCUITS

JTAG/IEEE 1149.1 Testability Circuits

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY							
				F	HC	HCT	AC	ACT	BCT	ABT	LVT
Buffers/Drivers	8	3S	'8240A						✔		
			'8244A						✔		
Transceivers	8	3S	'8245							✔	
			'8245A						✔		
	18	3S	'18245							✔	+
Transparent Latches	8	3S	'8373A						✔		
Flip-Flops	8	3S	'8374A						✔		
Registered Transceivers	8	3S	'8543							✔	
			'8646							✔	
			'8652							✔	
			'8952							✔	
	18	3S	'18502							✔	+
			'18646							✔	
			'18652							+	
	20	3S	'18504							✔	+
Test Bus Controllers		3S	'8990					✔			
Digital Bus Monitors		3S	'8994					✔			
Scan Path Linkers With Identification Buses	4	3S	'8997					✔			
	8	3S	'8999					✔			

✔ Product available in technology indicated
\+ New product planned in technology indicated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FLIP-FLOPS AND LATCHES

Flip-Flops

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Dual J-K Edge Triggered		'73				✔									
		'76				✔									
		'109	✔	✔	✔	✔									
		'11109						✔	✔						
		'112	✔		✔	✔								+	
		'11112						✔	✔						
		'113	✔			✔									
		'114	✔												
Dual D-Type		'74	✔	✔	✔	✔	✔						✔	+	
		'11074						✔	✔						
Dual D-Type With 2-Input NAND/NOR Gates		'7074				✔									
		'7075				✔									
		'7076				✔									
Dual 4-Bit D-Type Edge Triggered	3S	'874	✔	✔											
		'11874							✔						
		'876	✔	✔											
		'879	✔	✔											
Quad D-Type		'173				✔									
		'175	✔	✔	✔	✔									
		'11175						✔	✔						
Hex D-Type		'174	✔	✔	✔	✔							✔		
		'11174						✔	✔						
		'378			✔	✔									
Octal D-Type True Data	3S	'374	✔	✔	✔	✔	✔			✔	✔		+	+	
		'11374						✔	✔						
		'574	✔	✔	✔	✔	✔			✔	✔	✔	+	+	
Octal D-Type True Data With Clear		'273	✔			✔	✔				✔	✔	+		
		'11273						✔	✔						
	3S	'575	✔	✔											
		'874	✔	✔											
Octal D-Type True Data With Clock Enable		'377			✔	✔	✔				✔				
		'11377						✔	✔						
Octal D-Type Inverting	3S	'534	✔	✔		✔				✔	✔				
		'11534						✔	✔						
		'564	✔												
		'576	✔	✔											
		'29826								✔					

✔ Product available in technology indicated
+ New product planned in technology indicated

FLIP-FLOPS AND LATCHES (continued)

Flip-Flops (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Octal Dual-Ranked True Data	3S	'4374		✔											
Octal Inverting With Clear	3S	'577	✔												
		'879	✔	✔											
Octal Inverting With Preset	3S	'876	✔	✔											
Octal True Data	3S	'825		✔											
		'11825							✔						
		'29825								✔					
9-Bit True Data	3S	'823		✔							+			+	
		'29823	✔							✔					
9-Bit Inverting	3S	'824		✔											
		'29824	✔												
10-Bit True Data	3S	'821		✔							✔			+	
		'1821		✔											
		'11821							✔						
		'29821	✔							✔					
10-Bit Inverting	3S	'29822								✔					
16-Bit D-Type True Data With Clock Enable		'16377									+				
16-Bit Noninverting	3S	'16374						✔	✔		✔	+		+	+
16-Bit Inverting	3S	'16534									+				
18-Bit Noninverting	3S	'16823							✔		✔				+
20-Bit Noninverting	3S	'16821							✔		✔				+

✔ Product available in technology indicated
+ New product planned in technology indicated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FLIP-FLOPS AND LATCHES (continued)

Latches

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY												
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Bistable	4		'75				✔									
			'375				✔									
D-Type Edge Triggered Inverting and Noninverting	8		'996	✔												
D-Type Transparent Readback Latch, True	8	3S	'990	✔												
	9	3S	'992	✔												
	10	3S	'994	✔												
D-Type Transparent With Clear, True Outputs	8	3S	'666	✔												
D-Type Transparent With Clear, Inverting Outputs	8	3S	'667	✔												
D-Type Transparent True	8	3S	'373	✔	✔	✔	✔	✔			✔	✔		+	+	
			'11373						✔	✔						
			'573	✔	✔	✔	✔	✔			✔	✔	✔	+	+	
	16	3S	'16373						✔	✔		✔	+		+	+
			'16373A									✔				
	32	3S	'32373									+				
D-Type Dual 4-Bit Transparent True	8	3S	'873	✔	✔											
			'11873						✔							
D-Type Transparent Inverting	8	3S	'533	✔	✔						✔	✔				
			'11533						✔	✔						
			'563	✔			✔									
			'580	✔	✔											
	16	3S	'16533									+				
Dual 4-Bit Transparent Inverting	8	3S	'880	✔	✔											
2-Input Multiplexed	8	3S	'604				✔									
Addressable	8	2S	'259	✔			✔									
		Q	'4724				✔									

✔ Product available in technology indicated
+ New product planned in technology indicated

FLIP-FLOPS AND LATCHES (continued)

Latches (continued)

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY												
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
D-Type True Inputs	8	3S	'845	✔												
			'29845	✔												
	9	3S	'843	✔	✔							+			+	
			'1843		✔											
			'29843								✔					
	10	3S	'841	✔	✔							+			+	
			'29841	✔							✔					
	18	3S	'16843									+				+
	20	3S	'16841							✔		✔				+
D-Type Inverting Inputs	8	3S	'846	✔												
			'29846								✔					
	9	3S	'29844								✔					
	10	3S	'842	✔	✔											
			'29842	✔												

✔ Product available in technology indicated
+ New product planned in technology indicated

REGISTERS

Shift Registers

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY								
				ALS	AS	F	HC	HCT	AC	ACT	BCT	LV
Parallel In, Parallel Out, Bidirectional	4		'194		✔							
			'11194						✔	✔		
	8		'299	✔		✔						
			'323	✔								
Parallel In, Parallel Out	4		'195		✔							
Serial In, Parallel Out	8		'164	✔			✔					+
Parallel In, Serial Out	8		'165	✔			✔					
			'166	✔			✔					
Serial In, Parallel Out With Output Latches	8	3S	'594				✔					
			'595				✔					
Parallel Out	10		'11898						✔	✔		
Noninverting	8	3S	'299	✔								
	9	3S	'29823	✔								

Register Files

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual 16 Word × 4 Bits	3S	'870	✔								
		'871		✔							

✔ Product available in technology indicated
+ New product planned in technology indicated

COUNTERS

Synchronous Counters – Positive Edge Triggered

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
4-Bit Decade Up/Down	Sync	'568	✔							
4-Bit Binary	Sync	'161	✔	✔	✔	✔				
		'163	✔	✔	✔	✔				
		'561	✔							
4-Bit Binary Up/Down	Sync	'169	✔	✔	✔					
		'569	✔							
		'8169	✔							
	Async	'191	✔			✔				
		'11191						✔	✔	
		'193	✔			✔				
8-Bit Up/Down	Sync Clear	'869	✔	✔						
	Async Clear	'867	✔	✔						
		'11867							✔	
Divide-by-10 Counter	Sync	'4017				✔				

Asynchronous Counters (Ripple Clock) – Negative Edge Triggered

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
Dual 4-Bit Binary	None	'393				✔				
12-Bit Binary	Sync	'4040				✔				
14-Bit Binary	Sync	'4020				✔				
		'4060				✔				
		'4061				✔				

8-Bit Binary Counters With Registers

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
Parallel Register Outputs	3S	'590				✔				
		'11590						✔	✔	
Parallel Register Inputs	3S	'11593						✔	✔	

✔ Product available in technology indicated
✢ New product planned in technology indicated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

Encoders/Data Selectors/Multiplexers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Quad 2-to-1		'157	✔	✔	✔	✔	✔						+
		'11157						✔	✔				
		'158	✔	✔	✔	✔							
		'11158						✔	✔				
		'298		✔									
	3S	'257	✔	✔	✔	✔	✔						+
		'11257						✔	✔				
		'258	✔	✔	✔	✔							
		'11258							✔				
Dual 4-to-1		'153	✔	✔	✔	✔							
		'11153						✔	✔				
		'352	✔										
	3S	'253	✔	✔	✔	✔							
		'11253						✔	✔				
		'353		✔									
		'11353							✔				
Hex 2-to-1 Universal Multiplexer	3S	'857	✔										
8-to-1		'151	✔	✔	✔	✔							
		'11151						✔	✔				
	3S	'251	✔		✔	✔							
		'11251						✔					
		'354				✔							
16-to-1	3S	'250		✔									
		'850		✔									
		'851		✔									
Full BCD		'147				✔							
Cascadable Octal		'148				✔							

✔ Product available in technology indicated
+ New product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS (continued)

Decoders/Demultiplexers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Dual 2-to-4		'239				✔							
Dual 2-to-4		'139	✔			✔	✔						+
		'11139						✔	✔				
	OC	'156	✔										
3-to-8		'138	✔	✔	✔	✔	✔					✔	+
		'11138						✔	✔				
		'238					✔						
		'11238						✔	✔				
3-to-8 With Address Registers		'131		✔									
		'137	✔			✔							+
3-to-8 With Address Latches		'237				✔							
4-to-10 BCD-to-Decimal		'42				✔							
4-to-16		'154				✔							
4-to-16 With Address Latches		'4514				✔							
		'4515				✔							
Dual 2-to-4 for Battery Backed-Up Memories		'2414								✔			

Shifters

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Shifter	3S	'350			✔						

✔ Product available in technology indicated
+ New product planned in technology indicated

COMPARATORS AND PARITY GENERATORS/CHECKERS

Comparators

DESCRIPTION								TYPE	TECHNOLOGY							
INPUT	P=Q	$\overline{P=Q}$	P>Q	$\overline{P>Q}$	P<Q	OUTPUT	ENABLE		ALS	AS	F	HC	HCT	AC	ACT	BCT
8-Bit With 20-kΩ Pullup	Yes	No	No	No	No	OC	Yes	'518	✔							
	No	Yes	No	No	No	2S	Yes	'520	✔		✔					
								'11520						✔	✔	
	No	Yes	No	No	No	OC	Yes	'522	✔							
	No	Yes	No	Yes	No	2S	No	'682				✔				
8-Bit Standard	Yes	No	No	No	No	OC	Yes	'519	✔							
	No	Yes	No	No	No	2S	Yes	'521	✔		✔					
								'11521						✔	✔	
	No	Yes	No	Yes	No	2S	No	'684				✔				
	No	Yes	No	No	No	2S	Yes	'688	✔			✔				
8-Bit Latched P	No	No	Yes	No	Yes	2S	Yes	'885		✔						
8-Bit Latched P and Q	Yes	No	Yes	No	Yes	L	Yes	'866		✔						

Address Comparators

DESCRIPTION	OUTPUT ENABLE	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
16-Bit to 4-Bit	Yes	'677	✔								
12-Bit to 4-Bit	Yes	'679	✔								

Parity Generators/Checkers

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Odd/Even Generators/Checkers	9	'280	✔	✔	✔	✔					
		'11280						✔	✔		
		'286		✔							
		'11286						✔	✔		

✔ Product available in technology indicated
+ New product planned in technology indicated

BUS SWITCHES AND 5-V/3-V VOLTAGE TRANSLATORS

Crossbar Technology (CBT)

DESCRIPTION	TYPE	TECHNOLOGY
		CBT
Dual 4-Bit With '244 Pinout	'3244	+
8-Bit With '245 Pinout	'3245	+
10-Bit Bus Exchanger	'3383	+
Dual 5-Bit	'3384	+
10-Bit With Precharged Outputs for Live Insertion	'6800	+
18-Bit Bus Exchanger	'16209	+
24-Bit Bus Exchanger	'16212	+
12-Bit 3-to-1 Bus Select	'16214	+

ARITHMETIC CIRCUITS

Parallel Binary Adders

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit		'283			✔	✔					

Accumulators, Arithmetic Logic Units, Look-Ahead Carry Generators

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Arithmetic Logic Units: Function Generator		'181		✔							
		'11181							✔		
		'881		✔							
4-Bit Arithmetic Logic Units With Ripple Carry		'382			✔						

✔ Product available in technology indicated
+ New product planned in technology indicated

FIFO MEMORIES

First-In, First-Out Memories (FIFOs)

DESCRIPTION		OUTPUT	TYPE	TECHNOLOGY										
SIZE	TYPE†			LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
16 Words × 4 Bits	U	3S	'232B			✔								
16 Words × 5 Bits	U	3S	'225		✔									
			'229B			✔								
			'233B			✔								
32 Words × 9 Bits	B	3S	'2238			✔								
64 Words × 4 Bits	U	3S	'234			✔								
			'236			✔								
64 Words × 5 Bits	U	3S	'235			✔								
64 Words × 8 Bits	U	3S	'2232A			✔								
64 Words × 9 Bits	U	3S	'2233A			✔								
64 Words × 18 Bits	U, C	3S	'7813									✔		
	U	3S	'7814									✔		
64 Words × 36 Bits	B, C	3S	'3612											+
			'3614											+
	U, C	3S	'3611											+
			'3613											+
Dual 64 × 1	C	3S	'2226									✔		
			'2227									✔		
Dual 256 × 1	C	3S	'2228									✔		
			'2229									✔		
256 Words × 9 Bits	U	3S	'7200									✔		
256 Words × 18 Bits	U, C	3S	'7805									✔		
	U	3S	'7806									✔		
256 × 36 × 2 Bits	B, C	3S	'3622									+		
512 Words × 9 Bits	U	3S	'7201									✔		
	U, S	3S	'72211									✔		
512 Words × 18 Bits	U, C	3S	'7803									✔		
	U	3S	'7804									✔		
	B, C	3S	'7819											✔
	B	3S	'7820											✔
512 Words × 32 Bits	B, C	3S	'3638									+		
512 Words × 36 Bits	U, C	3S	'3631									+		
	B, C	3S	'3632									✔		

†U = Unidirectional
B = Bidirectional
C = Clocked
S = Synchronized
✔ Product available in technology indicated
+ New product planned in technology indicated

FIFO MEMORIES (continued)

First-In, First-Out Memories (FIFOs) (continued)

DESCRIPTION		OUTPUT	TYPE	TECHNOLOGY										
SIZE	TYPE†			LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
1K Words × 9 Bits	B	3S	'2235									✔		
			'2236									✔		
	U	3S	'7202									✔		
	U, S	3S	'72221									✔		
1K Words × 18 Bits	U, C	3S	'7801									✔		
			'7811									✔		
			'7881									+		
	U	3S	'7802									✔		
1K Words × 36 Bits	U, C	3S	'3641									+		
1K × 36 × 2 Bits	B, C	3S	'3642									+		
2K Words × 9 Bits	U, C	3S	'7807									✔		
	U	3S	'7203									+		
			'7808									✔		
	U, S	3S	'72231									✔		
2K Words × 18 Bits	U, C	3S	'7882									+		
2K Words × 36 Bits	U, C	3S	'3651									+		
4K Words × 9 Bits	U	3S	'7204									✔		
	U, S	3S	'72241									✔		
4K Words × 18 Bits	U, C	3S	'7884									+		

† U = Unidirectional
B = Bidirectional
C = Clocked
S = Synchronized

✔ Product available in technology indicated
\+ New product planned in technology indicated

CLOCK DISTRIBUTION CIRCUITS

Clock Distribution Circuits (CDC)

DESCRIPTION	TYPE	TECHNOLOGY								
		ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
3.3-V Hex Inverting Clock Drivers/Buffers	'203						✔			
Hex Inverting Clock Drivers/Buffers	'204						✔			
Dual 1-to-4 Clock Drivers/Buffers	'208							✔		
	'209						✔			
Octal Divide-by-2 Clock Drivers (6 Inverting, 2 Noninverting)	'303		✔							
Octal Divide-by-2 Clock Drivers (8 Noninverting)	'305		✔							
Octal Divide-by-2 Clock Drivers (4 Inverting, 4 Noninverting)	'304		✔							
1-to-6 Clock Drivers	'328									✔
	'328A									✔
	'329									✔
	'329A									✔
1-to-6 Clock Drivers With Output Enable	'391									✔
	'392									✔
1-to-8 Clock Drivers	'340									✔
	'341									✔
1-to-8, Divide-by-2 Clock Drivers	'337									✔
	'339									✔
Phase-Lock Loop 1-to-12 Clock Drivers	'582									+
	'586									+
	'2586									+

✔ Product available in technology indicated
+ New product planned in technology indicated

ECL TRANSLATORS

ECL-to-TTL or TTL-to-ECL Translators

DESCRIPTION	LEVEL TRANSLATION	OUTPUT	TYPE
Octal Bus Driver, Inverting	ECL-to-TTL	3S	10KHT5540
	TTL-to-ECL	OE	10KHT5542
Octal Bus Driver, Noninverting	ECL-to-TTL	3S	10KHT5541
	TTL-to-ECL	OE	10KHT5543
			100KT5543
Octal D-Type Latch, True	ECL-to-TTL	3S	10KHT5573
			100KT5573
Octal D-Type Flip-Flop, True	ECL-to-TTL	3S	10KHT5574
	TTL-to-ECL	OE	10KHT5578
			100KT5578

ABT OCTALS

Features

- EPIC-IIB™ BiCMOS process
- 0.8-µm CMOS core logic
- Bipolar output transistors
- Industry-standard corner-pin V_{CC} and GND pinout
- –40°/85° characterization
- DIP, SOIC, and EIAJ SSOP package options
- TI has established two alternate sources

Benefits

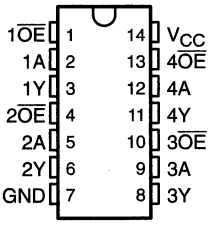
- Sub-5-ns maximum propagation delays for improved cycle time and performance
- Very low standby power consumption
- –32-/64-mA drive capability for high fanout and advanced backplane interface
- Drop-in replaceable to existing layouts and designs for easy upgradeability
- Industrial temperature range for field applications
- Flexible approaches for many board-space-saving needs
- Standardization that comes from a common product approach

The following table lists ABT octal devices currently being evaluated for market introduction. Customers interested in learning more about TI's plans for these devices should contact the Advanced System Logic Marketing hotline at (214) 997-5202.

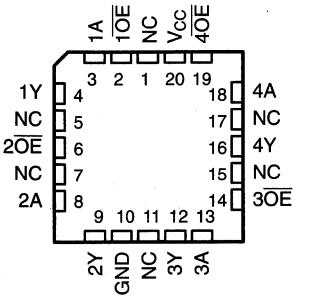
DEVICE	PIN COUNT	DESCRIPTION
'ABT563	20	Octal D-Type Transparent Latch
'ABT564	20	Octal D-Type Flip-Flop
'ABT648	24	Octal Registered Bus Transceiver
'ABT825	24	Octal Register
'ABT834	24	Octal Registered Bus Transceiver
'ABT845	24	Octal Latch
'ABT854	24	Octal Registered Bus Transceiver
'ABT864	24	9-Bit Transceiver

- **State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT125 . . . J PACKAGE
SN74ABT125 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54ABT125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT125 bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT125 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

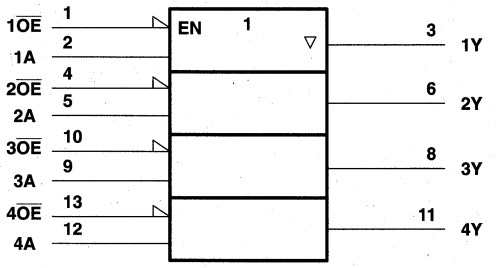
The SN54ABT125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

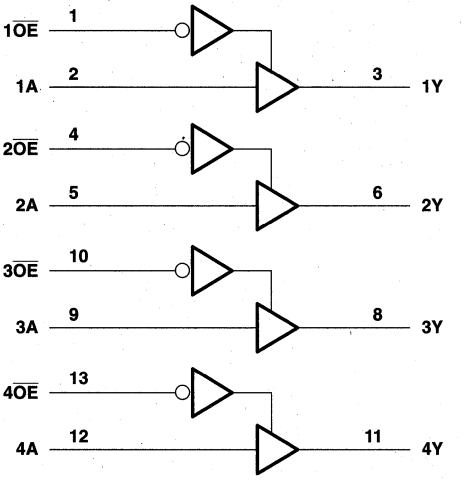
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT125 ..... 96 mA
SN74ABT125 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 0.7 W
DB package ..... 0.6 W
N package ..... 1.1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT125		SN74ABT125		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT125		SN74ABT125		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−200¶	−50	−200¶	−50	−200¶	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				7						pF

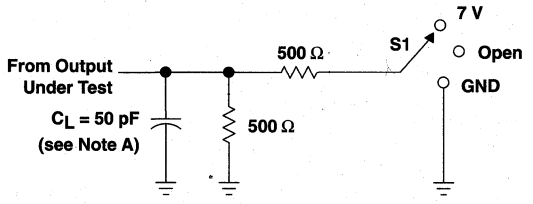
† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This data sheet limit may vary among suppliers.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT125		SN74ABT125		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}¶	A	Y	1	3.2	4.3	1	6.7	1	5.8	ns
t_{PHL}¶			1	3.7	4.9	1	6.2	1	5.9	
t_{PZH}¶	$\overline{OE}$	Y	1	3.6	4.8	1	6	1	5.9	ns
t_{PZL}¶			1	4.9	6.3	1	7.5	1	7.4	
t_{PHZ}	$\overline{OE}$	Y	1	3.5	5.4	1	6.3	1	6.2	ns
t_{PLZ}¶			1	3.3	5.3	1	7.2	1	6.3	

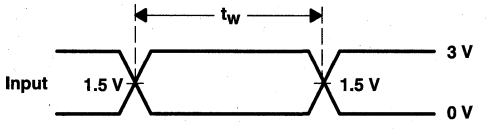
¶ This data sheet limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

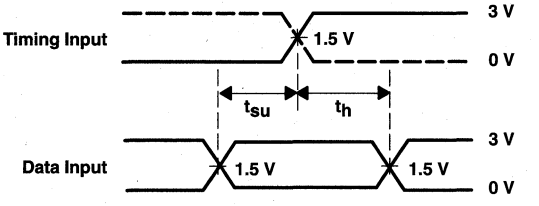


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

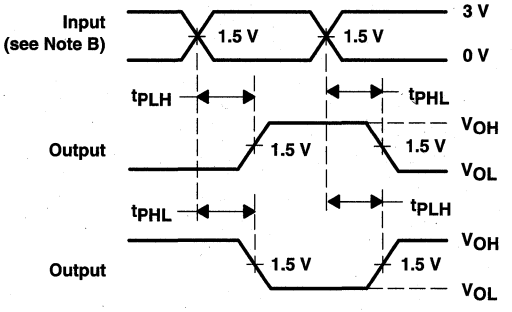
LOAD CIRCUIT FOR OUTPUTS



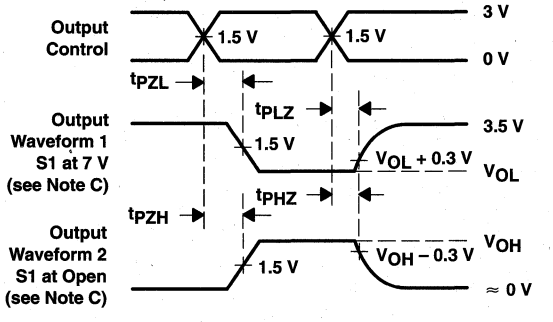
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



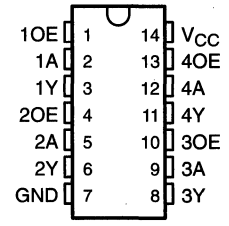
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O \doteq 50\ \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

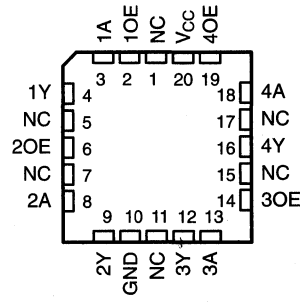
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT126 . . . J PACKAGE
SN74ABT126 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54ABT126 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT126 bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT126 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

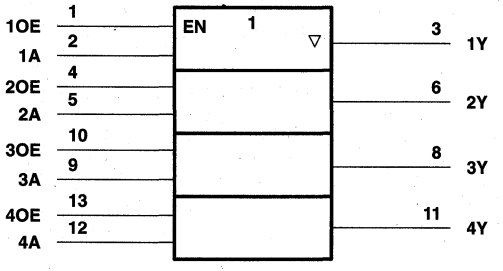
The SN54ABT126 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT126 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

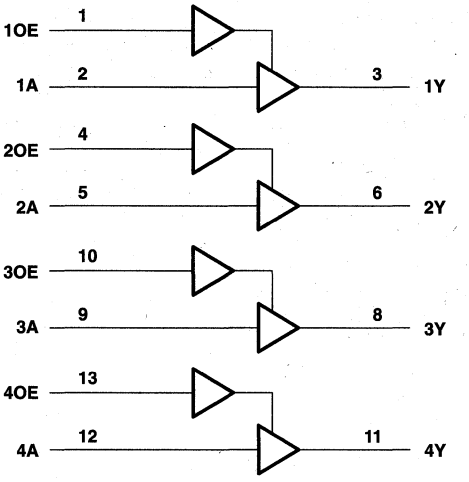
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT126 ..... 96 mA
SN74ABT126 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): D package ..... 0.7 W
DB package ..... 0.6 W
N package ..... 1.1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT126		SN74ABT126		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT126		SN74ABT126		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT126		SN74ABT126		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}†	A	Y	1	2.9	4.9	1	7.3	1	6.3	ns
t_{PHL}†			1	2.5	5.1	1	5.9	1	5.7	
t_{PZH}†	OE	Y	1	4.4	5.8	1	5.3	1	6.5	ns
t_{PZL}†			1	4.4	5.9	1	6.4	1	6.5	
t_{PHZ}†	OE	Y	1	3	5.7	1	6.9	1	6.8	ns
t_{PLZ}†			1	3	5.8	1	7.2	1	6.7	

† This data sheet limit may vary among suppliers.

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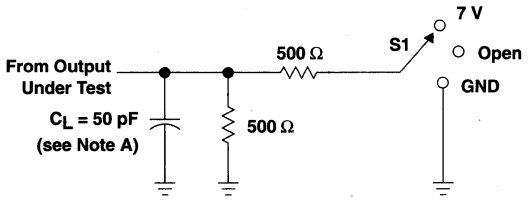
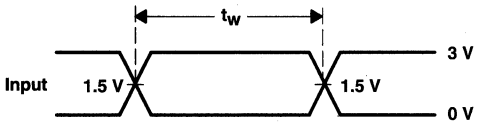
PARAMETER MEASUREMENT INFORMATION

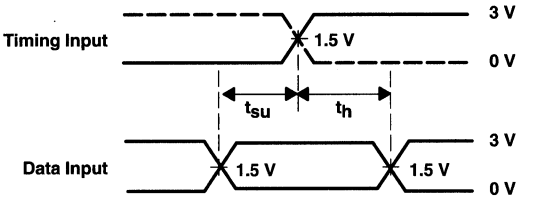


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

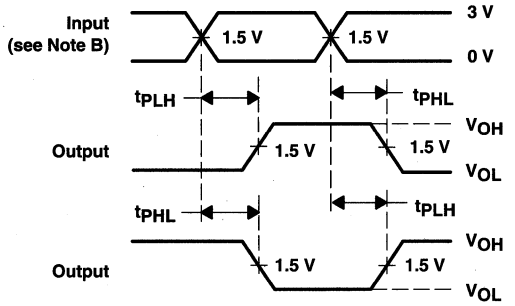
LOAD CIRCUIT FOR OUTPUTS



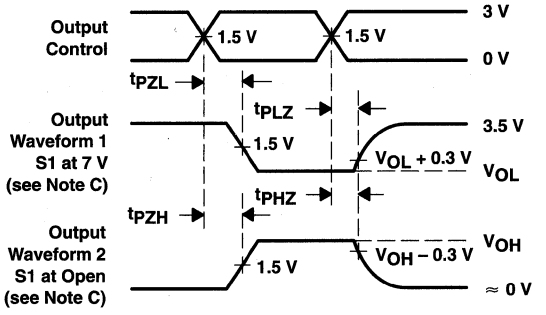
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



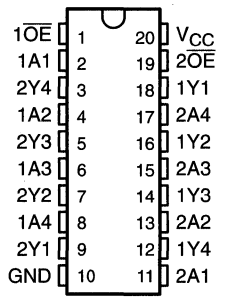
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

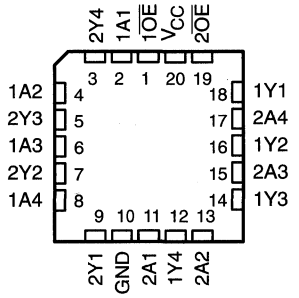
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT240 . . . J PACKAGE
SN74ABT240 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT241 and 'ABT244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs.

The 'ABT240 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

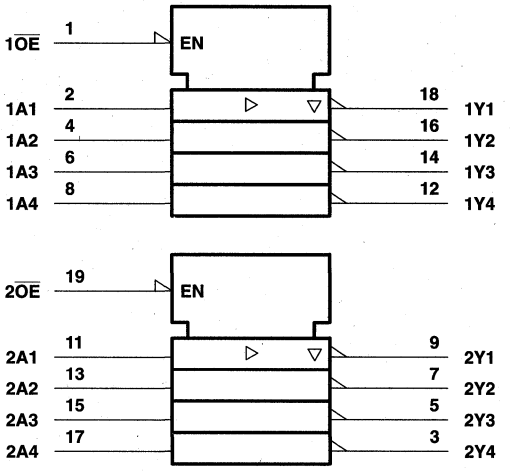
The SN54ABT240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

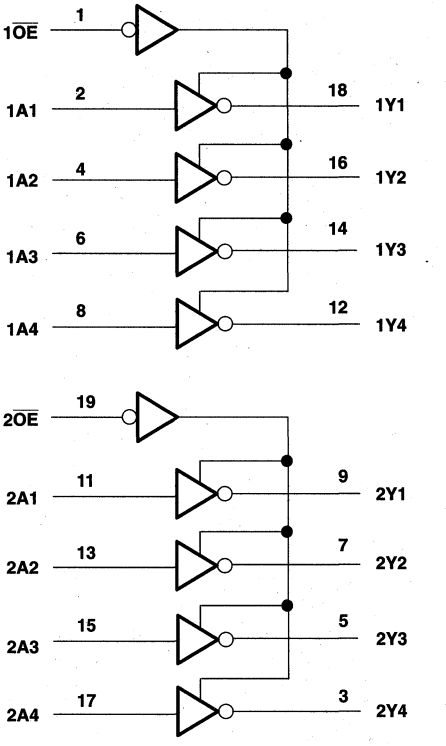
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT240 ..... 96 mA
SN74ABT240 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT240		SN74ABT240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

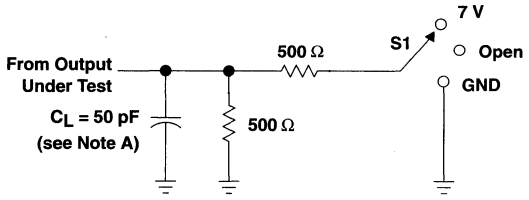
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT240		SN74ABT240		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = − 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = − 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = − 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				10§		10§		10§	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−10§		−10§		−10§	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

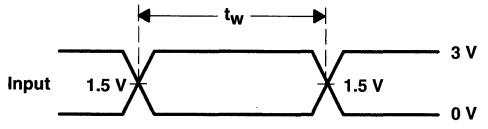
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT240		SN74ABT240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.9	4.1	0.8	5.5	1	4.8	ns
t_{PHL}			1.6	3.1	4.3	1	5.5	1.6	4.8	
t_{PZH}	$\overline{OE}$	Y	1.1	3.1	4.7	0.8	7.5	1.1	5.2	ns
t_{PZL}			1.1	2.7	5.8	0.8	7.7	1.1	6.2	
t_{PHZ}	$\overline{OE}$	Y	1.8	4.6	5.7	1.7	7	1.8	6.4	ns
t_{PLZ}			1.6	4	5.4	1.3	7.2	1.6	5.8	

PARAMETER MEASUREMENT INFORMATION

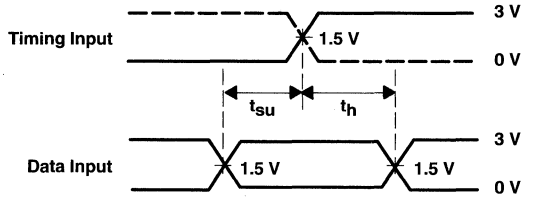


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

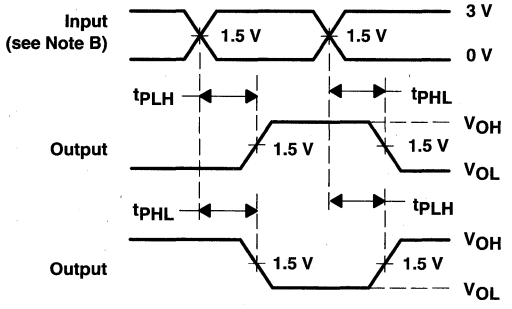
LOAD CIRCUIT FOR OUTPUTS



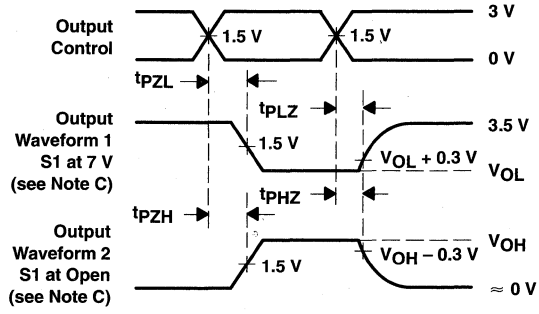
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



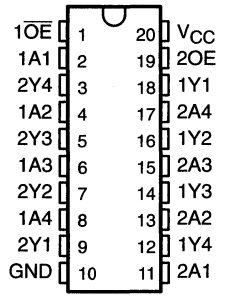
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

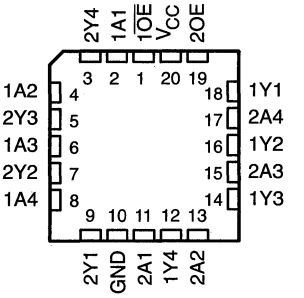
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT241 . . . J PACKAGE
SN74ABT241 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT241 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT240 and 'ABT244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT241 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT241 is characterized for operation from –40°C to 85°C.

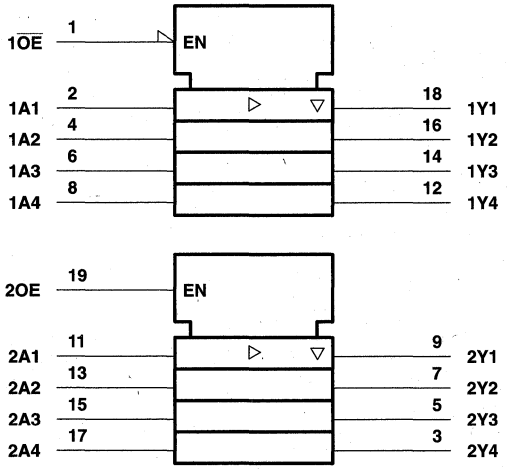
EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	H	H
L	L	L

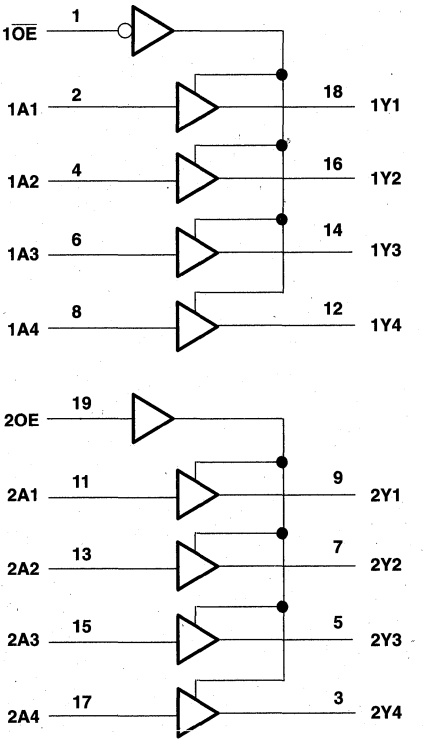
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT241 ..... 96 mA
SN74ABT241 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT241		SN74ABT241		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

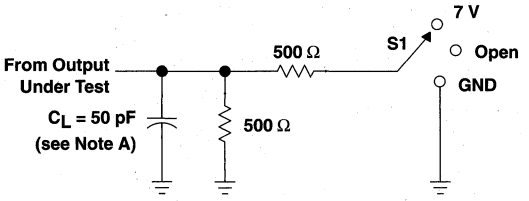
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT241		SN74ABT241		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

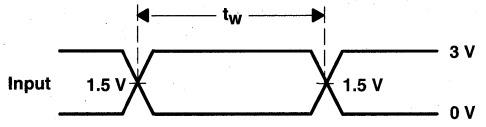
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT241		SN74ABT241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.6	4.1	0.8	5.3	1	4.6	ns
t_{PHL}			1	2.9	4.2	0.8	5	1	4.6	
t_{PZH}	$\overline{OE}$ or OE	Y	1.1	4.8	6.3	1	7	1.1	6.8	ns
t_{PZL}			1.3	4.3	5.8	1	7	1.3	6.8	
t_{PHZ}	$\overline{OE}$ or OE	Y	1.6	4.6	6.1	0.8	7.9	1.6	7.1	ns
t_{PLZ}			1	3.9	5.4	0.8	6.2	1	5.9	

PARAMETER MEASUREMENT INFORMATION

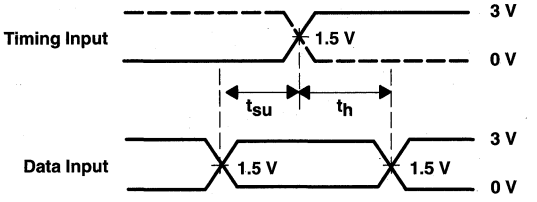


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

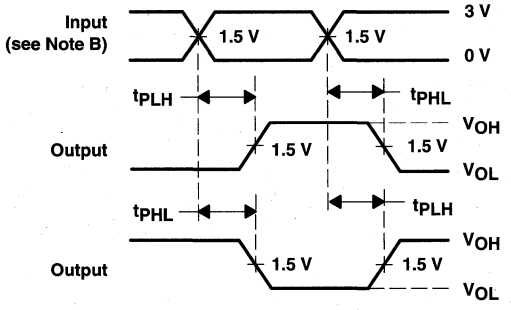
LOAD CIRCUIT FOR OUTPUTS



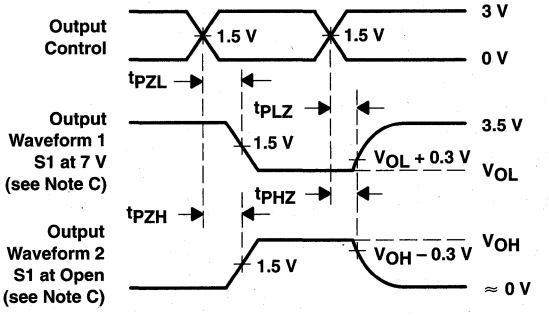
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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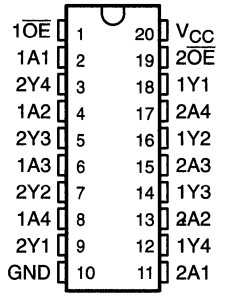
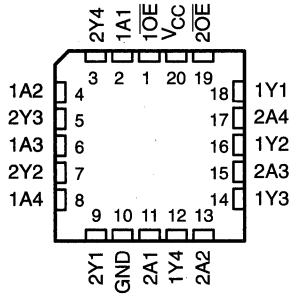
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT244 . . . J PACKAGE
SN74ABT244 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT244 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the ′ABT240 and ′ABT241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs.

The ′ABT244 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

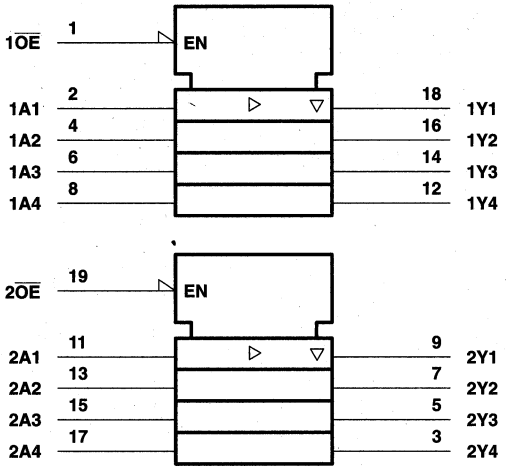
The SN54ABT244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT244 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

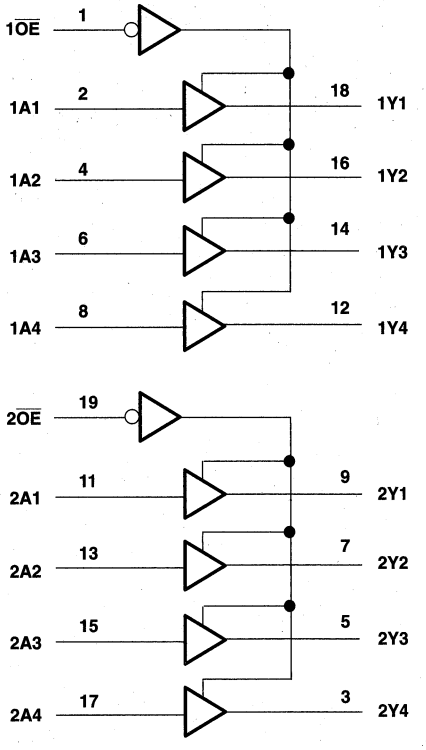
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT244 ..... 96 mA
SN74ABT244 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT244		SN74ABT244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

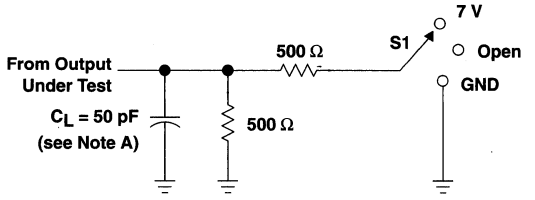
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT244		SN74ABT244		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = − 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = − 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = − 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				10§		10§		10§	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−10§		−10§		−10§	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

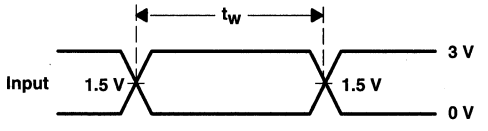
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT244		SN74ABT244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.6	4.1	1	5.3	1	4.6	ns
t_{PHL}			1	2.9	4.2	1	5	1	4.6	
t_{PZH}	$\overline{OE}$	Y	1.1	3.1	4.6	0.8	5.7	1.1	5.1	ns
t_{PZL}			2.1	4.1	5.6	1.2	7.9	2.1	6.1	
t_{PHZ}	$\overline{OE}$	Y	2.1	4.1	5.6	1.2	7.6	2.1	6.6	ns
t_{PLZ}			1.7	3.7	5.2	1	7.9	1.7	5.7	

PARAMETER MEASUREMENT INFORMATION

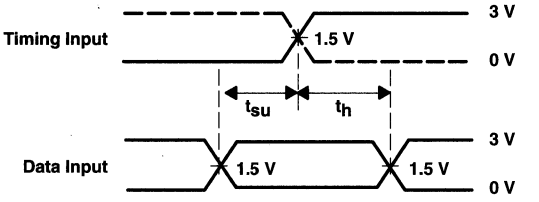


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

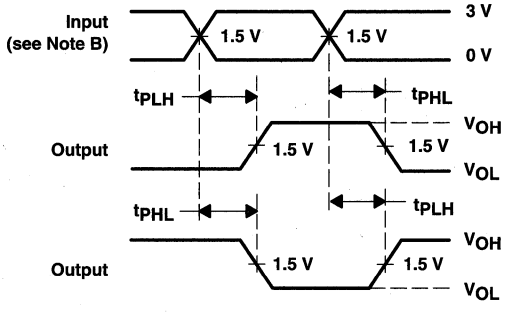
LOAD CIRCUIT FOR OUTPUTS



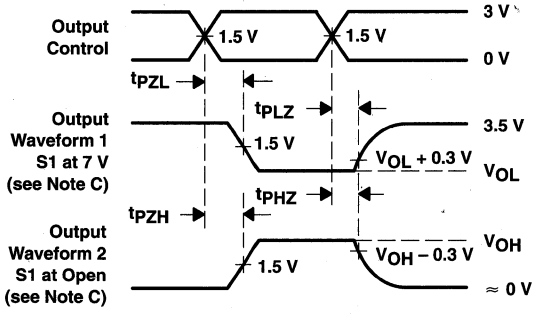
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



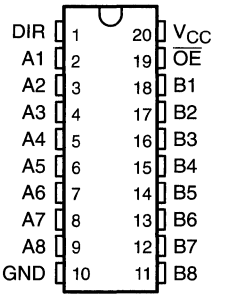
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

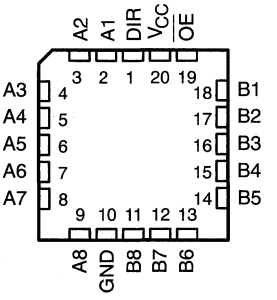
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT245 . . . J PACKAGE
SN74ABT245 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT245 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

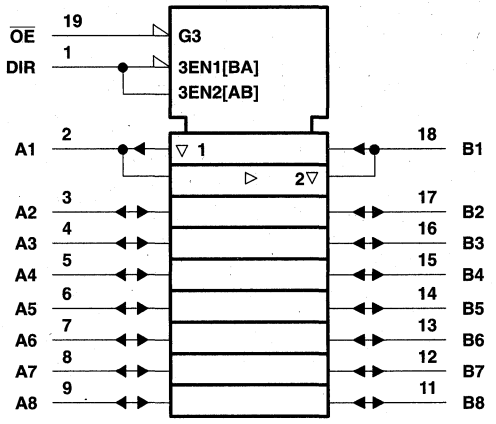
The SN54ABT245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

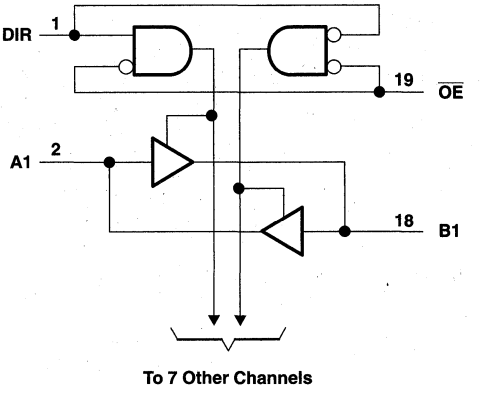
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT245 ..... 96 mA
SN74ABT245 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT245		SN74ABT245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT245		SN74ABT245		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				10¶		10¶		10¶	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−10¶		−10¶		−10¶	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O#	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−140	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		5	250		250		250	µA
			Outputs low		22	30		30		30	mA
			Outputs disabled		1	250		250		250	µA
ΔI_{CC}‖	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			50		50		50	µA
		Control inputs				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		8						pF

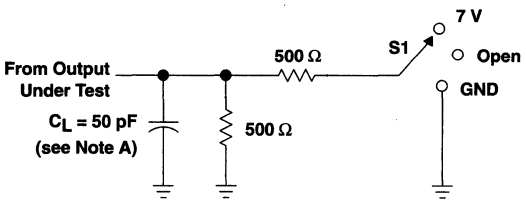
† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ This data sheet limit may vary among suppliers.
# Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT245		SN74ABT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.6	4.1	1	4.8	1	4.6	ns
t_{PHL}			1	2.9	4.2	1	4.8	1	4.6	
t_{PZH}	$\overline{OE}$	A or B	1.3	3.3	4.8	1	5.9	1.3	5.3	ns
t_{PZL}			2.3	4.3	5.8	2	7.5	2.3	6.3	
t_{PHZ}	$\overline{OE}$	A or B	1.7†	4.7	6.2	1.7	7.4	1.7†	7.2	ns
t_{PLZ}			1.7†	4.3	5.8	1.7	6.5	1.7†	6.3	

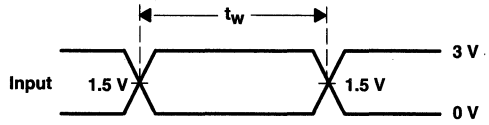
† This data sheet limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

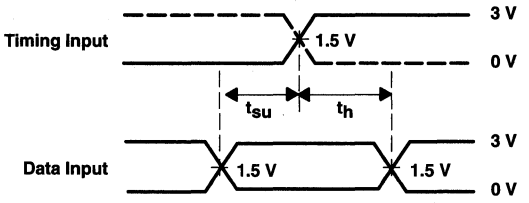


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

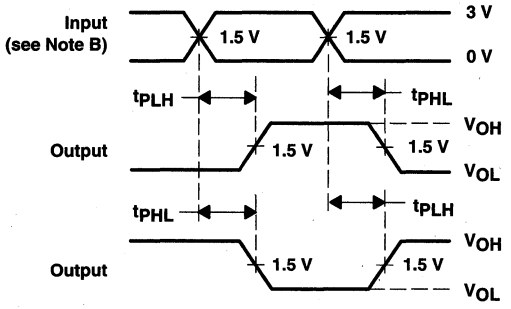
LOAD CIRCUIT FOR OUTPUTS



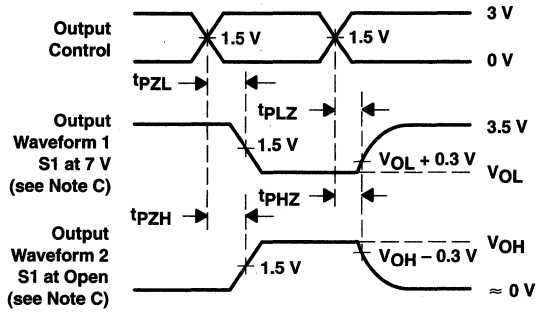
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



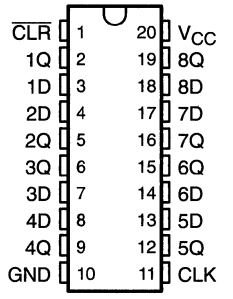
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

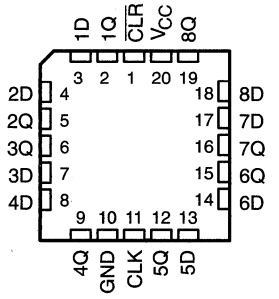
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT273 . . . J PACKAGE
SN74ABT273 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT273 . . . FK PACKAGE
(TOP VIEW)



description

The 'ABT273 is an 8-bit positive edge-triggered D-type flip-flop with a direct clear ($\overline{CLR}$) input. It is particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74ABT273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

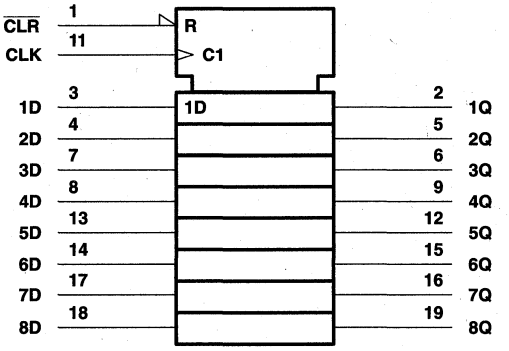
The SN54ABT273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT273 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

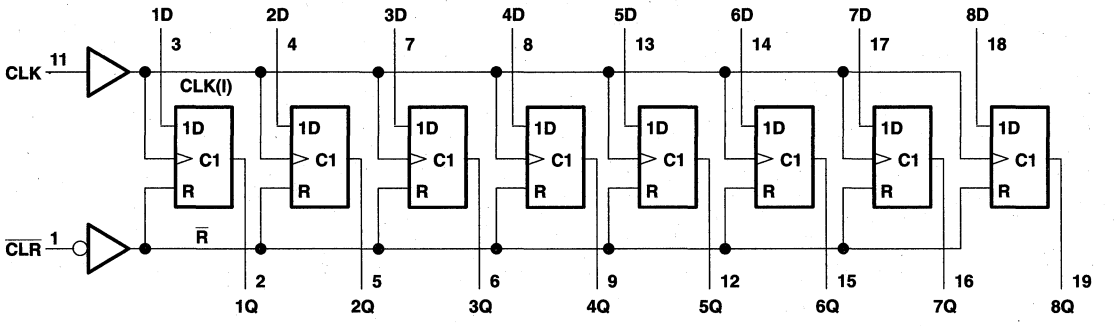
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT273 ..... 96 mA
SN74ABT273 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT273		SN74ABT273		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT273		SN74ABT273		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−200¶	−50	−200¶	−50	−200¶	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	400¶		400¶		400¶	µA
		Outputs low		24	30		30		30	mA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This data sheet limit may vary among suppliers.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

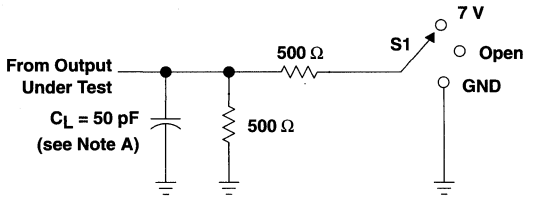
			V_{CC} = 5 V, T_A = 25°C		SN54ABT273		SN74ABT273		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	CLK high or low	3.3		3.3		3.3		ns
		$\overline{CLR}$ low	3.3		3.3		3.3		
t_{su}	Setup time before CLK↑	Data high	2		2		2		ns
		Data low	2.5		2.5		2.5		
		$\overline{CLR}$ high	2		2		2		
t_h	Hold time after CLK↑	Data high or low	1.2†		1.2†		1.2†		ns

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

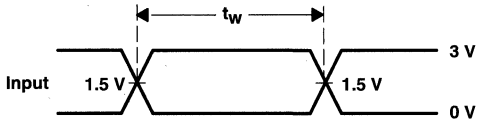
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT273		SN74ABT273		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			0		150	0	150	0	150	MHz
t_{PLH}	CLK	Q	2.5		6	2.5	6.8	2.5	6.5	ns
t_{PHL}			3.3		6.8	3.3	7	3.3	7.3	
t_{PHL}	$\overline{CLR}$	Q	2.5		6.7†	2.5	7.6	2.5	7.4†	ns

PARAMETER MEASUREMENT INFORMATION

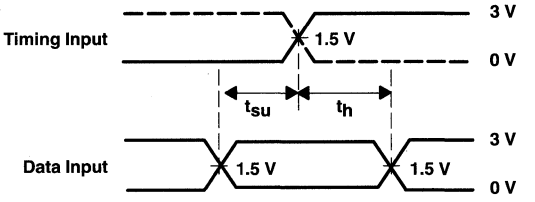


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

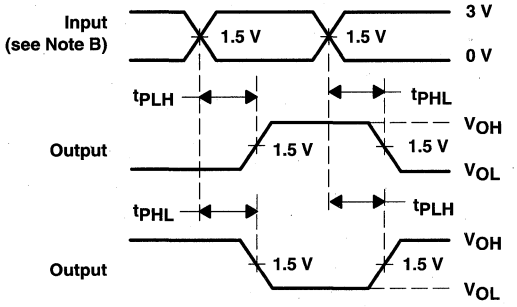
LOAD CIRCUIT FOR OUTPUTS



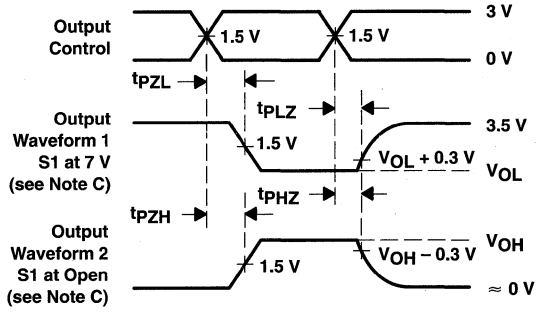
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



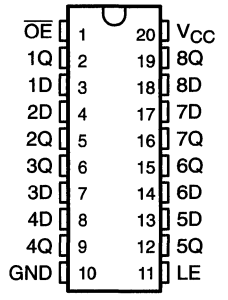
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

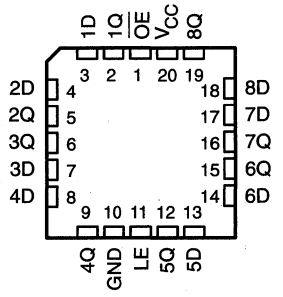
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT373 . . . J PACKAGE
SN74ABT373 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT373 . . . FK PACKAGE
(TOP VIEW)



description

The eight latches of the 'ABT373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

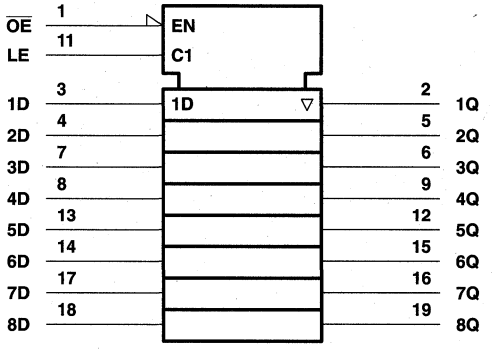
The SN54ABT373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

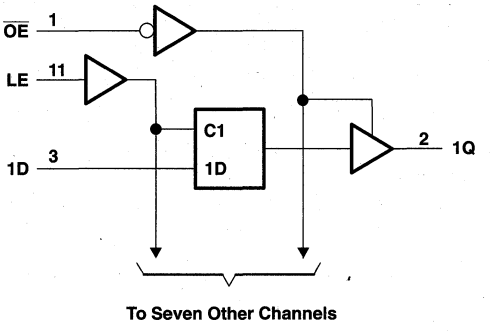
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT373 ..... 96 mA
SN74ABT373 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT373		SN74ABT373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT373		SN74ABT373		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				10§		10§		10§	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−10§		−10§		−10§	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			6						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

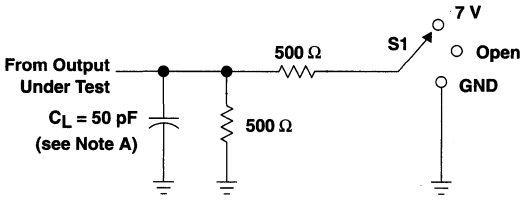
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT373		SN74ABT373		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	High	1.9		2.5		1.9		ns
		Low	1.5		2.5		1.5		
t_h	Hold time, data after LE↓	High or low	1		2.5		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

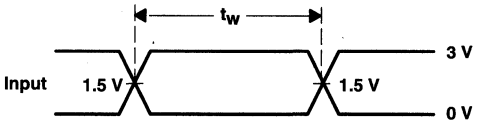
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT373		SN74ABT373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.9	3.9	5.4	1.3	6.8	1.9	5.9	ns
t_{PHL}			2.2	4.2	5.7	2	7	2.2	6.2	
t_{PLH}	LE	Q	2.6	4.6	6.1	1.8	7.7	2.6	6.6	ns
t_{PHL}			3.2	5.2	6.7	2.5	7.7	3.2	7.2	
t_{PZH}	$\overline{OE}$	Q	1.2	3.2	4.7	1	6.2	1.2	5.2	ns
t_{PZL}			2.7	4.7	6.2	1.5	7.2	2.7	6.7	
t_{PHZ}	$\overline{OE}$	Q	2.5	4.9	6.4	2.4	8	2.5	6.9	ns
t_{PLZ}			2	4.5	6	2	7	2	6.5	

PARAMETER MEASUREMENT INFORMATION

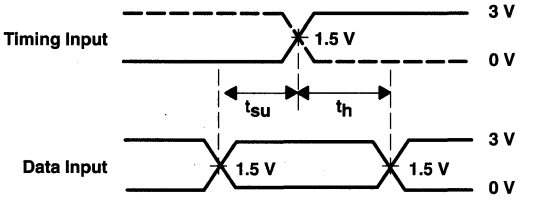


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

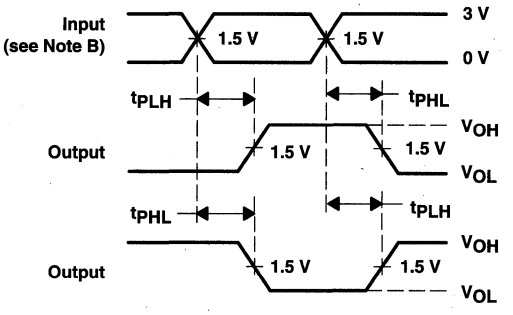
LOAD CIRCUIT FOR OUTPUTS



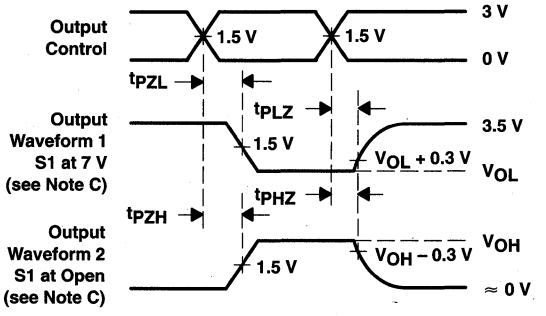
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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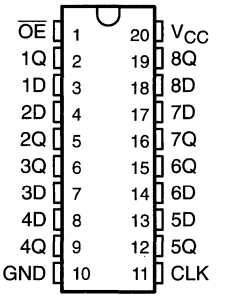
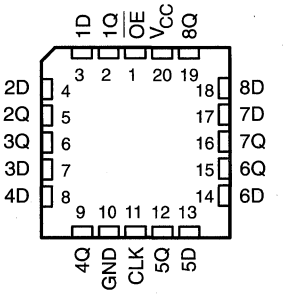
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT374 . . . J PACKAGE
SN74ABT374 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT374 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ABT374 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT374 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

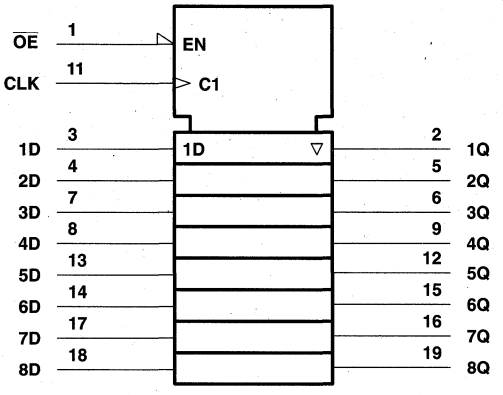
The SN54ABT374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

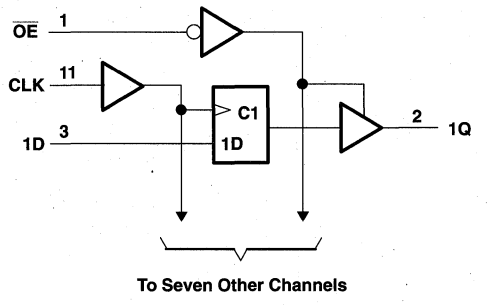
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT374 ..... 96 mA
SN74ABT374 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT374		SN74ABT374		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT374		SN74ABT374		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				10§		10§		10§	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−10§		−10§		−10§	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			250		250		250	µA
		Outputs low			30		30		30	mA
		Outputs disabled			250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			2.5						pF
C_o	V_O = 2.5 V or 0.5 V			7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

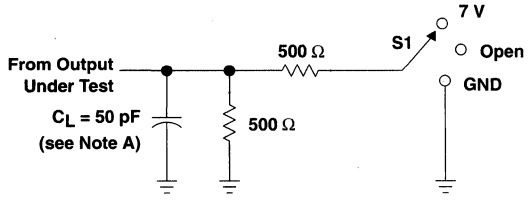
			V_{CC} = 5 V, T_A = 25°C		SN54ABT374		SN74ABT374		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	CLK high or low	3.3		3.3		3.3		ns
t_{su}	Setup time before CLK↑	Data high	1		2.5		1		ns
		Data low	1.9†		2.5		1.9†		
t_h	Hold time after CLK↑	Data high or low	1.6†		2.5		1.6†		ns

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

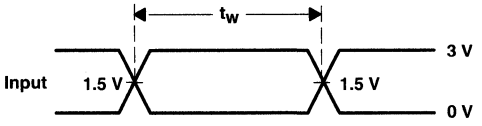
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT374		SN74ABT374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150		MHz
t_{PLH}	CLK	Q	2.2	4.2	5.7	1.8	6.6	2.2	6.2	ns
t_{PHL}			3.1	5.1	6.6	2.6	7.6	3.1	7.1	
t_{PZH}	$\overline{OE}$	Q	1.2	3.2	4.7	0.8	5.7	1.2	5.2	ns
t_{PZL}			2.7	4.7	6.2	1.5	7.2	2.7	6.7	
t_{PHZ}	$\overline{OE}$	Q	2.5	4.5	6	1.3	7.2	2.5	6.5	ns
t_{PLZ}			2	4.5	6	1	7	2	6.5	

PARAMETER MEASUREMENT INFORMATION

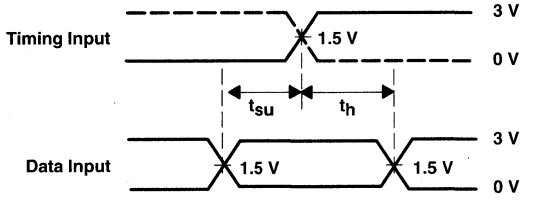


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

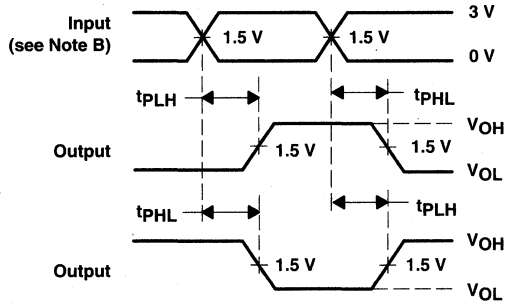
LOAD CIRCUIT FOR OUTPUTS



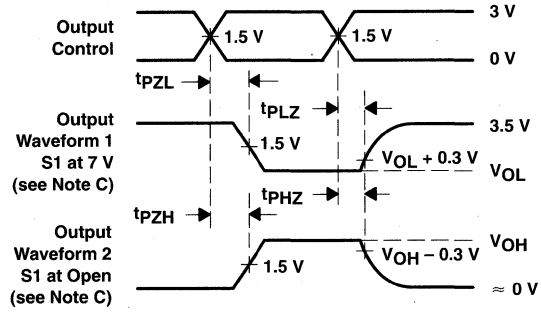
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



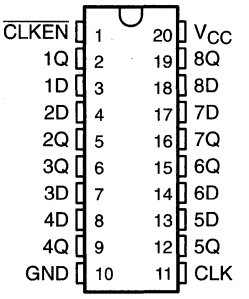
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

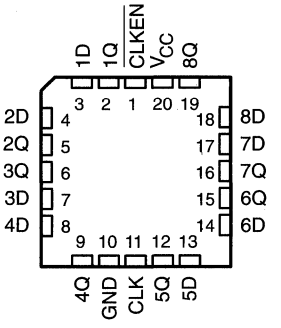
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT377 . . . J PACKAGE
SN74ABT377 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT377 . . . FK PACKAGE
(TOP VIEW)



description

The ′ABT377 is a 8-bit positive-edge-triggered D-type flip-flop with a clock (CLK) input. It is particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

Data (D) input information that meets the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the common clock-enable ($\overline{CLKEN}$) input is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the buffered clock (CLK) input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at $\overline{CLKEN}$.

The SN74ABT377 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

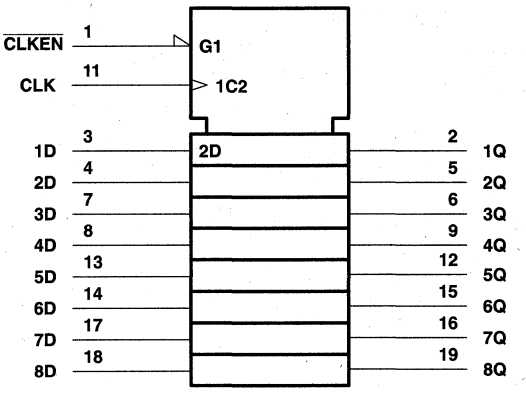
The SN54ABT377 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT377 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{CLKEN}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	H or L	X	Q_0

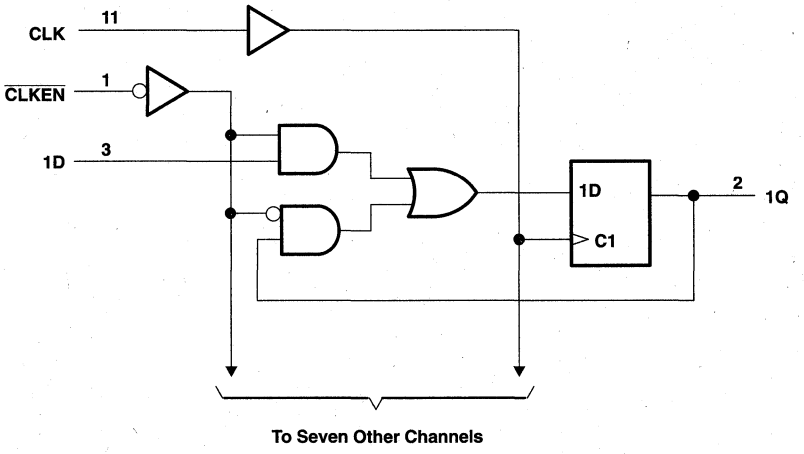
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT377 ..... 96 mA
SN74ABT377 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT377		SN74ABT377		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT377		SN74ABT377		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100		±500		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

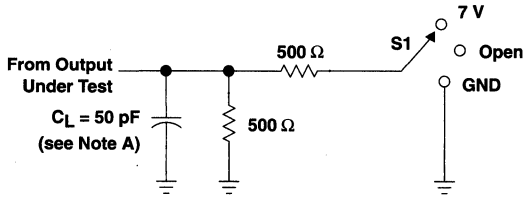
			V_{CC} = 5 V, T_A = 25°C		SN54ABT377		SN74ABT377		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	CLK high or low	3.3		3.3		3.3		ns
t_{su}	Setup time before CLK↑	Data high or low	2		2.5		2		ns
		$\overline{CLKEN}$ high or low	3		3		3		
t_h	Hold time after CLK↑	Data high or low	1.8#		1.8#		1.8#		ns
		$\overline{CLKEN}$ high or low	1.8#		1.8#		1.8#		

This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

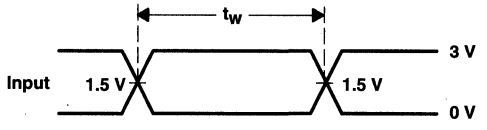
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT377		SN74ABT377		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLK	Q	2.2	4.5	6	2.2	7	2.2	6.5	ns
t_{PHL}			3.1	5.3	6.8	2	7.6	3.1	7.3	

PARAMETER MEASUREMENT INFORMATION

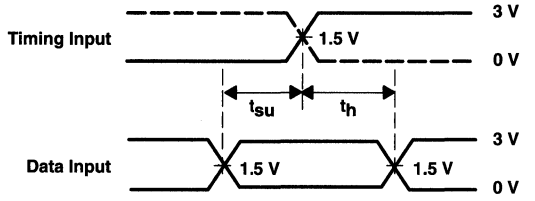


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

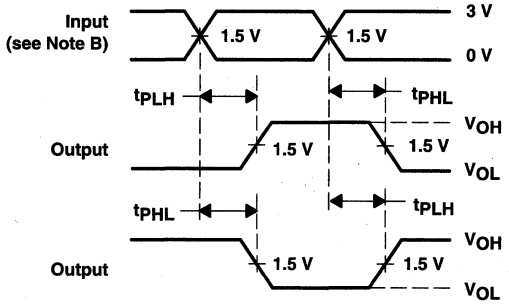
LOAD CIRCUIT FOR OUTPUTS



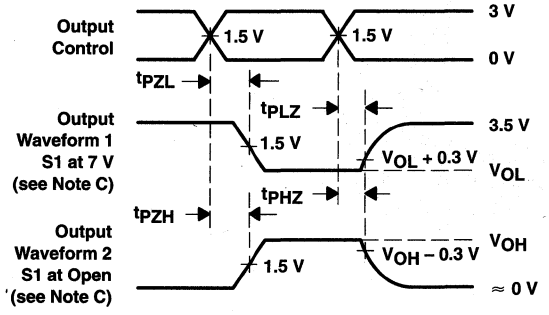
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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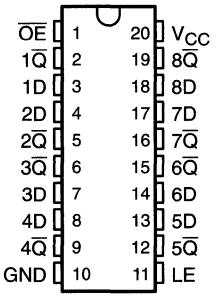
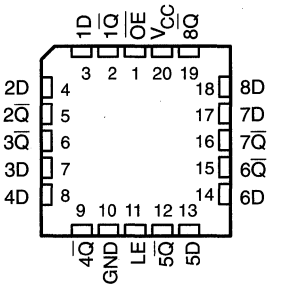
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT533 . . . J PACKAGE
SN74ABT533 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT533 . . . FK PACKAGE
(TOP VIEW)



description

The 'ABT533 is an 8-bit transparent D-type latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

When the latch-enable (LE) input is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{Q}$ outputs are latched at the inverse of the levels set up at the D inputs. The 'ABT533 provides inverted data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT533 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

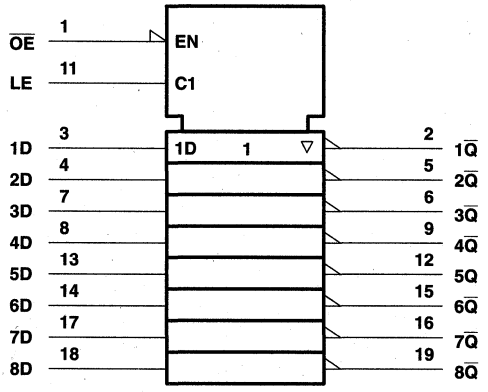
The SN54ABT533 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT533 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each latch)

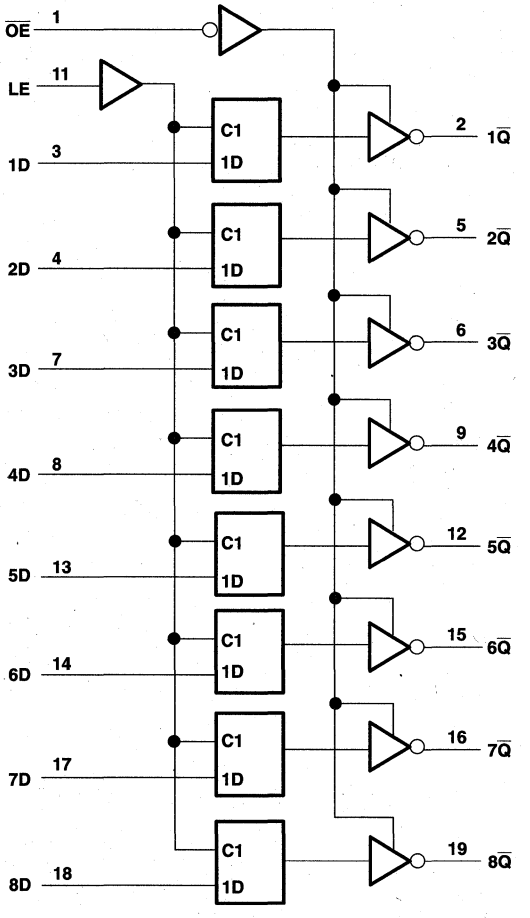
INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT533 ..... 96 mA
SN74ABT533 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT533		SN74ABT533		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT533		SN74ABT533		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				10§		10§		10§	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−10§		−10§		−10§	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±150				±150	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−140	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			1.5		1.5		1.5	
		Control inputs			1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

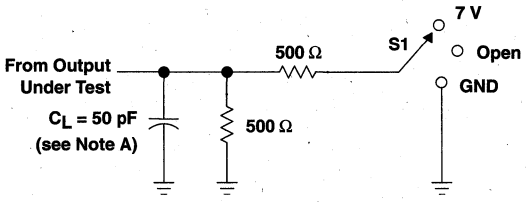
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT533		SN74ABT533		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	High or low	2.1		2.1		2.1		ns
t_h	Hold time, data after LE↓	High or low	1.5§		1.5§		1.5§		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

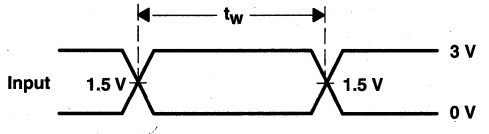
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT533		SN74ABT533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	1.9	4.2	5.4	1.9	6.7	1.9	6.4	ns
t_{PHL}			3.1	4.9	6.3	3.1	6.9	3.1	6.6	
t_{PLH}	LE	$\overline{Q}$	2.7	4.9	6.2	2.7	7.6	2.7	7.3	ns
t_{PHL}			3.5	5.4	6.8	3.5	7.5	3.5	7.3	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	1.6	3.7	4.8	1.6	5.8	1.6	5.7	ns
t_{PZL}			2.4	4.2	6.2	2.4	6.9	2.4	6.7	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	2.8	5.1	6.2	2.8	7.2	2.8	6.9	ns
t_{PLZ}			2	4.1	6	2	6.9	2	6.5	

PARAMETER MEASUREMENT INFORMATION

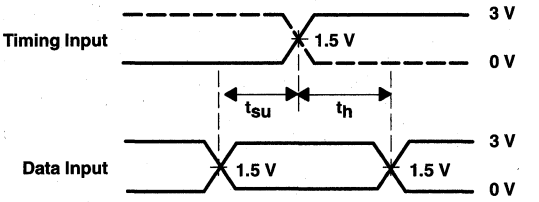


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

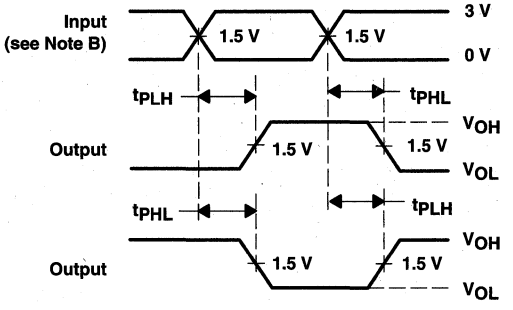
LOAD CIRCUIT FOR OUTPUTS



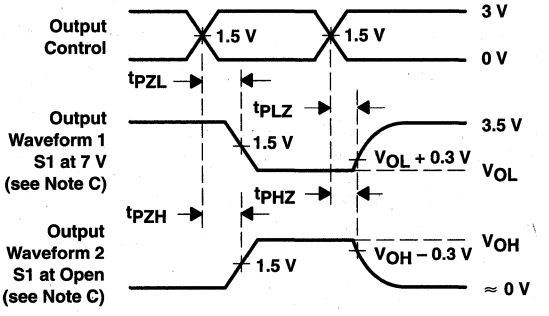
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



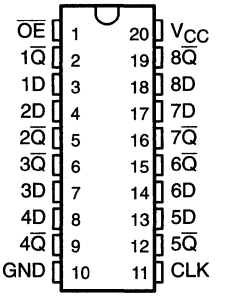
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

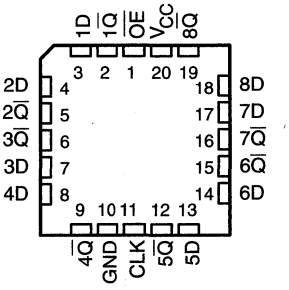
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT534 . . . J PACKAGE
SN74ABT534 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT534 . . . FK PACKAGE
(TOP VIEW)



description

The 'ABT534 is an 8-bit flip-flop with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ABT534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic levels that were set up at the data (D) inputs. The 'ABT534 provides inverted data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT534 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

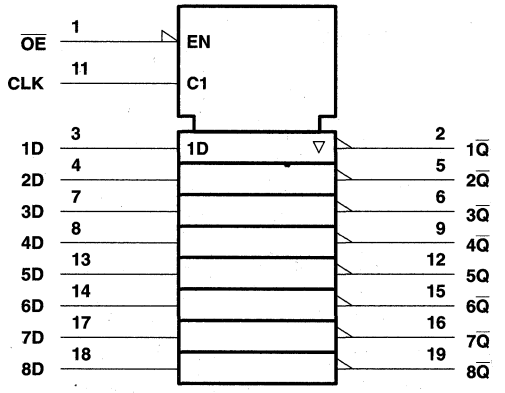
The SN54ABT534 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT534 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

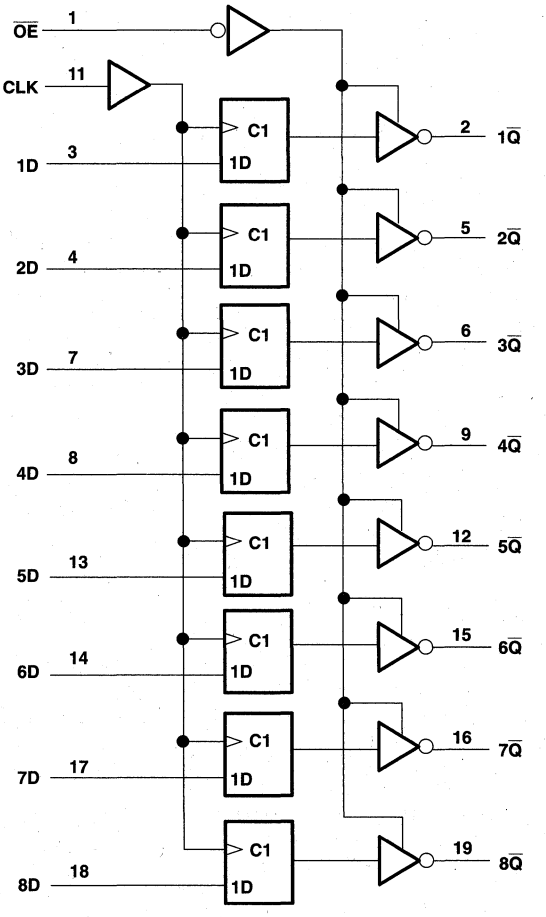
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	H or L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT534 ..... 96 mA
SN74ABT534 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT534		SN74ABT534		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT534		SN74ABT534		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−140	−200¶	−50	−200¶	−50	−200¶	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This data sheet limit may vary among suppliers.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

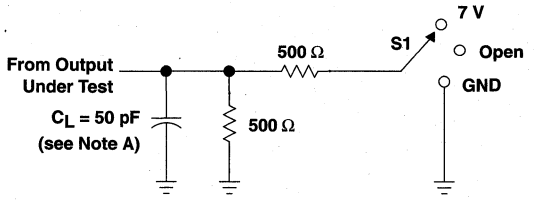
			V_{CC} = 5 V, T_A = 25°C		SN54ABT534		SN74ABT534		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			125		125		125	MHz
t_w	Pulse duration	CLK high or low	3.5		3.5		3.5		ns
t_{su}	Setup time, data before CLK↑	High or low	1.6		1.6		1.6		ns
t_h	Hold time, data after CLK↑	High or low	1.6¶		1.6¶		1.6¶		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT534		SN74ABT534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125	175		125		125		MHz
t_{PLH}	CLK	Q	2.6	4.5	6.1†	2.6	7	2.6	6.7	ns
t_{PHL}			3.4	5.5	6.7	3.4	7.9	3.4	7.6	
t_{PZH}	$\overline{OE}$	Q	1	3.4	5.2†	1	5.8	1	5.6†	ns
t_{PZL}			2.6	4	5.8	2.6	7	2.6	6.8	
t_{PHZ}	$\overline{OE}$	Q	2.4	4.7	6.6	2.4	7.6	2.4	7.3	ns
t_{PLZ}			2.3	3.8	5.8	2.3	6.8	2.3	6.5	

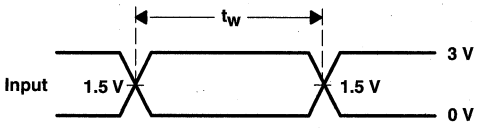
† This data sheet limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

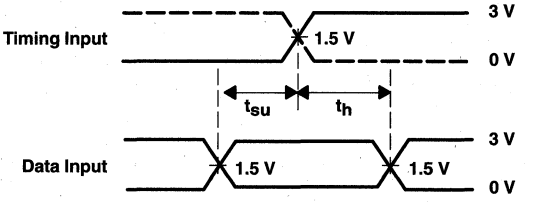


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

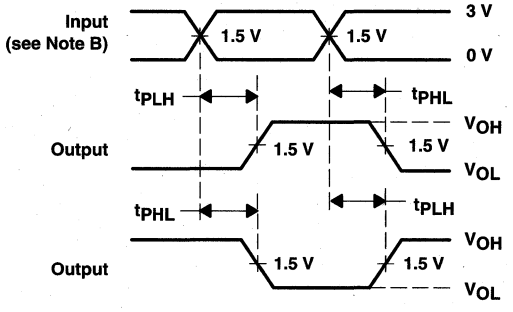
LOAD CIRCUIT FOR OUTPUTS



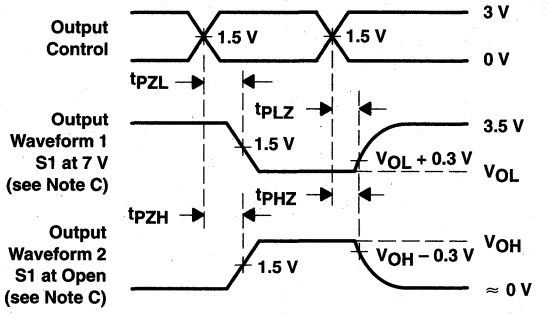
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



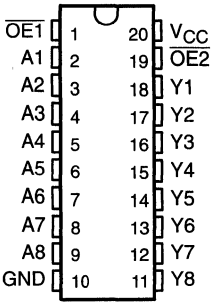
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

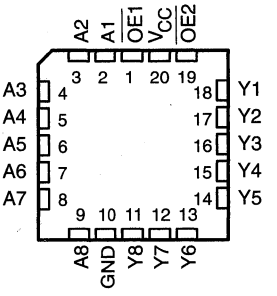
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT540 . . . J PACKAGE
SN74ABT540 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT540 . . . FK PACKAGE
(TOP VIEW)



description

The 'ABT540 octal buffers and line drivers are ideal for driving bus lines or buffer memory address registers. The device features inputs and outputs on opposite sides of the package that facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT540 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

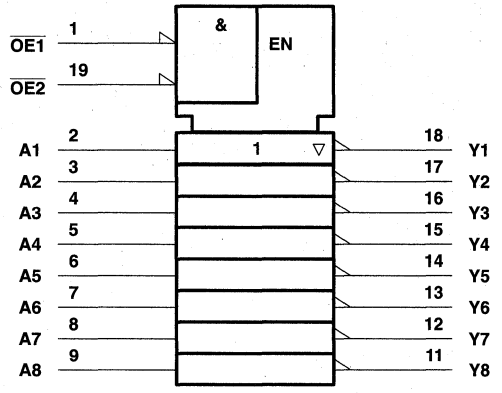
The SN54ABT540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

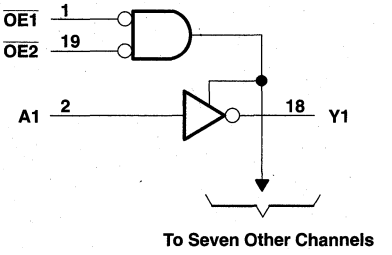
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT540 ..... 96 mA
SN74ABT540 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT540		SN74ABT540		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

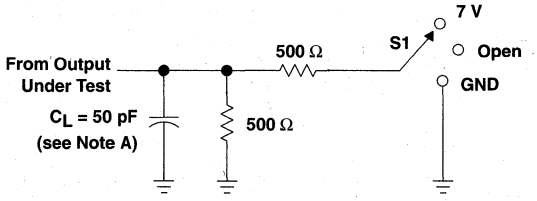
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT540		SN74ABT540		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

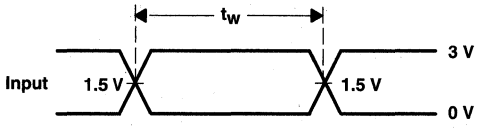
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT540		SN74ABT540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.9	4.1	1		1	4.8	ns
t_{PHL}			1.6	3.1	4.3	1.6		1.6	4.8	
t_{PZH}	$\overline{OE}$	Y	1.2	3.4	4.9	1.2		1.2	5.9	ns
t_{PZL}			1.2	3	4.4	1.2		1.2	5.1	
t_{PHZ}	$\overline{OE}$	Y	3.1	5.3	6.5	3.1		3.1	7.3	ns
t_{PLZ}			2.5	4.4	5.7	2.5		2.5	6.2	

PARAMETER MEASUREMENT INFORMATION

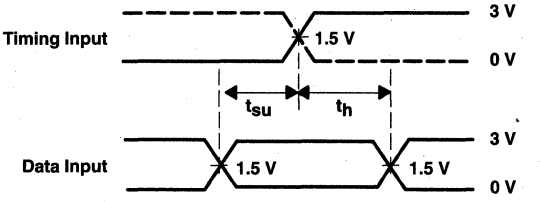


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

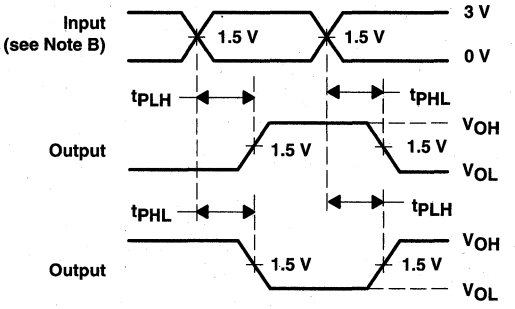
LOAD CIRCUIT FOR OUTPUTS



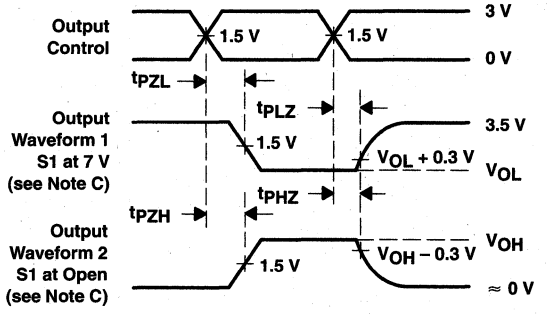
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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Figure 1. Load Circuit and Voltage Waveforms

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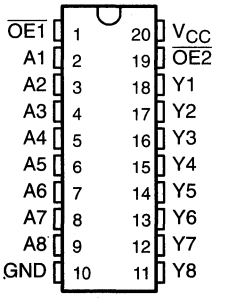
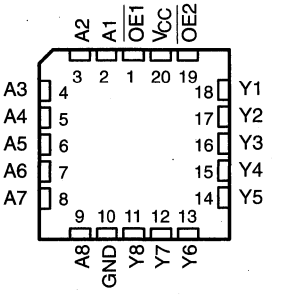
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT541 . . . J PACKAGE
SN74ABT541 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT541 . . . FK PACKAGE
(TOP VIEW)



description

The 'ABT541 octal buffer and line driver is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT541 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

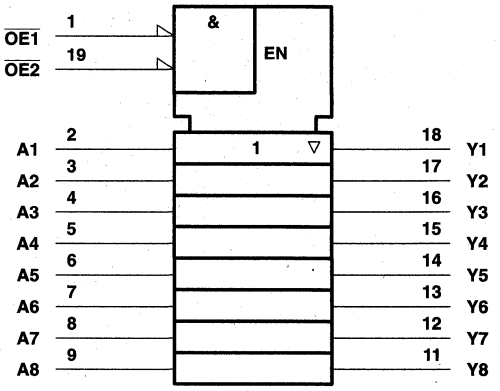
The SN54ABT541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

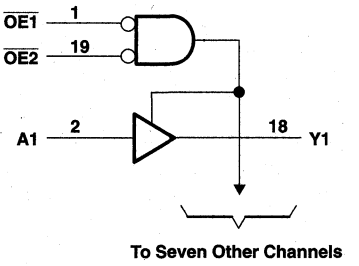
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range , V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT541 ..... 96 mA
SN74ABT541 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT541		SN74ABT541		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

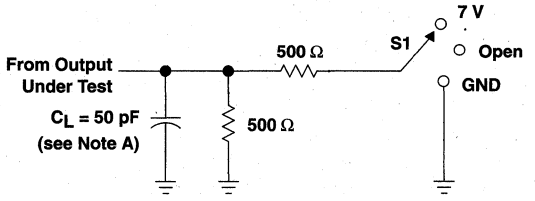
PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT541		SN74ABT541		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−140	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		5	250		250		250	µA
		Outputs low		22	30		30		30	mA
		Outputs disabled		1	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	µA
		Control inputs			1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			5						pF
C_o	V_O = 2.5 V or 0.5 V			5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

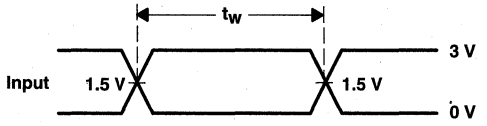
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT541		SN74ABT541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.6	4.1	1	4.6	1	4.6	ns
t_{PHL}			1	2.9	4.2	1	4.7	1	4.6	
t_{PZH}	$\overline{OE}$	Y	1.1	3.1	4.8	1.1	5.4	1.1	5.3	ns
t_{PZL}			2.1	4.4	5.9	2.1	6.5	2.1	6.4	
t_{PHZ}	$\overline{OE}$	Y	2.1	5.1	6.6	2.1	7.1	2.1	7.1	ns
t_{PLZ}			1.7	4.7	6.2	1.7	6.7	1.7	6.7	

PARAMETER MEASUREMENT INFORMATION

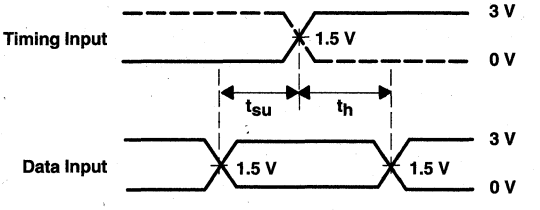


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

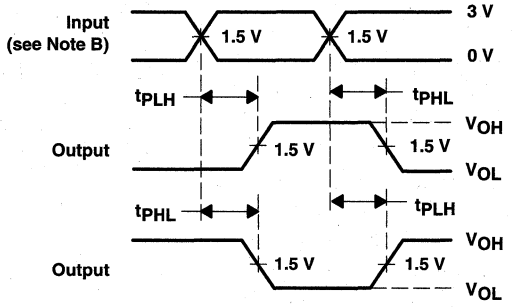
LOAD CIRCUIT FOR OUTPUTS



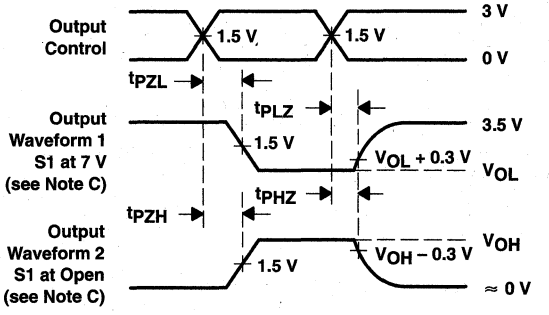
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



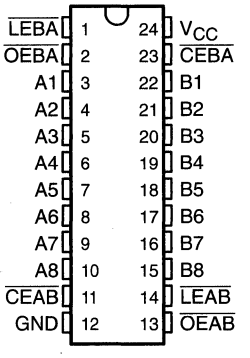
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

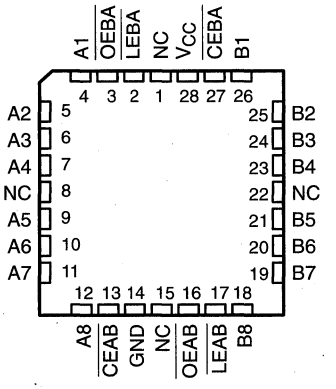
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT543 . . . JT PACKAGE
SN74ABT543 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT543 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ′ABT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT543 is characterized for operation from –40°C to 85°C.

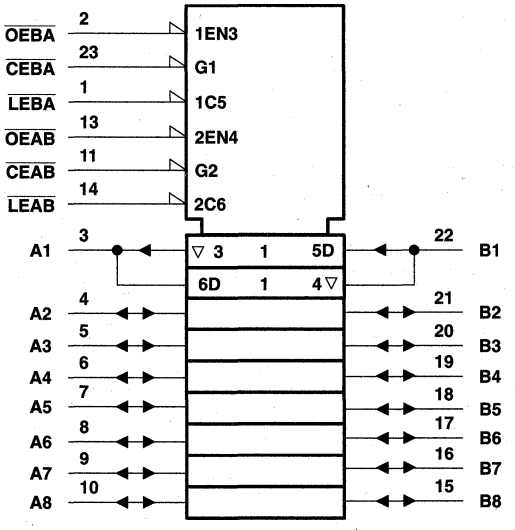
EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

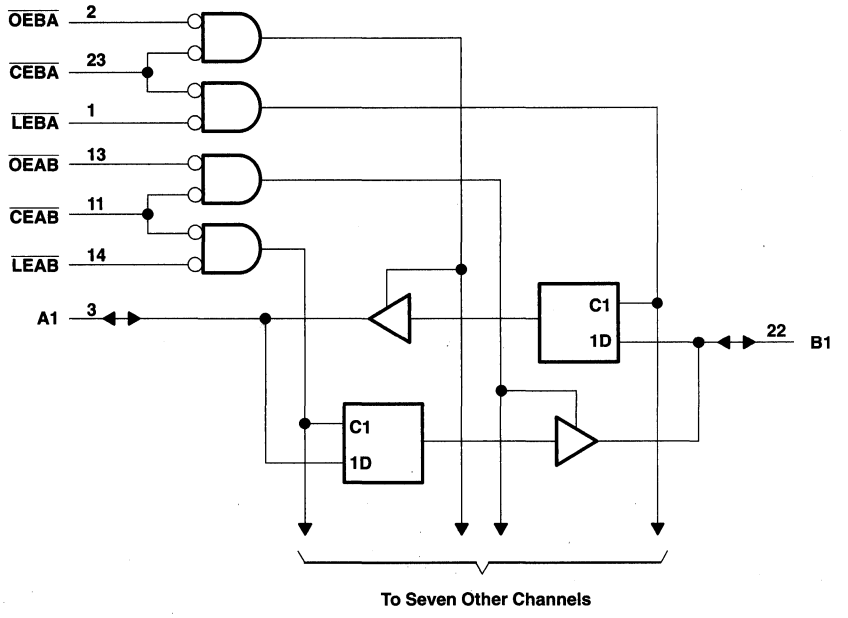
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT543 ..... 96 mA
SN74ABT543 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT543		SN74ABT543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT543		SN74ABT543		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				10¶		10¶		10¶	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−10¶		−10¶		−10¶	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O#	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	34¶		34¶		34¶	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}‖	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ This data sheet limit may vary among suppliers.
# Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

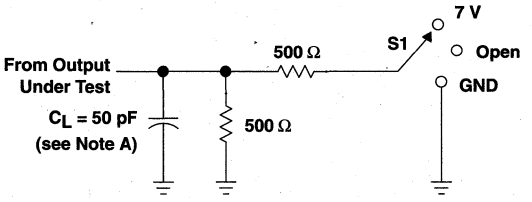
				V_{CC} = 5 V, T_A = 25°C		SN54ABT543		SN74ABT543		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low			3.5		3.5		3.5		ns
t_{su}	Setup time	Data before $\overline{LEAB}$ or $\overline{LEBA}$↑	High	3.5		3.5		3.5		ns
			Low	3		3		3		
		Data before $\overline{CEAB}$ or $\overline{CEBA}$↑	High	3.5		3.5		3.5		
			Low	3		3		3		
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}$↑		1†		1†		1†		ns
		Data after $\overline{CEAB}$ or $\overline{CEBA}$↑		1†		1†		1†		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT543		SN74ABT543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.9	4.4	5.9	1.9		1.9	6.9	ns
t_{PHL}			1.9	4.4	5.9	1.9		1.9	6.9	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	1.6	4.1	5.6	1.6		1.6	6.6	ns
t_{PHL}			2.1	4.6	6.1	2.1		2.1	7.1	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.4	3.9	5.4	1.4		1.4	6.4	ns
t_{PZL}			2.5	5	6.5	2.5		2.5	7.5	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.5†	5.9	7.4	2.5†		2.5†	8.4	ns
t_{PLZ}			3	5.5	7	3		3	8	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	1.4	3.9	5.4	1.4		1.4	6.4	ns
t_{PZL}			2.5	5	6.5	2.5		2.5	7.5	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.2†	5.9	7.4	3.2†		3.2†	8.4	ns
t_{PLZ}			3	5.5	7	3		3	8	

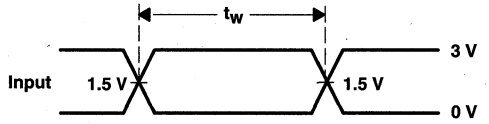
† This data sheet limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

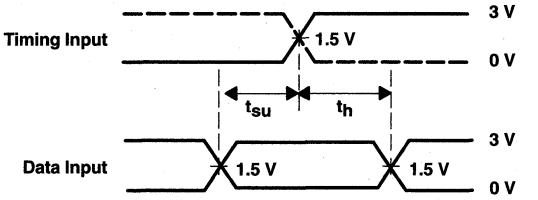


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

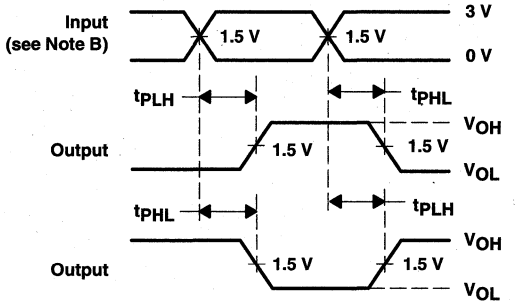
LOAD CIRCUIT FOR OUTPUTS



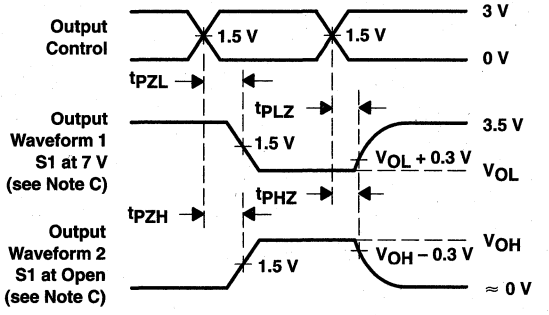
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
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NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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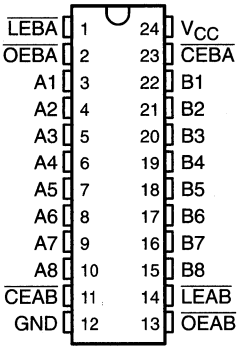
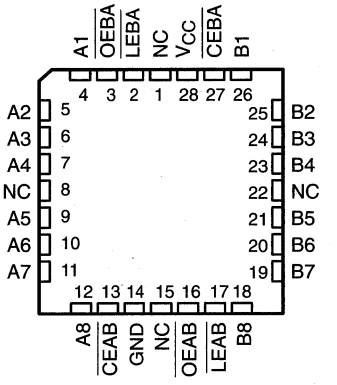
SN54ABT544 . . . JT PACKAGE
SN74ABT544 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT544 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

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To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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The SN54ABT544 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT544 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

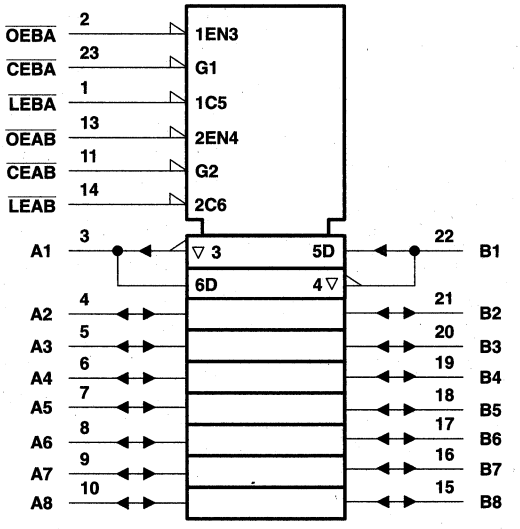
EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
L	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	H
L	L	L	H	L

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

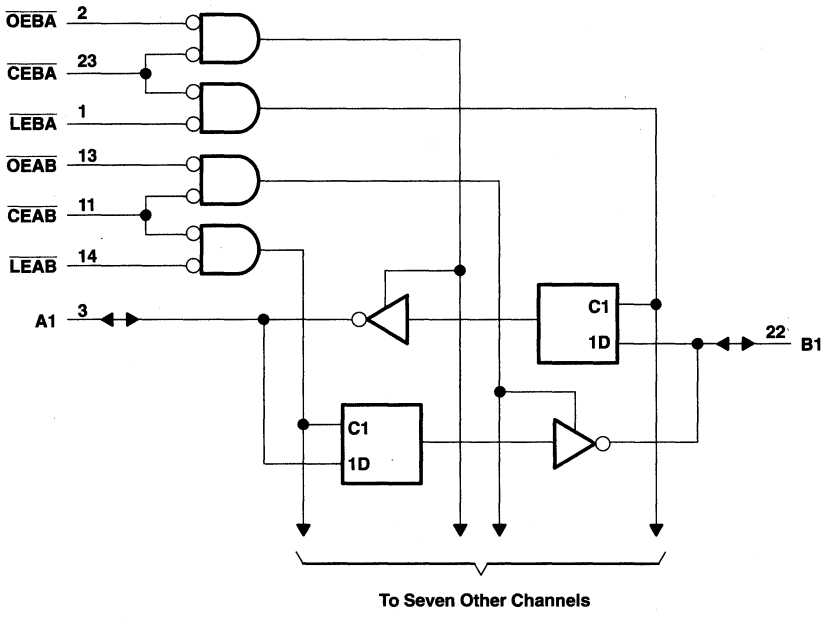
logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
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NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			SN54ABT544		SN74ABT544		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

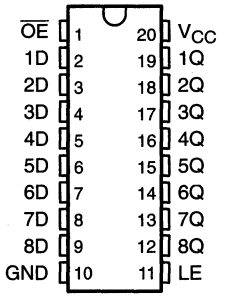
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT544		SN74ABT544		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	34#		34#		34#	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}‖	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This data sheet limit may vary among suppliers.
‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

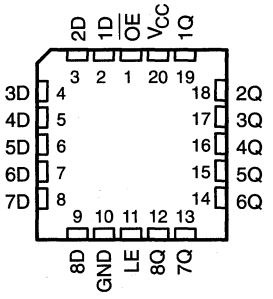
PRODUCT PREVIEW

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT573 . . . J PACKAGE
SN74ABT573 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT573 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ABT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

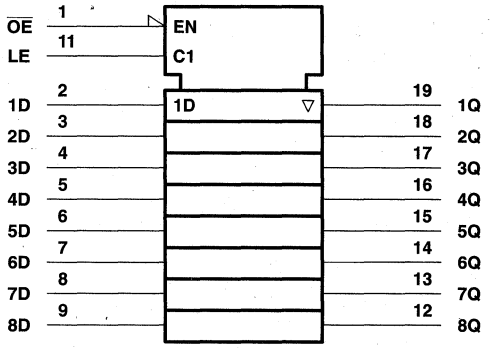
The SN54ABT573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT573 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

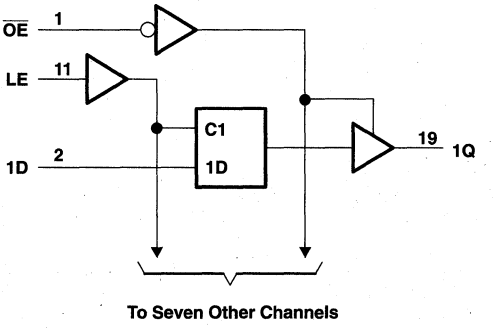
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT573 ..... 96 mA
SN74ABT573 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT573		SN74ABT573		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT573		SN74ABT573		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
V_{OH}	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		V
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		10		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−10		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100		±500		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			6						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

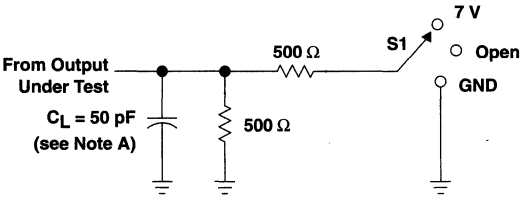
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT573		SN74ABT573		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	High	1.9		2.5		1.9		ns
		Low	1.5		2.5		1.5		
t_h	Hold time, data after LE↓		1		2.5		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

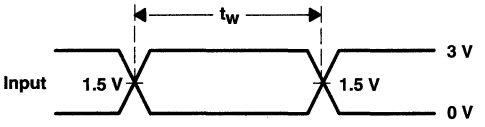
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT573		SN74ABT573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.9	3.2	5.4	1.4	6.4	1.9	5.9	ns
t_{PHL}			2.2	4.2	5.7	1.6	6.7	2.2	6.2	
t_{PLH}	LE	Q	2.2	4	6.1	2	7.1	2.2	6.6	ns
t_{PHL}			3.2	5.2	6.7	2.8	7.5	3.2	7.2	
t_{PZH}	$\overline{OE}$	Q	1.2	3.2	4.7	0.8	6.2	1.2	5.2	ns
t_{PZL}			2.7	4.7	6.2	2	7.2	2.7	6.7	
t_{PHZ}	$\overline{OE}$	Q	2.5	4.9	6.4	2.2	7.7	2.5	6.9	ns
t_{PLZ}			2	4.2	6	1.4	7	2	6.5	

PARAMETER MEASUREMENT INFORMATION

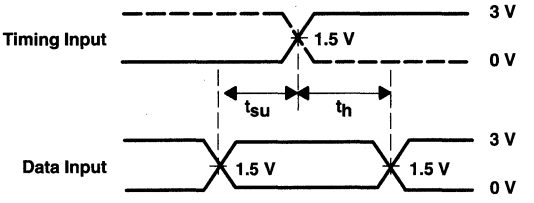


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

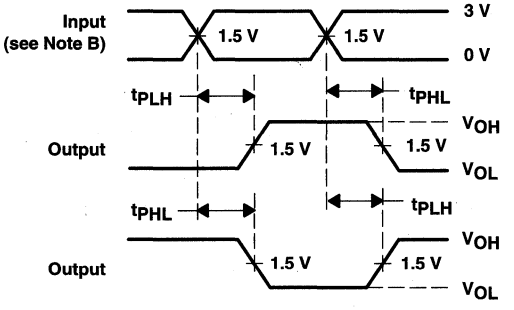
LOAD CIRCUIT FOR OUTPUTS



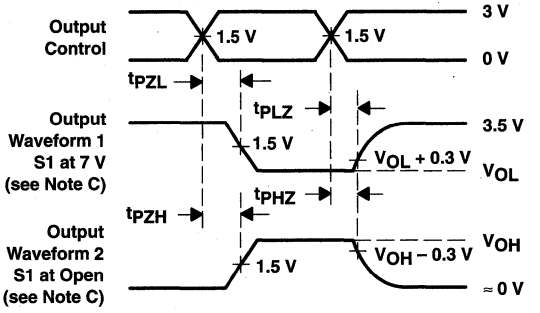
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



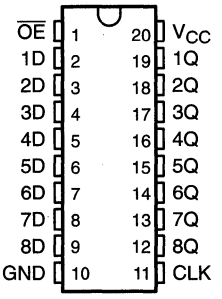
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

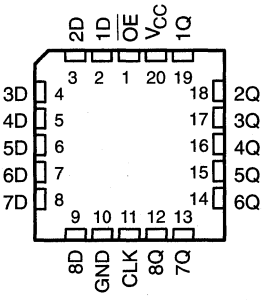
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT574 . . . J PACKAGE
SN74ABT574 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT574 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ABT574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

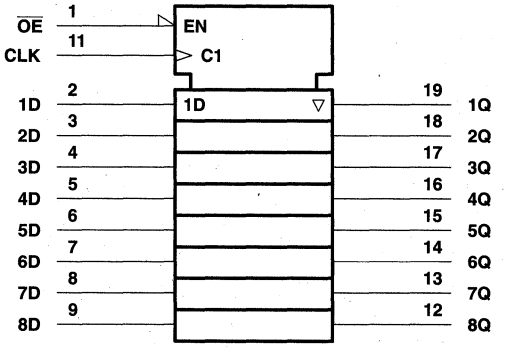
The SN54ABT574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT574 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

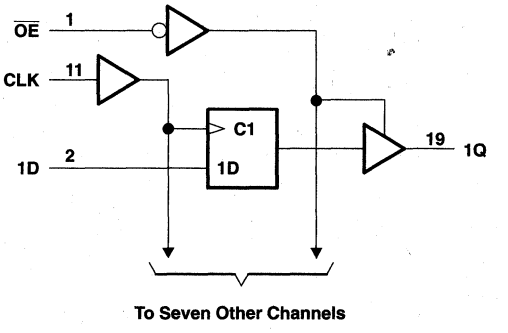
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT574 ..... 96 mA
SN74ABT574 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT574		SN74ABT574		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT574		SN74ABT574		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		10		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−10		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100		±500		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

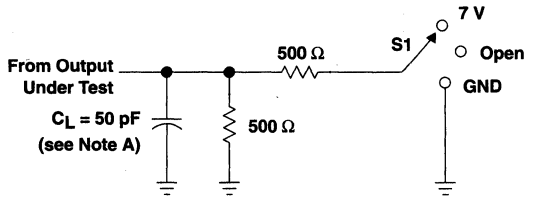
			V_{CC} = 5 V, T_A = 25°C		SN54ABT574		SN74ABT574		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150		150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	High	1		1.5		1		ns
		Low	1.5		2		1.5		
t_h	Hold time, data after CLK↑	High or low	1.5†		2		1.5†		ns

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

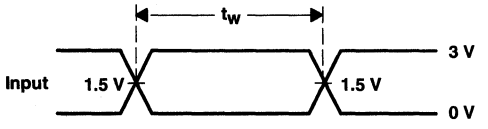
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT574		SN74ABT574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150		MHz
t_{PLH}	CLK	Q	2.2	3.9	6.2	2.2	7	2.2	6.8	ns
t_{PHL}			3	4.8	6.6	3	7.4	3	7.1	
t_{PZH}	$\overline{OE}$	Q	1	3.3	4.3	1	6	1	5.1	ns
t_{PZL}			2.5	4.7	5.9	2.5	6.8	2.5	6.7	
t_{PHZ}	$\overline{OE}$	Q	2.4	4.9	6.2	2.4	7.3	2.4	7	ns
t_{PLZ}			2	4	5.8	2	6.9	2	6.5	

PARAMETER MEASUREMENT INFORMATION

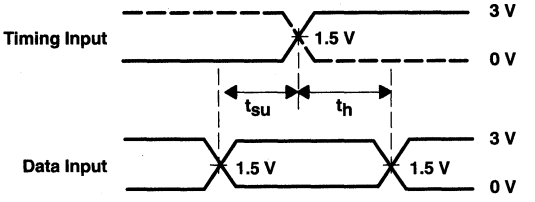


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

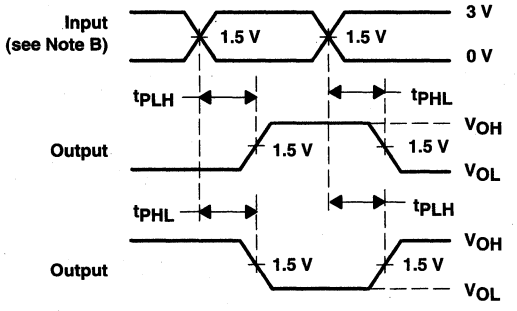
LOAD CIRCUIT FOR OUTPUTS



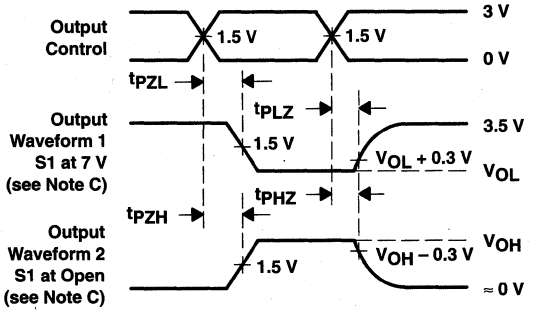
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



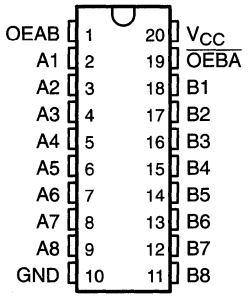
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

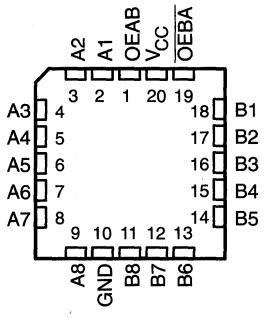
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT620 . . . J PACKAGE
SN74ABT620 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT620 . . . FK PACKAGE
(TOP VIEW)



description

The 'ABT620 bus transceiver is designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing. The 'ABT620 provides inverted data at its outputs.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and $\overline{\text{OEBA}}$) inputs.

The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. In this way, each output reinforces its input in this configuration.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT620 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

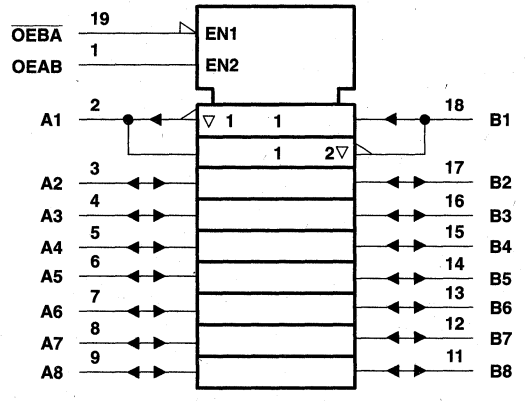
The SN54ABT620 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT620 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

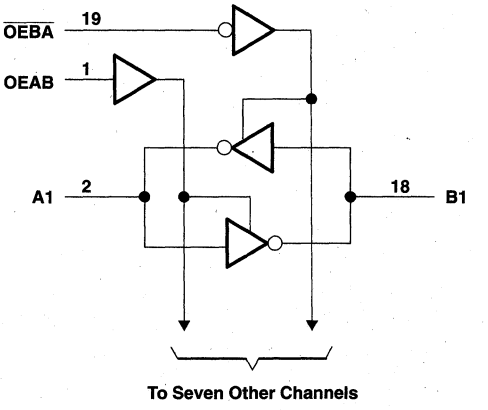
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus
H	L	Isolation
H	H	$\overline{A}$ data to B bus

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT620 ..... 96 mA
SN74ABT620 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT620		SN74ABT620		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT620		SN74ABT620		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		5	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT620		SN74ABT620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1		4.1	1		1	4.8	ns
t_{PHL}			1		4.3	1		1	4.8	
t_{PZH}	$\overline{OEBA}$	A	1.3		4.6	1.3		1.3	5.5	ns
t_{PZL}			1		6.1	1		1	7.1	
t_{PHZ}	$\overline{OEBA}$	A	2		6.3	2		2	7	ns
t_{PLZ}			1.4		5.4	1.4		1.4	5.8	
t_{PZH}	OEAB	B	1.6		6.2	1.6		1.6	6.8	ns
t_{PZL}			2		5.9	2		2	6.4	
t_{PHZ}	OEAB	B	1.2		5.6	1.2		1.2	6.5	ns
t_{PLZ}			1.1		4.7	1.1		1.1	5.6	

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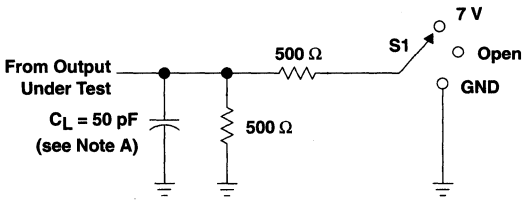
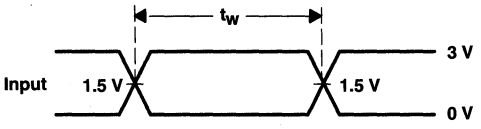
PARAMETER MEASUREMENT INFORMATION

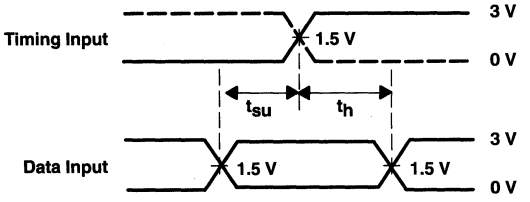


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

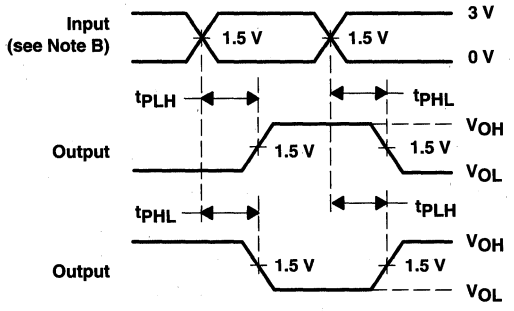
LOAD CIRCUIT FOR OUTPUTS



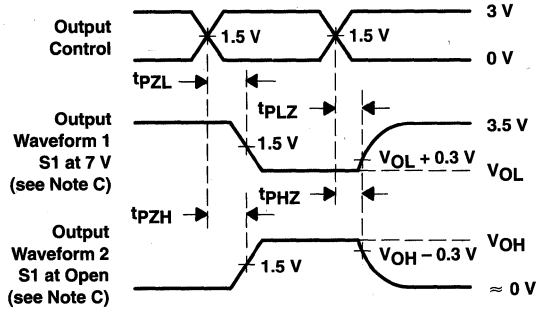
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
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D. The outputs are measured one at a time with one transition per measurement.

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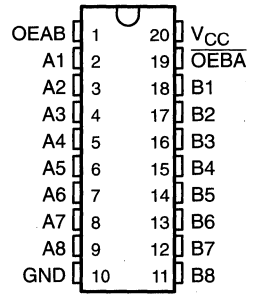
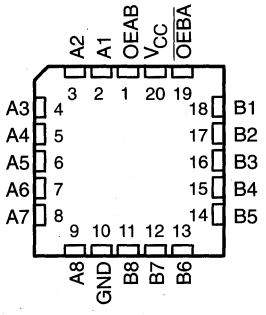
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT623A . . . J PACKAGE
SN74ABT623 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT623A . . . FK PACKAGE
(TOP VIEW)



description

The SN54ABT623A and SN74ABT623 bus transceivers are designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing. The SN54ABT623A and SN74ABT623 provide true data at their outputs.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and $\overline{\text{OEBA}}$) inputs.

The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this configuration. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT623 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

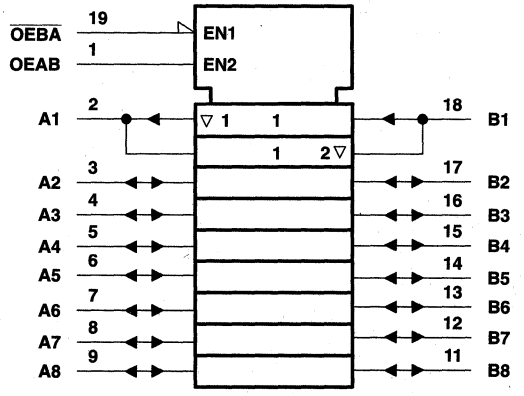
The SN54ABT623A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT623 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

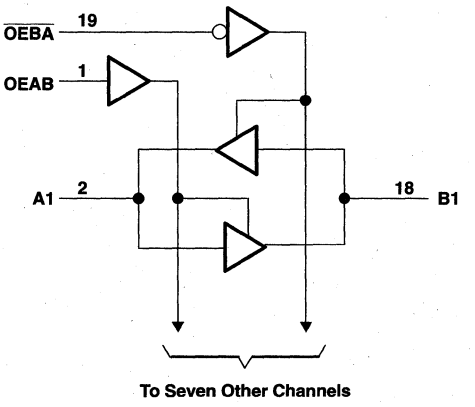
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	B data to A bus
L	H	B data to A bus, A data to B bus
H	L	Isolation
H	H	A data to B bus

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT623A ..... 96 mA
SN74ABT623 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT623A		SN74ABT623		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

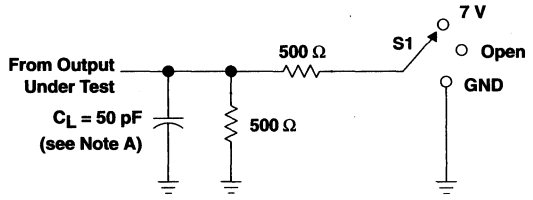
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT623A		SN74ABT623		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		5	250		250		250	µA
			Outputs low		22	30		30		30	mA
			Outputs disabled		1	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

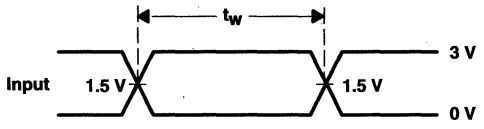
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT623A		SN74ABT623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.6	4.1	1	4.6	1	4.6	ns
t_{PHL}			1	2.6	4.2	1	4.6	1	4.6	
t_{PZH}	$\overline{OEBA}$	A	1.7	3.4	6.5	1.7	7.5	1.7	7.5	ns
t_{PZL}			1.7	3.8	6.5	1.7	7.5	1.7	7.5	
t_{PHZ}	$\overline{OEBA}$	A	1.7	4.2	6.5	1.7	7.5	1.7	7.5	ns
t_{PLZ}			1.7	4.7	6.5	1.7	7.5	1.7	7.5	
t_{PZH}	OEAB	B	1.7	4.8	6.5	1.7	7.5	1.7	7.5	ns
t_{PZL}			1.7	4	6.5	1.7	7.5	1.7	7.5	
t_{PHZ}	OEAB	B	1.7	3.9	6.5	1.7	7.5	1.7	7.5	ns
t_{PLZ}			1.7	3.2	6.5	1.7	7.5	1.7	7.5	

PARAMETER MEASUREMENT INFORMATION

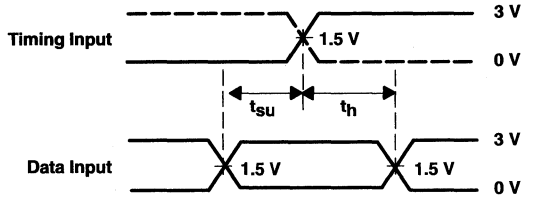


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

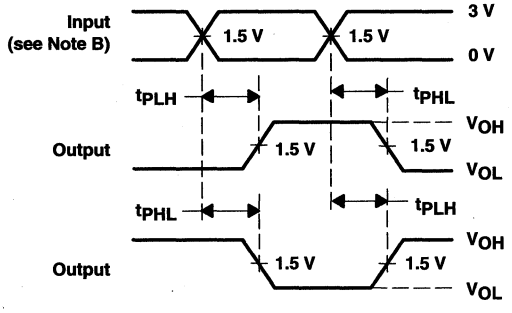
LOAD CIRCUIT FOR OUTPUTS



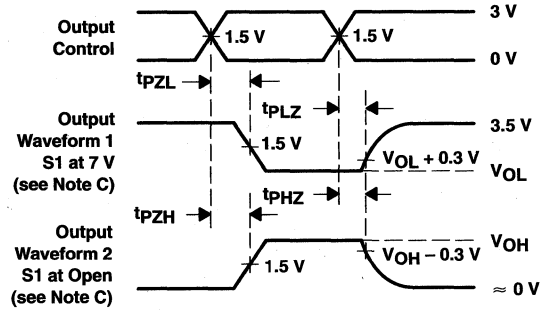
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



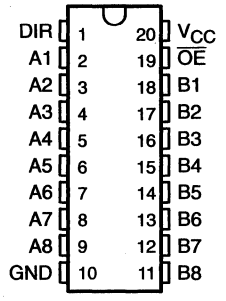
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

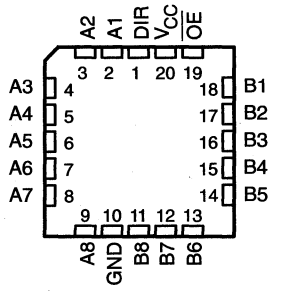
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT640 . . . J PACKAGE
SN74ABT640 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT640 . . . FK PACKAGE
(TOP VIEW)



description

The 'ABT640 bus transceiver is designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT640 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

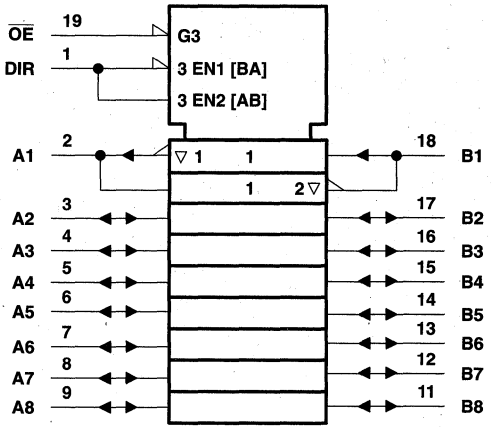
The SN54ABT640 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT640 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

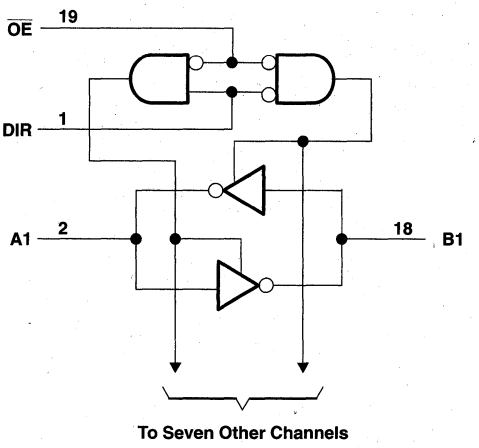
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT640 ..... 96 mA
SN74ABT640 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT640		SN74ABT640		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

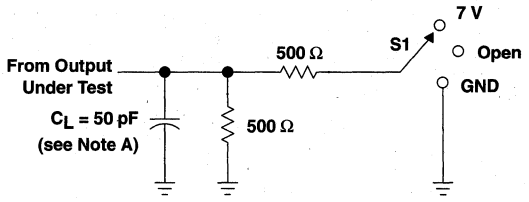
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT640		SN74ABT640		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		5	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

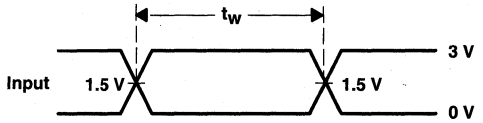
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT640		SN74ABT640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.7	4.2	1	5	1	4.9	ns
t_{PHL}			1.5	2.7	4.3	1.5	5	1.5	4.9	
t_{PZH}	$\overline{OE}$	A or B	1.5	3.7	4.9	1.5	6.9	1.5	5.8	ns
t_{PZL}			1.3	5	5.9	1.3	7.4	1.3	7.3	
t_{PHZ}	$\overline{OE}$	A or B	2.5	4.1	6.5	2.5	6.9	2.5	6.8	ns
t_{PLZ}			2	3.3	5.3	2	5.6	2	5.5	

PARAMETER MEASUREMENT INFORMATION

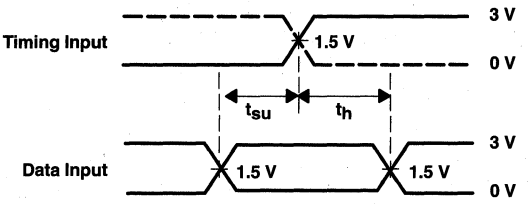


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

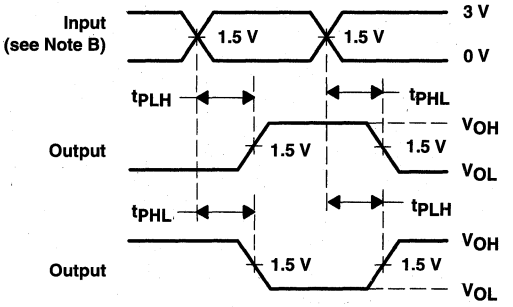
LOAD CIRCUIT FOR OUTPUTS



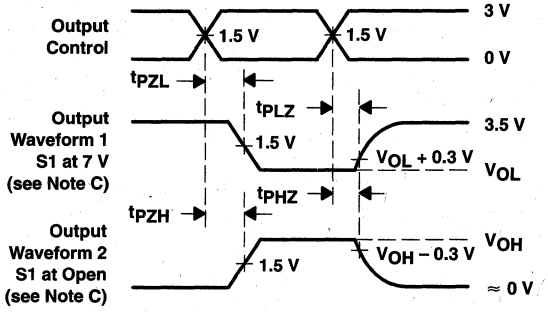
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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Figure 1. Load Circuit and Voltage Waveforms

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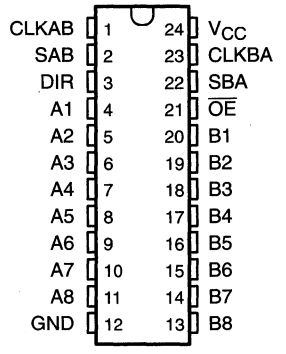
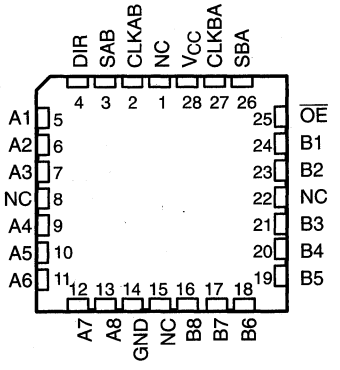
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT646 . . . JT PACKAGE
SN74ABT646 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′ABT646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

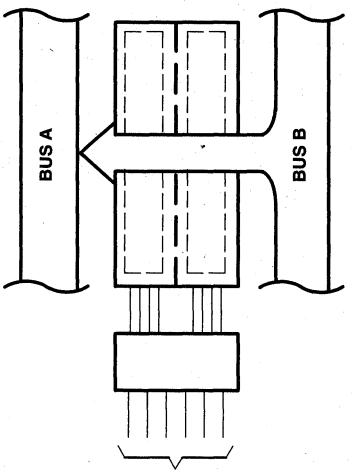
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT646 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

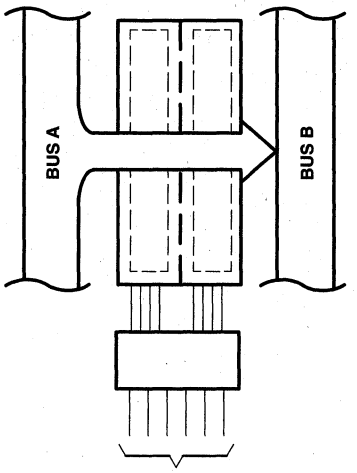
The SN54ABT646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT646 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



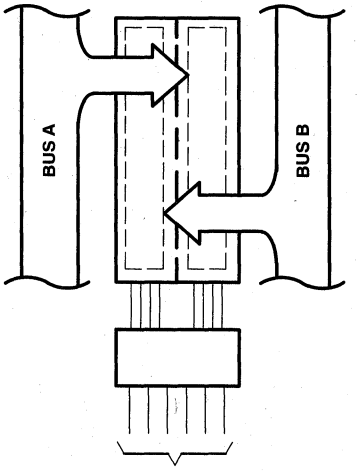
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



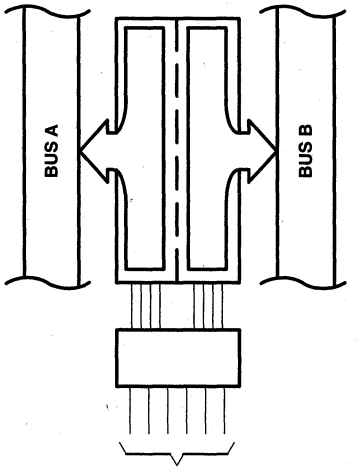
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

Figure 1. Bus-Management Functions

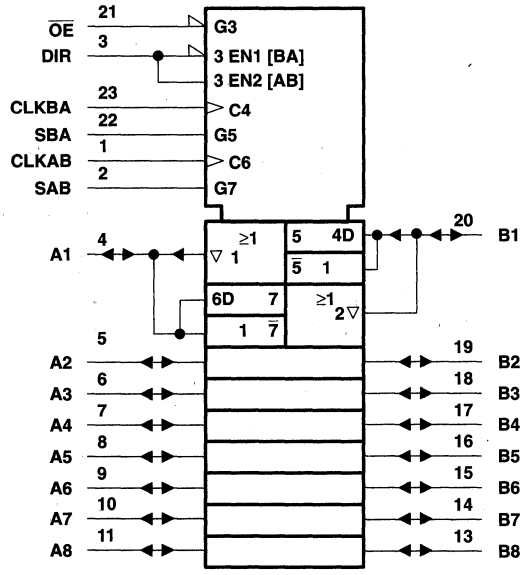
Pin numbers shown are for DB, DW, JT, and NT packages.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

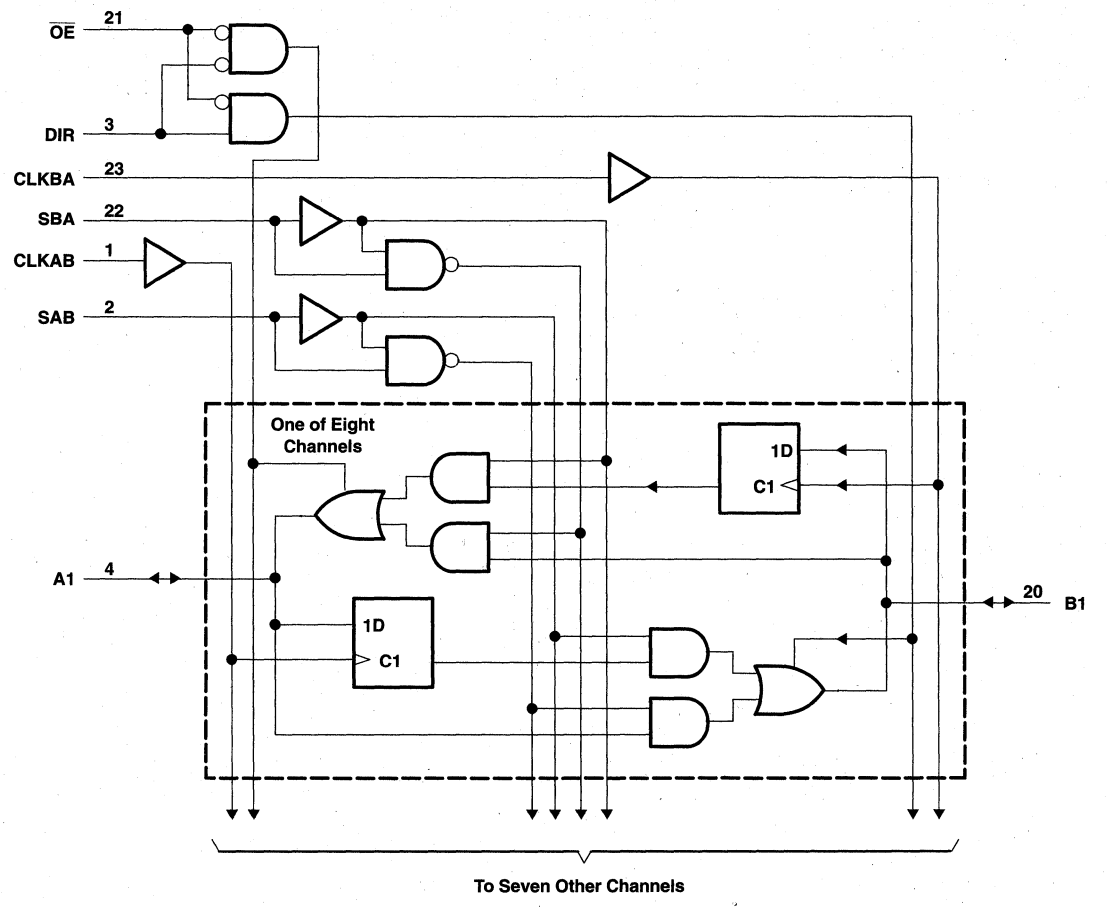
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT646 ..... 96 mA
SN74ABT646 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT646		SN74ABT646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT646		SN74ABT646		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Control inputs			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V				10¶		50		10¶	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V				−10¶		−50		−10¶	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O#	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			250		250		250	µA
		Outputs low			30		30		30	mA
		Outputs disabled			250		250		250	µA
ΔI_{CC}‖	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V	Control inputs		7						pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports		12						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ This data sheet limit may vary among suppliers.
# Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

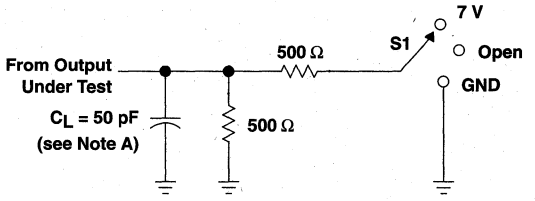
			V_{CC} = 5 V, T_A = 25°C		SN54ABT646		SN74ABT646		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low		4		4		4		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	High	3.5		3.5		3.5		ns
		Low	3		3		3		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑		0		0		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT646		SN74ABT646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125					125		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2.2	4	6.8			2.2	7.8	ns
t_{PHL}			1.7	4	7.4			1.7	8.4	
t_{PLH}	A or B	B or A	1.5	3	5.9			1.5	6.9	ns
t_{PHL}			1.5	3.3	5.9			1.5	6.9	
t_{PLH}	SAB or SBA†	B or A	1.5	4	6.1			1.5	7.1	ns
t_{PHL}			1.5	3.6	6.9			1.5	7.9	
t_{PZH}	$\overline{OE}$	A or B	1	4.3	5.3			1	6.3	ns
t_{PZL}			2.1	5.8	7.4			2.1	8.8	
t_{PHZ}	$\overline{OE}$	A or B	1.5	3.5	7.3			1.5	8.3	ns
t_{PLZ}			1.5	3	7			1.5	7.5	
t_{PZH}	DIR	A or B	1.2	4.5	5.7			1.2	6.7	ns
t_{PZL}			2.5	6.5	9			2.5	9.5	
t_{PHZ}	DIR	A or B	1.5	3.8	6.7			1.5	7.7	ns
t_{PLZ}			1.5	3.8	7.2			1.5	8.2	

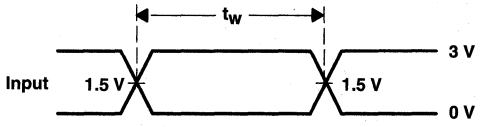
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

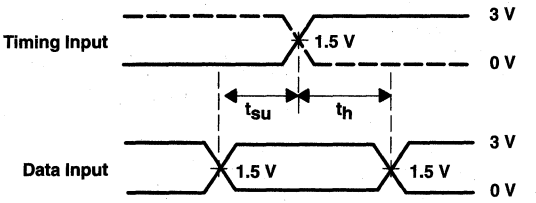


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

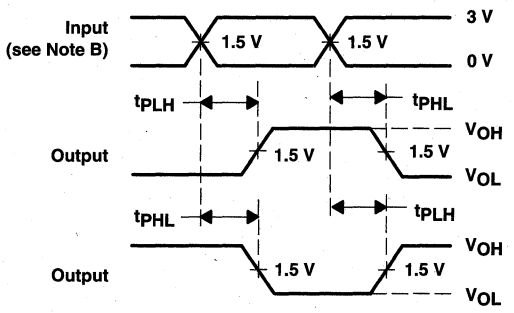
LOAD CIRCUIT FOR OUTPUTS



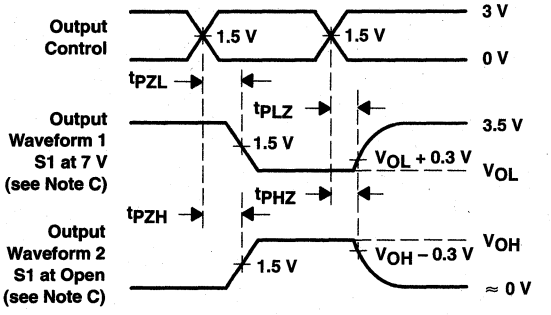
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



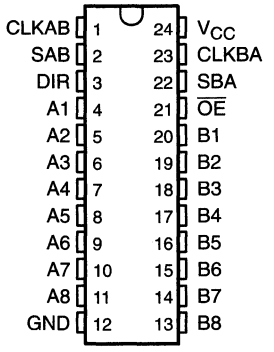
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

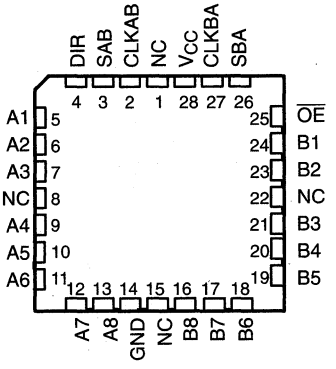
Figure 2. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT646A . . . JT PACKAGE
SN74ABT646A . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT646A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′ABT646A.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

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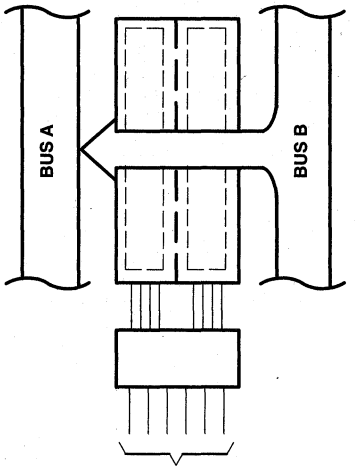
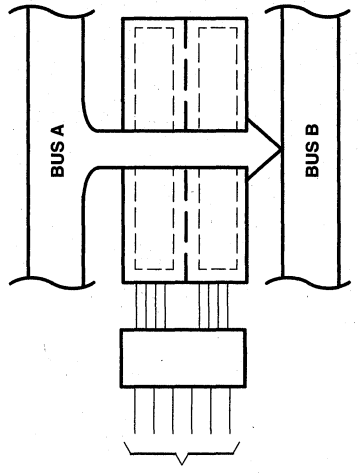


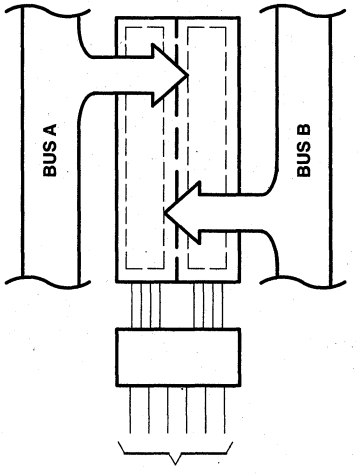
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



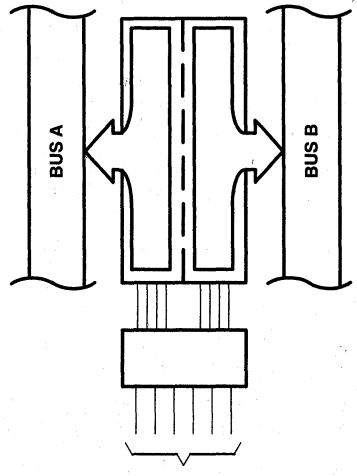
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

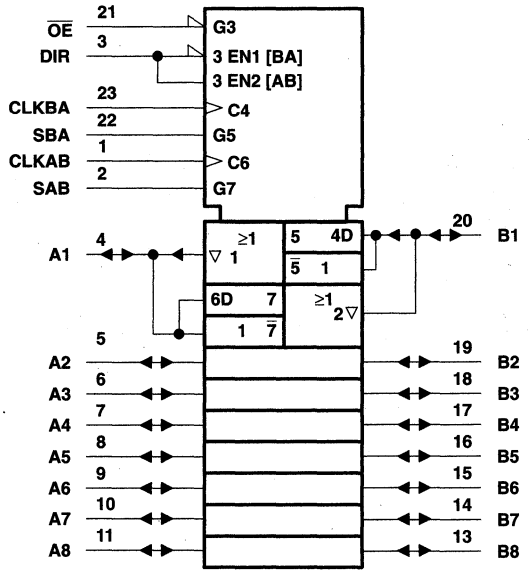
Pin numbers shown are for the DB, DW, JT, and NT packages.

FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

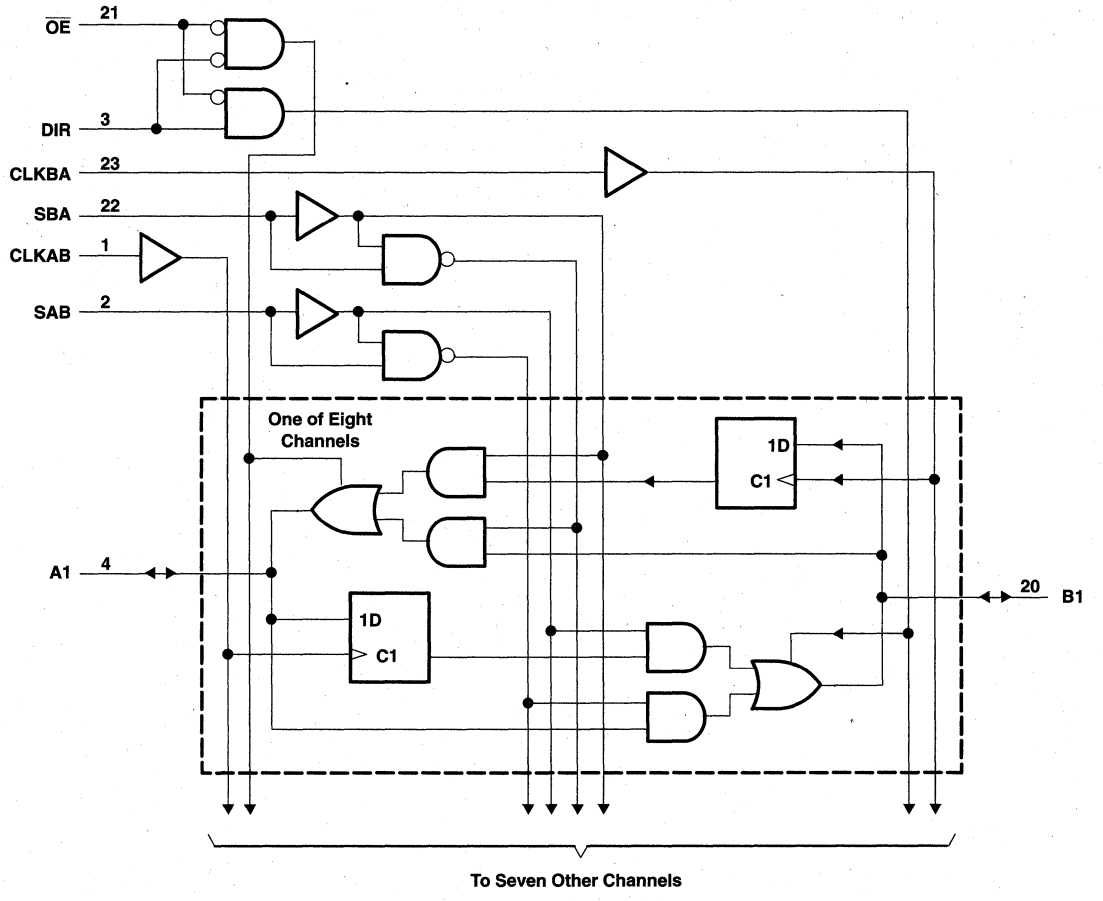
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT646A ..... 96 mA
SN74ABT646A ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT646A		SN74ABT646A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT646A		SN74ABT646A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Control inputs			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V				10¶		10¶		10¶	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V				−10¶		−10¶		−10¶	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O#	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			250		250		250	µA
		Outputs low			30		30		30	mA
		Outputs disabled			250		250		250	µA
ΔI_{CC}‖	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V	Control inputs		7						pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports		12						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ This data sheet limit may vary among suppliers.
# Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

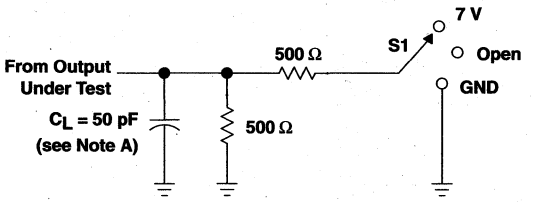
		V_{CC} = 5 V, T_A = 25°C		SN54ABT646A		SN74ABT646A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low	4		4		4		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3		3.5		3		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		1.5		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT646A		SN74ABT646A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	6.7	2.2	5.6	ns
t_{PHL}			1.7	4	5.1	1.2	6.7	1.7	5.6	
t_{PLH}	A or B	B or A	1.5	3	4.3	1.5	5	1.5	4.8	ns
t_{PHL}			1.5	3.3	4.6	1.5	5.6	1.5	5.4	
t_{PLH}	SAB or SBA†	B or A	1.5	4	5.1	1.5	7.8	1.5	6.5	ns
t_{PHL}			1.5	3.6	4.9	1.5	6.2	1.5	5.9	
t_{PZH}	$\overline{OE}$	A or B	1.5	4.3	5.3	1.5	7	1.5	6.3	ns
t_{PZL}			3	5.8	7.4	3	10.5	3	8.8	
t_{PHZ}	$\overline{OE}$	A or B	1.5	3.5	4.5	1	7.3	1.5	5	ns
t_{PLZ}			1.5	3	4	1.5	5.7	1.5	4.5	
t_{PZH}	DIR	A or B	1.5	4.5	5.7	1.5	7.3	1.5	6.7	ns
t_{PZL}			2.5	6.5	9	2.5	11	2.5	9.5	
t_{PHZ}	DIR	A or B	1.5	3.8	5	1	9	1.5	5.7	ns
t_{PLZ}			1.5	3.8	4.7	1.2	6.7	1.5	6	

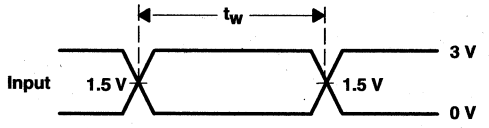
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

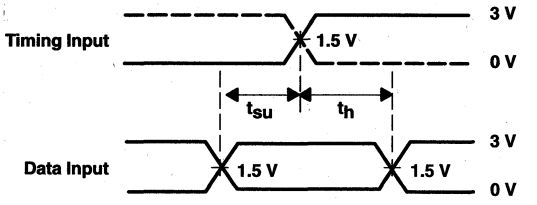


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

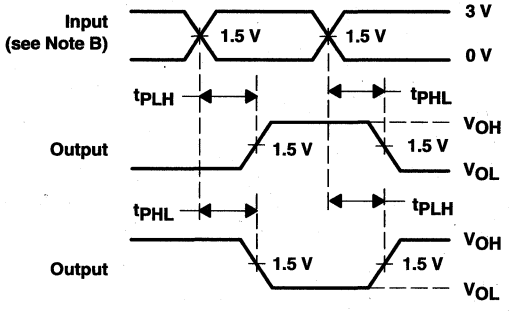
LOAD CIRCUIT FOR OUTPUTS



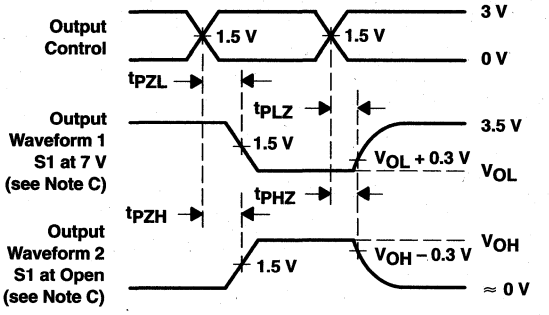
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



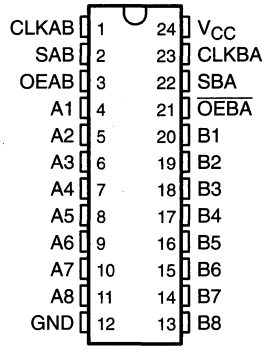
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

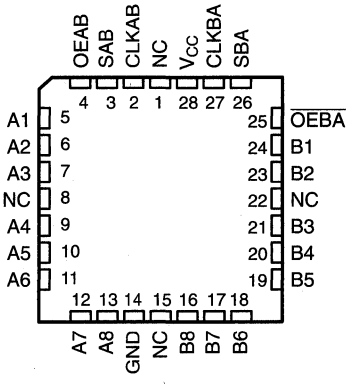
Figure 2. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Multiplexed Real-Time and Stored Data**
- **Inverting Data Paths**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT651 . . . JT PACKAGE
SN74ABT651 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT651 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. The select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′ABT651.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all the other data sources to the two sets of bus lines are at high impedance, each set will remain at its last state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

The SN74ABT651 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

description (continued)

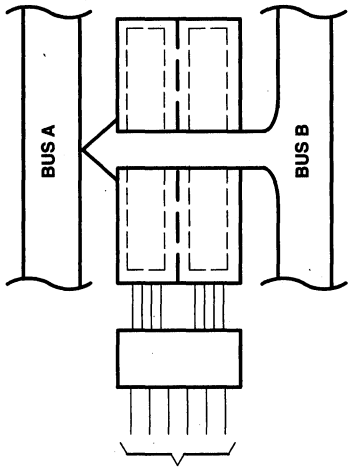
The SN54ABT651 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT651 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Output	Stored $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and stored B data to A bus

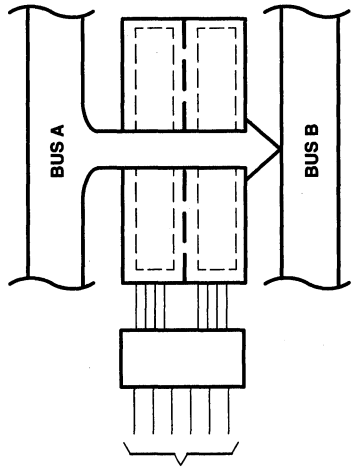
† The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ When select control is low, clocks can occur simultaneously so long as allowances are made for propagation delays from A to B (B to A) plus setup and hold times. When select control is high, clocks must be staggered in order to load both registers.



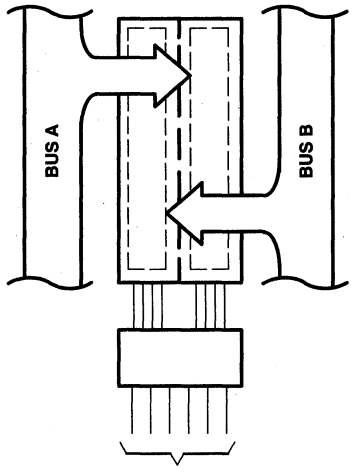
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



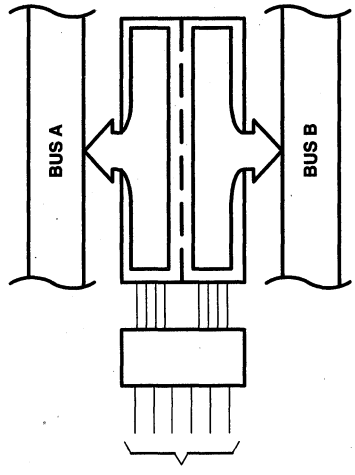
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



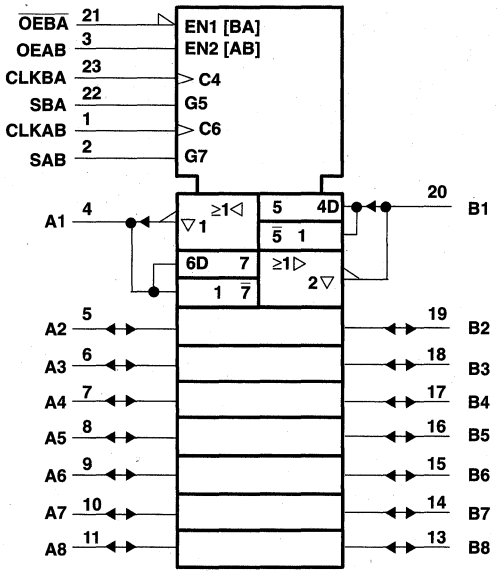
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

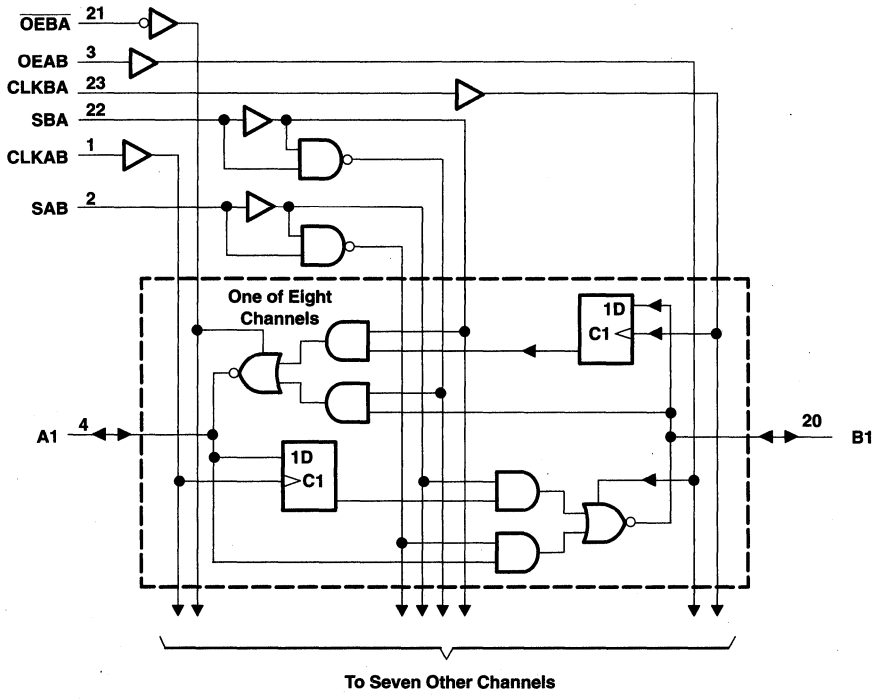
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT651	96 mA
SN74ABT651	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package	0.7 W
DW package	1 W
NT package	1.3 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT651		SN74ABT651		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT651		SN74ABT651		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Control inputs			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			250		250		250	µA
		Outputs low			30		30		30	mA
		Outputs disabled			250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V	Control inputs		6						pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports		7.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

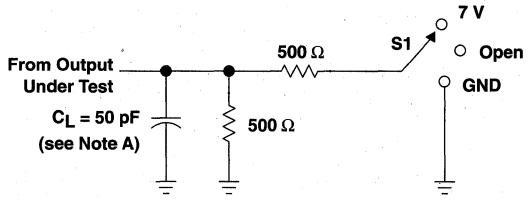
		V_{CC} = 5 V, T_A = 25°C		SN54ABT651		SN74ABT651		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low	4		4		4		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3		3		3		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		0		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT651		SN74ABT651		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	5.9	2.2	5.6	ns
t_{PHL}			1.7	4	5.1	1.7	5.9	1.7	5.6	
t_{PLH}	A or B	B or A	1.5	4	5.1	1.5	6.4	1.5	6.2	ns
t_{PHL}			1.5	3.3	4.6	1.5	5.6	1.5	5.4	
t_{PLH}	SAB or SBA†	A or B	1.5	4	5.1	1.5	6.8	1.5	6.5	ns
t_{PHL}			1.5	3.6	4.9	1.5	6.2	1.5	5.9	
t_{PZH}	$\overline{OEBA}$	A	1.3	3.6	4.6	1.3	5.9	1.3	5.8	ns
t_{PZL}			2.5	5.7	6.8	2.5	8.9	2.5	8.5	
t_{PHZ}	$\overline{OEBA}$	A	1.5	3.2	4.5	1.5	6.2	1.5	5	ns
t_{PLZ}			1.5	3	3.8	1.5	4.3	1.5	4.1	
t_{PZH}	OEAB	B	1.8	4.3	6.1	1.8	6.7	1.8	6.5	ns
t_{PZL}			2.9	5.5	6.5	2.9	7.6	2.9	7.4	
t_{PHZ}	OEAB	B	1.5	3.3	4.5	1.5	6.5	1.5	5.5	ns
t_{PLZ}			1.5	3.4	4.4	1.5	5.2	1.5	5.1	

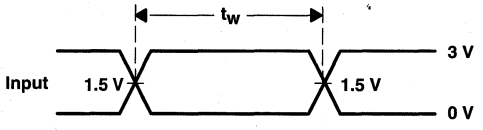
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

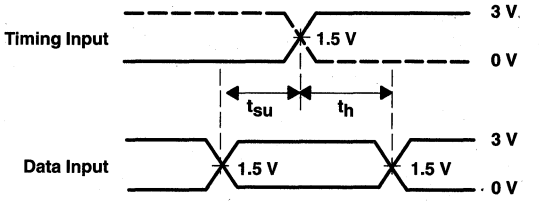


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

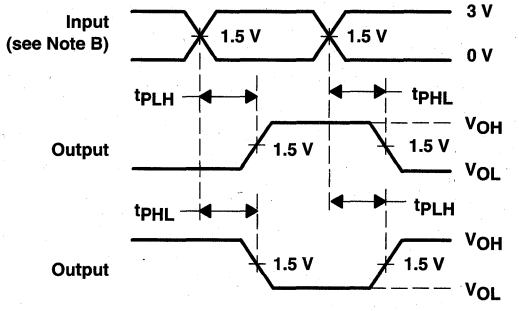
LOAD CIRCUIT FOR OUTPUTS



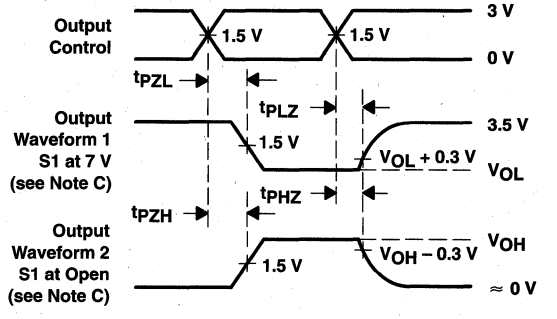
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



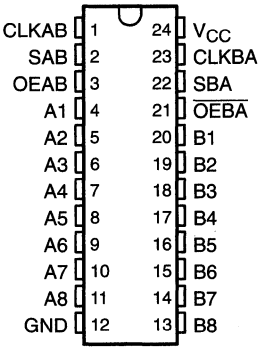
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

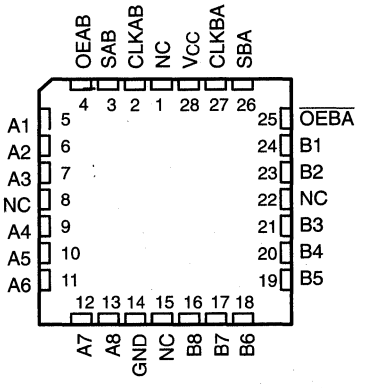
Figure 2. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT652 . . . JT PACKAGE
SN74ABT652 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT652 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

EPIC-IIB is a trademark of Texas Instruments Incorporated.

description (continued)

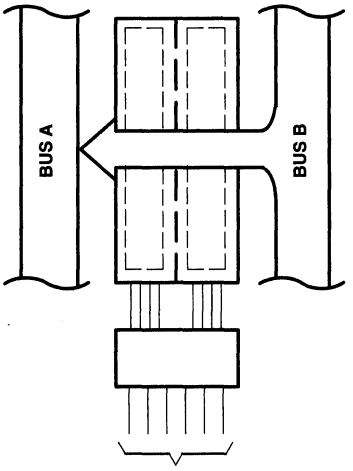
The SN74ABT652 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT652 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT652 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

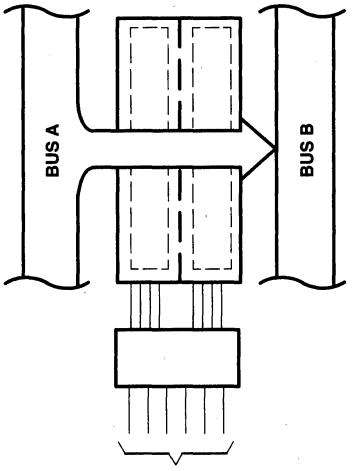
INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.



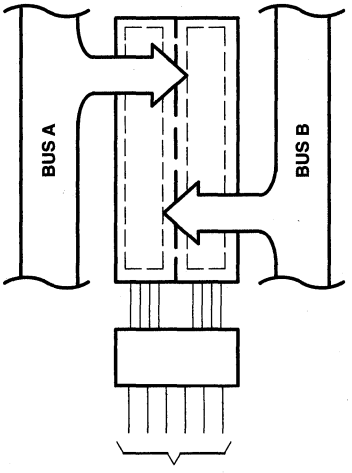
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



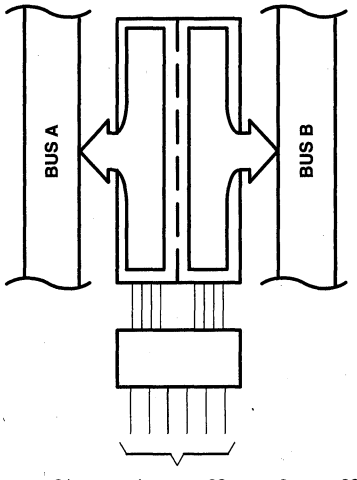
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



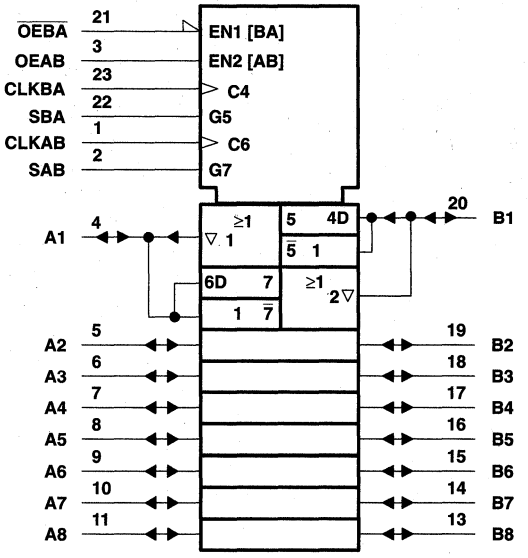
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

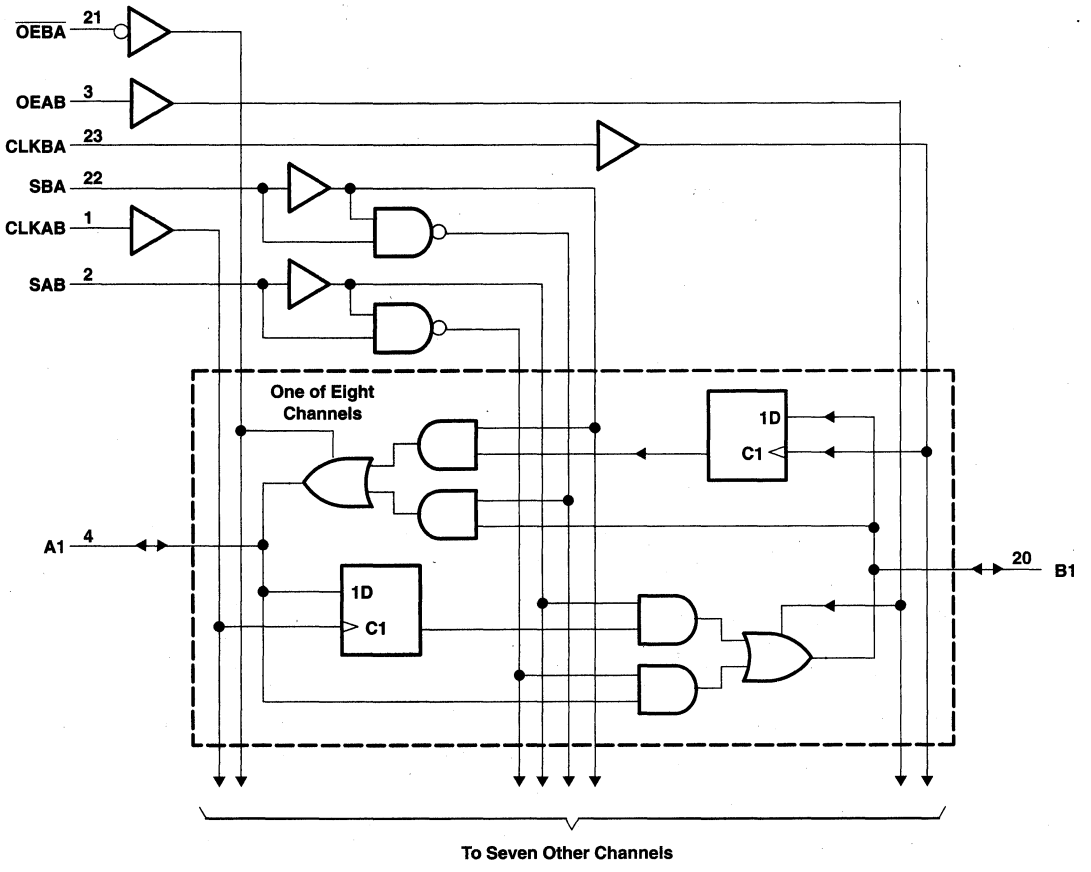
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT652 ..... 96 mA
SN74ABT652 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT652		SN74ABT652		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT652		SN74ABT652		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Control inputs			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			250		250		250	µA
		Outputs low			30		30		30	mA
		Outputs disabled			250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V	Control inputs		7						pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports		12						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

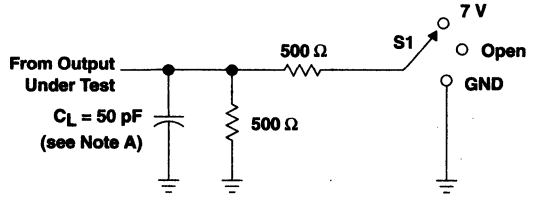
		V_{CC} = 5 V, T_A = 25°C		SN54ABT652		SN74ABT652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low	4		4		4		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3.5		3.5		3.5		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		0		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT652		SN74ABT652		UNIT
			MIN	TYP	MIN	MIN	MAX	MIN	MAX	
f_{max}			125	200		125		125		MHz
t_{PLH}	CLK	B or A	2.2	5.3	6.8	2.2	8.2	2.2	7.8	ns
t_{PHL}			1.7	5.9	7.4	1.7	8.8	1.7	8.4	
t_{PLH}	A or B	B or A	1.5	4.4	5.7	1.5	7	1.5	6.7	ns
t_{PHL}			1.5	4.4	5.7	1.5	7	1.5	6.7	
t_{PLH}	SAB or SBA†	B or A	1.5	4.6	5.9	1.5	7.4	1.5	6.9	ns
t_{PHL}			1.5	5.4	6.7	1.5	8	1.5	7.7	
t_{PZH}	$\overline{OEBA}$	A	1.3	3.3	4.6	1.3	6	1.3	5.8	ns
t_{PZL}			2.5	4.5	6.8	2.5	8.9	2.5	8.5	
t_{PHZ}	$\overline{OEBA}$	A	1.5	6.2	7.7	1.5	8.3	1.5	8.2	ns
t_{PLZ}			1.5	5	6.3	1.5	7.1	1.5	6.8	
t_{PZH}	OEAB	B	1.8	3.8	6.1	1.8	6.9	1.8	6.5	ns
t_{PZL}			2.9	4.9	6.5	2.9	7.6	2.9	7.4	
t_{PHZ}	OEAB	B	1.5	4.5	5.7	1.5	7.1	1.5	6.9	ns
t_{PLZ}			1.5	4.1	5.3	1.5	6.6	1.5	6.2	

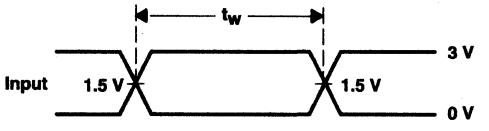
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

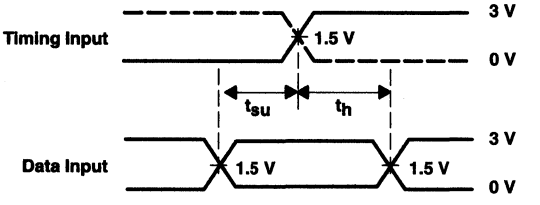


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

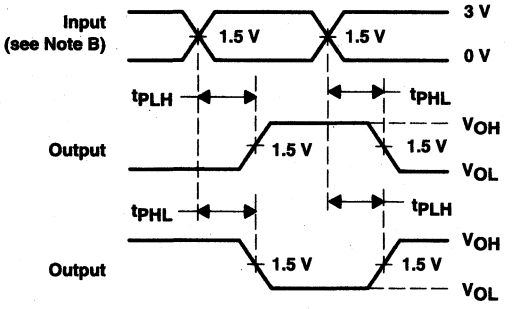
LOAD CIRCUIT FOR OUTPUTS



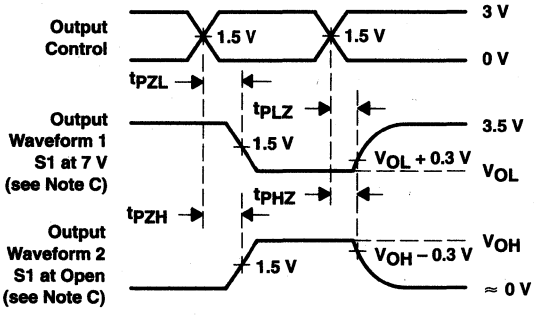
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



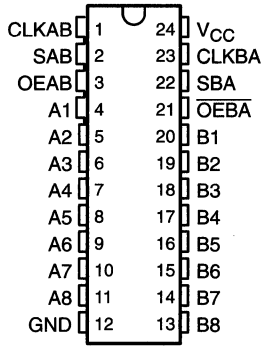
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

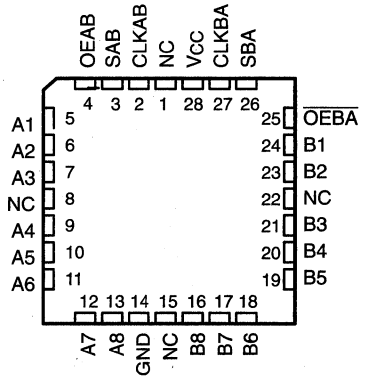
Figure 2. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT652A . . . JT PACKAGE
SN74ABT652A . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT652A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT652A.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

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description (continued)

The SN74ABT652A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT652A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT652A is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

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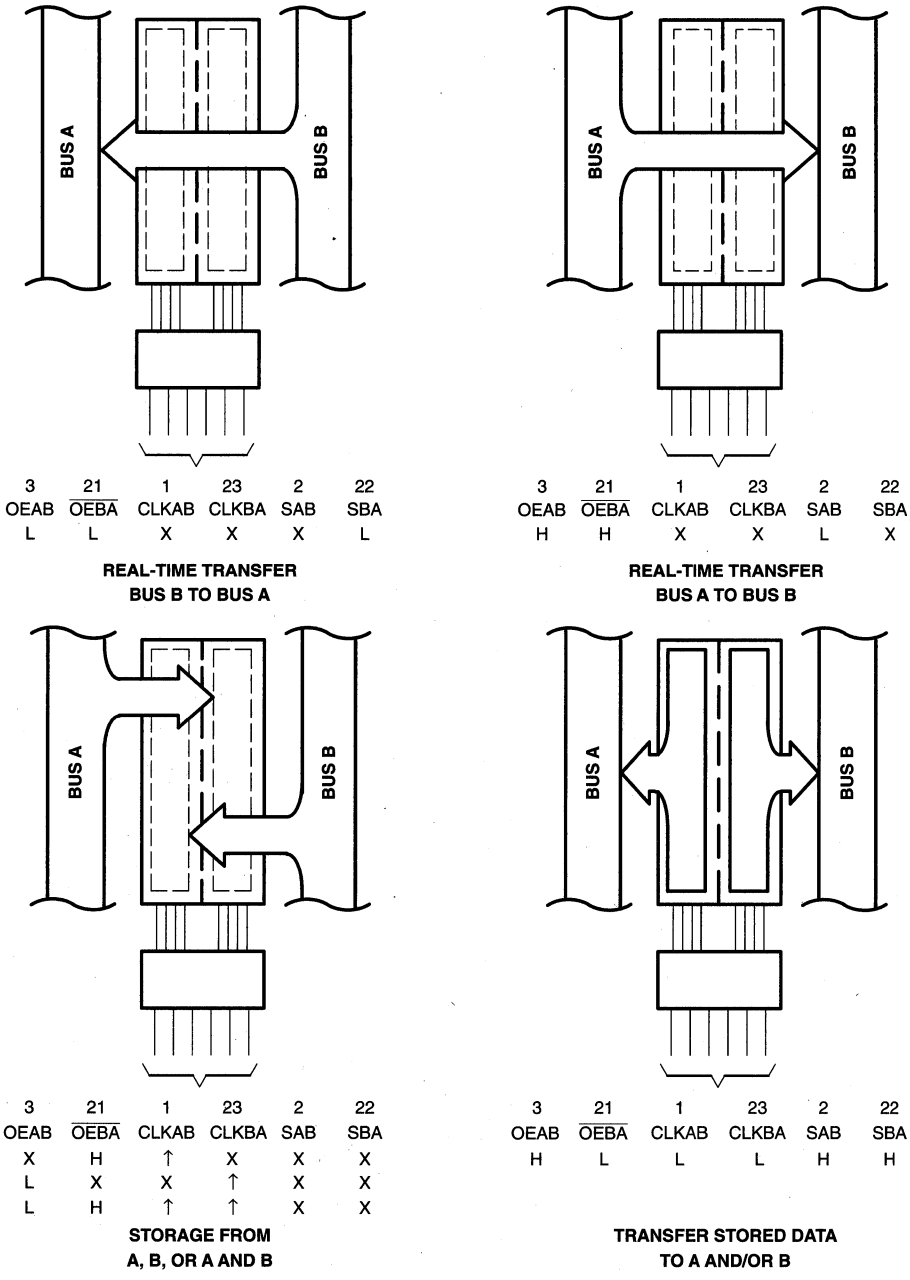
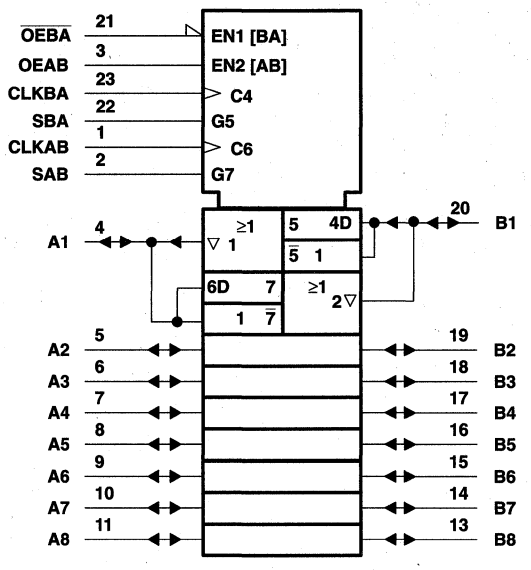


Figure 1. Bus-Management Functions

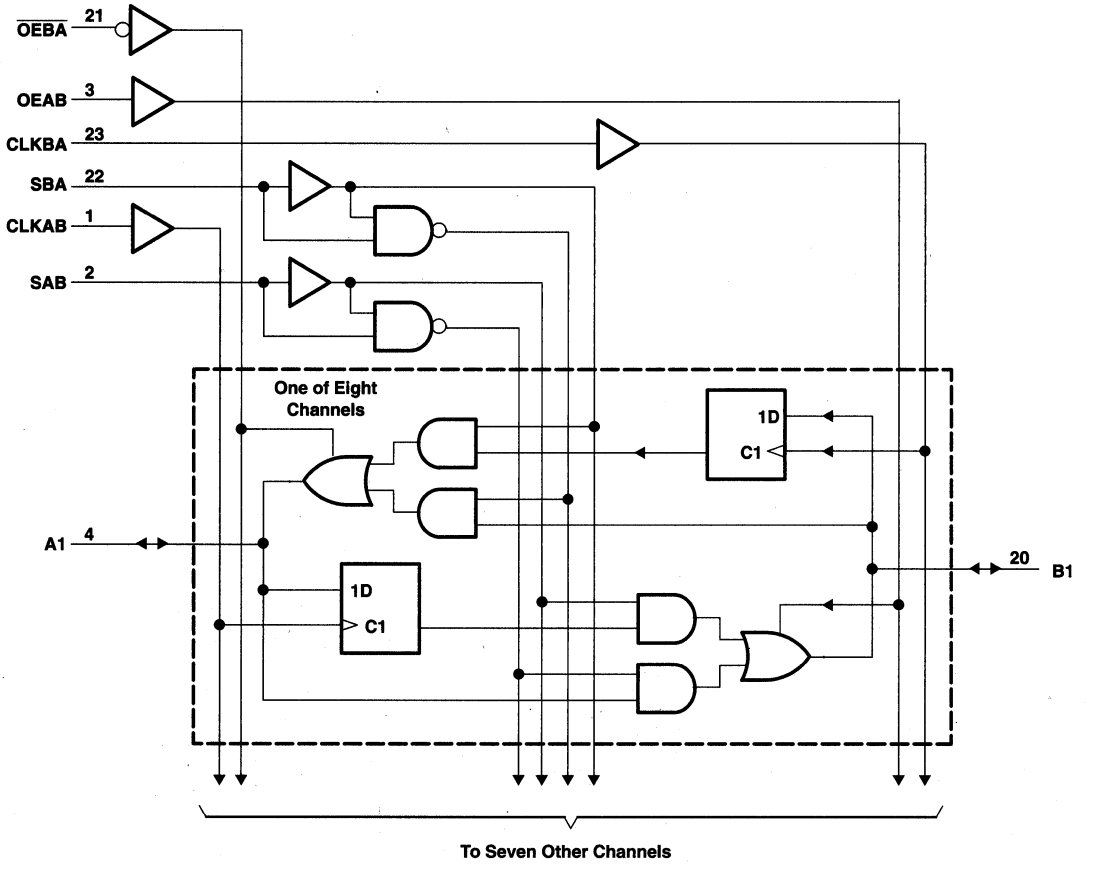
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT652A ..... 96 mA
SN74ABT652A ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT652A		SN74ABT652A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT652A		SN74ABT652A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Control inputs			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			250		250		250	µA
		Outputs low			30		30		30	mA
		Outputs disabled			250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V	Control inputs		7						pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports		12						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

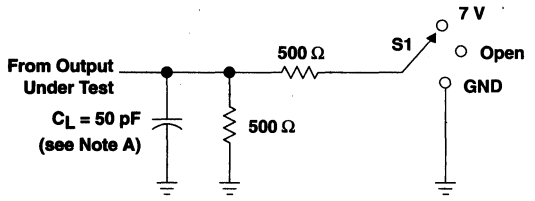
		V_{CC} = 5 V, T_A = 25°C		SN54ABT652A		SN74ABT652A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low	4		4		4		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3		3.5		3		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		1.5		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT652A		SN74ABT652A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125	200		125		125		MHz
t_{PLH}	CLK	B or A	2.2	4	5.1	1.7	5.9	2.2	5.6	ns
t_{PHL}			1.7	4	5.1	1.7	5.9	1.7	5.6	
t_{PLH}	A or B	B or A	1.5	3	4.3	1	5	1.5	4.8	ns
t_{PHL}			1.5	3.3	4.6	1	5.6	1.5	5.4	
t_{PLH}	SAB or SBA†	B or A	1.5	4	5.1	1.5	6.8	1.5	6.5	ns
t_{PHL}			1.5	3.6	4.9	1.5	6.2	1.5	5.9	
t_{PZH}	$\overline{OEBA}$	A	2	3.6	4.6	2	6.8	2	5.8	ns
t_{PZL}			3	5.7	6.8	3	9.2	3	8.5	
t_{PHZ}	$\overline{OEBA}$	A	1.5	3.2	4.5	1	7.5	1.5	5	ns
t_{PLZ}			1.5	3	3.8	1	4.6	1.5	4.1	
t_{PZH}	OEAB	B	2	4.3	6.1	2	7.8	2	6.5	ns
t_{PZL}			3	5.5	6.5	3	8.9	3	7.4	
t_{PHZ}	OEAB	B	1.5	3.3	4.5	1	8	1.5	5.5	ns
t_{PLZ}			1.5	3.4	4.4	1.5	6.8	1.5	5.1	

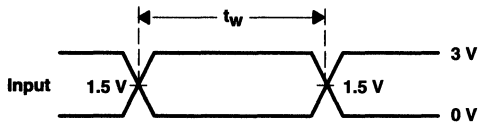
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

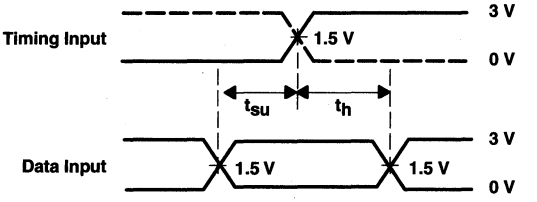


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

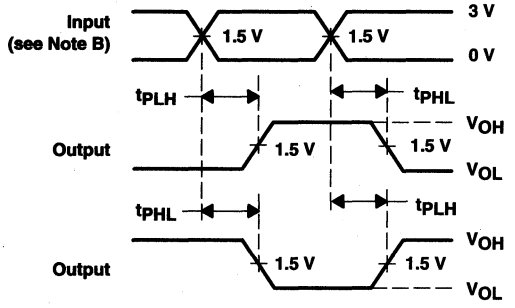
LOAD CIRCUIT FOR OUTPUTS



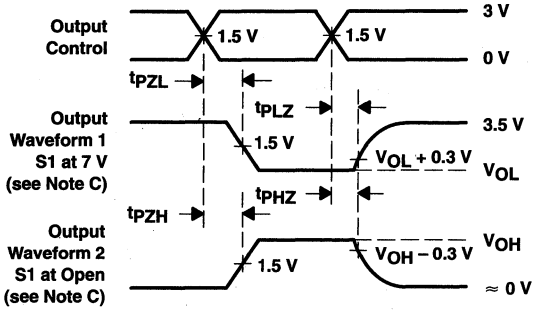
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
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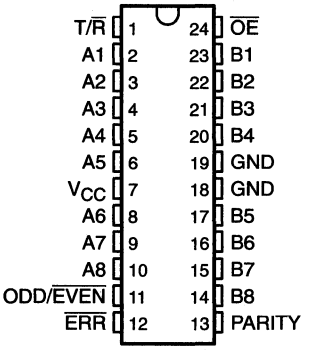
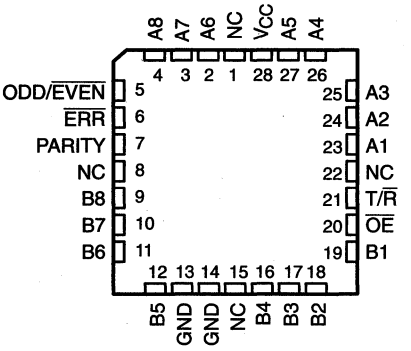
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT657 . . . JT PACKAGE
SN74ABT657 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT657 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT657 contains eight noninverting buffers with parity generator/checker circuits and control signals. The transmit/receive (T/$\overline{R}$) input determines the direction of data flow. When T/$\overline{R}$ is high, data flows from the A port to the B port (transmit mode); when T/$\overline{R}$ is low, data flows from the B port to the A port (receive mode). When the output-enable ($\overline{OE}$) input is high, both the A and B ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level on the ODD/$\overline{EVEN}$ input. PARITY carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the A bus is polled to determine the number of high bits, PARITY is set to the logic level that maintains the parity sense selected by the level at the ODD/$\overline{EVEN}$ input. For example, if ODD/$\overline{EVEN}$ is low (even parity selected) and there are five high bits on the A bus, then PARITY is set to the logic high level so that an even number of the nine total bits (eight A-bus bits plus parity bit) are high.

In the receive mode, after the B bus is polled to determine the number of high bits, the error ($\overline{ERR}$) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if ODD/$\overline{EVEN}$ is high (odd parity selected), PARITY is high, and there are three high bits on the B bus, then $\overline{ERR}$ is low, indicating a parity error.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT657 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

PRODUCT PREVIEW

EPIC-IIB is a trademark of Texas Instruments Incorporated.

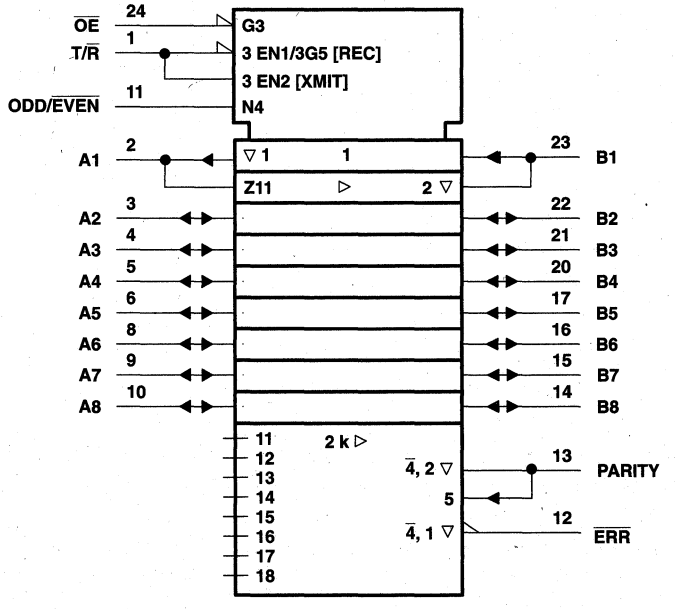
description (continued)

The SN54ABT657 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT657 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$		$\overline{ERR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†



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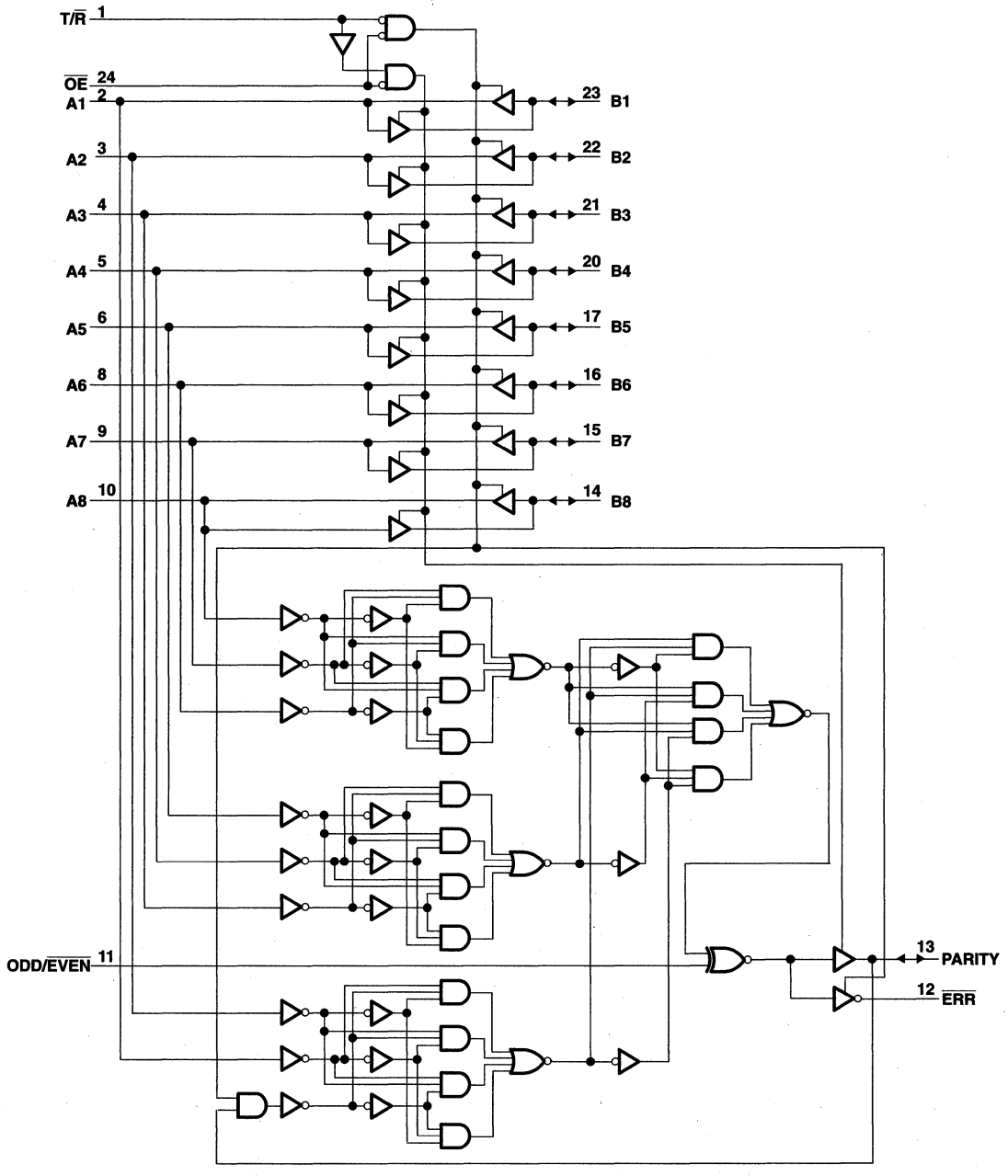
Pin numbers shown are for the DB, DW, JT, and NT packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT657 ..... 96 mA
SN74ABT657 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT657		SN74ABT657		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT657		SN74ABT657		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2§					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55§				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			250		250		250	µA
			Outputs low			30		30		30	mA
			Outputs disabled			250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs								pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports								pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

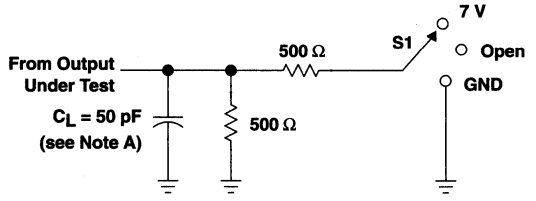
PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT657		SN74ABT657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.1	3.3	5	1.1		1.1	5.5	ns
t_{PHL}			1.2	3	4.3	1.2		1.2	4.8	
t_{PLH}	A	PARITY	2.6	6.5	8.7	2.6		2.6	10.1	ns
t_{PHL}			3.2	7	9.1	3.2		3.2	10.6	
t_{PLH}	ODD/$\overline{\text{EVEN}}$	PARITY, $\overline{\text{ERR}}$	1.7	5	6.6	1.7		1.7	7.3	ns
t_{PHL}			1.9	5	6.6	1.9		1.9	7.3	
t_{PLH}	B	$\overline{\text{ERR}}$	5.3	9.2	11.7	5.3		5.3	13.8	ns
t_{PHL}			5.2	9.6	12.1	5.2		5.2	14.5	
t_{PLH}	PARITY	$\overline{\text{ERR}}$	2.8	6	7.6	2.8		2.8	9.4	ns
t_{PHL}			3.5	6.4	8	3.5		3.5	9.4	
t_{PZH}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$	1.3	3.8	5.6	1.3		1.3	6.6	ns
t_{PZL}			1.9	4.4	7	1.9		1.9	8.2	
t_{PHZ}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$	3.1	5.1	7	3.1		3.1	7.6	ns
t_{PLZ}			3.4	5.4	7.6	3.4		3.4	8.1	

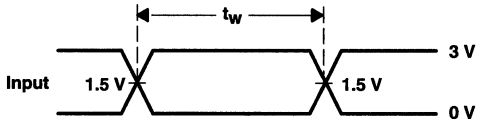
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

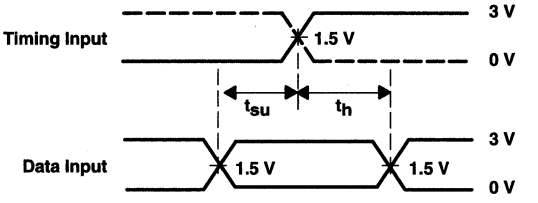


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

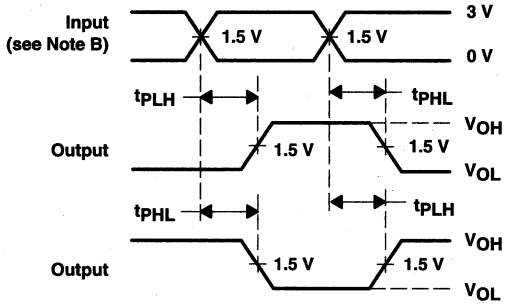
LOAD CIRCUIT FOR OUTPUTS



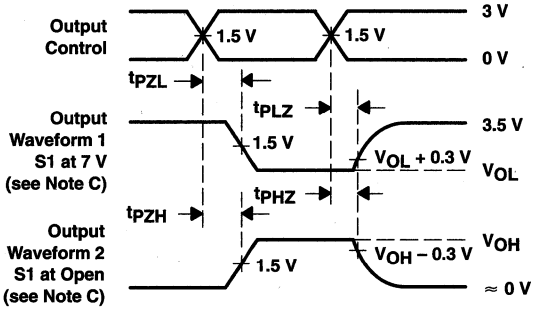
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

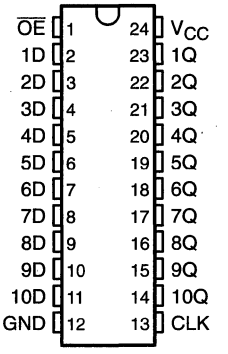
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

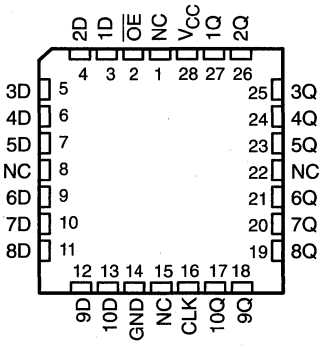
PRODUCT PREVIEW

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT821 . . . JT PACKAGE
SN74ABT821 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT821 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT821 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

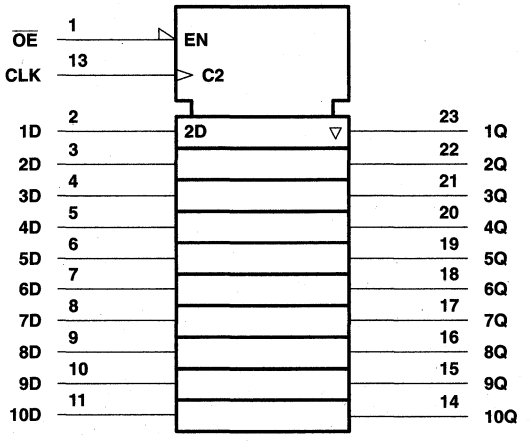
The SN54ABT821 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT821 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

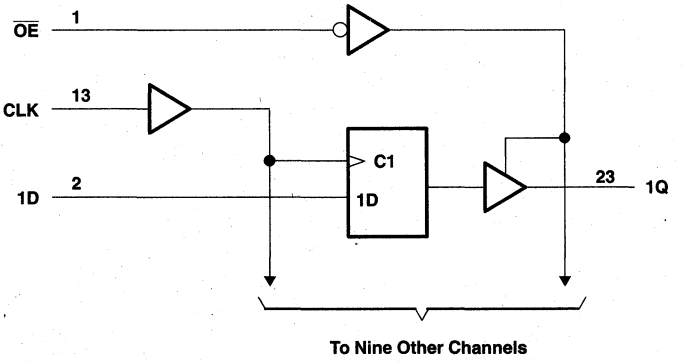
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT821 ..... 96 mA
SN74ABT821 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT821		SN74ABT821		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT821		SN74ABT821		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−140	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	38		38		38	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			4						pF
C_o	V_O = 2.5 V or 0.5 V			7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

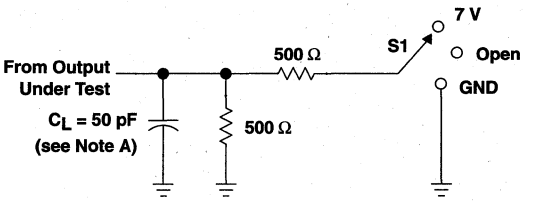
			V_{CC} = 5 V, T_A = 25°C		SN54ABT821		SN74ABT821		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low	High	2.9		2.9		2.9		ns
		Low	3.8		3.8		3.8		
t_{su}	Setup time, data before CLK↑		2.1		2.1		2.1		ns
t_h	Hold time, data after CLK↑		1.3		1.3		1.3		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT821		SN74ABT821		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	CLK	Q	1.6†	4.1	5.6	1.6†	6.9	1.6†	6.2	ns
t_{PHL}			2.1†	4.6	6.2	2.1†	6.9	2.1†	6.7	
t_{PZH}	$\overline{OE}$	Q	1	3	4.5	1	5.5	1	5.3	ns
t_{PZL}			2.2	4.1	5.6	2.2	6.4	2.2	6.3	
t_{PHZ}	$\overline{OE}$	Q	2.7	4.7	6.2	2.7	6.9	2.7	6.7	ns
t_{PLZ}			1.7†	4.6	6.1	1.7†	7	1.7†	6.5	

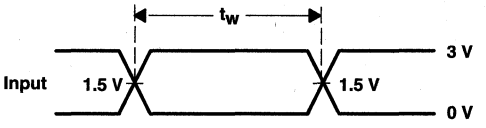
† This data sheet limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

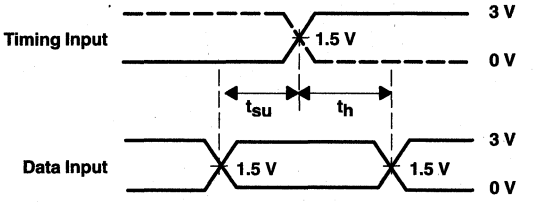


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

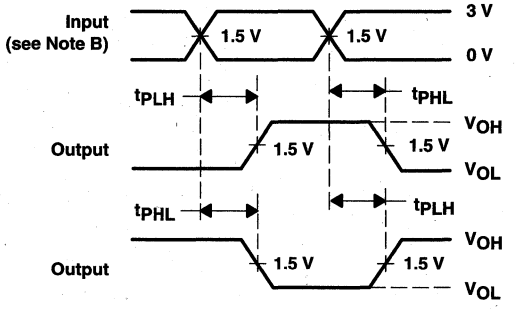
LOAD CIRCUIT FOR OUTPUTS



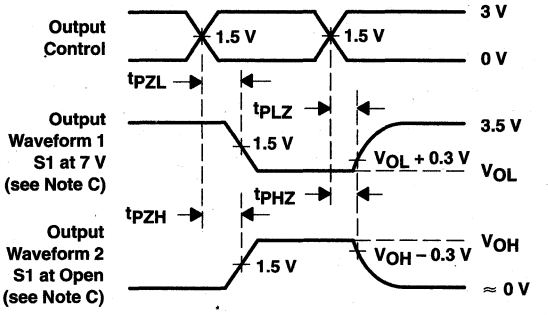
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



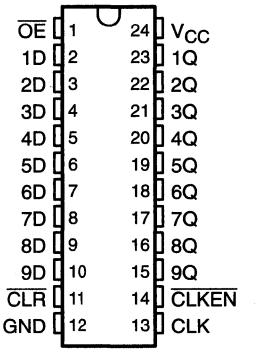
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

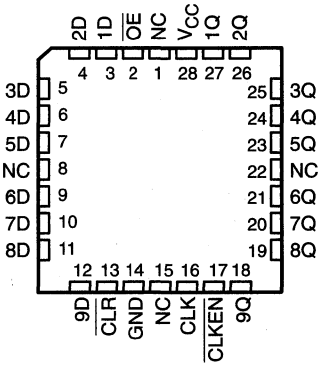
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT823 . . . JT PACKAGE
SN74ABT823 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT823 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

With the clock-enable ($\overline{CLKEN}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'ABT823 has noninverting data (D) inputs. Taking the clear ($\overline{CLR}$) input low causes the nine Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT823 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

PRODUCT PREVIEW

EPIC-IIB is a trademark of Texas Instruments Incorporated.

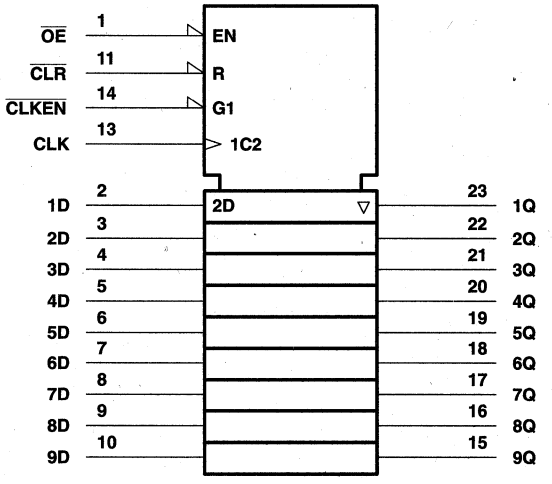
description (continued)

The SN54ABT823 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT823 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

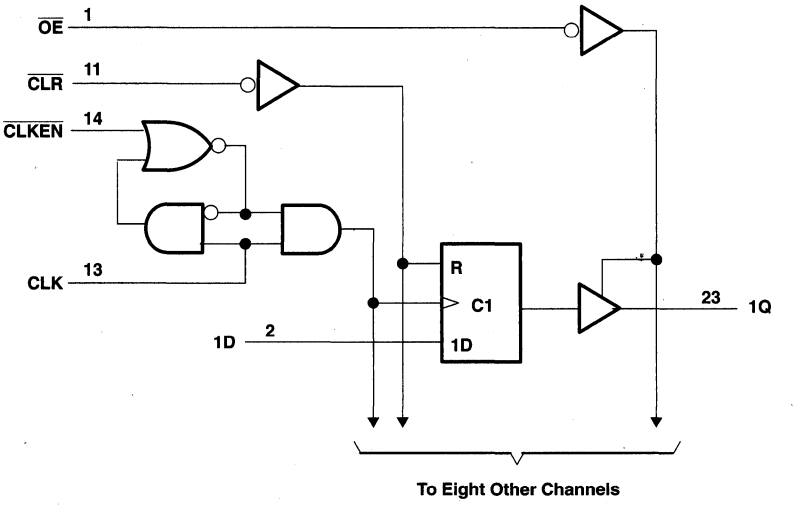
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT823	96 mA
SN74ABT823	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package	0.7 W
DW package	1 W
NT package	1.3 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

		SN54ABT823		SN74ABT823		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT823		SN74ABT823		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				10§		10§		10§	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−10§		−10§		−10§	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−140	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V									pF
C_o	V_O = 2.5 V or 0.5 V									pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

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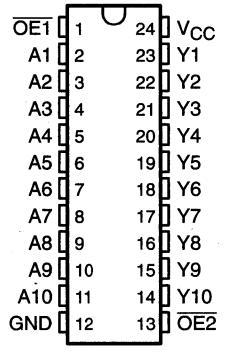
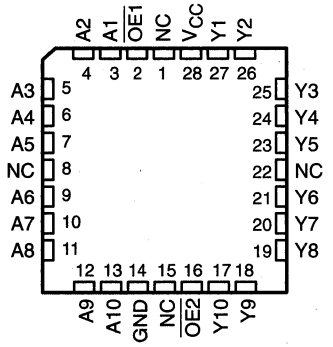
SN54ABT827 . . . JT PACKAGE
SN74ABT827 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT827 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 10-bit buffers or bus drivers provide a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The 'ABT827 provides true data at its outputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT827 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

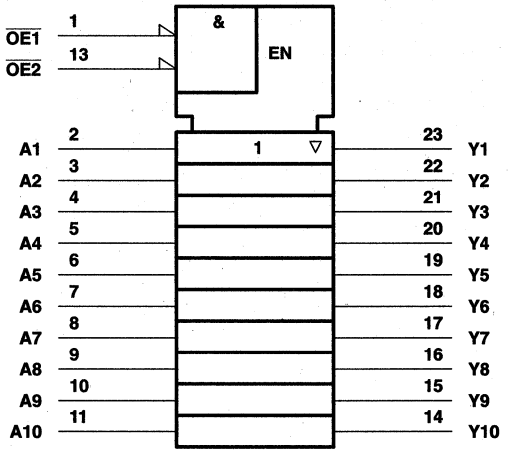
The SN54ABT827 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT827 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

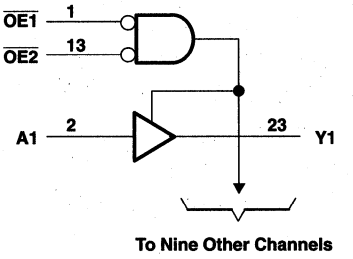
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and the NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT827 ..... 96 mA
SN74ABT827 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT827		SN74ABT827		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT827		SN74ABT827		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				10§		10		10§	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−10§		−10		−10§	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−140	−225§	−50	−225§	−50	−225§	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		80	250		250		250	µA
		Outputs low		35	40§		40		40§	mA
		Outputs disabled		80	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	µA
		Control inputs			1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			4						pF
C_o	V_O = 2.5 V or 0.5 V			8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT827		SN74ABT827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.1	2.6	4.4	1.1	7.5	1.1	4.8	ns
t_{PHL}			1.1	2.3	4.1	1.1	4.8	1.1	4.7	
t_{PZH}	$\overline{OE}$	Y	1†	3.2	5.1	1	6	1†	5.9	ns
t_{PZL}			1†	3.3	5.9	1	7.1	1†	6.9	
t_{PHZ}	$\overline{OE}$	Y	2	4.9	6.3	2	7	2	6.8	ns
t_{PLZ}			1.3†	4.2	6.6	1.3	7.9	1.3†	6.9	

† This data sheet limit may vary among suppliers.

TEXAS INSTRUMENTS
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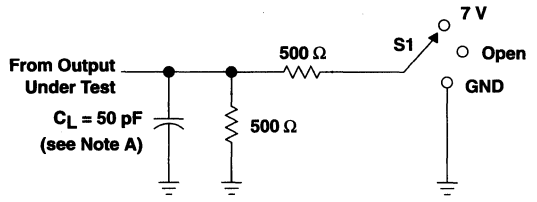
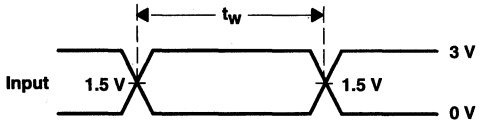
PARAMETER MEASUREMENT INFORMATION

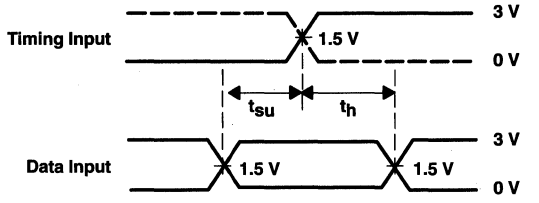


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

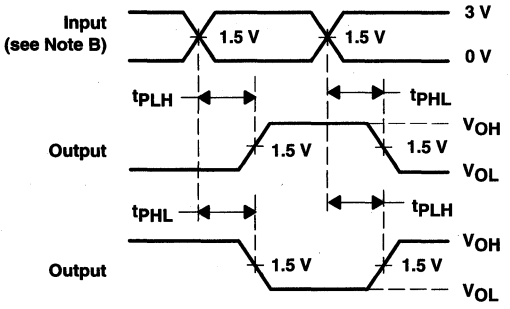
LOAD CIRCUIT FOR OUTPUTS



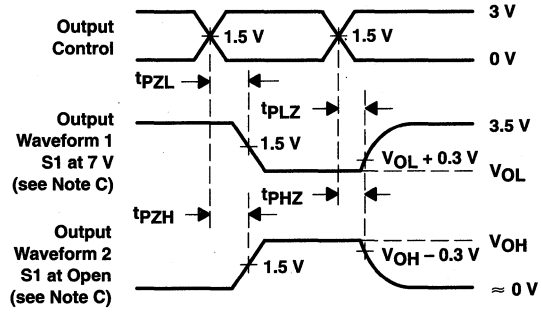
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

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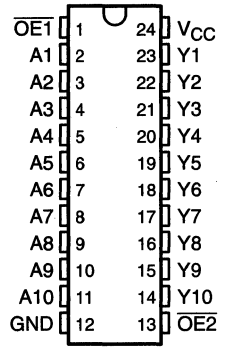

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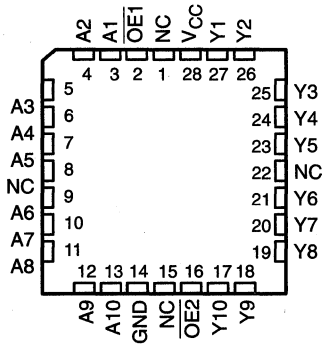

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description

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The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The 'ABT828 provides inverting data at its outputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT828 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT828 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT828 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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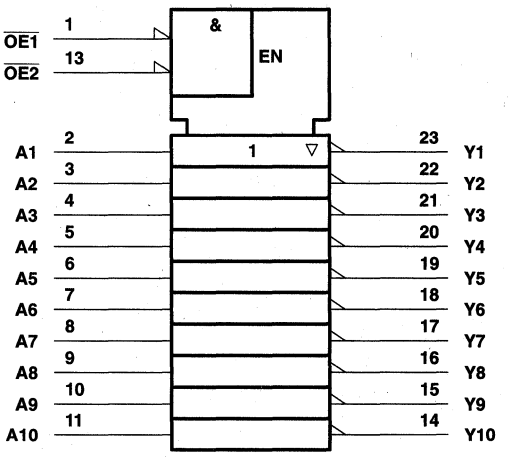
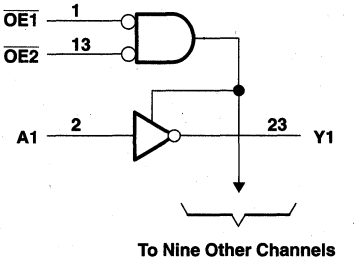
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT828 ..... 96 mA
SN74ABT828 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.7 W
NT package ..... 1.3 W
DW package ..... 1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

		SN54ABT828		SN74ABT828		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT828		SN74ABT828		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−140	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	µA
		Control inputs			1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			4						pF
C_o	V_O = 2.5 V or 0.5 V			7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

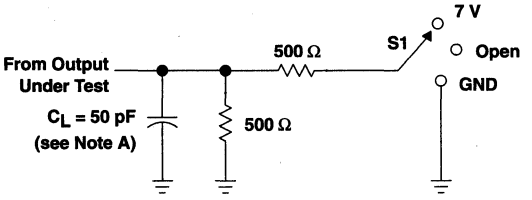
PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT828		SN74ABT828		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.1	3	4.4	1.1		1.1	4.8	ns
t_{PHL}			1.1	2.9	4.1	1.1		1.1	4.7	
t_{PZH}	$\overline{OE}$	Y	1.6	3.7	5.1	1.6		1.6	5.9	ns
t_{PZL}			2.6	4.6	5.9	2.6		2.6	6.9	
t_{PHZ}	$\overline{OE}$	Y	2	4.8	6.3	2		2	6.8	ns
t_{PLZ}			2.5	5.1	6.6	2.5		2.5	6.9	

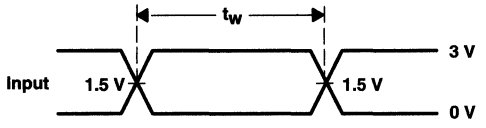
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

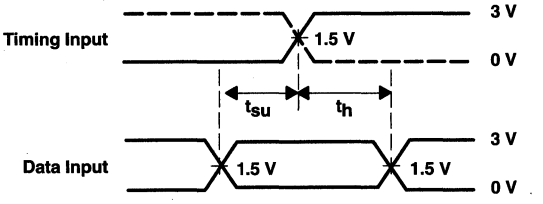


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

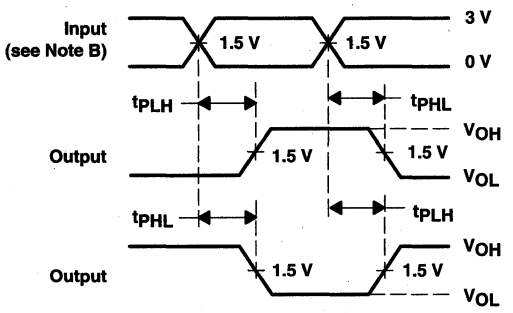
LOAD CIRCUIT FOR OUTPUTS



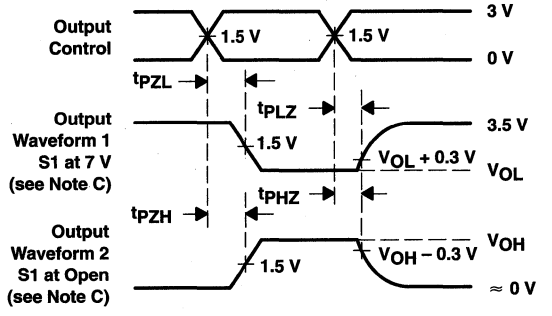
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

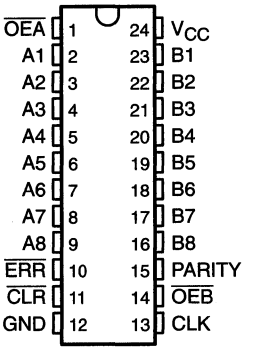
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

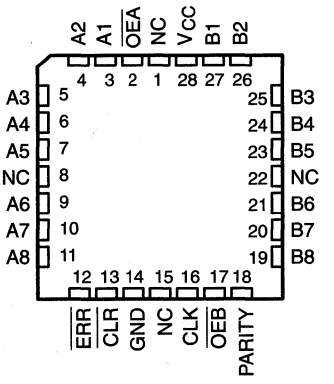
D3781, FEBRUARY 1991 – REVISED OCTOBER 1992

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Parity Error Flag With Parity Generator/Checker**
- **Register for Storage of the Parity Error Flag**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT833 . . . JT PACKAGE
SN74ABT833 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT833 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT833 8-bit to 9-bit parity transceiver is designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error ($\overline{ERR}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$ and $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT833 provides true data at its outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the $\overline{ERR}$ flag. The parity-error output is clocked into the register on the rising edge of the clock (CLK) input. The error flag register is cleared with a low pulse on the clear ($\overline{CLR}$) input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT833 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT833 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT833 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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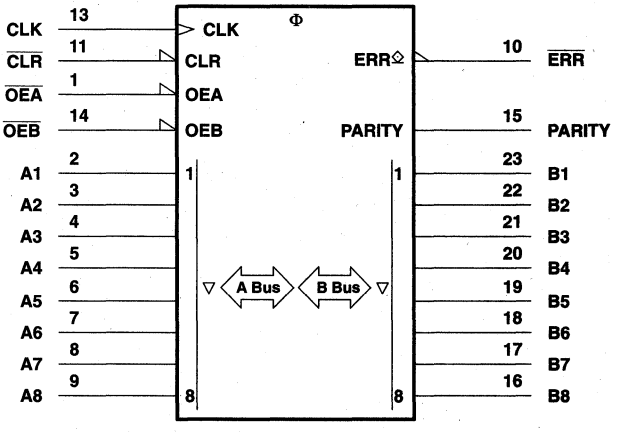
FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ OF H's	Bi† Σ OF H's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	H	No↑	X	X	Z	Z	Z	NC	Isolation§
		L	No↑	X					H	
		H	↑	Odd					H	
		H	↑	Even					L	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume the $\overline{ERR}$ output was previously high.
§ In this mode, the $\overline{ERR}$ output (when clocked) shows inverted parity of the A bus.

logic symbol¶



¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

PRODUCT PREVIEW

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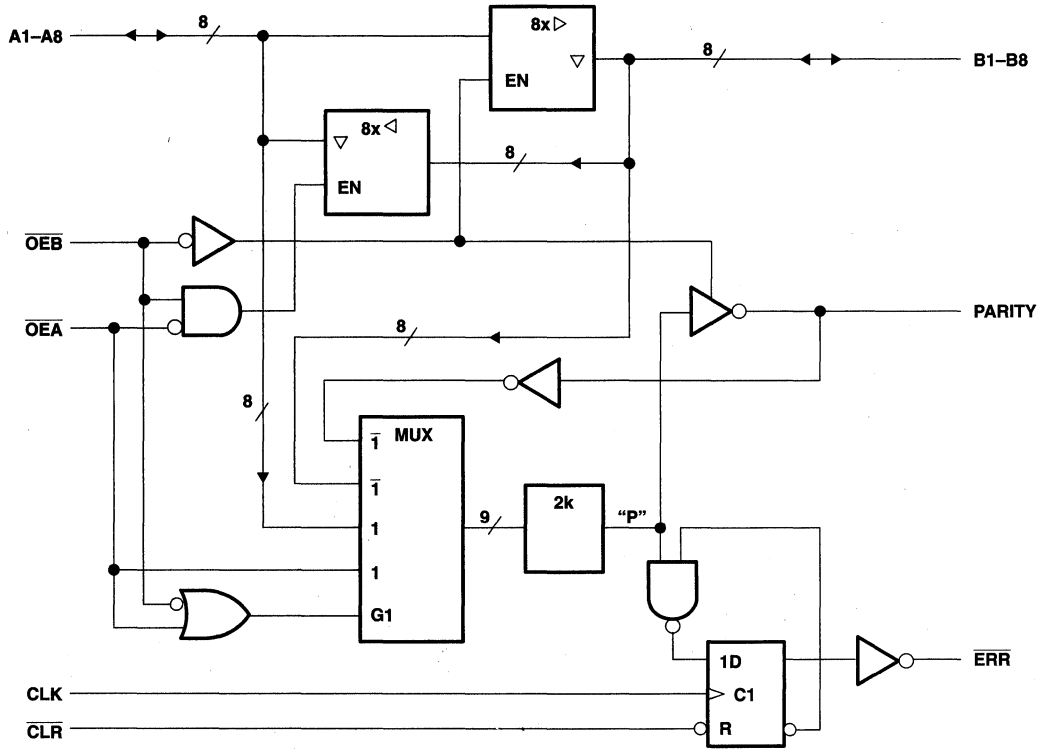
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram (positive logic)



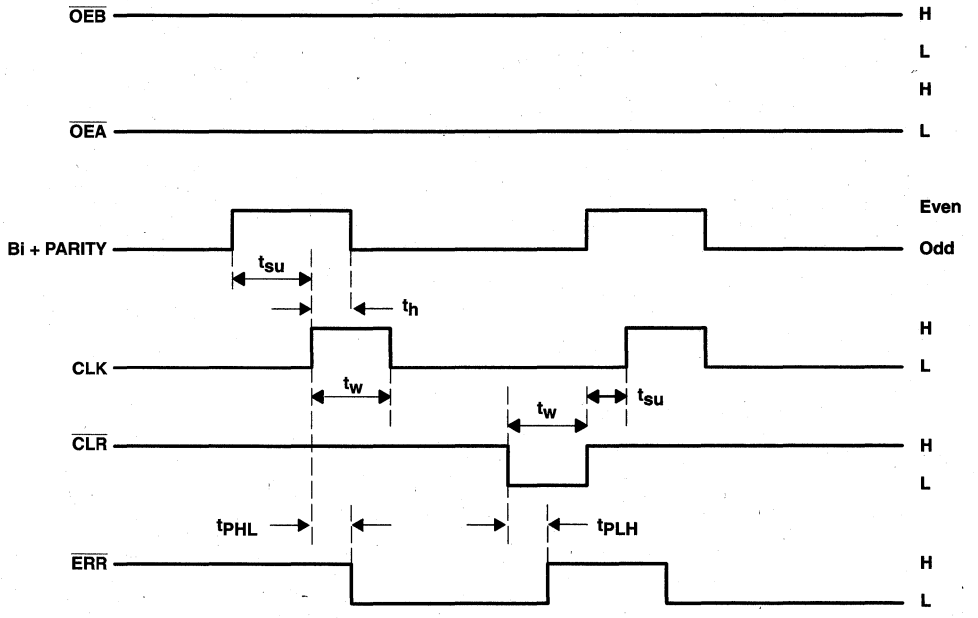
ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}_{n-1}$†		
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† The state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point "P".

PRODUCT PREVIEW

error-flag waveforms



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT833 ..... 96 mA
SN74ABT833 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			SN54ABT833		SN74ABT833		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{OH}	High-level output voltage	$\overline{ERR}$		5.5		5.5	V
I_{OH}	High-level output current	Except $\overline{ERR}$		−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT833		SN74ABT833		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		All outputs except $\overline{ERR}$	2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 24 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_{OH}	V_{CC} = 4.5 V, V_{OH} = 5.5 V		$\overline{ERR}$								µA
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IL}	V_{CC} = 0, V_I = GND		A or B ports			−50		−50		−50	µA
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs								pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports								pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT833		SN74ABT833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high							ns
		CLK low	3		3		3		
		$\overline{CLR}$ low	3		3		3		
t_{su}	Setup time before CLK↑	A port							ns
		$\overline{CLR}$							
t_h	Hold time after CLK↑	A port							ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT833		SN74ABT833		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	A or B								ns
t_{PZL}										
t_{PHZ}	$\overline{OE}$	A or B								ns
t_{PLZ}										
t_{PLH}	A or $\overline{OE}$	PARITY								ns
t_{PHL}										
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$			4.4				5.2	ns
t_{PHL}	CLK				5.7				6.2	

PRODUCT PREVIEW

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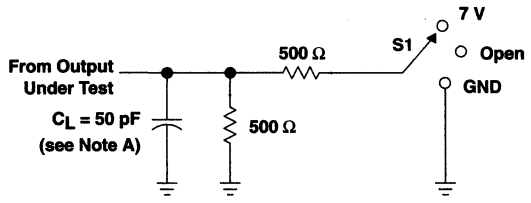
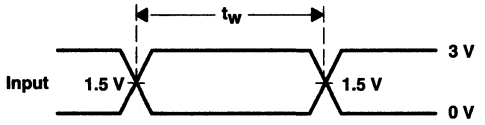
PARAMETER MEASUREMENT INFORMATION



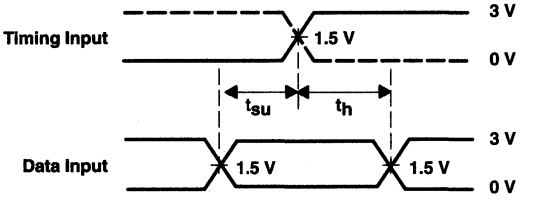
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

$\overline{ERR}$	S1
t_{PHL} (see Note E)	7 V
t_{PLH} (see Note F)	7 V

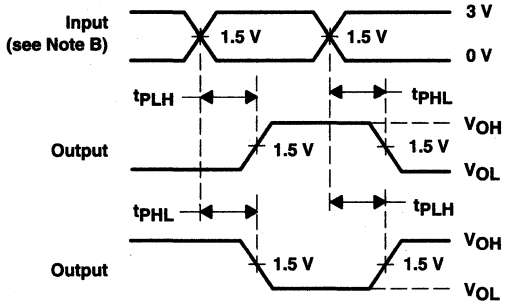
LOAD CIRCUIT FOR OUTPUTS



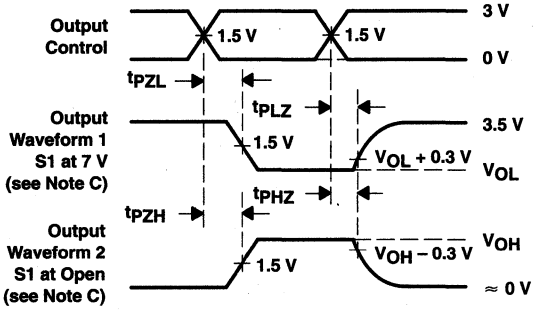
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

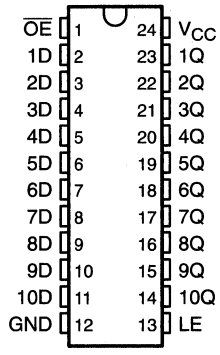
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PHL} is measured at 1.5 V.
F. t_{PLH} is measured at V_{OL} + 0.3 V.

Figure 1. Load Circuit and Voltage Waveforms

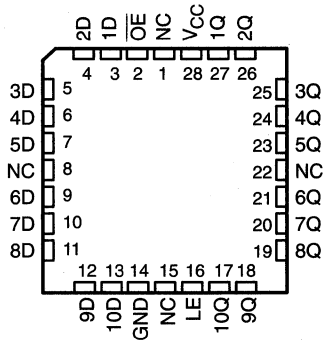
PRODUCT PREVIEW

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT841 . . . JT PACKAGE
SN74ABT841 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT841 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT841 10-bit latch is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT841 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT841 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT841 is characterized for operation from –40°C to 85°C.

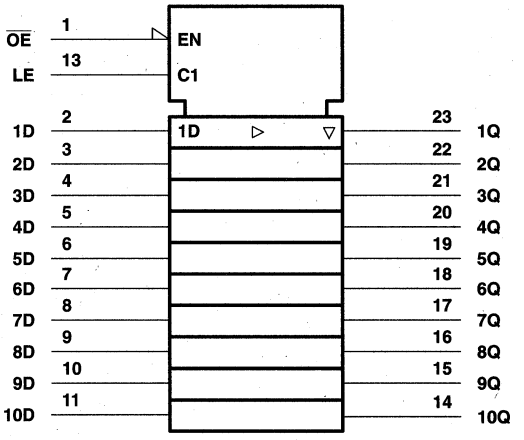
PRODUCT PREVIEW

EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

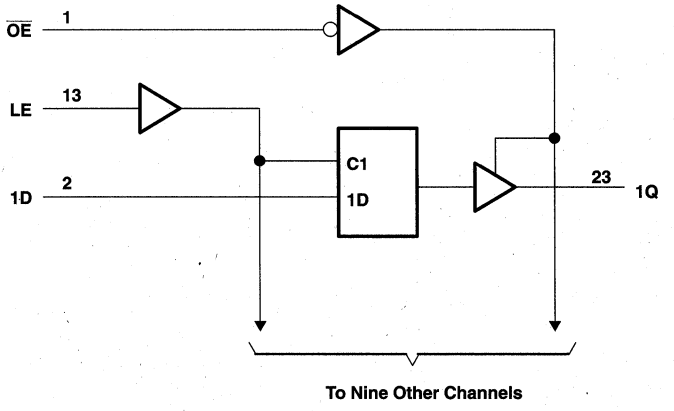
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT841 ..... 96 mA
SN74ABT841 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT841		SN74ABT841		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT841		SN74ABT841		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−140	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	µA
		Control inputs			1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V									pF
C_o	V_O = 2.5 V or 0.5 V									pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT841		SN74ABT841		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high or low		3.8		3.8		3.8		ns
t_{su}	Setup time, data before LE↓	High	2.5		2.5		2.5		ns
		Low	1.5		1.5		1.5		
t_h	Hold time, data after LE↓	High	1.5		1.5		1.5		ns
		Low	1		1		1		

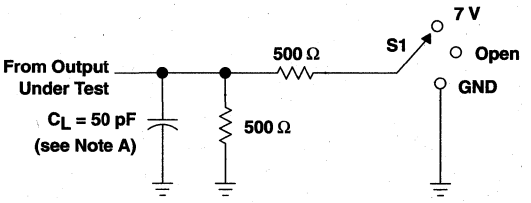
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT841		SN74ABT841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2.1	4.1	5.5	2.1	6.2	2.1	6.2	ns
t_{PHL}			2	4	5.4	2	6.1	2	6.1	
t_{PLH}	LE	Q	2.1	4.1	5.8	2.1	6.2	2.1	6.2	ns
t_{PHL}			2.8	4.6	6.2	2.8	6.7	2.8	6.7	
t_{PZH}	$\overline{OE}$	Q	1	3	4.5	1	5.3	1	5.3	ns
t_{PZL}			2.2	4.1	5.6	2.2	6.3	2.2	6.3	
t_{PHZ}	$\overline{OE}$	Q	2.7	4.7	6.2	2.7	7.1	2.7	7.1	ns
t_{PLZ}			2.8	4.6	6.1	2.8	6.5	2.8	6.5	

PRODUCT PREVIEW

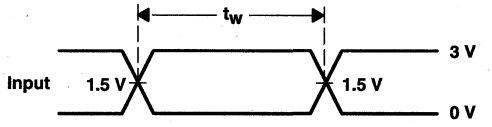
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

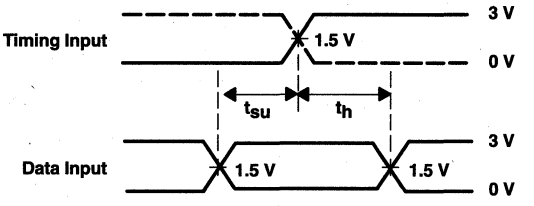


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

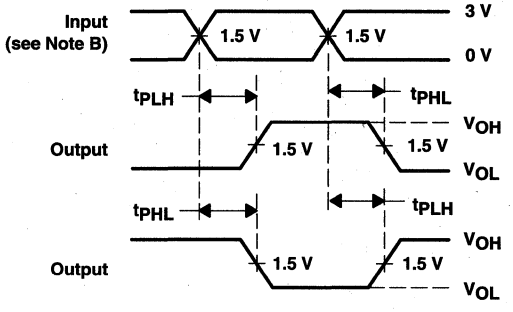
LOAD CIRCUIT FOR OUTPUTS



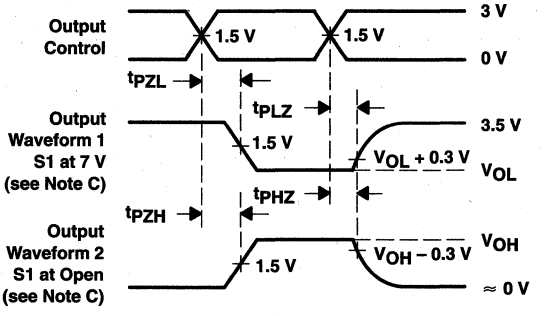
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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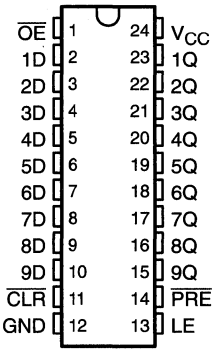
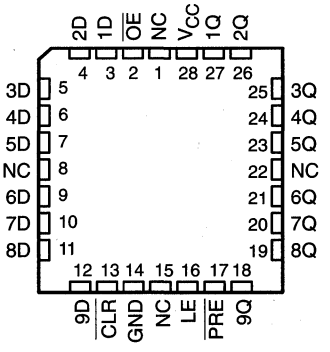
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT843 . . . JT PACKAGE
SN74ABT843 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT843 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ′ABT843 9-bit latch is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT843 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT843 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT843 is characterized for operation from –40°C to 85°C.

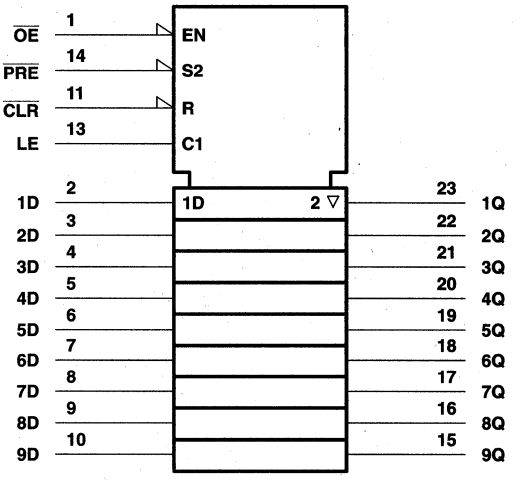
PRODUCT PREVIEW

EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

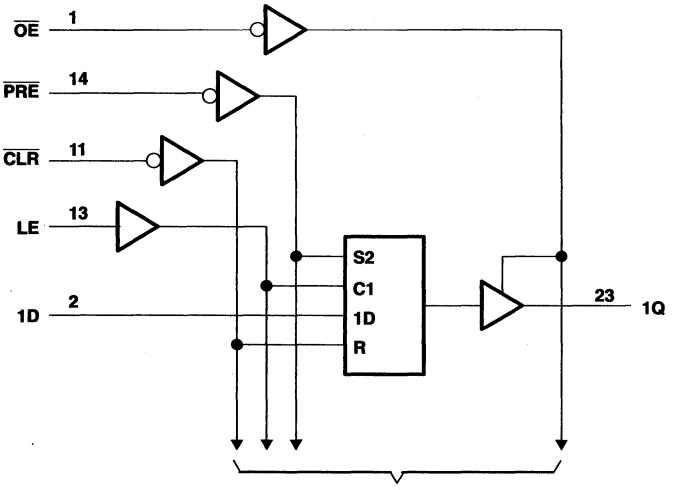
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range , V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT843 ..... 96 mA
SN74ABT843 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

		SN54ABT843		SN74ABT843		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT843		SN74ABT843		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−140	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			4						pF
C_o	V_O = 2.5 V or 0.5 V			7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

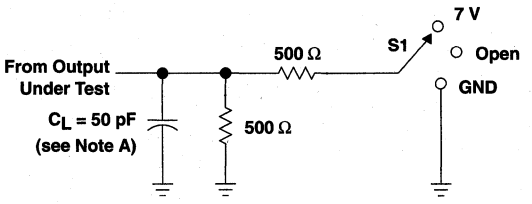
			V_{CC} = 5 V, T_A = 25°C		SN54ABT843		SN74ABT843		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5.5		5.5		5.5		ns
		$\overline{PRE}$ low	4.5		4.5		4.5		
		LE high	3.3		3.3		3.4		
t_{su}	Setup time, data before LE↓	High	2.5		2.5		2.5		ns
		Low	3		3		3		
t_h	Hold time, data after LE↓		0.5		0.5		0.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT843		SN74ABT843		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.6	3.6	5.2	1.6		1.6	6	ns
t_{PHL}			2.2	5	6.3	2.2		2.2	7.2	
t_{PLH}	LE	Q	2	4.1	5.6	2		2	6.5	ns
t_{PHL}			2.8	4.8	6.3	2.8		2.8	6.9	
t_{PLH}	$\overline{PRE}$	Q	2.2	4.7	6.2	2.2		2.2	7.4	ns
t_{PHL}			3	5.2	6.5	3		3	7.2	
t_{PLH}	$\overline{CLR}$	Q	2.5	5	6.3	2.5		2.5	7.1	ns
t_{PHL}			3.1	5.5	6.8	3.1		3.1	8	
t_{PZH}	$\overline{OE}$	Q	1	2.7	4.2	1		1	5.2	ns
t_{PZL}			2	4.2	5.5	2		2	6.5	
t_{PHZ}	$\overline{OE}$	Q	2.9	4.9	6.2	2.9		2.9	6.8	ns
t_{PLZ}			2.2	5	6.3	2.2		2.2	5.7	

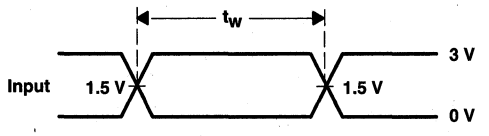
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

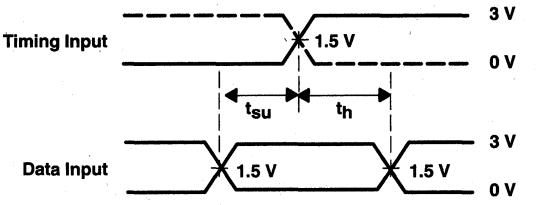


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

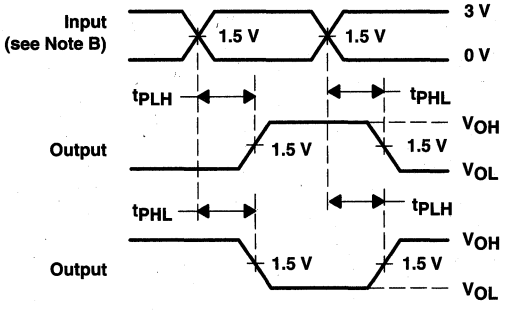
LOAD CIRCUIT FOR OUTPUTS



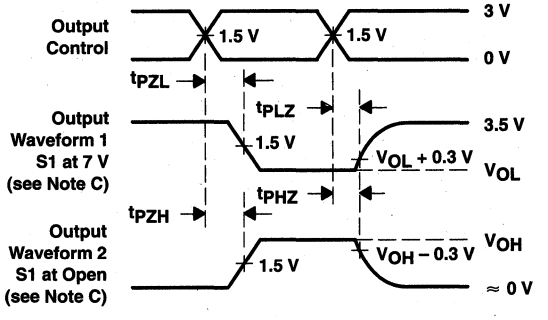
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

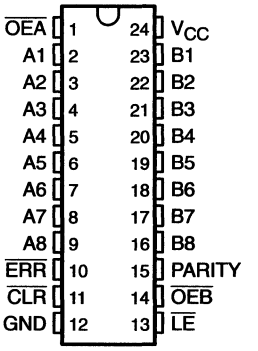
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

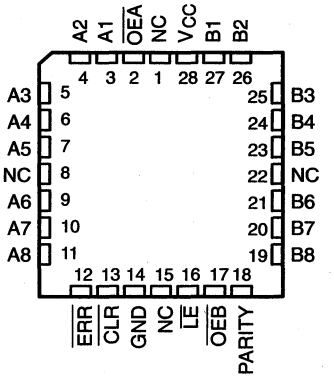
D3786, FEBRUARY 1991 – REVISED OCTOBER 1992

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Parity Error Flag With Parity Generator/Checker**
- **Latch for Storage of the Parity Error Flag**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT853 . . . JT PACKAGE
SN74ABT853 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT853 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT853 8-bit to 9-bit parity transceiver is designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error ($\overline{ERR}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$ and $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT853 provides true data at its outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the $\overline{ERR}$ flag. The parity-error output can be passed, sampled, stored, or cleared from the latch using the latch-enable ($\overline{LE}$) and clear ($\overline{CLR}$) control inputs. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT853 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT853 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT853 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

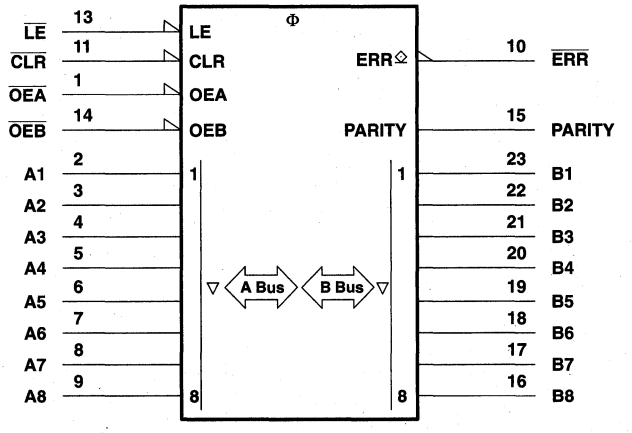
EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS						OUTPUTS AND I/Os				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	LE	Ai Σ OF H	Bi† Σ OF H	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error flag register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H H L	Isolation§ (parity check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume the $\overline{ERR}$ output was previously high.
§ In this mode, the $\overline{ERR}$ output (when clocked) shows inverted parity of the A bus.

logic symbol¶



¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

PRODUCT PREVIEW

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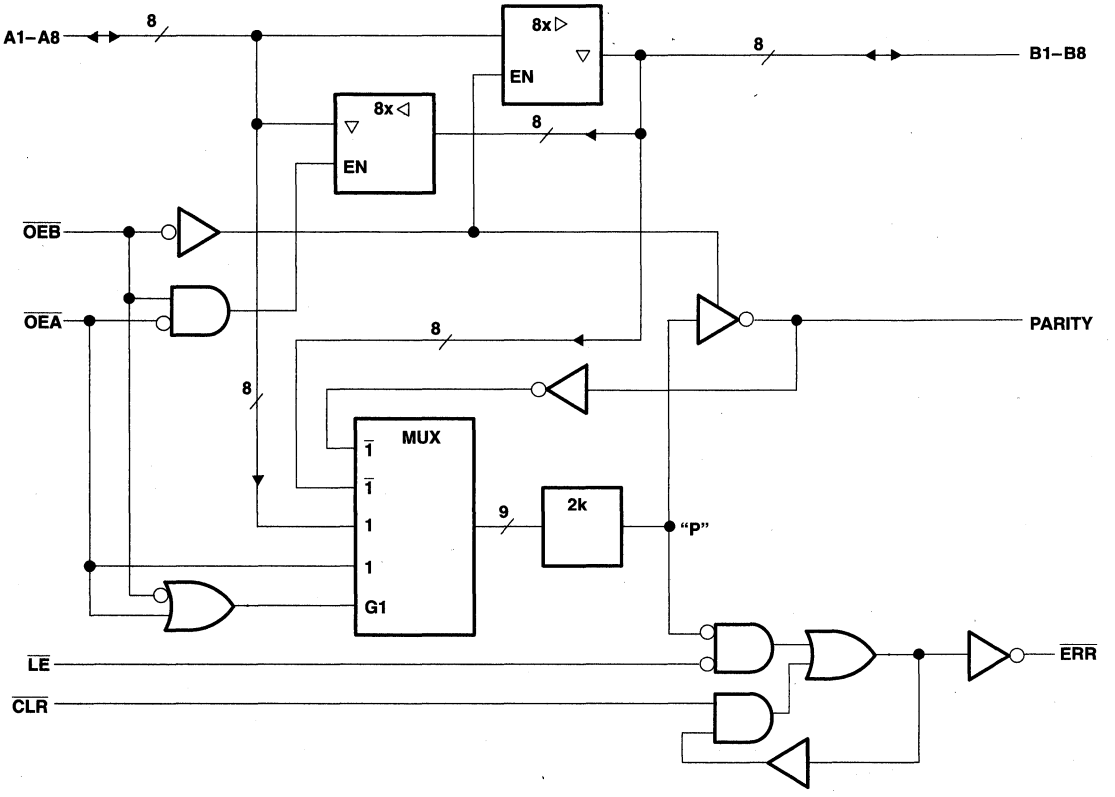
logic diagram (positive logic)



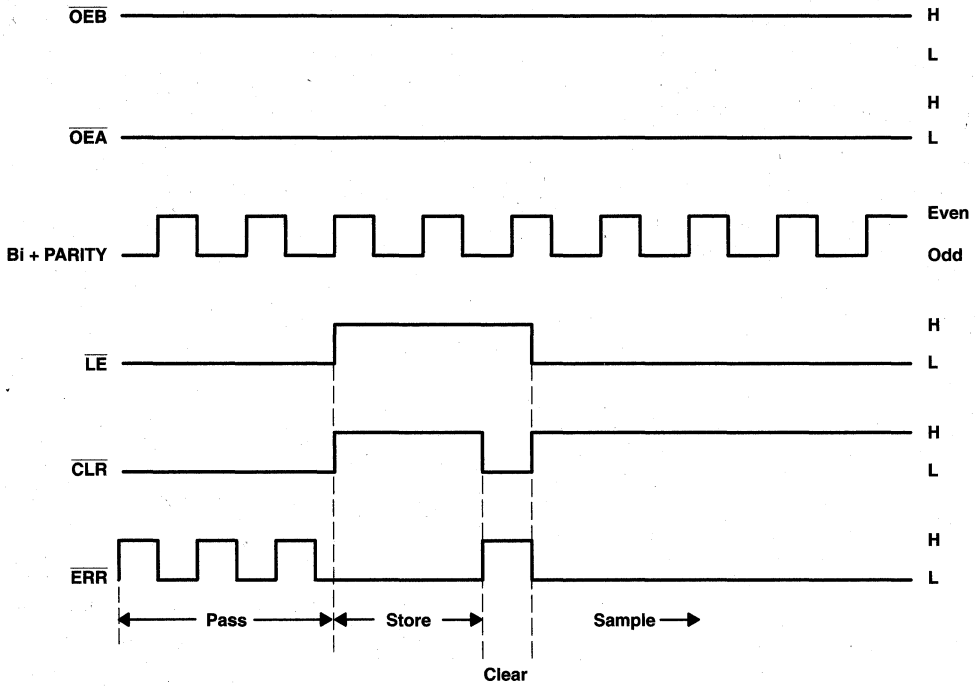
ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	$\overline{LE}$	POINT "P"	$\overline{ERR}_{n-1}$†		
L	L	L	X	L	Pass
		H		H	
H	L	L	X	L	Sample
		X	L	L	
		H	H	H	
L	H	X	X	H	Clear
H	H	X	L	L	Store
			H	H	

† The state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, $\overline{LE}$, or point "P".

PRODUCT PREVIEW

error-flag waveforms



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT853 ..... 96 mA
SN74ABT853 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			SN54ABT853		SN74ABT853		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{OH}	High-level output voltage	$\overline{ERR}$		5.5		5.5	V
I_{OH}	High-level output current	Except $\overline{ERR}$		−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

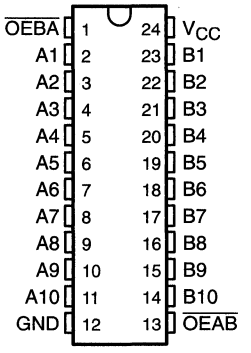
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT853		SN74ABT853		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	All outputs except $\overline{ERR}$	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 24 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V	$\overline{ERR}$								µA
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IL}	V_{CC} = 0,	V_I = GND	A or B ports			−50		−50		−50	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs								pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports								pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

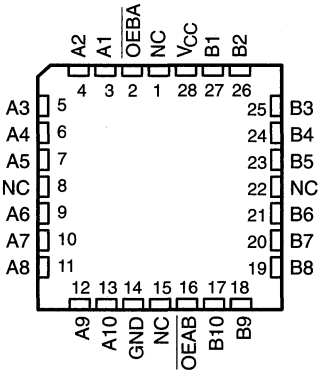
PRODUCT PREVIEW

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT861 . . . JT PACKAGE
SN74ABT861 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT861 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT861 is a 10-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT861 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT861 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT861 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

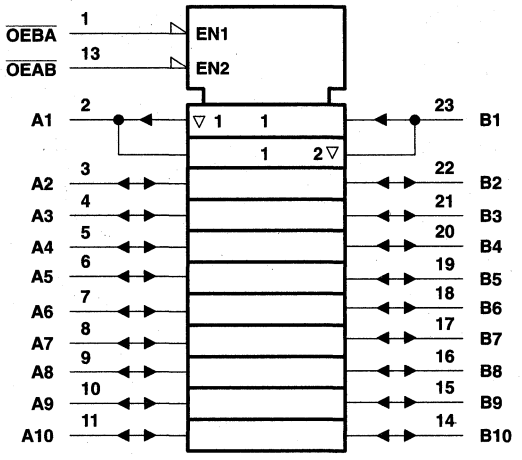
INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
L	H	A data to B bus
H	L	B data to A bus
H	H	Isolation
L	L	Latch A and B (A = B)

PRODUCT PREVIEW

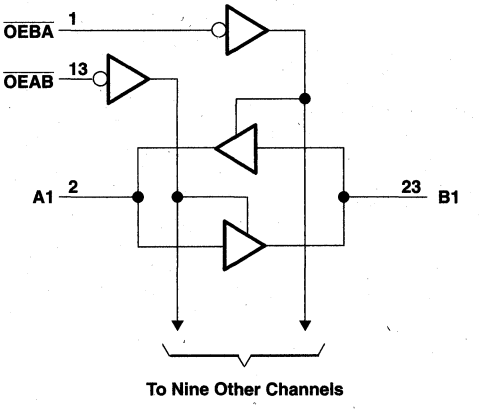
EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT861 ..... 96 mA
SN74ABT861 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT861		SN74ABT861		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT861		SN74ABT861		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

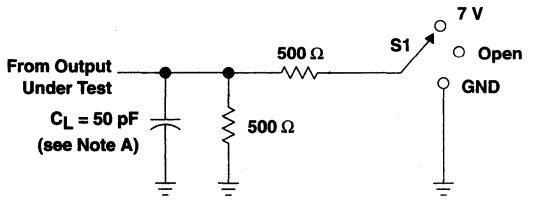
PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT861		SN74ABT861		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.1	3.4	4.9	1.1		1.1	5.2	ns
t_{PHL}			1	3.2	4.4	1		1	4.9	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	1.2	3.5	5	1.2		1.2	5.9	ns
t_{PZL}			2.4	4.6	6	2.4		2.4	6.9	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	3.1	5.3	6.5	3.1		3.1	7.5	ns
t_{PLZ}			3.7	5.3	6.6	3.7		3.7	7.1	

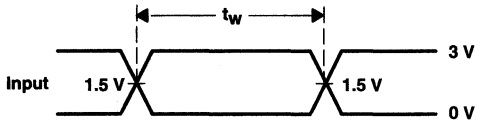
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

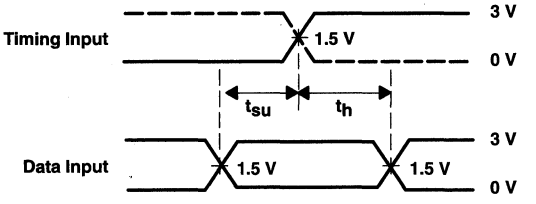


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

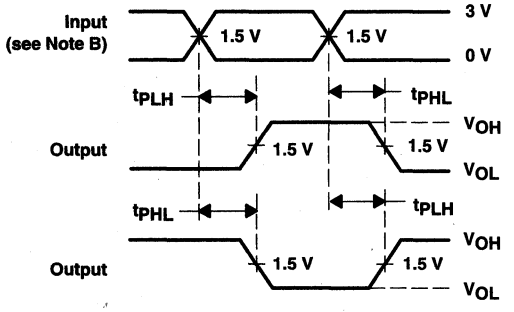
LOAD CIRCUIT FOR OUTPUTS



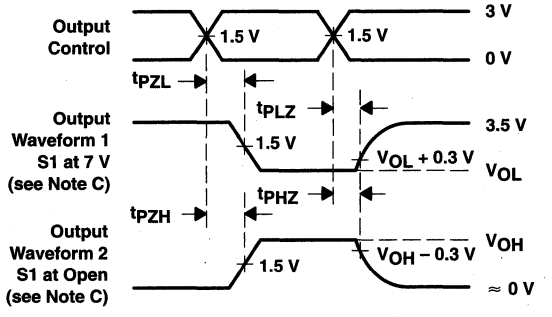
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

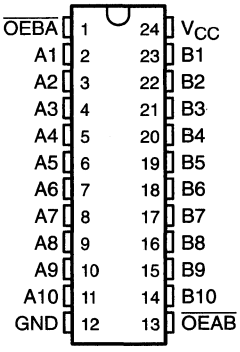
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

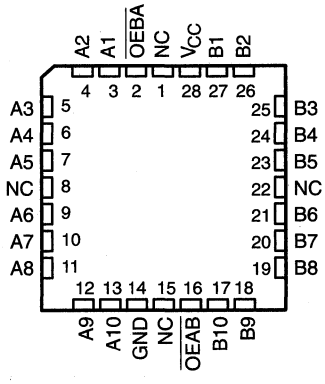
PRODUCT PREVIEW

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT862 . . . JT PACKAGE
SN74ABT862 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT862 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT862 is a 10-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT862 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT862 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT862 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

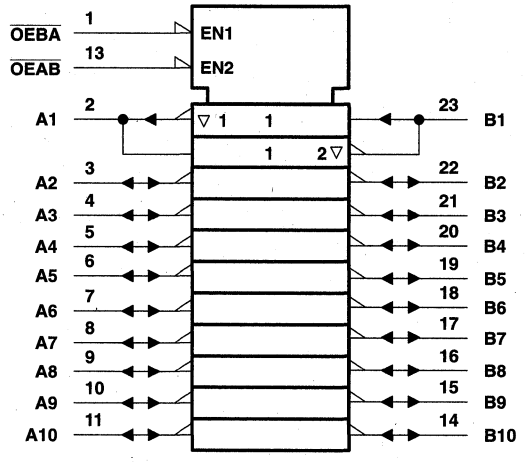
INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
L	H	$\overline{A}$ data to B bus
H	L	$\overline{B}$ data to A bus
H	H	Isolation
L	L	Latch A and B ($A = \overline{B}$)

PRODUCT PREVIEW

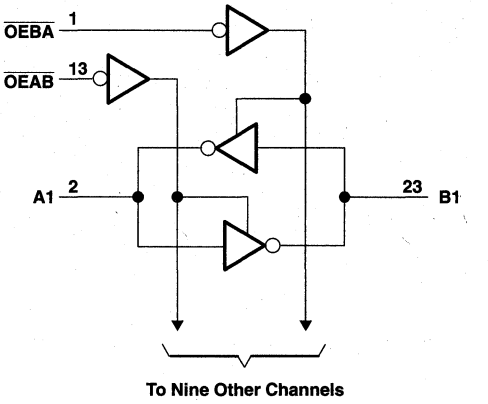
EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT862	96 mA
SN74ABT862	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package	0.7 W
DW package	1 W
NT package	1.3 W
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT862		SN74ABT862		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT862		SN74ABT862		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

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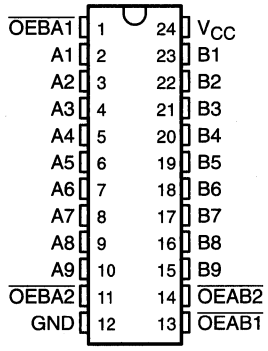
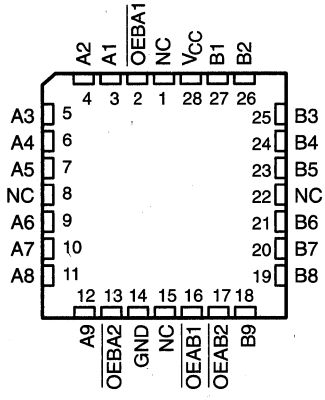
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT863 . . . JT PACKAGE
SN74ABT863 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT863 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ′ABT863 is a 9-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) inputs.

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT863 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT863 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT863 is characterized for operation from –40°C to 85°C.

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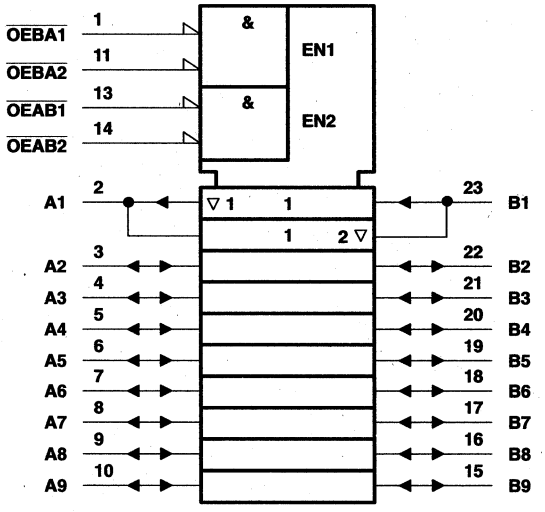
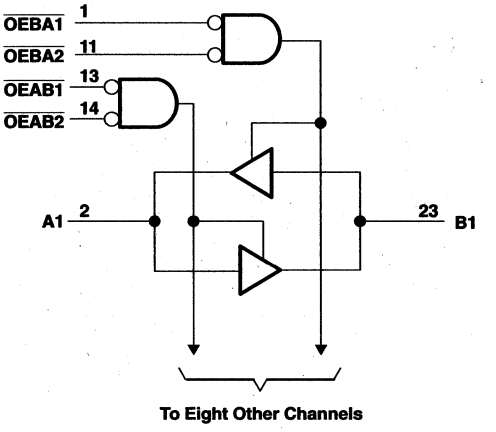
FUNCTION TABLE

INPUTS				OPERATION
$\overline{OEAB1}$	$\overline{OEAB2}$	$\overline{OEBA1}$	$\overline{OEBA2}$	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT863 ..... 96 mA
SN74ABT863 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT863		SN74ABT863		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

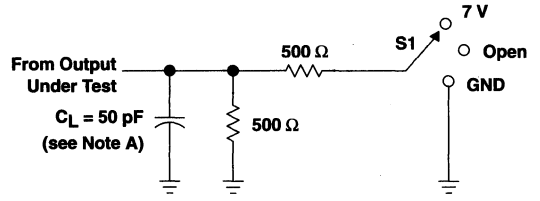
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT863		SN74ABT863		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	30		38		38	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

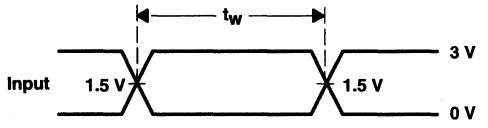
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT863		SN74ABT863		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.6	4.1	1	4.7	1	5.7	ns
t_{PHL}			1	2.3	3.3	1	3.9	1	3.9	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	1	3.2	4.3	1	5.4	1	5.5	ns
t_{PZL}			1	3.3	4.4		5.5	1	5.4	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2.5	4.8	6	2.5	6.8	2.5	6.7	ns
t_{PLZ}			1.5	4.4	5.9	1.5	7.8	1.5	6.9	

PARAMETER MEASUREMENT INFORMATION

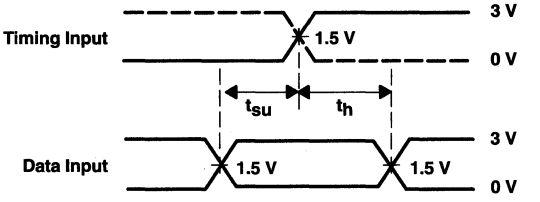


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

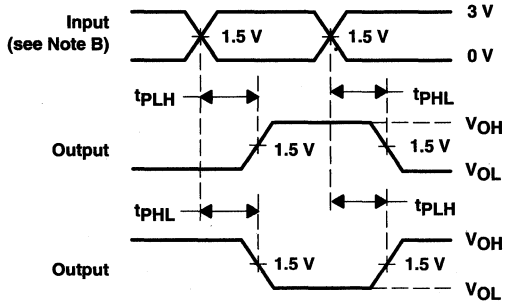
LOAD CIRCUIT FOR OUTPUTS



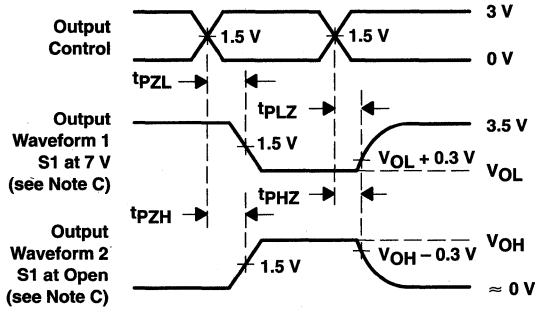
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



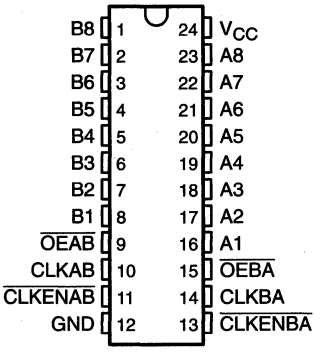
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

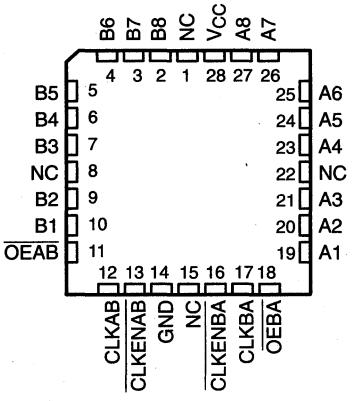
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions**
- **Noninverting Outputs**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT2952 . . . JT PACKAGE
SN74ABT2952 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT2952 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{CLKENAB}$ or $\overline{CLKENBA}$) input is low. Taking the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT2952 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2952 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT2952 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

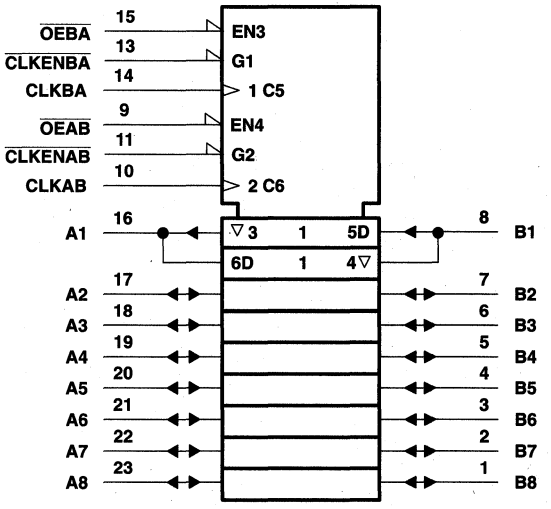
EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	B
H	X	L	X	B_0‡
X	H or L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.
‡ Level of B before the indicated steady-state input conditions were established.

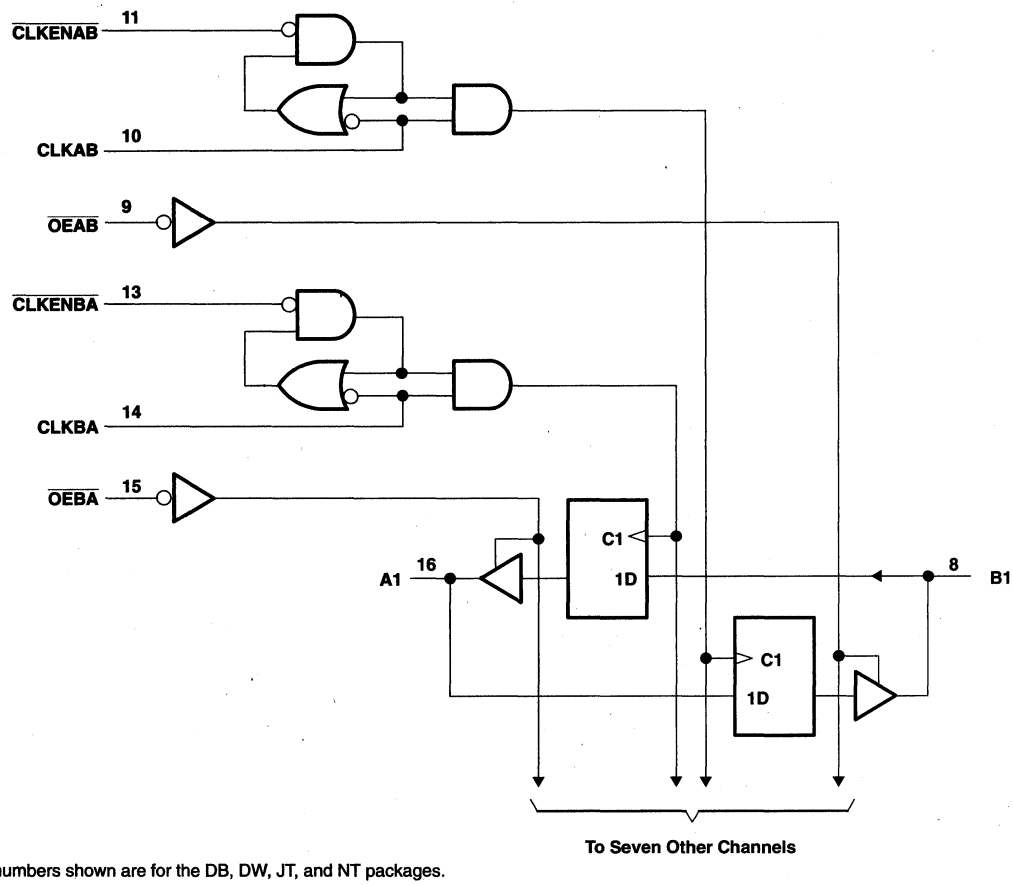
logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT2952	96 mA
SN74ABT2952	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package	0.7 W
DW package	1 W
NT package	1.3 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			SN54ABT2952		SN74ABT2952		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT2952		SN74ABT2952		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	35		35		35	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3.5						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

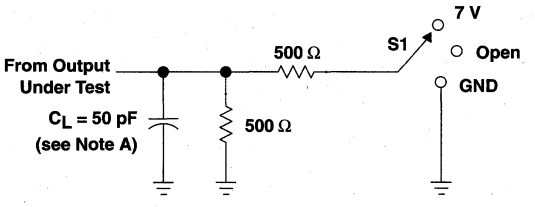
				V_{CC} = 5 V, T_A = 25°C		SN54ABT2952		SN74ABT2952		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	0	150	MHz
t_w	Pulse duration		CLK high	3		3		3		ns
			CLK low	3.5		3.5		3.5		
t_{su}	Setup time before CLK↑	A or B	High	4		4		4		ns
			Low	3		3		3		
		$\overline{CLKEN}$	High	3.5		3.5		3.5		
			Low	2.5		2.5		2.5		
t_h	Hold time after CLK↑	A or B		0		0		0		ns
		$\overline{CLKEN}$		0		0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2952		SN74ABT2952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLKAB or CLKBA	B or A								ns
t_{PHL}										
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B								ns
t_{PZL}										
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B								ns
t_{PLZ}										

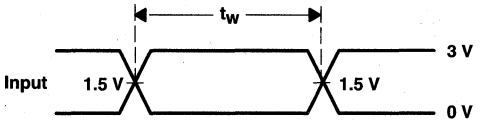
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

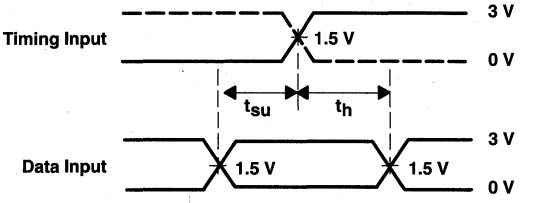


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

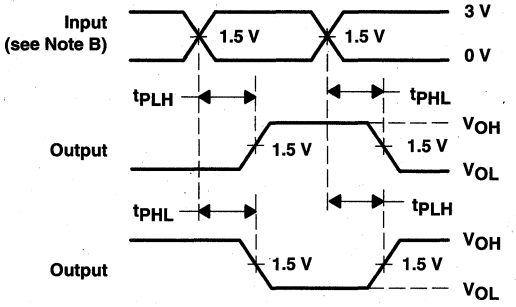
LOAD CIRCUIT FOR OUTPUTS



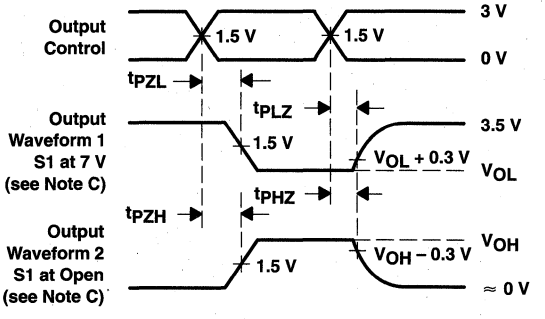
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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- **Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions**
- **Noninverting Outputs**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
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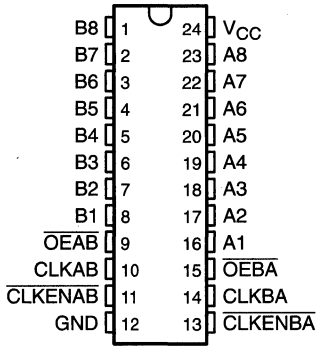
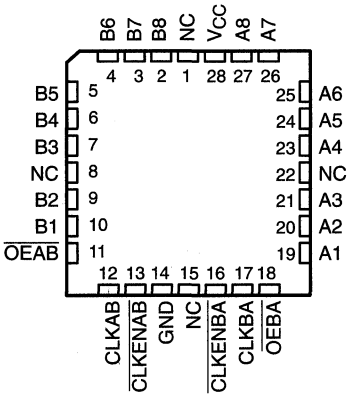
SN54ABT2952A . . . JT PACKAGE
SN74ABT2952A . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT2952A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT2952A consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{CLKENAB}$ or $\overline{CLKENBA}$) input is low. Taking the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT2952A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2952A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT2952A is characterized for operation from −40°C to 85°C.

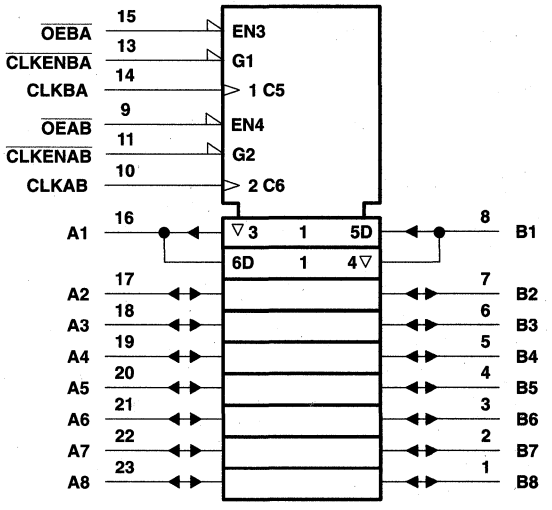
EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	B
H	X	L	X	B_0‡
X	H or L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

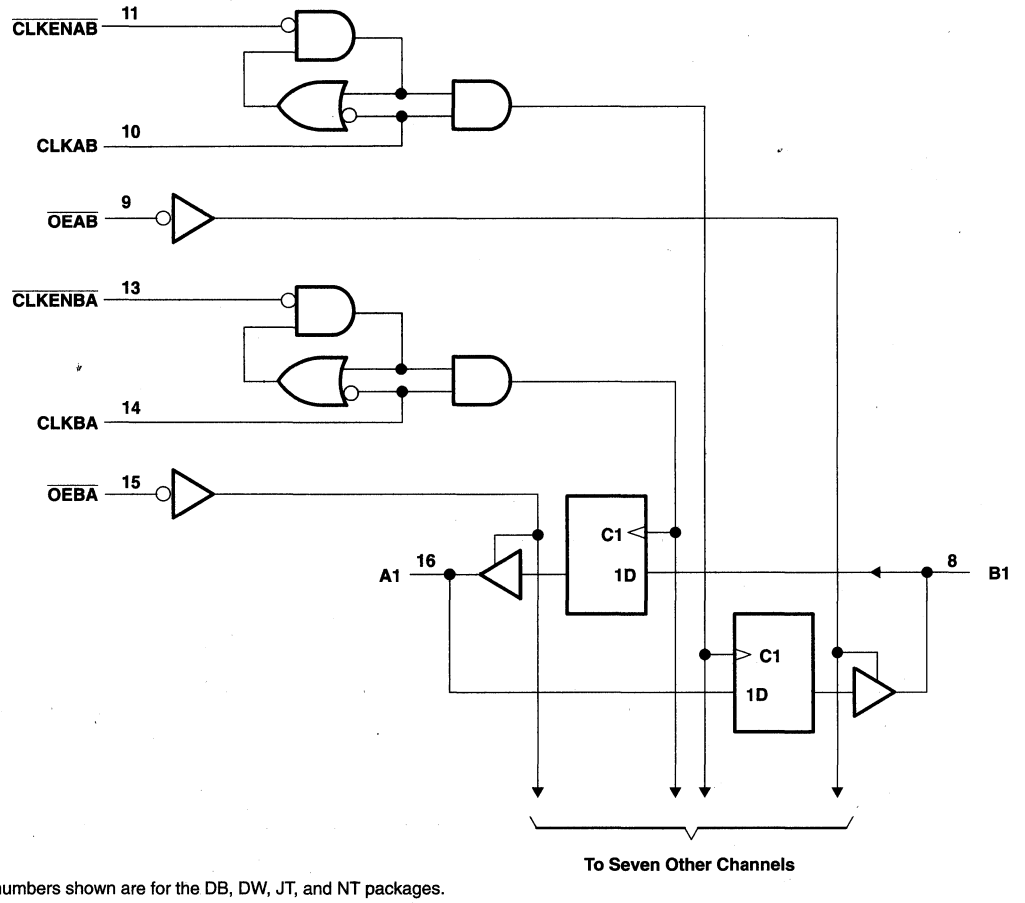
† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.
‡ Level of B before the indicated steady-state input conditions were established.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT2952A ..... 96 mA
SN74ABT2952A ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT2952A		SN74ABT2952A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT2952A		SN74ABT2952A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	35		35		35	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3.5						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

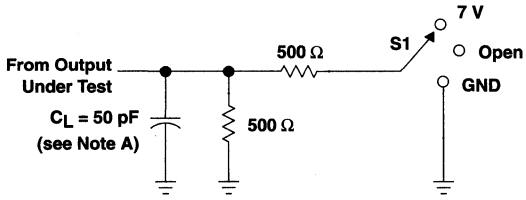
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				V_{CC} = 5 V, T_A = 25°C		SN54ABT2952A		SN74ABT2952A		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	0	150	MHz
t_w	Pulse duration		CLK high or low	3.3		3.3		3.3		ns
t_{su}	Setup time before CLK↑	A or B	High or low	2.5		2.5		2.5		ns
		$\overline{CLKEN}$	High or low	3		3		3		
t_h	Hold time after CLK↑	A or B		1.5		1.5		1.5		ns
		$\overline{CLKEN}$		2		2		2		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

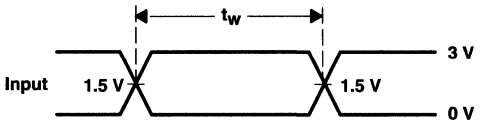
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2952A		SN74ABT2952A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLKAB or CLKBA	B or A	2	3.3	5.2	2	6.3	2	5.9	ns
t_{PHL}			2.5	4	6.1	2.5	6.8	2.5	6.3	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.5	3.2	4.7	1.5	5.7	1.5	5.6	ns
t_{PZL}			2	3.7	5.7	2	6.7	2	6.6	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.5	3.5	5.1	1.5	6.5	1.5	6.4	ns
t_{PLZ}			1.5	3.4	5.9	1.5	6.7	1.5	6.2	

PARAMETER MEASUREMENT INFORMATION

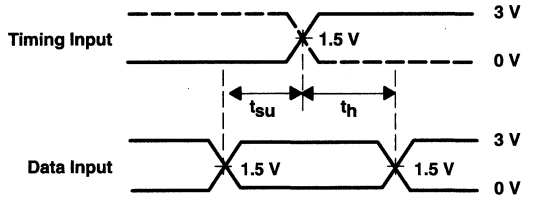


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

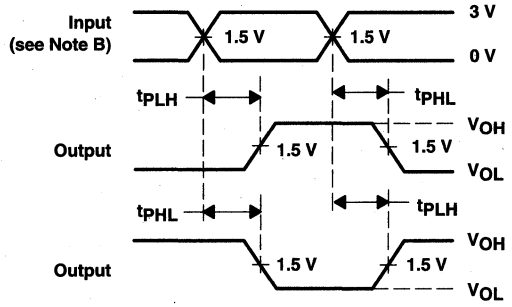
LOAD CIRCUIT FOR OUTPUTS



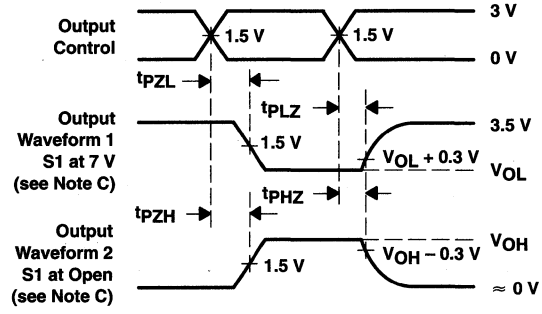
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

ABT Widebus™

Features

- Enhanced ac performance over ABT octals
- JEDEC standard 48-/56-pin SSOP package
- New EIAJ standard Shrink Widebus™ TSSOP package
- Flow-through package pinout organizes all inputs on one side and all outputs on the other side
- Distributed V_{CC} and GND pinouts
- Universal bus transceiver (UBT™) architectures
- Hot-card insertion and power-up 3-state circuitry
- TI has established an alternate source

Benefits

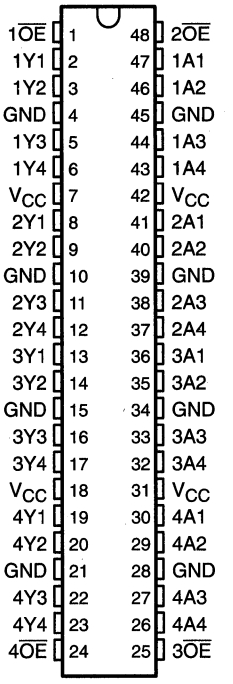
- Improved propagation delay versus number of outputs switching. Superior pin-to-pin output skew; 15–20% faster speed
- 16, 18, or 20 bits of logic in the same space as that of a typical octal
- 30% board space improvement over SSOP Widebus™ package; meets 1.1-mm height requirements for memory card and other thin applications
- Facilitates easy board layout; pin compatible with popular AC/ACT Widebus™ functions
- Minimized mutual coupling and 2:1 I/O-to-GND rates result in < 0.8-V simultaneous switching noise typically
- Advanced integration, as one UBT™ can replace nearly all common bus-interface logic
- Device protection for end-equipment-specific applications such as telecom
- Standardization that comes from a common product approach

The following table lists ABT Widebus™ devices currently being evaluated for market introduction. Customers interested in learning more about TI's plans for these devices should contact the Advanced System Logic Marketing hotline at (214) 997-5202.

DEVICE	PIN COUNT	DESCRIPTION
'ABT16544	56	16-Bit Registered Transceiver
'ABT16620	48	16-Bit Transceiver
'ABT16861	56	20-Bit Transceiver
'ABT16953	56	16-Bit Registered Transceiver

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16240 . . . WD PACKAGE
SN74ABT16240 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16240 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16240 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

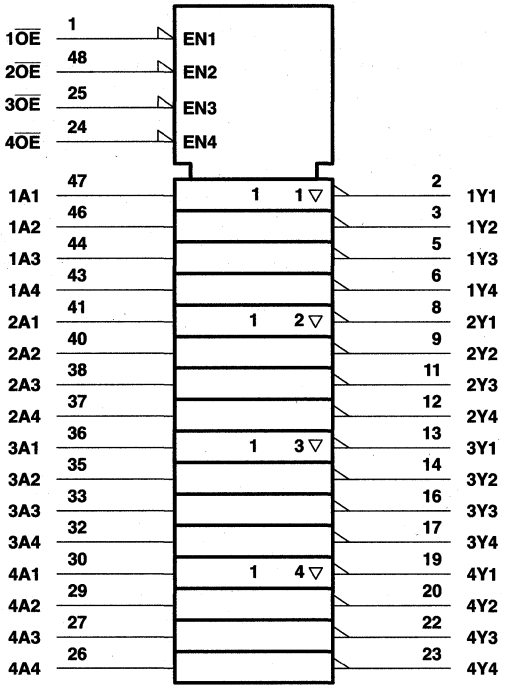
The SN54ABT16240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

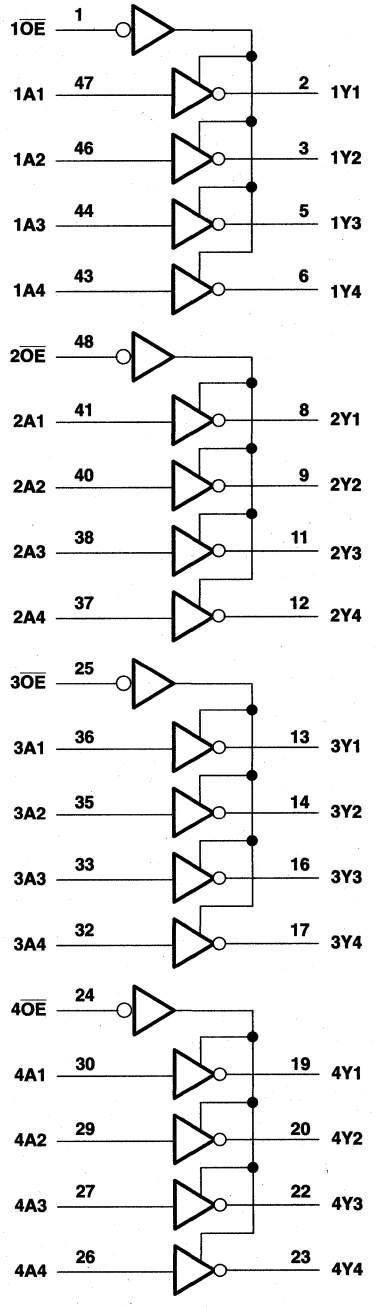
Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16240 ..... 96 mA
SN74ABT16240 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16240		SN74ABT16240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

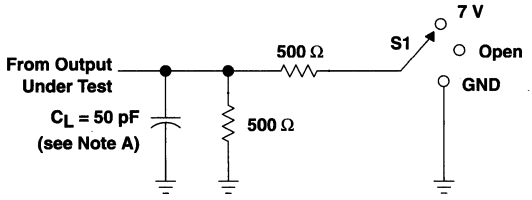
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16240		SN74ABT16240		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				7						pF
C_o	V_O = 2.5 V or 0.5 V				7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

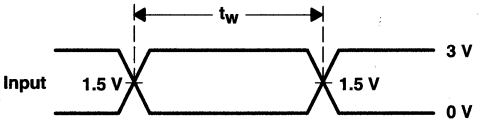
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16240		SN74ABT16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.7	3.8	0.8	4.8	1	4.7	ns
t_{PHL}			1.1	3.1	4.3	1.1	4.9	1.1	4.8	
t_{PZH}	$\overline{OE}$	Y	1.3	3.3	4.3	1.3	5.4	1.3	5.3	ns
t_{PZL}			1.4	3.4	6.2	1.4	7.2	1.4	7.1	
t_{PHZ}	$\overline{OE}$	Y	1.6	3.6	4.8	1.6	7.2	1.6	6.1	ns
t_{PLZ}			1.4	3	5.1	1.4	5.7	1.4	5.6	

PARAMETER MEASUREMENT INFORMATION

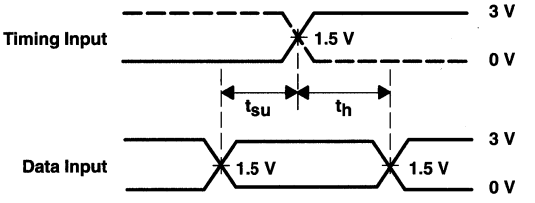


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

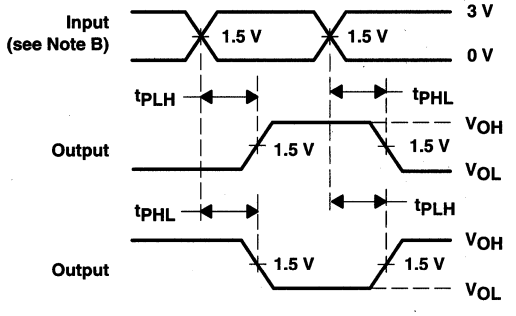
LOAD CIRCUIT FOR OUTPUTS



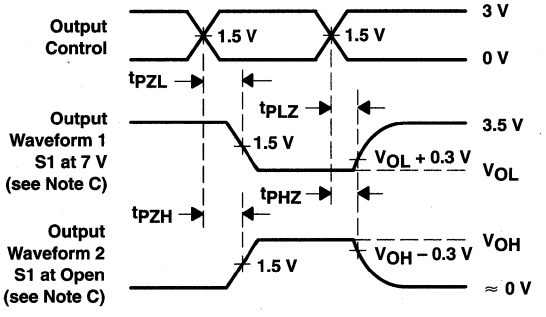
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



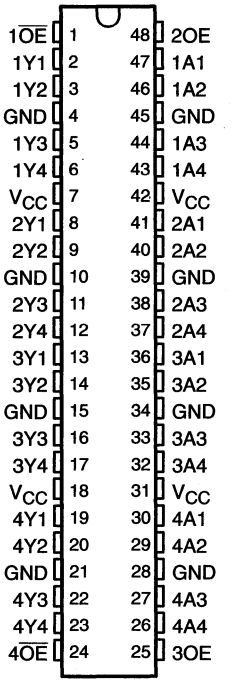
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16241 . . . WD PACKAGE
SN74ABT16241 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16241 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and complementary output-enable (OE and $\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16241 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16241 is characterized for operation from –40°C to 85°C.

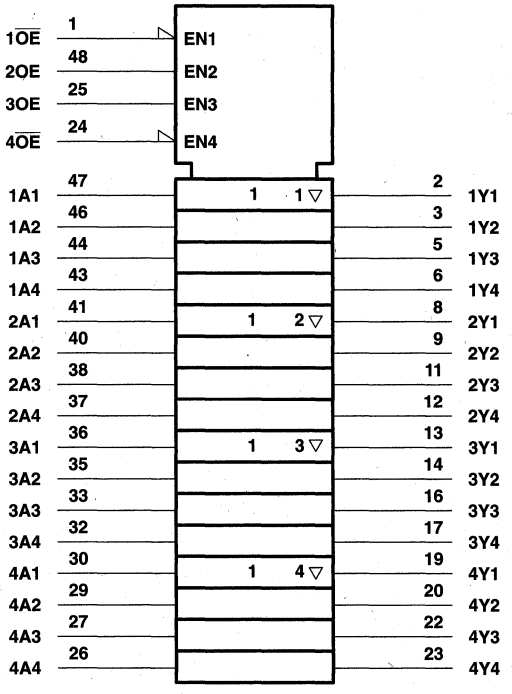
Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

FUNCTION TABLES

INPUTS		OUTPUTS
$1\overline{OE}$, $4\overline{OE}$	1A, 4A	1Y, 4Y
L	H	H
L	L	L
H	X	Z

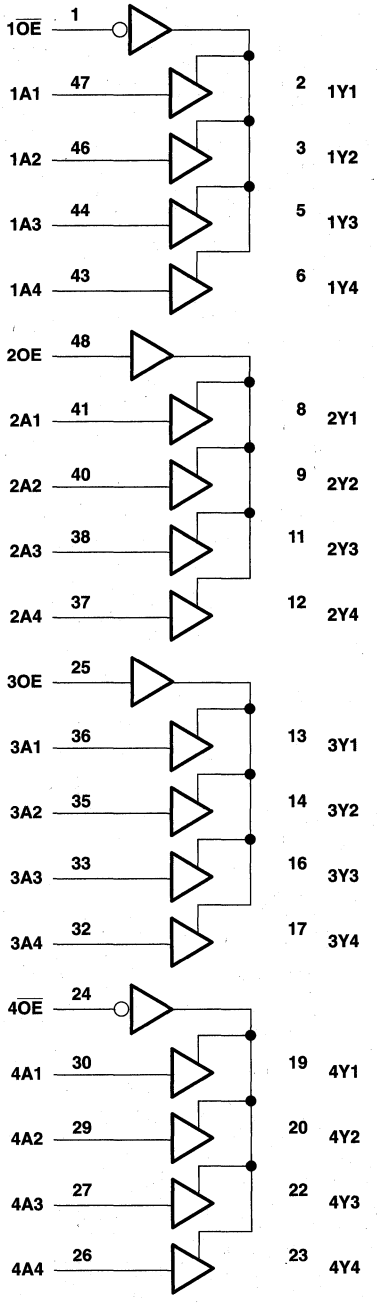
INPUTS		OUTPUTS
2OE, 3OE	2A, 3A	2Y, 3Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16241 ..... 96 mA
SN74ABT16241 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16241		SN74ABT16241		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

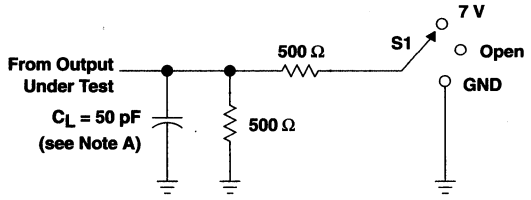
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16241		SN74ABT16241		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				7						pF
C_o	V_O = 2.5 V or 0.5 V				7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

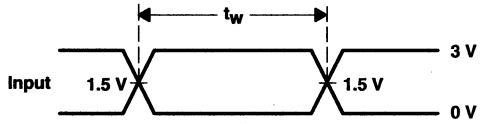
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16241		SN74ABT16241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.7	3.4	0.9	3.8	1	3.7	ns
t_{PHL}			1	2.7	3.9	0.9	4.6	1	4.5	
t_{PZH}	OE or $\overline{OE}$	Y	1.2	3.3	4.2	1.2	5.1	1.2	5	ns
t_{PZL}			1.3	3.4	5.9	1.3	7	1.3	6.9	
t_{PHZ}	OE or $\overline{OE}$	Y	1.5	4.1	5	1.5	7	1.5	6.2	ns
t_{PLZ}			1.7	3.6	5.1	1.7	5.7	1.7	5.6	

PARAMETER MEASUREMENT INFORMATION

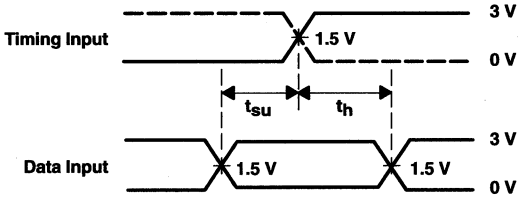


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

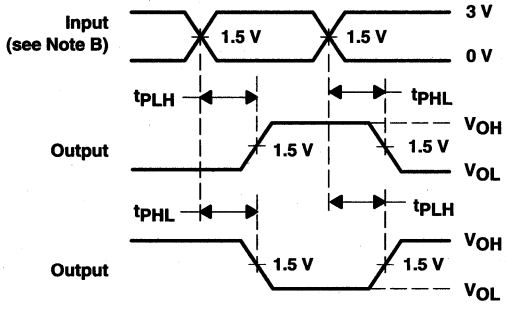
LOAD CIRCUIT FOR OUTPUTS



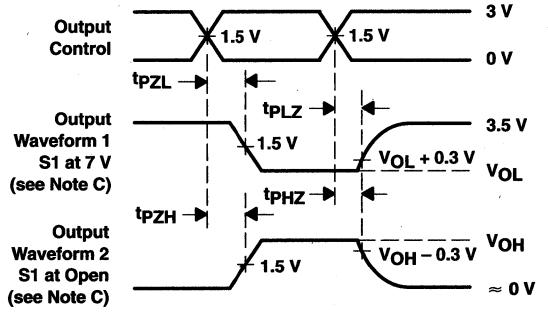
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



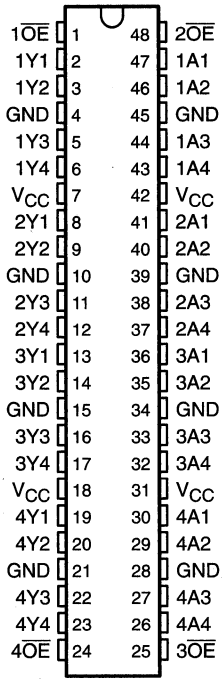
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16244 . . . WD PACKAGE
SN74ABT16244A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The SN54ABT16244 and SN74ABT16244A are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16244A is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

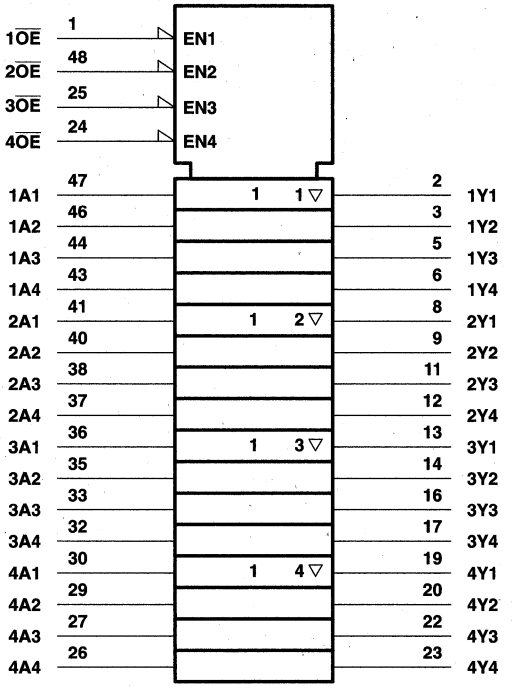
The SN54ABT16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16244A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

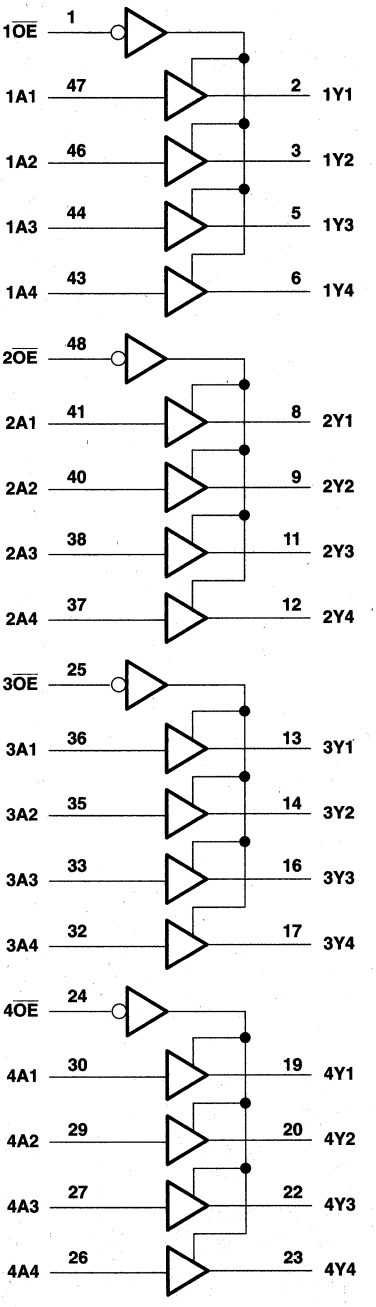
Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16244 ..... 96 mA
SN74ABT16244A ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16244		SN74ABT16244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

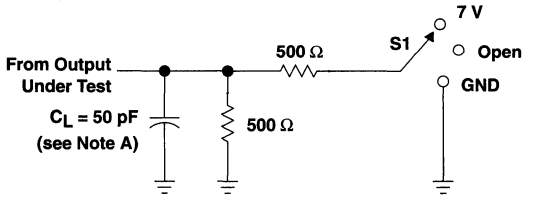
PARAMETER	TEST CONDITIONS			T_A = 25°C†			SN54ABT16244		SN74ABT16244A		UNIT
				MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2§					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55§				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				10¶		10		10¶	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–10¶		–10		–10¶	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100		±100		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O#	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			3		2		3	mA
			Outputs low			32		32		32	
			Outputs disabled			3		2		3	
ΔI_{CC}‖	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			0.05		1.5		0.05	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				0.05		1.5		0.05	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† Characteristics for TA = 25°C apply to the SN74ABT16244A only.
‡ All typical values are at V_{CC} = 5 V.
§ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
¶ This data sheet limit may vary among suppliers.
# Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

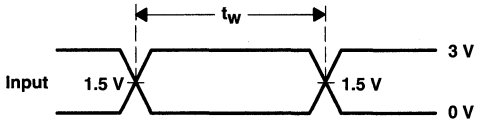
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C†			SN54ABT16244		SN74ABT16244A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.3	3.2	0.7	3.7	1	3.5	ns
t_{PHL}			1	2.6	3.7	0.5	4.3	1	4.1	
t_{PZH}	$\overline{OE}$	Y	1	3	3.8	0.7	5	1	4.8	ns
t_{PZL}			1	3.2	4	0.9	5	1	4.8	
t_{PHZ}	$\overline{OE}$	Y	1	3.6	4.4	1	5	1	4.8	ns
t_{PLZ}			1	2.9	3.7	1	4.3	1	4.1	

PARAMETER MEASUREMENT INFORMATION

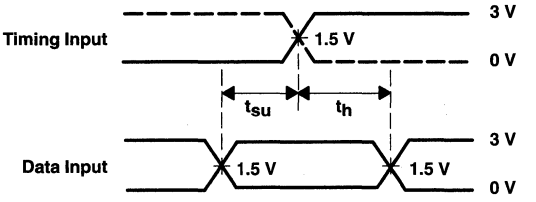


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

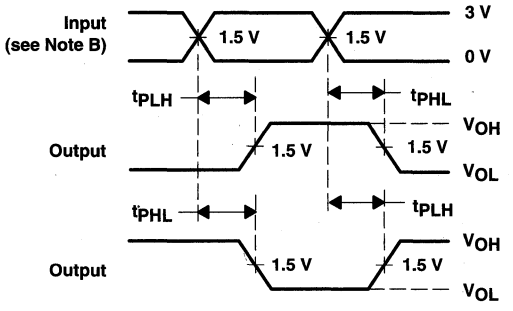
LOAD CIRCUIT FOR OUTPUTS



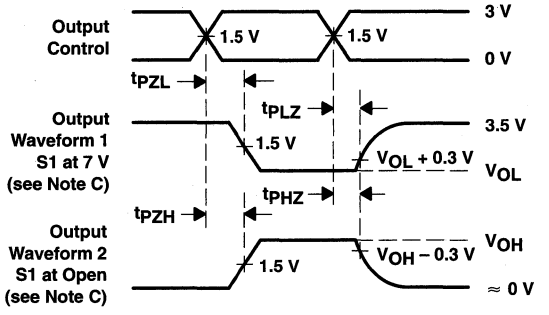
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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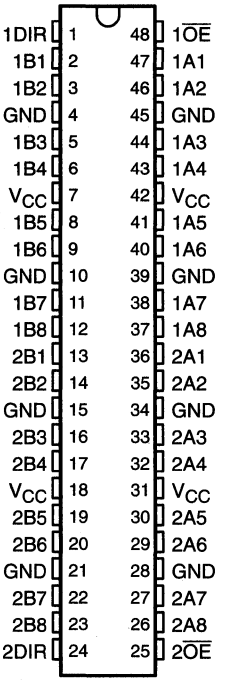
SN54ABT16245 . . . WD PACKAGE
SN74ABT16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT16245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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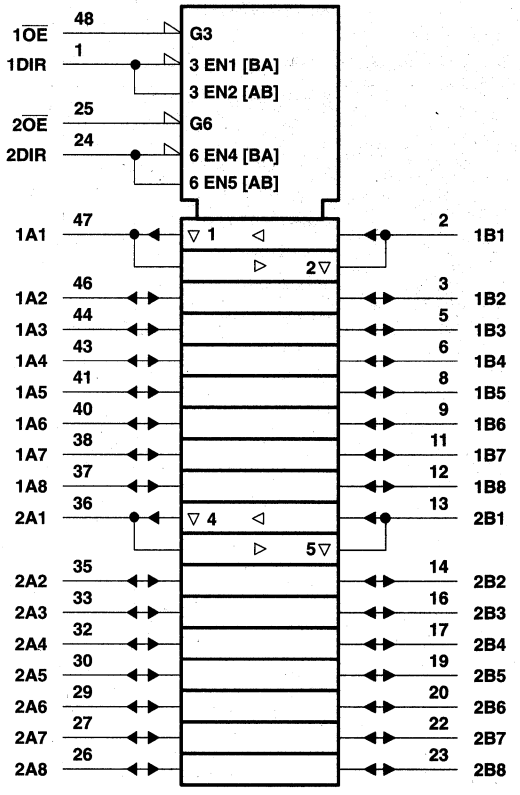
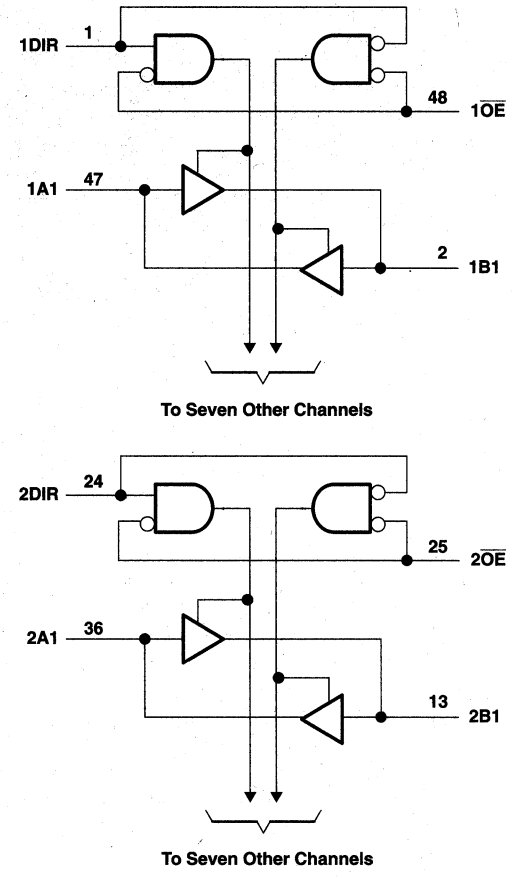
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16245 ..... 96 mA
SN74ABT16245 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16245		SN74ABT16245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

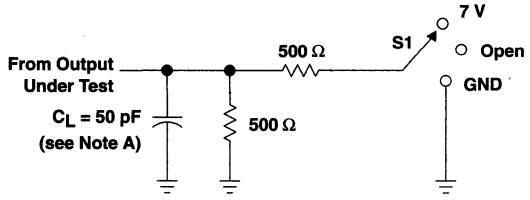
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16245		SN74ABT16245		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				10¶		10		10¶	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−10¶		−10		−10¶	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O#	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}‖	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		8.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ This data sheet limit may vary among suppliers.
# Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

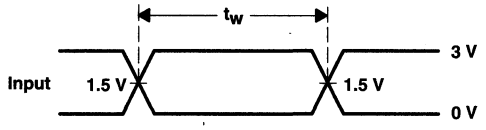
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16245		SN74ABT16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.2	3.4	0.5	4	1	3.9	ns
t_{PHL}			1	2.1	3.8	0.5	4.6	1	4.5	
t_{PZH}	OE	B or A	1	3.1	4.4	0.8	5.5	1	5.4	ns
t_{PZL}			1	3	6.1	0.9	7.3	1	7.2	
t_{PHZ}	OE	B or A	1.3	3.5	4.7	1.3	6.3	1.3	5.5	ns
t_{PLZ}			1.4	3.2	4.7	1.4	5.3	1.4	5.2	

PARAMETER MEASUREMENT INFORMATION

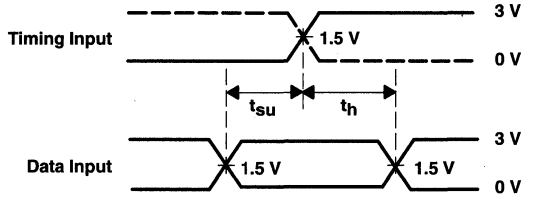


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

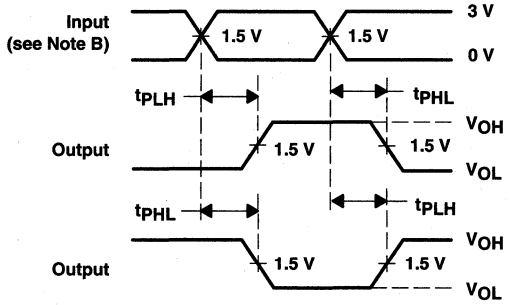
LOAD CIRCUIT FOR OUTPUTS



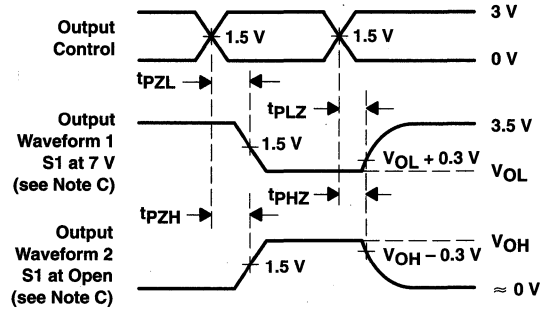
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



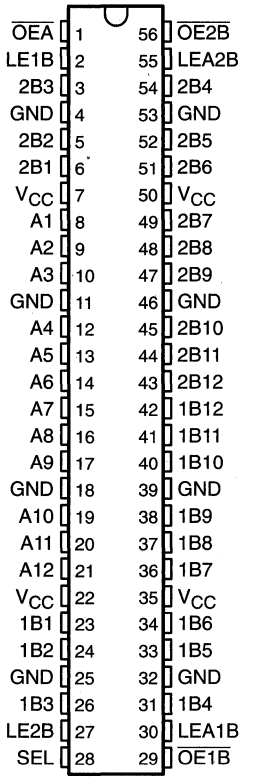
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16260 . . . WD PACKAGE
SN74ABT16260 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A to B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16260 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16260 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16260 is characterized for operation from –40°C to 85°C.

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

Function Tables

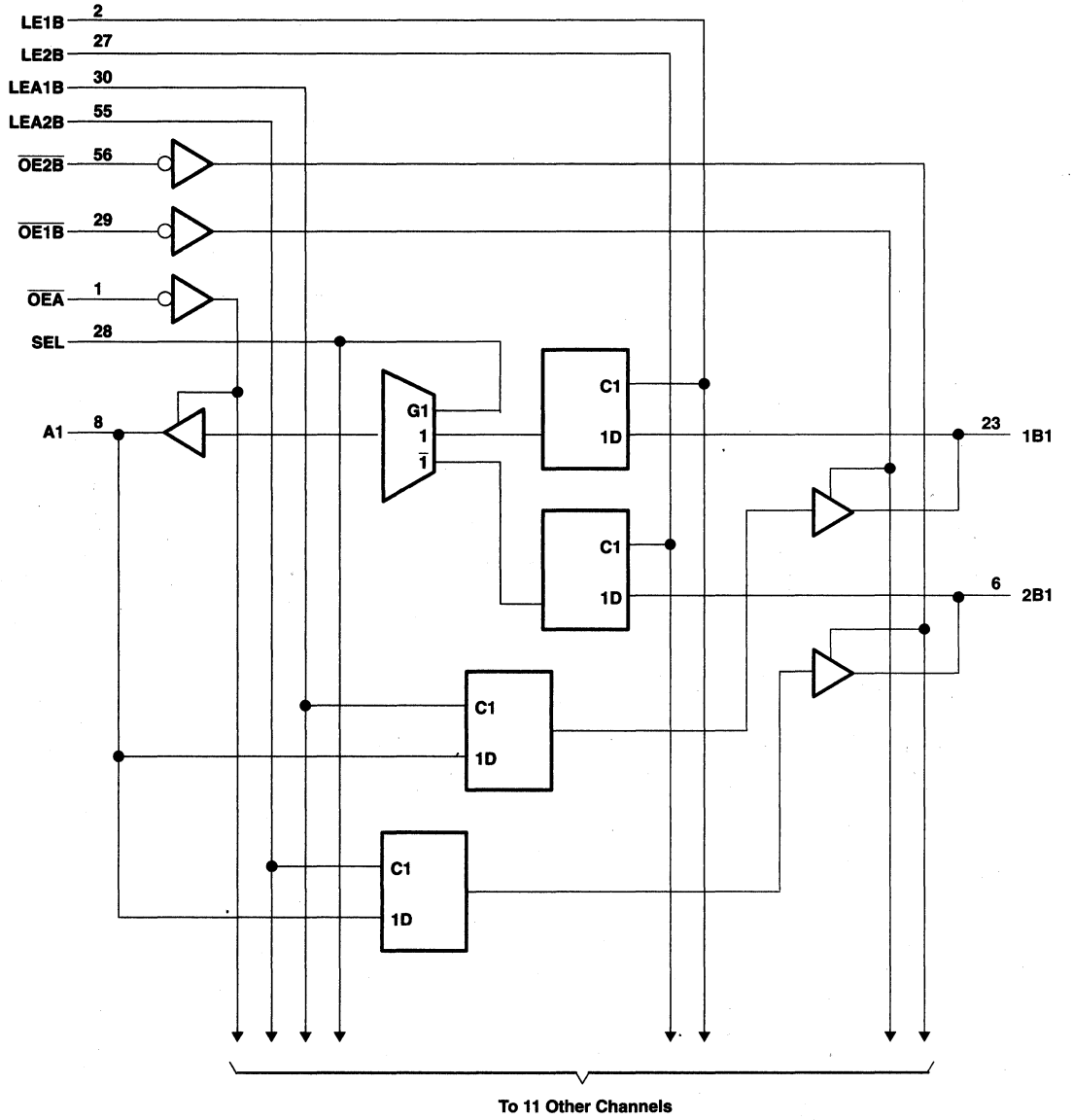
B TO A ($\overline{OEB}$ = H)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A_0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A_0
X	X	X	X	X	H	Z

A TO B ($\overline{OEA}$ = H)

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	$2B_0$
L	H	L	L	L	L	$2B_0$
H	L	H	L	L	$1B_0$	H
L	L	H	L	L	$1B_0$	L
X	L	L	L	L	$1B_0$	$2B_0$
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16260 ..... 96 mA
SN74ABT16260 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			SN54ABT16260		SN74ABT16260		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16260		SN74ABT16260		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Control inputs			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
$I_{I(hold)}$	V_{CC} = 4.5 V, V_I = 0.8 V	A or B ports						100		µA
	V_{CC} = 4.5 V, V_I = 2 V							−100		
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−225	−50	−225	−50	−225	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			1.5		1.5		1.5	mA
		Outputs low			63		63		63	
		Outputs disabled			1		1		1	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_{io}	V_O = 2.5 V or 0.5 V			11.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

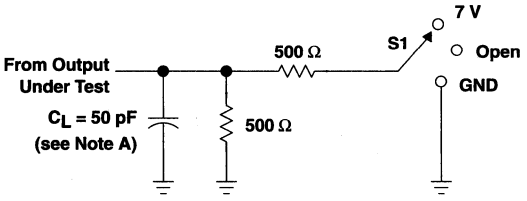
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V_{CC} = 5 V, T_A = 25°C		SN54ABT16260		SN74ABT16260		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1.5		1.5		1.5		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		1		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

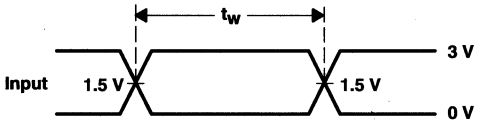
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16260		SN74ABT16260		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	3.1	4.8	1	5.9	1	5.6	ns
t_{PHL}			1	3.4	5	1	6.3	1	5.9	
t_{PLH}	$\overline{LE}$	A or B	1	3.2	4.9	1.1	6.6	1.1	5.8	ns
t_{PHL}			1.1	3.3	4.9	1.1	5.9	1.1	5.3	
t_{PLH}	SEL (B1)	A	1.3	3.2	4.6	1.3	5.4	1.3	5.3	ns
	SEL (B2)		1.1	3.4	4.9	1.1	6.3	1.1	6	
t_{PHL}	SEL (B1)		1.5	3.1	4.4	1.5	4.7	1.5	4.4	
	SEL (B2)		1.6	3.6	5.1	1.6	6.2	1.6	5.9	
t_{PZH}	$\overline{OE}$	A or B	1	3.3	4.7	1	6.4	1	5.7	ns
t_{PZL}			1.6	3.8	5.1	1.6	6.1	1.6	5.8	
t_{PHZ}	$\overline{OE}$	A or B	2.2	4.1	5.4	2.2	6.6	2.2	6.4	ns
t_{PLZ}			1.3	3.2	4.4	1.3	5.4	1.3	4.8	

PARAMETER MEASUREMENT INFORMATION

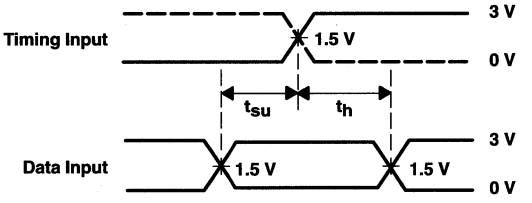


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

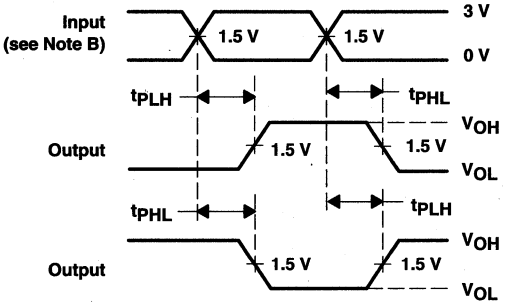
LOAD CIRCUIT FOR OUTPUTS



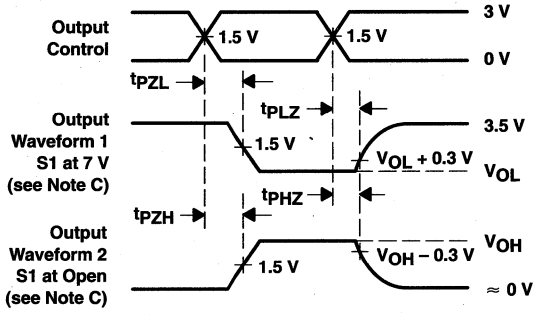
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



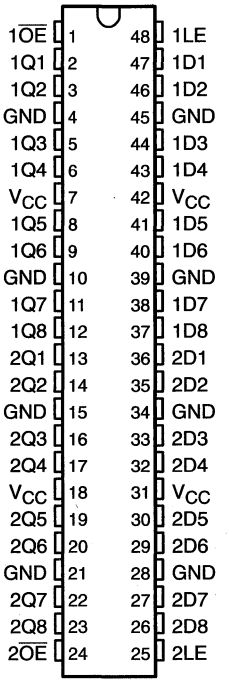
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16373A . . . WD PACKAGE
SN74ABT16373A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT16373A is a 16-bit transparent D-type latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components

The output enable ($\overline{OE}$) does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

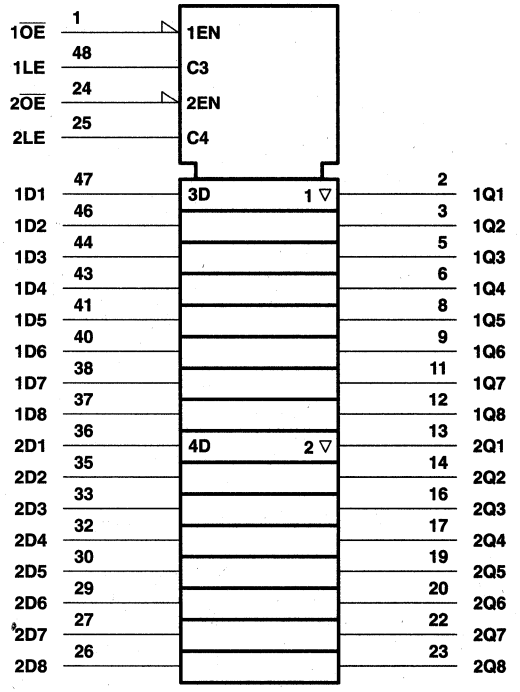
The SN74ABT16373A is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16373A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16373A is characterized for operation from –40°C to 85°C.

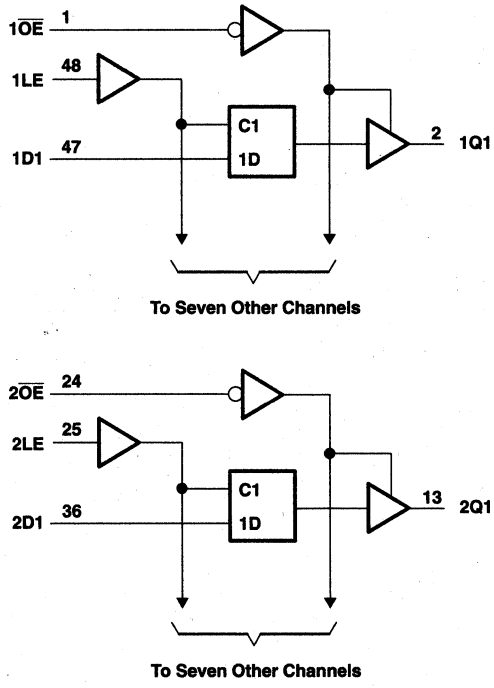
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16373A ..... 96 mA
SN74ABT16373A ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16373A		SN74ABT16373A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16373A		SN74ABT16373A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = –24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			2		2		2	mA
		Outputs low			85		85		85	
		Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3.5						pF
C_o	V_O = 2.5 V or 0.5 V			9.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

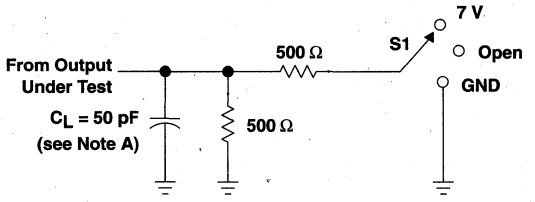
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V_{CC} = 5 V, T_A = 25°C		SN54ABT16373A		SN74ABT16373A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	1.5		1.5		1.5		ns
t_h	Hold time, data after LE↓	1		1		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

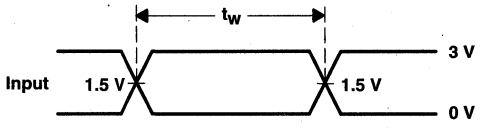
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16373A		SN74ABT16373A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.4	3.7	5.3	1.4	6.5	1.4	6.3	ns
t_{PHL}			2	4	5.4	2	6.5	2	6.2	
t_{PLH}	LE	Q	1.7	4.1	5.7	1.7	7	1.7	6.7	ns
t_{PHL}			2.3	4.3	5.6	2.3	6.3	2.3	6.1	
t_{PZH}	$\overline{OE}$	Q	1.1	3.4	5	1.1	6.4	1.1	6.1	ns
t_{PZL}			1.5	3.5	4.9	1.5	5.8	1.5	5.6	
t_{PHZ}	$\overline{OE}$	Q	2.4	5.1	7.1	2.4	8.5	2.4	8.1	ns
t_{PLZ}			1.6	4.4	5.8	1.6	8	1.6	6.5	

PARAMETER MEASUREMENT INFORMATION

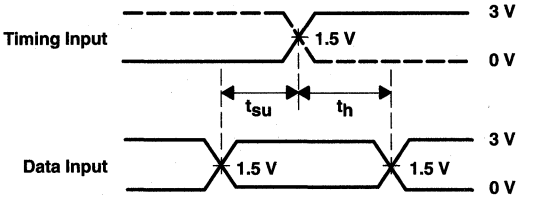


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

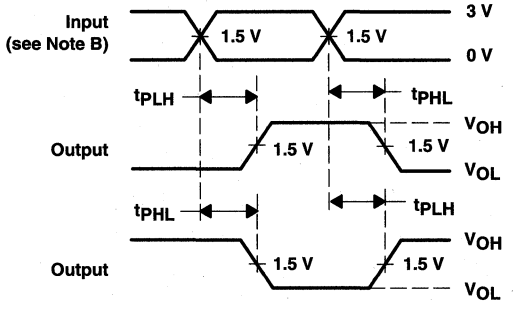
LOAD CIRCUIT FOR OUTPUTS



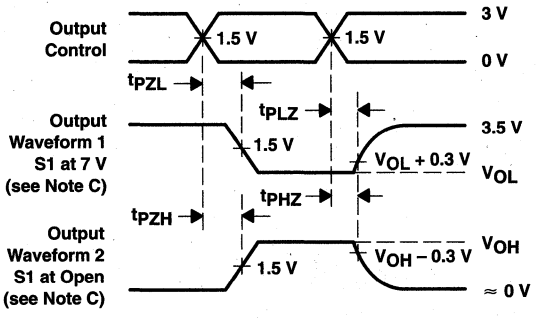
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



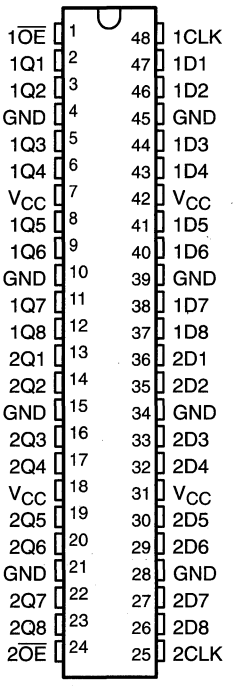
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16374A . . . WD PACKAGE
SN74ABT16374A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT16374A is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components

The output enable ($\overline{OE}$) does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16374A is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16374A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16374A is characterized for operation from –40°C to 85°C.

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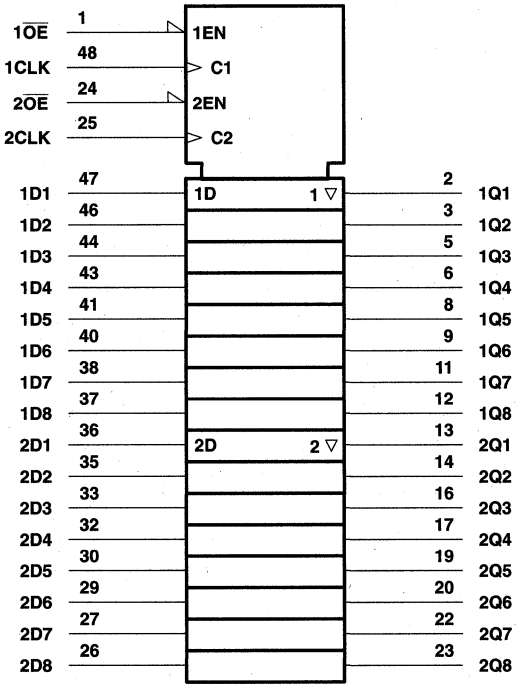
FUNCTION TABLE
(each flip-flop)

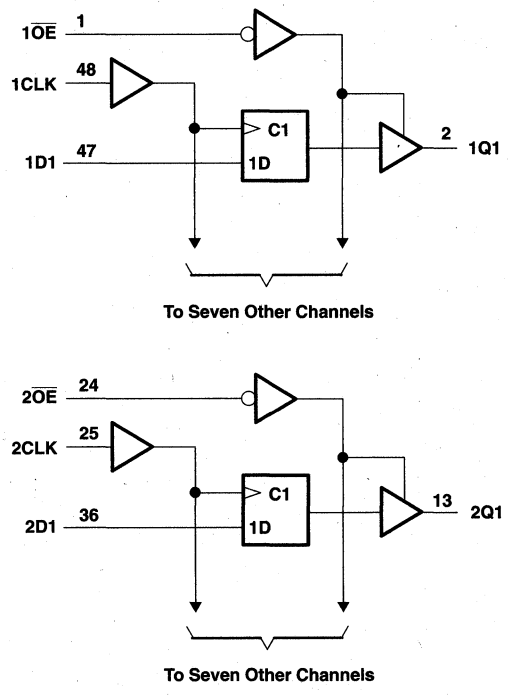
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16374A ..... 96 mA
SN74ABT16374A ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16374A		SN74ABT16374A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16374A		SN74ABT16374A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			2		2		2	mA
		Outputs low			72		72		72	
		Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3.5						pF
C_o	V_O = 2.5 V or 0.5 V			9.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

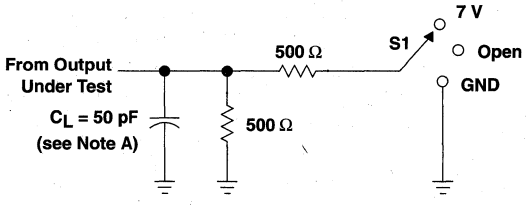
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V_{CC} = 5 V, T_A = 25°C		SN54ABT16374A		SN74ABT16374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	1.1		1.3		1.1		ns
t_h	Hold time, data after CLK↑	1.3		1.5		1.3		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

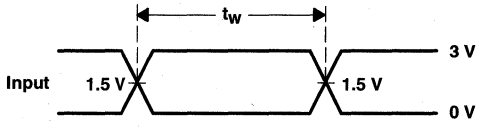
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16374A		SN74ABT16374A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLK	Q	1.8	4.3	5.4	1.5	6.9	1.8	6.2	ns
t_{PHL}			2.7	4.7	5.6	2.2	6.9	2.7	5.9	
t_{PZH}	$\overline{OE}$	Q	1.2	3.4	4.8	0.8	6.1	1.2	5.6	ns
t_{PZL}			1.6	3.5	4.7	1.2	5.5	1.6	5.3	
t_{PHZ}	$\overline{OE}$	Q	2.2	5.5	7.1	1.8	9.6	2.2	8.2	ns
t_{PLZ}			2.2	4.3	5.8	1.8	7.2	2.2	6.6	

PARAMETER MEASUREMENT INFORMATION

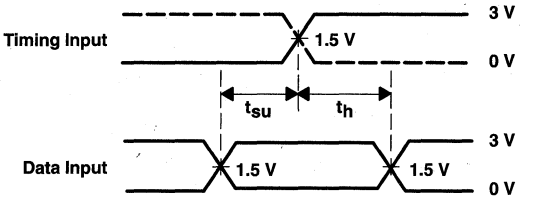


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

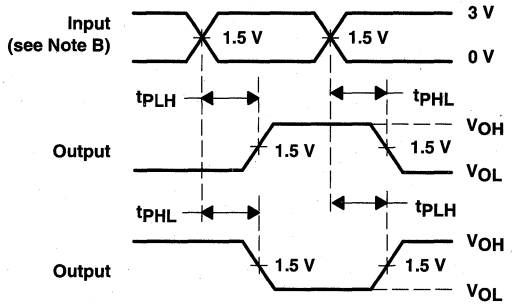
LOAD CIRCUIT FOR OUTPUTS



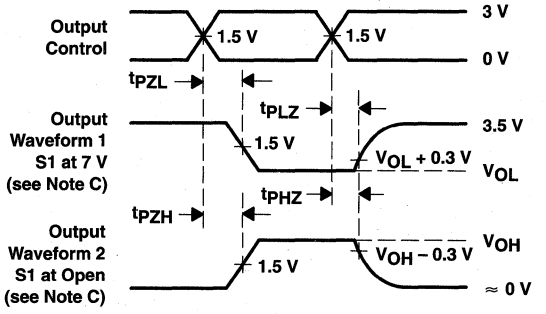
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



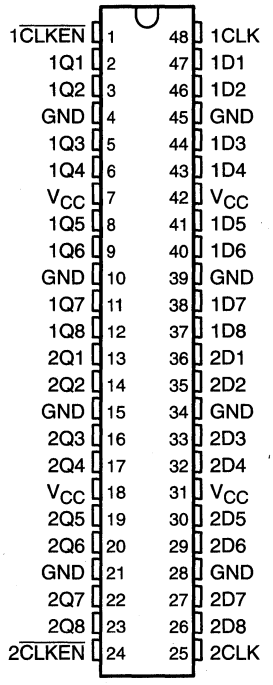
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16377 . . . WD PACKAGE
SN74ABT16377 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16377 is a 16-bit positive-edge-triggered D-type flip-flop with a clock (1CLK or 2CLK) input. It is particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

Data input information that meets the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the common clock-enable (1$\overline{\text{CLKEN}}$ or 2$\overline{\text{CLKEN}}$) input is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the buffered clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at $\overline{\text{CLKEN}}$.

The SN74ABT16377 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16377 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16377 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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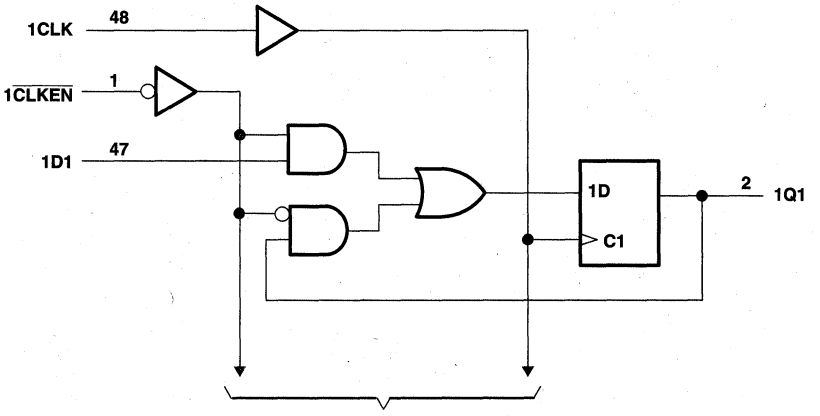
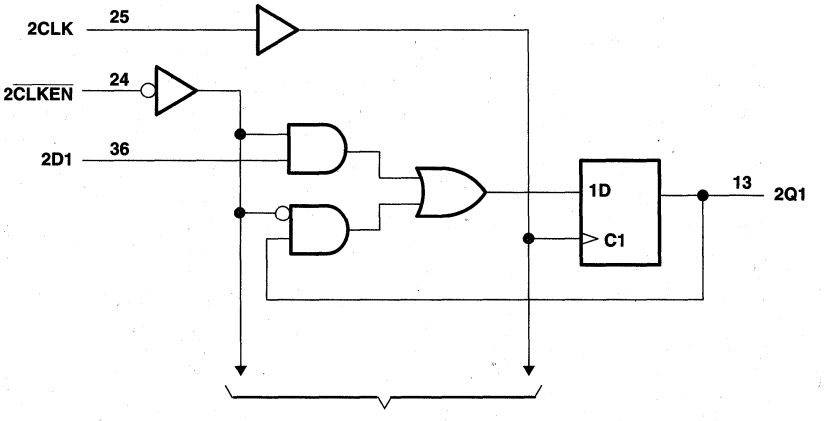
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLKEN}}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	H or L	X	Q_0

logic diagram (positive logic)





PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16377 ..... 96 mA
SN74ABT16377 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT16377		SN74ABT16377		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16377		SN74ABT16377		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			2		2		2	mA
		Outputs low			67		67		67	
		Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V									pF
C_o	V_O = 2.5 V or 0.5 V									pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

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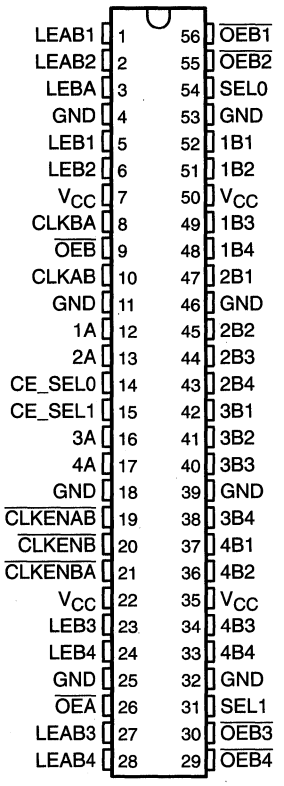
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16460 . . . WD PACKAGE
SN74ABT16460 . . . DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'ABT16460 is a 4-bit-to-1-bit multiplexed registered transceiver used in applications where four separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. This device is also useful in memory-interleaving applications.

Five 4-bit I/O ports (1A–4A, 1B1–4, 2B1–4, 3B1–4, and 4B1–4) are available for address and/or data transfer. The output-enable ($\overline{OEB}$, $\overline{OEB1}$–$\overline{OEB4}$, and $\overline{OEA}$) inputs control the bus transceiver functions. These control signals also allow 4-bit or 16-bit control depending on the $\overline{OEB}$ level.

Address and/or data information can be stored using the internal storage latches/flipflops. The latch-enable (LEB1–LEB4, LEBA, and LEAB1–LEAB4) and clock/clock-enable (CLK/$\overline{CLKEN}$) inputs are used to control data storage. When either one of the latch-enable inputs is high, the latch is transparent (clock is a don't care as long as the latch-enable is high). When the latch-enable input goes low (providing that the clock does not transit from low to high), the data present at the inputs is latched and remains latched until the latch-enable input is returned high. When the clock-enable is low and the corresponding latch-enable is low, data can be clocked on the low to high transition of the clock. When either the clock-enable or the corresponding latch-enable is high, the clock is a don't care.

Four select pins (SEL0, SEL1, CE_SEL0, and CE_SEL1) are provided to multiplex data (A port), or to select one of four clock-enables (B port). This allows the user to have the flexibility of controlling one bit at a time.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

description (continued)

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16460 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16460 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT16460 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
A-TO-B OUTPUT-ENABLE†

INPUTS		OUTPUT
$\overline{OEB}$	$\overline{OEBn}$	Bn
H	H	Z
H	L	Z
L	H	Z
L	L	Active

† n = 1, 2, 3, 4

FUNCTION TABLE
A-TO-B STORAGE (ASSUMING $\overline{OEB}$ = L, $\overline{OEBn}$ = L)‡

INPUTS								OUTPUTS			
$\overline{CLKENAB}$	CE_SEL1	CE_SEL0	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4
X	X	X	H or L	H	L	L	L	A	A_0	A_0	A_0
X	X	X	H or L	H	H	H	L	A	A	A	A_0
L	X	X	L	L	L	L	L	A_0	A_0	A_0	A_0
L	L	L	↑	L	L	L	L	A	A_0	A_0	A_0
L	L	H	↑	L	L	L	L	A_0	A	A_0	A_0
L	H	L	↑	L	L	L	L	A_0	A_0	A	A_0
L	H	H	↑	L	L	L	L	A_0	A_0	A_0	A
H	X	X	↑	L	L	L	L	A_0	A_0	A_0	A_0

‡ This table does not cover all the latch-enable cases since they have similar results.

PRODUCT PREVIEW

Function Tables

B-TO-A STORAGE (BEFORE POINT "P")

INPUTS								"P"
$\overline{\text{CLKENB}}$	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SEL0	
X	X	H	L	L	L	L	L	B1
X	X	L	H	L	L	L	H	B2
X	X	L	L	H	L	H	L	B3
X	X	L	L	L	H	H	H	B4
L	↑	L	L	L	L	L	L	B1
						L	H	B2
						H	L	B3
						H	H	B4
L	H or L	L	L	L	L	L	L	$B1_0$†
						L	H	$B2_0$†
						H	L	$B3_0$†
						H	H	$B4_0$†

B-TO-A STORAGE (AFTER POINT "P")

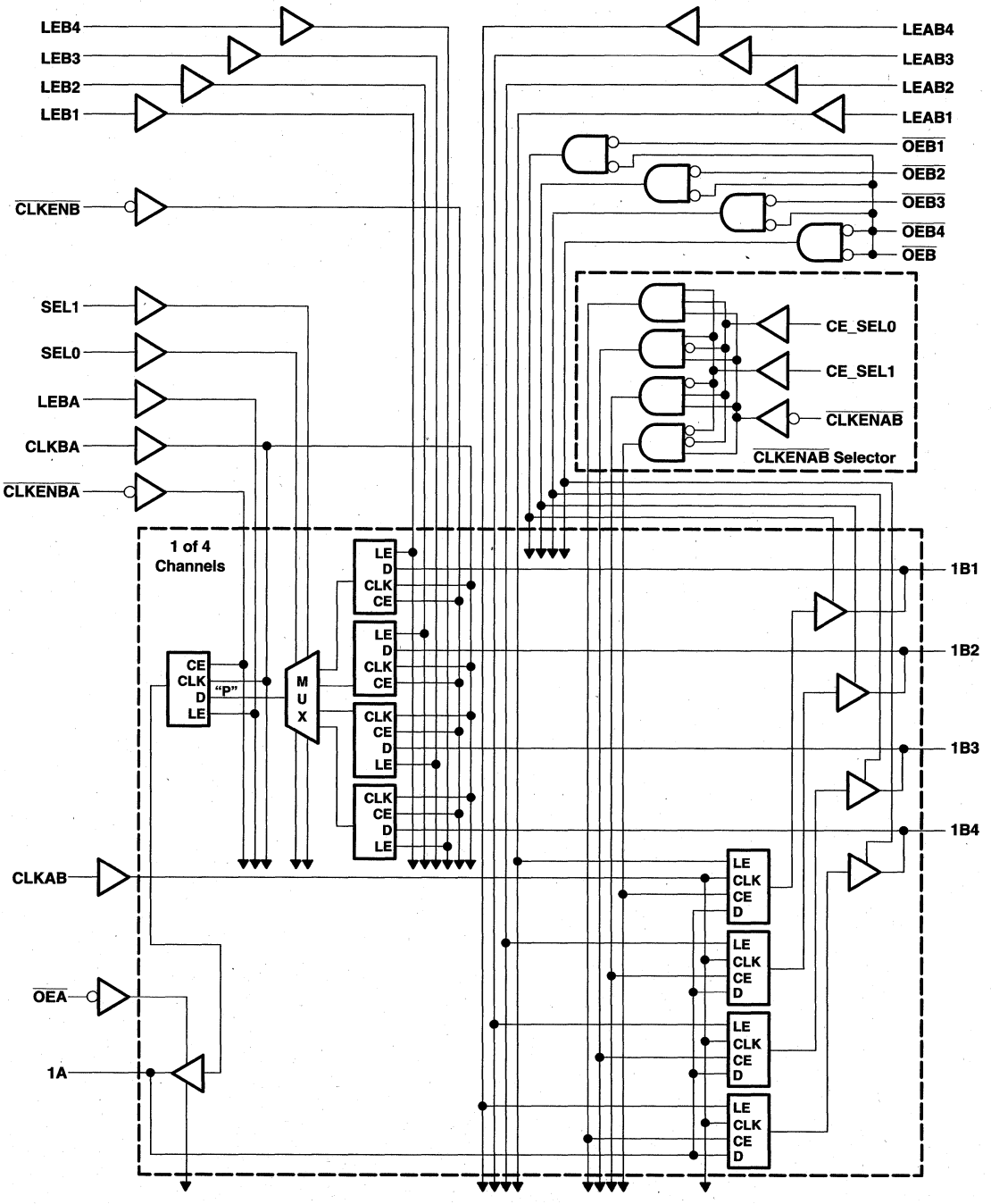
INPUTS					OUTPUT
$\overline{\text{CLKENBA}}$	CLKBA	LEBA	$\overline{\text{OEA}}$	B	A
X	X	X	H	X	Z
X	X	H	L	L	L
X	X	H	L	H	H
H	X	L	L	X	A_0†
L	↑	L	L	L	L
L	↑	L	L	H	H
L	H or L	L	L	X	A_0†

† Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16460 ..... 96 mA
SN74ABT16460 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16460		SN74ABT16460		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16460		SN74ABT16460		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
$I_{I(hold)}$	V_{CC} = 4.5 V,	V_I = 0.8 V	A or B ports						100		µA
	V_{CC} = 4.5 V,	V_I = 2 V							−100		
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			35		35		35	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs								pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports								pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

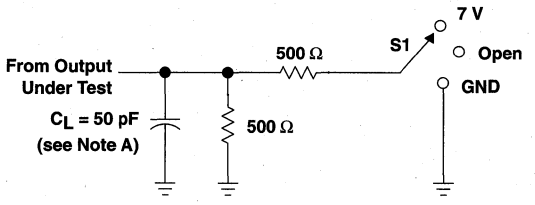
				SN54ABT16460		SN74ABT16460		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high				4		ns
		CLKAB or CLKBA high or low				4		
t_{su}	Setup time	Before CLK↑	A or B			2		ns
			$\overline{CLKEN}$			3		
		A before LEAB↓ or B before LEBA↓	CLK high			2		
			CLK low			2		
t_h	Hold time	After CLK↑	A or B			2		ns
			$\overline{CLKEN}$			2		
		A after LEAB↓ or B after LEBA↓				3		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16460		SN74ABT16460		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A							7	ns
t_{PHL}									7	
t_{PLH}	CLKAB	B								ns
t_{PHL}										
t_{PLH}	CLKBA	A								ns
t_{PHL}										
t_{PLH}	LEAB	B							7	ns
t_{PHL}									7	
t_{PLH}	LEBA	A							6	ns
t_{PHL}									6	
t_{PLH}	LEB	A							8	ns
t_{PHL}									8	
t_{PLH}	SEL	A							8	ns
t_{PHL}									8	
t_{PLH}	CE_SEL	B								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	A or B							10	ns
t_{PZL}									10	
t_{PHZ}	$\overline{OE}$	A or B							10	ns
t_{PLZ}									10	

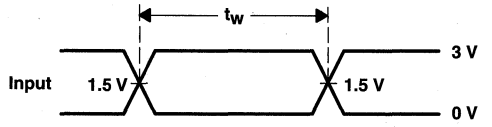
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

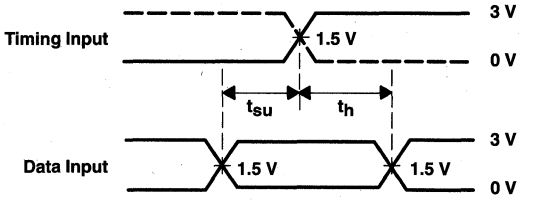


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

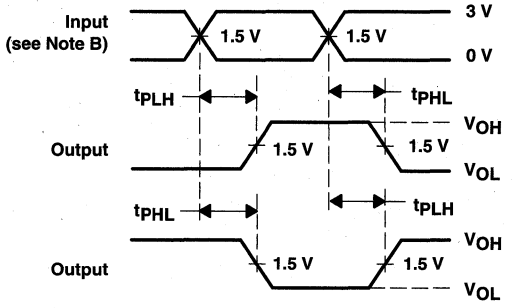
LOAD CIRCUIT FOR OUTPUTS



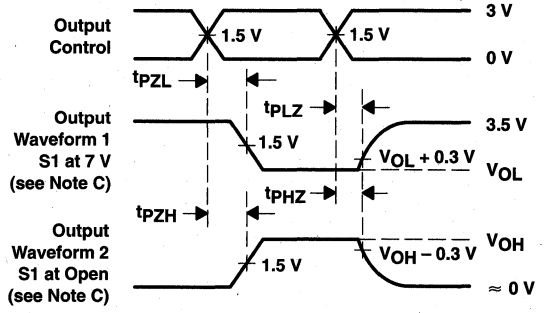
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

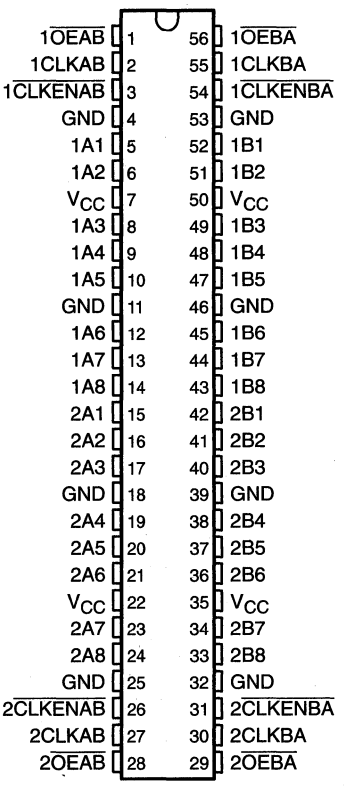
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16470 . . . WD PACKAGE
SN74ABT16470 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16470 is a 16-bit registered transceiver that contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. The 'ABT16470 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate clock (CLKAB or CLKBA) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

To avoid false clocking of the flip-flops, clock enable ($\overline{CLKEN}$) should not be switched from high to low while CLK is high.

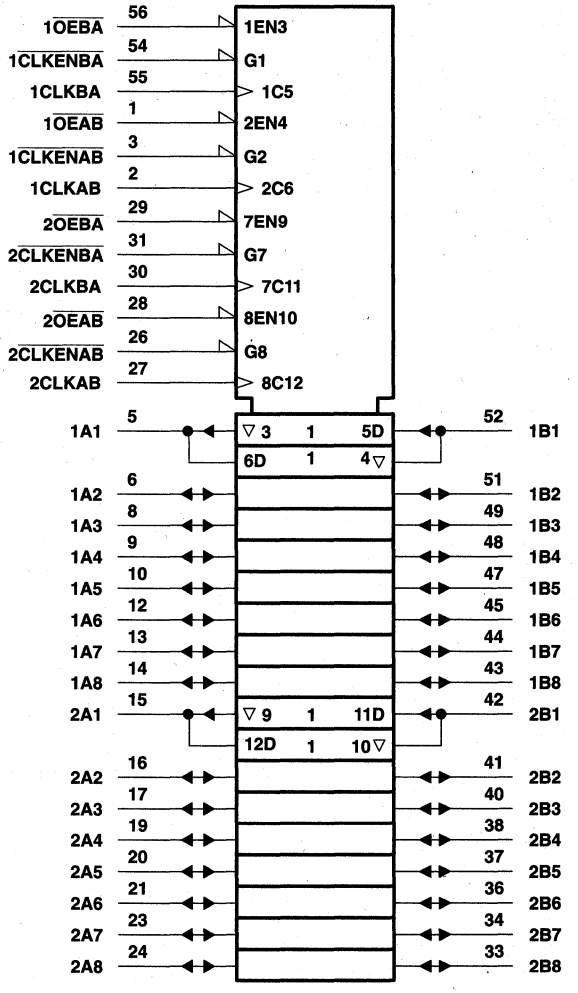
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16470 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16470 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16470 is characterized for operation from –40°C to 85°C.

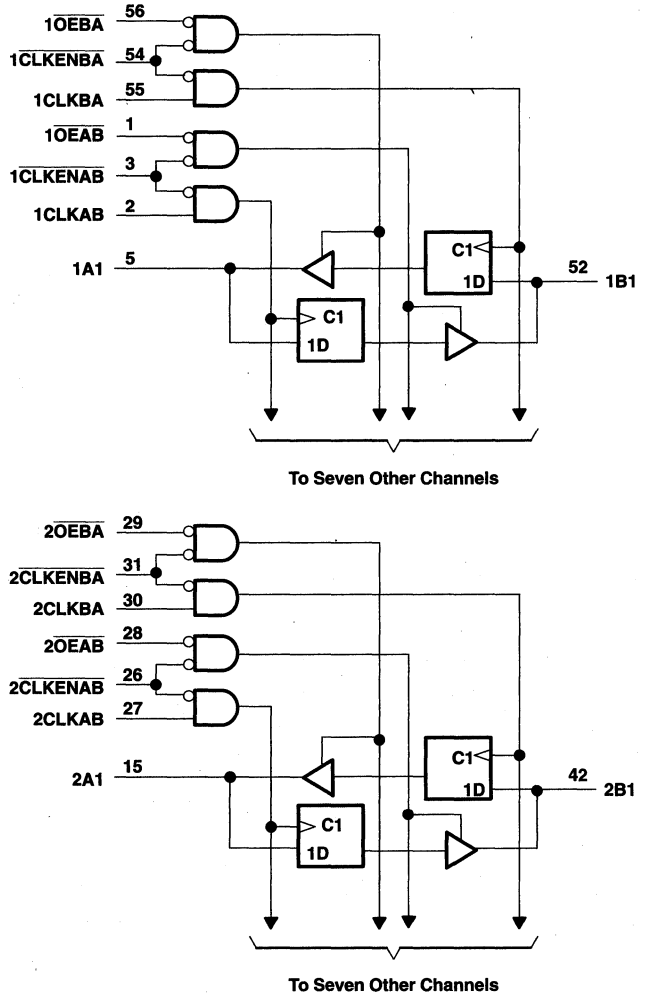
Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.
‡ Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16470 ..... 96 mA
SN74ABT16470 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16470		SN74ABT16470		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16470		SN74ABT16470		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–100	–200	–50	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			35		35		35	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				0.5		0.5		0.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		8.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V_{CC} = 5 V, T_A = 25°C		SN54ABT16470		SN74ABT16470		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	0	150	MHz
t_w‖	Pulse duration, CLKAB or CLKBA high or low	3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLKAB↑ or CLKBA↑	4		4		4		ns
t_h	Hold time, data after CLKAB↑ or CLKBA↑	1		1		1		ns

‖ This parameter is specified by design but not tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16470		SN74ABT16470		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLK	A or B	1.4	3.1	4.8	1.4	5.1	1.4	4.9	ns
t_{PHL}			1.3	3.2	4.6	1.3	5.1	1.3	4.9	
t_{PZH}	$\overline{OE}$	A or B	1	3.1	4.3	1	5	1	4.9	ns
t_{PZL}			1.2	3.6	5.8	1.2	6.9	1.2	6.8	
t_{PHZ}	$\overline{OE}$	A or B	1.9	3.7	4.9	1.9	6	1.9	5.5	ns
t_{PLZ}			1.6	3.3	4.8	1.6	5.4	1.6	5.3	
t_{PZH}	$\overline{CLKEN}$	A or B	1	3.4	4.6	1	5.8	1	5.7	ns
t_{PZL}			1.2	3.9	6	1.2	7.3	1.2	7.2	
t_{PHZ}	$\overline{CLKEN}$	A or B	1.7	3.9	5.2	1.7	6.2	1.7	5.8	ns
t_{PLZ}			1.5	3.6	5.3	1.5	5.5	1.5	5.4	

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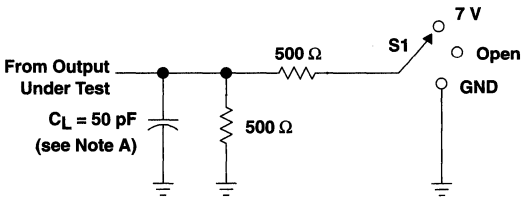
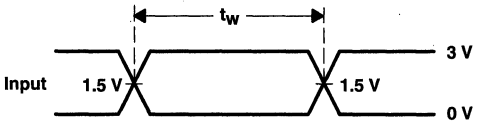
PARAMETER MEASUREMENT INFORMATION

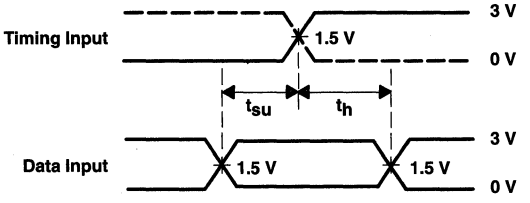


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

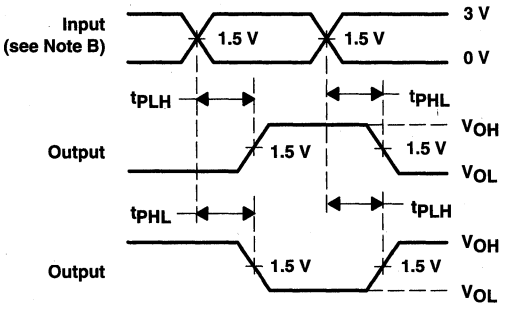
LOAD CIRCUIT FOR OUTPUTS



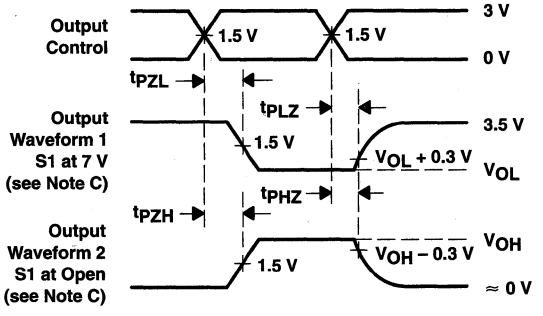
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



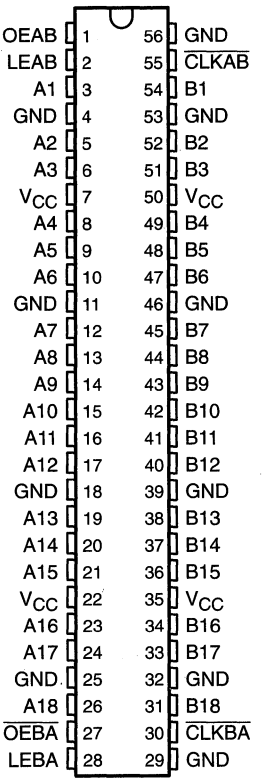
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16500B . . . WD PACKAGE
SN74ABT16500B . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16500B is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16500B is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT16500B is characterized for operation from −40°C to 85°C.

Widebus, EPIC-IIB, and UBT are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

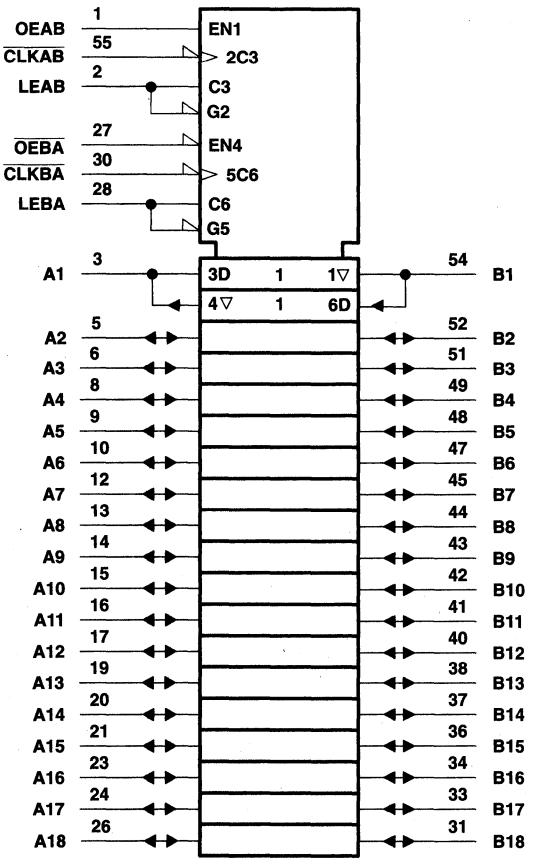
INPUTS				OUTPUT
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.

‡ Output level before the indicated steady-state input conditions were established.

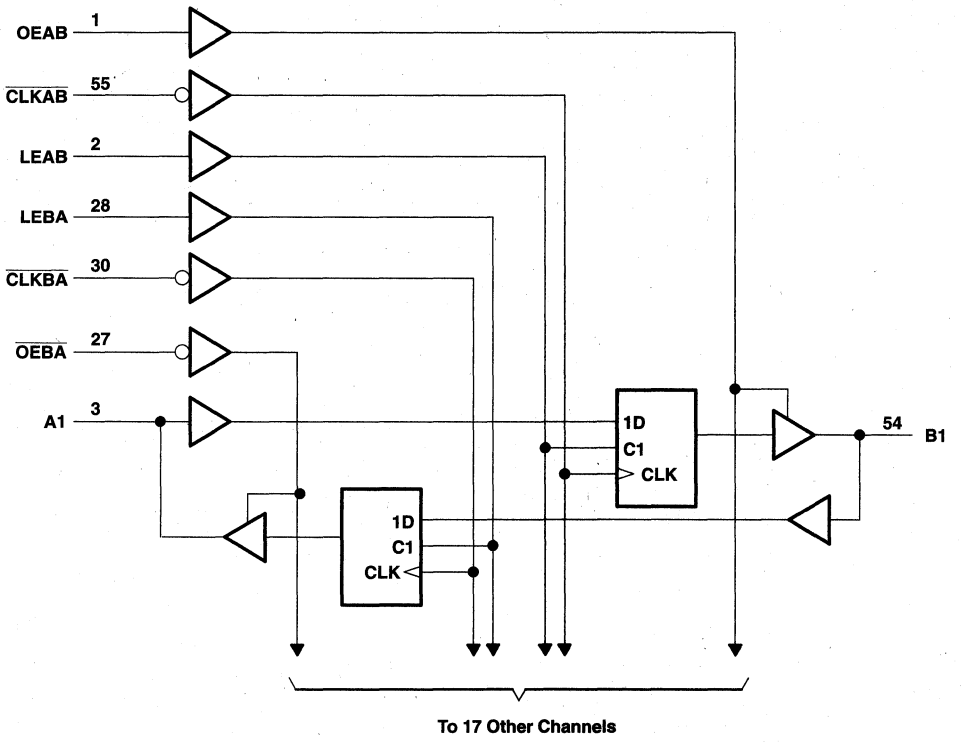
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16500B ..... 96 mA
SN74ABT16500B ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16500B		SN74ABT16500B		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±20		±20		±20	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					10		10		10	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					−10		−10		−10	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

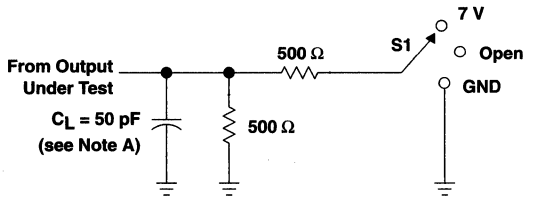
				SN54ABT16500B		SN74ABT16500B		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w†	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low		3		3		
t_{su}	Setup time	A before $\overline{CLKAB}$↓		3		3		ns
		B before $\overline{CLKBA}$↓		3		3		
		A before LEAB↓ or B before LEBA↓	$\overline{CLK}$ high	1		1		
			$\overline{CLK}$ low	2.5		2.5		
t_h	Hold time	A after $\overline{CLKAB}$↓ or B after $\overline{CLKBA}$↓		0		0		ns
		A after LEAB↓ or B after LEBA↓		2		2		

† This parameter is specified by design but not tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

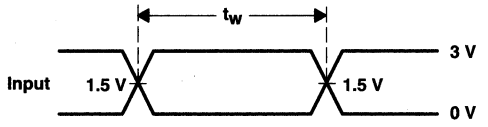
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150		MHz
t_{PLH}	A or B	B or A	1	2.5	3.6	1	4.2	1	4	ns
t_{PHL}			1	3.2	4.5	1	5.1	1	4.9	
t_{PLH}	LEAB or LEBA	B or A	1	3.2	4.5	1	5.6	1	5	ns
t_{PHL}			1	3.4	4.5	1	5.4	1	5	
t_{PLH}	$\overline{CLKAB}$ or $\overline{CLKBA}$	B or A	1	3.5	4.7	1	5.4	1	5.3	ns
t_{PHL}			1	3.5	4.7	1	5.4	1	5.3	
t_{PZH}	OEAB or $\overline{OEBA}$	B or A	1	3.4	4.6	1	5.3	1	5.1	ns
t_{PZL}			1.5	3.8	4.7	1.5	5.6	1.5	5.4	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A	1.5	4.5	5.7	1.5	6.9	1.5	6.5	ns
t_{PLZ}			1.4	3.4	4.7	1.4	5.8	1.4	5.4	

PARAMETER MEASUREMENT INFORMATION

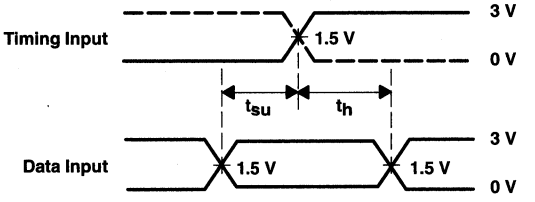


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

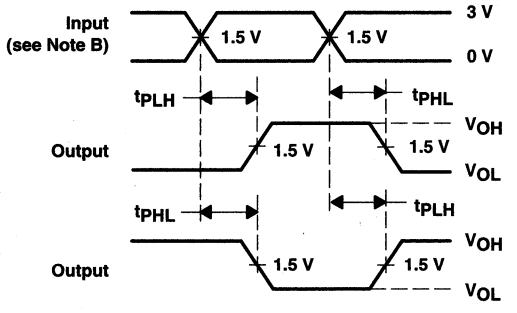
LOAD CIRCUIT FOR OUTPUTS



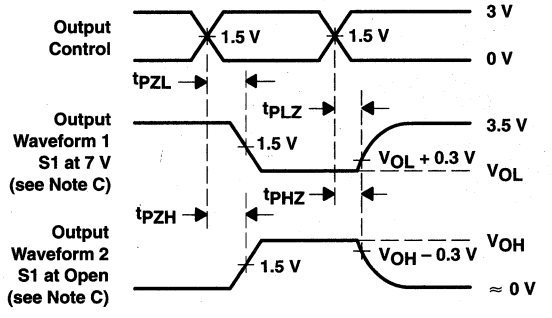
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



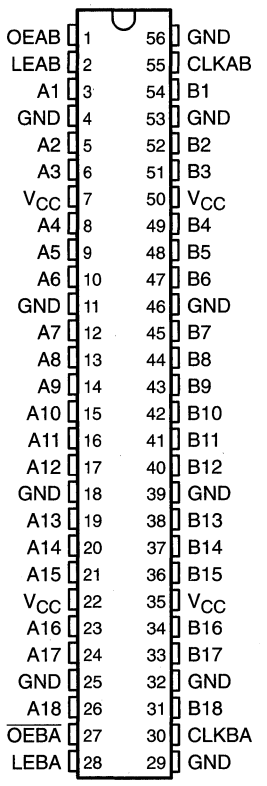
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16501 . . . WD PACKAGE
SN74ABT16501 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers consist of storage elements that can operate either as D-type latches or D-type flip-flops to allow data flow in transparent or clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16501 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16501 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT16501 is characterized for operation from −40°C to 85°C.

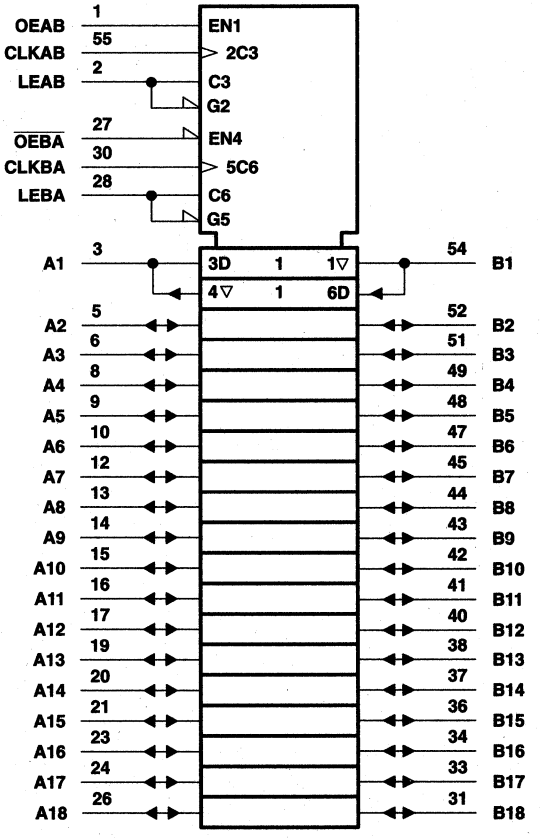
Widebus+, EPIC-IIB, and UBT are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

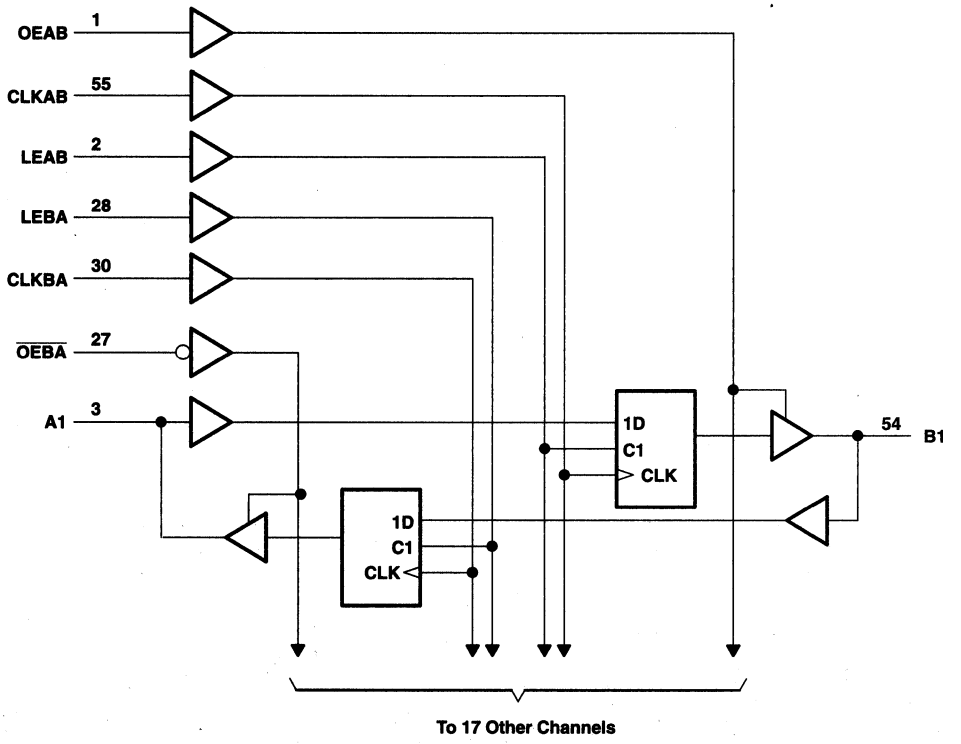
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.
§ Output level before the indicated steady-state input conditions were established.

logic symbol¶



¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16501 ..... 96 mA
SN74ABT16501 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16501		SN74ABT16501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16501		SN74ABT16501		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			3		5		3	mA
			Outputs low			76		76		76	
			Outputs disabled			3.3		5.3		3.3	
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,	Control inputs			5		6		5	mA
			A or B ports			1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

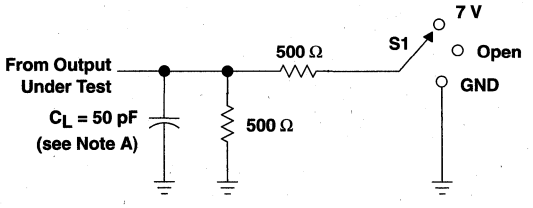
				SN54ABT16501		SN74ABT16501		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKAB or CLKBA			0	105	0	105	MHz
t_w†	Pulse duration	LEAB or LEBA high		3.3		3.3		ns
		CLKAB or CLKBA high or low		4.7		4.7		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑		4		3.5		ns
		A before LEAB↓ or B before LEBA↓	CLK high	4		4		
			CLK low	1.5		1.5		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑		1		1		ns
		A after LEAB↓ or B after LEBA↓		2.5		2.5		

† This parameter is specified by design but not tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

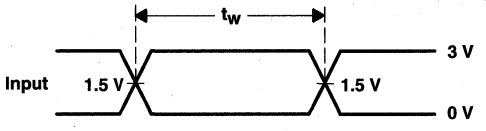
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16501		SN74ABT16501		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		105	160		105		105		MHz
t_{PLH}	A or B	B or A	1	2.6	3.4	1	3.9	1	3.7	ns
t_{PHL}			1	2.6	3.4	1	4.1	1	4	
t_{PLH}	LEAB or LEBA	B or A	1.3	3.3	4.3	1.3	5.4	1.3	5.1	ns
t_{PHL}			1.4	3.1	4.1	1.4	4.6	1.4	4.4	
t_{PLH}	CLKAB or CLKBA	B or A	1.5	3.5	4.5	1.5	5.3	1.5	5	ns
t_{PHL}			1.3	3.1	4.1	1.3	4.6	1.3	4.4	
t_{PZH}	OEAB or $\overline{OEBA}$	B or A	1	3	4	1	4.8	1	4.7	ns
t_{PZL}			2.6	4.9	5.9	2.6	6.6	2.6	6.5	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A	1.6	3.9	4.9	1.6	5.9	1.6	5.8	ns
t_{PLZ}			1.1	3.4	4.4	1.1	5.1	1.1	4.9	

PARAMETER MEASUREMENT INFORMATION

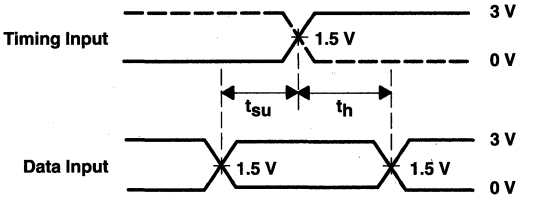


LOAD CIRCUIT FOR OUTPUTS

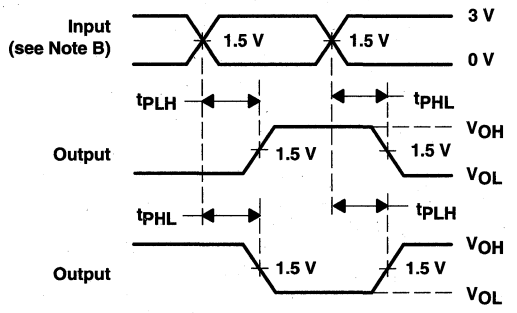
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



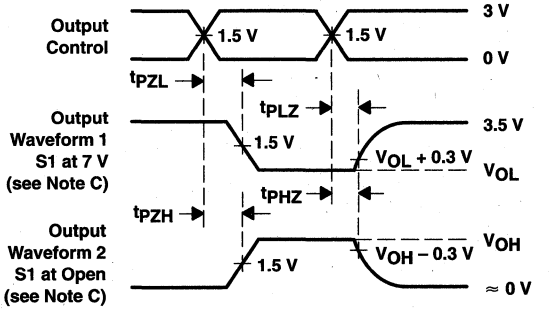
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

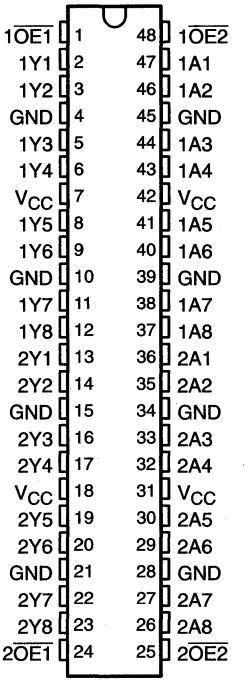
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3796, FEBRUARY 1991 – REVISED OCTOBER 1992

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16540 . . . WD PACKAGE
SN74ABT16540 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16540 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

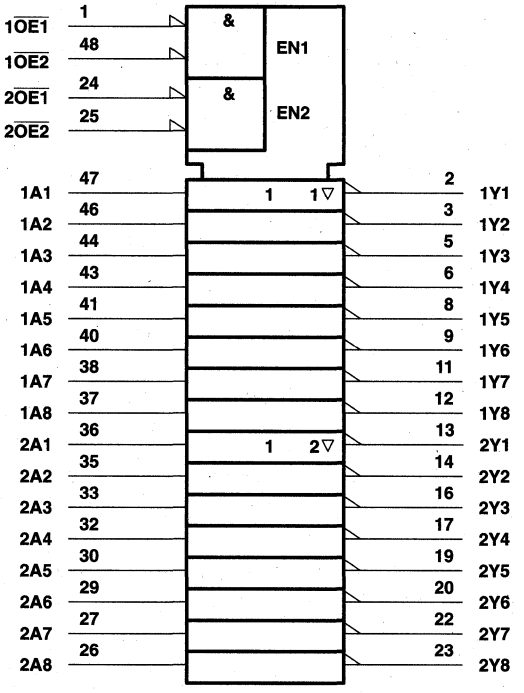
The SN54ABT16540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

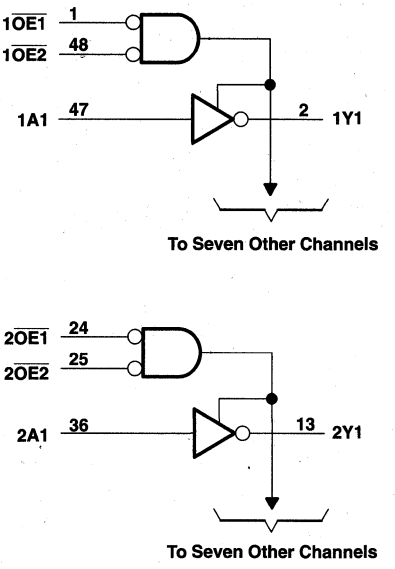
Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16540 ..... 96 mA
SN74ABT16540 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16540		SN74ABT16540		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

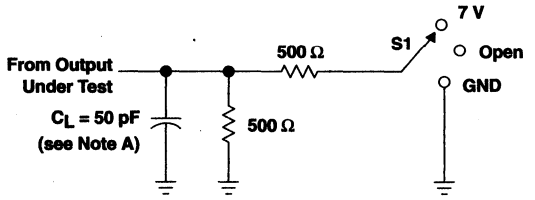
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16540		SN74ABT16540		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1		1	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				7						pF
C_o	V_O = 2.5 V or 0.5 V				7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

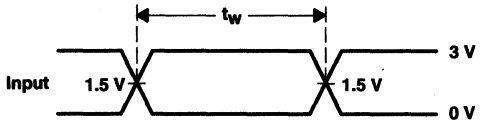
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16540		SN74ABT16540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.3	3.3	1	4.2	1	4.1	ns
t_{PHL}			1.1	2.5	4.1	1.1	4.4	1.1	4.3	
t_{PZH}	$\overline{OE}$	Y	1.1	3.1	4.2	1.1	5.2	1.1	5.1	ns
t_{PZL}			1.6	3.7	4.8	1.6	6	1.6	5.9	
t_{PHZ}	$\overline{OE}$	Y	1.6	3.4	4.6	1.6	5.4	1.6	5.3	ns
t_{PLZ}			1.4	2.9	4.1	1.4	4.7	1.4	4.4	

PARAMETER MEASUREMENT INFORMATION

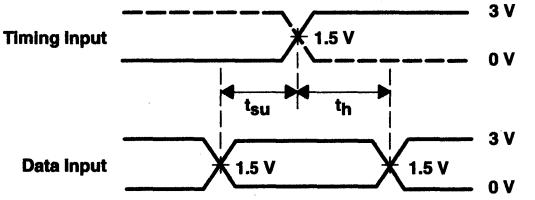


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

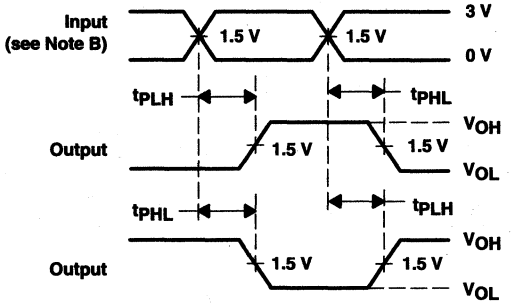
LOAD CIRCUIT FOR OUTPUTS



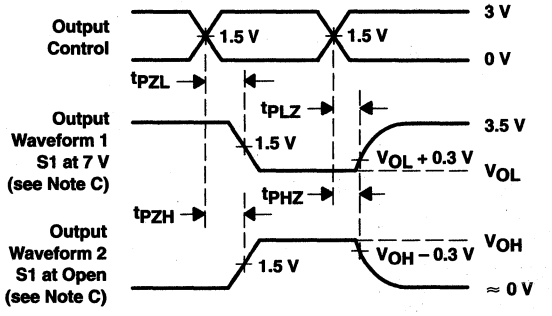
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



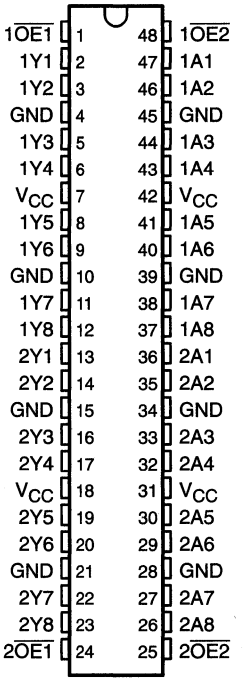
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16541 . . . WD PACKAGE
SN74ABT16541 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT16541 is a noninverting 16-bit buffer composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16541 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

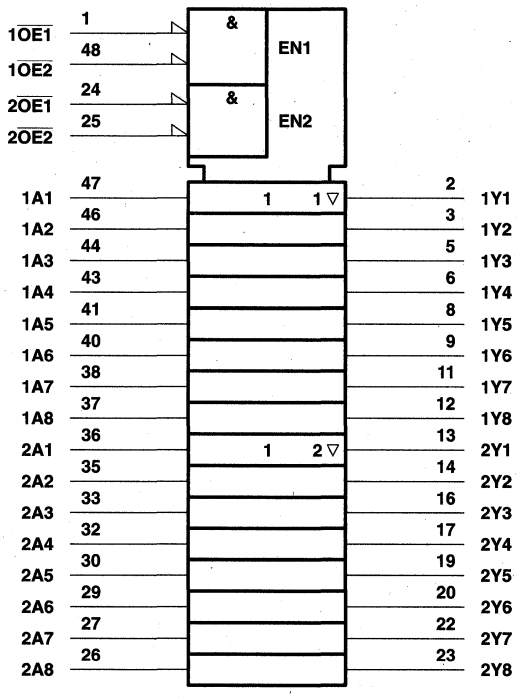
The SN54ABT16541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

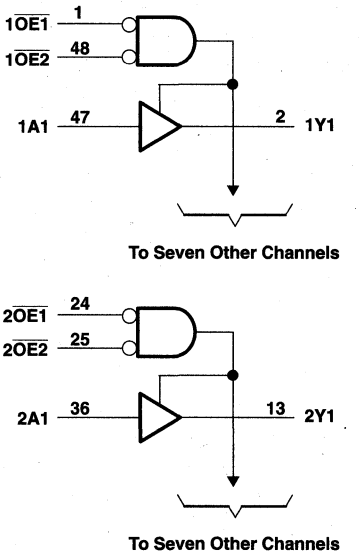
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16541 ..... 96 mA
SN74ABT16541 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16541		SN74ABT16541		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16541		SN74ABT16541		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND					±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V					−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V			−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		0.05		0.05	mA
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				7						pF
C_o	V_O = 2.5 V or 0.5 V				7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
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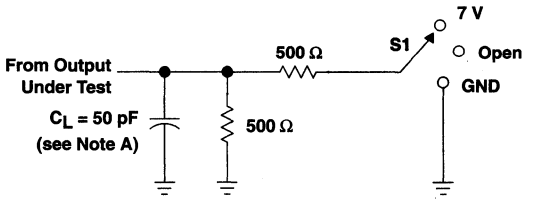
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

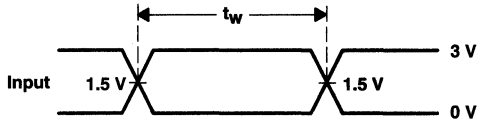
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16541		SN74ABT16541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.1	3	1	3.5	1	3.4	ns
t_{PHL}			1	2.5	3.6	1	4.3	1	4.2	
t_{PZH}	$\overline{OE}$	Y	1.3	3.2	4.3	1.3	5.3	1.3	5.2	ns
t_{PZL}			1.6	3.8	4.7	1.6	6.2	1.6	6	
t_{PHZ}	$\overline{OE}$	Y	1.3	3.4	4.4	1.3	5.4	1.3	5.1	ns
t_{PLZ}			1	2.7	3.6	1	4.3	1	3.9	

PARAMETER MEASUREMENT INFORMATION

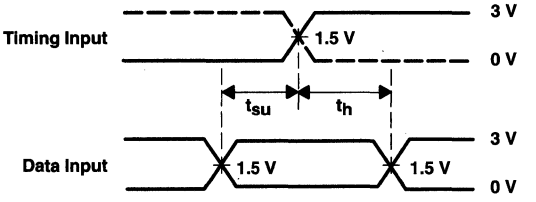


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

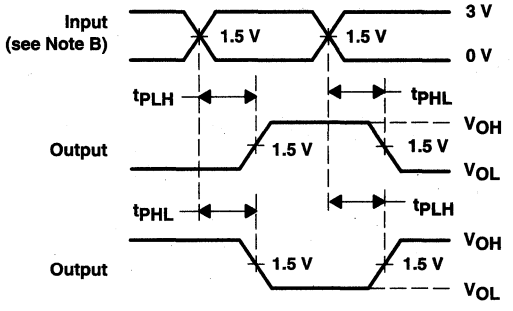
LOAD CIRCUIT FOR OUTPUTS



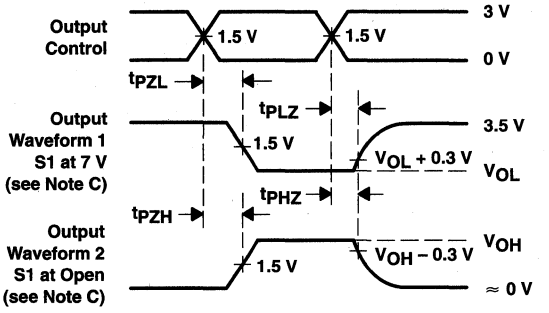
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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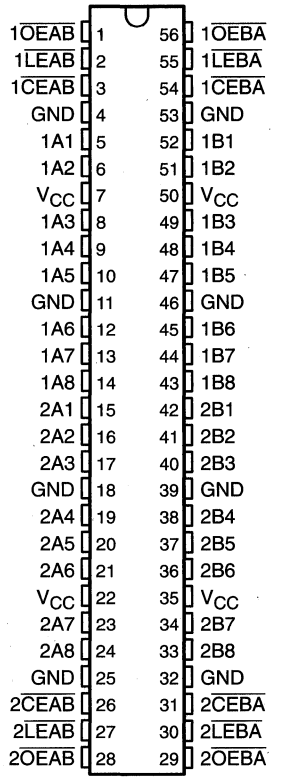
SN54ABT16543 . . . WD PACKAGE
SN74ABT16543 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT16543 16-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. The 'ABT16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16543 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16543 is characterized for operation from –40°C to 85°C.

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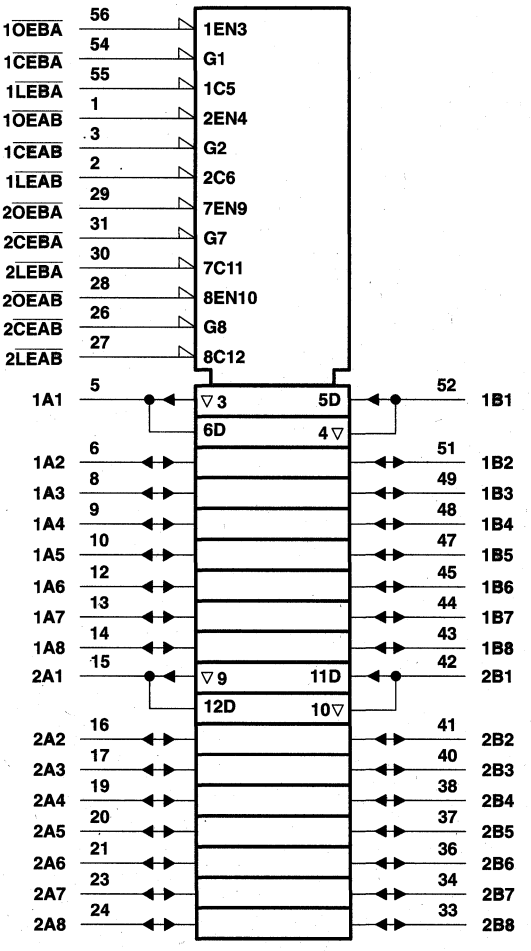
FUNCTION TABLE† (each 8-bit section)

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

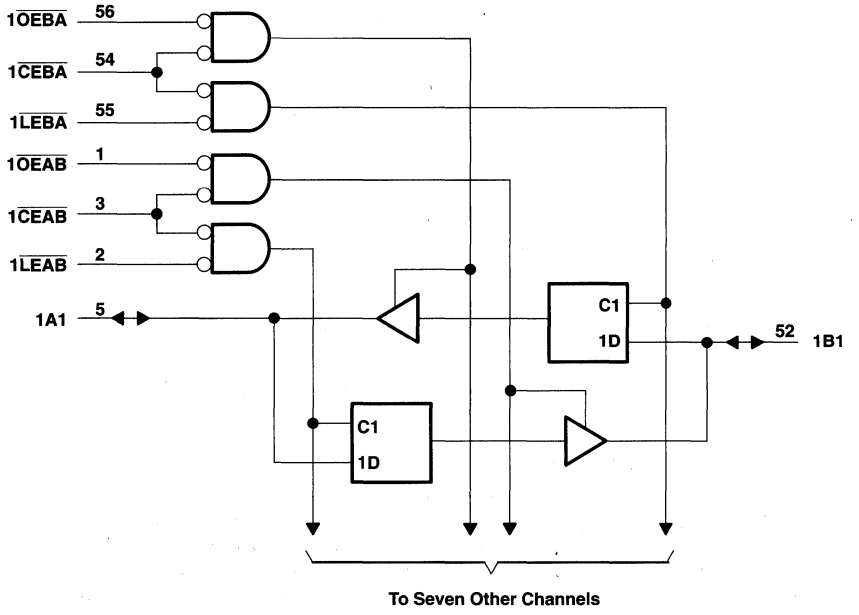
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16543 ..... 96 mA
SN74ABT16543 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16543		SN74ABT16543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16543		SN74ABT16543		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			35		35		35	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				0.5		0.5		0.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		8.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

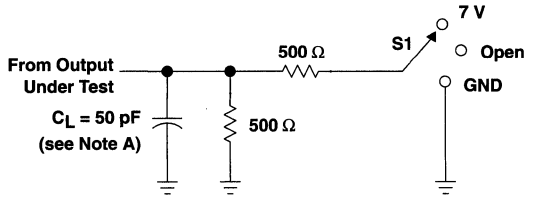
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT16543		SN74ABT16543		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		4		4		4		ns
t_{su}	Setup time, data before LEAB↑ or LEBA↑	High	1.5		1.5		1.5		ns
		Low	3.5		3.5		3.5		
t_h	Hold time, data after LEAB↑ or LEBA↑	High	1.5		1.5		1.5		ns
		Low	2		2		2		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

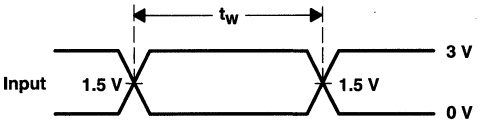
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16543		SN74ABT16543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.5	3.3	0.8	3.9	1	3.8	ns
t_{PHL}			1	2.7	4.4	0.9	5.2	1	5.1	
t_{PLH}	$\overline{LE}$	A or B	1	3.1	4.3	1	5.3	1	5.2	ns
t_{PHL}			1.2	3.3	4.8	1.2	5.7	1.2	5.6	
t_{PZH}	$\overline{OE}$	A or B	1	3.4	4.3	0.8	5.3	1	5.2	ns
t_{PZL}			1.1	3.8	5.9	1.1	7.1	1.1	7	
t_{PHZ}	$\overline{OE}$	A or B	1.9	4	5	1.9	7.2	1.9	5.7	ns
t_{PLZ}			1.6	3.3	4.2	1.6	5	1.6	4.6	
t_{PZH}	$\overline{CE}$	A or B	1	3.8	4.9	0.9	6.3	1	6.2	ns
t_{PZL}			1.2	4.2	6.5	1.2	7.9	1.2	7.8	
t_{PHZ}	$\overline{CE}$	A or B	2	4.5	5.6	2	7.3	2	6.6	ns
t_{PLZ}			1.7	3.9	5.1	1.7	5.6	1.7	5.4	

PARAMETER MEASUREMENT INFORMATION

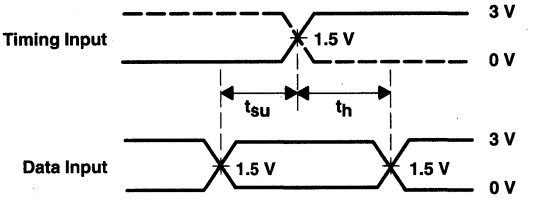


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

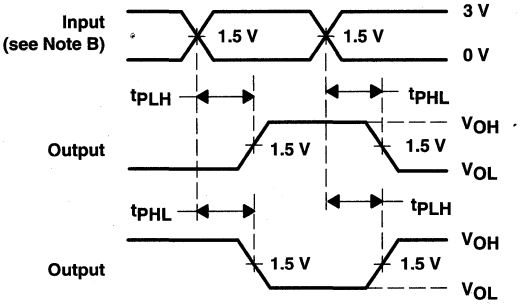
LOAD CIRCUIT FOR OUTPUTS



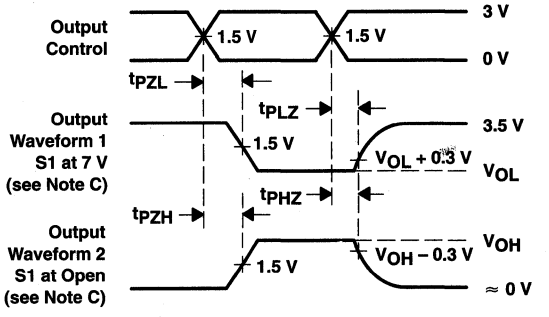
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



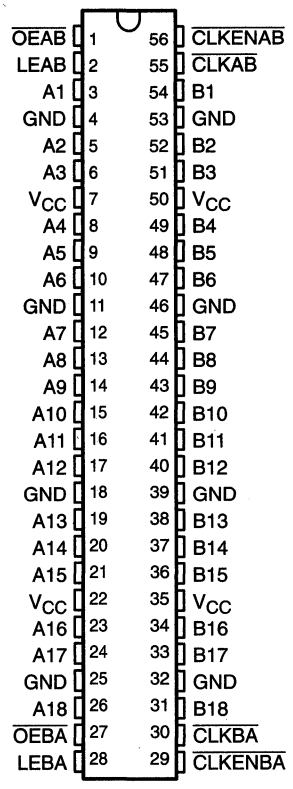
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16600 . . . WD PACKAGE
SN74ABT16600 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CLKAB}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{CLKAB}$. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CLKENBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16600 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16600 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT16600 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE†

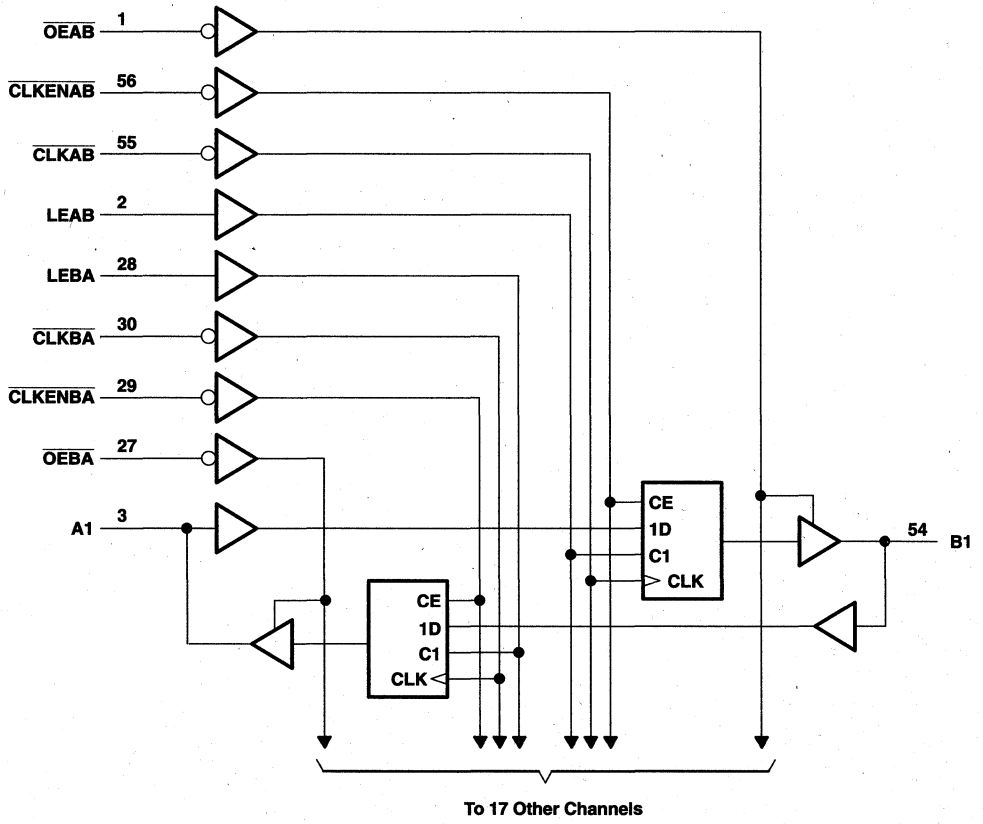
INPUTS					OUTPUT
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	$\overline{CLKAB}$	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B_0‡
L	L	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CLKENBA}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16600 ..... 96 mA
SN74ABT16600 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16600		SN74ABT16600		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16600		SN74ABT16600		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±20		±20		±20	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					10		10		10	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					−10		−10		−10	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

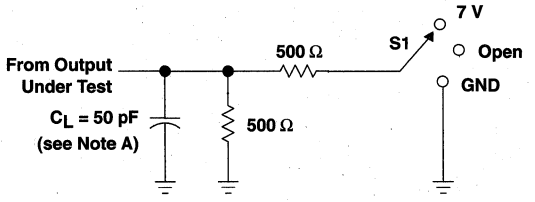
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54ABT16600		SN74ABT16600		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high	2.5		2.5		ns
		$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low	3		3		
t_{su}	Setup time	A before $\overline{CLKAB}\downarrow$ or B before $\overline{CLKBA}\downarrow$	3		3		ns
		A before LEAB↓ or B before LEBA↓	2.5		2.5		
		$\overline{CLKEN}$ before CLK↓	2.5		2.5		
t_h	Hold time	A after $\overline{CLKAB}\downarrow$ or B after $\overline{CLKBA}\downarrow$	0		0		ns
		A after LEAB↓ or B after LEBA↓	2		2		
		$\overline{CLKEN}$ after CLK↑	1		1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

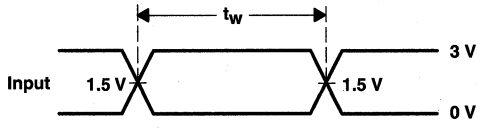
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16600		SN74ABT16600		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	A or B	B or A	1.5	2.5	3.6	1.5	4.2	1.5	4	ns
t_{PHL}			1.5	3.2	4.5	1.5	5.1	1.5	4.9	
t_{PLH}	LEAB or LEBA	B or A	2	3.2	4.5	2	5.6	2	5	ns
t_{PHL}			2	3.4	4.5	2	5.4	2	5	
t_{PLH}	$\overline{CLKAB}$ or $\overline{CLKBA}$	B or A	2	3.5	4.7	2	5.4	2	5.3	ns
t_{PHL}			2	3.5	4.3	2	5.2	2	5	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	1.5	3.4	4.6	1.5	5.3	1.5	5.1	ns
t_{PZL}			2	3.8	4.7	2	5.6	2	5.4	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.5	5.4	2	6.6	2	6.2	ns
t_{PLZ}			1.5	3.4	4.7	1.5	5.8	1.5	5.4	

PARAMETER MEASUREMENT INFORMATION

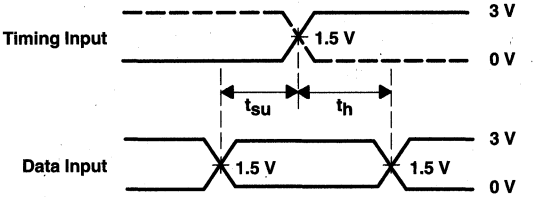


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

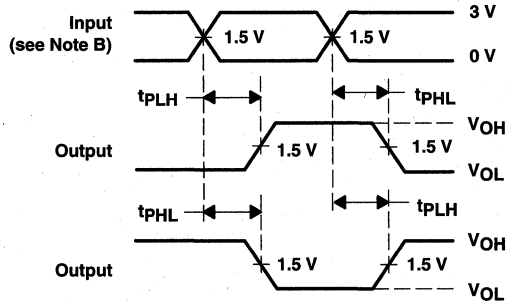
LOAD CIRCUIT FOR OUTPUTS



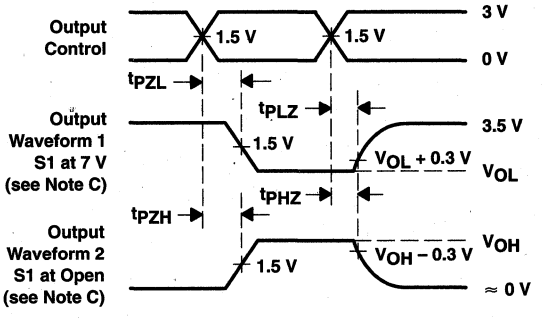
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



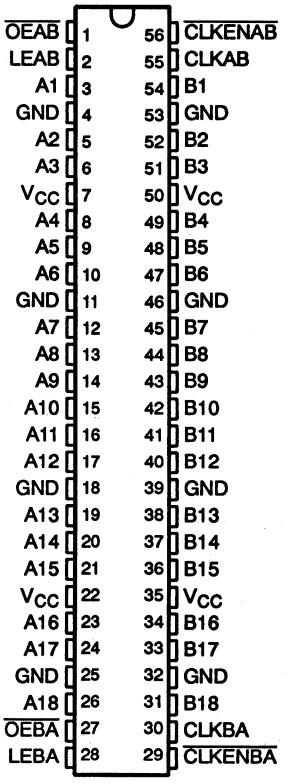
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BICMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16601 . . . WD PACKAGE
SN74ABT16601 . . . DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16601 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

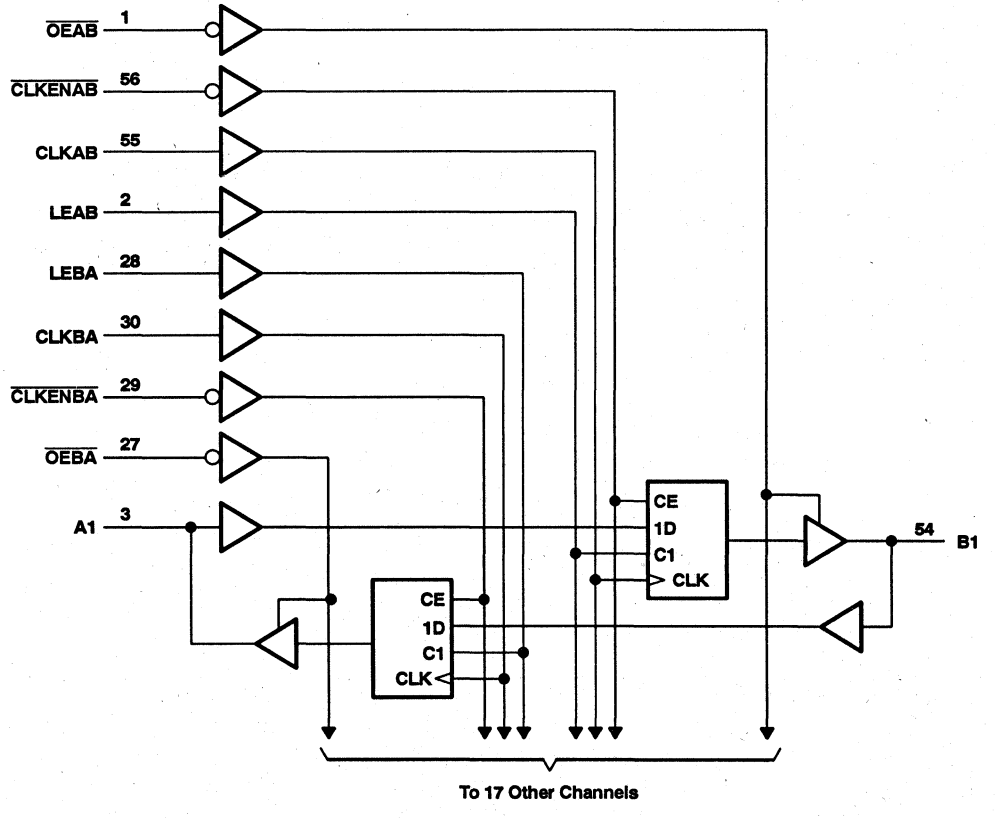
The SN54ABT16601 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT16601 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE†

INPUTS					OUTPUT
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.
‡ Output level before the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16601 ..... 96 mA
SN74ABT16601 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16601		SN74ABT16601		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16601		SN74ABT16601		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±20		±20		±20	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				10		10		10	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−10		−10		−10	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1.9	3		3		3	mA
			Outputs low		28	36		36		36	
			Outputs disabled		1.6	3		3		3	
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

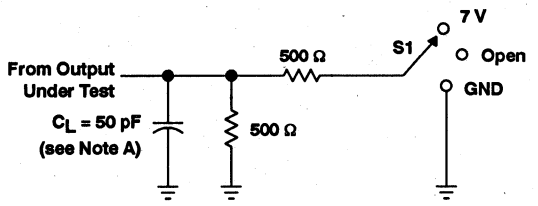
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ABT16601		SN74ABT16601		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		CLKAB or CLKBA high or low		3		3		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑		4		4		ns
		A before LEAB↓ or B before LEBA↓	CLK high	2.5		2.5		
			CLK low			1		
		$\overline{CLKEN}$ before CLK↑		2.5		2.5		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑		0		0		ns
		A after LEAB↓ or B after LEBA↓		2		2		
		$\overline{CLKEN}$ after CLK↑		0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

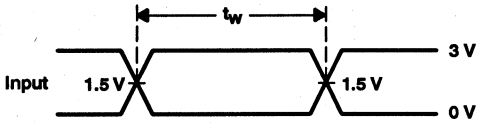
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16601		SN74ABT16601		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150		MHz
t_{PLH}	A or B	B or A	1.5	2.5	3.6	1.5	4.2	1.5	4	ns
t_{PHL}			1.5	3.4	4.7	1.5	5	1.5	4.9	
t_{PLH}	LEAB or LEBA	B or A	2	3.4	4.7	2	5.6	2	5	ns
t_{PHL}			2	3.7	5	2	5.5	2	5.2	
t_{PLH}	CLKAB or CLKBA	B or A	1.5	3.2	4.5	1.5	4.9	1.5	4.7	ns
t_{PHL}			1.5	3.2	4.4	1.5	4.8	1.5	4.6	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4	5	2	5.7	2	5.5	ns
t_{PZL}			2	4.2	5.6	2	6	2	5.8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.5	5.4	2	6.6	2	6.2	ns
t_{PLZ}			1.5	3.4	4.7	1.5	5.8	1.5	5.4	

PARAMETER MEASUREMENT INFORMATION

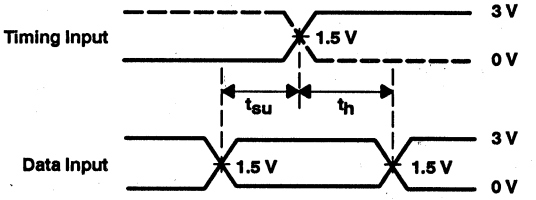


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

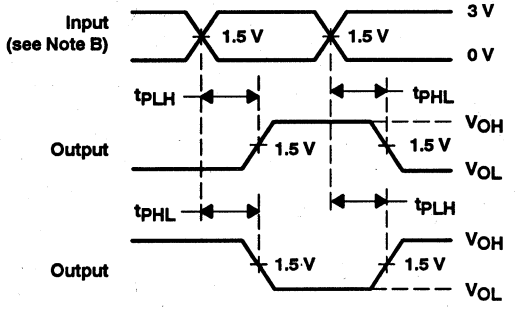
LOAD CIRCUIT FOR OUTPUTS



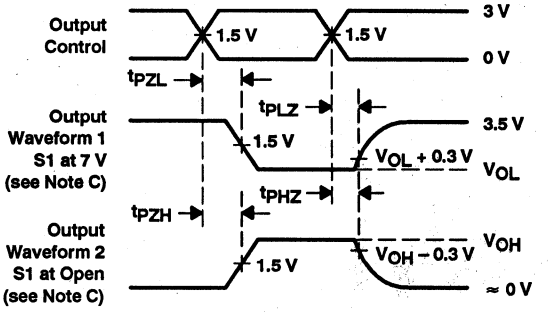
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

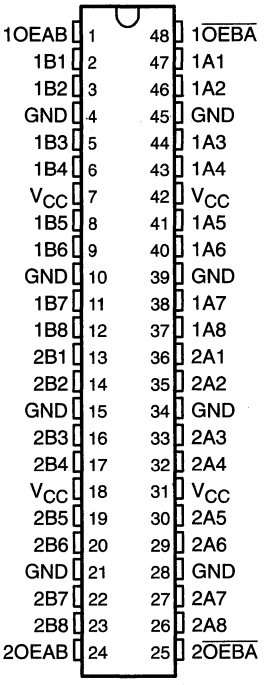
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3799, FEBRUARY 1991 – REVISED OCTOBER 1992

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16623 . . . WD PACKAGE
SN74ABT16623 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16623 is a 16-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing. The 'ABT16623 provides true data at its outputs.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and $\overline{\text{OEBA}}$) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this configuration. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (32 in all) will remain at their last states.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16623 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

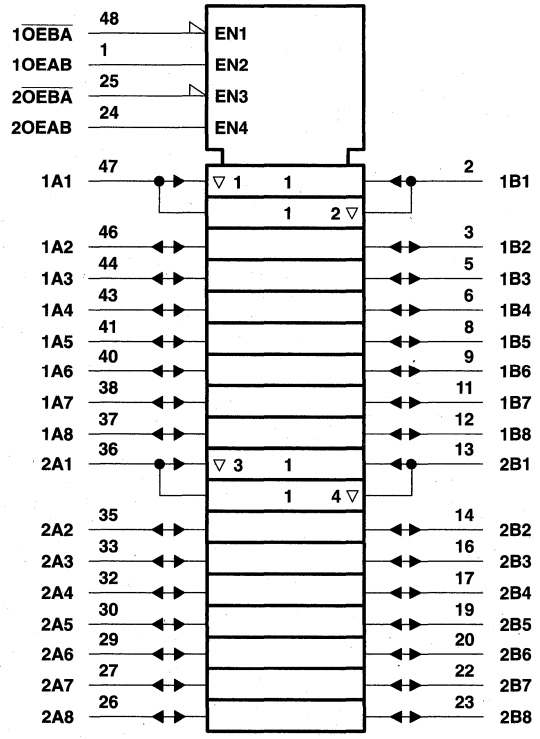
The SN54ABT16623 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16623 is characterized for operation from –40°C to 85°C.

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each 8-bit section)

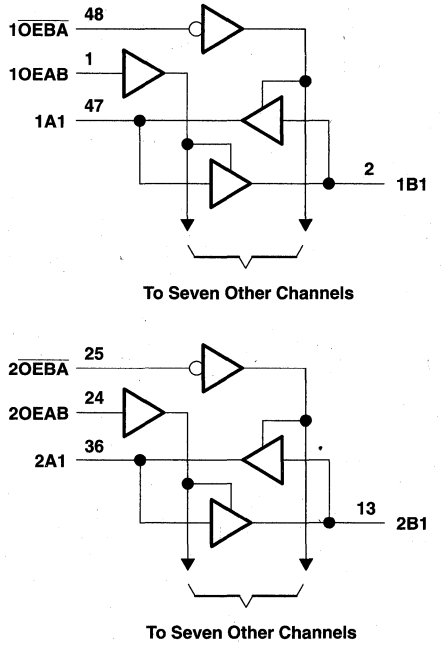
INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	B data to A bus
L	H	B data to A bus, A data to B bus
H	L	Isolation
H	H	A data to B bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16623 ..... 96 mA
SN74ABT16623 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16623		SN74ABT16623		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

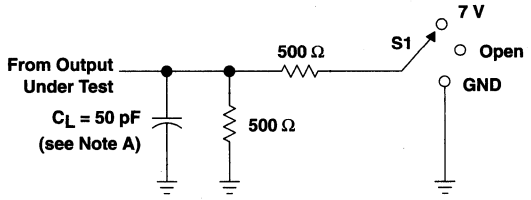
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16623		SN74ABT16623		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			35		35		35	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

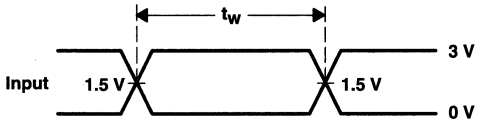
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16623		SN74ABT16623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2	3.2	1	3.7	1	3.6	ns
t_{PHL}			1	2.2	3.4	1	4.4	1	4.3	
t_{PZH}	$\overline{OEBA}$ or OEAB	A or B	1.1	3	4	1.1	5	1.1	4.9	ns
t_{PZL}			1.4	3.3	4.9	1.4	6.2	1.4	6	
t_{PHZ}	$\overline{OEBA}$ or OEAB	A or B	1	3.5	4.9	1	6.2	1	6	ns
t_{PLZ}			1.4	2.8	4.7	1.4	5.6	1.4	5.4	

PARAMETER MEASUREMENT INFORMATION

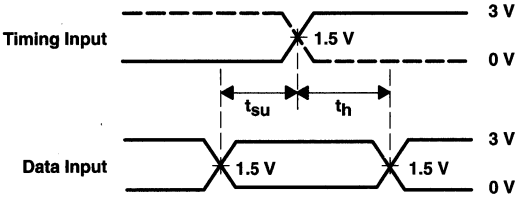


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

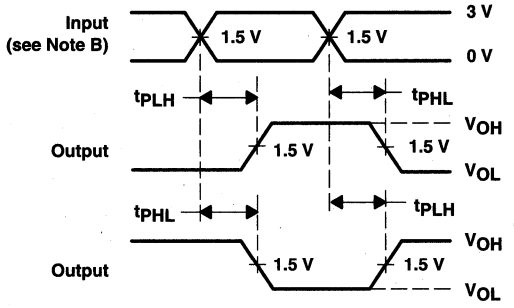
LOAD CIRCUIT FOR OUTPUTS



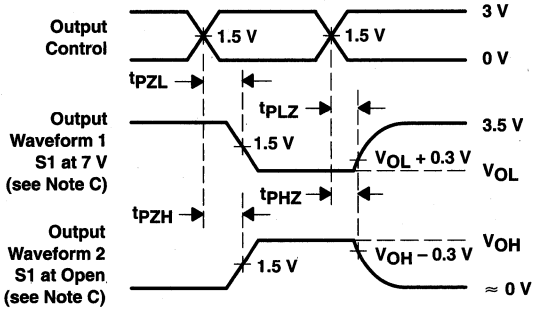
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



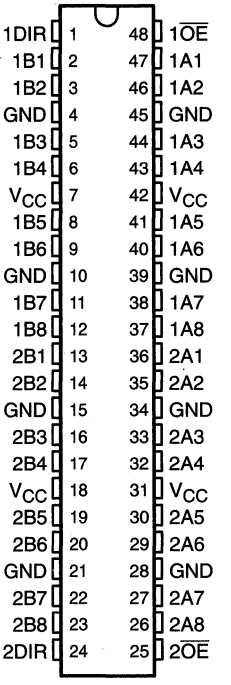
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16640 . . . WD PACKAGE
SN74ABT16640 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16640 is an inverting 16-bit transceiver designed for asynchronous communication between data buses.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (1DIR and 2DIR) inputs. The output-enable (1$\overline{OE}$ and 2$\overline{OE}$) inputs can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16640 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

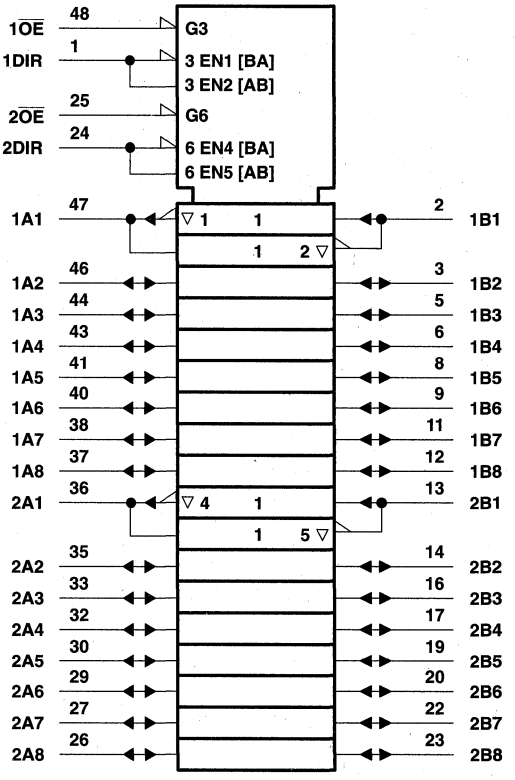
The SN54ABT16640 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16640 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

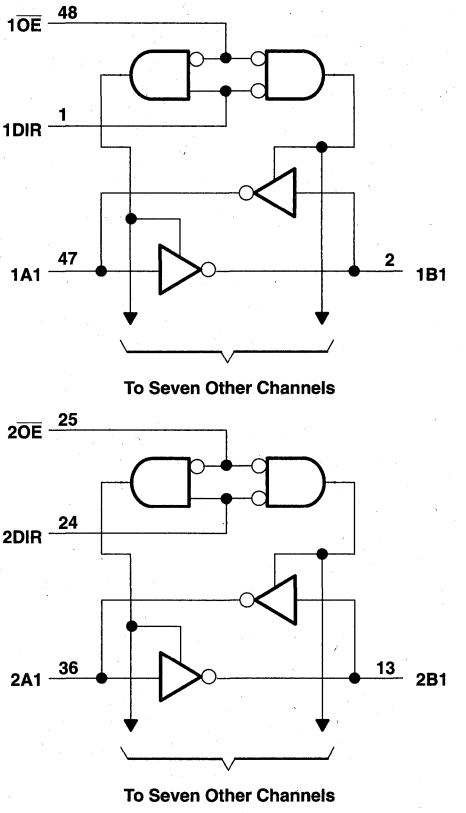
Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16640 ..... 96 mA
SN74ABT16640 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16640		SN74ABT16640		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

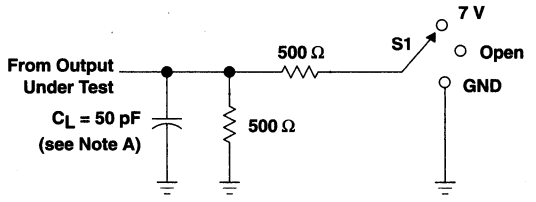
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16640		SN74ABT16640		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

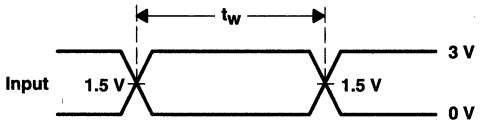
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16640		SN74ABT16640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.5	3.4	1	4.4	1	4.3	ns
t_{PHL}			1.1	2.8	3.6	1.1	4	1.1	3.9	
t_{PZH}	$\overline{OE}$	A or B	1.2	3.5	4.5	1.2	5.6	1.2	5.5	ns
t_{PZL}			1.5	3.9	5	1.5	6.4	1.5	6.3	
t_{PHZ}	$\overline{OE}$	A or B	1.8	3.8	4.8	1.8	6.5	1.8	6.3	ns
t_{PLZ}			1.5	3	3.9	1.5	4.4	1.5	4.2	

PARAMETER MEASUREMENT INFORMATION

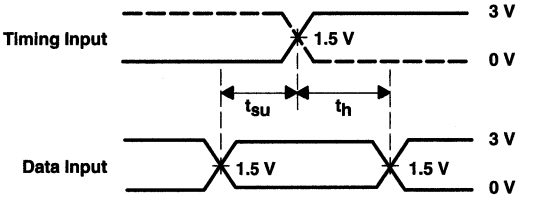


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

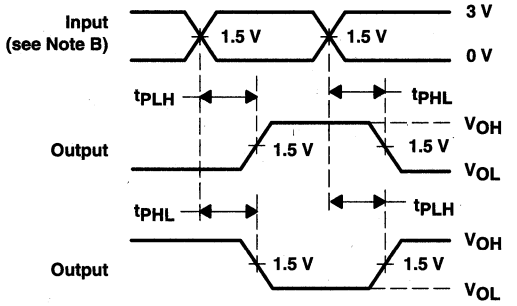
LOAD CIRCUIT FOR OUTPUTS



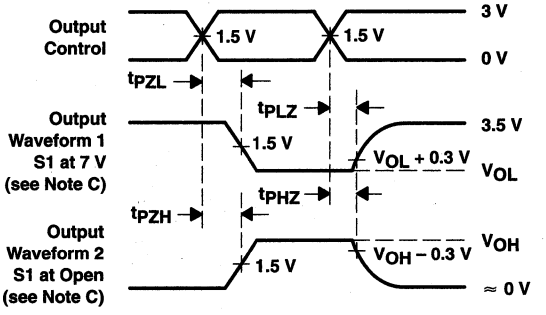
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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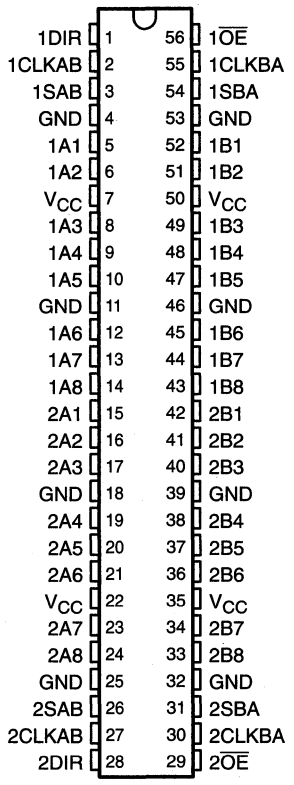
SN54ABT16646 . . . WD PACKAGE
SN74ABT16646 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16646 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16646 is characterized for operation from –40°C to 85°C.

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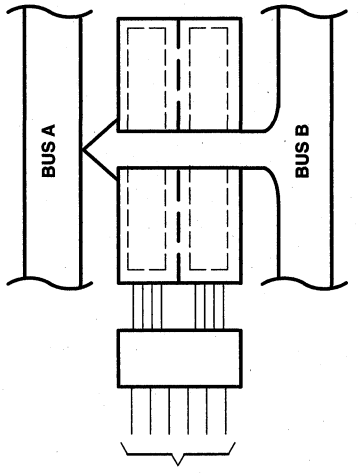
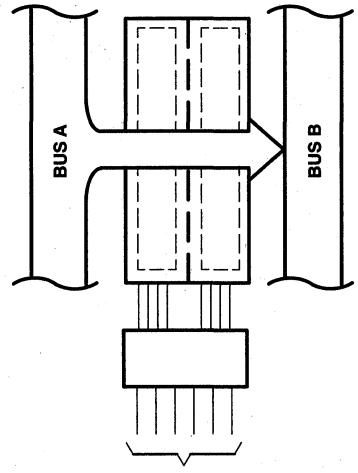


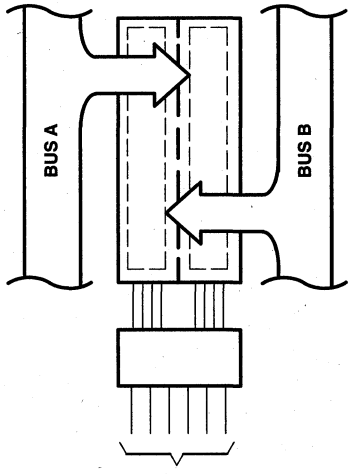
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



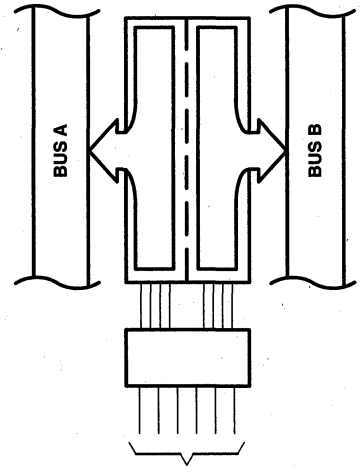
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

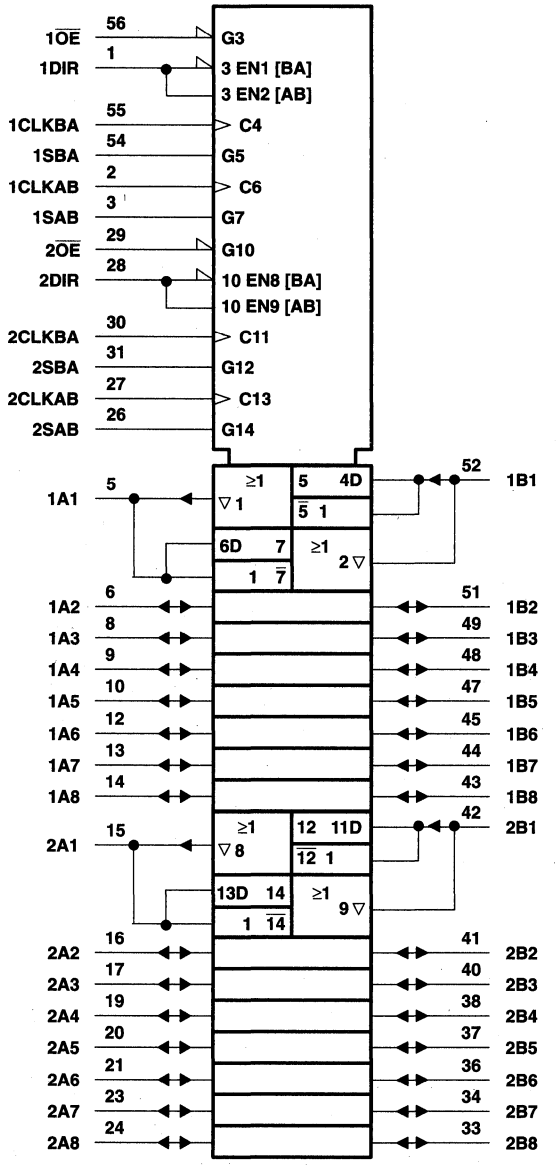


$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

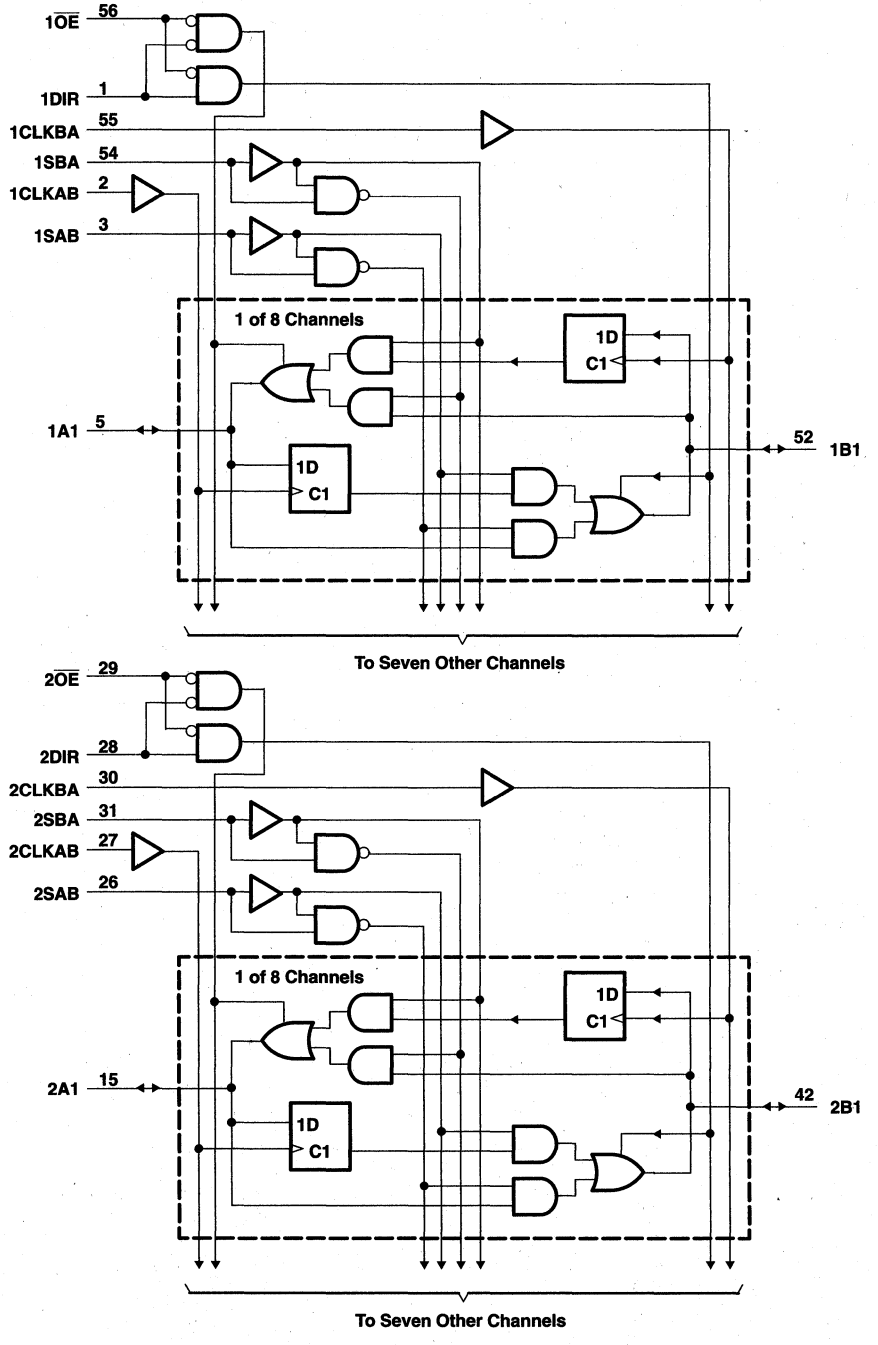
Figure 1. Bus-Management Functions

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16646 . . . . . 96 mA
SN74ABT16646 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Maximum power dissipation at T_A = 55°C (in still air) . . . . . 1 W
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16646		SN74ABT16646		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16646		SN74ABT16646		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±20		±20		±20	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					10		10		10	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–10		–10		–10	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			50		50		50	µA
			Outputs disabled			50		50		50	
		Control inputs				50		50		50	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

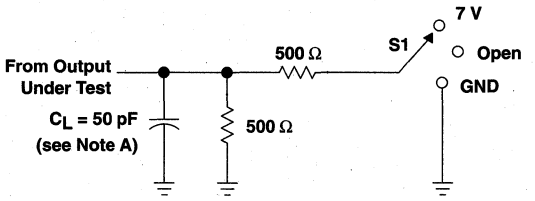
		V_{CC} = 5 V, T_A = 25°C		SN54ABT16646		SN74ABT16646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low	4.3		4.3		4.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3		4		3		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		0.5		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16646		SN74ABT16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.5	3.1	4	1	5	1.5	4.9	ns
t_{PHL}			1.5	3.2	4.1	1	5	1.5	4.7	
t_{PLH}	A or B	B or A	1	2.3	3.2	0.6	4	1	3.9	ns
t_{PHL}			1	3	4.1	0.6	4.9	1	4.6	
t_{PLH}	SAB or SBA†	B or A	1	2.9	4.3	0.6	5.3	1	5	ns
t_{PHL}			1	3.1	4.3	0.6	5.3	1	5	
t_{PZH}	$\overline{OE}$	A or B	1	3.4	4.6	0.6	5.9	1	5.5	ns
t_{PZL}			1.5	3.5	4.9	1	6	1.5	5.7	
t_{PHZ}	$\overline{OE}$	A or B	1.5	3.9	4.9	1	6.4	1.5	5.4	ns
t_{PLZ}			1.5	3.1	4.1	1	4.7	1.5	4.5	
t_{PZH}	DIR	A or B	1	3.2	4.5	0.6	5.8	1	5.4	ns
t_{PZL}			1.5	3.4	4.8	1	6.7	1.5	5.6	
t_{PHZ}	DIR	A or B	2	4.2	5.7	1.2	7.1	2	6.7	ns
t_{PLZ}			1.5	3.6	5.1	1	6.2	1.5	5.9	

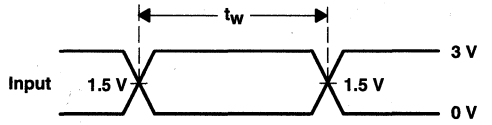
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

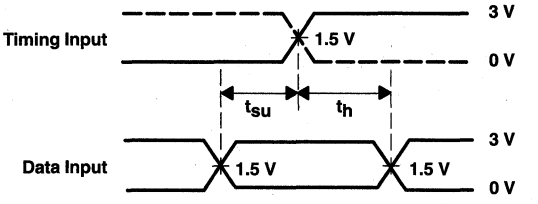


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

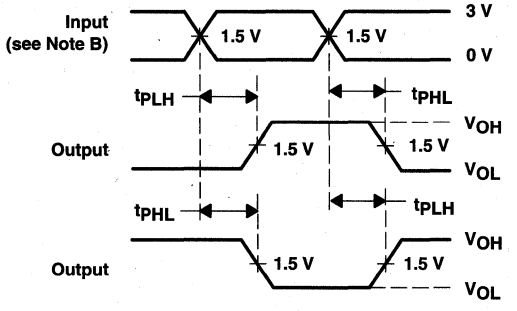
LOAD CIRCUIT FOR OUTPUTS



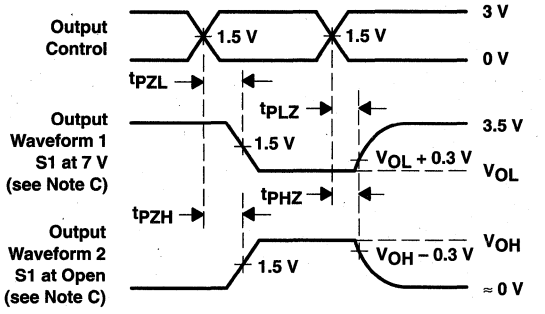
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



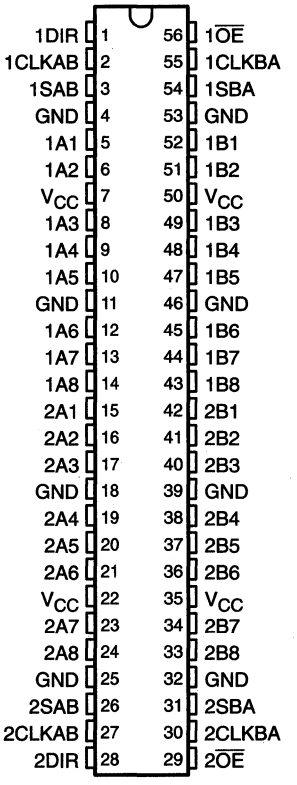
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16648 . . . WD PACKAGE
SN74ABT16648 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16648 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16648.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16648 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16648 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16648 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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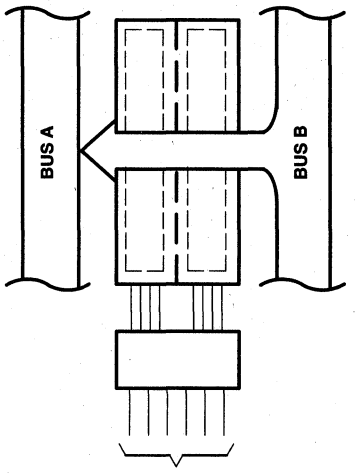
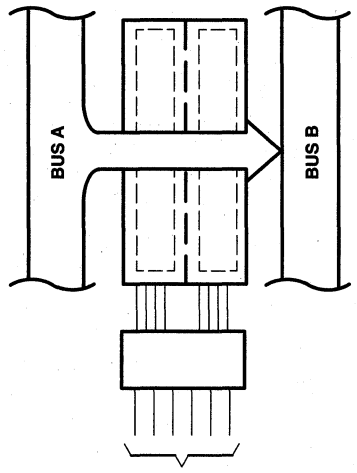


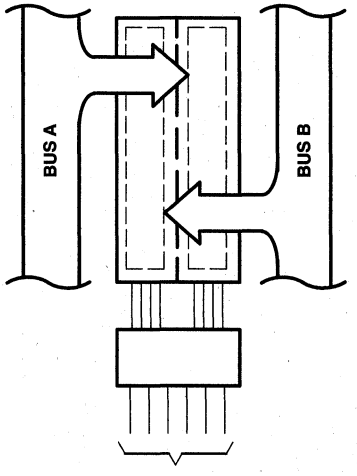
56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



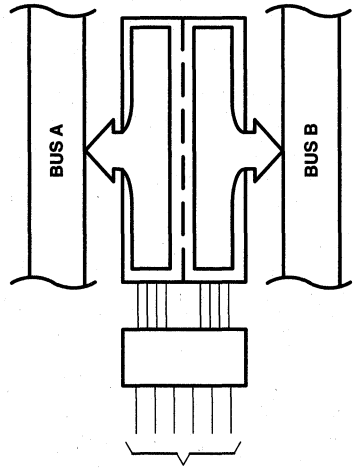
56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

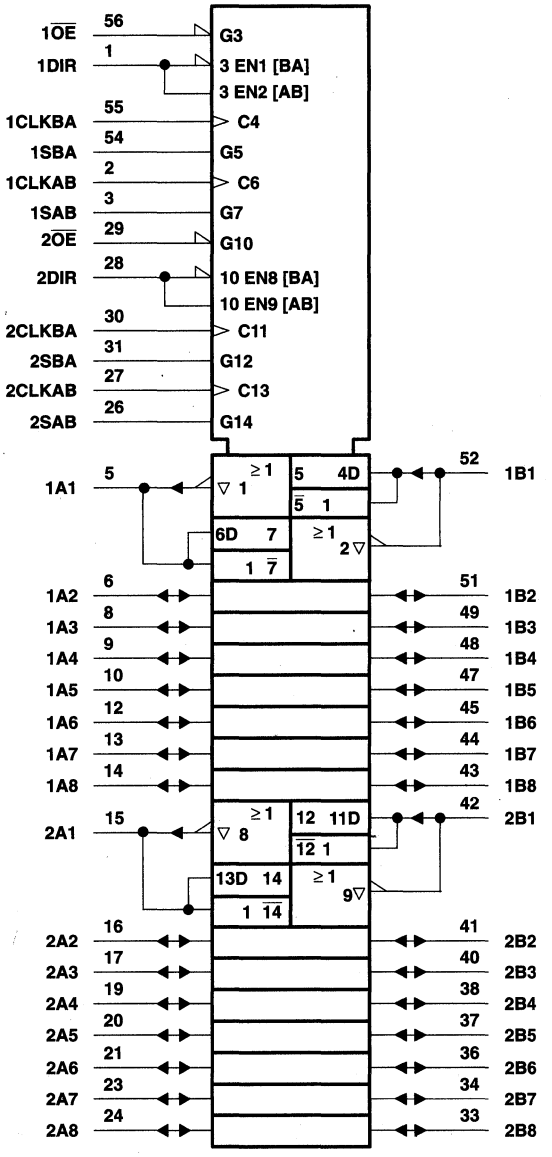


56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

logic symbol†

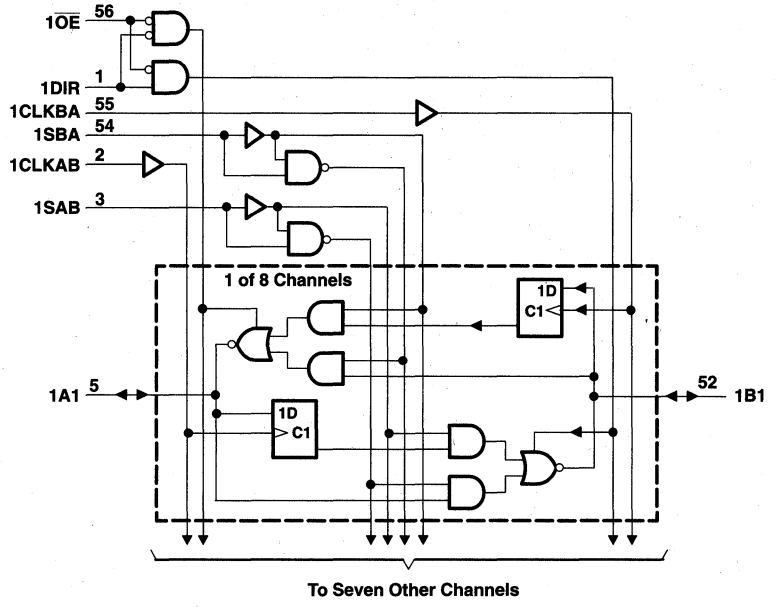


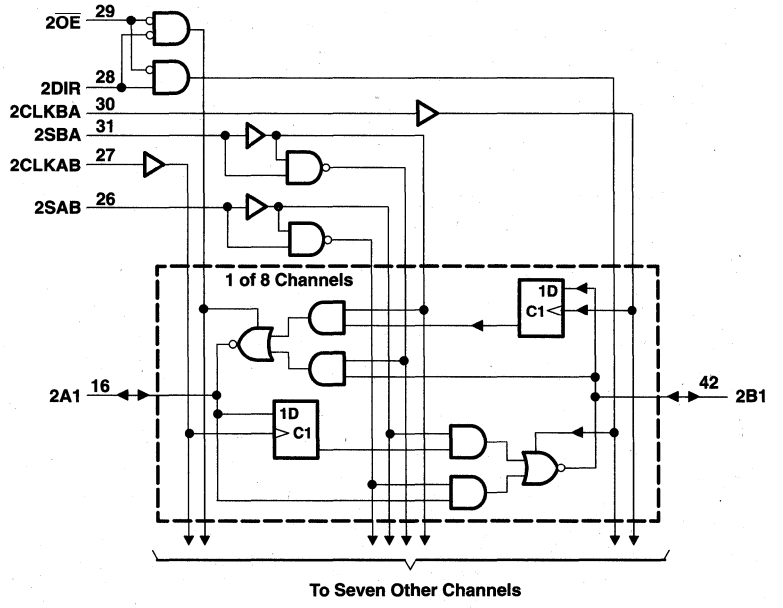
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram (positive logic)





FUNCTION TABLE
(each 8-bit section)

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
L	H	L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus

† The data output functions may be enabled or disabled by a variety of level combinations at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16648 . . . . . 96 mA
SN74ABT16648 . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . −18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) . . . . . 1 W
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16648		SN74ABT16648		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

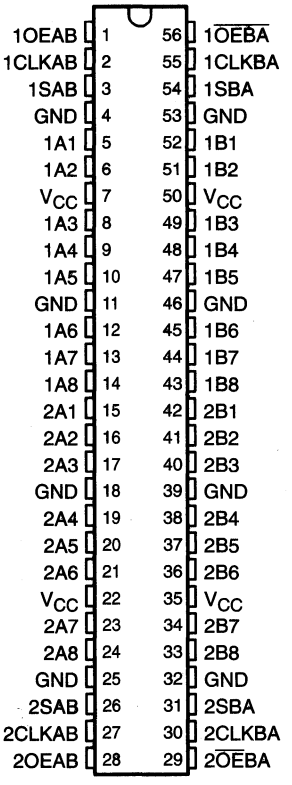
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16648		SN74ABT16648		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			72		72		30	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs								pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports								pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16651 . . . WD PACKAGE
SN74ABT16651 . . . DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'ABT16651 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16651.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

description (continued)

To ensure the high-impedance state during power up or power down, $\overline{OEBA}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

The SN74ABT16651 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16651 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT16651 is characterized for operation from −40°C to 85°C.

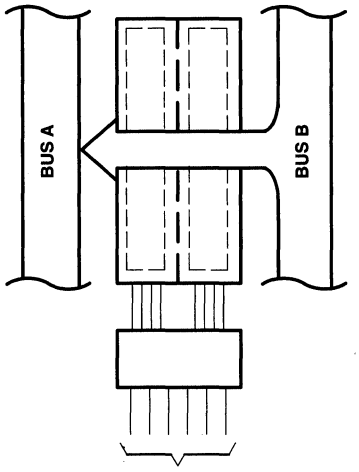
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Output	Stored $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

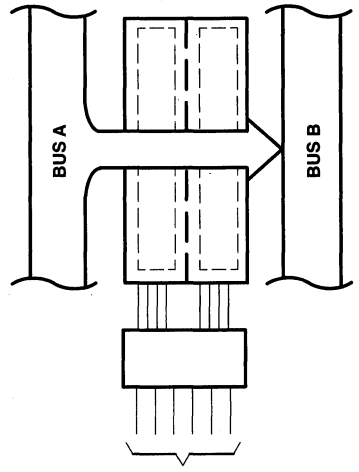
‡ When select control is low, clocks can occur simultaneously so long as allowances are made for propagation delays from A to B (B to A) plus setup and hold times. When select control is high, clocks must be staggered in order to load both registers.

PRODUCT PREVIEW



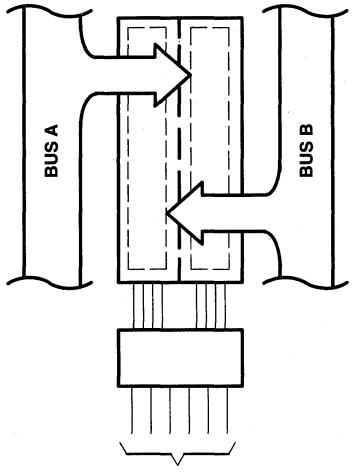
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



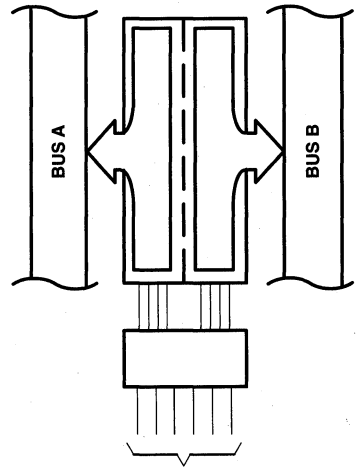
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

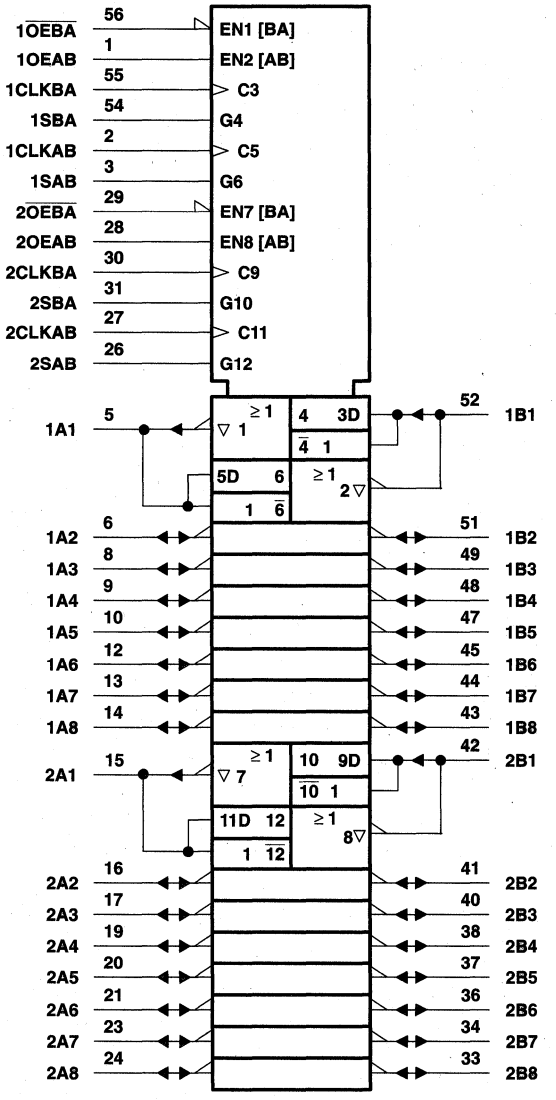
TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

PRODUCT PREVIEW

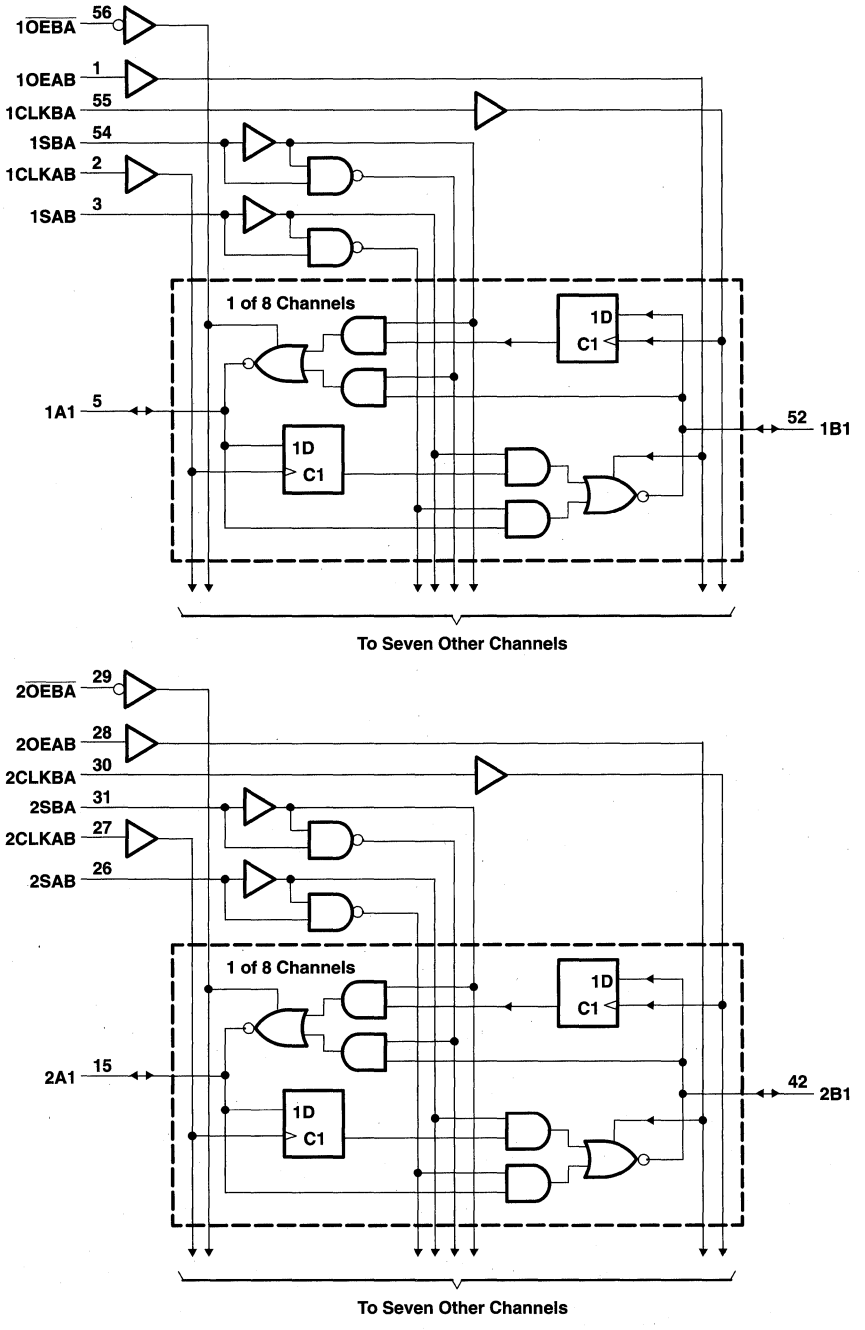
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16651 ..... 96 mA
SN74ABT16651 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16651		SN74ABT16651		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16651		SN74ABT16651		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			72		72		30	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs								pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports								pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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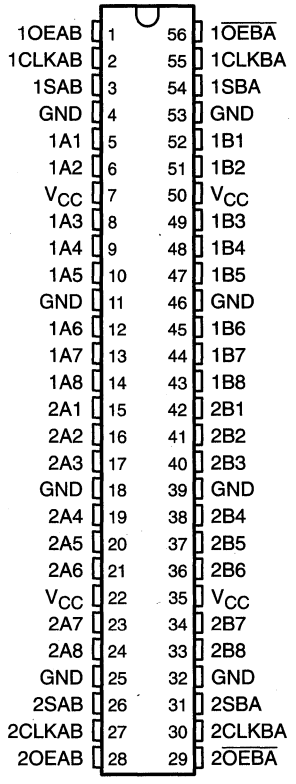
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16652 . . . WD PACKAGE
SN74ABT16652 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16652 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

The SN74ABT16652 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

description (continued)

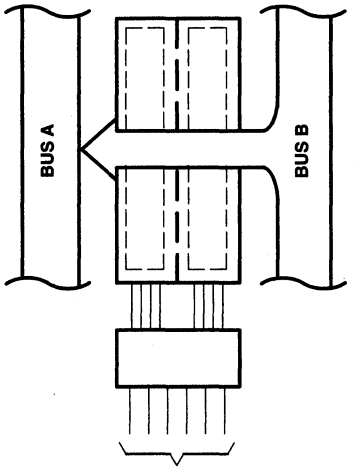
The SN54ABT16652 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT16652 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

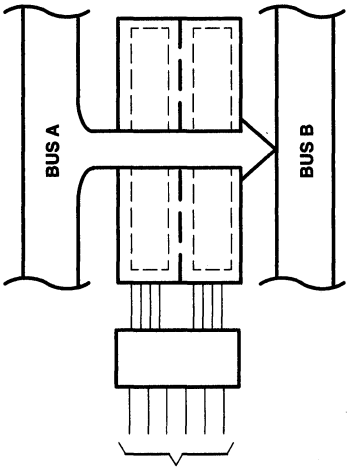
† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.



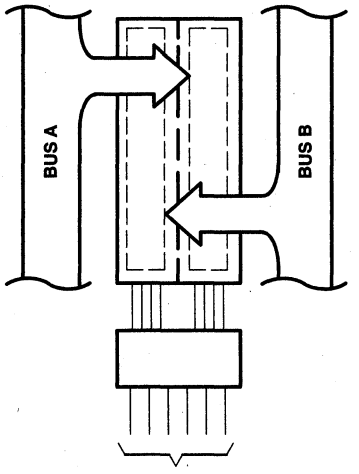
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



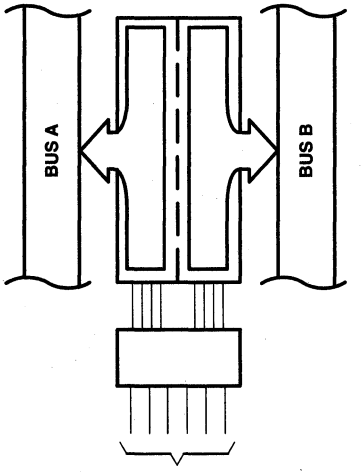
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

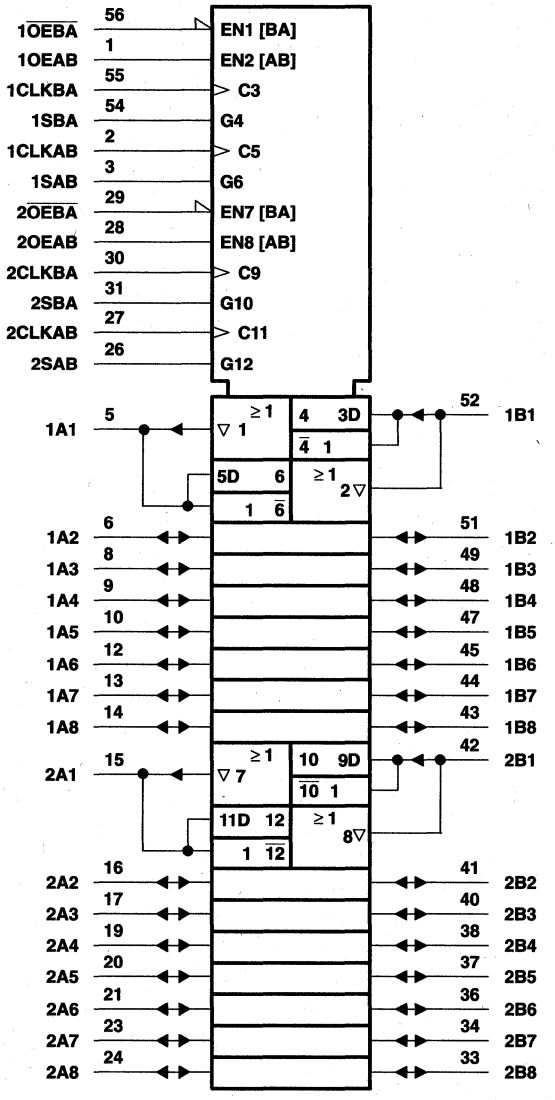


OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

TRANSFER STORED DATA
TO A AND/OR B

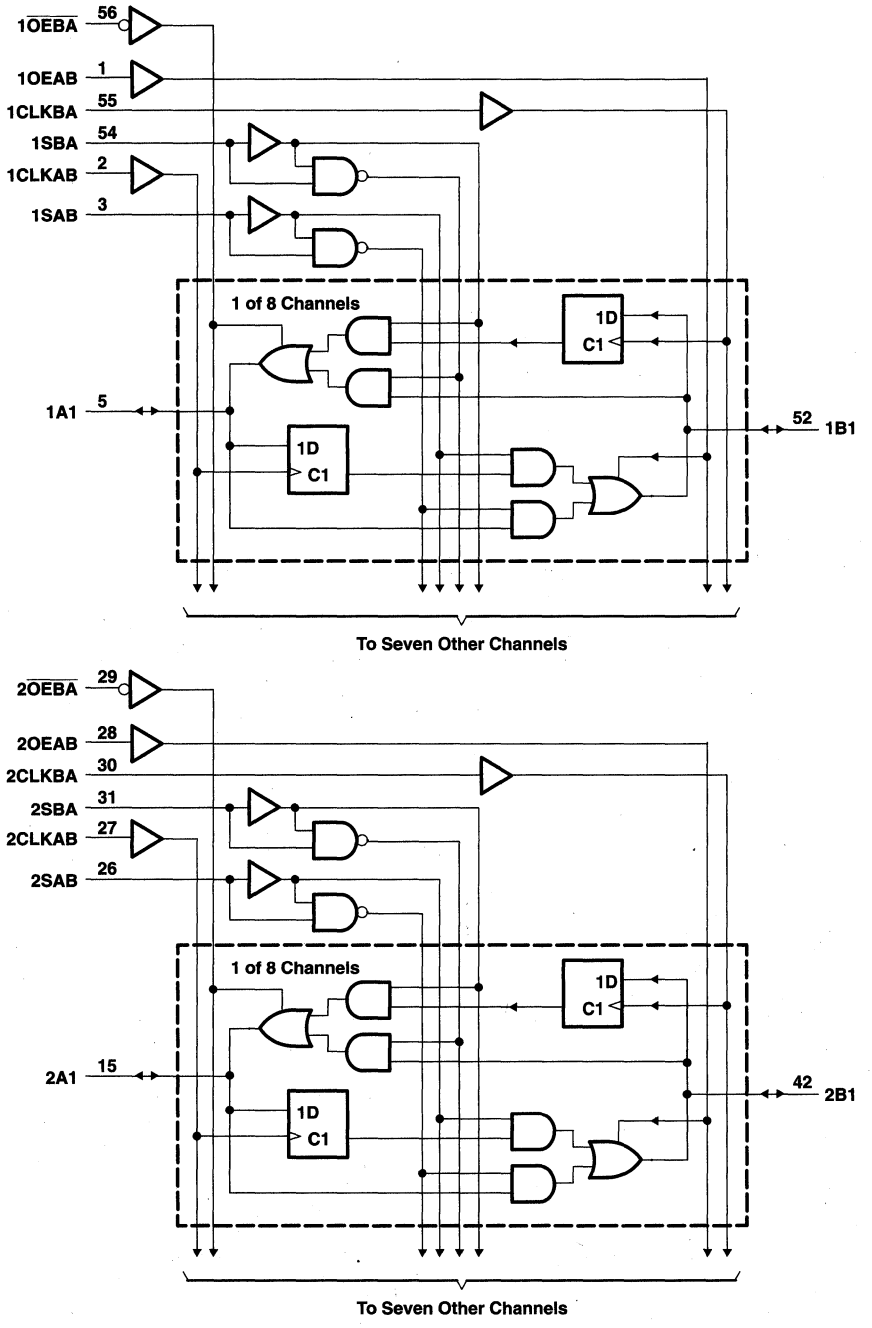
Figure 1. Bus-Management Functions

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16652 ..... 96 mA
SN74ABT16652 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16652		SN74ABT16652		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16652		SN74ABT16652		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±20		±20		±20	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				10		10		10	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−10		−10		−10	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			50		50		50	µA
			Outputs disabled			50		50		50	
		Control inputs				50		50		50	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

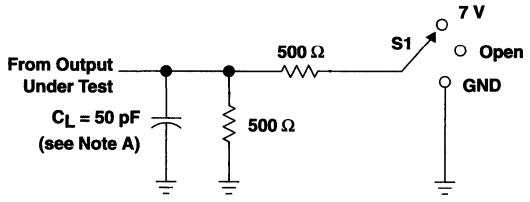
		V_{CC} = 5 V, T_A = 25°C		SN54ABT16652		SN74ABT16652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low	4.3		4.3		4.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3		4		3		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		0.5		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16652		SN74ABT16652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	CLK	B or A	1.5	3.1	4	1	5	1.5	4.9	ns
t_{PHL}			1.5	3.2	4.1	1	5	1.5	4.7	
t_{PLH}	A or B	B or A	1	2.3	3.2	0.6	4	1	3.9	ns
t_{PHL}			1	3	4.1	0.6	4.9	1	4.6	
t_{PLH}	SAB or SBA†	B or A	1	2.9	4.3	0.6	5.3	1	5	ns
t_{PHL}			1	3.1	4.3	0.6	5.3	1	5	
t_{PZH}	$\overline{OEBA}$	A	1	2.8	4.1	0.6	5.2	1	5	ns
t_{PZL}			1.5	3.1	4.4	1	5.4	1.5	5.3	
t_{PHZ}	$\overline{OEBA}$	A	1.5	3.4	4.4	0.8	5.3	1.5	4.9	ns
t_{PLZ}			1.5	2.7	3.6	1	5.3	1.5	4	
t_{PZH}	OEAB	B	1	2.6	3.6	0.8	4.7	1	4.2	ns
t_{PZL}			1.5	2.8	3.9	1	5	1.5	4.6	
t_{PHZ}	OEAB	B	2	4.2	5.5	1	6.4	2	5.9	ns
t_{PLZ}			1.5	3.4	4.5	1	5.9	1.5	5.2	

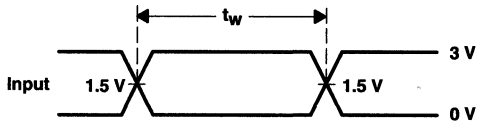
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

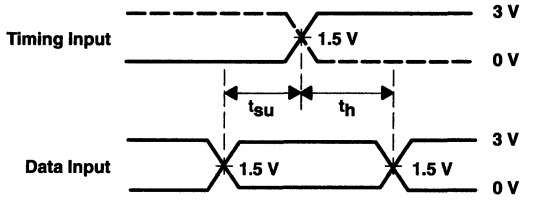


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

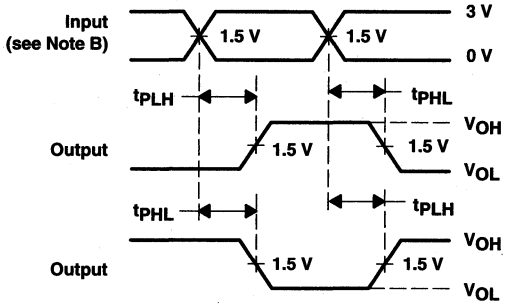
LOAD CIRCUIT FOR OUTPUTS



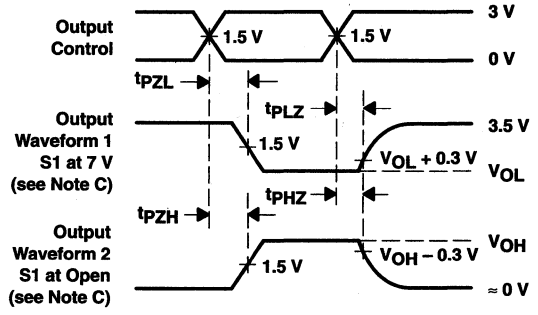
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



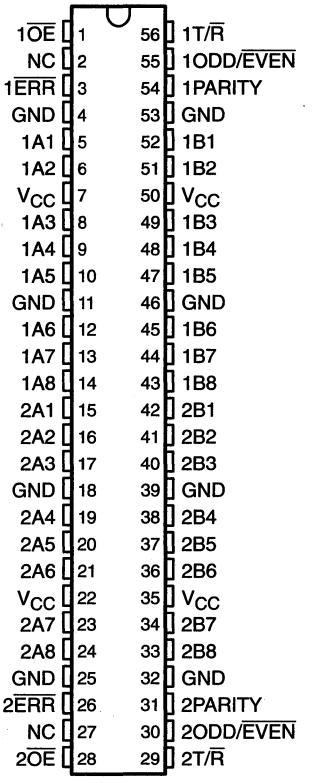
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16657 . . . WD PACKAGE
SN74ABT16657 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16657 contains two noninverting octal transceiver sections with separate parity generator/checker circuits and control signals. For either section, the transmit/receive (1T/$\overline{R}$ or 2T/$\overline{R}$) input determines the direction of data flow. When 1T/$\overline{R}$ (or 2T/$\overline{R}$) is high, data flows from the 1A (or 2A) port to the 1B (or 2B) port (transmit mode); when 1T/$\overline{R}$ (or 2T/$\overline{R}$) is low, data flows from the 1B (or 2B) port to the 1A (or 2A) port (receive mode). When the output-enable (1$\overline{OE}$ or 2$\overline{OE}$) input is high, both the 1A (or 2A) and 1B (or 2B) ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the 1ODD/$\overline{EVEN}$ (or 2ODD/$\overline{EVEN}$) input. 1PARITY (or 2PARITY) carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the 1A (or 2A) bus is polled to determine the number of high bits, 1PARITY (or 2PARITY) is set to the logic level that maintains the parity sense selected by the level at the 1ODD/$\overline{EVEN}$ (or 2ODD/$\overline{EVEN}$) input. For example, if 1ODD/$\overline{EVEN}$ is low (even parity selected) and there are five high bits on the 1A bus, then 1PARITY is set to the logic high level so that an even number of the nine total bits (eight 1A-bus bits plus parity bit) are high.

In the receive mode, after the 1B (or 2B) bus is polled to determine the number of high bits, the 1$\overline{ERR}$ (or 2$\overline{ERR}$) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if 1ODD/$\overline{EVEN}$ is high (odd parity selected), 1PARITY is high, and there are three high bits on the 1B bus, then 1$\overline{ERR}$ is low, indicating a parity error.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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description (continued)

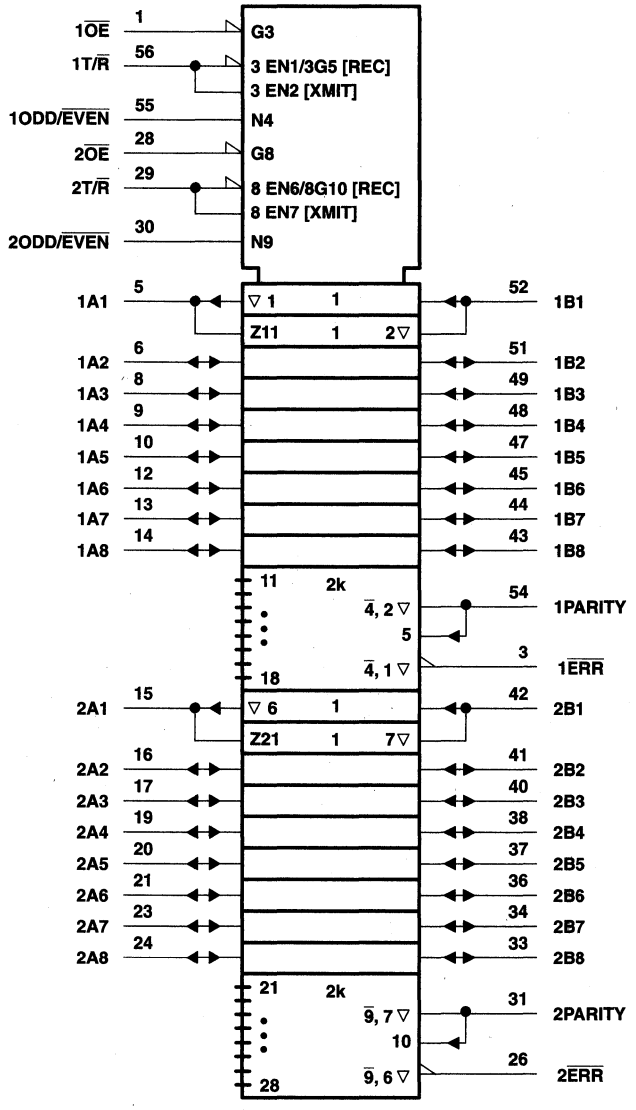
The SN74ABT16657 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16657 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT16657 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

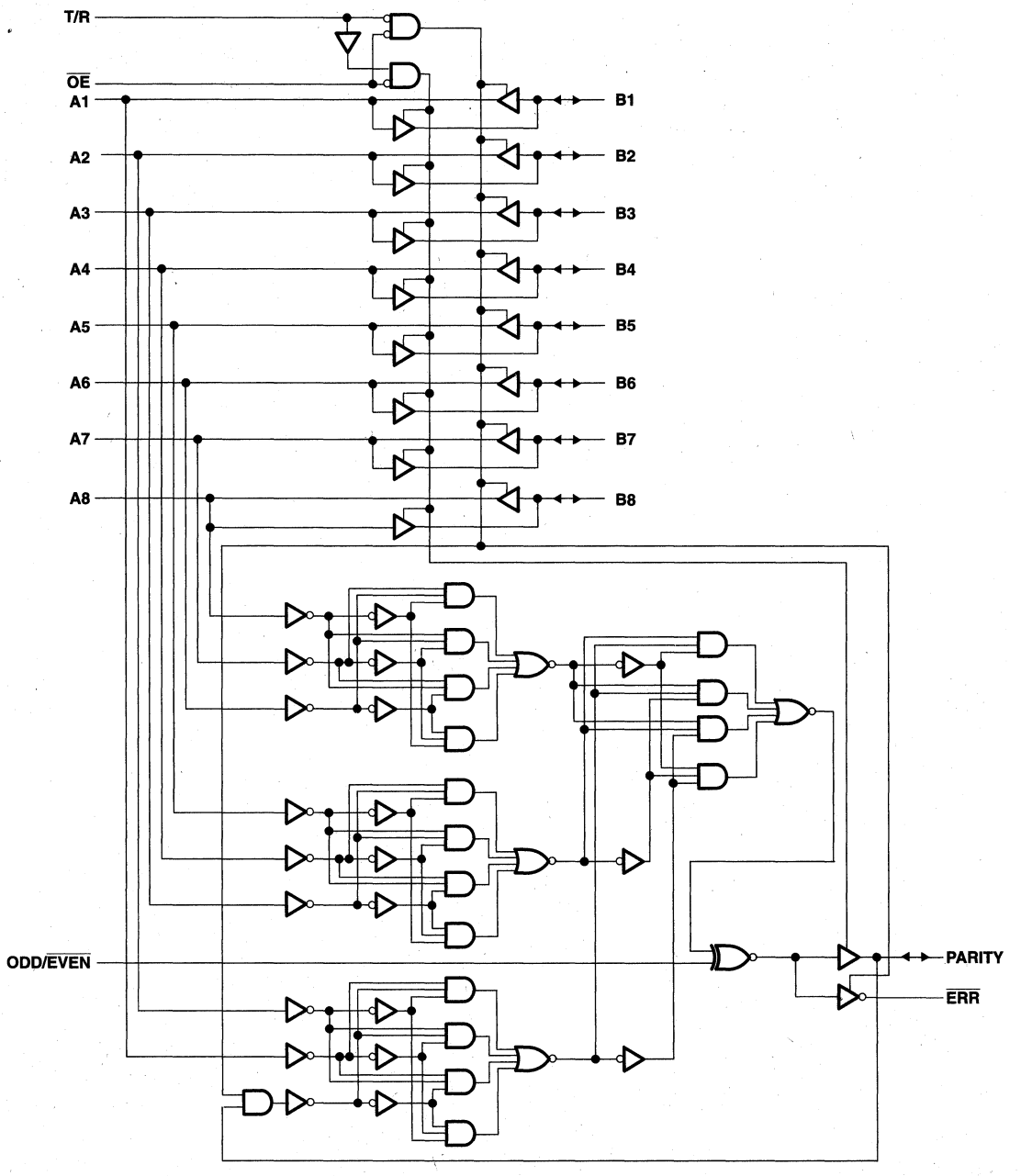
NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$		$\overline{ERR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each transceiver (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16657 ..... 96 mA
SN74ABT16657 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16657		SN74ABT16657		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

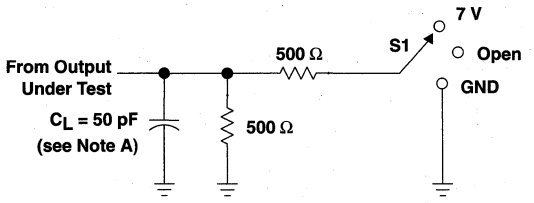
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16657		SN74ABT16657		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5				V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = –24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = –32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 24 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			36		36		36	
			Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		9						pF

† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

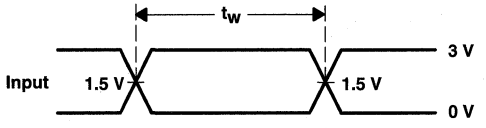
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16657		SN74ABT16657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
t_{PHL}			2	3.1	3.9	2	4.5	2	4.3	
t_{PLH}	A	PARITY	2	4.6	5.4	2	7	2	6.7	ns
t_{PHL}			2	4.3	5.1	2	6.5	2	6.1	
t_{PLH}	ODD/$\overline{\text{EVEN}}$	PARITY, $\overline{\text{ERR}}$	2	4.6	5.4	2	7	2	6.7	ns
t_{PHL}			2	4.3	5.1	2	6.5	2	6.1	
t_{PLH}	B	$\overline{\text{ERR}}$	2	4.6	5.4	2	7	2	6.7	ns
t_{PHL}			2	4.3	5.1	2	6.5	2	6.1	
t_{PLH}	PARITY	$\overline{\text{ERR}}$	2	4.6	5.4	2	7	2	6.7	ns
t_{PHL}			2	4.3	5.1	2	6.5	2	6.1	
t_{PZH}	$\overline{\text{OE}}$	A or B	2	3.9	4.9	2	5.8	2	5.6	ns
t_{PZL}			2.5	4.3	5.1	2.5	6.2	2.5	6	
t_{PHZ}	$\overline{\text{OE}}$	A or B	2	3.6	4.5	2	5.5	2	5.4	ns
t_{PLZ}			1.5	3	3.8	1.5	4.7	1.5	4.3	
t_{PZH}	$\overline{\text{OE}}$	PARITY, $\overline{\text{ERR}}$	2	4	4.9	2	5.8	2	5.6	ns
t_{PZL}			2.5	4.1	5.1	2.5	6.2	2.5	6	
t_{PHZ}	$\overline{\text{OE}}$	PARITY, $\overline{\text{ERR}}$	1	3.5	4.5	1	5.5	1	5.4	ns
t_{PLZ}			1.5	3	3.8	1.5	4.7	1.5	4.3	

PARAMETER MEASUREMENT INFORMATION

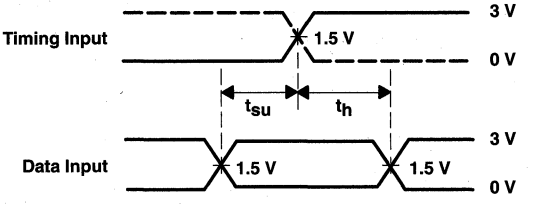


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

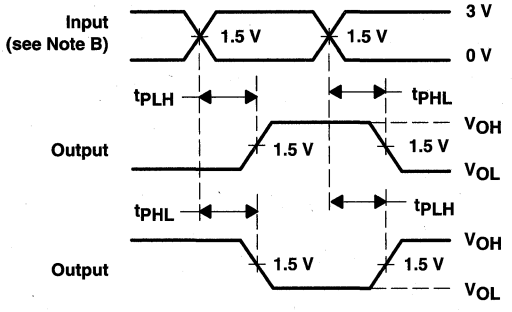
LOAD CIRCUIT FOR OUTPUTS



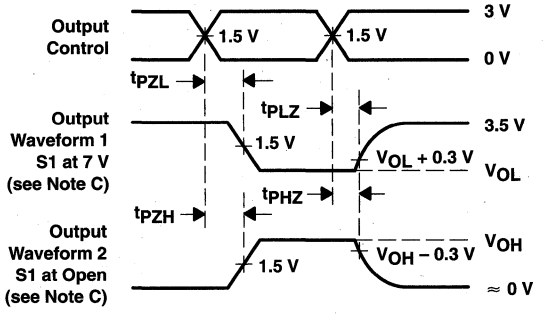
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



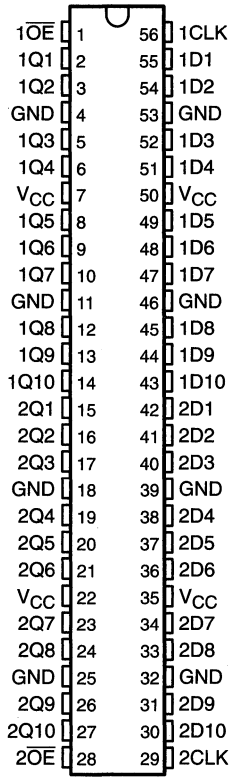
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16821 . . . WD PACKAGE
SN74ABT16821 . . . DL PACKAGE
(TOP VIEW)



description

These 20-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT16821 can be used as two 10-bit flip-flops or one 20-bit flip-flop. The twenty flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16821 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16821 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16821 is characterized for operation from –40°C to 85°C.

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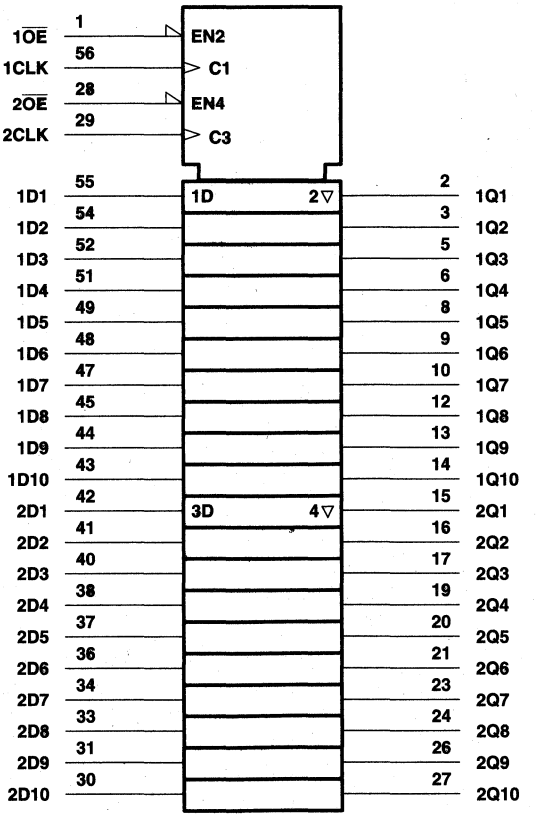
FUNCTION TABLE
(each flip-flop)

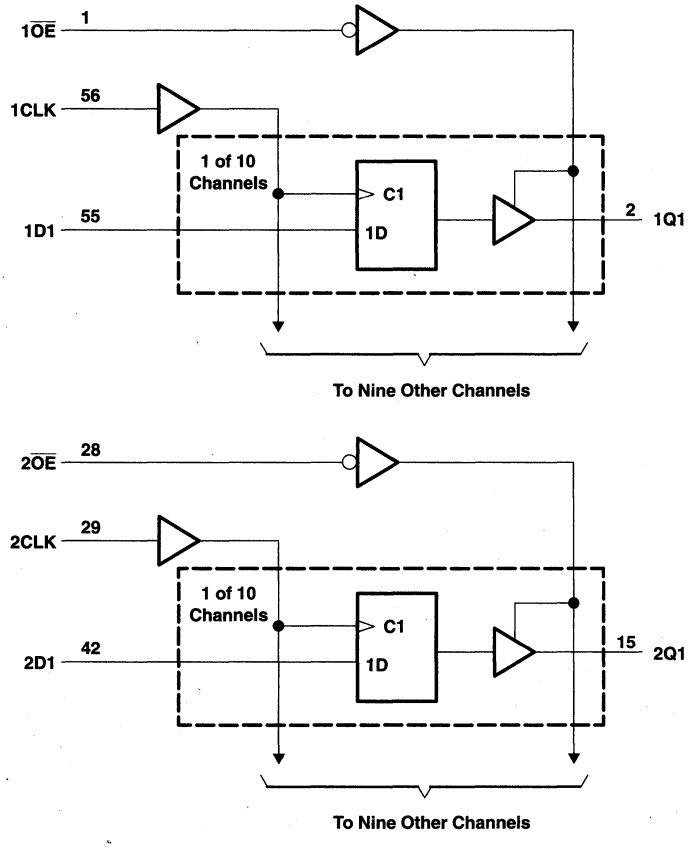
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16821	96 mA
SN74ABT16821	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air)	1 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16821		SN74ABT16821		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16821		SN74ABT16821		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			500		500		500	µA
		Outputs low			89		89		89	mA
		Outputs disabled			500		500		500	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3.5						pF
C_o	V_O = 2.5 V or 0.5 V			7.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

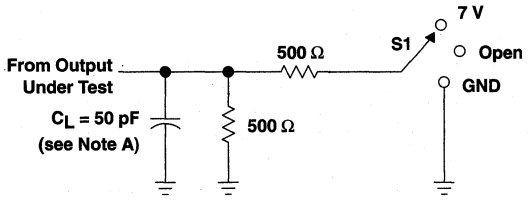
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V_{CC} = 5 V, T_A = 25°C		SN54ABT16821		SN74ABT16821		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	1.8		1.8		1.8		ns
t_h	Hold time, data after CLK↑	1.3		1.3		1.3		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

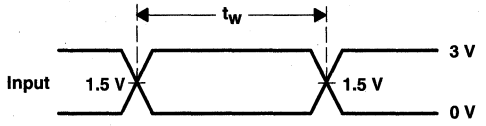
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16821		SN74ABT16821		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLK	Q	1.3	3.7	5.1	1.3	6.7	1.3	6.1	ns
t_{PHL}			1.6	3.9	5.1	1.6	5.8	1.6	5.4	
t_{PZH}	$\overline{OE}$	Q	1.1	3.2	4.7	1.1	5.8	1.1	5.7	ns
t_{PZL}			1.6	3.8	5	1.6	5.7	1.6	5.6	
t_{PHZ}	$\overline{OE}$	Q	2	4.5	5.7	2	6.6	2	6.5	ns
t_{PLZ}			1.8	4.1	5.8	1.8	8.4	1.8	7.1	

PARAMETER MEASUREMENT INFORMATION

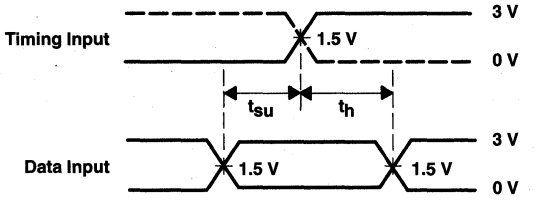


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

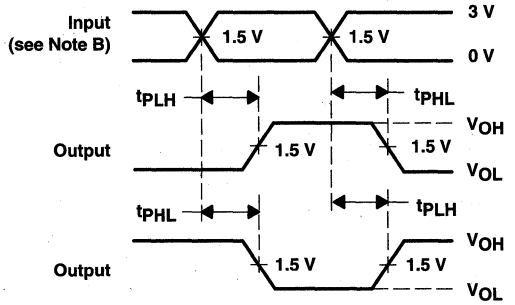
LOAD CIRCUIT FOR OUTPUTS



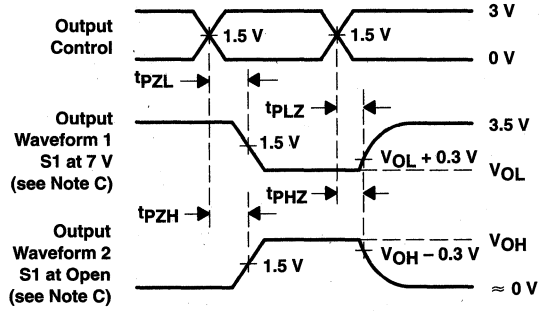
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
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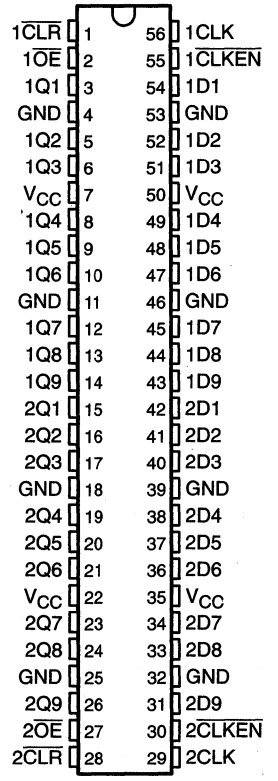
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16823 . . . WD PACKAGE
SN74ABT16823 . . . DL PACKAGE
(TOP VIEW)



description

These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{CLKEN}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{CLR}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

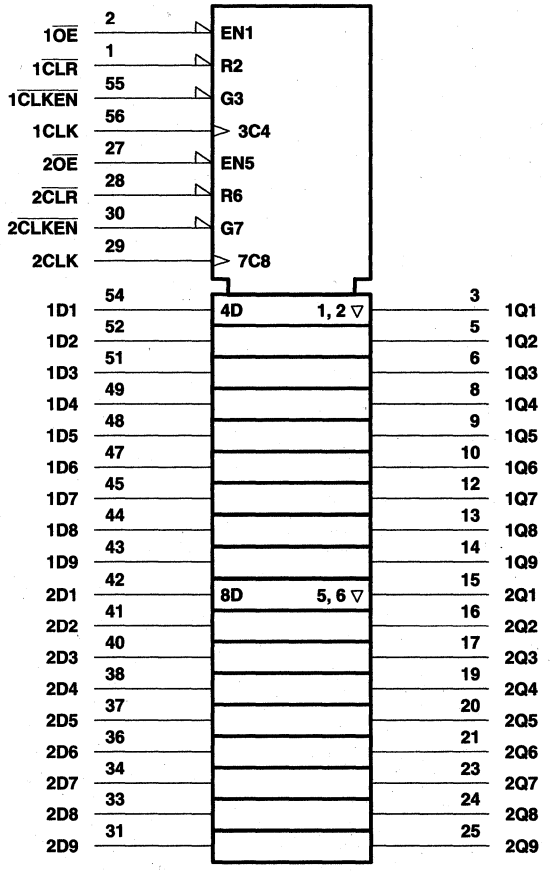
The SN74ABT16823 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16823 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16823 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit stage)

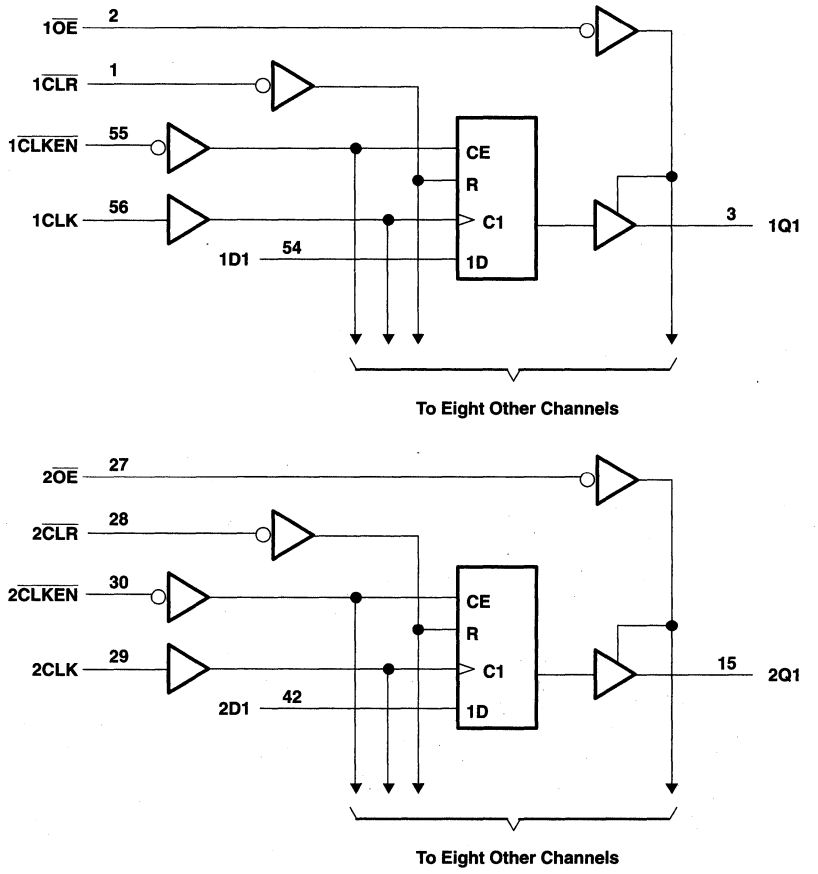
INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16823	96 mA
SN74ABT16823	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air)	1 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16823		SN74ABT16823		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16823		SN74ABT16823		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.5		0.5		0.5	mA
		Outputs low			80		80		80	
		Outputs disabled			0.5		0.5		0.5	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3.5						pF
C_o	V_O = 2.5 V or 0.5 V			7.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

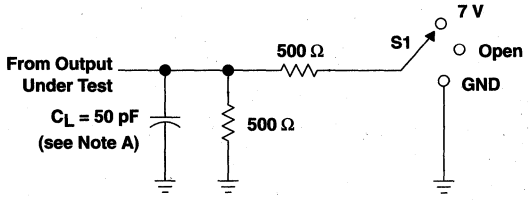
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT16823		SN74ABT16823		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	1.6		2		1.6		ns
		Data	1.7		1.7		1.7		
		$\overline{CLKEN}$ low	2.8		2.8		2.8		
t_h	Hold time after CLK↑	Data	1.2		1.2		1.2		ns
		$\overline{CLKEN}$ low	0.6		0.6		0.6		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

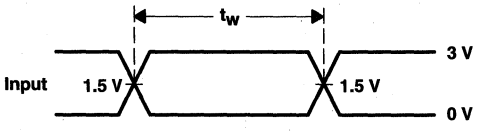
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16823		SN74ABT16823		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLK	Q	1.6	3.9	5.5	1.6	7.7	1.6	6.8	ns
t_{PHL}			2.1	3.9	5.4	2.1	6.4	2.1	6	
t_{PHL}	$\overline{CLR}$	Q	1.9	4.1	5.3	1.9	6.3	1.9	6.1	ns
t_{PZH}	$\overline{OE}$	Q	1	3.1	4.2	1	5.1	1	4.9	ns
t_{PZL}			1.5	3.5	4.6	1.5	5.7	1.5	5.5	
t_{PHZ}	$\overline{OE}$	Q	2.2	4.3	5.6	2.2	6.8	2.2	6.1	ns
t_{PLZ}			1.6	4.3	6.4	1.6	9.9	1.6	8.7	

PARAMETER MEASUREMENT INFORMATION

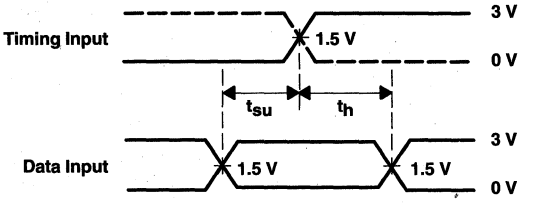


LOAD CIRCUIT FOR OUTPUTS

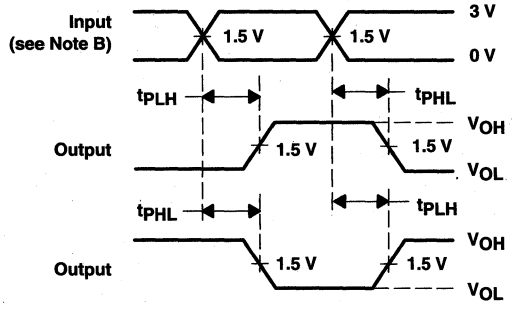
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



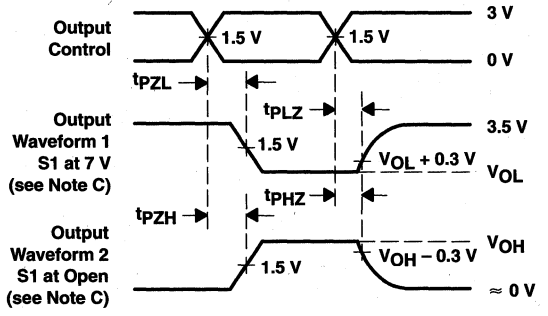
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
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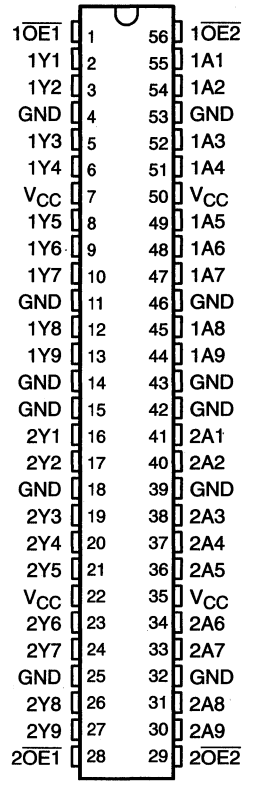
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16825 . . . WD PACKAGE
SN74ABT16825 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16825 is an 18-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all nine affected outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16825 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16825 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16825 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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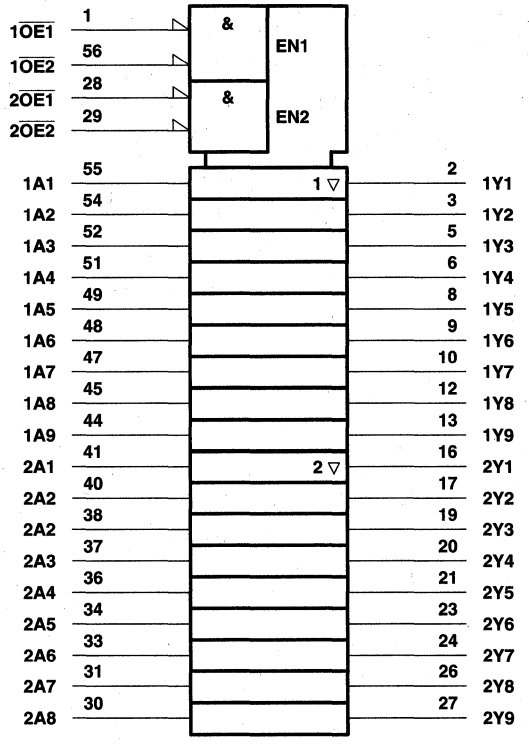
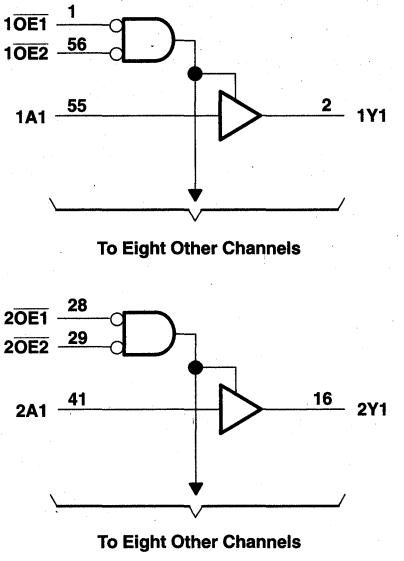
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16825 ..... 96 mA
SN74ABT16825 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... –50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16825		SN74ABT16825		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Control pins		4		4	ns/V
		Data pins		10		10	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

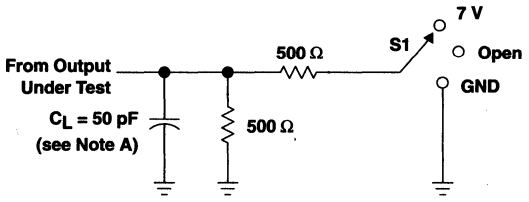
PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16825		SN74ABT16825		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			2		2		2	mA
		Outputs low			32		32		32	
		Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V									pF
C_o	V_O = 2.5 V or 0.5 V									pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

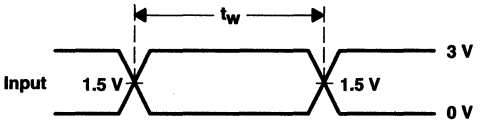
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16825		SN74ABT16825		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	1.9	3.6	1	4.1	1	3.9	ns
t_{PHL}			1	2.1	3.9	1	4.7	1	4.4	
t_{PZH}	$\overline{OE}$	Y	1	2.8	5.5	1	6.4	1	6.1	ns
t_{PZL}			1	2.8	5.4	1	6.3	1	6	
t_{PHZ}	$\overline{OE}$	Y	2.4	4.5	6.8	2.4	7.1	2.4	6.9	ns
t_{PLZ}			1.6	3.7	6.2	1.6	7.6	1.6	6.6	

PARAMETER MEASUREMENT INFORMATION

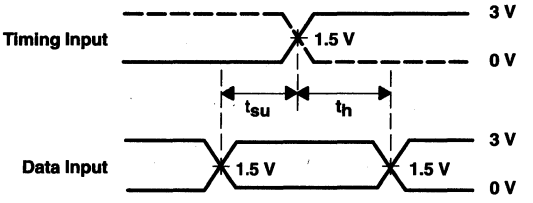


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

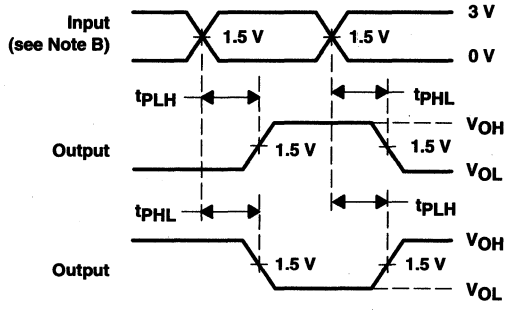
LOAD CIRCUIT FOR OUTPUTS



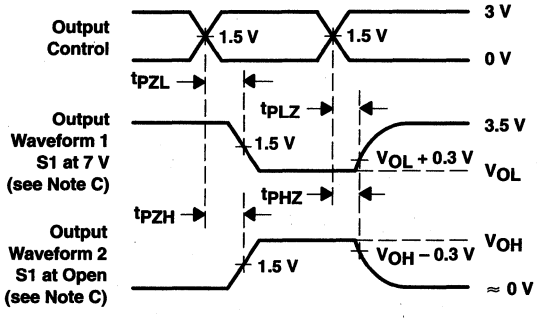
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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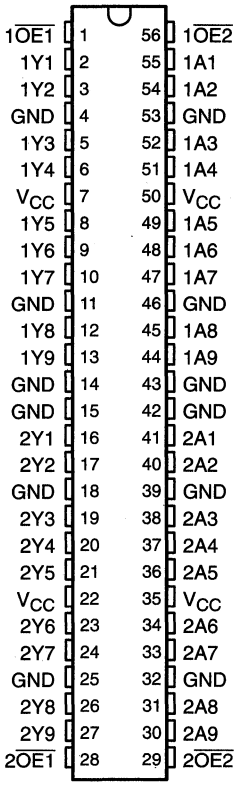
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16826 . . . WD PACKAGE
SN74ABT16826 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16826 is an 18-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all nine affected outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16826 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16826 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16826 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit section)

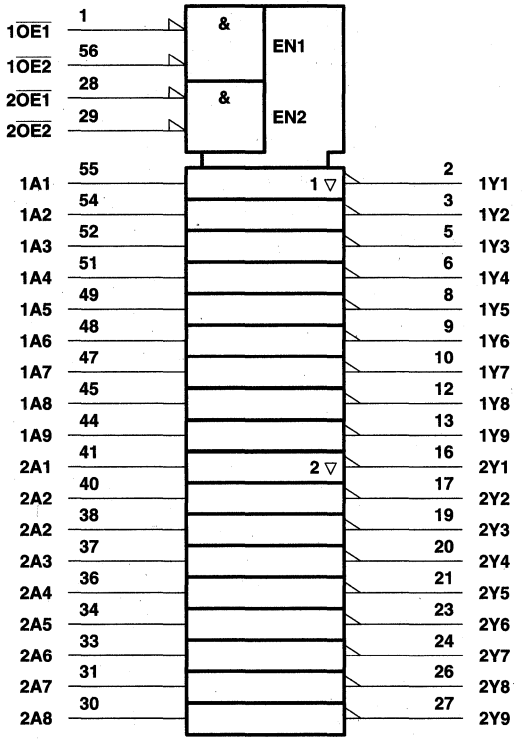
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW

logic symbol†



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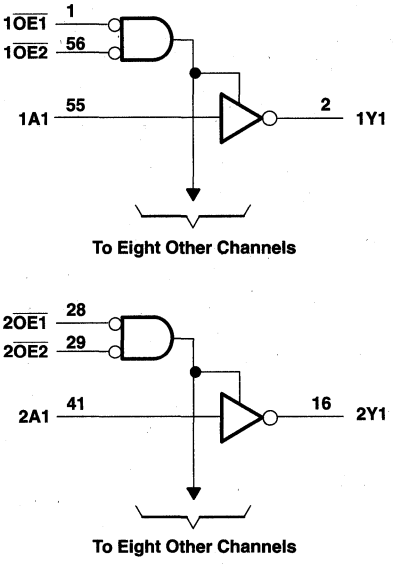
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16826 ..... 96 mA
SN74ABT16826 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16826		SN74ABT16826		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16826		SN74ABT16826		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			2		2		2	mA
		Outputs low			32		32		32	
		Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V									pF
C_o	V_O = 2.5 V or 0.5 V									pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
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SN54ABT16827 . . . WD PACKAGE
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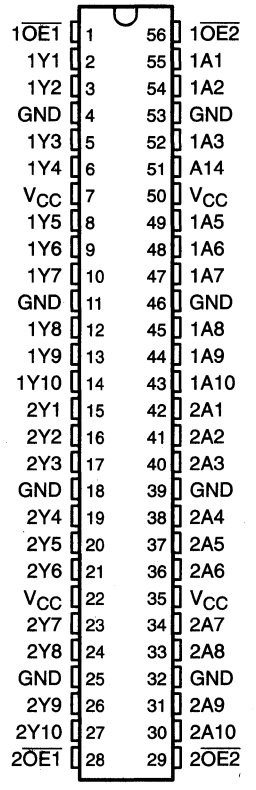
(TOP VIEW)



description

The 'ABT16827 is a noninverting 20-bit buffer composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16827 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16827 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16827 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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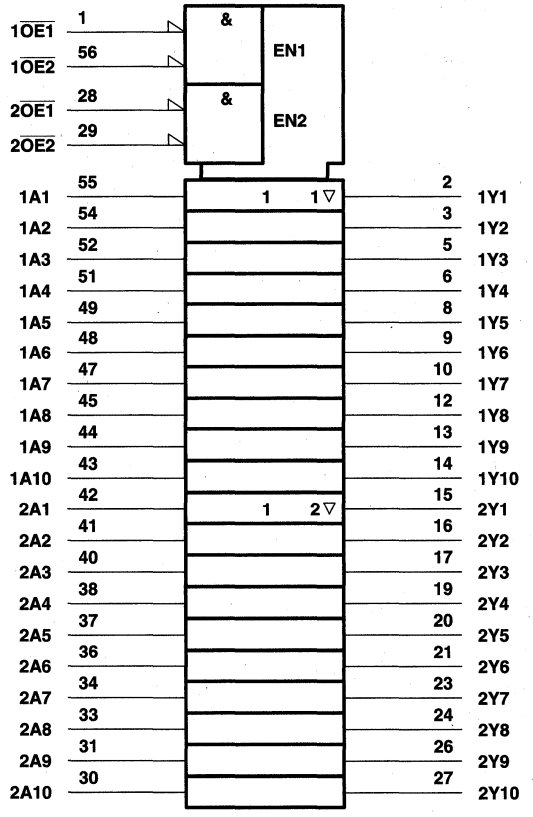
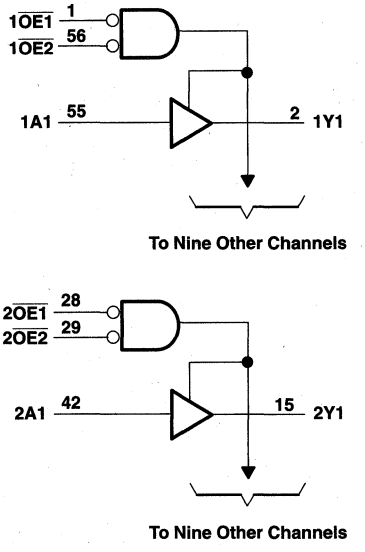
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16827 ..... 96 mA
SN74ABT16827 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16827		SN74ABT16827		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Control pins		4		4	ns/V
		Data pins		10		10	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

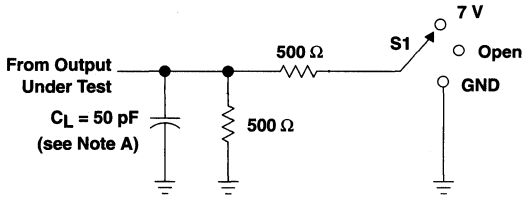
PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16827		SN74ABT16827		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			2		2		2	mA
		Outputs low			32		32		32	
		Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			7.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

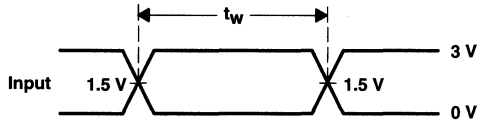
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16827		SN74ABT16827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	1.9	3.1	1	3.6	1	3.4	ns
t_{PHL}			1	2.1	3.7	1	4.5	1	4.2	
t_{PZH}	$\overline{OE}$	Y	1	2.8	5	1	5.9	1	5.6	ns
t_{PZL}			1	2.8	4.9	1	5.8	1	5.5	
t_{PHZ}	$\overline{OE}$	Y	2.4	4.5	6.5	2.4	6.8	2.4	6.6	ns
t_{PLZ}			1.6	3.7	5.7	1.6	7.1	1.6	6.1	

PARAMETER MEASUREMENT INFORMATION

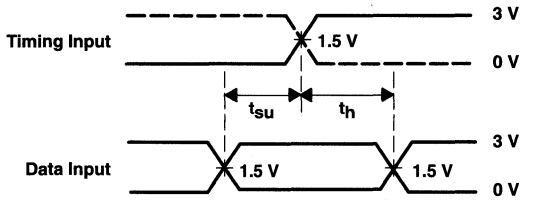


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

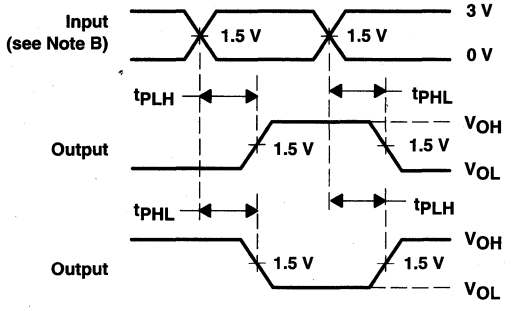
LOAD CIRCUIT FOR OUTPUTS



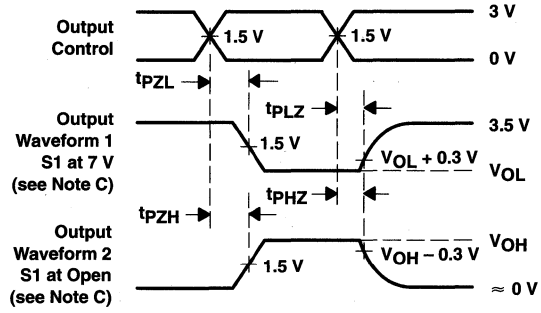
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



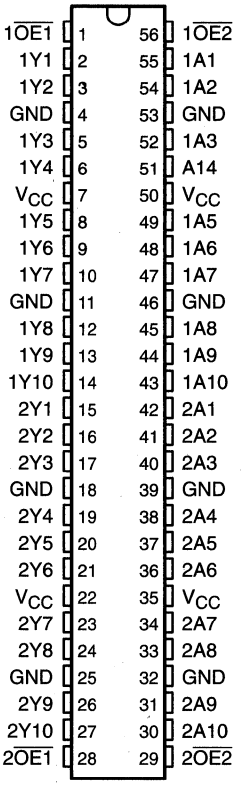
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (−32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16828 . . . WD PACKAGE
SN74ABT16828 . . . DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'ABT16828 is an inverting 20-bit buffer composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (1$\overline{OE1}$ and 1$\overline{OE2}$ or 2$\overline{OE1}$ and 2$\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16828 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16828 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT16828 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

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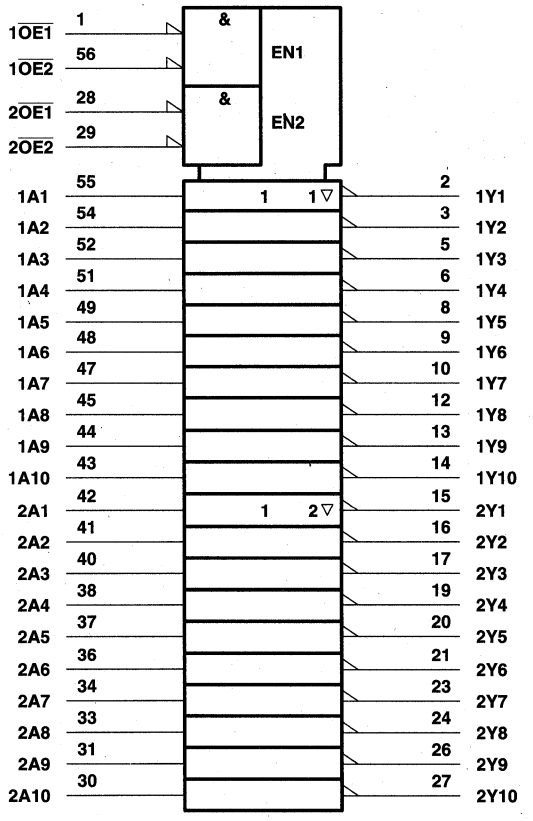
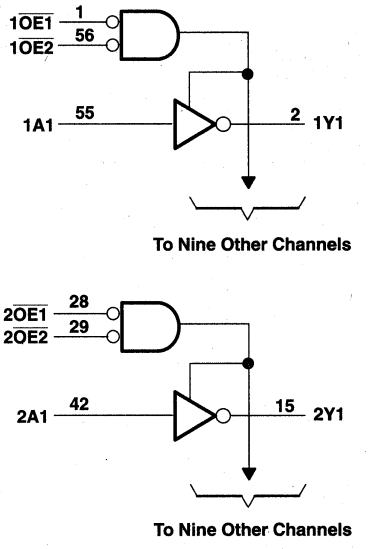
PRODUCT PREVIEW

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16828	96 mA
SN74ABT16828	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air)	1 W
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16828		SN74ABT16828		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16828		SN74ABT16828		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			2		2		2	mA
		Outputs low			32		32		32	
		Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V									pF
C_o	V_O = 2.5 V or 0.5 V									pF

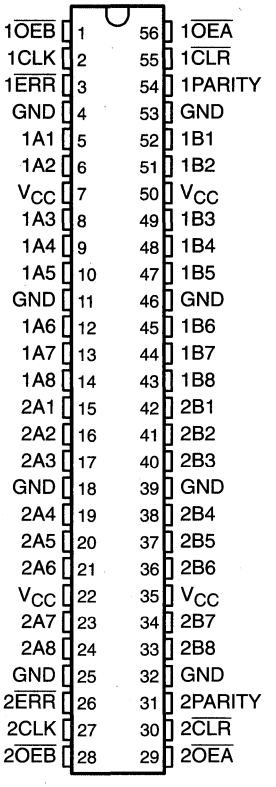
† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

SCBS097A – D3982, FEBRUARY 1991 – REVISED OCTOBER 1992

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Parity Error Flag With Parity Generator/Checker**
- **Register for Storage of the Parity Error Flag**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16833 . . . WD PACKAGE
SN74ABT16833 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16833 consists of two noninverting 8-bit to 9-bit parity bus transceivers and is designed for communication between data buses. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error (1$\overline{\text{ERR}}$ or 2$\overline{\text{ERR}}$) output is configured as an open-collector output. The B-to-A parity error flag is clocked into 1$\overline{\text{ERR}}$ (or 2$\overline{\text{ERR}}$) on the low-to-high transition of the clock (1CLK or 2CLK) input. 1$\overline{\text{ERR}}$ (or 2$\overline{\text{ERR}}$) is cleared (set high) by taking the clear (1$\overline{\text{CLR}}$ or 2$\overline{\text{CLR}}$) input low.

The output-enable ($\overline{\text{OEA}}$ and $\overline{\text{OEB}}$) inputs can be used to disable the device so that the buses are effectively isolated. When both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16833 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16833 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16833 is characterized for operation from –40°C to 85°C.

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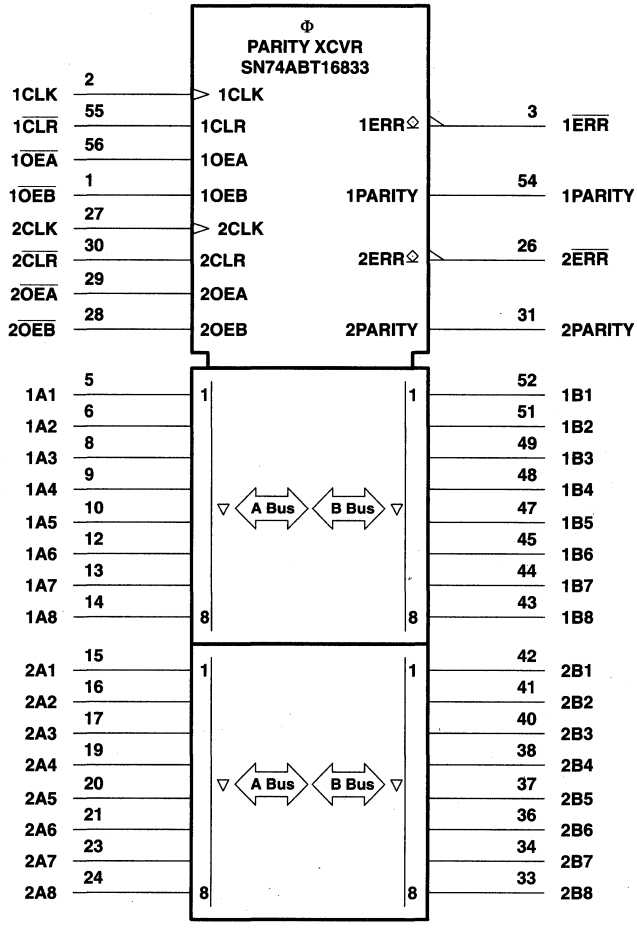
FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ OF H's	Bi† Σ OF H's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	H	No↑	X	X	Z	Z	Z	NC	Isolation§
		L	No↑	X					H	
		H	↑	Odd					H	
		H	↑	Even					L	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

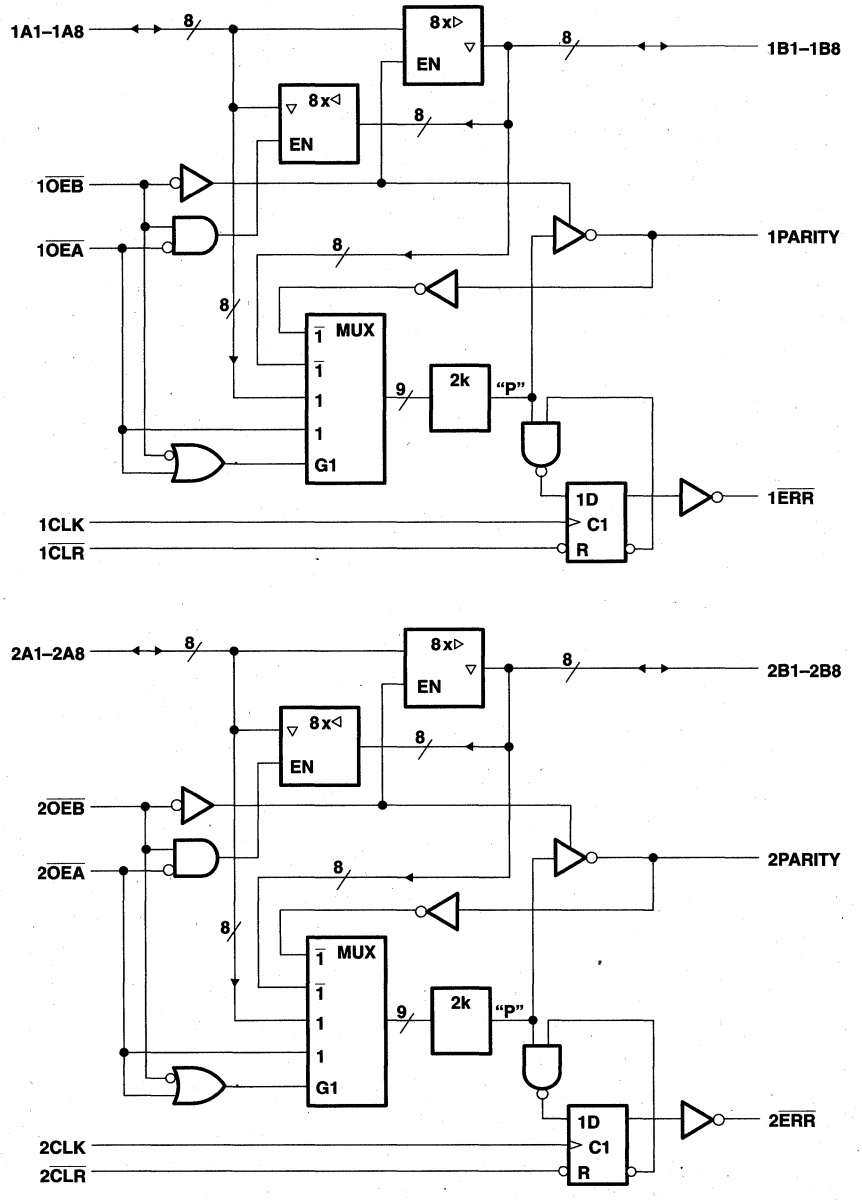
NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume the $\overline{ERR}$ output was previously high.
§ In this mode, the $\overline{ERR}$ output (when clocked) shows inverted parity of the A bus.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

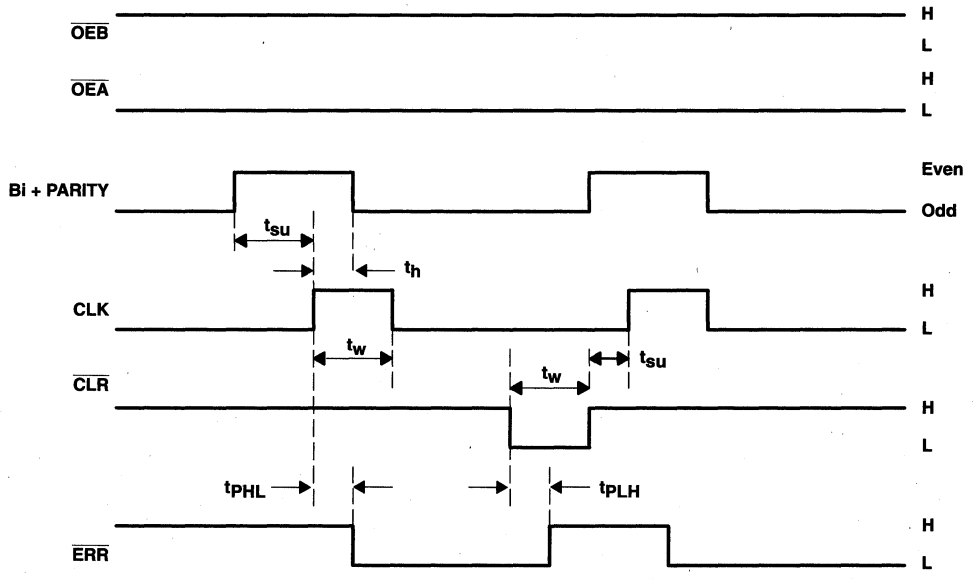


ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}_{n-1}$		
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† The state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point "P".

error-flag waveforms



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16833 ..... 96 mA
SN74ABT16833 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16833		SN74ABT16833		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{OH}	High-level output voltage	$\overline{ERR}$		5.5		5.5	V
I_{OH}	High-level output current	Except $\overline{ERR}$		−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16833		SN74ABT16833		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	All outputs except $\overline{ERR}$	2.5	3		2.5				V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3	3.4		3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA					2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡	2.7				2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 24 mA			0.25	0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA			0.3	0.55‡				0.55	
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V	$\overline{ERR}$			20		20		20	µA
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IL}	V_{CC} = 0,	V_I = GND	A or B ports			−50		−50		−50	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1.5	2		2		2	mA
			Outputs low		28	36		36		36	
			Outputs disabled		1	2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

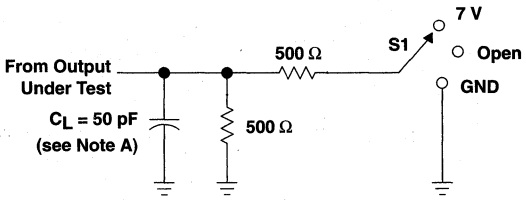
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C	SN54ABT16833		SN74ABT16833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	3		3		3		ns
t_{su}	Setup time before CLK↑	A port	4.5		4.5		4.5		ns
		$\overline{CLR}$	1		1		1		
t_h	Hold time after CLK↑	A port	0		0		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16833		SN74ABT16833		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
t_{PHL}			2	3.1	3.9	2	4.5	2	4.3	
t_{PZH}	$\overline{OE}$	A or B	2	3.9	4.9	2	5.8	2	5.6	ns
t_{PZL}			2.5	4.3	5.1	2.5	6.2	2.5	6	
t_{PHZ}	$\overline{OE}$	A or B	2	3.6	4.5	2	5.5	2	5.4	ns
t_{PLZ}			1.5	3	3.8	1.5	4.7	1.5	4.3	
t_{PLH}	A or $\overline{OE}$	PARITY	2	4.6	5.4	2	7	2	6.7	ns
t_{PHL}			2	4.3	5.1	2	6.5	2	6.1	
t_{PZH}	$\overline{OE}$	PARITY	2	3.6	5	2	5.8	2	5.7	ns
t_{PZL}			2.5	4.4	5.8	2.5	6.7	2.5	6.5	
t_{PHZ}	$\overline{OE}$	PARITY	1.5	3.2	4	1.5	4.8	1.5	4.7	ns
t_{PLZ}			1.5	2.9	3.7	1.5	4.2	1.5	4.1	
t_{PLH}	CLK, $\overline{CLR}$	$\overline{ERR}$	2	3.4	4.2	2	4.8	2	4.6	ns
t_{PHL}	CLK		2	2.8	3.6	2	4.1	2	3.9	

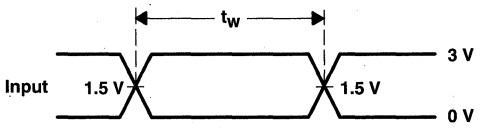
PARAMETER MEASUREMENT INFORMATION



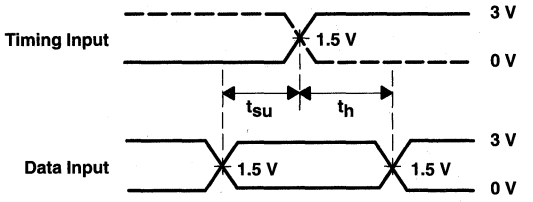
LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

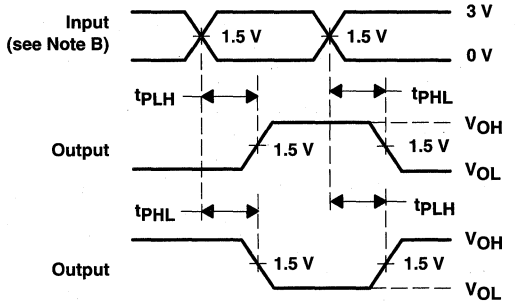
$\overline{ERR}$	S1
t_{PHL} (see Note E)	7 V
t_{PLH} (see Note F)	7 V



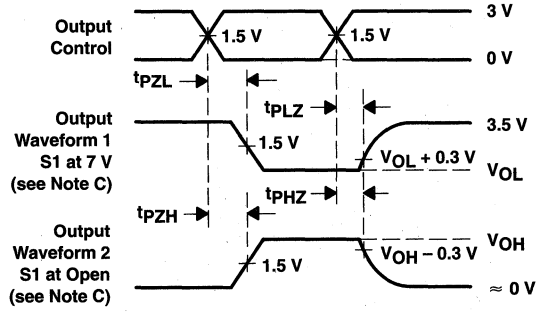
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



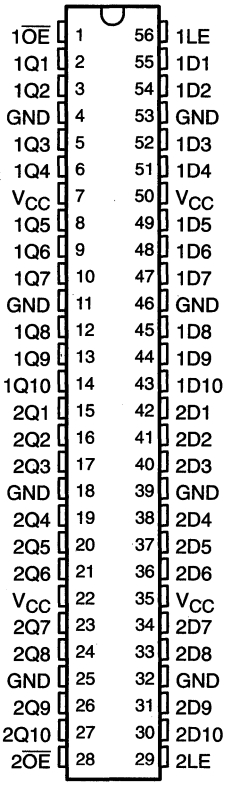
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PHL} is measured at 1.5 V.
F. t_{PLH} is measured at V_{OL} + 0.3 V.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16841 . . . WD PACKAGE
SN74ABT16841 . . . DL PACKAGE
(TOP VIEW)



description

These 20-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ABT16841 can be used as two 10-bit latches or one 20-bit latch. The twenty latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16841 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

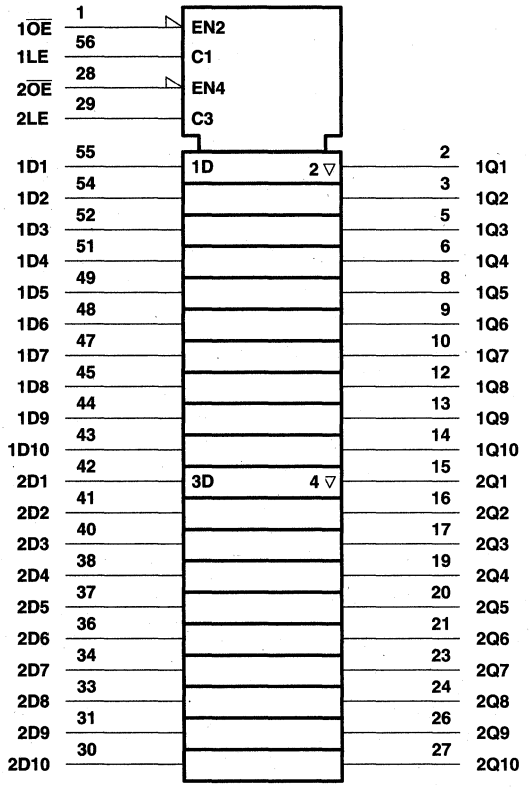
The SN54ABT16841 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16841 is characterized for operation from –40°C to 85°C.

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each 10-bit latch)

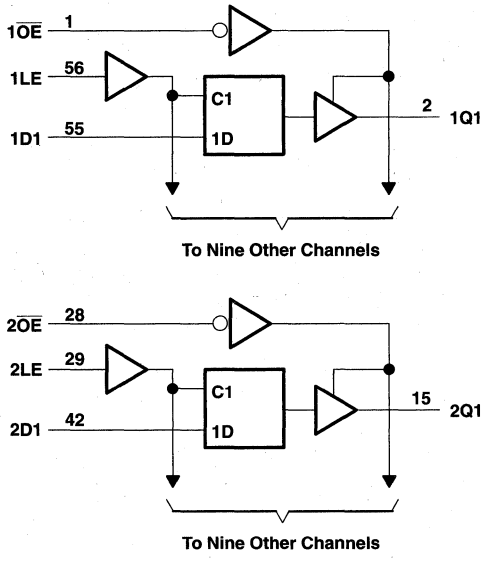
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16841 ..... 96 mA
SN74ABT16841 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16841		SN74ABT16841		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16841		SN74ABT16841		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.5		0.5		0.5	mA
		Outputs low			89		89		89	
		Outputs disabled			0.5		0.5		0.5	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3.5						pF
C_o	V_O = 2.5 V or 0.5 V			7.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

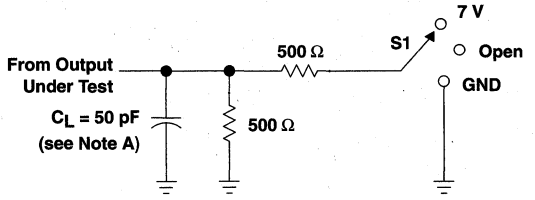
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V_{CC} = 5 V, T_A = 25°C		SN54ABT16841		SN74ABT16841		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high or low	4		4		4		ns
t_{su}	Setup time, data before LE↓	1		1		1		ns
t_h	Hold time, data after LE↓	2		2		2		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

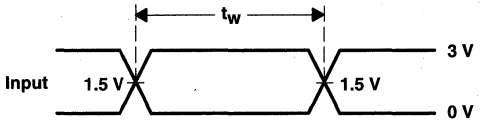
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16841		SN74ABT16841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.1	3.2	4.3	1.1	5.7	1.1	5	ns
t_{PHL}			1.6	3.5	4.5	1.6	5.8	1.6	5.1	
t_{PLH}	LE	Q	1.1	3.2	4.4	1.1	5.6	1.1	5	ns
t_{PHL}			1.6	3.4	4.6	1.6	5.3	1.6	5	
t_{PZH}	$\overline{OE}$	Q	1.2	3.2	4.7	1.2	5.8	1.2	5.7	ns
t_{PZL}			1.7	3.6	5	1.7	5.7	1.7	5.6	
t_{PHZ}	$\overline{OE}$	Q	2.2	4.1	5.7	2.2	6.6	2.2	6.5	ns
t_{PLZ}			1.9	4.4	5.8	1.9	8.4	1.9	7.1	

PARAMETER MEASUREMENT INFORMATION

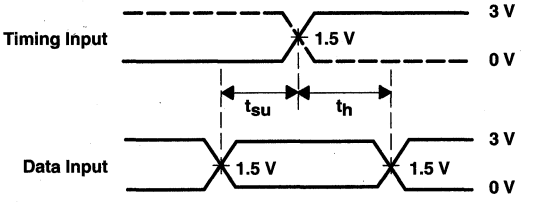


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

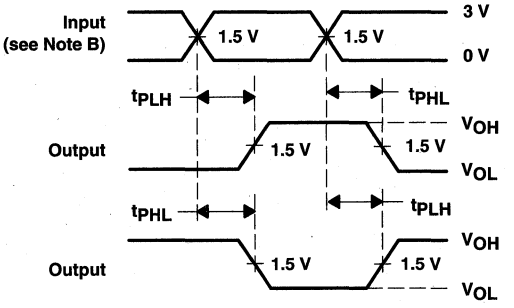
LOAD CIRCUIT FOR OUTPUTS



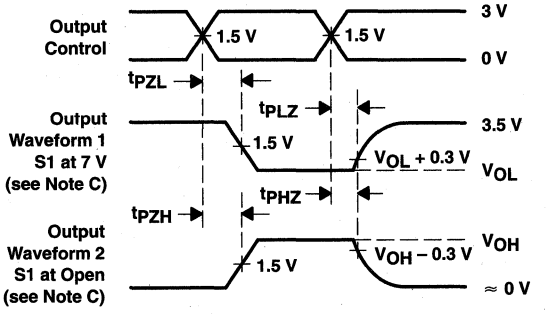
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



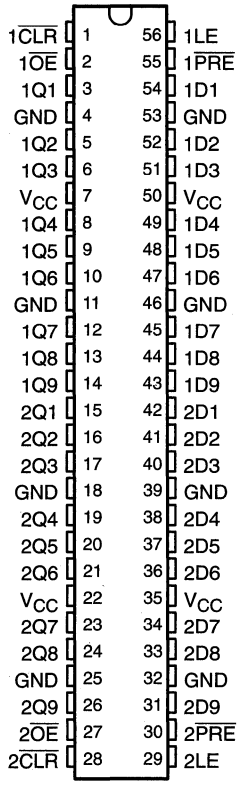
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16843 . . . WD PACKAGE
SN74ABT16843 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16843 18-bit latch is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ABT16843 can be used as two 9-bit latches or one 18-bit latch. The eighteen latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16843 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

PRODUCT PREVIEW

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description (continued)

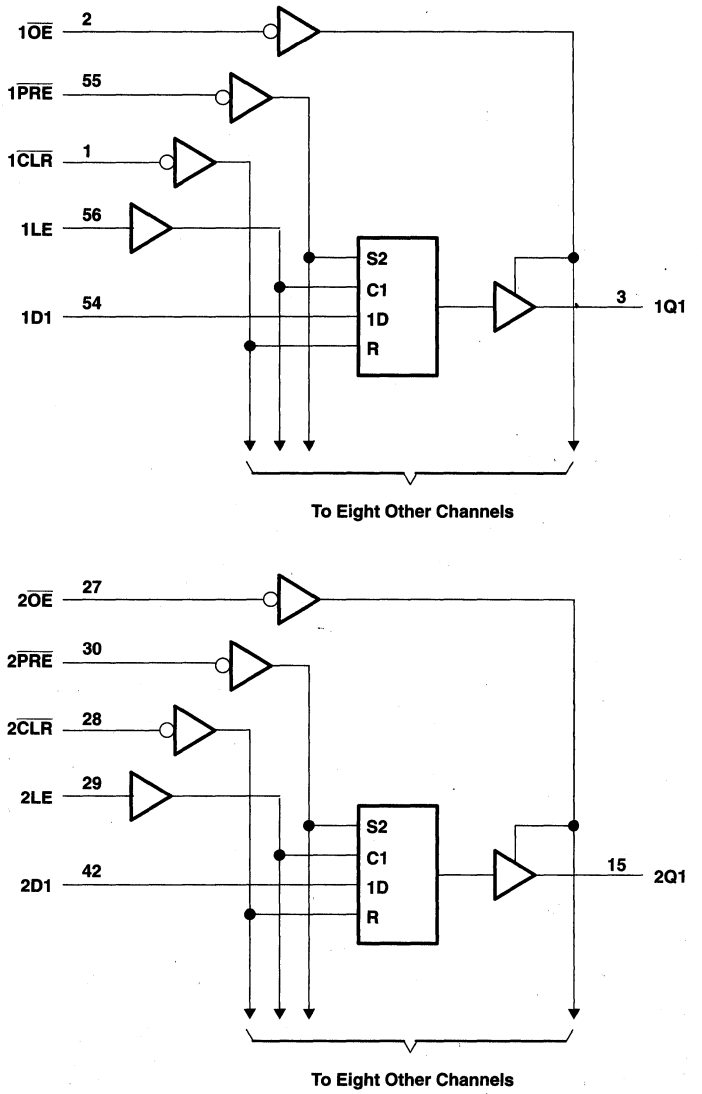
The SN54ABT16843 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16843 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit latch)

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16843 ..... 96 mA
SN74ABT16843 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16843		SN74ABT16843		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT16843		SN74ABT16843		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			500		500		500	mA
		Outputs low			85		85		85	
		Outputs disabled			500		500		500	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3.5						pF
C_o	V_O = 2.5 V or 0.5 V			7.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT16843		SN74ABT16843		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		3.3		ns
		$\overline{PRE}$ low	3.3		3.3		3.3		
		LE high	3.3		3.3		3.3		
t_{su}	Setup time, data before LE↓	High	1		1		1		ns
		Low	1		1		1		
t_h	Hold time, data after LE↓		1.4		1.4		1.4		ns

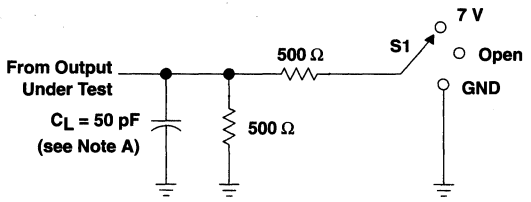
PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16843		SN74ABT16843		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.1	3	4.4	1.1	6	1.1	5.2	ns
t_{PHL}			1.4	3.2	4.9	1.4	5.6	1.4	5.4	
t_{PLH}	LE	Q	1.4	3.6	5.2	1.4	7	1.4	6.2	ns
t_{PHL}			1.9	3.7	5.1	1.9	6.2	1.9	5.8	
t_{PLH}	$\overline{PRE}$	Q	1	3.8	5.9	1	7.6	1	6.6	ns
t_{PHL}			1.7	3.6	5	1.7	6	1.7	5.6	
t_{PLH}	$\overline{CLR}$	Q	1.2	3.6	5.1	1.2	7.2	1.2	6.1	ns
t_{PHL}			2	4.2	6.1	2	6.9	2	6.7	
t_{PZH}	$\overline{OE}$	Q	1	2.9	4.6	1	5.8	1	5.7	ns
t_{PZL}			1.4	3.3	5.1	1.4	5.7	1.4	5.6	
t_{PHZ}	$\overline{OE}$	Q	2.4	4.1	6	2.4	6.6	2.4	6.5	ns
t_{PLZ}			1.9	4.2	6	1.9	9.6	1.9	7.7	

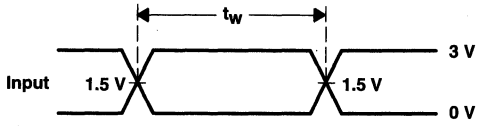
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

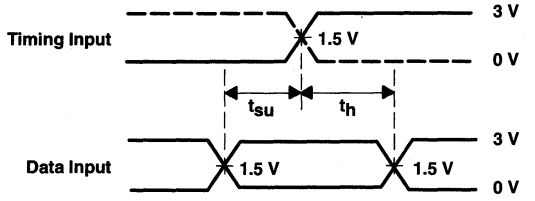


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

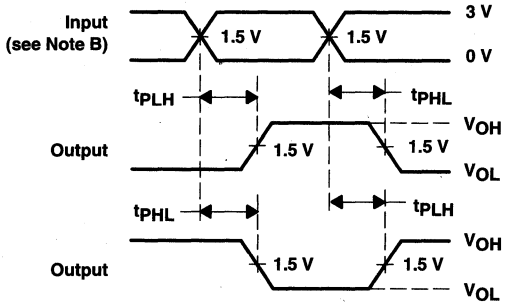
LOAD CIRCUIT FOR OUTPUTS



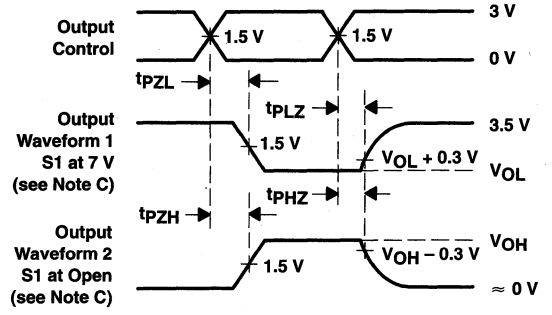
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

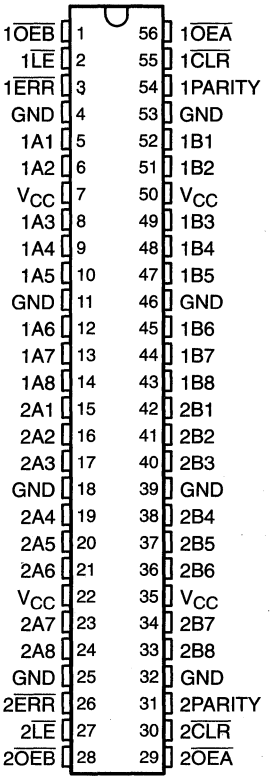
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

D4519, OCTOBER 1992 – REVISED DECEMBER 1992

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Parity Error Flag With Parity Generator/Checker**
- **Latch for Storage of the Parity Error Flag**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16853 . . . WD PACKAGE
SN74ABT16853 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16853 dual 8-bit to 9-bit parity transceiver is designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error ($\overline{ERR}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$ and $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT16853 provides true data at its outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the $\overline{ERR}$ flag. The parity-error output can be passed, sampled, stored, or cleared from the latch using the latch-enable ($\overline{LE}$) and clear ($\overline{CLR}$) control inputs. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus, and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16853 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16853 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16853 is characterized for operation from –40°C to 85°C.

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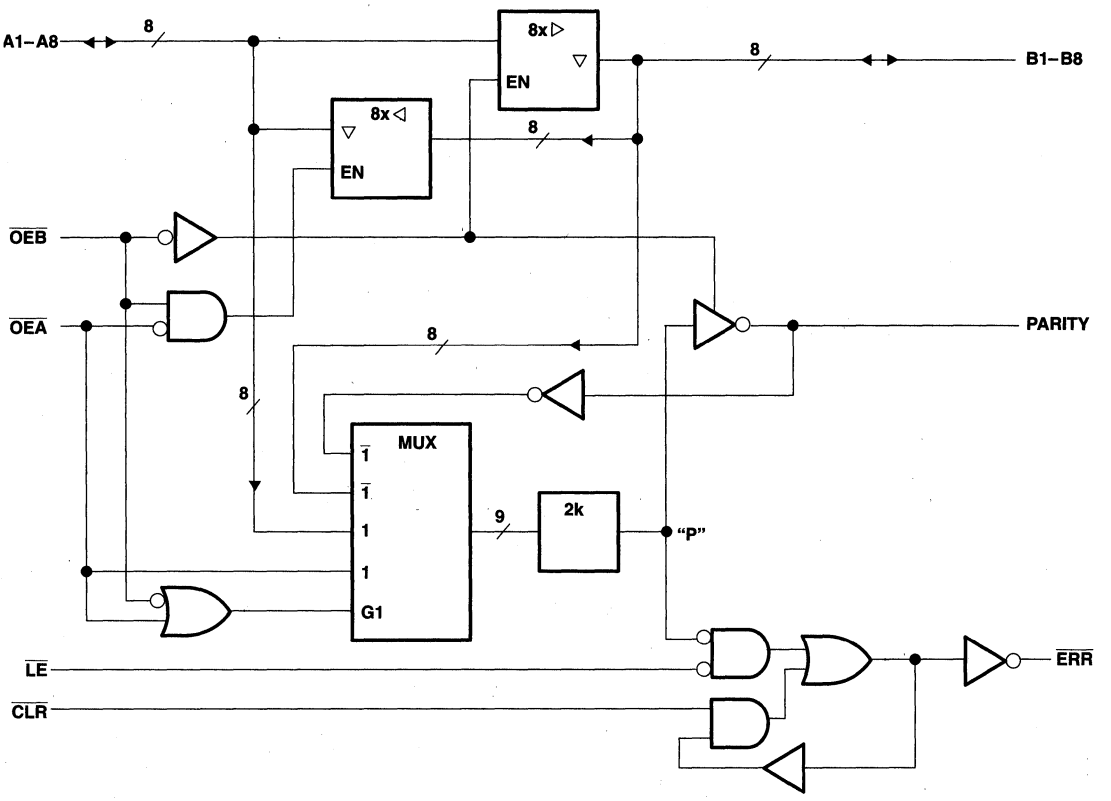
FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	LE	Ai Σ OF H	Bi† Σ OF H	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error flag register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H H L	Isolation§ (parity check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume the $\overline{ERR}$ output was previously high.
§ In this mode, the $\overline{ERR}$ output (when clocked) shows inverted parity of the A bus.

logic diagram (each transceiver) (positive logic)

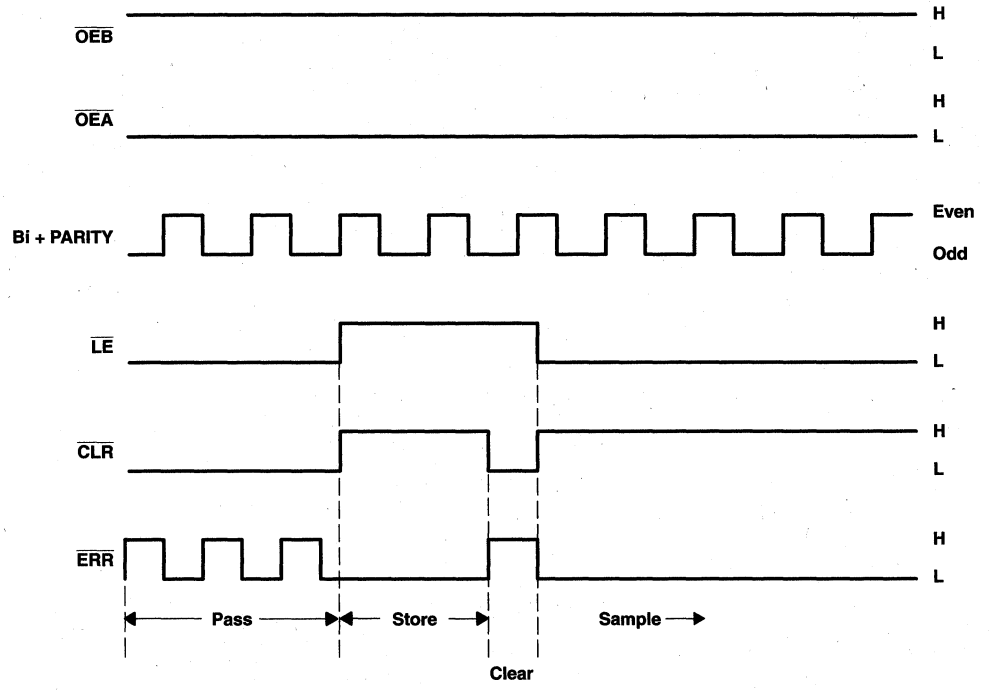


ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT	OUTPUT	FUNCTION
$\overline{CLR}$	$\overline{LE}$	POINT P	$\overline{ERR}_{n-1}$†	$\overline{ERR}$	
L	L	L	X	L	Pass
		H		H	
H	L	L	X	L	Sample
		X	L	L	
		H	H	H	
L	H	X	X	H	Clear
H	H	X	L	L	Store
			H	H	

† The state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, $\overline{LE}$, or point P

error-flag waveforms



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16853 ..... 96 mA
SN74ABT16853 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16853		SN74ABT16853		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{OH}	High-level output voltage	$\overline{ERR}$		5.5		5.5	V
I_{OH}	High-level output current	Except $\overline{ERR}$		−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16853		SN74ABT16853		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	All outputs except $\overline{ERR}$	2.5	3		2.5				V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3	3.4		3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA					2				
	V_{CC} = 4.5 V	I_{OH} = −32 mA		2‡	2.7				2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 24 mA			0.25	0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA			0.3	0.55‡				0.55	
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V	$\overline{ERR}$			20		20		20	µA
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IL}	V_{CC} = 0 V,	V_I = GND	A or B ports			−50		−50		−50	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1.5	2		2		2	mA
			Outputs low		32	40		40		40	
			Outputs disabled		1	2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

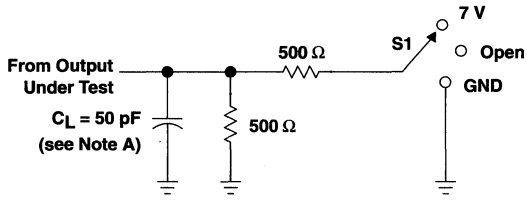
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT16853		SN74ABT16853		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{LE}$ high or low	8.5		8.5		8.5		ns
		$\overline{CLR}$ low	4		4		4		
t_{su}	Setup time	A, B, and PARITY before $\overline{LE}\downarrow$	10		10		10		ns
		$\overline{CLR}$ before $\overline{LE}\downarrow$	0		0		0		
t_h	Hold time	A, B, and PARITY after $\overline{LE}\downarrow$	0		0		0		ns
		$\overline{CLR}$ after $\overline{LE}\downarrow$	0		0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16853		SN74ABT16853		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
t_{PHL}			2	3.1	3.9	2	4.5	2	4.3	
t_{PLH}	A or $\overline{OE}$	PARITY	2	4.6	5.9	2	7.3	2	7.1	ns
t_{PHL}			2	4.8	6.2	2	7.6	2	7.2	
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	2	3.7	5.1	2	5.9	2	5.7	ns
t_{PZH}	$\overline{OE}$	A or B	2	3.9	4.9	2	5.8	2	5.6	ns
t_{PZL}			2.5	4.3	5.1	2.5	6.2	2.5	6	
t_{PHZ}	$\overline{OE}$	A or B	2	3.6	4.5	2	5.5	2	5.4	ns
t_{PLZ}			1.5	3	3.8	1.5	4.7	1.5	4.3	
t_{PZH}	$\overline{OE}$	PARITY	2	3.6	5	2	5.8	2	5.7	ns
t_{PZL}			2.5	4.4	5.8	2.5	6.7	2.5	6.5	
t_{PHZ}	$\overline{OE}$	PARITY	1.5	3.2	4	1.5	4.8	1.5	4.7	ns
t_{PLZ}			1.5	2.9	3.7	1.5	4.2	1.5	4.1	
t_{PLH}	$\overline{LE}$	$\overline{ERR}$	2	3.5	4.2	2	5	2	4.8	ns
t_{PHL}			2	3.4	4.4	2	5.2	2	4.9	
t_{PLH}	A, B, or PARITY	$\overline{ERR}$	2	4.5	6.3	2	7.5	2	7.2	ns
t_{PHL}			2	4.8	6.3	2	7.7	2	7.4	

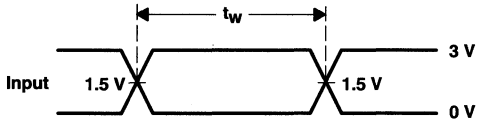
PARAMETER MEASUREMENT INFORMATION



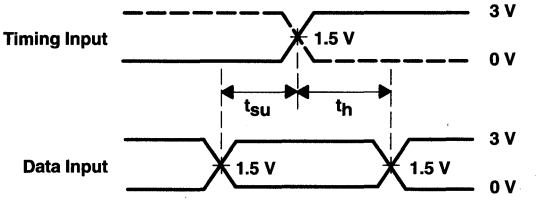
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

$\overline{ERR}$	S1
t_{PHL} (see Note E)	7 V
t_{PLH} (see Note F)	7 V

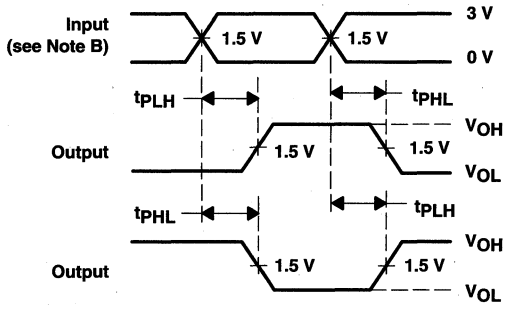
LOAD CIRCUIT FOR OUTPUTS



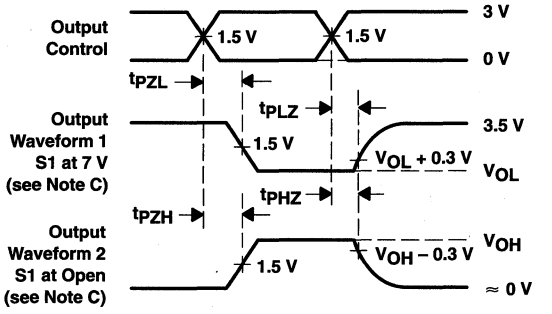
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



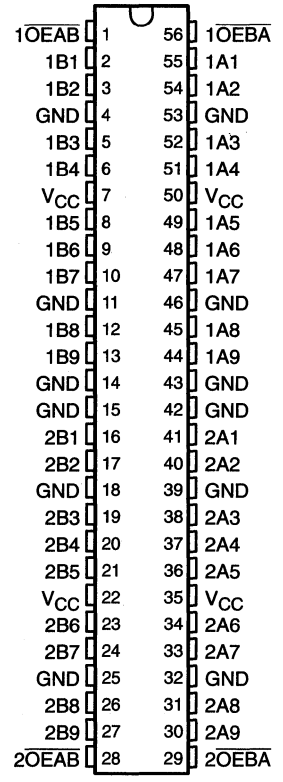
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PHL} is measured at 1.5 V.
F. t_{PLH} is measured at V_{OL} + 0.3 V.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16863 . . . WD PACKAGE
SN74ABT16863 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16863 is an 18-bit noninverting transceiver designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

The 'ABT16863 can be used as two 9-bit transceivers or one 18-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs.

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16863 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

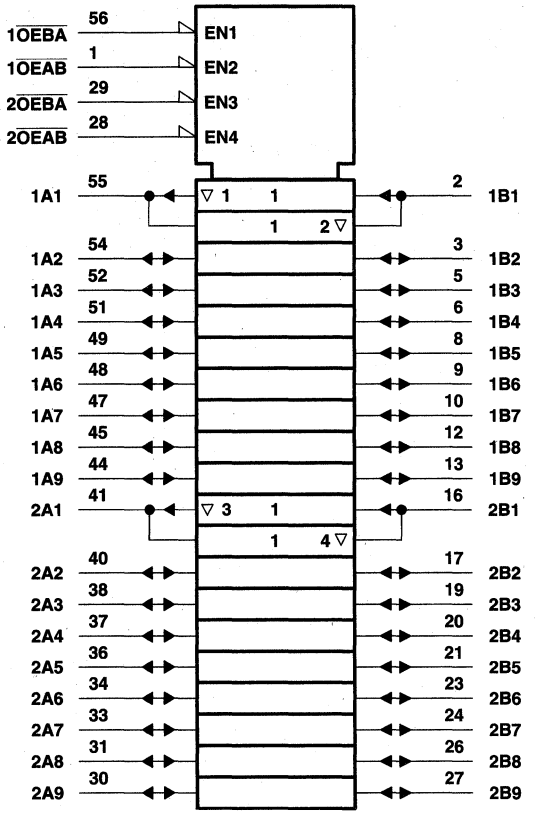
The SN54ABT16863 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16863 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit section)

INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
H	L	B data to A bus
L	H	A data to B bus
H	H	Isolation

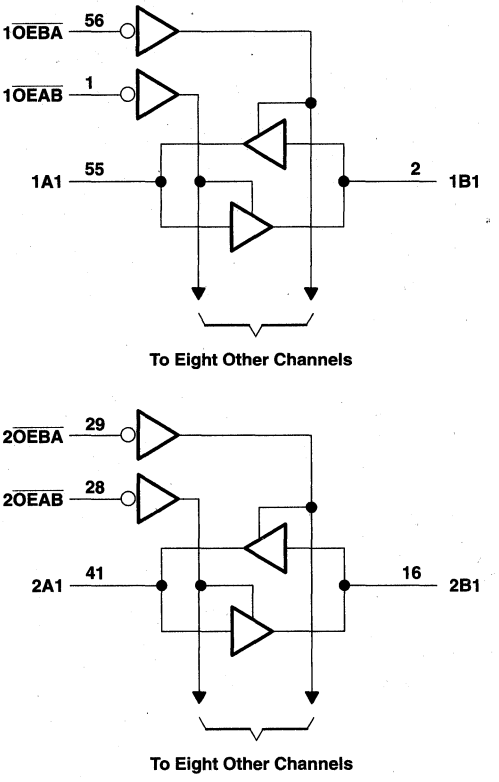
Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16863 . . . . . 96 mA
SN74ABT16863 . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . −18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) . . . . . 1 W
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16863		SN74ABT16863		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

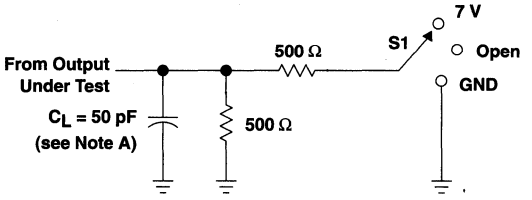
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16863		SN74ABT16863		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3.5						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		9.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

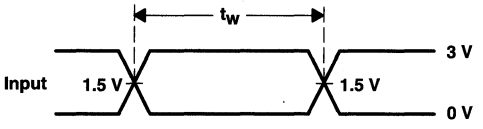
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16863		SN74ABT16863		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.2	3.2	1	3.7	1	3.5	ns
t_{PHL}			1	2.2	3.4	1	4.2	1	3.9	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1	2.9	4.5	1	5.7	1	5.4	ns
t_{PZL}			1	2.6	4.1	1	5.2	1	4.8	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.6	4.1	5.4	1.6	6.3	1.6	6	ns
t_{PLZ}			1.5	3.3	4.5	1.5	5.3	1.5	5	

PARAMETER MEASUREMENT INFORMATION

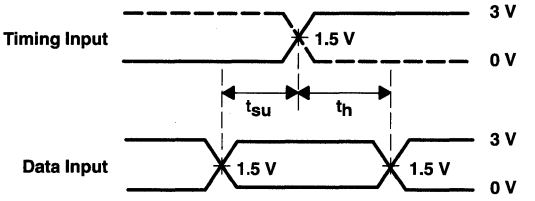


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

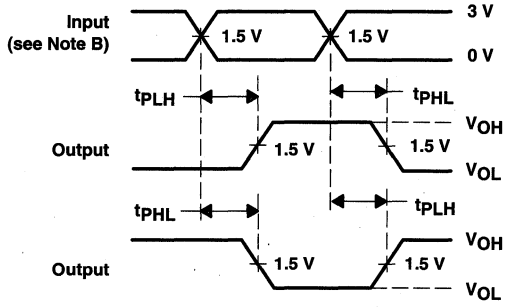
LOAD CIRCUIT FOR OUTPUTS



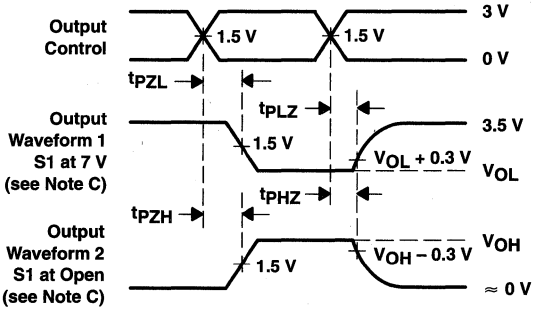
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



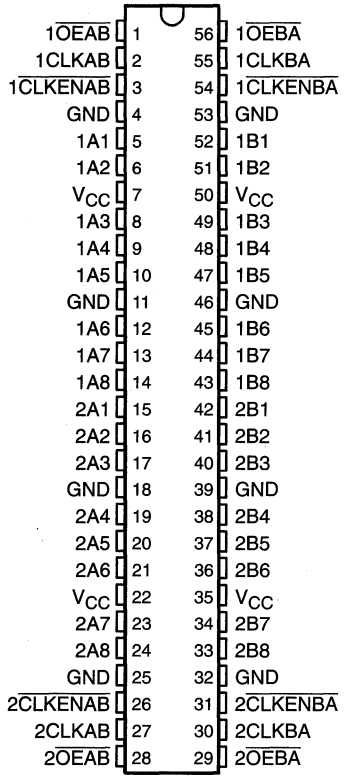
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16952 . . . WD PACKAGE
SN74ABT16952 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT16952 is a 16-bit registered transceiver that contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. The 'ABT16952 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16952 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16952 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16952 is characterized for operation from –40°C to 85°C.

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

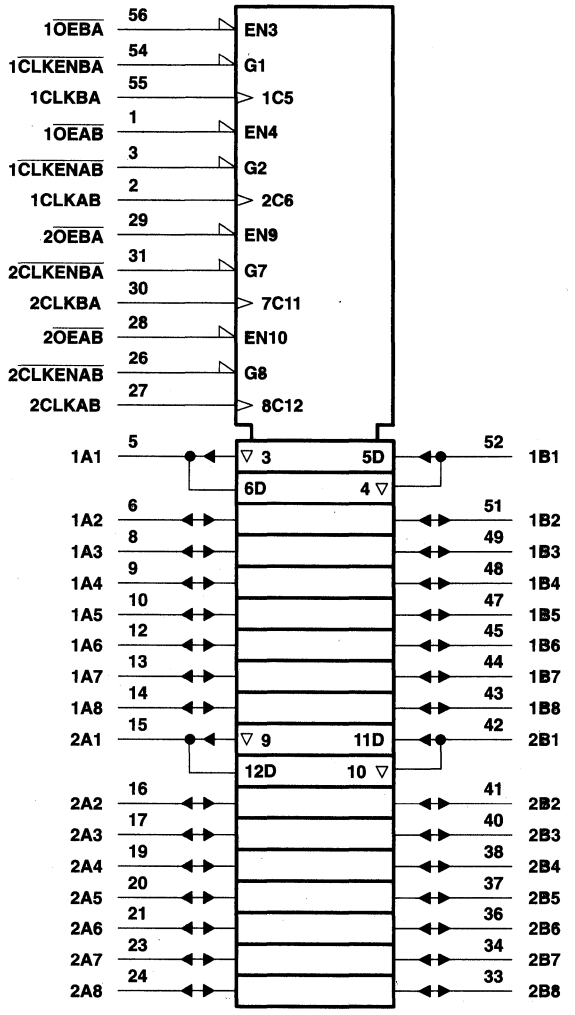
FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	B
H	X	L	X	B_0‡
X	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.

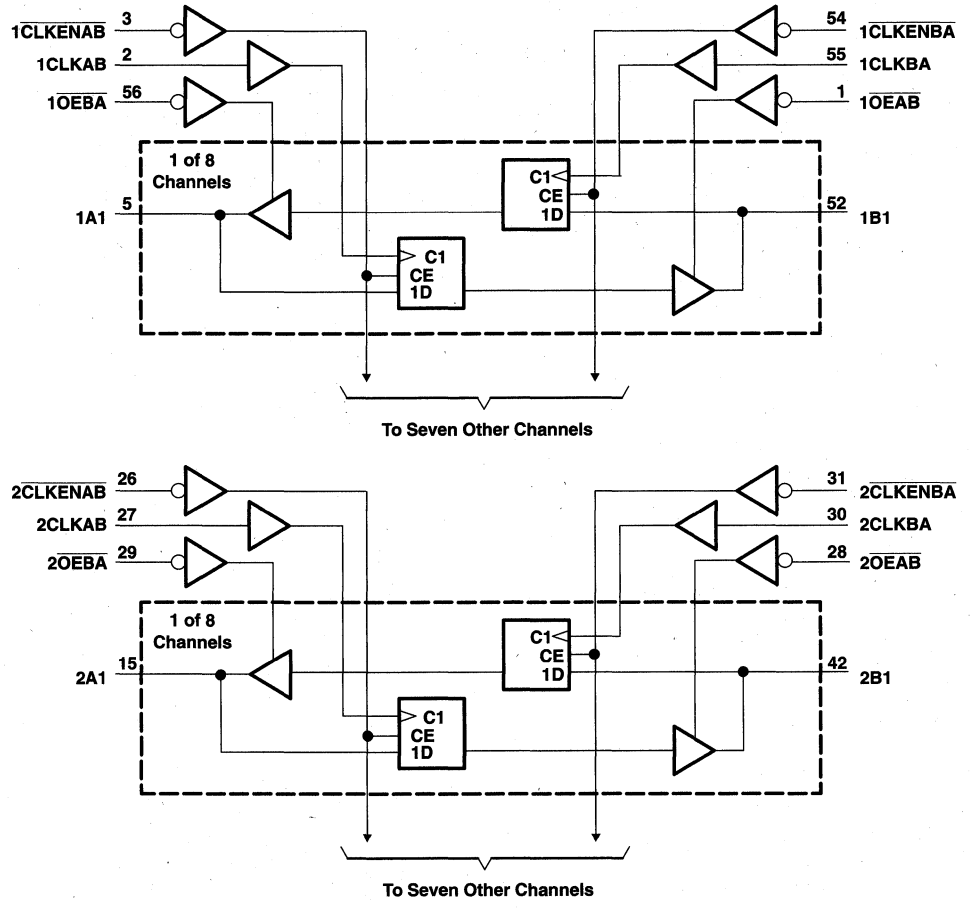
‡ Level of B before the indicated steady-state input conditions were established.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16952 ..... 96 mA
SN74ABT16952 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16952		SN74ABT16952		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16952		SN74ABT16952		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			35		35		35	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				0.5		0.5		0.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		8.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

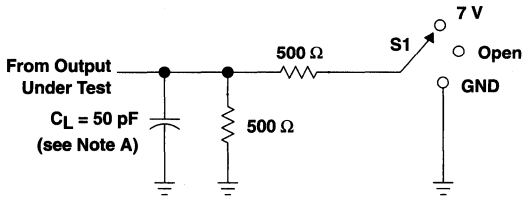
			V_{CC} = 5 V, T_A = 25°C		SN54ABT16952		SN74ABT16952		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w†	Pulse duration, CLKAB or CLKBA high or low		3.3		3.3		3.3		ns
t_{su}	Setup time, before CLKAB↑ or CLKBA↑	A or B	3.5		3.5		3.5		ns
		$\overline{CLKENAB}$ or $\overline{CLKENBA}$	3		3		3		
t_h	Hold time, after CLKAB↑ or CLKBA↑	A or B	1		1		1		ns
		$\overline{CLKENAB}$ or $\overline{CLKENBA}$	1		1		1		

† This parameter is specified by design but not tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

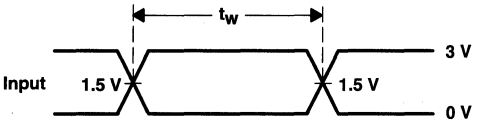
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16952		SN74ABT16952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLK	A or B	1	2.6	3.9	1	4.4	1	4.3	ns
t_{PHL}			1	2.6	4.2	1	4.6	1	4.5	
t_{PZH}	$\overline{OE}$	A or B	1	2.5	3.8	1	4.7	1	4.6	ns
t_{PZL}			1	2.8	5.1	1	6.1	1	6	
t_{PHZ}	$\overline{OE}$	A or B	1.7	3.4	4.7	1.7	6.1	1.7	5.5	ns
t_{PLZ}			1.3	3	3.9	1.3	4.8	1.3	4.2	

PARAMETER MEASUREMENT INFORMATION

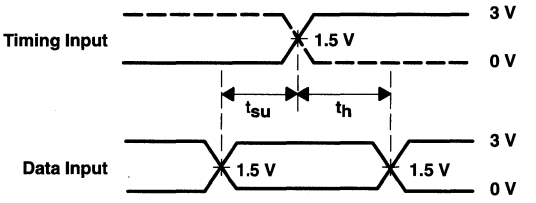


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

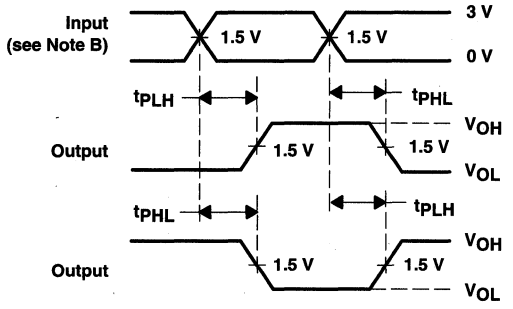
LOAD CIRCUIT FOR OUTPUTS



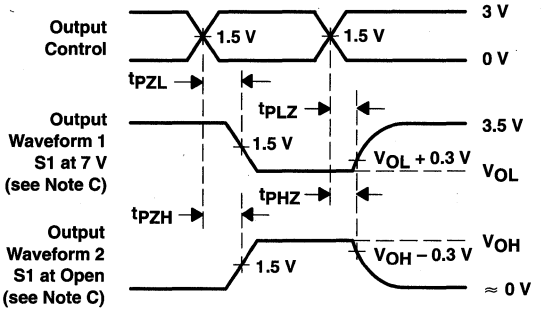
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

ABTE/ETL Widebus™

Features

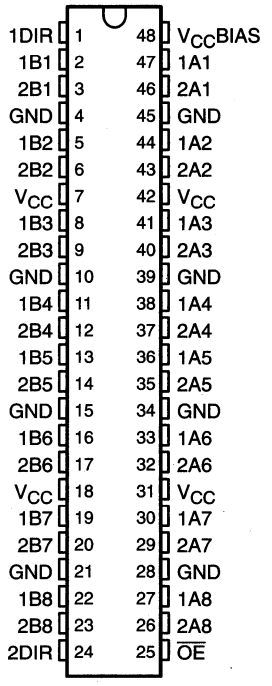
- Supports the VME64 ETL specification
- Reduced, TTL-compatible, input threshold range
- JEDEC standard 48-/56-pin SSOP package
- New EIAJ standard Shrink Widebus ™ TSSOP package
- Flow-through package pinout organizes all inputs on one side and all outputs on the other side
- Distributed V_{CC} and GND pinouts
- High-drive outputs (I_{OH} = −60 mA, I_{OL} = 90 mA)
- 25-Ω series-damping resistor on B port

Benefits

- Improved propagation delay versus number of outputs switching. Superior pin-to-pin output skew; 15–20% faster speed
- 30% board space improvement over SSOP Widebus™ package; meets 1.1-mm height requirements for memory card and other thin applications
- Minimized mutual coupling and 2:1 I/O-to-GND rates result in < 0.8-V simultaneous switching noise typically

- **Supports the VME64 ETL Specification**
- **Reduced, TTL-Compatible, Input Threshold Range**
- **High-Drive Outputs (I_{OH} = −60 mA, I_{OL} = 90 mA) Support 25-Ω Incident-Wave Switching**
- **V_{CC}BIAS Pin Minimizes Signal Distortion During Live Insertion**
- **Internal Pullup Resistor on $\overline{OE}$ Keeps Outputs in High-Impedance State During Power Up or Power Down**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **25-Ω Series-Dampening Resistor on B Port**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ABTE16245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The B port has a 25-Ω series output resistor to reduce ringing. Active bus-hold inputs are also found on the B port to hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CC}BIAS, which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

The SN74ABTE16245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ABTE16245 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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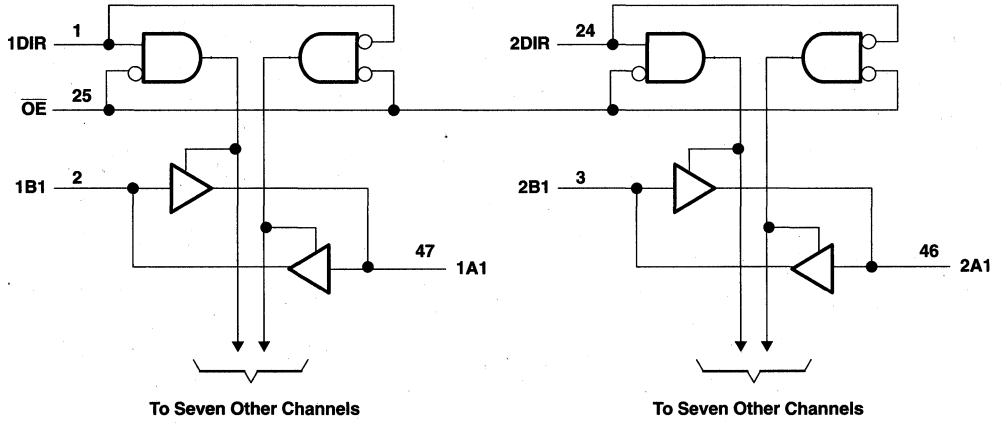
FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_{IH}	High-level input voltage	Except control pins	1.6		V
		Control pins	2		V
V_{IL}	Low-level input voltage	Except control pins		1.4	V
		Control pins		0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current	B bus		−12	mA
I_{OL}	Low-level output current	B bus		12	mA
I_{OH}	High-level output current	A bus		−32	mA
				−60†	
I_{OL}	Low-level output current	A bus		64	mA
				90†	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating pins (input or A-bus I/O) must be held high or low.
† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	B port	V_{CC} = 5.25 V	I_{OH} = − 100 µA			V_{CC}−1	V
		V_{CC} = 4.75 V	I_{OH} = − 1 mA		2.4		
			I_{OH} = − 12 mA		2		
	A port	V_{CC} = 4.75 V	I_{OH} = − 1 mA			4	
			I_{OH} = − 32 mA		2.4		
			I_{OH} = − 60 mA		2		
V_{OL}	B port	V_{CC} = 4.75 V	I_{OL} = 1 mA			0.4	V
			I_{OL} = 12 mA			0.8	
	A port	V_{CC} = 4.75 V	I_{OL} = 64 mA			0.55	
			I_{OL} = 90 mA			0.9	
$I_{I(hold)}$	B port	V_{CC} = 4.75 V	V_I = 0.8 V		100		µA
			V_I = 2 V		−100		
I_I	Control inputs	V_{CC} = 5.25 V,	V_I = V_{CC} or GND			±1	µA
	A or B ports					±100	
I_{OZH}†		V_{CC} = 5.25 V,	V_O = 2.4 V			10	µA
I_{OZL}†		V_{CC} = 5.25 V,	V_O = 0.4 V			−10	µA
I_{off}		V_{CC} = 0,	V_{CC}BIAS = 0	V_I or V_O ≤ 4.5 V		±100	µA
I_{CC}	A or B ports	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			mA
				Outputs low			
				Outputs disabled			
C_i	Control inputs	V_I = 2.5 V or 0.5 V					pF
C_{io}	B port	V_O = 2.5 V or 0.5 V				9	pF
	A port	Per IEEE 1194.0-1991				9	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

live insertion specifications over recommended operating free-air temperature range

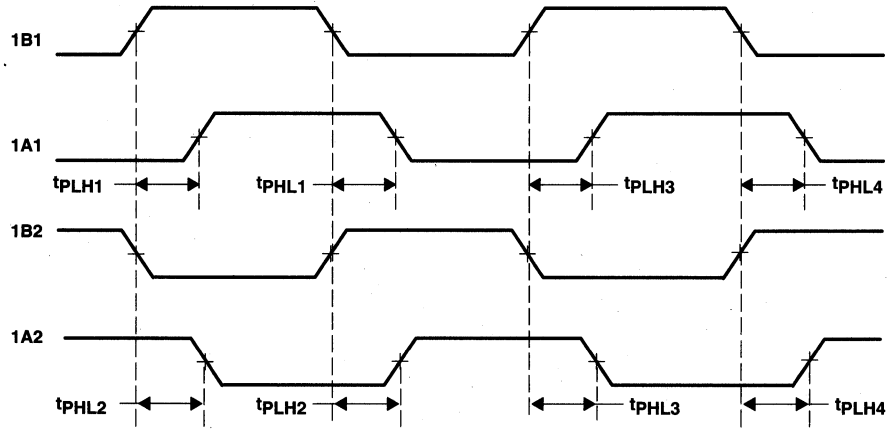
PARAMETER	TEST CONDITIONS				MIN	TYP	MAX	UNIT
I_{CC} (V_{CC}BIAS)	V_{CC} = 0 to 4.75 V,		V_{CC}BIAS = 4.75 V to 5.25 V,	$I_{O(DC)}$ = 0			500	µA
	V_{CC} = 4.75 V to 5.25 V,		V_{CC}BIAS = 4.75 V to 5.25 V,	$I_{O(DC)}$ = 0			20	
V_O	V_{CC} = 0,		V_{CC}BIAS = 4.75 V	A port	1.3	1.5	1.7	V
I_O	V_{CC} = 0,	V_O = 0,	V_{CC}BIAS = 4.75 V	A port	−20		−100	µA
	V_{CC} = 0,	V_O = 3 V,	V_{CC}BIAS = 4.75 V		20		100	

PRODUCT PREVIEW

extended output characteristics over recommended temperature and supply operating ranges (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	MIN	TYP	MAX	UNIT
$t_{sk(pr)}$†	A	B	V_{CC} = Constant, ΔT_A = 20°C				2.5	ns
	B	A		Z_O = 50 Ω, R_X = 55.6 Ω			4	
$t_{sk(load)}$†	B	A	V_{CC} = Constant, Temperature = Constant	Z_O = 50, 25, or 12.5 Ω, R_X = 55.6, 26.3, or 12.8 Ω			4	ns
t_t	B	A	Time between 1 V and 2 V	Z_O= 25 Ω, R_X = 26.3 Ω	1.2		3	ns
	A	B	Rise or fall time 10%–90%		3			

† $t_{sk(pr)} + t_{sk(load)} < 6$ ns

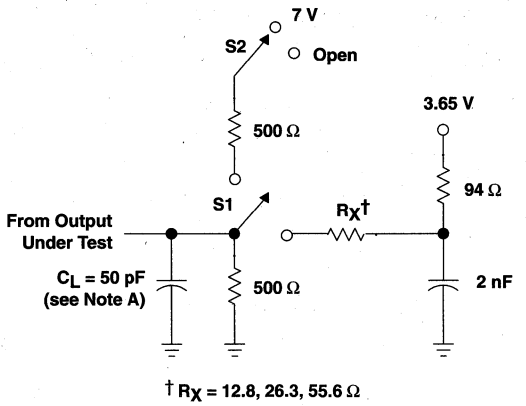


Output skew, $t_{sk(pr)}$, is calculated as the greater of the difference between the fastest and slowest of t_{PLH} and t_{PHL} (e.g., t_{PLHn}, n = 1 to 16; and t_{PHLn}, n = 1 to 16), with any combination of the inputs switching coincidently.

Figure 1. Voltage Waveforms for Extended Characteristics

PRODUCT PREVIEW

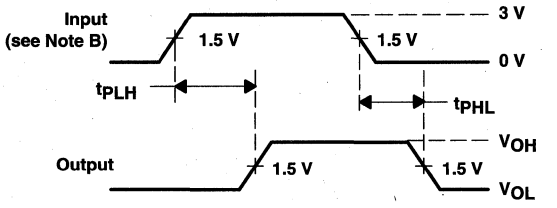
PARAMETER MEASUREMENT INFORMATION



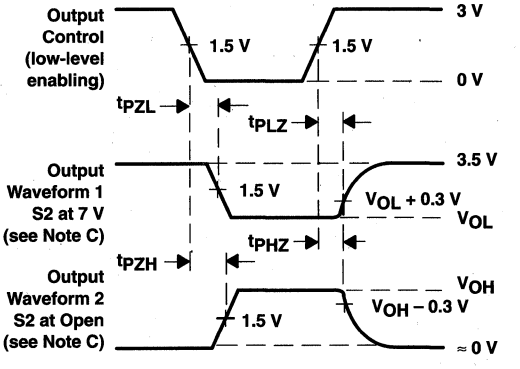
† RX = 12.8, 26.3, 55.6 Ω

LOAD CIRCUIT FOR OUTPUTS

TEST	S1	S2
t_{PLH}/t_{PHL} (A port)	Down	X
t_{PLH}/t_{PHL} (B port)	Up	Open
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH}	Up	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



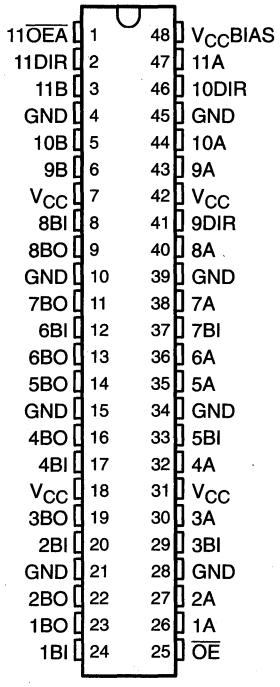
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Supports the VME64 ETL Specification**
- **Reduced, TTL-Compatible, Input Threshold Range**
- **High-Drive Outputs (I_{OH} = −60 mA, I_{OL} = 90 mA) Support 25-Ω Incident-Wave Switching**
- **V_{CC}BIAS Pin Minimizes Signal Distortion During Live Insertion**
- **Internal Pullup Resistor on $\overline{OE}$ Keeps Outputs in High-Impedance State During Power Up or Power Down**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **25-Ω Series-Dampening Resistor on B Port**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ABTE16246 is an 11-bit noninverting transceiver designed for synchronous two-way communication between buses.

This device consists of open-collector and 3-state outputs. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. When $\overline{OE}$ is low, the device is active.

The B port has a 25-Ω series output resistor to reduce ringing. Active bus-hold inputs are also found on the B port to hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CC}BIAS, which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

The SN74ABTE16246 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ABTE16246 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	A data to B bus
L	H	B data to A bus
H	X	Isolation

PRODUCT PREVIEW

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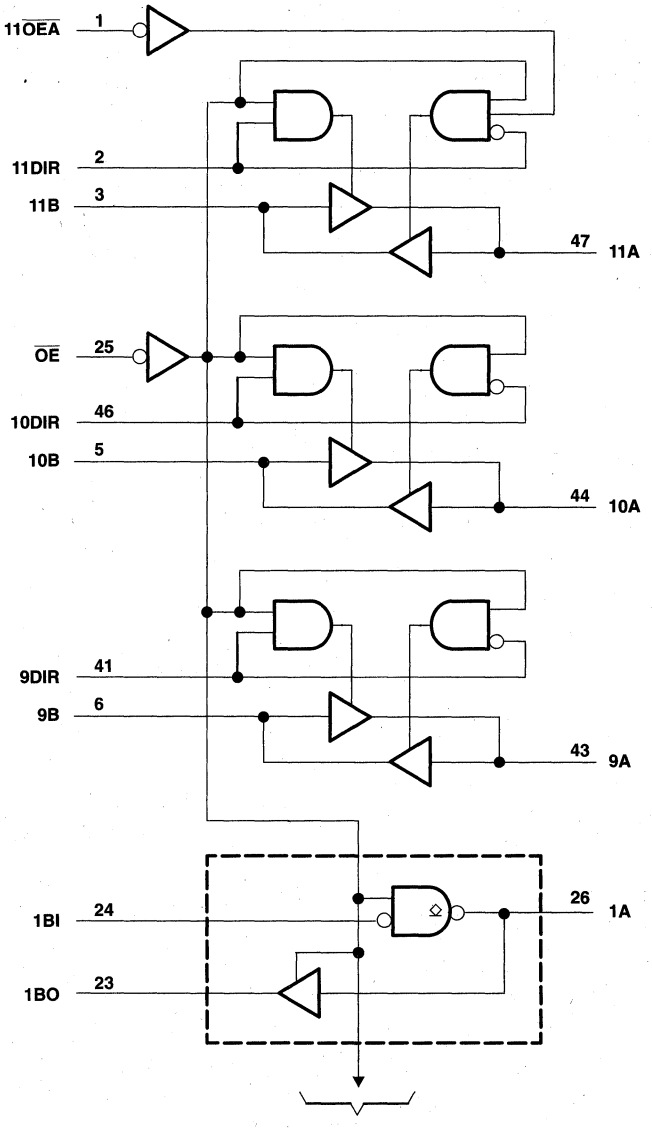
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_{IH}	High-level input voltage	Except control pins	1.6		V
		Control pins	2		
V_{IL}	Low-level input voltage	Except control pins		1.4	V
		Control pins		0.8	
V_I	Input voltage		0	V_{CC}	V
V_{OH}	High-level output voltage	1A–8A		5.25	V
I_{OH}	High-level output current	B bus		−12	mA
I_{OL}	Low-level output current	B bus		12	mA
I_{OH}	High-level output current	9A–11A		−32	mA
				−60‡	
I_{OL}	Low-level output current	A bus		64	mA
				90‡	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating pins (input or A-bus I/O) must be held high or low.
‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	B port	V_{CC} = 5.25 V	I_{OH} = − 100 µA			V_{CC}−1	V
		V_{CC} = 4.75 V	I_{OH} = − 1 mA		2.4		
			I_{OH} = − 12 mA		2		
	A port	V_{CC} = 4.75 V	I_{OH} = − 1 mA			4	
			I_{OH} = − 32 mA		2.4		
			I_{OH} = − 60 mA		2		
V_{OL}	B port	V_{CC} = 4.75 V	I_{OL} = 1 mA			0.4	V
			I_{OL} = 12 mA			0.8	
	A port	V_{CC} = 4.75 V	I_{OL} = 64 mA			0.55	
			I_{OL} = 90 mA			0.9	
I_{OH}	1A−8A	V_{CC} = 4.75 V,	V_{OH} = 5.25 V			20	µA
$I_{I(hold)}$	B port	V_{CC} = 4.75 V	V_I = 0.8 V		100		µA
			V_I = 2 V		−100		
I_I	Control inputs	V_{CC} = 5.25 V,	V_I = V_{CC} or GND			±1	µA
	A or B ports					±100	
I_{OZH}†		V_{CC} = 5.25 V,	V_O = 2.4 V			10	µA
I_{OZL}†		V_{CC} = 5.25 V,	V_O = 0.4 V			−10	µA
I_{off}		V_{CC} = 0,	V_{CC}BIAS = 0	V_I or V_O ≤ 4.5 V		±100	µA
I_{CC}	A or B ports	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			mA
				Outputs low			
	9A−11A or B port			Outputs disabled			
C_i	Control inputs	V_I = 2.5 V or 0.5 V					pF
C_{io}	B port	V_O = 2.5 V or 0.5 V				9	pF
	A port	Per IEEE 1194.0-1991				9	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

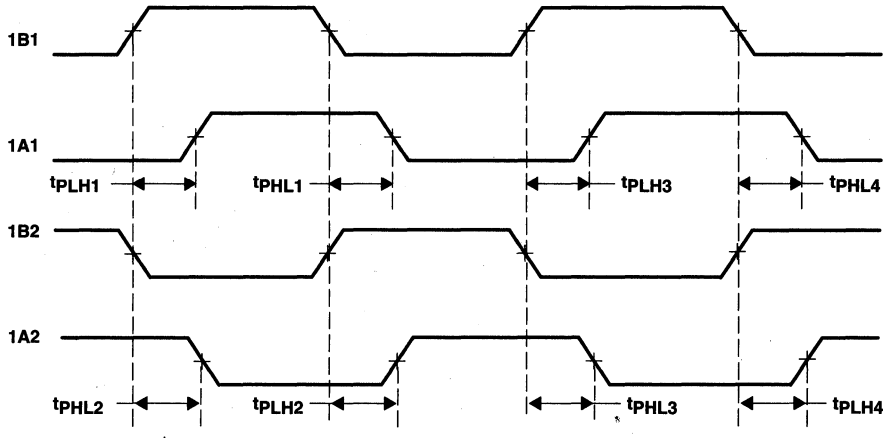
live insertion specifications over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS				MIN	TYP	MAX	UNIT
I_{CC} (V_{CC}BIAS)	V_{CC} = 0 to 4.75 V,		V_{CC}BIAS = 4.75,V to 5.25 V,	$I_{O(DC)}$ = 0			500	µA
	V_{CC} = 4.75 V to 5.25 V,		V_{CC}BIAS = 4.75 V to 5.25 V,	$I_{O(DC)}$ = 0			20	
V_O	V_{CC} = 0,		V_{CC}BIAS = 4.75 V	A port	1.3	1.5	1.7	V
I_O	V_{CC} = 0,	V_O = 0,	V_{CC}BIAS = 4.75 V	A port	−20		−100	µA
	V_{CC} = 0,	V_O = 3 V,	V_{CC}BIAS = 4.75 V		20		100	

extended output characteristics over recommended temperature and supply operating ranges (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	MIN	TYP	MAX	UNIT
$t_{sk(pr)}$†	A	B	V_{CC} = Constant, ΔT_A = 20°C				2.5	ns
	B	A		Z_O = 50 Ω, R_X = 55.6 Ω			4	
$t_{sk(load)}$†	B	A	V_{CC} = Constant, Temperature = Constant	Z_O = 50, 25, or 12.5 Ω, R_X = 55.6, 26.3, or 12.8 Ω			4	ns
t_t	B	A	Time between 1 V and 2 V	Z_O = 25 Ω, R_X = 26.3 Ω	1.2		3	ns
	A	B	Rise or fall time 10%–90%		3			

† $t_{sk(pr)} + t_{sk(load)} < 6$ ns

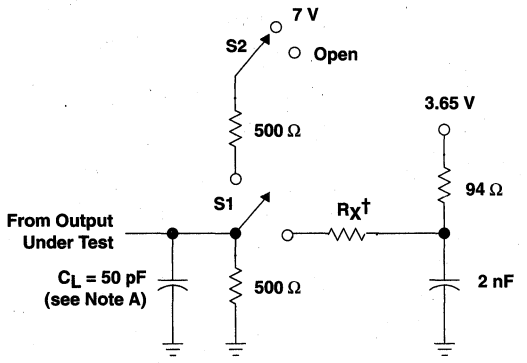


Output skew, $t_{sk(pr)}$, is calculated as the greater of the difference between the fastest and slowest of t_{PLH} and t_{PHL} (e.g., t_{PLHn}, n = 1 to 16; and t_{PHLn}, n = 1 to 16), with any combination of the inputs switching coincidently.

Figure 1. Voltage Waveforms for Extended Characteristics

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

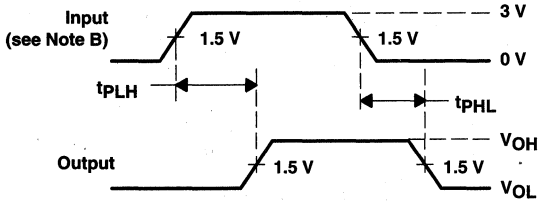


† R_X = 12.8, 26.3, 55.6 Ω

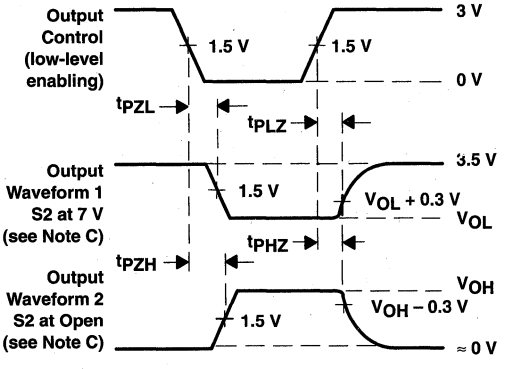
LOAD CIRCUIT FOR OUTPUTS

TEST	S1	S2
t_{PLH}/t_{PHL} (A port)	Down	X
t_{PLH}/t_{PHL} (B port)	Up	Open
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH}	Up	Open

OPEN COLLECTOR	S1	S2
t_{PHL} (see Note E)	Up	7 V
t_{PLH} (see Note F)	Up	7 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PHL} is measured at 1.5 V.
F. t_{PLH} is measured at V_{OL} + 0.3 V.

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

ABT Widebus+™

Features

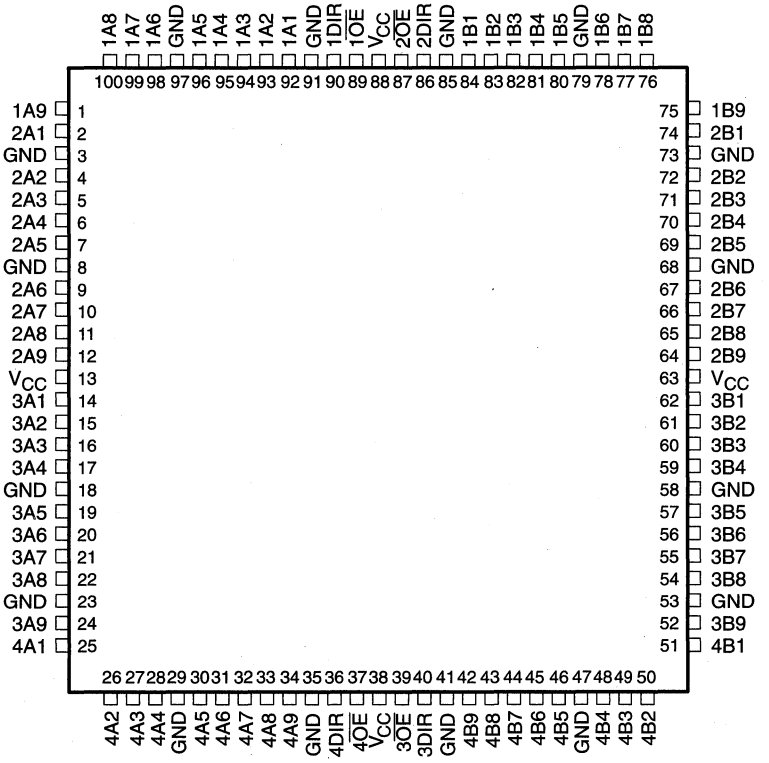
- 32- and 36-bit bus interface
- EIAJ standard 80-, 100-, and 120-pin shrink quad flat packages (SQFPs)
- Enhanced UBT™ architectures that include global controls and parity generate and check
- Multiport universal bus exchanger (UBE™) architectures
- Symmetrical flowthrough pinouts with *controls at the poles*
- Bit partitioning
- Distributed pinout with 12 GND pins and 4 V_{CC} pins
- Bus-hold circuitry
- Power-on-demand active feedback circuit
- TI has established an alternate source

Benefits

- Single-chip implementation for highest level of logic integration
- 35% less board space than equivalent PQFPs; over 50% less board space than four octal SOIC equivalents
- Special features for use in high-performance RISC/CISC/X86 microprocessor systems
- Multiplexing and memory interleaving capability for interbus communication
- Ease of board layout; provides compatible top-side or bottom-side mount
- Global, × 18-, or × 9-bit capability for flexible partitioning
- 3:1 signal-to-GND ratio minimizes simultaneous switching noise and mutual coupling effects
- Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Reduces enabled static power consumption (I_{CCL}) by over 50%
- Standardization that comes from a common product approach

- **Members of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in 100-Pin Plastic Shrink Quad Flat Packages (SQFP) With 14 × 14-mm Package Body Using 0.5-mm Lead Pitch**

SN74ABT32245 . . . PZ PACKAGE
(TOP VIEW)



description

The ′ABT32245 is a 36-bit (quad 9-bit) noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

PRODUCT PREVIEW

Widebus+ and EPIC-IIB are trademarks of Texas Instruments Incorporated.

description (continued)

This device can be used as four 9-bit transceivers, two18-bit transceivers, or one 36-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) inputs. The output-enable ($\overline{OE}$) inputs can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

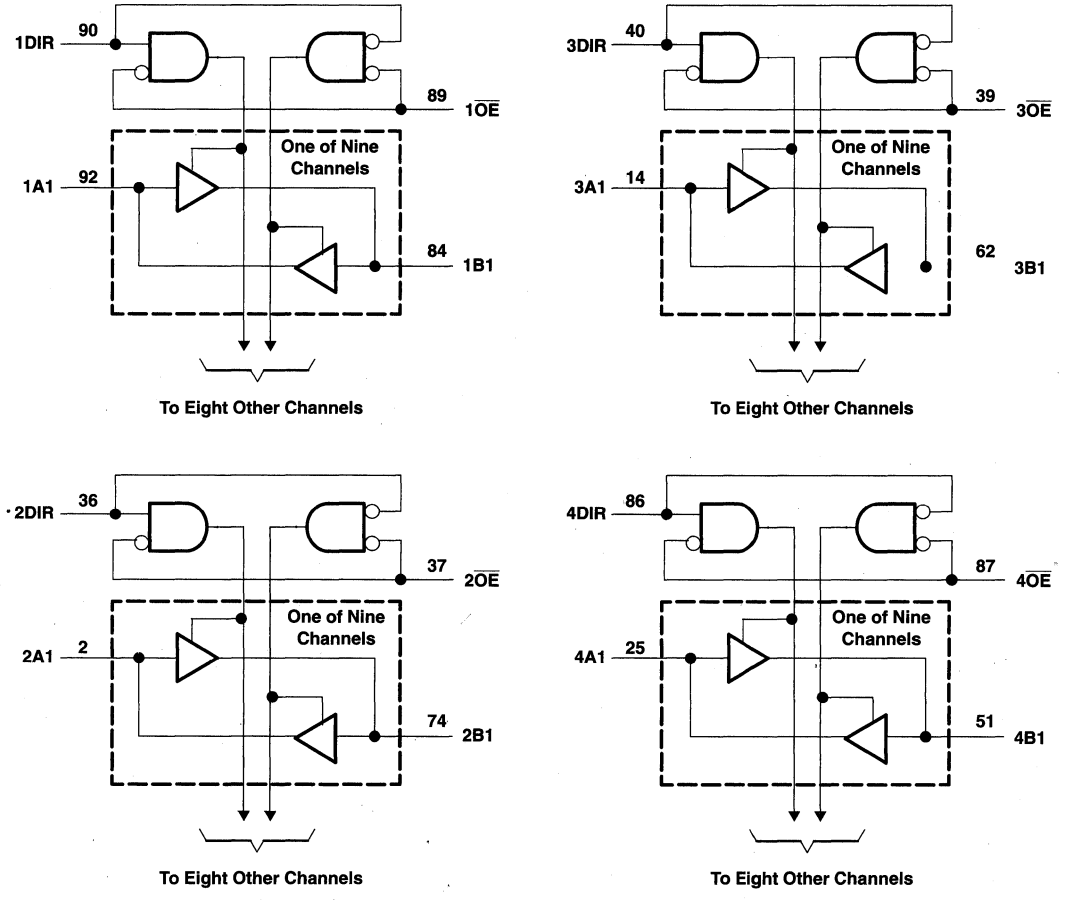
The SN54ABT32245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT32245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 9-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT32245	96 mA
SN74ABT32245	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air)	1.2 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			SN54ABT32245		SN74ABT32245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ABT32245		SN74ABT32245			UNIT
					MIN	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5		2.5			V
		V_{CC} = 5 V,	I_{OH} = −3 mA		3		3			
		V_{CC} = 4.5 V,	I_{OH} = −24 mA		2					
		V_{CC} = 4.5 V,	I_{OH} = −32 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55			0.55	V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND						±1	µA
	A or B ports								±100	
$I_{I(hold)}$	A or B ports	V_{CC} = 4.5 V,	V_I = 0.8 V				100			µA
		V_{CC} = 4.5 V,	V_I = 2 V				−100			
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V						50	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V						−50	µA
I_{off}		V_{CC} = 0,	V_I or $V_O \le$ 4.5 V						±100	µA
I_{CEX}		V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high					50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V				−50	−100	−180	mA
I_{CC}		V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high					2	mA
				Outputs low					5	
				Outputs disabled					0.5	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND							1	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V								pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V								pF

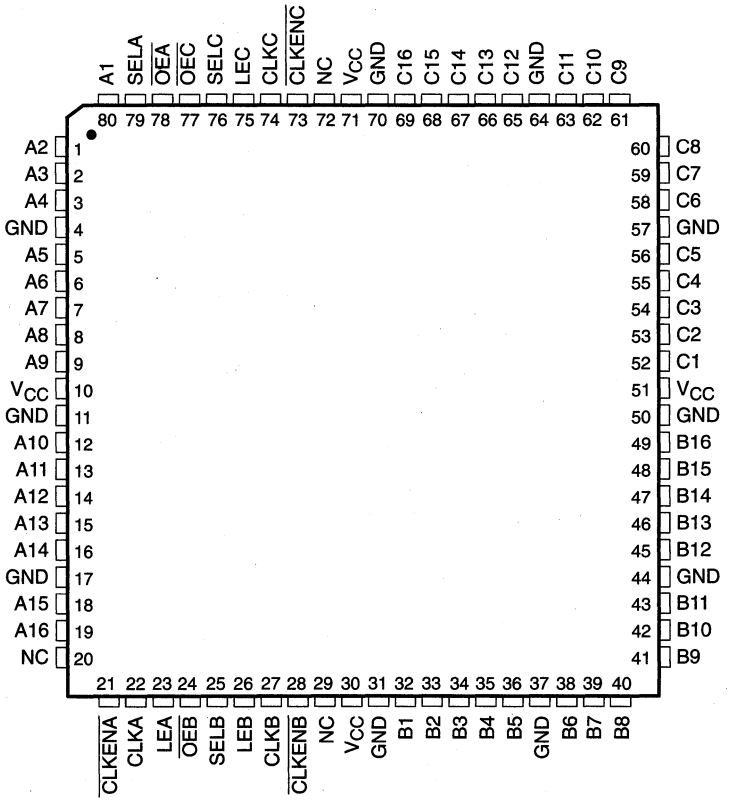
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

JUNE 1992 – REVISED MAY 1993

- **Members of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBE*™ (Universal Bus Exchanger) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in 80-Pin Plastic Shrink Quad Flat Packages (SQFP) With 12 × 12-mm Package Body Using 0.5-mm Lead Pitch**

SN74ABT32316 . . . PN PACKAGE
(TOP VIEW)



NC – No internal connection

Widebus+, EPIC-IIB, and UBE are trademarks of Texas Instruments Incorporated.

description

The 'ABT32316 consists of three 16-bit registered input/output (I/O) ports. These registers combine D-type latches and flip-flops to allow data flow in transparent, latch, and clock modes. Data from one input port can be exchanged to one or more of the other ports. Because of the universal storage element, multiple combinations of real-time and stored data can be exchanged among the three ports.

Data flow in each direction is controlled by the output-enable ($\overline{OEA}$, $\overline{OEB}$, and $\overline{OEC}$), select-control (SELA, SELB, and SELC), latch-enable (LEA, LEB, and LEC), and clock (CLKA, CLKB, and CLKC) inputs. The A data register operates in the transparent mode when LEA is high. When LEA is low, data is latched if CLKA is held at a high or low logic level. If LEA and clock-enable A ($\overline{CLKENA}$) are low, data is stored on the low-to-high transition of CLKA. Output data selection is accomplished by the select-control pins. All three ports have active-low output enables, so when the output-enable input is low, the outputs are active; when the output-enable input is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABT32316 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT32316 is characterized for operation from −40°C to 85°C.

STORAGE FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENA}}$	CLKA	LEA	A	
H	X	L	X	Q_0‡
L	↑	L	L	L
L	↑	L	H	H
X	H	L	X	Q_0‡
X	L	L	X	Q_0‡
X	X	H	L	L
X	X	H	H	H

† A-port register shown. B and C ports are similar but use $\overline{\text{CLKENB}}$, $\overline{\text{CLKENC}}$, CLKB, CLKC, LEB, and LEC.

‡ Output level before the indicated steady-state input conditions were established.

Function Tables

A-PORT OUTPUT

INPUTS		OUTPUT
$\overline{\text{OEA}}$	SELA	A
H	X	Z
L	H	Output of C register
L	L	Output of B register

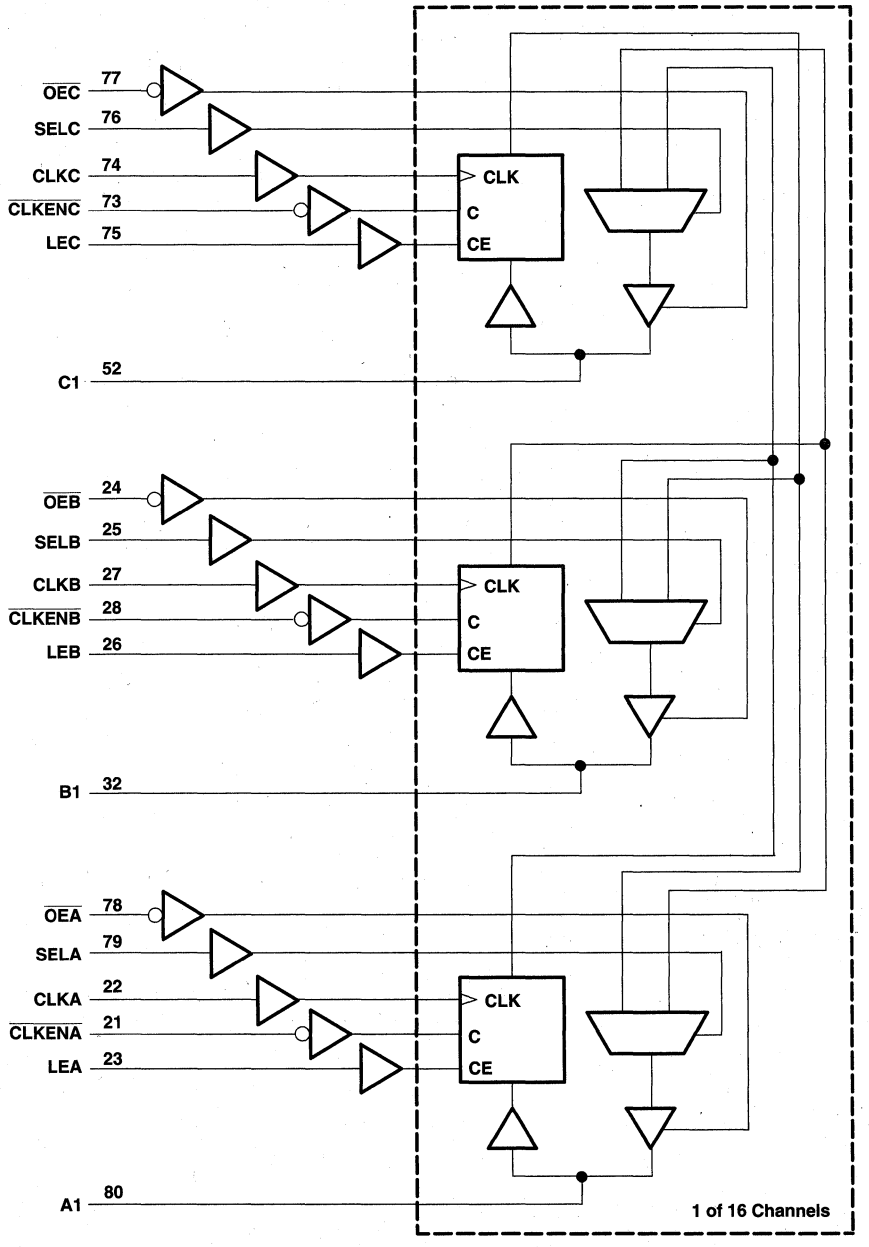
B-PORT OUTPUT

INPUTS		OUTPUT
$\overline{\text{OEB}}$	SELB	B
H	X	Z
L	H	Output of A register
L	L	Output of C register

C-PORT OUTPUT

INPUTS		OUTPUT
$\overline{\text{OEC}}$	SELC	C
H	X	Z
L	H	Output of B register
L	L	Output of A register

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT32316 ..... 96 mA
SN74ABT32316 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1.1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT32316		SN74ABT32316		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating control pins must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ABT32316		SN74ABT32316			UNIT
					MIN	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5		2.5			V
		V_{CC} = 5 V,	I_{OH} = – 3 mA		3		3			
		V_{CC} = 4.5 V,	I_{OH} = –24 mA		2					
		V_{CC} = 4.5 V,	I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND						±1	µA
	A, B, or C ports								±100	
$I_{I(hold)}$	A, B, or C ports	V_{CC} = 4.5 V,	V_I = 0.8 V				100			µA
		V_{CC} = 4.5 V,	V_I = 2 V				–100			
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V						50	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V						–50	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V						±100	µA
I_{CEX}		V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high					50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V				–50	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high					2	mA
				Outputs low					40	
				Outputs disabled					1	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND							0.5	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V						3		pF
C_{io}	A, B, or C ports	V_O = 2.5 V or 0.5 V						11.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

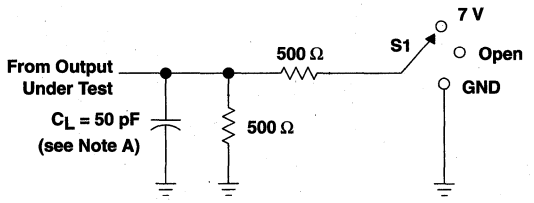
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT32316		SN74ABT32316		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	LE high	3.3		3.3		ns
		CLK high or low	3.3		3.3		
t_{su}	Setup time	A, B, or C before CLK↑	2.4		2.4		ns
		A or B before LE↓	2.1		2.1		
		$\overline{CLKEN}$ before CLK↑	3.2		3.2		
t_h	Hold time	A, B, or C after CLK↑	1.4		1.4		ns
		A or B after LE↓	2.1		2.1		
		$\overline{CLKEN}$ after CLK↑	1.1		1.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

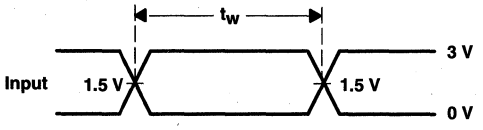
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT32316		SN74ABT32316		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
t_{PLH}	A, B, or C	C, B, or A	1.4	6.5	1.4	6.1	ns
t_{PHL}			1.1	6.8	1.1	6.6	
t_{PLH}	SEL	C, B, or A	1.4	6.7	1.4	6.5	ns
t_{PHL}			1.8	6.8	1.8	6.5	
t_{PLH}	LE	C, B, or A	2.6	8	2.6	7.5	ns
t_{PHL}			2.6	7.4	2.6	6.9	
t_{PLH}	CLK	C, B, or A	2.5	8	2.5	7.5	ns
t_{PHL}			2.5	7.2	2.5	6.7	
t_{PZH}	$\overline{OE}$	C, B, or A	1.5	6.7	1.5	6.4	ns
t_{PZL}			2.4	6.9	2.4	6.8	
t_{PHZ}	$\overline{OE}$	C, B, or A	1.5	6.1	1.5	6	ns
t_{PLZ}			1.9	6.4	1.9	6.1	

PARAMETER MEASUREMENT INFORMATION

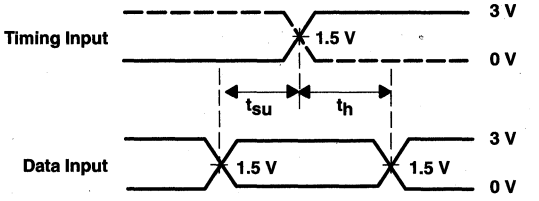


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

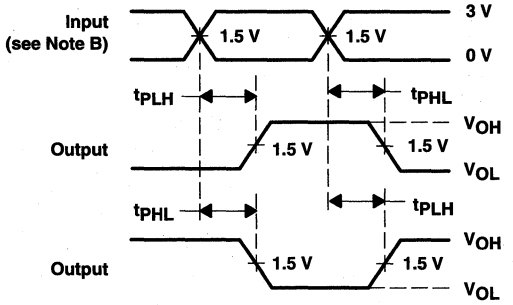
LOAD CIRCUIT FOR OUTPUTS



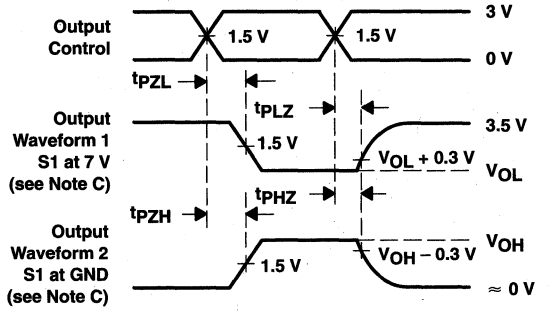
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

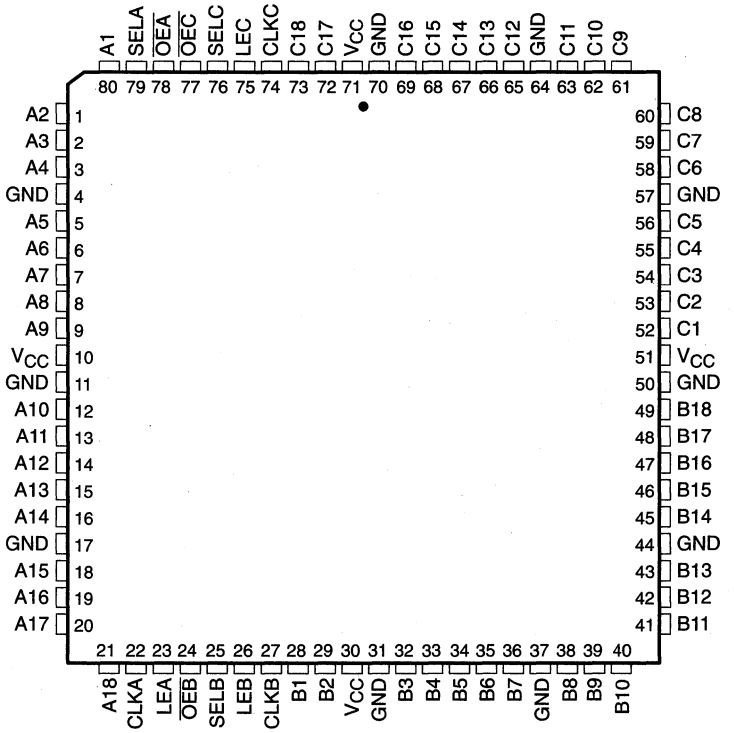
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

JUNE 1992 – REVISED JUNE 1993

- **Members of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBE*™ (Universal Bus Exchanger) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus-Hold Inputs Eliminate the Need for External Pullup/Pulldown Resistors**
- **Packaged in 80-Pin Plastic Thin Quad Flat Packages (TQFP) With 12 × 12-mm Package Body Using 0.5-mm Lead Pitch**

SN74ABT32318 . . . PN PACKAGE
(TOP VIEW)



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description

The 'ABT32318 consists of three 18-bit registered input/output (I/O) ports. These registers combine D-type latches and flip-flops to allow data flow in transparent, latch, and clock modes. Data from one input port can be exchanged to one or more of the other ports. Because of the universal storage element, multiple combinations of real-time and stored data can be exchanged among the three ports.

Data flow in each direction is controlled by the output-enable ($\overline{OEA}$, $\overline{OEB}$, and $\overline{OEC}$), select-control (SELA, SELB, and SELC), latch-enable (LEA, LEB, and LEC), and clock (CLKA, CLKB, and CLKC) inputs. The A data register operates in the transparent mode when LEA is high. When LEA is low, data is latched if CLKA is held at a high or low logic level. If LEA is low, data is stored on the low-to-high transition of CLKA. Output data selection is accomplished by the select-control pins. All three ports have active-low output enables, so when the output-enable input is low, the outputs are active; when the output-enable input is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABT32318 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT32318 is characterized for operation from −40°C to 85°C.

STORAGE FUNCTION TABLE†

INPUTS			OUTPUT
CLKA	LEA	A	
↑	L	L	L
↑	L	H	H
H	L	X	Q_0‡
L	L	X	Q_0‡
X	H	L	L
X	H	H	H

† A-port register shown. B and C ports are similar but use CLKB, CLKC, LEB, and LEC.

‡ Output level before the indicated steady-state input conditions were established.

Function Tables

A-PORT OUTPUT

INPUTS		OUTPUT
$\overline{OEA}$	SELA	A
H	X	Z
L	H	Output of C register
L	L	Output of B register

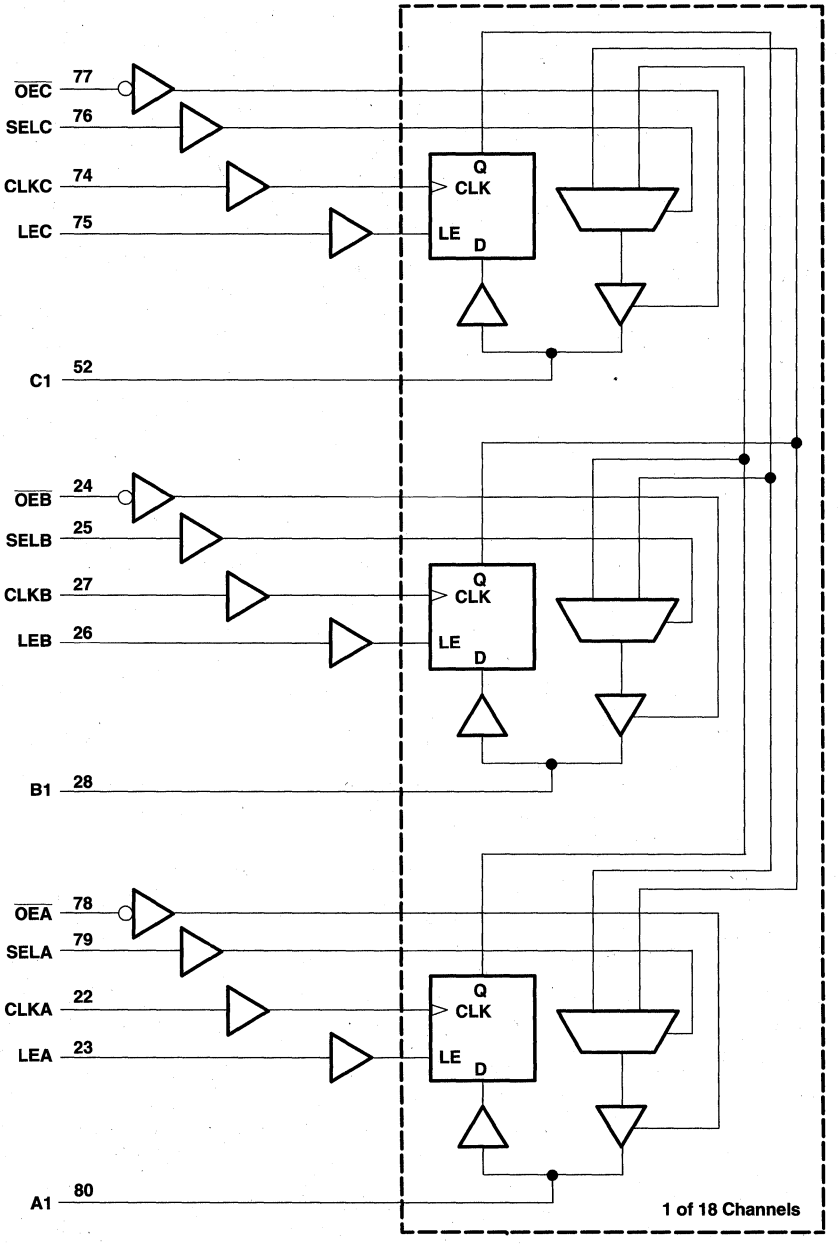
B-PORT OUTPUT

INPUTS		OUTPUT
$\overline{OEB}$	SELB	B
H	X	Z
L	H	Output of A register
L	L	Output of C register

C-PORT OUTPUT

INPUTS		OUTPUT
$\overline{OEC}$	SELC	C
H	X	Z
L	H	Output of B register
L	L	Output of A register

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT32318 ..... 96 mA
SN74ABT32318 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1.1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT32318		SN74ABT32318		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating control pins must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ABT32318		SN74ABT32318			UNIT
					MIN	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5		2.5			V
		V_{CC} = 5 V,	I_{OH} = – 3 mA		3		3			
		V_{CC} = 4.5 V,	I_{OH} = –24 mA		2					
		V_{CC} = 4.5 V,	I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55			0.55	V
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND						±1	µA
	A, B, or C ports								±100	
$I_{I(hold)}$	A, B, or C ports	V_{CC} = 4.5 V	V_I = 0.8 V				100			µA
			V_I = 2 V				–100			
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V						50	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V						–50	µA
I_{off}		V_{CC} = 0,	V_I or $V_O \leq$ 4.5 V						±100	µA
I_{CEX}		V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high					50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V				–50	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high					2	mA
				Outputs low					45	
				Outputs disabled					1	
ΔI_{CC}¶		V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,						0.5	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V						3		pF
C_{io}	A, B, or C ports	V_O = 2.5 V or 0.5 V						11.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

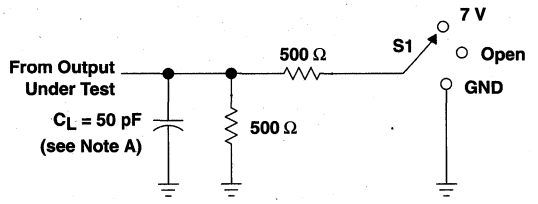
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT32318		SN74ABT32318		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration	LE high	3.3		3.3		ns
		CLK high or low	3.3		3.3		
t_{su}	Setup time	A, B, or C before CLK↑	2.4		2.4		ns
		A, B, or C before LE↓	2.1		2.1		
t_h	Hold time	A, B, or C after CLK↑	1.4		1.4		ns
		A, B, or C after LE↓	2.1		2.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

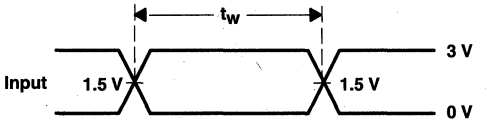
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT32318		SN74ABT32318		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
t_{PLH}	A, B, or C	C, B, or A	1.4	6.5	1.4	6.1	ns
t_{PHL}			1.1	6.8	1.1	6.6	
t_{PLH}	SEL	C, B, or A	1.4	6.7	1.4	6.5	ns
t_{PHL}			1.8	6.8	1.8	6.5	
t_{PLH}	LE	C, B, or A	2.6	8	2.6	7.5	ns
t_{PHL}			2.6	7.4	2.6	6.9	
t_{PLH}	CLK	C, B, or A	2.5	8	2.5	7.4	ns
t_{PHL}			2.5	7.2	2.5	6.7	
t_{PZH}	$\overline{OE}$	C, B, or A	1.4	6.9	1.4	6.8	ns
t_{PZL}			2.4	7.2	2.4	7.1	
t_{PHZ}	$\overline{OE}$	C, B, or A	1	6.4	1	6.2	ns
t_{PLZ}			2	6.4	2	6	

PARAMETER MEASUREMENT INFORMATION

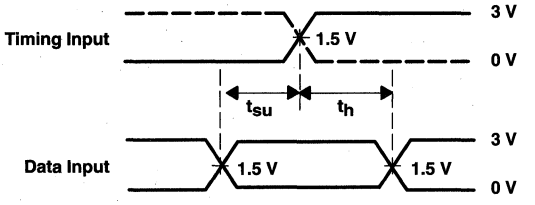


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

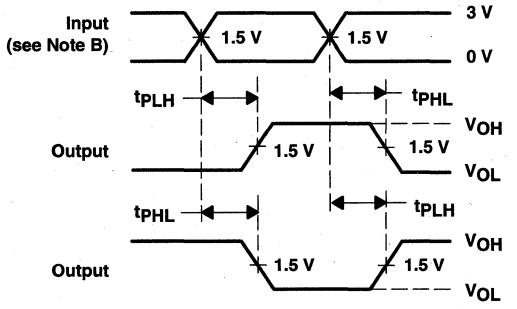
LOAD CIRCUIT FOR OUTPUTS



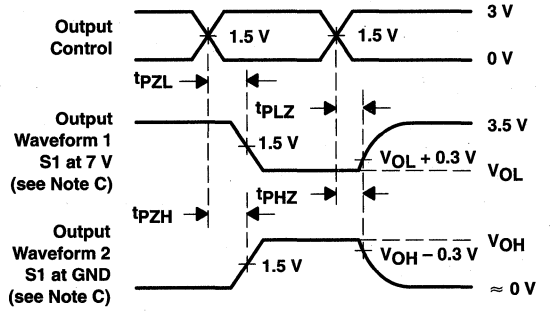
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



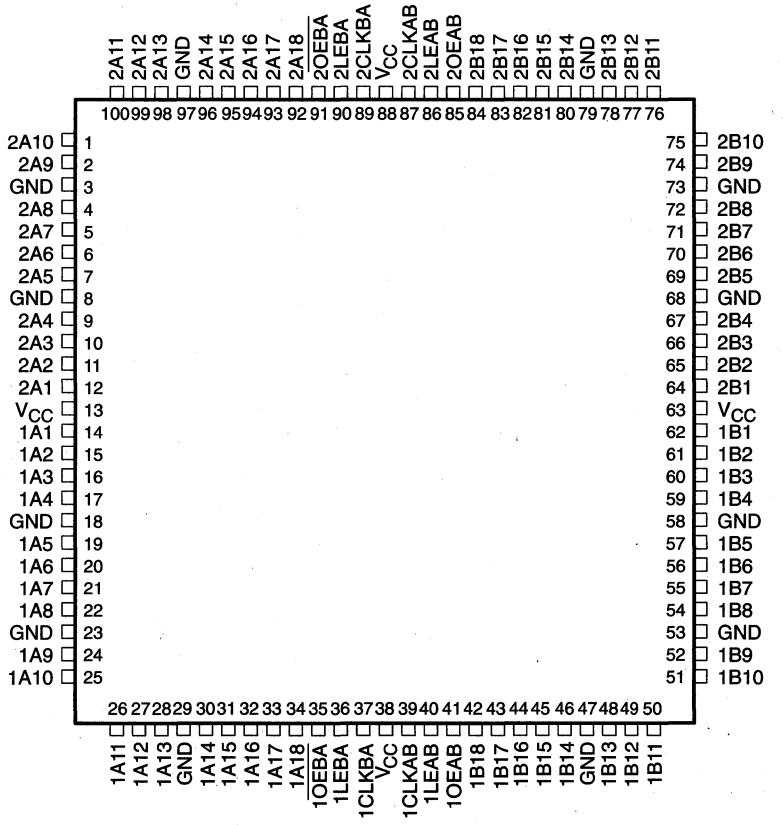
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in 100-Pin Plastic Thin Quad Flat Packages (TQFP) With 14 × 14-mm Package Body Using 0.5-mm Lead Pitch**

SN74ABT32501 . . . PZ PACKAGE
(TOP VIEW)



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description

These 36-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

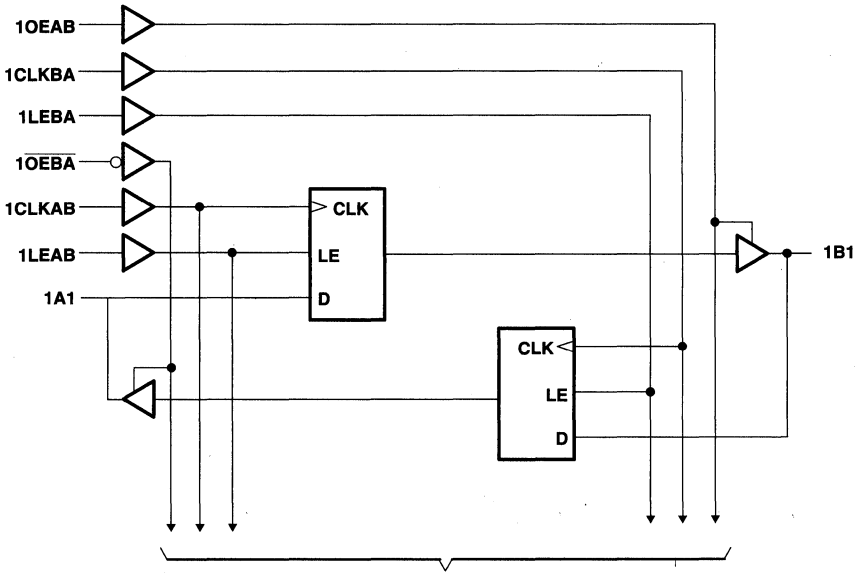
The SN54ABT32501 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT32501 is characterized for operation from −40°C to 85°C.

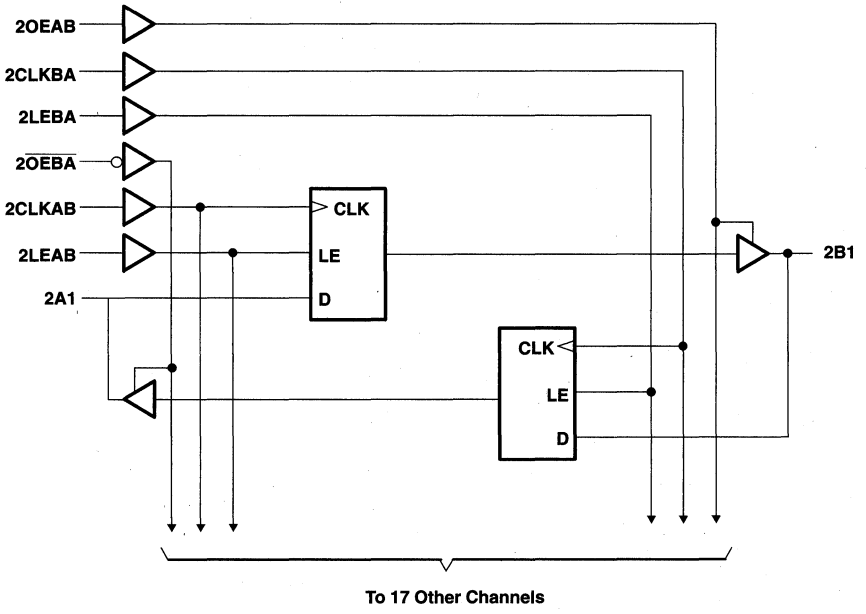
FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT32501 ..... 96 mA
SN74ABT32501 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT32501		SN74ABT32501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ABT32501		SN74ABT32501			UNIT
					MIN	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5		2.5			V
		V_{CC} = 5 V,	I_{OH} = −3 mA		3		3			
		V_{CC} = 4.5 V,	I_{OH} = −24 mA		2					
		V_{CC} = 4.5 V,	I_{OH} = −32 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55			0.55	V
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V	V_I = V_{CC}						1	µA
			V_I = GND						−5	
	A or B ports	V_{CC} = 5.5 V	V_I = V_{CC}						50	
			V_I = GND						−50	
$I_{I(hold)}$	A or B ports	V_{CC} = 4.5 V	V_I = 0.8 V					120		µA
			V_I = 2 V					−40		
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V						1	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V						−1	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V						±100	µA
I_{CEX}		V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high					50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V				−50	−100	−180	mA
I_{CC}		V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high					6	mA
				Outputs low					90	
				Outputs disabled					6	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND							1	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V						3.5		pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V						11.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

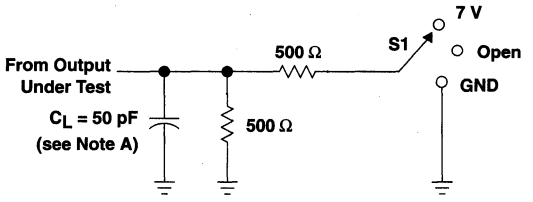
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT32501		SN74ABT32501		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				0	150	MHz
t_w	Pulse duration	LE high			3.3		ns
		CLK high or low			3.3		
t_{su}	Setup time	A or B before CLK↑			3.5		ns
		A or B before LE↓			1.6		
t_h	Hold time	A or B after CLK↑			0		ns
		A or B after LE↓			1.6		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

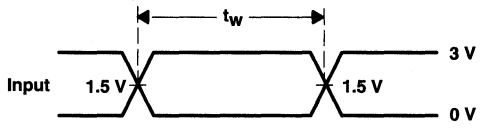
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT32501			SN74ABT32501			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}						150			MHz
t_{PLH}	A or B	B or A				1.3	2.9	4.8	ns
t_{PHL}						1.4	2.7	5.4	
t_{PLH}	LEAB or LEBA	B or A				1.6	3.4	5.3	ns
t_{PHL}						1.9	3.6	5.5	
t_{PLH}	CLKAB or CLKBA	B or A				1.5	3.2	5.3	ns
t_{PHL}						1.7	3.3	5.4	
t_{PZH}	OEAB or $\overline{OEBA}$	B or A				1.2	3.2	5.6	ns
t_{PZL}						1.5	3.6	6	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A				1.8	3.6	5.9	ns
t_{PLZ}						1.7	3.5	5.6	

PARAMETER MEASUREMENT INFORMATION

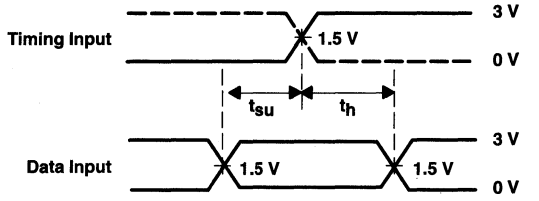


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

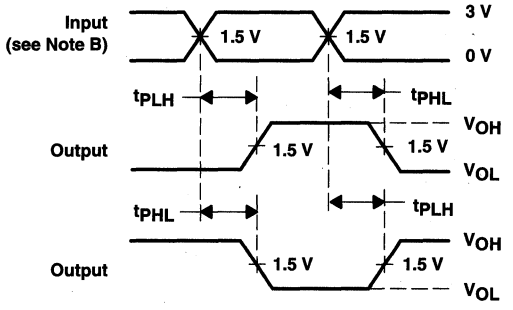
LOAD CIRCUIT FOR OUTPUTS



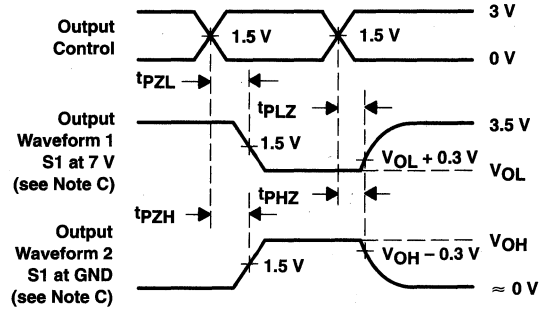
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



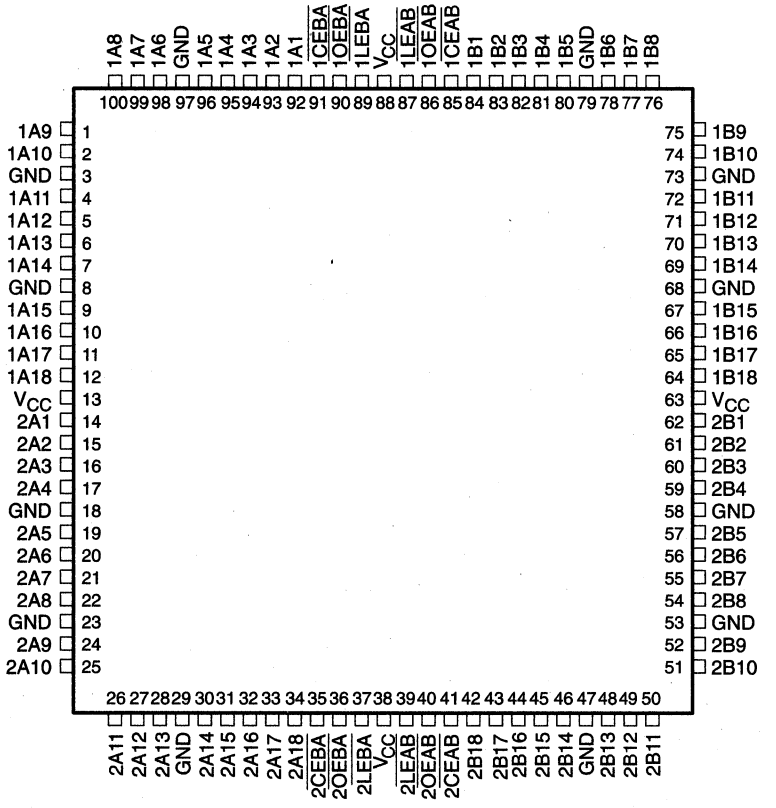
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in 100-Pin Plastic Shrink Quad Flat Packages (SQFP) With 14 × 14-mm Package Body Using 0.5-mm Lead Pitch**

SN74ABT32543 . . . PZ PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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description

The 'ABT32543 is a 36-bit registered transceiver that contains two sets of D-type latches for temporary storage of data flowing in either direction. The device can be used as two 18-bit transceivers or one 36-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABT32543 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT32543 is characterized for operation from −40°C to 85°C.

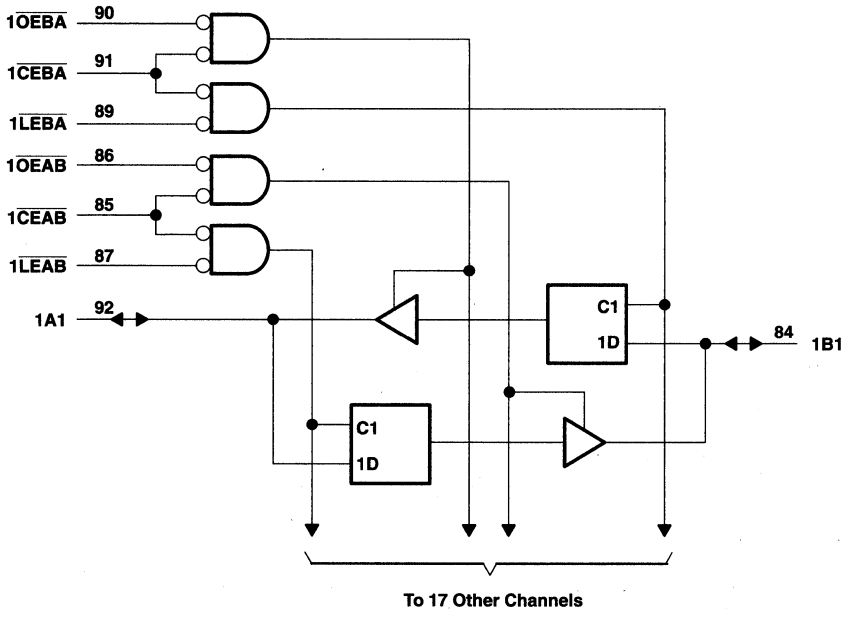
FUNCTION TABLE†
(each 18-bit section)

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT32543 ..... 96 mA
SN74ABT32543 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			SN54ABT32543		SN74ABT32543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ABT32543		SN74ABT32543			UNIT
					MIN	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5		2.5			V
		V_{CC} = 5 V,	I_{OH} = −3 mA		3		3			
		V_{CC} = 4.5 V,	I_{OH} = −24 mA		2					
		V_{CC} = 4.5 V,	I_{OH} = −32 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55			0.55	V
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND						±1	µA
	A or B ports								±100	
$I_{I(hold)}$	A or B ports	V_{CC} = 4.5 V	V_I = 0.8 V				100			µA
			V_I = 2 V				−100			
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V						50	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V						−50	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V						±100	µA
I_{CEX}		V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high					50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V				−50	−100	−180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high					2	mA
				Outputs low					5	
				Outputs disabled					0.5	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND							1	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V								pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V								pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- Members of the Texas Instruments *Widebus+*™ Family
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation
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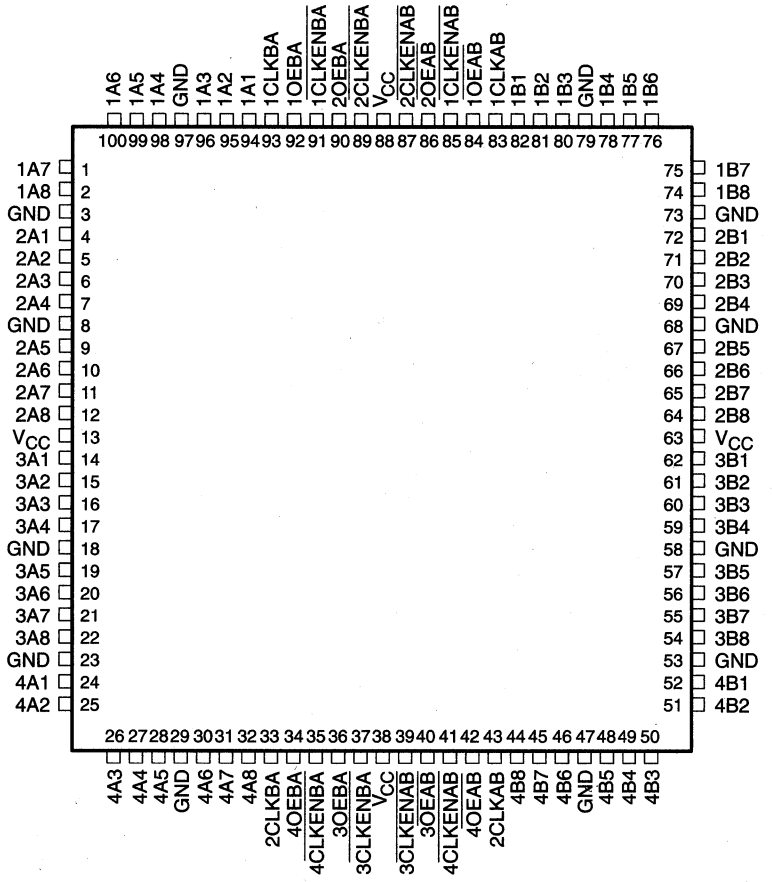
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in 100-Pin Plastic Shrink Quad Flat Packages (SQFP) With 14 × 14-mm Package Body Using 0.5-mm Lead Pitch

SN74ABT32952 . . . PZ PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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description

The 'ABT32952 is a 32-bit (quad 8-bit) transceiver with edge-triggered D-type flip-flops and 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The 'ABT32952 can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. Provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low on the positive transition of the clock (CLKAB or CLKBA) input, the output (B or A) of the flip-flop takes on the logic level set up at the input (A or B). The 'ABT32952 allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable inputs.

A buffered output-enable ($\overline{\text{OEAB}}$ or OEBA) input can be used to place the 32 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable ($\overline{\text{OEAB}}$ or OEBA) does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (A to B). OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (B to A).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABT32952 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT32952 is characterized for operation from −40°C to 85°C.

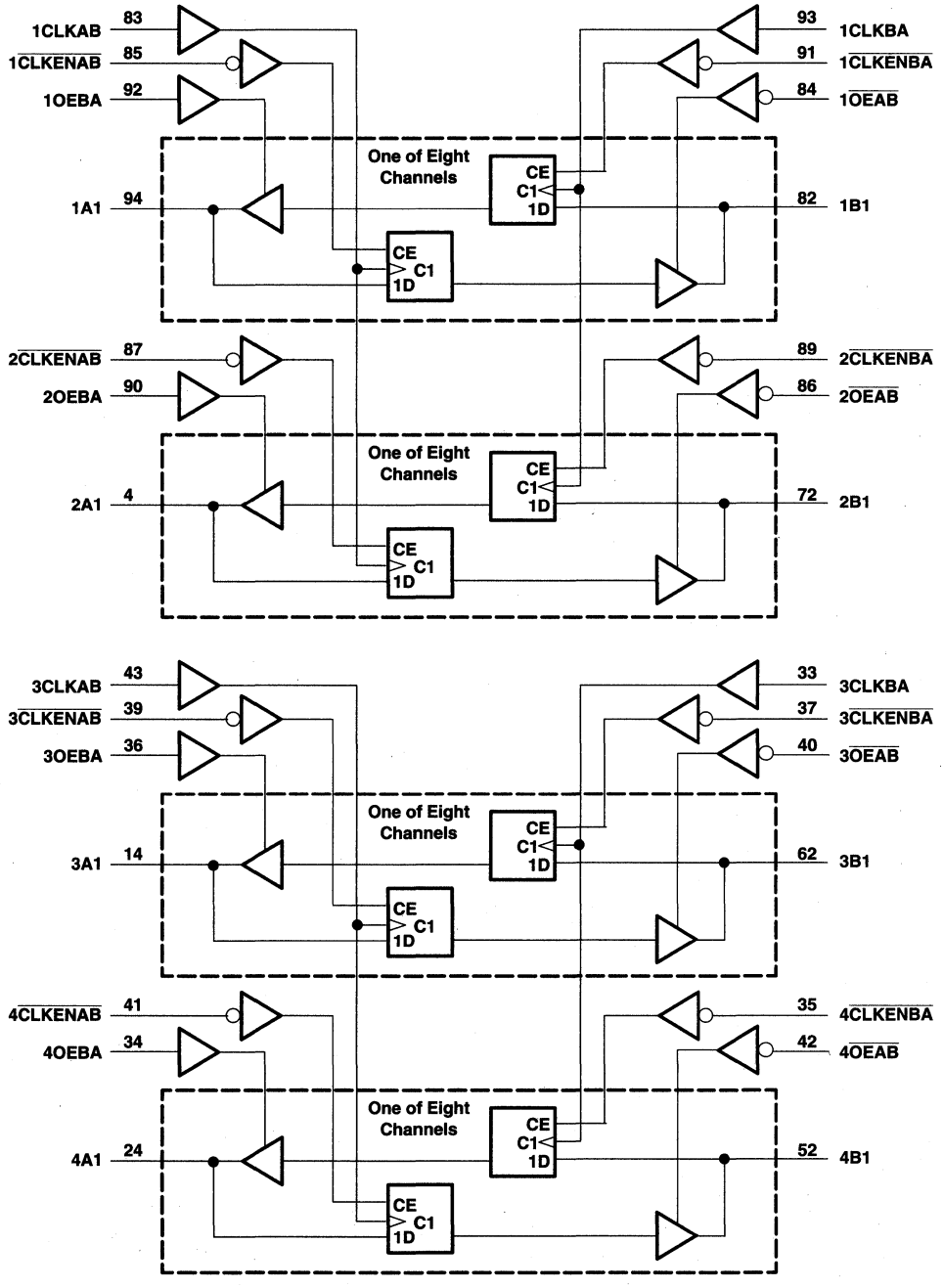
FUNCTION TABLE†
(each flip-flop)

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	CLKAB	A	B
L	L	↑	H	H
L	L	↑	L	L
H	L	X	X	Q_0
X	L	L	X	Q_0
X	H	X	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{CLKENBA}}$, OEBA, and CLKBA.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT32952 ..... 96 mA
SN74ABT32952 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			SN54ABT32952		SN74ABT32952		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ABT32952		SN74ABT32952			UNIT
					MIN	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5		2.5			V
		V_{CC} = 5 V,	I_{OH} = −3 mA		3		3			
		V_{CC} = 4.5 V,	I_{OH} = −24 mA		2					
		V_{CC} = 4.5 V,	I_{OH} = −32 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55			0.55	V
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND						±1	µA
	A or B ports								±100	
$I_{I(hold)}$	A or B ports	V_{CC} = 4.5 V	V_I = 0.8 V				100			µA
			V_I = 2 V				−100			
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V						50	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V						−50	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V						±100	µA
I_{CEX}		V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high					50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V				−50	−100	−180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high					2	mA
				Outputs low					5	
				Outputs disabled					0.5	
ΔI_{CC}¶	CLK inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND							1.5	mA
	Others								0.5	
C_i	Control inputs	V_I = 2.5 V or 0.5 V								pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V								pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

ABT MEMORY DRIVERS

Features

- Output ports have 25-Ω series resistors included on chip
- Octal, Widebus™ and Widebus+™ functional equivalents with complete pinout and package compatibility
- 8-, 9-, 10-, 11-, and 12-bit options
- 16-, 18-, 20-, 32-, and 36-bit options
- Typical V_{OLV} (voltage output low-level valley) < 0.5 V at V_{CC} = 5 V, T_A = 25°C
- Symmetrical, balanced output-drive capability of 12 mA

Benefits

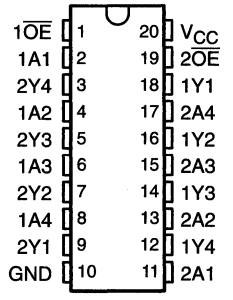
- Reduce component count and save valuable board space
- Drop-in replaceable series resistor options with characteristic ABT advanced system performance and minimal system power
- Reliably drive address lines of 64K, 256K, 1M, 4M, and 16M MOS dynamic random access memories (DRAMs)
- Highly integrated, undershoot-dampened line drivers for advanced lump load transmission conditions
- Reduced output undershoot experienced at the receiver input for increased system reliability
- Equivalent output high and low current levels optimally drive highly capacitive inputs

The following table lists ABT memory driver devices currently being evaluated for market introduction. Customers interested in learning more about TI's plans for these devices should contact the Advanced System Logic Marketing hotline at (214) 997-5202.

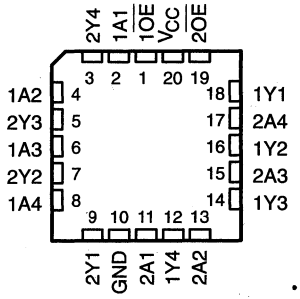
DEVICE	PIN COUNT	DESCRIPTION
'ABT2540	20	Octal Memory Driver
'ABT2541	20	Octal Memory Driver
'ABT2620	20	Octal Memory Driver
'ABT2623	20	Octal Memory Driver
'ABT2640	20	Octal Memory Driver
'ABT2827	24	10-Bit Inverting Memory Driver
'ABT2863	24	9-Bit Memory Driver
'ABT5410	24	12-Bit Memory Driver
'ABT5411	24	12-Bit Memory Driver
'ABT5412	24	12-Bit Memory Driver
'ABT5413	24	12-Bit Memory Driver
'ABT162241	48	Noninverting 16-Bit Buffer/Driver With Series Output Resistors
'ABT162825	56	Noninverting 18-Bit Buffer/Driver With Series Output Resistors
'ABT162827	56	Noninverting 20-Bit Buffer/Driver With Series Output Resistors
'ABT162861	56	Noninverting 20-Bit Transceiver With Series Output Resistors
'ABT162863	56	Noninverting 18-Bit Transceiver With Series Output Resistors
'ABT322245	100	36-Bit Bus Transceiver With Series Output Resistors
'ABT322316	80	16-Bit Tri-Port Universal Bus Exchanger With Series Output Resistors
'ABT322318	80	18-Bit Tri-Port Universal Bus Exchanger With Series Output Resistors
'ABT322501	100	36-Bit Universal Bus Transceiver With Series Output Resistors
'ABT322543	100	36-Bit Registered Bus Transceiver With Series Output Resistors

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT2240 . . . J PACKAGE
SN74ABT2240 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT2240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT2241 and 'ABT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs. These devices feature high fan-out and improved fan-in.

The 'ABT2240 is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT2240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

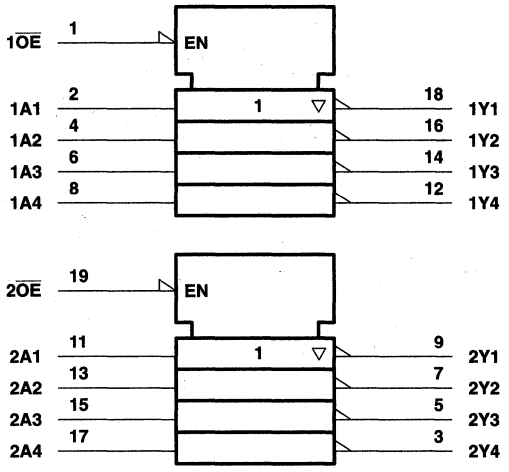
The SN54ABT2240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT2240 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

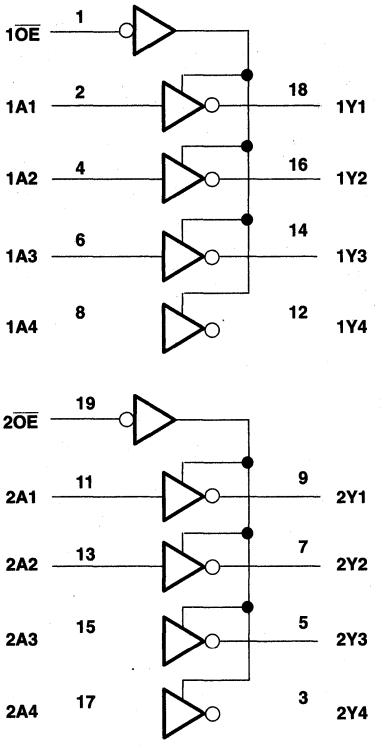
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†

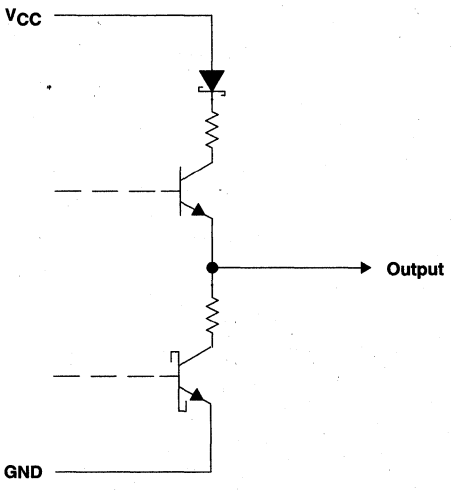


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of Y outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT2240		SN74ABT2240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

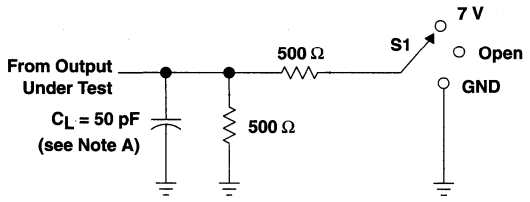
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT2240		SN74ABT2240		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA				0.8		0.8		0.8	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

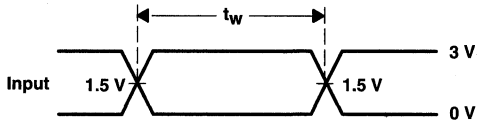
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2240		SN74ABT2240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3	4	1	5	1	4.9	ns
t_{PHL}			3	4.8	5.8	3	6.1	3	6	
t_{PZH}	$\overline{OE}$	Y	1.5	3.7	4.7	1.5	6.1	1.5	5.8	ns
t_{PZL}			4.2	6.5	7.6	4.2	8.6	4.2	8.4	
t_{PHZ}	$\overline{OE}$	Y	1.9	3.8	5	1.9	5.7	1.9	5.6	ns
t_{PLZ}			2.5	4.7	5.8	2.5	6.9	2.5	6.4	

PARAMETER MEASUREMENT INFORMATION

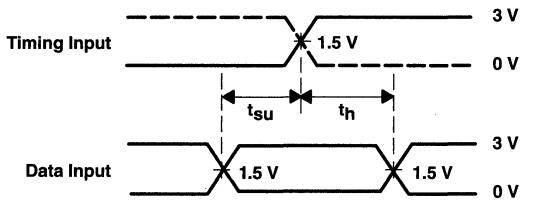


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

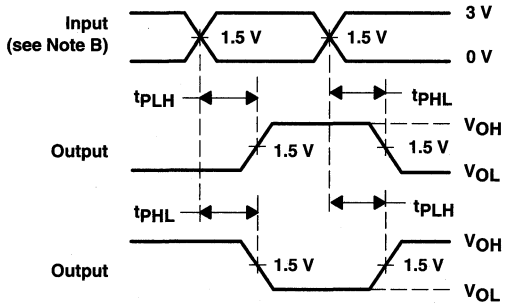
LOAD CIRCUIT FOR OUTPUTS



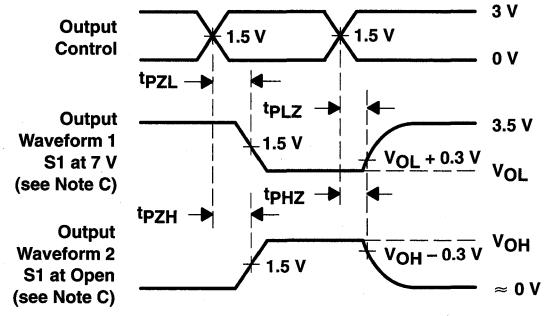
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



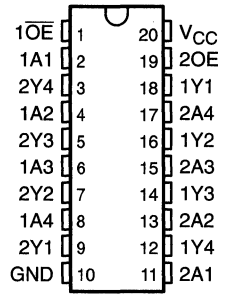
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

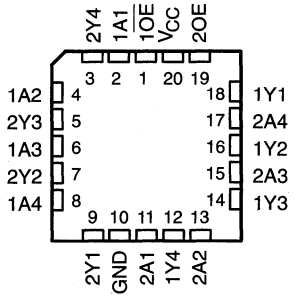
Figure 1. Load Circuit and Voltage Waveforms

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT2241 . . . J PACKAGE
SN74ABT2241 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT2241 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT2240 and 'ABT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs. These devices feature high fan-out and improved fan-in.

The outputs, which are designed to sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT2241 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2241 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT2241 is characterized for operation from −40°C to 85°C.

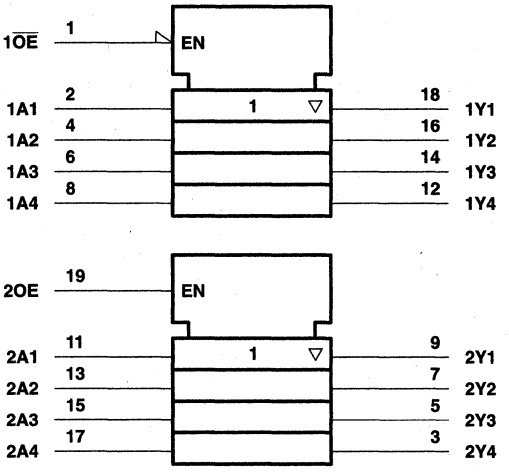
EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

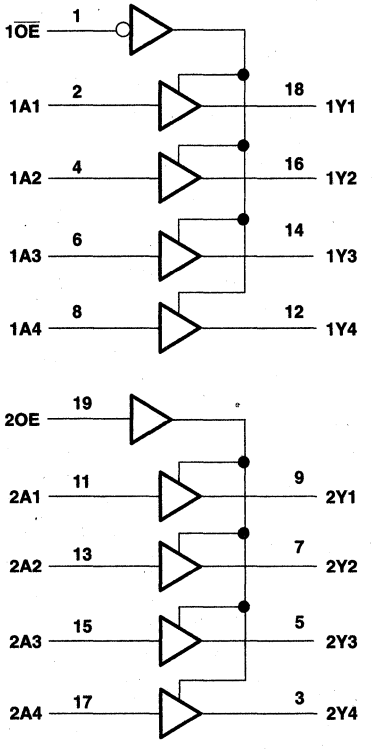
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†

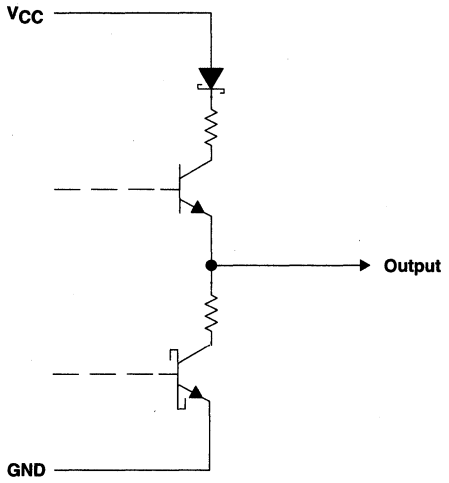


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, and N packages.

logic diagram (positive logic)



schematic of Y outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT2241		SN74ABT2241		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

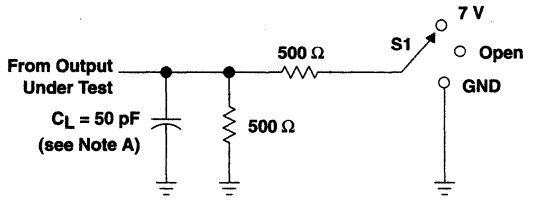
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT2241		SN74ABT2241		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA				0.8		0.8		0.8	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

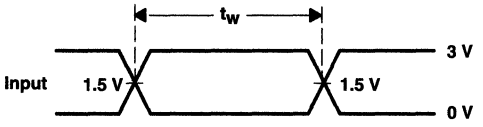
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2241		SN74ABT2241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3	4.3	1	4.8	1	4.7	ns
t_{PHL}			1	4.3	5.3	1	5.7	1	5.6	
t_{PZH}	OE or $\overline{OE}$	Y	1.1	3.5	4.8	1.1	6.1	1.1	5.8	ns
t_{PZL}			2.1	6.2	7.6	2.1	8.6	2.1	8.4	
t_{PHZ}	OE or $\overline{OE}$	Y	1.7	4.2	5.6	1.7	6.7	1.7	6.6	ns
t_{PLZ}			1.7	3.9	5.8	1.7	6.9	1.7	6.4	

PARAMETER MEASUREMENT INFORMATION

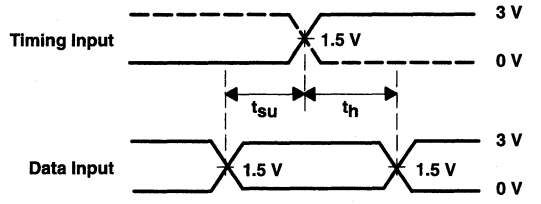


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

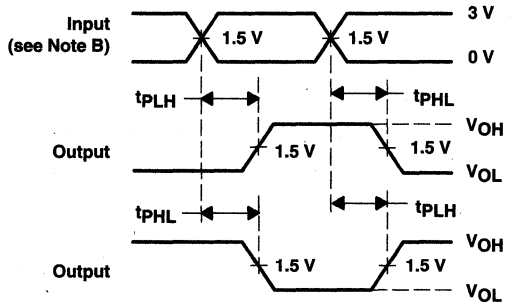
LOAD CIRCUIT FOR OUTPUTS



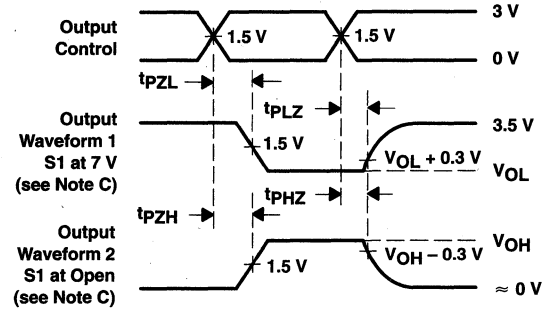
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



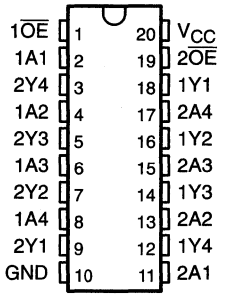
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

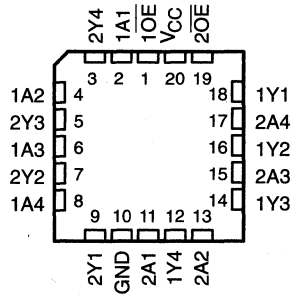
Figure 1. Load Circuit and Voltage Waveforms

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT2244 . . . J PACKAGE
SN74ABT2244 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT2244 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT2240 and 'ABT2241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs. These devices feature high fan-out and improved fan-in.

The outputs, which are designed to sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT2244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

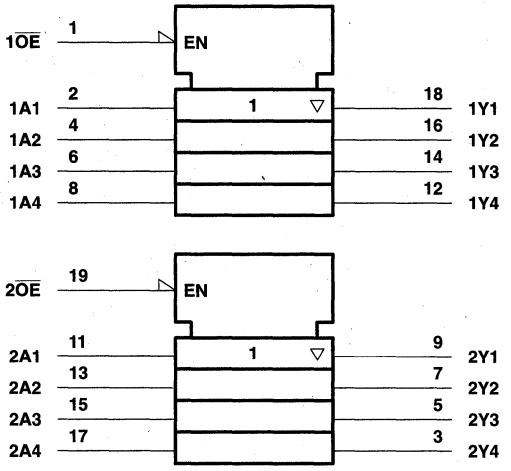
The SN54ABT2244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT2244 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

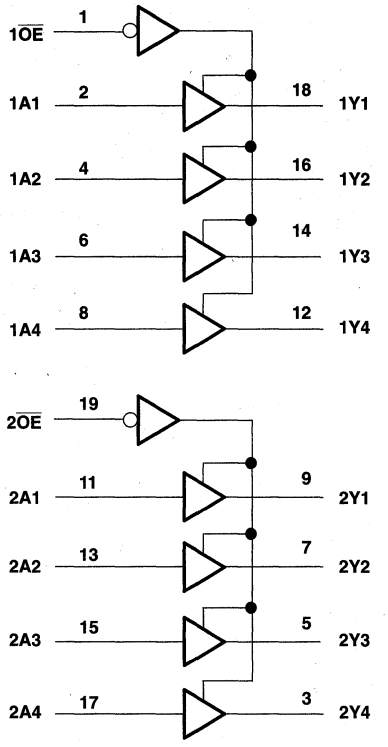
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†

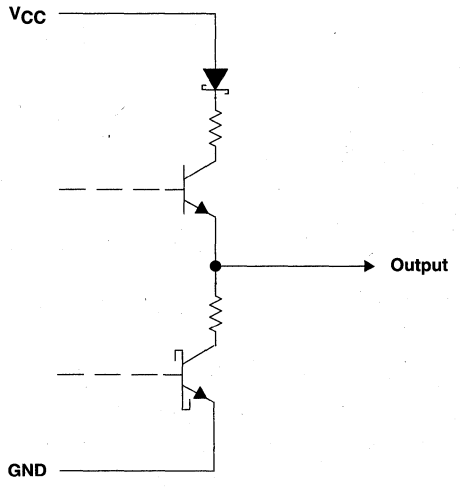


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of Y outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT2244		SN74ABT2244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

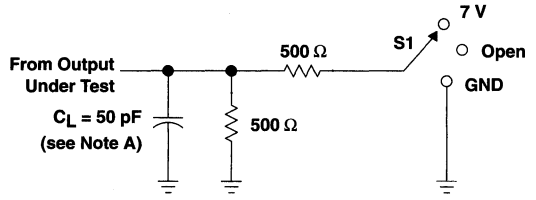
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT2244		SN74ABT2244		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA				0.8		0.8		0.8	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

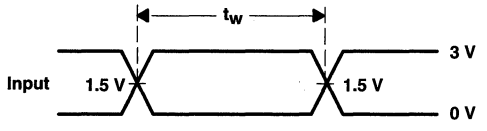
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2244		SN74ABT2244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3.4	4.3	1	5.3	1	4.7	ns
t_{PHL}			1	4.5	5.3	1	6.8	1	5.6	
t_{PZH}	$\overline{OE}$	Y	1.1	3.8	4.8	1.1	6.5	1.1	5.5	ns
t_{PZL}			2.1	6.3	7.3	2.1	10.2	2.1	8.3	
t_{PHZ}	$\overline{OE}$	Y	2.1	4.5	5.6	2.1	7	2.1	6.6	ns
t_{PLZ}			1.7	4.3	5.3	1.7	7.4	1.7	5.8	

PARAMETER MEASUREMENT INFORMATION

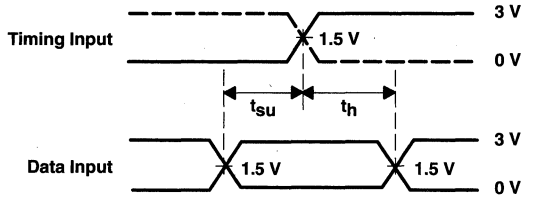


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

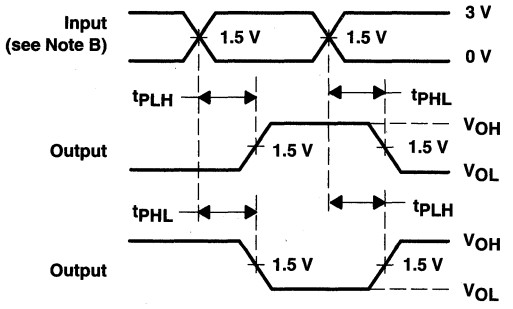
LOAD CIRCUIT FOR OUTPUTS



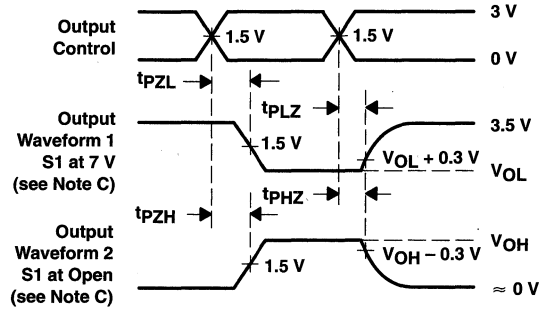
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



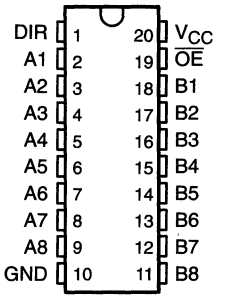
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

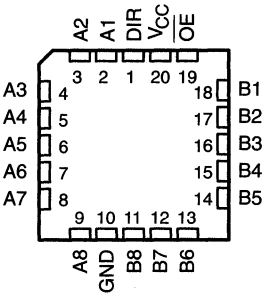
Figure 1. Load Circuit and Voltage Waveforms

- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT2245 . . . J PACKAGE
SN74ABT2245 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT2245 . . . FK PACKAGE
(TOP VIEW)



description

These octal transceivers and line drivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The A-port outputs, which are designed to sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT2245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT2245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

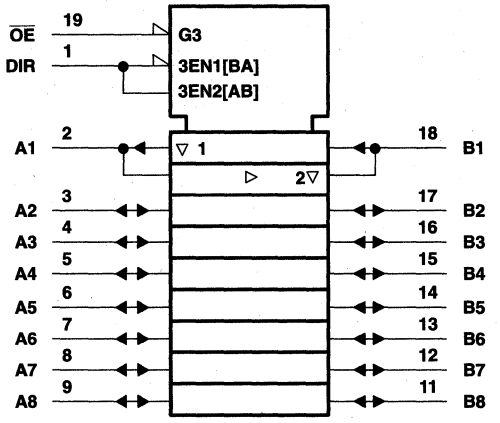
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

EPIC-IIB is a trademark of Texas Instruments Incorporated.

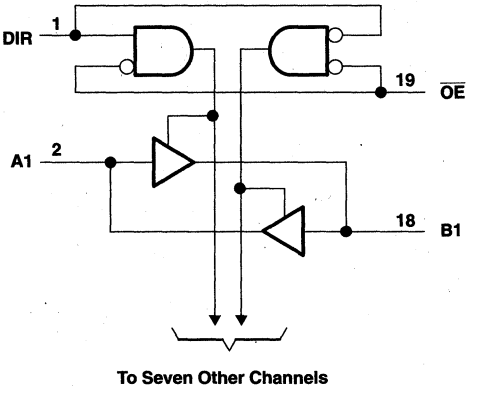
PRODUCT PREVIEW

logic symbol†

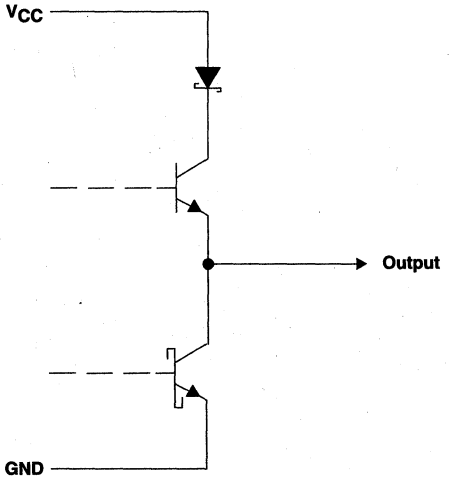


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

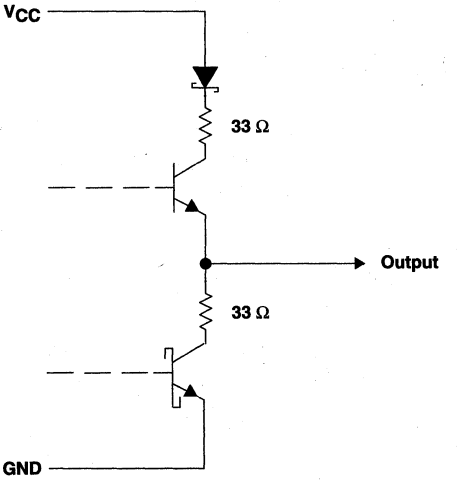
logic diagram (positive logic)



schematic of A-port outputs



schematic of B-port outputs



All resistor values shown are nominal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT2245 (except B port) ..... 96 mA
SN74ABT2245 (except B port) ..... 128 mA
B port ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
N package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT2245		SN74ABT2245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

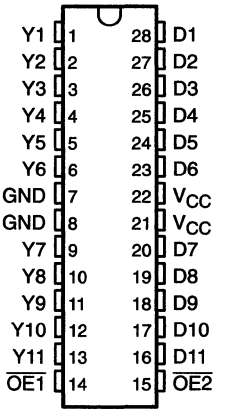
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT2245		SN74ABT2245		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 12 mA	B port			0.8		0.8		0.8	V
		I_{OL} = 48 mA	A port			0.55		0.55			
		I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V										pF
C_{io}	V_O = 2.5 V or 0.5 V										pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

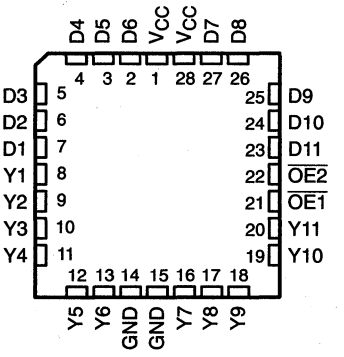
PRODUCT PREVIEW

- **Output Ports Have 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Typical V_{OLV} (Output Undershoot) < 0.5 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs**

SN54ABT5400 . . . JT PACKAGE
SN74ABT5400 . . . DW PACKAGE
(TOP VIEW)



SN54ABT5400 . . . FK PACKAGE
(TOP VIEW)



description

These 11-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all 11 outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

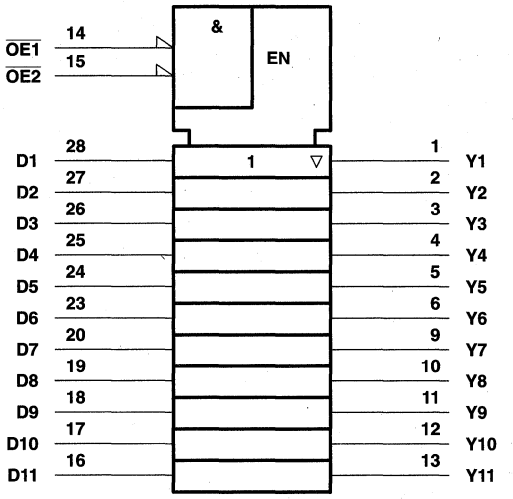
The SN54ABT5400 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT5400 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	D	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

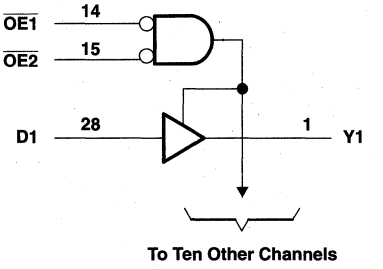
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW and JT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DW package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT5400		SN74ABT5400		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT5400		SN74ABT5400		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA		3.35	3.7		3.3		3.35		V
	V_{CC} = 5 V,	I_{OH} = −1 mA		3.85	4.2		3.8		3.85		
	V_{CC} = 4.5 V,	I_{OH} = −3 mA					3		3.1		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA		2.6					2.6		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA						0.8		0.65	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA								0.8	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O	V_{CC} = 5.5 V,	V_O = 2.5 V		−25	−45	−100	−25	−100	−25	−100	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0		−50		−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		5	50		50		50	µA
			Outputs low		36	45		45		45	mA
			Outputs disabled		1	50		50		50	µA
ΔI_{CC}§	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT5400		SN74ABT5400		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Y	2	4.5	5.7	2	6.7	2	6.5	ns
t_{PHL}			1.5	3.7	4.5	1.5	5.5	1.5	5.2	
t_{PZH}	$\overline{OE}$	Y	2.5	5.7	6.6	2.5	8.6	2.5	8.5	ns
t_{PZL}			2	4.4	5.5	2	6.9	2	6.8	
t_{PHZ}	$\overline{OE}$	Y	1.5	3.6	4.4	1.5	5.5	1.5	5.2	ns
t_{PLZ}			1.5	4.2	5.4	1.5	7.4	1.5	6.9	

TEXAS INSTRUMENTS
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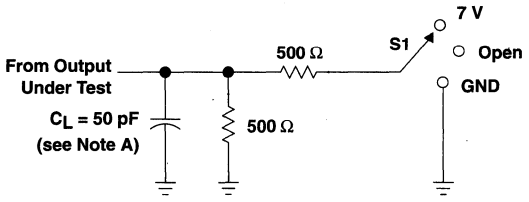
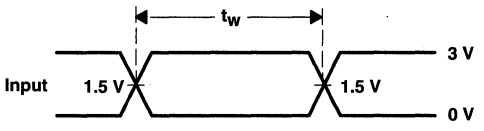
PARAMETER MEASUREMENT INFORMATION

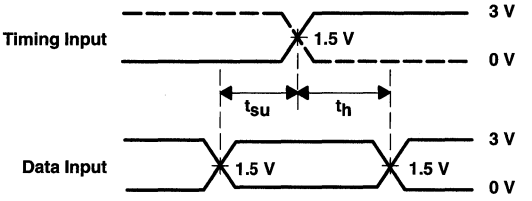


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

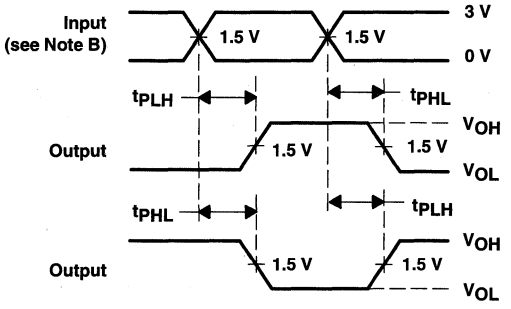
LOAD CIRCUIT FOR OUTPUTS



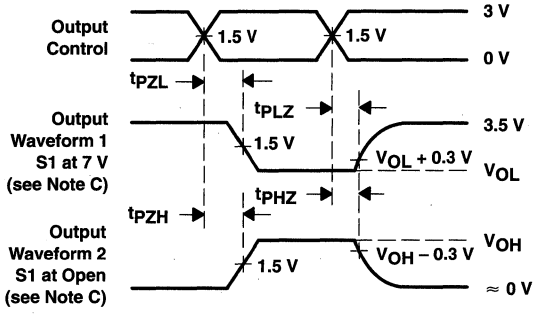
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



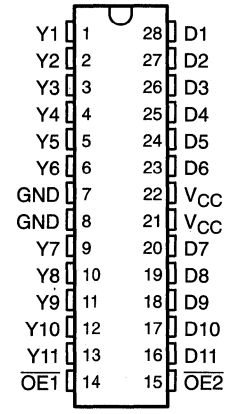
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

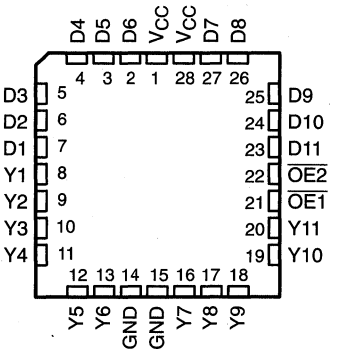
Figure 1. Load Circuit and Voltage Waveforms

- **Output Ports Have 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Typical V_{OLV} (Output Undershoot) < 0.5 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs**

SN54ABT5401 . . . JT PACKAGE
SN74ABT5401 . . . DW PACKAGE
(TOP VIEW)



SN54ABT5401 . . . FK PACKAGE
(TOP VIEW)



description

These 11-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all 11 outputs are in the high-impedance state. These devices provide inverted data.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

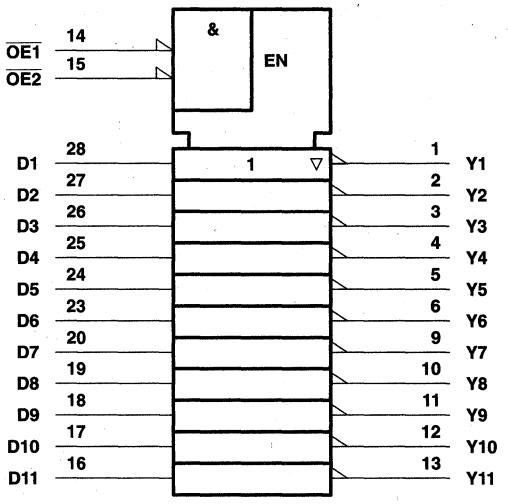
The SN54ABT5401 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT5401 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	D	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

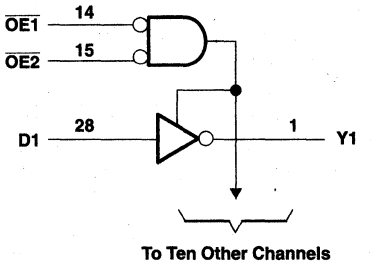
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW and JT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DW package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT5401		SN74ABT5401		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

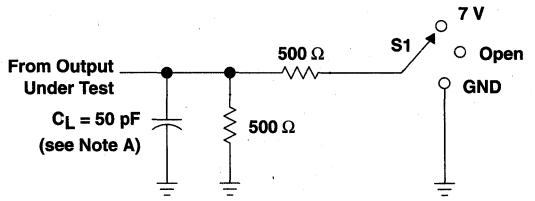
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT5401		SN74ABT5401		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −1 mA			3.35	3.7		3.3		3.35		V
	V_{CC} = 5 V, I_{OH} = −1 mA			3.85	4.2		3.8		3.85		
	V_{CC} = 4.5 V, I_{OH} = −3 mA						3		3.1		
	V_{CC} = 4.5 V, I_{OH} = −12 mA			2.6					2.6		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA							0.8		0.65	V
	V_{CC} = 4.5 V, I_{OL} = 12 mA									0.8	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND					±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V					−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O	V_{CC} = 5.5 V, V_O = 2.5 V			−25	−45	−100	−25	−100	−25	−100	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0			−50		−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		5	50		50		50	µA
			Outputs low		36	45		45		45	mA
			Outputs disabled		1	50		50		50	µA
ΔI_{CC}§	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

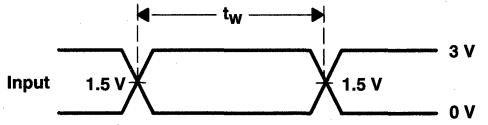
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT5401		SN74ABT5401		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Y	2	4.5	6.1	2	7	2	6.9	ns
t_{PHL}			1.5	4.4	5.2	1.5	5.9	1.5	5.7	
t_{PZH}	$\overline{OE}$	Y	2.5	5.7	6.6	2.5	8.6	2.5	8.5	ns
t_{PZL}			2	4.4	5.5	2	6.9	2	6.8	
t_{PHZ}	$\overline{OE}$	Y	1.5	3.6	4.4	1.5	5.5	1.5	5.2	ns
t_{PLZ}			1.5	4.2	5.4	1.5	7.4	1.5	6.9	

PARAMETER MEASUREMENT INFORMATION

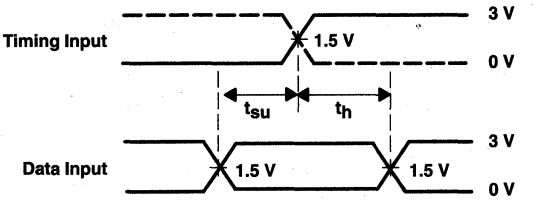


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

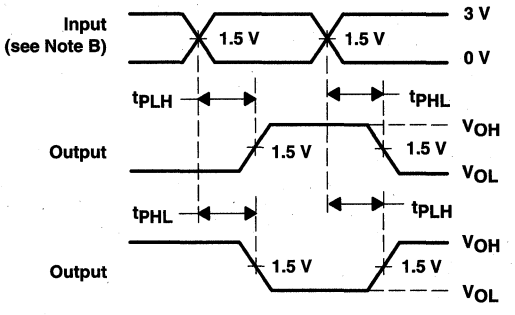
LOAD CIRCUIT FOR OUTPUTS



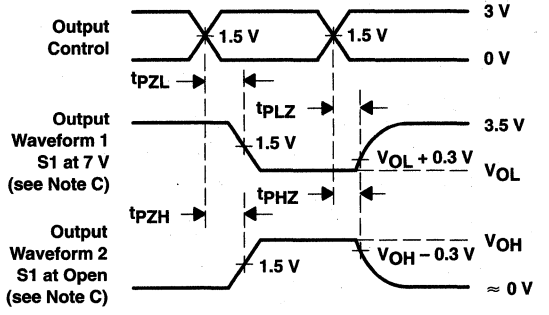
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



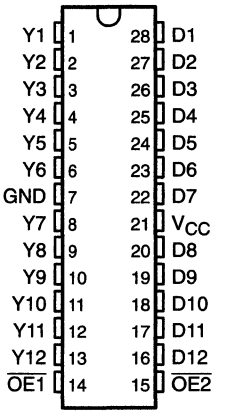
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

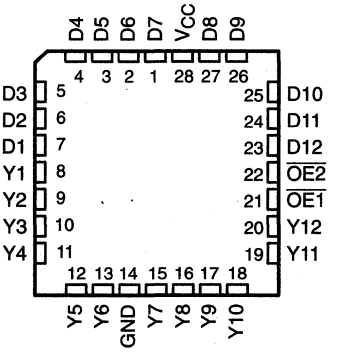
Figure 1. Load Circuit and Voltage Waveforms

- **Output Ports Have 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Typical V_{OLV} (Output Undershoot) < 0.5 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs**

SN54ABT5402 . . . JT PACKAGE
SN74ABT5402 . . . DW PACKAGE
(TOP VIEW)



SN54ABT5402 . . . FK PACKAGE
(TOP VIEW)



description

These 12-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all 12 outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

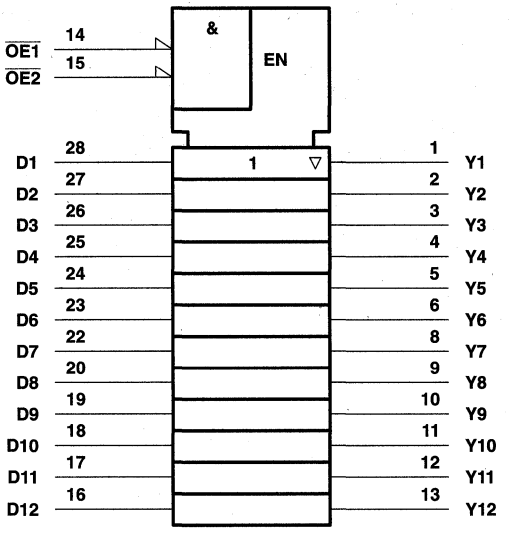
The SN54ABT5402 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT5402 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	D	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

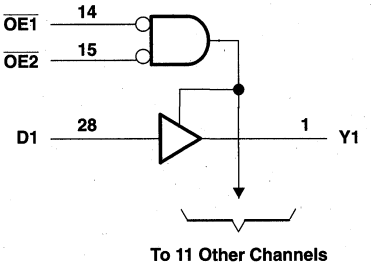
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW and JT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... –0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... –50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DW package ..... 1.2 W
Storage temperature range ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT5402		SN74ABT5402		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT5402		SN74ABT5402		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −1 mA			3.35	3.7		3.3		3.35		V
	V_{CC} = 5 V, I_{OH} = −1 mA			3.85	4.2		3.8		3.85		
	V_{CC} = 4.5 V, I_{OH} = −3 mA						3		3.1		
	V_{CC} = 4.5 V, I_{OH} = −12 mA			2.6					2.6		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA							0.8		0.65	V
	V_{CC} = 4.5 V, I_{OL} = 12 mA									0.8	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND					±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V					−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O	V_{CC} = 5.5 V, V_O = 2.5 V			−25	−45	−100	−25	−100	−25	−100	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0			−50		−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		5	50		50		50	µA
			Outputs low		36	45		45		45	mA
			Outputs disabled		1	50		50		50	µA
ΔI_{CC}§	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT5402		SN74ABT5402		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Y	2	4.5	5.7	2	6.7	2	6.5	ns
t_{PHL}			1.5	3.7	4.5	1.5	5.5	1.5	5.2	
t_{PZH}	$\overline{OE}$	Y	2.5	5.7	6.6	2.5	8.6	2.5	8.5	ns
t_{PZL}			2	4.4	5.5	2	6.9	2	6.8	
t_{PHZ}	$\overline{OE}$	Y	1.5	3.6	4.4	1.5	5.5	1.5	5.2	ns
t_{PLZ}			1.5	4.2	5.4	1.5	7.4	1.5	6.9	

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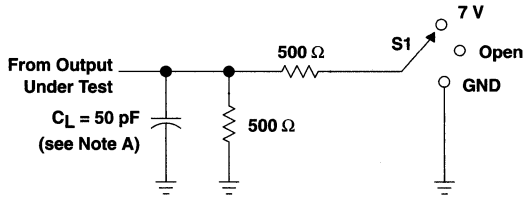
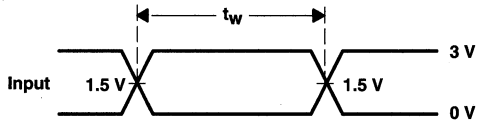
PARAMETER MEASUREMENT INFORMATION

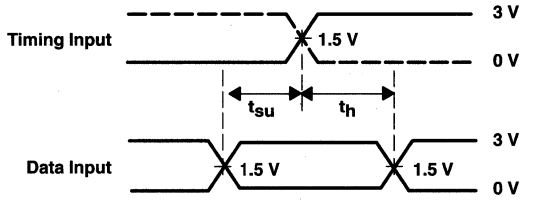


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

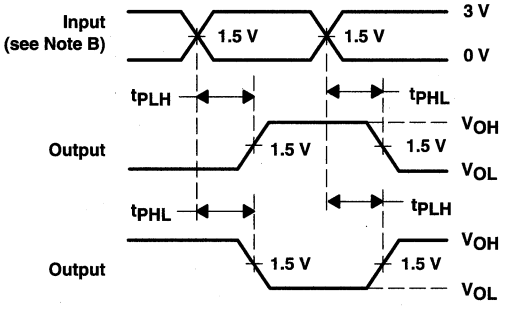
LOAD CIRCUIT FOR OUTPUTS



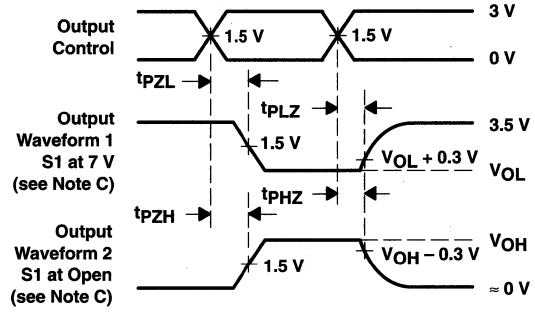
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



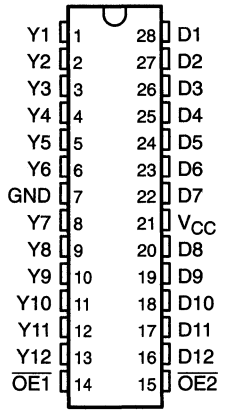
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

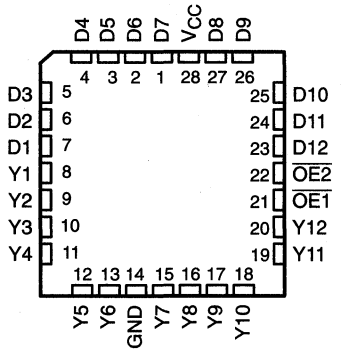
Figure 1. Load Circuit and Voltage Waveforms

- **Output Ports Have 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Typical V_{OLV} (Output Undershoot) < 0.5 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs**

SN54ABT5403 . . . JT PACKAGE
SN74ABT5403 . . . DW PACKAGE
(TOP VIEW)



SN54ABT5403 . . . FK PACKAGE
(TOP VIEW)



description

These 12-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all 12 outputs are in the high-impedance state. These devices provide inverted data.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

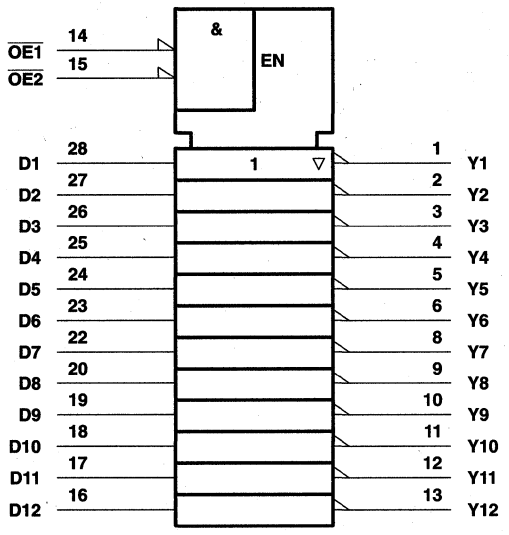
The SN54ABT5403 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT5403 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	D	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

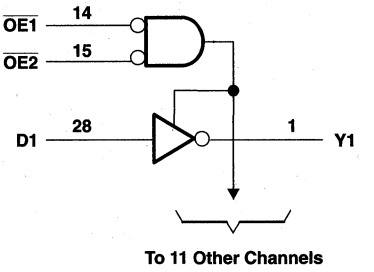
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW and JT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DW package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT5403		SN74ABT5403		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT5403		SN74ABT5403		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −1 mA			3.35	3.7		3.3		3.35		V
	V_{CC} = 5 V, I_{OH} = −1 mA			3.85	4.2		3.8		3.85		
	V_{CC} = 4.5 V, I_{OH} = −3 mA						3		3.1		
	V_{CC} = 4.5 V, I_{OH} = −12 mA			2.6					2.6		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA							0.8		0.65	V
	V_{CC} = 4.5 V, I_{OL} = 12 mA									0.8	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND					±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V					−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O	V_{CC} = 5.5 V, V_O = 2.5 V			−25	−45	−100	−25	−100	−25	−100	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0			−50		−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		5	50		50		50	µA
			Outputs low		36	45		45		45	mA
			Outputs disabled		1	50		50		50	µA
ΔI_{CC}§	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT5403		SN74ABT5403		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Y	2	4.5	6.1	2	7	2	6.9	ns
t_{PHL}			1.5	4.4	5.2	1.5	5.9	1.5	5.7	
t_{PZH}	$\overline{OE}$	Y	2.5	5.7	6.6	2.5	8.6	2.5	8.5	ns
t_{PZL}			2	4.4	5.5	2	6.9	2	6.8	
t_{PHZ}	$\overline{OE}$	Y	1.5	3.6	4.4	1.5	5.5	1.5	5.2	ns
t_{PLZ}			1.5	4.2	5.4	1.5	7.4	1.5	6.9	

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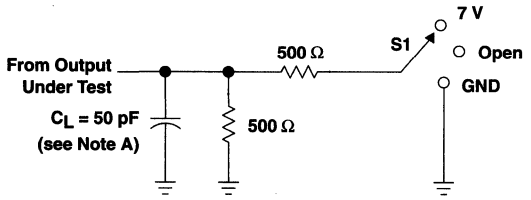
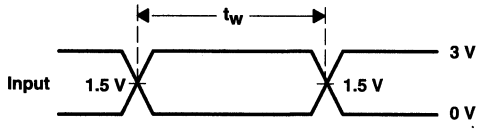
PARAMETER MEASUREMENT INFORMATION

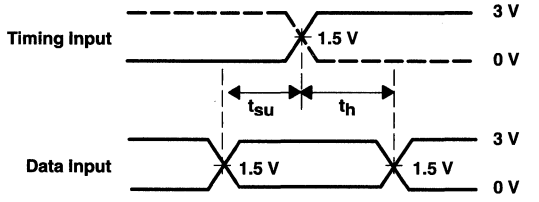


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

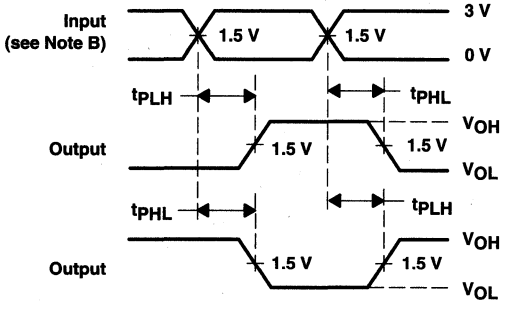
LOAD CIRCUIT FOR OUTPUTS



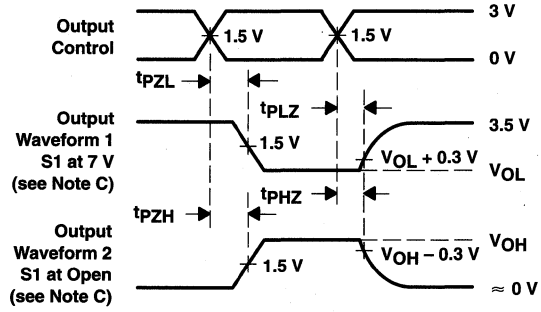
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



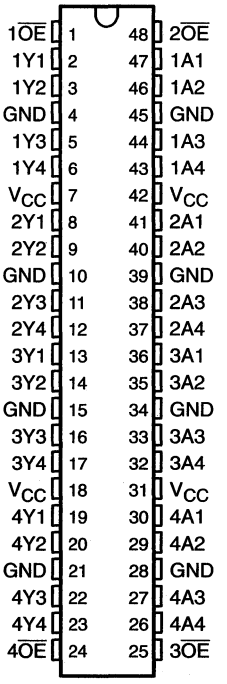
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162240 . . . WD PACKAGE
SN74ABT162240 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT162240 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162240 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT162240 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

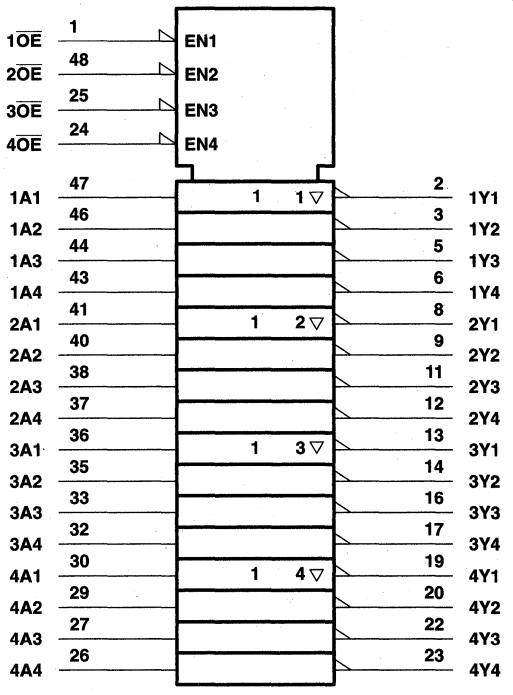
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

PRODUCT PREVIEW

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

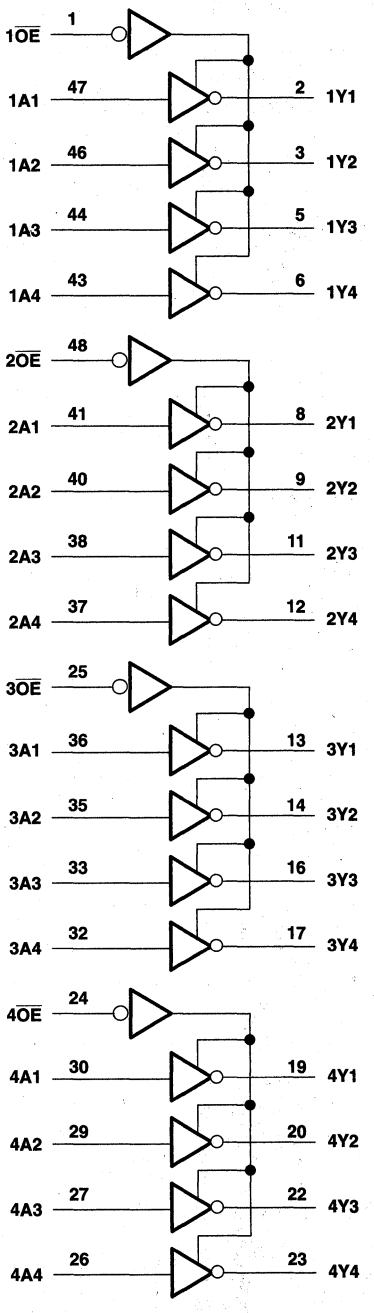
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162240		SN74ABT162240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

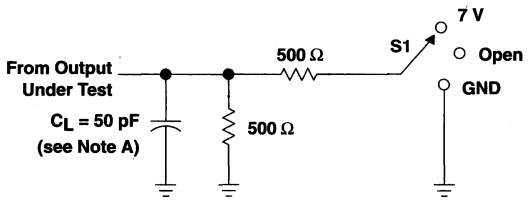
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT162240		SN74ABT162240		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 1 mA			3.35			3.3		3.35		V
	V_{CC} = 5 V, I_{OH} = – 1 mA			3.85			3.8		3.85		
	V_{CC} = 4.5 V, I_{OH} = – 3 mA			3.1			3		3.1		
	V_{CC} = 4.5 V, I_{OH} = – 12 mA			2.6‡					2.6		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA				0.4	0.8		0.8		0.65	V
	V_{CC} = 4.5 V, I_{OL} = 12 mA									0.8	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND					±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				7						pF
C_o	V_O = 2.5 V or 0.5 V				7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

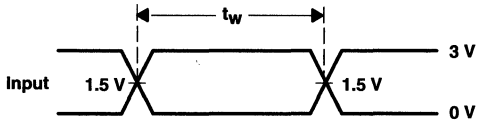
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

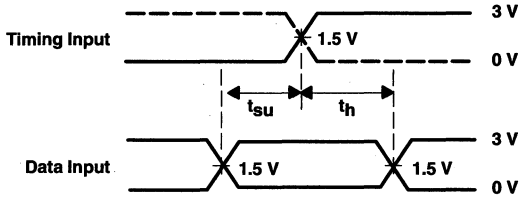


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

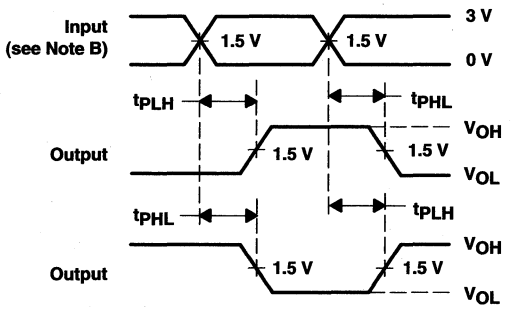
LOAD CIRCUIT FOR OUTPUTS



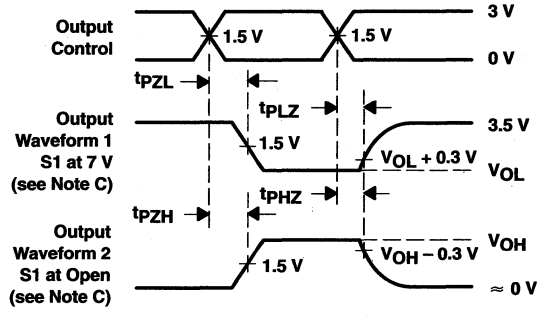
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

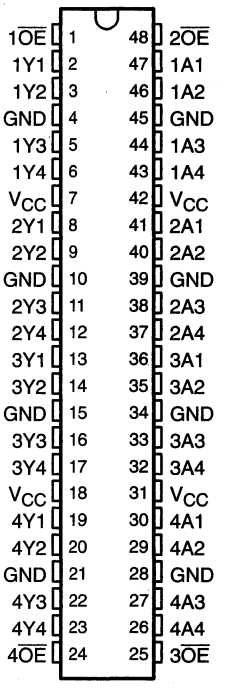
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162244 . . . WD PACKAGE
SN74ABT162244 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT162244 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides noninverting outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162244 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT162244 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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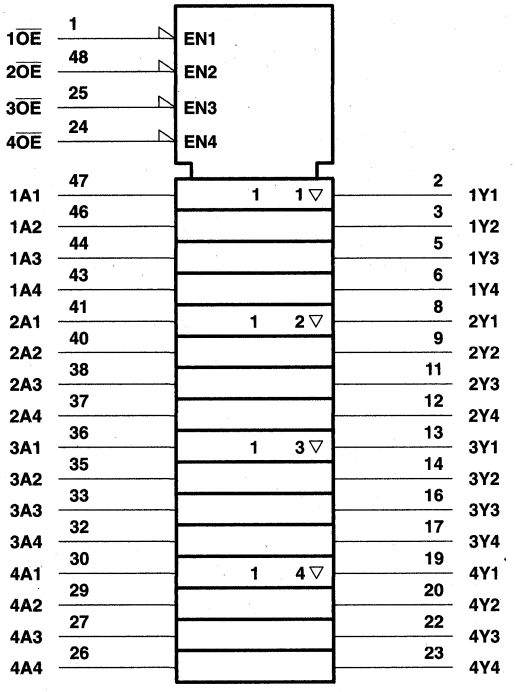
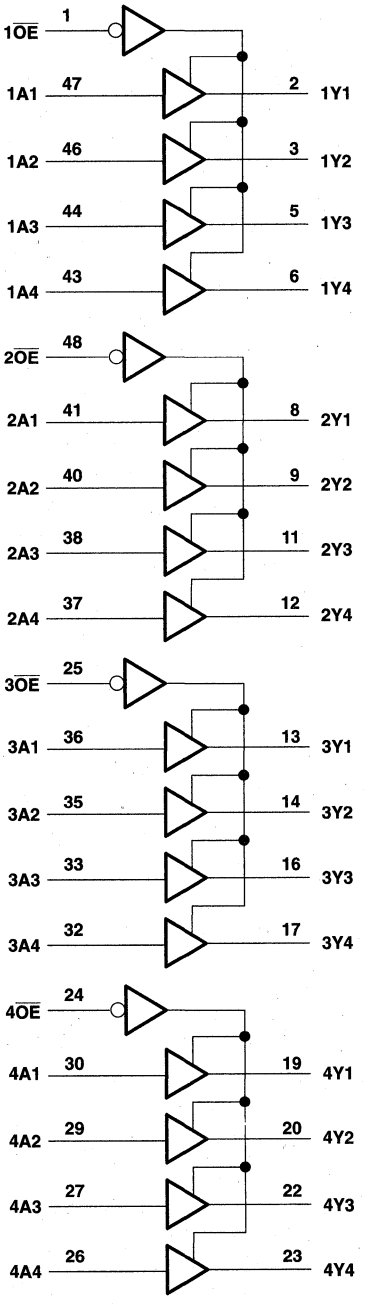
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162244		SN74ABT162244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

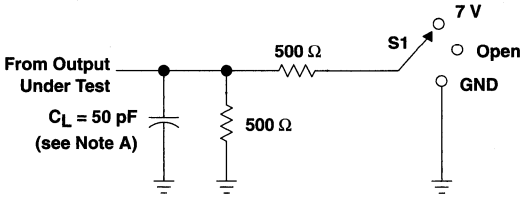
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT162244		SN74ABT162244		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 1 mA			3.35			3.3		3.35		V
	V_{CC} = 5 V, I_{OH} = – 1 mA			3.85			3.8		3.85		
	V_{CC} = 4.5 V, I_{OH} = – 3 mA			3.1			3		3.1		
	V_{CC} = 4.5 V, I_{OH} = – 12 mA			2.6‡					2.6		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA				0.4	0.8		0.8		0.65	V
	V_{CC} = 4.5 V, I_{OL} = 12 mA									0.8	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND					±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V					10		10		10	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V					–10		–10		–10	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100		±100		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V			–25	–55	–100	–25	–100	–25	–100	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			2		2		2	mA
			Outputs low			30		30		30	
			Outputs disabled			2		2		2	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			50		50		50	µA
			Outputs disabled			50		50		50	
		Control inputs				50		50		50	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

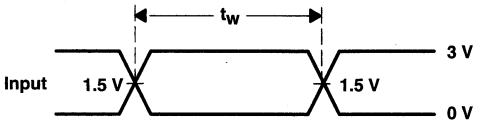
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT162244		SN74ABT162244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.5	3.2	1	4.1	1	3.9	ns
t_{PHL}			1	3.1	4	1	5	1	4.8	
t_{PZH}	$\overline{OE}$	Y	1	3.2	4.2	1	5.6	1	5.4	ns
t_{PZL}			1	3.2	4.1	1	5.2	1	5.1	
t_{PHZ}	$\overline{OE}$	Y	1	3.2	4	1	4.7	1	4.6	ns
t_{PLZ}			1	3.1	3.9	1	4.6	1	4.5	

PARAMETER MEASUREMENT INFORMATION

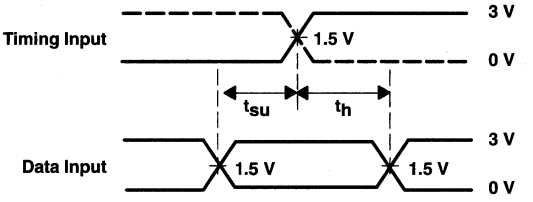


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

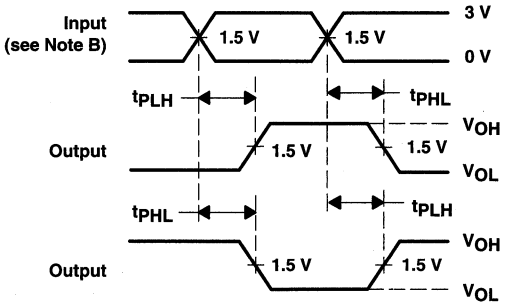
LOAD CIRCUIT FOR OUTPUTS



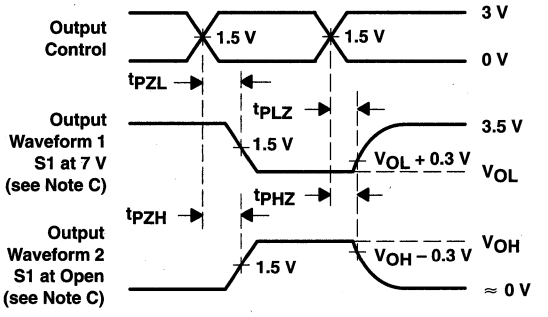
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



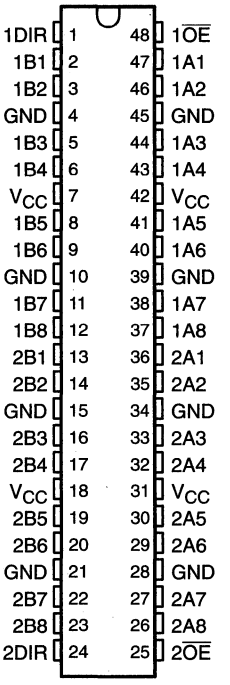
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **A-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162245 . . . WD PACKAGE
SN74ABT162245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT162245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT162245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

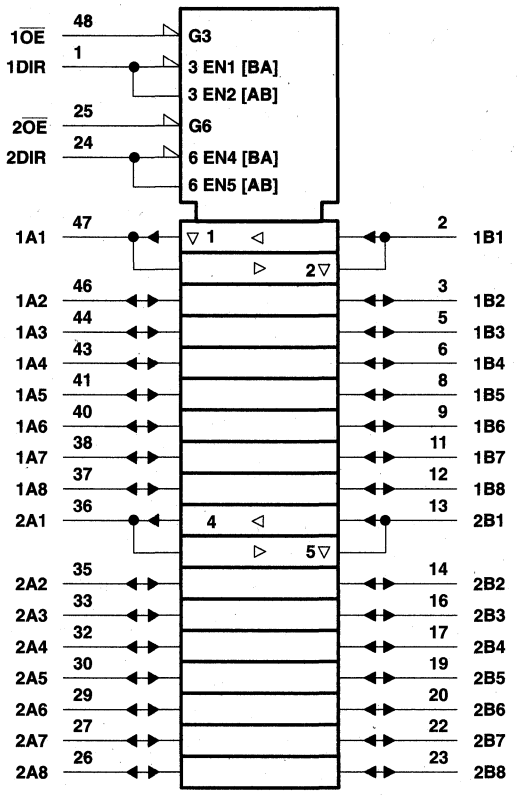
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

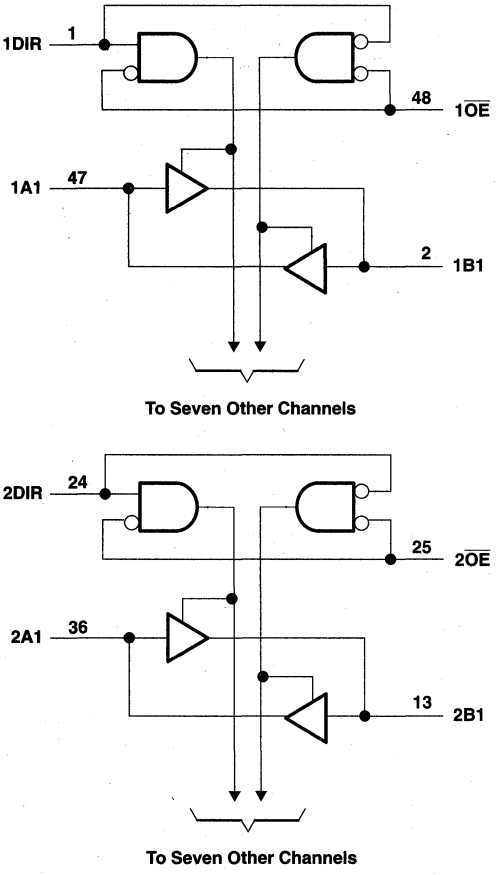
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT162245 (B port) ..... 96 mA
SN74ABT162245 (B port) ..... 128 mA
A port ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162245		SN74ABT162245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	B port		−24		−32	mA
		A port		−12		−12	
I_{OL}	Low-level output current	B port		48		64	mA
		A port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

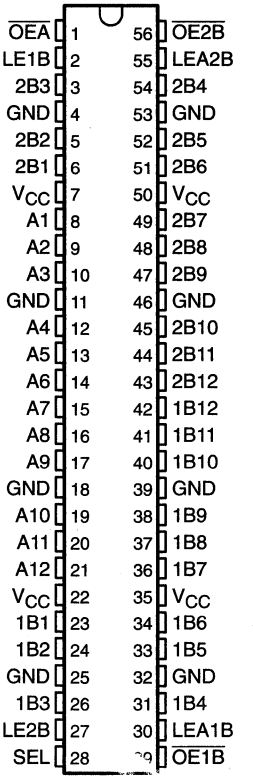
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT162245		SN74ABT162245		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	B port	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	A port	2.6‡					2.6		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 8 mA	A port		0.4	0.8		0.8		0.65	V
		I_{OL} = 12 mA								0.8	
		I_{OL} = 48 mA	B port			0.55		0.55			
		I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				7						pF
C_{io}	V_O = 2.5 V or 0.5 V				7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162260 . . . WD PACKAGE
SN74ABT162260 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT162260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A to B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

The B-port outputs, which are designed to sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

description (continued)

The SN74ABT162260 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162260 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT162260 is characterized for operation from −40°C to 85°C.

FUNCTION TABLES

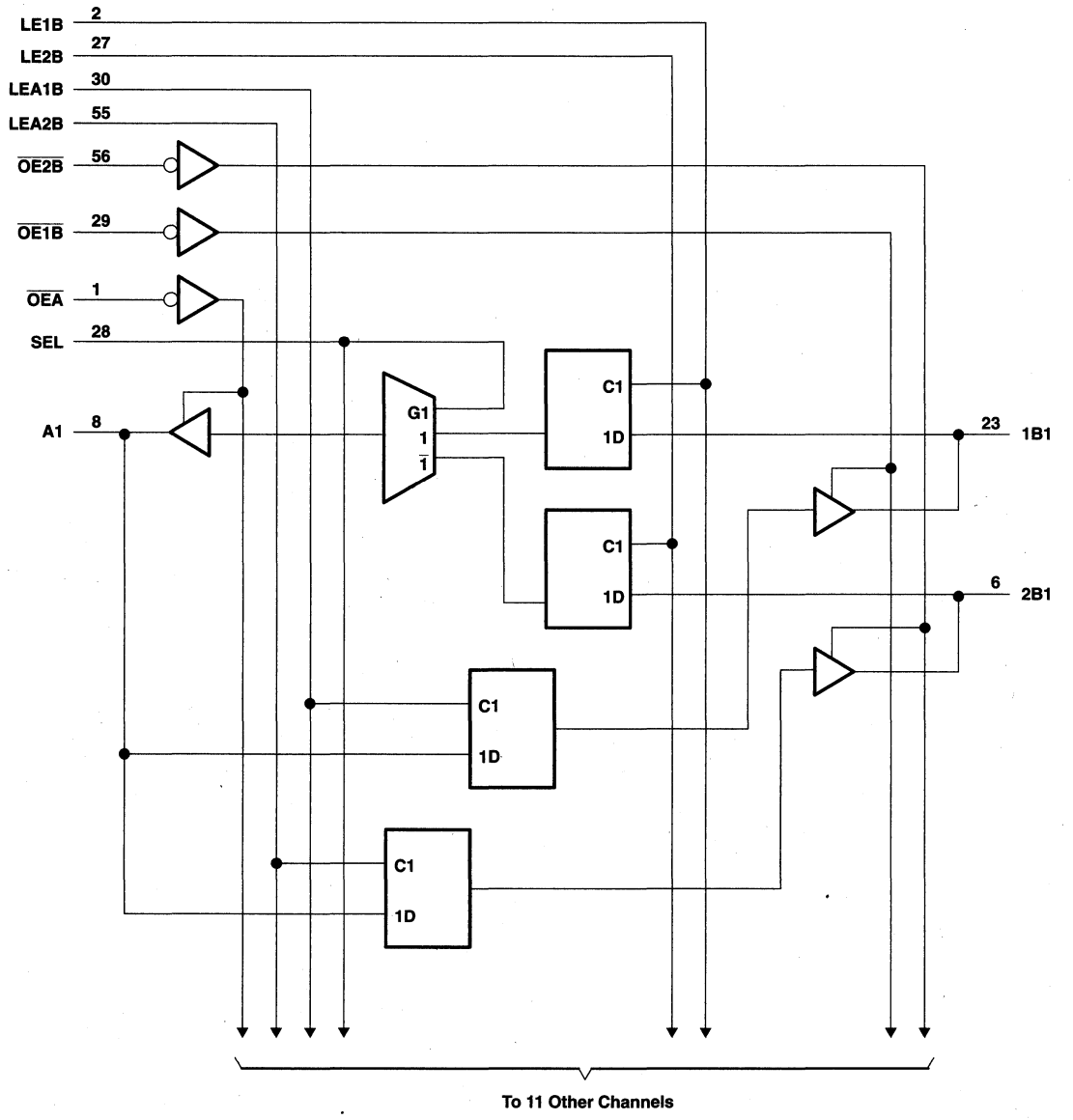
B TO A ($\overline{OEB}$ = H)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A_0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A_0
X	X	X	X	X	H	Z

A TO B ($\overline{OEA}$ = H)

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	$2B_0$
L	H	L	L	L	L	$2B_0$
H	L	H	L	L	$1B_0$	H
L	L	H	L	L	$1B_0$	L
X	L	L	L	L	$1B_0$	$2B_0$
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT162260 (A port) ..... 96 mA
SN74ABT162260 (A port) ..... 128 mA
B port ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162260		SN74ABT162260		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT162260		SN74ABT162260		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = –24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA	A port			0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA	A port			0.55‡				0.55	
	V_{CC} = 4.5 V, I_{OL} = 12 mA	B port			0.8		0.8		0.8	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Control inputs			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
$I_{(I)hold}$	V_{CC} = 4.5 V, V_I = 0.8 V	A or B ports						100		µA
	V_{CC} = 4.5 V, V_I = 2 V	A or B ports						–100		
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V		–50	–100	–225	–50	–225	–50	–225	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			1.5		1.5		1.5	mA
		Outputs low			63		63		63	
		Outputs disabled			1		1		1	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1		1.5		1	mA
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			11.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

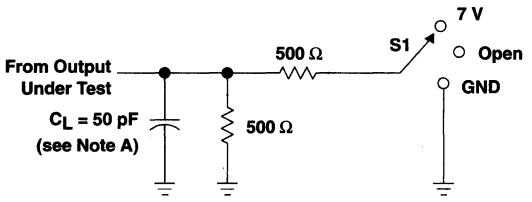
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V_{CC} = 5 V, T_A = 25°C		SN54ABT162260		SN74ABT162260		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1.5		1.5		1.5		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		1		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

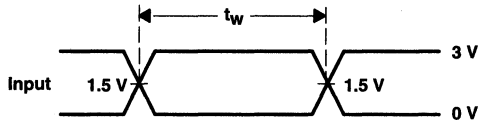
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT162260		SN74ABT162260		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.4	3.6	5.2	1.4	6.3	1.4	6.1	ns
t_{PHL}			2.7	4.8	6.4	2.7	7.4	2.7	7.1	
t_{PLH}	B	A	1.6	3.6	5.2	1.6	6.4	1.6	6	ns
t_{PHL}			1.7	3.8	5.5	1.7	6.5	1.7	6.2	
t_{PLH}	LE	A	1.8	3.9	5.3	1.8	6.6	1.8	6.3	ns
t_{PHL}			2.3	4.1	5.4	2.3	6.1	2.3	5.8	
t_{PLH}	LE	B	1.6	3.7	5.4	1.6	6.4	1.6	6.1	ns
t_{PHL}			2.8	4.9	6.4	2.8	7.5	2.8	7.1	
t_{PLH}	SEL (1B)	A	1.5	3.6	5	1.5	5.9	1.5	5.6	ns
t_{PHL}			1.8	3.5	4.8	1.8	5.2	1.8	5	
t_{PLH}	SEL (2B)	A	1.2	3.6	5.1	1.2	6.5	1.2	6.3	ns
t_{PHL}			1.7	4	5.5	1.7	6.5	1.7	6.2	
t_{PZH}	$\overline{OE}$	A	1.1	3.5	5.2	1.1	6.5	1.1	6.3	ns
t_{PZL}			2.1	4.2	5.7	2.1	6.6	2.1	6.5	
t_{PZH}	$\overline{OE}$	B	1	3.4	4.9	1	6.4	1	6.3	ns
t_{PZL}			2.9	5.5	6.8	2.9	8.3	2.9	8.2	
t_{PHZ}	$\overline{OE}$	A	2.5	4.5	5.9	2.5	6.9	2.5	6.7	ns
t_{PLZ}			1.8	3.4	4.8	1.8	5.6	1.8	5.2	
t_{PHZ}	$\overline{OE}$	B	2.1	4.4	5.7	2.1	7.7	2.1	7.5	ns
t_{PLZ}			1.7	3.9	5.4	1.7	6.3	1.7	6.2	

PARAMETER MEASUREMENT INFORMATION

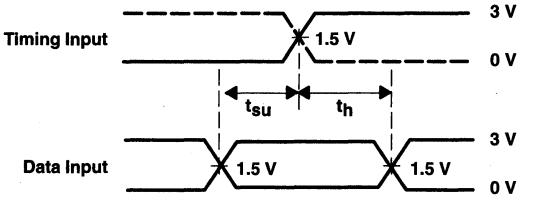


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

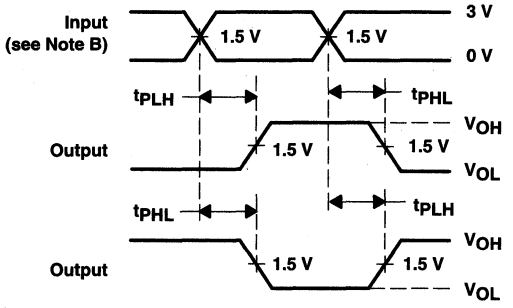
LOAD CIRCUIT FOR OUTPUTS



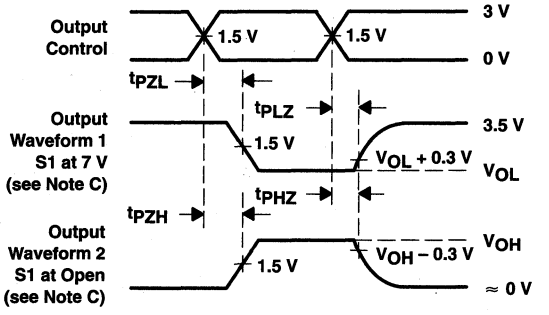
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



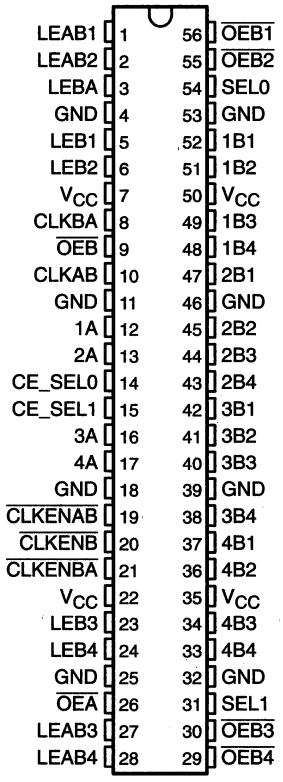
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162460 . . . WD PACKAGE
SN74ABT162460 . . . DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'ABT162460 is a 4-bit-to-1-bit multiplexed registered transceiver used in applications where four separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is also useful in memory-interleaving applications.

Five 4-bit I/O ports (1A–4A, 1B1–4, 2B1–4, 3B1–4, and 4B1–4) are available for address and/or data transfer. The output-enable ($\overline{OEB}$, $\overline{OEB1}$–$\overline{OEB4}$, and $\overline{OEA}$) inputs control the bus transceiver functions. These control signals also allow 4-bit or 16-bit control depending on the $\overline{OEB}$ level.

Address and/or data information can be stored using the internal storage latches/flip-flops. The latch-enable (LEB1–LEB4, LEBA, and LEAB1–LEAB4) and clock/clock-enable (CLK/$\overline{CLKEN}$) inputs are used to control data storage. When either one of the latch-enable inputs is high, the latch is transparent (clock is a don't care as long as the latch-enable is high). When the latch-enable input goes low (providing that the clock does not transit from low to high), the data present at the inputs is latched and remains latched until the latch-enable input is returned high. When the clock-enable is low and the corresponding latch-enable is low, data can be clocked on the low to high transition of the clock. When either the clock-enable or the corresponding latch-enable is high, the clock is a don't care.

Four select (SEL0, SEL1, CE_SEL0, and CE_SEL1) pins are provided to multiplex data (A port), or to select one of four clock-enables (B port). This allows the user to have the flexibility of controlling one bit at a time.

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description (continued)

The B-port outputs, which are designed to sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162460 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162460 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT162460 is characterized for operation from −40°C to 85°C.

A-TO-B OUTPUT-ENABLE TABLE†

INPUTS		OUTPUT
$\overline{OEB}$	$\overline{OEBn}$	Bn
H	H	Z
H	L	Z
L	H	Z
L	L	Active

† n = 1, 2, 3, 4

A-TO-B STORAGE TABLE (ASSUMING $\overline{OEB}$ = L, $\overline{OEBn}$ = L)‡

INPUTS								OUTPUTS			
$\overline{CLKENAB}$	CE_SEL1	CE_SEL0	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4
X	X	X	H or L	H	L	L	L	A	A_0	A_0	A_0
X	X	X	H or L	H	H	H	L	A	A	A	A_0
L	X	X	L	L	L	L	L	A_0	A_0	A_0	A_0
L	L	L	↑	L	L	L	L	A	A_0	A_0	A_0
L	L	H	↑	L	L	L	L	A_0	A	A_0	A_0
L	H	L	↑	L	L	L	L	A_0	A_0	A	A_0
L	H	H	↑	L	L	L	L	A_0	A_0	A_0	A
H	X	X	↑	L	L	L	L	A_0	A_0	A_0	A_0

‡ This table does not cover all the latch-enable cases since they have similar results.

PRODUCT PREVIEW

B-TO-A STORAGE TABLE (BEFORE POINT "P")

INPUTS								"P"
$\overline{\text{CLKENB}}$	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SEL0	
X	X	H	L	L	L	L	L	B1
X	X	L	H	L	L	L	H	B2
X	X	L	L	H	L	H	L	B3
X	X	L	L	L	H	H	H	B4
L	↑	L	L	L	L	L	L	B1
						L	H	B2
						H	L	B3
						H	H	B4
L	L	L	L	L	L	L	L	$B1_0$†
						L	H	$B2_0$†
						H	L	$B3_0$†
						H	H	$B4_0$†

B-TO-A STORAGE TABLE (AFTER POINT "P")

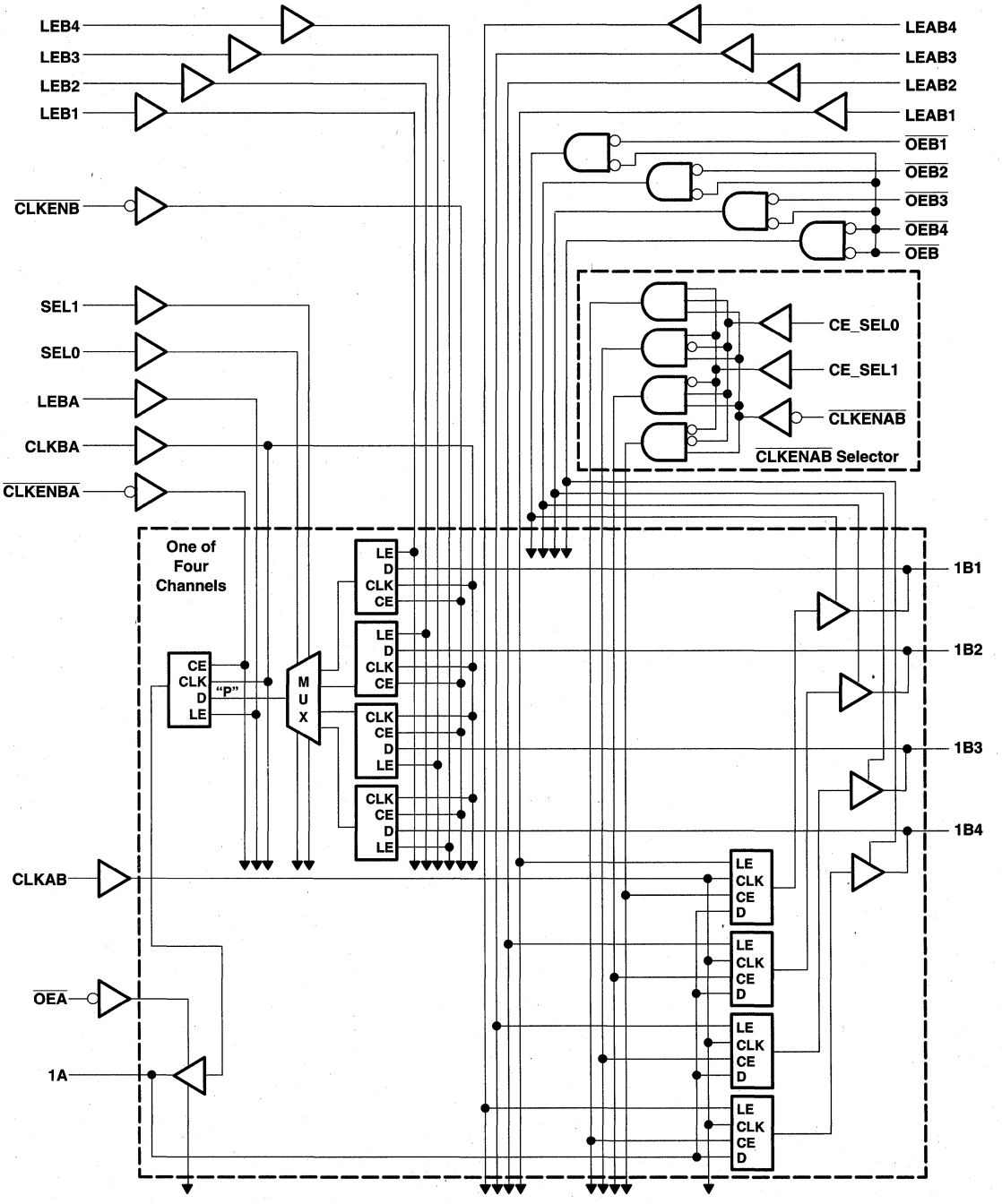
INPUTS					OUTPUT
$\overline{\text{CLKENBA}}$	CLKBA	LEBA	$\overline{\text{OEA}}$	B	A
X	X	X	H	X	Z
X	X	H	L	L	L
X	X	H	L	H	H
H	X	L	L	X	A_0†
L	↑	L	L	L	L
L	↑	L	L	H	H
L	L	L	L	X	A_0†

† Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT162460 (A port) ..... 96 mA
SN74ABT162460 (A port) ..... 128 mA
B port ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162460		SN74ABT162460		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT162460		SN74ABT162460		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA	A port				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
	V_{CC} = 4.5 V, I_{OL} = 12 mA	B port				0.8		0.8		0.8	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Control inputs				±1		±1		±1	µA
		A or B ports				±100		±100		±100	
$I_{I(hold)}$	V_{CC} = 4.5 V, V_I = 0.8 V	A or B ports							100		µA
	V_{CC} = 4.5 V, V_I = 2 V								−100		
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high				50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			−50	−100	−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			2		2		2	mA
			Outputs low			35		35		35	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V	Control inputs									pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports									pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

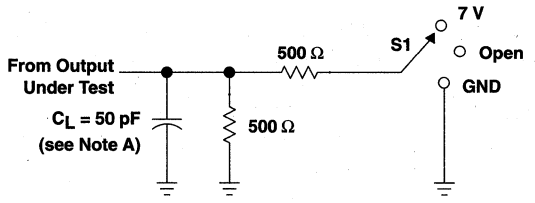
				SN54ABT162460		SN74ABT162460		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high				4		ns
		CLKAB or CLKBA high or low				4		
t_{su}	Setup time	Before CLK↑	A or B			2		ns
			$\overline{CLKEN}$			3		
		A before LEAB↓ or B before LEBA↓	CLK high			2		
			CLK low			2		
t_h	Hold time	After CLK↑	A or B			2		ns
			$\overline{CLKEN}$			2		
		A after LEAB↓ or B after LEBA↓				3		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT162460		SN74ABT162460		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	A or B	B or A							7	ns
t_{PHL}									7	
t_{PLH}	CLKAB	B								ns
t_{PHL}										
t_{PLH}	CLKBA	A								ns
t_{PHL}										
t_{PLH}	LEAB	B							7	ns
t_{PHL}									7	
t_{PLH}	LEBA	A							6	ns
t_{PHL}									6	
t_{PLH}	LEB	A							8	ns
t_{PHL}									8	
t_{PLH}	SEL	A							8	ns
t_{PHL}									8	
t_{PLH}	CE_SEL	B								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	A or B							10	ns
t_{PZL}									10	
t_{PHZ}	$\overline{OE}$	A or B							10	ns
t_{PLZ}									10	

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



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t_{PLZ}/t_{PZL}	7 V
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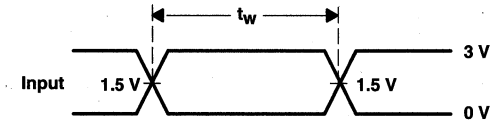
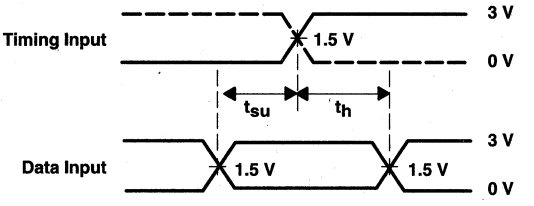
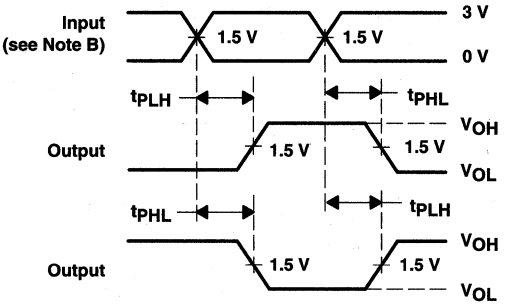
LOAD CIRCUIT FOR OUTPUTS



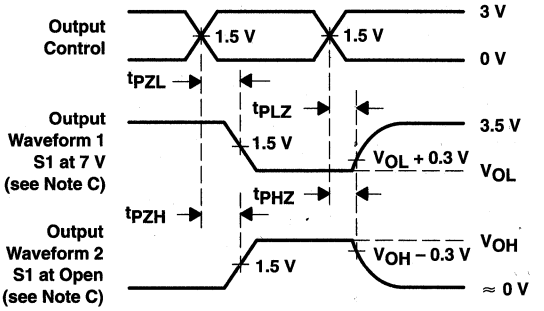
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
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D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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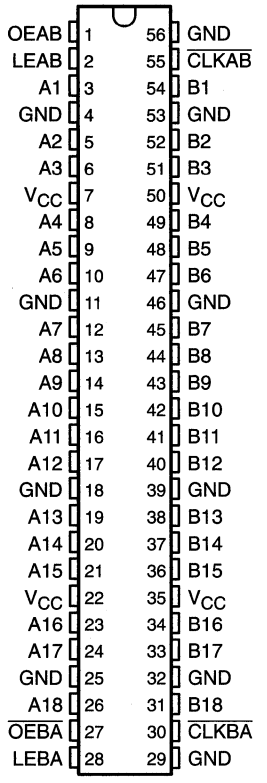
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162500 . . . WD PACKAGE
SN74ABT162500 . . . DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

The B-port outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Widebus+, EPIC-IIB, and UBT are trademarks of Texas Instruments Incorporated.

description (continued)

The SN74ABT162500 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162500 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT162500 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	$\overline{\text{CLKAB}}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

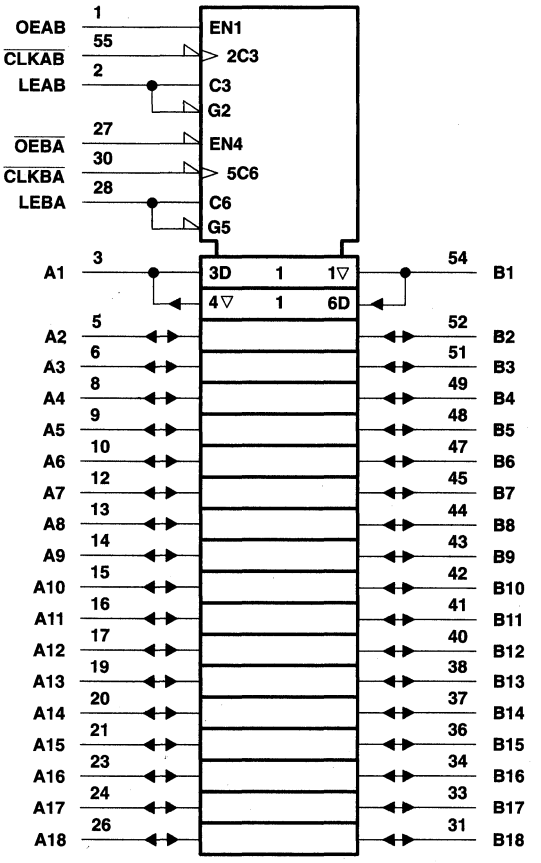
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low.

PRODUCT PREVIEW

logic symbol†

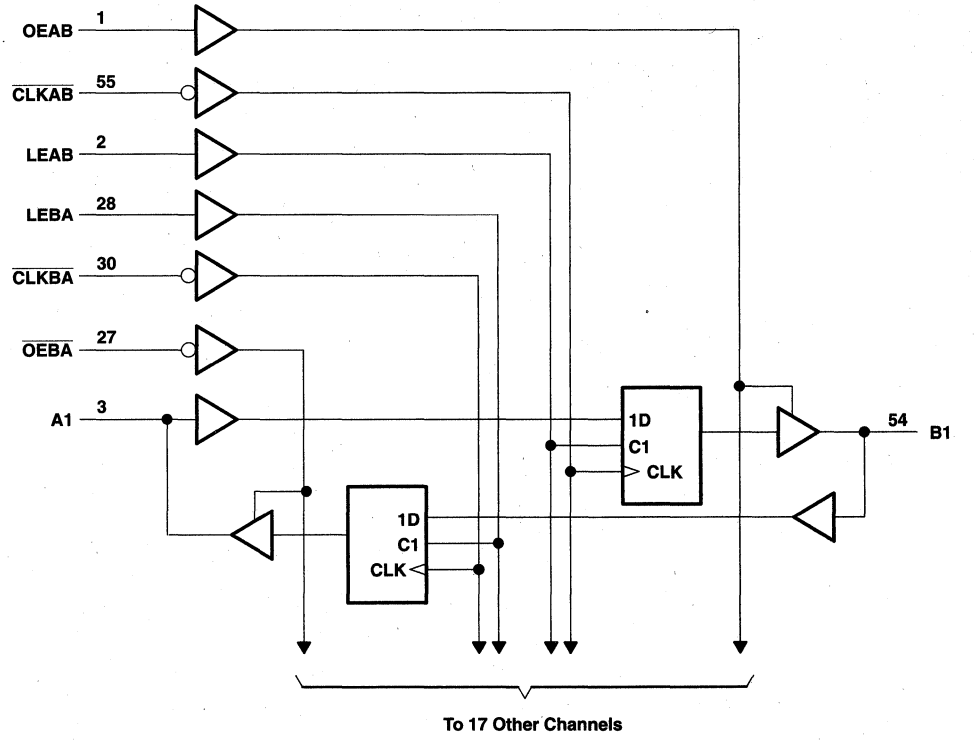


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT162500 (A port) ..... 96 mA
SN74ABT162500 (A port) ..... 128 mA
B port ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162500		SN74ABT162500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	A port		−24		−32	mA
		B port		−12		−12	
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT162500		SN74ABT162500		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}	A port	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = −3 mA	3			3		3		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2				
		V_{CC} = 4.5 V,	I_{OH} = −32 mA	2‡					2		
	B port	V_{CC} = 4.5 V,	I_{OH} = −1 mA	3.35			3.3		3.35		
		V_{CC} = 5 V,	I_{OH} = −1 mA	3.85			3.8		3.85		
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	3.1			3		3.1		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.6					2.6		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55‡				0.55	
	B port	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.8		0.8		0.8	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
	A or B ports					±20		±20		±20	
I_{OZH}§		V_{CC} = 5.5 V,	V_O = 2.7 V			10		10		10	µA
I_{OZL}§		V_{CC} = 5.5 V,	V_O = 0.5 V			−10		−10		−10	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	−50	−100	−180	−50	−180	−50	−180	mA
	B port	V_{CC} = 5.5 V	V_O = 2.5 V	−25	−55	−100	−25	−100	−25	−100	
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}#		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	µA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

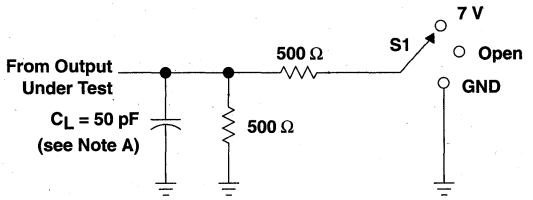
				SN54ABT162500		SN74ABT162500		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high						ns
		$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low						
t_{su}	Setup time	A before $\overline{CLKAB}$↓						ns
		B before $\overline{CLKBA}$↓						
		A before LEAB↓ or B before LEBA↓	$\overline{CLK}$ high					
			$\overline{CLK}$ low					
t_h	Hold time	A after $\overline{CLKAB}$↓ or B after $\overline{CLKBA}$↓						ns
		A after LEAB↓ or B after LEBA↓						

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT162500		SN74ABT162500		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150		MHz
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PLH}	LEAB or LEBA	B or A								ns
t_{PHL}										
t_{PLH}	$\overline{CLKAB}$ or $\overline{CLKBA}$	B or A								ns
t_{PHL}										
t_{PZH}	OEAB or $\overline{OEBA}$	B or A								ns
t_{PZL}										
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A								ns
t_{PLZ}										

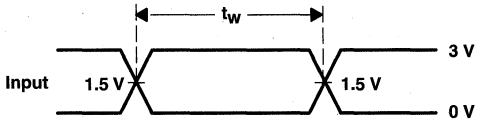
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

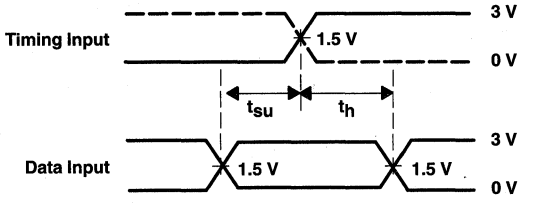


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

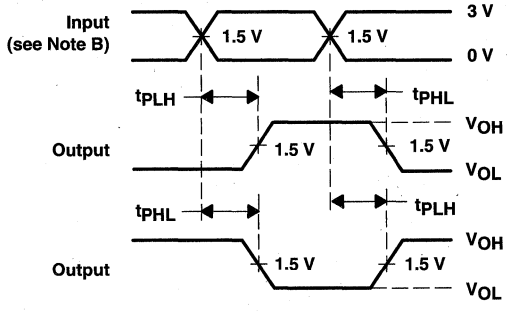
LOAD CIRCUIT FOR OUTPUTS



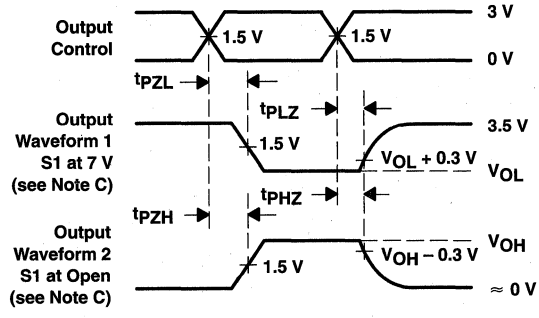
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
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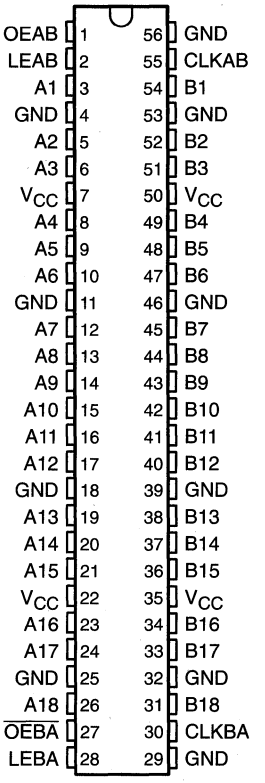
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162501 . . . WD PACKAGE
SN74ABT162501 . . . DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

These 18-bit universal bus transceivers consist of storage elements that can operate either as D-type latches or D-type flip-flops to allow data flow in transparent or clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

The B-port outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT162501 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

Widebus+, EPIC-IIB, and UBT are trademarks of Texas Instruments Incorporated.

description (continued)

The SN54ABT162501 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT162501 is characterized for operation from −40°C to 85°C.

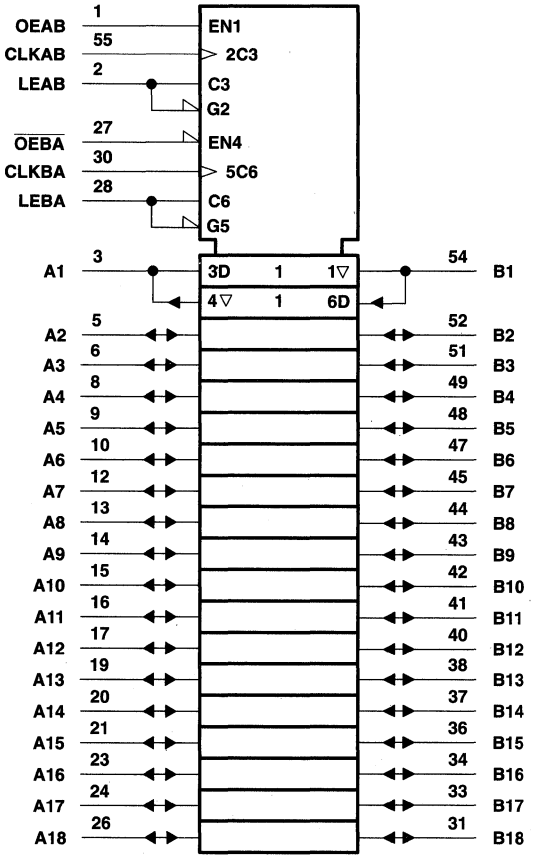
FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.
§ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

logic symbol†

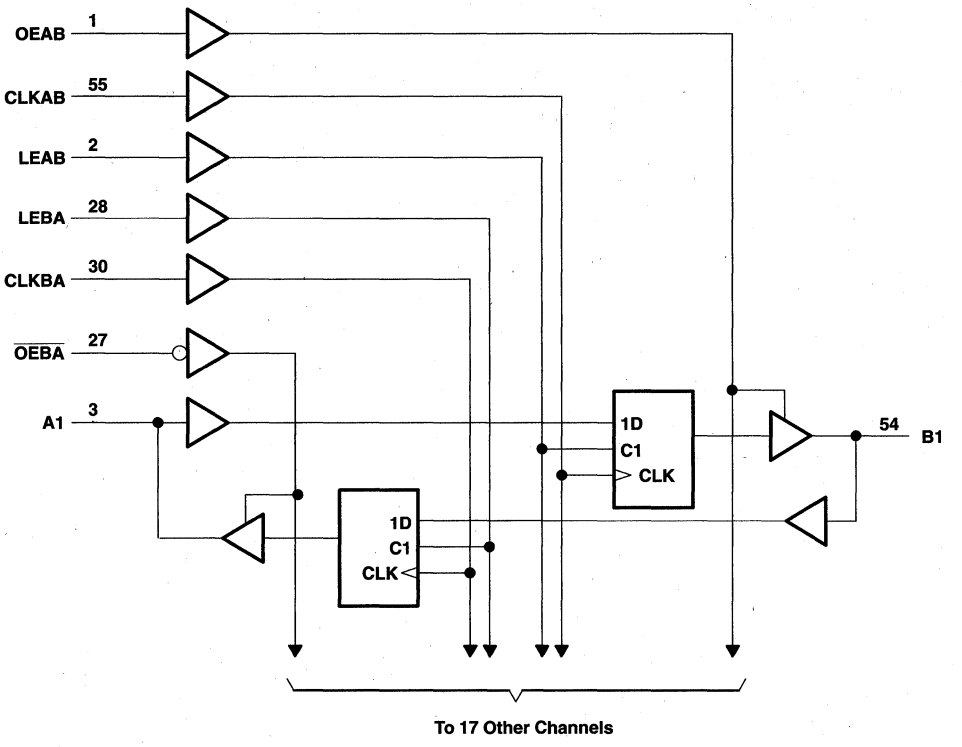


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT162501 (A port) ..... 96 mA
SN74ABT162501 (A port) ..... 128 mA
B port ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162501		SN74ABT162501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	A port		−24		−32	mA
		B port		−12		−12	
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

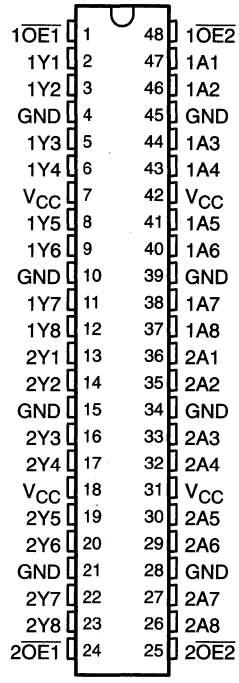
PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT162501		SN74ABT162501		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}	A port	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = −3 mA	3			3		3		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2				
		V_{CC} = 4.5 V,	I_{OH} = −32 mA	2‡					2		
	B port	V_{CC} = 4.5 V,	I_{OH} = −1 mA	3.35			3.3		3.35		
		V_{CC} = 5 V,	I_{OH} = −1 mA	3.85			3.8		3.85		
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	3.1			3		3.1		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.6					2.6		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55‡				0.55	
	B port	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.8		0.8		0.8	
I_I	Control inputs	V_{CC} = 5.5 V,				±1		±1		±1	µA
	A or B ports	V_I = V_{CC} or GND				±20		±20		±20	
I_{OZH}§		V_{CC} = 5.5 V,	V_O = 2.7 V			10		10		10	µA
I_{OZL}§		V_{CC} = 5.5 V,	V_O = 0.5 V			−10		−10		−10	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	−50	−100	−180	−50	−180	−50	−180	mA
	B port	V_{CC} = 5.5 V	V_O = 2.5 V	−25	−55	−100	−25	−100	−25	−100	
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}#		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	µA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162540 . . . WD PACKAGE
SN74ABT162540 . . . DL PACKAGE
(TOP VIEW)



description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162540 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162540 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT162540 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

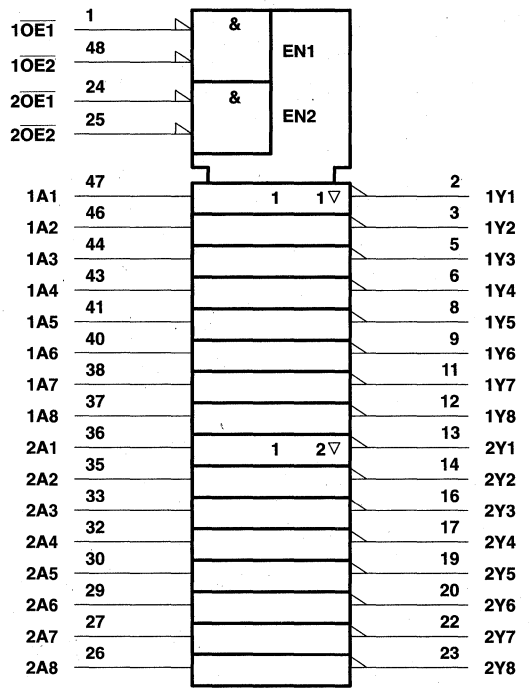
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

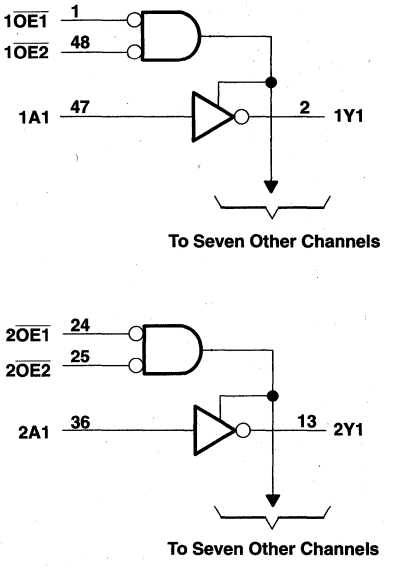
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162540		SN74ABT162540		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

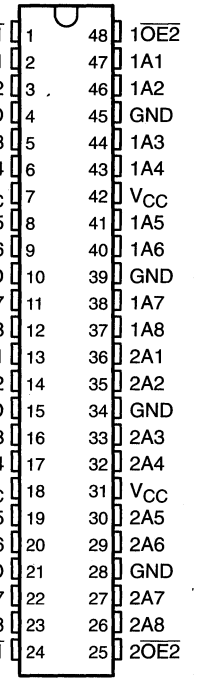
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT162540		SN74ABT162540		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA		3.35			3.3		3.35		V
	V_{CC} = 5 V,	I_{OH} = −1 mA		3.85			3.8		3.85		
	V_{CC} = 4.5 V,	I_{OH} = −3 mA		3.1			3		3.1		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA		2.6‡					2.6		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4	0.8		0.8		0.65	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA								0.8	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				7						pF
C_o	V_O = 2.5 V or 0.5 V				7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162541 . . . WD PACKAGE
SN74ABT162541 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT162541 is a noninverting 16-bit buffer composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162541 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162541 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT162541 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

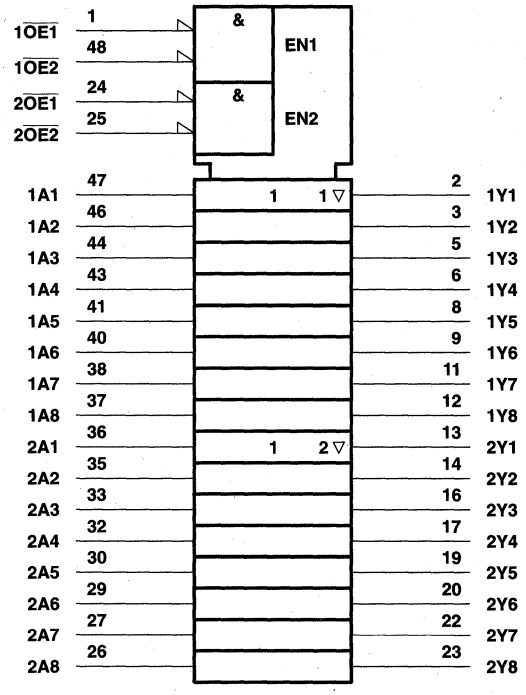
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

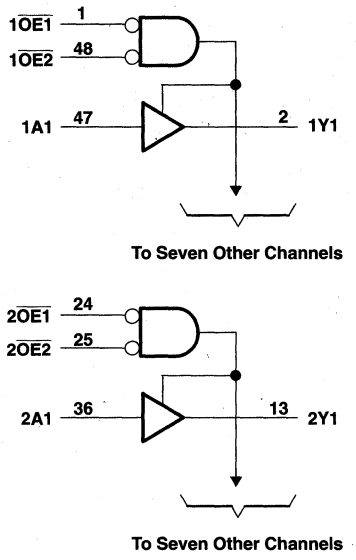
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162541		SN74ABT162541		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

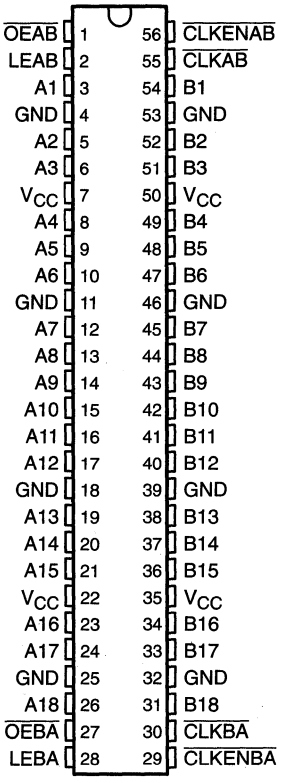
PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT162541		SN74ABT162541		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 1 mA		3.35			3.3		3.35		V
	V_{CC} = 5 V,	I_{OH} = − 1 mA		3.85			3.8		3.85		
	V_{CC} = 4.5 V,	I_{OH} = − 3 mA		3.1			3		3.1		
	V_{CC} = 4.5 V,	I_{OH} = − 12 mA		2.6‡					2.6		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4	0.8		0.8		0.65	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA								0.8	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				7						pF
C_o	V_O = 2.5 V or 0.5 V				7						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162600 . . . WD PACKAGE
SN74ABT162600 . . . DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CLKAB}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{CLKAB}$. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CLKENBA}$.

The B-port outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162600 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162600 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT162600 is characterized for operation from −40°C to 85°C.

Widebus, EPIC-IIB, and UBT are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS					OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	$\overline{\text{CLKAB}}$	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B_0‡
L	L	L	L	X	B_0§

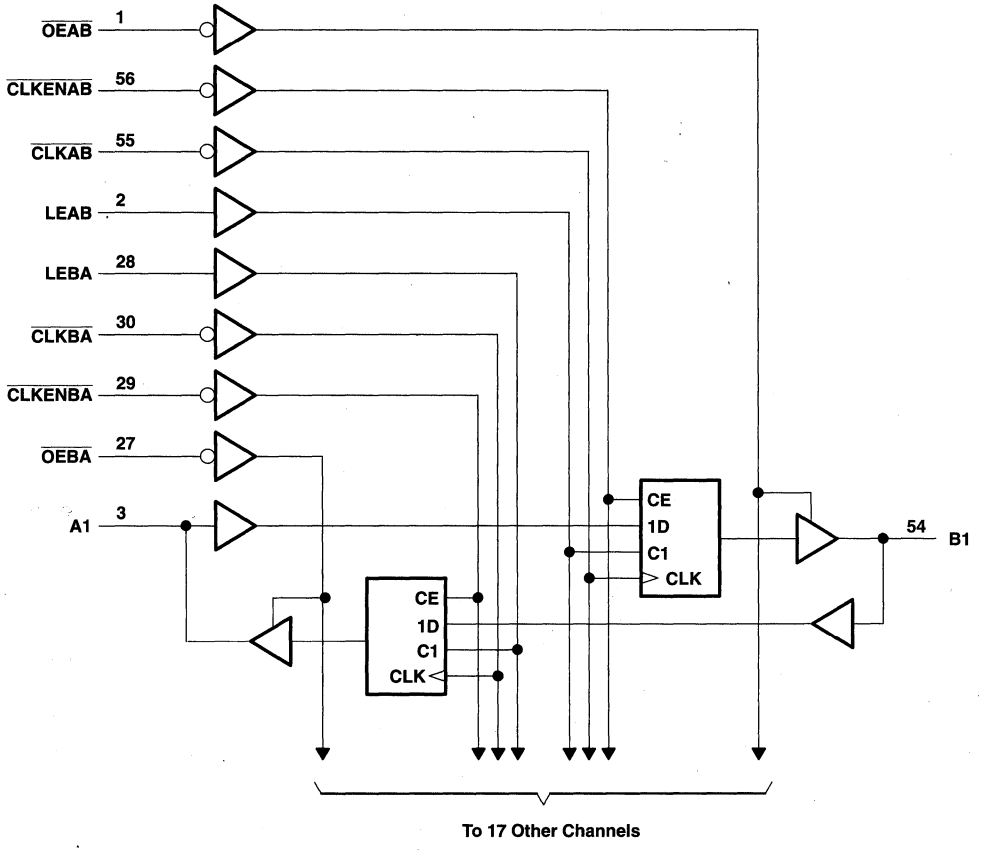
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, $\overline{\text{CLKBA}}$, and $\overline{\text{CLKENBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT162600 (A port) ..... 96 mA
SN74ABT162600 (A port) ..... 128 mA
B port ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162600		SN74ABT162600		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	A port		−24		−32	mA
		B port		−12		−12	
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT162600		SN74ABT162600		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}	A port	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = −3 mA	3			3		3		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2				
		V_{CC} = 4.5 V,	I_{OH} = −32 mA	2‡					2		
	B port	V_{CC} = 4.5 V,	I_{OH} = −1 mA	3.35			3.3		3.35		
		V_{CC} = 5 V,	I_{OH} = −1 mA	3.85			3.8		3.85		
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	3.1			3		3.1		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.6					2.6		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55‡				0.55	
	B port	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.8		0.8		0.8	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
	A or B ports					±20		±20		±20	
I_{OZH}§		V_{CC} = 5.5 V,	V_O = 2.7 V			10		10		10	µA
I_{OZL}§		V_{CC} = 5.5 V,	V_O = 0.5 V			−10		−10		−10	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	−50	−100	−180	−50	−180	−50	−180	mA
	B port	V_{CC} = 5.5 V	V_O = 2.5 V	−25	−55	−100	−25	−100	−25	−100	
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}#		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	µA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ABT162600		SN74ABT162600		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high						ns
		$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low						
t_{su}	Setup time	A before $\overline{CLKAB}\downarrow$						ns
		B before $\overline{CLKBA}\downarrow$						
		A before LEAB↓ or B before LEBA↓	$\overline{CLK}$ high					
			$\overline{CLK}$ low					
t_h	Hold time	A after $\overline{CLKAB}\downarrow$ or B after $\overline{CLKBA}\downarrow$						ns
		A after LEAB↓ or B after LEBA↓						

PRODUCT PREVIEW

TEXAS INSTRUMENTS
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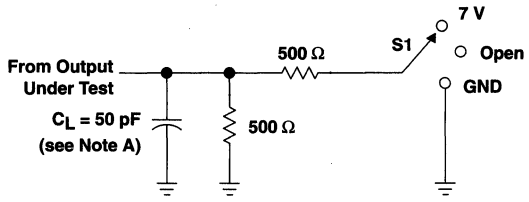
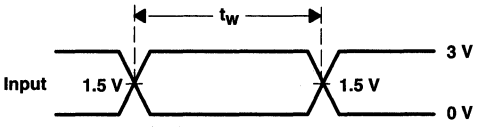
PARAMETER MEASUREMENT INFORMATION

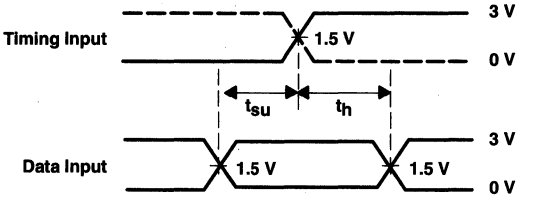


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

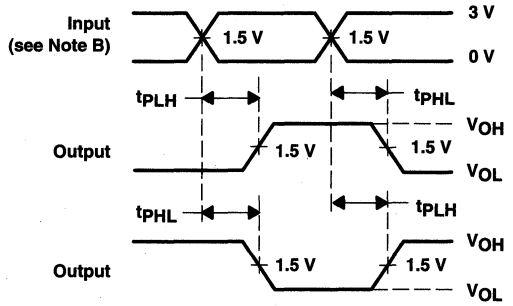
LOAD CIRCUIT FOR OUTPUTS



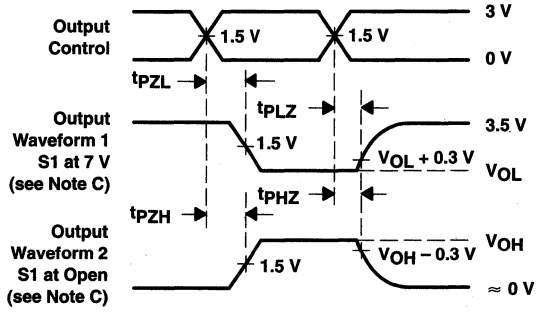
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

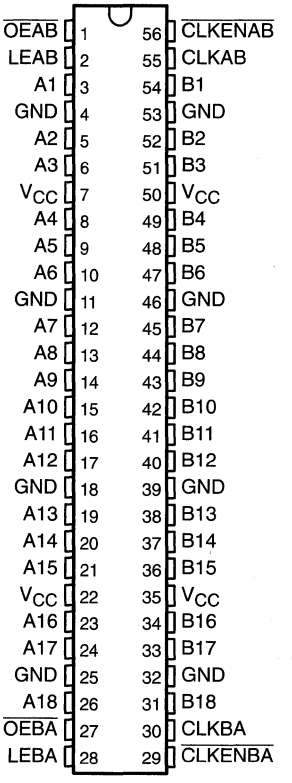
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162601 . . . WD PACKAGE
SN74ABT162601 . . . DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

The B-port outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162601 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162601 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT162601 is characterized for operation from −40°C to 85°C.

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FUNCTION TABLE†

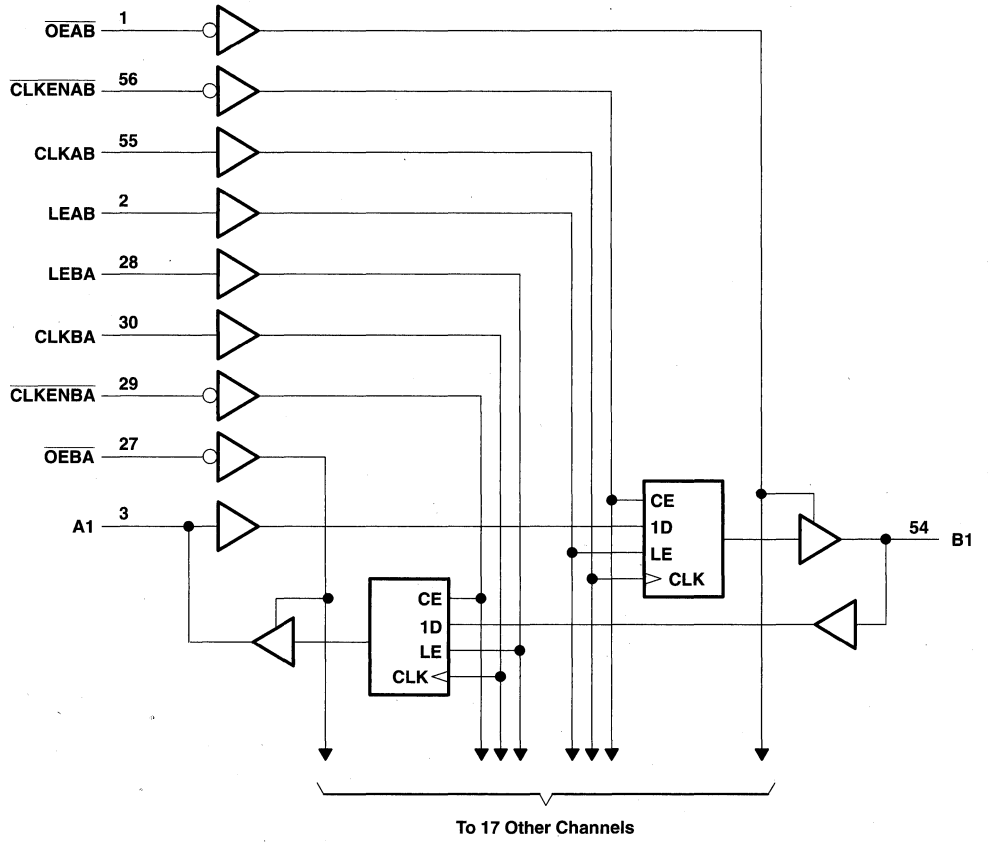
INPUTS					OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT162601 (A port) ..... 96 mA
SN74ABT162601 (A port) ..... 128 mA
B port ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162601		SN74ABT162601		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	A port		−24		−32	mA
		B port		−12		−12	
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT162601		SN74ABT162601		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}	A port	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = −3 mA	3			3		3		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2				
		V_{CC} = 4.5 V,	I_{OH} = −32 mA	2‡					2		
	B port	V_{CC} = 4.5 V,	I_{OH} = −1 mA	3.35			3.3		3.35		
		V_{CC} = 5 V,	I_{OH} = −1 mA	3.85			3.8		3.85		
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	3.1			3		3.1		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.6					2.6		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55‡				0.55	
	B port	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.8		0.8		0.8	
I_I	Control inputs	V_{CC} = 5.5 V,				±1		±1		±1	µA
	A or B ports	V_I = V_{CC} or GND				±20		±20		±20	
I_{OZH}§		V_{CC} = 5.5 V,	V_O = 2.7 V			10		10		10	µA
I_{OZL}§		V_{CC} = 5.5 V,	V_O = 0.5 V			−10		−10		−10	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	−50	−100	−180	−50	−180	−50	−180	mA
	B port	V_{CC} = 5.5 V	V_O = 2.5 V	−25	−55	−100	−25	−100	−25	−100	
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}#		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	µA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

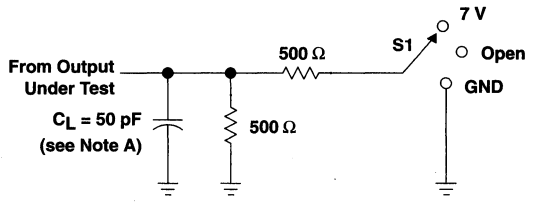
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ABT162601		SN74ABT162601		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		CLKAB or CLKBA high or low		3		3		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑		4.3		4.3		ns
		A before LEAB↓ or B before LEBA↓	CLK high	2.5		2.5		
			CLK low	1		1		
		CLKEN before CLK↑		2.7		2.7		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑		0		0		ns
		A after LEAB↓ or B after LEBA↓		0.5		0.5		
		CLKEN after CLK↑		0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

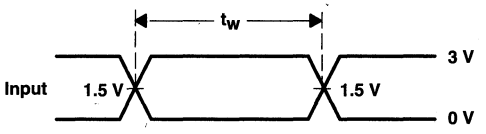
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT162601		SN74ABT162601		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	A	B	1.5	2.8	4	1.5	5.1	1.5	4.8	ns
t_{PHL}			2	3.7	5.2	2	6.1	2	5.7	
t_{PLH}	B	A	1	2.5	3.6	1	4.2	1	4	ns
t_{PHL}			2	3.3	4.5	2	5.1	2	4.9	
t_{PLH}	LEBA	A	2	3.3	4.5	2	5.6	2	5	ns
t_{PHL}			2	3.6	4.7	2	5.4	2	5	
t_{PLH}	LEAB	B	2	3.4	4.8	2	6.1	2	5.6	ns
t_{PHL}			2	3.8	5.2	2	6.4	2	5.9	
t_{PLH}	CLKBA	A	1.5	3.1	4.7	1.5	5.4	1.5	5.3	ns
t_{PHL}			1.5	3.1	4.3	1.5	5.2	1.5	5	
t_{PLH}	CLKAB	B	1.5	3.3	4.7	1.5	6	1.5	5.5	ns
t_{PHL}			1.5	3.5	4.8	1.5	5.8	1.5	5.3	
t_{PZH}	$\overline{OEBA}$	A	2	3.5	4.6	2	5.3	2	5.1	ns
t_{PZL}			2	3.7	4.7	2	5.6	2	5.4	
t_{PZH}	$\overline{OEAB}$	B	2	3.8	5.3	2	6.6	2	6.1	ns
t_{PZL}			2	3.6	5.1	2	6.2	2	5.7	
t_{PHZ}	$\overline{OEBA}$	A	2	3.6	5.4	2	6.6	2	6.2	ns
t_{PLZ}			1.5	3.2	4.7	1.5	5.8	1.5	5.4	
t_{PHZ}	$\overline{OEAB}$	B	2	3.4	4.8	2	5.6	2	5.4	ns
t_{PLZ}			1.5	3.2	4.5	1.5	5.7	1.5	5.2	

PARAMETER MEASUREMENT INFORMATION

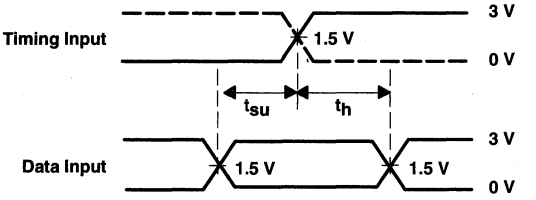


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

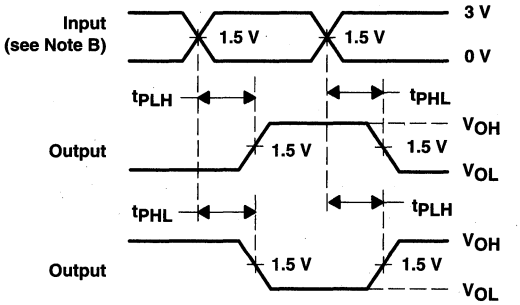
LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
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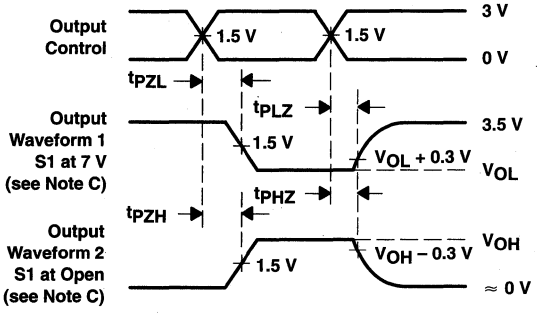

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
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NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
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D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
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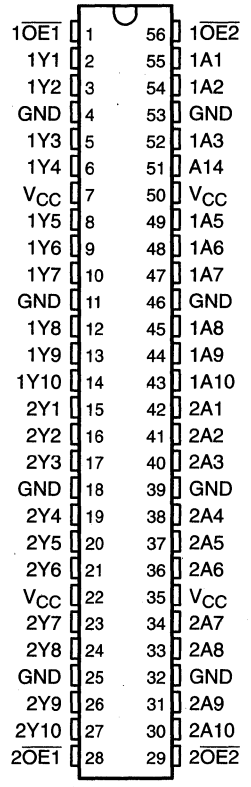
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT162827 . . . WD PACKAGE
SN74ABT162827 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT162827 is a noninverting 20-bit buffer composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162827 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162827 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT162827 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

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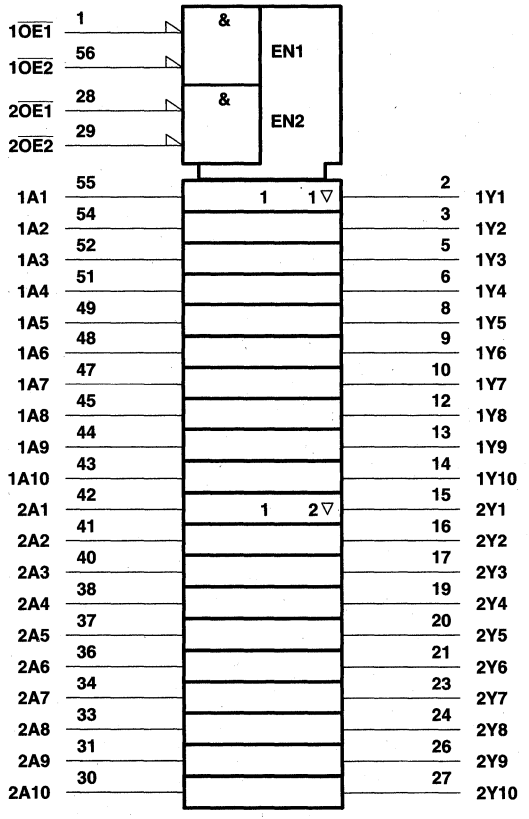
FUNCTION TABLE
(each 10-bit section)

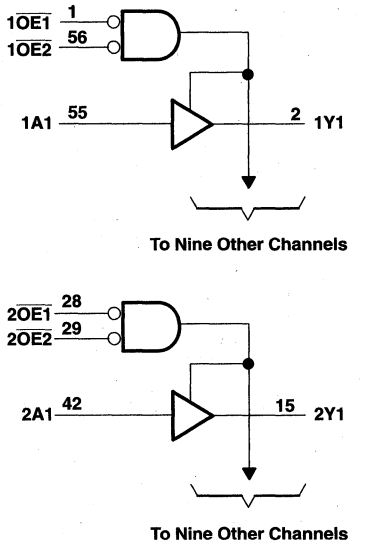
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT162827		SN74ABT162827		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT162827		SN74ABT162827		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −1 mA			3.35			3.3		3.35		V
	V_{CC} = 5 V, I_{OH} = −1 mA			3.85			3.8		3.85		
	V_{CC} = 4.5 V, I_{OH} = −3 mA			3.1			3		3.1		
	V_{CC} = 4.5 V, I_{OH} = −12 mA			2.6‡					2.6		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA				0.4	0.8		0.8		0.65	V
	V_{CC} = 4.5 V, I_{OL} = 12 mA									0.8	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND					±1		±1		±1	µA
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					−50		−50		−50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V										pF
C_o	V_O = 2.5 V or 0.5 V										pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

ABT 25-Ω INCIDENT-WAVE SWITCHING DRIVERS

Features

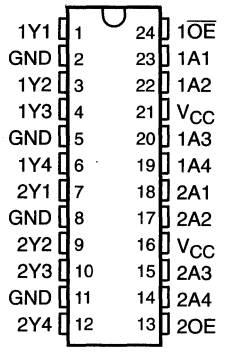
- Incident-wave switching (IWS)
- Increased output-drive capability over standard ABT devices
- Designed for output drive of $I_{OH} = -80$ mA, $I_{OL} = 188$ mA across temperature and V_{CC} conditions
- Sub-5-ns speed
- Power-on-demand active feedback circuitry
- Low input/output capacitance
- Widebus™ functionality planned with equivalent SSOP pinout

Benefits

- Improve system frequency response and reliability by eliminating 2 t_{pd} delay shelf in the transition region caused by reflected waves
- Ideally suited to drive transmission lines on the incident wave at impedances as low as 10 Ω typically
- Ensure IWS at the input of receivers in highly capacitive, heavily loaded, or advanced backplane conditions where equivalent impedances go as low as 25 Ω worst case
- High-performance equivalent to standard ABT
- Allow for low static enable current consumption equivalent to standard ABT
- As receiving devices, do not load down the driving devices
- Low simultaneous switching noise, $V_{OLP} < 0.8$ V typically
- Drop-in replaceable to standard Widebus™ SSOP pinouts

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74ABT25241 is a 25-Ω octal buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

The SN74ABT25241 contains complementary output-enable (1$\overline{OE}$ and 2OE) inputs. When 1$\overline{OE}$ is low and 2OE is high, the device transmits data from the A inputs to the Y outputs. When 1$\overline{OE}$ and 2OE are high, the outputs are in the high-impedance state. Output-enable 1$\overline{OE}$ affects only the 1Y outputs; output-enable 2OE affects only the 2Y outputs.

This buffer/driver is capable of sinking 188 mA of I_{OL} current, which facilitates switching 25-Ω transmission lines on the incident wave. The distributed V_{CC} and GND pins minimize switching noise for more reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT25241 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC-IIB is a trademark of Texas Instruments Incorporated.

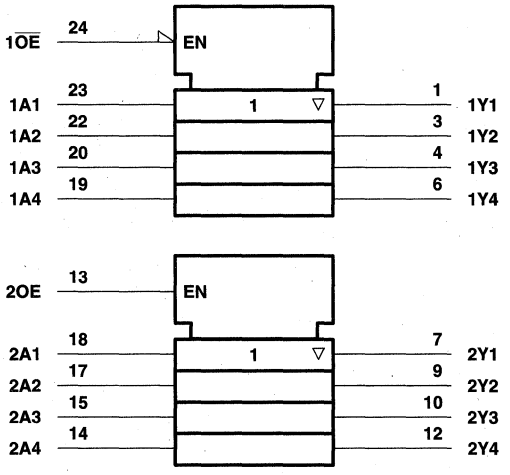
PRODUCT PREVIEW

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

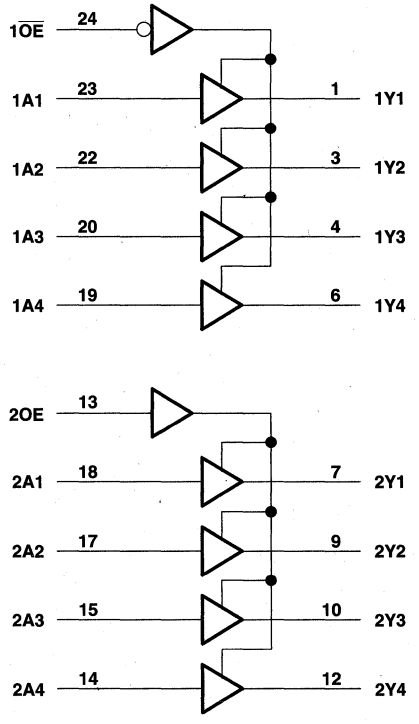
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O ..... −0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Current into any output in the low state, I_O ..... 376 mA
Operating free-air temperature range ..... −40°C to 85°C
Maximum power dissipation at T_A = 55°C (in still air): DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−80	mA
I_{OL}	Low-level output current			188	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

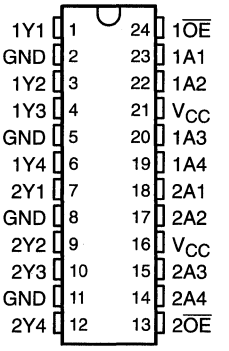
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.7			V
	V_{CC} = 5 V,	I_{OH} = – 80 mA		2.4			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 94 mA				0.55	V
		I_{OL} = 188 mA				0.7	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50	µA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.5 V		–50		180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Outputs open,	Outputs high			500	µA
			Outputs low			30	mA
			Outputs disabled			500	µA
ΔI_{CC}§	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1	mA
C_i	V_{CC} = 5 V,	V_I = V_{CC} or GND					pF
C_o	V_{CC} = 5 V,	V_O = V_{CC} or GND					pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The SN74ABT25244 is a 25-Ω octal buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

When the output-enable ($1\overline{OE}$ and $2\overline{OE}$) inputs are low, the device transmits data from the A inputs to the Y outputs. When $1\overline{OE}$ and $2\overline{OE}$ are high, the outputs are in the high-impedance state.

This buffer/driver is capable of sinking 188 mA of I_{OL} current, which facilitates switching 25-Ω transmission lines on the incident wave. The distributed V_{CC} and GND pins minimize switching noise for more reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT25244 is characterized for operation from −40°C to 85°C.

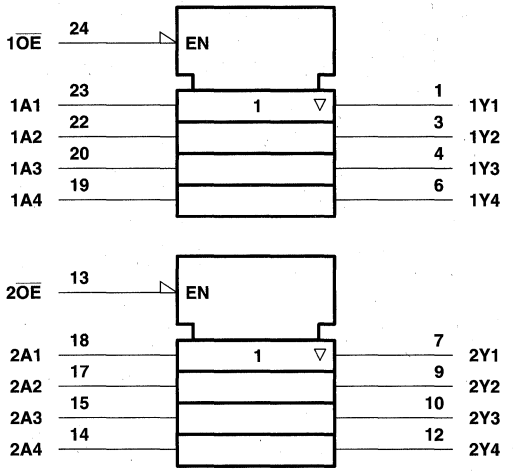
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

EPIC-IIB is a trademark of Texas Instruments Incorporated.

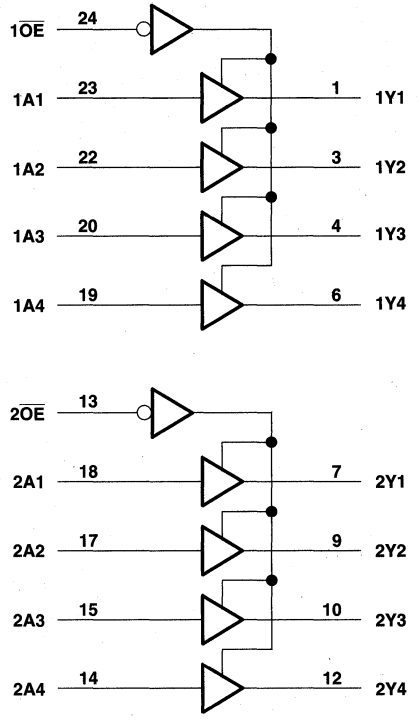
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O ..... −0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Current into any output in the low state, I_O ..... 376 mA
Operating free-air temperature range ..... −40°C to 85°C
Maximum power dissipation at T_A = 55°C (in still air): DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−80	mA
I_{OL}	Low-level output current			188	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

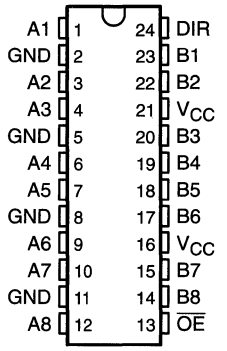
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.7			V
	V_{CC} = 5 V,	I_{OH} = −80 mA		2.4			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 94 mA				0.55	V
		I_{OL} = 188 mA				0.7	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1	μA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−50	μA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100	μA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50	μA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.5 V		−50		180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Outputs open,	Outputs high			500	μA
			Outputs low			30	mA
			Outputs disabled			500	μA
ΔI_{CC}§	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1	mA
C_i	V_{CC} = 5 V,	V_I = V_{CC} or GND					pF
C_o	V_{CC} = 5 V,	V_O = V_{CC} or GND					pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74ABT25245 is a 25-Ω octal bus transceiver designed for asynchronous communication between data buses. It improves both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can disable the device so that both buses are effectively isolated.

This transceiver is capable of sinking 188 mA of I_{OL} current, which facilitates switching 25-Ω transmission lines on the incident wave. The distributed V_{CC} and GND pins minimize switching noise for more reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT25245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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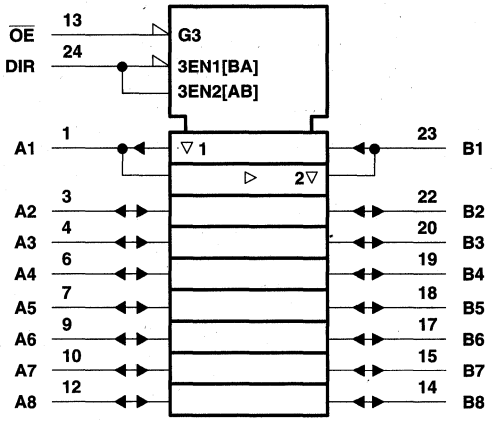
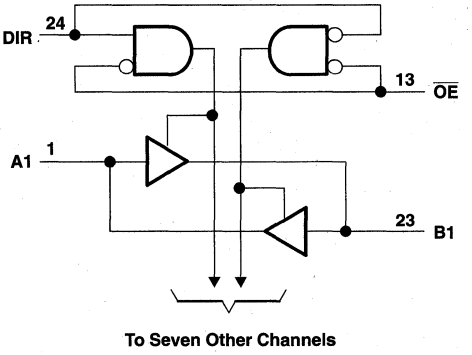
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O ..... −0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Current into any output in the low state, I_O: A port ..... 376 mA
B port ..... 128 mA
Operating free-air temperature range ..... −40°C to 85°C
Maximum power dissipation at T_A = 55°C (in still air): DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			4.5	5.5	V
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input voltage			0	V_{CC}	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current		A port		−80	mA
			B port		−32	
I_{OL}	Low-level output current		A port		188	mA
			B port		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	Control inputs		4	ns/V
			A or B ports		10	
T_A	Operating free-air temperature			−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

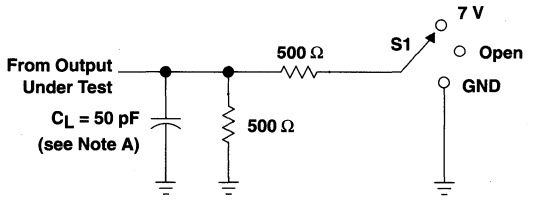
PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}	A port	V_{CC} = 4.75 V,	I_{OH} = −3 mA		2.7			V
		V_{CC} = 4.5 V,	I_{OH} = −80 mA		2.4			
	B port	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			
		V_{CC} = 5 V,	I_{OH} = −3 mA		3			
		V_{CC} = 4.5 V,	I_{OH} = −32 mA		2			
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 94 mA				0.55	V
			I_{OL} = 188 mA				0.7	
	B port	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1	µA
	A or B ports						±100	
$I_{I(hold)}$	A or B ports	V_{CC} = 4.5 V	V_I = 0.8 V		100			µA
			V_I = 2 V		−100			
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V				−50	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100	µA
I_{CEX}		V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50	µA
I_O§	B port	V_{CC} = 5.5 V,	V_O = 2.5 V		−50		−210	mA
I_{CC}		V_{CC} = 5.5 V, V_I = V_{CC} or GND	Outputs open,	Outputs high			500	µA
				Outputs low			20	mA
				Outputs disabled			500	µA
ΔI_{CC}¶		V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1	mA
C_i	Control inputs	V_{CC} = 5 V,	V_I = V_{CC} or GND			4		pF
C_{io}	A or B ports	V_{CC} = 5 V,	V_O = V_{CC} or GND			11.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

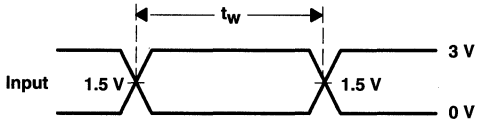
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1	2.3	3.5	1	3.9	ns
t_{PHL}			1	2.4	3.5	1	4.3	
t_{PZH}	$\overline{OE}$	A or B	1.5	3.7	5.4	1.5	6.5	ns
t_{PZL}			1.4	4	5.8	1.4	6.8	
t_{PHZ}	$\overline{OE}$	A or B	2	4.3	6.1	2	7.2	ns
t_{PLZ}			2	3.9	5.8	2	6.4	

PARAMETER MEASUREMENT INFORMATION

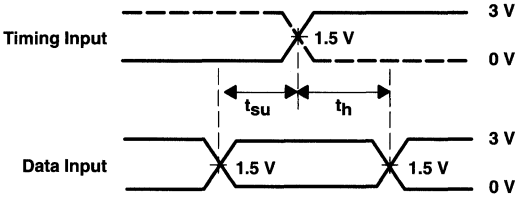


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

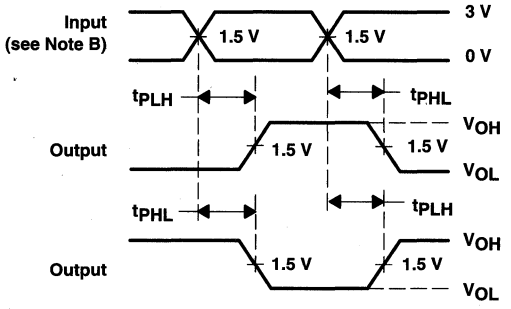
LOAD CIRCUIT FOR OUTPUTS



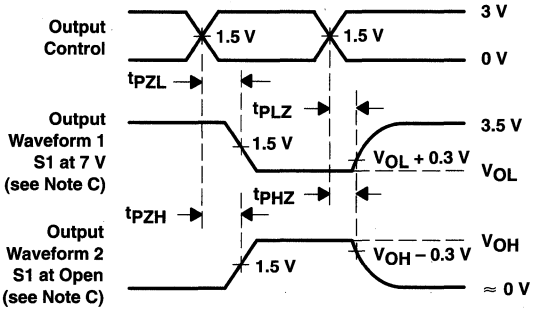
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

Futurebus+/BTL TRANSCEIVERS

Features

- Fully compatible with IEEE 1194.1-1991 (BTL) and IEEE 896-1991 (Futurebus+) standards
- Sub-5-ns performance
- 7-, 8-, and 9-bit versions
- 18-channel transceiver version
- TTL A port and BTL B port
- BTL edge rates > 2 ns/V
- Split I/O TTL port
- BIAS V_{CC} pin
- TTL input clamp circuitry
- Open-collector BTL outputs
- Isolated logic GNDs and bus GNDs
- JTAG test access port (TAP) availability on Futurebus+ transceivers
- 52-pin standard quad flat package and 100-pin shrink quad flat package availability
- TI has established an alternate source

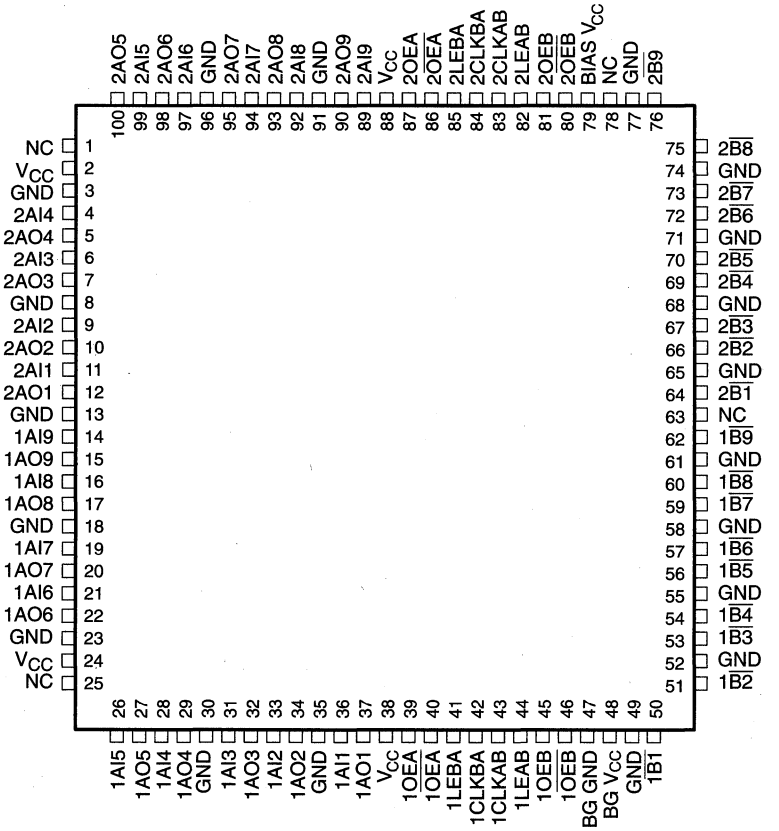
Benefits

- Execute proper BTL and Futurebus+ protocol
- ABT speed for Futurebus+ or advanced backplane transceiving
- Perform status/synch functions in Futurebus+ applications as well as UBT™ function in general-purpose BTL applications
- Can implement a full Futurebus+ interface with single-side mounting
- TTL-BTL and BTL-TTL translation
- High-throughput interface ideally suited for low-noise backplane applications
- Input and output pin separation allows for simultaneous data load/unload
- Minimize distortion during live insertion/withdrawal
- Allow for active termination
- High-drive 100-mA sink capability provides IWS capability down to 10 Ω
- Minimize device-generated noise and transmission environment noise
- Pins allocated for 4-wire IEEE 1149.1-1990 standard test bus, which will be implemented in future versions
- Fine-pitch surface-mount packaging saves valuable board space and meets Futurebus+ connector requirements
- Standardization that comes from a common product approach

AUGUST 1992 – REVISED JULY 1993

- **Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **Packaged in the High-Power Shrink Quad Flat Packages (SQFP) With 0.5-mm Pin Pitch**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **TTL Input Structures Incorporate Active Clamping and Bus Hold Networks**

PCA PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

AUGUST 1992 – REVISED JULY 1993

description

The SN74FB1650 contains two 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments. It is specifically designed to be compatible with IEEE 1194.1-1 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The $\overline{B}$ port operates at BTL signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

The A port operates at TTL signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

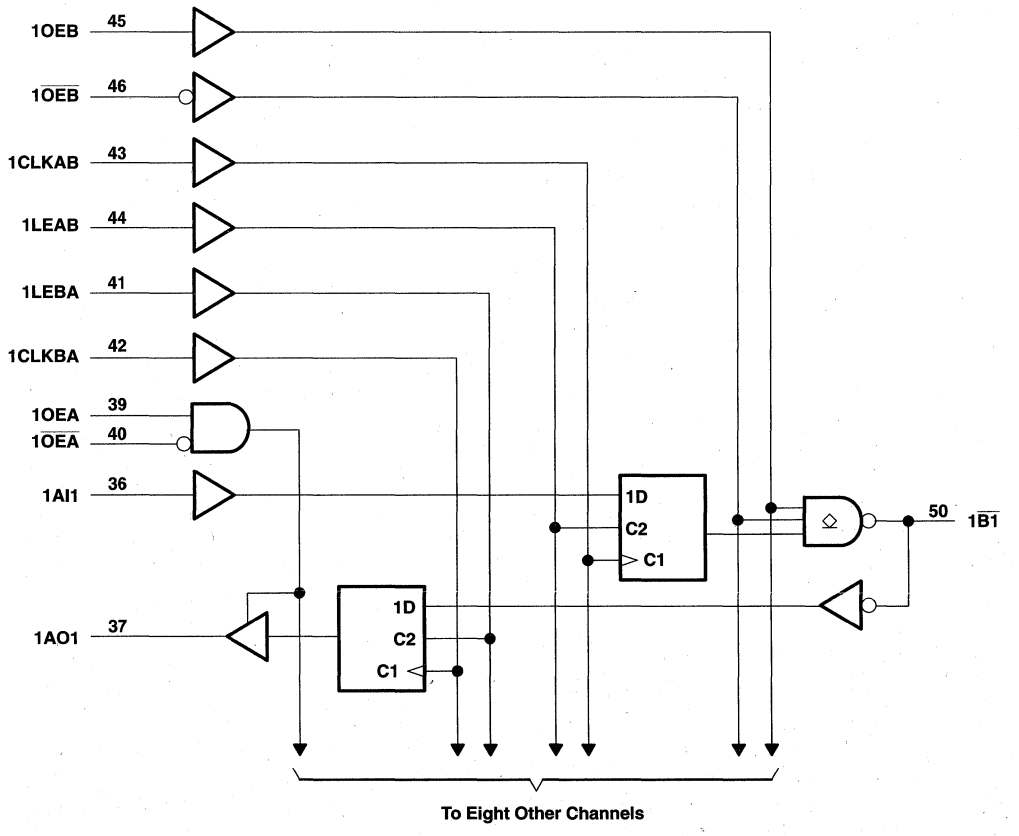
BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN74FB1650 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TRANSCEIVER FUNCTION TABLE

INPUTS				FUNCTION
$\overline{OEA}$	OEA	OEB	$\overline{OEB}$	
X	X	H	L	$\overline{A}$ data to B bus
L	H	X	X	$\overline{B}$ data to A bus
L	H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

STORAGE MODE TABLE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (except $\overline{B}$ port) . . . . . −1.2 V to 7 V
V_I ($\overline{B}$ port) . . . . . −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) . . . . . −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state . . . . . −5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . −5 V to V_{CC}
Current applied to any single output in the low state: A port . . . . . 96 mA
$\overline{B}$ port . . . . . 200 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A port			−3	mA
I_{OL}	Low-level output current	A port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
	Except $\overline{B}$ port and AO port	V_{CC} = 4.75 V,	I_I = −40 mA			−0.5	V
V_{OH}	AO port	V_{CC} = 4.75 V	I_{OH} = −1 mA				V
			I_{OH} = −3 mA	2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.35	0.5	V
	B port	V_{CC} = 4.75 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 5.25 V			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 0.5 V			−50	µA
	$\overline{B}$ port†	V_{CC} = 5.25 V,	V_I = 0.75 V			−100	
$I_{I(hold)}$	AI port	V_{CC} = 5.25 V,	V_I = 2 V	−100			µA
	AI port	V_{CC} = 5.25 V,	V_I = 0.5 V	100			
I_{OZH}	AO port	V_{CC} = 5.25 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.25 V,	V_O = 0.5 V			−50	µA
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.25 V,	V_O = 2.1 V			100	µA
I_{OS}§	A port	V_{CC} = 5.25 V,	V_O = 0	−30		−150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.25 V,	I_O = 0		25		mA
	$\overline{B}$ port to A port				60		
	Outputs disabled						
C_i		V_I = V_{CC} or GND				5	pF
C_o	A port	V_O = V_{CC} or GND					pF
C_{io}	B port per P1194.0	V_{CC} = 0 to 4.75 V				6	pF
		V_{CC} = 4.75 V to 5.25 V				5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.75 V,	V_B = 0 to 2 V	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			450	µA
		V_{CC} = 4.25 V to 5.25 V					10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		1.62		2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0 ,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	−1			µA
		V_{CC} = 0 to 5.25 V,	OEB = 0 to 0.8 V				100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V				100	

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			MIN	TYP	MAX	UNIT
t_w	Pulse duration, LCA or LCB					ns
t_{su}	Setup time	A or $\overline{B}$ before LE			2	ns
		A or $\overline{B}$ before CLK↑			2	
t_h	Hold time	A or $\overline{B}$ after LE			1	ns
		A or $\overline{B}$ after CLK↑			1	

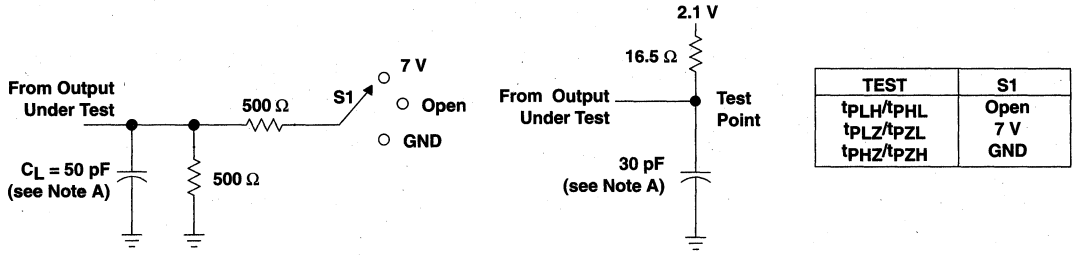
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A	$\overline{B}$			5	ns
t_{PHL}					5	
t_{PLH}	LEAB	$\overline{B}$			6	ns
t_{PHL}					6	
t_{PLH}	CLKAB	$\overline{B}$			6	ns
t_{PHL}					6	
t_{PLH}	LEBA	A			6	ns
t_{PHL}					6	
t_{PLH}	CLKBA	A			6	ns
t_{PHL}					6	
t_{PLH}	$\overline{B}$	A			5	ns
t_{PHL}					5	
t_{PLH}	OEB or $\overline{OEB}$	$\overline{B}$			5	ns
t_{PHL}					5	
t_{PZH}	OEA or $\overline{OEA}$	A			5	ns
t_{PZL}					5	
t_{PHZ}	OEA or $\overline{OEA}$	A			5	ns
t_{PLZ}					5	
$t_{sk(p)}$‡	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	A to $\overline{B}$ or $\overline{B}$ to A		0.5		ns
$t_{sk(o)}$‡	Skew between drivers in the same package	A to $\overline{B}$ or $\overline{B}$ to A		1		ns
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		1	2	3	ns
t_{PR}	$\overline{B}$-port input pulse rejection			1		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Skew values are applicable for through mode only.

PRODUCT PREVIEW

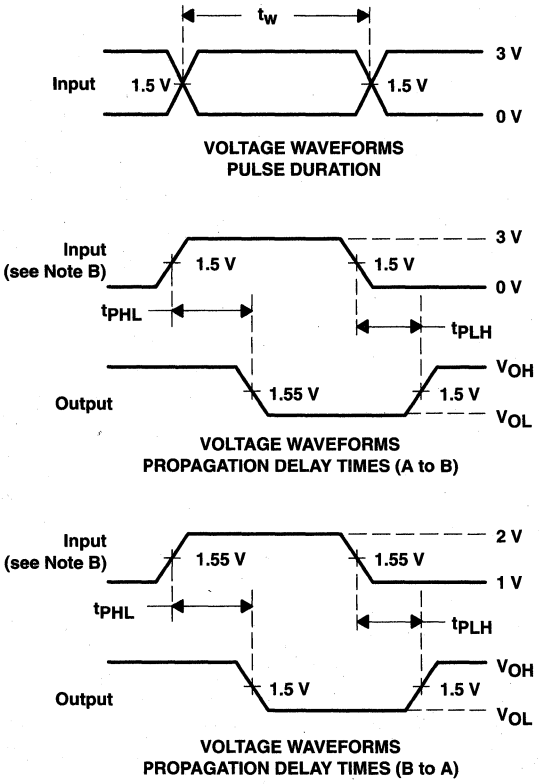
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR A OUTPUTS

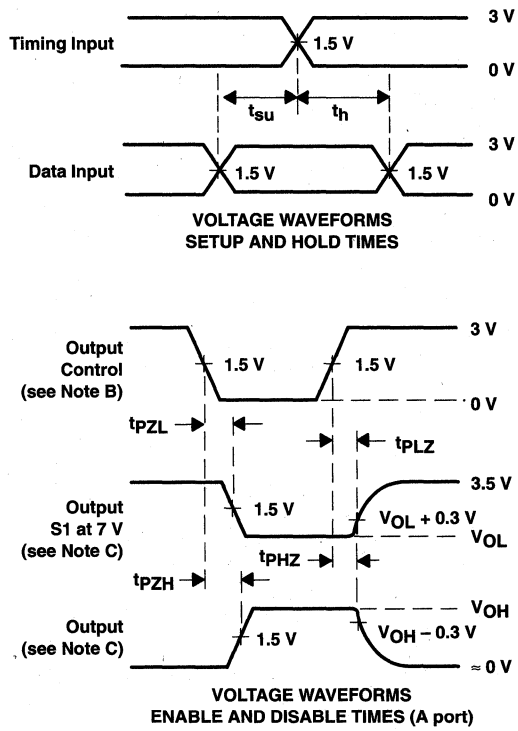
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL Inputs - PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns. BTL Inputs - PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

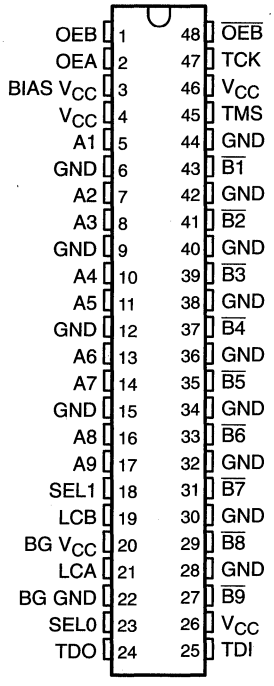
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

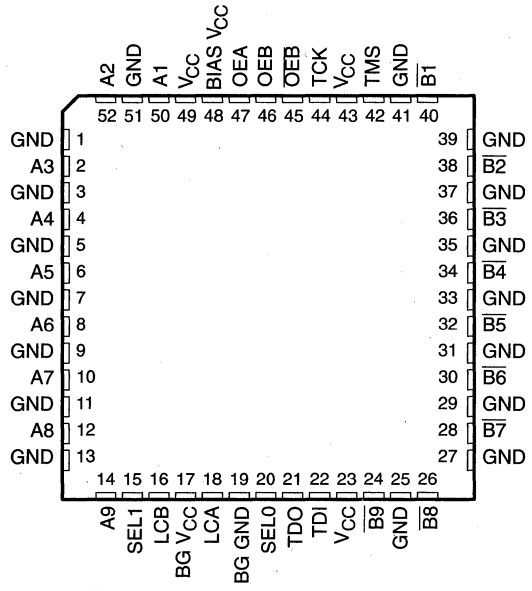
NOVEMBER 1991 – REVISED JULY 1993

- **Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Minimum $\overline{B}$-Port Edge Rate = 2 ns**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **Available in Plastic Quad Flatpack (RC) and Ceramic Flatpack (WD) Packages**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**

SN54FB2031 . . . WD PACKAGE
(TOP VIEW)



SN74FB2031 . . . RC PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'FB2031 is a 9-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. It is specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

description (continued)

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2031. Currently TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN54FB2031 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74FB2031 is characterized for operation from 0°C to 70°C.

TRANSCEIVER FUNCTION TABLE

INPUTS			FUNCTION
OEA	OEB	$\overline{OEB}$	
L	H	L	$\overline{A}$ data to B bus
H	L	X	$\overline{B}$ data to A bus
H	X	H	
H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
L	L	X	Isolation
L	X	H	

STORAGE MODE TABLE

LCA, LCB	RESULT
0	Transparent
1	Latches latched
↑	Flip-flops triggered

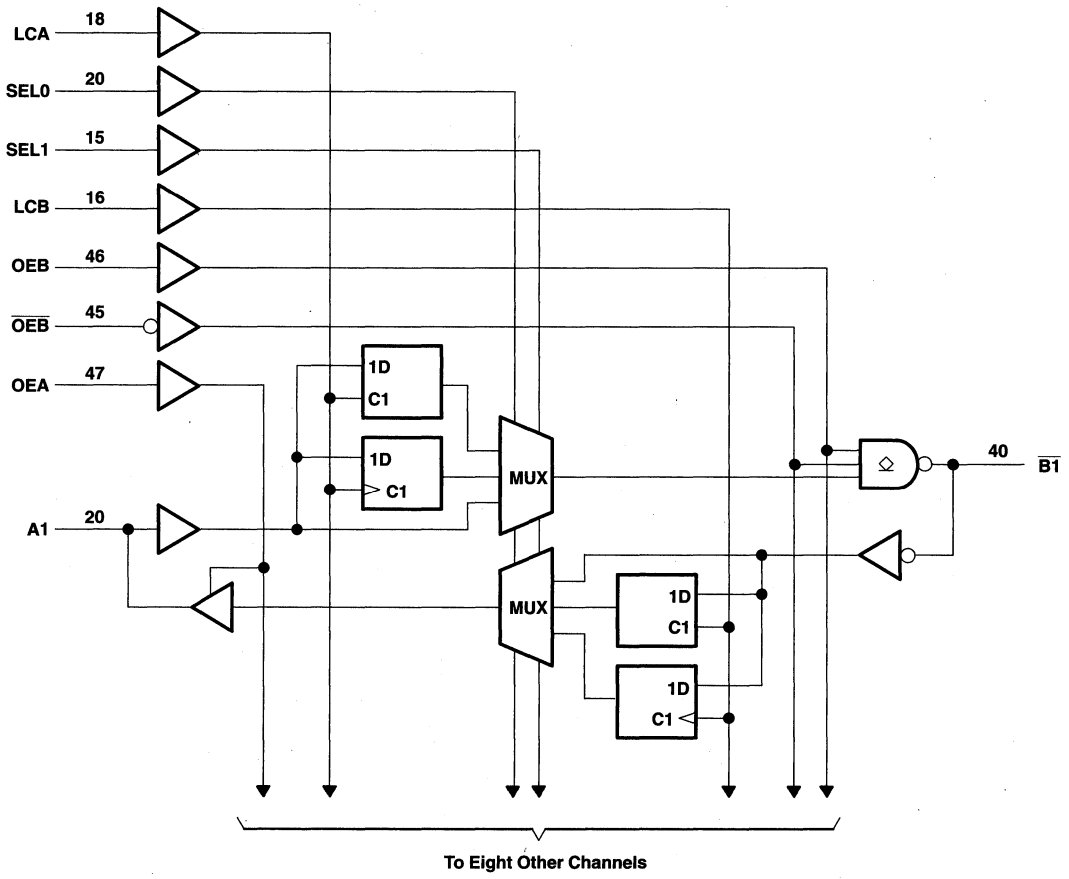
SELECT FUNCTION TABLE

SEL1	SEL0	MUX A→B	MUX B→A
0	0	Latch	Latch
0	1	Thru	Thru
1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except $\overline{B}$ port) ..... −1.2 V to 7 V
V_I ($\overline{B}$ port) ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −5 V to 5.5 V
Voltage range applied to any output in the high state ..... −5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 96 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air): RC package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

recommended operating conditions (see Note 1)

			SN54FB2031			SN74FB2031			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A port						−3	mA
I_{OL}	Low-level output current	A port						24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2031			SN74FB2031			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V,	I_I = −18 mA						−1.2	V
	Except $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = −40 mA						−0.5	
V_{OH}	A port	V_{CC} = 4.5 V	I_{OH} = −1 mA							V
			I_{OH} = −3 mA				2.5	3.3		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 20 mA							V
			I_{OL} = 24 mA					0.35	0.5	
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA				0.75		1.1	
			I_{OL} = 100 mA							
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V						50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V						50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V						−50	µA
	$\overline{B}$ port†	V_{CC} = 5.5 V,	V_I = 0.75 V						−100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V						100	µA
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0				−30		−150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0					25		mA
	$\overline{B}$ port to A port							60		
	Outputs disabled									
C_i		V_I = V_{CC} or GND							5	pF
C_o	A port	V_O = V_{CC} or GND								pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.5 V							6	pF
		V_{CC} = 4.5 V to 5.5 V							5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

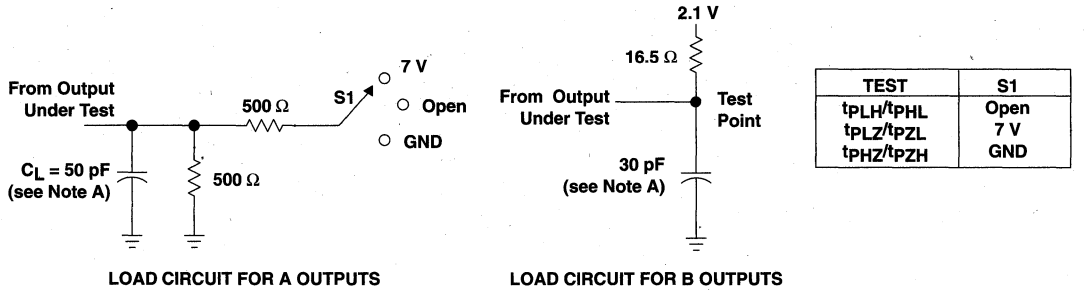
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB2031		SN74FB2031		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A (thru mode)	$\overline{B}$			5					ns
t_{PHL}					5					
t_{PLH}	A (transparent)	$\overline{B}$			6					ns
t_{PHL}					6					
t_{PLH}	LCA	$\overline{B}$			7					ns
t_{PHL}					7					
t_{PLH}	LCB	A			9					ns
t_{PHL}					9					
t_{PLH}	SEL1 or SEL0	A			5.5					ns
t_{PHL}					5.5					
t_{PLH}	SEL1 or SEL0	$\overline{B}$			7					ns
t_{PHL}					7					
t_{PLH}	$\overline{B}$ (thru mode)	A			6					ns
t_{PHL}					6					
t_{PLH}	$\overline{B}$ (transparent)	A			7					ns
t_{PHL}					7					
t_{PLH}	OEB or $\overline{OEB}$	$\overline{B}$			5.5					ns
t_{PHL}					5.5					
t_{PZH}	OEA	A			4					ns
t_{PZL}					4					
t_{PHZ}	OEA	A			5					ns
t_{PLZ}					5					
$t_{sk(p)}$	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	A to $\overline{B}$ or $\overline{B}$ to A		0.5						ns
$t_{sk(o)}$	Skew between drivers in the same package	A to $\overline{B}$ or $\overline{B}$ to A		1						ns
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)			2				1	3	ns
t_{PR}	$\overline{B}$-port input pulse rejection							1		ns

live insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			SN54FB2031		SN74FB2031		UNIT
					MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V				450	µA
		V_{CC} = 4.5 V to 5.5 V						10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V				1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V					100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V					100	

PRODUCT PREVIEW

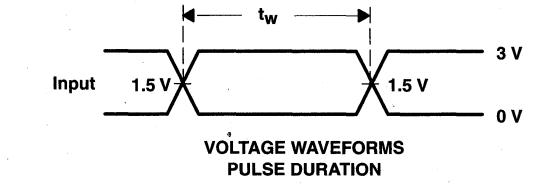
PARAMETER MEASUREMENT INFORMATION



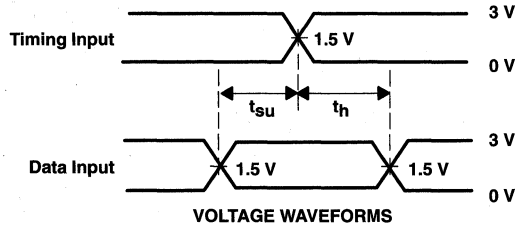
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR A OUTPUTS

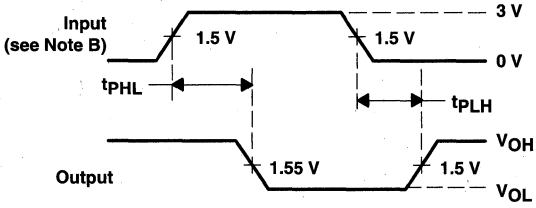
LOAD CIRCUIT FOR B OUTPUTS



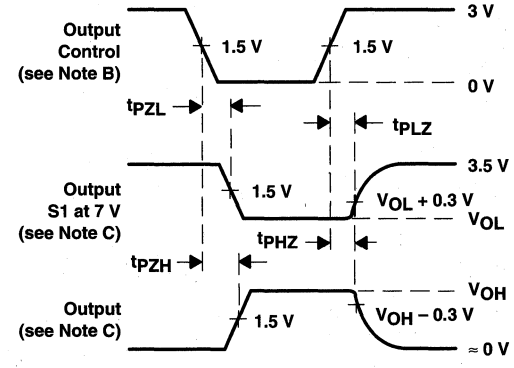
VOLTAGE WAVEFORMS
PULSE DURATION



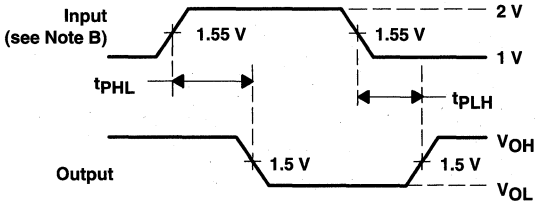
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL Inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL Inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

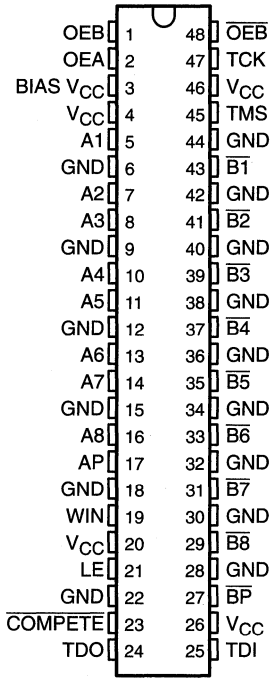
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

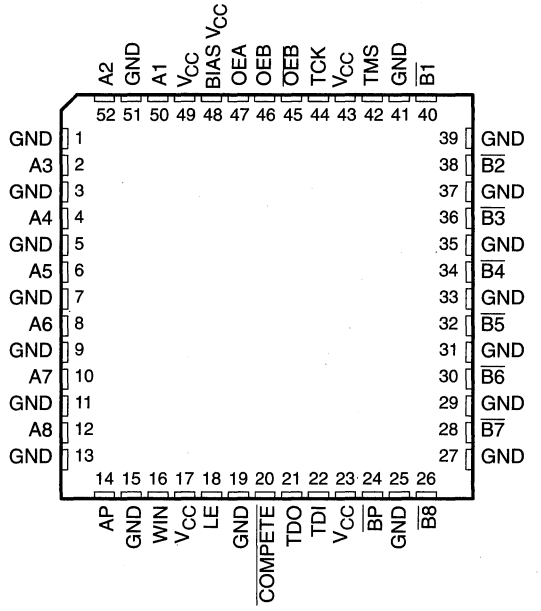
NOVEMBER 1991 – REVISED JULY 1993

- **Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Minimum $\overline{B}$-Port Edge Rate = 2 ns**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **Available in Plastic Quad Flatpack (RC) and Ceramic Flatpack (WD) Packages**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**

SN54FB2032 . . . WD PACKAGE
(TOP VIEW)



SN74FB2032 . . . RC PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'FB2032 is a 9-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments and to perform bus arbitration. It is specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

description (continued)

The A-port data can be latched by taking the latch enable (LE) high. When LE is low, the latches are transparent.

The Futurebus+ protocol logic can be activated by taking $\overline{\text{COMPETE}}$ low. The module (device) then compares its A data (arbitration number) against the A data of another identical module also connected to the $\overline{\text{B}}$ arbitration bus, and sets WIN high if the A data is greater than the A data of the other module (i.e., has higher priority). A8 and $\overline{\text{B8}}$ are the most significant bits, and A1 and $\overline{\text{B1}}$ are the least significant bits. If OEB is high and $\overline{\text{OEB}}$ is low during this operation, and the A bus of the first module wins priority, it will assert its arbitration number on the $\overline{\text{B}}$-arbitration bus.

AP and $\overline{\text{BP}}$ are the bus parity bits. The winning module may assert $\overline{\text{BP}}$ low if its parity bit (AP) is high.

In a typical operating sequence, a Futurebus+ arbitration controller will latch its arbitration number into the A port and wait for the results of a competition. When the competition is complete, and if the controller's arbitration number did not win, the controller will read back the current value of the $\overline{\text{B}}$ bus (by taking OEA high) and determine the winning arbitration number. This allows the module to change its arbitration number for the next competition cycle, if desired.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2032. Currently TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN54FB2032 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74FB2032 is characterized for operation from 0°C to 70°C.

TRANSCEIVER FUNCTION TABLE

INPUTS			FUNCTION
OEA	OEB	$\overline{\text{OEB}}$	
L	H	L	$\overline{\text{A}}$ data to B bus
H	L	X	$\overline{\text{B}}$ data to A bus
H	X	H	
H	H	L	$\overline{\text{A}}$ data to B bus, $\overline{\text{B}}$ data to A bus
L	L	X	Isolation
L	X	H	

STORAGE MODE TABLE

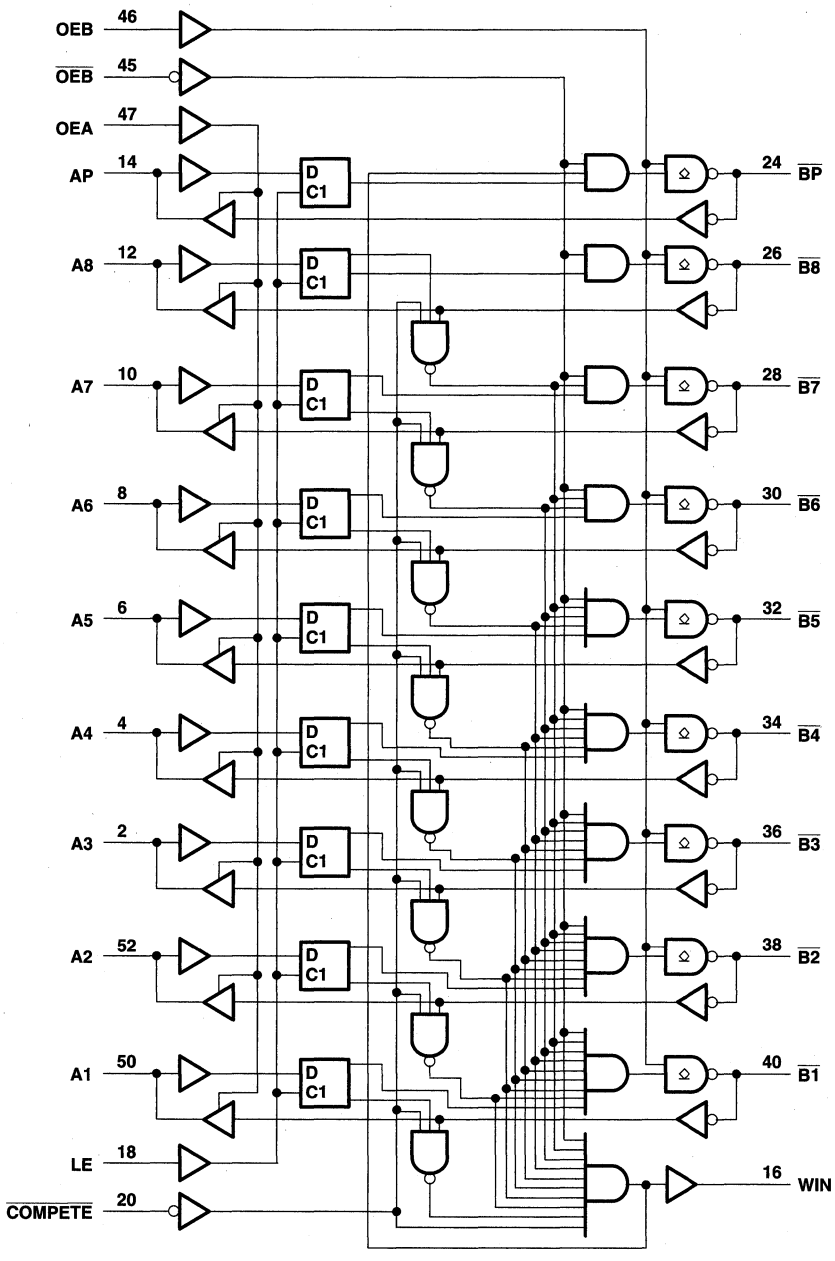
LCA, LCB	RESULT
0	Transparent
1	Latches latched
↑	Flip-flops triggered

SELECT FUNCTION TABLE

SEL1	SEL0	MUX A→B	MUX B→A
0	0	Latch	Latch
0	1	Thru	Thru
1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch

PRODUCT PREVIEW

functional block diagram



Pin numbers shown are for the RC package.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except $\overline{BP}$, $\overline{B}$ port) ..... −1.2 V to 7 V
V_I ($\overline{BP}$, $\overline{B}$ port) ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 96 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air): RC package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			SN54FB2032			SN74FB2032			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{BP}$, $\overline{B}$ port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{BP}$, $\overline{B}$ port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	AP, WIN, A port						−3	mA
I_{OL}	Low-level output current	AP, WIN, A port						24	mA
		$\overline{BP}$, $\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2032			SN74FB2032			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –18 mA						–1.2	V
	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –40 mA						–0.5	
V_{OH}	AP, WIN, A port	V_{CC} = 4.5 V	I_{OH} = –1 mA							V
			I_{OH} = –3 mA				2.5	3.3		
V_{OL}	AP, WIN, A port	V_{CC} = 4.5 V	I_{OL} = 20 mA							V
			I_{OL} = 24 mA					0.35	0.5	
	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA				0.75		1.1	
			I_{OL} = 100 mA							
I_I	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V						50	µA
I_{IH}‡	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V						50	µA
I_{IL}‡	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V						–50	µA
	$\overline{BP}$, $\overline{B}$ port†	V_{CC} = 5.5 V,	V_I = 0.75 V						–100	
I_{OH}	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V						100	µA
I_{OS}§	AP, WIN, A port	V_{CC} = 5.5 V,	V_O = 0				– 30		–150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0					25		mA
	$\overline{B}$ port to A port							60		
	Outputs disabled									
C_i		V_I = V_{CC} or GND							5	pF
C_o	A port	V_O = V_{CC} or GND								pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.5 V							6	pF
		V_{CC} = 4.5 V to 5.5 V							5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB2032		SN74FB2032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or AP	$\overline{B}$ or $\overline{BP}$							8	ns
t_{PHL}									8	
t_{PLH}	A	$\overline{B}_{n-1}$							9	ns
t_{PHL}									9	
t_{PLH}	A	$\overline{BP}$							10	ns
t_{PHL}									10	
t_{PLH}	$\overline{B}$	$\overline{B}_{n-1}$							9	ns
t_{PHL}									9	
t_{PLH}	LE	$\overline{B}$							7.5	ns
t_{PHL}									7.5	
t_{PLH}	LE	$\overline{BP}$							7.5	ns
t_{PHL}									7.5	
t_{PLH}	$\overline{B}$ or $\overline{BP}$	A or AP							7.5	ns
t_{PHL}									7.5	
t_{PLH}	$\overline{B}$	WIN							8.5	ns
t_{PHL}									8.5	
t_{PLH}	A	WIN							7.6	ns
t_{PHL}									7.6	
t_{PLH}	LE	WIN							7	ns
t_{PHL}									7	
t_{PLH}	$\overline{COMPETE}$	WIN							5.5	ns
t_{PHL}									5.5	
t_{PLH}	$\overline{OEB}$	WIN							6	ns
t_{PHL}									6	
t_{PLH}	$\overline{COMPETE}$	$\overline{B}$							7.5	ns
t_{PHL}									7.5	
t_{PLH}	$\overline{COMPETE}$	$\overline{BP}$							6.5	ns
t_{PHL}									6.5	
t_{PLH}	OEB	$\overline{B}$							6.5	ns
t_{PHL}									6.5	
t_{PLH}	$\overline{OEB}$	$\overline{B}$							6.5	ns
t_{PHL}									6.5	
t_{PZH}	OEA	A							5.5	ns
t_{PZL}									5.5	
t_{PHZ}	OEA	A							7	ns
t_{PLZ}									7	
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)			2				1	3	ns
t_{PR}	$\overline{B}$-port input pulse rejection								1	ns

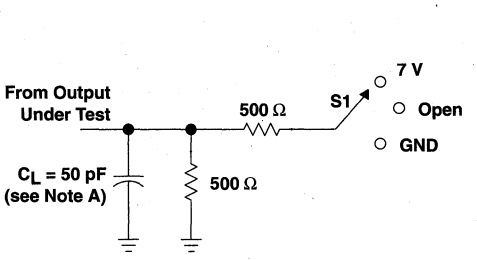
PRODUCT PREVIEW

live insertion specifications over recommended operating free-air temperature range

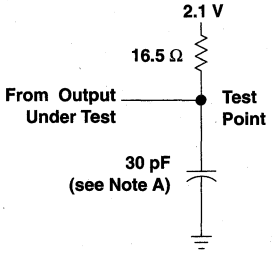
PARAMETER		TEST CONDITIONS		SN54FB2032		SN74FB2032		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V				450	μA
		V_{CC} = 4.5 V to 5.5 V					10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0 ,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			–1		μA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V				100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V				100	

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

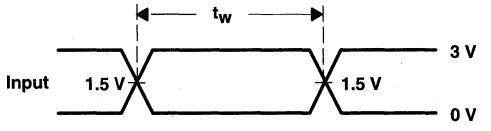


LOAD CIRCUIT FOR A OUTPUTS

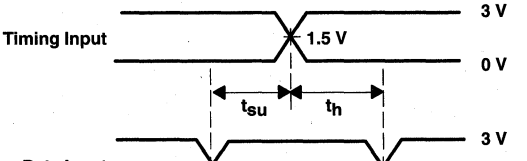


LOAD CIRCUIT FOR B OUTPUTS

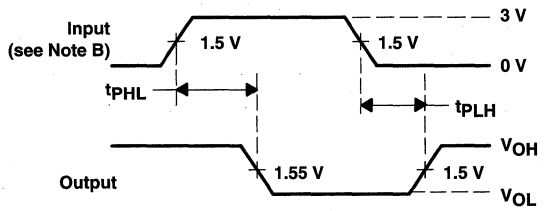
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



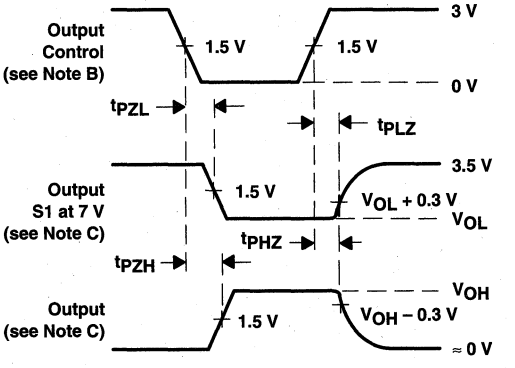
VOLTAGE WAVEFORMS
PULSE DURATION



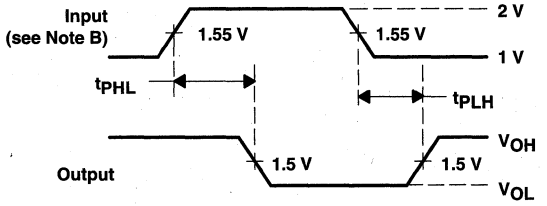
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL Inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL Inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

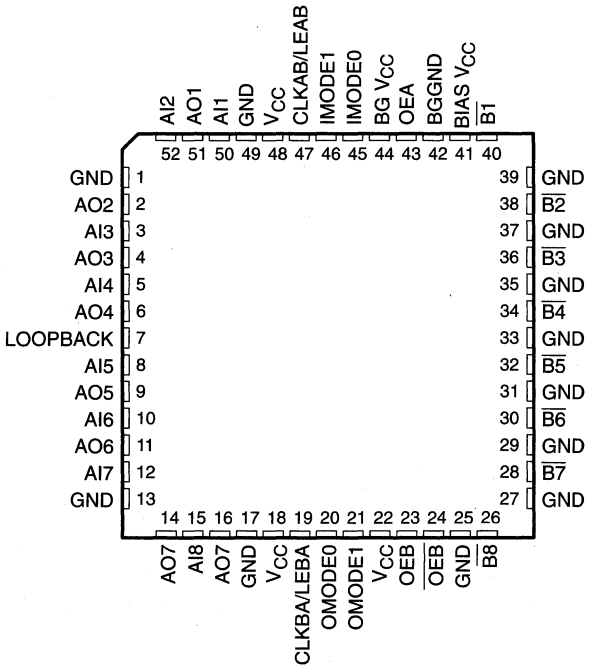
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

D4521, NOVEMBER 1990 – REVISED JULY 1993

- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **Packaged in Plastic Quad Flat Packages (PQFP) With 0.65-mm Pin Pitches**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**

RC PACKAGE
(TOP VIEW)



description

The SN74FB2033 is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common I/O, open-collector $\overline{B}$ port operates at backplane transceiver logic (BTL) signal levels.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverse of the input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock pins serve as transparent-high latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, $\overline{B}$-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

description (continued)

The AO port enable/disable control is provided by OEA. When OEA is low or when V_{CC} is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The $\overline{B}$ port is controlled by OEB and $\overline{OEB}$. If OEB is low or $\overline{OEB}$ is high or when V_{CC} is typically less than 2.5 V the $\overline{B}$ port is inactive. If OEB is high and $\overline{OEB}$ is low, the B port is active.

BG V_{CC} and BG GND are the bias generator reference inputs.

The A-to-B and B-to-A logic elements are active regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive ($\overline{B}$ port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on V_{OH} during a low-to-high transition. The other clamps out ringing below the BTL V_{OL} voltage of 0.75 V. Both these clamps are only active during AC switching and do not affect the BTL outputs during steady-state conditions.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN74FB2033 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS								FUNCTION/MODE
OEA	OEB	$\overline{OEB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	
L	L	X	X	X	X	X	X	Isolation
L	X	H	X	X	X	X	X	
X	H	L	L	L	X	X	X	AI to $\overline{B}$, buffer mode
X	H	L	L	H	X	X	X	AI to $\overline{B}$, flip-flop mode
X	H	L	H	X	X	X	X	AI to $\overline{B}$, latch mode
H	L	X	X	X	L	L	L	$\overline{B}$ to AO, buffer mode
H	X	H	X	X	L	L	L	
H	L	X	X	X	L	H	L	$\overline{B}$ to AO, flip-flop mode
H	X	H	X	X	L	H	L	
H	L	X	X	X	H	X	L	$\overline{B}$ to AO, latch mode
H	X	H	X	X	H	X	L	
H	L	X	X	X	L	L	H	AI to AO, buffer mode
H	X	H	X	X	L	L	H	
H	L	X	X	X	L	H	H	AI to AO, flip-flop mode
H	X	H	X	X	L	H	H	
H	L	X	X	X	H	X	H	AI to AO, latch mode
H	X	H	X	X	H	X	H	
H	H	L	X	X	X	X	L	AI to $\overline{B}$, $\overline{B}$ to AO

Function Tables

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEA	OEB	$\overline{OEB}$	AO	$\overline{B}$
L	X	X	Z	
H	X	X	Active (H or L)	
X	L	L		Inactive (H)
X	L	H		Inactive (H)
X	H	L		Active (H or L)
X	H	H		Inactive (H)

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q_0

LOOPBACK

LOOPBACK	Q†
L	$\overline{B}$ port
H	Point P‡

† Q is the input to the B-to-A logic element.
‡ P is the output of the A-to-B logic element (see functional block diagram).

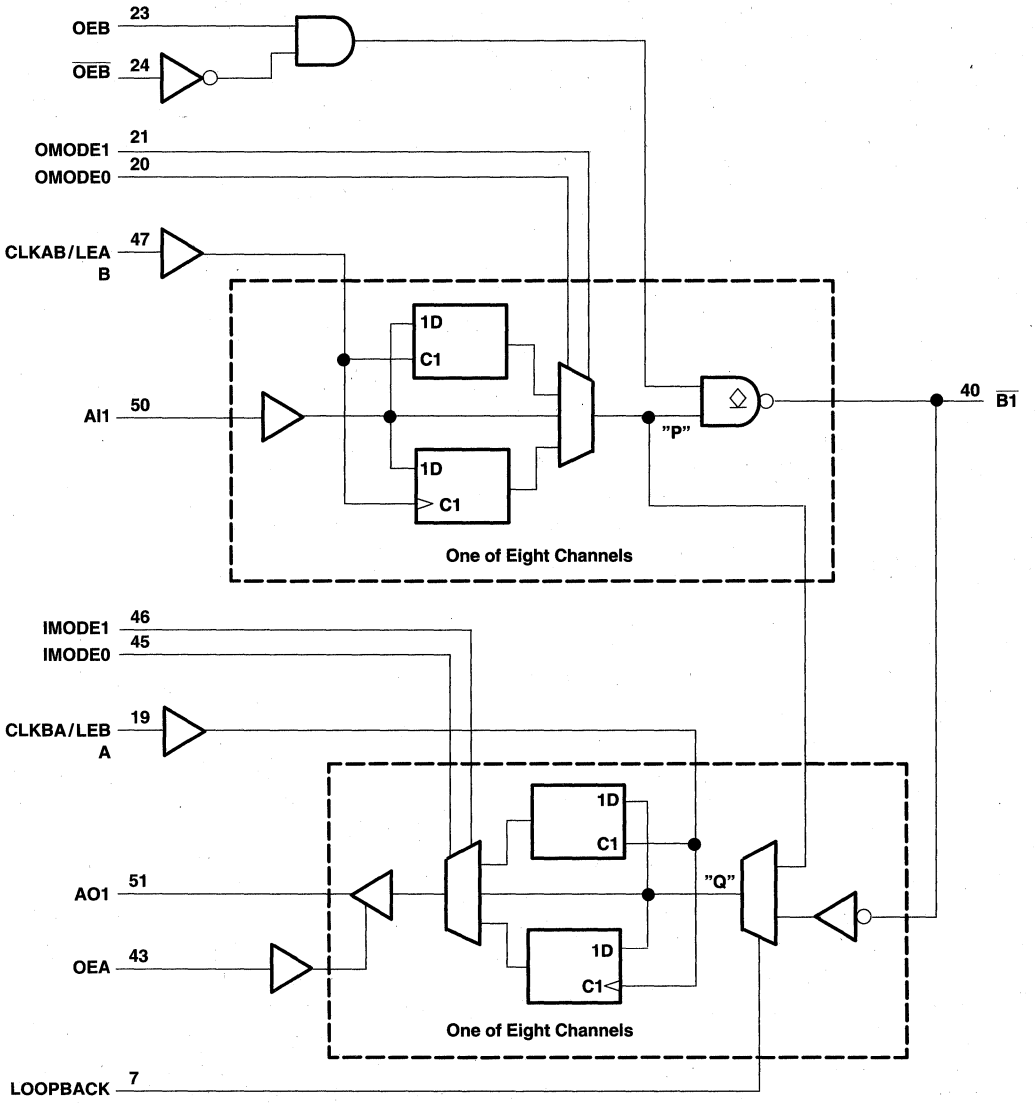
SELECT

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	H
↑	H	L

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except $\overline{B}$ port) ..... −1.2 V to 7 V
V_I ($\overline{B}$ port) ..... −1.2 V to 3.5 V
Input current range, (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any B output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 96 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{OH}	High-level output current	AO port			−3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	AO port	V_{CC} = 4.75 V to 5.25 V,	I_{OH} = −10 µA			V_{CC}−1.1	V
		V_{CC} = 4.75 V	I_{OH} = −3 mA	2.5	2.85	3.4	
			I_{OH} = −32 mA	2			
V_{OL}	AO port	V_{CC} = 4.75 V	I_{OL} = 20 mA		0.33	0.5	V
			I_{OL} = 55 mA			0.8	
	$\overline{B}$ port	V_{CC} = 4.75 V	I_{OL} = 100 mA	0.75		1.1	
			I_{OL} = 4 mA	0.5			
I_I	Except $\overline{B}$ port	V_{CC} = 0,	V_I = 5.25 V			100	µA
I_{IH}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 2.7 V			50	µA
	$\overline{B}$ port†	V_{CC} = 0 to 5.25 V,	V_I = 2.1 V			100	
I_{IL}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 0.5 V			−50	µA
	$\overline{B}$ port†	V_{CC} = 5.25 V,	V_I = 0.75 V			−100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.25 V,	V_O = 2.1 V			100	µA
I_{OZH}	AO port	V_{CC} = 5.25 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.25 V,	V_O = 0.5 V			−50	µA
I_{OS}‡	AO port	V_{CC} = 5.25 V,	V_O = 0	−40	−80	−150	mA
I_{CC}	All outputs on	V_{CC} = 5.25 V,	I_O = 0		45	60	mA
C_i	AI port and control inputs	V_I = V_{CC} or GND			5		pF
C_o	AO port	V_O = V_{CC} or GND			5		pF
C_{io}§	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.75 V				6	pF
		V_{CC} = 4.75 V to 5.25 V				6	

† For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
§ Parameter is based on characterization data but is not tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	150	0	150	MHz
t_w	Pulse duration, CLKAB/LEAB or CLKBA/LEBA	4		4		ns
t_{su}	Setup time, data before CLKAB/LEAB or CLKBA/LEBA↑	4		4		ns
t_h	Hold time, data after CLKAB/LEAB or CLKBA/LEBA↑	1		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	AI (thru mode)	$\overline{B}$	2.3	3.8	5.3	1.8	6.5	ns
t_{PHL}			1.2	2.6	4	1.2	4.2	
t_{PLH}	$\overline{B}$ (thru mode)	AO	2.2	3.9	5.7	1.9	6.6	ns
t_{PHL}			3.8	5.2	6.7	3.2	7.3	
t_{PLH}	AI (transparent)	$\overline{B}$	3.5	5	6.7	2.9	8.1	ns
t_{PHL}			2.1	3.6	5.3	2	5.7	
t_{PLH}	$\overline{B}$ (transparent)	AO	2.6	4.3	6.3	2.3	7.2	ns
t_{PHL}			4.3	5.6	7.1	3.7	7.6	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	2.4	3.7	5.3	2	6.4	ns
t_{PHL}			1.2	2.6	4.1	1.2	4.4	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	2.5	3.8	5.3	2.2	6.4	ns
t_{PHL}			1.4	2.9	4.5	1.3	4.9	
t_{PZH}	OEA	AO	1.8	3.5	5.1	1.5	5.6	ns
t_{PZL}			2.6	4.3	5.9	1.8	6.2	
t_{PHZ}	OEA	AO	1.7	3.5	5.3	1.4	5.7	ns
t_{PLZ}			1	2.7	4.5	1	4.9	
t_{PLH}	CLKAB/LEAB	$\overline{B}$	3.5	5	6.7	3	8.1	ns
t_{PHL}			2	3.6	5.2	1.9	5.5	
t_{PLH}	CLKBA/LEBA	AO	2.2	3.8	5.4	1.9	5.8	ns
t_{PHL}			2.7	4.1	5.6	2.4	5.7	
t_{PLH}	OMODE	$\overline{B}$	3.2	4.8	6.5	2.7	7.9	ns
t_{PHL}			1.9	3.5	5.2	1.7	5.7	
t_{PLH}	IMODE	AO	2	3.6	5.3	1.7	6	ns
t_{PHL}			2.5	4.1	5.6	1.8	5.8	
t_{PLH}	LOOPBACK	AO	2.3	4.6	6.8	2	7.5	ns
t_{PHL}			3.2	4.8	6.4	2.9	6.4	
t_{PLH}	AI	AO	2.1	3.7	5.4	1.9	5.8	ns
t_{PHL}			2.9	4.3	5.9	2.5	6.4	
t_t	Rise time 1.3 V to 1.8 V	$\overline{B}$		1.5				ns
	Fall time 1.8 V to 1.3 V			1.5				
	Rise or fall time 10% to 90%	AO		3.5				
t_{PR}	$\overline{B}$-port input pulse rejection					1		ns

live insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			400	μA
		V_{CC} = 4.5 V to 5.5 V					10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		1.62		2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1			μA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V				100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V				100	

miscellaneous characteristics

			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OHP}†	Peak bus voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1			4	V
V_{OHV}†	Minimum bus voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1	1.62			V
V_{OLV}	Minimum bus voltage during high to low switch	$\overline{B}$ port	I_{OL} = –50 mA	0.3			V

† Parameter is based on characterization data but not tested.

PARAMETER MEASUREMENT INFORMATION

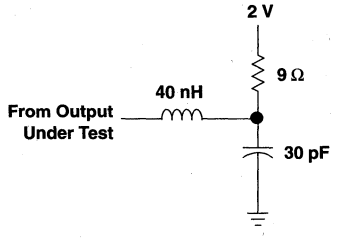
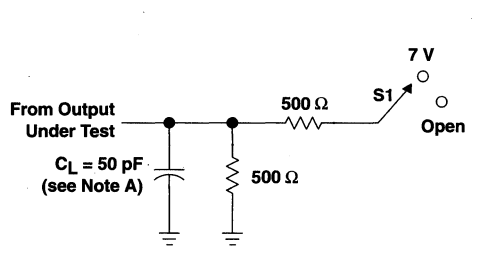
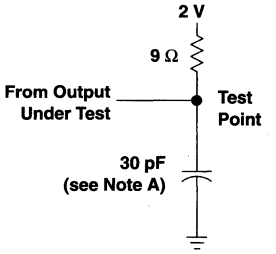


Figure 1. Load Circuit V_{OHP}, V_{OHV}

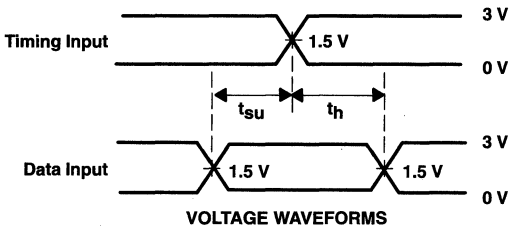


LOAD CIRCUIT FOR A OUTPUTS

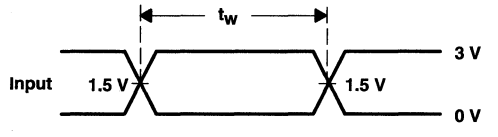


LOAD CIRCUIT FOR B OUTPUTS

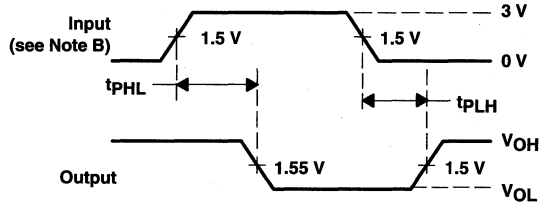
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



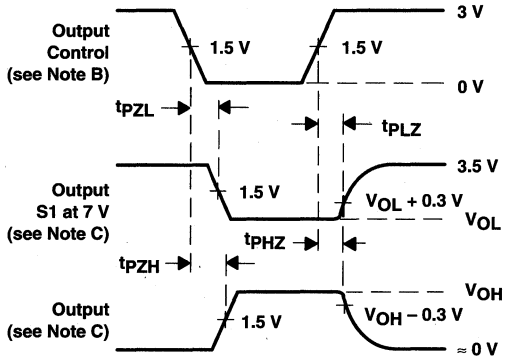
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



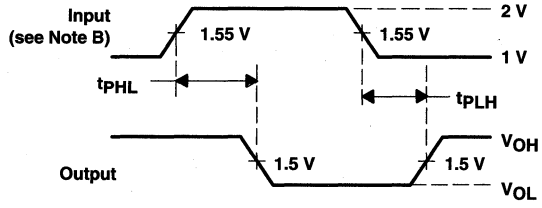
VOLTAGE WAVEFORMS
PULSE DURATION



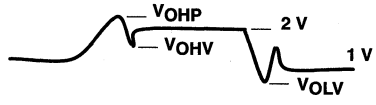
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
MISCELLANEOUS CHARACTERISTICS

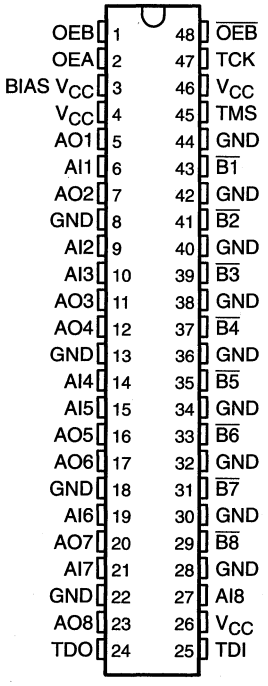
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns, BTL inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

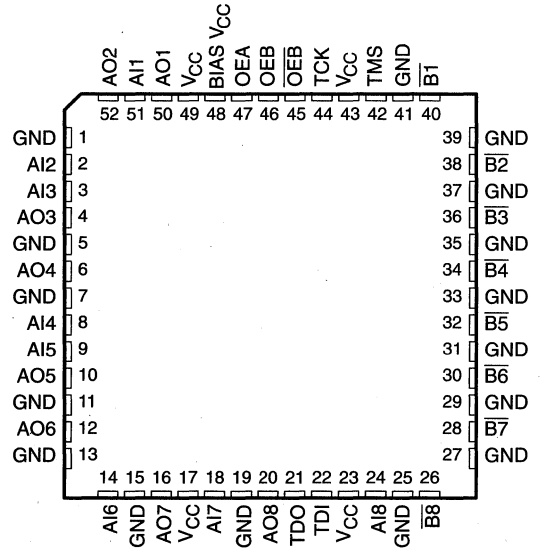
NOVEMBER 1991 – REVISED JULY 1993

- **Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Minimum $\overline{B}$-Port Edge Rate = 2 ns**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **Available in Plastic Quad Flatpack (RC) and Ceramic Flatpack (WD) Packages**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**

SN54FB2040 . . . WD PACKAGE
(TOP VIEW)



SN74FB2040 . . . RC PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'FB2040 is an 8-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. It is specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

description (continued)

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2040. Currently TMS and TCK are not connected and TDI is shorted to TDO.

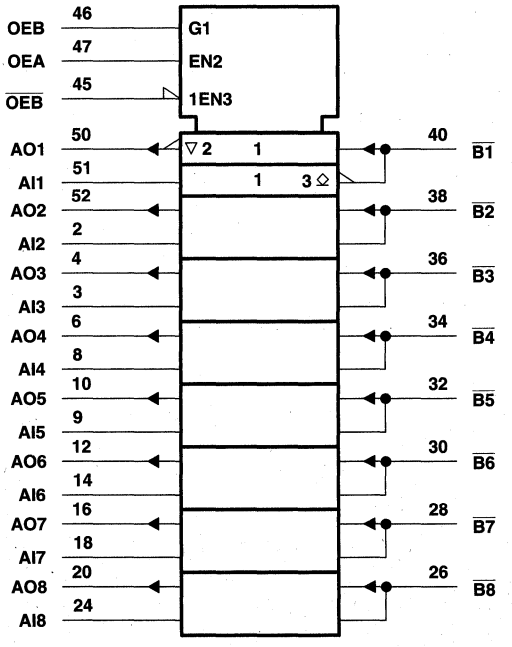
BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN54FB2040 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74FB2040 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L X	X H	L L	Isolation
L X	X H	H H	$\overline{B}$ data to AO bus
H	L	L	$\overline{AI}$ data to B bus
H	L	H	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus

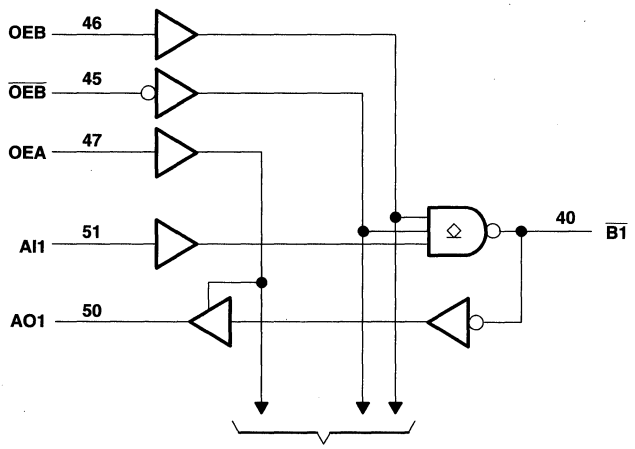
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the RC package.

PRODUCT PREVIEW

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except $\overline{B}$ port) ..... −1.2 V to 7 V
V_I ($\overline{B}$ port) ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −18 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 96 mA
($\overline{B}$ port) ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air): RC package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

recommended operating conditions (see Note 1)

			SN54FB2040			SN74FB2040			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	AO port						−3	mA
I_{OL}	Low-level output current	AO port						24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2040			SN74FB2040			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V,	I_I = −18 mA						−1.2	V
	Except $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = −40 mA						−0.5	
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = −1 mA							V
			I_{OH} = −3 mA				2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V	I_{OL} = 20 mA							V
			I_{OL} = 24 mA					0.35	0.5	
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA				0.75		1.1	
			I_{OL} = 100 mA						1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V						50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V						50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V						−50	µA
	$\overline{B}$ port†	V_{CC} = 5.5 V,	V_I = 0.75 V						−100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V						100	µA
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V						50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V						−50	µA
I_{OS}§	AO port	V_{CC} = 5.5 V,	V_O = 0				−30		−150	mA
I_{CC}	AI port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0					25		mA
	$\overline{B}$ port to AO port							60		
	Outputs disabled									
C_i	AI port and control inputs	V_I = V_{CC} or GND								pF
C_o	AO port	V_O = V_{CC} or GND								pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.5 V							6	pF
		V_{CC} = 4.5 V to 5.5 V							5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

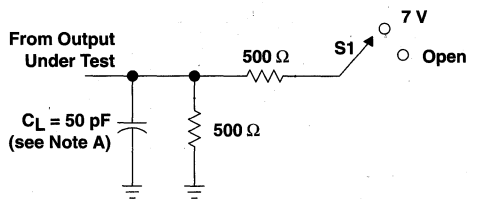
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB2040		SN74FB2040		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	AI	$\overline{B}$		3.9						ns
t_{PHL}				3.6						
t_{PLH}	$\overline{B}$	AO		3.9						ns
t_{PHL}				3.8						
t_{PLH}	OEB	$\overline{B}$		5.1						ns
t_{PHL}				4.3						
t_{PLH}	OEB	$\overline{B}$		4.4						ns
t_{PHL}				4.1						
t_{PZH}	OEA	AO		3.2						ns
t_{PZL}				3						
t_{PHZ}	OEA	AO		3.2						ns
t_{PLZ}				2.7						
$t_{sk(p)}$	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	AI to $\overline{B}$ or $\overline{B}$ to AO							0.75	ns
$t_{sk(o)}$	Skew between drivers in the same package	AI to $\overline{B}$ or $\overline{B}$ to AO		1	1.5				2	ns
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)			2				1	3	ns
t_{PR}	$\overline{B}$-port input pulse rejection							1		ns

live insertion specifications over recommended operating free-air temperature range

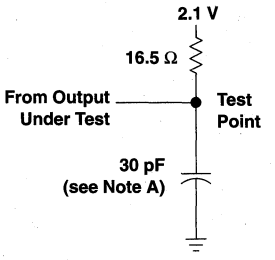
PARAMETER		TEST CONDITIONS		SN54FB2040		SN74FB2040		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V				450	µA
		V_{CC} = 4.5 V to 5.5 V					10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V				100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V				100	

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

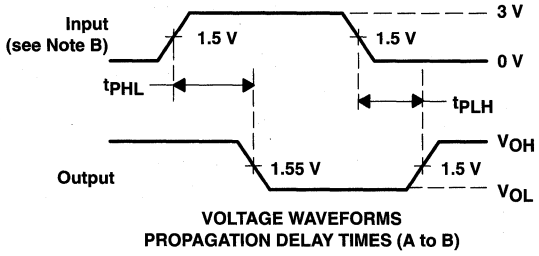


LOAD CIRCUIT FOR A OUTPUTS

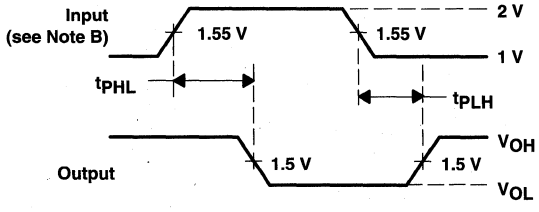


LOAD CIRCUIT FOR B OUTPUTS

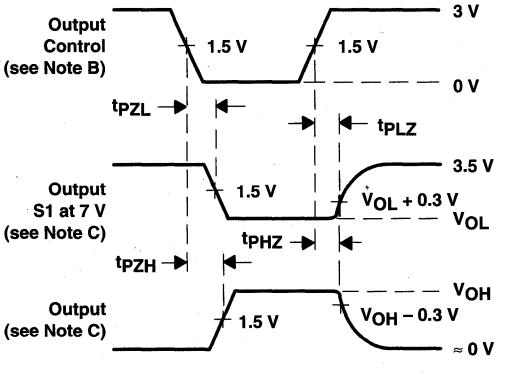
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL Inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL Inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

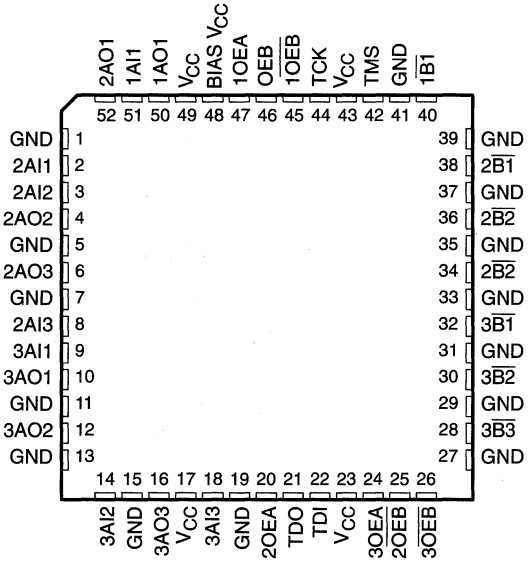
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

NOVEMBER 1991 – REVISED JULY 1993

- **Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Minimum $\overline{B}$-Port Edge Rate = 2 ns**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **Packaged in Plastic Quad-Flat Packages (PQFP) With 0.65-mm Pin Pitches**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**

RC PACKAGE
(TOP VIEW)



description

The SN74FB2041 is a 7-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. It is specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off. The enable/disable logic partitions the device as two 3-bit sections and one 1-bit section.

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the SN74FB2041. Currently TMS and TCK are not connected and TDI is shorted to TDO.

PRODUCT PREVIEW

description (continued)

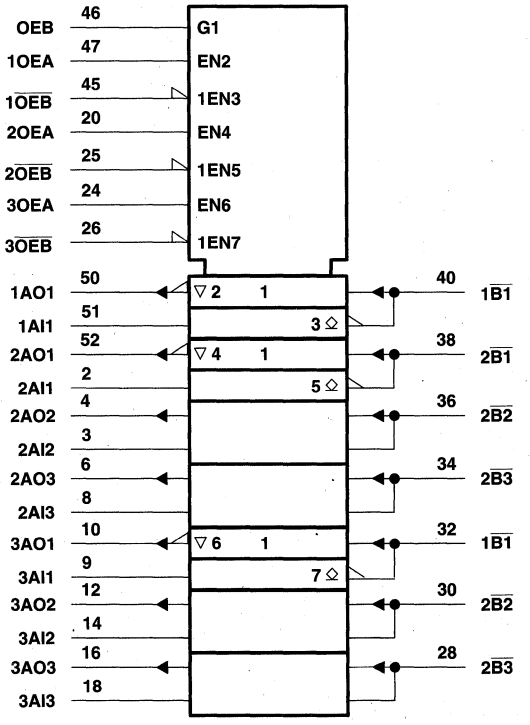
BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN74FB2041 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	$\overline{B}$ data to AO bus
X	H	H	
H	L	L	$\overline{AI}$ data to B bus
H	L	H	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus

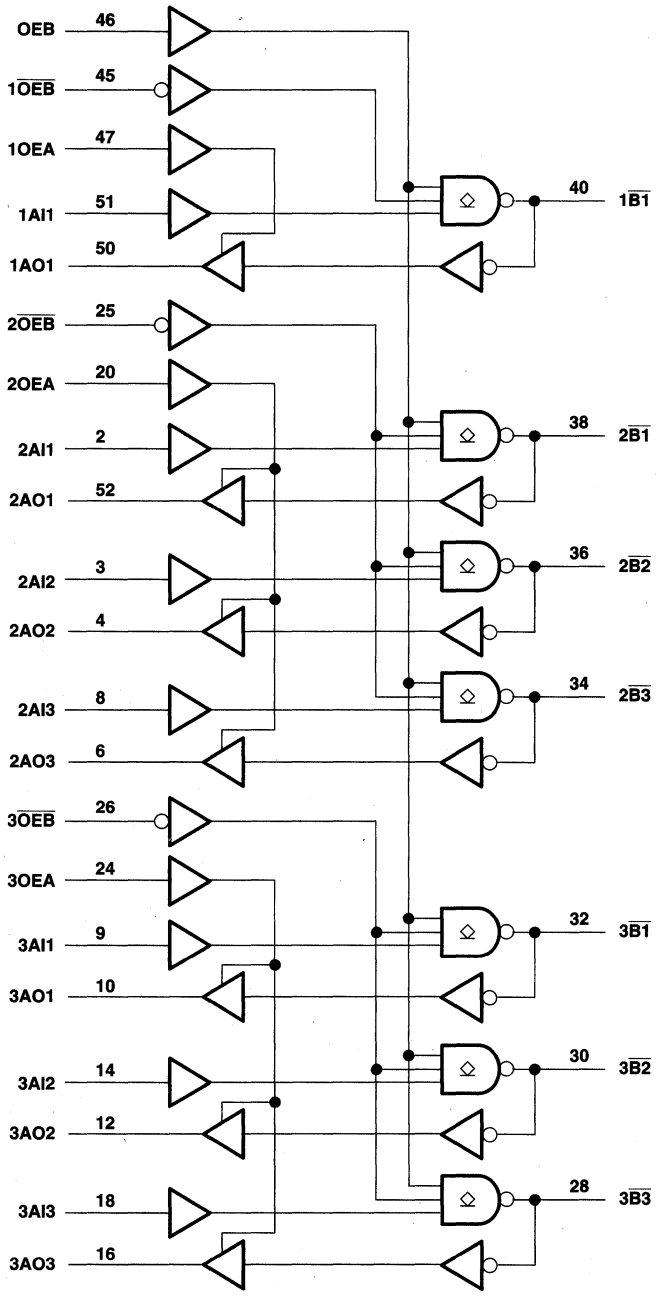
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except $\overline{B}$ port) ..... −1.2 V to 7 V
V_I ($\overline{B}$ port) ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −18 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 96 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	AO port			−3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
	Except $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = −40 mA			−0.5	V
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = −1 mA				V
			I_{OH} = −3 mA	2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V	I_{OL} = 20 mA				V
			I_{OL} = 24 mA		0.35	0.5	
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			−50	µA
	$\overline{B}$ port†	V_{CC} = 5.5 V,	V_I = 0.75 V			−100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100	µA
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			−50	µA
I_{OS}§	AO port	V_{CC} = 5.5 V,	V_O = 0	−30		−150	mA
I_{CC}	AI port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0		25		mA
	$\overline{B}$ port to AO port				65		
	Outputs disabled						
C_i	AI port and control inputs	V_I = V_{CC} or GND					pF
C_o	AO port	V_O = V_{CC} or GND					pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.5 V				6	pF
		V_{CC} = 4.5 V to 5.5 V				5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

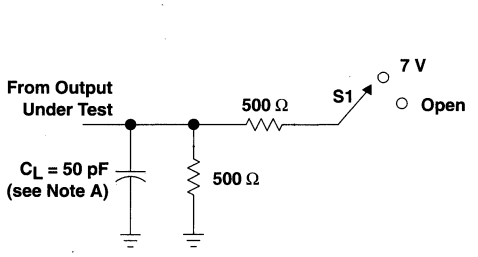
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	AI	$\overline{B}$		3.9				ns
t_{PHL}				3.6				
t_{PLH}	$\overline{B}$	AO		3.8				ns
t_{PHL}				3.8				
t_{PLH}	OEB	$\overline{B}$		4.8				ns
t_{PHL}				4.3				
t_{PLH}	OEB	$\overline{B}$		4.2				ns
t_{PHL}				3.8				
t_{PZH}	OEA	AO		3				ns
t_{PZL}				3				
t_{PHZ}	OEA	AO		3.3				ns
t_{PLZ}				2.6				
$t_{sk(p)}$	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	AI to $\overline{B}$ or $\overline{B}$ to AO					0.75	ns
$t_{sk(o)}$	Skew between drivers in the same package	AI to $\overline{B}$ or $\overline{B}$ to AO		1	1.5		2	ns
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)			2		1	3	ns
t_{PR}	$\overline{B}$-port input pulse rejection					1		ns

live insertion specifications over recommended operating free-air temperature range

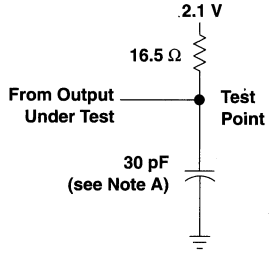
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			450	µA
		V_{CC} = 4.5 V to 5.5 V					10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		1.62		2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0 ,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1			µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V				100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V				100	

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

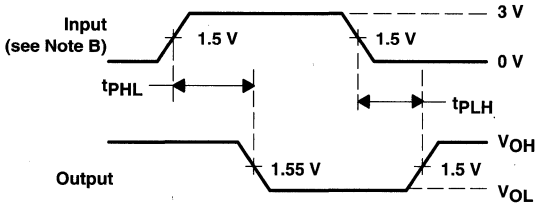


LOAD CIRCUIT FOR A OUTPUTS

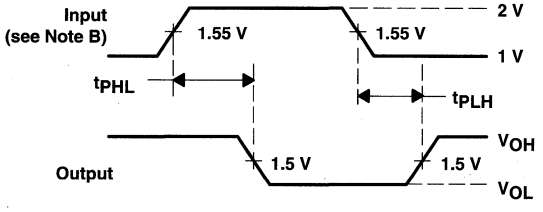


LOAD CIRCUIT FOR B OUTPUTS

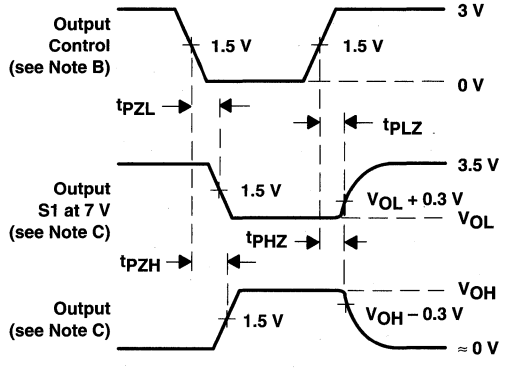
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL Inputs - PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns. BTL Inputs - PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

ABT JTAG/IEEE 1149.1

Features

- Compatibility with IEEE Standard 1149.1-1990 (JTAG) test access port (TAP) and boundary-scan architecture
- EPIC-IIB™ submicron process technology
- Sub-6-ns maximum propagation delays
- Octal and Widebus™ availability
- EIAJ TSSOP, JEDEC SSOP, and EIAJ TQFP fine-pitch surface-mount packaging
- Bus-hold circuitry ('ABT18XXXA devices only)
- 18- and 20-bit UBT™ architectures
- Additional SCOPE™ instructions available such as:
  - Parallel Signature Analysis (PSA)
  - Pseudo-Random Pattern Generation (PRPG)
- Test-mode or normal-mode operation
- Members of the Texas Instruments SCOPE™ family of testability products
- TI has established an alternate source

Benefits

- Facilitate testing of complex circuit board assemblies via a 4-wire test access port
- High-performance, low-power, high-drive, low-noise equivalents of standard ABT buffers/drivers/transceivers
- No system throughput or cycle time penalty for boundary-scan implementation
- Functional equivalents to standard ABT devices offer system and test designers flexible integration options
- Save valuable board space
- Reduce component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Advanced integration, as one UBT™ can replace nearly all common bus-interface logic
- Built-in self-test feature allows easy upgrade for advanced JTAG test applications
- IEEE Standard 1149.1-1990 protocol can be bypassed for applications not requiring boundary scan
- Compatible with complete line of system-level test products including controllers, bus monitors, scan path linkers, scan path selectors, application-specific products, and very large-scale integration products
- Standardization that comes from a common product approach

The following table lists ABT JTAG/IEEE 1149.1 devices currently being evaluated for market introduction. Customers interested in learning more about TI's plans for these devices should contact the Advanced System Logic Marketing hotline at (214) 997-5202.

DEVICE	PIN COUNT	DESCRIPTION
'ABT8240	24	Scan Test Device With Octal Driver
'ABT8244	24	Scan Test Device With Octal Buffer
'ABT8373	24	Scan Test Device With Octal Latch
'ABT8374	24	Scan Test Device With Octal Flip-Flop
'ABT18640	56	Scan Test Device With 18-Bit Inverting Bus Transceiver

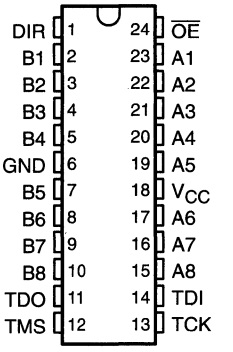
Information regarding the tap control state diagram, signal descriptions, and other related JTAG/IEEE 1149.1 information is similar for the 'ABT18245, 'ABT18502A, 'ABT18504A, 'ABT18646A, and 'ABT18652A. Therefore, this information will only be provided in the data sheet for the 'ABT18245. Please contact your local TI sales representative for further information.

DEVICE	DESCRIPTION	AVAILABILITY
'ABT8245	8-Bit Bus Transceiver	Now
'ABT8543	8-Bit Latched Transceiver	Now
'ABT8646	8-Bit Transceiver and Register	Now
'ABT8652	8-Bit Transceiver and Register	Now
'ABT8952	8-Bit Clocked Transceiver	Now
'ABT18245	18-Bit Bus Transceiver	Now
'ABT18502	18-Bit Universal Bus Transceiver	Now
'ABT18502A†	18-Bit Universal Bus Transceiver	1Q94
'ABT18504	20-Bit Universal Bus Transceiver	Now
'ABT18504A†	20-Bit Universal Bus Transceiver	1Q94
'ABT18646	18-Bit Transceiver and Register	Now
'ABT18646A†	18-Bit Transceiver and Register	1Q94
'ABT18652	18-Bit Transceiver and Register	Now
'ABT18652A†	18-Bit Transceiver and Register	1Q94

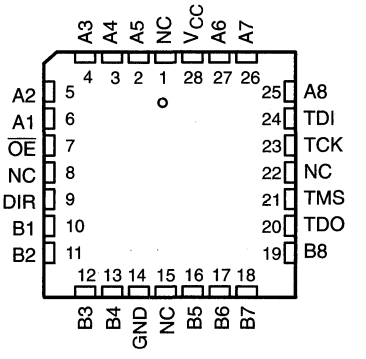
† With the exception of the 'ABT18245, the 'ABT18XXX family is being redesigned in order to enhance test mode as well as normal mode operation. As such, the 'ABT18XXXA devices are recommended for new designs and the data sheets for these devices are provided in this data book. Please note that the AC parameters shown are from the 'ABT18XXX device data sheets and serve as preliminary information design goals for the 'ABT18XXXA devices.

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to SN54/74F245 and SN54/74ABT245 in the Normal Function Mode**
- ***SCOPE*™ Instruction Set:**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs**

SN54ABT8245 . . . JT PACKAGE
SN74ABT8245 . . . DW PACKAGE
(TOP VIEW)



SN54ABT8245 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN54ABT8245 and SN74ABT8245 scan test devices with octal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F245 and SN54/74ABT245 octal bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

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description (continued)

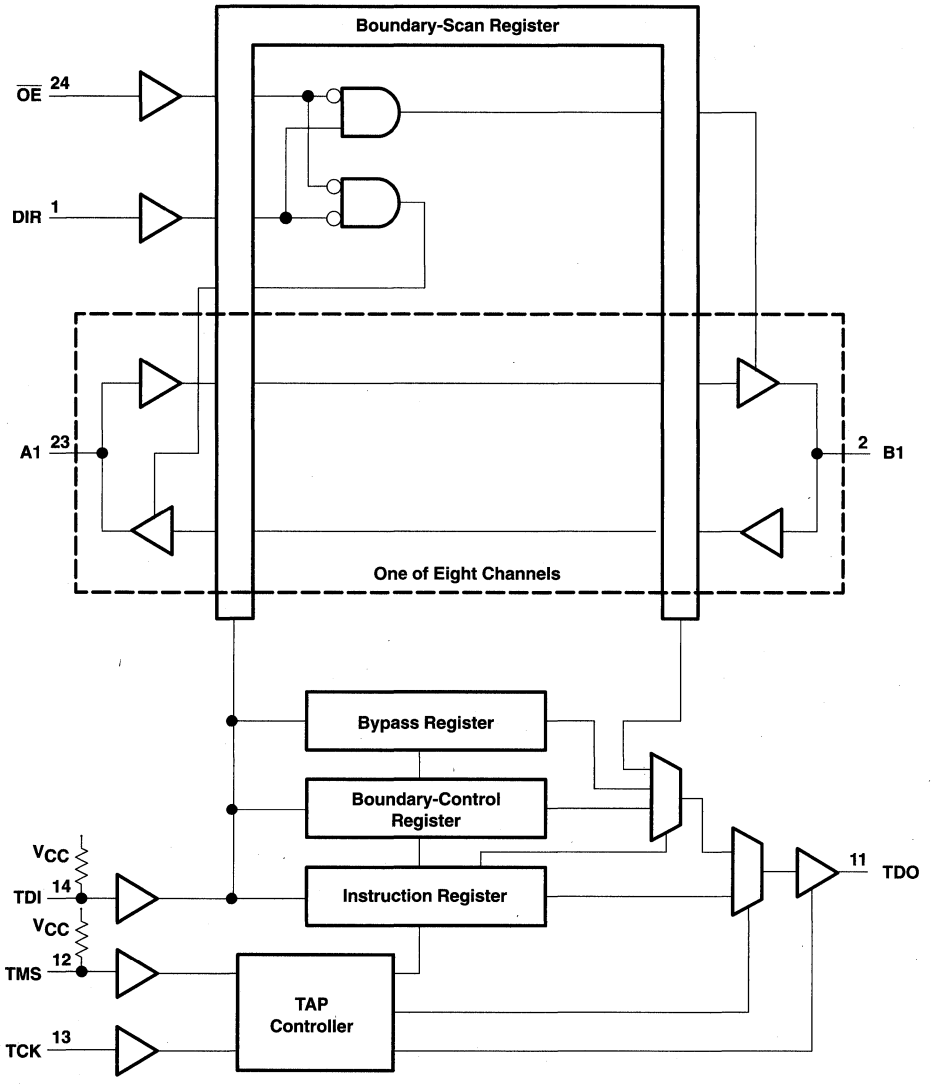
Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(normal mode)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

functional block diagram



Pin numbers shown are for the DB, DW, and JT packages.

Terminal Functions

PIN NAME	DESCRIPTION
A1 – A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1 – B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
DIR	Normal-function direction-control input. See function table for normal-mode logic.
GND	Ground
$\overline{OE}$	Normal-function output-enable input. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

test architecture

Serial test information is conveyed by means of a 4-wire test bus or test access port (TAP), that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and three test data registers: a 36-bit boundary-scan register, an 11-bit boundary-control register, and a one-bit bypass register.

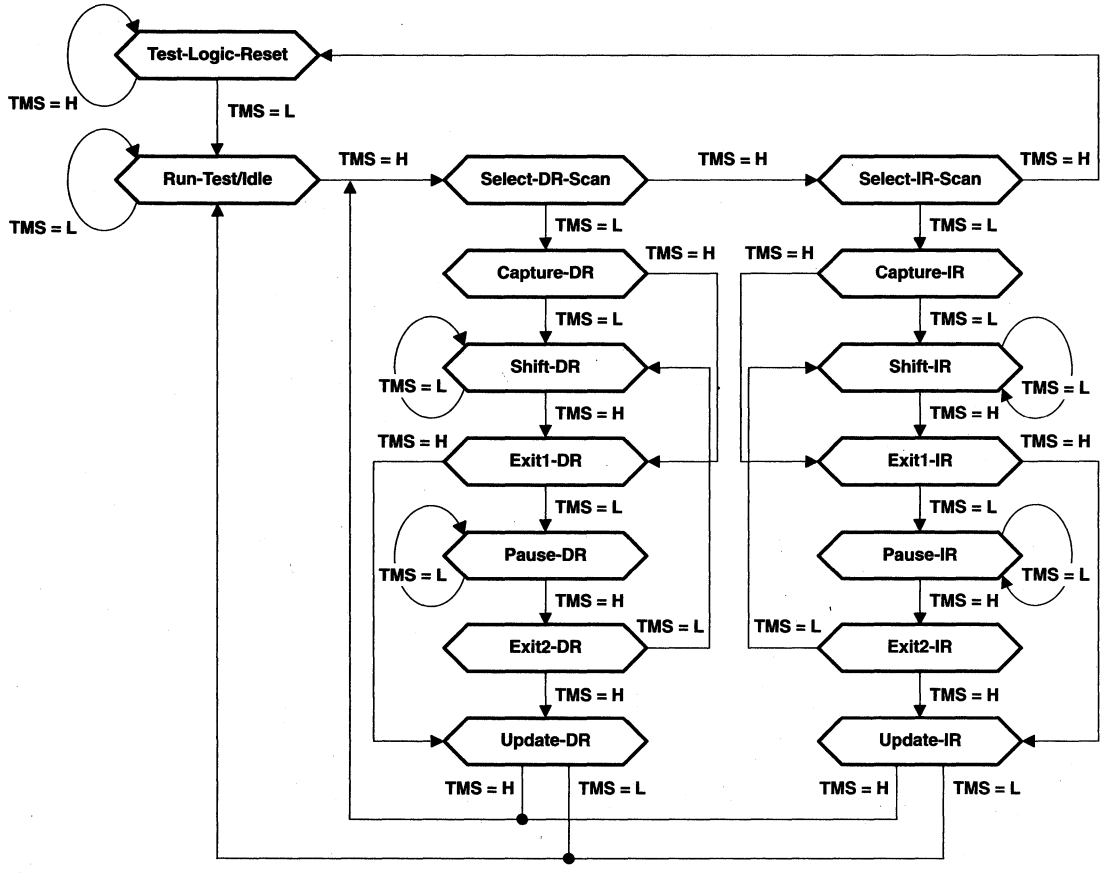


Figure 1. TAP Controller State Diagram

state diagram description

The test access port (TAP) controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated Figure 1 and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of sixteen states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller will return to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that will force it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8245, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0. The boundary-control register is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state can also be entered following data register or instruction register scans. Run-Test/Idle is provided as a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller will exit either of these states on the next TCK cycle. These states are provided to allow the selection of either data register scan or instruction register scan.

Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

state diagram description (continued)

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states used to end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state provides the capability of suspending and resuming data register scan operations without loss of data.

Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK following entry to the Update-DR state.

Capture-IR

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state.

For the 'ABT8245, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state provides the capability of suspending and resuming instruction register scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

register overview

With the exception of the bypass register, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register description

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8245. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction.

The instruction register order of scan is illustrated in Figure 2.

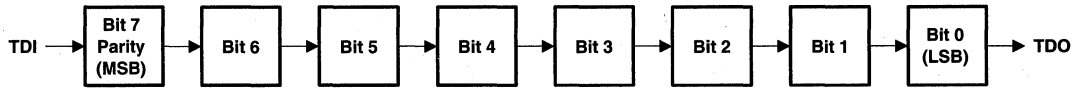


Figure 2. Instruction Register Order of Scan

data register description

boundary-scan register

The boundary-scan register (BSR) is 36 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, two BSCs for each normal-function I/O pin (one for input data and one for output data), and one BSC for each of the internally decoded output-enable signals (OEA and OEB). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0.

When external data is to be captured, the BSCs for signals OEA and $\overline{OEB}$ capture logic values determined by the following positive-logic equations: OEA = $\overline{OE}$ • $\overline{DIR}$, and OEB = $\overline{OE}$ • DIR. When data is to be applied externally, these BSCs control the drive state (active or high-impedance) of their respective outputs.

The boundary-scan register order of scan is from TDI through bits 35–0 to TDO. Table 1 shows the boundary-scan register bits and their associated device pin signals.

Table 1. Boundary-Scan Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
35	OEB	31	B8-I	23	B8-O	15	A8-I	7	A8-O
34	OEA	30	B7-I	22	B7-O	14	A7-I	6	A7-O
33	DIR	29	B6-I	21	B6-O	13	A6-I	5	A6-O
32	$\overline{OE}$	28	B5-I	20	B5-O	12	A5-I	4	A5-O
—	—	27	B4-I	19	B4-O	11	A4-I	3	A4-O
—	—	26	B3-I	18	B3-O	10	A3-I	2	A3-O
—	—	25	B2-I	17	B2-O	9	A2-I	1	A2-O
—	—	24	B1-I	16	B1-O	8	A1-I	0	A1-O

boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include pseudo-random pattern generation (PRPG), parallel signature analysis (PSA) with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The boundary-control register order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the boundary-control register bits and their associated test control signals.

data register description (continued)

Table 2. Boundary-Control Register Configuration

BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL
10	MASK8	6	MASK4	2	OPCODE2
9	MASK7	5	MASK3	1	OPCODE1
8	MASK6	4	MASK2	0	OPCODE0
7	MASK5	3	MASK1	—	—

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is illustrated in Figure 3.

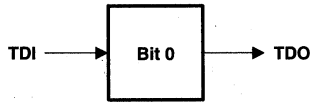


Figure 3. Bypass Register Order of Scan

Table 3. Instruction Register Opcodes

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	BYPASS‡	Bypass scan	Bypass	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	INTEST	Boundary scan	Boundary scan	Test
10000100	BYPASS‡	Bypass scan	Bypass	Normal
00000101	BYPASS‡	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS‡	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT8245.

instruction register opcode description

The instruction register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

control boundary to high impedance

This instruction conforms to the IEEE P1149.1A HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE P1149.1A CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the boundary-control register is executed during Run-Test/Idle. The five test operations decoded by the boundary-control register are: sample inputs/toggle outputs (TOPSIP), pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

boundary read

The boundary-scan register is selected in the scan path. The value in the boundary-scan register remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The boundary-scan register is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift register and shadow latch elements of the boundary-scan register. The device operates in the normal mode.

instruction register opcode description (continued)

boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

boundary-control register scan

The boundary-control register is selected in the scan path. The value in the boundary-control register remains unchanged during Capture-DR. This operation must be performed prior to a boundary run test operation in order to specify which test operation is to be executed.

Table 4. Boundary-Control Register Opcodes

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/16-bit mode (PRPG)
X10	Parallel signature analysis/16-bit mode (PSA)
011	Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT)

boundary-control register opcode description

The boundary-control register opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

It should be noted, in general, that while the control input BSCs (bits 35–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 35–34 of the BSR) do control the drive state (active or high impedance) of the selected device output pins. It also should be noted that these BCR instructions are only valid when the device is operating in one direction of data flow (that is, OEA ≠ OEB). Otherwise, the bypass instruction is operated.

PSA input masking

Bits 10–3 of the boundary-control register are used to specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in Table 3. When the mask bit which corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

boundary-control register opcode description (continued)

sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK.

pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK and then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK. This data is also updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Figures 4 and 5 illustrate the 16-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

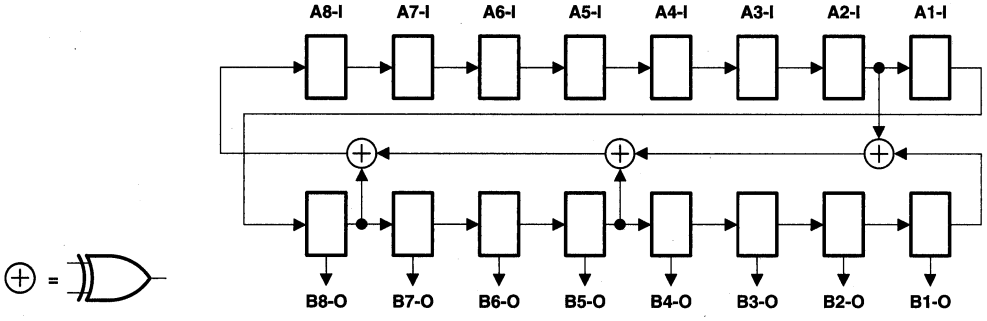


Figure 4. 16-Bit PRPG Configuration (OEA = 0, OEB = 1)

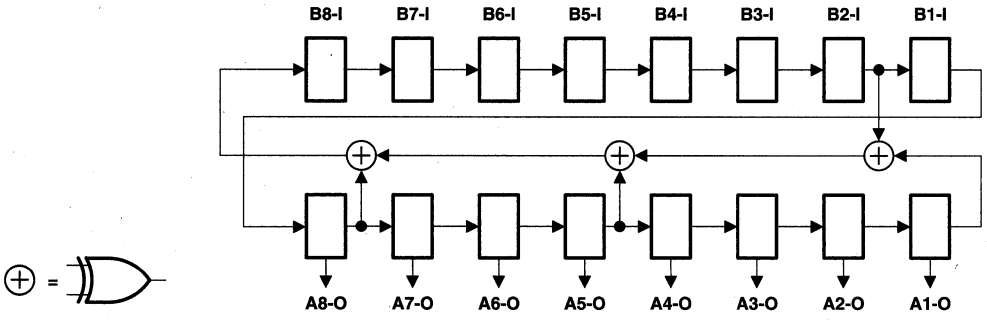


Figure 5. 16-Bit PRPG Configuration (OEA=1, OEB= 0)

boundary-control register opcode description (continued)

parallel signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 6 and 7 illustrate the 16-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

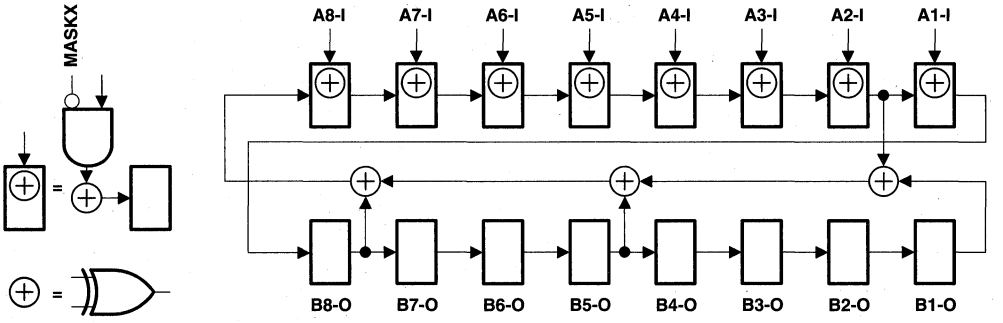


Figure 6. 16-Bit PSA Configuration (OEA = 0, OEB = 1)

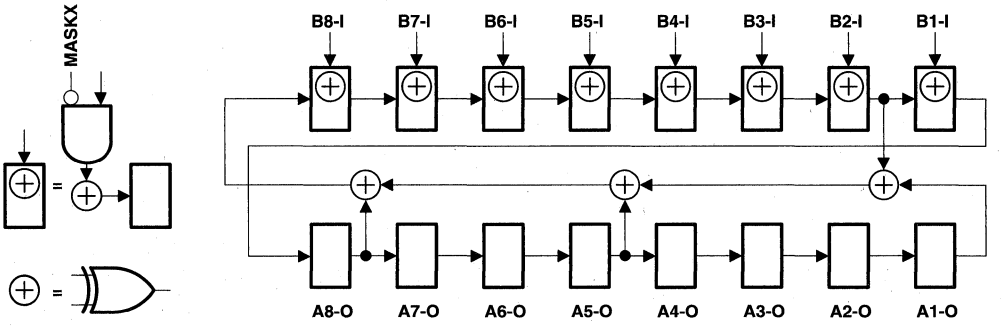


Figure 7. 16-Bit PSA Configuration (OEA = 1, OEB = 0)

boundary-control register opcode description (continued)

simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. Figures 8 and 9 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

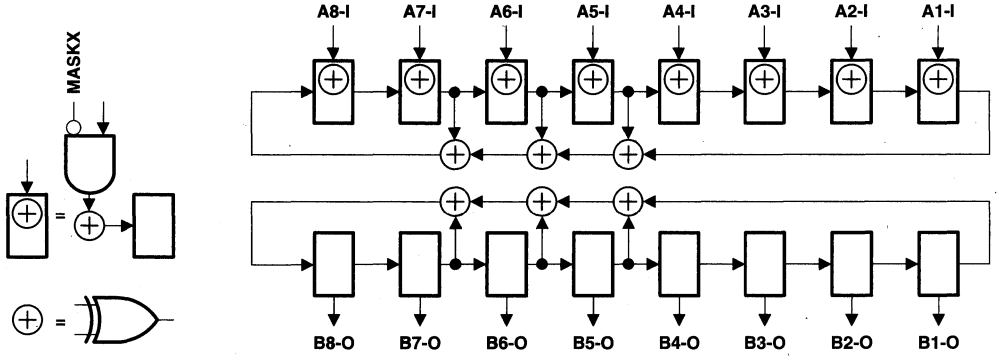


Figure 8. 8-Bit PSA/PRPG Configuration (OEA = 0, OEB = 1)

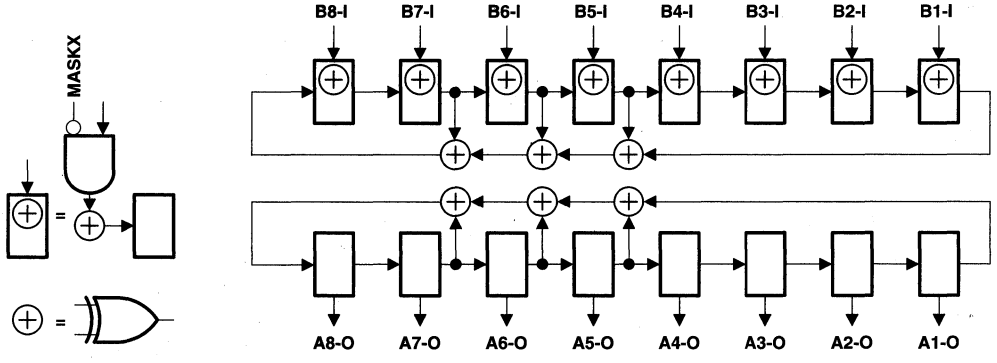


Figure 9. 8-Bit PSA/PRPG Configuration (OEA = 1, OEB = 0)

boundary-control register opcode description (continued)

simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. In addition, the shift-register elements of the opposite output BSCs are used to count carries out of the selected output BSCs and, thereby, extend the count to 16 bits. Figures 10 and 11 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

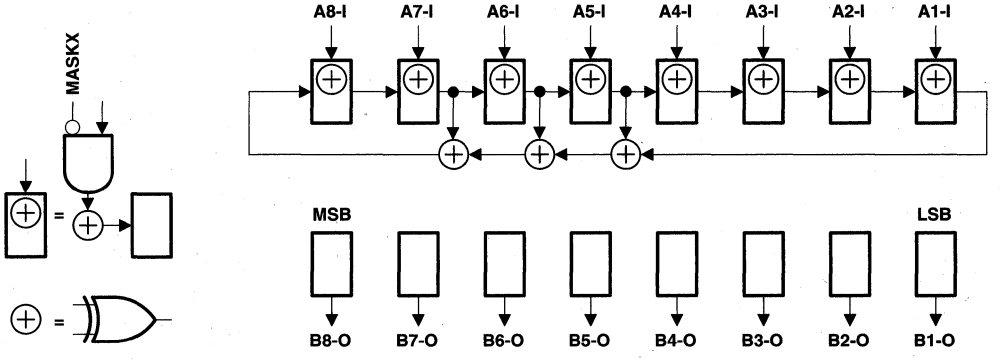


Figure 10. 8-Bit PSA/COUNT Configuration (OEA = 0, OEB = 1)

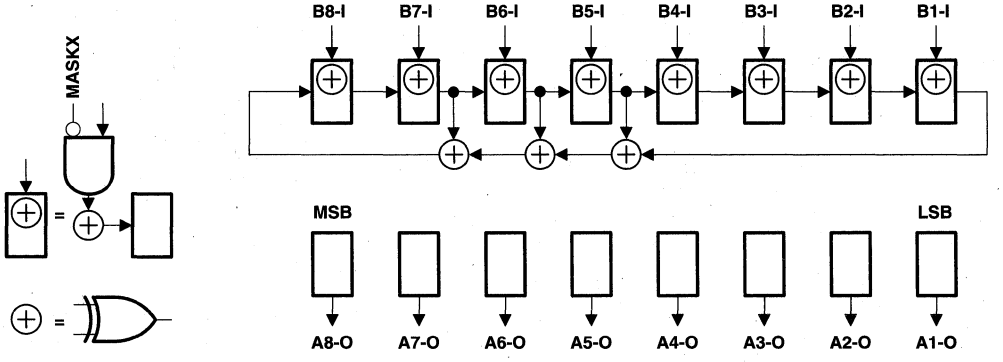


Figure 11. 8-Bit PSA/COUNT Configuration (OEA = 1, OEB = 0)

timing description

All test operations of the 'ABT8245 are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 12. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction register scan and one data register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

Table 5. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19–20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

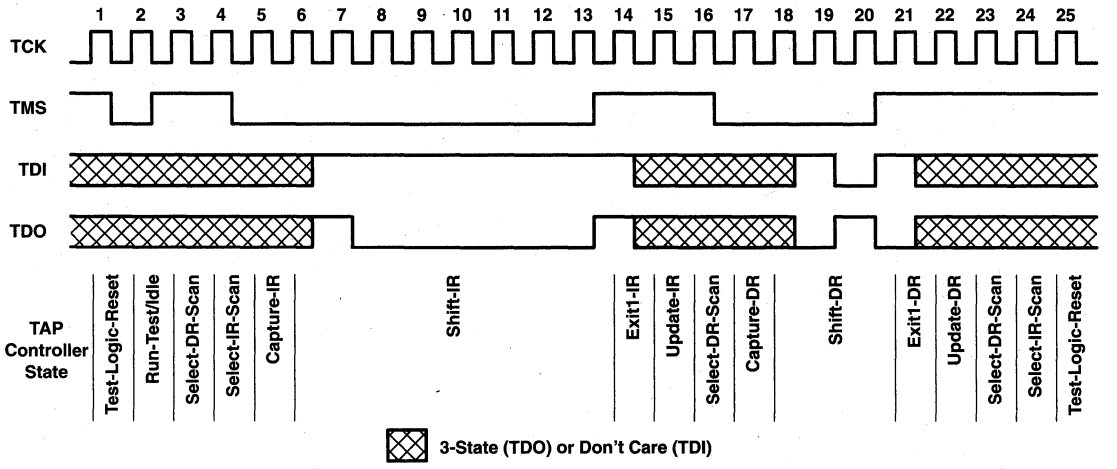


Figure 12. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8245 ..... 96 mA
SN74ABT8245 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8245		SN74ABT8245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT8245		SN74ABT8245		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		DIR, $\overline{OE}$, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC}	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	TDI, TMS			–160		–160		–160	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 5.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		0.9	2		2		2	mA
			Outputs low		30	38		38		38	
			Outputs disabled		0.9	2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

			SN54ABT8245		SN74ABT8245		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	5		5		ns
t_{su}	Setup time	A or B or DIR or $\overline{OE}$ before TCK↑	7		5		ns
		TDI before TCK↑	6		6		
		TMS before TCK↑	6		6		
t_h	Hold time	A or B or DIR or $\overline{OE}$ after TCK↑	0		0		ns
		TDI after TCK↑	0		0		
		TMS after TCK↑	0		0		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

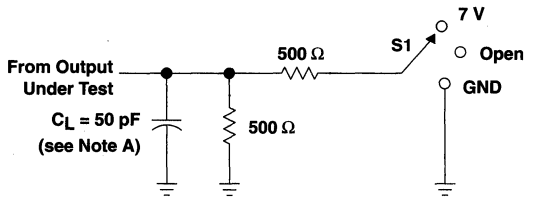
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8245		SN74ABT8245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	3.5	4.3	2	5.8	2	4.8	ns
t_{PHL}			2	3.4	4.2	2	5.5	2	5.1	
t_{PZH}	$\overline{OE}$	B or A	2.5	4.5	5.5	2.5	6.9	2.5	6.8	ns
t_{PZL}			3	5.2	6	3	8.1	3	7.5	
t_{PHZ}	$\overline{OE}$	B or A	3	6.1	7.1	3	8.9	3	8.4	ns
t_{PLZ}			3	5.5	6.6	3	8	3	7.5	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

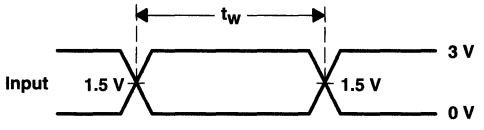
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8245		SN74ABT8245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t_{PHL}			3	7.7	9	3	12	3	11.5	
t_{PLH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PHL}			2.5	4.2	5.5	2.5	7	2.5	6.5	
t_{PZH}	TCK↓	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t_{PZL}			4.5	9	10.5	4.5	13.5	4.5	13	
t_{PZH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PZL}			2.5	4.9	6	2.5	7.8	2.5	7	
t_{PHZ}	TCK↓	A or B	3.5	8.4	10.5	3.5	14.2	3.5	13.5	ns
t_{PLZ}			3	8	10.5	3	13.5	3	13	
t_{PHZ}	TCK↓	TDO	3	5.9	7	2	9	3	8.5	ns
t_{PLZ}			3	5	6.5	3	8	3	7.5	

PARAMETER MEASUREMENT INFORMATION

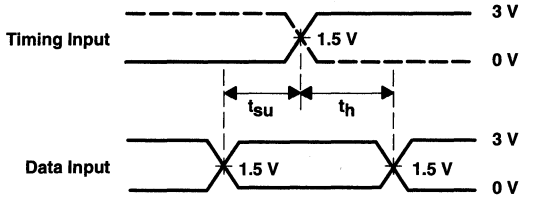


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

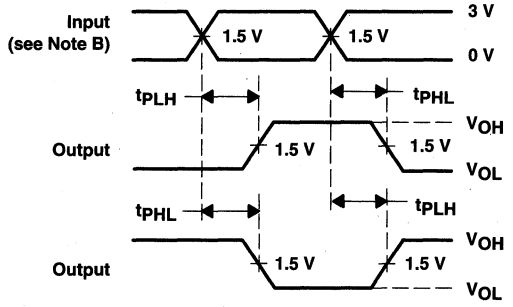
LOAD CIRCUIT FOR OUTPUTS



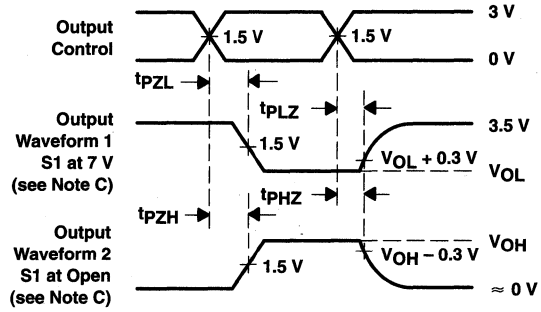
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



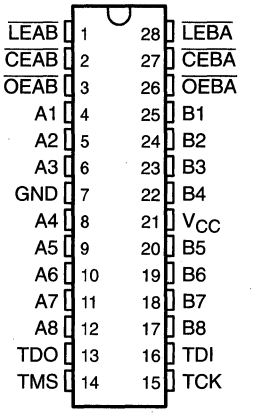
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

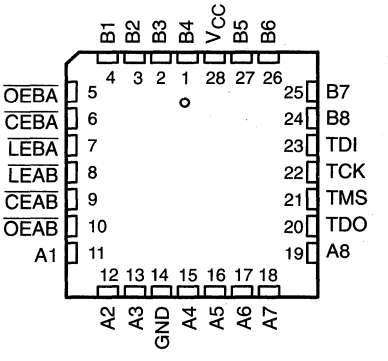
Figure 13. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to SN54/74F543 and SN54/74ABT543 in the Normal Function Mode**
- ***SCOPE*™ Instruction Set:**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs**

SN54ABT8543 . . . JT PACKAGE
SN74ABT8543 . . . DL OR DW PACKAGE
(TOP VIEW)



SN54ABT8543 . . . FK PACKAGE
(TOP VIEW)



description

The SN54ABT8543 and SN74ABT8543 scan test devices with octal registered bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F543 and SN54/74ABT543 octal registered bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal registered bus transceivers.

Data flow in each direction is controlled by latch-enable ($\overline{\text{LEAB}}$ and $\overline{\text{LEBA}}$), chip-enable ($\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$), and output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when $\overline{\text{LEAB}}$ and $\overline{\text{CEAB}}$ are both low. When either $\overline{\text{LEAB}}$ or $\overline{\text{CEAB}}$ is high, the A data is latched. The B outputs are active when $\overline{\text{OEAB}}$ and $\overline{\text{CEAB}}$ are both low. When either $\overline{\text{OEAB}}$ or $\overline{\text{CEAB}}$ is high, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B but uses $\overline{\text{LEBA}}$, $\overline{\text{CEBA}}$, and $\overline{\text{OEBA}}$.

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description (continued)

In the test mode, the normal operation of the SCOPE™ registered bus transceiver is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8543 is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74ABT8543 is characterized for operation from –40°C to 85°C.

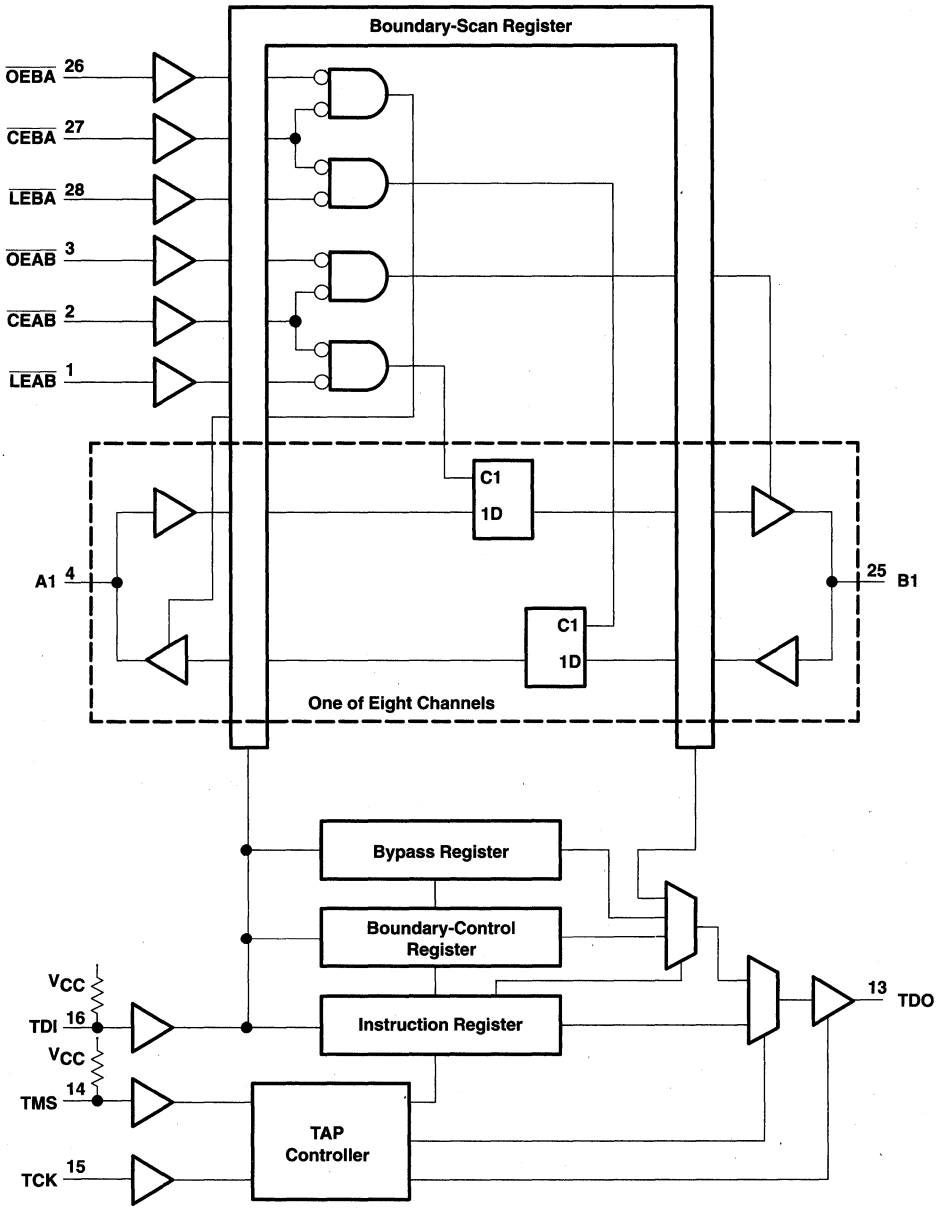
FUNCTION TABLE† (normal mode, each register)

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{OEAB}$	$\overline{LEAB}$	A	B
L	L	L	L	L
L	L	L	H	H
L	L	H	X	B_0‡
L	H	X	X	Z
H	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{CEBA}$, $\overline{OEBA}$, and $\overline{LEBA}$.

‡ Output level before the indicated steady-state input conditions were established.

functional block diagram



Pin numbers shown are for DL, DW, and JT packages.

Terminal Functions

PIN NAME	DESCRIPTION
A1 – A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1 – B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
$\overline{CEAB}$, $\overline{CEBA}$	Normal-function chip-enable inputs. See function table for normal-mode logic.
GND	Ground
$\overline{LEAB}$, $\overline{LEBA}$	Normal-function latch-enable inputs. See function table for normal-mode logic.
$\overline{OEAB}$, $\overline{OEBA}$	Normal-function output-enable inputs. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

test architecture

Serial test information is conveyed by means of a 4-wire test bus or test access port (TAP), that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and three test data registers: a 40-bit boundary-scan register, an 11-bit boundary-control register, and a one-bit bypass register.

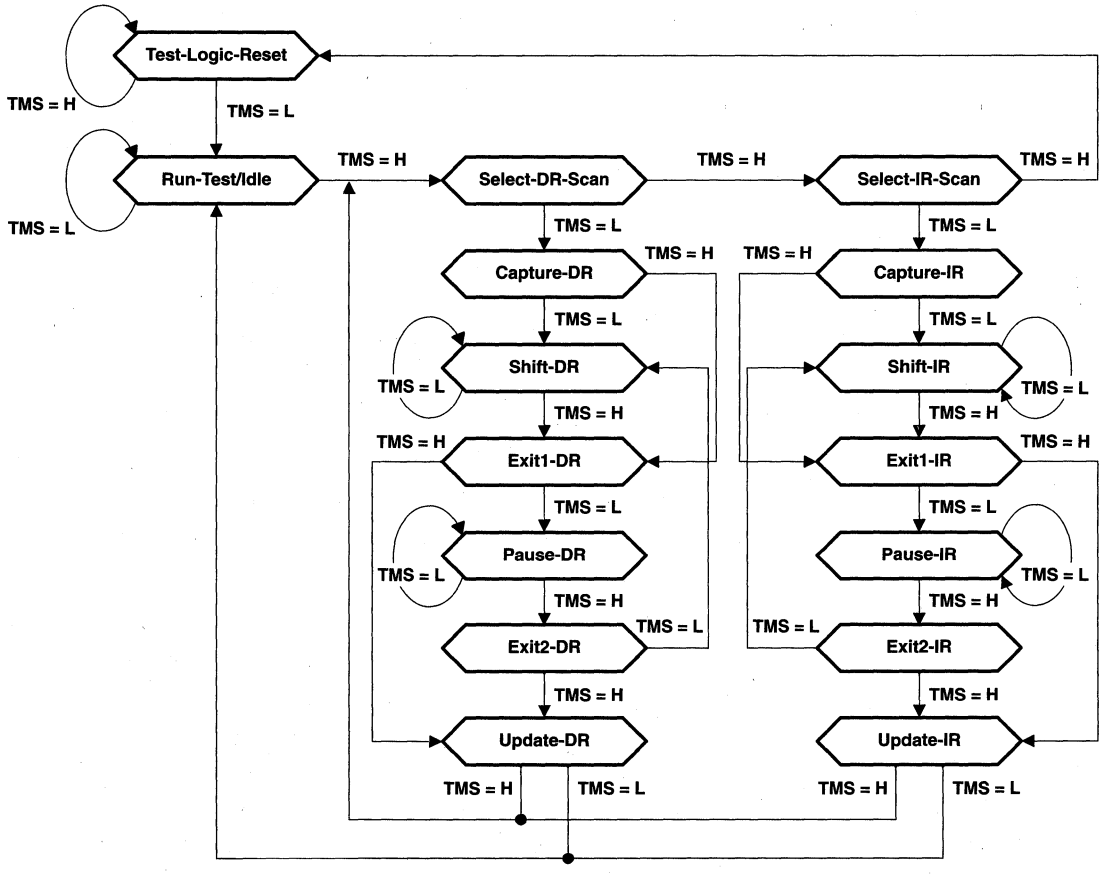


Figure 1. TAP Controller State Diagram

state diagram description

The test access port (TAP) controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated in Figure 1 and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of sixteen states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller will return to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that will force it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8543, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0. The boundary-control register is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state can also be entered following data register or instruction register scans. Run-Test/Idle is provided as a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller will exit either of these states on the next TCK cycle. These states are provided to allow the selection of either data register scan or instruction register scan.

Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

state diagram description (continued)

Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states used to end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state provides the capability of suspending and resuming data register scan operations without loss of data.

Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK following entry to the Update-DR state.

Capture-IR

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state.

For the 'ABT8543, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state provides the capability of suspending and resuming instruction register scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

register overview

the parity With the exception of the bypass register, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register description

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8543. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction.

The instruction register order of scan is illustrated in Figure 2.

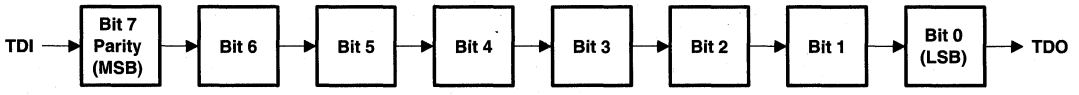


Figure 2. Instruction Register Order of Scan

data register description

boundary-scan register

The boundary-scan register (BSR) is 40 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, two BSCs for each normal-function I/O pin (one for input data and one for output data), and one BSC for each of the internally decoded output-enable signals (OEA and OEB). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0.

When external data is to be captured, the BSCs for signals OEA and OEB capture logic values determined by the following positive-logic equations: OEA = $\overline{OEBA}$ + $\overline{CEBA}$, and OEB = $\overline{OEAB}$ + $\overline{CEAB}$. When data is to be applied externally, these BSCs control the drive state (active or high-impedance) of their respective outputs.

The boundary-scan register order of scan is from TDI through bits 39–0 to TDO. Table 1 shows the boundary-scan register bits and their associated device pin signals.

Table 1. Boundary-Scan Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
39	OEB	31	A8-I	23	A8-O	15	B8-I	7	B8-O
38	OEA	30	A7-I	22	A7-O	14	B7-I	6	B7-O
37	$\overline{OEAB}$	29	A6-I	21	A6-O	13	B6-I	5	B6-O
36	$\overline{OEBA}$	28	A5-I	20	A5-O	12	B5-I	4	B5-O
35	$\overline{LEAB}$	27	A4-I	19	A4-O	11	B4-I	3	B4-O
34	$\overline{LEBA}$	26	A3-I	18	A3-O	10	B3-I	2	B3-O
33	$\overline{CEAB}$	25	A2-I	17	A2-O	9	B2-I	1	B2-O
32	$\overline{CEBA}$	24	A1-I	16	A1-O	8	B1-I	0	B1-O

boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include pseudo-random pattern generation (PRPG), parallel signature analysis (PSA) with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The boundary-control register order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the boundary-control register bits and their associated test control signals.

data register description (continued)

Table 2. Boundary-Control Register Configuration

BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL
10	MASK8	6	MASK4	2	OPCODE2
9	MASK7	5	MASK3	1	OPCODE1
8	MASK6	4	MASK2	0	OPCODE0
7	MASK5	3	MASK1	—	—

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is illustrated in Figure 3.

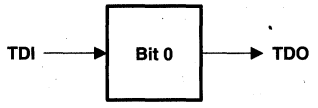


Figure 3. Bypass Register Order of Scan

Table 3. Instruction Register Opcodes

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	BYPASS‡	Bypass scan	Bypass	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	INTEST	Boundary scan	Boundary scan	Test
10000100	BYPASS‡	Bypass scan	Bypass	Normal
00000101	BYPASS‡	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS‡	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT8543.

instruction register opcode description

The instruction register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

control boundary to high impedance

This instruction conforms to the IEEE P1149.1A HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE P1149.1A CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the boundary-control register is executed during Run-Test/Idle. The five test operations decoded by the boundary-control register are: sample inputs/toggle outputs (TOPSIP), pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

boundary read

The boundary-scan register is selected in the scan path. The value in the boundary-scan register remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The boundary-scan register is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift register and shadow latch elements of the boundary-scan register. The device operates in the normal mode.

instruction register opcode description (continued)

boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

boundary-control register scan

The boundary-control register is selected in the scan path. The value in the boundary-control register remains unchanged during Capture-DR. This operation must be performed prior to a boundary run test operation in order to specify which test operation is to be executed.

Table 4. Boundary-Control Register Opcodes

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/16-bit mode (PRPG)
X10	Parallel signature analysis/16-bit mode (PSA)
011	Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT)

boundary-control register opcode description

The boundary-control register opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

It should be noted, in general, that while the control input BSCs (bits 39–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 39–38 of the BSR) do control the drive state (active or high impedance) of the selected device output pins. It also should be noted that these BCR instructions are only valid when the device is operating in one direction of data flow (that is, OEA ≠ OEB). Otherwise, the bypass instruction is operated.

PSA input masking

Bits 10–3 of the boundary-control register are used to specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in Table 3. When the mask bit which corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

boundary-control register opcode description (continued)

sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK.

pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK and then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK. This data is also updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Figures 4 and 5 illustrate the 16-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

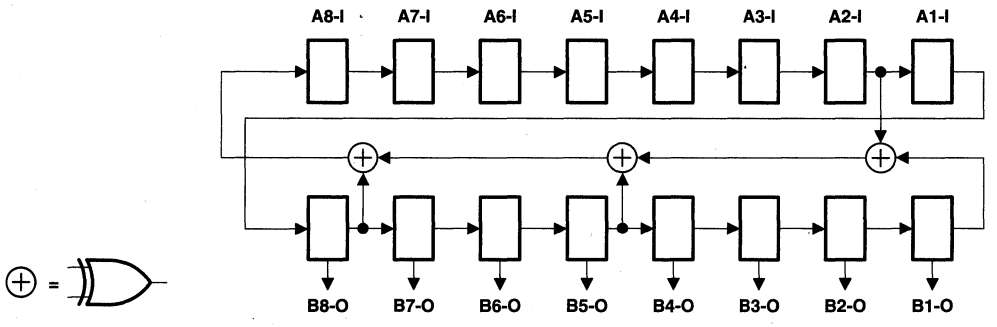


Figure 4. 16-Bit PRPG Configuration (OEA = 0, OEB = 1)

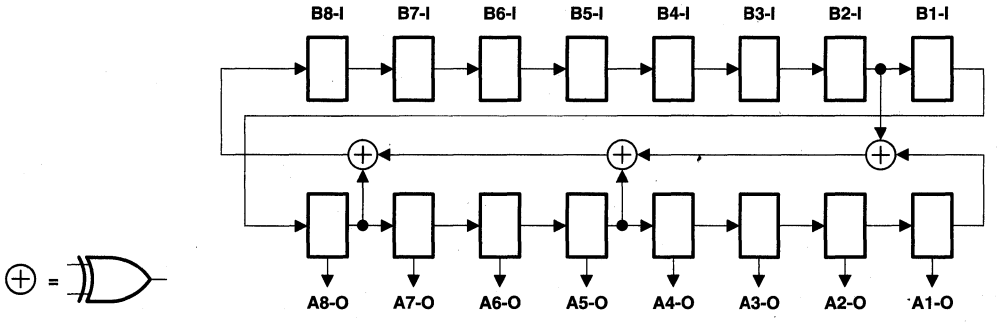


Figure 5. 16-Bit PRPG Configuration (OEA = 1, OEB = 0)

boundary-control register opcode description (continued)

parallel signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 6 and 7 illustrate the 16-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

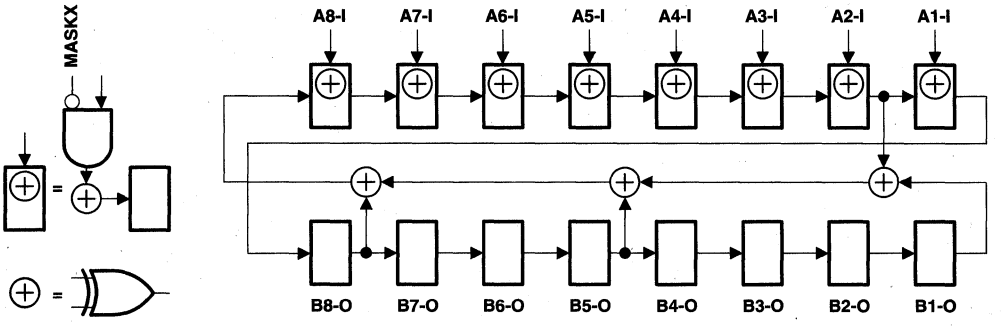


Figure 6. 16-Bit PSA Configuration (OEA = 0, OEB = 1)

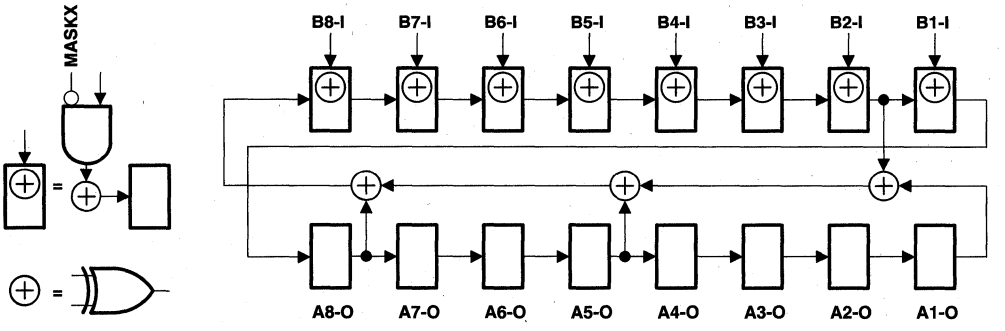


Figure 7. 16-Bit PSA Configuration (OEA = 1, OEB = 0)

boundary-control register opcode description (continued)

simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. Figures 8 and 9 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

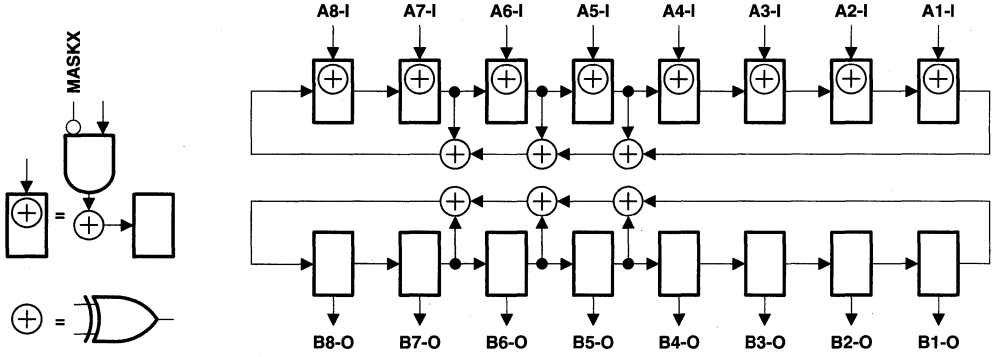


Figure 8. 8-Bit PSA/PRPG Configuration (OEA = 0, OEB = 1)

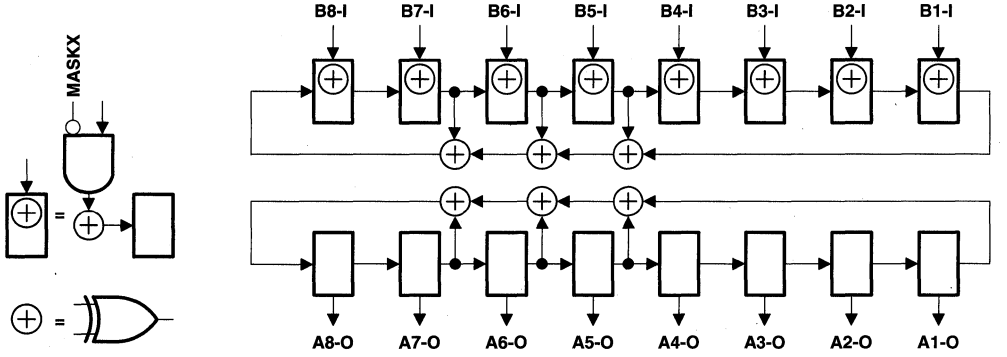


Figure 9. 8-Bit PSA/PRPG Configuration (OEA = 1, OEB = 0)

boundary-control register opcode description (continued)

simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. In addition, the shift-register elements of the opposite output BSCs are used to count carries out of the selected output BSCs and, thereby, extend the count to 16 bits. Figures 10 and 11 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

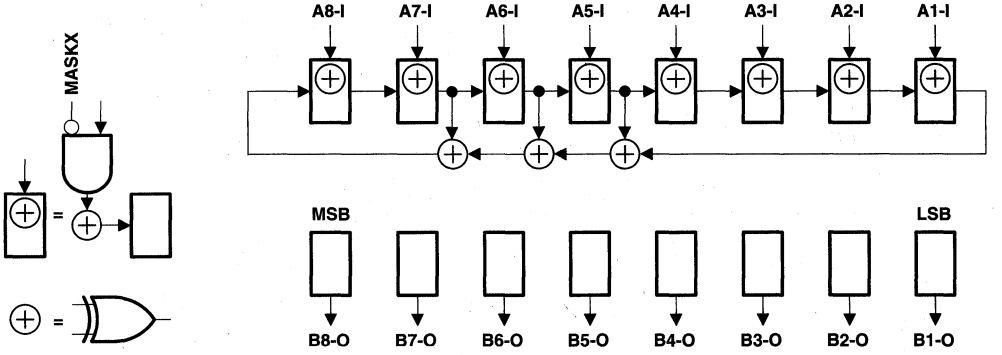


Figure 10. 8-Bit PSA/COUNT Configuration (OEA = 0, OEB = 1)

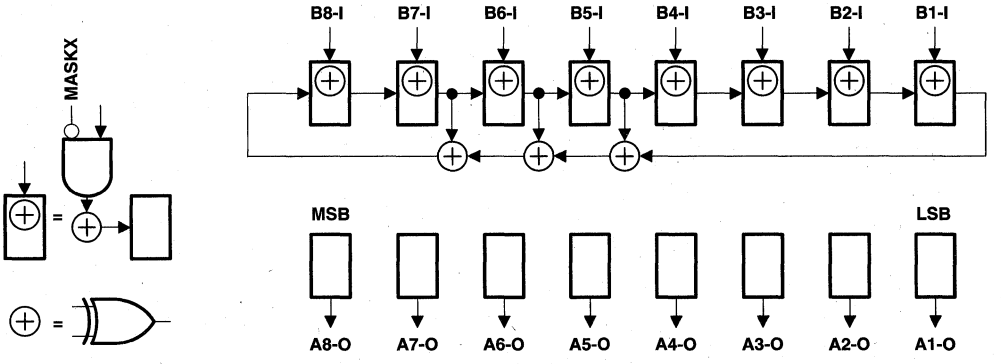


Figure 11. 8-Bit PSA/COUNT Configuration (OEA = 1, OEB = 0)

timing description

All test operations of the 'ABT8543 are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 12. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction register scan and one data register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

Table 5. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19–20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

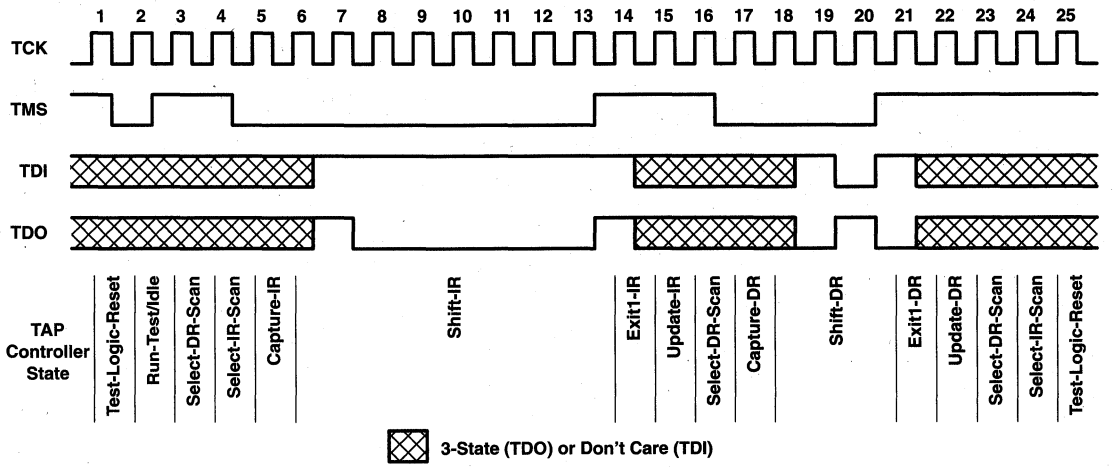


Figure 12. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) . . . . . −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8543 . . . . . 96 mA
SN74ABT8543 . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . −18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . −50 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8543		SN74ABT8543		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT8543		SN74ABT8543		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		$\overline{CE}$, $\overline{LE}$, $\overline{OE}$, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}		TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND		TDI, TMS			–160		–160		–160	µA
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 5.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		0.9	2		2		2	mA
			Outputs low		30	38		38		38	
			Outputs disabled		0.9	2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

			SN54ABT8543		SN74ABT8543		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	LEAB or LEBA high or low	3		3		ns
t_{su}	Setup time	A before $\overline{LEAB}\uparrow$ or B before $\overline{LEBA}\uparrow$	3		3		ns
t_h	Hold time	A after $\overline{LEAB}\uparrow$ or B after $\overline{LEBA}\uparrow$	0.5		0.5		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

			SN54ABT8543		SN74ABT8543		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	5		5		ns
t_{su}	Setup time	A or B or $\overline{CE}$ or $\overline{LE}$ or $\overline{OE}$ before TCK$\uparrow$	5		5		ns
		TDI before TCK$\uparrow$	6		6		
		TMS before TCK$\uparrow$	6		6		
t_h	Hold time	A or B or $\overline{CE}$ or $\overline{LE}$ or $\overline{OE}$ after TCK$\uparrow$	0		0		ns
		TDI after TCK$\uparrow$	0		0		
		TMS after TCK$\uparrow$	0		0		
t_d	Delay time	Power up to TCK$\uparrow$	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

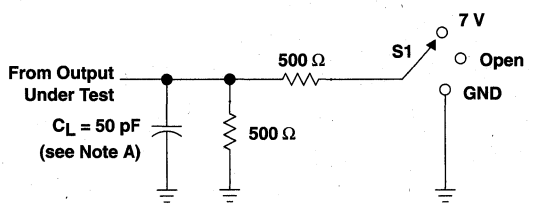
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8543		SN74ABT8543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	3.7	4.5	2	5.5	2	5.2	ns
t_{PHL}			1.5	3.5	4.4	1.5	5.8	1.5	5.5	
t_{PLH}	$\overline{LEAB}$ or $\overline{LEBA}$	B or A	2	4.7	5.6	2	8.1	2	7.8	ns
t_{PHL}			1.5	4.1	5	1.5	7.3	1.5	6.9	
t_{PZH}	$\overline{CEAB}$ or $\overline{CEBA}$	B or A	2	4.2	5.2	2	7.5	2	7.2	ns
t_{PZL}			2	4.7	5.7	2	8.4	2	8.3	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.4	5.4	2	6.7	2	6.5	ns
t_{PZL}			2	5.2	6.2	2	7.6	2	7.5	
t_{PHZ}	$\overline{CEAB}$ or $\overline{CEBA}$	B or A	2.5	5.8	6.8	2.5	9.1	2.5	8.8	ns
t_{PLZ}			2.5	5.3	6.3	2.5	8.7	2.5	8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	5.9	6.9	2	8.3	2	7.9	ns
t_{PLZ}			2	5.2	6.2	2	7.8	2	7.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

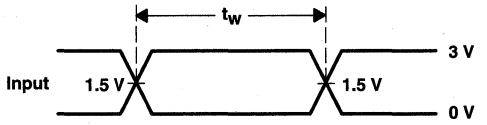
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8543		SN74ABT8543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t_{PHL}			3	7.7	9	3	12	3	11.5	
t_{PLH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PHL}			2.5	4.2	5.5	2.5	7	2.5	6.5	
t_{PZH}	TCK↓	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t_{PZL}			4.5	9	10.5	4.5	13.5	4.5	13	
t_{PZH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PZL}			2.5	4.9	6	2.5	7.5	2.5	7	
t_{PHZ}	TCK↓	A or B	3.5	8.4	10.5	3.5	14	3.5	13.5	ns
t_{PLZ}			3	8	10.5	3	13.5	3	13	
t_{PHZ}	TCK↓	TDO	3	5.9	7	3	9	3	8.5	ns
t_{PLZ}			3	5	6.5	3	8	3	7.5	

PARAMETER MEASUREMENT INFORMATION

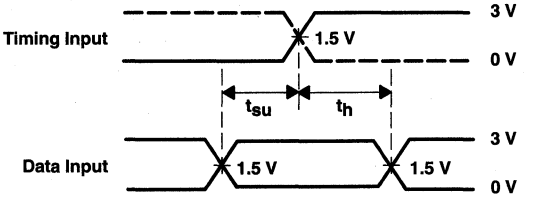


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

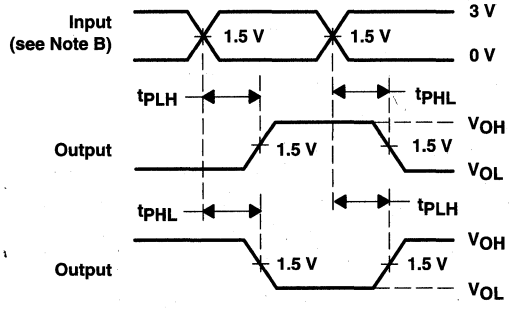
LOAD CIRCUIT FOR OUTPUTS



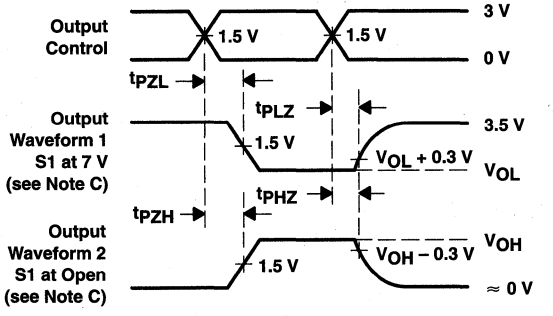
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



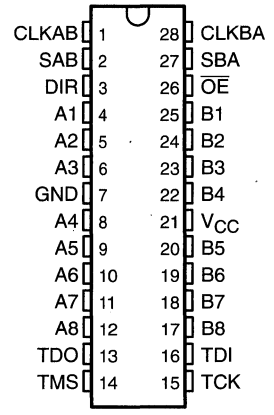
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

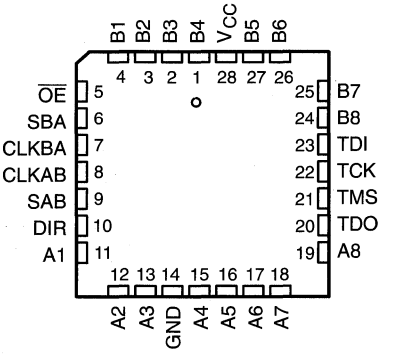
Figure 13. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to SN54/74F646 and SN54/74ABT646 in the Normal Function Mode**
- ***SCOPE*™ Instruction Set:**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs**

SN54ABT8646 . . . JT PACKAGE
SN74ABT8646 . . . DL OR DW PACKAGE
(TOP VIEW)



SN54ABT8646 . . . FK PACKAGE
(TOP VIEW)



description

The SN54ABT8646 and SN74ABT8646 scan test devices with octal bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F646 and SN54/74ABT646 octal bus transceivers and registers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers and registers.

Transceiver function is controlled by output-enable ($\overline{OE}$) and direction (DIR) inputs. When $\overline{OE}$ is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When $\overline{OE}$ is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

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description (continued)

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT8646.

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

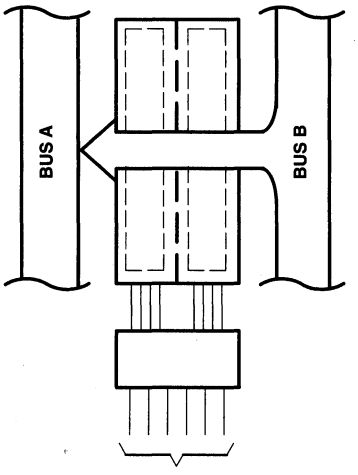
Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8646 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

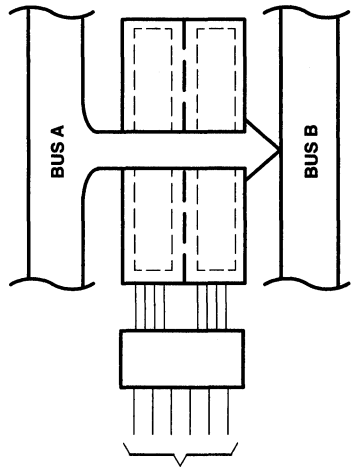
INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input disabled	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input disabled	Output	Stored A data to B bus

† The data output functions can be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



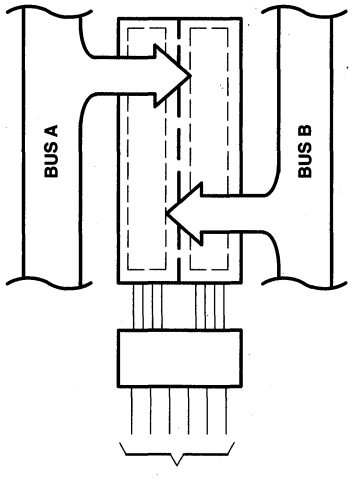
26 $\overline{OE}$	3 DIR	1 CLKAB	28 CLKBA	2 SAB	27 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



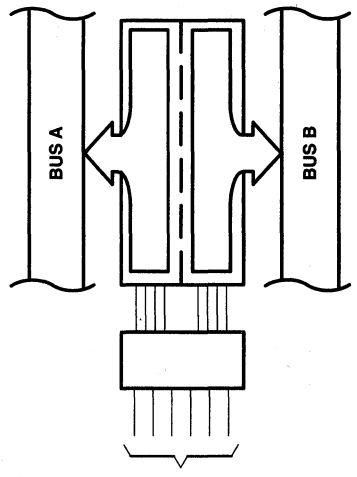
26 $\overline{OE}$	3 DIR	1 CLKAB	28 CLKBA	2 SAB	27 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



26 $\overline{OE}$	3 DIR	1 CLKAB	28 CLKBA	2 SAB	27 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



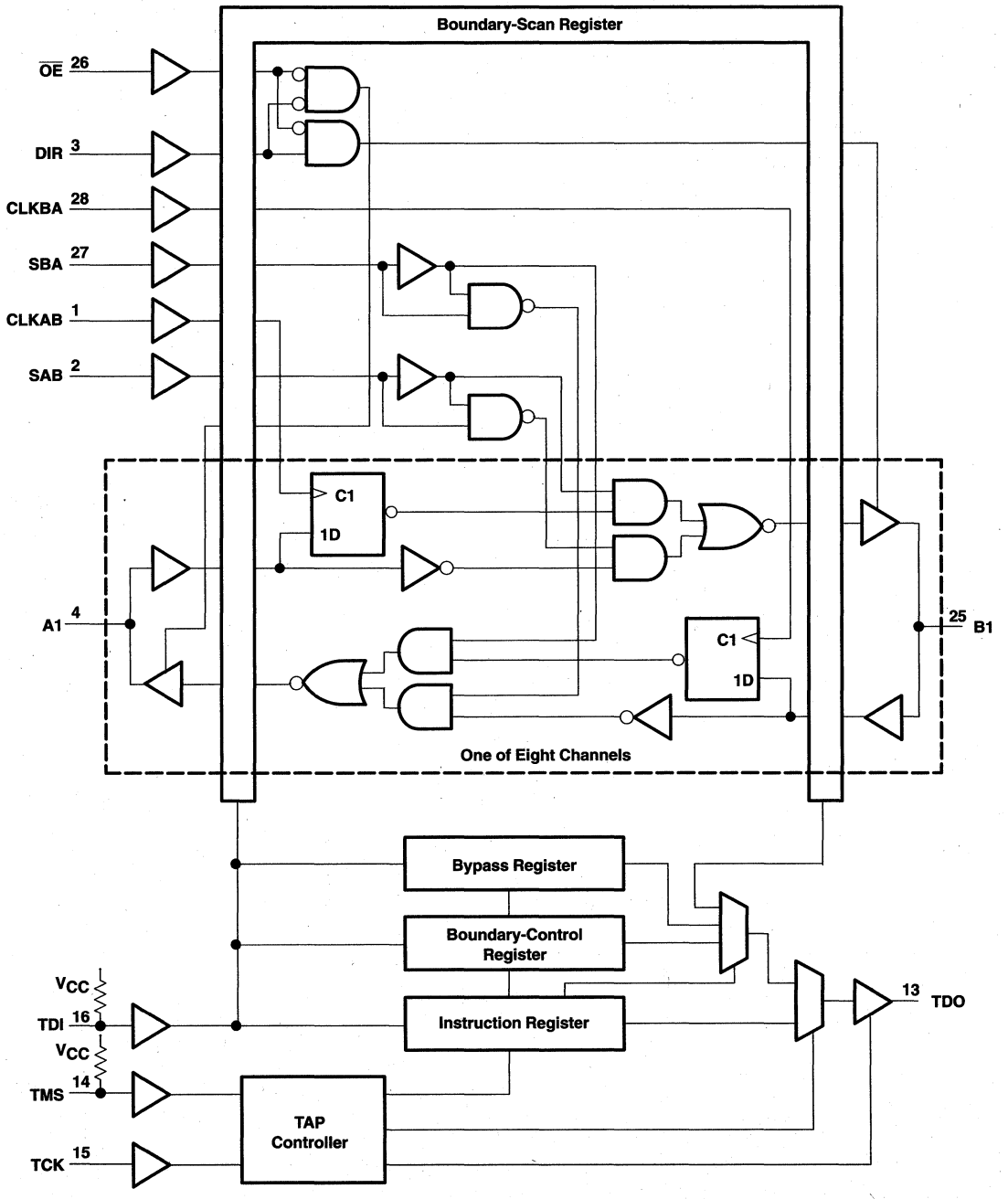
26 $\overline{OE}$	3 DIR	1 CLKAB	28 CLKBA	2 SAB	27 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

Pin numbers shown are for DL, DW, and JT packages.

functional block diagram



Pin numbers shown are for the DL, DW, and JT packages.

Terminal Functions

PIN NAME	DESCRIPTION
A1–A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1–B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
DIR	Normal-function direction-control input. See function table for normal-mode logic.
GND	Ground
$\overline{OE}$	Normal-function output-enable input. See function table for normal-mode logic.
SAB, SBA	Normal-function select inputs. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

test architecture

Serial test information is conveyed by means of a 4-wire test bus or test access port (TAP), that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. Figure 2 shows the TAP controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and three test data registers: a 40-bit boundary-scan register, an 11-bit boundary-control register, and a one-bit bypass register.

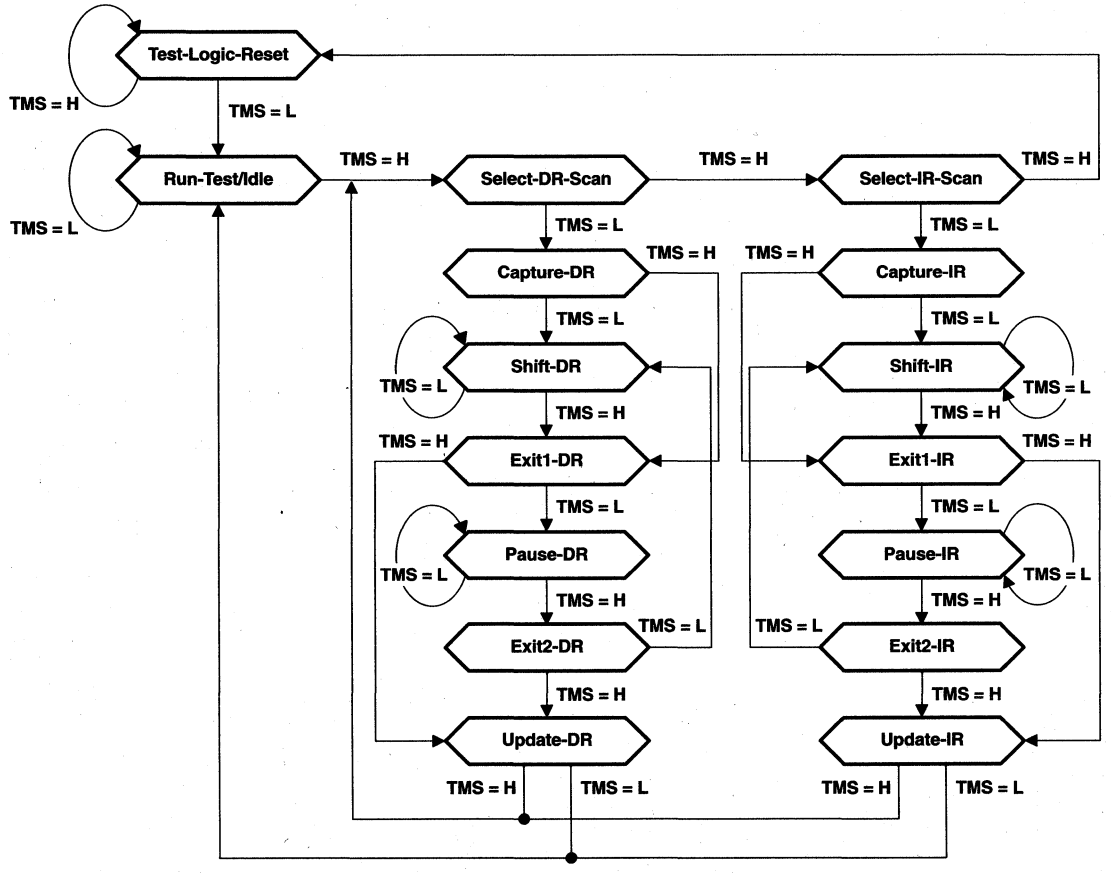


Figure 2. TAP Controller State Diagram

state diagram description

The test access port (TAP) controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated in Figure 2 and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of sixteen states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller will return to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that will force it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8646, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0. The boundary-control register is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state can also be entered following data register or instruction register scans. Run-Test/Idle is provided as a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller will exit either of these states on the next TCK cycle. These states are provided to allow the selection of either data register scan or instruction register scan.

Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

state diagram description (continued)

Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states used to end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state provides the capability of suspending and resuming data register scan operations without loss of data.

Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK following entry to the Update-DR state.

Capture-IR

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state.

For the 'ABT8646, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state provides the capability of suspending and resuming instruction register scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

register overview

With the exception of the bypass register, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register description

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8646. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction.

The instruction register order of scan is illustrated in Figure 3.

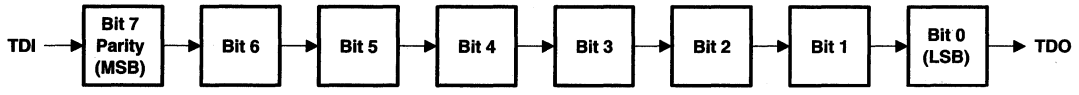


Figure 3. Instruction Register Order of Scan

data register description

boundary-scan register

The boundary-scan register (BSR) is 40 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, two BSCs for each normal-function I/O pin (one for input data and one for output data), and one BSC for each of the internally decoded output-enable signals (OEA and OEB). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0.

When external data is to be captured, the BSCs for signals OEA and $\overline{OEB}$ capture logic values determined by the following positive-logic equations: OEA = $\overline{OE} \bullet \overline{DIR}$, and OEB = $\overline{OE} \bullet$ DIR. When data is to be applied externally, these BSCs control the drive state (active or high-impedance) of their respective outputs.

The boundary-scan register order of scan is from TDI through bits 39–0 to TDO. Table 1 shows the boundary-scan register bits and their associated device pin signals.

Table 1. Boundary-Scan Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
39	OEB	31	A8-I	23	A8-O	15	B8-I	7	B8-O
38	OEA	30	A7-I	22	A7-O	14	B7-I	6	B7-O
37	DIR	29	A6-I	21	A6-O	13	B6-I	5	B6-O
36	$\overline{OE}$	28	A5-I	20	A5-O	12	B5-I	4	B5-O
35	CLKAB	27	A4-I	19	A4-O	11	B4-I	3	B4-O
34	CLKBA	26	A3-I	18	A3-O	10	B3-I	2	B3-O
33	SAB	25	A2-I	17	A2-O	9	B2-I	1	B2-O
32	SBA	24	A1-I	16	A1-O	8	B1-I	0	B1-O

boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include pseudo-random pattern generation (PRPG), parallel signature analysis (PSA) with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The boundary-control register order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the boundary-control register bits and their associated test control signals.

data register description (continued)

Table 2. Boundary-Control Register Configuration

BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL
10	MASK8	6	MASK4	2	OPCODE2
9	MASK7	5	MASK3	1	OPCODE1
8	MASK6	4	MASK2	0	OPCODE0
7	MASK5	3	MASK1	—	—

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is illustrated in Figure 4.

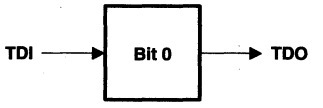


Figure 4. Bypass Register Order of Scan

Table 3. Instruction Register Opcodes

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	BYPASS‡	Bypass scan	Bypass	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	INTEST	Boundary scan	Boundary scan	Test
10000100	BYPASS‡	Bypass scan	Bypass	Normal
00000101	BYPASS‡	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS‡	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT8646.

instruction register opcode description

The instruction register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

control boundary to high impedance

This instruction conforms to the IEEE P1149.1A HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE P1149.1A CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the boundary-control register is executed during Run-Test/Idle. The five test operations decoded by the boundary-control register are: sample inputs/toggle outputs (TOPSIP), pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

boundary read

The boundary-scan register is selected in the scan path. The value in the boundary-scan register remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The boundary-scan register is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift register and shadow latch elements of the boundary-scan register. The device operates in the normal mode.

instruction register opcode description (continued)

boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

boundary-control register scan

The boundary-control register is selected in the scan path. The value in the boundary-control register remains unchanged during Capture-DR. This operation must be performed prior to a boundary run test operation in order to specify which test operation is to be executed.

Table 4. Boundary-Control Register Opcodes

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/16-bit mode (PRPG)
X10	Parallel signature analysis/16-bit mode (PSA)
011	Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT)

boundary-control register opcode description

The boundary-control register opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

It should be noted, in general, that while the control input BSCs (bits 39–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 39–38 of the BSR) do control the drive state (active or high impedance) of the selected device output pins. It also should be noted that these BCR instructions are only valid when the device is operating in one direction of data flow (that is, OEA ≠ OEB). Otherwise, the bypass instruction is operated.

PSA input masking

Bits 10–3 of the boundary-control register are used to specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in Table 3. When the mask bit which corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

boundary-control register opcode description (continued)

sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK.

pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK and then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK. This data is also updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Figures 5 and 6 illustrate the 16-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

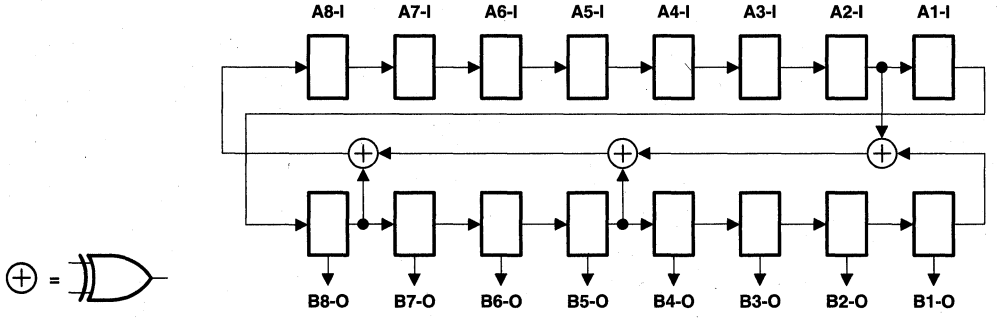


Figure 5. 16-Bit PRPG Configuration (OEA = 0, OEB = 1)

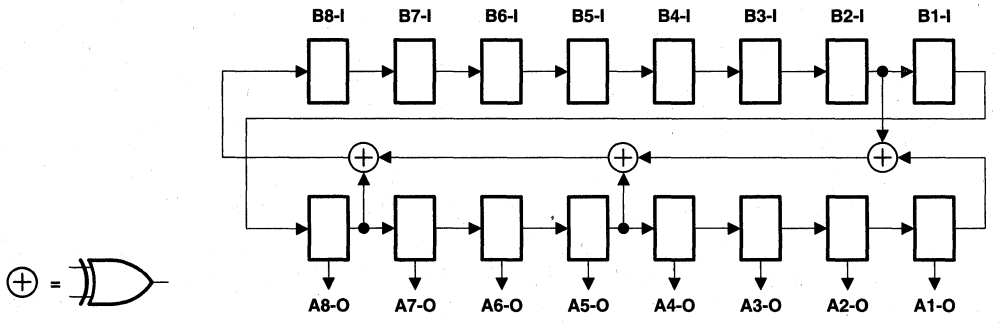


Figure 6. 16-Bit PRPG Configuration (OEA=1, OEB= 0)

boundary-control register opcode description (continued)

parallel signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 7 and 8 illustrate the 16-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

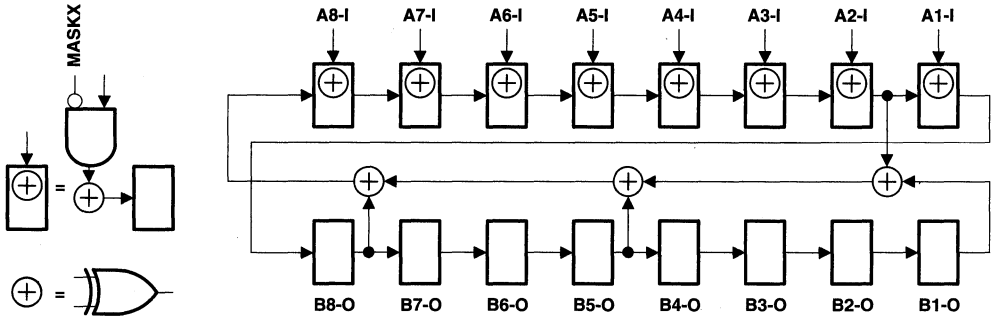


Figure 7. 16-Bit PSA Configuration (OEA = 0, OEB = 1)

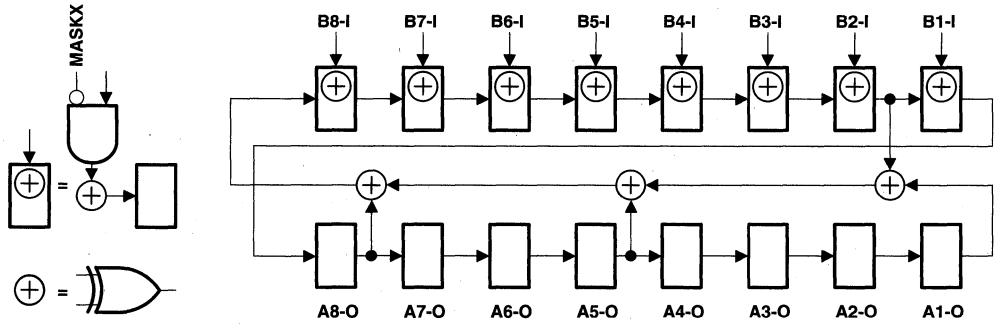


Figure 8. 16-Bit PSA Configuration (OEA = 1, OEB = 0)

boundary-control register opcode description (continued)

simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. Figures 9 and 10 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

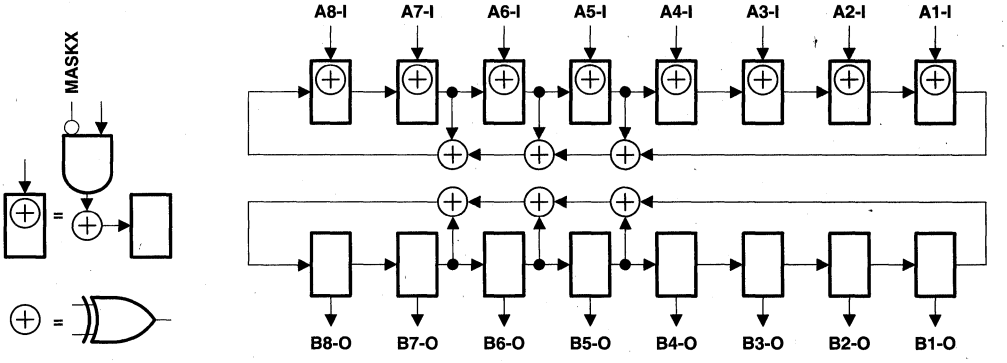


Figure 9. 8-Bit PSA/PRPG Configuration (OEA = 0, OEB = 1)

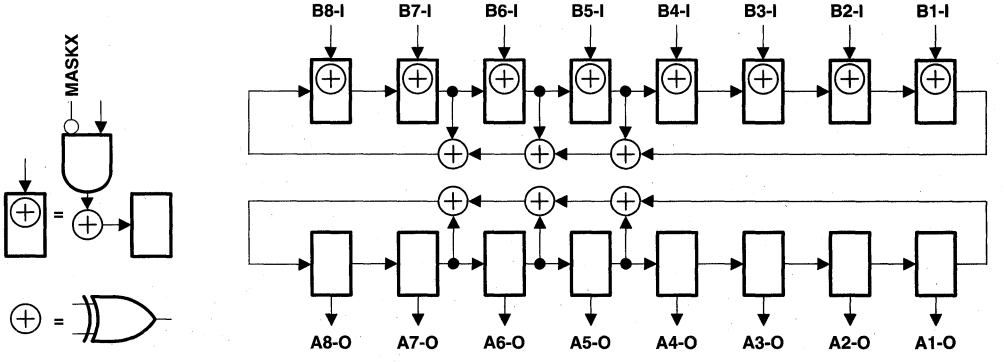


Figure 10. 8-Bit PSA/PRPG Configuration (OEA = 1, OEB = 0)

boundary-control register opcode description (continued)

simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. In addition, the shift-register elements of the opposite output BSCs are used to count carries out of the selected output BSCs and, thereby, extend the count to 16 bits. Figures 11 and 12 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

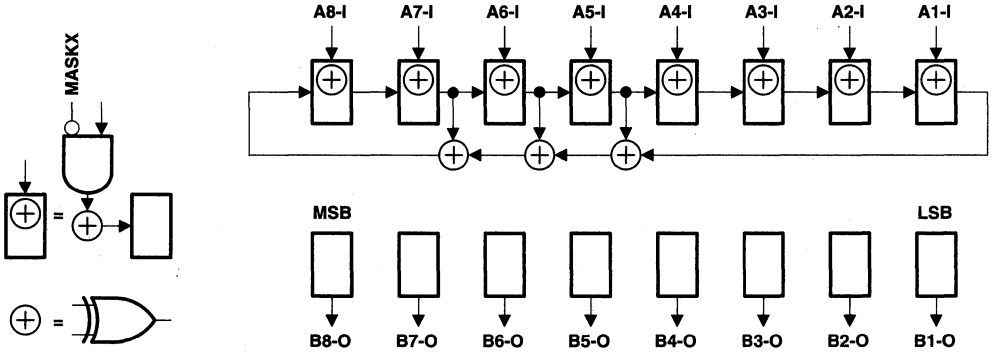


Figure 11. 8-Bit PSA/COUNT Configuration (OEA = 0, OEB = 1)

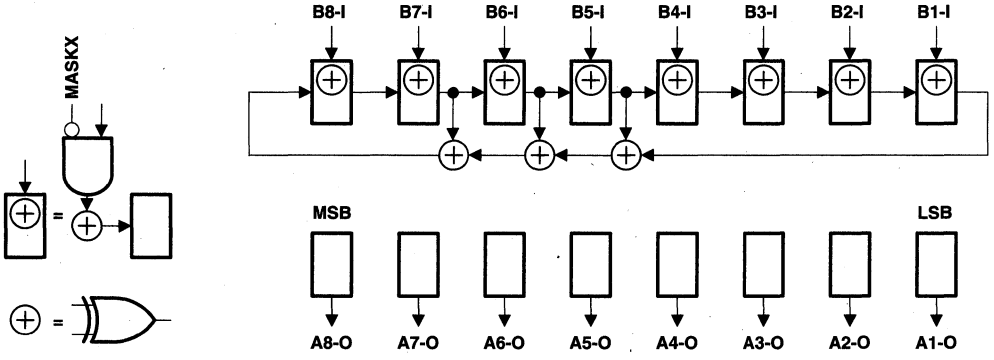


Figure 12. 8-Bit PSA/COUNT Configuration (OEA = 1, OEB = 0)

timing description

All test operations of the 'ABT8646 are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in Figure 2) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction register scan and one data register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

Table 5. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19–20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

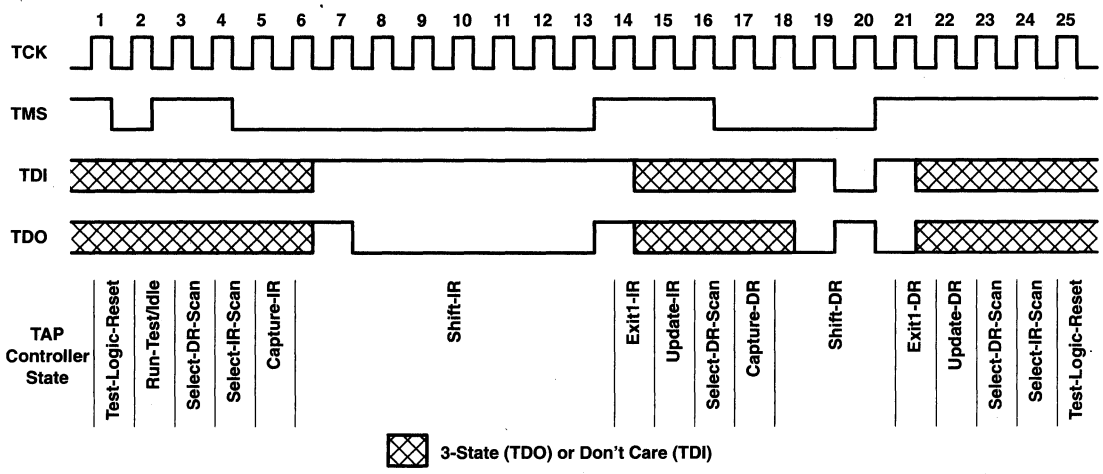


Figure 13. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8646 ..... 96 mA
SN74ABT8646 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8646		SN74ABT8646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT8646		SN74ABT8646		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, DIR, $\overline{OE}$, S, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC}	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	TDI, TMS			–160		–160		–160	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 5.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		0.9	2		2		2	mA
			Outputs low		30	38		38		38	
			Outputs disabled		0.9	2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

			SN54ABT8646		SN74ABT8646		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low	3		3		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑	4.5		4.5		ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑	0		0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

			SN54ABT8646		SN74ABT8646		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	5		5		ns
t_{su}	Setup time	A, B, CLK, DIR, $\overline{OE}$, or S before TCK↑	5		5		ns
		TDI before TCK↑	6		6		
		TMS before TCK↑	6		6		
t_h	Hold time	A, B, CLK, DIR, $\overline{OE}$, or S after TCK↑	0		0		ns
		TDI after TCK↑	0		0		
		TMS after TCK↑	0		0		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

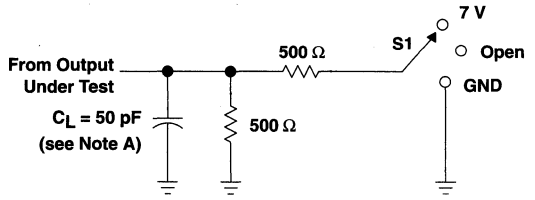
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8646		SN74ABT8646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A	2	3.7	4.5	2	5.5	2	5.2	ns
t_{PHL}			2	3.5	4.4	2	5.8	2	5,5	
t_{PLH}	CLKAB or CLKBA	B or A	3	4.4	5.3	3	6.3	3	6	ns
t_{PHL}			2.5	4.3	5.2	2.5	6.7	2.5	6.2	
t_{PLH}	SAB or SBA	B or A	2	4.8	6	2	7.5	2	7.3	ns
t_{PHL}			2	4.7	5.9	2	7.8	2	7.4	
t_{PZH}	DIR	B or A	2.5	4.4	5.3	2.5	6.6	2.5	6.5	ns
t_{PZL}			3	4.8	6.2	3	7.3	3	7.1	
t_{PZH}	$\overline{OE}$	B or A	2.5	4.4	5.4	2.5	6.7	2.5	6.5	ns
t_{PZL}			3	5.2	6.2	3	7.6	3	7.5	
t_{PHZ}	DIR	B or A	3	6	7	3	8.9	3	8.6	ns
t_{PLZ}			3	5.2	6.2	3	8.1	3	7.9	
t_{PHZ}	$\overline{OE}$	B or A	3	5.9	6.9	3	8.3	3	7.9	ns
t_{PLZ}			3	5.2	6.2	3	7.8	3	7.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

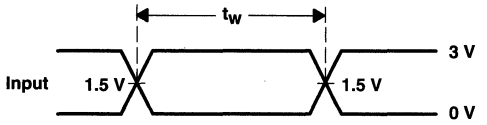
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8646		SN74ABT8646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t_{PHL}			3	7.7	9	3	12	3	11.5	
t_{PLH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PHL}			2.5	4.2	5.5	2.5	7	2.5	6.5	
t_{PZH}	TCK↓	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t_{PZL}			4.5	9	10.5	4.5	13.5	4.5	13	
t_{PZH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PZL}			2.5	4.9	6	2.5	7.5	2.5	7	
t_{PHZ}	TCK↓	A or B	3.5	8.4	10.5	3.5	14	3.5	13.5	ns
t_{PLZ}			3	8	10.5	3	13.5	3	13	
t_{PHZ}	TCK↓	TDO	3	5.9	7	3	9	3	8.5	ns
t_{PLZ}			3	5	6.5	3	8	3	7.5	

PARAMETER MEASUREMENT INFORMATION

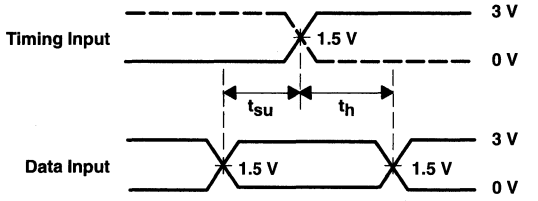


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

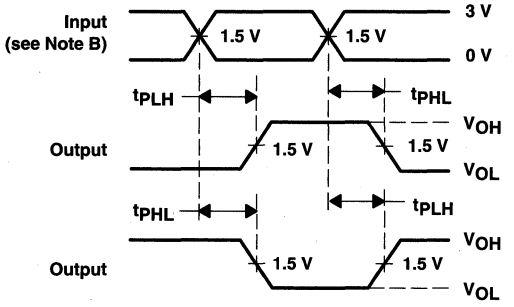
LOAD CIRCUIT FOR OUTPUTS



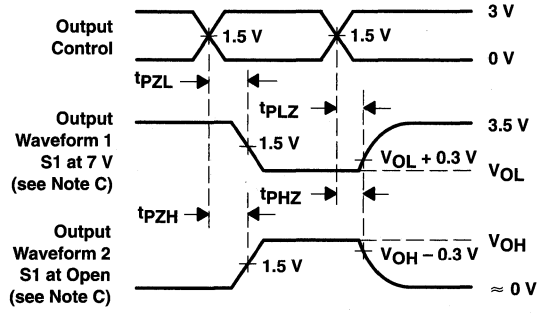
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



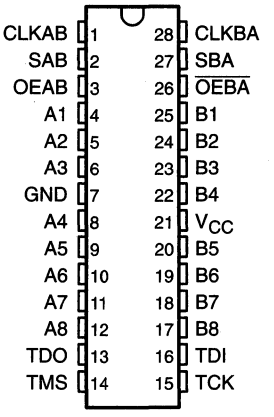
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

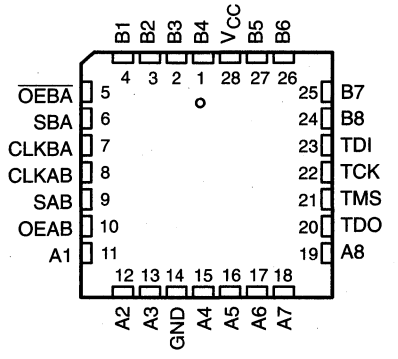
Figure 14. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to SN54/74F652 and SN54/74ABT652 in the Normal Function Mode**
- ***SCOPE*™ Instruction Set:**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs**

SN54ABT8652 . . . JT PACKAGE
SN74ABT8652 . . . DL OR DW PACKAGE
(TOP VIEW)



SN54ABT8652 . . . FK PACKAGE
(TOP VIEW)



description

The SN54ABT8652 and SN74ABT8652 scan test devices with octal bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F652 and SN54/74ABT652 octal bus transceivers and registers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers and registers.

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description (continued)

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and $\overline{\text{OEBA}}$ inputs. Since the $\overline{\text{OEBA}}$ input is active-low, the A outputs are active when $\overline{\text{OEBA}}$ is low and are in the high-impedance state when OEBA is high. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT8652.

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

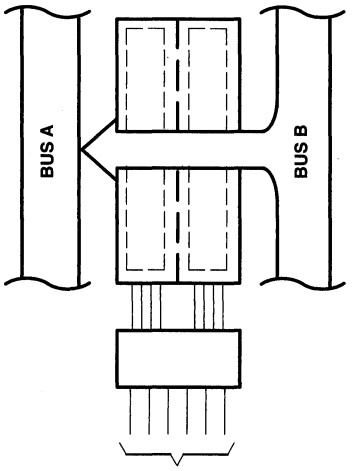
Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8652 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

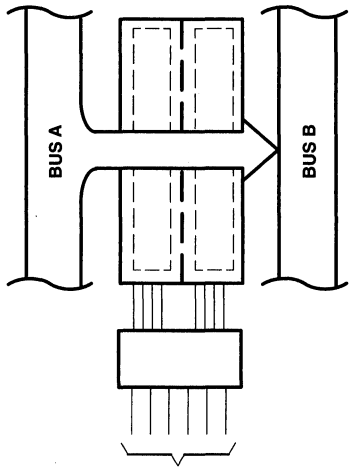
INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input disabled	Input disabled	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified†	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified†	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions can be enabled or disabled by a variety of level combinations at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.



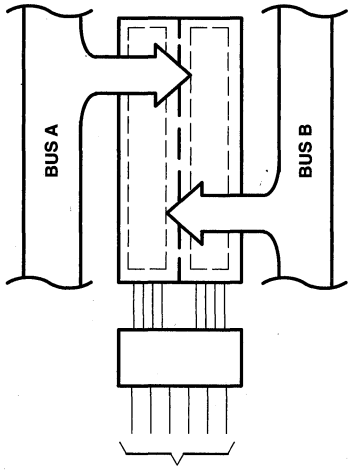
3	26	1	28	2	27
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



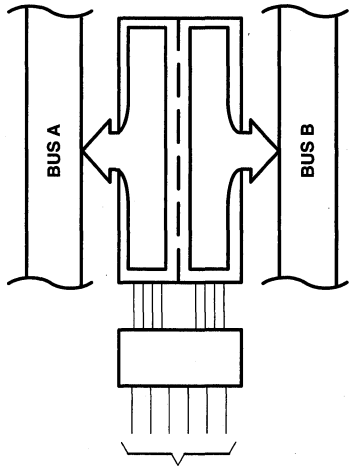
3	26	1	28	2	27
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



3	26	1	28	2	27
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



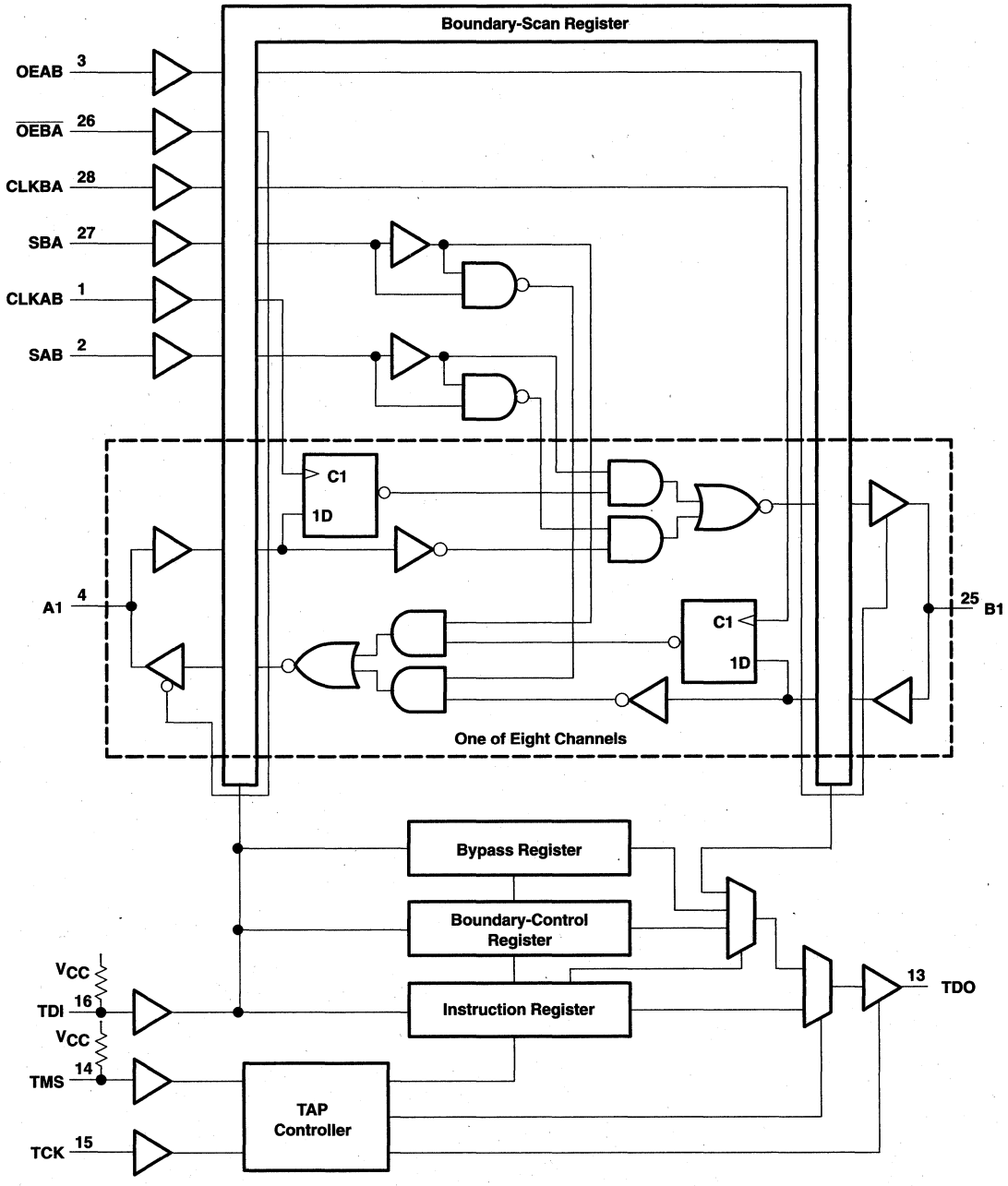
3	26	1	28	2	27
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

Pin numbers shown are for the DL, DW, and JT packages.

functional block diagram



Pin numbers shown are for the DL, DW, and JT packages.

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Terminal Functions

PIN NAME	DESCRIPTION
A1–A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1–B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
GND	Ground
OEAB, $\overline{OEBA}$	Normal-function output-enable inputs. See function table for normal-mode logic.
SAB, SBA	Normal-function select inputs. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

test architecture

Serial test information is conveyed by means of a 4-wire test bus or test access port (TAP), that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. Figure 2 shows the TAP controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and three test data registers: a 38-bit boundary-scan register, an 11-bit boundary-control register, and a one-bit bypass register.

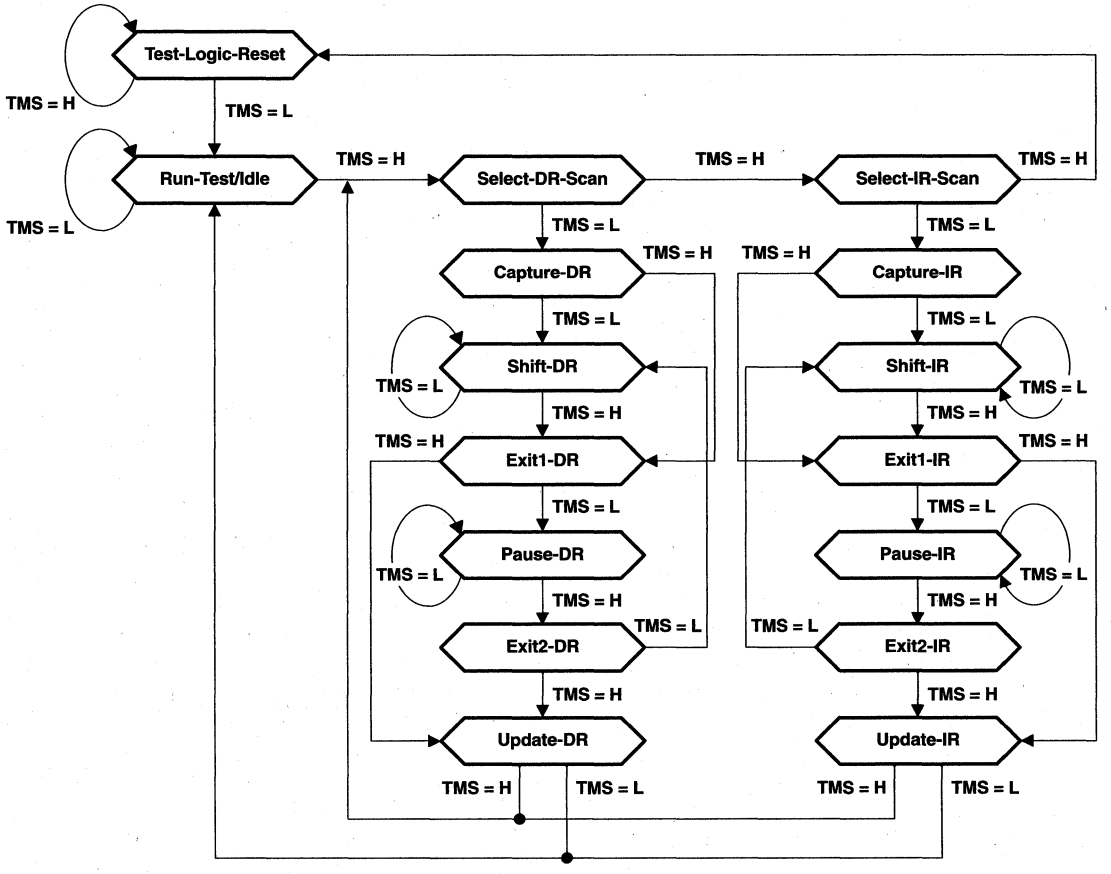


Figure 2. TAP Controller State Diagram

state diagram description

The test access port (TAP) controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated in Figure 2 and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of sixteen states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller will return to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that will force it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8652, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0 except bit 36, which is reset to logic 1. The boundary-control register is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state can also be entered following data register or instruction register scans. Run-Test/Idle is provided as a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller will exit either of these states on the next TCK cycle. These states are provided to allow the selection of either data register scan or instruction register scan.

Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

state diagram description (continued)

Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states used to end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state provides the capability of suspending and resuming data register scan operations without loss of data.

Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK following entry to the Update-DR state.

Capture-IR

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state.

For the 'ABT8652, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

state diagram description (continued)

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state provides the capability of suspending and resuming instruction register scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

register overview

With the exception of the bypass register, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register description

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8652. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction.

The instruction register order of scan is illustrated in Figure 3.

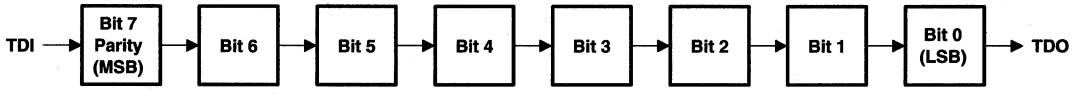


Figure 3. Instruction Register Order of Scan

data register description

boundary-scan register

The boundary-scan register (BSR) is 38 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and two BSCs for each normal-function I/O pin (one for input data and one for output data). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0 except BSC 36, which is reset to logic 1.

The boundary-scan register order of scan is from TDI through bits 37–0 to TDO. Table 1 shows the boundary-scan register bits and their associated device pin signals.

Table 1. Boundary-Scan Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
37	OEAB	31	A8-I	23	A8-O	15	B8-I	7	B8-O
36	$\overline{\text{OEBA}}$	30	A7-I	22	A7-O	14	B7-I	6	B7-O
35	CLKAB	29	A6-I	21	A6-O	13	B6-I	5	B6-O
34	CLKBA	28	A5-I	20	A5-O	12	B5-I	4	B5-O
33	SAB	27	A4-I	19	A4-O	11	B4-I	3	B4-O
32	SBA	26	A3-I	18	A3-O	10	B3-I	2	B3-O
—	—	25	A2-I	17	A2-O	9	B2-I	1	B2-O
—	—	24	A1-I	16	A1-O	8	B1-I	0	B1-O

boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include pseudo-random pattern generation (PRPG), parallel signature analysis (PSA) with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The boundary-control register order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the boundary-control register bits and their associated test control signals.

Table 2. Boundary-Control Register Configuration

BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL
10	MASK8	6	MASK4	2	OPCODE2
9	MASK7	5	MASK3	1	OPCODE1
8	MASK6	4	MASK2	0	OPCODE0
7	MASK5	3	MASK1	—	—

data register description (continued)

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is illustrated in Figure 4.

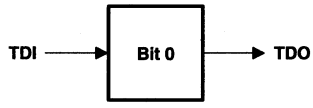


Figure 4. Bypass Register Order of Scan

Table 3. Instruction Register Opcodes

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	BYPASS‡	Bypass scan	Bypass	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	INTEST	Boundary scan	Boundary scan	Test
10000100	BYPASS‡	Bypass scan	Bypass	Normal
00000101	BYPASS‡	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS‡	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT8652.

instruction register opcode description

The instruction register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

control boundary to high impedance

This instruction conforms to the IEEE P1149.1A HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE P1149.1A CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the boundary-control register is executed during Run-Test/Idle. The five test operations decoded by the boundary-control register are: sample inputs/toggle outputs (TOPSIP), pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

boundary read

The boundary-scan register is selected in the scan path. The value in the boundary-scan register remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The boundary-scan register is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift register and shadow latch elements of the boundary-scan register. The device operates in the normal mode.

instruction register opcode description (continued)

boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

boundary-control register scan

The boundary-control register is selected in the scan path. The value in the boundary-control register remains unchanged during Capture-DR. This operation must be performed prior to a boundary run test operation in order to specify which test operation is to be executed.

Table 4. Boundary-Control Register Opcodes

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/16-bit mode (PRPG)
X10	Parallel signature analysis/16-bit mode (PSA)
011	Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT)

boundary-control register opcode description

The boundary-control register opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

It should be noted, in general, that while the control input BSCs (bits 37–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 37–36 of the BSR) do control the drive state (active or high impedance) of the selected device output pins. It also should be noted that these BCR instructions are only valid when the device is operating in one direction of data flow (that is, OEAB = $\overline{\text{OEBA}}$). Otherwise, the bypass instruction is operated.

PSA input masking

Bits 10–3 of the boundary-control register are used to specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in Table 3. When the mask bit which corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

boundary-control register opcode description (continued)

sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK.

pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK and then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK. This data is also updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Figures 5 and 6 illustrate the 16-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

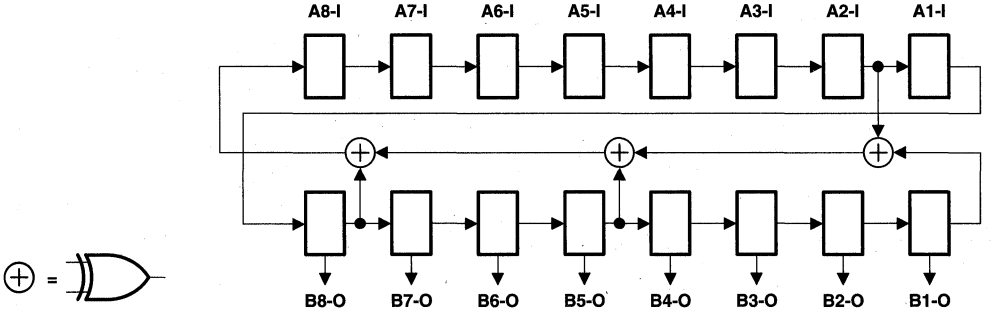


Figure 5. 16-Bit PRPG Configuration (OEAB = 1, $\overline{OEBA}$ = 1)

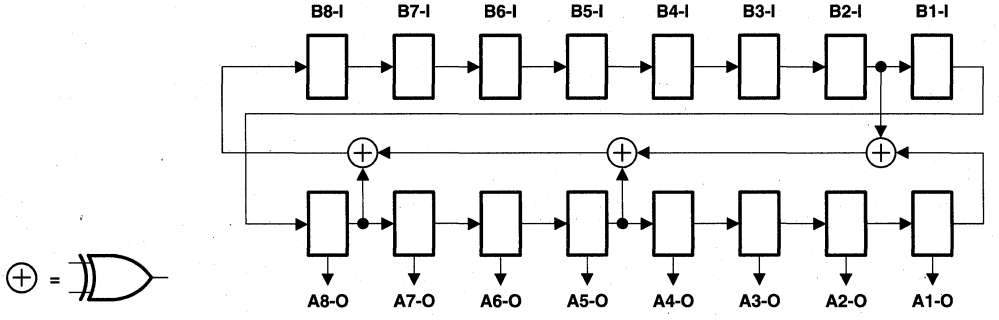


Figure 6. 16-Bit PRPG Configuration (OEAB = 0, $\overline{OEBA}$ = 0)

boundary-control register opcode description (continued)

parallel signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 7 and 8 illustrate the 16-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

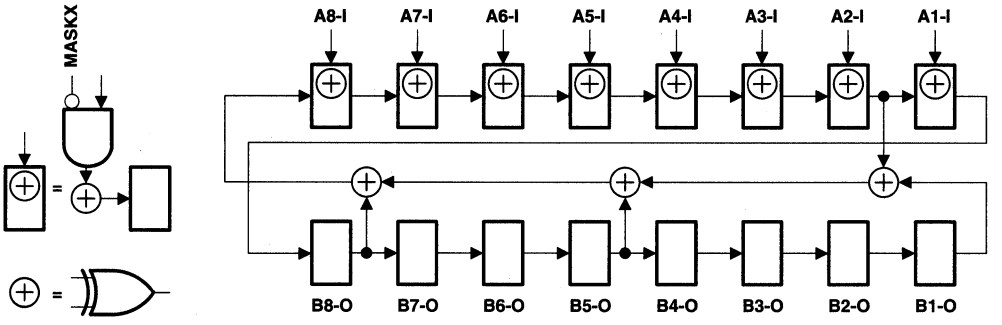


Figure 7. 16-Bit PSA Configuration (OEAB = 1, $\overline{OEBA}$ = 1)

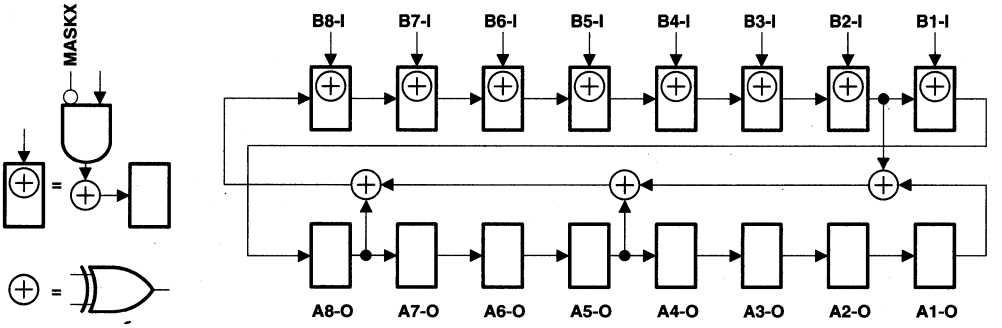


Figure 8. 16-Bit PSA Configuration (OEAB = 0, $\overline{OEBA}$ = 0)

boundary-control register opcode description (continued)

simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. Figures 9 and 10 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

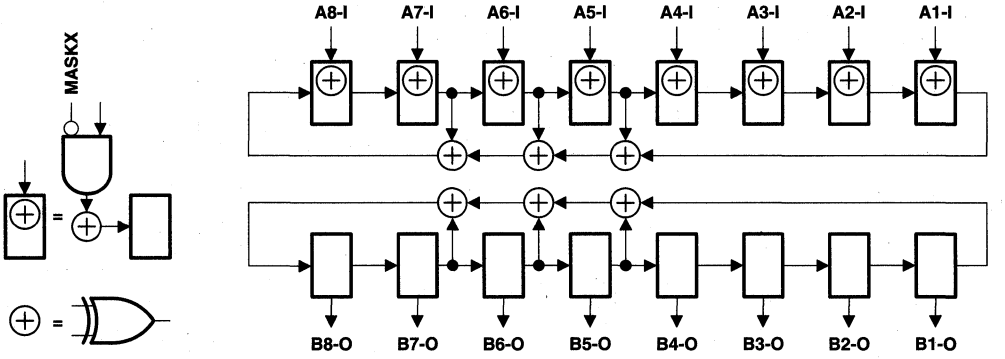


Figure 9. 8-Bit PSA/PRPG Configuration (OEAB = 1, $\overline{OEBA}$ = 1)

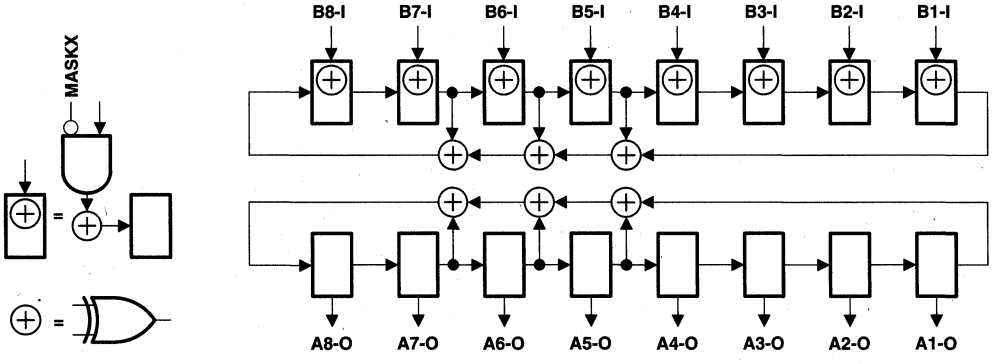


Figure 10. 8-Bit PSA/PRPG Configuration (OEAB = 0, $\overline{OEBA}$ = 0)

boundary-control register opcode description (continued)

simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. In addition, the shift-register elements of the opposite output BSCs are used to count carries out of the selected output BSCs and, thereby, extend the count to 16 bits. Figures 11 and 12 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

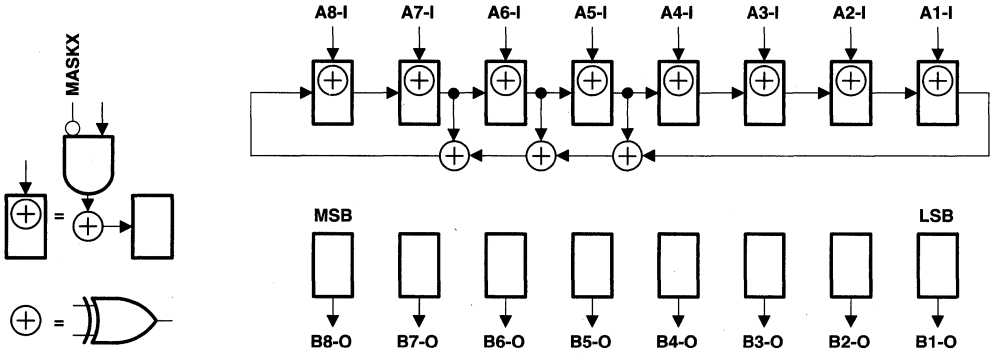


Figure 11. 8-Bit PSA/COUNT Configuration (OEAB = 1, $\overline{OEBA}$ = 1)

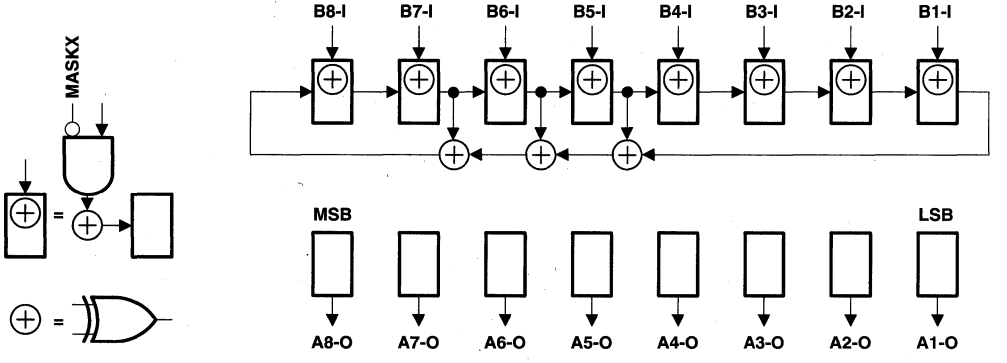


Figure 12. 8-Bit PSA/COUNT Configuration (OEAB = 0, $\overline{OEBA}$ = 0)

timing description

All test operations of the 'ABT8652 are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in Figure 2) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction register scan and one data register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

Table 5. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19–20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

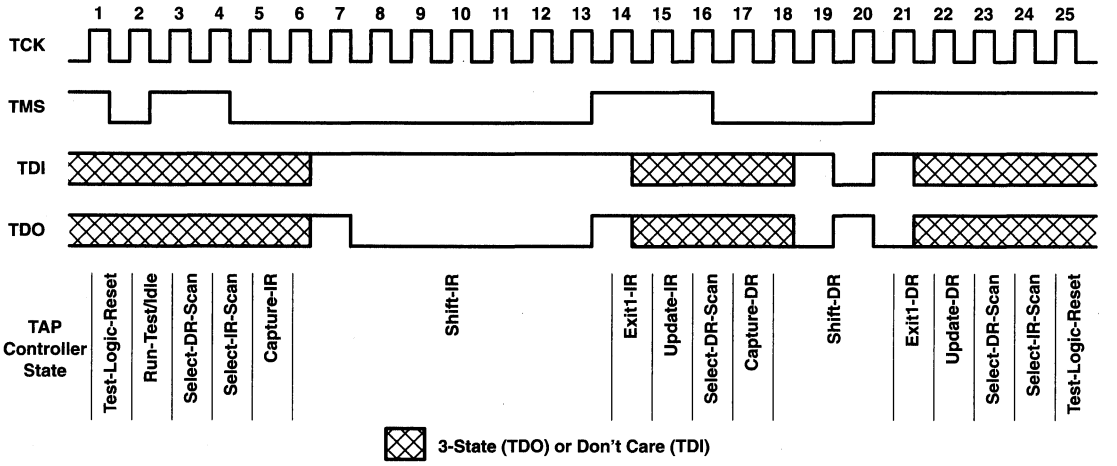


Figure 13. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8652 ..... 96 mA
SN74ABT8652 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8652		SN74ABT8652		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT8652		SN74ABT8652		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, OEAB, OEBA, S, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC}	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	TDI, TMS			–160		–160		–160	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{OFF}	V_{CC} = 0,	V_I or V_O ≤ 5.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		0.9	2		2		2	mA
			Outputs low		30	38		38		38	
			Outputs disabled		0.9	2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

			SN54ABT8652		SN74ABT8652		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low	3		3		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑	4.5		4.5		ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑	0		0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

			SN54ABT8652		SN74ABT8652		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	5		5		ns
t_{su}	Setup time	A, B, CLK, OEAB, $\overline{OEBA}$, or S before TCK↑	5		5		ns
		TDI before TCK↑	6		6		
		TMS before TCK↑	6		6		
t_h	Hold time	A, B, CLK, OEAB, $\overline{OEBA}$, or S after TCK↑	0		0		ns
		TDI after TCK↑	0		0		
		TMS after TCK↑	0		0		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

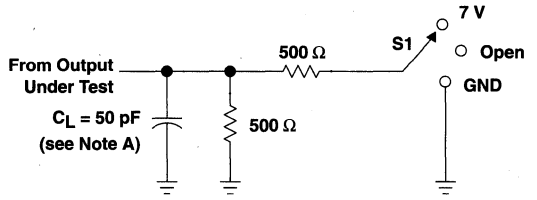
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8652		SN74ABT8652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A	2	3.7	4.5	2	5.5	2	5.2	ns
t_{PHL}			1.5	3.5	4.4	1.5	5.8	1.5	5.5	
t_{PLH}	CLKAB or CLKBA	B or A	2.5	4.4	5.3	2.5	6.3	2.5	6	ns
t_{PHL}			2.5	4.3	5.2	2.5	6.7	2.5	6.2	
t_{PLH}	SAB or SBA	B or A	2	4.8	6	2	7.5	2	7.3	ns
t_{PHL}			2	4.7	5.9	2	7.8	2	7.4	
t_{PZH}	OEAB or $\overline{OEBA}$	B or A	2	4.4	5.4	2	6.7	2	6.5	ns
t_{PZL}			2	5.2	6.2	2	7.6	2	7.5	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A	2	5.9	6.9	2	8.3	2	7.9	ns
t_{PLZ}			2	5.2	6.2	2	7.8	2	7.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

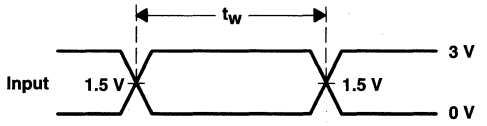
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8652		SN74ABT8652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t_{PHL}			3	7.7	9	3	12	3	11.5	
t_{PLH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PHL}			2.5	4.2	5.5	2.5	7	2.5	6.5	
t_{PZH}	TCK↓	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t_{PZL}			4.5	9	10.5	4.5	13.5	4.5	13	
t_{PZH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PZL}			2.5	4.9	6	2.5	7.5	2.5	7	
t_{PHZ}	TCK↓	A or B	3.5	8.4	10.5	3.5	14	3.5	13.5	ns
t_{PLZ}			3	8	10.5	3	13.5	3	13	
t_{PHZ}	TCK↓	TDO	3	5.9	7	3	9	3	8.5	ns
t_{PLZ}			3	5	6.5	3	8	3	7.5	

PARAMETER MEASUREMENT INFORMATION

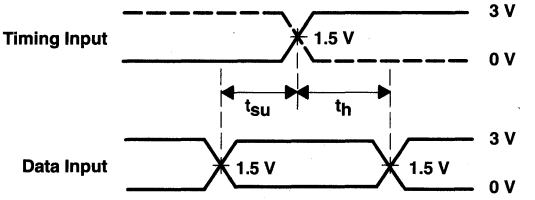


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

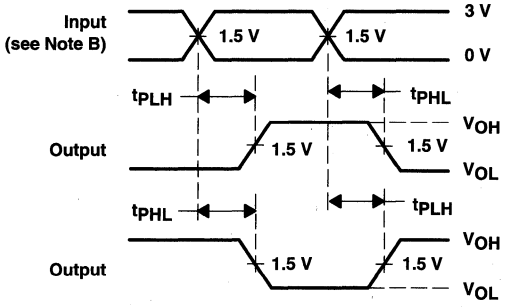
LOAD CIRCUIT FOR OUTPUTS



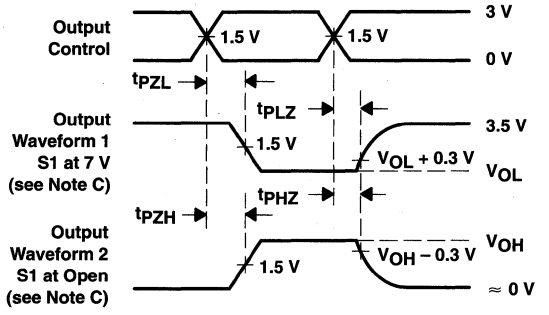
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



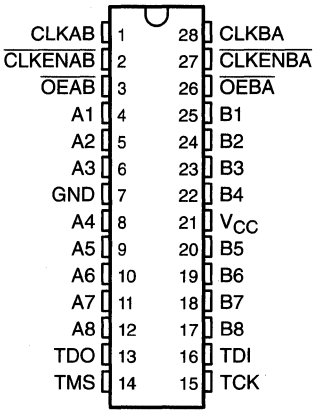
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

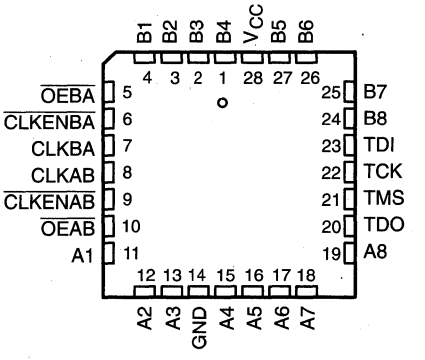
Figure 14. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to SN54/74BCT2952 and SN54/74ABT2952 in the Normal Function Mode**
- ***SCOPE*™ Instruction Set:**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs**

SN54ABT8952 . . . JT PACKAGE
SN74ABT8952 . . . DL OR DW PACKAGE
(TOP VIEW)



SN54ABT8952 . . . FK PACKAGE
(TOP VIEW)



description

The SN54ABT8952 and SN74ABT8952 scan test devices with octal registered bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74BCT2952 and SN54/74ABT2952 octal registered bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal registered bus transceivers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), clock-enable ($\overline{\text{CLKENAB}}$ and $\overline{\text{CLKENBA}}$), and output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, A-bus data is stored in the associated registers on the low-to-high transition of CLKAB provided that $\overline{\text{CLKENAB}}$ is low. Otherwise, if $\overline{\text{CLKENAB}}$ is high or CLKAB remains at a static low or high level, the register contents are not changed. When $\overline{\text{OEAB}}$ is low, the B outputs are active. When $\overline{\text{OEAB}}$ is high, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B but uses CLKBA, $\overline{\text{CLKENBA}}$, and $\overline{\text{OEBA}}$.

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description (continued)

In the test mode, the normal operation of the SCOPE™ registered bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

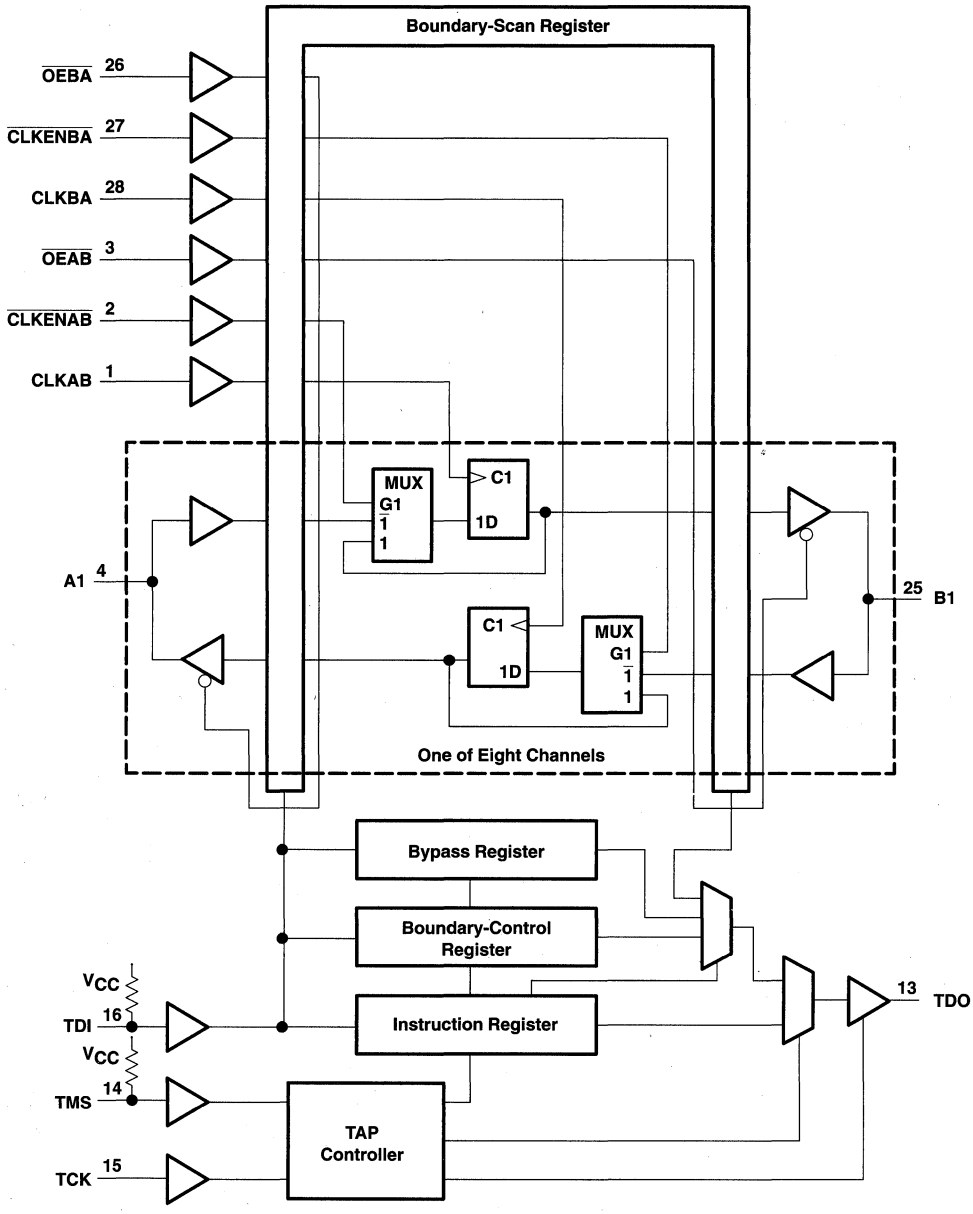
The SN54ABT8952 is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74ABT8952 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE† (normal mode, each register)

INPUTS				OUTPUT
$\overline{OEAB}$	$\overline{CLKENAB}$	CLKAB	A	B
L	L	↑	L	L
L	L	↑	H	H
L	H	X	X	B_0
L	X	L	X	B_0
H	X	X	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{OEBA}$, $\overline{CLKENBA}$, and CLKBA.

functional block diagram



Pin numbers shown are for the DL, DW, and JT packages.

Terminal Functions

PIN NAME	DESCRIPTION
A1–A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1–B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
$\overline{\text{CLKENAB}}$, $\overline{\text{CLKENBA}}$	Normal-function clock-enable inputs. See function table for normal-mode logic.
GND	Ground
$\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$	Normal-function output-enable inputs. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

test architecture

Serial test information is conveyed by means of a 4-wire test bus or test access port (TAP), that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and three test data registers: a 38-bit boundary-scan register, an 11-bit boundary-control register, and a one-bit bypass register.

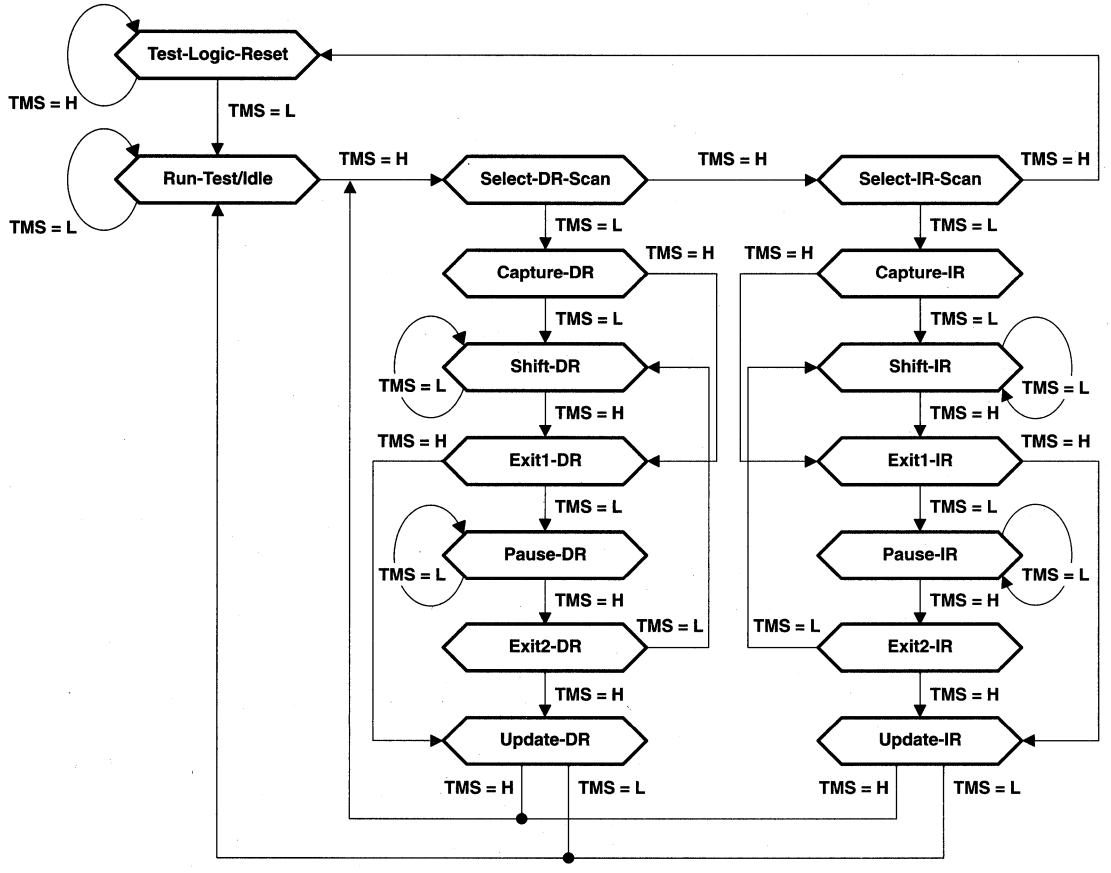


Figure 1. TAP Controller State Diagram

state diagram description

The test access port (TAP) controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated in Figure 1 and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of sixteen states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller will return to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that will force it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8952, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0 except bits 37–36, which are reset to logic 1. The boundary-control register is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state can also be entered following data register or instruction register scans. Run-Test/Idle is provided as a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller will exit either of these states on the next TCK cycle. These states are provided to allow the selection of either data register scan or instruction register scan.

Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

state diagram description (continued)

Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states used to end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state provides the capability of suspending and resuming data register scan operations without loss of data.

Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK following entry to the Update-DR state.

Capture-IR

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state.

For the 'ABT8952, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

state diagram description (continued)

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state provides the capability of suspending and resuming instruction register scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

register overview

With the exception of the bypass register, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register description

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8952. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction.

The instruction register order of scan is illustrated in Figure 2.

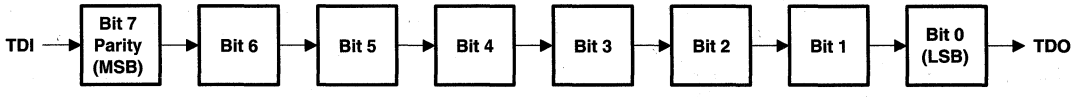


Figure 2. Instruction Register Order of Scan

data register description

boundary-scan register

The boundary-scan register (BSR) is 38 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and two BSCs for each normal-function I/O pin (one for input data and one for output data). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0 except BSCs 37–36, which are reset to logic 1.

The boundary-scan register order of scan is from TDI through bits 37–0 to TDO. Table 1 shows the boundary-scan register bits and their associated device pin signals.

Table 1. Boundary-Scan Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
37	$\overline{\text{OEAB}}$	31	A8-I	23	A8-O	15	B8-I	7	B8-O
36	$\overline{\text{OEBA}}$	30	A7-I	22	A7-O	14	B7-I	6	B7-O
35	CLKAB	29	A6-I	21	A6-O	13	B6-I	5	B6-O
34	CLKBA	28	A5-I	20	A5-O	12	B5-I	4	B5-O
33	$\overline{\text{CLKENAB}}$	27	A4-I	19	A4-O	11	B4-I	3	B4-O
32	$\overline{\text{CLKENBA}}$	26	A3-I	18	A3-O	10	B3-I	2	B3-O
—	—	25	A2-I	17	A2-O	9	B2-I	1	B2-O
—	—	24	A1-I	16	A1-O	8	B1-I	0	B1-O

boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include pseudo-random pattern generation (PRPG), parallel signature analysis (PSA) with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The boundary-control register order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the boundary-control register bits and their associated test control signals.

Table 2. Boundary-Control Register Configuration

BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL
10	MASK8	6	MASK4	2	OPCODE2
9	MASK7	5	MASK3	1	OPCODE1
8	MASK6	4	MASK2	0	OPCODE0
7	MASK5	3	MASK1	—	—

data register description (continued)

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is illustrated in Figure 3.

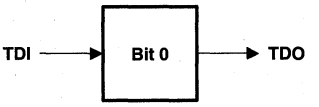


Figure 3. Bypass Register Order of Scan

Table 3. Instruction Register Opcodes

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	BYPASS‡	Bypass scan	Bypass	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	INTEST	Boundary scan	Boundary scan	Test
10000100	BYPASS‡	Bypass scan	Bypass	Normal
00000101	BYPASS‡	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS‡	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT8952.

instruction register opcode description

The instruction register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

control boundary to high impedance

This instruction conforms to the IEEE P1149.1A HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE P1149.1A CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the boundary-control register is executed during Run-Test/Idle. The five test operations decoded by the boundary-control register are: sample inputs/toggle outputs (TOPSIP), pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

boundary read

The boundary-scan register is selected in the scan path. The value in the boundary-scan register remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The boundary-scan register is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift register and shadow latch elements of the boundary-scan register. The device operates in the normal mode.

instruction register opcode description (continued)

boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

boundary-control register scan

The boundary-control register is selected in the scan path. The value in the boundary-control register remains unchanged during Capture-DR. This operation must be performed prior to a boundary run test operation in order to specify which test operation is to be executed.

Table 4. Boundary-Control Register Opcodes

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/16-bit mode (PRPG)
X10	Parallel signature analysis/16-bit mode (PSA)
011	Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT)

boundary-control register opcode description

The boundary-control register opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

It should be noted, in general, that while the control input BSCs (bits 37–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 37–36 of the BSR) do control the drive state (active or high impedance) of the selected device output pins. It also should be noted that these BCR instructions are only valid when the device is operating in one direction of data flow (that is, $\overline{OEAB} \neq \overline{OEBA}$). Otherwise, the bypass instruction is operated.

PSA input masking

Bits 10–3 of the boundary-control register are used to specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in Table 3. When the mask bit which corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

boundary-control register opcode description (continued)

sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK.

pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK and then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK. This data is also updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Figures 4 and 5 illustrate the 16-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

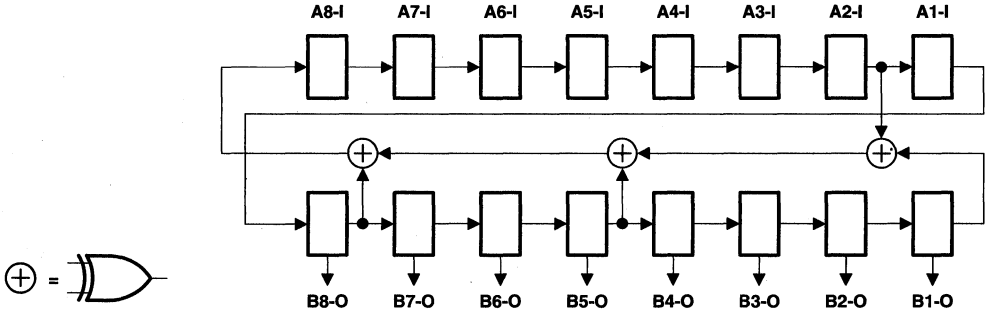


Figure 4. 16-Bit PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

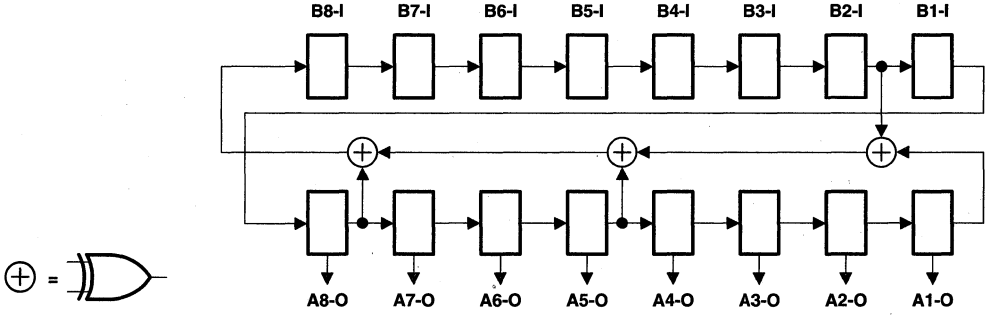


Figure 5. 16-Bit PRPG Configuration ($\overline{OEAB}$=1, $\overline{OEBA}$ = 0)

boundary-control register opcode description (continued)

parallel signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 6 and 7 illustrate the 16-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

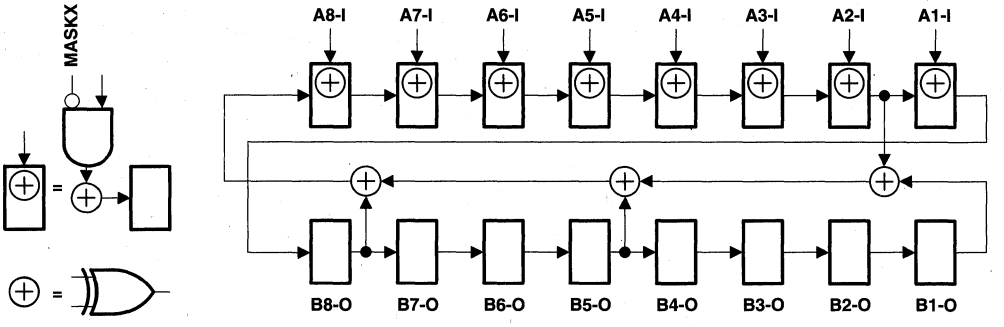


Figure 6. 16-Bit PSA Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

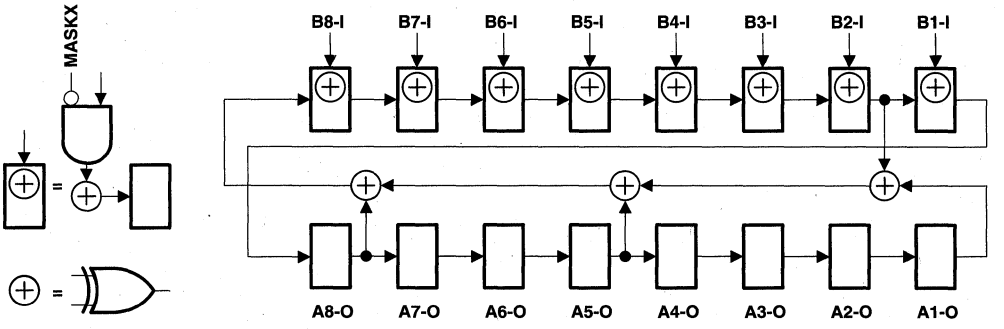


Figure 7. 16-Bit PSA Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

boundary-control register opcode description (continued)

simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. Figures 8 and 9 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

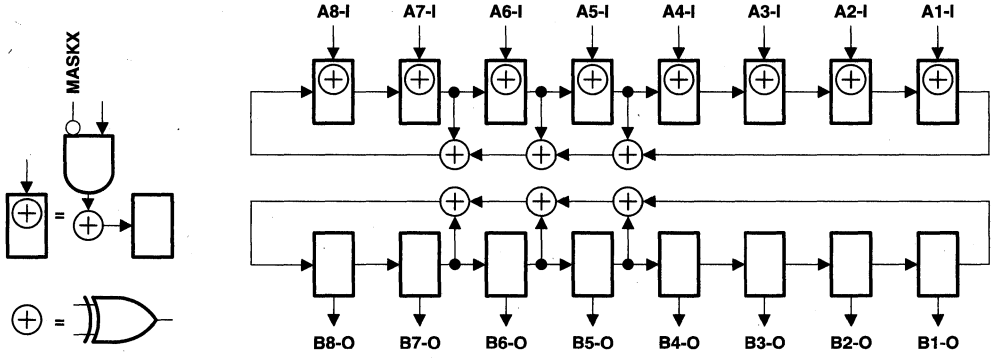


Figure 8. 8-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

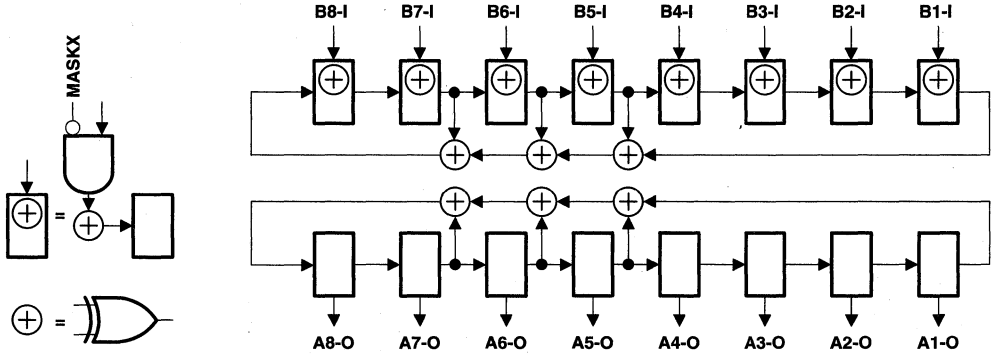


Figure 9. 8-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

boundary-control register opcode description (continued)

simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. In addition, the shift-register elements of the opposite output BSCs are used to count carries out of the selected output BSCs and, thereby, extend the count to 16 bits. Figures 10 and 11 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

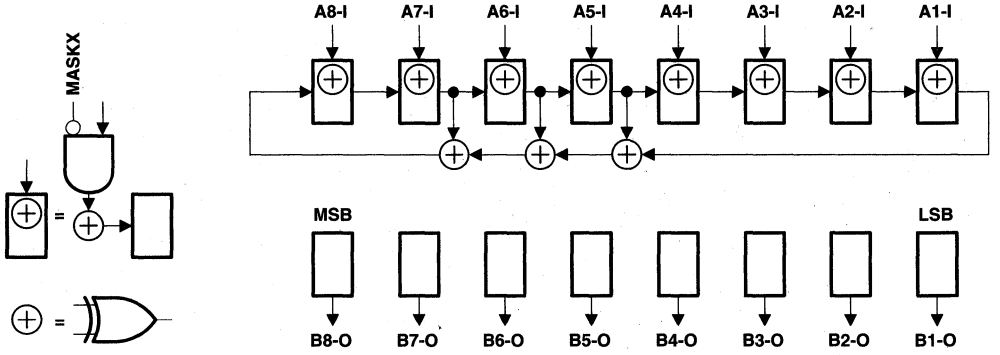


Figure 10. 8-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

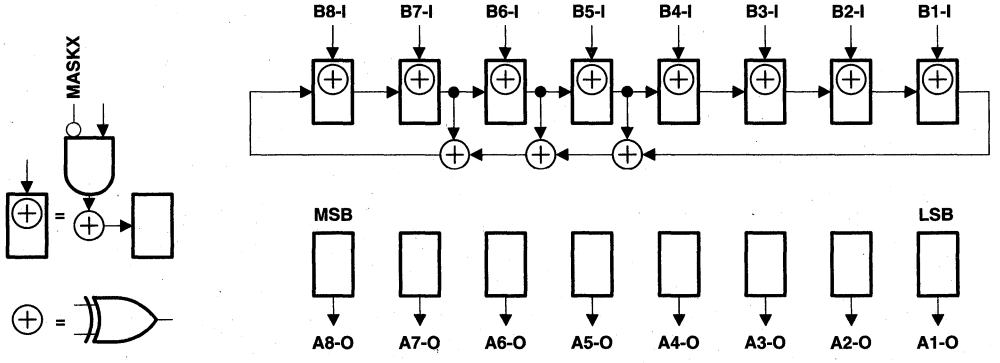


Figure 11. 8-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

timing description

All test operations of the 'ABT8952 are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 12. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction register scan and one data register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

Table 5. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19–20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

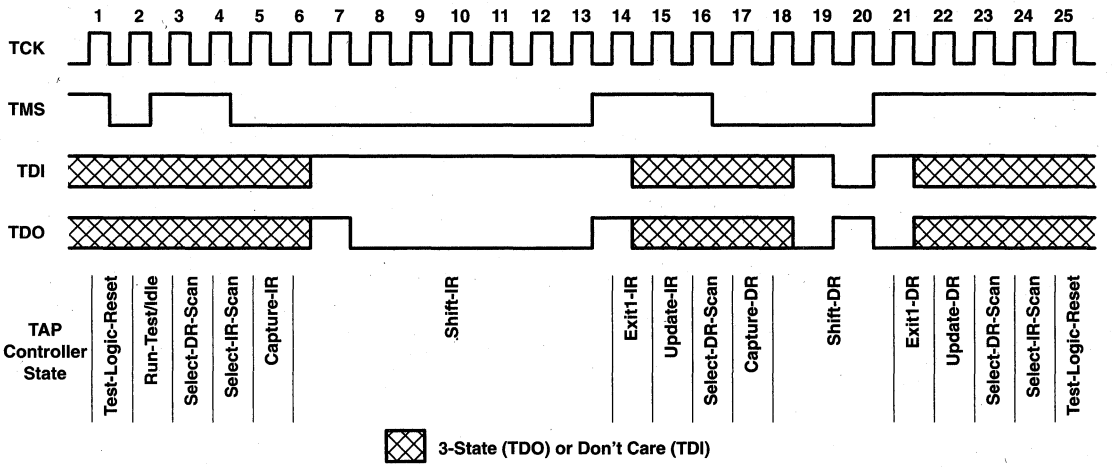


Figure 12. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8952 ..... 96 mA
SN74ABT8952 ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8952		SN74ABT8952		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT8952		SN74ABT8952		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, $\overline{CLKEN}$, $\overline{OE}$, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC}	TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	TDI, TMS			–160		–160		–160	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 5.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		0.9	2		2		2	mA
			Outputs low		30	38		38		38	
			Outputs disabled		0.9	2		2		2	
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

			SN54ABT8952		SN74ABT8952		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low	3		3		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑	4.5		4.5		ns
		$\overline{CLKEN}$ before CLK↑	4.5		4.5		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑	0		0		ns
		$\overline{CLKEN}$ after CLK↑	0		0		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

			SN54ABT8952		SN74ABT8952		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	5		5		ns
t_{su}	Setup time	A, B, CLK, $\overline{CLKEN}$, or $\overline{OE}$ before TCK↑	5		5		ns
		TDI before TCK↑	6		6		
		TMS before TCK↑	6		6		
t_h	Hold time	A, B, CLK, $\overline{CLKEN}$, or $\overline{OE}$ after TCK↑	0		0		ns
		TDI after TCK↑	0		0		
		TMS after TCK↑	0		0		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

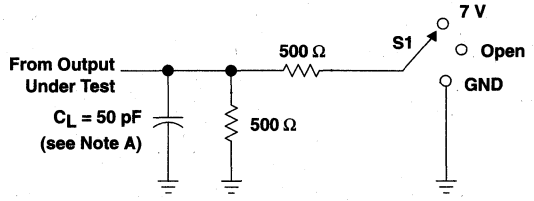
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8952		SN74ABT8952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLK	A or B	100	130		100		100		MHz
t_{PLH}	CLKAB or CLKBA	B or A	3	4.6	5.4	3	6.5	3	6.3	ns
t_{PHL}			2.5	3.8	4.6	2.5	5.5	2.5	5.3	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.1	4.9	2	5.9	2	5.8	ns
t_{PZL}			2.5	4.7	5.5	2.5	7.1	2.5	6.9	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2.5	5.3	6.1	2.5	7.5	2.5	7.3	ns
t_{PLZ}			3	4.5	5.3	3	6.3	3	6.1	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

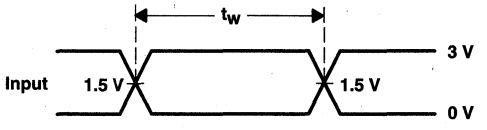
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT8952		SN74ABT8952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t_{PHL}			3	7.7	9	3	12	3	11.5	
t_{PLH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PHL}			2.5	4.2	5.5	2.5	7	2.5	6.5	
t_{PZH}	TCK↓	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t_{PZL}			4.5	9	10.5	4.5	13.5	4.5	13	
t_{PZH}	TCK↓	TDO	2.5	4.3	5.5	2.5	7	2.5	6.5	ns
t_{PZL}			2.5	4.9	6	2.5	7.5	2.5	7	
t_{PHZ}	TCK↓	A or B	3.5	8.4	10.5	3.5	14	3.5	13.5	ns
t_{PLZ}			3	8	10.5	3	13.5	3	13	
t_{PHZ}	TCK↓	TDO	3	5.9	7	3	9	3	8.5	ns
t_{PLZ}			3	5	6.5	3	8	3	7.5	

PARAMETER MEASUREMENT INFORMATION

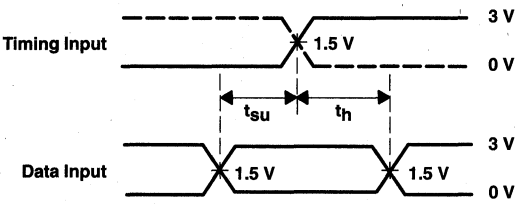


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

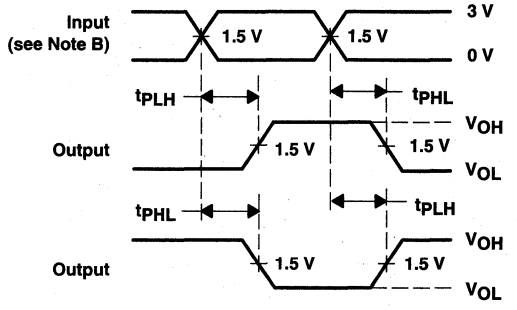
LOAD CIRCUIT FOR OUTPUTS



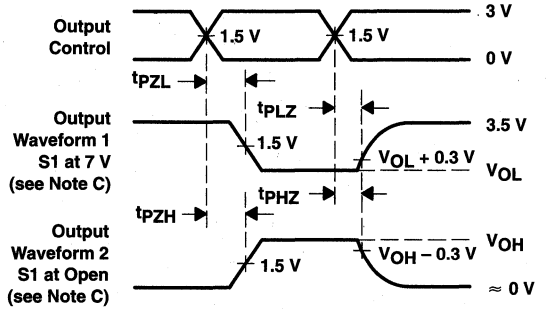
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



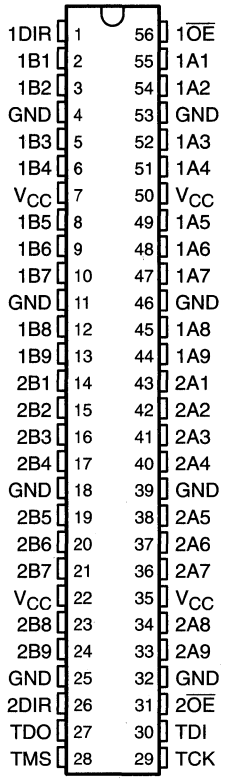
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 13. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT18245 . . . WD PACKAGE
SN74ABT18245 . . . DL PACKAGE
(TOP VIEW)



description

The SN54ABT18245 and SN74ABT18245 scan test devices with 18-bit bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit noninverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

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description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

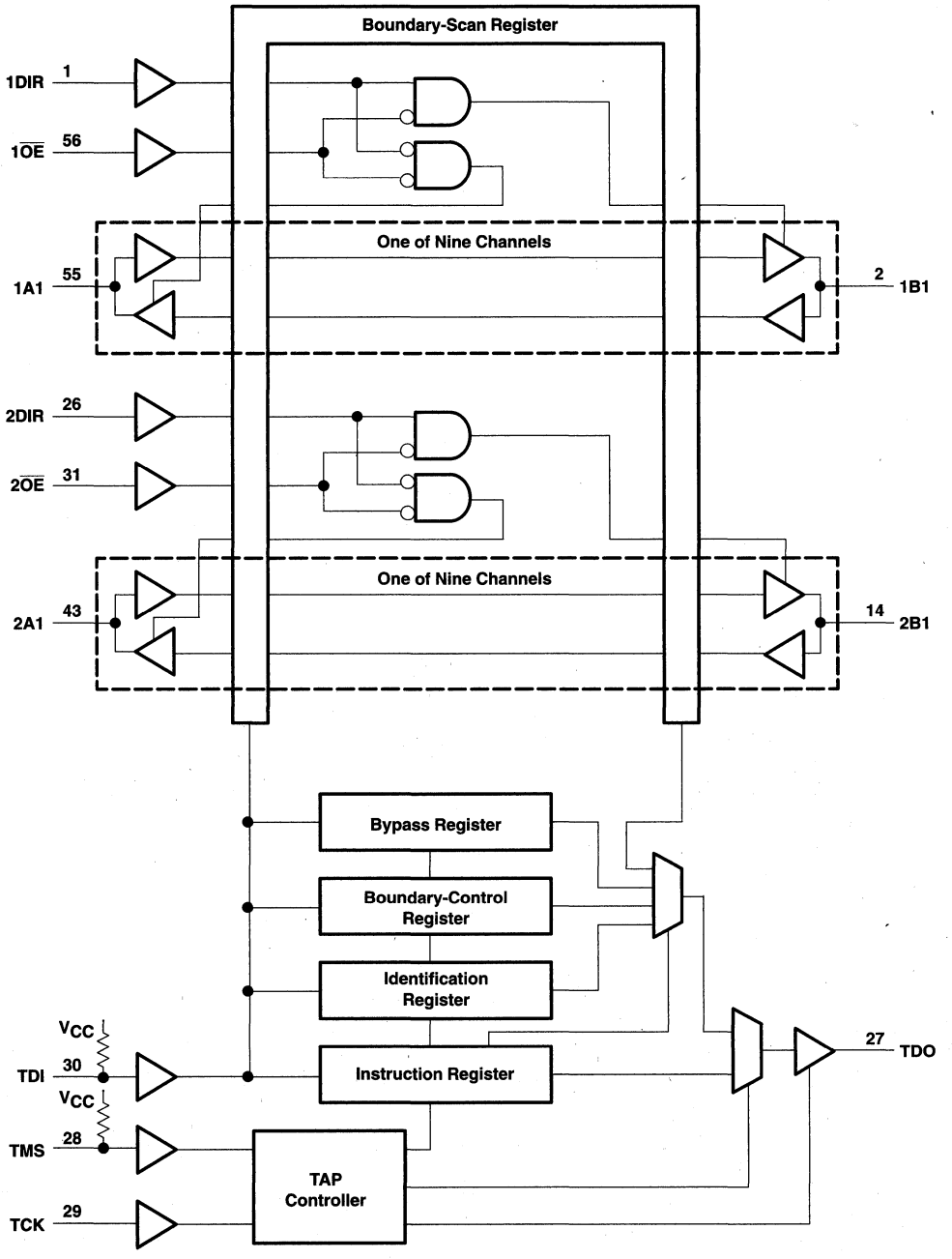
The SN74ABT18245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT18245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT18245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

functional block diagram



Terminal Functions

PIN NAME	DESCRIPTION
GND	Ground
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1DIR, 2DIR	Normal-function direction controls. See function table for normal-mode logic.
$1\overline{OE}$, $2\overline{OE}$	Normal-function output enables. See function table for normal-mode logic.

test architecture

Serial test information is conveyed by means of a 4-wire test bus or test access port (TAP), that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and four test data registers: a 44-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device identification register.

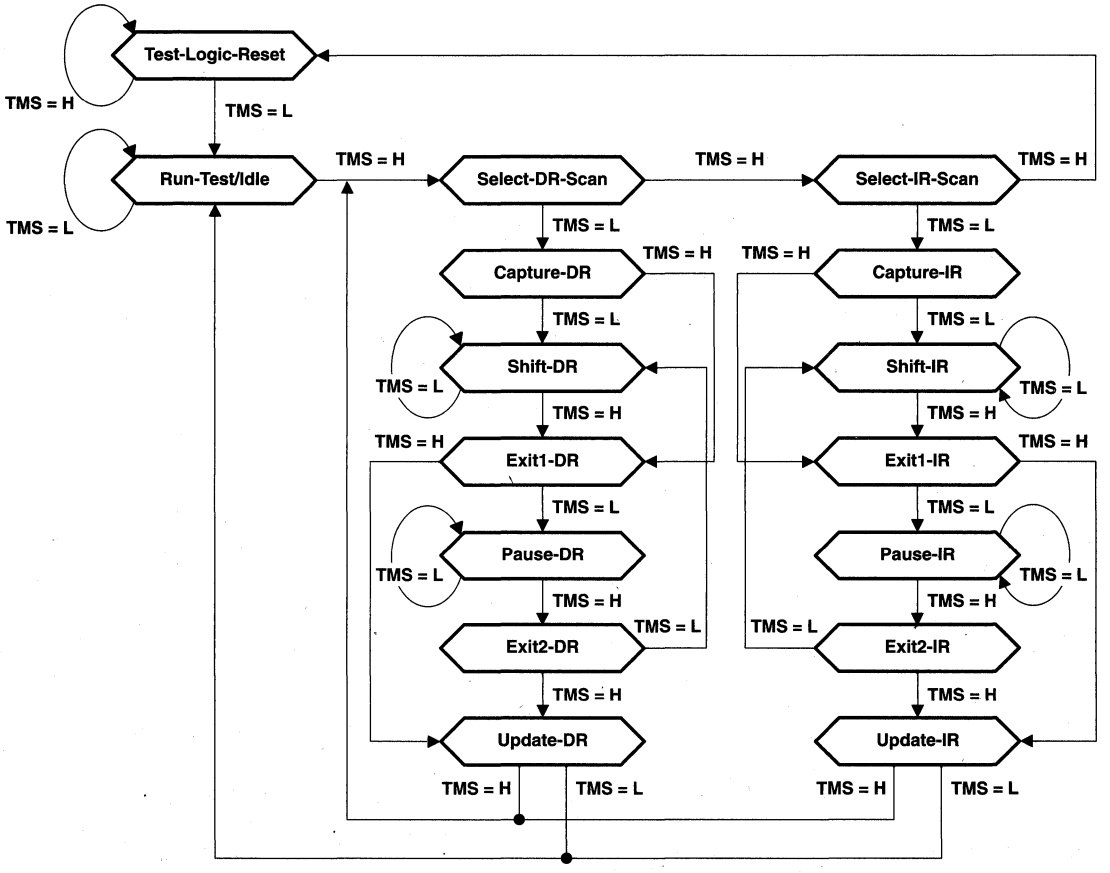


Figure 1. TAP Controller State Diagram

state diagram description

The test access port (TAP) controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated in Figure 1 and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of sixteen states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT18245, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Each bit in the boundary-scan register is reset to logic 0. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state can also be entered following data register or instruction register scans. Run-Test/Idle is provided as a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states are provided to allow the selection of either data register scan or instruction register scan.

Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

state diagram description (continued)

Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states used to end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state provides the capability of suspending and resuming data register scan operations without loss of data.

Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK following entry to the Update-DR state.

Capture-IR

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state.

For the 'ABT18245, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state provides the capability of suspending and resuming instruction register scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

register overview

With the exception of the bypass and device identification registers, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass and device identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register description

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT18245. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction.

The instruction register order of scan is illustrated in Figure 2.

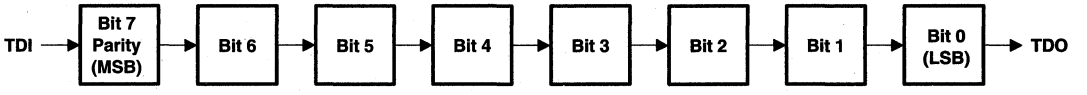


Figure 2. Instruction Register Order of Scan

data register description

boundary-scan register

The boundary-scan register (BSR) is 44 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, one BSC for each normal-function I/O pin (one single cell for both input data and output data), and one BSC for each of the internally decoded output-enable signals (1OEA, 2OEA, 1OEB, 2OEB). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0.

When external data is to be captured, the BSCs for signals 1OEA, 2OEA, $1\overline{OEB}$, and $2\overline{OEB}$ capture logic values determined by the following positive-logic equations: $1OEA = 1\overline{OE} \bullet \overline{1DIR}$, $2OEA = 2\overline{OE} \bullet \overline{2DIR}$, $1OEB = 1\overline{OE} \bullet DIR$, and $2OEB = 2\overline{OE} \bullet DIR$. When data is to be applied externally, these BSCs control the drive state (active or high impedance) of their respective outputs.

The boundary-scan register order of scan is from TDI through bits 43–0 to TDO. Table 1 shows the boundary-scan register bits and their associated device pin signals.

Table 1. Boundary-Scan Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
43	2OEB	35	2A9-I/O	26	1A9-I/O	17	2B9-I/O	8	1B9-I/O
42	1OEB	34	2A8-I/O	25	1A8-I/O	16	2B8-I/O	7	1B8-I/O
41	2OEA	33	2A7-I/O	24	1A7-I/O	15	2B7-I/O	6	1B7-I/O
40	1OEA	32	2A6-I/O	23	1A6-I/O	14	2B6-I/O	5	1B6-I/O
39	2DIR	31	2A5-I/O	22	1A5-I/O	13	2B5-I/O	4	1B5-I/O
38	1DIR	30	2A4-I/O	21	1A4-I/O	12	2B4-I/O	3	1B4-I/O
37	$2\overline{OE}$	29	2A3-I/O	20	1A3-I/O	11	2B3-I/O	2	1B3-I/O
36	$1\overline{OE}$	28	2A2-I/O	19	1A2-I/O	10	2B2-I/O	1	1B2-I/O
—	—	27	2A1-I/O	18	1A1-I/O	9	2B1-I/O	0	1B1-I/O

boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation.

The boundary-control register order of scan is illustrated in Figure 3.

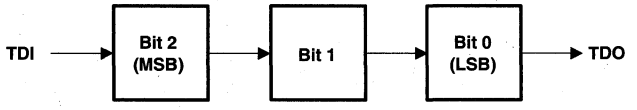


Figure 3. Boundary-Control Register Order of Scan

data register description (continued)

bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is illustrated in Figure 4.

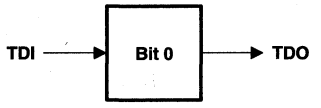


Figure 4. Bypass Register Order of Scan

device identification register

The device identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

During Capture-DR, the binary value 00000000000000000101000000101111 (0000502F, hex) is captured in the device identification register to identify this device as Texas Instruments SN54/74ABT18245, version 0.

The device identification register order of scan is from TDO through bits 31–0 to TDO. Table 2 shows the device identification register bits and their significance.

Table 2. Device Identification Register Configuration

IDR BIT NUMBER	IDENTIFICATION SIGNIFICANCE	IDR BIT NUMBER	IDENTIFICATION SIGNIFICANCE	IDR BIT NUMBER	IDENTIFICATION SIGNIFICANCE
31	VERSION3	27	PARTNUMBER15	11	MANUFACTURER10†
30	VERSION2	26	PARTNUMBER14	10	MANUFACTURER09†
29	VERSION1	25	PARTNUMBER13	9	MANUFACTURER08†
28	VERSION0	24	PARTNUMBER12	8	MANUFACTURER07†
—	—	23	PARTNUMBER11	7	MANUFACTURER06†
—	—	22	PARTNUMBER10	6	MANUFACTURER05†
—	—	21	PARTNUMBER09	5	MANUFACTURER04†
—	—	20	PARTNUMBER08	4	MANUFACTURER03†
—	—	19	PARTNUMBER07	3	MANUFACTURER02†
—	—	18	PARTNUMBER06	2	MANUFACTURER01†
—	—	17	PARTNUMBER05	1	MANUFACTURER00†
—	—	16	PARTNUMBER04	0	LOGIC1†
—	—	15	PARTNUMBER03	—	—
—	—	14	PARTNUMBER02	—	—
—	—	13	PARTNUMBER01	—	—
—	—	12	PARTNUMBER00	—	—

† Note that for TI products, bits 11–0 of the device identification register always contains the binary value 000000101111 (02F, hex).

Table 3. Instruction Register Opcodes

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	IDCODE	Identification read	Device identification	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	BYPASS‡	Bypass scan	Bypass	Normal
10000100	BYPASS‡	Bypass scan	Bypass	Normal
00000101	BYPASS‡	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS‡	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT18245.

instruction register opcode description

The instruction register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The boundary-scan register is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device I/O pins is passed through the I/O BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 43–40 of the BSR). When a given output enable is active (logic 1), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The device identification register is selected in the scan path. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The boundary-scan register is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

instruction register opcode description (continued)

bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

control boundary to high impedance

This instruction conforms to the IEEE P1149.1A HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE P1149.1A CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the boundary-control register is executed during Run-Test/Idle. The five test operations decoded by the boundary-control register are: sample inputs/toggle outputs (TOPSIP), pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

boundary read

The boundary-scan register is selected in the scan path. The value in the boundary-scan register remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The boundary-scan register is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift register and shadow latch elements of the boundary-scan register. The device operates in the normal mode.

boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

boundary-control register scan

The boundary-control register is selected in the scan path. The value in the boundary-control register remains unchanged during Capture-DR. This operation must be performed prior to a boundary run test operation in order to specify which test operation is to be executed.

Table 4. Boundary-Control Register Opcodes

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/36-bit mode (PRPG)
X10	Parallel signature analysis/36-bit mode (PSA)
011	Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT)

boundary-control register opcode description

The boundary-control register opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

In general, while the control input BSCs (bits 43–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 43–40 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when both bytes of the device are operating in one direction of data flow (that is, 1OEA ≠ 1OEB and 2OEA ≠ 2OEB) and in the same direction of data flow (that is, 1OEA = 2OEA and 1OEB = 2OEB). Otherwise, the bypass instruction is operated.

sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 illustrate the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. A seed value of all zeroes will not produce additional patterns.

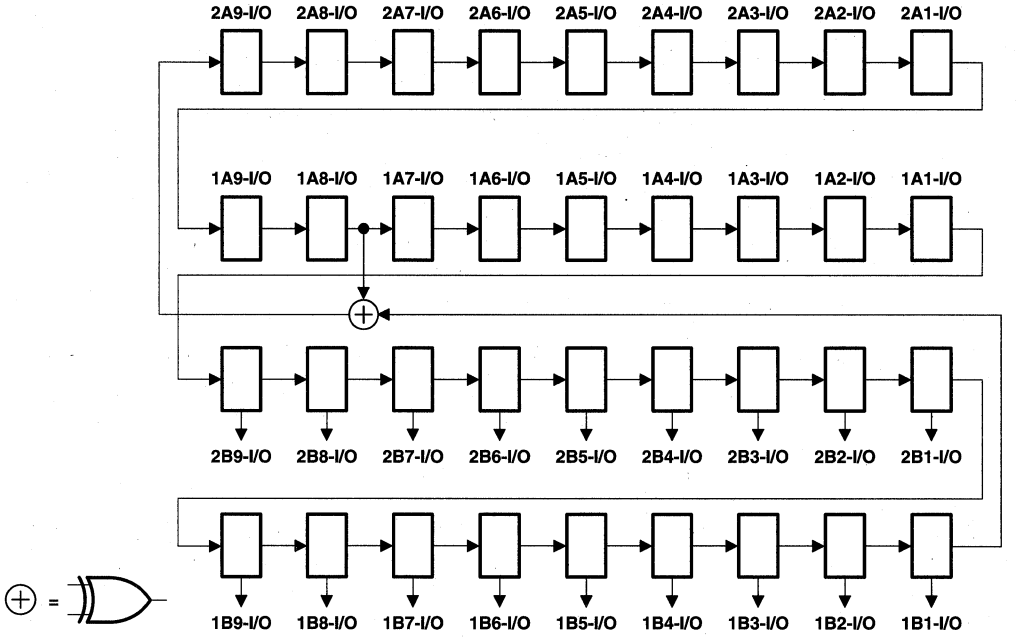


Figure 5. 36-Bit PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)

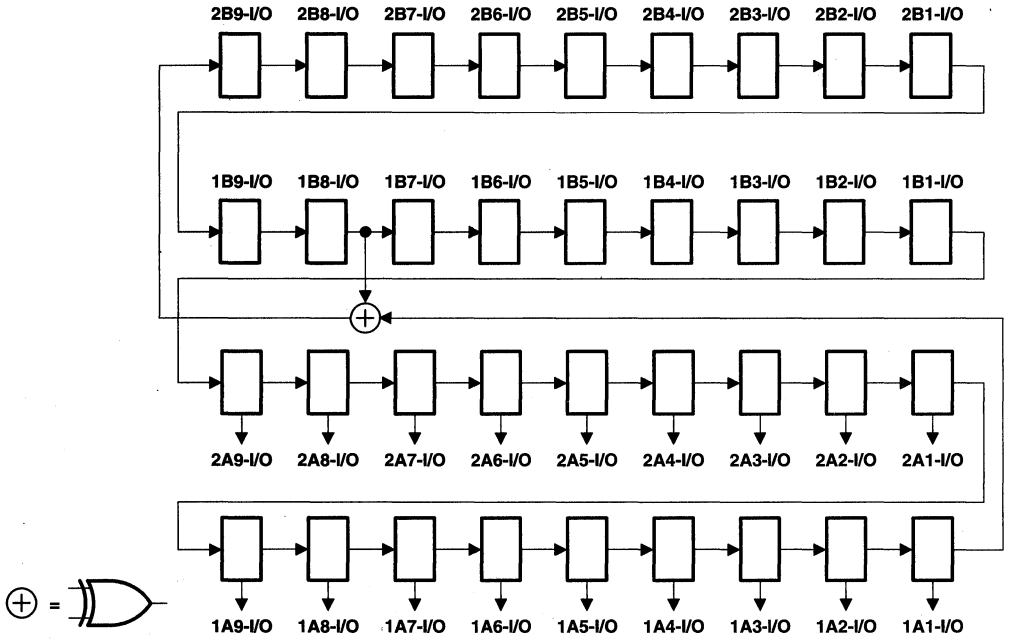


Figure 6. 36-Bit PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

boundary-control register opcode description (continued)

parallel signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 illustrate the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

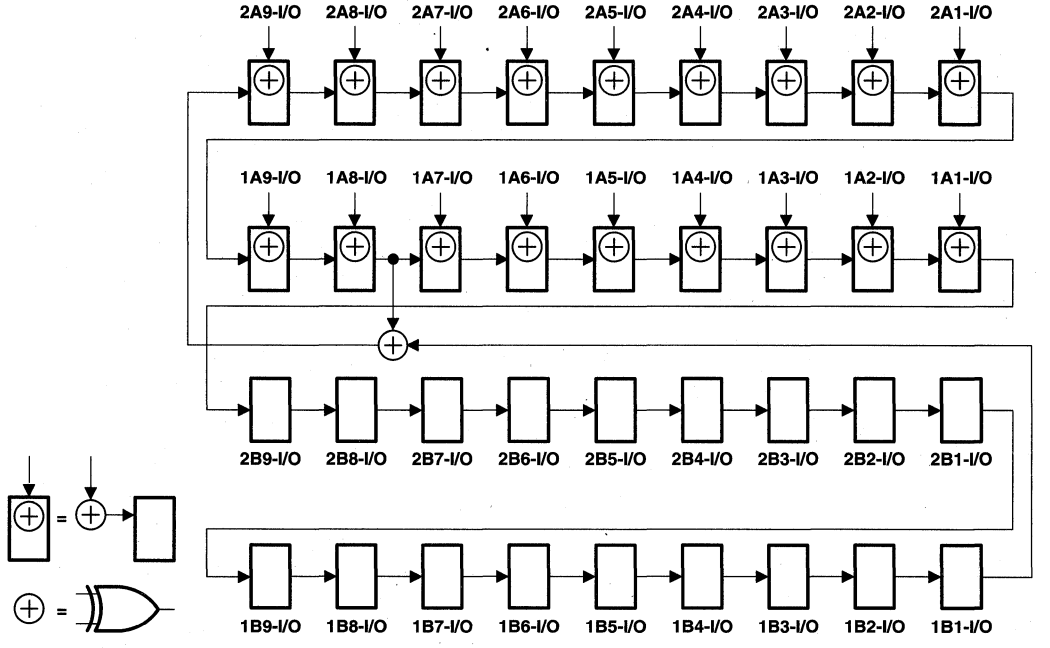


Figure 7. 36-Bit PSA Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)

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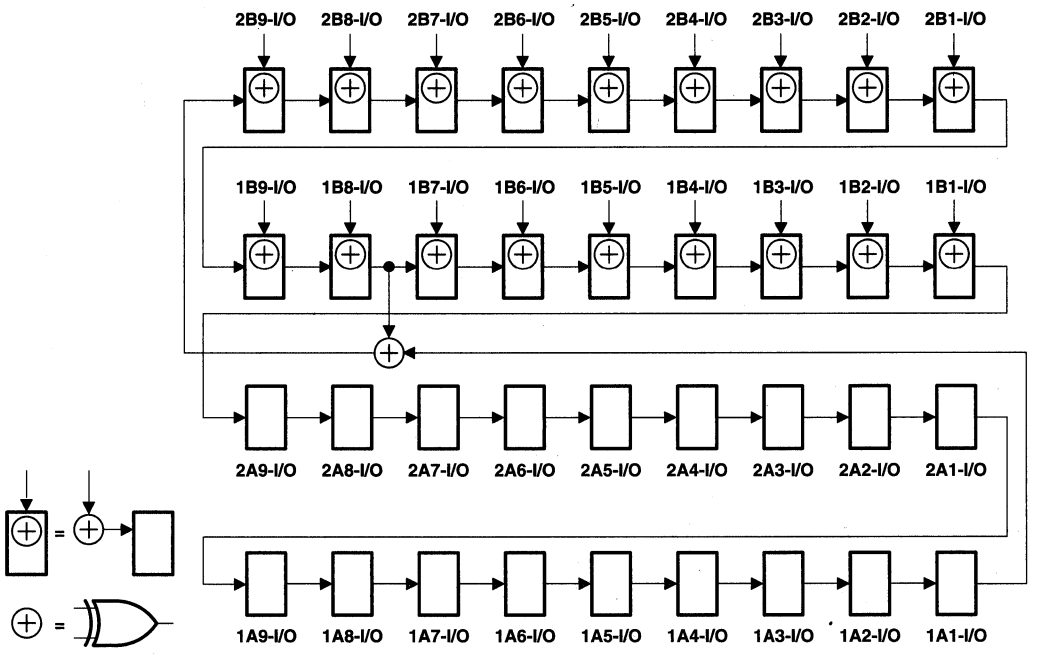

Figure 8. 36-Bit PSA Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

boundary-control register opcode description (continued)

simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. A seed value of all zeroes will not produce additional patterns.

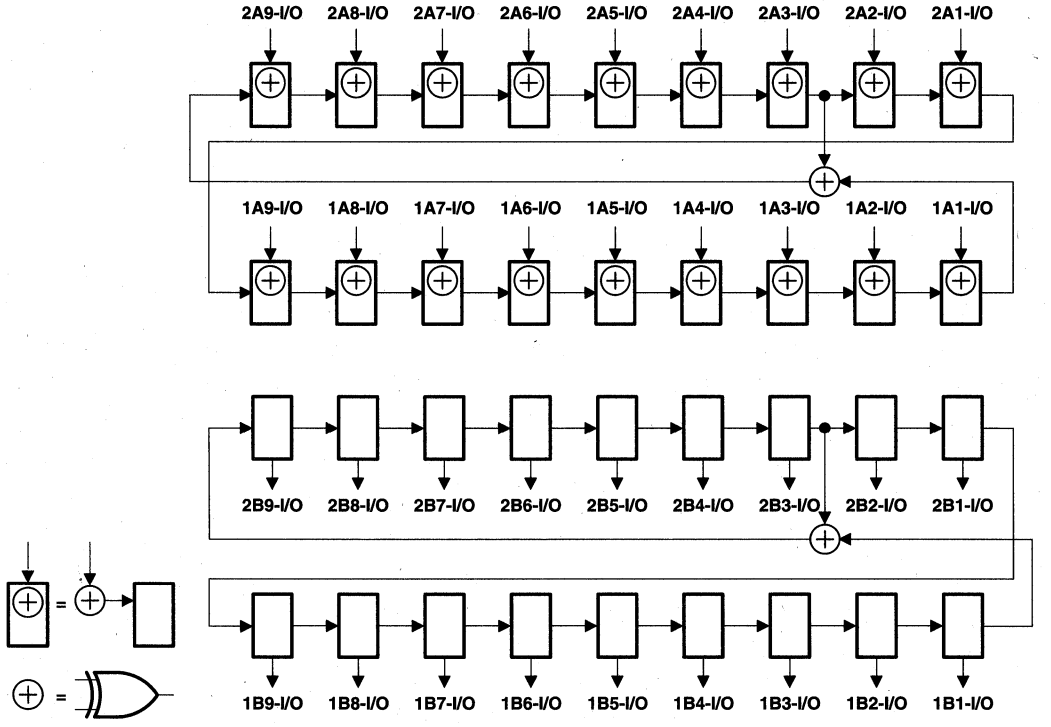

Figure 9. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)

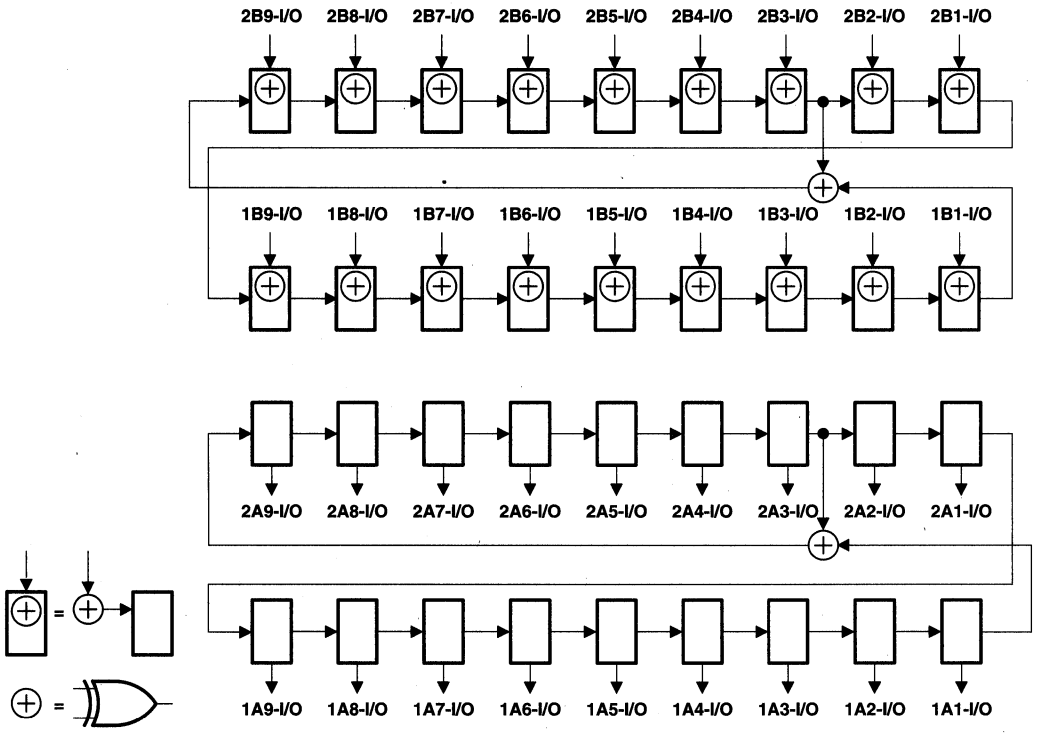

Figure 10. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

boundary-control register opcode description (continued)

simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

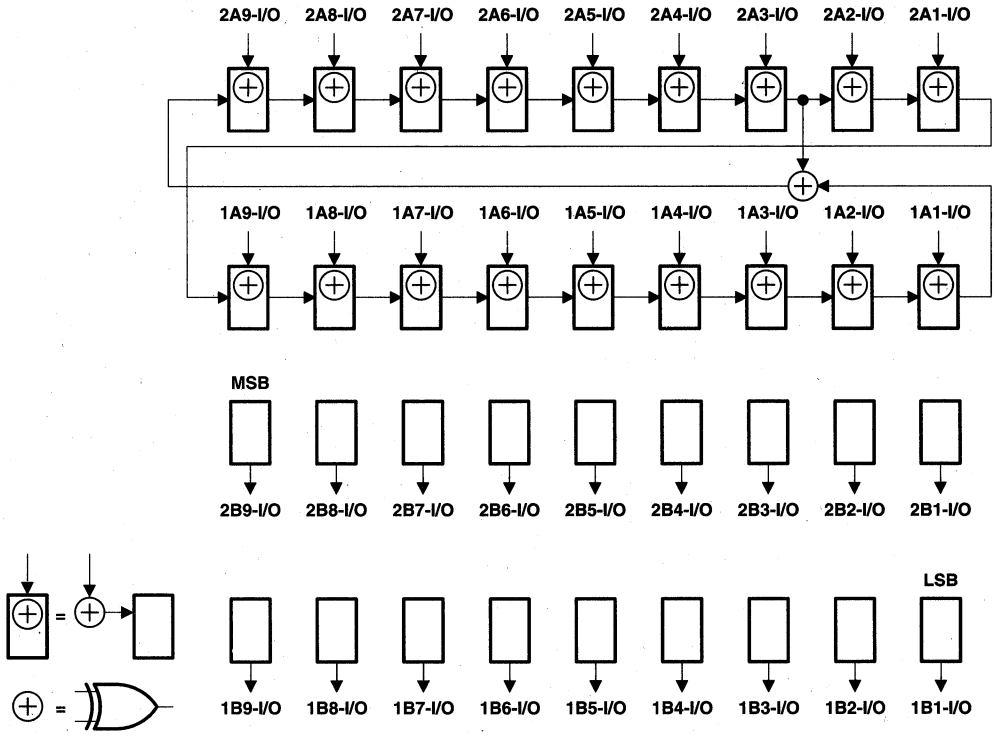

Figure 11. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)

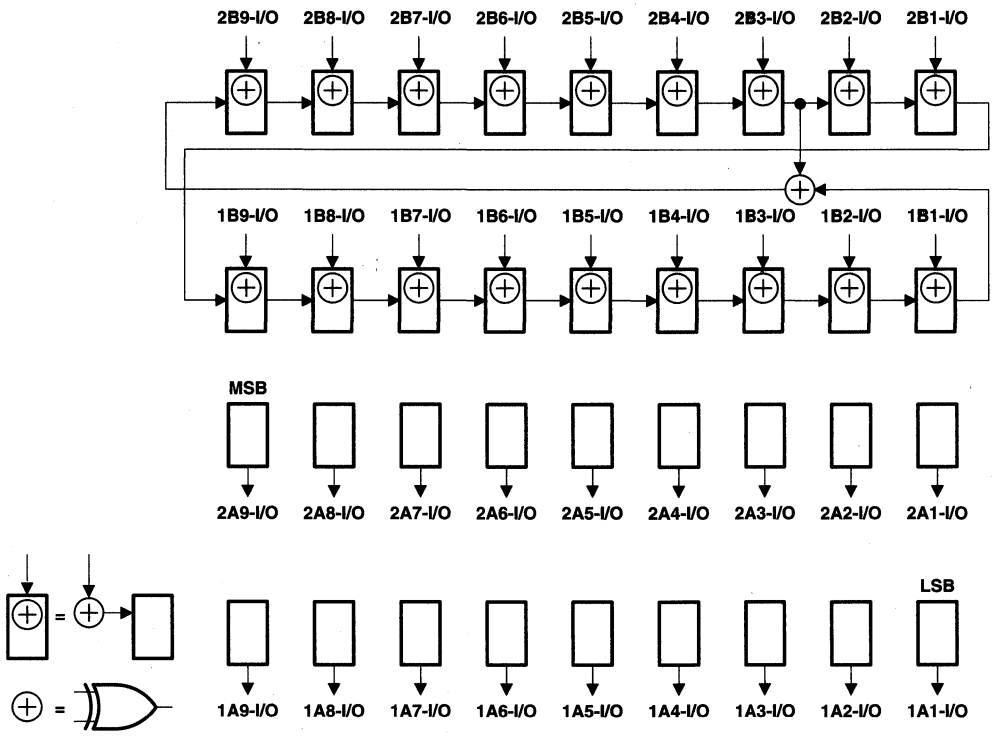

Figure 12. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

timing description

All test operations of the 'ABT18245 are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction register scan and one data register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

Table 5. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19–20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

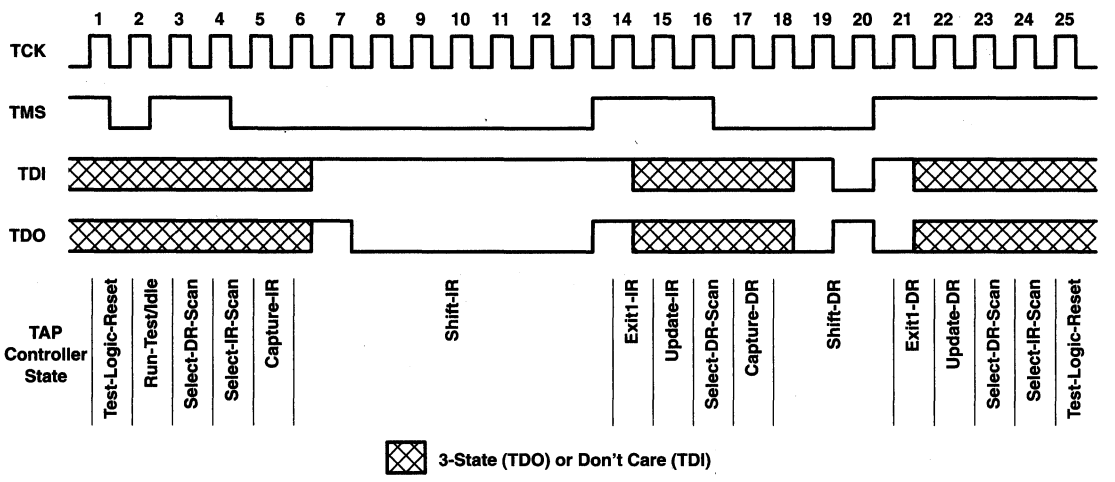

Figure 13. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1)	−0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18245	96 mA
SN74ABT18245	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Continuous current through V_{CC}	576 mA
Continuous current through GND	1152 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2)	950 mW
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18245 (DL package), the power derating factor for ambient temperatures greater than 55°C is −11.3 mW/°C.

recommended operating conditions (see Note 3)

		SN54ABT18245		SN74ABT18245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT18245		SN74ABT18245		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = −32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		DIR, $\overline{OE}$, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}		TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND		TDI, TMS			−150		−150		−150	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				−50		−50		−50	µA
I_{OZPU}	V_{CC} = 0 to 2 V, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			±50		±50		±50	µA
I_{OZPD}	V_{CC} = 2 V to 0, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			±50		±50		±50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−110	−200	−50	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		3.5	5		5		5	mA
			Outputs low		33	38		38		38	
			Outputs disabled		2.9	4.5		4.5		4.5	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

			SN54ABT18245		SN74ABT18245		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	8.1		8.1		ns
t_{su}	Setup time	A, B, DIR, or $\overline{OE}$ before TCK↑	7		7		ns
		TDI before TCK↑	4.5		4.5		
		TMS before TCK↑	3.6		3.6		
t_h	Hold time	A, B, DIR, or $\overline{OE}$ after TCK↑	0		0		ns
		TDI after TCK↑	0		0		
		TMS after TCK↑	0.5		0.5		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

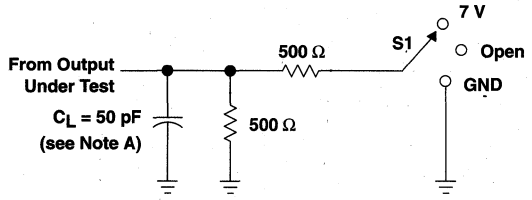
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18245		SN74ABT18245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	2.8	4.1	1.5	5.1	1.5	4.8	ns
t_{PHL}			1.5	3.1	4.6	1.5	5.8	1.5	5.4	
t_{PZH}	$\overline{OE}$	B or A	3	5.9	6.8	3	9.1	3	8.5	ns
t_{PZL}			3	6.3	7.2	3	9.5	3	9	
t_{PHZ}	$\overline{OE}$	B or A	3	7.4	8.6	3	10.4	3	9.5	ns
t_{PLZ}			3	6.6	8.6	3	10.2	3	9.5	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

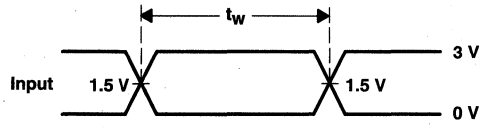
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18245		SN74ABT18245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK↓		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	3	7.1	10.1	3	14	3	13.1	ns
t_{PHL}			3	7	10.1	3	13.8	3	12.8	
t_{PLH}	TCK↓	TDO	2	3.4	5	2	6.4	2	6.1	ns
t_{PHL}			2	3.9	5.6	2	7	2	6.5	
t_{PZH}	TCK↓	A or B	4	7.5	10.6	4	14.1	4	13.4	ns
t_{PZL}			4	7.6	10.5	4	14.3	4	13.6	
t_{PZH}	TCK↓	TDO	2	3.8	5.5	2	7	2	6.6	ns
t_{PZL}			2.5	4	5.7	2.5	7.3	2.5	6.9	
t_{PHZ}	TCK↓	A or B	3.5	7.7	10.8	3.5	14.4	3.5	13.6	ns
t_{PLZ}			2.5	7.1	10.1	2.5	13.8	2.5	12.7	
t_{PHZ}	TCK↓	TDO	2	3.9	5.7	2	7.5	2	7.2	ns
t_{PLZ}			1.5	3.5	5.4	1.5	6.7	1.5	6.3	

PARAMETER MEASUREMENT INFORMATION

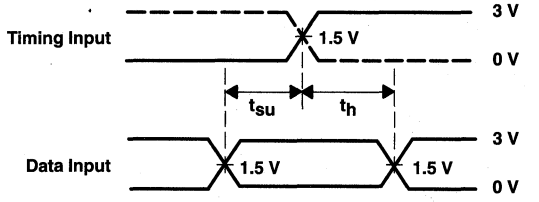


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

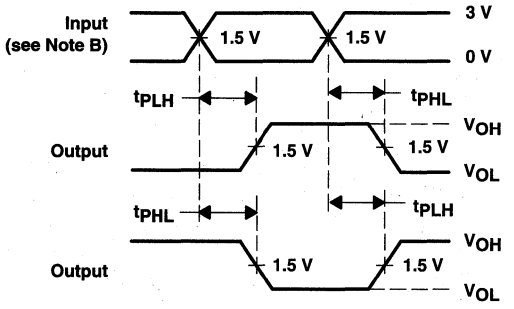
LOAD CIRCUIT FOR OUTPUTS



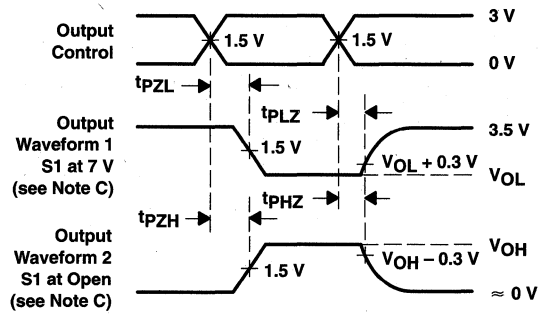
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



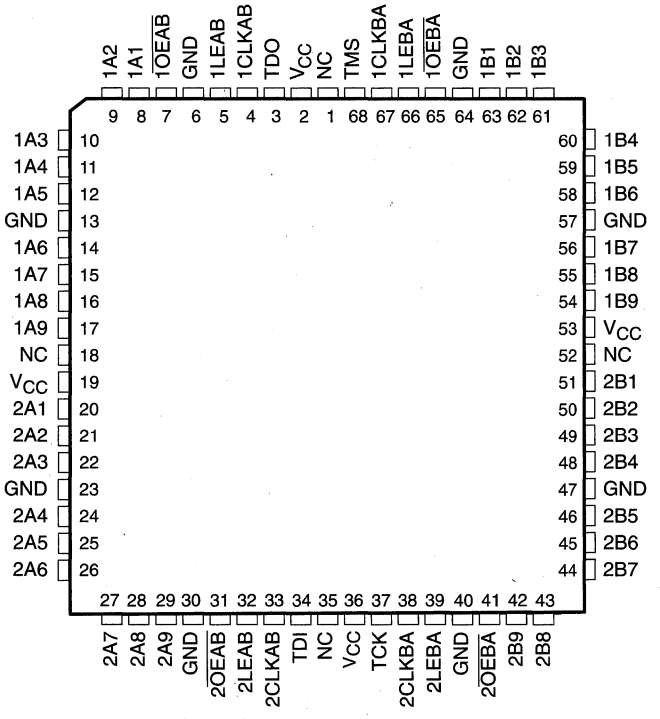
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 14. Load Circuit and Voltage Waveforms

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- One Boundary-Scan Cell per I/O Architecture Improves Scan Efficiency
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat Packages Using 25-mil Center-to-Center Spacings

SN54ABT18502A . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

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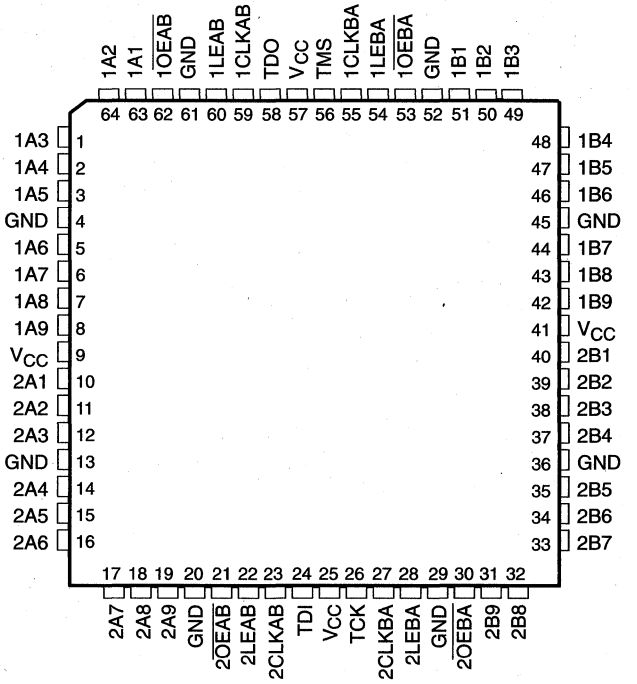
SN74ABT18502A . . . PM PACKAGE
(TOP VIEW)



description

The SN54ABT18502A and SN74ABT18502A scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

PRODUCT PREVIEW

description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Improved scan efficiency is accomplished through the adoption of a one boundary-scan cell (BSC) per I/O pin architecture. This architecture is implemented in such a way as to capture test data of most interest. A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18502A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT18502A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE† (normal mode, each register)

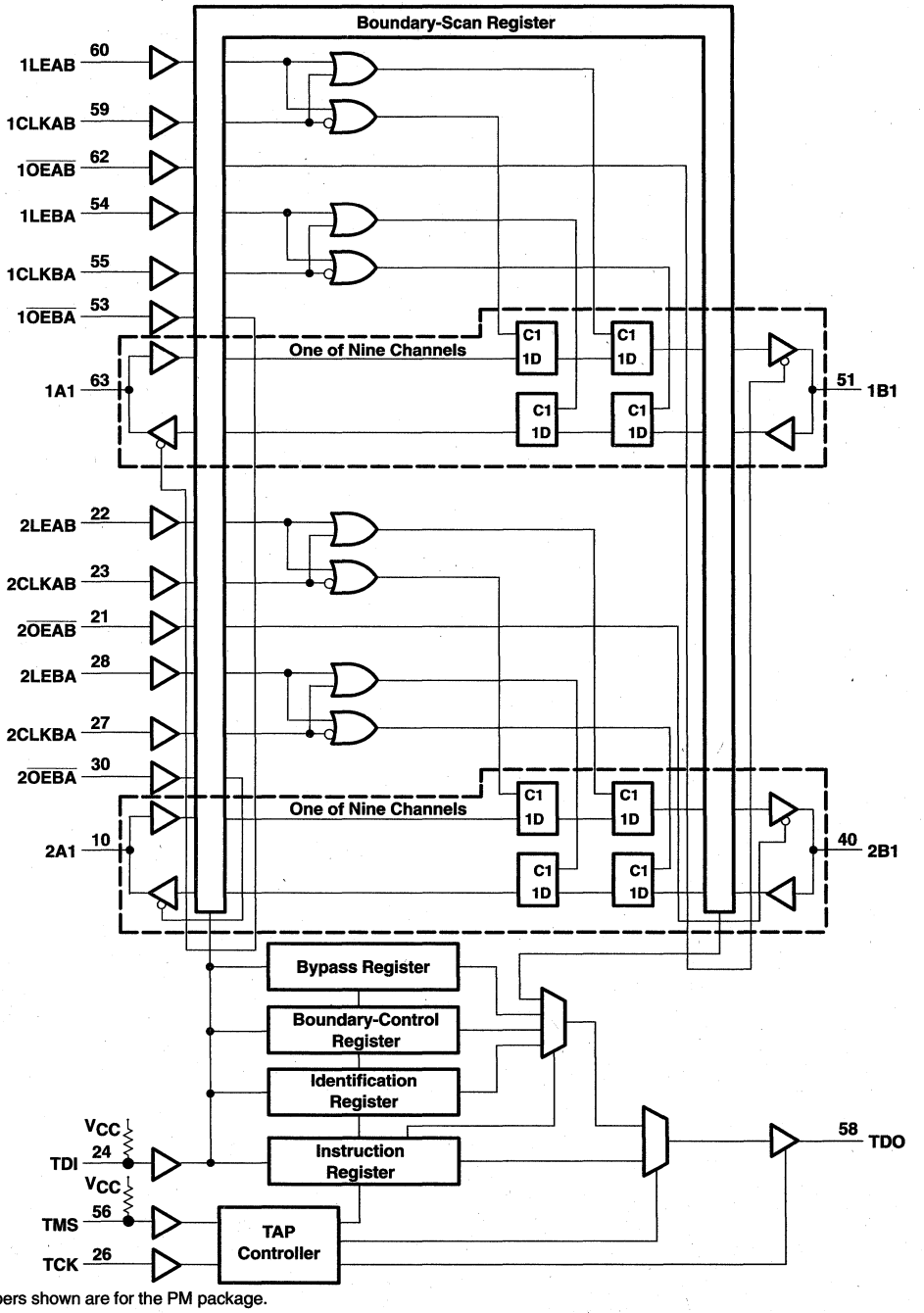
INPUTS				OUTPUT
$\overline{OEAB}$	LEAB	CLKAB	A	B
L	L	L	X	B_0‡
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

PRODUCT PREVIEW

functional block diagram



Pin numbers shown are for the PM package.

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Terminal Functions

PIN NAME	DESCRIPTION
GND	Ground
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
1LEAB, 1LEBA, 2LEAB, 2LEBA	Normal-function latch enables. See function table for normal-mode logic.
$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	Normal-function output enables. See function table for normal-mode logic.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18502A ..... 96 mA
SN74ABT18502A ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Continuous current through V_{CC} ..... 576 mA
Continuous current through GND ..... 1152 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2) ..... 885 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18502A (PM package), the power derating factor for ambient temperatures greater than 55°C is −10.5 mW/°C.

PRODUCT PREVIEW

recommended operating conditions

		SN54ABT18502A		SN74ABT18502A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT18502A		SN74ABT18502A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, LE, $\overline{OE}$, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}		TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND		TDI, TMS			–150		–150		–150	µA
$I_{I(hold)}$	V_{CC} = 4.5 V	V_I = 0.8 V	A or B ports						100		µA
		V_I = 2 V							–100		
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{OZPU}	V_{CC} = 0 to 2 V, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			±50		±50		±50	µA
I_{OZPD}	V_{CC} = 2 V to 0, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			±50		±50		±50	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–110	–200	–50	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		2	3		3		3	mA
			Outputs low		16	22		22		22	
			Outputs disabled		1	1.5		1.5		1.5	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.
† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

				SN54ABT18502A		SN74ABT18502A		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA		0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low				3.5		ns
		LEAB or LEBA high				3.5		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑				4		ns
		A before LEAB↓ or B before LEBA↓	CLK high			3.5		
			CLK low			2		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑				0		ns
		A after LEAB↓ or B after LEBA↓				2		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

			SN54ABT18502A		SN74ABT18502A		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			8		ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑			4.5		ns
		TDI before TCK↑			7.5		
		TMS before TCK↑			3		
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑			0.5		ns
		TDI after TCK↑			0.5		
		TMS after TCK↑			0.5		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18502A		SN74ABT18502A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A						2	6	ns
t_{PHL}								2	6	
t_{PLH}	CLKAB or CLKBA	B or A						2.5	6	ns
t_{PHL}								2.5	6	
t_{PLH}	LEAB or LEBA	B or A						2.5	7	ns
t_{PHL}								2.5	7	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						2	7	ns
t_{PZL}								2.5	8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						3	8.8	ns
t_{PLZ}								2.5	7.3	

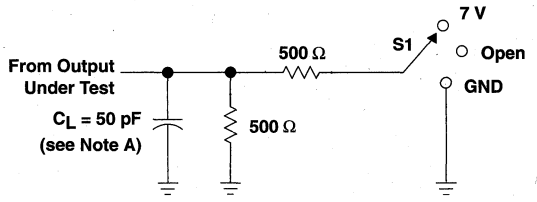
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18502A		SN74ABT18502A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						2.5	13.5	ns
t_{PHL}								2.5	12.4	
t_{PLH}	TCK↓	TDO						2	5.6	ns
t_{PHL}								2	6	
t_{PZH}	TCK↓	A or B						4.5	13.4	ns
t_{PZL}								5	14	
t_{PZH}	TCK↓	TDO						2.5	6.8	ns
t_{PZL}								3	7.5	
t_{PHZ}	TCK↓	A or B						4	16.3	ns
t_{PLZ}								3.5	15.3	
t_{PHZ}	TCK↓	TDO						3	7.6	ns
t_{PLZ}								3	7.6	

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

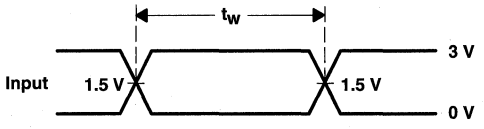
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

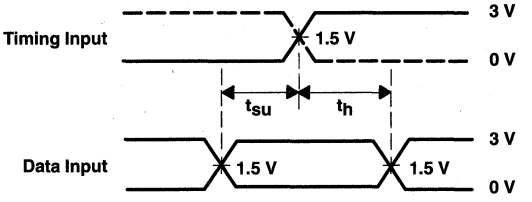


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

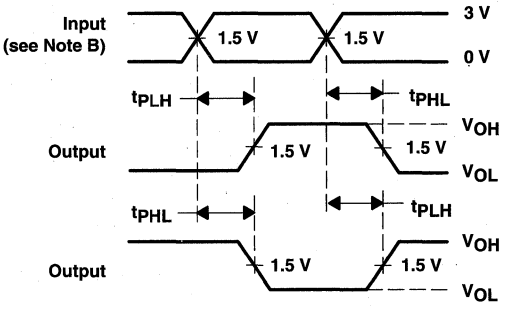
LOAD CIRCUIT FOR OUTPUTS



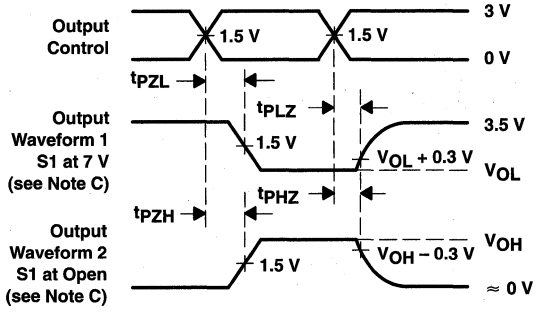
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

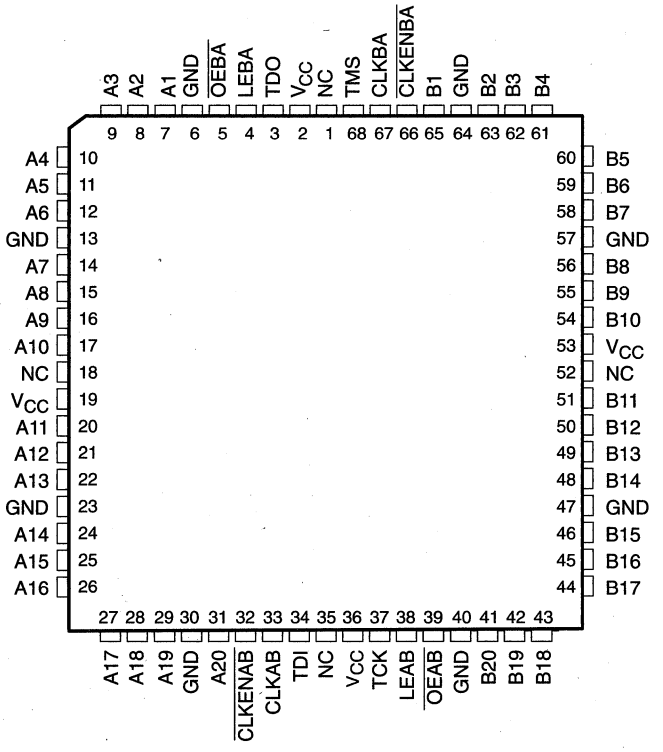
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- One Boundary-Scan Cell per I/O Architecture Improves Scan Efficiency
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat Packages Using 25-mil Center-to-Center Spacings

SN54ABT18504A . . . HV PACKAGE
(TOP VIEW)

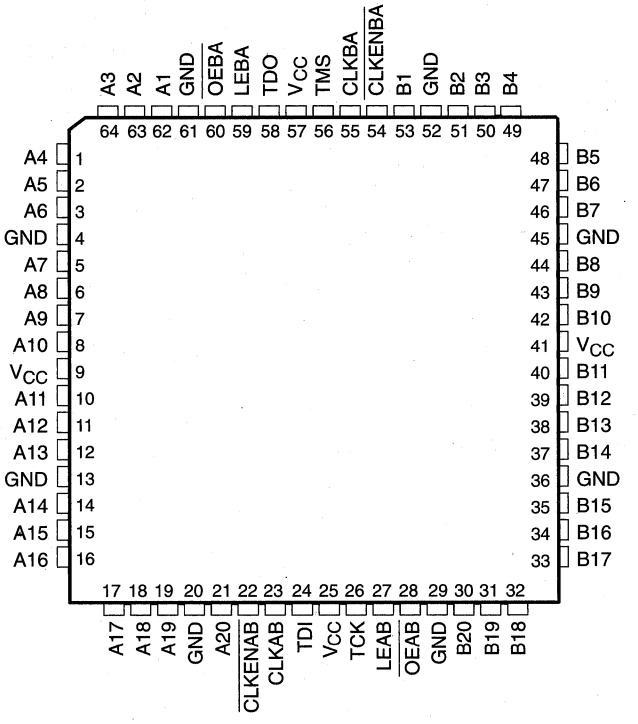


NC – No internal connection

PRODUCT PREVIEW

SCOPE, Widebus, UBT, and EPIC-IIB are trademarks of Texas Instruments Incorporated.

SN74ABT18504A . . . PM PACKAGE
(TOP VIEW)



description

The SN54ABT18504A and SN74ABT18504A scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while $\overline{CLKENAB}$ is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and $\overline{CLKENAB}$ is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

PRODUCT PREVIEW

description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Improved scan efficiency is accomplished through the adoption of a one boundary-scan cell (BSC) per I/O pin architecture. This architecture is implemented in such a way as to capture test data of most interest. A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18504A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT18504A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE† (normal mode, each register)

INPUTS					OUTPUT
$\overline{OEAB}$	LEAB	$\overline{CLKENAB}$	CLKAB	A	B
L	L	L	L	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	H	X	X	B_0‡
L	H	X	X	L	L
L	H	X	X	H	H
H	X	X	X	X	Z

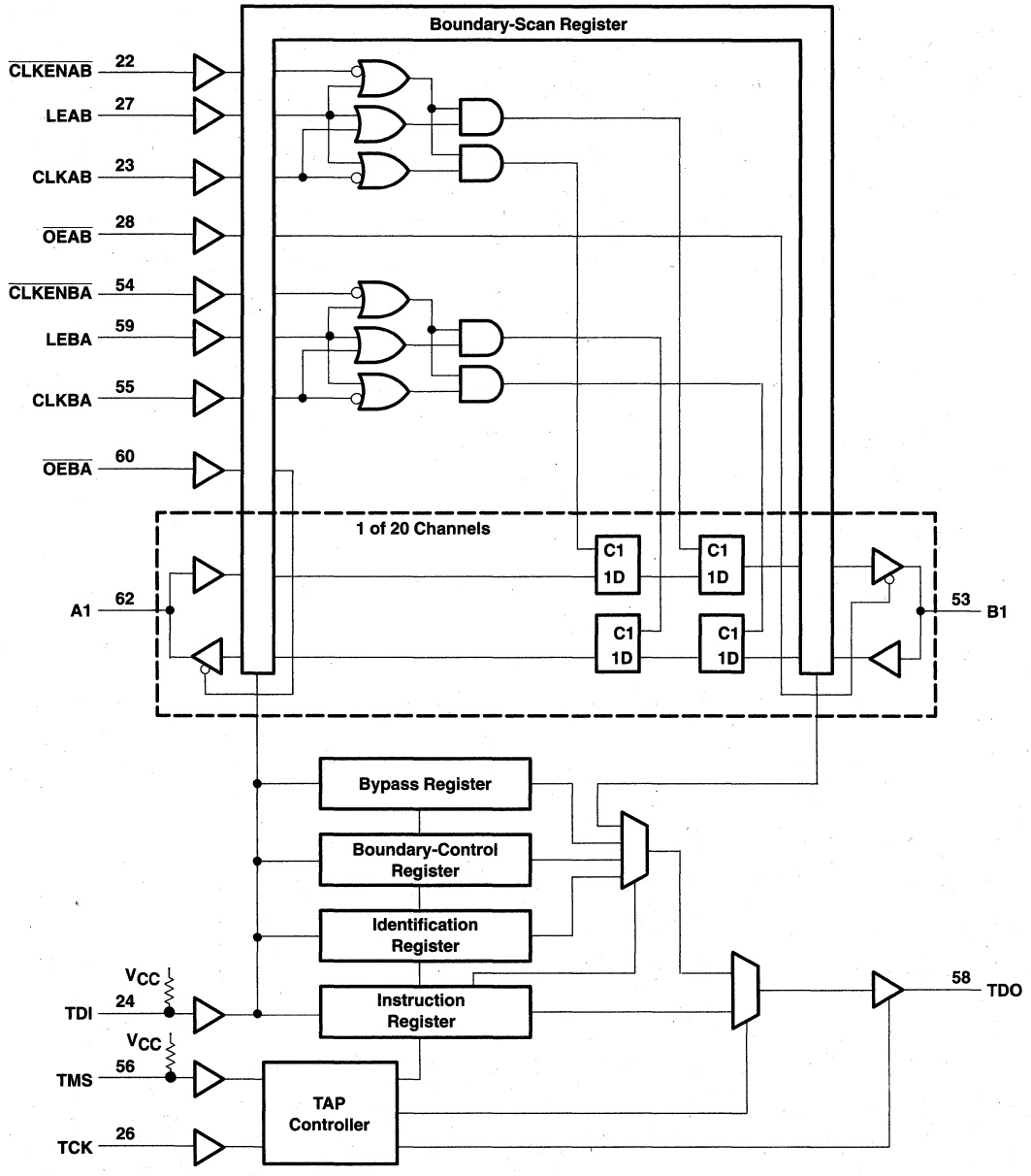
† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

PRODUCT PREVIEW

functional block diagram



Pin numbers shown are for the PM package.

Terminal Functions

PIN NAME	DESCRIPTION
A1–A20	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1–B20	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
$\overline{\text{CLKENAB}}$, $\overline{\text{CLKENBA}}$	Normal-function clock enables. See function table for normal-mode logic.
GND	Ground
LEAB, LEBA	Normal-function latch enables. See function table for normal-mode logic.
$\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18504A ..... 96 mA
SN74ABT18504A ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Continuous current through V_{CC} ..... 576 mA
Continuous current through GND ..... 1152 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) ..... 885 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18504A (PM package), the power derating factor for ambient temperatures greater than 55°C is −10.5 mW/°C.

PRODUCT PREVIEW

recommended operating conditions

		SN54ABT18504A		SN74ABT18504A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT18504A		SN74ABT18504A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, $\overline{CLKEN}$, LE, $\overline{OE}$, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}		TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND		TDI, TMS			–150		–150		–150	µA
$I_{I(hold)}$	V_{CC} = 4.5 V	V_I = 0.8 V	A or B ports						100		µA
		V_I = 2 V							–100		
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{OZPU}	V_{CC} = 0 to 2 V, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			±50		±50		±50	µA
I_{OZPD}	V_{CC} = 2 V to 0, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			±50		±50		±50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \leq$ 4.5 V					±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–110	–200	–50	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		2	3		3		3	mA
			Outputs low		18	24		24		24	
			Outputs disabled		1	1.5		1.5		1.5	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.
† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

				SN54ABT18504A		SN74ABT18504A		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA		0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low				4		ns
		LEAB or LEBA	CLK high or low			3.5		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑				4		ns
		A before LEAB↓ or B before LEBA↓	CLK high			3.5		
			CLK low			2		
		$\overline{CLKEN}$ before CLK↑				4		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑				0		ns
		A after LEAB↓ or B after LEBA↓	CLK high or low			2		
		$\overline{CLKEN}$ after CLK↑				0		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

			SN54ABT18504A		SN74ABT18504A		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			8		ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑			4.5		ns
		TDI before TCK↑			7.5		
		TMS before TCK↑			3		
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑			0.5		ns
		TDI after TCK↑			0.5		
		TMS after TCK↑			0.5		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18504A		SN74ABT18504A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A						2	6	ns
t_{PHL}								2	6.5	
t_{PLH}	CLKAB or CLKBA	B or A						2.5	6.8	ns
t_{PHL}								2.5	6.5	
t_{PLH}	LEAB or LEBA	B or A						2.5	7.1	ns
t_{PHL}								2.5	7.2	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						2	7	ns
t_{PZL}								2.5	8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						3	8.8	ns
t_{PLZ}								2.5	7.3	

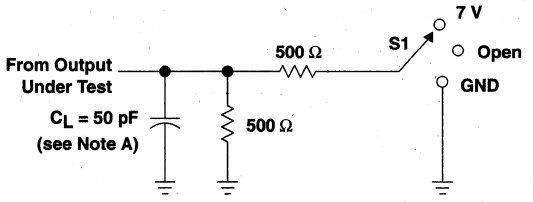
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18504A		SN74ABT18504A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						2.5	13.5	ns
t_{PHL}								2.5	12.5	
t_{PLH}	TCK↓	TDO						2	5.6	ns
t_{PHL}								2	6.5	
t_{PZH}	TCK↓	A or B						4.5	13.8	ns
t_{PZL}								5	14.5	
t_{PZH}	TCK↓	TDO						2	7	ns
t_{PZL}								3	7.5	
t_{PHZ}	TCK↓	A or B						4	17	ns
t_{PLZ}								3.5	16	
t_{PHZ}	TCK↓	TDO						3	7.5	ns
t_{PLZ}								3	7.5	

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

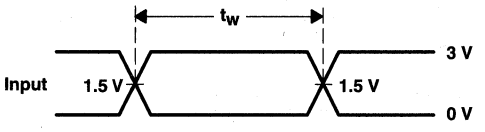
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

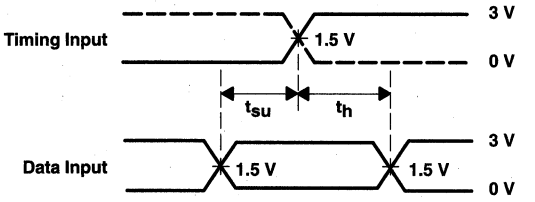


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

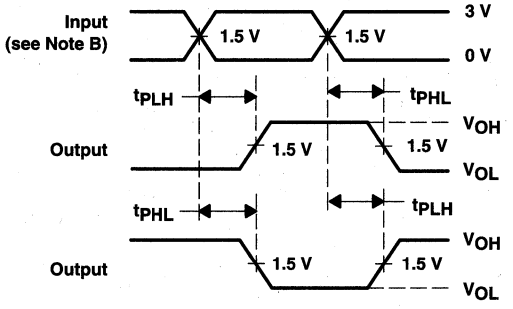
LOAD CIRCUIT FOR OUTPUTS



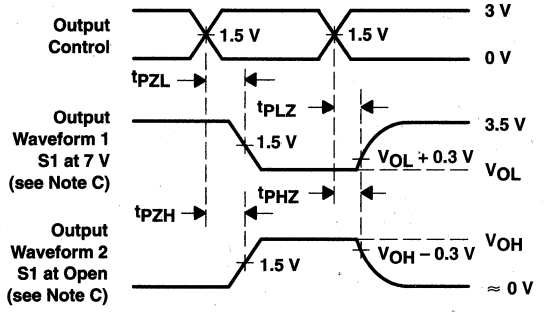
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

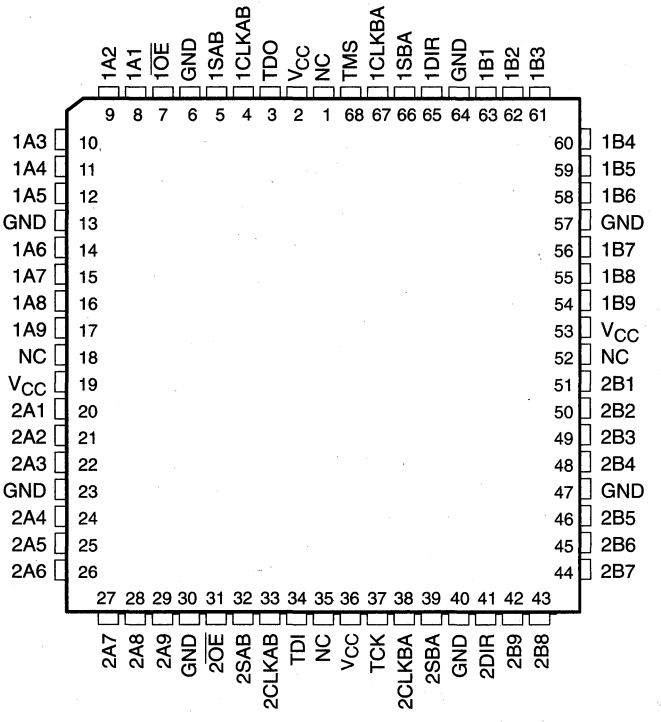
SN54ABT18646A, SN74ABT18646A
SCAN TEST DEVICES WITH 18-BIT TRANSCEIVERS AND REGISTERS

SCBS166 – AUGUST 1993

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- One Boundary-Scan Cell per I/O Architecture Improves Scan Efficiency
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat Packages Using 25-mil Center-to-Center Spacings

PRODUCT PREVIEW

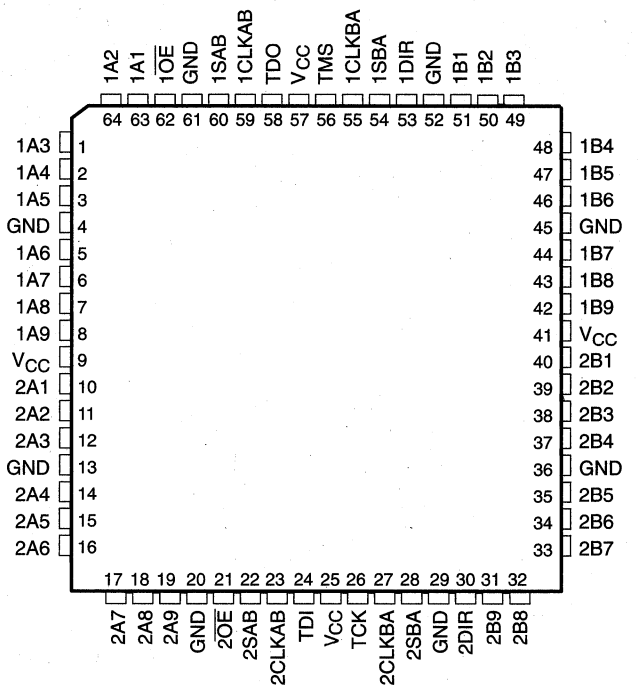
SN54ABT18646A . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

SCOPE, Widebus, and EPIC-IIB are trademarks of Texas Instruments Incorporated.

SN74ABT18646A . . . PM PACKAGE
(TOP VIEW)



description

The SN54ABT18646A and SN74ABT18646A scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Transceiver function is controlled by output-enable ($\overline{OE}$) and direction (DIR) inputs. When $\overline{OE}$ is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When $\overline{OE}$ is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′ABT18646A.

PRODUCT PREVIEW

description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Improved scan efficiency is accomplished through the adoption of a one boundary-scan cell (BSC) per I/O pin architecture. This architecture is implemented in such a way as to capture test data of most interest. A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

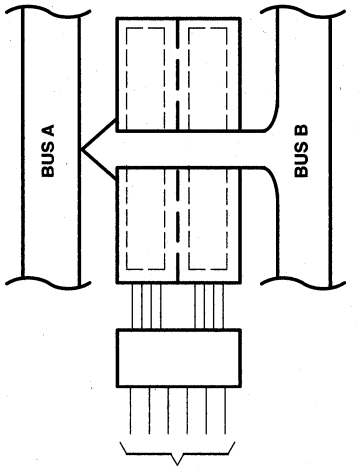
The SN54ABT18646A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT18646A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A9	B1 THRU B9	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input disabled	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input disabled	Output	Stored A data to B bus

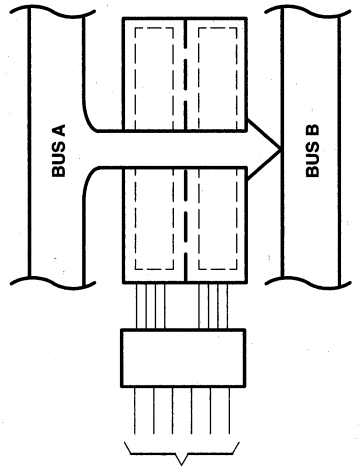
† The data output functions can be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

PRODUCT PREVIEW



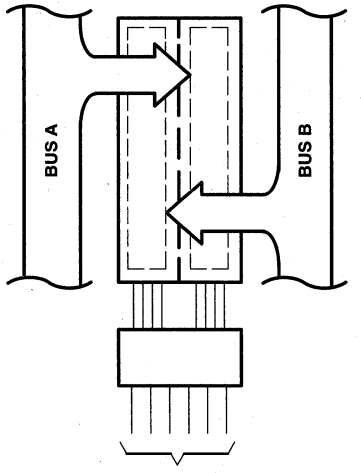
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



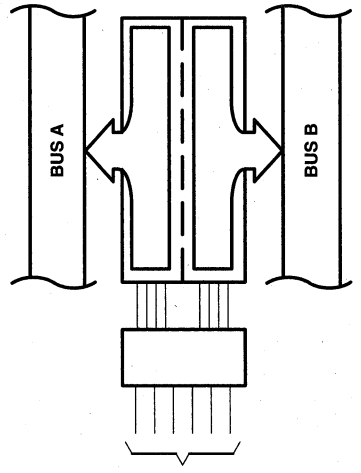
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

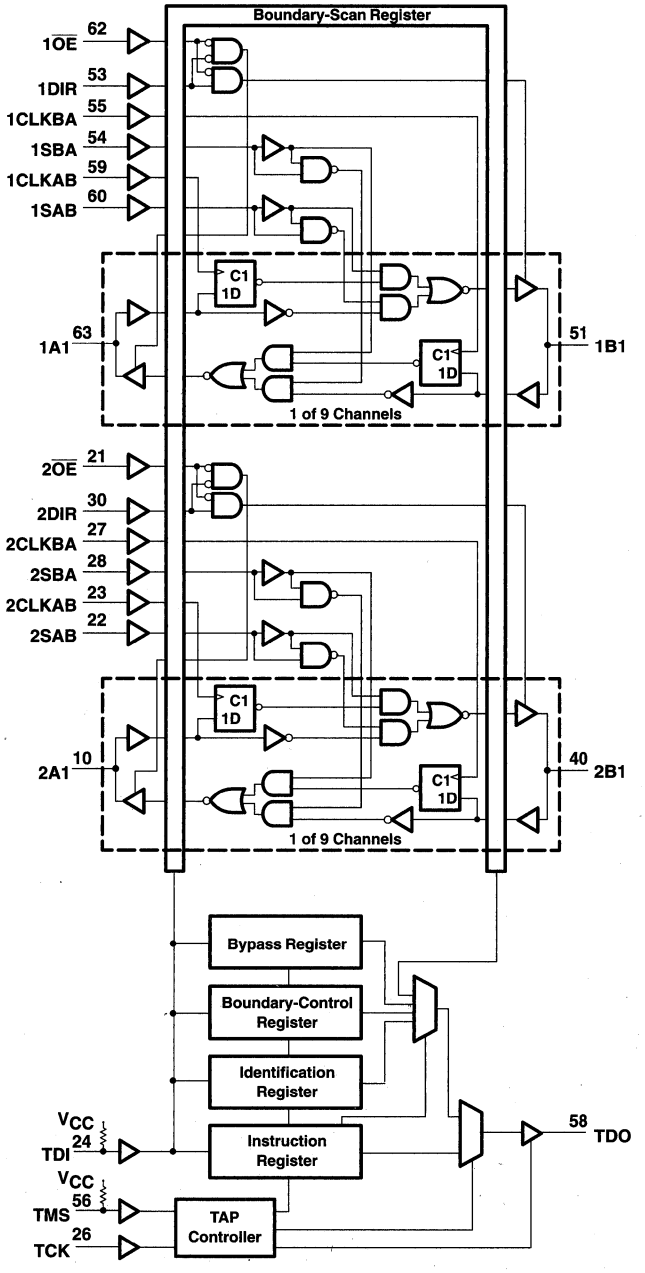


$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

functional block diagram



Pin numbers shown are for the PM package.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18646A ..... 96 mA
SN74ABT18646A ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum package power dissipation at $T_A = 55°C$ (in still air) (see Note 2) ..... 885 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18646A (PM package), the power derating factor for ambient temperatures greater than 55°C is −10.5 mW/°C.

recommended operating conditions

		SN54ABT18646A		SN74ABT18646A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT18646A		SN74ABT18646A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, DIR, $\overline{OE}$, S, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}		TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND		TDI, TMS			–150		–150		–150	µA
$I_{I(hold)}$	V_{CC} = 4.5 V	V_I = 0.8 V	A or B ports						100		µA
		V_I = 2 V							–100		
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{OZPU}	V_{CC} = 0 to 2 V, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			± 50		± 50		± 50	µA
I_{OZPD}	V_{CC} = 0 to 2 V, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			± 50		± 50		± 50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \leq$ 4.5 V					±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–110	–200	–50	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		2	3		3		3	mA
			Outputs low		16	22		22		22	
			Outputs disabled		1	1.5		1.5		1.5	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.
† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 2)

			SN54ABT18646A		SN74ABT18646A		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low			4		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑			4.5		ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑			0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 2)

			SN54ABT18646A		SN74ABT18646A		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			8		ns
t_{su}	Setup time	A, B, CLK, DIR, $\overline{OE}$, or S before TCK↑			4.5		ns
		TDI before TCK↑			7.5		
		TMS before TCK↑			4		
t_h	Hold time	A, B, CLK, DIR, $\overline{OE}$, or S after TCK↑			0.5		ns
		TDI after TCK↑			0.5		
		TMS after TCK↑			0.5		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

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PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18646A		SN74ABT18646A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A						2	5.4	ns
t_{PHL}								2	6.6	
t_{PLH}	CLKAB or CLKBA	B or A						2.5	8	ns
t_{PHL}								2.5	7.4	
t_{PLH}	SAB or SBA	B or A						2	7.5	ns
t_{PHL}								2	8	
t_{PZH}	DIR	B or A						2	8	ns
t_{PZL}								3	9.1	
t_{PZH}	$\overline{OE}$	B or A						2.5	8.6	ns
t_{PZL}								3	9.3	
t_{PHZ}	DIR	B or A						3.5	11.1	ns
t_{PLZ}								3	8.8	
t_{PHZ}	$\overline{OE}$	B or A						3.5	10.5	ns
t_{PLZ}								2	8.5	

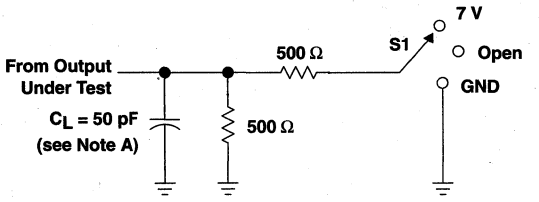
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18646A		SN74ABT18646A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						2.5	13.5	ns
t_{PHL}								2.5	12.5	
t_{PLH}	TCK↓	TDO						2	6.5	ns
t_{PHL}								2	6.5	
t_{PZH}	TCK↓	A or B						4.5	13.8	ns
t_{PZL}								5	14.5	
t_{PZH}	TCK↓	TDO						2	7	ns
t_{PZL}								3	7.5	
t_{PHZ}	TCK↓	A or B						4	17	ns
t_{PLZ}								3	16	
t_{PHZ}	TCK↓	TDO						3	9	ns
t_{PLZ}								3	7.5	

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

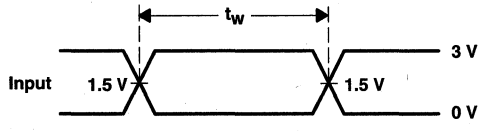
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

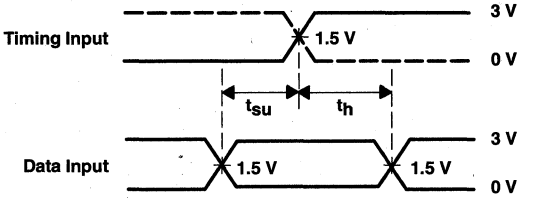


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

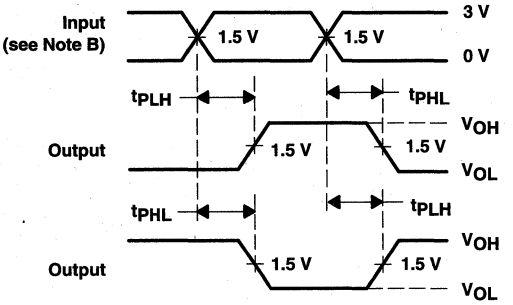
LOAD CIRCUIT FOR OUTPUTS



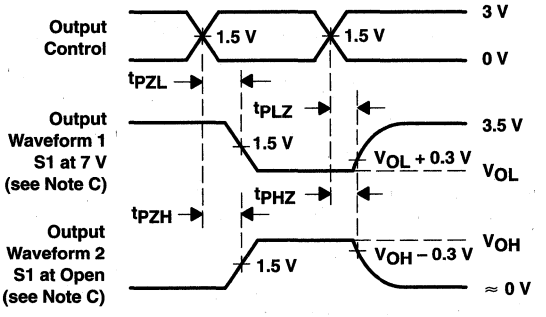
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

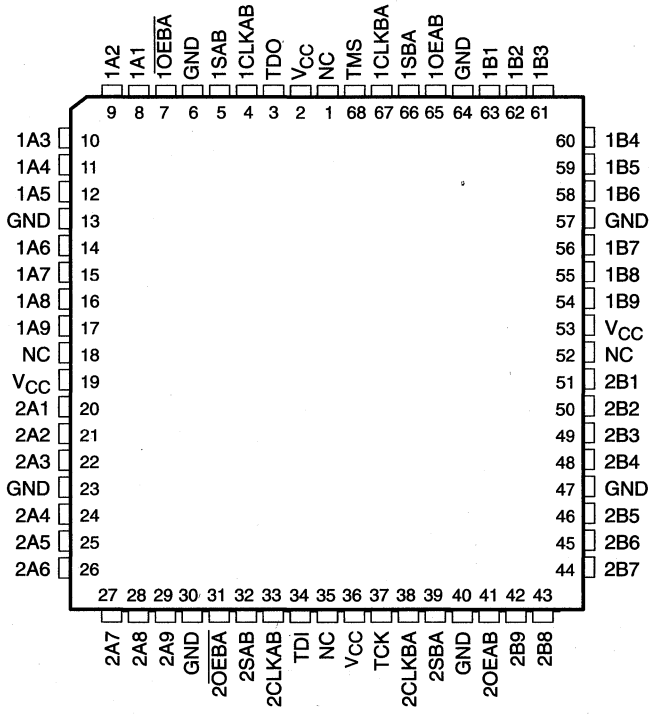
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation
- One Boundary-Scan Cell per I/O Architecture Improves Scan Efficiency
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat Packages Using 25-mil Center-to-Center Spacings

SN54ABT18652A . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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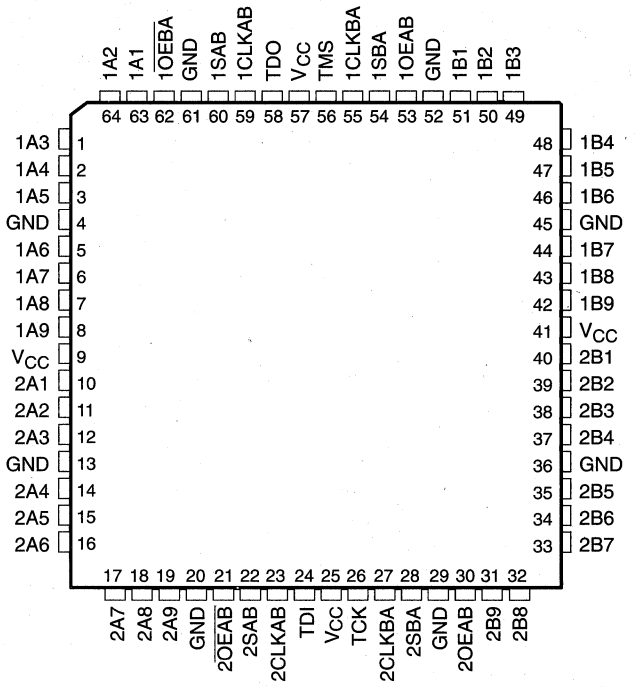
SN74ABT18652A . . . PM PACKAGE
(TOP VIEW)



description

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In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and $\overline{\text{OEBA}}$ inputs. Since the $\overline{\text{OEBA}}$ input is active-low, the A outputs are active when $\overline{\text{OEBA}}$ is low and are in the high-impedance state when $\overline{\text{OEBA}}$ is high. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT18652A.

PRODUCT PREVIEW

description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Improved scan efficiency is accomplished through the adoption of a one boundary-scan cell (BSC) per I/O pin architecture. This architecture is implemented in such a way as to capture test data of most interest. A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

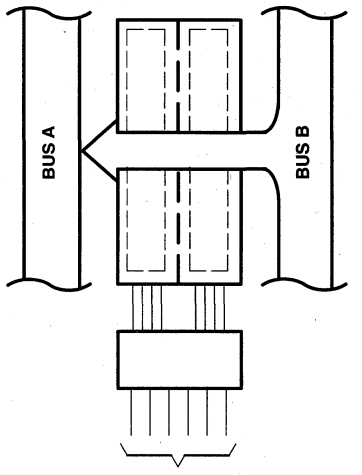
The SN54ABT18652A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT18652A is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A9	B1 THRU B9	
L	H	L	L	X	X	Input disabled	Input disabled	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified†	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified†	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

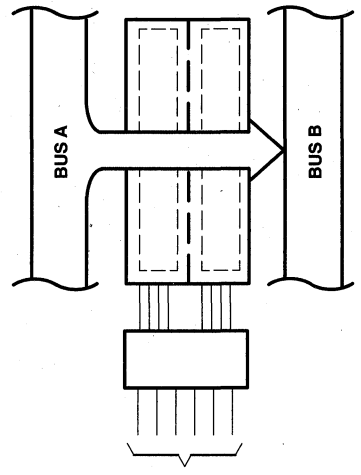
† The data output functions can be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

PRODUCT PREVIEW



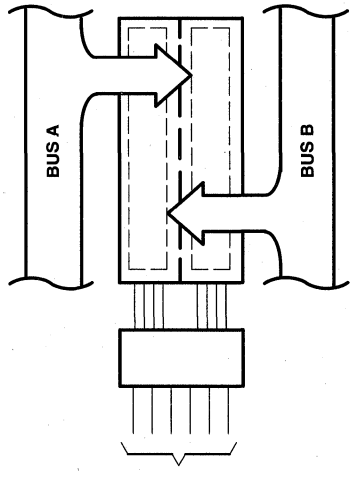
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



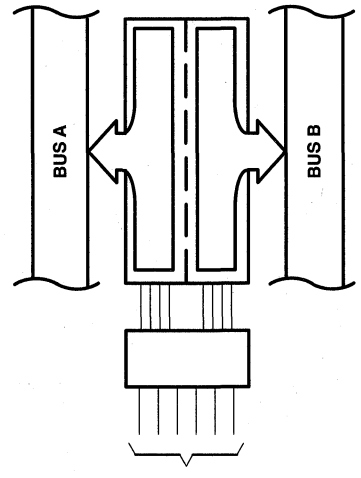
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

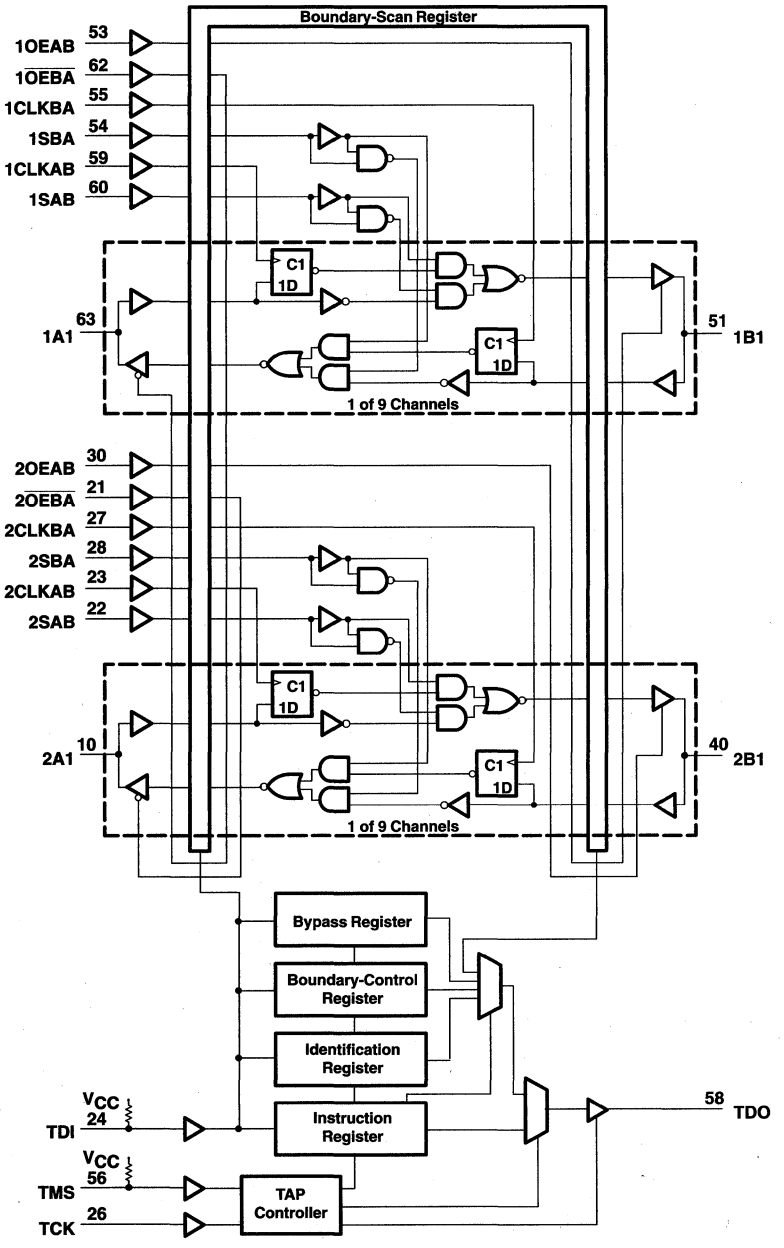


OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

functional block diagram



Pin numbers shown are for the PM package.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18652A ..... 96 mA
SN74ABT18652A ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum package power dissipation at $T_A = 55°C$ (in still air) (see Note 2) ..... 885 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18652A (PM package), the power derating factor for ambient temperatures greater than 55°C is −10.5 mW/°C.

recommended operating conditions

		SN54ABT18652A		SN74ABT18652A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT18652A		SN74ABT18652A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = –3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = –3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = –24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = –32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, OEAB, $\overline{OEBA}$, S, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}		TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND		TDI, TMS			–150		–150		–150	µA
$I_{I(hold)}$	V_{CC} = 4.5 V	V_I = 0.8 V	A or B ports						100		µA
		V_I = 2 V							–100		
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{OZPU}	V_{CC} = 0 to 2 V, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			± 50		± 50		± 50	µA
I_{OZPD}	V_{CC} = 0 to 2 V, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			± 50		± 50		± 50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V					±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–110	–200	–50	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		2	3		3		3	mA
			Outputs low		16	22		22		22	
			Outputs disabled		1	1.5		1.5		1.5	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.
† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 2)

			SN54ABT18652A		SN74ABT18652A		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low			4		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑			4.5		ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑			0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 2)

			SN54ABT18652A		SN74ABT18652A		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			8		ns
t_{su}	Setup time	A, B, CLK, OEAB, $\overline{OEBA}$, or S before TCK↑			4.5		ns
		TDI before TCK↑			7.5		
		TMS before TCK↑			4		
t_h	Hold time	A, B, CLK, OEAB, $\overline{OEBA}$, or S after TCK↑			0.5		ns
		TDI after TCK↑			0.5		
		TMS after TCK↑			0.5		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18652A		SN74ABT18652A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A						2	5.4	ns
t_{PHL}								2	6.6	
t_{PLH}	CLKAB or CLKBA	B or A						2.5	8	ns
t_{PHL}								2.5	7.4	
t_{PLH}	SAB or SBA	B or A						2	7.5	ns
t_{PHL}								2	8	
t_{PZH}	OEAB or $\overline{OEBA}$	B or A						2.5	8.6	ns
t_{PZL}								3	9.3	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A						3.5	10.5	ns
t_{PLZ}								2	8.5	

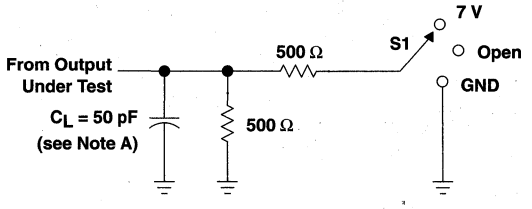
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18652A		SN74ABT18652A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						2.5	13.5	ns
t_{PHL}								2.5	12.5	
t_{PLH}	TCK↓	TDO						2	6.5	ns
t_{PHL}								2	6.5	
t_{PZH}	TCK↓	A or B						4.5	13.8	ns
t_{PZL}								5	14.5	
t_{PZH}	TCK↓	TDO						2	7	ns
t_{PZL}								3	7.5	
t_{PHZ}	TCK↓	A or B						4	17	ns
t_{PLZ}								3	16	
t_{PHZ}	TCK↓	TDO						3	9	ns
t_{PLZ}								3	7.5	

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

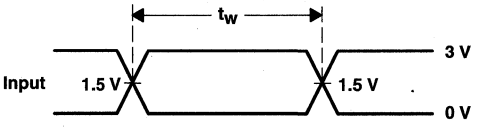
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

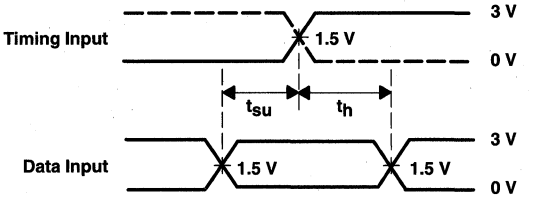


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

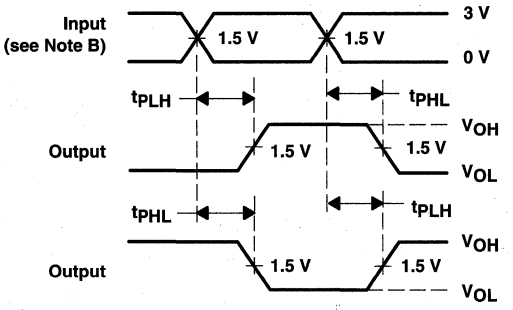
LOAD CIRCUIT FOR OUTPUTS



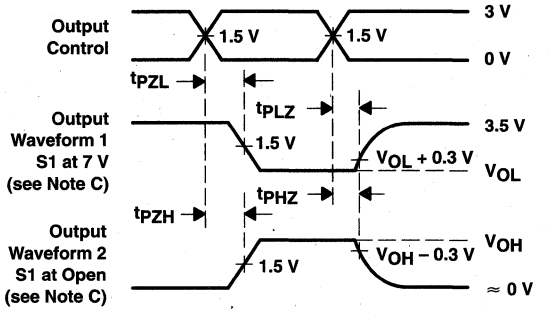
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

LVT JTAG/IEEE 1149.1

Features

- Compatibility with IEEE Standard 1149.1-1990 (JTAG) test access port (TAP) and boundary-scan architecture
- EPIC-IIB™ BiCMOS process with special low-voltage enhancements
- EIAJ TSSOP, JEDEC SSOP, and EIAJ TQFP fine-pitch surface-mount packaging
- Bus-hold circuitry
- 18- and 20-bit UBT™ architectures
- Additional SCOPE™ instructions available such as:
  - Parallel Signature Analysis (PSA)
  - Pseudo-Random Pattern Generation (PRPG)
- Test-mode or normal-mode operation
- Expanded V_{CC} range from 2.7 V to 3.6 V
- Members of the Texas Instruments SCOPE™ family of testability products
- TI has established an alternate source

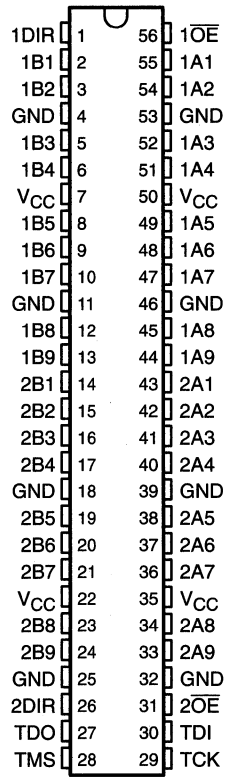
Benefits

- Facilitate testing of complex circuit board assemblies via a 4-wire test access port
- 3.3-V logic family with equivalent drive performance of 5-V ABT logic family – not just a recharacterized, scaled CMOS
- Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
- No system throughput or cycle time penalty for boundary-scan implementation
- Functional equivalents to standard ABT devices offer system and test designers flexible integration options
- Save valuable board space
- Reduce component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Advanced integration, as one UBT™ can replace nearly all common bus-interface logic
- Built-in self-test feature allows easy upgrade for advanced JTAG test applications
- IEEE Standard 1149.1-1990 protocol can be bypassed for applications not requiring boundary scan
- Compatible with complete line of system-level test products including controllers, bus monitors, scan path linkers, scan path selectors, application-specific products, and very large-scale integration products
- Standardization that comes from a common product approach

Information regarding the tap control state diagram, signal descriptions, and other related JTAG/IEEE 1149.1 information for the 'LVT18245, 'LVT18502, and 'LVT18504 is similar to that for the 'ABT18245. Therefore, this information will only be provided in the data sheet for the 'ABT18245 in section 9. Please contact your local TI sales representative for further information.

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT18245 . . . WD PACKAGE
SN74LVT18245 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The SN54LVT18245 and SN74LVT18245 scan test devices with 18-bit bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit noninverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

SCOPE and Widebus are trademarks of Texas Instruments Incorporated.

description (continued)

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT18245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

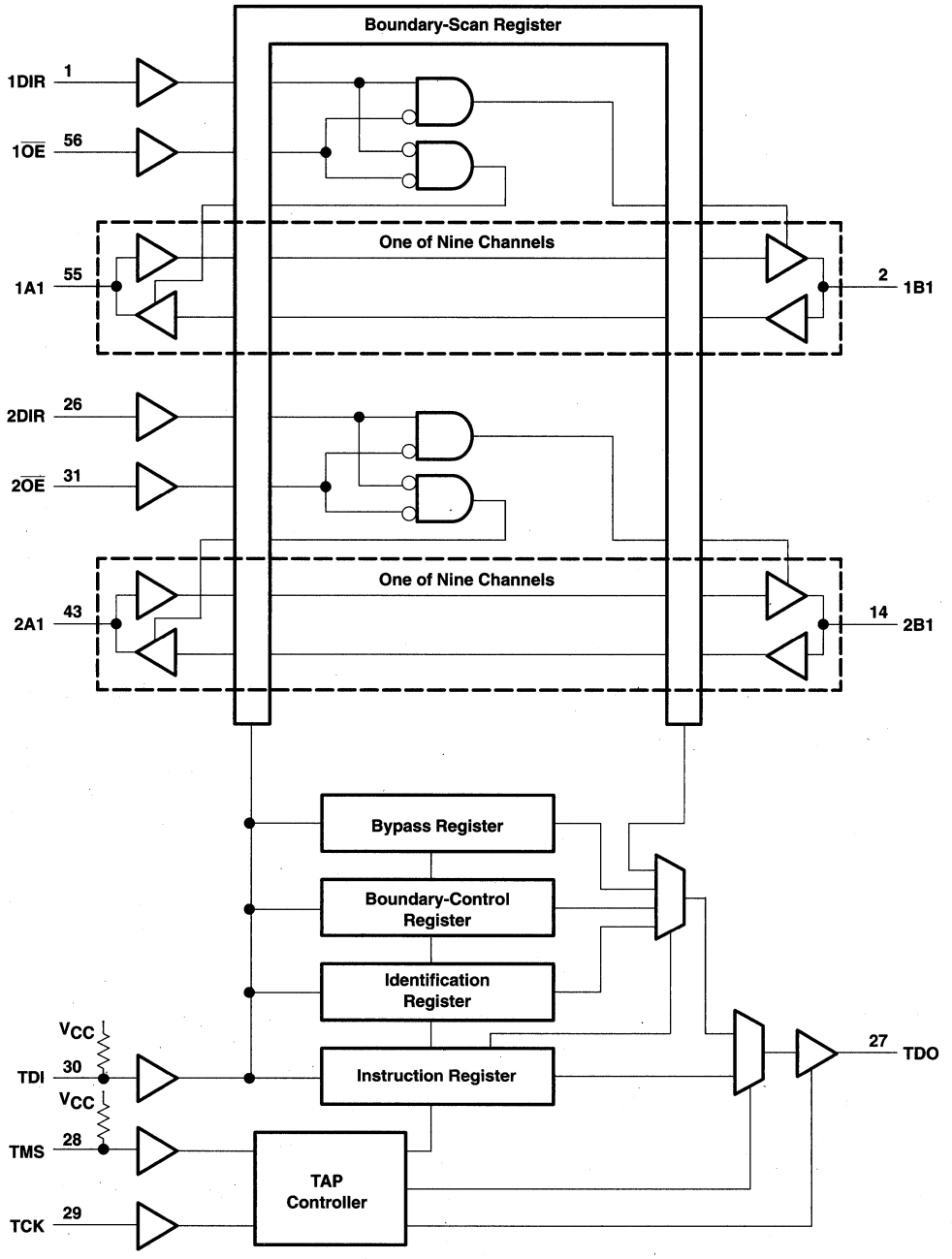
The SN54LVT18245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT18245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Terminal Functions

PIN NAME	DESCRIPTION
GND	Ground
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1DIR, 2DIR	Normal-function direction controls. See function table for normal-mode logic.
$1\overline{OE}$, $2\overline{OE}$	Normal-function output enables. See function table for normal-mode logic.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT18245 ..... 96 mA
SN74LVT18245 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18245 ..... 48 mA
SN74LVT18245 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 0.95 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT18245		SN74LVT18245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			SN54LVT18245			SN74LVT18245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	DIR, OE, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	TDI, TMS			50			50	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				–100			–100	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§			20			20	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			15			15	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

			SN54LVT18245				SN74LVT18245				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	50			MHz
t_w	Pulse duration	TCK high or low					8.1				ns
t_{su}	Setup time	A, B, DIR, or $\overline{OE}$ before TCK↑					7				ns
		TDI before TCK↑					4.5				
		TMS before TCK↑					3.6				
t_h	Hold time	A, B, DIR, or $\overline{OE}$ after TCK↑					0				ns
		TDI after TCK↑					0				
		TMS after TCK↑					0.5				
t_d	Delay time	Power up to TCK↑					50				ns
t_r	Rise time	V_{CC} power up					1				µs

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18245		SN74LVT18245		UNIT
			V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
			MIN MAX	MAX	MIN MAX	MAX	
t_{PLH}	A or B	B or A			1.5 4.8		ns
t_{PHL}					1.5 5.4		
t_{PZH}	$\overline{OE}$	B or A			3 8.5		ns
t_{PZL}					3 9		
t_{PHZ}	$\overline{OE}$	B or A			3 9.5		ns
t_{PLZ}					3 9.5		

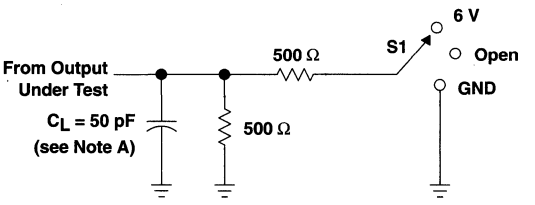
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18245		SN74LVT18245		UNIT
			V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
			MIN MAX	MAX	MIN MAX	MAX	
f_{max}	TCK↓				50		MHz
t_{PLH}	TCK↓	A or B			3 13.1		ns
t_{PHL}					3 12.8		
t_{PLH}	TCK↓	TDO			2 6.1		ns
t_{PHL}					2 6.5		
t_{PZH}	TCK↓	A or B			4 13.4		ns
t_{PZL}					4 13.6		
t_{PZH}	TCK↓	TDO			2 6.6		ns
t_{PZL}					2.5 6.9		
t_{PHZ}	TCK↓	A or B			3.5 13.6		ns
t_{PLZ}					2.5 12.7		
t_{PHZ}	TCK↓	TDO			2 7.2		ns
t_{PLZ}					1.5 6.3		

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

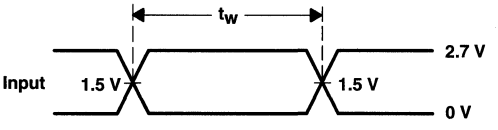
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

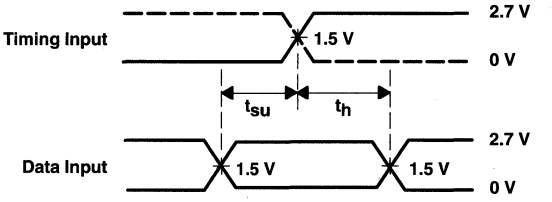


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

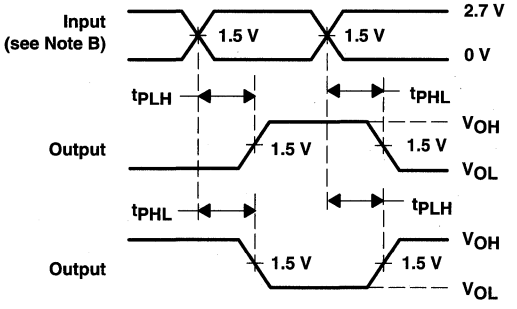
LOAD CIRCUIT FOR OUTPUTS



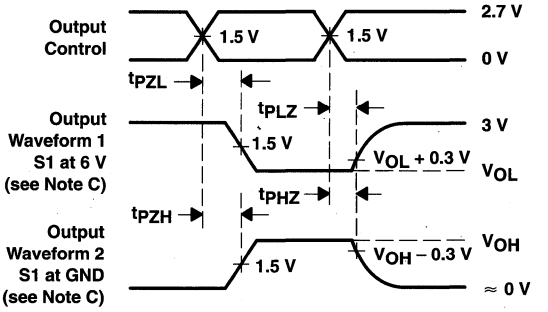
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

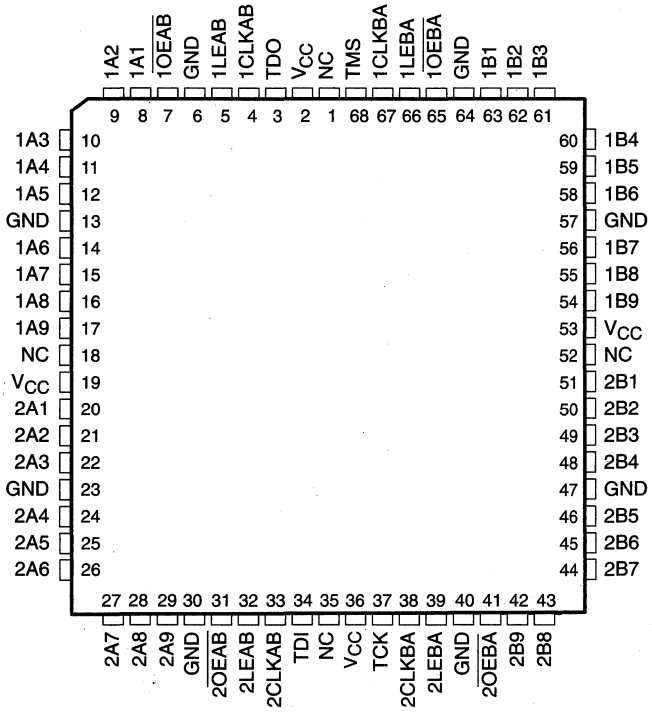
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT18502 . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

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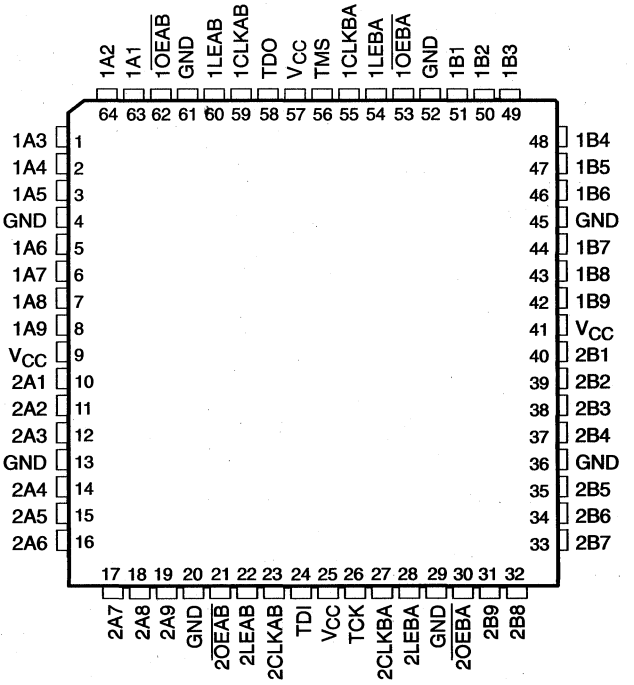
SN74LVT18502 . . . PM PACKAGE
(TOP VIEW)



description

The SN54LVT18502 and SN74LVT18502 scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

PRODUCT PREVIEW

description (continued)

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT18502 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT18502 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE† (normal mode, each register)

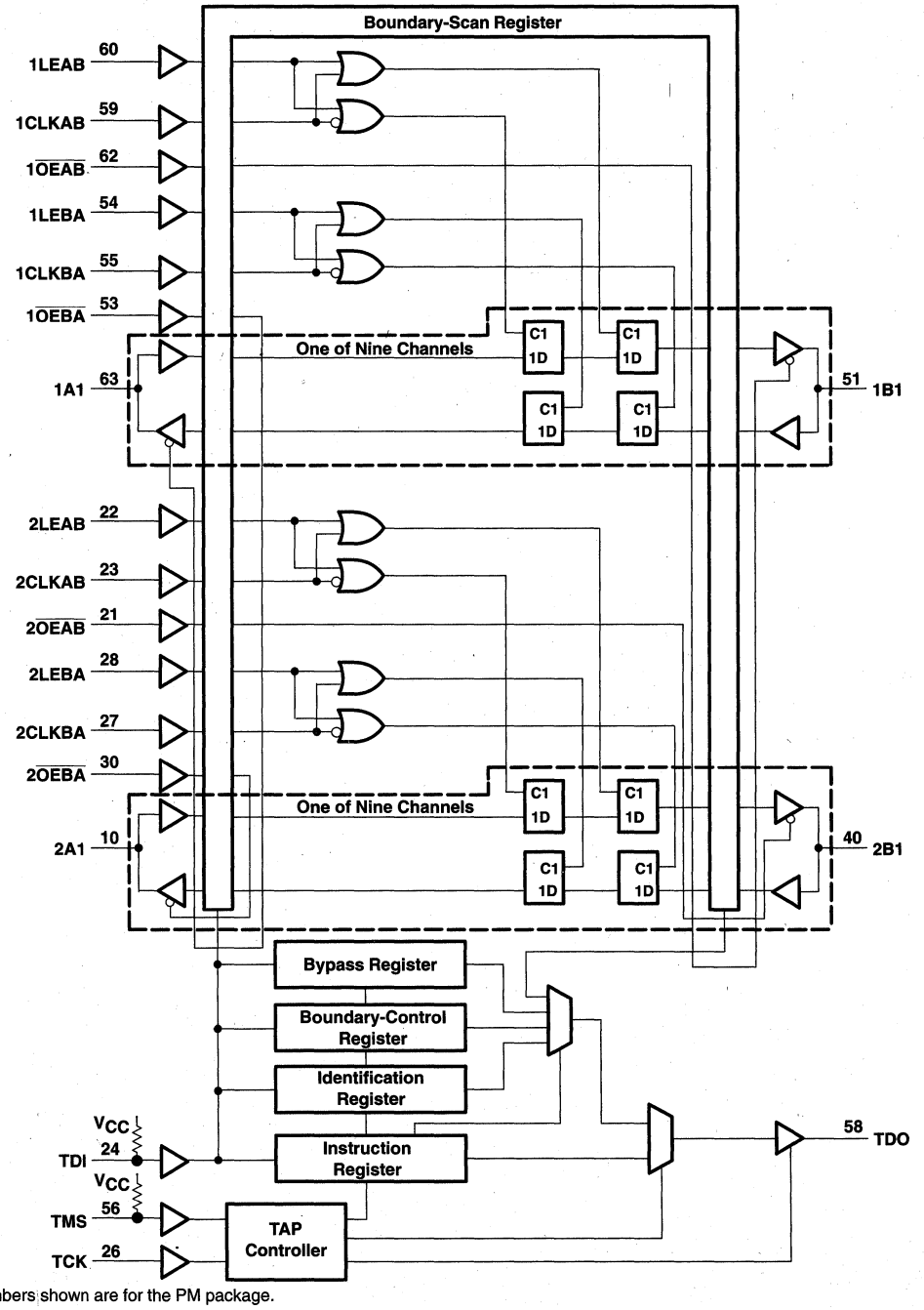
INPUTS				OUTPUT
$\overline{OEAB}$	LEAB	CLKAB	A	B
L	L	L	X	B_0‡
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

PRODUCT PREVIEW

functional block diagram



Pin numbers shown are for the PM package.

Terminal Functions

PIN NAME	DESCRIPTION
GND	Ground
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
1LEAB, 1LEBA, 2LEAB, 2LEBA	Normal-function latch enables. See function table for normal-mode logic.
$1\overline{OE}AB$, $1\overline{OE}BA$, $2\overline{OE}AB$, $2\overline{OE}BA$	Normal-function output enables. See function table for normal-mode logic.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT18502 ..... 96 mA
SN74LVT18502 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18502 ..... 48 mA
SN74LVT18502 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): PM package ..... 885 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT18502		SN74LVT18502		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			SN54LVT18502			SN74LVT18502			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = −8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = −24 mA		2						
	V_{CC} = 3 V,	I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, LE, OE, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	TDI, TMS			50			50	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				−100			−100	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§			20			20	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			15			15	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

				SN54LVT18502			SN74LVT18502			UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	
				MIN	MAX	MIN MAX	MIN	MAX	MIN MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA					0	100		MHz
t_w	Pulse duration	CLKAB or CLKBA high or low					3.5			ns
		LEAB or LEBA high					3.5			
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					4			ns
		A before LEAB↓ or B before LEBA↓	CLK high				3.5			
			CLK low				2			
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑					0			ns
		A after LEAB↓ or B after LEBA↓					2			

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

			SN54LVT18502			SN74LVT18502			UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	
			MIN	MAX	MIN MAX	MIN	MAX	MIN MAX	
f_{clock}	Clock frequency	TCK				0	50		MHz
t_w	Pulse duration	TCK high or low				8			ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑				4.5			ns
		TDI before TCK↑				7.5			
		TMS before TCK↑				3			
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑				0.5			ns
		TDI after TCK↑				0.5			
		TMS after TCK↑				0.5			
t_d	Delay time	Power up to TCK↑				50			ns
t_r	Rise time	V_{CC} power up				1			µs

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18502		SN74LVT18502		UNIT
			V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
			MIN MAX	MAX	MIN MAX	MAX	
f_{max}	CLKAB or CLKBA				100		MHz
t_{PLH}	A or B	B or A			2 6		ns
t_{PHL}					2 6		
t_{PLH}	CLKAB or CLKBA	B or A			2.5 6		ns
t_{PHL}					2.5 6		
t_{PLH}	LEAB or LEBA	B or A			2.5 7		ns
t_{PHL}					2.5 7		
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A			2 7		ns
t_{PZL}					2.5 8		
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A			3 8.8		ns
t_{PLZ}					2.5 7.3		

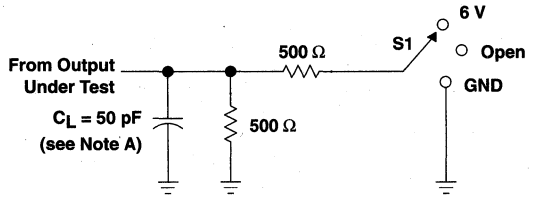
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18502		SN74LVT18502		UNIT
			V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
			MIN MAX	MAX	MIN MAX	MAX	
f_{max}	TCK				50		MHz
t_{PLH}	TCK↓	A or B			2.5 13.5		ns
t_{PHL}					2.5 12.4		
t_{PLH}	TCK↓	TDO			2 5.6		ns
t_{PHL}					2 6		
t_{PZH}	TCK↓	A or B			4.5 13.4		ns
t_{PZL}					5 14		
t_{PZH}	TCK↓	TDO			2.5 6.8		ns
t_{PZL}					3 7.5		
t_{PHZ}	TCK↓	A or B			4 16.3		ns
t_{PLZ}					3.5 15.3		
t_{PHZ}	TCK↓	TDO			3 7.6		ns
t_{PLZ}					3 7.6		

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

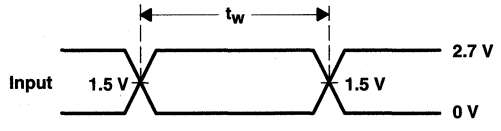
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

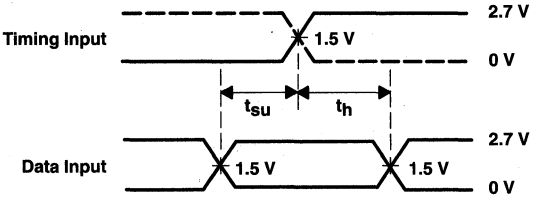


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

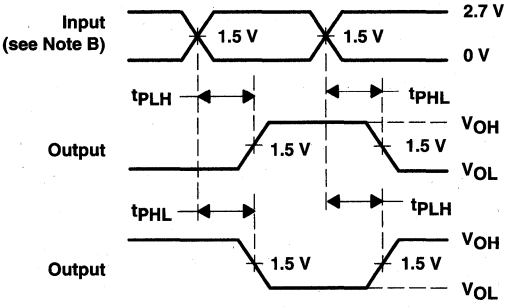
LOAD CIRCUIT FOR OUTPUTS



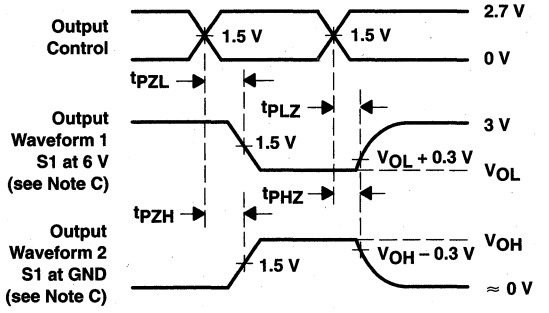
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

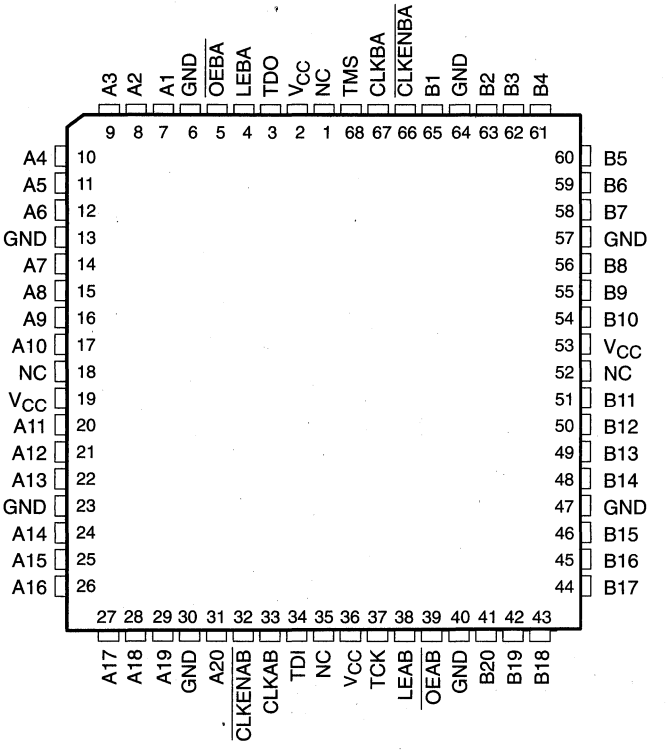
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat Packages Using 25-mil Center-to-Center Spacings

PRODUCT PREVIEW

SN54LVT18504 . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

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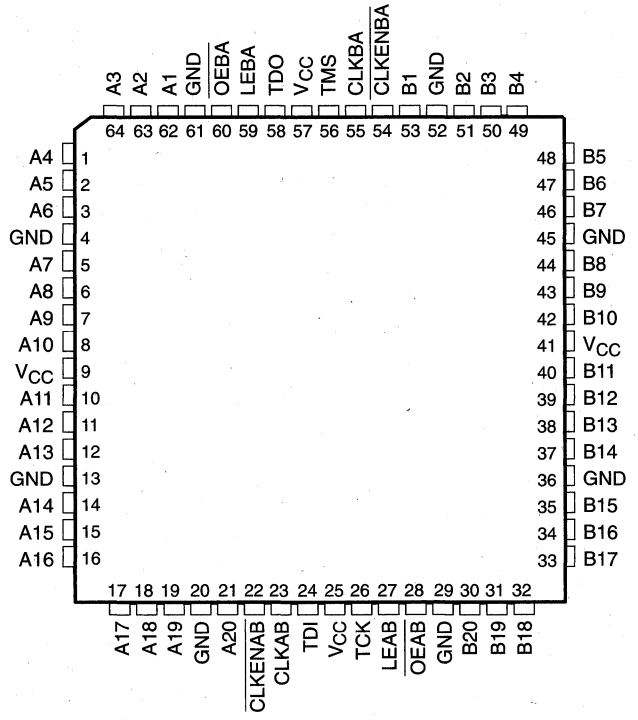
PRODUCT PREVIEW

SN74LVT18504 . . . PM PACKAGE
(TOP VIEW)



description

The SN54LVT18504 and SN74LVT18504 scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while $\overline{CLKENAB}$ is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and $\overline{CLKENAB}$ is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA inputs.

description (continued)

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT18504 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT18504 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

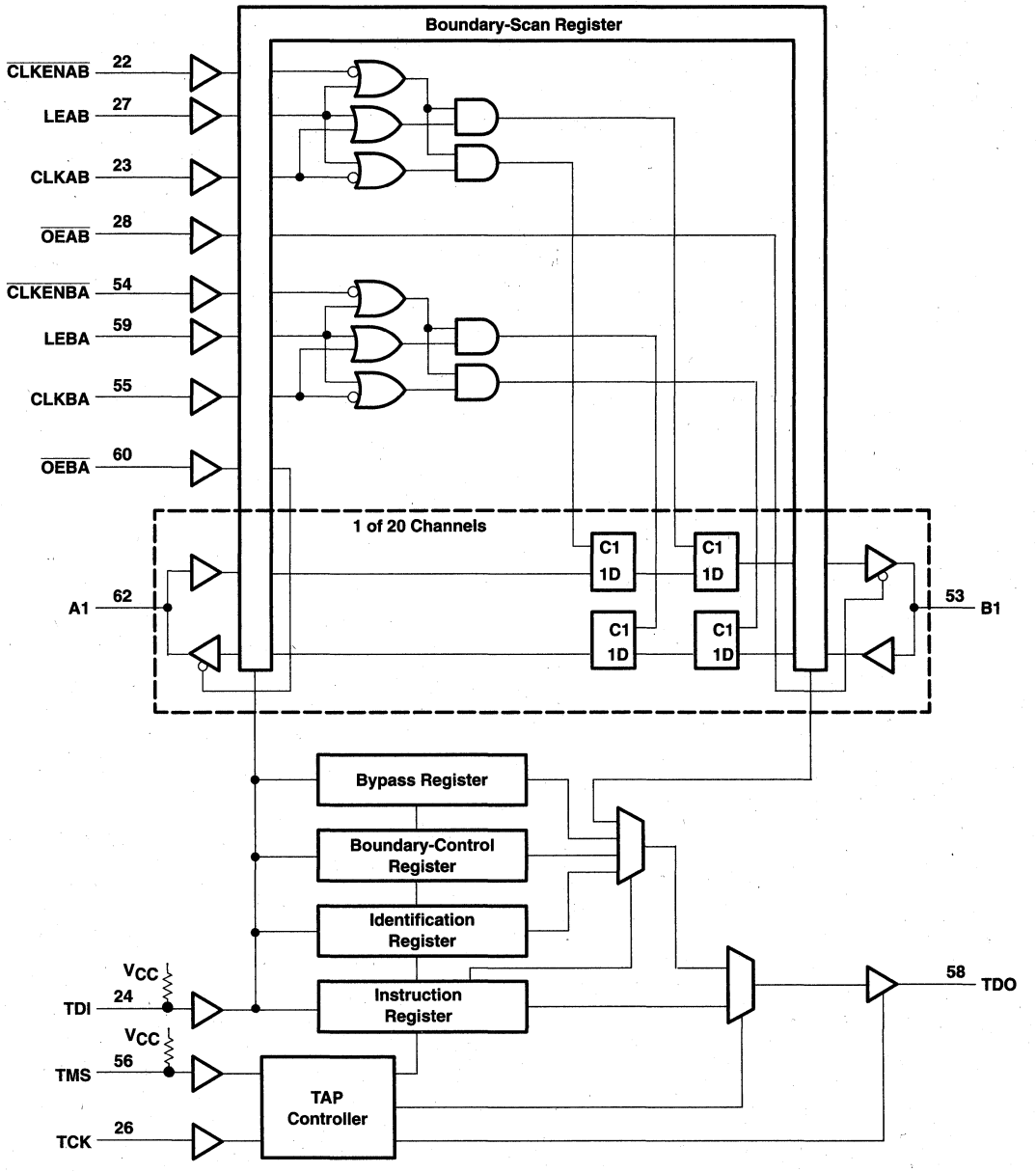
INPUTS					OUTPUT
$\overline{OEAB}$	LEAB	$\overline{CLKENAB}$	CLKAB	A	B
L	L	L	L	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	H	X	X	B_0‡
L	H	X	X	L	L
L	H	X	X	H	H
H	X	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

PRODUCT PREVIEW

functional block diagram



Pin numbers shown are for the PM package.

Terminal Functions

PIN NAME	DESCRIPTION
A1–A20	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1–B20	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
$\overline{\text{CLKENAB}}$, $\overline{\text{CLKENBA}}$	Normal-function clock enables. See function table for normal-mode logic.
GND	Ground
LEAB, LEBA	Normal-function latch enables. See function table for normal-mode logic.
$\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT18504 ..... 96 mA
SN74LVT18504 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18504 ..... 48 mA
SN74LVT18504 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): PM package ..... 885 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

PRODUCT PREVIEW

recommended operating conditions

			SN54LVT18504		SN74LVT18504		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			SN54LVT18504			SN74LVT18504			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = − 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, CLKEN, LE, $\overline{OE}$, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	TDI, TMS			50			50	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				−100			−100	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§			20			20	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			15			15	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

				SN54LVT18504		SN74LVT18504		UNIT
				V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
				MIN MAX	MIN MAX	MIN MAX	MIN MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA				0 100		MHz
t_w	Pulse duration	CLKAB or CLKBA high or low				4		ns
		LEAB or LEBA	CLK high or low			3.5		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑				4		ns
		A before LEAB↓ or B before LEBA↓	CLK high			3.5		
			CLK low			2		
		$\overline{CLKEN}$ before CLK↑				4		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑				0		ns
		A after LEAB↓ or B after LEBA↓				2		
		$\overline{CLKEN}$ after CLK↑				0		

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

			SN54LVT18504		SN74LVT18504		UNIT
			V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
f_{clock}	Clock frequency	TCK			0 50		MHz
t_w	Pulse duration	TCK high or low			8		ns
t_{su}	Setup time	A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ before TCK↑			4.5		ns
		TDI before TCK↑			7.5		
		TMS before TCK↑			3		
t_h	Hold time	A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ after TCK↑			0.5		ns
		TDI after TCK↑			0.5		
		TMS after TCK↑			0.5		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18504		SN74LVT18504		UNIT
			V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
			MIN MAX	MAX	MIN MAX	MAX	
f_{max}	CLKAB or CLKBA				100		MHz
t_{PLH}	A or B	B or A			2 6		ns
t_{PHL}					2 6.5		
t_{PLH}	CLKAB or CLKBA	B or A			2.5 6.8		ns
t_{PHL}					2.5 6.5		
t_{PLH}	LEAB or LEBA	B or A			2.5 7.1		ns
t_{PHL}					2.5 7.2		
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A			2 7		ns
t_{PZL}					2.5 8		
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A			3 8.8		ns
t_{PLZ}					2.5 7.3		

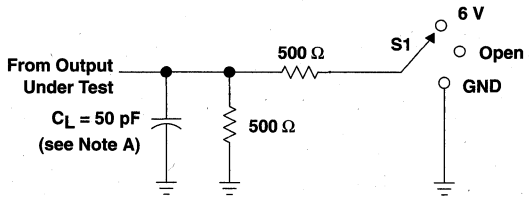
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18504		SN74LVT18504		UNIT
			V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
			MIN MAX	MAX	MIN MAX	MAX	
f_{max}	TCK				50		MHz
t_{PLH}	TCK↓	A or B			2.5 13.5		ns
t_{PHL}					2.5 12.5		
t_{PLH}	TCK↓	TDO			2 5.6		ns
t_{PHL}					2 6.5		
t_{PZH}	TCK↓	A or B			4.5 13.8		ns
t_{PZL}					5 14.5		
t_{PZH}	TCK↓	TDO			2 7		ns
t_{PZL}					3 7.5		
t_{PHZ}	TCK↓	A or B			4 17		ns
t_{PLZ}					3.5 16		
t_{PHZ}	TCK↓	TDO			3 7.5		ns
t_{PLZ}					3 7.5		

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

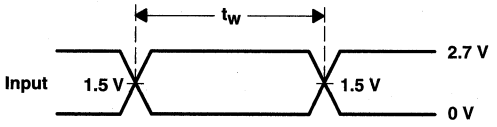
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

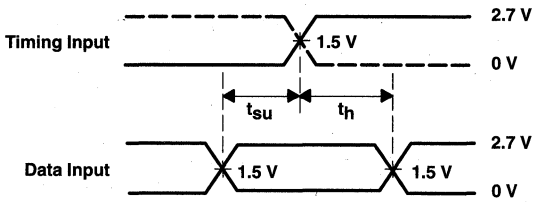


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

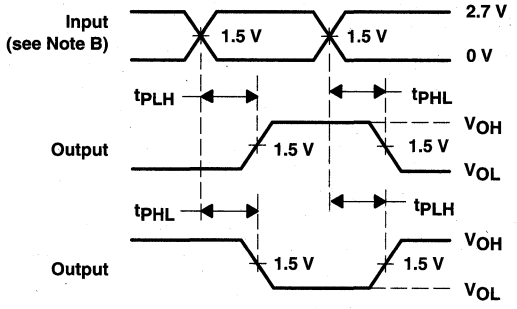
LOAD CIRCUIT FOR OUTPUTS



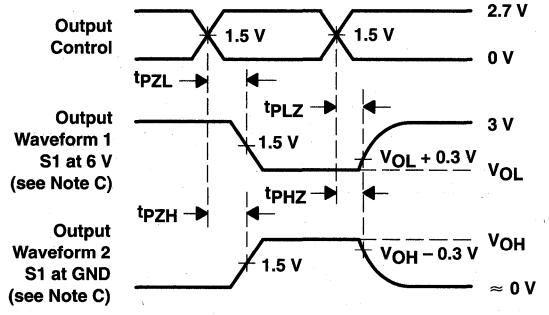
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

LVT OCTALS

Features

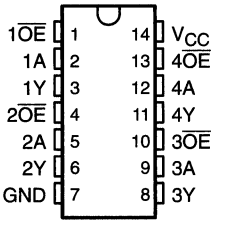
- EPIC-IIB™ BiCMOS process with special low-voltage enhancements
- Mixed-mode circuitry
- Expanded V_{CC} range from 2.7 V to 3.6 V
- Bus-hold circuitry
- Power-on-demand active feedback circuitry
- SOIC and EIAJ TSSOP packaging
- TI has established an alternate source

Benefits

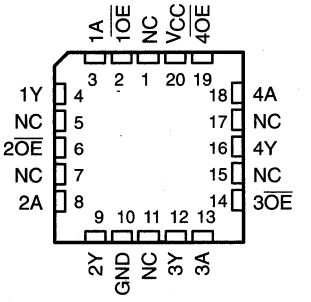
- 3.3-V logic family with equivalent speed and drive performance of 5-V ABT logic family – not just a recharacterized or scaled CMOS
- Complete input and output compatibility with 5 signals combined with a pure 3.3-V internal su signal – provides bidirectional 3-V to 5-V translation
- AC performance optimized for both regulated supply and unregulated battery operation
- Reduces component count by eliminating nee for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floatin
- Reduces disabled static power consumption (I_{CCZ}) to as little as 0.1 mA for power-conscious portable and battery-powered equipment
- Space-saving and height-saving surface-mour package options, pin compatible with existing families for easy conversion
- Standardization that comes from a common product approach

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT125 . . . J PACKAGE
SN74LVT125 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT125 features independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable ($\overline{OE}$) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

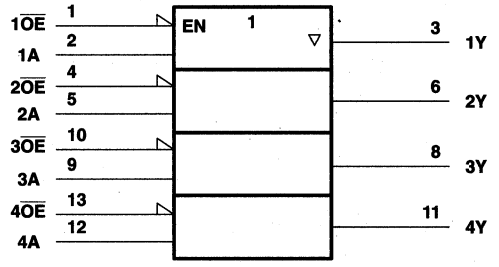
The SN74LVT125 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT125 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT125 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

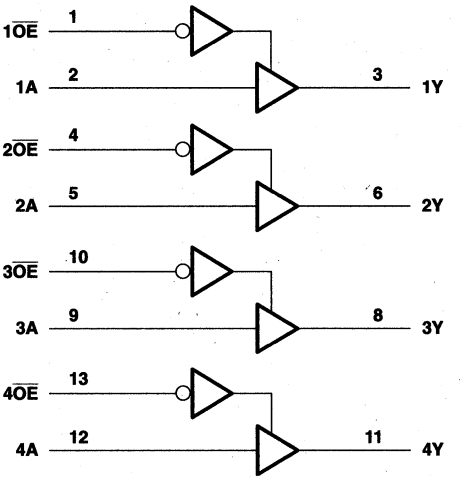
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, J, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT125 ..... 96 mA
SN74LVT125 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT125 ..... 48 mA
SN74LVT125 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.6 W
DW package ..... 0.85 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT125		SN74LVT125		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

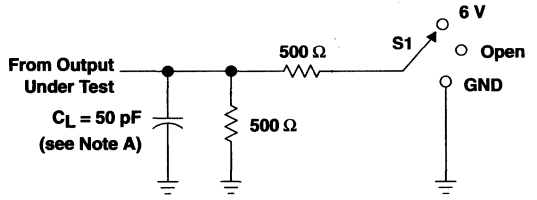
PARAMETER	TEST CONDITIONS			SN54LVT125			SN74LVT125			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0	Data pins			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V	Data inputs	–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.19		0.12	0.19	mA
			Outputs low		4.5	7		4.5	7	
			Outputs disabled		0.12	0.19		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

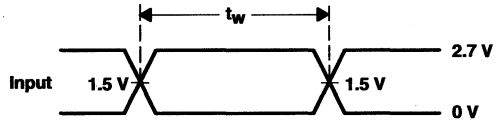
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT125			SN74LVT125				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	A	Y	1	4.2	4.7	1	2.7	4	4.5	ns
t_{PHL}			1	4.1	5.1	1	2.9	3.9	4.9	
t_{PZH}	$\overline{OE}$	Y	1	4.9	6.2	1	3.4	4.7	6	ns
t_{PZL}			1.1	4.9	6.7	1.1	3.4	4.7	6.5	
t_{PHZ}	$\overline{OE}$	Y	1.8	5.3	5.9	1.8	3.7	5.1	5.7	ns
t_{PLZ}			1.3	4.7	4.2	1.3	2.6	4.5	4	

PARAMETER MEASUREMENT INFORMATION

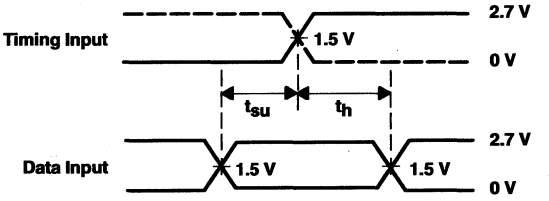


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

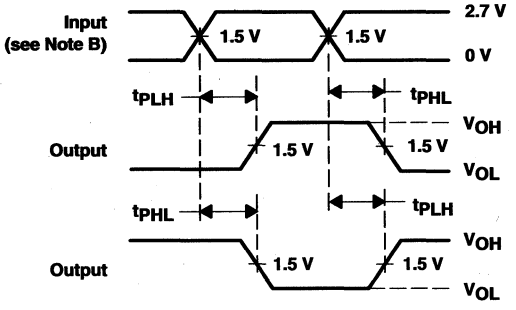
LOAD CIRCUIT FOR OUTPUTS



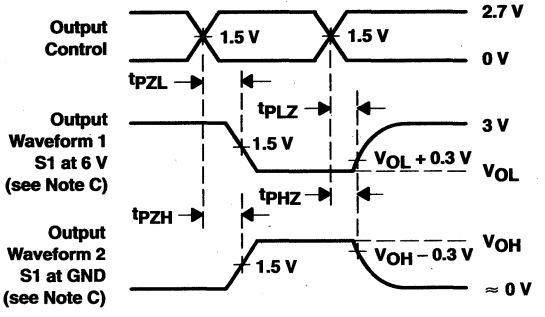
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



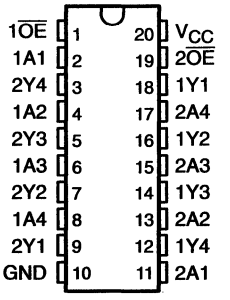
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

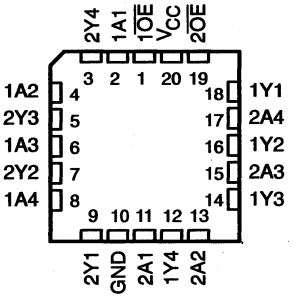
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT240 . . . J PACKAGE
SN74LVT240 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT240 is organized as two 4-bit buffer/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

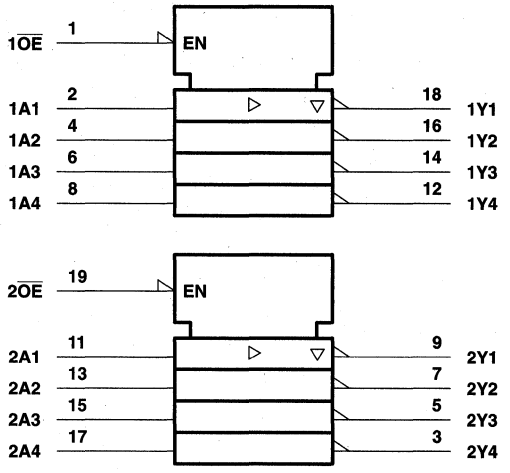
The SN74LVT240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

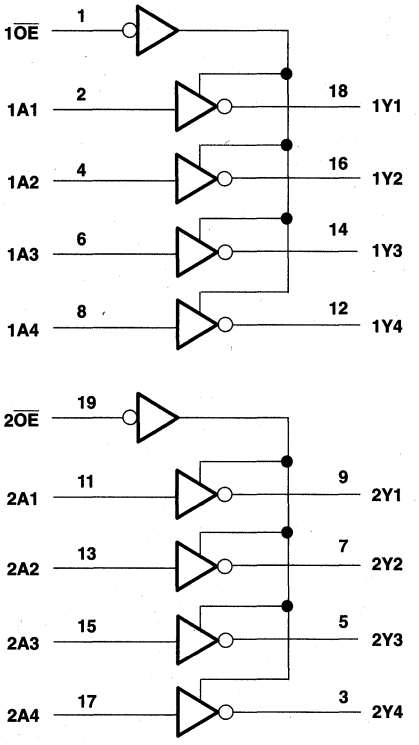
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT240 ..... 96 mA
SN74LVT240 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT240 ..... 48 mA
SN74LVT240 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
PW package ..... 0.6 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT240		SN74LVT240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

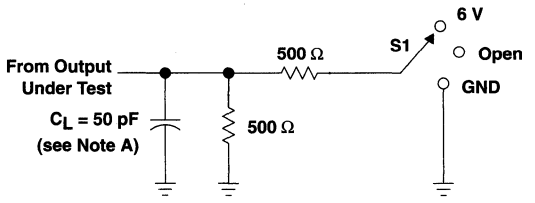
PARAMETER	TEST CONDITIONS			SN54LVT240			SN74LVT240			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.19		0.12	0.19	mA
			Outputs low		8.6	12		8.6	12	
			Outputs disabled		0.12	0.19		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

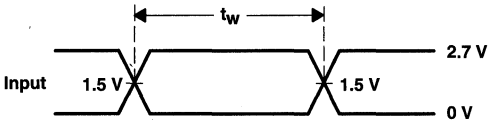
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT240			SN74LVT240				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	A	Y	1	4.5	5.4	1	2.5	4.3	5.2	ns
t_{PHL}			1	4.5	5.2	1	2.5	4.3	5	
t_{PZH}	$\overline{OE}$	Y	1	5.4	6.5	1	2.7	5.2	6.3	ns
t_{PZL}			1	5.4	7.4	1	3.1	5.2	6.7	
t_{PHZ}	$\overline{OE}$	Y	2	5.8	6.5	2	3.9	5.6	6.3	ns
t_{PLZ}			1.6	5.3	5.8	1.6	3.2	5.1	5.6	

PARAMETER MEASUREMENT INFORMATION

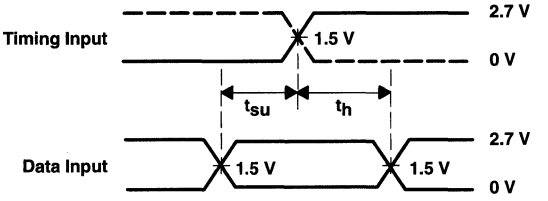


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

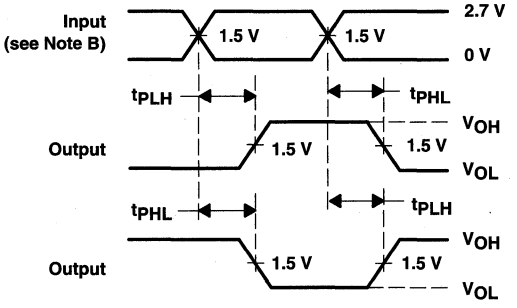
LOAD CIRCUIT FOR OUTPUTS



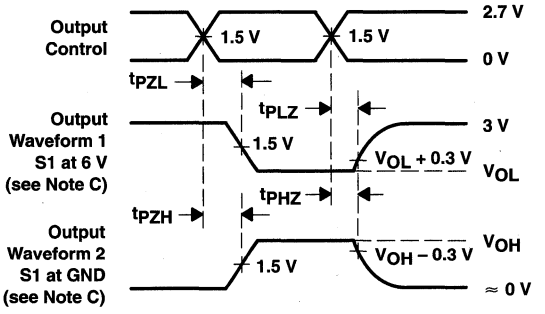
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



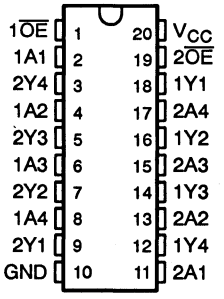
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

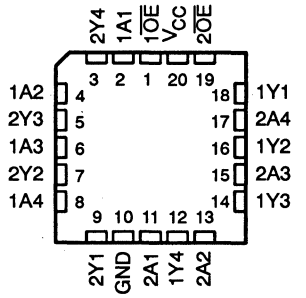
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT244A . . . J PACKAGE
SN74LVT244A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT244A . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT244A is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

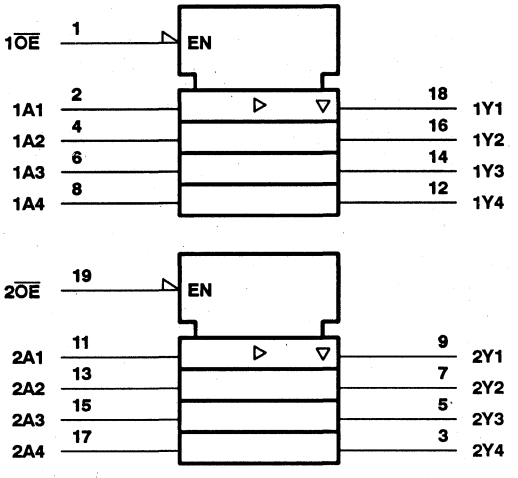
The SN74LVT244A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT244A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT244A is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

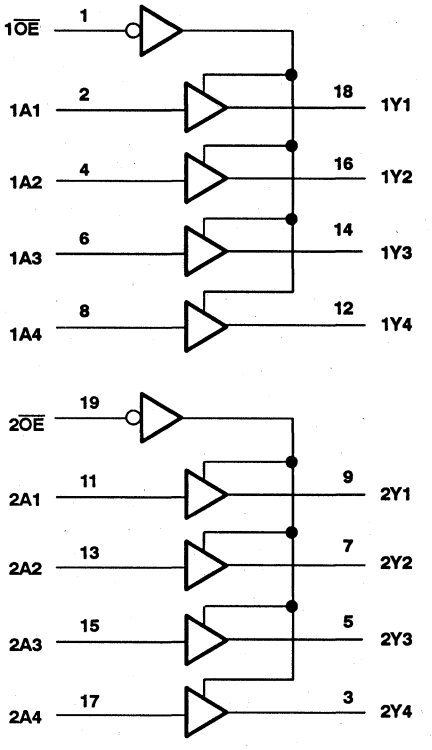
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT244A ..... 96 mA
SN74LVT244A ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT244A ..... 48 mA
SN74LVT244A ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
PW package ..... 0.6 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT244A		SN74LVT244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

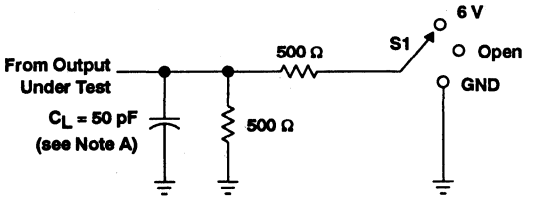
PARAMETER	TEST CONDITIONS			SN54LVT244A			SN74LVT244A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				50			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0	Data pins			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V	A inputs	–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.5		0.12	0.19	mA
			Outputs low		8.6	14		8.6	12	
			Outputs disabled		0.12	0.5		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

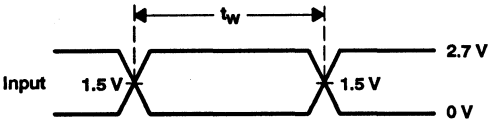
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT244A			SN74LVT244A				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	A	Y	0.5	4.7	5.2	1	2.5	4.1	5	ns
t_{PHL}			0.5	4.4	5.4	1	2.5	4.1	5.2	
t_{PZH}	$\overline{OE}$	Y	0.8	5.4	6.5	1	2.7	5.2	6.3	ns
t_{PZL}			0.8	5.4	7.6	1.1	3.1	5.2	6.7	
t_{PHZ}	$\overline{OE}$	Y	1.5	6.2	6.9	1.9	3.9	5.6	6.3	ns
t_{PLZ}			1.2	5.5	6	1.8	3.2	5.1	5.6	

PARAMETER MEASUREMENT INFORMATION

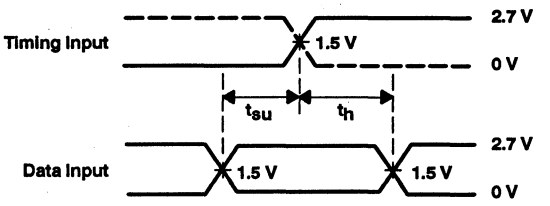


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

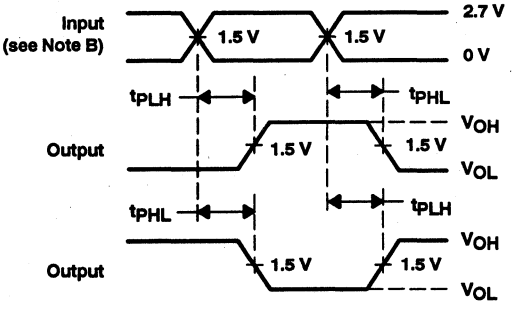
LOAD CIRCUIT FOR OUTPUTS



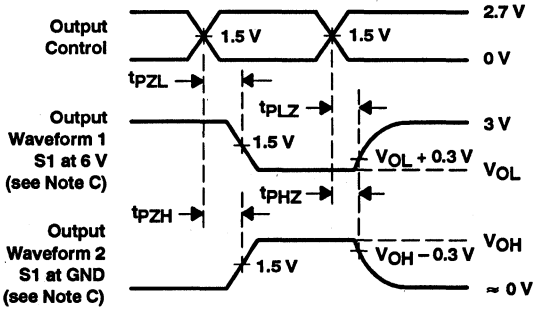
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



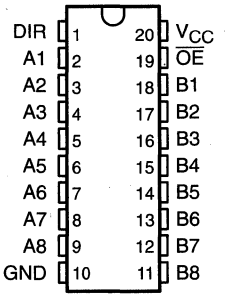
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

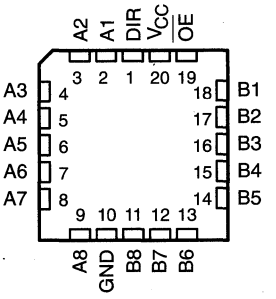
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT245 . . . J PACKAGE
SN74LVT245 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT245 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

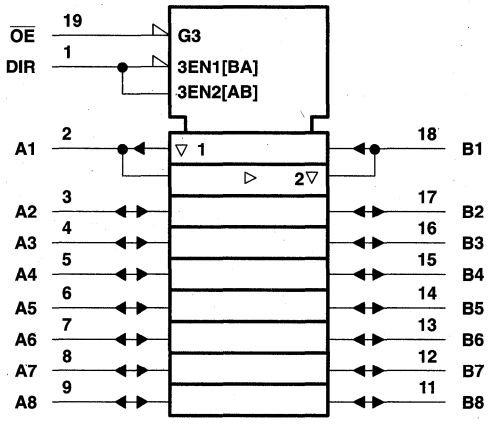
The SN74LVT245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT245 is characterized for operation from −40°C to 85°C.

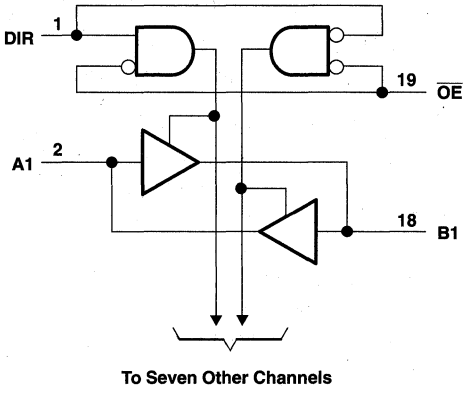
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) ..... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT245 ..... 96 mA
SN74LVT245 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT245 ..... 48 mA
SN74LVT245 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
PW package ..... 0.6 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT245		SN74LVT245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT245			SN74LVT245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§			100			20	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.5		0.13	0.19	mA
			Outputs low		8.8	14		8.8	12	
			Outputs disabled		0.13	0.5		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				10			10		pF

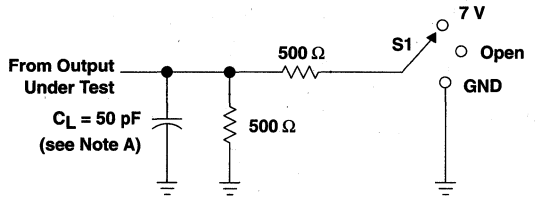
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT245			SN74LVT245				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	A or B	B or A	0.5	4.4	5.2	1	2.4	4	4.7	ns
t_{PHL}			0.5	4.2	4.8	1	2.4	4	4.6	
t_{PZH}	$\overline{OE}$	A or B	0.8	5.9	7.3	1.1	3.4	5.5	7.1	ns
t_{PZL}			1	5.9	7.2	1.5	3.6	5.5	6.5	
t_{PHZ}	$\overline{OE}$	A or B	1.5	6.5	7.2	2.2	4.3	5.9	6.5	ns
t_{PLZ}			1.5	6.1	6.5	2	3.5	4.8	4.8	

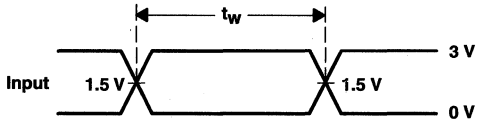
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

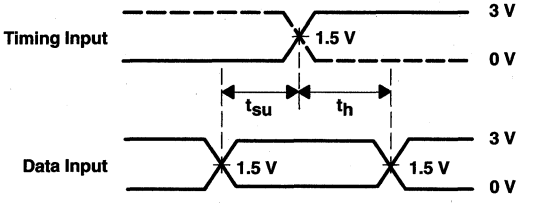


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

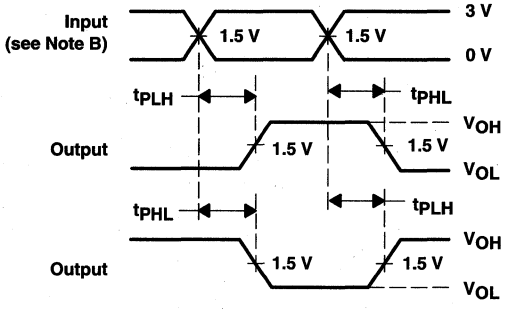
LOAD CIRCUIT FOR OUTPUTS



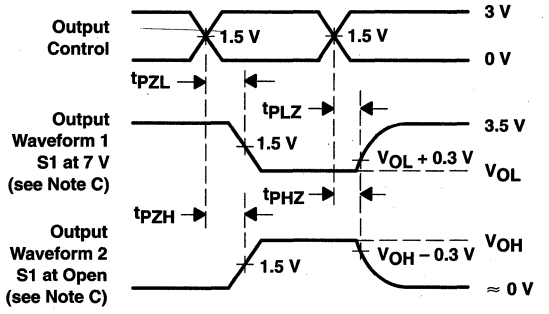
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



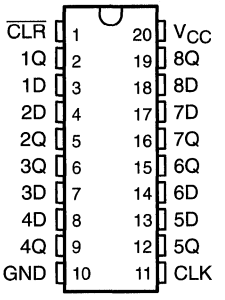
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

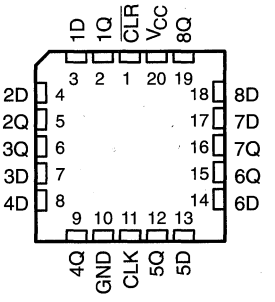
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Buffered Clock and Direct Clear Inputs**
- **Individual Data Input to Each Flip-Flop**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT273 . . . J PACKAGE
SN74LVT273 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT273 . . . FK PACKAGE
(TOP VIEW)



description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT273 is a positive-edge-triggered flip-flop with a direct clear input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

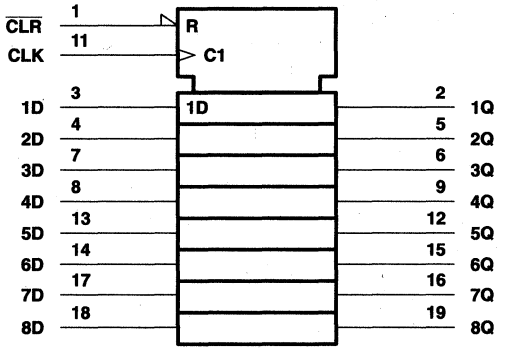
The SN74LVT273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT273 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

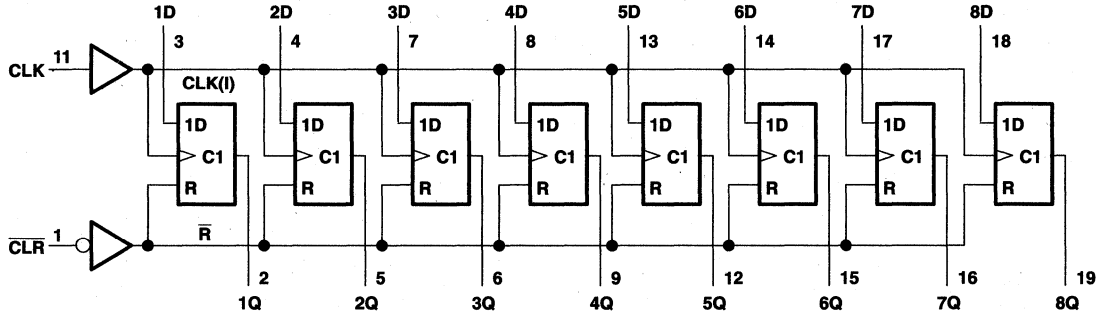
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H or L	X	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT273 ..... 96 mA
SN74LVT273 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT273 ..... 48 mA
SN74LVT273 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
PW package ..... 0.6 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT273		SN74LVT273		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		24		32	mA
I_{OL}‡	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT273			SN74LVT273			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0				–5			–5	
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.19		0.12	0.19	mA
			Outputs low		8.6	12		8.6	12	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0							4		pF
C_o	V_O = 3 V or 0							8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

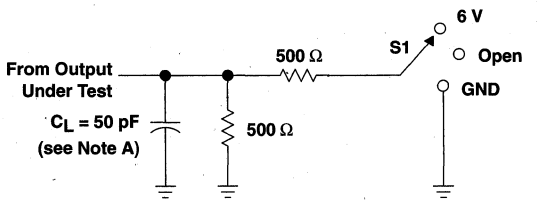
			SN54LVT273			SN74LVT273			UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	
			MIN	MAX	MIN	MIN	MAX	MIN	
f_{clock}	Clock frequency					0	150		MHz
t_w	Pulse duration					3.3		3.3	ns
t_{su}	Setup time before CLK↑	Data high or low				2.3		2.7	ns
		$\overline{CLR}$ high				2.7		3.2	
t_h	Hold time after CLK↑	Data high or low				0		0	ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT273			SN74LVT273				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
f_{max}						150				MHz
t_{PLH}	CLK	Any Q				1.7	3.5	5.5	6.3	ns
t_{PHL}						1.9	3.5	5.5	5.9	
t_{PHL}	$\overline{CLR}$	Any Q				1.3	3.2	5.1	6.2	ns

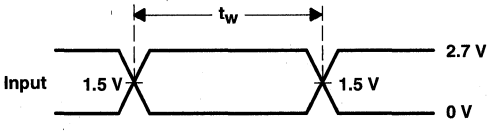
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

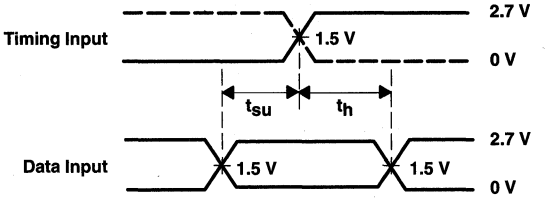


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

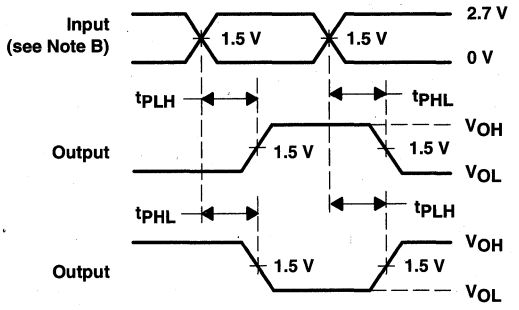
LOAD CIRCUIT FOR OUTPUTS



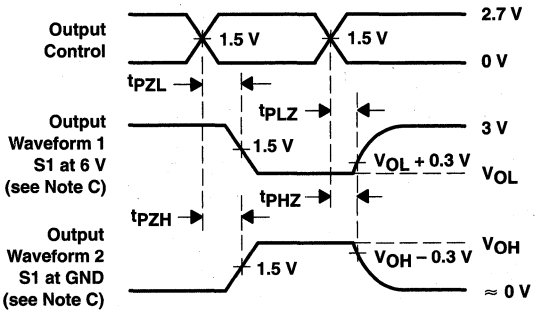
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



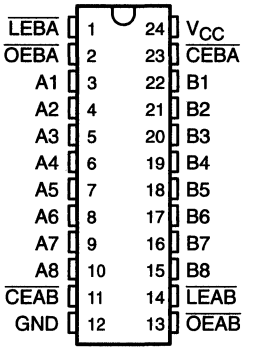
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

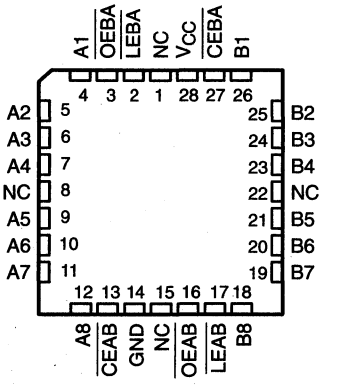
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT543 . . . JT PACKAGE
SN74LVT543 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT543 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These octal transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

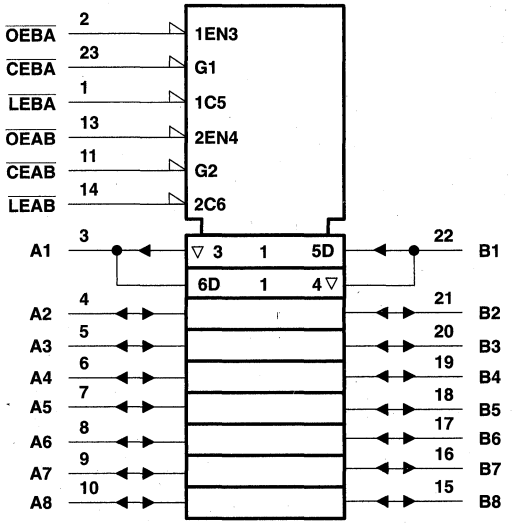
The SN54LVT543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT543 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

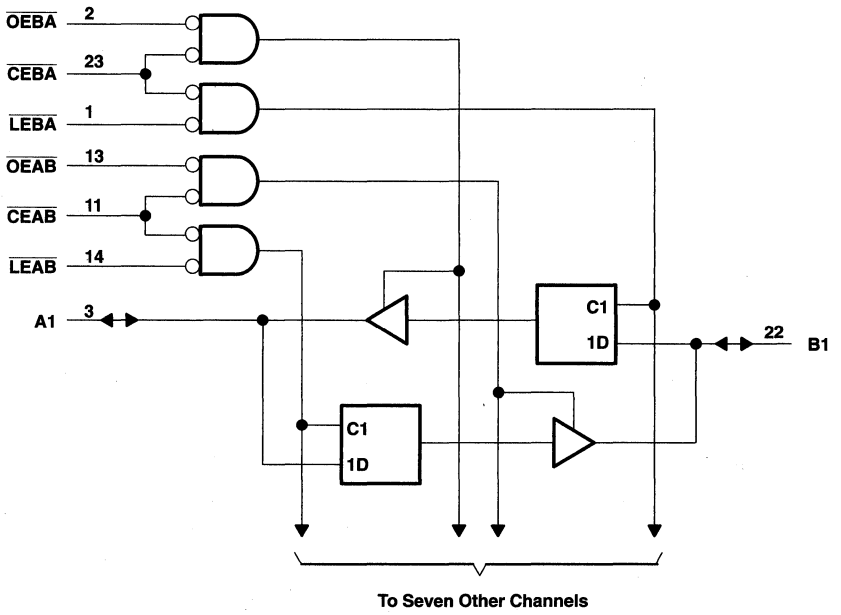
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT543 ..... 96 mA
SN74LVT543 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT543 ..... 48 mA
SN74LVT543 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.7 W
DW package ..... 1 W
PW package ..... 0.65 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT543		SN74LVT543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT543			SN74LVT543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V	Control pins			10			10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§			20			20	
	V_{CC} = 3.6 V,	V_I = V_{CC}	A or B ports§			1			1	
	V_{CC} = 3.6 V,	V_I = 0	A or B ports§			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V	A or B ports	–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.19		0.13	0.19	mA
			Outputs low		8.8	12		8.8	12	
			Outputs disabled		0.13	0.19		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4.5			4.5		pF
C_{io}	V_O = 3 V or 0				11			11		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

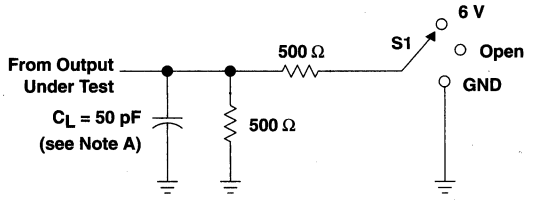
				SN54LVT543		SN74LVT543		UNIT
				V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
				MIN	MIN	MIN	MIN	
t_w	Pulse duration	$\overline{LEAB}$ or $\overline{LEBA}$ low		3.3	3.3	3.3	3.3	ns
t_{su}	Setup time	Data before $\overline{LEAB}$ or $\overline{LEBA}$↑	High	0	0	0	0	ns
			Low	0.8	1.1	0.8	1.1	
		Data before $\overline{CEAB}$ or $\overline{CEBA}$↑	High	0	0	0	0	
			Low	0.9	1.2	0.9	1.2	
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}$↑		1.7	1.7	1.7	1.7	ns
		Data after $\overline{CEAB}$ or $\overline{CEBA}$↑		1.8	1.8	1.8	1.8	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT543			SN74LVT543				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	A or B	B or A	1	4.9	5.7	1	2.9	4.7	5.5	ns
t_{PHL}			1	4.8	6	1	3.3	4.6	5.8	
t_{PLH}	$\overline{LE}$	A or B	1	6.1	7.5	1	4	5.9	7.3	ns
t_{PHL}			1	5.9	7.5	1	4.1	5.7	7.3	
t_{PZH}	$\overline{OE}$	A or B	1	6	7.8	1	4.1	5.8	7.6	ns
t_{PZL}			1.1	6.6	8.4	1.1	4.5	6.4	8.2	
t_{PHZ}	$\overline{OE}$	A or B	2.4	6.7	7.3	2.4	4.8	6.5	7.1	ns
t_{PLZ}			2	6	6.1	2	4	5.8	5.9	
t_{PZH}	$\overline{CE}$	A or B	1	6.2	7.8	1	4.2	6	7.6	ns
t_{PZL}			1.4	6.9	8.5	1.4	4.7	6.7	8.3	
t_{PHZ}	$\overline{CE}$	A or B	2.3	6.6	7.3	2.3	4.7	6.4	7.1	ns
t_{PLZ}			2	5.6	5.8	2	3.8	5.4	5.6	

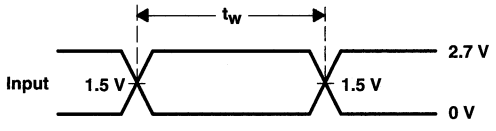
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

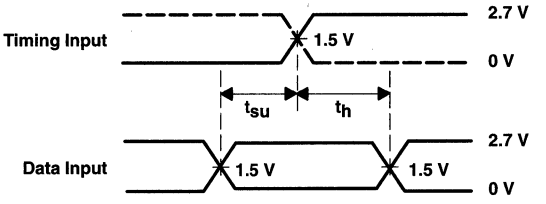


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

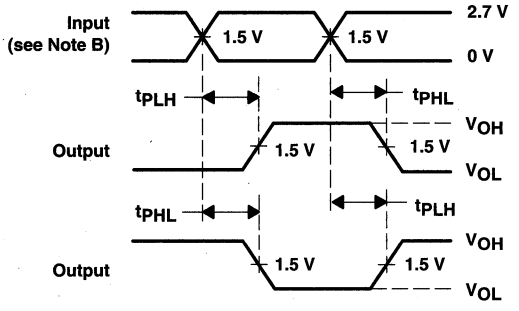
LOAD CIRCUIT FOR OUTPUTS



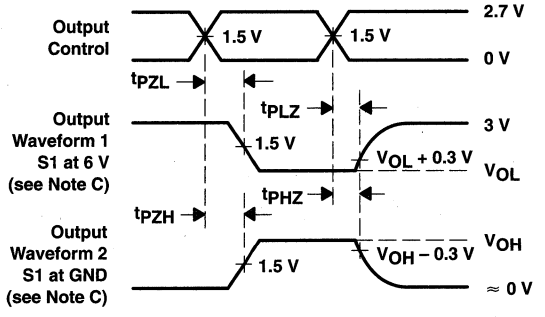
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



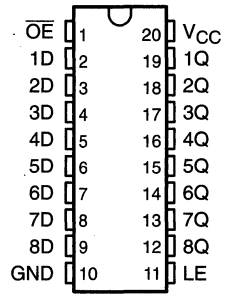
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

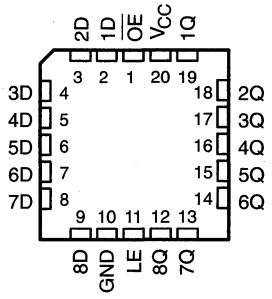
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT573 . . . J PACKAGE
SN74LVT573 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT573 . . . FK PACKAGE
(TOP VIEW)



description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels that were set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

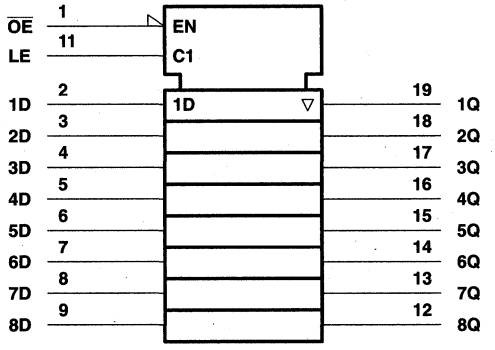
The SN74LVT573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT573 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

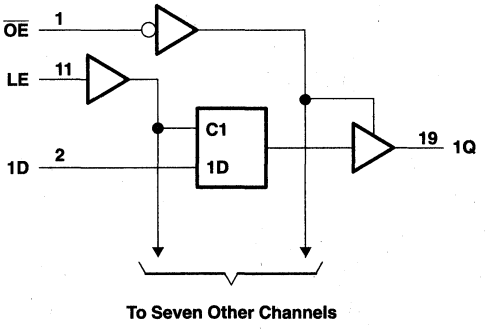
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT573 ..... 96 mA
SN74LVT573 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT573 ..... 48 mA
SN74LVT573 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
PW package ..... 0.6 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT573		SN74LVT573		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT573 MIN	SN54LVT573 TYP†	SN54LVT573 MAX	SN74LVT573 MIN	SN74LVT573 TYP†	SN74LVT573 MAX	UNIT
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0	Data pins			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V	Data inputs	–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.19		0.13	0.19	mA
			Outputs low		8.6	12		8.6	12	
			Outputs disabled		0.13	0.19		0.13	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

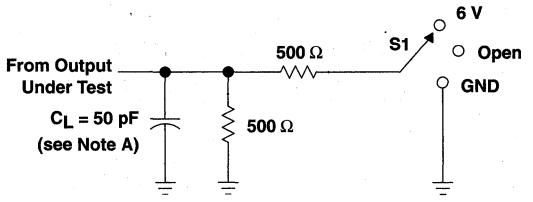
			SN54LVT573 V_{CC} = 3.3 V ± 0.3 V MIN	SN54LVT573 V_{CC} = 3.3 V ± 0.3 V MAX	SN54LVT573 V_{CC} = 2.7 V MIN	SN74LVT573 V_{CC} = 3.3 V ± 0.3 V MIN	SN74LVT573 V_{CC} = 3.3 V ± 0.3 V MAX	SN74LVT573 V_{CC} = 2.7 V MIN	UNIT
t_w	Pulse duration, LE high		3.3		3.3	3.3		3.3	ns
t_{su}	Setup time, data before LE↓	High or low	0.7		0.6	0.7		0.6	ns
t_h	Hold time, data after LE↓	High or low	1.6		1.8	1.6		1.8	ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT573			SN74LVT573				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	D	Q	1	4.4	4.9	1	2.5	4.2	4.7	ns
t_{PHL}			1	4.5	5.4	1	2.7	4.3	5.2	
t_{PLH}	LE	Q	1.6	5.8	6.5	1.6	3.5	5.6	6.3	ns
t_{PHL}			2.5	6.7	7.4	2.5	4.3	6.5	7.2	
t_{PZH}	$\overline{OE}$	Q	1	5.3	6.4	1	2.8	5.1	6.2	ns
t_{PZL}			1.3	5.7	6.8	1.3	3.3	5.5	6.6	
t_{PHZ}	$\overline{OE}$	Q	2	5.9	6.9	2	3.7	5.7	6.7	ns
t_{PLZ}			1.5	4.8	5.3	1.5	3	4.6	5.1	

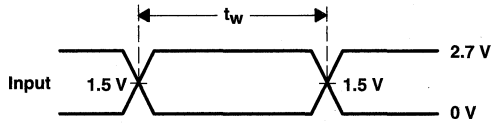
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

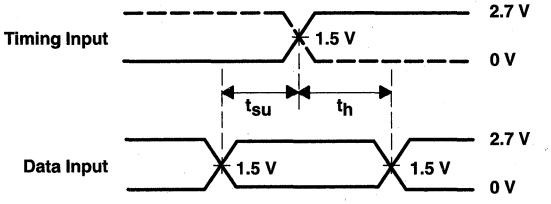


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

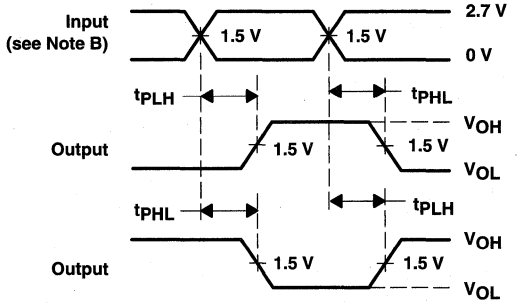
LOAD CIRCUIT FOR OUTPUTS



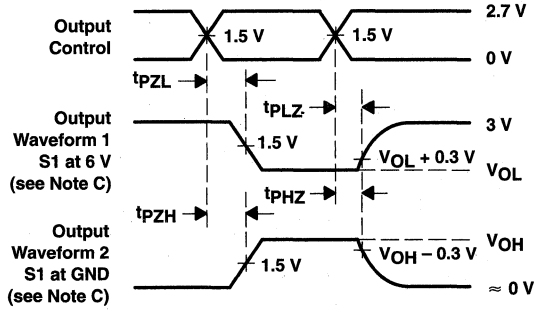
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



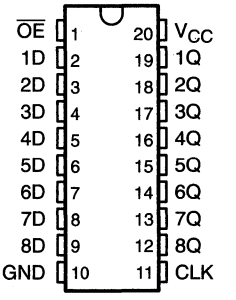
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

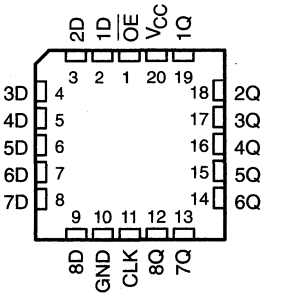
Figure 1. Load Circuit and Voltage Waveforms

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

SN54LVT574 . . . J PACKAGE
SN74LVT574 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT574 . . . FK PACKAGE
(TOP VIEW)



description

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVT574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

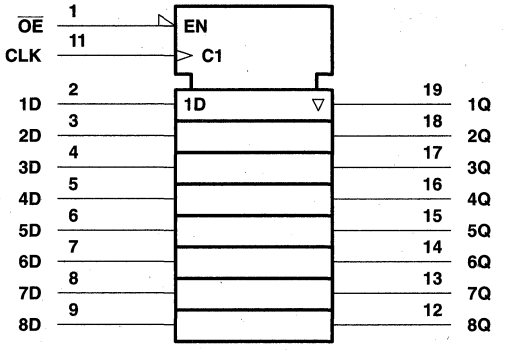
The SN74LVT574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT574 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT574 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

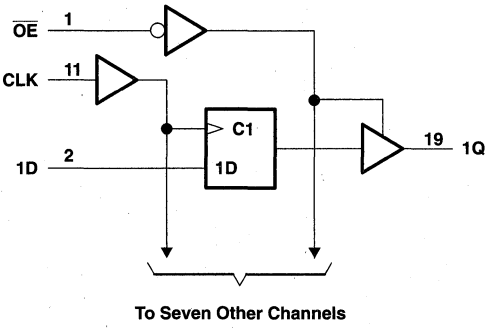
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT574 ..... 96 mA
SN74LVT574 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT574 ..... 48 mA
SN74LVT574 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
PW package ..... 0.6 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT574		SN74LVT574		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT574			SN74LVT574			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0	Data pins			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V	Data inputs	–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.19		0.13	0.19	mA
			Outputs low		8.7	12		8.7	12	
			Outputs disabled		0.13	0.19		0.13	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

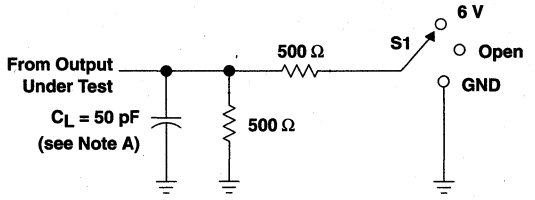
			SN54LVT574				SN74LVT574				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	High or low	2		2.4		2		2.4		ns
t_h	Hold time, data after CLK↑	High or low	0.3		0		0.3		0		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT574				SN74LVT574					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150		150		150			150		MHz
t_{PLH}	CLK	Q	1.7	5.6		6.4	1.7	3.6	5.4		6.2	ns
t_{PHL}			2.4	6.1		6.8	2.4	4.3	5.9		6.6	
t_{PZH}	$\overline{OE}$	Q	1	5		6.1	1	2.9	4.8		5.9	ns
t_{PZL}			1.3	5.3		6.4	1.3	3.4	5.1		6.2	
t_{PHZ}	$\overline{OE}$	Q	1.9	5.7		6.1	1.9	4	5.5		5.9	ns
t_{PLZ}			1.7	4.7		4.7	1.7	3.2	4.5		4.5	

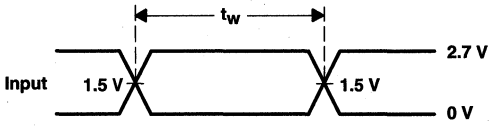
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

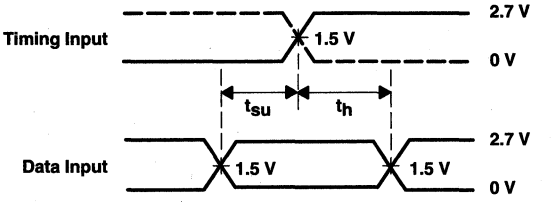


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

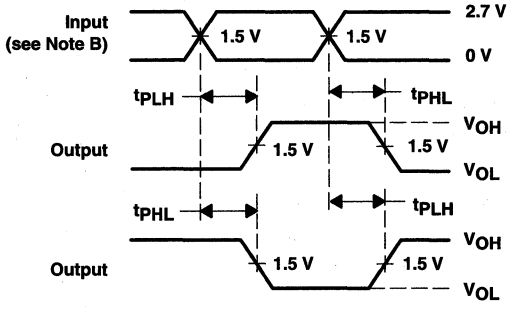
LOAD CIRCUIT FOR OUTPUTS



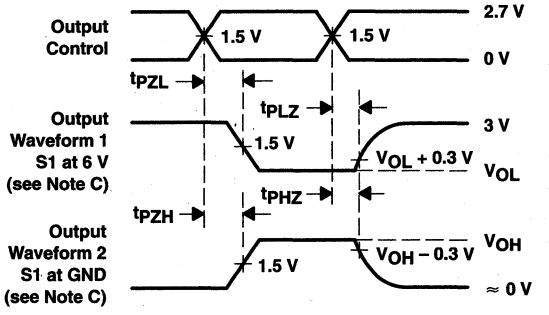
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



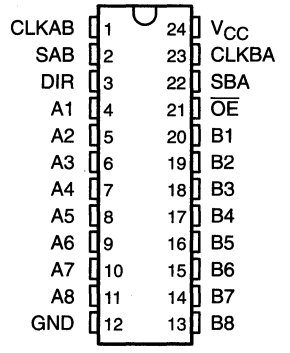
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

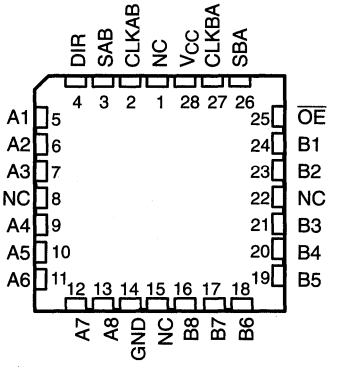
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT646 . . . JT PACKAGE
SN74LVT646 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT646 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

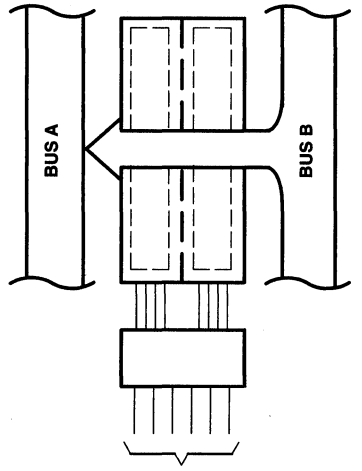
description (continued)

The SN54LVT646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT646 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

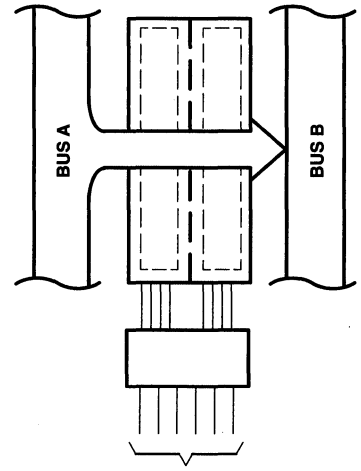
INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



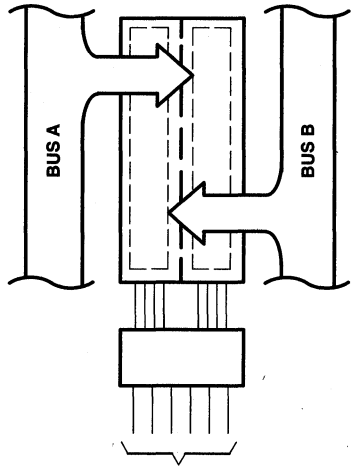
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



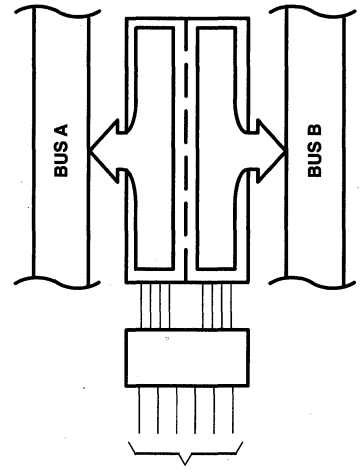
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



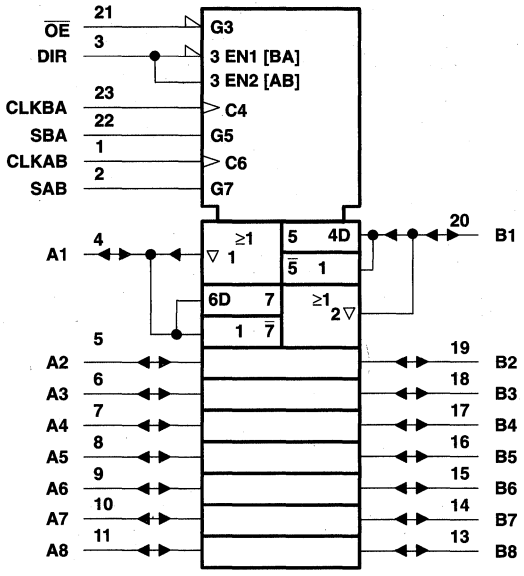
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

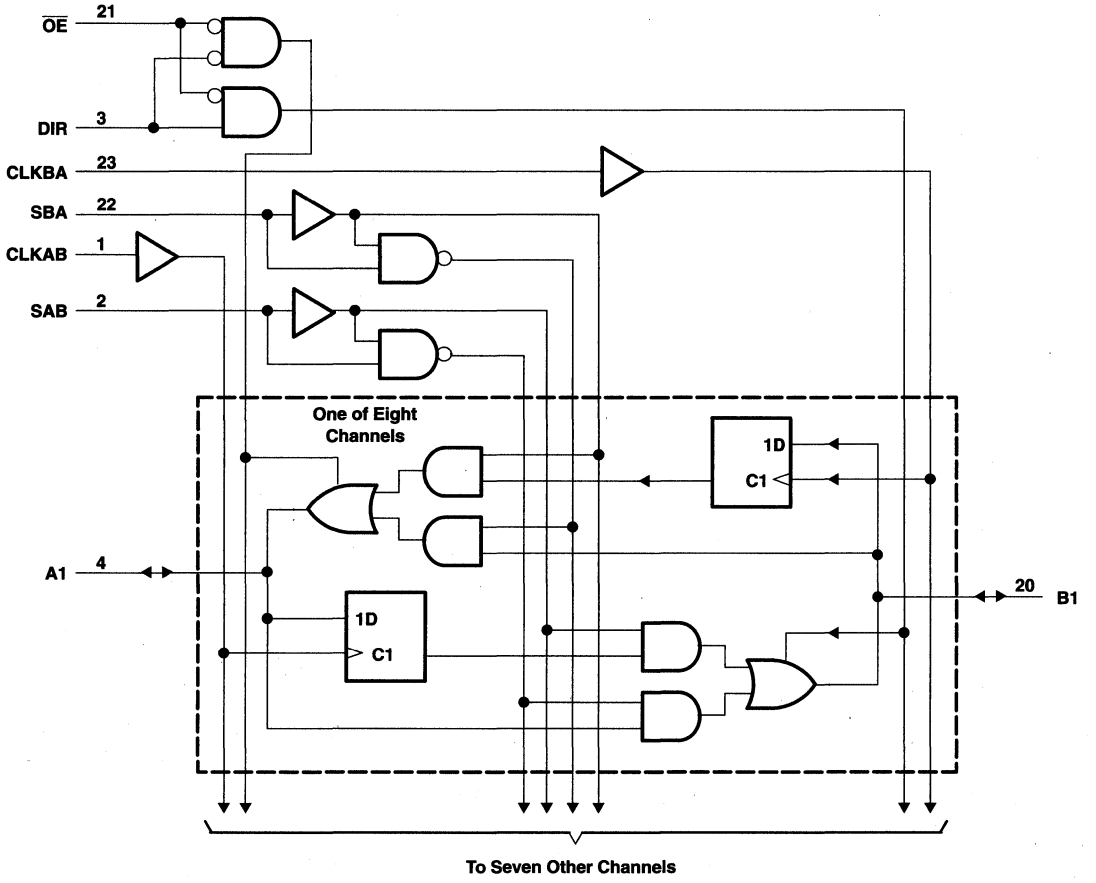
Pin numbers shown are for the DB, DW, JT, and PW packages.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT646 ..... 96 mA
SN74LVT646 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT646 ..... 48 mA
SN74LVT646 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
PW package ..... 0.65 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT646		SN74LVT646		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT646			SN74LVT646			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§			100			20	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.5		0.13	0.19	mA
			Outputs low		8.8	14		8.8	12	
			Outputs disabled		0.13	0.5		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4.5			4.5		pF
C_{io}	V_O = 3 V or 0				11			11		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

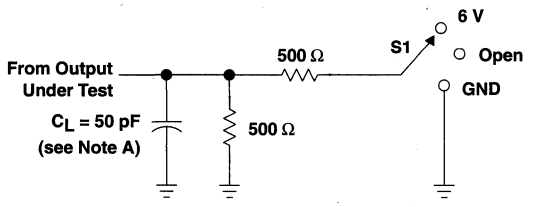
			SN54LVT646				SN74LVT646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	High	1.5		1.5		1.3		1.3		ns
		Low	2.5		3		2		2.4		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑		0.9		0.9		0.4		0.4		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT646			SN74LVT646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
f_{max}			150			150				MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.2	5.9	6.9	1.8	3.8	5.7	6.7	ns
t_{PHL}			1.2	5.9	6.6	2.1	3.8	5.7	6.4	
t_{PLH}	A or B	B or A	0.8	4.9	5.6	1.3	2.8	4.7	5.4	ns
t_{PHL}			0.6	4.8	5.5	1	2.7	4.6	5.3	
t_{PLH}	SBA or SAB‡	A or B	1	6.4	7.4	1.4	3.7	6.2	7.2	ns
t_{PHL}			1	6.4	7	1.4	3.8	6.2	6.8	
t_{PZH}	$\overline{OE}$	A or B	0.6	6	7.4	1	3	5.8	7.2	ns
t_{PZL}			0.6	6.2	7.5	1	3.2	6	7.3	
t_{PHZ}	$\overline{OE}$	A or B	1.4	6.7	7.1	2.3	4.3	6.5	6.9	ns
t_{PLZ}			1.4	6.4	6.5	2.2	3.8	5.8	5.9	
t_{PZH}	DIR	A or B	0.6	6.7	7.7	1	3.4	6.5	7.5	ns
t_{PZL}			0.8	6.5	7.3	1.2	3.4	6.3	7.1	
t_{PHZ}	DIR	A or B	0.8	7.4	8.3	1.7	4.1	7.2	8.1*	ns
t_{PLZ}			1	6.7	7	1.5	3.5	5.8	6.3	

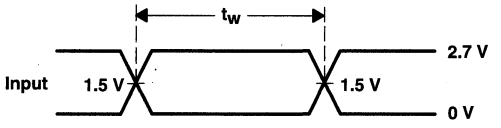
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

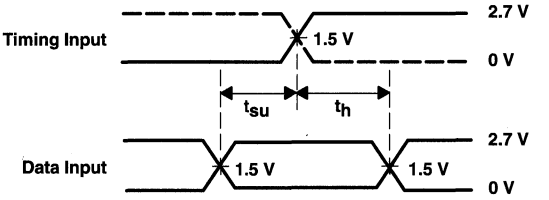


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

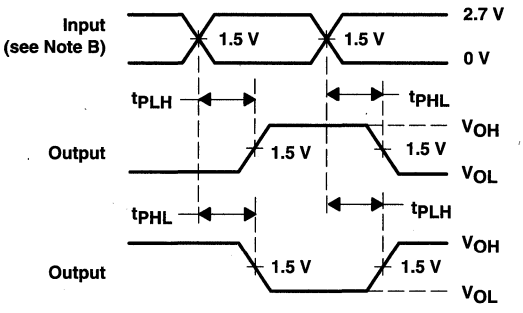
LOAD CIRCUIT FOR OUTPUTS



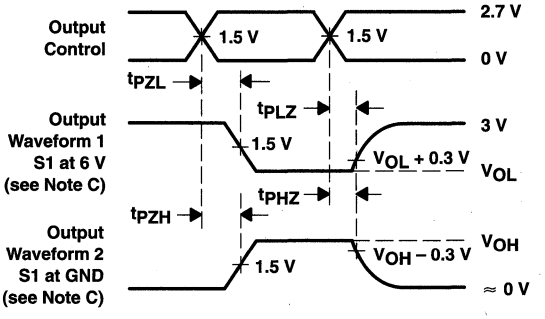
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



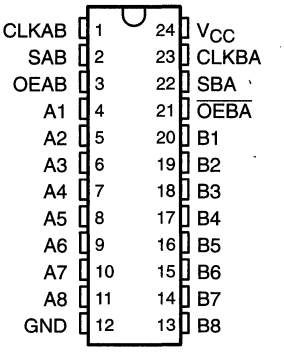
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

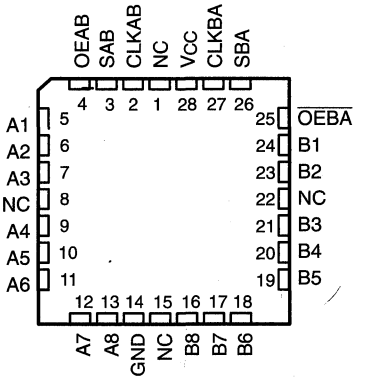
Figure 2. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT652 . . . JT PACKAGE
SN74LVT652 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT652 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

description (continued)

The SN74LVT652 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

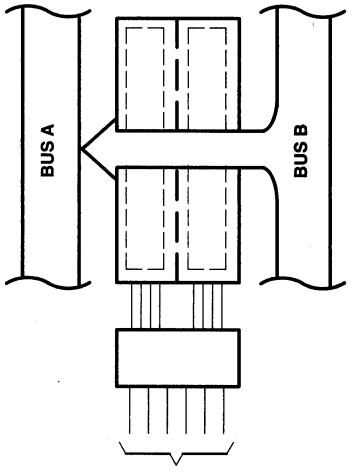
The SN54LVT652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT652 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

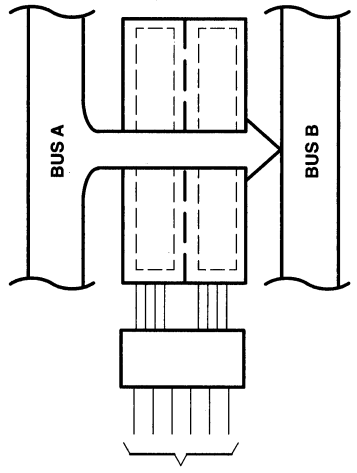
† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.



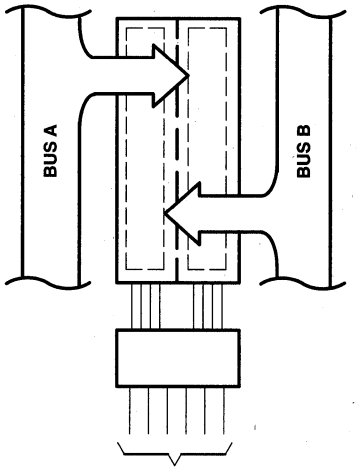
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



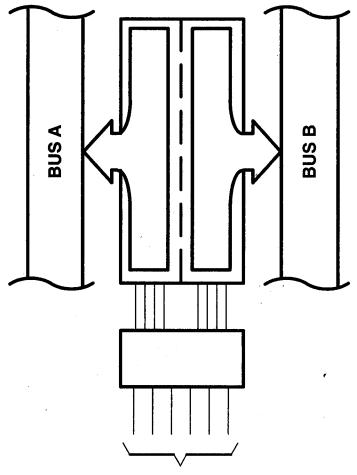
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



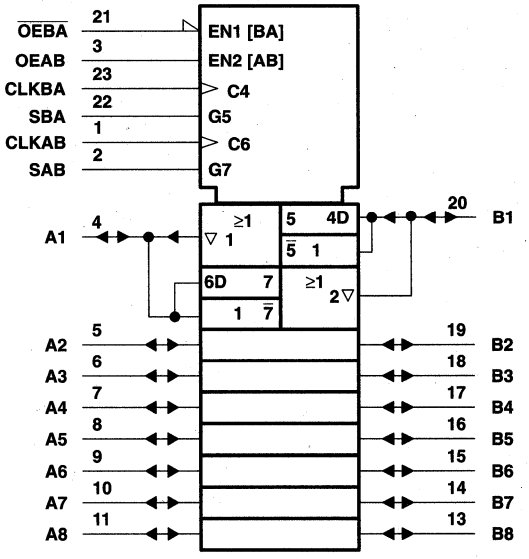
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

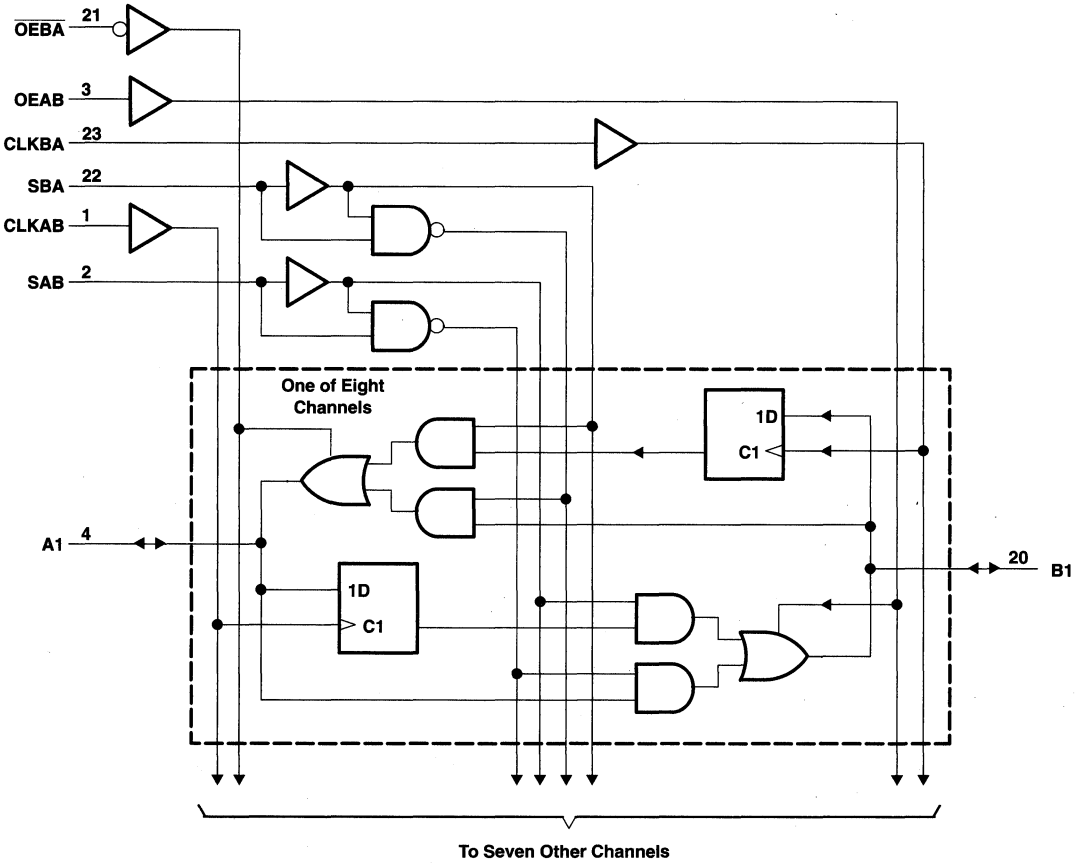
Pin numbers shown are for the DB, DW, JT, and PW packages.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT652 ..... 96 mA
SN74LVT652 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT652 ..... 48 mA
SN74LVT652 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
PW package ..... 0.65 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT652		SN74LVT652		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT652			SN74LVT652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§			20			20	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.19		0.13	0.19	mA
			Outputs low		8.8	12		8.8	12	
			Outputs disabled		0.13	0.19		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4.5			4.5		pF
C_{io}	V_O = 3 V or 0				11			11		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

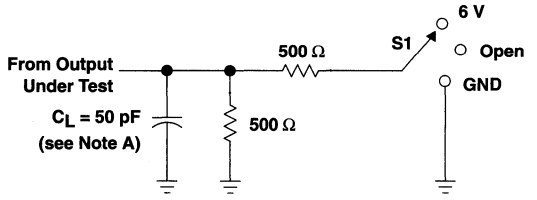
			SN54LVT652				SN74LVT652				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low						3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high					1.2		1.2		ns
		Data low					2		2.5		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑						0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT652				SN74LVT652					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}							150			150		MHz
t_{PLH}	CLKBA or CLKAB	A or B					1.8	3.7	6		6.9	ns
t_{PHL}							2	3.7	5.7		6.4	
t_{PLH}	A or B	B or A					1.2	2.8	4.7		5.5	ns
t_{PHL}							1	2.6	4.6		5.3	
t_{PLH}	SBA or SAB‡	A or B					1.4	3.7	6.4		7.6	ns
t_{PHL}							1.4	4	6.2		6.8	
t_{PZH}	$\overline{OEBA}$	A					1	2.9	5.8		7.2	ns
t_{PZL}							1	3	6		7.3	
t_{PHZ}	$\overline{OEBA}$	A					2.2	3.9	6.5		6.9	ns
t_{PLZ}							1.8	3.2	5.8		5.9	
t_{PZH}	OEAB	B					1	3.3	6.5		7.5	ns
t_{PZL}							1.2	3.4	6.3		7.1	
t_{PHZ}	OEAB	B					1.7	4.5	7.2		8.1	ns
t_{PLZ}							1.5	3.8	5.8		6.3	

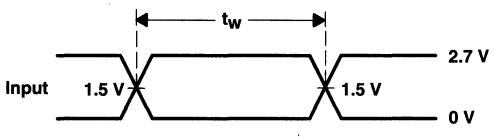
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

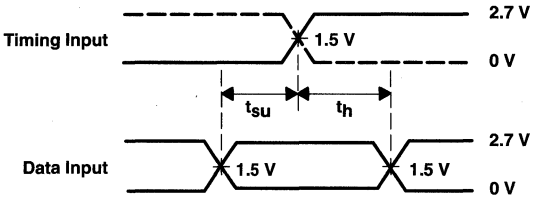


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

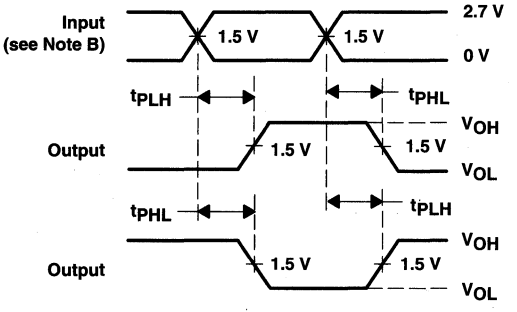
LOAD CIRCUIT FOR OUTPUTS



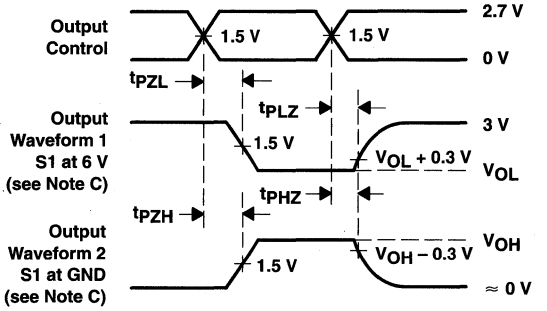
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



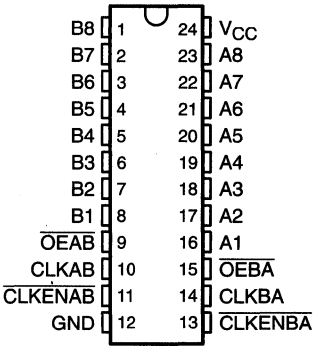
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

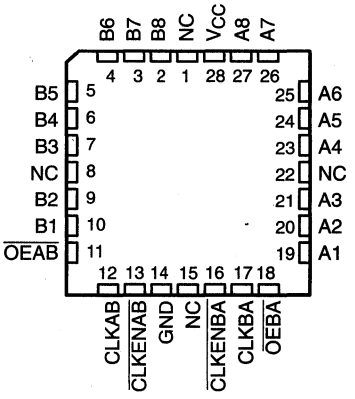
Figure 2. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT2952 . . . JT PACKAGE
SN74LVT2952 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT2952 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT2952 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

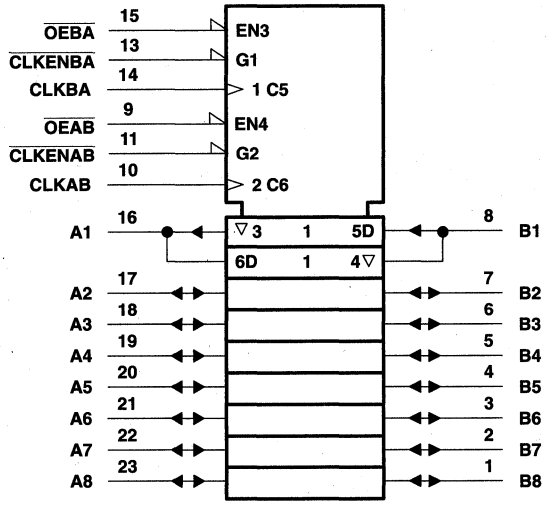
The SN54LVT2952 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT2952 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	B
H	X	L	X	B_0‡
X	H or L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

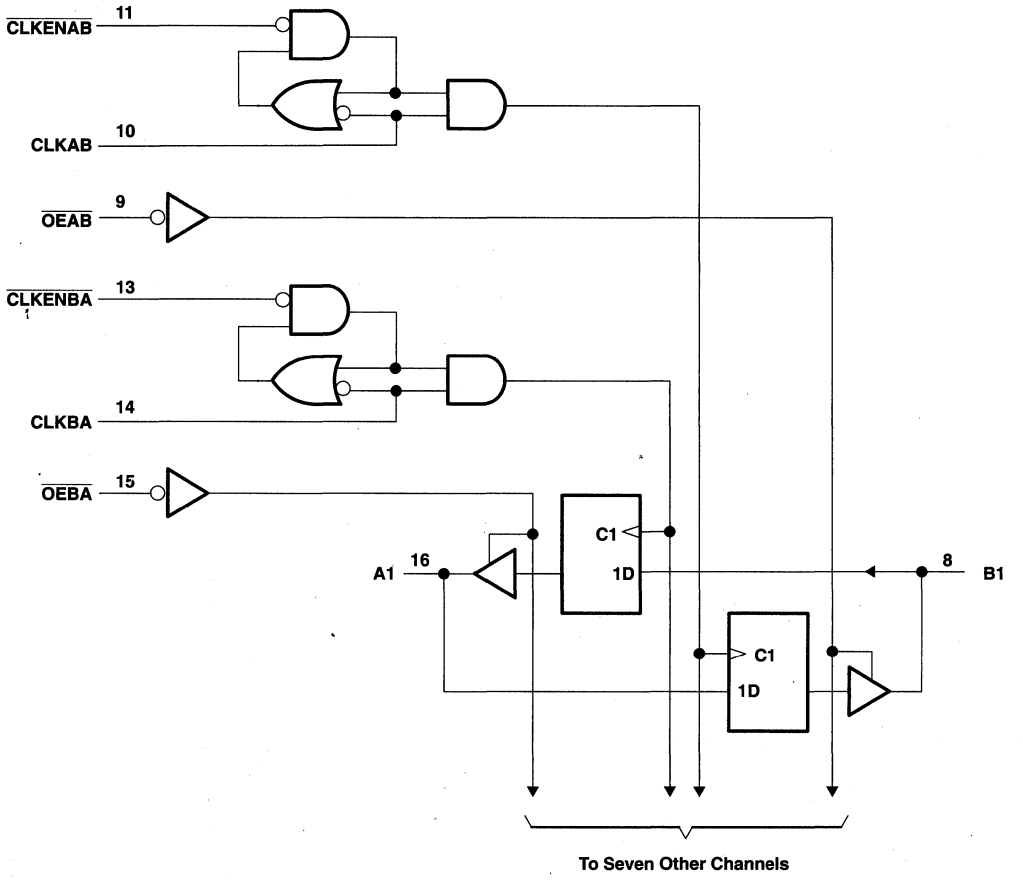
† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.
‡ Level of B before the indicated steady-state input conditions were established.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT2952 ..... 96 mA
SN74LVT2952 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT2952 ..... 48 mA
SN74LVT2952 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
PW package ..... 0.65 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT2952		SN74LVT2952		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT2952			SN74LVT2952			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = − 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§			20			20	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.19		0.13	0.19	mA
			Outputs low		8.8	12		8.8	12	
			Outputs disabled		0.13	0.19		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_I = 3 V or 0				4.5			4.5		pF
C_{io}	V_O = 3 V or 0				11.5			11.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirement over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

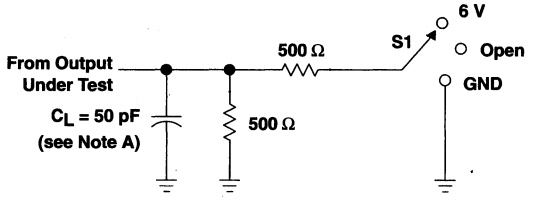
				SN54LVT2952				SN74LVT2952				UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency								150		150	MHz
t_w	Pulse duration		CLK high					3.3		3.3		ns
			CLK low					3.3		3.3		
t_{su}	Setup time before CLK↑	A or B	High	2.6		2.9		2.5		2.8		ns
			Low	2.6		3.1		2.5		3		
		$\overline{CE}$	High	0.9		0.8		0.9		0.8		
			Low	2.5		2.7		2.4		2.7		
t_h	Hold time after CLK↑	A or B		1.5		0.7		1.5		0.7		ns
		$\overline{CE}$		2.6		2.6		2.5		2.6		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT2952					SN74LVT2952					UNIT
			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP†	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}								150			150		MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.3		6.4	2.7	7.4	1.3	3.6	6.1	2.7	7.1	ns
t_{PHL}			1.8		6.1	2.7	7	1.8	3.7	6	2.7	6.9	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1		6.3	2.6	7.3	1	3.2	5.6	2.6	6.7	ns
t_{PZL}			1.1		6.6	2.9	8.2	1.2	3.2	6.5	2.9	8	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1		7	2.7	7.6	1	4.1	6.3	2.7	6.9	ns
t_{PLZ}			1.6		5.8	1.7	6	1.6	3.3	5.1	1.8	5.3	

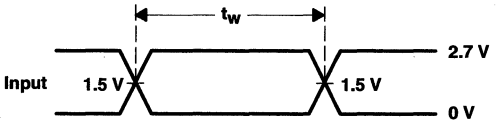
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

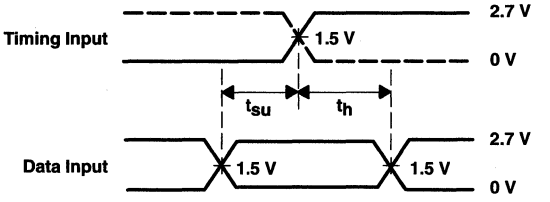


LOAD CIRCUIT FOR OUTPUTS

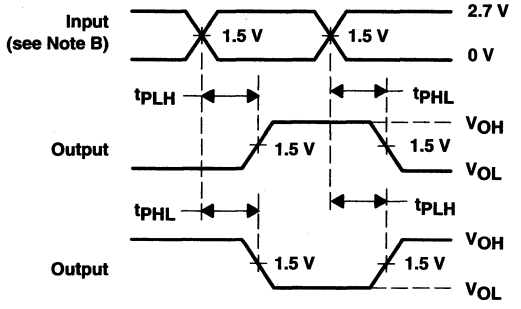
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



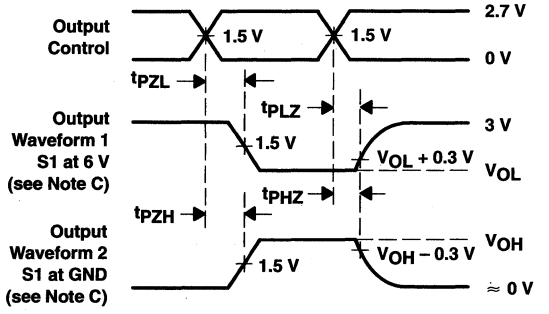
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

LVT Widebus™

Features

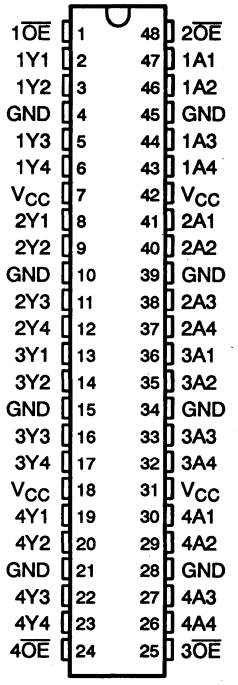
- EPIC-IIB™ BiCMOS process with special low-voltage enhancements
- Mixed-mode circuitry
- Expanded V_{CC} range from 2.7 V to 3.6 V
- Bus-hold circuitry
- Power-on-demand active feedback circuitry
- Widebus™ and UBT™ architectures
- JEDEC SSOP (Widebus™) and EIAJ TSSOP (Shrink Widebus™) packaging
- TI has established an alternate source

Benefits

- 3.3-V logic family with equivalent speed and drive performance of 5-V ABT logic family – not just a recharacterized or scaled CMOS
- Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
- AC performance optimized for both regulated supply and unregulated battery operation
- Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Reduces disabled static power consumption (I_{CCZ}) to as little as 0.1 mA for power-conscious portable and battery-powered equipment
- 16- and 18-bit densities for flexible integration
- Space-saving and height-saving surface-mount package options, pin compatible with existing 5-V families for easy conversion
- Standardization that comes from a common product approach

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16244A . . . WD PACKAGE
SN74LVT16244A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16244A is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

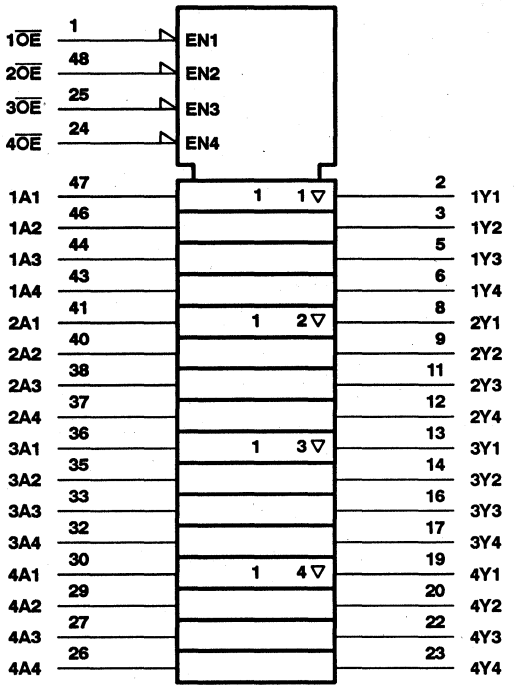
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16244A is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16244A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16244A is characterized for operation from −40°C to 85°C.

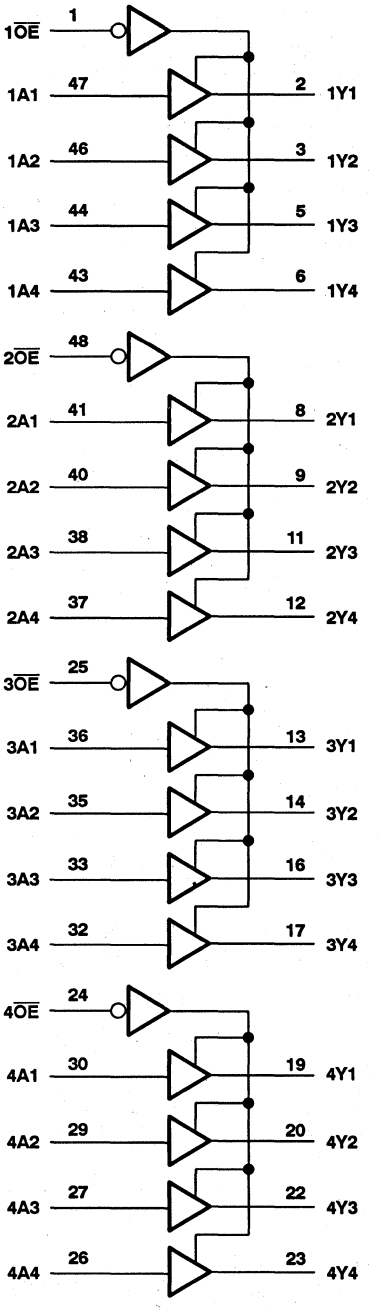
Widebus is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16244A ..... 96 mA
SN74LVT16244A ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16244A ..... 48 mA
SN74LVT16244A ..... 64 mA
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT16244A		SN74LVT16244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

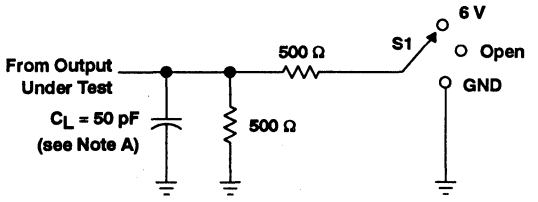
PARAMETER	TEST CONDITIONS			SN54LVT16244A		SN74LVT16244A			UNIT
				MIN	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2					
	V_{CC} = 3 V,	I_{OH} = –32 mA				2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA						0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins		1			1	
	V_{CC} = 3.6 V,	V_I = 0			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75		75			µA
		V_I = 2 V		–75		–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.09			0.09	mA
			Outputs low		5			5	
			Outputs disabled		0.09			0.09	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2			0.2	mA
C_i	V_I = 3 V or 0						4		pF
C_o	V_O = 3 V or 0						10		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

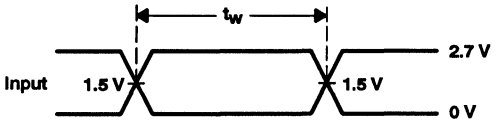
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16244A				SN74LVT16244A				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN MAX	
t_{PLH}	A	Y	1	4.2		5.1	1	2.3	4.1	5	ns
t_{PHL}			1	4.2		5.3	1	2.3	4.1	5.2	
t_{PZH}	$\overline{OE}$	Y	1	5.3		6.4	1	2.6	5.2	6.3	ns
t_{PZL}			1	5.5		6.8	1	2.6	5.2	6.7	
t_{PHZ}	$\overline{OE}$	Y	2.1	5.9		6.4	2.2	3.9	5.7	6.3	ns
t_{PLZ}			1.9	5.3		5.7	2	3.7	5.1	5.6	

PARAMETER MEASUREMENT INFORMATION

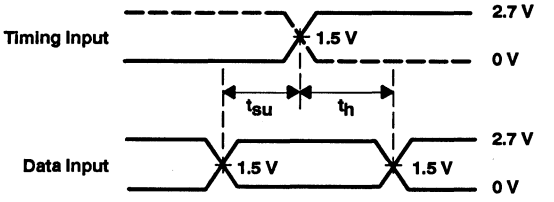


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

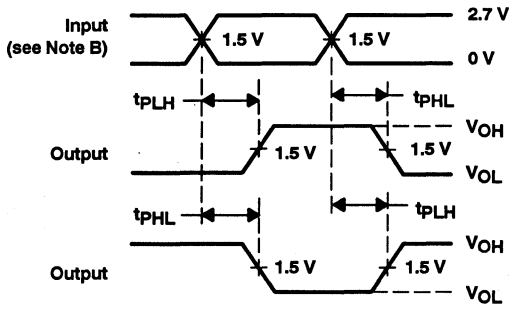
LOAD CIRCUIT FOR OUTPUTS



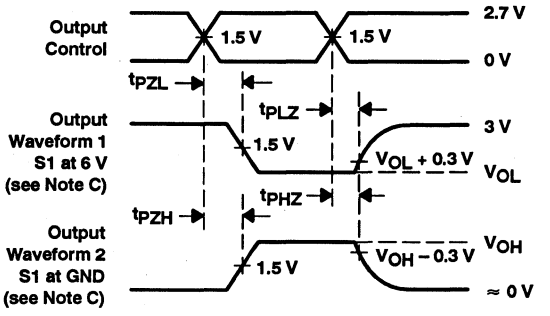
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



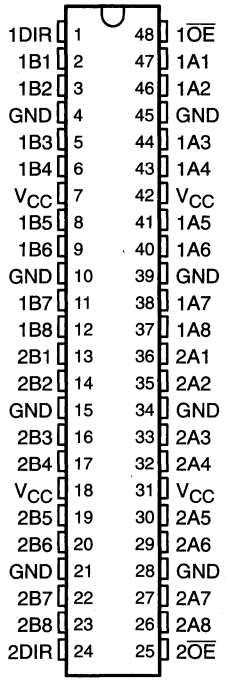
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16245 . . . WD PACKAGE
SN74LVT16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

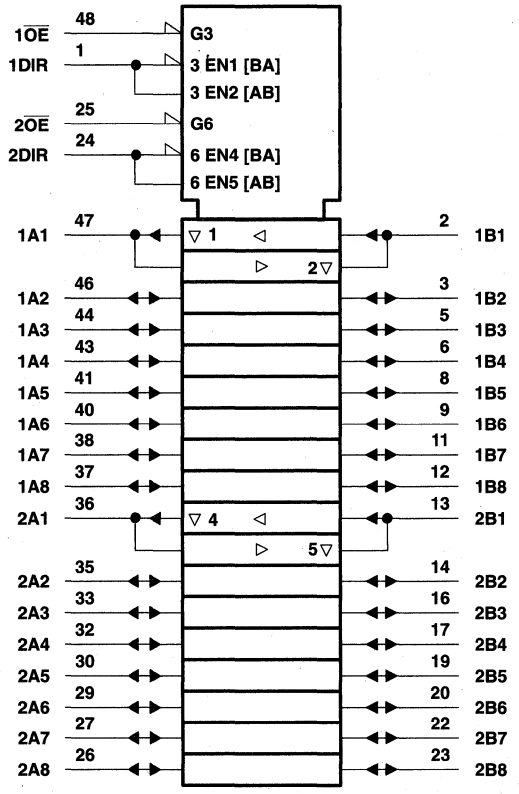
The SN54LVT16245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16245 is characterized for operation from −40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each 8-bit section)

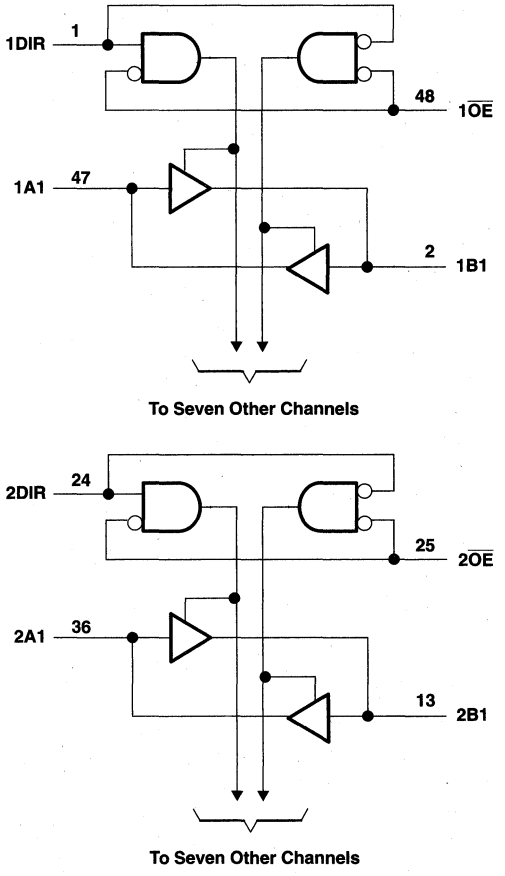
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16245 ..... 96 mA
SN74LVT16245 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16245 ..... 48 mA
SN74LVT16245 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT16245		SN74LVT16245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16245			SN74LVT16245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§			20			20	
	V_{CC} = 3.6 V,	V_I = V_{CC}				1			1	
	V_{CC} = 3.6 V,	V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF

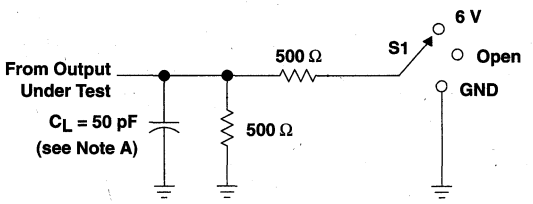
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16245				SN74LVT16245					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A or B	B or A					1	2.4	4.1		5	ns
t_{PHL}							1	2.3	4.1		5.2	
t_{PZH}	$\overline{OE}$	A or B					1	3	5.3		6.3	ns
t_{PZL}							1	3.1	5.2		6.7	
t_{PHZ}	$\overline{OE}$	A or B					2.7	4.6	6.4		7.2	ns
t_{PLZ}							2.6	4.3	5.8		6.1	

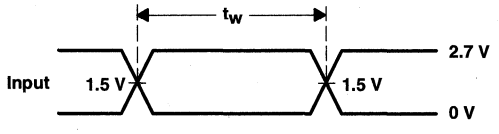
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

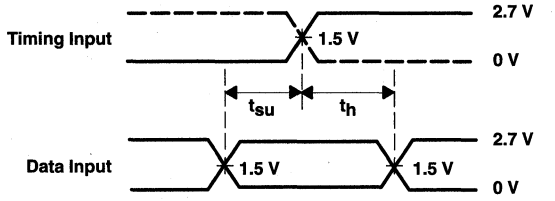


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

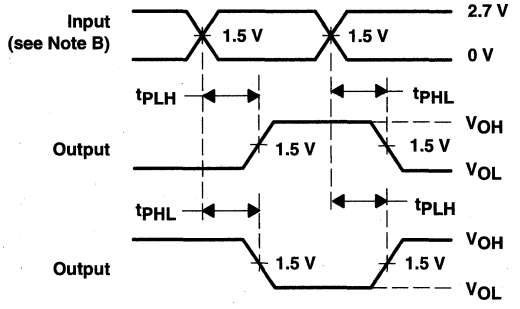
LOAD CIRCUIT FOR OUTPUTS



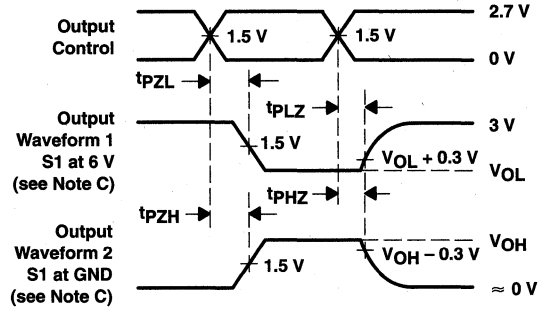
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



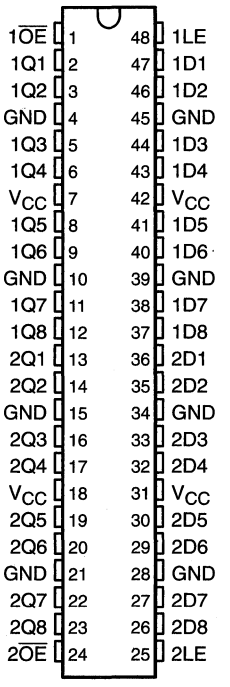
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16373 . . . WD PACKAGE
SN74LVT16373 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16373 is a 16-bit transparent D-type latch with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

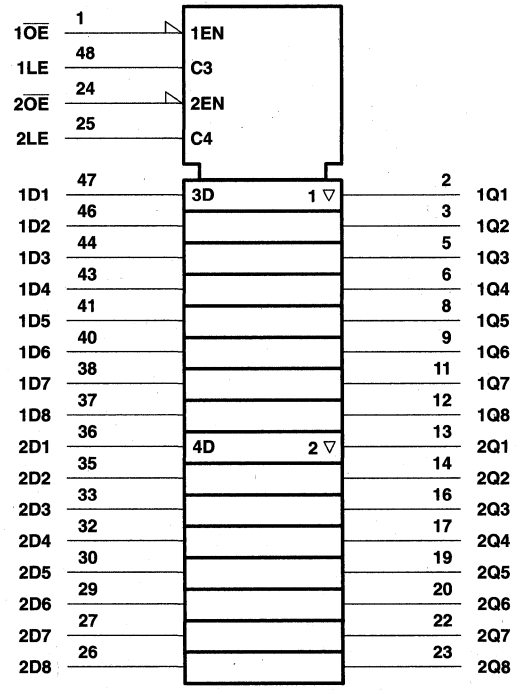
The SN74LVT16373 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16373 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

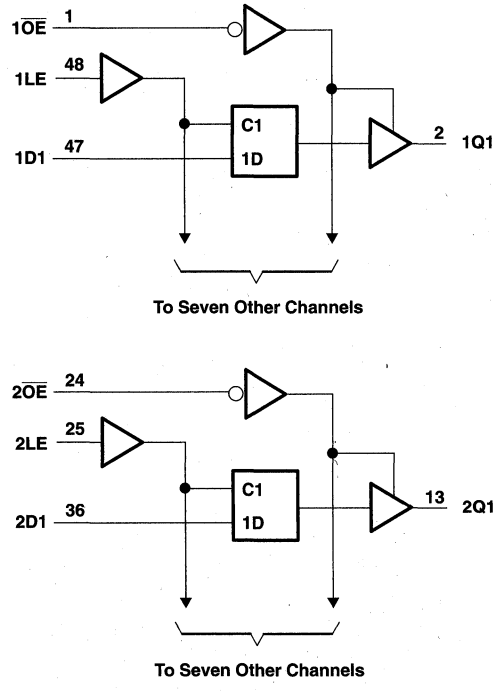
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16373 ..... 96 mA
SN74LVT16373 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16373 ..... 48 mA
SN74LVT16373 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT16373		SN74LVT16373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

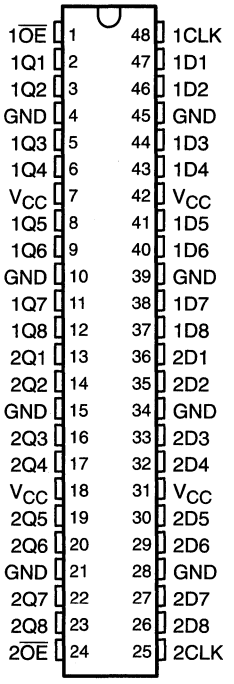
PARAMETER	TEST CONDITIONS			SN54LVT16373		SN74LVT16373		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2		0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins		1		1	
	V_{CC} = 3.6 V,	V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			5		5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–5		–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_o	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16374 . . . WD PACKAGE
SN74LVT16374 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'LVT16374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16374 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

Widebus is a trademark of Texas Instruments Incorporated.

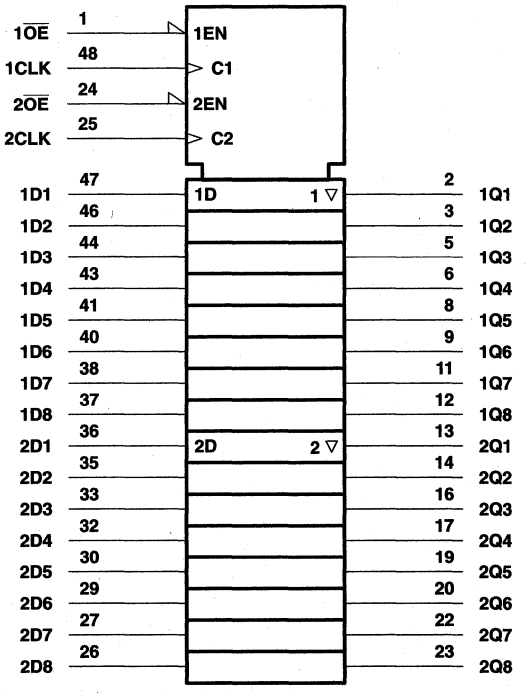
description (continued)

The SN54LVT16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

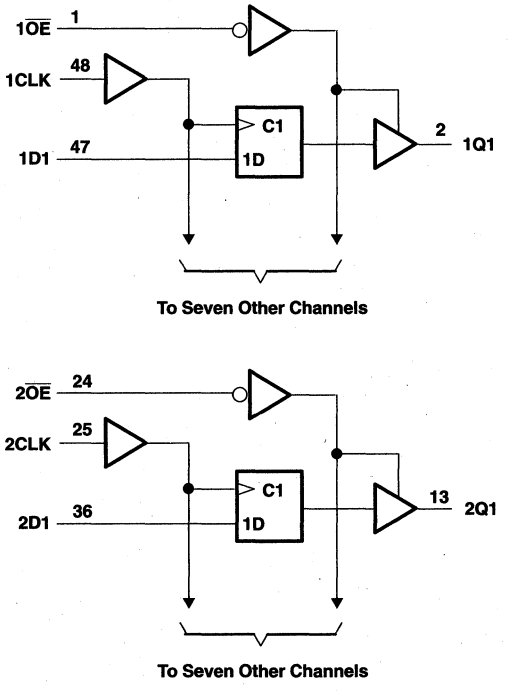
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16374 ..... 96 mA
SN74LVT16374 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16374 ..... 48 mA
SN74LVT16374 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT16374		SN74LVT16374		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

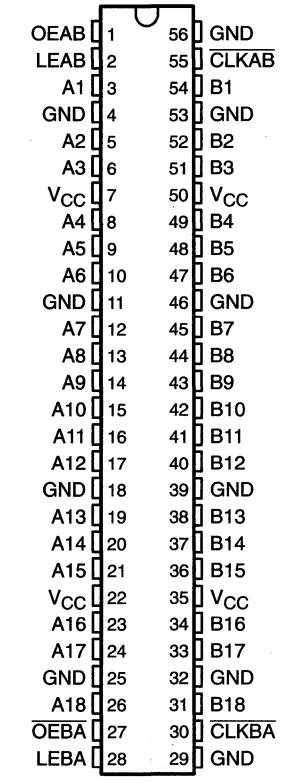
PARAMETER	TEST CONDITIONS			SN54LVT16374		SN74LVT16374		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2		0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins		1		1	
	V_{CC} = 3.6 V,	V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			5		5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–5		–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_o	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16500 . . . WD PACKAGE
SN74LVT16500 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16500 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus and UBT are trademarks of Texas Instruments Incorporated.

description (continued)

The SN74LVT16500 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16500 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16500 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	$\overline{\text{CLKAB}}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

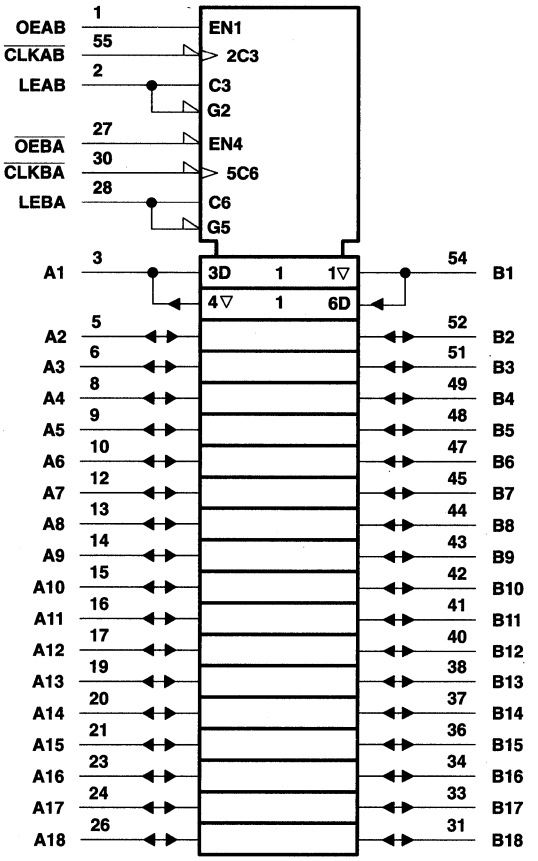
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low.

PRODUCT PREVIEW

logic symbol†

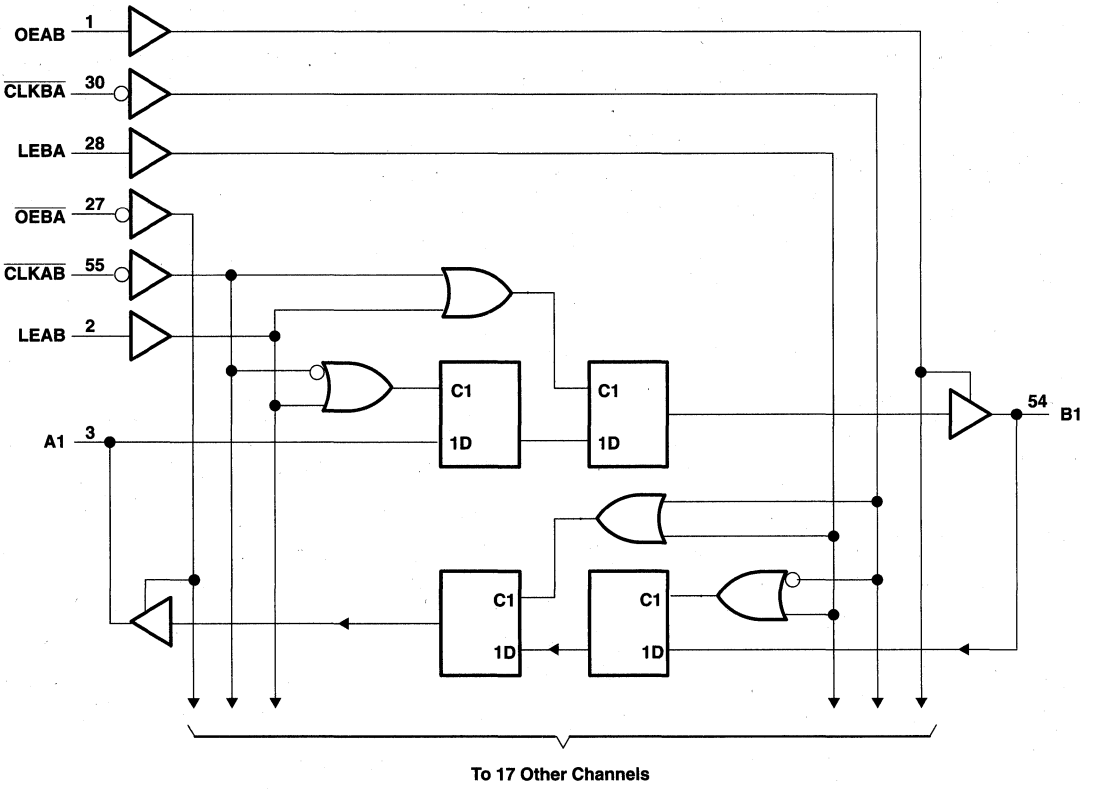


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16500 ..... 96 mA
SN74LVT16500 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16500 ..... 48 mA
SN74LVT16500 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT16500		SN74LVT16500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

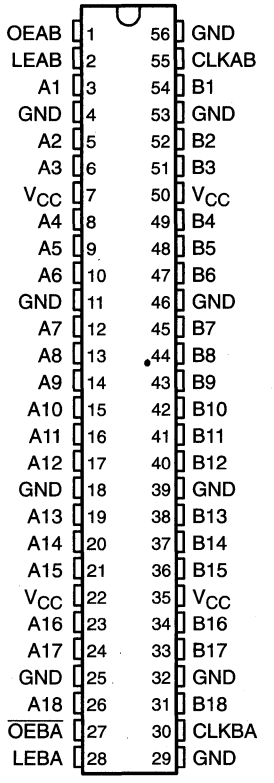
PARAMETER	TEST CONDITIONS			SN54LVT16500		SN74LVT16500		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2		0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§		20		20	
	V_{CC} = 3.6 V,	V_I = V_{CC}			1		1	
	V_{CC} = 3.6 V,	V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16501 . . . WD PACKAGE
SN74LVT16501 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16501 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus and UBT are trademarks of Texas Instruments Incorporated.

description (continued)

The SN74LVT16501 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16501 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16501 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

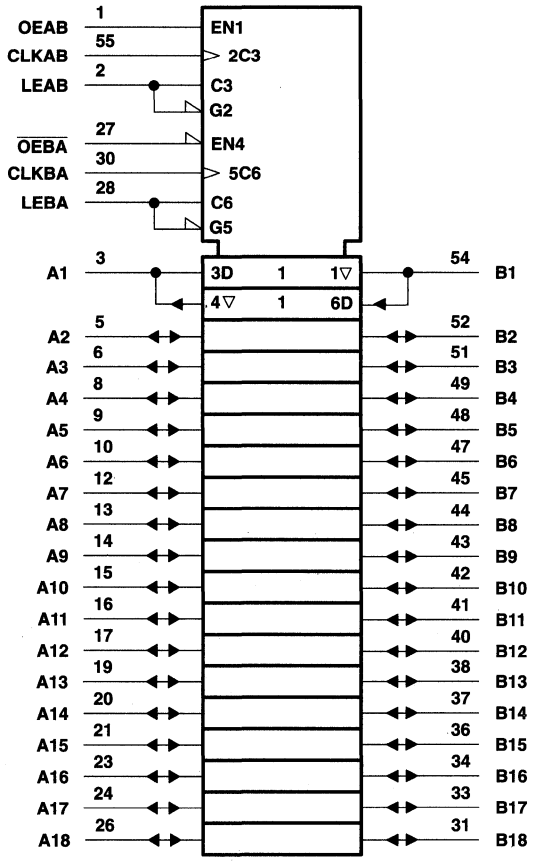
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

logic symbol†

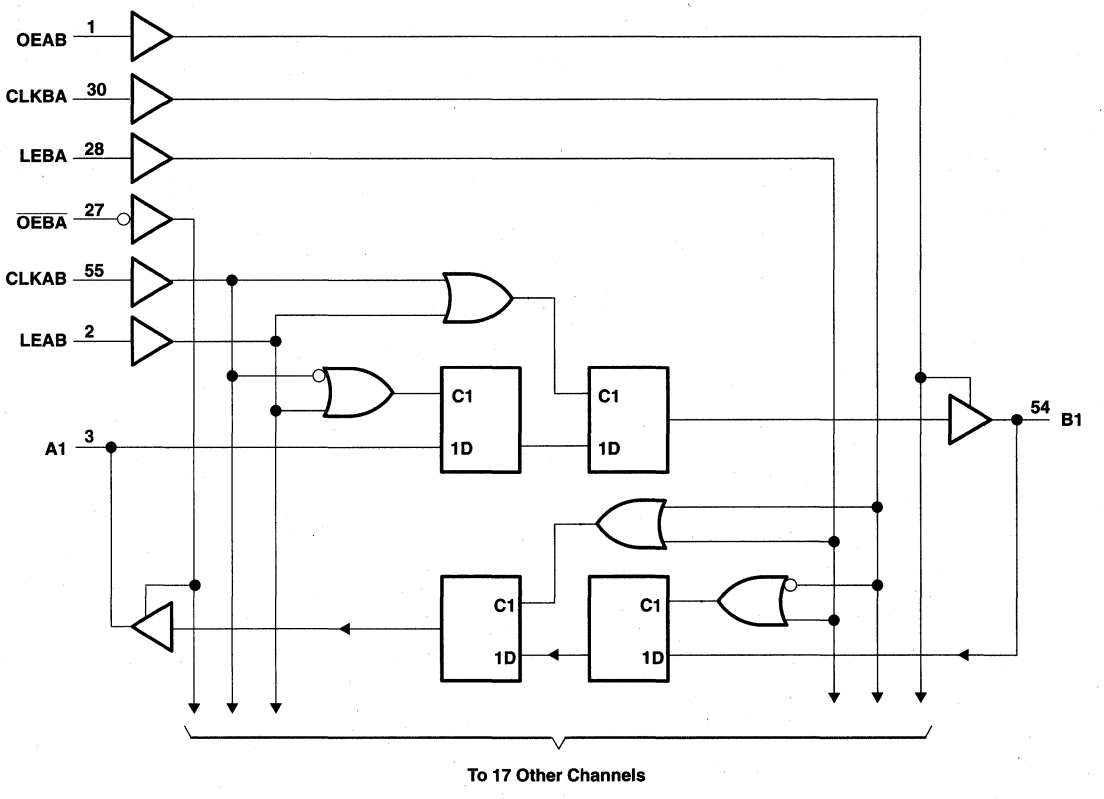


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16501 ..... 96 mA
SN74LVT16501 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16501 ..... 48 mA
SN74LVT16501 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT16501		SN74LVT16501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

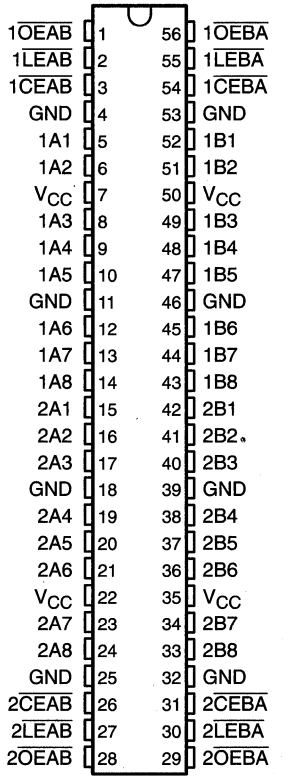
PARAMETER	TEST CONDITIONS			SN54LVT16501		SN74LVT16501		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2		0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§		20		20	
	V_{CC} = 3.6 V,	V_I = V_{CC}			1		1	
	V_{CC} = 3.6 V,	V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16543 . . . WD PACKAGE
SN74LVT16543 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16543 is a 16-bit registered transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

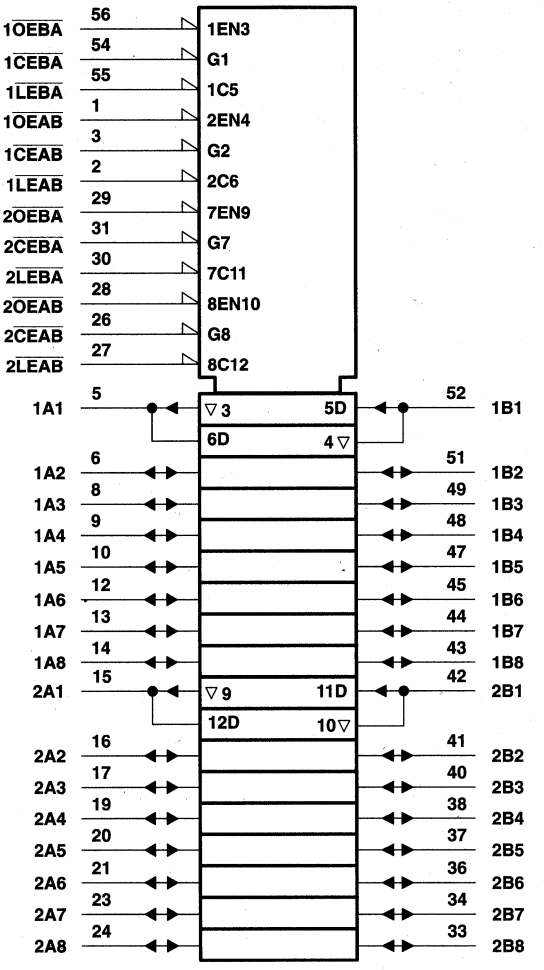
The SN74LVT16543 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16543 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16543 is characterized for operation from −40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated.

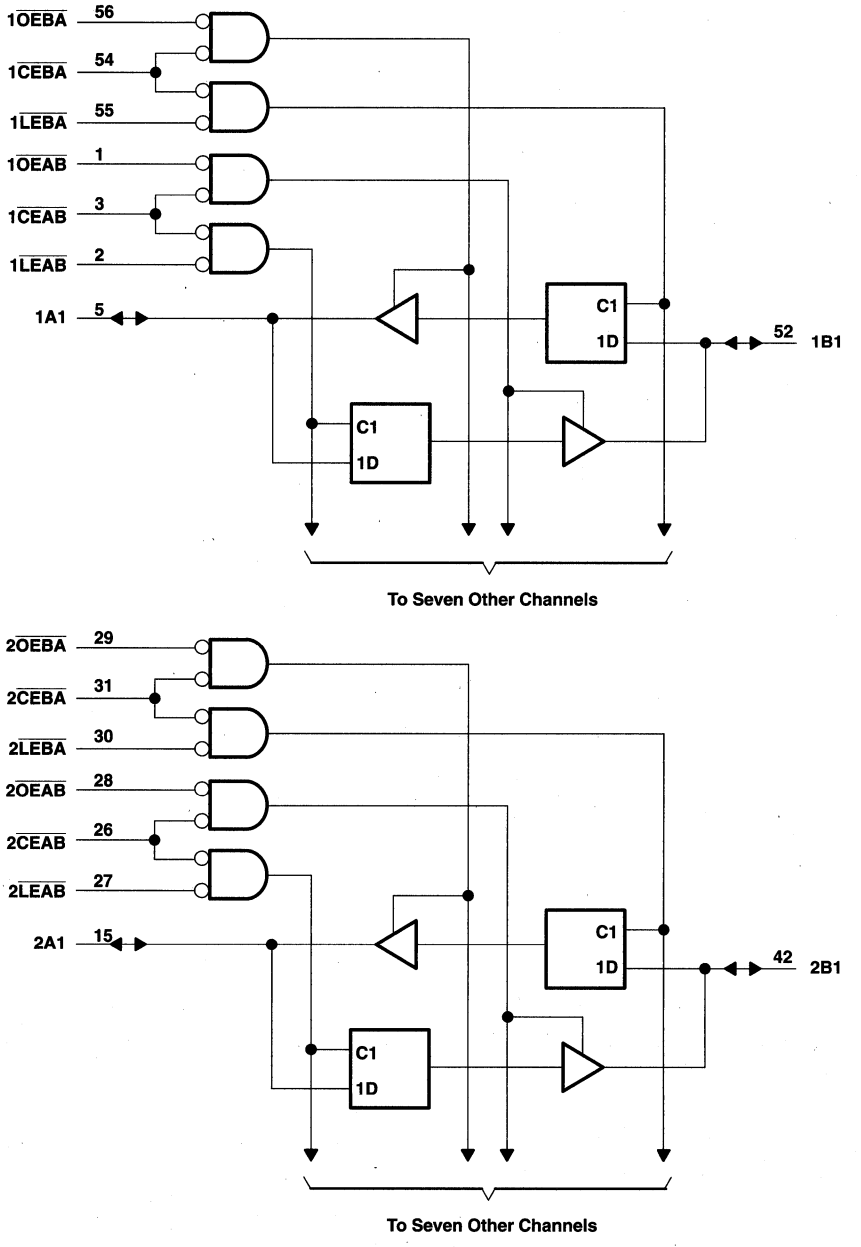
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE† (each 8-bit section)

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16543 ..... 96 mA
SN74LVT16543 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16543 ..... 48 mA
SN74LVT16543 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT16543		SN74LVT16543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}¶	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

¶ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

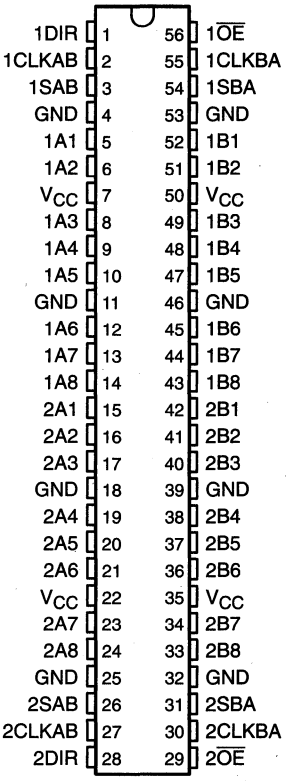
PARAMETER	TEST CONDITIONS			SN54LVT16543		SN74LVT16543		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2		0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§		20		20	
	V_{CC} = 3.6 V,	V_I = V_{CC}			1		1	
	V_{CC} = 3.6 V,	V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16646 . . . WD PACKAGE
SN74LVT16646 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16646 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

The SN74LVT16646 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

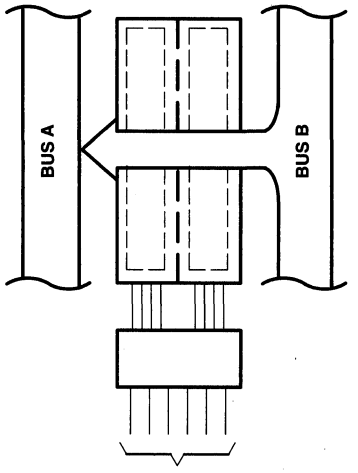
The SN54LVT16646 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16646 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

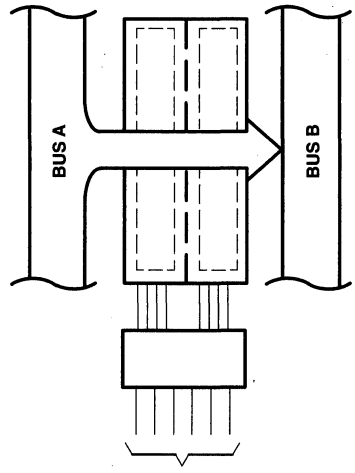
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

PRODUCT PREVIEW



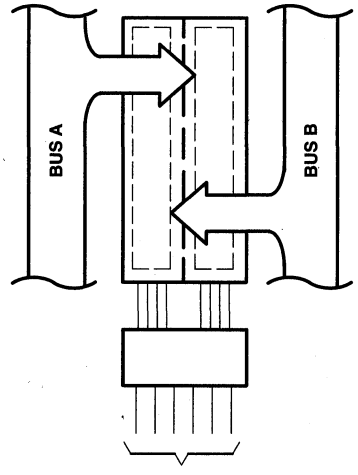
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



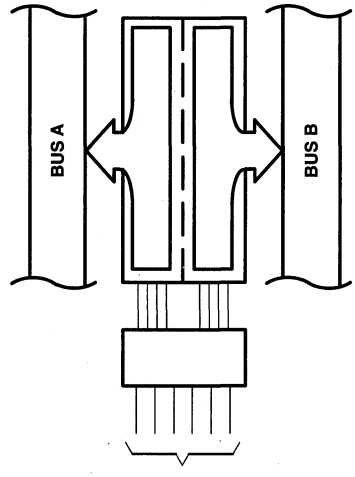
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

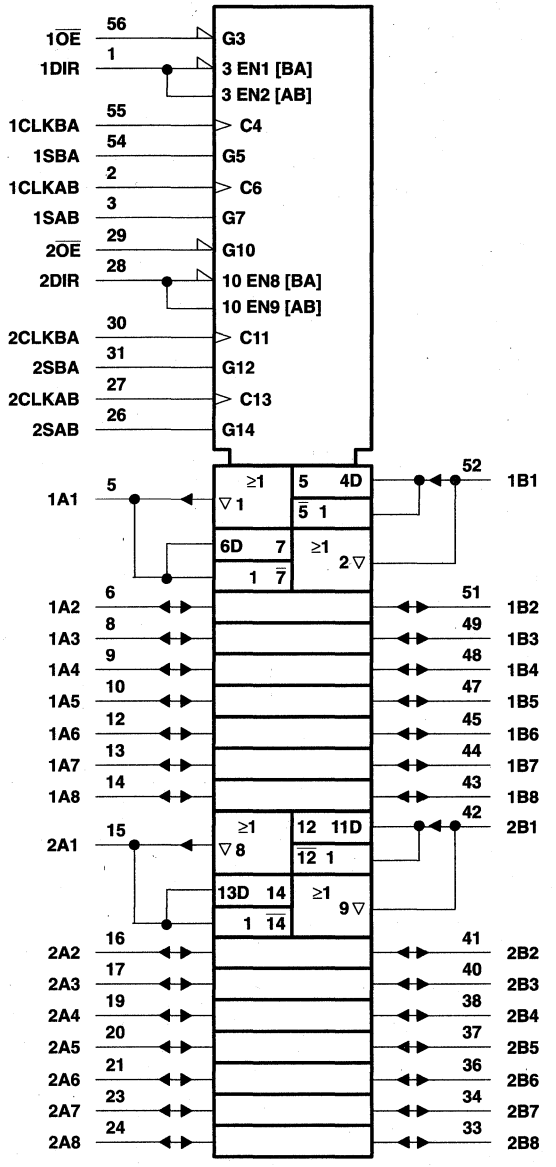
TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

PRODUCT PREVIEW

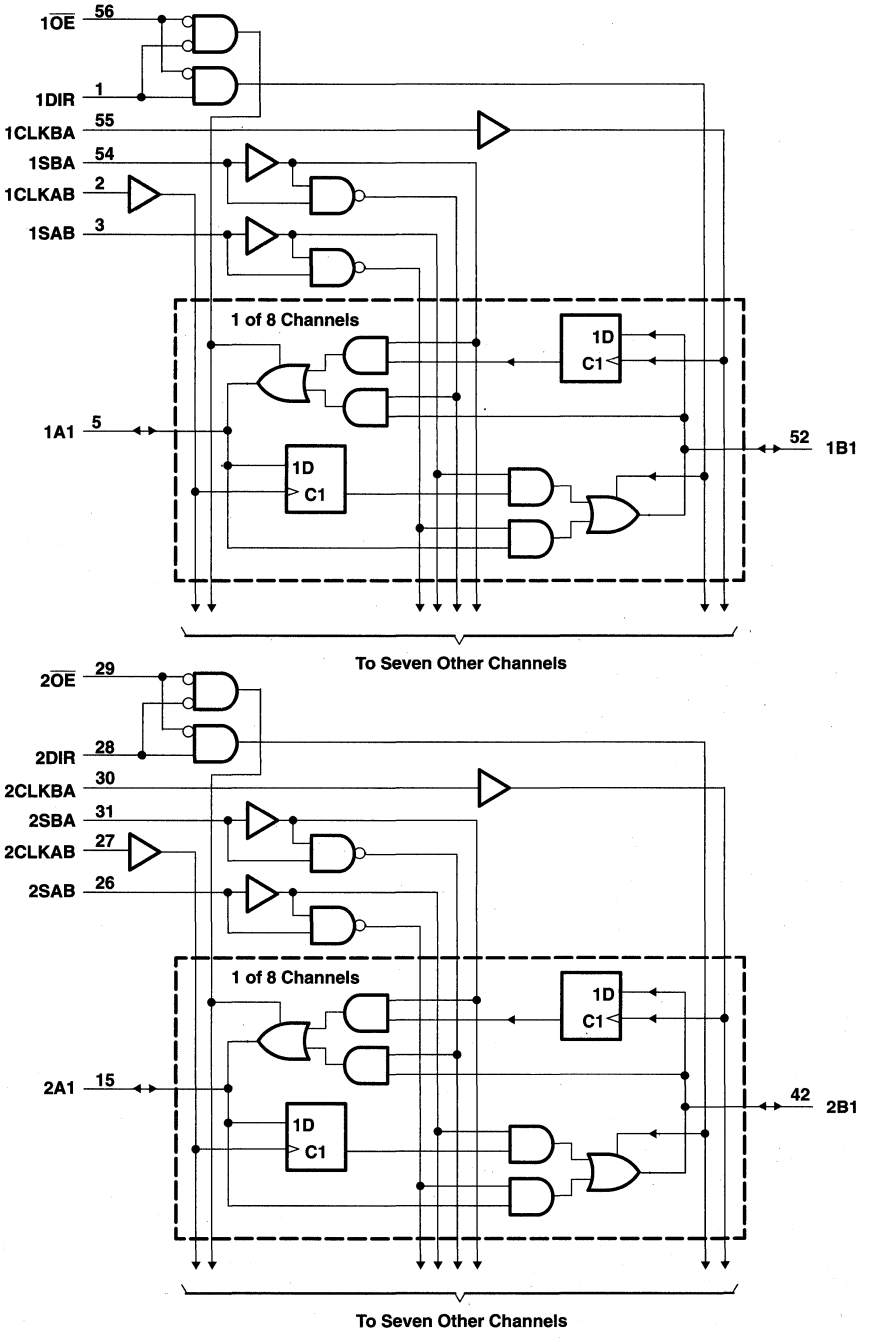
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16646 ..... 96 mA
SN74LVT16646 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16646 ..... 48 mA
SN74LVT16646 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

PRODUCT PREVIEW

recommended operating conditions

			SN54LVT16646		SN74LVT16646		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16646		SN74LVT16646		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2		0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§		20		20	
	V_{CC} = 3.6 V,	V_I = V_{CC}			1		1	
	V_{CC} = 3.6 V,	V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

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- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
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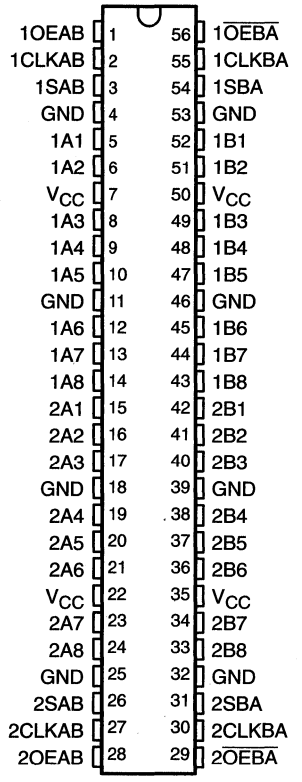
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16652 . . . WD PACKAGE
SN74LVT16652 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16652 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16652 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

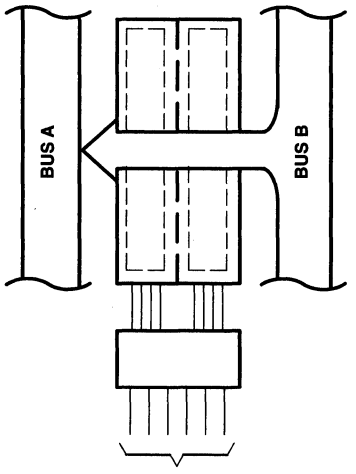
The SN54LVT16652 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16652 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

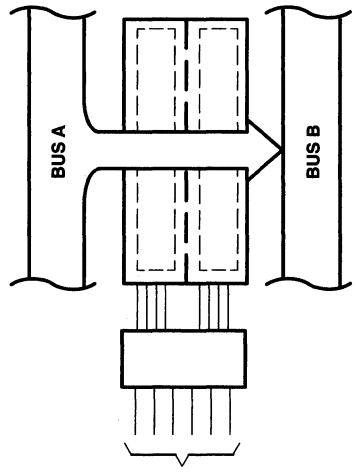
† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

PRODUCT PREVIEW



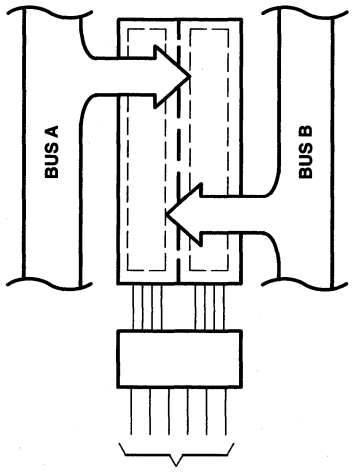
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



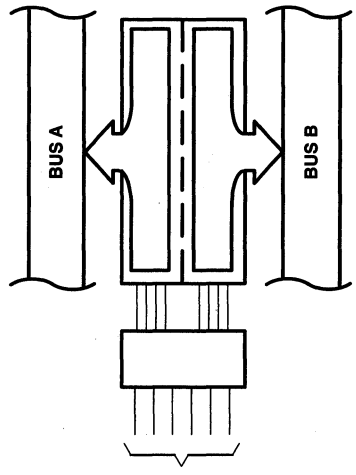
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

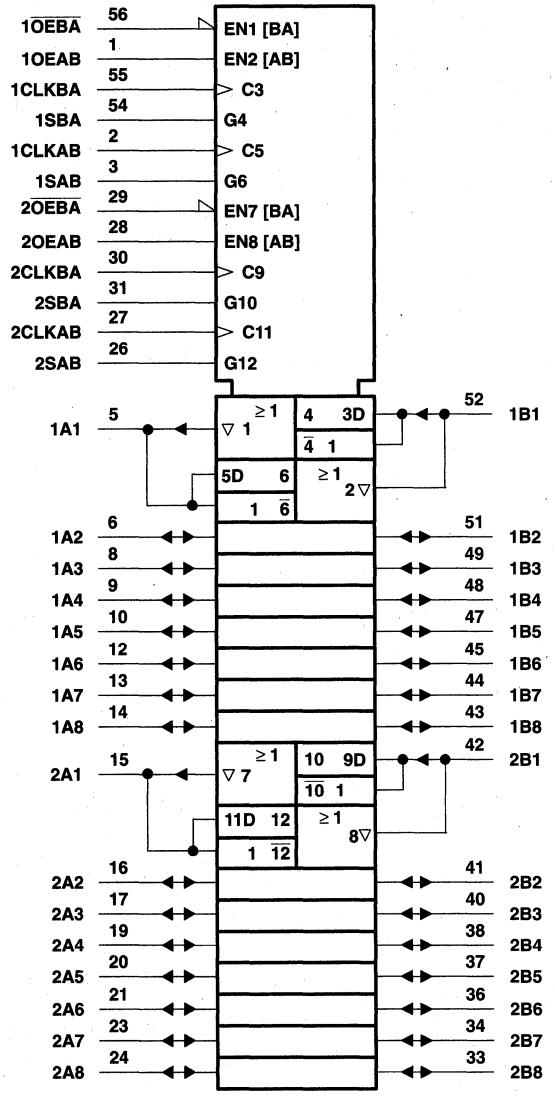
TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

PRODUCT PREVIEW

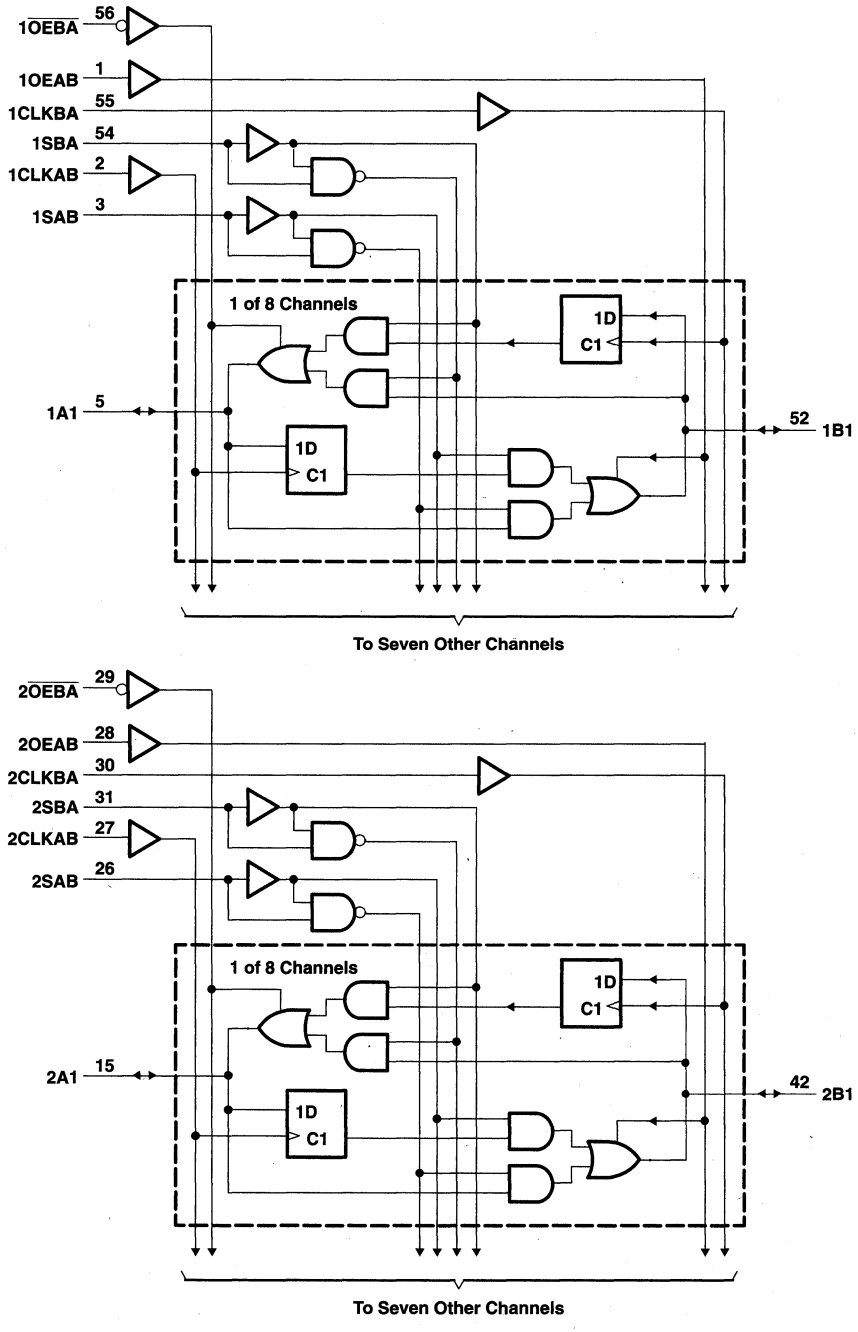
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16652 ..... 96 mA
SN74LVT16652 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16652 ..... 48 mA
SN74LVT16652 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

PRODUCT PREVIEW

recommended operating conditions

			SN54LVT16652		SN74LVT16652		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

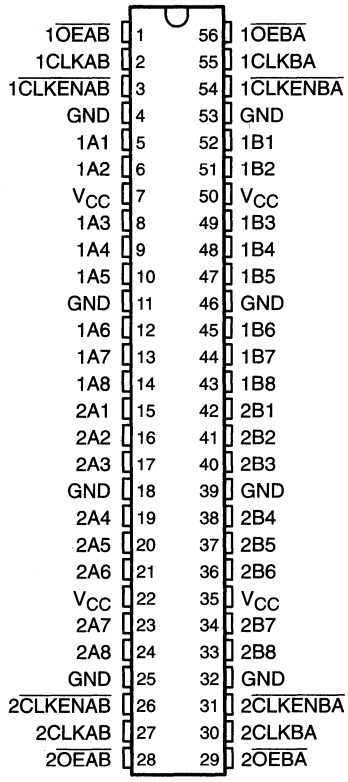
PARAMETER	TEST CONDITIONS			SN54LVT16652		SN74LVT16652		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2		0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§		20		20	
	V_{CC} = 3.6 V,	V_I = V_{CC}			1		1	
	V_{CC} = 3.6 V,	V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16952 . . . WD PACKAGE
SN74LVT16952 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16952 is a 16-bit registered transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

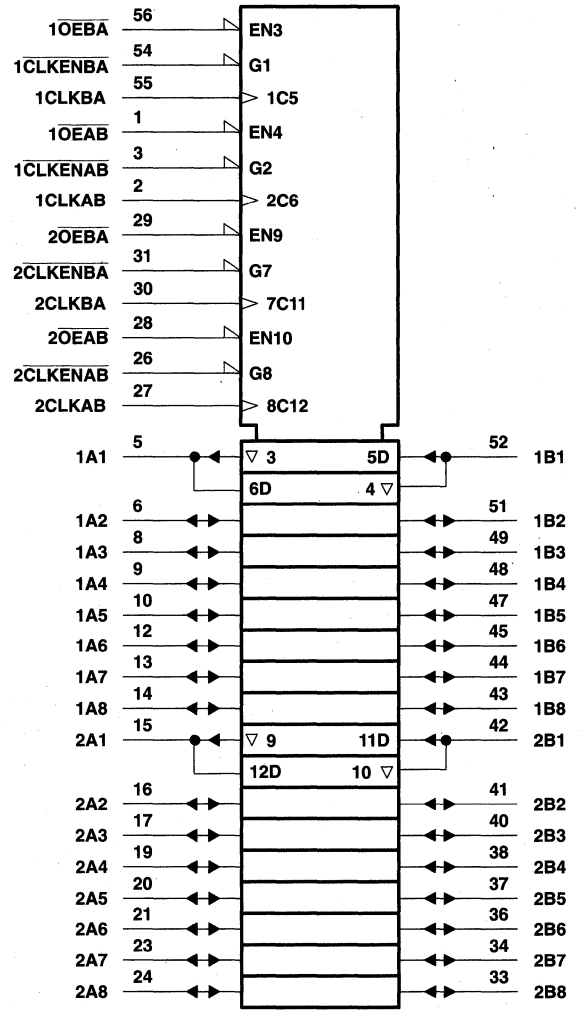
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16952 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16952 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16952 is characterized for operation from −40°C to 85°C.

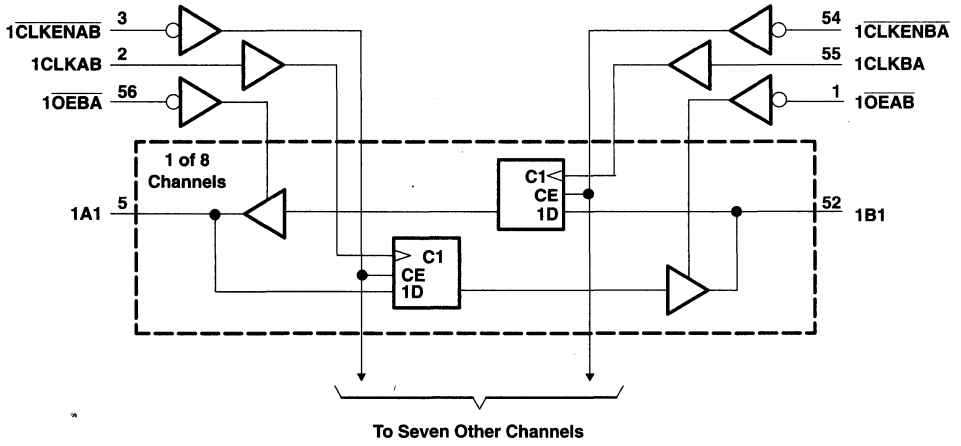
Widebus is a trademark of Texas Instruments Incorporated.

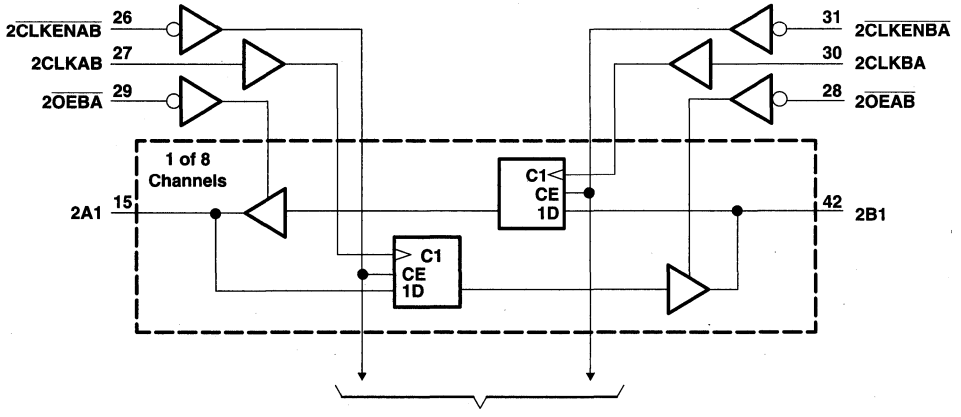
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	B
H	X	L	X	B_0‡
X	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.

‡ Level of B before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16952 ..... 96 mA
SN74LVT16952 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16952 ..... 48 mA
SN74LVT16952 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

PRODUCT PREVIEW

recommended operating conditions

			SN54LVT16952		SN74LVT16952		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16952		SN74LVT16952		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2		0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§		20		20	
	V_{CC} = 3.6 V,	V_I = V_{CC}			1		1	
	V_{CC} = 3.6 V,	V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

LVT MEMORY DRIVERS

Features

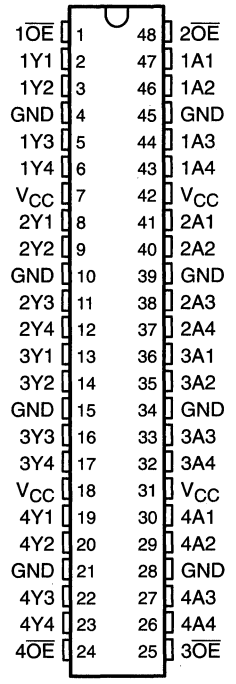
- Output ports have 25-Ω series resistors included on chip
- EPIC-IIB™ BiCMOS process with special low-voltage enhancements
- Mixed-mode circuitry
- Expanded V_{CC} range from 2.7 V to 3.6 V
- Bus-hold circuitry
- Power-on-demand active feedback circuitry
- JEDEC SSOP (Widebus™) and EIAJ TSSOP (Shrink Widebus™) packaging
- Functional equivalents with complete pinout and package compatibility

Benefits

- 3.3-V logic family with equivalent speed and drive performance of 5-V ABT logic family – not just a recharacterized or scaled CMOS
- Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
- AC performance optimized for both regulated supply and unregulated battery operation
- Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Reduces disabled static power consumption (I_{CCZ}) to as little as 0.1 mA for power-conscious portable and battery-powered equipment
- 16- and 18-bit densities for flexible integration
- Space-saving and height-saving surface-mount package options, pin compatible with existing 5-V families for easy conversion
- Drop-in replaceable series resistor options with characteristic LVT advanced system performance and minimal system power
- Reliably drives address lines of 64-K, 256-K, 1-M, 4-M, and 16-M MOS dynamic random access memories (DRAMs)
- Standardization that comes from a common product approach

- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT162240 . . . WD PACKAGE
SN74LVT162240 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162240 is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT162240 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT162240 is characterized for operation from −40°C to 85°C.

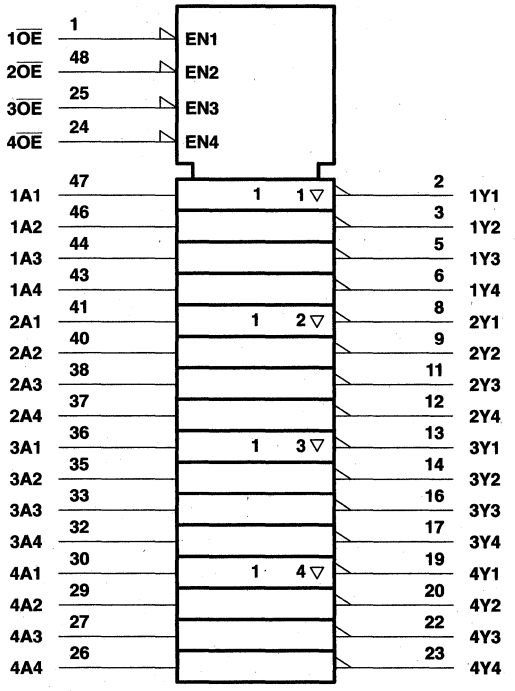
Widebus is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

FUNCTION TABLE
(each 4-bit buffer)

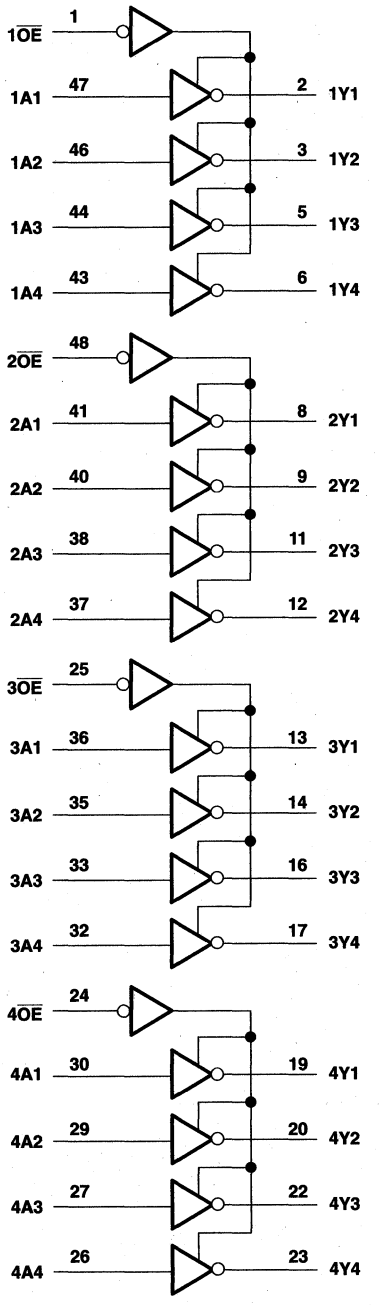
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 30 mA
Current into any output in the high state, I_O (see Note 2) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT162240		SN74LVT162240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

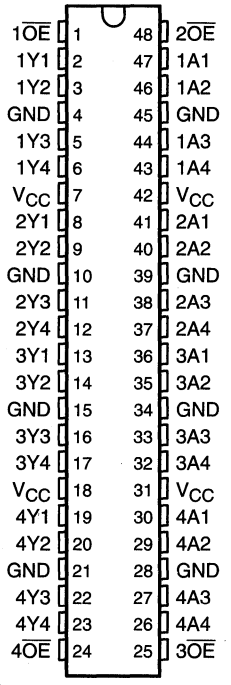
PARAMETER	TEST CONDITIONS			SN54LVT162240		SN74LVT162240		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA			−1.2		−1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = − 12 mA		2		2		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA			0.8		0.8	V
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	μA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins		1		1	
	V_{CC} = 3.6 V,	V_I = 0			−5		−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	μA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75		75		μA
		V_I = 2 V		−75		−75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	μA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			−1		−1	μA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.19		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.19		0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_o	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT162244 . . . WD PACKAGE
SN74LVT162244 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162244 is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT162244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT162244 is characterized for operation from −40°C to 85°C.

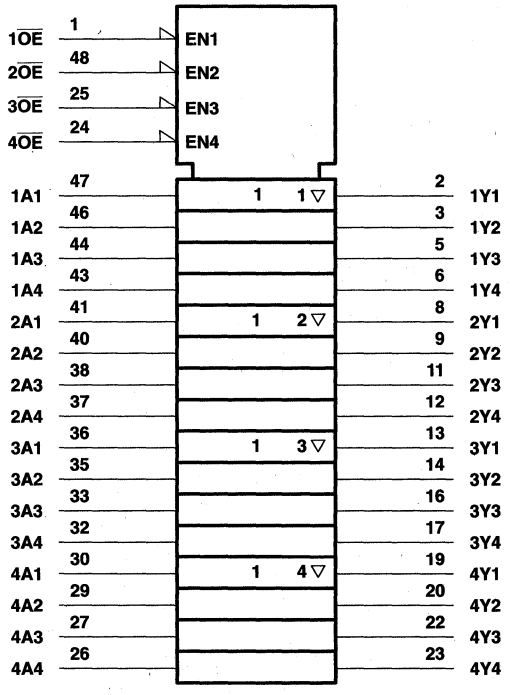
Widebus is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

FUNCTION TABLE
(each buffer)

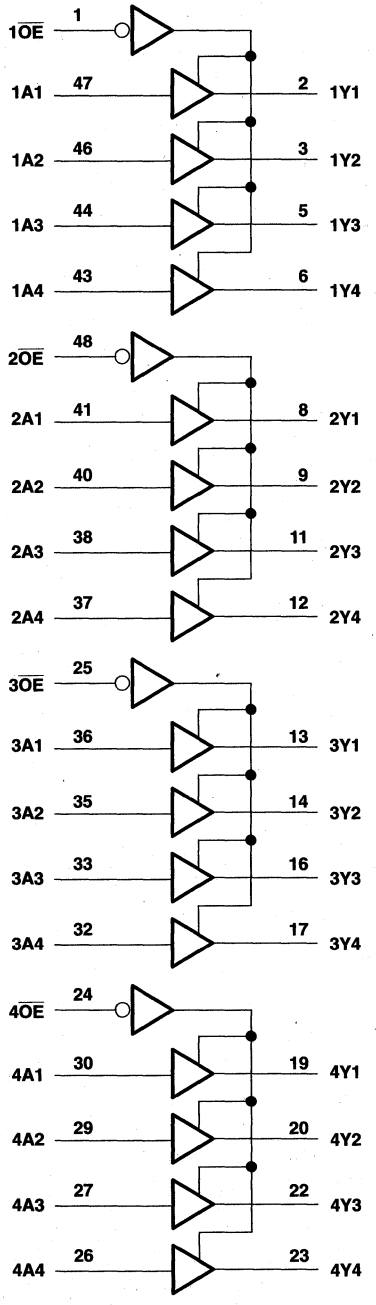
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 30 mA
Current into any output in the high state, I_O (see Note 2) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT162244		SN74LVT162244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

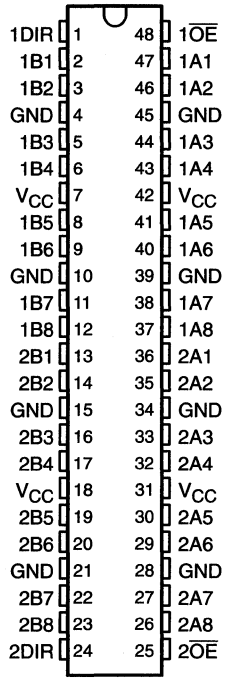
PARAMETER	TEST CONDITIONS			SN54LVT162244		SN74LVT162244		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA			−1.2		−1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = − 12 mA		2		2		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA			0.8		0.8	V
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins		1		1	
	V_{CC} = 3.6 V,	V_I = 0			−5		−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75		75		µA
		V_I = 2 V		−75		−75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			5		5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			−5		−5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.19		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.19		0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_o	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT162245 . . . WD PACKAGE
SN74LVT162245 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT162245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

Widebus is a trademark of Texas Instruments Incorporated.

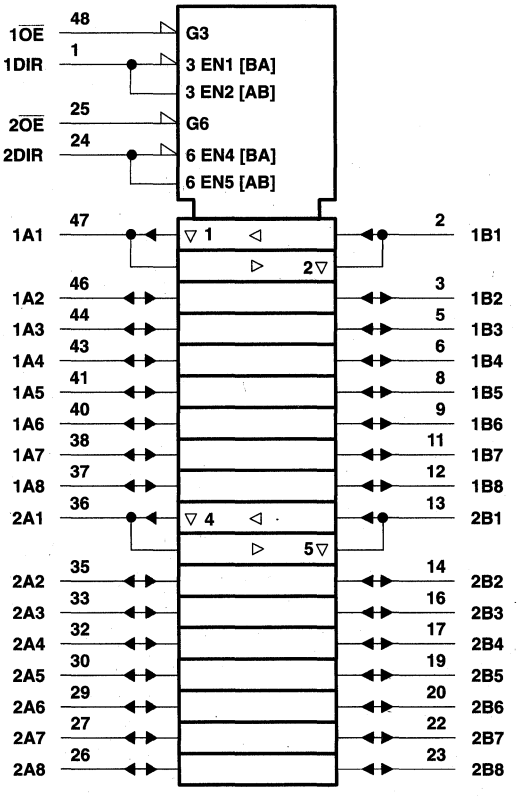
description (continued)

The SN54LVT162245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT162245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

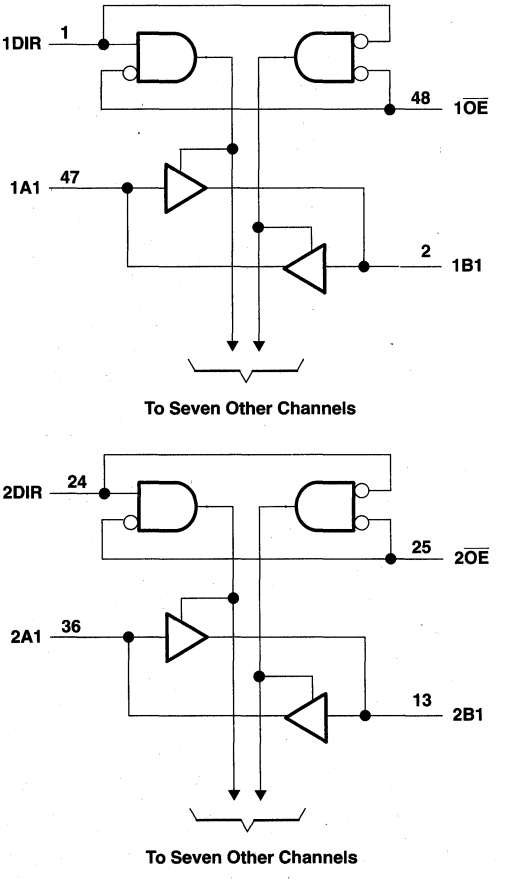
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT162245 (except A port) ..... 96 mA
SN74LVT162245 (except A port) ..... 128 mA
A port ..... 30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT162245 (B port) ..... 48 mA
SN74LVT162245 (B port) ..... 64 mA
A port ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT162245		SN74LVT162245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	B port		−24		−32	mA
		A port		−12		−12	mA
I_{OL}	Low-level output current	B port		24		32	mA
		A port		12		12	
I_{OL}‡	Low-level output current	B port		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

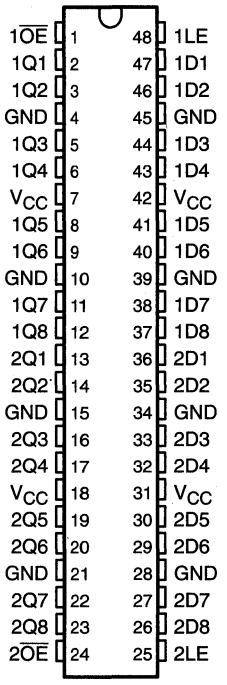
PARAMETER	TEST CONDITIONS			SN54LVT162245		SN74LVT162245		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA			−1.2		−1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = − 12 mA	A port	2		2		V
	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2		V_{CC}−0.2		
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = − 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = −32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 12 mA	A port		0.8		0.8	V
	V_{CC} = 2.7 V,	I_{OL} = 100 µA	B port		0.2		0.2	
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§		20		20	
	V_{CC} = 3.6 V,	V_I = V_{CC}			1		1	
	V_{CC} = 3.6 V,	V_I = 0			−5		−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		−75		−75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			−1		−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT162373 . . . WD PACKAGE
SN74LVT162373 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162373 is a 16-bit transparent D-type latch with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

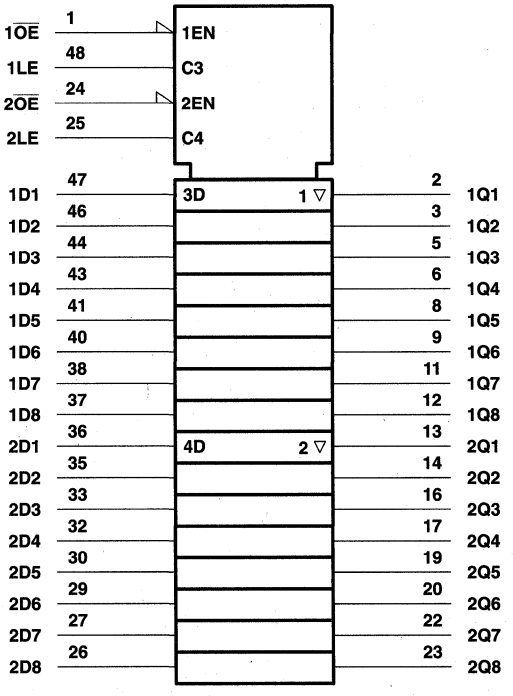
The SN74LVT162373 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT162373 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

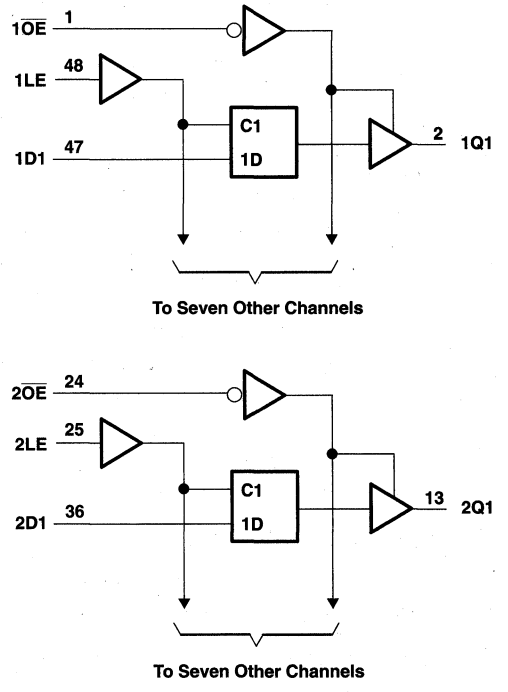
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 30 mA
Current into any output in the high state, I_O (see Note 2) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT162373		SN74LVT162373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

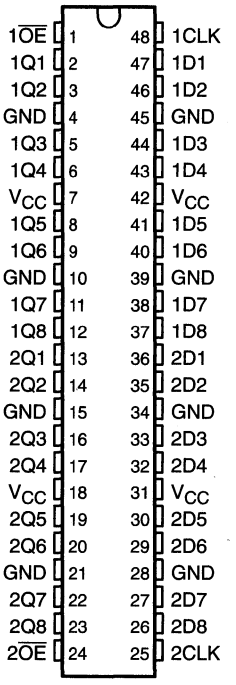
PARAMETER	TEST CONDITIONS			SN54LVT162373		SN74LVT162373		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA			−1.2		−1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = − 12 mA		2		2		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA			0.8		0.8	V
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	μA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins		1		1	
	V_{CC} = 3.6 V,	V_I = 0			−5		−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	μA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75		75		μA
		V_I = 2 V		−75		−75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	μA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			−1		−1	μA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.19		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.19		0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_o	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT162374 . . . WD PACKAGE
SN74LVT162374 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'LVT162374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

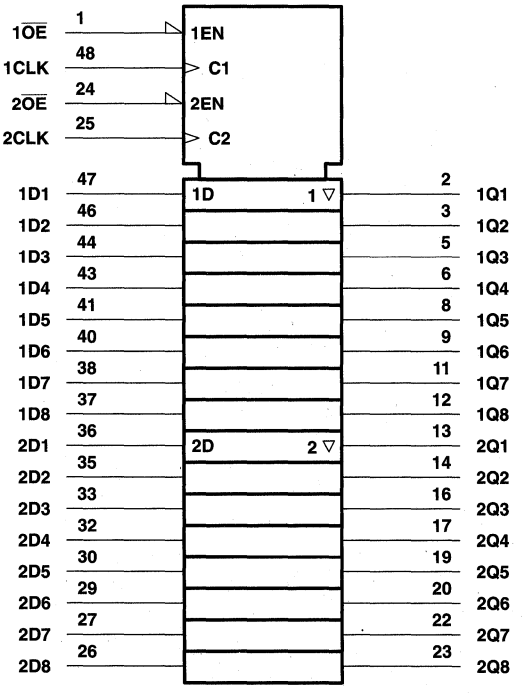
The SN74LVT162374 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT162374 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

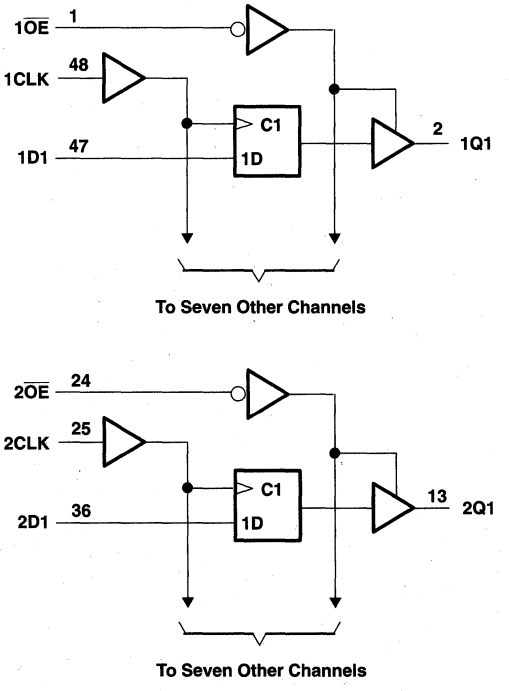
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 30 mA
Current into any output in the high state, I_O (see Note 2) ..... 30 mA
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT162374		SN74LVT162374		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT162374		SN74LVT162374		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA			−1.2		−1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = − 12 mA		2		2		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA			0.8		0.8	V
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	μA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins		1		1	
	V_{CC} = 3.6 V,	V_I = 0			−5		−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	μA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75		75		μA
		V_I = 2 V		−75		−75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	μA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			−1		−1	μA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.19		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.19		0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_o	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

LVT/GTL Widebus™

Features

- High-speed GTL/TTL translating
- Output edge-rate control (OEC™) options
- EPIC-IIB™ BiCMOS process with special low-voltage enhancements
- Mixed-mode signal operation on A port
- Bus-hold circuitry
- Power-on-demand active feedback circuitry
- Widebus™ and UBT™ architectures
- JEDEC SSOP (Widebus™) and EIAJ TSSOP (Shrink Widebus™) packaging

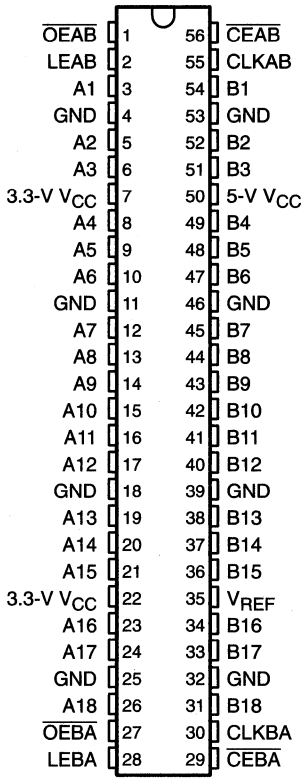
Benefits

- 3.3-V logic family with equivalent speed and drive performance of 5-V ABT logic family – not just a recharacterized or scaled CMOS
- Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
- Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Reduces disabled static power consumption (I_{CCZ}) to as little as 0.1 mA for power-conscious portable and battery-powered equipment
- 16- and 18-bit densities for flexible integration
- Space-saving and height-saving surface-mount package options, pin compatible with existing 5-V families for easy conversion
- Ideal for high-speed bus applications
- Standardization that comes from a common product approach

MARCH 1993

- **Translates Between GTL Signal Levels and LVCMOS, LVTTL, or 5-V TTL Signal Levels**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation on A Port (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **State-of-the-Art BiCMOS Design for Low-Static Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the chip-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16611 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVT16611 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

Widebus and UBT are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

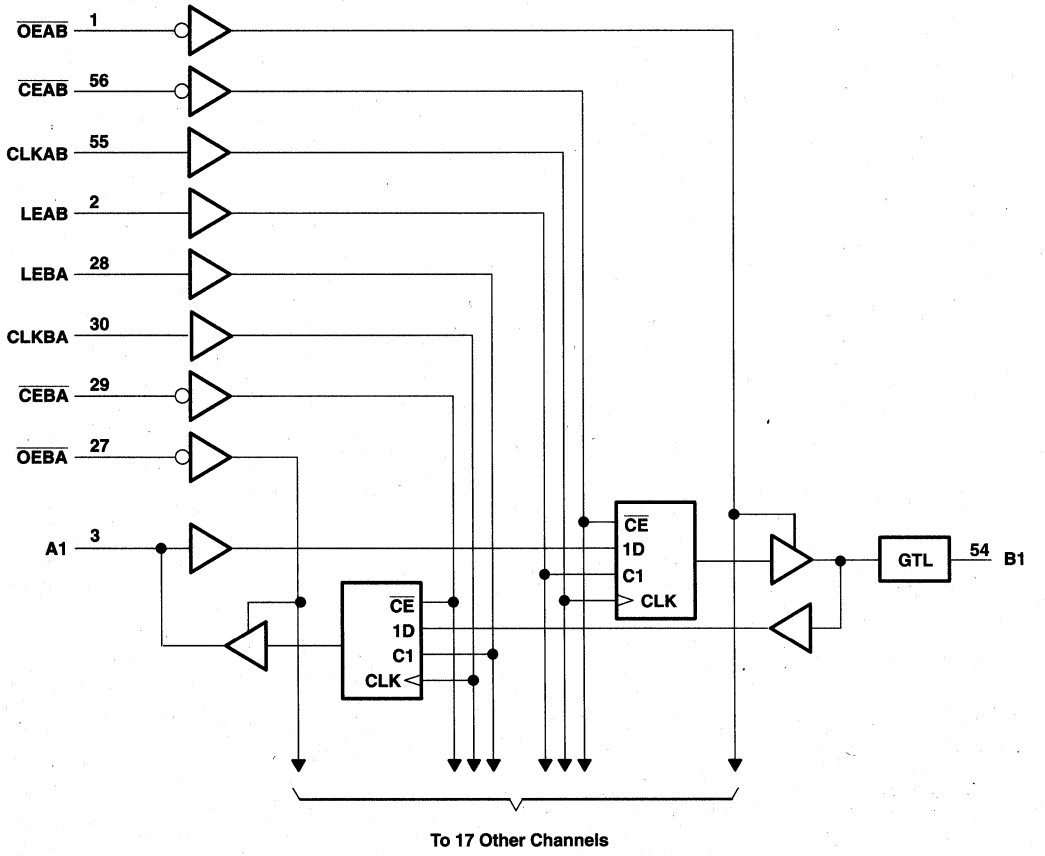
INPUTS					OUTPUT	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0‡	
L	L	L	L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CEBA}$.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, 3.3-V V_{CC} ..... −0.5 V to 4.6 V
Supply voltage range, 5-V V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any A-port output in the low state, I_O ..... 128 mA
Current into any B-port output in the low state, I_O ..... 80 mA
Current into any A-port output in the high state, I_O (see Note 2) ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, 3.3 V		3.15	3.3	3.45	V
	Supply voltage, 5 V		4.75	5	5.25	
V_{REF}	Supply voltage			0.8		V
V_I	Input voltage	B port			V_{CC}	V
		Except B port			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} +50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF} −50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A port			−32	mA
I_{OL}	Low-level output current	A port‡			64	mA
		B port			40	
T_A	Operating free-air temperature		0		70	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = −18 mA			−1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA	V_{CC} − 0.2			V
		V_{CC} = 3.15 V	I_{OH} = − 8 mA	2.4			
			I_{OH} = − 32 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 16 mA			0.4	
			I_{OL} = 32 mA			0.5	
			I_{OL} = 64 mA			0.55	
	B port	V_{CC} = 3.15 V,	I_{OL} = 40 mA			0.4	
I_I	Control pins	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10	µA
	A port§	V_{CC} = 3.45 V	V_I = 5.5 V			20	µA
			V_I = V_{CC}			1	
			V_I = 0			−5	
	B port	V_{CC} = 3.45 V	V_I = V_{CC}			5	
			V_I = 0			−5	
I_{off}	A port	V_{CC} = 0	V_I or V_O = 0 to 4.5 V			100	µA
	B port		V_I or V_O = 0 to 1.2 V			100	
$I_{I(hold)}$	A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			µA
			V_I = 2 V	−75			
I_{OZH}	A port	V_{CC} = 3.45 V	V_O = 3 V			1	µA
	B port		V_O = 1.2 V			10	
I_{OZL}	A port	V_{CC} = 3.45 V	V_O = 0.5 V			−1	µA
	B port		V_O = 0.4 V			−10	
I_{CC}	A port to B port	V_{CC} = 3.45 V, V_I = V_{CC} or GND	I_O = 0,				mA
	B port to A port						
	Outputs disabled						
ΔI_{CC}¶		V_{CC} = 3.45 V, A or control inputs at V_{CC} or GND	One input at 2.7 V,			1	mA
C_i	Control pins	V_I = 3.15 V or 0			4		pF
C_{io}	A port	V_O = 3.15 V or 0			10		pF
C_{io}	B port	Per IEEE1194.0-1991				5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

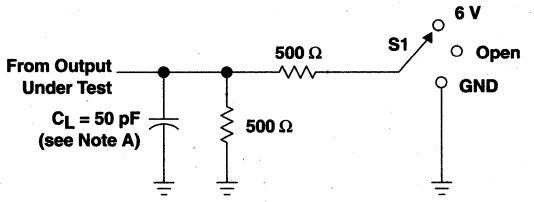
			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	150	MHz
t_w	Pulse duration	LEAB or LEBA high			ns
		CLKAB or CLKBA high or low			
t_{su}	Setup time	A before CLKAB↑	1.5		ns
		B before CLKAB↑	3		
		A before LEAB↓	0.5		
		B before LEBA↓	1.5		
		$\overline{CEAB}$ before CLKAB↑			
		$\overline{CEBA}$ before CLKBA↑			
		$\overline{CEAB}$ before LEAB↓			
		$\overline{CEBA}$ before LEBA↓			
t_h	Hold time	A after CLKAB↑	1		ns
		B after CLKAB↑	0		
		A after LEAB↓	2.5		
		B after LEBA↓	2		
		$\overline{CEAB}$ after CLKAB↑			
		$\overline{CEBA}$ after CLKBA↑			
		$\overline{CEAB}$ after LEAB↓			
		$\overline{CEBA}$ after LEBA↓			

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (see Figure 1)

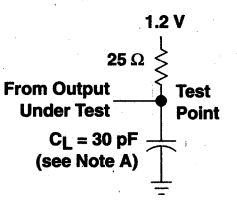
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}						MHz
t_{PLH}	A	B			3.2	ns
t_{PHL}					3.2	
t_{PLH}	LEAB	B			4	ns
t_{PHL}					4	
t_{PLH}	CLKAB	B			4.3	ns
t_{PHL}					4.3	
t_{PLH}	$\overline{OEAB}$	B			4.5	ns
t_{PHL}					4.5	
t_f	Transition time, B outputs (0.5 V to 1 V)			1.7		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.6		ns
t_{PLH}	B	A			6.5	ns
t_{PHL}					6.5	
t_{PLH}	LEBA	A			6.3	ns
t_{PHL}					6.3	
t_{PLH}	CLKBA	A			6.3	ns
t_{PHL}					6.3	
t_{EN}	$\overline{OEBA}$	A			5.5	ns
t_{DIS}					6	

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

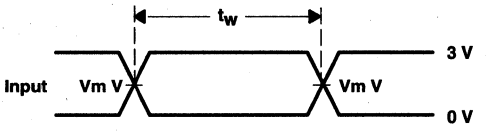


LOAD CIRCUIT FOR A OUTPUTS

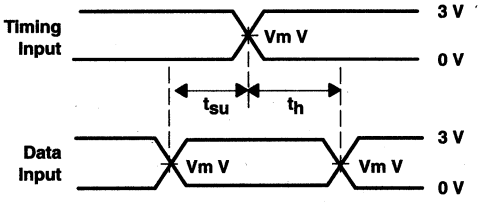


LOAD CIRCUIT FOR B OUTPUTS

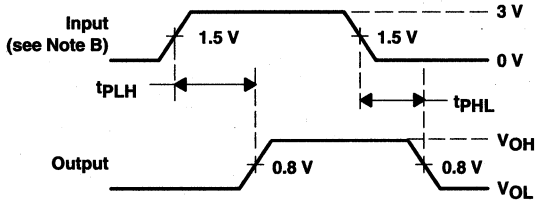
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



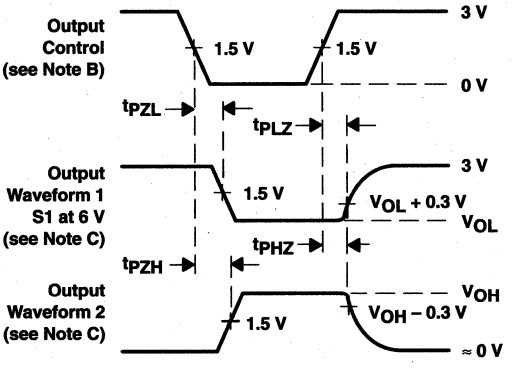
VOLTAGE WAVEFORMS
PULSE DURATION
(Vm = 1.5 V for A port and 0.8 V for B port)



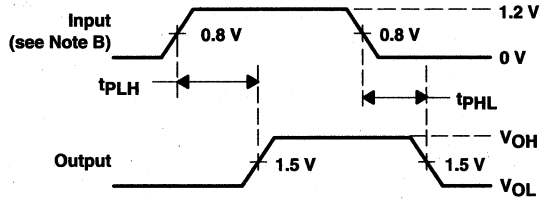
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(Vm = 1.5 V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

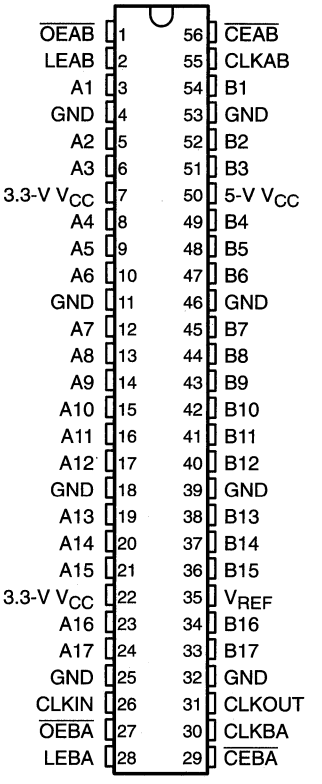
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Translates Between GTL Signal Levels and LVCMOS, LVTTL, or 5-V TTL Signal Levels**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation on A Port (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **State-of-the-Art BiCMOS Design for Low-Static Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages**

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

This 17-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. It provides for a copy of CLKAB at GTL logic levels (CLKOUT). It also provides a conversion of the GTL clock to a TTL environment (CLKIN).

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the chip-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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description (continued)

The SN74LVT16615 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVT16615 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE†

INPUTS					OUTPUT	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H or L	X	B_0‡	
L	L	L	H or L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

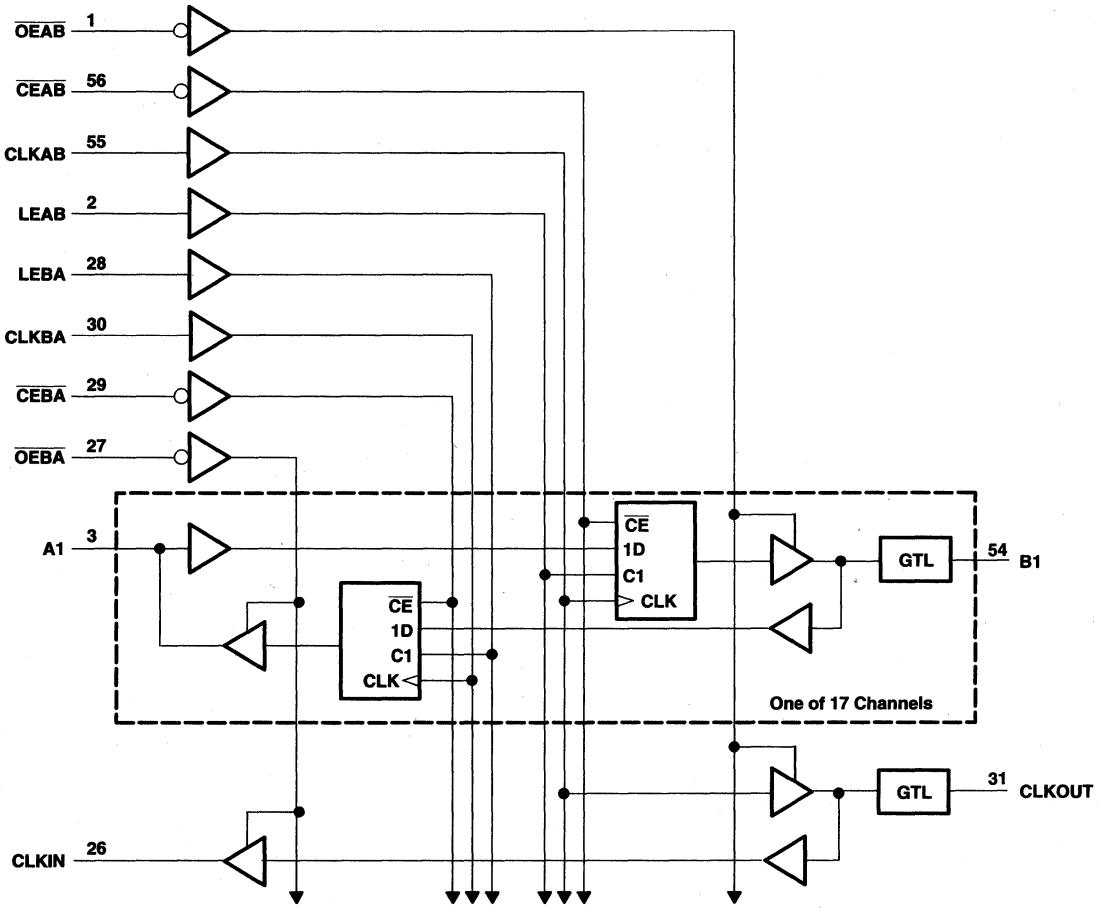
† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CEBA}$.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, 3.3 V, V_{CC} ..... −0.5 V to 4.6 V
Supply voltage range, 5 V, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any A-port output in the low state, I_O ..... 128 mA
Current into any B-port output in the low state, I_O ..... 80 mA
Current into any A-port output in the high state, I_O (see Note 2) ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

PRODUCT PREVIEW

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, 3.3 V		3.15	3.3	3.45	V
	Supply voltage, 5 V		4.75	5	5.25	
V_{REF}	Supply voltage			0.8		V
V_I	Input voltage	B port			V_{CC}	V
		Except B port			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} +50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF} −50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A port			−32	mA
I_{OL}	Low-level output current	A port‡			64	mA
		B port			40	
T_A	Operating free-air temperature		0		70	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = −18 mA			−1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA	V_{CC} − 0.2			V
		V_{CC} = 3.15 V	I_{OH} = − 8 mA	2.4			
			I_{OH} = − 32 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 16 mA			0.4	
			I_{OL} = 32 mA			0.5	
			I_{OL} = 64 mA			0.55	
	B port	V_{CC} = 3.15 V,	I_{OL} = 40 mA			0.4	
I_I	Control pins	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10	µA
	A port§	V_{CC} = 3.45 V	V_I = 5.5 V			20	µA
			V_I = V_{CC}			1	
			V_I = 0			−5	
	B port	V_{CC} = 3.45 V	V_I = V_{CC}			5	
			V_I = 0			−5	
I_{off}	A port	V_{CC} = 0	V_I or V_O = 0 to 4.5 V			100	µA
	B port		V_I or V_O = 0 to 1.2 V			100	
$I_{I(hold)}$	A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			µA
			V_I = 2 V	−75			
I_{OZH}	A port	V_{CC} = 3.45 V	V_O = 3 V			1	µA
	B port		V_O = 1.2 V			10	
I_{OZL}	A port	V_{CC} = 3.45 V	V_O = 0.5 V			−1	µA
	B port		V_O = 0.4 V			−10	
I_{CC}	A port to B port	V_{CC} = 3.45 V, V_I = V_{CC} or GND	I_O = 0,				mA
	B port to A port						
	Outputs disabled						
ΔI_{CC}¶		V_{CC} = 3.45 V, A or control inputs at V_{CC} or GND	One input at 2.7 V,			1	mA
C_i	Control pins	V_I = 3.15 V or 0			4		pF
C_{io}	A port	V_O = 3.15 V or 0			10		pF
C_{io}	B port	Per IEEE1194.0-1991				5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	150	MHz
t_w	Pulse duration	LEAB or LEBA high			ns
		CLKAB or CLKBA high or low			
t_{su}	Setup time	A before CLKAB↑	1.5		ns
		B before CLKAB↑	3		
		A before LEAB↓	0.5		
		B before LEBA↓	1.5		
		$\overline{CEAB}$ before CLKAB↑			
		$\overline{CEBA}$ before CLKBA↑			
		$\overline{CEAB}$ before LEAB↓			
		$\overline{CEBA}$ before LEBA↓			
t_h	Hold time	A after CLKAB↑	1		ns
		B after CLKAB↑	0		
		A after LEAB↓	2.5		
		B after LEBA↓	2		
		$\overline{CEAB}$ after CLKAB↑			
		$\overline{CEBA}$ after CLKBA↑			
		$\overline{CEAB}$ after LEAB↓			
		$\overline{CEBA}$ after LEBA↓			

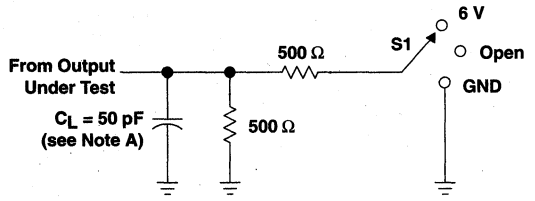
PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (see Figure 1)

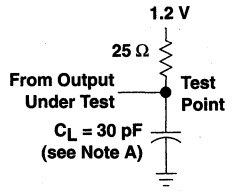
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}						MHz
t_{PLH}	A	B			3.2	ns
t_{PHL}					3.2	
t_{PLH}	LEAB	B			4	ns
t_{PHL}					4	
t_{PLH}	CLKAB	B			4.3	ns
t_{PHL}					4.3	
t_{PLH}	CLKAB	CLKOUT	2.3		6.5	ns
t_{PHL}			2.3		6.5	
t_{PLH}	$\overline{OEAB}$	B			4.5	ns
t_{PHL}					4.5	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.7		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.6		ns
t_{PLH}	B	A			6.5	ns
t_{PHL}					6.5	
t_{PLH}	LEBA	A			6.3	ns
t_{PHL}					6.3	
t_{PLH}	CLKBA	A			6.3	ns
t_{PHL}					6.3	
t_{PLH}	CLKOUT	CLKIN	4		13.5	ns
t_{PHL}			4		13.5	
t_{en}	$\overline{OEBA}$	A			5.5	ns
t_{dis}					6	

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

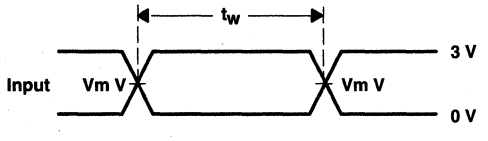


LOAD CIRCUIT FOR A OUTPUTS

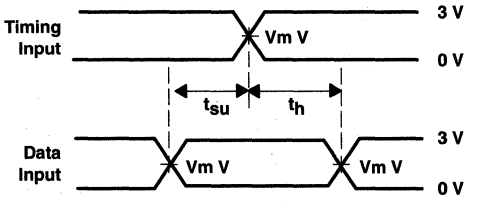


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

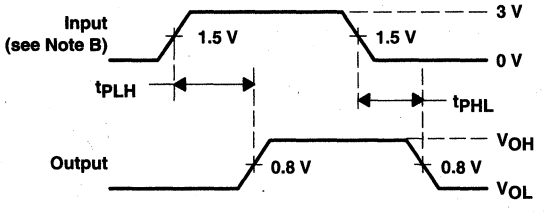
LOAD CIRCUIT FOR B OUTPUTS



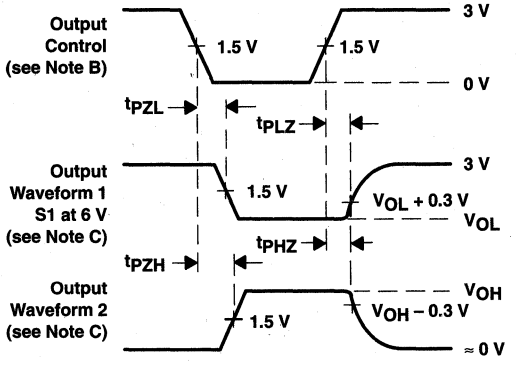
VOLTAGE WAVEFORMS
PULSE DURATION
(Vm = 1.5 V for A port and 0.8 V for B port)



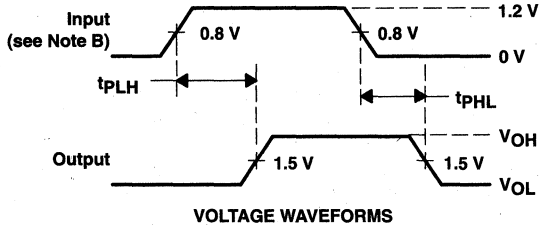
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(Vm = 1.5 V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

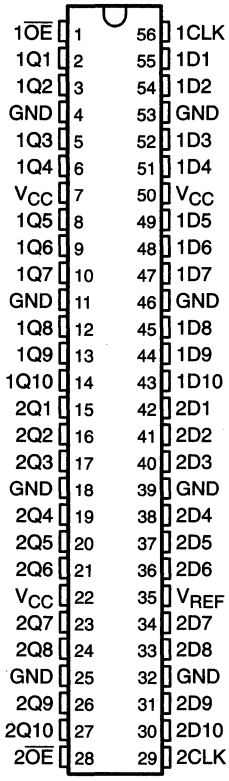
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- ***EPIC*-IIB™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Provides GTL Signals Levels on Both Inputs and Outputs**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74GTL16821 has 20 single-bit flip-flops which are designed to provide terminated GTL logic levels.

The device can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. The SN74GTL16821 provides true data at the Q outputs on the positive transition of the clock (CLK) input.

The output-enable ($\overline{OE}$) input can be used to place the outputs in a high state.The output-enable input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74GTL16821 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74GTL16821 is characterized for operation from 0°C to 70°C.

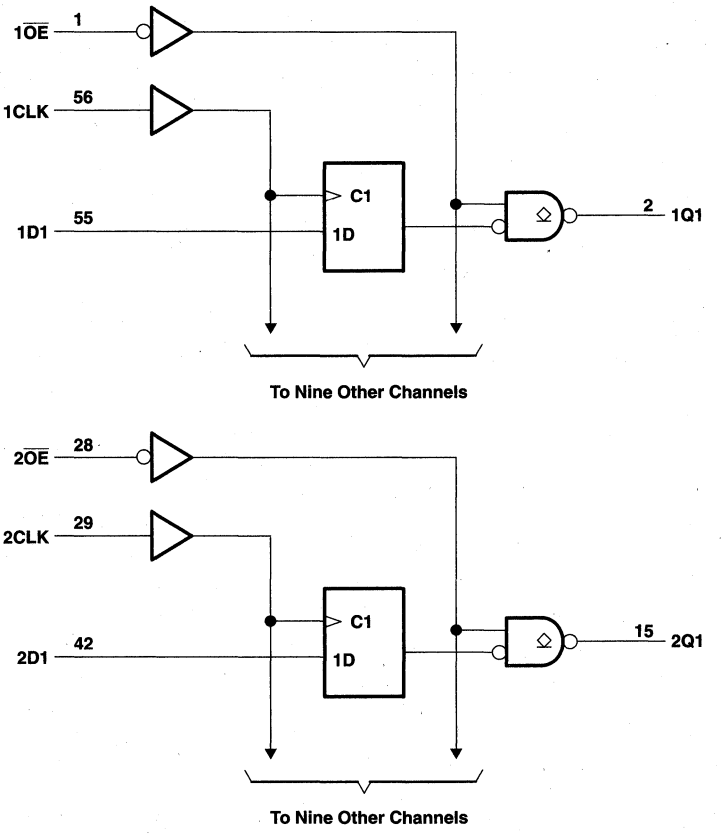
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

EPIC-IIB and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 4.6 V
Current into any output in the low state, I_O	80 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > 0$)	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		3.6	V
V_{REF}	Supply voltage	2/3 V_{CC} − 2%	0.8	2/3 V_{CC} + 2%	V
V_I	Input voltage	0		V_{CC}	V
V_{OH}	High-level output voltage			3.6	V
V_{IH}	High-level input voltage	V_{REF} +50 mV			V
V_{IL}	Low-level input voltage			V_{REF} − 50 mV	V
I_{IK}	Input clamp current			−18	mA
I_{OL}	Low-level output current			40	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA			−1.2	V
V_{OL}		V_{CC} = 3 V,	I_{OL} = 40 mA			0.4	V
I_I		V_{CC} = 3 V	V_I = V_{CC}			5	µA
			V_I = 0			−5	
I_{OH}		V_{CC} = 3 V,	V_{OH} = 3.6 V				µA
I_{CC}	Outputs high	V_{CC} = 3 V, V_I = V_{CC} or GND	I_O = 0,				mA
	Outputs low						
C_i		Per IEEE1194.0-1991			4		pF
C_o		Per IEEE1194.0-1991			6		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PRODUCT PREVIEW

Contents

The Bypass Capacitor in High-Speed Environments

Advanced BiCMOS Technology

Ramzi Ammar
Advanced System Logic – Semiconductor Group
Texas Instruments Incorporated

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Contents

List of Illustrations

Introduction

High-speed switching environments generate noise on power lines (or planes) due to the charging and discharging of internal and external capacitors of an integrated circuit. The instantaneous current generated with the rising and falling edges of the outputs causes the power line (or plane) to ring. This behavior can violate the V_{CC} recommended operating conditions or generate false signals, creating serious problems. A simple and easy solution must be considered to prevent such a problem from occurring. This solution is the bypass capacitor.

Bypass Definition

A bypass capacitor stores an electrical charge that is released to the power line whenever a transient voltage spike occurs. It provides a low impedance supply, thereby minimizing the noise generated by the switching outputs of the device.

Bypassing Considerations

A system without bypassing techniques can create severe power disturbance and cause circuit failures. Figure 1 shows the V_{CC} line of the 'ABT541 ringing while all outputs are switching. Note that there is no bypass capacitor at the V_{CC} pin. There are a few issues that should be considered when bypassing power lines (or planes).

- The capacitor type
- The capacitor placement
- The output load effect
- The capacitor size

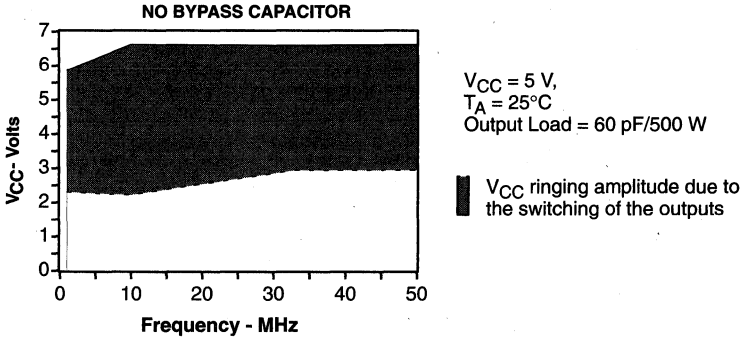


Figure 1. V_{CC} Line Disturbance vs Frequency

Capacitor Type

In a high-speed environment the lead inductances of a bypass capacitor become very critical. High-speed switching of a part's outputs generates high frequency noise (> 100 MHz) on the power line (or plane). These harmonics cause the capacitor with high lead inductance to act as an open circuit, preventing it from supplying the power line (or plane) with the current needed to maintain a stable level, and resulting in functional failure of the circuit. Therefore, bypassing a power line (or plane) from the device internal noise requires capacitors with very small inductances. That is why the multilayer ceramic chip capacitors (MLC) are more favorable than others for bypassing power lines (or planes). They exhibit negligible internal inductance, thereby allowing the charge to flow easily, when needed, without degradation.

Capacitor Placement

Most of the printed circuit boards are designed to maintain a short distance between power and ground. This is done by laminating the power line (or plane) with the ground plane and can be electrically approximated with lumped capacitances as shown in Figure 2. However, this is not enough to have a reliable system, and another technique must be considered to provide a low-impedance path for the transient current to be grounded. This can be done by placing the bypass capacitor close to the power pin of the device.

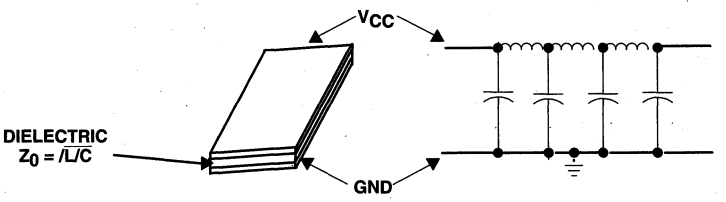


Figure 2. Typical Power Layout

Why This Location Is Very Important

Consider a device driving a line from low to high having an impedance ($Z \cong 100\ \Omega$) and a supply voltage ($V_{CC} = 5$ V) (see Figure 3). In order for the device to change state, an output current ($I = 50$ mA) is needed instantaneously. Note that for eight outputs switching $I = 50 \times 8 = 400$ mA. This current is provided by the power line (or plane) in a period ≤ the rise time of the output (approximately 3 ns for ABT). The bypass capacitor must supply the charge in that same period of time to avoid V_{CC} drop, therefore distance becomes an important issue. Line inductances can block the charge from flowing, leaving the power line (or plane) disturbed.

Using the formula for paralleled wires:

$$L = l\,\frac{\mu_0}{\pi}\,\mathrm{Ln}\,\frac{d}{r} \qquad (1)$$

where d is the distance between the wires, r is the radius of the wires, l is the length of the wires and μ_0 is the permeability of medium between wires, one can note that the inductance (L) is directly proportional to the distance between the lines as well as the length of the lines. Therefore, by reducing the loop ABCD in Figure 3, we can minimize the inductance and allow the capacitor to do its function more efficiently, and hence keep the noise off the power line (or plane).

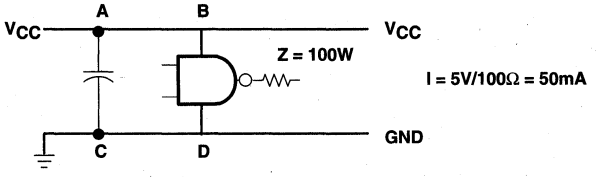
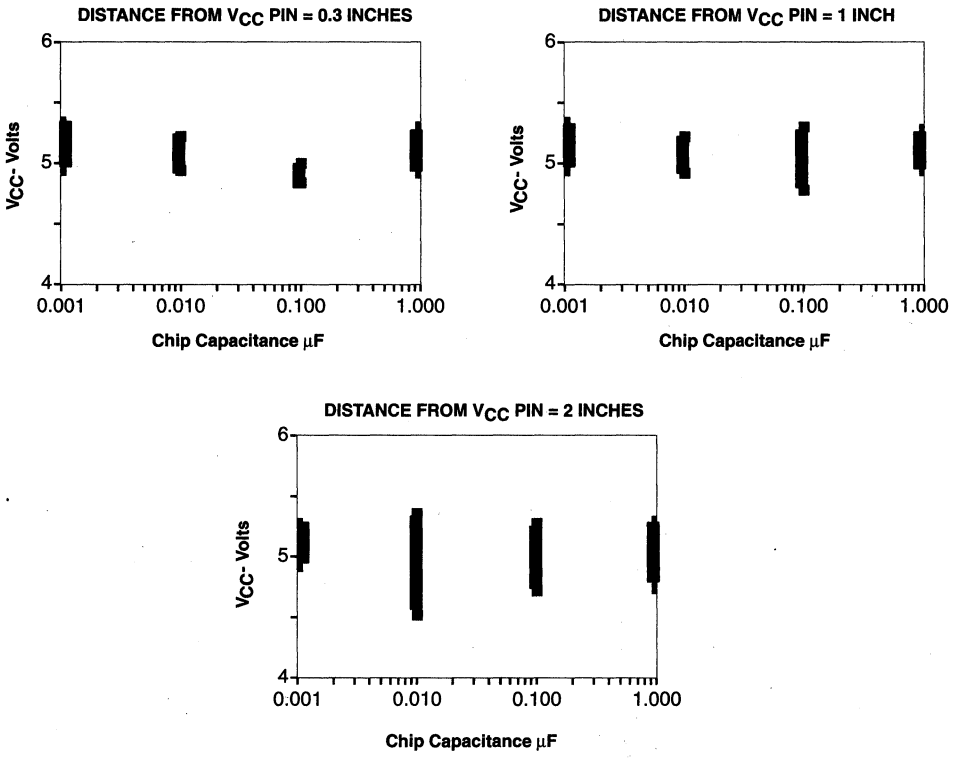


Figure 3. Capacitive Storage (Bypass Capacitor)

Several tests were done on an 'ABT541 device to study the behavior of its power line (or plane) as the outputs switch simultaneously. This data is taken at different distances from the power pin (0.3, 1, and 2 inches) using four chip capacitors (0.001, 0.01, 0.1, and 1 μF), with an input frequency of 33 MHz and all eight outputs switching (worst case). Figure 4 shows the line disturbance increases as the capacitor is moved away from the power pin.



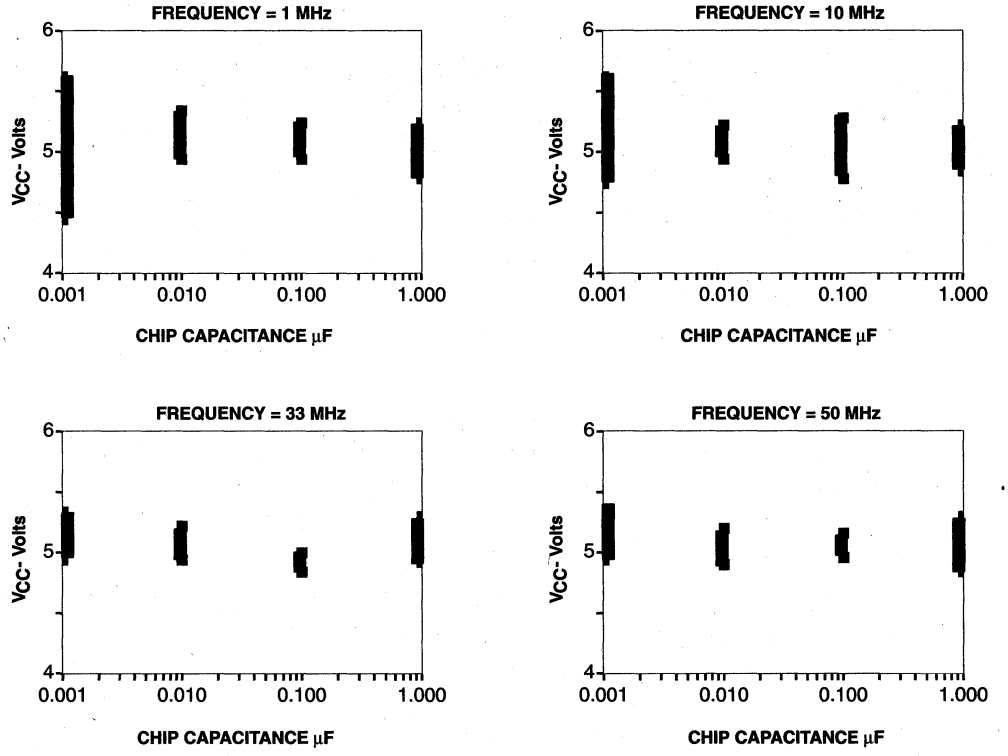
V_{CC} = 5 V, T_A = 25°C, Frequency = 33 MHz, Output Load = 500 Ω

V_{CC} ringing amplitude due to the switching of the device outputs

Figure 4. V_{CC} Line Disturbance vs Cap Size at Different Distances

Output Load Effect

Capacitive loads combined with increased frequency result in higher transient current and possible V_{CC} oscillation. If the output load is purely resistive, the increase in frequency does not affect the rising and falling edge of the outputs, therefore not increasing the V_{CC} line disturbance. Figure 5 shows the power line behavior across frequency while driving a resistive load only, and Figure 6 shows the same plot with an additional 60-pF capacitive load.



Distance From V_{CC} Pin = 0.3 Inch, V_{CC} = 5 V, T_A = 25°C, Output Load = 500Ω

V_{CC} ringing amplitude due to the switching of the device outputs

Figure 5. V_{CC} Line Disturbance vs Cap Size With Resistive Load at Different Frequencies

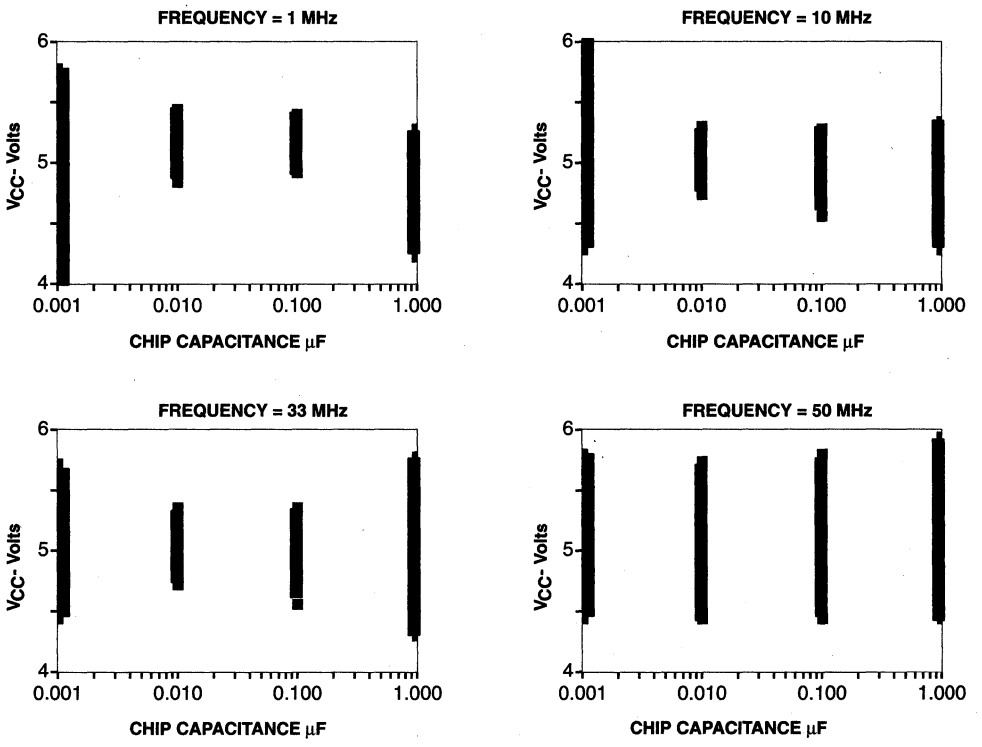
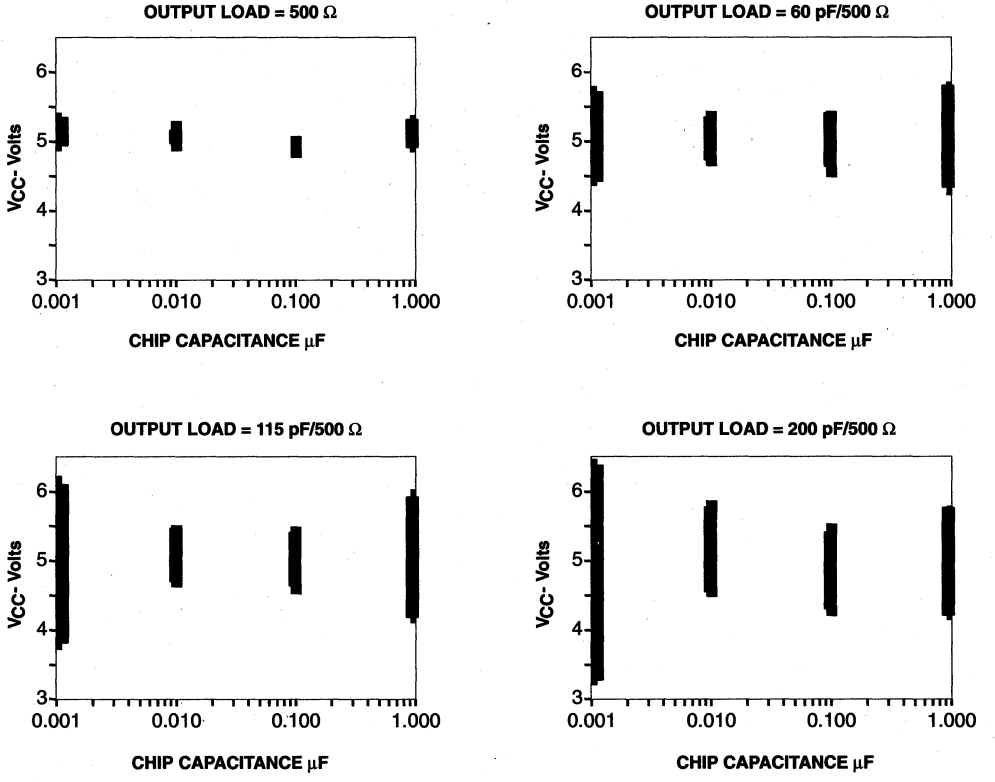


Figure 6. V_{CC} Line Disturbance vs Cap Size With 60-pF Load at Different Frequencies

When driving large capacitive loads, more charge will need to be supplied to the output load, resulting in a slower rising or falling edge. However, if the bypass capacitor is not capable of providing the needed charge, power lines (or planes) start to ring and eventually oscillate causing failures across the board. These oscillations can be of a great amplitude, 2 to 3 V p-to-p. Figure 7 shows these oscillations at four different loads (0, 60, 115 and 200 pF) using four different bypass capacitors (0.001, 0.01, 0.1, and 1 μF).



Distance From V_{CC} Pin = 0.3 Inch, V_{CC} = 5 V, T_A = 25°C, Frequency = 33 MHz

V_{CC} ringing amplitude due to the switching of the device outputs

Figure 7. V_{CC} Line Disturbance vs Cap Size at Different Capacitive Loads

Capacitor Size

How can we choose the right bypass capacitor? The most important parameter is the capability of supplying instantaneous current when it is needed.

There are two ways for calculating the bypass capacitor size for a device:

1. One must know the amount of current needed to switch one output from low to high (I), the number of outputs switching (N), the time required for the capacitor to charge the line (ΔT), and the drop in V_{CC} that can be tolerated (ΔV).

The following equation can be used:

$$C = \frac{I \times N \times \Delta T}{\Delta V} \quad (2)$$

where ΔT and ΔV can be assumed.

For example, say one has the following parameters: $\Delta V = 0.1$ V, $\Delta T = 3$ ns, N = 8, and I can be obtained from either Figure 3, for rough estimate or from the plot in Figure 8, assuming 50-MHz frequency. We are going to use the latter parameter for our example, I = 44 mA.

Then the equation is as follows:

$$C = \frac{44 \times 10^{-3} \times 8 \times 3 \times 10^{-9}}{0.1} = 10080 \times 10^{-12} = 0.01\ \mu F \quad (3)$$

2. Several of the capacitor manufacturers specify the maximum pulse slew rate. This allows the capacitor's maximum current to be calculated. For example, a 0.1-μF capacitor rated at 50 V/μs can supply: $i = C dv/dt = 0.1 \times 50 = 5$ A. This current is greater than the maximum current ($I \times N = 44$ mA $\times$ 8 outputs switching = 352 mA) required by the device used in the previous example.

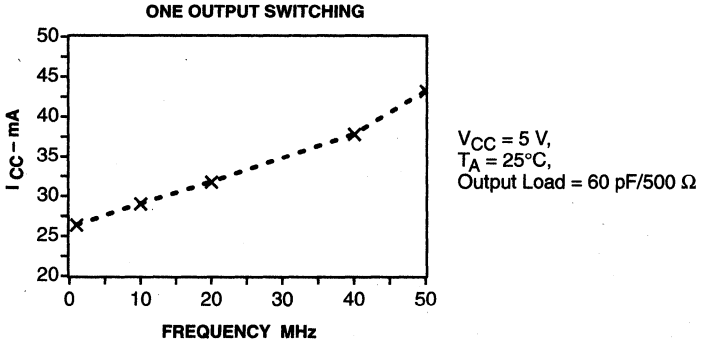


Figure 8. I_{CC} vs Frequency

Conclusion

From what was mentioned previously, one can see how important is the bypassing technique. Bypass capacitors play a major role in achieving reliable systems. The absence of the bypass capacitor can generate false signals and create major problems across the entire board. Figure 1 shows the undesired ringing caused by simultaneously switching the outputs of the 'ABT541. Also, choosing a capacitor with negligible lead inductance can avoid unpredictable behavior at high frequencies. Locating the capacitor closer to the V_{CC} pin of a device can avoid further complications and eliminate the ringing entirely. Figure 6 shows the V_{CC} line behavior with the bypass capacitor placed 0.3 inches away from the V_{CC} pin, whereas Figure 9 shows the same plot with the same load, but the bypass capacitor is located at the pin, one can see the dramatic improvement achieved in the latter case. This technique can also be applied to Texas Instruments *Widebus*™ family by bypassing all V_{CC} pins. This was proven to be the most effective method for eliminating the V_{CC} line ringing. It is always important to minimize the loop between the V_{CC} pin, the ground, and the bypass capacitor. Finally, choosing the capacitor size by using either method mentioned earlier is highly recommended. If one considers all these issues, a good bypass technique can be achieved.

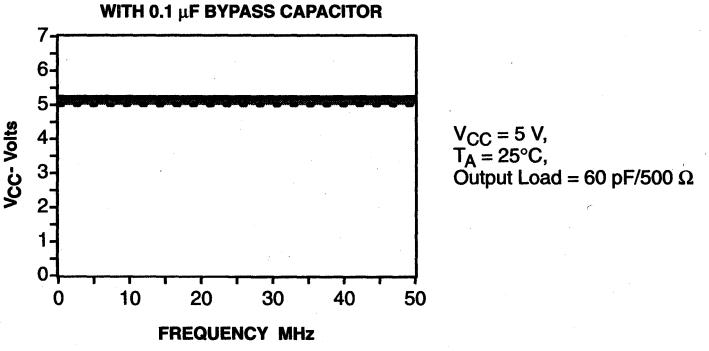


Figure 9. V_{CC} Line Disturbance vs Frequency

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[1] Texas Instruments, *Advanced Schottky Family (ALS/AS) Applications*

[2] Walton, D., *P.C.B. Layout for High-Speed Schottky TTL*

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Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices

Advanced BiCMOS Technology

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Advanced System Logic – Semiconductor Group
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Contents

List of Illustrations

Introduction

The data in this application note demonstrates the skew between the outputs of a sample of Texas Instruments Advanced BiCMOS (ABT) devices. This paper will explain which output skew is being examined, where the data for these curves comes from, and how the data is analyzed. Also, some of the errors that may be present in the data will be discussed.

Skews

Skew is a term that is used to define the difference, in time, between two different signal edges. There are several different types of skew currently being used, they are defined in JEDEC 99 clause 2.3.5:

> Output Skew ($t_{sk(o)}$) – The difference between two concurrent propagation delay times that originate at either a single input or two inputs switching simultaneously and terminating at different outputs.
>
> Input Skew ($t_{sk(i)}$) – The difference between two propagation delay times that originate at different inputs and terminate at a single output.
>
> Pulse Skew ($t_{sk(p)}$) – The difference between the propagation delay times t_{PLH} and t_{PHL} when a single switching input causes one or more outputs to switch.
>
> Process Skew ($t_{sk(pr)}$) – The difference between identically specified propagation delay times on any two samples of an IC at identical operating conditions.
>
> Limit Skew ($t_{sk(l)}$) – The difference between: 1. The greater of the maximum specified values of t_{PLH} and t_{PHL} and 2. The lesser of the minimum specified values of t_{PLH} and t_{PHL}.

The skew discussed here is the skew of propagation delays across the outputs of a device. More specifically, it is the difference between the largest value obtained for a propagation delay and the smallest value across all of the outputs. For example, if output 3 has the largest propagation delay t_{PLH} and output 14 has the smallest, then the output skew for this device would be the difference between the propagation delays for output 3 and output 14 (see Figure 1).

The majority of the curves presented in this paper consist of data taken on devices that have one output switching at a time. This produces a skew that should not be confused with the defined data sheet skew $t_{sk(o)}$. The data sheet value for $t_{sk(o)}$ is found by switching all of the outputs simultaneously. Two of the devices examined in this paper ('ABT16240, 'ABT16500A) include curves which present $t_{sk(o)}$ data.

Source of Data

The data used to produce the curves presented in this paper was extracted from the characterization data bases used to set the data sheets for the devices presented. The sample size of the data base is approximately thirty devices for each characterization lot (wafer) used.

The data was sorted so that the maximum skew for each device at a particular V_{CC} and temperature combination could be determined. Next, the maximum skew values were averaged to produce a data point for each transition. Further statistical analysis of this data was performed to calculate a standard deviation of the maximum skew across the devices. This value was then used to produce a three standard deviations data point for each V_{CC} and temperature combination. The data is presented as a family of curves across V_{CC} with each member of the family being an output skew versus temperature curve. The curves for each device are broken out by output transition (i.e. t_{PLH}, t_{PHL}). Each transition is further separated into a set of curves depicting the average skew across the devices and a set representing the average skew plus three standard deviations.

For those devices ('ABT16952 and 'ABT16500A) which have registers, the data path chosen for each device was the path which put the device in a transparent mode. Also, for the bidirectional devices ('ABT16245, 'ABT16952, and 'ABT16500A) the A-to-B direction was used.

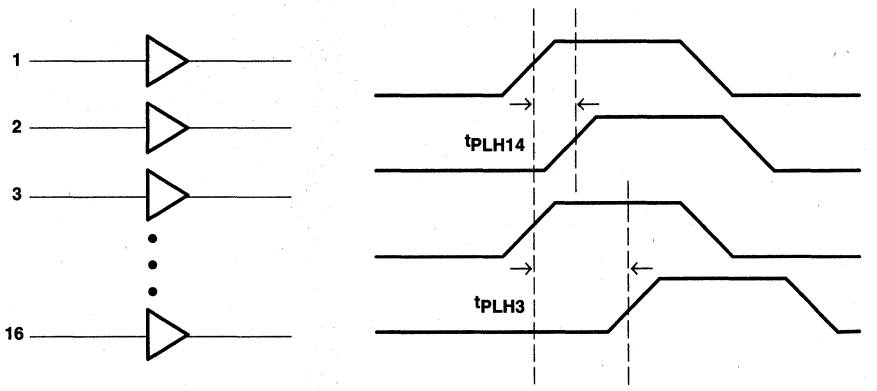


Figure 1. Skew = $|t_{PLH14} - t_{PLH3}|$

Sources of Error in Data

The data in this paper was taken on an IMPACT tester, which is a piece of automatic test equipment used to characterize integrated circuits. The tester is offset using a golden unit which has had data taken on a lab bench setup. It is this process of offsetting which is the main source of error in the data.

Briefly the tester is offset in the following manner: First the golden unit has its propagation delay measurements taken at 25°C and 85°C using a pulse generator as the source and an oscilloscope as the measurement unit. The golden unit is then placed on the IMPACT and the data is again taken. The difference between the two values is the offset. The 25°C offsets are used for the data taken at –55°C, –40°C and 25°C while the 85°C offsets are used at 85°C and 125°C.

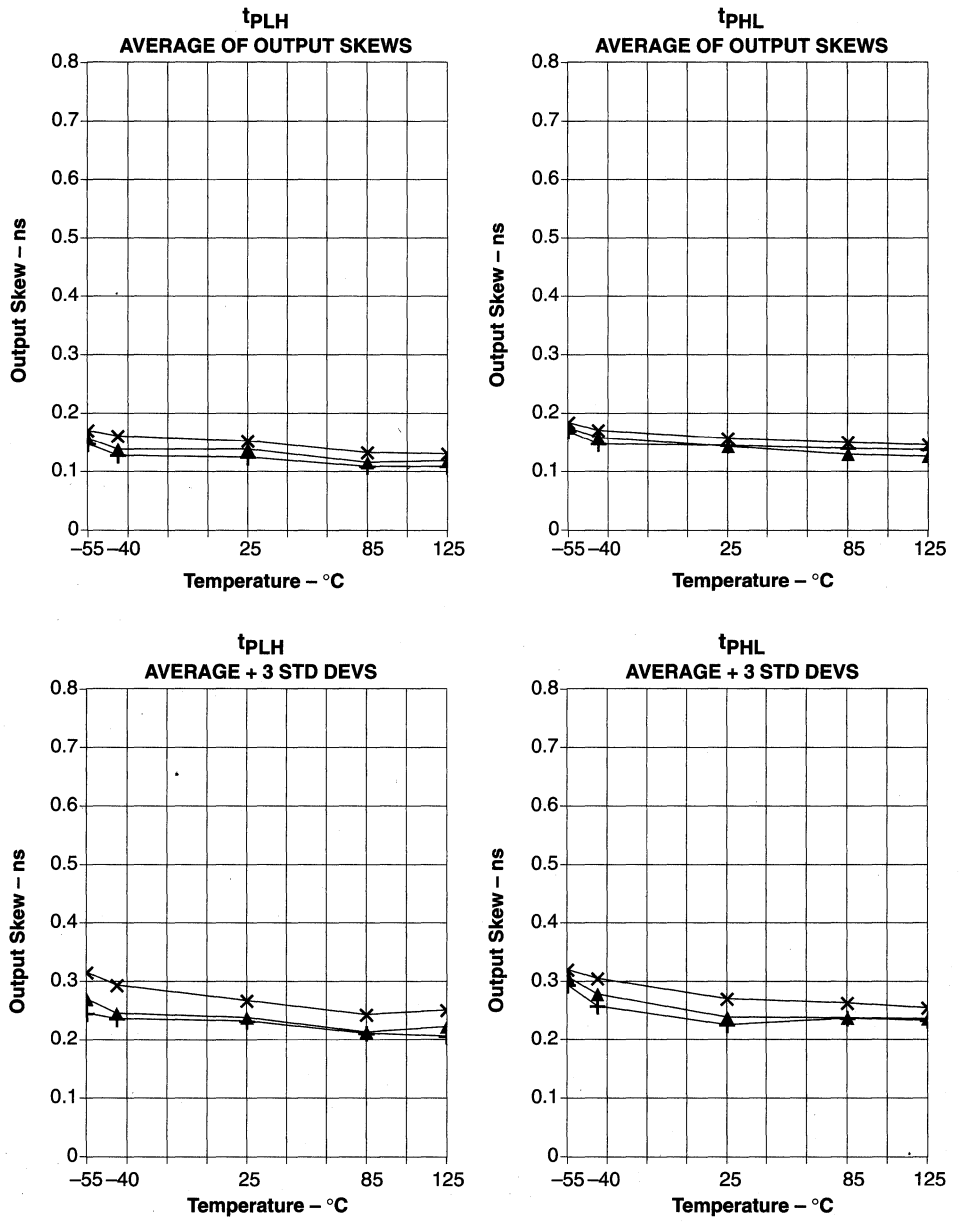
Great care is taken during this process to ensure that the induced error is kept to a minimum. For example, the boards are checked before use to ensure the output loads are correct, the oscilloscope is calibrated each day and the input signals are closely monitored to ensure that the intended signal is delivered to the golden unit.

This reduction in error is quite important in this application due to the fact that the average skews for the devices are about 200 ps. A 20-ps error in offsets translates into an approximate error of 10% in the output skew data.

However, it can be seen in the curves presented here that the error has been kept to a minimum and that the curves are fairly well behaved.

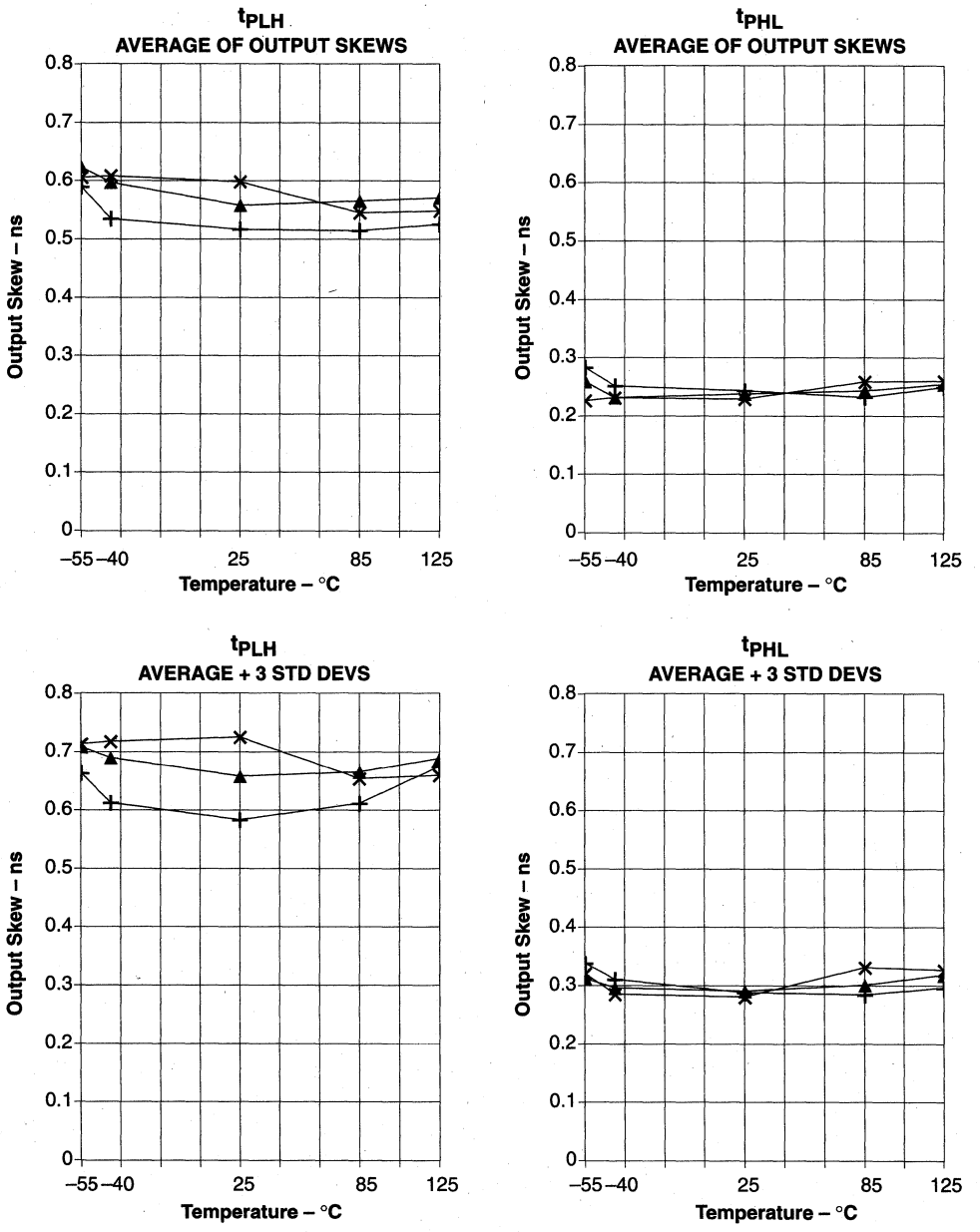
Conclusion

The family of curves presented in this paper demonstrates that the Texas Instruments Advanced BiCMOS family of devices can be expected to produce an average skew between outputs that will remain below 400 ps for devices with single switching outputs. Also, when a device has its outputs switching simultaneously, the average skew across the outputs can be expected to remain below 700 ps.



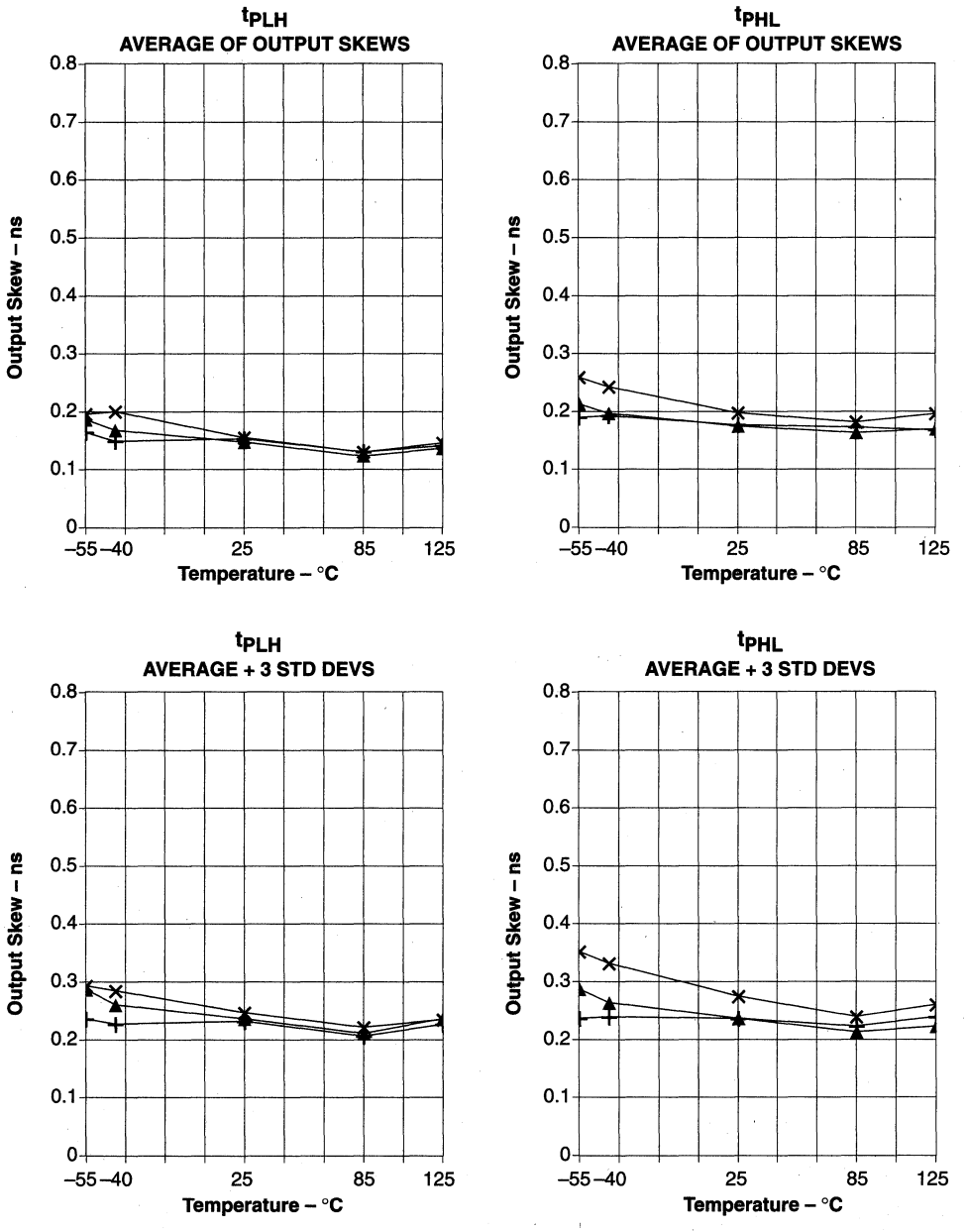
X – V_{CC} = 4.5 V, Y – V_{CC} = 5 V, +/ – V_{CC} = 5.5 V

Figure 2. 'ABT16240 – Single Switching



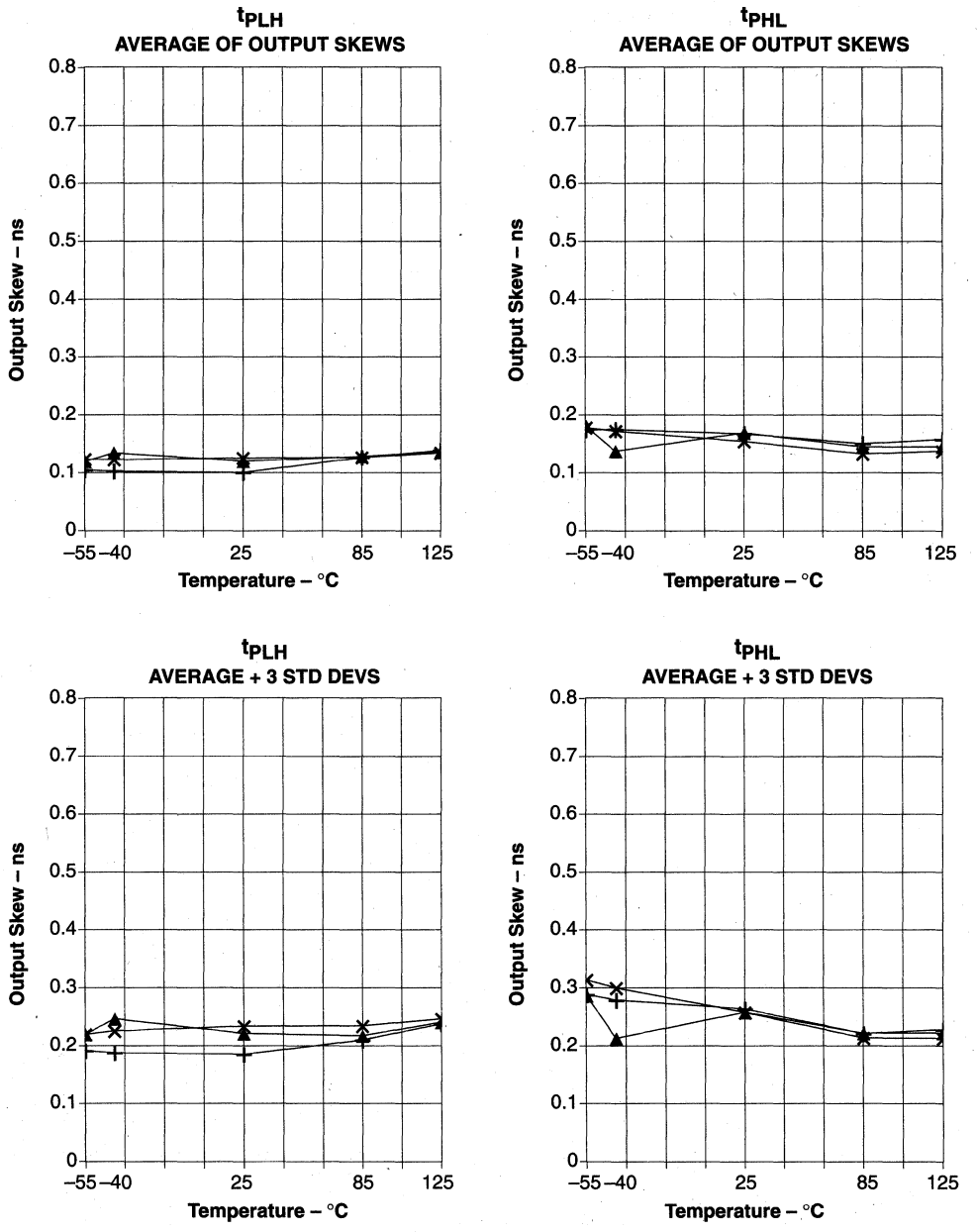
X – V_{CC} = 4.5 V, Y – V_{CC} = 5 V, +/ – V_{CC} = 5.5 V

Figure 3. 'ABT16240 – Simultaneous Switching



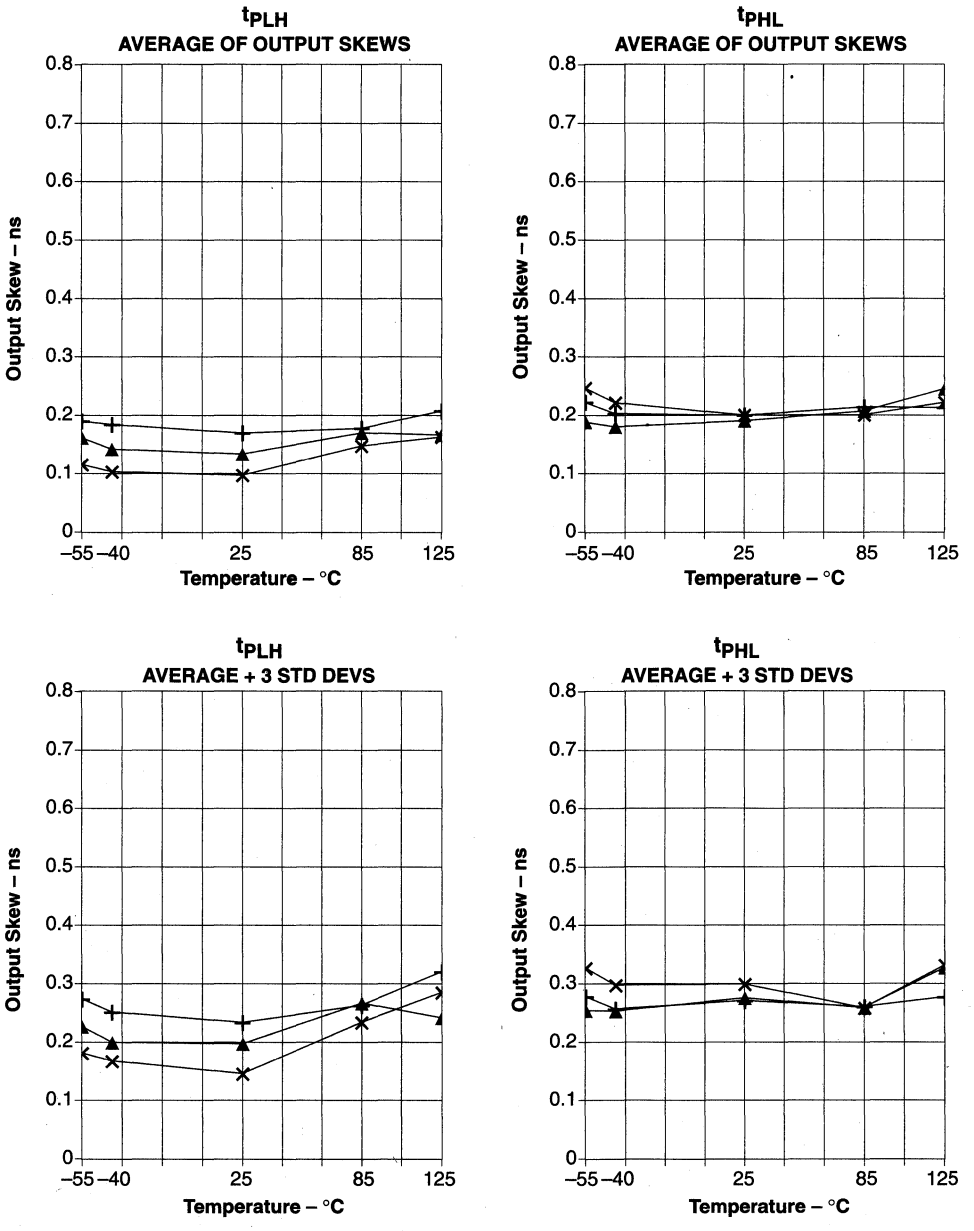
X – V_{CC} = 4.5 V, Y – V_{CC} = 5 V, +/ – V_{CC} = 5.5 V

Figure 4. 'ABT16245 – Single Switching



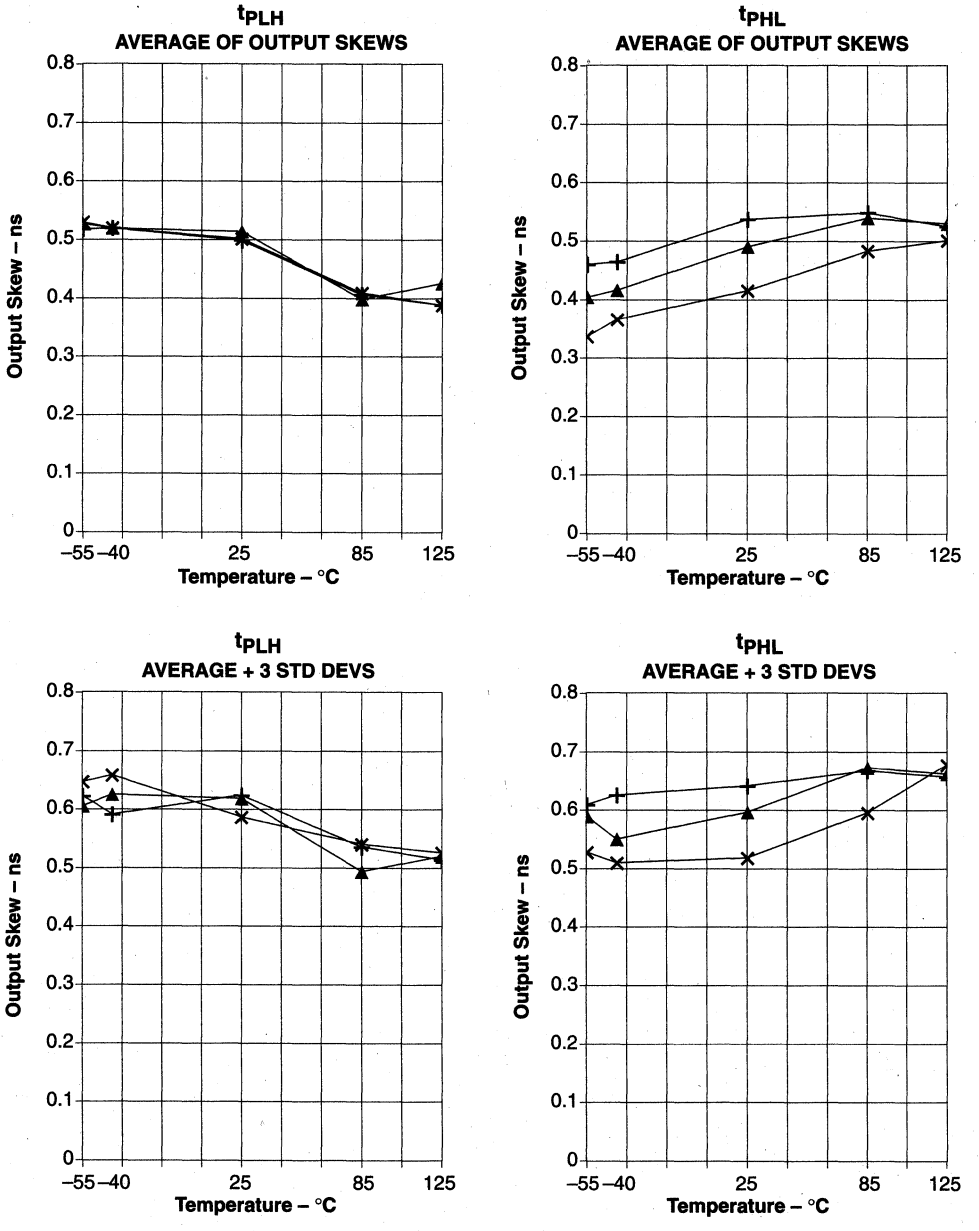
X – V_{CC} = 4.5 V, Y – V_{CC} = 5 V, + /– V_{CC} = 5.5 V

Figure 5. 'ABT16952 – Single Switching



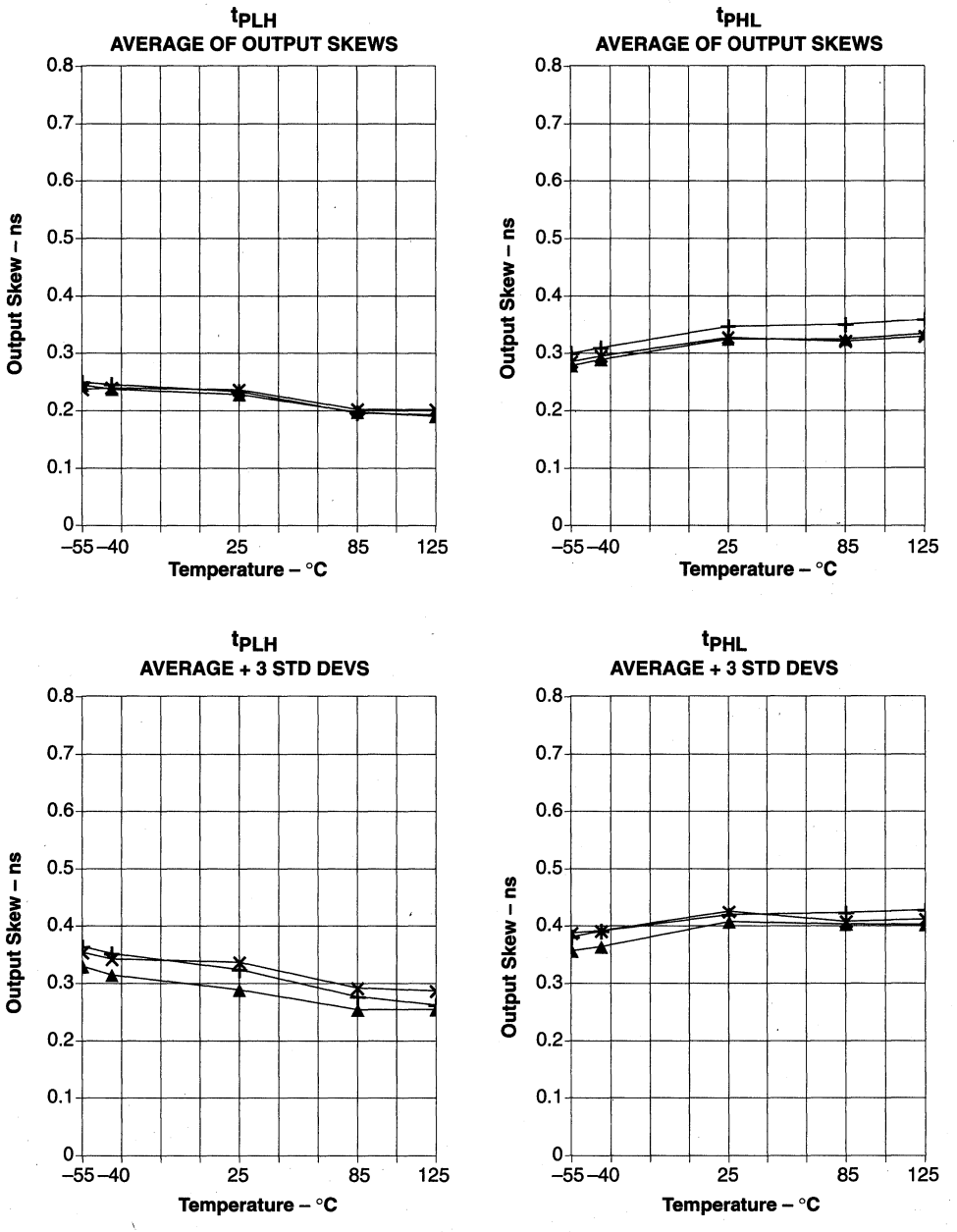
X – V_{CC} = 4.5 V, Y – V_{CC} = 5 V, + /– V_{CC} = 5.5 V

Figure 6. 'ABT16500A – Single Switching



X – V_{CC} = 4.5 V, Y – V_{CC} = 5 V, +/ – V_{CC} = 5.5 V

Figure 7. 'ABT16500A – Simultaneous Switching



X – V_{CC} = 4.5 V, Y – V_{CC} = 5 V, +/ – V_{CC} = 5.5 V

Figure 8. 'ABT244 – Single Switching

Mixing It Up With 3.3 Volts

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Contents

List of Illustrations

Introduction

The evolution to a 3.3-V supply voltage is being driven by a complex matrix of requirements. Leading the way are the characteristics of advanced semiconductor processing and the need to reduce system power without a corresponding tradeoff in system performance. Reduction of the horizontal and vertical feature sizes of transistors is the most common method of increasing the density of cells that can be contained in an integrated circuit. These feature sizes or geometries are typically represented as minimum process dimensions for advanced products such as dynamic random access memories (DRAMs).

DRAM manufacturers have forecasted that all 64M-bit versions will be developed for operation from a supply voltage of 3.3 ± 0.3 V. For 16M-bit DRAM products there is no such rule of thumb as certain vendors expect to operate from 3.3 V, while others will offer different product versions with differing voltage levels. An approach used by several manufacturers is to provide 5-V power supply operation externally with internal step-down conversion to 3.3 V. For static random access memories (SRAMs), manufacturers have announced that most 16M versions will operate at 3.3 V or lower (down to 2.7 V).

Typical 1M-bit DRAM geometries are on the order of 1.2 μm, and it is not a problem to apply a 5-V power supply to this type of product. However, as the feature sizes of DRAMs shrink, the stresses of 5-V operation can preclude their reliable operation due to high field-effect failures. One such effect is hot-carrier injection which over time increases the transistor's threshold, leading to eventual nonoperation. Another field-effect concern is the breakdown of the transistor's gate oxide causing internal shorts. Therefore, reducing the supply voltage is one way to ensure reliable operation of devices fabricated in state-of-the-art processes.

The reduction of V_{CC} from 5 V to 3.3 V reduces the power consumed by the device which increases system reliability while reducing costs associated with the removal of the heat. The power consumption of a device is primarily a function of its capacitive load, frequency of operation, and supply voltage. However, capacitive load and frequency have a linear effect on a device's power consumption while supply voltage has a square relationship. Because of this square relationship a small reduction in voltage significantly reduces the power consumed, as illustrated in Figure 1, and is a driving factor towards 3.3-V operation.

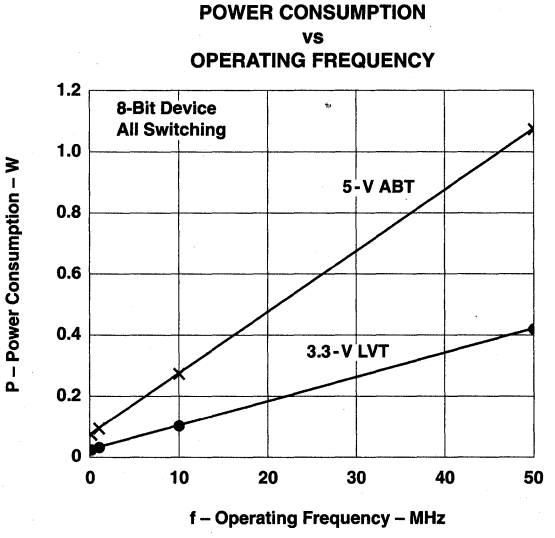

Figure 1. 3-V to 5-V Power vs Frequency Comparison

The Market for Low Voltage

User demand for low-voltage products can be grouped into specific brackets depending on their performance-power priorities. End equipments such as multiuser servers, engineering workstations, high-end desktop PCs, and other high-performance motherboards favor high performance over low power, but are interested in 3.3-V products to reduce or eliminate bulky, noisy cooling fans in the attempt to shrink external case size for better desktop fit. Some end equipments favor low power at the expense of high performance such as battery-powered notebooks and palmtop computers, portable test equipment, and point-of-sale terminals. A few end equipments require equal priority for high performance and low power such as laptop computers, automotive and air/space products.

The universal benefits to users of low-voltage products are higher reliability and lower cost. The higher reliability is relative to standard 5-V solutions and results from lower stress gradients on device junctions and oxides, lower buildup of heat due to lower power consumption, and improved signal integrity from the reduction in ground bounce and signal noise. Lower power consumption usually yields lower costs since power costs money to generate and heat costs money to dissipate. All things considered, it is desirable to use inexpensive plastic packages instead of metal or ceramic to dissipate heat. For battery users, an added benefit of the lower power consumption of low-voltage products is one of increased battery lifetime.

Of all the end-equipment groups which can benefit from the use of low-voltage products, it appears that demand will be initially driven by battery-operated computers. This market segment is defined by notebook and palmtop computers, as well as point-of-sale terminals which are designed to capture data at remote field sites and either store it for downloading later or transmit it real time via an on-board transmitter. The goal for these systems is to have a battery life of 8 to 10 hours, roughly the equivalent of one work day or the time to complete a transcontinental airplane trip.

The unregulated battery market is itself quite varied, however, because different batteries exhibit very different voltage characteristics between fully charged and discharged states. Two AA batteries provide for 3-V supply when charged, decreasing to about 2.7 V after use. Three NiCad batteries provide for a baseline 3.6-V supply fully charged but the spread actually runs from about 3.3 V up to 3.9 V. For now the unregulated battery market demands low-voltage products which are optimized to run from 2.7 V up as high as 3.9 V. Since performance is directly related to supply voltage, it is more important for device optimization to be extended down to 2.7 V, where devices will slow down appreciably.

There are some barriers for low-voltage acceptance in the short term. Specification standardization remains an issue. Also, the access to adequate supplies of 3.3-V devices can be a problem. Generally, DRAM memories are leading the way into 3.3-V operation with SRAM memories close behind. Coupled with the low-voltage microprocessors now available, systems are being implemented with the core components operating at 3.3 V, with volume requirements not beginning until the '94–'95 time frame. Hindering the migration to a full 3.3-V system is the availability of support products such as: disk drives, LCDs, A/D converters, RF transmitters, and EPROMS.

Migration to 3.3 V

The need to migrate to power supplies with supply voltages less than 3.3 V has been an issue since 1984 when two JEDEC standards were adopted. Standard 8.0 was intended to address both regulated (3-V to 3.6-V) and unregulated (2-V to 3.6-V) battery applications. Standard 8.1 was intended to address higher-performance applications operating from a regulated power supply that could interface to a standard 5-V TTL device as well as a low-voltage device. Essentially Standard 8.0 established regulated low-voltage CMOS (LVCMOS) and unregulated low-voltage battery-operated (LVBO) interfaces, and Standard 8.1 established the low-voltage TTL (LVTTL) interface.

Committee members have since determined that the original two standards are inadequate. Since most systems currently require a TTL interface, Standard 8.1 LVTTL is the most critical one being reviewed now. When ratified, the new LVTTL standard will present methods for interfacing with 5-V systems and contain a provision for battery-operated systems. Until this happens, a generic lack of compatibility will exist between the various 3.3-V and 5-V interfaces.

Existing solutions for 3.3-V operation have historically been 5-V products and processes characterized for 3.3-V operation. A CMOS process is typically chosen because of the scaling effect of the inverter thresholds with respect to the supply voltage. HCMOS and Advanced CMOS devices support both 5-V and 3.3-V operation by this method. One drawback is slower propagation delay when compared to parts specifically designed for 3-V operation. A limitation of many of these devices is their inability to directly interface to a 5-V system when running off a 3.3-V supply, due to diodes from the input and input/output (I/O) pins to V_{CC}. This limits input voltages to V_{CC} + 0.5 V and limits direct connection to a 5-V system.

Mixed-Mode Operation

This dilemma of device incompatibility between the large installed base of 5-V systems with the newly emerging 3.3-V systems is a serious industry concern. Mixed-mode operation allows for direct communication between the two systems. Devices which support this mode must be designed for maximum input voltages of 5.5 V without any long-term reliability issues. Another concern is that the output drive must be capable of driving a standard-TTL backplane, while still providing for rail-to-rail switching for compatibility with 3-V CMOS systems.

Figure 2 compares the standard-TTL dc interface levels with two of the emerging low-voltage standards. Low-voltage CMOS (LVCMOS) is a pure CMOS specification that specifies low current rail-to-rail output drive along with input voltage levels, V_{IH} and V_{IL}, which are ratios of V_{CC}. Low-voltage TTL (LVTTL) utilizes the standard-TTL input levels of 0.8 and 2 V as well as specifying a higher dc output drive than LVCMOS. To ensure interoperability between these three varied standards, a multipurposed low-voltage interface device must meet all of the requirements of the three different specifications.

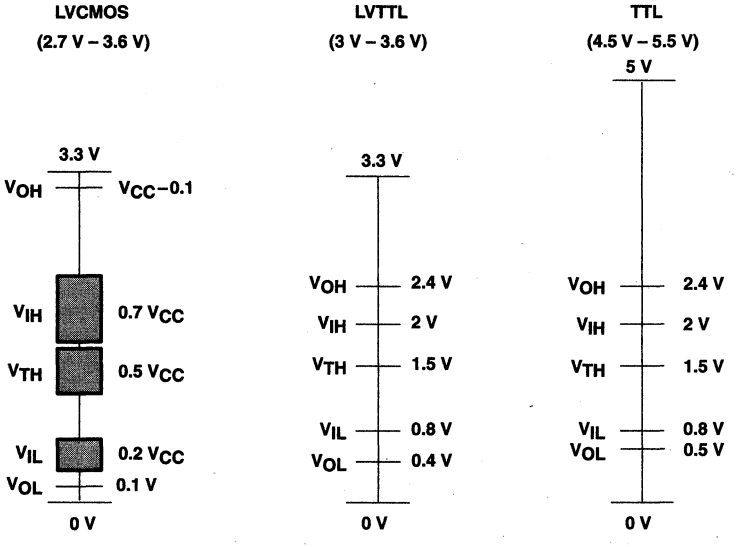

Figure 2. Comparison of 3.3-V and 5-V Interfaces

LVT Family Characteristics

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic parts capable of mixed-mode operation. The LVT series of parts rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT devices, and provides the following family characteristics:

5.5-V maximum input voltage

Specified 2.7- to 3.6-V supply voltage

I/O structures that support power-on (live) insertion

Standard TTL output drives of:
V_{OH} = 2 V at I_{OH} = –32 mA
V_{OL} = 0.55 V at I_{OL} = 64 mA

Rail-to-rail switching for driving CMOS

Maximum supply currents of:
$I_{CC(L)}$ = 15 mA
$I_{CC(H)}$ = 250 µA
$I_{CC(Z)}$ = 250 µA

Propagation delays of:
t_{pd} < 4.6 ns
t_{pd} (LE to Q) < 5.1 ns
t_{pd} (CLK to Q) < 6.3 ns

Surface-mount packaging support including fine-pitch packages:
48- and 56-pin SSOP for LVT Widebus™
20- and 24-pin TSSOP for standard LVT

LVT input/output characteristics

Figure 3 shows a simplified LVT output and illustrates the mixed-mode signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices, as shown in Figure 4, providing the dc drive needed for existing 5-V backplanes and allowing for a simple solution to reduce system power via the migration to 3.3-V operation.

Not only can LVT devices operate as 3-V-to-5-V level translators by supporting input or I/O voltages of 5.5 V with V_{CC} = 2.7 to 3.6 V, the inputs can withstand 5.5 V even when V_{CC} = 0 V. This allows for the devices to be used under partial system power-down applications or when live insertion is required.

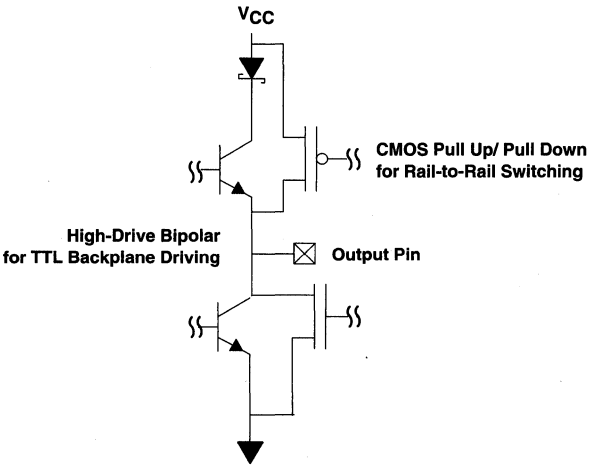

Figure 3. Simplified LVT Output Structure

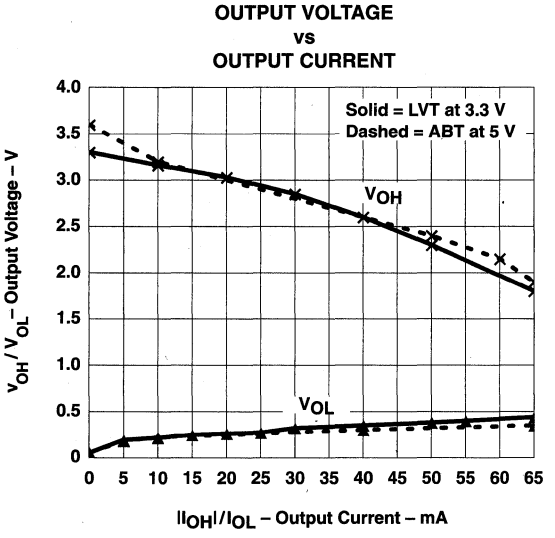

Figure 4. ABT vs LVT Output Drive Comparison

Bus Hold

Many times devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, ± 100 μA, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately ± 500 μA, to toggle the state of the input. This current is negligible when compared to the magnitude of current that is needed to charge a capacitive load, and does not affect the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent interface between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live insertion or partial-power applications while providing low-input leakage currents. The outputs are capable of driving today's 5-V backplanes with a considerable reduction in the device's power consumption and are packaged in state-of-the-art fine-pitch surface-mount packages.

Package Thermal Considerations

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Contents

List of Illustrations

Abstract

In order to meet current and future system requirements of increasing speed and decreasing size, integrated circuit manufacturers are pushing the edge on existing packaging technology. No longer is a component's performance determined by process technology alone but also by the thermal limitations of its package. As a leader in package technology, Texas Instruments has introduced a number of fine pitch packages and is acutely aware of the thermal considerations which must be examined by systems designers. This paper is intended to create awareness and understanding of thermal issues and to explore factors which influence thermal performance.

Introduction

Thermal awareness became an industry concern when surface mount (SMT) packages began replacing through hole (DIP) packages in PCB designs. Circuits operating at the same power enclosed in a smaller package meant higher power. To add to the issue, systems were requiring increased through-put which resulted in higher frequencies, increasing the power density even further. Not only are these same concerns still haunting designers today, they are progressively getting more severe.

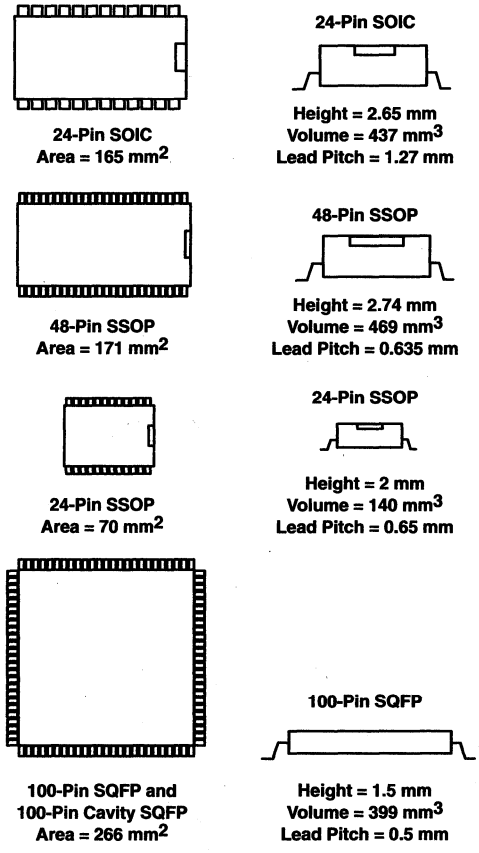


Figure 1. Advanced Packages

A glance at Figure 1 will explain part of the reason for increased attention to thermal issues. As a baseline for comparison the 24-pin SOIC is pictured along with several fine-pitch packages supplied by TI, including the 24-pin SSOP (shrink small-outline), 48-pin SSOP and the 100-pin SQFP (shrink quad flat pack). The 24-pin SSOP (8, 9, 10 bits) allows for the same circuit functionality of the 24-pin SOIC to be packaged in less than half the area, while the 48-pin SSOP (16, 18, 20 bits) occupies just slightly more area but has twice the functionality of the 24-pin SOIC. This same phenomena is expanded even further with the 100-pin SQFP (32 and 36 bits) which is the functional equivalent of four 24-pin or two 48-pin devices with additional board savings over that of the SSOP packages. As the trend in packaging technology continues to give way to smaller packages, attention must be focused on the thermal issues this creates.

Reliability

The overriding effect of increased power densities in integrated circuits is a decrease in overall system reliability. A direct relationship exists between junction temperature and reliability which can be shown using the Arrhenius equation.

$$AF = Exp\ [Ea/k(1/T1 - 1/T2)] \quad (1)$$

Where:
AF = acceleration factor
Ea = activation energy (eV)
k = Boltzmann's constant (8.617×10^{-5} eV/K)
T1 = use junction temperature (K)
T2 = stress junction temperature (K)

The acceleration factor can be used to determine the failure rate of a given component.

$$FR\ (failure\ rate) = 1/AF \quad (2)$$

Table 1 provides an example of a device with an initial junction temperature of 100°C and the calculated failure rate decrease as the in use junction temperature is lowered. The data given in Table 1 indicates that lower junction temperature will result in increased system reliability.

Table 1

TEMPERATURE °C	AF	FR	% FR DECREASE
100	1	1	0
90	1.54	0.65	35
80	2.41	0.41	59
70	3.9	0.26	74
60	6.48	0.15	85

Ea = 0.5eV
% FR decrease = 1 – FR

A better understanding of the factors which contribute to junction temperature (Tj) will provide a system designer with more flexibility when attempting to solve thermal issues. Device junction temperature is determined by the following:

$$Tj = Ta + [\Theta_{JA} \times P_T] \quad (3)$$

Where:
Tj = junction (die) temperature (°C)
Ta = ambient temperature (°C)
Θ_{JA} = thermal resistance of the package from the junction to the ambient (°C/W)
P_T = total power of the device (W)

Among the things that can alter junction temperature are lower chip power consumption, longer trace length, heat sinks, forced airflow, package mold compound, lead frame size and material, surface area, and die size. Some of these are mechanically inherent to a particular package while others are controlled by the designer and are application specific. To understand which variables can be influenced by practicing good thermal design techniques requires a more detailed investigation of power considerations as well as thermal resistance measurements.

Power Consumption

One way to lower the junction temperature (Tj) of a device, thus improving reliability, is to lower the power consumption. A variety of options are available to help achieve this, such as, low power process technologies, reduced output swing, and reduced power supply voltage. A close look at the power performance and advantages of several popular logic families will assist the designer when choosing what best fits his/her needs.

The choices available from Texas Instruments for high speed bus-interface ranges from standard bipolar (F) to advanced CMOS (ACL/ACT) to state-of-the-art BiCMOS (BCT) and advanced BiCMOS (ABT). Figures 2–4 show current consumption comparisons of '244 functions for these technologies across frequency. As expected, the bipolar device consumes more current than the CMOS device at lower frequency, but as frequency increases this relationship no longer holds true. In fact, there exists a region in the frequency range where the CMOS device will consume more current than the bipolar device. The point at which they are equal is referred to as the *cross-over* frequency. Notice the low frequency where the cross-over point for ABT and ACT occurs.

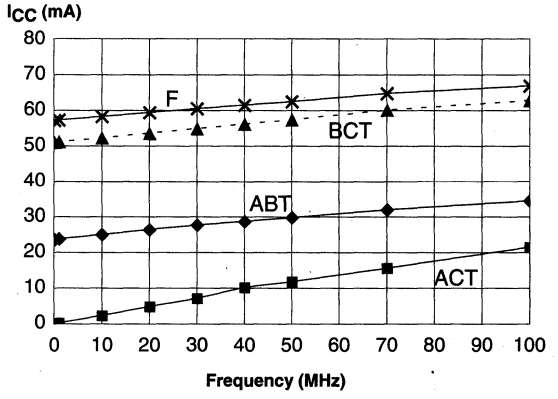


Figure 2. I_{CC} vs Frequency (One Switching, Unused Outputs Low)

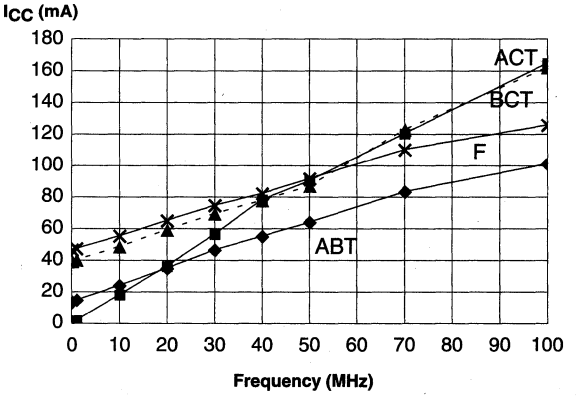


Figure 3. I_{CC} vs Frequency (All Outputs Switching)

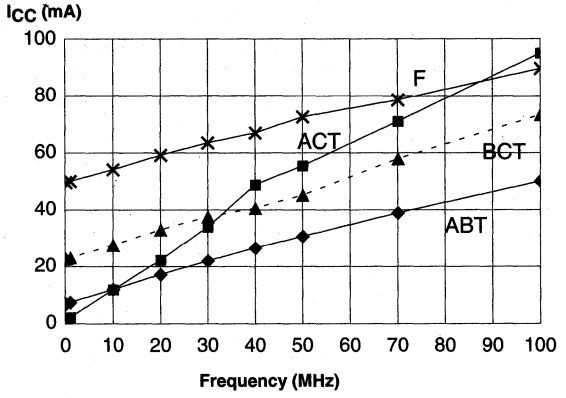


Figure 4. I_{CC} vs Frequency (All Switching, 50% Duty Cycle Enabled)

Typical applications for bus-interface devices require them to be disabled or in the *stand-by* mode during certain periods of time, for instance, while other devices access the bus. This can result in a large decrease in current consumption for ABT, BCT, and ACT devices which have low stand-by current. These values are given in the data sheets as I_{CC} for ACT and I_{CCZ} for ABT (250 μA) and BCT (≅ 10 mA). Current consumption data versus percent duty cycle enabled is shown in Figure 5. The frequency of the data is held constant at 25 MHz and all outputs are switching.

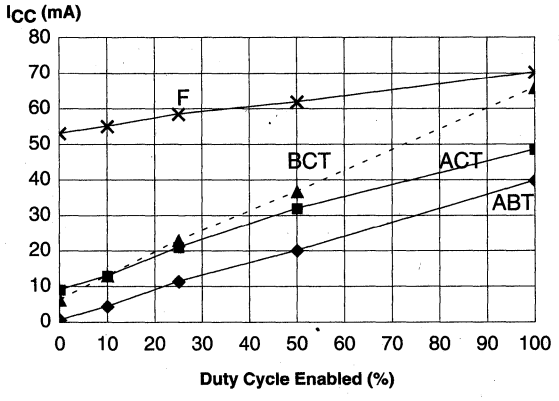


Figure 5. I_{CC} vs Duty Cycle Enabled (25 MHz)

The power consumption data provided is limited to a small range of variations, however, using this data along with standard formulas power consumption can be calculated for specific applications.

Power Calculations

When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account.

Both bipolar and BiCMOS devices have varying static current levels depending on the state of the output (I_{CCL}, I_{CCH}, I_{CCZ}), while a CMOS device has a single value for I_{CC}. (These values can be found in the individual data sheets.) ACT and ABT inputs when driven at TTL levels will also consume additional current because they may not be driven all the way to Vcc or GND, therefore the input transistors are not completely turned off. This value is known as ΔI_{CC} and is also provided in the datasheet.

Dynamic power consumption results from the charging and discharging of both internal parasitic capacitances as well as external load capacitance. The parameter for ACT and AC and devices which accounts for the parasitic capacitances is known as C_{pd} and is obtained using the following formula, and is found in the datasheet.

$$C_{pd} = [I_{CC}\ (\text{dynamic})/(V_{CC} \times Fi)] - C_L \quad (4)$$

Where:

Fi = input frequency (Hz)
V_{CC} = supply voltage (V)
C_L = load capacitance (F)
I_{CC} = measured value of current into the device

Although a C_{pd} value is not provided for ABT, BCT, or F devices, I_{CC} versus frequency curves display essentially the same information. The slope of the curve provides a value in the form of mA/(Mhzxbit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device (without the load current).

The following equations can be used to calculate total power for CMOS, Bipolar, and BiCMOS devices.

$$P_T = P_{S(\text{tatic})} + P_{D(\text{ynamic})} \quad (5)$$

CMOS

AC (CMOS-level inputs)

$$P_S = V_{CC} \times I_{CC}$$
$$P_D = [(C_{pd} + C_L) \times V_{CC}^2 \times f_1]\ N_{sw} \quad (6)$$

ACT (TTL-level inputs)

$$P_S = V_{CC}\ [I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)]$$
$$P_D = [(C_{pd} + C_L) \times V_{CC}^2 \times f_1]N_{sw} \quad (7)$$

BiCMOS/Bipolar

$$P_S = V_{CC}\ [DC_{en}(N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T)$$
$$+ (1\text{–}DC_{en})Iccz] + (N_{TTL} \times \Delta Icc \times DC_d) \quad (8)$$

Note: $\Delta I_{CC} = 0$ for bipolar devices

$$P_D = [DC_{en} \times N_{sw} \times V_{CC} \times f_1 \times (V_{OH} - V_{OL}) \times C_L]$$
$$+ [DC_{en} \times N_{sw} \times V_{cc}\ f_2 \times (\text{mA/MHz} \times \text{bit})] \times 10^{-3} \quad (9)$$

Where:

V_{CC} = supply voltage (V)
I_{CC} = power supply current (A) from the datasheet)
I_{CCL} = power supply current when outputs are in the low state (A) (from the datasheet)
I_{CCH} = power supply current when outputs are in the high state (A) (from the datasheet)
I_{CCZ} = power supply current when outputs are in the high–impedance state (A) (from the datasheet)
ΔI_{CC} = power supply current when inputs are at a TTL level (A) (from the datasheet)
DC_{en} = % duty cycle enabled (50% = 0.5)
DC_d = % duty cycle of the data (50% = 0.5)
N_H = number of outputs in the high state
N_L = number of outputs in the low state
N_{sw} = total number of outputs switching
N_T = total number of outputs
f_1 = operating frequency (Hz)
f_2 = operating frequency (MHz)
V_{OH} = output voltage in the high state (V)
V_{OL} = output voltage in the low state (V)
C_L = external load capacitance (F)
mA/(Mhzxbit) = slope of the I_{CC} vs frequency curve

Thermal Resistance Values

Design trends requiring board size reduction have made way for circuit manufacturers to produce fine-pitch packages which appear to threaten the reliability of systems due to further thermal constraints. As a leader in packaging technology, Texas Instruments has done considerable research into the validity of traditional thermal measurements and data provided by circuit manufacturers.

Unlike datasheet parameters, where the industry has adopted a standard load for measurement (50 pf, 500 Ω), the measurement of Θ_{JA} has no standard to which all manufacturers comply. The problem facing the designer wishing to make comparisons of thermal data from several manufacturers is that this could be an apples to oranges type comparison. As a result, a software package has been developed at TI to allow designers to obtain thermal data based on their specific application.

The validity and usefulness of the traditional approach to presenting Θ_{JA} values became a pressing issue when TI and another manufacturer measured an identical package and obtained results which varied by 40%. Extensive research led to the conclusion that the methodology used to measure Θ_{JA} did not cause the discrepancy but the physical aspects such as trace length, trace width, number of devices per board, and proximity of the other devices did.

To demonstrate the extreme impact of trace length alone, Figure 6 shows graphs of the Θ_{JA} values for Texas Instruments 48-pin shrink small-outline package (SSOP) at 0 lfm and 250 lfm with varying trace lengths. The 48-pin SSOP is pictured in Figure 1 for a side by side comparison with the standard 24-pin SOIC, the 24-pin SSOP and the 100-pin SQFP. The data in Figure 6 clearly shows the need for more complete thermal data, not simply a single data point.

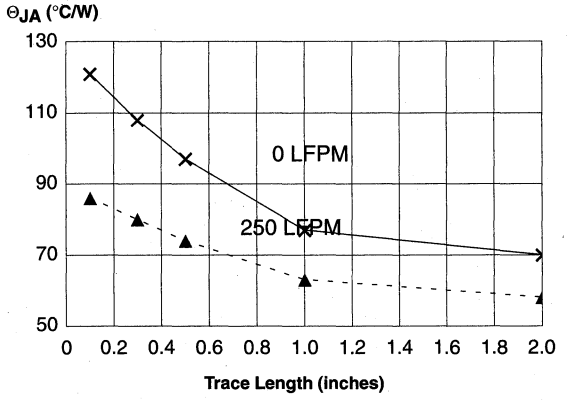


Figure 6. 48-Pin SSOP Θ_{JA} vs Trace Length

There are, of course, other methods to lower the Θ_{JA} of a device. Using heat sinks or blowing air across a device will certainly improve the ability to remove heat from its surface. Figure 7 provides Θ_{JA} data for the 48-pin SSOP with trace lengths of 200 mils and 1 inch while varying the amount of airflow. Although many applications tend to limit the amount of airflow allowed, it provides excellent benefits when possible.

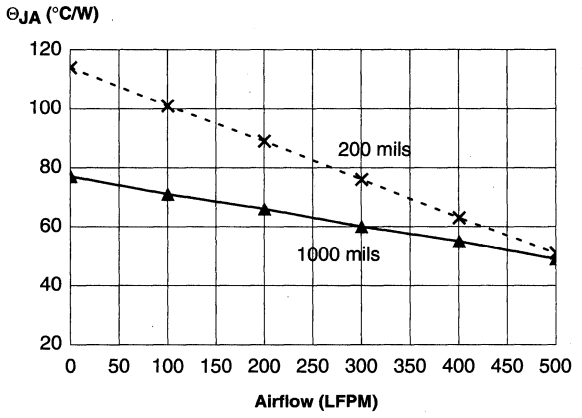
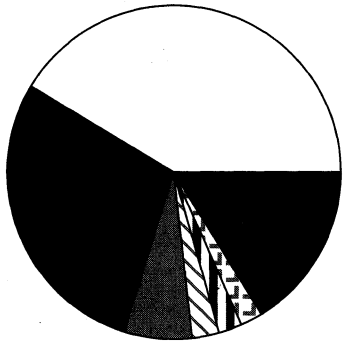


Figure 7. 48-Pin SSOP Θ_{JA} vs Airflow

A comparison was made of several variables which have a direct effect on Θ_{JA} values. This data is shown in Figure 8. Surprisingly, the major contributing factor is trace length not airflow. Once again, this validates the need for improvement not necessarily in the test methodology used to calculate Θ_{JA} values, but certainly in the way they are provided.



VARIABLE	RANGE	% CONTRIBUTION
Trace Length	75 mils – 2000 mils	41.4
Airflow	0 LFM – 500 LFM	28.8
Board Extension After Trace	0 mils – 400 mils	6.5
Board Extension After Package End	0 mils – 755 mils	2.6
Trace Thickness	1 oz – 2 oz	2.2
Trace Width	3 mils – 15 mils	2.1
Power	0.5 W – 1.5 W	0.1
Total Interactions Between Factors		16.3

Figure 8. 48-/56-Pin SSOP K-Factor Board Modeling

Texas Instruments has taken the step of providing Θ_{JA} values for a variety of packages (including the SOIC, SSOP and QSOP) in a user-friendly software package. The program allows the designer to specify his/her own conditions such as trace length, airflow, proximity of other devices, and trace width in order to obtain realistic thermal solutions.

Conclusion

How can a system avoid being a reliability nightmare in today's world where:

- Eight-bit devices are being replaced by 16 and 32 bits in a single package, increasing the power.
- Higher operating frequencies add to the increase in power.
- Fine-pitch packages are reducing the amount of available surface area to remove heat from a device.

Semiconductor manufacturers must take the first step and provide realistic and useful thermal information which will provide designers key variables to focus on for thermal management.

For Further Information

Thermal Software

Contact the factory – (903) 868-7682

Power Dissipation

Advanced CMOS Logic Designer's Handbook, Texas Instruments, 1988

SSOP Designer's Handbook, Texas Instruments, 1991

Recent Advancements in Bus-Interface Packaging and Processing

Ken Ristow
Advanced System Logic – Semiconductor Group
Texas Instruments Incorporated

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Contents

List of Illustrations

Introduction

Over the past several years the advancements in semiconductor processing have been combined with advanced surface mount packages to offer solutions to board area concerns, as well as, providing for increased system performance. Figure 1 compares the reduction of the package's lead pitch to that of both CMOS and BiCMOS transistor geometries. This paper will explore the different types of fine pitch logic packages and the bus interface solutions provided when they are combined with sub-micron semiconductor processes.

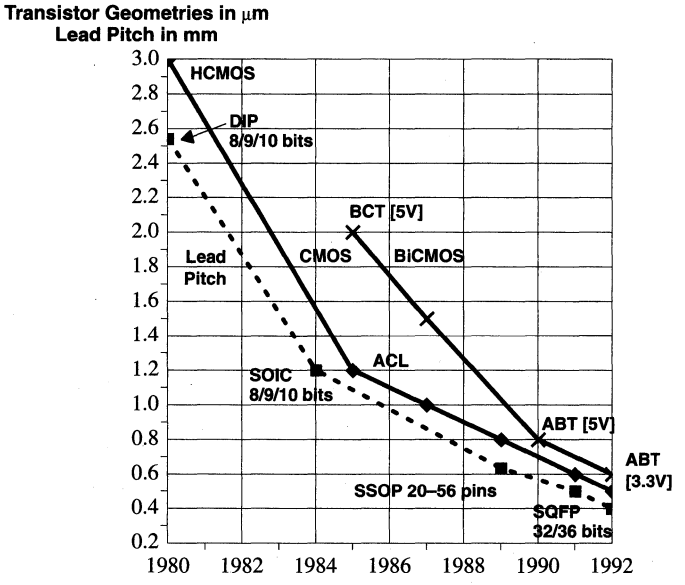


Figure 1. Packaging/Processing Evolution

Evolutions in Device Packaging

With the need for increased functionality in less board area has come the consolidation of much of the board's logic into higher complexity devices. In many cases the discrete logic parts that remain, primarily interface/bus drivers, must occupy the board area leftover after the higher level chips, i.e., microprocessor, ASICs, memory, etc., have been laid out. To meet this task the standard small-outline Integrated circuit (SOIC) has evolved in two distinct paths. One path reduces the package's area and volume (see Figure 2), and the other increases the bit density of the device (see Figure 3).

One method to increase bit density is to keep the number of pins constant while reducing both the lead pitch and package area. The 20/24 pin SSOPs utilize a 0.65-mm lead pitch to achieve over a 50% reduction in area, compared to their standard SOIC counterparts. The package height is also reduced from 2.65 mm for the SOIC to 2 mm for the 20/24-pin SSOPs. This reduction in volume translates into tighter board to board spacing, allowing for denser memory arrays.

The advent of the Personal Computer Memory Card International Association (PCMCIA) standard has required that the package height be reduced even further, thus spawning the thin small-outline package (TSOP). This package utilizes 0.65-mm lead pitch and has a maximum device height of 1.1 mm. With an area of 59 mm^2, this package utilizes 86% less volume than the standard 24-pin SOIC, facilitating the use of logic functions on these cards.

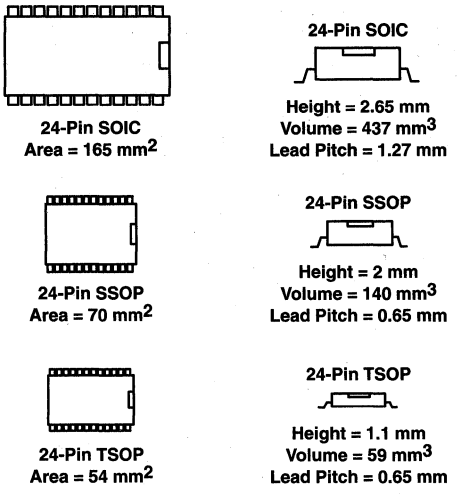


Figure 2. 24-Pin Surface Mount Comparison

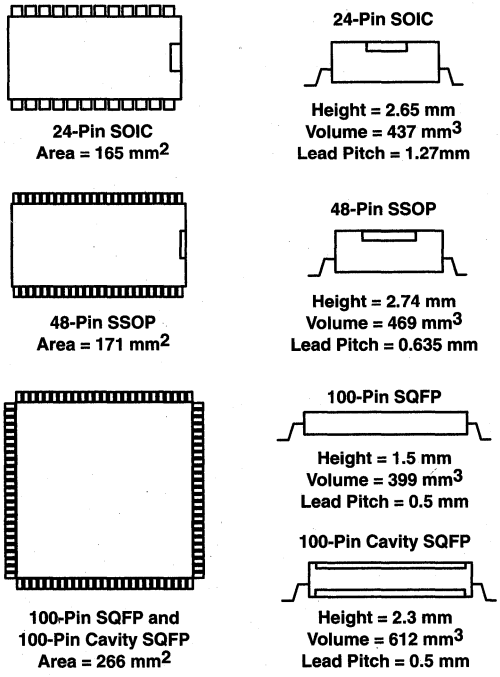


Figure 3. High Pin-Count Comparison

Another way to increase bit density is to reduce the lead pitch of the package. The 48/56-pin shrink small-outline package (SSOP) halves the lead pitch of the SOIC package from 1.27 mm to 0.635 mm, allowing for twice the number of I/0 pins in the same board area. Eight-, nine-, and ten-bit functions now become 16-, 18-, and 20-bit parts. The 100-pin shrink quad flat package (SQFP), along with the high-power cavity-SQFP, further reduce the lead pitch to 0.5 mm. These packages double the bit density over the 48-pin SSOP with only a 50% increase in area. Both of these high pin count packages allow for 32- and 36-bit logic functions, providing for efficient buffering of today's 32- and 64-bit bus widths.

Thermal Impedances of Fine-Pitch Packages

As package area decreases, which is the case for the 20- and 24-pin SSOP and TSOP, the thermal impedance of the package to the ambient environment (Θ_{JA}) increases. Figure 4 illustrates the fact that this relationship is almost linear, and for a 50% reduction in area, Θ_{JA} doubles for the 24-pin SSOP and TSOP. Because of the higher Θ_{JA}, additional attention must be given to the power dissipation of the device to insure proper operation.

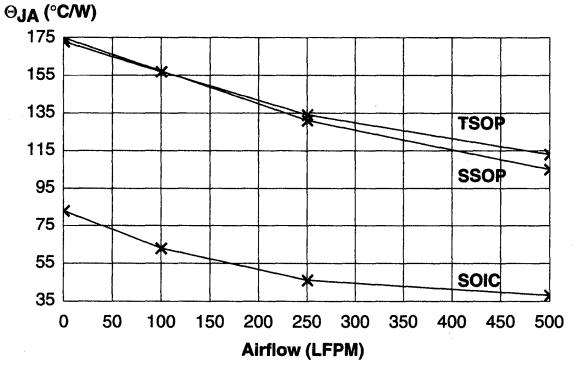


Figure 4. Θ_{JA} vs Airflow for 24-Pin Packages

A similar power consideration occurs with the high pin count packages due to the increased number of bits causing higher power dissipation per package. Figure 5 compares Θ_{JA} for the 24-pin SOIC, 48-pin SSOP, 100-pin SQFP, and cavity SQFP. The cavity package mounts the lead frame directly to one of the metal lids of the package. This mounting provides a direct path for the heat to flow from the die to the ambient environment. This package accommodates both cavity up or down assembly allowing for both conduction, into the board, or convection, into the ambient, cooling.

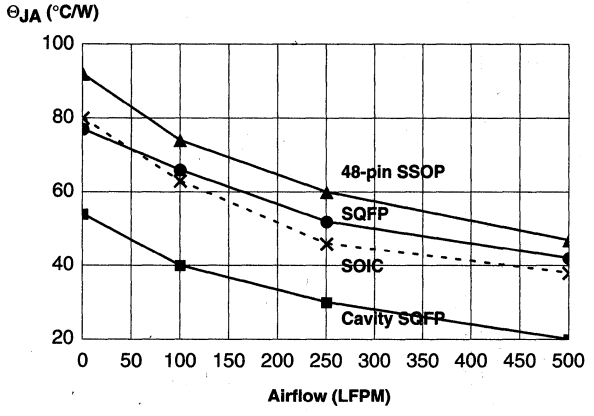


Figure 5. Θ_{JA} vs Airflow

One factor influencing Θ_{JA} is the trace length that is connected to the package lead finger. This is because some of the heat is taken out of the package through the lead and dissipated into the board as well as through the package top and into the ambient air. Non-standard trace length factors have been identified as a major contributing factor in differences between different manufacturer's published thermal values. Figure 6 shows the effect that trace length has on the 48-pin SSOP's Θ_{JA}.

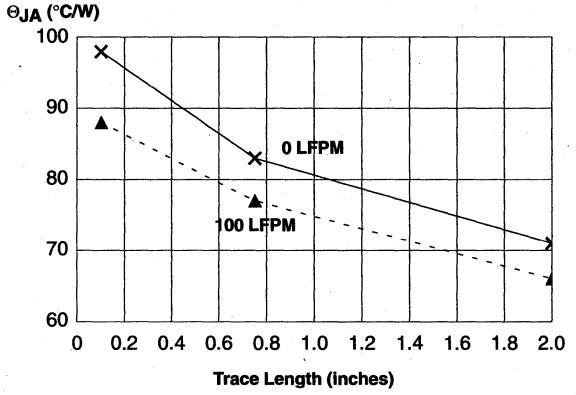


Figure 6. 48-Pin SSOP Θ_{JA} vs Trace Length

Evolutions in Device Processing

With the improvements to microprocessor clock rates and memory access times, bus-interface devices have become a larger percentage of the total bus cycle time. To keep pace with the need for faster logic many semiconductor manufactures are utilizing sub-micron BiCMOS processes, utilizing shorter gate lengths and thinner gate oxide for device speed improvements. The reductions in transistor area result in less intrinsic capacitance allowing faster internal gate delays, as well as lowering the output capacitance (Ci/o). With a lower Ci/o, ABT devices minimize their impact to system loading.

In a transmission line environment, when the driver's edge rate is less than twice the line's propagation delay, distributed output loading has the effect of reducing the characteristic impedance (Zo) of the transmission line. The higher the distributed capacitive load, the lower the apparent impedance, making it harder for the driver to switch the line on the incident wave. This well known transmission line loading equations is:

$$Z'_o = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} \quad (1)$$

where Z_o is the line's unloaded characteristic impedance, C_o is its intrinsic capacitance per unit length, and C_d is the distributed capacitive load per unit length.

Figure 7 shows how the a device's output capacitance can lower a line's impedance, as in the case of a backplane. If the effects of the other board capacitance contributors – connectors, vias, and trace stubs, are assumed to be constant regardless of the device used, and thus ignored, a comparison of transmission line loading between different technologies can be made.

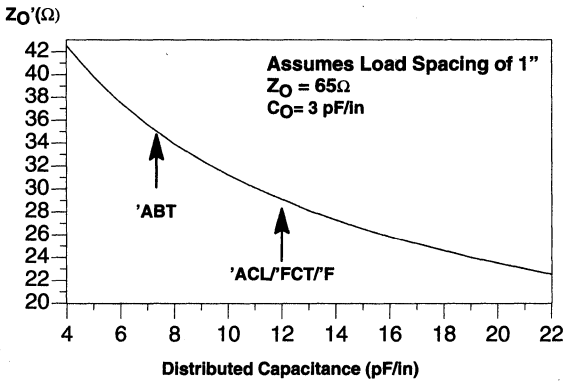


Figure 7. Loaded Z_O vs Distributed Capacitance

3.3-V Operation

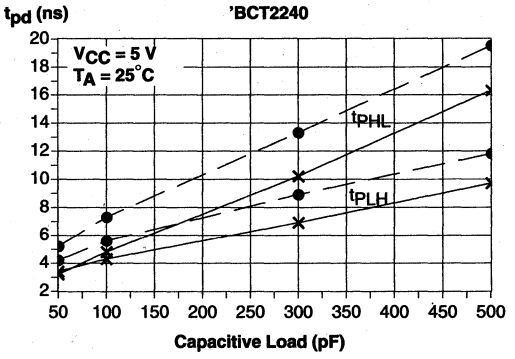
As process geometries move towards gate lengths of 0.5 μ and below, coupled with the desire for lower power consumption, 3.3-V operation becomes necessary. Because the migration to 3.3 V will be gradual, gated by the availability of semiconductor functions, the need for mixed signal level operation will be critical for bus interface devices. That is the input and I/O pins will be able to have input voltage levels up to 5.5 V without any conduction paths to V_{CC}. The outputs should also be capable of driving a standard 5-V backplane, which would translate into drive currents of at least –15 mA of I_{OH} and 64 mA of I_{OL}.

Advanced Bus-Interface Solutions

Memory Driver Usages for the SSOP

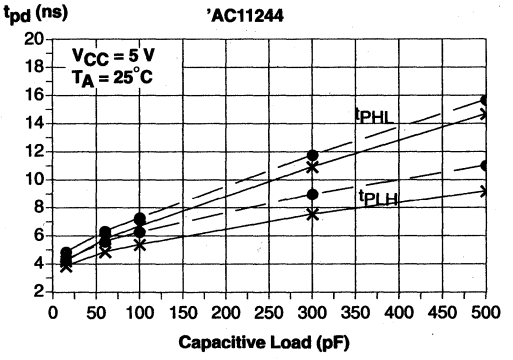
As pointed out above, any of the SSOPs can be utilized as buffers in high-density memory arrays. In many instances, series-dampening termination is chosen, due to its ease of implementation and power savings. Numerous logic devices are available that incorporate the series-dampening resistor on chip, as in the BCT2XXX series of products, simplifying this type of termination. When these parts are packaged in the 20-pin SSOP, as in the 'BCT2240DB, a tremendous board real estate savings is realized over a discrete approach using external resisters and SOIC devices. For PCMCIA cards the driver must also offer low-power consumption, necessary for battery operation. The 'AC11244PW (TSOP package) can be used in these applications due to its low static power CMOS characteristics.

Many times when an output switches a large memory array the capacitive load is localized in close proximity to the driver and can be treated as a simple lumped load. In these instances it is useful to know how the propagation delay (t_{pd}) of the driver changes with the additional capacitive load. The change in the driver's t_{pd} is due to the interaction of its source impedance, R_{on}, with the capacitive load, C_l. Figures 8, 9, and 10 show this phenomena for the 'AC11244, 'BCT2240, 'ABT16244, and 'ABT32245 for both single and multiple outputs switching.



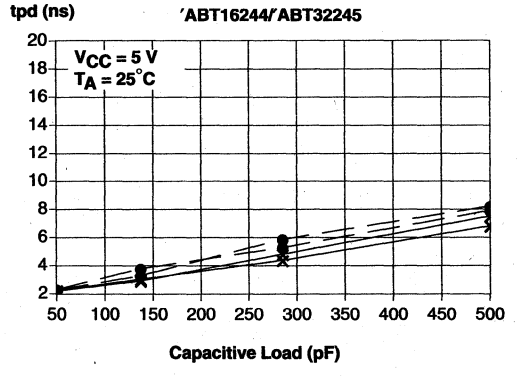
Solid = Single Output Switching
Dashed = Eight Outputs Switching

Figure 8. Typical t_{pd} vs Capacitive Load



Solid = Single Output Switching
Dashed = All Outputs Switching

Figure 9. Typical t_{pd} vs Capacitive Load



Solid = Single Output Switching
Dashed = All Outputs Switching

Figure 10. Typical t_{pd} vs Capacitive Load

These three figures illustrate the effect that the output impedance of the driver has over t_{pd} degradation. Figure 8 shows that even though the 'AC11244 has symmetrical high and low output drive current ratings of 24 mA, t_{PHL} show more degradation versus capacitive loading due to the graded turn-on of the output to minimize simultaneous switching noise [ground bounce]. Many advanced CMOS logic devices utilize this graded turn-on, but not without the penalty of slower propagation delays at higher capacitive loads. Figure 7 shows a similar asymmetrical t_{PHL} performance, but now it is due to the inclusion of a 33-Ω series output resistor. Contrasting the previous two graphs is Figure 10 which highlights the high-drive capability of the ABT16XXX and ABT32XXX devices, along with the symmetrical t_{pd} performance that the –32/64 mA outputs deliver.

Bus-Interface Usages for the SSOP

The gains made by utilizing devices with faster propagation delays can be lost if the propagation delay degrades when multiple outputs on a package are switched simultaneously. This effect is greatly reduced when a device is packaged in the 48/56-pin SSOP, because this package allows the signal-to-ground ratio of a standard 8-bit function to be improved from 8:1 to 2:1, and the signal-to-V_{CC} ratio improves from 8:1 to 4:1. This multiple power pin system translates into a quieter on-chip power system when multiple outputs switch, resulting in less propagation delay degradation compared to a standard 8-bit function. The same can be said of the 100-pin SQFP and cavity SQFP which utilizes a 3:1 signal-to-ground ratio. Figure 11 compares the change in t_{pd} vs number of outputs switching (in phase) of a typical '244, buffer-type function when packaged in a 48-pin SSOP and 100-pin SQFP to the performance in a 20-pin DIP and SOIC.

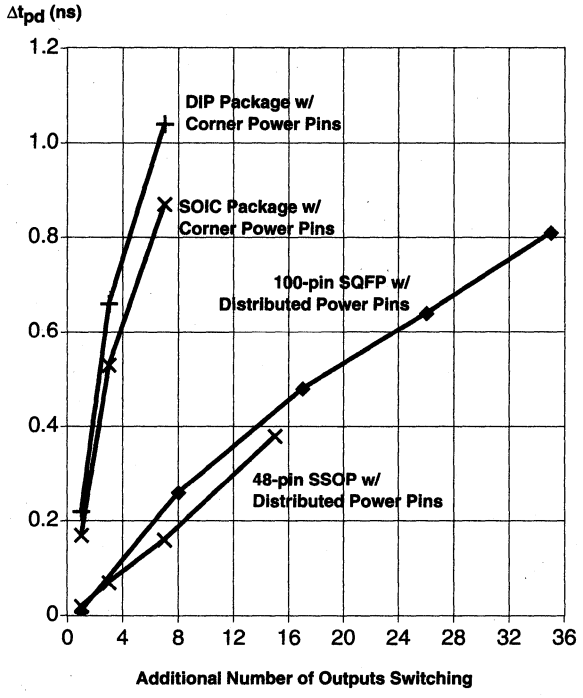


Figure 11. Typical Δt_{pd} vs Outputs Switching

Conclusion

The various fine pitch surface-mount packages give the designer a wide range of solutions to today's system area and volume constraints. The high pin count SSOP and SQFP packages allow bus-interface devices to track the trend of wider data bus widths, while providing superior electrical performance when compared to the standard end-pin product. The cavity SQFP allows for higher power dissipation applications, allowing the interface device to operate at higher frequencies. The low pin count SSOPs occupy less volume than other surface mount devices, facilitating their use in height critical applications.

For Further Information

Transmission Lines

Advanced Schottky Family Applications, Texas Instruments Advanced Schottky Data Book, 1986
Advanced CMOS Logic Designer's Handbook, Texas Instruments, 1988

Power Dissipation

SSOP Designer's Handbook, Texas Instruments, 1991

ABT Enables Optimal System Design

Steve Perna
Advanced System Logic – Semiconductor Group
Texas Instruments Incorporated

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ABT ENABLES OPTIMAL SYSTEM DESIGN

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As the operating frequencies of microprocessors increase, the period of time allotted for memory access, arithmetic computation or similar operation decreases. With this in mind, a new series of Advanced Bus Interface Logic (ABIL) products developed with Texas Instruments' sub-micron Advanced BiCMOS (ABT) process technology assume a prominent role as the key high performance logic needed in today's workstation, personal and portable computer, and telecom systems. The goal of this family of products is to provide system designers a bus interface solution combining high drive capability, low power consumption, signal integrity and propagation delays fast enough to appear transparent with respect to overall system performance. Fine pitch package options simplify layout, reduce required board space and decrease overall system costs. Novel circuit design techniques add value over competitive solutions.

TRENDS IMPORTANT FOR TODAY'S SYSTEM DESIGNER

Modern system designers face many complex challenges in meeting their design goals. The trends toward (need for) faster cycle times, lower power consumption, smaller footprints, greater reliability and lower total system cost combine to put ever increasing pressure on today's system designer.

The need for faster cycle time has traditionally been addressed by the microprocessor manufacturer. Clock and microprocessor frequencies have increased steadily with each succeeding product generation. The most advanced RISC processors in development are touting frequencies in the area of 200 MHz. For production systems it is not unusual for processors to run on the order of 50 MHz and above. Increasing clock and microprocessor frequencies are now beginning to put pressure on surrounding memory and logic to make greater contributions in reducing overall system cycle times and improving overall system performance.

Higher performance systems require the designer to focus on total system power requirements. Faster systems traditionally require more power which often means more costly solutions. Power costs money to supply and heat buildup due to this power costs money to remove. Also, excess power consumption adversely affects reliability due to the increase in the junction temperature of the silicon components. Lower power devices reduce requirements for larger power supplies and high cost cooling techniques, and could lead to smaller system packaging.

Occurring in parallel with demands for increased system performance and reduced system power consumption is demand to house systems in smaller cases, boxes, chassis and cabinets. This miniaturization requires that each system component be optimally laid out in silicon, packaged and mounted on the PCB board.

Speed, power, size, cost and reliability are all parameters by which system and end

equipment success are measured. Semiconductor manufacturers must be sensitive to these parameters and be able to provide well-defined and designed products to meet these needs.

ADVANCED BUS INTERFACE LOGIC (ABIL) AS THE SYSTEM BUS INTERFACE

Semiconductor vendors are required by system design houses to provide new products which are faster, consume less power, exist in smaller packages and present a lower relative cost than their predecessors. Since the early 1970s many different logic product technologies have attempted to meet these demands.

Early logic product technologies often forced the system designer to make tradeoffs. As Figure 1 details, speed and power were the most typical design goals traded off. Solutions such as Schottky or HCMOS respectively offered high speed at the expense of low power or low power at the expense of high speed. In a typical system application this logic sat between only a few system blocks such as a simple 8 MHz processor, a slow 256K DRAM, and a local TTL bus. Their functional role was little more than small-scale integration (SSI) or medium-scale integration (MSI). Despite these shortcomings, early logic technologies thrived because they were cheap and readily available.

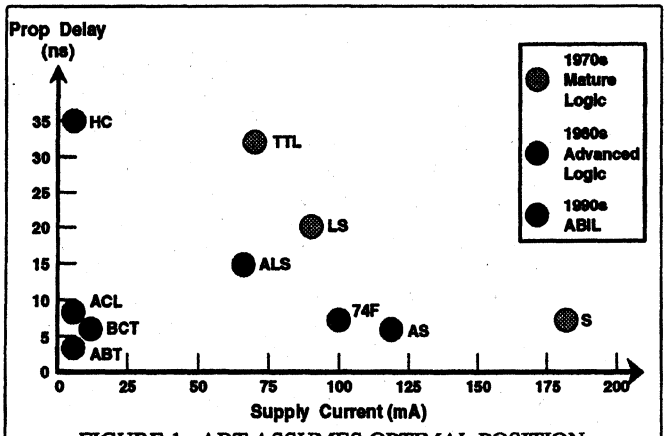


FIGURE 1. ABT ASSUMES OPTIMAL POSITION

The cycle time requirements for interface logic vary as a function of microprocessor and clock speed. In an 8 MHz system, the total system cycle available for completion of all operations is 250 nanoseconds. This can be roughly budgeted into 160 nanoseconds for the memory access, 45 nanoseconds for processor set-up and 45 nanoseconds for the interface logic (including signal propagation across printed circuit board traces). With 45 nanoseconds available for interface, a forgiving, low-performance technology such as Low-power Schottky or HCMOS can be utilized.

The situation changes dramatically when system speeds increase to 45 or 50 MHz. At 45 MHz only 44 nanoseconds of total cycle time is available to complete all operations. Now, more expensive memories are needed with access times down in the 20 nanosecond range. Microprocessor set-ups can only be 8 nanoseconds. This leaves only 16 nanoseconds for interface and signal trace propagation delay. The interface cycle time is a much higher percentage of the total system cycle time at 45 MHz than at 8 MHz.

As cycle time requirements shrink, each nanosecond becomes critical in meeting the total system 'budget'. The system designer has the option of using higher performance memories, processors or interface logic in squeezing additional nanoseconds out of the system delay. There is great demand for in using interface logic to meet these budget needs because it is typically much less expensive for the designer to use than higher performance memories or processors.

In light of decreasing total system cycle time requirements, the early logic technologies gave way to faster technologies. Significant gains made since the Schottky and HCMOS days result in products which no longer force the system designer into a tradeoff box. New product development in the area of complex memories, processors and ASIC's has led the way for an equal, if not greater, acceleration in new product development for advanced digital logic products.

This development has propelled logic up from the ranks of "glue" status, used to fill in design gaps around the other major system blocks, to its new position as the system "bus interface". Advanced Bus Interface Logic (ABIL) products are now responsible for controlling the signals between the backplane busses and the other major system design blocks. They have become a major system design block in their own right exerting significant influence over the performance of the final design.

In a modern-day system ABIL products are likely to connect many major system design blocks including application specific parallel processors, 4M DRAM's, fast cache SRAM's and complex ASIC gate arrays/standard cells. The task of this new breed of advanced logic is to effectively transceive the address, data and control signals of these IC elements to and from heavily loaded TTL/CMOS/BTL system backplanes.

A wide variety of industry standard and proprietary backplane specs add to the difficulty of the task. At the low-end of the scale, exhibiting data transfer rates in the range of 10-20 MByte/sec, are the PC AT and EISA type busses. For mid-range server and graphics workstation applications, the 50-100 MByte/sec data transfer rate range of Multibus II and Microchannel type busses is typical. High-end server and mainframe computer applications require the greater than 100 MByte/sec data transfer rates of Futurebus + type busses. Transceivers connecting to each of these backplanes need to provide very high drive current capability to effectively and reliably migrate signals across. ABIL products from Texas Instruments uniquely address this need.

ENABLERS TO CONTINUOUS NEW PRODUCT DEVELOPMENT

Reduction in minimum process dimension, enhanced value-added circuit design techniques, utilization of fine-pitch packaging and incorporation of lower power supply voltages are the most important enablers to continuous new development for logic products.

The minimum process dimension represents the width of the transistor gate region and gives an indication of the switching speed of the transistor. In general, the smaller the minimum process dimension the faster the transistors will switch. An added advantage of reducing the minimum process dimension is the gain in gate density which can be achieved. A gain in gate density results in increased device functionality without a corresponding increase in silicon die area. Currently state-of-the-art high volume production logic processes consider a 0.8 micron minimum process dimension. However, work is ongoing to prototype more advanced processes characterized by 0.6, 0.5 and 0.35 micron minimum process dimensions.

Enhanced value-added circuit design techniques act to greatly increase the functionality of a logic device as well as improving its performance. These techniques often eliminate the need for the designer to utilize discrete components such as resistors, capacitors and diodes because these are built into the silicon device itself. Additionally optimizations in I/O or core circuitry can positively effect speed and power performance.

An aggressive drive exists to convert classic through-hole package approaches to totally above board surface mount approaches. Occurring in parallel is a drive to upgrade existing surface mount packages with finer pin-to-pin pitches so as to minimize total package area. With smaller packages come increased reliance on thermal management techniques however. The increased difficulty in removing heat from the smaller packages may preclude the use inexpensive plastic

packages. The necessity to use ceramic or other alternatives would act to drive design costs up.

Finally, system designers are beginning to drive the semiconductor industry to move below 5 Volts as the baseline for power supply of operation. The migration to lower voltages such as 3.3 Volts enhances the reliability of advanced process technologies exhibiting minimum process dimensions of 0.6microns or lower. The need for low voltage memory and processor product interface, lower device generated noise levels, lower power consumption and increased battery life for unregulated portable systems accelerate the demand for 3.3 Volt logic. New 3.3 Volt logic opportunities will emerge as system designers continue to rely on advanced process technologies.

WHAT IS ADVANCED BICMOS (ABT) ?

Advanced BiCMOS (ABT) is a product technology available today from Texas Instruments to aid designers doing high performance bus management. It is currently available in many different product options including 8-bit octal, 16/18/20-bit Widebus and 32/36-bit Widebus + versions.

At TI ABT evolved from an earlier 1.5 micron BiCMOS process. It was designed to provide speeds equivalent to existing advanced bipolar solutions but with 90% less device power. This standard BiCMOS introduced high performance, lower power bus interface products to the marketplace two years ahead of the nearest competitor. Since its bus interface introduction in 1987, TI has utilized BiCMOS and Advanced BiCMOS in products such as mixed-signal integrated circuits, high performance gate arrays, high speed cache tags, and application specific processors like the SuperSPARC.

ABT employs a sub-micron 0.8 minimum process dimension. It combines elements of both bipolar and CMOS circuit/process technologies onto a single silicon chip. ABT offers the system designer the best combination of high speed, high drive and low power consumption in the industry. As shown in Figure 1, ABT provides a performance point closer to the origin of the speed/power graph than any other logic technology available. Specifically ABT is based on a CMOS core circuit structure with an NPN bipolar output transistor module added. This means adding about four additional masks to the CMOS process. The current single NPN transistor output structure of ABT has been optimized for 5 Volt operation.

Simplified input and output stages of an ABT transceiver are shown in Figure 2. The inputs are designed to offer TTL compatible levels with guaranteed switching between a Vih min of 2.0 Volts and a Vil max of 0.8Volts. Since these inputs are implemented with CMOS circuitry they offer characteristic high impedance for low leakage and low capacitance for minimal bus loading. The CMOS supply voltage of the input stage is dropped by diode D1 and transistor Q1, centering the threshold around 1.5 Volts. When inputs are in the LOW state, Qr raises the voltage of source Qp up to the rail ensuring proper

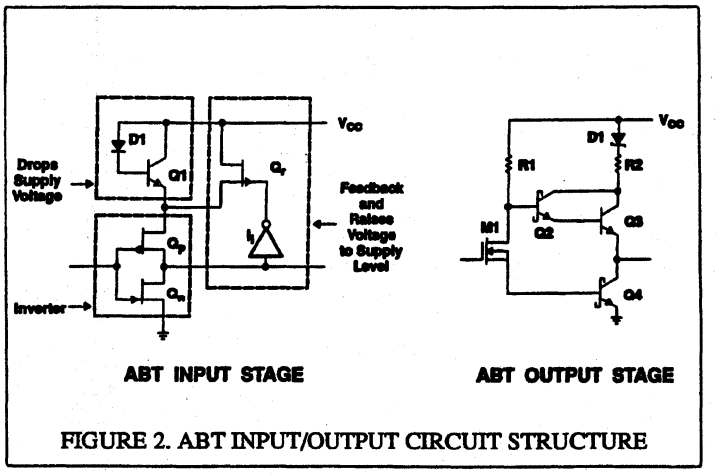


FIGURE 2. ABT INPUT/OUTPUT CIRCUIT STRUCTURE

operation of the feedback stage. This stage provides about 100 mV of input hysteresis increasing noise margins and reducing oscillations.

ABT outputs utilize bipolar circuitry to provide the high speed and drive necessary for bus interface. A major advantage for using bipolar circuitry in the output stage is the reduced voltage swing which lowers ground noise, improves signal integrity and reduces dynamic power consumption. In the figure M1 acts as a current switch which drives the output LOW when conducting current from R1 through to the base of Q4. The base of Q2 is pulled LOW turning off the upper output. For a LOW to HIGH output transition, M1 turns off and current through R1 charges the base of Q2. As Q2 goes high, the Darlington pair Q2 and Q3 turns on. With its supply of base current now cut off, Q4 turns off and the output transition switches LOW to HIGH. R2 limits output current in the HIGH state and D1 is a blocking diode preventing current flow in power-down applications.

By virtue of its small minimum process geometry, tight metal pitch and shallow junctions, ABT can provide for strong output drive currents (sink currents speced at 64 milliamps and source currents speced at 32 milliamps) and low parasitic capacitances. As a result of these enhancements, internal propagation delays are very fast and very well behaved. Figure 3 shows that typical prop delays are on the order of 2-3 nanoseconds across temperature. This excellent consistency allows ABT to be specified over the industrial temperature range of -40 to +85 degrees Celsius. The figure also shows that ABT performance is very well behaved across capacitive load and multiple output switching conditions.

Maximum prop delays for ABT are as low as 4-5 nanoseconds depending on the device type and propagation path. Figure 4 compares the datasheet maximums of several ABT 16-bit Widebus transceiver devices with competing FCTB/C CMOS and 74F/ALS bipolar solutions. It is clear from both Figure 3 and Figure 4 that ABT is the system designer's best choice for bus interface applications which require consistent speed performance over many different conditions.

Registered Transceiver with ClkEN	ABT16952	29FCT52C	F2952
t_{pd} CLK to A/B	4.5 ns	6.3 ns	9.0 ns
$t_{pd(en)}$ OE to A/B	6.0 ns	7.0 ns	10.0 ns
$t_{pd(dis)}$ OE to A/B	5.5 ns	6.5 ns	9.0 ns
Transceiver with Parity	**ABT16657**	**ABT657**	**F657**
t_{pd} A to B	4.3 ns	5.5 ns	8.0 ns
t_{pd} A to Parity	6.7 ns	11.3 ns	16.0 ns
t_{pd} B to ERROR	6.7 ns	15.7 ns	22.5 ns
Registered Parity Transceiver	**ABT16833**	**FCT833B**	**ALS29833**
t_{pd} A to B	4.3 ns	7.0 ns	10.0 ns
t_{pd} A to Parity	6.7 ns	10.5 ns	15.0 ns
t_{pd} CLK to ERRO	4.6 ns	15.0 ns	16.0 ns

FIGURE 4. ABT IS THE SPEED BENCHMARK

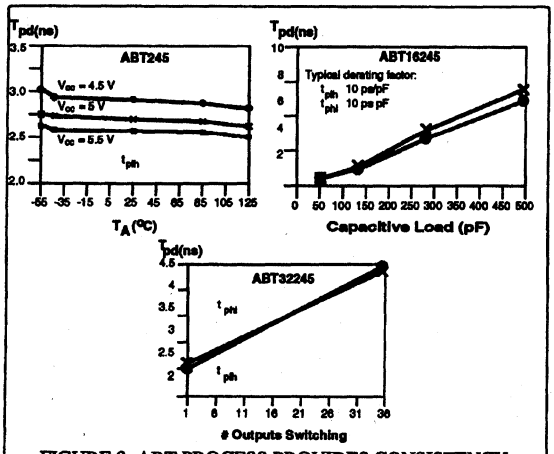


FIGURE 3. ABT PROCESS PROVIDES CONSISTENCY

From a power (current) consumption standpoint the use of bipolar in the output stage is advantageous for two reasons. First the voltage swing is less than that of a CMOS output. The power consumed when charging or discharging internal circuit capacitances and the external load capacitance is reduced. Second the bipolar transistors are capable of turning off more efficiently than CMOS transistors. The wasteful flow of current from Vcc to GND is reduced. Although bipolar does tend to have a high static power consumption, its lower dynamic power consumption allows for better overall power performance at high frequencies than either pure bipolar or

CMOS. This is because the dynamic power component makes up the majority of a device's overall power consumption.

The ABT maximum high impedance supply currents (Iccz) range from about 50 microamps for 8-bit octals to about 2-3 milliamps for 16-bit Widebus products. Maximum dynamic supply currents (Iccl) range from about 30milliamps for 8-bit octals to about 34 milliamps for 16-bit Widebus products. Power-on-demand, an enhanced circuit design improvement to the bipolar output stage on new ABT product families, reduces dynamic current consumption levels by up to 50%. High impedance and dynamic supply current goals for the new 32/36-bit Widebus + family are 500 microamps and 60 milliamps respectively.

Bus Hold, shown in Figure 5, is another example of an enhanced, value-added circuit design technique available on new ABT product families. The Bus Hold cell provides for a small holding current of 100 microamps to be delivered to I/O pins configured as inputs left unused or floating. This current latches the last known input state to a valid logic level. Floating input conditions are common to CMOS backplanes or device bus interface situations where driving entities are periodically required to be in 3-state. Bus Hold cells eliminate passive pull-up (to Vcc) or pull-down (to GND) termination resistors necessary to prevent application problems or oscillations. External provision for these resistors by the system designer consumes board area, increases bus capacitance, contributes to bus loading and lowers system performance. The Bus Hold feature is particularly effective when offered on products with a lot of I/O capability such as 32/36-bit Widebus + devices.

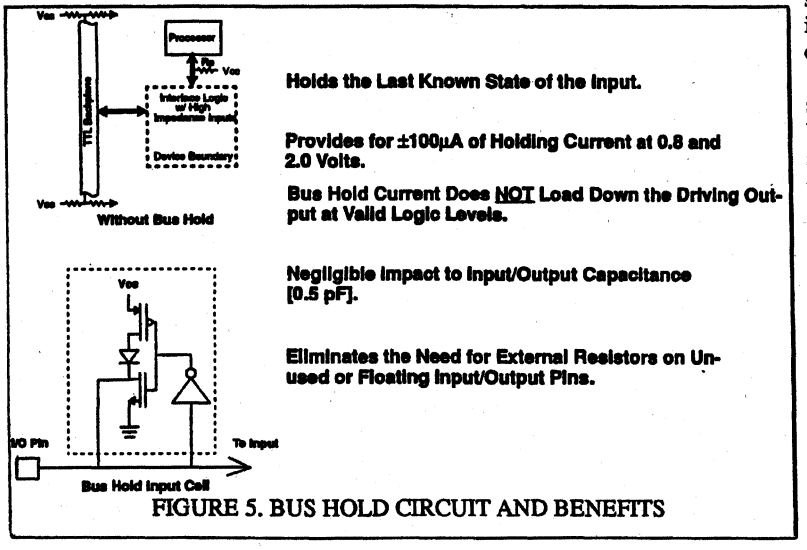


FIGURE 5. BUS HOLD CIRCUIT AND BENEFITS

FINE-PITCH PACKAGING SHRINKS ABT DEVICE SIZE

As the push for smaller system sizes becomes intense, the system designer will require the logic manufacturer to house high performance silicon in increasingly space conscious packages. Most notably the system designer has been leveraging the advantages of plastic leaded chip carriers (PLCC's) and small outline integrated circuits (SOIC's).

Both PLCC and SOIC packages provide a gull wing lead profile. Both utilize a 1.27 millimeter pin-to-pin pitch spacing. The reduced pitch offers a huge space improvement over bulky plastic dual-in-line (PDIP) through-hole packages. The major difference between PLCC and SOIC is philosophical. The PLCC has pins on all four sides (arranged either in square or rectangular configuration) while the SOIC has pins on only two sides (arranged in flow through configuration).

In spite of the advantages of PLCC and SOIC, system designers are beginning to specify surface mount packages with finer pitch values to keep their end equipments competitive in the marketplace or to avoid falling behind more aggressive rivals. Such fine pitch versions available in volume today offer improvements in the pin-to-pin pitch down to 0.635 millimeters. More advanced fine pitch alternatives exhibiting characteristic pitches of 0.5, 0.4 and 0.3 millimeters are on the horizon.

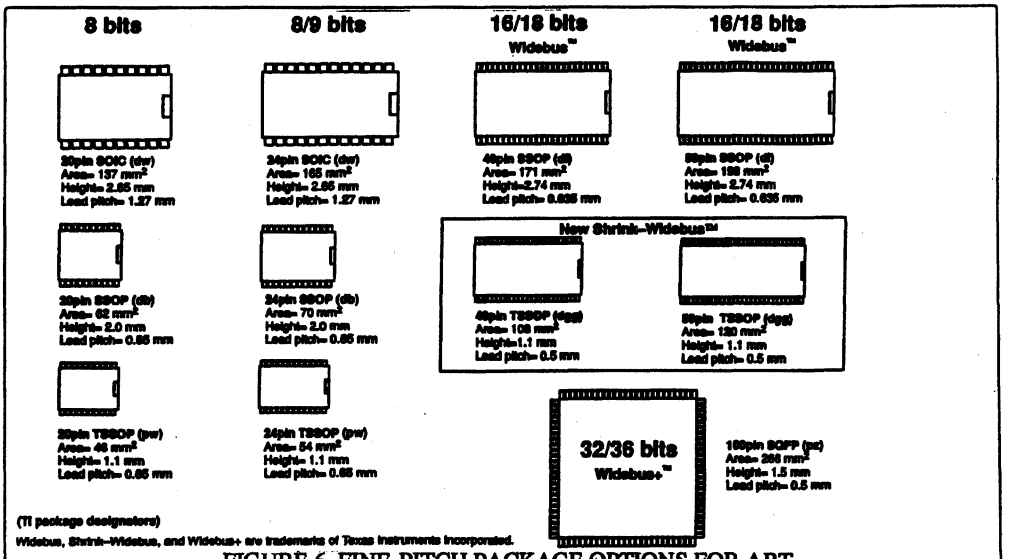


FIGURE 6. FINE-PITCH PACKAGE OPTIONS FOR ABT

The plastic quad flat pack (PQFP) is a fine-pitch version of the PLCC package. It offers a 0.635 millimeter pitch and is widely used for microprocessors, ASIC's or other custom devices. The 44-pin PQFP is the smallest used in volume while the largest versions provide over 200 pin capability. For the system designer using ABIL products however, it is advantageous to combine the fine-pitch capability of the PQFP with the two-sided dual-in-line design of the SOIC.

SOIC's have evolved in two distinct paths to meet this need. The first path considers reducing the surface area and pin pitch of the package while keeping the pin count and bit density constant. The second path considers increasing the bit density of the package by increasing pin count and reducing pin pitch. Figure 6 clearly shows both of these migratory paths starting from the standard octal SOIC package in the upper left hand corner.

Package size reductions are shown vertically down the figure with each succeeding reduction occupying a new row at constant bit density and pin count. Bit density and pin count increases are shown horizontally across the figure.

There are five new fine-pitch packages represented in the figure. Four of these offer a density upgrade path for the SOIC. The fifth is a new package offering a density upgrade for the PQFP. All of these packages were developed and standardized exclusively for high performance ABIL ABT products by TI.

The Shrink Small Outline Package (SSOP) is available in two worldwide standard form factors. The first, approved by the Joint Electron Device Engineering Council (JEDEC), allows for 16-, 18-, or 20-bit I/O functions in a

package roughly the same size as the octal SOIC. The pin pitch for the JEDEC SSOP is 0.635 millimeters. The JEDEC SSOP is available in a 48-pin version for basic 16-bit driver and transceiver functions and in a 56-pin version for complex 16- to 20-bit transceiver functions. The very popular ABT Widebus family uses the JEDEC approved SSOP.

The second form factor, approved by the Electronics Industry Association of Japan (EIAJ), allows for 8- and 9-bit I/O functions in a package about 40%of the size of the octal SOIC. The pin pitch for the EIAJ SSOP is 0.65 millimeters. The EIAJ SSOP is available in a 20-pin version for basic ABT 8-bit driver and transceiver functions and in a 24-pin version for complex ABT 8- and 9-bit transceiver functions.

Bottom row of figure 6 represents the third form factor upgrade to the SOIC available from TI. The Thin Shrink Small Outline Package (TSSOP) is EIAJ approved and offers a reduced thickness (height) spec of 1.1 millimeters. The pin pitch of the EIAJ TSOP is 0.65 millimeters. (The body width is 4.4 millimeters). The TSSOP is compatible to Type I and Type II card physical requirements of the Personal Computer Memory Card International Association (PCMCIA). TSSOP offers the smallest package size available for 20-and 24-pin drivers and transceivers. For denser memory arrays TSSOP facilitates front and back side mount in under 3.3 millimeter thickness specified by PCMCIA if card thicknesses are kept under 1.0millimeters.

For wideword applications with extreme space and height restrictions, TI will offer Widebus devices in a new package called the Shrink Widebus (TM). Available in 48- and 56-pin versions, this new package has a 1.1 millimeter maximum height, a 6.1 millimeter body width and a 0.5 millimeter lead-pitch. The Shrink Widebus package, developed by TI, is registered with the EIAJ, meets the requirements of the PCMCIA and consumes 40 percent less board area than the standard JEDEC SSOP.

Providing the density upgrade path for the PQFP is the EIAJ Shrink Quad Flat Pack (SQFP). This 100-pin package allows single chip 32- and 36-bit I/O solutions in over 50% less area than with octal SOIC connections. The pin pitch for the EIAJ SQFP is 0.5 millimeters which is the smallest in production today. The reduced pitch of the SQFP offers a 35% area reduction over 100-pin PQFP solutions. The new 32- and 36-bit ABT Widebus + family, recently announced at the BUSCON '92 WEST trade show in Long Beach, California, uses the 100-pin SQFP.

All the above fine-pitch package options are superior for space saving applications. The JEDEC SSOP and EIAJ SQFP are superior in several other areas as well. The JEDEC SSOP incorporates a flow-through architecture where input and output pins each have their own dedicated side of the package. Flow through pinouts offer the system designer a very easy route path for signal traces.

A standard SOIC octal package can only afford 1 GND pin for every 8 I/O's. This ratio improves to 2:1 and 3:1 for JEDEC SSOP and EIAJ SQFP respectively. Both the JEDEC SSOP and the EIAJ SQFP provide multiple Vcc and GND pins distributed along the sides. The improved GND number and distribution of these pinouts is very forgiving from a noise generation standpoint and allows for less propagation delay than octal functions. As a result, ABT octals, ABT Widebus and ABT Widebus + all exhibit less than 1 Volt of noise typically, even though the maximum number of switched outputs increases from 8- to 18- to 36-bits with each respective family.

As package area decreases, the thermal impedance of the package to the ambient environment increases. Thermal impedance represents the ability of a package to dissipate heat. The higher the thermal impedance the more difficulty the package has in dissipating heat. The higher thermal impedances of fine-pitch packages require additional attention and care from the system designer. Proper thermal management techniques as well as proper power dissipation guidelines must be used to ensure operation. Fortunately the low power of ABT ABIL products

NAME	EXAMPLE PART NO.	KEY FEATURES	NUMBER OF BITS	PACKAGES	MAX PROP DELAY (ns)	I_{CCZ} (mA)	I_{OL} (mA)	I_{OH} (mA)	TARGET APPLICATIONS
ABT	SN74ABT245	0.8 micron process, -40/85°C temperature	8, 9, 10	DIP/SOIC/ SSOP (EIA-J)	4.8	0.05	64	32	High-speed bus interface, PC, EWS, Telecom
ABT Widebus	SN74ABT16245	Flow-through pinouts, low noise	16, 18, 20	SSOP (JEDEC)	4.1	2	64	32	Higher performance, space conscious applications
ABT Widebus+	SN74ABT32245	Bus hold cell, power-on-demand	32, 36	SQFP (EIAJ)	4.9	0.5	64	32	Single chip 32-bit interface
IWS Drivers	SN74ABT25245	Enhanced output drivers	8	DIP/SOIC	4.5	0.1	188	96	25 Ω incident wave switching
Memory Drivers	SN74ABT2245	Series output dampening resistors	8, 10, 11, 12, 16, 18, 32, 36	DIP/SOIC/ SSOP (EIAJ)/ SSOP(JEDEC)/ SQFP (EIAJ)	5.0 - 5.5	0.05 - 0.5	12	12	Low noise, high reliability driving, memory interface
Futurebus+	SN74FB2031	BTL port, 2 ns minimum edge rate	8, 9, 18	PQFP/ SSOP (JEDEC) SQFP (EIAJ)	5.5	10	100	3	I.E.E.E. 896.1 backplane interface
BTL Drivers	SN74FB2033	BTL-TTL level translation	8, 9	PQFP/ SSOP (JEDEC)	5.5	10	100	3	I.E.E.E. 1194.1 backplane interface
Scope	SN74ABT8245	Testability, built-in self test	8, 16, 18	DIP/SOIC/ SSOP (EIAJ)/ SSOP (JEDEC)/ SQFP (EIAJ)	4.7	0.05	64	32	I.E.E.E. 1149.1 backplane interface
LVT	SN74LVT245	3.3 V V_{CC}, mixed mode, bus hold	8	SOIC/TSOP	6.0	0.2	64	32	Battery portables, notebook computers, POS terminals
LVT Widebus	SN74LVT16245	3.3 V V_{CC}, mixed mode, bus hold, power-on-demand	16, 18	SSOP (JEDEC)	5.5	0.1	64	32	Workstations, portable computers

FIGURE 7. ABT PRODUCT AND FEATURE TABLE

is more conducive to a fine-pitch packaging approach than competitive CMOS solutions.

ABT PRODUCTS PROVIDE END EQUIPMENT SPECIFIC SOLUTIONS

Combining previously discussed state-of-the-art elements of the ABT process with its numerous advanced fine-pitch package options and its enhanced circuit design features yields a very impressive portfolio of new products. These new products emerge to eloquently serve distinct needs of the workstation, personal and portable computer, and telecom end equipment markets.

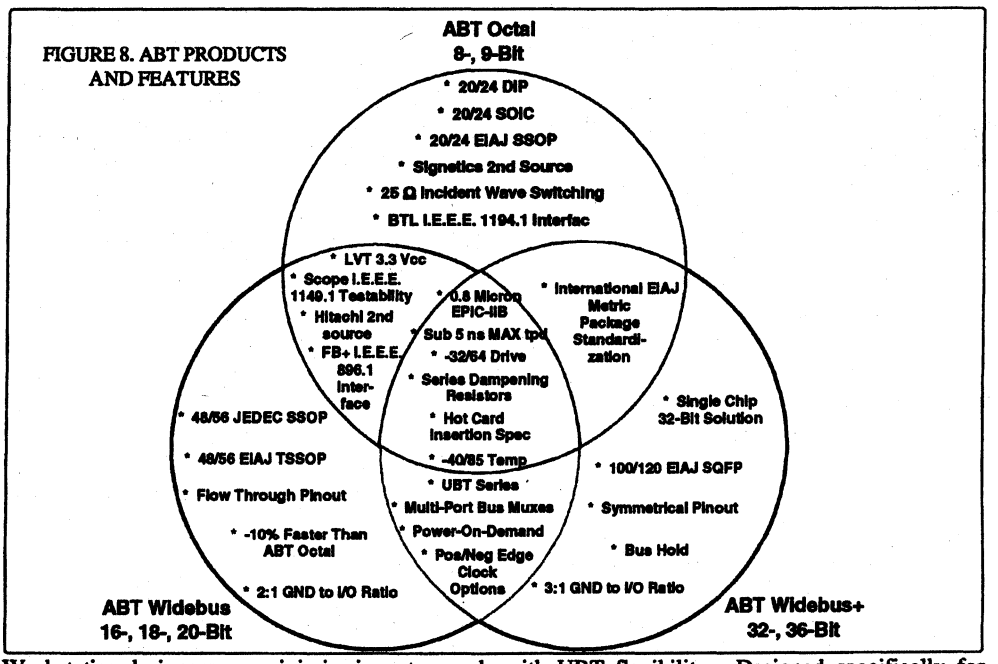
Figure 7 categorizes the entire ABIL product spectrum built with the ABT process technology. These families offer features and benefits dedicated to specific markets and industry standards. Figure 8 (next page) organizes these features and benefits graphically.

For high performance engineering workstation and server markets, the ABT Widebus and ABT Widebus + families provide the highest integration and performance. They are necessary to connect the most demanding CISC/RISC microprocessors to the most heavily loaded, high frequency backplanes.

The Universal Bus Transceiver (UBT) is unique in the industry because it can be operated in several distinct bus interface modes. Each package contains D-type latches and D-type flip-flops. Flexible control logic options provide for output enable, latch enable, clock and clock enable combinations.

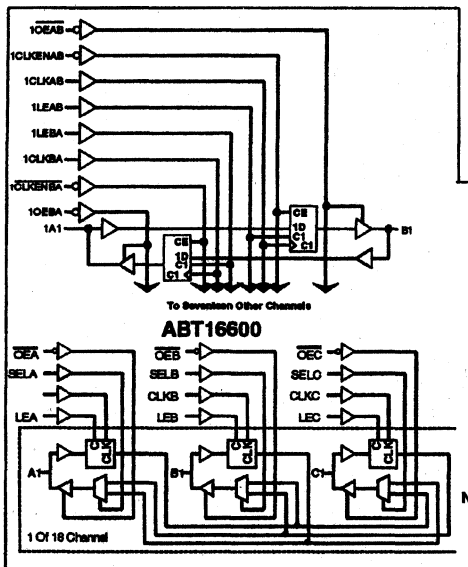
UBT's can be configured as transparent data flow through transceivers (like the dedicated '245 function), latch enabled transceivers (like the dedicated '543 function), clocked registered transceivers (like the dedicated '646 function) and clock enabled registered transceivers (like the dedicated '952 function).

FIGURE 8. ABT PRODUCTS AND FEATURES



Workstation designers can minimize inventory and procurement requirements, costs and overhead with UBT flexibility. Designed specifically for workstation bus interface applications, the UBT is perfect as an interface to the many different microprocessor architectures and system backplane specs available.

Figure 9 details the current UBT portfolio from TI and includes block diagrams for 2 devices



SERIES	# OF BITS	# OF PORTS	PACK-AGE	# OF PINS	PARTI-TIONING	PARITY GEN/CH	CONTROL LOGIC OE	LE	CLK	CLKEN
16500	18	2	SSOP	56	x 18	No	Yes	Yes	Yes	No
16600	18	2	SSOP	56	x 18	No	Yes	Yes	Yes	Yes
32316	16	3	SQFP	80	x 16	No	Yes	Yes	Yes	Yes
32318	18	3	SQFP	80	x 18	No	Yes	Yes	Yes	No
32500	36	2	SQFP	100	x 18	No	Yes	Yes	Yes	No
32600	36	2	SQFP	100	x 18	No	Yes	Yes	Yes	Yes
32700	36	2	SQFP	120	x 9	No	Yes	Yes	Yes	Yes
32900	36	2	SQFP	120	x 9	Yes	Yes	Yes	Yes	Yes

Note: Positive and negative edge triggered clock, and series output dampening resistor options available for each version in the table

FIGURE 9. UNIVERSAL BUS TRANSCIEVER PORTFOLIO

in the series. The ABT16600 is an 18-bit UBT packaged in the 56-pin SSOP package. It can be configured in each of 4 different data flow modes between its A-port and B-port.

The ABT32318 is an 18-bit muxed UBT which can be configured in each of 3 different data flow modes between its A-port, B-port and C-port. This UBT allows the system designer multiple combinations for real-time and stored data exchanges between the three ports. It is particularly useful for multi-bus communication, multi-way interleaving memory applications and high performance multiplexed address and data bus interface.

The ABT32901 (not pictured) is a 36-bit UBT which provides the most flexibility to the designer packaged in a 120-pin SQFP. The devices can be configured in transparent, latched, clocked or clock enabled data flow modes and has additional benefits of parity generate and check as well as byte (x9) enable. The 120-pin SQFP offers the same 14 x 14 millimeter body sizes as the 100-pin SQFP, but with a 0.4 millimeter leadpitch.

Several ABT product families directly address upper end workstation and server equipment. A series of transceivers compliant to the I.E.E.E. 896.1 Futurebus + backplane interface standard are available. The special Futurebus + protocols dictate special electrical requirements of the transceivers in order to ensure proper connection to Futurebus + backplanes. Each of 7 transceivers in the series utilize backplane transceiver logic (BTL) switching levels in accordance with the Futurebus + standard. Complementing these Futurebus + transceivers are a series of BTL transceivers compliant with the I.E.E.E. 1194.1 standard. Both transceiver series contain a TTL A-port along with the BTL B-port and can perform TTL-to-BTL and BTL-to-TTL level translation.

Scope transceivers and drivers are available in ABT which are compliant with the I.E.E.E. 1149.1 testability standard. For high reliability and fault-tolerant system needs these devices provide their own internal self-test capabilities. A complete line of Scope hardware and software system products have been developed by TI.

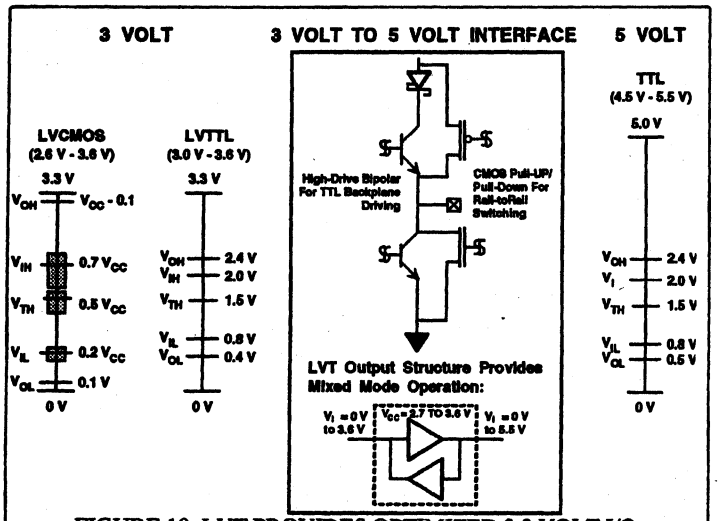


FIGURE 10. LVT PROVIDES OPTIMIZED 3.3 VOLT I/O

The personal computer market is characterized by very short design cycle times and intense pressure to lower costs. The major driving force is to put workstation-type performance in machines designed for desktop, home and portable applications. ABT in fine-pitch package options meets these needs nicely.

A new series of low voltage products definitively addresses the needs of the portable sub-segment of this market. The Low Voltage Technology (LVT) family has been developed

with the sub-micron ABT process and will be available in both 8-bit octal and 16/18-bit Widebus density versions. Supply voltage for LVT is specified from 2.7 Volts to 3.6 Volts. LVT 8-bit product uses the TSOP to facilitate the smallest area for portable applications. LVT Widebus product uses both the JEDEC SSOP and the 48/56-pin EIAJ Shrink Widebus SSOP.

Market requirements for 3.3 Volt logic products are being driven now by battery laptops and hand-held instruments. Higher performance desktop PC's and workstations could lag a year behind portables in their demand for 3.3Volt logic.

As shown in Figure 10, the 5 Volt ABT I/O structure has been optimized for use with 3.3 Volt supply currents. LVT 3.3 Volt speed performance is equivalent to ABT 5 Volt speed performance. This special I/O circuitry also allows for a "mixed-mode" 3.3 Volt to 5 Volt interface capability. Designers can use the same LVT logic for core 3.3 Volt system partition as for external 5 Volt backplane interface. This is particularly important as other system elements (microprocessors, ASIC's, memories) migrate to 3.3 Volts at different rates.

LVT I/O circuitry provides multiple output current ratings for multiple system requirements. LVT devices are specified to drive at rail-to-rail low voltage CMOS levels and standard 5 Volt TTL levels. LVT employs Bus Hold and Power-on-demand circuits increasing reliability, decreasing discrete component count and minimizing enabled and disabled static power consumption. Maximum Iccl, Icch, and Iccz current specs are 5, 0.1 and 0.1 milliamps respectively.

The majority of classic telecom end equipments can be classified into switching and transmission categories. Switching equipment such as central offices, cross connects and branch exchanges are analogous to large mainframes or supercomputers. ABT octal and Widebus product families are targeted for these telecom equipments.

For transmission equipment such as line cards, bridgers and routers, product with enhanced datasheet specifications covering hot card insertion and power up/down is required. In these applications a board (card) is typically removed (inserted) from an active (hot) system for upgrade, maintenance or repair. The additional specifications characterize the device's performance when supply currents change (ramp) rapidly.

It is necessary to know how the device behaves when Vcc is 0 Volts, when Vcc is at the rail (5.5 Volts) and when Vcc ramps between these voltages. To address this requirement specifically for telecom transmission applications, ABT transceiver datasheets take into account Ii, Iozh, Iozl and Ioz current conditions for various Vcc ramp rates. Transmission system designers can then profile ABT device performance in hot card insertion and power up/down conditions.

SUMMARY

Texas Instruments provides the system designer with the most advanced products to date aiding the solution of complex design challenges. Advanced Bus Interface Logic (ABIL) products processed in sub-micron Advanced BiCMOS (ABT) address specific end equipment demands of the workstation, personal and portable computer, and telecom markets. Advanced fine-pitch package options such as SSOP, TSOP and SQFP offer space saving form factors. Circuit design techniques such as Bus Hold and Power-on-demand add value over competitive solutions.

The evolutionary roadmaps of process and package technology are summarized graphically in Figure 11 (next page). Solid lines indicate process technology migration for CMOS and BiCMOS. The minimum process dimension is represented on the ordinate in units of microns. The dashed line indicates package technology migration from PDIP to SOIC to SSOP to SQFP. For the dashed line, the ordinate now represents minimum lead pitch in millimeters.

The figure points out some interesting trends. BiCMOS solutions, initially well behind

their CMOS cousins in terms of performance, have closed the gap almost completely during the past 6 years. For 5 Volt logic applications ABT offers significant opportunity over an equivalent CMOS version particularly with the advent of thermally sensitive fine-pitch packages like the SQFP.

The Advanced BiCMOS opportunity is to provide more processing capability and overall throughput at a time when the next generation CMOS technologies are not quite ready or where a mixed technology approach provides a more practical solution. For ABIL products the high performance and drive capability of ABT are necessary for rack-mount supercomputers, workstation and telecom switching equipment. However, the low power consumption of ABT is necessary if these end equipments are to easily exist on the desktop. Low voltage LVT product appears positioned to supply personal computer and battery systems as they strive to incorporate workstation performance in portable formats.

As process geometries drop to 0.6 microns and below, Advanced BiCMOS and Advanced CMOS will continue to do battle in the pursuit of the best low voltage solutions. Future enhancements to Advanced BiCMOS may include extensions to a complementary structure of NPN and PNP transistors to better cope with reduction in power supply voltages. As supply voltages drop to 2.6 Volts and below, it appears more than likely that Advanced BiCMOS and Advanced CMOS will coexist as viable product technologies each supporting a dedicated group of customers. Time will tell.

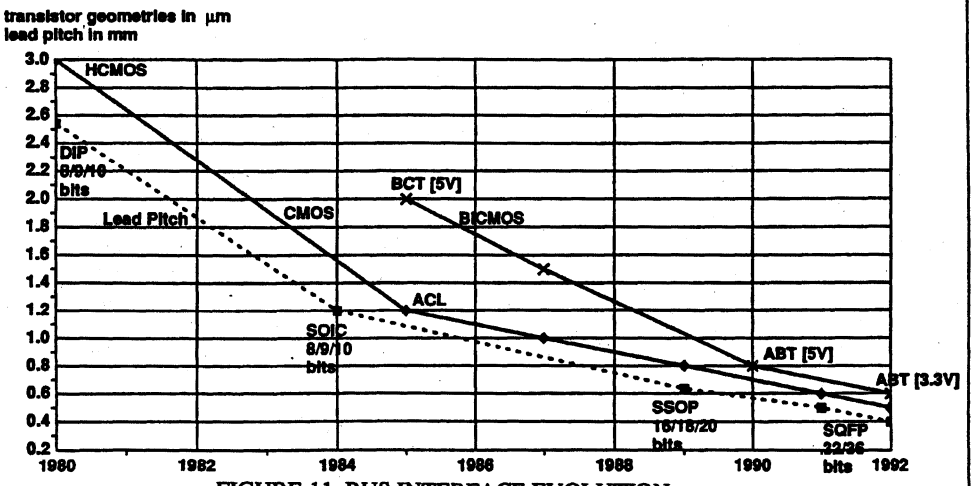


FIGURE 11. BUS INTERFACE EVOLUTION

ABT
Advanced BiCMOS Technology Characterization Information

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Contents

List of Illustrations

Appendices

INTRODUCTION

The purpose of this document is to assist the designers of high-performance digital logic systems in using the advanced BiCMOS technology logic family, referred to as ABT.

Detailed electrical characteristics of these bus interface devices are provided and, if available, tables and graphs have been included that compare specific parameters of the ABT family with those of other logic families.

In addition, typical data is provided to give the hardware designer a better understanding of how the ABT devices operate under various conditions.

The major subject areas covered in the report are as follows:

- AC Performance
- Power Considerations
- Input Characteristics
- Output Characteristics
- Signal Integrity
- Advanced Packaging
- Characterization Information

The characterization information provided is typical data and is not intended to be used as minimum or maximum specifications, unless noted as such.

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AC PERFORMANCE

As microprocessor operating frequencies increase, the period of time allotted for operations, such as memory access or arithmetic functions, decreases. With this in mind, Texas Instruments has developed a new family of bus interface devices – ABT, utilizing advanced BiCMOS technology. The goal of the ABT family of devices is to give system designers one bus interface solution which provides high drive capability, good signal integrity, and propagation delays short enough to appear transparent with respect to overall system performance.

Advances in IC process technology including smaller minimum feature size, tighter metal pitch, and shallower junctions, combine to provide stronger drive strengths and smaller parasitic capacitances. As a result, internal propagation delays have become extremely short. With the advent of the 0.8-µm, EPIC-IIB™ BiCMOS process and new circuit innovations, the ABT family offers typical propagation delays as low as 2-3 ns as shown in Figure 1. Maximum specifications are as low as 3-5 ns depending on the device type.

Figure 2 shows the propagation delay versus change in both temperature and supply voltage for an 'ABT16244A, 'FCT244A, and a 'F244 device. The graphs highlight two important aspects of the new ABT logic family. First, ABT interface devices have extremely short propagation delay times. The figures clearly show the improvement in speed of an ABT device over that of a 74F and 74FCTA device. Second, the variance in speed with respect to both temperature and supply voltage is minimal for ABT. At low temperatures, the increase in CMOS performance compensates for the decrease in bipolar device strength. At high temperatures, the reverse occurs. This complementary performance of both CMOS and bipolar devices on a single chip results in a slope which is virtually flat across the entire temperature range of –55°C to 125°C.

For most applications, the datasheet specifications may not provide all of the information a designer would like to see for a particular device. For instance, a designer might benefit from data such as propagation delay with multiple outputs switching or with various loads. This type of data is extremely difficult to test using automatic test equipment; therefore, it is provided in this document as family characteristics shown in Figure 2 and Figure 3.

In order to get a clear picture of where ABT stands in reference to other logic families, data is shown for a comparable (same function) 74F and 74FCTA device. It is clear that ABT is the designer's best choice for bus- interface applications which require consistent speed performance over various conditions.

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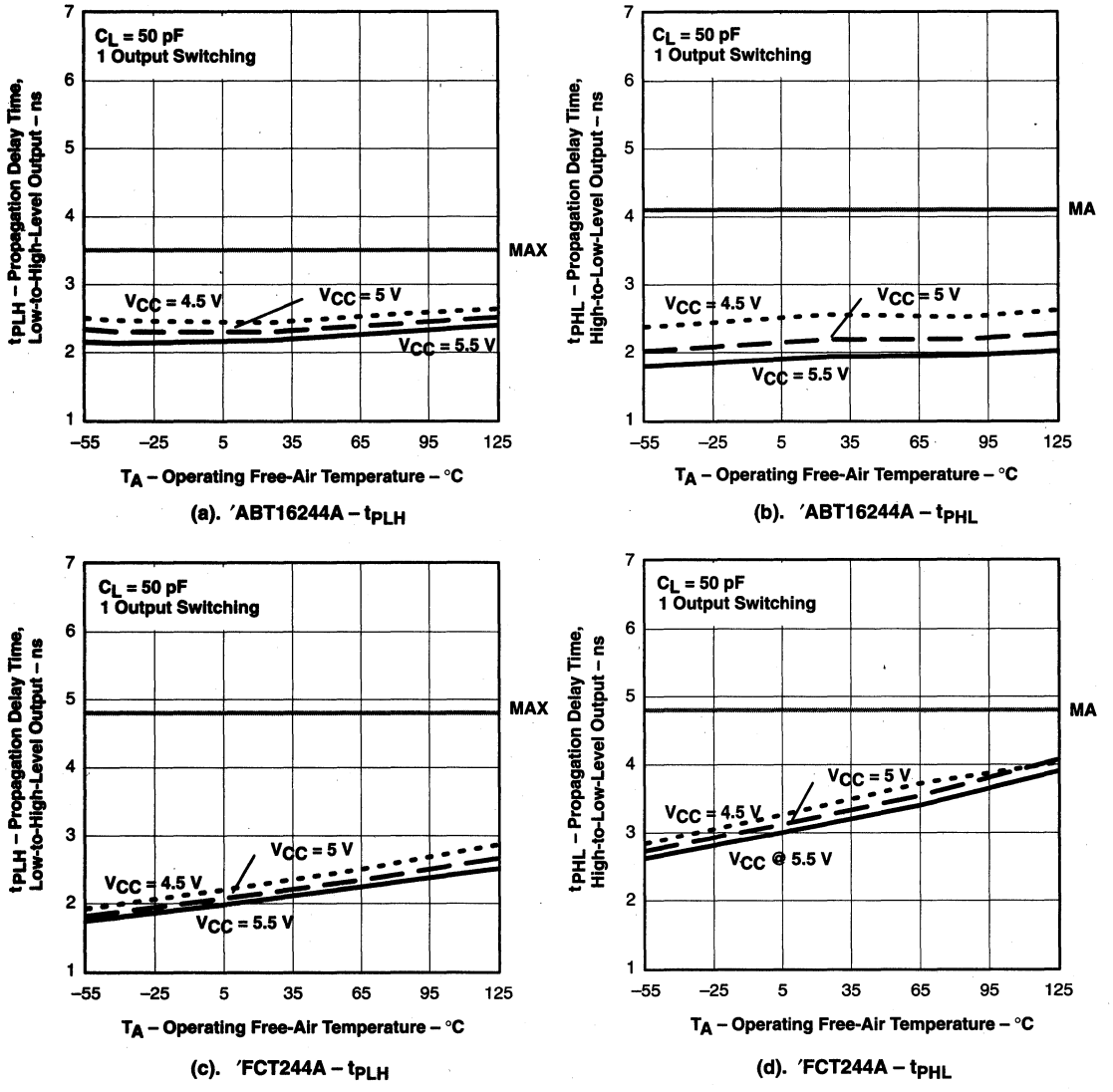
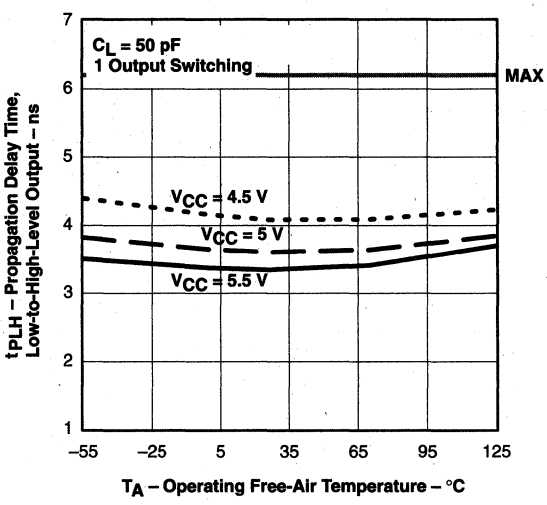
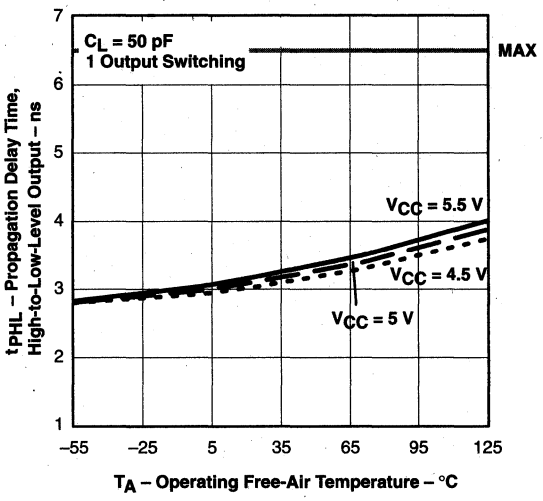


NOTE: MAX is datasheet specification.

Figure 1. Propagation Delay vs Operating Free-Air Temperature A to Y



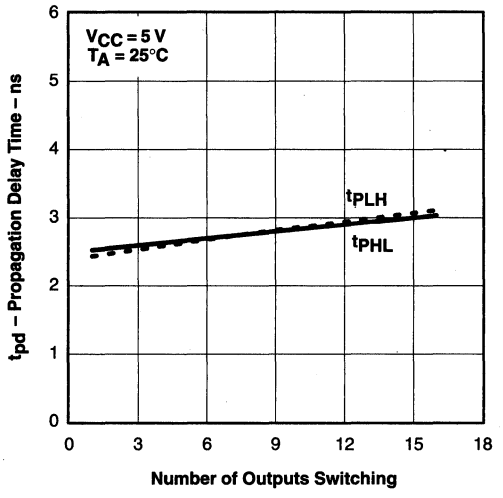
(e). 'F244 – t_{PLH}



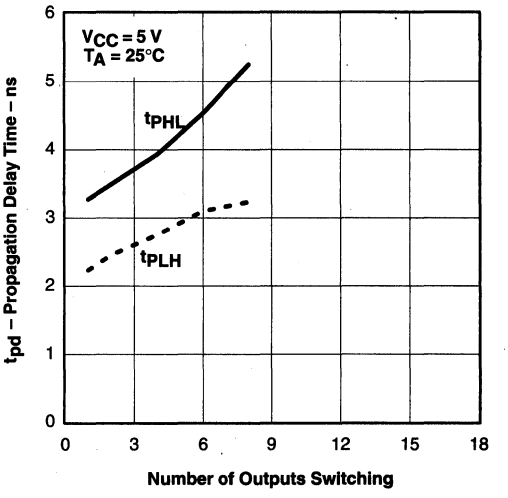
(f). 'F244 – t_{PHL}

NOTE: MAX is datasheet specification.

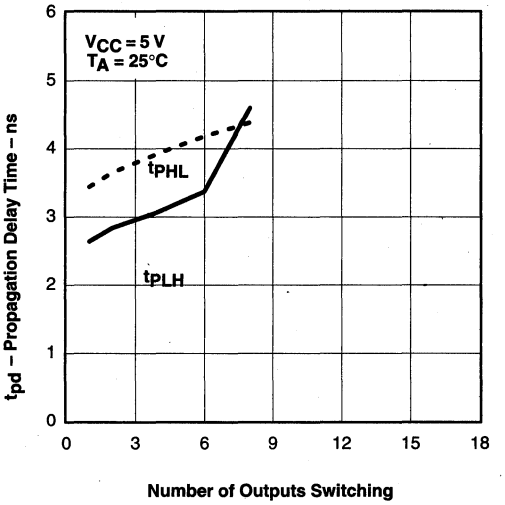
Figure 1. Propagation Delay vs Operating Free-Air Temperature A to Y (continued)



(a). 'ABT16244A

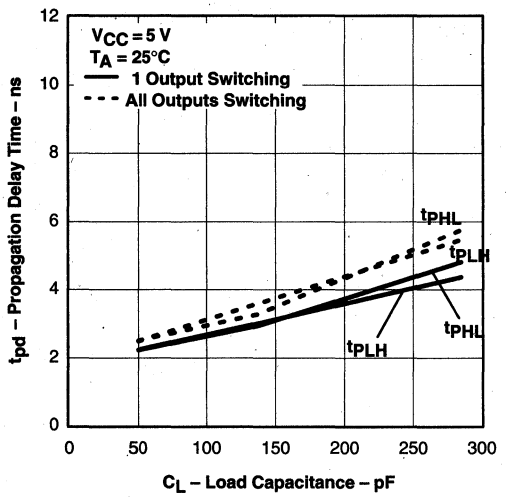


(b). 'FCT244A

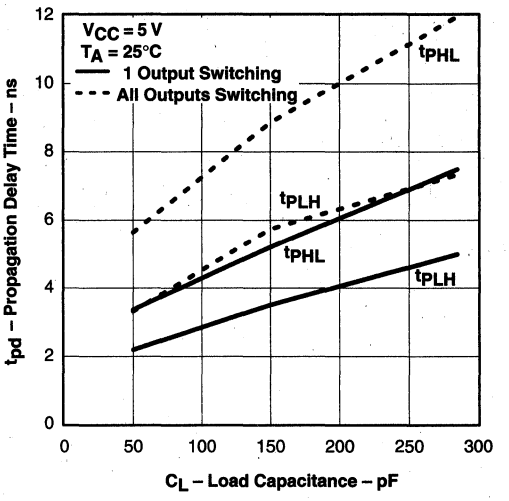


(c). 'F244

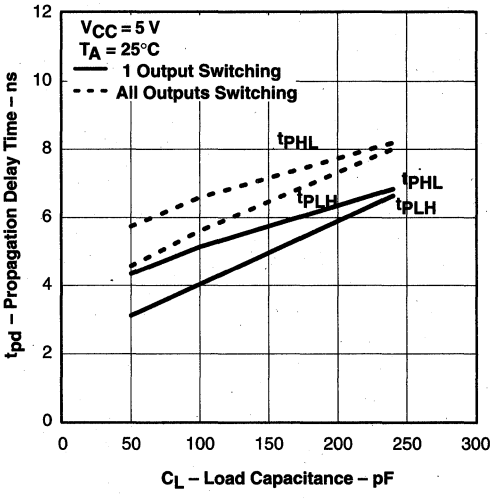
Figure 2. Propagation Delay Time vs Number of Outputs Switching



(a). 'ABT16244A



(b). 'FCT244A



(c). 'F244

Figure 3. Propagation Delay Time vs Capacitive Load

POWER CONSIDERATIONS

With the challenge to make systems more dense while improving performance comes the need to replace power-hungry devices without compromising speed. The ABT family of drivers provides a solution with low CMOS power consumption and high-speed bipolar technology together on a single device.

There are two basic things to consider when calculating power consumption, static (dc) power and dynamic power. Static power is calculated using the value of I_{CC} as shown in the datasheet. This is a dc value with no load on the outputs. To understand the relationship between pure CMOS, pure bipolar, and advanced BiCMOS for dc power rating, see Table 1 which shows the various datasheet values. The bipolar device shows the highest I_{CC} values, with little relief regardless of the state of the outputs. This is not the case with ABT octals, which offer the low static power consumption of CMOS while in the high-impedance state, or when the outputs are high (I_{CCZ}, I_{CCH}).

Dynamic power involves the charging and discharging of internal capacitances as well as the external load capacitance. It is this dynamic component which makes up the majority of the total power dissipation. Figure 4 shows power as a function of frequency for ABT, FCT and F devices. Although bipolar devices tend to have extremely high static power, there is a point on the frequency curve, commonly referred to as the crossover point, where the CMOS device no longer consumes less power. With ABT devices, the power increase at higher frequencies is less than that of the pure CMOS FCT.

The use of bipolar transistors in the output stage is advantageous in two ways. First, the voltage swing is less than with a CMOS output, reducing the power consumed when charging or discharging the external load. Second, bipolar transistors are capable of turning off more efficiently than CMOS transistors, thus reducing the flow of current from V_{CC} to GND. Combined, these features allow for better power performance at high frequencies.

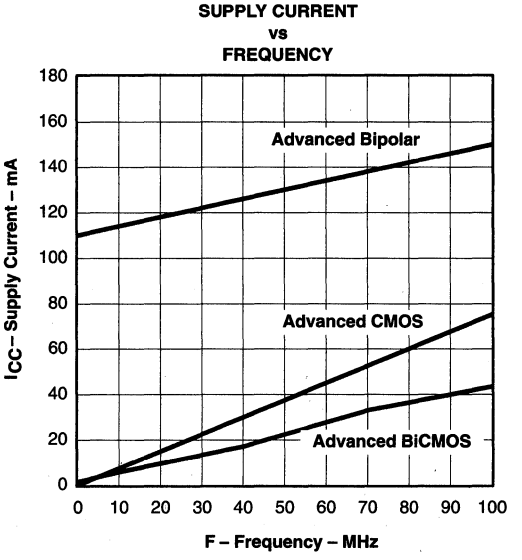


Figure 4. Supply Current vs Frequency

Table 1. Supply Current

PARAMETER	TEST CONDITIONS		'F244		'FCT244		SN74ABT244	
			MIN	MAX	MIN	MAX	MIN	MAX
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		60 mA				250 µA
		Outputs low		90 mA				30 mA
		Outputs disabled		90 mA				250 µA
I_{CC}	V_{CC} = maximum, V ≥ V_{CC} – 0.2 V, V ≤ V_{CC} – 0.2 V					1.5 mA		

INPUT CHARACTERISTICS

ABT bus interface devices are designed to guarantee TTL-compatible input levels switching between 0.8 V and 2 V (typically 1.5 V). Additionally, these inputs are implemented with CMOS circuitry, resulting in high impedance (low leakage) and low capacitance which reduces overall bus loading. This section is an overview of the circuitry utilized for a typical ABT input, the corresponding electrical characteristics, and guidelines for proper termination of unused inputs.

ABT Input Circuitry

Figure 5 shows a typical ABT input schematic. A pure CMOS-input threshold is normally set at one half of V_{CC}. In order to shift the threshold voltage to be centered around 1.5 V (see Figure 6), the supply voltage of the input stage is dropped by the diode, D1, and the transistor, Q1. Reducing the voltage at the source of Q_p enables it to turn off more efficiently when flow is from V_{CC} to GND (ΔI_{CC}). When the input is in the low state, Q_r raises the voltage of the source of Q_p to V_{CC} to ensure proper operation of the following stage. This feedback circuit provides approximately 100 mV of input hysteresis which increases the noise margin and helps ensure the device will be free from oscillations when operated within specified input ramp rates.

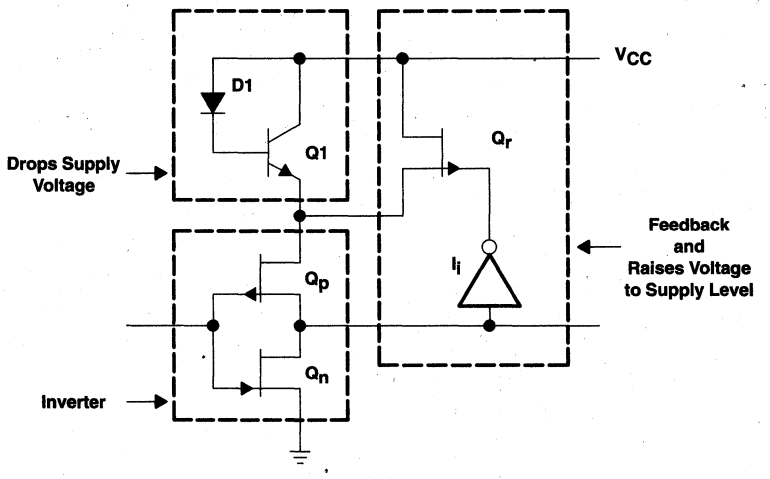


Figure 5. Simplified Input Stage of an ABT Circuit

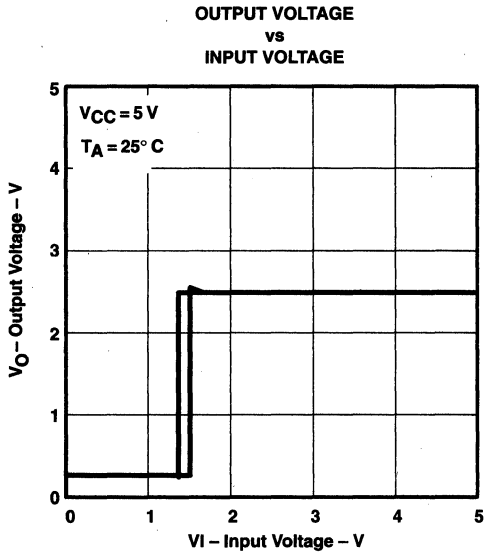


Figure 6. Output Voltage vs Input Voltage

INPUT CURRENT LOADING

The utilization of sub-micron (0.8-µm) CMOS technology for the input stage of ABT devices causes minimal loading of the system bus due to low leakage currents and low capacitance. The small geometries of the EPIC-IIB™ process have resulted in capacitances as low as 3 pF for inputs and 8 pF for $C_{i/o}$ of a transceiver. Figure 7 and Table 2 indicate the low input current performance and specifications. Considering this low capacitance along with the negligible input current, it is clear that systems designers will be able to decrease their overall bus loading.

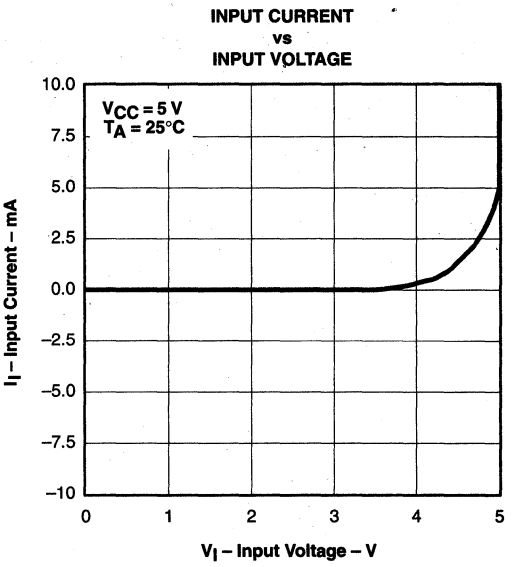


Figure 7. Input Current vs Input Voltage

Table 2. Input Current Specifications

PARAMETER	TEST CONDITIONS	T_A = 25°C			SN54ABT245		SN74ABT245		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND			±1		±1		±1	µA
I_{OZH}†	V_{CC} = 5.5 V, V_O = 2.7 V			50		50		50	µA
I_{OZL}†	V_{CC} = 5.5 V, V_O = 0.5 V			−50		−50		−50	µA

† The parameters I_{OZH} and I_{OZL} include the input leakage current

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SUPPLY CURRENT CHANGE (ΔI_{CC})

Because ABT devices utilize a CMOS-input stage but operate in a TTL-level signal environment, there is a current specification unique to this set of conditions known as ΔI_{CC}. Given a CMOS inverter with the input voltage set so that both the p and n channel devices are on, current will flow from V_{CC} to GND. This can occur when the input to an ABT device is at a valid high level (>2 V) which will turn on the n-channel, but not high enough to completely turn off the p-channel device. The current which flows under these conditions is specified in the datasheet (ΔI_{CC}) and is measured one input at a time with the input voltage set at 3.4 V. Figure 8 shows the change in I_{CC} as the input is ramped from 0 V to 5 V. For ABT non-storage devices, a feature is added which turns the input off when the outputs are disabled in order to reduce power consumption (see Table 3 for an example. Refer to individual datasheets for this specification).

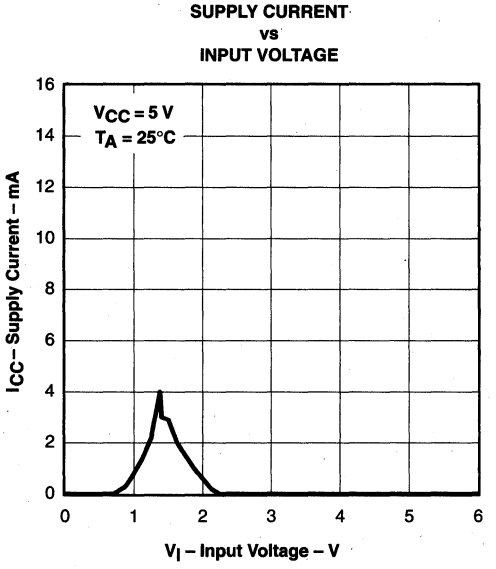

Figure 8. Supply Current vs Input Voltage

Table 3. Supply Current Change (ΔI_{CC})

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT244		SN74ABT244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC}†	V_I = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	µA

† This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Proper Termination of Unused Inputs

With advancements in speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output glitching or, in some cases, oscillations. Similar situations can occur if an unused input is left floating or not being actively held at a valid logic level.

These problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 9). Since the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, the inductive voltage spikes (V_{gnd}) affect the way signals appear to the internal gate structures. For instance, as the voltage at the device's ground node rises, the input signal (V_i') will appear to decrease in magnitude. This undesirable phenomena can erroneously change the output's transition if a threshold violation takes place.

In the case of a slowly rising input edge, if the ground movement is large enough, the apparent signal, V_i', at the device will appear to be driven back through the threshold and the output will start to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents) the slow input edge will be repeatedly driven back through the threshold, resulting in output oscillation.

ABT devices are recommended to have input edge rates faster than 5 ns/V for standard parts, and 10 ns/V for the Widebus™ series of products when the outputs are enabled. A critical area for this edge rate is in the transition region between 1 V and 2 V. It is also recommended to hold inputs or I/O pins at a valid logic high or low when they are not being used or when the part driving them is in the high-impedance state.

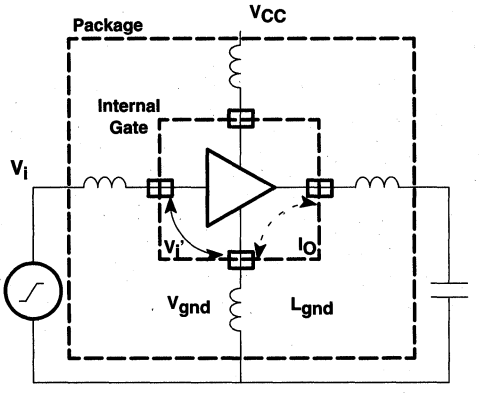

Figure 9. Sample Input/Output Model

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OUTPUT CHARACTERISTICS

The current trend is consolidation of the functionality of multiple logic devices into complex, high pin-count ASICs and programmables. There are a number of important advantages for utilizing bus-interface devices in standard high-volume packages. These include the need for high drive capability and good signal integrity. The use of bipolar circuitry in the output stage makes it possible to provide these requirements, along with increased speed, using the ABT family.

Figure 10 shows a simplified schematic of an ABT output stage. Data is transmitted to the gate of M1, which acts as a simple current switch. When M1 is turned on, current flows through R1 and M1 to the base of Q4, turning it on and driving the output low. At the same time, the base of Q2 is pulled low, thus turning off the upper output. For a low-to-high transition, the gate of M1 must be driven low, turning M1 off. Current through R1 will charge the base of Q2, pulling it high and turning on the Darlington pair consisting of Q2 and Q3. Meanwhile, with its supply of base drive cut off, Q4 turns off, and the output switches from low to high. R2 is used to limit output current in the high state, and D1 is a blocking diode used to prevent reverse current flow in specific power-down applications.

A clear advantage of using bipolar circuitry in the output stage (as opposed to CMOS) is the reduced voltage swing. This helps to lower ground noise and reduce power consumption. Refer to the sections on Signal Integrity and Power Considerations for further information.

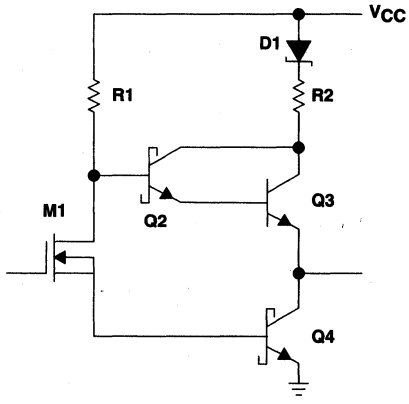


Figure 10. Simplified ABT Output Stage

Output Drive

The I_{OH} and I_{OL} curves for a typical ABT output are shown in Figure 11. With a specified I_{OL} of 64 mA and I_{OH} of −32 mA, ABT will accommodate many standard backplane specifications. However, these devices are capable of driving well beyond these limits. This is important when considering switching a low-impedance backplane on the incident wave.

Incident-wave switching ensures that for a given transition (either high-to-low or low-to-high) the output will reach a valid V_{IH} or V_{IL} level on the initial wave front (i.e., does not require reflections). Figure 12 shows the possible problems a designer might encounter when a device does not switch on the incident wave. A shelf below $V_{IL(max)}$, signal A, will cause the propagation delay to slow by the amount of time it takes for the signal to reach the receiver and reflect back. Signal B shows the case where there is a shelf in the threshold region. When this happens the input to the receiver is uncertain and could cause several problems associated with slow input edges, depending on the length of time the shelf remains in this region. A signal as seen in example C will not cause a problem because the shelf does not occur until the necessary V_{IH} level has been attained.

Using typical V_{OH} and V_{OL} values along with data points from the curves, ABT devices can typically drive lines in the 25-Ω range on the incident wave.

For a low-to-high transition,
(I_{OH} = 85 mA @ V_{OH} = 2.4 V)

$$Z_{LH} = \frac{V_{OH}(min) - V_{OL}(typ)}{I_{OH}} = \frac{2.4\ V - 0.3\ V}{85\ mA} = 25\ \Omega$$

For a high-to-low transition,
(I_{OL} = 135 mA @ V_{OL} = 0.5 V)

$$Z_{HL} = \frac{V_{OH}(typ) - V_{OL}(max)}{I_{OL}} = \frac{3.5\ V - 0.5\ V}{135\ mA} = 22\ \Omega$$

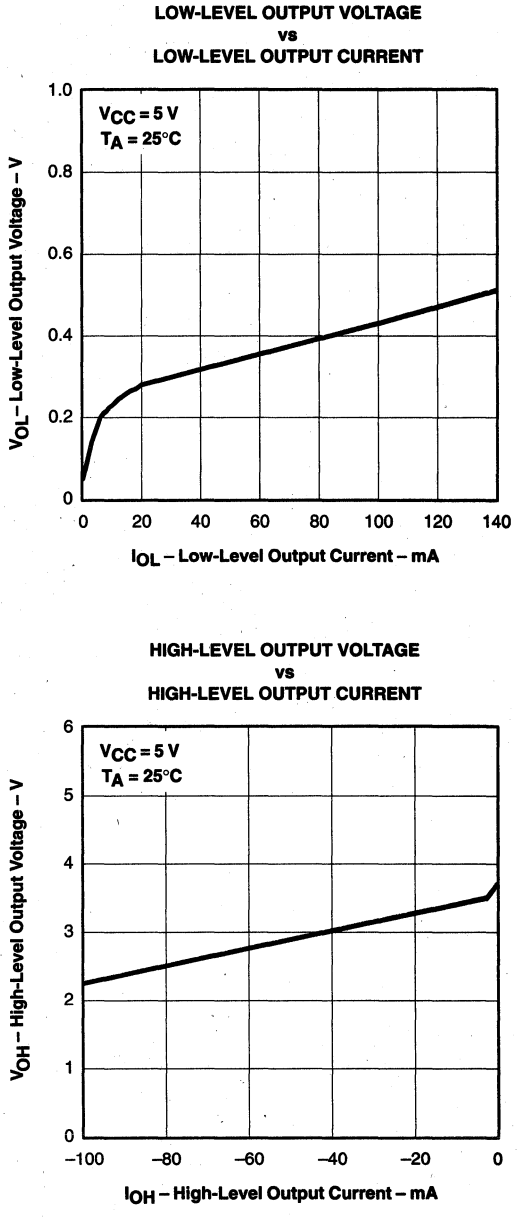


Figure 11. Typical ABT Output Characteristics

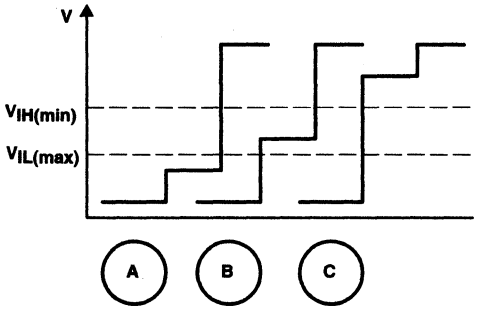


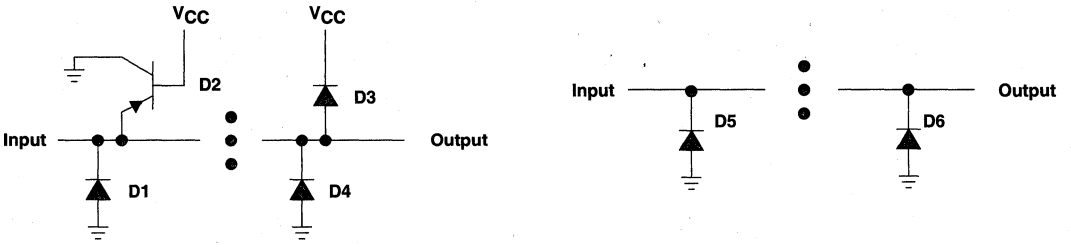
Figure 12. Reflected Wave Switching

Partial Power Down

One application, addressed when designing the ABT family, is partial system power down. When using a standard CMOS device, there is a path from either the input or the output (or both) to V_{CC}. This prevents partial power down for such applications as *hot card insertion* without adding current limiting components. This is not the case with ABT as these paths have been eliminated with the use of blocking diodes.

Figure 13 shows functionally equivalent schematics of the input structures for CMOS and ABT devices.

Consider the situation shown in Figure 14. The driving device is powered with V_{CC} = 5 V while the receiving device is powered down (V_{CC} = 0). If these devices are CMOS, the receiver can be powered up through the diode, D2, when the driver is in a high state. ABT devices do not have a comparable path and are thus immune to this problem, making them more desirable for this application.



(a) CMOS EQUIVALENT INPUT STRUCTURE

(b) ABT EQUIVALENT INPUT STRUCTURE

Figure 13. Simplified Input Structures for CMOS and ABT Devices

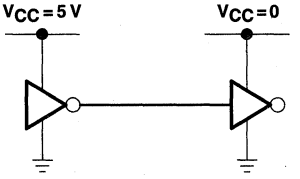


Figure 14. Example of Partial System Power Down

SIGNAL INTEGRITY

A frequent concern system designers have is the performance degradation of ICs when outputs are switched. Texas Instruments priority when designing the ABT bus interface family is to insure signal integrity and eliminate the need for excess settling time of an output waveform. This section addresses the simultaneous switching performance of both the ABT octals and the Widebus™ functions.

Simultaneous Switching Phenomenon

NO TAG shows a simple model of an output pin, including the associated capacitance of the output load and the inherent inductance of the ground lead. The voltage drop across the GND inductor, V_L, is determined by the value of the inductance and the rate of change in current across the inductor. When multiple outputs are switched from high to low, the transient current (di/dt) through the GND inductor generates a difference in potential on the chip ground with respect to the system ground. This induced GND variation can be observed indirectly as shown in Figure 16. The voltage output low peak (V_{OLP}) is measured on one quiet output when all others are switched from high to low.

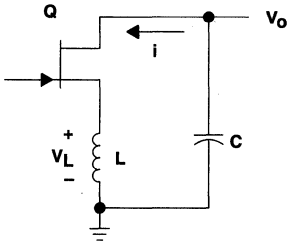
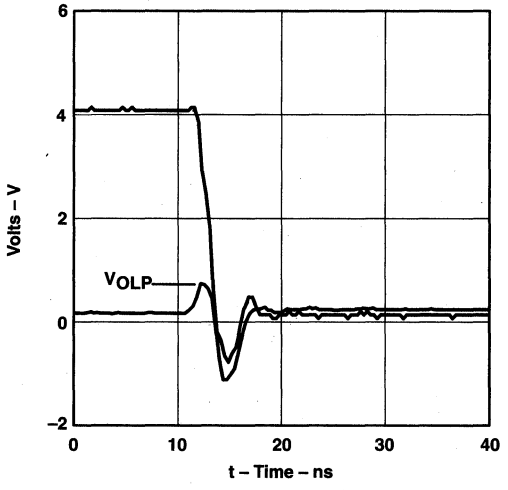


Figure 15. Simultaneous Switching Output Model



NOTE: V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs

Figure 16. Simultaneous Switching Noise Waveform

A similar phenomena occurs with respect to the V_{CC} plane on a low-to-high transition, known as voltage output high valley (V_{OHV}). Most problems are associated with a large V_{OLP} because the range for a logic 0 is much less than the range for a logic 1, as seen in Figure 17. For a comprehensive discussion of simultaneous switching, see the "Simultaneous Switching Evaluation and Testing" application note or the *Advanced CMOS Logic Designer's Handbook* from Texas Instruments.

The impact of these voltage noise spikes on a system can be extreme. The noise can cause loss of stored data, severe speed degradation, false clocking, and/or reduction in system noise immunity. For an overview of how propagation delay is affected by the switching of multiple outputs, please refer to the AC Performance section of this document.

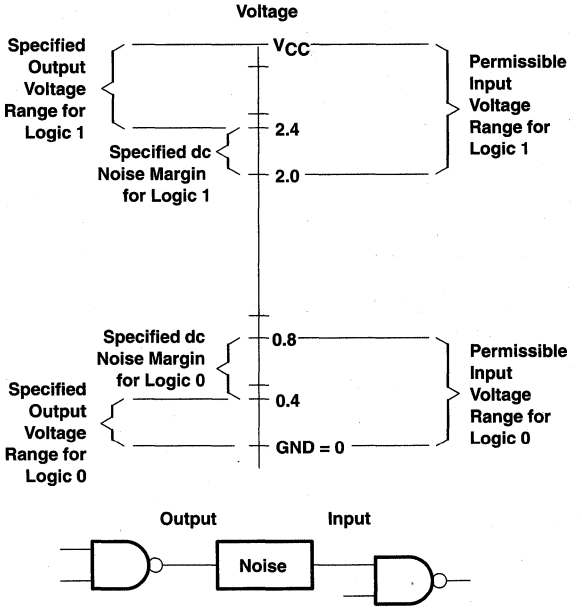


Figure 17. TTL dc Noise Margin

Simultaneous Switching Solutions

Some methods an IC manufacturer can use to reduce the effects of simultaneous switching include: reducing the inductance of the power pins, adding multiple power pins, and controlling the turn on of the output. These techniques are described in depth in the 1988 Texas Instruments *Advanced CMOS Logic (ACL) Designer's Handbook.*

Octal ABT devices employ the standard end-pin GND and V_{CC} configuration while maintaining acceptable simultaneous switching performance, as seen in Figure 18. This is due to the TTL-level output swing (0.3–3 V) and a controlled feedback which limits the base drive to the lower output.

The ABT Widebus™ series (16-, 18-, and 20-bit functions) are offered in an SSOP package (see the Packaging section of this document) which was developed by Texas Instruments to save valuable board space and reduce simultaneous switching effects. One might expect an increase in noise with sixteen outputs switching in a single package; however, the simultaneous switching performance is actually improved. There is a GND pin for every two outputs and a V_{CC} pin for every four. This allows the transient current to be distributed across multiple power pins and decreases the overall d_i/d_t effect. This results in a typical V_{OLP} value on the order of 500 mV for the ABT16500, as shown in Figure 19.

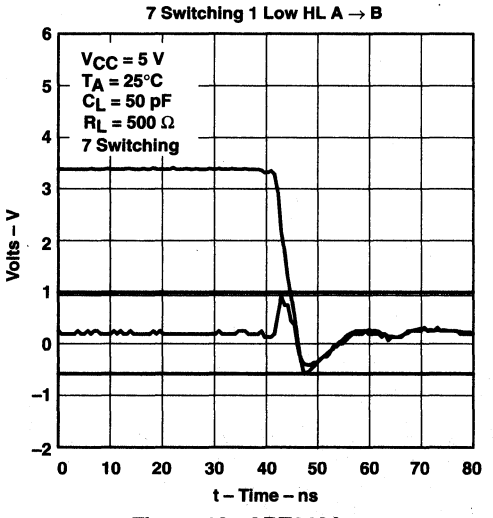


Figure 18. ABT646A Simultaneous Switching Waveform

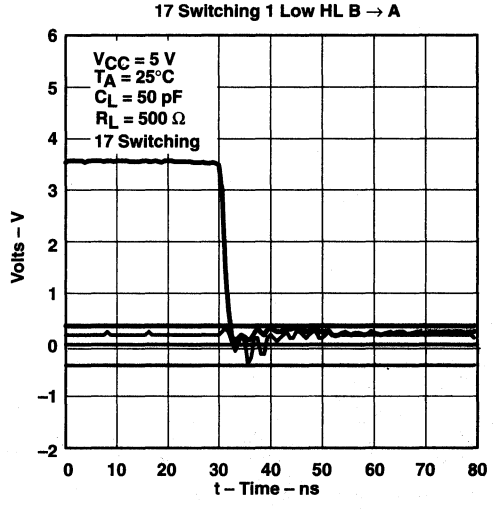


Figure 19. ABT16500A Simultaneous Switching Waveform

ADVANCED PACKAGING

Along with a strong commitment to provide fast, low- power, high-drive integrated circuits, Texas Instruments is the clear-cut leader in logic packaging advancements. The development of the shrink small- outline package (SSOP) in 1989 provided system designers the opportunity to reduce the amount of board space required for bus interface devices by 50%. Several 24-pin solutions including the familiar SOIC, the SSOP, and the TSOP (thin small-outline package) are shown in Figure 20.

The 48/56-pin SSOP packages allow for twice the functionality (16-, 18-, and 20-bit functions) in approximately the same board area as a standard SOIC. This is accomplished by using a 25-mil (0.635 mm) lead pitch, as opposed to 50-mil (1.27 mm) in SOIC. NO TAG shows a typical pinout structure for the 48-pin SSOP. The flow-through architecture is standard for all Widebus™ devices, making signal routing easier during board layout. Also note the distributed GND and V_{CC} pins, which improve simultaneous switching effects as discussed in the Signal Integrity section of this document.

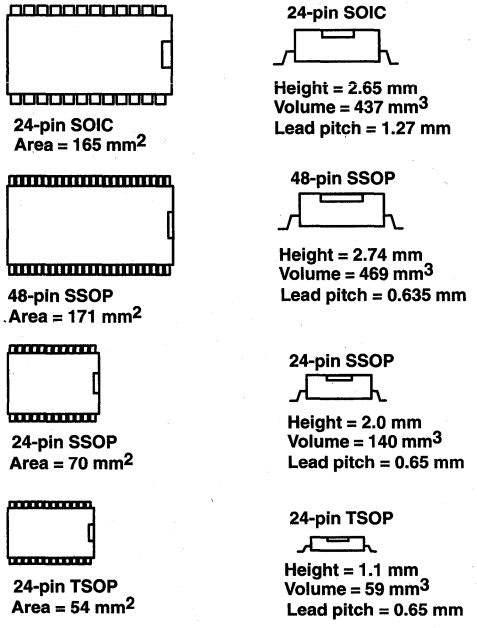


Figure 20. 24-Pin Surface Mount Comparison

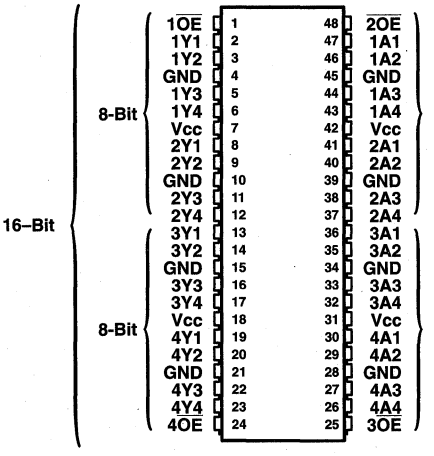


Figure 21. Distributed Pinout of 'ABT16244A

When using the small pin count SSOPs (8-, 9-, and 10-bit functions) the same functionality will occupy less than half the board area of a SOIC (70 mm^2 vs 165 mm^2). There is also a height improvement over the SOIC which is beneficial when the spacing between boards is a consideration. For very dense memory arrays the packaging evolution has been taken one step further with the emerging TSOP. The TSOP thickness of 1.1 mm gives a 58% height improvement over the SOIC.

Table 4 provides a quick reference of the mechanical specifications of the various SSOP packages. If more specific information is required see the *SSOP Designer's Handbook* or the application note Advanced Bus Interface Solutions Utilizing Fine Pitch Surface Mount Packages.

Table 4. SSOP Metric Specifications

PACKAGE SPECIFICATIONS						PIN SPECIFICATIONS	
PACKAGE TYPE	PINS	INDUSTRY STANDARD	THICKNESS (mm)	BODY WIDTH (mm)	STANDOFF HEIGHT (mm)†	PIN PITCH (mm)	PIN WIDTH (mm)
SSOP	20	EIAJ	2.00	5.3	0.05	0.650	0.30
SSOP	24	EIAJ	2.00	5.3	0.05	0.650	0.30
SSOP	28	JEDEC	2.59	7.5	0.20	0.635	0.25
SSOP	48	JEDEC	2.59	7.5	0.20	0.635	0.25
SSOP	56	JEDEC	2.59	7.5	0.20	0.635	0.25

† Minimum values

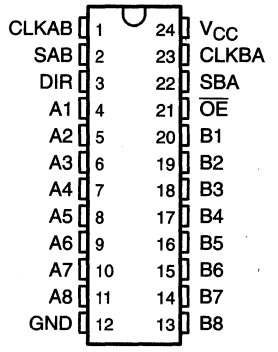
All values are maximum typical values unless otherwise indicated.

APPENDIX A
'ABT646A

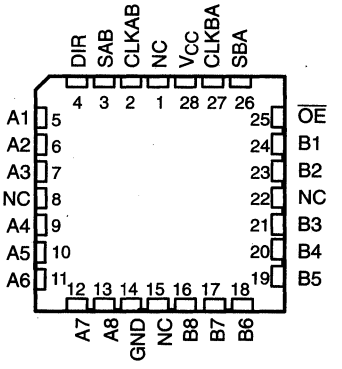
A

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT646A . . . JT PACKAGE
SN74ABT646A . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT646A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT646A.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

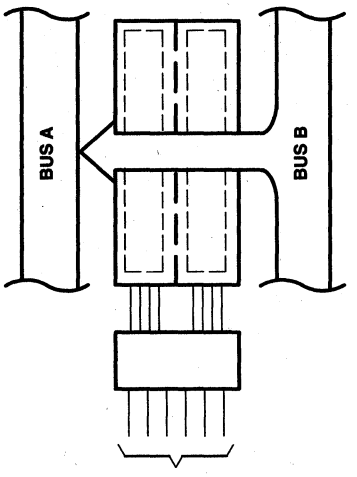
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT646A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

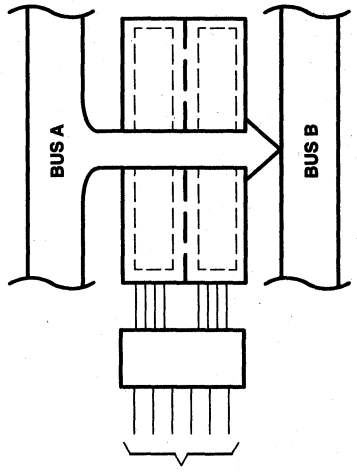
The SN54ABT646A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT646A is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



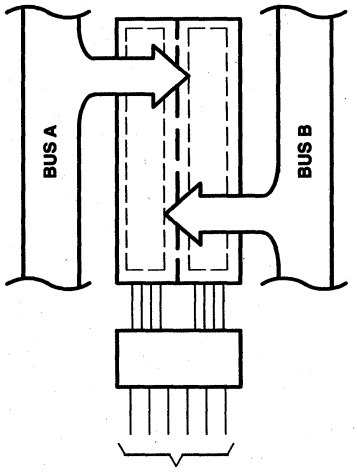
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



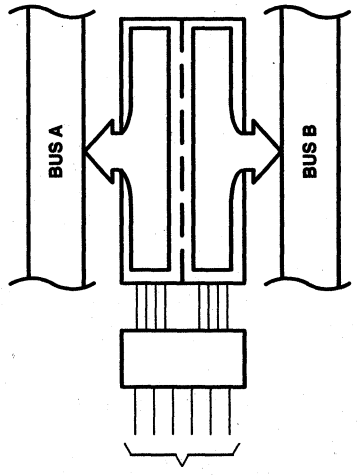
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

Figure 1. Bus-Management Functions

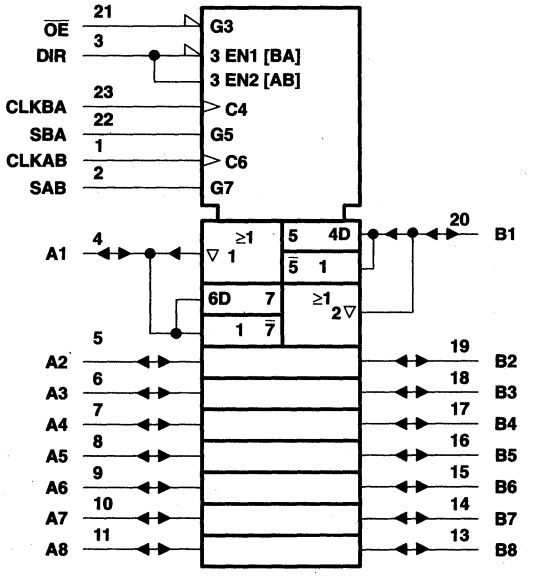
Pin numbers shown are for the DB, DW, JT, and NT packages.

FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

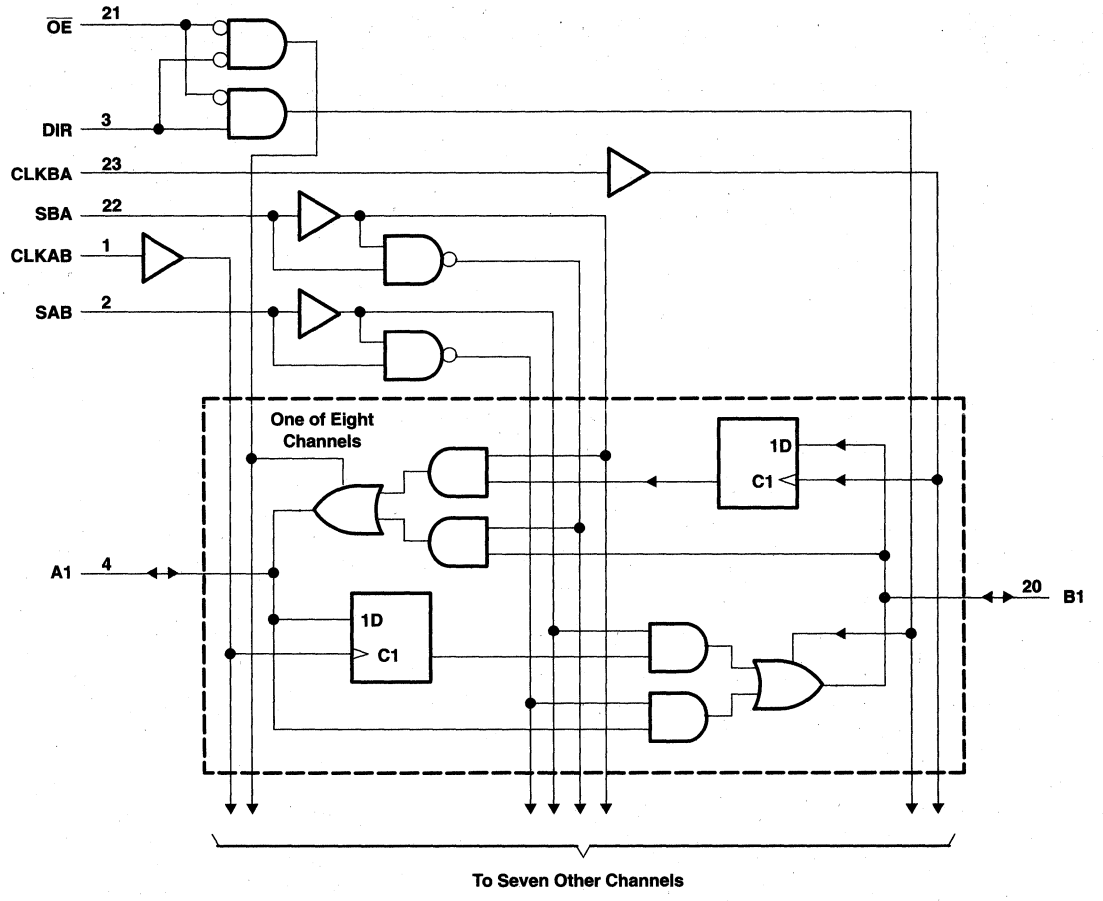
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT646A ..... 96 mA
SN74ABT646A ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.7 W
DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT646A		SN74ABT646A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT646A		SN74ABT646A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = –3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V, I_{OH} = –24 mA		2			2				
	V_{CC} = 4.5 V, I_{OH} = –32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Control inputs			±1		±1		±1	µA
		A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V				10¶		10¶		10¶	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V				–10¶		–10¶		–10¶	µA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O#	V_{CC} = 5.5 V, V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			250		250		250	µA
		Outputs low			30		30		30	mA
		Outputs disabled			250		250		250	µA
ΔI_{CC}‖	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V	Control inputs		7						pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports		12						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ This data sheet limit may vary among suppliers.
# Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

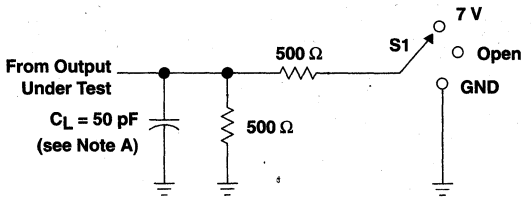
		V_{CC} = 5 V, T_A = 25°C		SN54ABT646A		SN74ABT646A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low	4		4		4		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3		3.5		3		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		1.5		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT646A		SN74ABT646A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	6.7	2.2	5.6	ns
t_{PHL}			1.7	4	5.1	1.2	6.7	1.7	5.6	
t_{PLH}	A or B	B or A	1.5	3	4.3	1.5	5	1.5	4.8	ns
t_{PHL}			1.5	3.3	4.6	1.5	5.6	1.5	5.4	
t_{PLH}	SAB or SBA†	B or A	1.5	4	5.1	1.5	7.8	1.5	6.5	ns
t_{PHL}			1.5	3.6	4.9	1.5	6.2	1.5	5.9	
t_{PZH}	$\overline{OE}$	A or B	1.5	4.3	5.3	1.5	7	1.5	6.3	ns
t_{PZL}			3	5.8	7.4	3	10.5	3	8.8	
t_{PHZ}	$\overline{OE}$	A or B	1.5	3.5	4.5	1	7.3	1.5	5	ns
t_{PLZ}			1.5	3	4	1.5	5.7	1.5	4.5	
t_{PZH}	DIR	A or B	1.5	4.5	5.7	1.5	7.3	1.5	6.7	ns
t_{PZL}			2.5	6.5	9	2.5	11	2.5	9.5	
t_{PHZ}	DIR	A or B	1.5	3.8	5	1	9	1.5	5.7	ns
t_{PLZ}			1.5	3.8	4.7	1.2	6.7	1.5	6	

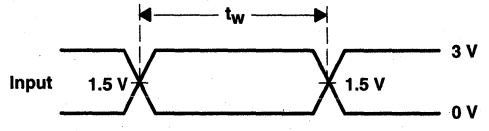
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

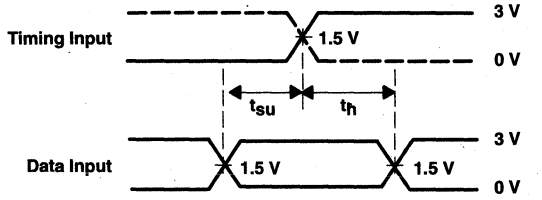


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

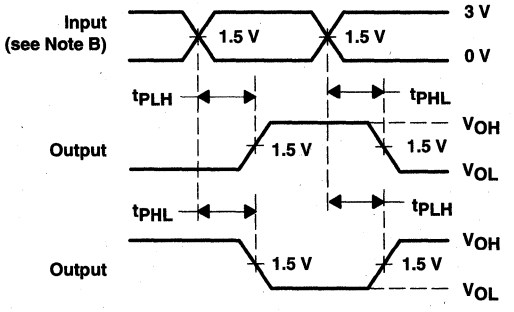
LOAD CIRCUIT FOR OUTPUTS



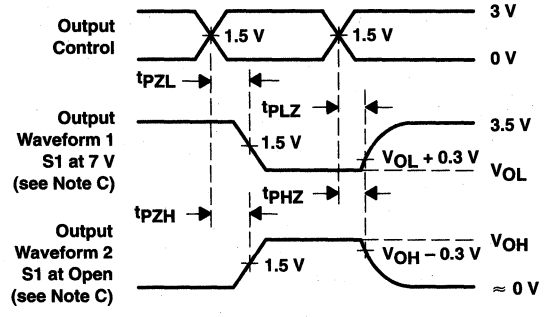
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



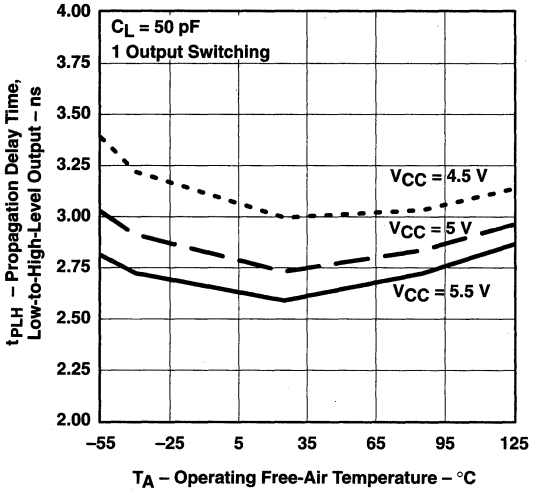
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

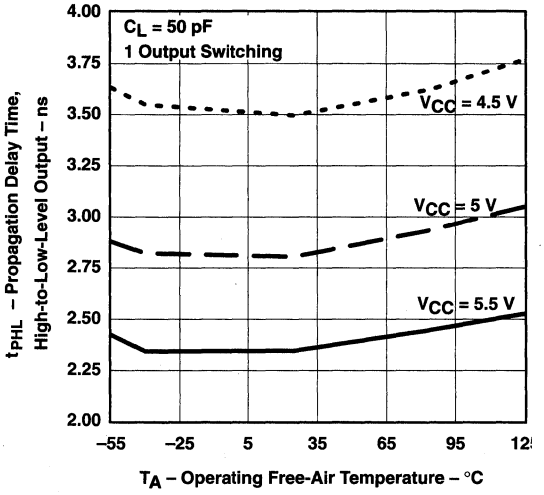
Figure 2. Load Circuit and Voltage Waveforms

Propagation Delay Time vs Temperature

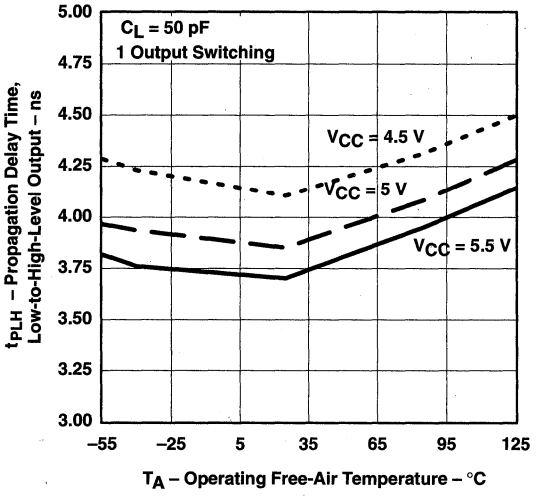
PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A to B



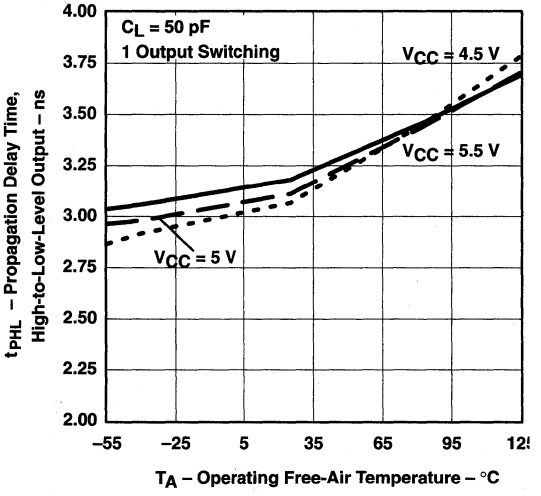
PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A to B



PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
CLKAB to B

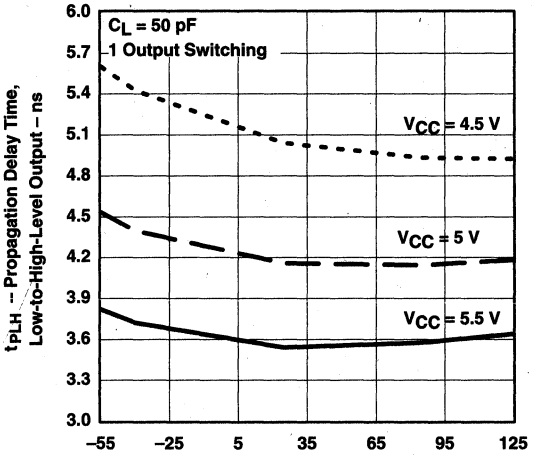


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
CLKAB to B

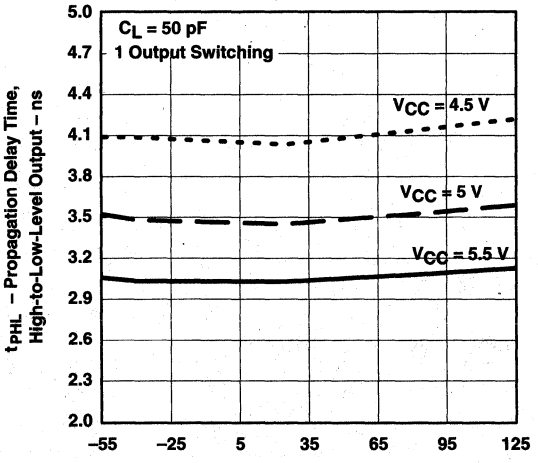


Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
SAB to B

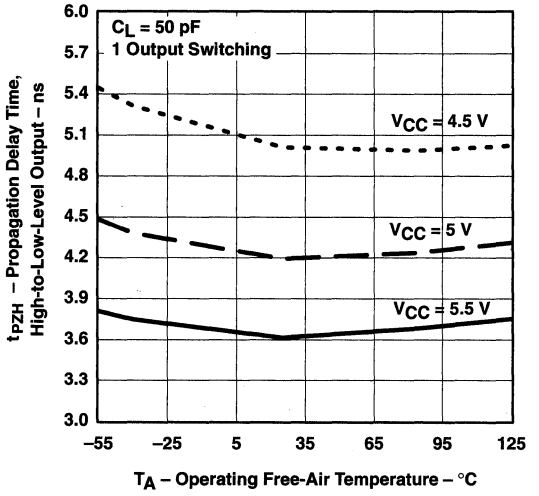


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
SAB to B

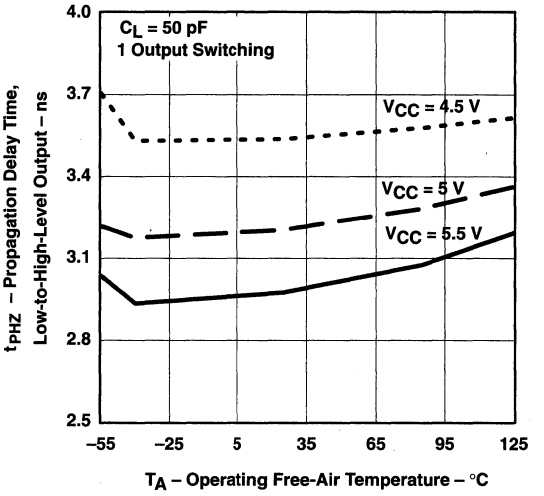


Propagation Delay Time vs Temperature

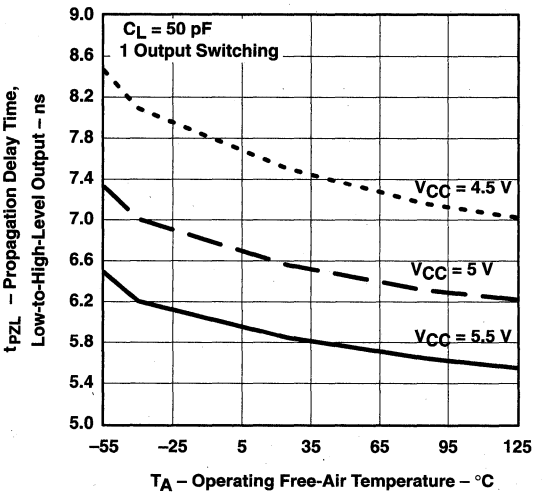
PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ to B



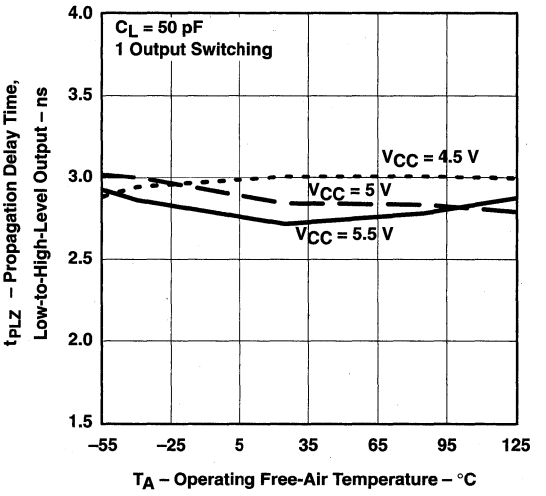
PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ to B



PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ to B

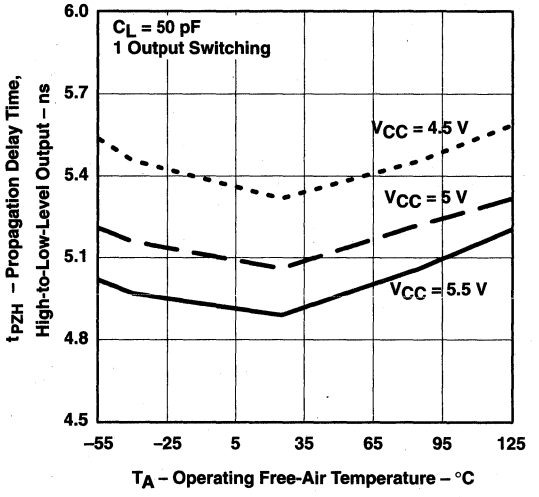


PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ to B

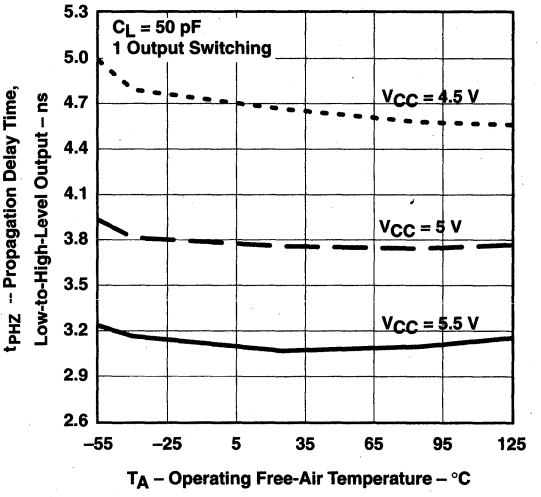


Propagation Delay Time vs Temperature

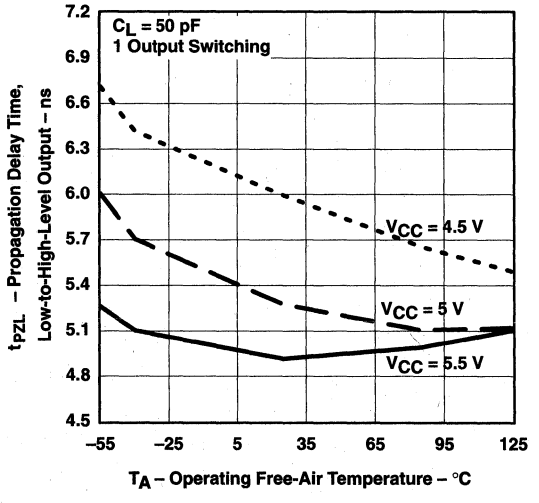
PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR to B



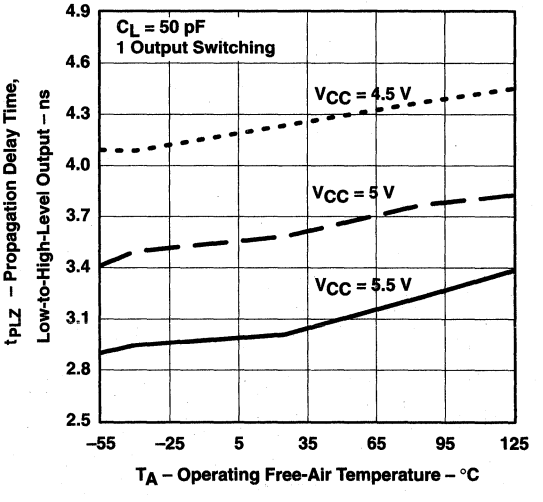
PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR to B



PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR to B

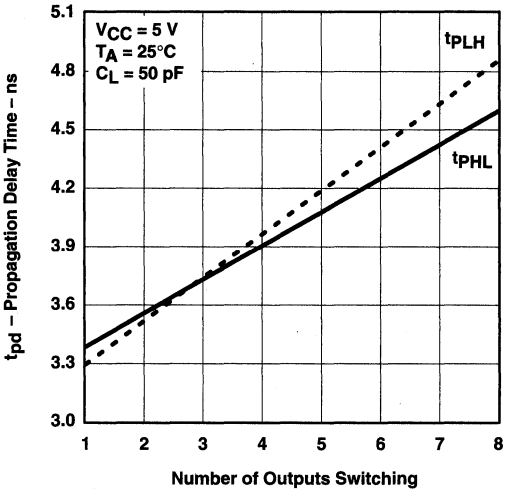


PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR to B

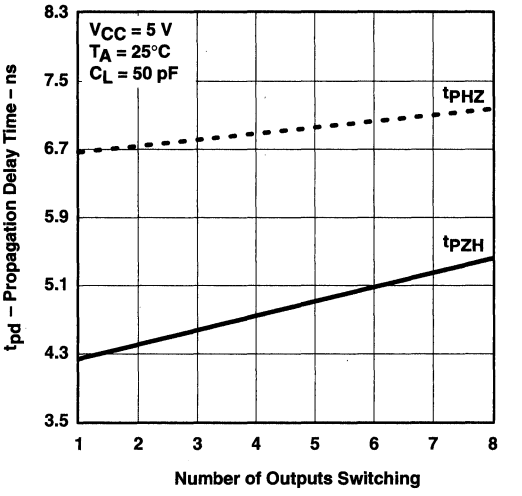


Propagation Delay Time vs Number of Outputs Switching

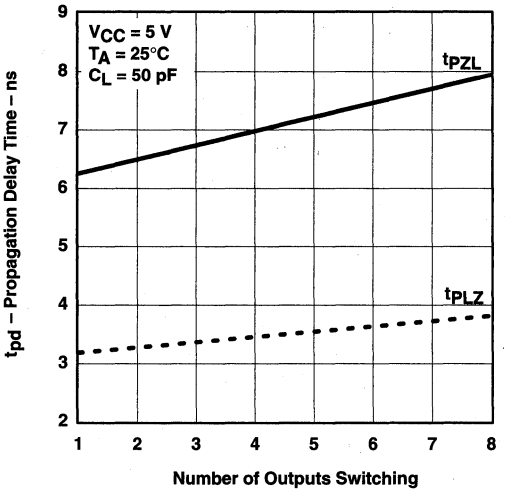
PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A to B



PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A to B

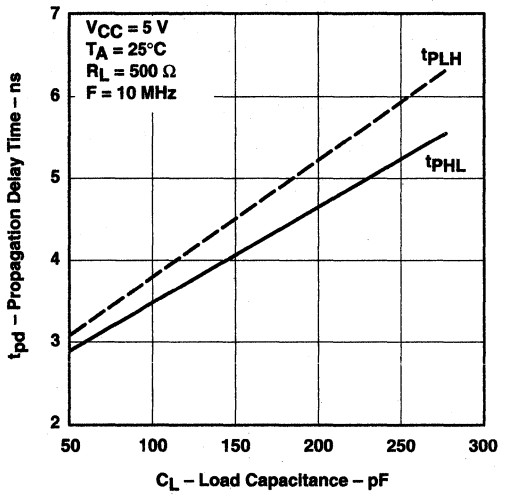


PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A to B

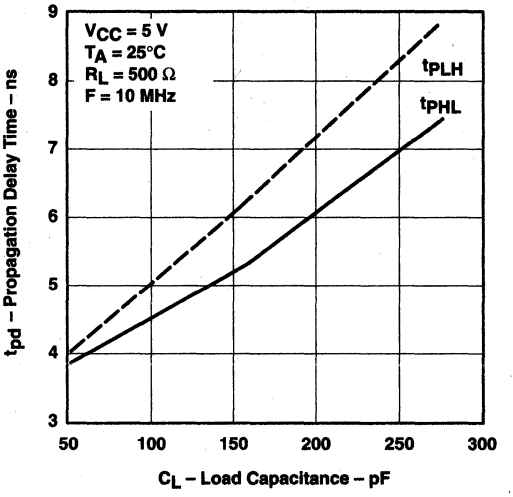


Propagation Delay Time vs Load Capacitance

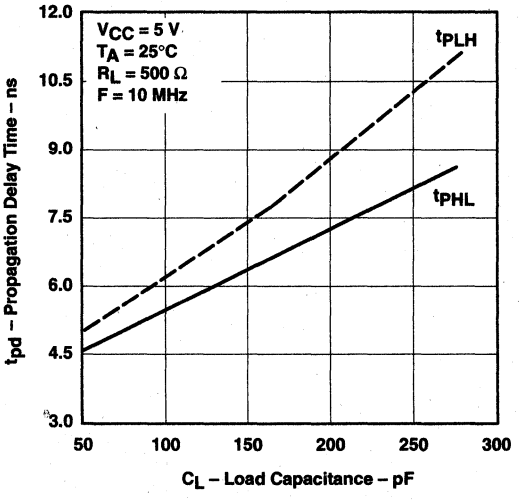
A to B
1 OUTPUT SWITCHING



A to B
4 OUTPUTS SWITCHING

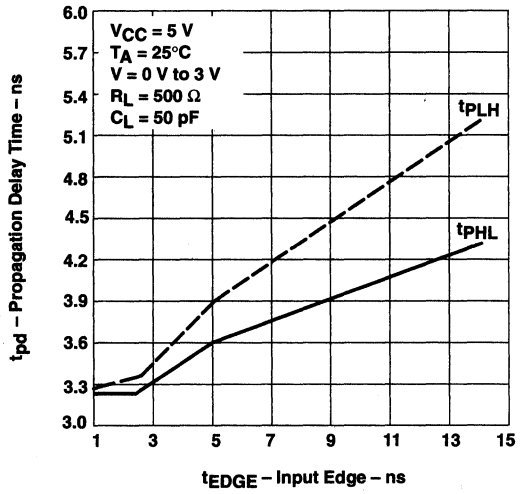


A to B
8 OUTPUTS SWITCHING

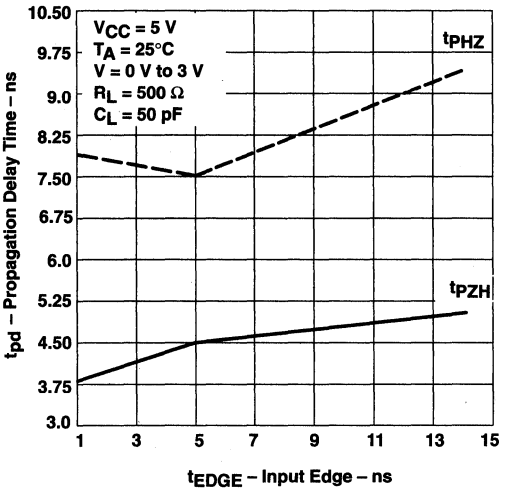


Propagation Delay Time vs Input Edge

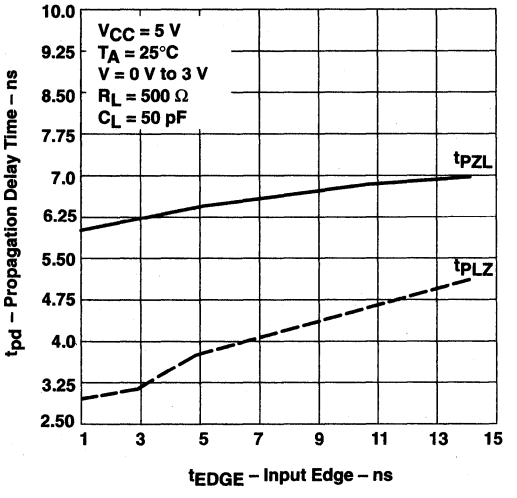
PROPAGATION DELAY TIME
vs
INPUT EDGE
A to B



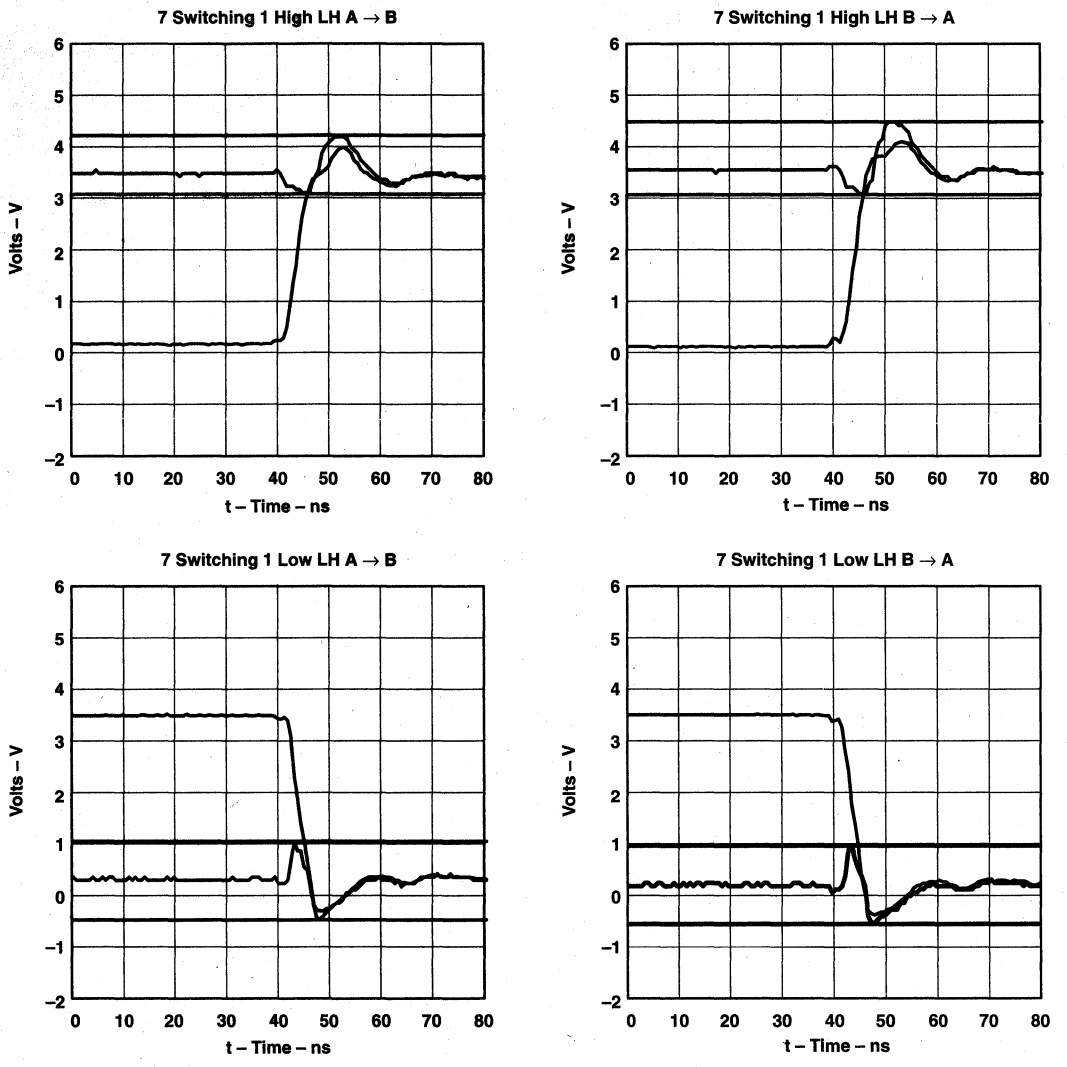
PROPAGATION DELAY TIME
vs
INPUT EDGE
A to B



PROPAGATION DELAY TIME
vs
INPUT EDGE
A to B



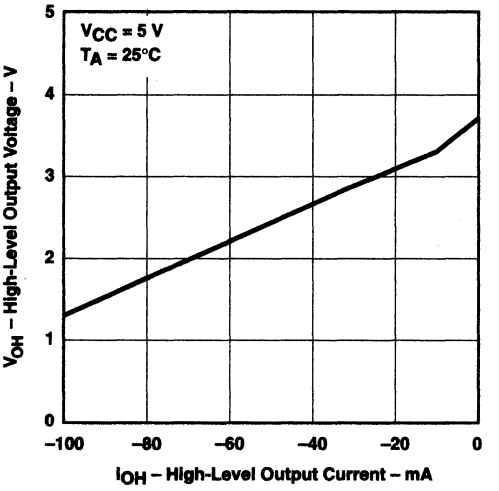
V_{OHV} and V_{OLP}



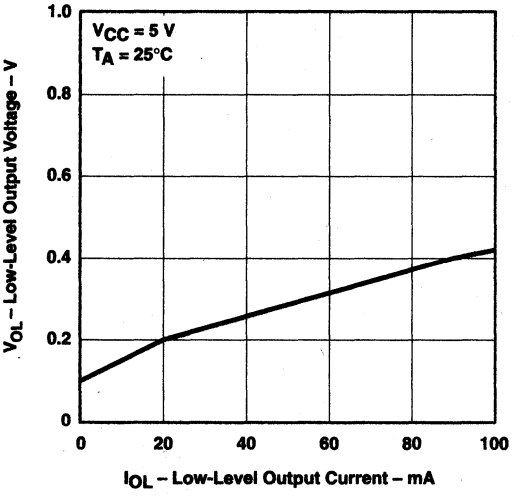
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

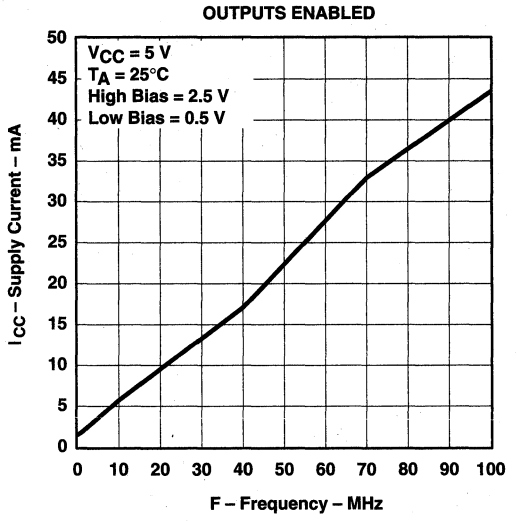
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

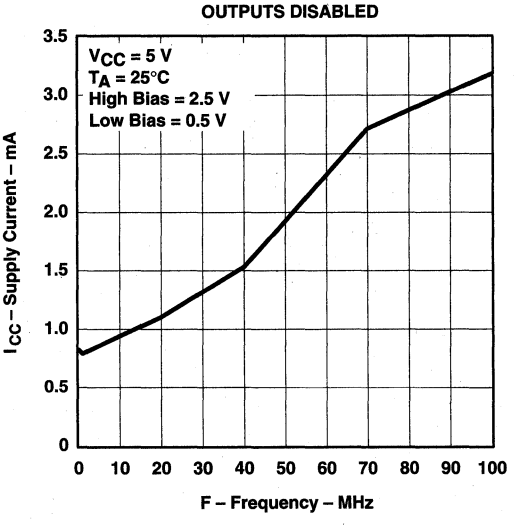


LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT



Supply Current vs Frequency



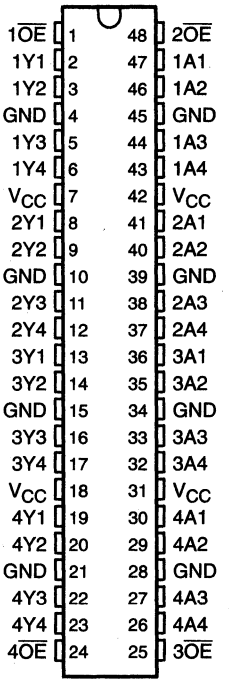


APPENDIX B
SN54ABT16244, SN74ABT16244A

B

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16244 . . . WD PACKAGE
SN74ABT16244A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The SN54ABT16244 and SN74ABT16244A are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16244A is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

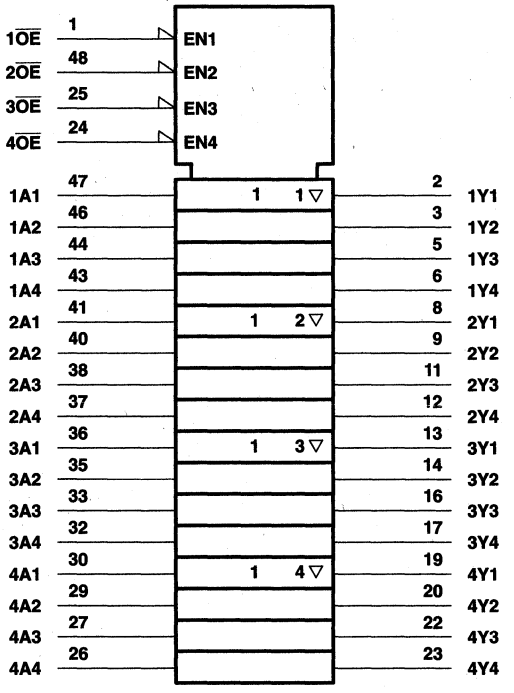
The SN54ABT16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16244A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

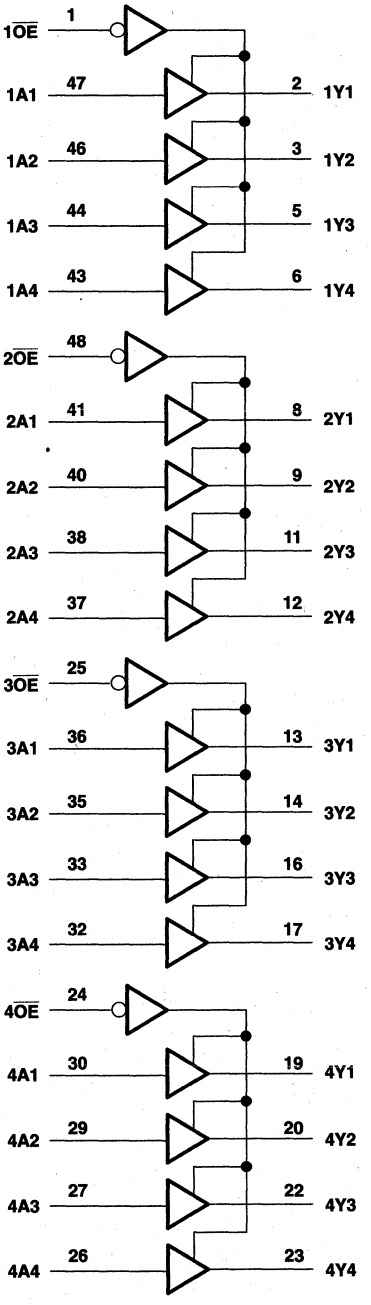
Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16244 ..... 96 mA
SN74ABT16244A ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.8 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16244		SN74ABT16244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

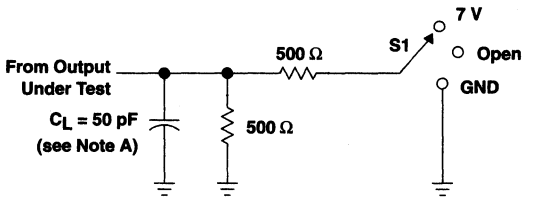
PARAMETER	TEST CONDITIONS			T_A = 25°C†			SN54ABT16244		SN74ABT16244A		UNIT
				MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2§					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55§				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				10¶		10		10¶	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–10¶		–10		–10¶	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100		±100		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O#	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			3		2		3	mA
			Outputs low			32		32		32	
			Outputs disabled			3		2		3	
ΔI_{CC}‖	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			0.05		1.5		0.05	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				0.05		1.5		0.05	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

† Characteristics for TA = 25°C apply to the SN74ABT16244A only.
‡ All typical values are at V_{CC} = 5 V.
§ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
¶ This data sheet limit may vary among suppliers.
# Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

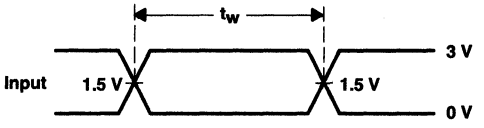
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C†			SN54ABT16244		SN74ABT16244A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.3	3.2	0.7	3.7	1	3.5	ns
t_{PHL}			1	2.6	3.7	0.5	4.3	1	4.1	
t_{PZH}	$\overline{OE}$	Y	1	3	3.8	0.7	5	1	4.8	ns
t_{PZL}			1	3.2	4	0.9	5	1	4.8	
t_{PHZ}	$\overline{OE}$	Y	1	3.6	4.4	1	5	1	4.8	ns
t_{PLZ}			1	2.9	3.7	1	4.3	1	4.1	

PARAMETER MEASUREMENT INFORMATION

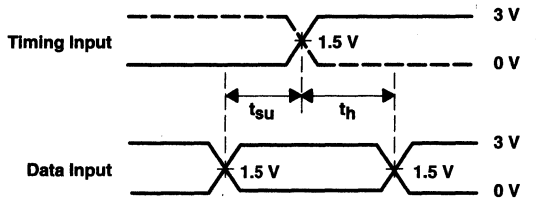


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

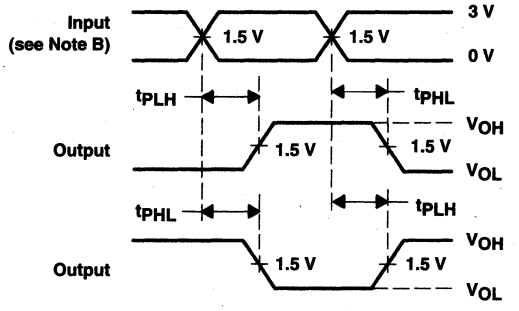
LOAD CIRCUIT FOR OUTPUTS



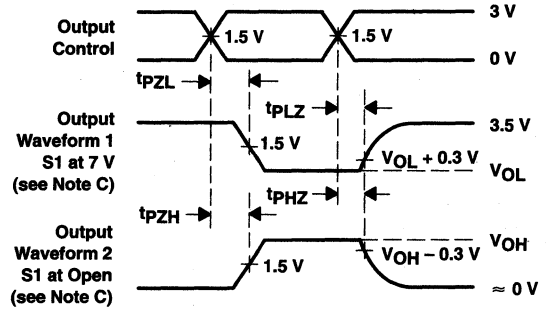
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



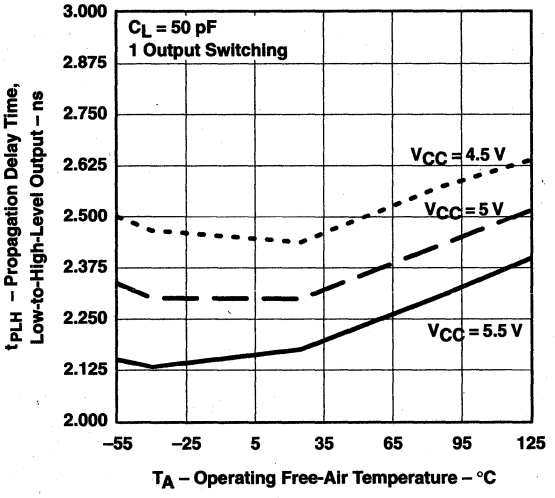
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

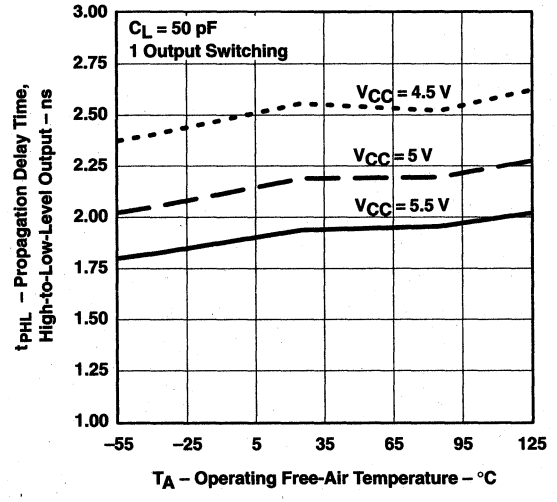
Figure 1. Load Circuit and Voltage Waveforms

Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A to Y

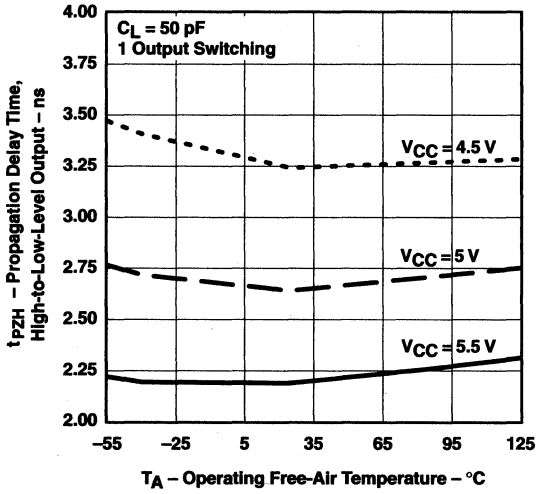


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A to Y

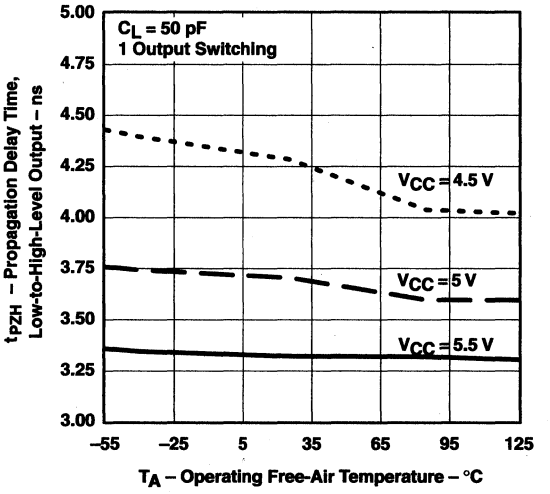


Propagation Delay Time vs Temperature

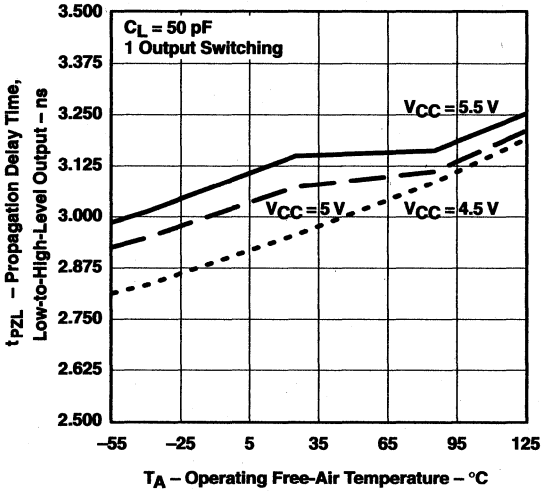
PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ to Y



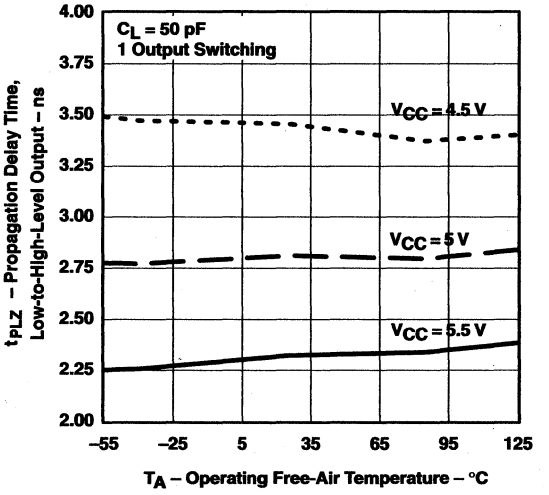
PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ toY



PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ to Y

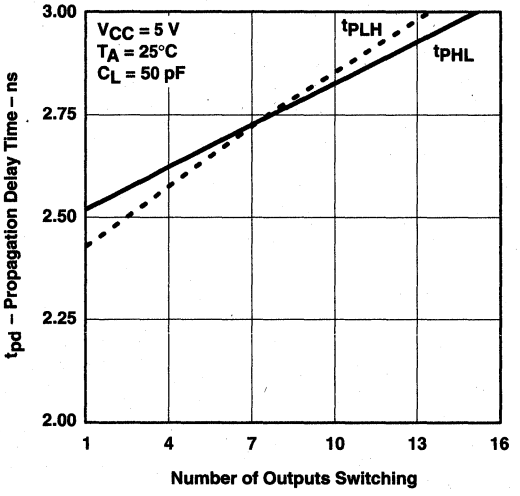


PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ to Y

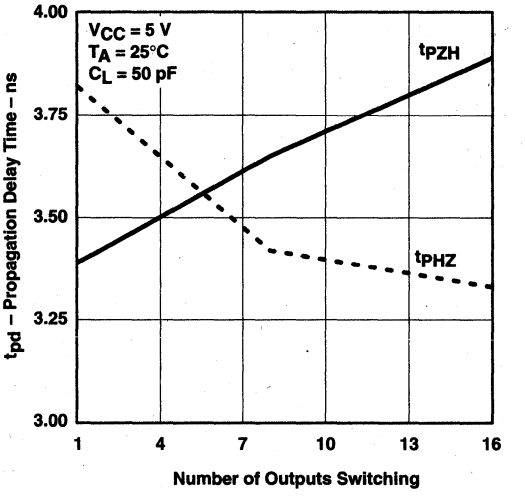


Propagation Delay Time vs Number of Outputs Switching

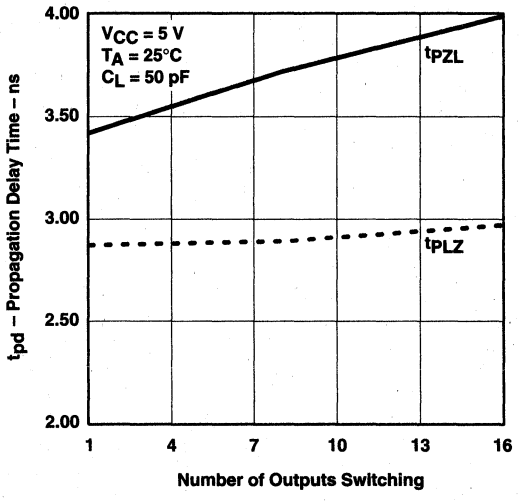
PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A to Y



PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
$\overline{OE}$ to Y

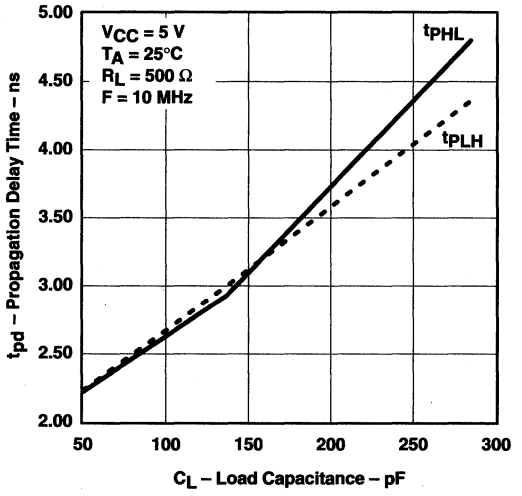


PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
$\overline{OE}$ to Y

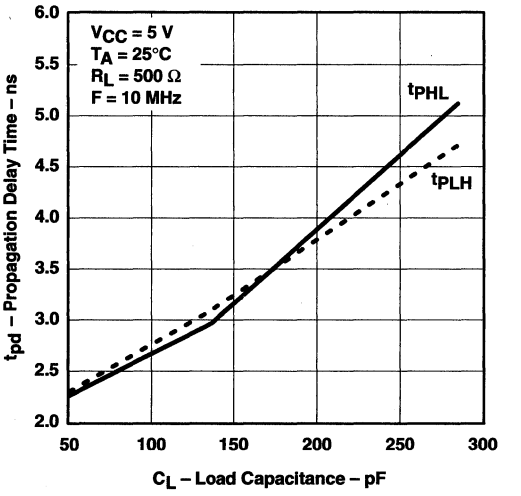


Propagation Delay Time vs Load Capacitance

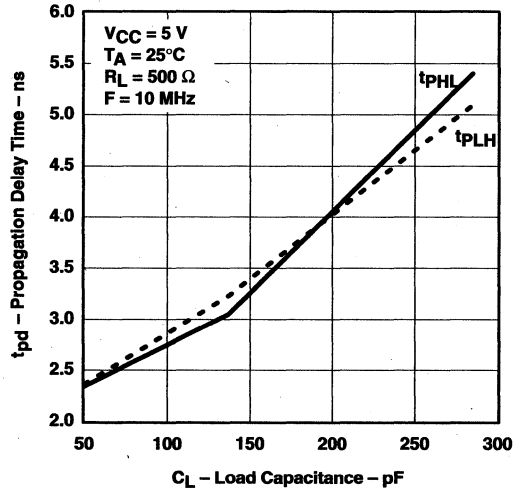
A to Y
1 OUTPUT SWITCHING



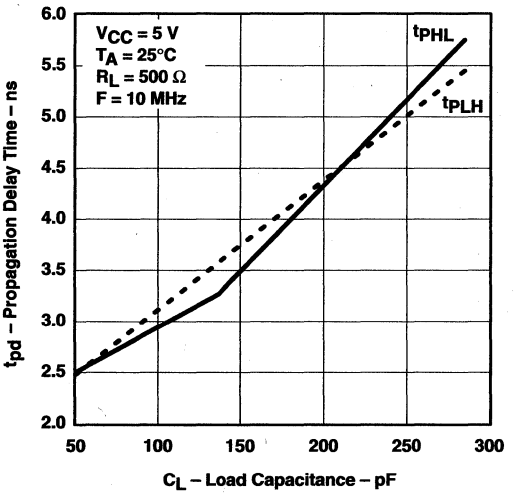
A to Y
4 OUTPUTS SWITCHING



A to Y
8 OUTPUTS SWITCHING

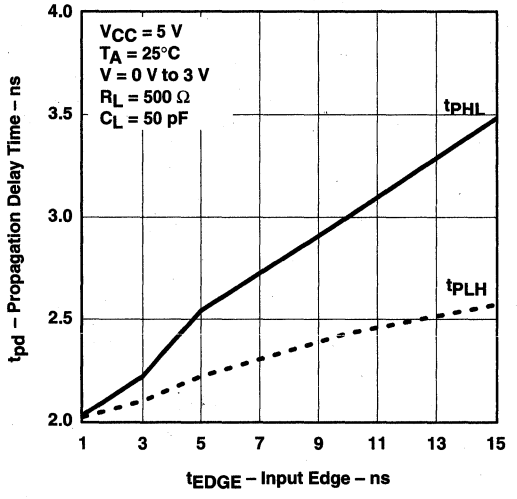


A to Y
16 OUTPUTS SWITCHING

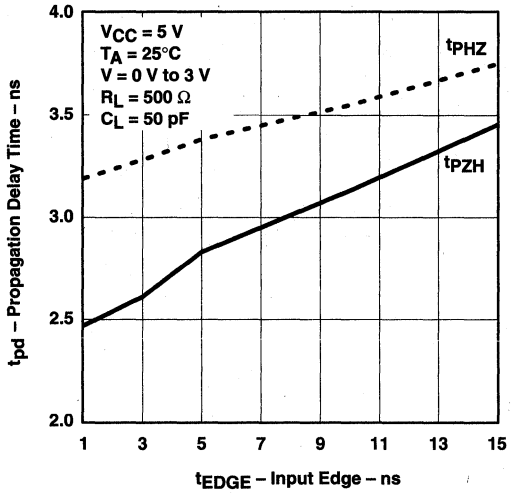


Propagation Delay Time vs Input Edge

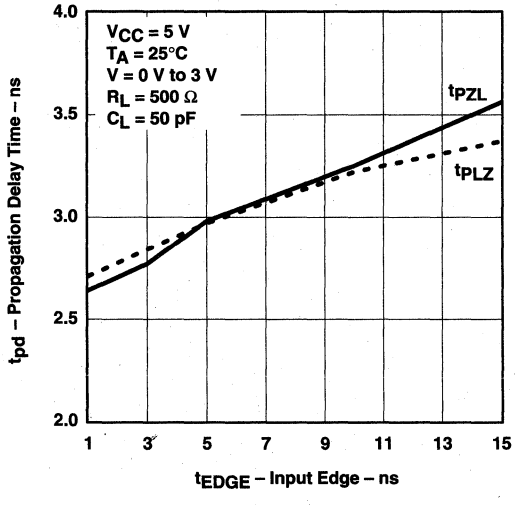
PROPAGATION DELAY TIME
vs
INPUT EDGE
A to Y



PROPAGATION DELAY TIME
vs
INPUT EDGE
$\overline{OE}$ to Y

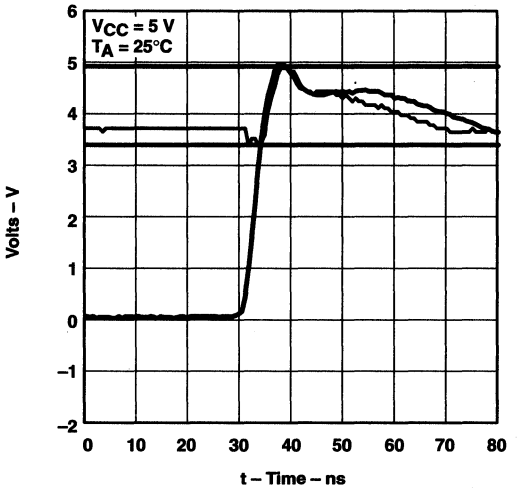


PROPAGATION DELAY TIME
vs
INPUT EDGE
$\overline{OE}$ to Y

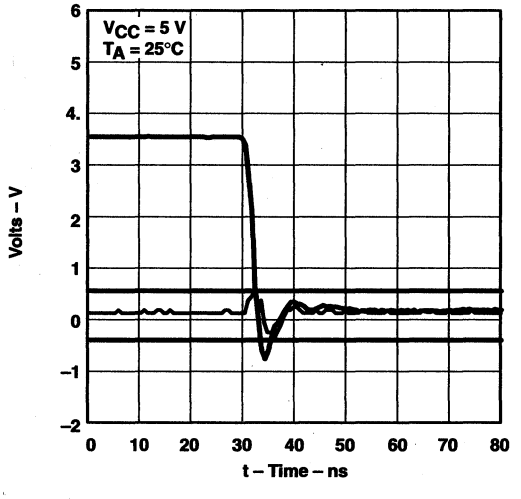


V_{OHV} and V_{OLP}

15 Switching 1 High LH A → Y



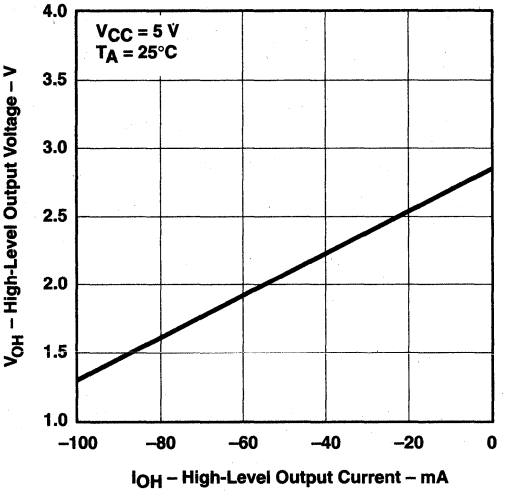
15 Switching 1 Low HL A → Y



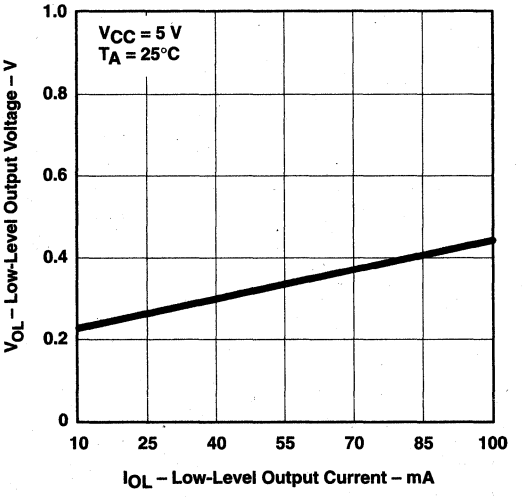
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

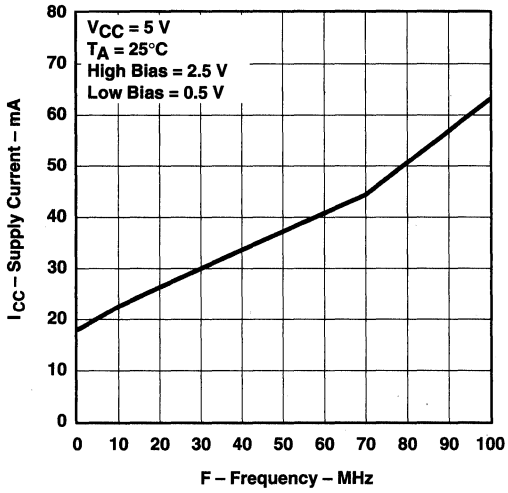


LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

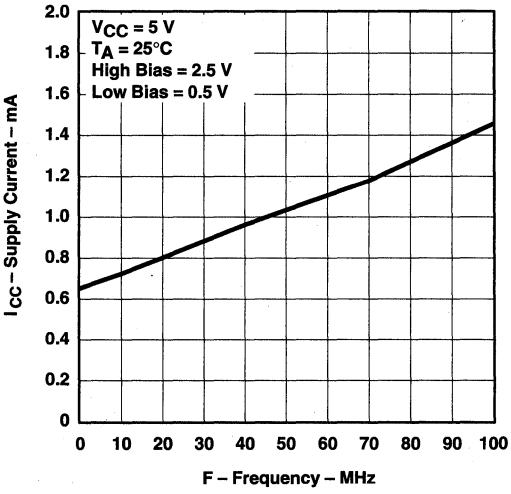


Supply Current vs Frequency

OUTPUTS ENABLED



OUTPUTS DISABLED

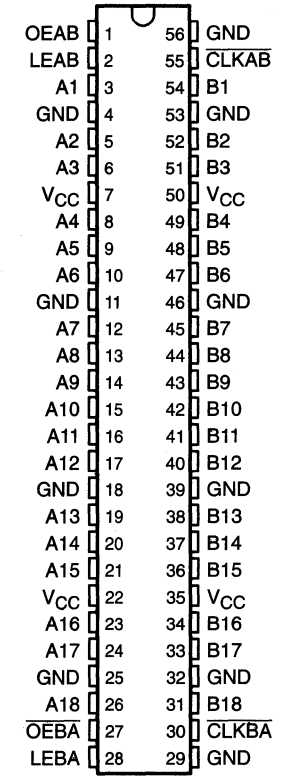


APPENDIX C
'ABT16500B

C

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16500B . . . WD PACKAGE
SN74ABT16500B . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16500B is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16500B is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT16500B is characterized for operation from −40°C to 85°C.

Widebus, EPIC-IIB, and UBT are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

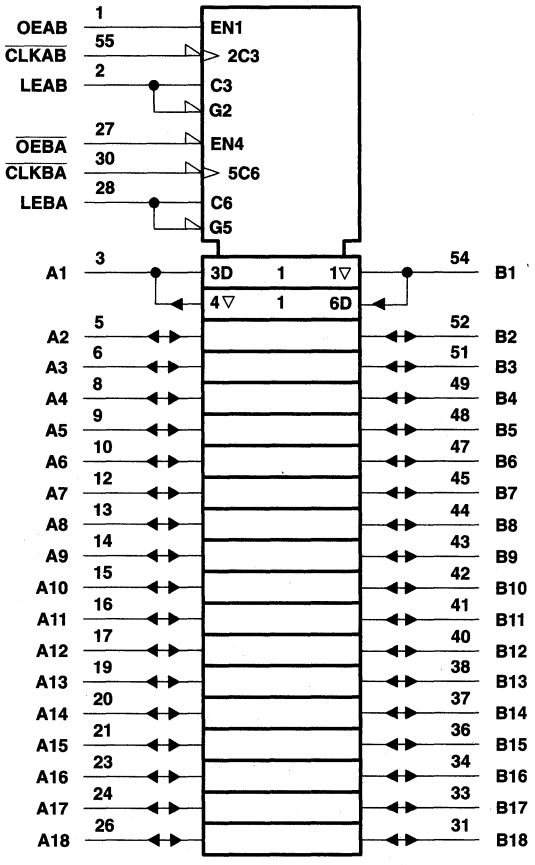
INPUTS				OUTPUT
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.

‡ Output level before the indicated steady-state input conditions were established.

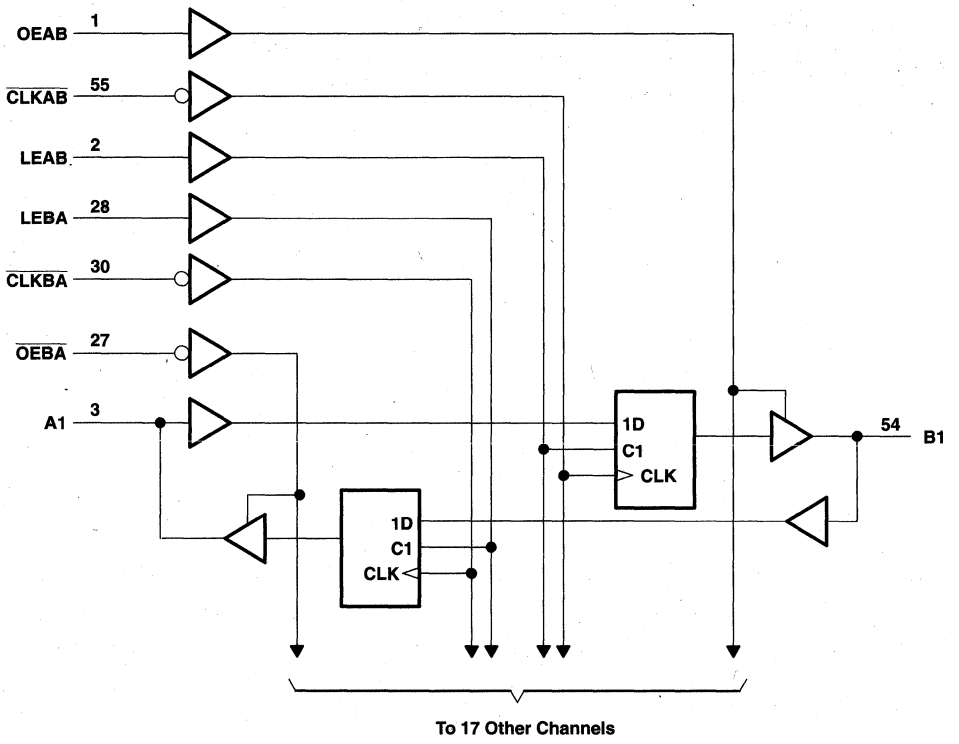
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16500B ..... 96 mA
SN74ABT16500B ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT16500B		SN74ABT16500B		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±20		±20		±20	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					10		10		10	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					−10		−10		−10	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		9						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

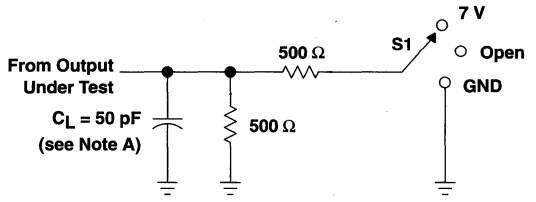
				SN54ABT16500B		SN74ABT16500B		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w†	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low		3		3		
t_{su}	Setup time	A before $\overline{CLKAB}$↓		3		3		ns
		B before $\overline{CLKBA}$↓		3		3		
		A before LEAB↓ or B before LEBA↓	$\overline{CLK}$ high	1		1		
			$\overline{CLK}$ low	2.5		2.5		
t_h	Hold time	A after $\overline{CLKAB}$↓ or B after $\overline{CLKBA}$↓		0		0		ns
		A after LEAB↓ or B after LEBA↓		2		2		

† This parameter is specified by design but not tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

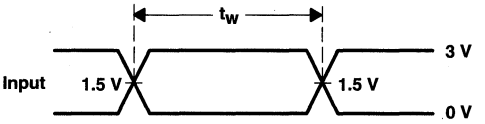
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150		MHz
t_{PLH}	A or B	B or A	1	2.5	3.6	1	4.2	1	4	ns
t_{PHL}			1	3.2	4.5	1	5.1	1	4.9	
t_{PLH}	LEAB or LEBA	B or A	1	3.2	4.5	1	5.6	1	5	ns
t_{PHL}			1	3.4	4.5	1	5.4	1	5	
t_{PLH}	$\overline{CLKAB}$ or $\overline{CLKBA}$	B or A	1	3.5	4.7	1	5.4	1	5.3	ns
t_{PHL}			1	3.5	4.7		5.4	1	5.3	
t_{PZH}	OEAB or $\overline{OEBA}$	B or A	1	3.4	4.6	1	5.3	1	5.1	ns
t_{PZL}			1.5	3.8	4.7	1.5	5.6	1.5	5.4	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A	1.5	4.5	5.7	1.5	6.9	1.5	6.5	ns
t_{PLZ}			1.4	3.4	4.7	1.4	5.8	1.4	5.4	

PARAMETER MEASUREMENT INFORMATION

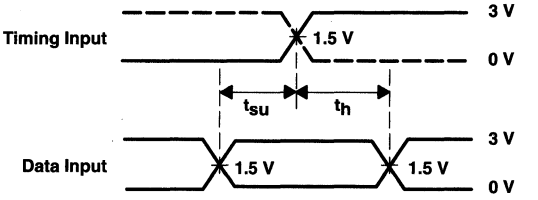


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

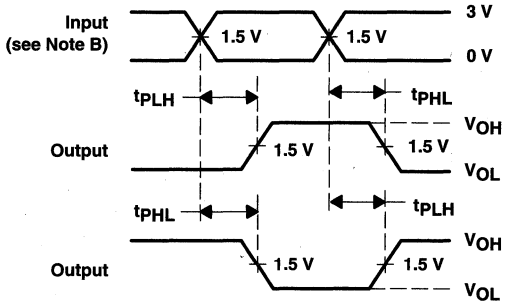
LOAD CIRCUIT FOR OUTPUTS



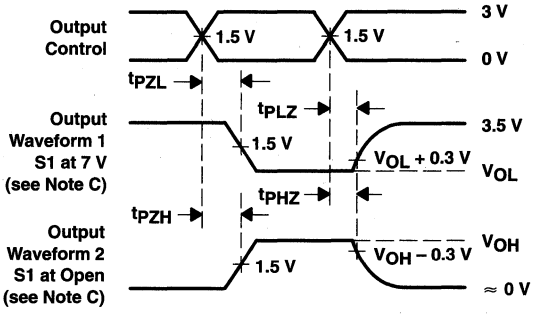
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



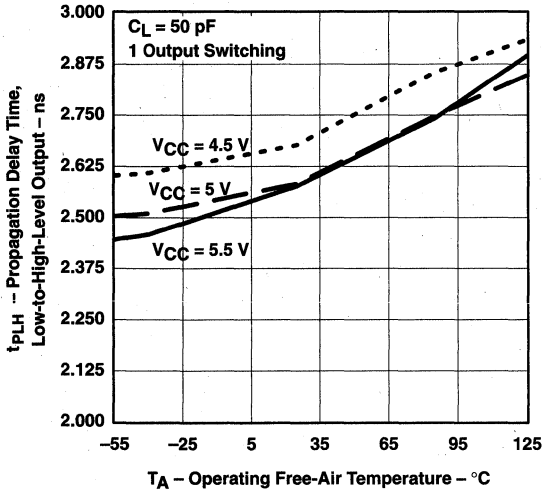
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

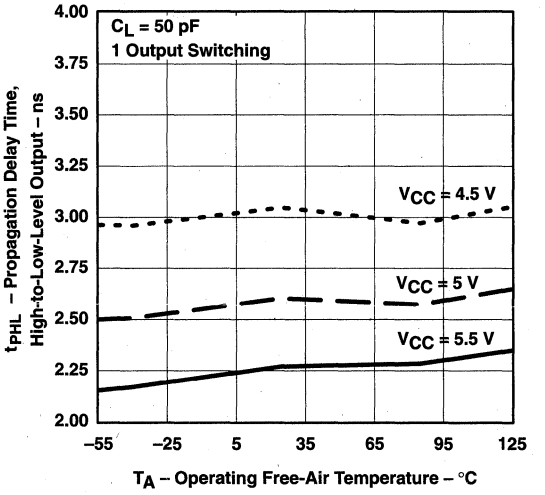
Figure 1. Load Circuit and Voltage Waveforms

Propagation Delay Time vs Temperature

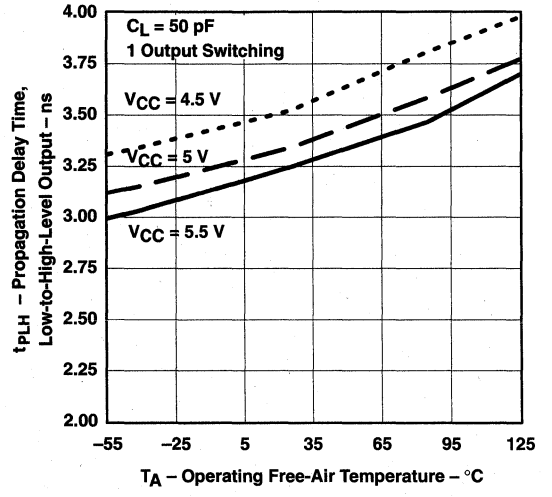
PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A to B



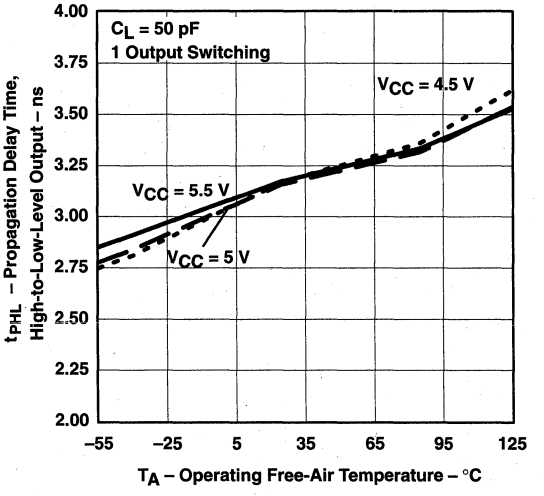
PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A to B



PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
LEAB to B

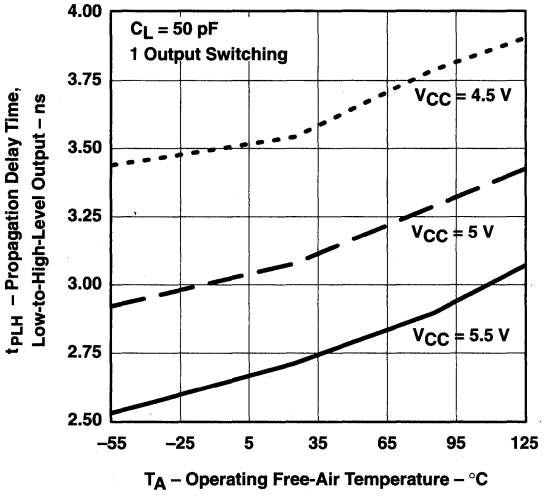


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
LEAB to B

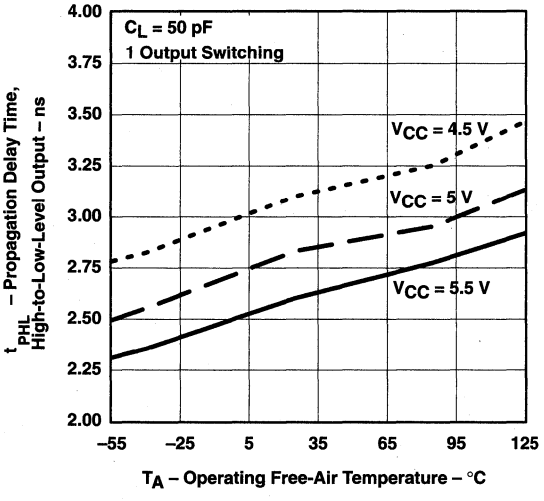


Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{CLKAB}$ to B

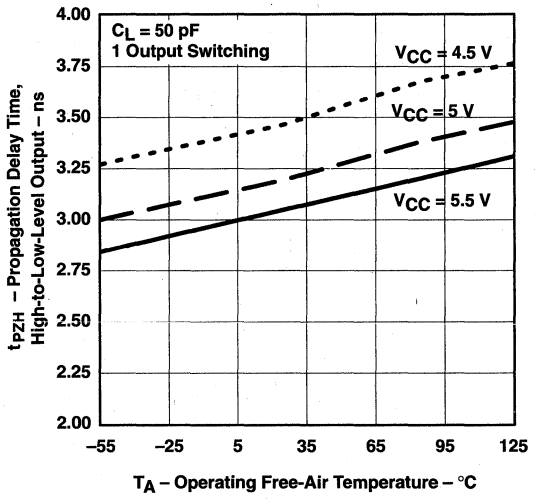


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{CLKAB}$ to B

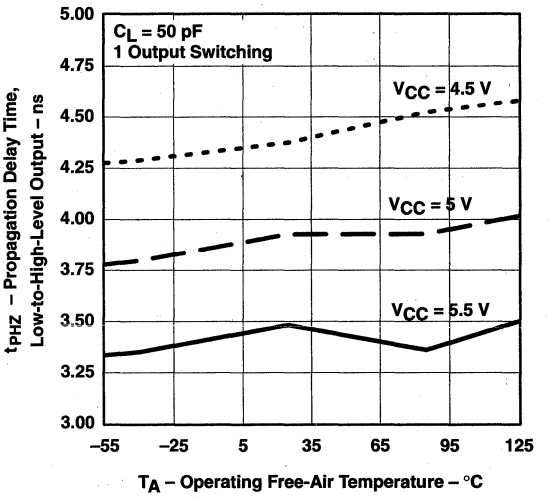


Propagation Delay Time vs Temperature

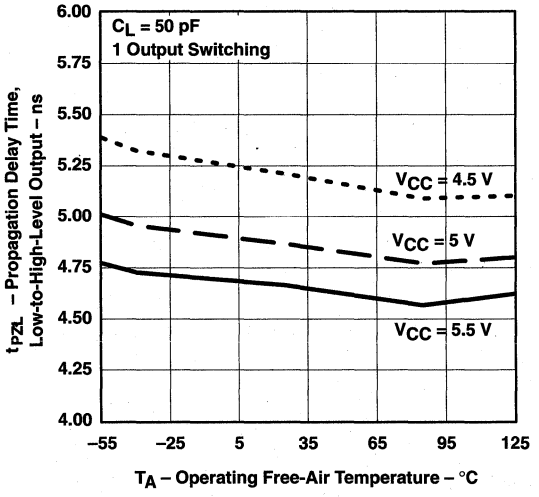
PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB to B



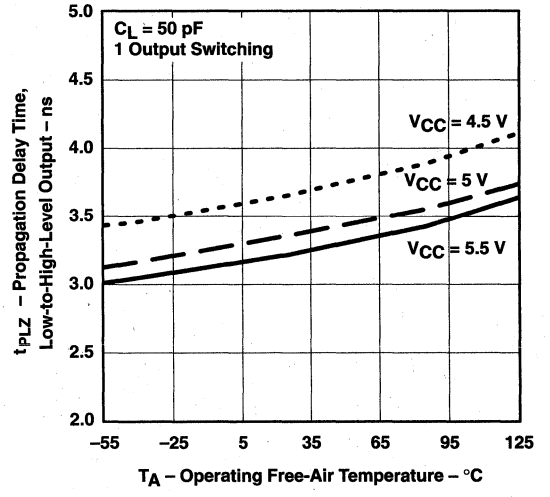
PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB to B



PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB to B

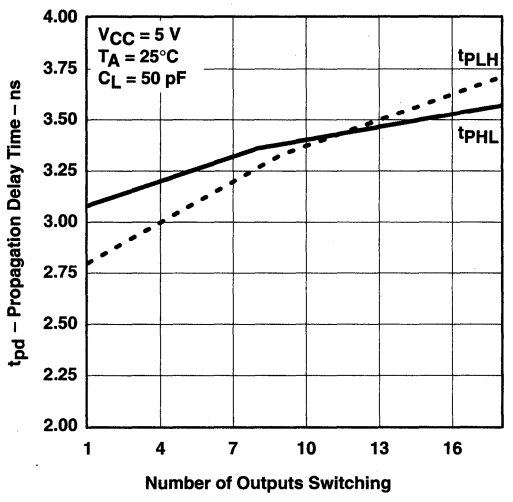


PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB to B

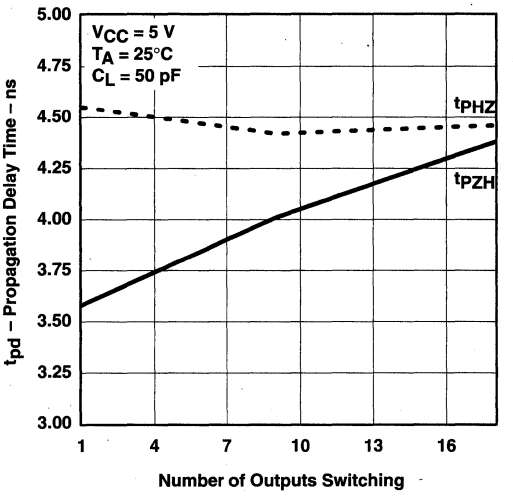


Propagation Delay Time vs Number of Outputs Switching

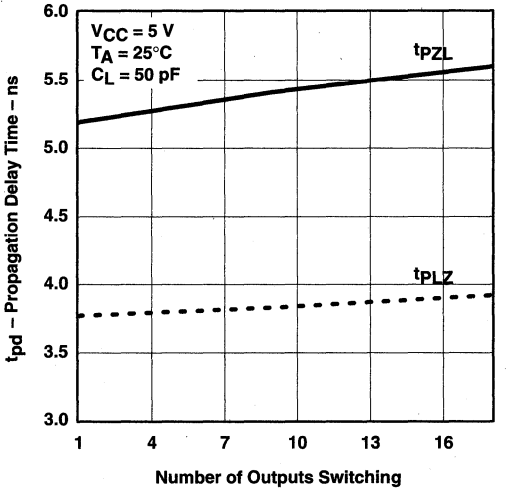
PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A to B



PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
OEAB to B

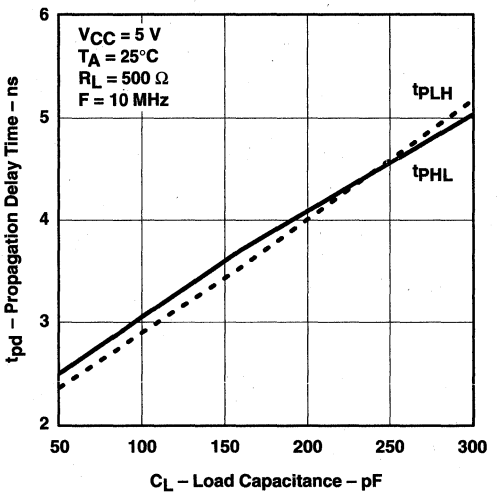


PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
OEAB to B

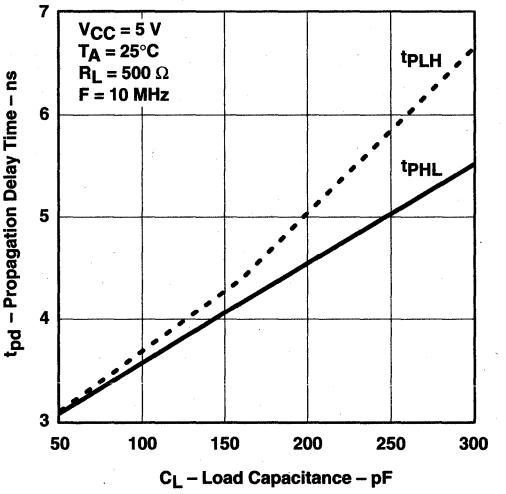


Propagation Delay Time vs Load Capacitance

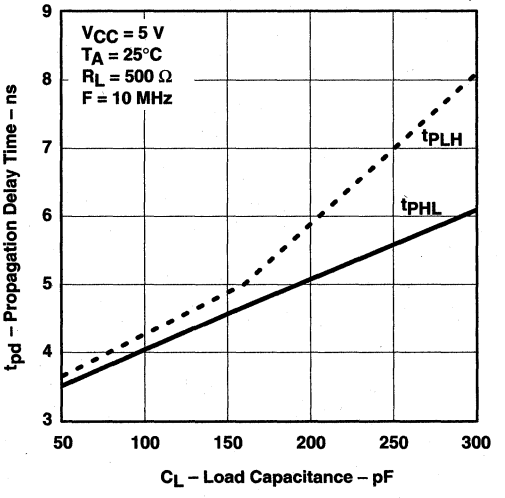
A to B
1 OUTPUT SWITCHING



A to B
9 OUTPUTS SWITCHING

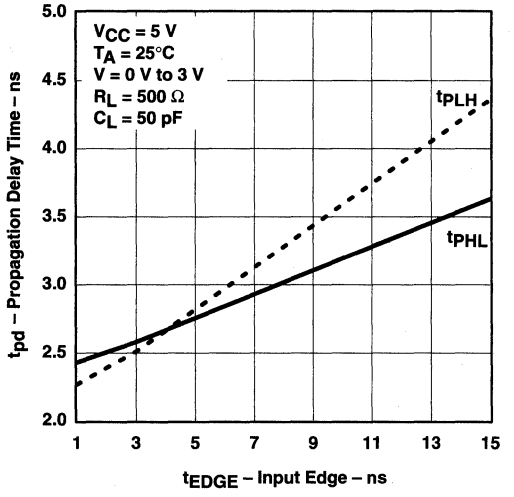


A to B
18 OUTPUTS SWITCHING

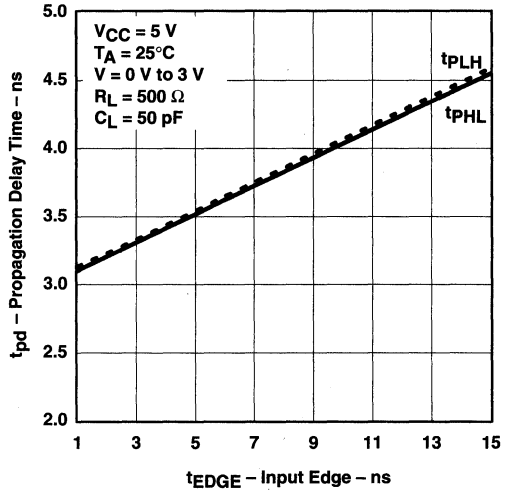


Propagation Delay Time vs Input Edge

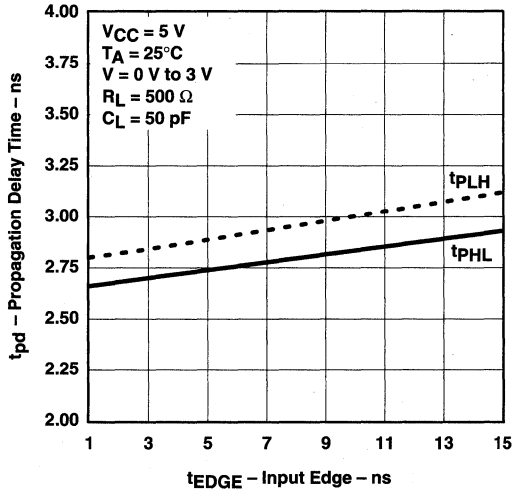
PROPAGATION DELAY TIME
vs
INPUT EDGE
A to B



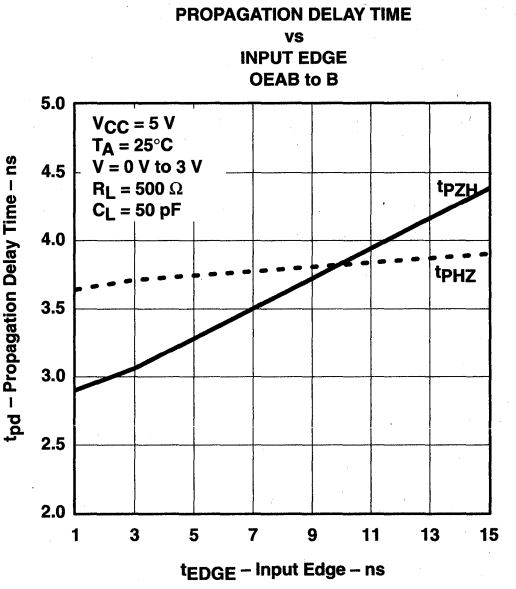
PROPAGATION DELAY TIME
vs
INPUT EDGE
LEAB to B

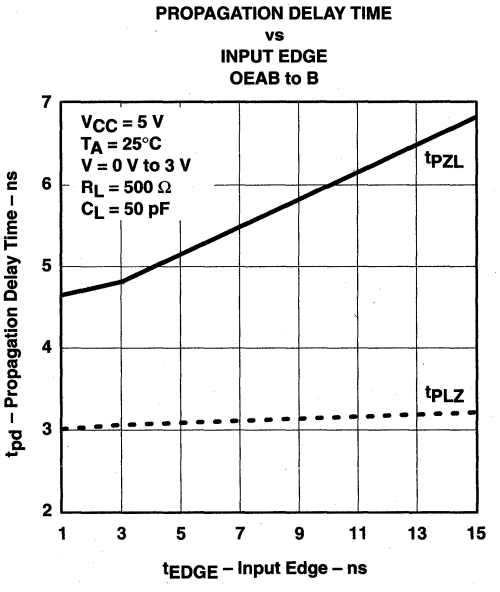


PROPAGATION DELAY TIME
vs
INPUT EDGE
CLKAB to B

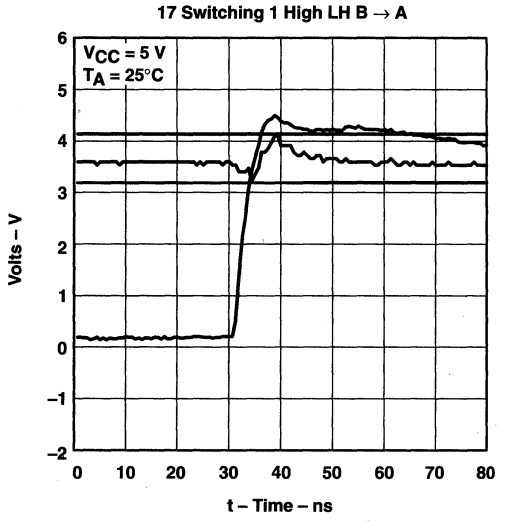


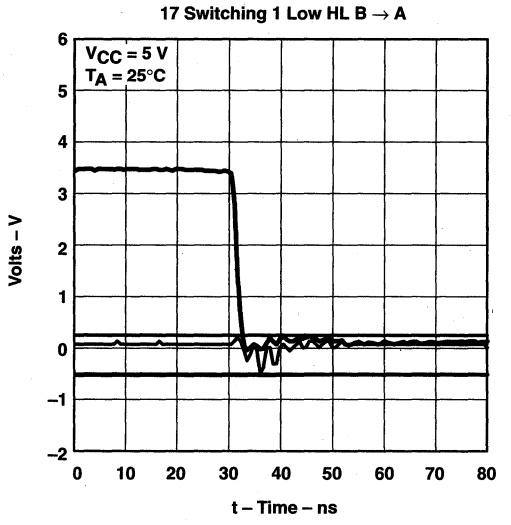
Propagation Delay Time vs Input Edge





V_{OHV} and V_{OLP}



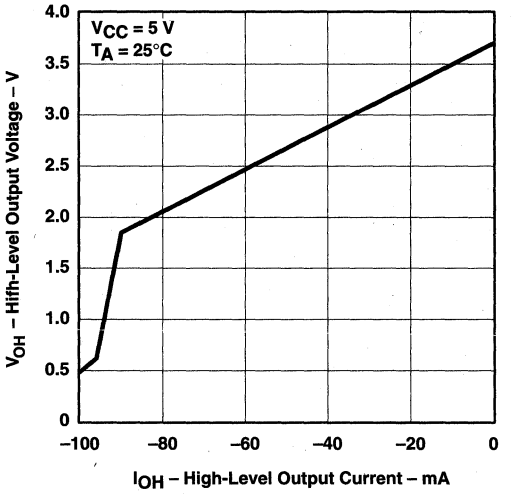


V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.

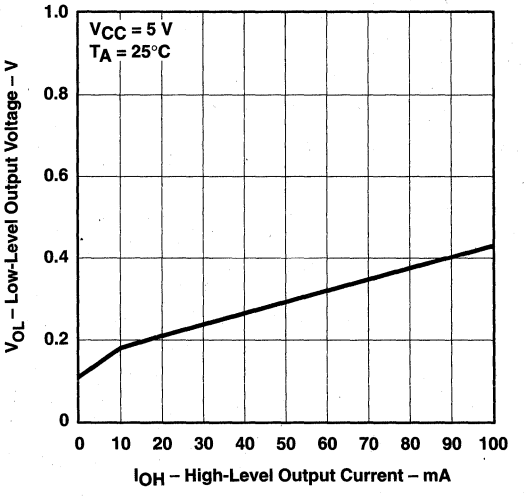
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

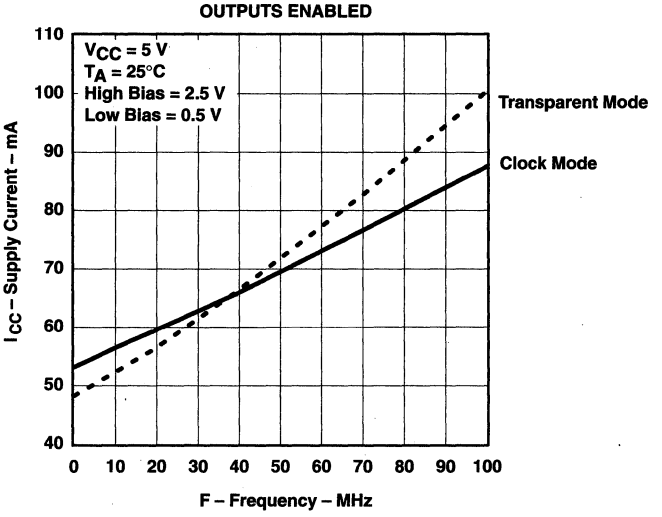
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

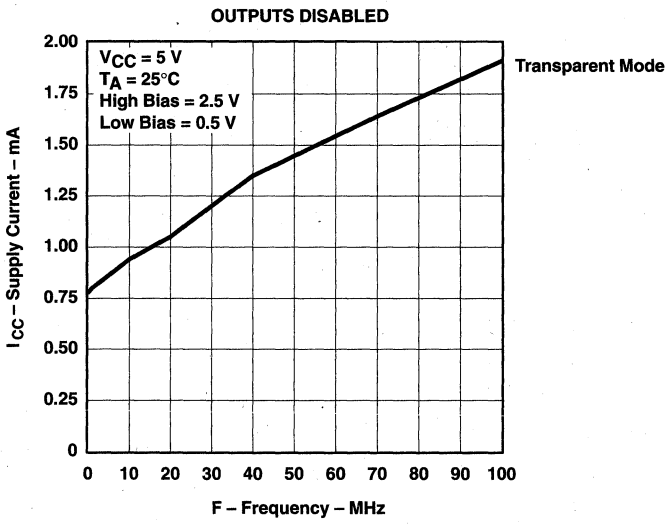


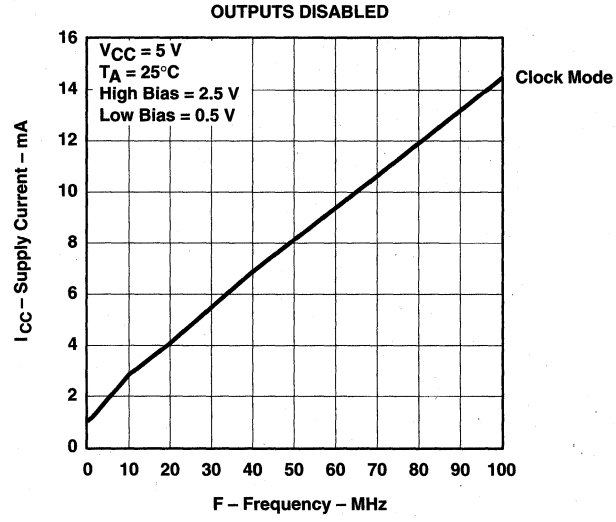
Supply Current vs Frequency



NOTE: Characteristics for latch mode are similar to those when in clock mode.

Supply Current vs Frequency





NOTE: Characteristics for latch mode are similar to those when in clock mode.

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: **SN** **74ABT16500B** **DL** **R**

Prefix

Blank = (Standard product)
SN = Standard prefix
SNJ = Mil-Std-883, Class B

Unique Circuit Description

MUST CONTAIN FIVE TO NINE CHARACTERS
(from individual data sheet)

Package

MUST CONTAIN ONE TO THREE LETTERS

D, DW	=	plastic small-outline package (SOIC)
DB	=	plastic shrink small-outline package (SSOP)
DGG	=	plastic Shrink Widebus™ package
DL	=	plastic small-outline Widebus™ package
FK	=	ceramic chip carrier
HV	=	ceramic quad flat package
J, JT	=	ceramic dual-in-line package
N, NT	=	plastic dual-in-line package (DIP)
PCA, PM, PN, PZ	=	plastic thin quad flat package (TQFP)
PW	=	plastic thin shrink small-outline package (TSSOP)
RC	=	plastic quad flat package
W	=	ceramic flat package
WD	=	ceramic Widebus™ flat package

Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

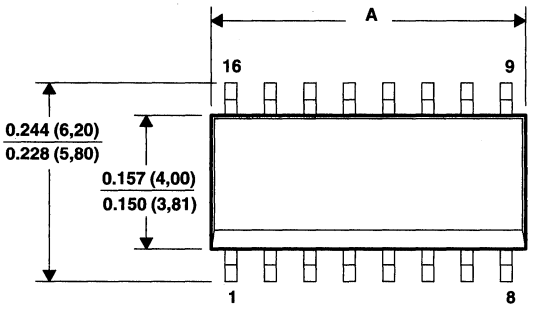
MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for DB and PW packages)
R = Standard tape and reel (required for DGG; optional for D, DW, and DL packages)

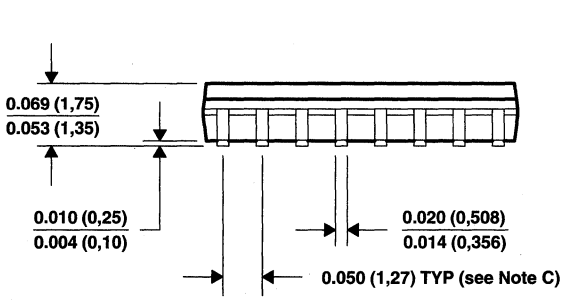
D/R-PDSO-G**

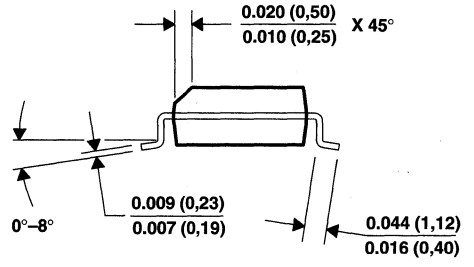
PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE

16-PIN SHOWN



DIM \ PINS**	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)





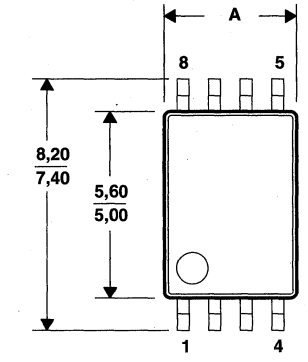
4040047/A–07/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).
F. Maximum deviation from coplanarity is 0.004 (0,10).

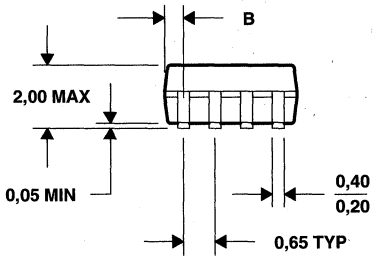
DB/R-PDSO-G**

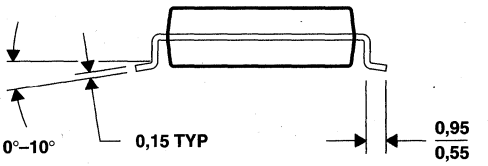
PLASTIC SMALL-OUTLINE PACKAGE

8-PIN SHOWN



DIM \ PINS**	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30
B MAX	0,68	1,30	0,98	0,83	0,68	1,03	0,70	0,60

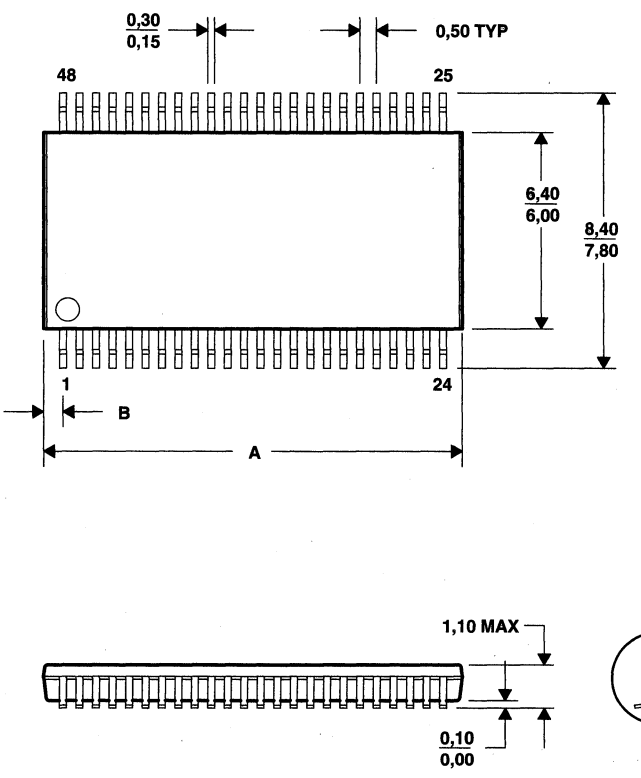




4040065/A–07/93

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

DGG/R-PDSO-G** **300-MIL THIN SHRINK SMALL-OUTLINE PACKAGE**



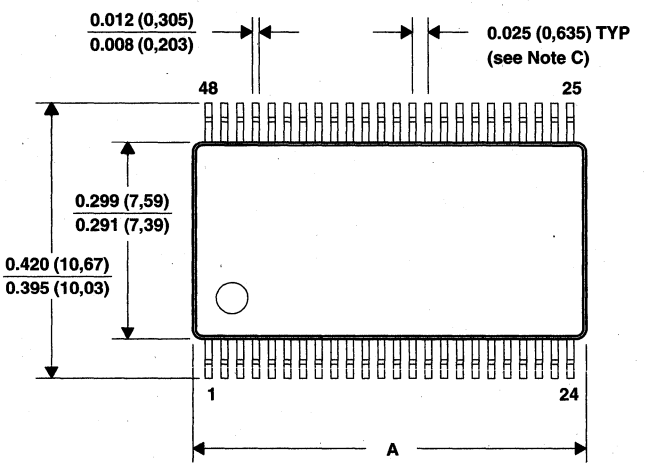
DIM \ PINS**	48	56
A MAX	12,80	14,30
A MIN	12,40	13,90
B MAX	0,65	0,40

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

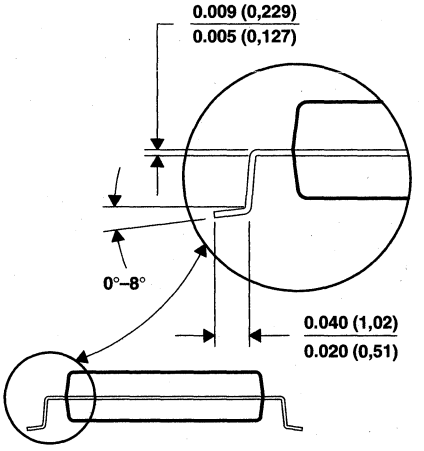
DL/R-PDSO-G**

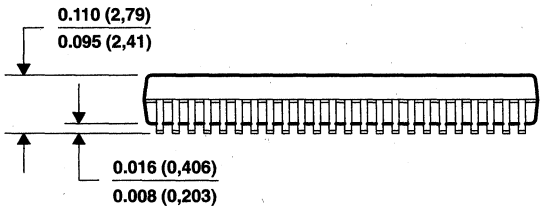
PLASTIC SHRINK SMALL-OUTLINE PACKAGE

48-PIN SHOWN



DIM \ PINS**	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)



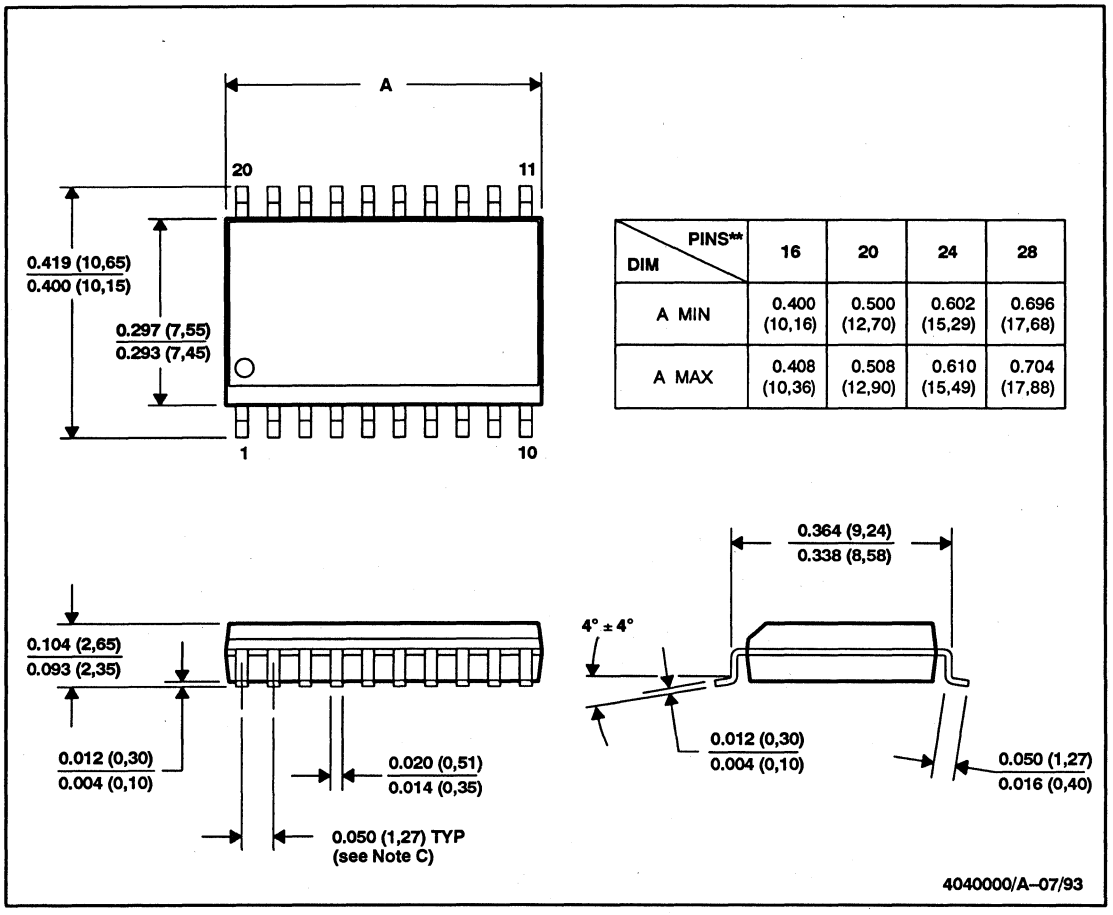


4040048/A–07/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.0035 (0,089) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash , protrusion or gate burr.
E. Mold flash or protrusion or gate burr shall not exceed 0.015 (0,381).
F. Lead tips coplanar within 0.004 (0,102).
G. Lead length measured from lead top to point 0.010 (0,254) above seating plane.

DW/R-PDSO-G**
20-PIN SHOWN

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE



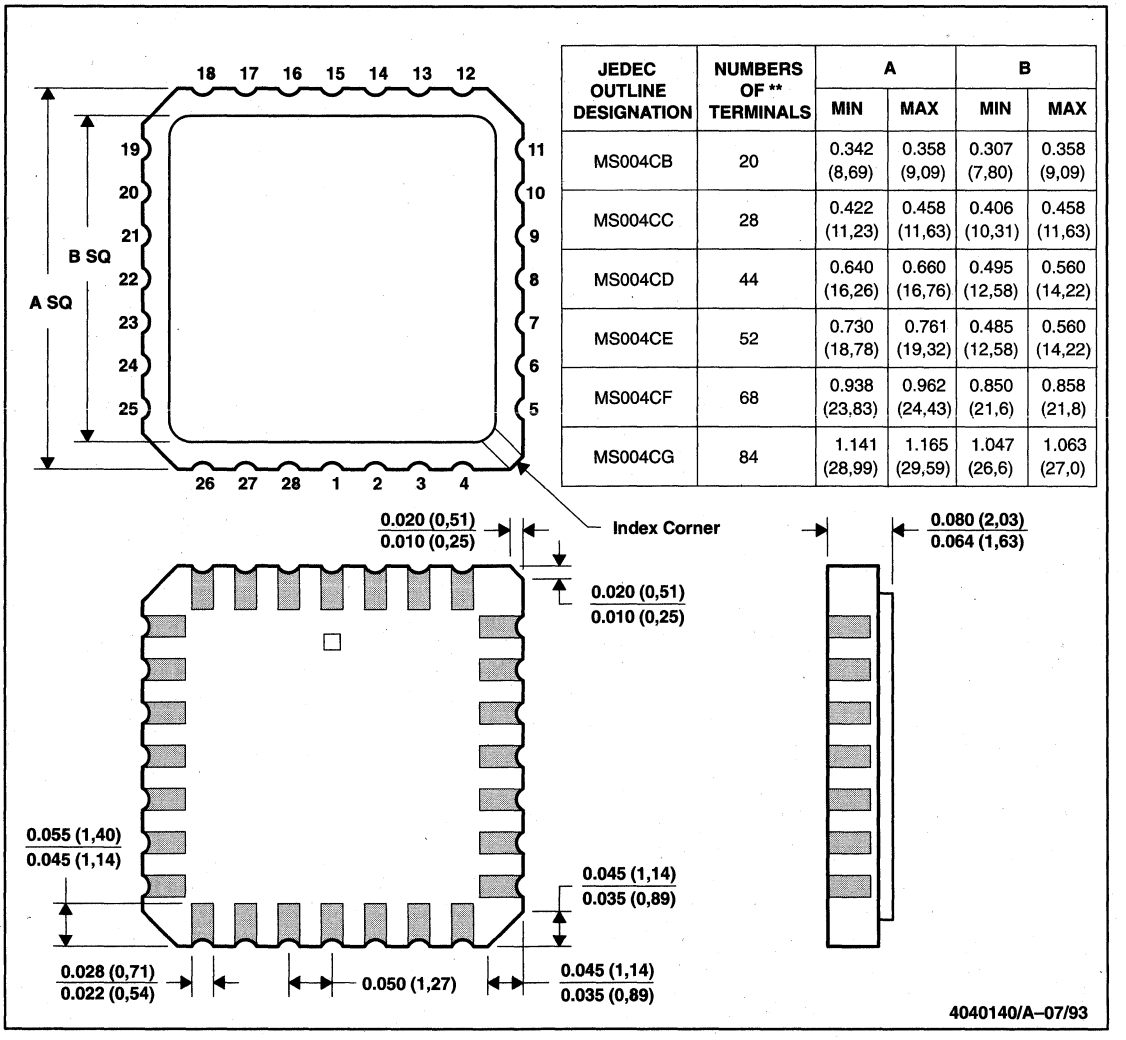
DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.602 (15,29)	0.696 (17,68)
A MAX	0.408 (10,36)	0.508 (12,90)	0.610 (15,49)	0.704 (17,88)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.10 (0,25) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold flash or protrusion shall not exceed 0.006 (0,15).
F. Lead tips coplanar within ±0.004 (±0,10) exclusive of solder.

FK/S-CQCC-N**

28-TERMINAL SHOWN

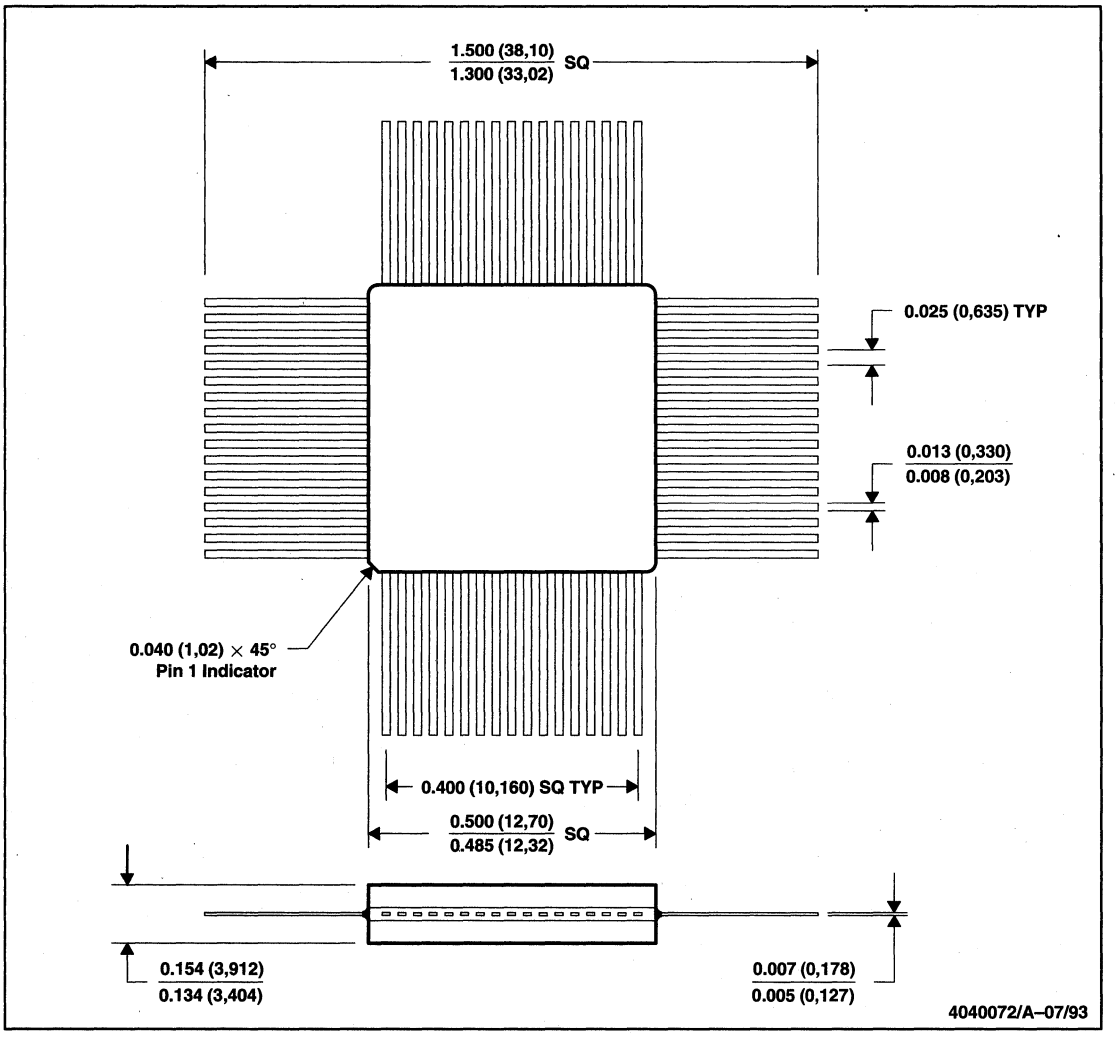
CERAMIC CHIP CARRIER



JEDEC OUTLINE DESIGNATION	NUMBERS OF ** TERMINALS	A		B	
		MIN	MAX	MIN	MAX
MS004CB	20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
MS004CC	28	0.422 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
MS004CD	44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
MS004CE	52	0.730 (18,78)	0.761 (19,32)	0.485 (12,58)	0.560 (14,22)
MS004CF	68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
MS004CG	84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Three-layer ceramic base with a metal lid and braze seal.
D. FK package terminal assignments conform to JEDEC Standards 1,2 and 11.
E. The packages are intended for surface mounting on solder lands on 0.050 (1,27) centers.

HV/S-GQFP–F68 **CERAMIC QUAD FLAT PACKAGE**

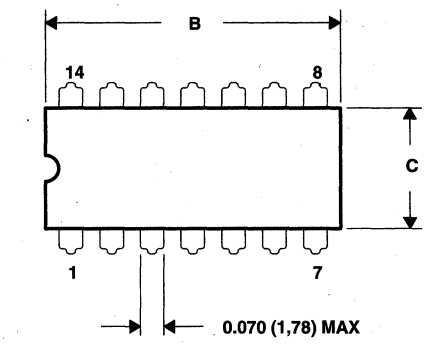


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

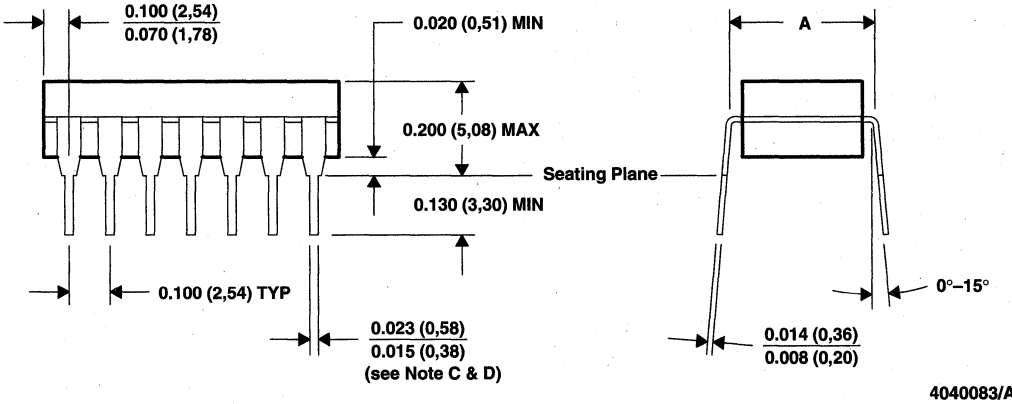
J/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

14-PIN SHOWN



DIM \ PINS**	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)	—
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	—



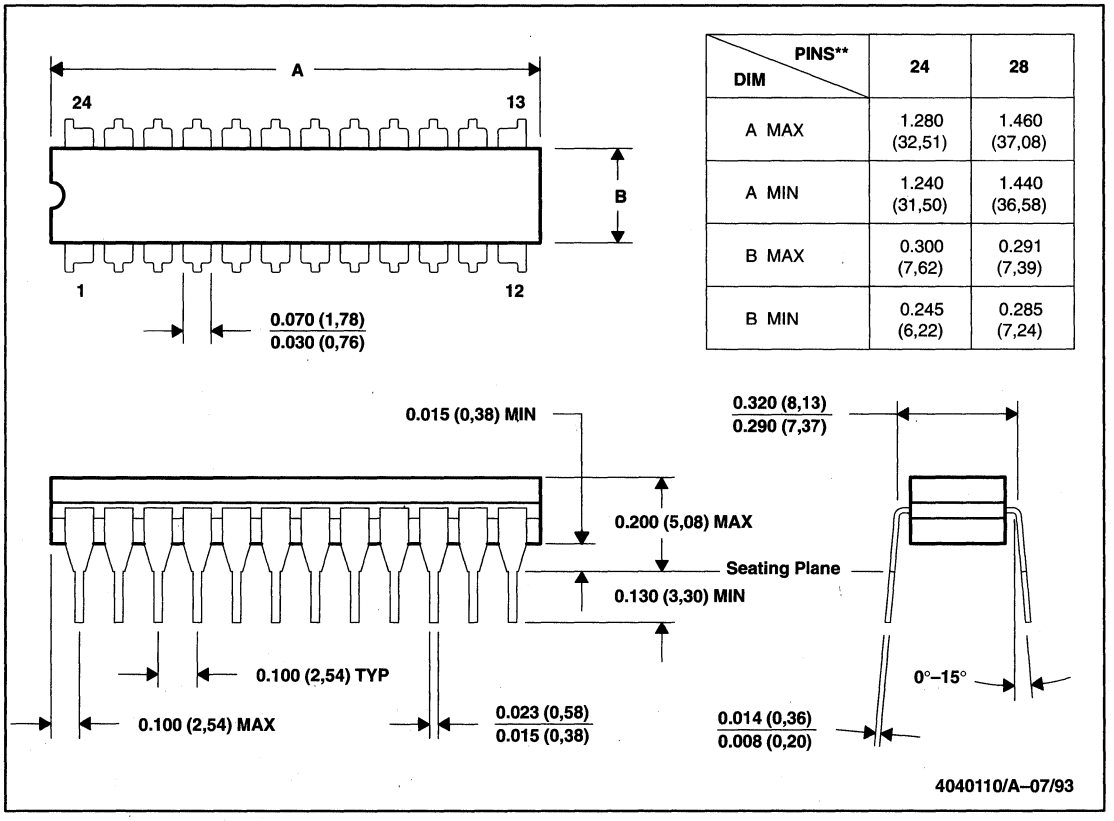
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This dimension does not apply for solder dipped leads.
D. For solder dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0.51) above seating plane.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

JT/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

24-PIN SHOWN



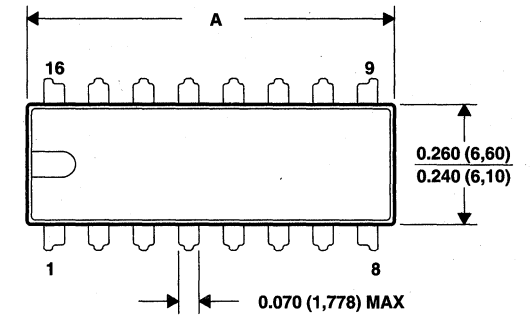
DIM \ PINS**	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is glass seal.

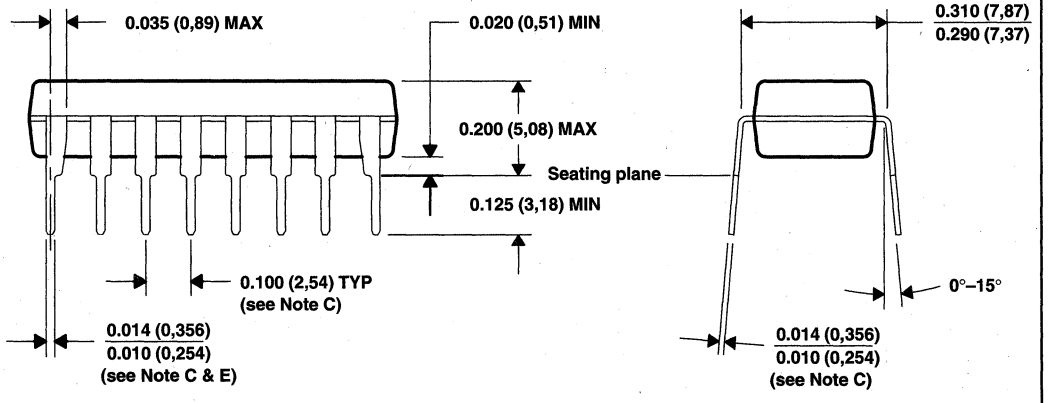
N/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

16-PIN SHOWN



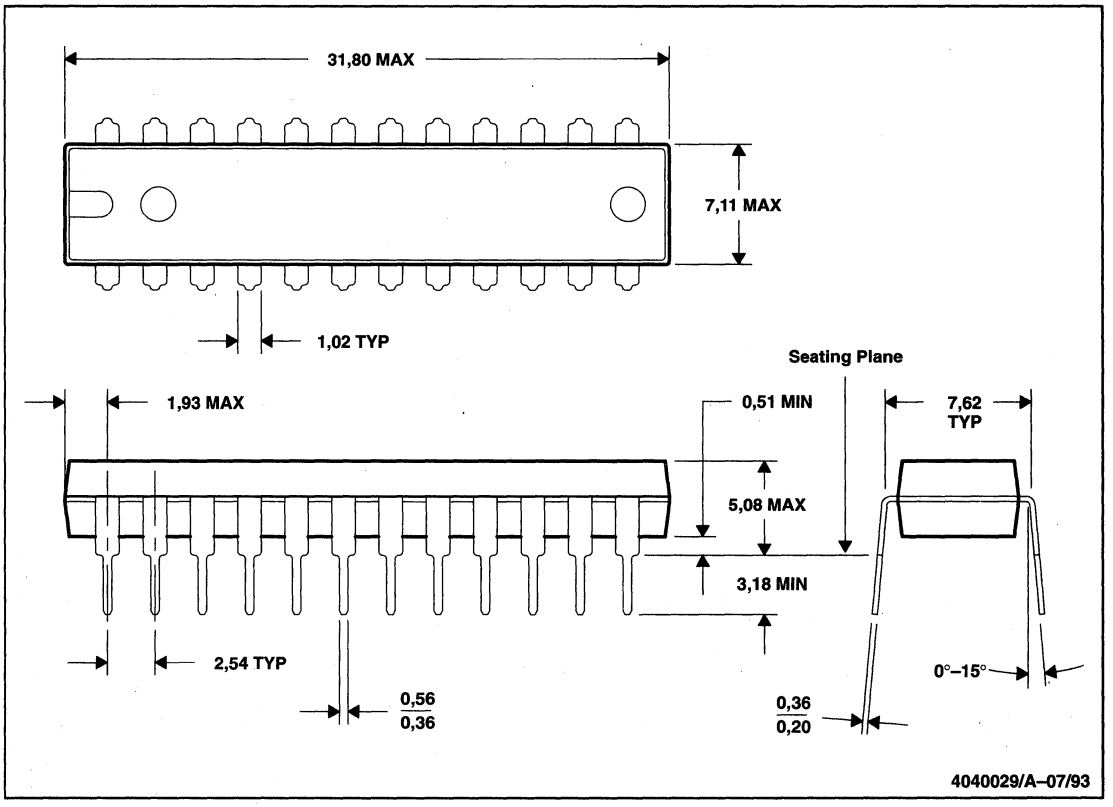
DIM \ PINS**	14	16	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.940 (23,88)



4040049/A–07/93

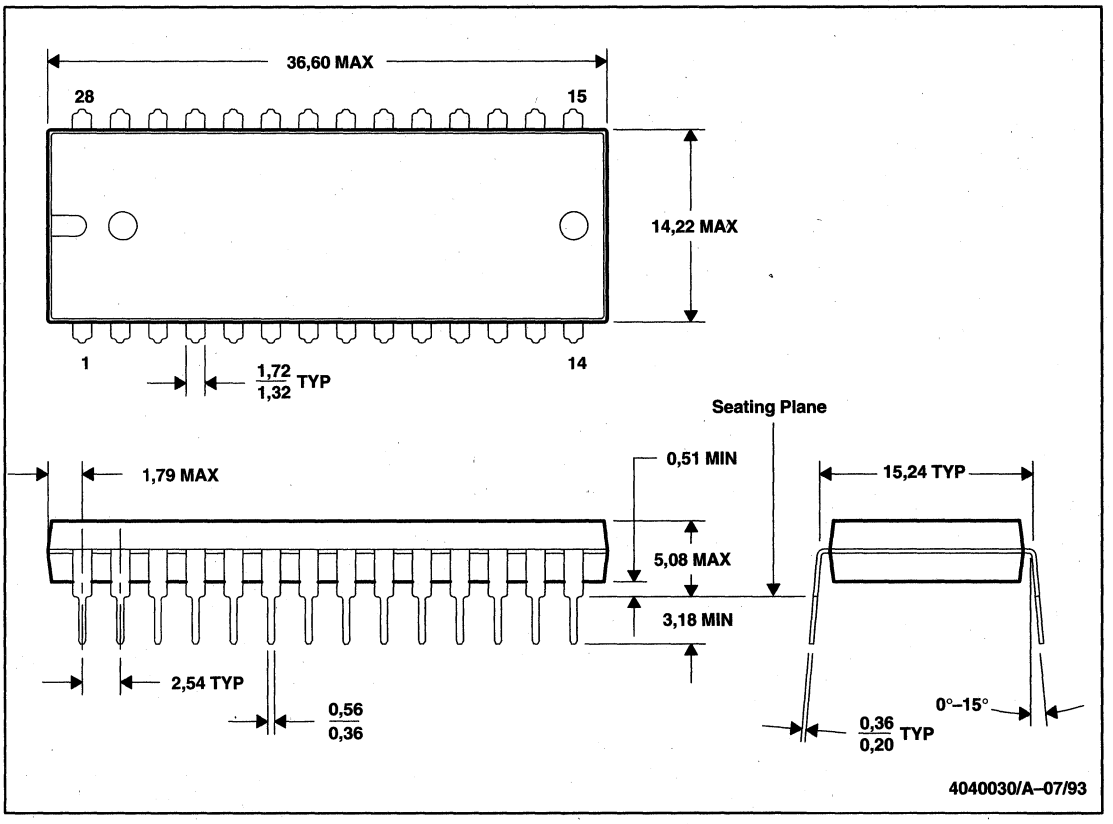
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each pin centerline is located within 0.010 (0,254) of its true longitudinal position.
D. This dimension does not apply for solder dipped leads.
E. For solder dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0,51) above seating plane.

NT/R-PDIP-T24 **PLASTIC DUAL-IN-LINE PACKAGE**



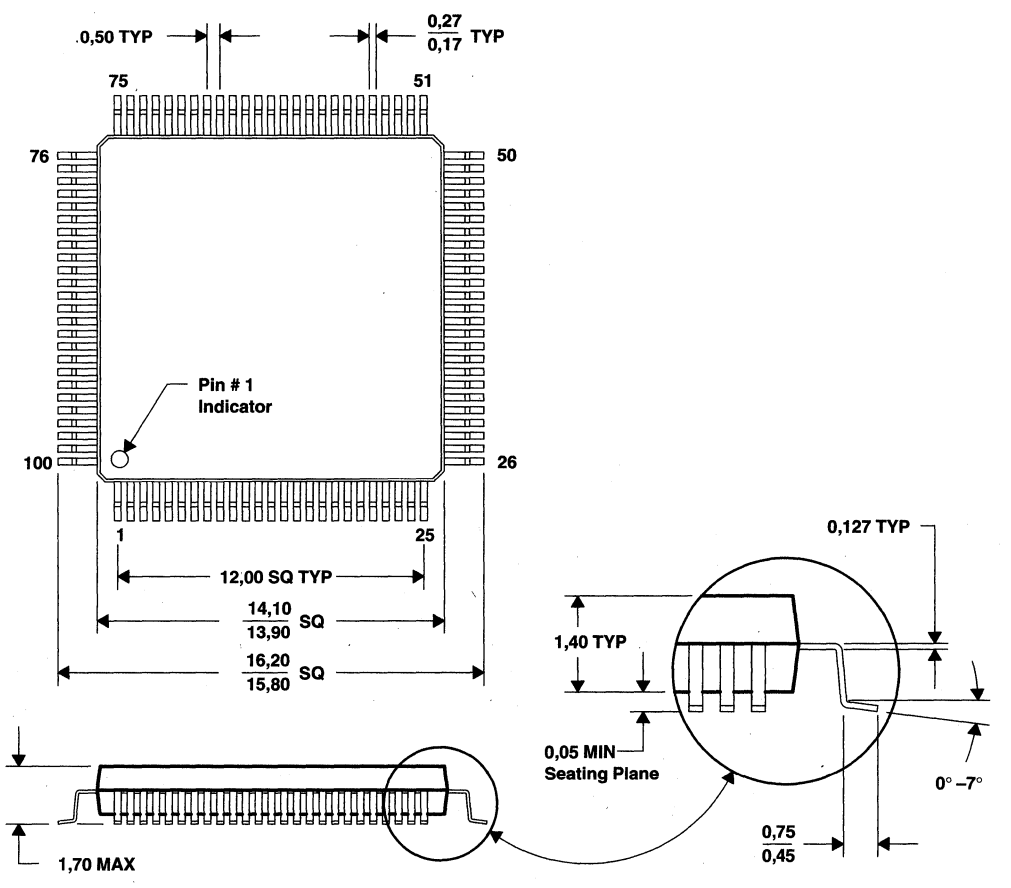
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

N/R-PDIP-T28 **PLASTIC DUAL-IN-LINE PACKAGE**



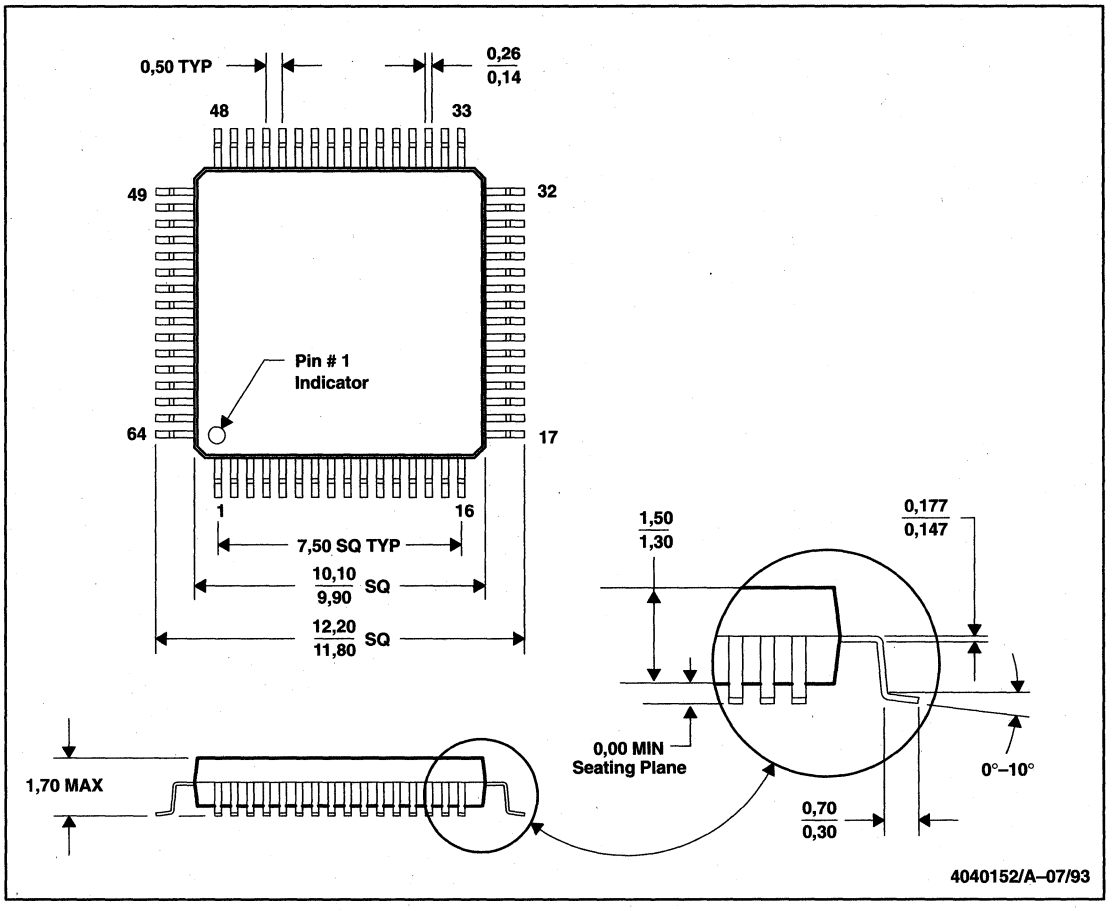
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

PZ/S-PQFP-G100 **PLASTIC QUAD FLAT PACKAGE**



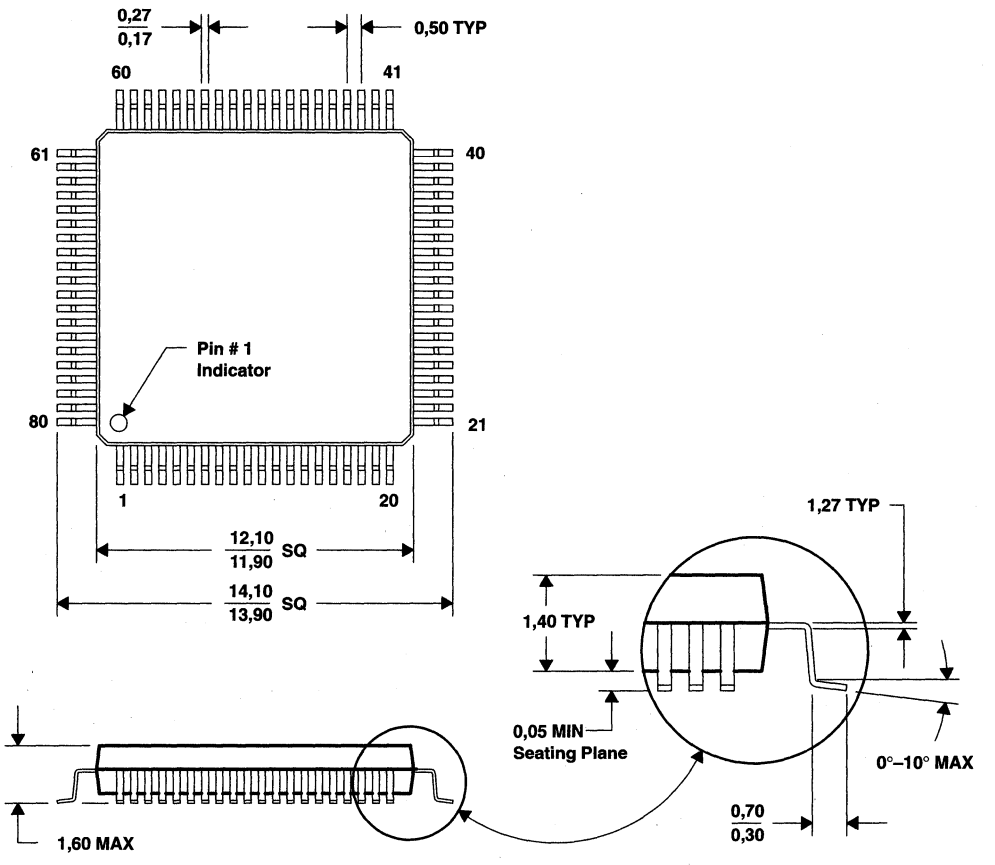
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Maximum deviation from caplanarity is 0,08 mm.

PM/S-PQFP-G64 **PLASTIC QUAD FLAT PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Maximum deviation from coplanarity is 0,08 mm.
D. Body dimensions do not include mold flash or protrusion.

PN/S-PQFP-G80 **PLASTIC QUAD FLAT PACKAGE**

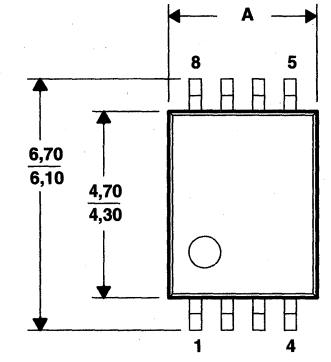


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Maximum deviation from coplanarity is 0,08 mm.

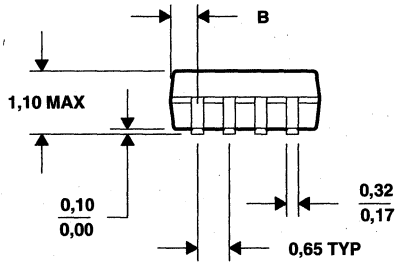
PW/R-PDSO-G**

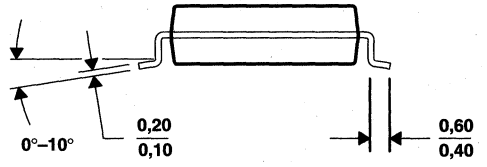
PLASTIC SMALL-OUTLINE PACKAGE

8-PIN SHOWN



DIM \ PINS**	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60
B MAX	0,65	0,70	0,38	0,48	0,48	0,78

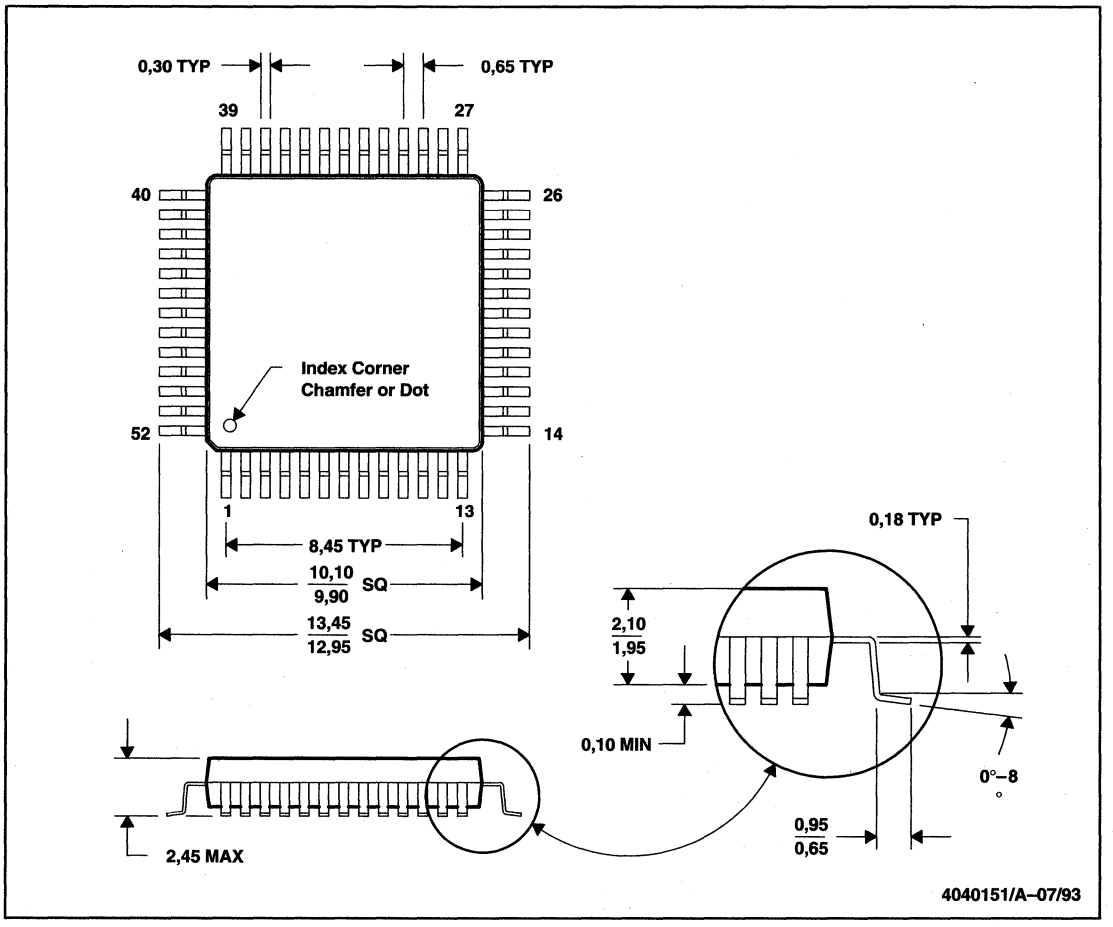




4040064/A–07/93

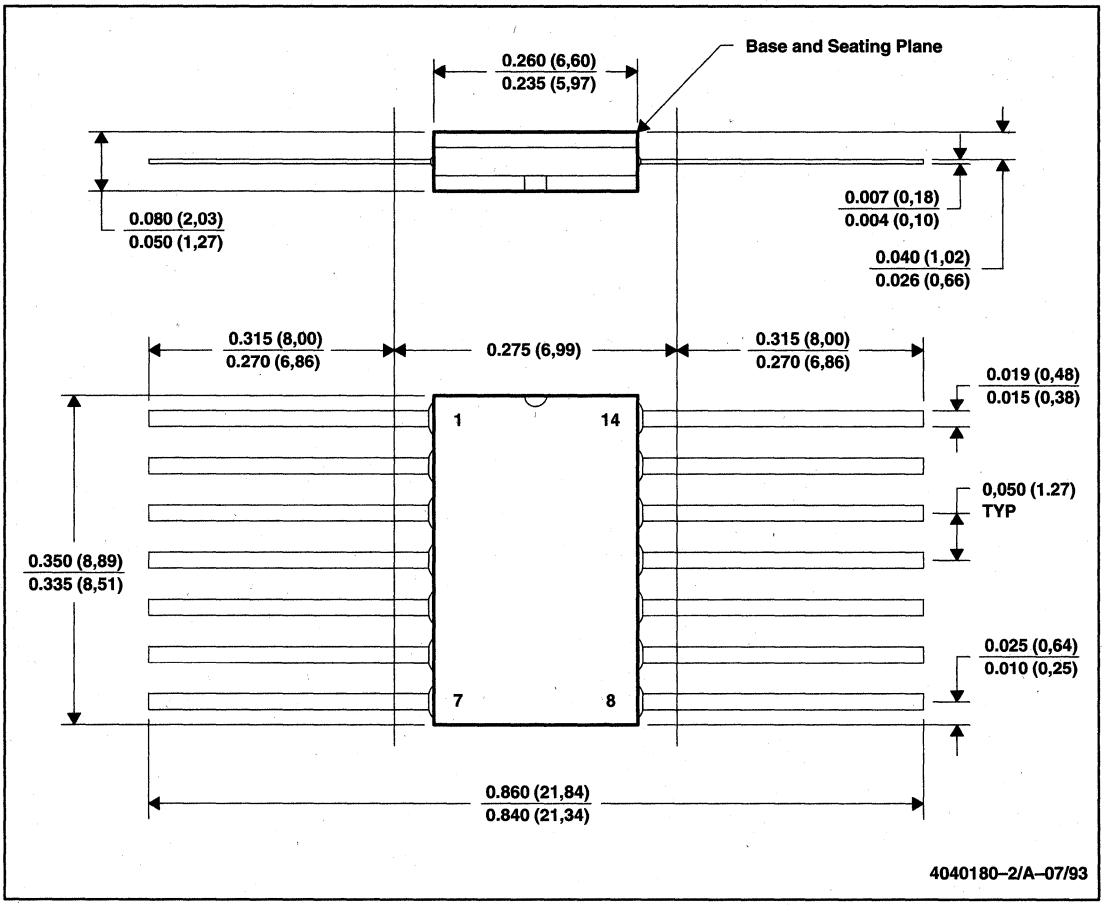
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

RC/S-PQFP–G52 **PLASTIC QUAD FLAT PACKAGE**



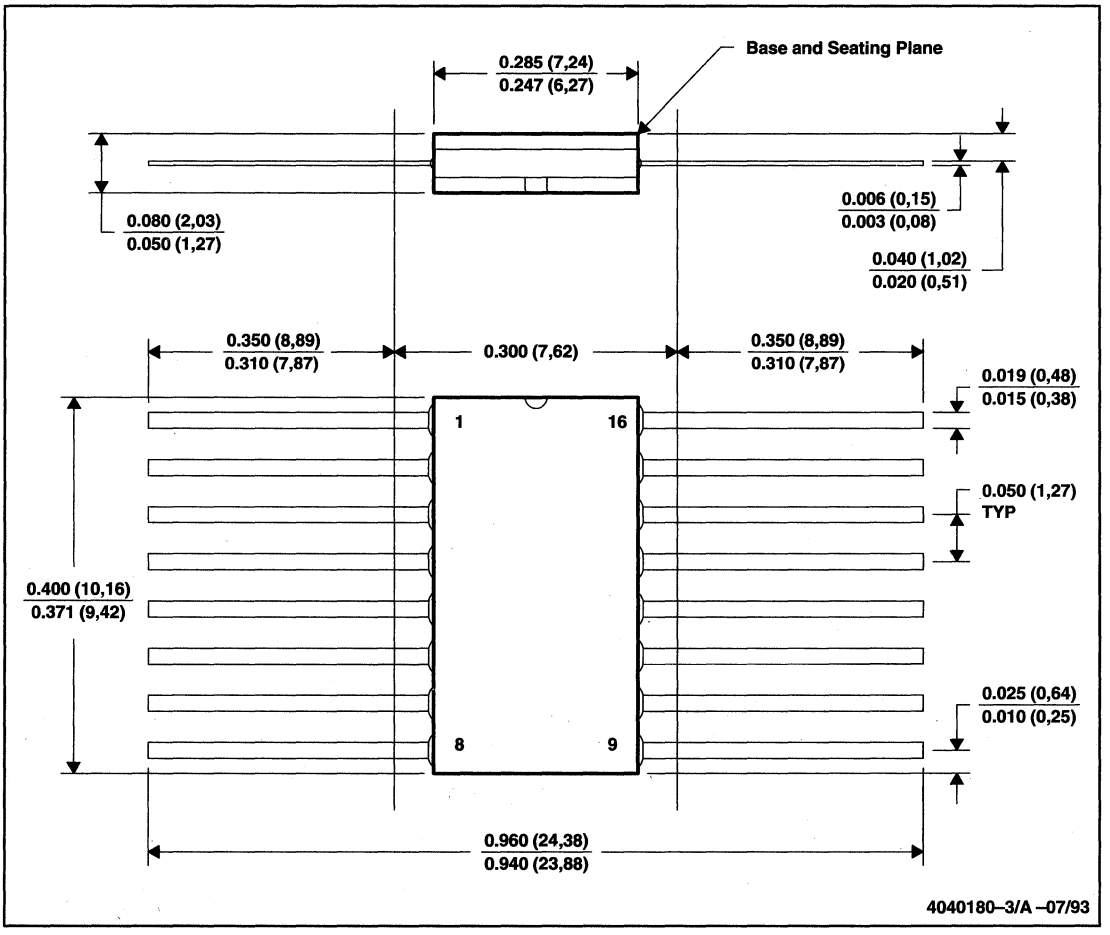
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

W/R-GDFP–F14 **CERAMIC FLAT PACKAGE**



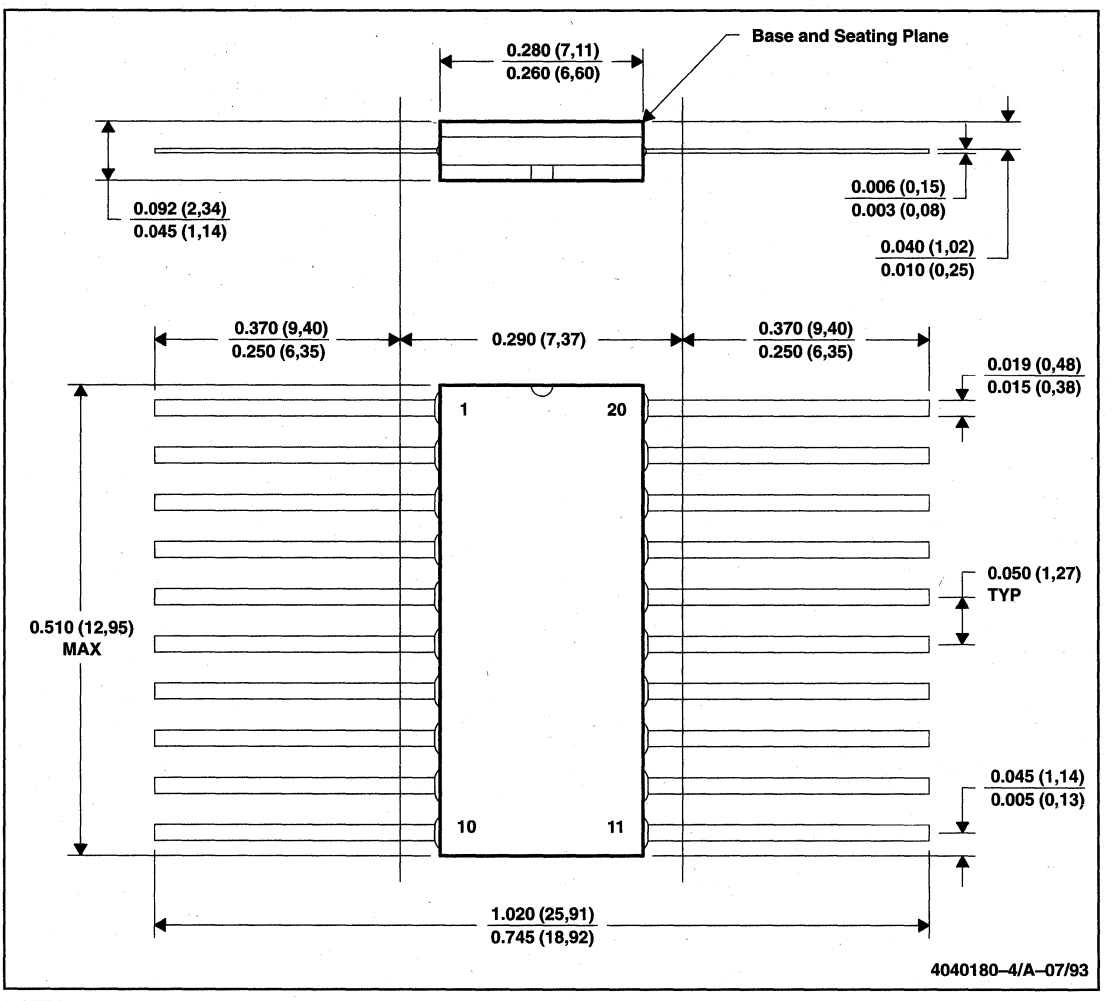
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
D. Falls within JEDEC MO-004AA dimensions.

W/R-GDFP–F16 **CERAMIC FLAT PACKAGE**



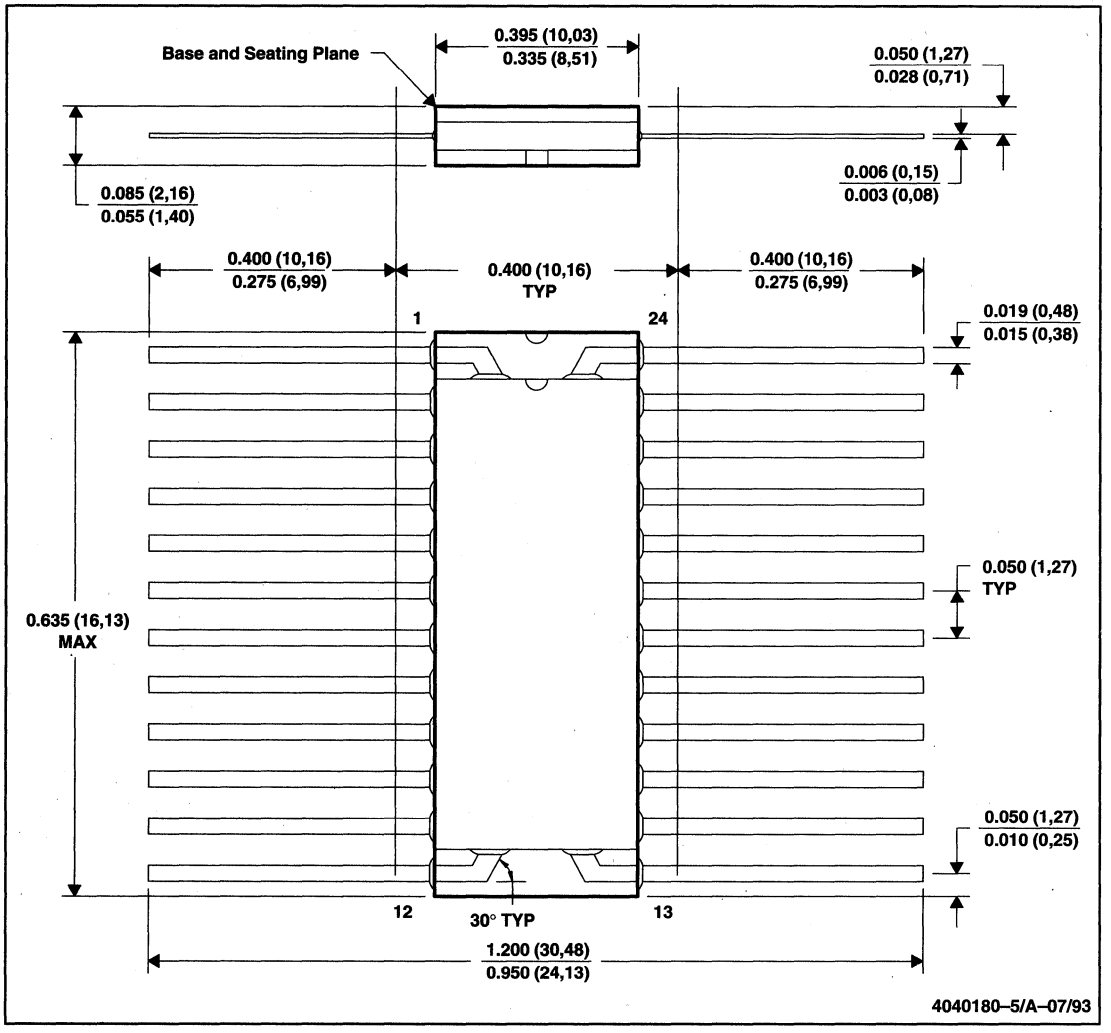
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
D. Falls within JEDEC MO-004AA dimensions.
E. Index point is provided on cap for terminal identification only.

W/R-GDFP–F20 **CERAMIC FLAT PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
D. Index point is provided on cap for terminal identification only.

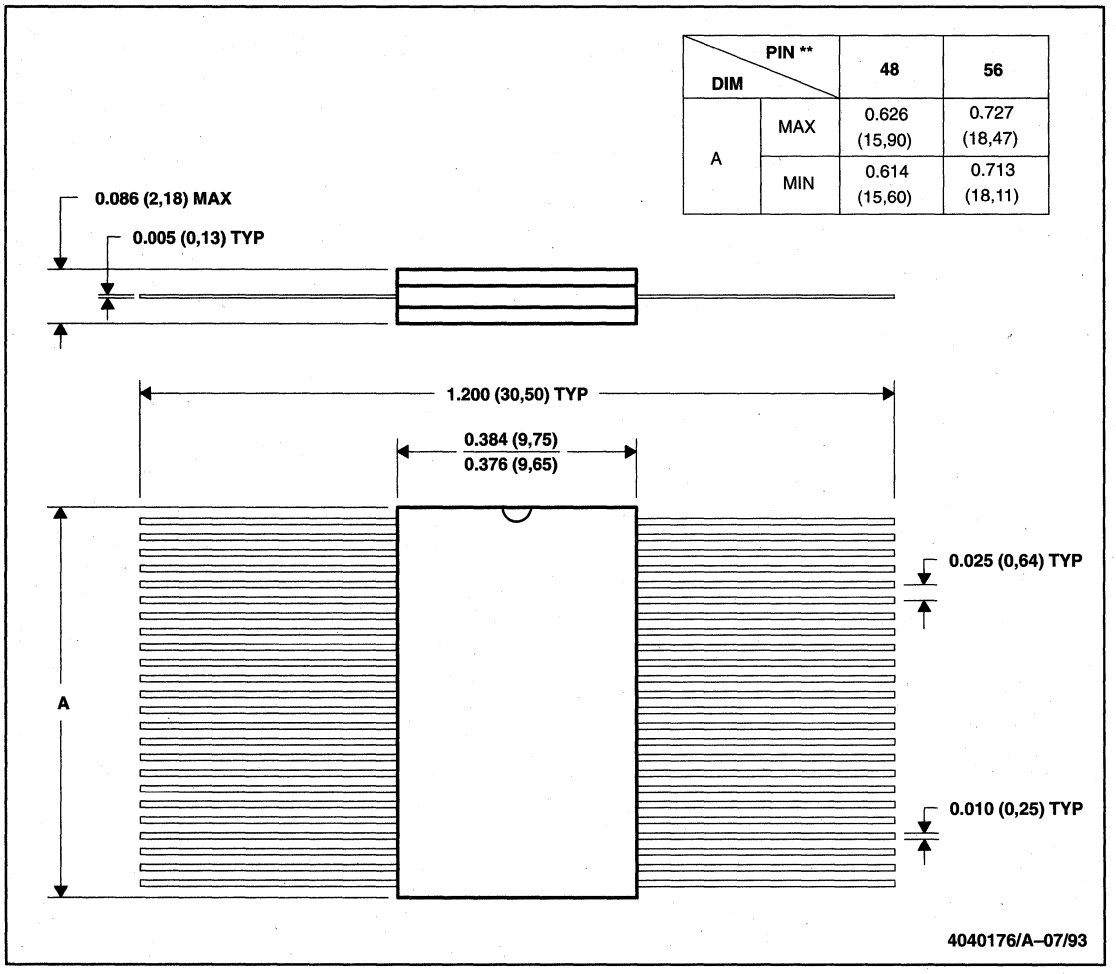
W/R-GDFP–F24 **CERAMIC FLAT PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
D. Falls within JEDEC MO-019AA dimensions.
E. Index point is provided on cap for terminal identification only.
F. End configuration of 24-pin package is at the option of TI.
G. Not applicable for solder-dipped leads. When solder-dipped leads are specified, dipped area extends from lead tip to within 0.050 (1,27) of the package body.

WD/R-GDFP-F** **CERAMIC FLAT PACKAGE**

48-PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

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D0293

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A0293

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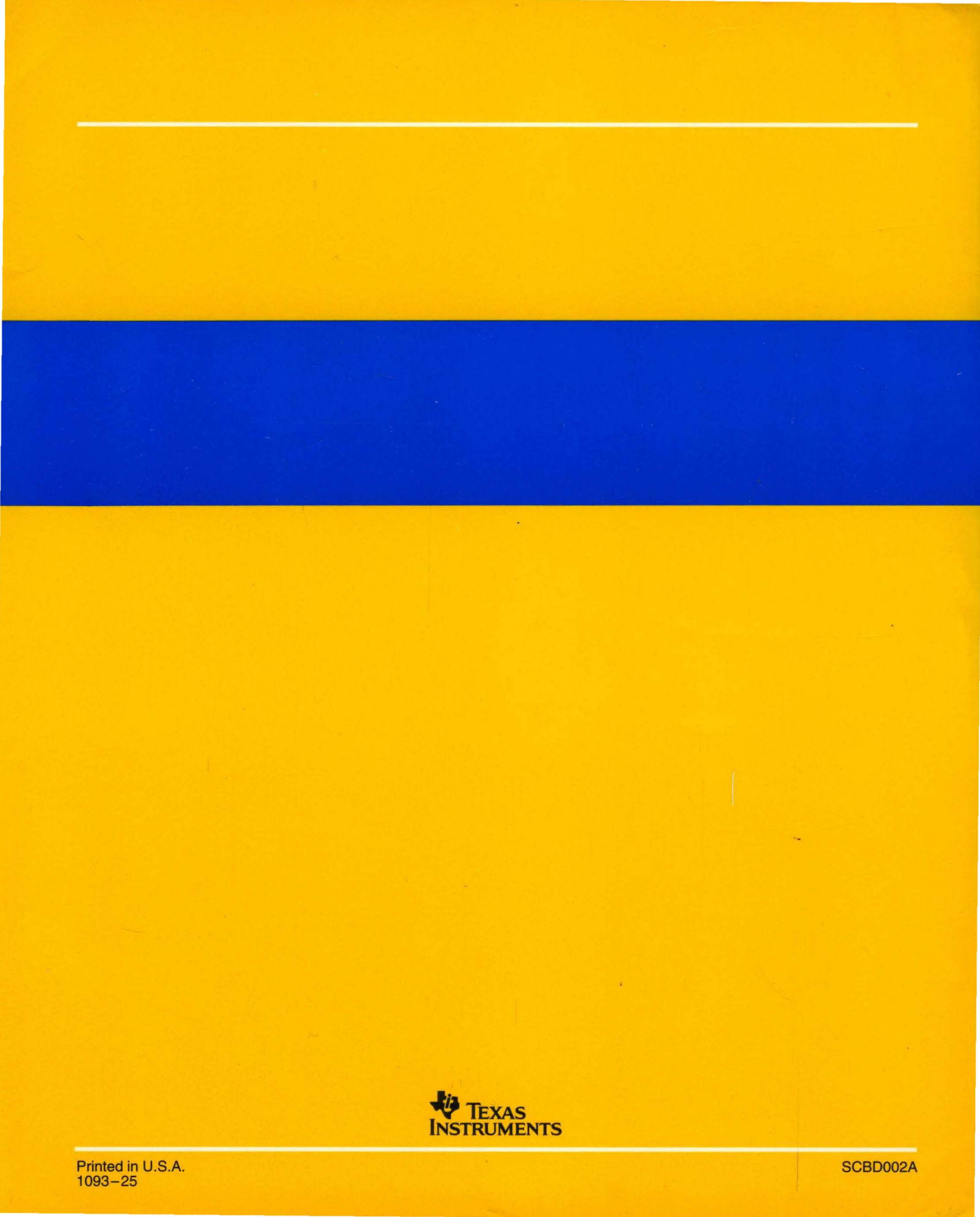

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