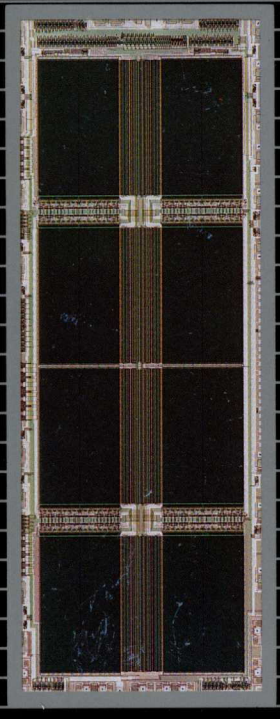
TOSHIBA



NON-VOLATILE MEMORY 1990

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

TOSHIBA

NON-VOLATILE MEMORY 1990

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Non-Volatile Product Guide

1. EPROM/HIGH SPEED EPROM

CAPACITY	PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	POWER SUPPLY (V)	OPERATING TEMPERATURE (℃)	POWER DISSIPATION max (mW)		PIN COUNT	PACKAGE	PACKAGE WIDTH (inch)
						ACTIVE	STANDBY		D P F J	
256K	TC57256AD-12	32Kx8	120	5V±5%	0 ~ 70	158	0.525	28	■	0.6
	TC57256AD-15		150		-40 ~ 85				■	
	TC57256AD-120		120	5V±10%	0 ~ 70	165	0.550		■	
	TC57256AD-150		150						■	
	TC57256AD-20		200	5V±5%	-40 ~ 85	158	0.525		■	
	TC57H256D-70		70		0 ~ 70	263	0.525		■	
	TC57H256D-85		85	5V±10%		275	0.550		■	
512K	TC57512AD-15	64Kx8	150	5V±5%	-40 ~ 85	158	0.525	28	■	0.6
	TC57512AD-20		200						■	
1M	TC571000AD-12	128Kx8	120	5V±5%	0 ~ 70	158	0.525	32	■	0.6
	TC571000AD-150		150	5V±10%		165	0.550		■	
	TC571001AD-12		120	5V±5%		158	0.525		■	
	TC571001AD-150		150	5V±10%		165	0.550		■	
	TC57H1000AD-85		85	5V±10%	0 ~ 70	220	0.550		■	
	TC57H1000AD-100		100						■	
	TC57H1001AD-85		85						■	
	TC57H1001AD-100		100						■	
	TC571024D-15	64Kx16	150	5V±5%	0 ~ 70	210	0.525	40	■	0.6
	TC571024D-20		200		-40 ~ 85				■	
	TC571024D-200		200	5V±10%		220	0.550		■	
	TC57H1024D-85		85	5V±5%	0 ~ 70	210	0.525		■	
	TC57H1024D-10		100						■	
	TC57H1024D-100		100	5V±10%		220	0.550		■	
	TC57H1025AD-55		55	5V±5%		315	52.5		■	
	TC57H1026D-45		45			368	52.5		■	
	TC57H1026D-35		35						■	
4M	TC574000D-12	512Kx8	120	5V±5%	0 ~ 70	315	0.525	32	■	0.6
	TC574000D-120		120	5V±10%		330	0.550		■	
	TC574000D-150		150						■	
	TC574000DI-150		150		-40 ~ 85	275	0.550		■	
	TC574000DI-200		200						■	
	TC574200D-120	256Kx16/512Kx8	120	5V±10%	0 ~ 70	330	0.550	40	■	
	TC574200D-150		150						■	
	TC574200D-200		200						■	

D = CERAMIC DIP, P = PLASTIC DIP, F = PLASTIC FLAT PACKAGE (SOP), J = PLASTIC SOJ

2. OTP/HIGH SPEED OTP

CAPACITY	PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	POWER SUPPLY (V)	OPERATING TEMPERATURE (°C)	POWER DISSIPATION max (mW)		PIN COUNT	PACKAGE	PACKAGE WIDTH (inch)
						ACTIVE	STANDBY		D P F J	
256K	TC54256AP/AF-20	32Kx8	200	5V±5%	-40 ~ 85	158	0.525	28	■ ■	0.6 (P) 0.45 (F)
512K	TC54512AP/AF-15	64Kx8	150	5V±5%	-40 ~ 85	158	0.525	28	■ ■	0.6 (P)
	TC54512AP/AF-20		200							0.45 (F)
1M	TC541000J-15	128Kx8	150	5V±5%	0 ~ 70	158	0.525	28	■	0.4
	TC541001J-15		150						■	
	TC541000J-20		200		-40 ~ 85				■	
	TC541001J-20		200						■	
	TC541000P/F-15		150		0 ~ 70				■ ■	0.6 (P) 0.525 (F)
	TC541001P/F-15		150						■ ■	
	TC541000P/F-20		200		-40 ~ 85				■ ■	
	TC541001P/F-20		200						■ ■	
	TC54H1024P/F-85	64Kx16	85	5V±5%	0 ~ 70	210	0.525	40	■ ■	0.6 (P) 0.525 (F)
	TC54H1024P/F-10		100						■ ■	
4M	TC544000P/F-12	512Kx8	120	5V±5%	0 ~ 70	315	0.525	32	■ ■	0.6 (P)
	TC544000P/F-120		120	5V±10%		330	0.550	32	■ ■	0.525 (F)
	TC544000P/F-150								■ ■	

D = CERAMIC DIP, P = PLASTIC DIP, F = PLASTIC FLAT PACKAGE (SOP), J = PLASTIC SOJ

3. MROM/HIGH SPEED MROM

CAPACITY	PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	POWER SUPPLY (V)	OPERATING TEMPERATURE (°C)	POWER DISSIPATION max (mW)		PIN COUNT	PACKAGE D P F J	PACKAGE WIDTH (inch)
						ACTIVE	STANDBY			
1M	TC531000CP/CF-12	128Kx8	120	5V±10%	-40 ~ 70	220	0.11	28	■ ■	0.6 (P)
	TC531000CP/CF		150			193			■ ■	0.525 (F)
	TC531001CP/CF-12		120			220			■ ■	
	TC531001CP/CF		150			193			■ ■	
	TC531024P/F-12	64Kx16	120	5V±5%	0 ~ 70	220		40	■ ■	
	TC531024P/F-15		150	5V±10%		193			■ ■	
4M	TC534000P/F	512Kx8	200	5V±5%	-40 ~ 70	165	0.11	32	■ ■	0.6 (P)
	TC534000P/F		250	5V±10%	-40 ~ 85				■ ■	0.525 (F)
	TC534000AP/AF		150		0 ~ 70	220			■ ■	
	TC534200P/F	256Kx16/512Kx8	150			275		40	■ ■	
8M	TC538200P/F	512Kx16/1Mx8	200	5V±10%	0 ~ 70	275	0.55	42P 44F	■ ■	0.6 (P) 0.6 (F)
16M	TC5316200P/F	1Mx16/2Mx8	200	5V±10%	0 ~ 70	275	0.55	42P 44F	■ ■	0.6 (P) 0.6 (F)

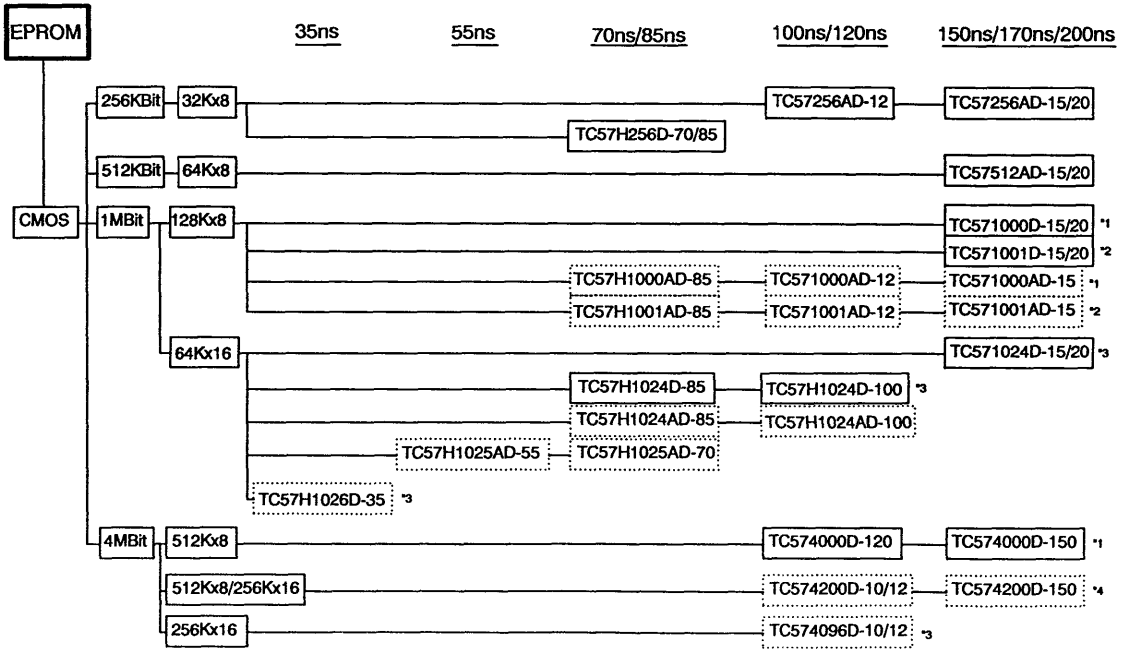
D = CERAMIC DIP, P = PLASTIC DIP, F = PLASTIC FLAT PACKAGE (SOP), J = PLASTIC SOJ

4. FLASH E²PROM

CAPACITY	PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	POWER SUPPLY (V)	OPERATING TEMPERATURE (°C)	POWER DISSIPATION max (mW)		PIN COUNT	PACKAGE D P F J	PACKAGE WIDTH (inch)
						ACTIVE	STANDBY			
256K	TC58257AP/AF-17LV	32Kx8	170	5V±10%	-10 ~ 70	165	0.55	28	■ ■	0.6 (P)
	TC58257AP/AF-20LV		200						■ ■	0.45 (F)
	TC58257AP/AF-25LV		250						■ ■	
1M	TC58F1000P/F/J-15	128Kx8	150	5V±10%	0 ~ 70	165	0.55	32	■ ■ ■	0.6 (P)
	TC58F1000P/F/J-20		200						■ ■ ■	0.525 (F) 0.4 (J)

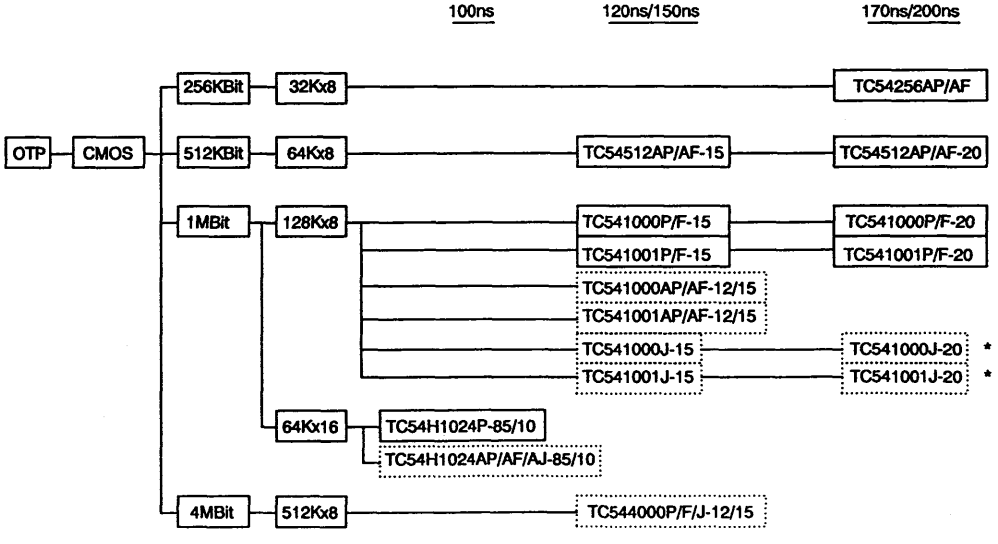
D = CERAMIC DIP, P = PLASTIC DIP, F = PLASTIC FLAT PACKAGE (SOP), J = PLASTIC SOJ

TOSHIBA EPROM/HIGH SPEED EPROM



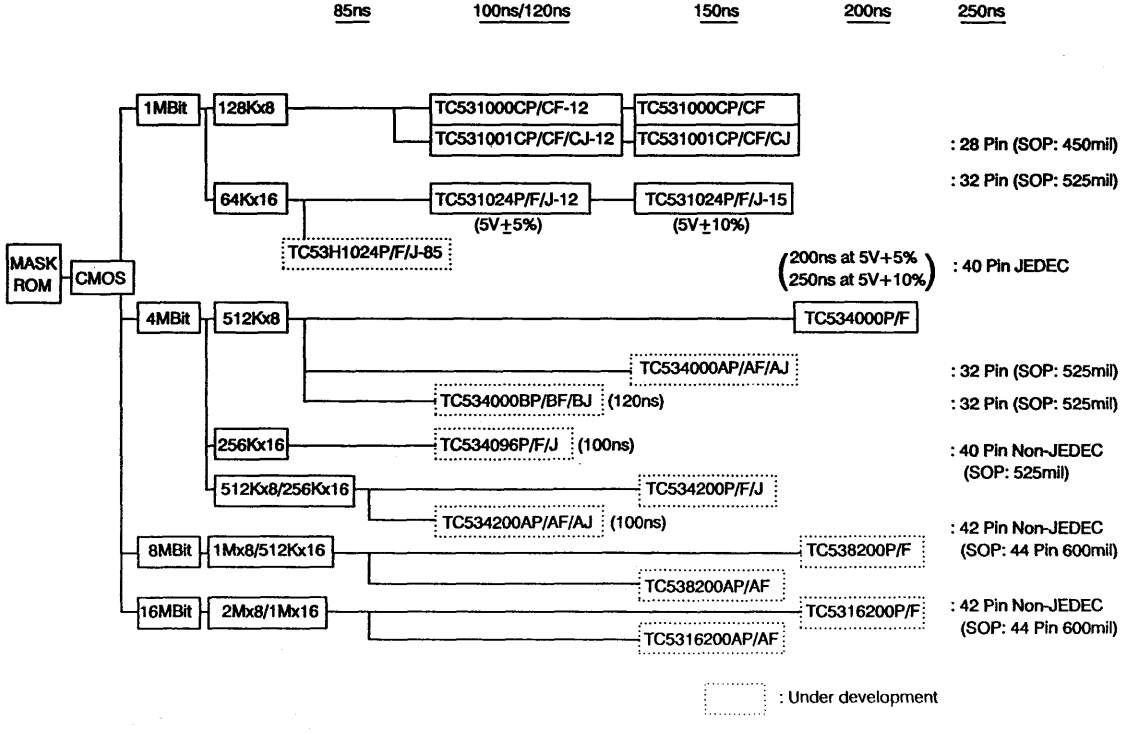
*1 : 32 Pin JEDEC Standard
*2 : 32 Pin (MROM Pin Compatible)
*3 : 40 Pin JEDEC Standard
*4 : 40 Pin (MROM Pin Compatible)

TOSHIBA OTP/HIGH SPEED OTP

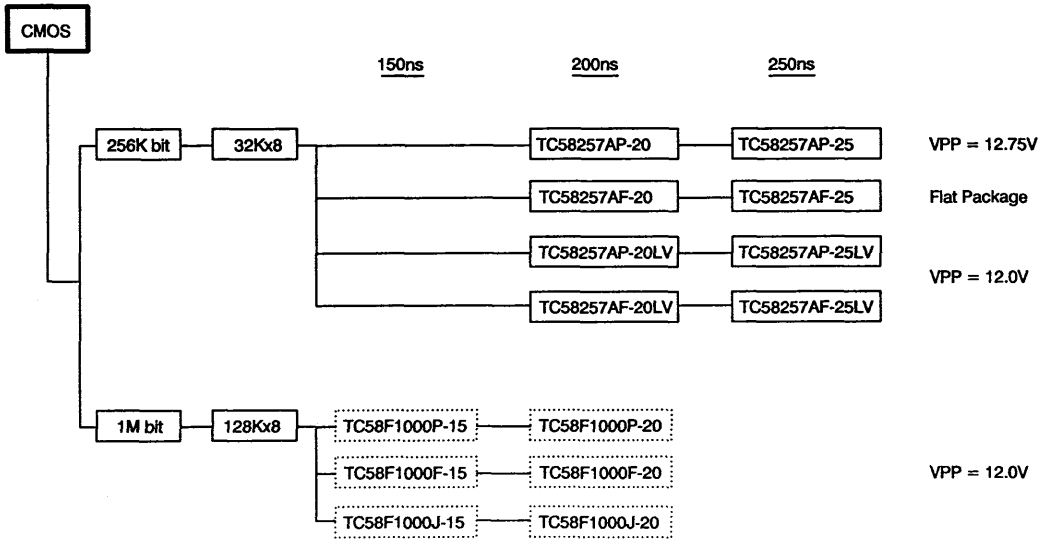


* : 400mil 32pin SOJ

TOSHIBA MASK ROM/HIGH SPEED MASK ROM



FLASH E²PROM



Non-Volatile Cross Reference

1. EPROM

ORGANIZATION	32Kx8	64Kx8	128Kx8	128Kx8	64Kx16
PACKAGE WIDTH	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP
TOSHIBA	TC57256AD	TC57512AD	TC571000AD	TC571001AD	TC571024D
AMD	AM27C256	AM27C512	AM27C010		AM27C1024
FUJITSU	MBM27C256A	MBM27C512	MBM27C1001	MBM27C1000	MBM27C1024
HITACHI	HN27C256		HN27C101	HN27C301	HN27C1024
INTEL	27C256		27C010		27C210
MITSUBISHI	M5M27C256	M5M27C512A	M5M27C101	M5M27C100	M5M27C102
NEC	uPD27C256A	uPD27C512	uPD27C1001	uPD27C1000	uPD27C1024
OKI	MSM27256				
TI	TMS27C256	TMS27C512	TMS27C010		TMS27C210

ORGANIZATION	512Kx8	512Kx8	512Kx8/256Kx16
PACKAGE WIDTH	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP
TOSHIBA	TC574000D	TC574000DI	TC574200D
AMD			
FUJITSU	MBM27C4000/1		MBM27C4096
HITACHI			
INTEL			27C240
MITSUBISHI			
NEC	uPD27C4001		
OKI			
TI			

2. HIGH SPEED EPROM

ORGANIZATION	32Kx8	128Kx8	64Kx16	64Kx16	64Kx16
PACKAGE WIDTH	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP
TOSHIBA	TC57H256D	TC57H1000/1AD	TC57H1024D	TC57H1025AD	TC57H1026D
HITACHI	HN27C256H		HN27C1024H		

3. OTP

ORGANIZATION	32Kx8		64Kx8		128Kx8	
PACKAGE WIDTH	0.6 in DIP	0.45 in SOP	0.6 in DIP	0.45 in SOP	0.6 in DIP	0.525 in SOP
TOSHIBA	TC54256AP	TC54256AF	TC54512AP	TC54512AF	TC541000P	TC541000F
AMD	AM27C256		AM27C512		AM27C010	
FUJITSU						
HITACHI		HN27C256FP			HN27C101P	HN27C101FP
INTEL	27C256				27C010	
MITSUBISHI	M5M27C256P	M5M27C256FP	M5M27C512AP	M5M27C512AFP	M5M27C101P	M5M27C101FP
NEC						
OKI						
TI	TMS27PC256					

DESCRIPTION	128Kx8		512Kx8	
PACKAGE WIDTH	0.6 in DIP	0.525 in SOP	0.6 in DIP	0.525 in SOP
TOSHIBA	TC541001P	TC541001F	TC544000P	TC544000F
AMD				
FUJITSU				
HITACHI	HN27C301P	HN27C301FP		
INTEL				
MITSUBISHI	M5M27C100P	M5M27C100FP		
NEC				
OKI				
TI				

4. HIGH SPEED OTP

ORGANIZATION		
PACKAGE WIDTH	0.6 in DIP	0.525 in SOP
TOSHIBA	TC54H1024P	TC54H1024F
AMD		
FUJITSU		
HITACHI	HN27C1024HG	
INTEL		
MITSUBISHI		
NEC		
OKI		
TI		

5. MASK ROM

ORGANIZATION	128Kx8		128Kx8	
PACKAGE WIDTH	0.6 in DIP	0.45 in SOP	0.6 in DIP	0.525 in SOP
TOSHIBA	TC531000CP	TC531000CF	TC531001CP	TC531001CF
FUJITSU	MB831000			
HITACHI	HN62321/31P	HN62321/31F	HN62321A/31AP	HN62321A/31AF
MITSUBISHI	M5M231000P			
NEC	uPD23C1000C	uPD23C1000G	uPD23C1001EC	
OKI	MSM531000RS			
SHARP	LH531000			
SONY	CXK381000P			

ORGANIZATION	64Kx16	64Kx16	512Kx8/256Kx16	
PACKAGE WIDTH	0.6 in DIP	0.6 in DIP	0.6 in DIP	0.525 in SOP
TOSHIBA	TC531024P	TC53H1024P	TC534200P	TC534200F
FUJITSU			MB834100	
HITACHI			HN62404P	
MITSUBISHI			M5M23C400P	
NEC	uPD23C1024EP			
OKI				
SHARP			LH534000	
SONY				

5. MASK ROM

ORGANIZATION	1Mx8/512Kx16		2Mx8/1Mx16	
PACKAGE WIDTH	0.6 in DIP	0.6 in SOP	0.6 in DIP	0.6 in SOP
TOSHIBA	TC538200P	TC538200F	TC5316200P	TC5316200F
FUJITSU				
HITACHI	HN62801P	HN62801F	HN621601P	HN621601F
MITSUBISHI	M5M23C800P	M5M23C800FP	M5M231600P	M5M231600FP
NEC	uPD23C8000C	uPD23C8000G	uPD23C1600C	uPD23C1600G
OKI				
SHARP	LH538100	LH538100	LH531601	LH531601
SONY				

ORGANIZATION	512Kx8	
PACKAGE WIDTH	0.6 in DIP	0.525 in SOP
TOSHIBA	TC534000AP	TC534000AF
FUJITSU	MB834000	MB834000
HITACHI	HN62401P	HN62401F
MITSUBISHI	M5M23C400P	M5M217C400FP
NEC	uPD23C4000C	uPD23C4000G
OKI		
SHARP	LH534100	LH534100
SONY		

6. FLASH E²PROM

ORGANIZATION	32Kx8		128Kx8		
PACKAGE WIDTH	0.6 in DIP	0.45 in SOP	0.6 in DIP	0.525 in SOP	0.4 in SOJ
TOSHIBA	TC58257AP	TC58257AF	TC58F1000P	TC58F1000F	TC58F1000J
INTEL	27/28F256		28F010		
SEEQ			48C1024		

EPROM

32,768 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC57256AD is a 32,768 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256AD's access time is 120ns, and the TC57256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/8.3MHz and standby current to 100μA. For program operation, the programming is achieved by using the high speed programming mode. TC57256AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

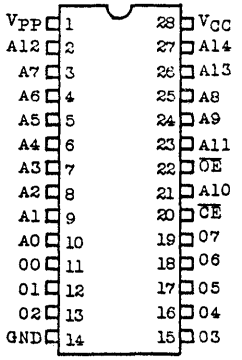
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS

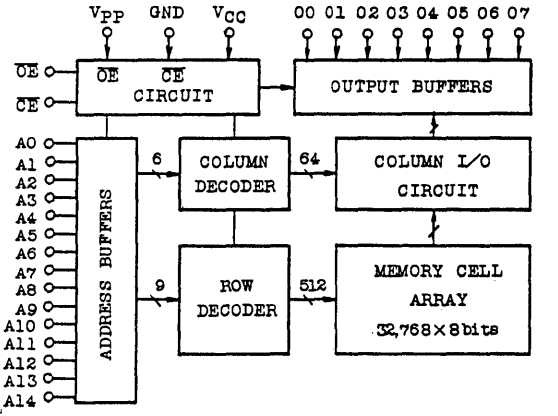
	-12	-120	-150
V_{CC}	5V±5%	5V±10%	
t_{ACC}	120ns	120ns	150ns

- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256D
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ~ A14	Address Inputs
O0 ~ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ~ O7 (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V 1)	6V 1)	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L	12.75V 2)	6.25V 2)	Data Out	

* H or L 1); HIGH SPEED PROGRAM MODE I,
2): HIGH SPEED PROGRAM MODE II

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	0 ∿ 70	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57256AD-12	TC57256AD-120/150
Ta	Operating Temperature	0 ∿ 70°C	0 ∿ 70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6V ∿ V_{CC}+0.6V	V_{CC}-0.6V ∿ V_{CC}+0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4 ∿ V_{CC}		-	-	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}$=0V	f=8.3MHz	-	-	30	mA
I_{CCO2}		I_{OUT}=0mA	f=1MHz	-	-	15	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{IH}	Input High Voltage	-		2.2	-	V_{CC}+0.3	V
V_{IL}	Output Low Voltage	-		-0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=V_{CC}-0.6 ∿ V_{CC}+0.6		-	-	±10	μA

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TC57256AD-120/12		TC57256AD-150		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	120	-	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	120	-	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	60	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	50	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	0	-	ns

A.C. TEST CONDITIONS

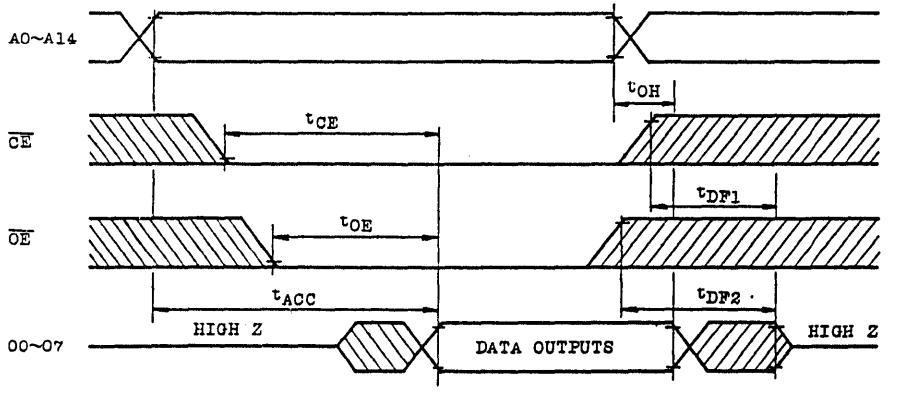
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM MODE I

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : $0.45V \sim 2.4V$
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overpgoram pulse may vary as a function of the counter value X.

HIGH SPEED PROGRAM OPERATION II

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	Vpp Power Supply Voltage	12.50	12.75	13.00	V

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	Vpp Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

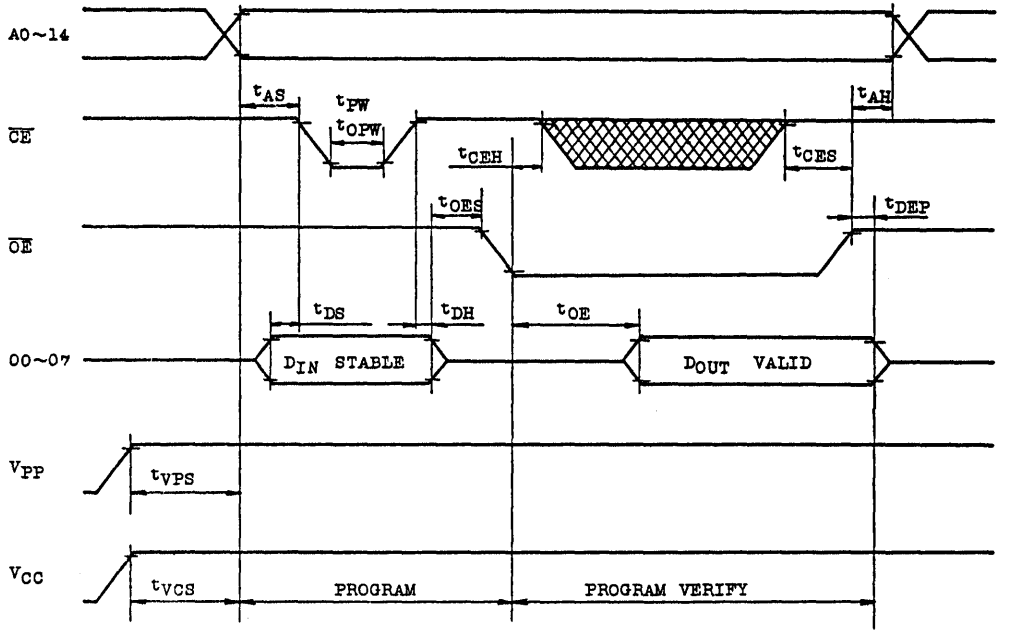
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	Vpp Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM MODE I (V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)
HIGH SPEED PROGRAM MODE II (V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)



Note 1. V_{CC} must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V (12.75V) may cause permanent damage to the device.

3. The Vpp supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537A°(Angstroms) to the chip through the transparent window.
The integrated dose (ultraviolet light intensity [w/cm^2] x exposure time [sec.]) for erasure should be a minimum of 15 [w • sec/cm^2]
When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.
And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In the case, the integrated dose is 12000 [μw/cm^2] x (20 x 60) [sec] = 15 [w • sec/cm^2].)
The TC57256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the fluorescent lamps will include 3000∅4000A°wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57256AD's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=0 ∿ 70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	1) 12.5V	1) 6V	Data In	Active
	Program Inhibit	H	H	2) 12.75V	2) 6.25V	High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}, 1); HIGH SPEED PROGRAM MODE I
2); HIGH SPEED PROGRAM MODE II

READ MODE

The TC57256AD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two or more TC57256AD's can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256AD has a low power standby mode controlled by the $\overline{CE}$ signal.
By applying a high level to the $\overline{CE}$ input, the TC57256AD is placed in the standby mode which reduces the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TC57256AD is in the programming mode when the Vpp input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$.
The TC57256AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V or +12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC57256AD from being programmed.
Programming of two or more TC57256AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

The program time can be greatly decreased by using this high speed programming mode.
The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with $V_{CC}=Vpp=5V$.

HIGH SPEED PROGRAM MODE II

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC}=6.25V.

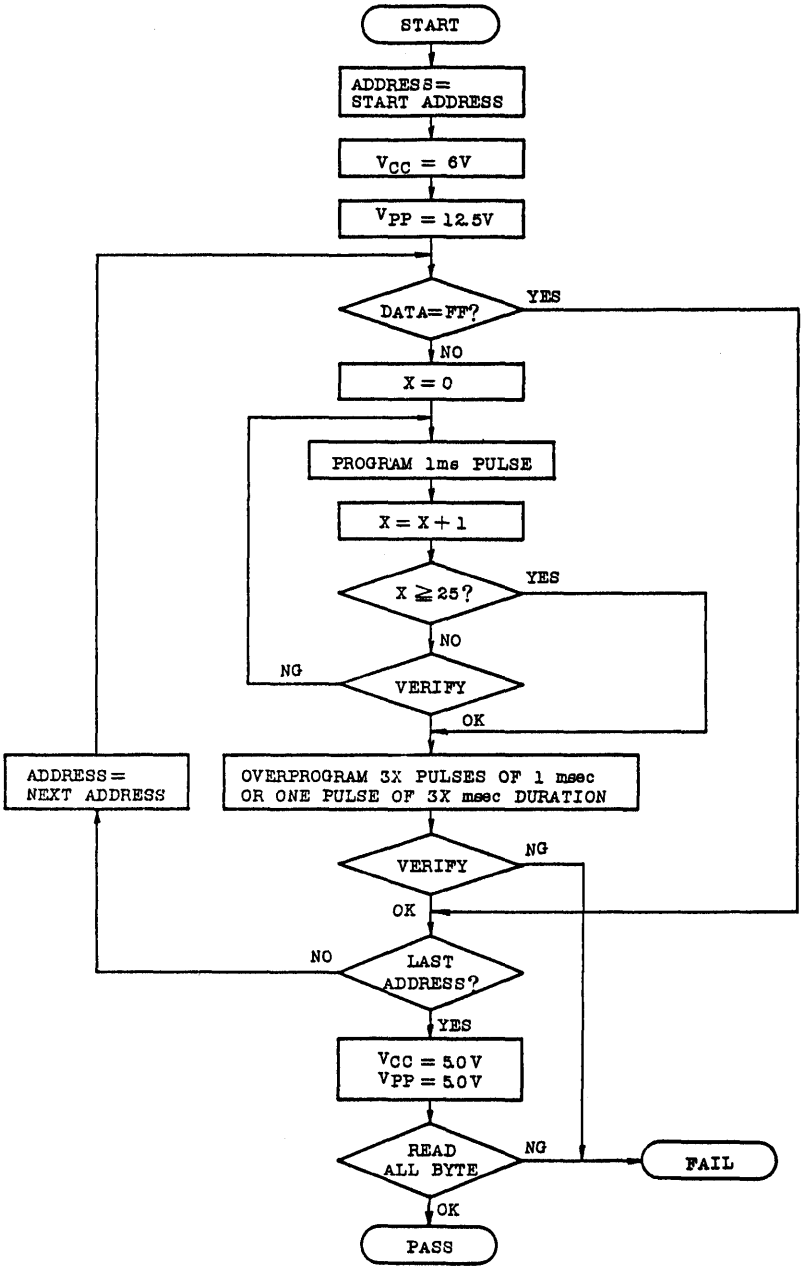
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

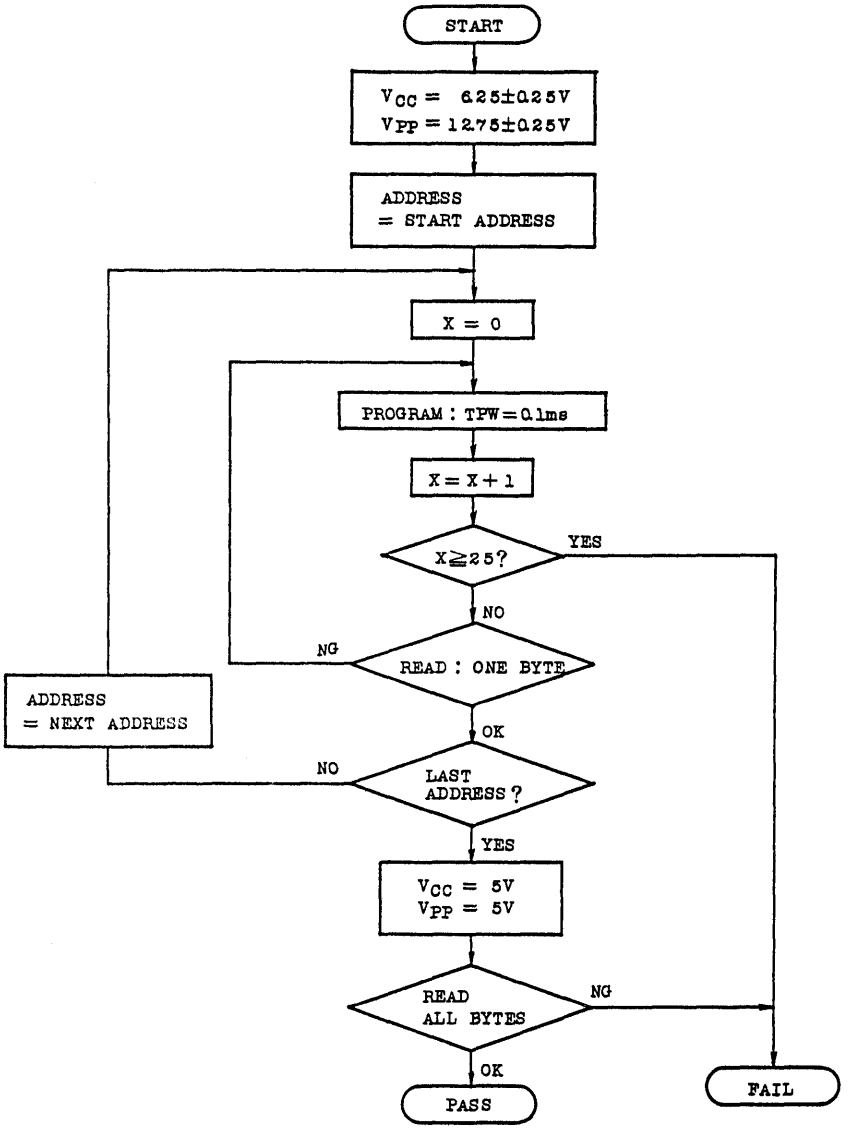
HIGH SPEED PROGRAM MODE I

FLOW CHART



HIGH SPEED PROGRAM MODE II

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57256AD which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC57256AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7). The following table shows electric signature of TD57256AD.

PINS / SIGNATURE	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

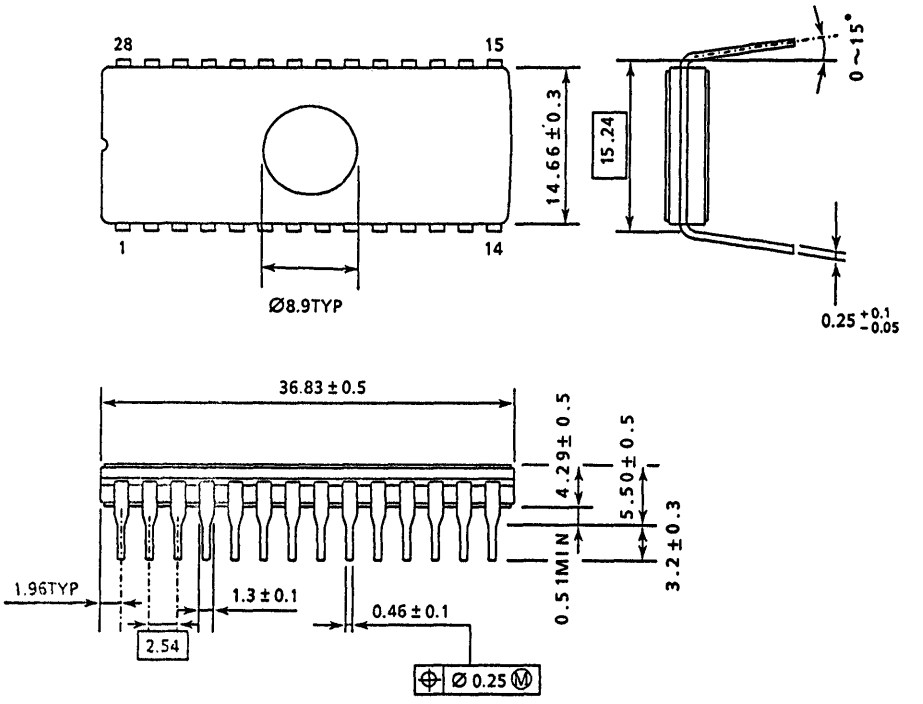
Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}$=V_{IL}

OUTLINE DRAWINGS

WDIP28-G-600

Unit : mm



32,768 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

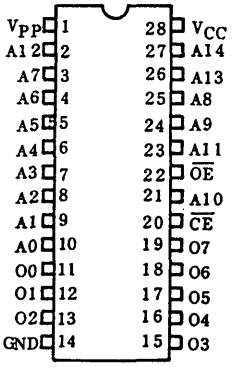
DESCRIPTION

The TC57256AD is a 32,768 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256AD's access time is 150ns, and the TC57256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/6.7MHz and standby current to 100μA. For program operation, the programming is achieved by using the high speed programming mode. TC57256AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

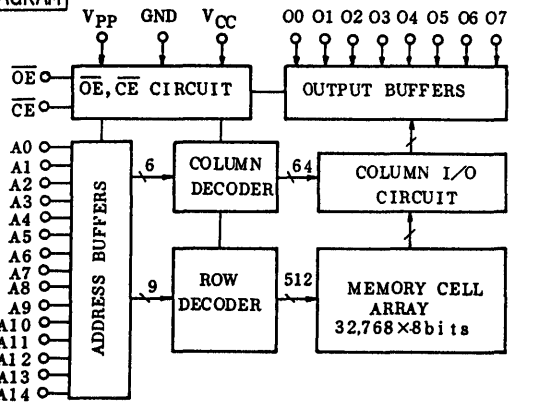
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  Active : 30mA/6.7MHz
  Standby: 100μA
- Fast access time: TC57256AD-15 150ns
  TC57256AD-20 200ns
- Single 5V power supply
- Fully static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256D
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A14	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	

DC and OPERATING CHARACTERISTICS (Ta=-40 ∿ 85°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0V ∿ V_{CC}		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$=0V, I_{OUT}=0mA	f=6.7MHz	-	-	30	mA
I_{CC02}			f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{CC} Current	V_{PP}=V_{CC}±0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ∿ V_{CC}		-	-	±10	μA

AC CHARACTERISTICS ($Ta=-40 \sim 85°C$, $V_{CC}=5V \pm 5\%$, $V_{PP}=V_{CC} \pm 0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	TC57256AD-15		TC57256AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	150	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	70	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	0	60	
t_{OH}	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	0	-	

AC TEST CONDITIONS

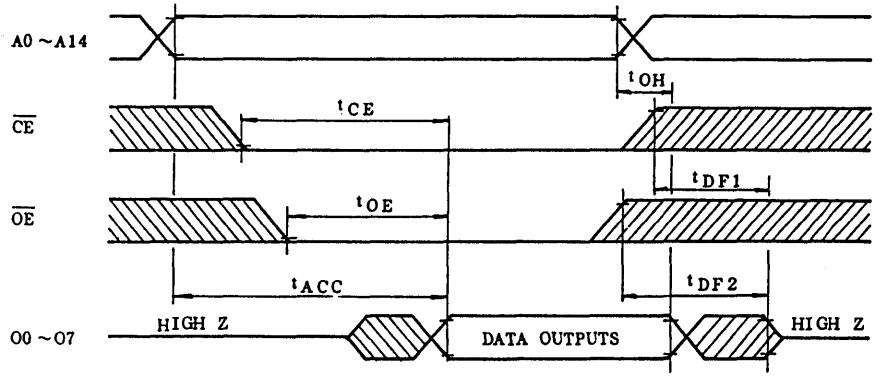
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

DC and OPERATING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

AC PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

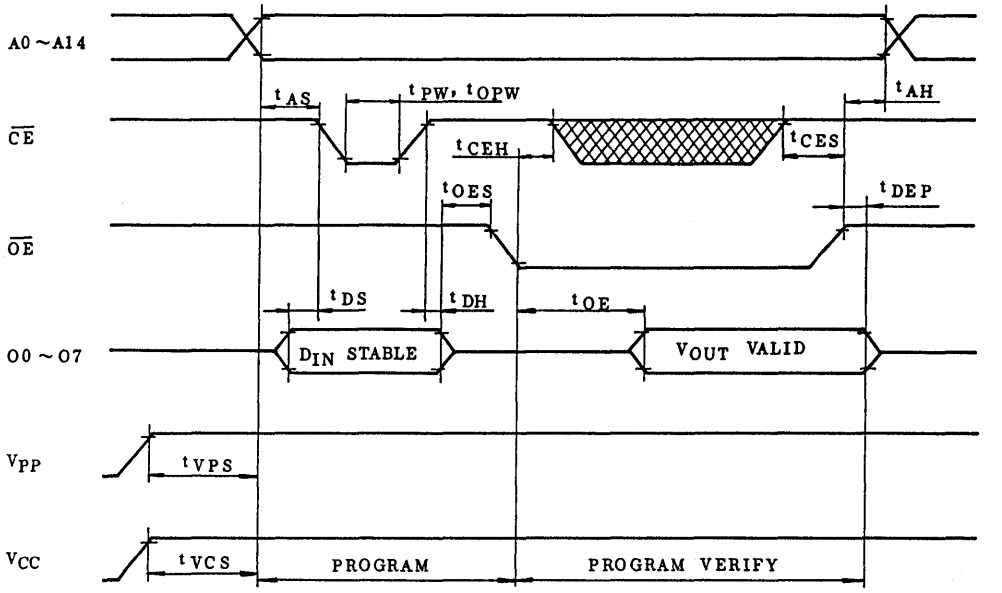
AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : $0.45V \sim 2.4V$
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation.
So the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537A°(Angstroms) to the chip through the transparent window.
The integrated dose (ultraviolet light intensity [w/cm^2] x exposure time [sec.]) for erasure should be a minimum of 15 [w • sec/cm^2].
When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.
And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm^2] x (20 x 60) [sec] = 15 [w • sec/cm^2].)
The TC57256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the fluorescent lamps will include 3000~4000A°wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57256AD's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=-40 ∿ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC57256AD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two or more TC57256AD's can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256AD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC57256AD is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TC57256AD is in the programming mode when the Vpp input is at 12.5V and CE is at TTL-Low under $\overline{OE}=V_{IH}$.
The TC57256AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly porgrammed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL}.

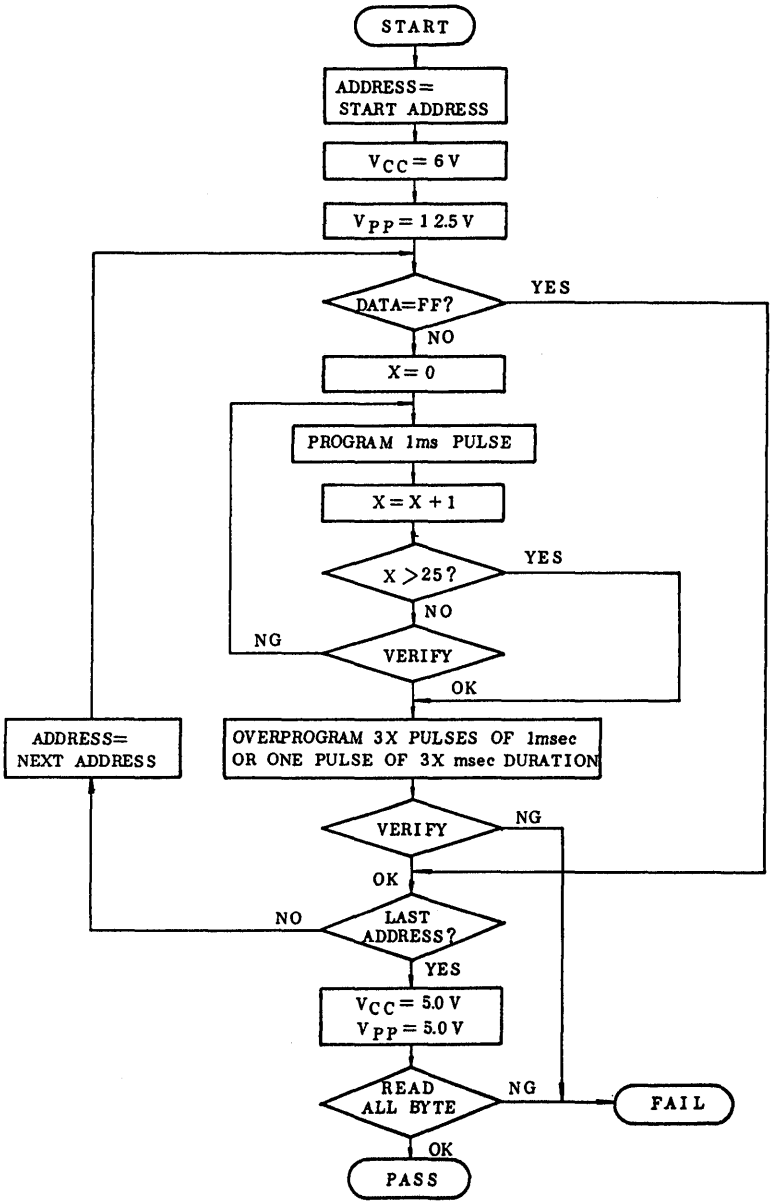
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to Vpp terminal, a high level $\overline{CE}$ input inhibits the TC57256AD from being programmed.
Programming of two or more TC57256AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.
The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)
After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57256AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57256AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TC57256AD.

PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

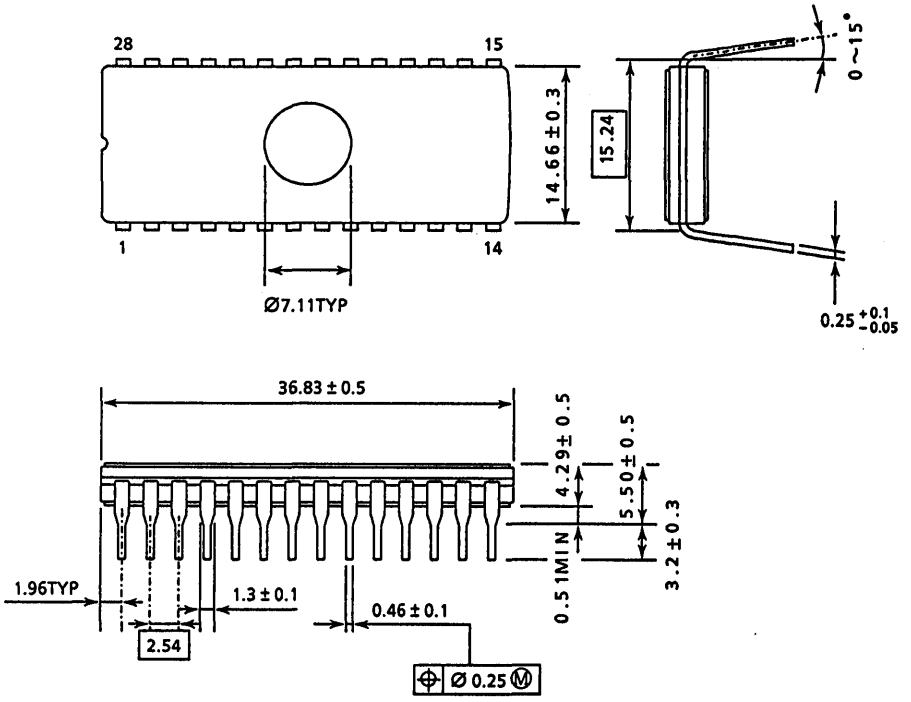
Notes: A9=12V±0.5V

A1∿A8, A10∿A14, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS

WDIP28-G-600A

Unit : mm



65,536 WORDS x 8 BITS CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

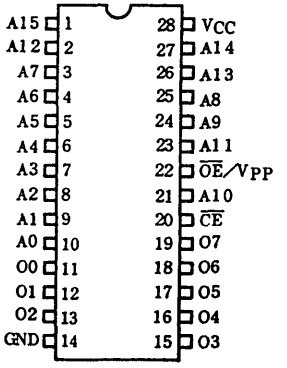
DESCRIPTION

The TC57512AD is a 65,536 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57512AD's access time is 150ns/200ns, and the TC57512AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/6.7MHz and standby current to 100μA. For program operation, the programming is achieved by using the high speed programming mode. TC57512AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

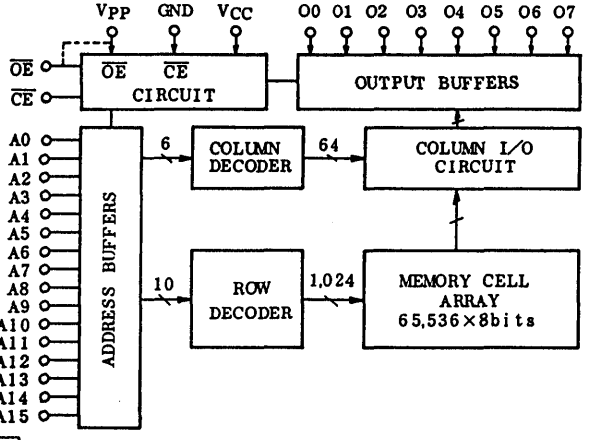
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Fast access time:
  TC57512AD-15 150ns
  TC57512AD-20 200ns
- Low power dissipation
  Active : 30mA/6.7MHz
  Standby: 100μA
- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A15	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$/VPP	Output Enable Input / Program Supply Voltage
VCC	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$/VPP (22)	VCC (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	VPP	6V 1)	Data In	Active
Program Inhibit	H	VPP	2)	High Impedance	
Program Verify	L	L	6.25V	Data Out	

*: H or L

1): HIGH SPEED PROGRAMMING MODE I
2): HIGH SPEED PROGRAMMING MODE II

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C•sec
T_{STG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57512AD-15/TC57512AD-20
Ta	Operating Temperature	-40 ∿ 85°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4 ∿ V_{CC}		-	-	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}$=0V	f=6.7MHz	-	-	30	mA
I_{CCO2}		I_{OUT}=0mA	f=1MHz	-	-	15	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V.		-	-	100	μA
V_{IH}	Input High Voltage	-		2.2	-	V_{CC}+0.3	V
V_{IL}	Output Low Voltage	-		-0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0 ∿ V_{CC}+0.6		-	-	±10	μA

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TC57512AD-15		TC57512AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	150	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	70	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	0	-	ns

A.C. TEST CONDITIONS

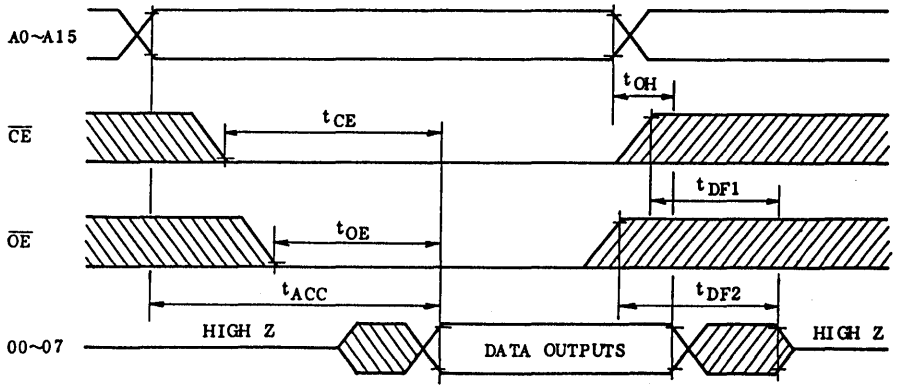
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{IN2}	$\overline{OE}$/Vpp Input Capacitnace	V_{IN}=0V	-	50	60	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM MODE I

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

DC and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}$/V_{PP} Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}$/V_{PP} Hold Time	-	2	-	-	μs
t_{PRT}	$\overline{OE}$/V_{PP} Pulse Rise Time	-	50	-	-	ns
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VR}	$\overline{OE}$/V_{PP} Recovery Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$/V_{PP}=V_{PP}	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}$/V_{PP}=V_{IL}	-	-	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$/V_{PP}=V_{IL}	-	-	130	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

HIGH SPEED PROGRAM MODE II

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.0	6.25	6.5	V
V_{PP}	V_{PP} Power Supply Voltage	12.5	12.75	13.0	V

DC and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

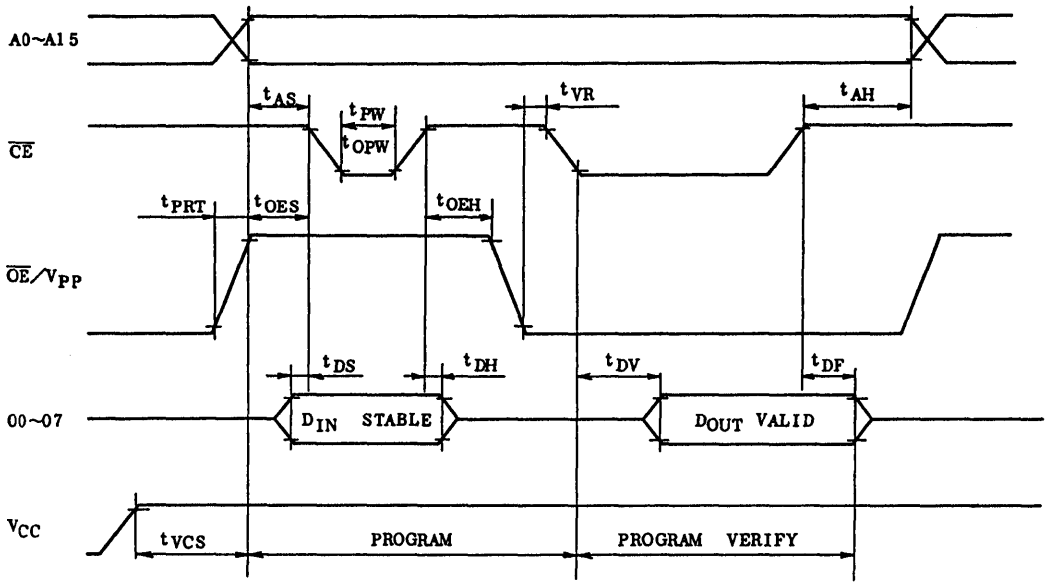
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	-	2	-	-	μs
t_{PRI}	$\overline{OE}/V_{PP}$ Pulse Rise Time	-	50	-	-	ns
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}/V_{PP}=V_{PP}$	0.095	0.1	0.105	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	-	-	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	-	-	130	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAMMING MODE I (V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)
HIGH SPEED PROGRAMMING MODE II (V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5±0.5V or V_{PP}=12.75±0.25V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57512AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (ultraviolet light intensity [w/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [w•sec/cm^2]. When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm^2] × (20 × 60) [sec] ≒ 15 [w•sec/cm^2].) The TC57512AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000 ∿ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57512AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=-40 ∿ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V[1)]	6V[1)]	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L	12.75V[2)]	6.25V	Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}, 1); HIGH SPEED PROGRAM MODE I, 2); HIGH SPEED PROGRAM MODE II

READ MODE

The TC57512AD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC57512AD's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57512AD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC57512AD is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57512AD are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC57512AD is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 12.5V or 12.75V and $\overline{CE}$ is at TTL-Low level. The TC57512AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}/V_{PP}$ at V_{IL} and $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V or +12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC57512AD from being programmed. Programming of two or more TC57512AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

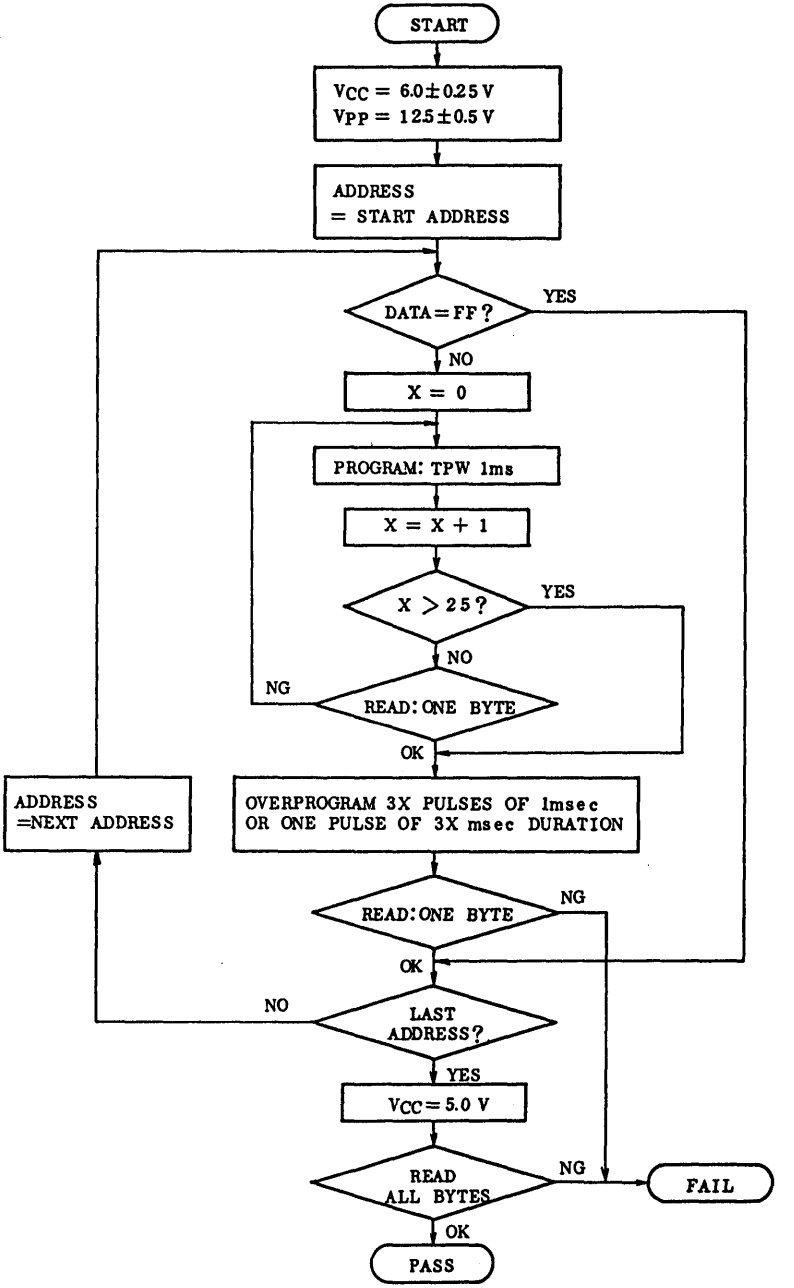
This high speed programming mode I is performed at V_{CC}=6.0V and $\overline{OE}/V_{PP}$=12.5V.
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
After correctly programming the selected address, the additional program pulse with pulse width 3 times that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with V_{CC}=5V.

HIGH SPEED PROGRAM MODE II

The program time can be greatly decreased by using this high speed programming mode II. This high speed programming mode II is performed at V_{CC}=6.25V and $\overline{OE}/V_{PP}$=12.75V.
The programming is achieved by applying a single TTL low level 0.1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
When programming has been completed, the data in all addresses should be verified with V_{CC}=5V.

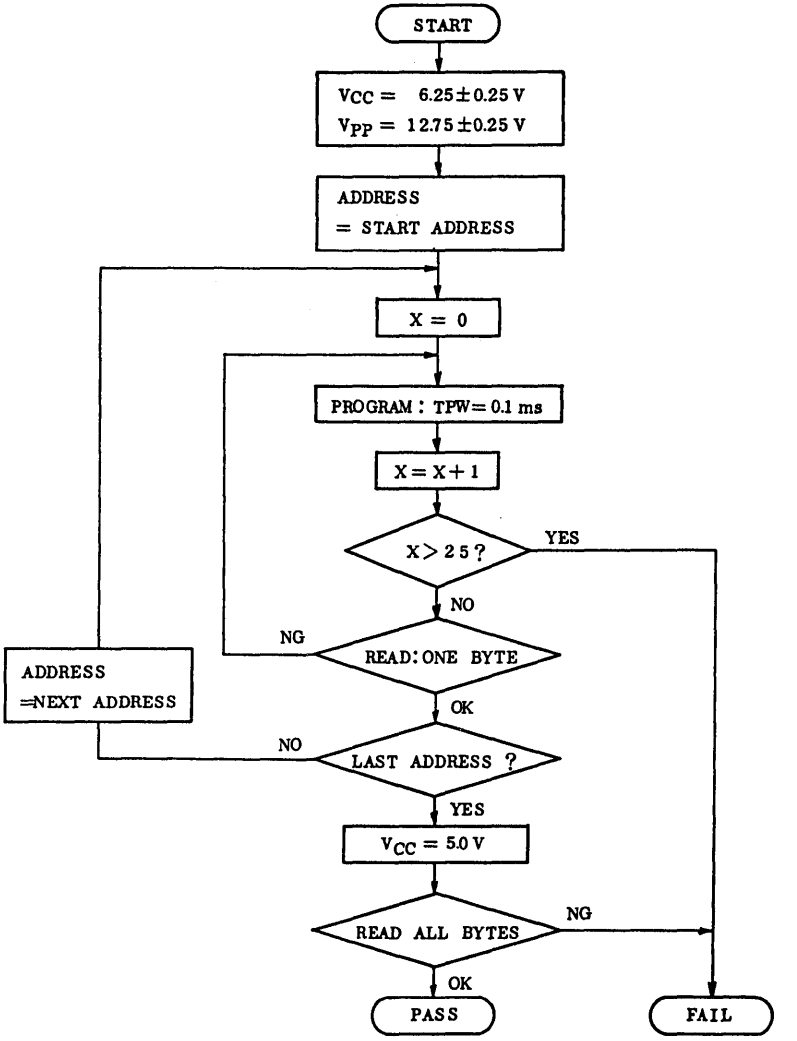
HIGH SPEED PROGRAM MODE I

FLOW CHART



HIGH SPEED PROGRAM MODE II

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57512AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57512AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TC57512AD.

PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

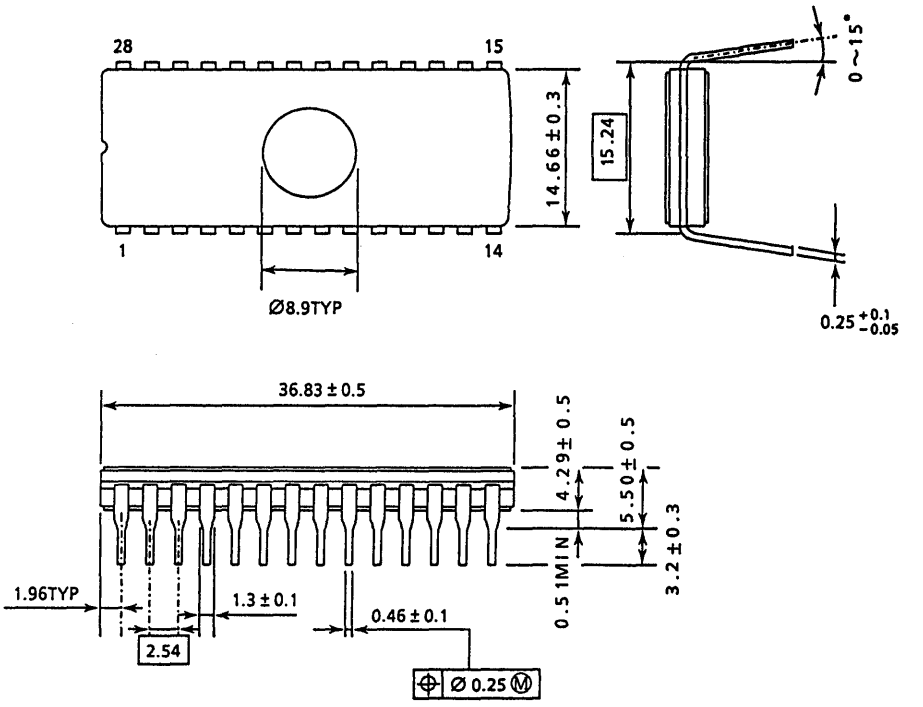
Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A15, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS

WDIP28-G-600

Unit : mm



131,072 WORD × 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC571000AD / TC571001AD is a 131,072 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571000AD is JEDEC standard pin configuration and the TC571001AD is compatible with 28 pin 1M bit Mask ROM. Both products are packed in 32 pin standard cerdip package.

The TC571000AD / TC571001AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 30mA / 8.3MHz and access time of 120ns / 150ns.

The programming times of the TC571000AD / TC571001AD except overhead times of EPROM programmer is only 14 seconds by using the high speed programming algoritim.

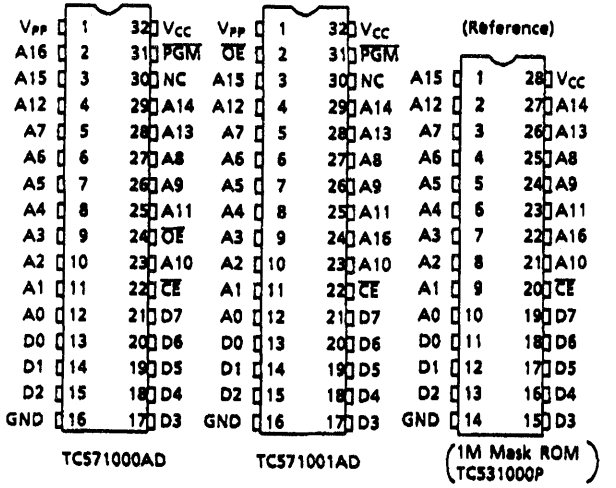
FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Access time

	-12	-150
V_{CC}	5V ± 5%	5V ± 10%
t_{ACC}	120ns	150ns

- Low power dissipation
  Active : 30mA / 8.3MHz
  Standby: 100μA
- Wide operating temperature range : 0~70°C
- Single 5V power supply
- Full static operation
- High speed programming operation : t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin : TC571000AD
- 1M MROM compatible : TC571001AD
- Standard 32 pin DIP cerdip package

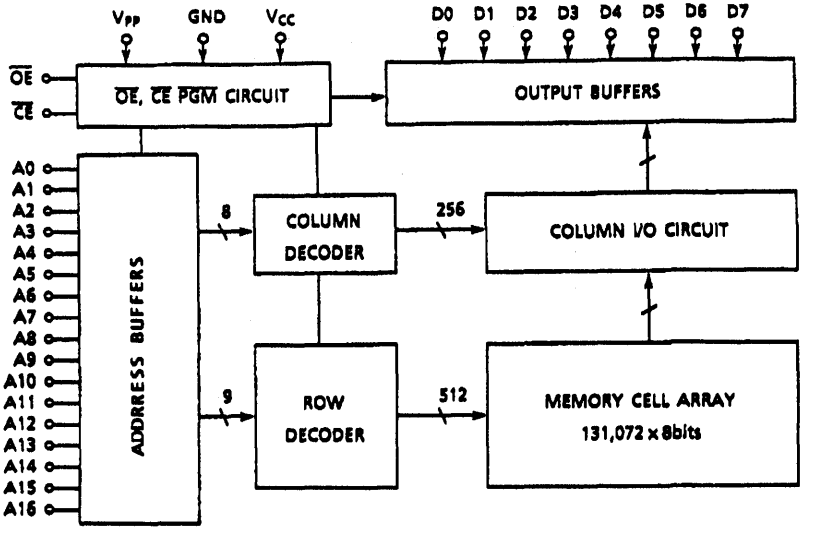
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A16	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	PGM	CE	OE	Vpp	Vcc	D0~D7	Power
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6~V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260·10	°C·sec
T_{STRG}	Storage Temperature	-65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC571000AD/1001AD-12		TC571000AD/1001AD -150		UNIT
		MIN.	MAX.	MIN.	MAX.	
V_{IH}	Input High Voltage	2.2	$V_{CC}+0.3$	2.2	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	-0.3	0.8	-0.3	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.25	4.50	5.50	V
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC}-0.6$	$V_{CC}+0.6$	$V_{CC}-0.6$	$V_{CC}+0.6$	V

DC AND OPERATING CHARACTERISTICS (Ta=0~70°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$		–	–	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}=0V$	f=8.3MHz	–	–	30	mA
I_{CCO2}		$I_{OUT}=0mA$	f=1MHz	–	–	10	
I_{CCS1}	Standby Current	$\overline{CE}=V_{IH}$		–	–	1	mA
I_{CCS2}		$\overline{CE}=V_{CC}-0.2V$		–	–	100	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$		2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$		–	–	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=V_{CC}\pm0.6V$		–	–	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4V\sim V_{CC}$		–	–	10	μA

AC CHARACTERISTICS (Ta=0~70°C, $V_{PP}=V_{CC}\pm0.6V$)

SIMBOL	PARAMETER	TC571000AD/1001AD-12		TC571000AD/1001AD -150		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	–	120	–	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	120	–	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	60	–	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	–	60	–	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	50	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	50	0	60	ns
t_{OH}	Output Data Hold Time	0	–	0	–	ns

TC571000AD/TC571001AD-12 are satisfied with the specification of TC571000AD/TC571001AD-150.

AC TEST CONDITIONS

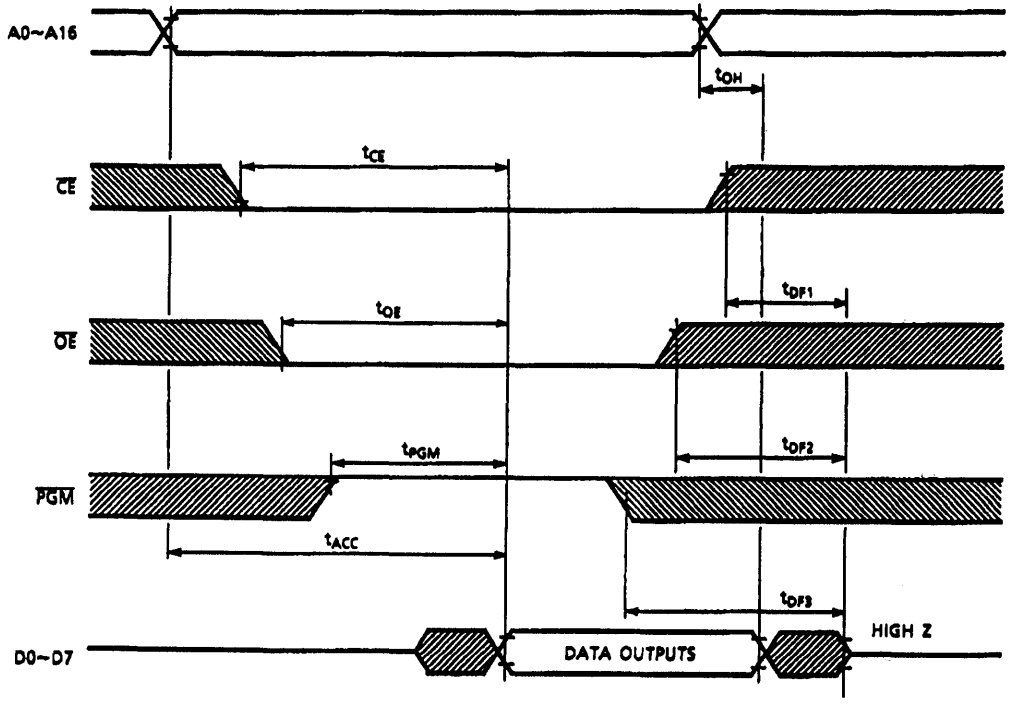
- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	-	4	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	10	12	

* This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS ($Ta=25\pm5°C, V_{CC}=6.25V\pm0.25V, Vpp=12.75V\pm0.25V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C, V_{CC}=6.25V\pm0.25V, Vpp=12.75V\pm0.25V$)

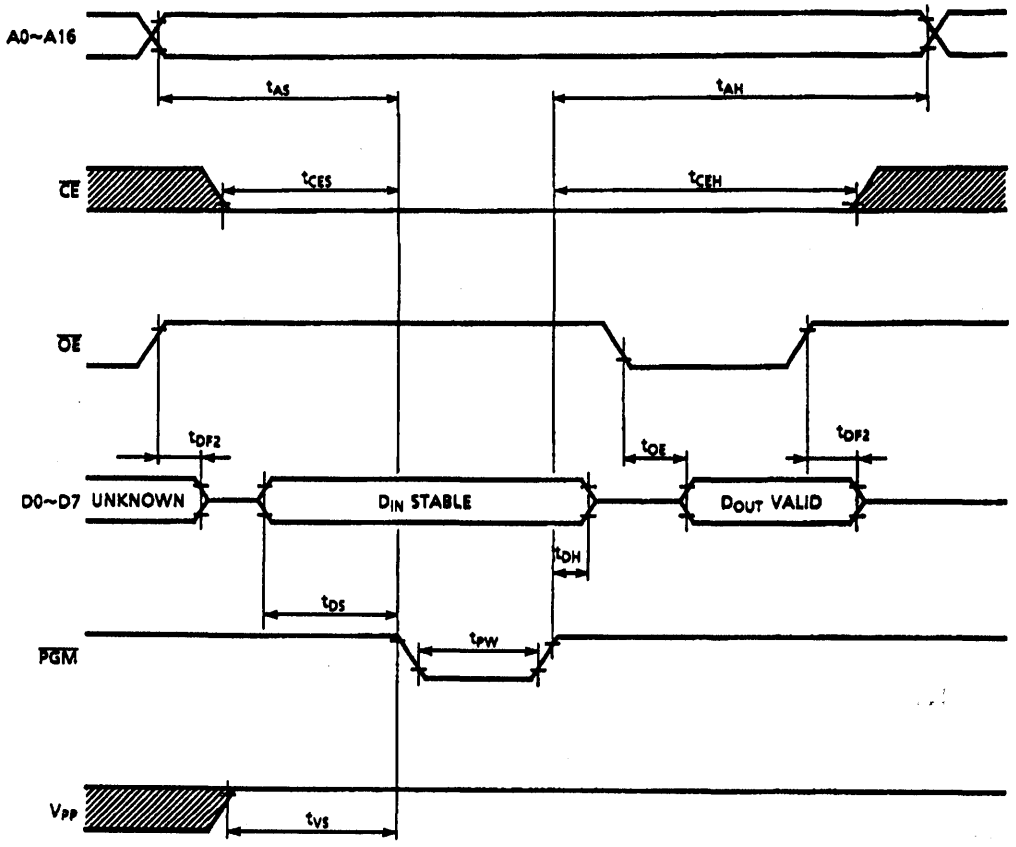
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Set up Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Set up Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	-	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	-	-	-	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	-	-	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation.
So the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC571000AD / TC571001AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity [w/cm^2]×exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000[μw/cm^2]×(20×60) [sec.] ≈15 [w·sec/cm^2].)

The TC571000AD / TC571001AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC571000AD / TC571001AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN		$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	POWER
Read Operation (Ta = 0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselet	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
Program Operation (Ta = 25 ± 5°C)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC571000AD/TC571001AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data will be valid at the output after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$. And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC571000AD/TC571001AD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC571000AD/TC571001AD is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC571000AD/TC571001AD is in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The levels required for all inputs are TTL.

The TC571000AD / TC571001AD can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC571000AD/TC571001AD from being programmed.

Programming of two or more EPROM's in inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

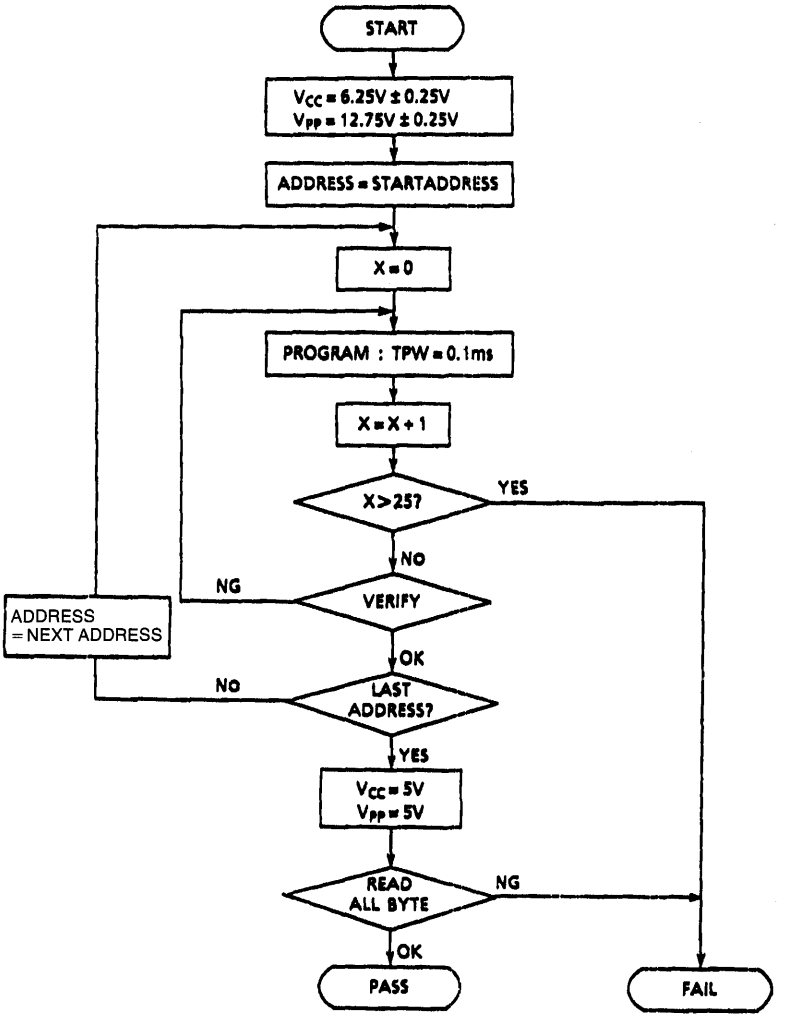
The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC571000AD / TC571001AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC571000AD / TC571001AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC571000AD / TC571001AD.

SIGNATURE \ PINS		A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX Data
Manufacture Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC571000AD	V_{IH}	1	0	0	0	0	1	1	0	86
	TC571001AD		0	0	0	0	0	1	1	1	07

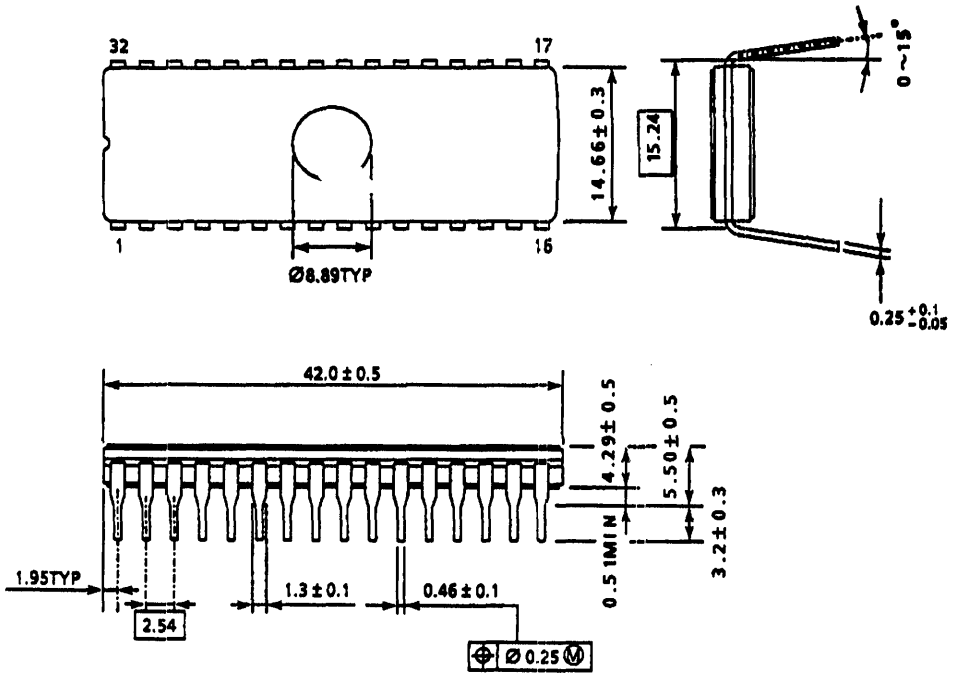
Notes: A9 = 12V ± 0.5V
A1~A8, A10~A16, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

- **Cerdip DIP**

WDIP32-G-600

Unit : mm



1 MEGA BIT (65,536 WORD x 16 BIT)
CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC571024D is a 65,536 word × 16 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571024D is JEDEC standard pin configuration. This product is packaged in 40 pin standard cerdip package.

TC571024D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and lowpower features with a maximum operating current of 40mA/6.7MHz and access time of 150ns/200ns.

The programming times of the TC571024D except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

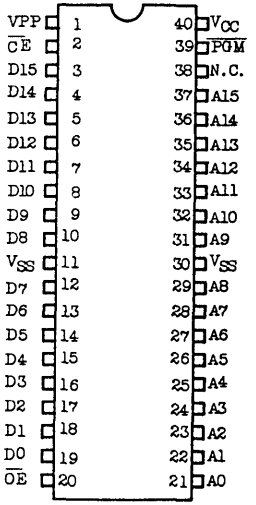
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Fast access time

	TC571024D-15	TC571024D-20	TC571024D-200
Ta	0 ∿ 70°C	-40 ∿ 85°C	
V_{CC}	5V±5%		5V±10%
t_{ACC}	150ns	200ns	

- Low power dissipation
  Active : 40mA/6.7MHz
  Standby: 100μA
- Single 5V power supply
- Full static operation
- High speed programming operation:
  t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 40 pin: TC571024D
- Standard 40 pin DIP cerdip package

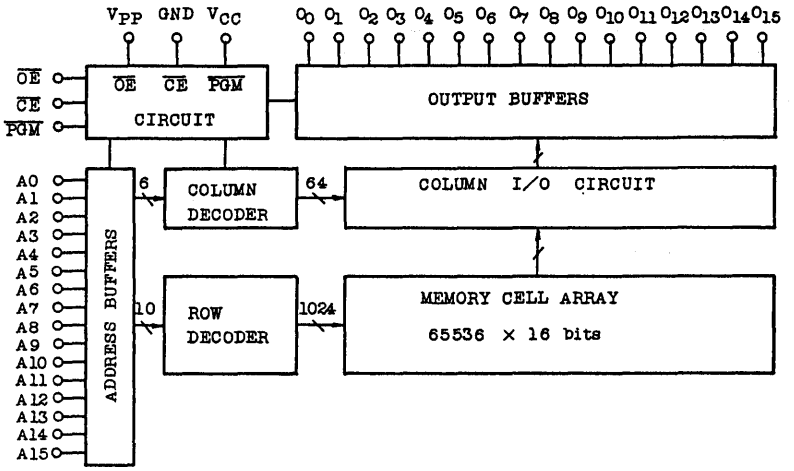
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A15	Address Inputs
D0 ∿ D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	VCC Supply Voltage
V_{PP}	Program Supply Voltage
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	$D_0 \sim D_{15}$	POWER
Read	L	L	H	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*	*			High Impedance	Standby
Program	L	*	L	12.75V	6.25V	Data In	Active
Program Inhibit	H	*	*			High Impedance	
	L	H	H				
Program Verify	L	L	H			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
V_{IN} (A9)	Input Voltage (A9)	-0.6 ∿ 13.5	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 • 10	°C•sec
T_{STRG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC571024D-15	TC571024D-20	TC571024D-200
Ta	Ambient Temperature	0∿70°C	-40∿85°C	
V_{CC}	V_{CC} Power Supply Voltage	5V±5%		5V±10%
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6V∿V_{CC}+0.6V		V_{CC}-0.6V∿V_{CC}+0.6V

D.C. and OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0∿V_{CC}		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$=0V	t_{cycle}=150ns	-	-	40	mA
I_{CC02}		I_{OUT}=0mA	t_{cycle}=1μs	-	-	20	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{IH}	Input High Voltage	-		2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-		-0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=V_{CC}±0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V∿V_{CC}		-	-	±10	μA

A.C. CHARACTERISTICS (V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TC571024D-15		TC571024D-200/-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	150	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	
t_{OH}	Output Data Hold Time	0	-	0	-	

A.C. TEST CONDITIONS

Output Load : 1 TTL Gate and C_L=100pF

Input Pulse Rise and Fall Times : 10ns Max.

Input Pulse Levels : 0.45V to 2.4V

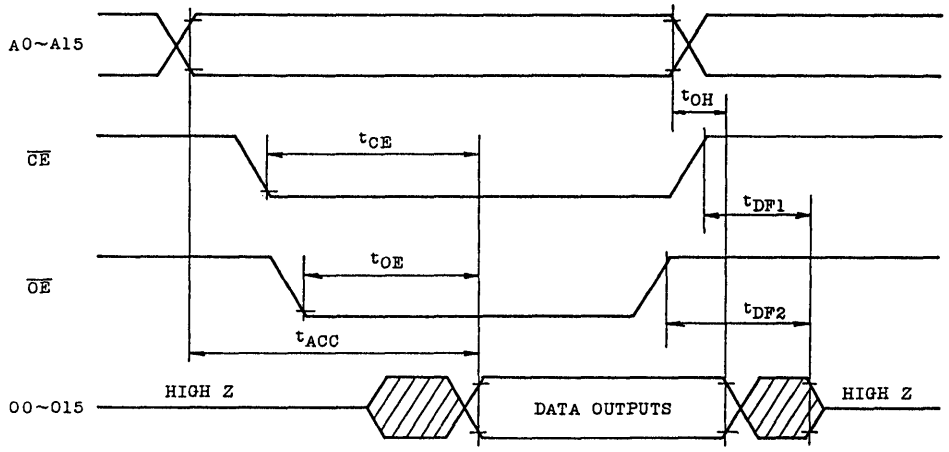
Timing Measurement Reference Level: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	10	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	100	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

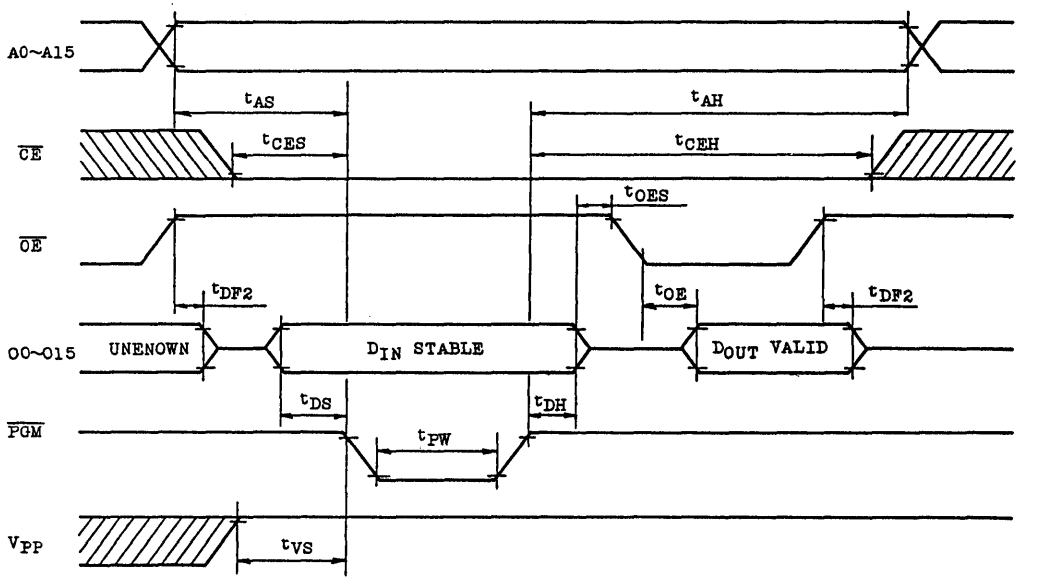
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	Vpp Setup Time	-	2	-	-	μs
T_{PW}	Program Pulse Width	-	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid		-	-	500	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	-	-	150	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2.0	-	-	μs

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with Vpp=12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC571024D erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (Ultraviolet light intensity [W/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [$W \cdot sec/cm^2$].
When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [$\mu W/cm^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [$\mu W/cm^2$] × (20 × 60) [sec] ≅ 15 [$W \cdot sec/cm^2$].)
The TC571024D erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000 ∿ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC571024D six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

	PIN / MODE	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0 ∿ D15	POWER
READ OPERATION	Read	L	L	H	5V	5V	Data Out	Active
	Output Deselect	*	H	*			High Impedance	
	Standby	H	*	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	*	L	12.75V	6.25V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
		L	H	H				
	Program Verify	L	L	H			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC571024D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection.
Assuming in that $\overline{CE}$=$\overline{OE}$=V_{IL} and $\overline{PGM}$=V_{IH}, the output data is valid at the output after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL}, $\overline{PGM}$=V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two or more ROMs can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC571024D has a low power standby mode controlled by the $\overline{CE}$ signal.
By applying a high level to the $\overline{CE}$ input, the TC571024D is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC571024D are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The levels required for all inputs are TTL. The TC571024D can be programmed any location at anytime——either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

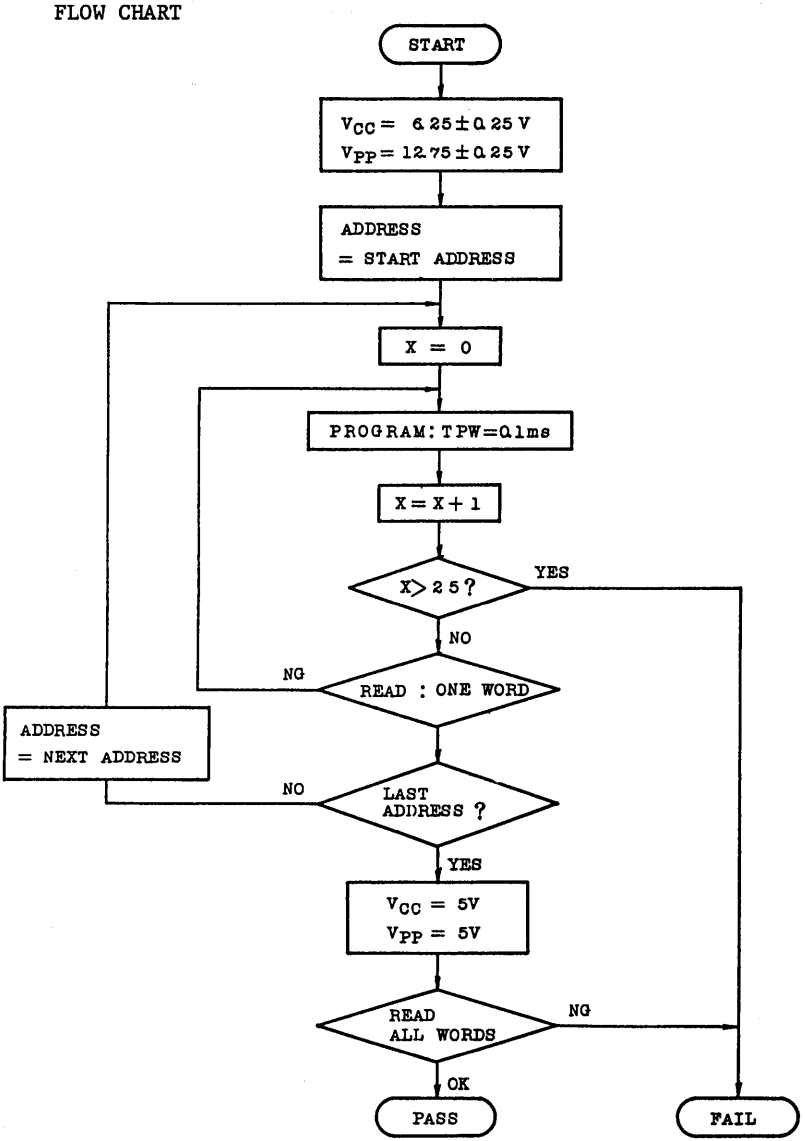
Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC571024D from being programmed.
Programming of two or more EPROMS in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC}=6.25V and $\overline{PGM}$=V_{IH}.
The programming is achieved by applying a single TTL low level 0.1 ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC571024D which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC571024D by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of (O_7).

The following table shows electric signature of TC571024D.

PINS / SIGNATURE	A_0	O_{15}	O_{14}	O_{13}	O_{12}	O_{11}	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	HEX. DATA
Manufacture Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	0	0	0	0	1	0	0	0	**08

Notes: A9=12V±0.5V, A1 ∿ A8, A10 ∿ A15, $\overline{CE}$, $\overline{OE}=V_{IL}$, $\overline{PGM}=V_{IH}$ *: Don't Care

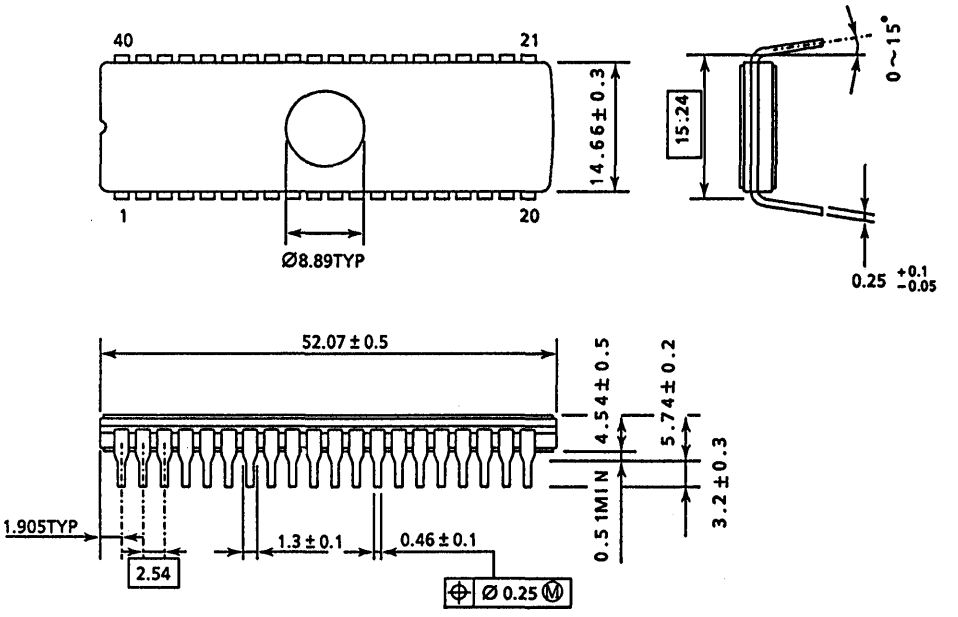
D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{ID}	A9 Auto Select Voltage	11.5	12.0	12.5	V

OUTLINE DRAWINGS

WDIP40-G-600

単位：mm



524,288 WORD × 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC574000D is a 524,288 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC574000D's access time is 120ns, and the TC574000D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

Advanced CMOS technology reduces the maximum active current to 60mA / 8.3MHz and standby current to 100μA. For program operation, the programming is achieved by using the high speed programming mode. TC574000D is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

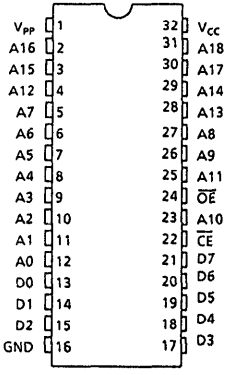
FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Access time

	-12	-120	-150
V_{CC}	5V ± 5%	5V ± 10%	
Temp	0°C~70°C		
t_{ACC}	120ns		150ns

- Low power dissipation
  Active : 60mA / 8.3MHz
  Standby: 100μA (Ta = 70°C)
- High speed programming operation
- Single 5V power supply
- Full static operation
- Input and output TTL compatible
- JEDEC standard 32 pin
- Standard 32 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)

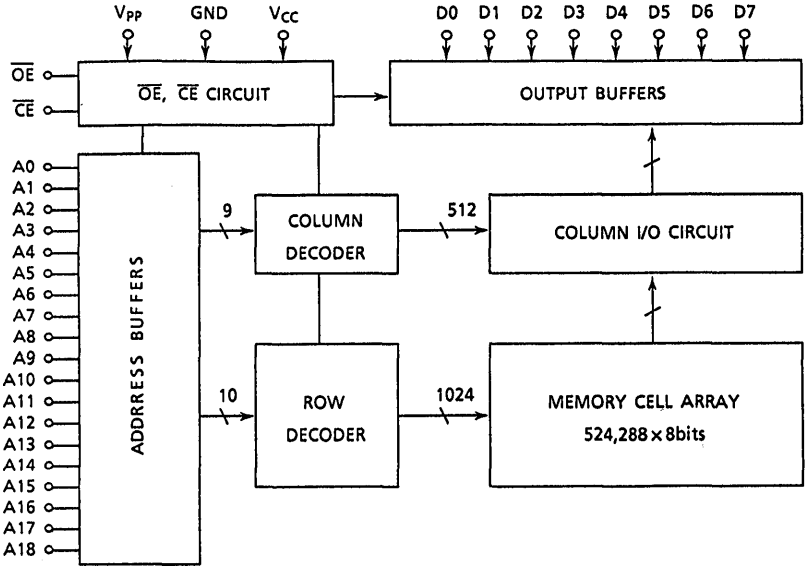


TC574000D

PIN NAMES

A0~A18	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	Power
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.50V	6.25V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{IN} (A9)	Input Voltage (A9)	−0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	−0.6~V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~125	°C
T_{opr}	Operating Temperature	0~70	°C

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC574000D-12	TC574000D-120/150
V_{IH}	Input High Voltage	2.2V~V_{CC}+0.3V	2.2V~V_{CC}+0.3V
V_{IL}	Input Low Voltage	-0.3V~0.8V	0.3V~0.8V
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6V~V_{CC}+0.6V	V_{CC}-0.6V~V_{CC}+0.6V

DC AND OPERATING CHARACTERISTICS (Ta=0~70°C)

SIMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		-	-	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}$=V_{IL}, I_{OUT}=0mA	f=8.3MHz	-	-	60	mA
			f=6.7MHz	-	-	50	
I_{CCO2}			f=1MHz	-	-	15	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=V_{CC}±0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V~V_{CC}		-	-	±10	μA

AC CHARACTERISTICS (Ta=0~70°C, V_{PP}=V_{CC}±0.6V)

SIMBOL	PARAMETER	TEST CONDITION	TC574000D-12/120		TC574000D-150		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	120	-	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	120	-	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	60	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	50	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	0	-	ns

AC TEST CONDITIONS

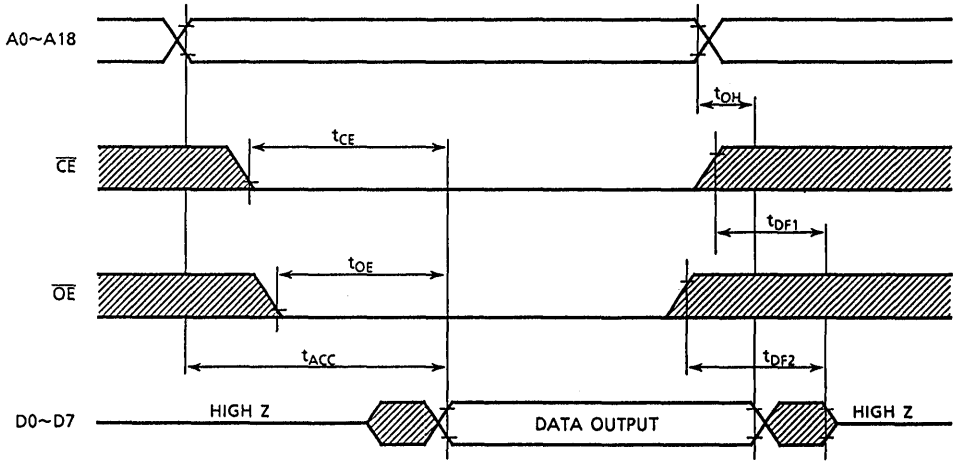
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	-	9	PF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	13	

*This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPERATING CHARACTERISTICS

($Ta=25\pm5°C, V_{CC}=6.25V\pm0.25V, Vpp=12.50V\pm0.30V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=12.8V$	–	–	50	mA

AC PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.50V\pm0.30V$)

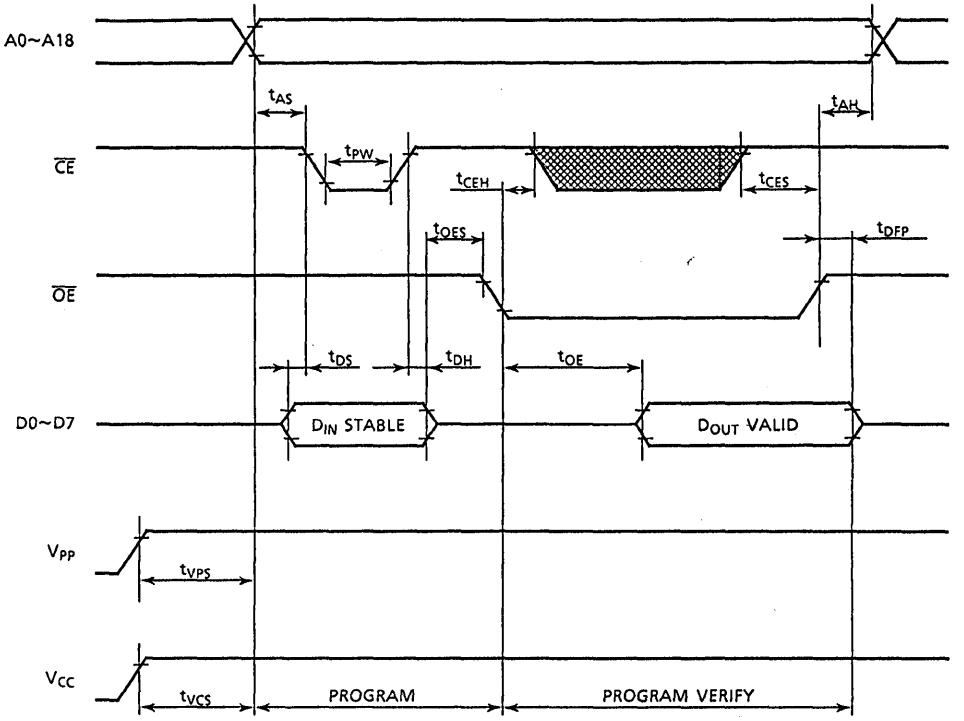
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	μs
t_{OES}	$\overline{OE}$ Set up Time	–	2		–	μs
t_{DS}	Data Set up Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VPS}	V_{PP} Set up Time	–	2	–	–	μs
t_{VCS}	V_{CC} Set up Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	–	–	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	–	–	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with VPP=12.50V may cause permanent damage to the device.

3. The VPP supply voltage is permitted up to 14V for program operation.
So the voltage over 14V should not be applied to the VPP terminal.
When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC574000D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity [w/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [w · sec/cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of lcm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the intergrated dose is 12000[μw/cm^2]× (20×60) [sec.] ≃15 [w · sec/cm^2].)

The TC574000D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC902-are available.

OPERATION INFORMATION

The TC574000D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (22)	$\overline{OE}$ (24)	V_{PP} (1)	V_{CC} (32)	D0~D7 (13~15, 17~21)	POWER
Read Operation (Ta = 0~70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselet	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta = 25 ± 5°C)	Program	L	H	12.50V	6.25V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC574000D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC574000D's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574000D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC574000D is placed in the standby mode which reduces the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC574000D are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC574000D is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at Low under $\overline{OE}=V_{IH}$.

The TC574000D can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ and $\overline{OE}$ input inhibits the TC574000D from being programmed.

Programming of two or more TC574000D's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a low level program pulse is applied to the $\overline{CE}$ of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$.

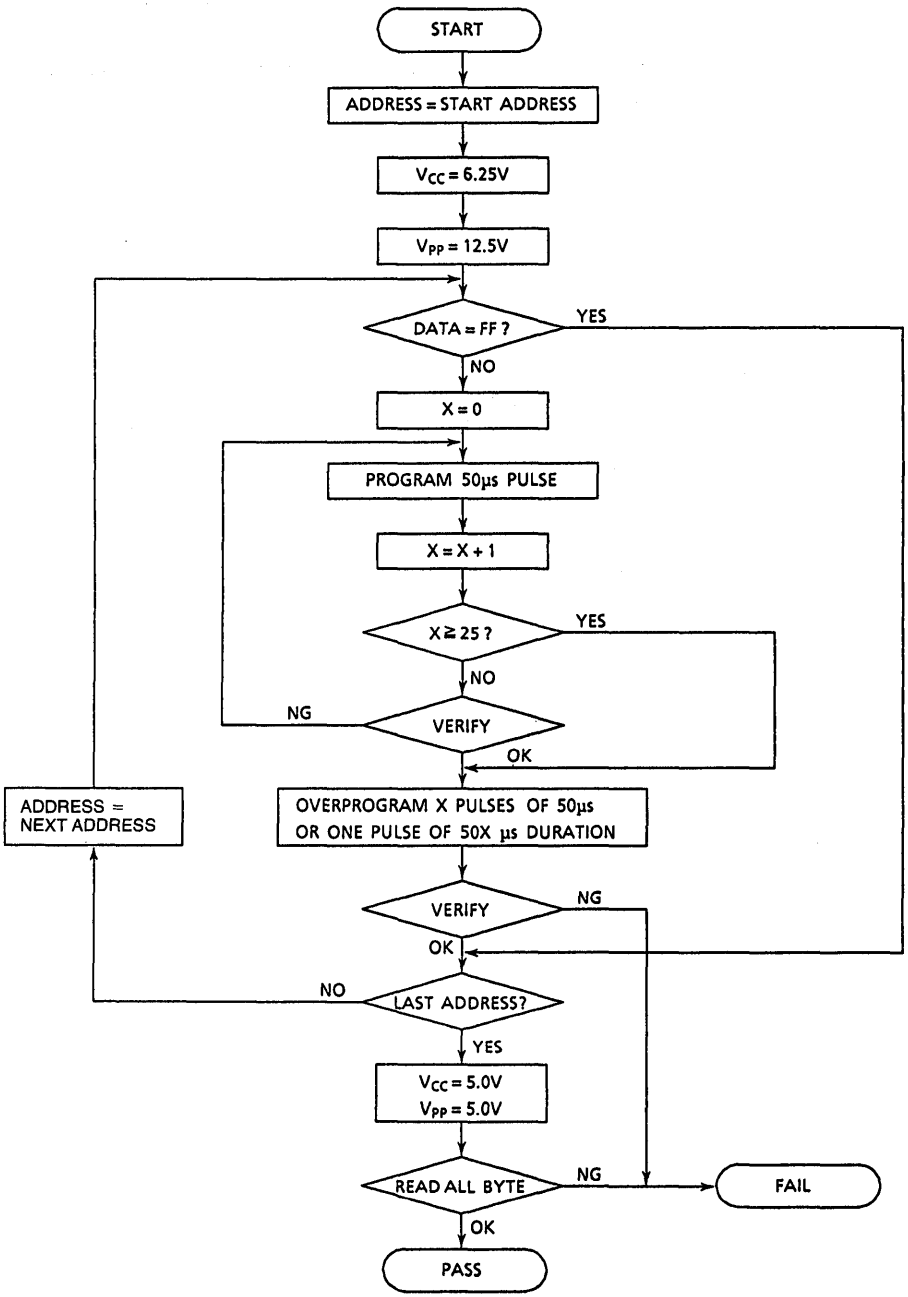
The programming is achieved by applying a single low level 50μs pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 50μs is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574000D which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC574000D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC574000D.

PINS / SIGNATURE	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	0	1	1	0	0	8C

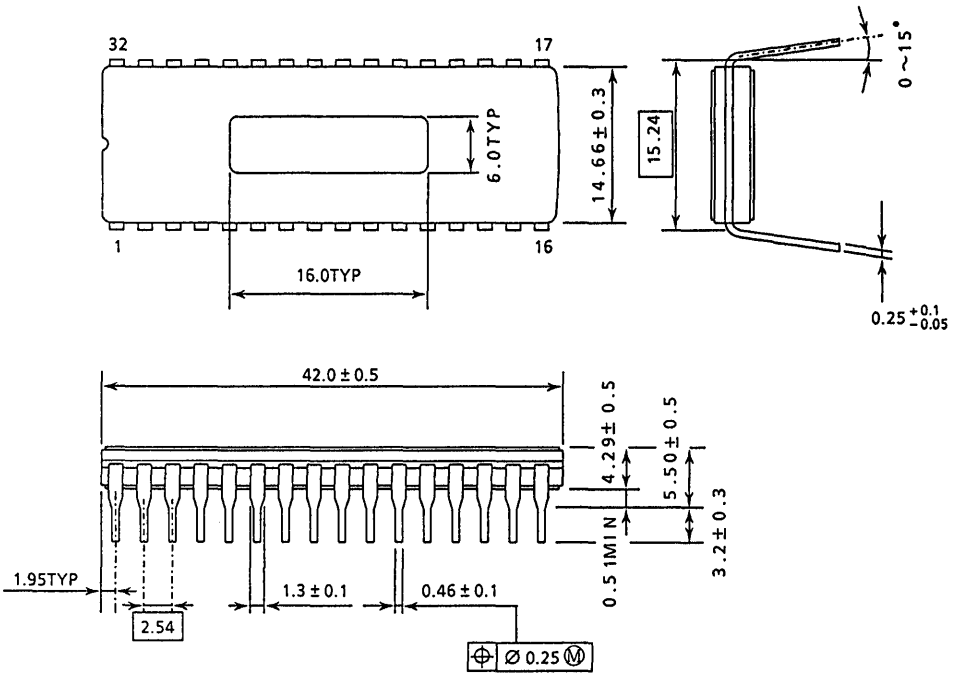
Notes: A9=12V±0.5V
A1~A8, A10~A18, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS

- Cerdip DIP

WDIP32-G-600A

Unit : mm



524,288 WORD×8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC574000DI is a 524,288 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC574000DI's access time is 150ns, and the TC574000DI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

Advanced CMOS technology reduces the maximum active current to 50mA/6.7MHz and standby current to 100μA. For program operation, the programming is achieved by using the high speed programming mode. TC574000DI is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

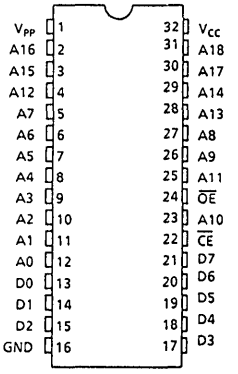
FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Access time

	-150	-200
V_{CC}	5V ± 10%	
Temp	-40~85°C	
t_{ACC}	150ns	200ns

- Low power dissipation
  Active : 50mA/6.7MHz
  Standby: 100μA (Ta=85°C)
- High speed programming operation
- Single 5V power supply
- Full static operation
- Input and output TTL compatible
- JEDEC standard 32 pin
- Standard 32 pin DIP cerdip package

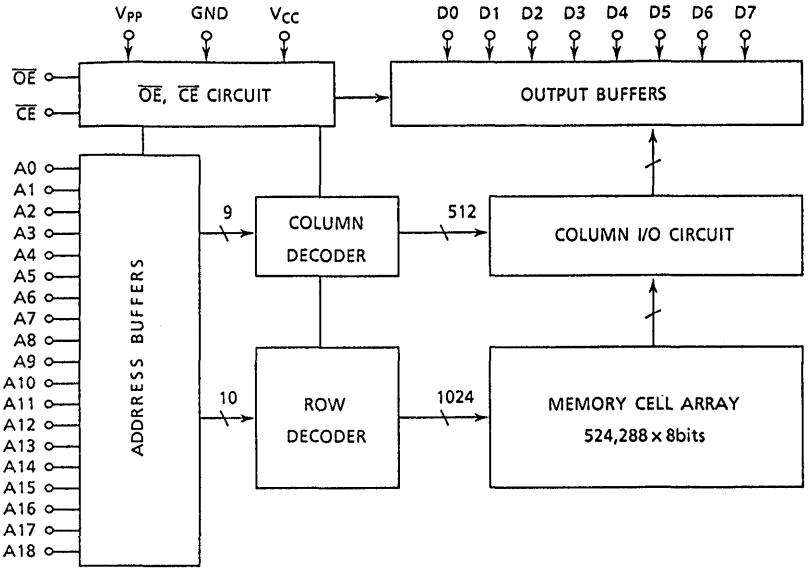
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A18	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	Power
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.50V	6.25V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~125	°C
T_{opr}	Operating Temperature	−40~85	°C

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	V

DC AND OPERATING CHARACTERISTICS (Ta = −40~85°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$		–	–	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}=V_{IL}$	f = 6.7MHz	–	–	50	mA
I_{CCO2}		I_{OUT} = 0mA	f = 1MHz	–	–	15	
I_{CCS1}	Standby Current	$\overline{CE}=V_{IH}$		–	–	1	mA
I_{CCS2}		$\overline{CE}=V_{CC}-0.2V$		–	–	100	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$		2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$		–	–	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=V_{CC}\pm0.6V$		–	–	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4V\sim V_{CC}$		–	–	10	μA

AC CHARACTERISTICS (Ta = −40~85°C, $V_{PP}=V_{CC}\pm0.6V$)

SIMBOL	PARAMETER	TEST CONDITION	TC574000DI-150		TC574000DI-200		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	–	150	–	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	–	150	–	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	–	70	–	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	–	0	–	ns

AC TEST CONDITIONS

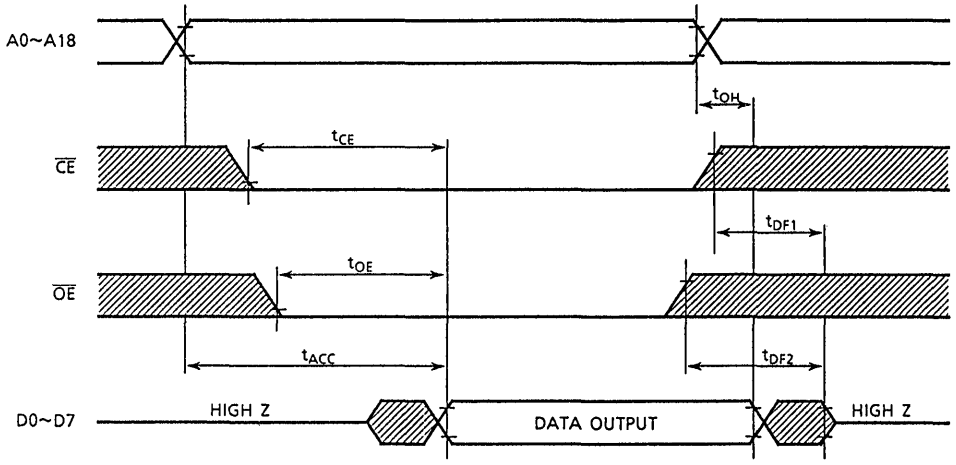
- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	-	9	PF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	13	

* This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPERATING CHARACTERISTICS ($Ta=25\pm5°C, V_{CC}=6.25V\pm0.25V, Vpp=12.50V\pm0.30V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=12.8V$	–	–	50	mA
V_{ID}	A9 Auto Select Voltage	–	11.5	12.0	12.5	V

AC PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6.25V\pm0.25V$, $Vpp=12.50V\pm0.30V$)

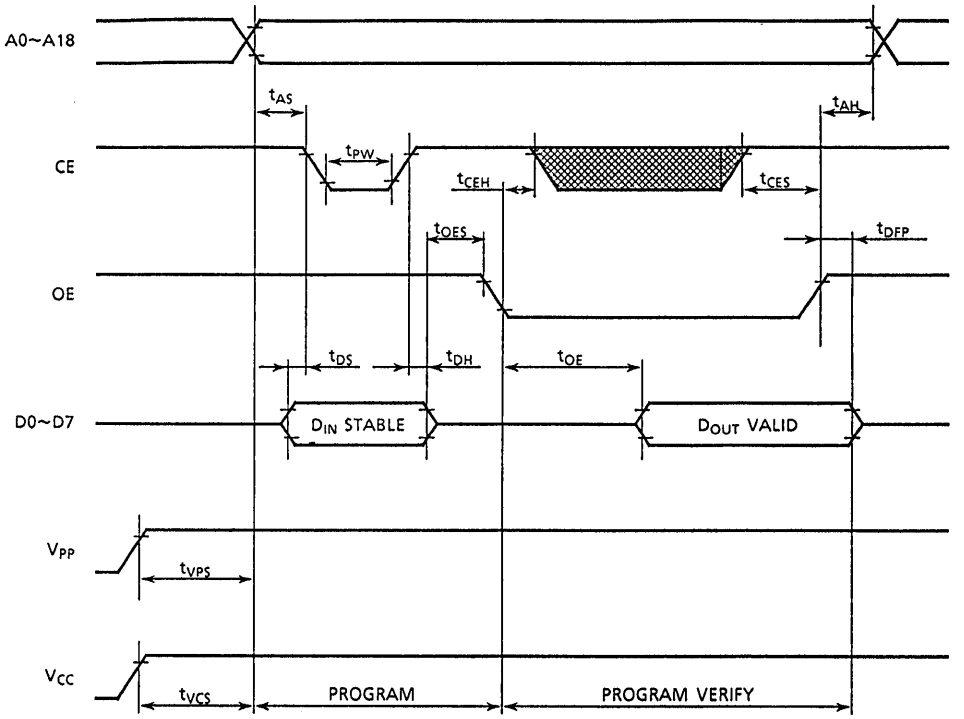
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	μs
t_{OES}	$\overline{OE}$ Set up Time	–	2		–	μs
t_{DS}	Data Set up Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VPS}	V_{PP} Set up Time	–	2	–	–	μs
t_{VCS}	V_{CC} Set up Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	–	–	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	–	–	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



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The integrated dose (ultraviolet light intensity [w/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [w · sec/cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of lcm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 1200∅[μw/cm^2] × (20×60) [sec.] ≃15 [w · sec/cm^2].)

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OPERATION INFORMATION

The TC574000DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (22)	$\overline{OE}$ (24)	V_{PP} (1)	V_{CC} (32)	D0~D7 (13~15, 17~21)	POWER
Read Operation (Ta = −40~85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselet	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta = 25 ± 5°C)	Program	L	H	12.50V	6.25V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC574000DI has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC574000DI's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574000DI has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC574000DI is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC574000DI are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC574000DI is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at Low under $\overline{OE}=V_{IH}$.

The TC574000DI can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ and $\overline{OE}$ input inhibits the TC574000DI from being programmed.

Programming of two or more TC574000DI's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a low level program pulse is applied to the $\overline{CE}$ of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up is the high speed programming mode when the programming voltage (+12.50V) is applied to the V_{PP} terminal with V_{CC}=6.25V.

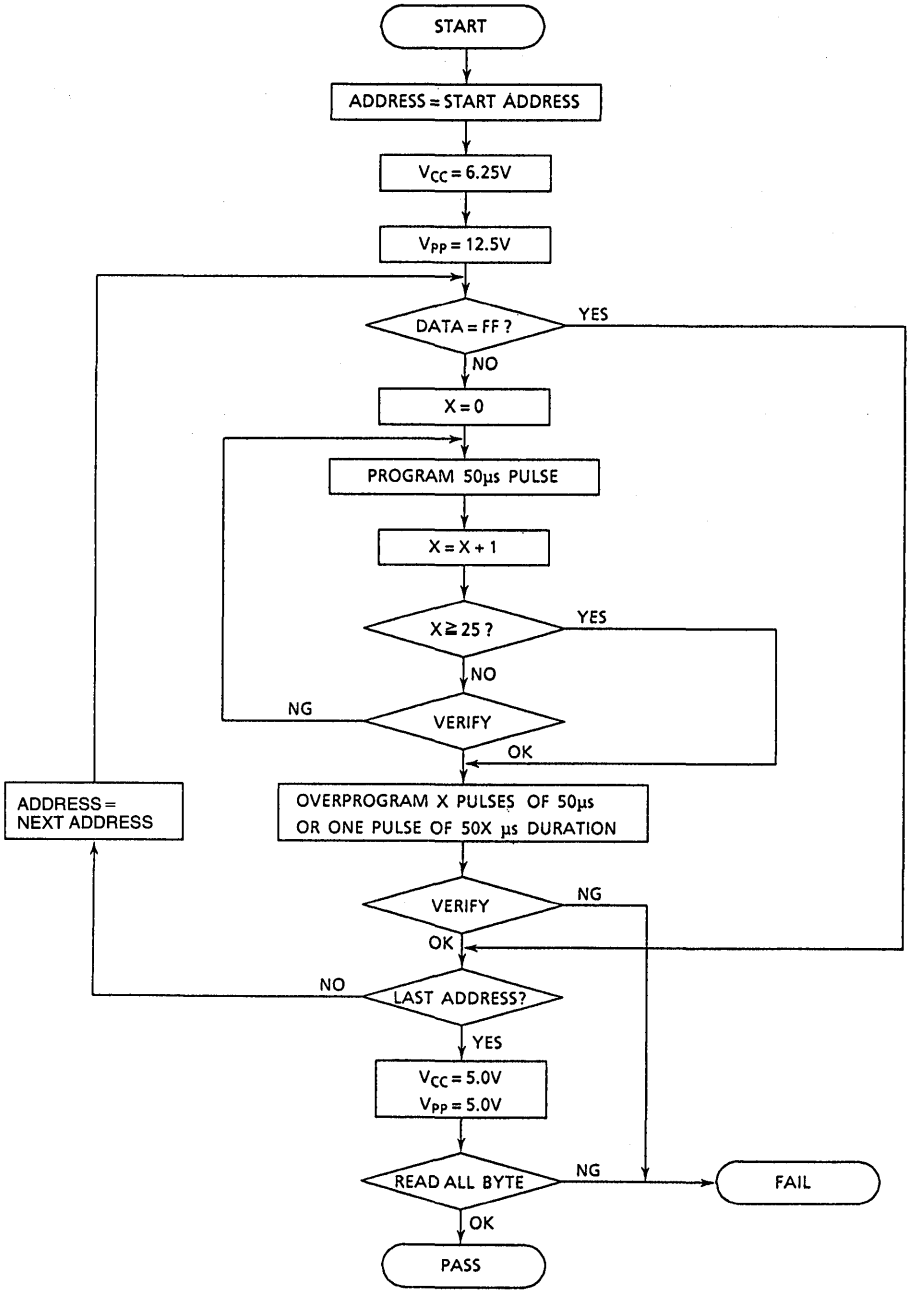
The programming is achieved by applying a single low level 50μs pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574000DI which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC574000DI by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC574000DI.

PINS / SIGNATURE	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	0	1	1	0	0	8C

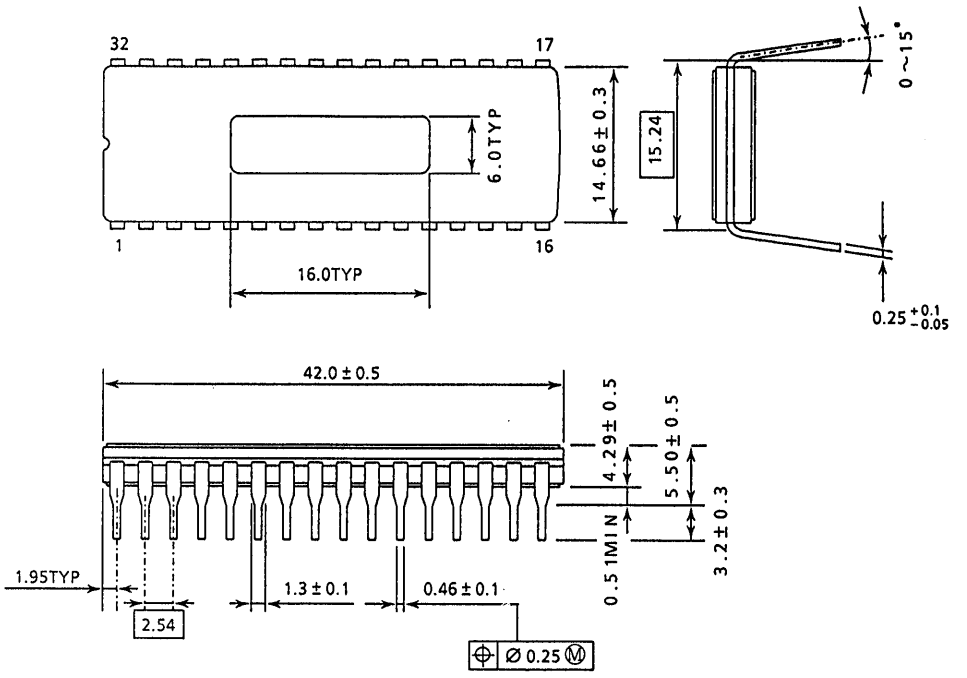
Notes: A9 = 12V ± 0.5V
A1~A8, A0~A18, $\overline{CE}$, $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS

- Cerdip DIP

WDIP32-G-600

Unit : mm



4MEGA BIT (262,144 WORD × 16BIT / 524,288 WORD × 8BIT)
CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

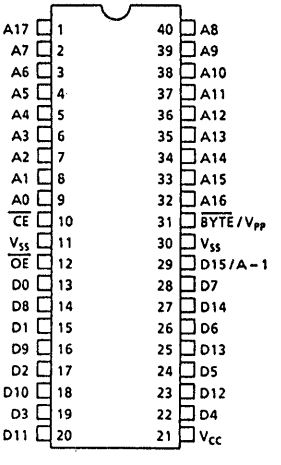
The TC574200D is a 4,194,304 bit CMOS ultraviolet light erasable and electrically programmable read only memory. It is organized as 256K words of 16 bit or 512K words of 8 bit. The TC574200D is compatible with 40 pin 4M bit Mask ROM. This product is packed in 40 pin standard cerdip package. The TC574200D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with access time of 120ns / 150ns / 200ns and a maximum operating current of 60mA / 8.3MHz. The programming time of the TC574200D except overhead times of EPROM programmer is only 28 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
  Memory cell : NMOS
- Fast access time
  (V_{CC} = 5V ± 10%, Ta = 0~70°C)
  TC574200D - 120 : 120ns
  TC574200D - 150 : 150ns
  TC574200D - 200 : 200ns
- Single 5V power supply
- Low power dissipation
  Standby : 100μA
- Full static operation
- Input and output TTL compatible
- Three state output
- High speed programming operation : t_{PW} 50μs
- 4M MROM compatible pinout : TC534200P
- Standard 40 pin DIP cerdip package

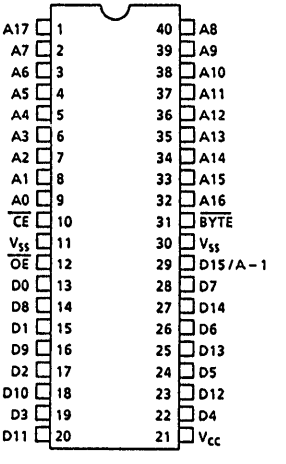
PIN CONNECTION

(TOP VIEW)



TC574200D

(Reference)

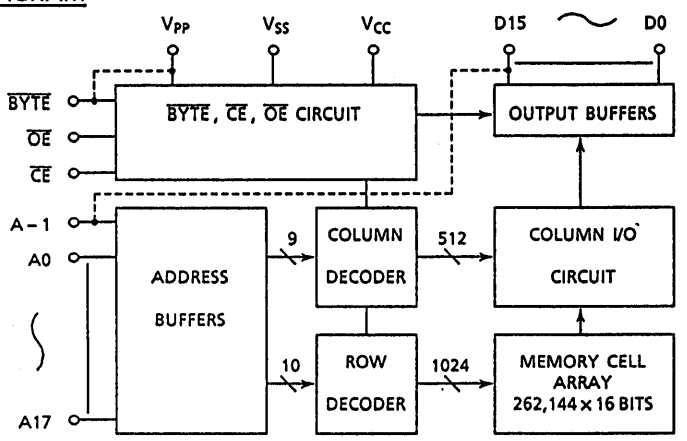


4M Mask ROM
TC534200P

PIN NAMES

A0~A17	Address Input
D0~D14	Output (Input)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A-1	Output (Input) / Address Input
$\overline{BYTE}$/V_{PP}	Word, Byte select Input / Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage
V_{SS}	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$ / V_{PP}	V_{CC}	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance			Standby
			L		High Impedance		*	
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
V_{IN} (A9)	Input Voltage (A9)	-0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	-0.6~V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260·10	°C · sec
T_{STRG}	Storage Temperature	-65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V

D.C. AND OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0V\sim V_{CC}$	-	-	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}=0V$ $I_{OUT}=0mA$ f=8.3MHz	-	-	60	mA
I_{CCO2}		$\overline{CE}=0V$ $I_{OUT}=0mA$ f=1MHz	-	-	30	mA
I_{CCS1}	Standby Current	$\overline{CE}=V_{IH}$	-	-	1	mA
I_{CCS2}		$\overline{CE}=V_{CC}-0.2V$	-	-	100	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=0V\sim V_{CC}+0.6V$	-	-	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4V\sim V_{CC}$	-	-	±10	μA

A.C. CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	-120		-150		-200		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	120	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	120	-	150	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	-	60	-	70	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High Impedance	0	50	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High Impedance	0	50	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	-	0	-	0	-	ns
t_{BT}	$\overline{BYTE}$ to Output Valid	-	120	-	150	-	200	ns
t_{BTD}	$\overline{BYTE}$ to Output in High Impedance	-	50	-	60	-	60	ns

- A.C. TEST CONDITIONS
  - Output Load : 1 TTL Gate and CL = 100PF
  - Input Pulse Rise and Fall Time : 10ns Max
  - Input Pulse Levels : 0.45V and 2.4V
  - Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

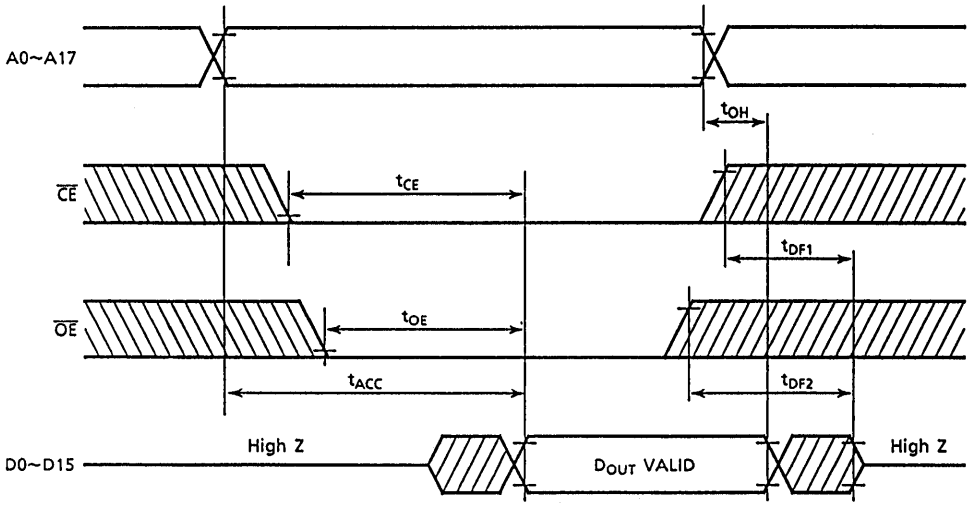
CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	V_{IN} = 0V	-	6	10	pF
C_{IN2}	Input Capacitance ($\overline{BYTE}$ / V_{PP})	V_{IN} = 0V	-	50	60	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	10	12	pF

* This parameter is periodically sampled and is not 100% tested.

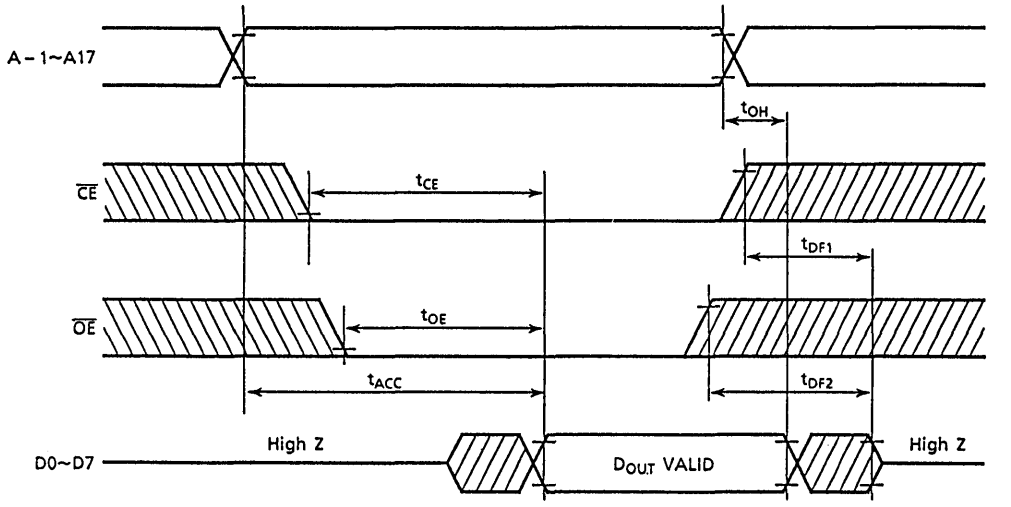
TIMING WAVEFORMS

WORD - WIDE READ MODE



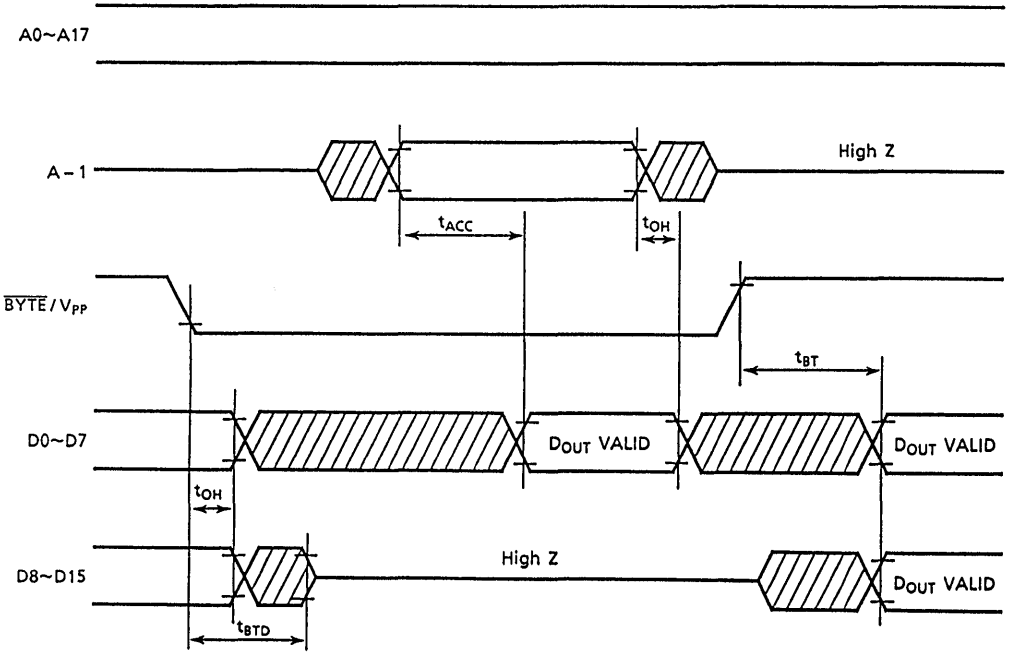
Note: $\overline{BYTE}$ / V_{PP} = V_{IH}

BYTE – WIDE READ MODE



Note: $\overline{BYTE}$ / $V_{PP} = V_{IL}$

$\overline{BYTE}$ TRANSITION



Note: $\overline{CE}$, $\overline{OE} = V_{IL}$

HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

D.C. AND OPERATING CHARACTERISTICS ($Ta = 25 \pm 5°C$, $V_{CC} = 6.25 \pm 0.25V$, $V_{PP} = 12.50 \pm 0.30V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0V \sim V_{CC}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 12.8V$	–	–	100	mA

A.C. PROGRAMMING CHARACTERISTICS ($Ta = 25 \pm 5°C$, $V_{CC} = 6.25 \pm 0.25V$, $V_{PP} = 12.50 \pm 0.30V$)

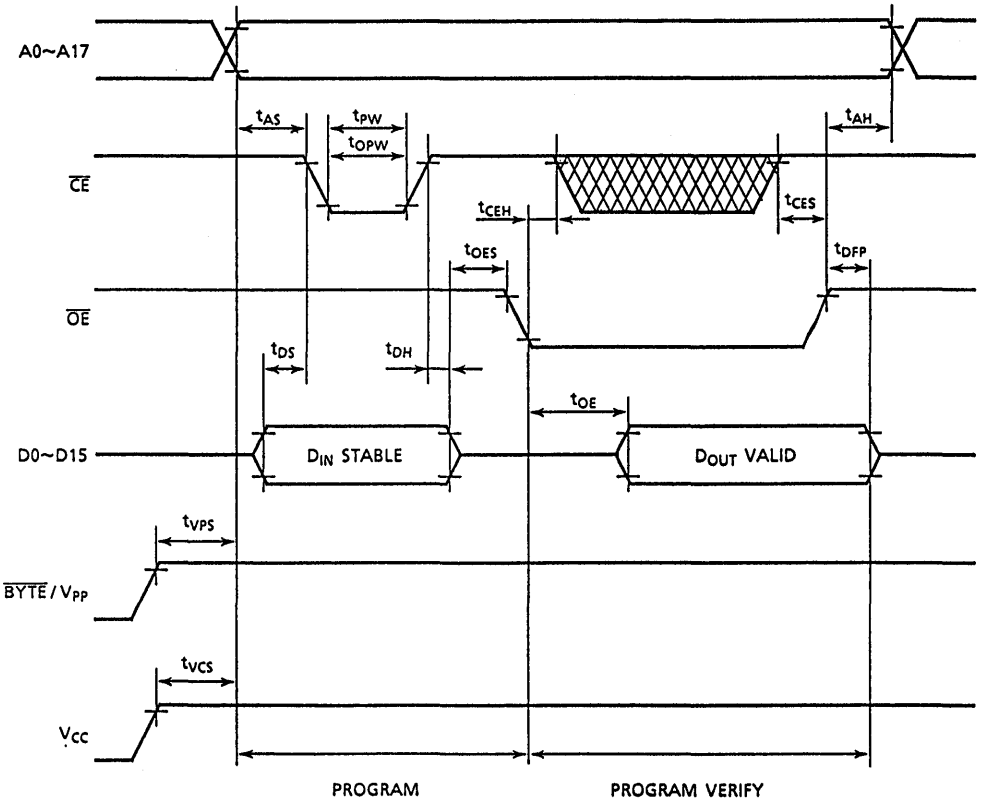
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	μs
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VPS}	V_{PP} Setup Time	–	2	–	–	μs
t_{VCS}	V_{CC} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	–	45	50	55	μs
t_{OPW}	Overprogram Pulse Width	Note 1	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	–	–	100	ns
t_{DFP}	$\overline{OE}$ to Output in High Impedance	$\overline{CE} = V_{IH}$	–	–	90	ns

- A.C. TEST CONDITIONS
  - Output Load : 1 TTL Gate and CL = 100PF
  - Input Pulse Rise and Fall Time : 10ns Max
  - Input Pulse Levels : 0.45V and 2.4V
  - Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1 : t_{OPW} depends on the program pulse width which is required in the initial program.

TIMING WAVEFORMS

HIGH SPEED PROGRAM OPERATION



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.50V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC574200D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (ultraviolet light intensity [W / cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [W · sec / cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW / cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW / cm^2] × (20×60) [sec] ≒ 15 [W · sec / cm^2].)

The TC574200D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC902 - are available.

OPERATION INFORMATION

The TC574200D's eight operation mode are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$ / V_{PP}	V_{CC}	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance			Standby
			L		High Impedance		*	
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

READ MODE

The TC574200D has the $\overline{BYTE}$/V_{PP} terminal that selects word-wide output and byte-wide output. When $\overline{BYTE}$/V_{PP} is set to V_{IH}, the word-wide output is selected, and D15/A-1 pin is used for D15 data output.

When $\overline{BYTE}$/V_{PP} is set to V_{IL}, the byte-wide output is selected, and D15/A-1 pin is used for A-1 address input. When A-1 is set to V_{IL} in this condition, the data output is selected lower 8 bits of the 16 bit data which has been programmed. When A-1 is set to V_{IH}, the data output is selected upper 8 bits.

The TC574200D has two control function. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC574200D's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574200D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC574200D is placed in the standby mode which reduces the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

PROGRAM MODE

Initially, when recieved by customers, all bits of the TC574200D are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit location by electrically programming. The TC574200D is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$. Data to be programmed must be applied 16 bits in parallel to the data pins.

The TC574200D can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL}. The programmed data should be compared with the original word-wide (16 bit) data.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC574200D from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

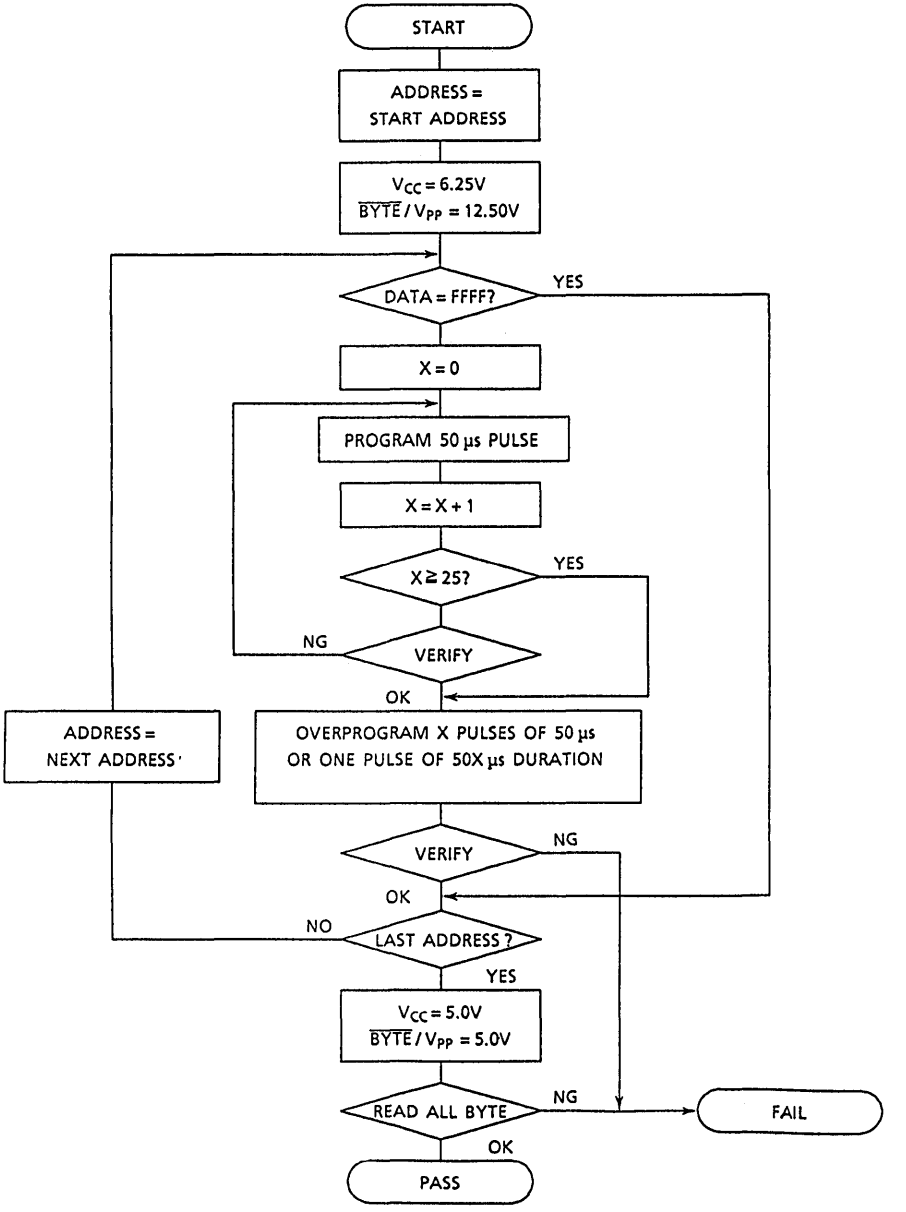
HIGH SPEED PROGRAM MODE

The device is set up the high speed programming mode when the programming voltage (12.50V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$. The programming is achieved by applying a single TTL low level 50μs pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 50μs is applied and then the programmed data is verified. This should be repeated until the program operates correctly(max. 25 times).

After correctly programming the selected address, the overprogram pulse of same length that needed for initial programming should be applied. When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574200D which identifies its manufacturer and device type. The programming equipment may read out manufacturer code and device code from TC574200D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC574200D.

PINS / SIGNATURE	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	1	0	0	0	1	1	1	1	**8F

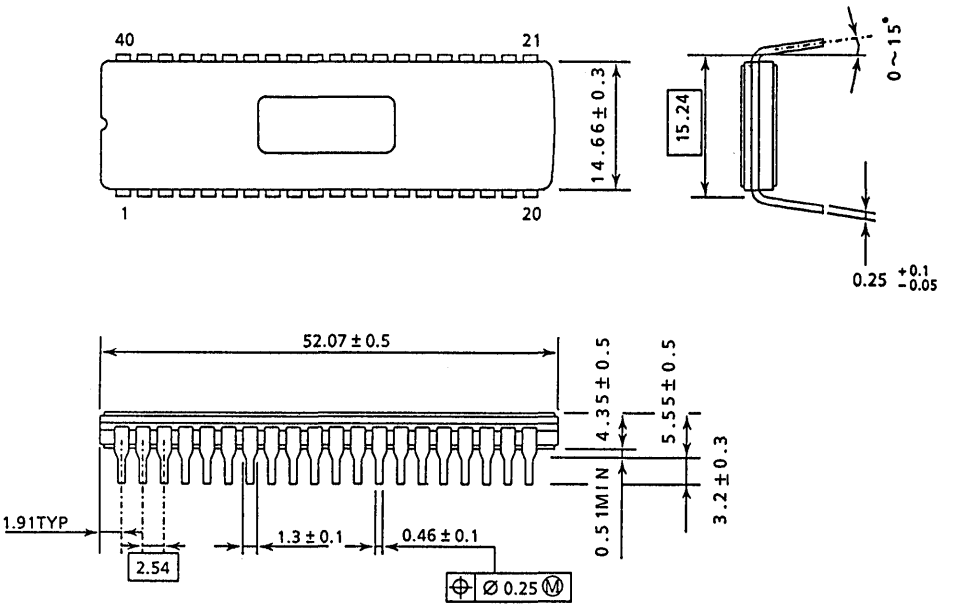
Note: A1 – A8, A10 – A17, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{BYTE}$ / VPP = V_{IH}
* Don't care

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V
V_{ID}	A9 Auto Select Voltage	11.50	12.00	12.50	V

OUTLINE DRAWINGS

Unit in mm



HIGH-SPEED EPROM

32,768 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC57H256D is a 32,768 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57H256D's access time is 70ns, and the TC57H256D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 50mA/14.2MHz and standby current to 100μA. For program operation, the programming is achieved by using the high speed programming mode. For program operation, the programming is achieved by using high speed programming mode. TC57H256D is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

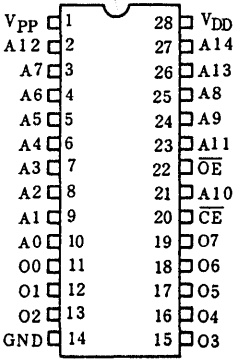
FEATURES

- Peripheral circuit: CMOS
- Memory cell : N-MOS

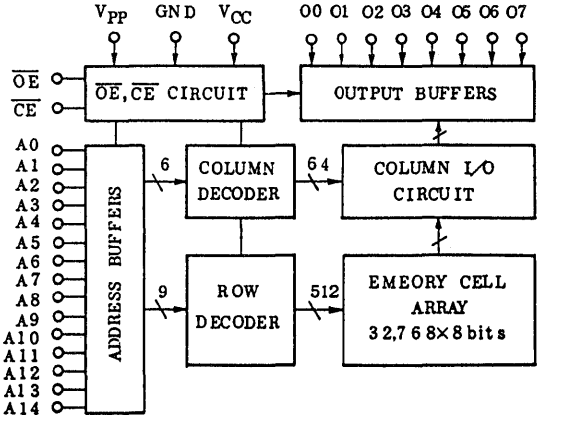
	-70	-85
V_{CC}	5V±5%	5V±10%
t_{ACC}	70ns	85ns

- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256AD
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A14	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11∿13, 15∿19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V 1)	6V 1)	Data In	Active
Program Inhibit	H	H	12.75V 2)	6.25V 2)	High Impedance	
Program Verify	*	L			Data Out	

* H or L 1): HIGH SPEED PROGRAM MODE I
2): HIGH SPEED PROGRAM MODE II

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
t_{STG}	Storage Temperature	-65 ∿ 125	°C
t_{OPR}	Operating Temperature	0 ∿ 70	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H256D-70	TC57H256D-85
Ta	Operating Temperature	0 ∿ 70°C	0 ∿ 70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	Vpp Power Supply Voltage	V_{CC}-0.6V ∿ V_{CC}+0.6V	V_{CC}-0.6V ∿ V_{CC}+0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4 ∿ V_{CC}		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$=0V	f=14.2MHz	-	-	50	mA
I_{CC02}		I_{OUT}=0mA	f=1MHz	-	-	20	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{IH}	Input High Voltage	-		2.2	-	V_{CC}+0.3	V
V_{IL}	Output Low Voltage	-		-0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=0400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	Vpp Current	V_{PP}=V_{CC}-0.6 ∿ V_{CC}+0.6		-	-	±10	μA

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TC57H256D-70		TC57H256D-85		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	70	-	85	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	70	-	85	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	40	-	45	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	30	0	30	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	30	0	30	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	5	-	5	-	ns

A.C. TEST CONDITIONS

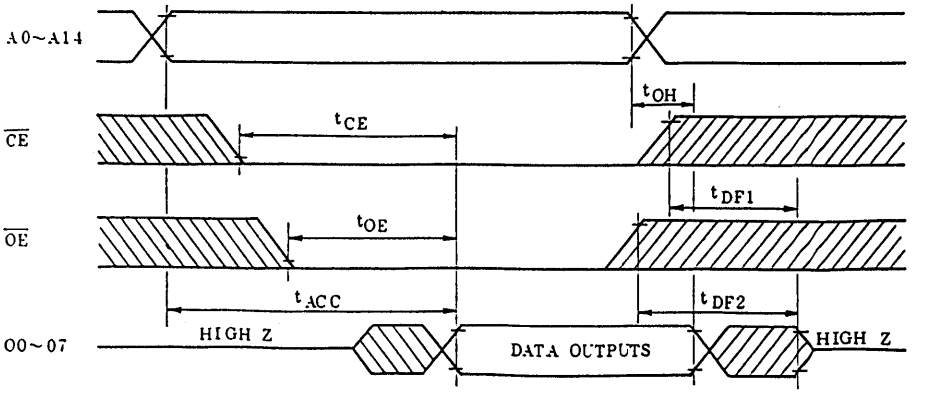
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM MODE I

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	μs
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Date Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : $0.45V \sim 2.4V$
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

HIGH SPEED PROGRAM OPERATION II

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0∿V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, Vpp=12.75±0.25V)

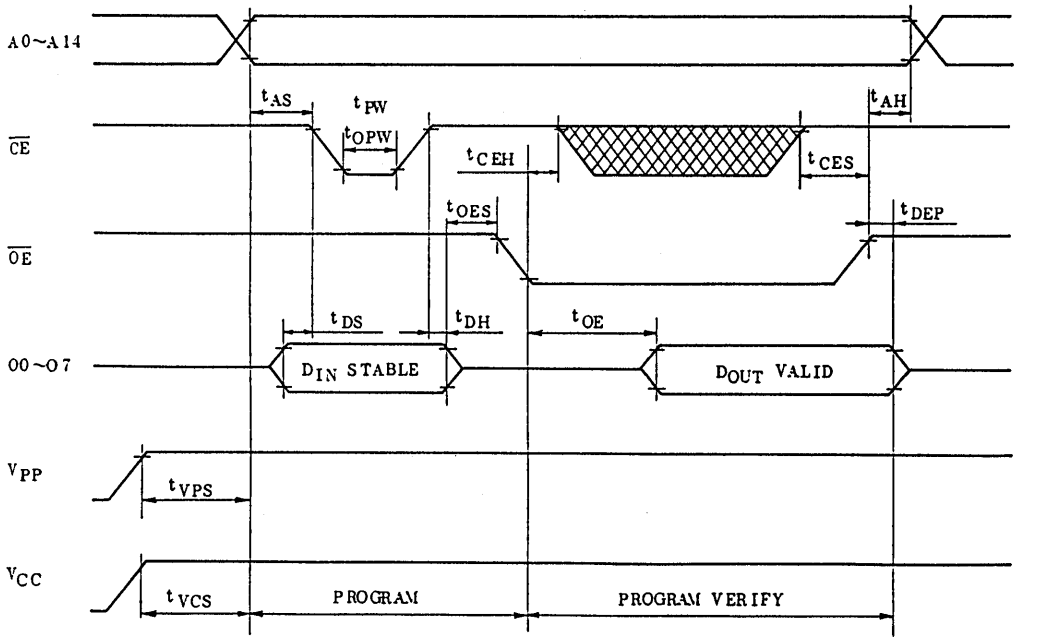
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	Vpp Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM MODE I (V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)
HIGH SPEED PROGRAM MODE II (V_{CC}=6.25V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V(12.75V) may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57H256D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.
The integrated dose (ultraviolet light intensity [w/cm²] 4×1 exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm^2].
When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm^2] × (20 × 60) [sec] ≅ 15 [w·sec/cm^2].)
The TC57H256D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000 ∿ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57H256D's six operation modes are listed in the following table.
Mode selection can be achived by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=0 ∿ 70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	1) 12.5V 2) 12.75V	1) 6V 2) 6.25V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}; L; V_{IL}; *; V_{IH} or V_{IL},

1): HIGH SPEED PROGRAM MODE I,
2): HIGH SPEED PROGRAM MODE II

READ MODE

The TC57H256D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two or more TC57H256D's can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H256D has a low power standby mode controlled by the $\overline{CE}$ signal.
By applying a high level to the $\overline{CE}$ input, the TC57H256D is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H256D are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TC57H256D is in the programming mode when the Vpp input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$.
The TC57H256D can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL}.

PROGRAM INHIBIT MODE

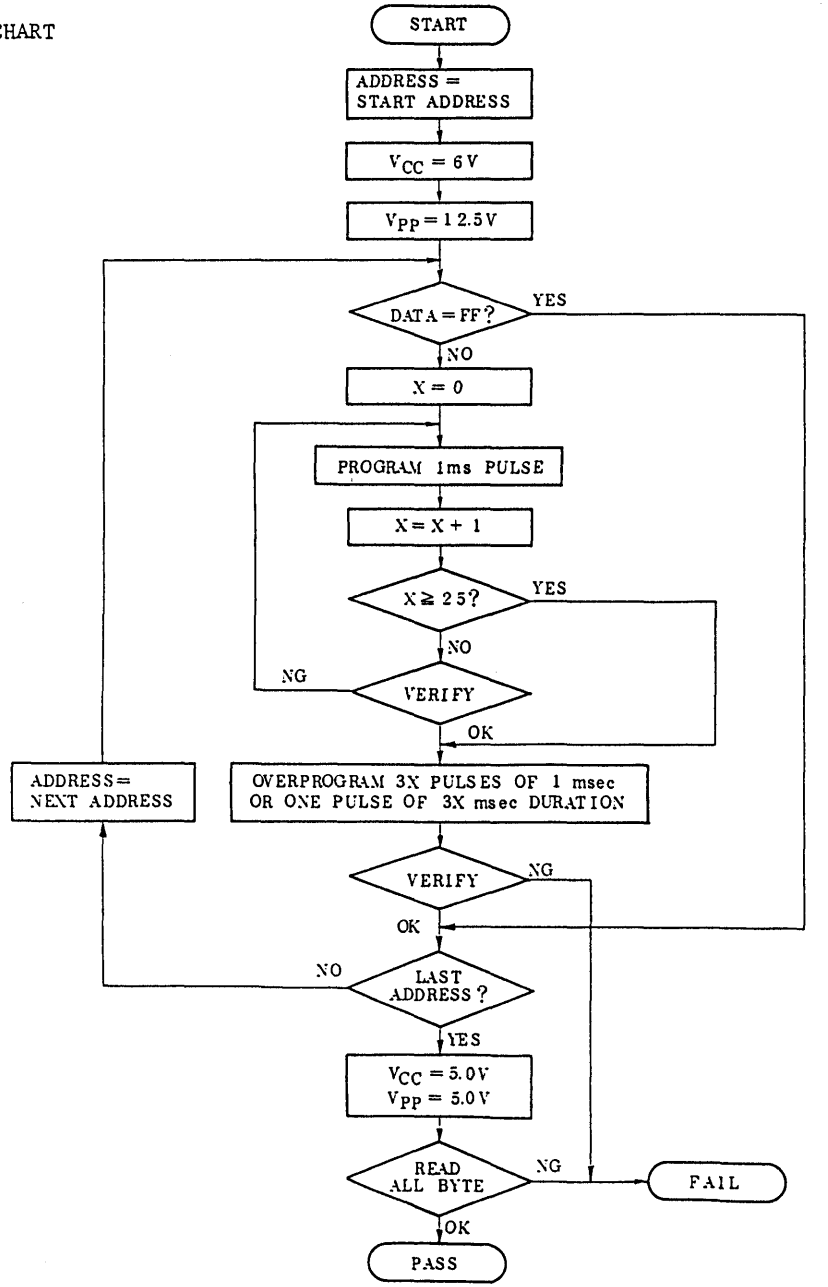
Under the condition that the program voltage (+12.5V or 12.75V) is applied to Vpp terminal, a high level $\overline{CE}$ input inhibits the TC57H256D from being programmed.
Programming of two or more TC57H256D's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

The program time can be greatly decreased by using this high speed programming mode.
The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the Vpp terminal with $V_{CC}=6V$.
The programming is achieved by applying a single TTL low level 1ms pulse to the CE input after addresses and data are stable. Then the programmed data is verified by using Progam Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with $V_{CC}=Vpp=5V$.

HIGH SPEED PROGRAM MODE I

FLOW CHART

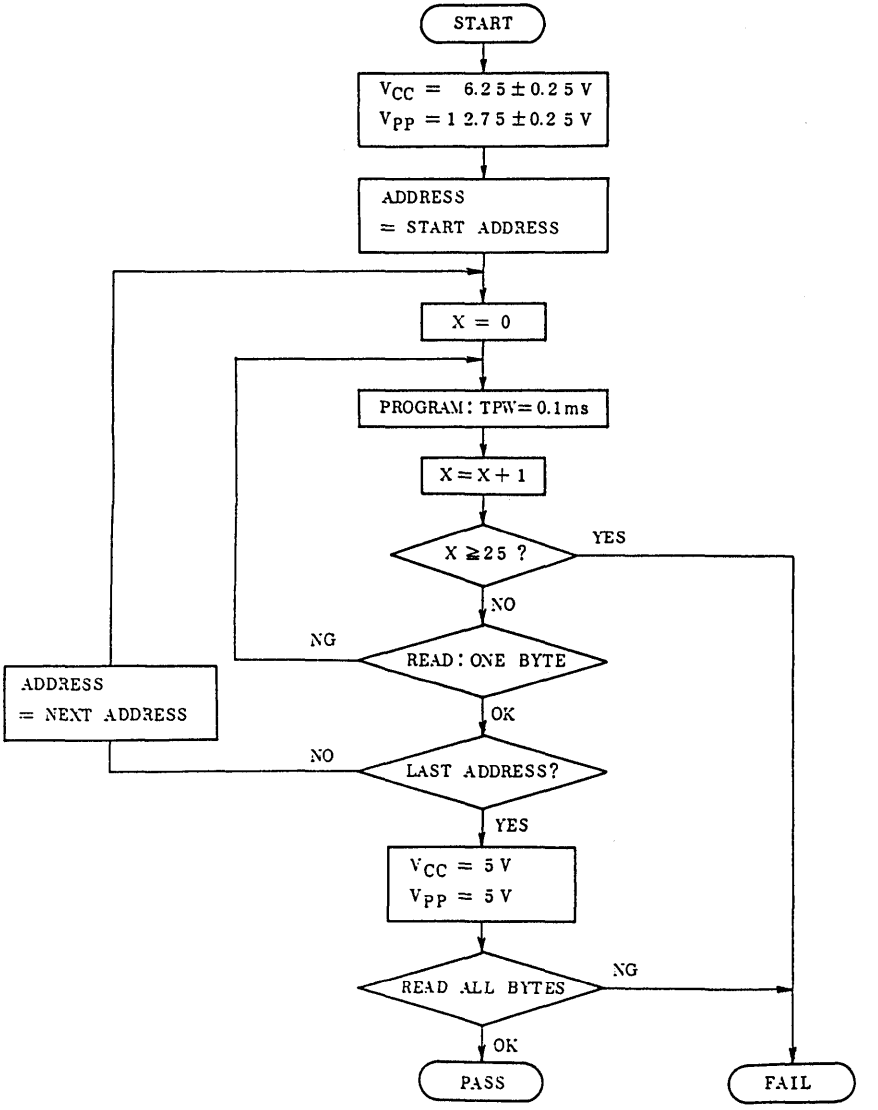


HIGH SPEED PROGRAM MODE II

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC}=6.25V.
The programming is achieved by applying a single TTL low level 0.1ms pulse the CE input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM MODE II

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H256D which identifies its manufacturer and device type.

The programming equipment may read out manufacturer coce and device code from TC57H256D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TC57H256D.

PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	0	0	1	0	1	45

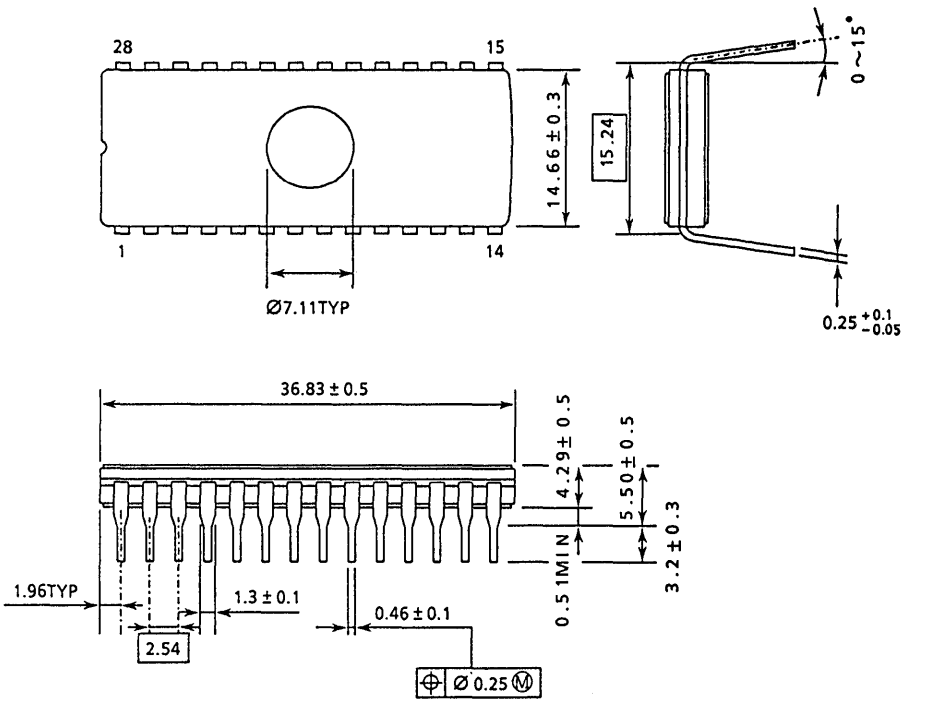
Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS

WDIP28-G-600A

Unit : mm



131,072 WORD × 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC57H1000AD / TC57H1001AD is a 131,072 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC57H1000AD is JEDEC standard pin configuration and the TC57H1001AD is compatible with 28 pin 1M bit Mask ROM. Both products are packed in 32 pin standard cerdip package.

The TC57H1000AD / TC57H1001AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 40mA / 11.8MHz and access time of 85ns / 100ns.

The programming times of the TC57H1000AD / TC57H1001AD except overhead times of EPROM programmer is only 14 seconds by using the high speed programming algoritim.

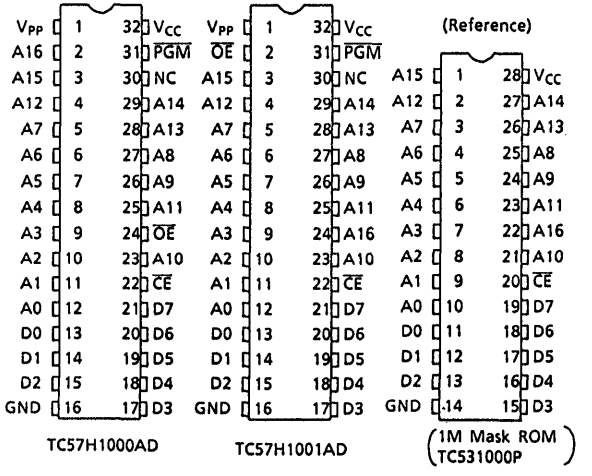
FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Access time

	-85	-100
t_{ACC}	85ns	100ns
V_{CC}	5V ± 10%	

- Low power dissipation
  Active : 40mA / 11.8MHz
  Standby: 100μA (Ta = 70°C)
- Wide operating temperature range : 0~70°C
- Single 5V power supply
- Full static operation
- High speed programming operation : t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin : TC57H1000AD
- 1M MROM compatible : TC57H1001AD
- Standard 32 pin DIP cerdip package

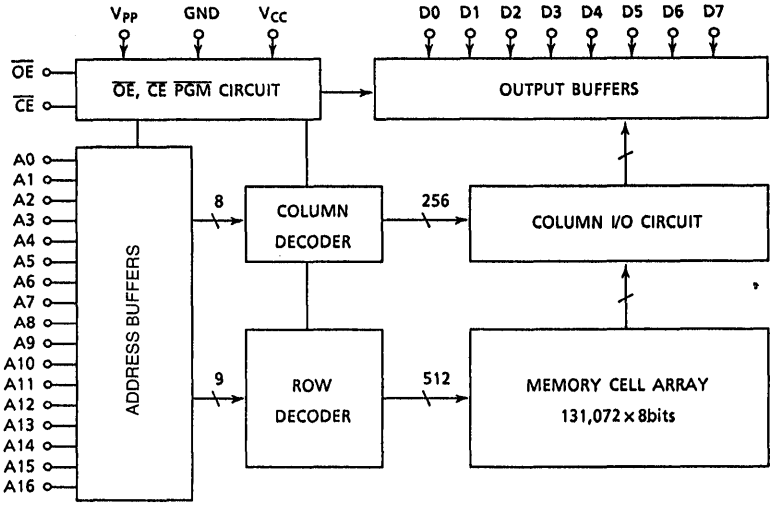
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A16	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	PGM	CE	OE	VPP	VCC	D0~D7	Power
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260·10	°C·sec
T_{STRG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H1000AD/1001AD-85/-100		UNIT
		MIN.	MAX.	
V_{IH}	Input High Voltage	2.2	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	-0.3	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.50	V
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC}-0.6$	$V_{CC}+0.6$	V

DC AND OPERATING CHARACTERISTICS (Ta=0~70°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$		—	—	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}=0V$	f=11.8MHz	—	—	40	mA
I_{CCO2}		$I_{OUT}=0mA$	f=1MHz	—	—	15	
I_{CCS1}	Standby Current	$\overline{CE}=V_{IH}$		—	—	1	mA
I_{CCS2}		$\overline{CE}=V_{CC}-0.2V$		—	—	100	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$		2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$		—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=V_{CC}\pm0.6V$		—	—	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4V\sim V_{CC}$		—	—	10	μA

AC CHARACTERISTICS (Ta=0~70°C, $V_{PP}=V_{CC}\pm0.6V$)

SIMBOL	PARAMETER	TC57H1000AD/1001AD-85		TC57H1000AD/1001AD-100		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	85	—	100	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	85	—	100	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	45	—	50	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	45	—	50	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	30	0	40	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	30	0	40	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	30	0	40	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

AC TEST CONDITIONS

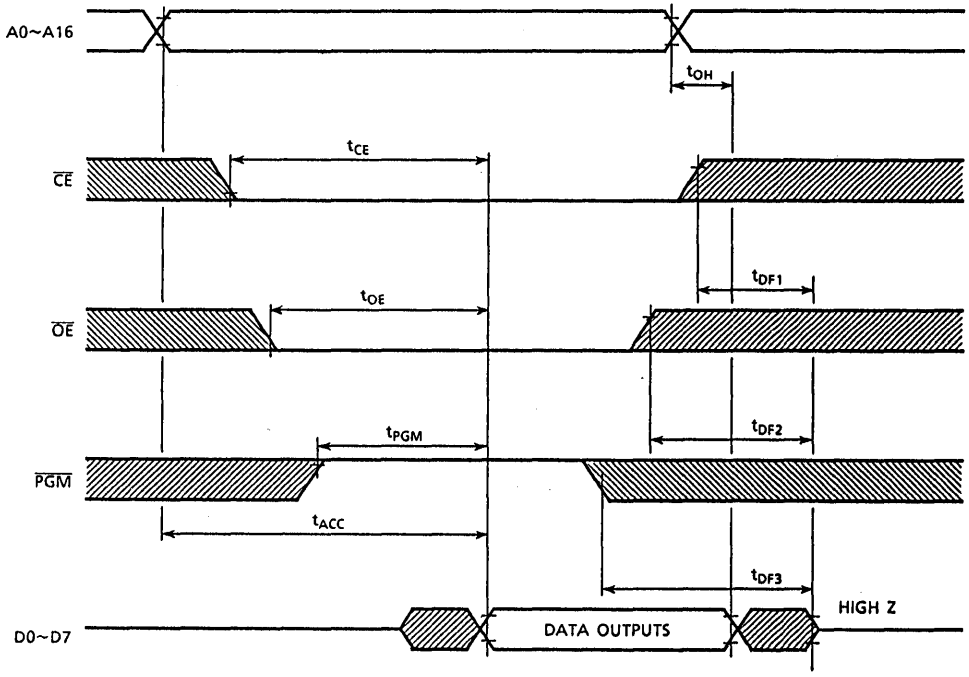
- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	4	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	10	12	

*This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS (Ta = 25 ± 5°C, V_{CC} = 6.25V ± 0.25V, Vpp = 12.75V ± 0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0~V_{CC}	–	–	± 10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 13.0V	–	–	50	mA

AC PROGRAMMING CHARACTERISTICS (Ta = 25 ± 5°C, V_{CC} = 6.25V ± 0.25V, Vpp = 12.75V ± 0.25V)

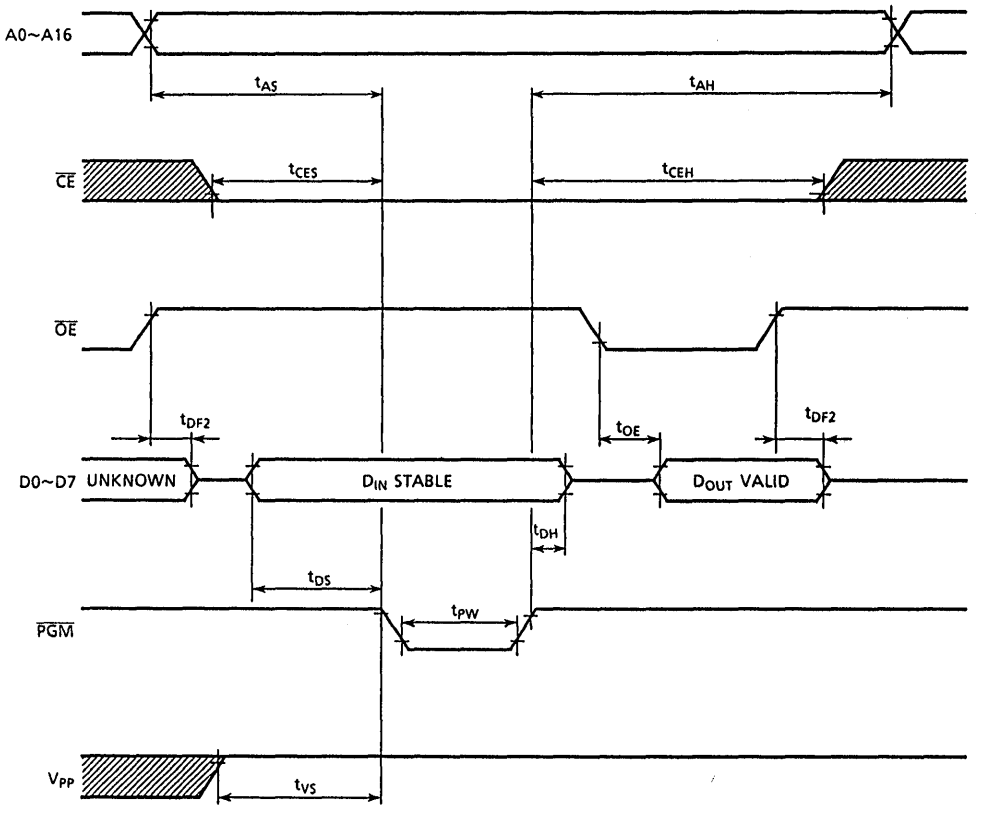
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Set up Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Set up Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	–	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}	–	–	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with VPP=12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation.
So the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57H1000AD / TC57H1001AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity [w/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [w · sec/cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of lcm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000[μw/cm^2] × (20 × 60) [sec.] ≃ 15 [w · sec/cm^2].)

The TC57H1000AD / TC57H1001AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57H1000AD / TC57H1001AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN		$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	POWER
Read Operation (Ta = 0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselet	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
Program Operation (Ta = 25 ± 5°C)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC57H1000AD/TC57H1001AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers independent of device selection.

Assuming in that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses. The CE to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$. And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1000AD/TC57H1001AD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC57H1000AD/TC57H1001AD is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1000AD/TC57H1001AD is in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The levels required for all inputs are TTL.

The TC57H1000AD/TC57H1001AD can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC57H1000AD/TC57H1001AD from being programmed.

Programming of two or more EPROM's in inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

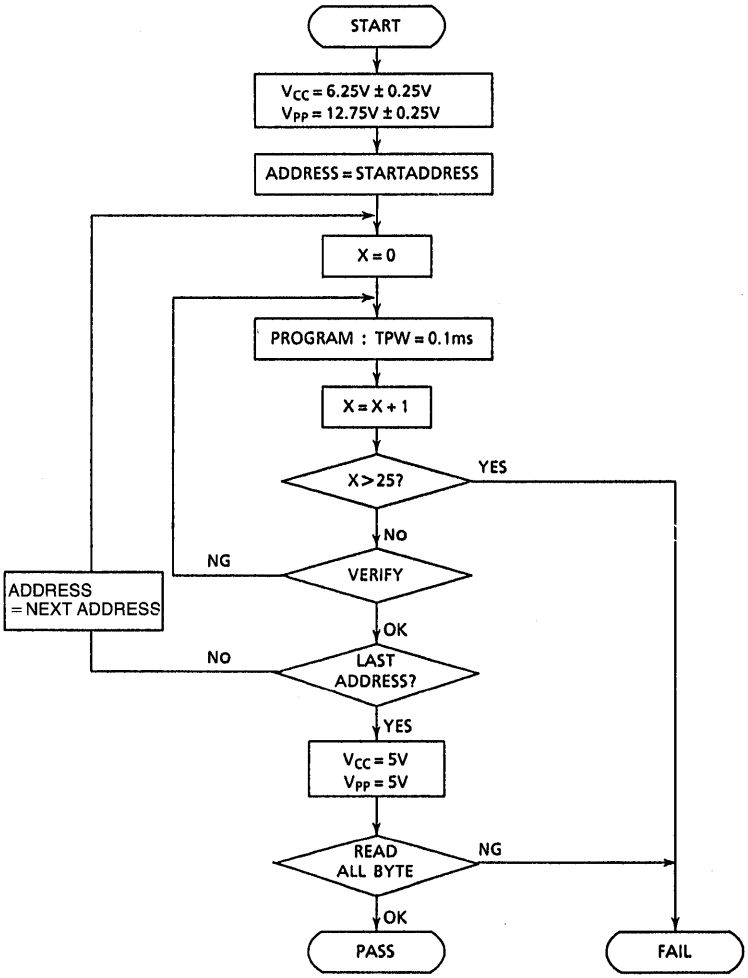
The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1000AD / TC57H1001AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57H1000AD / TC57H1001AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC57H1000AD / TC57H1001AD.

PINS / SIGNATURE		A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX Data
Manufacture Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC57H1000AD	V_{IH}	1	0	0	0	0	1	1	0	86
	TC57H1001AD		0	0	0	0	0	1	1	1	07

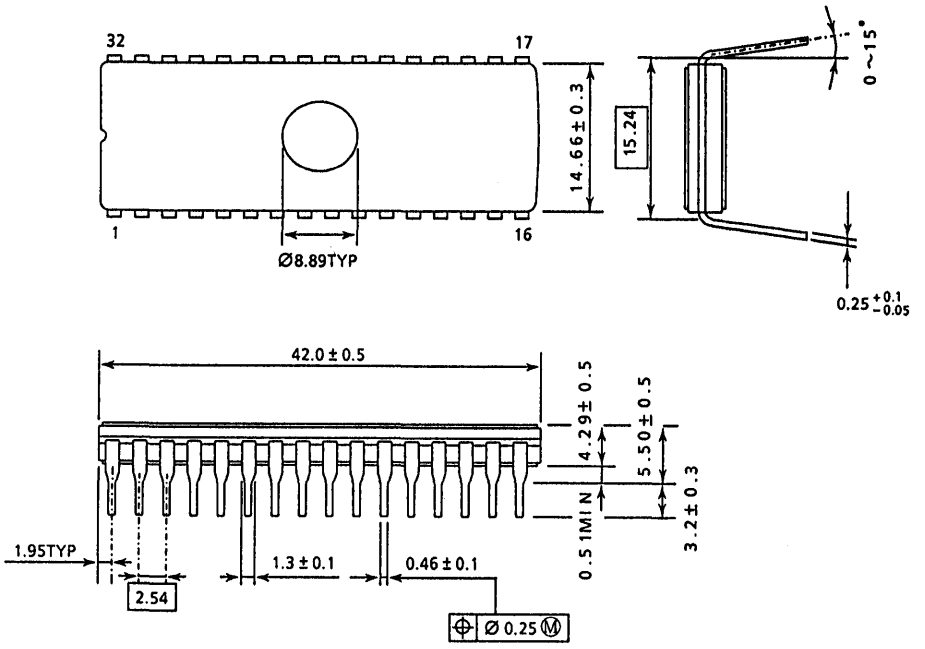
Notes: A9 = 12V ± 0.5V
A1~A8, A0~A16, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

- Cerdip DIP

WDIP32-G-600

Unit : mm



PRELIMINARY

1 MEGA BIT (65,536 WORD × 16 BIT)
CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57H1024D is a 65,536 word × 16 bit CMOS ultraviolet light erasable and electrically programmable read only memory. The TC57H1024D is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

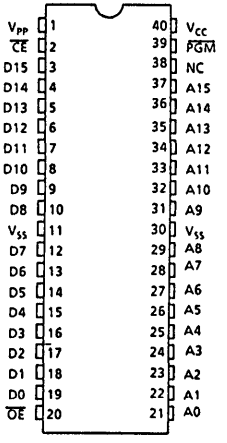
TC57H1024D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 40mA/1MHz and access time of 85ns/100ns.

The programming times of the TC57H1024D except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Fast access time
  TC57H1024D-85 : 85ns
  TC57H1024D-10/100 : 100ns
- Low power dissipation
  Active : 40mA/1MHz
  Standby : 100μA
- Single 5V power supply
- Full static operation
- High speed programming operation : t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 40 pin : TC57H1024D
- Standard 40 pin DIP cerdip package

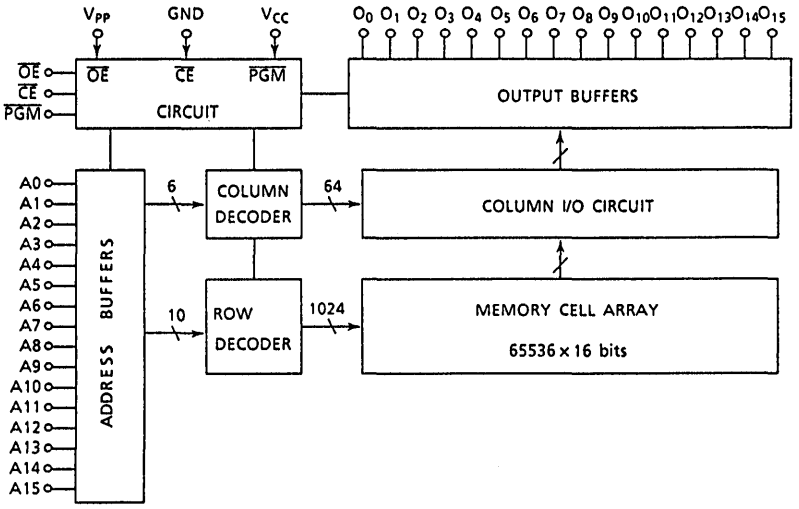
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
Read	L	L	H	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*	*				Standby
Program	L	H	L	12.75V	6.25V	Data In	Active
Program Inhibit	H	*	*			High Impedance	
	L	H	H				
Program Verify	L	L	H			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
V_{IN} (A9)	Input Voltage (A9)	-0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	-0.6~V_{CC} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	-65~125	°C
T_{opr}	Operating Temperature	0~70	°C

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H1024D-85/10	TC57H1024D-100
Ta	Ambient Temperature	0~70°C	
V_{CC}	V_{CC} Power Supply Voltage	5V ± 5%	5V ± 10%
V_{PP}	V_{PP} Power Supply Voltage	0V~V_{CC} + 0.6V	

DC AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0~V_{CC}	–	–	± 10	μA
I_{CCO}	Operating Current	$\overline{CE}$ = 0V, I_{OUT} = 0mA, t_{cycle} = 1μs	–	–	40	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	–	1	mA
I_{CCS2}		$\overline{CE}$ = V_{CC} – 0.2V	–	–	100	μA
V_{IH}	Input High Voltage	—	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	—	– 0.3	–	0.8	V
V_{OH}	Output High Voltage	I_{OH} = – 400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = V_{CC} ± 0.6V	–	–	± 10	μA
I_{LO}	Ouptut Leakage Current	V_{OUT} = 0.4V~V_{CC}	–	–	± 10	μA

AC CHARACTERISTICS (V_{PP}=0V~V_{CC}+0.6V)

SYMBOL	PARAMETER	TC57H1024D-85		TC57H1024D-10/100		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	–	85	–	100	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	85	–	100	
t_{OE}	$\overline{OE}$ to Output Valid	–	45	–	50	
t_{DF1}	$\overline{CE}$ to Output in High-Z	–	30	–	50	
t_{DF2}	$\overline{OE}$ to Output in High-Z	–	30	–	50	
t_{OH}	Output Data Hold Time	5	–	10	–	

TC57H1024D-85 is satisfied with the specification of TC57H1024D-100.

AC TEST CONDITIONS

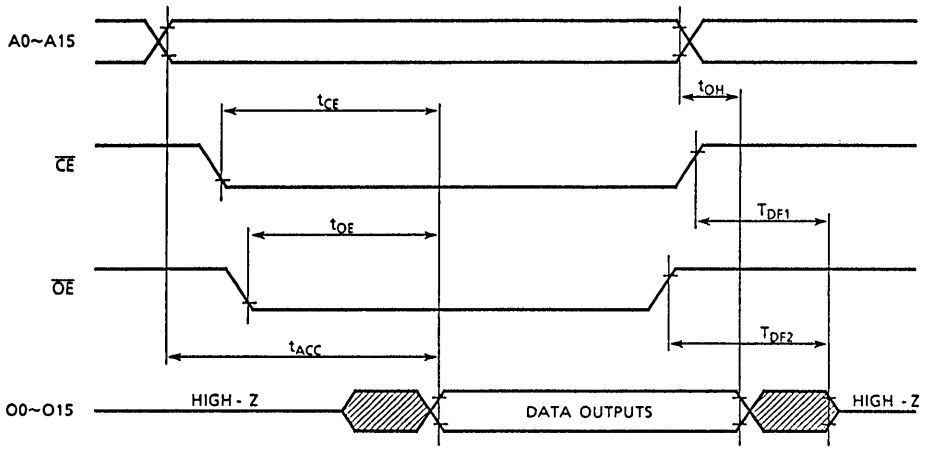
Ouput Load : 1 TTL Gate and C_L=100pF
Input Pulse Rise and Fall Times : 10ns Max.
Input Pulse Levels : 0.45V to 2.4V
Timing Measurement Reference Levels : Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	10	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS($Ta=25\pm5°C, V_{CC}=6.25V\pm0.25V, V_{PP}=12.75V\pm0.25V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	50	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	–	–	100	mA

AC PROGRAMMING CHARACTERISTICS($Ta=25\pm5°C$, $V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.75V\pm0.25V$)

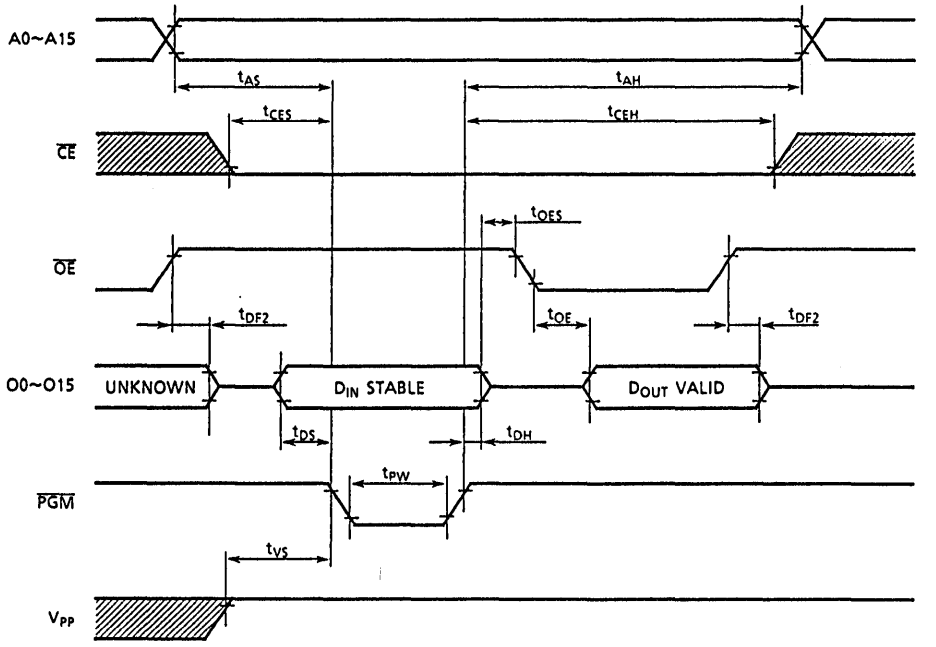
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	–	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	500	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	–	–	150	ns
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Levels: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP} = 12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57H1024D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (Ultraviolet light intensity [W/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm^2] × (20 × 60) [sec]≃15 [W·sec./cm^2].)

The TC57H1024D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC57H1024D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
READ OPERATION	Read	L	L	H	5V	5V	Data Out	Active
	Output Deselect	*	H	*			High Impedance	
	Standby	H	*	*				Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program	L	H	L	12.75V	6.25V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
		L	H	H				
	Program Verify	L	L	H			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC57H1024D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1024D has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC57H1024D is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1024D are in the "1" state which is erased state.

Therefore the program operation is to introduce "Ø" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC57H1024D can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC57H1024D from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

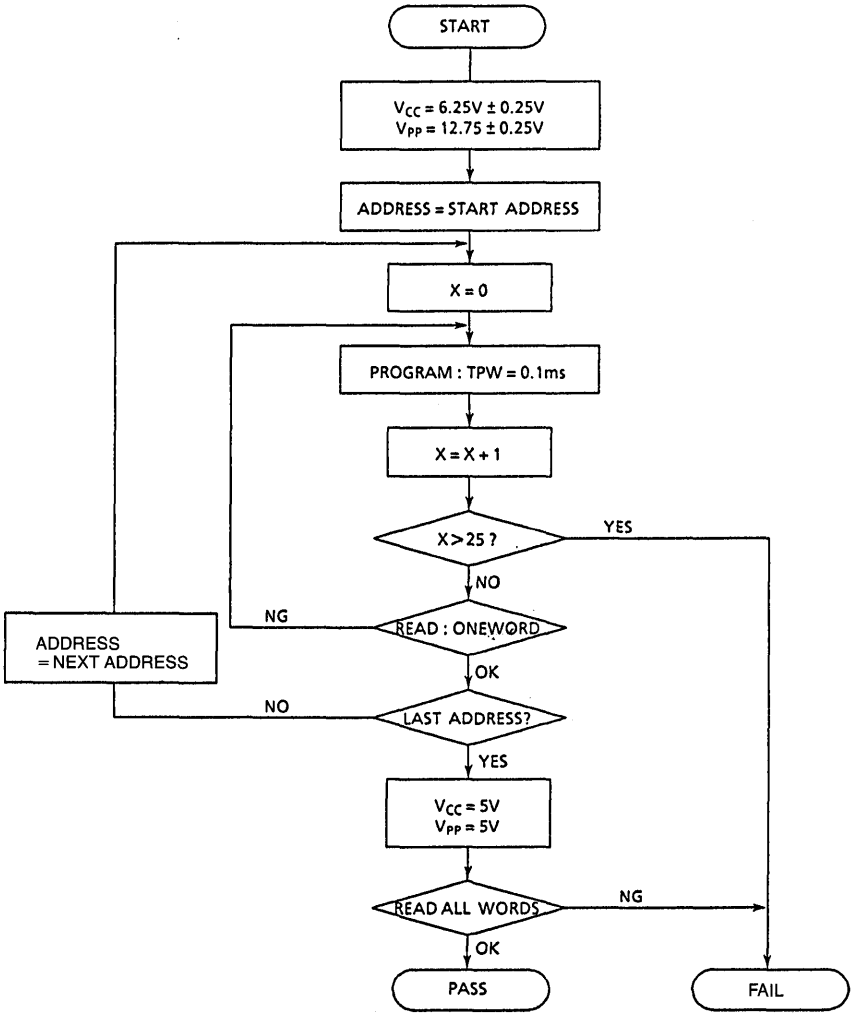
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1024D which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC57H1024D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of (O7).

The following table shows electric signature of TC57H1024D.

PINS / SIGNATURE	A_0	O_{15}	O_{14}	O_{13}	O_{12}	O_{11}	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	HEX DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	1	0	0	0	1	0	0	1	**89

Notes: $A9 = 12V \pm 0.5V$, $A_1 - A_8$, $A_{10} - A_{15}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ *: Don't care

DC AND OPERATING CHARACTERISTICS

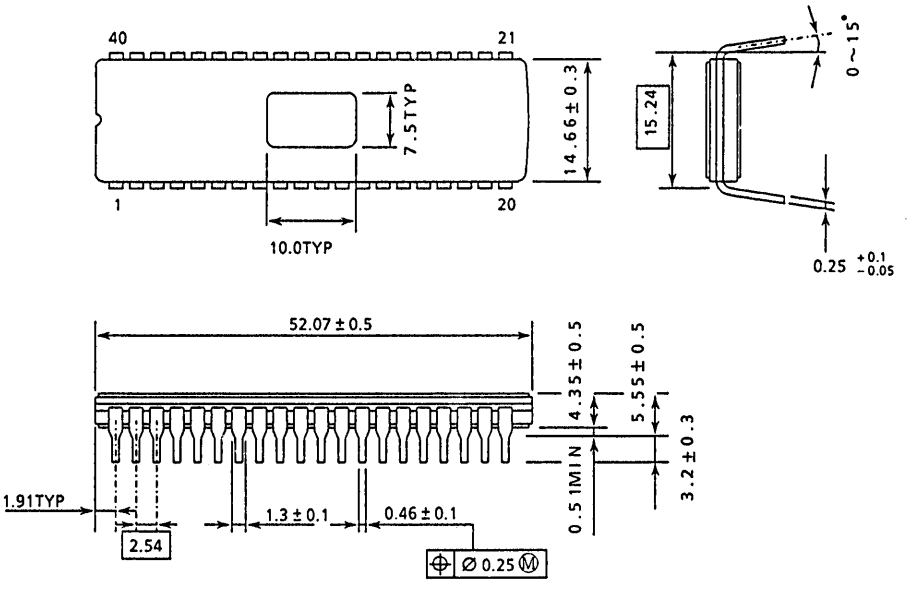
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{ID}	A_9 Auto Select Voltage	11.5	12.0	12.5	V

OUTLINE DRAWINGS

- Cerdip DIP

WDIP40-G-600A

Unit : mm



1 MEGA BIT (65,536 WORD × 16 BIT) HIGH SPEED CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57H1025AD is a 65,536 word × 16 bit high speed CMOS ultraviolet light erasable and electrically programmable read only memory. The TC57H1025AD is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

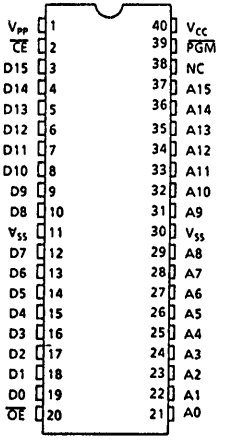
TC57H1025AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 60mA/1MHz and access time of 55ns.

The programming time of the TC57H1025AD except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
  Memory cell : NMOS
- Fast access time
  TC57H1025AD-55 : 55ns
- Low power dissipation
  Active : 60mA/1MHz
  Standby : 10mA
- Single 5V power supply
- Full static operation
- High speed programming operation : t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 40 pin
- Standard 40 pin DIP cerdip package

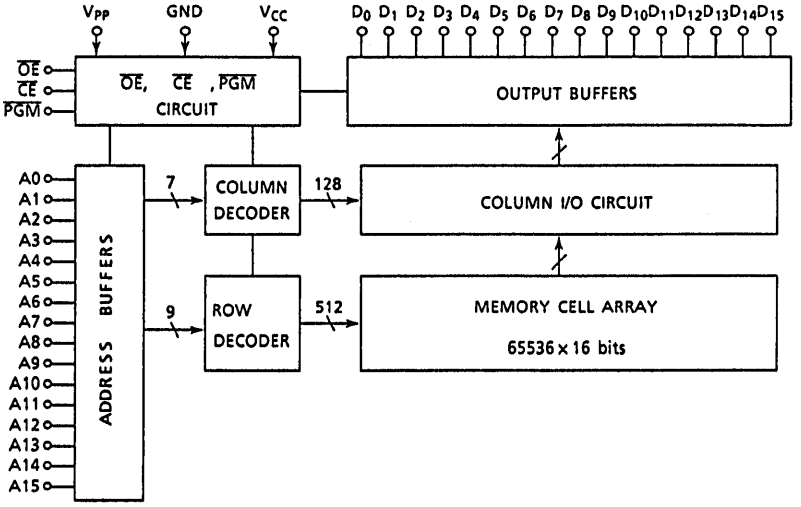
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
Read	L	L	H	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*	*				Standby
Program	L	H	L	12.75V	6.25V	Data In	Active
Program Inhibit	H	*	*			High Impedance	
	L	H	H				
Program Verify	L	L	H			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{IN} (A9)	Input Voltage (A9)	−0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	−0.6~V_{CC} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~125	°C
T_{opr}	Operating Temperature	0~70	°C

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H1025AD-55
Ta	Ambient Temperature	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V ± 5%
V_{PP}	V_{PP} Power Supply Voltage	0V~V_{CC} + 0.6V

DC AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0~V_{CC}	–	–	± 10	μA
I_{CCO}	Operating Current	$\overline{CE}$ = 0V, I_{OUT} = 0mA, t_{cycle} = 1μs	–	–	60	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	–	12	mA
I_{CCS2}		$\overline{CE}$ = V_{CC} – 0.2V	–	–	10	mA
V_{IH}	Input High Voltage	—	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	—	– 0.3	–	0.8	V
V_{OH}	Output High Voltage	I_{OH} = – 4.0mA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA	–	–	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = V_{CC} + 0.6V	–	–	± 10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V~V_{CC}	–	–	± 10	μA

AC CHARACTERISTICS (V_{PP} = 0V~V_{CC} + 0.6V)

SYMBOL	PARAMETER	TC57H1025AD-55		UNIT
		MIN.	MAX.	
t_{ACC}	Address Access Time	–	55	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	55	
t_{OE}	$\overline{OE}$ to Output Valid	–	30	
t_{DF1}	$\overline{CE}$ to Output in High-Z	–	25	
t_{DF2}	$\overline{OE}$ to Output in High-Z	–	25	
t_{OH}	Output Data Hold Time	0	–	

AC TEST CONDITIONS

- Output Load : See Fig.1
- Input Pulse Rise and Fall Times : 5ns Max.
- Input Pulse Levels : 0V to 3V
- Timing Measurement Reference Levels : Inputs 1.5V Outputs 1.5V

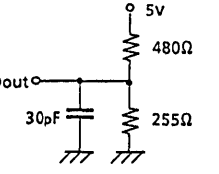


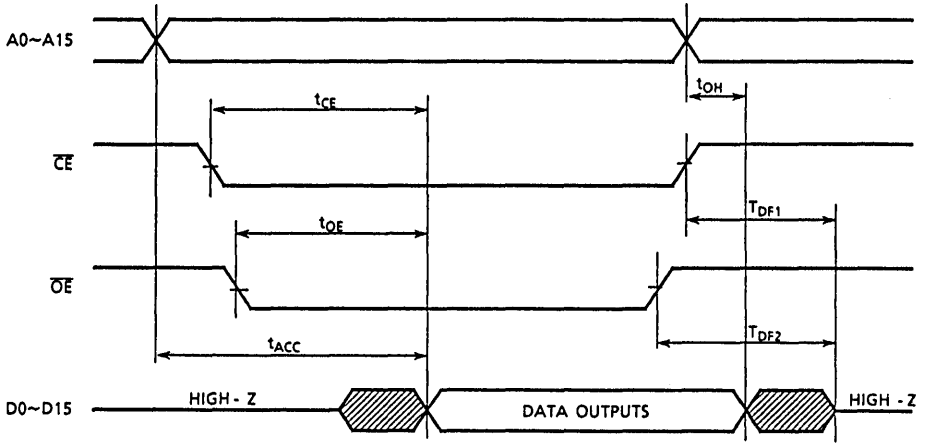
Fig.1 OUTPUT LOAD

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	10	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS($Ta=25\pm5°C$, $V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.75V\pm0.25V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-4.0mA$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL}=8.0mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	50	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	–	–	100	mA

AC PROGRAMMING CHARACTERISTICS($Ta=25\pm5°C$, $V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.75V\pm0.25V$)

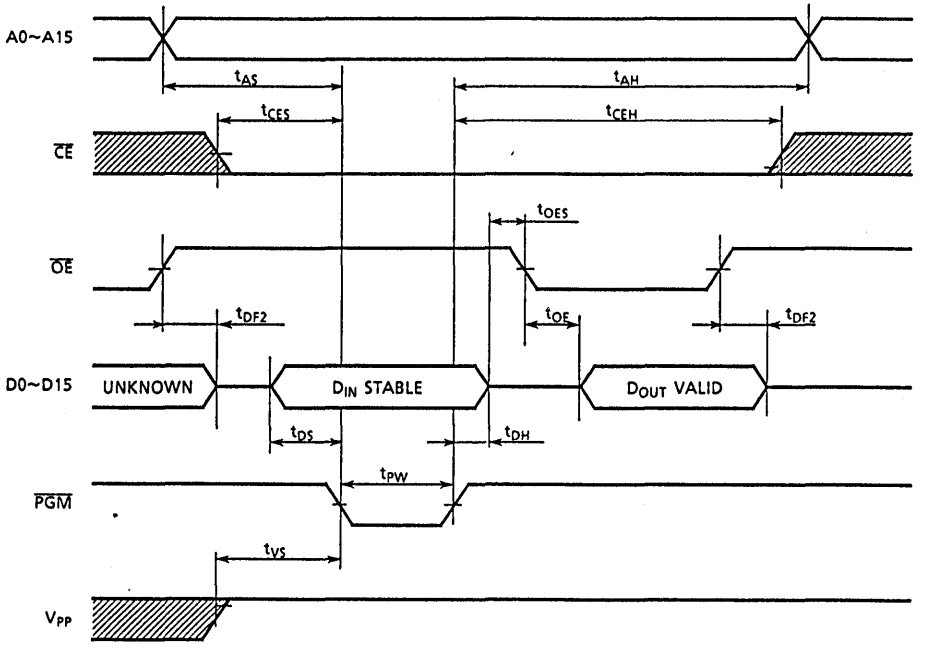
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	–	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	500	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	–	–	150	ns
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs

AC TEST CONDITION

- Output Load : See Fig.1
- Input Pulse Rise and Fall Times : 5ns Max.
- Input Pulse Levels : 0V to 3V
- Timing Measurement Reference Levels : Inputs 1.5V Outputs 1.5V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with VPP=12.75V may cause permanent damage to the device.

3. The VPP supply voltage is permitted up to 14V for program operation. Voltages greater than should not be applied to the VPP terminal.
When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its 14V should not be applied to the VPP terminal.

ERASURE CHARACTERISTICS

The TC57H1025AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (Ultraviolet light intensity [W/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm^2] × (20 × 60) [sec] ≃ 15 [W·sec./cm^2].)

The TC57H1025AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Sunlight and fluorescent lamps include 3000~4000Å wavelength components. Therefore components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC57H1025AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
READ OPERATION (Ta = 0~70°C)	Read	L	L	H	5V	5V	Data Out	Active
	Output Deselect	*	H	*			High Impedance	
	Standby	H	*	*				Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program	L	H	L	12.75V	6.25V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
		L	H	H				
	Program Verify	L	L	H			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC57H1025AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1025AD has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC57H1025AD is placed in the standby mode which reduces the operating current to 10mA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1025AD are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC57H1025AD can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC57H1025AD from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

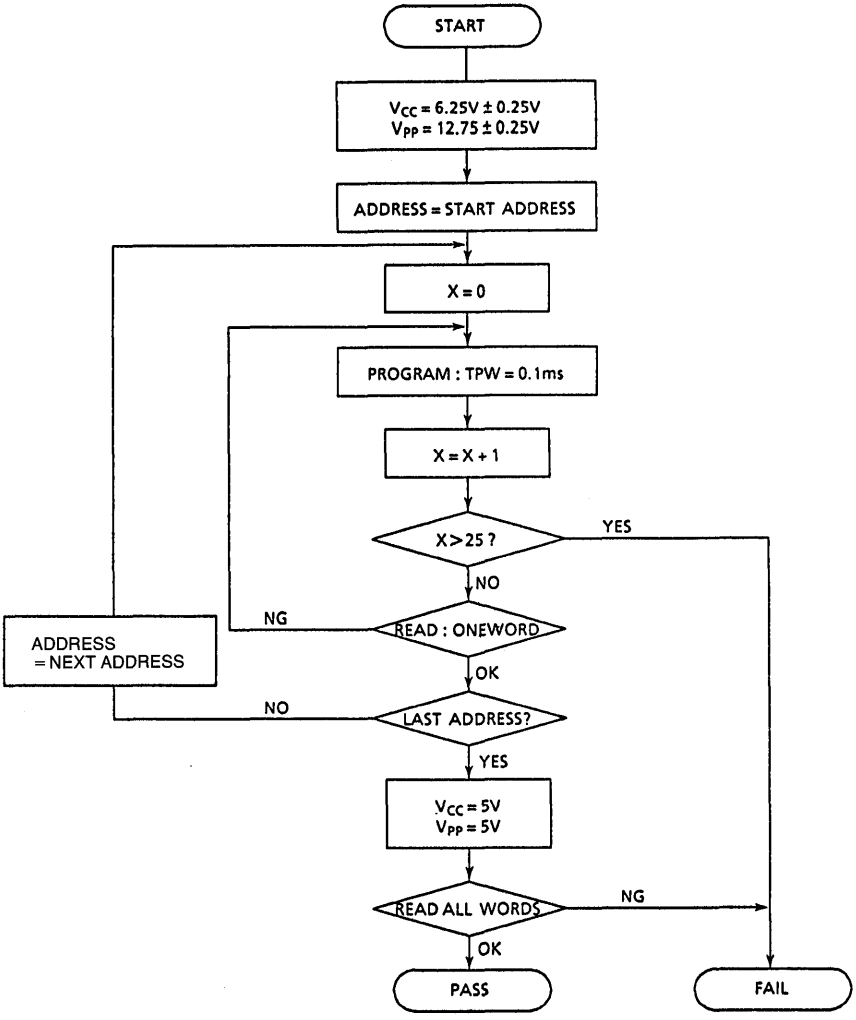
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1025AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC57H1025AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC57H1025AD.

PINS / SIGNATURE	A_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	1	0	0	0	1	0	0	1	**89

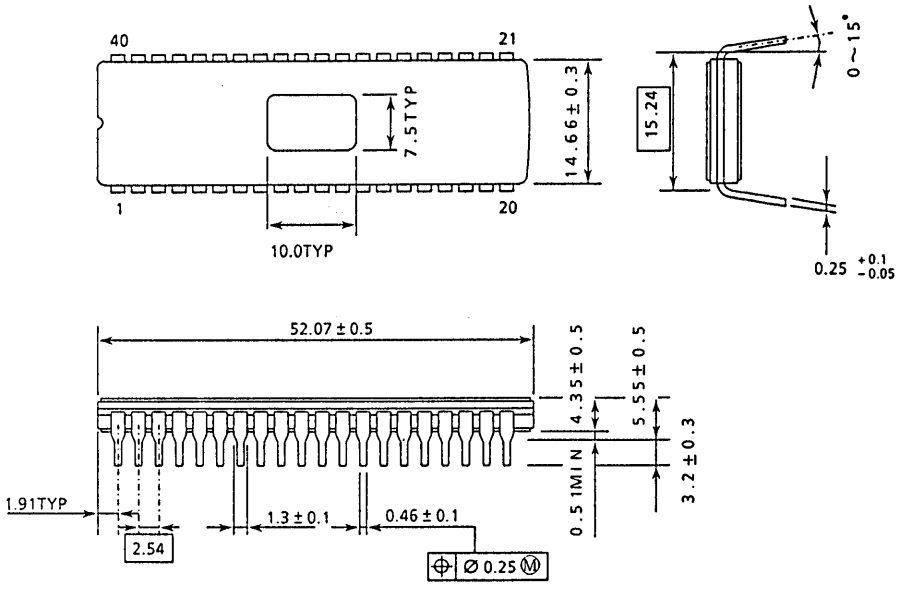
Note: $A9 = 12V \pm 0.5V$, $A_1 - A_8$, $A_{10} - A_{15}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ *: Don't care

OUTLINE DRAWINGS

- Cerdip DIP

  WDIP40-G-600A

Unit : mm



1 MEGA BIT (65,536 WORD × 16 BIT) HIGH SPEED CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57H1026D is a 65,536 word × 16 bit high speed CMOS ultraviolet light erasable and electrically programmable read only memory. The TC57H1026D is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

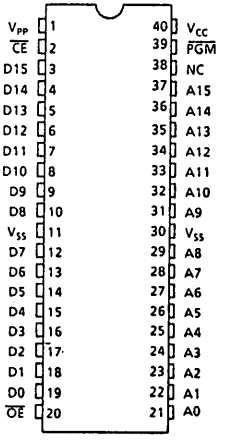
TC57H1026D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 70mA/1MHz and access time of 35ns.

The programming times of the TC57H1026D except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
  Memory cell : NMOS
- Fast access time
  TC57H1026D-35 : 35ns
- Low power dissipation
  Active : 70mA/1MHz
  Standby : 10mA
- Single 5V power supply
- Full static operation
- High speed programming operation : t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 40 pin
- Standard 40 pin DIP cerdip package

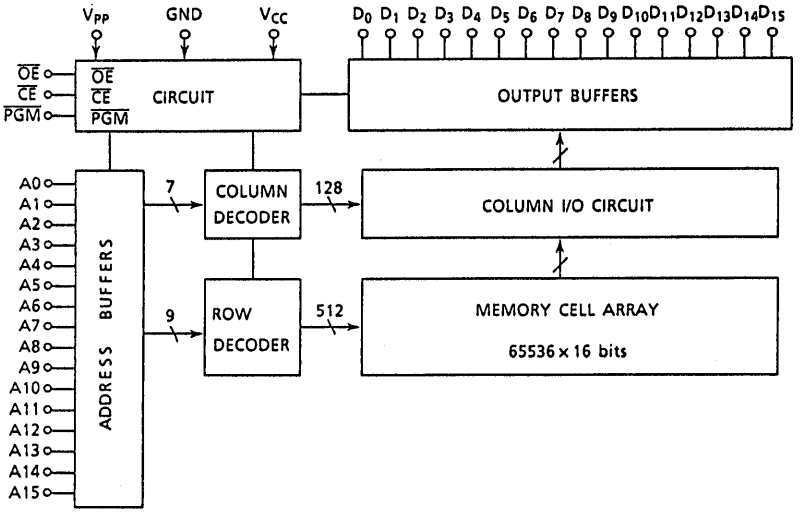
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
Read	L	L	H	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*	*				Standby
Program	L	H	L	12.75V	6.25V	Data In	Active
Program Inhibit	H	*	*			High Impedance	
	L	H	H				
Program Verify	L	L	H			Data Out	
Blank Check One	L	L	HH	5V	5V	Data Out One (FFFF)	Active
Blank Check Zero	L	H	HH			Data Out Zero (0000)	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{IN} (A9)	Input Voltage (A9)	−0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	−0.6~V_{CC} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~125	°C
T_{opr}	Operating Temperature	0~70	°C

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H10246D-35, 45
Ta	Ambient Temperature	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V ± 5%
V_{PP}	V_{PP} Power Supply Voltage	V_{CC} – 0.6v~V_{CC} + 0.6V

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0~V_{CC}	–	–	± 10	μA
I_{CCO}	Operating Current	$\overline{CE}$ = 0V, I_{OUT} = 0mA, t_{cycle} = 1μs	–	–	70	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	–	12	mA
I_{CCS2}		$\overline{CE}$ = V_{CC} – 0.2V	–	–	10	mA
V_{IH}	Input High Voltage	——	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	——	– 0.3	–	0.8	V
V_{OH}	Output High Voltage	I_{OH} = – 4.0mA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA	–	–	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = V_{CC} ± 0.6V	–	–	± 10	μA
I_{LO}	Ouptut Leakage Current	V_{OUT} = 0.4V~V_{CC}	–	–	± 10	μA

AC CHARACTERISTICS (V_{PP}=V_{CC}–0.6v~V_{CC}+0.6V)

SYMBOL	PARAMETER	TC57H1026D-35		TC57H1026D-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	–	35	–	45	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	35	–	45	
t_{OE}	$\overline{OE}$ to Output Valid	–	20	–	20	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	20	0	20	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	20	0	20	
t_{OH}	Output Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

- Output Load : See Fig. 1
- Input Pulse Rise and Fall Time : 5ns Max.
- Input Pulse Levels : 0V to 3V
- Timing Measurement Reference Level : Inputs 1.5V Outputs 1.5V

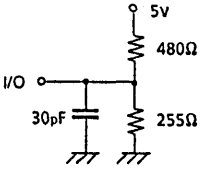


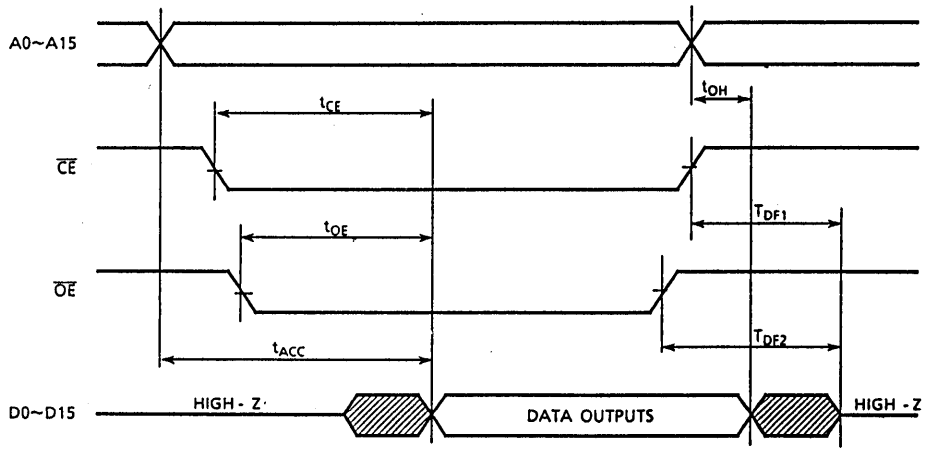
Fig. 1 OUTPUT LOAD

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	3.0	–	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	−0.3	–	0.6	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC PROGRAMMING CHARACTERISTICS($Ta=25\pm5°C, V_{CC}=6.25V\pm0.25V, V_{PP}=12.75V\pm0.25V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-4.0mA$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL}=8.0mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	50	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	–	–	100	mA

AC PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6.25V°0.25V$, $V_{PP}=12.75V\pm0.25V$)

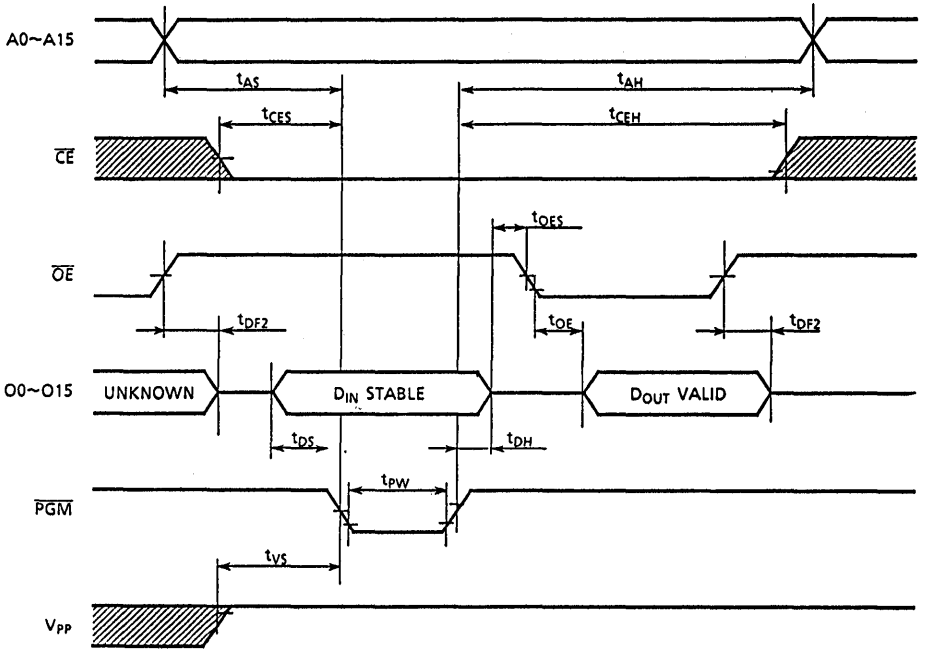
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Hold Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	–	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	500	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	–	–	150	ns
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs

AC TEST CONDITIONS

- Output Load : See Fig. 1
- Input Pulse Rise and Fall Time : 5ns Max.
- Input Pulse Levels : 0V and 3V
- Timing Measurement Reference Level : Input 1.5V, Ouptut 1.5V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with VPP=12.75V may cause permanent damage to the device.
3. The VPP supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the VPP terminal.
When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57H1026D erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (Ultraviolet light intensity [W/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm^2] × (20 × 60) [sec] ≃ 15 [W·sec./cm^2].)

The TC57H1026D erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seal - Toshiba EPROM Protect Seal AC902 - is available.

OPERATION INFORMATION

The TC57H1026D' eight operation modes are listed in the following table.

Mode selection can be achieved by applying TTL-level signal to all inputs.

MODE \ PIN		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
READ OPERATION (Ta = 0~70°C)	Read	L	L	H	5V	5V	Data Out	Active
	Output Deselet	*	H	*			High Impedance	
	Standby	H	*	*				Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program	L	H	L	12.75V	6.25V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
		L	H	H				
	Program Verify	L	L	H			Data Out	
Blank Check OPEREATION	Blank Check One	L	L	HH	5v	5v	Data Out One	Active
	Blank Check Zero	L	H	HH			Data Out Zero	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}
HH ; 12V ± 0.5V

READ MODE

The TC57H1026D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1026D has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC57H1026D is placed in the standby mode which reduce the operating current to 10mA by applying MOS-high level (V_{CC}) and then the ouptuts are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1026D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0'S" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC57H1026D can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC57H1026D from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated unitl the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

BLANK CHECK MODE

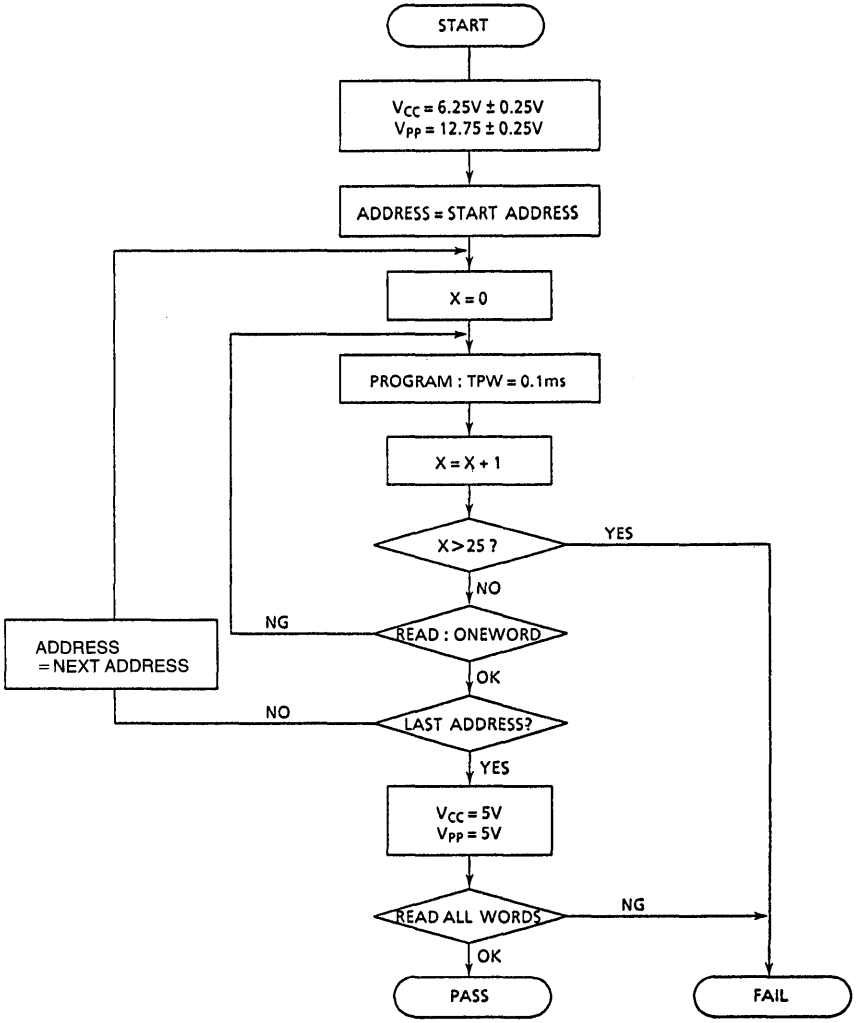
In the erase state a device contains neither a one nor a zero, because of the differential memory cell. The erase state of this device is verified by using the two blank check modes.

BLANK CHECK ZERO mode, which is to check that one side of the differential memory cell is "1" data, is accomplished with $\overline{OE}=\overline{CE}=V_{IL}$ and $\overline{PGM}=12V$.

BLANK CHECK ONE mode, which is to check that the other side of the differential memory cell is "0" data, is accomplished with $\overline{OE}=V_{IH}$, $\overline{CE}=V_{IL}$ and $\overline{PGM}=12V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1026D which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC57H1026D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC57H1026D.

PINS / SIGNATURE	A_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	1	0	0	0	1	0	0	1	**C7

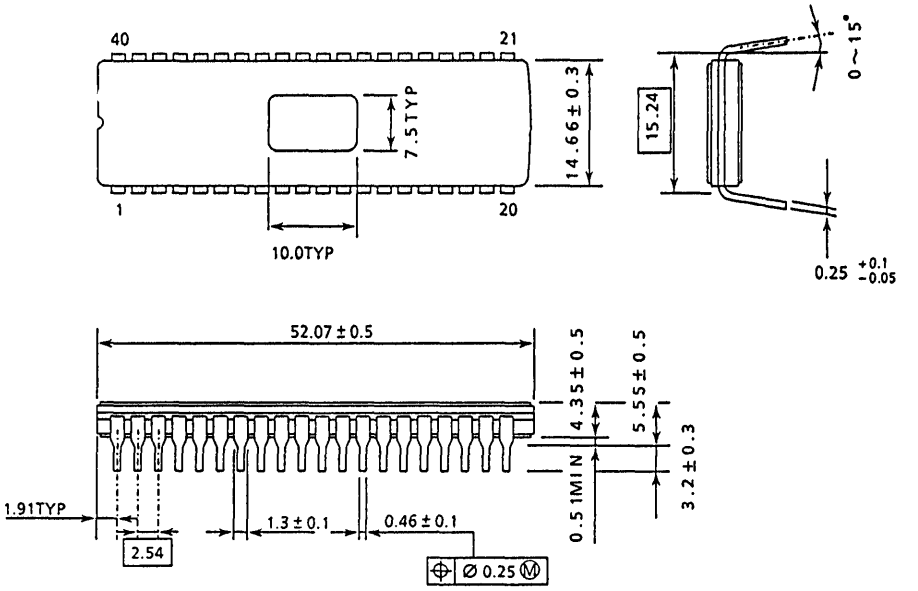
Note: $A9 = 12V \pm 0.5V$, $A_1 - A_8$, $A_{10} - A_{15}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ *: Don't care

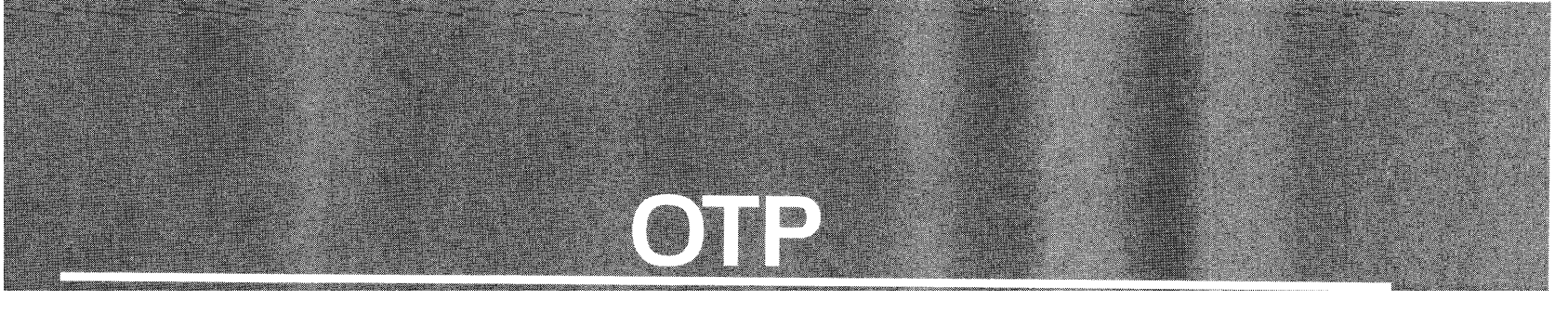
OUTLINE DRAWINGS

- Cerdip DIP

  WDIP40-G-600A

Unit : mm




OTP

32,768 WORD × 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

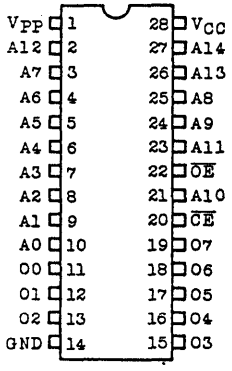
DESCRIPTION

The TC54256AP/AF is a 32,768 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic package. The TC54256AP/AF's access time is 200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC57256AD's. Once programmed, the TC54256AP/AF cannot be erased because of using plastic DIP without transparent window.

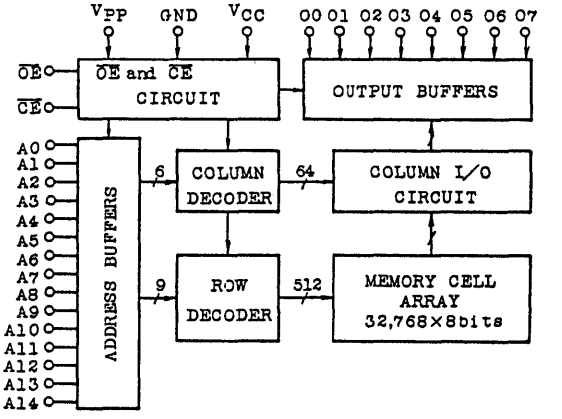
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  Active : 30mA/6.7MHz
  Standby: 100μA
- Fast access time: 200ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, TC57256D/AD, One time PROM TMM24256P/AP and TC54256P
- Standard 28 pin DIP plastic package: TC54256AP
- Plastic Flat Package : TC54256AF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A14	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ~ 14.0	V
V_{IN}	Input Voltage	-0.6 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ~ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	-65 ~ 125	°C
T_{OPR}	Operating Temperature	-40 ~ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	Vpp Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	

D.C. and OPERATING CHARACTERISTICS (Ta=-40 ~ 85°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0V ~ V_{CC}		-	-	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}$=0V	f=6.7MHz	-	-	30	mA
I_{CCO2}			f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	Vpp Current	V_{PP}=V_{CC}±0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ~ V_{CC}		-	-	±10	μA

A.C. CHARACTERISTICS (Ta=-40∼85°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	
t_{OH}	Output Data in Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	

A.C. TEST CONDITIONS

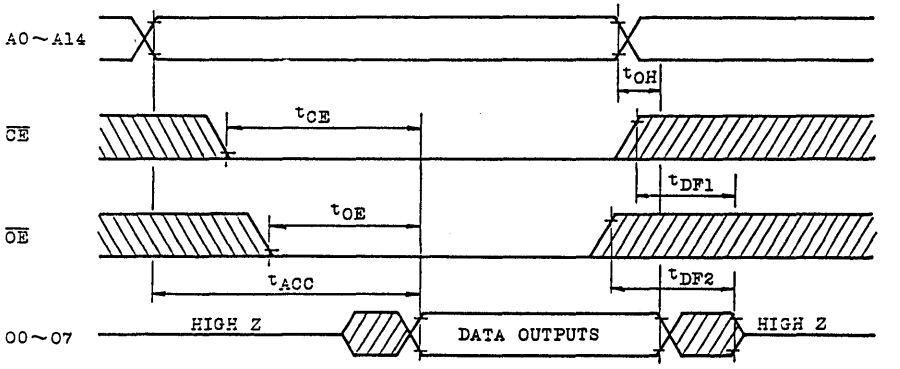
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V∼2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	130	ns

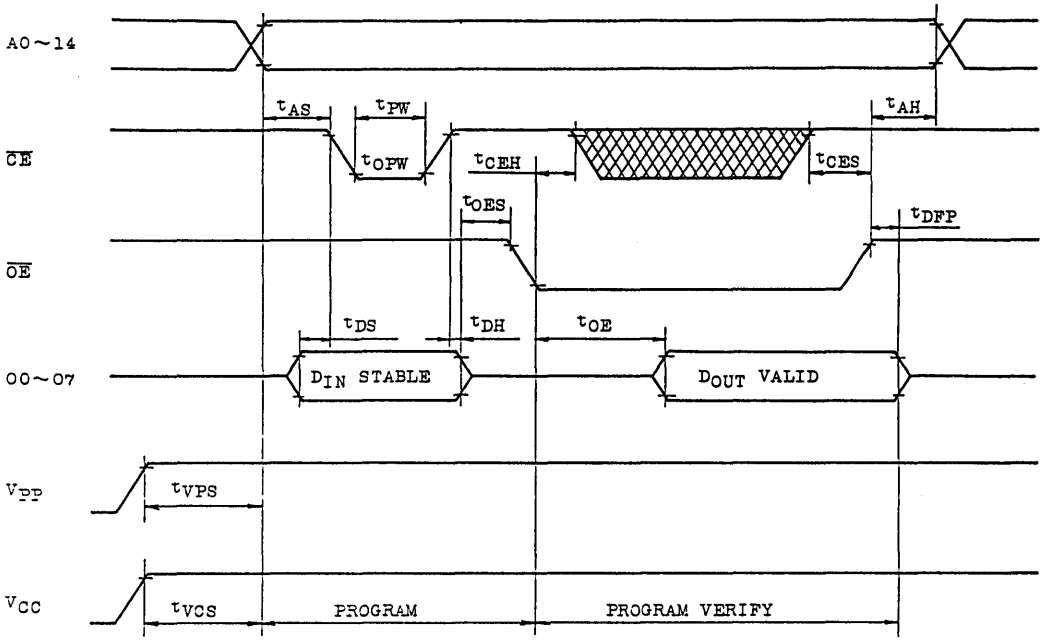
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC54256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=-40 ∿ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC54256AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TC54256AP/AF's can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54256AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC54256AP/AF is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54256AP/AF are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TC54256AP/AF is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-Low level under $\overline{OE}=V_{IH}$.
The TC54256AP/AF can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL}.

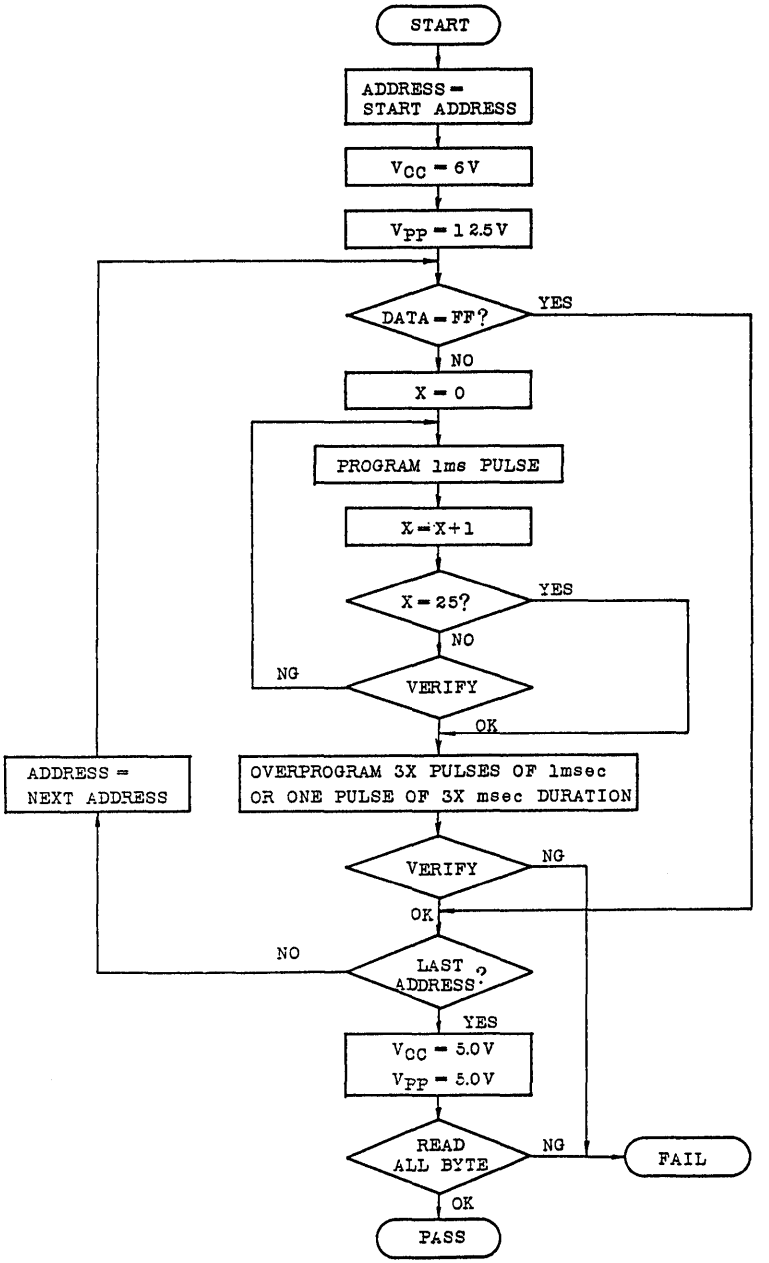
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TC54256AP/AF from being programmed.
Programming of two or more TC54256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54256AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7). The following table shows electric signature of TC54256AP/AF.

PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

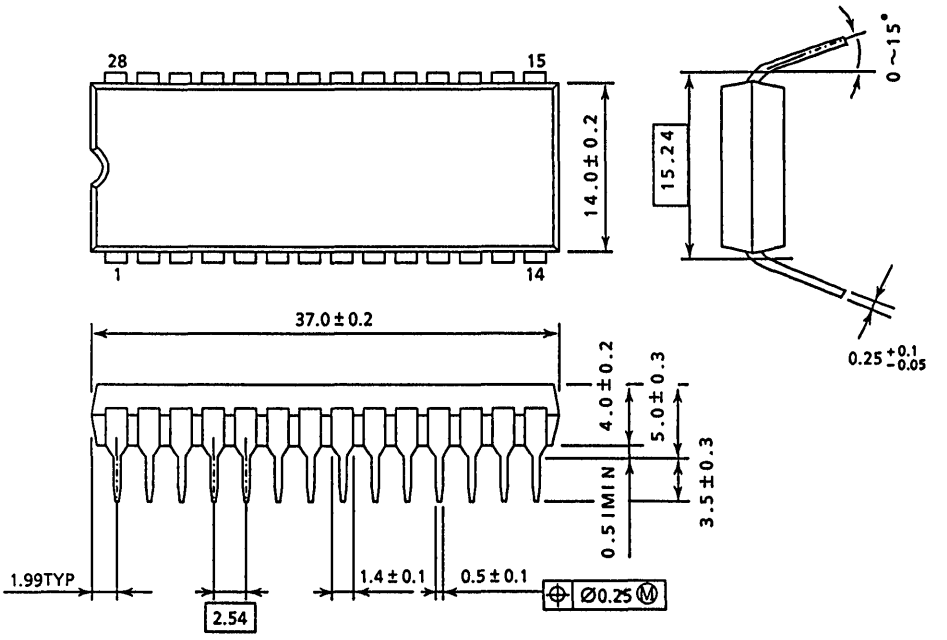
Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS

DIP28-P-600

Unit: mm

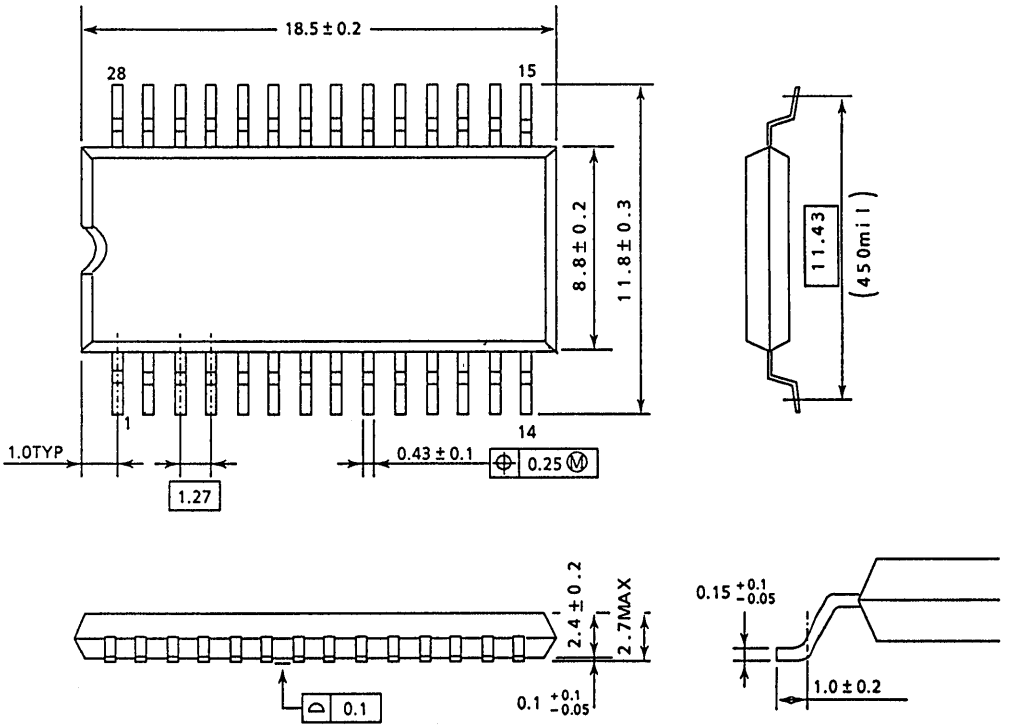


Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

SOP28-P-450

Unit : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

65,536 WORDS x 8 BITS CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

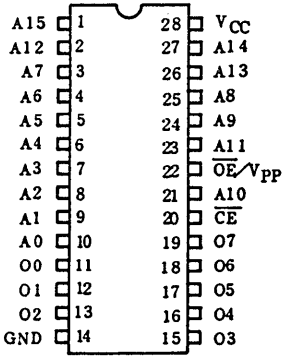
DESCRIPTION

The TC54512AP/AF is a 65,536 word × 8 bit CMOS one time programmable read only memory, and molded in a 28 pin plastic package. For read operation, the TC54512AP/AF's access time is 150ns/200ns, and the TC54512AP/AF operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/5.9MHz and standby current to 100μA. The electrical characteristics and programming method are the same as U.V. EPROM TC57512AD's. Once programmed, the TC54512AP/AF cannot be erased because of using plastic DIP without transparent window.

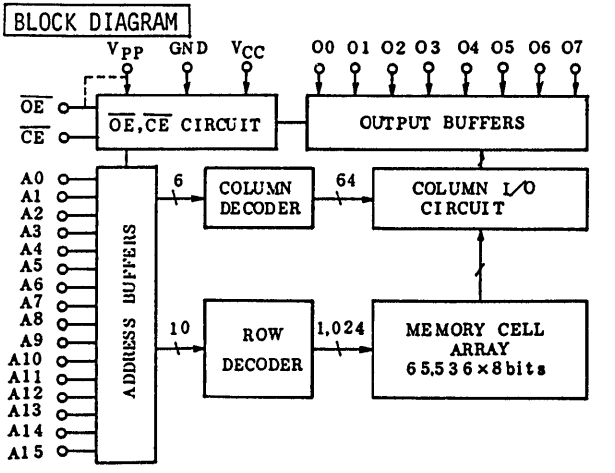
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Fast access time:
  TC54512AP/AF-15 150ns
  TC54512AP/AF-20 200ns
- Low power dissipation
  Active : 30mA/5.9MHz
  Standby: 100μA
- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Standard 28 pin DIP plastic package: TC54512AP
- 28 pin plastic Flat Package : TC54512AF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A15	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$/Vpp	Output Enable Input / Program Supply Voltage
VCC	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$/Vpp (22)	VCC (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	Vpp	6V 1)	Data In	Active
Program Inhibit	H	Vpp	2)	High Impedance	
Program Verify	L	L	6.25V	Data Out	

*: H or L

1): HIGH SPEED PROGRAMMING MODE I

2): HIGH SPEED PROGRAMMING MODE II

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature·Time	260 · 10	°C·sec
T_{STG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC54512AP/AF-15/TC54512AP/AF-20
Ta	Operating Temperature	-40 ∿ 85°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4 ∿ V_{CC}		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$=0V, I_{OUT}=0mA	f=5.9MHz	-	-	30	mA
I_{CC02}			f=1MHz	-	-	15	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{IH}	Input High Voltage	-		2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-		-0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PPI}	V_{PP} Current	V_{PP}=0 ∿ V_{CC}+0.6		-	-	±10	μA

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TC54512AP/AF-15		TC54512AP/AF-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	150	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	70	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	0	-	ns

A.C. TEST CONDITIONS

Output Load : 1 TTL Gate and C_L=100pF

Input Pulse Rise and Fall Times : 10ns Max.

Input Pulse Levels : 0.45V ~ 2.4V

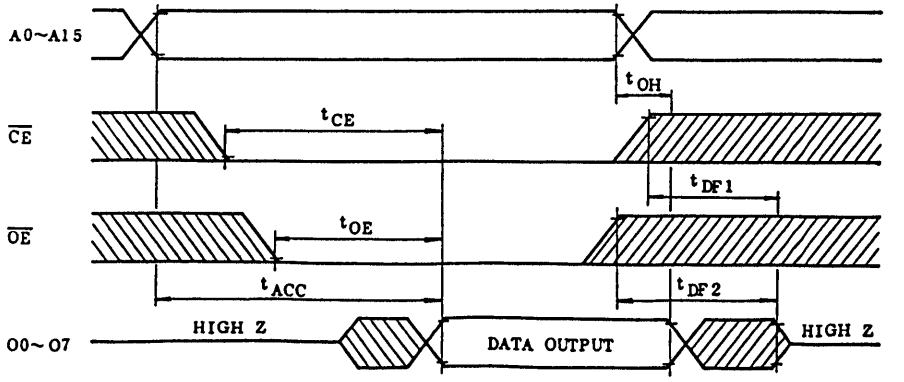
Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{IN2}	$\overline{OE}$/V_{PP} Input Capacitance	V_{IN}=0V	-	50	60	pF
C_{OUT}	Output Capacitance	V_{OUT}=V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM MODE I

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

DC and OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}$/V_{PP} Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}$/V_{PP} Hold Time	-	2	-	-	μs
t_{PRT}	$\overline{OE}$/V_{PP} Pulse Rise Time	-	50	-	-	ns
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VR}	$\overline{OE}$/V_{PP} Recovery Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$/V_{PP}=V_{PP}	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}$/V_{PP}=V_{IL}	-	-	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$/V_{PP}=V_{IL}	-	-	130	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

HIGH SPEED PROGRAM MODE II

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.0	6.25	6.5	V
V_{PP}	V_{PP} Power Supply Voltage	12.5	12.75	13.0	V

DC and OPERATING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.75V\pm0.25V$)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$V_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.75V\pm0.25V$)

SYMBOL	PAPAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}$/Vpp Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}$/Vpp Hold Time	-	2	-	-	μs
t_{PRI}	$\overline{OE}$/Vpp Pulse Rise Time	-	50	-	-	ns
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VR}	$\overline{OE}$/Vpp Recovery Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}/V_{PP}=V_{PP}$	0.095	0.1	0.105	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	-	-	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	-	-	130	ns

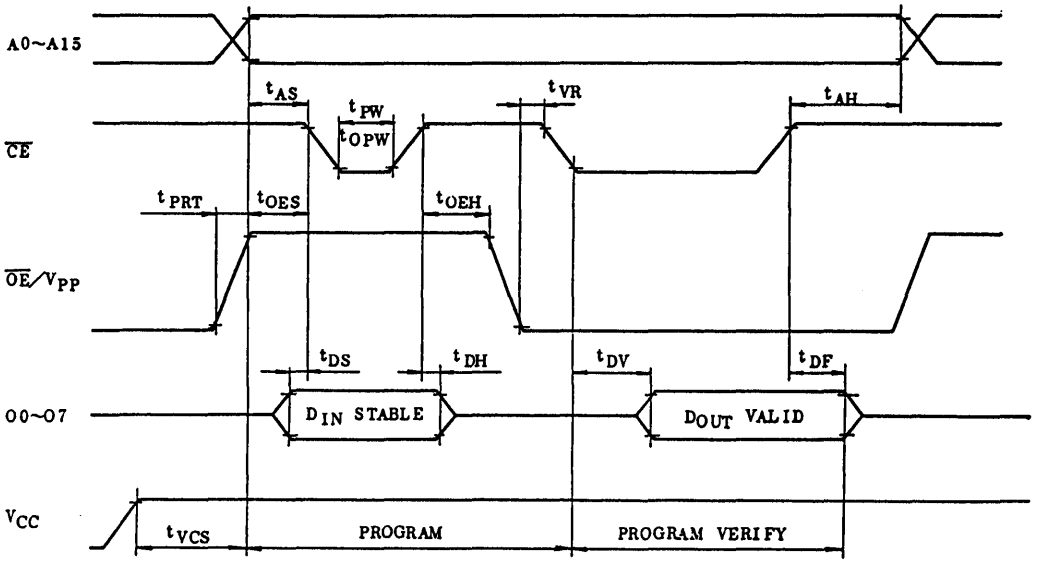
AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAMMING MODE I (V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

HIGH SPEED PROGRAMMING MODE II (V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5±0.5V or V_{PP}=12.75±0.25V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC54512AP/AF's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=-40 ∿ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V[1)] / 12.75V[2)]	6V[1)] / 6.25V[2)]	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *: V_{IH} or V_{IL},
1); HIGH SPEED PROGRAM MODE I
2); HIGH SPEED PROGRAM MODE II

READ MODE

The TC54512AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TC54512AP/AF's can be connected together on a common bus line. When $\overline{CE}$ is decode for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54512AP/AF has a low power standby mode controlled by the CE signal. By applying a high level to the $\overline{CE}$ input, the TC54512AP/AF is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54512AP/AF are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC54512AP/AF is in the programming mode when the $\overline{OE}$/Vpp input is at 12.5V or 12.75V and $\overline{CE}$ is at TTL-Low level. The TC54512AP/AF can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$/Vpp at V_{IL} and $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V or +12.75V) is applied to Vpp terminal, a high level $\overline{CE}$ input inhibits the TC54512AP/AF from being programmed. Programming of two or more TC54512AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for CE may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

This high speed programming mode I is performed at V_{CC}=6.0V and $\overline{OE}/V_{PP}$=12.5V. The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=5V.

HIGH SPEED PROGRAM MODE II

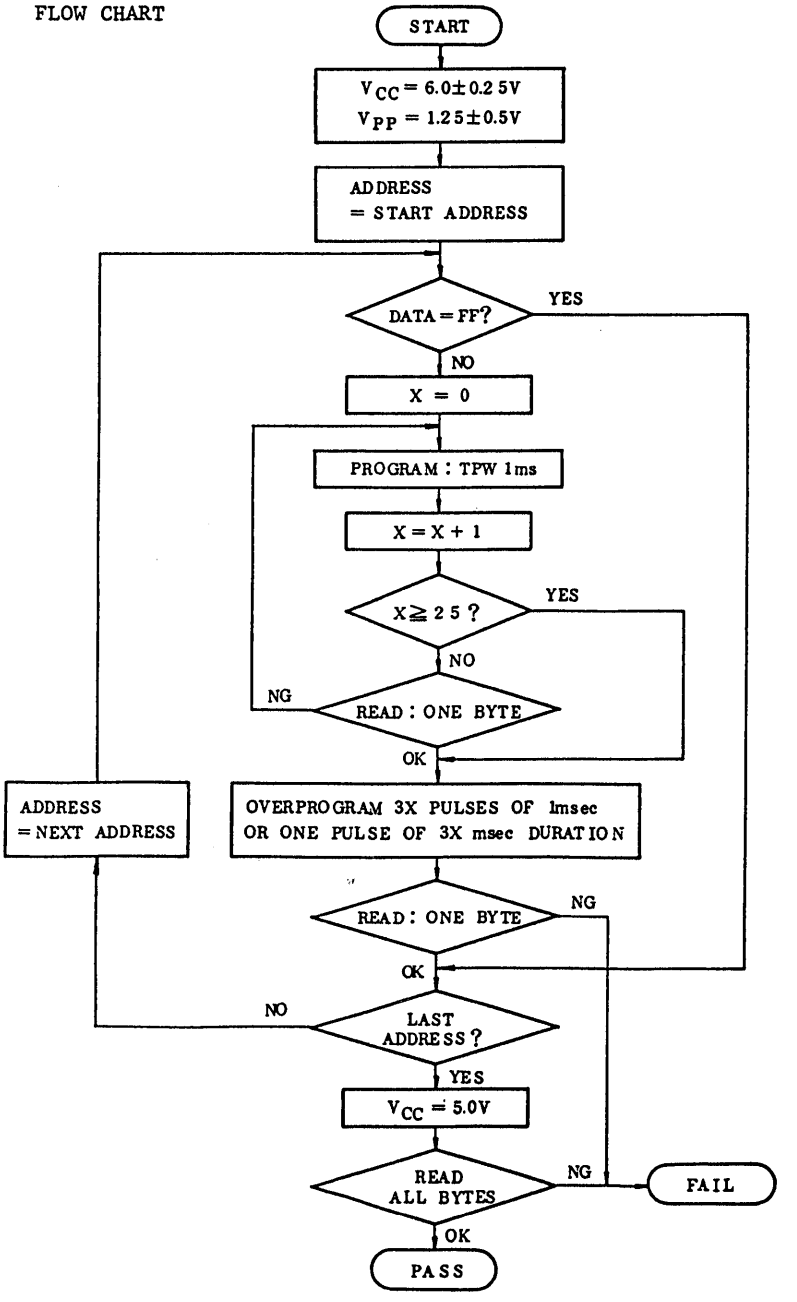
The program time can be greatly decreased by using this high speed programming mode II. This high speed programming mode II is performed at V_{CC}=6.25V and $\overline{OE}/V_{PP}$=12.75V. The programming is achieved by applying a single TTL low level 0.1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with V_{CC}=5V.

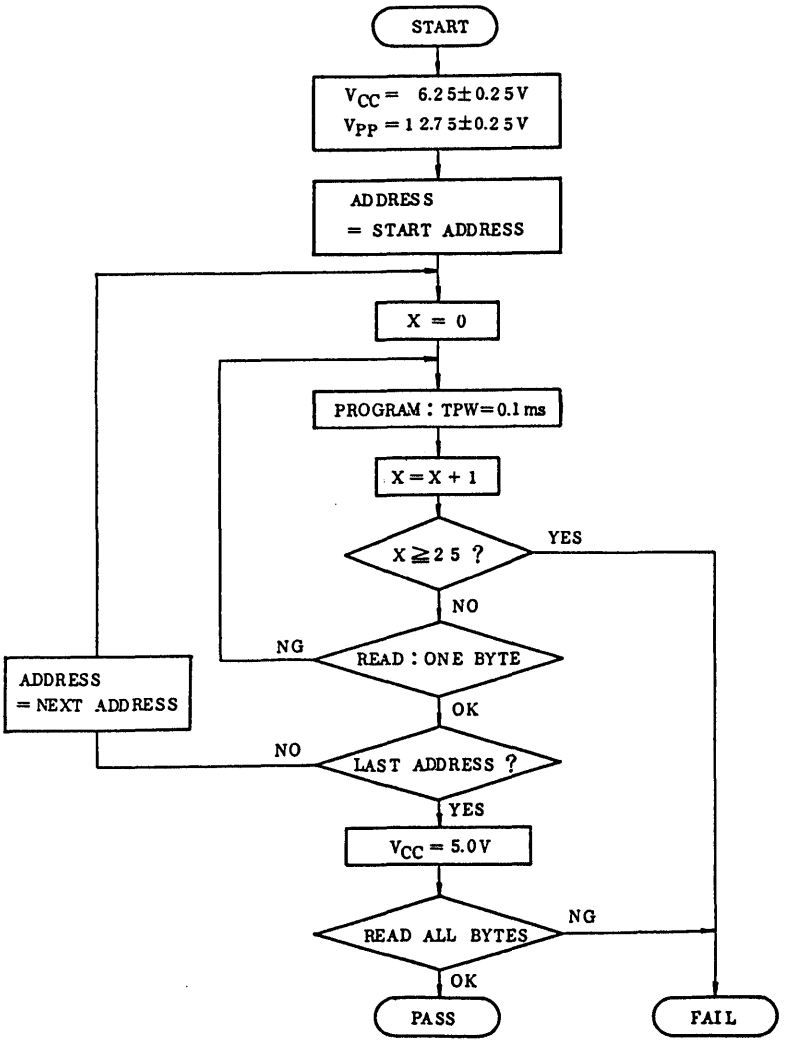
HIGH SPEED PROGRAM MODE I

FLOW CHART



HIGH SPEED PROGRAM MODE II

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54512AP/AF which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC54512AP/AF by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TC54512AP/AF.

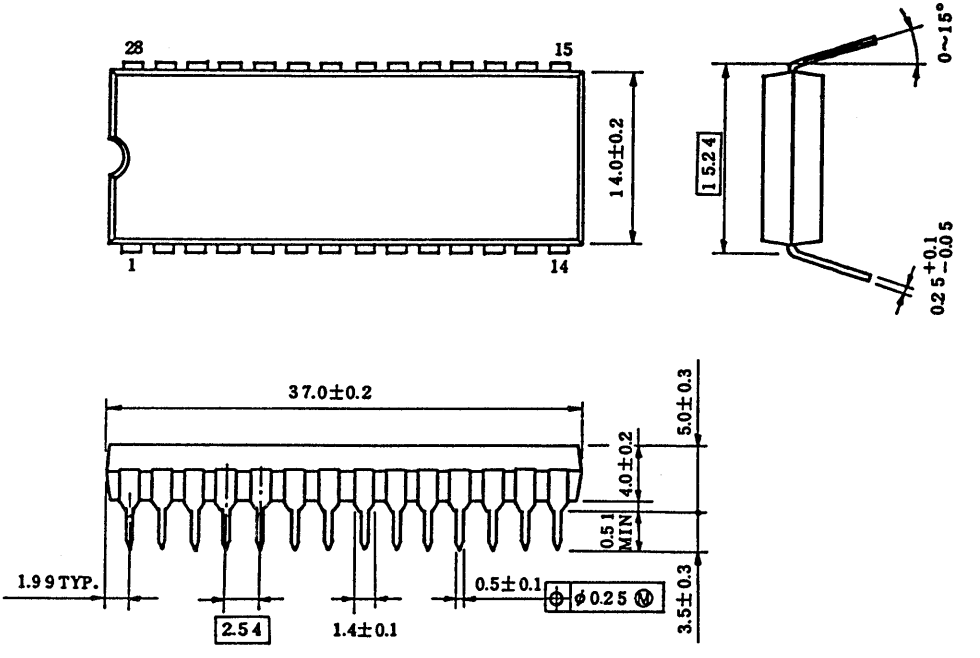
PINS / SIGNATURE	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A15, $\overline{CE}$, $\overline{OE}$=V_{IL}

OUTLINE DRAWINGS (TC54512AP) DIP28-P-600

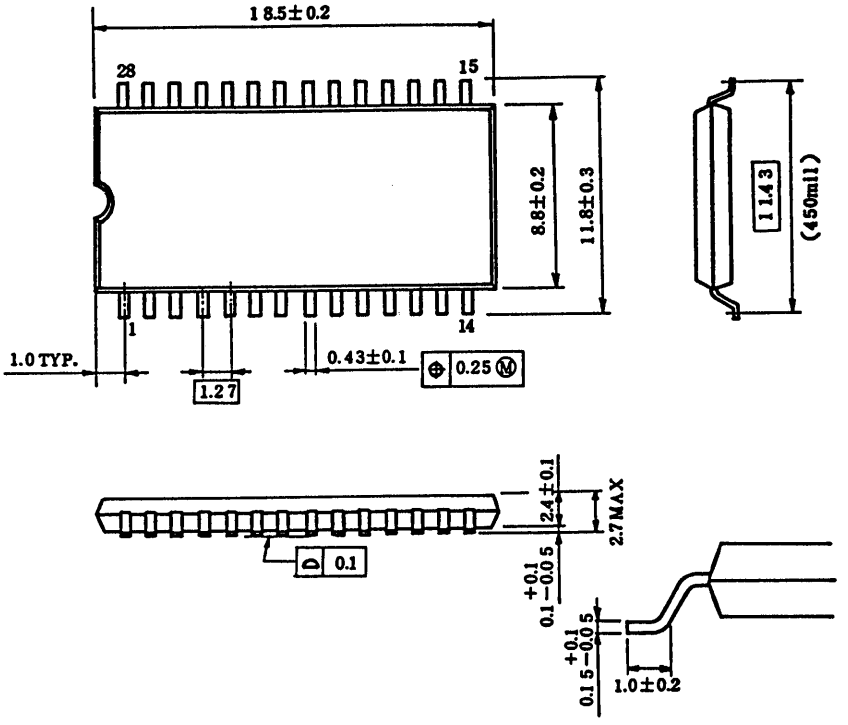
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (TC54512AF) SOP28-P-450

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

131,072 WORD x 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC541000J/TC541001J is a 131,072 word × 8 bit one time programmable read only memory, and molded in a 32 pin plastic package.

The TC541000J/TC541001J's access time is 150ns/200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC571000D/TC571001D's.

Once programmed, the TC541000J/TC541001J cannot be erased because of using plastic package without transparent window.

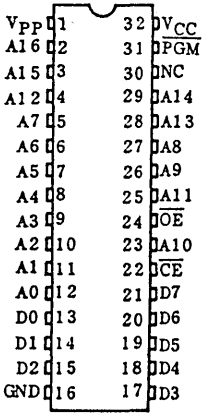
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Access Time

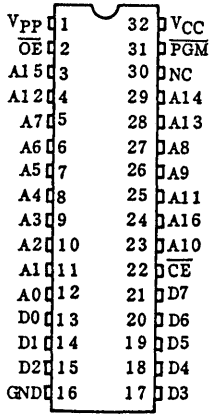
	-15	-20
Temp	0 ~ 70°C	-40 ~ 85°C
t_{ACC}	150ns	200ns

- Low power dissipation
  Active : 30mA/6.7MHz
  Standby: 100μA (Ta=85°C)
- Single 5V power supply
- Full static operation
- High speed programming operation: t_{PW} 0.1ms
- Input and output TTL compatible
- Standard 32 pin DIP plastic package

PIN CONNECTION (TOP VIEW)

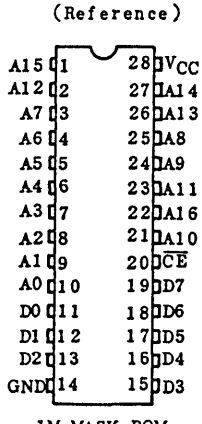


TC541000J



TC541001J

(Reference)



(1M MASK ROM TC531000P)

PIN NAMES

A0~A16	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	

DC and OPERATING CHARACTERISTICS (Ta=-40∿85°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0∿V_{CC}		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$=0V, I_{OUT}=0mA	f=6.7MHz	-	-	30	mA
I_{CC02}			f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=V_{CC}±0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V∿V_{CC}		-	-	±10	μA

Ta=0∿70°C for TC541000J/TC541001J-15

AC CHARACTERISTICS (Ta=-40∿85°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

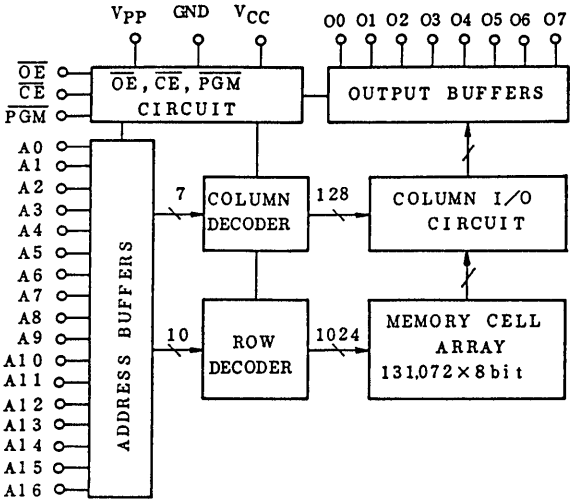
SYMBOL	PARAMETER	TC541000J/1001J -15		TC541000J/1001J -20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Vaild	-	150	-	200	
t_{OE}	$\overline{OE}$ to Output Vaild	-	70	-	70	
t_{PGM}	PGM to Output Vaild	-	70	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	
t_{DF3}	PGM to Output in High-Z	0	60	0	60	
t_{OH}	Output Data Hold Time	0	-	0	-	

Ta=0∿70°C for TC541000J/TC541001J-15

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O0∿O7	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

*: H or L

MAXIMUM RATINGS

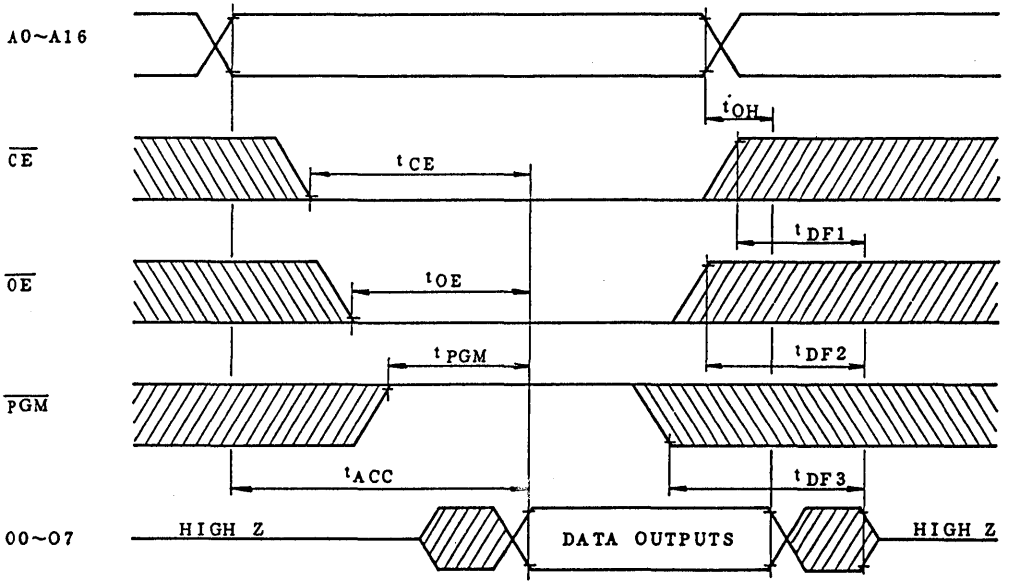
SYMBOL	ITEM	RATING	UNIT
V_{CC}	VCC Power Supply Voltage	-0.6∿7.0	V
V_{PP}	Program Supply Voltage	-0.6∿14.0	V
V_{IN}	Input Voltage	-0.6∿7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6∿V_{CC}+0.5	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature . Time	260 • 10	°C•sec
T_{STRG}	Storage Temperature	-65∿125	°C
T_{OPR}	Operating Temperature	-40∿85	°C

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	10	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	

DC AND OPERATING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6.25\pm0.25V$, $Vpp=12.75\pm0.25V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6.25\pm0.25V$, $V_{PP}=12.75\pm0.25V$)

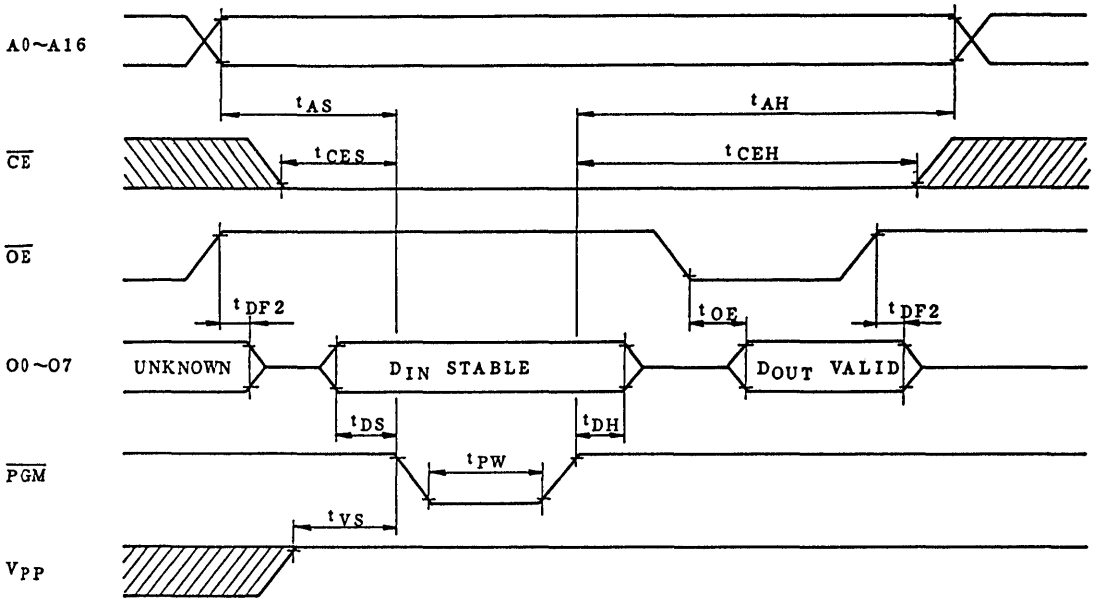
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	-	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	-	-	-	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	-	-	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC541000J/TC541001J's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

PINS		$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O0 ∿ O7	POWER
READ OPERATION (Ta=-40 ∿ 85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}
Ta=0 ∿ 70°C for TC541000J/TC574001J-15

READ MODE

The TC541000J/TC541001J has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.
Assuming in that $\overline{CE}$=$\overline{OE}$=V_{IL} and $\overline{PGM}$=V_{IH}, the output data is valid at the output after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL}, $\overline{PGM}$=V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.
And assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two or more ROMs can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC541000J/TC541001J has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC541000J/TC541001J is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC541000J/TC541001J are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The levels required for all inputs are TTL. The TC541000J/TC541001J can be programmed any location at anytime ------ either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and PGM at V_{IH}.

PROGRAM INHIBIT MODE

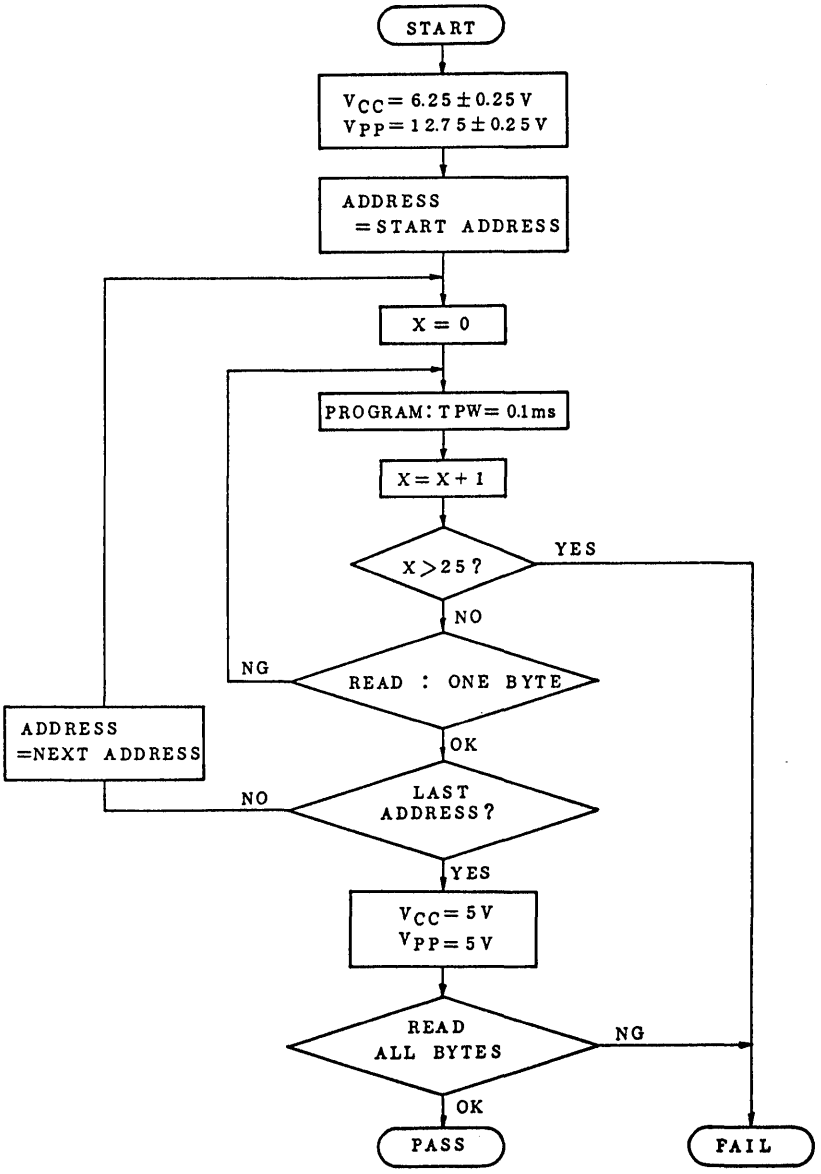
Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC541000J/TC541001J from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC}=6.25V and $\overline{PGM}$=V_{IH}.
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC541000J/TC541001J which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC541000J/TC541001J by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TC541000J/TC541001J.

PINS / SIGNATURE		A0	O7	O6	O5	O4	O3	O2	O1	O0	HEX DATA
Manufacture Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC541000J	V_{IH}	1	0	0	0	0	1	1	0	86
	TC541001J		0	0	0	0	0	1	1	1	07

Notes: A9=12V±0.5V

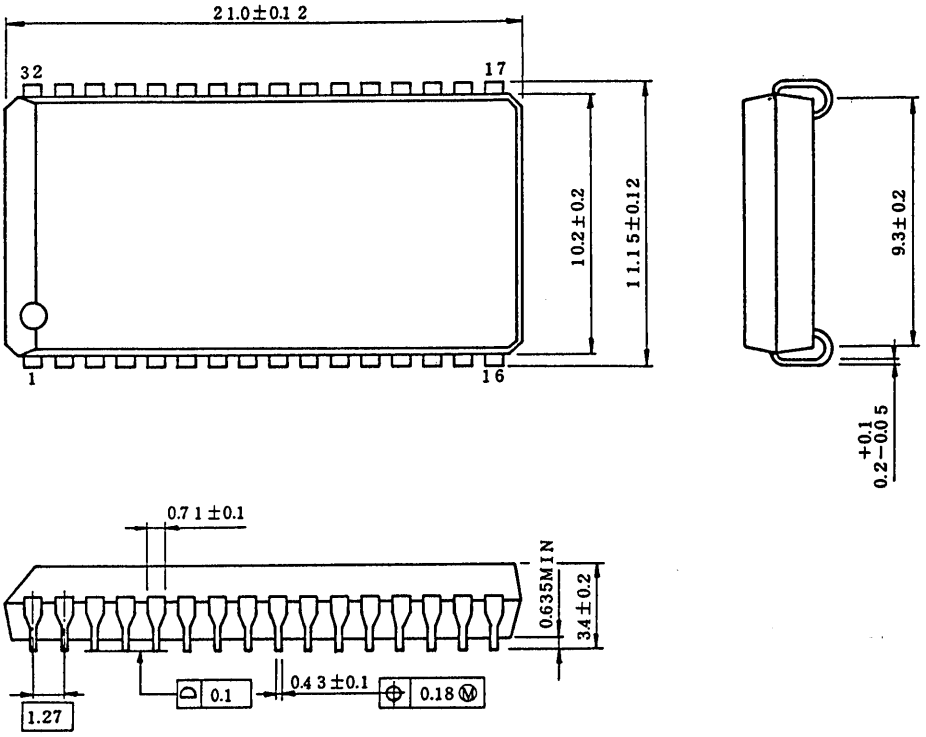
A1 ∿ A8, A10 ∿ A16, $\overline{CE}$, $\overline{OE}=V_{IL}$

$\overline{PGM}=V_{IH}$

OUTLINE DRAWINGS (SOJ32-P-400)

Plastic SOJ

Unit in mm



Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.

131,072 WORD x 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC541000P/F and TC541001P/F are a 131,072 word x 8 bit one time programmable read only memory and molded in a 32 pin plastic package.

The TC541000P/F and TC541001P/F's access time are 150ns/200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC571000D/TC571001D's. Once programmed, the TC541000P/F and TC541001P/F cannot be erased because of using plastic package without transparent window.

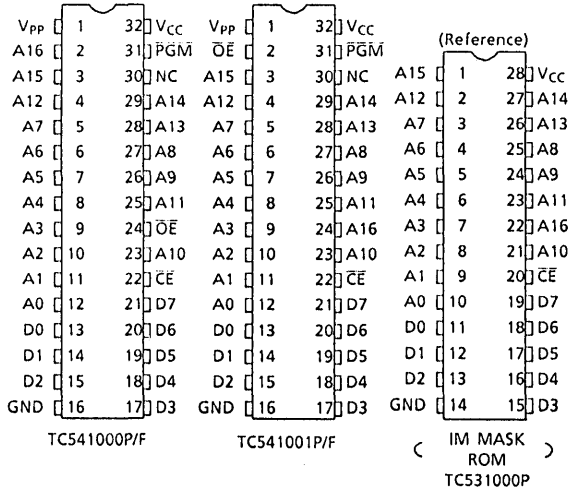
FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Access Time

	-15	-20
Temp	0~70°C	-40~85°C
t_{ACC}	150ns	200ns

- Low power dissipation
  Active : 30mA/6.7MHz
  Standby : 100μA
- Single 5V power supply
- Full static operation
- Hiigh speed programming operation : t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin : TC541000P/F
- 1M MROM compatible : TC541001P/F
- Standard 32 pin DIP plastic package : TC541000P/TC541001P
- S32Pin Plastic Flat Package : TC541000F/TC541001F

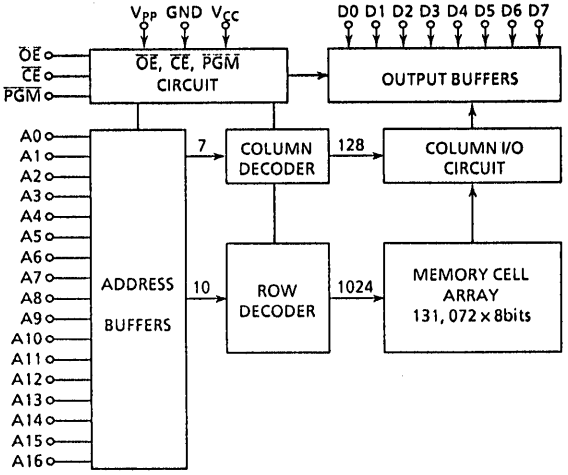
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A16	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	Power
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	- 0.6~7.0	V
V_{PP}	Program Supply Voltage	- 0.6~14.0	V
V_{IN}	Input Voltage	- 0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	- 0.6~V_{CC} + 0.5	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	- 65~125	°C
T_{OPR}	Operating Temperature	- 40~85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	– 0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	V_{CC} – 0.6V	V_{CC}	V_{CC} – 0.6	V

D.C. AND OPERATING CHARACTERISTICS (Ta = – 40~85℃, V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0~V_{CC}		–	–	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE}$ = 0V	f = 6.7MHz	–	–	30	mA
I_{CCO2}		I_{OUT} = 0mA	f = 1MHz	–	–	10	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = VIH		–	–	1	mA
I_{CCS2}		$\overline{CE}$ = V_{CC} – 0.2V		–	–	100	μA
V_{OH}	Output High Voltage	I_{OH} = – 400μA		2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		–	–	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = V_{CC} ± 0.6V		–	–	± 10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V~V_{CC}		–	–	± 10	μA

Ta = 0~70℃ for TC541000P/F/TC541001P/F – 15

A.C. CHARACTERISTICS (Ta = – 40~85℃, V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V)

SYMBOL	PARAMETER	TC541000P – 15 / TC541001P – 15 TC541000F – 15 / TC541001F – 15		TC541000P – 20 / TC541001P – 20 TC541000F – 20 / TC541001F – 20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	–	150	–	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	150	–	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	70	–	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	–	70	–	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	PGM to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	–	0	–	ns

Ta = 0~70℃ for TC541000P/F/TC541001P/F – 15

A.C. TEST CONDITIONS

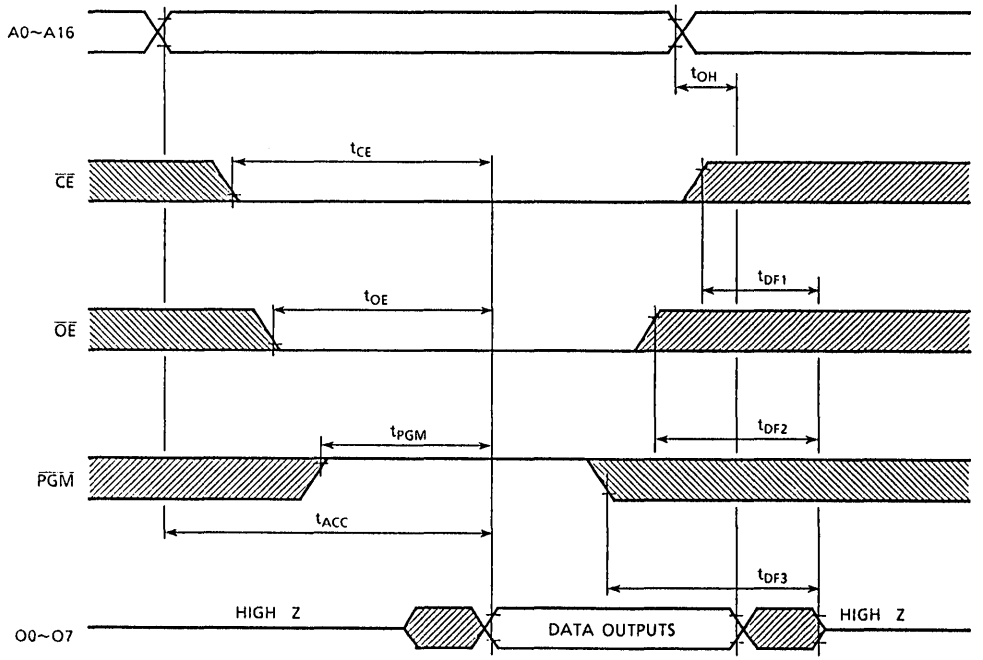
- Output Load : 1 TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	-	4	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	10	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

D.C. AND OPERATING CHARACTERISTICS (Ta = 25 ± 5°C, V_{CC} = 6.25 ± 0.25V, V_{PP} = 12.75 ± 0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0~V_{CC}	–	–	± 10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 13.0V	–	–	50	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta = 25 ± 5°C, V_{CC} = 6.25 ± 0.25V, V_{PP} = 12.75 ± 0.25V)

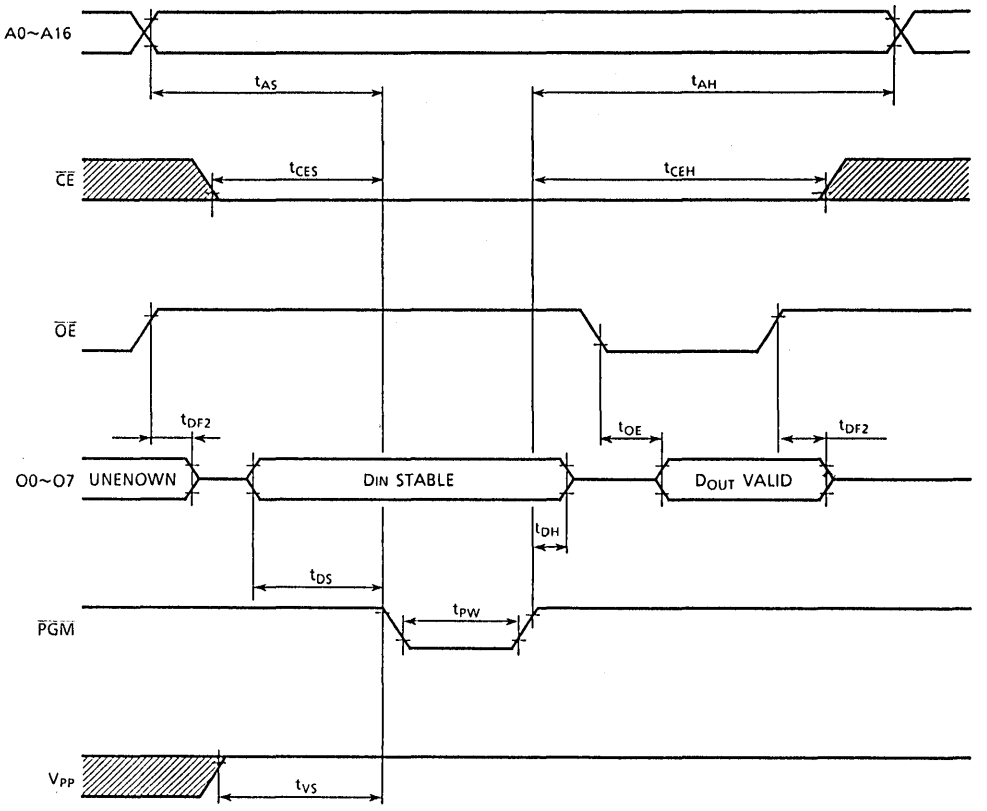
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	–	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}	–	–	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC541000P / F / TC541001P / F's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

		$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O0~O7	Power
READ OPERATION	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note : H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC541000P / F / TC541001P / F has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers independent of device selection.

Assuming in that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state.

So two or more ROMs can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC541000P/F/TC541001P/F has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC541000P/F/TC541001P/F is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC541000P/F/TC541001P/F are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC541000P/F/TC541001P/F can be programmed any location at anytime - either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC541000P/F/TC541001P/F from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

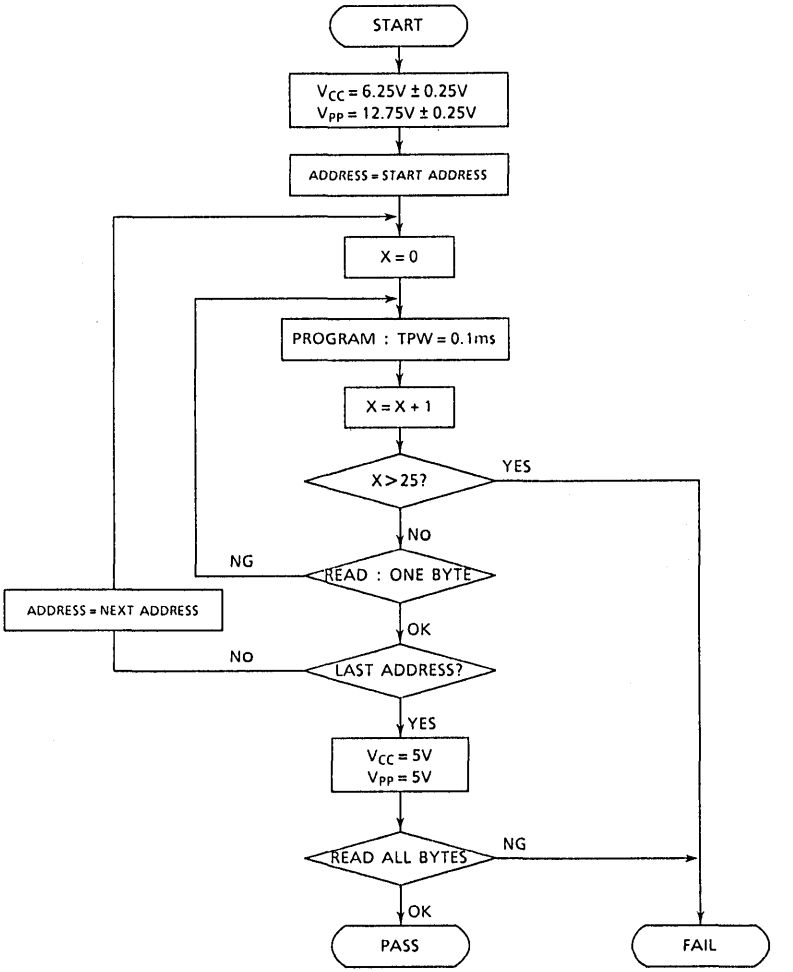
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC541000P / F / TC541001P / F which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC541000P / F / TC541001P / F by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TC541000P / F / TC541001P / F.

SIGNATURE \ PINS		A0	O7	O6	O5	O4	O3	O2	O1	O0	HEX. DATA
Manufacture Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC541000P / F	V_{IH}	1	0	0	0	0	1	1	0	86
	TC541001P / F		0	0	0	0	0	1	1	1	07

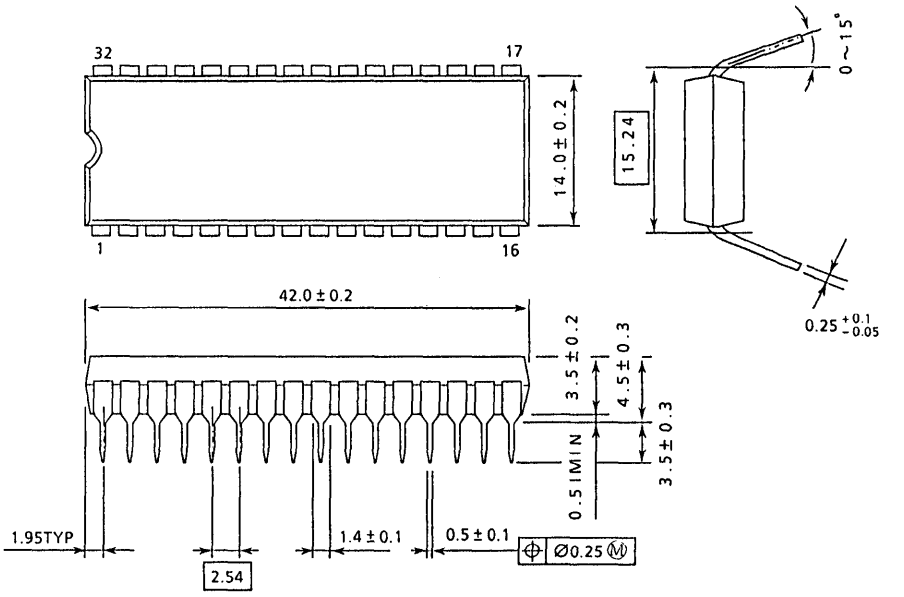
Notes : A9 = 12V ± 0.5V
A1~A8, A10~A16, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

• Plastic DIP

DIP32-P-600

Unit : mm



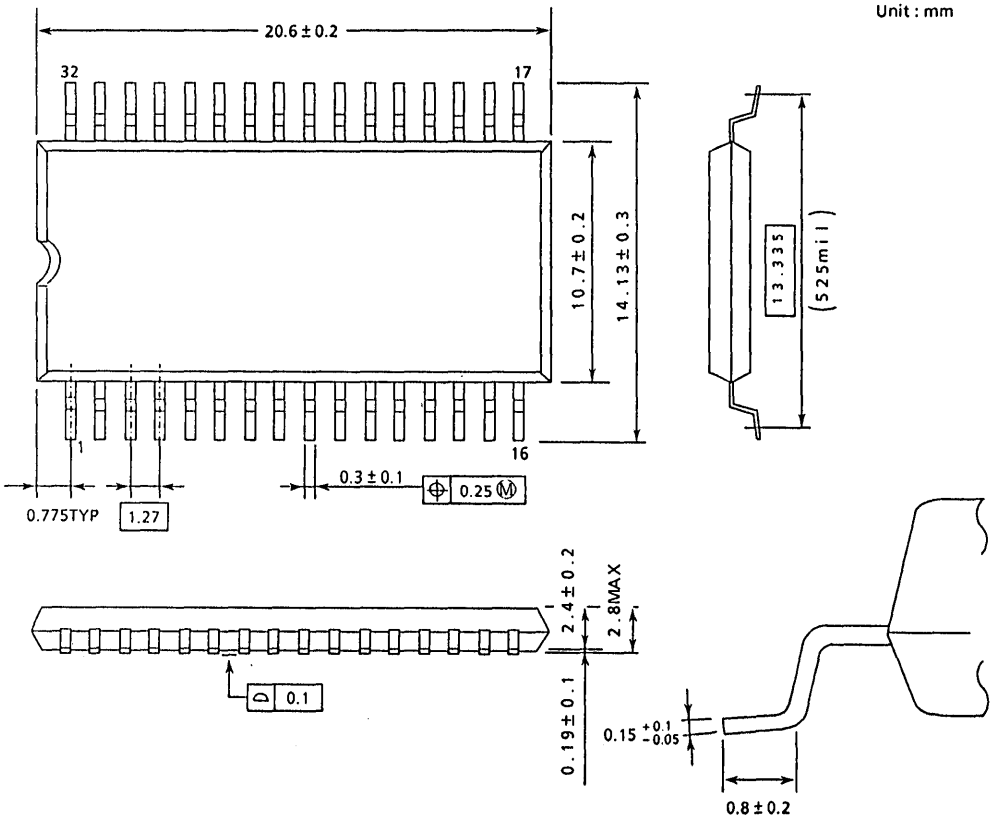
Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm

OUTLINE DRAWINGS

• Plastic SOP

SOP32-P-525

Unit : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm

524,288 WORD×8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC544000P/F is a 524,288 word × 8 bit one time programmable read only memory, and molded in a 32 pin plastic package. The access time of TC544000P/F is 120ns/150ns and has low power standby mode which reduces the power dissipation without increasing access time.

The electrical characteristics and programming method are the same as U.V. EPROM TC574000D's once programmed, the TC544000P/F cannot be erased because of using plastic DIP without transparent window.

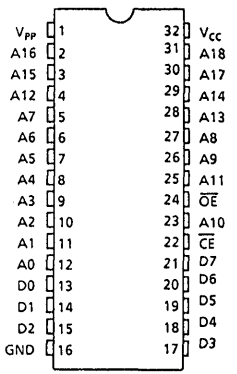
FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Access time

	-12	-120	-150
V_{CC}	5V ± 5%	5V ± 10%	
Temp	0°C~70°C		
t_{ACC}	120ns		150ns

- Low power dissipation
  Active : 60mA/8.3MHz
  Standby: 100μA (Ta=70°C)
- High speed programming operation
- Single 5V power supply
- Full static operation
- Input and output TTL compatible
- JEDEC standard 32 pin
- Standard 32 pin DIP plastic package : TC544000P
  32 pin plastic Flat Package : TC544000F

PIN CONNECTION (TOP VIEW)

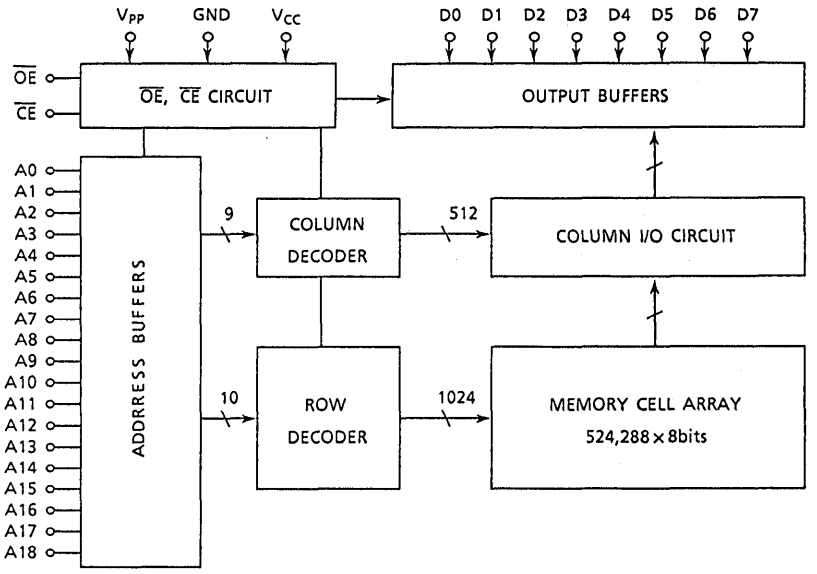


TC544000P/F

PIN NAMES

A0~A18	Address Inputs
D0~D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~D7	Power
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.50V	6.25V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{IN} (A9)	Input Voltage (A9)	−0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	−0.6~V_{CC} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~125	°C
T_{opr}	Operating Temperature	0~70	°C

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC544000P/F-12	TC544000P/F-120/-150
V_{IH}	Input High Voltage	2.2V~V_{CC}+0.3V	2.2V~V_{CC}+0.3V
V_{IL}	Input Low Voltage	-0.3V~0.8V	0.3V~0.8V
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6V~V_{CC}+0.6V	V_{CC}-0.6V~V_{CC}+0.6V

DC AND OPERATING CHARACTERISTICS (Ta=0~70°C)

SIMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		-	-	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}$=V_{IL}, I_{OUT}=0mA	f=8.3MHz	-	-	60	mA
			f=6.7MHz	-	-	50	
I_{CCO2}			f=1MHz	-	-	15	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=V_{CC}±0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V~V_{CC}		-	-	±10	μA

AC CHARACTERISTICS (Ta=0~70°C, V_{PP}=V_{CC}±0.6V)

SIMBOL	PARAMETER	TEST CONDITION	TC544000P/F-12/-120		TC544000P/F-150		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	120	-	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	120	-	150	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	60	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	50	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	50	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	0	-	ns

AC TEST CONDITIONS

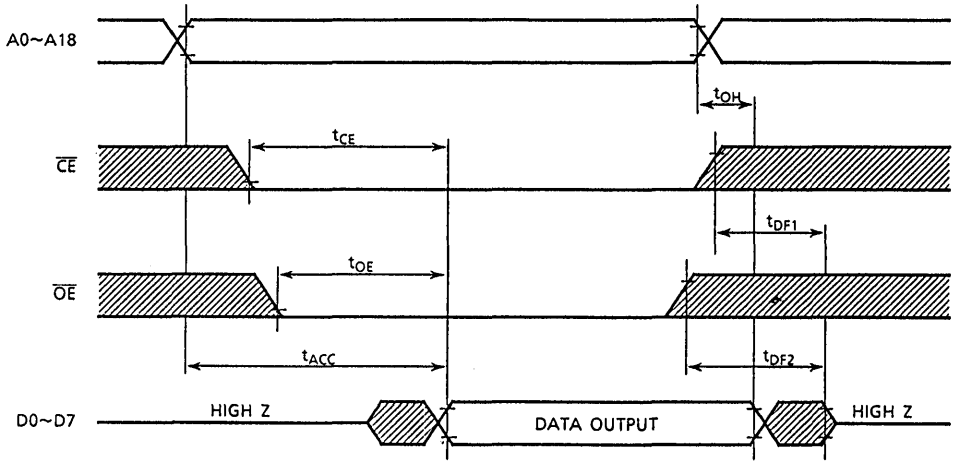
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	-	9	PF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	13	

*This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPERATING CHARACTERISTICS ($Ta=25\pm5°C, V_{CC}=6.25V\pm0.25V, Vpp=12.50V\pm0.30V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=12.8V$	–	–	50	mA

AC PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.50V\pm0.30V$)

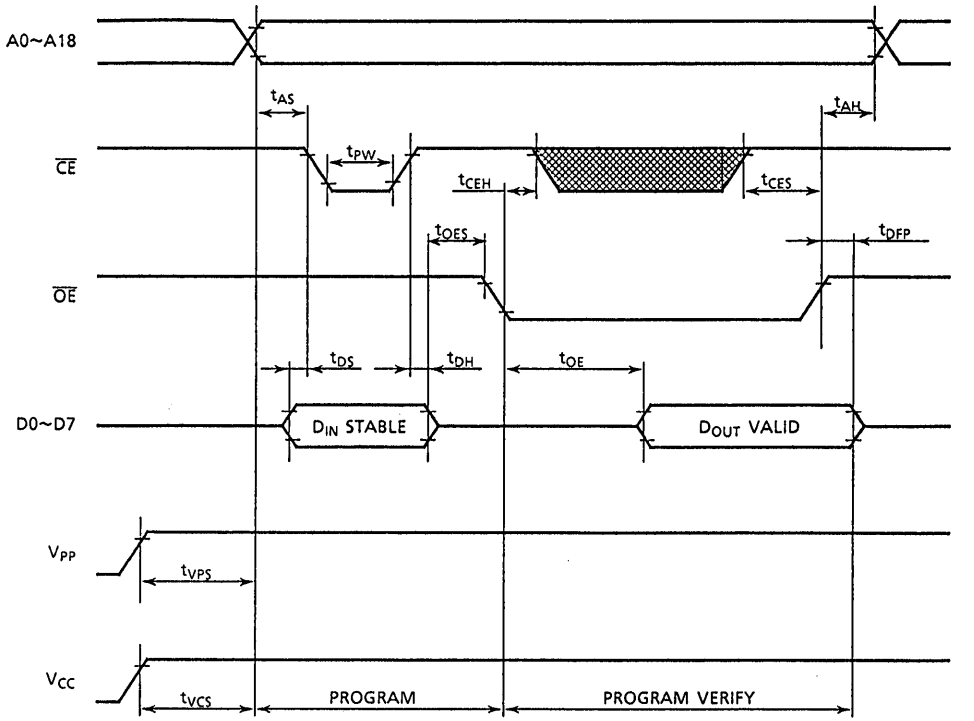
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	μs
t_{OES}	$\overline{OE}$ Set up Time	–	2		–	μs
t_{DS}	Data Set up Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VPS}	V_{PP} Set up Time	–	2	–	–	μs
t_{VCS}	V_{CC} Set up Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	45	50	55	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	–	–	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	–	–	90	ns

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with VPP=12.50V may cause permanent damage to the device.

3. The VPP supply voltage is permitted up to 14V for program operation.
So the voltage over 14V should not be applied to the VPP terminal.
When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC544000P / F's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (22)	$\overline{OE}$ (24)	V_{PP} (1)	V_{CC} (32)	D0~D7 (13~15, 17~21)	POWER
Read Operation (Ta = 0~70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselet	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta = 25 ± 5°C)	Program	L	H	12.50V	6.25V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC544000P / F has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC544000P / F's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC544000P / F has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC544000P / F is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC544000P/F are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC544000P/F is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at Low under $\overline{OE}=V_{IH}$.

The TC544000P / F can be programmed any location at any time either indivicually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ and $\overline{OE}$ input inhibits the TC544000P/F from being programmed.

Programming of two or more TC544000P / F's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a low level program pulse is applied to the $\overline{CE}$ of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$.

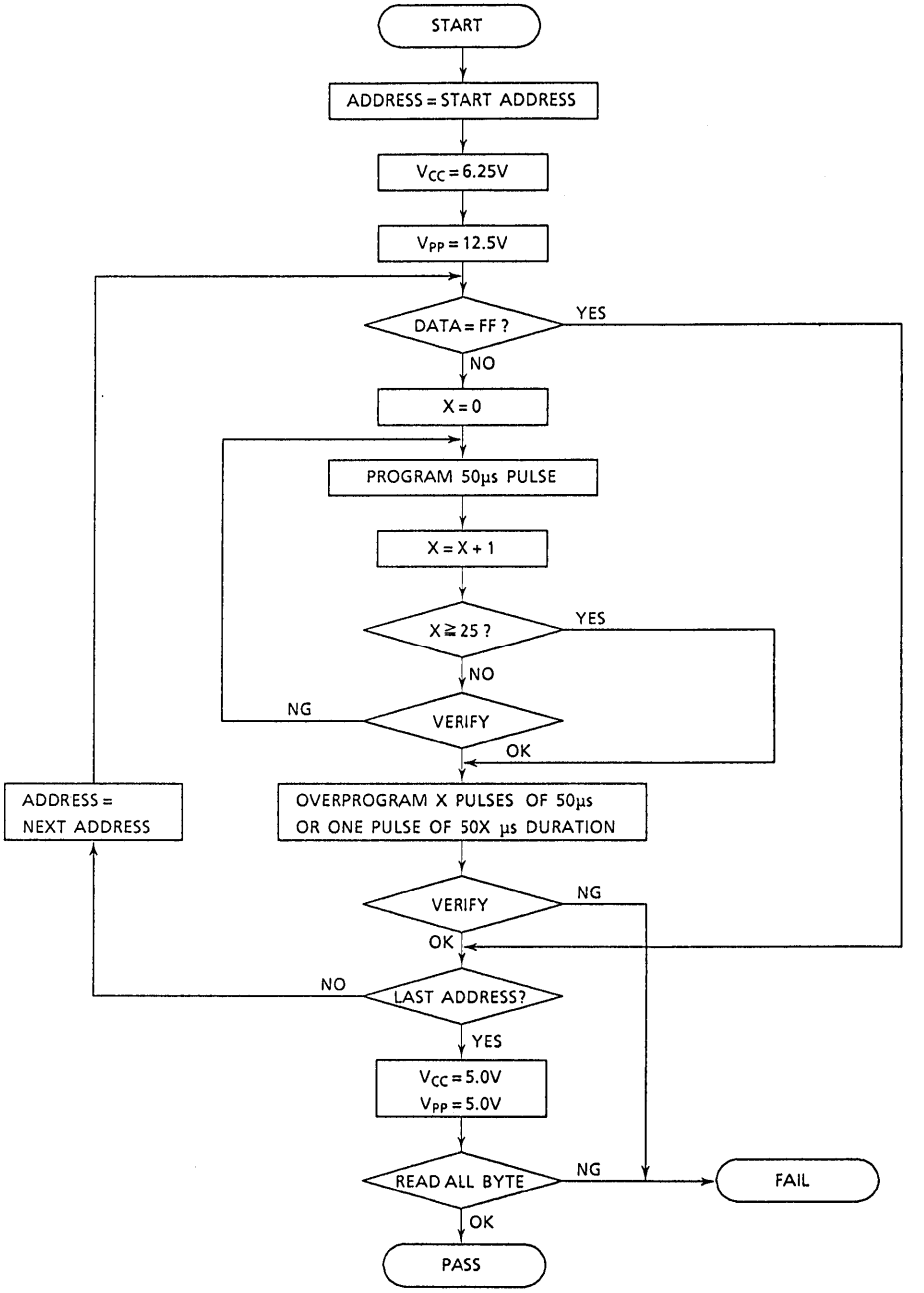
The programming is achieved by applying a single low level 50μs pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 50μs is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC544000P / F which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC544000P / F by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC544000P / F.

PINS / SIGNATURE	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	0	1	1	0	0	8C

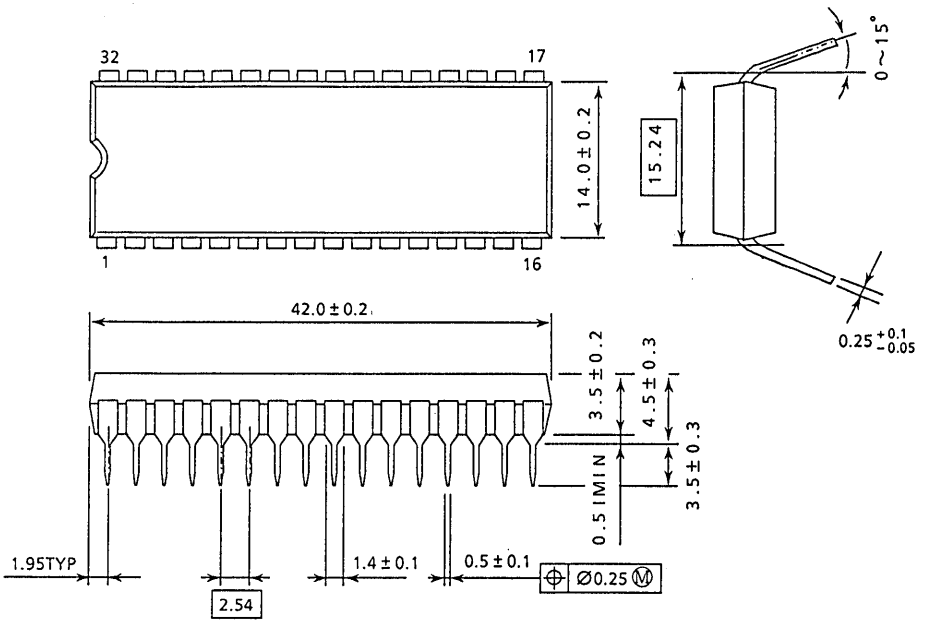
Notes: A9 = 12V ± 0.5V
A1~A8, A10~A18, $\overline{CE}$, $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS

- Plastic DIP

DIP32-P-600

Unit : mm



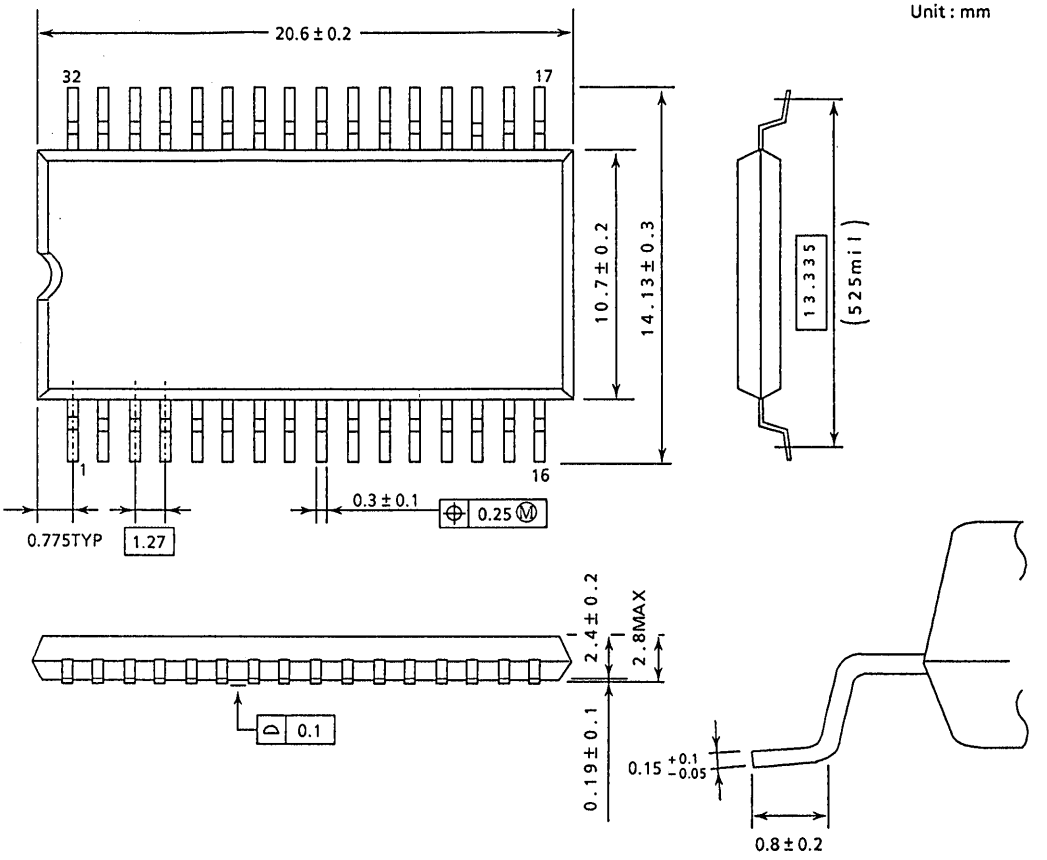
Note : Package width and length do not include mold protrusion, allowable mode protrusion is 0.15mm.

OUTLINE DRAWINGS

- Plastic SOP

SOP32-P-525

Unit : mm



Note : Package width and length do not include mold protrusion, allowable mode protrusion is 0.15mm.

HIGH-SPEED OTP

1 MEGA BIT (65,536 WORD × 16 BIT)
CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC54H1024P/F is a 65,536 word × 16 bit one time programmable read only memory. and molded in a 40 pin plastic package.

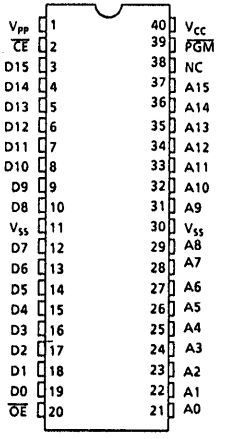
TC54H1024P/F is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 40mA/1MHz.

The electrical characteristics and programming method are the same as U.V.EPROM TC57H1024D. Once programmed, the TC54H1024P/F cannot be erased because of using plastic package without transparent window.

FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Fast access time
  TC54H1024P/F-85 : 85ns
  TC54H1024P/F-10 : 100ns
- Low power dissipation
  Active : 40mA/1MHz
  Standby : 100μA
- Single 5V power supply
- Full static operation
- High speed programming operation : t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 40 pin
- TC54H1024P : standard 40pin plastic package
- TC54H1024F : 40pin plastic package

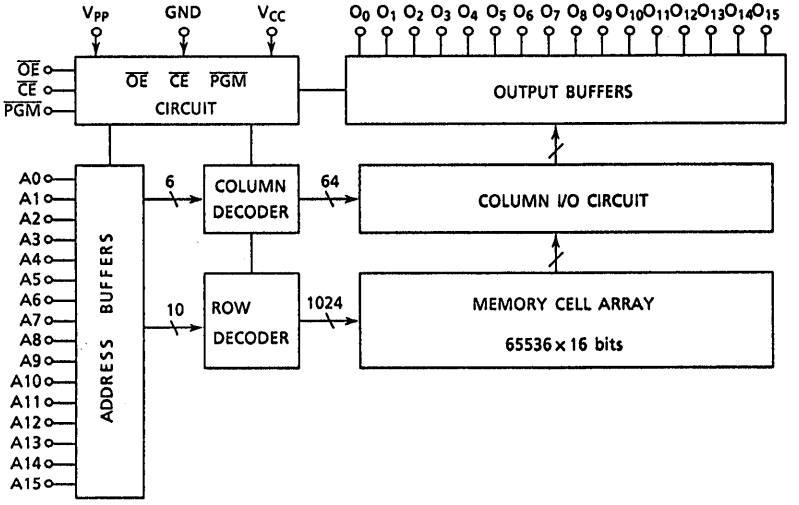
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
Read	L	L	H	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*	*				Standby
Program	L	*	L	12.75V	6.25V	Data In	Active
Program Inhibit	H	*	*			High Impedance	
	L	H	H				
Program Verify	L	L	H			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{IN} (A9)	Input Voltage (A9)	−0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	−0.6~V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260·10	°C·sec
T_{strg}	Storage Temperature	−65~125	°C
T_{opr}	Operating Temperature	0~70	°C

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC54H1024P/F-85/10
Ta	Ambient Temperature	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V ± 5%
V_{PP}	V_{PP} Power Supply Voltage	0V~V_{CC} + 0.6V

DC and OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0~V_{CC}		-	-	± 10	μA
I_{CCO}	Operating Current	$\overline{CE}$ = 0V I_{OUT} = 0mA	t_{cycle} = 1μs	-	-	40	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$ = V_{CC} - 0.2V		-	-	100	μA
V_{IH}	Input High Voltage	——		2.2	-	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	——		- 0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH} = - 400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = V_{CC} ± 0.6V		-	-	± 10	μA
I_{LO}	Ouptut Leakage Current	V_{OUT} = 0.4V~V_{CC}		-	-	± 10	μA

AC CHARACTERISTICS (VPP = 0V~VCC + 0.6V)

SYMBOL	PARAMETER	TC54H1024P/F-85		TC54H1024P/F-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	85	-	100	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	85	-	100	
t_{OE}	$\overline{OE}$ to Output Valid	0	45	-	50	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	30	0	50	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	30	0	50	
t_{OH}	Output Data Hold Time	5	-	10	50	

AC TEST CONDITIONS

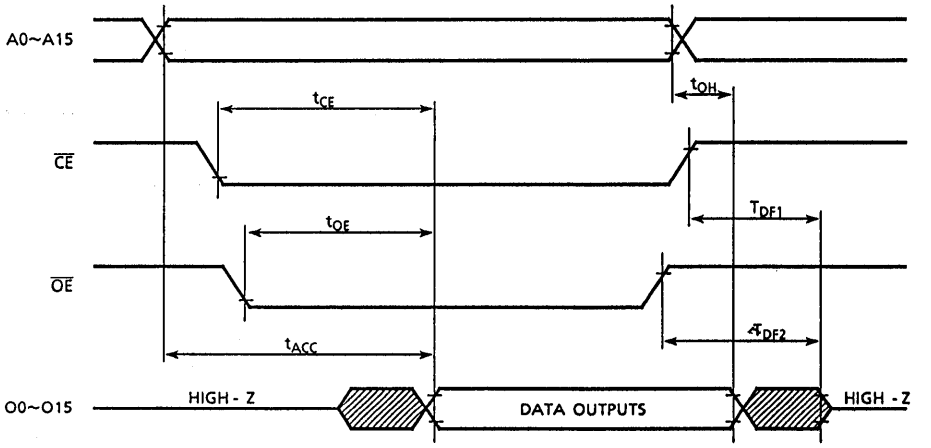
Ouput Load : 1 TTL Gate and C_L = 100pF
Input Pulse Rise and Fall Time : 10ns Max.
Input Pulse Levels : 0.45V to 2.4V
Timing Measurement Reference Level : Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	10	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS(Ta = 25 ± 5°C, VCC = 6.25V ± 0.25V, VPP = 12.75V ± 0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	–	–	± 10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	50	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	–	–	100	mA

AC PROGRAMMING CHARACTERISTICS (Ta = 25 ± 5°C, VCC = 6.25V ± 0.25V, VPP = 12.75V ± 0.25V)

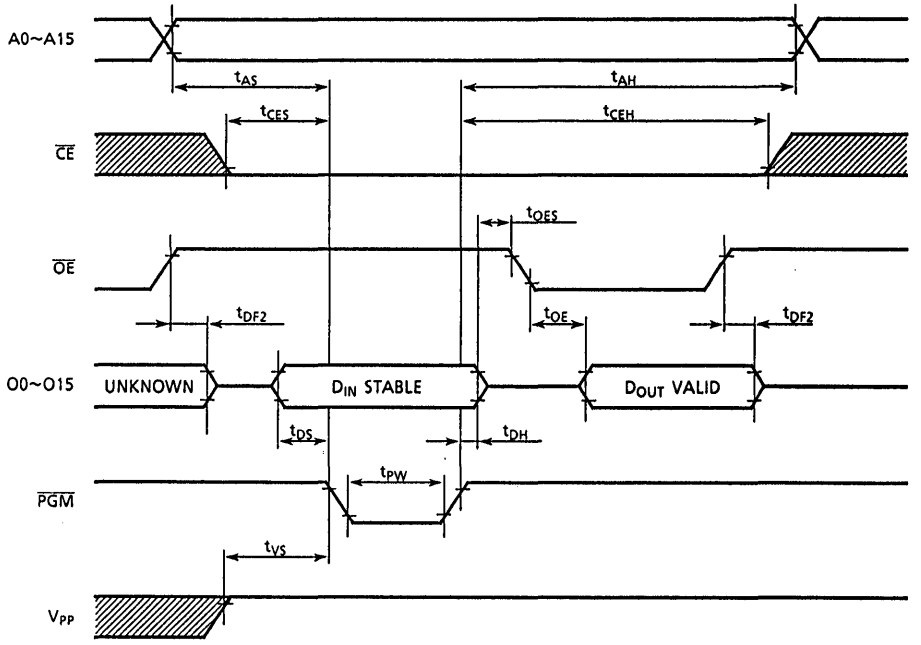
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	–	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	500	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	–	–	150	ns
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs

AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Ouptut 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC54H1024P/F's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0~D15	Power
READ OPERATION	Read	L	L	H	5V	5V	Data Out	Active
	Output Deselet	*	H	*			High Impedance	
	Standby	H	*	*				Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program	L	*	L	12.75V	6.25V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
		L	H	H				
	Program Verify	L	L	H			Data Out	

Note : H ; V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TC54H1024P/F has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming in that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54H1024P/F has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC54H1024P/F is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the ouptuts are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54H1024P/F are in the "1" state which is erased state.

Therefore the program operation is to introduce O'S data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC54H1024P/F can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC54H1024P/F from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

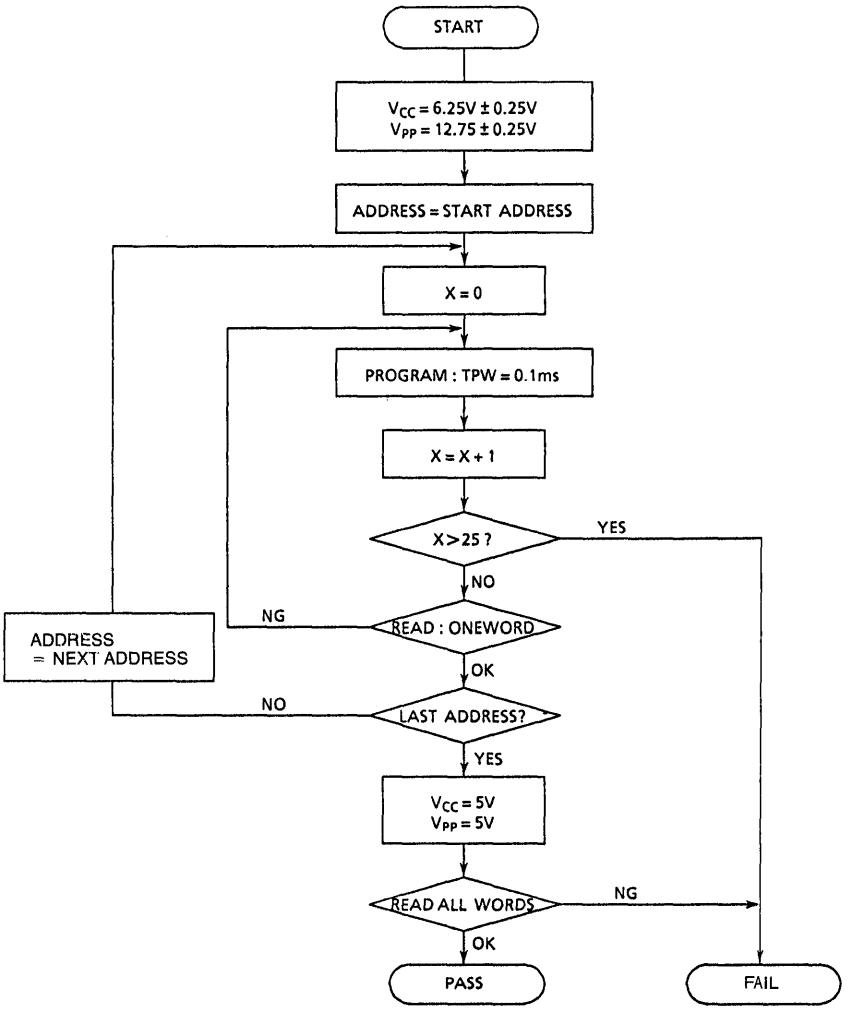
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated unitl the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54H1024P/F which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54H1024P/F by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of (O7).

The following table shows electric signature of TC54H1024P/F.

PINS / SIGNATURE	A_0	O_{15}	O_{14}	O_{13}	O_{12}	O_{11}	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	HEX DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	1	0	0	0	1	0	0	1	**89

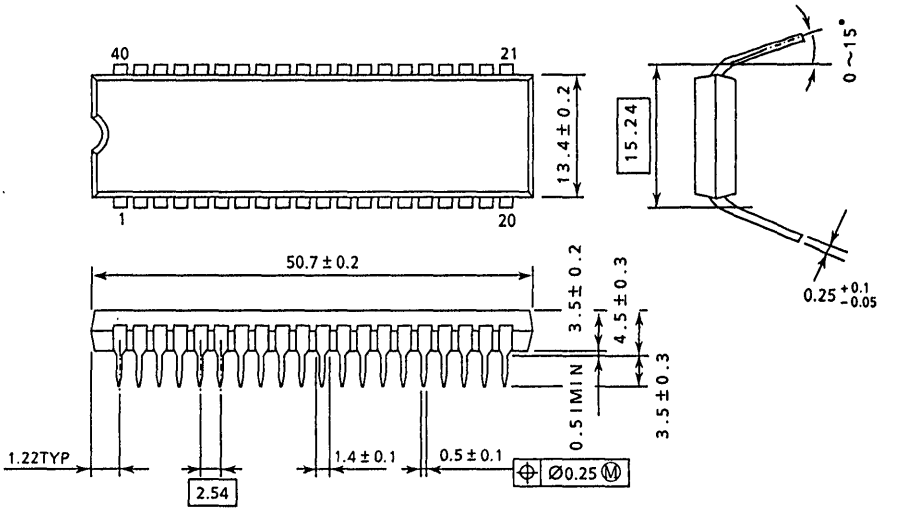
Notes: A9 = 12V ± 0.5V, $A_1 - A_8$, $A_{10} - A_{15}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$

*: Don't care

OUTLINE DRAWINGS

DIP40-P-600

Unit : mm



MROM

1M BIT (128K WORD x 8 BIT) CMOS MASK ROM
SILICON GATE CMOS

DESCRIPTION

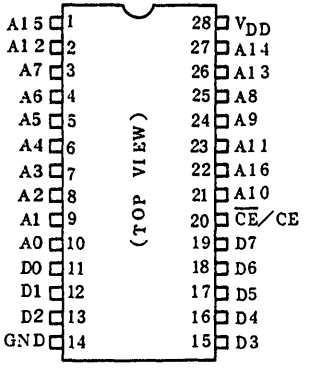
The TC531000CP/CF is a 1,048,576 bits read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, especially character generator. The TC531000CP/CF using CMOS technology is most suitable for low power applications where battery operation are required.
The TC531000CP/CF has one chip enable input CE/$\overline{CE}$, programmable for device selection.

FEATURES

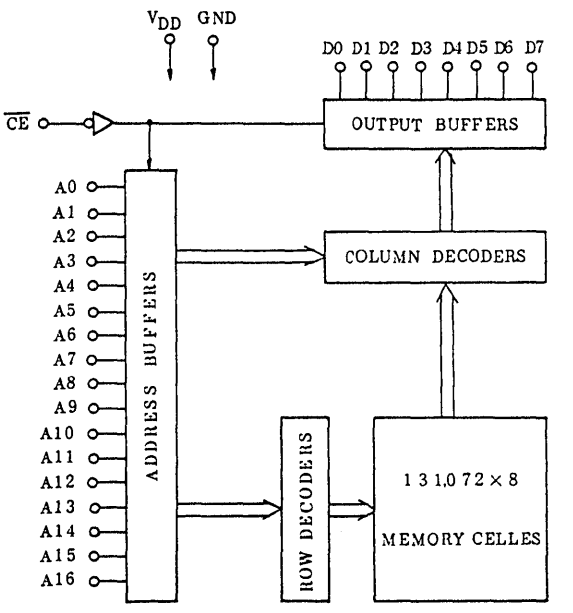
TC531000CP/CF	120ns Version	150ns Version
Access Time (max.)	120ns	150ns
Power Dissipation Operation Current (max.)	40mA	35mA
Power Dissipation Standby Current (max.)	20μA	20μA

- Single 5V Power Supply
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- Package
  Plastic DIP: TC531000CP
  Plastic FP : TC531000CF

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A16	Address Inputs
D0 ∿ D7	Data Outputs
$\overline{CE}$/CE	Chip Enable Input
VDD	Power Supply
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ∿ 7.0	V
V_{IN}	Input Voltage	-0.5 ∿ V_{DD}	
V_{OUT}	Output Voltage	0 ∿ V_{DD}	
P_D	Power Dissipation	1.0/0.6 *	W
T_{STG}	Storage Temperature	-55 ∿ 150	°C
T_{OPR}	Operating Temperature	-40 ∿ 70	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec

Note: * Plastic FP

DC OPERATING CONDITIONS (Ta=-40∿70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	
V_{IL}	Input Low Voltage	-0.3	-	0.8	

DC and OPERATING CHARACTERISTICS (Ta=-40∿70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0∿V_{DD}		-	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH}, V_{OUT}=0∿V_{DD}		-	±5.0	
I_{OH}	Output High Current	V_{OH}=2.4V		-1.0	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		3.2	-	
I_{DDS1}	Standby Current	CE=0.8V ($\overline{CE}$=2.2V)		-	2	
I_{DDS2}	Standby Current	CE=0.2V ($\overline{CE}$=V_{DD}-0.2V)		-	20	μA
I_{DDO1}	Operating Current	V_{IN}=V_{IH}/V_{IL}, I_{OUT}=0mA	t_{cycle}=120ns	-	50	mA
			t_{cycle}=150ns	-	45	
I_{DDO2}		V_{IN}=V_{DD}-0.2V/0.2V, I_{OUT}=0mA	t_{cycle}=120ns	-	40	
			t_{cycle}=150ns	-	35	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f=1MHz, Ta=25°C	-	10	pF
C_{OUT}	Output Capacitance	f=1MHz, Ta=25°C	-	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (V_{DD}=5V±10%, Ta=-40 ∿ 70°C)

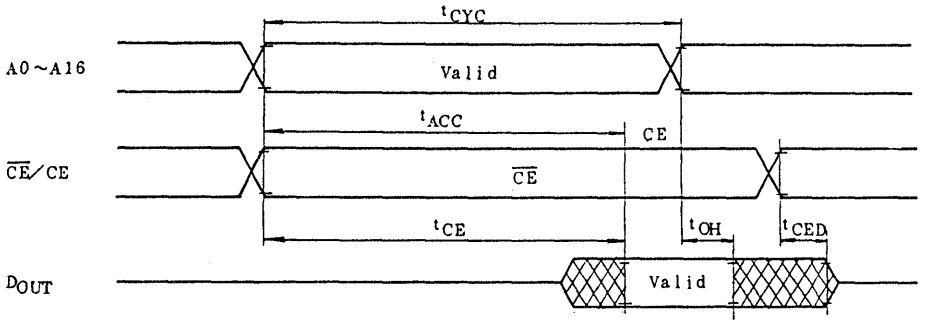
SYMBOL	PARAMETER	120ns Version		150ns Version		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{cycle}	Cycle Time	120	-	150	-	ns
t_{ACC}	Access Time	-	120	-	150	
t_{CE}	Chip Enable Access Time	-	120	-	150	
t_{CED}	Output Disable Time	-	50	-	50	
t_{OH}	Output Hold Time	5	-	5	-	

AC TEST CONDITION

- Output Load : 100pF + 1TTL
- Input Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels

  Input : 0.8V, 2.2V
  Output: 0.8V, 2.0V
- Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATING MODE

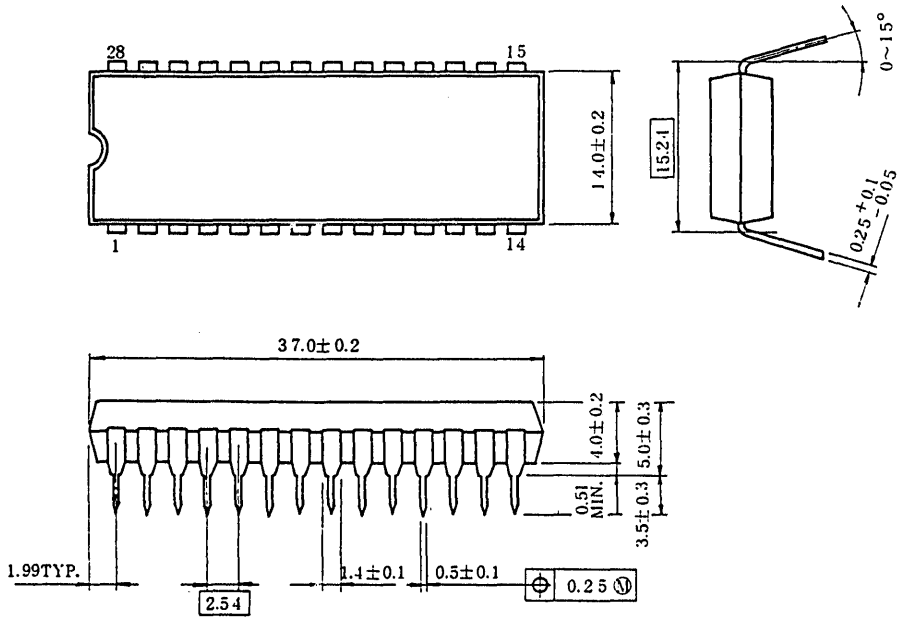
MODE	$\overline{CE}$(CE)	A0 ∿ 16	Outputs	Power
Read	L(H)	Valid	Data Out	Operating
Standby	H(L)	*	High-Z	Standby

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWINGS

Plastic DIP (DIP28-P-600)

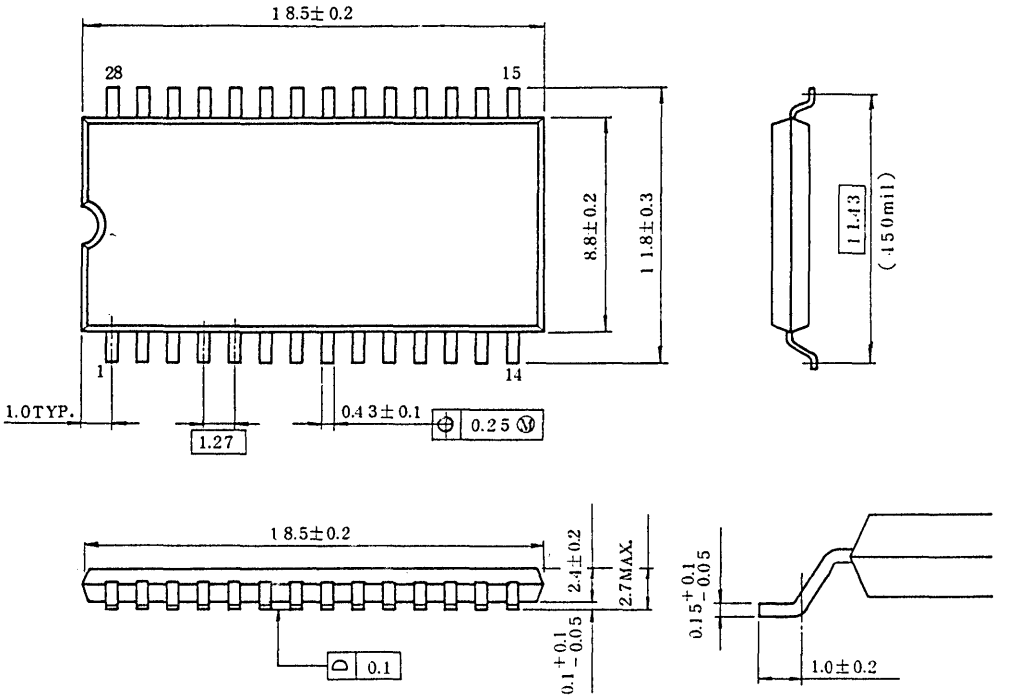
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

Plastic FP (SOP28-P-450)

unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

1M BIT (128K WORD x 8 BIT) CMOS MASK ROM

SILICON GATE CMOS

DESCRIPTION

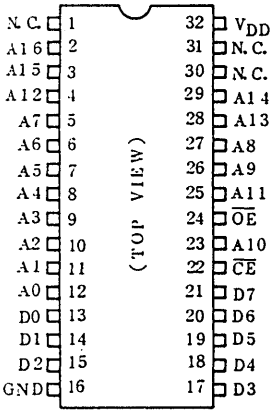
The TC531001CP/CF is a 1,048,576 bits read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, and data memory, especially character generator. The TC531001CP/CF using CMOS technology is most suitable for low power applications where battery operations are required.
The TC531001CP/CF has one chip enable input $\overline{CE}$ for device selection.

FEATURES

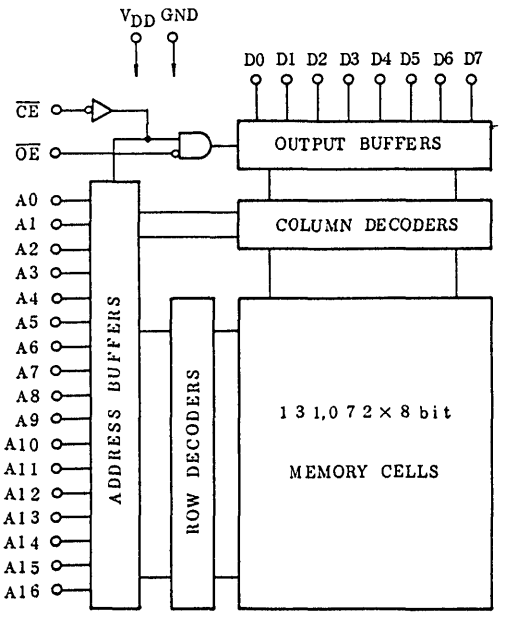
TC531001CP/CF		120ns Version	150ns Version
Access Time	(max.)	120ns	150ns
Power Dissipation Operating Current	(max.)	40mA	35mA
Power Dissipation Standby Current	(max.)	20μA	20μA

- Single 5V Power Supply
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- Fully Static Operation
- Package Plastic DIP: TC531001CP
  Plastic FP : TC531001CF

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A16	Address Inputs
D0 ∿ D7	Data Outputs
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ∿ 7.0	V
V_{IN}	Input Voltage	-0.5 ∿ V_{DD}	V
V_{OUT}	Output Voltage	0 ∿ V_{DD}	V
P_D	Power Dissipation	1.0/0.6 *	W
T_{STG}	Storage Temperature	-55 ∿ 150	°C
T_{OPR}	Operating Temperature	-40 ∿ 70	°C
T_{SOLDER}	Soldering Temperature Time	260 • 10	°C•sec

Note: * Plastic FP

DC OPERATING CONDITIONS (Ta=-40∿70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	
V_{IL}	Input Low Voltage	-0.3	-	0.8	

DC and OPERATING CHARACTERISTICS (Ta=-40∿70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	CONDITION		MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0∿V_{DD}		-	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH}, V_{OUT}=0V∿V_{DD}		-	±5.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V		-1.0	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		3.2	-	mA
I_{DDS1}	Standby Current	$\overline{CE}$=2.2V		-	2	mA
I_{DDS2}	Standby Current	$\overline{CE}$=V_{DD}-0.2V		-	200	μA
I_{DDO1}	Operating Current	V_{IN}=V_{IH}/V_{IL}	t_{cycle}=120ns	-	50	mA
		I_{OUT}=0mA	t_{cycle}=150ns	-	45	
I_{DDO2}		V_{IN}=V_{DD}-0.2V/0.2V	t_{cycle}=120ns	-	40	
		I_{OUT}=0mA	t_{cycle}=150ns	-	35	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f=1MHz, Ta=25°C	-	10	pF
C_{OUT}	Output Capacitance	f=1MHz, Ta=25°C	-	10	

Note: This parameter is periodically sampled and is not 100% tested.

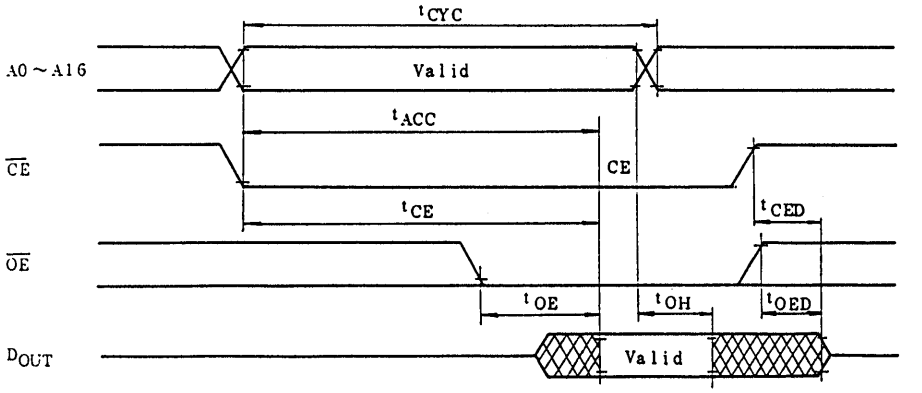
AC CHARACTERISTICS (Ta=-40∿70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	120ns Version		150ns Version		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{cycle}	Cycle Time	120	-	150	-	ns
t_{ACC}	Access Time	-	120	-	150	
t_{CE}	Chip Enable Access Time	-	120	-	150	
t_{OE}	Output Enable Access Time	-	70	-	70	
t_{CED}	Output Disable Time from $\overline{CE}$	-	50	-	50	
t_{OED}	Output Disable Time from $\overline{OE}$	-	50	-	50	
t_{OH}	Output Hold Time	5	-	5	-	

AC TEST CONDITIONS

- Output Load : 100pF + 1TTL
- Input Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels Input: 0.8V, 2.2V
  Output: 0.8V, 2.0V
- Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATION MODE

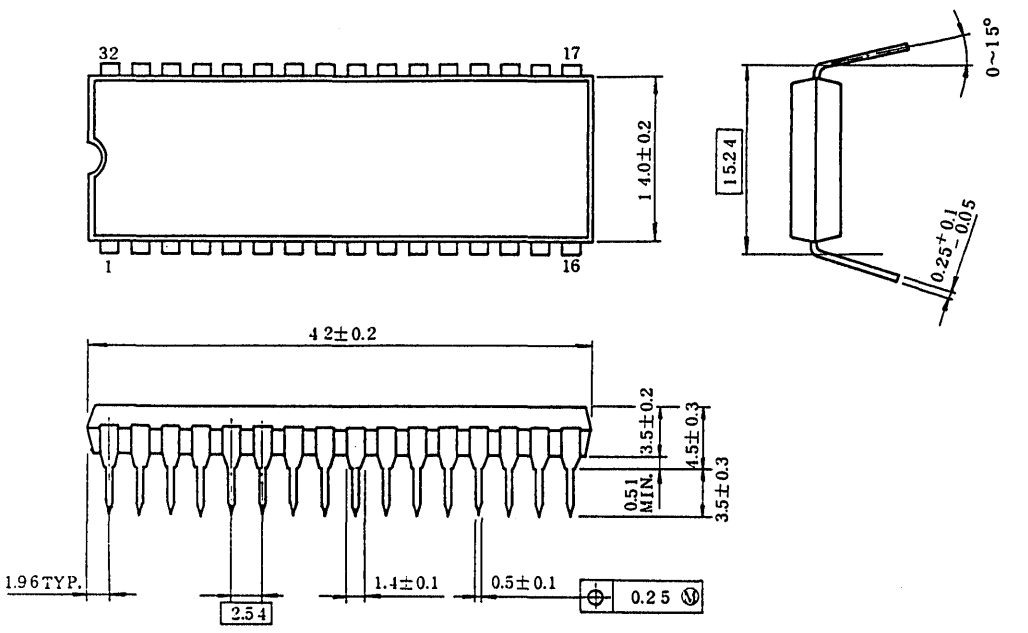
MODE	$\overline{CE}$	$\overline{OE}$	A0 ∿ 16	Outputs	Power
Read	L	L	Valid	Data Out	Operating
Standby	H	*	*	High-Z	Standby
Output Deselect	L	H	*	High-Z	Operating

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWINGS

Plastic DIP (DIP32-P-600)

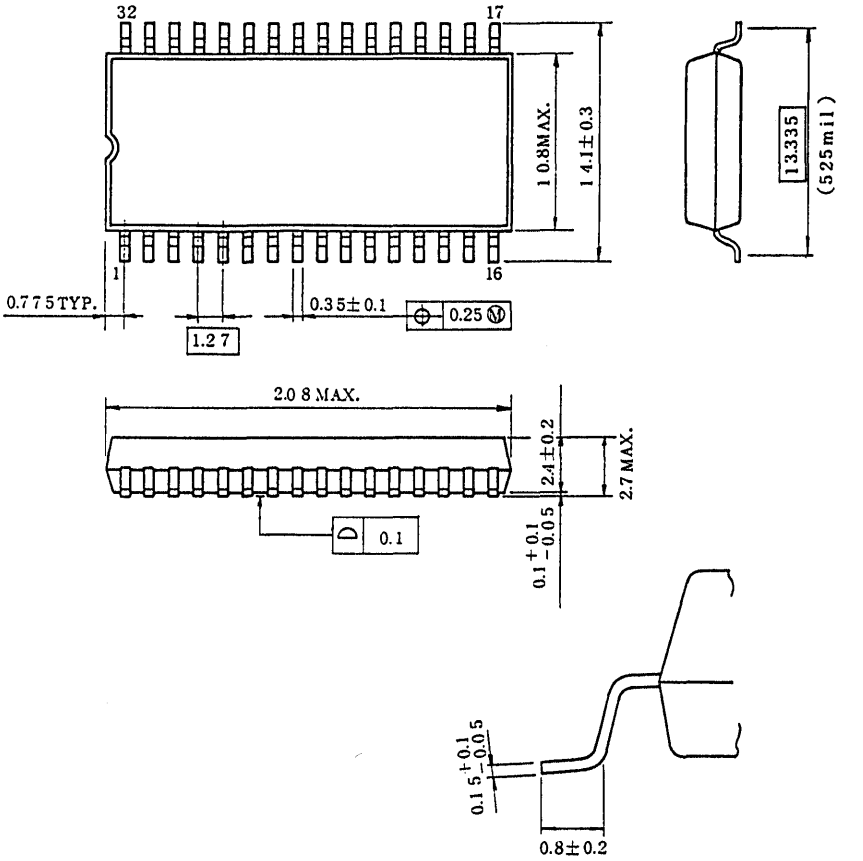
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

Plastic FP (SOP32-P-525)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

1M BIT (65,536 WORD × 16 BIT) CMOS MASK ROM

DESCRIPTION

The TC531024P/F is a 1,048,576 bits read only memory organized as 65,536 words by 16 bits.

The TC531024P/F is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 120ns/150ns, an operation current of 40mA at 8.3MHz and a standby current of 20μA.

The TC531024P/F is packaged in a standard 600mil 40pin DIP, or 525mil 40pin SOP.

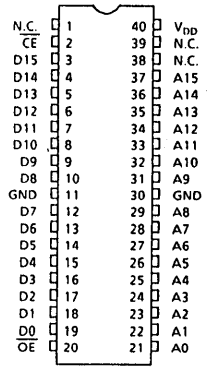
FEATURES

TC531024P/F	-12	-15
Power Supply	5V ± 5%	5V ± 10%
Access Time (Max.)	120ns	150ns
Power Dissipation : Operating Current (Max.)	40mA	35mA
Power Dissipation : Standby Current (Max.)	20μA	20μA

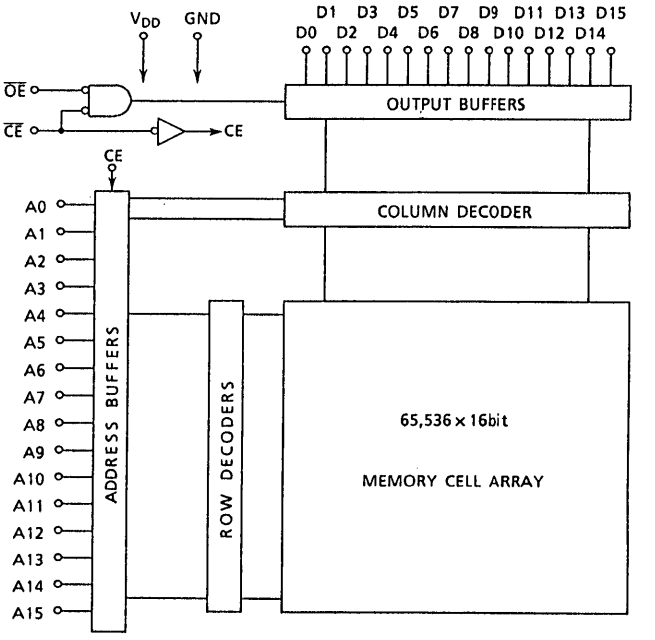
- Single 5V Power Supply
- Fully Static Operation
- All Input and Output : TTL Compatible
- Three State Output
- 40pin 600mil width Plastic DIP
- 40pin 525mil width Plastic SOP

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0~A15	Address inputs
D0~D15	Data Outputs
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature - Time	260 · 10	°C · sec

Note : * Plastic FP.

D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	0.8	V

D.C. OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0V \leq V_{IN} \leq V_{DD}$		−	± 1.0	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{DD}$		−	± 5.0	
I_{OH}	Output High Current	V_{OH} = 2.4V		−1.0	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		3.2	−	
I_{DDS1}	Standby Current	$\overline{CE}$ = 2.2V		−	2.0	
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V		−	20	μA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} / V_{IL}, I_{OUT} = 0mA	t_{cycle} = 120ns	−	50	mA
			t_{cycle} = 150ns	−	45	
I_{DDO2}		$\overline{CE}$ = 0.2V, V_{IN} = V_{DD} − 0.2V / 0.2V, I_{OUT} = 0mA	t_{cycle} = 120ns	−	40	
			t_{cycle} = 150ns	−	35	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	−	10	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	−	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

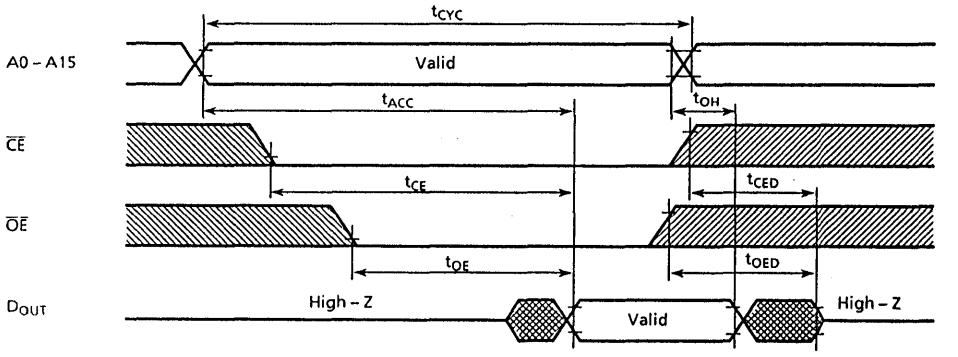
A.C. CHARACTERISTICS (Ta = 0°C~70°C)

SYMBOL	PARAMETER	V_{DD} = 5V ± 5%		V_{DD} = 5V ± 10%		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Access Time	–	120	–	150	ns
t_{CE}	Chip Enable Access Time	–	120	–	150	ns
t_{OE}	Output Enable Access Time	–	70	–	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	0	60	0	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	0	60	0	60	ns
t_{OH}	Output Hold Time	5	–	5	–	ns
t_{CYC}	Cycle Time	120	–	150	–	ns

A.C. TEST CONDITIONS

Output Load		: 100pF + 1TTL
Input Levels		: 0.6V / 2.4V
Timing Measurement Reference Levels	Input	: 0.8V / 2.2V
	Output	: 0.8V / 2.0V
Input Rise and Fall Time (10%~90%)		: 5ns

TIMING WAVEFORMS



OPERATION MODE

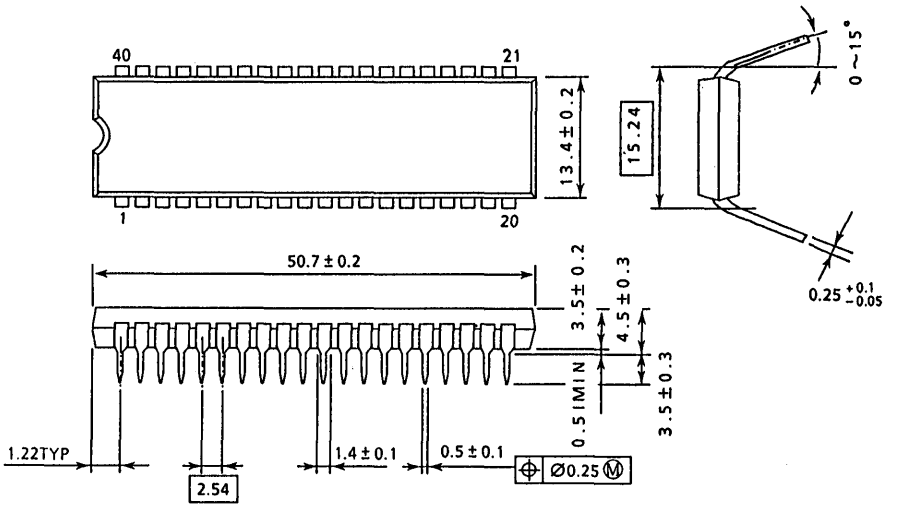
MODE	$\overline{CE}$	$\overline{OE}$	A0~A15	Outputs	Power
Read	L	L	Valid	Data Out	Operating
Standby	H	*	*	High-Z	Standby
Output Deselect	L	H	*	High-Z	Operating

H : VIH L : VIL * : VIH or VIL

OUTLINE DRAWINGS

Plastic DIP (DIP40-P-600)

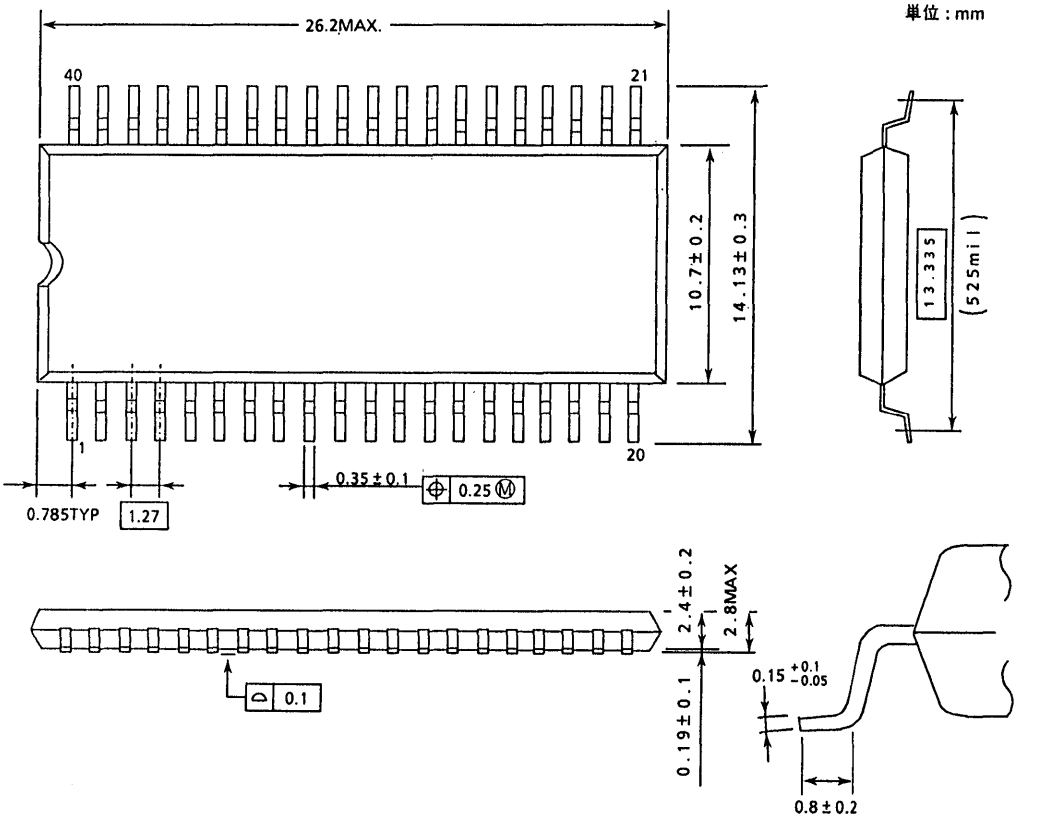
単位 : mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic FP (SOP40-P-525)



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

4M BIT (512K WORD × 8 BIT) CMOS MASK ROM

DESCRIPTION

The TC534000P/F is a 4,194,304 bits read only memory organized as 524,288words by 8bits.

The TC534000P/F is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 200ns/250ns, an operation current of 30mA at 5MHz and a standby current of 20μA.

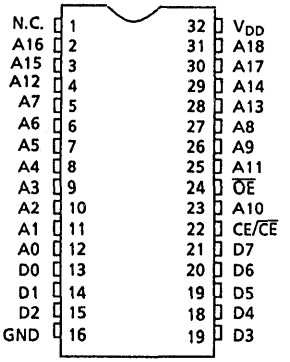
The TC534000P/F has one programmable chip enable input CE/$\overline{CE}$ for device selection.

The TC534000P/F is packaged in a standard 600mil 32pin DIP or 525mil 32pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 250ns (Max.) V_{DD}=5V±10%
  : 200ns (Max.) V_{DD}=5V±5%
- Power Dissipation
  Operating Current : 30mA (Max.)
  Standby Current : 20μA (Max.)
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- Package Plastic DIP : TC534000P
  Plastic FP : TC534000F

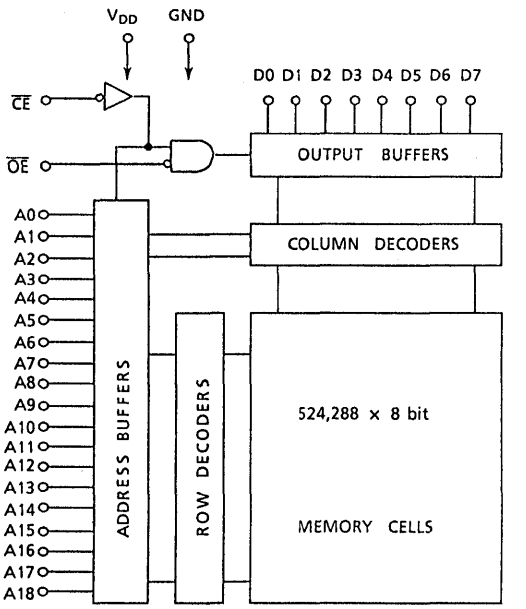
PIN CONNECTION



PIN NAMES

A0~A18	Address inputs
D0~D7	Data Outputs
$\overline{OE}$	Output Enable Input
CE/$\overline{CE}$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	−40~85	°C
T_{SOLDER}	Soldering Temperature - Time	260 · 10	°C · sec

Note : * Plastic FP.

D.C. OPERATING CONDITIONS (Ta = −40~85°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS (V_{DD} = 5V ± 10% , Ta = −40~85°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	−	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} , V_{OUT} = 0~V_{DD}	−	± 5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	−	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	−	2	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} and V_{IN} = 0V (V_{DD})	−	20	μA
I_{DDO1}	Operating Current	V_{IN} = V_{IH}/V_{IL} , t_{cycle} = 250ns	−	40	mA
I_{DDO2}		V_{IN} = V_{DD}/0V , t_{cycle} = 250ns	−	30	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz , Ta = 25°C	−	8	pF
C_{OUT}	Output Capacitance	f = 1MHz , Ta = 25°C	−	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

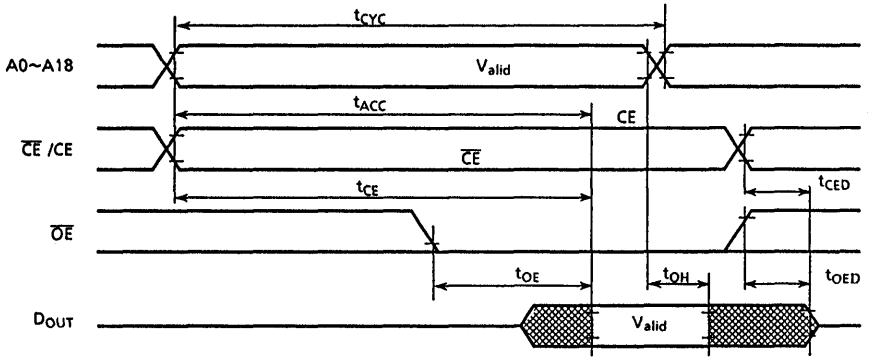
A.C. CHARACTERISTICS

SYMBOL	PARAMETER	Ta = −40~85°C, V_{DD} = 5V ± 10%		Ta = −40~70°C, V_{DD} = 5V ± 5%		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Access Time	−	250	−	200	ns
t_{CE}	Chip Enable Access Time	−	250	−	200	ns
t_{OE}	Output Enable Access Time	−	70	−	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	0	70	0	70	ns
t_{OED}	Output Disable Time from $\overline{OE}$	0	70	0	70	ns
t_{OH}	Output Hold Time	10	−	10	−	ns
t_{CYC}	Cycle Time	250	−	200	−	ns

A.C. TEST CONDITIONS

Output Load		: 100pF + 1TTL
Input Levels		: 0.6V , 2.4V
Timing Measurement Reference Levels	Input	: 0.8V , 2.2V
	Output	: 0.8V , 2.0V
Input Rise and Fall Time		: 5ns

TIMING WAVEFORMS



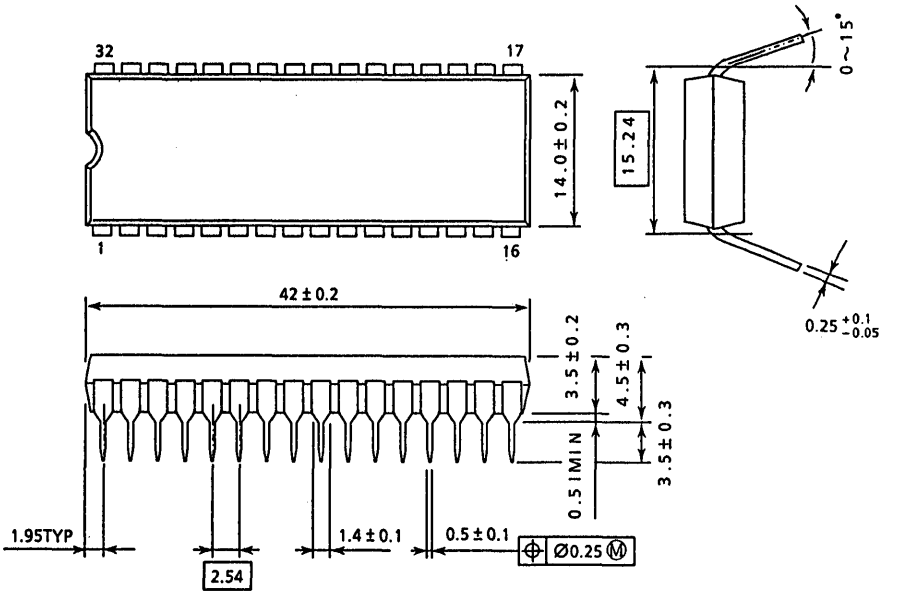
OPERATION MODE

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A0~A18	Outputs	Power
Read	L(H)	L	Valid	Data Out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H : VIH L : VIL * : VIH or VIL

OUTLINE DRAWINGS
Plastic DIP (DIP32 - P - 600)

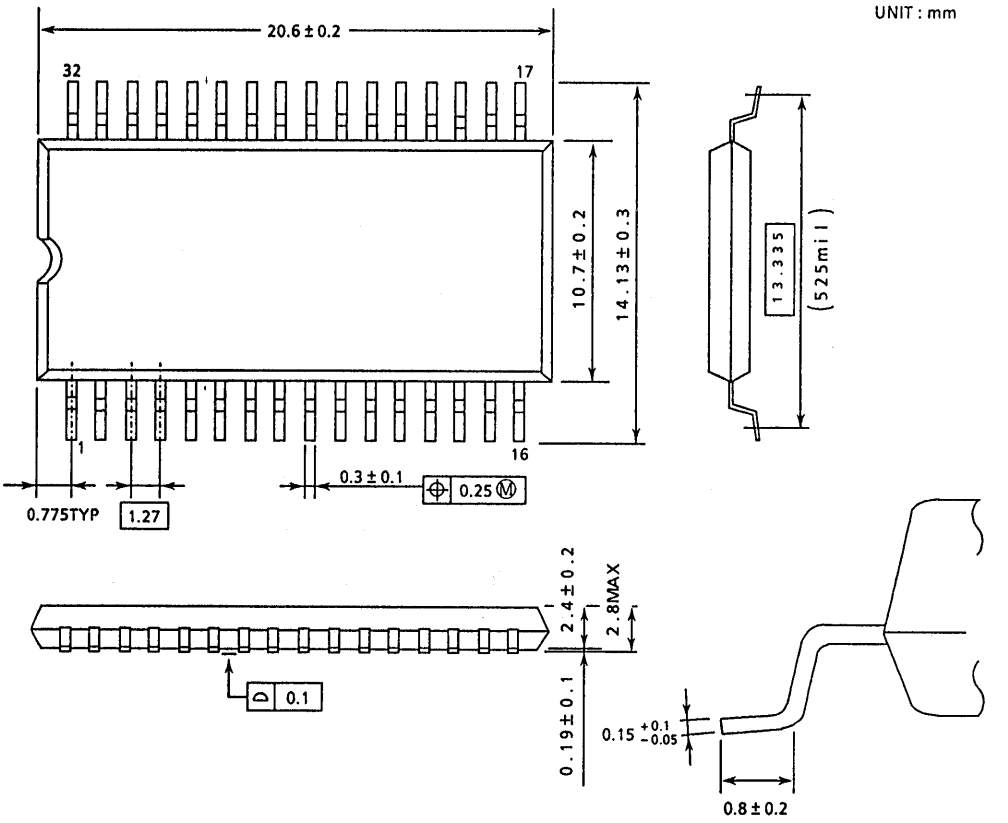
UNIT : mm



Note : Package width and length do not include mold protrusion , allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS
Plastic FP (SOP32-P-525)

UNIT : mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

4M BIT (256K WORD × 16 BIT/512K WORD × 8BIT) CMOS MASK ROM

PRELIMINARY

DESCRIPTION

The TC534200P/F is a 4,194,304 bits read only memory organized as 262,144 words by 16 bits when $\overline{BYTE}$ is logical high, and is organized as 524,288 words by 8 bits when $\overline{BYTE}$ is logical low.

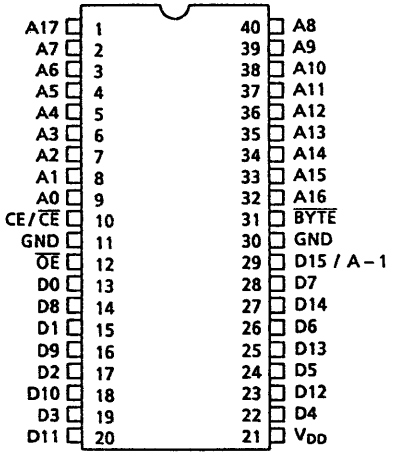
The TC534200P/F is most suitable for in program memory of 16 bits microprocessor, data memory, and character generator. The TC534200P/F has a programmable chip enable input CE/$\overline{CE}$ for device selection.

The TC534200P/F is packaged in a standard 600mil 40pin DIP, or 525mil 40 pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.)
- Power Dissipation
  - Operating Current : 50mA (Max.)
  - Standby Current : 20μA (Max.)
- Fully Static Operation
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Programmable Chip Enable
- 40pin 600mil width Plastic DIP
- 40pin 525mil width Plastic SOP

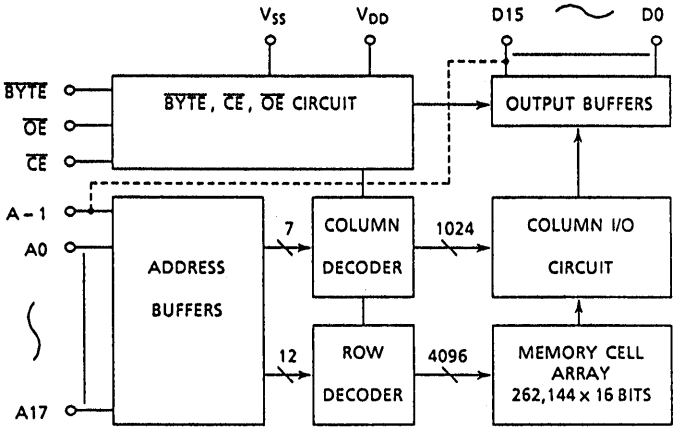
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A17	Address inputs
D0~D14	Data Outputs
CE/$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A-1	Data Output Address Input
$\overline{BYTE}$	Word, Byte selection Input
V_{DD}	Power Supply
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	$\overline{BYTE}$	D0 – D7	D8 – D14	D15/A – 1
Read (16 Bit)	L (H)	L	H	Data Out		
Read (8 Bit)	L (H)	L	L	Data Out (Lower 8bit)	High Impedance	L
Read (8 Bit)	L (H)	L	L	Data Out (Upper 8bit)	High Impedance	H
Output Deselect	L (H)	H	*	High Impedance		
Standby	H (L)	*	*	High Impedance		

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	– 0.5~7.0	V
V_{IN}	Input Voltage	– 0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	– 55~150	°C
T_{OPR}	Operating Temperature	– 40~85	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

* SOP

D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	– 0.3	–	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	± 1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0 \sim V_{DD}$	–	± 5.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	– 1.0	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	2.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	–	2	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$	–	20	μA
I_{DDO1}	Operating Current	$V_{IN} = V_{IH} / V_{IL}$, $t_{cycle} = 150ns$	–	60	mA
I_{DDO2}		$V_{IN} = V_{DD} - 0.2V / 0.2V$, $t_{cycle} = 150ns$	–	50	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz , Ta = 25°C	–	10	pF
C_{OUT}	Output Capacitance	f = 1MHz , Ta = 25°C	–	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

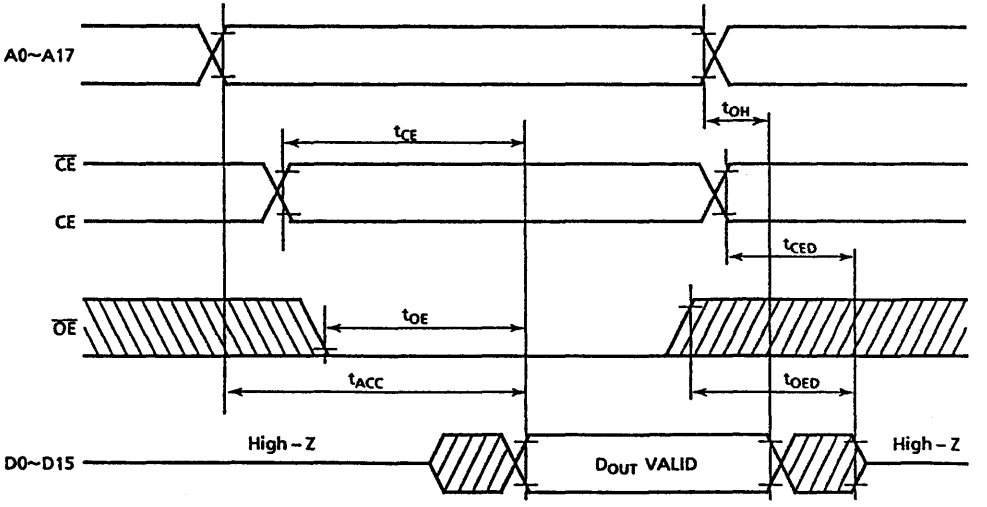
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	ns
t_{CE}	Chip Enable Access Time	–	150	ns
t_{BT}	$\overline{BYTE}$ Access Time	–	150	ns
t_{OE}	Output Enable Access Time	–	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	–	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	–	60	ns
t_{BTD}	Output Disable Time from $\overline{BYTE}$	–	60	ns
t_{OH}	Output Hold Time	5	–	ns

A.C. TEST CONDITIONS

Output Load		: 100pF + 1TTL
Input Levels		: 0.6V , 2.4V
Timing Measurement Reference Levels	Input	: 0.8V , 2.2V
	Output	: 0.8V , 2.0V
Input Rise and Fall Time		: 5ns

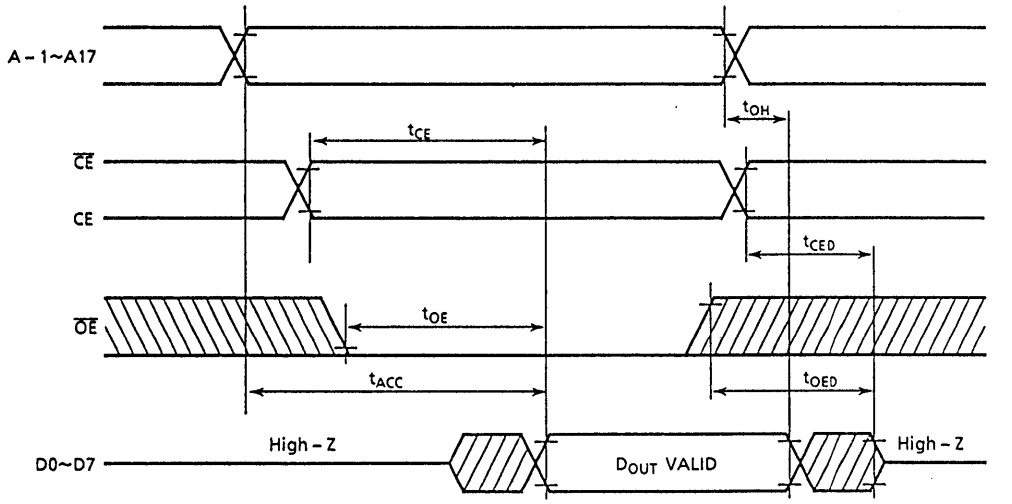
TIMING WAVEFORMS

WORD – WIDE READ MODE



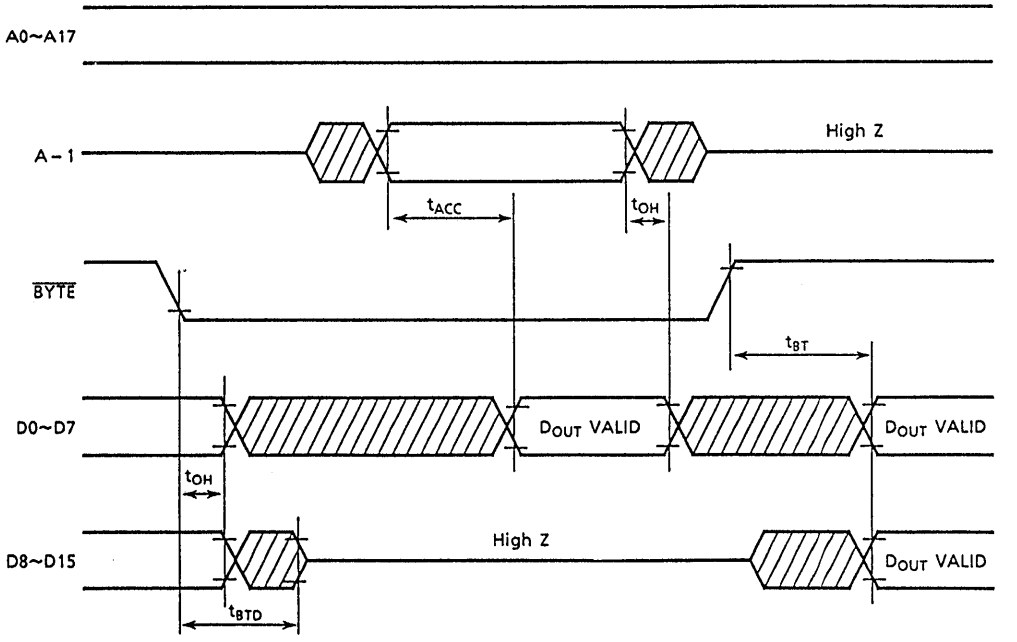
Note: $\overline{BYTE}$ = V_{IH}

BYTE – WIDE READ MODE



Note: $\overline{BYTE}$ = V_{IL}

$\overline{BYTE}$ TRANSITION



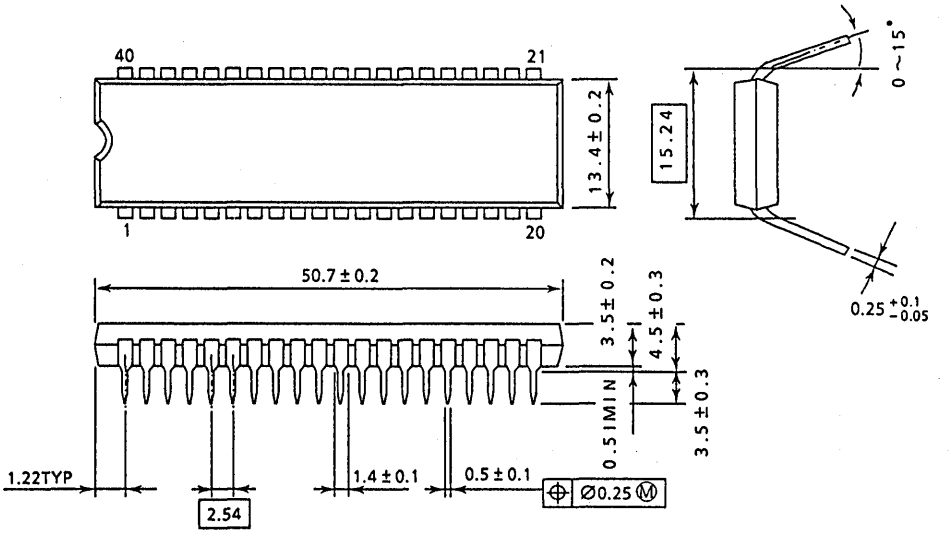
Note: $\overline{CE}$, $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS

- Plastic DIP

DIP40-P-600

Unit : mm

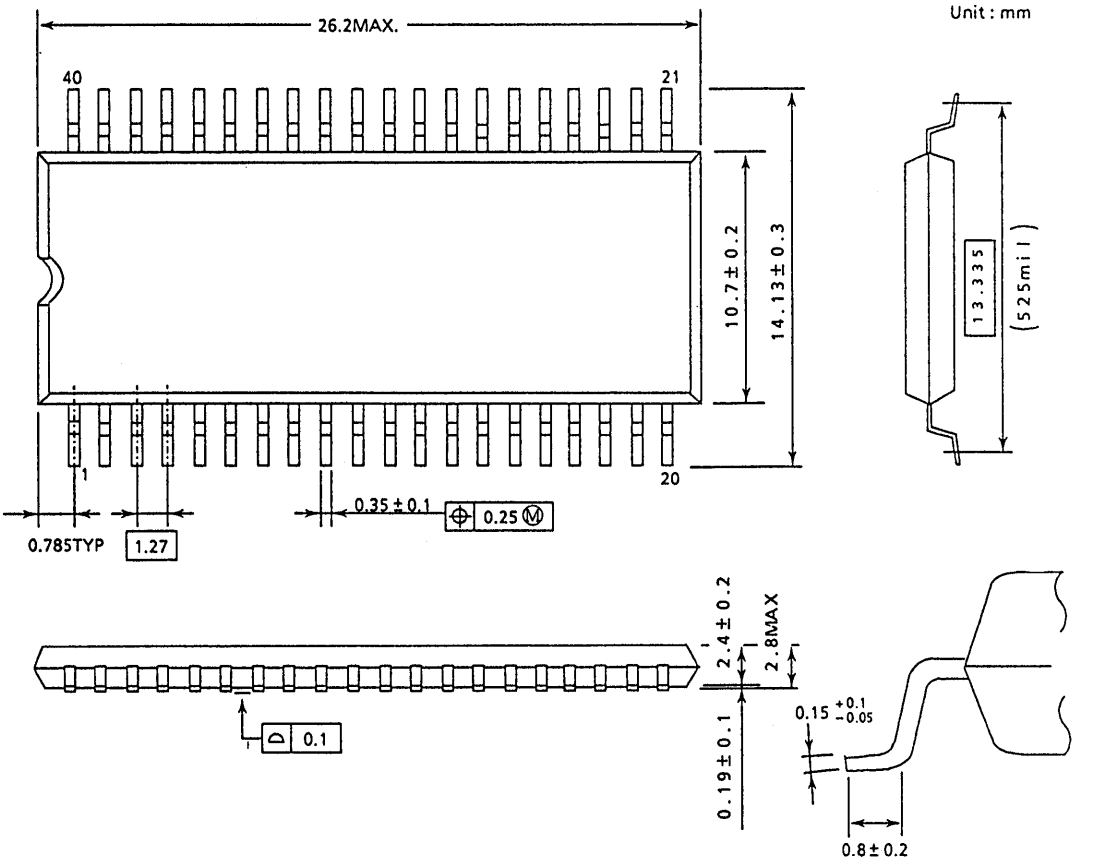


Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

- Plastic SOP

  SOP40-P-525



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

8M BIT (512K WORD × 16 BIT/1M WORD × 8BIT) CMOS MASK ROM

PRELIMINARY

DESCRIPTION

The TC538200P/F is a 8,388,608 bits read only memory organized as 524,288 words by 16 bits when $\overline{BYTE}$ is logical high, and is organized as 1,048,576 words by 8 bits when $\overline{BYTE}$ is logical low.

The TC538200P/F is most suitable for the program memory, data memory, and character generator.

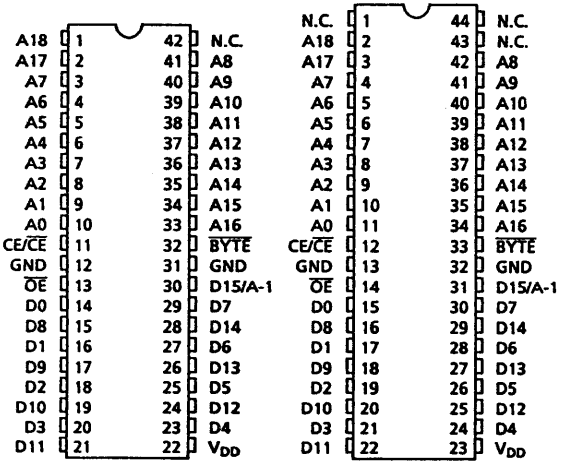
The TC538200P/F has a programmable chip enable input CE/$\overline{CE}$ for device selection.

The TC538200P/F is packaged in a standard 600mil 42pin DIP, or 600mil 44 pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 200ns (Max.)
- Power Dissipation
  - Operating Current : 50mA (Max.)
  - Standby Current : 100μA (Max.)
- Fully Static Operation
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Programmable Chip Enable
- 42pin 600mil width Plastic DIP
- 44pin 600mil width Plastic SOP

PIN CONNECTION (TOP VIEW)

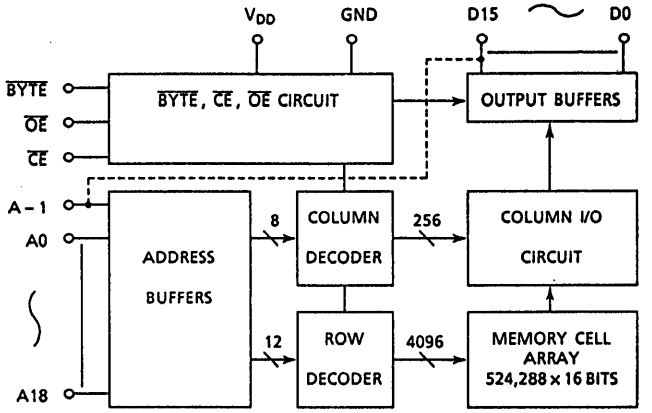


TC538200P TC538200F

PIN NAMES

A0~A18	Address inputs
D0~D14	Data Outputs
CE/$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A-1	Data Output/Address Input
$\overline{BYTE}$	Word, Byte selection Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	$\overline{BYTE}$	D0 – D7	D8 – D14	D15/A – 1	Power
Read (16 Bit)	L (H)	L	H	Data Out			Active
Read (8 Bit)	L (H)	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L (H)	L	L	Data Out (Upper 8bit)	High Impedance	H	Active
Output Deselect	L (H)	H	*	High Impedance			Active
Standby	H (L)	*	*	High Impedance			Standby

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	– 0.5~7.0	V
V_{IN}	Input Voltage	– 0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	– 55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

* SOP

D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	- 0.3	-	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	± 1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0 \sim V_{DD}$	-	± 5.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	- 1.0	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	2.0	-	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	-	2	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$	-	100	μA
I_{DDO1}	Operating Current	$V_{IN} = V_{IH} / V_{IL}$, $t_{cycle} = 200ns$	-	60	mA
I_{DDO2}		$V_{IN} = V_{DD} - 0.2V / 0.2V$, $t_{cycle} = 200ns$	-	50	mA

CAPACITANCE f = 1MHz , Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	-	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	-	12	pF

Note : This Parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta = 0 \sim 70°C, V_{DD} = 5V \pm 10\%$)

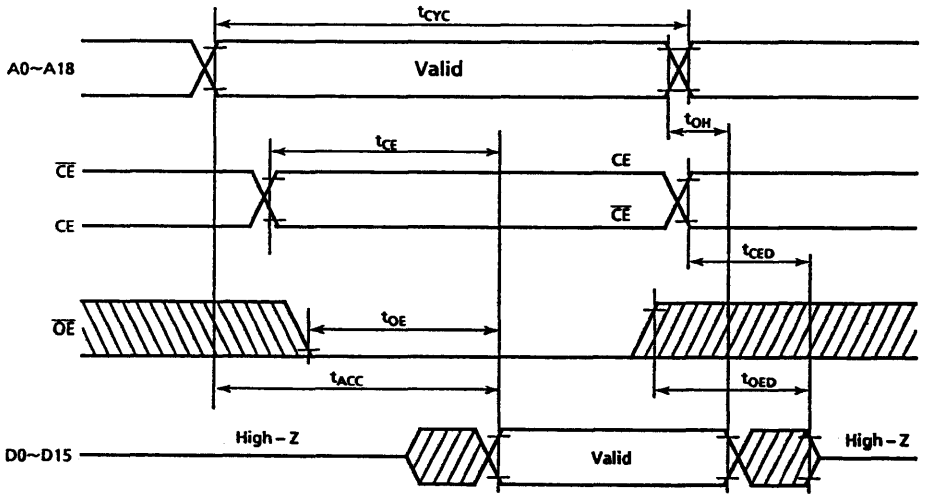
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	200	–	ns
t_{ACC}	Address Access Time	–	200	ns
t_{CE}	Chip Enable Access Time	–	200	ns
t_{BT}	$\overline{BYTE}$ Access Time	–	200	ns
t_{OE}	Output Enable Access Time	–	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	–	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	–	60	ns
t_{BTD}	Output Disable Time from $\overline{BYTE}$	–	60	ns
t_{OH}	Output Hold Time	5	–	ns

A.C. TEST CONDITIONS

Output Load		: 100pF + 1TTL
Input Levels		: 0.6V , 2.4V
Timing Measurement Reference Levels	Input	: 0.8V , 2.2V
	Output	: 0.8V , 2.0V
Input Rise and Fall Time		: 5ns

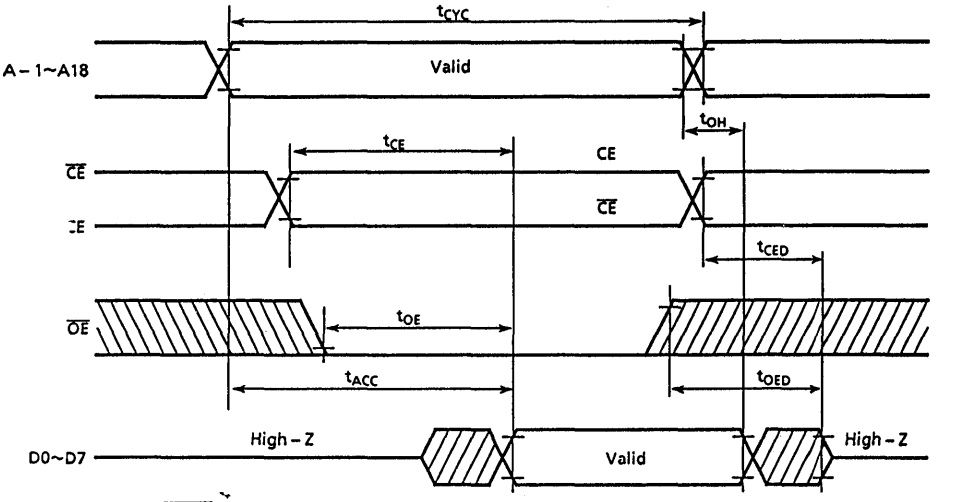
TIMING WAVEFORMS

WORD – WIDE READ MODE



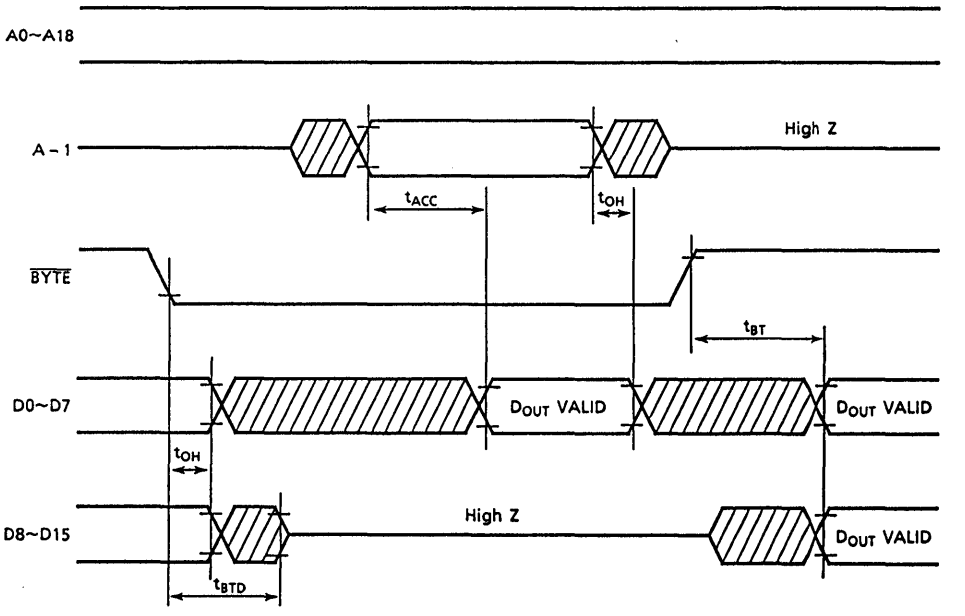
Note: $\overline{BYTE} = V_{IH}$

BYTE-WIDE READ MODE



Note: $\overline{BYTE}$ = V_{IL}

$\overline{BYTE}$ TRANSITION



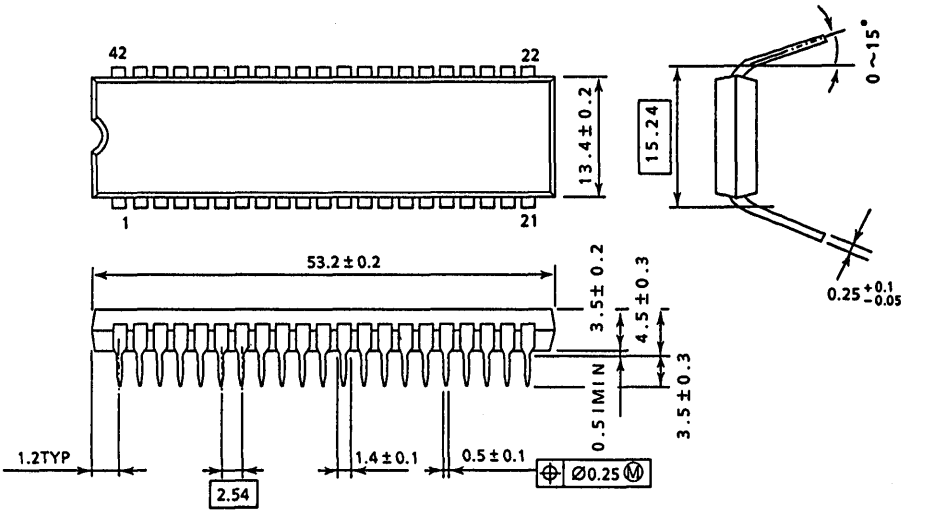
Note: CE($\overline{CE}$) = V_{IH}(V_{IL}), $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS

- Plastic DIP

DIP42-P-600

Unit : mm

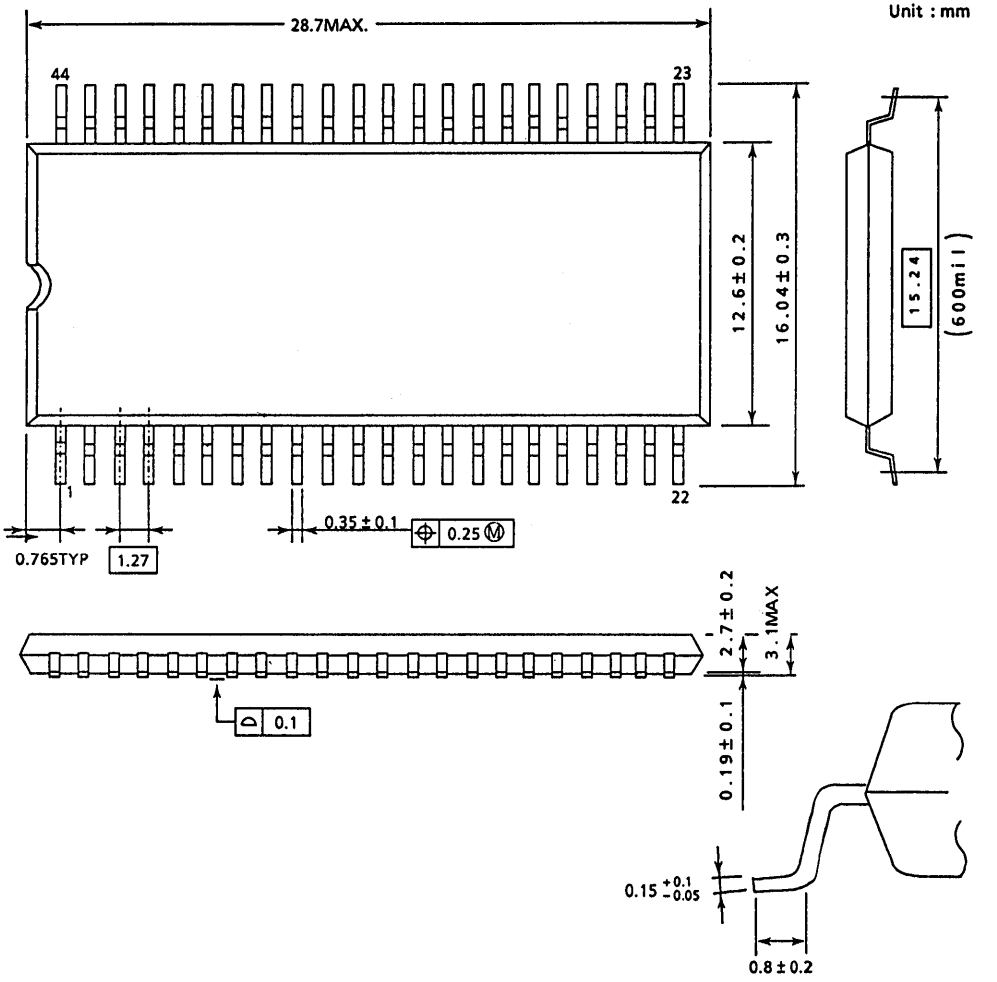


Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

- Plastic SOP

SOP44-P-600



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

16M BIT (1M WORD × 16 BIT / 2M WORD × 8BIT) CMOS MASK ROM

PRELIMINARY

DESCRIPTION

The TC5316200P / F is a 16,777,216 bits read only memory organized as 1,048,576 words by 16 bits when $\overline{BYTE}$ is logical high, and is organized as 2,097,152 words by 8 bits when $\overline{BYTE}$ is logical low.

The TC5316200P/F is most suitable for the program memory. data memory, and character generator.

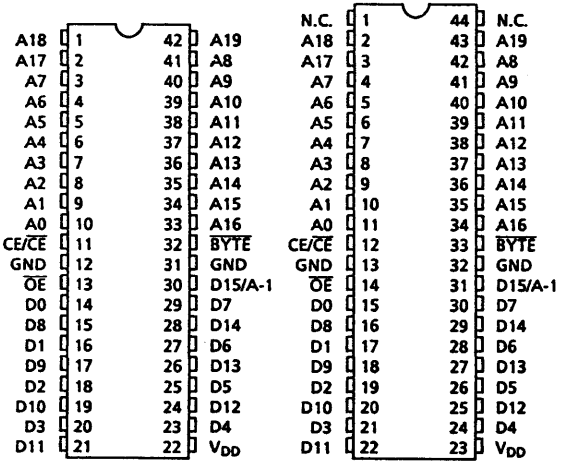
The TC5316200P/F has a programmable chip enable input CE/$\overline{CE}$ for device selection.

The TC5316200P / F is packaged in a standard 600mil 42pin DIP, or 600mil 44 pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 200ns (Max.)
- Power Dissipation
  - Operating Current : 50mA (Max.)
  - Standby Current : 100μA (Max.)
- Fully Static Operation
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Programmable Chip Enable
- 42pin 600mil width Plastic DIP
- 44pin 600mil width Plastic SOP

PIN CONNECTION (TOP VIEW)

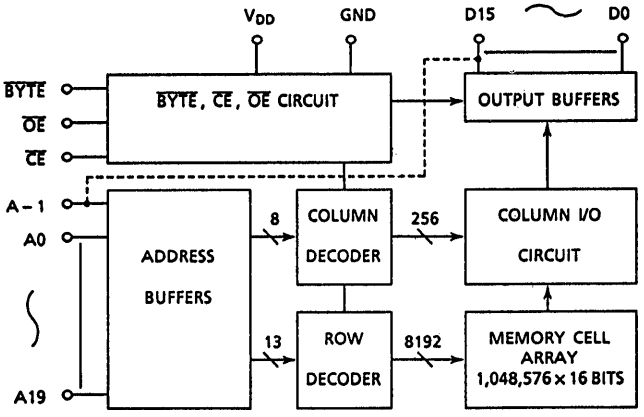


TC5316200P TC5316200F

PIN NAMES

A0~A19	Address inputs
D0~D14	Data Outputs
CE / $\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15 / A-1	Data Output/Address Input
$\overline{BYTE}$	Word, Byte selection Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	$\overline{BYTE}$	D0 - D7	D8 - D14	D15/A-1	Power
Read (16 Bit)	L (H)	L	H	Data Out			Active
Read (8 Bit)	L (H)	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L (H)	L	L	Data Out (Upper 8bit)	High Impedance	H	Active
Output Deselect	L (H)	H	*	High Impedance			Active
Standby	H (L)	*	*	High Impedance			Standby

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	-55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

* SOP

D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	-	±1.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0~V_{DD}	-	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-1.0	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	-	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	-	2	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V	-	100	μA
I_{DDO1}	Operating Current	V_{IN} = V_{IH} / V_{IL} , t_{cycle} = 200ns	-	60	mA
I_{DDO2}		V_{IN} = V_{DD} - 0.2V / 0.2V, t_{cycle} = 200ns	-	50	mA

CAPACITANCE f = 1MHz , Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	-	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	12	pF

Note : This Parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

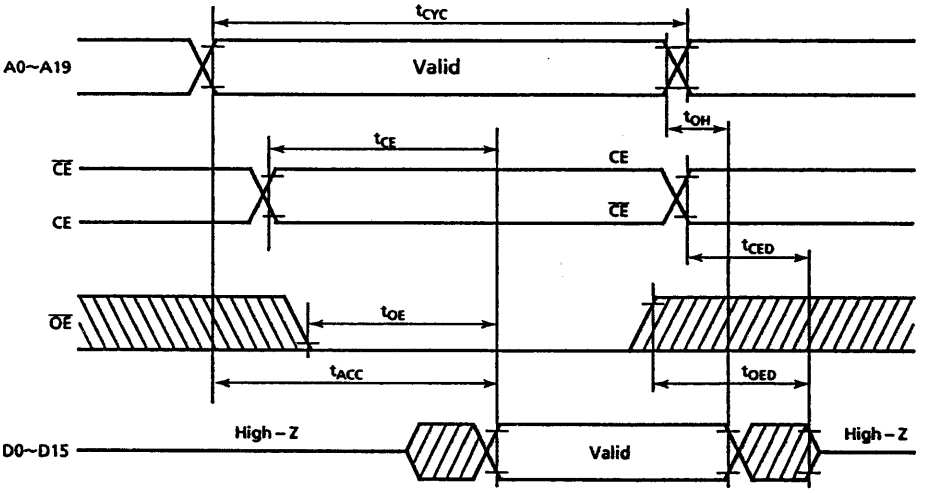
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	200	–	ns
t_{ACC}	Address Access Time	–	200	ns
t_{CE}	Chip Enable Access Time	–	200	ns
t_{BT}	$\overline{BYTE}$ Access Time	–	200	ns
t_{OE}	Output Enable Access Time	–	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	–	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	–	60	ns
t_{BTD}	Output Disable Time from $\overline{BYTE}$	–	60	ns
t_{OH}	Output Hold Time	5	–	ns

A.C. TEST CONDITIONS

Output Load		: 100pF + 1TTL
Input Levels		: 0.6V , 2.4V
Timing Measurement Reference Levels	Input	: 0.8V , 2.2V
	Output	: 0.8V , 2.0V
Input Rise and Fall Time		: 5ns

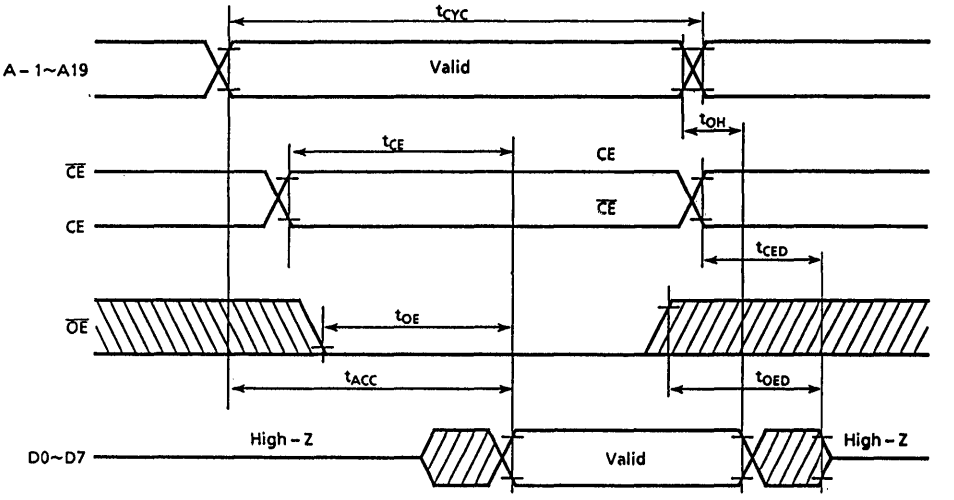
TIMING WAVEFORMS

WORD – WIDE READ MODE



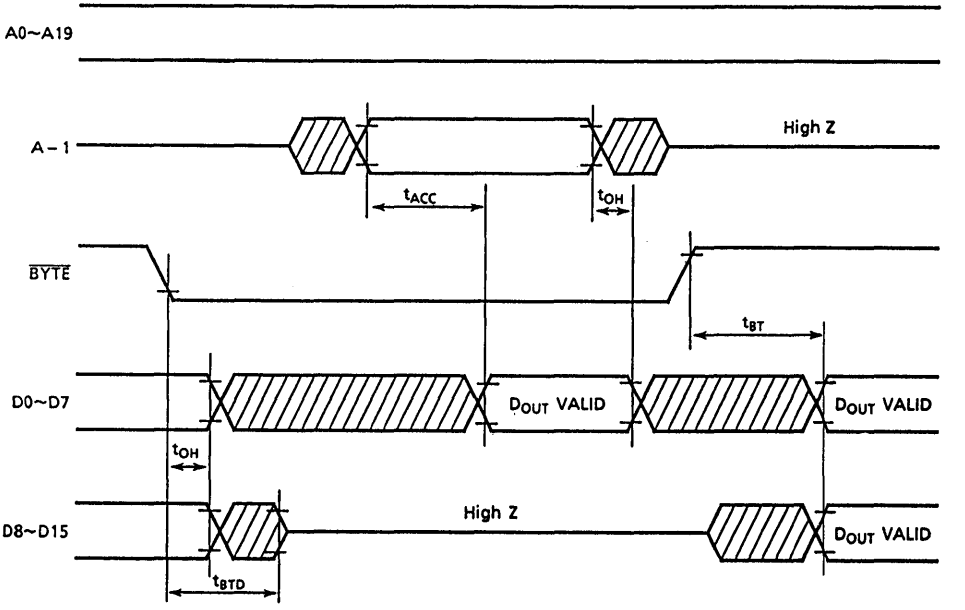
Note: $\overline{BYTE}$ = V_{IH}

BYTE-WIDE READ MODE



Note: $\overline{BYTE}$ = V_{IL}

$\overline{BYTE}$ TRANSITION



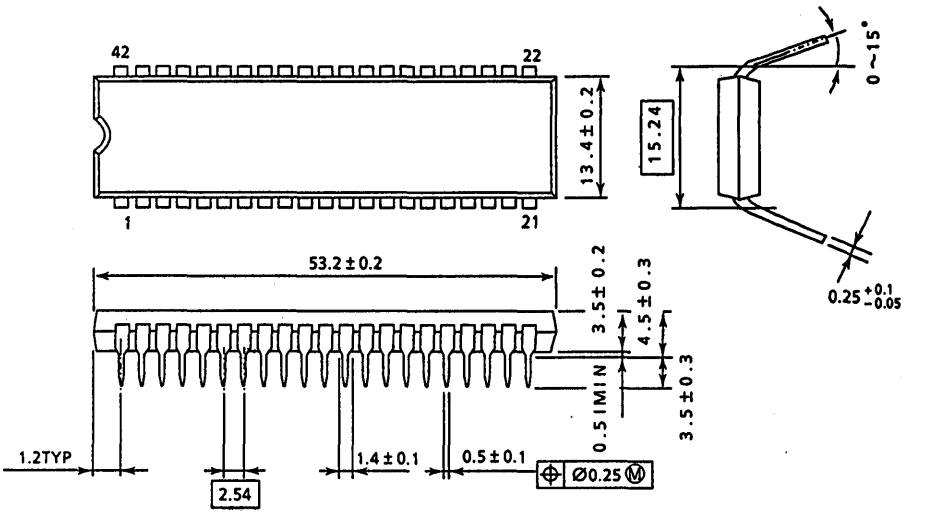
Note: CE($\overline{CE}$) = V_{IH}(V_{IL}), $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS

- Plastic DIP

DIP42-P-600.

Unit : mm

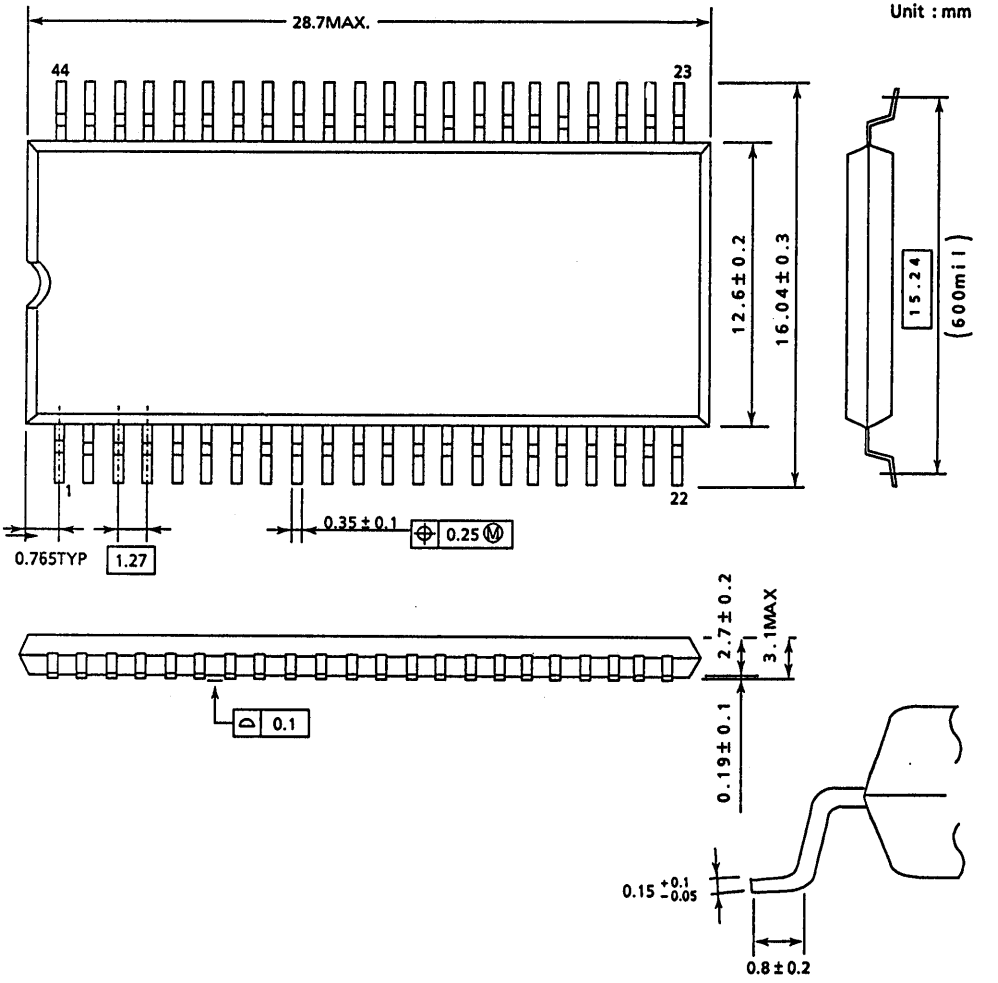


Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

- Plastic SOP

  SOP44-P-600



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

4M BIT (512K WORD × 8 BIT) CMOS MASK ROM

PRELIMINARY

DESCRIPTION

The TC534000AP/AF is a 4,194,304 bits read only memory organized as 524,288words by 8bits.

The TC534000AP/AF is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 150ns, an operation current of 40mA at 6.7MHz and a standby current of 20μA.

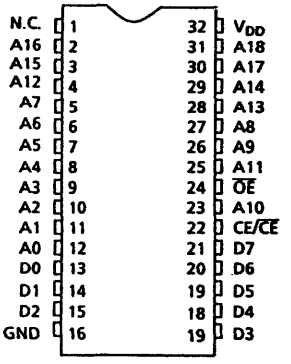
The TC534000AP/AF has one programmable chip enable input CE/$\overline{CE}$ for device selection.

The TC534000AP/AF is packaged in a standard 600mil 32pin DIP or 525mil 32pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.) V_{DD}=5V±10%
- Power Dissipation
  - Operating Current : 40mA (Max.)
  - Standby Current : 20μA (Max.)
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- Package Plastic DIP : TC534000AP
  Plastic FP : TC534000AF

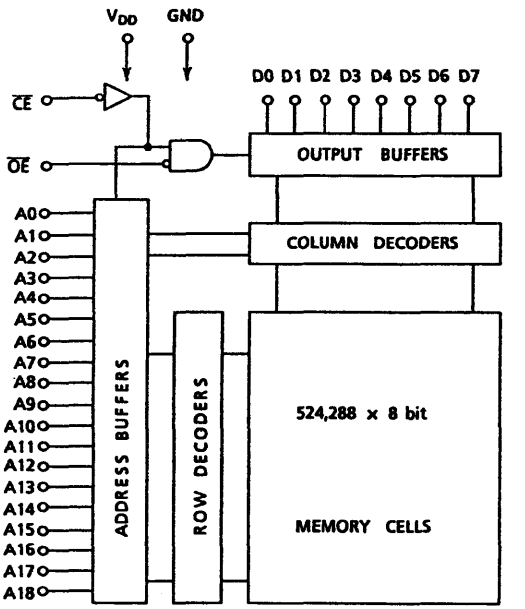
PIN CONNECTION



PIN NAMES

A0~A18	Address inputs
D0~D7	Data Outputs
$\overline{OE}$	Output Enable Input
CE/$\overline{CE}$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature - Time	260 · 10	°C · sec

Note : * Plastic FP.

D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS (V_{DD} = 5V ± 10% , Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	−	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} , V_{OUT} = 0~V_{DD}	−	± 5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	− 1.0	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	−	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	−	2	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} and V_{IN} = 0V (V_{DD})	−	20	μA
I_{DDO1}	Operating Current	V_{IN} = V_{IH} / V_{IL} , t_{cycle} = 150ns	−	50	mA
I_{DDO2}		V_{IN} = V_{DD} / 0V , t_{cycle} = 150ns	−	40	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz , Ta = 25°C	−	10	pF
C_{OUT}	Output Capacitance	f = 1MHz , Ta = 25°C	−	10	pF

Note: This Parameter is periodically sampled and is not 100% tested.

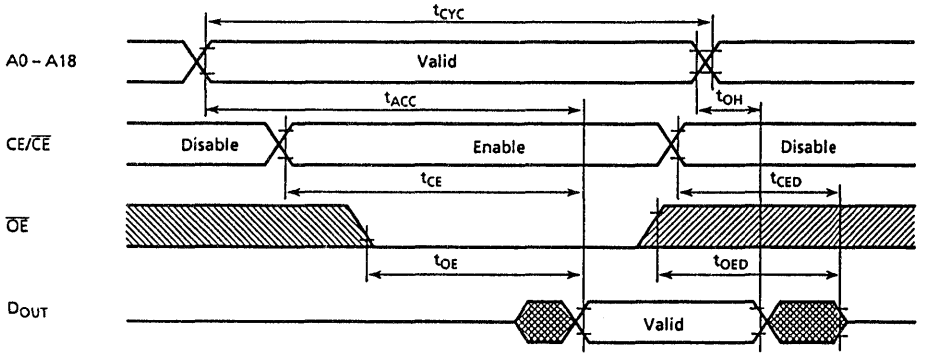
A.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	-	150	ns
t_{CE}	Chip Enable Access Time	-	150	ns
t_{OE}	Output Enable Access Time	-	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	0	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	0	60	ns
t_{OH}	Output Hold Time	10	-	ns
t_{CYC}	Cycle Time	150	-	ns

A.C. TEST CONDITIONS

Output Load		: 100pF + 1TTL
Input Levels		: 0.6V , 2.4V
Timing Measurement Reference Levels	Input	: 0.8V , 2.2V
	Output	: 0.8V , 2.0V
Input Rise and Fall Time		: 5ns

TIMING WAVEFORMS



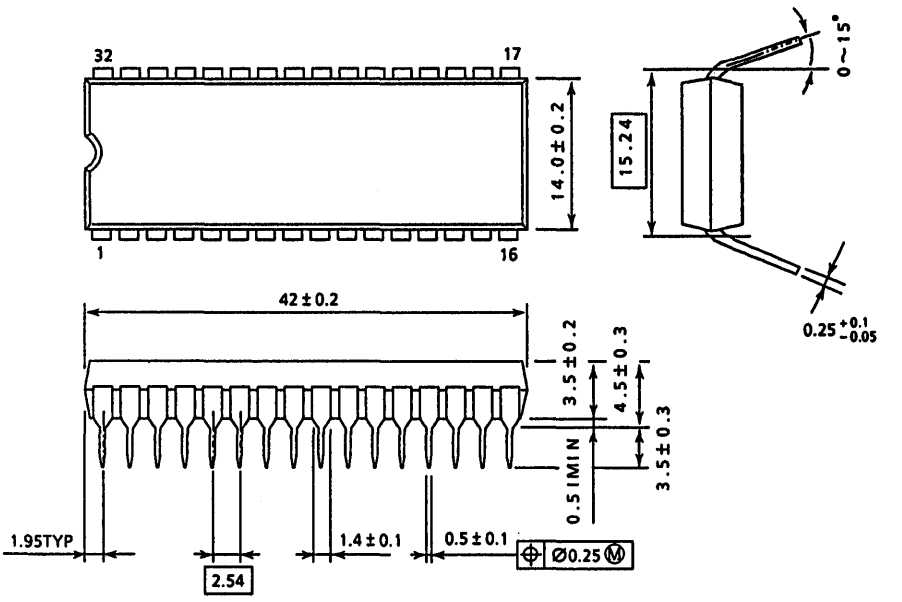
OPERATION MODE

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A0~A18	Outputs	Power
Read	L(H)	L	Valid	Data Out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H : VIH L : VIL * : VIH or VIL

OUTLINE DRAWINGS
Plastic DIP (DIP32-P-600)

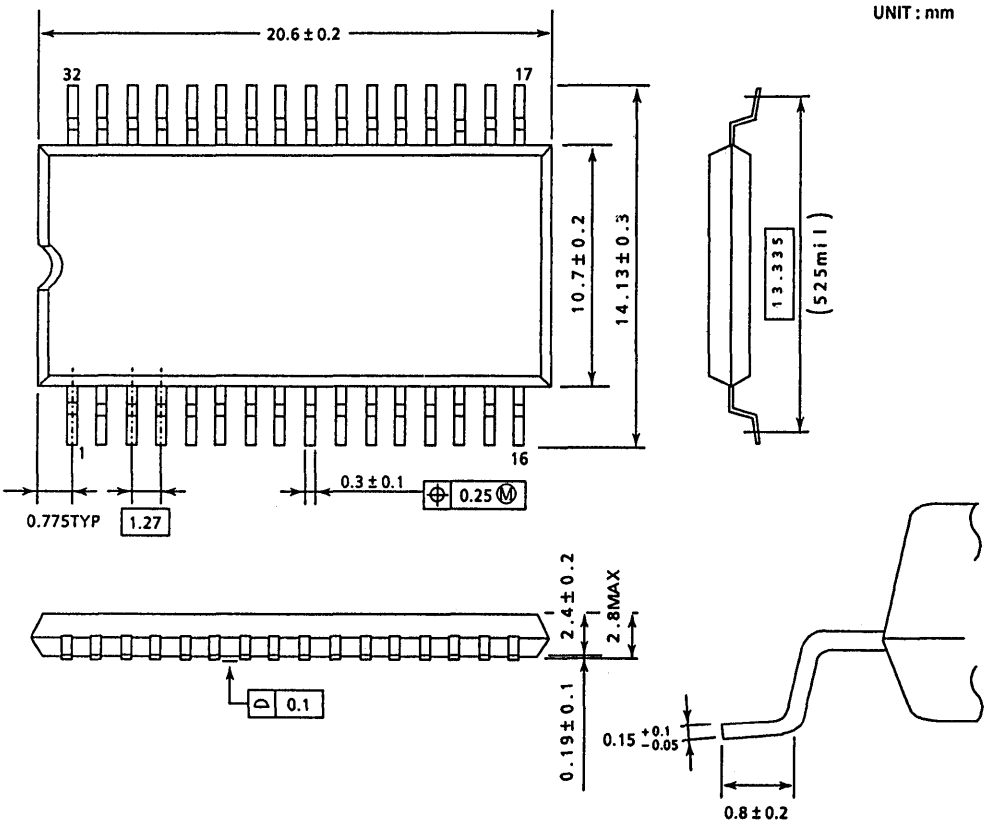
UNIT: mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS
Plastic FP (SOP32-P-525)

UNIT : mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

HIGH-SPEED MROM

TC53H1024P-85

TARGET

1M BIT (64K WORD x 16 BIT) HIGH-SPEED CMOS MASK ROM
SILICON GATE CMOS

DESCRIPTION

The TC53H1024P is a high-speed 1,048,576 bits read only memory organized as 65,536 words by 16 bits with a low bit cost, thus being suitable for use in program memory of microprocessors.

The TC53H1024P is molded in a 40 pin standard plastic package, 0.6 inch in width.

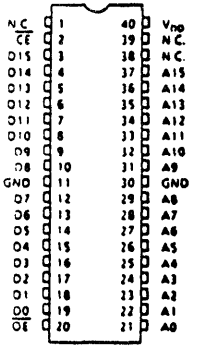
FEATURES

TC53H1024P	-85
Access Time (max)	85ns
Power Dissipation Operation Current (max)	60mA
Power Dissipation Standby Current (max)	100uA

- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- Fully Static Operation
- Pin Compatible with 1M High-Speed EPROM TC57H1024D
- Package
  Plastic DIP: TC53H1024P
- Single 5V Power Supply

PIN CONNECTION

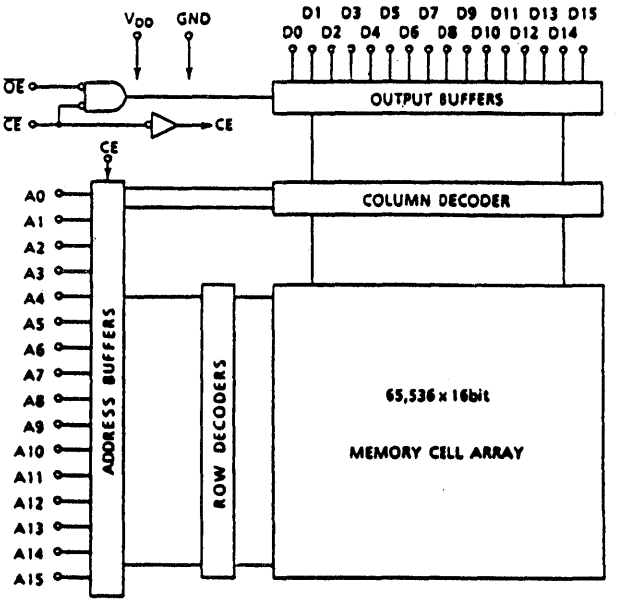
(TOP VIEW)



PIN NAMES

A0~A15	Address Inputs
D0~D15	Data Outputs
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C	No Connection

BLOCK DIAGRAM



Flash E^2 PROM

TC58257AP/AF 32,768 WORD x 8 BIT ELECTRICALLY CHIP ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

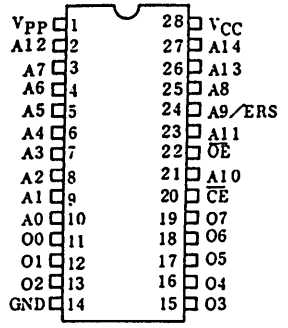
DESCRIPTION

TC58257AP/AF is a 32,768 word × 8 bit electrically chip erasable and programmable read only memory, and molded in a 28 pin plastic package. The TC58257AP/AF's access time is 170ns/200ns/250ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics are the same as U.V.EPROM TC57256AD's. For program operation, the programming is achieved by using the high speed programming mode. The TC58257AP/AF has an electrically chip erasing mode which can erase whole bits at the same time.

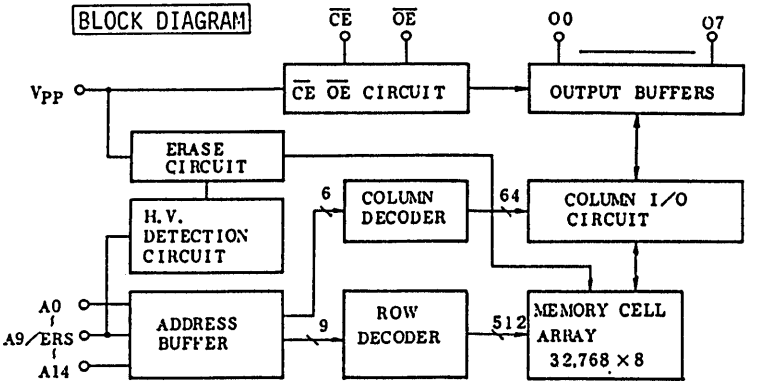
FEATURES

- Peripheral circuit: CMOS
  Memory cell : NMOS
- Fast access time: TC58257AP/AF-17LV 170ns
  TC58257AP/AF-20LV 200ns
  TC58257AP/AF-25LV 250ns
- Low power dissipation
  Active : 30mA/5.9MHz
  Standby: 100μA
- Full static operation
- High speed programming mode
- Electrically chip erasing mode
- Inputs and outputs TTL compatibility
- Pin compatible with MASK ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, and TC57256D/AD, one time PROM TMM24256P/AP/AF and TC54256P/AP/AF
- Standard 28 pin DIP
  plastic package : TC58257AP
- Plastic Flat package: TC58257AF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0~A14	Address Inputs
O0 ~ O7	Output (Input)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
A9/ERS	Address And Erase Control Input
VPP	Program And Erase Power Supply Voltage
VCC	VCC Power Supply Voltage
GND	Ground

MODE SELECTION

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	A9	VPP	VCC	A0~A8 (10~14)	O0 ~ O7	Power
Read	L	L	*	5V	5V	*	Data Output	Active
Output Deselect	*	H	*			*	High Impedance	
Standby	H	*	*			*	High Impedance	Standby
Program	L	H	*	12V	5V	*	Data Input	Active
Program Inhibit	H	*	*			*	High Impedance	
Program Verify	L	L	*			*	Data Out	
Chip Erase	L	H	12V	12V	5V	*	Don't Care	Active
Chip Erase Inhibit	H	*				*	High Impedance	

*: V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-10 ∿ 70	°C
N_{EW}	Erase Write Endurance	100	Cycles

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	V

DC AND OPERATING CHARACTERISTICS (Ta=-10 ∿ 70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$=0V	f=5.9MHz	-	-	30	mA
I_{CC02}			f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=V_{CC}-0.6∿V_{CC}+0.6		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4 ∿ V_{CC}		-	-	±10	μA

AC CHARACTERISTICS (Ta=-10∿70°C, V_{CC}=5V±10%, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	-17		-20		-25		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	170	-	200	-	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	170	-	200	-	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	70	-	70	-	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	0	60	0	90	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	0	-	0	-	ns

AC TEST CONDITIONS

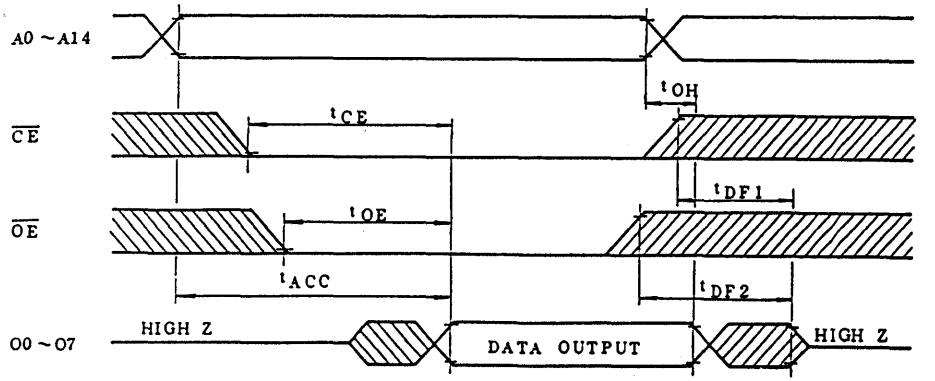
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V∿2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.5	5.0	5.5	V
V_{PP}	V_{PP} Power Supply Voltage	11.5	12.0	12.5	V

DC AND OPERATING CHARACTERISTICS (Ta=-10∿70°C, V_{CC}=5.0V±10%, V_{PP}=12.0V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0∿V_{CC}	-	-	10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS (Ta=-10∿70°C, V_{CC}=5.0V±10%, V_{PP}=12.0V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{DV}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	-	1	μs
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	-	-	150	ns

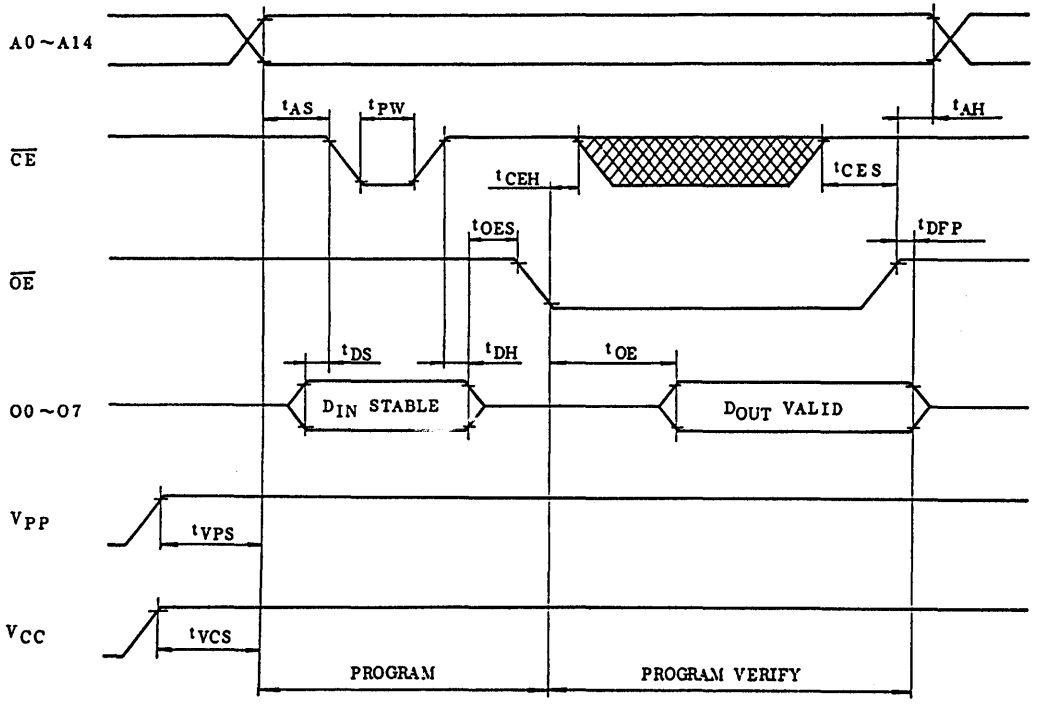
AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V∿2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=5.0V±10%, V_{PP}=12.0V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.0V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation.
So the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not exceed 14V.

ERASE OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.5	5.0	5.5	V
V_{PP}	V_{PP} Power Supply Voltage	11.5	12.0	12.5	V
V_{IHH}	Input High Voltage	11.5	12.0	12.5	V

DC AND OPERATING CHARACTERISTICS (Ta=-10∿70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0∿V_{CC}	-	-	±10	μA
I_{LIE}	A9/ERS Input Current	A9/ERS=0∿V_{IHH}	-	-	±100	μA
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=12.5V	-	-	50	mA

AC ERASING CHARACTERISTICS (Ta=-10∿70°C, V_{CC}=5V±10%, V_{PP}=12.0V±0.5V)

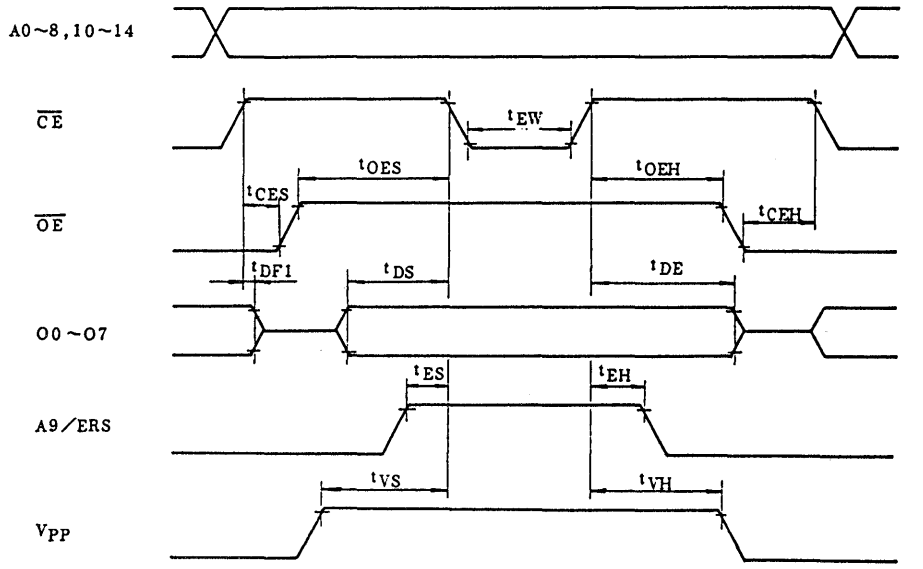
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}$ Hold Time	-	500	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	500	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VH}	V_{PP} Hold Time	-	500	-	-	μs
t_{ES}	A9/ERS Setup Time	-	2	-	-	μs
t_{EH}	A9/ERS Hold Time	-	2	-	-	μs
t_{EW}	Erase Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, A9=V_{IHH}	1950	2000	2050	ms
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	-	-	150	ns

Input Pulse Rise and Fall Time: 10ns Max.

Input Pulse Levels : 0.45V∿2.4V

TIMING WAVEFORMS (ERASE)

(V_{CC}=5V±10%, V_{PP}=12.0V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.0V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for erase operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not exceed 14V.

Read \ Pin		$\overline{CE}$	$\overline{OE}$	A9	V_{PP}	V_{CC}	O0 ∿ O7	Power
Read Operation	Read	L	L	*	5V	5V	Data Out	Active
	Output Deselect	*	H	*			High Impedance	
	Standby	H	*	*			High Impedance	Standby
Program Operation	Program	L	H	*	12V	5V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
	Program Verify	L	L	*			Data Out	
Erase Operation	Erase	L	H	12V	12V	5V	Don't Care	Active
	Erase Inhibit	H	*				High Impedance	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC58257AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operat power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TC58257AP/AF's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC58257AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC58257AP/AF is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC58257AP/AF are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC58257AP/AF is in the programming mode when the V_{PP} input is at 12V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$. The TC58257AP/AF can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check if desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.0V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC58257AP/AF from being programmed. Programming of two or more TC58257AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.0V) is applied to the V_{PP} terminal with $V_{CC}=5.0V$. The programming is achieved by applying a single TTL low level 100μs pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 100μs is applied and then the programmed data is verified. The should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

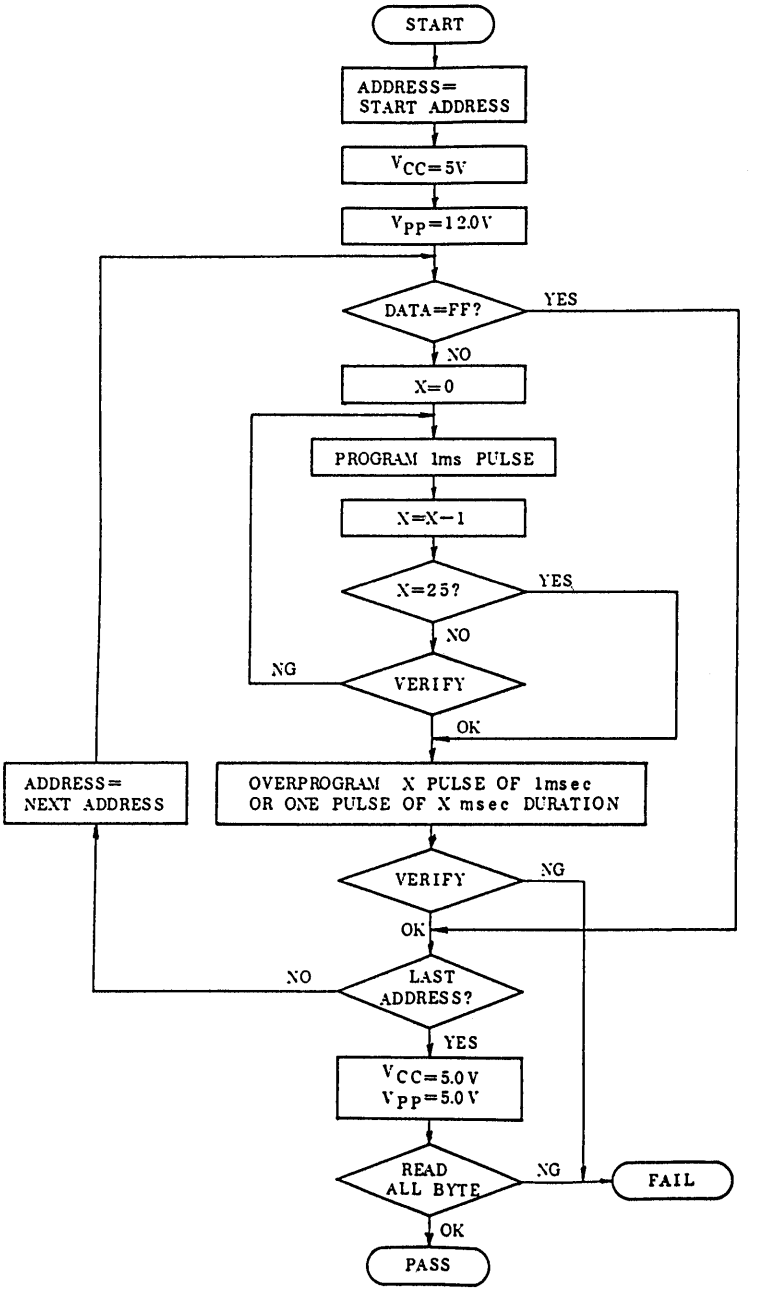
CHIP ERASE MODE

The TC58257AP/AF is in chip erase mode when the Vpp input is 12.0V and $\overline{CE}$ is at TTL-Low level under the condition of A9=12V, $\overline{OE}=V_{IH}$. The chip erase pulse width is only 1 sec. Once chip is erased, all bits of the device are in "1" state.

ERASE INHIBIT

Under the condition that the erase voltage (12.0V) is applied to Vpp terminal and 12V is to A9 input, TTL-High level $\overline{CE}$ input inhibits the TC58257AP/AF from being erased.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TC58257AP/AF which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC58257AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is the manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7). The following table shows the electric signature of TC58257AP/AF.

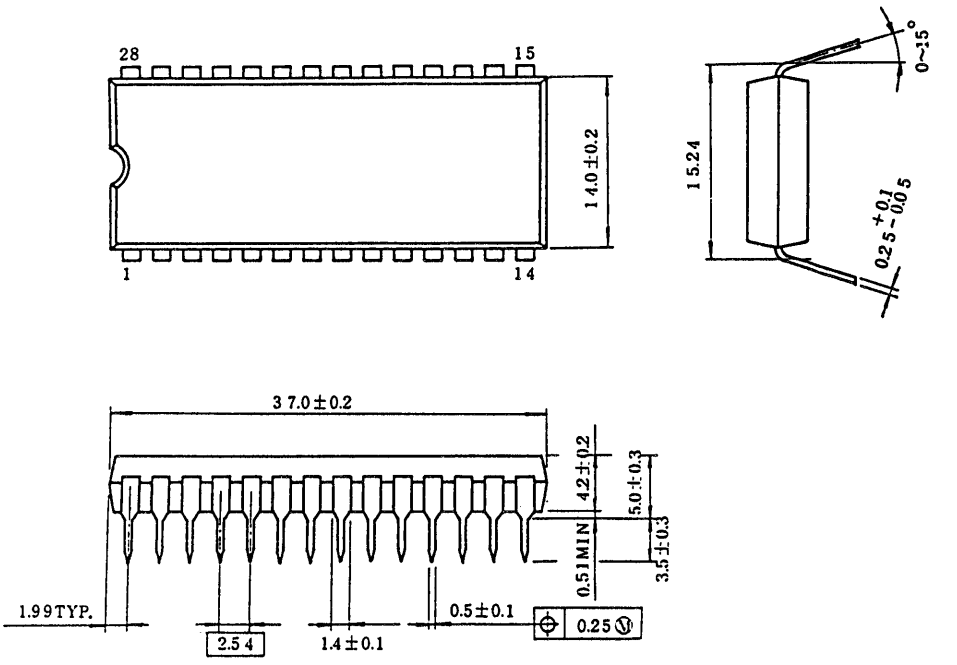
PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	1	0	0	1	0	1	25

Notes: A9=12V±0.5V

A1∿A8, A10∿A14, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS (TC58257AP)

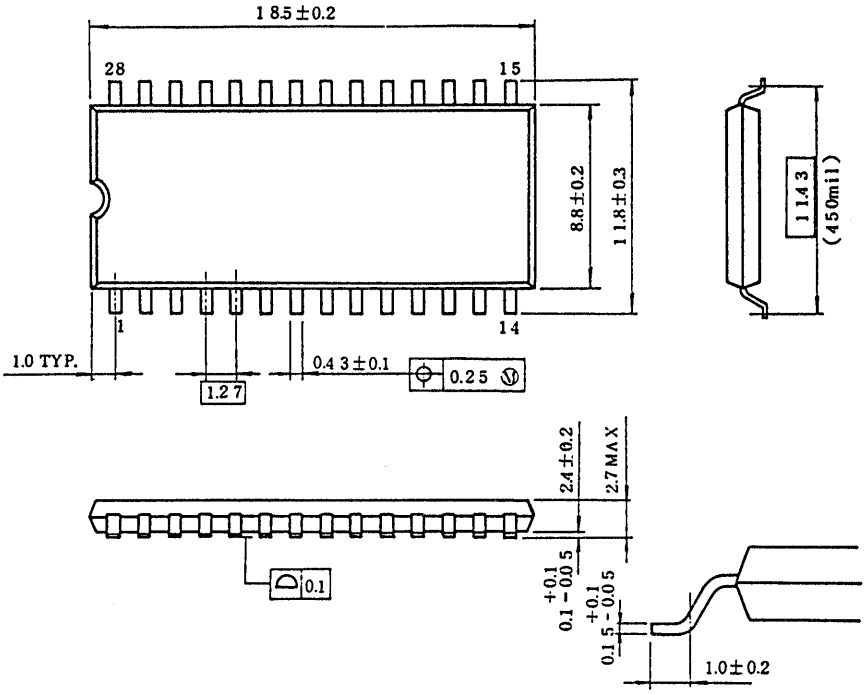
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (TC58257AF)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

TC58F1000P/F/J 131,072WORD × 8BIT CMOS FLASH E^2 PROM

DESCRIPTION

The TC58F1000P/F/J is a 1,048,576 bits, Flash Electrically Erasable and Programmable Read Only Memory (FE^2PROM) organized as 131,072 words by 8 bits. The TC58F1000P/F/J is fabricated by using advanced CMOS technology which provides the high speed and low power features with access times of 150ns/200ns, an operating current of 30mA at 6.7 MHz and a standby current of 100μA.

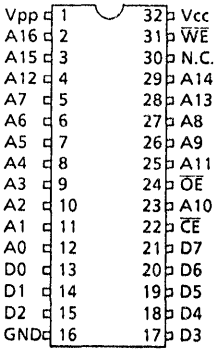
The TC58F1000P/F/J features a command control mode and an EPROM compatible mode for programming and erasing. The command control mode is used for in-system programming controlled by the MPU timing. A specific software sequence must be executed to enable the program, program-verify, chip-erase, block-erase, erase-verify, signature read and mode reset operations. The EPROM compatible mode is used for programming and erasing with a conventional EPROM programmer. The programming time is 14-seconds and the erasing time is only 1-second. The TC58F1000P/F/J is also provided with a block-erase feature. The programming time of 1 block (4K byte) is only 0.5-second.

The TC58F1000P/F/J has a JEDEC standard pinout configuration and is packaged in either a 32-pin plastic DIP, 32-pin flat package (SOP) or 32-pin SOJ.

FEATURES

- Access time : 150ns/200ns
- Power dissipation
  - Operating : 30mA
  - Standby : 100μA
- Erase/Write endurance
  - 100 cycles
  - 10,000 cycles (Option)
- High-speed programming
  - 14 second/chip
  - 0.5 second/block
- Electrical erase mode
  - Chip erase 1 second
  - Block erase 1 second
  - (Block size : 4K Byte × 32 blocks)
- Package options
  - suffix "P" : 32-pin Plastic DIP
  - suffix "F" : 32-pin Plastic flat package (SOP)
  - suffix "J" : 32-pin Plastic SOJ
- Program/Erase mode
  - Command control mode
  - EPROM compatible mode

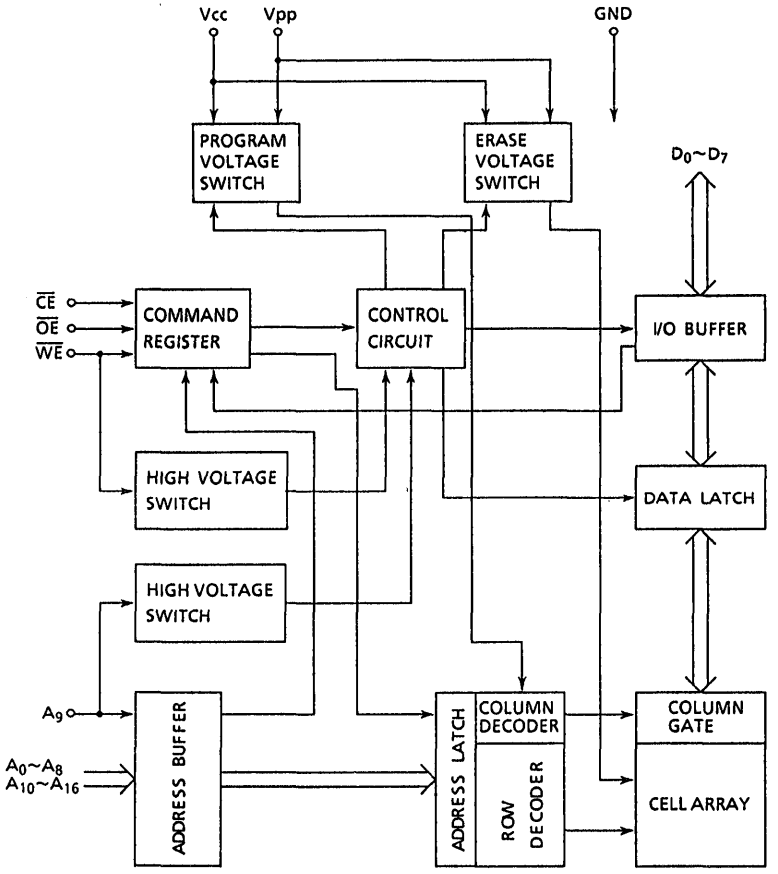
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~16	Address input
D0~7	Data input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable/EPROM mode switch
N.C.	NO connection
V_{PP}	Program and erase power Supply
V_{CC}	Power Supply
GND	Ground

BLOCK DIAGRAM



OPERATING MODE

<Command Control Mode>

① $\overline{WE}$ Control

MODE		$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~7	Power
Read	Read	H	L	L	0V~V_{CC} or 12V	5V	Data Output	Active
	Output Deselect	*	*	H			High-Z	
	Standby	*	H	*				Standby
Command Input		⌐⌐	L	H	12V	5V	Data Input	Active
Program or Erase		H	*	*			**	
Program Verify or Erase Verify		H	L	L			Data Output	
Signature Read		H	L	L			Code Output	

Note : *: V_{IH} or V_{IL}, H: V_{IH}, L: V_{IL}
**: Data Input or Data Output or High-Z

② $\overline{CE}$ Control

MODE		$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~7	Power
Read	Read	H	L	L	0V~V_{CC} or 12V	5V	Data Output	Active
	Output Deselect	*	*	H			High-Z	
	Standby	*	H	*				Standby
Command Input		L	⌐⌐	H	12V	5V	Data Input	Active
Program or Erase		H	*	*			**	
Program Verify or Erase Verify		H	L	L			Data Output	
Signature Read		H	L	L			Code Output	

Note : *: V_{IH} or V_{IL}
**: Data Input or High-Z

<EPROM Compatible Mode>

MODE		A9	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~7	Power
Read	Read	*	H	L	L	0V~V_{CC} or 12V	5V	Data Output	Active
	Output Deselect	*	*	*	H			High-Z	
		*	L	*	*				
	Standby	*	*	H	*				Standby
Program	Program	*	V_{WE}	L	H	12V	5V	Data Input	Active
	Program Inhibit	*	V_{WE}	H	*			High-Z	
	Program Verify	*	V_{WL}	*	L			Data Output	
Erase (Chip Erase)	Erase	V_{ID}	V_{WE}	L	H	12V	5V	*	Active
	Erase inhibit	V_{ID}	V_{WE}	H	*			High-Z	
Signature Read		V_{ID}	H	L	L	0V~V_{CC} or 12V	5V	Code Output	Active

Note : *: V_{IH} or V_{IL}, H: V_{IH}, L: V_{IL}
V_{ID}, V_{WE} = 12V

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{CC}	Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program / Erase Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input / Output Voltage	−0.6~V_{CC} + 0.5	V
P_D	Power Dissipation	1.0 / 0.6*	W
T_{SOLDER}	Soldering Temperature · Time	260·10	°C·sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
N_{EW}	Erase Write Endurance	100 / 10000**	Cycle
V_{ID} / V_{WE}	Input Voltage (A9 / $\overline{WE}$)	−0.6~13.5	V

Note : * Plastic FP & Plastic SOJ
** 10000 cycle is optional

D.C. RECOMMENDED OPERATING CONDITION (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
V_{CC}	Vcc Power Supply Voltage	4.5	5.5	V
V_{IH}	Input high Voltage	2.2	V_{CC} + 0.3	
V_{IL}	Input Low Voltage	−0.3	0.8	
V_{ID}	A9 Pin Identifier Mode Voltage	11.4	12.6	
V_{WE}	WE Pin EPROM Command Mode Switch Voltage	11.4	12.6	
V_{PP}	V_{PP} Power Supply Voltage (Read Operation and Signature Read Operation)	0	12.6	
	V_{PP} Power Supply Voltage (Program, Erase, and Verify Operation)	11.4	12.6	

D.C. AND OPERATING CHARACTERISTICS (Ta=0~70°C, VCC=5.0V±10%, VPP=12.0V±5%)

SYMBOL	PARAMETER		TEST CONDITION	MIN	MAX	UNIT
I_{LI}	Input Leakage Current		$0V \leqq V_{IN} \leqq V_{CC}$	–	± 10	μA
I_{LO}	Output Leakage Current		$0V \leqq V_{OUT} \leqq V_{CC}$	–	± 10	
V_{OH}	Output High Voltage		$I_{OH} = -0.400mA$	2.4	–	V
V_{OL}	Output Low Voltage		$I_{OL} = +2.10mA$	–	0.4	
I_{CC1}	V_{CC} Supply Current (Read / Verify / Signature Read Operation)		$V_{IN} = V_{IH} / V_{IL}$, $I_{OUT} = 0mA$, $t_{cycle} = 150ns$	–	30	mA
I_{CC2}	V_{CC} Supply Current (Program / Erase Operation)		$V_{IN} = V_{IH} / V_{IL}$, $I_{OUT} = 0mA$, $t_{cycle} = 90\mu s$	–	30	
I_{CCS1}	V_{CC} Standby Current (Read Operation)		$\overline{CE} = V_{IH}$	–	1	mA
I_{CCS2}			$\overline{CE} = V_{CC} - 0.20V$	–	100	μA
I_{PP1}	V_{PP} Supply Current (Read / Verify / Signature Read Operation)		$0V \leqq V_{PP} \leqq V_{CC} + 0.6V$, $V_{IN} = V_{IH} / V_{IL}$	–	± 10	μA
			$11.4V \leqq V_{PP} \leqq 12.6V$, $V_{IN} = V_{IH} / V_{IL}$	–	200	
I_{PP2}	V_{PP} Supply Current	Program	$11.4V \leqq V_{PP} \leqq 12.6V$	–	50	mA
		Erase	$V_{IN} = V_{IH} / V_{IL}$	–	30	
I_{ID}	A9 Pin Identifier Mode Current		$11.4V \leqq V_{ID} \leqq 12.6V$	–	200	μA
I_{WE}	$\overline{WE}$ Pin EPROM Compatible Mode Switch Current		$11.4V \leqq V_{WE} \leqq 12.6V$	–	200	

A.C. CHARACTERISTICS

1. READ OPERATION (Ta=0~70°C, V_{CC}=5.0V±10%, V_{PP}=0V~V_{CC} or 12.0V±5%)

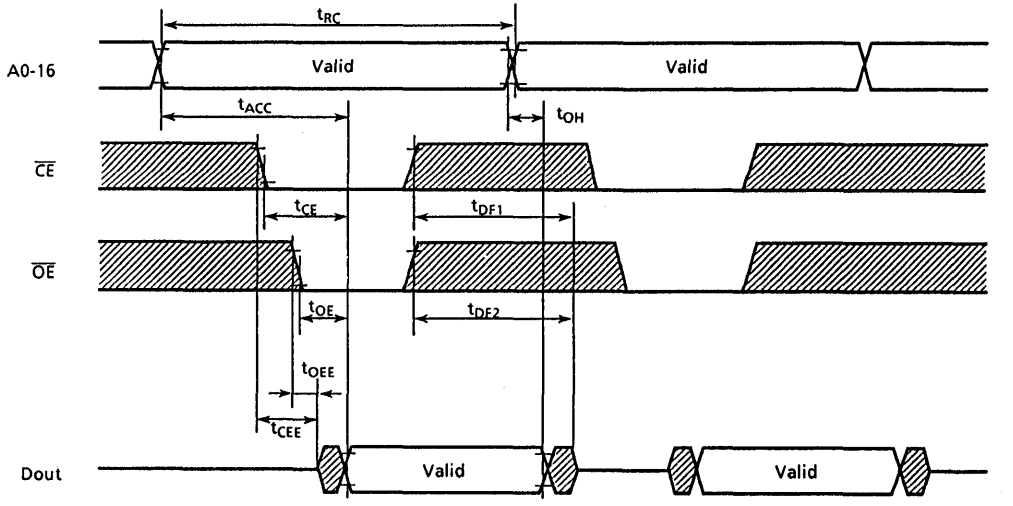
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	150/200*	-	-	ns
t_{ACC}	Address Access Time	-	-	150/200*	
t_{CE}	Chip Enable Access Time	-	-	150/200*	
t_{OE}	Output Enable Access Time	-	-	70	
t_{CEE}	Chip Enable to Output in Low-Z	0	-	-	
t_{OEE}	Output Enable to Output in Low-Z	0	-	-	
t_{OH}	Output Data Hold Time	0	-	-	
t_{DF1}	Chip Enable to Output in High-Z	-	-	60	
t_{DF2}	Output Enable to Output in High-Z	-	-	60	

Note : * 150ns for TC58F1000P/F/J-15
200ns for TC58F1000P/F/J-20

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time (10%~90%) : 5ns
- Input Pulse Levels : 0.45V to 2.40V
- Timing Measurement Reference Levels Input : 0.80V/2.20V
  Output : 0.80V/2.00V

Timing Waveform of Read Cycle



2. COMMAND CONTROL OPERATION (Ta = 0~70°C, V_{CC} = 5.0V ± 10%, V_{PP} = 12.0V ± 5%)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{AS}	Address Setup time	0	–	–	ns
t_{AH}	Address Hold time	100	–	–	
t_{CES}	Chip Enable Setup time or Command Cycle	0	–	–	
t_{CEH}	Chip Enable Hold time or Command Cycle	10	–	–	
t_{OES}	Output Enable Setup time	0	–	–	
t_{OEH}	Output Enable Hold time	10	–	–	
t_{WES}	Write Enable Setup time on Command Cycle	0	–	–	
t_{WEH}	Write Enable Hold time on Command Cycle	10	–	–	
t_{DS}	Data Setup time	50	–	–	
t_{DH}	Data Hold time	0	–	–	
t_{WELH}	Write Enable Low Level Hold time	100	–	–	
t_{WEHH}	Write Enable High Level Hold time	50	–	–	
t_{CELH}	Chip Enable Low Level Hold time	90	–	–	
t_{CEHH}	Chip Enable High Level Hold time	50	–	–	
t_{CMC}	Command Cycle time	150	–	–	
t_{PH}	Programming Hold time	90	–	150	µs
t_{PRV}	Program Recovery time before Program Verify	2	–	–	
t_{EH}	Erasing Hold time	0.9	–	1.5	s
t_{ERV}	Erase Recovery time before Erase Verify	500	–	–	µs
t_{ACC}	Address Access time	–	–	150/200*	ns
t_{CE}	Chip Enable Access time	–	–	150/200*	
t_{OE}	Output Enable Access time	–	–	70	
t_{CEE}	Chip Enable to Output in Low-Z	0	–	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	–	
t_{OH}	Output Data Hold time	0	–	–	
t_{DF1}	Chip Enable to Output in High-Z	–	–	60	
t_{DF2}	Output Enable to Output in High-Z	–	–	60	
t_{WESV}	Write Enable Setup time on Verify Cycle	0	–	–	
t_{WEHV}	Write Enable Hold time on Verify Cycle	0	–	–	
t_{RC}	Verify Cycle time	150/200*	–	–	

Note : * 150ns for TC58F1000P/F/J-15
200ns for TC58F1000P/F/J-20

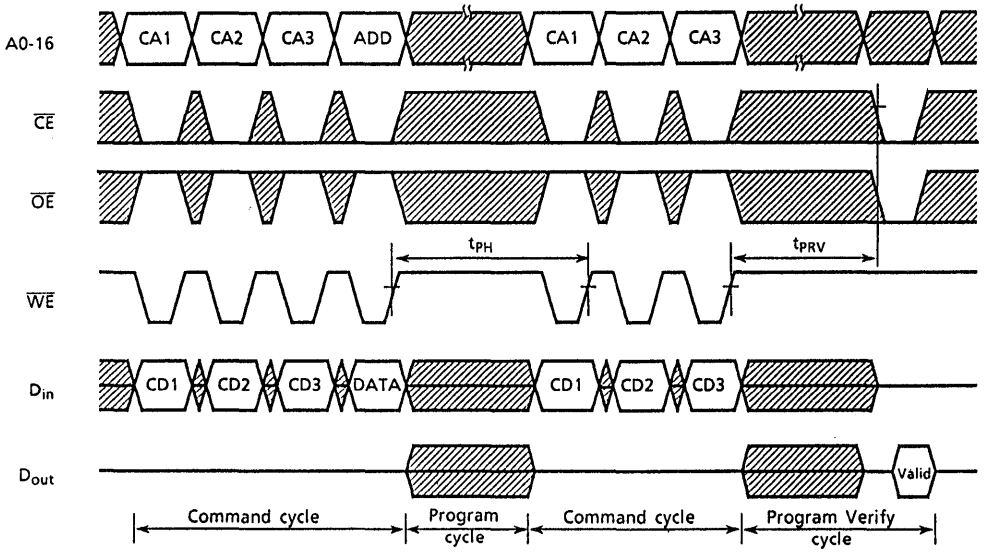
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time (10%~90%) : 5ns
- Input Pulse Levels : 0.45V to 2.40V
- Timing Measurement Reference Levels Input : 0.80V/2.20V
  Output : 0.80V/2.00V

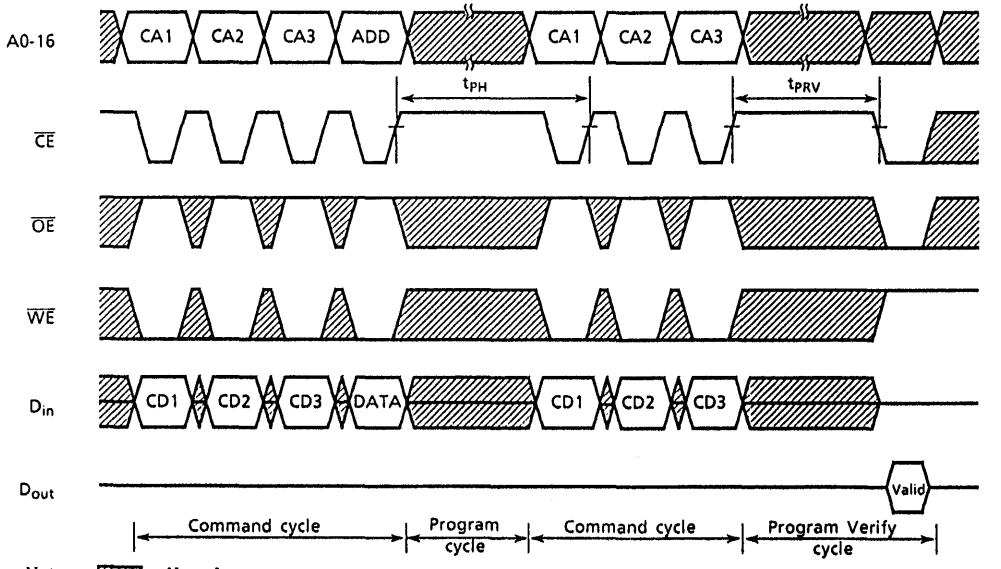
Timing Waveform of Command Control Operation

Program and Program Verify Operation

$\overline{WE}$ Control



$\overline{CE}$ Control



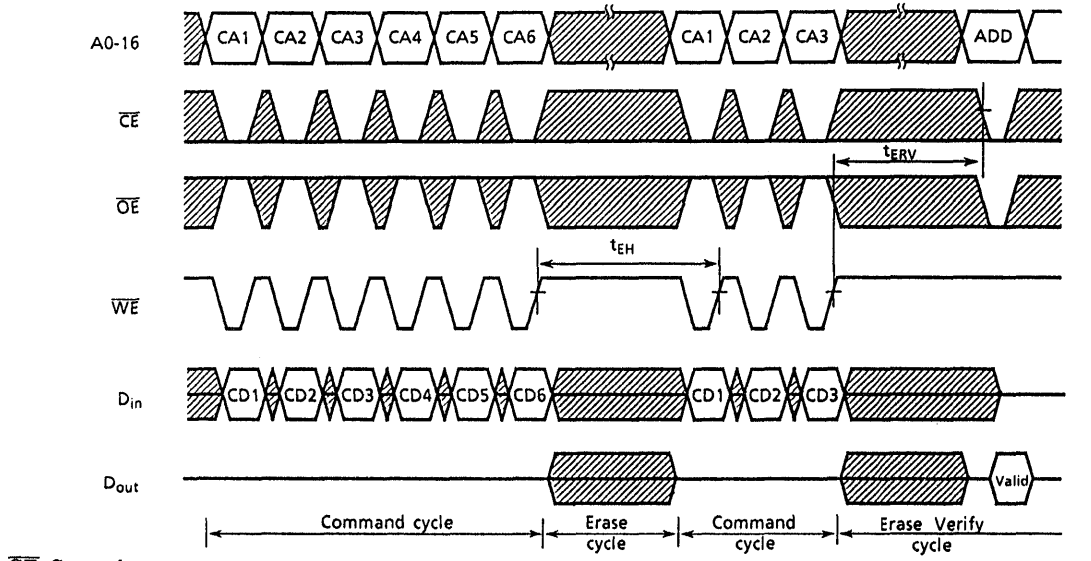
Note : H or L

: H or L or Hi-Z

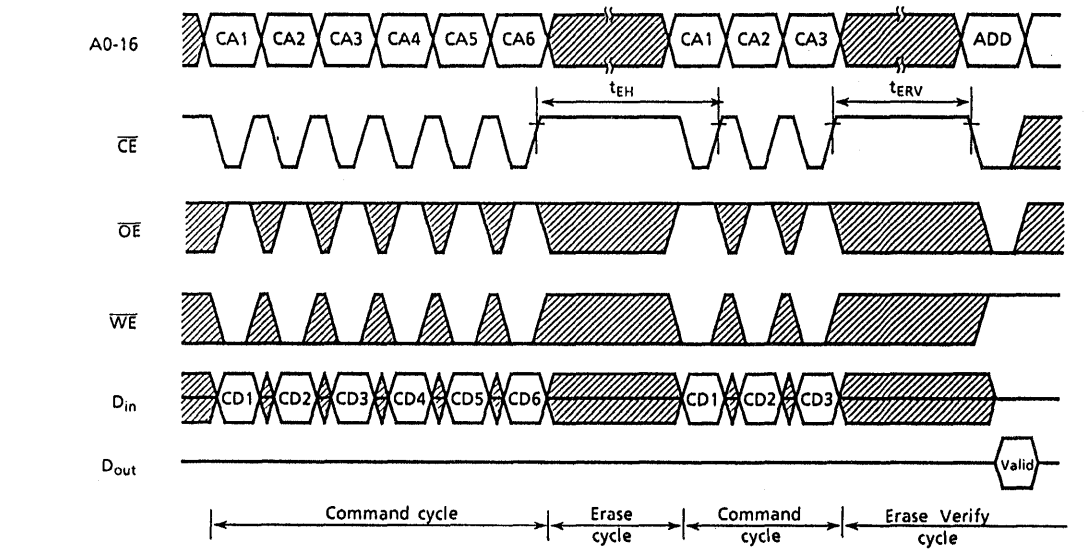
Timing Waveform of Command Control Operation

Chip Erase and Erase Verify Operation

$\overline{WE}$ Control



$\overline{CE}$ Control



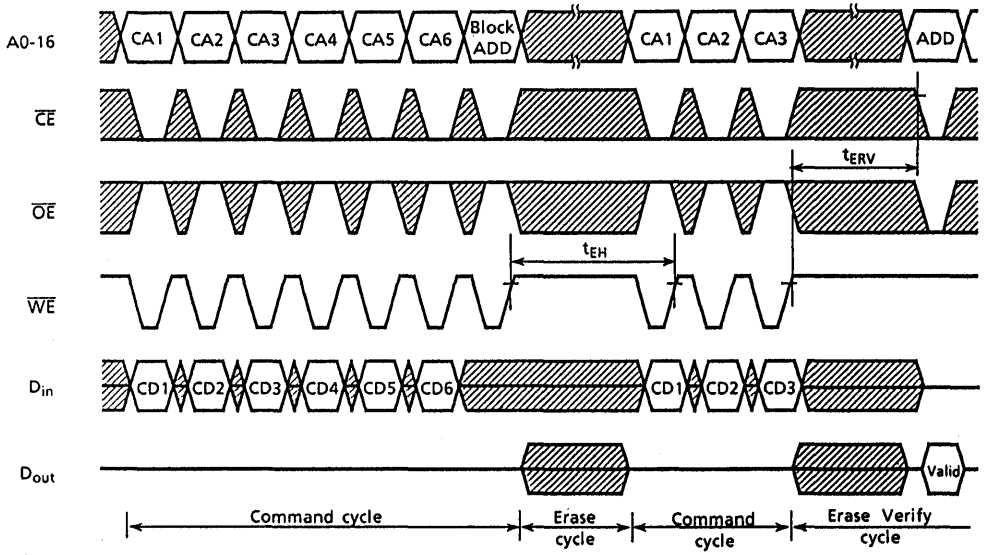
Note : H or L

: H or L or Hi-Z

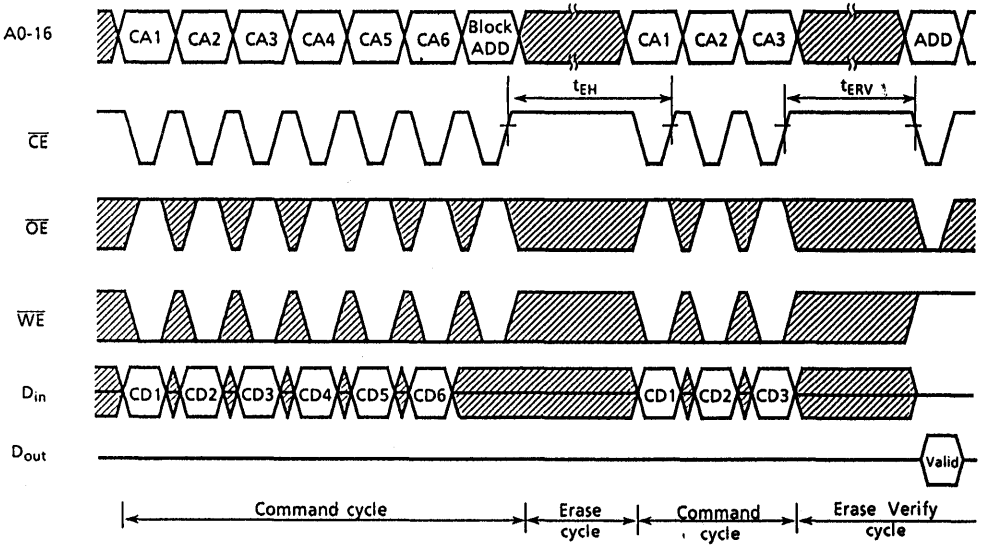
Timing Waveform of Command Control Operation

Block Erase and Erase Verify Operation

$\overline{WE}$ Control



$\overline{CE}$ Control



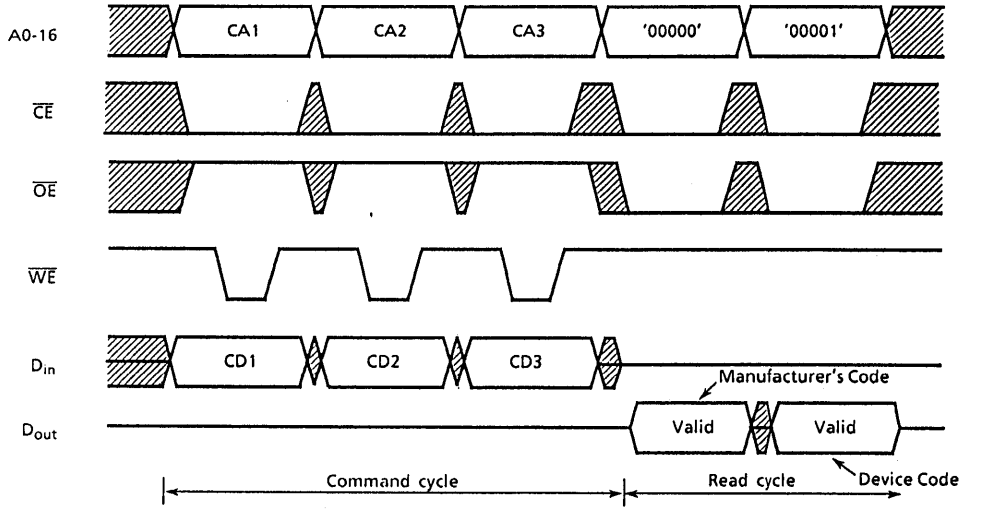
Note : H or L

: H or L or Hi-Z

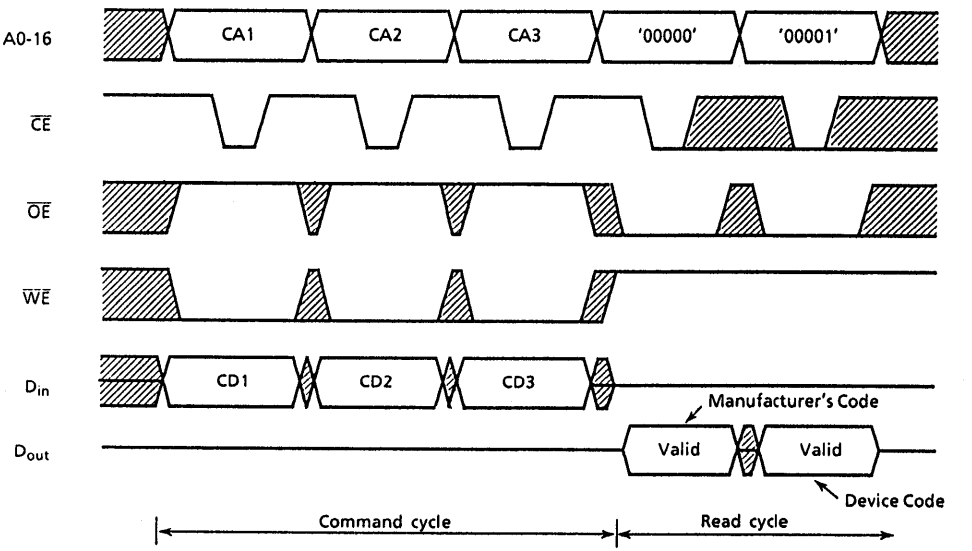
Timing Waveform of Command Control Operation

Signature Read Operation

$\overline{WE}$ Control



$\overline{CE}$ Control



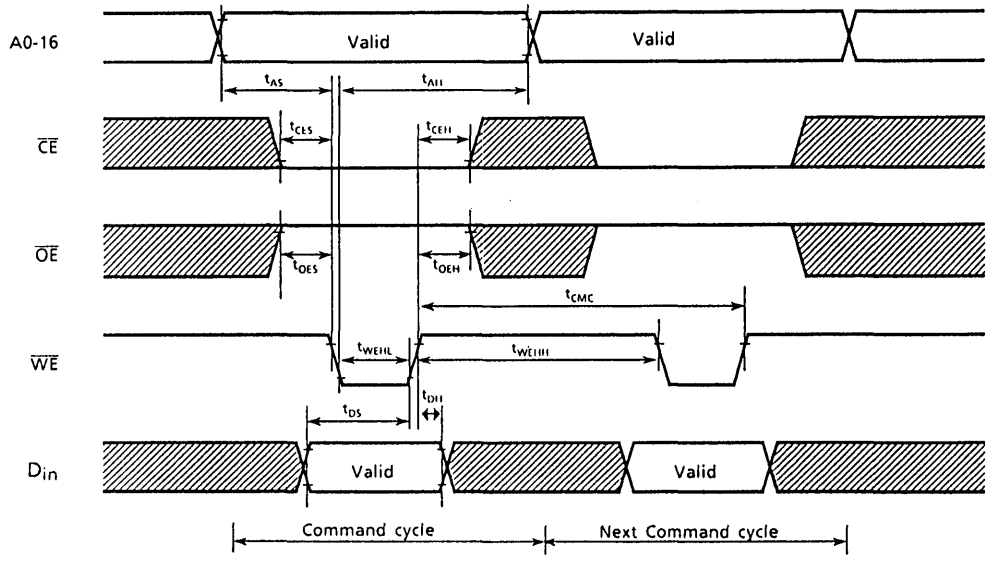
Note : H or L

: H or L or Hi-Z

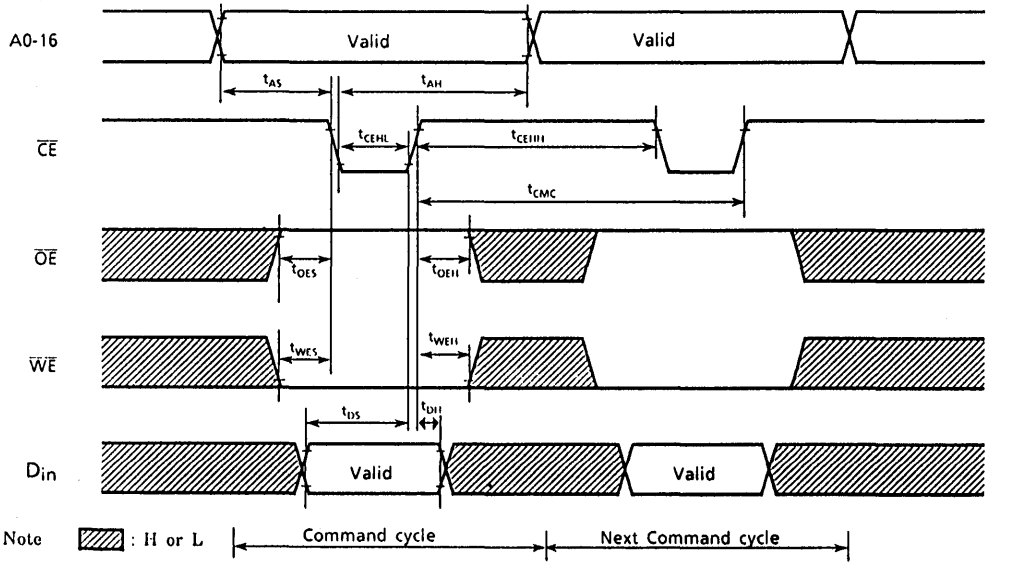
Timing Waveform of Command Control Operation

Timing Waveform of Command Cycle

$\overline{WE}$ Control

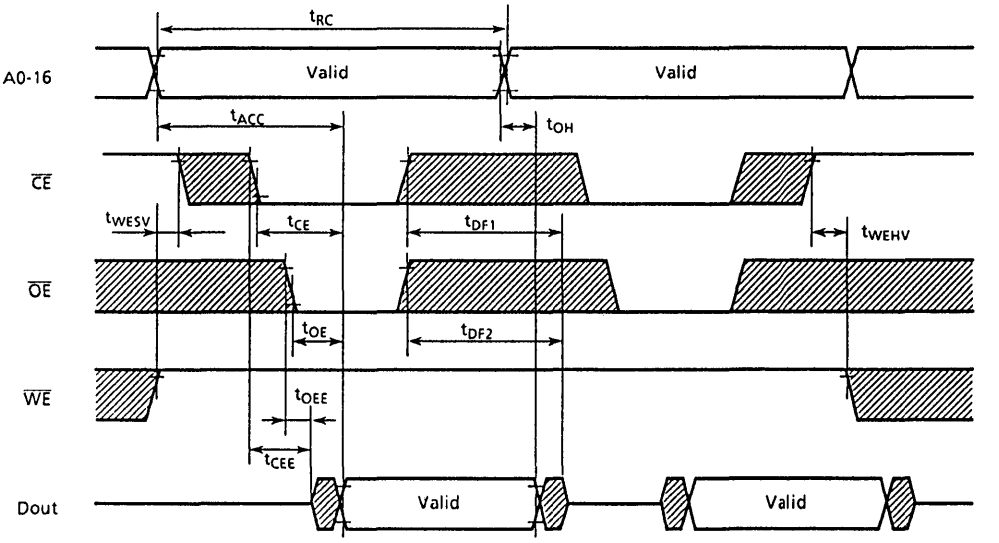


$\overline{CE}$ Control



Timing Waveform of Command Control Operation

Timing Waveform of Verify Cycle



Note : H or L

3. EPROM COMPATIBLE OPERATION

(Ta=0~70°C, V_{CC}=5V±10%, V_{PP}=12.0V±5%, V_{WE}=12.0V±5%)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT
t_{AS}	Address Setup time	0	–	–	ns
t_{AH}	Address Hold time	100	–	–	
t_{WP}	Programming Pulse Width	90	120	150	µs
t_{OESP}	Output Enable Setup time on Program Operation	2.0	–	–	
t_{DS}	Data Setup time	50	–	–	ns
t_{DH}	Data Hold time	0	–	–	
t_{EW}	Erasing Pulse Width	0.9	1.2	1.5	s
t_{OESE}	Output Enable Setup time on Erase Operation	0	–	–	ns
t_{OEHE}	Output Enable Hold time on Erase Operation	500	–	–	µs
t_{ACC}	Address Access time	–	–	150/200*	ns
t_{CE}	Chip Enable Access time	–	–	150/200*	
t_{OE}	Output Enable Access time	–	–	70	
t_{CEE}	Chip Enable to Output in Low-Z	0	–	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	–	
t_{OH}	Output Data Hold time	0	–	–	
t_{DF1}	Chip Enable to Output in High-Z	–	–	60	
t_{DF2}	Output Enable to Output in High-Z	–	–	60	
t_{RC}	Read/Verify cycle time	150/200*	–	–	
t_{VS}	V_{PP} Setup time	2.0	–	–	µs
t_{A9S}	V_{ID} Setup time	2.0	–	–	
t_{WES}	V_{WE} Setup time	2.0	–	–	

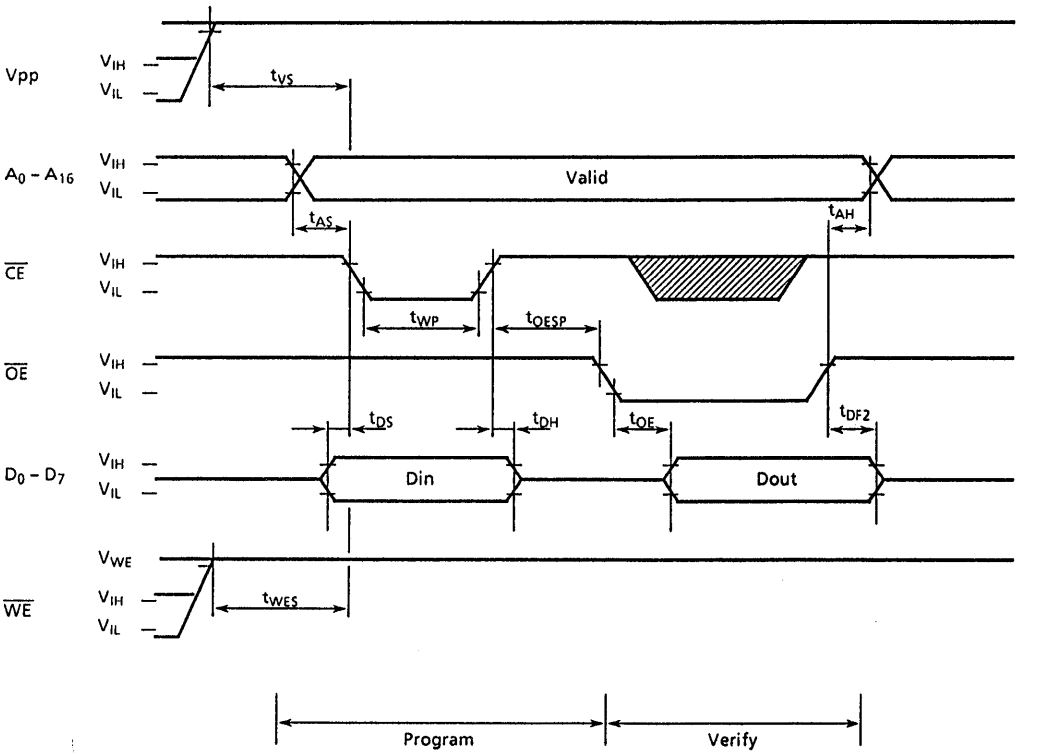
Note : * 150ns for TC58F1000P/F/J-15
200ns for TC58F1000P/F/J-20

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time (10%~90%) : 5ns
- Input Pulse Levels : 0.45V to 2.40V
- Timing Measurement Reference Levels Input : 0.80V/2.20V
  Output : 0.80V/2.00V

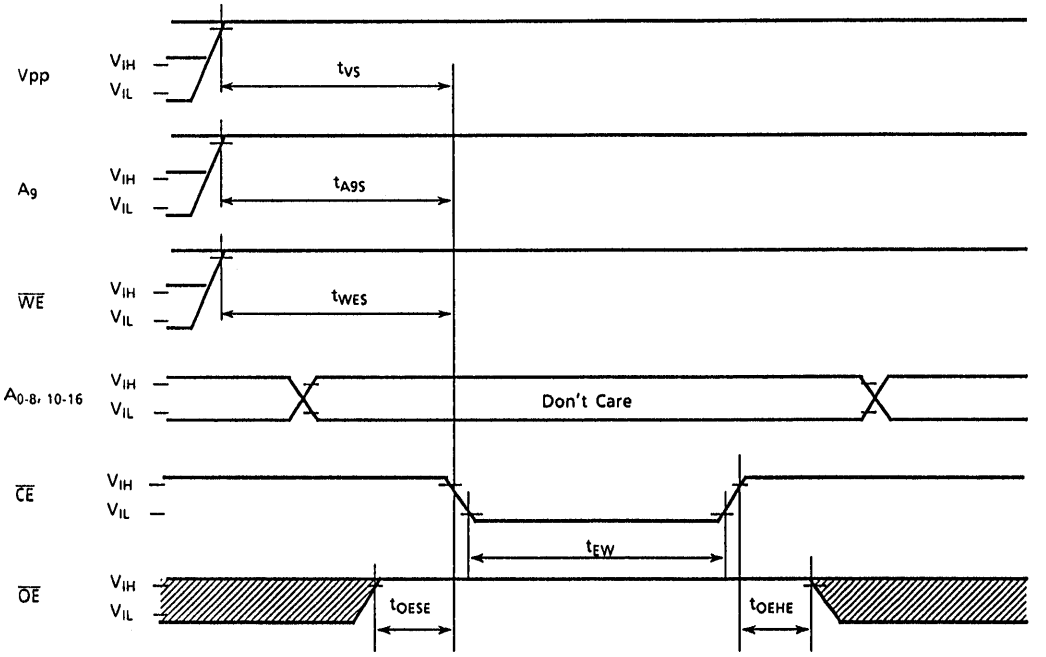
Timing Waveform of EPROM Compatible Operation

Program and Program Verify Operation



Timing Waveform of EPROM Compatible Operation

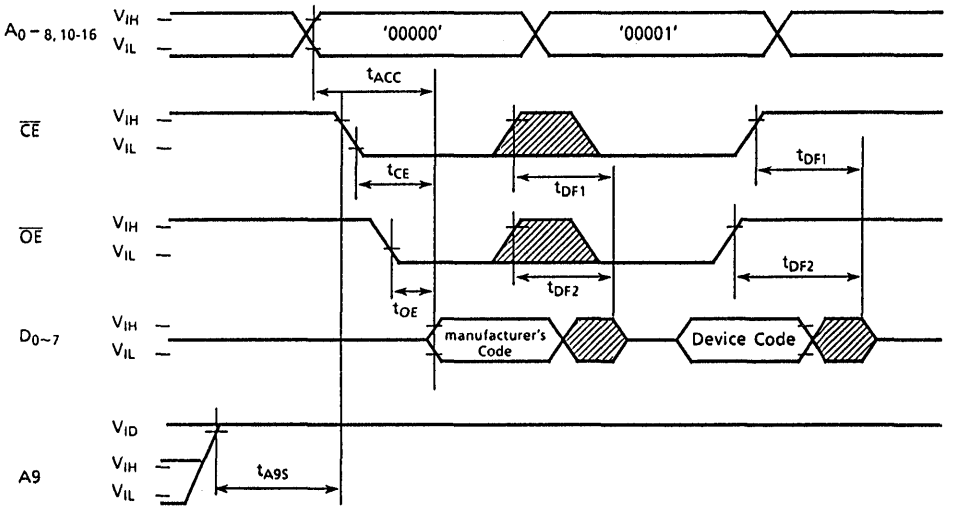
Erase Operation



Note : Din is don't care (H or L)

Timing Waveform of EPROM Compatible Operation

Signature Read Operation

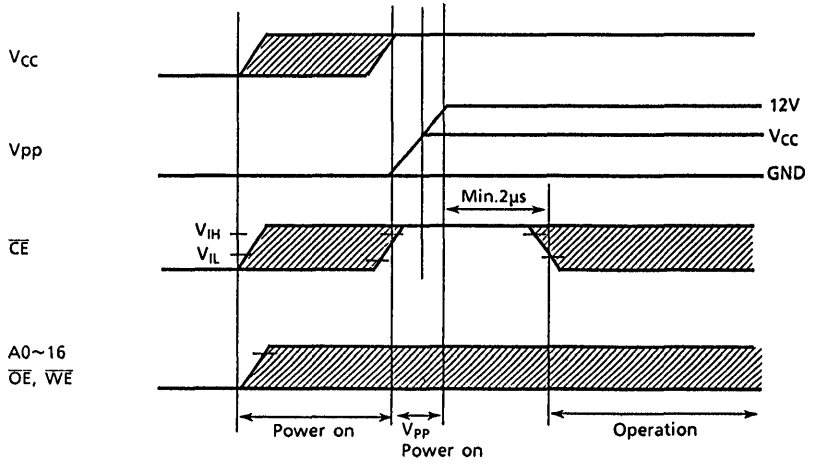


Note : $\overline{WE}=V_{IH}$, $V_{PP}=0V\sim V_{CC}$ or 12V

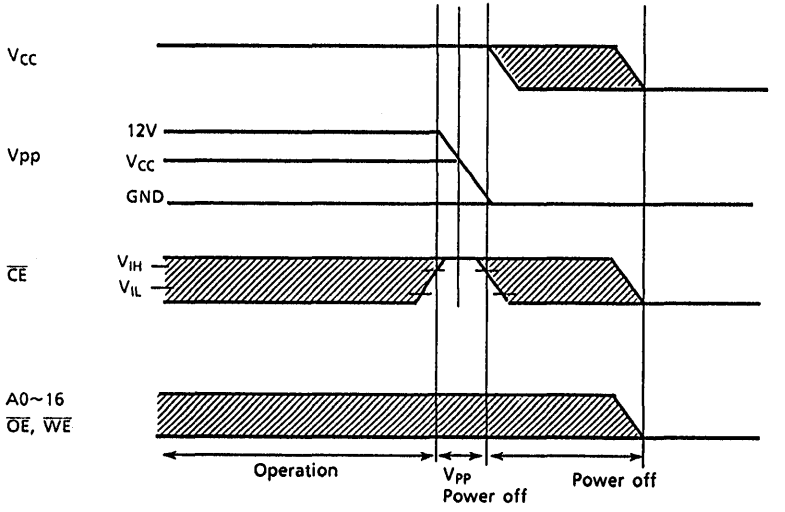
POWER ON / OFF SEQUENCE

This power on/off sequence protects against inadvertent programming or erasure.
In case of power on, V_{CC} and $\overline{CE}$ must be high level before V_{PP} becomes a high level.
In case of power off, V_{CC} and $\overline{CE}$ must remain high level until V_{PP} becomes a low level.

(1) Power on



(2) Power off



OPERATIONS

READ

The TC58F1000P / F / J has two control input pins. The chip enable ($\overline{CE}$) controls the operating power and should be used for device selection / deselection. The $\overline{CE}$ access time (t_{CE}) is equal to the address access time (t_{ACC}). The output enable ($\overline{OE}$) controls the output buffers. The output data is valid after a delay of t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DISABLE

When the $\overline{OE}$ input control is high, the outputs are placed in the high-impedance state.

STANDBY

The TC58F1000P / F / J has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC58F1000P / F / J is placed in the standby mode and the outputs are in the high impedance state, independent of the $\overline{OE}$ and $\overline{WE}$ inputs.

PROGRAM / PROGRAM-VERIFY / ERASE / ERASE-VERIFY / SIGNATURE READ

The TC58F1000P / F / J features a command control mode and an EPROM compatible mode. The command control mode is used to enable the program, program-verify, chip-erase, block erase, erase-verify, signature read and reset operations and the EPROM compatible mode controls the program, program-verify, chip erase and signature read operations.

1. COMMAND CONTROL MODE

The command code must be entered into the TC58F1000P / F / J before performing program, program-verify, erase (chip-erase and block-erase operations), erase-verify, signature read, reset operations.

The command control is a useful software protection method to protect from inadvertent operation. The command control mode is enabled when a high voltage (12V) is applied V_{PP}.

TC58F1000P / F / J has an internal command register circuit and the operation mode is defined by the command codes. The specific addresses and data presented to the TC58F1000P / F / J are latched in the command registers and the operation mode is defined. Address and data code are latched by the $\overline{WE}$ signal. The address is latched at the falling edge of $\overline{WE}$, and the data is latched at the rising edge of $\overline{WE}$.

1) PROGRAM OPERATION

The program operation is setup by the first 3 steps of command codes and performed during the 4th step by providing the address and data to be programmed.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
3	Write	5555(H) : A0~14	A0(H)
4	Write	Address : A0~16	Data-in

2) PROGRAM-VERIFY OPERATION

The program-verify operation is setup by the first 3 steps of command codes and performed during the 4th step. The program-verify address is a don't care because the address is latched during the program operation. Between the 3rd and 4th bus cycles a 2μs (minimum) program recovery delay is required.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
3	Write	5555(H) : A0~14	B0(H)
4	Read	Don't Care	Data-out

Note: *The addresses which are not defined in the table are "don't care."

3) ERASE OPERATION

The chip erase operation is setup and performed after 6 steps of command codes. The block erase operation is setup by 6 steps of command codes and performed after the 7th step by giving the first address of each block.

The command codes are as follows.

a) Chip erase operation

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
3	Write	5555(H) : A0~14	80(H)
4	Write	5555(H) : A0~14	AA(H)
5	Write	2AAA(H): A0~14	55(H)
6	Write	5555(H) : A0~14	10(H)

b) Block erase operation

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
3	Write	5555(H) : A0~14	60(H)
4	Write	5555(H) : A0~14	AA(H)
5	Write	2AAA(H): A0~14	55(H)
6	Write	5555(H) : A0~14	20(H)
7	Write	Block Add.: A12~16	Don't Care

Note : * The addresses which are not defined in the table are "don't care".

4) ERASE-VERIFY OPERATION

The erase-verify operation is setup by 3 steps of command codes and performed by presenting the erase-verify address during the 4th step. By providing the next erase-verify address during subsequent steps, additional erase verify operations can be performed. Between the 3rd and 4th steps a 500μs (minimum) erase recovery time required.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H) : A0~14	55(H)
3	Write	5555(H) : A0~14	D0(H)
4	Read	Address : A0~16	Data-out

5) SIGNATURE READ OPERATION

The signature-read operation is setup by 3 steps of command codes and by providing address 00000(H) to read the manufacturers code and address 00001(H) to read the device code during the 4th or 5th steps.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H) : A0~14	55(H)
3	Write	5555(H) : A0~14	90(H)
4	Read	0 : A0~16	Manufacturer's Code
5	Read	1 : A0~16	Device Code

Note : * The addresses which are not defined in the table are "don't care".

6) RESET

Each operation mode is cleared by the reset command and the operation mode returns to the initial state which is the read mode. The reset operation is performed by 3 steps of command codes.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
3	Write	5555(H) : A0~14	F0(H)

Note : * The addresses which are not defined in the table are "don't care".

<Command Control Code Table>

		Command Step						
		1	2	3	4	5	6	7
Program	Mode	Write	Write	Write	Write			
	Address	5555 (A0 - 14)	2AAA (A0 - 14)	5555 (A0 - 14)	Program Add. (A0 - 16)			
	D0~7	AA	55	A0	Data in			
Program - Verify	Mode	Write	Write	Write	Read			
	Address	5555 (A0 - 14)	2AAA (A0 - 14)	5555 (A0 - 14)	Don't care			
	D0~7	AA	55	B0	Data out			
Signature Read	Mode	Write	Write	Write	Read	Read		
	Address	5555 (A0 - 14)	2AAA (A0 - 14)	5555 (A0 - 14)	00000 (A0 - 16)	00001 (A0 - 16)		
	D0~7	AA	55	90	Manu - facturer's code	Device code		

		Command Step						
		1	2	3	4	5	6	7
Chip Erase	Mode	Write	Write	Write	Write	Write	Write	
	Address	5555 (A0 - 14)	2AAA (A0 - 14)	5555 (A0 - 14)	5555 (A0.- 14)	2AAA (A0 - 14)	5555 (A0 - 14)	
	D0~7	AA	55	80	AA	55	10	
Block Erase	Mode	Write	Write	Write	Write	Write	Write	Write
	Address	5555 (A0 - 14)	2AAA (A0 - 14)	5555 (A0 - 14)	5555 (A0 - 14)	2AAA (A0 - 14)	5555 (A0 - 14)	Block Add. (A12 - 16)
	D0~7	AA	55	60	AA	55	20	Don't care
Erase - Verify	Mode	Write	Write	Write	Read			
	Address	5555 (A0 - 14)	2AAA (A0 - 14)	5555 (A0 - 14)	Verify Add. (A0 - 16)			
	D0~7	AA	55	D0	Data out			
Reset	Mode	Write	Write	Write				
	Address	5555 (A0 - 14)	2AAA (A0 - 14)	5555 (A0 - 14)				
	D0~7	AA	55	F0				

Note: *The addresses which are not defined in the table are "don't care."

BLOCK ERASE MODE

<Block Address Table>

Block No.	Addresss Area	Hex Adresss	A16	A15	A14	A13	A12	A11~A0
1	00000~00FFF	00XXX	0	0	0	0	0	Don't Care
2	01000~01FFF	01XXX	0	0	0	0	1	Don't Care
3	02000~02FFF	02XXX	0	0	0	1	0	Don't Care
4	03000~03FFF	03XXX	0	0	0	1	1	Don't Care
5	04000~04FFF	04XXX	0	0	1	0	0	Don't Care
6	05000~05FFF	05XXX	0	0	1	0	1	Don't Care
7	06000~06FFF	06XXX	0	0	1	1	0	Don't Care
8	07000~07FFF	07XXX	0	0	1	1	1	Don't Care
9	08000~08FFF	08XXX	0	1	0	0	0	Don't Care
10	09000~09FFF	09XXX	0	1	0	0	1	Don't Care
11	0A000~0AFFF	0AXXX	0	1	0	1	0	Don't Care
12	0B000~0BFFF	0BXXX	0	1	0	1	1	Don't Care
13	0C000~0CFFF	0CXXX	0	1	1	0	0	Don't Care
14	0D000~0DFFF	0DXXX	0	1	1	0	1	Don't Care
15	0E000~0EFFF	0EXXX	0	1	1	1	0	Don't Care
16	0F000~0FFFF	0FXXX	0	1	1	1	1	Don't Care
17	10000~10FFF	10XXX	1	0	0	0	0	Don't Care
18	11000~11FFF	11XXX	1	0	0	0	1	Don't Care
19	12000~12FFF	12XXX	1	0	0	1	0	Don't Care
20	13000~13FFF	13XXX	1	0	0	1	1	Don't Care
21	14000~14FFF	14XXX	1	0	1	0	0	Don't Care
22	15000~15FFF	15XXX	1	0	1	0	1	Don't Care
23	16000~16FFF	16XXX	1	0	1	1	0	Don't Care
24	17000~17FFF	17XXX	1	0	1	1	1	Don't Care
25	18000~18FFF	18XXX	1	1	0	0	0	Don't Care
26	19000~19FFF	19XXX	1	1	0	0	1	Don't Care
27	1A000~1AFFF	1AXXX	1	1	0	1	0	Don't Care
28	1B000~1BFFF	1BXXX	1	1	0	1	1	Don't Care
29	1C000~1CFFF	1CXXX	1	1	1	0	0	Don't Care
30	1D000~1DFFF	1DXXX	1	1	1	0	1	Don't Care
31	1E000~1EFFF	1EXXX	1	1	1	1	0	Don't Care
32	1F000~1FFFF	1FXXX	1	1	1	1	1	Don't Care

2. EPROM COMPATIBLE MODE

This mode is the same as used for Toshiba's 256K FE²PROM, the TC58257A. When a high-voltage (12V) is applied to the $\overline{WE}$ pin of the TC58F1000P/F/J, the program and erase operations are enabled and can be performed by any conventional EPROM programmer.

(1) PROGRAM OPERATION

TC58F1000P/F/J is placed in the programming mode by applying a high voltage (12V) to the V_{PP} and $\overline{WE}$ pins. During the programming cycle the addresses and input data must be held valid, the $\overline{OE}$ signal must be held high and the $\overline{CE}$ input must be clocked. The programming is controlled by the $\overline{CE}$ input timing.

(2) PROGRAM-VERIFY OPERATION

The programmed data is verified with the V_{PP} and $\overline{WE}$ pins held at high voltage (12V) level and with $\overline{OE}$ held at V_{IL}.

(3) CHIP ERASE OPERATION

TC58F1000P/F/J is placed in the chip erase mode by applying a high voltage (12V) to the V_{PP}, $\overline{WE}$ and A9 pins. During the chip erase cycle, addresses A0~A8 and A10~A16 are "don't care", $\overline{OE}$ must be held high and $\overline{CE}$ must be clocked.

(4) ELECTRIC SIGNATURE READ

With V_{PP} held at a voltage between 0 and V_{CC}, $\overline{WE}$ held at VIH and by applying a high voltage (12V) to the A9 address input, the manufacturer's code can be read by specifying address 00000(H) and the device code can be read by specifying address 00001(H). Toshiba's manufacturer code and the TC58F1000P/F/J device code are shown in the table below.

TC58F1000P/F/J

Signature	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Manufacturer's Code	0	1	0	0	1	1	0	0	0	98
Device Code	1	0	0	1	0	0	1	1	0	26

APPLICATIONS

Toshiba's TC58F1000P / F / J Flash-EEPROM offers a cost-competitive and reliable alternative for applications which have traditionally employed the U.V. EPROM or O.T. PROM.

The Flash-EEPROM adds electrical erasure capability and eliminates the time consuming and labor intensive process of U.V. light exposure for erasing EPROMS. Furthermore, the Flash-EEPROM is electrically reprogrammable and thus eliminates the one-time programmable limitation of the O.T. PROM.

The TC58F1000P / F / J is offered in plastic DIP and surface mount packages (SOP and SOJ) which can be processed through the automated assembly line process. The electrically programmable and erasable features of the Flash-EEPROM eliminate the need for sockets both at the prototype stage and at the production stage. The major application advantages offered by the Flash-EEPROM in system design are listed below.

In-System Programming

The TC58F1000P / F / J is provided with a command control mode which makes it possible to program and erase data by using the system MPU timing. The TC58F1000P / F / J can be used for updating the system operating code or data in the system through a telecommunication line or a floppy disk interface. In this case, a 12V power supply must be available in the system.

On-Board Programming with an External Programmer

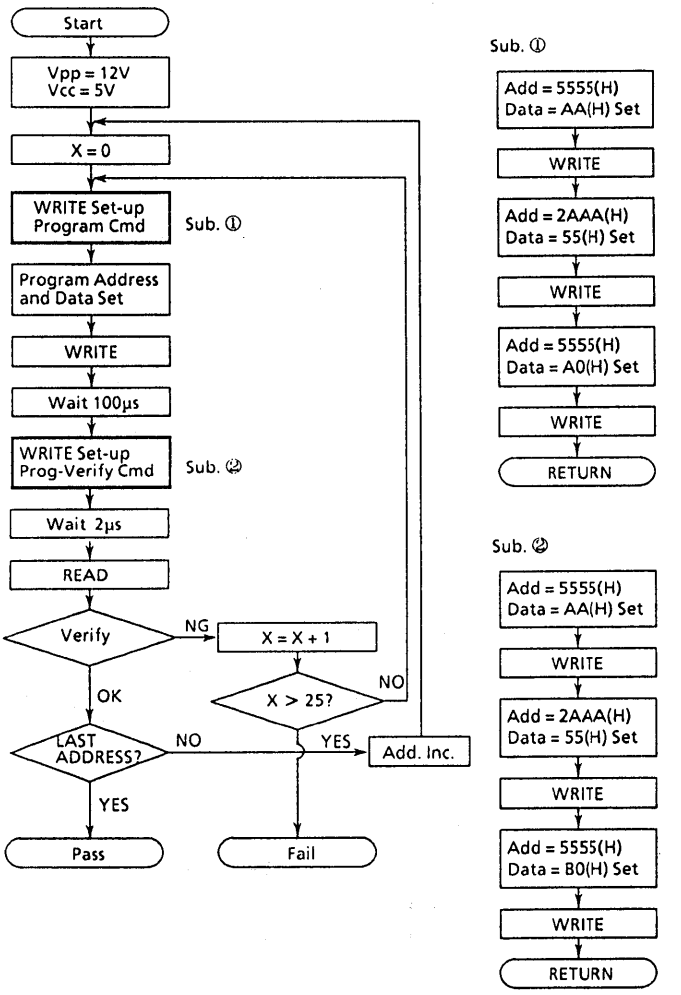
The TC58F1000P / F / J can be mounted directly onto the system board and all subsequent program and erase operations can be handled by an external PROM programmer through a connector. Since the TC58F1000P / F / J supports an EPROM compatible programming mode, a conventional PROM programmer can be used for this operation.

Card and Cartridge Applications

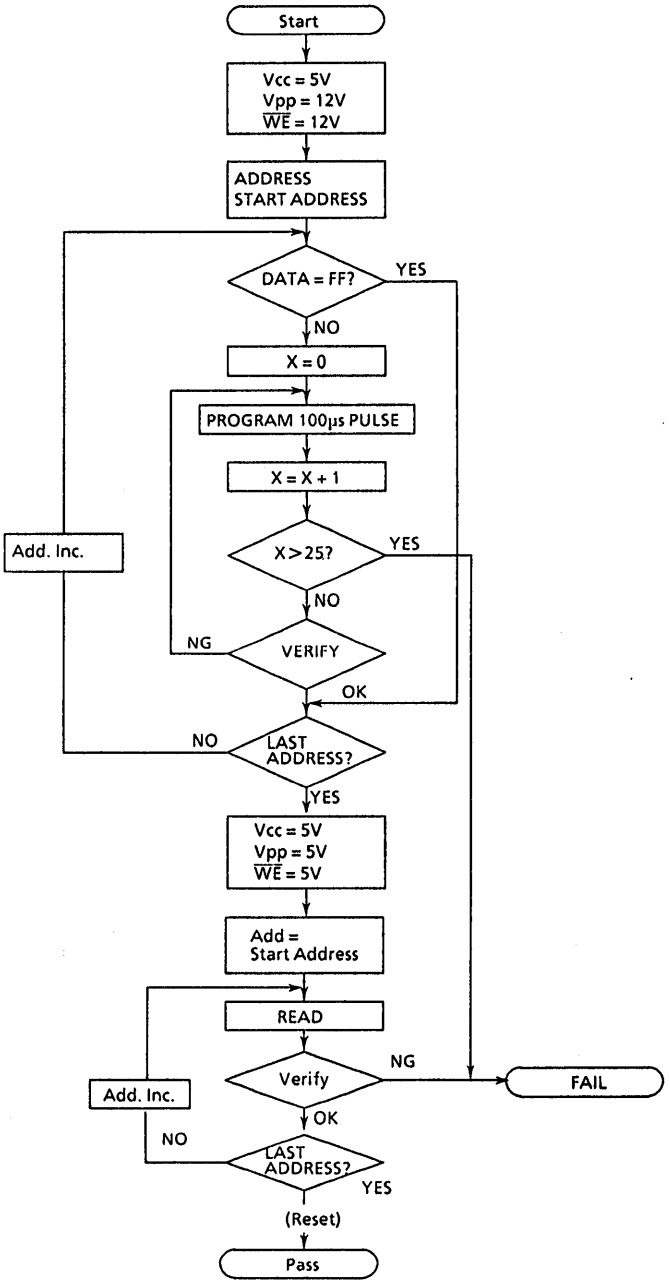
High density non-volatile memory cards and cartridges can be assembled using the SOP or SOJ surface mount version of Toshiba's TC58F1000. These cards and cartridges can be erased and reprogrammed using either the in-system programming method or an external programmer.

Program Flow Chart

① Command Control mode



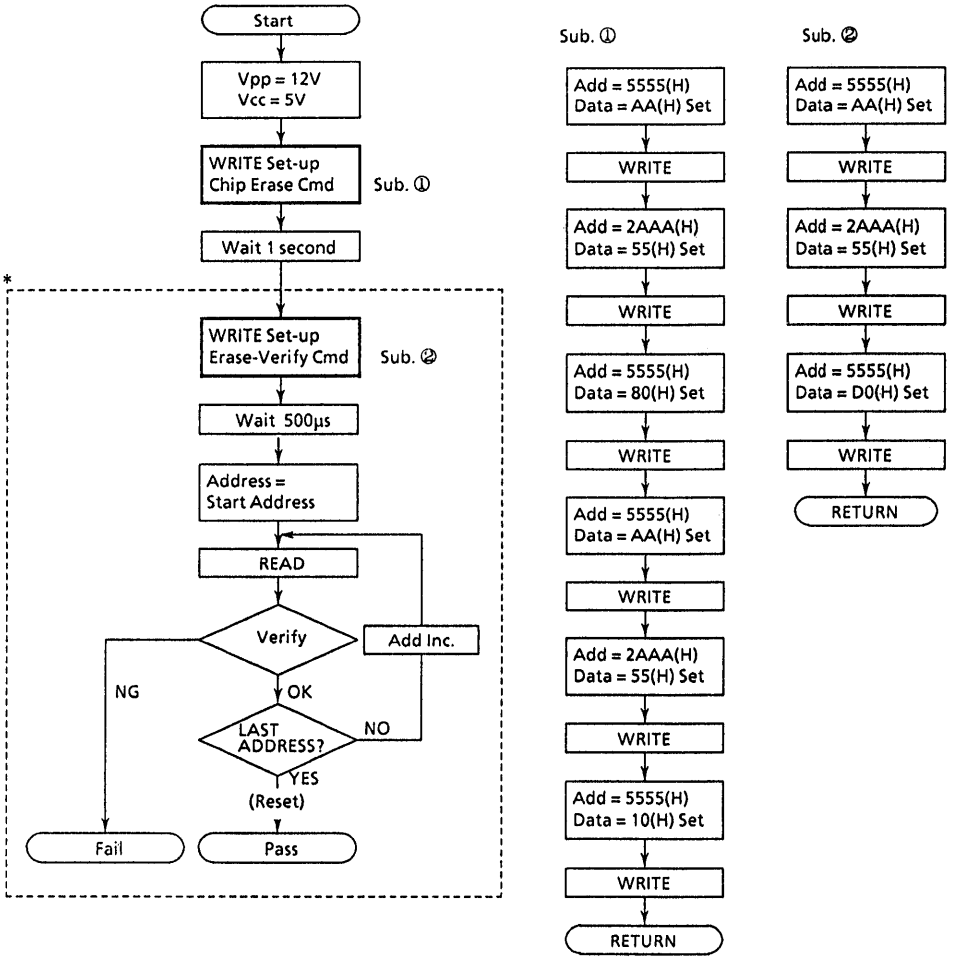
② EPROM Compatible mode



Electrical Erase Flow Chart

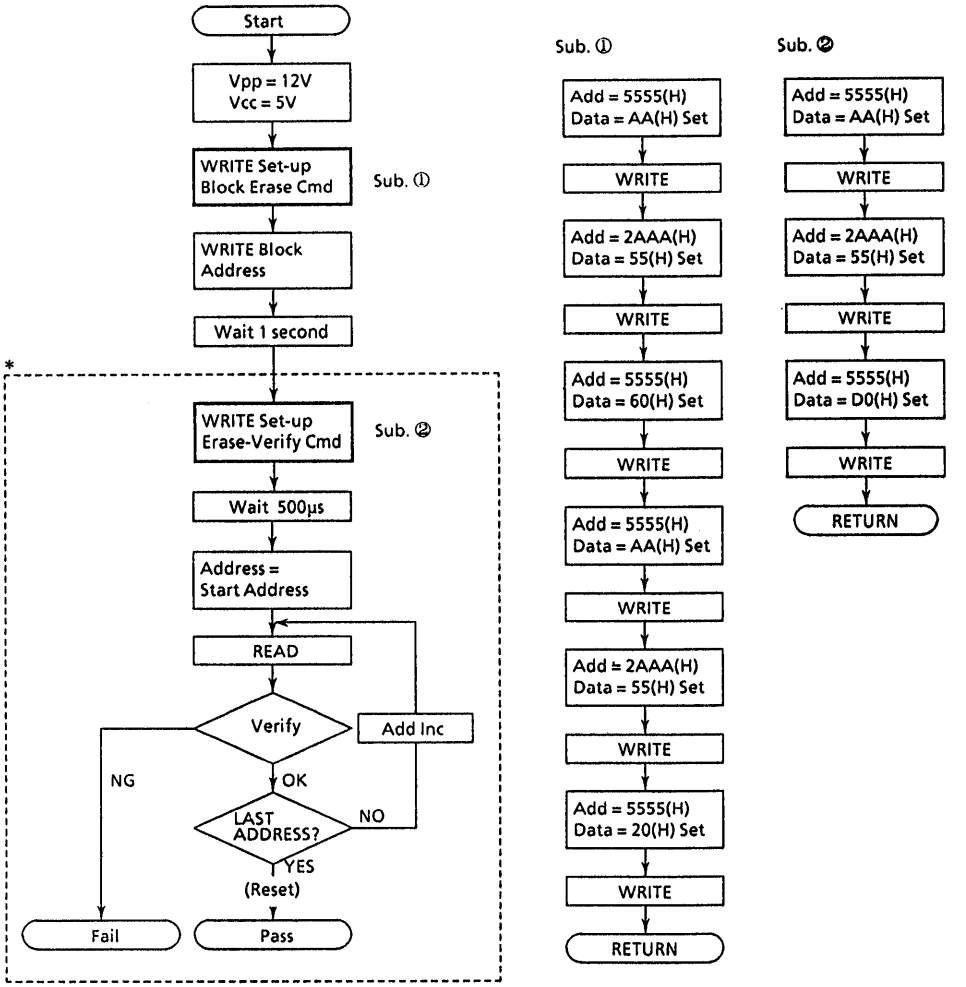
① Command Control mode

1) Chip Erase mode



Note : * : This part is an erase verify sequence part.
It is helpful to verify the amount of erasing.

2) Block Erase mode



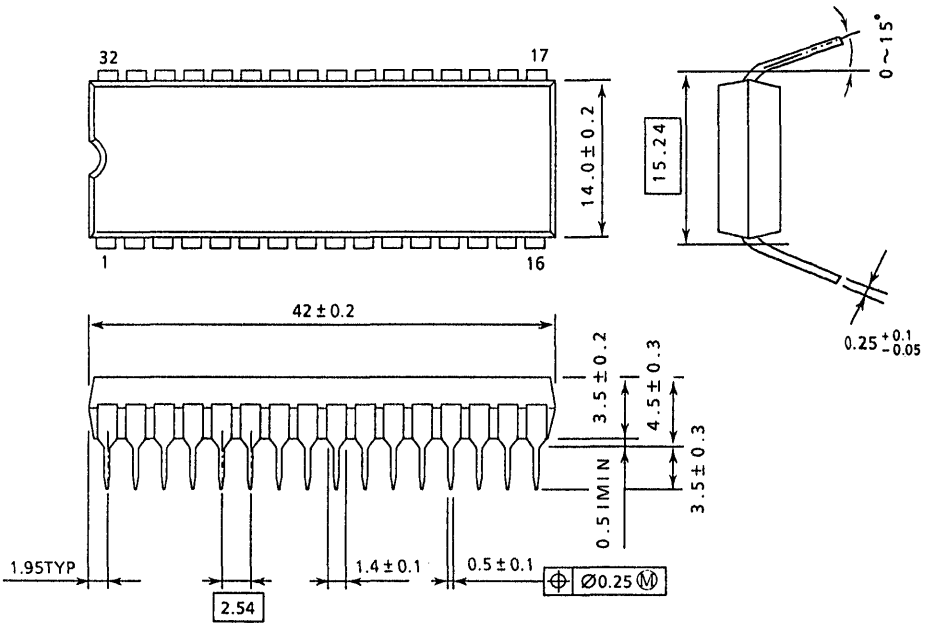
Note : * : This part is an erase verify sequence part.
It is helpful to verify the amount of erasing.

OUTLINE DRAWINGS

- Plastic DIP

DIP32-P-600

UNIT : mm

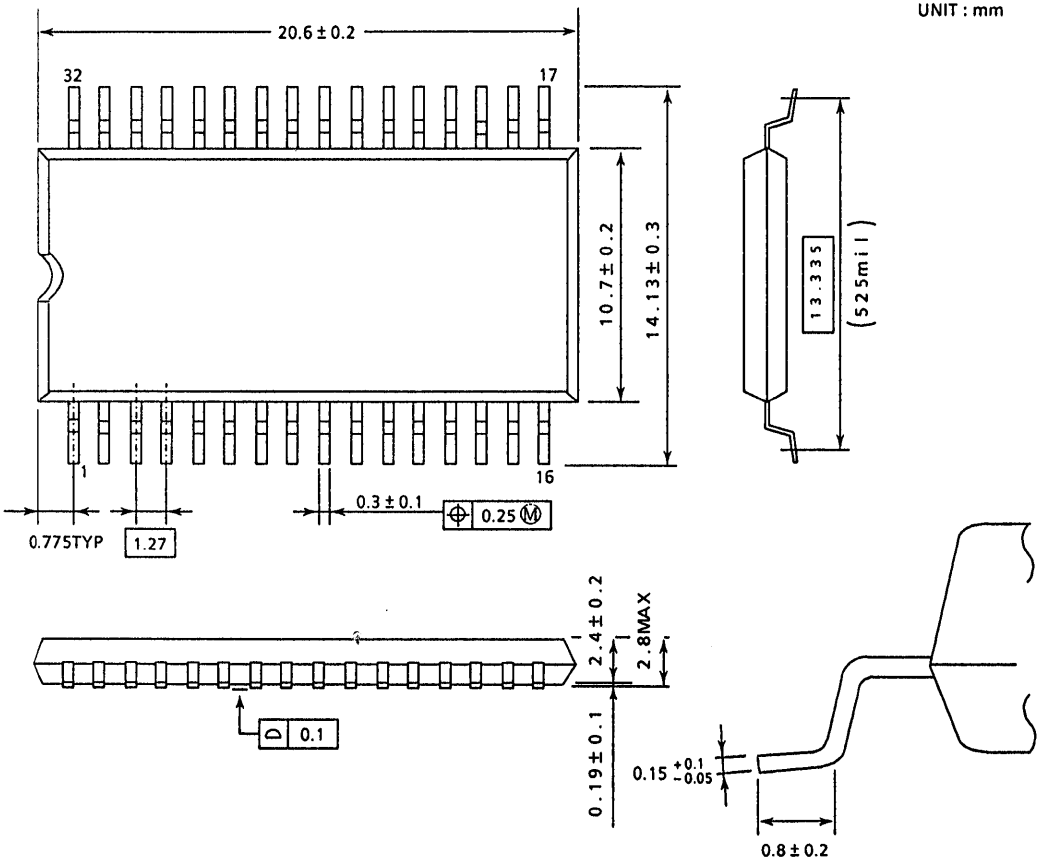


OUTLINE DRAWINGS

• Plastic SOP

SOP32–P–525

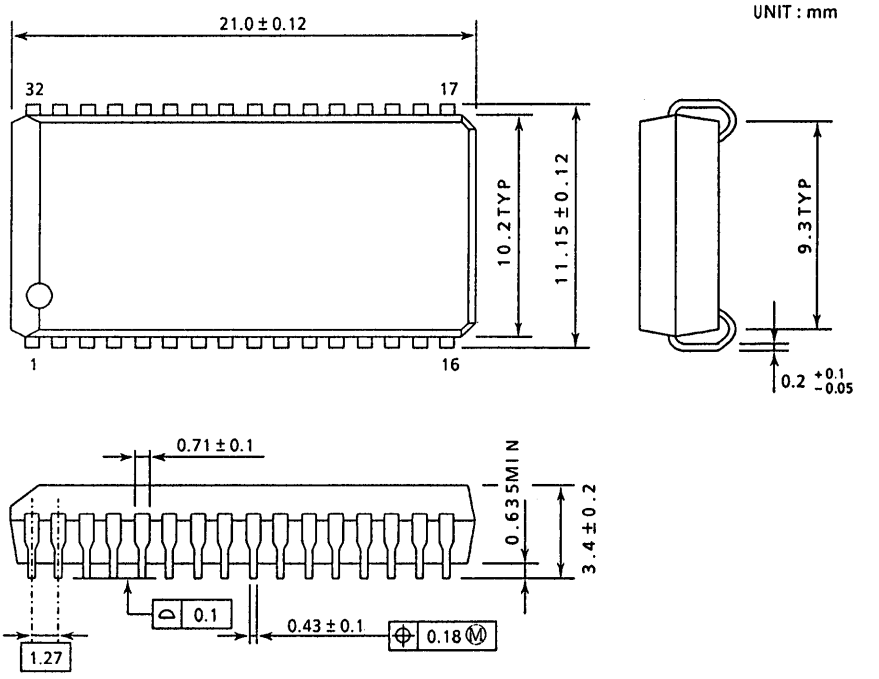
UNIT : mm



OUTLINE DRAWINGS

- Plastic SOJ

SOJ32–P–400



TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

REGIONAL SALES OFFICES

NORTHWEST REGION
1220 Midas Way
Sunnyvale, CA 94086
TEL: (408) 737-9844
FAX: (408) 737-9905

SOUTHWEST REGION
15621 Redhill Ave.
Suite 205
Tustin, CA 92680
TEL: (714) 259-0368
FAX: (714) 259-9439

CENTRAL REGION
One Parkway North
Suite 500
Deerfield, IL 60015-2547
TEL: (708) 945-1500
FAX: (708) 945-1044
TWX: 29-7131

SOUTHCENTRAL REGION
777 E. Campbell Road
Suite 650
Richardson, TX 75081
TEL: (214) 480-0470
FAX: (214) 235-4114

EASTERN REGION
25 Mall Road
5th Floor
Burlington, MA 01803
TEL: (617) 272-4352
FAX: (617) 272-3089
TWX: 710-321-6730

SOUTHEAST REGION
Waterford Centre
5555 Triangle Parkway
Suite 300
Norcross, GA 30092
TEL: (404) 368-0203
FAX: (404) 368-0075

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