32-Bit TX System RISC

Family



The **TX19** Family of RISC microprocessors for embedded-system use is derived from the **TX39** Family that was developed by Toshiba based on the R3000A architecture designed by the MIPS Group in the U.S.A. The **TX19** Family features the MIPS16™ ASE (Application-Specific Extension), a highly efficient instruction set from the MIPS Group. The result is a new Toshiba 32-bit RISC processor family.

Future development of the **TX19** Family will focus on products built around the **TX19** processor core; peripheral functions will be incorporated. The **TX19** processor core will also be made available as a CPU core for ASIC (application-specific IC) microcomputers. Hence, the **TX19** Family will offer you the resources necessary to create a system using a single chip.

High-performance RISC technology

- R3000A architecture
- TX19/L processing performance: 42 MIPS

(when operating at 40 MHz) (Dhrystone 2.1)

- Non-blocking load function
 - If the instruction following the load instruction does not use the result of the load operation, execution continues without a pipeline stall.
- DSP function

A 32-bit multiplier accumulator (MAC) operation takes only 1 clock cycles to execute.

Low power consumption

- Design optimized using low power consumption libraries
- Low power consumption modes

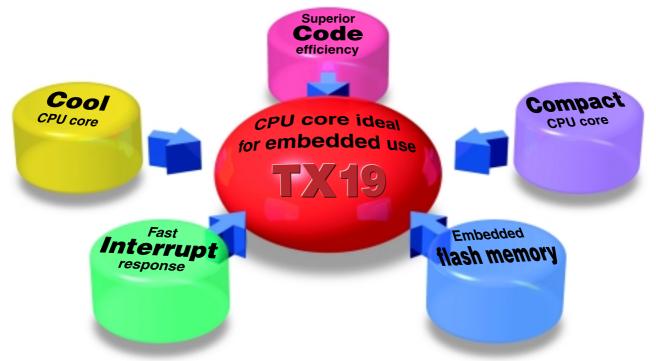
Clock gear Dual clock Various standby modes

Functions suitable for embedded applications

- Ocde size reduction based on 16-bit codes Object code-compatible with MIPS16™ ASE
- Increased real-time capability
 Faster interrupt response: 8x conventional (Toshiba) speed

Useful as CPU core for gate arrays/cell-based ICs

- TC240 process technology
- Compact core
- Complete development environment



Core simultaneously realizes low power consumption and high performance.

- Low power consumption
 - Design optimized for low power consumption
 - Clock gear
 - Standby modes
- Low operating voltage
 - 2.7-V operation possible

Twin 16-/32-bit instruction sets improve code efficiency and computing performance.

- Better computing performance
 32-bit instruction codes
 Object code-compatible with TX39
- Support for multiply/add operations and coprocessor instructions
- 16-bit instruction codes

 Increased code efficiency
 Support for PC-relative instructions

■ Main applications

- Portable devices: PCI, personal organizers, digital cellular 'phones
- PC peripherals: HDDs, DVD-ROM drives, printers
- Home electronics: DVD players, DVCs, DSCs



■ Superior code efficiency

- 16-bit ISA* Mode compatible with MIPS16[™]ASE

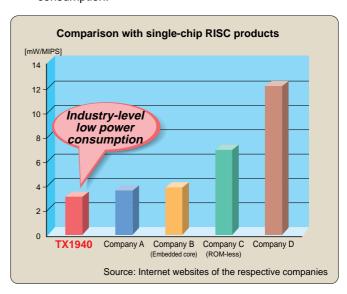
 object code level provides high code efficiency.
- Code size can be reduced by about 30% compared to 32-bit ISA Mode.

* ISA: instruction set architecture

O.7 32-bit ISA 16-bit ISA

■ Superior performance with minimal power consumption

An optimized design based on a low power consumption library results in high performance with low power consumption.





TX19 Series single-chip microcomputers with built-in ROM/RAM

TMP1940CYAF*/FDAF*



■ 32-bit single-chip RISC microprocessors for real-time control

The **TMP1940CYAF/FDAF** are 32-bit RISC microprocessors built around the **TX19/L** processor core with built-in fast ROM/RAM. They incorporate peripherals such as a DMA controller, timers, a serial interface and an AD converter. Offering characteristically low voltage and low power consumption, these devices are ideal for battery-driven applications such as portable information equipment for personal use.

Internal ROM

TMP1940CYAF: mask ROM, 256 Kbytes **TMP1940FDAF**: flash E²PROM, 512 Kbytes

Internal RAM

TMP1940CYAF: 10 Kbytes TMP1940FDAF: 16 Kbytes

DMA controller: 4 channels
 Memory-to-memory transfer, memory-to-I/O transfer

Interrupt controller: 12 external sources

MAC: 1 clock cycle execution (on 32-bit operands)

• 16-bit timer/counter: 4 channels

• 8-bit timer/counter: 4 channels

Timer

Serial interface
 UART/SIO: 4 channels
 I²C bus / SIO: 1 channel

10-bit AD converter: 8 channels

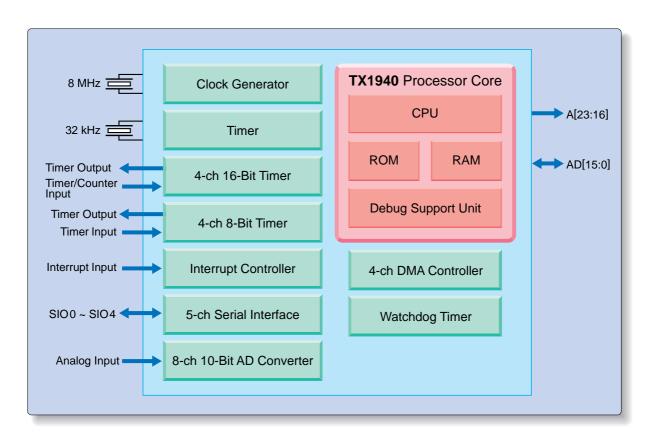
Watchdog timer

Maximum operating frequency: 32 MHz

Supply voltage: 2.7 V to 3.6 V

100-pin miniflat package

(14 X 20 mm, 0.5 mm pitch, 1.4 mm thick)





Purchase of Toshiba I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

32-Bit TX System RISC

Family



The **TX39** Family of embedded-use RISC microprocessors was developed by Toshiba based on the R3000A architecture designed by the MIPS Group, a division of Silicon Graphics, Inc. It is an original Toshiba 32-bit processor family. Using the **TX39** or the high-speed **TX39/H** and **TX39/H2** as the CPU core for gate arrays and cell-based ICs, you can accomplish greater integration in your system.

High-performance RISC technology

- R3000A architecture
- TX39/H processing performance: 74 MIPS

(when operating at 70 MHz)

TX39 processing performance: 52 MIPS

(when operating at 50 MHz) (Dhrystone 2.1)

- Built-in cache memory
- Non-blocking load function

The instructions which follow the instruction currently being executed are executed while the cache is being refilled.

DSP function

A 32-bit multiplier accumulator (MAC) operation takes only 1 clock cycle to execute.

Low power consumption

- Low power consumption modes
- Clock stop function

Functions suitable for embedded applications

- Reduced code size and improved performance
 Use of branch-likely instructions
 Hardware interlock function
- Increased real-time capability Cache lock function
- Real-time debugger system connection
 Real-time debugging is possible while cache is on.

Useful as CPU core for gate arrays / cell-based ICs

- TX39/H2: TC240 process technology
- TX39/H: TC220 process technology
- OTX39: TC200 process technology
- Complete development environment

NEW PRODUCIS

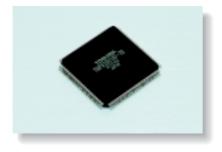
General-purpose MPU

TMPR3901AF-70

■ 32-bit general-purpose RISC microprocessor based on the TX39/H core

The **TMPR3901AF** is built around the **TX39/H** high-speed core and incorporates peripheral circuits such as a clock generator and a write buffer.

As well as being used as a general-purpose MPU, this microprocessor can also be used to evaluate performance or create function prototypes when ASICs using the **TX39/H** core are being developed.



- Instruction cache: 4 Kbytes built in
- Data cache: 1 Kbyte built in
- Clock generator with x8 PLL
- 4-stage write buffer
- Half-Speed Bus Mode

System bus frequency is halved.

- Low power consumption modes
 Doze/Halt Modes to reduce power consumption when idle
 RF function to reduce operating frequency
- Built-in debug support unit
- Maximum operating frequency: 70 MHz
- Supply voltage: 3.3 V
- Package: 160-pin QFP

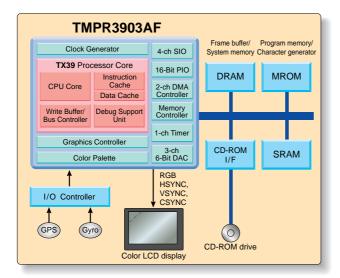
NEW PRODUCIS

Suitable for car navigation

TMPR3903AF

■ 32-bit RISC microprocessor with graphics controller

The **TMPR3903AF** is a 32-bit RISC microprocessor, incorporating graphics control and other functions suitable for car navigation systems, portable information terminals and other systems which require color displays. In addition, this microprocessor contains a memory controller, DMA controller, SIO, PIO and other peripheral circuits all encapsulated in a 208-pin QFP package.



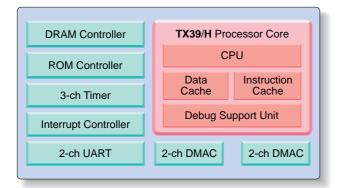
- Instruction cache: 4 Kbytes built in
- Data cache: 1 Kbyte built in
- MAC: 1 clock cycle execution (on 32-bit operandes)
- Clock generator with x4 PLL
- 4-stage write buffer
- Half-Speed Mode
 System bus frequency is halved.
- Built-in debug support unit
- Graphics control functions
 - Frame buffer configured using DRAM
 - Fast Page Mode / Hyper Page Mode
 - 4-plane superimposition performed by hardware
 - Display synchronization signals HSYNC, VSYNC and CSYNC are generated.
 - Built-in color palette and 3-ch video DAC
- DMA controller: 2 channels
- Interrupt controller: 3 external sources
- SIO: 4 channels: PIO: 16 bits
- Timer (free-running counter)
- Maximum operating frequency: 50 MHz
- Operating temperature range: -40° to 85°C
- Supply voltage: 3.3 V
- Package: 208-pin QFP

General-purpose MPU

TMPR3904AF-66

■ 32-bit general-purpose RISC microprocessors with peripheral functions

The **TMPR3904AF** is a 32-bit RISC microprocessor built around the **TX39/H** high-speed processor core and incorporating peripheral circuits such as a memory controller, DMA controller, UART and timer – all highly suitable for general-purpose use.



- Instruction cache: 4 Kbytes built in
- Data cache: 1 Kbyte built in
- MAC: 1 clock cycle execution (on 32-bit operandes)
- ROM controller: 16-bit bus width can also be set.
 Page Mode Read supported
- DRAM controller: 16-bit bus width can also be set.
 Fast Page Mode, Hyper Page Mode
- DMA controller: 4 channels
 Memory-to-memory transfer, memory-to-I/O transfer
- Interrupt controller: 8 external sources
- Timer: 3 channels
- UART: 2 channels
- PIO: 8 bits X 3 ports
- Maximum operating frequency: 66 MHz
- Supply voltage: 3.3 V
- Package: 208-pin QFP



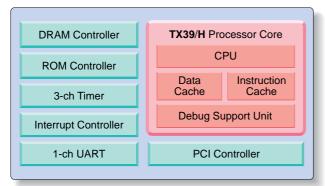
Built-in PCI controller

TMPR3907F

■ 32-bit RISC microprocessor with PCI controller

The **TMPR3907F** is a 32-bit RISC microprocessor built around the **TX39/H** processor core. It incorporates a PCI controller and other peripheral circuits such as a memory controller, UART and timer.

Using the **TX39/H** high-speed core, this microprocessor operates at 66 MHz, with the PCI bus operating at 33 MHz.



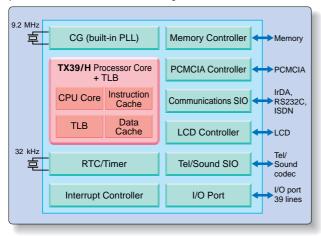
- Instruction cache: 4 Kbytes built in
- Data cache: 1 Kbyte built in
- MAC: 1 clock cycle execution (on 32-bit operands)
- PCI controller: 3 slots supported
- ROM controller: interleaved operation also possible
- DRAM controller
- Interrupt controller: 3 external sources
- Timer: 3 channels
- UART: 1 channel
- Maximum operating frequency: 66 MHz
- Supply voltage: 3.3 VPackage: 208-pin QFP

Suitable for Windows® CE

TMPR3912

■ 32-bit RISC microprocessor with peripheral functions for portable information equipment

The **TMPR3912** is an application-specific standard product (ASSP) built around the **TX39/H** processor core and incorporating the peripheral functions required for portable information communicators (PICs) on a single chip. In addition, this microprocessor has an enhanced power management function, making it ideal for PICs. All told, the **TMPR3912** helps you minimize the size, reduce the cost, and increase the functionality of your portable information terminal system.



- Instruction cache: 4 Kbytes built in
- Data cache: 1 Kbyte built in
- MAC: 1 clock cycle execution (on 32-bit operands)
- Memory management unit (TLB):

32-entry, 4-Kbyte pages

- Memory controller: supports SDRAM, DRAM (EDO), SRAM, ROM and flash memory.
- Communications interface: supports CHI/UART/IrDA/SPI.
- PCMCIA interface
- LCD interface: supports monochrome and color.
 1024 X 1024 pixels maximum
- Timer: 2 channels (RTC and/or watchdog timer)
- I/O port: 39 bits
- Low power consumption modes: Doze/Sleep
- Maximum operating frequency: 75 MHz / 92 MHz
- Supply voltage: 3.3 V
- Package: 208-pin LQFP (1.4 mm thick)
 217-pin FBGA (1.4 mm thick)

TMPR3912AU: LQFP, 75-MHz version TMPR3912XB-75: FBGA, 75-MHz version TMPR3912AU-92: LQFP, 92-MHz version TMPR3912XB-92: FBGA, 92-MHz version



Suitable for Windows® CE

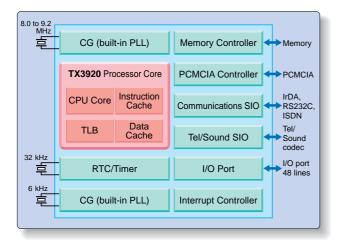
NEW

TMPR3922

■ 32-bit RISC microprocessor with peripheral functions for high performance

The **TMPR3922** is an application-specific standard product (ASSP) built around the **TX3920** processor core and incorporating the peripheral functions required for portable information communicators (PICs) on a single chip. In addition, this microprocessor has an enhanced power management function, making it ideal for PICs. Therefore, the **TMPR3922** helps you minimize the size,

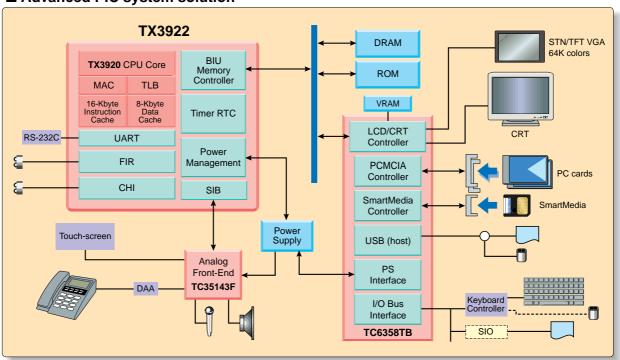
Therefore, the **TMPR3922** helps you minimize the size, reduce the cost, and increase the functionality of your portable information terminal system or multimedia device.



- Instruction cache: 16 Kbytes built in (2-way set-associative)
- Data cache: 8 Kbytes built in (2-way set-associative)
- MAC: 1 clock cycle execution (on 32-bit operands)
- Memory management unit (TLB): 64-entry
 4-K/16-K/64-K/256-K/1-M/4-Mbyte pages
- Memory controller: supports SDRAM, DRAM (EDO), SRAM, ROM and flash memory.
- Communications interface: supports CHI/UART/IrDA/SPI.
- PCMCIA interface
- Timer: 2 channels, watchdog timer
- RTC
- I/O port: 48 pins
- Low power consumption modes: Doze / Sleep
- Maximum operating frequency: 129 MHz / 148 MHz
- I/O supply voltage: 3.3 V
- Internal supply voltage: 2.7 V
- Package: 208-pin LQFP (1.4 mm thick)
 217-pin FBGA (1.4 mm thick)

TMPR3922AU: LQFP, 129-MHz version TMPR3922XB: FBGA, 129-MHz version TMPR3922CU: LQFP, 148-MHz version TMPR3922XB-148: FBGA, 148-MHz version

■ Advanced PIC system solution



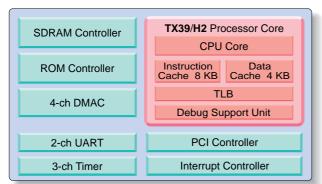


Built-in PCI controller TMPR3927F* *Under development

■ 32-bit RISC microprocessor with PCI controller

The **TMPR3927F** is a 32-bit RISC microprocessor built around the **TX39/H2** processor core. It incorporates a PCI controller and other peripheral circuits such as a memory controller, UART and timer.

Using the **TX39/H2** high-speed core, this microprocessor operates at 133 MHz, with the PCI bus operating at 33 MHz.

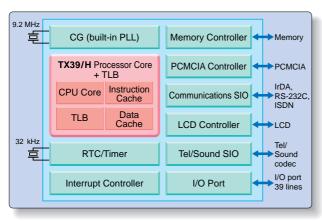


- Instruction cache: 8 Kbytes 2-way built in
- Data cache: 4 Kbyte 2-way built in
- MAC: 1 clock cycle execution (on 32-bit operands)
- Memory management unit (TLB): 64-entry4-K/16-K/64-K/256-K/1-M/4-Mbyte pages
- Memory controller: supports SDRAM, SGRAM, SMROM, SRAM, ROM and flash memory.
- Interrupt controller: 6 external sources
- Timer: 3 channels
- UART: 2 channels
- PCI controller: 4 slots supported
- DMA controller: 4 channels
- I/O ports: 16 pins
- Maximum operating frequency: 133 MHz
- I/O supply voltage: 3.3 V
- Internal supply voltage: 2.5 V
- Package: 240-pin PQFP (3.6 mm thick)

Suitable for PDA TMPR3911AU/XB* * Under development

■ 32-bit RISC microprocessor with peripheral functions for portable information equipment

The **TMPR3911AU/XB** are low power consumption version of **TMPR3912** based on the **TX39/H** processor core and incorporating the peripheral functions required for portable information communicators (PICs) on a single chip. In addition, this microprocessor has an enhanced power management function, making it ideal for PICs. Therefore, the **TMPR3911AU/XB** help you minimize the size, reduce the cost, and increase the functionality of your portable information terminal system.



- Instruction cache: 4 Kbytes built in
- Data cache: 1 Kbyte built in
- MAC: 1 clock cycle execution (on 32-bit operands)
- Memory management unit (TLB):

32-entry, 4-Kbyte pages

- Memory controller: supports SDRAM, DRAM (EDO), SRAM, ROM and flash memory.
- Communications interface: supports CHI/UART/IrDA/SPI.
- PCMCIA interface
- LCD interface: supports monochrome and color.
 1024 X 1024 pixels maximum
- Timer: 2 channels (RTC and/or watchdog timer)
- I/O port: 39 bits
- Low power consumption modes: Doze/Sleep
- Maximum operating frequency: 36.8 MHz
- Supply voltage: 3.3 V
- Package: 176-pin LQFP (1.4 mm thick)
 217-pin FBGA (1.4 mm thick)