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GATE ARRAY DESIGN MANUAL

VGC SERIES

GATE ARRAY DESIGN MANUAL

VGC Series CMOS Gate Array Design Manual

Version 4.0

CONTENTS

CHAPTER 1

INTRODUCTION

GENERAL INFORMATION

This manual provides the information necessary to prepare a design for implementation in any VTI VGC Series 2-micron CMOS gate array. VTI also offers classroom instruction covering this information. The VGC Series Design Manual consists of two parts:

- Part I (Chapters 1 - 9) contains the general information, design rules and procedures for design preparation prior to computer-aided design.
- Part II (Appendices) contains the VGC Series Macro Library, which includes the individual specifications for each available macro. The other appendices contain the VGC data sheets and an application note. Refer to Chapter 4 for a detailed description of macro specifications and their use.

Terminology

Unless otherwise noted, the terms "chip" and "array" in all descriptions and illustrations refer to the VGC gate array.

The VGC Series

Figure 1-1 presents a brief comparison of the main elements of each array in the VGC Series. Refer to the section, **Features**, for a more detailed description of the VGC Series features.

Additional Publications

Where applicable, this manual refers to the **VLSI Design System Reference Manual**, a reference guide to the VTI's Computer-Aided Design system.

	VGC0500	'0900	'1200	'1900	'2400	'3200	'4000	'6000	'8000
Internal Cells	360	576	792	1288	1728	2160	2640	4000	5264
Equiv. Gates (1)	540	864	1188	1932	2592	3240	3960	6000	7896
Pin Count:									
Input-only Cells	0	23	27	35	39	43	47	55	63
I/O Cells	40	38	46	58	70	78	86	106	118
Power Pins	4	4	8	8	8	8	8	8	16
Testability Pins	0	3	3	3	3	3	3	3	3
Total Pins	44	68	84	104	120	132	144	172	200

Note 1: An "equivalent gate" is one 2-input NAND gate.

Figure 1-1. VGC Series Summary

FEATURES

VGC Series gate arrays are fabricated with VTI's advanced 2-micron double-metal silicon gate CMOS technology. Each array consists of a mixture of functionally differentiated cell types (Internal, Input-only and I/O) and dedicated support structures such as power buses. The key features of the arrays are:

- 500 to 8000 equivalent gates
- True 2-micron Silicon Gate Geometries
- High Performance - 1.1 ns typical gate delay
  1.9 ns worst case gate delay (Commercial/Industrial)
  2.0 ns worst case gate delay (Military)
- High output drive - 8 mA for single-output buffer (10 mA for VGC0500)
- Low Power Dissipation - 20 microWatts/gate/MHz
- Individually Selectable CMOS or TTL Inputs
- Single 5 V Power Supply
- On-chip Testability Features (Except on the VGC0500)
- Wide Choice of Package Pin-counts and Styles
- CAD Support on VAX* and Apollo using VTI's proprietary design system
- CAD support on popular Daisy and Mentor engineering workstations

The transistors that make up the cells are diffused in standard patterns and interconnected using a combination of standard and special (user-selected) metal patterns. The standard metal patterns include power and ground buses, pads and the I/O cell control buses. The special metal patterns interconnect the transistors in one or more cells to form functional logic macros.

*VAX is a trademark of Digital equipment corp.

VTI'S ADVANCED CMOS TECHNOLOGY

VTI'S advanced CMOS technology is a 2-micron CMOS process; the circuits use true 2-micron design rules. The bulk CMOS process uses p-wells and all devices are ion implanted. Oxide isolation between devices is employed and interconnections are made by two layers of metal. The process uses plasma etching for all etching steps.

Figure 1-2 shows a typical cross section of the process. Both p- and n-channel transistors are shown with their associated conductors, through which the CMOS structure is formed. The p- and n-channel device areas and substrate contacts are defined by the selectively grown field oxide shown between and on the left- and right-hand sides of the devices.

A single layer of n+ doped polysilicon conductors provide the common gate electrode for both devices. This gate, as well as source and drain implants, are contacted by first-layer metal (metal 1), which in turn connects to second-layer metal (metal 2) through vias in the inter-metal (SiO2) insulator.

The key design rules of the process are:

- 2-micron polysilicon gate width
- 2.5-micron x 2.5-micron first contact
- 3-micron x 3-micron via
- 6-micron metal I pitch
- 7-micron metal II pitch

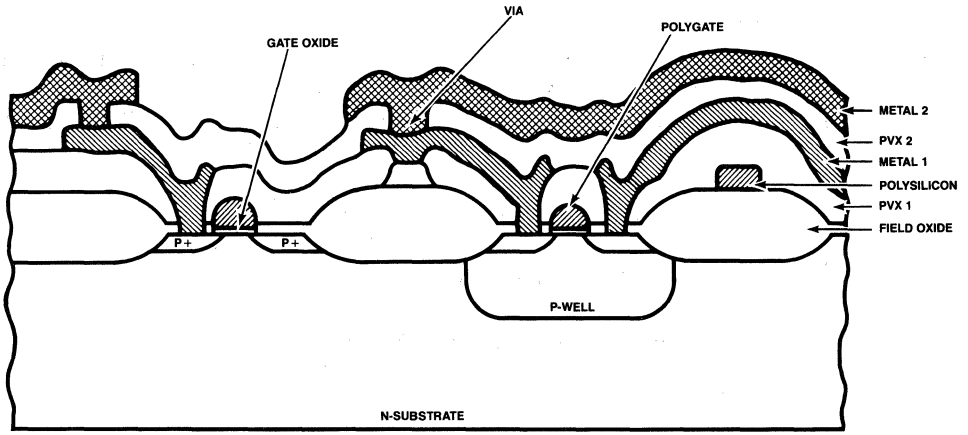


Figure 1-2. VTI Advanced CMOS Cross Section

DESIGNING A GATE ARRAY OPTION

A specific gate-array circuit design is called an "option". The option must first be defined in an objective specification, explained in the next section.

All aspects of option logic design, simulation, testing, placement, routing, checking and mask-tape generation are done on VTI's proprietary design system, which is described later in this chapter. Alternatively, logic design capture and simulation can be done on engineering workstations such as Daisy and Mentor. Gate array design kits for other engineering workstations will be available in the near future.

A brief description of fabrication and assembly is included in this chapter.

Objective Specification

The first step in designing an option is to establish an objective specification. This specification is the focal point of communication between the designer and VTI and will ultimately define the circuit to be produced. Chapter 6 provides information the gate array designer needs to prepare for the objective specification.

Computer Aided Design With VTI's Design System

VTI's design system is an interactive CAD system that combines gate array design functions in a single system. It performs schematic capture, logic and timing simulation, test vector grading, macro placement and routing. The same basic system is used for all VTI's gate arrays. The system runs on VAX 11/780 and Apollo computers at VTI, provides local and remote access and works in the following manner:

Logic Schematic Entry

Initially, a logic design may be entered through an interactive graphics system. The user selects and places symbols representing library macros and interconnects them using a graphics terminal. (The VGC Series macro library is summarized in Chapter 4). The designer may also specify logic design by entering a netlist through an alphanumeric terminal.

Logic Simulation and Test Grading

VTI's logic simulation verifies logical operation and timing, and checks the designer-generated test sequence. The logic simulator links the netlist with a technology database library containing the required macro logic-timing models. Logic and timing simulations are performed with a sequence of test vectors. When the network is found to operate properly, a more complete sequence of test vectors may be graded by the fault simulator to determine fault coverage. Normally this requires an iterative process of generating and evaluating test vector sequences. For the VGC Series, the final sequence of test vectors is produced in a tape format compatible with the VTI SENTRY automatic test system. This test sequence is used later to functionally test the chip.

Generating an adequate test sequence is the designer's responsibility. Fault simulation (optional) program determines the test coverage provided by the test sequence. If the testability is not satisfactory to both VTI and the designer, VTI may request that additional test vectors be supplied or that test circuitry be included on the gate array.

Placement

After simulation, a separate section of the VTI gate array design system aids the designer in performing physical design or layout. As soon as the simulation is complete, the logic netlist is transferred to the physical design section of the system. There, the physical layouts of the required macros are obtained from a physical design library and linked to the netlist. At this point, the user may specify manual macro placement on an interactive graphics terminal or may let automatic placement software perform this task. Manual pre-placement requirements are described in greater detail in Chapter 6.

Automatic and Interactive Routing

An automatic router interconnects the macros as specified in the netlist. If the routing is not completed, further automatic routing may be performed or the routing may be completed interactively at a graphics terminal. With the VTI gate array routing system operated in the interactive mode, control of the netlist is maintained at all times to avoid the need for checking the accuracy of post-routing connectivity. Only connections in the netlist can be made.

Resimulation After Routing

After routing, the wire lengths and other physical attributes of the design are returned to the logic simulator. Array simulation may be repeated to evaluate timing performance and new macro placements may be assigned to correct timing problems. In that case, automatic routing and simulation are repeated to verify improvement.

Design Checking

Two types of design checks are performed. The first check is performed by VTI gate array design system after the logic is entered. This program checks fan-in, fan-out and macro output configurations to verify that no logic design rules are violated. Error messages are generated and the design cannot proceed until all errors have been corrected. After a physical design is complete, design rule checking (DRC) and netcompare is performed by VTI, using a DRC program. The DRC program checks for mask design rule violations such as metal width and spacing errors, via placement errors and layer-to-layer registration errors. The netcompare program compares the schematic netlist to the netlist created by the placement and routing program to insure correct implementation of the designed circuit.

Mask Tape Generation

After routing and logic simulation, the placement and routing data base is merged with the fixed interconnection data base to produce drawings for the two layers of metal and the via plane. DRC checks are performed and a fracturing program generates the control tapes for electron-beam mask making equipment.

VTI gate array design system flow is outlined in Figure 1-3.

Fabrication and Assembly

Mask Making

Electron-beam mask making equipment produces masks suitable for use in the manufacturing process.

Gate Array Customization

VGC Series wafers are fabricated in volume up to the first metal deposition step and placed in a wafer bank for array-option prototypes. Four processing steps complete wafer fabrication. These steps are:

- First metallization masking and etching
- Vias (windows in intermetal oxide)
- Second metallization masking and etching
- Silicon-nitride scratch protection layer

To customize a gate array, only three masks are generated with each design, namely metal1, via, and metal2 masks. All others remain unchanged.

Wafer Probe, Assembly and Test

When fabrication is complete, the wafers are probed and functionally tested by VTI using the customer-generated test sequence. The wafers are then sawed, the good dice are assembled in packages and the packaged chips are retested prior to shipment.

Delivery of Prototypes

Ten packaged gate arrays, which meet VTI parametric (input and output) specifications and which meet the customer-generated test sequence, will be supplied.

DESIGN SUPPORT

VTI is ready to assist you in preparing your gate array design by providing training classes and impromptu information from your nearest VTI design center.

Training

Two types of design classes are available for engineers wishing to design with the VGC Series gate arrays. One-week classes provide hands on training on the VTI Design System as well as covering the specifics of the array family and array design considerations. For those planning to use other CAD systems, a two-day class will be available covering only the array specifics and design considerations.

Contact your Sales Engineer or VTI representative for class schedules and contents.

Applications Assistance

Application assistance is available in VTI's extensive network of design centers. The network is comprised of VTI Design Centers and independent Authorized Design Centers. Design Centers provide customers access to extensive CAD resources and experienced design engineers. For the location of the Design Center nearest you, contact your VTI sales engineer or VTI representative.

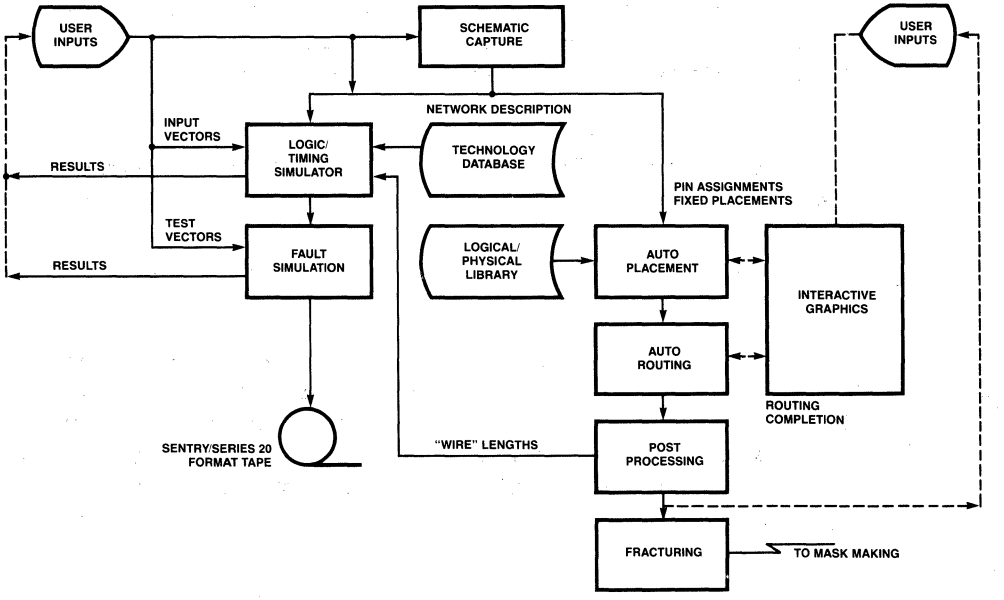


Figure 1-3. VTI Gate Array Design Flow Diagram

CHAPTER 2

PHYSICAL DESCRIPTION

ARRAY ARCHITECTURE

This chapter describes the physical layout of the structures on a VGC Series gate array. First, the various types of cells are discussed in the next section. Internal cells make up the bulk of a gate array; they implement the basic logic network. I/O and input cells provide connections to the outside world. Voltage and ground buses, described in the section after that, are necessary for all cells and are distributed over the array's surface. The section, **Signal Routing**, describes cell interconnection. The last section in this chapter details the pre-defined metallization.

CELLS

A cell is a functionally differentiated area that contains a standard pattern of transistors and support structures designed for one of three applications:

- Internal logic
- I/O
- Input only

For each macro selected by the designer for use in their design, one or more of the appropriate cells will be employed. The transistors within each cell (or cells) committed to a specific macro will be interconnected according to the metallization pattern specific to the macro selected.

Internal Cells

Internal cells are used to build the internal logic functions that comprise the bulk of the gate array option. The internal cells are in the center of the array, interspersed with alternating horizontal VSS and VDD power buses. There are no vertical divisions between cells.

Figure 2-1 shows the VGC1200. It has 36 rows and 22 columns, for a total of 792 internal cells. Figure 2-2 shows the VGC4000 chip with its 2640 internal cells. Figure 2-3 is a more detailed view of the power bussing for a single internal cell. The individual internal cell structure is the same for all arrays in the VGC Series.

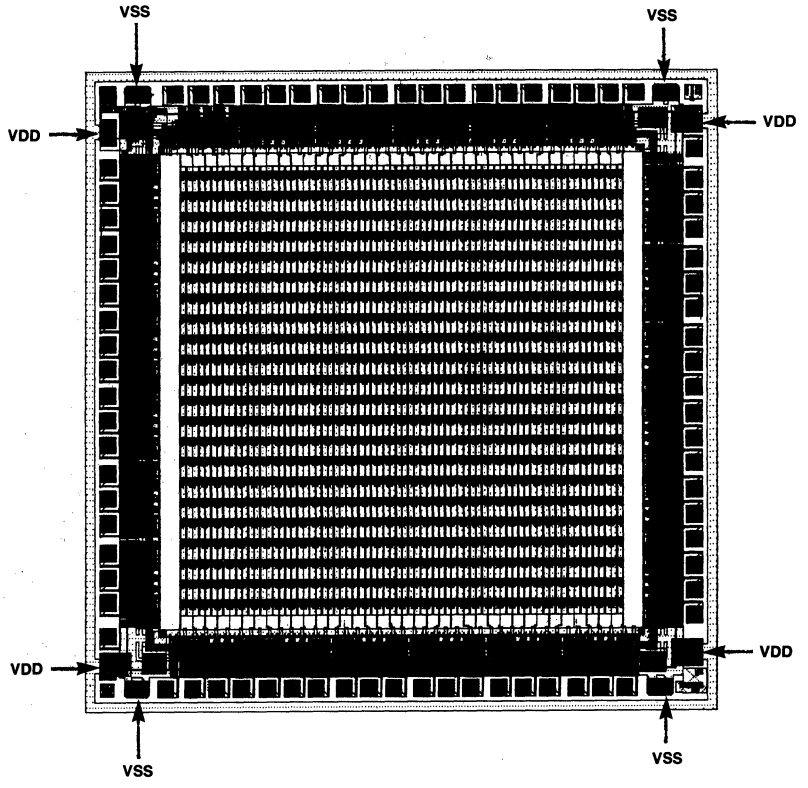
I/O Cells

I/O cells are used to build input buffers, output drivers or transceivers. The VGC1200 has 46 I/O cells around its edges, as shown in Figure 2-1. The VGC4000 has 86 I/O cells around its edges, as shown in Figure 2-2.

Input Cells

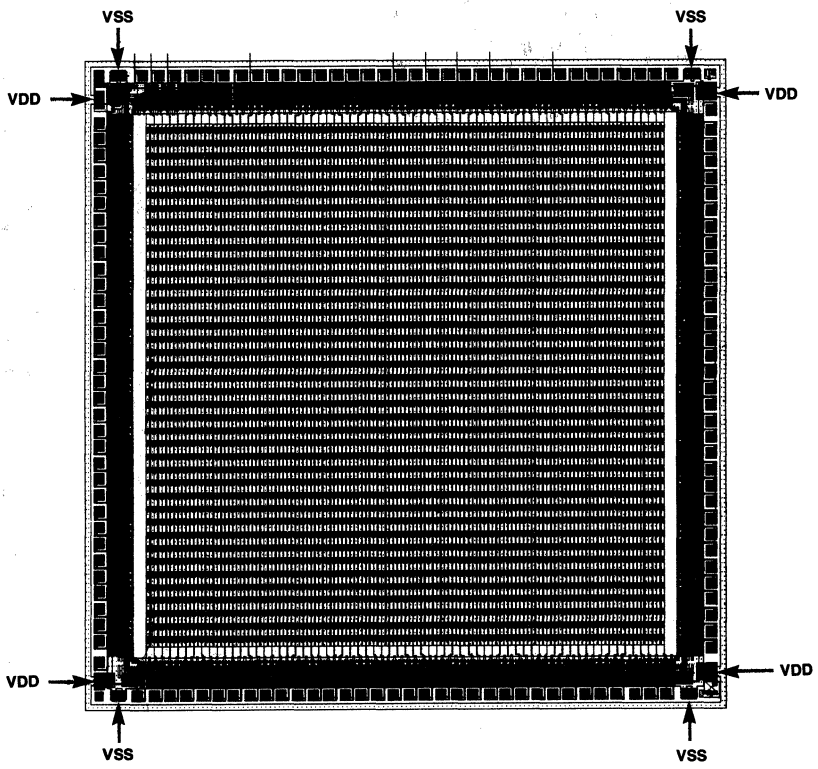
Only input buffers may be built in input cells and all arrays in the VGC Series have them except the VGC0500. The VGC4000 has 47 input cells around its edges, each sandwiched between two I/O cells. See Figure 2-4.

Input-only cells require less space than I/O cells. By including some input-only cells, more total buffering capability can be provided around a gate array's limited edge space.




```
Number of Internal Cells    = 792 (Which equals 1188 two-input
                              NAND equivalent gates)
Number of Input-only cells  = 27
Number of I/O Cells         = 46
Number of Power Pads        =  8 (two for VSS, two for VDD)
```

Figure 2-1. VGC1200 Cells and Buses




```
Number of Internal Cells     = 2640 (Which equals 4000 two-input
                                NAND equivalent gates)
Number of Input-only Cells   =   47
Number of I/O Cells          =   86
Number of Power Pads         =    8 (four for VSS, four for VDD)
```

Figure 2-2. VGC4000 Cells and Buses

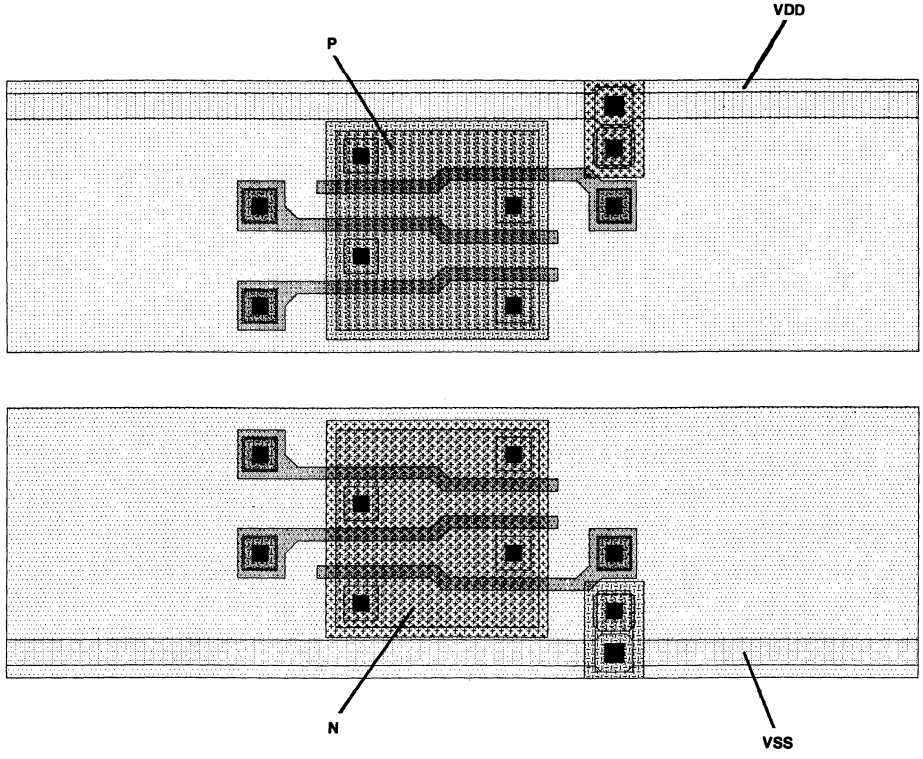


Figure 2-3. An Internal Cell

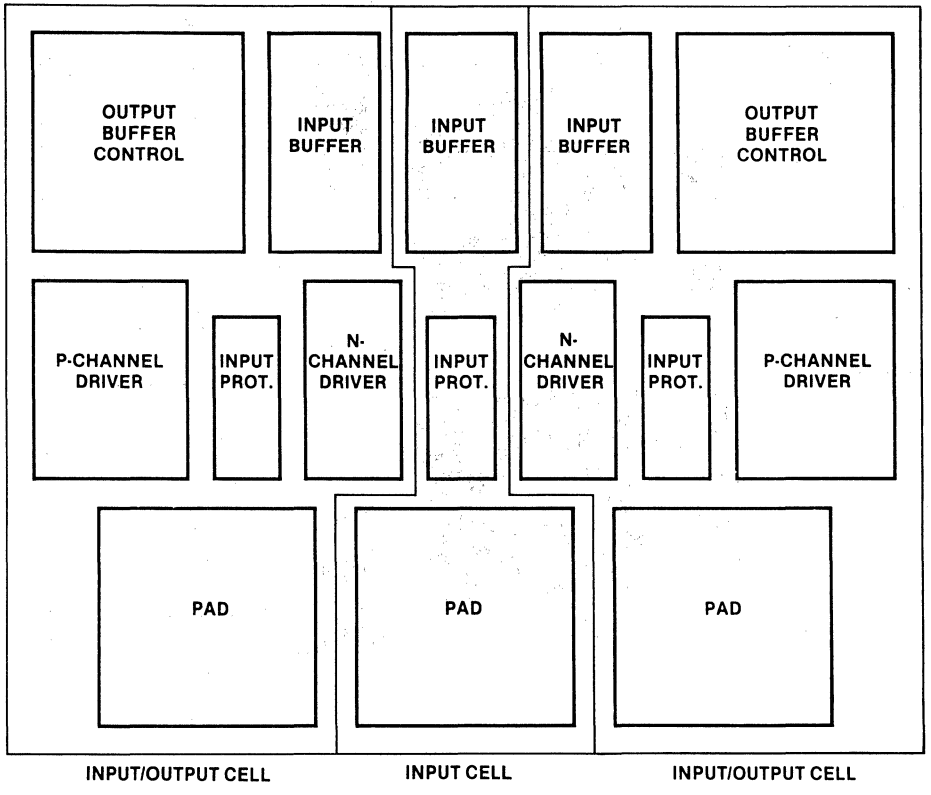


Figure 2-4. I/O and Input Cell Layout

VOLTAGE AND GROUND BUSES

There are two separate rings of power buses on the chip. The outermost set is dedicated to the I/O and input cells. The inner set, surrounding the internal cells, supplies the horizontal power and ground buses throughout the internal cell matrix.

The outer set of buses is supplied by power pads on the perimeter of the chip. On the VGC0500 there are four power pads, two for VSS and two for VDD, placed in opposite corners of the chip. The VGC8000 has sixteen power pads. The inner set of buses is connected to the outer set at the corners.

By segregating the power buses for the internal cells from the power buses for the I/O and input cells, the VGC Series minimizes noise problems of switching transients. Voltage drops are also minimized by wider bus lines for the I/O cells.

SIGNAL ROUTING

Signal routing occurs on the two layers of metal that interconnect cells and macros, along well-defined vertical and horizontal channels. The two routing layers are described below.

First-layer Routing Channels

First-layer metal runs vertically in 18 channels per cell. Four of the channels are partially blocked by first contacts which are access points to the source, drain and gate of the transistors. Intra-macro connections are primarily made with first-layer metallization located over the cells.

Second-layer Routing Channels

Second-layer metal runs horizontally in 11 channels per cell with one channel used for power buses and the other ten employed for cell routing. Inter-macro connections are made with both first-layer and second-layer metal, above the first-layer metal, in patterns running over the cells.

PRE-DEFINED METALL-IZATION

The VTI automatic router generates only the metallization patterns for the macro interconnections specified by the netlist. All other metallization is fixed or standard. Standard structures are: power buses, ground buses, and certain portions of internal and I/O macros.

The user-selected (automatically routed) metallization and the standard metallization are merged by VTI to produce the complete metallization database.

Power and Ground Buses

The locations of power and ground buses are described in the previous section. The power and ground buses are a fixed-grid structure. When a macro is placed on the array, it includes the vias and standard metallization necessary to connect that macro to power and ground.

Internal Macros

Internal macros are pre-defined to perform specific logic functions. The only information required by the router is the X-Y coordinates of the input and output connection points to the macro. The router lays traces to the specified coordinate position on second-layer metal and inserts necessary vias to contact first-layer metal. This allows second-layer metal to be routed over unused macro inputs or outputs so that second-layer routing channels are not blocked.

All internal cells have standard first-layer metallization which covers transistor contacts. This means that all unused cells have a first-layer metallization pattern and cannot be used for additional first-layer routing channels.

I/O and Input Macros

Each I/O cell and input cell location includes standard metallization which covers all contacts and bonding pad areas. The additional metal required to complete a specified macro is added to the standard cell metallization when the I/O macro is specified. This additional metal includes the vias and connections necessary to connect power and ground.

The X-Y coordinates of the routing targets are stored in a program file. When an I/O macro is placed, the placement coordinates automatically specify a set of corresponding routing targets. The router has all information necessary to make connections between internal and I/O or input macros as specified by the netlist.

CHAPTER 3

CIRCUIT TOPOLOGY AND OPERATION

INTRODUCTION

Chapter 3 initially reviews the fundamentals of CMOS circuits. The remainder of the chapter is devoted to VGC Series component layout, function and operation.

Internal cell macros are described. Examples are given for input, output and transceiver macros.

CMOS CIRCUIT FUNDAMENTALS

CMOS circuits are popular because of their low power dissipation, high noise immunity and their ability to operate from a wide range of supply voltages . CMOS is built with metal-oxide semiconductor field-effect transistors (MOSFETs). Each FET has three elements: a source, a drain, and a gate. As their names imply, the source and the drain are input and output for current, while the gate controls the flow of that current. The voltage on the gate, separated from the channel between the source and drain by an insulator, causes an opposing charge to gather in the channel directly underneath the gate. The gate can thus control the conductivity of the channel.

Inverter

The simplest CMOS device is an n-channel/p-channel MOSFET pair connected in parallel to form an inverter. This structure is shown in Figure 3-1. When the signal at IN is HIGH, the p-channel transistor will turn off. The HIGH on its gate will pull a negative charge into the channel and choke off conduction. At the same time, the n-channel transistor will turn on, the HIGH on its gate bringing the necessary negative charge into the channel for conduction. OUT will be pulled down to VSS . When IN is LOW, the n-channel MOSFET will turn off, the p-channel MOSFET will turn on and OUT will be pulled up to VDD. Power will be consumed only during the output voltage transition. For this reason, CMOS circuits consume extremely small amounts of power when operated at low frequencies. The only power consumed in static conditions comes from leakage currents. Because little current actually flows during the transition, power dissipation is due almost entirely to capacitive loading.

The DC fan-out is limited only by the wiring capacitance effects. Larger fan-outs will mean greater propagation delays. More details on this subject can be found in Chapter Four under the section entitled **UNIT LOADS**.

Transmission Gate

The other major building block in CMOS systems is the transmission gate (shown in Figure 3-2). Because it has almost infinite resistance when open and almost zero resistance in either direction when closed, it functions as a nearly ideal switch.

The gate is on when G1 is LOW and G2 is HIGH. It is off when G1 is HIGH and G2 is LOW. Because these signals are opposite in both situations, they are commonly derived from a single source with one branch running through an inverter.

More complicated functions are often constructed of inverters and transmission gates. Later in this chapter, the sub-section entitled "Internal-Cell Macro Operation" describes a D-latch, for the VGC Series, that is built in this manner.

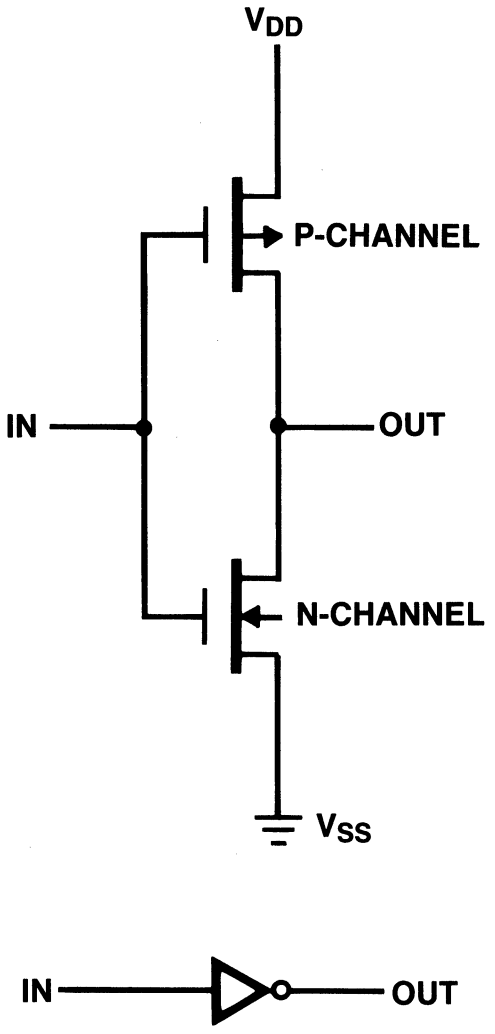


Figure 3-1. CMOS Inverter Schematic and Logic Symbol

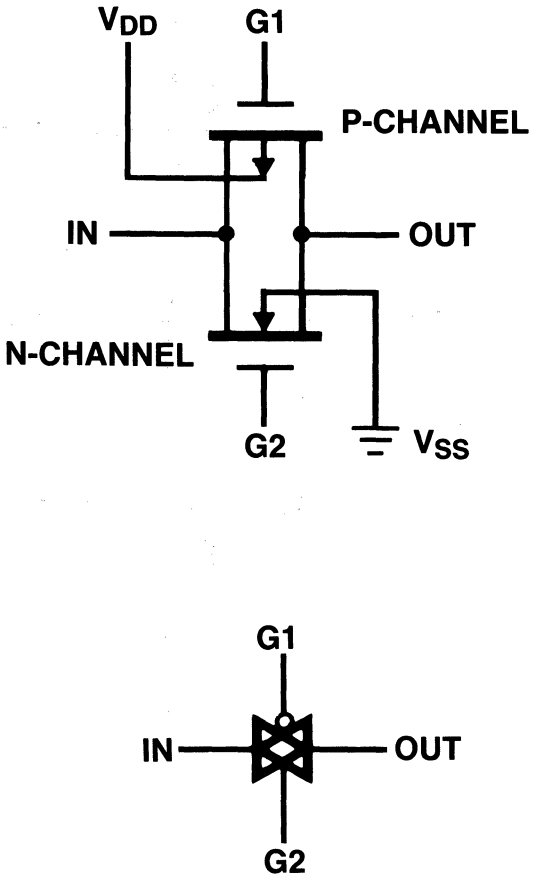


Figure 3-2. CMOS Transmission Gate Schematic And Logic Symbol

INTERNAL CELLS AND MACROS

The internal cells take up most of the gate array area. They are used to implement all logic except input and output requirements.

Internal Cell Components

The components of an internal cell are listed in Figure 3-3; also see the illustration in Figure 2-3. The cell consists of six transistors; three p-channel and three n-channel. The cell uses a bent-gate pattern to optimize performance and minimize size. Logic functions implemented with a single cell include two inverters, a 2-input NAND or NOR and an inverter and a 3-input NAND or NOR.

Internal-Cell Macro Operation

The following paragraphs describe a representative circuit and its operation. The circuit is a D-latch macro called "LAE01" in the VGC Series macro library.

LAE01: Clocked D-latch

See Figure 3-4.

Data will feed through LAE01 when the clock (CK) is LOW. A LOW clock signal turns on the upper transmission gate (T1) and turns off the lower gate, (T2). The data signal can then feed through to the inverter (I2). After inversion, the data signal is fed to a pair of inverters (I3 and I4). The top inverter (I3), produces the Q (data) signal, while the other inverter (I4) feeds back into the lower transmission gate (T2) when the clock is HIGH; that causes signal to latch. The value will then remain static until the clock goes LOW again.

The inverter (I1) inverts the clock signal to CK.

Component	Quantity
n-channel transistor	3
p-channel transistor	3

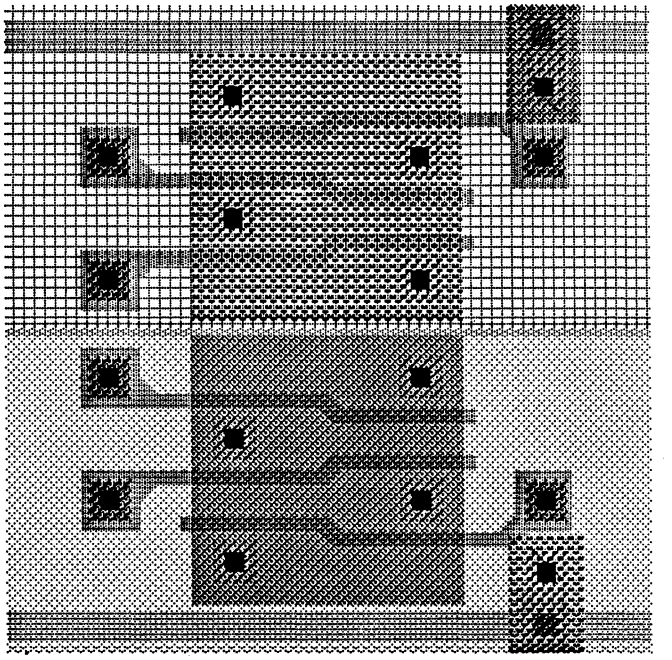


Figure 3-3. Internal Cell Components

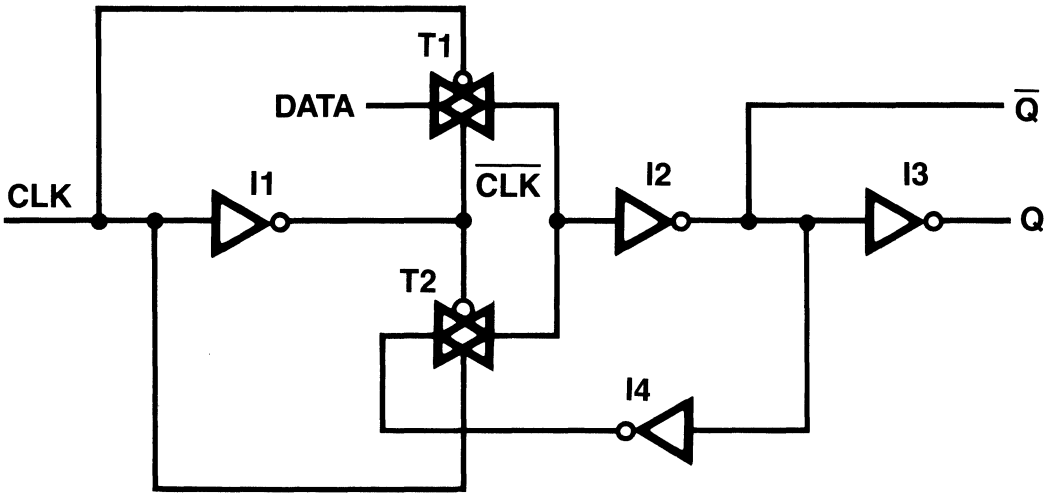


Figure 3-4. D-Latch Logic Diagram and Schematic

Example Internal-Cell Macro Routing

Figure 3-5 illustrates the standard first-layer metallization of the LAE01 D-latch.

I/O CELLS AND MACROS

The components within each I/O cell are interconnected in different configurations to form I/O macros.

Figure 3-6 is a simplified schematic of an I/O cell. The input buffer line at the bottom of the schematic is fairly straightforward. The signal labeled OUTPUT ENABLE is used in transceiver macros to control the direction of information flow.

Input Buffer Macros

I/O cells can serve as input buffers, just like the input cells that are described in the section, **Input Cells**. The logic diagram for the standard input buffer is shown in Figure 3-7. Input buffers may have a CMOS or TTL-compatible interface, a Schmitt trigger and either a floating input or a pull-up to VDD. Figure 3-8 lists the options and the macros with which they are associated.

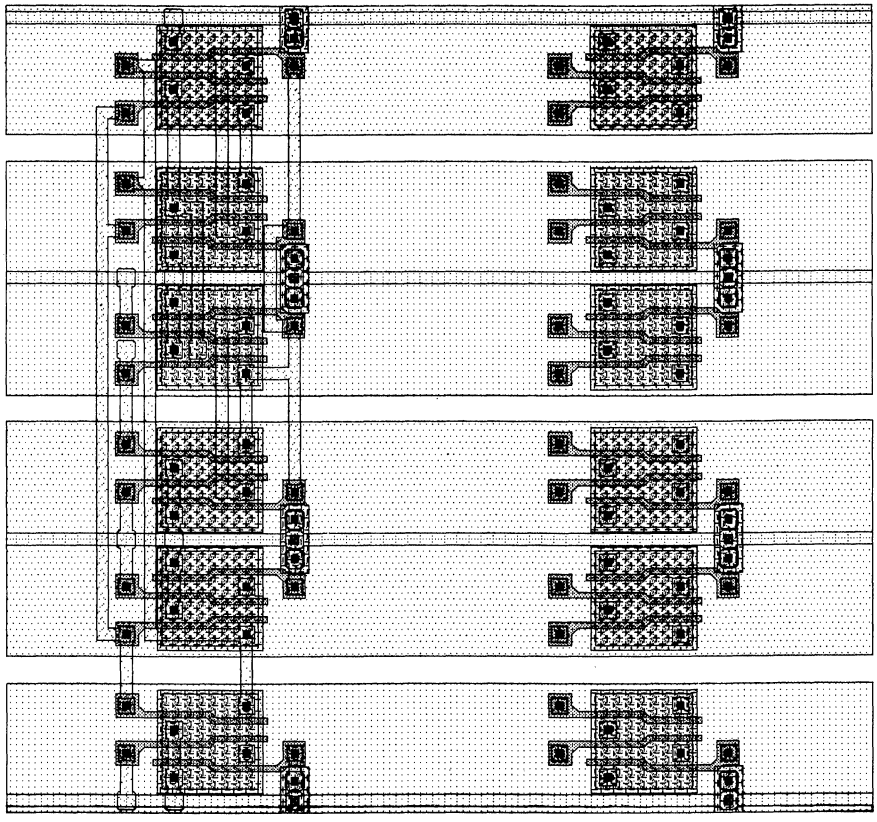


Figure 3-5. D-latch First-layer Metallization

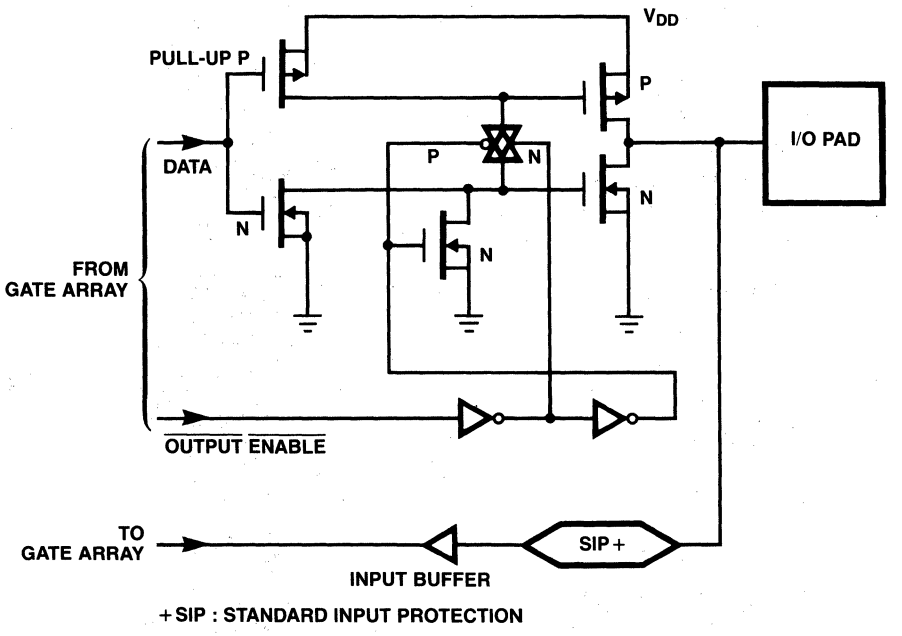


Figure 3-6. Simplified Schematic of I/O Cell

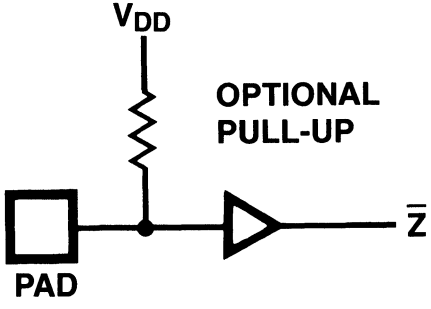


Figure 3-7. Logic Diagram for Input Buffer Macro

NAME	Interface CMOS	Interface TTL	Input Configuration Floating	Input Configuration Pull-up	Schmitt Input	VGC0500 Only
IOSO2		X	X		X	
IOSO2F		X	X		X	X
IOSO21F		X		X	X	X
IOCO1	X		X			
IOCO11	X			X		
IOCO1F	X		X			X
IOCO11F	X			X		X
IOTO1		X	X			
IOTO11		X		X		
IOTO1F		X	X			X
IOTO11F		X		X		X
IOTO4		X	X			
IOTO41		X		X		

Figure 3-8. Input Buffer Macros

Output Buffer Macros

I/O cells can also be used as output buffers. The available output buffer macros are listed in Figure 3-9. Figure 3-10 shows the logic diagram of an output buffer. These buffers have an integral test capability as shown in the table at the bottom of the figure.

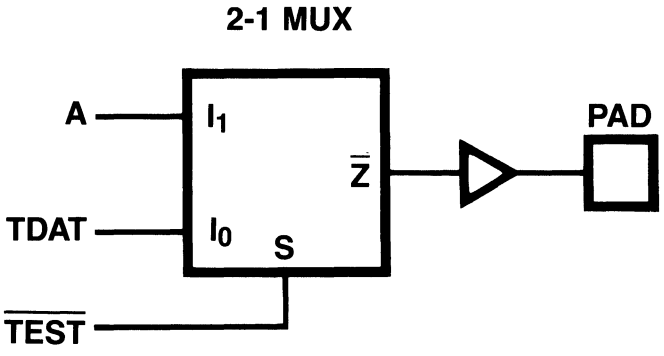
Figure 3-11 shows the same information, logic diagram and test states, for a 3-state output buffer.

The built-in testability (described in more detail in Chapter 7) shortens the test time and reduces the front-end design effort for the gate arrays.

Output buffers sink 8 mA (10 mA for VGC0500) current over the worst-case commercial/industrial temperature range (85 deg. C, 4.5V). Military worst-case temperature range will sink 6 mA (8 mA for VGC0500) at 125 deg. C and 4.5V.

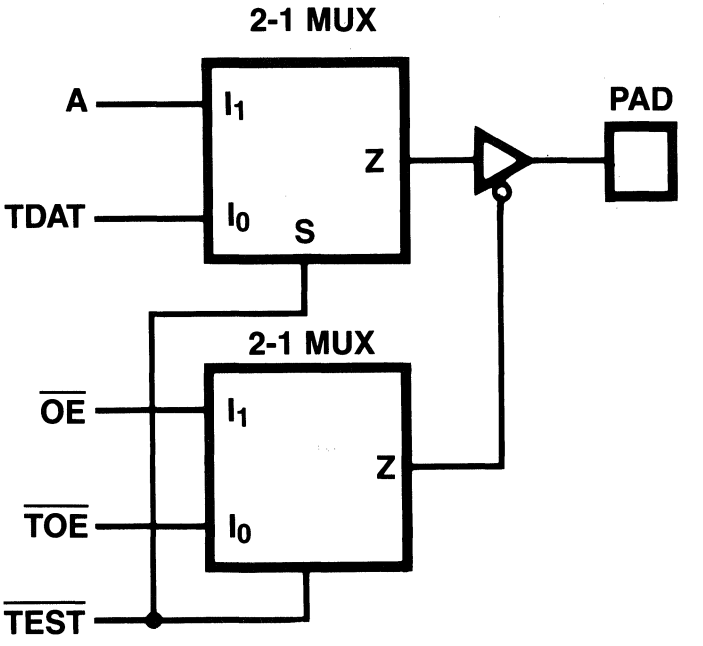
NAME	Output Configuration Standard	3-State	VGC0500 Only
OBO1	X		
OBO3		X	
OBO1F	X		X
OBO3F		X	X
OBO4F	X		X

Figure 3-9. Output Buffer Macros



A	TDAT	TEST	DESCRIPTION
Input	X	1	Normal operation
X	TDAT	0	DC parametric tests

Figure 3-10. Output Buffer Logic Diagram



A	TDAT	TEST	OE	TOE	DESCRIPTION
Input	X	1	OEN	X	Normal operation
X	TDAT	0	X	0	DC parametric tests
X	0	0	X	1	3-state leakage
X	1	0	X	1	Standby current

Figure 3-11. 3-State Output Buffer Logic Diagram

Transceiver Macros

I/O cells can also support transceiver macros. These structures can either transmit or receive data, depending on the state of OUTPUT ENABLE. Figure 3-12 shows the logic diagram for a typical transceiver. These macros are non-inverting, can have a CMOS or TTL-compatible interface and a Schmitt trigger input.

Figure 3-13 lists the transceiver macro options.

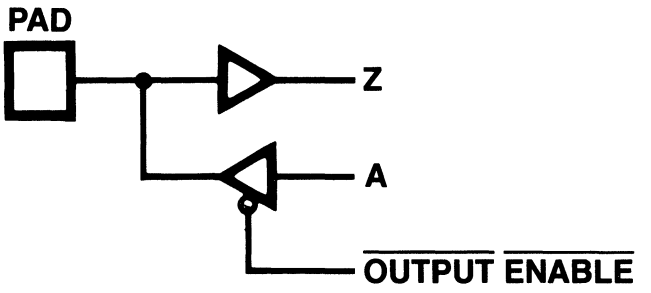


Figure 3-12. Transceiver Logic Diagram

NAME	Interface CMOS	Interface TTL	Pull-Up	VGC0500 Only
TRC03	X			
TRC031	X		X	
TRC03F	X			X
TRT03		X		
TRT031		X	X	
TRT03F		X		X

Figure 3-13. Transceiver Macros

INPUT CELLS

All gate arrays in the VGC Series, except the VGC0500, have input-only cells in addition to full-function I/O cells. This is done to conserve chip area.

Figure 3-7 shows the logic diagram for a typical input buffer. As with I/O buffer macros, the input buffer macro can have a CMOS or TTL-compatible interface, a floating input or a pull-up to VDD and a Schmitt trigger (except on the VGC0500). These options are listed in Figure 3-8.

CHAPTER 4

MACRO LIBRARY SUMMARY

INTRODUCTION

The macro library contains the logical and electrical specifications for all VGC Series macros. The designer must specify these macros and use their logical symbols, names and pin numbers to enter design data into the VTI gate array design system. Table 4-1 is a partial list of the macros now available.

Appendix A of this manual presents the complete VGC Series Macro Library. These macros are used for all arrays in the VGC Series. A sample macro specification is included at the end of this chapter.

The initial macros in the internal cell library were chosen to simplify conversion from 74XX functions to CMOS. Other macros, some already in the library and others in planning, extend beyond those functions. General categories of the library are:

- Basic gates
- Inverters/Buffers
- Complex gates
- Latches
- Flip-Flops
- Multiplexers/Decoders
- Arithmetic functions

- Input buffers
- Output buffers
- Transceivers
- Power pads

TABLE 4-1: VGC SERIES MACRO LIBRARY

INTERNAL CELL MACROS

	MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION
BASIC	GATES		
	NA02	1	2-NAND
	NA02I	1	2-NAND & INVERTER
	NA03	1	3-NAND
	NA04	2	4-NAND
	NA05	2	5-NAND
	NA05I	3	5-NAND & INVERTER
	NA06	2	6-NAND
	NOR02	1	2-NOR
	NOR02I	1	2-NOR & INVERTER
	NOR03	1	3-NOR
	NOR04	2	4-NOR
	AND02	1	2-AND
	OR02	1	2-OR
	X2NA04	3	DUAL 4-INPUT NAND
INVERTERS/BUFFERS			
	INV11	1	DUAL 1X INVERTERS
	INV12	1	INVERTERS (1X and 2X)
	INV03	1	INVERTERS (3X)
	BUF02	1	NON-INVERTING INTERNAL BUFFER, 2X
	INV01T	1	3-STATE INVERTER (INTERNAL,1X)
	INV02T	2	3-STATE INVERTER (INTERNAL,2X)
	INV03T	3	3-STATE INVERTER (INTERNAL,3X)
COMPLEX GATES			
	XOR02	2	2-IN EXCLUSIVE-OR
	XNOR02	2	2-IN EXCLUSIVE-NOR
	XNOR021	2	2-IN EXCLUSIVE-NOR
	AOI21	1	2-1 AND-OR-INVERTER
	OAI21	1	2-1 OR-AND-INVERTER
	AO22	2	2-2 AND-OR W/COMP. OUTPUTS

INTERNAL CELL MACROS (continued)

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION
COMPLEX GATES (continued)		
AOI222	2	2-2-2 AND-OR-INVERTER
AOI22I	2	2-2 AND-OR-INVERT & 2X INV.
AOI33	2	3-3 AND-OR-INVERTER
LATCHES		
LAO1	3	BUFFERED LATCH,
LAE01	3	D-LATCH
LAE01T	4	W/3-STATE OUTPUT
LAE01S	5	W/SCAN LOGIC
LAO2	3	W/CLEAR, BUFFERED OUTPUTS
LAE02	3	W/CLEAR
LAE021	2	W/CLEAR, EXTERNAL ENABLE
LAE021T	3	W/CLEAR, EXTERNAL ENABLE & 3-STATE OUTPUTS,
MEM01	3	GATED W/3-STATE OUTPUT
MEM02	3	GATED W/3-STATE OUTPUT
FLIP FLOPS		
DFP01	4	D FLIP-FLOP
DFP74	6	W/SET, CLEAR
DFP011	4	W/EXTERNAL CLOCKS
DFP011T	4	W/3-STATE OUTPUT, EXT. CLK
DFP01S	6	W/SCAN LOGIC
DFP02	5	W/CLEAR DIRECT
DFP021	4	W/CLEAR, EXTERNAL CLOCKS
DFP021T	5	W/CLEAR, EXTERNAL CLOCKS, 3-STATE OUTPUT
DFP02S	7	W/SCAN, CLEAR
DFP03	5	W/SET
DFP031	4	W/SET, EXTERNAL CLOCKS
DFP04	6	W/SET, CLEAR
DFP05	4	W/BUFFERED OUTPUT
JKN02	7	JK FLIP-FLOP W/ CLEAR
JKN76	8	JK FLIP-FLOP
TF02	5	TOGGLE FLIP-FLOP W/CLEAR

INTERNAL CELL MACROS (continued)

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION
MULTIPLEXERS/DECODERS		
MX02	3	2 TO 1 MULTIPLEXER (MUX)
MX04	5	4 TO 1 MUX
MXE04	6	4 TO 1 MUX (1/2 74153)
MXE041	5	4 TO 1 MUX W/ENABLE
DC24	4	1 OF 4 DECODER
DC139	7	1 OF 4 DECODER, W/ENABLE
MISC. MACROS		
ADD01	6	1-BIT FULL ADDER

EXTERNAL CELL MACROS

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION
INPUT BUFFERS		
IOT01F	1	TTL INPUT BUFFER, VGC0500
IOT01	1	INPUT BUFFER
IOT011F	1	INPUT BUFFER W/PULL-UP, VGC0500
IOT011	1	INPUT BUFFER W/PULL-UP
IOC01F	1	CMOS INPUT BUFFER, VGC0500
IOC01	1	INPUT BUFFER
IOC011F	1	INPUT BUFFER W/PULL-UP, VGC0500
IOC011	1	INPUT BUFFER W/PULL-UP
IOT04	1	TTL INPUT BUFFER; 4:1 RATIO
IOT041	1	TTL INPUT BUFFER W/PULL-UP, 4:1 RATIO

IOS02	1	SCHMITT TRIGGER INPUT BUFFER
IOS02F	1	INPUT BUFFER, VGC0500
IOS021F	1	INPUT BUFFER W/PULL-UP, VGC0500

EXTERNAL CELL MACROS (continued)

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION
OUTPUT BUFFERS		
OB01F	1	STANDARD, 10 mA, VGC0500
OB03F	1	3-STATE, VGC0500
OB04F	1	STANDARD, 8 mA VGC0500
OB01	1	STANDARD, 8 mA
OB03	1	3-STATE
TRANSCEIVERS		
TRT03	1	TTL TRANSCEIVER INTERFACE
TRT031	1	TTL TRANSCEIVER INTERFACE W/PULL-UP
TRT03F	1	TTL TRANSCEIVER INTERFACE, VGC0500
TRC03	1	CMOS TRANSCEIVER INTERFACE
TRC031	1	CMOS TRANSCEIVER INTERFACE W/PULL-UP
TRC03F	1	CMOS TRANSCEIVER INTERFACE, VGC0500
POWER PADS		
IOVSSF	1	VSS POWER PAD, VGC0500
IOVSS	1	VSS POWER PAD,
IOVDDF	1	VDD POWER PAD, VGC0500
IOVDD	1	VDD POWER PAD,

LIBRARY FORMAT

The macro library has a section for each macro. These sections are divided into logical subsections that contain the various specifications. The order of those specifications is described below.

First Page

The first page of a specification describes the macro's logical capability and includes the following:

- Macro name
- Logic function
- Functional description of the logic
- Number of cells/equivalent gates
- Cell type that the macro will use
- Logic symbol
- Function table
- Pin description table
- Revision number

The logic symbol appears on the specification exactly as it will appear on all VTI gate array design system graphics displays and plots.

The Pin Description table lists all inputs and outputs for the macro, giving the correct pin name and function for each. In addition, the fan-in (in Unit Loads) is given for each input.

The Function Description presents a brief description of the logic function(s) performed by the macro.

Second And/or Third Page

The following pages include the circuit schematic diagram.

The following pages contain AC characteristics for the macro. Voltage, temperature, and process conditions are specified at which the propagation delays for sample loads are shown. Performance equations for the key parameters are also shown. Delays under any conditions can be estimated by using these equations and the derating curves shown in Chapter Five under the section, **Performance**.

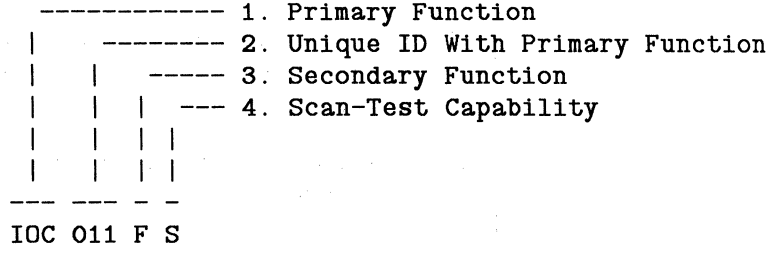
Performance equations are given in the form

```
tTOTAL = tDEL + tINT + tNLF * UL.
```

tTOTAL = total delay (ns) from specified input to specified output
tDEL = internal delay (ns) of the cell
tINT = delay (ns) due to the intrinsic output capacitance
tNLF = normalized load factor (ns/UL)
UL = unit load = 0.15pF

NAMING CONVENTIONS

The macro names are composed of up to four fields. In the example name below, the fields have been separated with blank spaces to clarify their boundaries:



The contents of the four fields are explained below:

1. Primary Function (2 to 4 alphas)

   A partial list includes:

```
AND  -  AND gate
AOI  -  AND-OR-invert
BUF  -  Buffer
DFN  -  D flip-flop (net) (negative edge triggered)
DFP  -  D flip-flop (pet) (positive edge triggered)
IB   -  Input buffer (Input Cell)
INV  -  Inverter
IO   -  Input buffer (I/O Cell)
IOC  -  Input buffer, CMOS
IOT  -  Input buffer, TTL
JKN  -  JK flip-flop (net)
JKP  -  JK flip-flop (pet)
NA   -  NAND gate
NOR  -  NOR gate
OAI  -  OR-AND-invert
OB   -  Output buffer
OR   -  OR gate
PUP  -  Pull-up
TR   -  Transceiver
TRC  -  Transceiver, CMOS
TRT  -  Transceiver, TTL
XNOR -  Exclusive NOR gate
XOR  -  Exclusive OR gate
```

2. Unique ID Within Primary Function (2 to 4 digits)

   Simple combinatorial functions:

   First two digits indicate the number of inputs; a third digit, if used, identifies a variation on the function.

   Sequential functions:

   Start with "01" and count up; a third digit, if used, identifies a variation on the function.

   AOI and OAI macros:

   Up to four digits, one for each first-stage gate, where the digit represents the number of inputs in that first-stage gate.

   Input/output buffers:

```
"01"    Standard input or totem-pole output
"011"   Standard input with pull-up
"02"    Schmitt-trigger input
"021"   Schmitt-trigger input with pull-up
"03"    3-state output
```

3. Secondary Function (1 alpha, if applicable)

   A partial list includes:
   - A AND gate
   - D D flip-flop
   - F VGC0500 only
   - I Inverter
   - L Latch
   - O OR gate
   - T 3-state output (internal cells)

4. Scan-Test Capability (1 alpha, if applicable)

   An S is present in sequential macros that have a scan-test capability.

Table 4-1 is a partial list of macros that apply to the VGC gate array family.

UNIT LOADS

Input capacitance (fan-in) may be expressed in terms of Unit Loads (U.L.). For the VGC Series, one Unit Load is equal to 0.15 pF, the capacitance presented by a single p-channel/n-channel transistor pair. The VGC Series Macro Library specifies the fan-in for each macro input in terms of Unit Loads. Fractional Unit Loads are possible; several examples are shown in the library.

Fan-out is often expressed in terms of Unit Loads. This is correct when fan-out is taken to mean only the capacitive loading due to input capacitance in the net. However, fan-out can also be expressed in terms of the number of inputs driven by a macro output. This is useful for the purpose of calculating loading effects due to the length of interconnect

metallization in a net. In this case a macro driving four inputs would be said to have a fan-out of four.

Since the input capacitance of a macro input often exceeds one Unit Load, it would be incorrect to assume that the fan-out in Unit Loads is the same as the fan-out expressed in terms of number of input connections. To avoid confusion in this manual, "number of connections" will be implied when fan-out does not specify Unit Loads.

CMOS circuits don't have a sharp breakoff point where increased fan-out disrupts function. Instead, as additional loads are added to a circuit, the delay increases. This is due to the combined effects of interconnect capacitance and input capacitance. It is up to the designer to specify and work within a maximum delay. Chapter 5 provides more information on calculating capacitive loading effects on various macros.

MACRO LIBRARY EXAMPLE

The remainder of this chapter is an example of the NA02 2-input NAND gate macro. The macro library itself is **Appendix B** of this manual.

NA02

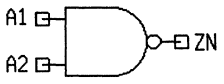
2-INPUT NAND GATE

DESCRIPTION

The NA02 combines inputs A1 and A2, to provide the NAND function at output ZN.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS	OUTPUTS
A1 A2	ZN
L X	H
X L	H
H H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
ZN	Output	-	Data Output

NA02

2-INPUT NAND GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A2->ZN	1.0 + 0.7 + 0.26 * UL	0.2 + 0.6 + 0.21 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

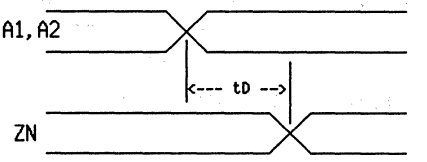
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.0	1.0	2.2	1.2	3.0	1.9	4.3	2.9

Note: For other operating conditions, use derating curves given in the performance section.

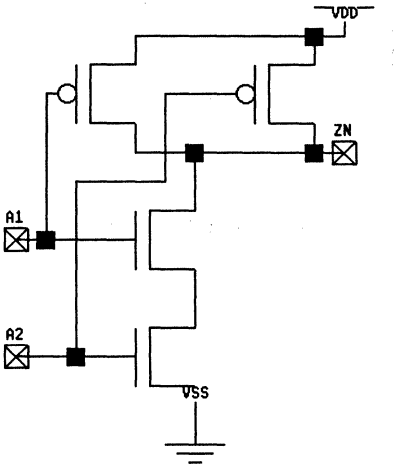
NA02

2-INPUT NAND GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



CHAPTER 5

LOGIC DESIGN

INTRODUCTION

This chapter presents design rules governing use of CMOS macros in the implementation of your design. VGC Series DC specifications are also presented, as well as procedures for estimating the AC performance of your design.

PHYSICAL MACROS

A physical macro is a standard metallization pattern that combines the previously unconnected components of one or more cells of a gate array into a larger functional circuit element. Physical macros are also sometimes referred to simply as "hard macros". In this manual, physical macros are referred to simply as "macros".

Combining Existing Physical Macros to Form a Logical Macro

The macros presently available are all simple SSI or MSI functions. More complex functions can be formed by combining existing physical macros to form shift registers, counters, parity trees, etc. The new function, known as a "logical macro" or "soft macro", can then be saved and used in designing the complete circuit option.

Designing New Physical Macros

The design of new functions which are not combinations of existing macros is not normally permitted because of the time required to obtain electrical characterization data and to develop accurate simulation models.

LOGIC SCHEMATIC

The first step in the design of a gate array option is to draw a logic schematic which implements the required logical functions using the macros from the macro library or convert an existing schematic to a schematic containing only functions available in the macro library.

Logic Symbols

The symbols shown in the library are available to VTI CAD software or schematic capture programs running workstations such as Mentor and Daisy and should be used to speed up CAD schematic entry. In addition, the user may create new symbols to represent new logic macros formed by combining existing physical macros.

Maximum Cell Utilization

When the logic schematic is completed, the total number of cells required must be calculated. If the number of cells exceeds 80% of the total cells available, 100% automatic routing will be increasingly difficult. Additional time will be needed to complete the routing manually. If the logic design contains a large percentage of series-connected logic (shift registers, counters, etc.) or memory, instead of random logic, then higher utilizations may be possible.

VTI will calculate cell utilization. When cell utilization exceeds 80%, the designer should consider partitioning the required logic into two gate arrays or placing part of the logic on another gate array which has low cell utilization. VTI's applications engineers may also be able to provide suggestions to simplify the logic.

Pin-Out Limitations

The next step is to count input pins, output pins, ground pins and power pins. The total must be compared to the desired package type, the number of bonding pads on the chosen chip, the maximum number of input and I/O cells and the number of extra power pads needed.

LOGIC DESIGN RULES

Follow these rules to assure a functional design. The fan-out and unused input rules apply to CMOS circuits in general. The internal 3-state rules are more specific to the VGC Series. VTI's prescreen programs will verify that these rules are followed.

AC Fan-out

Increasing the fan-out of a gate will increase the delay. Simulation will quantify the delay, but the designer must decide what is acceptable.

Unused Inputs

All macro inputs in a design must be connected. That is, every input must be connected to a signal net, pulled to a logic LOW or pulled to a logic HIGH. A POWER macro with output pins for VSS (logic LOW) and VDD (logic HIGH) is provided for this purpose. This macro must be placed once on the schematic and a connector labeled "VDD" or "VSS" tied to all the unused macro inputs.

Routing software automatically converts each of these bullets into a connection to either the VDD or the VSS bus. This method is ideal for two reasons: First no cells are required for the placement of actual macros. Second, the use of routing channels is minimized because the unused input is connected to an adjacent power bus.

Internal 3-state Buses

All arrays in the VGC Series have provisions for internal buses. Internal macros with names ending in a "T" have 3-state driver outputs. These outputs may be connected together as a bus which drives a load. The procedures for designing with 3-state buses are described below.

Internal buses must always be defined. A "floating" bus may result in propagation of an incorrect logic state. In addition, since the designer implements the bus structure, these buses have no inherent "pre-charge" circuitry. Instead, the designer must use pull-up macros to perform this function.

With this pull-up circuitry in place, the bus will revert to a logic HIGH state when all of the bus source outputs are in the high-impedance state (all OE signals are HIGH).

DC Characteristics

Figure 5-1 describes the absolute maximum ratings and the operating ranges.

Figure 5-2 lists D.C. specifications of the VGC series.

ABSOLUTE MAXIMUM RATINGS	Above which the useful life may be impaired
Suppy voltage, VDD	-0.5V to +6V
Voltage on any input	-0.5V to VDD + 0.5V
Current into any input	+/-10mA
Storage Temperature	
Ceramic Packages	-65 to +150 degrees C
Plastic Packages	-40 to +125 degrees C
Lead temperature (Soldering, 10 sec.)	300 degrees C

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE, VDD			Ambient Temperature*
MIN	TYP	MAX	
4.5	5.0	5.5	-40 to + 85 deg. C (comm./ind.) -55 to +125 deg. C (military)

*Junction temperature not to exceed ambient temperature by more than 20 degrees C.

Figure 5-1. VGC Series DC Maximum Ratings And Operating Ranges

DC CHARACTERISTICS $T_A = -55°$ to $+125°C$, $V_{DD} = 5.0\,V \pm 10\%$

Symbol	Parameter	Min	Max	Unit	Conditons
VIH	Input HIGH Voltage CMOS Input TTL Input	 3.5 2.0	 VDD VDD	V	Guaranteed Input HIGH Voltage
VIL	Input LOW Voltage CMOS Input TTL Input	 −0.5 −0.5	 1.5 0.8	V	Guaranteed Input LOW Voltage
VOH	Output HIGH Voltage OB01F OB01	VDD − 0.05 2.4 2.4		V	IOH = −1 µA, VDD = 4.5 V IOH = −10 mA, TA = 85°C, VDD = 4.5 V IOH = −8 mA, TA = 125°C, VDD = 4.5 V IOH = −8 mA, TA = 85°C, VDD = 4.5 V IOH = −6 mA, TA = 125°C, VDD = 4.5 V
VOL	Output LOW Voltage OB01F OB01		0.1 0.4 0.4	V	IOL = 1 µA, VDD = 4.5 V IOL = 10 mA, TA = 85°C, VDD = 4.5 V IOL = 8 mA, TA = 125°C, VDD = 4.5 V IOL = 8 mA, TA = 85°C, VDD = 4.5 V IOL = 6 mA, TA = 125°C, VDD = 4.5 V
IIN	Input Leakage Current	−10	10	µA	VIN = VDD or GND
IOZ	3-State Output Leakage Current	−10	10	µA	VOUT = VDD or GND

CAPACITANCE $T_A = -55°C$ to $+125°C$, $V_{DD} = 5.0\,V \pm 10\%$

Symbol	Parameter	Min	Max	Unit	Conditons
CIN	Input Capacitance		5	pF	Excluding Package
COUT	Output Capacitance		5	pF	Excluding Package
CI/O	Transceiver Capacitance		10	pF	Excluding Package

Figure 5-2. VGC Series DC Specifications

PERFORMANCE

This section contains a general description of the factors affecting performance of the VGC Series of CMOS gate arrays, as well as methods for estimating the performance of a specific design.

Factors affecting propagation delay need to be considered in the design of a gate array option. These factors include:

- Temperature
- Supply voltage
- Process variations
- Load capacitance

Of these four, the first three will be known, or easily estimated, by the designer prior to entering the design. The fourth, load capacitance, cannot be fully defined until the design has been placed and routed. This factor is very important in determining actual propagation delays. The section, **Sample Calculations** (this chapter) presents a complete discussion of methods for calculating estimated propagation delays prior to placement and routing.

Temperature Voltage & Process Effects

Figures 5-3, 5-4, and 5-5 illustrate the derating factors which apply to VTI's VGC Series CMOS gate arrays over standard temperature, supply voltage, and process ranges. These figures are for comparison only. The effects represented in them are included in all data presented as "worst case" in this manual.

Estimation of Performance-Degradation

Where critical path timing performance may be a factor in the design of a gate array option, estimation of performance degradation is essential. Such estimation is based on the following factors:

- Base (or inherent) macro delay for each macro in the path (ns)
- Normalized load factor (ns/UL)
- Load capacitance (pF)

The base delay consists of the inherent delay through a given macro, independent of capacitive loading effects.

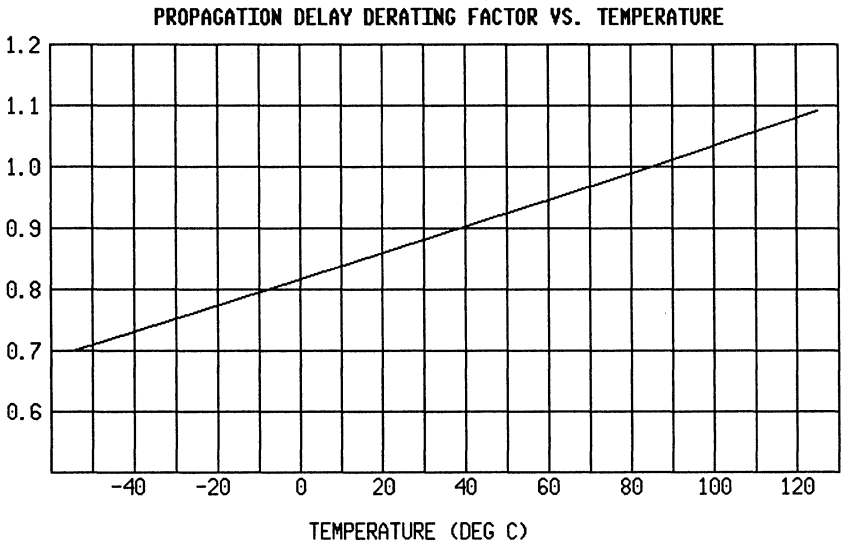


Figure 5-3. VGC Series Propagation Delay vs. Temperature

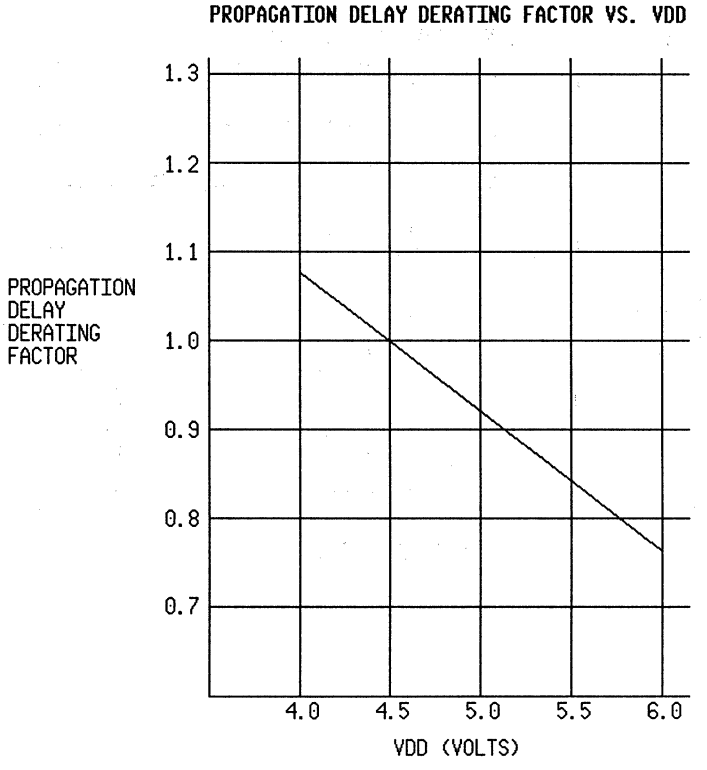


Figure 5-4. VGC Series Propagation Delay vs. Supply Voltage

PROPAGATION DELAY DERATING FACTOR VS. PROCESS

PROCESS	FACTOR
SLOW	1.00
TYPICAL	0.82
FAST	0.66

Figure 5-5. VGC Series Propagation Delay vs. Process

The load factor is a variable determined by SPICE circuit simulation performed by VTI for each macro. It is used to estimate delays due to loading effects for a given macro. Load factors are found in the Macro Library entry for each macro.

Load capacitance is a combination of the input capacitance of the individual loads on a macro output and the capacitance that can be attributed to the total length of the metal interconnecting a macro output and its loads. The general formula for calculating propagation delay is:

```
tTOTAL = tDEL + tINT + tNLF * UL
```

where:

```
tTOTAL = Total delay (ns)

tDEL   = Internal delay (ns)

tINT   = Intrinsic output delay (ns)

tNLF   = Normalized load factor (ns/UL)

UL     = Unit load (0.15pF)
```

Base Delay = tDEL + tINT

In the formula above, both the Base Delay and normalized Load Factor can be obtained from the Macro Library entry for each macro. Since the Load Capacitance depends on the actual interconnect metal lengths, calculations prior to placement and routing of the design must be done using assumed values. The section, **Sample Calculations**, discusses how to calculate delays as accurately as possible before placement and routing.

Propagation Delay Calculations

The general propagation delay formula shown in the previous section can be expanded to provide reasonably accurate estimates of propagation delays in a given design. This section describes the expanded version of the formula and how to use it to calculate delays.

Expansion of the delay formula occurs in the Load Capacitance variable. This value is the sum of the following factors:

- Fan-out, or sum of fan-in capacitances of all inputs in the net expressed as Unit Loads

- metal capacitance (pF)

Fan-out is expressed in terms of Unit Loads. One Unit Load equals 0.15 pF, therefore a macro driving a single input with a fan-in of 0.15 pF (1 Unit Load) would have a fan-out of 1 Unit Load. Similarly, a macro driving two inputs with fan-ins of 0.30 pF (2 U.L.) and 0.225 pF (1.5 U.L.) would have a fan-out of 3.5 Unit Loads. The fan-out, for a given macro output, is the sum of the fan-in capacitances presented by all the inputs connected to that output, expressed as Unit Loads. The Unit Load presented by a given macro input can be found in the Pin Description table on page 1 of the Macro Library entry for that macro.

Metal capacitance per unit length (pF/mil) depends upon the metal layer in question; ie.,

0.00648 pF/mil for first-layer metal

0.00419 pF/mil for second-layer metal

Since the actual metal length cannot be determined before placement and routing, approximations have been developed to aid in metal capacitance calculations. These are as follows:

typical metal length per connection	15 mils
maximum metal length per connection	30 mils

Since the VGC Series has routing on both first- and second-layer metal, these lengths are split between the two metal layers as follows:

typical	30% first-layer metal, 70% second-layer metal
worst case	50% first-layer metal, 50% second-layer metal

Remember that the metal length per input connection and the layer-to-layer metal ratio are approximations only. However, the values are based on statistical values and therefore represent reasonable estimates to facilitate performance estimates prior to placement and routing.

Sample Calculations

To calculate the industrial LOW-to-HIGH delay for an NA02 macro driving four inputs of three other macros, proceed as follows:

- **From the NA02 AC Characteristics table (Figure 5-5), obtain the following:**

  Load Factor 0.26 ns/pF

  Base Delay 1.4 ns
  =(tDEL+tINT)

- **From your schematic and the Macro Library entries for each macro in the net, obtain the following:**

```
Fan-out     5.50 U.L.
(sum of fan-in values for
all macro inputs in the net)

 ______       1.1  _________              1.1 U.L.
|NA02|-----|--->|Macro A|
           |
           |1.9  _________                1.9 U.L.
           |--->|Macro B|
           |
           |1.0  _________                1.0 U.L.
           |--->|Macro C|
           |--->|       |
            1.5                           1.5 U.L.
                                        ________
                                          5.5 U.L.
```

- **Calculate the total interconnect metal length:**

```
@ 15 mils/connection:

 total length = 4 x 15 mils = 60 mils
```

- **Calculate the total metal capacitance:**

```
first-layer length = 30% x 60 mils = 18 mils

second-layer length = 70% x 60 mils = 42 mils

first-layer capacitance = 0.00648 pF/mil x 18 mils

                        = 0.117 pF

second-layer capacitance = 0.00419 pF/mil x 42 mils

                         = 0.176 pF

total metal capacitance = 0.117 pF
                        + 0.176 pF
                        ----------
                          0.293 pF   0.293 pF
Equivalent unit load = 0.293/0.15 = 2 UL
```

- **Calculate the total delay:**

```
tPD = Base Delay + (Normalized Load Factor x Unit Load)

= 1.4 ns + (0.26 ns/UL x (metal UL + fan-in UL))

= 1.4 ns + (0.26 ns/UL x (2 + 5.5 pF))

= 1.4 ns + (0.26 ns/UL x 7.5)

= 1.4 ns + 1.95 ns = 3.35 ns
```

This type of calculation would be repeated for each macro in the critical path and the sum of the individual delays would be the total critical path delay. In the same manner, delay values for worst case conditions could be calculated by substituting worst case values for Base Delay, Load Factor, Metal Length and Metal Split.

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A2->ZN	1.0 + 0.7 + 0.26 * UL	0.2 + 0.6 + 0.21 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.0	1.0	2.2	1.2	3.0	1.9	4.3	2.9

Note: For other operating conditions, use derating curves given in the performance section.

Figure 5-6. NA02 AC Characteristics Table

CHAPTER 6

DESIGN PROCEDURE

INTRODUCTION

This chapter discusses the following aspects of gate array option design procedure:

- Specifications
- Diagrams for function and timing
- Preliminary power dissipation calculations
- Manual pre-placement, prior to automatic placement (optional)

SPECIFICATIONS

Design specifications for a gate array option are established in two stages. The first (objective specification) details performance goals. The second (final specification) is derived from the objective specification after simulation and testing. Both are described in the following paragraphs.

Objective Specification

The objective specification is a statement of the performance goals to be met and includes the following:

- A functional block diagram and explanation of the logic circuitry
- AC specifications, timing diagrams and critical delay path definitions
- Bonding pad assignments and a logic pre-placement diagram (optional)
- Test vectors required for fault simulation (optional) and test grading
- Power dissipation requirements at system frequency
- Packaging requirements
- Marking specifications

VTI's application engineers are available to review the objective specification to verify that it is compatible with the capabilities of the VGC Series gate arrays. A final design review meeting will be held between the customer and VTI to complete the objective specification.

Final Specification

A final specification will be derived from the objective specification after logic simulation, test vector grading, placement, routing and simulation of the logic are completed. The final specification will be the objective specification modified by the post route simulation results.

LOGIC DESIGN

The designer should prepare a logic diagram and the test sequences necessary for logic simulation, fault simulation and test grading before starting the design. Having all the information listed above will help assure a rapid, error-free and more economical design. VTI will not normally review or in any way accept responsibility for the logical accuracy of the design.

The design will be reviewed only for testability, because VTI must be able to reliably test gate array options in a reasonable amount of time. If testability is not adequate, VTI may insist on additional test vectors and, possibly, the addition of circuitry to make the logic more testable.

FUNCTIONAL BLOCK DIAGRAM

A functional description of the logic system including a timing description must be prepared.

Requirements

This description should be a block diagram and a series of waveforms which illustrate the timing relationship required between the various inputs and outputs. A few paragraphs describing the operation of the logic option should also be supplied. VTI requires these items to assure that the gate array option may be tested properly and debugged, if necessary.

An Example Design

An example of a functional block diagram for the circuitry on a gate array is shown in Figure 6-1. This diagram should be a condensed version of the complete logic diagram showing only the major functions of the circuit. All inputs and outputs are shown but similar functions are combined for simplification.

The 16-bit registered comparator (with mask) consists of two 16-bit buses, A (a bidirectional bus) and B. The comparator operates in two basic modes. In the FAST COMPARE mode, the A bus bypasses the register logic to achieve a fast A-to-B comparison. The other mode, REGISTERED COMPARE, allows a 16-bit word to be loaded into either a word or mask register. The word register latches a 16-bit word to the A side of the comparator. The source can be either the A or B bus. In addition, either the A or the B bus can be loaded into a mask register, which serves to mask unwanted bits out of the final comparison. The contents of the mask register can be read from the A bus by controlling the MASK REGISTER READ signal.

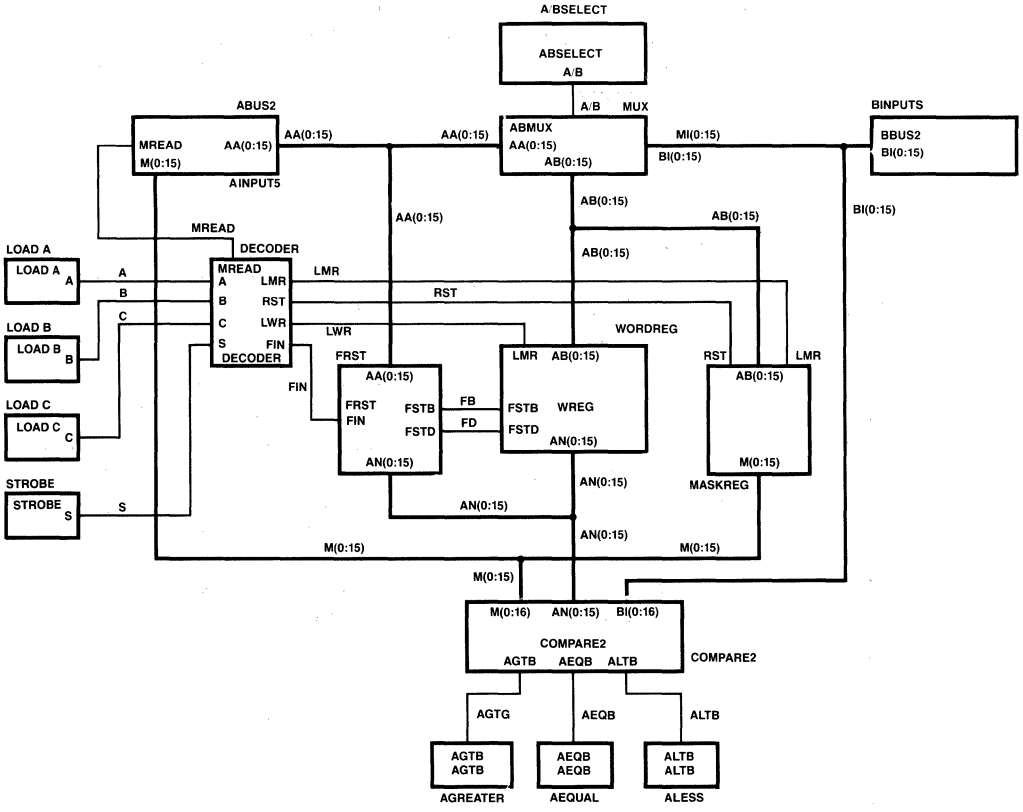


Figure 6-1. Block Diagram of an Example Circuit (16-bit Maskable Comparator)

Timing Diagrams and Definitions

In the objective specification, these diagrams should illustrate the delays between the various inputs and outputs which are required for proper operation of the gate array option. Critical or worst case delay paths should be defined as well as any propagation delay times that are specified for measurement during final electrical tests.

Estimating Propagation Delay Times

The delay time for a given path through a chain of macros can be estimated by using the propagation delay data presented in the sections, **Propagation Delay Calculations** and **Sample Calculations** in Chapter Five.

POWER DISSIPATION

Power Pins

The number of required power pins depends upon several factors: The size of the array, the utilization of the array, the operating frequency, and the number of simultaneously switching ouputs. The architecture of the power buses in the VGC series gate arrays is very good at isolating I/O noise from the internal core, however, it is recommended that all VDD and VSS locations be used in the arrays. This is particularly important for the 3200 and larger arrays when they are highly utilized and a large percentage of the circuitry operates above 10MHz. If you wish to use less than the total number of available VDD and VSS locations, you should consult with a VTI CAD applications engineer.

Additional VDD and VSS pins may be required in the case of simultaneously switching outputs. When an output switches from VDD to VSS a large instantaneous current will occur. This current in turn causes voltage spikes on the power buses. It is recommended that a VDD/VSS power pad pair be placed between each 8 outputs switching simultaneously.

Power Supply

CMOS arrays function over a wide range of supply voltage, the specific performance for the VGC series of arrays is guaranteed over a 4.5 to 5.5 volt range. The maximum range of the supply voltage is -0.5 to +6.0 volts. Outside this range permanent damage may occur to the arrays.

Power Dissipation Calculation

Total power dissipation is a function of the following:

1. Leakage current.

   This is the current flowing through reverse biased diodes. It is negligible.

2. Direct Current though turned on Transistors.

   This current can be itemized as follows:

   - TTL input levels at 2.0V. This current is difficult to specify. It depends heavily on processing. It can be the largest of the direct current through on transistors.
   - Gates whose inputs are left floating. In the VGC series arrays all unused inputs are tied off to prevent this situation from occuring.
   - Outputs which sink or source current.
   - A low on an input with a pullup resistor. The pullup resistors are in the hundreds of K Ohms range, so these currents will always be a very small component.

3. Crowbar effect.

   This current occurs during switching transitions. For a brief period when the input to a gate is switching, there will be a time when the input is at a voltage such that both the P and N devices are partially on causing DC current spike. This phenomenon account for roughly 10% of the power dissipation.

4. Switching Current.

   This current account for 90% of the power dissipated. The currents come from capacitors being charged up by the P devices and then discharged by the N devices. The formula for this power dissipation is:

   P= C * V * V * F

where C is the capacitance on the node,
V is the power supply voltage (5.5 Volts worst case),
and F is the frequency at which the node is switching.

For many of the macros this information is already calculated and given in the form of microwatts/MHz. All that needs to be done is to determine the frequency in MHz at which each particular macro switches, multiply this by the microwatt/MHz number given for the macro and add these up for all the macros. For the macros which do not have a microwatt/MHz number it is necessary to use the above power formula for all the nodes in the macro. A short cut would be to use the microwatt/MHz number from a similar macro.

Once this is done add 20% to the total power number to account for the three second order effects mentioned above.

A short cut would be as follows:

1. Determine the total number of utilized gates.

2. Assume all internal gates drive on the average 1pF.

3. Assume a worst case power supply of 5.5V.

4. Assume only 20% of the internal gates switch each cycle.

   Then for the core power dissipation the numbers for the power formula are:

   C = (20% of the Total utilized gates) * 1 pF
   V = 5.5V
   F = Master Clock Frequency

5. Assume power dissipation from outputs comes only from driving external loads.

   Then for the output power dissipation the numbers for the power formula are:

   C = Capacitance being driven by each output
   V = 5.5V
   F = Average frequency at which each output is switching

   This power number must be computed for each output and then summed together with the core power dissipation number to obtain the total power dissipation.

MACRO PRE-PLACE-MENT AND BONDING PAD ASSIGN-MENTS

Although the VTI gate array design system allows completely automatic placement, the designer may wish to manually pre-place some portion of the design. This is particularly true when the design contains critical delay paths, or when a fixed pinout is needed.

Input and I/O-cell macros must be manually placed to achieve a fixed pinout. The designer should determine the desired package pinout and then use bonding maps to determine the necessary die pinout. There are two other important considerations when determining pinout. The first impulse is to place related outputs (such as the lines of a data bus) together on the package. However, this can place together outputs which switch simultaneously and might require additional power pads. The second consideration is the placement of the remaining logic on the array. If the internal logic consists of independent or specialized blocks, the placement of these blocks should be considered when placing the I/O functions.

To minimize performance degradation due to capacitive loading in critical paths, the designer can manually place the components in these paths. Factors to consider are:

- Load factors of the components
- Transitions (HL, LH) in the path

All inputs and outputs of on-chip buses should be placed as closely together as possible to reduce the capacitance of the bus.

The only way to guarantee placement of macros in a specified location is to manually pre-place them. Any component can be manually pre-placed. If a partial manual pre-placement is done, the automatic placer will complete the task without disturbing those which were manually placed.

The automatic placer is unlikely to improve upon routing from a good manual placement. Such an improvement would need many iterations and some interactive designer intervention.

Macro placement should be governed by these criteria:

- Work around the required pinout
- Minimize interconnect length
- Minimize wiring congestion
- Conserve routing tracks

The first two criteria often conflict with each other so a compromise is usually necessary. Minimizing wiring length requires that macros with associated functions be clustered. If the macros involved utilize all of their I/O pins, wiring will be congested and pins will be blocked.

Macro Pre-Placement Diagram

A special plot of the gate array is used to perform a manual pre-placement of macros. This plot includes the following features:

- Bonding pad locations and numbers
- Voltage and ground pad designations
- A definition of all cell locations

Pre-Placement Procedure

The steps in the macro pre-placement procedure are:

1. Assign I/O functions to specific bonding pads if their location is pre-determined.
2. Place macros which connect directly to an I/O buffer or bonding pad near that pad.
3. Place macros in critical speed paths to minimize interconnect length.
4. Place the remaining macros in as logical a manner as possible to minimize interconnect length.

CHAPTER 7

TESTABILITY

INTRODUCTION

Incorporated into the VGC Series (excluding the VGC0500) are Design For Testability (DFT) features that enhance testability and simplify device testing. Two major DFT features are available.

The first DFT scheme, which is automatically available on all VGC-Series arrays (except the VGC0500), consists of three tests: output-buffer parametric tests, DC functional tests and an AC monitor test. Each gate array has three dedicated pads for these tests. Figure 7-1 summarizes these tests and Figure 7-2 shows the three test pads.

The second DFT scheme is called Level-Sensitive Scan Design (LSSD)* and is described in the final portion of this chapter. It is a structured testing method that simplifies testing of complex sequential circuits. LSSD must be designed into the gate array option using VTI gate array design system.

* IBM Patent Number 3783254, January 1, 1974.

Type	Inputs TEST	TOE	TDAT	Output ACOUT	Tests Performed	Description
Output Buffer Parametric Tests	1	X	1	Disabled		Normal Operation Test Data signal TDAT appears on all outputs
	0	0	TDAT	Disabled	VOH,VOL,IOH,IOL	
	0	1	0	Enabled	3-State Leakage	All outputs in 3-state mode
	0	1	1	Disabled	Standby Current	Measurement of static power dissipation
DC Functional Tests	1	X	0	Disabled	Jam Reset	Resets all flip-flops to a LOW state
	1	CK	0	Disabled	Scan Test	Allows data to be serially scanned into all flip-flops
AC Monitor	0	1	0	Enabled	Ring Oscillator frequency	Enables on-chip ring oscillator to monitor AC performance

Figure 7-1. Testing and Testability Summary

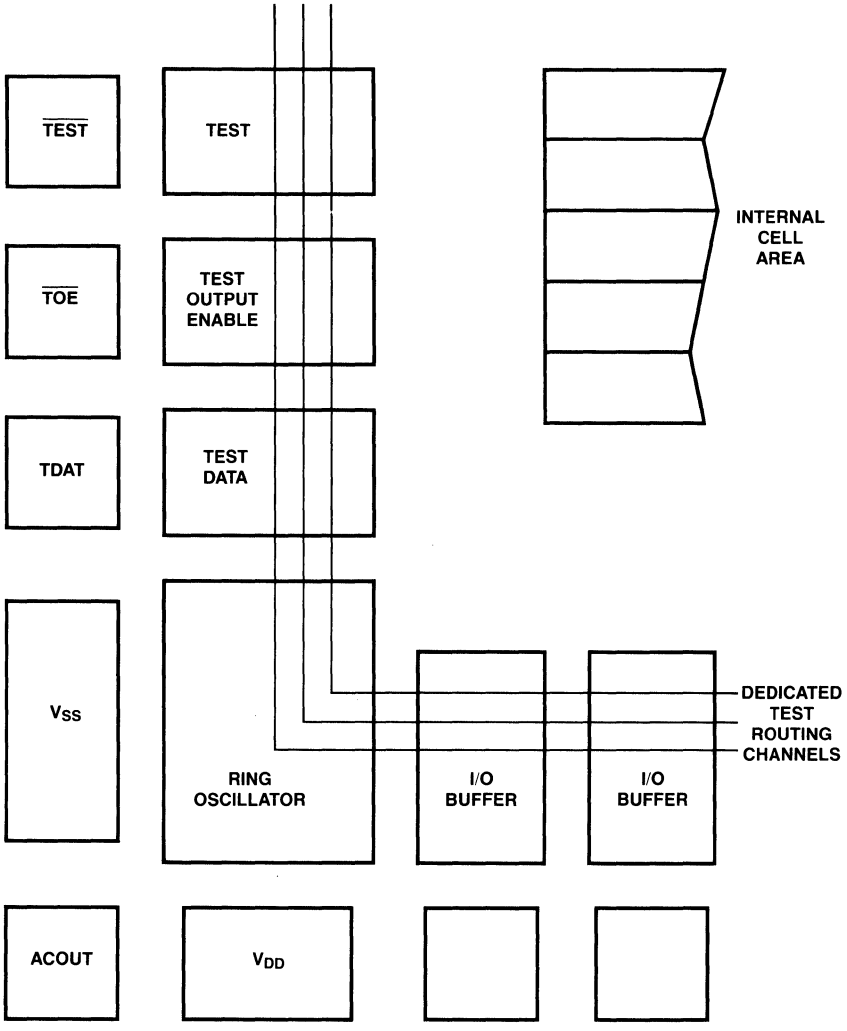


Figure 7-2. Dedicated Test Pads

STANDARD TESTING FEATURES

The following tests are available for all gate arrays in the VGC Series except the VGC0500. They are implemented by bonding to the appropriate test pads (shown in Figure 7-2).

Output Buffer Parametric Tests

The output buffer parametric tests allow DC data to be measured on all outputs by controlling the three dedicated test pins, TEST Bar, TOE Bar (Test Output Enable) and TDAT (Test Data). This feature avoids the need for a lengthy test program to force outputs into the correct state for parametric testing. The outputs are forced to HIGH, LOW, or 3-state conditions. VOH, VOL, IOH, IOL, 3-state leakage and static power dissipation can then be measured. More details of this test are shown in Figure 7-3.

DC Functional Tests

Pins TDAT and TOEN can be used to:

- JAM RESET – TDAT will set all flip-flops to zero
- SCAN TEST – TOEN will act as the scan test clock

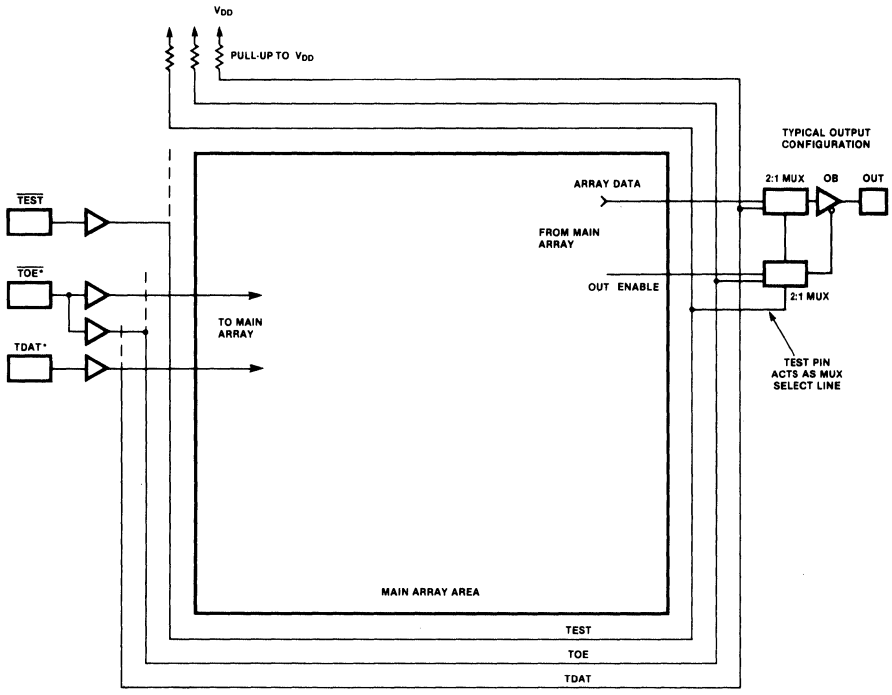
System initialization is greatly simplified by the JAM RESET shown in Figure 7-4. All flip-flops in a design can be simultaneously reset to zero, thereby reducing the complex task of testing sequential circuits to the simpler task of testing combinatorial circuits. This avoids long vector sequences to initialize a device into a known state.

AC Monitor Test

An on-chip ring oscillator is provided as an indicator of the AC performance of each device. The frequency is monitored by VTI at the wafer level as part of the outgoing test procedure. This signal may also be bonded out at the expense of an I/O pad and used as an incoming customer acceptance criterion. Figure 7-5 illustrates this test.

total pin overhead: 2

(Dedicated pins TEST & TDAT)



* TOE = Test Output Enable
* TDAT = Test Data

For Normal Operation

TEST = 1 & TOE Pin in usual array input mode

For Output Buffer Parametric Tests

TEST = 0, TOE = 0 or 1 For 3-state Enable or Disable Operation.
TDAT = 0 or 1 For VOL or VOH Tests On The Output Buffers.

Figure 7-3. Output Buffer Parametric Testing Scheme

```
*TOE  = Test Output Enable
*TDAT = Test Data

Before Functional Testing, TEST = 1 and TDAT = 0
------------------------------------------------
```

- JAM RESET resets all internal flip-flops.
- Sequential circuit can then be looked at as a simpler combinational logic circuit.
- Has minimum impact on the macro design of internal flip-flop
- Rapid functionality testing for limited coverage can be achieved with this scheme.

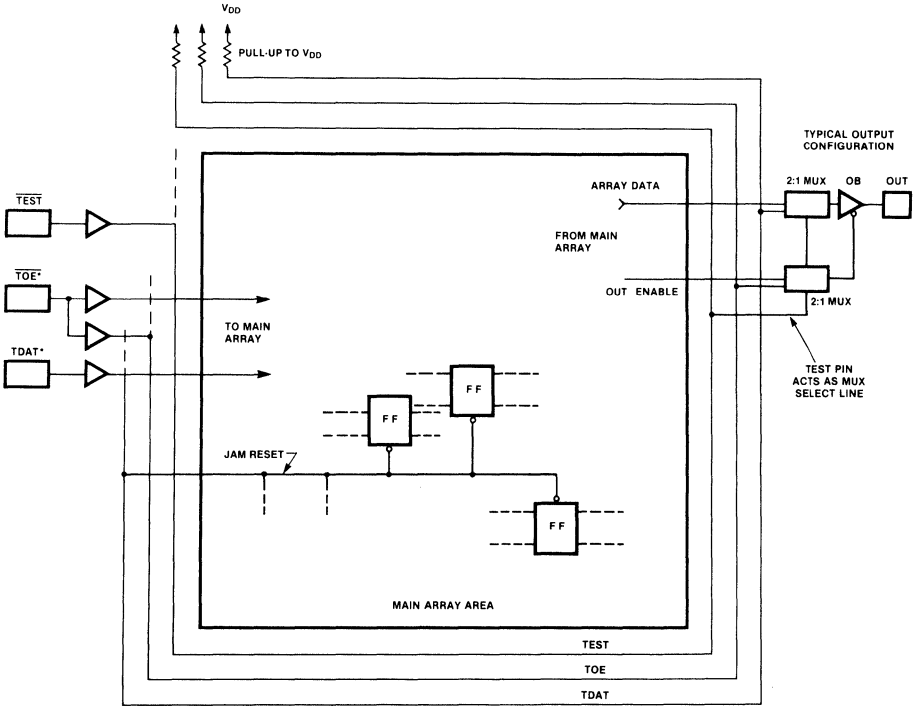
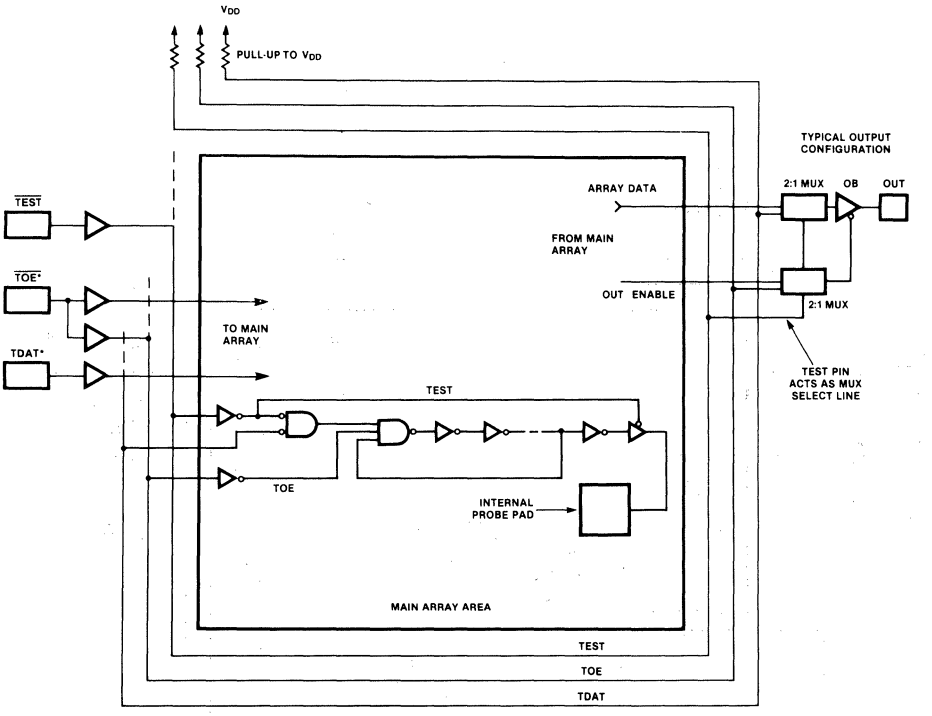


Figure 7-4. JAM RESET for Functional Testing




```
*TOE  = Test Output Enable
*DATA = Test Data

TO ACTIVATE AC MONITOR:
-----------------------

TEST/ = 0
TDAT  = 0
TOE/  = 1
```

Figure 7-5. Ring Oscillator AC Monitor Scheme

LEVEL SENSITIVE SCAN DESIGN

Level-Sensitive Scan Design (LSSD) is another testing scheme available for the VGC Series. It is a structured approach that must be designed into the gate array option. LSSD takes the form of extra hardware on the chip that can control the states of the macros. This hardware takes up approximately 20% of the chip area, but helps solve the huge problem of VLSI testing.

Definition

LSSD is a combination of two strategies:

Level-Sensitivity means that a logical network operates independently of internal circuit delays. VTI gate array design rules specify this effect.

Scan Design means that sequential elements have an auxiliary mode that lets them be connected as a shift register.

Operation

LSSD reduces sequential network testing to the much simpler task of combinatorial logic testing by controlling and observing the latches on the chip. Algorithms for thoroughly testing a combinatorial network are much easier to write and execute than those required to test a sequential network.

Test patterns can be obtained from the VTI gate array design system or pseudo-random patterns can be used. LSSD requires VTI gate array design system support to generate patterns and determine the fault coverage or to determine the coverage of pseudo-random patterns. LSSD also requires more silicon area than other, less structured, testing techniques. VTI gate array design system determines that area.

Tests

The following tests are possible with LSSD:

- Logic Analyzer:
  Array I/O pins are monitored during system operation with no interference to normal operation.

- Static Chip Test
  Array inputs are held in a desired static state while the resulting array outputs are gated to the output register. This allows specific test cases to be injected into array inputs and the resulting output states to be monitored during wafer, chip and system test.

- Dynamic Signature Analysis Chip Test
  Array inputs are sequenced through a series of repeatable pseudo-random patterns and the resulting outputs are accumulated into a checksum for rapid checking against known quantities.

Summary

LSSD provides a high-level testing methodology. Because every latch can be loaded and unloaded by shifting or addressing, design and debugging are simplified.

CHAPTER 8

USER GUIDELINES

INTRODUCTION

The characteristic susceptibility of CMOS to latch-up and electrostatic discharge are discussed in this chapter. Background technical information, VTI design features to avoid the problems and guidelines for safe design and handling are all presented.

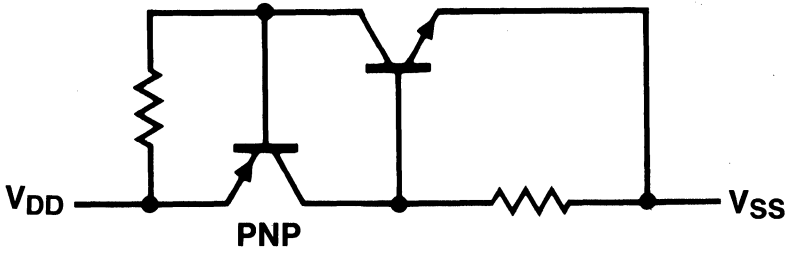
LATCH-UP

CMOS devices are intrinsically susceptible to the self-destructive state called latch-up. An excessive current accompanied by a collapsing or low-voltage condition, latch-up usually disrupts the circuit's logic function and often causes permanent damage by shorting the power supply or burning out the chip.

CAUSES OF LATCH-UP

In CMOS circuits, where both p-channel and n-channel MOS transistors are used, parasitic bipolar transistor structures exist due to different types of diffusions. In such parasitic four-layer PNPN devices, an NPN transistor coupled with a PNP transistor produces regenerative switching which allows large and uncontrolled current to flow. Figure 8-1 shows the cross-section of a p-well structure, after first metal and the corresponding circuit schematic of the parasitic transistors.

Latch-up starts when parasitic silicon-controlled rectifiers (SCRs) are triggered. There are two types of triggering: static and dynamic. Static triggering comes from the variations in operating voltages. Dynamic triggering comes from high-speed pulses and transients.



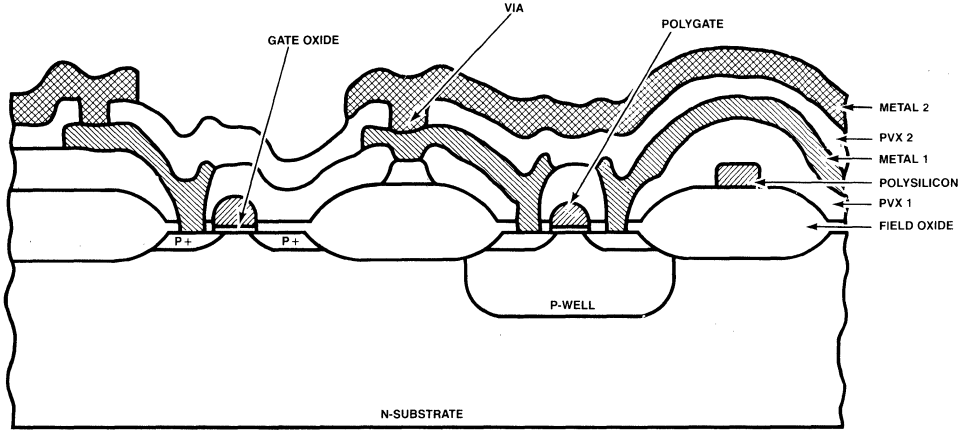


Figure 8-1. P-well CMOS Structure

One of the most common avenues for latch-up is provided by an input or output voltage greater than VDD or less than VSS. Normally, the vertical NPN transistor (formed by the n+ diffusion, p-well and n-substrate) and the lateral PNP transistor (p+ diffusion, n-substrate and p-well) are biased off. However, when unusually high currents are present in either n-substrate or p-well during switching or "power-on" actions, the emitter junctions become forward biased, turning on the PNPN structure. The only solution is to disconnect power from the device.

The problem of latch-up becomes more severe as chip patterns shrink and operating speeds increase. That means that even though latch-up can be avoided by external system design techniques, such fixes will be less effective.

In the end, there is no single technique for dealing with latch-up. In fact, as NMOS and bipolar patterns get smaller, they too begin to encounter latch-up problems. The only realistic conclusion is that designers must defend against latch-up from chip design, through processing, to final system design.

Latch-up Solutions

Design Related Solutions

VTI's CMOS gate arrays have been designed to minimize latch-up. The techniques employed include:

- Guard rings of VDD and VSS around large diffusion areas. These act as dummy collectors, or lateral blocking devices, to catch injected currents and reduce the gain (beta) of parasitic transistors. Figure 8-2 shows the layout of this protection network.
- Minimization of space between the p-channel device drain and substrate n+.
- Minimization of space between p-well contacts to ground and metal.

Process Related Solutions

The major process related solution is oxide isolation. This forces a longer current route for minority carriers between diffused regions, which in turn reduces the gain of the parasitic transistors. Heavily-doped epitaxial substrates also reduce substrate resistances, thereby minimizing latch-up.

Application Related Solutions

To avoid latch-up, take the following precautions during power-up:

- Do not allow inputs to go higher than VDD by 0.5 V or lower than VSS by 0.5 V.
- Regulate the power supply voltages with transient suppressing capacitors.
- Use clean waveforms for clock lines.

Latch-up most commonly occurs when inputs go higher than the power supply during power-up. Latch-up can cause immediate and severe damage to the array in a poor design. While VTI arrays are designed for immunity from such problems, power sequence should not be mixed: always connect ground first and then power up slowly. Avoid switching transients.

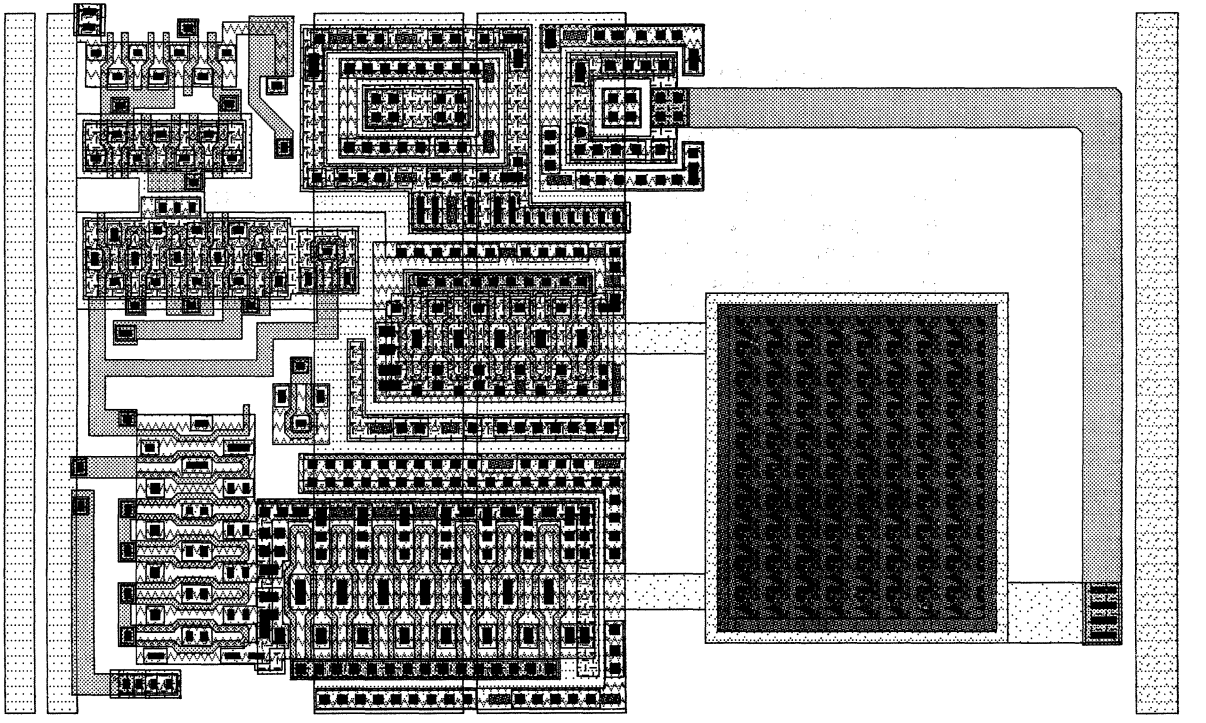


Figure 8-2. Protection Network Layout

ELECTROSTATIC DISCHARGE

All CMOS devices are susceptible to damage by electrostatic discharge into pins. This special sensitivity is caused by the high input impedance. In turn, the impedance is high because the input capacitance is in parallel with an extremely high input resistance. That makes it very easy for electrostatic charges to build up on the pins.

Where Static Charges Are Found

Static charges are always present in manufacturing. In fact, such charges are commonly present in any working environment. Such charges are frequently generated by friction. Walking across a floor, a worker may build a charge of several thousand volts. Working at a bench, sliding on a stool or picking up a tool can generate high static potentials. Higher humidity decreases static charges because moisture in the air provides a leakage path.

How Static Discharge Can Damage the Array

When static discharges, it can break down the extremely thin (approximately 300-500 Angstroms) gate oxide insulator beneath the gate on the transistors. The presence of defects in the gate oxide, such as pinholes or lattice defects, reduces the already low dielectric strength. The breakdown field can change as much as 100 times (from 8-10 million V/cm to 30-40 thousand V/cm). This dielectric strength is the voltage limiting factor for CMOS devices. If the voltage is too high, a permanent short can result.

Design Features to Deter Discharge

It is a common industry practice to use networks of diodes to protect against discharge damage. The diodes shunt surges around the circuit, restricting them from doing any damage. Figure 8-3 is a schematic of the input protection network used by VTI. This network is automatically built into every gate array option.

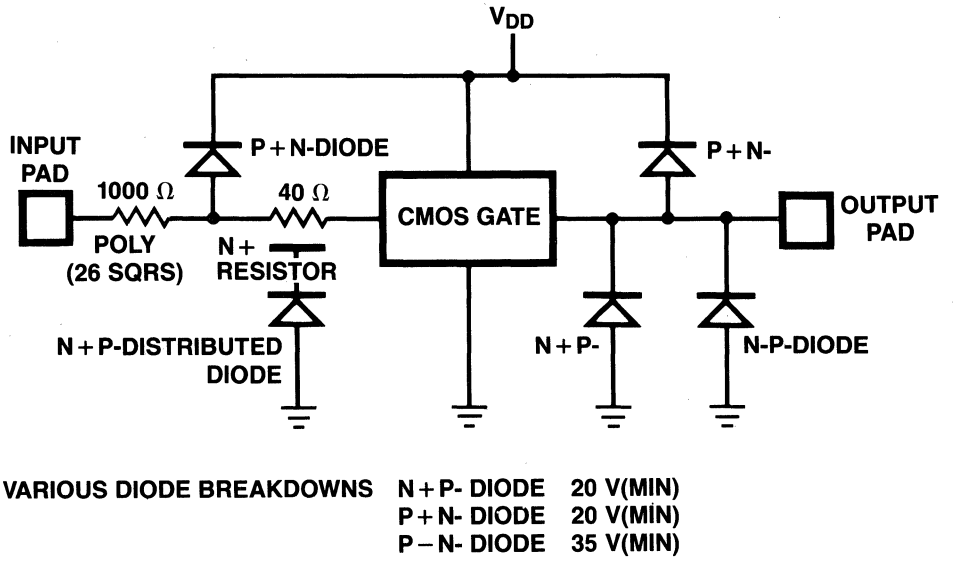


Figure 8-3. Diode Protection Network Schematic

Handling Rules to Avoid Discharge

Even the best protection design cannot save a CMOS device from the static charges common to manufacturing. Therefore, prevention is even more important than the protection that is built into the array. Furthermore, because prevention consists of simple steps, it should be a priority:

- Avoid differences in potential between pins.
- Use conductive carriers, foams, or rails for storage and transport.
- Ground soldering iron tips, metal fixtures, tools and workers.
- Insert or remove devices only with the power off.
- Cover tables with conductive tops and cover test area floors with conductive material.
- Make all personnel aware of static dangers.
- Use ionized-air blowers if necessary.

Important Design Practices

Good design practice will assure 100% working prototypes with shortest possible time. The following hints point out some potential pitfalls.

- All unused inputs should be tied to either VDD or VSS. This will assure that a floating input will not put a gate into a state where both transistors are "ON".
- Using DeMorgan's Theorem along with the logic conversion techniques will improve the speed of your array and reduce the gate count.
- Extra pins can be utilized to enhance the testability of a design and to add more functionality. Some of these extra pins may also be used as additional power and ground pins.
- Follow power pad design rules very carefully. Provide VDD and VSS pads at regular intervals to minimize spikes and ground noise.
- All pads on the array must interface through an I/O macro.
- Keep the system synchronous and thus predictable. The fact that the delay paths are not predefined makes asynchronous paths hard to predict.
- Internal buses takes up a lot of routing area and should be accounted for,

especially for arrays that are highly utilized.

- Avoid monostable, one-shot, on-circuit capacitor and diode structures.
- Internal buses must always be defined. a floating bus may result in propagation of an incorrect logic state.
- Run simulation on the entire array before releasing it to VTI for placement and routing.

CHAPTER 9

PACKAGING

INTRODUCTION

This chapter describes the packaging options for the VGC series. A wide range of package styles and lead counts including DIP, Pin Grid Array, Leadless Chip Carrier and Leaded Chip Carrier will be offered. Custom packages are available in some circumstances.

The next section briefly describes several of the packages while the section after that lists advantages and disadvantages of the various package types.

Detailed drawings of some packages and of mounting methods, appear as figures in the last section at the end of this chapter.

INDIVIDUAL PACKAGE DESCRIPTIONS

This section of the manual describes several of the most popular packages.

84-Terminal Ceramic Chip Carrier

This package is a multi-layer ceramic JEDEC Type D Leadless Chip Carrier with a glass hermetic seal. The package can be provided with either the cavity-up or the cavity-down configuration.

If this package is surface mounted on a printed circuit board, the cavity-up configuration must be used to place the heat radiating surface of the package next to the mounting surface. If the Leadless Chip Carrier is mounted in a socket, either the cavity-up or the cavity-down configuration can be used.

PACKAGE CONSIDERATIONS

No single package type is superior for all applications. Use the following list of advantages and disadvantages when you choose a package for your gate array. A point to remember is that a larger number of pins means a higher cost, no matter which package you choose.

PACKAGE TYPES AND SIZES

DIP

- Predominant style for fewer than 64 leads
- Ceramic is available for hermetic and low volume applications
- Plastic is available for high volume, cost sensitive applications

Pin-Grid Array

- 68 to 172 leads
- High pin density
- Integrates easily with existing PCB technology

- Hermetic and non-hermetic versions are available

Leadless Chip Carrier

- 44 to 84 leads
- Plastic Quadpak (44 leads) is low cost
- Socketable ceramic versions (68 or 84 leads) are available
- Surface mount ceramic versions (84 leads) are available
- Good thermal conductivity

Leaded Chip Carrier

- 84 to 172 leads
- 0.050" and 0.025" centers
- Attractive, low cost, high lead count, hermetic package

PACKAGE DIAGRAMS

Figures 9-1, 9-2 and 9-3 show some of the critical dimensions of Leadless Chip Carriers, DIPs and S/B packages. Figures 9-4 and 9-5 show the dimensions of a popular type of connector/socket for Leadless Chip Carriers and Pin Grid Array packages.

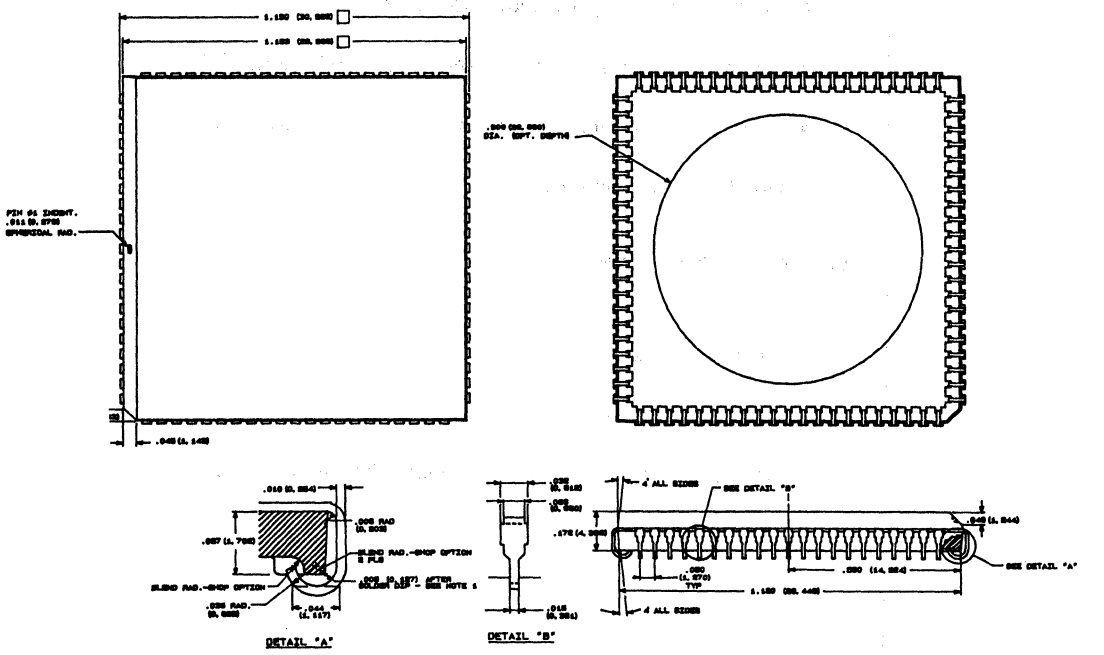


Figure 9-1. 84 Plastic Leadless Chip Carrier

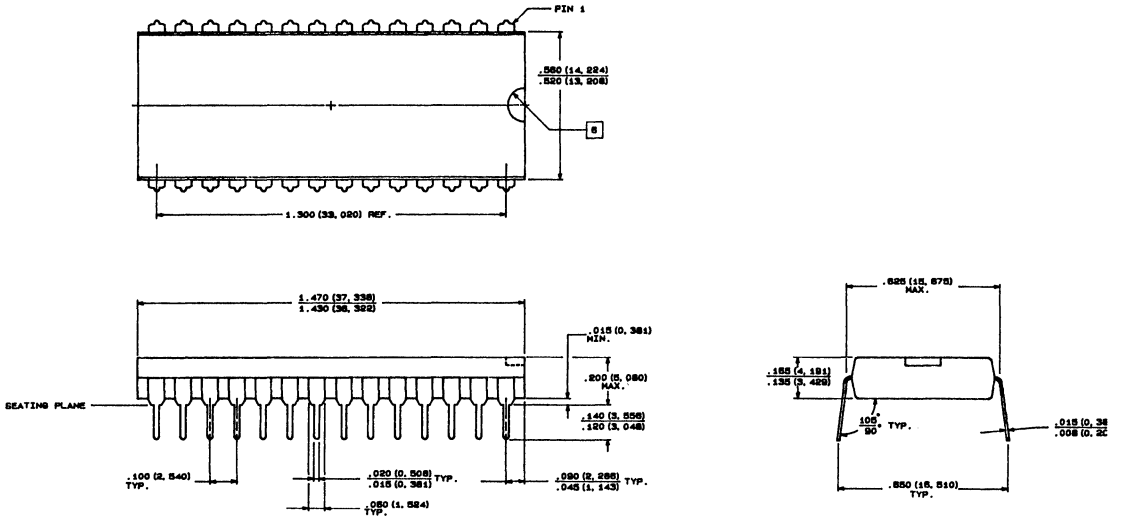


Figure 9-2. 28 Lead Molded Package

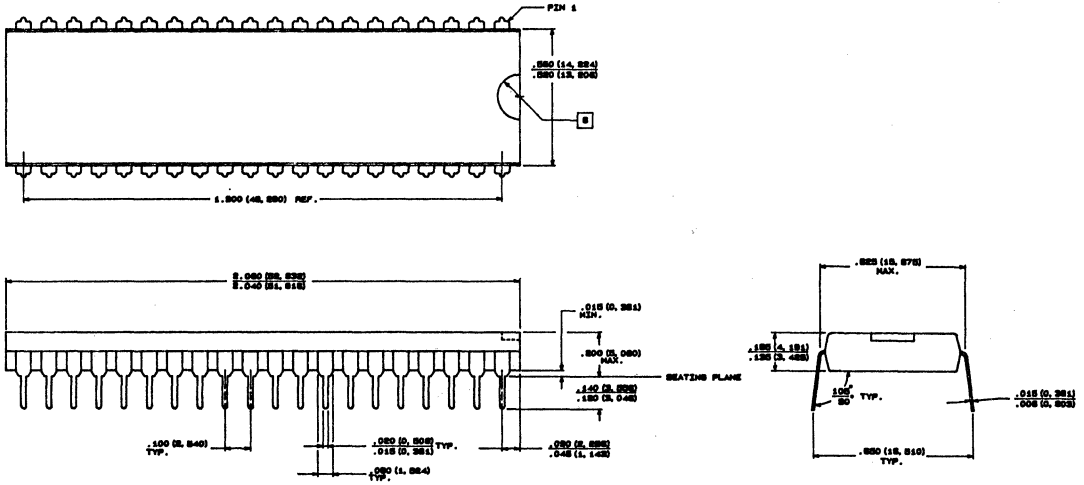


Figure 9-3. 40 Lead S/B Package

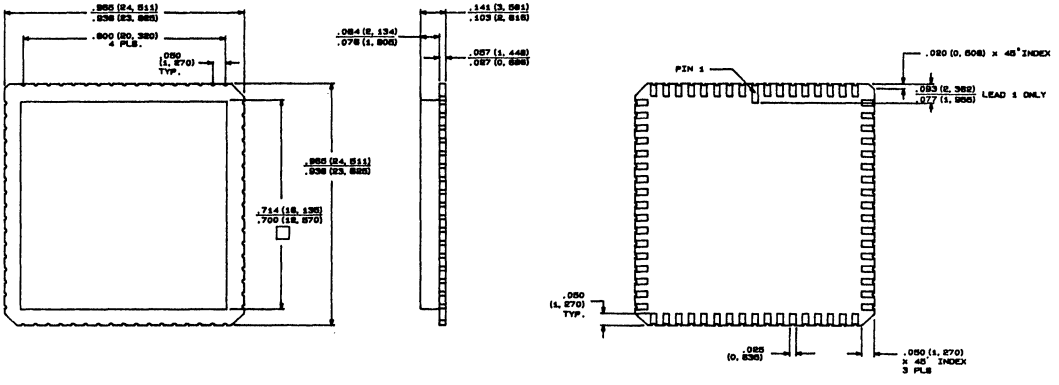


Figure 9-4. 68-Lead Leadless Chip Carrier

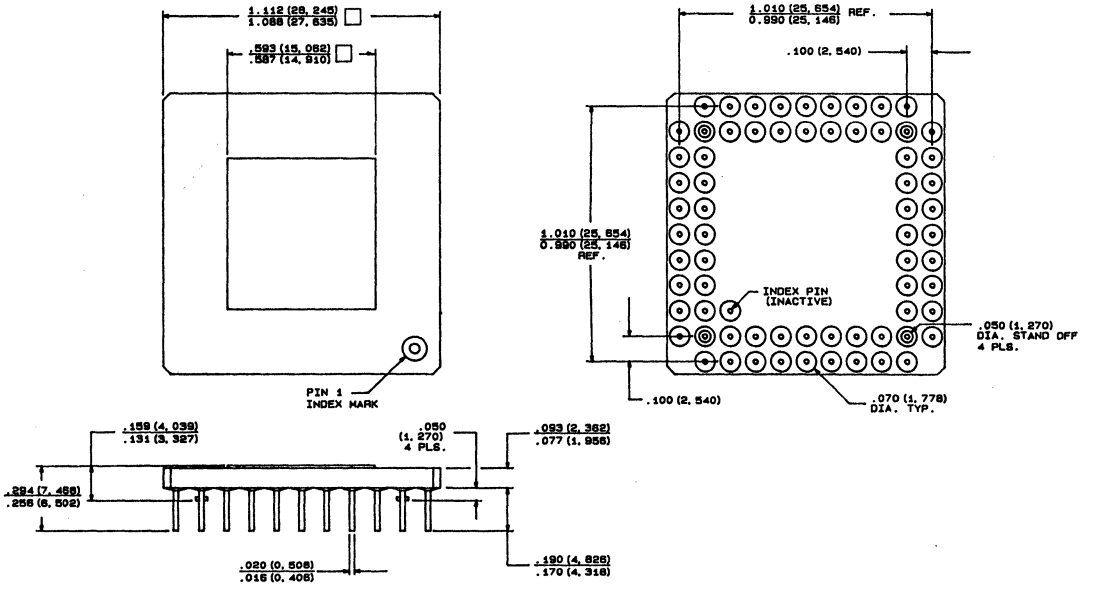


Figure 9-5. 68-Lead Pin Grid Array Package

APPENDIX A

MACRO LIBRARY

TABLE A-1: VGC SERIES MACRO LIBRARY

INTERNAL CELL MACROS

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION	PAGE NO.
BASIC GATES			
NA02	1	2-NAND	127
NA02I	1	2-NAND & INVERTER	130
NA03	1	3-NAND	133
NA04	2	4-NAND	136
NA05	2	5-NAND	139
NA05I	3	5-NAND & INVERTER	142
NA06	2	6-NAND	145
NOR02	1	2-NOR	148
NOR02I	1	2-NOR & INVERTER	151
NOR03	1	3-NOR	154
NOR04	2	4-NOR	157
AND02	1	2-AND	160
OR02	1	2-OR	163
X2NA04	3	DUAL 4-INPUT NAND	166
INVERTERS/BUFFERS			
INV11	1	DUAL 1X INVERTERS	169
INV12	1	INVERTERS (1X and 2X)	172
INV03	1	INVERTERS (3X)	175
BUF02	1	NON-INVERTING INTERNAL BUFFER, 2X	178
INV01T	1	3-STATE INVERTER (INTERNAL,1X)	181
INV02T	2	3-STATE INVERTER (INTERNAL,2X)	184
INV03T	3	3-STATE INVERTER (INTERNAL,3X)	187
COMPLEX GATES			
XOR02	2	2-IN EXCLUSIVE-OR	190
XNOR02	2	2-IN EXCLUSIVE-NOR	193
XNOR021	2	2-IN EXCLUSIVE-NOR	196
AOI21	1	2-1 AND-OR-INVERTER	199
OAI21	1	2-1 OR-AND-INVERTER	202
AO22	2	2-2 AND-OR W/COMP. OUTPUTS	205

INTERNAL CELL MACROS (continued)

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION	PAGE NO.
COMPLEX GATES (continued)			
AOI222	2	2-2-2 AND-OR-INVERTER	208
AOI22I	2	2-2 AND-OR-INVERT & 2X INV.	211
AOI33	2	3-3 AND-OR-INVERTER	214
LATCHES			
LA01	3	BUFFERED LATCH,	217
LAE01	3	D-LATCH	220
LAE01T	4	W/3-STATE OUTPUT	223
LAE01S	5	W/SCAN LOGIC	226
LA02	3	W/CLEAR, BUFFERED OUTPUTS	229
LAE02	3	W/CLEAR	232
LAE021	2	W/CLEAR, EXTERNAL ENABLE	235
LAE021T	3	W/CLEAR, EXTERNAL ENABLE & 3-STATE OUTPUTS,	238
MEM01	3	GATED W/3-STATE OUTPUT	241
MEM02	3	GATED W/3-STATE OUTPUT	244
FLIP FLOPS			
DFP01	4	D FLIP-FLOP	247
DFP74	6	W/SET, CLEAR	250
DFP011	4	W/EXTERNAL CLOCKS	253
DFP011T	4	W/3-STATE OUTPUT, EXT. CLK	256
DFP01S	6	W/SCAN LOGIC	259
DFP02	5	W/CLEAR DIRECT	262
DFP021	4	W/CLEAR, EXTERNAL CLOCKS	265
DFP021T	5	W/CLEAR, EXTERNAL CLOCKS, 3-STATE OUTPUT	268
DFP02S	7	W/SCAN, CLEAR	271
DFP03	5	W/SET	274
DFP031	4	W/SET, EXTERNAL CLOCKS	277
DFP04	6	W/SET, CLEAR	280
DFP05	4	W/BUFFERED OUTPUT	283
JKN02	7	JK FLIP-FLOP W/ CLEAR	286
JKN76	8	JK FLIP-FLOP	289
TF02	5	TOGGLE FLIP-FLOP W/CLEAR	292

INTERNAL CELL MACROS (continued)

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION	PAGE NO.
MULTIPLEXERS/DECODERS			
MX02	3	2 TO 1 MULTIPLEXER (MUX)	295
MX04	5	4 TO 1 MUX	298
MXE04	6	4 TO 1 MUX (1/2 74153)	301
MXE041	5	4 TO 1 MUX W/ENABLE	304
DC24	4	1 OF 4 DECODER	307
DC139	7	1 OF 4 DECODER, W/ENABLE	310
MISC. MACROS			
ADD01	6	1-BIT FULL ADDER	313

EXTERNAL CELL MACROS

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION	PAGE NO.
INPUT BUFFERS			
IOT01F	1	TTL INPUT BUFFER, VGC0500	316
IOT01	1	INPUT BUFFER	319
IOT011F	1	INPUT BUFFER W/PULL-UP, VGC0500	322
IOT011	1	INPUT BUFFER W/PULL-UP	325
IOC01F	1	CMOS INPUT BUFFER, VGC0500	328
IOC01	1	INPUT BUFFER	331
IOC011F	1	INPUT BUFFER W/PULL-UP, VGC0500	334
IOC011	1	INPUT BUFFER W/PULL-UP	337
IOT04	1	TTL INPUT BUFFER; 4:1 RATIO	340
IOT041	1	TTL INPUT BUFFER W/PULL-UP, 4:1 RATIO	343

EXTERNAL CELL MACROS (continued)

EXPLANATION OF VGC SERIES PROPAGATION DELAY VALUES

Delay Conditions

The macro propagation delay values are given for typical, industrial worst case, and military worst case conditions. These conditions are defined below:

Typical:
`Typical process, TA = 25 deg C, VDD = +5.0V`

Industrial worst case:
`Worst-case process, TA = 85 deg C, VDD = +4.5V`

Military worst case:
`Worst-case process, TA = 125 deg C, VDD = +4.5V`

Junction temperature (TJ) of a device is always higher than the ambient temperature (TA) and is a function of the heat dissipation capability of the package and the power consumption of the device.

Input Edge Rates

The input edge rates (tr, tf) are assumed as follows for all conditions:

TTL Input Buffers	6.25 ns
CMOS Input Buffers	3.125 ns
All Internal Macros	2.5 ns
Output Buffers	2.5 ns

Macro Delays

The macro delays are specified as a base delay and a normalized load factor for both HIGH-LOW and LOW-HIGH transitions. The base delay represents the macro delay with no additional load capacitance. The delay due to loading is found by multiplying the normalized load factor (ns/UL) times the Unit Load. See Chapter 5 of the Design Manual for sample calculations.

AC PARAMETER DEFINITIONS

fmax
Toggle Frequency - The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

tPLH
Propagation Delay Time, LOW TO HIGH - The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

tPHL
Propagation Delay Time, HIGH TO LOW - The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

tW
Pulse Width - Time between 50% amplitude points on the leading and trailing edges of a pulse.

tH
Hold Time - The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

tS
Setup Time - The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recog- nized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

tPHZ
Output Disable Time From HIGH Level - The time between the specified reference points on the control input and output voltage waveforms, with the output changing from the defined HIGH level to a high impedance state.

tPLZ
Output Disable Time from LOW Level - The time between the specified reference points on the control input and output voltage waveforms, with the output changing from the defined LOW level to a high impedance state.

tPZH Output Enable Time to HIGH Level - The time between the specified reference points on the control input and output voltage waveforms, with the output changing from a high impedance state to the defined HIGH level.

tPZL
Output Enable Time to Low Level - The time between the specified reference points on the control input and output voltage waveforms, with the output changing from a high impedance state to the defined LOW level.

tREL
Release Time - The time between the specified reference point on the trailing edge of an asynchronous input control pulse and the leading edge of a synchronous input pulse such taht the function will respond to the synchronous input.

tr
Rise Time

tf
Fall Time

FUNCTION TABLE NOTATION

The following symbols are used in function tables on the data sheets:

L	= LOW level	Q	= Present state of Q
H	= HIGH level	QN	= Present state of QN also compliment of Q
⌐	= LOW to HIGH transition		
⌙	= HIGH to LOW transition	Z	= Output disabled state
X	= Any level (Don't Care)		

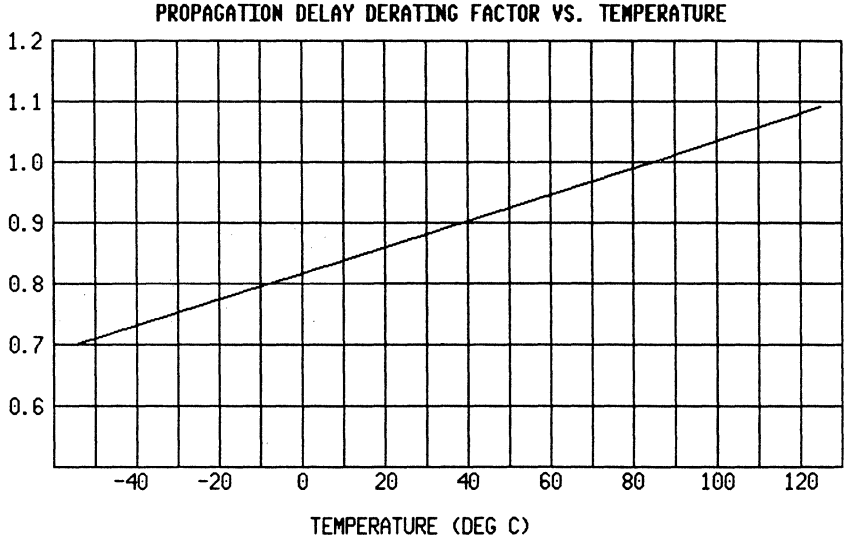
DERATING FACTORS FOR PROPAGATION DELAYS

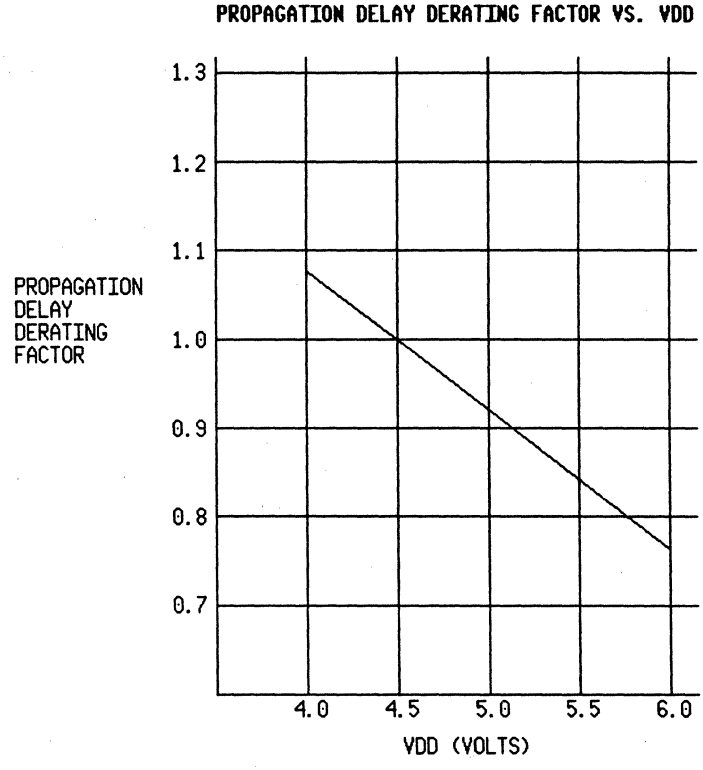
To obtain the propagation delays for conditions different than specified, use the following equation:

```
tDELAY(new) = tDELAY(data sheet) * kT * kV * kP

kT = derating factor for Temperature
kV = derating factor for Voltage (VDD)
kP = derating factor for Process
```

EXAMPLE

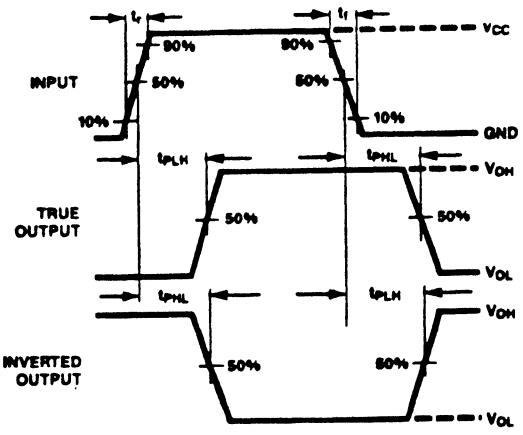
```
Conditions:  junction temperature = 27 deg C
             VDD = 5.0 V, typical process
             tDELAY(data sheet) = 5.0 ns

tDELAY(new) = 5.0 * 0.87 * 0.92 * 0.82 = 3.3 ns
```



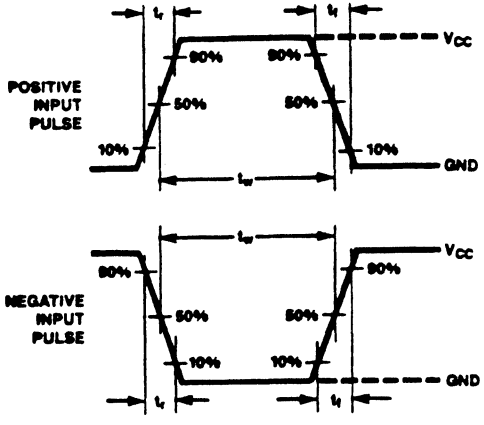


PROPAGATION DELAY DERATING FACTOR VS. PROCESS

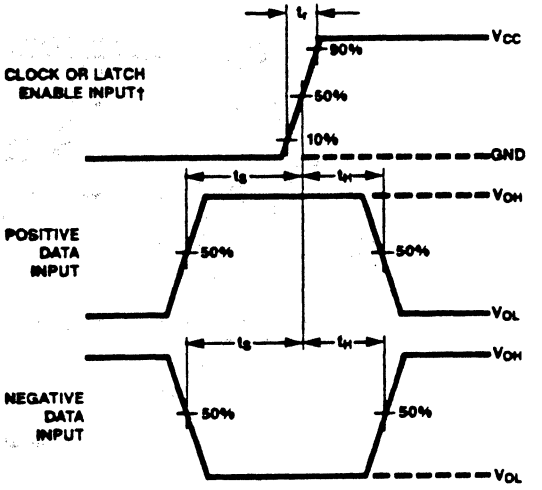
PROCESS	FACTOR
SLOW	1.00
TYPICAL	0.82
FAST	0.66



Propagation Delay Waveforms

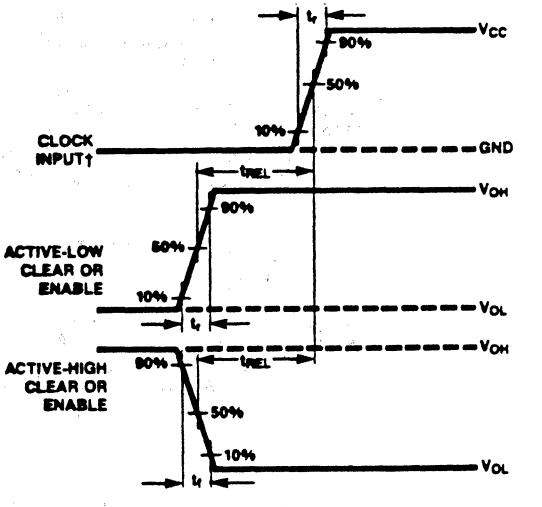


Input Pulse Width Waveforms

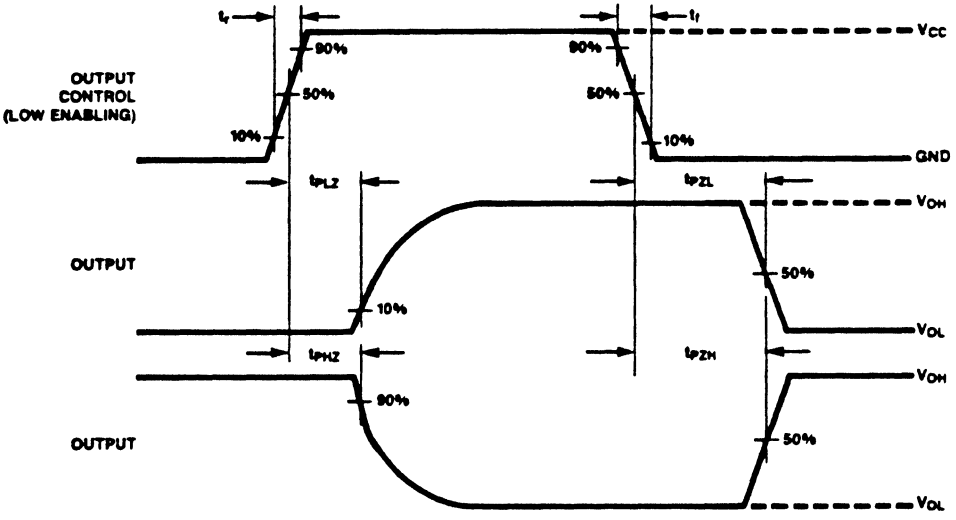


Setup and Hold Time Waveforms

†Waveform for negative edge sensitive circuits will be inverted.



Release Time Waveforms



3-State Output Enable and Disable Waveforms

APPENDIX B

VGC SERIES DATA SHEETS

NA02

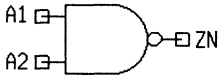
2-INPUT NAND GATE

DESCRIPTION

The NA02 combines inputs A1 and A2, to provide the NAND function at output ZN.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS	OUTPUTS
A1 A2	ZN
L X	H
X L	H
H H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
ZN	Output	-	Data Output

NA02

2-INPUT NAND GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A2->ZN	1.0 + 0.7 + 0.26 * UL	0.2 + 0.6 + 0.21 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

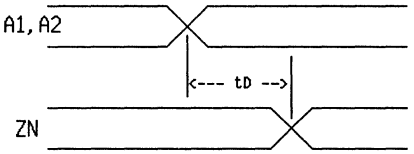
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.0	1.0	2.2	1.2	3.0	1.9	4.3	2.9

Note: For other operating conditions, use derating curves given in the performance section.

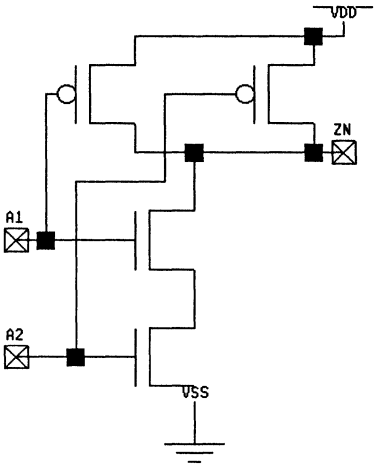
NA02

2-INPUT NAND GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



NA02I

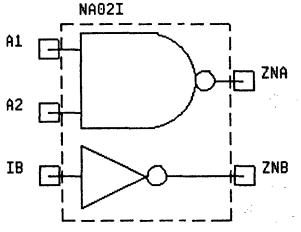
2-INPUT NAND GATE PLUS INVERTER

DESCRIPTION

The NA02I combines a 2-Input NAND gate with an inverter, in one macro. If either of the gates are unused, their input(s) must be tied to VDD or VSS.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT	INPUTS	OUTPUT
A1	A2	ZNA	IB	ZNB
L	X	H	L	H
X	L	H	H	L
H	H	L	-	-

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	NAND Gate Input
A2	Input	1.0	NAND Gate Input
ZNA	Output	-	NAND Gate Output
IB	Input	1.0	INVERTER Input
ZNB	Output	-	INVERTER Output

NA02I

2-INPUT NAND GATE PLUS INVERTER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDA, A2->ZNA	0.9 + 0.5 + 0.26 * UL	0.3 + 0.4 + 0.21 * UL
tDB, IB->ZNB	0.5 + 0.5 + 0.19 * UL	0.1 + 0.2 + 0.07 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

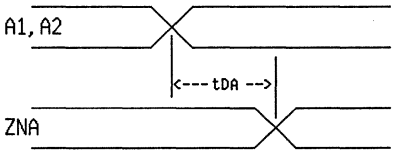
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDA	1.7	0.9	1.9	1.1	2.7	1.8	4.0	2.8
tDB	1.2	0.4	1.4	0.4	2.0	0.7	2.9	1.0

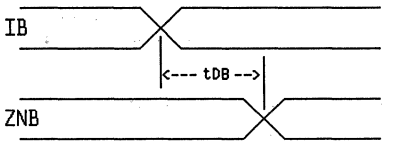
Note: For other operating conditions, use derating curves given in the performance section.

NA02I

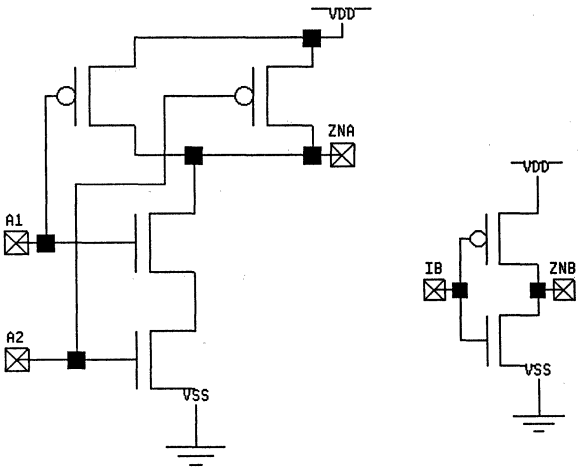
2-INPUT NAND GATE PLUS INVERTER

AC CHARACTERISTICS (cont'd)





CIRCUIT DIAGRAM



NA03

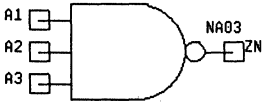
3-INPUT NAND GATE

DESCRIPTION

The NA03 combines inputs A1, A2, and A3 to provide the NAND function at the output ZN.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS	OUTPUTS
A1 A2 A3	ZN
L X X	H
X L X	H
X X L	H
H H H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
A3	Input	1.0	Data Input
ZN	Output	-	Data Output

NA03

3-INPUT NAND GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A3->ZN	1.0 + 0.8 + 0.26 * UL	0.2 + 0.9 + 0.28 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

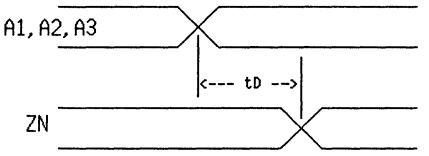
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.1	1.4	2.3	1.7	3.1	2.5	4.4	3.9

Note: For other operating conditions, use derating curves given in the performance section.

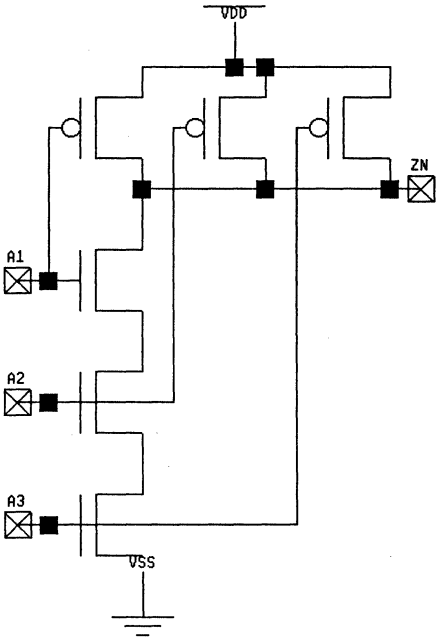
NA03

3-INPUT NAND GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



NA04

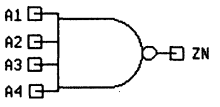
4-INPUT NAND GATE

DESCRIPTION

The NA04 combines inputs A1 through A4 to provide the NAND function at output ZN.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS
A1	A2	A3	A4	ZN
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
A3	Input	1.0	Data Input
A4	Input	1.0	Data Input
ZN	Output	-	Data Output

NA04

4-INPUT NAND GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A4->ZN	0.8 + 1.1 + 0.26 * UL	0.1 + 1.5 + 0.37 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

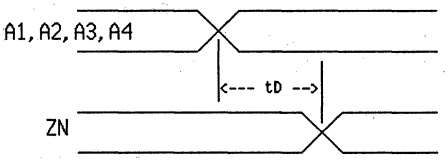
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.2	2.0	2.4	2.3	3.2	3.5	4.5	5.3

Note: For other operating conditions, use derating curves given in the performance section.

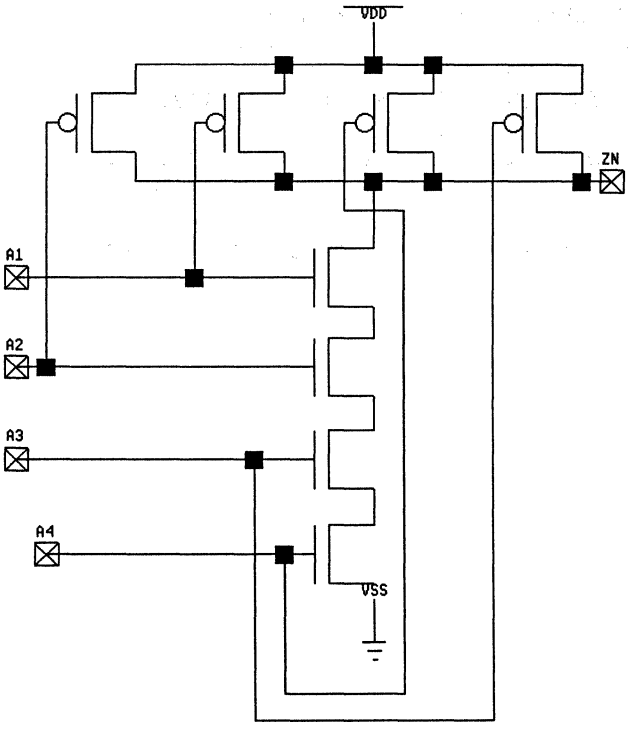
NA04

4-INPUT NAND GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



NA05

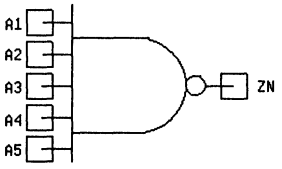
5-INPUT NAND GATE

DESCRIPTION

The NA05 combines inputs A1 through A5 to provide the NAND function at output ZN.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS					OUTPUTS
A1	A2	A3	A4	A5	ZN
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
A3	Input	1.0	Data Input
A4	Input	1.0	Data Input
A5	Input	1.0	Data Input
ZN	Output	-	Data Output

NA05

5-INPUT NAND GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A5->ZN	0.9 + 1.4 + 0.26 * UL	0.5 + 2.3 + 0.43 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

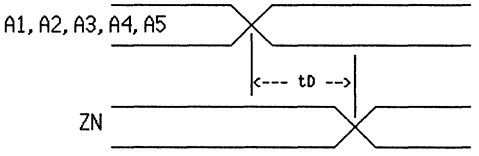
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.6	3.2	2.8	3.7	3.6	5.0	4.9	7.1

Note: For other operating conditions, use derating curves given in the performance section.

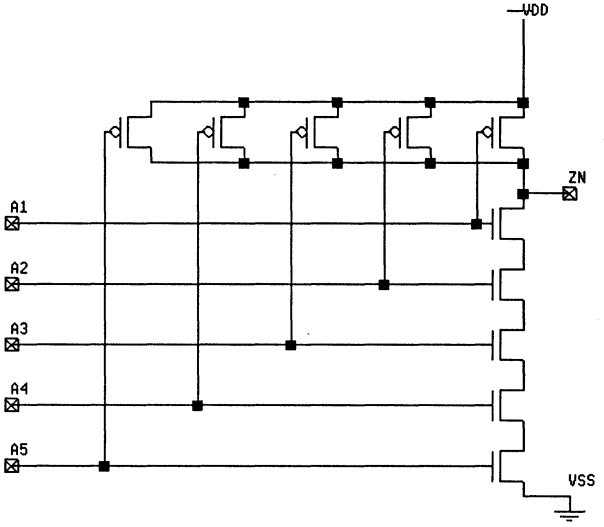
NA05

5-INPUT NAND GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



NA05I

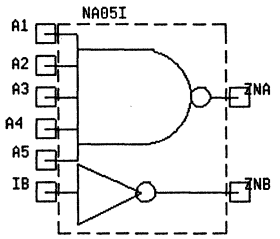
5-INPUT NAND PLUS INVERTER

DESCRIPTION

The NA05I contains two seperate functions: a 5-Input NAND gate and a single Inverter. If one of the functions is not used, the corresponding inputs must be connected to VDD or VSS bus.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS					OUTPUTS	INPUT	OUTPUT
A1	A2	A3	A4	A5	ZNA	IB	ZNB
L	X	X	X	X	H	L	H
X	L	X	X	X	H	H	L
X	X	L	X	X	H	-	-
X	X	X	L	X	H	-	-
X	X	X	X	L	H	-	-
H	H	H	H	H	L	-	-

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	NAND Data Input
A2	Input	1.0	NAND Data Input
A3	Input	1.0	NAND Data Input
A4	Input	1.0	NAND Data Input
A5	Input	1.0	NAND Data Input
IB	Input	1.0	Inverter Data Input
ZNA	Output	-	NAND Data Output
ZNB	Output	-	Inverter Data Output

NA05I

5-INPUT NAND PLUS INVERTER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDA, A1->ZNA	3.1 + 0.6 + 0.26 * UL	3.8 + 0.4 + 0.17 * UL
tDB, IB->ZNB	0.5 + 0.5 + 0.19 * UL	0.1 + 0.2 + 0.07 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

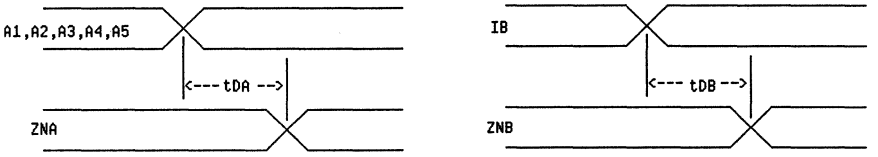
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDA	4.0	4.4	4.2	4.5	5.0	5.1	6.3	5.9
tDB	1.2	0.4	1.4	0.4	2.0	0.7	2.9	1.0

Note: For other operating conditions, use derating curves given in the performance section.

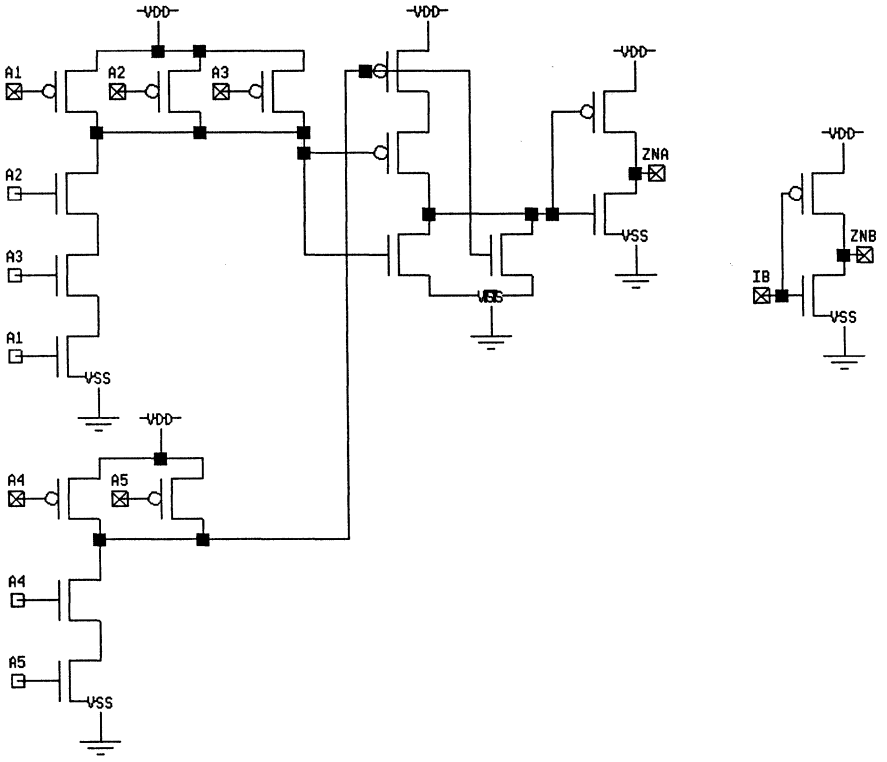
NA05I

5-INPUT NAND PLUS INVERTER

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



NA06

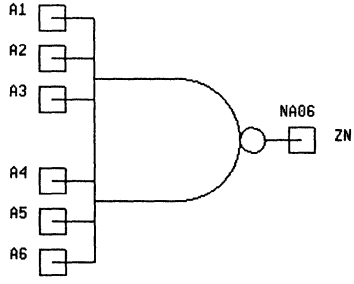
6-INPUT NAND GATE

DESCRIPTION

The NA06 combines inputs A1 through A6 to provide the NAND function at output ZN.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	A4	A5	A6	ZN
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
A3	Input	1.0	Data Input
A4	Input	1.0	Data Input
A5	Input	1.0	Data Input
A6	Input	1.0	Data Input
ZN	Output	-	Data Output

NA06

6-INPUT NAND GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A6->ZN	1.1 + 1.5 + 0.29 * UL	0.5 + 2.9 + 0.54 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

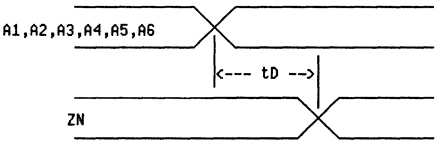
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.9	3.9	3.2	4.5	4.1	6.1	5.5	8.8

Note: For other operating conditions, use derating curves given in the performance section.

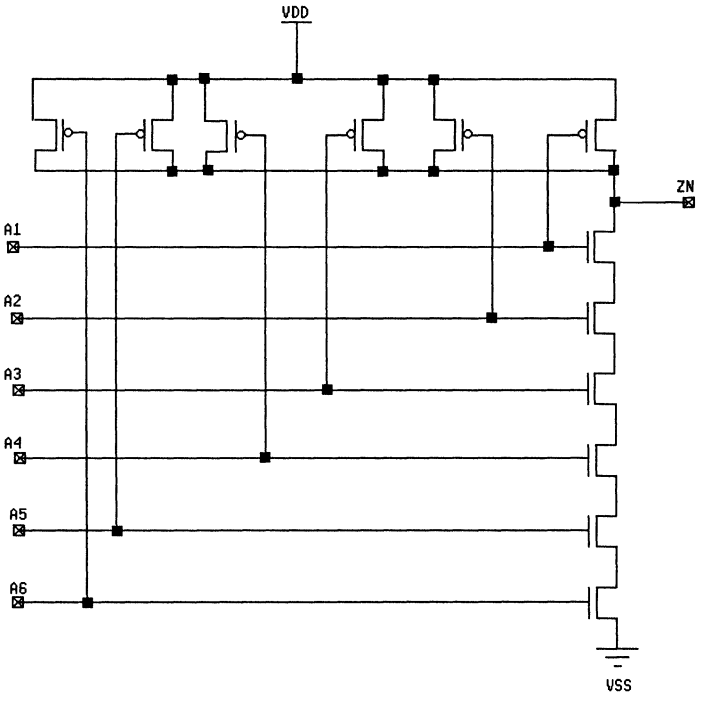
NA06

6-INPUT NAND GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



NOR02

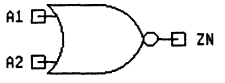
2-INPUT NOR GATE

DESCRIPTION

The NOR02 combines inputs A1 and A2 to provide the NOR function at output ZN.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
A1	A2	ZN
H	X	L
X	H	L
L	L	H

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
ZN	Output	-	Data Output

NOR02

2-INPUT NOR GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A1->ZN	0.5 + 1.2 + 0.45 * UL	0.1 + 0.4 + 0.14 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

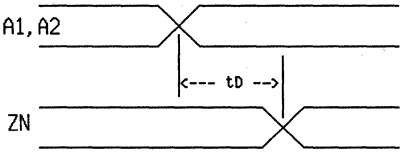
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.2	0.6	2.6	0.8	4.0	1.1	6.2	1.9

Note: For other operating conditions, use derating curves given in the performance section.

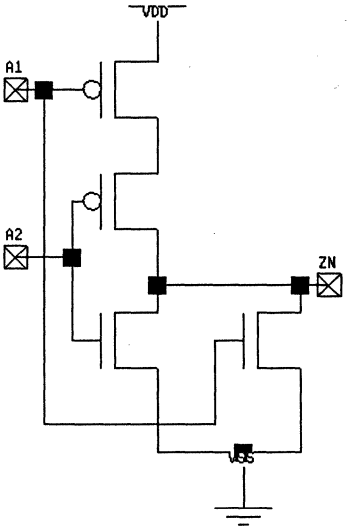
NOR02

2-INPUT NOR GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



NOR02I

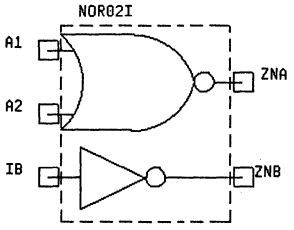
2-INPUT NOR GATE PLUS INVERTER

DESCRIPTION

The NOR02I combines a 2-Input NOR gate with an inverter in one macro. If either of the gates are unused, their input(s) must be tied to VDD or VSS.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	INPUTS	OUTPUTS
A1	A2	ZNA	IB	ZNB
H	X	L	L	H
X	H	L	H	L
L	L	H	-	-

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	NOR Gate Input
A2	Input	1.0	NOR Gate Input
ZNA	Output	-	NOR Gate Output
IB	Input	1.0	INVERTER Input
ZNB	Output	-	INVERTER Output

NOR02I

2-INPUT NOR GATE PLUS INVERTER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDA, A2->ZNA	0.5 + 0.9 + 0.45 * UL	0.3 + 0.2 + 0.12 * UL
tDB, IB->ZNB	0.5 + 0.5 + 0.19 * UL	0.1 + 0.2 + 0.07 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

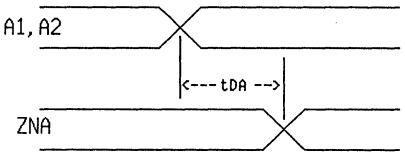
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDA	1.9	0.6	2.3	0.7	3.7	1.1	5.9	1.7
tDB	1.2	0.4	1.4	0.4	2.0	0.7	2.9	1.0

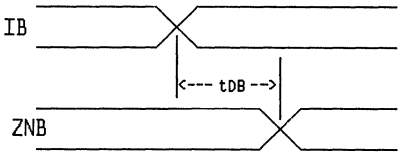
Note: For other operating conditions, use derating curves given in the performance section.

NOR02I

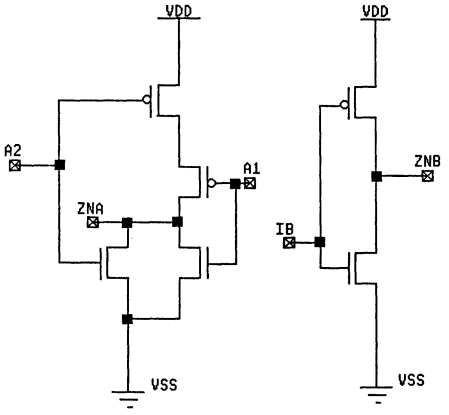
2-INPUT NOR GATE PLUS INVERTER

AC CHARACTERISTICS (cont'd)





CIRCUIT DIAGRAM



NOR03

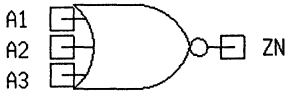
3-INPUT NOR GATE

DESCRIPTION

The NOR03 combines inputs A1,A2 and A3 to provide the NOR function at output ZN.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS			OUTPUT
A1	A2	A3	ZN
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
A3	Input	1.0	Data Input
ZN	Output	-	Data Output

NOR03

3-INPUT NOR GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A1->ZN	0.2 + 2.2 + 0.72 * UL	0.2 + 0.4 + 0.12 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

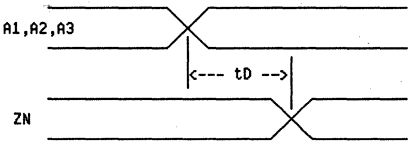
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	3.1	0.7	3.8	0.8	6.0	1.2	9.6	1.8

Note: For other operating conditions, use derating curves given in the performance section.

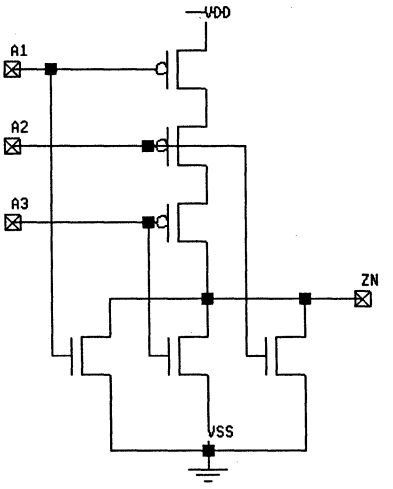
NOR03

3-INPUT NOR GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



NOR04

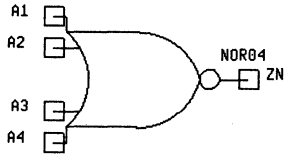
4-INPUT NOR GATE

DESCRIPTION

The NOR04 combines inputs A1 through A4 to provide the NOR function at the output ZN.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUT
A1	A2	A3	A4	ZN
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
A3	Input	1.0	Data Input
A4	Input	1.0	Data Input
ZN	Output	-	Data Output

NOR04

4-INPUT NOR GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A1->ZN	0.5 + 3.7 + 0.95 * UL	0.3 + 0.5 + 0.12 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

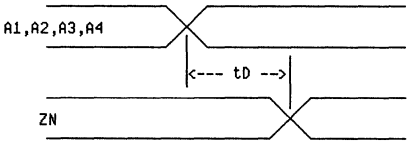
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	5.2	0.9	6.1	1.0	9.0	1.4	13.7	2.0

Note: For other operating conditions, use derating curves given in the performance section.

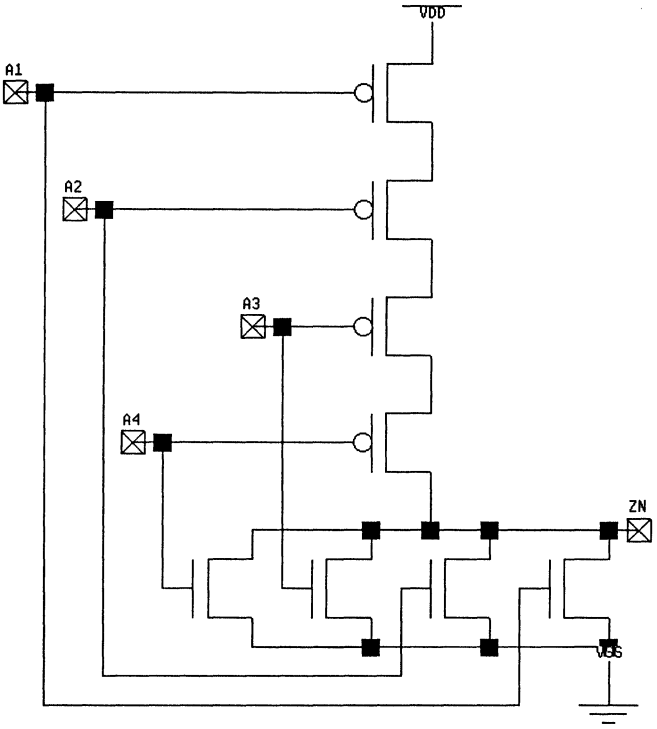
NOR04

4-INPUT NOR GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



AND02

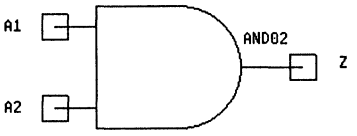
2-INPUT AND

DESCRIPTION

AND02 combines the inputs A1 and A2 to provide the AND function at output Z.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
A1	A2	Z
L	L	L
L	H	L
H	L	L
H	H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
Z	Output	-	Data Output

AND02

2-INPUT AND

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A1->Z	1.2 + 0.7 + 0.29 * UL	1.9 + 0.3 + 0.14 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

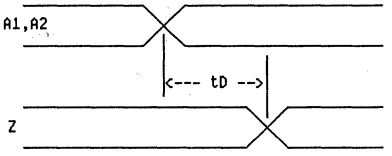
	UL = 1.0		UL = 2.0		UL = 5.0		UL = 10.0	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.2	2.3	2.5	2.5	3.4	2.8	4.8	3.6

Note: For other operating conditions, use derating curves given in the performance section.

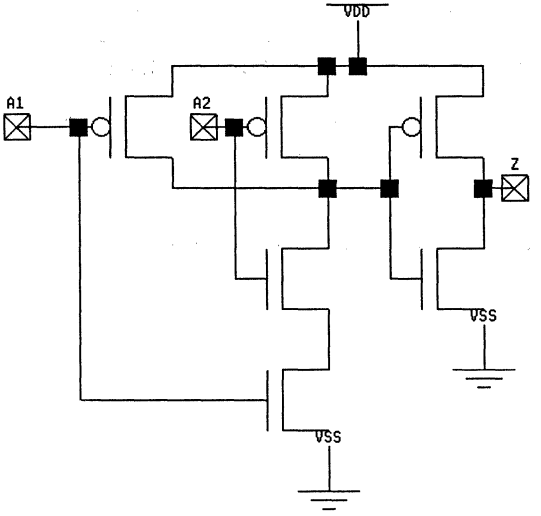
AND02

2-INPUT AND

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



OR02

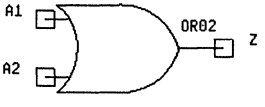
2-INPUT OR GATE

DESCRIPTION

The OR02 combines inputs A1 and A2 to provide the OR function at the output Z.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
A1	A2	Z
L	L	L
H	L	H
L	H	H
H	H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
Z	Output	-	Data Output

OR02

2-INPUT OR GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A1->Z	0.9 + 0.6 + 0.26 * UL	2.1 + 0.4 + 0.15 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

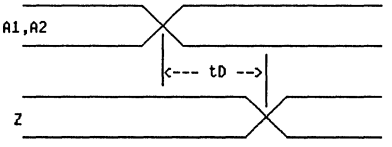
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	1.8	2.7	2.0	2.8	2.8	3.3	3.6	4.0

Note: For other operating conditions, use derating curves given in the performance section.

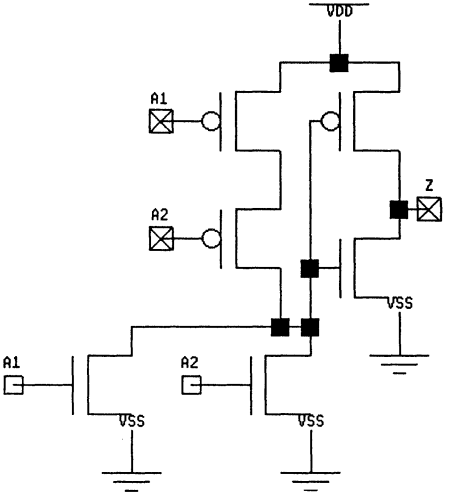
OR02

2-INPUT OR GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



X2NA04

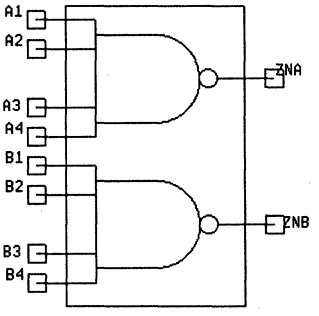
DUAL 4-INPUT NAND GATE

DESCRIPTION

The X2NA04 combines two 4-Input NAND gates in one macro.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	INPUTS				OUTPUTS
A1	A2	A3	A4	ZNA	B1	B2	B3	B4	ZNB
L	X	X	X	H	L	X	X	X	H
X	L	X	X	H	X	L	X	X	H
X	X	L	X	H	X	X	L	X	H
X	X	X	L	H	X	X	X	L	H
H	H	H	H	L	H	H	H	H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	NAND Gate Input A
A2	Input	1.0	NAND Gate Input A
A3	Input	1.0	NAND Gate Input A
A4	Input	1.0	NAND Gate Input A
ZNA	Output	-	NAND Gate Output A
B1	Input	1.0	NAND Gate Input B
B2	Input	1.0	NAND Gate Input B
B3	Input	1.0	NAND Gate Input B
B4	Input	1.0	NAND Gate Input B
ZNB	Output	-	NAND Gate Output B

X2NA04

DUAL 4-INPUT NAND GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDA, A4->ZNA	1.0 + 1.3 + 0.29 * UL	0.3 + 1.7 + 0.37 * UL
tDB, B4->ZNB	1.1 + 1.2 + 0.29 * UL	0.5 + 1.5 + 0.37 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

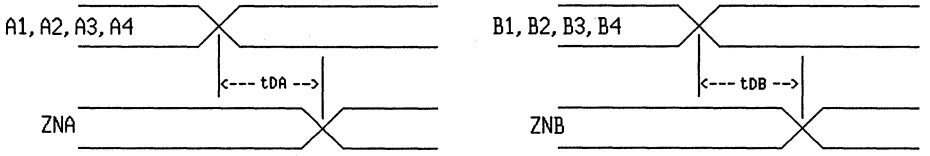
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDA	2.6	2.4	2.9	2.7	3.8	3.9	5.2	5.7
tDB	2.6	2.4	2.9	2.7	3.8	3.9	5.2	5.7

Note: For other operating conditions, use derating curves given in the performance section.

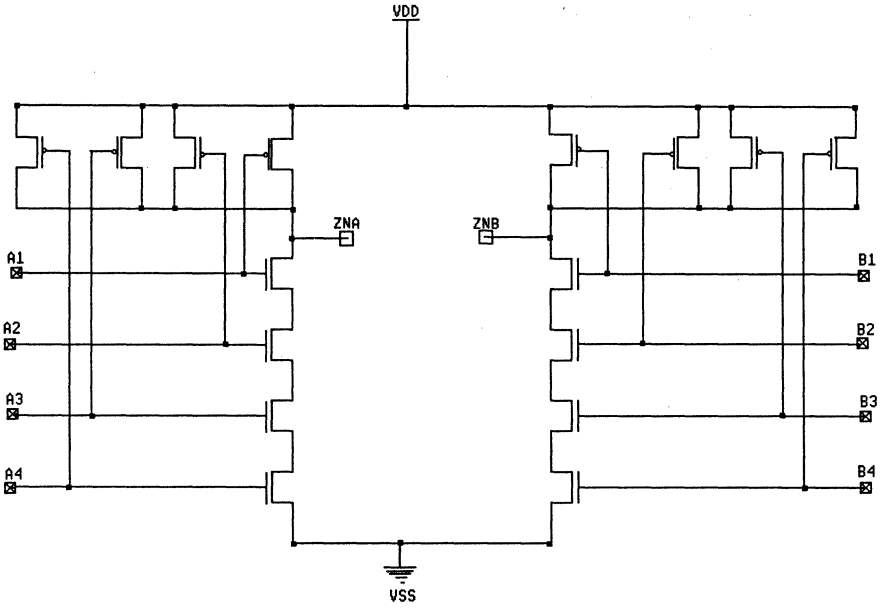
X2NA04

DUAL 4-INPUT NAND GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



INV11

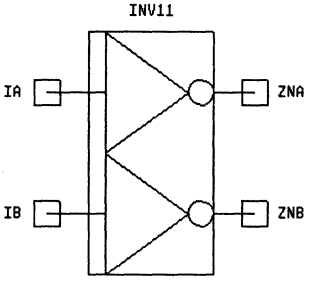
DUAL 1X INVERTERS

DESCRIPTION

The INV11 provides two independent inverters. Outputs ZNA and ZNB provide the logical inverse of their respective inputs, IA and IB. If only one inverter is used, the other input must be connected to VDD or VSS.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT	INPUT	OUTPUT
IA	ZNA	IB	ZNB
L	H	L	H
H	L	H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
IA	Input	1.0	Data Input
IB	Input	1.0	Data Input
ZNA	Output	-	Data Output
ZNB	Output	-	Data Output

INV11

DUAL 1X INVERTERS

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, IA,IB->ZNA,ZNB	0.5 + 0.4 + 0.19 * UL	0.1 + 0.2 + 0.07 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

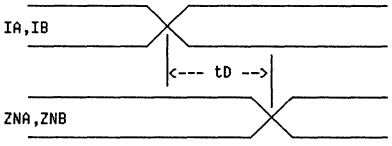
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	1.1	0.40	1.3	0.44	1.9	0.70	2.8	1.0

Note: For other operating conditions, use derating curves given in the performance section.

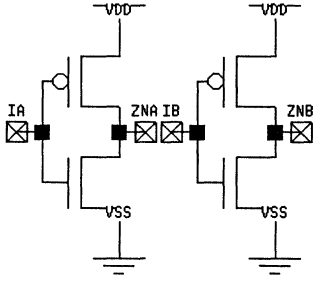
INV11

DUAL 1X INVERTERS

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



INV12

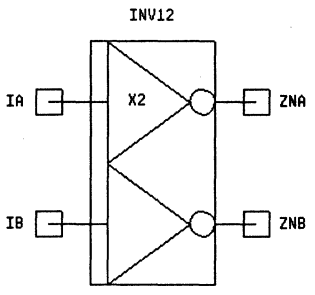
INVERTERS (1X AND 2X)

DESCRIPTION

The INV12 consists of two independent inverters; a single inverter and a paralleled inverter. The single inverter provides the logical inverse of the input IB at the output ZNB. The paralleled inverter, which consists of two inverters sharing a common input, IA, and a common output, ZNA, provides the same logic function as the single inverter, but with increased output drive capability. If only one inverter is used, the other input must be connected to VDD or VSS.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT	INPUT	OUTPUT
IA	ZNA	IB	ZNB
L	H	L	H
L	L	H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
IA	Input	2.0	Data Input
IB	Input	1.0	Data Input
ZNA	Output	-	Data Output
ZNB	Output	-	Data Output

INV12

INVERTERS (1X AND 2X)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDA, IA->ZNA	0.6 + 0.3 + 0.15 * UL	0.3 + 0.1 + 0.06 * UL
tDB, IB->ZNB	0.5 + 0.5 + 0.19 * UL	0.1 + 0.2 + 0.07 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

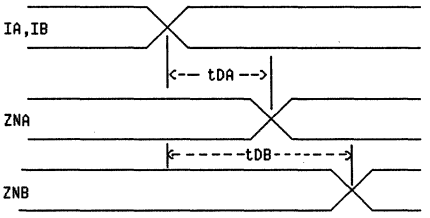
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDA	1.1	0.5	1.2	0.5	1.7	0.7	2.4	1.0
tDB	1.2	0.4	1.4	0.4	2.0	0.7	2.9	1.0

Note: For other operating conditions, use derating curves given in the performance section.

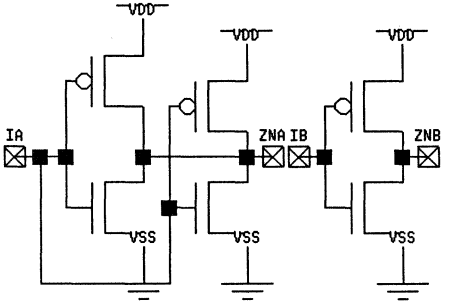
INV12

INVERTERS (1X AND 2X)

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



INV03

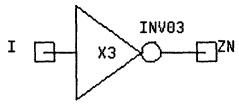
INVERTER (3X)

DESCRIPTION

The INV03 consists of three paralleled inverters with one common input and output. The output, ZN, provides the logical inverse of the input I.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS	OUTPUTS
I	ZN
L	H
H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	3.0	Data Input
ZN	Output	-	Data Output

INV03

INVERTER (3X)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, I->ZN	0.5 + 0.4 + 0.1 * UL	0.2 + 0.2 + 0.04 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

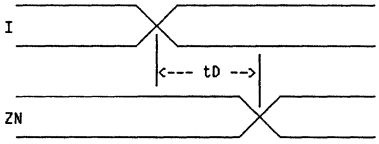
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	1.0	0.4	1.1	0.5	1.4	0.6	1.9	0.8

Note: For other operating conditions, use derating curves given in the performance section.

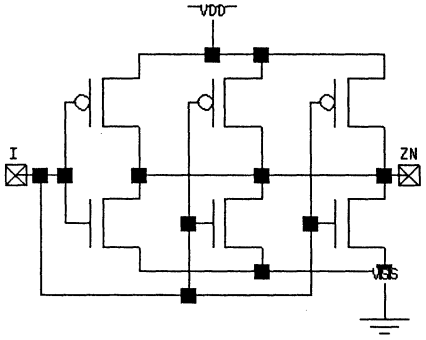
INV03

INVERTER (3X)

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



BUF02

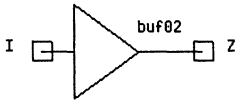
NON-INVERTING INTERNAL BUFFER, 2X

DESCRIPTION

The BUF02 consists of a single inverter driving a pair of paralleled inverters to form a non-inverting buffer.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
I	Z
L	L
H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	1.0	Data Input
Z	Output	-	Data Output

BUF02

NON-INVERTING INTERNAL BUFFER, 2X

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, I->Z	1.1 + 0.2 + 0.1 * UL	1.4 + 0.1 + 0.07 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

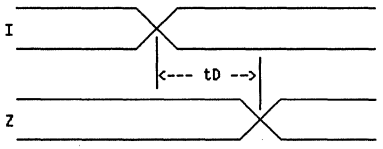
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	1.4	1.6	1.5	1.6	1.8	1.9	2.3	2.2

Note: For other operating conditions, use derating curves given in the performance section.

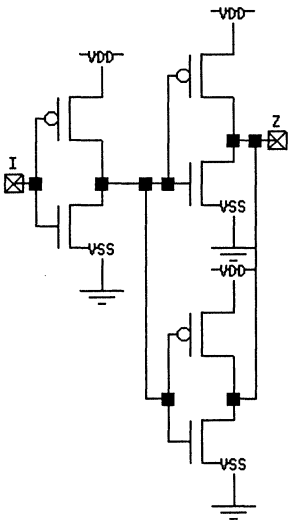
BUF02

NON-INVERTING INTERNAL BUFFER, 2X

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



INV01T

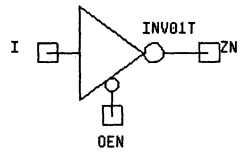
3-STATE INVERTER (INTERNAL, 1X)

DESCRIPTION

The INV01T is an internal 1X inverting buffer with 3-state output capability. When the OEN is HIGH, the output is in the high impedance state.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
I	OEN	ZN
L	L	H
H	L	L
X	H	Z

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	1.0	Data Input
OEN	Input	1.5	3-State ENABLE (Active-LOW)
ZN	Output	-	Data Output

INV01T

3-STATE INVERTER (INTERNAL, 1X)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, I->ZN	1.3 + 1.1 + 0.49 * UL	0.6 + 0.5 + 0.2 * UL
tOE, OEN->ZN	0.3 + 0.8 + 0.35 * UL	1.1 + 0.1 + 0.05 * UL
tOD, OEN->ZN	0.9 ns	1.0 ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

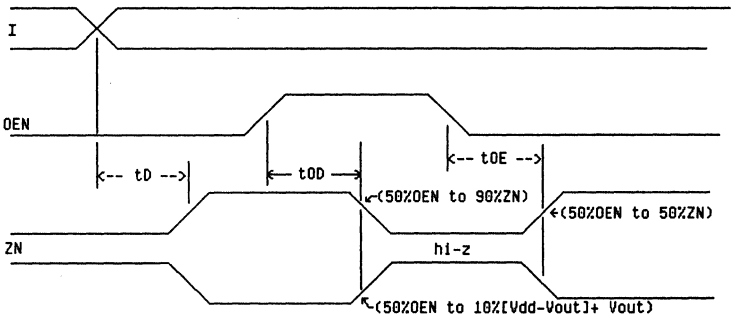
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.9	1.3	3.4	1.5	4.9	2.1	7.3	3.1
tOE	1.5	1.3	1.8	1.3	1.6	1.5	4.6	1.7
tOD	0.9	1.0	0.9	1.0	0.9	1.0	0.9	1.0

Note: For other operating conditions, use derating curves given in the performance section.

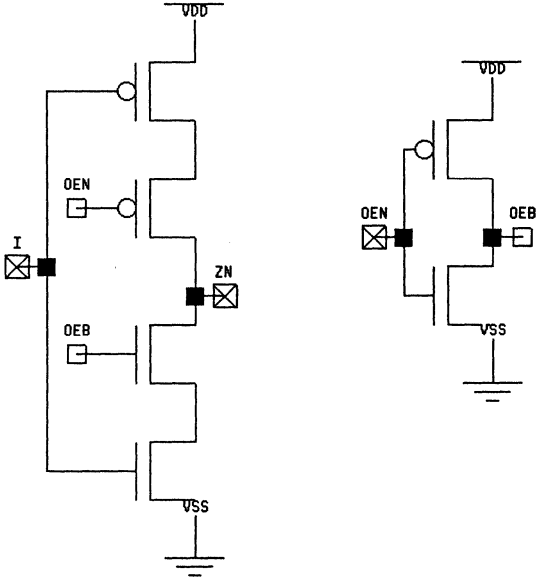
INV01T

3-STATE INVERTER (INTERNAL, 1X)

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



INV02T

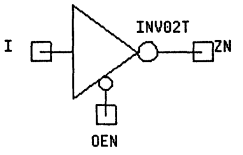
3-STATE INVERTER (INTERNAL, 2X)

DESCRIPTION

The INV02T is a 2X inverter with a 3-state output structure. When the output ENABLE signal is LOW, data passes through the inverter. When the output ENABLE is HIGH, the output presents a high impedance. This macro is designed for on-chip bus applications.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
I	OEN	ZN
L	L	H
H	L	L
X	H	Z

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	2.0	Data Input
OEN	Input	3.0	3-State ENABLE (Active-LOW)
ZN	Output	-	Data Output

INV02T

3-STATE INVERTER (INTERNAL, 2X)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, I->ZN	1.3 + 1.1 + 0.25 * UL	0.5 + 0.5 + 0.10 * UL
tOD, OEN->ZN	1.3 ns	0.3 ns
tOE, OEN->ZN	0.6 + 1.4 + 0.30 * UL	1.0 + 0.1 + 0.03 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

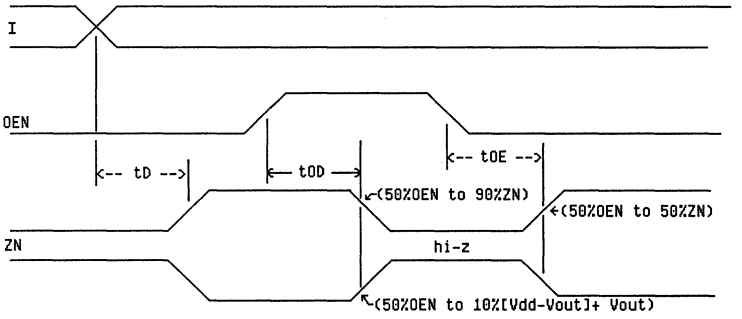
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.7	1.1	2.9	1.2	3.7	1.5	4.9	2.0
tOD	1.3	0.3	1.3	0.3	1.3	0.3	1.3	0.3
tOE	2.3	1.1	2.6	1.2	3.5	1.3	5.0	1.4

Note: For other operating conditions, use derating curves given in the performance section.

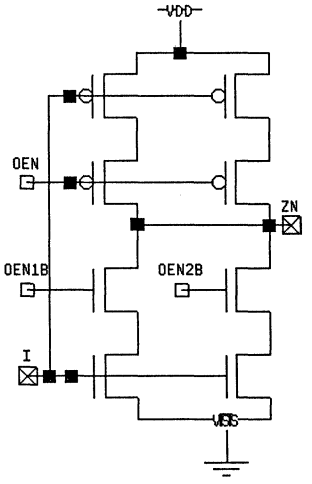
INV02T

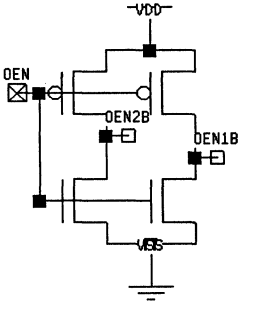
3-STATE INVERTER (INTERNAL, 2X)

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM





INV03T

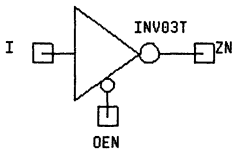
3-STATE INVERTER (INTERNAL, 3X)

DESCRIPTION

The INV03T is an internal 3X, 3-state buffer, which allows internal bus operations to be accomplished. When OEN is HIGH, the output, ZN, is in the high impedance state. When OEN is LOW, data at the input, I, is inverted at output ZN.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
I	OEN	ZN
L	L	H
H	L	L
X	H	Z

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	3.0	Data Input
OEN	Input	4.5	3-State ENABLE (Active-LOW)
ZN	Output	-	Data Output

INV03T

3-STATE INVERTER (INTERNAL, 3X)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, I->ZN	1.2 + 1.2 + 0.17 * UL	0.5 + 0.5 + 0.07 * UL
tOD, OEN->ZN	1.7 ns	0.6 ns
tOE, OEN->ZN	0.6 + 1.3 + 0.19 * UL	0.9 + 0.1 + 0.02 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

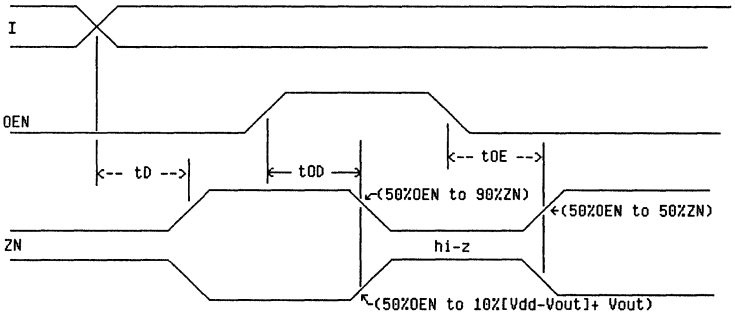
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.6	1.1	2.7	1.1	3.3	1.4	4.1	1.7
tOD	1.7	0.6	1.7	0.6	1.7	0.6	1.7	0.6
tOE	2.1	1.0	2.3	1.0	2.9	1.1	3.8	1.2

Note: For other operating conditions, use derating curves given in the performance section.

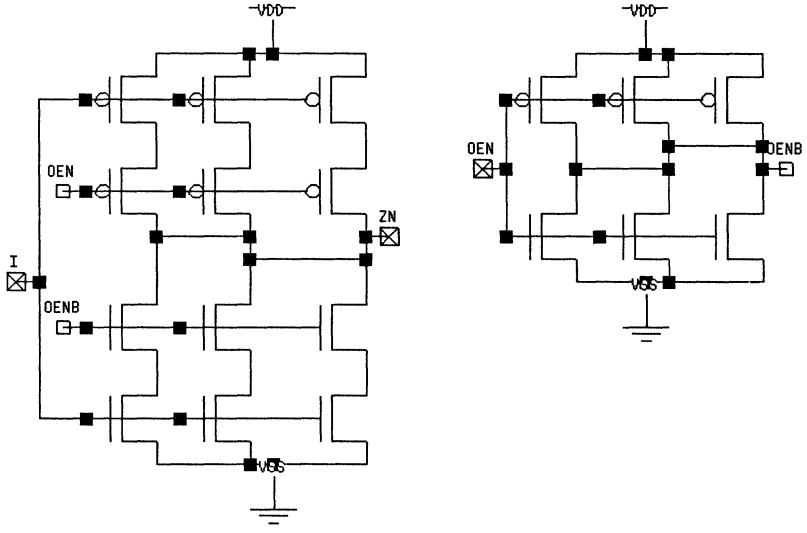
INV03T

3-STATE INVERTER (INTERNAL, 3X)

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



XOR02

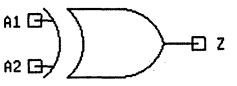
2-INPUT EXCLUSIVE-OR

DESCRIPTION

The XOR02 combines inputs A1 and A2 to provide the Exclusive-OR function at the output, Z.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS	OUTPUTS
A1 A2	Z
L L	L
L H	H
H L	H
H H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	2.0	Data Input
Z	Output	-	Data Output

XOR02

2-INPUT EXCLUSIVE-OR

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A2->Z	3.0 + 0.7 + 0.30 * UL	3.2 + 0.4 + 0.15 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

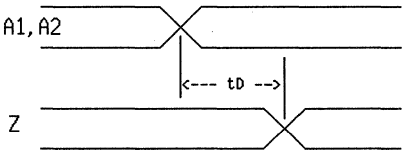
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	4.0	3.8	4.3	3.9	5.2	4.4	6.7	5.1

Note: For other operating conditions, use derating curves given in the performance section.

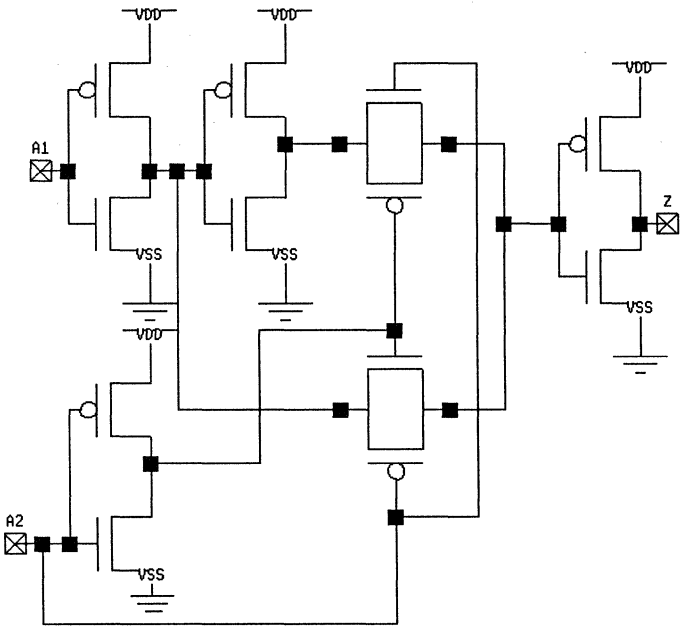
XOR02

2-INPUT EXCLUSIVE-OR

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



XNOR02

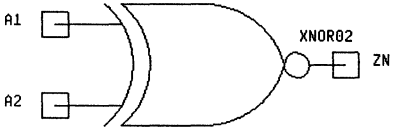
2-INPUT EXCLUSIVE NOR GATE

DESCRIPTION

The XNOR02 combines inputs A1 and A2 to provide the Exclusive-NOR function at the output ZN.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
A1	A2	ZN
L	L	H
H	L	L
L	H	L
H	H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	5.0	Data Input
A2	Input	2.0	Data Input
ZN	Output	-	Data Output

XNOR02

2-INPUT EXCLUSIVE NOR GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A2->ZN	1.5 + 0.7 + 0.30 * UL	3.2 + 0.4 + 0.15 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

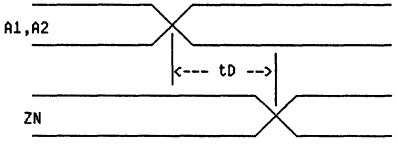
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.5	3.8	2.8	3.9	3.7	4.4	5.2	5.1

Note: For other operating conditions, use derating curves given in the performance section.

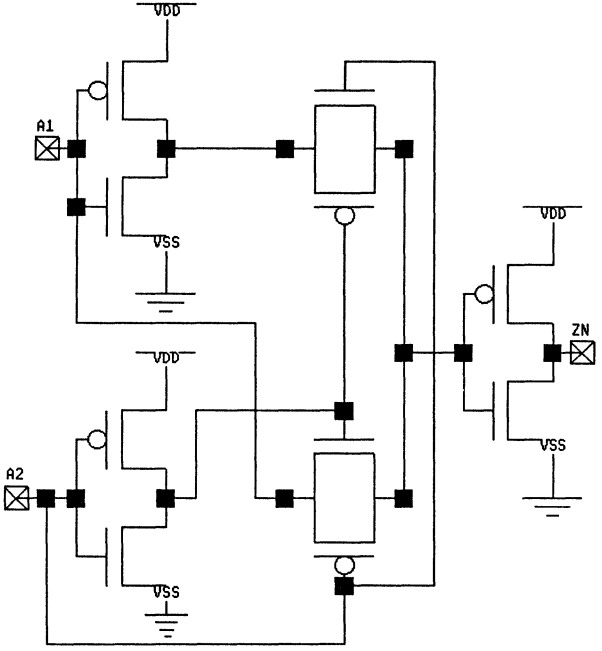
XNOR02

2-INPUT EXCLUSIVE NOR GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



XNOR021

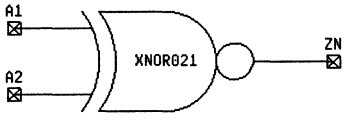
2-INPUT EXCLUSIVE NOR GATE

DESCRIPTION

The XNOR021 combines inputs A1 and A2 to provide the Exclusive-NOR function at the output ZN. This macro is a variation of XNOR02 to reduce the fan-in on pin A1.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
A1	A2	ZN
L	L	H
H	L	L
L	H	L
H	H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	2.0	Data Input
A2	Input	2.0	Data Input
ZN	Output	-	Data Output

XNOR021

2-INPUT EXCLUSIVE NOR GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A1->ZN	2.2 + 0.8 + 0.26 * UL	2.0 + 0.6 + 0.20 * UL
tDQ, A2->ZN	2.2 + 0.8 + 0.26 * UL	2.4 + 0.6 + 0.20 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

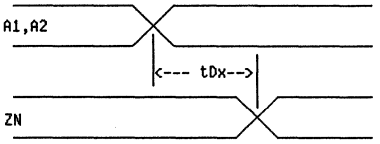
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	3.3	2.8	3.5	3.0	4.3	3.6	5.6	4.6
tDQ	3.3	3.2	3.5	3.4	4.3	4.0	5.6	5.0

Note: For other operating conditions, use derating curves given in the performance section.

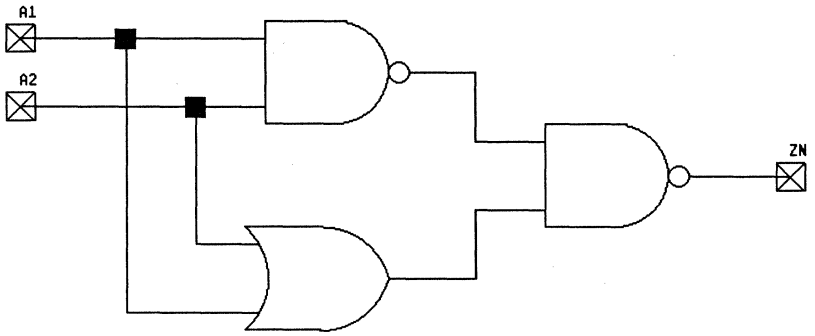
XNOR021

2-INPUT EXCLUSIVE NOR GATE

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



AOI21

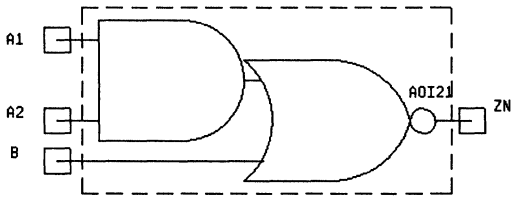
2-1 AND-OR-INVERT

DESCRIPTION

The AOI21 provides the combinational function (A1)(A2) + B at the output ZN.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS			OUTPUT
A1	A2	B	ZN
X	X	H	L
X	L	L	H
L	X	L	H
H	H	L	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
B	Input	1.0	Data Input
ZN	Output	-	Data Output

AOI21

2-1 AND-OR-INVERT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tAZN, A1->ZN	0.9 + 1.5 + 0.49 * UL	0.4 + 0.6 + 0.2 * UL
tBZN, B->ZN	1.5 + 1.5 + 0.49 * UL	0.6 + 0.4 + 0.11 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

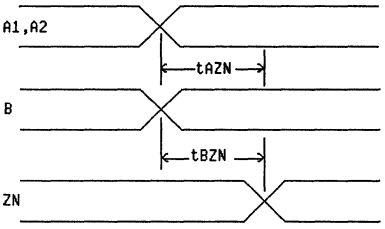
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tAZN	2.9	1.2	3.4	1.4	4.9	2.0	7.3	3.0
tBZN	3.5	1.1	4.0	1.2	5.6	1.6	7.9	2.1

Note: For other operating conditions, use derating curves given in the performance section.

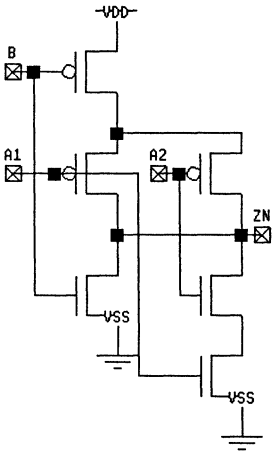
AOI21

2-1 AND-OR-INVERT

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



OAI21

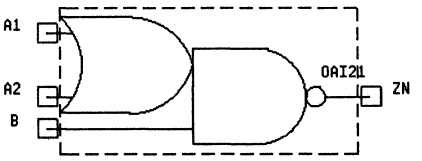
2-1 OR-AND-INVERT

DESCRIPTION

The OAI21 provides the combinational (A1 + A2)(B) function at the output ZN.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS			OUTPUT
A1	A2	B	ZN
H	X	H	L
X	H	H	L
X	X	L	H
L	L	X	H

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
B	Input	1.0	Data Input
ZN	Output	-	Data Output

OAI21

2-1 OR-AND-INVERT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDA, A1>ZN	1.6 + 0.7 + 0.36 * UL	0.7 + 0.3 + 0.16 * UL
tDB, B->ZN	0.5 + 0.4 + 0.19 * UL	0.6 + 0.3 + 0.16 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

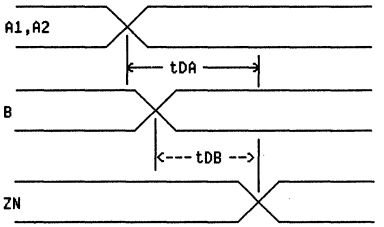
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDA	2.7	1.2	3.0	1.3	4.1	1.8	5.9	2.6
tDB	1.1	1.1	1.3	1.2	1.9	1.7	2.8	2.5

Note: For other operating conditions, use derating curves given in the performance section.

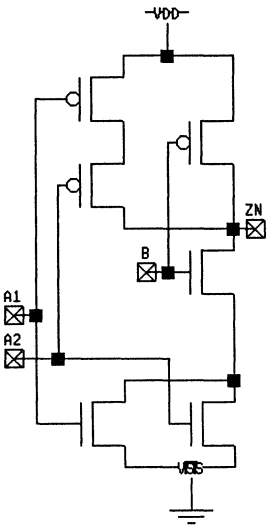
OAI21

2-1 OR-AND-INVERT

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



AO22

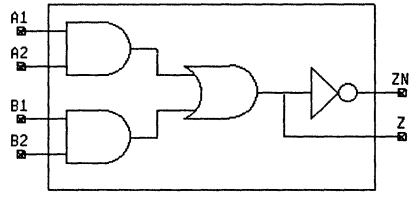
2-2 AND-OR-INVERT WITH COMPLIMENTARY OUTPUTS

DESCRIPTION

The AO22 provides the 2-2 AND-OR-Invert function with complimentary outputs. Two internal parallel inverters drive output Z for greater (2X) output drive capability.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUT	
A1	A2	B1	B2	Z	ZN
X	L	X	L	L	H
L	X	X	L	L	H
X	L	L	X	L	H
L	X	L	X	L	H
H	H	X	X	H	L
X	X	H	H	H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	A Data Input
A2	Input	1.0	A Data Input
B1	Input	1.0	B Data Input
B2	Input	1.0	B Data Input
Z	Output	-	Data Output (2X Drive)
ZN	Output	-	Complimentary Data Output

AO22

2-2 AND-OR-INVERT WITH COMPLIMENTARY OUTPUTS

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDZ, A1/B1-Z	2.9 + 0.3 + 0.15 * UL	5.9 + 0.2 + 0.11 * UL
tDZN, A1/B1-ZN	3.4 + 2.1 + 0.49 * UL	0.9 + 0.9 + 0.21 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

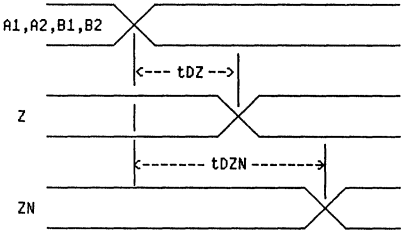
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDZ	3.4	6.2	3.5	6.3	4.0	6.7	4.7	7.2
tDZN	6.0	2.0	6.5	2.2	8.0	2.9	10.4	3.9

Note: For other operating conditions, use derating curves given in the performance section.

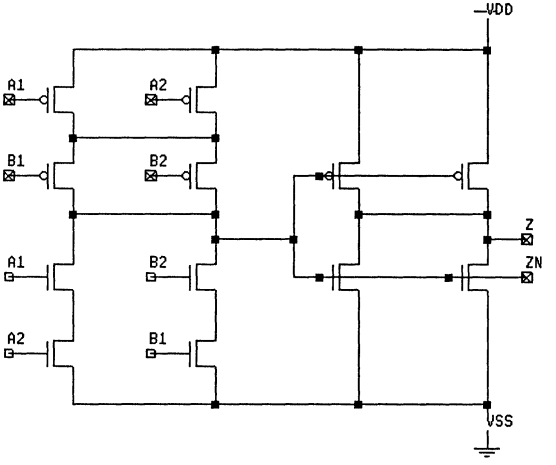
AO22

2-2 AND-OR-INVERT WITH COMPLIMENTARY OUTPUTS

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



AOI222

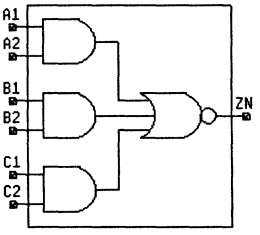
2-2-2 AND-OR-INVERT

DESCRIPTION

The AOI222 provides a 2-2-2 AND-OR-Invert function.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	B1	B2	C1	C2	ZN
X	L	X	L	X	L	H
X	L	X	L	L	X	H
X	L	L	X	X	L	H
X	L	L	X	L	X	H
L	X	X	L	X	L	H
L	X	X	L	L	X	H
L	X	L	X	X	L	H
L	X	L	X	L	X	H
X	X	X	X	H	H	L
X	X	H	H	X	X	L
H	H	X	X	X	X	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	A Data Input
A2	Input	1.0	A Data Input
B1	Input	1.0	B Data Input
B2	Input	1.0	B Data Input
C1	Input	1.0	C Data Input
C2	Input	1.0	C Data Input
ZN	Output	-	Data Output

AOI222

2-2-2 AND-OR-INVERT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDZ, A2-ZN	5.7 + 3.2 + 0.72 * UL	0.8 + 1.0 + 0.22 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

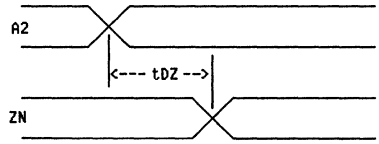
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDZ	9.6	2.0	10.3	2.2	12.5	2.9	16.1	4.0

Note: For other operating conditions, use derating curves given in the performance section.

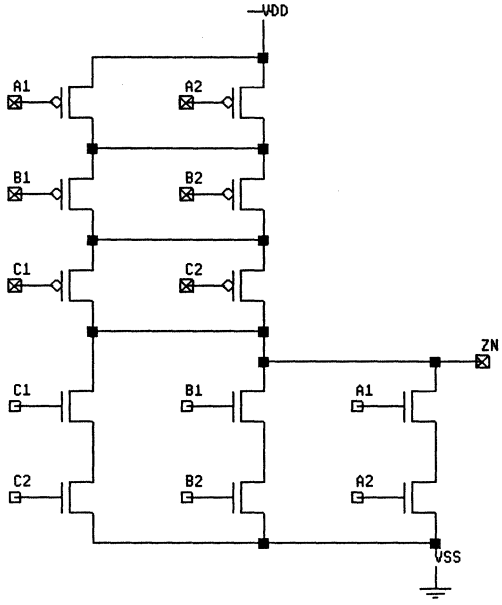
AOI222

2-2-2 AND-OR-INVERT

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



AOI22I

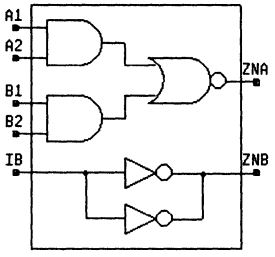
2-2 AND-OR-INVERT PLUS 2X INVERTER

DESCRIPTION

The AOI22I provides a 2-2 AND-OR-Invert and a 2x inverter as separate functions. The inverter can be used at the output of the AOI to provide a HIGH drive, positive logic output. If the inverter is not used, the input must be tied to VDD or VSS.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS					OUTPUTS	
A1	A2	B1	B2	IB	ZNA	ZNB
X	L	X	L	H	H	L
L	X	L	X	L	H	H
L	X	X	L	-	H	-
X	L	L	X	-	H	-
H	H	X	X	-	L	-
X	X	H	H	-	L	-

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	A Data Input
A2	Input	1.0	A Data Input
B1	Input	1.0	B Data Input
B2	Input	1.0	B Data Input
IB	Input	2.0	Inverter Data Input
ZNA	Output	-	AOI Data Output
ZNB	Output	-	Inverter Data Output

AOI22I

2-2 AND-OR-INVERT PLUS 2X INVERTER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDA, A1,B1-ZNA	3.6 + 0.9 + 0.49 * UL	1.0 + 0.4 + 0.21 * UL
tDB, IB-ZNB	0.6 + 0.3 + 0.15 * UL	0.3 + 0.1 + 0.06 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

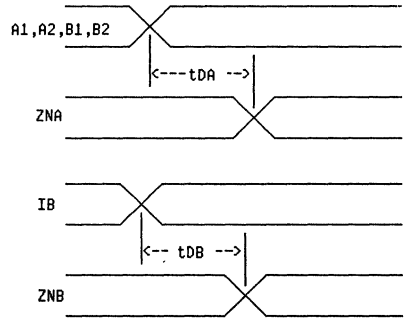
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDA	5.0	1.6	5.5	1.8	7.0	2.5	9.4	3.5
tDB	1.1	0.5	1.2	0.5	1.7	0.7	2.4	1.0

Note: For other operating conditions, use derating curves given in the performance section.

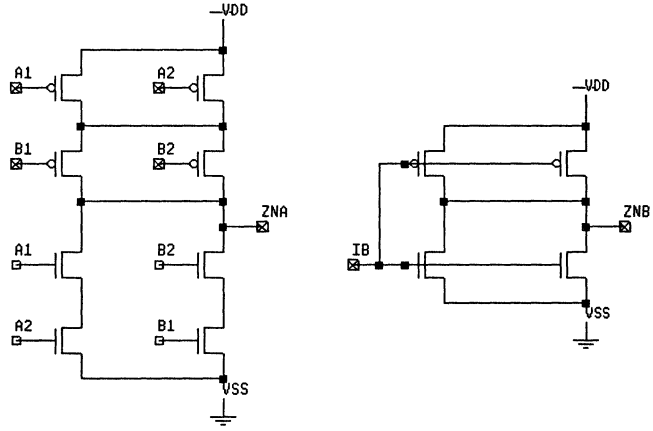
AOI22I

2-2 AND-OR-INVERT PLUS 2X INVERTER

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



AOI33

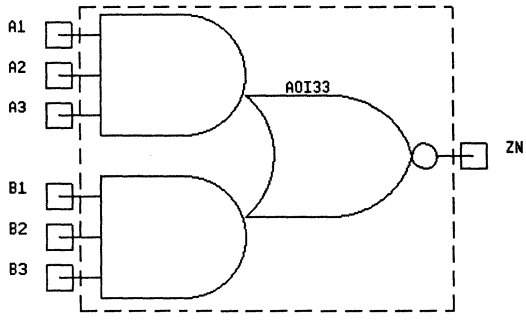
3-3 AND-OR-INVERT

DESCRIPTION

The AOI33 privides the combinational function (A1)(A2)(A3) + (B1)(B2)(B3) at the output ZN.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS						OUTPUT
A1	A2	A3	B1	B2	B3	ZN
X	X	L	X	X	L	H
X	X	L	X	L	X	H
X	X	L	L	X	X	H
X	L	X	X	X	L	H
X	L	X	X	L	X	H
X	L	X	L	X	X	H
L	X	X	X	X	L	H
L	X	X	X	L	X	H
L	X	X	L	X	X	H
H	H	H	X	X	X	L
X	X	X	H	H	H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
A3	Input	1.0	Data Input
B1	Input	1.0	Data Input
B2	Input	1.0	Data Input
B3	Input	1.0	Data Input
ZN	Output	-	Data Output

AOI33

3-3 AND-OR-INVERT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tAZN, A3->ZN	2.3 + 2.1 + 0.49 * UL	1.7 + 1.2 + 0.29 * UL
tBZN, B3->ZN	1.3 + 2.1 + 0.49 * UL	1.5 + 1.3 + 0.29 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

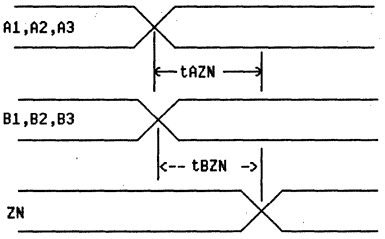
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tAZN	4.9	3.2	5.4	3.5	6.9	4.4	9.3	5.8
tBZN	3.9	3.1	4.4	3.4	5.9	4.3	8.3	5.7

Note: For other operating conditions, use derating curves given in the performance section.

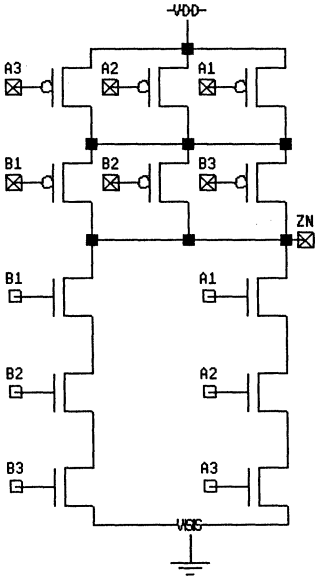
AOI33

3-3 AND-OR-INVERT

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



LA01

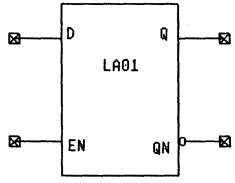
BUFFERED LATCH

DESCRIPTION

LA01 is an active-LOW Latch. The ENABLE and Data inputs, EN and D, and the outputs, Q and QN, are buffered. When EN is LOW, data at D is transferred to the Q and QN outputs.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
EN	D	Q	QN
L	L	L	H
L	H	H	L
H	X	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	1.0	Data Input
EN	Input	2.0	ENABLE Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

LA01

BUFFERED LATCH

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, D-Q	2.2 + 0.6 + 0.28 * UL	3.3 + 0.4 + 0.17 * UL
tQN, D-QN	4.4 + 0.6 + 0.26 * UL	3.7 + 0.3 + 0.13 * UL
tEQ, EN-Q	2.5 + 0.6 + 0.28 * UL	2.7 + 0.4 + 0.17 * UL
tEQN, EN-QN	3.7 + 0.6 + 0.26 * UL	3.9 + 0.3 + 0.12 * UL

tWEN, EN	3.6	ns
tS, D-EN	4.3	ns
tH, EN-D	0	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

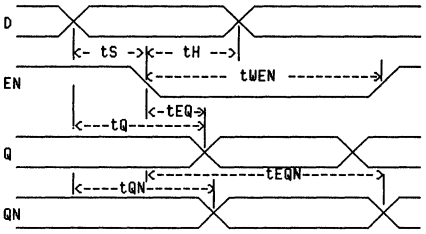
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	3.1	3.9	3.4	4.0	4.2	4.6	5.6	5.4
tQN	5.3	4.1	5.5	4.3	6.3	4.7	7.6	5.3
tEQ	3.4	3.3	3.7	3.4	4.5	4.0	5.9	4.8
tEQN	4.6	4.3	4.8	4.4	5.6	4.8	6.9	5.4

Note: For other operating conditions, use derating curves given in the performance section.

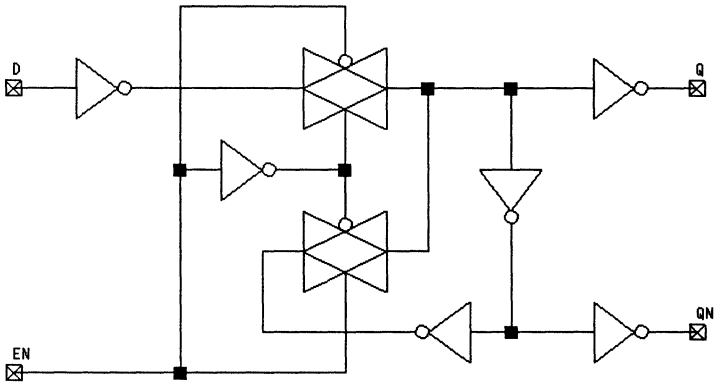
LA01

BUFFERED LATCH

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



LAE01

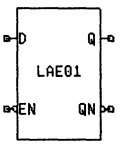
D-LATCH

DESCRIPTION

The LAE01 is a D-Latch. Information present at the input, D, is transferred to the Q output when the ENABLE signal, EN, is LOW. The Q output will follow the input, D, as long as ENABLE remains LOW. When the ENABLE goes HIGH, information at the data input at the time of transition is retained until ENABLE goes LOW. Output QN drives two internal loads.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
D	EN	Q	QN
L	L	L	H
H	L	H	L
X	H	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
EN	Input	2.0	ENABLE Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

LAE01

D-LATCH

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, EN-Q	2.1 + 0.8 + 0.50 * UL	2.4 + 0.9 + 0.56 * UL
tQN, EN-QN	1.4 + 1.5 + 0.30 * UL	1.6 + 0.6 + 0.12 * UL
tDQ, D-Q	1.3 + 0.8 + 0.50 * UL	1.4 + 0.9 + 0.56 * UL
tDQN, D-QN	0.5 + 1.4 + 0.30 * UL	0.8 + 0.6 + 0.12 * UL

tWEN, EN	2.4	ns
tS, D-EN	1.8	ns
tH, EN-D	0	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

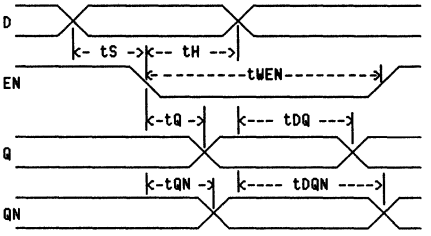
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	3.4	3.9	3.9	4.4	5.4	6.1	7.9	8.9
tQN	3.2	2.3	3.5	2.4	4.4	2.8	5.9	3.4
tDQ	2.6	2.9	3.1	3.4	4.6	5.1	7.1	7.9
tDQN	2.2	1.5	2.5	1.6	3.4	2.0	4.9	2.6

Note: For other operating conditions, use derating curves given in the performance section.

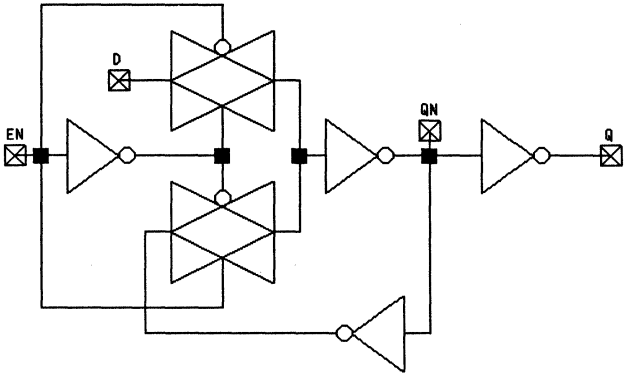
LAE01

D-LATCH

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



LAE01T

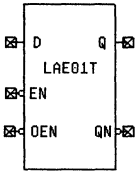
D-LATCH W/3-STATE OUTPUT

DESCRIPTION

LAE01T is a D-Latch with active-LOW 3-state output ENABLE. Information present at Input D is transferred to output Q and inverted at complimentary output QN, when ENABLE Input EN is set LOW, and is latched when EN is HIGH. Outputs Q and QN are enabled when OEN is set LOW, and are in high impedance state when OEN is HIGH.

Cells: 4 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	
EN	OEN	D	Q	QN
L	L	D	D	$\bar{D}$
H	L	X	D	$\bar{D}$
X	H	X	Z	Z

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	1.0	Data Input
EN	Input	1.0	ENABLE Input (Active-LOW)
OEN	Input	2.0	Output ENABLE (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

LAE01T

D-LATCH W/3-STATE OUTPUT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDQ, D-Q	2.7 + 1.1 + 0.50 * UL	3.4 + 0.6 + 0.26 * UL
tDQN, D-QN	5.4 + 1.1 + 0.49 * UL	3.9 + 0.5 + 0.23 * UL
tQ, EN-Q	3.0 + 1.1 + 0.50 * UL	2.4 + 0.6 + 0.26 * UL
tQN, EN-QN	4.3 + 1.1 + 0.49 * UL	4.1 + 0.5 + 0.23 * UL
tOE, OEN-Q	0.7 + 1.8 + 0.81 * UL	1.5 + 0.5 + 0.24 * UL
tOD, OEN-Q	0.8 ns	0.3 ns

tWEN, EN	2.8 ns
tS, D-EN	2.4 ns
tH, EN-D	0 ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

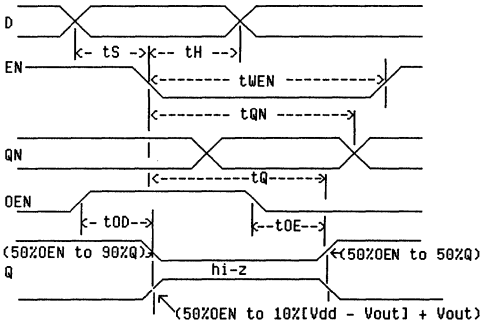
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDQ	4.3	4.3	4.8	4.5	6.3	5.3	8.8	6.6
tDQN	7.0	4.6	7.5	4.9	9.0	5.6	11.4	6.7
tQ	4.6	3.3	5.1	3.5	6.6	4.3	9.1	5.6
tQN	5.9	4.8	6.4	5.1	7.9	5.8	10.3	6.9
tOE	3.3	2.2	4.1	2.5	6.6	3.2	10.6	4.4
tOD	0.8	0.3	0.8	0.3	0.8	0.3	0.8	0.3

Note: For other operating conditions, use derating curves given in the performance section.

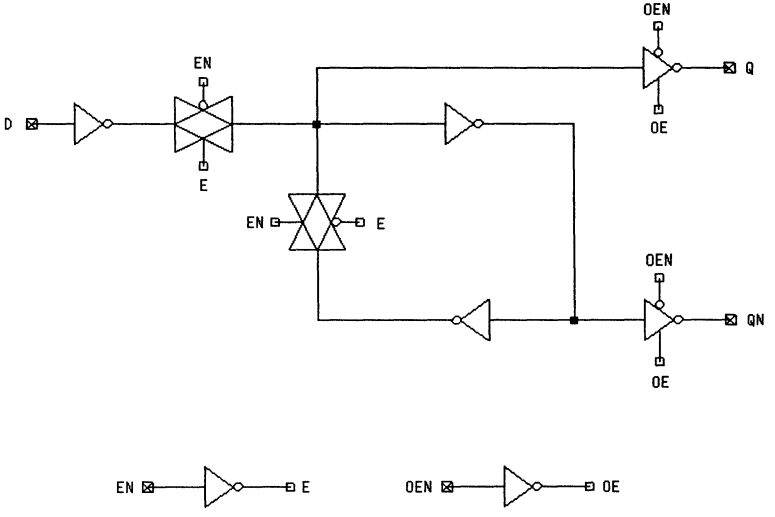
LAE01T

D-LATCH W/3-STATE OUTPUT

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



LAE01S

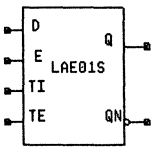
D-LATCH W/SCAN LOGIC

DESCRIPTION

LAE01S is an active-LOW D-Latch, with Scan Test logic. Information at the D input is transferred to the output when Test Enable, TE, and ENABLE, E signals are both LOW. Test Data input TI, and TE additionally serve to support Scan Data path test methodology. This macro has buffered clock inputs and outputs.

Cells: 5 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS					OUTPUTS	
E	EN	TE	TI	D	Q	QN
H	L	L	X	L	L	H
H	L	L	X	H	H	L
H	L	H	L	X	L	H
H	L	H	H	X	H	L
L	H	L	X	X	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	1.0	Data Input
E	Input	2.0	ENABLE Input (Active-LOW)
TI	Input	1.0	Test Data Input
TE	Input	2.0	Test ENABLE Input
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

LAE01S

D-LATCH W/SCAN LOGIC

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, D-Q	6.0 + 0.6 + 0.25 * UL	8.7 + 0.3 + 0.13 * UL
tQN, D-QN	7.3 + 0.5 + 0.28 * UL	4.8 + 0.3 + 0.17 * UL
tEQ, E-Q	5.7 + 0.6 + 0.26 * UL	8.8 + 0.3 + 0.13 * UL
tEQN, E-QN	7.8 + 0.4 + 0.27 * UL	4.6 + 0.3 + 0.20 * UL
tTQ, TE-Q	5.7 + 0.6 + 0.25 * UL	8.8 + 0.3 + 0.11 * UL
tTQN, TE-QN	7.8 + 0.5 + 0.29 * UL	4.8 + 0.3 + 0.15 * UL
tIQ, TI-Q	6.4 + 0.7 + 0.27 * UL	9.8 + 0.3 + 0.13 * UL
TIQN, TI-QN	8.0 + 0.5 + 0.31 * UL	5.3 + 0.3 + 0.20 * UL

tWEN, E	3.6 ns
tS, D-E	4.8 ns
tH, E-D	0 ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

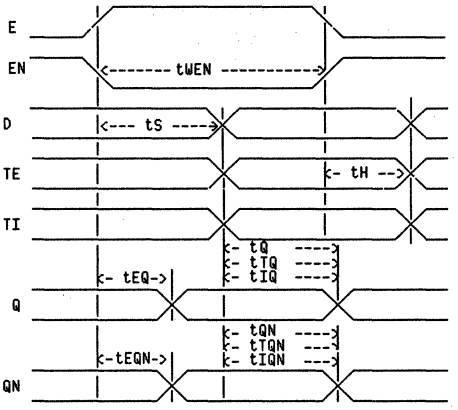
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	6.9	9.1	7.1	9.3	7.9	9.7	9.1	10.3
tQN	8.1	5.3	8.4	5.4	9.2	6.0	10.6	6.8
tEQ	6.6	9.2	6.8	9.5	7.6	9.8	8.9	10.4
tEQN	8.5	5.1	8.7	5.3	9.6	5.9	10.9	6.9
tTQ	6.6	9.2	6.8	9.3	7.6	9.6	8.8	10.2
tTQN	8.6	5.3	8.9	5.4	9.8	5.9	11.2	6.6
tIQ	7.4	10.2	7.6	10.4	8.5	10.8	9.8	11.4
tIQN	8.8	5.8	9.1	6.0	10.0	6.6	11.6	7.6

Note: For other operating conditions, use derating curves given in the performance section.

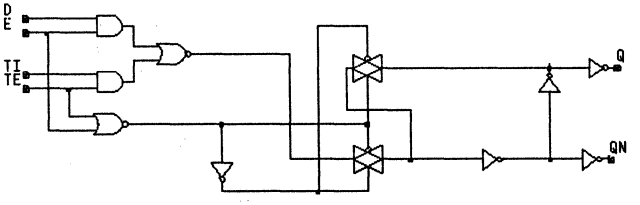
LAE01S

D-LATCH W/SCAN LOGIC

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



LA02

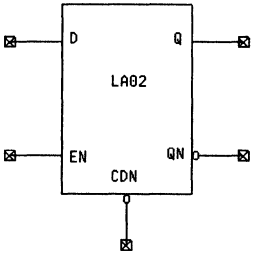
BUFFERED LATCH W/CLEAR

DESCRIPTION

LA01 is an active-LOW Latch. The ENABLE input, EN, and the outputs, Q and QN, are buffered. When EN is LOW, data at D is transferred to the Q and QN outputs.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	
CDN	EN	D	Q	QN
L	X	X	L	H
H	L	L	L	H
H	L	H	H	L
H	H	X	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
EN	Input	2.0	ENABLE Input (Active-LOW)
CDN	Input	1.0	CLEAR Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

LA02

BUFFERED LATCH W/CLEAR

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, D-Q	2.4 + 0.6 + 0.27 * UL	2.9 + 0.3 + 0.13 * UL
tQN, D-QN	3.7 + 0.6 + 0.26 * UL	3.9 + 0.3 + 0.13 * UL
tEQ, EN-Q	3.3 + 0.6 + 0.27 * UL	4.0 + 0.2 + 0.08 * UL
tEQN, EN-QN	4.8 + 0.6 + 0.26 * UL	4.8 + 0.3 + 0.13 * UL
tCQ, CDN-Q		1.9 + 0.3 + 0.13 * UL
tCQN, CDN-QN	3.4 + 0.7 + 0.27 * UL	

tWEN, EN	3.6 ns
tS, D-EN	4.3 ns
tH, EN-D	0 ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

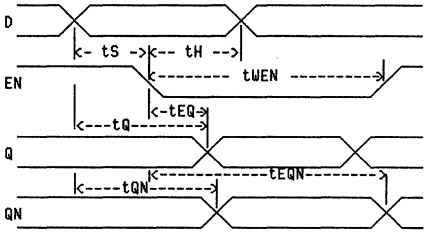
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	3.3	3.3	3.5	3.5	4.4	3.9	5.7	4.5
tQN	4.6	4.3	4.8	4.5	5.6	4.9	6.9	5.5
tEQ	4.2	4.3	4.4	4.4	5.3	4.6	6.6	5.0
tEQN	5.7	5.2	5.9	5.4	6.7	5.8	8.0	6.4
tCQ		2.3		2.5		2.9		3.5
tCQN	4.4		4.6		5.5		6.8	

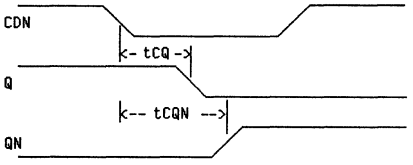
Note: For other operating conditions, use derating curves given in the performance section.

LA02

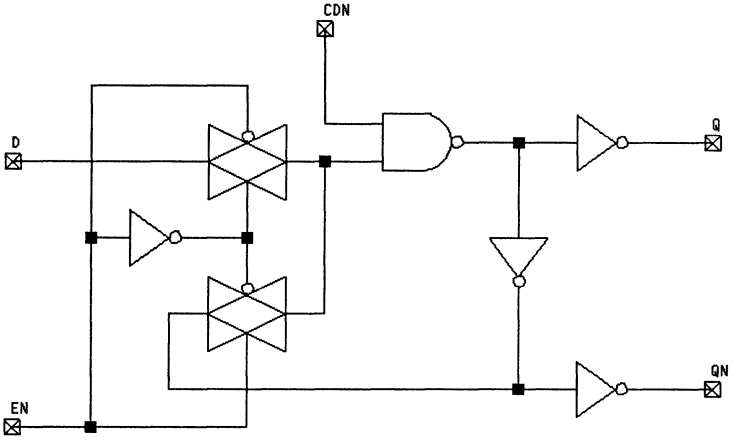
BUFFERED LATCH W/CLEAR

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



LAE02

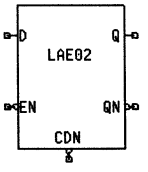
D-LATCH, W/CLEAR

DESCRIPTION

The LAE02 is a D-Latch, identical to LAE01, except that an Active-LOW CLEAR has been added. Information present at the Data Input D is transferred to the Q and QN outputs when the ENABLE signal, EN, is LOW. The Q output will follow the input, D, as long as ENABLE remains LOW. When the ENABLE goes HIGH, information at the Data input at the time of transition is retained until ENABLE goes LOW. A LOW on the CDN input overrides other inputs to pull Q LOW. QN drives two internal loads.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	
CDN	D	EN	Q	QN
L	X	X	L	H
H	L	L	L	H
H	H	L	H	L
H	X	H	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
EN	Input	2.0	ENABLE Input (Active-LOW)
CDN	Input	1.0	CLEAR Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

LAE02

D-LATCH, W/CLEAR

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, EN-Q	1.9 + 0.9 + 0.53 * UL	2.2 + 0.6 + 0.37 * UL
tQN, EN-QN	1.5 + 0.9 + 0.18 * UL	1.5 + 0.7 + 0.15 * UL
tDQ, D-Q	1.5 + 0.8 + 0.31 * UL	2.0 + 0.4 + 0.18 * UL
tCQ, CDN-Q		1.4 + 0.6 + 0.37 * UL
tCQN, CDN-QN	0.9 + 0.8 + 0.18 * UL	

tWEN, EN	2.2	ns
tS, D-EN	1.8	ns
tH, EN-D	0	ns
tREL, CDN-EN	0	ns
tWCDN, CDN	1.8	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

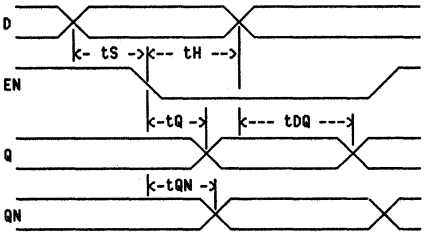
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	3.3	3.2	3.9	3.5	5.5	4.7	8.1	6.5
tQN	2.6	2.4	2.8	2.5	3.3	3.0	4.2	3.7
tDQ	2.6	2.6	2.9	2.8	3.8	3.3	5.4	4.2
tCQ		2.4		2.7		3.9		5.7
tCQN	1.9		2.1		2.6		3.5	

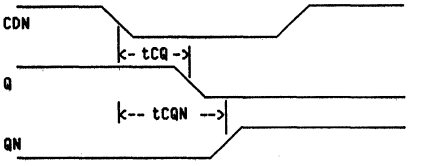
Note: For other operating conditions, use derating curves given in the performance section.

LAE02

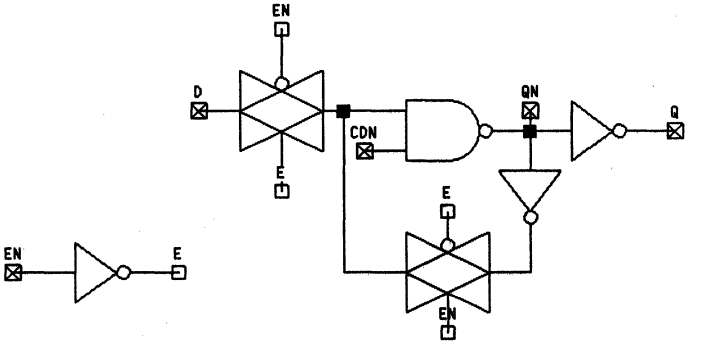
D-LATCH, W/CLEAR

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



LAE021

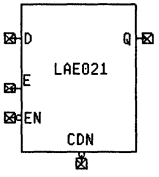
D-LATCH WITH CLEAR, EXTERNAL ENABLE

DESCRIPTION

The LAE021 is a D-Latch, with an asynchronous, Active-LOW CLEAR Input. Information present at the D Input while E is HIGH and EN is LOW is transferred to the Q Output. Data is latched while E is LOW, and EN is HIGH. E and EN must be complimentary for the proper operation of this macro.

Cells: 2 **Cell Type:** Internal

SYMBOL



FUNCTION

INPUTS				OUTPUT
D	E	EN	CDN	Q
X	X	X	L	L
L	H	L	H	L
H	H	L	H	H
X	L	H	H	Q

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
EN	Input	1.0	ENABLE Input
CDN	Input	1.0	CLEAR Input (Active-LOW)
Q	Output	-	Data Output

LAE021

D-LATCH WITH CLEAR, EXTERNAL ENABLE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, EN-Q	2.1 + 0.8 + 0.31 * UL	2.1 + 0.4 + 0.17 * UL
tDQ, D-Q	1.5 + 0.8 + 0.31 * UL	2.0 + 0.4 + 0.18 * UL
tCQ, CDN-Q		1.3 + 0.4 + 0.18 * UL

tWEN	2.2	ns
tS, D-EN	1.8	ns
tH, EN-D	0	ns
tREL, CDN-EN	0	ns
tWCDN, CDN	1.8	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

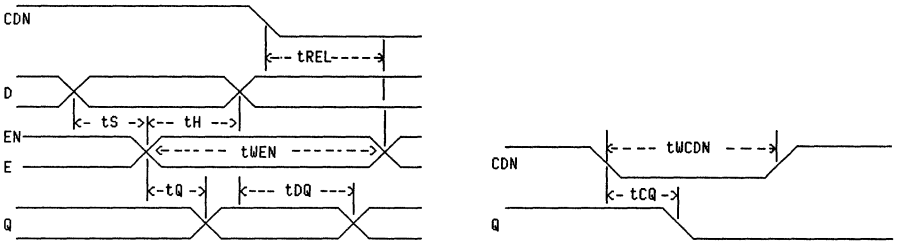
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	3.2	2.7	3.5	2.8	4.5	3.4	6.0	4.2
tDQ	2.6	2.6	2.9	2.8	3.9	3.3	5.4	4.2
tCQ		1.9		2.1		2.6		3.5

Note: For other operating conditions, use derating curves given in the performance section.

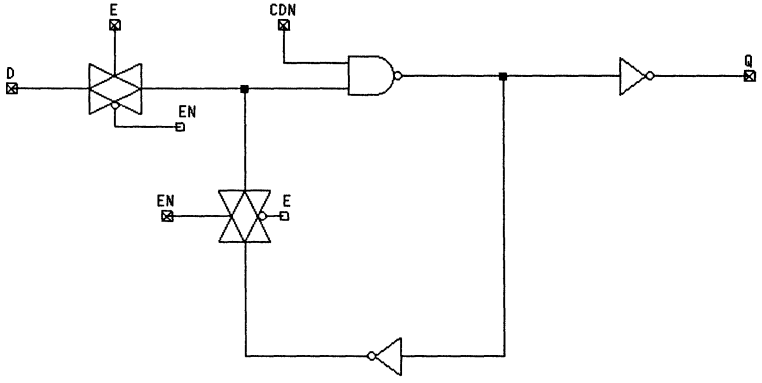
LAE021

D-LATCH WITH CLEAR, EXTERNAL ENABLE

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



LAE021T

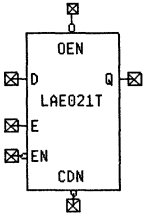
D-LATCH W/CLEAR, EXTERNAL ENABLE, AND 3-STATE OUTPUT

DESCRIPTION

The LAE021T is a D-Latch with an asynchronous, Active-LOW CLEAR Input. Information present at the D Input while E is HIGH and EN is LOW is transferred to the Q Output. Data is latched while E is LOW and EN is HIGH. E and EN must be complimentary for the proper operation of this macro. The Q Output is in a high-impedence state when OEN is HIGH.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION

INPUTS					OUTPUT
D	E	EN	CDN	OEN	Q
X	X	X	X	H	Z
X	X	X	L	L	L
L	H	L	H	L	L
H	H	L	H	L	H
X	L	H	H	L	Q

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
E	Input	1.0	ENABLE Input
EN	Input	1.0	Complimentary ENABLE Input
CDN	Input	1.0	CLEAR Input (Active-LOW)
OEN	Input	1.5	Output ENABLE (Active-LOW)
Q	Output	-	3-State Data Output

LAE021T

D-LATCH W/CLEAR, EXTERNAL ENABLE, AND 3-STATE OUTPUT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, EN-Q	2.5 + 1.3 + 0.56 * UL	2.3 + 0.6 + 0.26 * UL
tDQ, D-Q	1.9 + 1.3 + 0.56 * UL	2.3 + 0.6 + 0.56 * UL
tCQ, CDN-Q		1.6 + 0.6 + 0.26 * UL
tOE, OE-Z	0.1 + 0.8 + 0.58 * UL	0.6 + 0.6 + 0.26 * UL
tOD, OE-Z	1.1 ns	0.20 ns

tWEN, EN	2.0 ns
tS, D-EN	1.8 ns
tH, EN-D	0 ns
tREL, CDN-E	0 ns
tWCDN, CDN	1.8 ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

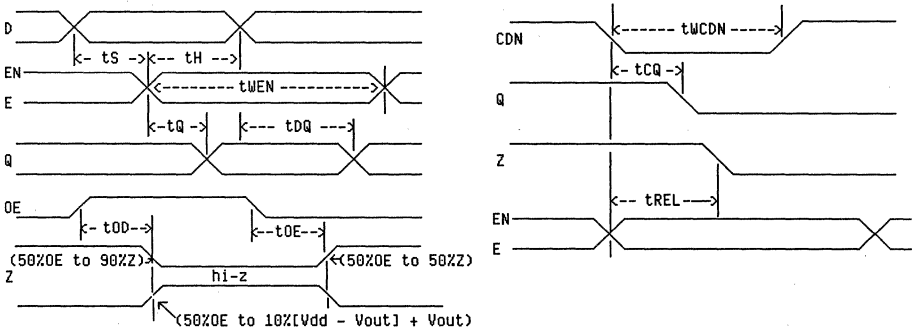
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	4.4	3.2	4.9	3.4	6.6	4.2	9.4	5.5
tDQ	3.8	3.5	4.3	4.0	6.0	5.7	8.8	8.5
tCQ		2.5		2.7		3.5		4.8
tOE	1.5	1.5	2.1	1.7	3.8	2.5	6.7	3.8
tOD	1.1	0.2	1.1	0.2	1.1	0.2	1.1	0.2

Note: For other operating conditions, use derating curves given in the performance section.

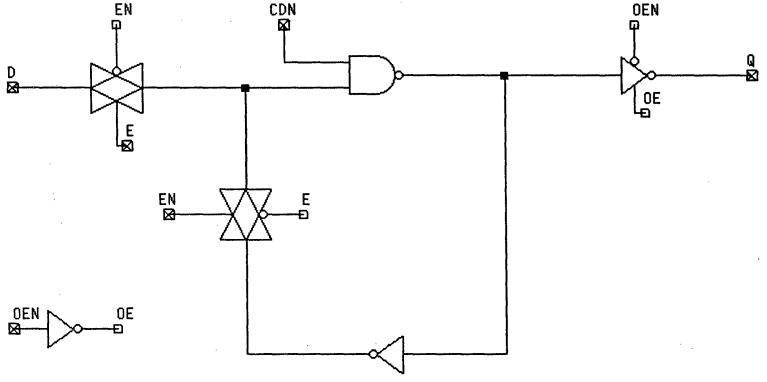
LAE021T

D-LATCH, W/CLEAR, EXTERNAL ENABLE, AND 3-STATE OUTPUT

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



MEM01

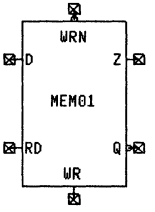
D-LATCH, GATED WITH 3-STATE OUTPUT

DESCRIPTION

The MEM01 is a D-Latch, gated, with 3-state Output. Data is transferred to the Q output when WRN is LOW. The output Q will follow the input as long as WRN remains LOW. Data present at input when WRN goes HIGH is retained until WRN goes LOW. The Z output is active when RD is HIGH, and 3-state when RD is LOW.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	
D	RD	WR	WRN	Q	Z
H	H	H	L	H	H
L	H	H	L	L	L
D	L	H	L	D	Z
X	L	L	H	Q	Z
X	H	L	H	Q	Z(t)

Q, Z(t) = State of Q, Z before transition on WR and WRN.

Z = High impedance state

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	1.0	Data Input
WR	Input	1.0	Write Input
WRN	Input	1.0	Complimentary Write Input
RD	Input	1.5	Read ENABLE
Q	Output	-	Data Output
Z	Output	-	3-State Output

MEM01

D-LATCH, GATED WITH 3-STATE OUTPUT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDQ, D-Q	1.7 + 1.2 + 0.25 * UL	3.0 + 0.7 + 0.15 * UL
tDZ, D-Z	3.7 + 1.1 + 0.53 * UL	4.8 + 0.8 + 0.39 * UL
tWQ, WR,WRN-Q	1.2 + 1.2 + 0.25 * UL	1.8 + 0.7 + 0.15 * UL
tWZ, WR,WNR-Z	3.2 + 1.1 + 0.53 * UL	3.6 + 0.8 + 0.39 * UL
tOE, RD-Z	1.1 + 0.1 + 0.06 * UL	0.1 + 0.1 + 0.06 * UL
tOD, RD-Z	0.41 ns	1.32 ns

tW, WR,WRN	2.0 ns
tS, D-WR,WRN	4.1 ns
tH, WR,WRN-D	0 ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

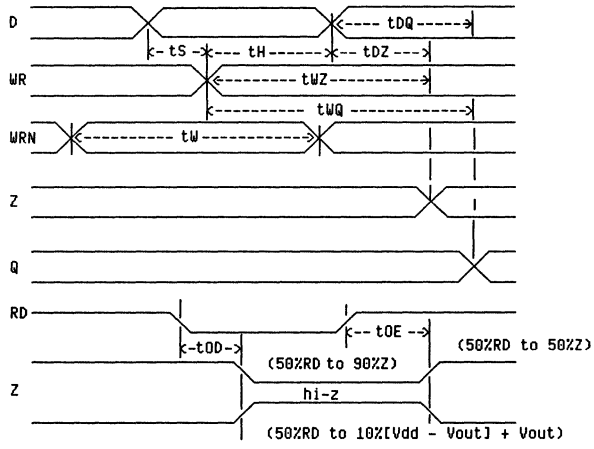
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDQ	3.2	3.9	3.4	4.0	4.2	4.5	5.4	5.2
tDZ	5.3	6.0	5.9	6.4	7.5	7.6	10.1	9.5
tWQ	2.7	2.7	2.9	2.8	3.7	3.3	4.9	4.0
tWZ	4.8	4.8	5.4	5.2	7.0	6.4	9.6	8.3
tOE	1.3	0.3	1.3	0.3	1.5	0.5	1.8	0.8
tOD	0.4	1.3	0.4	1.3	0.4	1.3	0.4	1.3

Note: For other operating conditions, use derating curves given in the performance section.

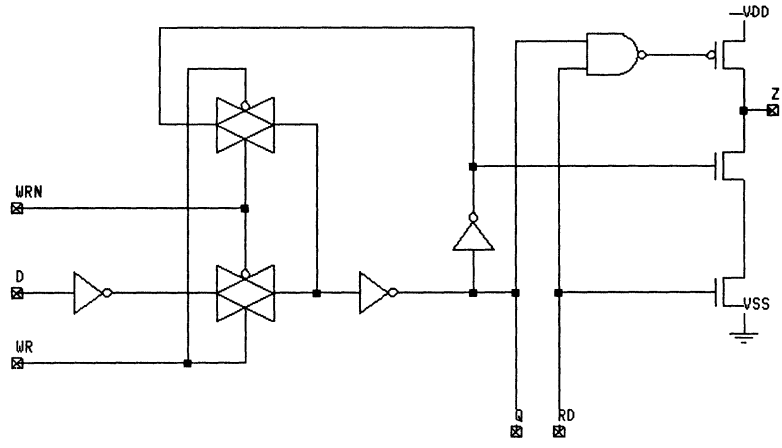
MEM01

D-LATCH, GATED WITH 3-STATE OUTPUT

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



MEM02

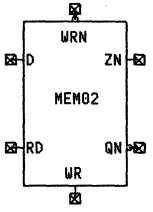
D-LATCH, GATED WITH 3-STATE OUTPUT

DESCRIPTION

The MEM02 is a D-Latch, gated, with 3-state Output. Data is transferred to the QN output when WRN is LOW. The output QN will follow the input as long as WRN remains LOW. Data present at input when WRN goes HIGH is retained until WRN goes LOW. The ZN output is active when RD is HIGH, and 3-State when RD is LOW.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	
D	RD	WR	WRN	QN	ZN
H	H	H	L	L	L
L	H	H	L	H	H
D	L	H	L	$\overline{D}$	Z
X	L	L	H	QN	Z
X	H	L	H	QN	ZN

Q, QN = State of Q, QN before transition on WR and WRN.

Z = High impedance state

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	1.0	Data Input
WR	Input	1.0	Write Input
WRN	Input	1.0	Complimentary Write Input
RD	Input	1.5	Read ENABLE
QN	Output	-	Data Output
ZN	Output	-	3-State Output

MEM02

D-LATCH, GATED WITH 3-STATE OUTPUT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDQ, D-QN	0.1 + 1.2 + 0.25 * UL	1.4 + 0.7 + 0.15 * UL
tDZ, D-ZN	2.4 + 1.1 + 0.53 * UL	3.0 + 0.8 + 0.39 * UL
tWQ,WR,WRN-QN	1.2 + 1.2 + 0.25 * UL	1.8 + 0.7 + 0.15 * UL
tWZ,WR,WRN-ZN	3.2 + 1.1 + 0.53 * UL	3.6 + 0.8 + 0.39 * UL
tOE, RD-ZN	1.1 + 0.1 + 0.06 * UL	0.1 + 0.1 + 0.06 * UL
tOD, RD-ZN	0.41 ns	1.32 ns

tW, WR,WRN	2.0	ns
tS, D-WR,WRN	4.1	ns
tH, WR,WRN-D	0	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

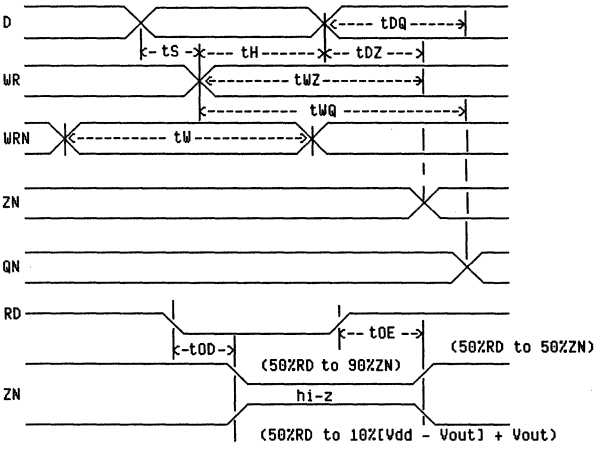
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDQ	1.6	2.3	1.8	2.4	2.6	2.9	3.8	3.6
tDZ	4.0	4.2	4.6	4.6	6.2	5.8	8.8	7.7
tWQ	2.7	2.7	2.9	2.8	3.7	3.3	4.9	4.0
tWZ	4.8	4.8	5.4	5.2	7.0	6.4	9.6	8.3
tOE	1.3	0.3	1.3	0.3	1.5	0.5	1.8	0.8
tOD	0.4	1.3	0.4	1.3	0.4	1.3	0.4	1.3

Note: For other operating conditions, use derating curves given in the performance section.

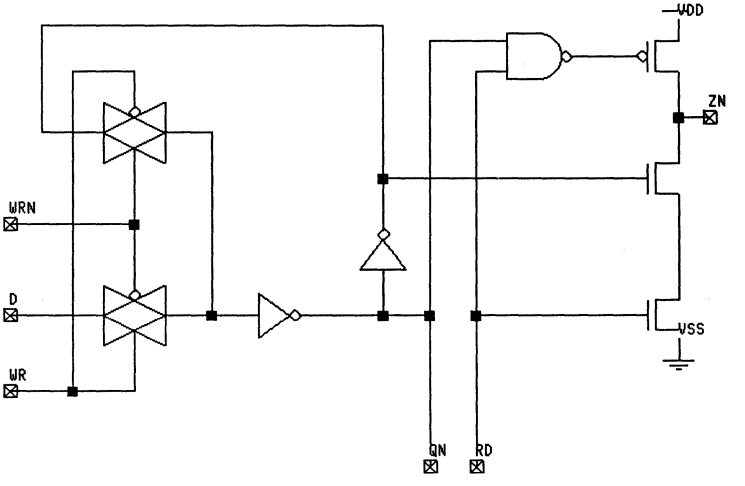
MEM02

D-LATCH, GATED WITH 3-STATE OUTPUT

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



DFP01

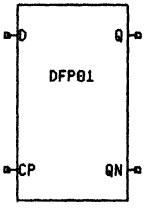
D FLIP-FLOP

DESCRIPTION

The DFP01 is a positive edge-triggered Master/Slave D Flip-Flop. Information at the D Input is transferred to the output on the positive edge of the clock pulse. After the clock pulse input threshold has been exceeded, the data input is locked out and information present will not be transferred to the outputs until the next rising edge of the clock pulse. Q drives 1 internal load.

Cells: 4 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
D	CP	Q	QN
L	⌐	L	H
H	⌐	H	L
X	L	Q	QN
X	H	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
CP	Input	1.0	Clock Input
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

DFP01

D FLIP-FLOP

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CP-Q	3.3 + 1.0 + 0.27 * UL	3.2 + 0.5 + 0.13 * UL
tQN, CP-QN	4.0 + 0.8 + 0.47 * UL	4.1 + 0.9 + 0.49 * UL

fMAX, Cld = 1.0 pF	92	MHz
tWCP, CP	4.2	ns
tS, D-CP	2.7	ns
tH, CP	0	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

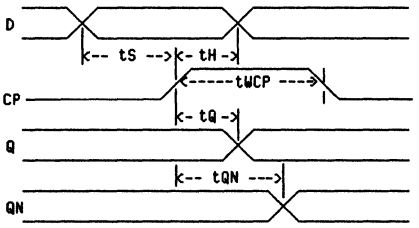
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	4.6	3.8	4.8	4.0	5.7	4.4	7.0	5.0
tQN	5.3	5.5	5.7	6.0	7.2	7.5	9.5	9.9

Note: For other operating conditions, use derating curves given in the performance section.

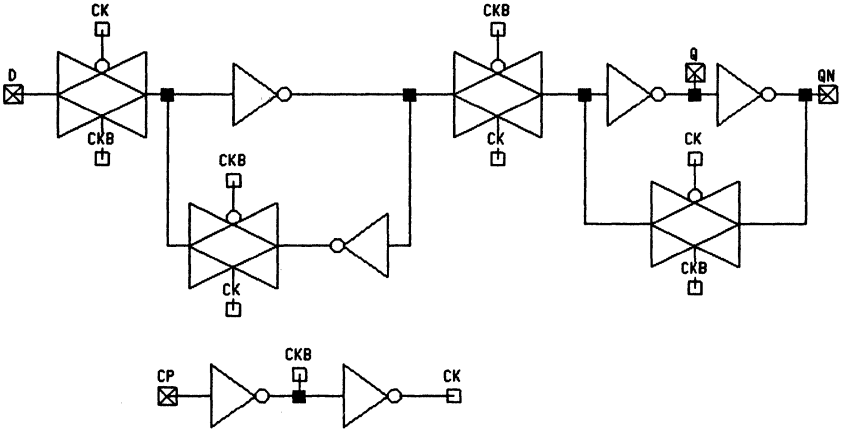
DFP01

D FLIP-FLOP

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



DFP74

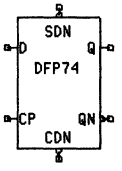
D FLIP-FLOP W/SET, CLEAR

DESCRIPTION

The DFP74 is a Master Slave D-type Flip-Flop with asychronous SET and CLEAR. The macro is positive edge-triggered; information on the D Input is transferred to the Q Outputs on the rising edge of the clock pulse.

Cells: 6 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	
CP	SDN	CDN	D	Q	QN
X	H	L	X	L	H
X	L	H	X	H	L
X	L	L	X	L*	L*
⌐⌐	H	H	L	L	H
⌐⌐	H	H	H	H	L
H	H	H	X	D	DN

*UNSTABLE STATE

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
CP	Input	1.0	Clock Input (positive-edge)
SDN	Input	2.0	SET Input (Active-LOW)
CDN	Input	2.0	CLEAR Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

DFP74

D FLIP-FLOP W/SET, CLEAR

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CP-Q	4.1 + 0.5 + 0.28 * UL	3.8 + 0.3 + 0.15 * UL
tQN, CP-QN	5.5 + 0.6 + 0.26 * UL	6.3 + 0.3 + 0.12 * UL
tSQ, SDN-Q	8.1 + 0.5 + 0.27 * UL	
tSQN, SDN-QN		1.8 + 0.3 + 0.12 * UL
tCQ, CDN-Q		0.8 + 0.3 + 0.15 * UL
tCQN, CDN-QN	5.7 + 0.5 + 0.24 * UL	

fMAX, Cld = 1.0 pF	70	MHz
tWCP, CP	4.2	ns
tS, D-CP	3.1	ns
tH, CP-D	0	ns
tREL, CDN/SDN-CP	0	ns
tWCDN, CDN	3.6	ns
tWSDN, SDN	2.9	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

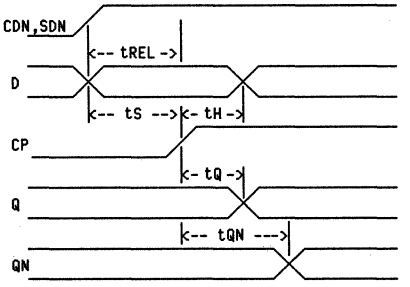
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	4.9	4.3	5.2	4.4	6.0	4.9	7.4	5.6
tQN	6.4	6.7	6.6	6.8	7.4	7.2	8.7	7.8
tSQ	8.9		9.1		10.0		11.3	
tSQN		2.2		2.3		2.7		3.3
tCQ		1.3		1.4		1.9		2.6
tCQN	6.4		6.7		7.4		8.6	

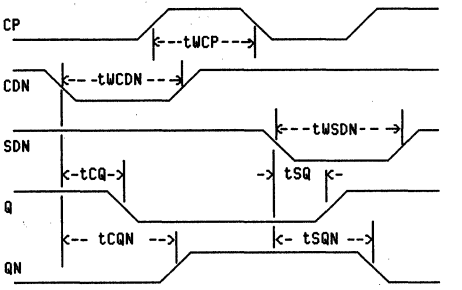
Note: For other operating conditions, use derating curves given in the performance section.

DFP74

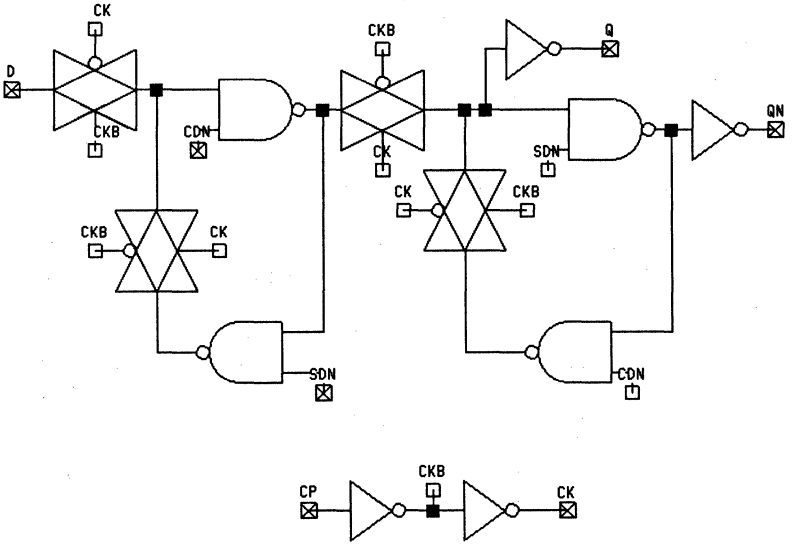
D FLIP-FLOP W/SET, CLEAR

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



DFP011

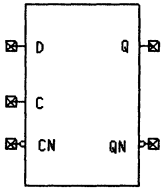
D FLIP-FLOP W/EXTERNAL CLOCKS

DESCRIPTION

DFP011 is a positive edge-triggered D Flip-Flop with external clocks C and CN. Information present at input D during the positive edge of C and negative of CN is transferred to outputs Q and QN and is locked during a clock pulse until the next rising edge of C and falling edge of CN.

Cells: 4 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	
C	CN	D	Q	QN
⎍	⎾	L	L	H
⎍	⎾	H	H	L
L	H	X	Q	QN
H	L	X	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
Cn	Input	2.0	Clock Input
CN	Input	2.0	Complimentary Clock Input
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

DFP011

D FLIP-FLOP W/EXTERNAL CLOCKS

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, C-Q	1.2 + 0.6 + 0.28 * UL	1.3 + 0.5 + 0.21 * UL
tQN, C-QN	2.9 + 0.5 + 0.23 * UL	2.6 + 0.3 + 0.15 * UL

fMAX, Cld = 1.0 pF	112	MHz
tW, C	2.6	ns
tS, D-C,CN	2.0	ns
tH, C,CN-D	0	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

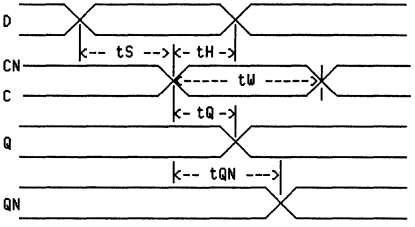
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	2.1	2.0	2.4	2.2	3.2	2.9	4.6	3.9
tQN	3.6	3.1	3.9	3.2	4.6	3.7	5.7	4.4

Note: For other operating conditions, use derating curves given in the performance section.

DFP011

D FLIP-FLOP W/EXTERNAL CLOCKS

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM

DFP011T

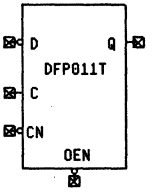
D FLIP-FLOP W/3-STATE OUTPUT AND EXTERNAL CLOCKS

DESCRIPTION

DFP011T is a positive edge-triggered D Flip-Flop with external clocks C and CN, and 3-state output, OEN. Information present at input D is transferred to output Q during the rising edge of C and falling edge of CN, and is locked during the clock pulse until the next rising edge of C and CN. Output Q is enabled when OEN is set LOW and goes to high impedance when OEN is set to HIGH.

Cells: 4 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUT
C	CN	OEN	D	Q
L	H	L	X	D
X	X	H	X	Z
↓	↑	L	L	L
↓	↑	L	H	H
H	L	L	X	D

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
C	Input	2.0	Clock Input
CN	Input	2.0	Complimentary Clock Input
OEN	Input	1.0	Output ENABLE (Active-LOW)
Q	Output	-	3-State Data Output

DFP011T

D FLIP-FLOP W/3-STATE OUTPUT AND EXTERNAL CLOCKS

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, C-Q	2.0 + 1.1 + 0.50 * UL	1.8 + 0.6 + 0.26 * UL
tOE, OEN-Q	0.6 + 1.9 + 0.82 * UL	1.3 + 0.6 + 0.26 * UL
tOD, OEN-Q	0.2 ns	0.8 ns

fMAX, Cld = 1.0 pF	109	MHz
tW, C	2.1	ns
tS, D-C,CN	2.2	ns
tH, C,CN-D	0	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

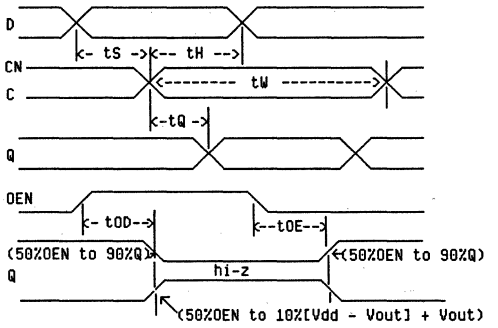
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	3.6	2.7	4.1	2.9	5.6	3.7	8.1	5.0
tOE	3.3	2.2	4.1	2.4	6.6	3.2	10.7	4.5
tOD	0.2	0.8	0.2	0.8	0.2	0.8	0.2	0.8

Note: For other operating conditions, use derating curves given in the performance section.

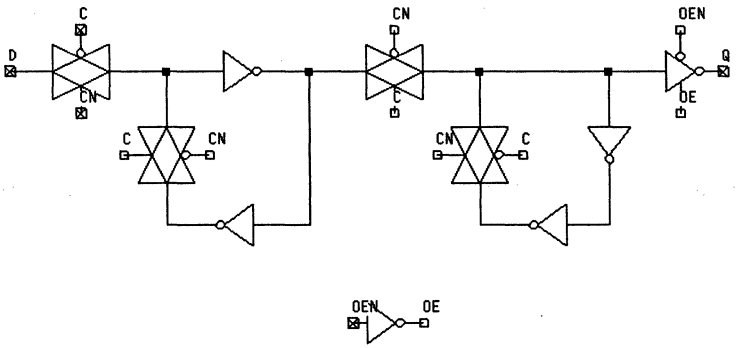
DFP011T

D FLIP-FLOP W/3-STATE OUTPUT AND EXTERNAL CLOCKS

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



DFP01S

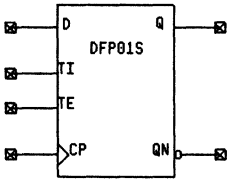
D FLIP-FLOP W/ SCAN LOGIC

DESCRIPTION

The DFP01S is a positive edge-triggered Master/Slave D Flip-Flop. Information at the D input is transferred to the output on the positive edge of the clock pulse. After the clock pulse input threshold has been passed, the data input is locked out and information present will not be transferred to the outputs until the next rising edge of the clock pulse pulse input. This macro contains a 2:1 multiplexer on the data input to support Scan Data path test methodology.

Cells: 6 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	
CP	TE	TI	D	Q	QN
⎍	H	L	X	L	H
⎍	H	H	X	H	L
⎍	L	X	L	L	H
⎍	L	X	H	H	L
L	X	X	X	Q	QN
H	X	X	X	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	1.0	Data Input
TI	Input	1.0	Test Data Input
CP	Input	1.0	Clock Pulse Input (Positive-Edge)
TE	Input	2.0	Test ENABLE Input
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

DFP01S

D FLIP-FLOP W/ SCAN LOGIC

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CP-Q	4.4 + 0.6 + 0.26 * UL	4.8 + 0.3 + 0.12 * UL
tQN, CP-QN	3.3 + 0.7 + 0.28 * UL	3.5 + 0.4 + 0.17 * UL

fMAX, Cld = 1.0 pF	86	MHz
tWCP, CP	4.0	ns
tS, TE-CP	4.3	ns
tSTI, TI-CP	5.1	ns
tH, D,TI-CP;TE-CP	0	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

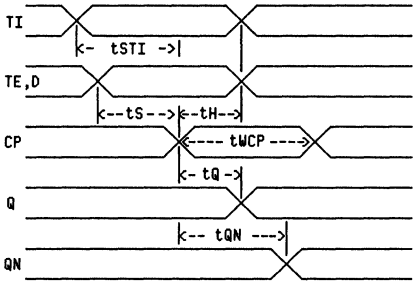
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	5.3	5.2	5.5	5.3	6.3	5.7	7.6	6.3
tQN	4.3	4.1	4.6	4.2	5.4	4.8	6.8	5.6

Note: For other operating conditions, use derating curves given in the performance section.

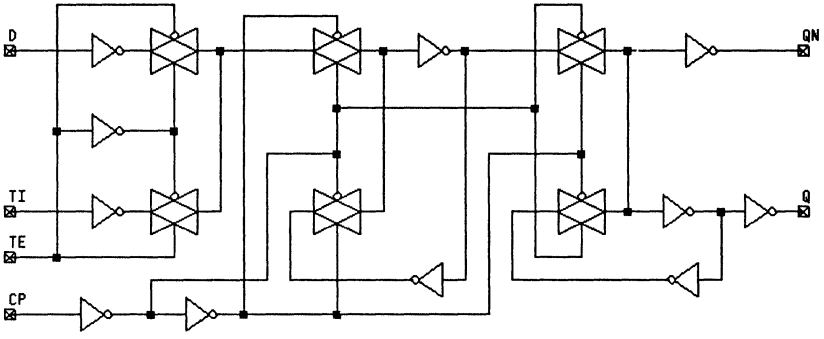
DFP01S

D FLIP-FLOP W/ SCAN LOGIC

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



DFP02

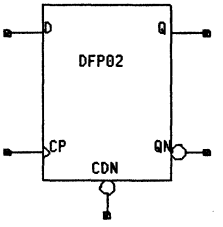
D FLIP-FLOP W/CLEAR DIRECT

DESCRIPTION

DFP02 is a positive-edge triggered Master-Slave D type Flip-Flop with asynchronous clear. The data present at D enters the master when the clock is LOW, and is transferred to the outputs on the positive transition of the clock. A LOW on the CDN input overrides all inputs to pull Q LOW.

Cells: 5 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	
CDN	CP	D	Q	QN
L	X	X	L	H
H	⌋⌈	L	L	H
H	⌋⌈	H	H	L
H	L	X	Q	QN
H	H	X	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	1.0	Data Input
CP	Input	1.0	Clock Input (Positive-Edge)
CDN	Input	2.0	Asynchronous CLEAR Input
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

DFP02

D FLIP-FLOP W/CLEAR DIRECT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CP-Q	4.7 + 0.7 + 0.27 * UL	4.8 + 0.3 + 0.13 * UL
tQN, CP-QN	5.5 + 0.6 + 0.26 * UL	6.2 + 0.3 + 0.12 * UL
tCQ, CDN-Q		2.3 + 0.3 + 0.13 * UL
tCQN, CDN-QN	3.8 + 0.7 + 0.27 * UL	

fMAX, Cld = 1.0 pF	87	MHz
tWCP, CP	3.5	ns
tS, D-CP	2.8	ns
tH, CP-D	0	ns
tREL, CDN-CP	0	ns
tWCDN, CDN	3.4	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

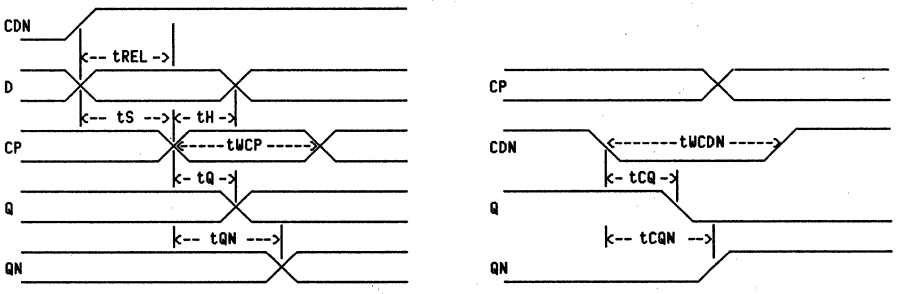
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	5.7	5.2	5.9	5.4	6.8	5.8	8.1	6.4
tQN	6.4	6.6	6.6	6.7	7.4	7.1	8.7	7.7
tCQ		2.7		2.9		3.3		3.9
tCQN	4.8		5.0		5.9		7.2	

Note: For other operating conditions, use derating curves given in the performance section.

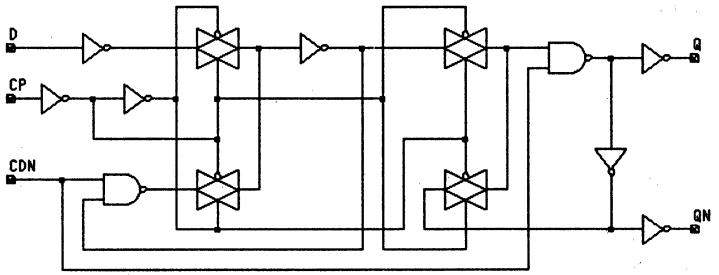
DFP02

D FLIP-FLOP W/CLEAR DIRECT

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



DFP021

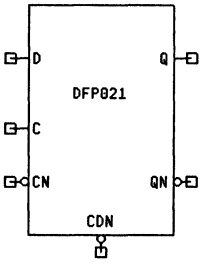
D FLIP-FLOP WITH CLEAR, EXTERNAL CLOCKS

DESCRIPTION

The DFP021 is a positive edge-triggered D Flip-Flop with an asynchronous, active-LOW CLEAR input. Information present at the D input during the positive edge of C and the negative edge of CN, is transferred to the Q and QN outputs. External complimentary clocks must be provided for the proper operation of this macro.

Cells: 4 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	
CDN	C	CN	D	Q	QN
L	X	X	X	L	H
H	⌐	⌐	L	L	H
H	⌐	⌐	H	H	L
H	L	H	X	Q	QN
H	H	L	X	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
C	Input	2.0	Clock Input
CN	Input	2.0	Complementary Clock Input
CDN	Input	2.0	CLEAR Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

DFP021

D FLIP-FLOP WITH CLEAR, EXTERNAL CLOCKS

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, C-Q	2.3 + 0.8 + 0.33 * UL	2.6 + 0.4 + 0.17 * UL
tQN, C-QN	3.2 + 0.6 + 0.26 * UL	3.7 + 0.4 + 0.15 * UL
tCQ, CDN-Q		1.4 + 0.4 + 0.15 * UL
tCQN, CDN-QN	1.5 + 0.6 + 0.26 * UL	

fMAX, Cld = 1.0 pF	103	MHz
tWC, C	2.4	ns
tS, D-C	2.0	ns
tH, C-D	0	ns
tREL, CDN-C	2.5	ns
tWCDN, CDN	2.7	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

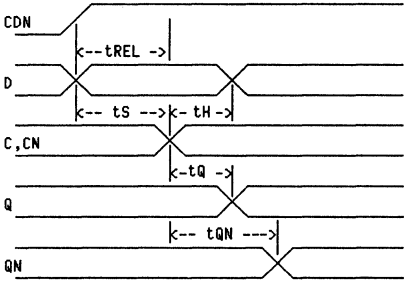
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	3.4	3.2	3.8	3.3	4.8	3.9	6.4	4.7
tQN	4.1	4.3	4.3	4.4	5.1	4.9	6.4	5.6
tCQ		2.0		2.1		2.6		3.3
tCQN	2.4		2.6		3.4		4.7	

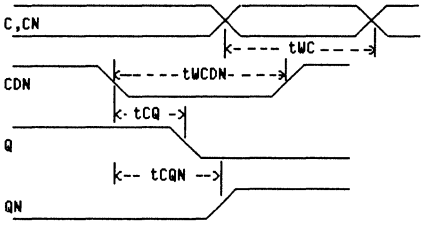
Note: For other operating conditions, use derating curves given in the performance section.

DFP021

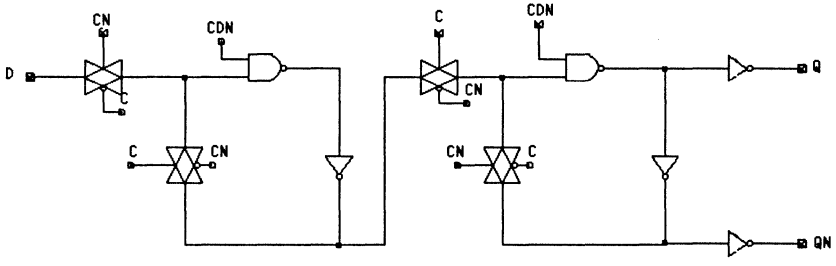
D FLIP-FLOP WITH CLEAR, EXTERNAL CLOCKS

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



DFP021T

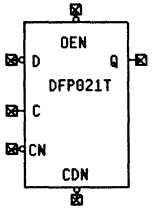
D FLIP-FLOP W/CLEAR, EXTERNAL CLOCKS AND 3-STATE OUTPUT

DESCRIPTION

The DFP021T is a positive edge-triggered D Flip-Flop with external clocks C and CN, active-LOW CLEAR, CDN, and 3-state output OEN. Information present at input D is transferred to output Q during the rising edge of C and the falling edge of CN, and remains latched until the next edge-trigger of C and CN. Output is set to LOW when CDN is enabled LOW and is in high impedance state when OEN is set to HIGH.

Cells: 5 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS					OUTPUT
CDN	C	CN	OEN	D	Q
L	X	X	L	X	L
X	X	X	H	X	Z
H	↓	↑	L	L	L
H	↓	↑	L	H	H
H	↓	↑	H	L	Z
H	↓	↑	H	H	Z
H	L	H	L	X	Q
H	L	H	H	X	Z

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
C	Input	2.0	Clock Input
CN	Input	2.0	Complimentary Clock Input
CDN	Input	2.0	CLEAR Input (Active-LOW)
OEN	Input	1.0	Output ENABLE (Active-LOW)
Q	Output	-	3-State Data Output

DFP021T

D FLIP-FLOP W/CLEAR, EXTERNAL CLOCKS AND 3-STATE OUTPUT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, C-Q	3.9 + 1.1 + 0.50 * UL	2.9 + 0.5 + 0.23 * UL
tCQ, CDN-Q		2.0 + 0.5 + 0.23 * UL
tOE, OEN-Q	0.6 + 1.9 + 0.82 * UL	1.4 + 0.6 + 0.24 * UL
tOD, OEN-Q	0.2 ns	0.8 ns

fMAX, Cld = 1.0 pF	69	MHz
tW, C	2.3	ns
tS, D-C,CN	3.5	ns
tH, C,CN-D	0	ns
tREL, CDN-C,CN	1.3	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

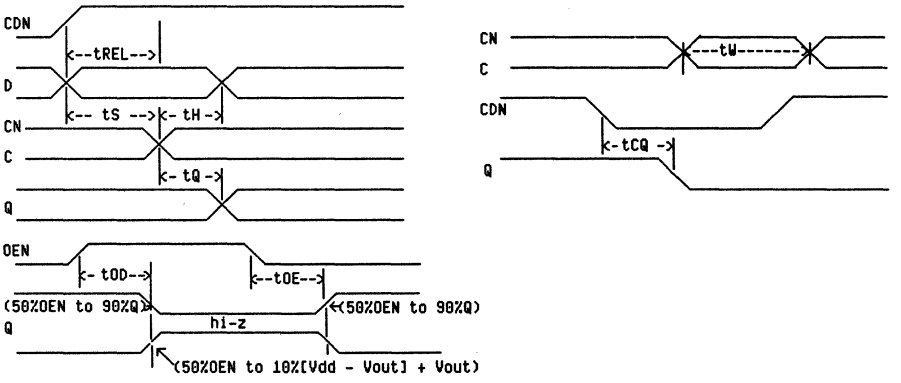
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	5.5	3.6	6.0	3.9	7.5	4.6	10.0	5.7
tCQ		2.7		3.0		3.7		4.8
tOE	3.3	2.2	4.1	2.5	6.6	3.2	10.7	4.4
tOD	0.2	0.8	0.2	0.8	0.2	0.8	0.2	0.8

Note: For other operating conditions, use derating curves given in the performance section.

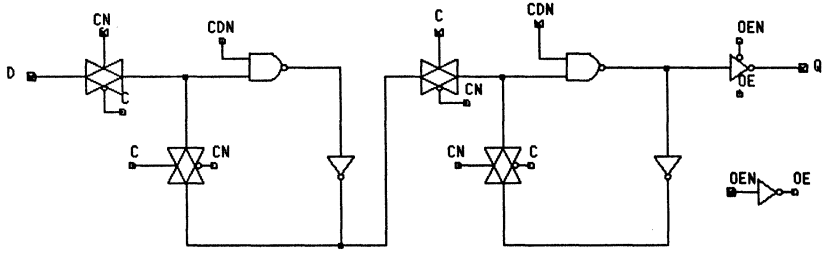
DFP021T

D FLIP-FLOP W/CLEAR, EXTERNAL CLOCKS AND 3-STATE OUTPUT

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



DFP02S

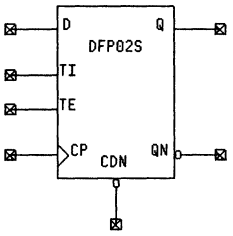
D FLIP-FLOP WITH SCAN, CLEAR

DESCRIPTION

The DFP02S is a Master/Slave D type Flip-Flop with asynchronous Active-LOW CLEAR. The macro contains a 2:1 mux on the data input to support Scan Data path test methodology.

Cells: 7 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS					OUTPUTS	
CDN	CP	TE	TI	D	Q	QN
L	X	X	X	X	L	H
H	⌐	H	L	X	L	H
H	⌐	H	H	X	H	L
H	⌐	L	X	L	L	H
H	⌐	L	X	H	H	L
H	L	X	X	X	Q	QN
H	H	X	X	X	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	1.0	Data Input
TI	Input	1.0	Test Data Input
TE	Input	1.0	Test ENABLE
CP	Input	1.0	Clock Input
CDN	Input	2.0	CLEAR Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

DFP02S

D FLIP-FLOP WITH SCAN, CLEAR

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CP-Q	4.7 + 0.6 + 0.27 * UL	4.7 + 0.3 + 0.13 * UL
tQN, CP-QN	5.5 + 0.6 + 0.26 * UL	6.2 + 0.3 + 0.12 * UL
tCQ, CDN-Q		2.3 + 0.3 + 0.13 * UL
tCQN, CDN-QN	3.8 + 0.6 + 0.27 * UL	

fMAX, Cld = 1.0 pF	72	MHz
tWCP, CP	4.0	ns
tS, D-CP	5.1	ns
tSTE, TE-CP	4.3	ns
tH, CP-D,TE,TI	0	ns
tREL, CDN-CP	0	ns
tWCDN, CDN	3.3	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

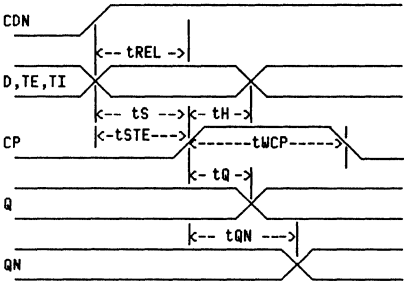
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	5.6	5.1	5.8	5.3	6.7	5.7	8.0	6.3
tQN	6.4	6.6	6.6	6.7	7.4	7.1	8.7	7.7
tCQ		2.7		2.9		3.3		3.9
tCQN	4.7		4.9		5.8		7.1	

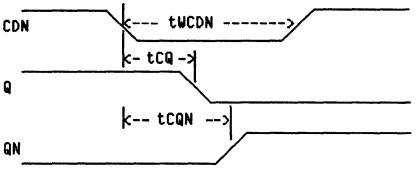
Note: For other operating conditions, use derating curves given in the performance section.

DFP02S

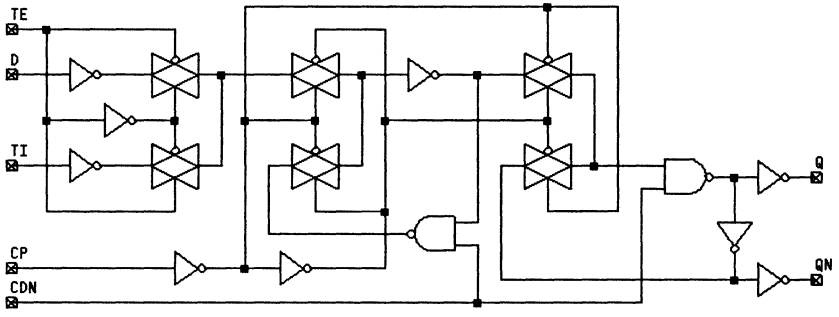
D FLIP-FLOP WITH SCAN, CLEAR

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



DFP03

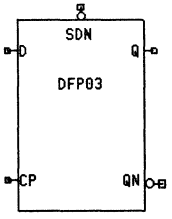
D FLIP-FLOP WITH SET

DESCRIPTION

The DFP03 is a positive edge-triggered D Flip-Flop with an asynchronous, Active-LOW SET Input. Information present at the D Input during the positive edge of CP is transferred to the Q and QN Outputs.

Cells: 5 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	
D	CP	SDN	Q	QN
X	X	L	H	L
L	⌐	H	L	H
H	⌐	H	H	L
X	L	H	Q	QN
X	H	H	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
CP	Input	1.0	Clock Input
SDN	Input	2.0	SET Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

DFP03

D FLIP-FLOP WITH SET

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CP-Q	6.5 + 0.7 + 0.28 * UL	6.4 + 0.3 + 0.13 * UL
tQN, CP-QN	5.0 + 0.7 + 0.31 * UL	6.1 + 0.4 + 0.15 * UL
tSQ, SDN-Q	2.4 + 0.7 + 0.28 * UL	
tSQN, SDN-QN		1.6 + 0.4 + 0.18 * UL

fMAX, Cld = 1.0 pF	95	MHz
tWCP, CP	2.6	ns
tS, D-CP	2.5	ns
tH, CP-D	0	ns
tREL, SDN-CP	0	ns
tWSDN, SDN	2.9	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

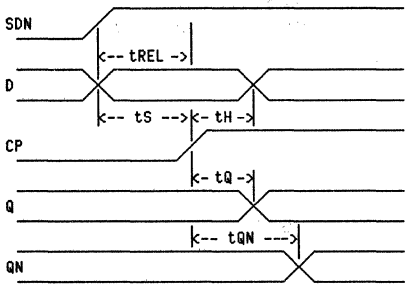
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	7.5	6.8	7.8	7.0	8.6	7.4	10.0	8.0
tQN	6.0	6.7	6.3	6.8	7.3	7.3	8.8	8.0
tSQ	3.4		3.7		4.5		5.9	
tSQN		2.2		2.4		2.9		3.8

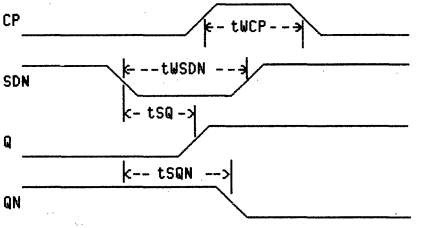
Note: For other operating conditions, use derating curves given in the performance section.

DFP03

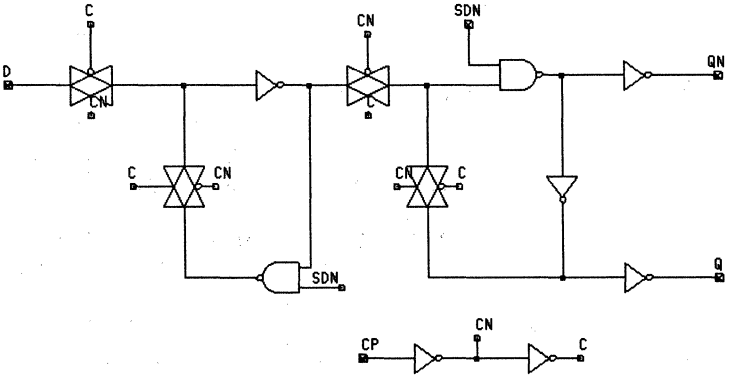
D FLIP-FLOP WITH SET

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



DFP031

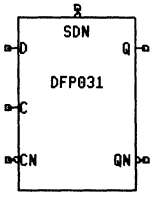
D FLIP-FLOP WITH SET, EXTERNAL CLOCKS

DESCRIPTION

The DFP031 is a positive edge-triggered Flip-Flop with an asynchronous, Active-LOW SET Input. Information present at the D Input during the positive edge of C and the negative edge of CN is transferred to the Q and QN Outputs. External complimentary clocks must be provided for the proper operation of this macro.

Cells: 4 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	
D	C	CN	SDN	Q	QN
X	X	X	L	H	L
L	⌐	¬	H	L	H
H	⌐	¬	H	H	L
X	L	H	H	Q	QN
X	H	L	H	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	4.0	Data Input
C	Input	2.0	Clock Input
CN	Input	2.0	Complimentary Clock Input
SDN	Input	2.0	SET Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

DFP031

D FLIP-FLOP WITH SET, EXTERNAL CLOCKS

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, C-Q	3.7 + 0.7 + 0.30 * UL	4.4 + 0.4 + 0.17 * UL
tQN, C-QN	3.2 + 0.8 + 0.33 * UL	2.9 + 0.5 + 0.20 * UL
tSQ, SDN-Q	2.6 + 0.7 + 0.30 * UL	
tSQN, SDN-QN		1.7 + 0.5 + 0.20 * UL

fMAX, Cld = 1.0 pF	101	MHz
tWC, C	2.6	ns
tS, D-C	2.5	ns
tH, C-D	0	ns
tREL, SDN-C	0	ns
tWSDN, SDN	2.8	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

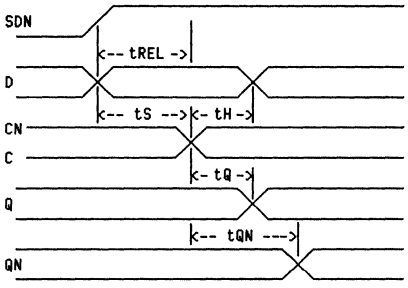
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	4.7	5.0	5.0	5.1	5.9	5.7	7.4	6.5
tQN	4.3	3.6	4.7	3.8	5.7	4.4	7.3	5.4
tSQ	3.6		3.9		4.8		6.3	
tSQN		2.4		2.6		3.2		4.2

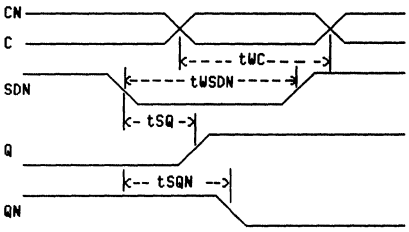
Note: For other operating conditions, use derating curves given in the performance section.

DFP031

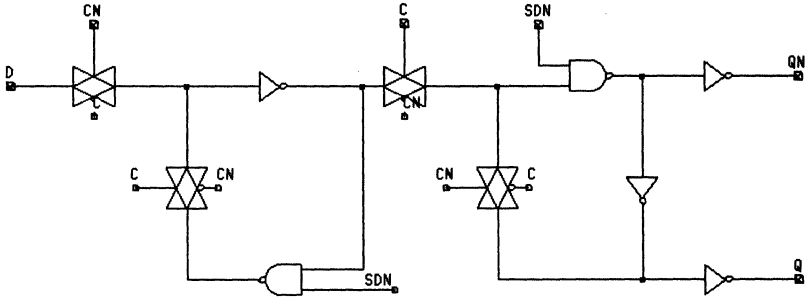
D FLIP-FLOP WITH SET, EXTERNAL CLOCKS

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



DFP04

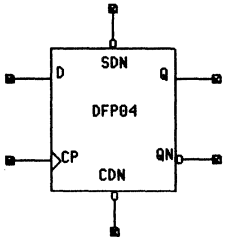
D FLIP-FLOP W/SET AND CLEAR

DESCRIPTION

The DFP04 is a Master-Slave D Flip-Flop with asynchronous SET and CLEAR. Information at the D Input is transferred to the output on the positive edge of the clock pulse. After the clock pulse input threshold has been passed, the data input is locked out and information present will not be transferred to the outputs until the next rising edge of the clock pulse input.

Cells: 6 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	
CDN	SDN	CP	D	Q	QN
L	H	X	X	L	H
H	L	X	X	H	L
H	H	⌐	L	L	H
H	H	⌐	H	H	L
H	H	L	X	Q	QN
H	H	H	X	Q	QN
L	L	X	X	L*	L*

* Unstable state

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	1.0	Data Input
CP	Input	1.0	Clock Pulse Input
SDN	Input	2.0	SET Input (Active-LOW)
CDN	Input	2.0	CLEAR Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

DFP04

D FLIP-FLOP W/SET AND CLEAR

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CP-Q	4.7 + 0.6 + 0.27 * UL	5.5 + 0.3 + 0.14 * UL
tQN, CP-QN	7.2 + 0.6 + 0.27 * UL	6.3 + 0.3 + 0.13 * UL
tCQ, CDN-Q		1.8 + 0.3 + 0.13 * UL
tCQN, CDN-QN	4.5 + 0.7 + 0.29 * UL	
tSQ, SDN-Q	5.7 + 0.6 + 0.27 * UL	
tSQN, SDN-QN		3.3 + 0.4 + 0.16 * UL

fMAX, Cld = 1.0 pF	77	MHz
tWCP, CP	4.2	ns
tS, D/TI-CP	3.3	ns
tH, CP-D/TI	0	ns
tREL, CDN/SDN-CP	0	ns
tWCDN, CDN	4.7	ns
tWSDN, SDN	4.2	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

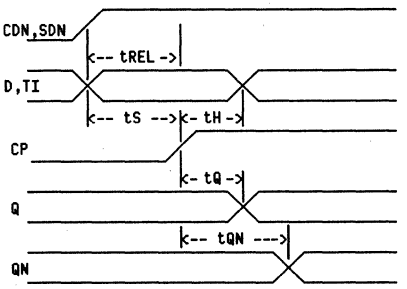
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	5.6	5.9	5.8	6.1	6.7	6.5	8.0	7.2
tQN	8.1	6.7	8.3	6.9	9.2	7.3	10.5	7.9
tCQ		2.2		2.4		2.8		3.4
tCQN	5.5		5.8		6.7		8.1	
tSQ	6.6		6.8		7.7		9.0	
tSQN		3.9		4.0		4.5		5.3

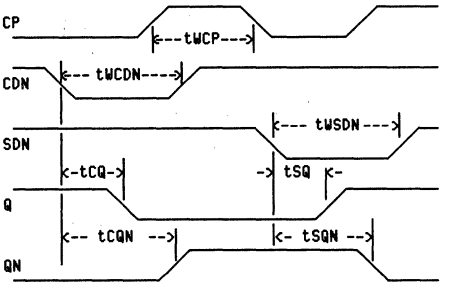
Note: For other operating conditions, use derating curves given in the performance section.

DFP04

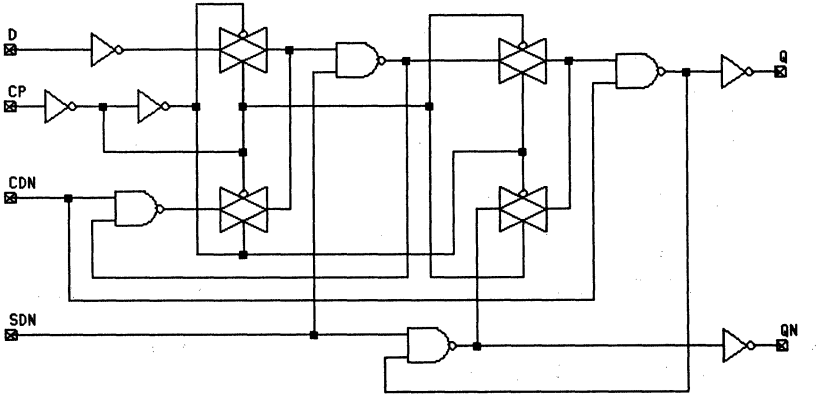
D FLIP-FLOP W/SET AND CLEAR

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



DFP05

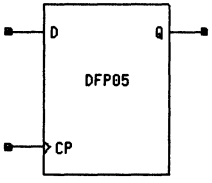
D FLIP-FLOP W/BUFFERED OUTPUT

DESCRIPTION

The DFP05 is a positive edge-triggered D Flip-Flop with buffered Data, D, and Output, Q. The DFP05 differs from the DFP01 in that it has no QN output.

Cells: 4 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
CP	D	Q
⌐	L	L
⌙	L	Q
⌐	H	H
⌙	H	Q

Q = Previous state

PIN DESCRIPTION

Name	Type	U.L.	Description
D	Input	1.0	Data Input
CP	Input	1.0	Clock Pulse Input (Positive Edge-Triggered)
Q	Output	-	Data Output

DFP05

D FLIP-FLOP W/BUFFERED OUTPUT

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CP-Q	3.9 + 0.6 + 0.27 * UL	4.4 + 0.3 + 0.13 * UL

fMAX, Cld = 1.0 pF	92	MHz
tWCP, CP	3.4	ns
tS, D-CP	2.5	ns
tH, CP-D	0	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

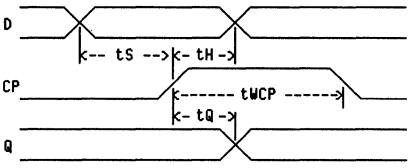
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	4.8	4.8	5.0	5.3	5.9	5.4	7.2	6.0

Note: For other operating conditions, use derating curves given in the performance section.

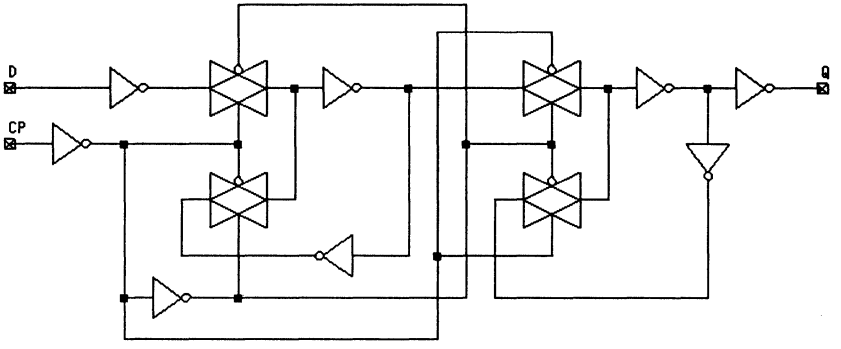
DFP05

D FLIP-FLOP W/BUFFERED OUTPUT

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



JKN02

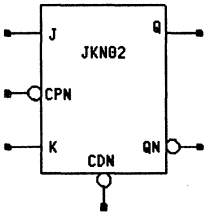
JK FLIP-FLOP W/CLEAR

DESCRIPTION

JKN02 is a positive-edge-triggered J-K flip-flop with an active-LOW CLEAR, CDN. The clock input , CP, and the outputs, Q and QN, are buffered.

Cells: 7 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	
CDN	CPN	J	K	Q	QN
L	X	X	X	L	H
H	⎍	L	L	Q	QN
H	⎍	L	H	L	H
H	⎍	H	L	H	L
H	⎍	H	H	QN	Q
H	L	X	X	Q	QN
H	H	X	X	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
J	Input	1.0	J Input
K	Input	1.0	K Input
CPN	Input	1.0	Clock Input
CDN	Input	2.0	CLEAR Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

JKN02

JK FLIP-FLOP W/CLEAR

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CPN-Q	4.0 + 0.7 + 0.31 * UL	4.3 + 0.5 + 0.20 * UL
tQN, CPN-QN	6.1 + 0.6 + 0.26 * UL	6.2 + 0.4 + 0.15 * UL
tCQ, CDN-Q		3.6 + 0.5 + 0.21 * UL
tCQN, CDN-QN	5.6 + 0.6 + 0.26 * UL	

fMAX, Cld = 1.0 pF	85	MHz
tWCPN, CPN	3.7	ns
tS, J,K-CPN	5.2	ns
tH, CPN-J,K	0	ns
tREL, CDN-CPN	0	ns
tWCDN, CDN	3.7	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

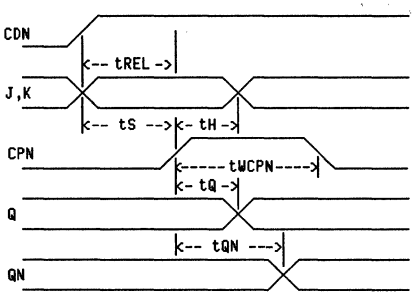
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	5.0	5.0	5.3	5.2	6.3	5.8	7.8	6.8
tQN	7.0	6.8	7.2	6.9	8.0	7.4	9.3	8.1
tCQ		4.3		4.5		5.2		6.2
tCQN	6.5		6.7		7.5		8.8	

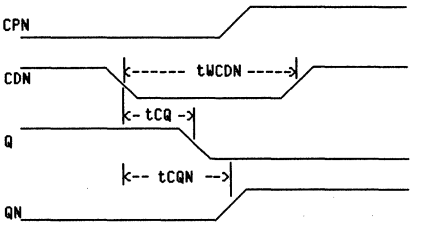
Note: For other operating conditions, use derating curves given in the performance section.

JKN02

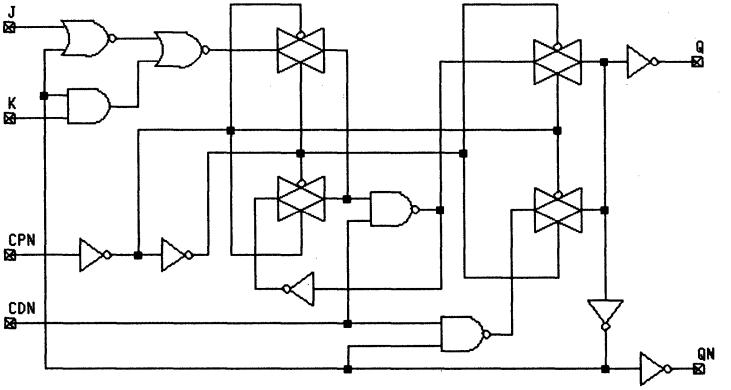
JK FLIP-FLOP W/CLEAR

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



JKN76

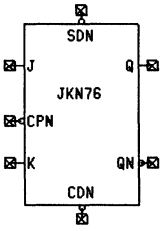
JK FLIP-FLOP

DESCRIPTION

The JKN76 is a Master/Slave Flip-Flop. Data is transferred to the output on the HIGH-to-LOW clock transition. The SET and CLEAR functions, SDN and CDN, respectively, are independent of the clock input and are accomplished by a LOW logic level on the corresponding input pin. QN drives 2 internal nodes.

Cells: 8 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS					OUTPUTS	
SDN	CDN	CPN	J	K	Q	QN
H	H	⌐	L	L	Q	QN
H	H	⌐	L	H	L	H
H	H	⌐	H	L	H	L
H	H	⌐	H	H	QN	Q
H	H	H	X	X	Q	QN
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*

*UNSTABLE STATE

PIN DESCRIPTION

Name	Type	U.L.	Description
J	Input	1.0	Data Input
K	Input	1.0	Data Input
CPN	Input	1.0	Clock Pulse (negative-edge)
SDN	Input	2.0	Asynchronous SET (Active-LOW)
CDN	Input	2.0	Asynchronous CLEAR (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

JKN76

JK FLIP-FLOP

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CPN-Q	3.9 + 0.5 + 0.28 * UL	3.3 + 0.3 + 0.15 * UL
tQN, CPN-QN	6.1 + 0.4 + 0.18 * UL	6.1 + 0.3 + 0.12 * UL
tCQ, CDN-Q	3.8 + 0.2 + 0.13 * UL	
tCQN, CDN-QN		6.6 + 0.6 + 0.26 * UL
tSQ, SDN-Q	7.6 + 0.5 + 0.27 * UL	
tSQN, SDN-QN		2.7 + 0.3 + 0.13 * UL

fMAX, Cld = 1.0 pF	90	MHz
tWCPN, CPN	6.8	ns
tS, J/K-CPN	5.0	ns
tH, CPN-J/K	1.7	ns
tREL, CDN/SDN-CPN	0	ns
tWSDN, SDN	7.2	ns
tWCDN, CDN	5.1	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

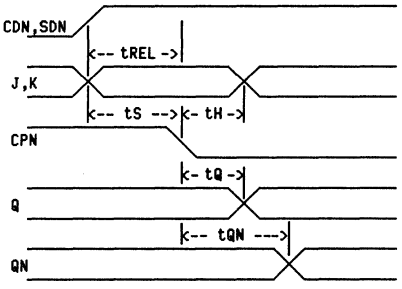
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	4.7	3.8	5.0	3.9	5.8	4.4	7.2	5.1
tQN	6.7	6.5	6.9	6.6	7.4	7.0	8.3	7.6
tCQ	4.1		4.3		4.7		5.3	
tCQN		7.5		7.7		8.5		9.8
tSQ	8.4		8.6		9.5		10.8	
tSQN		3.1		3.3		3.7		4.3

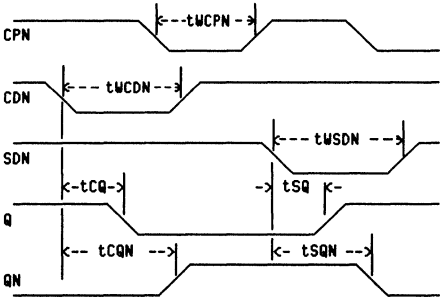
Note: For other operating conditions, use derating curves given in the performance section.

JKN76

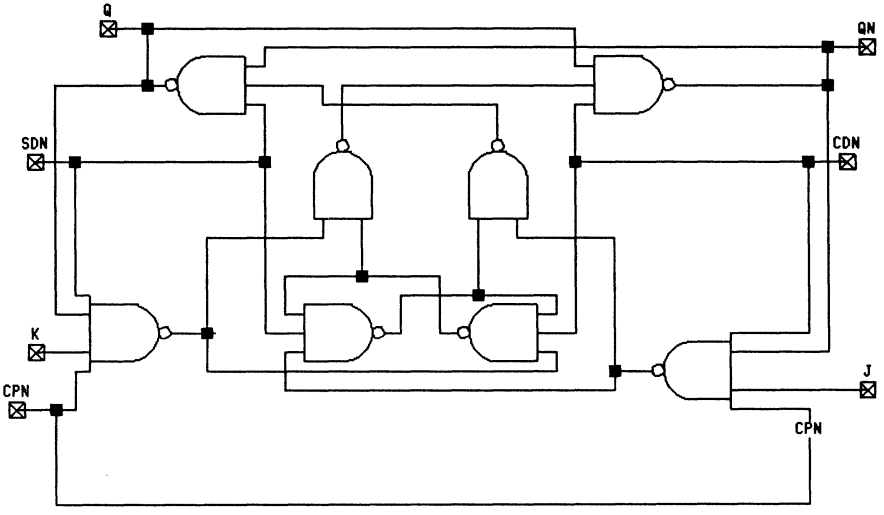
JK FLIP-FLOP

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



TF02

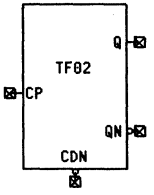
TOGGLE FLIP-FLOP WITH CLEAR

DESCRIPTION

The TF02 is a positive edge-triggered Toggle Flip-Flop, with an asychronous, active-LOW CLEAR Input.

Cells: 5 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
CDN	CP	Q	QN
L	X	L	H
H	⌐	QN	Q
H	L	Q	QN
H	H	Q	QN

PIN DESCRIPTION

Name	Type	U.L.	Description
CP	Input	1.0	Clock Input
CDN	Input	2.0	CLEAR Input (Active-LOW)
Q	Output	-	Data Output
QN	Output	-	Complimentary Data Output

TF02

TOGGLE FLIP-FLOP WITH CLEAR

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tQ, CP-Q	5.0 + 0.7 + 0.31 * UL	5.3 + 0.4 + 0.18 * UL
tQN, CP-QN	6.3 + 0.7 + 0.28 * UL	6.2 + 0.3 + 0.13 * UL
tCQ, CDN-Q		2.7 + 0.4 + 0.17 * UL
tCQN, CDN-QN	3.6 + 0.7 + 0.28 * UL	

fMAX, Cld = 1.0 pF	101	MHz
tWCP, CP	2.4	ns
tREL, CDN-CP	1.0	ns
tWCDN, CDN	2.7	ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

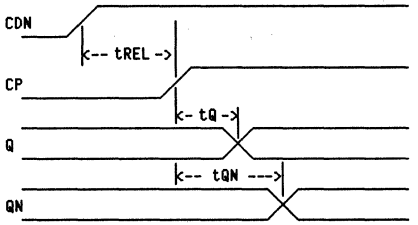
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tQ	6.0	5.9	6.3	6.1	7.3	6.6	8.8	7.5
tQN	7.3	6.6	7.6	6.8	8.4	7.2	9.8	7.8
tCQ		3.3		3.4		4.0		4.8
tCQN	4.6		4.9		5.7		7.1	

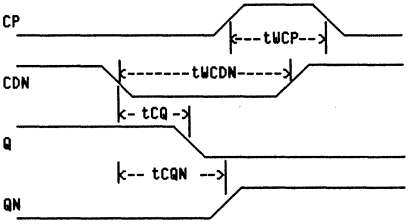
Note: For other operating conditions, use derating curves given in the performance section.

TF02

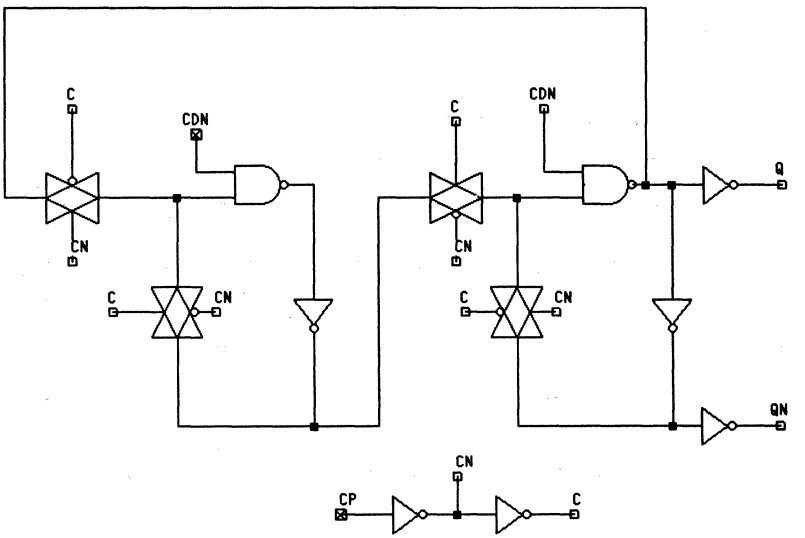
TOGGLE FLIP-FLOP WITH CLEAR

AC CHARACTERISTICS (cont'd)





LOGIC DIAGRAM



MX02

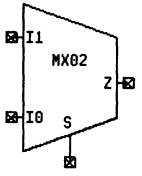
2 to 1 MULTIPLEXER

DESCRIPTION

The MX02 is a two-input multiplexer. The state of the SELECT signal, S, determines which data, I0 or I1, will be present at the output.

Cells: 3 **Cell Type:** Internal

SYMBOL



FUNCTION

INPUT			OUTPUT
S	I1	I0	Z
L	X	L	L
L	X	H	H
H	H	X	H
H	L	X	L

PIN DESCRIPTION

Name	Type	U.L.	Description
I0	Input	1.0	Data Input
I1	Input	1.0	Data Input
S	Input	2.0	SELECT Input
Z	Output	-	Data Output

MX02

2 to 1 MULTIPLEXER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tIZ, I1-Z	2.1 + 0.4 + 0.26 * UL	3.1 + 0.2 + 0.14 * UL
tSZ, S-Z	2.6 + 0.4 + 0.26 * UL	2.4 + 0.2 + 0.14 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

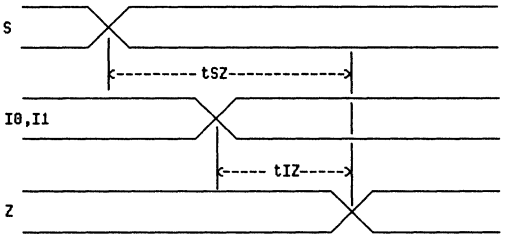
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tIZ	2.8	3.4	3.1	3.6	4.1	4.0	5.1	4.7
tSZ	3.3	2.7	3.5	2.9	4.6	3.3	5.6	4.0

Note: For other operating conditions, use derating curves given in the performance section.

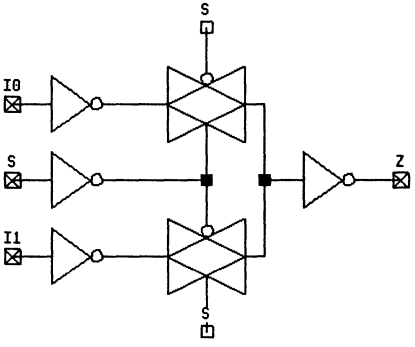
MX02

2 to 1 MULTIPLEXER

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



MX04

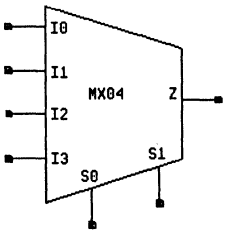
4:1 MULTIPLEXER

DESCRIPTION

The MX04 decodes the two select inputs to pass one of the four inputs to the output.

Cells: 5 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS						OUTPUTS
S0	S1	I0	I1	I2	I3	Z
L	L	L	X	X	X	L
L	L	H	X	X	X	H
H	L	X	L	X	X	L
H	L	X	H	X	X	H
L	H	X	X	L	X	L
L	H	X	X	H	X	H
H	H	X	X	X	L	L
H	H	X	X	X	H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
I0	Input	1.0	Data Input
I1	Input	1.0	Data Input
I2	Input	1.0	Data Input
I3	Input	1.0	Data Input
S0	Input	1.0	SELECT Input
S1	Input	2.0	SELECT Input
Z	Output	-	Data Output

MX04

4:1 MULTIPLEXER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tIZ, I-Z	2.9 + 0.7 + 0.31 * UL	4.6 + 0.6 + 0.26 * UL
tSOZ, S0-Z	4.6 + 0.7 + 0.30 * UL	5.3 + 0.6 + 0.25 * UL
tS1Z, S1-Z	1.5 + 0.7 + 0.29 * UL	2.3 + 0.5 + 0.21 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

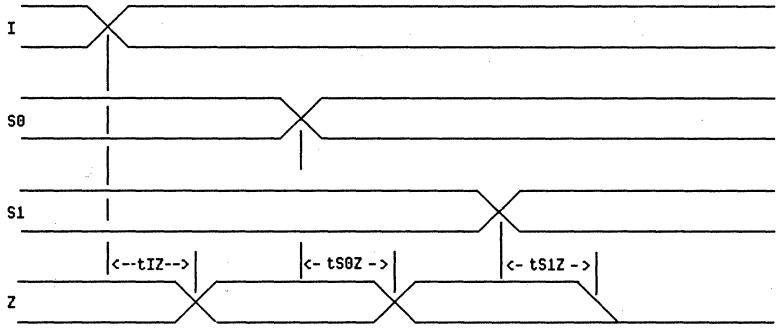
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tIZ	3.9	5.5	4.2	5.7	5.2	6.5	6.7	7.8
tSOZ	5.6	6.2	5.9	6.4	6.8	7.2	8.3	8.4
tS1Z	2.5	3.0	2.8	3.2	3.7	3.9	5.1	4.9

Note: For other operating conditions, use derating curves given in the performance section.

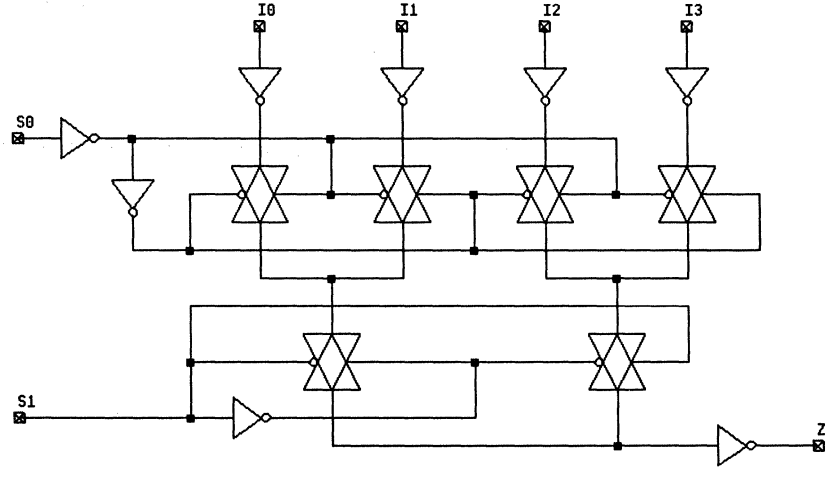
MX04

4:1 MULTIPLEXER

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



MXE04

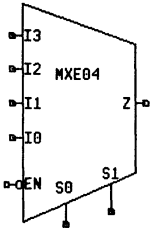
4:1 MULTIPLEXER (1/2 74153)

DESCRIPTION

The MXE04 passes one of four input signals, I0 - I3, to the output Z, depending upon the state of the SELECT inputs, S0 and S!. EN is an active-LOW ENABLE.

Cells: 6 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS							OUTPUTS
EN	S0	S1	I0	I1	I2	I3	Z
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
L	H	L	X	L	X	X	L
L	H	L	X	H	X	X	H
L	L	H	X	X	L	X	L
L	L	H	X	X	H	X	H
L	H	H	X	X	X	L	L
L	H	H	X	X	X	H	H
H	X	X	X	X	X	X	L

PIN DESCRIPTION

Name	Type	U.L.	Description
I0	Input	7.0	Data Input
I1	Input	7.0	Data Input
I2	Input	7.0	Data Input
I3	Input	7.0	Data Input
S0	Input	3.0	SELECT Input
S1	Input	2.0	SELECT Input
EN	Input	1.0	ENABLE Input (Active-LOW)
Z	Output	-	Data Output

MXE04

4:1 MULTIPLEXER (1/2 74153)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tI3Z, I3-Z	2.5 + 0.3 + 0.20 * UL	2.8 + 0.1 + 0.08 * UL
tS0Z, S0-Z	3.3 + 0.3 + 0.20 * UL	3.8 + 0.1 + 0.09 * UL
tS1Z, S1-Z	3.4 + 0.3 + 0.20 * UL	3.9 + 0.1 + 0.06 * UL
tENZ, EN-Z	1.9 + 0.3 + 0.20 * UL	1.5 + 0.2 + 0.14 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

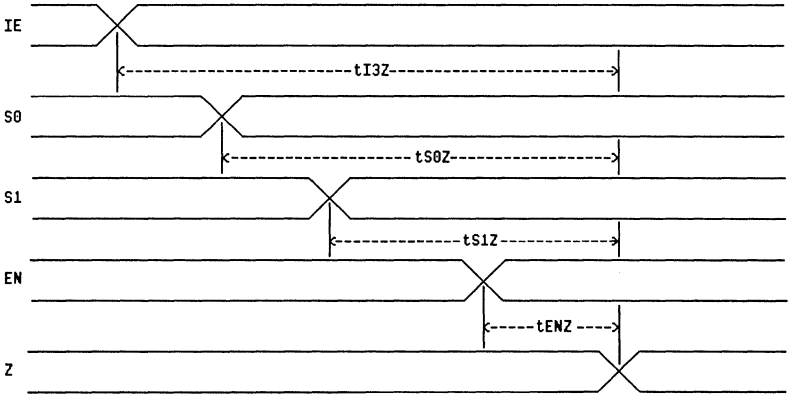
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tI3Z	3.0	3.0	3.2	3.1	3.8	3.3	4.8	3.7
tS0Z	3.8	4.0	4.0	4.1	4.6	4.4	5.6	4.8
tS1Z	3.9	4.1	4.1	4.1	4.7	4.3	5.7	4.6
tENZ	2.4	1.8	2.6	2.0	3.2	2.4	4.2	3.1

Note: For other operating conditions, use derating curves given in the performance section.

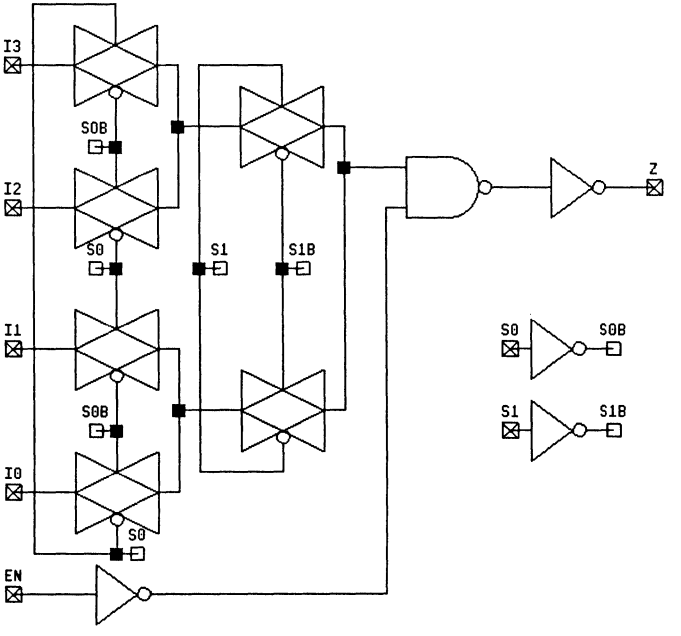
MXE04

4:1 MULTIPLEXER (1/2 74153)

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



MXE041

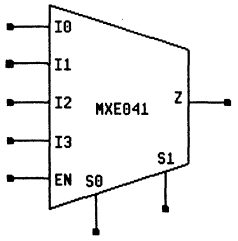
4:1 MULTIPLEXER W/ENABLE

DESCRIPTION

The MXE041 is a redesign of the MXE04. The MXE041 has a fan-in of one on the data inputs.

Cells: 5 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS							OUTPUTS
EN	S0	S1	I0	I1	I2	I3	Z
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
L	H	L	X	L	X	X	L
L	H	L	X	H	X	X	H
L	L	H	X	X	L	X	L
L	L	H	X	X	H	X	H
L	H	H	X	X	X	L	L
L	H	H	X	X	X	H	H
H	X	X	X	X	X	X	L

PIN DESCRIPTION

Name	Type	U.L.	Description
I0	Input	1.0	Data Input
I1	Input	1.0	Data Input
I2	Input	1.0	Data Input
I3	Input	1.0	Data Input
S0	Input	3.0	SELECT Input
S1	Input	2.0	SELECT Input
EN	Input	1.0	ENABLE Input (Active-LOW)
Z	Output	-	Data Output

MXE041

4:1 MULTIPLEXER W/ENABLE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tIZ, I-Z	4.2 + 1.0 + 0.50 * UL	5.3 + 0.5 + 0.23 * UL
tOE, EN-Z	0.7 + 1.0 + 0.49 * UL	0.5 + 0.3 + 0.12 * UL
tSOZ, S0-Z	5.6 + 1.0 + 0.50 * UL	5.4 + 0.5 + 0.23 * UL
tS1Z, S1-Z	3.3 + 1.0 + 0.48 * UL	2.5 + 0.4 + 0.22 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

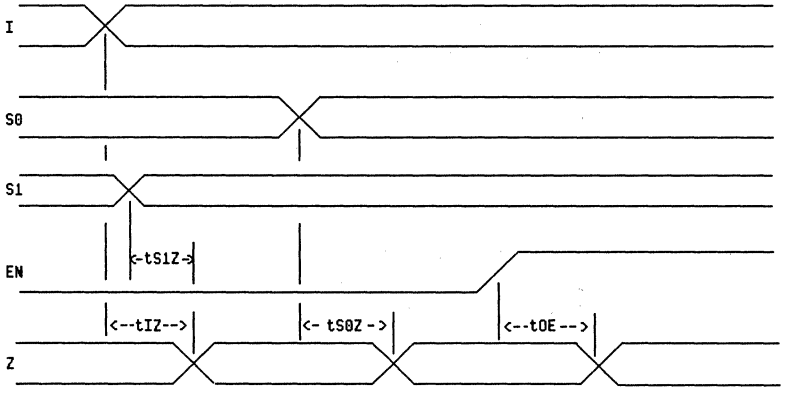
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tIZ	5.7	6.0	6.2	6.3	7.7	7.0	10.2	8.1
tOE	2.2	0.9	2.7	1.0	4.2	1.4	6.6	2.0
tSOZ	7.1	6.1	7.6	6.4	9.1	7.1	11.6	8.2
tS1Z	4.8	3.1	5.3	3.3	6.7	4.0	9.1	5.1

Note: For other operating conditions, use derating curves given in the performance section.

MXE041

4:1 MULTIPLEXER W/ENABLE

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM

DC24

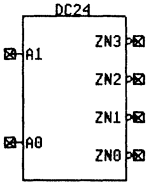
1 OF 4 DECODER

DESCRIPTION

The DC24 accepts a 2-bit binary-coded address and converts this into four active-LOW, mutually exclusive outputs. There are no ENABLE inputs.

Cells: 4 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS			
A0	A1	ZN0	ZN1	ZN2	ZN3
L	L	L	H	H	H
H	L	H	L	H	H
L	H	H	H	L	H
H	H	H	H	H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A0	Input	1.0	Address Input, LSB
A1	Input	1.0	Address Input, MSB
ZN0	Output	-	Decoded Output, 0
ZN1	Output	-	Decoded Output, 1
ZN2	Output	-	Decoded Output, 2
ZN3	Output	-	Decoded Output, 3

DC24

1 OF 4 DECODER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDA0, A0-ZN1	3.6 + 0.5 + 0.23 * UL	2.9 + 0.4 + 0.18 * UL
tDA1, A1-ZN2	3.8 + 0.4 + 0.21 * UL	3.0 + 0.4 + 0.18 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

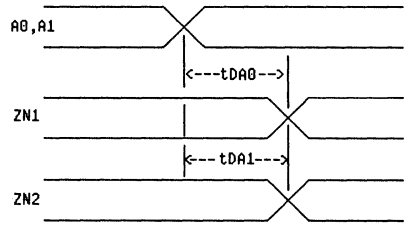
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDA0	4.3	3.5	4.6	3.7	5.3	4.2	6.4	5.1
tDA1	4.4	3.6	4.6	3.8	5.3	4.3	6.3	5.2

Note: For other operating conditions, use derating curves given in the performance section.

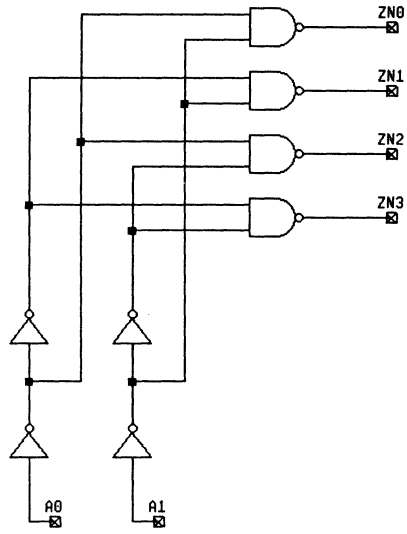
DC24

1 OF 4 DECODER

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



DC139

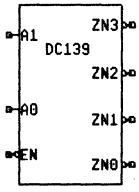
1 of 4 DECODER, W/ENABLE

DESCRIPTION

The DC139 accepts a binary-coded address (A0, A1), and provides four mutually exclusive active-LOW outputs. It is functionally equivalent to the 74139.

Cells: 7 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS			
A0	A1	EN	ZN0	ZN1	ZN2	ZN3
L	L	L	L	H	H	H
H	L	L	H	L	H	H
L	H	L	H	H	L	H
H	H	L	H	H	H	L
X	X	H	H	H	H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
A0	Input	1.0	Address Input, LSB
A1	Input	1.0	Address Input, MSB
EN	Input	1.0	ENABLE Input (Active-LOW)
ZN0	Output	-	LSB Output
ZN1	Output	-	Output
ZN2	Output	-	Output
ZN3	Output	-	MSB Output

DC139

1 of 4 DECODER, W/ENABLE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tDAO, A0-ZN3	2.7 + 0.9 + 0.29 * UL	2.3 + 1.0 + 0.32 * UL
tEN, EN-ZN3	1.5 + 0.7 + 0.20 * UL	2.2 + 0.7 + 0.23 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

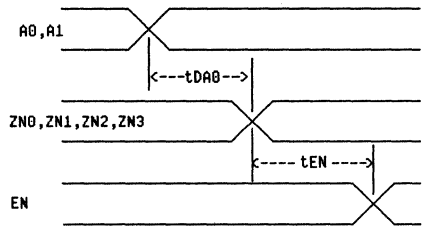
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tDAO	3.9	3.6	4.2	3.9	5.1	4.9	6.5	6.5
tEN	2.4	3.1	2.6	3.4	3.2	4.1	4.2	5.2

Note: For other operating conditions, use derating curves given in the performance section.

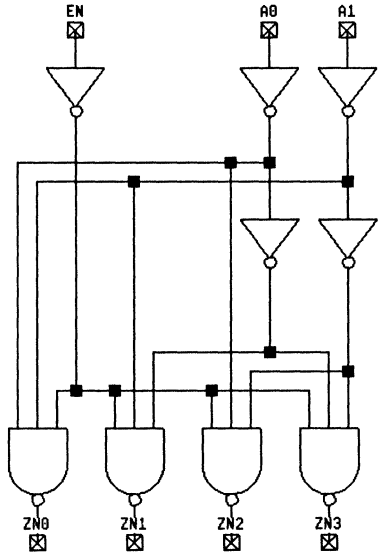
DC139

1 of 4 DECODER, W/ENABLE

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



ADD01

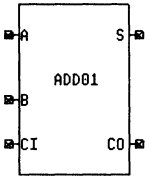
1-BIT FULL ADDER

DESCRIPTION

The ADD01 is a one-bit full adder. The A and B Inputs and the CARRY Input are combined to provide the SUM and CARRY out.

Cells: 6 **Cell Type:** Internal

SYMBOL



FUNCTION

INPUTS			OUTPUTS	
A	B	CI	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
A	Input	4.0	Operand
B	Input	4.0	Operand
CI	Input	4.0	CARRY Input
CO	Output	-	CARRY Output
S	Output	-	SUM Output

ADD01

1-BIT FULL ADDER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tAS, A->S	6.0 + 1.0 + 0.53 * UL	6.5 + 0.4 + 0.25 * UL
tBS, B->S	4.8 + 1.0 + 0.54 * UL	6.4 + 0.5 + 0.26 * UL
tCS, CI->S	1.6 + 1.0 + 0.53 * UL	2.7 + 0.3 + 0.17 * UL
tACO, A->CO	2.5 + 0.8 + 0.35 * UL	5.6 + 0.6 + 0.26 * UL
tBCO, B->CO	2.6 + 0.8 + 0.35 * UL	6.8 + 0.8 + 0.31 * UL
tCCO, CI->CO	2.3 + 0.8 + 0.35 * UL	6.3 + 0.7 + 0.30 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

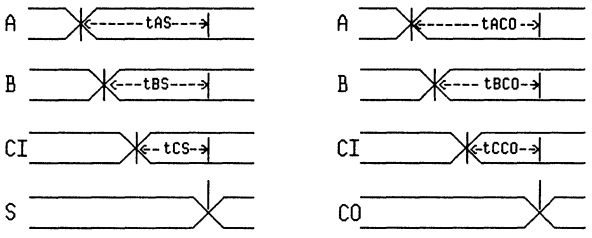
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tAS	7.5	7.2	8.1	7.4	9.7	8.2	12.3	9.4
tBS	6.3	7.2	6.9	7.4	8.5	8.2	11.2	9.5
tCS	3.1	3.2	3.7	3.3	5.3	3.9	7.9	4.7
tACO	3.7	6.5	4.0	6.7	5.1	7.5	6.8	8.8
tBCO	3.8	7.9	4.1	8.2	5.2	9.2	6.9	10.7
tCCO	3.5	7.3	3.8	7.6	4.9	8.5	6.6	10.0

Note: For other operating conditions, use derating curves given in the performance section.

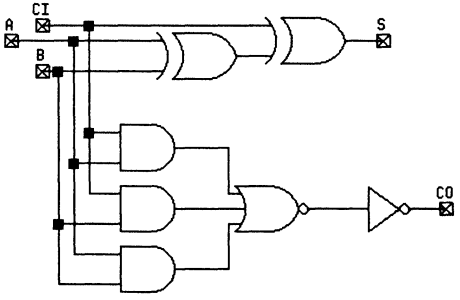
ADD01

1-BIT FULL ADDER

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



IOT01F

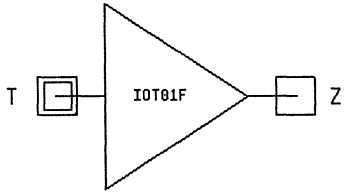
TTL INPUT BUFFER W/O PULL-UP

DESCRIPTION

The IOT01F is an input buffer designed to accept an external TTL signal. The input pad will float when left unconnected. This macro is designed for use only with the VGC0500.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
T	Z
L	L
H	H
open	unknown

PIN DESCRIPTION

Name	Type	U.L.	Description
T	Input	-	Data Input
Z	Output	-	Data Output

IOT01F

TTL INPUT BUFFER
W/O PULL-UP

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tTZ, T-Z	3.2 + 0.2 + 0.18 * UL	5.1 + 0.3 + 0.21 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

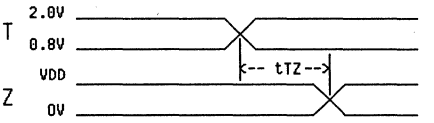
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tTZ	3.6	5.6	3.8	5.8	4.3	6.5	5.2	7.5

Note: For other operating conditions, use derating curves given in the performance section.

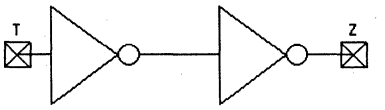
IOT01F

TTL INPUT BUFFER W/O PULL-UP

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



IOT01

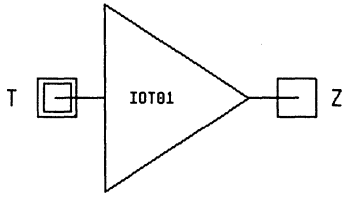
TTL INPUT BUFFER

DESCRIPTION

The IOT01 is a non-inverting TTL input buffer, for interface to TTL signal levels. This macro is designed for use with the VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
T	Z
H	H
L	L

PIN DESCRIPTION

Name	Type	U.L.	Description
T	Input	-	Data Input
Z	Output	-	Data Output

IOT01

TTL INPUT BUFFER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tTZ, T-Z	2.7 + 0.4 + 0.12 * UL	3.0 + 0.6 + 0.18 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

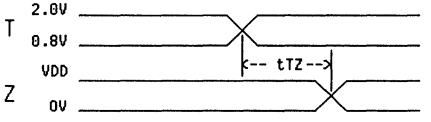
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tTZ	3.2	3.8	3.3	4.0	3.7	4.5	4.3	5.4

Note: For other operating conditions, use derating curves given in the performance section.

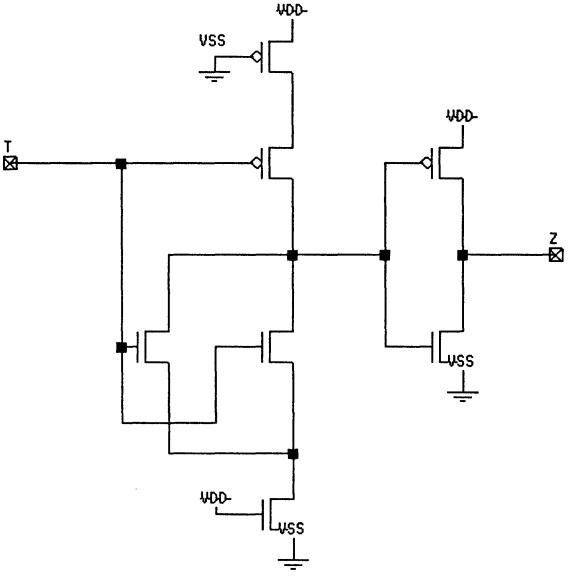
IOT01

TTL INPUT BUFFER

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



IOT011F

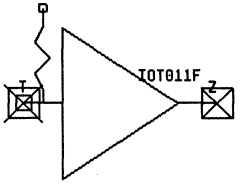
TTL INPUT BUFFER W/PULL-UP (VGC0500)

DESCRIPTION

The IOT011f is a TTL-compatible non-inverting input buffer. An input pull-up resistor ensures that the output Z remains HIGH when the input pad is unconnected. This macro is designed for use only on the VGC0500.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
T	Z
L	L
H	H
open	H

PIN DESCRIPTION

Name	Type	U.L.	Description
T	Input	-	Data Input
Z	Output	-	Data Output

IOT011F

TTL INPUT BUFFER W/PULL-UP (VGC0500)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tTZ, T-Z	3.2 + 0.2 + 0.18 * UL	5.1 + 0.3 + 0.21 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

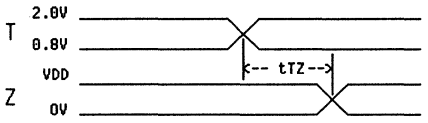
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tTZ	3.6	5.6	3.8	5.8	4.3	6.5	5.2	7.5

Note: For other operating conditions, use derating curves given in the performance section.

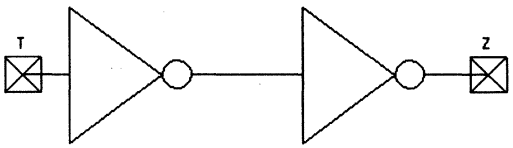
IOT011F

TTL INPUT BUFFER W/PULL-UP (VGC0500)

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



IOT011

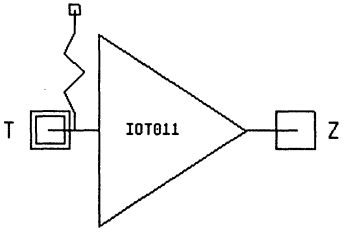
TTL INPUT BUFFER W/PULL-UP

DESCRIPTION

The IOT011 is a non-inverting TTL input buffer, for interface to TTL signal levels. A pull-up resistor is provided on the input. This macro is designed for use with the VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
T	Z
H	H
L	L
open	H

PIN DESCRIPTION

Name	Type	U.L.	Description
T	Input	-	Data Input
Z	Output	-	Data Output

IOT011

TTL INPUT BUFFER W/PULL-UP

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tTZ, T-Z	2.7 + 0.4 + 0.12 * UL	3.0 + 0.6 + 0.18 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

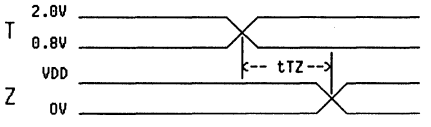
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tTZ	3.2	3.8	3.3	4.0	3.7	4.5	4.3	5.4

Note: For other operating conditions, use derating curves given in the performance section.

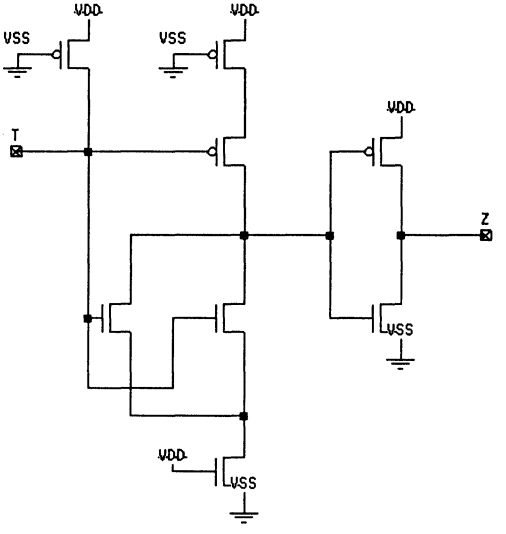
IOT011

TTL INPUT BUFFER W/PULL-UP

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



IOC01F

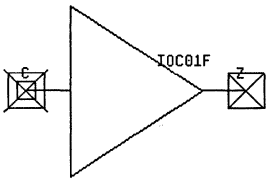
CMOS INPUT BUFFER
W/O PULL-UP (VGC0500)

DESCRIPTION

The IOC01F is an input buffer designed to accept an external CMOS signal. The input pad will float when left unconnected (no pull-up). This macro is designed for use only with the VGC0500.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
C	Z
L	L
H	H
open	unknown

PIN DESCRIPTION

Name	Type	U.L.	Description
C	Input	-	Data Input
Z	Output	-	Data Output

IOC01F

CMOS INPUT BUFFER W/O PULL-UP (VGC0500)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tCZ, C-Z	2.7 + 0.2 + 0.14 * UL	3.1 + 0.2 + 0.14 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

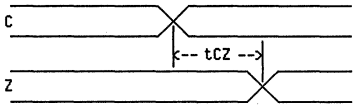
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tCZ	3.0	3.4	3.2	3.6	3.6	4.0	4.3	4.7

Note: For other operating conditions, use derating curves given in the performance section.

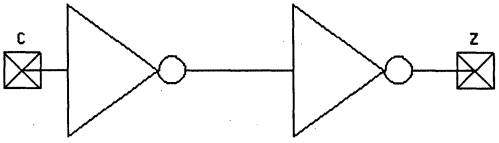
IOC01F

CMOS INPUT BUFFER W/O PULL-UP (VGC0500)

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



IOC01

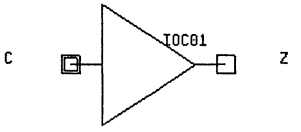
CMOS INPUT BUFFER

DESCRIPTION

The IOC01 is a non-inverting CMOS input buffer, for interface to CMOS signal levels. This macro is designed for use with the VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUTS	OUTPUTS
C	Z
L	L
H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
C	Input	-	Data Input
Z	Output	-	Data Output

IOC01

CMOS INPUT BUFFER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tCZ, C-Z	1.5 + 0.4 + 0.13 * UL	2.9 + 0.3 + 0.09 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

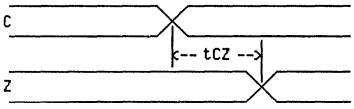
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tCZ	2.0	3.3	2.2	3.4	2.6	3.7	3.2	4.1

Note: For other operating conditions, use derating curves given in the performance section.

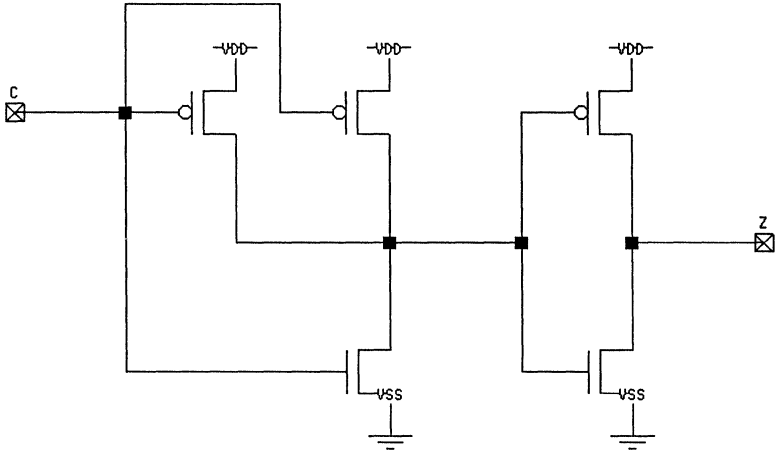
IOC01

CMOS INPUT BUFFER

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



IOC011F

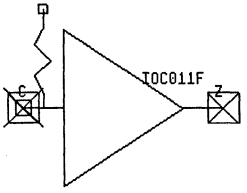
CMOS INPUT BUFFER W/PULL-UP (VGC0500)

DESCRIPTION

The IOC011F allows an external CMOS signal to connect with an internal cell. A pull-up resistor ensures that the output Z remains HIGH when the input pad is unconnected. This macro is for use only with the VGC0900.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
C	Z
L	L
H	H
open	H

PIN DESCRIPTION

Name	Type	U.L.	Description
C	Input	-	Data Input
Z	Output	-	Data Output

IOC011F

CMOS INPUT BUFFER W/PULL-UP (VGC0500)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tCZ, C-Z	2.7 + 0.2 + 0.14 * UL	3.1 + 0.2 + 0.14 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

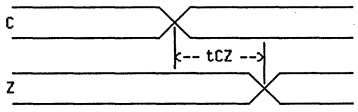
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tCZ	3.0	3.4	3.2	3.6	3.6	4.0	4.3	4.7

Note: For other operating conditions, use derating curves given in the performance section.

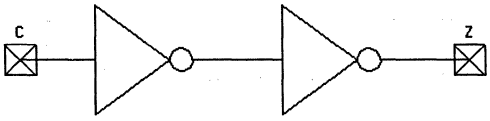
IOC011F

CMOS INPUT BUFFER W/PULL-UP (VGC0500)

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



IOC011

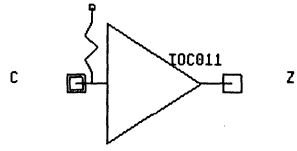
CMOS INPUT BUFFER W/PULL-UP

DESCRIPTION

The IOC011 is a non-inverting CMOS input buffer, used to interface with CMOS signals. A pull-up resistor is provided at the input. This macro is designed for use with the VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUTS	OUTPUTS
C	Z
L	L
H	H
OPEN	H

PIN DESCRIPTION

Name	Type	U.L.	Description
C	Input	-	Data Input
Z	Output	-	Data Output

IOC011

CMOS INPUT BUFFER W/PULL-UP

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tCZ, C-Z	1.5 + 0.4 + 0.13 * UL	2.9 + 0.3 + 0.09 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

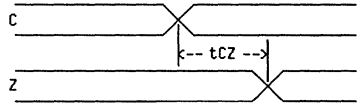
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tCZ	2.0	3.3	2.2	3.4	2.6	3.7	3.2	4.1

Note: For other operating conditions, use derating curves given in the performance section.

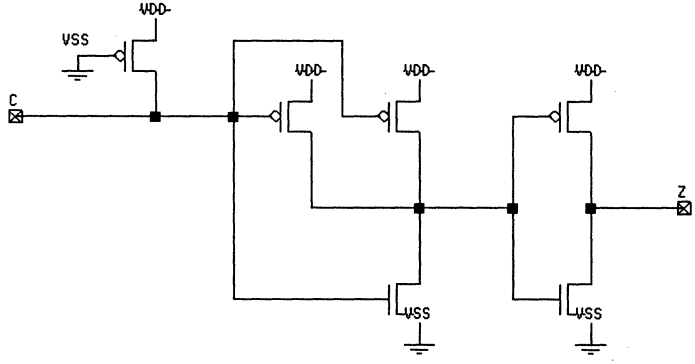
IOC011

CMOS INPUT BUFFER W/PULL-UP

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



IOT04

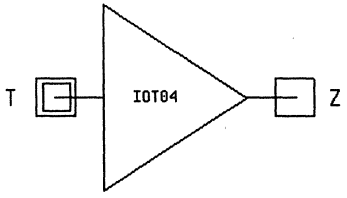
TTL INPUT BUFFER

DESCRIPTION

The IOT04 is a non-inverting TTL input buffer, for interface to TTL signal levels. This macro has an input stage ratio of 4:1, for improved DC switching levels. For use with the VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
T	Z
H	H
L	L

PIN DESCRIPTION

Name	Type	U.L.	Description
T	Input	-	Data Input
Z	Output	-	Data Output

IOT04

TTL INPUT BUFFER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tTZ, T-Z	2.7 + 0.4 + 0.12 * UL	6.1 + 0.6 + 0.18 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

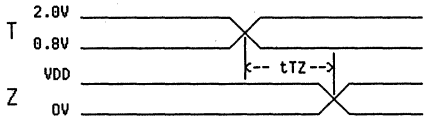
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tTZ	3.2	6.9	3.3	7.1	3.7	7.6	4.3	8.5

Note: For other operating conditions, use derating curves given in the performance section.

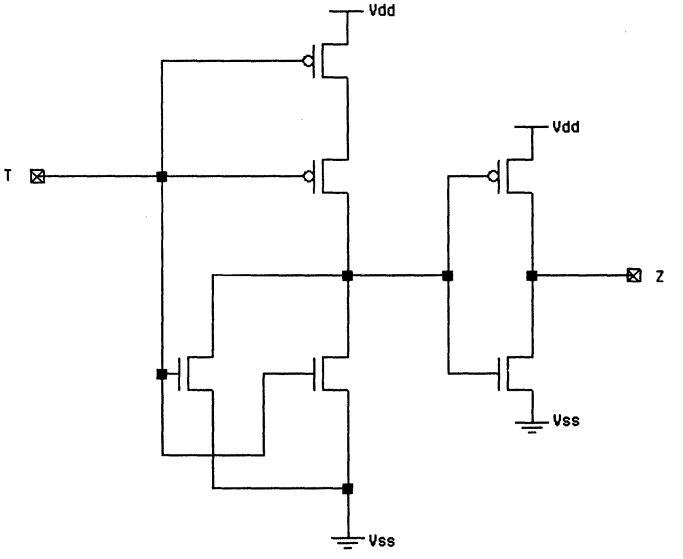
IOT04

TTL INPUT BUFFER

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



IOT041

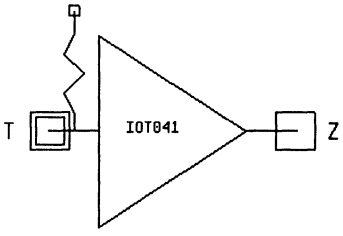
TTL INPUT BUFFER W/PULL-UP

DESCRIPTION

The IOT041 is a non-inverting TTL input buffer, for interface to TTL signal levels. A pull-up resistor is provided on the input. This macro has an input ratio of 4:1, for improved DC switching levels. For use with VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
T	Z
H	H
L	L
open	H

PIN DESCRIPTION

Name	Type	U.L.	Description
T	Input	-	Data Input
Z	Output	-	Data Output

IOT041

TTL INPUT BUFFER W/PULL-UP

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tTZ, T-Z	2.7 + 0.4 + 0.12 * UL	6.1 + 0.6 + 0.18 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

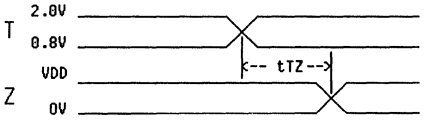
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tTZ	3.2	6.9	3.3	7.1	3.7	7.6	4.3	8.5

Note: For other operating conditions, use derating curves given in the performance section.

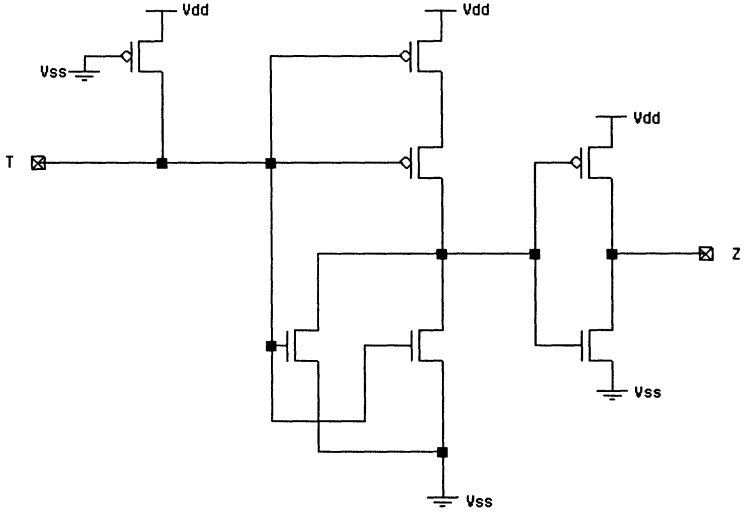
IOT041

TTL INPUT BUFFER W/PULL-UP

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



IOS02

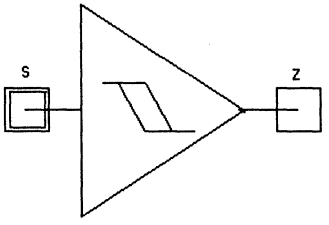
SCHMITT TRIGGER

DESCRIPTION

The IOS02 is a non-inverting Schmitt Trigger input buffer used for bringing slow signals on chip. Signals at input S is buffered and the output is provided at Z, with different voltage thresholds for positive and negative-going inputs. This macro is designed for use with VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
S	Z
L	L
H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
S	Input	-	Data Input
Z	Output	-	Data Output

IOS02

SCHMITT TRIGGER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, S-Z	7.4 + 0.8 + 0.23 * UL	8.9 + 0.9 + 0.27 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	8.4	10.1	8.7	10.3	9.4	11.2	10.5	12.5

DC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

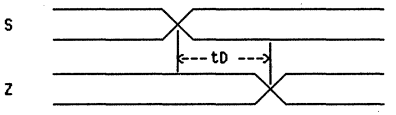
SYMBOL	UNITS	INDUSTRIAL
VT+	Volts	2.49
VT-	Volts	1.27
Hysteresis	Volts	1.22

Note: For other operating conditions, use derating curves given in the performance section.

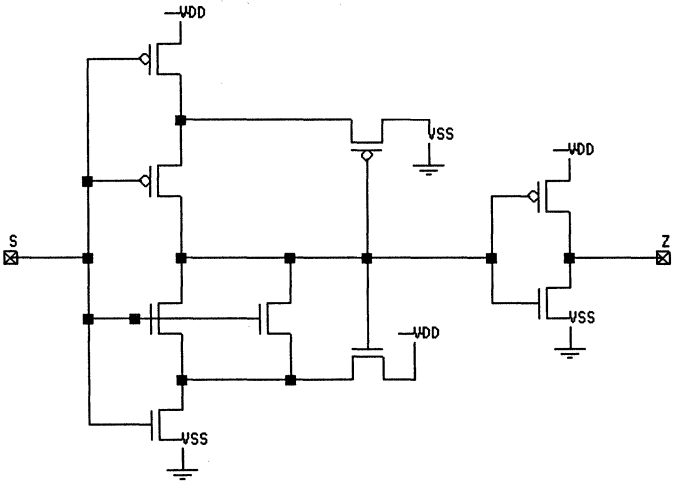
IOS02

SCHMITT TRIGGER

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



IOS02F

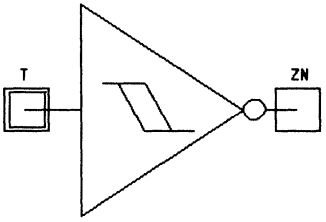
SCHMITT TRIGGER

DESCRIPTION

The IOS02F is an inverting Schmitt Trigger input buffer used for bringing TTL signals on chip. Signals at input T are inverted and output is provided at ZN, with different voltage thresholds for positive and negative-going inputs.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
T	ZN
L	H
H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
T	Input	3.5	Data Input
ZN	Output	-	Data Output

IOS02F

SCHMITT TRIGGER

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, T-ZN	1.4 + 4.3 + 1.96 * UL	0.6 + 0.2 + 0.09 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	7.7	0.9	9.6	1.0	15.5	1.3	25.3	1.7

DC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

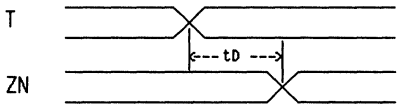
SYMBOL	UNITS	INDUSTRIAL
VT+	Volts	2.05
VT-	Volts	1.14
Hysteresis	Volts	0.91

Note: For other operating conditions, use derating curves given in the performance section.

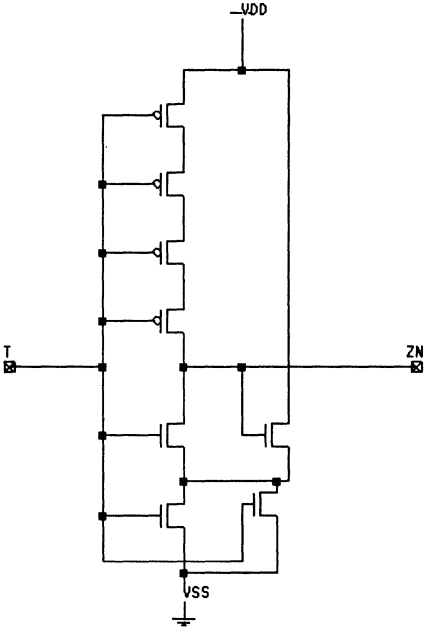
IOS02F

SCHMITT TRIGGER

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



IOS021F

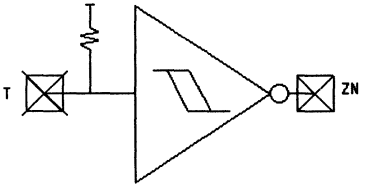
SCHMITT TRIGGER W/PULL-UP

DESCRIPTION

The IOS021F is an inverting Schmitt Trigger input buffer with a pull-up input, used for bringing TTL signals on chip. Signals at input T are inverted and the output is provided at ZN, with different voltage thresholds for positive and negative-going inputs. If the input is left floating, the pull-up resistor will make the output logic LOW. This macro is designed for use with the VGC0500 only.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
T	ZN
L	H
H	L
open	L

PIN DESCRIPTION

Name	Type	U.L.	Description
T	Input	4.0	Data Input
ZN	Output	-	Data Output

IOS021F

SCHMITT TRIGGER W/PULL-UP

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, T-ZN	1.4 + 4.3 + 1.96 * UL	0.6 + 0.2 + 0.09 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	7.7	0.9	9.6	1.0	15.5	1.3	25.3	1.7

DC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

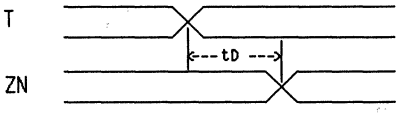
SYMBOL	UNITS	INDUSTRIAL
VT+	Volts	2.05
VT-	Volts	1.14
Hysteresis	Volts	0.91

Note: For other operating conditions, use derating curves given in the performance section.

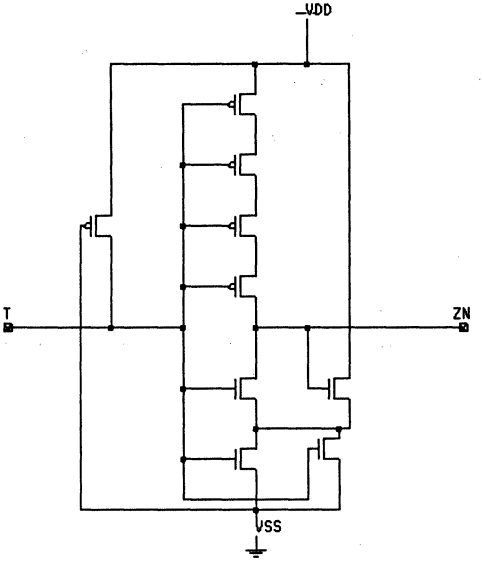
IOS021F

SCHMITT TRIGGER W/PULL-UP

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



OB01F

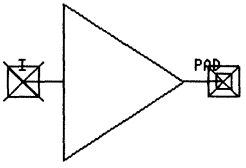
OUTPUT BUFFER
(VGC0500)

DESCRIPTION

The OB01F is a high-drive output buffer, designed for minimum propagation delay. It consists of five paralleled CMOS pairs; two pairs are predrivers and three pairs are for the driver stage. The output drive for this macro is 10mA worst-case Industrial and 8mA worst-case Military. This macro is designed for the use with the VGC0500 only.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
I	PAD
L	L
H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	3.0	Data Input
PAD	Output	-	Data Output

OB01F

OUTPUT BUFFER (VGC0500)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, I-PAD	2.3 + 0.2 + 0.011 * UL	3.5 + 0.2 + 0.010 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

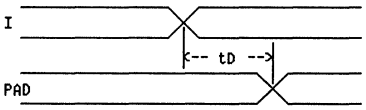
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.51	3.71	2.52	3.72	2.55	3.75	2.61	3.80

Note: For other operating conditions, use derating curves given in the performance section.

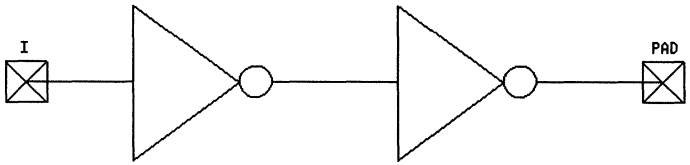
OB01F

OUTPUT BUFFER
(VGC0500)

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



OB03F

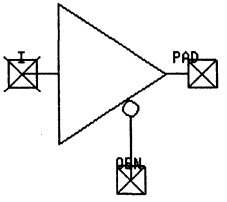
3-STATE OUTPUT BUFFER (VGC0500)

DESCRIPTION

The OB03F is a non-inverting, 3-state output buffer, with Active-LOW output ENABLE. The output drive for this macro is 8mA worst-case Industrial and 6mA worst-case Military. This macro is designed for the use with VGC0500 only.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT		OUTPUT
I	OEN	PAD
L	L	L
H	L	H
X	H	Z

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	3.6	Data Input
OEN	Input	1.9	Output ENABLE (Active-LOW)
PAD	Output	-	Data Output

OB03F

3-STATE OUTPUT BUFFER (VGC0500)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, I-PAD	3.5 + 0.1 + 0.014 * UL	3.8 + 0.2 + 0.012 * UL
tOE,OEN-PAD	3.9 + 0.1 + 0.014 * UL	3.8 + 0.1 + 0.014 * UL
tOD,OEN-PAD	3.10 ns	3.40 ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

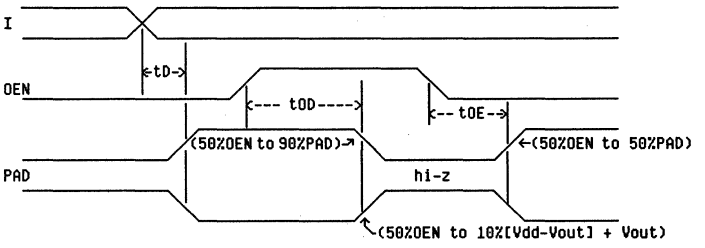
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	3.61	4.01	3.63	4.02	3.67	4.06	3.74	4.12
tOE	4.01	3.91	4.03	3.93	4.07	3.97	4.14	4.04
tOD	3.10	3.40	3.10	3.40	3.10	3.40	3.10	3.40

Note: For other operating conditions, use derating curves given in the performance section.

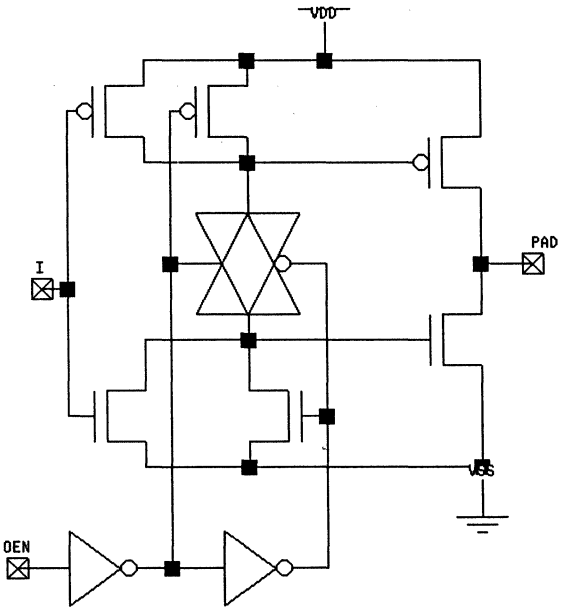
OB03F

3-STATE OUTPUT BUFFER (VGC0500)

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



OB04F

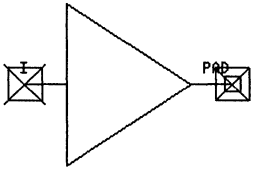
OUTPUT BUFFER
(VGC0500)

DESCRIPTION

The OB04F is a standard output buffer, designed to interface an internal array signal to the external pad. The output drive for this macro is 8mA worst-case Industrial and 6mA worst-case Military. This macro is designed for use with the VGC0500 only.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
I	PAD
L	L
H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	3.6	Data Input
PAD	Output	-	Data Output

OB04F

OUTPUT BUFFER
(VGC0500)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, I-PAD	3.5 + 0.1 + 0.014 * UL	3.8 + 0.2 + 0.012 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

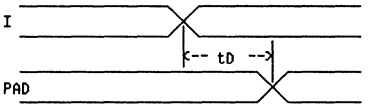
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	3.61	4.01	3.63	4.02	3.67	4.06	3.74	4.12

Note: For other operating conditions, use derating curves given in the performance section.

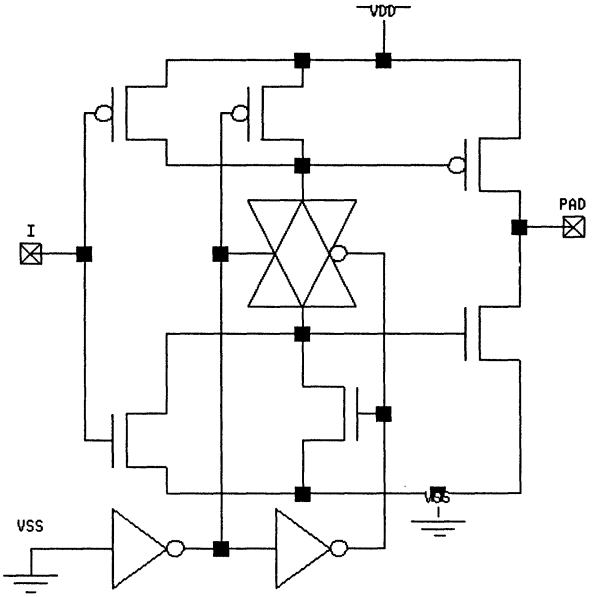
OB04F

OUTPUT BUFFER (VGC0500)

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



OB01

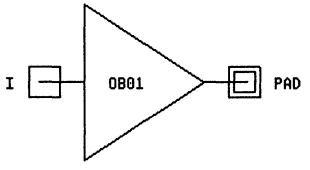
OUTPUT BUFFER, STANDARD

DESCRIPTION

The OB01 is a non-inverting standard output buffer, with built-in testability. The CAD system automatically connects the TDAT, TEST, TESTN, and TOEN signals, via dedicated routing channels, to the TDAT, TEST, TESTN, and TOEN input buffers, located in the lower left-hand corner of the chip. These signals allow test data on the TDAT pin to force all outputs for parametric testing, when TESTN is LOW. The TOEN input provides for the 3-state function, when TESTN is LOW. The output drive for this macro is 8mA worst-case Industrial and 6mA worst-case Military. This macro is designed for use with the VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT					OUTPUT
I	TDAT	TEST	TESTN	TOEN	PAD
H	X	L	H	X	H
L	X	L	H	X	L
X	H	H	L	L	H
X	L	H	L	L	L
X	X	H	L	H	Z

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	4.7	Data Input
TDAT	N/A	-	Test Data Input
TEST	N/A	-	Test ENABLE Input
TESTN	N/A	-	Complimentary Test ENABLE Input
TOEN	N/A	-	Test 3-State Input
PAD	Output	-	Data Output

OB01

OUTPUT BUFFER, STANDARD

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, I-PAD	4.3 + 0.3 + 0.014 * UL	5.1 + 0.2 + 0.012 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

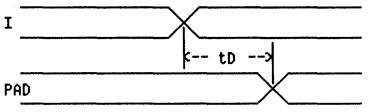
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	4.61	5.31	4.63	5.32	4.67	5.36	4.74	5.42

Note: For other operating conditions, use derating curves given in the performance section.

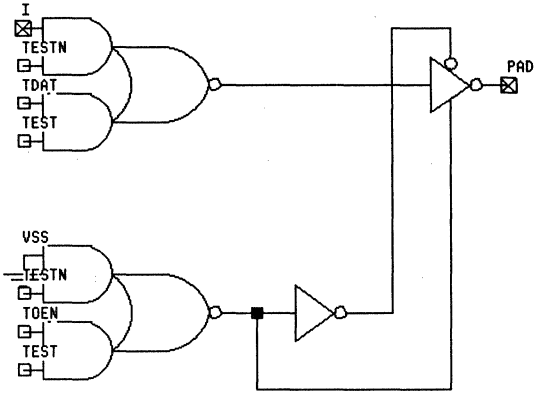
OB01

OUTPUT BUFFER, STANDARD

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



OB03

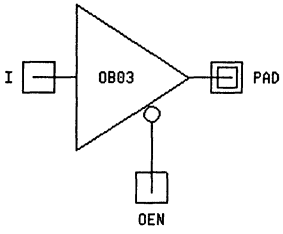
OUTPUT BUFFER, 3-STATE

DESCRIPTION

The OB03 is a non-inverting, 3-state standard output buffer, with active-LOW ENABLE, and built-in testability. An internal multiplexing scheme allows test data to be sent to the output, by manipulation of the test signals, TDAT, TEST, TESTN, and TOEN. The CAD system automatically connects these signals, via dedicated routing channels, to the TDAT, TEST, TESTN, and TOEN input buffers, located in the lower left-hand corner of the chip. The OEN input provides for an external 3-state function, active-LOW. The output drive for this macro is 8mA worst-case Industrial and 6mA worst-case Military. This macro is designed for use with the VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT						OUTPUT
I	OEN	TDAT	TEST	TESTN	TOEN	PAD
H	L	X	L	H	X	H
L	L	X	L	H	X	L
X	H	X	L	H	X	Z
X	X	H	H	L	L	H
X	X	L	H	L	L	L
X	X	X	H	L	H	Z

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	4.7	Data Input
OEN	Input	2.3	ENABLE Input (Active-LOW)
TDAT	N/A	-	Test Data Input
TEST	N/A	-	Test ENABLE Input
TESTN	N/A	-	Complimentary Test ENABLE Input
TOEN	N/A	-	Test 3-State Input
PAD	Output	-	Data Output

OB03

OUTPUT BUFFER, 3-STATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, I-PAD	4.3 + 0.3 + 0.014 * UL	5.1 + 0.2 + 0.012 * UL
tOE, OEN-PAD	5.1 + 0.3 + 0.014 * UL	4.7 + 0.3 + 0.014 * UL
tOD, OEN-PAD	4.3 ns	4.7 ns

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

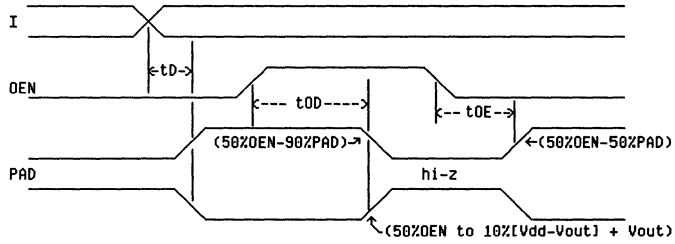
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	4.61	5.31	4.63	5.32	4.67	5.36	4.74	5.42
tOE	5.41	5.01	5.43	5.03	5.47	5.07	5.54	5.14
tOD	4.30	4.70	4.30	4.70	4.30	4.70	4.30	4.70

Note: For other operating conditions, use derating curves given in the performance section.

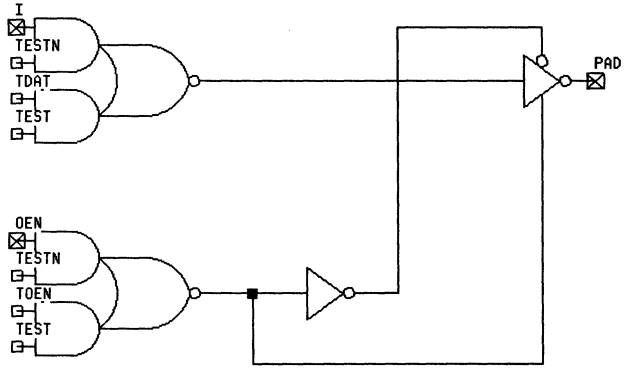
OB03

OUTPUT BUFFER, 3-STATE

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



TRT03

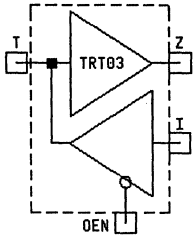
TTL TRANSCEIVER INTERFACE

DESCRIPTION

TRT03 is a non-inverting bidirectional transceiver, with built-in testability. When OEN is HIGH, the output buffer is in the high impedance state. The threshold on the input buffer stage is designed for interface with TTL signal levels. Output drive is 8 mA Industrial worst-case and 6 mA Military worst-case. The CAD system automatically connects the TDAT, TEST, TESTN, and TOEN signals, via dedicated routing channels to the TDAT, TEST, TESTN and TOEN input buffers, located in the lower left-hand corner of the chip. These signals allow test data on the TDAT pin to force all outputs for parametric testing, when TESTN is LOW. The TOEN input provides for the 3-state function, when TESTN is LOW. This macro is designed for use with VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUTS						I/O	OUTPUT
I	OEN	TDAT	TEST	TESTN	TOEN	T	Z
L	L	X	L	H	X	L	L
H	L	X	L	H	X	H	H
X	H	X	L	H	X	Z	T
H	L	H	H	L	L	H	H
L	L	L	H	L	L	L	L
X	L	X	H	L	H	Z	T

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	5.0	Output Buffer Input
OEN	Input	3.0	ENABLE Input (Active-LOW)
TDAT	N/A	-	Test Data Input
TEST	N/A	-	Test ENABLE Input
TESTN	N/A	-	Complimentary Test ENABLE Input
TOEN	N/A	-	Test 3-State Input
T	I/O	-	Input/Output
Z	Ouput	-	Input Buffer Output

TRT03

TTL TRANSCEIVER INTERFACE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tT, I-T	4.3 + 0.3 + 0.014 * UL	5.1 + 0.2 + 0.012 * UL
tOE, OEN-T	5.1 + 0.3 + 0.014 * UL	4.7 + 0.3 + 0.014 * UL
tOD, OEN-T	4.30 ns	4.70 ns
tZ, T-Z	2.7 + 0.4 + 0.12 * UL	3.0 + 0.6 + 0.18 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

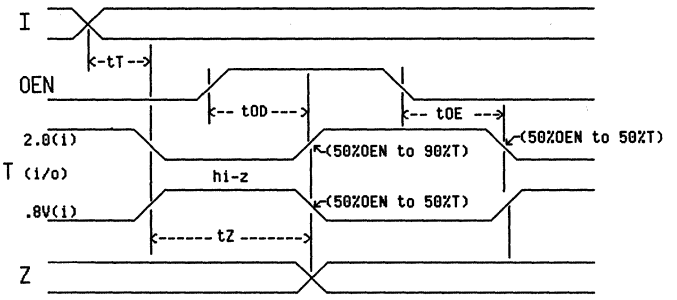
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tT	4.61	5.31	4.63	5.32	4.67	5.36	4.74	5.42
tOE	5.41	5.01	5.43	5.03	5.47	5.07	5.54	5.14
tOD	4.30	4.70	4.30	4.70	4.30	4.70	4.30	4.70
tZ	3.22	3.78	3.34	3.96	3.70	4.50	4.30	5.40

Note: For other operating conditions, use derating curves given in the performance section.

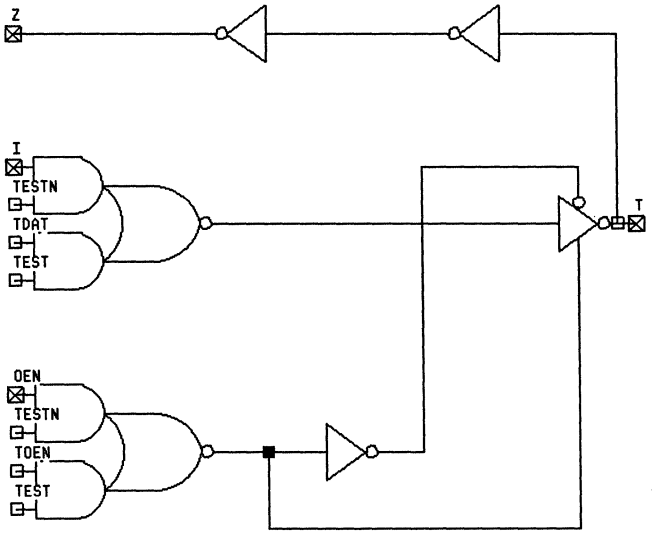
TRT03

TTL TRANSCEIVER INTERFACE

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



TRT031

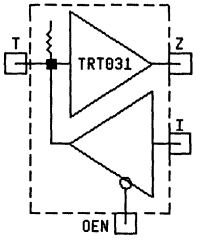
TTL TRANSCEIVER INTERFACE

DESCRIPTION

TRT031 is a non-inverting bidirectional transceiver, with built-in testability. When OEN is HIGH, the output buffer is in the high impedance state. The threshold on the input buffer section is designed for interface with TTL signal levels. Output drive is 8 mA Industrial worst-case and 6 mA Military worst-case. The CAD system automatically connects the TDAT, TEST, TESTN, and TOEN signals, via dedicated routing channels, to the TDAT, TEST, TESTN, and TOEN input buffers, located in the lower left-hand corner of the chip. These signals allow test data on the TDAT pin to force all outputs for parametric testing, when TESTN is LOW. The TOEN input provides for the 3-state function, when TESTN is LOW. If the input is left floating, the pull-up resistor will pull the output to a logic HIGH. This macro is designed for use on VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUTS						I/O	OUTPUT
I	OEN	TDAT	TEST	TESTN	TOEN	T	Z
L	L	X	L	H	X	L	L
H	L	X	L	H	X	H	H
X	H	X	L	H	X	Z	T
H	L	H	H	L	L	H	H
L	L	L	H	L	L	L	L
X	L	X	H	L	H	Z	T
open	H	X	L	H	X	H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	5.0	Output Buffer Input
OEN	Input	3.0	ENABLE Input (Active-LOW)
TDAT	N/A	-	Test Data Input
TEST	N/A	-	Test ENABLE Input
TESTN	N/A	-	Complimentary Test ENABLE Input
TOEN	N/A	-	Test 3-State Input
T	I/O	-	Input/Output
Z	Ouput	-	Input Buffer Output

TRT031

TTL TRANSCEIVER INTERFACE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tT, I-T	4.3 + 0.3 + 0.014 * UL	5.1 + 0.2 + 0.012 * UL
tOE, OEN-T	5.1 + 0.3 + 0.014 * UL	4.7 + 0.3 + 0.014 * UL
tOD, OEN-T	4.30 ns	4.70 ns
tZ, T-Z	2.7 + 0.4 + 0.12 * UL	3.0 + 0.6 + 0.18 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

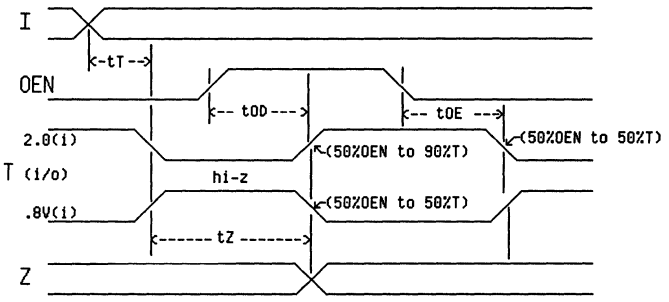
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tT	4.61	5.31	4.63	5.32	4.67	5.36	4.74	5.42
tOE	5.41	5.01	5.43	5.03	5.47	5.07	5.54	5.14
tOD	4.30	4.70	4.30	4.70	4.30	4.70	4.30	4.70
tZ	3.22	3.78	3.34	3.96	3.70	4.50	4.30	5.40

Note: For other operating conditions, use derating curves given in the performance section.

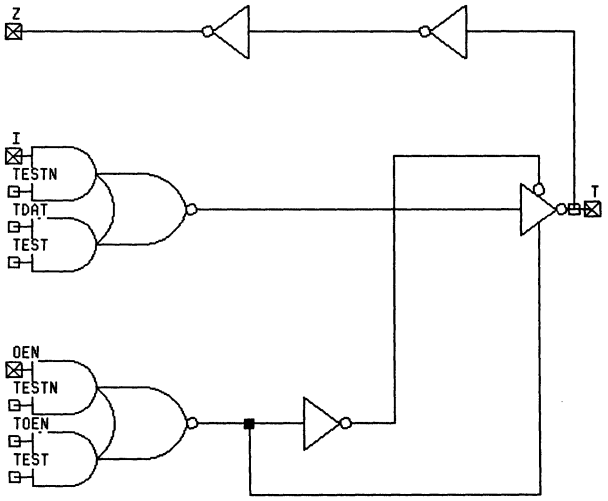
TRT031

TTL TRANSCEIVER INTERFACE

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



TRT03F

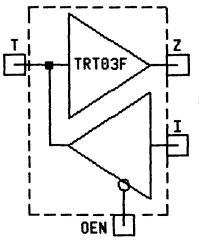
TTL TRANSCEIVER (VGC0500)

DESCRIPTION

The TRT03F is a bidirectional, non-inverting output buffer, made for two-way data transmission. The output ENABLE signal, OEN, is controlled by internal signals only. When OEN is HIGH, the output is in the high impedance state. The threshold of the input buffer is designed to interface with TTL signal levels. This macro is designed for use with the VGC0500 only.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT		I/O	OUTPUT
I	OEN	T	Z
L	L	L	L
H	L	H	H
X	H	hi-z	T

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	3.6	Output Buffer Input
OEN	Input	1.9	ENABLE Input (Active-LOW)
T	I/O	-	Input/Output
Z	Ouput	-	Input Buffer Output

TRT03F

TTL TRANSCEIVER (VGC0500)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tT, I-T	3.3 + 0.3 + 0.014 * UL	3.8 + 0.2 + 0.012 * UL
tOE, OEN-T	3.7 + 0.3 + 0.014 * UL	3.6 + 0.3 + 0.014 * UL
tOD, OEN-T	3.10 ns	3.40 ns
tZ, T-Z	3.2 + 0.2 + 0.18 * UL	5.1 + 0.3 + 0.21 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

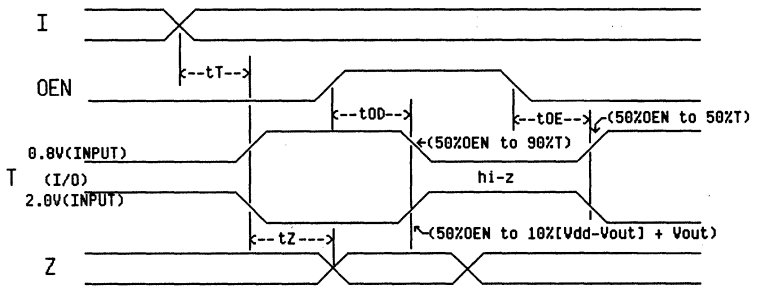
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tT	3.61	4.01	3.63	4.02	3.67	4.06	3.74	4.12
tOE	4.01	3.91	4.03	3.93	4.07	3.97	4.14	4.04
tOD	3.10	3.40	3.10	3.40	3.10	3.40	3.10	3.40
tZ	3.58	5.61	3.76	5.82	4.30	6.45	5.20	7.50

Note: For other operating conditions, use derating curves given in the performance section.

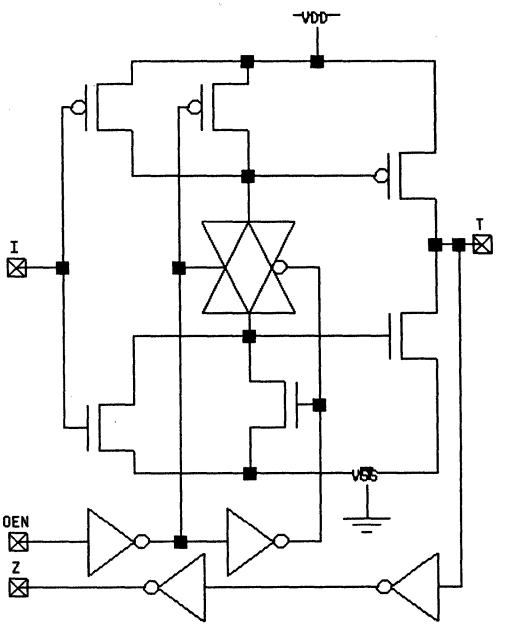
TRT03F

TTL TRANSCEIVER (VGC0500)

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



TRC03

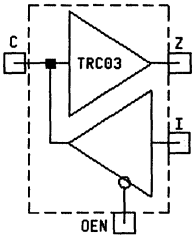
CMOS TRANSCEIVER INTERFACE

DESCRIPTION

The TRC03 is a non-inverting bidirectional transceiver, with built-in testability designed to interface to CMOS signal levels. When OEN is HIGH, the output buffer is in the high impedance state. The output drive is 8mA Industrial worst-case and 6mA Military worst-case. The CAD system automatically connects the TDAT, TEST, TESTN, and TEST signals, via dedicated routing channels to the TDAT, TEST, TESTN, and TOEN input buffers, located in the lower left-hand corner of the chip. These signals allow test data on the TDAT pin to force all outputs for parametric testing, when TESTN is low. This macro is designed for use with VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUTS						I/O	OUTPUT
I	OEN	TDAT	TEST	TESTN	TOEN	C	Z
L	L	X	L	H	X	L	L
H	L	X	L	H	X	H	H
X	H	X	L	H	X	Z	C
H	L	H	H	L	L	H	H
L	L	L	H	L	L	L	L
X	L	X	H	L	H	Z	C

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	5.0	Output Buffer Input
OEN	Input	3.0	ENABLE Input (Active-LOW)
TDAT	N/A	-	Test Data Input
TEST	N/A	-	Test ENABLE Input
TESTN	N/A	-	Complimentary Test ENABLE Input
TOEN	N/A	-	Test 3-State Input
C	I/O	-	Input/Output
Z	Output	-	Input Buffer Output

TRC03

CMOS TRANSCEIVER INTERFACE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tC, I-C	4.56 + 0.04 + 0.01 * UL	5.26 + 0.04 + 0.01 * UL
tOD, OEN-C	4.30 ns	4.70 ns
tOE, OEN-C	5.40 + 0.01 + 0.01 * UL	5.00 + 0.01 + 0.01 * UL
tZ, C-Z	1.47 + 0.43 + 0.13 * UL	2.89 + 0.31 + 0.09 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

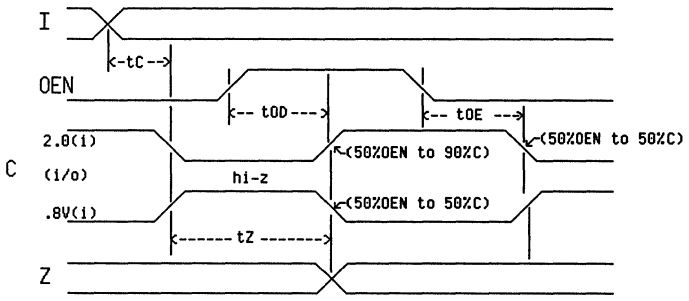
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tC	4.61	5.31	4.62	5.32	4.65	5.35	4.70	5.40
tOD	4.30	4.70	4.30	4.70	4.30	4.70	4.30	4.70
tOE	5.42	5.02	5.43	5.03	5.46	5.06	5.51	5.11
tZ	2.03	3.29	2.16	3.38	2.55	3.65	3.20	4.10

Note: For other operating conditions, use derating curves given in the performance section.

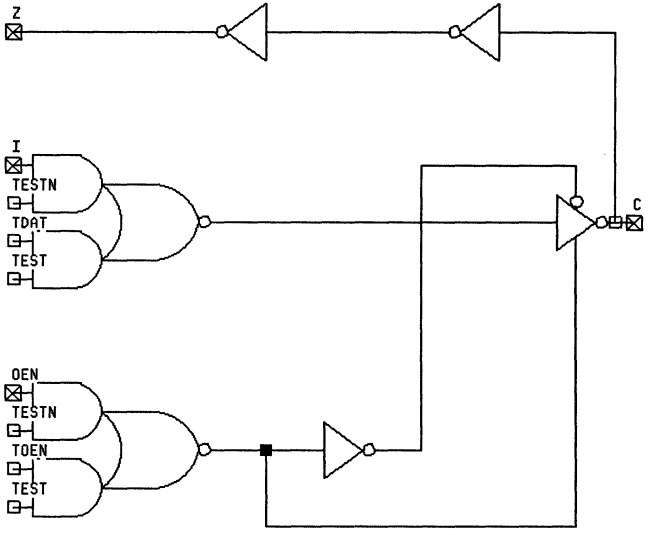
TRC03

CMOS TRANSCEIVER INTERFACE

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



TRC031

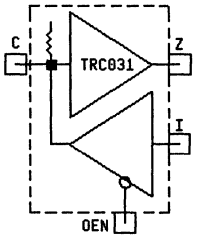
CMOS TRANSCEIVER INTERFACE W/PULL-UP

DESCRIPTION

The TRC031 is a non-inverting bidirectional transceiver, with built-in testability, designed to interface to CMOS signal levels. When OEN is HIGH, the output buffer is in the high impedance state. The output drive is 8 mA Industrial worst-case and 6 mA Military worst-case. The CAD system automatically connects the TDAT, TEST, TESTN, and TOEN signals, via dedicated routing channels, to the TDAT, TEST, TESTN, and TOEN input buffers, located in the lower left-hand corner of the chip. These signals allow test data on the TDAT pin to force all outputs for parametric testing, when TESTN is low. If the input is left floating, the pull-up resistor will pull the output to a logic HIGH. This macro is designed for use with VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUTS						I/O	OUTPUT
I	OEN	TDAT	TEST	TESTN	TOEN	C	Z
L	L	X	L	H	X	L	L
H	L	X	L	H	X	H	H
X	H	X	L	H	X	Z	C
H	L	H	H	L	L	H	H
L	L	L	H	L	L	L	L
X	L	X	H	L	H	Z	C
open	H	X	L	H	X	H	H

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	5.0	Output Buffer Input
OEN	Input	3.0	ENABLE Input (Active-LOW)
TDAT	N/A	-	Test Data Input
TEST	N/A	-	Test ENABLE Input
TESTN	N/A	-	Complimentary Test ENABLE Input
TOEN	N/A	-	Test 3-State Input
C	I/O	-	Input/Output
Z	Output	-	Input Buffer Output

TRC031

CMOS TRANSCEIVER INTERFACE W/PULL-UP

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tC, I-C	4.56 + 0.04 + 0.01 * UL	5.26 + 0.04 + .01 * UL
tOD, OEN-C	4.30 ns	4.70 ns
tOE, OEN-C	5.40 + 0.01 + 0.01 * UL	5.00 + 0.01 + 0.01 * UL
tZ, C-Z	1.47 + 0.43 + 0.13 * UL	2.89 + 0.31 + 0.09 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

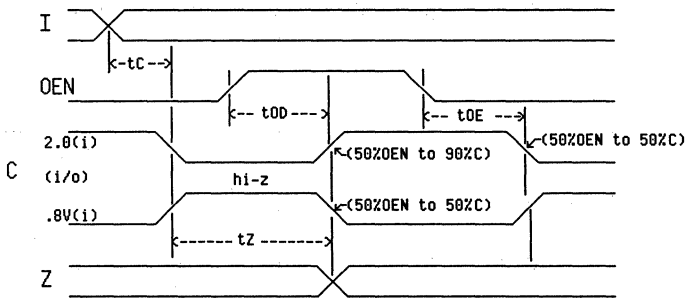
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tC	4.61	5.31	4.62	5.32	4.65	5.35	4.70	5.40
tOD	4.30	4.70	4.30	4.70	4.30	4.70	4.30	4.70
tOE	5.42	5.02	5.43	5.03	5.46	5.06	5.51	5.11
tZ	2.03	3.29	2.16	3.38	2.55	3.65	3.20	4.10

Note: For other operating conditions, use derating curves given in the performance section.

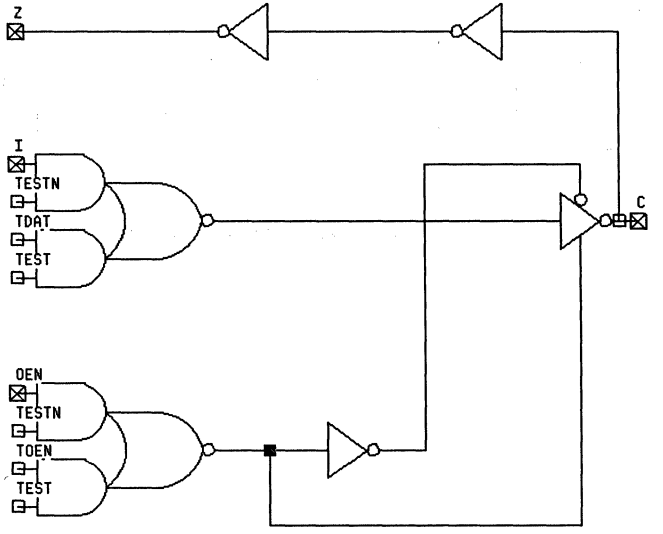
TRC031

CMOS TRANSCEIVER INTERFACE W/PULL-UP

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



TRC03F

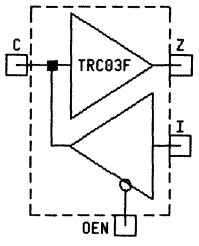
CMOS TRANSCEIVER (VGC0500)

DESCRIPTION

The TRC03F is a bidirectional, non-inverting output buffer made for two-way data transmission. The output ENABLE signal, OEN, is controlled by internal signals only. When OEN is HIGH, the output is in the high impedance state. The threshold of the input buffer is designed to interface with CMOS signal levels. This macro is designed for use with the VGC0500 only.

I/O Cells: 1 **Cell Type:** I/O

SYMBOL



FUNCTION TABLE

INPUT		I/O	OUTPUT
I	OEN	C	Z
L	L	L	L
H	L	H	H
X	H	hi-z	C

PIN DESCRIPTION

Name	Type	U.L.	Description
I	Input	3.6	Output Buffer Input
OEN	Input	1.9	ENABLE Input (Active-LOW)
C	I/O	-	Input/Output
Z	Ouput	-	Input Buffer Output

TRC03F

CMOS TRANSCEIVER (VGC0500)

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tC, I-C	3.4 + 0.3 + 0.014 * UL	3.8 + 0.2 + 0.012 * UL
tOE, OEN-C	3.8 + 0.3 + 0.014 * UL	3.7 + 0.3 + 0.014 * UL
tOD, OEN-C	3.10 ns	3.40 ns
tZ, C-Z	2.7 + 0.2 + 0.140 * UL	3.1 + 0.2 + 0.140 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

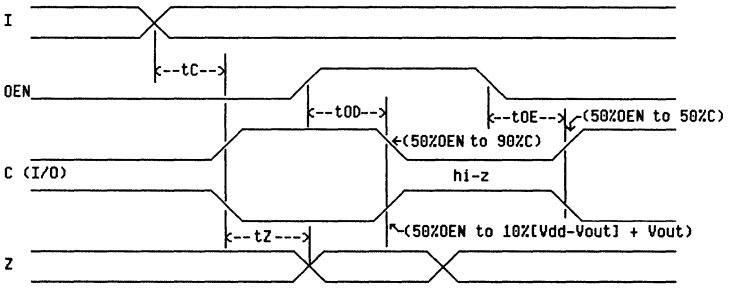
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tC	3.71	4.01	3.73	4.02	3.77	4.06	3.84	4.12
tOE	4.11	4.01	4.13	4.03	4.17	4.07	4.24	4.04
tOD	3.10	3.40	3.10	3.40	3.10	3.40	3.10	3.40
tZ	3.04	3.44	3.18	3.58	3.60	4.00	4.30	4.70

Note: For other operating conditions, use derating curves given in the performance section.

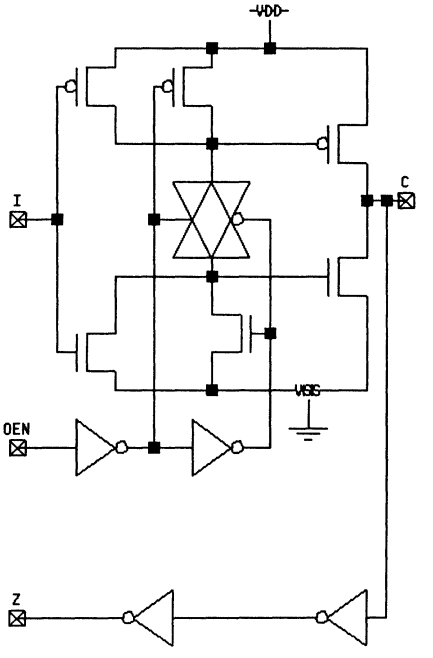
TRC03F

CMOS TRANSCEIVER (VGC0500)

AC CHARACTERISTICS (cont'd)



LOGIC DIAGRAM



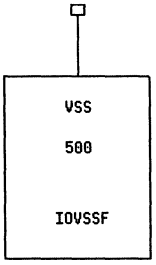
IOVSSF

VSS PAD

DESCRIPTION

The IOVSSF converts any I/O pad into a VSS power connection. This macro is designed for the use with the VGC0500 only.

I/O Cells: 1 **Cell Type:** Ground Pad



PIN DESCRIPTION

Name	Parameter	Maximum DC Current (mA)	Description
VSS	Max. current	51	VSS ground bus to the core

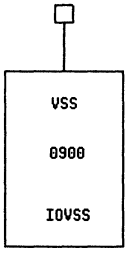
IOVSS

VSS PAD

DESCRIPTION

The IOVSS converts any I/O pad into a VSS power connection. This macro is designed for the use with the VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** Ground Pad



PIN DESCRIPTION

Name	Parameter	Maximum DC Current (mA)	Description
VSS	Max. current	51	VSS ground bus to the core

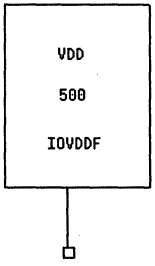
IOVDDF

VDD POWER PAD

DESCRIPTION

The IOVDDF converts any I/O pad into a VDD power connection. This macro is designed for use with the VGC0500 only.

I/O Cells: 1 **Cell Type:** Power Pad



PIN DESCRIPTION

Name	Parameter	Maximum DC Current (mA)	Description
VDD	Max. current	22	VDD power bus to the core

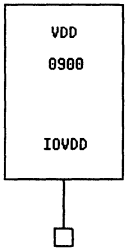
IOVDD

VDD POWER PAD

DESCRIPTION

The IOVDD converts any I/O pad into a VDD power connection. This macro is designed for use with the VGC0900 and above arrays.

I/O Cells: 1 **Cell Type:** Power Pad



PIN DESCRIPTION

Name	Parameter	Maximum DC Current (mA)	Description
VDD	Max. current	63	VDD power bus to the core

Application Note:

Designing with VTI Gate Arrays

APPENDIX C

APPLICATION NOTE:DESIGNING WITH VTI GATE ARRAYS

Advances in CMOS technology and CAE/CAD tools, which offer designers new opportunities and design techniques, are rapidly making it possible for CMOS gate arrays to replace TTL-based devices. The performance of CMOS arrays now exceeds that of equivalent TTL functions, and levels of integration are possible with CMOS arrays that are not feasible with TTL. As a result, there are not only a large number of new design starts using CMOS gate arrays, but even larger numbers of existing TTL-based designs are being replaced by CMOS arrays.

VLSI Technology (VTI) offers a family of nine high-speed, high-density CMOS gate arrays -- the VGC Series (Table 1) -- that have gate densities ranging from 500 to 8000 two-input equivalent gates. Fabricated using advanced 2-micron silicon-gate CMOS technology, these arrays have an effective channel length of 1.3 microns, and are fully supported by design tools that provide an effective means of reducing complex logic or memory functions to single-chip solutions.

	VGC0500	'0900	'1200	'1900	'2400	'3200	'4000	'6000	'8000
Internal Cells	360	576	792	1288	1728	2160	2640	4000	5264
Equiv. Gates 1	540	864	1188	1932	2592	3240	3960	6000	7896
Pin Count:									
Input-only Cells	0	23	27	35	39	43	47	55	63
I/O Cells	40	38	46	58	70	78	86	106	118
Power Pins	4	8	8	8	8	8	8	12	16
Testability Pins	0	3	3	3	3	3	3	3	3
Total Pins	44	72	84	104	120	132	144	176	200

Note 1: An "equivalent Gate" is one 2-input NAND gate.

TABLE I. VGC GATE ARRAY FAMILY

LOGIC RECONFIGURATION

The majority of logic designs implemented in gate arrays fall into two categories:

1. New designs that are defined using gate array macros, thereby achieving optimum performance and gate densities.

2. Existing designs implemented in TTL logic using SSI/MSI functions, which are replaced with equivalent CMOS functions using gate array macros to obtain the desired performance.

In replacing TTL functions, several factors must be considered to most efficiently use gate arrays and maximize the performance of the circuit.

System Partitioning

Although most circuit functions can be implemented very efficiently in CMOS gate arrays, there are some situations in which arrays do not represent the best cost/performance solution. Knowing which functions can most efficiently be implemented is helpful when system partitioning is done.

Gate arrays are ideal for integrating SSI/MSI functions, which are commonly known as randon, or "glue," logic. In a typical system random logic occupies a major portion of board space, which can usually be reduced by replacing the SSI/MSI logic with a few gate arrays. Such functions as encoders, decoders, multiplexers, counters, shift registers, and adders can be effectively integrated in gate arrays, and the majority of the functions of such logic families as the TTL 7400 series and CMOS 4000 series can be replaced.

Programmable logic devices, such as FPLAs, IFLs, and PALs*, consist of AND/OR arrays and offer a fairly rigid structure for logic implementation. For example, they are not well-suited for implementing asynchronous or unstructured logic functions. Gate arrays, however, have an uncommitted logic structure and offer total design flexibility; they can efficiently integrate functions implemented in programmable logic. Yet this internal architecture also makes it impractical to use gate arrays to implement RAM or ROM functions, particularly high-density devices. However, low-denisty, low-performance RAM and ROM devices can be designed as special cases. Other devices for which CMOS arrays are not the best solution because of development time and cost considerations include microprocessors and such large peripheral devices as video and DMA

*PAL is a trademark of Monolithic Memories Inc.

controllers. Also, though it is normally an advantage that CMOS gate arrays offer lower power at high gate desities, this makes them inappropriate for designing high-current drivers. The upper limits for the output drivers of the VGC Series, for example, are from approximately 8mA to 24 mA, which is obtained by paralleling the output buffers.

Unused Logic

In gate array design, the most efficient silicon usage is typically achieved by converting large functional blocks into their primitive components, gates and flip-flops. With a design defined in TTL and implemented using SSI/MSI components, the schematic of the design is first expanded by converting large MSI functional blocks, such as decoders, counters, and shift registers, into more primitive macros, such as NAND/NOR gates, latches, and flip-flops. Functions, inputs, and outputs that are not actually going to be used in the device applications are then deleted to reduce the gate count and improve the performance of the design; this can be a key item in the conversion of an SSI/MSI design into a gate array.

For example, a 4-bit 74LS163 synchronous counter with Load, Clear, Carry-In, and Carry-Out options (figure 1) will always contain the same number of elements, whether or not they are used, and would require 60 gates to be implemented in a gate array. If, however, the counter is to be used only as a 3-bit counter without the Load, Clear, Carry-In, and Carry-Out options options (figure 2), the gate count can be reduced to 30, for a 50% savings. This also improves overall performance because it reduces fan-in and fan-out requirements.

Gate Count

In CMOS gate arrays, a single gate is defined as a two-input NAND or NOR gate that required four transistors, two p-type and two n-type; when being converted to gate arrays, all SSI/MSI components are defined in terms of this basic gate. In the VGC Series, a "core cell" consists of three p-type and three n-type transistors (figure 3), which is equivalent to 1.5 gates. A two-input NAND or NOR gate with a single converter can thus be implemented with a single core cell. Table 2 presents the gate count for basic CMOS functions.

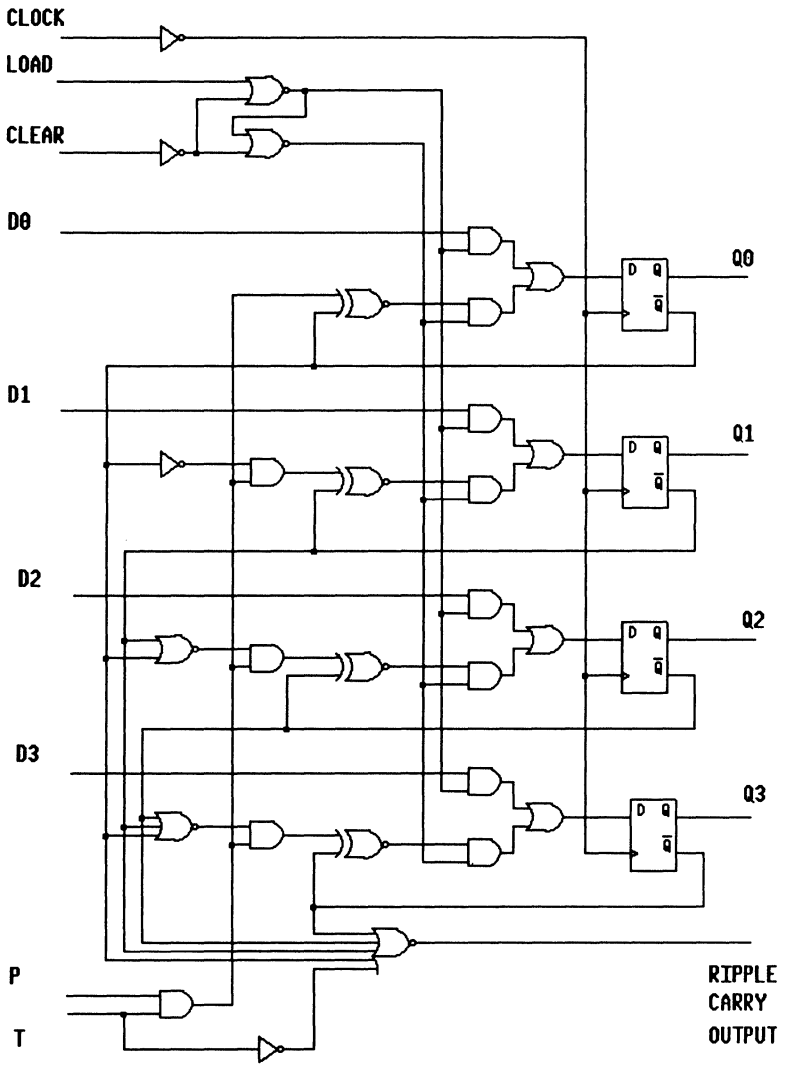


Fig. 1 4-BIT SYNCHRONOUS BINARY COUNTER (74LS163) EQUIV. GATES = 60

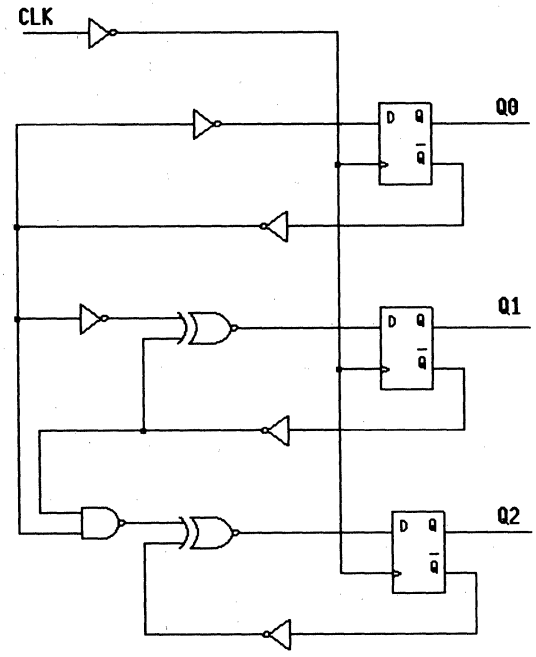


FIG. 2 3-BIT UP COUNTER
GATES = 30

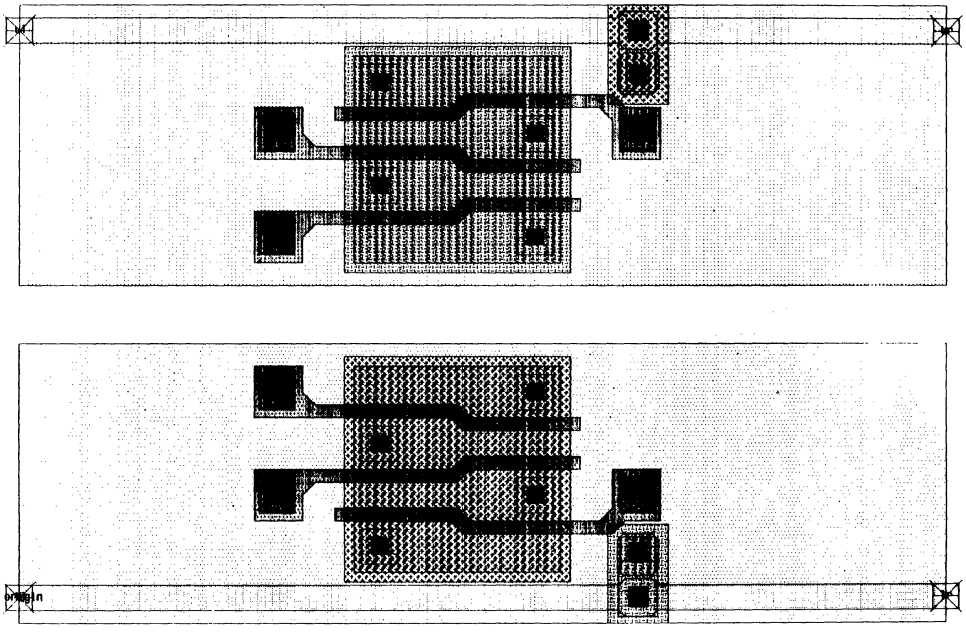


FIG. 3 CORE CELL

BASIC FUNCTION	GATE EQUIVALENCE
INVERTER	.5 or 1
1 TO 5-IN NAND	.5 PER INPUT
6 TO 10-IN NAND	.5 PER INPUT + 2
1 TO 5-IN NOR	.5 PER INPUT
6 TO 10-IN NOR	.5 PER INPUT + 2
1 TO 4-IN AND	.5 PER INPUT + .5
5 TO 8-IN AND	.5 PER INPUT + 2.5
1 TO 4-IN OR	.5 PER INPUT + .5
5 TO 8-IN OR	.5 PER INPUT + 2.5
EXCLUSIVE OR/NOR	2.5
AND-OR-INVERT	.5 PER INPUT
OR-AND-INVERT	.5 PER INPUT
2 TO 1 MUX	2
DATA LATCH WITH SET OR RESET	2.5
DATA LATCH WITH SET AND RESET	3
D FLIP-FLOP WITH SET OR RESET	5
D FLIP-FLOP WITH SET AND RESET	6 or 7
J-K FLIP-FLOP	8

TABLE II. GATE COUNT FOR BASIC CMOS FUNCTIONS

Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv
7400	4	7470	14	74150	61	74248	62
7401	4	7471	18	74151	28	74249	62
7402	4	7472	14	74152	28	74251	32
7403	4	7473	16	74153	24	74253	26
7404	3	7474	12	74154	50	74257	18
7405	3	7475	10	74155	20	74258	16
7406	3	7476	16	74156	20	74259	68
7407	6	7477	10	74157	15	74260	6
7408	6	7478	18	74158	17	74261	72
7409	6	7480	16	74159	50	74265	5
7410	5	7482	26	74160	65	74266	12
7411	6	7483	55	74161	60	74273	44
7412	5	7485	50	74162	65	74276	38
7415	6	7486	10	74163	60	74278	38
7416	3	7487	17	74164	50	74279	10
7417	6	7490	40	74165	70	74280	56
7420	4	7491	50	74166	65	74281	163
7421	5	7492	35	74167	60	74283	62
7422	4	7493	21	74168	70	74290	41
7423	7	7494	35	74169	70	74293	37
7425	6	7495	40	74170	120	74295	41
7426	4	7496	40	74173	40	74298	36
7427	5	7497	110	74174	35	74299	132
7428	4	7498	35	74175	25	74323	132
7430	6	7499	45	74176	40	74348	49
7432	6	74100	25	74177	38	74351	64
7433	4	74102	26	74178	55	74352	26
7437	4	74103	16	74179	55	74353	28
7438	4	74106	18	74180	27	74363	25
7440	4	74107	16	74181	104	74364	47
7442	30	74108	18	74182	34	74373	33
7443	30	74109	18	74183	15	74374	55
7444	30	74110	12	74190	70	74375	10
7445	30	74111	18	74191	66	74376	40
7448	60	74112	18	74192	73	74377	72
7449	50	74113	18	74193	67	74378	54
7451	8	74114	18	74194	59	74379	40
7452	7	74116	25	74195	38	74381	160
7453	10	74120	15	74196	40	74386	12
7454	9	74135	20	74197	38	74390	52
7455	6	74136	10	74198	88	74393	42
7460	5	74138	25	74199	86	74395	40
7461	6	74139	22	74226	70	74398	36
7462	9	74145	24	74245	52	74399	36
7464	10	74147	35	74246	58	74670	125
7465	10	74148	35	74247	58		

TABLE III. GATE COUNT FOR 74XX TTL FAMILY

Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv
4000	4	4022	40	4069	3	40163	54
4001	4	4024	40	4070	10	40174	35
4002	4	4026	60	4071	6	40175	23
4006	103	4027	23	4072	5	40192	65
4007	2	4028	26	4073	6	40193	62
4008	32	4029	80	4075	6	4510	82
4009	3	4030	10	4076	49	4511	52
4010	3	4032	63	4077	10	4512	23
4011	4	4034	110	4078	6	4514	78
4012	4	4035	39	4081	6	4515	78
4013	12	4038	64	4082	5	4516	79
4014	51	4040	66	4089	80	4518	44
4015	58	4041	6	4094	86	4519	36
4017	48	4042	13	4099	82	4520	42
4018	41	4043	24	40106	30	4532	39
4019	10	4044	24	40107	18	4555	15
4020	77	4051	15	40160	59	4556	11
4021	55	4068	6	40162	59		

TABLE IV. GATE COUNT FOR CMOS 4000 SERIES

FUSE PROGRAMMABLE LOGIC	TYPICAL GATE COUNT
PAL SERIES 20:	
- PAL 10L8, 10H8, 12L6, 12H6, 14L4, 14H4, 16L2, 16H2, 16C1	50 - 70
- PAL 16L8, 16R8, 16R6, 16R4	150 - 180
PAL SERIES 24:	
- PAL 12L10, 14L8, 16L6, 18L4, 20L2, 20C1	80 - 100
- PAL 20L0, 20X10, 20X8, 20X4	200 - 250
IFL SERIES 28:	
- FPLA 82S100/101	230 - 240
- FPLA 82S102/103	50 - 60
- FPLS 82S104/105	340 - 350
- FPRP 82S106/107	230 - 240
IFL SERIES 20:	
- FPGA 82S150/151	50 - 60
- FPLA 82S152/153	150 - 160
- FPLS 82S154-159	200 - 220

TABLE V. TYPICAL GATE COUNT FOR FUSE PROGRAMMABLE LOGIC

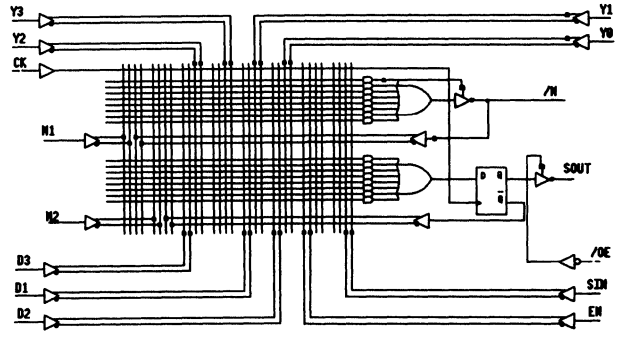
The equivalent gate count for such standard devices as the 74LS TTL series (table 3) and 4000 CMOS series (table 4) is based on the assumption that all the device functions are being used. However, in most applications, not all the functions in a component are in fact used; therefore, the gate count for a given component can be minimized when implemented in a CMOS array. This allows more efficient use of silicon and, because the gate count contributes to the interal fan-in and fan-out requirements, greater control over delay factors.

All existing fuse-programmable logic devices use bipolar TTL logic. The internal structures of these devices consist of AND/OR logic, which is usually represented in Boolean expressions or in fuse format. Such logic can very easily be directly translated into NAND/NAND logic in gate arrays. As a result of their high drive capability, bipolar programmable devices can have AND gates with as many as 20 inputs. In CMOS arrays, such high-input gates are replaced with multi-level, low-input logically equivalent gates. With typical gate utilization of a programmable device being less than 50%, arrays can yield significant savings in silicon area and power consumption. (Table 5 presents equivalent gate counts for various programmable logic devices.)

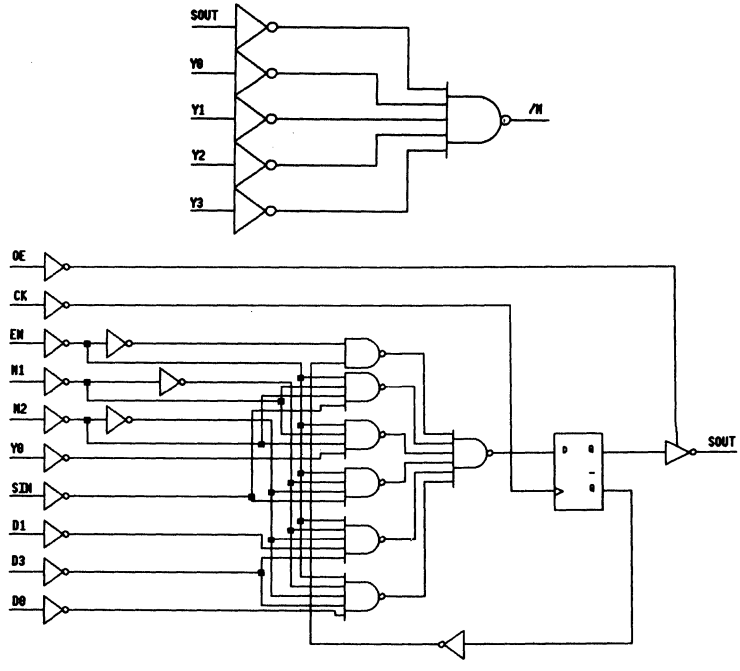
For example, figure 4 illustrates the conversion of a PAL circuit into its equivalent gate array logic. A portion of the PAL logic diagram is shown, with intact fuses represented by "X", in figure 4A; the equivalent logic as implemented in the CMOS array, in which the AND/OR structure of the TTL implementation has been replaced by NAND/NAND logic, is presented in figure 4B. The PAL circuit contains AND and OR gates whose fixed inputs may or may not be used, while unused gates in the gate array logic have been eliminated, simplifying the logic and reducing the gate count.

PERFORMANCE DETERMINERS

In CMOS gate array design, the primary factors that influence the AC performance of a gate are:



A. PORTION OF PAL LOGIC DIAGRAM
(X REPRESENT FUSE INTACT)



B. CMOS GATE ARRAY IMPLEMENTATION

FIG. 4 PAL TO GATE ARRAY LOGIC CONVERSION

1. Supply voltage
2. Operating Temperature
3. Process variation
4. Capacitive loading (fan-out)
5. LOW-to-HIGH and HIGH-to-LOW (L-H and H-L) transitions, which have an impact on fan-in requirements.

As the supply voltage is raised, propagation delay through a gate is reduced (figure 5). However, due to a reduction in carrier mobility, the propagation delay of a gate increases with a rise in temperature (figure 6).

Depending upon the heat-dissipating capability of the package, junction rather than ambient temperature may be used to calculate performance. When this is done, the junction temperature is obtained by adding the rise in temperature under dynamic conditions to the operating temperature.

Normal variations in process parameters cause changes in the threshold voltage of a CMOS gate, which affects speed. The propagation delay of a gate increases significantly when worst-case rather than nominal process parameters are encountered.

Fan-Out Considerations

The performance of a CMOS gate is determined by its intrinsic delay and by the capacitive loading at its output (fan-out). The propagation delay of a CMOS gate can be approximated by:

```
tTOTAL = tDEL + tINT + tNLF * UL
```

where
tTOTAL = Total delay (ns)

tDEL = Internal delay (ns)

tINT = Intrinsic output delay (ns)

tNFL = Normalized load factor (ns/UL)

UL = Unit Load (0.15pF)

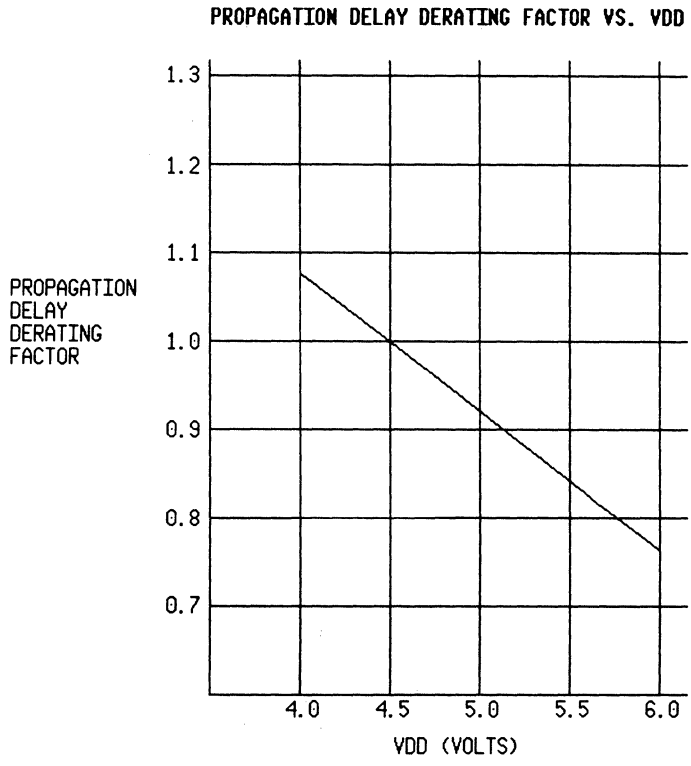


FIG. 5 PROPAGATION DELAYS VS SUPPLY VOLTAGE

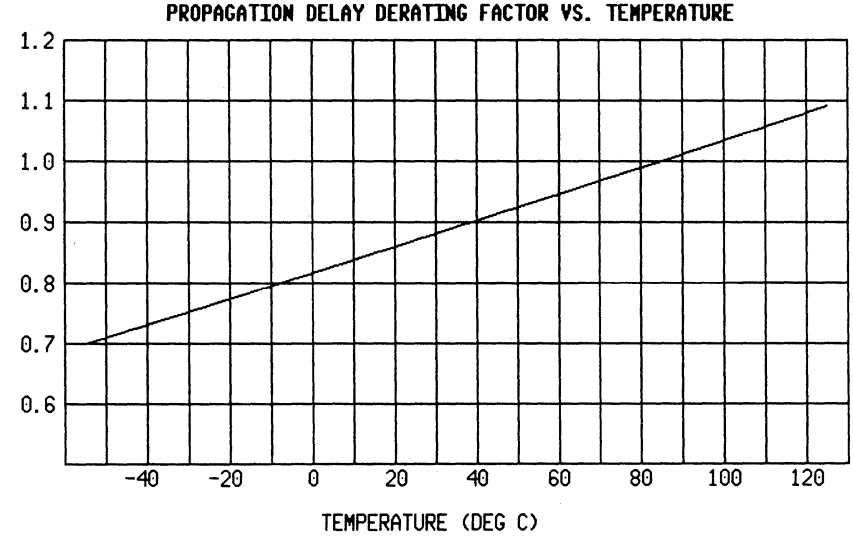


FIG. 6 PROPAGATION DELAY VS TEMPERATURE

In the formula above, the internal, intrinsic delay and normalzed load factor can be obtained from the Macro Library entry for each macro. The actual interconnect capacitance is not known until the mask layout is completed, so statistical values are used in the initial stages of the design cycle. The fan-out of a gate, expressed in terms of unit loads, can be approximated by assuming the following values:

```
One unit load (a single input)= 0.15 pF
Metal capacitance/unit length
     First-layer metal          = 0.00648 pF/mil
     Second-layer metal         = 0.00419 pF/mil
Typical metal
  length/connection             = 15 mils
Worst-case expected metal
  length/connection             = 30 mils
For typical wire length:
     First-layer metal          = 30%
     Second-layer meta          = 70%
For worst-case wire length:
     First-layer metal          = 50%
     Second-layer metal         = 50%
```

In general, if a CMOS gate with heavy fan-out is part of the critical path on a chip, redundant circuitry should be added to minimize the propagation delay of the signals. For example, a two-input NAND gate driving a two-input NOR gate with a fan-out of 15 unit loads may be part of three critical paths in a gate array application; this might require the NOR gate to be replicated three times and the NAND gate to be duplicated (figure 7).

The amount of redundancy introduced into the curcuit to optimize fan-out/speed tradeoffs is entirely dependent upon the individual application. Every time a gate is duplicated, the fan-out of the previous gate is increased. In some cases, redundant gates may need to be added back to the input pins.

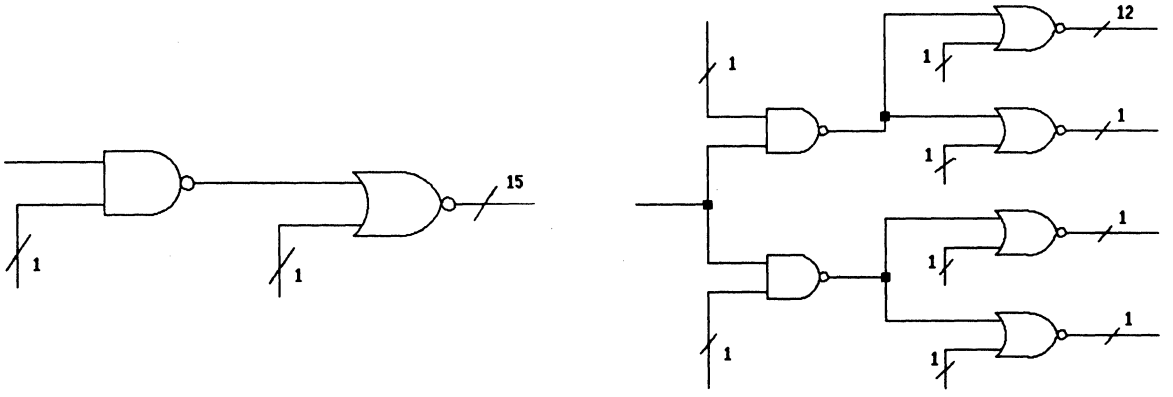


FIG. 7 FAN-OUT DISTRIBUTION

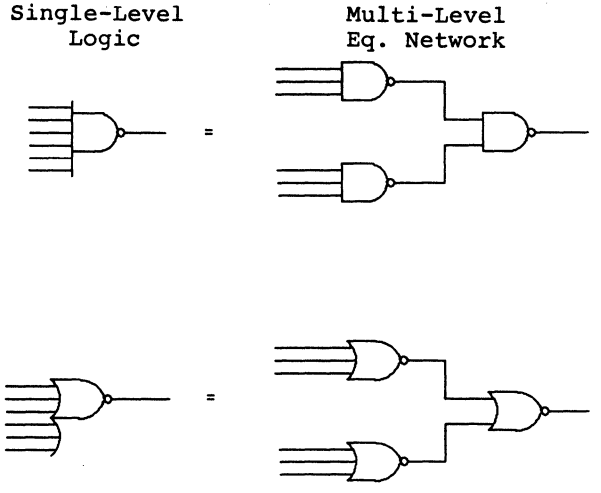


FIG. 8 EQUIVALENT GATE NETWORK

Fan-In Considerations

In CMOS, p-type transistors are slower than n-type transistors of the same size. This causes disparities between LOW-to-HIGH and HIGH-to-LOW transitions that can, under some circumstances, be very significant.

The performance of a CMOS gate is degraded as the number of inputs to it is increased. As a rule, logic gates requiring more than five inputs should be implemented in two or more levels of logic by using simple transformation techniques derived from Boolean algebra. (Figure 8 illustrates the conversion of six-input CMOS gates into two-level logic equivalent gates using this technique.)

As the number of inputs to a CMOS NOR gate increases, the L-H transition becomes worse because of the increased series resistance of the p-channel devices. Similarly, an increase in the number of inputs to a CMOS NAND gate adversely affects the H-L transition. For a given number of inputs to a CMOS NAND gate gate is faster than a NOR gate. In certain instances, the performance of a critical path may be optimized by replacing NOR/OR structures with equivalent NAND gates (figure 9).

Common industry practice is to present propagation delays that are developed by averaging the L-H and H-L transitions. Because of the importance of these parameters, however, VTI macro data sheets contain data for both transitions.

Delay Calculation Example

Use of the transition specifications in determining delay can be seen in the calculations for the A-to-Z delay (tPD) of the two-input NAND gate shown in figure 10. The steps in this calculation are:

1. Calculate number of Unit Loads (UL) at the output node (Z) of NAND gate.

```
T(UL) = I(UL) + M(UL)

where
I(UL) = Number of Unit Loads due to INV03
M(UL) = Number of Unit Loads due to
          interconnect metal
      = Interconnect Metal capacitance/0.15 pF
      = (30 x 0.00648 + 30 x 0.00419)/0.15
      = 2 UL

T(UL) = 3 + 2 = 5 UL
```

2. Calculate delay (tPD) using transition values from the macro data sheet (appendix A) and the formula: tTOTAL = tDEL + tINT + tNLF * UL.

```
tPD = (tPLH + tPHL)/2

where
tPLH = 0.9 ns + 0.5 ns + 0.26 ns/UL * 5 UL
     = 2.7 ns
tPHL = 0.3 ns + 0.4 ns + 0.14 ns/UL * 5 UL
     = 1.4 ns

 tPD = (2.7 ns + 1.4 ns)/2 = 2.05 ns
```

This delay is calculated assuming worst-case parameters, an operating voltage (VDD) of 4.5 V, and an operating temperature (TA) of 85 deg. C. Performance at any other voltage or temperature can be calculated using the derating curves shown in figures 5 and 6.

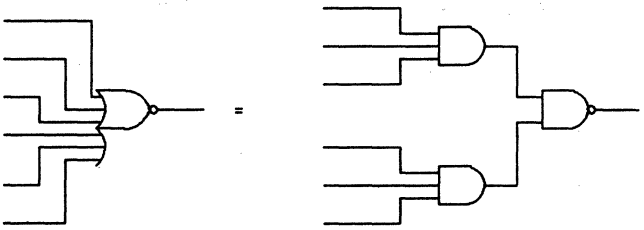


FIG 9. OR GATE EQUIVALENCE

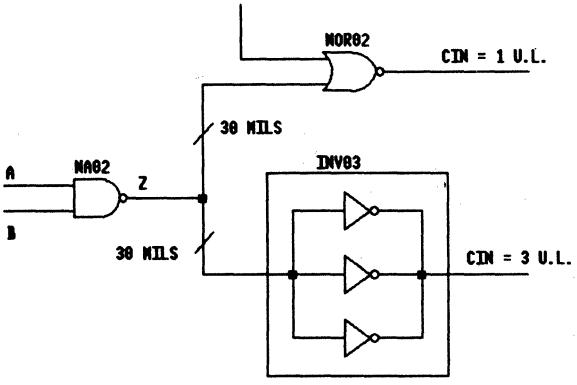


FIG.10 DELAY CALCULATION EXAMPLE

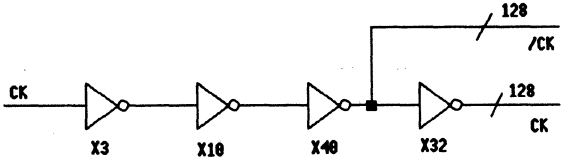


FIG 11. CLOCK TREE FOR A 64-BIT SHIFT REGISTER

Power Dissipation

In CMOS gate arrays, power dissipation is determined by leakage currents, transient currents, and frequency of operation:

```
P = Pq + Pt + Pd
```

where
Pq = power dissipation due to leakage
Pt = power dissipation due to transient currents
Pd = power dissipation due to frequency of operation (under dynamic conditions).

In CMOS devices, Pq is the quiescent power dissipation and is typically a few microwatts. Transient currents are associated with input switching transitions, in which the pull-up and pull-down transistors are both simultaneously on for a short time. They are dependent upon device geometries, and upon the frequency and rise and fall times of the input signal. Typically, the power dissipation due to transient spikes is negligible.

Power consumption under dynamic conditions can be calculated by:

```
Pd = C x V*V  x F
```

where
Pd = power dissipation per gate under dynamic conditions
C = capacitive load per gate
V = operating voltage
F = frequency of operation

Because not all gates switch simultaneously or operate at the maximum frequency, it is difficult to calculate the actual power consumption in a gate array. In many cases, a reasonable approximation can be obtained by multiplying the number of gates used in a design. For example, typical power consumption of a VGC0500 with an operating frequency of 10 MHz, an operating voltage of 5.0 V, and a per-gate capacitance of 0.5 pF could be estimated by:

```
Pd = 0.5 pF/gate x 5.0 V x 5.0 V x 10 MHz
   = 125 uW/gate
```

Number of gates: 540
Number of gates utilized (80%): 432
Number of gates switching each cycle (20% typical): 86
Total core dissipation = 10 mW

Number of I/O buffers: 40
Number of output buffers switching each cycle: 8
Output capacitive load: 50 pF
Total output dissipation = 100 mW

Total power dissipation = 110 mW

VTI MACROS

Hard Macros

A hard macro is defined as a function that has been pre-designed and implemented in gate arrays and whose electrical characteristics can be determined accurately because it has a fixed layout structure. The VGC Series offers an extensive library of hard macros. (Table 6 provides a listing of hard macros available in VTI's gate array macro library).

The internal hard macros cover a wide range of such basic logic functions as inverters, buffers, and NAND/NOR gates with from two to eight inputs, and include complex gates and internal three-state devices. In addition, a variety of latches and flip-flops with such options as Set, Reset, buffered clock, and scan test inputs are available.

TABLE VI. VGC SERIES MACRO LIBRARY

INTERNAL CELL MACROS

	MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION
BASIC	GATES		
	NA02	1	2-NAND
	NA02I	1	2-NAND & INVERTER
	NA03	1	3-NAND
	NA04	2	4-NAND
	NA05	2	5-NAND
	NA05I	3	5-NAND & INVERTER
	NA06	2	6-NAND
	NOR02	1	2-NOR
	NOR02I	1	2-NOR & INVERTER
	NOR03	1	3-NOR
	NOR04	2	4-NOR
	AND02	1	2-AND
	OR02	1	2-OR
	X2NA04	3	DUAL 4-INPUT NAND
INVERTERS/BUFFERS			
	INV11	1	DUAL 1X INVERTERS
	INV12	1	INVERTERS (1X and 2X)
	INV03	1	INVERTERS (3X)
	BUF02	1	NON-INVERTING INTERNAL BUFFER, 2X
	INV01T	1	3-STATE INVERTER (INTERNAL,1X)
	INV02T	2	3-STATE INVERTER (INTERNAL,2X)
	INV03T	3	3-STATE INVERTER (INTERNAL,3X)
COMPLEX GATES			
	XOR02	2	2-IN EXCLUSIVE-OR
	XNOR02	2	2-IN EXCLUSIVE-NOR
	XNOR021	2	2-IN EXCLUSIVE-NOR
	AOI21	1	2-1 AND-OR-INVERTER
	OAI21	1	2-1 OR-AND-INVERTER
	AO22	2	2-2 AND-OR W/COMP. OUTPUTS

INTERNAL CELL MACROS (continued)

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION
COMPLEX GATES (continued)		
AOI222	2	2-2-2 AND-OR-INVERTER
AOI22I	2	2-2 AND-OR-INVERT & 2X INV.
AOI33	2	3-3 AND-OR-INVERTER
LATCHES		
LA01	3	BUFFERED LATCH,
LAE01	3	D-LATCH
LAE01T	4	W/3-STATE OUTPUT
LAE01S	5	W/SCAN LOGIC
LA02	3	W/CLEAR, BUFFERED OUTPUTS
LAE02	3	W/CLEAR
LAE021	2	W/CLEAR, EXTERNAL ENABLE
LAE021T	3	W/CLEAR, EXTERNAL ENABLE & 3-STATE OUTPUTS,
MEM01	3	GATED W/3-STATE OUTPUT
MEM02	3	GATED W/3-STATE OUTPUT
FLIP FLOPS		
DFP01	4	D FLIP-FLOP
DFP74	6	W/SET, CLEAR
DFP011	4	W/EXTERNAL CLOCKS
DFP011T	4	W/3-STATE OUTPUT, EXT. CLK
DFP01S	6	W/SCAN LOGIC
DFP02	5	W/CLEAR DIRECT
DFP021	4	W/CLEAR, EXTERNAL CLOCKS
DFP021T	5	W/CLEAR, EXTERNAL CLOCKS, 3-STATE OUTPUT
DFP02S	7	W/SCAN, CLEAR
DFP03	5	W/SET
DFP031	4	W/SET, EXTERNAL CLOCKS
DFP04	6	W/SET, CLEAR
DFP05	4	W/BUFFERED OUTPUT
JKN02	7	JK FLIP-FLOP W/ CLEAR
JKN76	8	JK FLIP-FLOP
TF02	5	TOGGLE FLIP-FLOP W/CLEAR

INTERNAL CELL MACROS (continued)

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION
MULTIPLEXERS/DECODERS		
MX02	3	2 TO 1 MULTIPLEXER (MUX)
MX04	5	4 TO 1 MUX
MXE04	6	4 TO 1 MUX (1/2 74153)
MXE041	5	4 TO 1 MUX W/ENABLE
DC24	4	1 OF 4 DECODER
DC139	7	1 OF 4 DECODER, W/ENABLE
MISC. MACROS		
ADD01	6	1-BIT FULL ADDER

EXTERNAL CELL MACROS

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION
INPUT BUFFERS		
IOT01F	1	TTL INPUT BUFFER, VGC0500
IOT01	1	INPUT BUFFER
IOT011F	1	INPUT BUFFER W/PULL-UP, VGC0500
IOT011	1	INPUT BUFFER W/PULL-UP
IOC01F	1	CMOS INPUT BUFFER, VGC0500
IOC01	1	INPUT BUFFER
IOC011F	1	INPUT BUFFER W/PULL-UP, VGC0500
IOC011	1	INPUT BUFFER W/PULL-UP
IOT04	1	TTL INPUT BUFFER; 4:1 RATIO
IOT041	1	TTL INPUT BUFFER W/PULL-UP, 4:1 RATIO

IOS02	1	SCHMITT TRIGGER INPUT BUFFER
IOS02F	1	INPUT BUFFER, VGC0500
IOS021F	1	INPUT BUFFER W/PULL-UP, VGC0500

EXTERNAL CELL MACROS (continued)

MACRO NAME	NO. OF CELLS	MACRO DESCRIPTION
OUTPUT BUFFERS		
OB01F	1	STANDARD, 10 mA, VGC0500
OB03F	1	3-STATE, VGC0500
OB04F	1	STANDARD, 8 mA VGC0500
OB01	1	STANDARD, 8 mA
OB03	1	3-STATE
TRANSCEIVERS		
TRT03	1	TTL TRANSCEIVER INTERFACE
TRT031	1	TTL TRANSCEIVER INTERFACE W/PULL-UP
TRT03F	1	TTL TRANSCEIVER INTERFACE, VGC0500
TRC03	1	CMOS TRANSCEIVER INTERFACE
TRC031	1	CMOS TRANSCEIVER INTERFACE W/PULL-UP
TRC03F	1	CMOS TRANSCEIVER INTERFACE, VGC0500
POWER PADS		
IOVSSF	1	VSS POWER PAD, VGC0500
IOVSS	1	VSS POWER PAD,
IOVDDF	1	VDD POWER PAD, VGC0500
IOVDD	1	VDD POWER PAD,

NA02

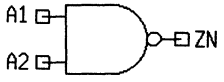
2-INPUT NAND GATE

DESCRIPTION

The NA02 combines inputs A1 and A2, to provide the NAND function at output ZN.

Cells: 1 **Cell Type:** Internal

SYMBOL



FUNCTION TABLE

INPUTS	OUTPUTS
A1 A2	ZN
L X	H
X L	H
H H	L

PIN DESCRIPTION

Name	Type	U.L.	Description
A1	Input	1.0	Data Input
A2	Input	1.0	Data Input
ZN	Output	-	Data Output

NA02

2-INPUT NAND GATE

AC CHARACTERISTICS

CONDITIONS: VDD = 4.5 V, worst-case process
TEMP = 70 deg C ambient, 85 deg C junction
UL = Unit Load = 0.15 pF

PERFORMANCE EQUATIONS

	RISE	FALL
tD, A2->ZN	1.0 + 0.7 + 0.26 * UL	0.2 + 0.6 + 0.21 * UL

PROPAGATION DELAYS (ns) FOR SAMPLE LOADS

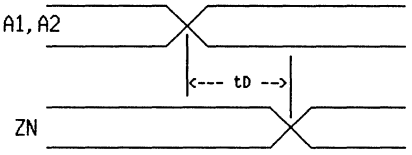
	UL = 1		UL = 2		UL = 5		UL = 10	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
tD	2.0	1.0	2.2	1.2	3.0	1.9	4.3	2.9

Note: For other operating conditions, use derating curves given in the performance section.

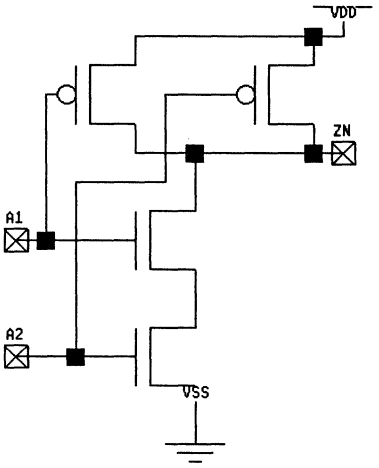
NA02

2-INPUT NAND GATE

AC CHARACTERISTICS (cont'd)



CIRCUIT DIAGRAM



Peripheral macros include input, output, and transceiver cells. The input buffer macros offer TTL and CMOS interface options with or without pull-up. Output buffer macros are available with standard, three-state, and bidirectional features, and with variable output drive.

Each hard macro is fully characterized for typical, worst-case industrial and worst-case military conditions. For each of these conditions, base delay (in nanoseconds) and load factor (in nanoseconds/picofarad) for both the LOW-to-HIGH and HIGH-to-LOW transitions are given. Input capacitance (fan-in) is expressed in terms of unit load; for a single input, the unit load is 0.15 pF. Fan-out delays are calculated using input capacitance and capaticance due to metal length. The performance of TTL buffers is calculated for a 2.5 V midpoint.

Soft Macros

Soft macros do not have a fixed layout structure, but are laid out during the place-and route process. They may have more than one configuration, depending upon design criteria and functional variation. The advantage is that the designer can define complex structures directly in TTL-like logic functions and avoid time-consuming TTL-to-CMOS conversion, and simultaneously optimize performance of the design.

Soft macros are hierarchically designed using hard macros as primitives, but they cannot be accurately characterized prior to their implementation in a gate array. Therefore, during the initial design phase, soft macros should only be used to approximately estimate delays through logic networks.

The soft macros reside in the CAE/CAD system; a designer may select one, modify it to meet specific requirements, then refer to it as a new soft macro. The actual implementation of these macros is handled by design automation tools that expand them into their hard macro primitives during the schematic capture phase.

VTI's soft macro library will include some of the most commonly used functions, including decoders, encoders, magnitude comparators, parity checkers, binary/decade and up/down counters, shift registers, adders, and ALUs. The design of these is based on optimizing performance characteristics and gate usage.

CONSIDERATIONS FOR DESIGNING WITH VTI MACROS

Clock Drivers

When long chains of counters or shift registers are used in CMOS circuits, special care must be taken to minimize the skew between the opposite phases of the clock signals. If, because of excessive skew in the clock drivers, the overlap between the two phases of the clock is long enough, master/slave flip-flops could become transparent latches and cause the circuit to malfunction.

Some flip-flops contain an internal clock buffer and require a single clock edge. Other designs require both polarities of the clock to be generated externally. Clock drivers for such flip-flops are constructed by parelleling inverters in a tree configuration, in which the maximum allowable load on any given inverter is two flip-flops (the equivalent of four gate pairs).

With one clock edge derived from the other, one of the clock drivers will have a heavier load than the other because, in addition to the flip-flops, a driver must drive the inverters that generate the opposite clock signal. To compensate for this, the initial step in building a clock tree is to determine the number of inverters needed to drive only the flip-flops, using the "maximum of two flip-flops per single inverter" rule. The rest of the tree is then developed backwards, using the "four gate pairs per inverter" rule, until the load of the final driver is less than four gates. This technique, applied to a 64-bit shift register, is illustrated in figure 11.

Input Interface

Maximum and minimum input threshold levels for CMOS logic are specified as being 30% and 70%, respectively, of the supply voltage. The maximum logic 0 (LOW) level for a device operating at 5 V would thus be 1.5 V and the minimum logic 1 (HIGH) level would be 3.5 V. For TTL logic families, the maximum LOW level is 0.8 V and the minimum HIGH level is 2.0 V. Because the minimum TTL HIGH level is lower than the minimum level recognized by a CMOS gate, level translation buffers are used when CMOS arrays interface with TTL or LSTTL components.

Level translation buffers dissipate power unless the input signals are pushed all the way to the rails. For a given operating voltage, the gate current is dependent upon the input voltage. Therefore, if power dissipation is an important consideration, it is recommended that a pull-up device be connected to the gate input to fully switch off the p-channel devices.

VTI's gate array macro library contains peripheral cells that can interface with either CMOS or TTL input signals and do not require any additional cells from the core. In addition, each input cell is protected against electrostatic discharge by an input network consisting of a series resistor and shunt diodes. The resistor-diode combination clamps the input voltage to within a diode voltage drop of the power rail levels, which prevents gate-oxide ruptures due to electrostatic discharge.

Pull-Up / Pull-Down

The high-impedance characteristics of CMOS gates combine with leakage currents to cause logic gates with floating inputs to be biased in the linear region, in which the pull-up and pull-down devices are both on. Besides increasing overall power dissipation in the circuit, floating gates have indeterminant output levels, which can cause logic malfunctions. It is strongly recommended that on-chip or off-chip components be used to terminate either to VDD or VSS those gates that could be unconnected or temporarily left open.

VTI's gate array macro library includes input buffers with built-in pull-up resistors. The equivalent impedance of these devices when biased into saturation is relatively large, minimizing power consumption on the chip. Because they are susceptible to threshold variations and the equivalent impedance may vary over the entire range of process variations, these resistors are for pull-up use only.

I/O Cells

The type of peripheral I/O cell used in the VGC Series is totally user-definable. Any cell can be designed as a TTL or CMOS input ,a standard or three-state output, or a transceiver whose output enable is controlled by an interanl signal. The I/O cells also support on-chip test features. All of these functions can be performed without involving any extra internal gates.

Symmetrical output drive and propagation delays are achieved by making the p-channel device of the output driver physically larger than the n-channel device. A single output buffer sinks 8 mA (10 mA for VGC0500) over the worst-case commercial/industrial voltage and temperature ranges, and output buffers can be paralleled to increase sinking or sourcing currents. However, care should be taken not to increase the maximum current density limits to levels that would cause reliability hazards.

In addition, an increase in output current may cause a significant voltage drop across the power rails that would require additional power pins to preserve the noise margin of the device. Also, if several outputs with high capacitive loads are switching simultaneously, the internal logic should be isolated from large AC currents. This can be accomplished by providing the logic with a different pair of power supply pins from that used to operate the output buffers.

Internal Three-State Buses

Internal buses may be designed using transmission gates or other macros from the macro library, but transmission gates should not be used unless recommended by VTI's applications staff.

When designing with transmission gates, care must be taken that all internal buses be defined because a floating bus may result in propagation of an incorrect logic state. In addition, since the designer implements the bus structure, these buses have no pre-charge circuitry; pull-up macros must be used to perform this function, allowing the bus to revert to a logic 1 (HIGH) state when all of the bus source outputs are in the high-impedance state.

Testability

Because testability should be incorporated into a circuit during the early stages of the design phase rather than as an afterthought, VTI's macros include three pins that are dedicated to implementing various test schemes. The VGC Series also offers other "design for testability" (DFT) features that enhance testability and simplify device testing.

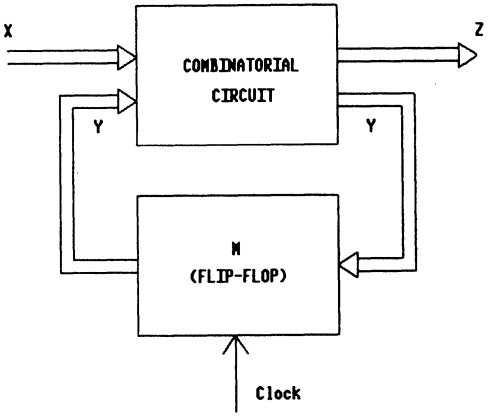
The primary considerations in designing for testability are controlability, observability, and predictability. Controlability refers to the ability to excite a given circuit node from external inputs, while observability refers to the ability to observe the response of the excited nodes at external outputs. Both of these capabilities can be improved by using test points as primary inputs and outputs. The predictability of the design can be enhanced by adding power-up initialization circuitry for all sequential components.

The task of test pattern generation and fault simulation is proportional to the number of logic gates (n) to the third power (n3). Significant savings in testing costs can be achieved by partioning the design into smaller subsystems.

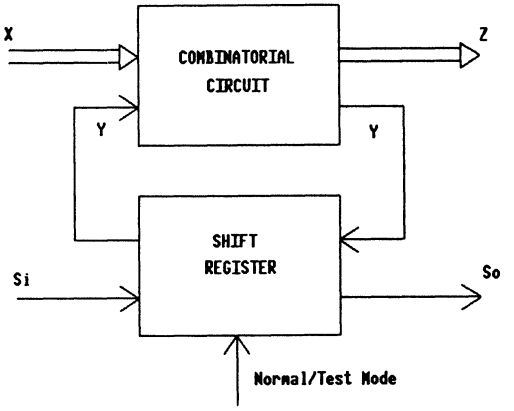
Various structured techniques can be implemented to enhance testability. Most of these are based on the "shift register" method, which involves serially connecting all memory elements in the circuit and using them as inputs for testing purposes. Figure 12A illustrates a generalized sequential circuit model under normal operation. Figure 12B illustrates the connection of the flip-flops into a register by

means of external test mode control using the shift register approach. This configuration enhances controlability and observability of all interanl memory elements through the scan-in (Si) and scan-out (So) lines. Amont the commonly used shift register approaches are the level-sensitive scan design (LSSD), scan/set logic, random access scan, and scan path techniques.

In the scan path method (figure 13), for example, the basic concept involves scanning in the test input and scanning out the test results. The storage element consists of two D-type master/slave flip-flowps with related gates and two clocks (C1, C2) that operate in an exclusive mode. The test input vectors are applied to the primary inputs and internal memory elements. This method reduces test generation time by almost one order of magnitude.

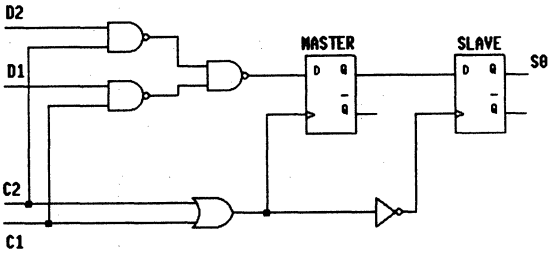


A. GENERALIZED SEQUENTIAL CIRCUIT

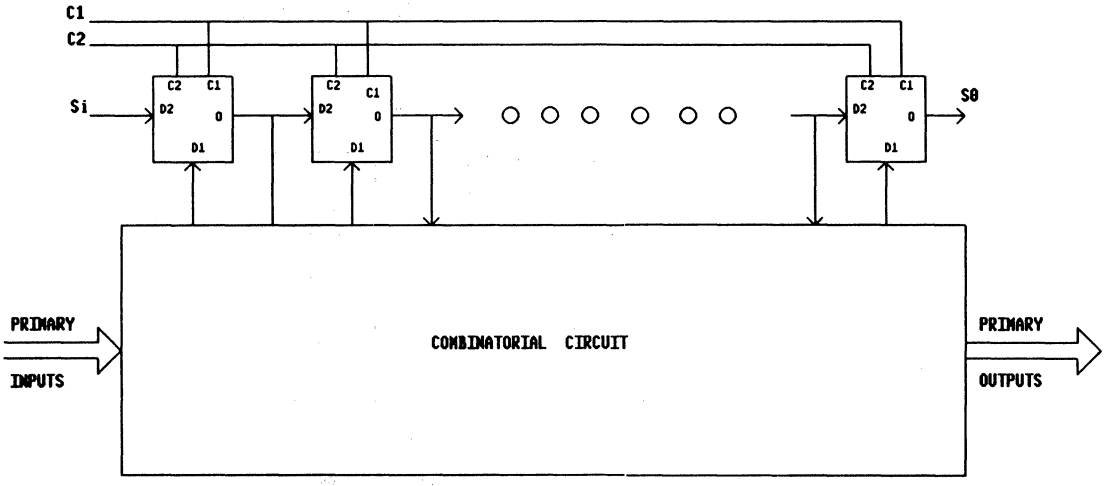


B. SHIFT REGISTER CONFIGURATION

FIG. 12 USE OF SEQUENTIAL CIRCUIT AS SHIFT REGISTER



A. BASIC STORAGE ELEMENT



B. SCAN PATH IMPLEMENTATION

FIG. 13 SCAN PATH METHOD

The GATE ARRAY DEVELOPMENT CYCLE

Selecting Array Size and Packaging

Before the actual gate array design activity begins, the array size and package type best suited to the application should be known. The steps involved in making these determinations are:

1. Select the function to be implemented and perform system partitioning, excluding those functions that are not suitable for implementing in gate arrays.

2. If the design is new, define it using VTI's CMOS library. If the design exists in a TTL form, perform TTL-to-CMOS logic conversion and minimize logic requirements by eliminating unused functions.

3. Analyze fan-out requirements, paying special attention to clock lines and critical nets. If necessary, add buffers to drive the internal logic.

4. Perform critical path analysis by using characterization data available for each macro. If necessary, add buffers and parallel gates, or redesign the logic to meet the desired specifications.

5. Specify TTL, CMOS and other input levels. Define the amount of drive for each output and determine the number of peripheral cells and output pads required.

6. Calculate the number of gates required for the design. Also add the number of inputs, outputs, transceivers and test pins to determine the total number of pads required. In selecting a VGC Series array to fit the design, typical gate utilization of the array should be set at approximately 80% with maximum pad usage.

7. Based on the total number of pads and level of screening, select a package type. VTI offers a wide selection of packages for its gate array family (table 7).

TABLE VII. VTI-VGC SERIES GATE ARRAYS PACKAGING MATRIX

	ARRAY PADS LEADS	VGC0500 44	VGC0900 72	VGC1200 84	VGC1900 100	VGC2400 120	VGC3200 132	VGC4000 144	VGC6000 172
CDIP	24	X	X	X					
Ceramic	28	X	X	X	X	X			
	40	X	X	X	X	X			
	48	X	X	X	X	X			
PDIP	24	X	X	X					
Plastic	28	X	X	X	X	X			
Dip	40	X	X	X	X	X			
	48	X	X	X	X	X			
LLCC	44	X	X	X	X	X			
Leadless	68	X	X	X	X	X	X	X	X
Ceramic	84	X	X	X	X	X	X	X	X
Chip Carrier									
PLCC	44	X	X	X	X	X	X		
Plastic	68		X	X	X	X	X	X	
Leadless	84			X	X	X	X	X	
Chip Carrier									
LDCC	44	X	X	X	X	X			
Leaded	68		X	X	X	X	X	X	X
Ceramic	84			X	X	X	X	X	X
Chip Carrier									
CPGA	68			X	X	X	X		
Ceramic	84			X	X	X	X	X	
Pin Grid	100				X	X	X	X	
Array	120					X	X	X	X
	132						X	X	X
	144							X	X
	172								X

TABLE VII. GATE ARRAY PACKAGING

Gate Array Design

When the logic, electrical specifications, type of array and package have been defined, CAD tools are used to complete the design. VTI offers a totally integrated, interactive CAD system to support its VGC Series CMOS gate array family. This system operates on VAX* 11/780 and Apollo workstations.

The typical gate array development flow (figure 14) begins with schematic capture of a design, from which a net list is generated. The net list is converted to the desired format and a design check performed. Logic simulation is then performed using estimated delays, with fault simulation optionally performed for testability analysis.

Following successful simulation, the circuit is placed and routed, either manually or automatically. Actual wire lengths are measured when routing is complete and the circuit is resimulated to verify the timing of critical nets. The final data base is then used to create a pattern generation tape and masks. A test program is developed using simulation vectors as test vectors.

The key program in the design cycle, and the responsibility for performing them, are:

1. Schematic capture (customer or VTI)
   A design may be entered using an interactive graphics system in which the user selects and places symbols representing library macros. Thisp program supports many hierarchical levels of logic and provides interfaces to various logic simulators. It allows net list extraction and checking. If desired, a net list may also be directly entered through an alphanumeric terminal.

2. Design pre-screening (customer or VTI)
   This program checks for compliance with design, rules and flags design violations. Among the checks are fan-in, fan-out and macro output configurations, which verifies that no logic design rules are violated.

3. Logic simulation (customer or VTI)
   The logic simulator is used for functional verification, timing validation and test pattern generation. It is a nine-value simulator that is capable of setting and inspecting the internal nodes. The logic simulator links the net list with a technology data base library containing the required macro logic-timing models; the customer provides input test vectors that are used to simulate the design.

*VAX is a trademark of Digital Equipment Corp.

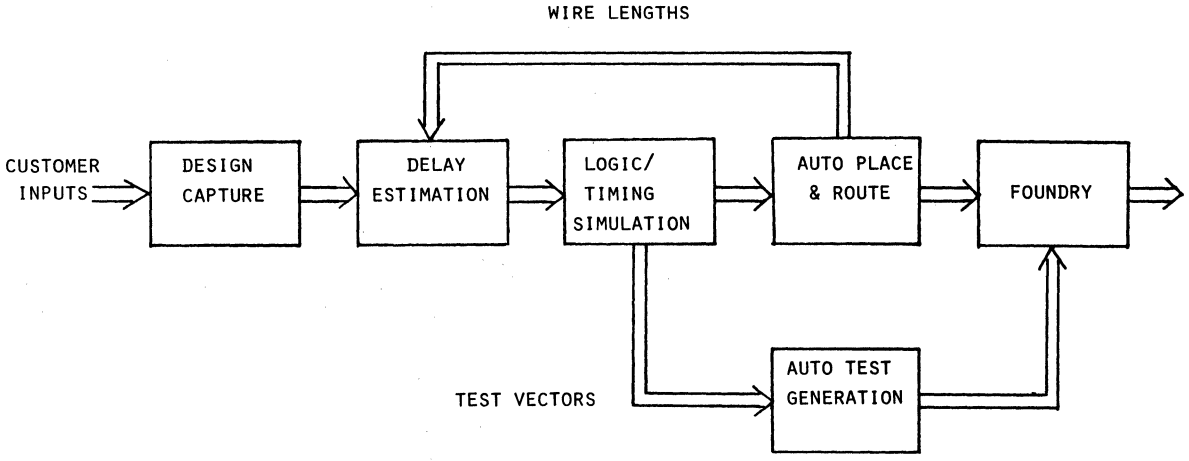


FIG. 14 TYPICAL GATE ARRAY DEVELOPMENT VGC SERIES

Simulation can be accomplished using either the highly accurate cell-based custom design simulator or a gate-level simulator.

4. Fault grading (customer or VTI)
   The sequence of input test vectors is graded by the fault simulator to determine fault coverage. This optional program checks for stuck-at-one and stuck-at-zero faults and determines the number of faults not detected by the test sequence. If the fault coverage is not satisfactory, additional test vectors should be included in the program.

5. Placement (VTI)
   When simulation is satisfactorily completed, the logic net list is transferred to the physical design secition of the CAD system, where physical data for the macros is linked to the net list. At this point, the user may specify manual macro placement on an interactive graphics terminal (particularly desirable if the part is a critical net) or may allow automatic placement software to perform the task. The metal interconnect length and macro congestion are displayed after placement and can be minimized by an iterative process. Critical macros are not moved by the automatic improvement system.

6. Routing (VTI)
   An automatic router interconnects the macros as specified in the net list. For overflow conditions and critical paths, an interactive graphics terminal may be used for manual routing. In the interactive mode, connections can only be made between the nodes specified in the net list.

7. Resimulation after routing (customer or VTI)
   After routing, the wire lengths and other physical attributes of the design are returned to the logic simulator. Logic is then resimulated using actual delay values. Changes in macro placement or routing may be required to meet the timing specifications, in which autorouting and simulation may not be repeated to verify the improvements.

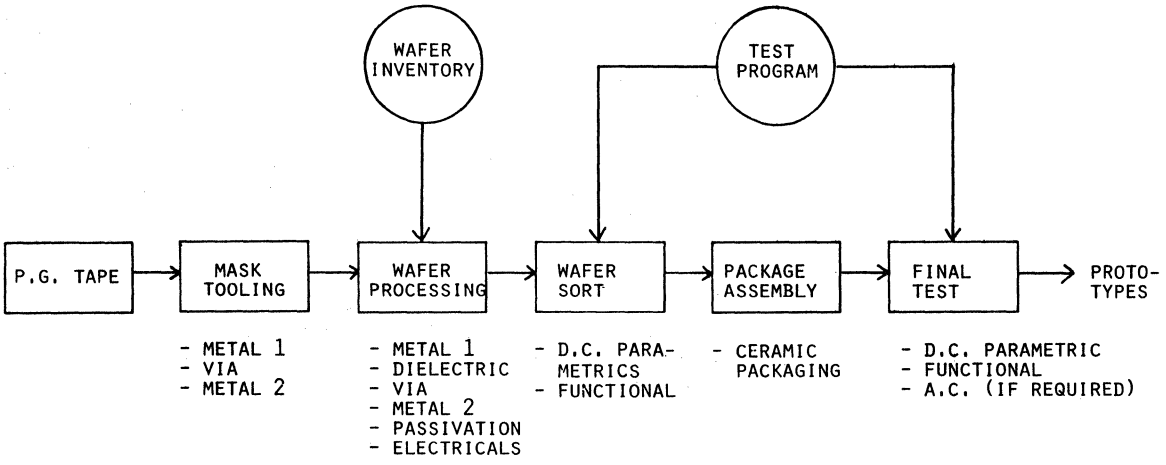


FIG. 15 GATE ARRAY MANUFACTURING FLOW

8. Pattern generation tape creation (VTI)
   After routing and simulation are successfully completed, the placement and routing data base is merged with the fixed interconnection data base to produce drawings for the two layers of metal and the via plane that will implement the design. Control tapes for electron-beam mask-making equipment are then generated.

9. Test program generation (customer or VTI)
   The final sequence of output test vectors is obtained after logic simulation and fault grading. The simulation inputs are converted into a format that is compatible with Fairchild's SENTRY automatic test system. This pattern is then used to test the chip.

10. Manufacturing (VTI)
    After the pattern generation tape is created, reticles for the metal 1, via and metal 2 layers are produced for a precision stepper photolithography manufacturing process (figure 16). The reticles are thoroughly inspected for dimensional accuracy of critical feature sizes and defect density.

    The required number of pre-qualified wafers are taken from inventory and processed through the metal 1 masking, intermetal dielectric and via masking, and metal 2 deposition and masking steps. The top protective passivation layer is then deposited and pad masked.

    Finished wafers are electrically tested for conformance with process and device characteristic standards; electrically acceptable wafers are sorted using the test program developed during the development cycle according to customer specifications. Good product dice are sent to assembly.

    To ensure quick turn-around of prototypes, the good dice are assembled in ceramic packages that are footprint-compatible with the specified high-volume production plastic packages. The assembled devices are then marked with customer option code number, product type and date code information.

    Final test of assembled parts is done using a temperature guard-banded test program at 25 degrees C. Final units thus meet 100% of the customer's dc and functional specifications. If required, selected critical ac measurements can also be made.

Ten final-tested prototype devices are shipped for customer approval. When the prototypes are approved, high-volume production begins.

Design Center Support

To ensure first-time project success, design and application support and high-quality design tools are available at every stage of the gate array development process from VTI's design centers. At the centers, customers have access to VTI CAD tools and to consulting and design support services that allow them to develop gate array or cell-based designs. These centers also offer regularly scheduled CMOS gate array and cell-based custom design training classes in which customers learn about design techniques and receive hands-on experience with VTI's CAD tools.

Design centers are currently in operation in San Jose, Santa Ana, Boston, Dallas, Chicago, and Munich.

Work-station Interface and Design Require-ments

In addition to the VAX-VMS, Apollo, ELXSI, Ridge and other computers, VTI also supports Mentor and Daisy workstations. Development is underway to support Valid, CAE and futurenet workstations. Customers wishing to simulate designs using other logic simulators should contact VTI sales representative.

Remote access to VTI CAD tools will also be provided to allow customers to develop gate arrays in their own facilities.

For any gate array development, a customer is expected to provide:

- A logic schematic
- Both DC and AC parametric test specifications
- A timing diagram
- Input test vectors for simulation
- Packaging and screen information.

Gate array development time can be improved significantly if the customer's inputs are comprehensive and of high quality. Optimal design cycle time therefore depends upon a good VTI/customer relationship, beginning at project inception.

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