WD57C65 Floppy Disk Subsystem Controller

FEATURES

- IBM* PS/2* and IBM PC XT* Compatible
- 100% Software Compatible with WD37C65B
- Integrated High Performance DPLL Data Separator
  - —<10E-9 industry standard error rates
  - —Data rates of 125, 250, 300, 500 Kbits/second
- Automatic Write Precompensation
  - —Defeat option
  - —Programmable values of 62,125,187, and 250 nanoseconds for standard data rates.
- On Chip Clock Generation
  - —Two TTL clock inputs (44 pin PLCC)
  - —One XTAL oscillator circuit for standard data rates.
- Enhanced Host Interface
  - —Read/write accesses compatible with an 8 or 12 MHz 286 microprocessor with 0 wait states
  - —Twenty LSTTL output drive capability
  - —TTL Schmitt trigger inputs (except Data Bus)
- Direct Floppy Disk Drive Interface - No Buffers Needed
  - —48mA sink output drivers
  - —Schmitt trigger input line receivers
  - —Supports three drives
- Complete Application Support for Systems Compatible with the IBM PS/2 and IBM PC XT.
  - —Register file on chip.
  - —PC XT mode provides required signal qualification to DMA channel
  - —BIOS compatible

DESCRIPTION

The WD57C65 Floppy Disk Subsystem Controller is an LSI device which incorporates all the functional blocks that typically make up a floppy disk subsystem controller, such as the formatter/controller, data separation, write precompensation, data rate selection, clock generation, and floppy drive interface drivers and receivers. Traditionally, data rate selection, drive selection, and motor control have been output ports of the host processor's architecture. The WD57C65 provides all the necessary status and control registers necessary to integrate all the functions of the floppy disk subsystem on a single chip.

The WD57C65 is designed for systems compatible with the IBM PS/2 and IBM PC XT and interfaces with three 5.25 or 3.5-inch floppy disk drives. It is available in a 40-pin, totally encapsulated plastic DIP or a 44-pin PLCC package.

The WD57C65 retains the core of the WD37C65B floppy disk controller so that the Micro-Sequencer is functionally equivalent and all commands will execute identically to ensure software compatibility. The Control State Machine is also functionally equivalent. The Micro-Sequencer and the Control State Machine operate at eight times the selected bit data rate in MFM and sixteen times the bit data rate in FM.

Figure 1 shows a block diagram of the WD57C65 "superchip".

Host Interface

The host interface provides the standard host access signals (eight control signals and eight data signals), but with enhanced timing. A detailed interface description appears in the Interface section of this document.

Floppy Drive Interface

The floppy drive interface provides data separation that has been designed to address high-performance error rates on floppy disk drives. It contains all the necessary logic to achieve 2nd order, type 2, phase-locked loop performance. Write precompensation is included along with the usual formatting, encoding/decoding, stepper motor control, and status sensing functions. A detailed interface description appears in the Interface section of this document.

Clock and Timing Generator

This logical block provides all the clocks needed by the WD57C65: Master Clock, Write Clock and Sampling Clock. Sampling Clock (SCLK) is the clock which drives the digital phase lock loop data separator that is used during data recovery. This clock frequency is always 32 times the selected data rate. The encoder logic uses the Write Clock (WCLK) to place MFM or FM on the serial Write Data stream to the disk. WCLK always has a frequency two times the selected data rate. Master clock (MCLK) is used by the microsequencer. MCLK and MCLK/ clock all latches in a two-phase scheme. One microinstruction cycle is four MCLK cycles. MCLK has a frequency equal to eight times the selected MFM data rate or 16 times the

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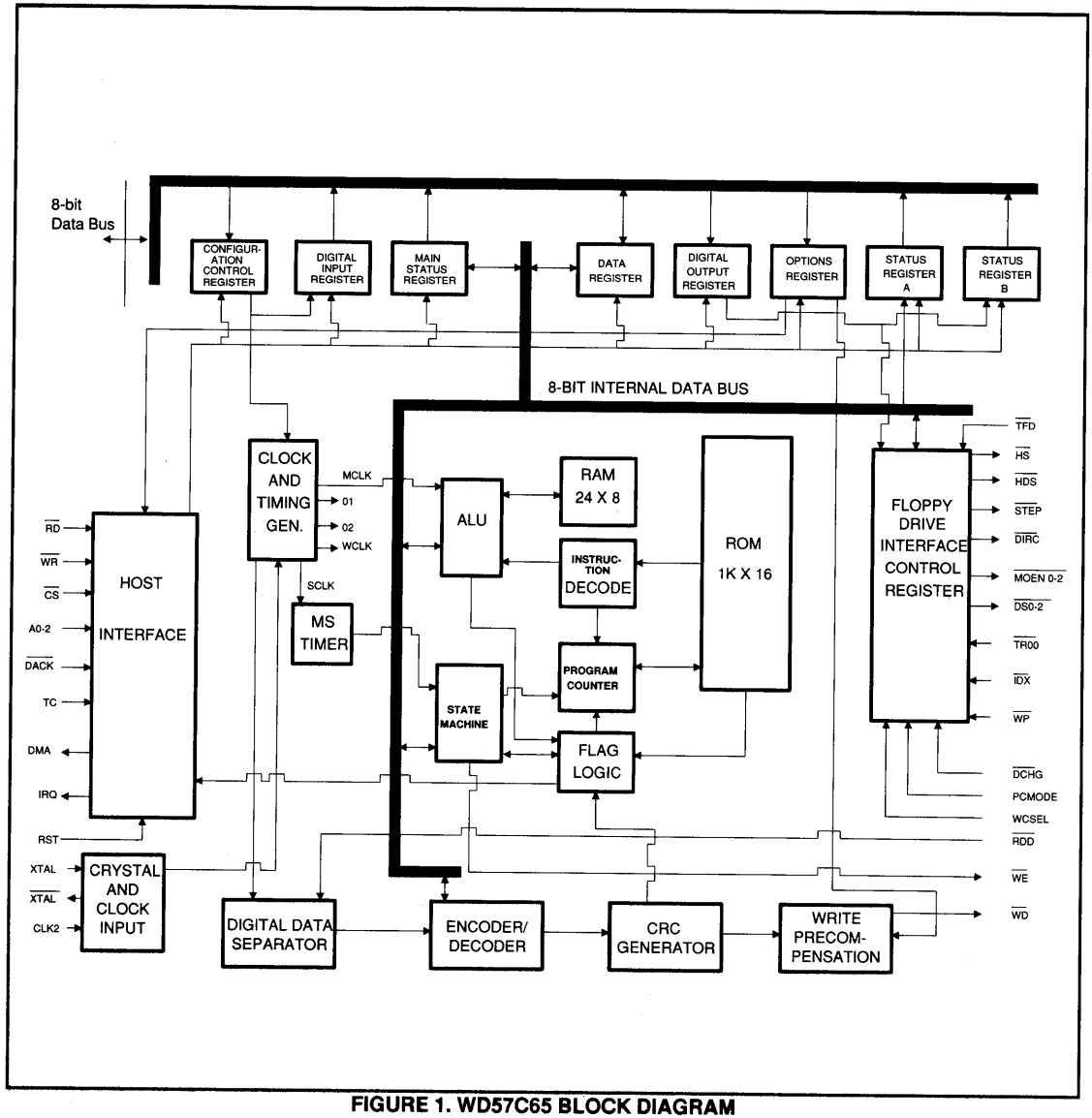
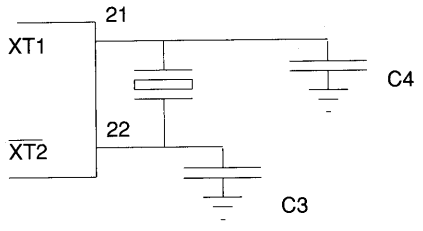


FIGURE 1. WD57C65 BLOCK DIAGRAM

TABLE 1. CLOCK DATA RATE

DATA RATE	CODE	SCLK	MCLK	WCLK
500 kb/s	MFM	16.0 MHz	4.0 MHz	1.0 MHz
250 kb/s	FM	8.0 MHz	4.0 MHz	500 KHz
250 kb/s	MFM	8.0 MHz	2.0 MHz	500 KHz
125 kb/s	FM	4.0 MHz	2.0 MHz	250 KHz
300 kb/s	MFM	9.6 MHz	2.4 MHz	600 KHz



16.0 MHz +/- 100 ppm
R series = 30 Ohms maximum
C shunt = 10 pf maximum
C3 = 47 pf 5% mica
C4 = 15 pf 5% mica

FIGURE 2. XTAL OSCILLATOR CIRCUITS FOR THE 44-PIN PLCC

FM data rate. Table 1 presents the Clock Data Rates. Figure 2 illustrates the XTAL oscillator circuits for the 44-pin PLCC configuration.

Crystal and Clock Input

An XTAL oscillator circuit (Figure 2) provides the necessary signal for internal timing when using the 44-pin PLCC package. There is one 16 Mhz oscillator on the WD57C65 which handles all standard data rates (500, 250, 125 Kbits/sec) and one TTL level clock input used for non-standard data rates; e.g. 300 Kbits/second used in PC AT* designs. **Note, however, that the WD57C65 does not support the IBM PC AT due to register address mapping conflicts.**

When using the 40-pin DIP, one TTL level clock input handles the standard data rates. The 40-pin DIP does not support non-standard rates.

Write Precompensation

The WD57C65 maintains the standard first level algorithm to determine when write precompensation should be applied. These EARLY and LATE signals are used internally to select the appropriate delay in the Write Data pulse stream. The encoded write data signal is synchronized to the 16 MHz clock, if this is the frequency on pin XTAL, and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has 25% duty cycle, i.e. one-fourth of the bit cell period, also equal to half of the WCLK period.

The Write Precompensation value is micro programmable. The precompensation values are

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defined by two bits in the Options Register (bit 2 and 3). After reset the default value for Precompensation is +/- two clocks and is valid for all tracks. There is no write precompensation value for FM. Precompensation can be disabled by the use of bit 2 in the Configuration Control Register for models compatible with the IBM PS/2 Model 30. For models compatible with the IBM PS/2 Models 50,60 and 80, bit 4 in the Options Register disables Write precompensation. The precompensation value is independent of track.

Data Separator

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase-locked loop performance. Figure 3 is a simplified block diagaram of the WD92C32. The bit jitter tolerance for the data separator is 60%, which guarantees an error rate of <10E-9.

WD57C65 Registers

The WD57C65 provides nine registers for status, control, option selection and buffering functions. These registers are described in detail in the Interface Description.

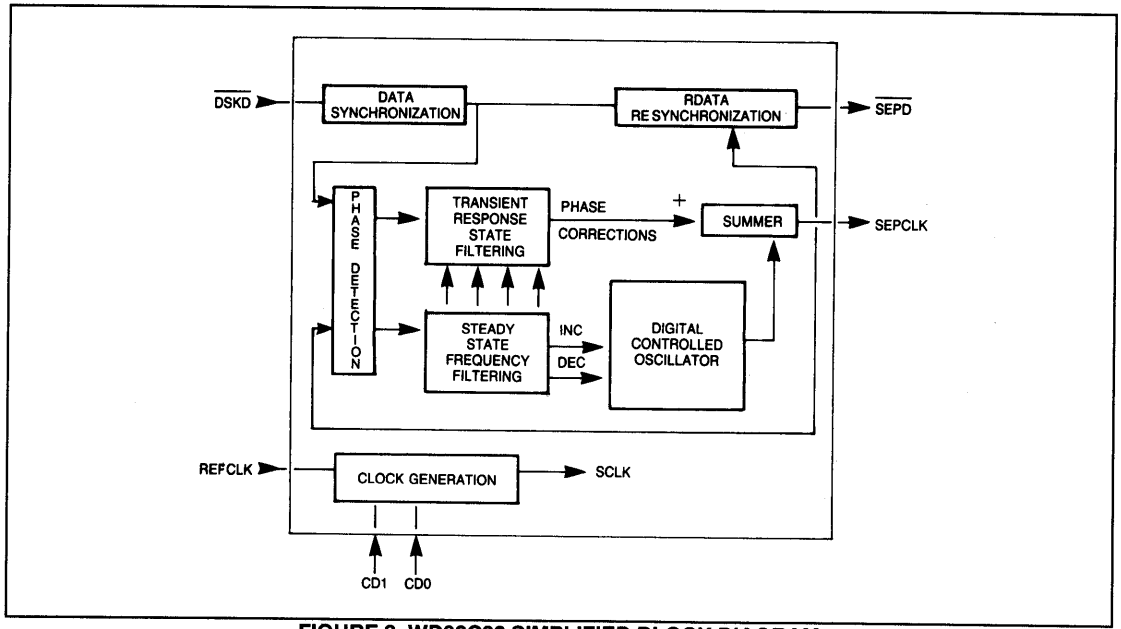

FIGURE 3. WD92C32 SIMPLIFIED BLOCK DIAGRAM

INTERFACE DESCRIPTION

Figures 4 and 5 show the pinouts of the floppy subsystem controllers for systems compatible with the IBM PS/2. Table 2 provides a pinout signal description of the WD57C65.

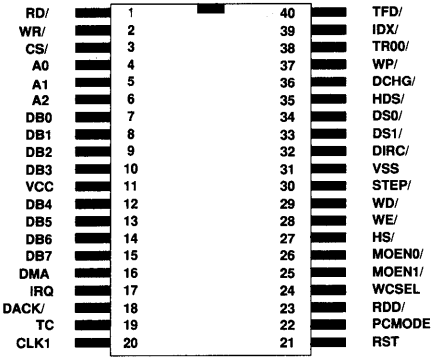

FIGURE 4. WD57C65 40-PIN DIP

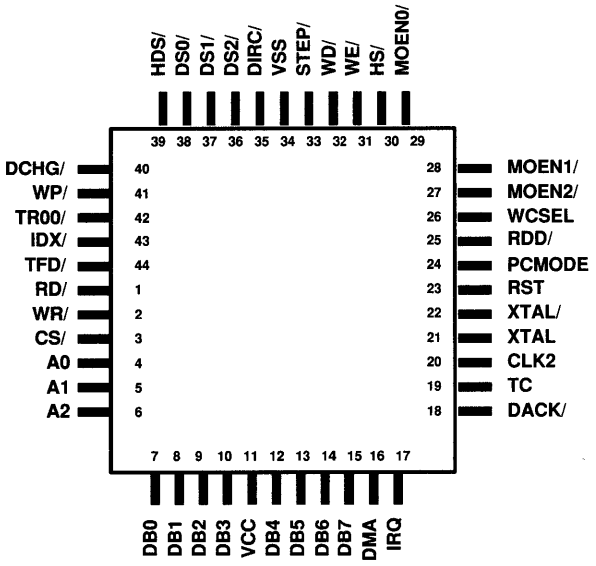

FIGURE 5. WD57C65 44-PIN PLCC

Table 2 below lists the DIP/PLCC pin numbers and the corresponding signal and signal function description. Note: For pin numbers separated by a "/", the first number is a DIP pin number. The number following the slash is the PLCC pin number.

TABLE 2. PINOUT DESCRIPTION

D/P PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
1	RD/	Read	I	Control signal for transfer of data or status onto the data bus by WD57C65.
2	WR/	Write	I	Control signal for latching data from the bus into WD57C65 buffer register. Also other registers of Write - only type.
3	CS/	Chip Select	I	Enables RD/ or WR/ operation from the host.
4-6	A0-2	Address	I	Address lines selecting data.
7-10,12-15	DB0-7	Data Bus	I/O	8 bit bi-directional tri-state data bus.
11	VCC			+5V Supply
16	DMA	Direct Memory-Access	O	DMA request for byte transfers of data. In a mode compatible with the IBM PC XT and IBM PS/2 Model 30, this pin is tri-stated, enabled by DMAEN signal from the Digital Output register. In modes compatible with the IBM PS/2 Models 50, 60 and 80, this internal signal, DMAEN, is always forced valid.
17	IRQ	Interrupt Request	O	Interrupt request indicating completion IRQ/ of command execution or data transfer requests (in non-DMA mode). In modes compatible with the IBM PC XT and PS/2 model 30, this pin is tri-stated, enabled by DMAEN signal from the Digital Output register and is active high. It is open drain for modes compatible with the IBM PS/2 Models 50, 60 and 80, requires external pull-up, and is active low.
18	DACK/	DMA Acknowledge	I	Used by DMA controller to transfer data from WD57C65 onto the bus. Logical equivalent to CS/ and Addr=101 . In a mode compatible with the IBM PC XT and IBM PS/2 Model 30, this signal is qualified by DMAEN from the Digital Output register. In modes compatible with the IBM PS/2 Model 50, 60 and 80, this signal is not qualified.
19	TC	Terminal Count	I	This signal indicates to WD57C65 that TC/ data transfer is complete. TC is always qualified by DACK/. In the IBM PC XT and IBM PS/2 Model 30, qualification by DACK/ requires Digital Output Register signal DMAEN to be logically true. In the IBM PS/2 models 50, 60 and 80, TC is active low, and the internal signal DMAEN is always forced valid.
20/NA	CLK1	Clock 1	I	16 MHz TTL level clock input used to generate all internal timings for standard data rates. Non-standard data rates (300 Kbits/second) are not supported by the 40-pin dip package.

TABLE 2. PINOUT DESCRIPTION (CONTINUED)

D/P PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
NA/20	CLK2	Clock 2	I	TTL level clock input used for non-standard data rates, such as 300 Kbits/second in an IBM PC AT application. Must be 32 times MFM data rate; i.e. 9.6 MHz for 300 Kbits/second, and can only be selected from the Control Register. It has an internal pull-up.
NA/21	XTAL	XTAL	I	Oscillator input requiring 16MHz crystal. This oscillator is used for all standard data rates. It may be driven with a TTL level signal.
NA/22	XTAL/	XTAL	O	XTAL oscillator drive output fro 44-pin PLCC.
21/23	RST	Reset	I	Resets controller, placing micro-sequencer in idle. Resets device outputs.
22/24	PCMODE	PC MODE	I	PC application mode select. Selects a mode compatible with the IBM's PC XT and IBM PS/2 Model 30, or a mode compatible with the IBM PS/2 Models 50, 60 and 80.
23/25	RDD/	Read Disk Data	I	This Schmitt Trigger (ST) input senses the serial bit stream from the disk drive. The falling edge of each pulse represents a flux transition of the encoded data.
24/26	WCSEL	Write Control Select	I	Allows direct interface to both 5.25 and 3.5-inch floppy disk drives. For logical function see Table 3.
NA/27	MOEN2/	Floppy Drive Motor Enable	O	This high current driver (HCD) output, when active low, enables disk drive #2. This signal comes from Digital Output Register.
25/28	MOEN1/	Floppy Drive Motor Enable	O	This HCD output, when active low, enables disk drive #1. This signal comes from Digital Output Register.
26/29	MOEN0/	Floppy Drive Motor Enable	O	This HCD output, when active low, enables disk drive #0. This signal comes from Digital Output Register
27/30	HS/	Head Select	O	This HCD output selects the head, or side of the floppy disk that is being read or written. Logic 1 = side 0, logic 0 = side 1.
28/31	WE/	Write Enable	O	This HCD output goes active low just prior to writing on the diskette. This allows current to flow through the write head.
29/32	WD/	Write Data	O	This HCD output is write data. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
30/33	STEP/	Step	O	This HCD output issues an active low pulse for each track-to-track movement of the head. The state of the Direction signal at the trailing edge of the STEP pulse determines the direction of the head motion.

TABLE 2. PINOUT DESCRIPTION (CONTINUED)

D/P PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
31/34	VSS			Ground
32/35	DIRC/	Direction Control	O	This HCD output determines the direction of the head stepper motor. Logic 1 = outward motion, logic 0 = inward motion.
35/39	HDS/	High Density Select	O	This HCD output indicates to the drive the appropriate write current level to use for the data rate and media density currently being used. The active logic level used to select between High Density vs Double Density is determined by the WCSEL input pin.
34/38	DS0/	Drive Select 0	O	This HCD output, when active low, enables Drive O's interface. This signal comes from the Digital Output register. This signal is qualified by MOEN0/ active low.
33/37	DS1/	Drive Select 1	O	This HCD output, when active low, enables Drive 1's interface. This signal comes from the Digital Input register. This signal is qualified by MOEN1/ active low.
NA/36	DS2/	Drive Select 2	O	This HCD output, when active low, enables Drive 2's interface. This signal comes from the Digital input Digital Input register. This signal is qualified by MOEN2/ active low.
36/40	DCHG/	Diskette Change	I	This is a Schmitt Trigger input which is an active low signal when the disk drive door is open or if the diskette has possibly changed since last drive selection. This status is reflected in the Digital Input Register.
37/41	WP/	Write Protected	I	This Schmitt Trigger input indicates status from the disk drive, going active low when a diskette is Write Protected.
38/42	TR00/	Track 00	I	This Schmitt Trigger input indicates status from the drive, going active low when the head is positioned over the outermost track, track 00.
39/43	IDX/	Index	I	This Schmitt Trigger input indicates status from the drive, going active low when the head is positioned over the beginning of a track marked by an index hole.
40/44	TFD/	Twp Floppy Drive	I	This Schmitt Trigger input indicates status from the drive, going active low when a second drive is installed.

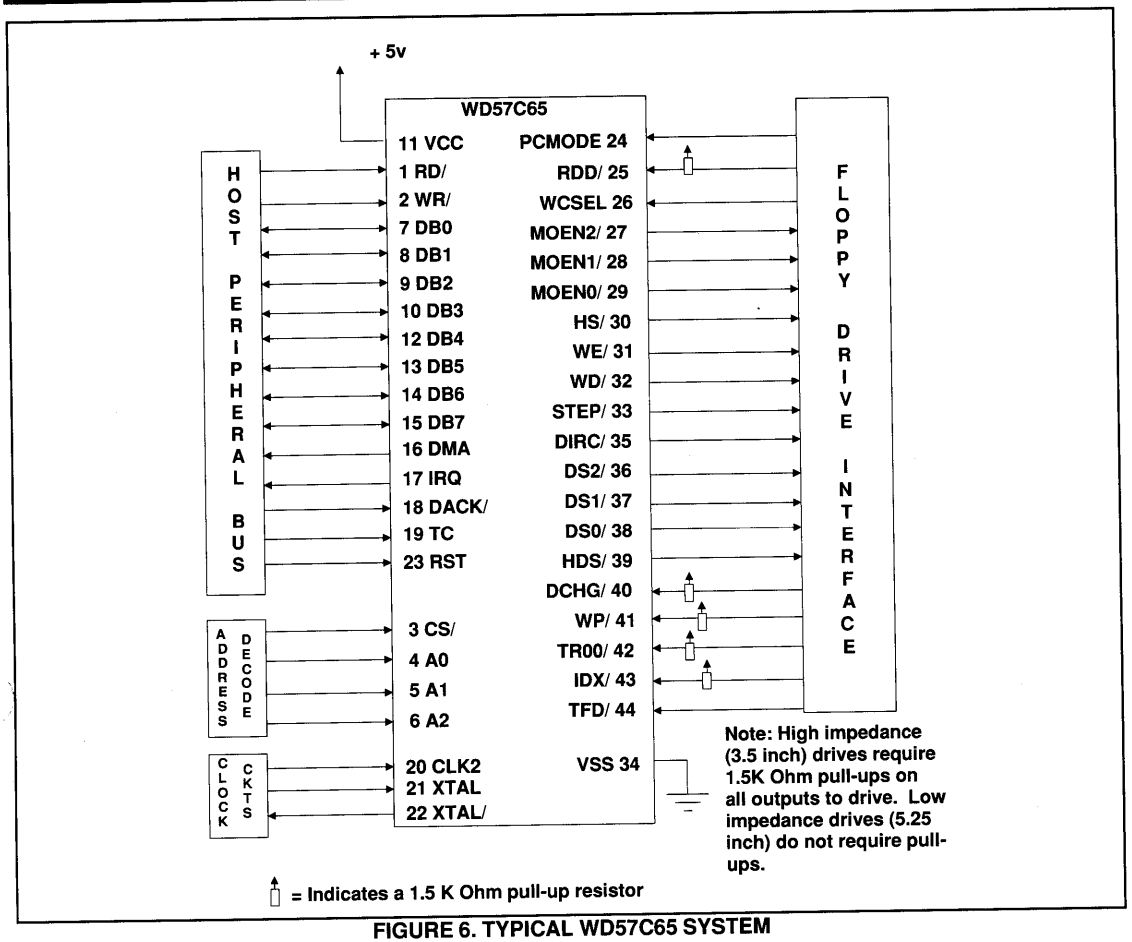

FIGURE 6. TYPICAL WD57C65 SYSTEM

Figure 6 illustrates a typical interface system for the WD57C65.

Floppy Drive Interface

The WD57C65 Floppy Drive Interface provides different options than its predecessor, the WD37C65B. Most notably, it supports three drives rather than just two. A new input signal, Write Control Select (WCSEL) allows interfacing with 5.25 and 3.5 inch floppy drives. WCSEL and the selected data rate determine the correct logical level on the High Density Select (HDS/) output pin. If WCSEL = 0, HDS/ = CR0/. If WCSEL =1, HDS/ = CR1. Refer to Table 3, HDS Truth Table.

PCMODE input signal selects either IBM PC XT-PS/2 30 mode or the PS/2 50, 60, and 80 mode. WD57C65 does not support IBM AT systems.

Since PS/2 compatible systems require a Two Floppy Drive (TFD/) pin, the WD57C65 provides TFD/ and has dropped the PCVAL pin used for precompensation in the WD37C65B predecessor. Write precompensation values are determined by bits 2 and 3 in the Options Register. The reset default value for write precompensation is +/- 2 clocks.

TABLE 3. HDS TRUTH TABLE

DATA RATE AND CODE	WCSEL	HDS	DESCRIPTION
500 K MFM or 250 K FM	0 1	1 0	5.25" High Density / 1.2 MByte FDD 3.5" High Density / 1.44 MByte FDD
300 K MFM	0 1	0 0	5.25" Double Density / 1.2 MByte FDD Not Defined
250 K MFM or 125 K FM	0 1	1 1	5.25" Double Density / 360 KByte FDD 3.5" Double Density / 720 KByte FDD or 1.44 MByte FDD
125 K FM	0 1	0 1	5.25" Single Density / 360 KByte FDD 3.5" Single Density / 720 KByte FDD

Host Interface

Host Microprocessor Peripheral Bus provides eight control signals and eight data signals. In the XT and PS2 30 mode, IRQ and DMA Request are tri-stated and enabled by DMAEN, which is internally provided by the Digital Output Register. In PS/2 50, 60 and 80 mode, IRQ is open drain, active low, requires external pull-up, and DMAEN is always forced valid. The data bus, DMA, and IRQ outputs are designed to handle 20 LSTTL loading. Inputs, except the data bus, are Schmitt trigger receivers and can be hooked up to a bus or backplane without any additional buffering.

During the command or result phases, the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU should wait for 12 microseconds before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a "0" and "1" state, respectively, before each byte of the command word may be written into the WD57C65. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the WD57C65. During the result phase, Bits D6 and D7 in the Main Status Register must both be "1's" before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the WD57C65 is required only in the command and result phases, and not during the execution phase. Note also that DB6 and DB7 in the MSR can be polled instead of waiting 12 microseconds.

During the execution phase, the Main Status Register need not be read. If the WD57C65 is in the non-DMA mode, then receipt of each data byte (WD57C65 is reading data from the FDD) is indicated by an interrupt signal on pin 17 (IRQ=1). The generation of a Read signal (RD=0) will clear the interrupt as well as output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13 microseconds for the MFM mode and 27 microseconds for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the interrupt signal. If a Write command is in process, then the WR signal performs the reset to the Interrupt signal.

All timing mentioned above is double for mini-floppy (5.25-inch) data rates.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the WD57C65 is in the DMA mode, no interrupt signals are generated during the execution phase. The WD57C65

TABLE 4. ADDRESS REGISTER MAP

ADDRESS MAP	CS/	A2	A1	A0	R/W/RW
Status Register A	0	0	0	0	Read only
Status Register B	0	0	0	1	Read only
Digital Output Register	0	0	1	0	Write only
Not Defined	0	0	1	1	Not defined
Main Status Register	0	1	0	0	Read only
Main Data Register	0	1	0	1	Read/Write
Options Register	0	1	1	0	Write only
Digital Input Register	0	1	1	1	Read only
Configuration Control Register	0	1	1	1	Write only

generates DMA requests when each byte of data is available. The DMA controller responds to this request with both DACK/ = 0 (DMA Acknowledge) and a RD/ =0 (Read signal). When the DMA Acknowledge signal goes low (DACK/ = 0), then the DMA Request is cleared (DMA = 0). If a Write Command has been issued, then a WR signal will appear instead of RD. After the execution phase has been completed (Terminal Count has occurred or the EOT sector is read or written), then an interrupt occurs (IRQ = 1). This signifies the beginning of the Result phase. When the first byte of data is read during the result phase, the Interrupt automatically clears (IRQ = 0).

The RD/ or WR/ signals should be asserted while DACK/ is true. The CS/ signal is used in conjunction with RD/ and WR/ as a gating function during programmed I/O operations. CS has no effect during DMA operations. If the non-DMA mode is chosen, the DACK/ signal should be pulled up to VCC. During the result phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has several bytes of data in the result phase. All seven bytes must be read in order to successfully complete the Read Data command. The WD57C65 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase. The WD57C65 contains an address decoder for the register file on the host interface side. The address mapping is shown in Table 4. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the result phase and may be read only after completing a command. The particular command that has been executed determines how many of the status registers will be read.

The bytes of data which are sent to the WD57C65 during the command phase, and are read out of the WD57C65 in the result phase, must occur in the order shown in the Command Table. The command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the command or result phases is allowed. After the last byte of data in the command phase is sent to the WD57C65, the execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the WD57C65 is ready for a new command.

Configuration Control Register

The Configuration Control Register provides support logic that latches the three least significant bits of the data bus upon receiving CS/ Address = 111 and WR/. These bits select the desired data rate, which in turn controls the internal clock generation. Clock switchover is internally "deglitched," allowing continuous operation after changing data rates. If the Configuration Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 32 times the desired MFM data rate up to a maximum frequency of 16 MHz. This implies a maximum data rate of 500 kbits/second, unless the Configuration Control Register is used.

Switching this clock must be "glitchless" or the device will need to be reset. Tables 5 and 6 show the Configuration Control Register.

TABLE 5. CONFIGURATION CONTROL REGISTER FOR SYSTEMS COMPATIBLE WITH IBM PS/2 50, 60 & 80

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Data Rate	F/F	0	None (1)
1	Data Rate	F/F	0	None (1)
2	Reserved	None	N/A	None
3	Reserved	None	N/A	None
4	Reserved	None	N/A	None
5	Reserved	None	N/A	None
6	Reserved	None	N/A	None
7	Reserved	None	N/A	None

Note 1: 250K data rate is selected if bits 0 and 1 are anything but "0,0" in models compatible with the IBM PS/2 50, 60 and 80.

TABLE 6. CONFIGURATION CONTROL REGISTER FOR SYSTEMS COMPATIBLE WITH IBM PC XT & PS/2 30.

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Data Rate	F/F	0	None (3)
1	Data Rate	F/F	0	None
2	No Write Precompensation	F/F	0	None
3	Reserved	None	N/A	None
4	Reserved	None	N/A	None
5	Reserved	None	N/A	None
6	Reserved	None	N/A	None
7	Reserved	None	N/A	None

Note 3: Undefined in applications compatible with IBM PS/2 30, but supported by the 57C65.

TABLE 7. DATA RATE SELECTION

CR1	CR0	DATA RATE	COMMENTS
0	0	500 K	MFM, RST default (Defined in both modes)
0	0	250 K	FM (Undefined in PC applications)
0	1	300 K	MFM (Defined in applications compatible with IBM PC/AT)
1	0	250 K	MFM (Defined in modes compatible with PC XT and PS/2)
1	0	125 K	FM (Undefined in PC applications)
1	1	125 K	FM (Undefined in PC applications)

Bit 2 (CR2) is undefined in the IBM PS/2 50, 60 and 80 modes, and is set to a "1".

Bit 4 (CR4) enables (0) or disables (1) write precompensation in the IBM PS/2 50, 60 and 80 mode.

In the IBM PC XT and PS/2 30 mode, CR2 enables (0) or disables (1) write precompensation

Main Status Register

The Main Status Register is an eight-bit register that contains the status information of the FDC, and may be accessed at any time. Only the Main Status Register may be read and used to facilitate the transfer of data between the processor and WD57C65. The DIO and RQM bits in the Main Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD or WR during a command or result phase and DIO and RQM getting set is 12 microseconds if 500 kbits/second MFM data rate is selected. (If 250 kbits/second MFM is selected the delay is 24 microseconds.) For this reason, every time the Main Status Register is read, the CPU should wait 12 microseconds. The maximum time from the trailing edge of the last RD/ in the result phase to when DB4 (FDC busy) goes low is 12 microseconds. Tables 8 through 12 show the bits in the Master Status Register and Status Registers 0 through 3.

TABLE 8. MAIN STATUS REGISTER BITS

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
DB0	FDD 0 BUSY	D0B	FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB1	FDD 1 BUSY	D1B	FDD number 1 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB2	FDD 2 BUSY	D2B	FDD number 2 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB3	FDD 3 BUSY	D3B	FDD number 3 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB4	FDC BUSY	CB	A READ or WRITE command is in progress. FDC will not accept any other command.
DB5	EXECUTION MODE	EXM	This bit is set only during Execution phase in non-DMA mode. When DB5 goes low Execution phase has ended and Results Phase has started. It operates only during non-DMA mode of operation.
DB6	DATA INPUT	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO=1, then transfer is from Data Register to the processor. If DIO=0, then transfer is from the processor to Data Register.
DB7	REQUEST FOR MASTER	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

TABLE 9. STATUS REGISTER 0 BITS

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
D7	INTERRUPT CODE	IC	D7=0 and D6=0. Normal termination of command was completed and properly executed. D7=0 and D6=1. Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
D6			D7=1 and D6=0. Invalid command issue, (IC). Command which was issued was never started.
D5	SEEK END	SE	When the FDC completes the SEEK command, this flag is set to 1 (high).
†D4	EQUIPMENT CHECK	EC	If the Track 0 signal fails to occur after 255 step pulses (Recalibrate Command), then this flag is set.
†D3	NOT READY	NR	Since drive Ready is always presumed true, this will always be a logic 0.
D2	HEAD SELECT	HS	This flag is used to indicate the state of the head at interrupt.
D1	UNIT SELECT 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
D0	UNIT SELECT 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.

TABLE 10. STATUS REGISTER 1 BITS

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
D7	END OF CYLINDER	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D6			Not used. This bit is always 0 (low).
D5	DATA ERROR	DE	When the FDC detects a *CRC error in either the ID field or the data field, this flag is set.
D4	OVERRUN	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D3			Not used. This bit is always 0 (low).
D2	NO DATA	ND	During execution of READ DATA, WRITE DELETED DATA, or SCAN command, if the FDC cannot find the sector specified in the **IDR Register, this flag is set. During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set. During execution of the READ A TRACK command, if the starting sector cannot be found, then this flag is set.
D1	NOT WRITEABLE	NW	During execution of WRITE DATA, WRITE DELETED DATA or FORMAT A TRACK commands, if the FDC detects a $\overline{WP}$ signal from the FDD, then this flag is set.
D0	MISSING ADDRESS MARK	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.

TABLE 11. STATUS REGISTER 2 BITS

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
D7			Not Used. This bit is always 0 (low).
D6	CONTROL MARK	CM	During execution of the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D5	DATA ERROR	DD	If the FDC detects a CRC error in the data field, then this flag is set.
D4	WRONG CYLINDER	WC	This bit is related to the ND bit, and when the contents of ***C on the medium is different from that stored in the IDR, this flag is set.
D3	SCAN EQUAL	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D2	SCAN NOT	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D1	BAD CYLINDER	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set.
D0	MISSING ADDRESS MARK IN DATA FIELD	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

TABLE 12. STATUS REGISTER 3 BITS

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
†D7	–	–	Not used. Will always be logic 0.
D6	$\overline{\text{WRITE PROTECTED}}$	$\overline{\text{WP}}$	This bit is used to indicate the status of the $\overline{\text{WRITE PROTECTED}}$ signal from the FDD.
†D5	READY	RY	This bit will always be a logic 1. Drive is presumed to be ready.
D4	TRACK 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
†D3	$\overline{\text{WRITE PROTECTED}}$	$\overline{\text{WP}}$	This bit is used to indicate the status of the $\overline{\text{WRITE PROTECTED}}$ signal from the FDD.
D2	HEAD SELECT	HS	This bit is used to indicate the status of the Side Select signal to the FDD.
D1	UNIT SELECT 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D0	UNIT SELECT 2	US0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

Status Register A (CS/ = 0 and Address = 000 - Read Only)

TABLE 13. STATUS REGISTER A FOR SYSTEMS COMPATIBLE WITH IBM PS/2 50, 60 AND 80

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	+ Direction	TSB	N/A	None
1	- Write Protection	TSB	N/A	None
2	- Index	TSB	N/A	None
3	+ Head 1 Select	TSB	N/A	None
4	- Track 0	TSB	N/A	None
5	+ Step	TSB	N/A	None
6	- 2nd Drive Installed	TSB	N/A	None
7	Interrupt	TSB	N/A	None

TABLE 14. STATUS REGISTER A FOR SYSTEMS COMPATIBLE WITH THE IBM PC XT AND IBM PS/2 30

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	- Direction	TSB	N/A	None
1	+ Write Protect	TSB	N/A	None
2	+ Index	TSB	N/A	None
3	- Head 1 Select	TSB	N/A	None
4	+Track 0	TSB	N/A	None
5	+ Step	SR F/F	0	STEP (1)
6	+ DRQ	TSB	N/A	None
7	Interrupt	TSB	N/A	None

Note 1: Not synchronized to unknown PAL clocks in systems compatible with the IBM PS2. Reset is forced to logic "0" for test purposes. Also resets to logic "0" when address 3F7 is read and STEP causes a set condition.

TSB = Tri-state buffer

SR F/F = Set Reset Flip Flop

If Storage Element is "none", Reset Condition reflects fixed logic state.

Status Register B (CS/ = 0 and Address = 001 - Read Only)

TABLE 15. STATUS REGISTER B FOR SYSTEMS COMPATIBLE WITH THE IBM PS/2 50, 60, AND 80.

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Motor Enable 0	TSB	N/A	None
1	Motor Enable 1	TSB	N/A	None
2	Write Enable	TSB	N/A	None
3	Read Data	Toggle F/F	0	RDD/ (1)
4	Write Data	Toggle F/F	0	WD/ (2)
5	Drive Select	TSB	N/A	None (3)
6	Reserved	Unused TSB	1	None
7	Reserved	Unused TSB	1	None

Note 1: Not synchronized to unknown PAL clocks in systems compatible with the IBM PS/2 50, 60 and 80. Reset is forced to logic "0" for test purposes.

Note 2: Not synchronized to unknown PAL clocks in systems compatible with the IBM PS/2 50, 60 and 80. Reset is forced to logic "0" for test purposes. This "WD" clock is an internal signal not qualified by WE/ signal.

Note 3: This status reflects Digital Output Register bit 0 only.

TABLE 16. STATUS REGISTER B FOR SYSTEMS COMPATIBLE WITH IBM PC XT AND IBM PS/2 MODEL 30

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	- Drive Select 2	TSB	N/A	None (5)
1	- Drive Select 3	TSB	N/A	None (5)
2	Write Enable	SR F/F	0	WE/ (4)
3	Read Data	SR F/F	0	RDD/ (4)
4	Write Data	SR F/F	0	WD/ (4)
5	- Drive Select 0	TSB	N/A	None (5)
6	- Drive Select 1	TSB	N/A	None (5)
7	Reserved	Unused TSB	0	None

Note 4: Not synchronized to unknown PAL clocks in systems compatible with IBM PS/2 30. Reset is forced to logic "0" for test purposes and when reading address 357. WE/, RDD/ and WD/ are internal signals and cause a set condition.

Note 5: Drive select signals (0-3) are qualified by Motor Enable signals (0-3)

TSB = Tri-state Buffer

SR F/F = Set Reset Flip Flop.

If Storage Element is none, Reset Condition reflects fixed logic state.

Data Register

The eight-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The relationship between the Master Status Register and the Data Register and the signals RD/, WR/, CS/ and A0-A2 are shown in Table 17.

TABLE 17. MASTER STATUS AND DATA REGISTERS RELATIONSHIP

A0	A1	A2	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	FUNCTION
1	0	0	0	0	1	Read Main Status Register
1	0	1	0	0	1	Read from Data Register
1	0	1	0	1	0	Write into Data Register

Digital Output Register (CS/=0 and Address = 010 - Write Only)

The Digital Output Register (DOR) provides support logic that latches the data bus upon receiving CS/, Address = 010 and WR/. This register replaces the typical latched port seen in floppy subsystems used to control disk drive spindle motors and select drives. Table 18 illustrates the bit decode (bits 0 and 1 of the DOR) used to select drives 0 through 2. Table 19 provides a bit descsription of the contents of the DOR.

TABLE 18. BIT DECODE FOR DRIVE SELECT

DSEL1	DSEL0	DRIVE
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Not Supported

TABLE 19. DIGITAL OUTPUT REGISTER

BIT	SIGNAL	FUNCTION
DOR0	DSEL0	Drive Select. If decode select is "0" and MOEN0/ is active low, then DS0/ is selected. If decode select is "1" and MOEN1/ is active low, then DS1/ is selected. If decode select is "2" and MOEN2/ is active low, then DS2/ is selected if in a mode compatible with the IBM PC XT and IBM PS/2 Model 30. Although DS2/ is undefined in applications compatible with the IBM PS/2 50, 60 and 80, the WD57C65 supports DS2/ in both modes.
DOR1	DSEL1	Drive Select
DOR2	SRST/	Soft Reset, active low
DOR3	DMAEN	DMA Enable. Active in a mode compatible with the IBM PC XT and IBM PS/2 Model 30, qualifies DMA and IRQ outputs and also DACK/input. In modes compatible with the IBM PS/2 models 50, 60 and 80 this internal signal is always valid.

BIT	SIGNAL	COMMENTS
DOR 4	MOEN0	Motor enable (Inverted output is MOEN0/)
DOR 5	MOEN1	Motor enable (Inverted output is MOEN1/)
DOR6	MOEN2	Motor enable (Inverted output is MOEN2/) Undefined in applications compatible with the IBM PS/2 50, 60 and 80, but supported by the WD57C65 in both modes.)
DOR7		Reserved

TABLE 20. DIGITAL OUTPUT REGISTER FOR SYSTEMS COMPATIBLE WITH IBM PS/2 50,60, AND 80

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Drive Select	F/F	0	None (1)
1	Drive Select	F/F	0	None (1)
2	- Reset	F/F	0	None
3	Reserved	Unused F/F	N/A	None
4	Motor 0	F/F	0	None
5	Motor 1	F/F	0	None
6	Motor 2	F/F	0	None (1)
7	Reserved	Unused F/F	N/A	None

Note 1: Although undefined in applications compatible with the IBM PS/2 50, 60 and 80, this signal is supported by the WD57C65.

TABLE 21. DIGITAL OUTPUT REGISTER FOR SYSTEMS COMPATIBLE WITH IBM PC XT AND IBM PS/2 30.

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Drive Select	F/F	0	None
1	Drive Select	F/F	0	None
2	- Reset	F/F	0	None
3	DMA and Interrupt Enable	F/F	0	None
4	Motor 0	F/F	0	None
5	Motor 1	F/F	0	None
6	Motor 2	F/F	0	None
7	Reserved	Unused F/F	N/A	None (2)

Note 2: This bit is defined as Motor Enable 3 in models compatible with the IBM PS/2 30, but WD57C65 does not support it.

TSB = Tri-state Buffer F/F = Flip Flop

If Storage Element is "none", Reset condition reflects fixed logic state.

Digital Input Register (CS/=0 and Address = 111 - Read only)

TABLE 22. DIGITAL INPUT REGISTER FOR SYSTEMS COMPATIBLE WITH THE IBM PS/2 50, 60 AND 80

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	- High Density Select	TSB	N/A	None
1	Reserved	Unused TSB	1	None
2	Reserved	Unused TSB	1	None
3	Reserved	Unused TSB	1	None
4	Reserved	Unused TSB	1	None
5	Reserved	Unused TSB	1	None
6	Reserved	Unused TSB	1	None
7	Disk Change	TSB	N/A	None

TABLE 23. DIGITAL INPUT REGISTER FOR SYSTEMS COMPATIBLE WITH THE IBM PC XT AND IBM PS/2 30

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Reserved	Unused TSB	0	None
1	250K Rate Select	TSB	N/A	None
2	No Write Precompensation	TSB	N/A	None
3	DMA, Interrupt Enable	TSB	N/A	None
4	Reserved	Unused TSB	0	None
5	Reserved	Unused TSB	0	None
6	Reserved	Unused TSB	0	None
7	- Disk Change	TSB	N/A	None

TSB = Tri-state Buffer

F/F = Flip Flop

If Storage Element is "none" or "unused", Reset Condition reflects fixed logic state.

Options Register

TABLE 24. OPTIONS REGISTER

BIT	SIGNAL	FUNCTION
0	Boot Disk Select	If "0", causes DS1/ and MOEN/1 to be swapped in H/W with DS0/ and MOEN0/. Therefore, if DOR selects Drive 0, then actually Drive #1 will be selected and enabled, allowing a S/W operating system to be booted from the disk drive.
1	SWTC	Software Terminal Count allows a TC to be issued to the core controller under BIOS driver control.
2-3	PCV	These two bits define the precompensation values, as shown in the truth table below.
4	NWP	This bit disables write precompensation in modes compatible with IBM PS/2 50, 60 and 80 only.

TABLE 25. TRUTH TABLE

BIT 3	BIT 2	PRECOMP VALUE
0	0	+/- 1 Clocks
0	1	+/- 2 Clocks *
1	0	+/- 3 Clocks
1	1	+/- 4 Clocks
* RST Default		

Note: Clk = Clk 1 for all data rates, except when 300 Kb/s is selected which requires Clk 2. In PS/2 model 30 precompensation can be disabled by using bit 2 in the Configuration Control Register. In PS/2 50, 60 and 80, bit 4 of the Options Register disables precompensation.

TABLE 26. OPTIONS REGISTER

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Boot Disk Select	F/F	0	None
1	SWTC	F/F	0	None
2	PCV	F/F	0	None
3	PCV	SR F/F	1	None
4	No Write Precompensation	F/F	0	None
5	Reserved	Unused F/F	0	None
6	Reserved	Unused F/F	0	None
7	Reserved	Unused F/F	0	None

F/F = Flip Flop SR F/F = Set Reset Flip Flop

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS - all voltages referenced to VSS

VCC	7.0 Volts
Voltage at any pin	-0.3 to VCC +0.3 Volts
Storage Temperature	-55^{o} to $+150^{o}$ C
Operating Temperature	0^{o} to $+70^{o}$ C

DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
+5V Supply	VCC	4.5	5.5	V
Input Low Voltage - Data Bus & XTOSC	VIL		0.8	V
Input High Volt - Data Bus & XTOSC	VIH	2.0		V
Input Low Threshold-Schmitt Trigger	VILT	0.8		V
Input High Threshold-Schmitt Trigger	VIHT		2.0	V
Schmitt Trigger Input Hysteresis	VIHYS	0.45		V
Output Low - DBx,IRQ,DMA ; Io=12.0mA	VOL		0.4	V
Output High - DBx,IRQ,DMA; Io=-5.0mA	VOH	2.8		V
Output Low - High Current; Io=48mA	VOLHC		0.4	V
PQR trip threshold	VPQR	2.75	4.35	V
Latch Up Current Low	ILUL	40		mA
Latch Up Current High	ILUH	-40		mA
Leakage Current Low	ILL		10	µA
Leakage Current High	ILH		-10	µA
Supply Current - 100µA source loads	ICC		40	mA
Supply Current - 5mA source loads	ICCHL		90	mA
Power Dissipation - ICC max *	PD		400	mW
Power Dissipation - ICCHL max *	PDHL		550	mW

* Includes open drain high current drivers at Vol = 0.4V

TIMING CHARACTERISTICS (CL=100pf):

PARAMETER	SYMBOL	MIN	MAX	UNIT
Clock Period	tCY	60		nS
Clock Active (High or Low)	tPH	25		nS
Clock Rise Time (Vin 0.8 to 2.0)	tR		5	nS
Clock Fall Time (Vin 2.0 to 0.8)	tF		5	nS
A0-2 Set Up Time to RD- low	tAR	10		nS
A0-2, Hold Time to RD- high	tRA	0		nS
CS-, DACK Set Up Time to RD- low	tCDR	0		nS
CS-, DACK Hold Time to RD- high	tRCD	0		nS
RD- Width	tRR	80		nS
Data Access Time from RD- low	tRD		70	nS

PARAMETER	SYMBOL	MIN	MAX	UNIT
DB to Float Delay from RD- high	tDF	10	40	nS
A0-2 Set Up Time to WR- low	tAW	10		nS
A0-2, Hold Time to WR- high	tWA	0		nS
CS-, DACK Set Up Time to WR- low	tCDR	0		nS
CS-, DACK Hold Time to WD- high	tRCD	0		nS
WR- Width	tWW	60		nS
Data Set Up Time to WR- high	tDW	60		nS
Data Hold Time from WR- high	tWD	0		nS
IRQ Reset Delay Time from RD- high	tRI		1MCY+100nS	
IRQ Reset Delay Time from WR- high	tWI		1MCY+100nS	
DMA Cycle Time	tMCY	52		MCY
DMA Reset Delay Time from DACK- low	tAM		80	nS
DACK- Delay Time from DMA high	tMA	0		nS
DACK- Width	tAA	80		MCY
TC Width	tTC	60		nS
Reset Width - TTL driven CLK1	tRST	60		nS
Reset Width - Software Reset	tSRST	5		MCY
RDD- Active Time Low	tRDD	40		nS
WD- Write Data Width Low	tWDD	1/2 (typ)		WCY
DIRC- Hold & Set Up to STEP- low	tDST	4		MCY
DSx- Hold time from STEP- low	tSTU	20		MCY
STEP- Active Time Low	tSTP	24		MCY
STEP- Cycle Time	tSC	132		MCY
DIRC- Hold Time after STEP-	tSTD	96		MCY
IDX- Index Pulse Width	tIDX	2		MCY
RD- Delay from DMA	tMR	0		nS
WR- Delay from DMA	tMW	0		nS
RD- or WR- Response from DMA high	tMRW		48	MCY
Chip Access Delay from RST low - TTL	tCA	32		MCY
Chip Access Delay from SRST- low	tCAS	40		MCY
Chip Access Delay - osc XT1 at 16 MHz	tXCA	500		µS
TC Delay from last DMA or IRQ, RD-	tTCR	0	192	MCY
TC Delay from last DMA or IRQ, WR-	tTCW	0	384	MCY

Note:

1) CY = CLK1 or XT1 period

2) MCY = MCLK period, dependent on selected data rate

3) WCY = WCLK period, dependent on selected data rate

4) Timing based on 3.5-inch floppy data rates.

- **MCY:**
  - 500 KByte MFM = 250 nsec.
  - 250 KByte MFM = 500 nsec.
- **MCLK:**
  - 8.0 MHz = 125 nsec.
  - 4.0 MHz = 250 nsec.
  - 2.0 MHz = 500 nsec.

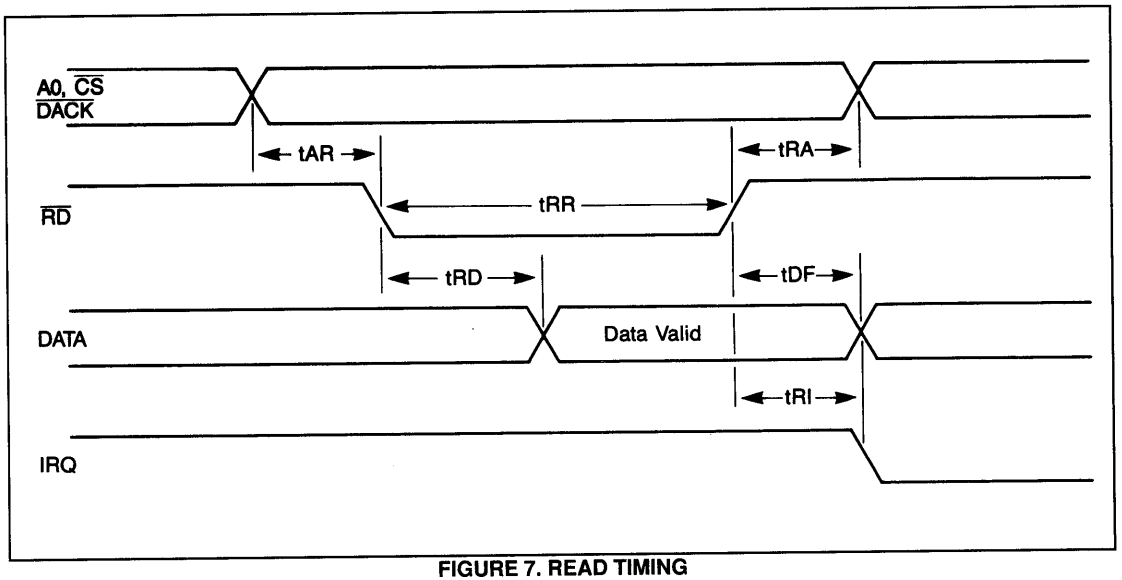

FIGURE 7. READ TIMING

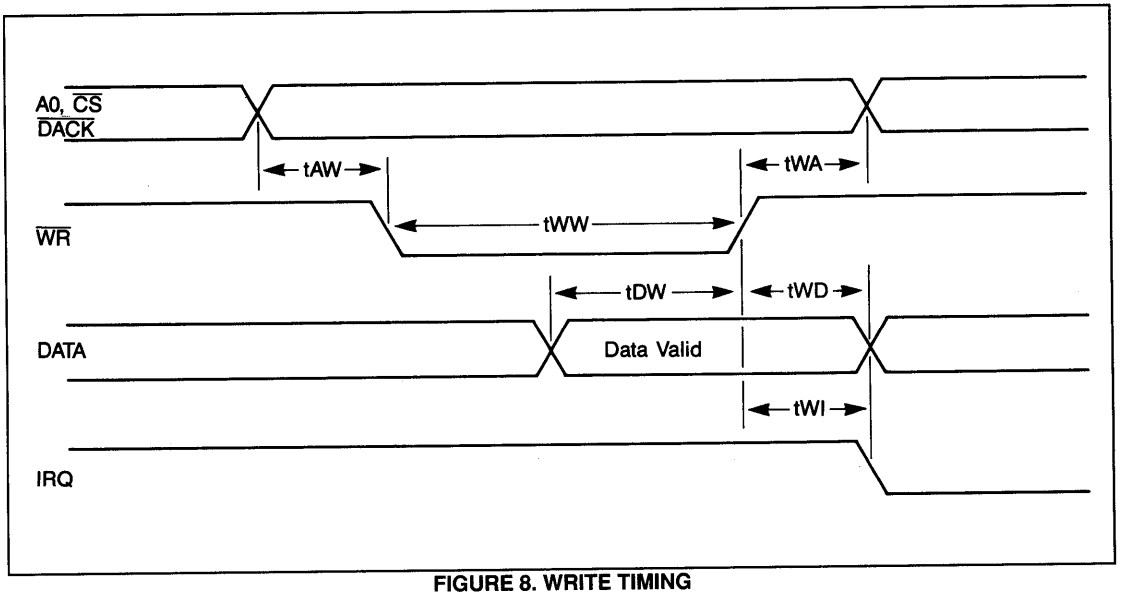

FIGURE 8. WRITE TIMING

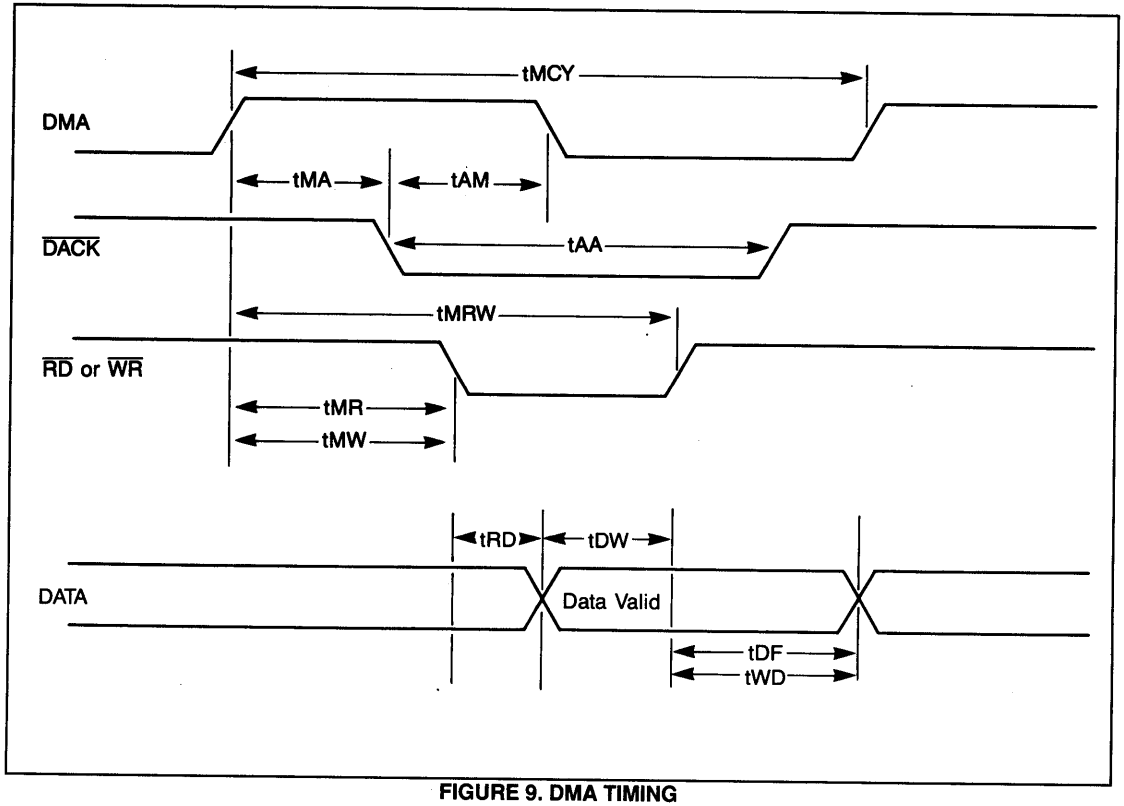

FIGURE 9. DMA TIMING

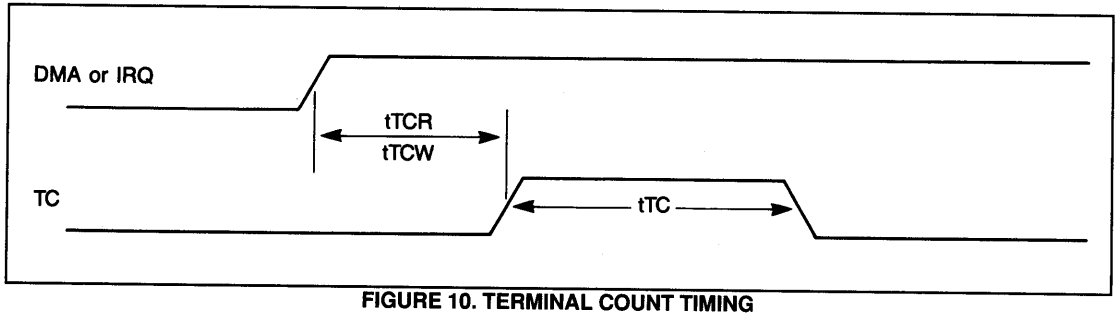

FIGURE 10. TERMINAL COUNT TIMING

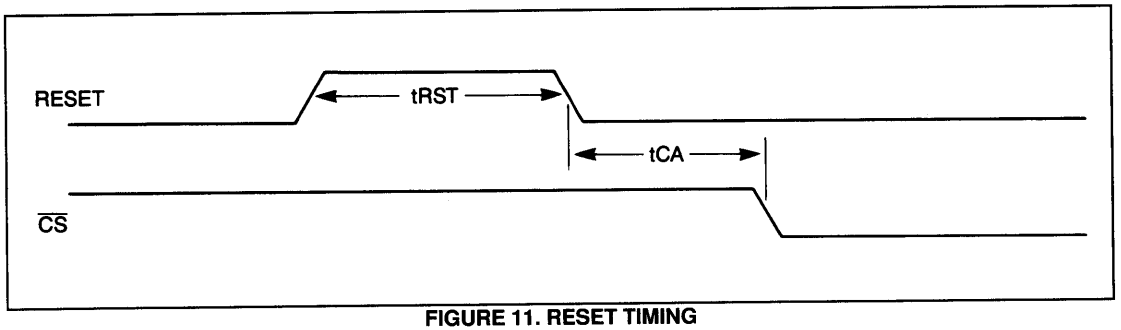

FIGURE 11. RESET TIMING

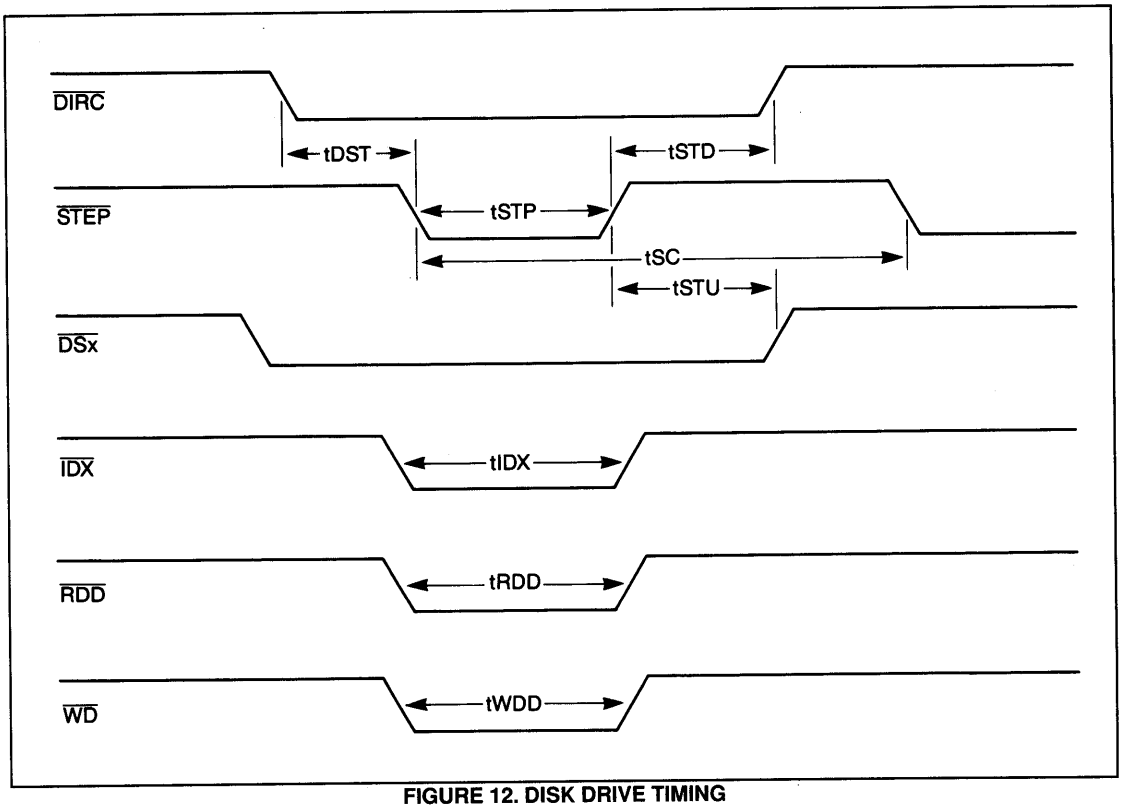

FIGURE 12. DISK DRIVE TIMING

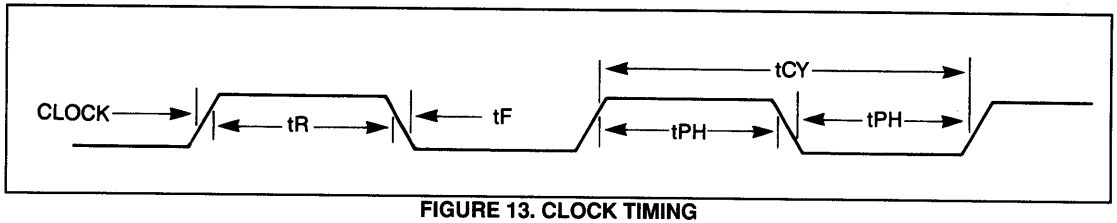

FIGURE 13. CLOCK TIMING

COMMAND SUMMARY

Command Parameters

The WD57C65 performs 15 different host supplied commands:

- READ DATA
- READ DELETED DATA
- WRITE DATA
- WRITE DELETED DATA
- READ A TRACK
- READ ID
- FORMAT A TRACK
- SCAN EQUAL
- SCAN LOW OR EQUAL
- SCAN HIGH OR EQUAL
- RECALIBRATE
- SENSE INTERRUPT STATUS
- SPECIFY
- SENSE DRIVE STATUS
- SEEK

A multibyte transfer from the processor initiates each command. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases: the command phase, the execution phase, and the result phase.

Command phase - The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor.

Execution phase - The FDC performs the operation it was instructed to do.

Result phase - After completion of the operation, status and other housekeeping information are available to the processor.

Tables 27 through 41 show the required parameters and results for each command. Most commands require nine command bytes and return seven bytes during the result phase. The "W" to the left of each bytes indicates a command phase byte to be written. An "R" indicates a result byte. Table 42, page 35, lists and defines all of the symbols used in tables 27 through 41.

TABLE 27. READ DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			C				→	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 28. READ DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			C				→	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 29. WRITE DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← DTL →								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 30. WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← DTL →								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 31. READ A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			C				→	Sector ID information prior to command execution.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
EXECUTION										Data transfer between FDD and main system. FDD reads all data fields from index hole to EOT.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 32. READ ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
EXECUTION										The first correct ID information on the cylinder is stored in Data Register.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information read during Execution Phase from floppy disk.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 33. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0		1	1	0	1	Command Codes
	W	X	X	X	X		X	HS	US1	US0	
	W	←				N				→	Bytes/Sector
	W	←				SC				→	Sectors/Track
	W	←				GPL				→	Gap 3
	W	←				D				→	Filler Byte
EXECUTION											Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R	←				ST0				→	Status information after command execution.
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	In this case, the ID information has no meaning.
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

TABLE 34. SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1		0	0	0	1	Command Codes
	W	X	X	X	X		X	HS	US1	US0	
	W	←				C				→	Sector ID information prior to command execution.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				STP				→	
EXECUTION											Data compared between the FDD and main system.
RESULTS	R	←				ST0				→	Status information after command execution.
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution.
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

TABLE 35. SCAN LOW OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← STP →								
EXECUTION										Data compared between the FDD and main system.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 36. SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← STP →								
EXECUTION										Data compared between the FDD and main system.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 37. RECALIBRATE

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
EXECUTION										Head retracted to Track zero.

TABLE 38. SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	0	0	0	Command Codes
RESULTS	R	←ST0→								Status information about the FDC at the
	R	←PCN→								end of seek operation.

TABLE 39. SPECIFY

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	0	1	1	Command Codes
	W	←SRT→				←HUT→				
	W	←HLT→							ND	

TABLE 40. SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
RESULTS	R	←ST3→								Status information about the FDC.

TABLE 41. SEEK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←NCN→								
EXECUTION										Head is positioned over proper cylinder on the diskette.

TABLE 42. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
A0	ADDRESS LINE 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1).
C	CYLINDER NUMBER	C stands for the current/selected cylinder (track) numbers 0 through 255 of the medium.
D	DATA	D stands for the data pattern which is going to be written into a sector.
D7 - D0	DATA BUS	8-bit DATA BUS, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	DATA LENGTH	When N is defined as 00, DTL stands for the DATA LENGTH which users are going to read out or write into the sector.
EOT	END OF TRACK	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	GAP LENGTH	GPL stands for the length of Gap 3. During the FORMAT Command, it determines the size of Gap 3.
H	HEAD ADDRESS	H stands for head number 0 or 1, as specified in the ID field.
HLT	HEAD LOAD TIME	HLT stands for the HEAD LOAD TIME in FDD (2 to 254ms in 2ms increments).
HS	HEAD SELECT	HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC).
HUT	HEAD UNLOAD TIME	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240ms in 16ms increments).
MF	FM or MFM	If MF is low, FM mode is selected. If it is high, MFM mode is selected.
MT	MULTITRACK	If MT is high, a MULTITRACK operation is performed. If MT=1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	NUMBER	N stands for the NUMBER of data bytes written in a sector.
NCN	NEW CYLINDER NUMBER	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head.
ND	NON-DMA MODE	ND stands for operation in the NON-DMA MODE.
PCN	PRESENT CYLINDER	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head at present time.
R	RECORD	R stands for the sector number which will be read or written.
R/W	READ/WRITE	R/W stands for either READ or WRITE signal.
SC	SECTOR	SC indicates the number of sectors per cylinder.
SK	SKIP	SK stands for SKIP Deleted Data Address mark.
SRT	STEP RATE TIME	SRT stands for the Stepping Rate for the FDD (1 to 16ms in 1ms increments). Stepping Rate applies to all drives. In 2's complement format, F(Hex)=1ms, E(Hex)=2ms, etc.

TABLE 42. COMMAND SYMBOL DESCRIPTIONS (CONTINUED)

SYMBOL	NAME	DESCRIPTION
ST0 ST1 ST2 ST3	STATUS 0 STATUS 1 STATUS 2 STATUS 3	ST0 – 3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0=0). ST0 – 3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a SCAN operation, if STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectors are read and compared.
US0,US1	UNIT SELECT	US stands for a selected drive; binary encoded, 1 of 4.

Command Descriptions

Read Data

A set of nine byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits for the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number (R) stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and placed on the data bus. This continuous read function is called a "Multi-sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time as the DACK/ for the last byte of data. Upon receipt of this signal, the FDC stops outputting data to the processor, but continues to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and terminate the Read Data command at the end of the sector. The amount of data handled by a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (number of bytes/sector). Table 43 lists the Transfer Capacity.

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note: this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length as a sector. If DTL is smaller than the actual data length of a sector, the data beyond DTL in the sector is not sent to the Data Bus. The FDC reads (internally) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read operation. When N is non-zero, then DTL has no meaning and sets to FF (hexadecimal.)

Upon completion of the Read Data command, and after Head Unload Time Interval (specified in the Specify command) has elapsed, the head un-

TABLE 43. TRANSFER CAPACITY

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

loads. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a "1" (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to "0" and "1", respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If it detects a read error (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to "1" (high). If a CRC error occurs in the Data Field, the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a "1" (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to "0" and "1", respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in status Register 2 to a "1" (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the processor must service the FDC every 27 microseconds in the FM mode, and every 13 microseconds in the MFM mode. If not, the FDC sets the OR (Overrun) flag in Status Register 1 to a "1" (high), and terminates the Read Data command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result phase is dependent upon the state of the MT bit and EOT byte. Table 44 shows the values for C, H, R, and N, when the processor terminates the command.

TABLE 44. C, H, R, AND N VALUES

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
	0	Equal to EOT	C+1	NC	R=01	NC
	1	Less than EOT	NC	NC	R+1	NC
	1	Equal to EOT	C+1	NC	R=01	NC
1	0	Less than EOT	NC	NC	R+1	NC
	0	Equal to EOT	NC	LSB	R=01	NC
	1	Less than EOT	NC	NC	R+1	NC
	1	Equal to EOT	C+1	LSB	R=01	NC

Notes: NC (No Change): The same value as the one at the beginning of command execution. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

The FDC requires nine bytes of command for the Write Data mode. After the Write Data command issues, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C,H,R,N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in "R" is incremented by one, and the next data field is written. The FDC continues this Multi-Sector Write Operation until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC, the FDC continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detect a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a "1" (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to "0" and "1", respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer Capacity
- EN (End of Cylinder) flag
- ND (No Data) flag
- Head Unload Time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N≠0

In the Write Data mode, data transfers between

the processor and FDC via the data bus, must occur every 27 microseconds in the FM mode and every 13 microseconds in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a "1" (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to "0" and "1", respectively.)

Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address mark is written at the beginning of the data field instead of the normal Data Address mark.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK = 0 [low]), it will read all the data in the sector and set the CM flag in Status Register 2 to a "1" (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

Read A Track

This command is similar to the Read Data command, except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hold, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR. It sets the ND flag of the Status REgister 1 to a "1" (high) if there is no comparison. Multi-Track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses the index hold for the second time, it sets the MA (missing Address mark) flag in Status Register 1 to a "1" (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to "0" and "1", respectively.)

Read ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a "1" (high). If no data is found, then the ND (No Data) flag is also set in Status Register 1 to a "1" (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to "0" and "1", respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette: Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which the processor supplies during the command phase. The data field is filled with the byte of data stored in D. The processor supplies the ID field for each sector; that is, the processor makes four data requests per sector for C (cylinder number), H (head number), R (sector number) and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the WD57C65 for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by "1" after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

Table 45 shows the relationship between N, SC, and GPL for various sector sizes.

TABLE 45. N, SC, AND GPL RELATIONSHIP

Format	Sector Size	N	SC	GPL[1]	GPL[2] [3]
	8" Standard Floppy				
FM Mode	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode[4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
	5¼" Minifloppy				
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode[4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
	3½" Sony Microfloppy				
FM Mode	128 bytes/sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode[4]	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Notes: [1] Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
[2] Suggested values of GPL in format command.
[3] All values except sector size are hexidecimal.
[4] In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00)

increments (R + STP $\longrightarrow_8$ R), and the scan operation continues. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a "1" (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a "1" (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 46 shows the status of bits SH and SN under various conditions of Scan.

TABLE 46. STATUS OF BITS SH AND SN

	Status Register 2		
Command	Bit 2 = SN	Bit 3 = SH	Comments
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	0	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
	0	1	$D_{FDD} = D_{Processor}$
Scan High or Equal	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexadecimal byte of FF either from memory or from FDD, can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). If, after a whole sector of data is compared, and the conditions are not met, the sector number

If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control Mark) flag of Status Register 2 to a "1" (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control mark) flag of Status Register 2 to a "1" (high) in order to show that a deleted sector had been encountered.

During the Scan command, the processor or DMA controller supplies the data for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status

Register 1, it is necessary to have the data available in less than 27 microseconds (FM mode) or 13 microseconds (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to "0" and "1", respectively.

Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a "1" (high), and step pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD set to a "0" (low), and step pulses are issued. (Step Out)

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse issues, NCN is compared against PCN, and when NCN = PCN, the SE (Seek End) flag sets in Status Register 0 to a "1" (high), and the command terminates. At this point FDC interrupt goes high. Bits D0B-D3B in the Main Status Register set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state; but during the Execution phase, it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If the time to write three bytes of Seek command exceeds 150 microseconds, the timing between the first two step pulses may be shorter than set in the Specify command by as much as 1 millisecond.

Recalibrate

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a "1" (high) and the command terminates. If the Track 0 signal is still low after 77 step pulses have issued, the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both "1s" (highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to "0" and "1", respectively.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following conditions:

1. Upon entering the Result phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Cylinder command
   g. Write Deleted Data command
   h. Scan commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate command
4. During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an Execution phase in non-DMA mode, DB5 in the Main Status Register is high. Upon entering the Result phase, this bit clears. Conditions 1 and 4 do not require Sense Interrupt Status commands. The interrupt clears by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of

TABLE 47. INTERRUPT CAUSE

Seek End	Interrupt Code		
Bit 5	Bit 6	Bit 7	Cause
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate command
1	1	0	Abnormal Termination of Seek or Recalibrate command

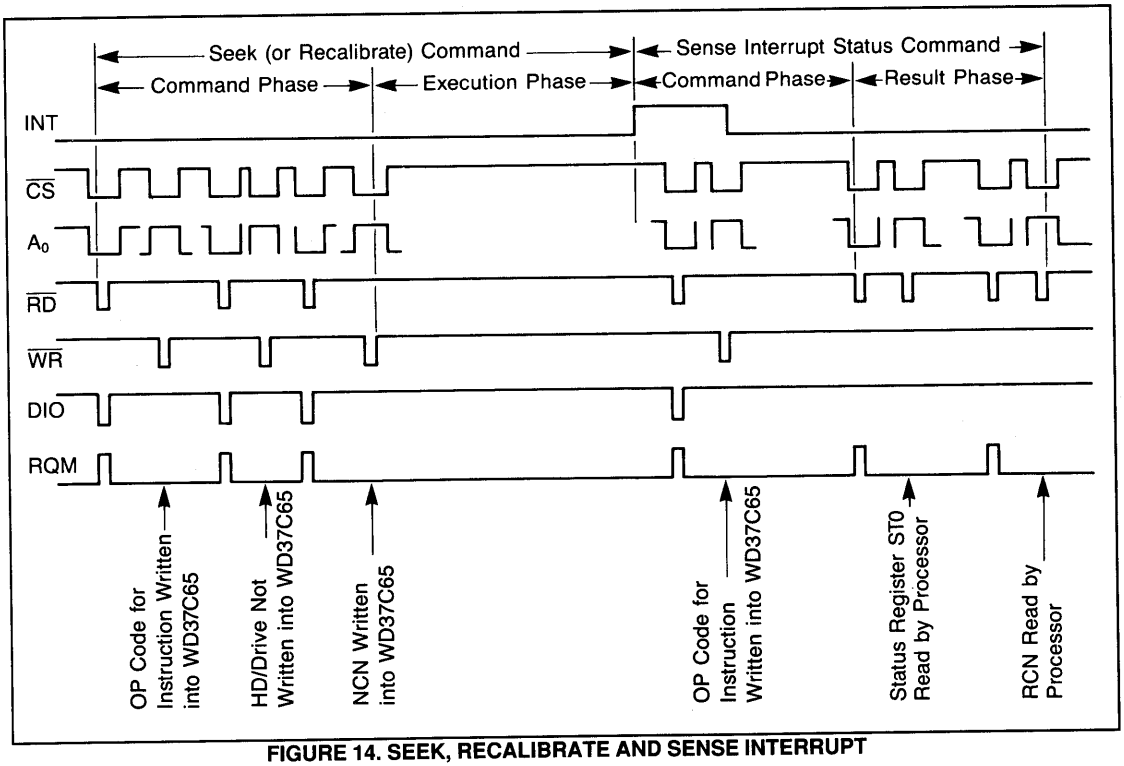

FIGURE 14. SEEK, RECALIBRATE AND SENSE INTERRUPT

the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and via bits 5,6, and 7 of Status Register 0, identifies the cause of the interrupt.

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no Result phase. When the disk drive has reached the desired head position, the WD57C65 will set the interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. See Figure 14.

The Specify command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240 milliseconds in increments of 16 milliseconds (01 = 16 milliseconds, 02 = 32 milliseconds . . . OF_{16} = 240 milliseconds). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 milliseconds in increments of 1 millisecond (F = 1 millisecond, E = 2 milliseconds, D = 3 milliseconds, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 milliseconds in increments of 2 milliseconds (011 = 2 milliseconds, 02 = 4 milliseconds, 03 = 6milliseconds ...7F = 254 milliseconds).

The time intervals mentioned above are a direct function of the clock (CLK on pin 20). Times indicated above are for a 16 MHz clock; if the clock was reduced to 8 MHz, then all time intervals are increased by a factor of 2.

The choice of DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1), the Non-DMA mode is selected; and when ND = 0, the DMA mode is selected.

Sense Drive Status

The processor uses this command whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to "1" and "0", respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the WD57C65 is in the result phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0, it will find 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must follow after a Seek or Recalibrate interrupt; otherwise the FDC will not consider the next command.

In some applications, the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

APPENDIX

Device Resets

The WD57C65 supports both a hardware reset pin, RST, and a software reset, SRST/, through use of the Digital Output Register. The RST pin causes a device reset for the active duration. After a hardware reset, RST active, the WD57C65 is held in soft reset, SRST/ active, until SRST/ clears ,and default selects 500K MFM (or 250K FM, code dependent) as the data rate (16 MHz input clock). SRST/ also causes a reset condition for the active duration, which resets the microcontroller like RST, but does NOT affect the current data rate selection. RST, when active, disables the high current driver outputs to the disk drive.

Any reset will cause an IRQ since the WD57C65 always assumes the drive is READY. This happens because the drive polling routine senses a change in status from NOT READY to READY. In the IBM PC XT and IBM PS/2 Model 30, if DMAEN is not active for at least one millisecond after reset becomes inactive, the IRQ latch may set before it is enabled.

If the XTAL oscillator is used, instead of a TTL driven clock input, the reset time requirement is greater. The oscillator circuit is designed so that RST bootstraps the circuit into oscillation within a fixed amount of time. The extended reset time allows the oscillator to achieve a stable internal clock timing.

PQR (Power Qualified Reset)

The "PQR" is a power-up and power failure reset. It prevents glitches at the Drive Interface upon power-up or during power failure. The PQR has a clock detection circuit to ensure that the clock is stable. In PQR mode all the HCD drivers are disabled and they stay in reset mode. The "PQR" acts exactly like "RST" (Hardware reset).

Radio Frequency Interference Statement

This Western Digital product has been certified to comply with the limits for a Class B computing device pursuant to subpart J of Part 115 of FCC rules. This does not guarantee that interference will not occur in individual installations. Western Digital is not responsible for any television, radio, or other interference caused by unauthorized modifications of this product.

If interference problems do occur, please consult the system equipment owner's manual for suggestions. Some of these suggestions include relocation of the computer system away from the television or radio or placing the computer AC power connection on a different circuit or outlet.

The product was tested and certified with a shielded interconnecting cable; therefore, a shielded cable is required to be used with this product.

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Western Digital
2445 McCabe Way
Irvine, California 92714
(800) 847-6181 (714) 863-0102
FAX (714) 660-4909 TLX 910-595-1139

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