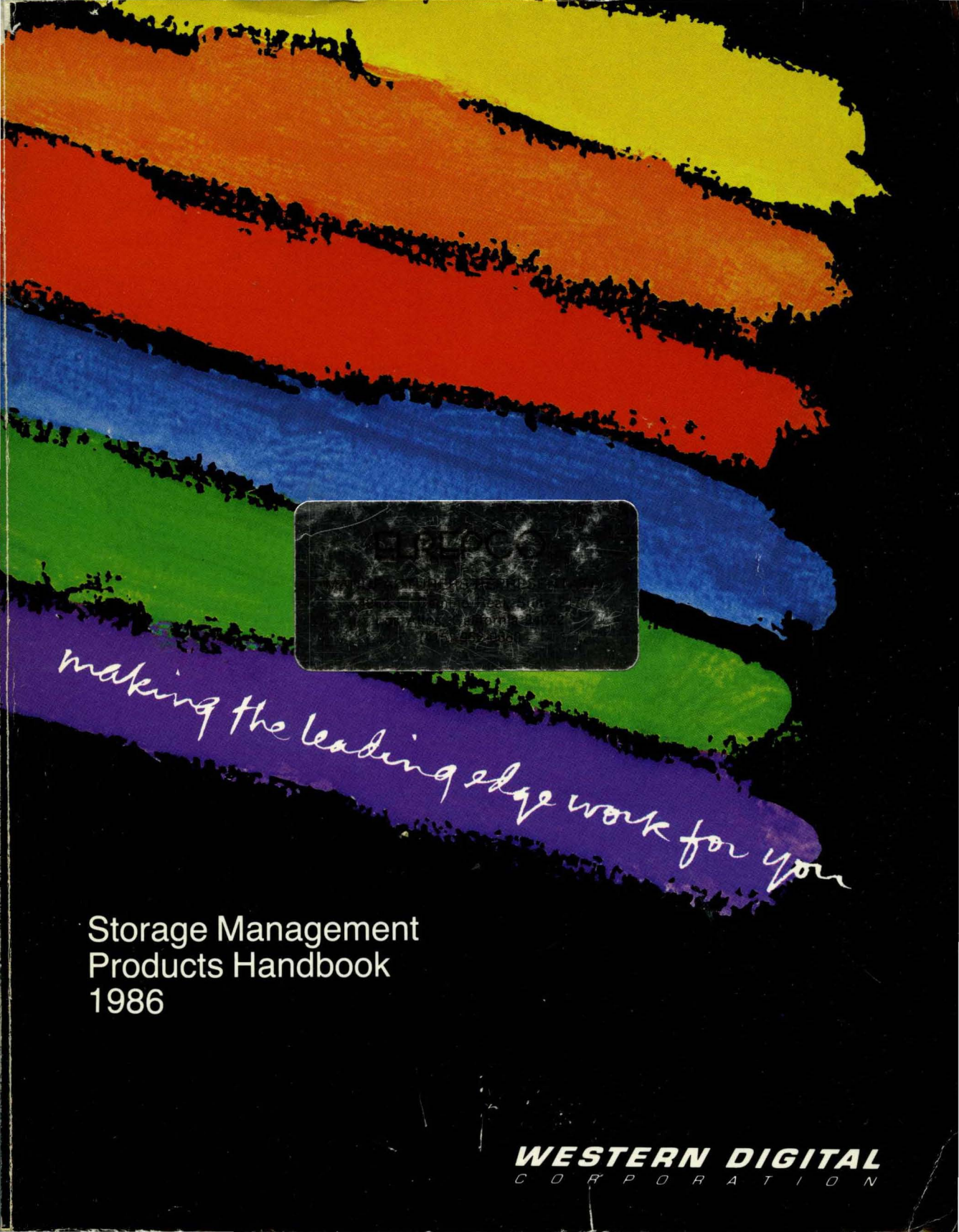

Storage Management Products Handbook 1986

WESTERN DIGITAL
CORPORATION

1986
Storage Management
Products Handbook

Corita Kent, the cover artist, is an American whose work presents an optimistic, yet philosophical view of the world we live in. A former Catholic nun and teacher, Corita now devotes her life and energies to her artwork and the "human needs she feels transcend national and religious barriers." A true "citizen of the world," Corita's philosophy positions her "on the positive side of hope." Her depiction of the Western Digital mission . . . "Making the leading edge work for you" . . . dramatizes the spectrum of solutions we provide our customers.

Making the Leading Edge Work for You

This handbook is designed for you, the engineer. It's intended to be a useful tool, enabling you to make a preliminary evaluation of our products and later, with samples in hand, design our products into your own systems.

The data in these pages have been reviewed by our Marketing, Engineering, Manufacturing, and Quality groups. Now we would like you to review the information we've provided and tell us how we can improve it. Please feel free to suggest any changes, additions, or clarifications that occur to you. And don't hesitate to call to our attention any sins of omission or commission we may have made.

We're eager to help upgrade the quality of information our industry provides to its customers. So, please, help us. Direct your comments to:

WESTERN DIGITAL CORPORATION
Literature Department
2445 McCabe Way
Irvine, CA 92714
(714) 863-0102

WESTERN DIGITAL
C O R P O R A T I O N

Regional and District Sales Offices

NORTHEASTERN
UNITED STATES/EASTERN CANADA

Corporate Place I-95
100 Corporate Place
Suite 302
Peabody, MA 01960
(617) 535-5914

111 Madison Avenue
Morristown, NJ 07960
(201) 292-1490

NORTH CENTRAL
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(612) 835-1003

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UNITED STATES

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(404) 476-7704

2300 W. Meadowview Road
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Greensboro, NC 27407
(919) 299-6733

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(214) 248-6785

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6405 Congress Avenue
Suite 110
Boca Rotan, FL 33431
(305) 994-6900

WESTERN
UNITED STATES/WESTERN CANADA

2302 Martin Street
Suite 325
Irvine, CA 92714
(714) 851-1221

5743 Corsa Avenue
Suite 201
Westlake Village, CA 91361
(818) 991-2556

201 San Antonio Circle
Building E, Suite 172
Mountain View, CA 94040
(415) 941-0216

INTERNATIONAL OFFICES

Western Digital (U.K.) Ltd.
55 East Street
Epsom, Surrey KT17 1BP
United Kingdom
(03727) 42955

Western Digital Deutschland GmbH
Prinzregentenstr. 120
D-8000 Muenchen 80
Federal Republic of Germany
(089) 470-7021

Western Digital Corp.
12 Rue Auber
75009 Paris, France
(01) 266-1020

Western Digital Japan Ltd.
8th Floor Dai-44 Kowa Bldg
1-2-7, Higashiyama, Meguro-Ku
Tokyo 153 Japan
(03) 791-2001

WESTERN DIGITAL
C O R P O R A T I O N
2445 McCabe Way
Irvine, CA 92714
(714) 863-0102

Table of Contents

Data Sheets with the Heading below:

Advance Information: This product has not been produced in volume and is subject to functional and timing revisions. Prior to designing with the product, it is necessary to contact Western Digital Corporation for current information.

Functional Index

WINCHESTER BOARD PRODUCTS

TAPE DRIVE CONTROLLER PRODUCTS

MAIN MEMORY DEVICE

INTEGRATED DRIVE ELECTRONICS

Numerical Index

System Product Quality/Reliability

QUALITY PROGRAM DESCRIPTION

The Quality Organization shown on the attached organization chart (Figure 2) reports directly to the President of Western Digital. It assures compliance to design control, quality, and reliability specifications pursuant to corporate policy. Quality assurance provisions are derived in part from MIL-Q-9858, as applied to high grade commercial products.

CORPORATE QUALITY POLICY

It is the policy of Western Digital Corporation that every employee be committed to quality excellence in producing products/processes which conform to acceptable requirements. The total quality program is managed and monitored by the quality assurance organization. Quality assurance is chartered to review marketing product requirements, qualify hardware and software designs, certify manufacturing operations and monitor performance/control conformance to product specifications.

Primary responsibility for execution of the quality program rests with functional organizations to design, produce, and market high quality and high reliability products specified to our customers.

DESIGNING FOR RELIABILITY

The premise upon which board and system manufacturing operations are based is that quality is planned and designed-in, not screened-in or selected. A well-tested, high-quality design is far more reliable than a marginal design with any amount of burn-in or fixes. To assure top quality design, Western Digital maintains one of the most experienced board/system design staffs in the industry. A tightly controlled design review team comprising members from Quality Assurance, Marketing, Manufacturing and several experienced design engineers, provides review of each new design several times during its development to ensure widest possible performance margins. The production release procedure assures a checklist for:

- Test Method/Program Qualifications
- Characterization Report
- Field Test (Beta Test) Report
- Product Qualification Audit
- Documentation Package Release for Document Control
- Software/Diagnostics Qualification

MAINTAINING QUALITY/RELIABILITY IN PRODUCTION

The Quality Control Testing Flow Chart shown on Figure 1 defines the exact stages contained in the production process. Internally manufactured LSI components undergo 100% testing at maximum specified operating temperatures as well as strict quality controls defined to assure high quality and reliability. Components not designed and manufactured by Western Digital are also 100% screened during incoming inspection at 70°C. The tests performed include selective active component burn-in performed at 125°C for 160 hours to insure guaranteed levels of reliability. This 125°C accelerated testing eliminates defects that cannot effectively be accelerated by burning-in boards and systems which have temperature limitations. Key quality control procedures include:

- Incoming Inspection Procedure
- In-Process Travel Card Traceability
- Workmanship Standards
- Quality Corrective Action Notice/MRB Procedure
- Quality Audit Procedure

PRODUCT FINAL TEST/CORRECTIVE ACTION

All boards are 100% in-circuit tested and 100% functional tested for acceptable performance according to applicable test specifications on testers qualified by QA. Products are tested at maximum specified temperature and voltage margins using diagnostic software to ensure greater performance margins. Failures are logged on a travel card specifically designed to insure traceability to manufacturing steps and to maintain failure records for QA corrective action.

If the board is designed to perform in a Host system, further diagnostics are performed in an environment configured to actual customer requirements.

PRODUCT ACCEPTANCE

Upon completing the final test, the board/system undergoes QC final workmanship standards inspection and selective samples are audited to the functional product specification to guarantee quality at specified operating margins to the customer.

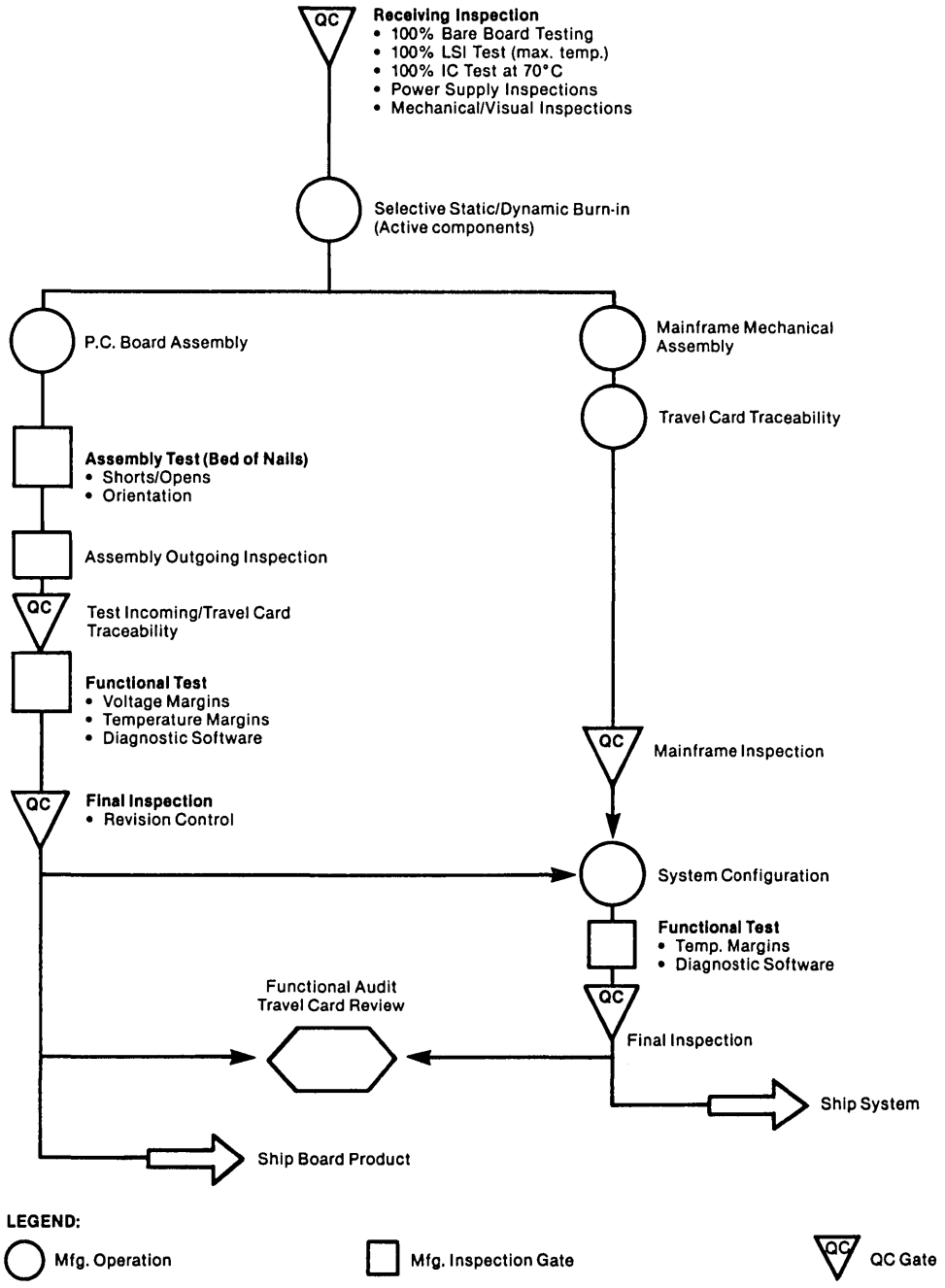


Figure 1. QUALITY CONTROL TESTING FLOW CHART

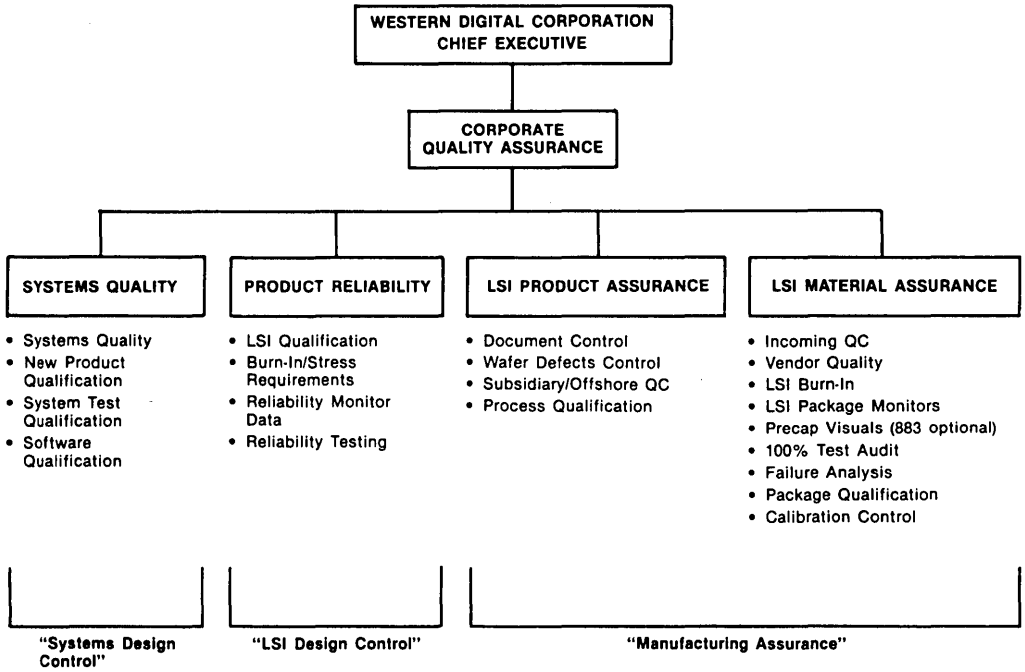


Figure 2. QUALITY ORGANIZATION

Quality/Reliability To Leading Edge Technology

QUALITY ASSURANCE PROGRAM HIGHLIGHTS

- LSI manufacturing assurance provisions are derived in part from MIL-M-38510 and MIL-STD-883B as applied to high grade commerical components.
- All process raw materials used in the Mask/Wafer fabrication and assembly operations are monitored by Material Assurance.
- Material Assurance maintains a thorough control of incoming material and has developed unique "use/stress tests" (look ahead sample build acceptance) which critical material must pass before acceptance.
- The product assurance Department continuously monitors the internal and external manufacturing flow (shown in Figure 1) and issues process control reports displaying detailed data and trends for the associated areas.
  - Document control is an integral part of Product Assurance. All specifications are issued and controlled by this activity.
  - The Western Digital Malaysian assembly operation uses specifications and quality control provisions controlled by Document Control. Indicators of Malaysia quality are reviewed weekly.
  - Purchased FAB and assembly operations are individually qualified and are certified against standard specifications during vendor qualification and monitored against reliability criteria.
  - Defect control within the process assures the highest levels of built-in reliability.
- Quality audits and gates are located throughout the manufacturing process in order to assure a stable process and thus, a quality product to our customers. Figure 1 illustrates the manufacturing/screening/inspection flow diagram and identifies the steps as they relate to the production of LSI devices.
- Testing assures quality margins through 100% testing by manufacturing and, in addition, all products must pass a specified AQL sample test performed by QA at maximum operating temperature as follows:

Outgoing Quality Levels

SUBGROUPS	INSPECTION LEVEL
Subgroup 1-Final 100% Electrical Audit @ Max °C	0.5 AQL
Subgroup 2-Visual (Marking, Lead Integrity, Package, Verify customer shipper)	1.0 AQL
Subgroup 3-Shipping Visual Audit	1.0 AQL

*The double sampling techniques used allow considerably better AQL's in most all cases.

- LSI devices are 100% tested on industry standard test systems. Quality outgoing testing (auditing) is done on the Fairchild Sentry Series 20 where possible to allow better correlation with customers.

- **PROGRAMS TO ASSURE OPTIMUM RELIABILITY**

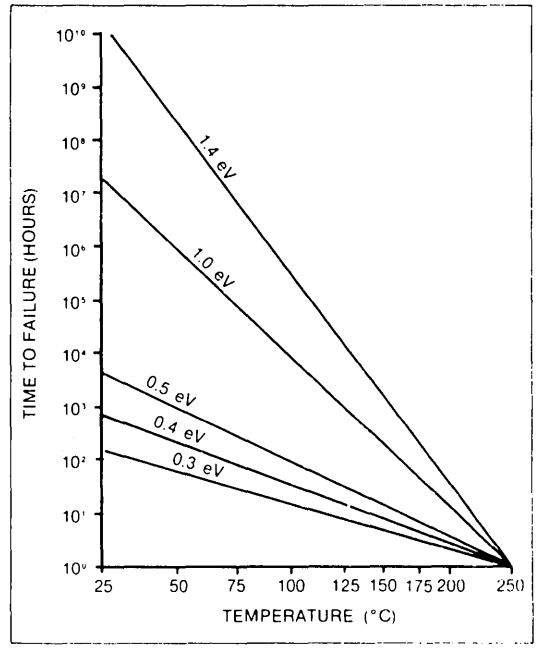
Improved levels of reliability are available under custom reliability programs using static and dynamic burn-in to further improve reliability. These programs focus on MOS failure mechanisms as follows:

FAILURE MECHANISMS IN MOS

FAILURE MECHANISM	EFFECT ON DEVICE	ESTIMATED ACTIVATION ENERGY	SCREENING METHOD
Slow Trapping	Wearout	1.0 eV	Static Burn-In
Contamination	Wearout/ Infant	1.4 eV	Static Burn-In
Surface Charge	Wearout	0.5-1.0 eV	Static Burn-In
Polarization	Wearout	1.0 eV	Static Burn-In
Electromigration	Wearout	1.0 eV	Dynamic Burn-in
Microcracks	Random	-	100% Temp. Cycling
Contacts	Wearout/ Infant	-	Dynamic Burn-in
Oxide Defects	Infant Random	0.3 eV	Dynamic Burn-In at max. voltage
Electron Injection	Wearout	-	Low Temp. Voltage Operating Life.

Temperature Acceleration of Failure

The Arrhenius Plot defines a failure rate proportional to exp (- Ea/kt) where Ea is the activation energy for the failure mechanism. The figure on the right indicates that lower activation energy failures are not effectively accelerated by temperature alone; hense, maximum voltage operation is selectively applied to optimize the burn-in process.



Static Burn-In (125°C-48 hours or 160 hours)

Provided on a sample basis for process monitor/control of 0.5 eV - 1.0 eV failure mechanisms. 100% static burn-in may be specified at an additional cost. However, static burn-in is considered only partially effective for internal LSI gates at logic "O" levels.

Dynamic Burn-In (Pattern test/125°C - 8 hours to 160 hours)

Accelerated functional dynamic operating life effectively controls internal MOS gate defects buried from external pin access. The input pattern is optionally pseudo-random or fixed pattern programmable to simulate 1000-3000 hours of field operation at maximum operating voltage(s).

High-Rel "K" Testing Program

General conformance to MIL-STD-883B method 5004.4, Class B with static Burn-In (Dynamic Burn-In may be specified as an option).

RELIABILITY MEANS LASTING VALUE

DESIGNING FOR RELIABLILITY

The Production release procedure for an LSI device is designed to assure maximum reliability with a Quality checklist for:

- ☑ Test Program Qualifications
- ☑ Characterization report
- ☑ Field test (Beta Test) report
- ☑ Reliability Lifetest Qualifications
- ☑ Infrared Thermal Analysis
- ☑ Static Protection

All New devices and major process changes must pass reliability qualification before incorporation into production using the criteria defined in Tables 2-4. The infrared microscope assures optimum burn-in temperatures and margins of safety. The dynamic burn-in system is one of two custom designed systems which assure protective device isolation during burn-in.

- **MAINTAINING RELIABILITY IN PRODUCTION**

Process defect controls are defined to continually measure built-in reliability, as measured by the following criteria:

TABLE 1

PROCESS RELIABILITY CONTROL	METHOD	CONDITION	SAMPLE*
Subgroup 1-Defects Control			
a. Oxide Integrity	Non-destructive bubble test	Pinhole defect density	5 wafers
b.Polysilicon Integrity	SEM Analysis	Visual	5 wafers
Subgroup 2-Electro-Migration Control			
Metal Step Coverage	MIL-STD-883 Method 2018	SEM Analysis	5 wafers
Subgroup 3-Defect Density	Critical layers Field Gate Contact Metal	Visual of Photo defects (Defects/in^2)	8 wafers each layer
Subgroup 4-Passivation/Insulation Priority	MIL-STD-883 Method 2021	Visual of Pinhole defect density	Final Silox 5 wafers Intermediate 5 wafers

Inspection intervals are defined by the in-line process control data reviewed on a lot-by-lot basis.

TABLE 2 STANDARD RELIABILITY LEVELS

TEST	METHOD	CONDITION	FAILURE
Infant Mortality (see note)	Static Burn-In	125°C - 160 hrs.	<0.5%
Long Term Failure Rate	Dynamic Life Test	125°C - 1000 hrs.	<.05%/1000 hrs. @55°C 60% Confidence

*NOTE: Devices failing the infant mortality target remain in burn-in until acceptable failure rates are obtained.

TABLE 3 GROUP A DEVICE RELIABILITY MONITORS

TEST	METHOD	CONDITIONS	LTPD
Subgroup 1			
a.Internal Visual			15
b.Thermal Shock	1011	Test Failure Used (cond. B or C)	
c.Bond Strength	2011	Test Failures (cond.B)	
d.Die Shear Strength	2019	Test Failures	
Subgroup 2			
a.Seal-Gross Leak		Fluorocarbon detection 10-3 atm/cc/sec	15
b.Seal-Fine Leak	1014	Test Condition A	
Subgroup 3			
a.Rotating Steady State Life Test	1005	Static 160 hr. Burn-In 125°C plus 125°C Lifetest - 1000 hrs.	5
b.Electrical Parameters	-	Final electrical @ 25°C (with data @ 70°C)	

TABLE 4 GROUP B PACKAGE RELIABILITY MONITORS

TEST	METHOD	CONDITIONS	LTPD
Subgroup 1			
a. Thermal Shock	1011	Test Condition B or C	15
b. Temperature Cycling	1010	Test Condition B or C	
c. Seal-Gross Leak	-	Fluorocarbon detection 10^{-3} atm/cc/sec	
d. Seal-Fine Leak (ceramic	1014	Test Conditoin A	
e. Electrical Parameters	-	Electrical at max-C	
f. 85/85 Moisture Resistance (plastic only)	-	85% RH/85°C for 1000 hours PDA = 10%	
g.Electrical Parameters	-	Final electrical @25°C	
Subgroup 2			
a. High Temp. Storage	1008	Test Condition B or C	
b. Mechanical Shock	2002	Test Condition B	15
c. Seal - Gross Leak	-	Fluorocarbon detection 10^{-3} atm/cc/sec	
d. Seal - Fine Leak (ceramic)	1014	Test Condition A	
e. Electrical Parameters	-	Final electrical @ 25°C/max. C	
Subgroup 3			
a. Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
b. Seal - Gross Leak	-	Fluorocarbon detection 10^{-3} atm/cc/sec	
c. Seal - Fine Leak (ceramic)	1014	Test Condition A	

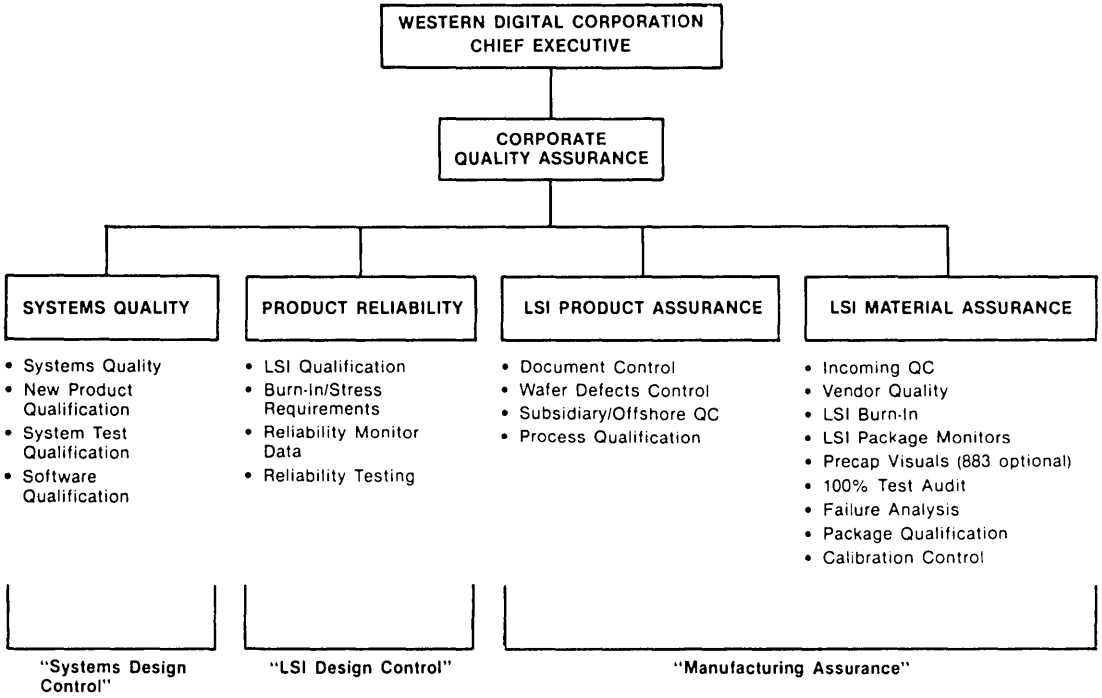


Figure 2 QUALITY ORGANIZATION

Announcing Burn-in Program Availability/Warranties

Western Digital now supports customer burn-in requirements for both static and dynamic burn-in under the strict control of the QA-Reliability Organization.

This burn-in provides high peformance 125°C static and dynamic burn-in for 8-160 hours to eliminate infant mortality and improve reliability. This process is executed using custom modified 32Bit, AEHR test commerical burn-in equipment which provide monitored fixed pattern or pseudo random burn-in with power supply and resistor device pin isolation.

LSI dynamic burn-in is verified in all cases by the design engineer for proper functioning. LSI Chip sets are also individually burned-in with dynamic equivalency to assure high performance bundled reliability.

The warranty on the program will optionally provide certificate of compliance to standard or custom designed burn-in programs and guarantee <.05%/Khrs failure rate.

CAUTION

Using outside burn-in methods not certified as acceptable by Western Digital may result in voided warranty, due to mishandling, junction temperature stress, or electrical damage. Further, since most burn-in houses do not support testing, catastrophic system condition can result in substantial damage before a problem is identified.

One consistent problem experienced with outside LSI burn-in houses can cause reliability problems; namely, parallelling totem pole MOS outputs, where the output states are not predictable, can cause a single (or a few) device(s) to sink all the current from the other devices on the burn-in tray - electromigration or current zaps are both possible.

Western Digital burn-in diagrams, dated after 1/1/82, must be used exactly as shown and will be provided upon request.

SEE YOUR LOCAL REPRESENTATIVE FOR COSTS AND ORDERING INFORMATION ON THIS NEW PROGRAM.

Hi-Rel "K" Testing Program

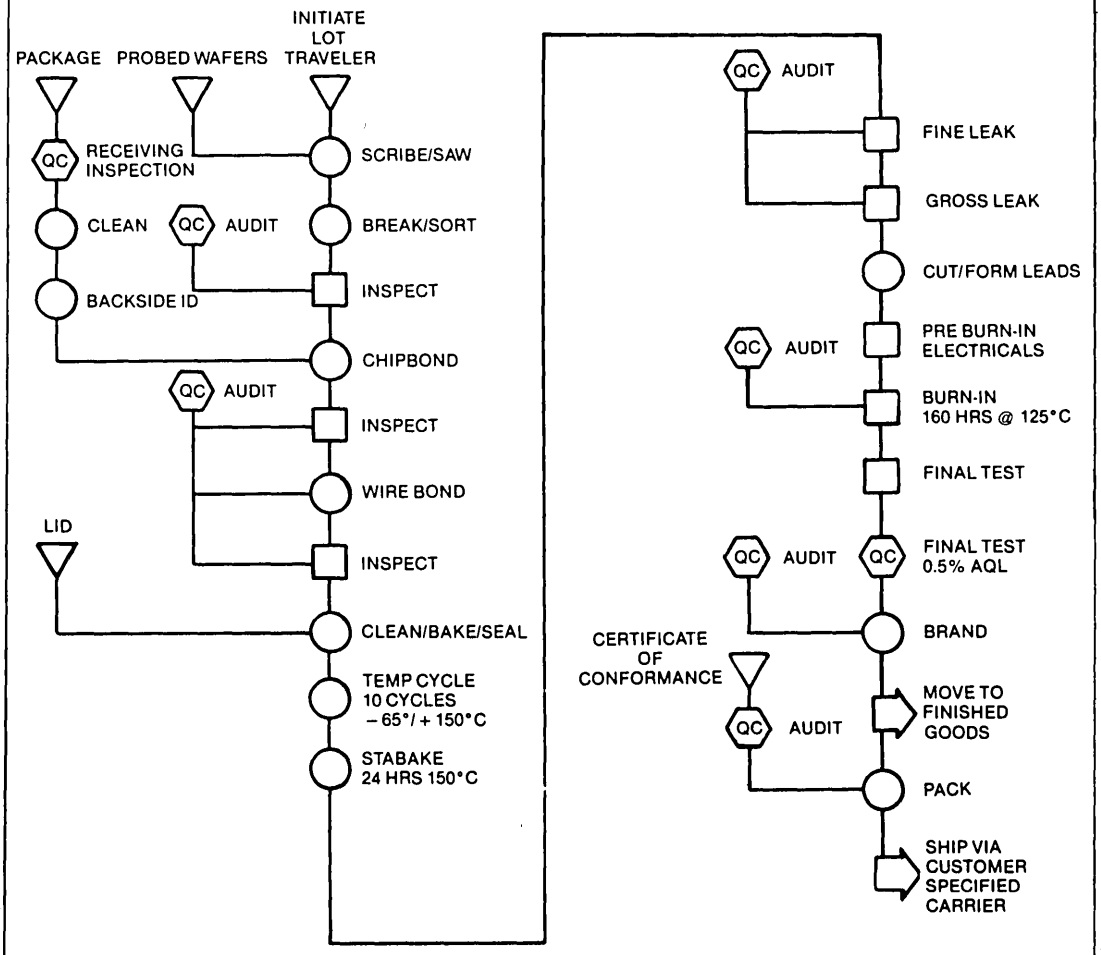
FEATURES

GENERAL CONFORMANCE TO MIL-STD-883B, METHOD 5004.4, CLASS B (SEE COMPARISON ON FOLLOWING PAGES)

- INCLUDES:
  - PRECAP VISUALS
  - SEAL INTEGRITY
  - POWER CONDITIONING
  - ENHANCEMENT OPTIONS

GENERAL DESCRIPTION

Western Digital's Hi-Rel "K" program is designed to provide high reliability devices for extended temperature environments. Individual enhancements may be specified to meet a customer's requirements.



HI-REL "K" PROGRAM FLOW DIAGRAM

COMPARISON OF MIL-STD-883 AND HI-REL "K" TEST PROGRAM

MIL-STD-883B, METHOD 5004.4, CLASS B	HI-REL "K" TEST
3.1.1 Internal Visual Method 2010.3 Test Condition B	All Hi-Rel "K" devices receive 100% inspections prior to lid seal. These inspections together comprise criteria comparable to Mil-Std-883, method 2010.3, test condition B.
3.1.2 Stabilization Bake Method 1008.1 Test condition C 24 hours at 150°C	Same
3.1.3 Temperature Cycling Method 1010.2, Test condition C -65°C to 150°C for 10 cycles, with 10 minutes dwell and 5 minutes maximum transfer time	Same
3.1.4 Constant Acceleration Method 2001.2, Test condition E 30,000 G stress level	Not done Unless Specified
3.1.5 Visual Inspection Visual inspection for catastrophic failures after screens	Same
3.1.6 Seal Method 1014.2 (a) Helium fine leak - Test condition A_1. Bomb condition 2 hours at 60 psig. Reject limit $5x10^{-8}$ torr	Same
(b) Fluorocarbon gross leak - Test condition C	Same
3.1.9 Interim (pre-burn-in) Electricals Per applicable device specification	Preburn-in test at 25°C. Must meet requirements of device data sheets.
3.1.10 Burn-in Test Method 1015.2 160 hours @ 125°C	Same
3.1.13 Interim (Post burn-in) electricals Per applicable device specification	Burn-in equipment isolate failures automatically to assure no harmful interaction.
3.1.15 Final Electrical Test (a) Static Tests (1) 25°C (2) Minimum and Maximum Operating Temperatures (b) Dynamic and Switching Tests at 25°C (c) Functional Tests at 25°C	Same
3.1.17 Qualification or Quality Conformance Inspection and Test Sample Selection	Not done unless specified using method 5005 as a guide.
3.1.18 External Visual Method 2009.2	Same

WESTERN DIGITAL RELIABILITY ENHANCEMENT OPTIONS

100% Temperature Testing

Level .....-40° to +85°C
.....-55° to +125°C

Thermal, Shock (Liquid to Liquid)

Level .....0° to +100°C, 15 cycles
.....-55° to +125°C
.....-65° to +150°C

Extended High Temperature Storage

+150°C for 24 hours standard, other time/temperature storage requirements available required.

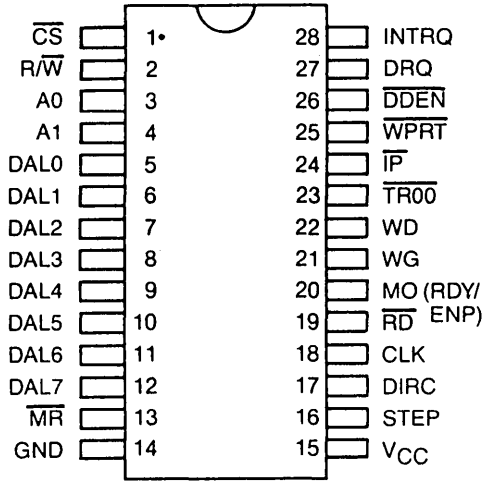
Dynamic Burn-In

Per note previously supplied.

WD177X-00 Floppy Disk Formatter/Controller

FEATURES

- 28 PIN DIP
- SINGLE 5V SUPPLY
- BUILT-IN DIGITAL DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- SINGLE (FM) AND DOUBLE (MFM) DENSITY
- MOTOR CONTROL (WD1770 AND WD1772)
- 128, 256, 512 OR 1024 SECTOR LENGTHS
- TTL COMPATIBLE
- 8-BIT BI-DIRECTIONAL DATA BUS
- TWO VERSIONS AVAILABLE
  WD1770/WD1773 = STANDARD 179X STEP RATES
  WD1772 = FASTER STEP RATES
- THE WD1773 HAS 100% COMPATIBLE SOFTWARE WITH THE WD1793



DIP PIN DESIGNATION

GENERAL DESCRIPTION

The WD177X-00 is a MOS/LSI device which performs the functions of a Floppy Disk Formatter/Controller. It is similar to its predecessor, the FD179X, but also contains a digital data separator and write precompensation circuitry. The drive side of the interface needs no additional logic except for buffers/receivers. It is designed for single (FM) or double (MFM) density operation.

The WD177X-00 is implemented in NMOS silicon gate technology and is available in a 28-pin dual-in-line as well as in quad pack.

Three versions of the WD177X-00 are available. The WD1770, WD1772 and the WD1773.

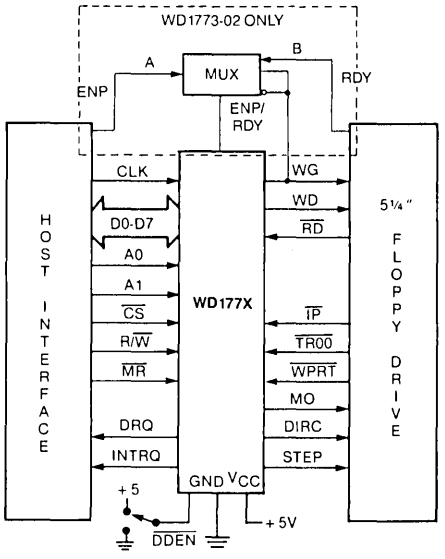
With the exception of the enable precomp/ready line, the WD1773 is identical to the WD1770 controller. It is fully software compatible with the WD1793. The WD1770-00 and WD1773-00 are compatible with the FD179X stepping rates, while the WD1772-00 offers stepping rates of 2, 3, 6, and 12 msec.

The WD177X-00 devices all contain a built-in digital data separator which virtually eliminates all external components and adjustments associated with data recovery in previous designs. A single read line (RD, Pin 19) is the only input required to recover serial FM or MFM data from the disk drive. The device is designed for control of floppy disk drives with data rates of 125 KBits/Sec (single density) and 250 KBits/Sec (double density). In addition, write precompensation of 125 nsec from nominal is enabled at any point through simple software commands. Another programmable feature on the WD1770/WD1772 is Motor On, which enables the spindle motor automatically prior to operating a selected drive.

The processor interface consists of an 8-bit bi-directional bus for transfer of status, data, and commands. All Host communication with the drive occurs through these lines. They are capable of driving one standard TTL load or three LS loads.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	A logic low on this input selects the chip and enables Host communication with the device.
2	R/$\overline{W}$	READ/$\overline{WRITE}$	I	A logic high on this input controls the placement of data on the D0-D7 lines from a selected register, while a logic low causes a write operation to a selected register.
3,4	A0,A1	ADDRESS 0,1	I	These two inputs select a register to Read/Write data: $\overline{CS}$ A1 A0 R/$\overline{W}$ = 1 R/$\overline{W}$ = 0 0 0 0 Status Reg Commad Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
5-12	DAL0-DAL7	DATA ACCESS LINES 0 THROUGH 7	I/O	Eight-bit bi-directional bus used for transfer of data, control, or status. This bus is enabled by $\overline{CS}$ and R/$\overline{W}$. Each line will drive one TTL load.
13	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	A logic low pulse on this line resets the device and initializes the Status Register (internal pull-up).
14	GND	GROUND		Ground.
15	V_{CC}	POWER SUPPLY	I	+5V ± 5% power supply input.
16	STEP	STEP	O	The Step output contains a pulse for each step of the drive's R/W head. The WD1770-00 and WD1772-00 offer different step rates.
17	DIRC	DIRECTION	O	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
18	CLK	CLOCK	I	This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHz +0.1%.
19	$\overline{RD}$	$\overline{READ\ DATA}$	I	This active low input is the raw data line containing both clock and data pulses from the drive.
20	RDY/ENP	READY/ENABLE PRECOMP (WD1773)	I	Serves as a READY input from the drive during READ/STEP operations and as a Write Precomp enable during Write operations. The state of READY is latched upon WG true, and this dual input is used for precompensation enable.
20	MO	MOTOR ON (WD1770 or WD-1772)	O	Active high output used to enable the spindle motor prior to read, write or stepping operations. (WD1770, WD1772 only)
21	WG	WRITE GATE	O	This output is made valid prior to writing on the diskette.
22	WD	WRITE DATA	O	FM or MFM clock and data pulses are placed on this line to be written on the diskette.
23	$\overline{TR00}$	$\overline{TRACK\ 00}$	I	This active low input informs the WD1770-00 that the drive's R/W heads are positioned over Track zero.
24	$\overline{IP}$	$\overline{INDEX\ PULSE}$	I	This active low input informs the WD1770-00 when the physical index hole has been encountered on the diskette.
25	$\overline{WPRT}$	$\overline{WRITE\ PROTECT}$	I	This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing (internal pull-up).

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
26	$\overline{\text{DDEN}}$	$\overline{\text{DOUBLE}}$ $\overline{\text{DENSITY}}$ $\overline{\text{ENABLE}}$	I	This input pin selects either single (FM) or double (MFM) density. When $\overline{\text{DDEN}}$ = 0, double density is selected (internal pull-up).
27	DRQ	DATA REQUEST	O	This active high output indicates that the Data Register is full (on a Read) or empty (on a Write operation).
28	INTRQ	INTERRUPT REQUEST	O	This active high output is set at the completion of any command, is reset by a read of the Status Register.



WD177X-02 SYSTEM BLOCK DIAGRAM

ARCHITECTURE

The primary sections of the Floppy Disk Formatter are the Parallel Processor Interface and the Floppy Disk Interface.

Data Shift Register – This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RD}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register – This 8-bit register is used as a holding register during Disk Read and Write operations. In disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek Command, the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register is not loaded when the device is busy.

Sector Register (SR) – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register is not loaded when the device is busy.

Command Register (CR) – This 8-bit register holds the command presently being executed. This register is not loaded when the device is busy unless the new command is a force interrupt. The Command Register is loaded from the DAL, but not read onto the DAL.

Status Register (STR) – This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register is read onto the DAL, but not loaded from the DAL.

CRC Logic – This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is:
$G(x) = x^{16} + x^{12} + x^5 + 1$.
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC Register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

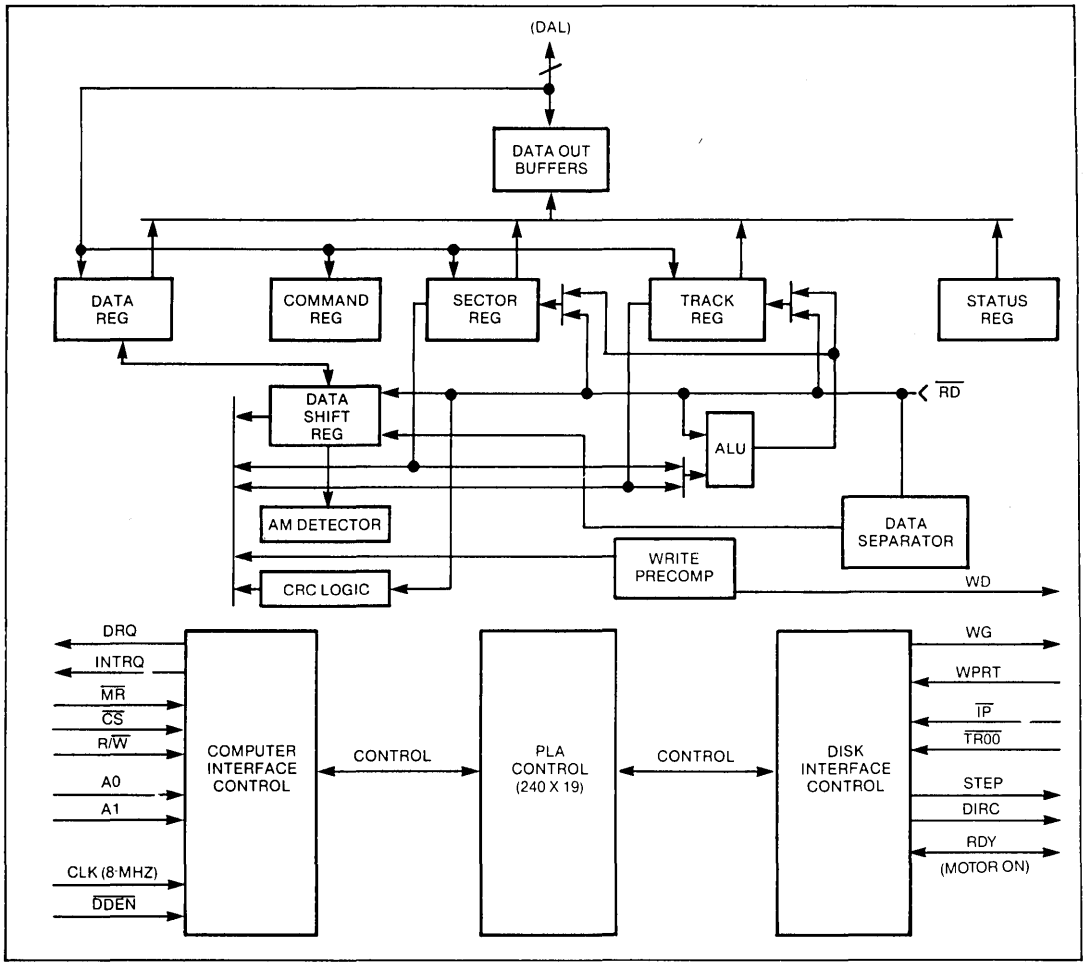


FIGURE 1. WD177X-00 BLOCK DIAGRAM

Timing and Control – All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The WD177X-00 has two different modes of operation according to the state of DDEN.

When $\overline{DDEN}$ = 0, double density (MFM) is enabled. When DDEN = 1, single density is enabled.

AM Detector – The address mark detector detects ID, data and index address marks during read and write operations.

Data Separator – A digital data separator consisting of a ring shift register and data window detection logic provides read data and a recovery clock to the AM detector.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD177X-00. The DAL are three state buffers that are enabled as output drivers when $\overline{CS}$ and R/$\overline{W}$ = 1 are active or act as input receivers when $\overline{CS}$ and R/$\overline{W}$ = 0 are active.

When transfer of data with the Floppy Disk Controller is required by the Host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signal R/$\overline{W}$ during a Read operation or Write operation are interpreted as selecting the following registers:

A1 - A0	READ (R/$\overline{W}$ = 1)	WRITE (R/$\overline{W}$ = 0)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

After any register is written to, the same register cannot be read from until 16 μsec in MFM or 32 μsec in FM have elapsed.

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD177X-00 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request bit is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operations continue until the end of sector is reached.

On Disk Write operations the Data Request bit is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the Status Register or by loading the Command Register with a new command. In addition, INTRQ is generated if a Force Interrupt Command condition is met.

The WD177X-00 has two modes of operation according to the state $\overline{DDEN}$. When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input is at 8 MHz.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ is placed to a logical 1. For MFM formats, $\overline{DDEN}$ is placed to a logical 0. Sector lengths are determined at format time by the fourth byte in the ID field.

SECTOR LENGTH TABLE	
SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

The number of sectors per track for the WD177X-00 are from 1 to 240. The number of tracks for the WD177X-00 are 0 to 240.

GENERAL DISK WRITE OPERATION

When writing on the diskette the WG output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte is loaded into the Data Register in response to a Data Request from the device before the WG is activated.

Writing is inhibited when the $\overline{WPRT}$ input is asserted, in which case any Write Command is immediately terminated, an interrupt is generated and the Write Protect Status bit is set.

For Write operations, the WD177X-00 provides WG to enable a Write condition, and WD which consists of a series of active high pulses. These pulses contain both Clock and Data information in FM and MFM. WD provides the unique missing clock patterns for recording Address Marks.

The WD1773-00 enables write precompensation when RDY/ENP is asserted. When WG is asserted the READY status has been latched. WG is then used to demultiplex drive Ready Status from Host supplied enable for write precompensation at desired tracks.

On the WD1770-02 or WD1772-00, the Precomp Enable bit in Write Commands allows automatic Write precompensation to take place. The outgoing Write Data stream is delayed or advanced from nominal by 125 nsec according to the following table:

PATTERN				MFM	FM
X	1	1	0	Early	N/A
X	0	1	1	Late	N/A
0	0	0	1	Early	N/A
1	0	0	0	Late	N/A

Next Bit to be sent
Current Bit sending
Previous Bits sent

Precompensation is typically enabled on the innermost tracks where bit shifts usually occur and bit density is at its maximum. READY is true for read/write operations (all Type II and III Command executions).

COMMAND DESCRIPTION

The WD177X-00 accepts 11 commands. Command words are only loaded in the Command Register when the Busy Status bit is off (Status bit 0). The one exception is the Force Interrupt Command. Whenever a command is being executed, the Busy Status bit is set. When a command is completed, an interrupt is generated and the Busy Status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. Commands are divided into four types and are summarized in the following pages.

COMMAND SUMMARY

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step-in	0	1	0	u	h	V	r_1	r_0
I	Step-out	0	1	1	u	h	V	r	r_0
II	Read Sector	1	0	0	m	h/s	E	0/C	0
II	Write Sector	1	0	1	m	h/s	E	P/C	a_0
III	Read Address	1	1	0	0	h/o	E	0	0
III	Read Track	1	1	1	0	h/o	E	0	0
III	Write Track	1	1	1	1	h/o	E	P/O	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TYPE I COMMANDS

h = Motor On Flag (Bit 3) (1770/2).

h = 0, Enable Spin-up Sequence
h = 1, Disable Spin-up Sequence

V = Verify Flag (Bit 2) (1770/2/3)

V = 0, No Verify
V = 1, Verify on Destination Track

r_1, r_0 = Stepping Rate (Bits 1,0)

r_1	r_0	WD1770-00 WD1773-00	WD1772-00
0	0	6 ms	6 ms
0	1	12 ms	12 ms
1	0	20 ms	2 ms
1	1	30 ms	3 ms

u = Update Flag (Bit 4) (1770/2/3)

u = 0, No Update
u = 1, Update Track Register

TYPE II & III COMMANDS

m = Multiple Sector Flag (Bit 4) (1770/2/3)

m = 0, Single Sector
m = 1, Multiple Sector

H = Motor on Flag (Bit 3) (1770/2)

H = 0, Enable Spin-up Sequence
H = 1, Disable Spin-up Sequence

S = Side Compare Flag (Bit 3) (1773 only)

S = 0, Compare for side 0
S = 1, Compare ;for side 1
For all Type III commands bit 3 must be 0.

a_0 = Data Address Mark (Bit 0) (1770/2/3)

a_0 = 0, Write Normal Data Mark
a_0 = 1, Write Deleted Data Mark

TYPE II & III COMMANDS (Continued)

E = 30ms Settling Delay (Bit 2) (1770/2/3)

E = 0, No Delay
E = 1, Add 30ms Delay (1772 Add 15ms Delay*

C = Side Compare Flag (Bit 1) (1773 only)

C = 0, Disable Side Compare
C = 1, Enable Side Compare
For all Type III commands bit 1 must be 0.

P = Write Precompensation (Bit 1) (1770/2/3)

P = 0,Enable Write Precomp
P = 1,Disable Write Precomp

TYPE IV COMMANDS

I_3-I_0 Interrupt Condition (Bits 3-0)

I_0 = Not Used (WD1770-00, WD1772-00)
Not Ready to Ready Transition (WD1773-00)
I_1 = Not Used (WD1770-00, WD1772-00)
Ready to Not Ready Transition (WD1773-00)
I_2 = Interrupt on Index Pulse
I_3 = Immediate Interrupt
I_3-I_0 = Terminate without interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out Commands. Each of the Type I Commands contains a rate field (r_0,r_1), which determines the stepping motor rate.

A 4 μsec (MFM) or 8 μsec (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip steps the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 24 μsec before the first stepping pulse is generated.

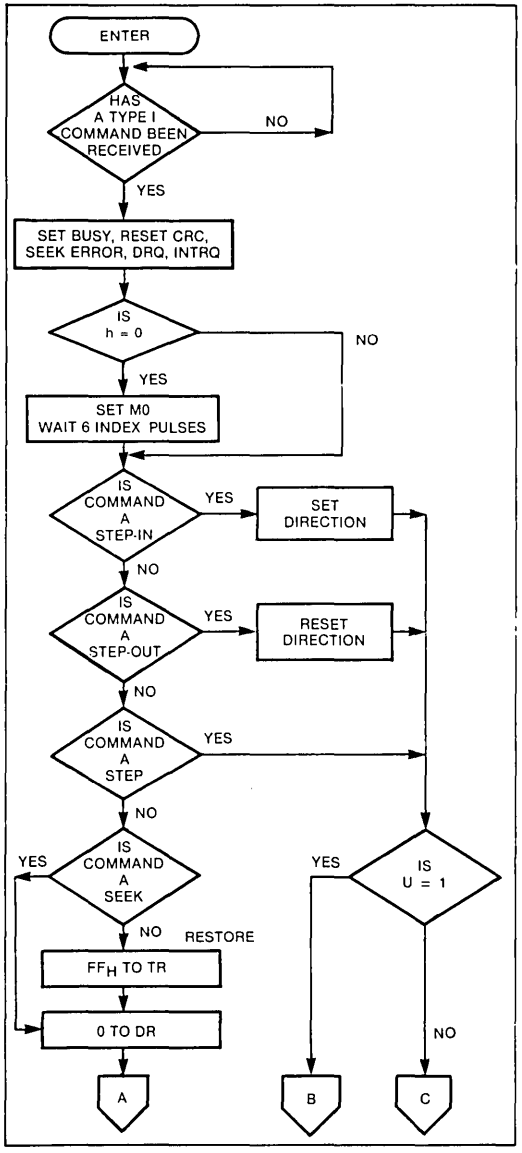
After the last directional step an additional *30 msec of head settling time takes place if the Verify flag is set in Type I Commands. There is also a *30 msec head settling time if the E flag is set in any Type II or III Command.

When a Seek, Step or Restore Command is executed, an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the *30 msec settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field CRC is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not

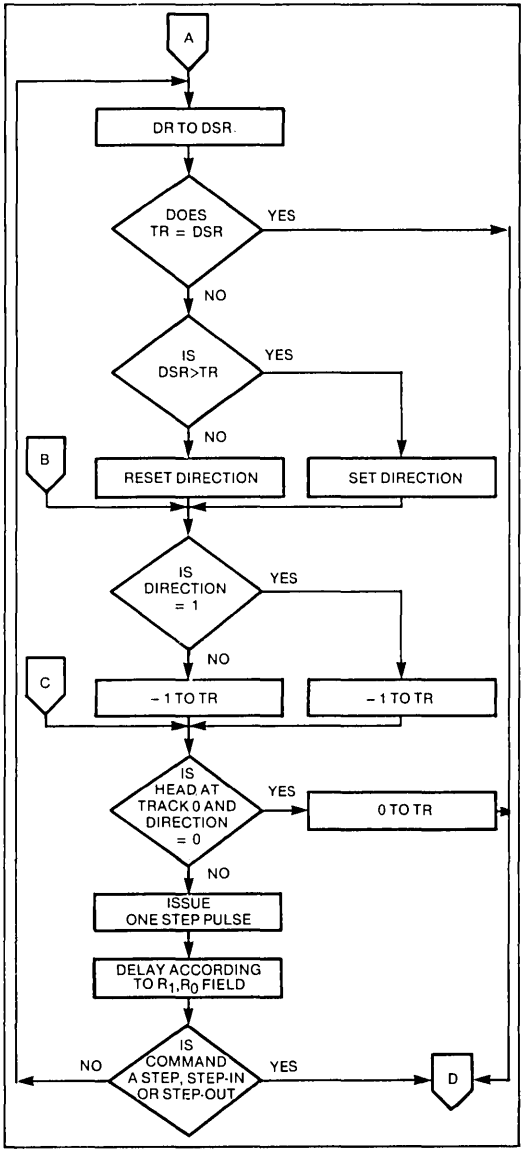
a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID Field is read from the disk for the verification operation.

The WD177X-00 finds an ID Field with correct track number and correct CRC within 5 revolutions of the media, or the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

On the WD1770-00 and WD1772-00 only, all commands, except the Force Interrupt Command, are programmed via the h Flag to delay for spindle motor start up time. If the h Flag is not set and the MO signal is low when a command is received, the WD1770/2-00 forces MO to a logic 1 and waits 6 revolutions before executing the command. At 300 RPM, this guarantees a one second spindle start up time. If after finishing the command, the device remains idle for 9 revolutions, the MO signal goes back to a logic 0. If a command is issued while MO



TYPE I COMMAND FLOW



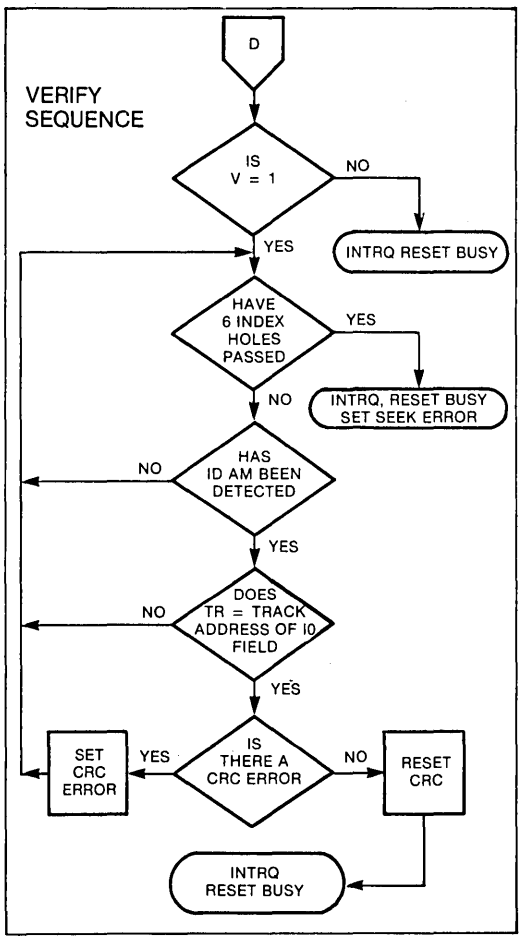
TYPE I COMMAND FLOW

is high, the command executes immediately, defeating the 6 revolution start up. This feature allows consecutive Read or Write commands without waiting for motor start up each time; the WD1770/2-00 assumes the spindle motor is up to speed.

RESTORE (SEEK TRACK 0)

Upon receipt of this command, the Track 00 (TR00) input is sampled. If TR00 is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If TR00 is not active low, stepping pulses at a rate specified by the r_1,r_0 field are issued until the TR00 input is activated.

At this time, the Track Register is loaded with zeroes and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the WD177X-00 terminates operation, interrupts, and sets the Seek Error status bit, providing the V flag is set.



TYPE I COMMAND FLOW

A verification operation also takes place if the V flag is set. The h bit allows the Motor On option at the start of a command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD177X-00 updates the Track Register and issues stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the Track Register is updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the WD177X-00 issues one Stepping Pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD177X-00 issues one Stepping Pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

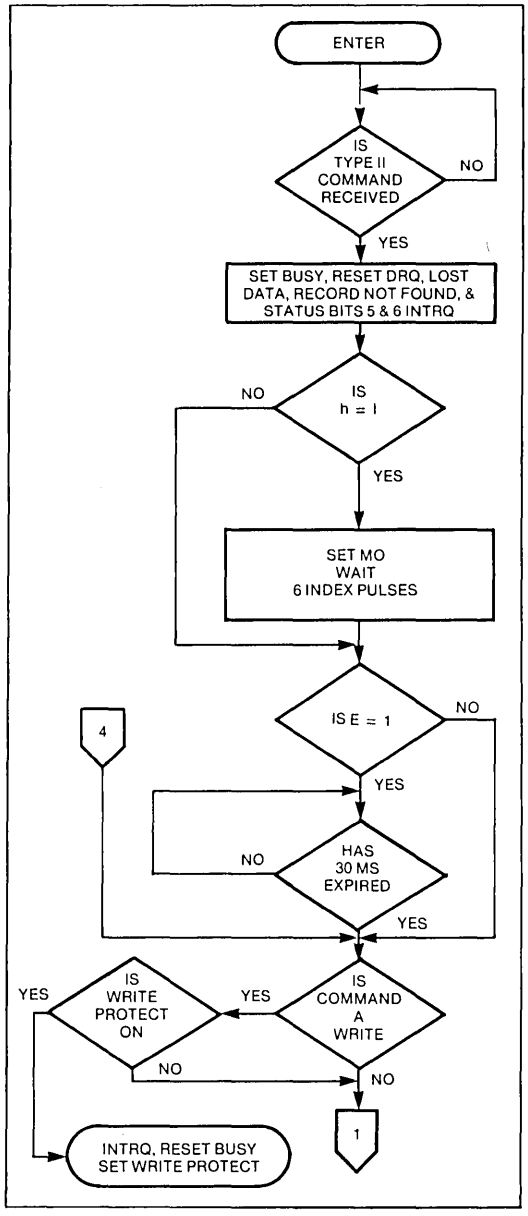
STEP-OUT

Upon receipt of this command, the WD177X-00 issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer loads the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy Status bit is set. If the E flag = 1 the command executes after a 30 msec delay.

When an ID field is located on the disk, the WD177X-00 compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the Sec-



TYPE II COMMAND

tor Number of the ID field is compared with the Sector Register. If there is no Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is located and is either written into, or read from, depending upon the command. The WD177X-00 finds an ID field with a Track number, Sector number, and CRC within four revolutions of the disk, or, the Record Not Found Status bit is set (Status Bit 4) and the command is terminated with an INTRQ.

Each of the Type II Commands contains an m flag which determines if multiple records (sectors) are read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification occurs on the next record. The WD177X-00 continues to read or write multiple records and updates the Sector Register in numerical ascending sequence until the Sector Register exceeds the number of sectors on the track or until the Force Interrupt Command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the WD177X-00 is instructed to read sector 27 and there are only 26 on the track, the Sector Register exceeds the number available. The WD177X-00 searches for 5 disk revolutions, interrupts out, resets Busy, and sets the Record Not Found Status Bit.

READ SECTOR

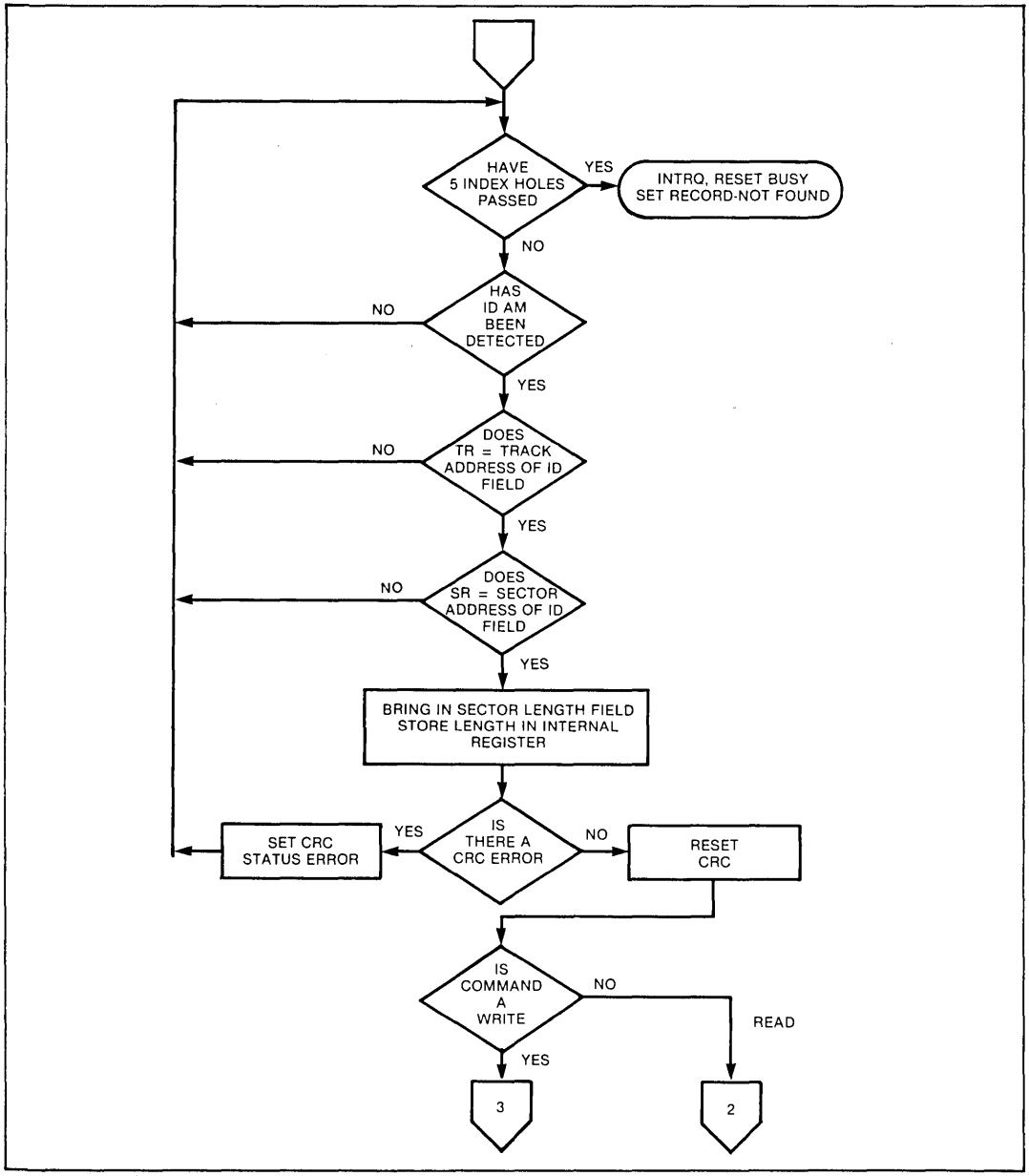
Upon receipt of the Read Sector Command, the Busy Status Bit is set, then when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field is found with 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte. If not, the ID field is searched for and verified again followed by the Data Address Mark search. If, after five revolutions the DAM is not found, the Record Not Found Status Bit is set and the operation is terminated. When the first character or byte of the data field is shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status Bit is set. This sequence continues until the complete data field is inputted to the computer. If there is a CRC error at the end of the data field, the CRC Error Status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector Command, the Busy Status Bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The WD177X-00 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the WG

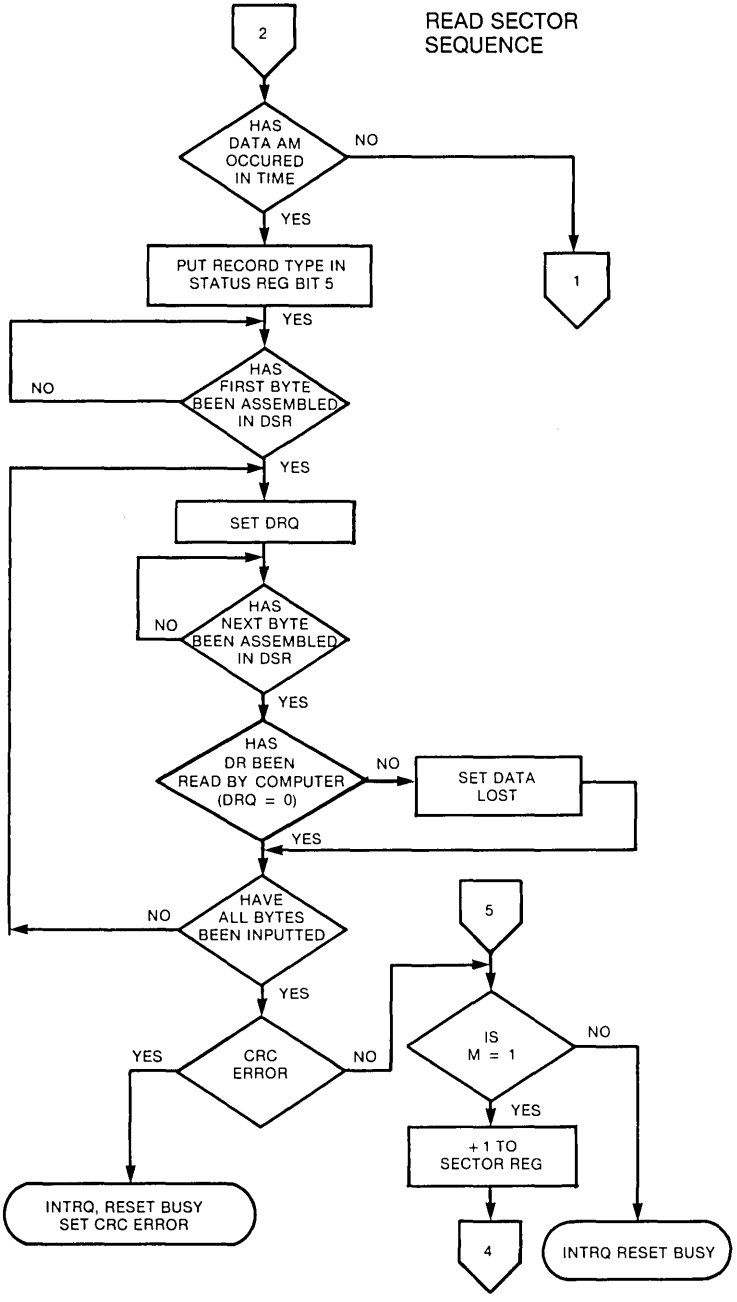


TYPE II COMMAND

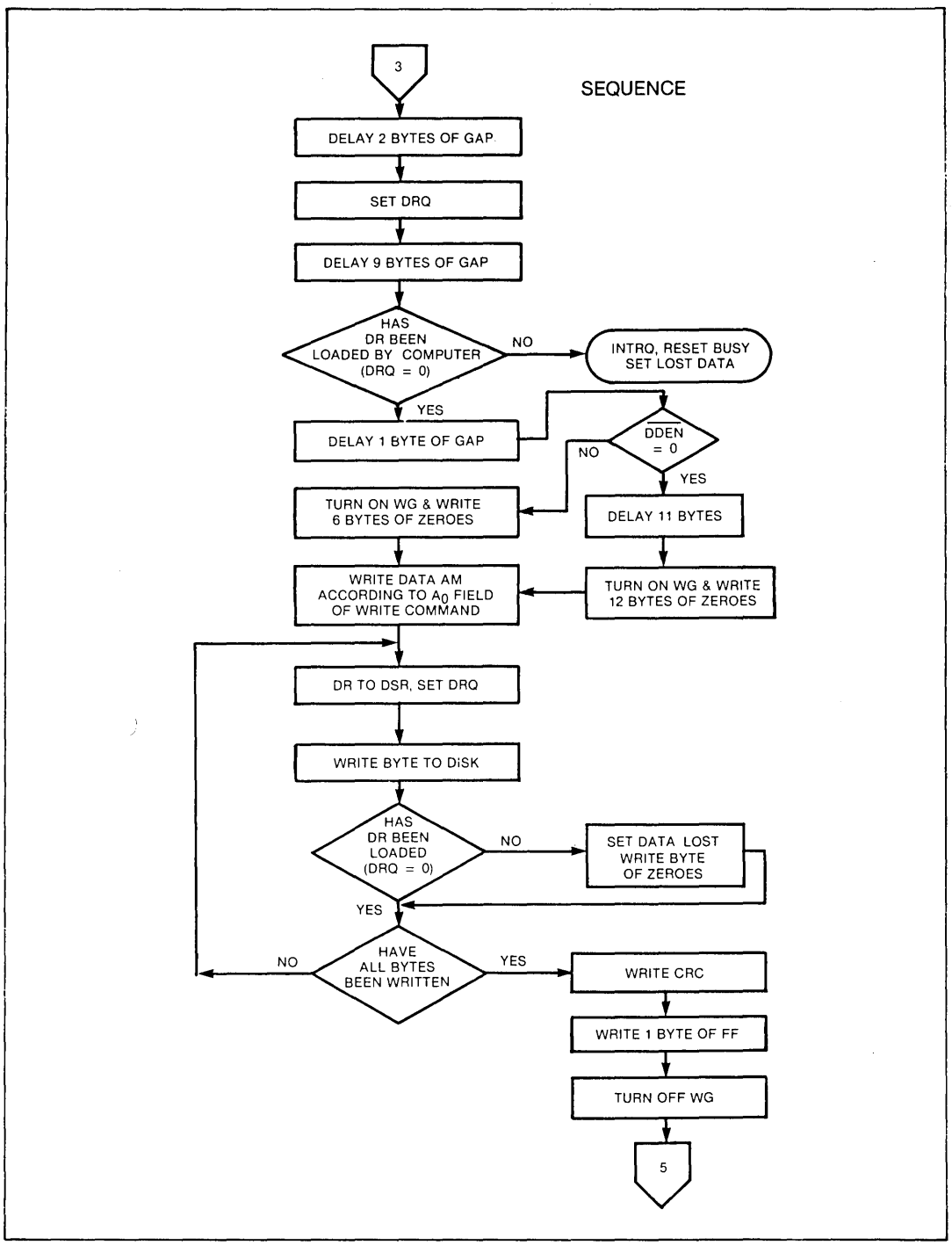
output is made active if the DRQ is serviced (i.e., the DR is loaded by the computer). If DRQ is not serviced, the command is terminated and the Lost Data Status Bit is set. If the DRQ is serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are written on the disk. The Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown:

a_0	DATA ADDRESS MARK (BIT 0)
1	Deleted Data Mark
0	Data Mark

The WD177X-00 writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status



TYPE II COMMAND



TYPE II COMMAND

Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte is written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. INTRQ sets 24 μsec (MFM) after the last CRC byte is written. For partial sector writing, the proper method is to write data and fill the balance with zeroes.

TYPE III COMMANDS

Read Address

Upon receipt of the Read Address Command, the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown:

TRACK ADDR	SIDE NUMBER	SECTOR ADDR	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the WD177X-00 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

Read Track

Upon receipt of the Read Track Command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; and the Address Mark Detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM.

The ID AM, ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector are correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on TYPE III commands for flow diagrams.)

Data and gap information are provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track Command.

Upon receipt of the Write Track Command, the Busy Status Bit is set. Writing starts with the leading edge of the first encountered Index Pulse and continues until the next Index Pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing does not start until after the first byte is loaded into the Data Register. If the DR is not loaded within three byte times, the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

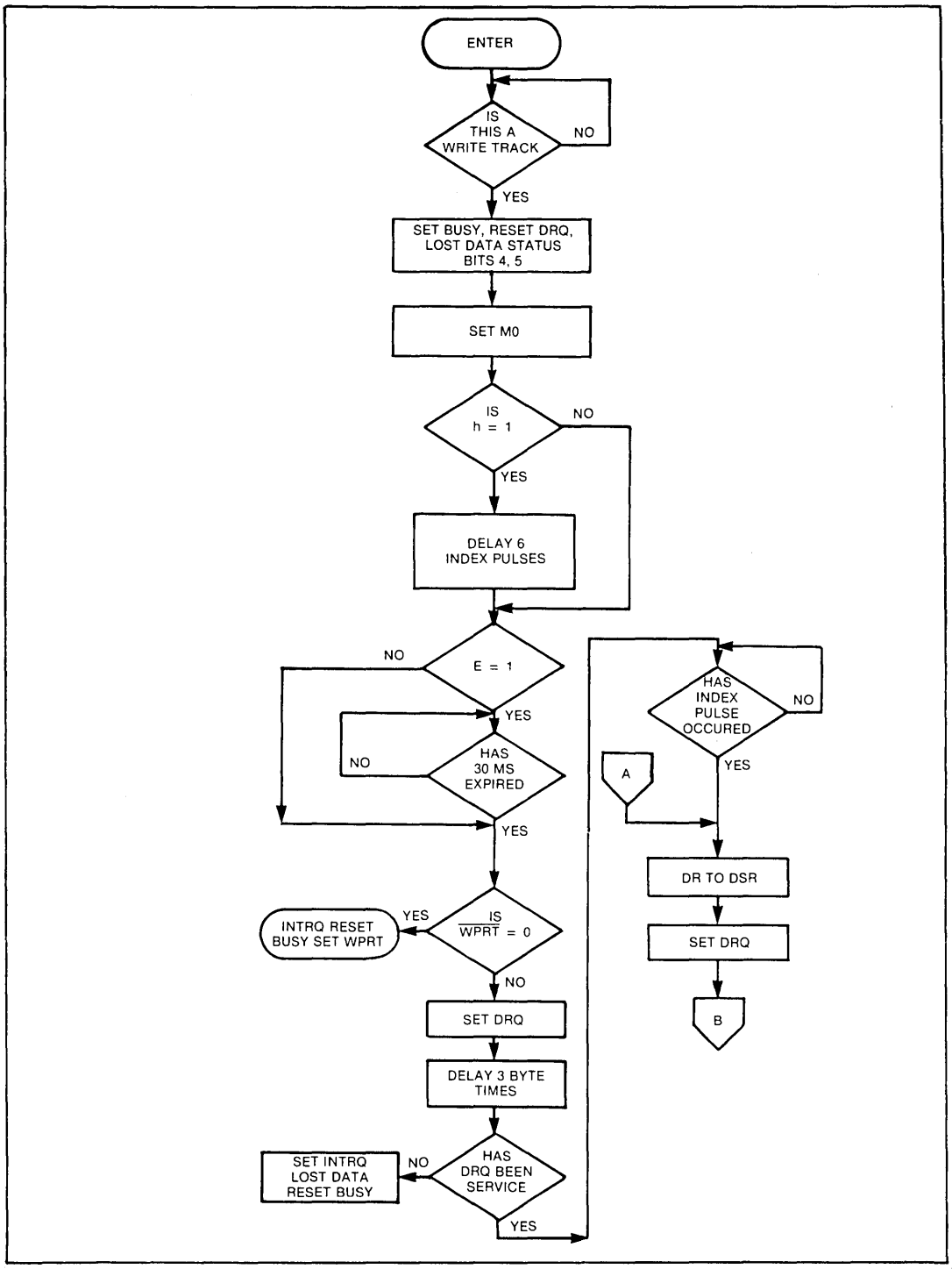
This sequence continues from one Index Pulse to the next. Normally whatever data pattern appears in the Data Register is written on the disk with a normal clock pattern. However, if the WD177X-00 detects a data pattern of F5 through FE in the Data Register, this is interpreted as Data Address Marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern generates two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE do not appear in the gaps, data field, or ID fields. Also, CRC's are generated by an F7 pattern.

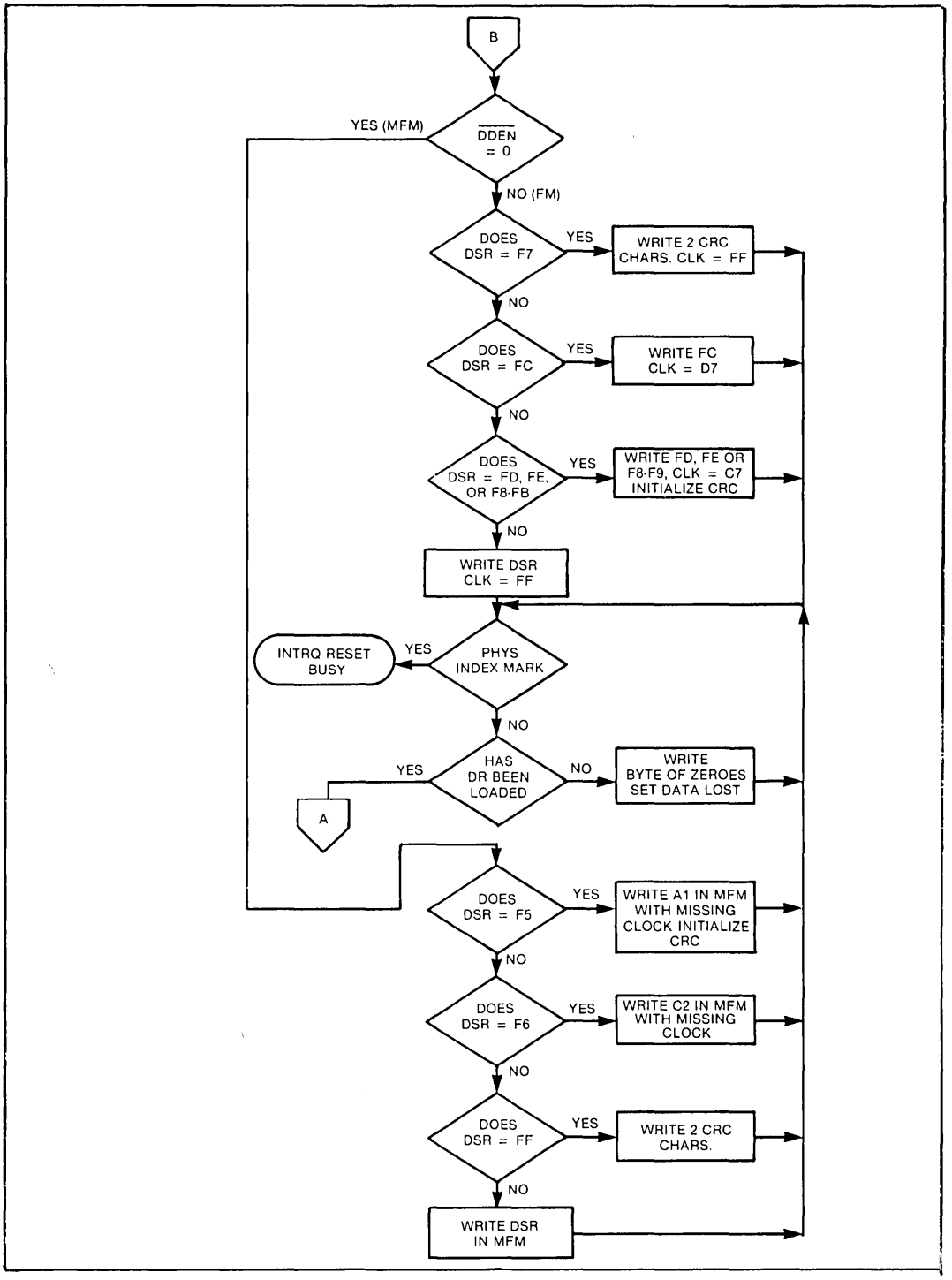
Disks are formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

DATA PATTERN IN DR (HEX)	IN FM ($\overline{\text{DDEN}}$ = 1)	IN MFM ($\overline{\text{DDEN}}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Present CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5.
**Missing clock transition between bits 3 and 4.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

TYPE IV COMMANDS

The Forced Interrupt Command is used to terminate a multiple sector read or write command or to insure Type I status in the Status Register. This command is loaded into the Command Register at any time. If there is a current command under execution (Busy Status Bit set) the command is terminated and the Busy Status Bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not used (WD1770-00, WD1772-00), Not Ready To Ready Transition (WD1773-00)
I_1 = Not Used (WD1770-00, WD1772-00), Ready To Not Ready Transition (WD1773-00)
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3-I_0) are set to a 1. When the condition for interrupt is met the INTRQ line goes high signifying that the condition specified has occurred. If I_3-I_0 are all set to zero (Hex D0), no interrupt occurs but any command presently under execution is immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt is immediately generated and the current command terminated. Reading the status or writing to the Command Register does not automatically clear the interrupt. The Hex D0 is the only command that enables the immediate interrupt (Hex D8) to clear on a subsequent load Command Register or Read Status Register operation. Follow a Hex D8 with D0 command.

Wait 16 μsec (double density) or 32 μsec (single density) before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this nullifies the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt waits until ALU operations in progress are complete (CRC calculations, compares, etc.).

Status Register

Upon receipt of any command, except the Force Interrupt Command, the Busy Status Bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy Status Bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt Command is received when there is not a current command under execution, the Busy Status Bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the Status Register through program control or using the DRQ line with DMA or interrupt methods. When the Data Register is read the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes both DRQ's to reset.

The Busy Bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a Busy Status check is not recommended because a read of the Status Register to determine the condition of busy resets the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Because of internal sync cycles, certain time delays are observed when operating under programmed I/O, as shown.

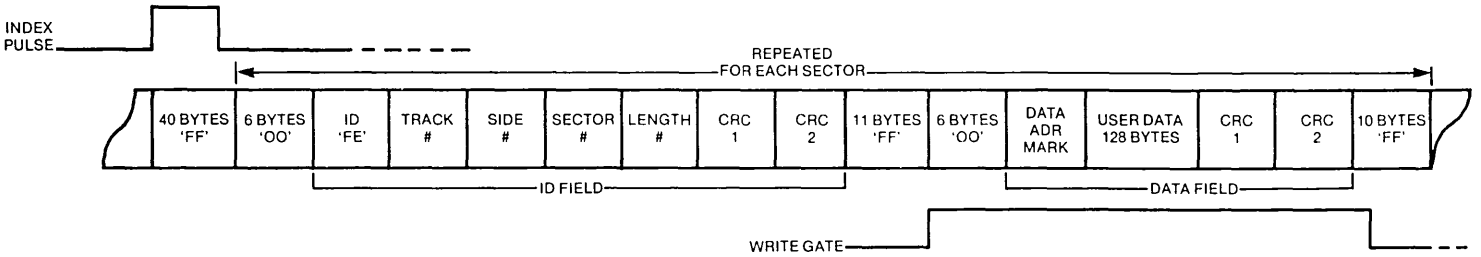
Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	48μsec	24μsec
Write to Command Reg.	Read Status Bits 1-7	64μsec	32μsec
Write Register	Read Same Register	32μsec	16μsec

RECOMMENDED - 128 BYTES/SECTOR

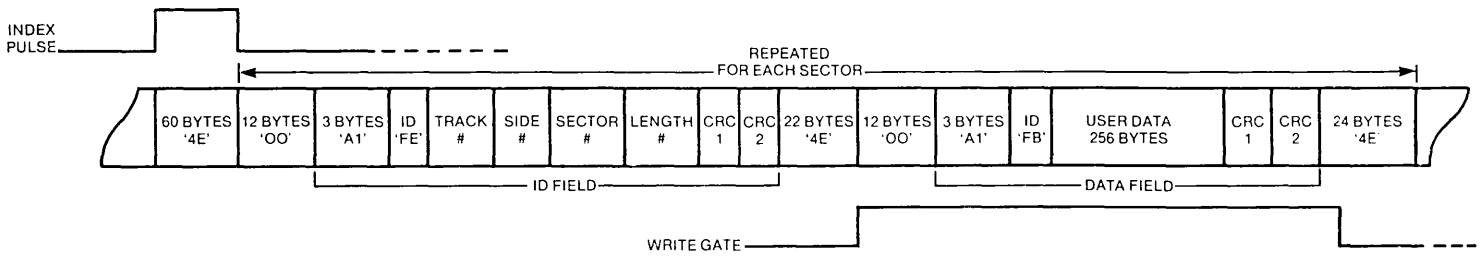
The recommended single-density format with 128 bytes/sector is shown. In order to format a diskette, the user issues the Write Track Command, and loads the Data Register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 10)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
10	FF (or 00)
369**	FF (or 00)

*Write bracketed field 16 times.
**Continue writing until WD177X-00 interrupts out. Approx. 369 bytes.



SINGLE DENSITY FORMAT



DOUBLE DENSITY FORMAT

256 BYTES/SECTOR

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user issues the Write Track Command and loads the Data Register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
60	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 10)
1	01 (Sector Length)
1	F7 (2 CRC's written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (Data Address Mark)
24	4E
668**	4E

*Write bracketed field 16 times.
**Continue Writing until WD177X-00 interrupts out. Approx. 668 bytes.

1. Non-Standard Formats

Variations in the recommended formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.
2) Gap 2 cannot be varied from the recommended format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the WD177X-00. Gap 1, 3 and 4 lengths are as short as 2 bytes for WD177X-00 operation, however PLL lock up time, motor speed variation, write-splice area, etc. adds more bytes to each gap to achieve proper operation. For highest system reliability use the recommended format.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

STATUS REGISTER DESCRIPTION (WD1770-00 and WD1772-00 only)

BIT NAME	MEANING
S7 MOTOR ON	This bit reflects the status of the Motor On output.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/SPIN-UP	When set, this bit indicates that the Motor Spin-Up sequence has completed (6 revolutions) on Type I commands. Type 2 & 3 commands, this bit indicates record Type. 0 = Data Mark. 1 = Deleted Data Mark.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error data field. This bit is reset when updated.
S2 LOST DATA/ BYTE	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. On Type I commands, this bit reflects the status of the TR00 signal.
S1 DATA REQUEST INDEX	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. On Type 1 commands, this bit indicates the status of the IP signal.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

STATUS REGISTER SUMMARY (WD1773-00 only)

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS (WD1773-00 only)

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically "ORed" with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set, command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS (WD1773-00 ONLY)

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and "ORed" with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a Zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desire track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

DC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Storage Temperature .....55°C (67°F) to +125°C (257°F)

Operating Temperature.....0°C (32°F) to 70°C (158°F) Ambient

Maximum Voltage to Any Input with Respect to V_{SS}.....+7V to -0.5V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

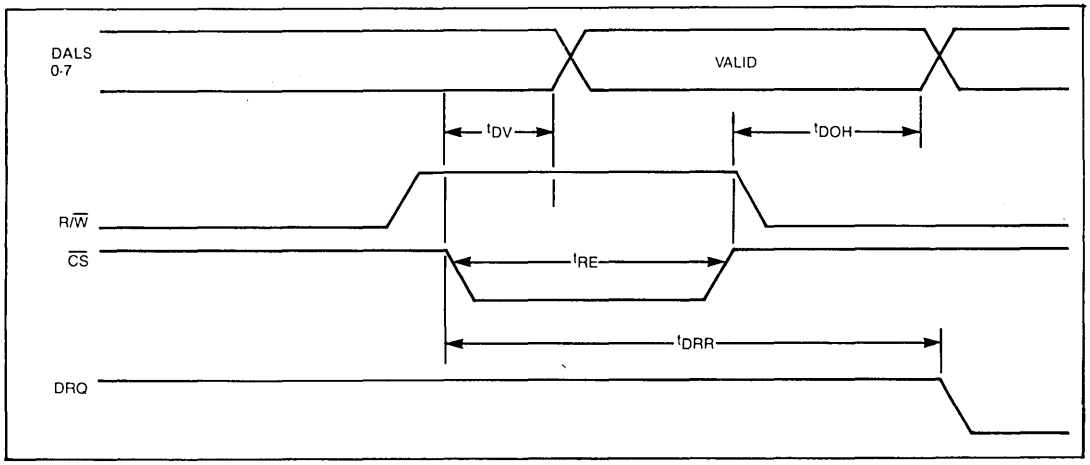
DC OPERATING CHARACTERISTICS

TA = 0°C(32°F) to 70°C (158°F), V_{SS} = OV, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IH}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_0 = -100 μA
V_{OL}	Output Low Voltage		0.40	V	I_0 = 1.6 mA
P_D	Power Dissipation		.75	W	
R_{PU}	Internal Pull-Up	100	1700	μA	V_{IN} = 0V
I_{CC}	Supply Current	75(Typ)	150	mA	

AC TIMING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F), ^{V}SS = 0V, ^{V}CC = +5V ± .25V

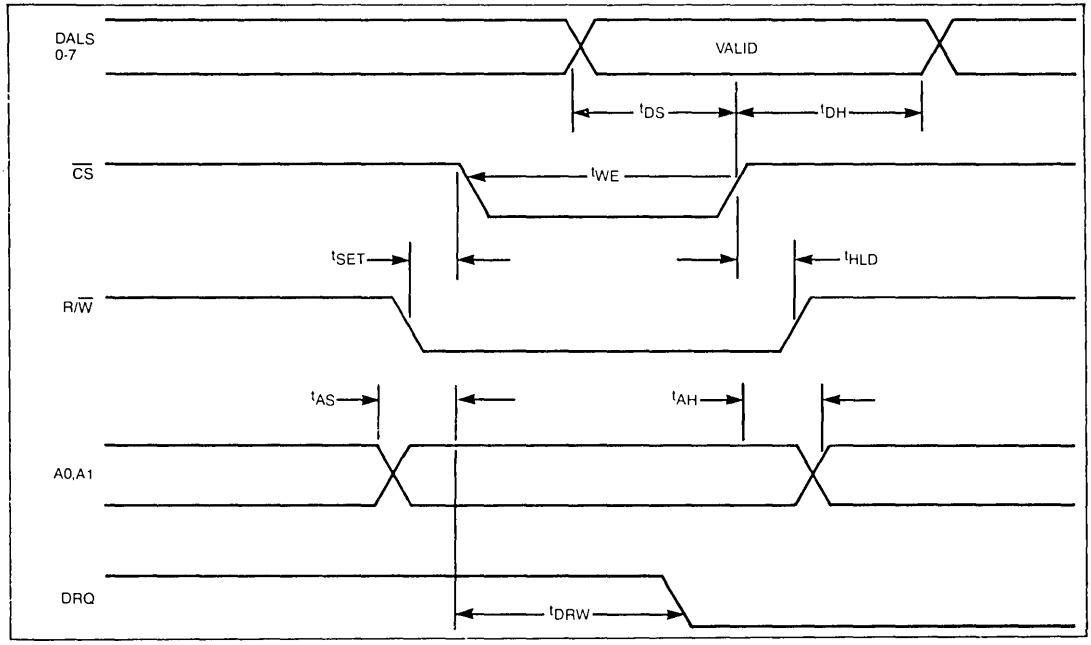


READ ENABLE TIMING

READ ENABLE TIMING – $\overline{RE}$ such that: R/$\overline{W}$ = 1, CS = 0.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RE}	$\overline{RE}$ Pulse Width of $\overline{CS}$	200			nsec	C_L = 50 pf
t_{DRR}	DRQ Reset from $\overline{RE}$		200	300	nsec	
t_{DV}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
t_{DOH}	Data Hold from $\overline{RE}$	20		150	nsec	C_L = 50 pf
	INTRQ Reset from $\overline{RE}$			8	μsec	

Note: DRQ and INTRQ reset are from rising edge (lagging) of $\overline{RE}$, whereas resets are from falling edge (leading) of $\overline{WE}$. Worst case service time for DRQ is 23.5 μsec for MFM and 47.5 μsec for FM.



WRITE ENABLE TIMING

WRITE ENABLE TIMING - $\overline{WE}$ such that: R/$\overline{W}$ = 0, $\overline{CS}$ = 0.

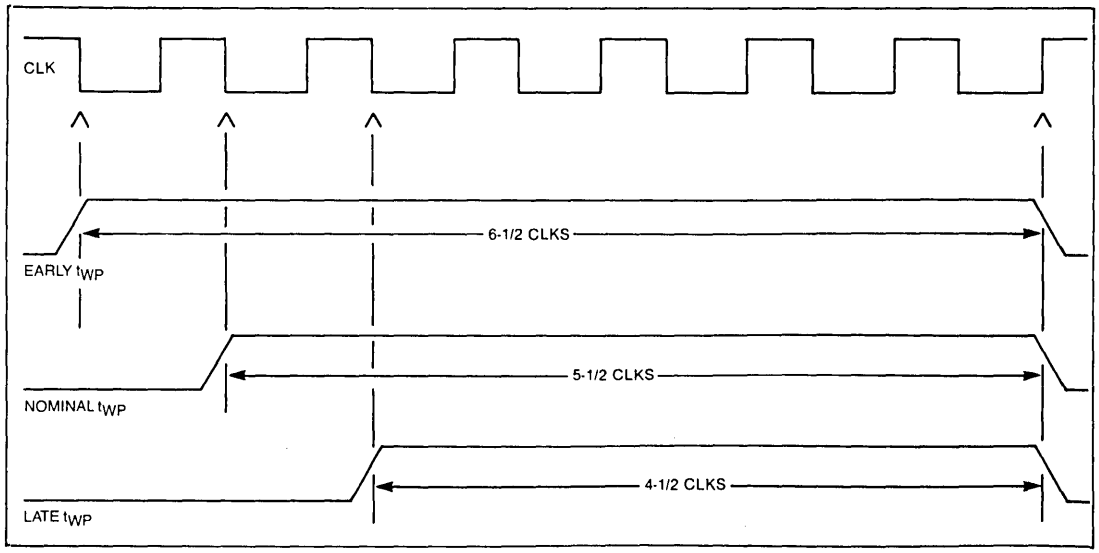
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{AS}	Setup ADDR to $\overline{CS}$	50			nsec	
t_{SET}	Setup R/$\overline{W}$ to $\overline{CS}$	0			nsec	
t_{AH}	Hold ADDR from $\overline{CS}$	10			nsec	
t_{HLD}	Hold R/$\overline{W}$ from $\overline{CS}$	0			nsec	
t_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
t_{DRW}	DRQ Reset from $\overline{WE}$		100	200	nsec	
t_{DS}	Data Setup to $\overline{WE}$	150			nsec	
t_{DH}	Data Hold from $\overline{WE}$	0			nsec	
	INTRQ Reset from $\overline{WE}$			8	μsec	

READ DATA TIMING:

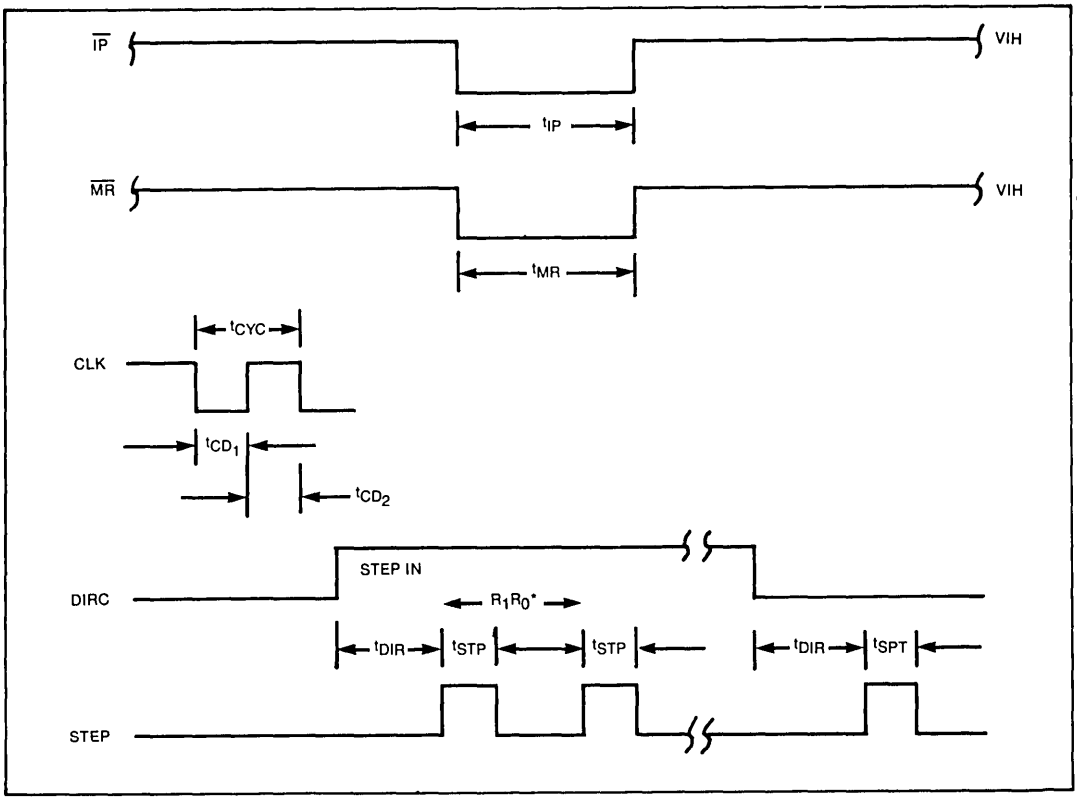
CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{\text{Raw Read}}$ Pulse Width	.200		3	μsec	MFM
	.400		3		FM
$\overline{\text{Raw Read}}$ Cycle Time	3			μsec	

WRITE DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
	Write Gate to Write Data		4		μsec	FM
			2		μsec	MFM
	Write Data Cycle Time		4,6,8		μsec	
	Write Gate off from WD		4		μsec	FM
			2		μsec	MFM
t_{WP}	Write Data Pulse Width		820		nsec	Early MFM
			690		nsec	Nominal MFM
			570		nsec	Late MFM
			1.38		μsec	FM



WRITE DATA TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{CD1}	Clock Duty (low)	50	67		nsec	
t_{CD2}	CLock Duty (high)	50	67		nsec	
t_{STP}	Step Pulse Output		4		µsec	MFM
			8			FM
t_{DIR}	Dir Setup to Step		24		µsec	MFM
			48			FM
t_{MR}	Master Reset Pulse Width	50			µsec	
t_{IP}	Index Pulse Width	20			µsec	

WD177X-00 Floppy Disk Formatter/Controller Family Application Notes

INTRODUCTION

To meet the demand for a low cost compact LSI Floppy Disk Controller device, Western Digital has developed the WD177X-00. The WD177X-00 is a NMOS Floppy Disk Controller device that incorporates the FD179X, a digital data separator and write precompensation circuitry all in a single chip. The device offers soft sector formatting, selectable stepping rates, automatic track seek with verify, and variable sector lengths. The FD177X-00 comes in a 28-pin dual-in-line package or quad pack and operates from a single 5 volt only power supply.

APPLICATIONS

The Mini-Floppy Controller is targeted for the low cost sector of the disk drive market, where digital data separation is preferred over analog phase lock loop. Included in this market are Personal Computers, Portable Computers and Small Business Computers.

FOLLOW ON DEVICES

WD1772-02

The device is the same as the WD1772-00 except for an enhanced digital data separator.

HOST INTERFACING

Interfacing to a Host processor is accomplished through the eight bit bi-directional Data Access Lines (DAL) and associated control lines. The DAL is used to transfer data, status and control words out of or into WD177X-00. The DAL having three states enabled as an output when Chip Select (CS) is active low and Read/Write (R/W) is high or as input receiver when CS and R/W is low. When transfer of data with the device is required by the Host CS is made low. The address bits A0 and A1 combined with the R/W line select the register and the direction of data.

During Direct Memory Access (DMA) data transfers between the WD177X-00 and Host Memory, the Data Request (DRQ) line is used in Data Transfer Control. This signal also appears as status bit 1 during Read/Write operations. On Disk Read operations the DRQ is active when an assembled byte is present in the Data Register, then reset when read by the Host. If the Host fails to read the Data Register before the following byte is assembled in the Data Register, the lost data bit is set in Status Register.

At the completion of every command INTRQ is asserted. INTRQ is de-asserted by either reading the status or by loading the Command Register.

DISKETTE DRIVE INTERFACING

The WD177X-00 has two modes of operation depending on the state of DDEN, regardless of the state of DDEN the CLK input remains at 8 MHz. Disk Reads with sector lengths of 128, 256, 512 and 1024 byte sector in both FM or MFM diskettes is accomplished via the internal digital data separator. Disk Write operation in MFM on inner tracks may require write precompensation. Write precompensation is enabled when bit 1 = 0, in the Write command and a precompensation value of 125 nsec is produced.

The diskettes spindle motor is controlled by bit 3 of any Type I, II or III command, upon receiving a command with bit 3 = 0, the spin up sequence is enabled.

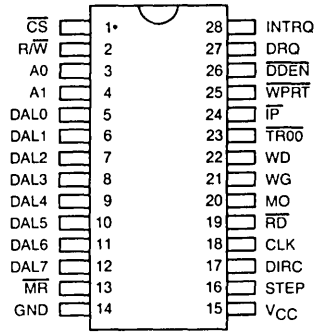
GENERAL INFORMATION

A +5 volt supply ±5% is used as V_{CC}, and the clock input requires a free running 50% duty cycle at 8 MHz ±0.1%.

WD1772-02 Floppy Disk Formatter/Controller

FEATURES

- 28 PIN DIP
- SINGLE 5V SUPPLY
- **HIGH PERFORMANCE DPLL BUILT-IN DIGITAL DATA SEPARATOR**
- BUILT-IN WRITE PRECOMPENSATION, INCREASED TO 187 MS
- SINGLE AND DOUBLE DENSITY
- MOTOR CONTROL
- 128, 256, 512 OR 1024 SECTOR LENGTHS
- TTL COMPATIBLE
- 8-BIT BI-DIRECTIONAL DATA BUS
- 100% PIN COMPATIBLE WITH WD1770-00 AND WD1772-00
- ENHANCED STEP/RATES 2,3,6,12 MS



PIN DESIGNATION

DESCRIPTION

The WD1772-02 is a MOS/LSI device which performs the functions of a Floppy Disk Formatter/Controller. It is similar to its predecessor, the FD179X, but also contains a digital data separator and write precompensation circuitry. The drive side of the interface needs no additional logic except for buffers/receivers. Designed for single (FM) or double (MFM) density operation, the device contains a programmable Motor On signal.

The WD1772-02 is implemented in NMOS silicon gate technology and is available in a 28 pin dual-in-line.

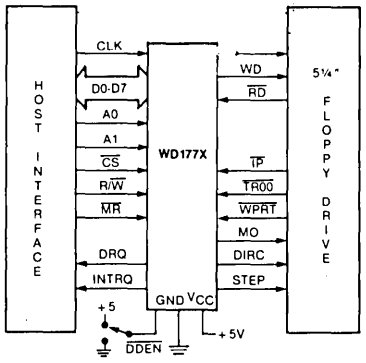
The WD1772-02 is a low cost version of the FD179X Floppy Disk Controller/Formatter. It is similar to the FD179X, but has a built-in digital data separator and write precompensation circuits.

A single read line (RD, Pin 19) is the only input required to recover serial FM of MFM data from the disk drive. The device is designed for control of floppy disk drives with data rates of 125 KBits/Sec (single density) and 250 KBits/Sec (double density). In addition, write precompensation of 187 nsec from nominal is enabled at any point through simple software commands. Another programmable feature, Motor On, enables the spindle motor automatically prior to operating a selected drive.

The WD1772-02 offers stepping rates of 2, 3, 6 and 12 msec. The processor interface consists of an 8-bit bi-directional bus for transfer of status, data, and commands. All Host communication with the drive occurs through these lines. They are capable of driving one standard TTL load or three LS loads.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	A logic low on this input selects the chip and enables Host communication with the device.
2	R/$\overline{W}$	READ/$\overline{WRITE}$	I	A logic high on this input controls the placement of data on the D0-D7 lines from a selected register, while a logic low causes a write operation to a selected register.
3,4	A0,A1	ADDRESS 0,1	I	These two inputs select a register to Read/Write data: $\overline{CS}$ A1 A0 R/$\overline{W}$ = 1 R/$\overline{W}$ = 0 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
5-12	DAL0-DAL7	DATA ACCESS LINES 0 THROUGH 7	I/O	Eight-bit bi-directional bus used for transfer of data, control, or status. This bus is enabled by $\overline{CS}$ and R/$\overline{W}$. Each line will drive one TTL load.
13	$\overline{MR}$	$\overline{MASTER\ RESET}$		A logic low pulse on this line resets the device and initializes the Status Register (internal pull-up).
14	GND	GROUND		Ground.
15	V_{CC}	POWER SUPPLY	I	+5V ±5% power supply input.
16	STEP	STEP	O	The Step output contains a pulse for each step of the drive's R/W head.
17	DIRC	DIRECTION	O	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
18	CLK	CLOCK	I	This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHz ±0.1%.
19	$\overline{RD}$	$\overline{READ\ DATA}$	I	This active low input is the raw data line containing both clock and data pulses from the drive.
20	MO	MOTOR ON	O	Active high output used to enable the spindle motor prior to read, write or stepping operations.
21	WG	WRITE GATE	O	This output is made valid prior to writing on the diskette.
22	WD	WRITE DATA		FM or MFM clock and data pulses are placed on this line to be written on the diskette.
23	$\overline{TR00}$	$\overline{TRACK\ 00}$	I	This active low input informs the WD1772-02 that the drive's R/W heads are positioned over Track zero.
24	$\overline{IP}$	$\overline{INDEX\ PULSE}$	I	This active low input informs the WD1772-02 when the physical index hole has been encountered on the diskette.
25	$\overline{WPRT}$	$\overline{WRITE\ PROTECT}$	I	This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing (internal pull-up).

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
26	$\overline{\text{DDEN}}$	$\overline{\text{DOUBLE}}$ $\overline{\text{DENSITY}}$ $\overline{\text{ENABLE}}$	I	This input pin selects either single (FM) or double (MFM) density. When $\overline{\text{DDEN}}$ = 0, double density is selected (internal pull-up).
27	DRQ	DATA REQUEST	O	This active high output indicates that the Data Register is full (on a Read) or empty (on a Write operation).
28	INTRQ	INTERRUPT REQUEST	O	This active high output is set at the completion of any command, is reset by a read of the Status Register.



WD1772-02 SYSTEM BLOCK DIAGRAM

ARCHITECTURE

The primary sections of the Floppy Disk Formatter are the parallel processor interface and the Floppy disk interface.

Data Shift Register – This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RD}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register – This 8-bit register is used as a holding register during Disk Read and Write operations. In disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek Command, the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register is not loaded when the device is busy.

Sector Register (SR) – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register is not loaded when the device is busy.

Command Register (CR) – This 8-bit register holds the command presently being executed. This register is not loaded when the device is busy unless the new command is a forced interrupt. The Command Register is loaded from the DAL, but not read onto the DAL.

Status Register (STR) – This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register is read onto the DAL, but not loaded from the DAL.

CRC Logic – This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is:

$G(x) = x^{16} + x^{12} + x^5 + 1.$

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC Register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

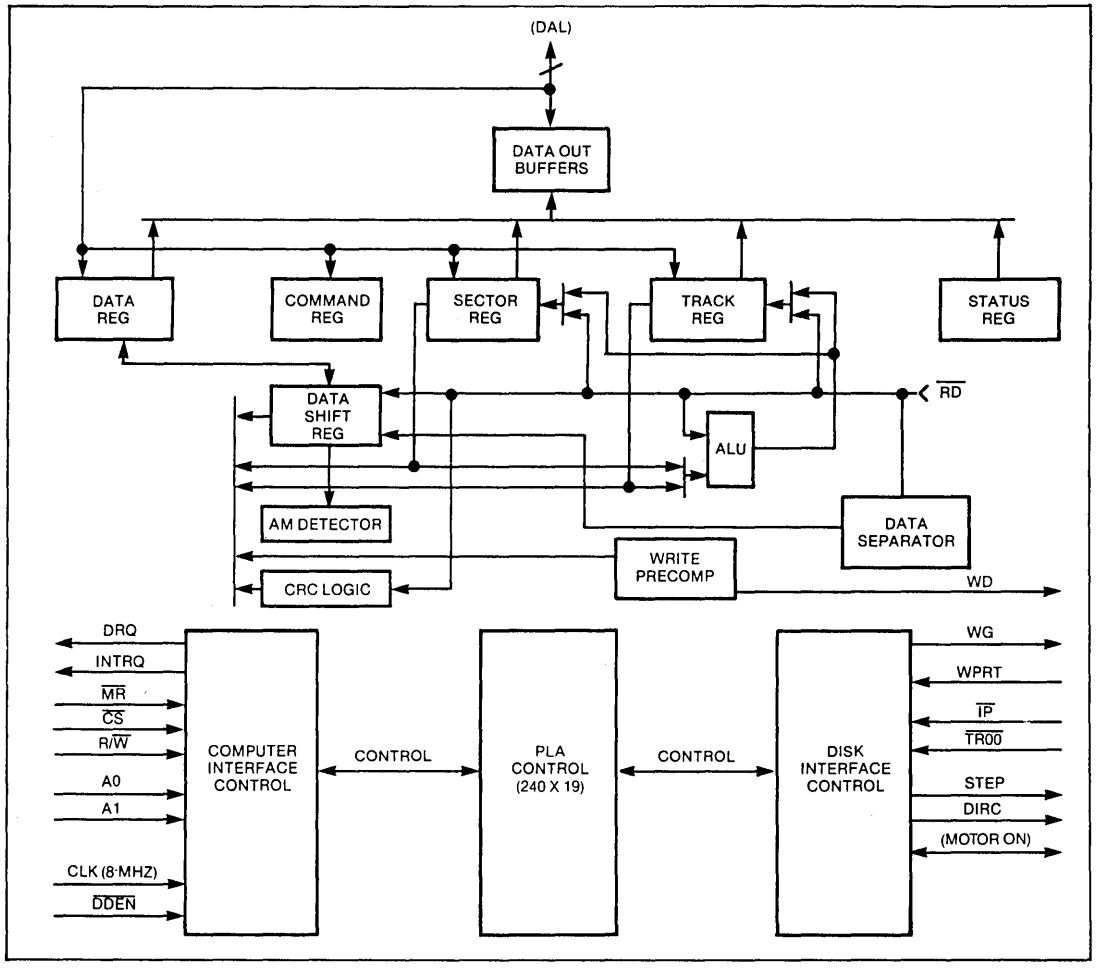


FIGURE 1. WD1772-02 BLOCK DIAGRAM

Timing and Control – All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The WD1772-02 has two different modes of operation according to the state of DDEN.

When $\overline{DDEN}$ = 0, double density (MFM) is enabled. When DDEN = 1, single density is enabled.

AM Detector – The address mark detector detects ID, data, and index address marks during read and write operations.

Data Separator – A digital phase lock loop (DPLL) of type 2, second order performs the data separator function. DPLL has a filter transfer function used to remove jitter effects thereby achieving adequate window margin. The algorithm used gives performance equal to second order analog designs.

DPLL performance specifications are as follows:

Fc capture range ±6% (min)
TI lock response 4 bytes 00H (max)
Wt window tolerance 50% for 10E-9 error rate

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD1772-02. The DAL are three state buffers that are enabled as output drivers when $\overline{CS}$ and R/W = 1 are active or act as input receivers when $\overline{CS}$ and $\overline{RW}$ = 0 are active.

When transfer of data with the Floppy Disk Controller is required by the Host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signal R/W during a Read operation or Write operation are interpreted as selecting the following registers:

A1 - A0	READ (R/$\overline{W}$ = 1)	WRITE (R/$\overline{W}$ = 0)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

After any register is written to, the same register cannot be read from until 16 μsec in MFM or 32 μsec in FM have elapsed.

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD1772-02 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations, the Data Request bit is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operations continue until the end of sector is reached.

On Disk Write operations, the Data Request bit is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit set in the Status Register.

At the completion of every command, an INTRQ is generated. INTRQ is reset by either reading the Status Register or by loading the Command Register with a new command. In addition, INTRQ is generated if a Force Interrupt Command condition is met.

The WD1772-02 has two modes of operation according to the state $\overline{DDEN}$. When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input is at 8 MHz.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ is placed to logical 1. For MFM formats, $\overline{DDEN}$ is placed to a logical 0. Sector lengths are determined at format time by the fourth byte in the ID field.

SECTOR LENGTH TABLE	
SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

The number of sectors per track for the WD1772-02 are from 0 to 244. The number of tracks for the WD1772-02 are 0 to 244.

GENERAL DISK WRITE OPERATION

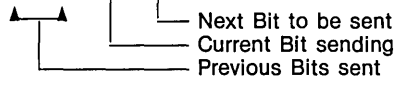
When writing on the diskette, the WG output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte is loaded into the Data Register in response to a Data Request from the device before the WG is activated.

Writing is inhibited when the $\overline{WPRT}$ input is asserted, in which case any Write Command is immediately terminated, an interrupt is generated and the Write Protect Status bit is set.

For Write operations, the WD1772-02 provides WG to enable a Write condition, and WD which consists of a series of active high pulses. These pulses contain both Clock and Data information in FM and MFM. WD provides the unique missing clock patterns for recording Address Marks.

On the WD1772-02, the Precomp Enable bit in Write Commands allows automatic Write precompensation to take place. The outgoing Write Data stream is delayed or advanced from nominal by 187 nsec according to the following table:

PATTERN				MFM	FM
X	1	1	0	Early	N/A
X	0	1	1	Late	N/A
0	0	0	1	Early	N/A
1	0	0	0	Late	N/A



Precompensation is typically enabled on the innermost tracks where bit shifts usually occur and bit density is at its maximum.

COMMAND DESCRIPTION

The WD1772-02 accepts 11 commands. Command words are only loaded in the Command Register when the Busy Status bit is off (Status bit 0). The one exception is the Force Interrupt Command. Whenever a command is being executed, the Busy Status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. Commands are divided into four types and are summarized in the following pages.

COMMAND SUMMARY

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step-in	0	1	0	u	h	V	r_1	r_0
I	Step-out	0	1	1	u	h	V	r	r_0
II	Read Sector	1	0	0	m	h	E	0	0
II	Write Sector	1	0	1	m	h	E	P	a_0
III	Read Address	1	1	0	0	h	E	0	0
III	Read Track	1	1	1	0	h	E	0	0
III	Write Track	1	1	1	1	h	E	P	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TYPE I COMMANDS

h = Motor On Flag (Bit 3)

h = 0, Enable Spin-up Sequence
h = 1, Disable Spin-up Sequence

V = Verify Flag (Bit 2)

V = 0, No Verify
V = 1, Verify on Destination Track

r_1, r_0 = Stepping Rate (Bits 1,0)

r_1	r_0	WD1772-02
0	0	6 ms
0	1	12 ms
1	0	2 ms
1	1	3 ms

u = Update Flag (Bit 4)

u = 0, No Update
u = 1, Update Track Register

TYPE II & III COMMANDS

m = Multiple Sector Flag (Bit 4)

m = 0, Single Sector
m = 1, Multiple Sector

H = Motor On Flag (Bit 3)

H = 0, Enable Spin Up Sequence
H = 1, Disable Spin Up Sequence

a_0 = Data Address Mark (Bit 0)

a_0 = Write Normal Data Mark
a_0 = 1, Write Deleted Data Mark

E = 15ms Settling Delay (Bit 2)

E = 0, No Delay
E = 1, Add 15ms Delay

P = Write Precompensation (Bit 1)

P = 0,Enable Write Precomp
P = 1,Disable Write Precomp

TYPE IV COMMANDS

I_3-I_0 Interrupt Condition (Bits 3-0)

I_0 = 1, Not Used
I_1 = 1, Not Used
I_2 = 1, Interrupt on Index Pulse
I_3 = 1, Immediate Interrupt
I_3-I_0 = 0, Terminate without interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out Commands. Each of the Type I Commands contains a rate field (r_0,r_1), which determines the stepping motor rate.

A 4 μsec (MFM) or 8 μsec (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip steps the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 24 μsec before the first stepping pulse is generated.

After the last directional step, an additional 15 msec of head settling time takes place if the Verify flag is set in Type I Commands. There is also a 15 msec head settling time if the E flag is set in any Type II or III Command.

When a Seek, Step, or Restore Command is executed, an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 msec settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field CRC is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID Field is read from the disk for the verification operation.

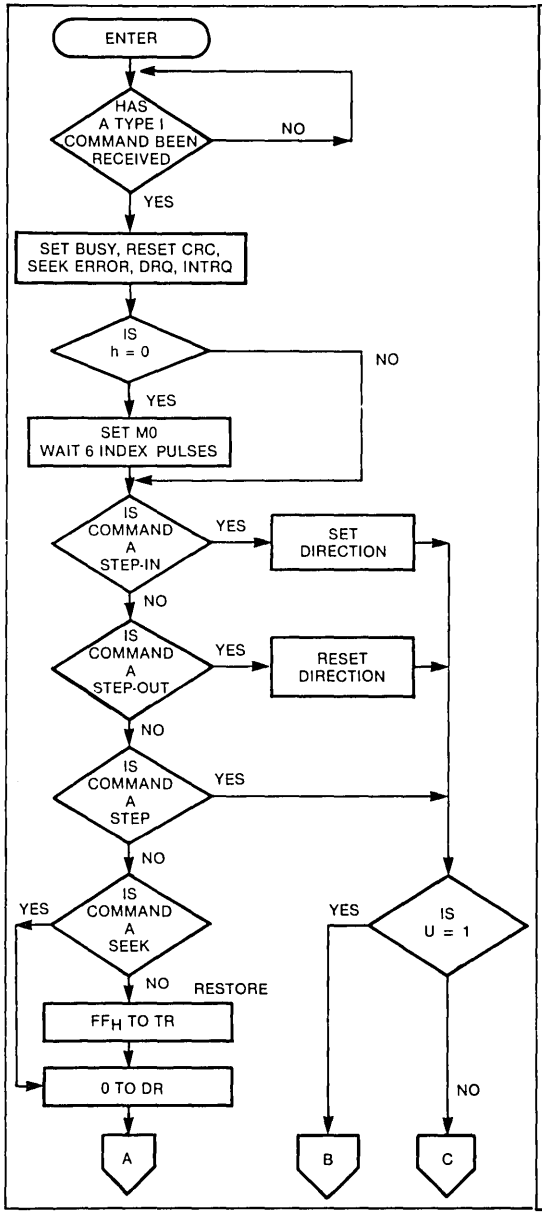
The WD1772-02 finds an ID Field with correct track number and correct CRC within 5 revolutions of the media, or the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

On the WD1772-02, all commands, except the Force Interrupt Command, are programmed via the h Flag to delay for spindle motor start up time. If the h Flag is not set and the MO signal is low when a command is received, the WD1772-02 forces MO to a logic 1 and waits 6 index pulses before executing the command. At 300 RPM, this guarantees a one second spindle start up time. If after finishing the command, the device remains idle for 9 revolutions, the MO

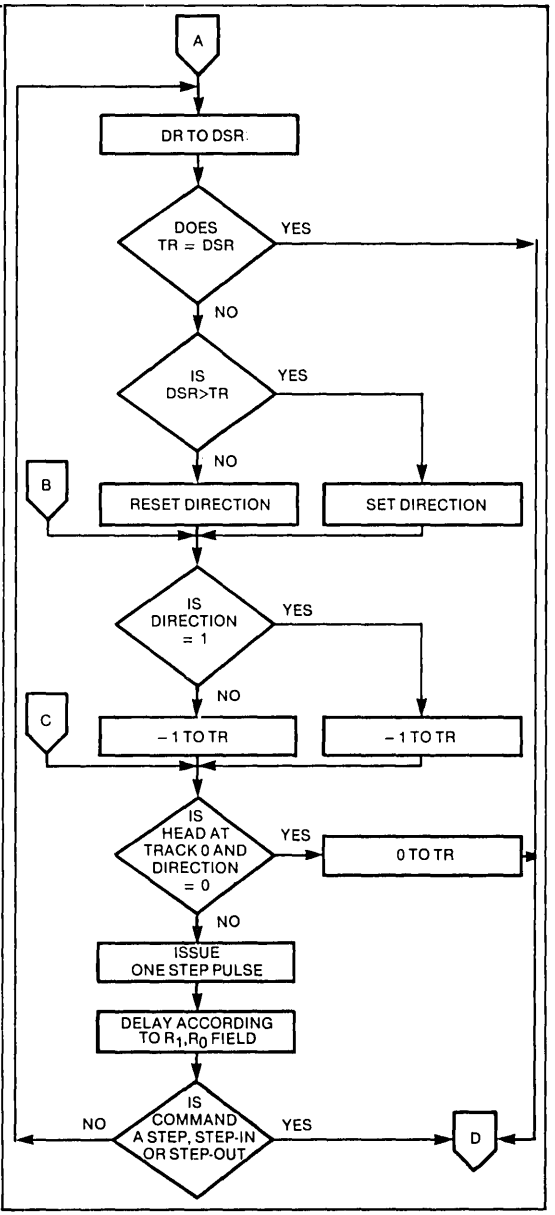
signal goes back to a logic 0. If a command is issued while MO is high, the command executes immediately, defeating the 5 revolution start up. This feature allows consecutive Read or Write commands without waiting for motor start up each time; the WD1772-02 assumes the spindle motor is up to speed.

RESTORE (SEEK TRACK 0)

Upon receipt of this command, the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low, indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r_1,r_0 field are issued until the $\overline{TR00}$ input is activated.



TYPE I COMMAND FLOW

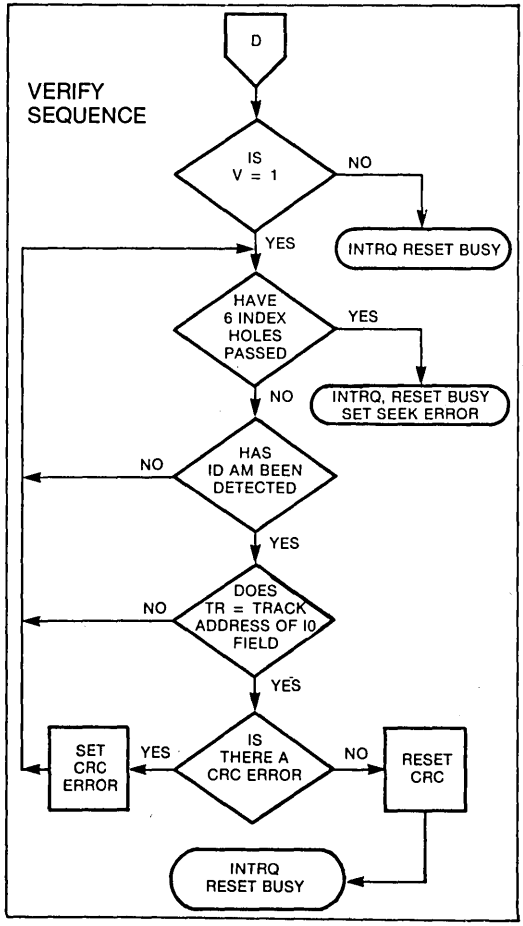


TYPE I COMMAND FLOW

At this time, the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the WD1772-02 terminates operation, interrupts, and sets the Seek Error status bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the Motor On option at the start of a command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD1772-02 updates the Track Register and issues stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the Track Register is updated for the drive selected before seeks are issued.



TYPE I COMMAND FLOW

STEP

Upon receipt of this command, the WD1772-02 issues one Stepping Pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD1772-02 issues one Stepping Pulse in the direction towards the inner most track. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

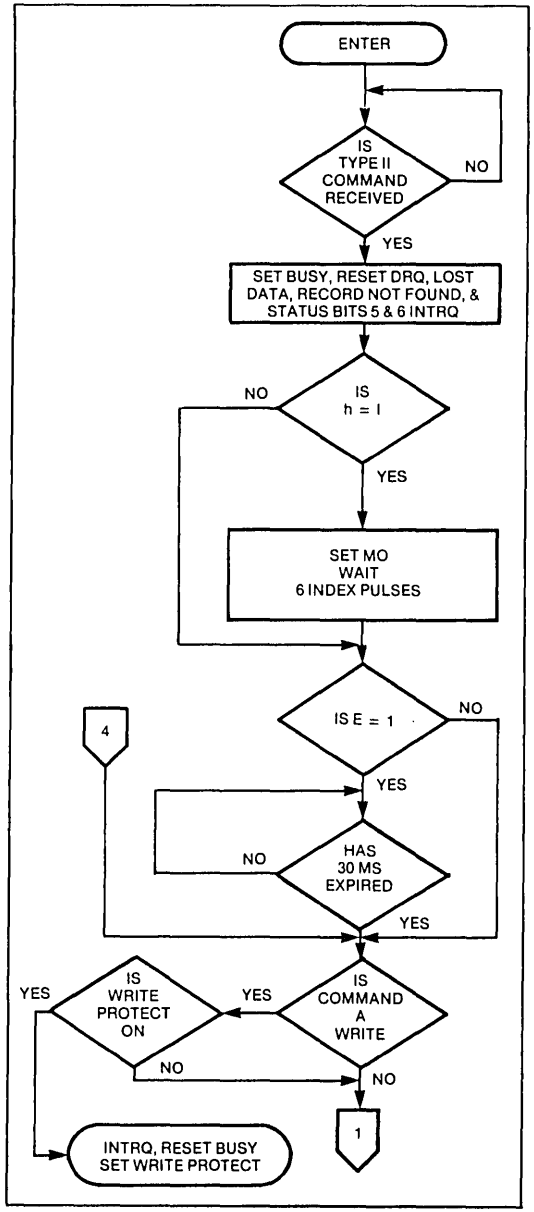
STEP-OUT

Upon receipt of this command, the WD1772-02 issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer loads the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy Status bit is set. If the E flag = 1, the command executes after a 15 msec delay.

(When an ID field is located on the disk, the WD1772-02 compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made). If there is a match, the Sector Number of the ID field is compared with the Sector Register. If there is no Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is located and is either written into, or read from, depending upon the command.



TYPE II COMMAND

The WD1772-02 finds an ID field with a Track number, Sector number, and CRC within 5 revolutions of the disk, or, the Record Not Found Status bit is set (Status Bit 4) and the command is terminated with an INTRQ.

Each of the Type II Commands contains an m flag which determines if multiple records (sectors) are read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification occurs on the next record. The WD1772-02 continues to read or write multiple records and updates the Sector Register in numerical ascending sequence until the Sector Register exceeds the number of sectors on the track or until the Force Interrupt Command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the WD1772-02 is instructed to read sector 27 and there are only 26 on the track, the Sector Register exceeds the number available. The WD1772-02 searches for 5 disk revolutions, interrupts out, resets Busy, and sets the Record Not Found Status Bit.

READ SECTOR

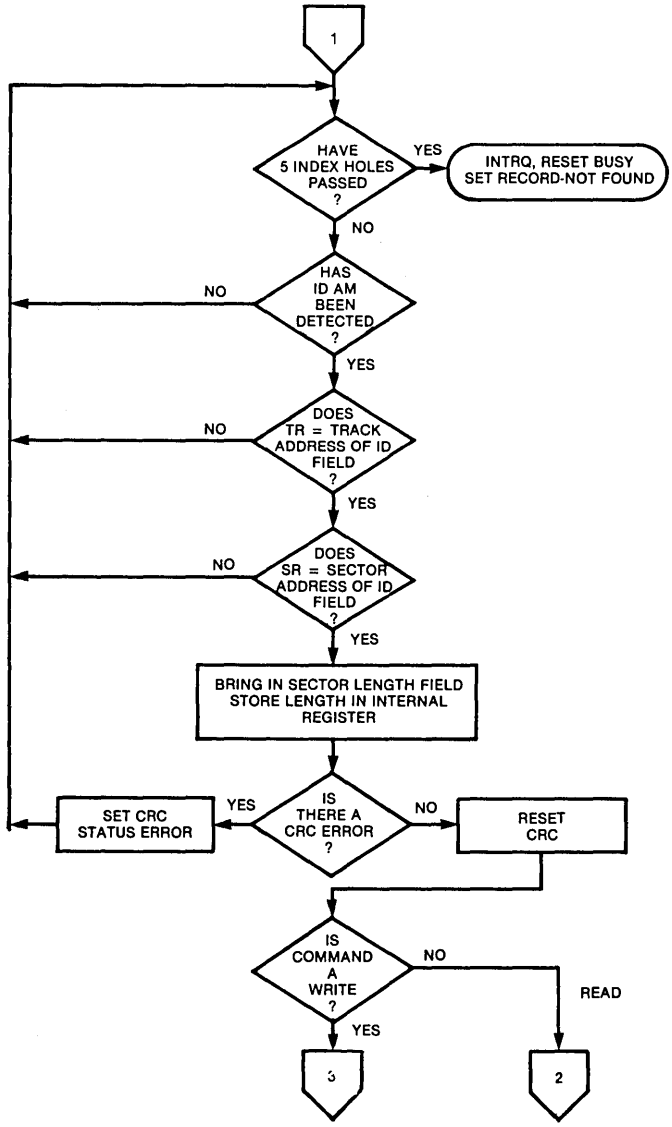
Upon receipt of the Read Sector Command, the Busy Status Bit is set, then when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field is found with 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte. If not, the ID field is searched for and verified again followed by the Data Address Mark search. If, after five revolutions the DAM is not found, the Record Not Found Status Bit is set and the operation is terminated. When the first character or byte of the data field is shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred, that character is lost and the Lost Data Status Bit is set. This sequence continues until the complete data field is inputted to the computer. If there is a CRC error at the end of the data field, the CRC Error Status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector Command, the Busy Status Bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The WD1772-02 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the WG

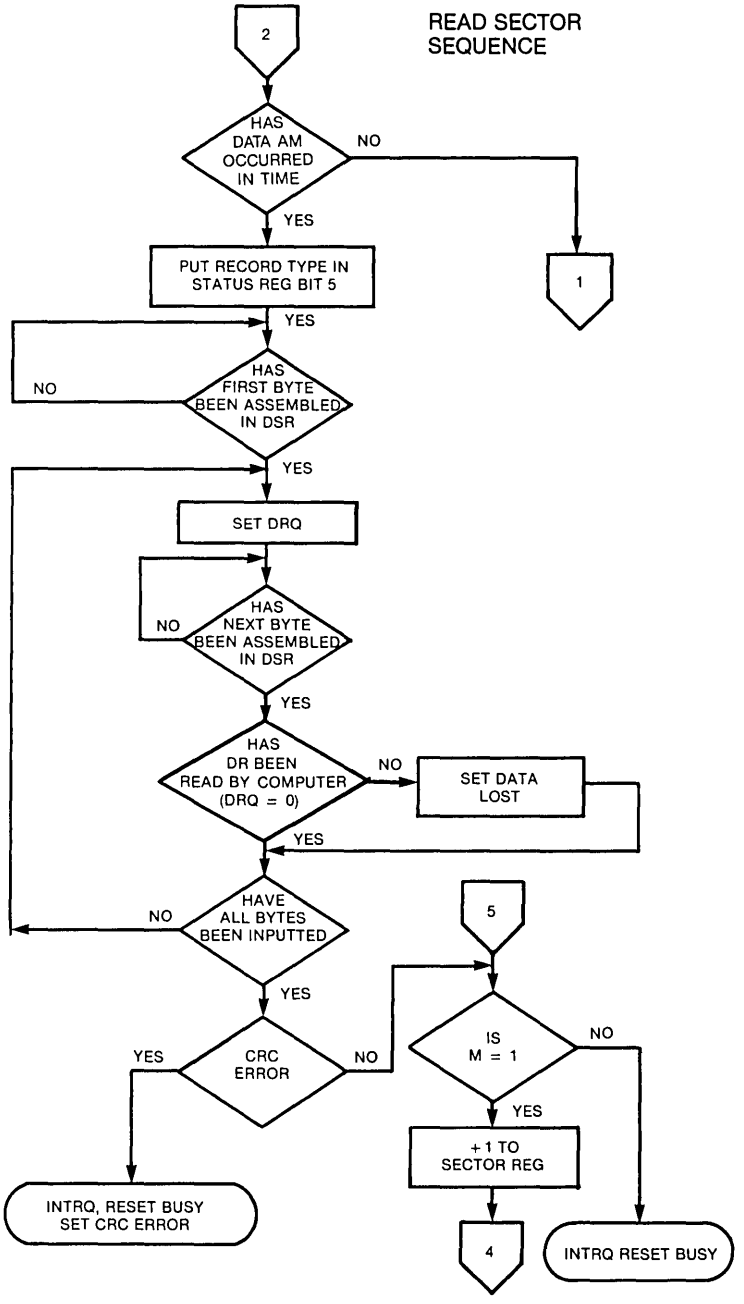


TYPE II COMMAND

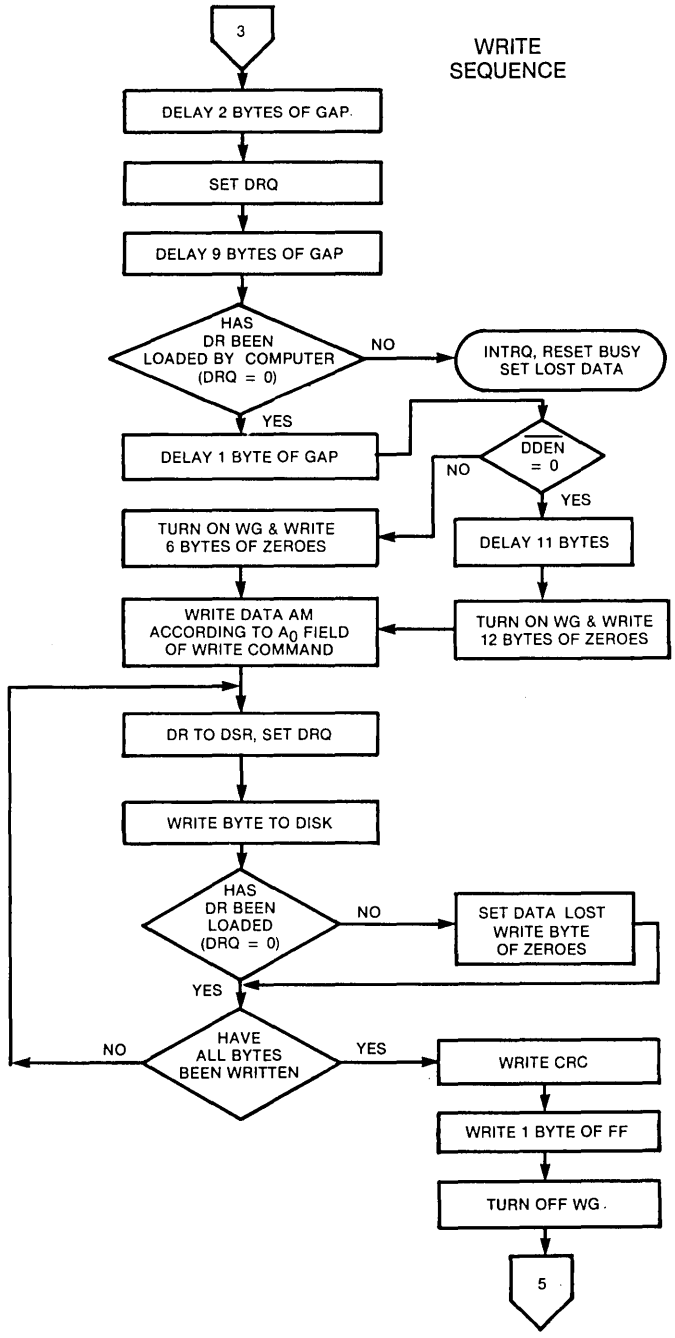
ouput is made active if the DRQ is serviced (i.e., the DR is loaded by the computer). If DRQ is not serviced, the command is terminated and the Lost Data Status Bit is set. If the DRQ is serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are written on the disk. The Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown:

a_0	DATA ADDRESS MARK (BIT 0)
1	Deleted Data Mark
0	Data Mark

The WD1772-02 writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status



TYPE II COMMAND



TYPE II COMMAND

Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte is written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. INTRQ sets 24 μsec (MFM) after the last CRC byte is written. For partial sector writing, the proper method is to write data and fill the balance with zeroes.

TYPE III COMMANDS

Read Address

Upon receipt of the Read Address Command, the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown:

TRACK ADDR	SIDE NUMBER	SECTOR ADDR	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the WD1772-02 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation, an interrupt is generated and the Busy Status is reset.

Read Track

Upon receipt of the Read Track Command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. These characteristics are: no CRC checking is performed; gap information is included in the data stream; and the Address Mark Detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM.

The ID AM, ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector are correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

Data and gap information are provided at the computer interface. Formatting the disk is accomplished by positioning the head over the desired track number and issuing the Write Track Command.

Upon receipt of the Write Track Command, the Busy Status Bit is set. Writing starts with the leading edge of the first encountered Index Pulse and continues until the next Index Pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing does not start until after the first byte is loaded into the Data Register. If the DR is not loaded within three byte times, the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

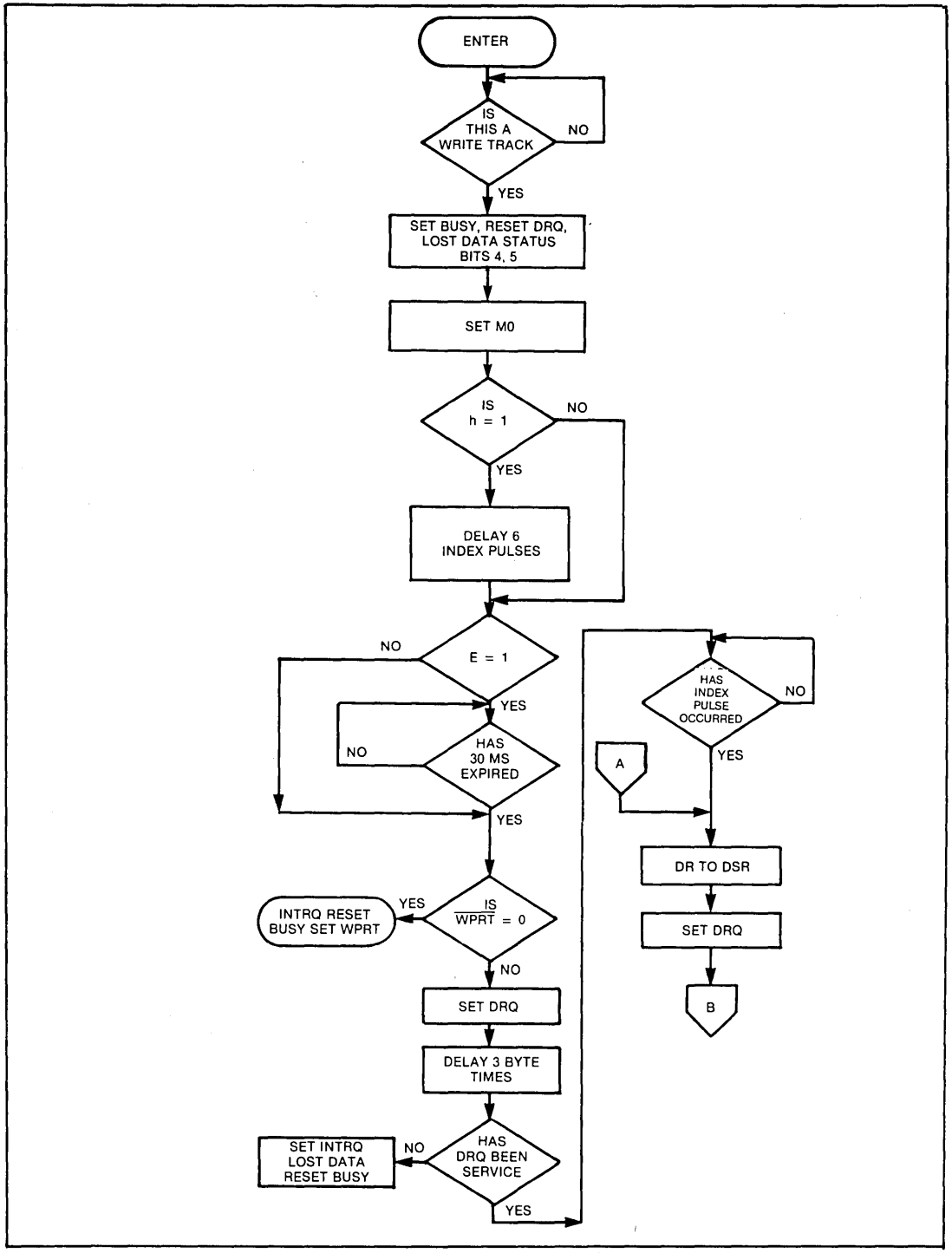
This sequence continues from one Index Pulse to the next. Normally, whatever data pattern appears in the Data Register is written on the disk with a normal clock pattern. However, if the WD1772-02 detects a data pattern of F5 through FE in the Data Register, this is interpreted as Data Address Marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern generates two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE do not appear in the gaps, data field, or ID fields. Also, CRC's are generated by an F7 pattern.

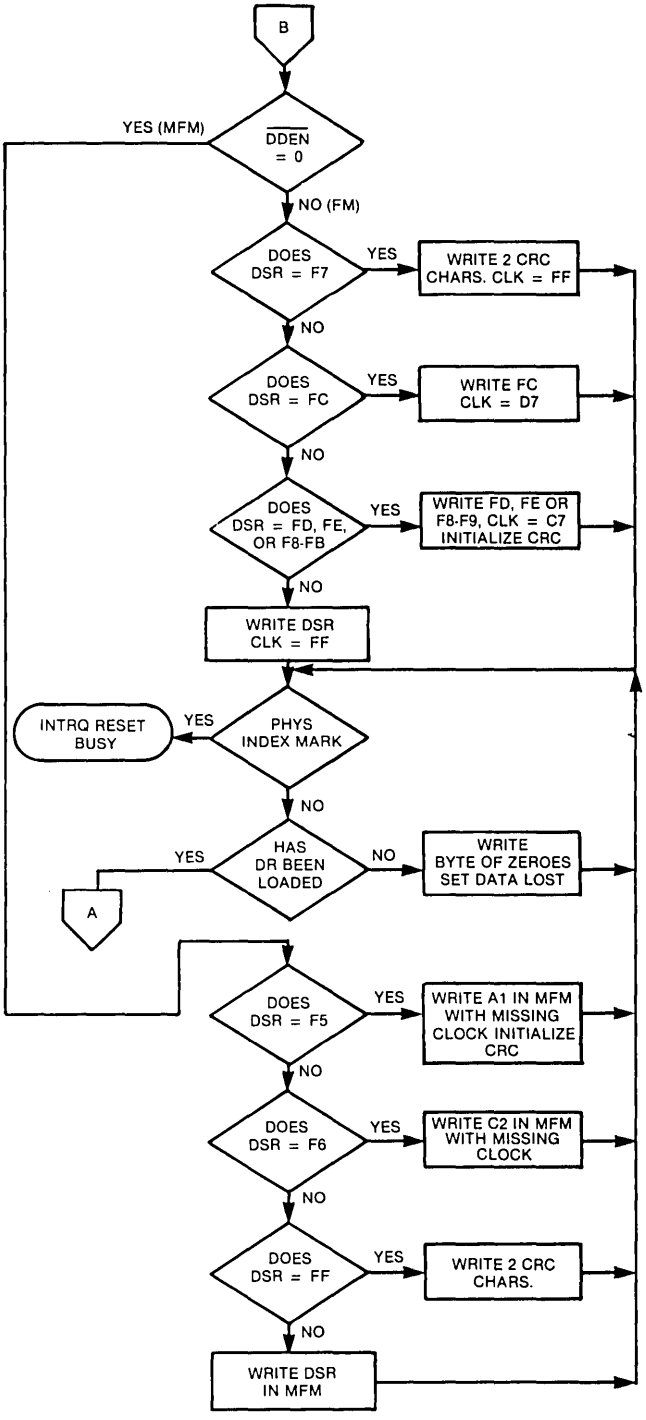
Disks are formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

DATA PATTERN IN DR (HEX)	IN FM ($\overline{DDEN}$ = 1)	IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Present CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F9 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5.
**Missing clock transition between bits 3 and 4.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

TYPE IV COMMANDS

The Forced Interrupt Command is used to terminate a multiple sector read or write command or to ensure Type I status in the Status Register. This command is loaded into the Command Register at any time. If there is a current command under execution, (Busy Status Bit set), the command is terminated and the Busy Status Bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not used

I_1 = Not Used

I_2 = Every Index Pulse

I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3-I_0) are set to a 1. When the condition for interrupt is met, the INTRQ line goes high signifying that the condition specified has occurred. If I_3-I_0 are all set to zero (Hex D0), no interrupt occurs but any command presently under execution is immediately terminated. When using the immediate interrupt condition (I_3 = 1), an interrupt is immediately generated and the current command terminated. Reading the status or writing to the command register does not automatically clear the interrupt. The Hex D0 is the only command that enables the immediate interrupt (Hex D8) to clear on a subsequent load Command Register or Read Status Register operation. Follow a Hex D8 with D0 command.

Wait 16 μsec (double density) or 32 μsec (single density) before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this nullifies the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt waits until ALU operations in progress are complete (CRC calculations, compares, etc.).

Status Register

Upon receipt of any command, except the Force Interrupt Command, the Busy Status Bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy Status Bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt Command is received when there is not a current command under execution, the Busy Status Bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the Status Register through program control or using the DRQ line with DMA or interrupt methods. When the Data Register is read, the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes both DRQ's to reset.

The Busy Bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a Busy Status check is not recommended because a read of the Status Register to determine the condition of busy resets the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Because of internal sync cycles, certain time delays are observed when operating under programmed I/O, as shown.

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	48μsec	24μsec
Write to Command Reg.	Read Status Bits 1-7	64μsec	32μsec
Write Register	Read Same Register	32μsec	16μsec

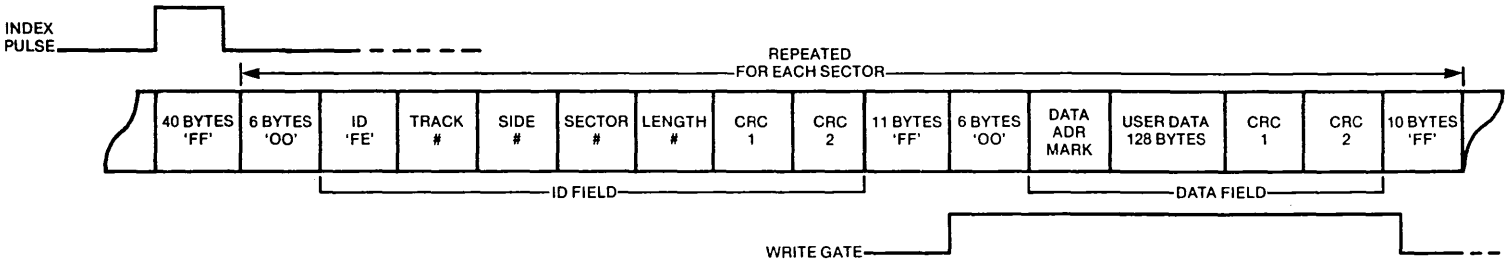
RECOMMENDED - 128 BYTES/SECTOR

The recommended single-density format with 128 bytes/sector is shown below. In order to format a diskette, the user issues the Write Track Command, and loads the Data Register with the following values. For every byte to be written, there is one Data Request.

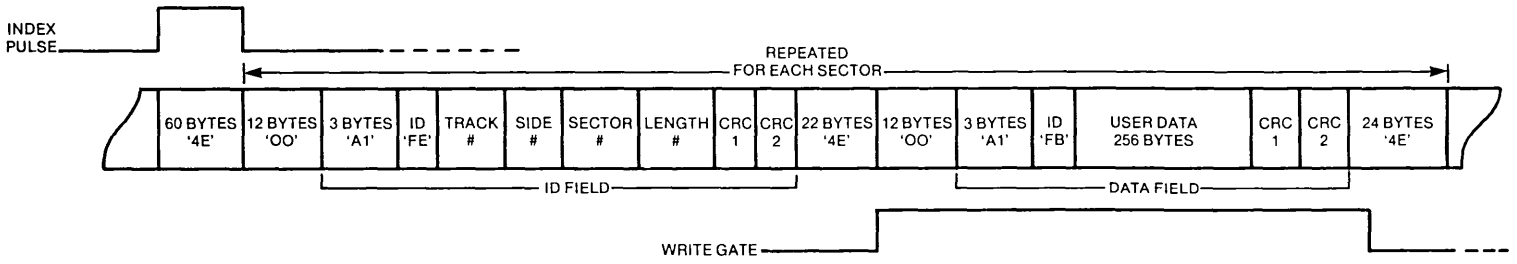
NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
10	FF (or 00)
369**	FF (or 00)

*Write bracketed field 16 times.

**Continue writing until WD1772-02 interrupts out. Approx. 369 bytes.



SINGLE DENSITY FORMAT



DOUBLE DENSITY FORMAT

256 BYTES/SECTOR

Shown above is the recommended dual-density format with 256 bytes/sector. In order to format a diskette, the user issues the Write Track Command and loads the Data Register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
60	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRC's written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (Data Address Mark)
24	4E
668**	4E

*Write bracketed field 16 times.
**Continue Writing until WD1772-02 interrupts out. Approx. 668 bytes.

1. Non-Standard Formats

Variations in the recommended formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.
2) Gap 2 cannot be varied from the recommended format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the WD1772-02. Gap 1, 3 and 4 lengths are as short as 2 bytes for WD1772-02 operation, however PLL lock up time, motor speed variation, write-splice area, etc. adds more bytes to each gap to achieve proper operation. For highest system reliability, use the recommended format.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

STATUS REGISTER DESCRIPTION

BIT NAME	MEANING
S7 MOTOR ON	This bit reflects the status of the Motor On output.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/SPIN-UP	When set, this bit indicates that the Motor Spin-Up sequence has completed (5 revolutions) on Type I commands. Type 2 & 3 commands, this bit indicates record Type. 0 = Data Mark. 1 = Deleted Data Mark.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error data field. This bit is reset when updated.
S2 LOST DATA/ BYTE	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. On Type I commands, this bit reflects the status of the TR00 signal.
S1 DATA REQUEST INDEX	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. On Type 1 commands, this bit indicates the status of the IP signal.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

DC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Storage Temperature ..... −55°C(−67°F) to +125°C (257°F)
Operating Temperature ..... 0°C(32°F) to 70°C (158°F) Ambient
Maximum Voltage to Any Input with Respect to V_{SS} ..... +7V to −0.5V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

DC OPERATING CHARACTERISTICS

TA = 0°C(32°F) to 70°C (158°F), V_{SS} = OV, V_{CC} = +5V ± .25V

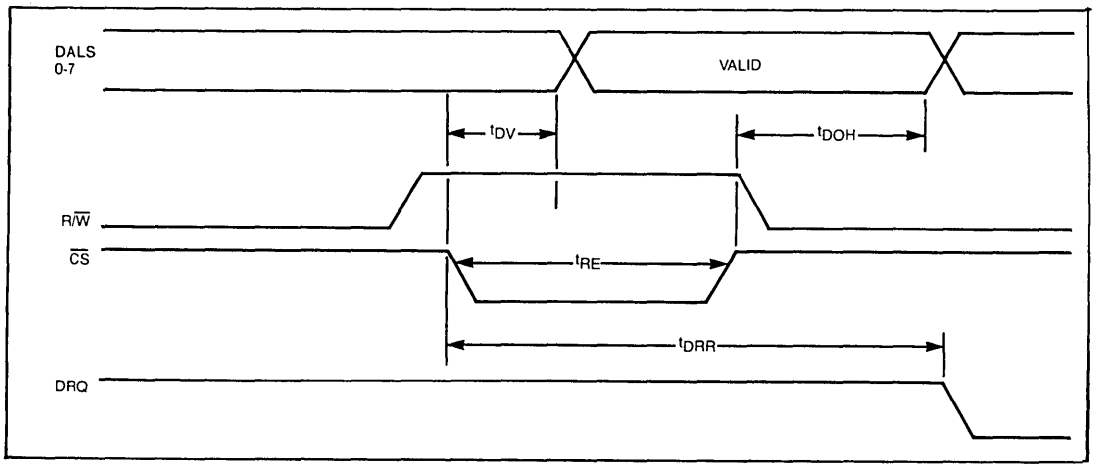
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IH}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_0 = -100 μA
V_{OL}	Output Low Voltage		0.40	V	I_0 = 1.6 mA
P_D	Power Dissipation		.75	W	
R_{PU}	Internal Pull-Up	100	1700	μA	V_{IN} = 0V
I_{CC}	Supply Current	75(Typ)	150	mA	

DPLL SPECIFICATION

F_C Capture Range ± 6% (min)
T_l Lock Response 4 bytes 00 hex (max)
WT Window Tolerance 50% for 10E-9 Error Rate (min)

AC TIMING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F), ^{V}SS = 0V, ^{V}CC = +5V ± .25V

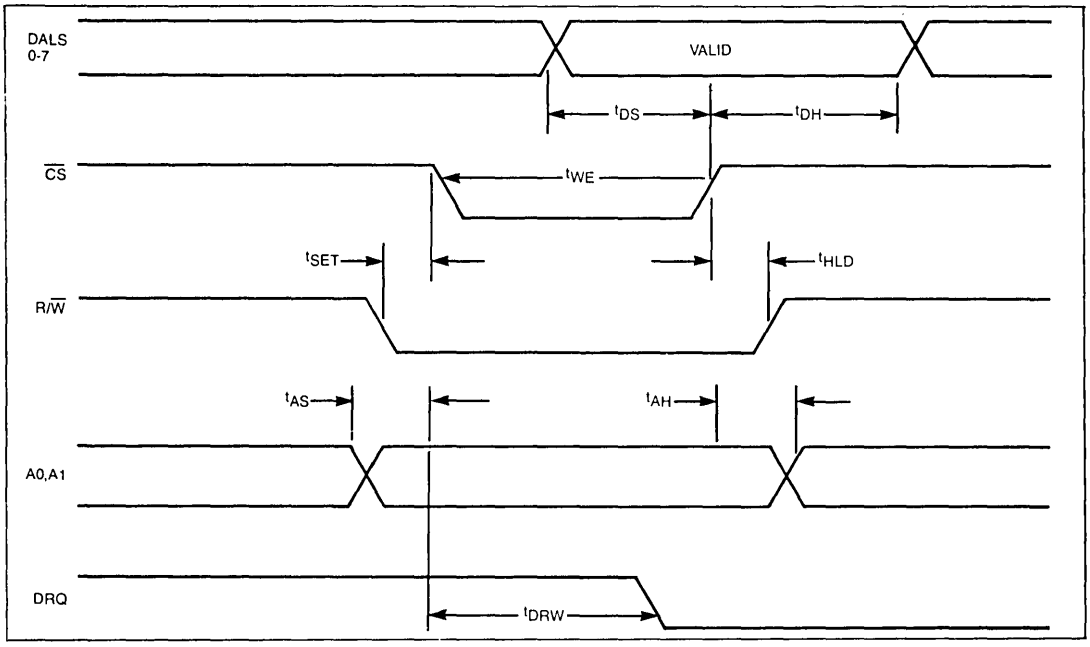


READ ENABLE TIMING

READ ENABLE TIMING – $\overline{RE}$ such that: R/$\overline{W}$ = 1, CS = 0.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RE}	$\overline{RE}$ Pulse Width of $\overline{CS}$	200			nsec	C_L = 50 pf
t_{DRR}	DRQ Reset from $\overline{RE}$		200	300	nsec	
t_{DV}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
t_{DOH}	Data Hold from $\overline{RE}$	20		150	nsec	C_L = 50pf
	INTRQ Reset from $\overline{RE}$			8	μsec	

Note: Worst case service time for DRQ is 23.5 μsec for MFM and 47.5 μsec for FM.



WRITE ENABLE TIMING

WRITE ENABLE TIMING - $\overline{WE}$ such that: R/$\overline{W}$ = 0, $\overline{CS}$ = 0.

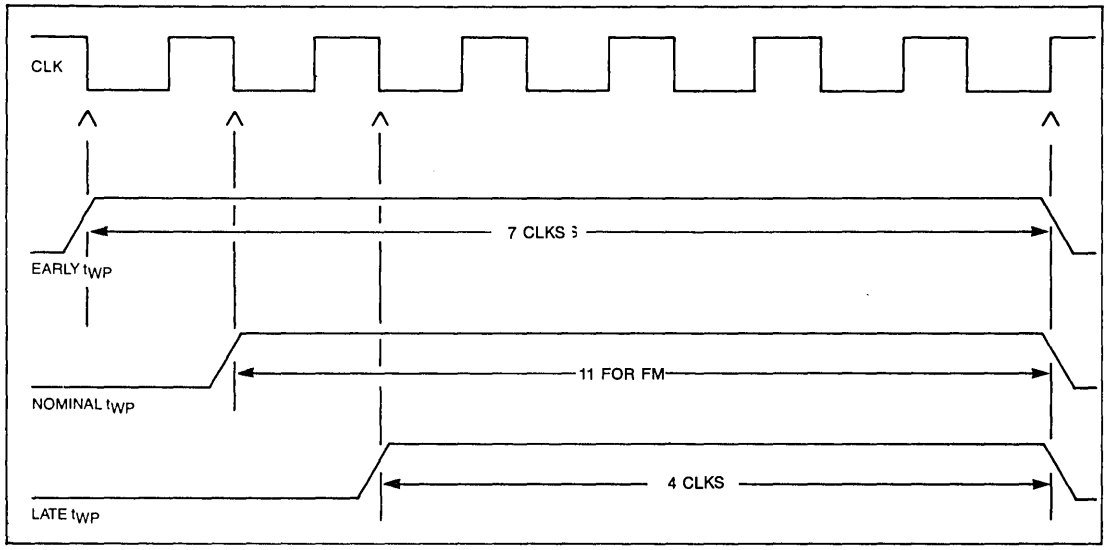
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{AS}	Setup ADDR to $\overline{CS}$	50			nsec	
t_{SET}	Setup R/$\overline{W}$ to $\overline{CS}$	0			nsec	
t_{AH}	Hold ADDR from $\overline{CS}$	10			nsec	
t_{HLD}	Hold R/$\overline{W}$ from $\overline{CS}$	0			nsec	
t_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
t_{DRW}	DRQ Reset from $\overline{WE}$		100	200	nsec	
t_{DS}	Data Setup to $\overline{WE}$	150			nsec	
t_{DH}	Data Hold from $\overline{WE}$	0			nsec	
	INTRQ Reset from $\overline{WE}$			8	µsec	

READ DATA TIMING:

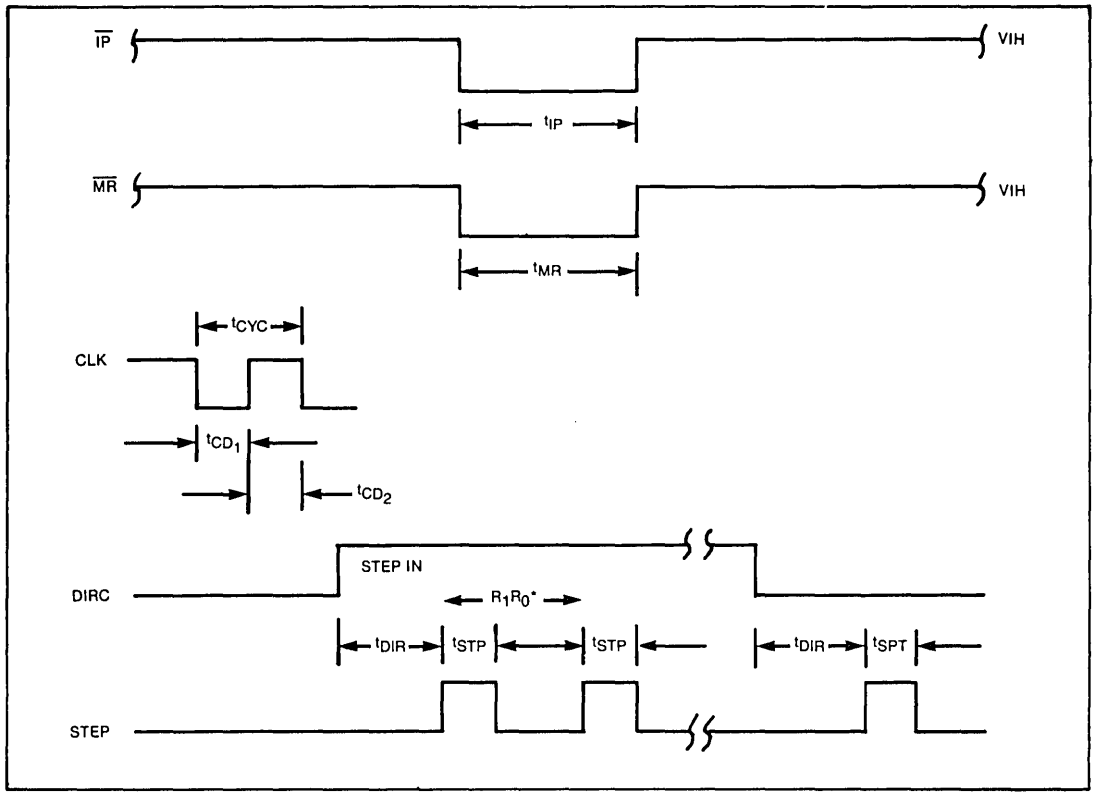
CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{\text{Raw Read}}$ Pulse Width	.200		3	µsec	MFM
	.400		3		FM
$\overline{\text{Raw Read}}$ Cycle Time	3			µsec	

WRITE DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
	Write Gate to Write Data		4		μsec	FM
			2		μsec	MFM
	Write Data Cycle Time		4,6,8		μsec	
	Write Gate off from WD		4		μsec	FM
			2		μsec	MFM
t_{WP}	Write Data Pulse Width		820		nsec	Early MFM
			690		nsec	Nominal MFM
			570		nsec	Late MFM
			1.38		μsec	FM



WRITE DATA TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{CD1}	Clock Duty (low)	50	67		nsec	
t_{CD2}	CLock Duty (high)	50	67		nsec	
t_{STP}	Step Pulse Output		4		µsec	MFM
			8			FM
t_{DIR}	Dir Setup to Step		24		µsec	MFM
			48			FM
t_{MR}	Master Reset Pulse Width	50			µsec	
t_{IP}	Index Pulse Width	20			µsec	

WD1772-02 Floppy Disk Formatter/Controller Family Application Notes

INTRODUCTION

To meet the demand for a low cost compact LSI Floppy Disk Controller device, Western Digital has developed the WD1772-02. The WD1772-02 is a NMOS Floppy Disk Controller device that incorporates the FD179X, a digital data separator and write precompensation circuitry all in a single chip. The device offers soft sector formatting, selectable stepping rates, automatic track seek with verify, and variable sector lengths. The WD1772-02 comes in a 28-pin dual-in-line package or quad pack and operates from a single 5 volt only power supply.

APPLICATIONS

The Mini-Floppy Controller is targeted for the low cost sector of the disk drive market, where digital data separation is preferred over analog phase lock loop. Included in this market are Personal Computers, Portable Computers and Small Business Computers.

HOST INTERFACING

Interfacing to a Host processor is accomplished through the eight bit bi-directional Data Access Lines (DAL) and associated control lines. The DAL is used to transfer data, status and control words out of or into WD1772-02. The DAL having three states enabled as an output when Chip Select (CS) is active low and Read/Write (R/W) is high or as input receiver when CS and R/W is low. When transfer of data with the device is required by the Host CS is made low. The address bits A0 and A1 combined with the R/W line select the register and the direction of data.

During Direct Memory Access (DMA) data transfers between the WD1772-02 and Host Memory, the Data Request (DRQ) line is used in Data Transfer Control. This signal also appears as status bit 1 during Read/Write operations. On Disk Read operations the DRQ is active when an assembled byte is present in the Data Register, then reset when read by the Host. If the Host fails to read the Data Register before the following byte is assembled in the Data Register, the lost data bit is set in Status Register.

At the completion of every command INTRQ is asserted. INTRQ is de-asserted by either reading the status or by loading the Command Register.

DISKETTE DRIVE INTERFACING

The WD1772-02 has two modes of operation depending on the state of DDEN, regardless of the state DDEN the CLK input remains at 8 MHz. Disk Reads with sector lengths of 128, 256, 512 and 1024 byte sector in both FM or MFM from diskettes is accomplished via the internal digital data separator. Disk Write operation in MFM on inner tracks may require write precompensation. Write precompensation is enabled when bit 1 = 0, in the Write command and a precompensation value of 187 nsec is produced.

The diskettes spindle motor is controlled by bit 3 of any Type I, II or III command, upon receiving a command with bit 3 = 0, the spin up sequence is enabled.

GENERAL INFORMATION

A +5 volt supply ±5% is used as V_{CC}, and the clock input requires a free running 50% duty cycle at 8 MHz ±0.1%.

FD179X-02 Floppy Disk Formatter/Controller Family

FEATURES

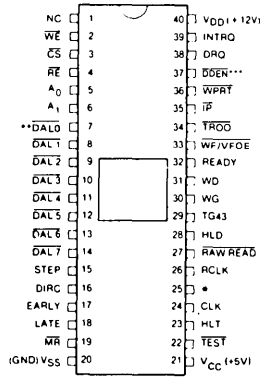
- TWO VFO CONTROL SIGNALS - RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY
- FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
  - Non IBM Format for Increased Capacity
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- INTERFACES TO WD1691 DATA SEPARATOR
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1792	1793	1794	1795	1797
Single Density (FM)	X	X	X	X	X	X
Double Density (MFM)	X		X		X	X
True Data Bus		X	X		X	
Inverted Data Bus	X	X		X		
Write Precomp	X	X	X	X	X	X
Side Selection Output				X	X	

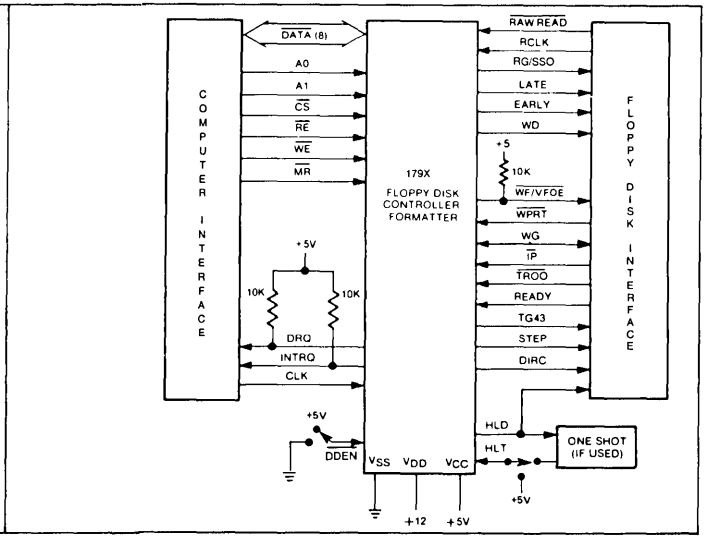
APPLICATIONS

8" FLOPPY AND 5 1/4" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS
***1792/4 OPEN

PIN DESIGNATION



FD179X SYSTEM BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0,A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	Eight bit bi-directional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$. Each line will drive 1 standard TTL load.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ±1% for 8" drives, 1 MHz ±1% for mini-floppies.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occuring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated steppers.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.
25	READ GATE (1791,1792,1793,1794)	RG	This output is used for synchronization of external data separators. The output goes high after two Bytes of zeroes in single density, or 4 Bytes of either zeroes or ones in double density operation.
25	SIDE SELECT OUTPUT (1794,1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector ID Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e., RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read / Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 50ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE FAULT	WF/VFOE VFO ENABLE	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 function as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resister.
34	TRACK 00	TR00	This input informs the FD179X that the Read / Write head is positioned over Track 00.
35	INDEX PULSE	IP	This input informs the FD179X when the index hole is encountered on the diskette.
36	WRITE PROTECT	WPRT	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	DDEN	This input pin selects either single or double density operation. When DDEN = 0, double density is selected. When DDEN = 1, single density is selected. This line must be left open on the 1792/4.

GENERAL DESCRIPTION

The FD179X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to Read/Write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bit directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793 respectively. On these devices, DDEN must be left open.

ORGANIZATION

The Floppy Disk Formatter is illustrated in the block diagram. The primary sections include the parallel processor interface and the Floppy Disk Interface.

Data Shift Register - This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register - This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) - This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

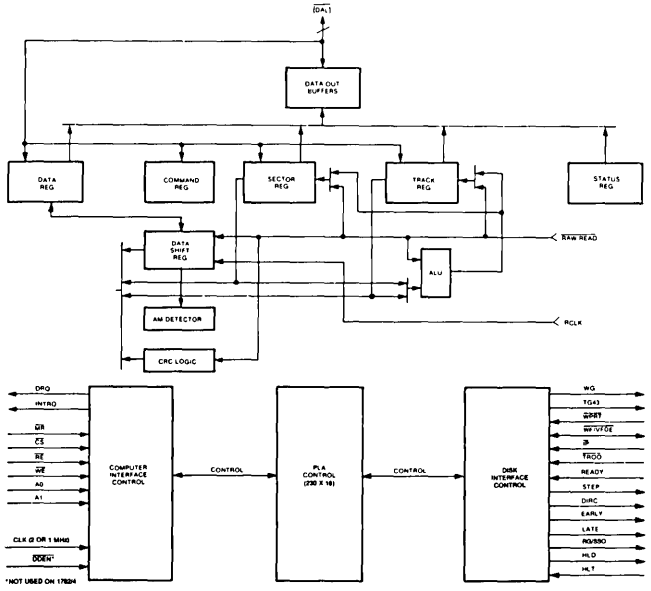
CRC Logic - This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^6 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control - All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD179X has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN} = 0$ double density (MFM) is assumed. When $\overline{DDEN} = 1$, single density (FM) is assumed. 1792 & 1794 are single density only.



FD179X BLOCK DIAGRAM

AM Detector - The address mark detector detects ID, data and Index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Regiser	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the DF179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK Input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*1795/97 may vary - see command summary.

The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations in 8" double density the FD179X requires RAW READ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. THE RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1791/92/93/94 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM. RG is made true when

2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active low when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WFVFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read / Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault Input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault Input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM (DDEN = 1) and 200 ns pulses in MFM (DDEN = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD 179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

READY

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 1791, 1792, 1793, 1794

		Bits							
Type	Command	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

B. Commands for Models: 1795, 1797

		Bits							
Type	Command	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Seek	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 2. FLAG SUMMARY

FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0,No verify V = 1,Verify on destination track
I	3	h = Head Load Flag	h = 1,Load head at beginning h = 0 Unload head at beginning
I	4	T = Track Update Flag	T = 0,No update T = 1,Update track register
II	0	a_0 = Data Address Mark	a_0 = 0,FB(DAM) a_0 = 1,F8(deleted DAM)
II	1	C = Side Compare Flag	C = 0,Disable side compare C = 1,Enable side compare
II & III	1	U = Update SSO	U = 0,Update SSO to 0 U = 1,Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0,No 15 MS delay E = 1,15 MS delay
II	3	S = Side Compare Flag	S = 0,Compare for side 0 S = 1,Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field 00: L=0 256, L=1 128 01: L=0 512, L=1 256 10: L=0 1024, L=1 512 11: L=0 128, L=1 1024
II	4	m = Multiple Record Flag	m = 0,Single record m = 1,Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

NOTE: See Type IV Command Description for further information.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0 r_1), which determines the stepping motor rate as defined in Table 3.

A 2μs (MFM) or 4μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12μs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1	X	X
R1 R0	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 0	$\overline{TEST}$ = 0
0 0	3 ms	3 ms	6 ms	6 ms	185μs	368μs
0 1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1 0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1 1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

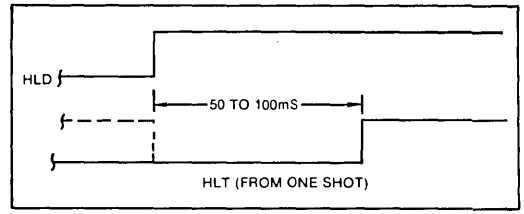
After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read / write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

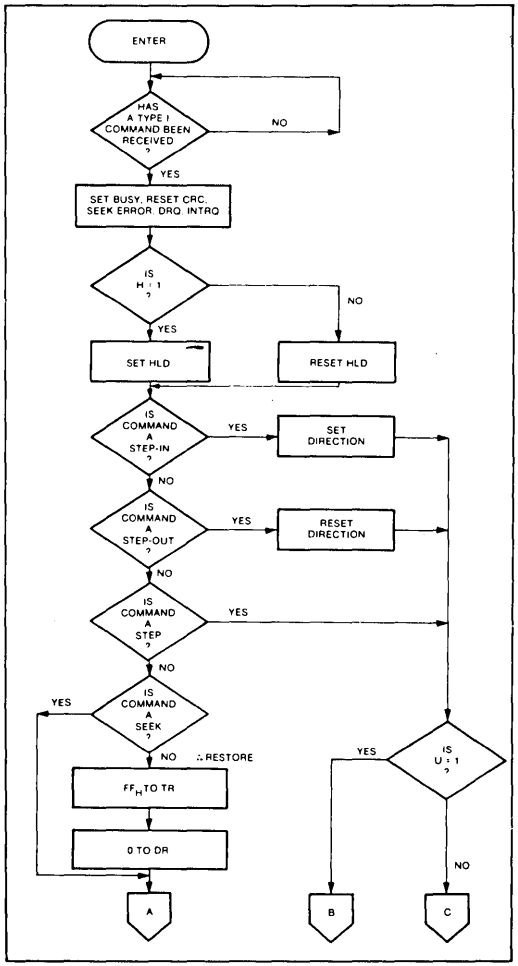
When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD 179X then waits for HLT to occur.

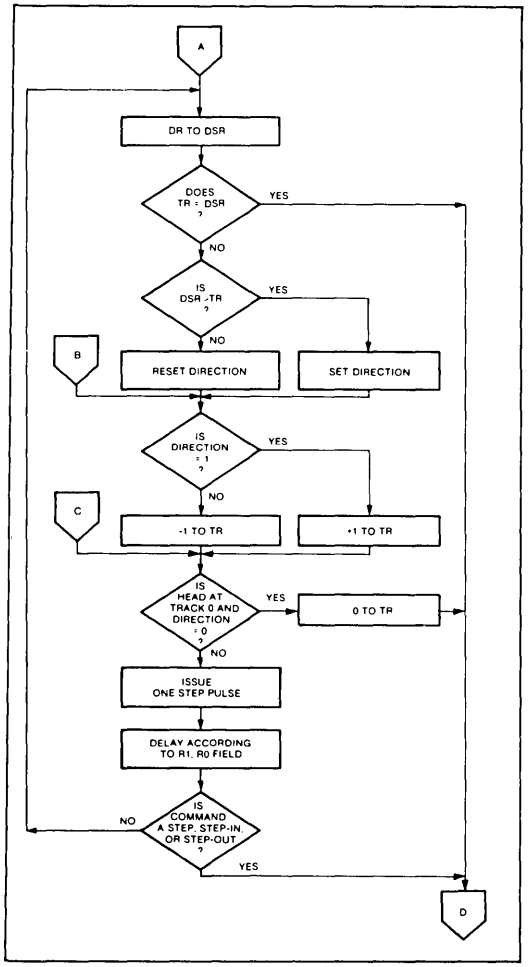
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

Upon receipt of this comand the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state and that the DRQ pin stays low.



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the

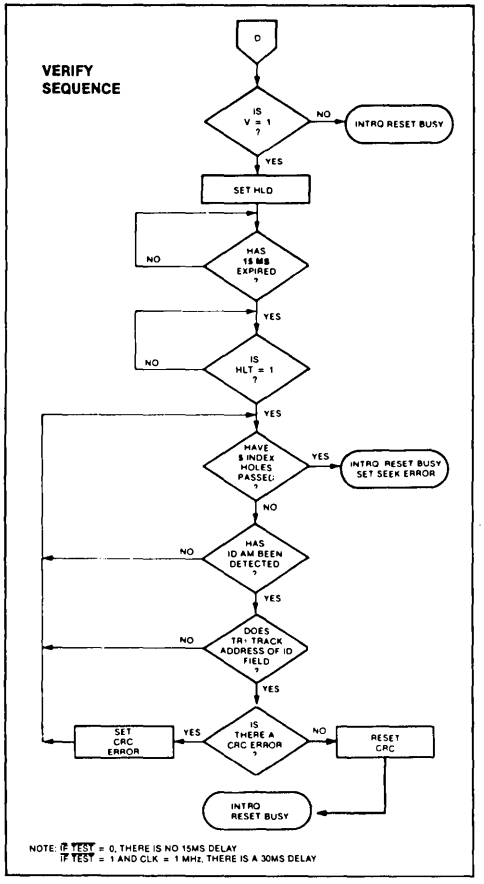
command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 1795 / 7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

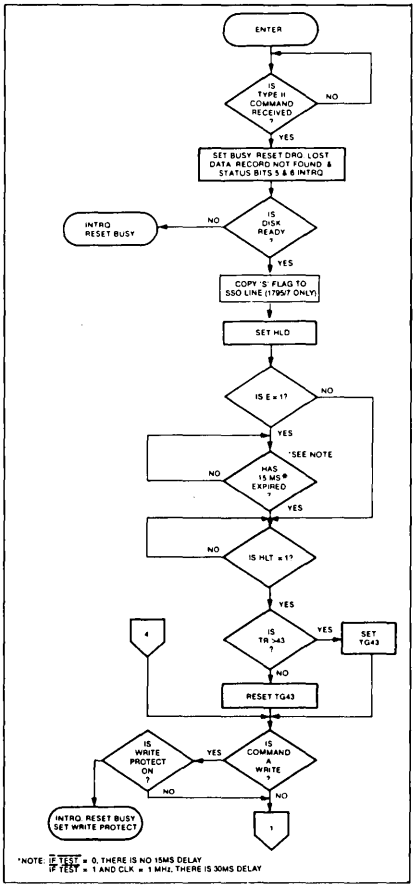


TYPE I COMMAND FLOW

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is ready and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record Not Found status bit is set (Status bit 3) and the command is terminated with an interrupt.

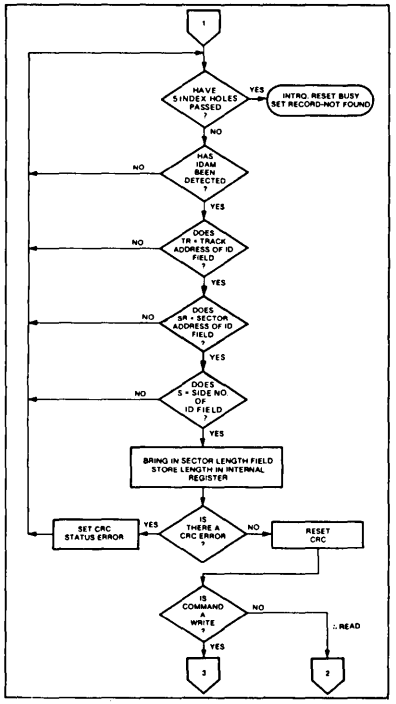


TYPE II COMMAND

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with sector register internally updated so that an address verification can occur on the next record. The WD179X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the FD 179X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD179X will search for 5 disk revolutions, interrupt out, reset busy, and set the Record Not Found status bit.

The Type II commands for 1791-94 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record Not Found status bit is set.



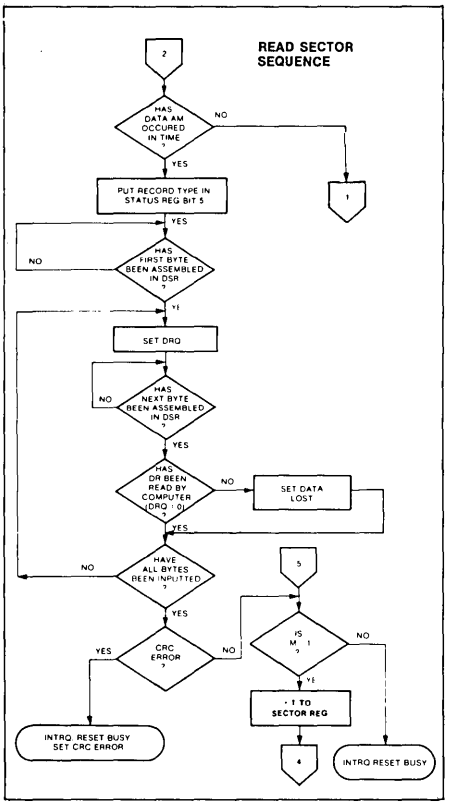
TYPE II COMMAND

The Type II and III commands contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

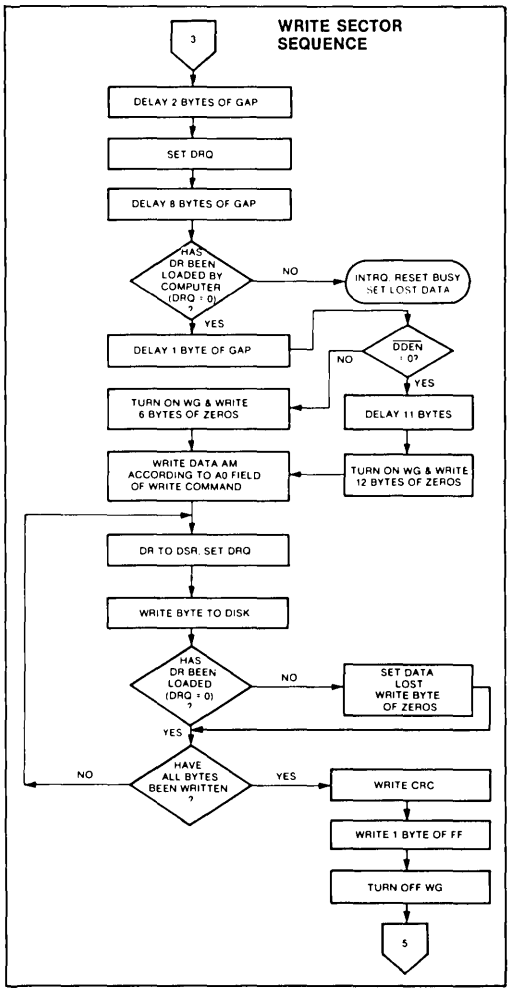
The 1795 / 7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability. the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID filed is searched for and verified again followed by the Data Address Mark search. If after 5 revolutions the DAM cannot be found, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the



TYPE II COMMAND



TYPE II COMMAND

data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Status Data Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector

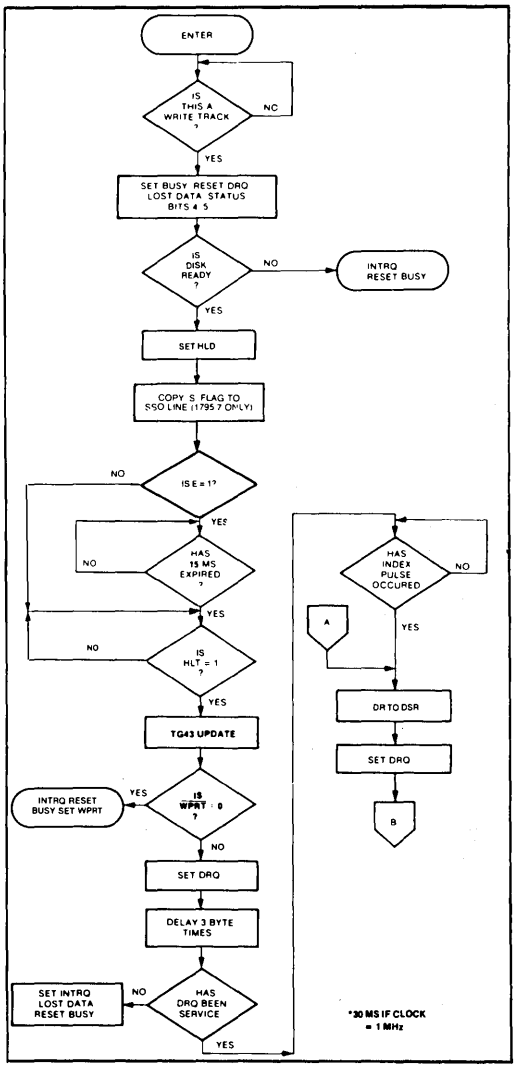
register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

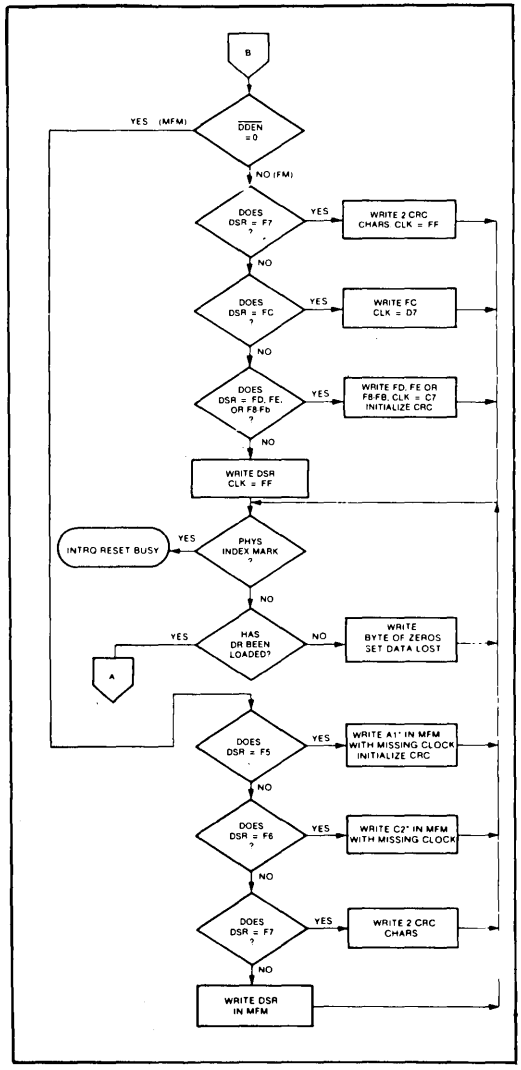
Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WIRTE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM (DDEN = 1)	FD1791 / 3 INTERPRETATION IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4,in MFM
F5	Not Allowed	Write A1* in MFM, Present CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5. **Missing clock transition between bits 3 and 4.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I / O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R / W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continued from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 through FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, of ID fields. Also, CRC's must be generated by an F7 pattern. Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

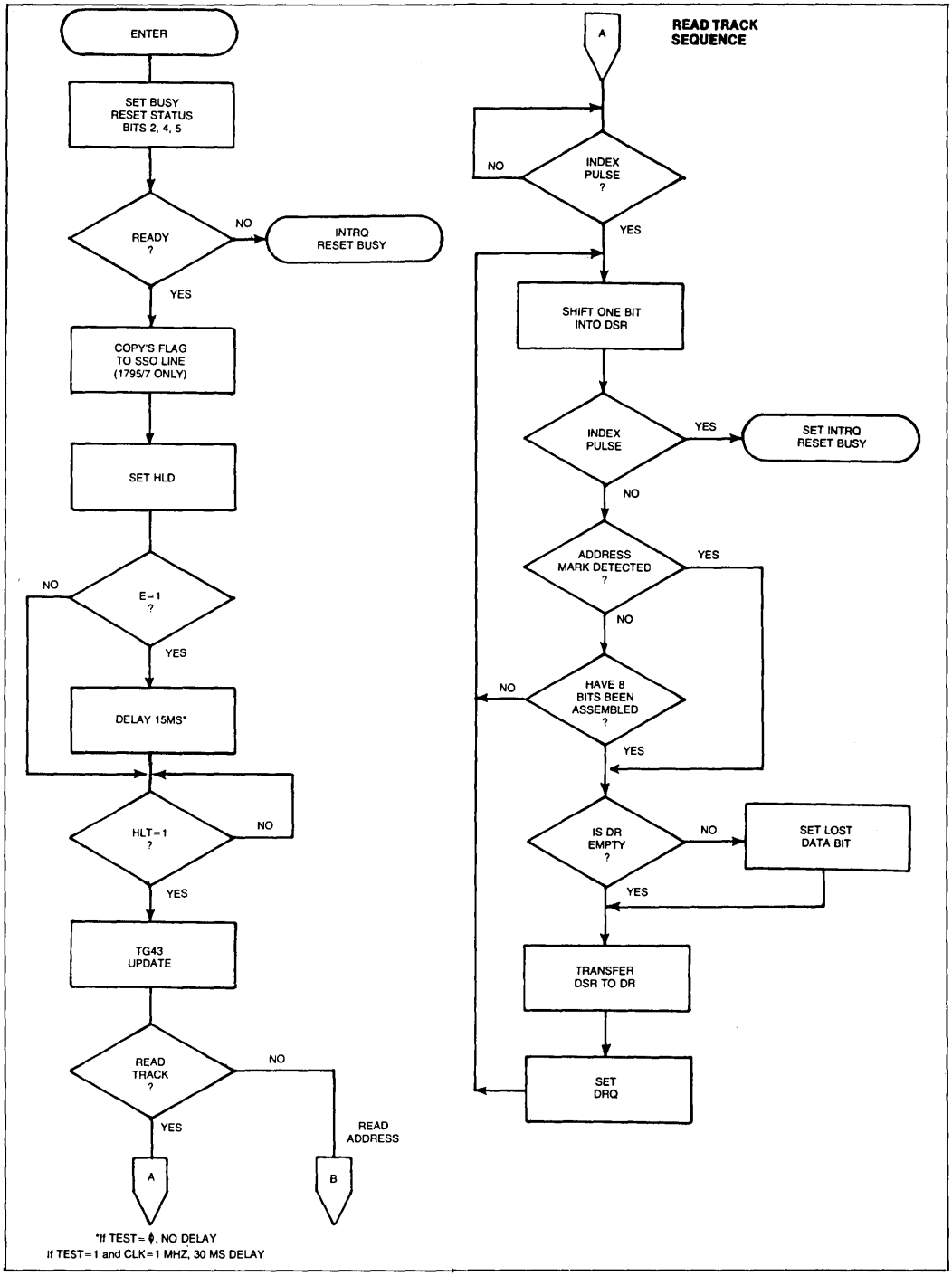
I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Read Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3-I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3-I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

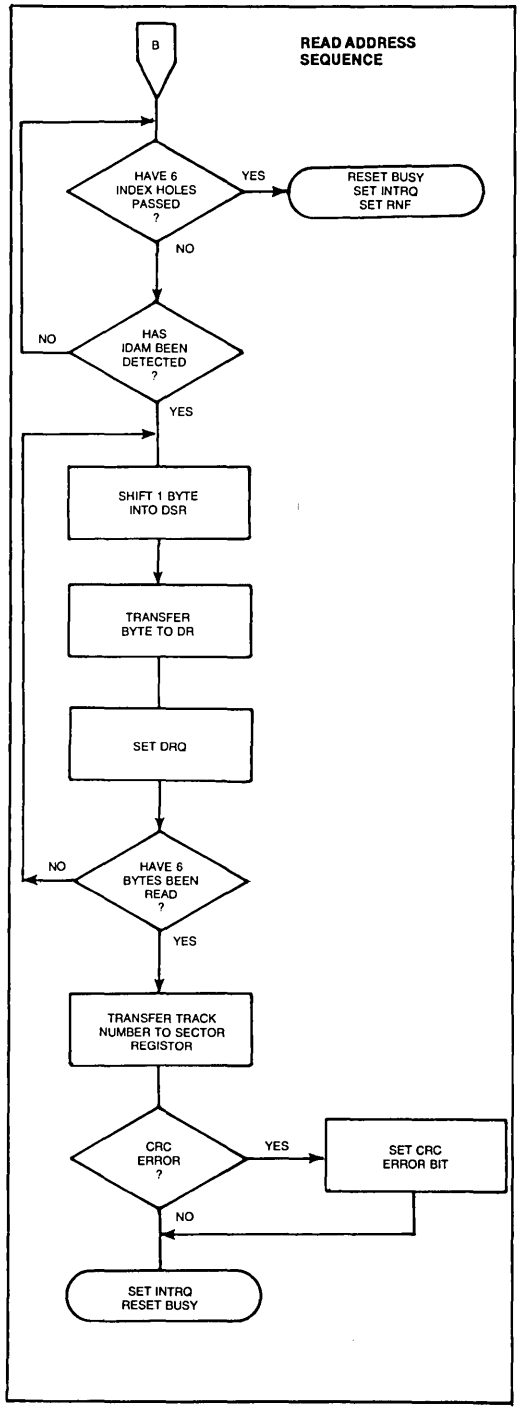
Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.



TYPE III COMMAND

Read Track / Address



TYPE III COMMAND
Read Track / Address

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of that status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

BITS							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I / O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12μs	6μs
Write to Command Reg.	Read Status Bits 1-7	28μs	14μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT - 128 BYTES / SECTOR

Shown below is the IBM single-density format with 128 bytes / sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

IBM 3740 FORMAT - 128 BYTES / SECTOR

Shown below is the IBM single-density format with 128 bytes / sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

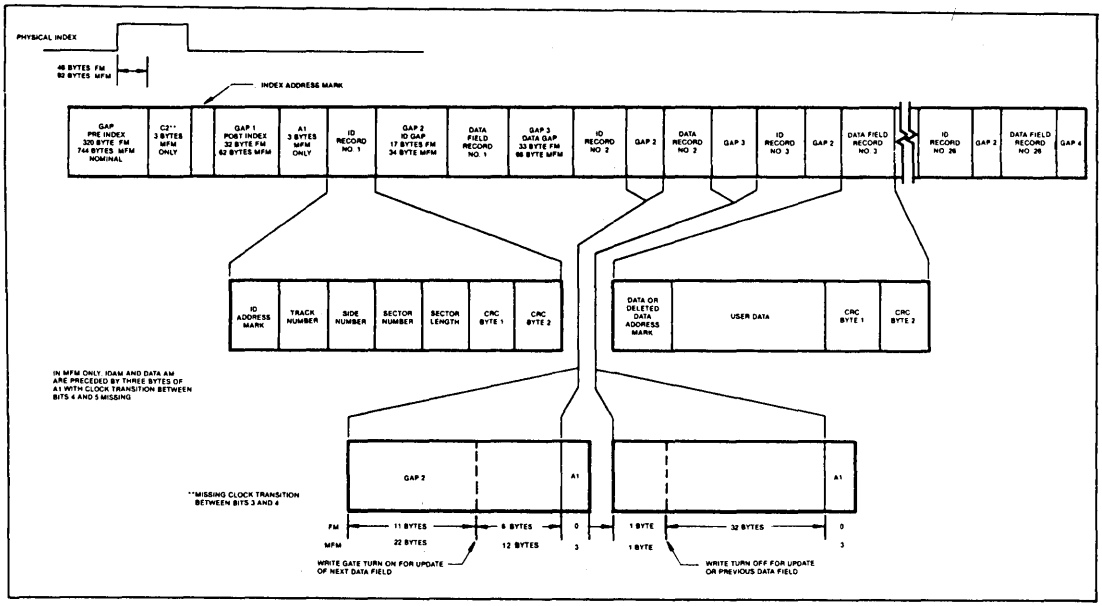
	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	FF (or 00)[1]
	6	00
	1	FC (Index Mark)
*	26	FF (or 00)[1]
	6	00
	1	FE (ID Address Mark)
	1	Track Number
	1	Side Number (00 or 01)
	1	Sector Number (1 thru 1A)
	1	00 (Sector Length)
	1	F7 (2 CRC's written)
	11	FF (or 00)ses E5)[1]
	6	00
	1	FB (Data Address Mark)
	128	Data (IBM uses E5)
	1	F7 (2 CRC's written)
	27	FF (or 00)[1]
	247**	FF (or 00)[1]

*Write bracketed field 26 times.
**Continue writing until FD179X interrupts out. Approx. 247 bytes.
1-Optional '00' on 1795/7 only.

Shown below is the IBM dual-density format with 256 bytes / sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	80	4E
	12	00
	3	F6 (Writes C2)
	1	FC (Index Mark)
*	50	4E
	12	00
	3	F5 (Writes A1)
	1	FE (ID Address Mark)
	1	Track Number (0 thru 4C)
	1	Side Number (0 or 1)
	1	Sector Number (1 thru 1A)
	1	01 (Sector Length)
	1	F7 (2 CRC's written)
	22	4E
	12	00
	3	F5 (Writes A1)
	1	FB (Data Address Mark)
	256	DATA
	1	F7 (2 CRC's written)
	54	4E
	598**	4E

*Write bracketed field 26 times.
**Continue writing until FD179X interrupts out. Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

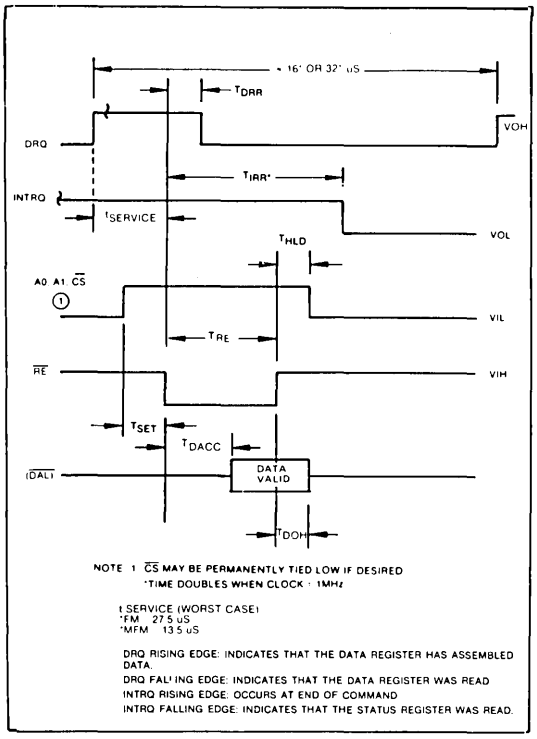
Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512, 1024 bytes.
2) Gap 2 cannot be vaired from the IBM format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the FD179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD179X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



READ ENABLE TIMING

TIMING CHARACTERISTICS

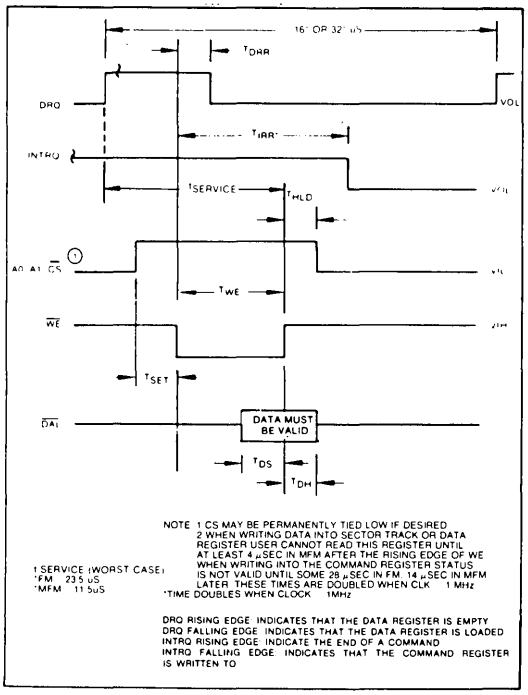
T_A = 0°C to 70°C, V_{DD} = +12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING

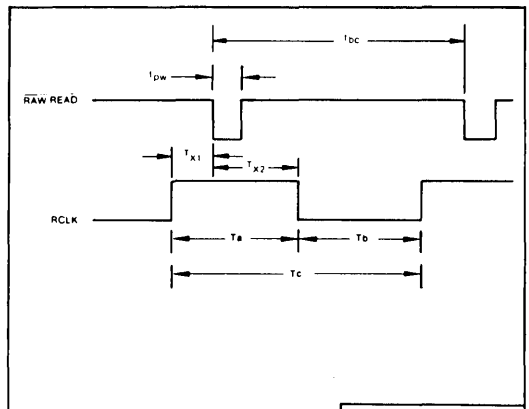
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 50 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 50 pf

WRITE ENABLE TIMING (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDRS & CS TO $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note 5
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$		70		nsec	



WRITE ENABLE TIMING



DISKETTE	MODE	DDEN	CLK	NOMINAL Ta	Tb	Tc
8"	MFM	0	2 MHz	1 μS	1 μS	2 μS
8"	FM	1	2 MHz	2 μS	2μS	4 μS
5"	MFM	0	1 MHz	2 μS	2μS	4 μS
5"	FM	1	1 MHz	4 μS	4 μS	8 μS

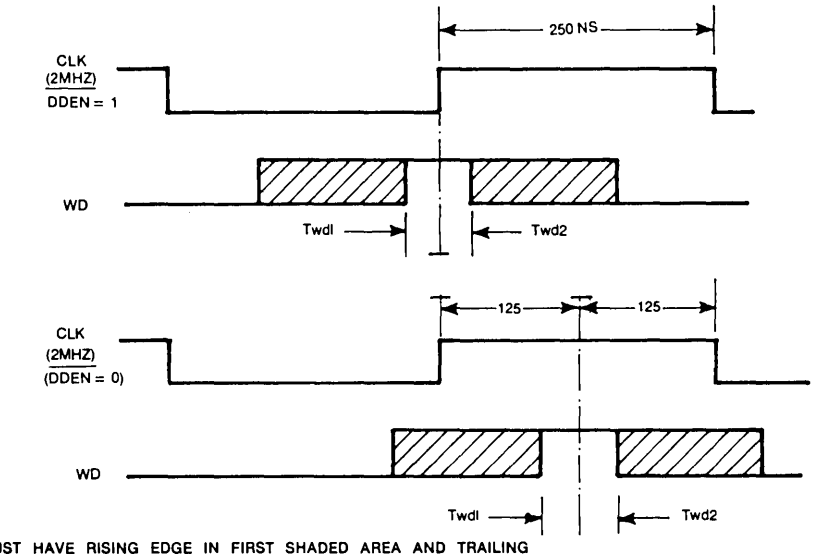
INPUT DATA TIMING

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{PW}	Raw Read Pulse Width	100	200		nsec	See Note 1
T_{BC}	Raw Read Cycle Time	1500	2000		nsec	1800 ns @ 70°C
T_{CK}	RCLK Cycle Time	1500	2000		nsec	1800 ns @ 70°C
T_{X1}	RCLK hold to Raw Read	40			nsec	See Note 1
T_{X2}	Raw Read hold to RCLK	40			nsec	See Note 1

WRITE DATA TIMING:(ALL TIMES DOUBLE WHEN CLK = 1 MHz)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width		500	650	nsec	FM
			200	350	nsec	MFM
Twg	Write Gate to Write DATA		2		μsec	FM
			1		μsec	MFM
Tbc	Write Data Cycle Time		2,3,or 4		μsec	± CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM
Twdl	WD Valid Clk	100			nsec	CLK = 1 MHz
		50			nsec	CLK = 2 MHz
Twd2	WD Valid after CLK	100			nsec	CLK = 1 MHZ
		30			nsec	CLK = 2 MHz



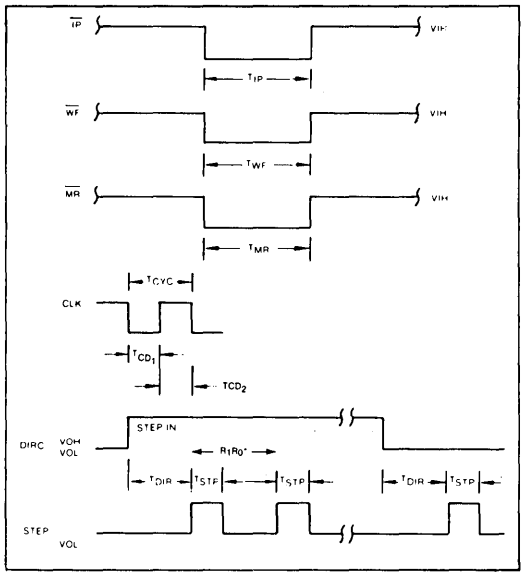
WD MUST HAVE RISING EDGE IN FIRST SHADED AREA AND TRAILING EDGE IN SECOND SHADED AREA.

WRITE DATA/CLOCK RELATIONSHIP

WRITE DATA TIMING

MISCELLANEOUS TIMING: (Times Double When Clock = 1MHz)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230	250	20000	nsec	
TCD_2	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			μsec	See Note 5
TDIR	Dir Setup to Step		12		μsec	± CLK ERROR
TMR	Master Reset Pulse Width	50			μsec	
TIP	Index Pulse Width	10			μsec	See Note 5
TWF	Write Fault Pulse Width	10			μsec	



MISCELLANEOUS TIMING

*FROM STEP RATE TABLE

NOTES:

1. Pulse width on $\overline{\text{RAW READ}}$ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2μs, nominal in MFM and 4μs nominal in FM. Times double when $\overline{\text{CLK}}$ = 1 MHz.
4. RCLK may be high or low during $\overline{\text{RAW READ}}$ (Polarity is unimportant).
5. Times double when clock = 1 MHz.
6. Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically "ored" with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read / Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set, command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and "ORed" with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desire track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

V_{DD} with respect to V_{SS}(ground): +15 to -0.3V

Voltage to any input with respect to V_{SS} = +15 to -0.3V

I_{CC} = 60 MA (35 MA nominal)

I_{DD} = 15 MA (10 MA nominal)

C_{IN} & C_{OUT} = 15 pF max with all pins grounded except one under test.

Operating temperature = 0°C to 70°C

Storate temperature = -55°C to +125°C

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = OV, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{DD}**
I_{OL}	Output Leakage		10	μA	V_{OUT} = V_{DD}
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	I_0 = -100μA
V_{OL}	Output Low Voltage		0.45	V	I_0 = 1.6mA
P_D	Power Dissipation		0.6	W	

*1792 and 1794 I_0 = 1.0 mA

**Leakage conditions are for input pins without internal pull-up resistors. Pins 22, 23, 33, 36, and 37 have pull-up resistors.

FD179X Application Notes

INTRODUCTION

Over the past several years, the Floppy Disk Drive has become the most popular on-line storage device for mini and microcomputer systems. Its fast access time, reliability and low cost-per-bit ratio enables the Floppy Disk Drive to be the solution in mass storage for microprocessor systems. The drive interface to the Host system is standardized, allowing the OEM to substitute one drive for another with minimum hardware/software modifications.

Since Floppy Disk Data is stored and retrieved as a self-clocking serial data stream, some means of separating the clock from the data and assembling this data in parallel form must be accomplished. Data is stored on individual Tracks of the media, requiring control of a stepper motor to move the Read/Write head to a predetermined Track. Byte synchronization must also be accomplished to ensure that the parallel data is properly assembled. After all the design considerations are met, the final controller can consist of 40 or more TTL packages.

To alleviate the burden of Floppy Disk Controller design, Western Digital has developed a Family of LSI Floppy Disk controller devices. Through its own set of macro commands, the FD179X Controller Family will perform all the functions necessary to read and write data to the drive. Both the 8" standard and 5 ¼" mini-floppy are supported with single or double density recording techniques. The FD179X is compatible with the IBM 3740 (FM) data format, or the System 34 (MFM) standards. Provisions for non-standard formats and variable sector lengths have been included to provide more storage capability per track. Requiring standard +5, +12 power supplies, the FD179X is available in a standard 40-pin dual-in-line package.

The FD179X Family consists of 6 devices. The differences between these devices is summarized in Figure 1. The 1792 and 1794 are "single density only" devices, with the Double Density Enable pin ($\overline{\text{DDEN}}$) left open by the user. Both True and inverted Data Bus devices are available. Since the 179X can only drive one TTL Load, a true data bus system may use the 1791 with external inverting buffers to arrive at a true bus scheme. The 1795 and 1797 are identical to the 1791 and 1793, except a side select output has been added that is controlled through the Command Register.

SYSTEM DESIGN

The first consideration in Floppy Disk Design is to determine which type of drive to use. The choice ranges from single-density single sided mini-floppy to the 8" double-density double-sided drive. Figure 2 illustrates the various drive and data capacities associated with each type. Although the 8" double-density drive offers twice as much storage, a more complex data separator and the addition of Write Precompensation circuits are mandatory for reliable data transfers. Whether to go with 8" double-density or not is dependent upon PC board space and the additional circuitry needed to accurately recover data with extreme bit shifts. The byte transfer time defines the nominal time required to transfer one byte of data from the drive. If the CPU used cannot service a byte in this time, then a DMA scheme will probably be required. The 179X also needs a few microseconds for overhead, which is subtracted from the transfer time. Figure 3 shows the actual service times that the CPU must provide on a byte-by-byte basis. If these times are not met, bytes of data will be lost during a read or write operation. For each byte transferred, the 179X generates a DRQ (Data Request) signal on Pin 38. A bit is provided in the Status Register which is also set upon receipt of a byte from the Disk. The user has the option of reading the status register through program control or using the DRQ Line with DMA or interrupt schemes. When the data register is read, both the Status Register DRQ bit and the DRQ Line are automatically reset. The next full byte will again set the DRQ and the process continues until the sector(s) are read. The Write operation works exactly the same way, except a WRITE to the Data Register causes a reset of both DRQ's.

RECORDING FORMATS

The FD179X accepts data from the disk in a Frequency- Modulated (FM) or Modified-Frequency-Modulated (MFM) Format. Shown in Figures 4A and 4B are both these Formats when writing a hexidecimal byte of 'D2.' In the FM mode, the 8 bits of data are broken up into "bit cells." Each bit cell begins with a clock pulse and the center of the bit cell defines the data. If the data bit = 0, no pulse is written; if the data = 1, a pulse is written in the center of the cell. For the 8" drive, each clock is written 4 microseconds apart.

In the MFM mode, clocks are decoded into the data stream. The byte is again broken up into bit cells, with the data bit written in the center of the bit cell if data = 1. Clocks are only written if both surrounding data bits are zero. Figure 4B shows that this occurs only once between bit cell 4 and 5. Using this encoding scheme, pulses can occur 2, 3 or 4 microseconds apart. The bit cell time is now 2 microseconds; twice as much data can be recorded without increasing the Frequency rate due to the encoding scheme.

The 179X was designed to be compatible with the IBM 3740 (FM) and System 34 (MFM) Formats. Although most users do not have a need for data exchange with IBM mainframes, taking advantage of these well studied formats will ensure a high degree of system performance. The 179X will allow a change in gap fields and sector lengths to increase usable storage capacity, but variations away from these standards is not recommended. Both IBM standards are soft-sector format. Because of the wide variation in address marks, the 179X can only support soft-sectored media. Hard sectored diskettes have continued to lose popularity, mainly due to the unavailability of a standard and the limitation of sector lengths imposed by the physical sector holes in the diskette.

PROCESSOR INTERFACE

The Interface of the 179X to the CPU consists of an 8-bit Bi-directional bus, read/write controls and optional interrupt lines. By selecting the device via the CHIP SELECT Line, each of the five internal registers can be accessed.

Shown below are the registers and their addresses:

PIN 3 CS	PIN 6 A_1	PIN 5 A_0	PIN 4 $\overline{RE}=0$	PIN 2 $\overline{WE}=0$
0	0	0	STATUS REG	COMMAND
0	0	1	TRACK REG	REG
0	1	0	SECTOR REG	TRACK REG
0	1	1	DATA REG	SECTOR REG
1	X	X	H1-Z	DATA REG
				H1-Z

Each time a command is issued to the 179X, the Busy Bit is set and the INTRQ (Interrupt Request) Line is reset. The user has the option of checking the Busy Bit or use the INTRQ Line to denote command completion. The Busy Bit will be reset whenever the 179X is idle and awaiting a new command. The INTRQ Line, once set, can only be reset by a READ of the Status Register or issuing a new command. The MR (Master Reset) Line does not affect INTRQ.

The A_0, A_1, Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU address lines, in which case the 179X will be memory-mapped and addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6820, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the 179X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY REQ'D
WRITE TO COMMAND REG	READ STATUS REGISTER	MFM = 14μ s* FM = 28μ s
WRITE TO ANY REGISTER	READ FROM A DIFFERENT REG	NO DELAY

*NOTE: Times Double when CLK = 1MHz (5¼" drive).

Other CPU interface lines are CLK, $\overline{MR}$ and $\overline{DDEN}$. The CLK line should be 2 MHz (8" drive) or 1 MHz (5 ¼" drive) with a 50% duty cycle. Accuracy should be +1% (crystal source) since all internal timing, including stepping rates, are based upon this clock.

The $\overline{MR}$ or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a Restore Command (Hex '03') on the rising edge. A quicker stepping rate can be written to the Command Register after a $\overline{MR}$, in which case the remaining steps will occur at the faster programmed rate. The 179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{TR00}$ line to go active low. This line should be connected to the drive's $\overline{TR00}$ sensor.

The $\overline{DDEN}$ line causes selection of either single density ($\overline{DDEN}$ = 1) or double density operation. $\overline{DDEN}$ should not be switched during a read or write operation.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the 179X. Inputs to the 179X may be buffered or tied to the drive's outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed -0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with a period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\overline{IP}$ or Index Pulse. This Line is tied to the drives Index L.E.D. sensor and makes an active transition for each revolution of the diskette. The $\overline{TR00}$ Line is another L.E.D. sensor that informs the 179X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open," Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The 179X will look at the ready signal prior to executing READ/WRITE commands. READY is *not* inspected during any Type I commands. All Type I commands will execute regardless of the Logic Level on this Line.

WRITE SIGNALS

Writing of data is accomplished by the use of the WD, WG, WF, TG43, EARLY and LATE Lines. The WG or Write Gate Line is used to enable write current at the drive's R/W head. It is made active prior to writing data on the disk. The WF or WRITE FAULT Line is used to inform the 179X of a failure in drive electronics. This signal is multiplexed with the VFOE Line and must be logically separated if required. Figure 5 illustrates three methods of demultiplexing.

The TG43 or "TRACK GREATER than 43" Line is used to decrease the Write Current on the inner tracks, where bit densities are the highest. If not required on the drive, TG43 may be left open.

WRITE PRECOMPENSATION

The 179X provides three signals for double density Write Precompensation use. These signals are WRITE DATA, EARLY and LATE. When using single density drives (eighter 8" or 5 1/4"), Write Precompensation is not necessary and the WRITE DATA line is generally TTL Buffered and sent directly to the drive. In this mode, EARLY and LATE are left open.

For double density use, Write Precompensation is a function of the drive. Some manufacturers recommend Precompensating the 5 1/4" drive, while others do not.

With the 8" drive, Precompensation may be specified from TRACK 43 on, or in most cases, all TRACKS. If the recommended Precompensation is not specified, check with the manufacturer for the proper configuration required.

The amount of Precompensation time also varies. A typical value will usually be specified from 100-300ns. Regardless of the parameters used, Write Precompensation must be done external to the 179X. When DDEN is tied low, EARLY or LATE will be activated at least 125ns. before and after the Write Data pulse. An Algorithm internal to the 179X decides whether to raise EARLY or LATE, depending upon the previous bit pattern sent. As an example, suppose the recommended Precomp value has been specified at 150ns. The following action should be taken:

EARLY	LATE	ACTION TAKEN
0	0	delay WD by 150 ns (nominal)
0	1	delay WD by 300ns (2X value)
1	0	do not delay WD

There are two methods of performing Write Precompensation:

1) External Delay elements
2) Digitally

Shown in Figure 6 is a Precomp circuit using the Western Digital 2143 clock generator as the delay element. The WD pulse from the 179X creates a strobe to the 2143, causing subsequent output pulses on the 01, 02 and 03 signals. The 5K Precomp adjust sets the desired Precomp value. Depending upon the condition of EARLY and LATE, 01 will be used for EARLY, 02 for nominal (EARLY = LATE = 0), and 03 for LATE. The use of "one-shots" or delay line in a Write Precompensation scheme offers the user the ability to vary the Precomp value. The 04 output resets the 74LS175 Latch in anticipation of the next WD pulse. Figure 7 shows the WD-EARLY/LATE relationship, while Figure 8 shows the timing of this write Precomp scheme.

Another method of Precomp is to perform the function digitally. Figure 9 illustrates a relationship between the WD pulse and the CLK pin, allowing a digital Precomp scheme. Figure 10 shows such a scheme with a preset Write Precompensation value of 250ns. The synchronous counter is used to generate 2 MHz and 4 MHz clock signals. The 2MHz clock is sent to the CLK input of the 179X and the 4 MHz is used by the 4-bit shift register. When a WD pulse is not present, the 4 MHz clock is shifting "ones" through the shift register and maintaining Q_D at a zero level. When a WD pulse is present, a zero is loaded at either A, B, or C depending upon the states of LATE, EN PRECOMP and EARLY. The zero is then shifted by the 4 MHz clock until it reaches the Q_D output. The number of shift operations determines whether the WRITE DATA pulse is written early, nominal or late. If both FM and MFM operations is a system requirement, the output of this circuit should be disabled and the WD pulse should be sent directly to the drive.

DATA SEPARATION

The 179X has two inputs (RAW READ & RCLK) and one output (VFOE) for use by an external data separator. The RAW READ input must present clock and data pulses to the 179X, while the RCLK input provides a "window" or strobe signal to clock each RAW READ pulse into the device. An ideal Data Separator would have the leading edge of the RAW READ pulse occur in the exact center of the RCLK strobe.

Motor Speed Variation, Bit shifts and read amplifier recovery circuits all cause the RAW READ pulses to drift away from their nominal positions. As this occurs, the RAW READ pulses will shift left or right with respect to RCLK. Eventually, a pulse will make its transition outside of its RCLK window, causing either a CRC error or a Record-Not-Found error at the 179X.

A Phase-Lock-Loop circuit is one method of achieving synchronization between the RCLK and RAW READ signals. As RAW READ pulses are fed to the PLL, minor adjustments of the free-running RCLK frequency can be made. If pulses are occurring too far apart, the RCLK frequency is *decreased* to keep synchronization. If pulses begin to occur closer together, RCLK is *increased* until this new higher frequency is achieved. In normal read operations, RCLK will be constantly adjusted in an attempt to match the incoming RAW READ frequency.

Another method of Data Separation is the Counter-Separator technique. The RCLK signal is again free-running at a nominal rate, until a RAW READ pulse occurs. The Separator then denotes the position of the pulse with respect to RCLK (by the counter value), and counts down to increase or decrease the current RCLK window. The next RCLK window will occur at a nominal rate and will continue to run at this frequency until another RAW READ pulse adjusts RCLK, but only the present window is adjusted.

Both PPL and Counter/Separator are acceptable methods of Data Separation. The PPL has the highest reliability because of its "tracking" capability and is recommended for 8" double density designs.

As a final note, the term "Data Separator" may be misleading, since the physical separation of clock and data bits are not actually performed. This term is used throughout the industry, and can better be described as a "Data Recovery Circuit" rather than a Data Separator.

The VFOE signal is an output from the 179X that signifies the head has been loaded and valid data pulses are appearing on the RAW READ line. It can be used to enable the Data Separator and to insure clean RCLK transitions to the 179X. Since some drives will output random pulses when the head is disengaged, VFOE can prevent an erratic RCLK signal during this time. If the Data Separator requires synchronization during a known pattern of one's or zero's, then RG (READ GATE) can be used. The RG signal will go active when the 179X is currently over a field of zero's or ones. RG is not available on the 1795/1797 devices, since this signal was replaced with the SSO (Side Select Output) Line.

Shown in Figure 11 is a 2½ IC Counter/Separator. The 74LS193 free runs at a frequency determined by the CRYCLK input. When a RAW READ pulse occurs, the counter is loaded with a starting count of '5.' When the RAW READ Line returns to a Logic 1, the counter counts down to zero and again free runs. The 74LS74 insures a 50% duty cycle to the 179X and performs a divide-by-two of the $Q_D$output.

Figure 12 illustrates another Counter/Separator utilizing a PROM as the count generator. Depending upon the RAW READ phase relationship to RCLK, the PROM is addressed and its data output is used as the counter value. A 16 MHz clock is required for 8" double density, while an 8 MHz clock can be used for single density.

Figure 13 shows a Phase-Lock-Loop data recovery circuit. The phase detector (U2, Figure 2) compares the phase of the SHAPED DATA pulse to the phase of VFO CLK 2. If VFO CLK 2 is lagging the SHAPED DATA pulse an output pulse on #9, U2 is generated. The filter/amplifier converts this pulse into a DC signal which increases the frequency of the VCO.

If, correspondingly, CLK 2 is leading the SHAPED DATA pulse, an output pulse on #5, U2 is generated. This pulse is converted into a DC signal which decreases the frequency of the VCO. These two actions cause the VCO to track the frequency of the incoming READ DATA pulses. This correction process to keep the two signals in phase is constantly occurring because of spindle speed variation and circuit parameter variations.

The operating specifications for this circuit are as follows:

Free Running Frequency	2 MHz
Capture Range	+ 15%
Lock Up Time	50 microsec. "1111" or "0000" Pattern 100 Microsec "1010" Pattern

The RAW READ pulses are generated from the falling edge of the SHAPED DATA pulses. The pulses are also reshaped to meet the 179X requirements. VFO CLK 2 OR 4 is divided by 2 once again to obtain VFO CLK OUT whose frequency is that required by the 179X RCLK input. RCLK must be controlled by VFOE so VFOE is sampled on each rising edge of VFO CLK OUT. When VFOE goes active EN RCLK goes active in synchronization with VFO CLK OUT preventing any glitches on the RCLK output. When VFOE goes inactive EN RCLK goes inactive in synchronization with VFO CLK OUT, again preventing any glitches on the RCLK output.

Figure 14 illustrates a PPL data recovery circuit using the Western Digital 1691 Floppy Support device. Both data recovery and Write Precomp Logic is contained within the 1691, allowing low chip count and PLL

reliability. The 74S124 supplies the free-running VCO output. The PUMP UP and PUMP DOWN signals from the 1691 are used to control the 74S124's frequency.

COMMAND USAGE

Whenever a command is successfully or unsuccessfully completed, the busy bit of the Status Register is reset and the INTRQ line is forced high. Command termination may be detected either way. The INTRQ can be tied to the host processor's interrupt with an appropriate service routine to terminate commands. The busy bit may be monitored with a user program and will achieve the same results through software. Performing both an INTRQ and a busy bit check is not recommended because a read of the Status Register to determine the condition of the busy bit will reset the INTRQ line. This can cause an INTRQ from not occurring.

RESTORE COMMAND

On some disk drives, it is possible to position the R/W head outward past Track 00 and prevent the TR00 line from going low unless a STEP IN is first performed. If this condition exists in the drive used, the RESTORE command will never detect a TR00. Issuing several STEP IN pulses before a RESTORE command will remedy this situation. The RESTORE and all other Type I commands will execute even though the READY bit indicates the drive is not ready (NOT READY = 1).

READ TRACK COMMAND

The READ TRACK command can be used to manually inspect data on a hard copy printout. Gaps, address marks and all data are brought in to the Data Register during this command. The READ TRACK command may be used to inspect diskettes for valid formatting and data fields as well as address marks. Since the 179X does not synchronize clock and data until the Index Address Mark is detected, data previous to this ID mark will not be valid. READ GATE (RG) is not actuated during this command.

READ ADDRESS COMMAND

In systems that use either multiple drives or sides, the read address command can be used to tell the host processor which drive or side is selected. The current position of the R/W head is also denoted in the six bytes of data that are sent to the computer.

TRACK SIDE	SECTOR	CRS LENGTH	CRC 1	CRC 2

The READ ADDRESS command as well as all other Type II and Type III commands will not execute if the READY line is inactive (READY = 0). Instead, an interrupt will be generated and the NOT READY status bit will be set to a 1.

FORCED INTERRUPT COMMAND

The Forced Interrupt command is generally used to terminate a multiple sector command or to insure Type I status in the Status Register. The lower four bits of the command determine the conditional interrupt as follows:

I_0 = NOT-READY TO READY TRANSITION
I_1 = READY TO NOT-READY TRANSITION
I_2 = EVERY INDEX PULSE
I_3 = IMMEDIATE INTERRUPT

Regardless of the conditional interrupt set, any command that is currently being executed when the Forced Interrupt command is loaded will immediately be terminated and the Busy Bit will be reset indicating an idle condition.

Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occured.

The conditional interrupt is enabled when the corresponding bit positions of the command (I3 - I0) are set to a 1. If I_3 - I_0 are all set to zero, no interrupt will occur, but any command presently under execution will be immediately terminated upon receipt of the Force Interrupt command (HEX D0).

As usual, to clear the interrupt a read of the Status Register or a write to the command register is required. The exception is when using the immediate interrupt condition (I_3 = 1). If this command is loaded into the command register, an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt; another forced interrupt command with I_3 - I_0 = 0 must be loaded into the command register in order to reset the INTRQ from this condition.

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition I_1 = 1 and the Every Index Pulse I_2 = 1 are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

DATA RECOVERY

Occasionally, the R/W head of the disk drive may get "off track", and dust and dirt may get trapped on the media. Both of these conditions will cause a RECORD NOT FOUND and/or a CRC error to occur. This "soft error" can usually be recovered by the following procedure:

1. Issue the command again
2. Unload and load the head and repeat step
3. Issue a restore, seek the track, and repeat step 1

If RNF or CRC errors are still occurring after trying these methods, a "hard error" may exist. This is usually caused by improper disk handling, exposure to high magnetic fields, etc. and generally results in destroying portions or tracks of the diskette.

FIGURE 1. DEVICE CHARACTERISTICS

DEVICE	SNGL DENSITY	DBLE DENSITY	INVERTED BUS	TRUE BUS	DOUBLE-SIDED
1791	X	X	X		
1792	X		X		
1793	X	X		X	
1794	X			X	
1795	X	X	X		X
1797	X	X		X	X

FIGURE 2. STORAGE CAPACITIES

SIZE	DENSITY	SIDES	UNFORMATTED CAPACITY (NOMINAL)		BYTE TRANSFER TIME	FORMATTED CAPACITY	
			PER TRACK	PER DISK		PER TRACK	PER DISK
5 1/4"	SINGLE	1	3125	109,375*	64μs	2304**	80,640
5 1/4"	DOUBLE	1	6250	218,750	32μs	4608***	161,280
5 1/4"	SINGLE	2	3125	218,750	64μs	2304	161,280
5 1/4"	DOUBLE	2	6250	437,500	32μs	4608	322,560
8"	SINGLE	1	5208	401.016	32μs	3328	256,256
8"	DOUBLE	1	10,416	802,032	16μs	6656	512,512
8"	SINGLE	2	5208	802,032	32μs	3328	512,512
8"	DOUBLE	2	10,416	1,604,064	16μs	6656	1,025,024

*Based on 35 Tracks/Side.
**Based on 18 Sectors/Track (128 byte/sec).
***Based on 18 Sectors/Track (256 bytes/sec).

FIGURE 3. NOMINAL VS. WORST CASE SERVICE TIME

SIZE	DENSITY	NOMINAL TRANSFER TIME	WORST-CASE 179X SERVICE TIME	
			READ	WRITE
5 1/4"	SINGLE	64μs	55.0μs	47.0μs
5 1/4"	DOUBLE	32μs	27.5μs	23.5μs
8"	SINGLE	32μs	27.5μs	23.5μs
8"	DOUBLE	16μs	13.5μs	11.5μs

FIGURE 4A. FM RECORDING

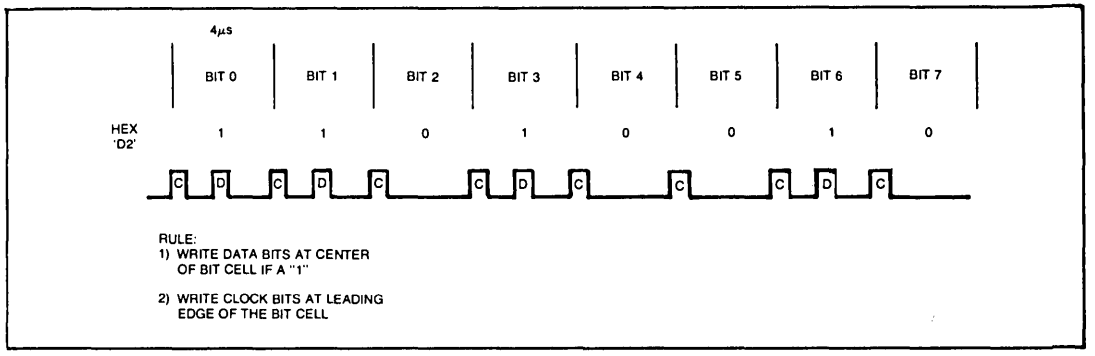


FIGURE 4B. MFM RECORDING

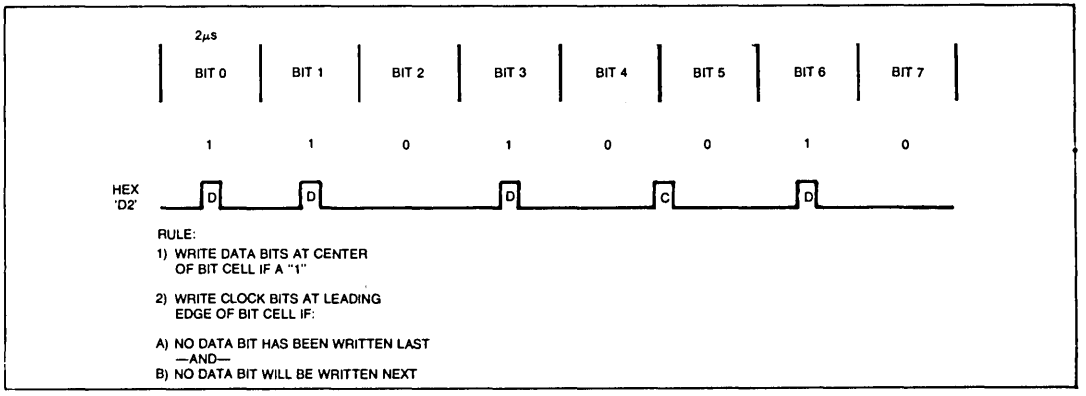
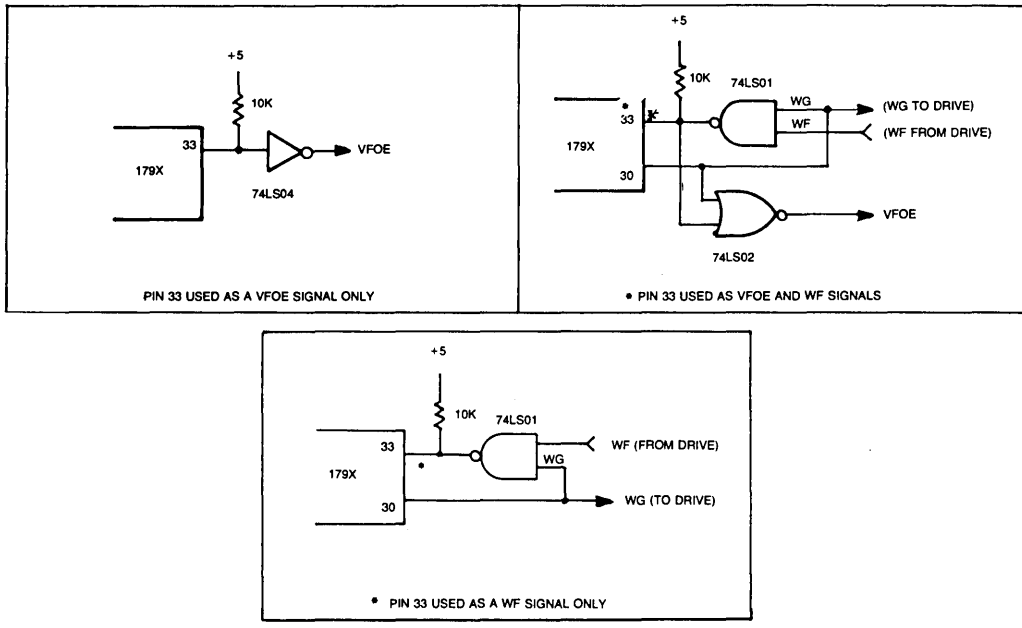


FIGURE 5. WF / VFOE DEMULTIPLEXING CIRCUITRY



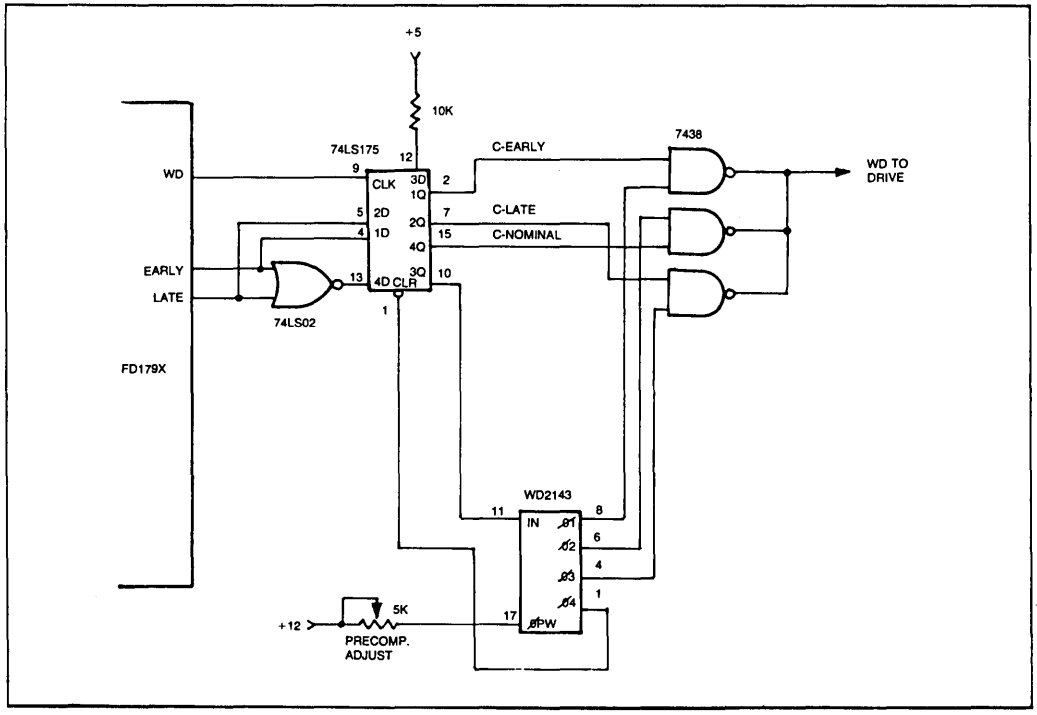


FIGURE 6. 179X WRITE PRE-COMP

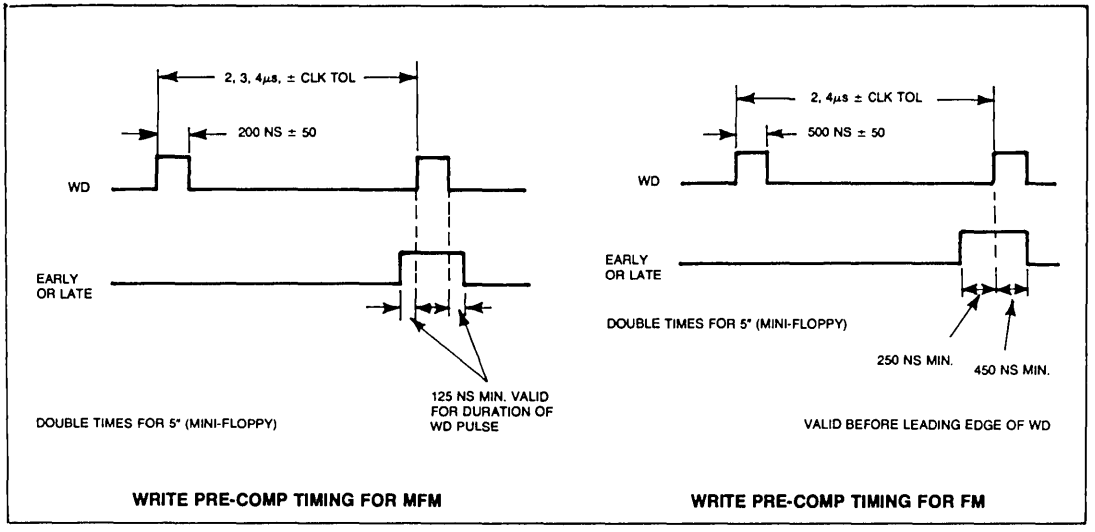


FIGURE 7. WRITE PRE-COMP TIMING

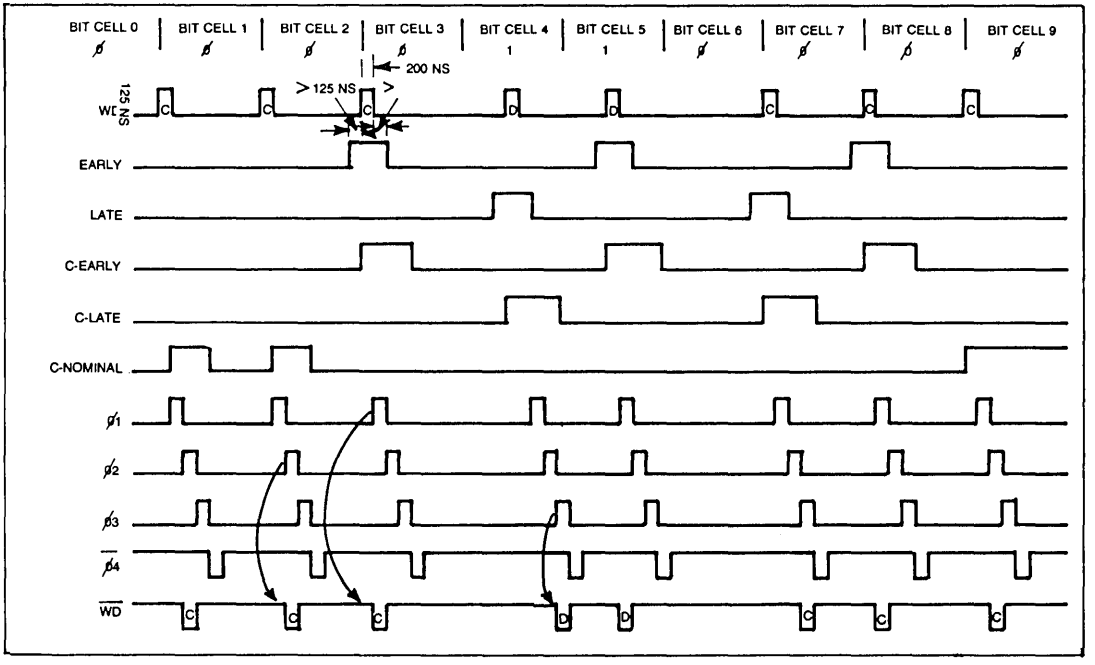


FIGURE 8. PRE-COMP TIMING FOR CIRCUIT IN FIGURE 6

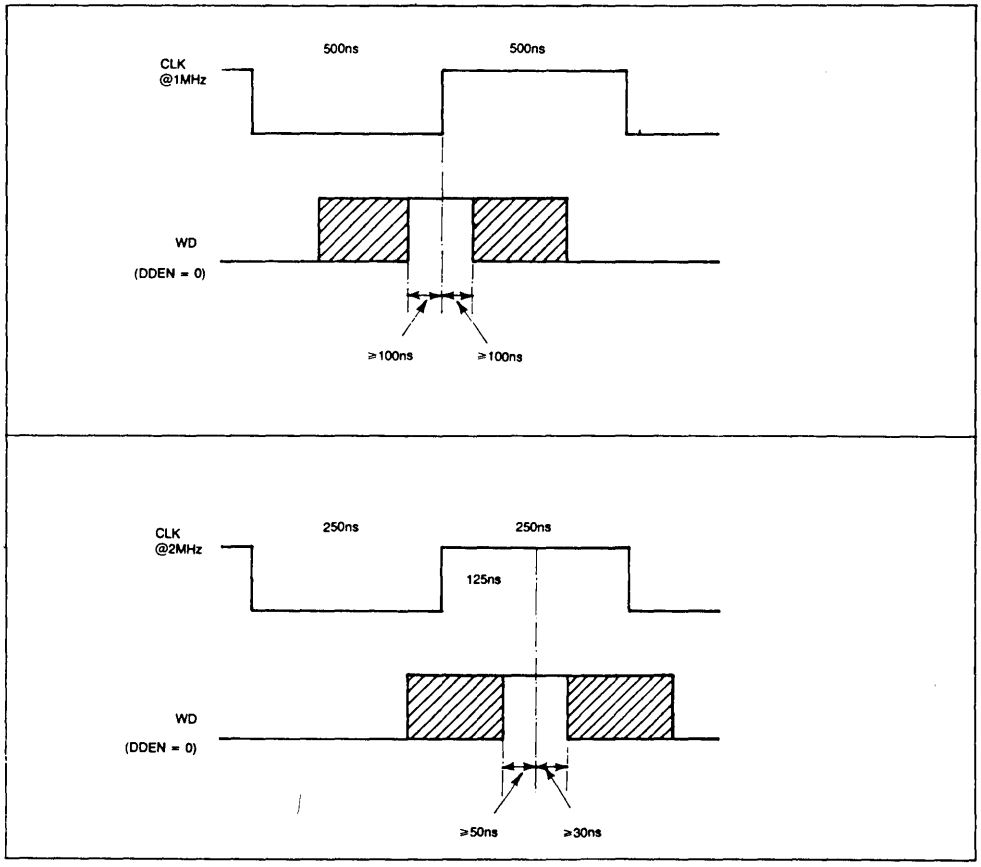


FIGURE 9. WD/CLK RELATIONSHIP FOR WRITE PRECOMP USE

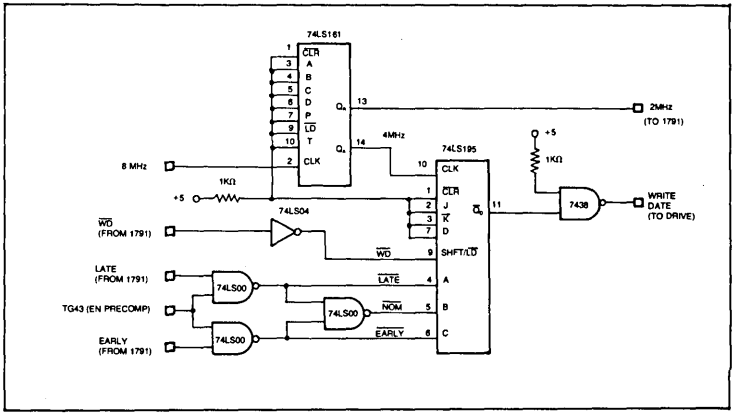
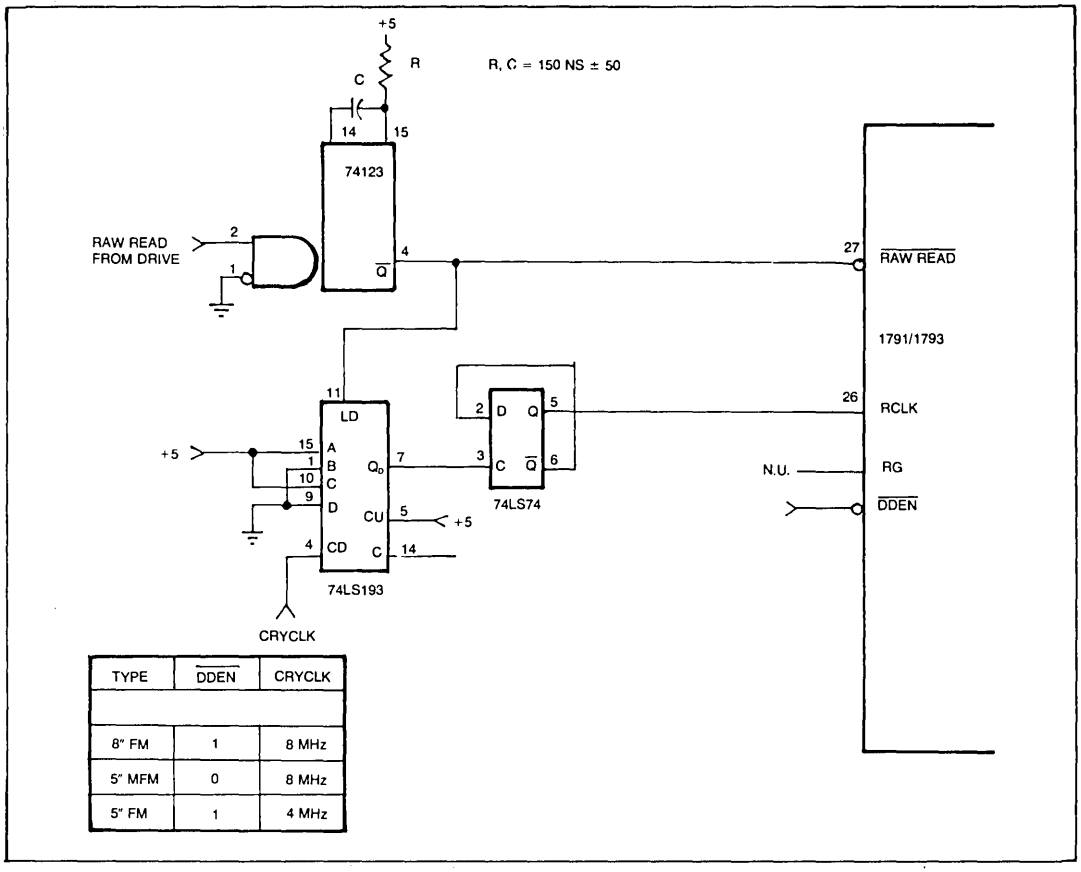
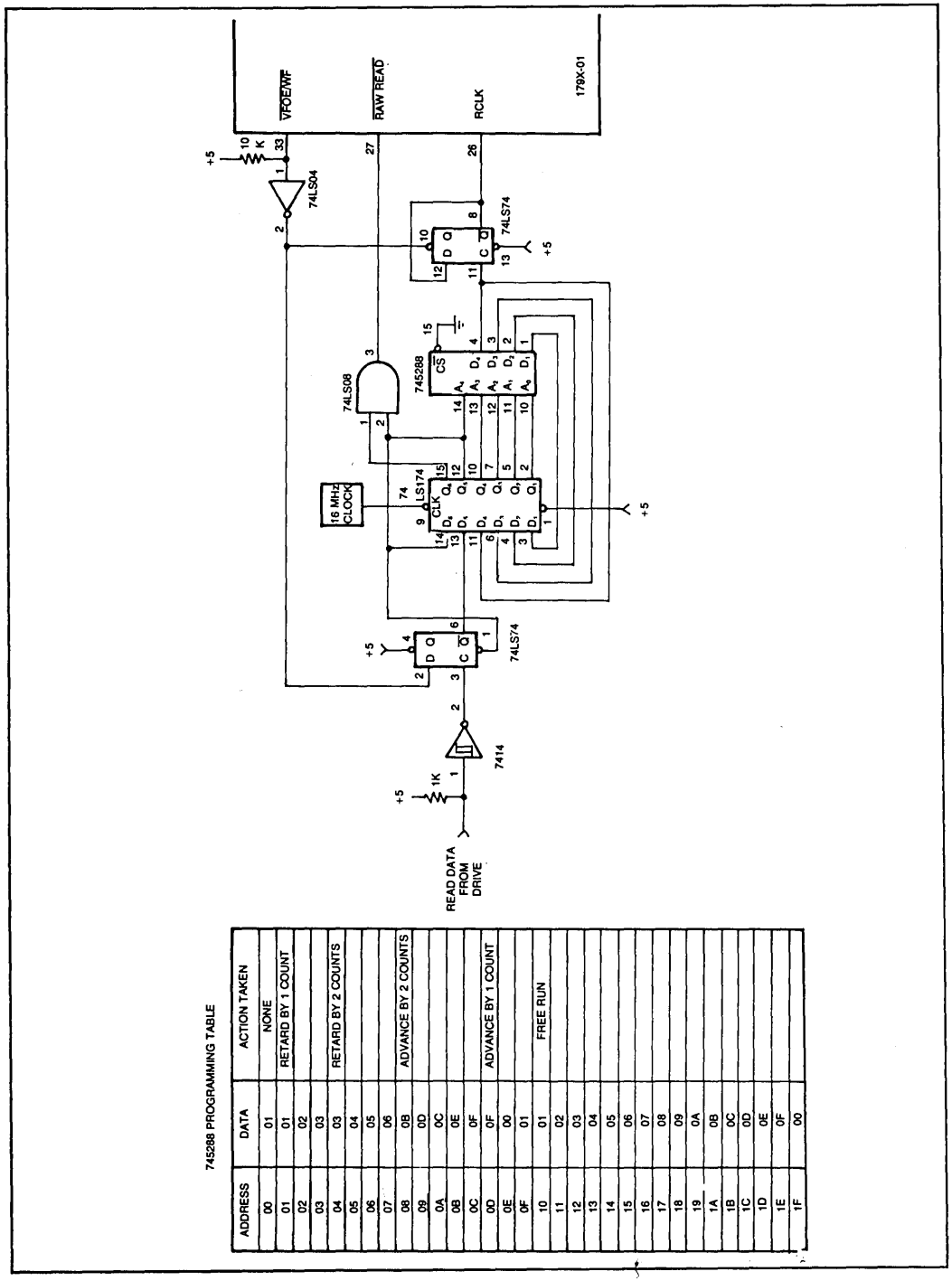


FIGURE 10. DIGITAL WRITE PRECOMP CIRCUIT
(PROVIDED COURTESY OF MPI, OKLAHOMA CITY, OK 73112)



TYPE	$\overline{\text{DDEN}}$	CRYCLK
8" FM	1	8 MHz
5" MFM	0	8 MHz
5" FM	1	4 MHz

FIGURE 11. COUNTER / SEPARATOR



745288 PROGRAMMING TABLE

ADDRESS	DATA	ACTION TAKEN
00	01	NONE
01	01	RETARD BY 1 COUNT
02	02	
03	03	RETARD BY 2 COUNTS
04	03	
05	04	
06	05	
07	06	
08	08	ADVANCE BY 2 COUNTS
09	0D	
0A	0C	
0B	0E	
0C	0F	
0D	0F	ADVANCE BY 1 COUNT
0E	00	
0F	01	FREE RUN
10	01	
11	02	
12	03	
13	04	
14	05	
15	06	
16	07	
17	08	
18	09	
19	0A	
1A	0B	
1B	0C	
1C	0D	
1D	0E	
1E	0F	
1F	00	

FIGURE 12. 179X DATA SEPARATOR
(PROVIDED COURTESY OF ANDROMEDA SYSTEMS, PANORAMA CITY, CA 91402)

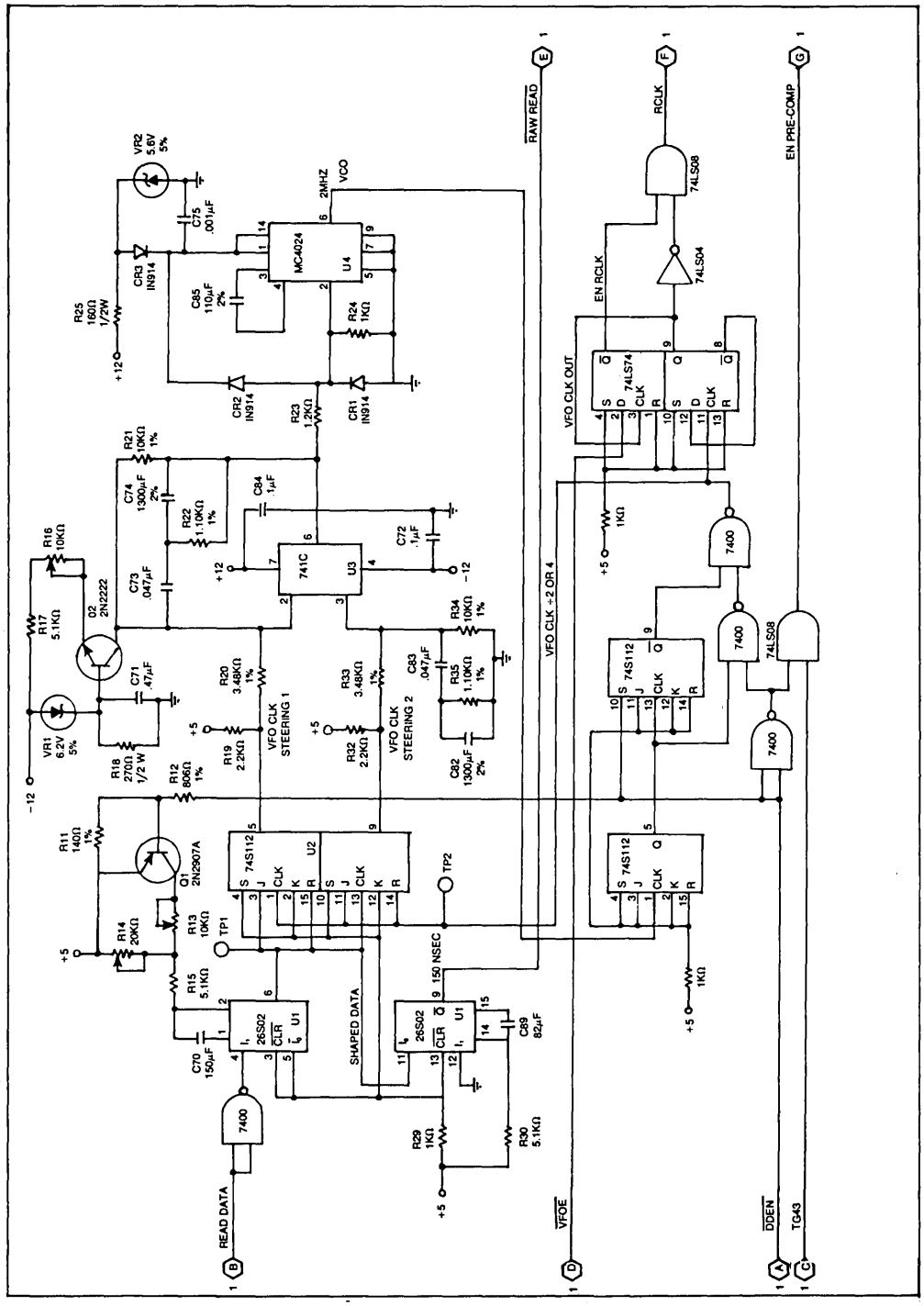


FIGURE 13. PLL DATA RECOVERY CIRCUIT
(PROVIDED COURTESY OF MPI, OKLAHOMA CITY, OK 73112)

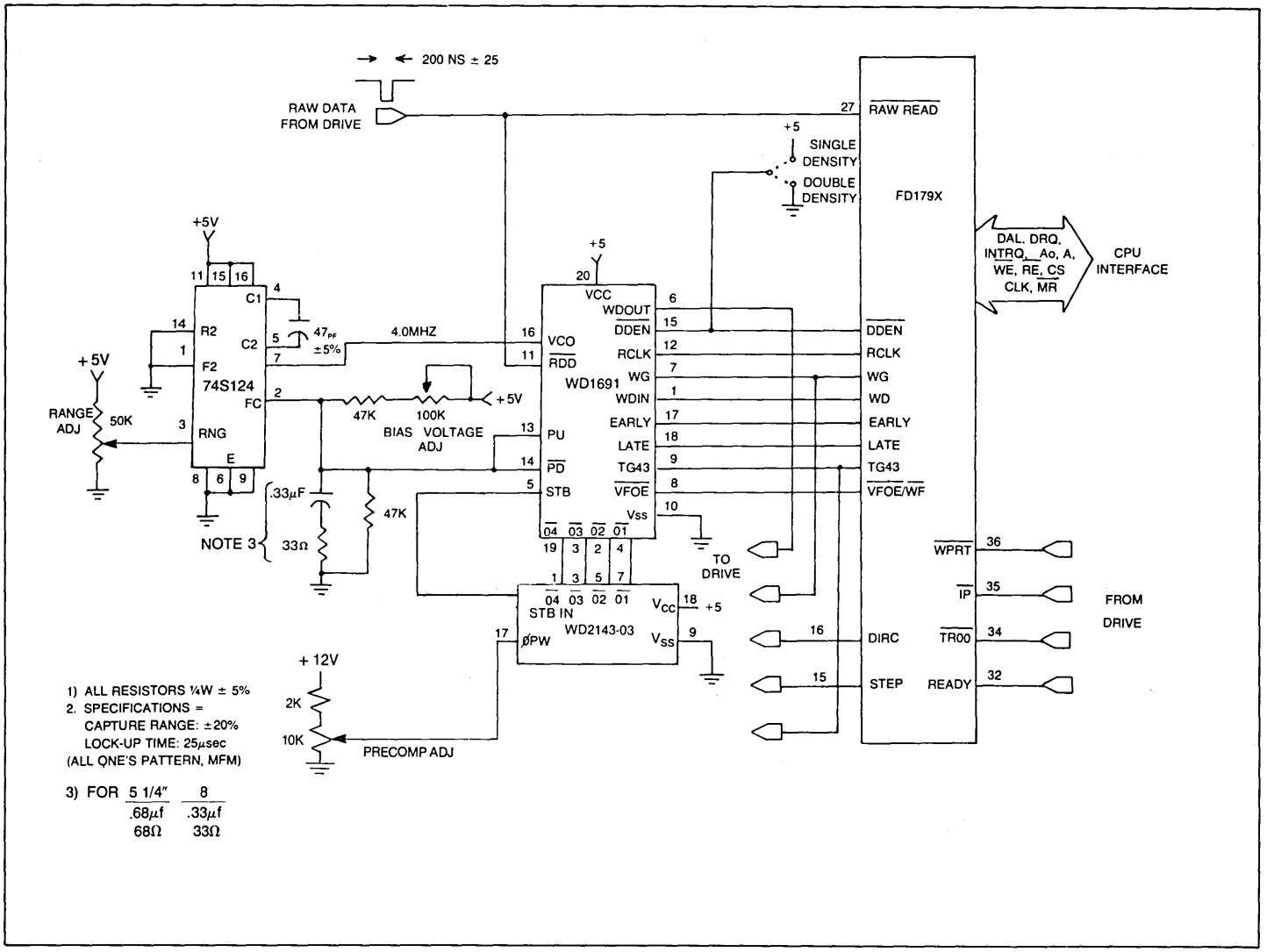


FIGURE 14. 8" SINGLE / DOUBLE DENSITY SYSTEM

WD279X-02 Floppy Disk Formatter/Controller Family

FEATURES

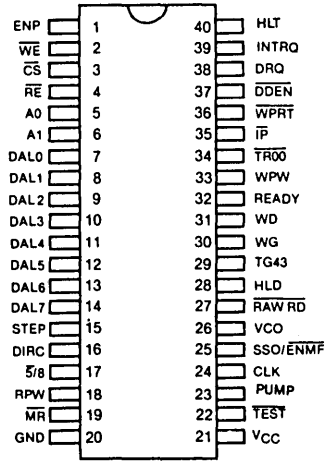
- ON-CHIP PLL DATA SEPARATOR
- ON-CHIP WRITE PRECOMPENSATION LOGIC
- SINGLE +5V SUPPLY
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 (FM)
  - IBM 34 (MFM)
- AUTOMATIC SEEK WITH VERIFY
- MULTILE SECTOR READ/WRITE
- TTL COMPATIBLE
- PROGRAMMABLE CONTROL
  - SELECTABLE TRACK-TO-TRACK ACCESS
  - HEAD LOAD TIMING
- SOFTWARE COMPATIBLE WITH THE FD179X SERIES
- SOFT SECTOR FORMAT COMPATIBILITY

DESCRIPTION

The WD279X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The WD279X, which can be considered the end result of both the FD1771 and FD179X designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The WD279X contains all the features of its predecessor the FD179X plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD179X and WD279X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical.

Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

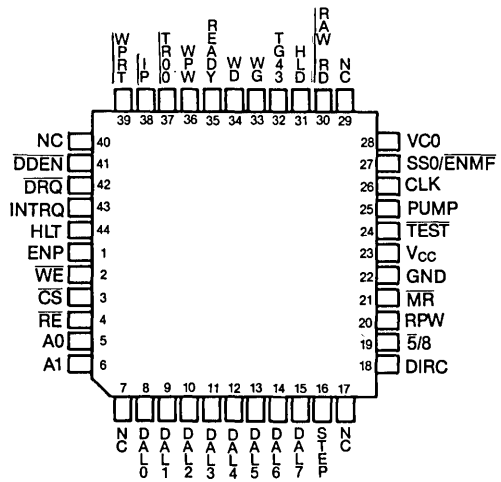
The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The WD279X is set up to operate on a multiplexed bus with other bus-oriented devices.



PIN DESIGNATION

The WD279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The WD2793 is identical to the WD2791 except the DAL lines are TRUE for systems that utilize true data busses.

The WD2795/7 has a side select output for controlling double-sided drives.



PIN DESCRIPTION

PIN NUMBER	SIGNAL NAME	MNEMONIC	FUNCTION
1	ENABLE PRECOMP	ENP	A Logic high on this input enables write precompensation to be performed on double density Write Data output only.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V [25]
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0,A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit bi-directional bus used for transfer of commands, status, and data. These lines are inverted (active low) on WD2791 and WD2795.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ±1% for 8" drives, 1 MHz ±1% for mini-floppies.
38	DATA REQUEST	DRQ	This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR.

PIN DESCRIPTION (Continued)

PIN NUMBER	SIGNAL NAME	MNEMONIC	FUNCTION
39	INTERRUPT REQUEST	INTRQ	This output is set at the completion of any command and is reset when the Status register is read or the command register is written to.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	5 1/4," 8" SELECT	$\overline{5/8}$	This input selects the internal VCO frequency for use with 5 1/4" drives or 8" drives.
18	READ PULSE WIDTH	RPW	An external potentiometer tied to this input controls the phase comparator within the data separator.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins.
23	PUMP	PUMP	High-Impedance output signal which is forced high or low to increase or decrease the VCO frequency.
25	$\overline{\text{ENABLE MINI-FLOPPY}}$ (2791, 2793)	$\overline{\text{ENMF}}$	A logic low on this input enables an internal ÷2 of the Master Clock. This allows both 5 1/4" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a Logic 1.
25	SIDE SELECT OUTPUT (2795, 2797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector ID Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	VOLTAGE-CONTROLLED OSCILLATOR	VCO	An external capacitor tied to this pin adjusts the VCO center frequency.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between track 44 and the inside track. This output is valid only during Read and Write Commands.

PIN DESCRIPTION (Continued)

PIN NUMBER	SIGNAL NAME	MNEMONIC	FUNCTION
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	MFM or FM output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE PRECOMP WIDTH	WPW	An external potentiometer tied to this input controls the amount of delay in Write precompensation mode.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the WD279X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the WD279X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This input pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected.
40	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.

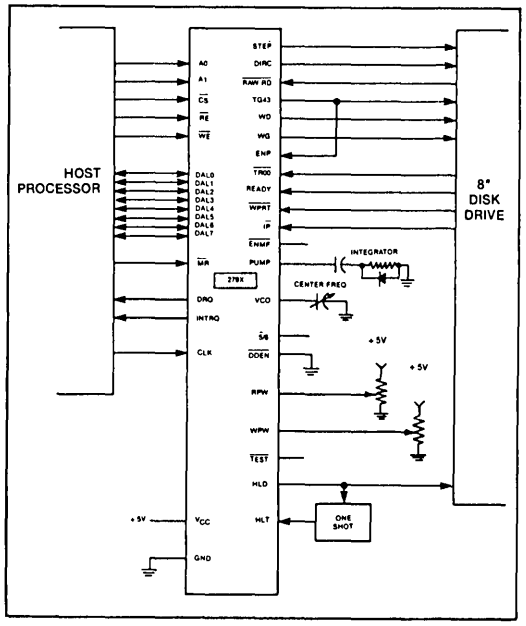


Figure 1.

APPLICATIONS

8" FLOPPY AND 5 1/4" MINI-FLOPPY CONTROLLER SINGLE OR DOUBLE DENSITY CONTROLLER/-FORMATTER

The WD279X Family are MOS/LSI devices which perform the functions of a Floppy Disk Controller/Formatter. Software compatible with its predecessor, the FD179X, the device also contains a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic.

When operating in Double Density mode, Write Precompensation may be enabled, its value predetermined by an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5 1/4" or 8" Floppy Disk interfacing.

The WD279X is fabricated in NMOS silicon gate technology and available in a 40-pin dual-in-line package, as well as 44-pin quad packs.

FEATURES	2791	2793	2795	2797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Side Select Out			X	X
Internal CLK Divide	X	X		

ORGANIZATION

Refer to the Floppy Disk Formatter block diagram in Figure 2. The primary sections include the parallel processor interface and the Floppy Disk Interface.

Data Shift Register – This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register–This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) – This 8-bit register holds the address of the sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)–This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)–This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic–This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)–The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control –All computer and Floppy Disk interface controls are generated through this logic.

The internal device timing is generated from an external crystal clock.

AM Detector - The address mark detector detects ID, data and Index address marks during read and write operations.

Write Precompensation - enables write precompensation to be performed on the Write Data ouput.

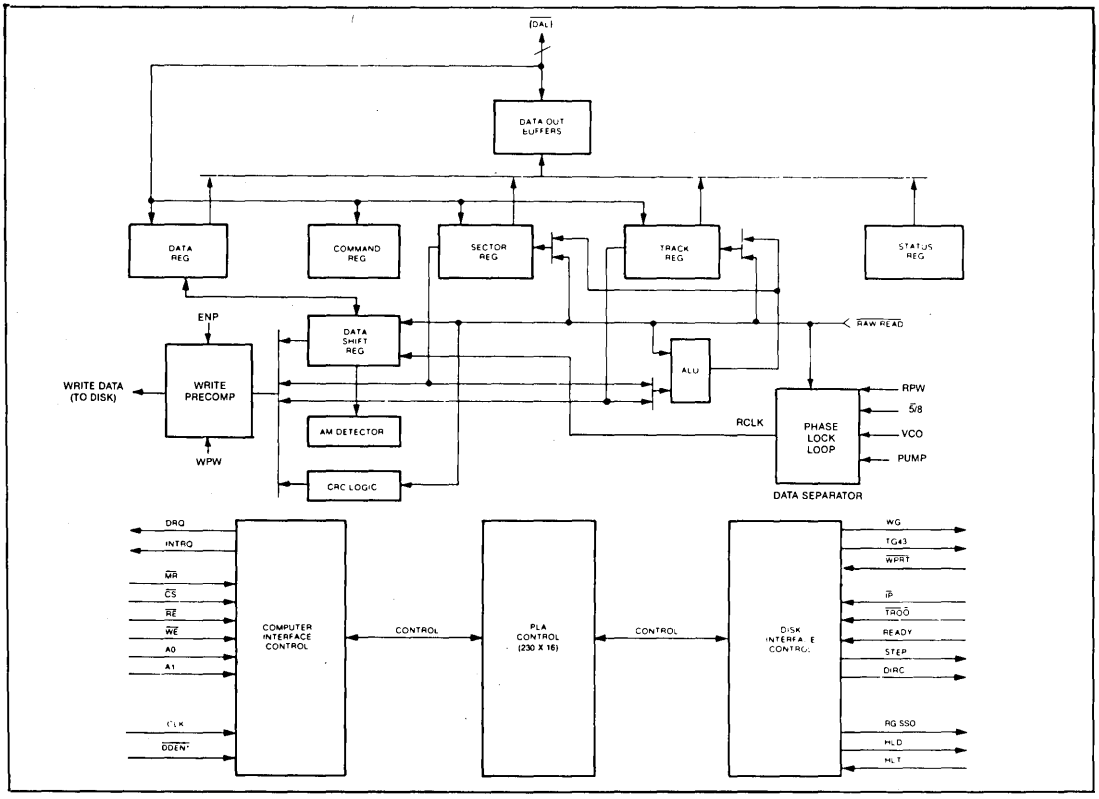


Figure 2. WD279X BLOCK DIAGRAM

Data Separator - a high performance Phase-Lock-Loop Data Separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

PROCESSOR INTERFACE

The Interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD279X. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Regiser	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD279X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The WD279X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 5 1/4" drives.

On the WD2791/WD2793, the $\overline{ENMF}$ input (Pin 25) can be used for controlling both 5 1/4" and 8" drives with a single 2 MHz clock. When $\overline{ENMF}$ = 0, an internal ÷2 of the CLK is performed. When $\overline{ENMF}$ = 1, no divide takes place. This allows the use of a 2 MHz clock for both 5 1/4" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The $\overline{5/8}$ input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When $\overline{5/8}$ = 0, 5 1/4" data separation is selected; when $\overline{5/8}$ = 1, 8" drive data separation is selected.

CLOCK (24)	$\overline{ENMF}$ (25)	$\overline{5/8}$ (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	5¼
1 MHz	1	0	5¼

FUNCTIONAL DESCRIPTION

The WD279X-02 is software compatible with the FD179X-02 series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 179X can be transferred to a 279X system without modification.

In addition to the WD179X, the WD279X contains an internal Data Separator and Write precompensation circuit. The $\overline{TEST}$ (Pin 22) line is used to adjust both data separator and precompensation. When $\overline{TEST}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished.

A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths.

Similarly, Data separation is also adjusted with $\overline{TEST}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (.5 MHz for 8" drives). The VCO Trimming capacitor (Pin 26) is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The $\overline{TEST}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{TEST}$ pin, overriding the pull-up. The $\overline{TEST}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the WD179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: $\overline{ENP}$, $\overline{5/8}$, $\overline{ENMF}$, $\overline{WPRT}$, $\overline{DDEN}$, HLT, TEST, and $\overline{MR}$.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0". Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*2795/97 may vary - see command summary.

The WD279X recognizes tracks and sectors numbered 00-FF Hex. However, due to programming restrictions, only tracks and sectors 00 through F4 can be formatted.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the WD279X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the WD279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater then the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the WD279X samples the Ready input. If this input is logic low, the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: WD2791, WD2793

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_0	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

B. Commands for Models: WD2795, WD2797

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0= Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0,No verify V = 1,Verify on destination track
I	3	h = Head Load Flag	h = 0,Unload head at beginning h = 1,Load head at beginning
I	4	T = Track Update Flag	T = 0,No update T = 1,Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0,FB(DAM) a_0 = 1,F8(deleted DAM)
II	1	C = Side Compare Flag	C = 0,Disable side compare C = 1,Enable side compare
II & III	1	U = Update SSO	U = 0,Update SSO to 0 U = 1,Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0,No. 15 MS delay E = 1,15 MS delay (30 MS for 1 Mhz)
II	3	S = Side Compare Flag	S = 0,Compare for side 0 S = 1,Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field: L = 0: 00 256, 01 512, 10 1024, 11 128; L = 1: 00 128, 01 256, 10 512, 11 1024
II	4	m = Multiple Record Flag	m = 0,Single record m = 1,Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset* I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

NOTE: See Type IV Command Description for further information.

WRITE PRECOMPENSATION

When operating in Double Density mode ($\overline{DDEN} = 0$), the WD279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the TEST line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{TEST} = 0$.

DATA SEPARATION

The WD279X can operate with either an external data separator or its own internal recovery circuits. The condition of the TEST line (Pin 22) in conjunction with MR (Pin 19) will select internal or external mode.

To program the 279X for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST} = 0$. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8" Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. TEST is returned to a Logic 1 for normal operation.

Note: To maintain this mode, $\overline{TEST}$ must be held low whenever MR is applied.

For internal VCO operation, the $\overline{TEST}$ line must be high during the MR pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG 43), adjust the RPW pulse (250 ns for 8" Double Density). An external variable capacitor of C-60 pf is tied to the VCO input (Pin 26). It is highly recommended to use at least a negative 3500 PPM Temperature coefficient trimmer capacitor. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 KHz for 8" Double Density). The DDEN line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

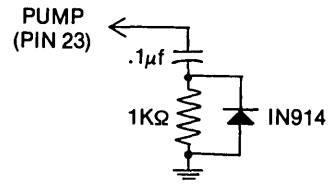
After adjustments have been made, the $\overline{TEST}$ pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCP to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to PUMP runaway. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:



Since 5¼" Drives operate at exactly one-half the data rate (250 Kb/sec) the above capacitor should be doubled to .2 or .22 μf.

NOTE 1: A Diode with the lowest on resistance will enhance PUMP response.

NOTE 2: It is recommended to replace the 1K resistor with a 1K (nominal at 25°c) thermister (approximating 400 ohms at 50°c and approximatley 2.8K ohms at 0°c) to improve capture range.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0 r_1), which determines the stepping motor rate as defined in Table 3.

A 2μs (MFM) or 4μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The direction signal is active high when stepping in and low when stepping out. The direction signal is valid before the first stepping pulse is generated. The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK		2 MHz	1 MHz
R1	R0	$\overline{TEST} = 1$	$\overline{TEST} = 1$
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

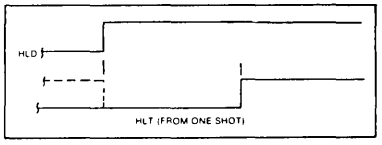
After the last directional step, an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step, or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The WD279X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the WD279X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the WD279X which is used for the head engage time. When HLT = 1, the WD279X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the WD279X.



HEAD LOAD TIMING

When both HLD and HLT are true, the WD279X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the WD279X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the WD279X then waits for HLT to occur.

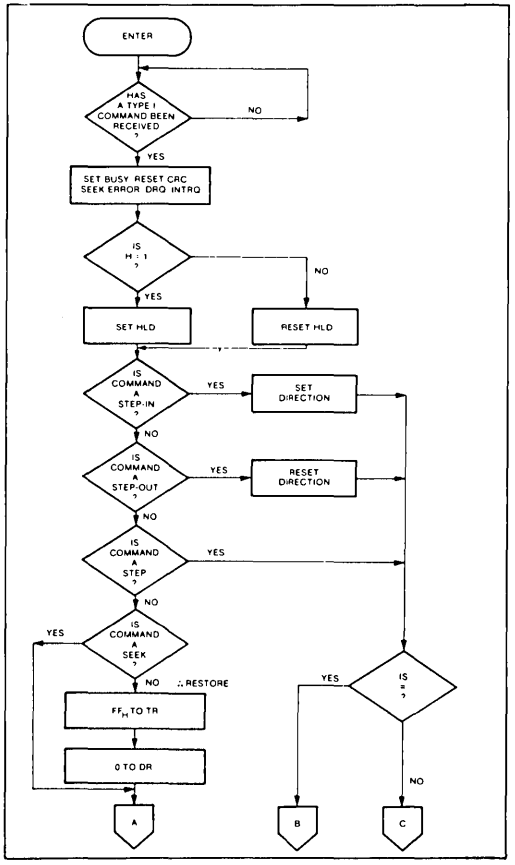
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

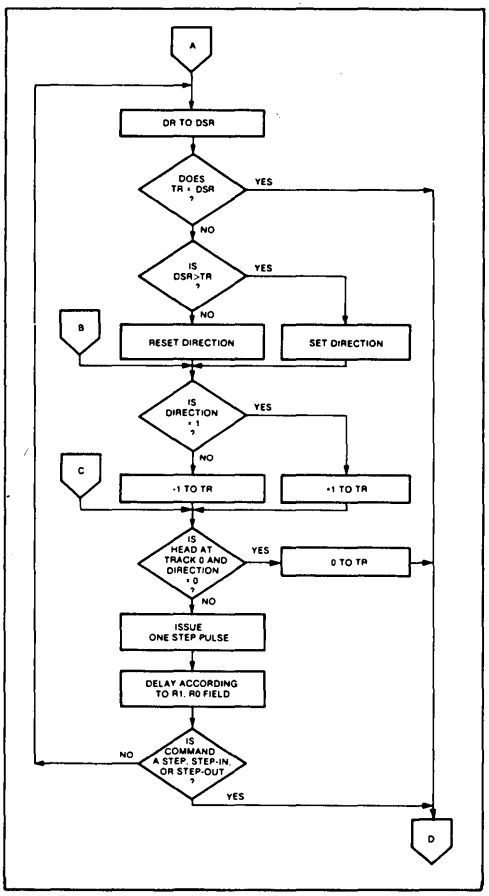
Upon receipt of this command the Track 00($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read- Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r1r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the WD279X terminates operation, interrupts, and sets the Seek error status bit. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.

SEEK

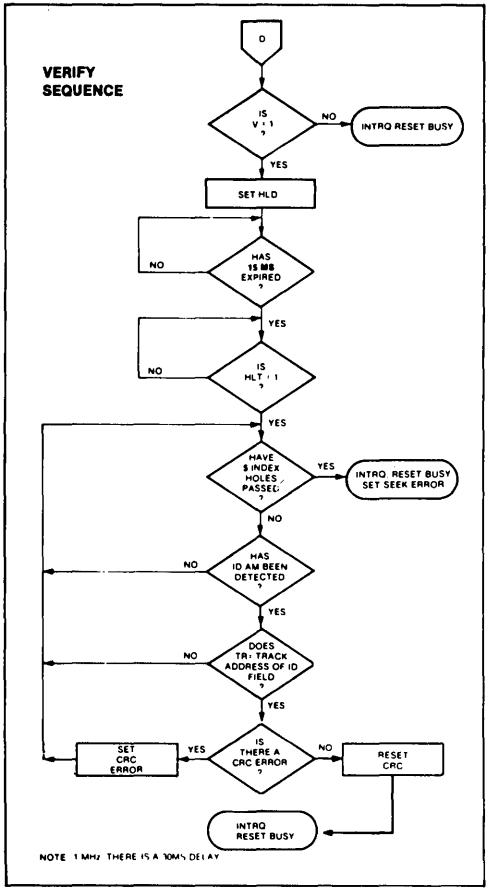
This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the WD279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command.

An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD279X issues one stepping pulse in the direction away from track zero. If the T flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the WD279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a

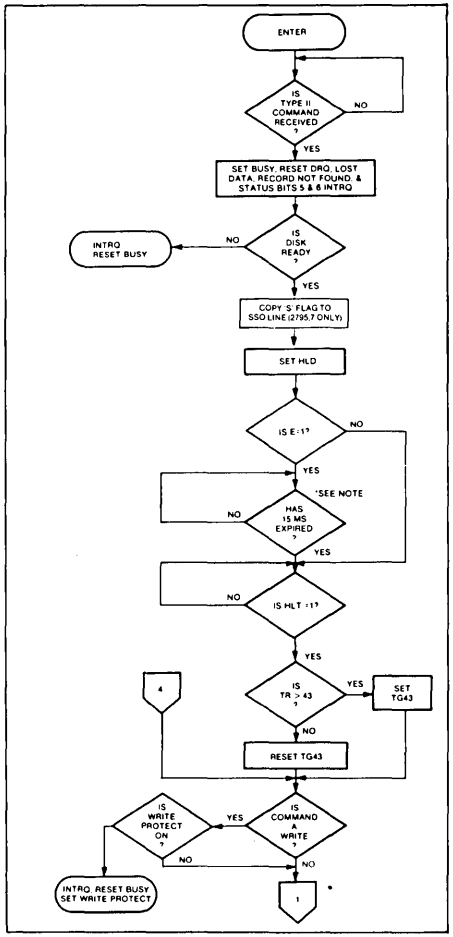
verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

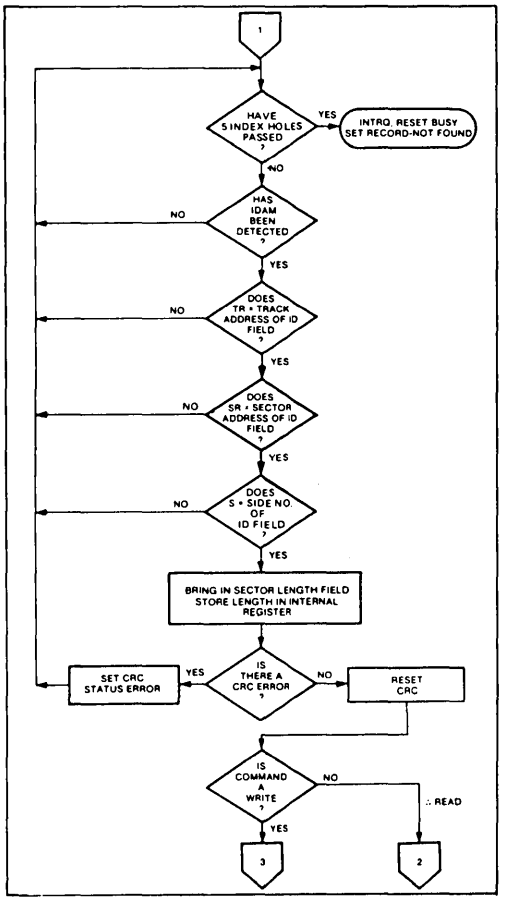
On the WD2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loadng the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.



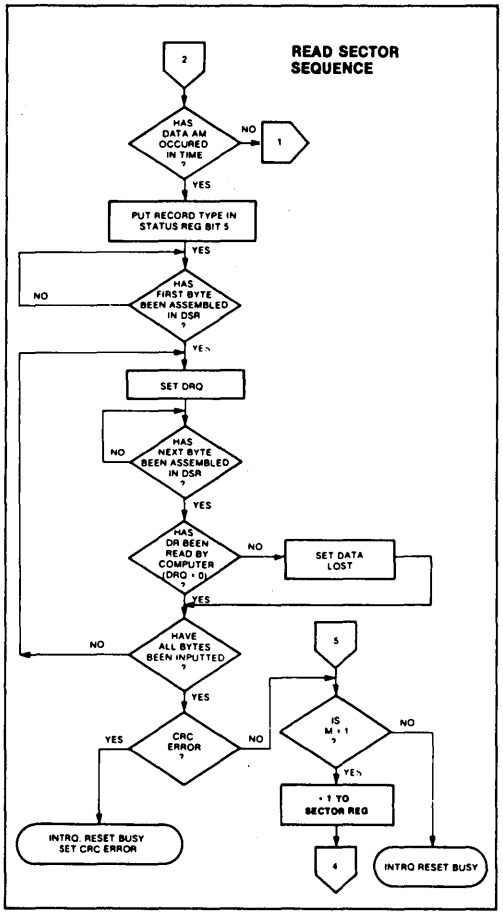
TYPE II COMMAND

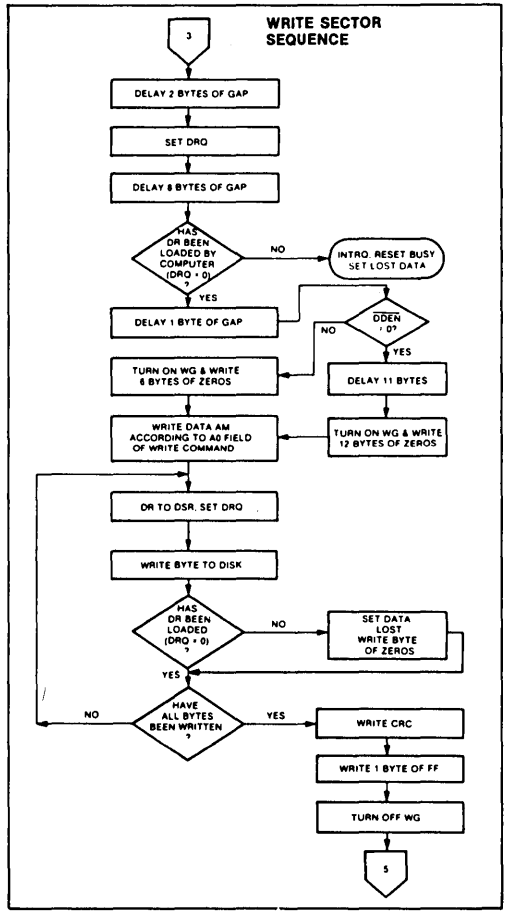


TYPE II COMMAND

When an ID field is located on the disk, the WD279X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is ready and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The WD279X must find an ID field with a Track number, Sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record Not Found status bit is set (Status bit 4) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command.





TYPE II COMMAND

If m = 1, multiple records are read or written with sector register internally updated so that an address verification can occur on the next record. The WD279X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the WD279X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The WD279X will search for 5 disk revolutions, interrupt out, reset busy, and set the Record Not Found status bit.

The Type II commands for WD2791-93 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field,

TYPE II COMMAND

the WD279X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III for the WD2795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The WD2795/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID field, allows different byte lengths to be implemented in each sector. For IBM compatibility. the 'L' flag should be set to one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID

field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field search is repeated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status Bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The WD279X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the $^{a}0$ field of the command as shown below:

$^{a}0$	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The WD279X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

TYPE III COMMANDS
READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDR	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the WD279X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is

included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag will be set.

The ID A.M., ID field, ID CRC bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

Because these synchronization problems almost always occur in the Data Area, this command will not function as a Track Copy and should be used only as a Diagnostic Program to test the ability to read addresses.

WRITE TRACK FORMATTING THE DISK

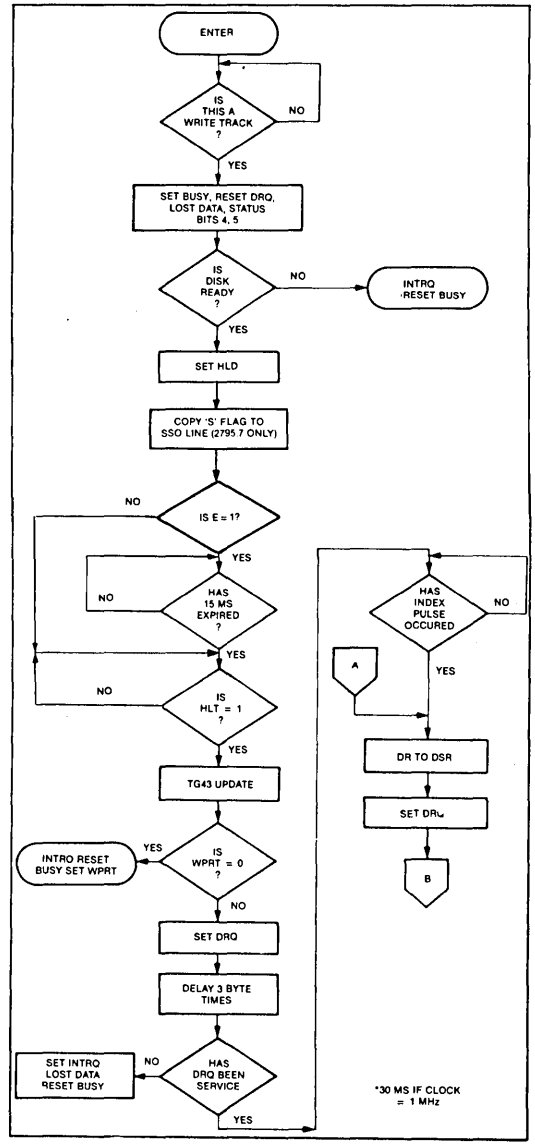
(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

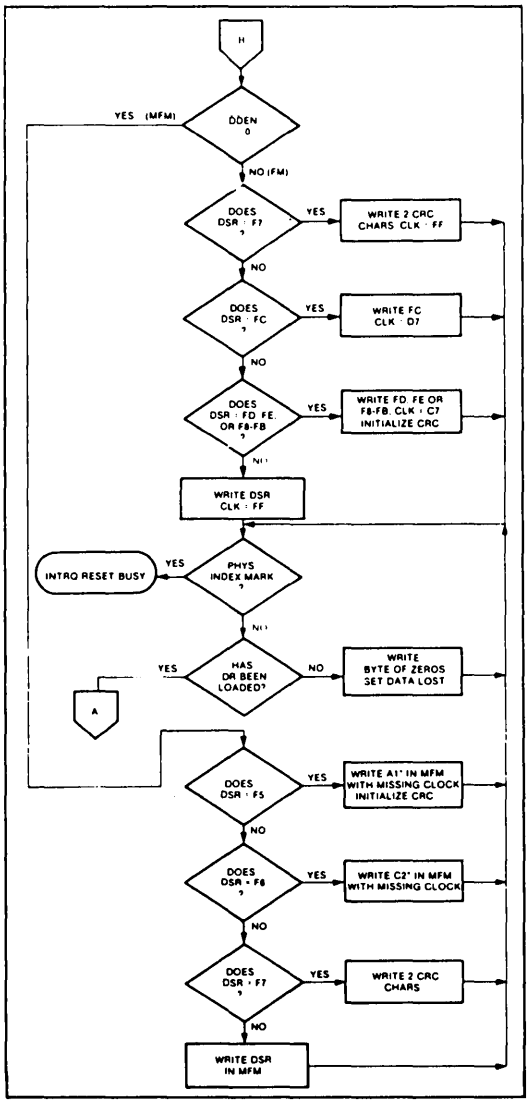
Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by (within three byte times) the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, an the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the WD279X detects a data pattern of F5 through FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector Read or Write Command or to insure Type I status in the Status Register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Read Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3-I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3-I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	WD279X INTERPRETATION IN FM (DDEN = 1)	WD279X INTERPRETATION IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

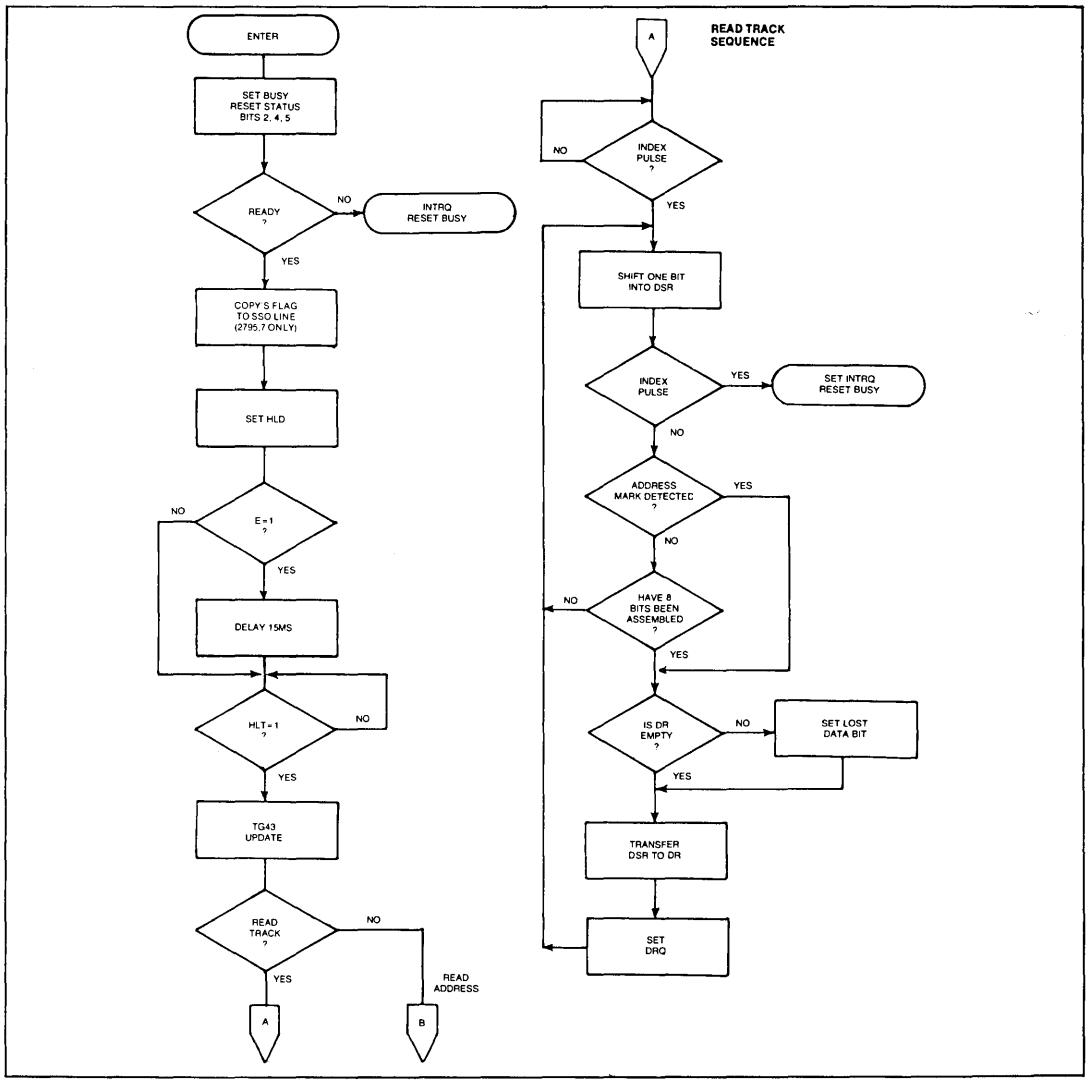
*Missing clock transition between bits 4 and 5. **Missing clock transition between bits 3 and 4.

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Impulse will cause an interrupt condition.

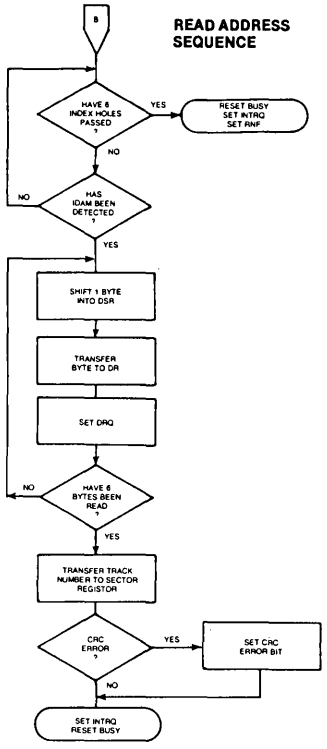
STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt Command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the Status Register through program control or using the DRQ line with DMA or interrupt methods. When the Data Register



TYPE III COMMAND
Read Track/Address



TYPE III COMMAND
Read Track/Address

is read the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

BITS							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12μs	6μs
Write to Command Reg.	Read Status Bits 1-7	28μs	14μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT - 128 BYTES/SECTOR

Shown below is the IBM single density-format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track Command, and load the Data Register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)[3]
6	00
1	FC (Index Mark)
[1]26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247[2]	FF (or 00)

1. Write bracketed field 26 times.
2. Continue writing until 279X interrupts out. Approx. 247 bytes.
3. A '00' option is allowed.

IBM SYSTEM 34 FORMAT
256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track Command and load the Data Register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
*50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRC's written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRC's written)
54	4E
598**	4E

*Write bracketed field 26 times.
**Continue writing until 279X interrupts out. Approx. 598 bytes.

1. NON-IBM FORMATS

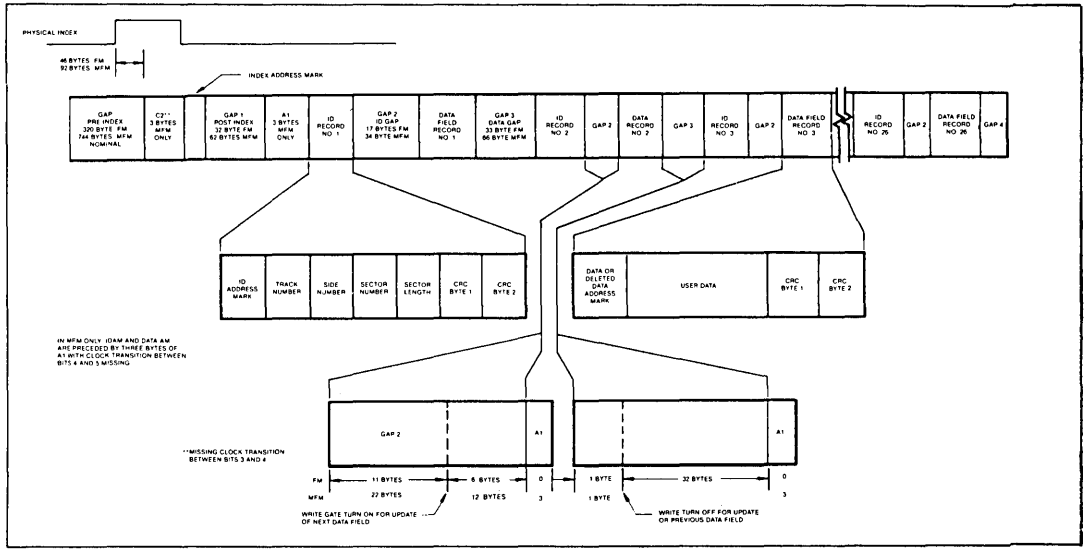
Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1. Sector size must be 128, 256, 512, of 1024 bytes.
2. Gap 2 cannot be vaired from the IBM format.
3. 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the WD279X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for WD279X operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



IBM TRACK FORMAT

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage to any input with respect to V_{SS} = +7 to -0.5V

Operating Temperature: +15°C to +50°C (NPO Capacitor, Pin 26)
+5°C to +60°C (minimum, Neg. 3500 TC capacitor, Pin 26)
0°C to +70°C (minimum, Neg. 3500 TC capacitor, Pin 26 and a thermistor in pump circuit)

Storage temperature = -55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating characteristics.

OPERATING CHARACTERISTICS (DC)

T_A = See Electrical Characteristics

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage			10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	I_O = -100μA
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6mA
V_{OHP}	Output High PUMP	2.2			V	I_{OP} = -1.0 mA
V_{OLP}	Output Low PUMP			0.2	V	I_{OP} = +1.0 mA
P_D	Power Dissipation			.75	W	All Outputs Open
R_{PU}	Internal Pull-Up*	100		1700	μA	V_{IN} = 0V
I_{CC}	Supply Current		70	150	mA	All Outputs Open

*Internal Pull-up resistors on PINS 1, 17, 19, 22, 36, 37 and 40. Also pin 25 on WD2791 and 3.

TIMING CHARACTERISTICS

T_A See Electrical Characteristics V_{SS} = OV, V_{CC} = +5 ±.25V

READ ENABLE TIMING (See Note 2.)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{RE}$	50			nsec	See Note 3
T_{HLD}	Hold ADDR & CS from $\overline{RE}$	10			nsec	
T_{RE}	$\overline{RE}$ Pulse Width	200			nsec	C_L = 50 pf
T_{DRR}	DRQ Reset from $\overline{RE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Fig. 3
T_{DACC}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
T_{DOH}	Data Hold From $\overline{RE}$	20		150	nsec	C_L = 50 pf

WRITE ENABLE TIMING (See Note 2)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDRS & CS TO $\overline{WE}$	50			nsec	See Note 3
T_{HLD}	Hold ADDR & CS from $\overline{WE}$	10			nsec	
T_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
T_{DRR}	DRQ Reset from $\overline{WE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Fig. 4
T_{DS}	Data Setup to $\overline{WE}$	150			nsec	
T_{DH}	Data Hold from $\overline{WE}$	50			nsec	

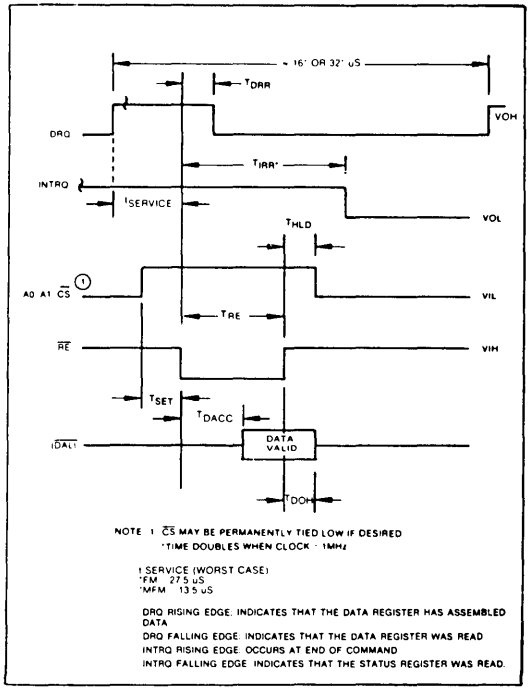


FIGURE 3. READ ENABLE TIMING

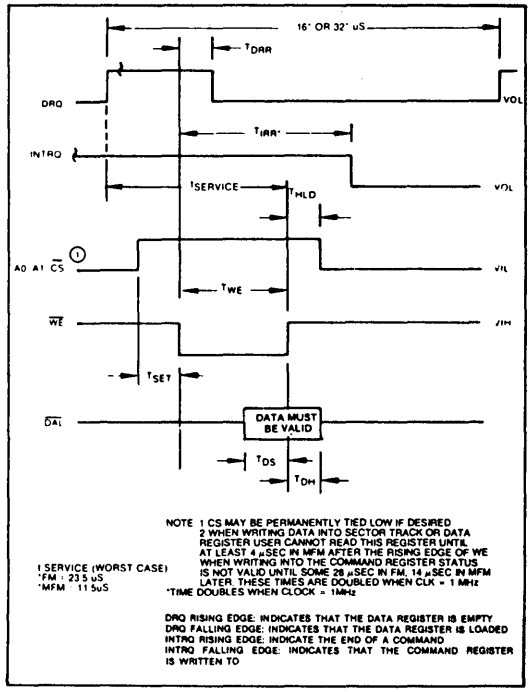


FIGURE 4. WRITE ENABLE TIMING

INPUT DATA TIMING

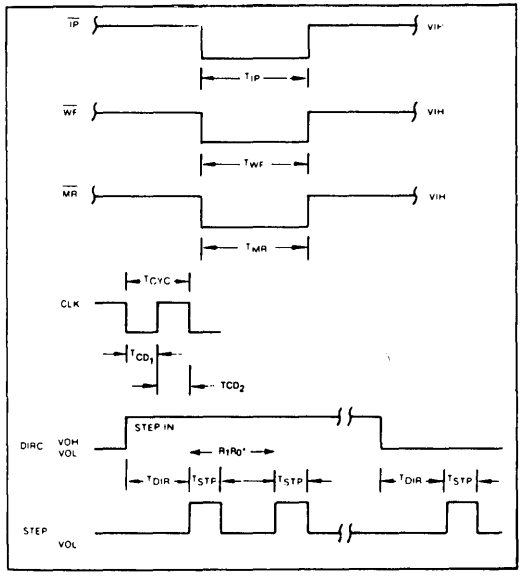
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{PW}	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	
T_{BC}	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)(NO WRITE PRECOMPENSATION)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{WP}	Write Data Pulse Width	400	500	600	nsec	FM
		200	250	300	nsec	MFM
T_{WG}	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
T_{WF}	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{CD1}	Clock Duty (low)	230	250	20000	nsec	
T_{CD2}	Clock Duty (high)	230	250	20000	nsec	
T_{STP}	Step Pulse Output	2 or 4			μsec	See Notes 1 & 2
T_{DIR}	Dir Setup to Step		12		μsec	± CLK ERROR
T_{MR}	Master Reset Pulse Width	50			μsec	
T_{IP}	Index Pulse Width	10			μsec	See Notes 1 & 2
RPW	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
	Precomp. Adjust	100		300	nsec	MFM
WPW	Write Data Pulse Width					Precomp = 100 nsec
		200	300	400	nsec	MFM
WPW	Write Data Pulse Width					Precomp = 300 nsec
		600	900	1200	nsec	MFM
VCO	Free Run Voltage Controlled	6.0			MHz	Cext = 0
	Oscillator. Adjustable by		4.0		MHz	Cext = 35 pf
	ext. capacitor on Pin 26					
	Pump Up +25%	5.0			MHz	PU = 2.2V
						Cext = 35 pf
VCO	Pump Down -25%			3.0	MHz	$\overline{PD}$ = 0.2V
						Cext = 35 pf
	5% Change V_{CC}	3.8		4.2	MHz	Cext = 35 pf
VCO	T_A = 75°C	3.5			MHz	Cext = 35 pf
Cext	Adjustable external capacitor	6	25	60	pf	VCO = 4.0 MHz
						nom
RCLK	Derived read clock					VCO = 4.0 MHz
	= VCO + 8, 16, 32					
			500		KHz	$\overline{DDEN}$ = 0
						$\overline{5/8}$ = 1
			250		KHz	$\overline{DDEN}$ = 0
						$\overline{5/8}$ = 0
			250		KHz	$\overline{DDEN}$ = 1
						$\overline{5/8}$ = 1
			125		KHz	$\overline{DDEN}$ = 1
						$\overline{5/8}$ = 0
PU/DON	PU/$\overline{PD}$ time on			250	ns	MFM
	(pulse width)			500	ns	FM

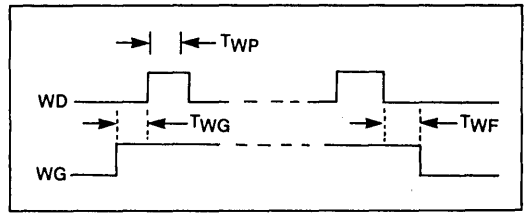


MISCELLANEOUS TIMING

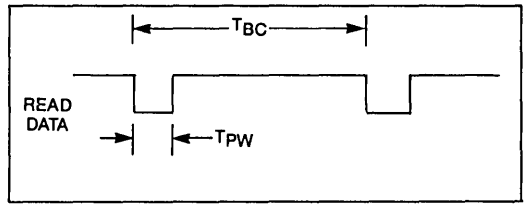
*FROM STEP RATE TABLE

NOTES:

1. Times double when clock = 1 MHz.
2. Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.
3. T_{SET} may be reduced to 0 nsec if T_{RE} and T_{WE} are increased the same amount.



WRITE DATA TIMING



READ DATA TIMING

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically "ORed" with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and "ORed" with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

SUMMARY OF ADJUSTMENT PROCEDURE

WRITE PRECOMPENSATION

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe MR (Pin 19).
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe pulse width on WD (Pin 31).
5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
6) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

DATA SEPARATOR

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe MR (Pin 19). Insure that 5 /8, and $\overline{\text{DDEN}}$ are set properly.
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe Pulse Width on TG43 (Pin 29).
5) Adjust RPW (Pin 18) for (205ns for 8" DD 450ns for 5 1/4" DD, etc.).
6) Observe Frequency on DIRC (Pin 16).
7) Adjust variable capacitor on VCO pin for Data Rate (500 KHz for 8" DD, 250 KHz for 5 1/4" DD, etc.).
8) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}}$ = 1 whenever a master reset pulse is applied.

WD279X-02 Floppy Disk Formatter/Controller Family Application Notes

INTRODUCTION

In an effort to simplify Floppy Diskette interfacing, Western Digital has been constantly improving the LSI Controller/Formatter, the most recent of which is the WD279X Family of LSI controller devices, incorporating advanced technology to include controller, Write Compensation and Analog Phase Lock Loop in a single 40-pin dual-in-line package. With this package we can now offer the designer the simplest ever interfacing option.

The family consists of four members: WD2791, WD2793, WD2795 and WD2797. WD2791 and WD2793 offer internal clock divide in true and inverted data bus. The WD2795 and WD2797 offer internal side select. The family supports both 5 1/4" and 8" Diskette Drives and both single and double density.

HOST INTERFACING

The LSI Diskette Controller has been developed to ease the interfacing of Processor to Disk Device. The Host interfacing with WD279X Family is accomplished with minimum external devices via an 8-bit bi-directional bus, read/write controls, register select lines and optional control line for chip select, 5 1/4" or 8" select, enable mini floppy, double density enable. The basic operation at the controller is accomplished by selecting the device via (CS) chip select line, enabling selection of one of the five internal registers (Figure 1).

A1	A0	READ (RE)	WRITE (WE)
0	0	Status Regiser	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

FIGURE 1.

Each time a command is issued to the WD279X, the busy bit is set and INTRQ (Interrupt Request) line is reset. The user has the option of testing for the busy bit or polling INTRQ to determine if command has been completed.

The busy bit will be reset whenever the WD279X is idle and awaiting a new command. The INTRQ line once set, can only be reset by reading of the status register or issuing a new command.

The A_0, A_1 Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6250, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the WD279X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY FM	REQ'D. MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12μs	6μs
Write to Command Reg.	Read Status Bits 1-7	28μs	14μs
Write Any Register	Read From Diff. Register	0	0

Other CPU interface lines are CLK, $\overline{MR}$ and $\overline{DDEN}$. The CLK line should be 2 MHz (8" drive) or 1 MHz (5 1/4" drive) with 50% duty cycle. Accuracy should be +1% (crystal source) since all internal timing, including stepping rates, are based upon this clock, or a single 2 MHz CLK on WD2791 and WD2793 since $\overline{ENMF}$ line will internally divide CLK.

The Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a $\overline{MR}$, in which case the remaining steps will occur at the faster programmed rate. The WD179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{TR00}$ line to go active low. This line should be connected to the drive's $\overline{TR00}$ sensor.

The $\overline{DDEN}$ line causes selection of either single density ($\overline{DDEN}$ = 1) or double density operation. $\overline{DDEN}$ should not be switched during a read or write operation.

The 5/8 Line selects internal VCO frequency to be used with 5 1/4" or 8" drives.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection

to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs rom the WD279X. Inputs to the WD279X may be buffered or tied to the Drives' outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed -0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\overline{IP}$ or Index Pulse. This Line is tied to the drives' Index L.E.D. sensor that informs the WD279X that the stepper motor is at is furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open," Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The WD279X will look at the ready signal prior to executing READ/WRITE commands. READY is not inspected during any Type 1 commands. All Type 1 commands will execute regardless of the Logic Level on this Line.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the WD279X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the $\overline{\text{Write Protect}}$ status bit is set.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If TR00 is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1 r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the WD279X terminates operations, interrupts, and sets the Seek error status bit. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the WD279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD279X issues one stepping pulse in the direction away from track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r_1 r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the WD2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

For write operations, the WD279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the WD279X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, and interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1 and Table 2.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 2791, 2793

	Bits								
Type Command	7	6	5	4	3	2	1	0
I Restore	0	0	0	0	h	V	r_1	r_0
I Seek	0	0	0	1	h	V	r_1	r_0
I Step	0	0	1	T	h	V	r_1	r_0
I Step-in	0	1	0	T	h	V	r_1	r_0
I Step-out	0	1	1	T	h	V	r_1	r_0
II Read Sector	1	0	0	m	S	E	C	0
II Write Sector	1	0	1	m	S	E	C	a_0
III Read Address	1	1	0	0	0	E	0	0
III Read Track	1	1	1	0	0	E	0	0
III Write Track	1	1	1	1	0	E	0	0
IV Force Interrupt	1	1	0	I_1	I_3	I_2	I_1	I_0

B. Commands for Models: 2795, 2797

	Bits							
Type Command	7	6	5	4	3	2	1	0
I Restore	0	0	0	0	h	V	r_1	r_0
I Seek	0	0	0	1	h	V	r_1	r_0
I Step	0	0	1	T	h	V	r_1	r_0
I Step-in	0	1	0	T	h	V	r_1	r_0
I Step-out	0	1	1	T	h	V	r_1	r_0
II Read Sector	1	0	0	m	L	E	U	0
II Write Sector	1	0	1	m	L	E	U	a_0
III Read Address	1	1	0	0	0	E	U	0
III Read Track	1	1	1	0	0	E	U	0
III Write Track	1	1	1	1	0	E	U	0
IV Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0,No verify V = 1,Verify on destination track
I	3	h = Head Load Flag	h = 0,Load head at beginning h = 2,Unload head at beginning
I	4	T = Track Update Flag	T = 0,No update T = 1,Update track register
II	0	a_0 = Data Address Mark	a_0 = 0,FB(DAM) a_0 = 1,F8(deleted DAM)
II & III	1	C = Side Compare Flag	C = 0,Disable side compare C = 1,Enable side compare
II & III	1	U = Update SSO	U = 0,Update SSO to 0 U = 1,Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0,No 15 MS delay E = 1,15 MS delay (30 MS for 1 MHz)
II	3	S = Side Compare Flag	S = 0,Compare for side 0 S = 1,Compare for side 1
II	3	L = Sector Length Flag	

LSB's Sector Length in ID Field	00	01	10	11
L = 0	256	512	1024	128
L = 1	128	256	512	1024

II	4	m = Multiple Record Flag	m = 0,Single record m = 1,Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset* I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

WD1691 Floppy Support Logic (F.S.L)

FEATURES

- DIRECT INTERFACE TO THE FD179X
- ELIMINATES EXTERNAL FDC LOGIC
- DATA SEPARATION / RCLK GENERATION
- WRITE PRECOMPENSATION SIGNALS
- VFOE / WF DEMULTIPLEXING
- PROGRAMMABLE DENSITY
- 8" OR 5.25" DRIVE COMPATIBLE
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE
- SINGLE + 5V SUPPLY

GENERAL DESCRIPTION

The WD1691 F.S.L. has been designed to minimize the external logic required to interface the 179X Family of Floppy Disk Controllers to a drive. With the use of an external VCO, the WD1691 will generate the RCLK signal for the WD179X, while providing an adjustment pulse (PUMP) to control the VCO frequency. $\overline{VFOE/WF}$ de-multiplexing is also accomplished and Write Precompensation signals have been included to interface directly with the WD2143 Clock Generator.

The WD1691 is implemented in N-MOS silicon gate technology and is available in a plastic or ceramic 20 pin dual-in-line package.

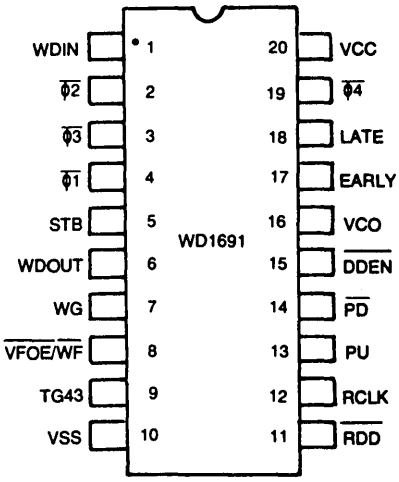


Figure 1. WD1691 PIN DESIGNATION

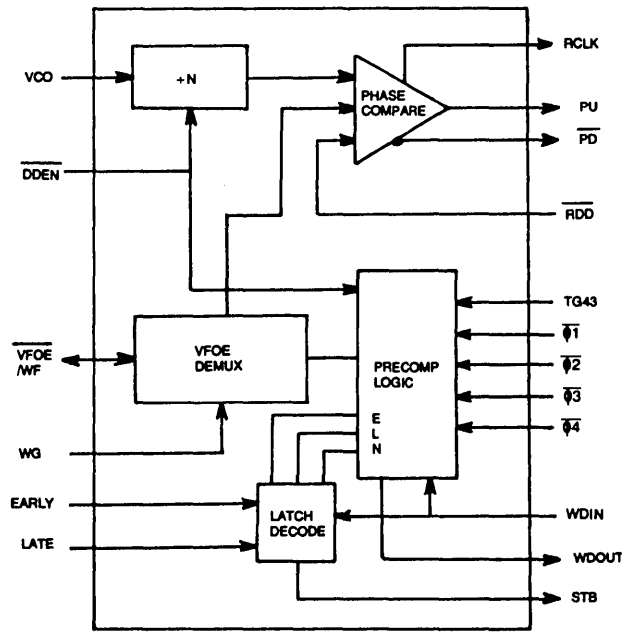


Figure 2. WD1691 BLOCK DIAGRAM

PIN	NAME	SYMBOL	FUNCTION
1	WRITE DATA INPUT	WDIN	Ties directly to the FD179X WD pin.
2, 3, 4, 19	PHASE 2, 3, 1, 4	$\overline{\phi 2}$ $\overline{\phi 3}$ $\overline{\phi 1}$ $\overline{\phi 4}$	4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.
5	STROBE	STB	Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04.
6	WRITE DATA OUTPUT	WDOUT	Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.
7	WRITE GATE	WG	Ties directly to the FD179X pin.
8	VFO ENABLE / WRITE FAULT	$\overline{\text{VFOE}}$ / $\overline{\text{WF}}$	Ties directly to the FD179X $\overline{\text{VFOE}}$ / $\overline{\text{WF}}$ pin.
9	TRACK 32	TG43	Ties directly to the FD179X TG43 pin, If Write Precompensation is required on TRACKS 44-76.
10	V_{SS}	V_{SS}	Ground
11	READ DATA	$\overline{\text{RDD}}$	Composite clock and data stream input from the drive.
12	READ CLOCK	RCLK	RCLK signal generated by the WD1691, to be tied to the FD179X RCLK pin.
13	PUMP UP	PU	Tri-state output that will be forced high when the WD1691 requires an increase in VCO frequency.
14	PUMP DOWN	$\overline{\text{PD}}$	Tri-state output that will be forced low when the WD1691 required a decrease in VCO frequency.
15	Double Density Enable	$\overline{\text{DDEN}}$	Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two.
16	Voltage Controlled Oscillator	VCO	A nominal 4.0 MHz (8" drive) or 2.0 MHz (5.25" drive) master clock input.
17, 18	EARLY LATE	EARLY LATE	EARLY and LATE signals from the FD179X, used to determine Write Precompensation.
20	V_{CC}	V_{CC}	+ 5V ± 10% power supply

Table 1. PIN DEFINITIONS

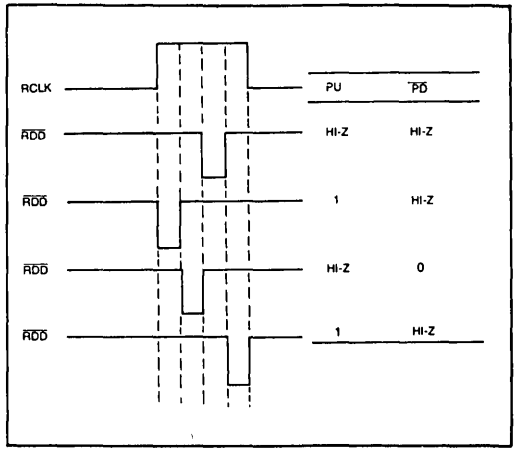


Figure 3 PUMP SIGNAL TIMING DIAGRAM

DEVICE DESCRIPTION

The WD1691 is divided into two sections:

1. Data Recovery Circuit
2. Write Precompensation Circuit

The Data Separator or Recovery Circuit has four inputs: DDEN, VCO, RDD, and VFOE/WF; and three outputs: PU, PD, and RCLK. The VFOE/WF input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

The Write Precompensation circuit has been designed to be used with the WD2143-03 clock generator. When the WD1691 is operated in a "single density only" mode, write precompensation as well as the WD2143-03 is not needed. In this case, 01,02,03,04, and STB should be tied together, DDEN left open, and TG43, WDIN, Early, and Late tied to ground.

In the double-density mode (DDEN = 0), the signals Early and Late are used to select a phase input (01 - 04) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143-03 to start its pulse generation. 02 is used as the write data pulse on nominal (Early = Late = 0) 01 is used for early, and 03 is used for late. The leading edge of 04 resets the STB line in anticipation of the next write data pulse. When TG43 = 0 or DDEN = 1, Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic 1) while DDEN = 0.

The signals, DDEN, TG43, and RDD have internal pull-up resistors and may be left open if a logic 1 is desired on any of these lines.

WG	VFOE/WF	RDD	PU+PD
1	X	X	HI-Z
0	1	X	HI-Z
0	0	1	HI-Z
0	0	0	Enable

Figure 4 DATA RECOVERY LOGIC

When VFOE/WF and WRITE GATE are low, the data recovery circuit is enabled. When the RDD line goes Active Low, the PU or PD signals will become active. See Figure 4. If the RDD line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic 1, requesting an *increase* in VCO frequency. If the RDD line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while PD will go to a logic zero, requesting a *decrease* in VCO frequency. When the leading edge of RDD occurs in the center of the RCLK window, both PU and PD will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. See Figure 3. The RCLK signal is a divide-by-16 (DDEN = 1) or a divide-by-8 (DDEN = 0) of the VCO frequency.

The minimum Voh level on PU is specified at 2.4V, sourcing 200ua. During PUMP UP time, this output will go from a tri-state to .4V minimum. By typing PU and PD together, a PUMP signal is created that will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider can be used to set the tri-state level to approximately 1.4V. This yields a worst case swing of + 1V; acceptable for most VCO chips with a linear voltage-to-frequency characteristic.

Both PU and PD signals are affected by the width of the RAW READ (RDD) pulse. The wider the RAW READ pulse, the longer the PU or PD signal (depending upon the phase relationship to RCLK) will remain active. If the RAW READ pulse exceeds 250ns, (VCO = 4 MHz, DDEN = 0), or 500 ns. (VCO = 2 MHz, DDEN = 1), then both a PU and PD will occur in the same window. This is undesirable and reduces the accuracy of the external integrator or low-pass filter to convert the PUMP signals into a slow moving D.C. correction voltage.

Eventually, the PUMP signals will have corrected the VCO input to exactly the same frequency multiple as the RAW READ signal. The leading edge of the RAW READ pulse will then occur in the exact center of the RCLK window, an ideal condition for the FD179X internal recovery circuits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias .....–25°C (-13°F) to 70°C (158°F)
Voltage on any pin with respect
to Ground (V_{SS}) .....-0.2 to +7V
Power Dissipation.....1W

Storage Temperature
Ceramic–65°C (-85°F) to +150°C (302°F)
Plastic–55°C (-67°F) to +125°C (257°F)

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

^{T}A = 0°C (32°F) to 70°C (158°F); V_{CC} = 5.0V + 10%;V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IL}	Input Low Voltage	-0.2		+0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.45	V	^{I}0L = 3.2 MA
V_{OH}	High Level Output Voltage	2.4			V	^{I}OH = -200μ a
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		40	100	MA	All outputs open

NOTE: For AC and functional testing purposes, a Logic '0' is measured at 0.8V, and a Logic '1' at 2.0V.

AC ELECTRICAL CHARACTERISTICS

^{T}A = 0°C (32°F) to 70°C (158°F);V_{CC} = 5V + 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
FIN	VCO Input Frequency	.5	4	6	MHz	$\overline{\text{DDEN}}$ = 0
		.5	2	6	MHz	DDEN = 1
R_{pw}	$\overline{\text{RDD}}$ Pulse Width	100	200		ns.	
W_{el}	EARLY (LATE) to WDIN	100			ns.	
P_{on}	PUMP UP/DN Time	0		250	ns.	
W_{pi}	WDIN to WDOUT			80	ns.	$\overline{\text{DDEN}}$ = 1
I_{nr}	Internal Pull-up Resistor	4.0	6.5	10 K		

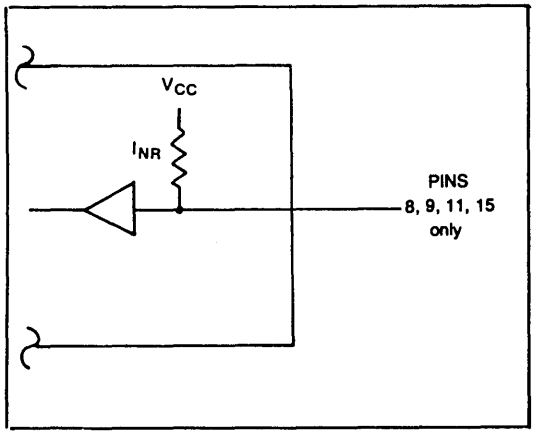


Figure 5. INTERNAL PULL-UP RESISTOR

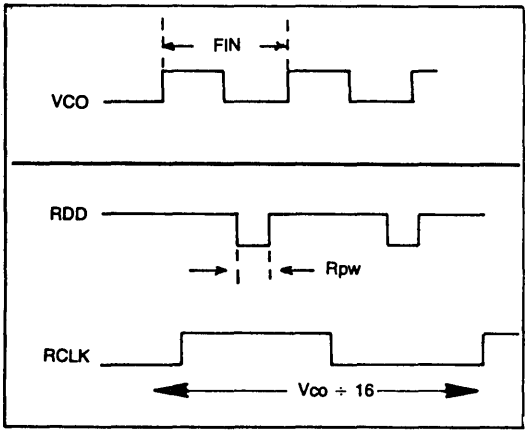


Figure 6. RDD AND RCLK PULSE DIAGRAMS

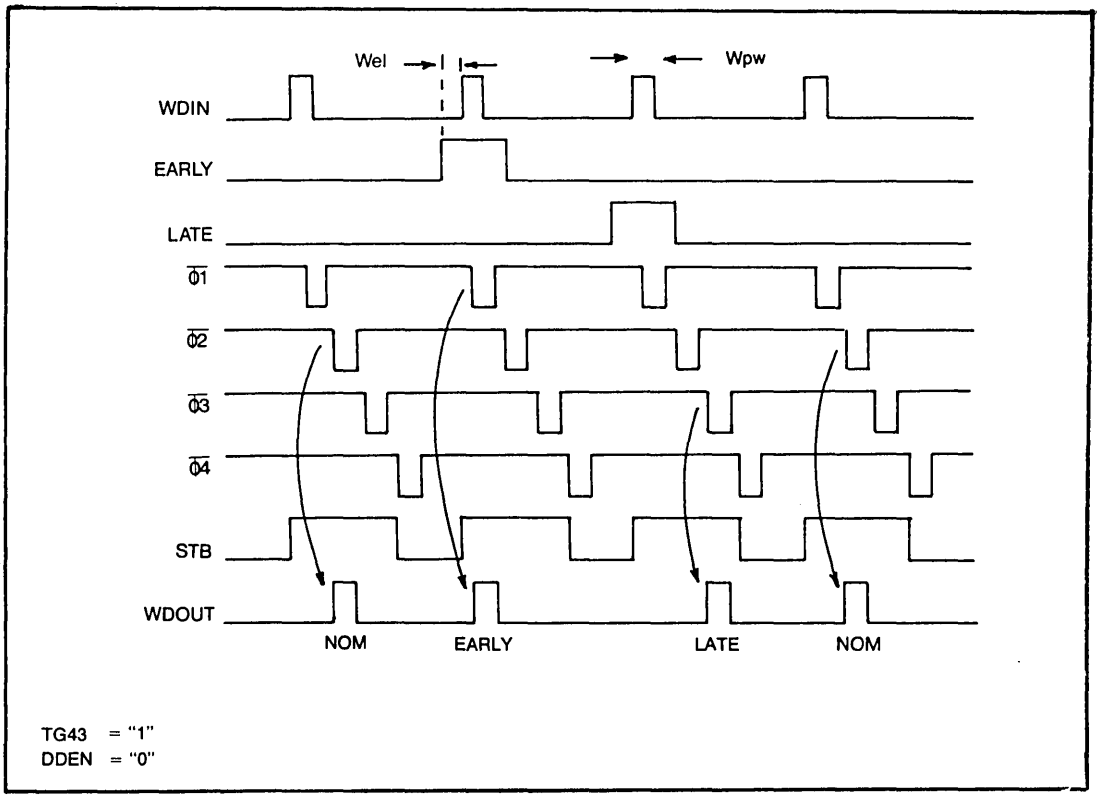


Figure 7. WRITE DATA TIMING (MFM)

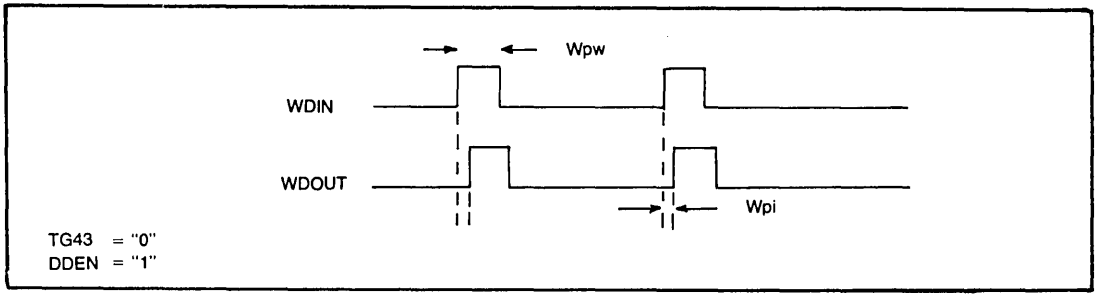


Figure 8. WRITE DATA TIMING (FM)

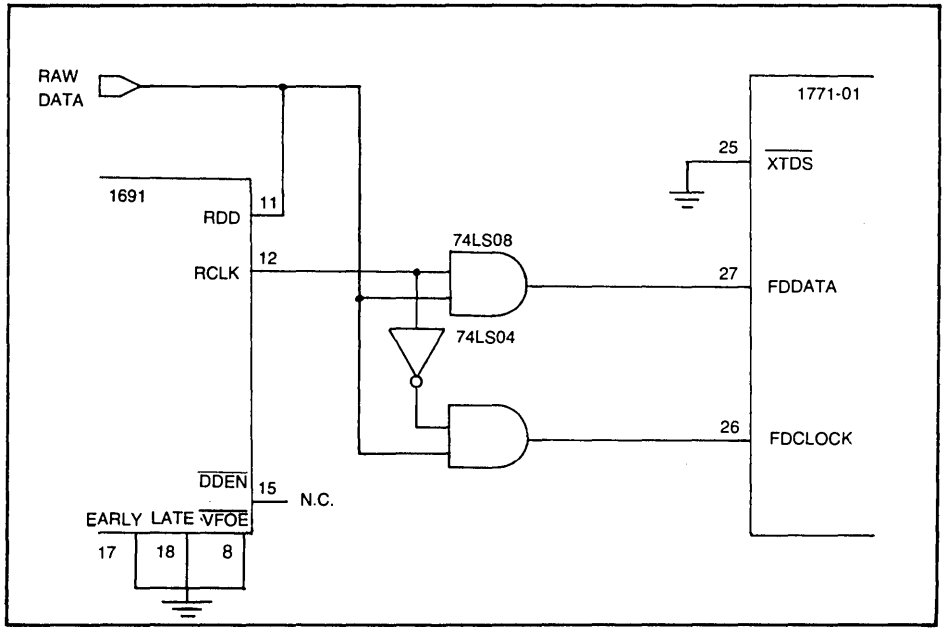


Figure 9. WD1691 to FD1771-01 INTERFACE

TYPICAL APPLICATIONS

Figure 9 illustrates the WD1691 to FD1771-01 floppy disk controller. The RCLK signal is used to gate the RAW data pulses which are inverted by the 74LS04 inverter. Since RLCK will be high during data and low during clock a 74LS08 is used to switch the proper clock or data pulse to the FD1771.

Shown in Figure 10 is a Phase-Lock Loop data separator and the support logic for a single and double-density 8" drive. The raw data (both clock and data bits) are fed to the WD1691 and FD179X. The WD1691 outputs its PU or $\overline{PD}$ signal, which is integrated by the .33uf capacitor and 33ohm resistor to form a control voltage for the 74S124 VCO device. The 4.0 MHz nominal output of the VCO then feeds back to the WD1691 completing the loop. The WD2143-03 is also used, providing write precompensation when in double-density, from tracks 44-77. The $\overline{DDEN}$ line can either be controlled by a toggle switch or a logic level from the host system.

ALIGNMENT

To adjust write precompensation, issue a command to the FD179X so that write data pulses are present. This can be done with a 'WRITE TRACK' command and the $\overline{IP}$ line open, or a continuous 'WRITE SECTOR' operation. With a scope on pin 4 of the WD1691, adjust the precomp pot for the desired value. This will range from 100 to 300 ns typically.

The pulse width set on pin 4 (01) will be the desired precomp delay from nominal.

The data separator must be adjusted with the $\overline{RDD}$ or VFOE/WF line at Logic 1. Adjust the bias voltage potentiometer for 1.4V on pin 2 of the 74S124. Then adjust the range control to yield 4.0 MHz on pin 7 of the 74S124.

SUBSTITUTING VCO'S

There are other VCO circuits available that may be substituted for the 74S124. The specifications required are:

1) The VCO must free run at 4.0 MHz with a 1.4V control signal. The WD1691 will force this voltage 1 Volt in either direction (i.e., .4V = decrease frequency, 2.4V = increase frequency). If a + 15% capture range is desired, then a 1 Volt change on the VCO input should change the frequency by 15%. Capture range should be limited to about + 25%, to prevent the VCO from breaking into oscillation and/or losing lock because of noise spikes (causing abnormally quick adjustments of the VCO frequency). Jitter in the VCO output frequency may further be reduced by increasing the integration capacitor/resistor, but this will also decrease the final capture range and lock-up time.
2) The sink output current of the WD1691 is 3.2ma minimum. The source output current is -200ua. Therefore, source current is the limiting factor. Insure that the input circuitry of the VCO does not require source current in excess of -200ua.

Another alternative is to use a voltage follower/level shifter circuit to match the input requirements of the VCO chosen. A more complex filter can be used to convert the PUMP UP/PUMP DOWN pulses to the varying DC voltage signal required by the VCO, achieving an optimum condition between lock-up time and high frequency rejection.

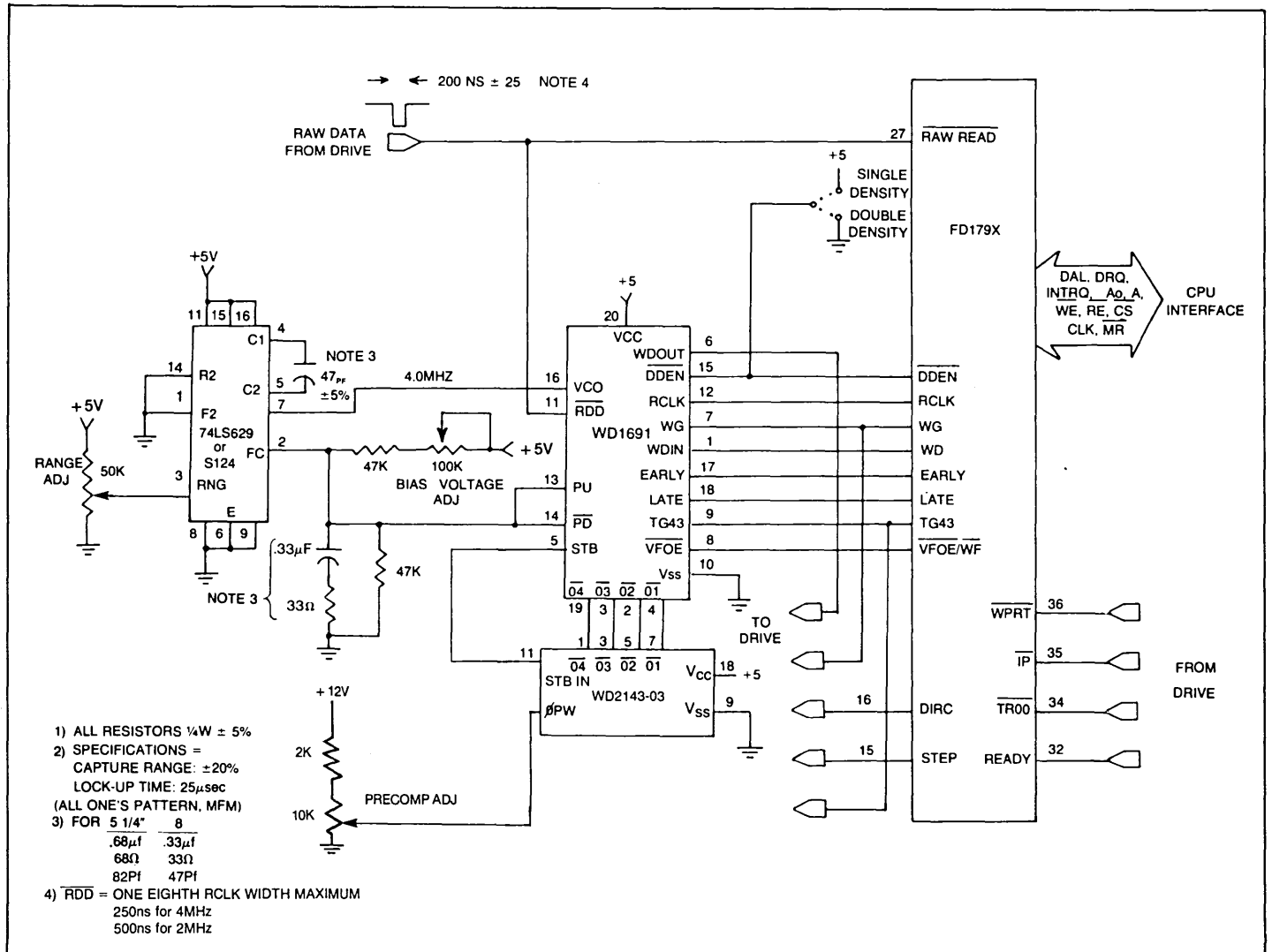
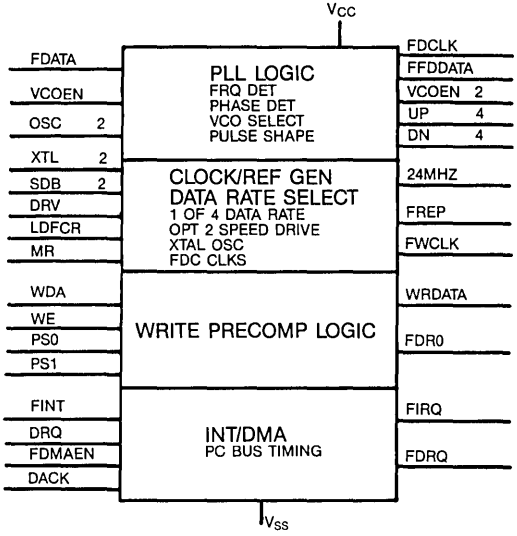


Figure 10. 8" SINGLE/DOUBLE DENSITY FLOPPY INTERFACE

WD16C92 Floppy Read/Write Circuit Device

FEATURES

- Compatible with NEC 765A Floppy Disk Controller
- CMOS
- TTL Compatible
- Single +5V Supply
- Phase Detector and Pulse shaping for Read Data
- Write Data Precompensation
- Floppy Controller Read/Write Clock Generation
- IBM PC/PC AT Bus Timing Compatible



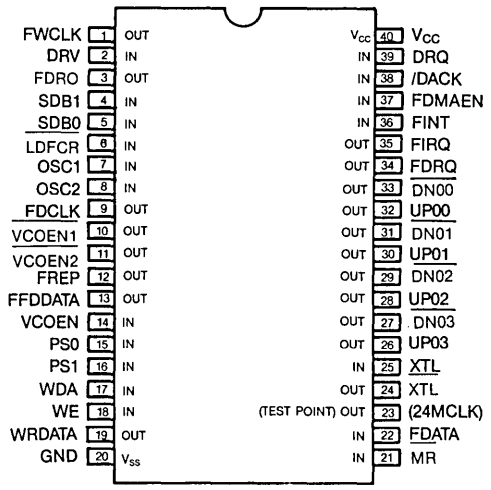
40 PIN DIP/44 PIN PLCC

DESCRIPTION

The WD16C92 is a 40-pin CMOS custom LSI device with full TTL level compatibility on input and output. It is intended to replace a number of discrete components needed with the NEC765A Floppy Disk Controller. The WD16C92 handles four primary functions:

- PLL Logic
- Clock Generation
- Write Precompensation
- Interrupt/DMA timing PC/PC AT Bus

This floppy support device augments the 765A controller while it reduces overall cost.



SIGNAL DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	FWCLK	WRITE CLOCK – TTL output, clock for write data.
2	DRV	DRIVE TYPE – TTL input with internal pullup resistor. Low level indicates special drive.
3	FDR0	SPEED SELECT – TTL output, latched image SDB0. (effective only on dual speed drives.)
4	SDB1	DATA BUS BIT 1 – TTL input, of data bus bit 1.
5	SDB0	DATA BUS BIT 0 – TTL input, of data bus bit 0.
6	$\overline{\text{LDFCR}}$	$\overline{\text{LOAD FLOPPY CONTROL REGISTER}}$ – TTL input causes SDB0 and SDB1 to be latched internally.
7	$\overline{\text{OSC1}}$	$\overline{\text{OSCILLATOR 1}}$ – TTL input, for 500 Kbs, 250 Kbs and 125 Kbs data rates (nominally 2.0 MHz)
8	$\overline{\text{OSC2}}$	$\overline{\text{OSCILLATOR 2}}$ – TTL input for 300 Kbs data rate (nominally 2.4 MHz)
9	FDCLK	READ DATA CLOCK – TTL output, provides window for floppy read data pulse.
10	$\overline{\text{VCOEN1}}$	$\overline{\text{VCO ENABLE 1}}$ – TTL output, enables VCO for 300 Kbs data rate.
11	$\overline{\text{VCOEN2}}$	$\overline{\text{VCO ENABLE 2}}$ – TTL output, enables VCO for 500, 250 and 125 Kbs data rates.
12	FREP	CLOCK OUTPUT – TTL output, provides clock signal for the μPD765A.
13	FFDDATA	READ DATA – TTL output, floppy read data pulses.
14	VCOEN	VC0 ENABLE – TTL input, from the μPD765A when high enables reading from the floppy disk.
15	PS0	PRECOMP BIT 0 – TTL input, decodes for precompensation of write data.
16	PS1	PRECOMP BIT 1 – TTL input, decodes for precompensation of write data.
17	WDA	WRITE DATA – TTL input, write floppy data from the μPD765A.
18	WE	WRITE ENABLE – TTL input, from the μPD765A to enable writing data on the floppy disk.
19	WRDATA	WRITE DATA – TTL output, precompensated data from the WD16C92 to be written on the floppy drive.
20	GND	GROUND
21	$\overline{\text{MR}}$	$\overline{\text{MASTER RESET}}$ – TTL input, clears all internal conditions to be reset. WD16C92 will default to the 500 Kbs data rate following a $\overline{\text{MR}}$.
22	FDATA	READ DATA – TTL input, raw read data from the floppy drive.
23	24MCLK	24 MHz CLOCK TEST POINT – TTL output, for test monitoring only; NOT to be used to drive any external circuitry.
24	$\overline{\text{XTL}}$	CRYSTAL RETURN – TTL output, return for 24 MHz crystal when used; otherwise not connected.
25	XTL	CRYSTAL INPUT – TTL input connection for 24 MHz crystal. Can optionally be used for 24 MHz TTL level square wave clock input.
26	UP03	UP PUMP 3 – Open drain output, provides up pump for 125 Kbs data rate.
27	$\overline{\text{DN03}}$	$\overline{\text{DOWN PUMP 3}}$ – Open drain output, provides down pump for 125 Kbs data rate.
28	UP02	UP PUMP 2 – Open drain output, provides up pump for 250 Kbs data rate.
29	$\overline{\text{DN02}}$	$\overline{\text{DOWN PUMP 2}}$ – Open drain output, provides down pump for 250 Kbs data rate.
30	UP01	UP PUMP 1 – Open drain output, provides up pump for 300 Kbs data rate.
31	$\overline{\text{DN01}}$	$\overline{\text{DOWN PUMP 1}}$ – Open drain output, provides down pump for 300 Kbs data rate.
32	UP00	UP PUMP 0 – Open drain output, provides up pump for 500 Kbs data rate.
33	$\overline{\text{DN00}}$	$\overline{\text{DOWN PUMP 0}}$ – Open drain output, provides down pump for 500 Kbs data rate.

SIGNAL DESCRIPTION (cont.)

PIN	MNEMONIC	DESCRIPTION
34	FDRQ	DELAYED DATA REQUEST – TTL TRI-STATE output, is the DRQ delayed by 2 μs and enabled by FDMAEN.
35	FIRQ	INTERRUPT REQUEST – TTL TRI-STATE output, generates an interrupt request on the PC/AT compatible bus and is gated by FDMAEN.
36	FINT	FLOPPY INTERRUPT – TTL input from μPD765A to generate bus interrupt request.
37	FDMAEN	FLOPPY DMA ENABLE – TTL input to gate FIRQ and FDRQ onto the PC/AT compatible bus.
38	$\overline{\text{DACK}}$	$\overline{\text{DATA ACKNOWLEDGE}}$ – TTL input, data acknowledge signal from the PC/AT compatible bus.
39	DRQ	DATA REQUEST – TTL input, from the μPD765A to request a data transfer between the data bus.
40	VCC	+5 volt ± 5% power supply input.

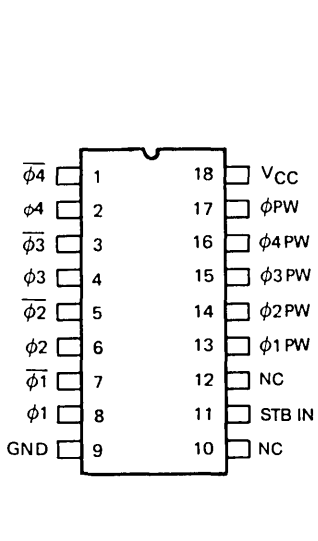
WD2143-03 Four Phase Clock Generator

FEATURES

- IMPROVED VERSION OF WD2143-01
- TRUE AND INVERTED OUTPUTS
- SINGLE 5 VOLT SUPPLY
- TTL COMPATABLE
- ON CHIP OSCILLATOR
- TTL CLOCK INPUT
- TTL CLOCK OUTPUT
- PROGRAMMABLE PULSE WIDTHS
- PROGRAMMABLE PHASE WIDTHS
- NO EXTERNAL CAPACITOR

GENERAL DESCRIPTION

The WD2143-03 Four-Phase Clock Generator is a MOS/LSI device capable of generating four phase clocks. The ouput pulse widths are controlled by tying an external resistor to the proper control inputs. All pulse widths may be set to the same width by tying the ϕPW line through an external resistor. Each pulse width can also be individually programmed by tying a resistor through the appropriate ϕ1PW-ϕ4PW control inputs.



PIN DESIGNATION

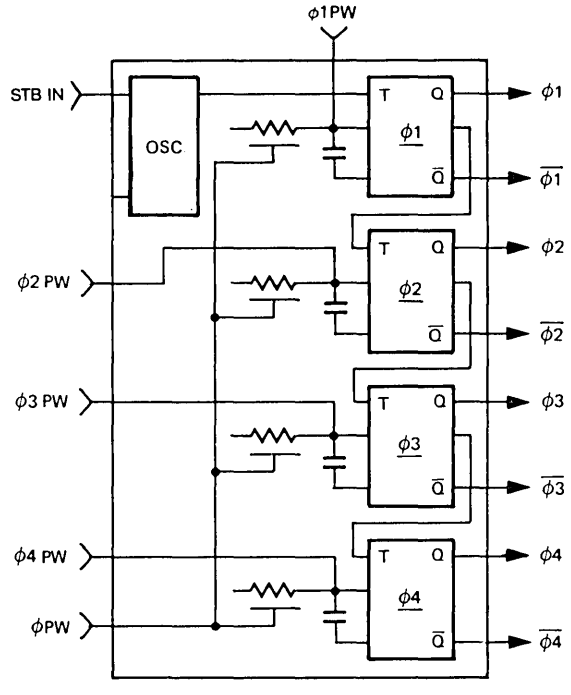


Figure 1. WD2143-03 BLOCK DIAGRAM

DEVICE OPERATION

Each of the phase outputs can be controlled individually by tying an external resistor from ϕ1PW-ϕ4PW to a +5V supply. When it is desired to have ϕ1 through ϕ4 outputs the same width, the ϕ1PW-ϕ4PW inputs should be left open and an external resistor tied from the ϕPW (Pin 17) input to +12V. STROBE IN (pin 11) is driven by a TTL square wave. Each of the four phase outputs provide both true and inverted signals, capable of driving 1 TTL load each.

PIN NUMBER	SYMBOL	DESCRIPTION
1,3,5,7	$\overline{\phi 1}$-$\overline{\phi 4}$	Four phase clock outputs. These outputs are inverted (active low).
2,4,6,8	$\phi 1$-$\phi 4$	Four Phase clock outputs. These outputs are true (active high).
9	GND	Ground.
10	NC	No connection.
11	STB IN	Input signal to initiate four-phase clock outputs.
12	NC	No connection.
13-16	ϕ1PW-ϕ4PW	External resistor inputs to control the individual pulse widths of each output. These pins can be left open if ϕPW is used.
17	ϕPW	External resistor input to control all phase outputs to the same pulse widths.
18	V_{CC}	+5V ± 5% power supply input.

Table 1. PIN DESCRIPTIONS

TYPICAL APPLICATIONS

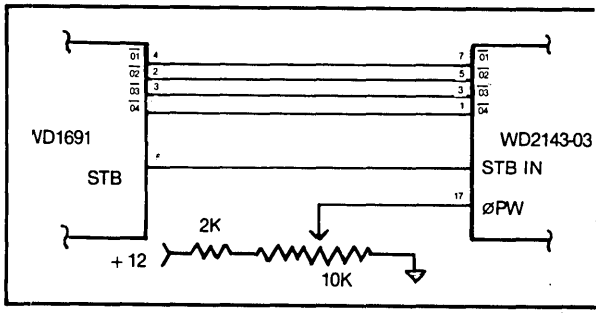


Figure 2. WRITE PRECOMP OPERATION WITH F.S.L. WD1691

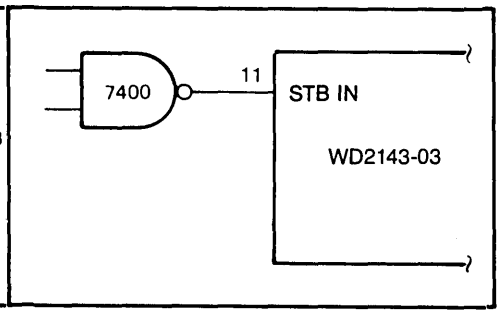


Figure 3. TTL SQUARE WAVE OPERATION

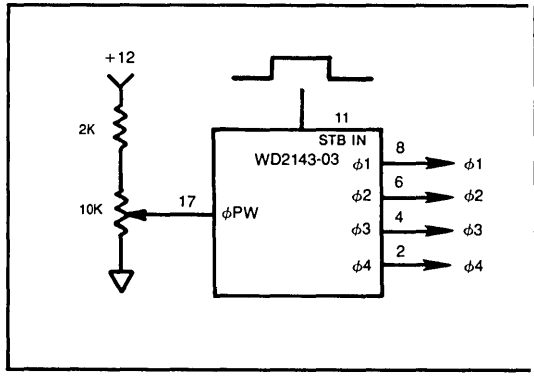


Figure 4. EQUAL PULSE WIDTH OUTPUTS

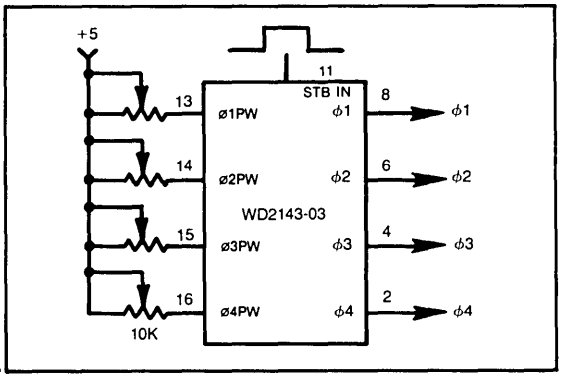


Figure 5. INDIVIDUAL PULSE WIDTH OUTPUTS

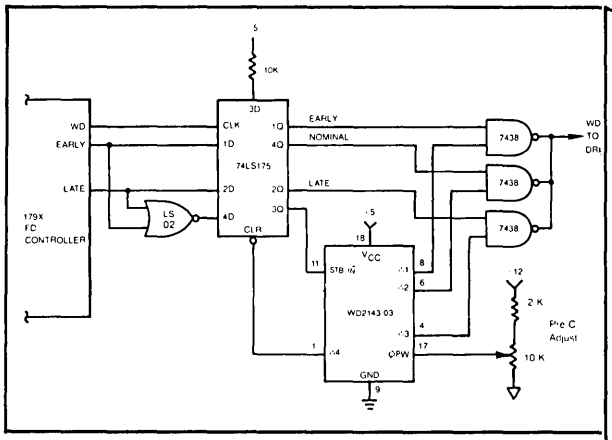


Figure 6. WRITE PRECOMP FOR FLOPPY DISK

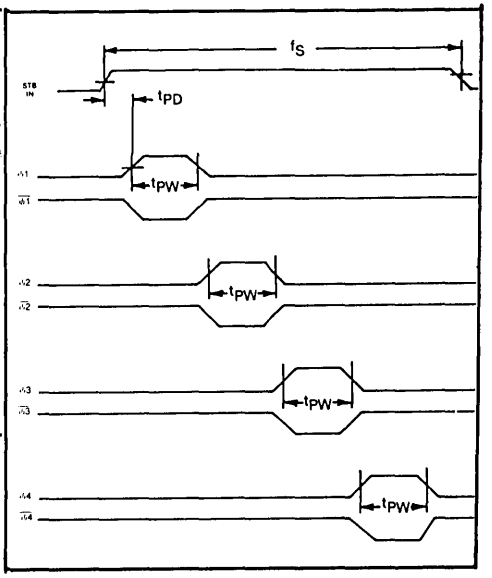


Figure 7. WD2143-03 TIMING DIAGRAM

SPECIFICATIONS

Absolute Maximum Ratings
Operating
Temperature .....0°C (32°F) to +70°C (158°F)
Voltage on any pin with
respect to Ground* -0.5 to +7V
Power Dissipation 1 Watt
Storage Temperature
plastic .....-55°C (-67°F) to +125°C (257°F)
ceramic .....-65°C (-85°F) to +150°C (302°F)

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to the DC electrical characteristics specified.

*Pin 27 = -0.5V to +12V. Increasing voltage on Pin 17 will decrease T_{pw}.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ± 5%, GND = 0V, T_A = 0°C (32°F) to 70°C (158°F).

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{OL}	TTL low level output		0.4	V	I_{OL} = 1.6 mA
V_{OH}	TTL high level output	2.0		V	I_{OH} = -100μ A
V_{IL}	STB in low voltage		0.8	V	
V_{IH}	STB in high voltage	2.4		V	
I_{CC}	Supply Current		80	mA	All outputs open

Table 2. DC ELECTRICAL CHARACTERISTICS

SWITCHING CHARACTERISTICS

V_{CC} = 5V ± 5%, GND = 0V, T_A = 0°C (32°F) to 70°C (158°F)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
t_{PD}	STB IN to ϕ1		140	ns	
t_{pw}	Pulse Width (any output)	100	300	ns	CL = 30pf
t_{PR}	Rise Time (any output)		30	ns	CL = 30pf
t_{PF}	Fall Time (any output)		25	ns	CL = 30pf
f_S	STROBE PULSE WIDTH		1.0	ns	combined t_{pw} = 400 ns
t_{DWP}	Pulse Width Differential		± 10	%	Referenced to ϕ1, 100-300 ns

Table 3. SWITCHING CHARACTERISTICS

Note: T_{PW} measured at 50% V_{OH} Point; V_{OL} = 0.8V, V_{OH} = 2.0V.

WESTERN DIGITAL
CORPORATION

WD9216-00/WD9216-01
Floppy Disk Data Separator — FDDS

FEATURES

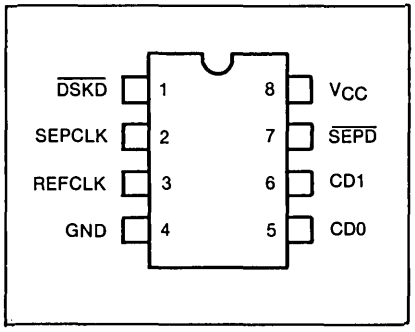
- PERFORMS COMPLETE DATA SEPARATION FUNCTION FOR FLOPPY DISK DRIVES
- SEPARATES FM OR MFM ENCODED DATA FROM ANY MAGNETIC MEDIA
- ELIMINATES SEVERAL SSI AND MSI DEVICES NORMALLY USED FOR DATA SEPARATION
- NO CRITICAL ADJUSTMENTS REQUIRED
- COMPATIBLE WITH WESTERN DIGITAL 179X, 176X AND OTHER FLOPPY DISK CONTROLLERS
- SMALL 8-PIN DUAL-IN-LINE PACKAGE
- +5 VOLT ONLY POWER SUPPLY
- TTL COMPATIBLE INPUTS AND OUTPUTS

GENERAL DESCRIPTION

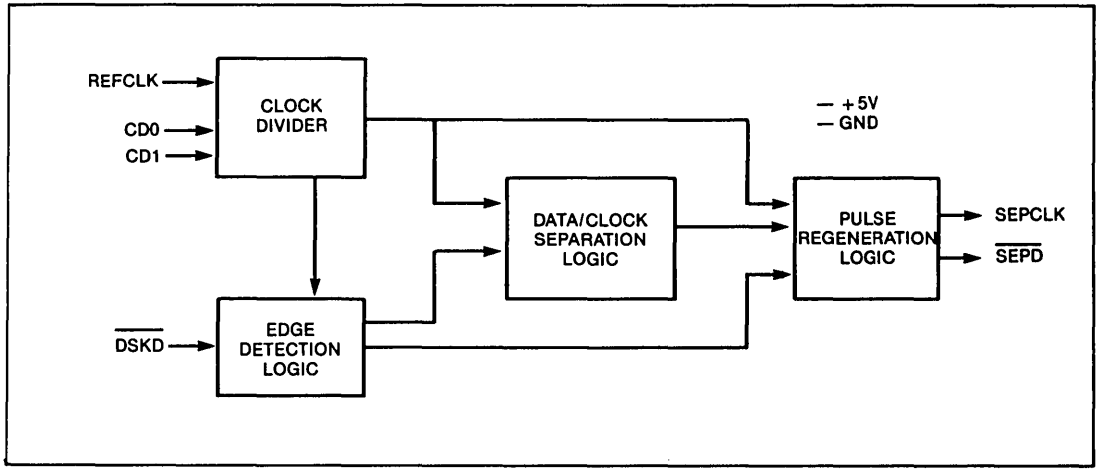
The Floppy Disk Data Separator provides a low cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate Clock and Data Inputs for a Floppy Disk Controller.

The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry. Supplied in an 8-pin Dual-in-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL compatible on all inputs and outputs.

The WD9216 is available in two versions; the WD9216-00, which is intended for 5 1 / 4" disks and the WD9216-01 for 5 1 / 4" and 8" disks.



PIN CONFIGURATION



FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Operating Temperature Rnge .....0°C to +70°C
Storage Temperature Range.....-55°C TO 125°
Positive Voltage on any Pin,
with respect to ground ..... +8.0V
Negative Voltage on any Pin,
with respect to ground.....-0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

OPERATING CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = ± 5%, unless otherwise noted.)

PARAMETER		MIN.	TYP.	MAX.	UNITS	COMMENTS
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level V_{IL}				0.8	V	
High Level V_{IL}		2.0			V	
OUTPUT VOLTAGE LEVELS						
Low Level V_{OL}				0.4	V	I_{OL} = 1.6 mA
High Level V_{OH}		2.4			V	I_{OH} = -100 A
INPUT CURRENT						
Leakage I_{IL}				10	μA	0 < V_{IN} < V_{DD}
INPUT CAPACITANCE						
All Inputs				10	pF	
POWER SUPPLY CURRENT						
I_{DD}				50	mA	
A.C. CHARACTERISTICS						
Symbol						
f_{CY}	REFCLK Frequency	0.2		4.3	MHz	WD9216-00
f_{CY}	REFCLK Frequency	0.2		8.3	MHz	WD9216-01
t_{CKH}	REFCLK High Time	50		2500	ns	
t_{CKL}	REFCLK Low Time	50		2500	ns	
t_{SDON}	REFCLK to $\overline{SEPD}$ "ON" Delay		100		ns	
t_{SDOFF}	REFCLK to SEPD "OFF" Delay		100		ns	
t_{SPCK}	REFCLK to SEPCLK Delay	100			ns	
t_{DLL}	DSKD Active Low Time	0.1		100	μs	
t_{DLK}	DSKD Active High Time	0.2		100	μs	

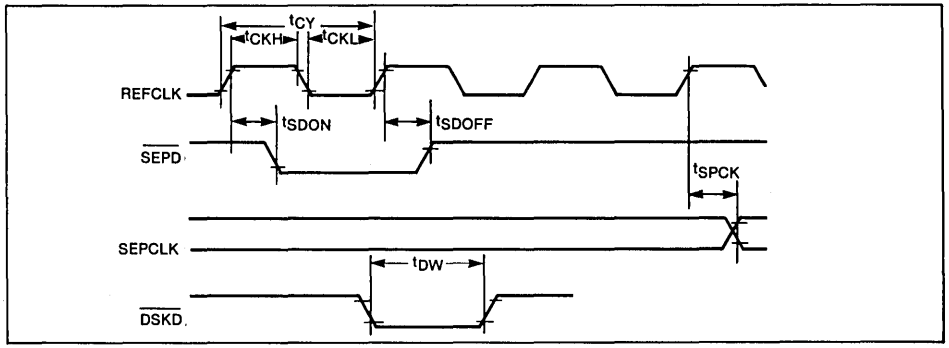


Figure 3. AC CHARACTERISTICS

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	$\overline{\text{Disk Data}}$	$\overline{\text{DSKD}}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Referenced Clock	REFLCK	Reference clock input.
4	Ground	GND	Ground.
5,6	Clock Divisor	CD0,CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: CD1 CD0 Divisor 0 0 1 0 1 2 1 0 4 1 1 8
7	$\overline{\text{Separated Data}}$	$\overline{\text{SEPD}}$	SEPD is the data output of the FDDS.
8	Power Supply	V_{CC}	+5 volt power supply.

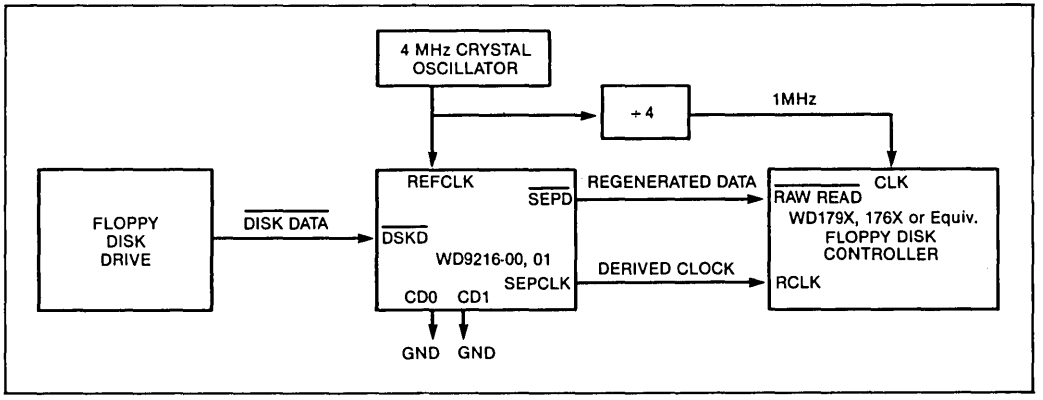


Figure 1. TYPICAL SYSTEM CONFIGURATION (5 1 / 4" Drive, Double Density)

OPERATION

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per Table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output. Separate short and long term timing correctors assure accurate clock separation.

The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

Table 1. CLOCK DIVIDER SELECTION TABLE

DRIVE (8" or 5 1 / 4")	DENSITY (DD or SD)	REFCLK MHz	CD1	CD0	REMARKS
8	DD	8	0	0	
8	SD	8	0	1	Select either one
8	SD	4	0	0	
5 1/4	DD	8	0	1	
5 1/4	DD	4	0	0	Select either one
5 1/4	SD	8	1	0	
5 1/4	SD	4	0	1	Selecct any one
5 1/4	SD	2	0	0	

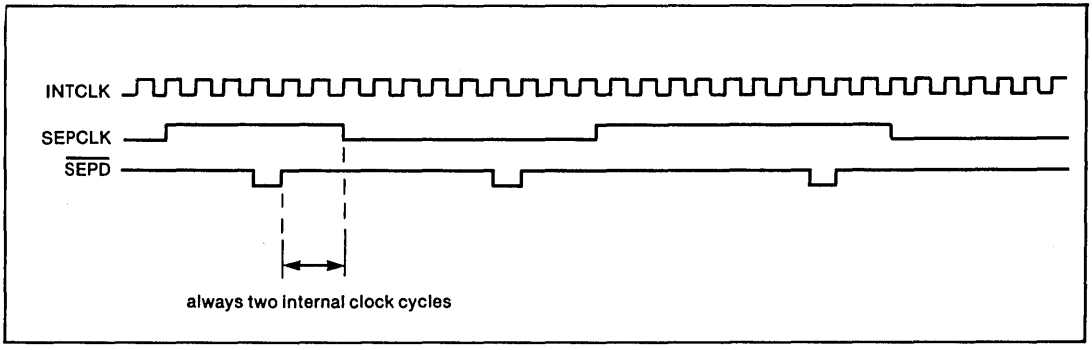
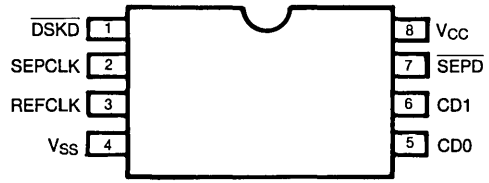


Figure 2. REFERENCE CLOCK TIMING

WD92C32 Floppy Disk Digital Data Separator

FEATURES

- HIGH PERFORMANCE DIGITAL DATA SEPARATOR (Low error rates)
- NO ADJUSTMENTS
- 8 PIN DIP
- TTL COMPATIBLE
- CMOS
- SINGLE 5V SUPPLY
- PIN FUNCTION COMPATIBLE WITH THE WD9216



PIN CONFIGURATION

GENERAL DESCRIPTION

The WD92C32 digital data separator has been designed to address the high performance 5¼" or 8" floppy disk drive market. It is pin function compatible with the WD9216, although it provides superior performance in terms of available bit jitter window margins. The WD92C32 is designed to operate at data rates of 125, 250 and 300, and 500 Kb/s.

The WD92C32 is a CMOS LSI product with TTL compatible I/O which operates from a single 5 volt supply. Packaged as an 8 pin DIP, the WD92C32 represents a significant cost savings when compared to the cost of the analog components required to achieve equal performance.

The device contains an internal power-up reset along with all of the necessary logic to achieve classical 2nd order phase locked loop performance. Implemented digitally this design does not require any external adjustments or any additional logic to perform the data separation.

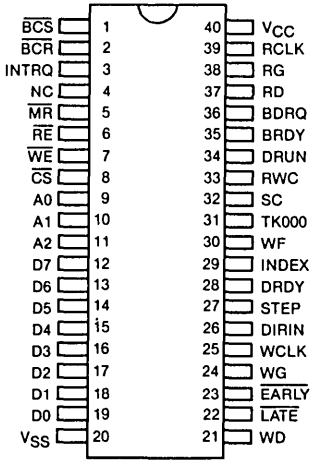
DESCRIPTIONS OF PIN FUNCTIONS

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
1	$\overline{\text{DSKD}}$	$\overline{\text{Disk Data}}$	Data input signal from the floppy drive containing both clock and data information.
2	SEPCLK	Separated Clock	Resultant clock recovered from the disk serial bit stream. Sometimes called RCLK.
3	REFCLK	Reference Clock	Reference clock input from a crystal oscillator.
4	V_{SS}	Ground	Ground
5 6	CD0, CD1	Clock Divisor	Encoded bits which are used to select 1 of 4 reference clock division factors.
7	$\overline{\text{SEPD}}$	$\overline{\text{Separated Data}}$	Sometimes called RDATA, this is still the encoded serial bit stream, but which has been re-synchronized to the phase of Recovered Clock.
8	V_{CC}	Power Supply	+5V power supply

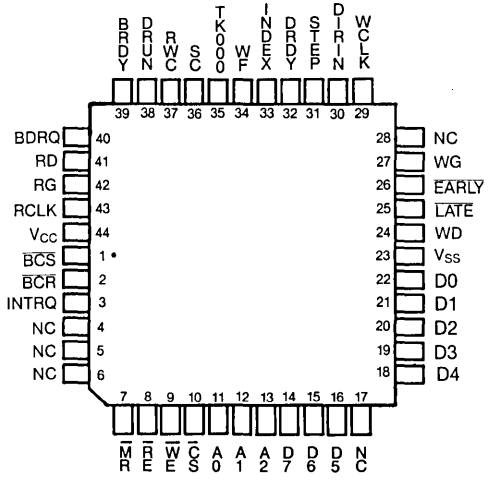
WD1010-05 Winchester Disk Controller

FEATURES

- ST506-SA1000 COMPATIBLE
- MULTIPLE SECTOR READ/WRITE
- UP TO 5 MBITS/SEC DATA RATE
- UNLIMITED SECTOR INTERLEAVE
- AUTOMATIC FORMATTING
- CRC/ECC CAPABILITY WITH EXTERNAL ECC GENERATOR/CHECKER
- PROGRAMMABLE RETRIES
- VARIABLE SECTOR SIZE
- SINGLE +5V SUPPLY



PIN DESIGNATION



QUAD PIN DESIGNATION

DESCRIPTION

The WD1010-05 is a MOS/LSI device which performs the functions of a Winchester Disk Controller/Formatter. It is compatible with the Seagate ST506 and the Shugart Associates SA1000 drives, as well as all other 5 ¼" and 8" products utilizing the same type of interface. On the host side, an 8-bit bi-directional bus accepts all commands, data, and status bytes. The Western Digital WD1000 series of board level controllers are software compatible with the WD1010-05.

Operating from a single 5 volt supply, the WD1010-05 is implemented in NMOS silicon gate technology and is available in a 40-pin dual-in-line and QSM package.

ARCHITECTURE

The WD1010-05 Winchester Disk Controller provides the necessary link between an 8-bit, parallel processor and a Winchester disk drive. The WD1010-05 may be programmed to either automatically retry errors, or to terminate the command. The internal architecture of the WD1010-05 is shown in Figure 1. Its major functional blocks are:

PLA Controller

The PLA interprets commands and provides all control functions. It is synchronized with WCLK.

Magnitude Comparator

A 10-bit magnitude comparator is used for calculation of drive step, direction, present and desired cylinder position.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
1	$\overline{BCS}$	BUFFER CHIP SELECT	Active low output used to enable reading or writing of the external sector buffer.
2	$\overline{BCR}$	BUFFER COUNTER RESET	Active low output that is strobed by the WD1010-05 prior to read/write operations. This pin is strobed whenever BCS changes state.
3	INTRQ	INTERRUPT REQUEST	INTRQ is an output asserted upon completion of a command and de-asserted when the Status Register is read or a new command is written into the Command Register. This signal can be programmed to occur with BDRQ and DRQ during Read Command.
4	NC	NO CONNECTION	
5	$\overline{MR}$	MASTER RESET	A logic low in this input will initialize all internal logic.
6	$\overline{RE}$	READ ENABLE	Tri-state bi-directional line used as an input for reading the task register and an output when the WD1010-05 is reading the buffer.
7	$\overline{WE}$	WRITE ENABLE	Tri-state bi-directional line used as an input for writing into the task register and as an output when the WD1010-15 is writing to the buffer.
8	$\overline{CS}$	CHIP SELECT	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
9 10 11	A0 A1 A2	ADDRESS 0 ADDRESS 1 ADDRESS 2	These three inputs select the register to receive/transmit data on D0-D7.
12 thru 19	D7 thru D0	DATA 7 thru DATA 0	8-bit tri-state bi-directional bus used for transfer of commands, status, and data.
20	V_{SS}	GROUND	Ground.
21	WD	WRITE DATA	This output contains the MFM clock and data pulses to be written on the disk.
22 23	$\overline{LATE}$ $\overline{EARLY}$	$\overline{LATE}$ $\overline{EARLY}$	Precompensation outputs used to delay the WD pulses externally.
24	WG	WRITE GATE	This output is set to a logic high before writing is to be performed on the disk.
25	WCLK	WRITE CLOCK	4.34 or 5.0 MHz clock input used to derive all internal write timing.
26	DIRIN	DIRECTION IN	This output determines the direction the stepping motor will move the heads. High = in, Low = out.
27	STEP	STEP PULSE	This output generates a pulse for stepping the drive motor.
28	DRDY	DRIVE READY	This input must be at a logic high in order for commands to execute.
29	INDEX	INDEX PULSE	A rising edge on this input informs the WD1010-05 when the index hole has been encountered.
30	WF	WRITE FAULT	An error input to the WD1010-05 which indicates a fault condition at the drive.
31	TK000	TRACK 000	An input to the WD1010-05 which indicates positioning over track 000.

PIN DESCRIPTION (Continued)

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
32	SC	SEEK COMPLETE	A rising edge on this input informs the WD1010-05 when head settling time has expired. In the Format Command, it is used to extend the gap.
33	RWC	REDUCED WRITE CURRENT	This output can be programmed to reduce write current on a selected starting cylinder.
34	DRUN	DATA RUN	This input informs the WD1010-05 when a field of ones or zeroes have been detected.
35	BRDY	BUFFER READY	The rising edge of this input informs the controller that the Sector Buffer is full or empty.
36	BDRQ	BUFFER DATA REQUEST	BDRA and DRQ (Bit 3 Status Register) are asserted when the Buffer is to be read from or written to, by the Host. BDRQ can be used by a DMA controller or by the Host during Programmed I/O. DRQ must be polled by the Host if used during programmed I/O.
37	RD	READ DATA	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
38	RG	READ GATE	This output is set to a logic high when data is being inspected from the disk.
39	RCLK	READ CLOCK	A nominal square wave clock input derived from the external data recovery circuits.
40	V_{CC}	+5 VOLT	+5V

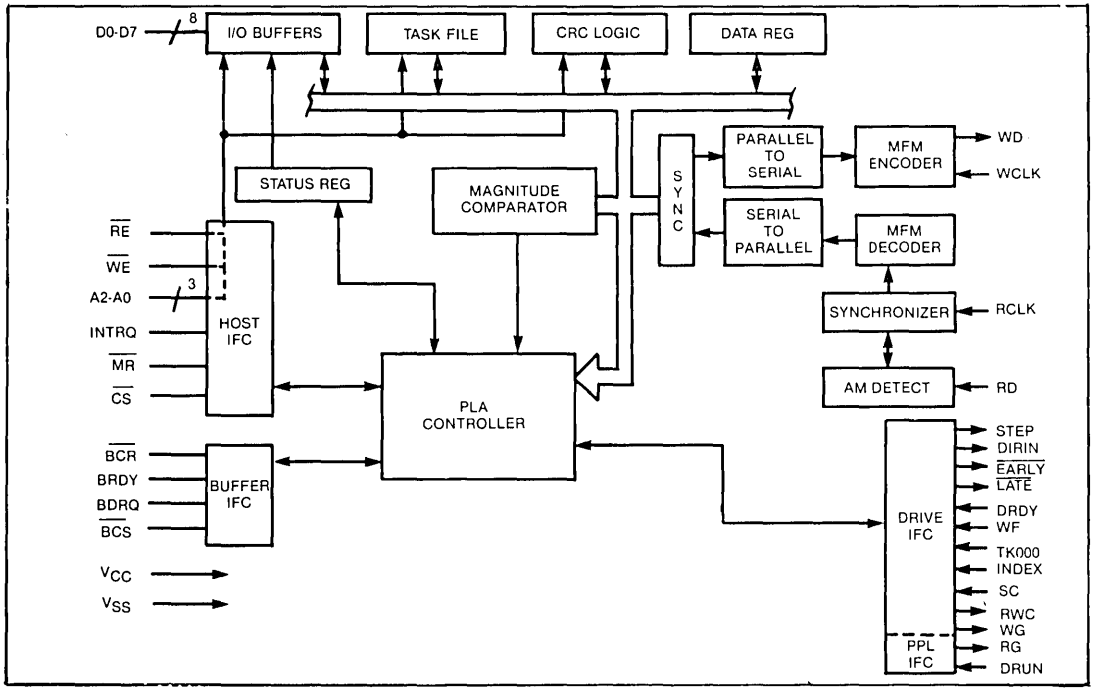


FIGURE 1.
WD1010 BLOCK DIAGRAM

CRC Logic

Generates and checks the cyclic redundancy check characters appended to the ID and data fields. The polynomial is $X^{16} + X^{12} + X^5 + 1$.

MFM Encode/Decode

Encodes and decodes MFM data to be written/read from the drive. The MFM encoder operates from WCLK; a clock having a frequency equivalent to the bit rate. The MFM decode operates from RCLK; a bit rate clock generated from the external data separator. RCLK and WCLK need not be synchronized.

AM Detect

The address mark detector checks the incoming data stream for a unique missing clock pattern (Data = A1 hex, Clock = 0A hex) used in each ID and data field.

Host/Buffer IFC

This logic contains all of the necessary circuitry to communicate with the 8-bit host processor.

Drive IFC

This logic controls and monitors all lines from the drive, with the exception of read and write data.

DRIVE INTERFACE

The drive side of the WD1010-05 controller requires three sections of external logic. These are buffers/receivers, data separator, and write precompensation. Figure 2 illustrates a drive side interface.

The buffer/receivers condition the control lines to be driven down the cable to the drive. The control lines are typically single-ended, resistor terminated TTL levels. The data lines to and from the drive also require buffering, but are differential RS-422 levels. The interface specification to the drive can be found in the manufacturers' OEM manual. The WD1010-05 supplies TTL compatible signals, and will interface to most buffer/driver devices.

The data recovery circuits consist of a phase-lock loop data separator and associated components. The WD1010-05 interacts with the data separator through the DRUN and RG signals. The block diagram of the

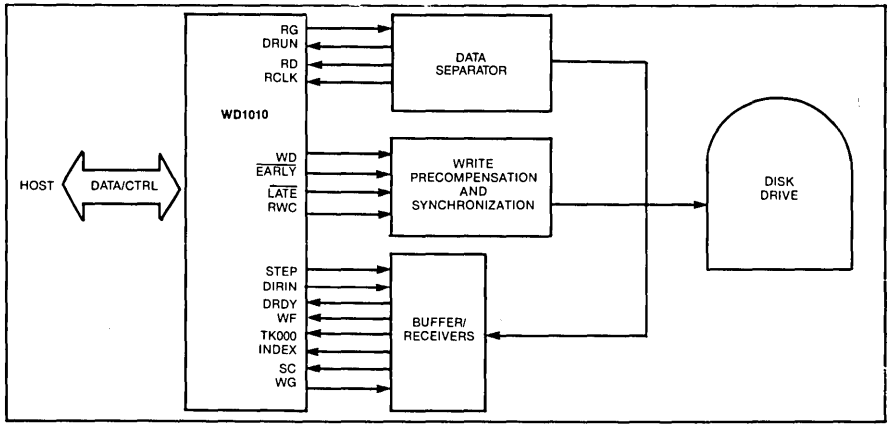


FIGURE 2. DRIVE INTERFACE BLOCK DIAGRAM

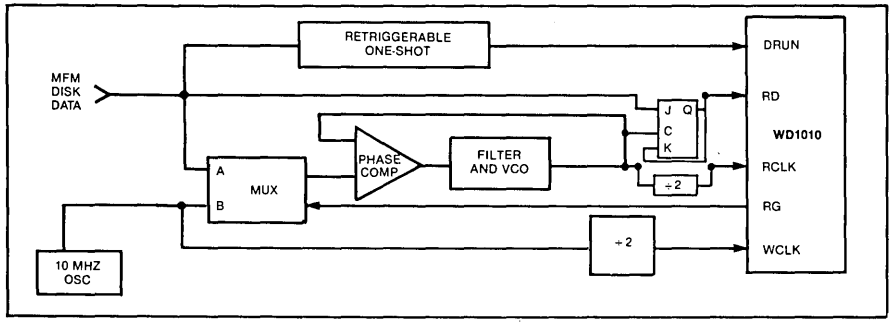


FIGURE 3. DATA RECOVERY CIRCUIT

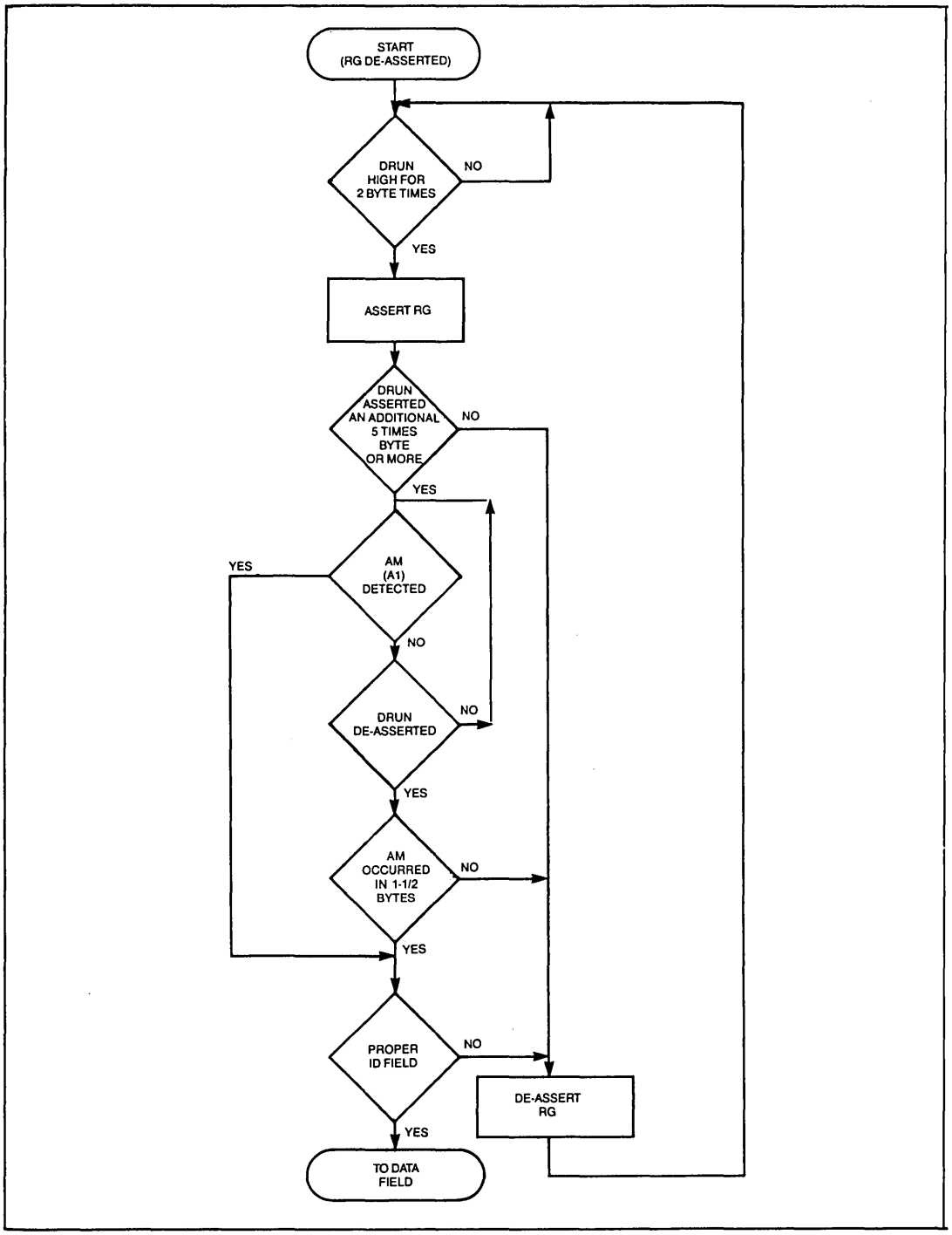


FIGURE 4. PLL CONTROL SEQUENCE FOR ID FIELD

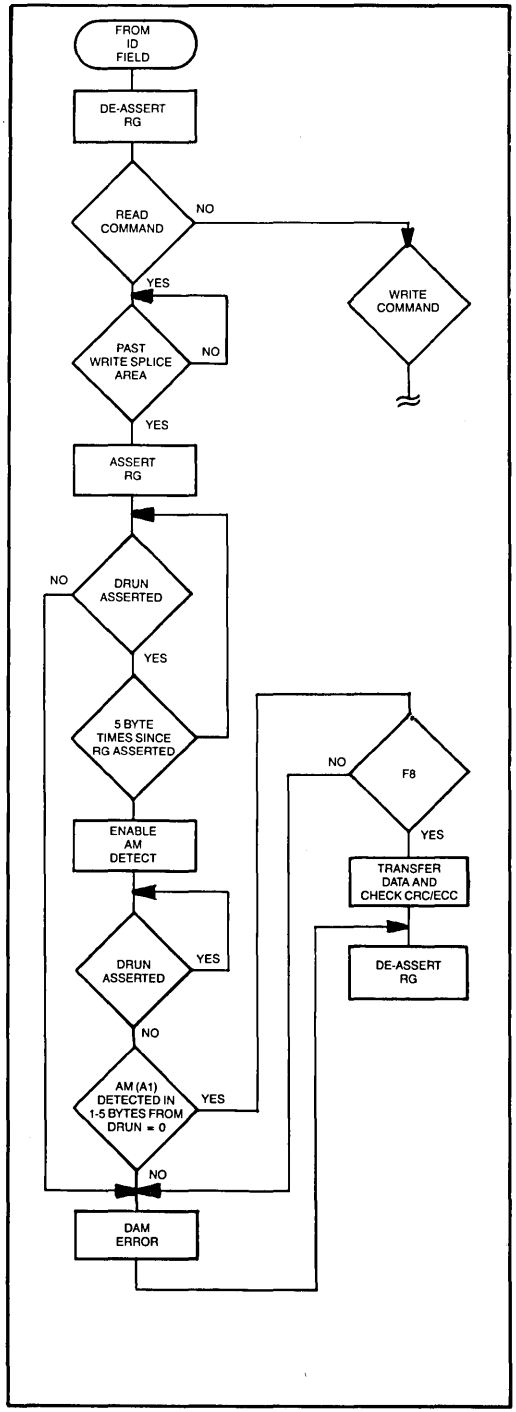


FIGURE 4. (CONT.)
PPL CONTROL SEQUENCE FOR DATA FIELD

data separator circuit is shown in Figure 3. Read data from the drive is presented to the RD input of the WD1010-05, the reference multiplexor, and a retriggerable one shot. The read gate output will be low when the WD1010-05 is not inspecting data. The PLL at this time should remain locked to the reference clock.

When any Read/Write command is initiated and a search for address marks begins, the DRUN input is examined. The DRUN one-shot is set for slightly greater than one bit time, allowing it to retrigger constantly on a field of ones and zeroes. An internal counter times out to see that DRUN is high for 2 byte times. Read gate is set by the WD1010-05, switching the data separator to lock onto the incoming data stream. If DRUN falls prior to 7 bytes times, RG is lowered and the process is repeated. Read gate will remain active high until a non-zero, non-address mark byte is detected. It then will lower read gate for 2 byte times (to allow the PLL to lock back on the reference clock) and start the DRUN search over again. If an address mark is detected, read gate will be held high and the command will continue searching for the proper ID field. This sequence is shown in the flow chart of Figure 4.

The write precompensation logic is controlled by the signals RWC, EARLY and LATE. The cylinder in which the RWC line becomes active is controlled by a register in the Task File. It can be used to turn on the precomp circuitry on a predetermined cylinder. If the write precomp register value is FF, then RWC will always be low.

The signals $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ are used to tell the precomp how much delay is required on the write data pulse about to be sent. The amount of delay is determined externally through a digital delay line or equivalent circuitry. Since the signal $\overline{\text{EARLY}}$ occurs after the fact, write data should be delayed one interval when both $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ are deasserted; two intervals when $\overline{\text{LATE}}$ is asserted; and no delay when $\overline{\text{EARLY}}$ is asserted. An interval, for example, is 12-15 ns. on the ST506. $\overline{\text{EARLY}}$ or $\overline{\text{LATE}}$ will be active slightly ahead of the write data pulse; $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ will never be asserted at the same time. The $\overline{\text{EARLY}}$ $\overline{\text{LATE}}$ signals function independently of the content of the RWC register.

Examples for all three of the above circuits can be found in the WD1010 Application Note.

HOST INTERFACE

The primary interface between the host processor and the WD1010-05 is through an 8-bit bi-directional bus. This bus is used to transmit/receive data to both the WD1010-05 and a sector buffer. The sector buffer is constructed with either FIFO memory or static RAM and a counter. Since the WD1010-05 will make the bus active when accessing the sector buffer, a transceiver must be used to isolate the host during this time. Figure 5 shows a typical connection to a sector buffer implemented with RAM memory.

Whenever the WD1010-05 is not using the sector buffer, the $\overline{BCS}$ is de-asserted. This allows the host to access the WD1010's Task File, and to set up parameters prior to issuing a command. It also allows the host to access the RAM buffer. A decoder is used to generate a chip select when A_0- A_2 are '000'; an unused address in the WD1010-05. A binary counter is enabled whenever $\overline{RE}$ or $\overline{WE}$ goes active and incremented on the trailing edge of the chip select. This allows the host to access sequential bytes within the RAM. The decoder also generates another chip select when A_0-A_2 '000'; allowing access to the WD1010-05's internal registers while keeping the RAM tri-stated.

During write sector commands, the processor sets up data in the Task File and issues the command. The WD1010 then generates a status to inform the host it may load the buffer with the data to be written. When the counter reaches its maximum count, the BRDY signal is made active (by the "carry" out of the counter), informing the WD1010-05 that the buffer is full. (BRDY is a rising edge activated signal). The $\overline{BCS}$ is then asserted, disconnecting the host through the transceivers, and the $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1010-05 to allow it access to the buffer. When the WD1010-05 is done using the buffer, it disables $\overline{BCS}$ which again allows host access to this local bus. The read sector commands operate in a similar manner, except the buffer is loaded by the WD1010-05 instead of the host.

Another control signal called BDRQ can be connected to a DMA controller in the Host, or can be polled by the Host for programmed I/O. For further explanation, refer to the description of the individual commands and the A.C. Timing Specifications. In a read command; an interrupt may be specified to occur either at the end of the command or when BDRQ is activated. The INTRQ is cleared either by reading the status register or by writing a new command in the command register.

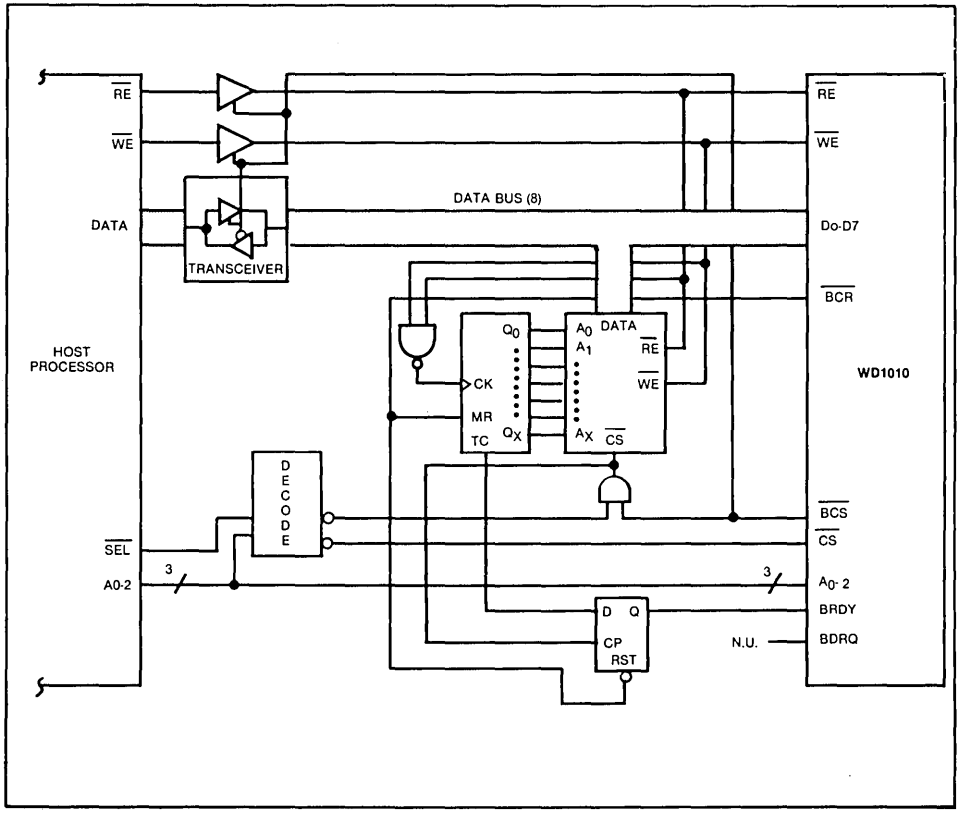


FIGURE 5.
HOST INTERFACE

TASK FILE

The Task File is a bank of nine registers used to hold parameter information pertaining to each command. These registers and their addresses are:

A_2	A_1	A_0	READ	WRITE
0	0	0	(Bus Tri-Stated)	(Bus Tri-Stated)
0	0	1	Error Flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Low	Cylinder Low
1	0	1	Cylinder High	Cylinder High
1	1	0	SDH	SDH
1	1	1	Status Register	Command Register

NOTE: Registers are not cleared by master reset ($\overline{MR}$).

ERROR REGISTER

This read-only register contains specific error status after the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC	-	ID	-	AC	TK	DM

Bit 7 – Bad Block Detect

This bit is set when an ID field has been encountered that contains a bad block mark. Used for bad sector mapping.

Bit 6 – CRC Data Field

This bit is set when a CRC error occurs in the data field. With Retry enabled, ten more attempts are made to read the sector correctly. If none of these attempts are successful, the Error Status is set also (bit 0 in the Status Register). If one of the attempts is successful, this bit remains set to inform the Host that a marginal condition exists. However, the Error Status bit is not set. Even if errors exist, the data can be read.

Bit 5 – Reserved

Not used; forced to a zero.

Bit 4 – ID Not Found

This bit is set to indicate that the correct cylinder, head, sector number or sector size parameter could not be found, or that a CRC error occurred on the ID field. This bit is set on the first failure and remains set even if the error is recovered on a Retry. When recovery is unsuccessful, the Error Status bit is set also (bit 0 in the Status Register).

Bit 3 – Reserved

Not used; forced to a zero.

Bit 2 – Aborted Command

This bit is set if a command was issued while the DRDY is de-asserted or the WF is asserted. The aborted command bit will also be set if an undefined command code is written into the command register, but an implied seek will be executed.

Bit 1 – Track Zero Error

This bit is set only by the restore command. It indicates that the TK000 has not gone active after the issuance of 1024 stepping pulses.

Bit 0 – Data Address Mark Not Found

This bit is set during a read sector command if the data address mark is not found after the proper sector ID is read.

WRITE PRECOMP CYLINDER

This register is used to define the cylinder number where the RWC is to be asserted:

7	6	5	4	3	2	1	0
CYLINDER NUMBER ÷ 4							

The value 00-FF loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted. Thus, a value of 01 hex will cause RWC to activate on cylinder 4; 02 hex on cylinder 8, and so on. Switching points are then 0, 4, 8, . . . The RWC will be asserted when the present cylinder is equal to 4 times or more than the value in this register. For example, the ST506 requires precomp on cylinder 128 (80 hex) and above. Therefore, the write precomp cylinder register should be loaded with 32 (20 hex).

A value of FF hex will always cause RWC to be low, no matter what the cylinder number values are.

SECTOR COUNT

This register holds the number of sectors that are to be transferred to the buffer.

7	6	5	4	3	2	1	0
# OF SECTORS							

This register is used during a multiple sector R/W command. The written value is decremented after each sector is transferred to the sector buffer. A zero represents a 256 sector transfer, a 1 = one sector transfer, etc. This register is a "don't care" when single sector commands are specified.

SECTOR NUMBER

This register holds the sector number of a desired sector:

7	6	5	4	3	2	1	0
SECTOR NUMBER							

During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. The sector number register may contain any value from 0 to 255.

CYLINDER NUMBER LOW

This register holds the least significant eight bits of the desired cylinder number.

7	6	5	4	3	2	1	0
LS BYTE OF CYLINDER NUMBER							

It is used with the cylinder number high register to specify a range of 0 to 1023.

CYLINDER NUMBER HIGH

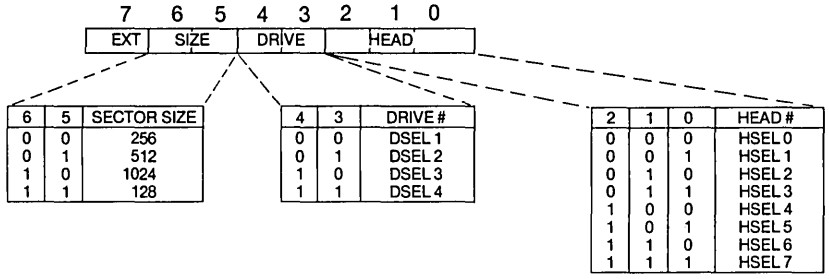
This register defines the two most significant bits of the cylinder number desired:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	(9)	(8)

Internal to the WD1010-05 is another pair of registers that hold the actual position number where the R/W heads are located. The cylinder number high and lkow registers can be considered the cylinder destination for seeks and other commands. After these commands are executed, the internal cylinder position registers' contents are equal to the cylinder high/low registers. If a drive number change is detected on a new command, the WD1010-05 automatically reads an ID field to update its internal cylinder position registers. This affects all commands except a Restore.

SDH BYTE

This register contains the desired sector size, drive number, and head number parameters. The format is:



6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

Both head number and sector size is compared against the disks' ID field. Head select and drive select lines are not available as outputs from the WD1010-05, and must be generated externally. Figure 6 shows the logic to implement these select lines.

Bit 7, the extension bit, is used to extend the data field by seven bytes when using ECC codes. CRC is not appended to the data field when EXT = 1; the data field becomes "sector size + 7" bytes long. CRC is checked on the ID field regardless of the state of the extention bit. Note that the sector size bits are written to the ID during a format command. The SDH byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number written but does have bad block mark written. The format is:

BAD BLOCK	SIZE	0 0	HEAD#
7	6 5	4 3	2 1 0

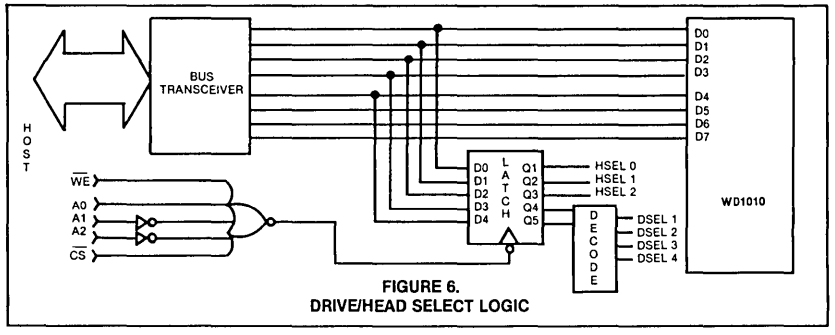


FIGURE 6.
DRIVE/HEAD SELECT LOGIC

STATUS REGISTER

The status register is a read-only register which informs the host of certain events performed by the WD1010 as well as reporting status from the drive control lines. The term INTRQ, if set, will be cleared when the status register is read. The format is:

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	-	CIP	ERR

Bit 7 – Busy

This bit is set whenever the WD1010-05 is accessing the disk. Commands should not be loaded into the command register while busy is set. Busy is made active when a command is written into the WD1010-05 and is deactivated at the end of all commands except the read sector. While executing a read sector command, busy is deactivated after the sector buffer has been filled. When the BUSY bit is set, no other bits in either the status or other registers are valid.

Bit 6 – Ready

This bit reflects the state of DRDY.

Bit 5 – Write Fault

This bit reflects the state of the WF. Whenever the WF bit goes high, an interrupt will be generated.

Bit 4 – Seek Complete

This bit reflects that state of the SC. When a seek has been initiated by a command, it will pause until the seek is completed.

Bit 3 – Data Request

This bit reflects the state of the BDRQ. It is set when the sector buffer should be loaded with data or read by the host, depending upon the command. DRQ/BDRQ remains high until BRDY is sensed, indicating the operation is completed. The BRDQ signal can be used in DMA interfacing or Programmed I/O, while the DRQ bit can be used only for programmed I/O transfers.

Bit 2 – Reserved

Not used. This bit is always forced to a zero.

Bit 1 – Command In Progress

When this bit is set, a command is being executed and a new command should not be loaded until reset. Although a command may be executing, the sector buffer is still available for access by the host. When the WD1010 is not busy (bit 7 = 0) the status register may be read. If other registers are read while CIP, the status register contents are returned.

Bit 0 – Error

This bit indicates that a non-recoverable error has occurred. When the Host reads the status and finds this bit set, it must then read the Error Register to determine the type of error. This bit is reset when a new command is written into the command register.

COMMAND REGISTER

This write-only register is loaded with desired command:

7	6	5	4	3	2	1	0
C	O	M	M	A	N	D	

The command begins to execute immediately upon loading. This register should not be loaded while the Busy or CIP bits are set in the status register. The INTRQ, if set, will be cleared by a write to the command register.

INSTRUCTION SET

The WD1010 will execute six commands. Prior to loading the command register, the host must first set up the task file with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. Any subsequent writes to the command register will be ignored until execution is completed indicated by the resetting of the CIP bit in the status register.

COMMAND SUMMARY

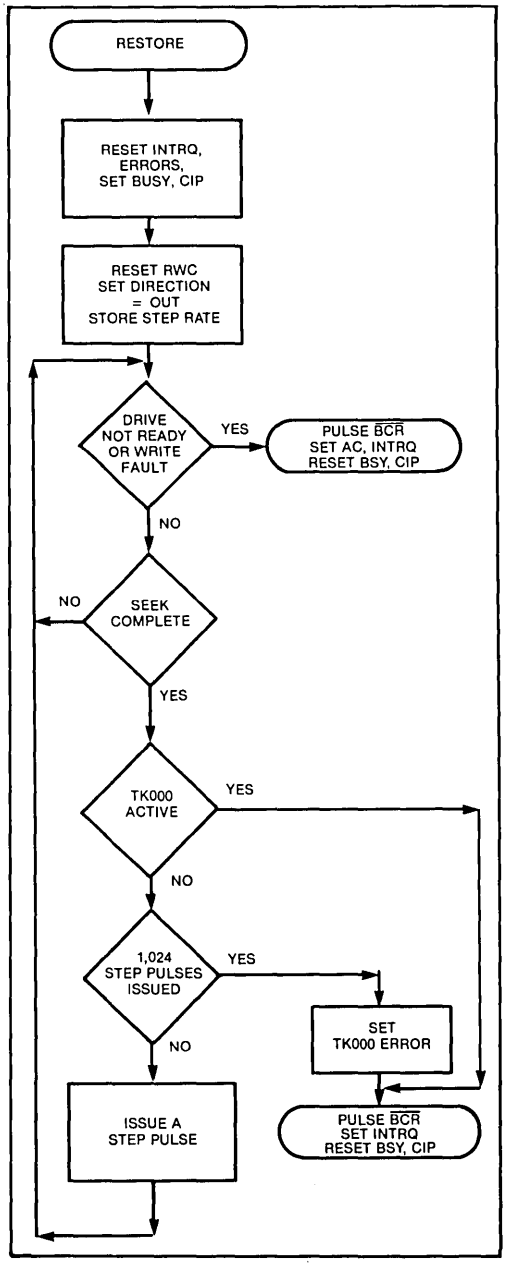
COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R_3	R_2	R_1	R_0
SEEK	0	1	1	1	R_3	R_2	R_1	R_0
READ SECTOR	0	0	1	0	I	M	0	T
WRITE SECTOR	0	0	1	1	0	M	0	T
SCAN ID	0	1	0	0	0	0	0	T
WRITE FORMAT	0	1	0	1	0	0	0	0

R_3-R_0 Rate Field
For 5 MHz WCLK:
R_3-R_0 = 0000 - 35 μs.
0001 - .5 ms.
0010 - 1.0 ms.
0011 - 1.5 ms.
0100 - 2.0 ms.
0101 - 2.5 ms.
0110 - 3.0 ms.
0111 - 3.5 ms.
1000 - 4.0 ms.
1001 - 4.5 ms.
1010 - 5.0 ms.
1011 - 5.5 ms.
1100 - 6.0 ms.
1101 - 6.5 ms.
1110 - 7.0 ms.
1111 - 7.5 ms.

Bit 0, ("T") Read Sector, Write Sector Commands
T = 0 Enable retries
T = 1 Disable retries

M = Multiple Sector Flag
M = 0 Transfer 1 sector
M = 1 Transfer multiple sectors

I = Interrupt Enable
I = 0 Interrupt at BDRQ time
I = 1 Interrupt at end of command



RESTORE COMMAND

The restore command is usually used on a power-up condition. The actual stepping rate used for the restore is determined by Seek Complete time. A step pulse is issued and the WD1010-05 waits for a rising edge on the seek complete line before issuing the next pulse. If 10 index pulses are received without a rising edge of seek complete, the WD1010 will switch to sensing the level of the SC line. If after 1,024 stepping pulses, the TK000 lines do not go active, the WD1010-05 will set the Track Zero error bit in the error register and terminate with an INTRQ. An interrupt will also occur if the write fault goes active or the DRDY goes inactive during execution.

The rate field specified (R3-R0) is stored in an internal register for future use in commands with implied seeks.

SEEK COMMAND

Since except for the SCAN ID all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The actual step rate used is taken from the rate field, which is also stored in an internal register for future use. If DRDY goes inactive or WF goes active, the command is terminated and an INTRQ is generated.

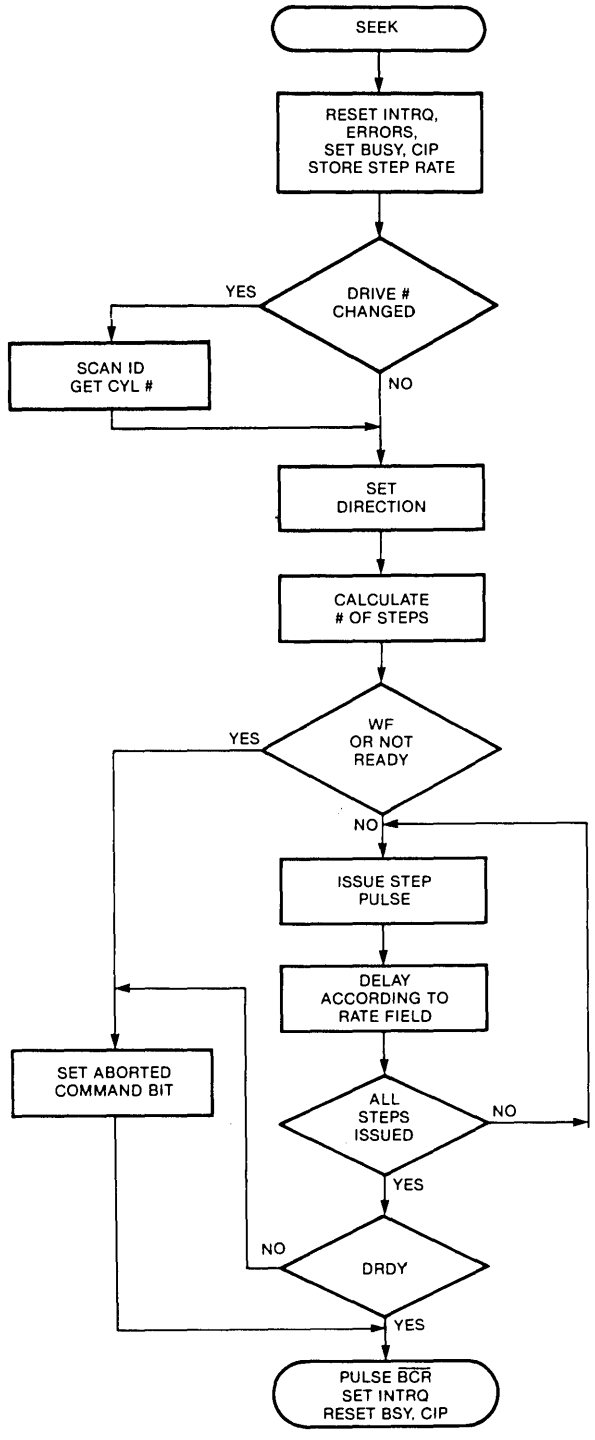
The direction and number of step pulses needed are calculated by comparing the contents of the cylinder register high/low to the cylinder position number stored internally. After all steps have been issued, the internal cylinder position register is updated and the command is terminated. Seek complete is not checked at the beginning or end of the command.

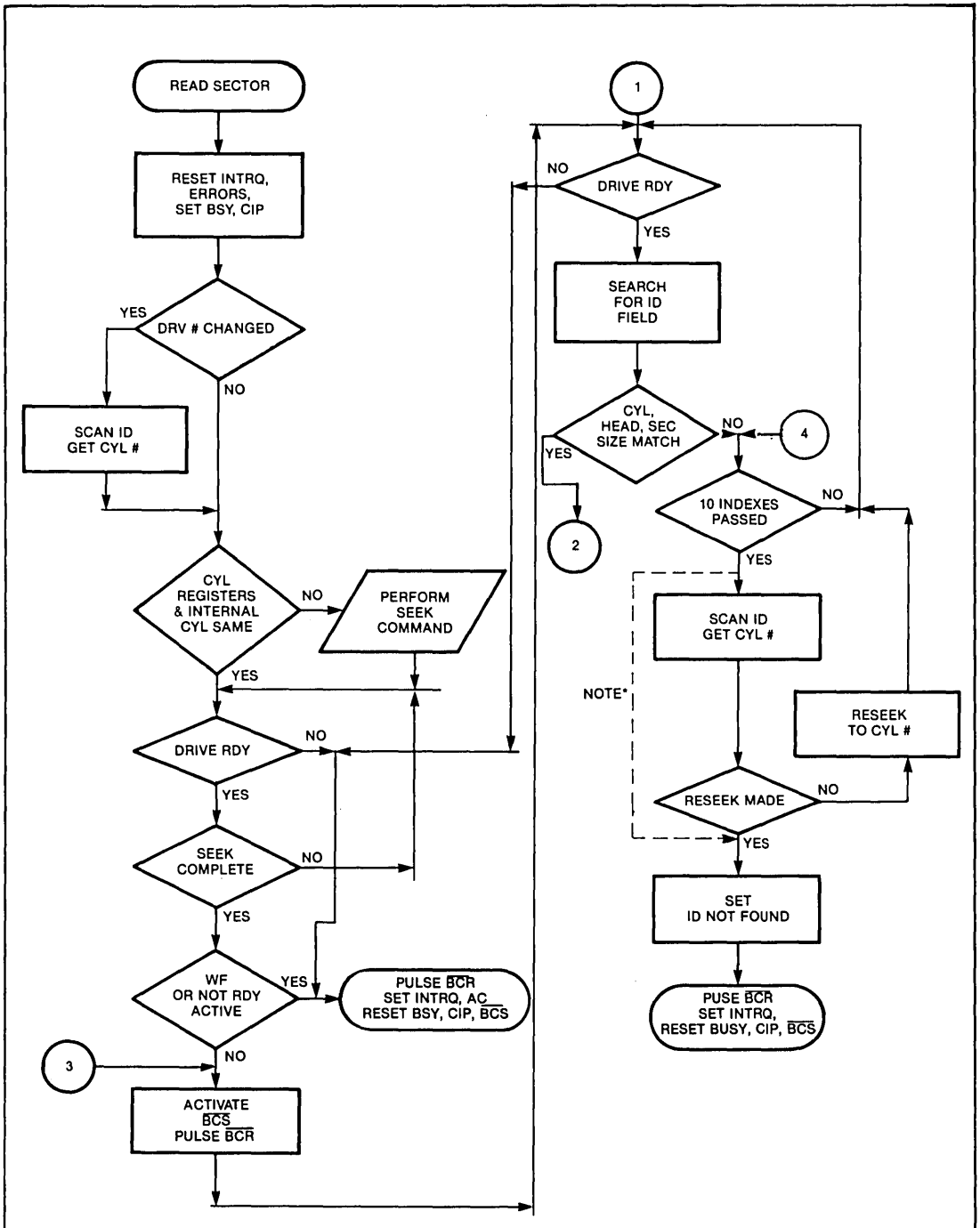
If an implied seek was performed, the WD1010-05 will wait until a rising edge of SC is received. If 10 revolutions occur before the rising edge of SC, the WD1010 will switch to level sensing of SC.

READ SECTOR

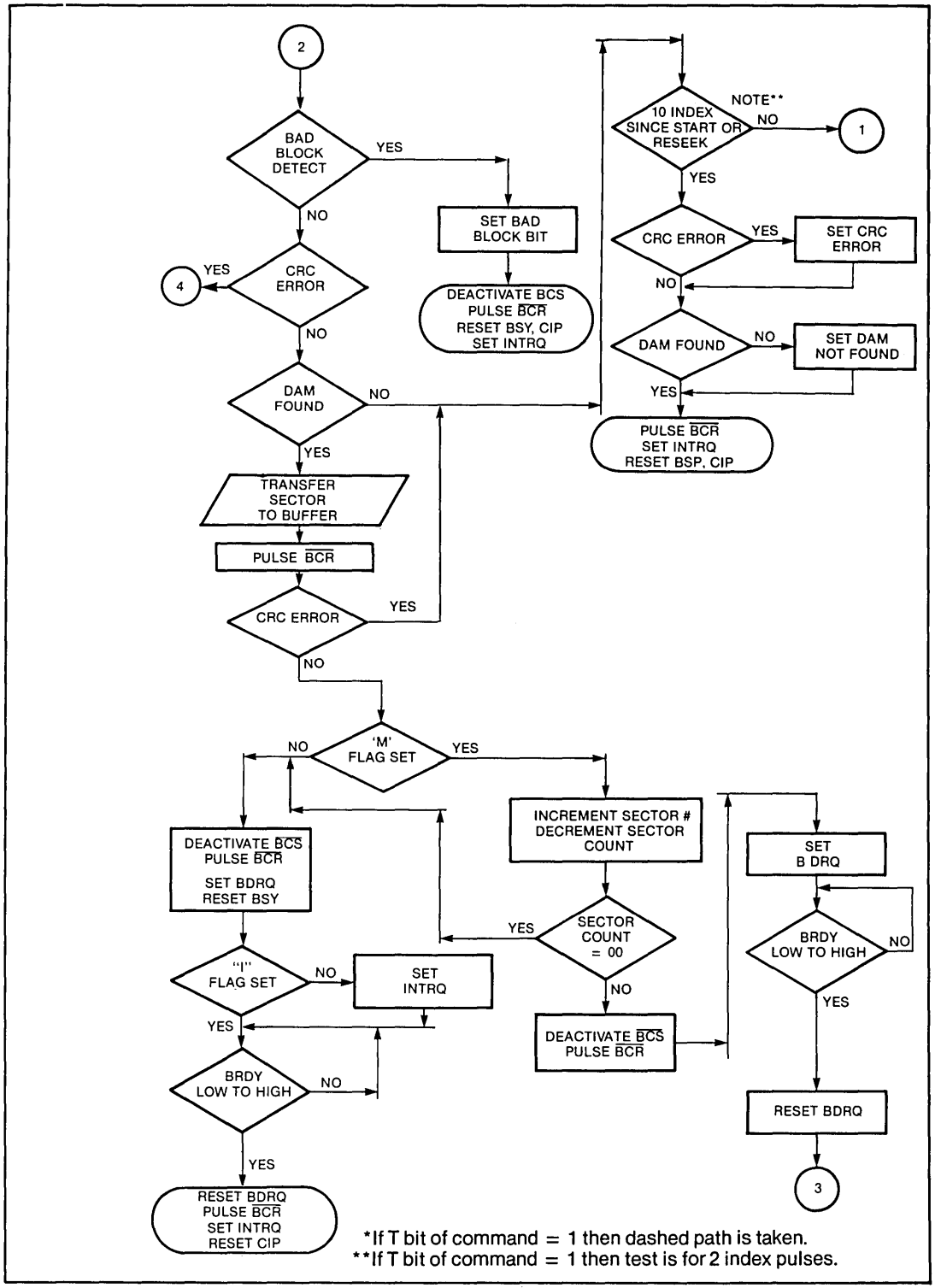
The read sector command is used to transfer one or more sectors of data from the disk to the sector buffer. Upon receipt of this command, the WD1010-05 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps calculation is performed and seek takes place. If an implied seek was performed, the WD1010-05 will search until a rising edge of seek complete is received. Write Fault and DRDY lines are checked throughout the command.

After seek complete is found to be true (with or without an implied seek), the search for an ID field occurs. The WD1010-05 must find an ID with the correct cylinder, head, sector size, and CRC within 10 revolutions if T bit of command is zero, and within 2 revolutions if T = 1; else the appropriate error bits will be set and the command terminated if T = 1. Both the Read and Write sector commands feature a "simulated completion" to ease programming. DRQ/BDRQ will be generated upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command. If T = 0, an automatic scan ID is performed to obtain cylinder position information and then, if necessary, a seek is performed. The search for the correct ID field is continued for 10 more disk rotations.


SEEK
RESET INTRQ, ERRORS, SET BUSY, CIP STORE STEP RATE
DRIVE # CHANGED
YES
NO
SCAN ID GET CYL #
SET DIRECTION
CALCULATE # OF STEPS
WF OR NOT READY
YES
NO
ISSUE STEP PULSE
DELAY ACCORDING TO RATE FIELD
SET ABORTED COMMAND BIT
ALL STEPS ISSUED
NO
YES
DRDY
NO
YES
PULSE BCR
SET INTRQ
RESET BSY, CIP



*If T bit of command = 1 then dashed path is taken after 2 index pulses.



*If T bit of command = 1 then dashed path is taken.
**If T bit of command = 1 then test is for 2 index pulses.

When the data address mark is found, the WD1010-05 is ready to transfer data to the buffer. After the sector data has been transferred, the I flag is checked. If the I flag is 0, the INTRQ is made active coincident with BDRQ, indicating a transfer of data is required by the host. If I = 1, the INTRQ will occur at the end of the command (i.e., after the buffer is unloaded by the host).

An optional M flag may be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count register is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD1010-05 decrements the sector count register and increments the sector number register. The next logical sector will be transferred, regardless of the interleave. Sectors are numbered at format time by a byte in the ID field.

For the WD1010 to make multiple sector transfers to the buffer, the BRDY line must be toggled low to high for each sector. The sector transfers will continue until the sector count register equals zero. If the sector count register is non-zero (indicating more sectors are to be transferred but the buffer is full), BDRQ will be made active and the host must unload the buffer. Once this occurs, the buffer will again be free to accept the next sector in this multiple sector read command.

When M = 0 (Single Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes BCR; sets $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Strobes BCR; sets $\overline{BCS}$ = 1 (Off).
(5)	1010:	Sets BDRQ = 1; sets DRQ flag.
(6)	1010:	If I bit = 1 then (9).
(7)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$).
(8)	1010:	Waits for BRDY then sets INTRQ = 1; End.
(9)	1010:	Sets INTRQ = 1.
(10)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$); End.

When M = 1 (Multiple Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes BCR; sets $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Decrements sector count register; increments sector number register.
(5)	1010:	Strobes BCR; sets $\overline{BCS}$ = 1 (Off).
(6)	1010:	Sets BDRQ = 1; DRQ flag = 1.
(7)	Host:	Reads out content of buffer (by $\overline{RE}$ strobes).
(8)	Buffer:	Indicates data has been transferred by asserting BRDY.
(9)	1010:	When BRDY is asserted, go to (11) if sector count = 0.
(10)	1010:	Go to Step (2).
(11)	1010:	Activates INTRQ.

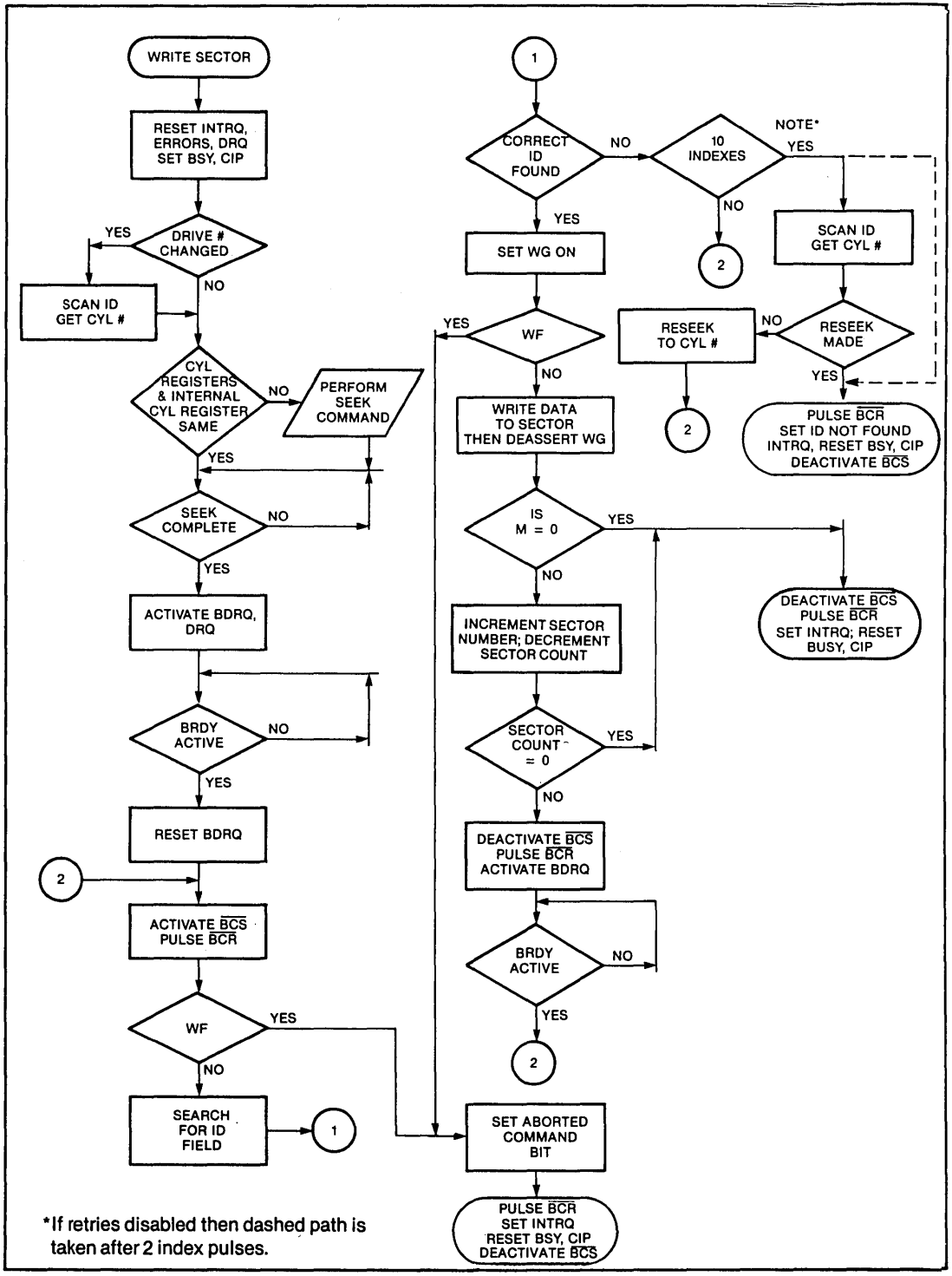
WRITE SECTOR

The write sector command is used to write one or more sectors of data to the disk. Upon receipt of this command, the WD1010-05 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps are calculated and a seek command takes place. Write fault and DRDY lines are checked throughout the command.

After Seek complete is found to be true (with or without an implied seek), the BDRQ signal is made active and the host proceeds to load the buffer. When the WD1010-05 senses the BRDY line going high, the ID field with the specified cylinder, head, and sector size is searched for. Once found, the write gate signal is raised and the data is written to the disk. It is necessary to resynchronize the write data due to the fact that a bit cell can extend from 295ns to 315ns during a write cycle. If retries are disabled and if the ID field cannot be found within 2 revolutions, the ID not found bit is set and the command is terminated.

If retries are enabled, and the ID field cannot be found within 10 revolutions, an automatic scan ID and seek commands are performed. The ID Not Found error bit is set if the ID field is not found after 10 more revolutions.

During a multiple sector write operation (M flag = 1), the sector number is incremented and the sector count register is decremented. If the BRDY lines is asserted after the first sector is read out of the buffer, the WD1010-05 will continue to read data out of the buffer for the next sector. If BRDY is inactive, the WD1010-05 will raise BRDQ and wait for the host to place more data in the buffer.


WRITE SECTOR
RESET INTRQ, ERRORS, DRQ SET BSY, CIP
DRIVE # CHANGED
YES
NO
SCAN ID GET CYL #
CYL REGISTERS & INTERNAL CYL REGISTER SAME
NO
PERFORM SEEK COMMAND
YES
SEEK COMPLETE
NO
YES
ACTIVATE BDRQ, DRQ
BRDY ACTIVE
NO
YES
RESET BDRQ
2
ACTIVATE BCS PULSE BCR
WF
YES
NO
SEARCH FOR ID FIELD
1
1
CORRECT ID FOUND
NO
10 INDEXES
NOTE*
YES
NO
2
SCAN ID GET CYL #
YES
SET WG ON
YES
WF
NO
RESEEK TO CYL #
NO
RESEEK MADE
YES
2
PULSE BCR SET ID NOT FOUND INTRQ, RESET BSY, CIP DEACTIVATE BCS
WRITE DATA TO SECTOR THEN DEASSERT WG
IS M = 0
YES
NO
DEACTIVATE BCS PULSE BCR SET INTRQ; RESET BUSY, CIP
INCREMENT SECTOR NUMBER; DECREMENT SECTOR COUNT
SECTOR COUNT = 0
YES
NO
DEACTIVATE BCS PULSE BCR ACTIVATE BDRQ
BRDY ACTIVE
NO
YES
2
SET ABORTED COMMAND BIT
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
*If retries disabled then dashed path is taken after 2 index pulses.

In summary then, the write sector operation is as follows:

(1)	Host:	Sets up parameters; issues write sector command.
(2)	1010:	Sets BDRQ = 1, DRQ flag = 1.
(3)	Host:	Loads buffer with data (by $\overline{WE}$ strobes).
(4)	1010:	Waits for BRDY = low to high.
(5)	1010:	Finds specified ID field, write out sector.
(6)	1010:	If M = 0, then interrupt; End.
(7)	1010:	Increments sector number, decrements sector count.
(8)	1010:	If sector count = 0, then interrupt; End.
(9)	1010:	Go to (2).

SCAN ID

The scan ID command is used to update the head, sector size, sector number and cylinder registers.

The ready and write fault lines are checked throughout the command. When the first ID field is encountered, the ID information is loaded into the SDH, cylinder, and sector number registers. The internal cylinder position register is also updated. If a bad block is detected, the bad block bit will also be set. CRC is checked and if an error is found, the WD1010-05 will retry up to 10 revolutions to find an error-free ID field. There is no implied seek with this command and the buffer is left undisturbed.

FORMAT

The format command is used to format one track using the task file and the sector buffer. During this command, the sector buffer is used for additional parameter information instead of sector data. Shown in Figure 7 is the contents of the sector buffer for a 32 sector track format with an interleave factor of two. Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. A 00 is normal; an 80 hex indicates a bad block mark for that sector. In the example of Figure 7, sector 04 will get a bad block mark recorded.

The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its purpose is only to generate a BRDY to tell the WD1010-05 to begin formatting the track.

An implied seek is also in effect on this command. As in other commands, if the drive number has changed, an ID field will be scanned for cylinder position information before the implied seek is performed. If no ID field can be read (because the track had been erased or because an incompatible format had been used), an IDNF error will result and the Format command will be aborted. This can be avoided by issuing a Restore command before formatting.

The sector count register is used to hold the total number of sectors to be formatted, while the sector number register holds the number of bytes minus 3 to be used for Gap 1 and Gap 3. For instance, if the sector count register value is 2 and the sector number register value is 0, then 2 sectors are written and 3 bytes of 4E hex are written for Gap 1 and Gap 3. The data fields are filled with FF hex, and CRC is automatically generated and appended. The sector extension bit of the SDH register should not be set. After the last sector is written, 4E hex is filled until index.

The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining

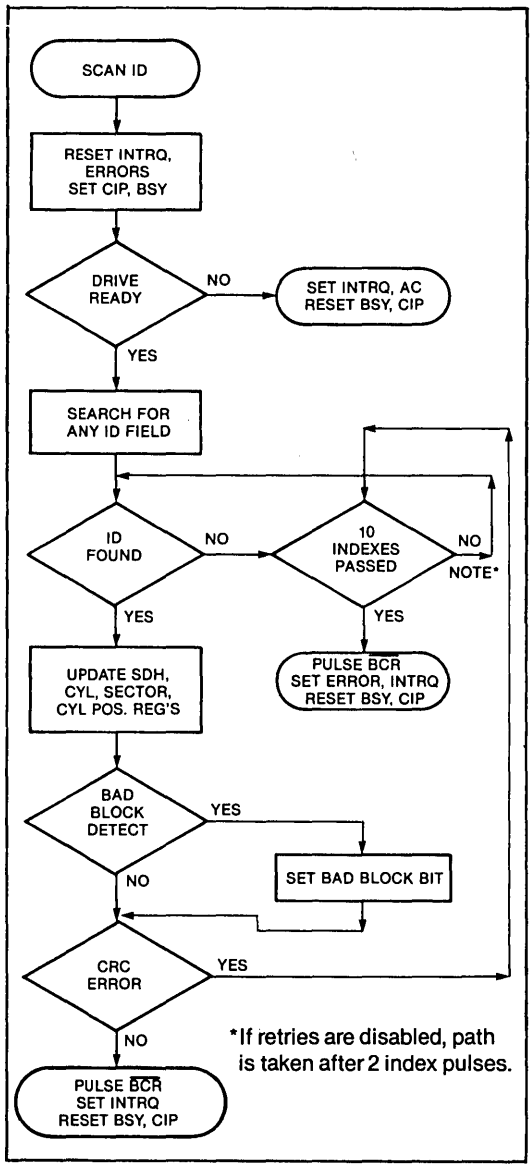
	DATA							
ADDR	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
:				:				
:				:				
F0	FF	FF	FF	FF	FF	FF	FF	FF

FIGURE 7.
FORMAT COMMAND BUFFER CONTENTS

the minimum Gap 3 value is:

Gap 3 = 2*M*S + K + E
M = motor speed variation (e.g., .03 for ± 3%)
S = sector length in bytes
K = 25 for interleave factor of 1
K = 0 for any other interleave factor
E = 7 if the sector is to be extended

Like all commands, a write fault or not ready condition will terminate the command. Figure 8 shows the format that the WD1010-05 will write on the Disk.



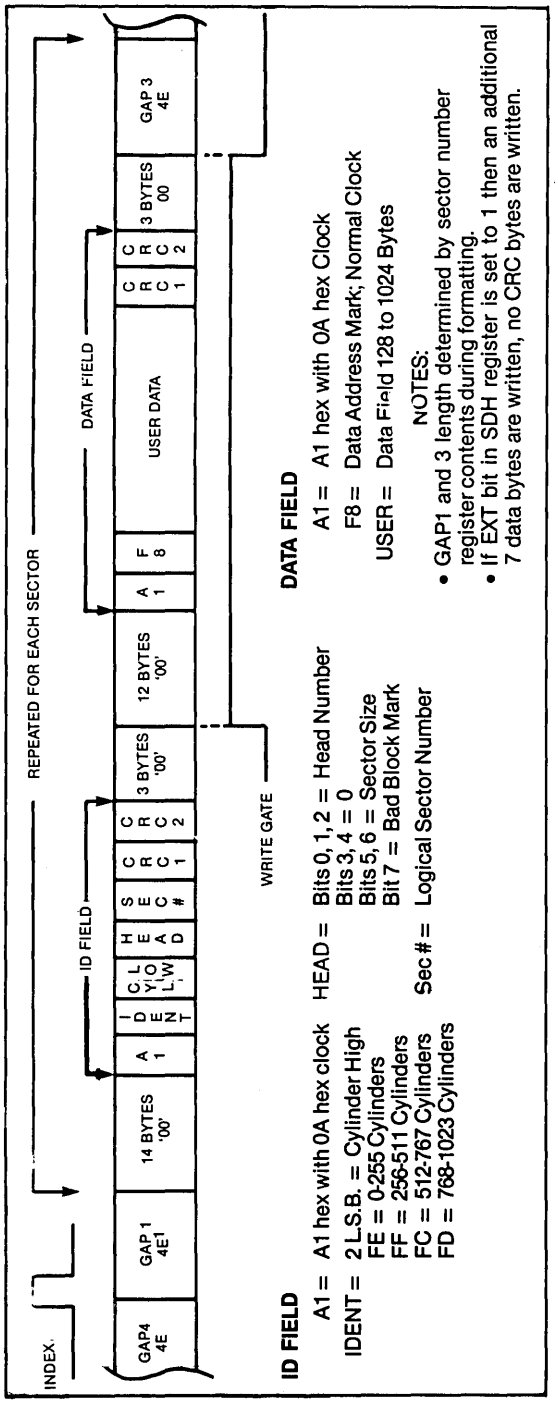
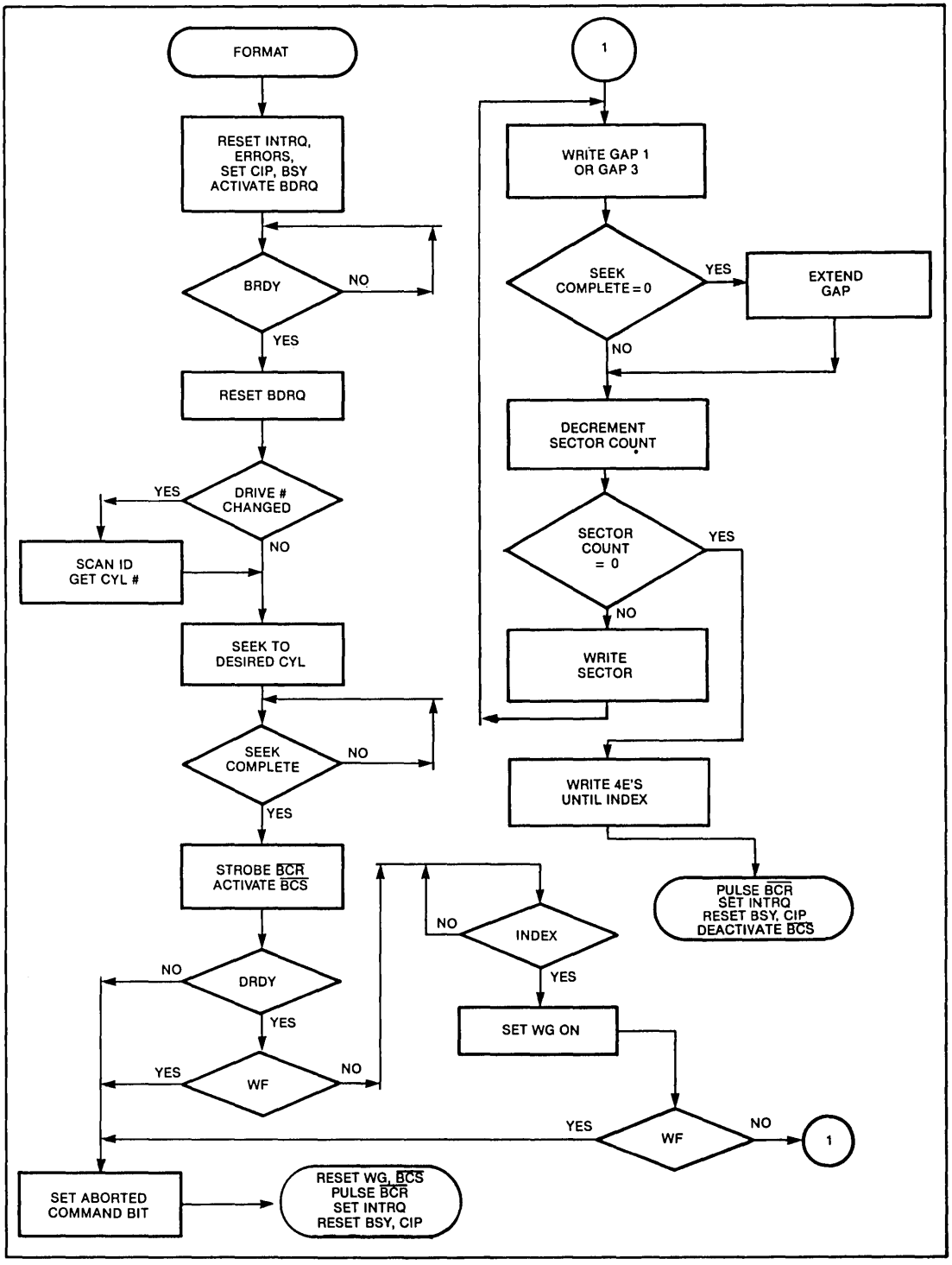


FIGURE 8.
FORMAT


FORMAT
RESET INTRQ, ERRORS, SET CIP, BSY ACTIVATE BDRQ
BRDY
NO
YES
RESET BDRQ
DRIVE # CHANGED
YES
NO
SCAN ID GET CYL #
SEEK TO DESIRED CYL
SEEK COMPLETE
NO
YES
STROBE BCR ACTIVATE BCS
DRDY
NO
YES
WF
YES
NO
SET ABORTED COMMAND BIT
RESET WG, BCS PULSE BCR SET INTRQ RESET BSY, CIP
1
WRITE GAP 1 OR GAP 3
SEEK COMPLETE = 0
YES
EXTEND GAP
NO
DECREMENT SECTOR COUNT
SECTOR COUNT = 0
YES
NO
WRITE SECTOR
WRITE 4E'S UNTIL INDEX
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
INDEX
NO
YES
SET WG ON
WF
YES
NO
1

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

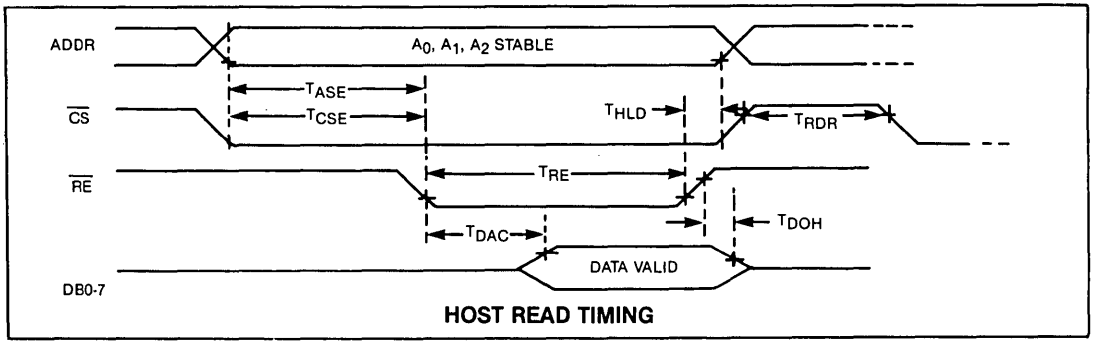
V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with
respect to V_{SS} .....-0.5V to +7.0V
Operating Temperature .....0°C to 70°C
Storage Temperature .....-55°C to +125°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ±.25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Drain)		±10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = - 100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6mA
V_{OL}	Output Low Voltage(Pins 21-23)		0.45	V	IO = 4.8mA See Note 10
I_{CC}	Supply Current		200	mA	All Outputs Open
	For Pins 25, 34, 39:				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise and Fall Time		30	nsec	.9V to 4.2V points
C_{IN}	Input Capacitance		15	pF	

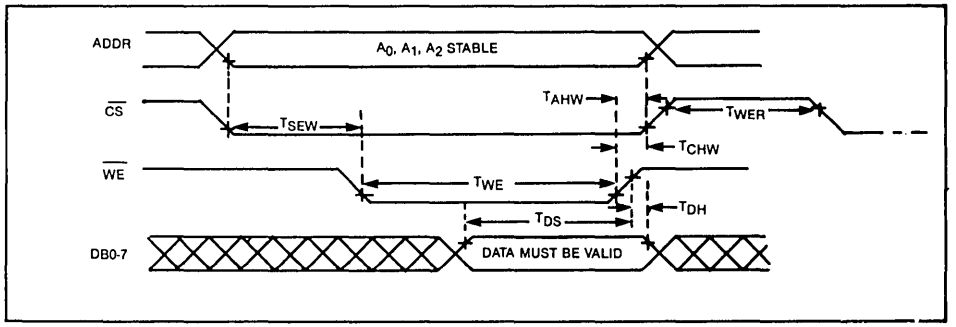
AC Timing Characteristics T_A = 0°C to 50°C; V_{SS} = 0V, V_{CC} = +5V ±.25V



HOST READ TIMING

HOST READ TIMING WD1010-05 WC = 5 MHZ

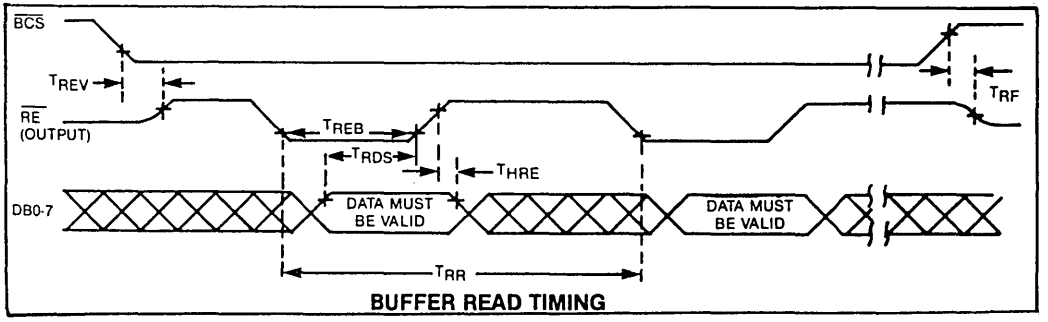
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITION
T_{ASE}	ADDR Setup to $\overline{RE}$	100		nsec	
T_{DAC}	Data Valid from $\overline{RE}$		375	nsec	
T_{RE}	Read Enable Pulse Width	.4	10	μsec	
T_{DOH}	Data Hold from $\overline{RE}$	20	200	nsec	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		nsec	
T_{RDR}	Read Recovery Time	300		nsec	
T_{CSE}	$\overline{CS}$ Setup to $\overline{RE}$	0		nsec	See Note 8



HOST WRITE TIMING

HOST WRITING TIMING WD1010-05

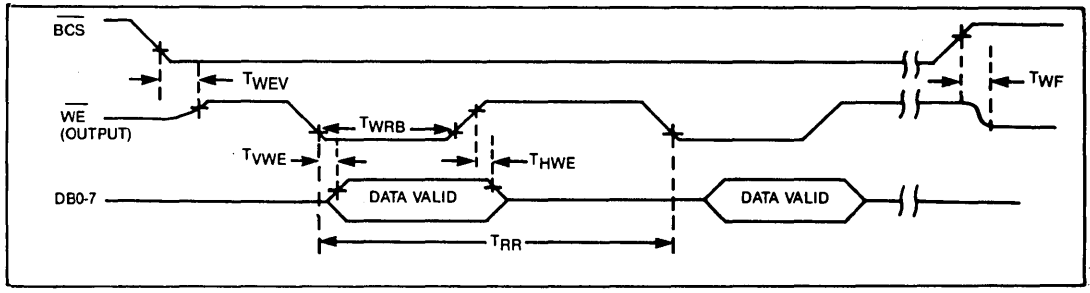
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITION
T_{SEW}	ADDR, $\overline{CS}$ Setup to $\overline{WE}$	0	10	μsec	
T_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	μsec	
T_{WE}	Write Enable Pulse Width	.2	10	μsec	
T_{DH}	Data Bus Hold from $\overline{WE}$	10		nsec	
T_{AHW}	ADDR Hold from $\overline{WE}$	30		nsec	
T_{WER}	Write Recovery Time	1.0		μsec	See Note 1
T_{CHW}	$\overline{CS}$ Hold Time from $\overline{WE}$	0			See Note 9



BUFFER READ TIMING

BUFFER READ TIMING (WRITE SECTOR CMD) WD1010-05 WC = 5MHZ

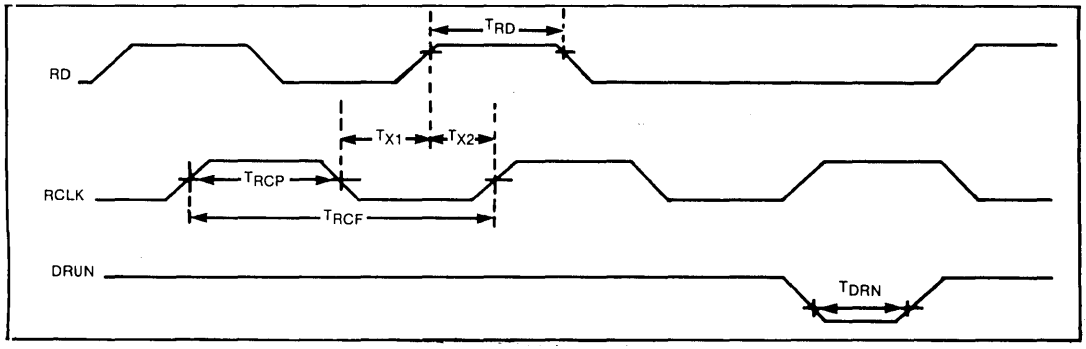
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	nsec	C_L = 50 pf
T_{REB}	$\overline{RE}$ Output Pulse Width	300	400	500	nsec	See Note 4
T_{RDS}	Data Setup to $\overline{RE}$	140			nsec	
T_{RR}	$\overline{RE}$ Repetition Rate	1.2	1.6	2.0	μsec	
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	nsec	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			nsec	



BUFFER WRITE TIMING

BUFFER WRITE TIMING (READ SECTOR CMD) WD1010-05 WC = 5 MHZ

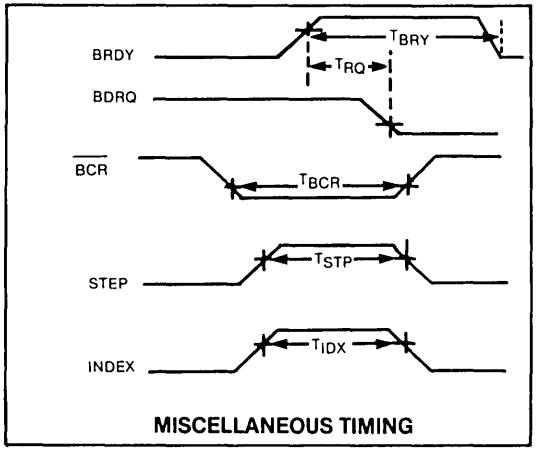
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	nsec	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	nsec	See Note 4
T_{VWE}	Data Valid from $\overline{WE}$			150	nsec	
T_{HWE}	Data Hold from $\overline{WE}$	60			nsec	
T_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	μsec	See Note 2
T_{WF}	$\overline{WE}$ Float from $\overline{BCS}$	15		100	nsec	C_L = 50 pf



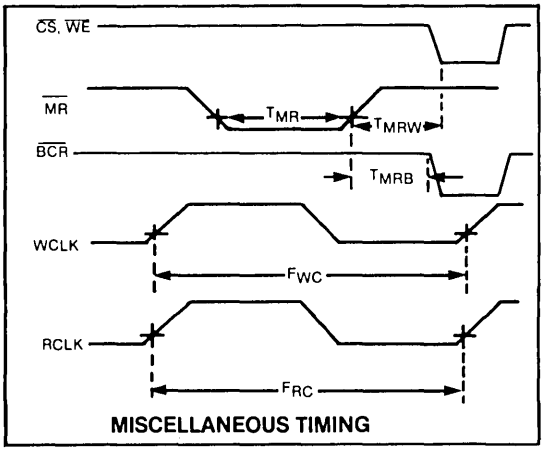
READ DATA TIMING

READ DATA TIMING WD1010-05 WC = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	95		2000	nsec	50% Duty Cycle
T_{X1}	RD from RCLK Transition	0		T_{RCP}	nsec	
T_{X2}	RD to RCLK Transition	20		T_{RCP}	nsec	
T_{RD}	RD Pulse Width	40		T_{RCP}	nsec	
T_{DRN}	DRUN Pulse Width	30			nsec	
T_{RCF}	RCLK Frequency	.250		5.25	MHz	See Note 6



MISCELLANEOUS TIMING

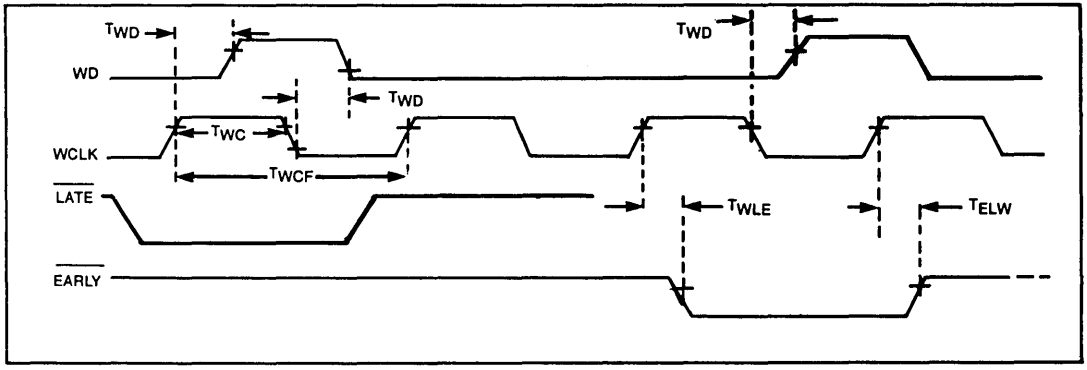


MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RQ}	BDRQ Reset from BRDY	40		200	nsec	
T_{BCR}	Buffer Counter Reset Pulse Width	1.4	1.6	1.8	μsec	See Note 2
T_{STP}	Step Pulse Width	8.3	8.4	8.7	μsec	See Note 2
T_{IDX}	Index Pulse Width	500			nsec	
T_{MR}	Master Reset Pulse Width	24			WC	See Note 3
F_{WC}(-05)	Write Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle
F_{RC}(-05)	Read Clock Frequency	.25	5.0	5.25	MHz	See Note 6
T_{BRY}	BRDY Pulse Width	800			nsec	See Note 5
T_{MRB}	$\overline{MR}$ Trailing to $\overline{BCR}$	1.6	3.2	6.4	μsec	See Note 2
T_{MRW}	$\overline{MR}$ Trailing to Host Write	6.4			μsec	See Note 2

NOTES:
1. AC timing measured at V_{OH} = 2.0V, V_{OL} = 0.8V, C_L = 50 pf.
2. Based on WCLK = 5.0 MHz.
3. 24 WCLK periods (4.8 μsec at 5.0 MHz).
4. 2 WCLK ± 100 nsec.
5. To drive a DMA controller, BRDY must be >4 μsec or a spurious BDRQ pulse may exist for up to 4 μsec after rising edge of BRDY.
6. T_{RCF} = T_{WCF} ± 15%.
7. 2 WCLK ± 50 nsec.
8. $\overline{RE}$ may precede $\overline{CS}$ if $\overline{CS}$ plus $\overline{RE}$ meets the TRE width.
9. $\overline{WE}$ may precede $\overline{CS}$ if $\overline{CS}$ plus $\overline{WE}$ meets the TWE width.
10. Pins 21-23 should be loaded with a 1K pull-up resistor.



WRITE DATA TIMING

WRITE DATA TIMING WD1010-05 WC = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	nsec	
T_{WD}	Propagation Delay WCLK to WD	10		65	nsec	
T_{WLE}	WCLK to Leading Early/Late	10		65	nsec	
T_{ELW}	WCLK to Trailing Early/Late	10		65	nsec	
T_{WCF}	WCLK Frequency	.250		5.25	MHz	See Note 6

FLEXIBLE CONTROLLER MATES WITH POPULAR WINCHESTER DRIVES

To take advantage of the growing demand for Seagate Technology-type 5 1/4-in. Winchester disk drives in personal computers, electronic work stations, and small-business systems, designers need an appropriate controller that is inexpensive. In fact, today's designs must implement the control link between a Host CPU and a disk drive at far lower cost than the drive itself. That requires a single-chip controller rather than discrete, gate-array-intensive circuits that take up valuable board space in ever smaller computer equipment.

Such a device is now available in the form of an LSI single-chip Winchester controller-formatter. The chip incorporates 80% of the circuitry required for Winchester control, eliminating between 50 and 75 SSI and MSI devices used in earlier designs.

A controller that claims Seagate compatibility must be sufficiently flexible to meet not only the company's original ST506 specifications, but also the various deviations from them. The basic specifications include a data rate of 5.0 Mbits/s and open-collector outputs and differential signal inputs for the separate control and data interface cables. The recording format is modified frequency modulation (MFM), but more importantly, the structure of the format defines both specific address-mark bytes and ID fields. These are fixed specifications, but manufacturers of Seagate-type drives sometimes make other changes. For example, the track density on high-capacity drives may be greater than that in the original ST506 specification. Also, the number of sectors and bytes per sector on each cylinder can vary according to the application. In each case, a compatible controller must be able to handle the original specifications plus the deviations.

The ST506 interface is a spinoff of the Shugart Associates SA1000 drive, first introduced in 1979. Two important differences between the interfaces are the data rates and a timing-clock differential signal on the SA1000. The latter operates at 4.34 Mbits/s vs 5 Mbits/s for the ST506, but the remaining signals have enough similarity to permit a single controller design to run either an 8-in. SA1000 drive or the 5 1/4-in. ST506 drive. The advantage of the WD1010 Winchester controller-formatter is that it works with either and with other manufacturers' variations as well.

Operation of the drive begins when a Host processor initiates a command after first loading a set of internal task registers called the task file. Information such as cylinder, sector, and head number is written to these registers, which are selected by address lines. The memory-mapped register scheme allows individual accesses to each register. Thus, the Host need not waste valuable time reading all the registers to obtain a specific parameter.

The WD1010, which comes in a 40-pin DIP or 44-pin QSM, is run by an internal microcontroller – a PLA (programmable logic array) serving as a state machine (Fig. 1). This logic controls the flow of data throughout the chip, recognizes and processes commands, and formats the data.

WRITING AND READING DATA

During a write operation, parallel data is read from the data bus and written to a specific sector. But first the cylinder and sector must be located on the requested disk drive. The WD1010's microcontroller accesses its internal cylinder-position data and compares it with the requested cylinder number. If necessary, a seek is performed automatically to position the head assembly over the desired cylinder.

If the drive requested is changed before a Seek Command is executed, the WD1010 enables its read logic and searches for an ID field on the currently selected drive. Then it reads the cylinder number for the new ID field and determines whether to seek in or out to find the requested cylinder. This so-called implied seek is a feature of all commands (see "Macro Commands Provide Multiple Options").

After the WD1010 finds an ID field that matches the cylinder, head, sector, sector size and CRC (cyclic redundancy check) value, it writes a field of 0s and a new address mark – later these two fields will be used for synchronization during a read operation. The chip then reads parallel data in from the data bus, serializes it, and converts it into the MFM format. Next, a new CRC value is calculated for the incoming data and is appended to the data field (after the last byte). If the original command specifies multiple sectors, the next logical sector must be searched for and the process repeated. After the last sector is written, the WD1010 gives the bus back to the Host and waits for the next command.

Although the chip does not generate an error correction signal, an optional command bit can be set to disable cyclic redundancy checks of the data field. The sector is extended by seven bytes to allow the Host to write its 56-bit error detection and correction code. Later, during a read operation, these seven bytes are transferred back to the Host to permit it to identify a syndrome and correct any errors that were encountered. For systems that require such operations, the WD1014 error detection and correction and

WD1015 buffer controller chips are available.

Reading is similar to writing except that data is sent out on the data bus and written into the sector buffer at the Host. MFM data is entered on the RD pin along with a synchronous clock (RCLK) generated from an external data separator (Figure 2).

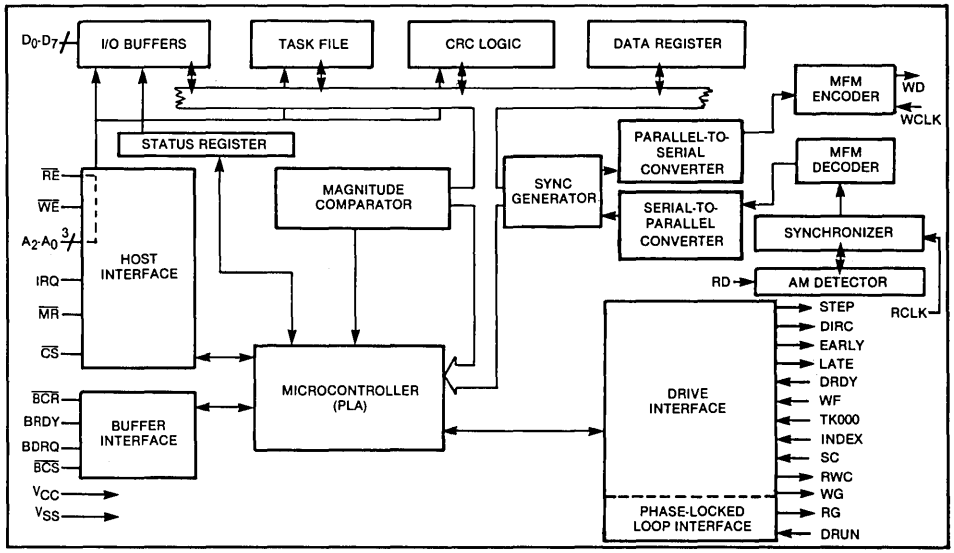


Figure 1.

The architecture of the WD1010 Winchester controller-formatter chip is designed to reduce a Host processor's overhead burden. An internal microcontroller (PLA) manages data flow, incoming commands, and formatting.

Since the data rate is relatively high, the data separator must instruct the controller to lock on to the incoming data stream only during a field of 1s and 0s. A Data Run (DRUN) signal to the WD1010 indicates such an occurrence. When DRUN is active, the WD1010 counts off 16 bits – 2 byte time – sets the Read Gate (RG) signal, and starts to search the data stream for an address mark.

IMPLEMENTING THE PRECOMPENSATION ALGORITHM				
ALREADY SENT		SENDING	TO BE SENT	SHIFT REQUIRED
X	1	1	0	Early
X	0	1	1	Late
0	0	0	1	Early
1	0	0	0	Late

NOTE: All other patterns produce no shift.

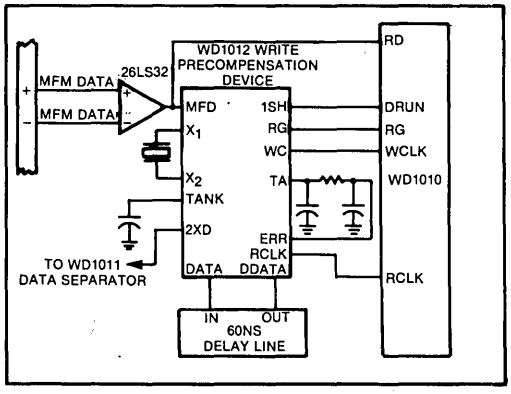


Figure 2.

A separate IC – the WD1012 – performs the data separation for the WD1010. The data separator sends a DRUN signal to the controller when it encounters a data field (1s and 0s).

An address mark is a unique pattern of clock and data bits that does not appear in any place that normal MFM data appears. If an address mark is not detected within nine bytes or if a non-0 pattern is detected within nine bytes, RG is turned off and the search is repeated. Since the data fields within sectors can contain 0s or all 1s, the DRUN algorithm is also triggered in these cases. But the address mark will not be detected, preventing erroneous data from being transferred.

After the ID field is compared and verified, a search begins for the address mark. Resynchronization occurs and the data is transferred to an internal MFM-to-NRZ converter. Data is then shifted through a double-buffered shift register and placed on the data bus for loading to the buffer. Either the cyclic redundancy code at the end of the data field is checked or the error detection and correction bytes are transferred in parallel to the host, depending on which option is used. Then the host processor can read the data from its local buffer.

Like all magnetic recording media, Winchester disks are not immune to the effects of bit shifts at high recording densities. The WD1010 uses an algorithm that informs external delay circuits when to shift outgoing data. A register within the task file specifies which cylinder receives reduced write current and if precompensation is needed. Typically, both occur on the same cylinder about half way down the disk surface.

The WD1010's precompensation signals are called $\overline{\text{Early}}$ and Late. Depending on the bit pattern leaving the device, data will be shifted early, late, or not at all. The WD1011 data separator implements the precompensation delay network (Figure 2).

Since the $\overline{\text{Early}}$ signal and the current data (or clock) bits leaving the WD1010 have already occurred, the WD1011 performs no delay function on $\overline{\text{Early}}$. If both $\overline{\text{Early}}$ and Late are inactive, the WD1011 inserts a 12-ns delay; if only Late is active, it inserts a 24-ns delay. The result is a ± 12-ns shift of the data from its nominal position. An inactive Reduced Write Current (RWC) signal from the WD1010 disables the WD1011. The WD1010 then furnishes precompensation signals independent of current cylinder position.

INTERFACING WITH CABLES AND BUSES

The remaining function on the drive side is to provide sufficient buffers to drive the cables between the chip and the interface connectors. Single-ended open-collector signals are used for the control cable, and differential receiver-drivers are used for the data cable (Figure 3). Each line must have such buffers, since the controller is designed to drive one TTL load on all inputs and outputs.

At a 5-Mbit/s data transfer rate to the host interface, a byte of data must be read every 1.6 μs – in 8-bit parallel form. Few microprocessors can access a port and check status within this period. Consequently, a design objective of the WD1010 is compatibility with a programmed I/O environment, as well as the support of off-line error detection and correction. Moreover, the chip can transfer multiple sectors on one command. To achieve such performance within the constraints of a 40-pin package, the WD1010 relies on a unique approach to the traditional peripheral interface.

Three modes of communication can exist at the host interface: between the host and the WD1010, between the host and the buffer, and between the WD1010 and the buffer. For the host-WD1010 communication the

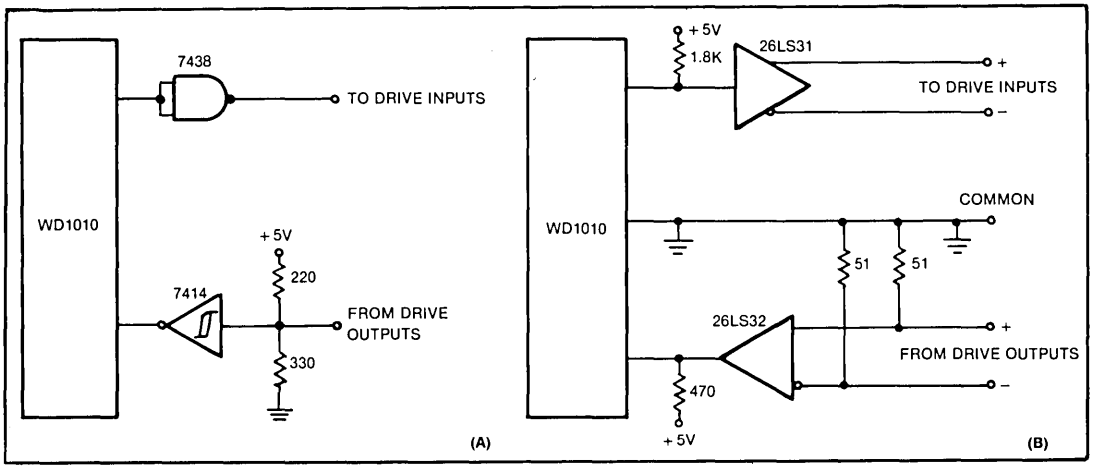


Figure 3.

Buffering circuits from the WD1010 to the control cable (A) and the data cable (B) must be used because the controller has a rather limited drive capability (one TTL load each on inputs and outputs).

chip, like many microprocessors, talks over an 8-bit bi-directional bus, plus Read, Write and chip select lines (Figures 4,5). Three address lines access registers within the chip.

In host-buffer or WD1010-buffer communications (Figures 4,5), when the chip reads or writes to the buffer, the Buffer Chip Select ($\overline{BSC}$) line is pulled low. This signal should be used to disconnect the host data bus and Read and Write lines from the WD1010.

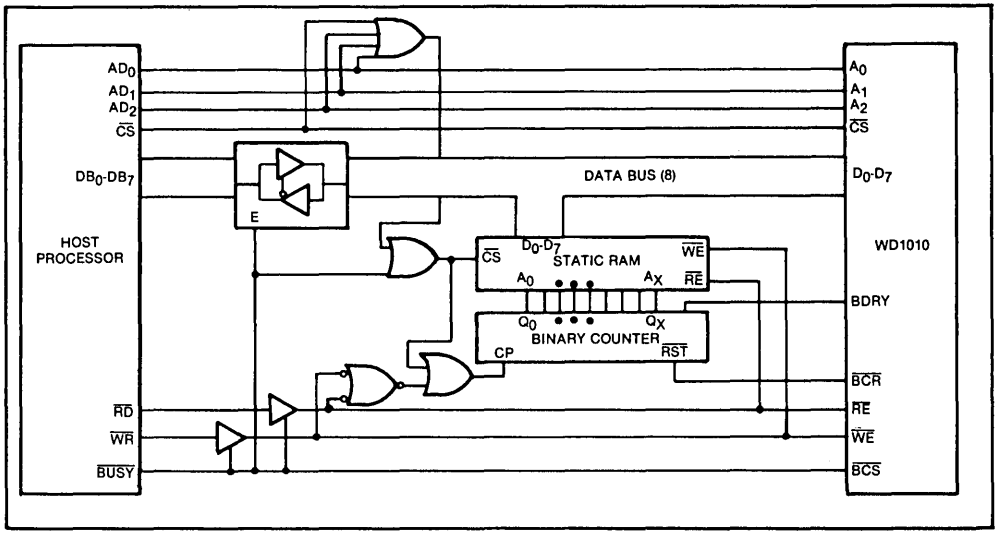


Figure 4.

Communications between a host and the WD1010 can be effected with the static RAM and binary counter circuitry shown in Figure 4. These devices form a sector buffer that stores data sent from the host or the controller. This hardware handles both read and write operations on multiple sectors.

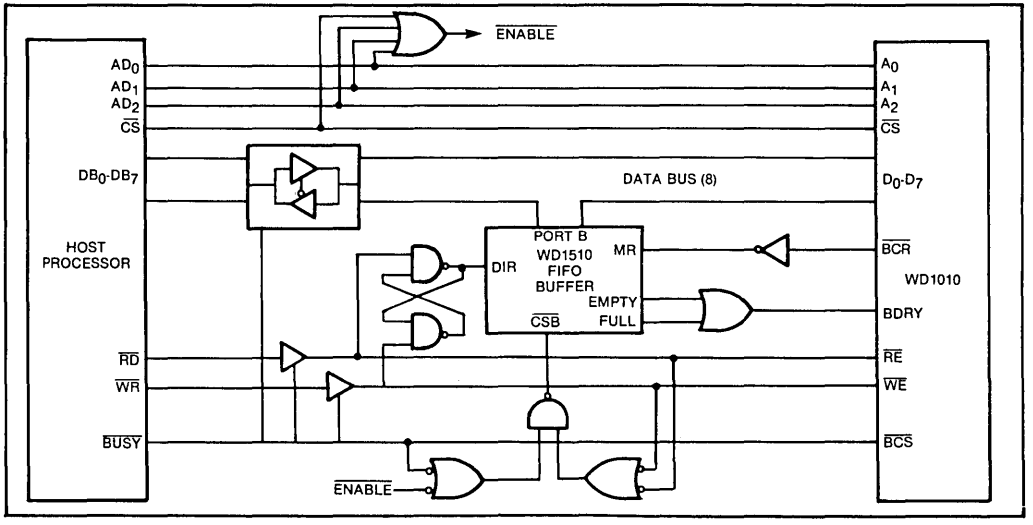


Figure 5.

A variation on the circuit of Figure 4. uses a WD1510 FIFO buffer to replace the counter-RAM circuitry. The scheme works well at high throughput rates since the buffer need not be filled to transfer data supplied by the WD1010 to the host.

The Read ($\overline{RE}$) and Write ($\overline{WR}$) lines become outputs from the WD1010 and are strobed as each byte is placed on the bus.

The sector buffer in Figure 4 is implemented with a binary counter and a static RAM. With each $\overline{RE}$ or $\overline{WE}$ probe, the counter is incremented so that the following byte can be read from or written to the next sequential location in the RAM. After all memory locations are written to, a carry signal from the counter goes to the Buffer Ready (BRDY) line of the WD1010. This signal informs the controller that the counter has rolled over and that the buffer is either full or empty, depending on the command.

During multiple-sector transfers, the RAM can be as large as the available sectors on each cylinder. The controller continues to load the RAM with data when a sector is being read. When no more memory is available, BRDY signals the WD1010. The command will then pause, wait for the host to dump the memory, and then begin filling the RAM again. This scheme permits both read and write operations on multiple sectors.

Signals for host and buffer control include the Buffer Counter Reset (BCR) line, which is pulsed when BCS makes an active transition. BCR resets the binary counter before a read or write operation. Since address location 000 does not exist in the WD1010, a decoder can be used to make this address location enable the RAM and simulate a data register. For DMA applications, the Buffer Data Request (BRDQ) line is activated when data is available for host use.

Numerous other methods can be used with these same control signals. For example, a first-in, first-out buffer (Figure 5) can replace the counter-RAM. In this scheme, the host can dump data before the WD1010 fills the buffer. With sufficient throughput, the FIFO buffer need not have the storage capacity of an entire sector if the host can empty it quickly enough with a burst mode. In that case, the BRDY signal becomes the OR function of the Empty and Full signals from the FIFO buffer.

MACRO COMMANDS PROVIDE MULTIPLE OPTIONS

Each of the WD1010 Winchester controller-formatter's six macro commands contains several option flags. These flags allow the selection of stepping rates, multiple-sector transfers, and interrupt timing. The WD1010's task file contains additional options that are programmed before the command is actually issued. The operations of each command are as follows:

Restore causes the read/write head assembly to move to track 000. The stepping rate is determined by the state of Seek Complete (pin 32), which is activated by the drive to indicate its readiness. The stepping rate specified in the Restore Command is not actually used but retained internally for an implied track later on.

Activation of Seek causes a seek operation for any desired cylinder. The selected cylinder is loaded into the cylinder register. Then the controller decides which way to seek and how many steps to use. The Seek Complete line is not checked, making possible overlapping seek operations on several drives.

The actual transfer of data from the WD1010 to sector buffer is performed under the Read Sector command. This command also causes a search for the specified cylinder, drive, head, and sector. Multiple sectors are specified and enabled through the sector count register. If the multiple-option flag is set, the number of sectors specified are transferred to the buffer.

Data in the sector buffer is written on the disk under the Write Sector command. Like the Read Sector command, it specifies and enables multiple drives through the sector count register.

Both the Read and Write Sector commands will retry up to eight times before automatically performing a restore operation. After a restoration, the controller seeks out the marginal sector and tries to determine whether an error condition was caused by a mispositioning of the head or a problem in the actuator.

The Format command is used to initialize a track with ID fields, gaps, and all information necessary for subsequent read and write operations. The sector buffer plays a unique role in this command, since it provides information on error mapping and interleaving rather than data from a sector. The order in which each sector is to be recorded is specified in the buffer, together with information indicating whether a sector contains a bad block or an error flag. Gap sizes, number of sectors, and other information are specified in the task file to allow further control over the format. By incrementing the cylinder number register, an entire surface can be formatted by accessing just two registers.

THE WD1010'S MACRO COMMANDS

	CODE							
	7	6	5	4	3	2	1	0
Restore	0	0	0	1	R_3	R_2	R_1	R_0
Seek	0	1	1	1	R_3	R_2	R_1	R_0
Read Sector	0	0	1	0	1	M	0	0
Write Sector	0	0	1	1	0	M	0	0
Scan ID	0	1	0	0	0	0	0	0
Write Format	0	1	0	1	0	0	0	0

M = Multiple Sector Flag

M = 0 – transfer 1 sector
M = 1 – transfer multiple sectors

I = Interrupt Enable

I = 0 – interrupt at BDRQ time
I = 1 – interrupt at end of command

A MULTIPLE-DRIVE SYSTEM

For multiple drive-head configurations, the WD1010's sector-drive-head (SDH) register is decoded at address 110 to produce individual, latched drive-selection signals whenever the host writes to this address location. Binary head selection does not require a separate decoder, since one is located at the drive.

When the WD1010 senses a change in drive number, it automatically reads a cylinder. This takes place before the execution of the current command. The chip records the new cylinder number it has read and stores it internally as a reference for future seek operations on the current drive.

After the execution of any command, the WD1010 informs the host processor of any errors encountered during execution. On-board status and error registers report error conditons and signal status from the drive. To eliminate tedious error detection procedures, the host processor need only check the error bit in the status register to determine whether any bits are set in the error register.

Bit 0 of the status register is set if any of 5 bits in the 8-bit error register are set – bit 0 establishes the logical OR of the status register. Other error indicators include a Bad Block Detect bit, which is activated when an ID field contains a bad block mark, and an ID Not Found bit, which is set when the desired cylinder, head, sector, or size parameter is not found after 16 revolutions of the disk. The latter is also set if the data address mark of the data field is incorrect when a read is executed.

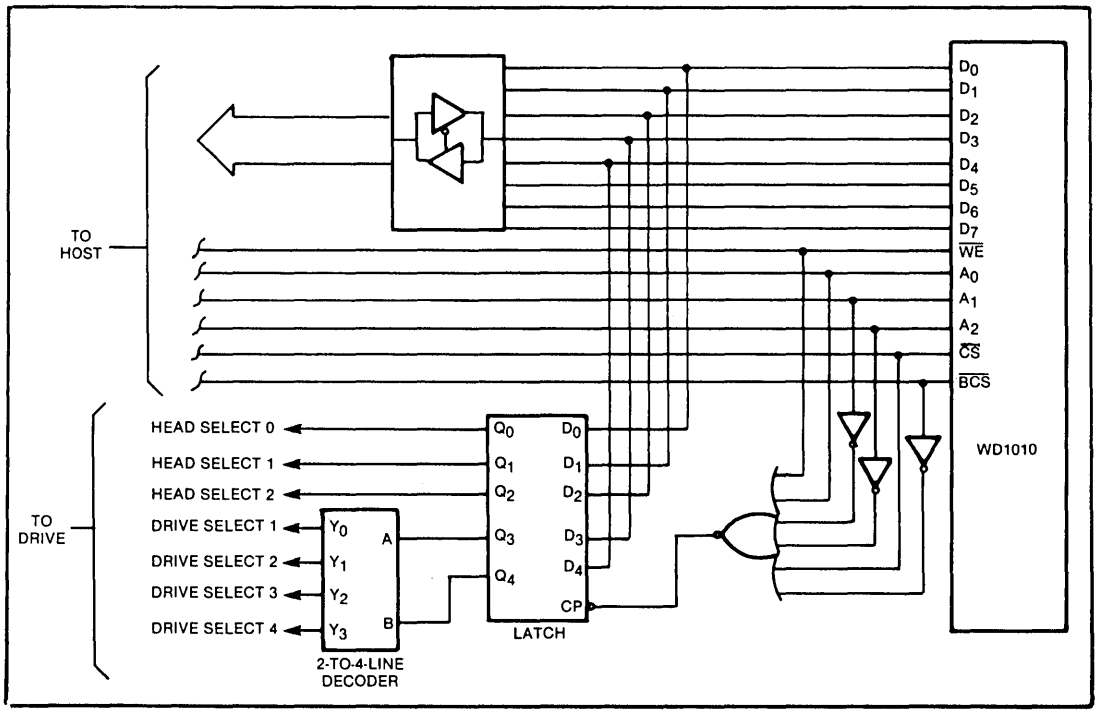


Figure 6.

Four Winchester drives can be controlled by the WD1010 using an external latch and a 2-to-4-line decoder. If the drive being accessed changes, the controller performs an automatic read operation. It records the cylinder number of the read for future seeks.

WD1050 SMD Controller/Formatter

FEATURES

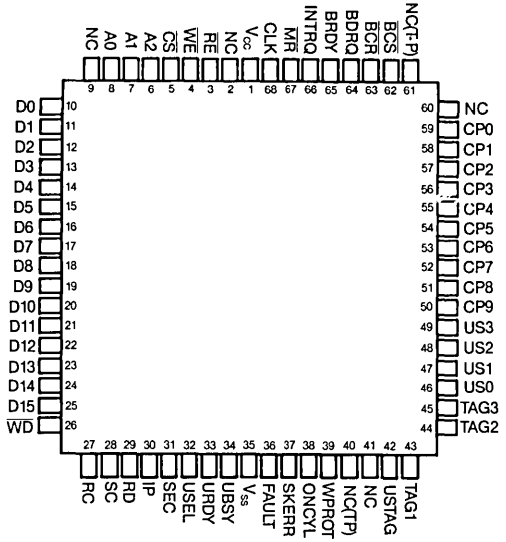
- 16 BIT HOST INTERFACE
- 9.677 MBITS/SEC DATA RATE
- SINGLE/MULTIPLE SECTOR TRANSFERS
- FIXED SECTOR FROMAT
- TTL COMPATIBLE INPUT/OUTPUT
- 68 PIN JEDEC TYPE C CHIP CARRIER PACKAGE
- COMPATIBLE WITH SMD, MMD, FHT, LMD, AND CMD FAMILIES
- SINGLE +5V SUPPLY

DESCRIPTION

The WD1050 SMD Controller/Formatter is an MOS/LSI device designed to interface an SMD compatible rigid disk drive to a Host processor. The device is compatible with all rigid disk drives adhering to Control Data Corporation's flat cable interface for SMD, MMD, FHT, FMD, LMD and CMD families (CDC specification 64712400 Rev H). It is TTL compatible on most inputs and outputs, with interface capability for 8 or 16 bit data buses.

The WD1050 contains a powerful set of Macro Commands for Read/Write and control functions. An internal 16 bit task file is used to process a selected command based upon parameter information in the file.

The WD1050 operates from a single +5V supply and is available in a 68 pin JEDEC Type C chip-carrier package.



PIN DESIGNATION

PIN NUMBER	NAME	SYMBOL	DESCRIPTION
1	V_{CC}	V_{CC}	+5V ±5% power supply input
2	NO CONNECTION	NC	
3	$\overline{\text{READ ENABLE}}$	$\overline{RE}$	Tri-state bi-directional line, used as an input when reading the task file and an output when the WD1050 is reading from the buffer.
4	$\overline{\text{WRITE ENABLE}}$	$\overline{WE}$	Tri-state bi-directional line used as an input when writing to the task file and an output when the WD1050 is writing to the buffer.
5	$\overline{\text{CHIP SELECT}}$	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals as inputs.
6-8	ADDRESS 0-2	A_0A_2	These three inputs select a task file register to receive/transmit data.
9	NO CONNECTION	NC	
10-25	DATA BUS 0-15	D0-D15	Sixteen bit bi-directional bus used for transfer of commands, status, and data.
26	$\overline{\text{WRITE DATA}}$	$\overline{WD}$	Open drain, NRZ data output which is synchronized to the Servo Clock Input.
27	READ CLOCK	RCLK	Input clock from the drive which is synchronized with the Read Data input.
28	SERVO CLOCK	SCLK	A nominal 9.677 MHz clock input from the drive. This clock must be valid when Unit Ready (Pin 31) is active and Fault (Pin 34) is inactive.
29	READ DATA	RD	NRZ data input from the drive which must be synchronized to the Read Clock (Pin 25) input.
30	INDEX PULSE	IP	Active high input used to monitor the Index signal from the drive.
31	SECTOR	SEC	Active high input used to monitor sector pulses from the drive.
32	UNIT SELECTED	USEL	Active high input used to verify the selected drive.
33	UNIT READY	URDY	Active high input used to inform the WD1050 of a ready condition on a selected drive. If this line is made inactive during any command, command execution is terminated.
34	UNIT BUSY	UBSY	Active high input used to monitor drive status during a unit selection. If the unit had previously been selected and/or reserved prior to issuing a USTAG, the UBSY must be made active within one microsecond of the USTAG selection. This signal is used for dual-channel access applications and should be tied to ground when not used.
35	GROUND	V_{SS}	Ground.
36	FAULT	FAULT	Active high input used to detect a fault condition at the drive. Command execution is terminated if Fault is made active during any command. Only the Fault Clear Command may be issued while this line is asserted.

PIN NUMBER	NAME	SYMBOL	DESCRIPTION
37	SEEK ERROR	SKERR	Active high input used to detect a seek error at the drive.
38	ON CYLINDER	ONCYL	Active high input used to inform the WD1050 when the heads are settled and positioned over a cylinder.
39	WRITE PROTECT	WPROT	Active high input used to monitor the Write Protect signal from the drive.
40	NO CONNECTION	NC(TP)	Test Point.
41	NO CONNECTION	NC	
42	UNIT SELECT TAG	USTAG	Active high output used for selection of a unit on USO-US3 lines.
43-45	TAG1-TAG3	TAG1-TAG3	Active high outputs used to strobe specific data out on the Control Port Lines. Tag definitions are: TAG1 __ Cylinder address TAG2 __ Head/Volume select TAG3 __ Control Tag
46-49	UNIT SELECT 0-3	USO-US3	These four outputs reflect the contents of the unit address field of the task file and are used to select one of 16 drives.
50-59	CONTROL PORT BITS 9-0	CP9-CP0	Ten bit output bus used to issue tag parameters to the selected drive.
60	NO CONNECTION	NC	
61	NO CONNECTION	NC(TP)	Test Point.
62	BUFFER CHIP SELECT	$\overline{BCS}$	Active low output used to enable reading or writing to the external buffer by the WD1050.
63	BUFFER COUNTER RESET	$\overline{BCR}$	Active low output that is strobed prior to Read/Write Commands. Used to clear an external buffer counter.
64	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the external buffer.
65	BUFFER READY	BRDY	This input informs the WD1050 that the buffer is either full or empty.
66	INTERRUPT REQUEST	INTRQ	Active high output which is set at the completion of any command, providing the 'I' bit is also set in the command word. INTRQ is reset subsequent to a Status register read.
67	MASTER RESET	$\overline{MR}$	Active low input used to initialize the WD1050, usually after a power-UP condition.
68	CLOCK	CLK	2 MHz Master Clock is input.

FUNCTION DESCRIPTION

The WD1050 SMD Winchester Controller performs the necessary link between an 8 or 16 bit processor and an SMD compatible drive. The internal architecture of the WD1050 is shown in Figure 1. The major functional blocks are:

CONTROL UNIT

This section decodes commands, implements command execution sequencing, monitors the comparator and CRC logic, monitors status and issues control to the Host and Drive Interfaces. It also writes appropriate information to the Status register during command execution.

DATA I/O BUFFERS

A 16-bit bi-directional three-state bus (D15-D0) for data transfers between the Host CPU or data buffer and the HDC. (The higher order 8-bits of this bus [D15-D8] may be used for 8-bit data bus transfers between the Host CPU and the HDC).

HOST/BUFFER CONTROL

This section allows HDC register selection and communication by the CPU, issues interrupt requests, and provides Direct Buffer Access (DBA) transfers between the disk drive and the data buffer.

STATUS REGISTER

A 16-bit register reflecting operational status of the HDC and disk drive. This is a read-only register.

COMMAND REGISTER

A 16-bit field containing command information that dictates operational control sequencing of the Host and Drive Interfaces by the HDC. This is a write-only register.

DATA REGISTER

A 16-bit field used to assemble/disassemble words/bytes during data transfers. This register is internally interfaced to the HDC's Data I/O Buffers ('D' bus) and the HDC's Read Data Holding (RDH) register or Write Data Holding (WDH) register (as appropriate) during Host/drive data transfers. The contents of this register are compared to the appropriate Task File field as required by command execution.

CRC LOGIC

This logic is used to generate or check the 16-bit Cyclic Redundancy Check (CRC). The polynominal is:

$$G(x) = X^{16} + X^{12} + X^5 + 1$$

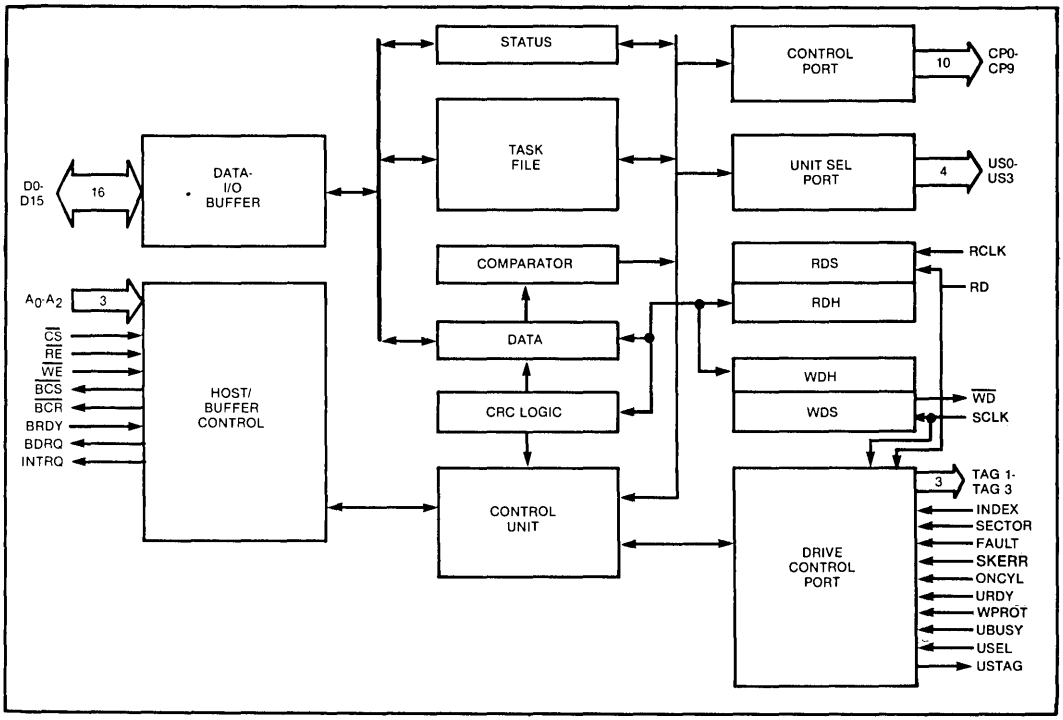


Figure 1. BLOCK DIAGRAM

The CRC includes all information beginning with the Sync character and ending with the CRC word. The CRC is preset to ones prior to a data transmission.

The CRC is implemented in parallel eight bits at a time as data is transferred between the HDC's Data register and the HDC's Read or Write Data Holding registers. The CRC word is transferred to the HDC's Data register and appended to the ID Field and Data Field (if enabled) during Format Sector or Write Data Commands.

COMPARATOR

A 16-bit comparator used to compare the appropriate HDC's Task File field with the respective byte(s) read from the disk.

READ DATA SHIFT REGISTER (RDS)

This 8-bit register shifts data read from Read Data (RD) input via the drives Read Clock (HDC's RCLK input).

READ DATA HOLDING REGISTER (RDH)

This 8-bit holding register assembles bytes from the Read Data Shift register and transfers them to the Data register.

WRITE DATA HOLDING REGISTER (WDH)

This 8-bit holding register receives bytes from the Data register and provides an eight bit parallel input to the HDC's Write Data Shift register (WDS).

WRITE DATA SHIFT REGISTER (WDS)

This 8-bit shift register converts the eight bit parallel input from the Write Data Holding register (WDH) into a serial bit stream issued to the HDC's Write Data ($\overline{WD}$) output via the drive's Servo Clock (HDC's SCLK input).

DRIVE CONTROL

This section monitors drive status, synchronizes the byte boundaries generated by the Servo Clock to the sync character read from the disk or the drive's Index or Sector pulse as appropriate, and issues control tags to the drive.

CONTROL PORT (CPO-9)

This 10-bit output is used to provide the drive with volume/head #, cylinder address, and control information in conjunction with outputs Tag 1 (cylinder address), Tag 2 (volume/head #), and Tag 3 (control). The contents of the appropriate HDC register or signals generated from the Control Unit are gated to the Control Port during command execution.

UNIT SELECT PORT (US0-3)

This 4-bit output port reflects the contents of the Unit Address register. The Unit Select Tag output selects the desired disk drive unit.

HOST INTERFACE

The primary interface between the Host processor and the WD1050 is through a 16-bit bi-directional bus. This bus is used to transfer status, parameter, and command information between the WD1050 and the Host, as well as data between the WD1050 and sector buffer. The external sector buffer is constructed with either FIFO memory or a RAM and binary counter. Since the WD1050 will make this bus active when accessing the sector buffer, a transceiver must be used to isolate this bus from the Host. Figure 2 shows a typical Host Interface using a RAM and Binary counter. The Sector Buffer may be one or more sectors in length, depending upon system requirements.

Whenever the WD1050 is not using the sector buffer, the Buffer Chip Select ($\overline{BCS}$) is high (disabled). This allows the Host to access the WD1050's Task File, read status, and issue commands. It also allows the Host to access data within the Sector Buffer. A separate RAM select line from the Host is used to access the data in memory. With each $\overline{RE}$ or $\overline{WE}$ strobe from the Host, the address counter is incremented on the trailing edge of $\overline{RE}$ or $\overline{WE}$, pointing to the next sequential memory location. Whenever the WD1050 changes the state of $\overline{BCS}$, the Buffer Counter Reset ($\overline{BCR}$) Line is strobed, causing the address counter to be reset to zero. The $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1050 to allow access to the buffer only when $\overline{BCS}$ is low. Although 8-bit programming is allowed via the use of Address Line 0. the data path to and from the WD1050 must be 16 bits wide.

TASK FILE

The WD1050 contains five 16-bit registers called the Task File. These registers are used to set up parameter information prior to issuing a command. These registers are:

A2	A1	A0	15 REGISTER 0
0	0	0	HEAD/SECTOR ADDRESS
0	1	0	SECTOR COUNT/LENGTH & UNIT ADDRESS
1	0	0	CYLINDER REGISTER
1	1	0	COMMAND REGISTER (WRITE ONLY)
1	1	0	STATUS REGISTER (READ ONLY)

Each register in the Task File is accessed by selecting the proper address while $\overline{CS}$ (pin 4) is low, then strobing the $\overline{WE}$ or $\overline{RE}$ lines. All registers in the Task File are Read/Write except for the Command/Status register. The Command register can only be written to, while the Status register is a read-only register. The command and status registers have the same address.

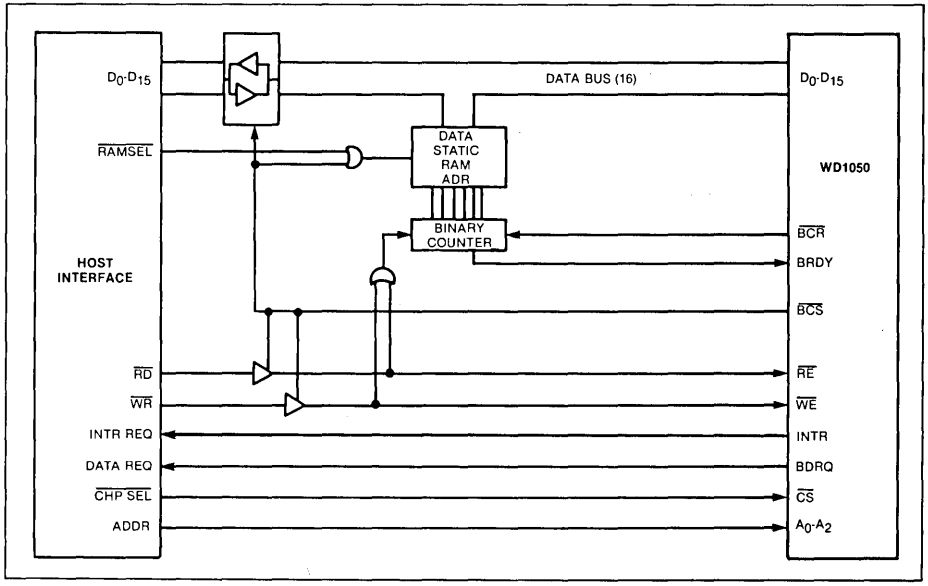


Figure 2. TYPICAL HOST INTERFACE

An 8-bit mode can also be used for accessing the Task File. Data is read/written on the most significant 8-bits of the Data bus (D15-D8). The upper byte is accessed with A_0 (pin 7) is high, and the lower byte is accessed when A_0 is low. The upper byte (A_0 = 1) must be accessed first, followed by the lower byte. This insures that data is transferred to the internal 16-bit bus properly, and that a command will execute after the full 16-bit word is written.

HEAD/SECTOR ADDRESS

This register holds the Head number and Sector Address fields:

15 — 8	7 — 0
HEAD NUMBER	SECTOR ADDR

The Sector Address byte (bits 7-0) holds the logical sector number used for comparison when searching for the specified ID field. The Head number byte (bits 15-8) holds the logical head number, and volume flag (where applicable). This 8 bit field is sent to the drive via the Control Port (CP7-0) when Tag 2 is issued. Note that all 8-bits of each byte are wrtten into the ID field during formats and are compared during other commands.

CYLINDER REGISTER

This register holds the 16-bit cylinder number:

15 — 0
CYLINDER REGISTER

The least significant 10-bits of this register (bits 9- 0) are transferred to the Control Port (CP9-0) when Tag 1 is issued. All sixteen bits of this register are written to the ID field during formats and are compared during other commands.

SECTOR COUNT/LENGTH & UNIT ADDRESS

This register holds the Sector Count, Sector Length and Unit Address fields:

15	14 — 8	7 — 4	3 — 0
M	SECTOR COUNT	LENGTH	UNIT

The four bit Unit Address field (bits 3-0) contains the physical Unit Address and is reflected at the drive via the Unit Select Port (US3-0). This port is used in conjunction with the Unit Select Tag (USTAG) output to select the desired drive.

The four bit sector length field is used to determine the number of bytes to be read/written from the disk. The allowable Sector Lengths are:

BITS				# OF BYTES
7	6	5	4	IN DATA FIELD
1	0	0	0	128
0	1	0	0	256
0	0	1	0	512
0	0	0	1	1024

If the CE bit (CRC Enable) in the command word is zero, an additional 8 bytes are added to the above sector length (and the CRC bytes are not appended to the data field). These bytes can be used to append ECC codes to each sector.

The Sector Count Field, seven bits of which (bits 14-8) are used to control single/multiple record operation for commands where the LS (Logical Sector) Flag is set, is decremented by one for each sector encountered after the desired sector has been located on the disk. The Op Code Command is repeated until the contents of this field (bits 14-8) are equal to zero. For single sector operation, this field (bits 14-8) must equal "0000000". (This field [bits 14-8] is ignored for the Fault Clear Command).

For the Format Sector, Verify Sector, and commands where the LS flag is not set, the Sector Count Field (bits 14-8) must contain the desired physical sector location (i.e., the Sector Count number of sector pulses from the Index Pulse = physical sector location). This register is counted down to zero to determine the physical sector location for these commands. For physical sectored commands, bit 15 is used as a one bit field controlling single/multiple record operation. For bit 15 equal to '0', a single sector command is executed. For bit 15 equal to '1', these commands are repeated until the Index pulse is re-encountered, allowing multiple sector operations.

For logical sectoring, bit 15 of this register should equal '0'.

COMMAND REGISTER

This "write-only" register is used to load in the desired command:

15	0
COMMAND REGISTER	

The command register may be loaded whenever the Command-In-Process (CIP) status bit is low.

STATUS REGISTER

This "ready-only" register is used to monitor status and error conditions as the result of command execution or its format is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCS	CIP	UBSY	USEL	WPRT	URDY	OCYL	SKER	BCS	FLT	BDRQ	-	DFCE	DFNF	IDCE	IDNF

BIT	NAME	DESCRIPTION
0	ID Field Not Found (ID/NF)	Set if the sync character preceding the ID Field contents read from the disk do not match the respective Task File contents.
1	ID CRC Error (IDCE)	Set if the CRC calculation on the ID Field read from the disk is in error.
2	Data Field Not Found (DFNF)	Set if the Data Field sync pattern following the ID Field does not match the sync character.
3	Data Field CRC Error (DFCE)	Set if the CRC Calculation on the Data Field read from the disk is in error.
4	Not Used	This bit is not used; it is forced to a zero.
5	Buffer Data Request (BDRQ)	Reflects the Buffer Data Request output.
6	Fault (FLT)	Reflects the status of the Fault (FLT) input.
7	Buffer Chip Select ($\overline{BSC}$)	This bit is an inverted copy of the Buffer Chip Select (BCS) output.
8	Seek Error (SKER)	Reflects the status of the Seek Error (SKER) input.
9	On Cylinder (ONCYL)	Reflects the status of the On Cylinder (ONCYL) input.
10	Unit Ready (URDY)	Reflects the status of the Unit Ready (URDY) input.
11	Write Protect (WPRT)	Reflects the status of the Write Protect (WPRT).
12	Unit Selected (USEL)	Reflects the status of the Unit Selected (USEL) input.
13	Unit Busy (UBSY)	Reflects the status of the Unit Busy (UBSY) input.
14	CIP	Set when a command is in progress.
15	Buffer Chip Select (BCS)	This bit is an inverted copy of the Buffer Chip Select (BCS) output. This bit also appears in Status Bit 7.

Note: That Status Register bits 13-8 are frozen upon premature command termination (as described in Command Execution, step 2). These bits are released to active monitoring and error bits 3-0 are reset low following a read of the Status register (or following programming of the Command register) when the Command register CIP bit is low and/or the INTR output is inactive.

INSTRUCTION SET

The WD1050 will execute eight commands. Prior to issuing a command, the Host must first setup the Task File with parameter information.

A command can only be accepted if the CIP bit in the status register is low.

COMMAND	MSB COMMAND REGISTER BITS LSB															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fault Clear	1	0	0	0	0	0	0	I	0	0	0	0	U	S	E	D
Return to Zero	1	0	0	1	0	0	0	I	0	0	0	M	U	S	E	D
Seek Cylinder	1	0	1	0	V	L	O	I	Z	C	H	M	U	S	E	D
Read ID Field	1	0	1	1	R	L	O	I	Z	C	H	M	U	S	E	D
Read Sector	1	1	0	0	R	L	O	I	Z	C	H	M	U	S	E	D
Write Sector	1	1	0	1	R	L	O	I	Z	C	H	0	U	S	E	D
Format	1	1	1	0	R	P	O	I	Z	C	H	0	U	S	E	D
Verify	1	1	1	1	R	P	O	I	Z	C	H	M	U	S	E	D

FLAG SUMMARY	
V = Verify	I = Interrupt Enable
R = CRC Enable	Z = Volume/Head Change
L = Logical Sectoring	C = Cylinder Addr
P = Programmable Sectors	H = Head Selection
O = On Cylinder	M = Marginal Data Recovery
E = Priority Release/Early	U = Unit Sel/Servo Minus
D = Unit Deselect/LATE	S = Priority Sel/Servo Plus

COMMAND FLAG DESCRIPTION

BIT	NAME	DESCRIPTION
V	Verify	Compare The Head number and Cylinder Address word of the ID field with the appropriate Task File field when On Cylinder becomes active. The Sector Address byte in the ID Field is not compared, althought the CRC is checked. This flag is valed only for the Seek Cylinder Command.
R	Data Field CRC Enable	Data Field CRC is enabled. If the flag is not set, the condition of the DFCRC Status bit will not affect command execution; the data field is extended by four words (8 bytes), and the CRC bytes are not appended.
L	Logical Sectoring	Locate sector by matching the ID Field bytes read from the disk to the appropriate field in the HDC Task File. The Sector Count register in the Task File is used to indicate the additional number of sectors to be transferred for multiple sector commands. If L is not set, physical sectoring is implemented. The Task File Sector Count register is decremented to locate the desired physical sector from the Indes pulse. ID Field compares are made, but do not affect command execution.
P	Programmamble Sectors	The Head Number/Sector Address register is read from the buffer as each sector is encountered per command execution. (This allows an entire track to be formatted/verified with interleave sectors in one revolution of the disk). This flag is valid only for the Format Sector or Verify Sector Commands.
O	On Cylinder	For the Seek Cylinder Command, command completion requires activation of On Cylinder or Seek Error inputs. For other commands, On Cylinder is required before a read or write can occur.
I	Interrupt Enable	Enable the interrupt output (INTRQ) for activation upon completion or termination of command execution.

COMMAND FLAG DESCRIPTION

BIT	NAME	DESCRIPTION
Z	Volume/Head	Issue Tag 2 as required for volume/head change.
C	Cylinder	Issue Tag 1 as required for cylinder address selection. (Tag 1 will follow Tag 2 if the Z and C flags are both set).
H	Head	Issue Tag 2 as required for head selection. (Tag 2 will follow Tag 1 if the C and H flags are both set).
M	Marginal Data	Attempt a marginal data recovery. (marginal data recovery may be attempted only where a command requires reading from the drive). This bit controls the function of bits 3-0 (U, S, E, D). (See Note 1)
U	Unit Select/Servo Offset Minus	For M = 0 (or not applicable, set Unit Select Tag as required for unit selection. Unit Selected must become active for command execution to continue.
S	Priority Select/ Servo Offset Plus	For M = 0, issue priority select control as required to reserve the unit. See Note 2). For M = 1, issue servo offset plus control for marginal data recovery attempt.
E	Priority Release/ Data Strobe Early	For M = o, issue priority release control as required to release reserve of the unit. (See Note 2) For M = 1, issue data strobe early control for marginal data recovery attempt.
D	Unit Deselect/Data Strobe Late	For M - 0, reset Unit Select Tag at Completion of the command. For M - 1, issue data strobe late contron for marginal data recovery attempt.

Note 1: Certain marginnal data recovery features are not applicable depending on the particular drive type under control. (Refer to CDC Interface Specification 64712400).

Note 2: Priority select and release features are applicable only for dual channel drive applications.

COMMAND EXECUTION

Command work architecture has been designed to provide comprehensive control of the drive unit via programmable macro-level commands. For example, unit selection, cylinder seek, head selection, Op Code execution (of multiple records if desired), and unit deselection can be performed with a single command.

Command execution follows the following sequence (for 'M'flag = 0):

1. If the U flag is set, the Unit Select (US) Tag is activated. (The drive should select the unit specified by the Unit Select bus [US0-3] when the US Tag is activated.)

   If the S flag is also set, CP9 will be activated when the US Tag is activated (exclusively reserving the unit to that channel until released).

2. The following conditions must be met and maintained for command execution to continue:
   Unit Ready input active
   Unit Selected input active
   Unit Busy input not active

   If these comditions are not met, command execution is terminated with the appropriate bit set in the Status register.

   For all commands except the Fault Clear Command, the Fault input must also be inactive and remain inactive for command execution to continue.

3. For the Write Data and Format Commands, the Write Protect Status bit is checked; if true command execution is terminated.

4. For the Write Data Command, and the Format Verify Command with the P (programmable sector) flag set, the HDC activates BDRQ requesting the Host to provide the required data to the buffer.

5. If the Z flag is set (indicating a volume change), the Head number field of the Task File is issued to the Control Port (Head field bits 15-8 to CP lines 7-0 respectively), and Tag 2 is pulsed. (Applies only for drives with volume select.)

6. If the C flag is set (indicating a cylinder address seek), the Cylinder Address field of the Task File is issued to the Control Port (bits 9-0 respectively), and Tag 1 is pulsed.

NOTE:

For the Seek Cylinder Command, and for other commands where the On Cylinder flag is set, the On Cylinder input must be active before Tag 1 will be issued. (If the Seek Error input is active or becomes active before On Cylinder is active, execution is terminated with the Seek Error status recorded in the Status register).

7. If the H flag is set (indicating a head selection), the Head number field of the Task File is issued to the Control Port (Head field bits 15-8 to CP lines 7-0 respectively), and Tag 2 is pulsed.
8. For commands other than Seek Cylinder, O flag operation is as follows:

   If O is set, execution is suspended pending an active On Cylinder input.

   if O is not set, the command is executed regardless of the condition of On Cylinder.

   NOTE:

   Data transfer to/from the drive with On Cylinder inactive is allowed only under certain circumstances on specific drives. For example, on a drive with both fixed and moveable heads, it is possible to execute a Seek Cylinder Command with the C flag not set to the moveable heads (On Cylinder will drop). The fixed heads may then be given a Read Data command with the O flag not set. The Fixed head can then be read regardless of the condition of On Cylinder. (This is an overlap seek within a given unit between the fixed and moveable media). For valid read/write operation without an active On Cylinder, refer to the appropriate drive operating specification.

   For commands with C set and Seek Error received instead of On Cylinder, command execution is terminated.
9. For the Write Data Command, and the Format and Verify Commands with the P flat set, the BRDY input is inspected. Command execution is suspended pending reception of a low to high transtion on the BRDY input.

   NOTE:

   For commands where M is set, marginal data recovery control as described in the chart below is issued to the control port prior to the activation of Tag 3. Note that unit selection, channel reserve control, and unit deselection must be accomplished with a non-marginal data recovery command since the U, S, E, and D flags assume marginal data recovery control significance.

COMMAND FLAG IF MD IS SET	FEATURE	CONTROL PORT BIT ACTIVATED
U	Servo Offset Plus	2
S	Servo Offset Minus	3
E	Data Strobe Early	7
D	Data Strobe LATE	8

Location of the appropriate sector within the cylinder is common to all commands except Fault Clear and RTZ. One of two methods is used: logical sector search (for commands where the L flag is set) and physical sector locating (for the Format and Verify Commands and commands where the L bit is not set).

Logical sector search consists of reading the first encountered ID Field, comparing these bytes to the appropriate fields in the HDC's Task File, (including the sync byte) and checking the ID Field CRC bytes. When a valid compare with correct CRC are found, execution continues. If a valid compare with correct CRC are not found before four Index pulses are detected, the appropriate Status bits are set (IDNF and/or IDCE) and command execution is complete. For mulitple sector commands, The Sector Address field of the Task File is incremented between sectors and the Sector Count field is used to indicate the number of additional sectors for which the command is to be executed. A single sector sommand is executed for Sector Count = '00. . .00".

Physical sector locating is accomplished by decrementing the Sector Count field of the Task File by one for each Sector pulse encountered after the Index pulse is located until the Sector Count field = '0000000'. For Sector Count = '0000000', the command will be executed to the sector immediately following the Index pulse. The ID Field compares and the IDCE check are still made and the appropriate bit set in the Status register (if applicable), but command execution is not affected by an error condition. A single sector command is executed if bit 15 of the Sector Count/Sector Length/Unit Address register of the Task File is zero. If bit 15 is one, command execution is repeated until the Index pulse is re-encountered. Note that Status register error bits are not cleared between sectors (one's catching).

Tag 3 (Control Select) is activated for all commands except Seek Cylinder with the V flag not set.

When the appropriate Sector pulse is encountered, CPI (Read Gate) is activated and the HDC synchronizes to the first low to high transition on the Read Data (RD) input. This initiates the following three compares: the sync byte FE preceded by eight zeros, the upper and lower Cylinder Address, and the Head number and Sector Address. (The Sector Address compare is suppressed on the Seek Cylinder command). The ID FIELD CRC is then checked. CPI is deactivated and command execution follows.

FAULT CLEAR

CP4 (Fault Clear) is pulsed and this completes execution. This command is intended to clear the Fault output of the drive. The condition causing the fault within the drive should no longer exist when this command is issued.

RTZ (RETURN TO ZERO)

CP6 (RTZ) is pulsed and the Cylinder Address, Head number, and Sector Address fields of the Task File are all set to zero. This completes execution.

SEEK CYLINDER

Execution of this command is controlled completely by the command flags. If O is set, execution is suspended until On Cylinder (or Seek Error) is received. If the V flag is not set, receipt of On Cylinder completes execution. If C and V are both set, and On Cylinder is received, CPI (Read Data) is issued and the ID Field is inspected. The Sector Address compare is not made for this command.

NOTE:

If L is set (logical sectoring), execution is complete when ID Field is successfully found or when the 4th Index pulse is encountered. There is no multiple sector operation when L is set for this command. If L is not set (physical sectoring). the IDNF and IDCE Status bit are one's catching. (The entire track may be verified with multiple sector operation).

The V flag is ignored if the O flag is not set.

If the C flag is not set, this command may be used for Unit Select only functions.

READ ID FIELD

The Read ID Field command is provided to allow transfer of the ID Field formatted on the disk to the data buffer (i.e., $\overline{BCS}$ • D15-Do • $\overline{WE}$ pulses). The Sector Address field is not compared in this command.

If the L flag is set, the first encountered ID Field is transferred to the buffer. The following bytes are transfered: 00FE, Upper and Lower Cylinder Address, Head number, Sector Address, and two CRC bytes. Thus four $\overline{WE}$ pulses are issued.

If the L flag is not set, the physical sector is located and the corresponding ID Field is transferred to the buffer.

There are no retries with this command if ID Field compare errors result.

For the Read ID Field command, CP1 is reactivated, and the first low to high transition on the RD input initiates a compare for the Data Field sync character. If the compare does not match, the Data Field Not Found (DFNF) Status bit is set. The Data Field CRC (DFCE) Status bit is set if an error is detected. CP1 is then deactivated.

Note that the Data Field is not transferred with this command, but that the following eight bytes are transferred: 00, FE, Upper Cylinder Address, Lower Cylinder Address, Head #, Sector Address, and the two CRC bytes.

If the L flag is not set, multiple sector operation continues to the next INDX pulse without inspection BRDY.

For multiple sector operation, the Sector Address Field of the Task File is automatically incremented. If the L flag is set, the BRDY input is inspected following each sector's transfer. If a low to high transition has not occurred (i.e., buffer not full) execution is then repeated. If a low to high transition has occurred, (i.e., buffer is full) BSC is deactivated, BCR is pulsed, and BDRQ is activated. Execution is suspended pending a low to high transition of BRDY (i.e., buffer empty). BCR is then pulsed, and execution is repeated. If a Data Field CRC is detected, the command will not terminate.

READ DATA

After the appropriate sector has been located, Data Field operation is as described under the Read ID Field Command, except that the Data Field is transferred to the buffer. Note that only the Data Field data bytes are transferred with this command.

This completes execution for single sector commands and for multiple sector commands where the L and R flags are set. If a Data Field sync error (DFNF) or a Data Field CRC (DFCE) error has occurred, the command will be terminated.

For multiple sector commands where the R flag and/or L flag is not set, or for multiple sector commands where no Data Field error has occured, execution is repeated.

Note that if the R flag and/or the L flag is not set, the DFNF and DFCF Status bits are one's catching.

WRITE DATA

After the appropriate sector has been located, CPO (Write Gate) is activated. Thirteen bytes of zeros (two Write Splice bytes and eleven PL0 Sync bytes) are written followed by the sync character. The Data Field is then written to the disk from the data buffer (i.e., $\overline{BCS}$ • D15-D0 • $\overline{Re}$ pulses). The CRC bytes and two bytes of zeros (End of Record) are appended to the Data Field and written to the disk.

For multiple sector operation, the BRDY input is inspected following each sector's transfer. If a low to high transition has not occurred (i.e., buffer empty), $\overline{BCS}$ is deactivated, $\overline{BCR}$ is pulsed, and BDRQ is activated. Execution is suspended pending a low to high transition on BRDY (i.e., buffer full). $\overline{BCR}$ is then pulsed, and execution is repeated.

FORMAT SECTOR

Physical sectoring only applies to the Format Sector Command. Upon reception of the appropriate Sector pulse, CP0 (Write Gate) is activated. Twenty seven bytes of zeros (16 Head Scatter bytes and eleven PL0 Sync bytes), and the sync character are written to the disk from the HDC's Task File, and the resultant CRC is appended. Thirteen bytes of zeros are written (two Write Splice bytes and eleven PL0 sync bytes) followed by the sync character. The Data Field (Format Character E5 repeated) is then written. If the R bit is set, then the two CRC bytes are appended; if

R is not set, eight additional E5's are added to the data field. Zeros are written until the next Sector or Index pulse is encountered.

For single sector operations CP0 is then deactivated. For multiple sector operation, CP0 remains active, and execution is repeated until the Index pulse is again encountered.

If the P flag is set, the HDC will fetch the Head Number / Sector Address from the data buffer prior to encountering each ID Field. Thus, by filling the data buffer with the desired Head Number / Sector Address information, the HDC can format an entire track with any given programmed sector interleave in one revolution.

If the P Flag is not set, the contents of the Sector Address field of the Task File will be incremented by one between sectors.

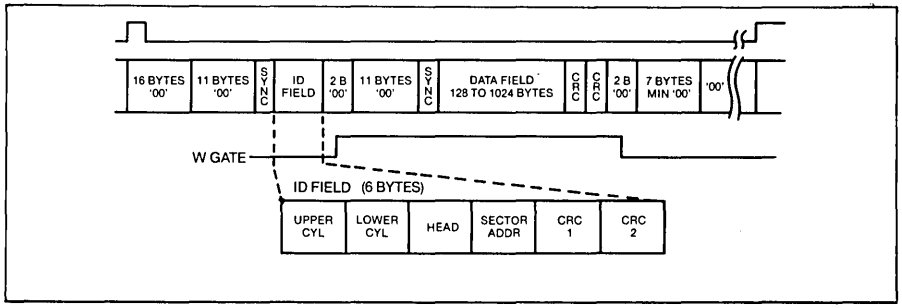
The BCS output will remain active for the duration of this command.

VERIFY SECTOR

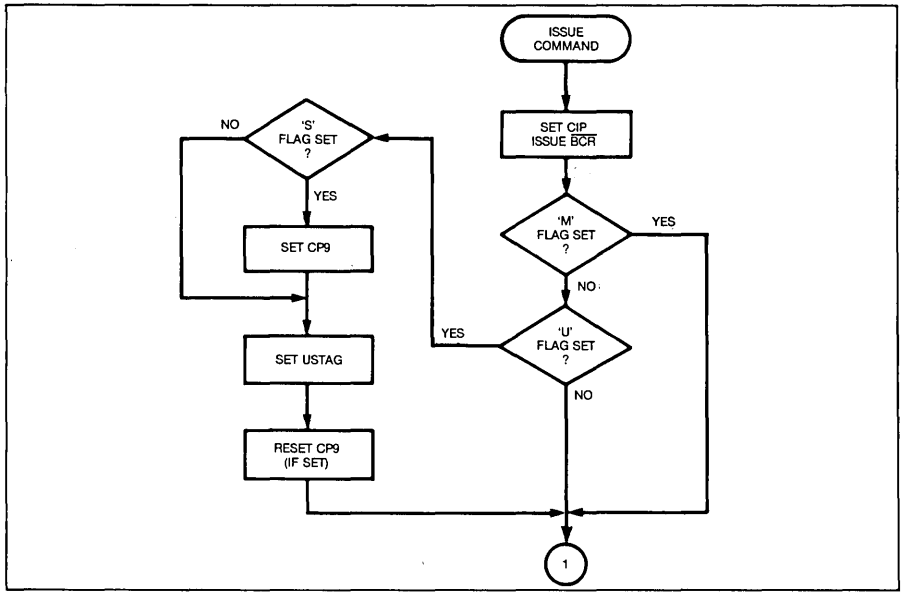
This command allows verification of sector format without transfer of data. Sector addressing is identical to that described for the Format Sector Command. The IDNF, IDCE, DFND and DFCE bits are set if errors are found (all bits are one's catching for multiple sector operation). With multiple sector operation, an entire track can be verified in a single revolution.

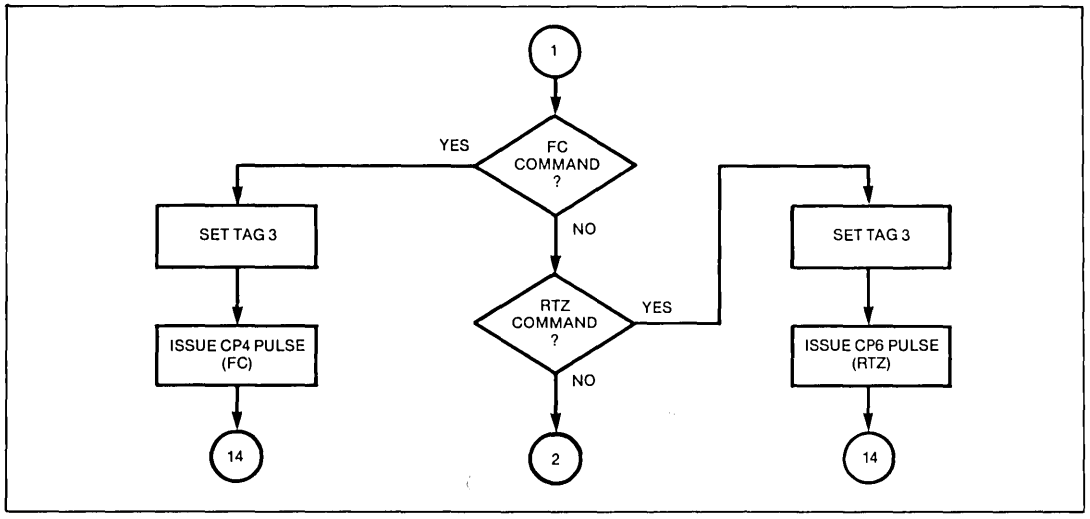
NOTE:

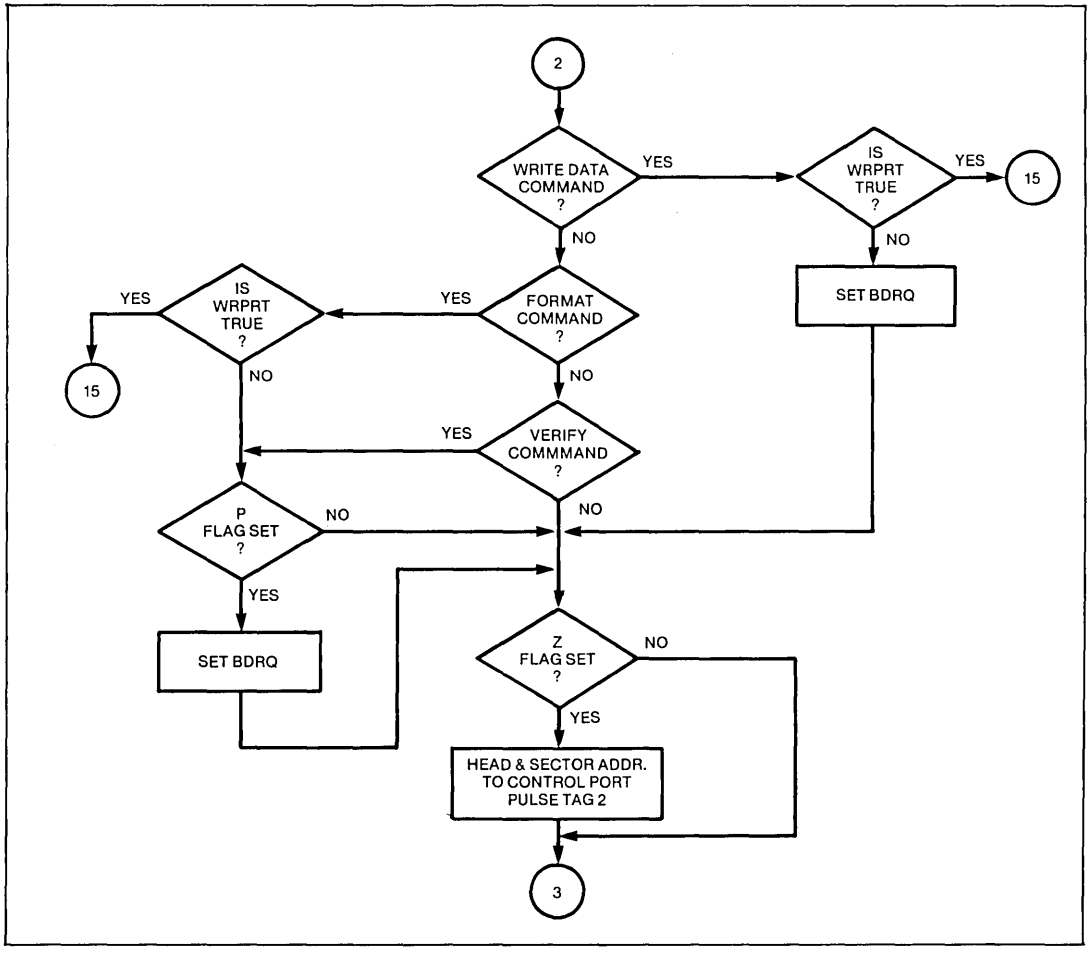
When used with the Lark drive, the validity of the DFCE bit is not guaranteed with this command if it immediately follows a FORMAT of the sector.

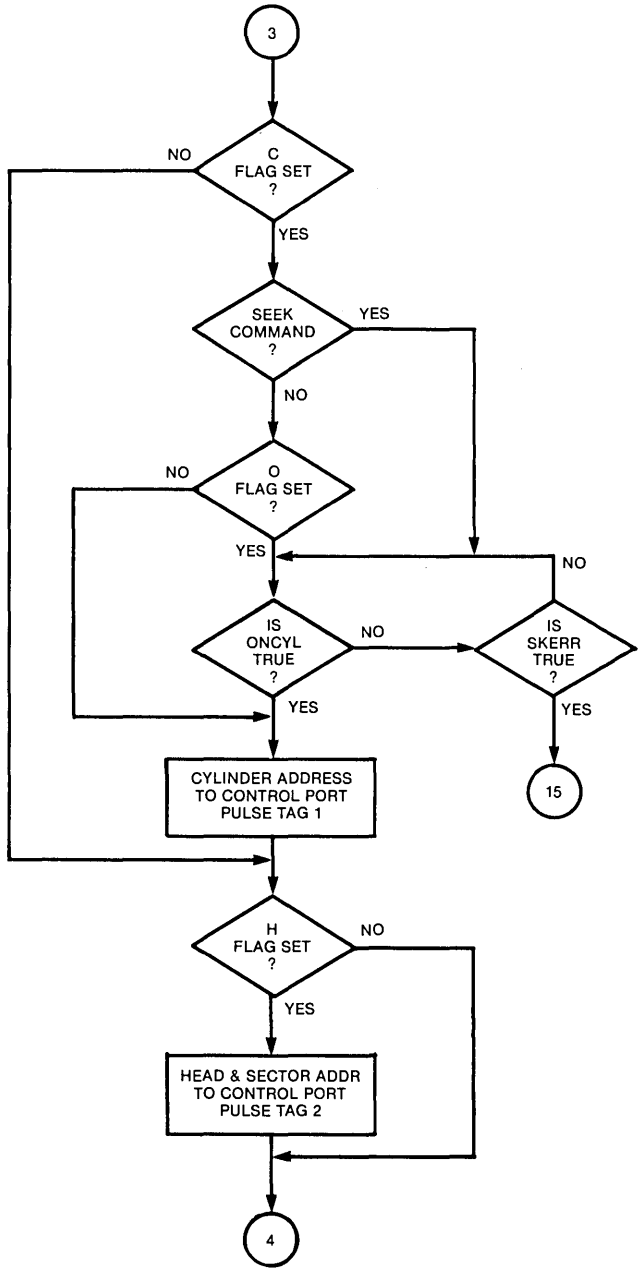


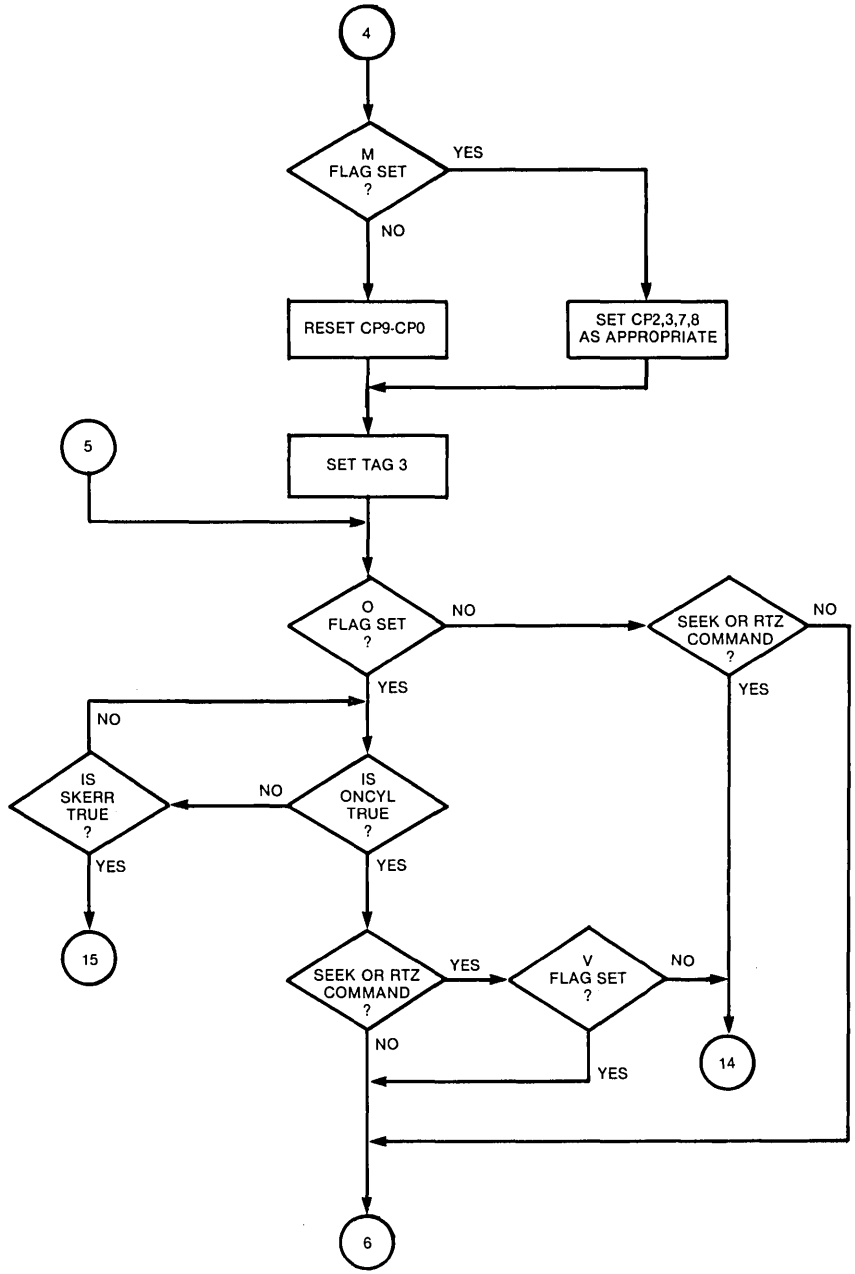
FIXED SECTOR FORMAT

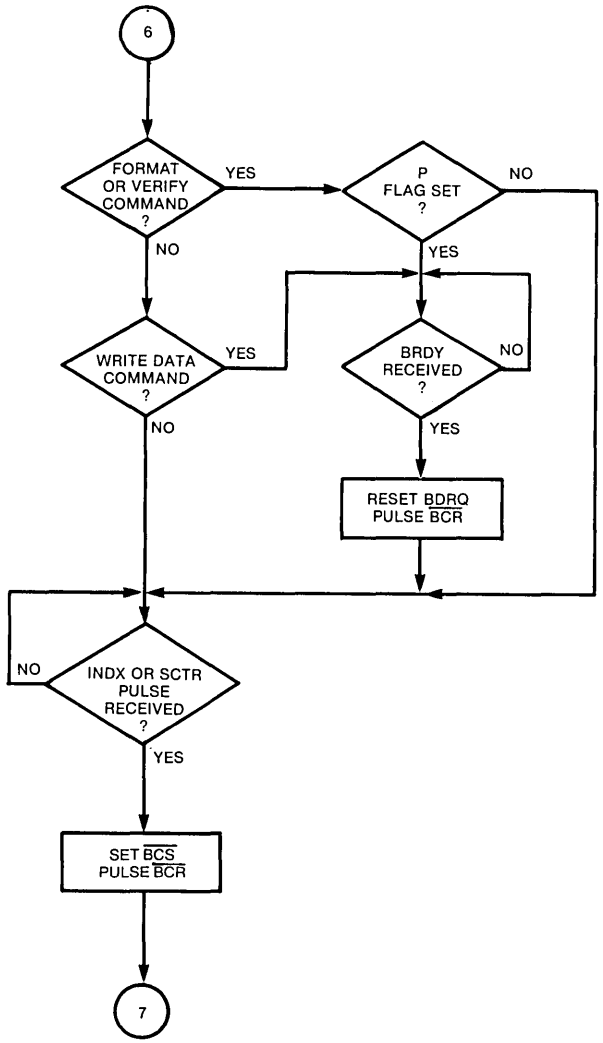


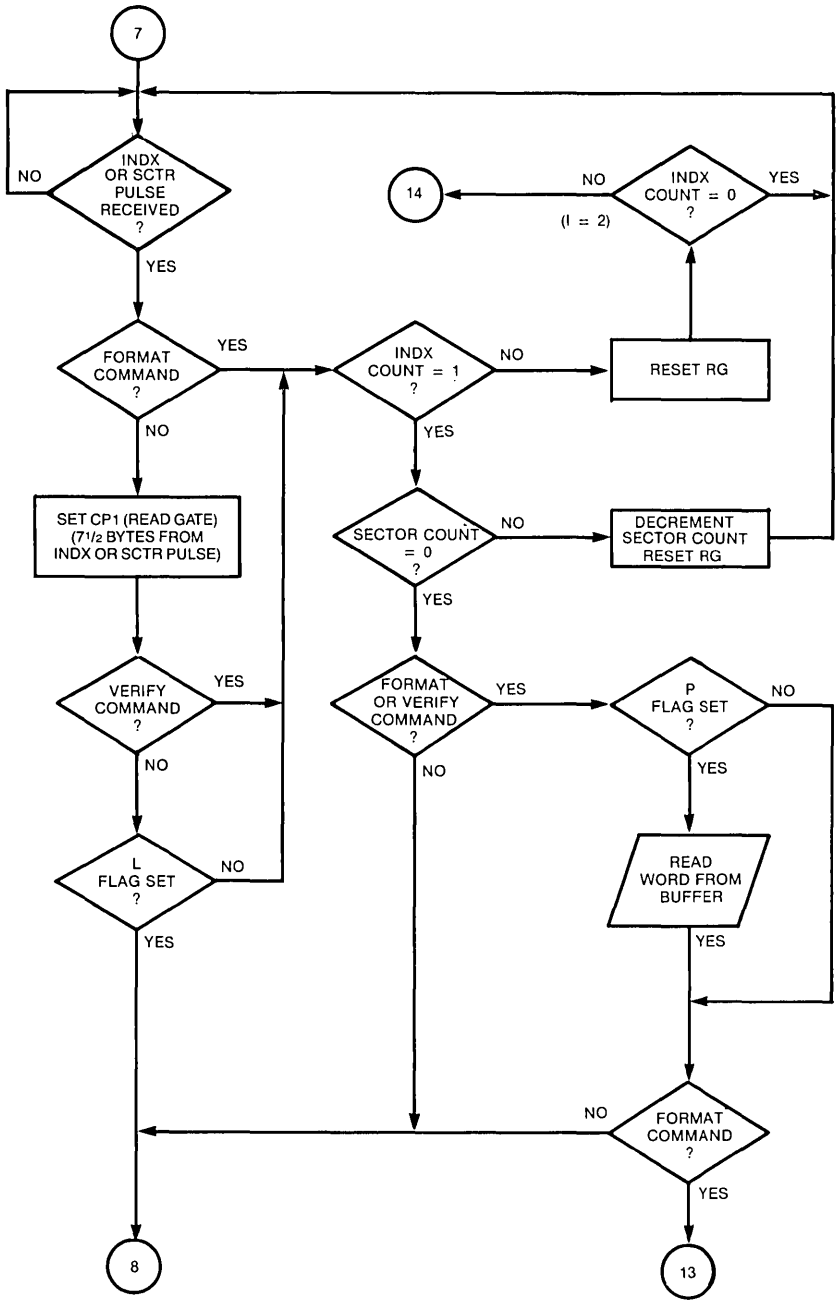

1
FC COMMAND ?
YES
NO
SET TAG 3
ISSUE CP4 PULSE (FC)
14
RTZ COMMAND ?
YES
NO
2
SET TAG 3
ISSUE CP6 PULSE (RTZ)
14

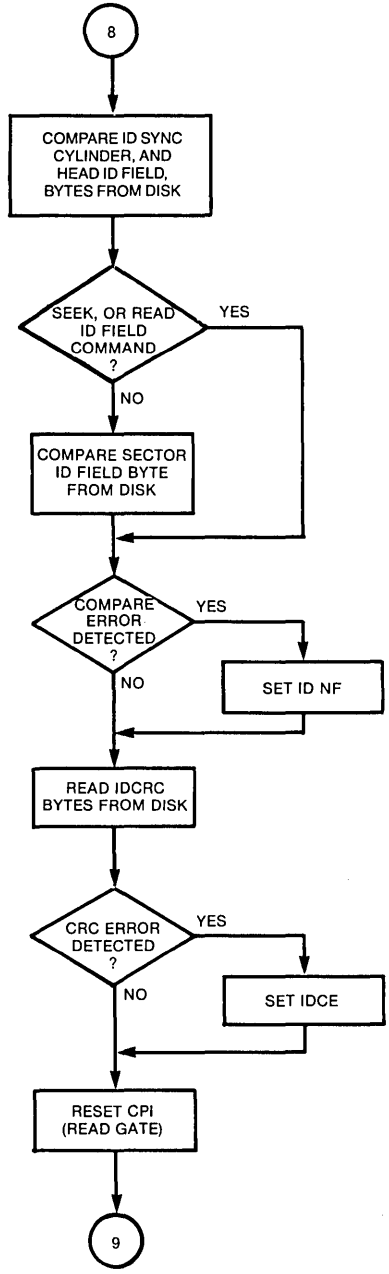

2
WRITE DATA COMMAND ?
YES
NO
IS WRPRT TRUE ?
YES
15
NO
SET BDRQ
FORMAT COMMAND ?
YES
IS WRPRT TRUE ?
YES
15
NO
NO
VERIFY COMMMAND ?
YES
P FLAG SET ?
NO
YES
SET BDRQ
NO
Z FLAG SET ?
NO
YES
HEAD & SECTOR ADDR. TO CONTROL PORT PULSE TAG 2
3

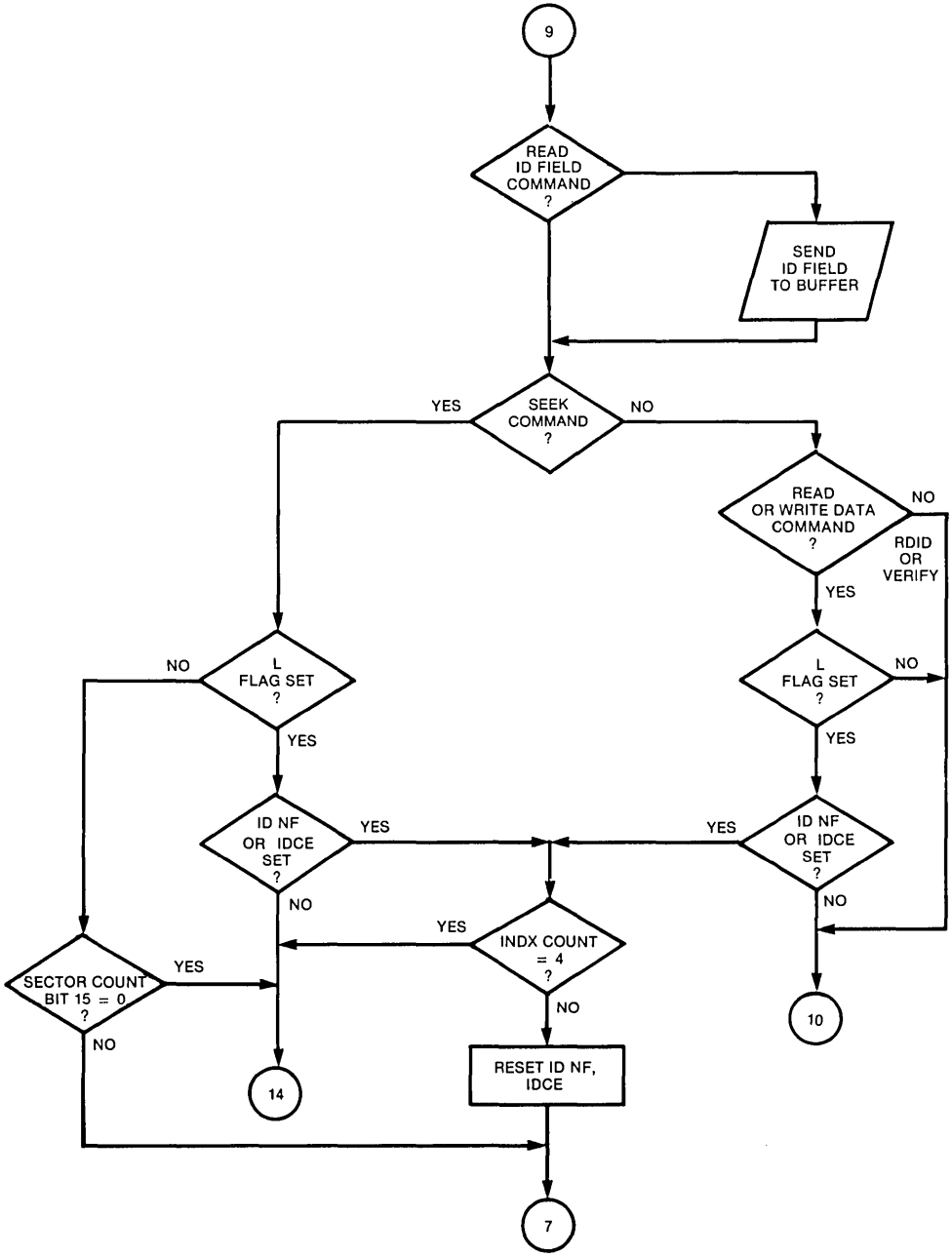

3
C FLAG SET ?
NO
YES
SEEK COMMAND ?
YES
NO
O FLAG SET ?
NO
YES
NO
IS ONCYL TRUE ?
NO
IS SKERR TRUE ?
YES
YES
CYLINDER ADDRESS TO CONTROL PORT PULSE TAG 1
15
H FLAG SET ?
NO
YES
HEAD & SECTOR ADDR TO CONTROL PORT PULSE TAG 2
4


4
M FLAG SET ?
YES
NO
RESET CP9-CP0
SET CP2,3,7,8 AS APPROPRIATE
5
SET TAG 3
O FLAG SET ?
NO
SEEK OR RTZ COMMAND ?
NO
YES
YES
NO
IS SKERR TRUE ?
NO
IS ONCYL TRUE ?
YES
YES
15
SEEK OR RTZ COMMAND ?
YES
V FLAG SET ?
NO
NO
YES
14
6

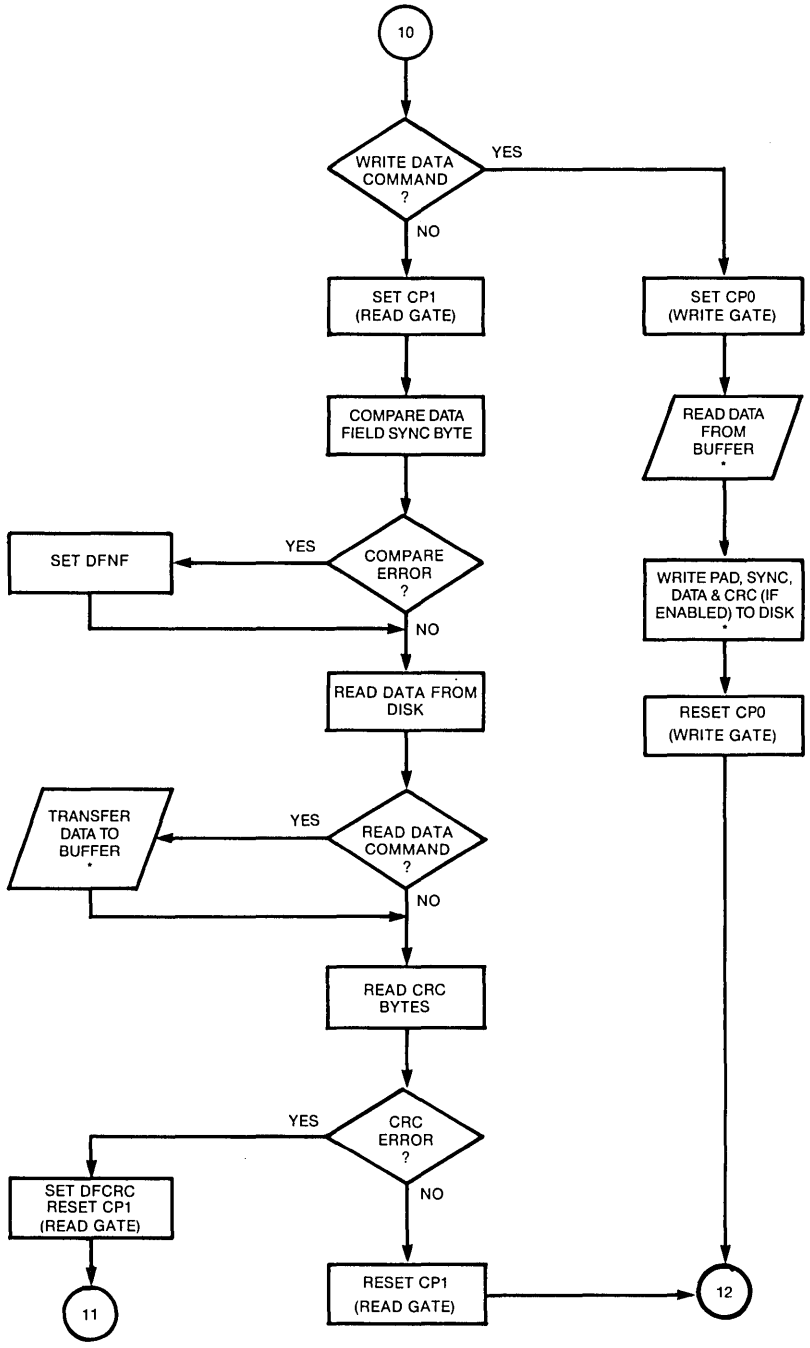

6
FORMAT OR VERIFY COMMAND ?
YES
NO
P FLAG SET ?
NO
YES
WRITE DATA COMMAND ?
YES
NO
BRDY RECEIVED ?
NO
YES
RESET BDRQ PULSE BCR
NO
INDX OR SCTR PULSE RECEIVED ?
YES
SET BCS PULSE BCR
7

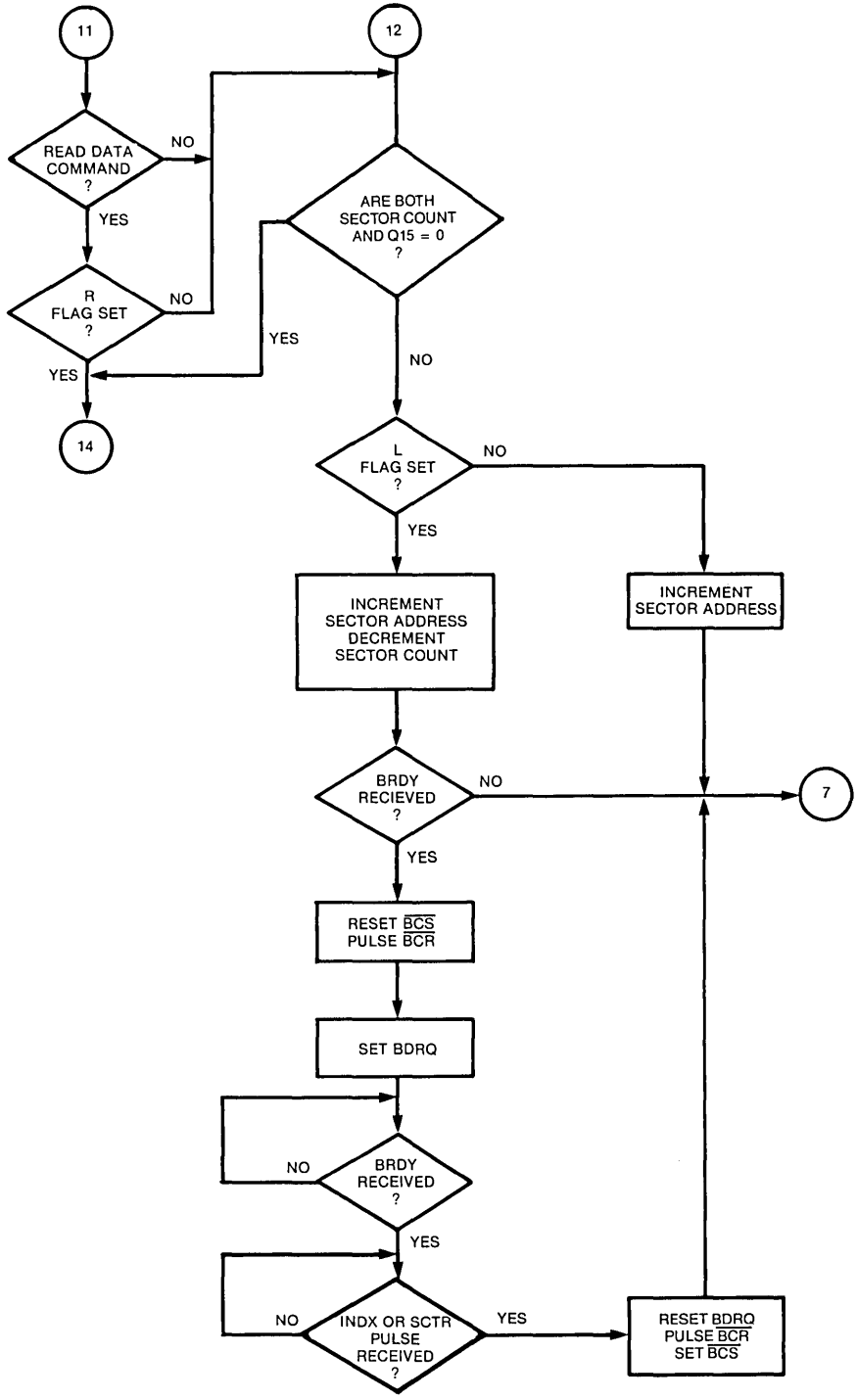

7
INDX OR SCTR PULSE RECEIVED ?
NO
YES
FORMAT COMMAND ?
YES
NO
SET CP1 (READ GATE) (7 1/2 BYTES FROM INDX OR SCTR PULSE)
VERIFY COMMAND ?
YES
NO
L FLAG SET ?
NO
YES
8
INDX COUNT = 1 ?
NO
YES
RESET RG
SECTOR COUNT = 0 ?
NO
YES
DECREMENT SECTOR COUNT RESET RG
FORMAT OR VERIFY COMMAND ?
YES
NO
P FLAG SET ?
NO
YES
READ WORD FROM BUFFER
YES
NO
FORMAT COMMAND ?
YES
13
14
NO
(I = 2)
INDX COUNT = 0 ?
YES


8
COMPARE ID SYNC CYLINDER, AND HEAD ID FIELD, BYTES FROM DISK
SEEK, OR READ ID FIELD COMMAND ?
YES
NO
COMPARE SECTOR ID FIELD BYTE FROM DISK
COMPARE ERROR DETECTED ?
YES
NO
SET ID NF
READ IDCRC BYTES FROM DISK
CRC ERROR DETECTED ?
YES
NO
SET IDCE
RESET CPI (READ GATE)
9

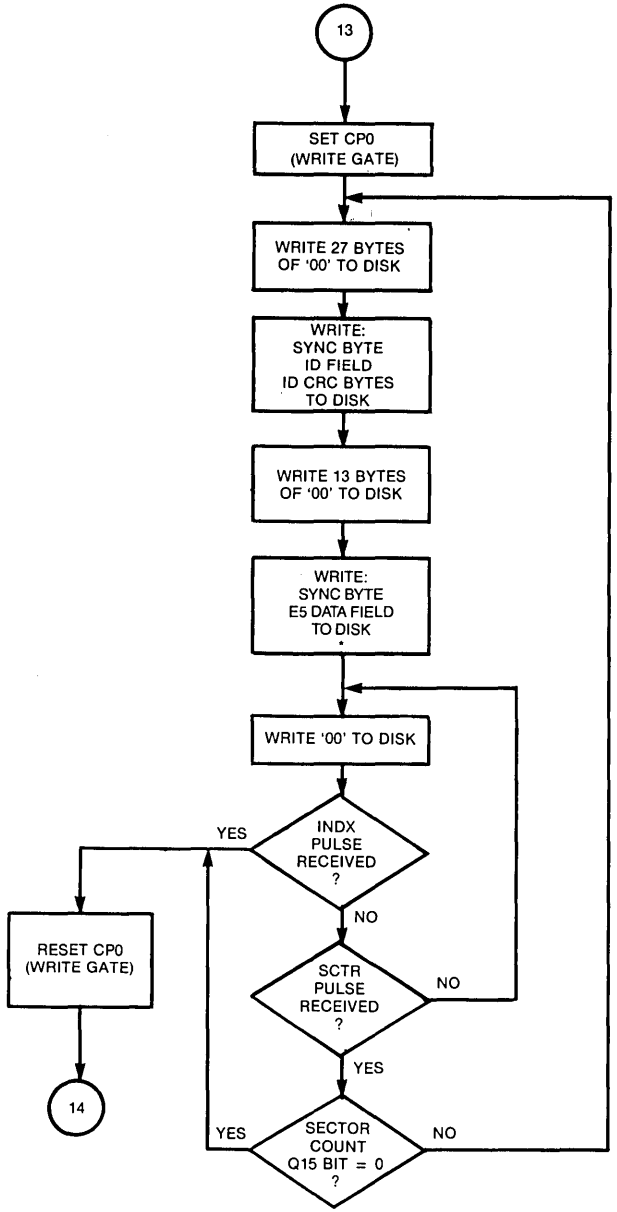


Note: If the R Flag is not set, 8 additional bytes are included in the Data Field for appended ECC.

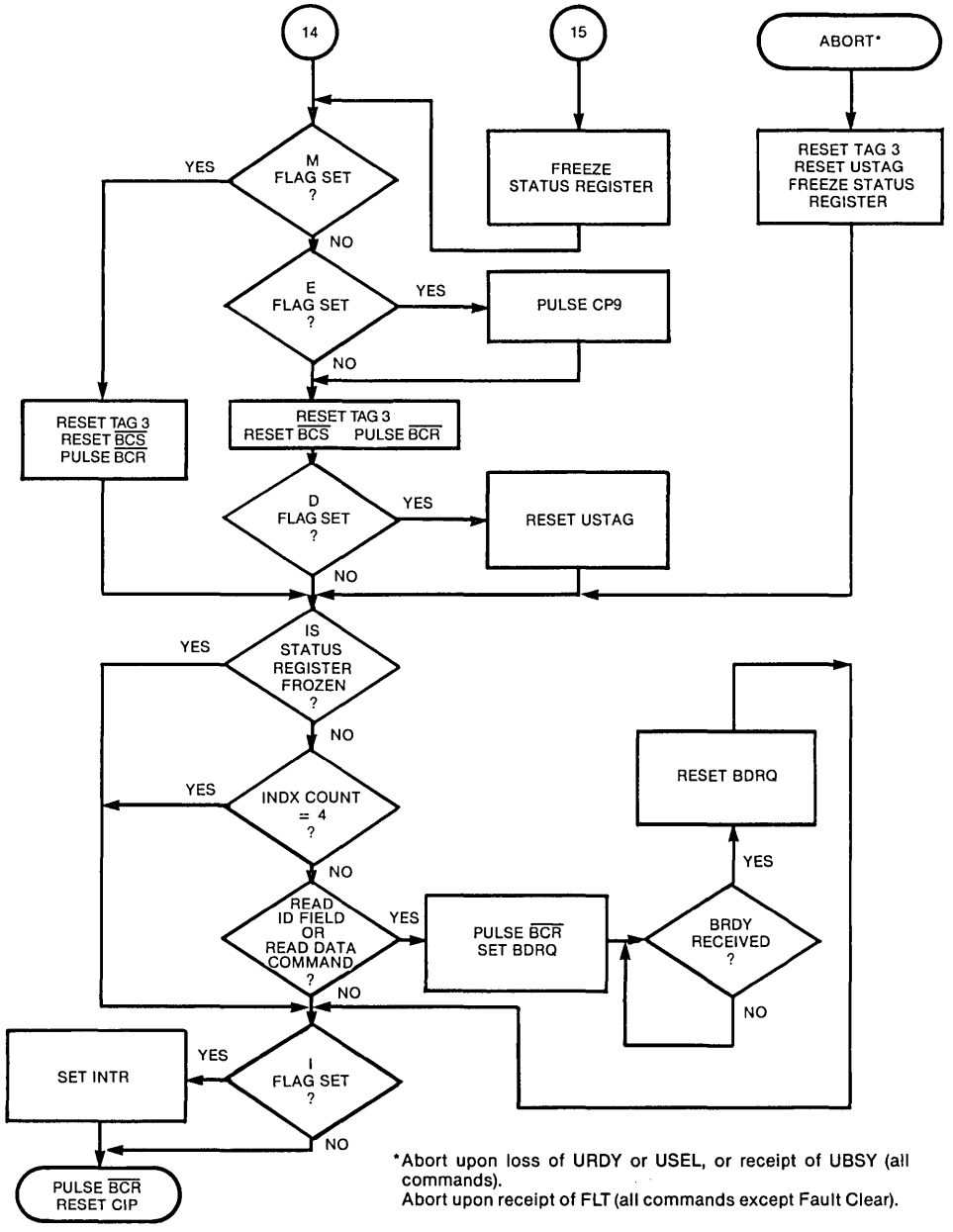

10
WRITE DATA COMMAND ?
YES
NO
SET CP1 (READ GATE)
SET CP0 (WRITE GATE)
COMPARE DATA FIELD SYNC BYTE
READ DATA FROM BUFFER
SET DFNF
YES
COMPARE ERROR ?
WRITE PAD, SYNC, DATA & CRC (IF ENABLED) TO DISK
NO
READ DATA FROM DISK
RESET CP0 (WRITE GATE)
TRANSFER DATA TO BUFFER
YES
READ DATA COMMAND ?
NO
READ CRC BYTES
YES
CRC ERROR ?
SET DFCRC RESET CP1 (READ GATE)
NO
RESET CP1 (READ GATE)
11
12



Note: if the R flag is not set, 8 additional E5 bytes are included in the Data Field for ECC extension.



* Abort upon loss of URDY or USEL, or receipt of UBSY (all commands).
Abort upon receipt of FLT (all commands except Fault Clear).



*Abort upon loss of URDY or USEL, or receipt of UBSY (all commands).
Abort upon receipt of FLT (all commands except Fault Clear).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with
respect to V_{SS} .....-0.5V to +7V
Operating Temperature...0°C(32°F) to 70°C(158°F)
Storage Temperature .....-55°C(-67°F) 50
+125°C(257°F)

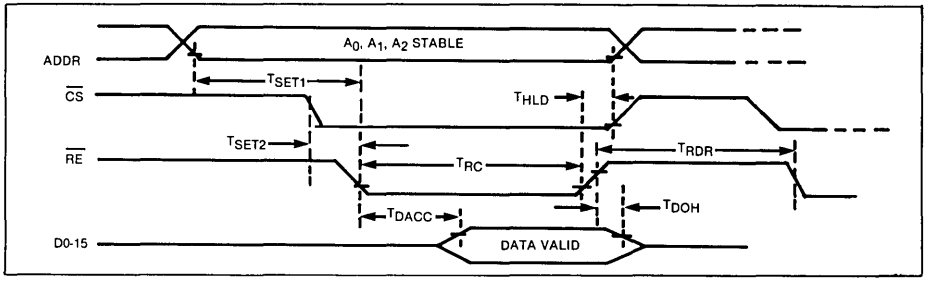
NOTE:

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = OV, V_{CC} = +5V ±.25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = 100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
I_{CC}	Supply Current		200	mA	All Outputs Open
	FOR PINS 25, 26,27:				See Note 1
V_{IH}	Input High Voltage	V_{CC}		V	
V_{IL}	Input Low Voltage		V_{SS} + ≤0.4 V	V	

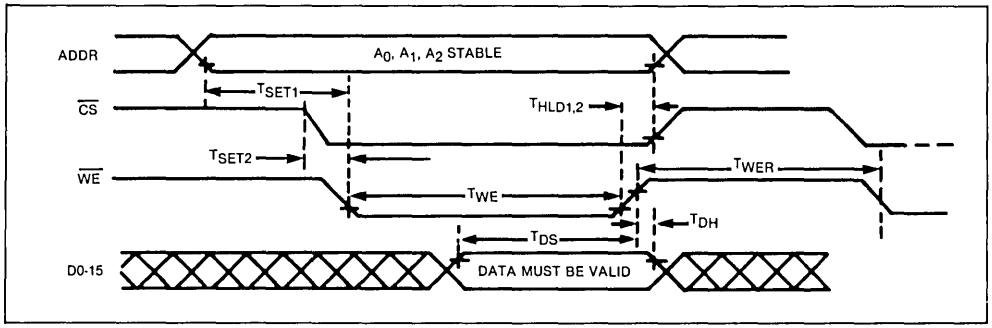
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = OV, V_{CC} = +5V ±.25V



HOST READ TIMING

HOST READ TIMING

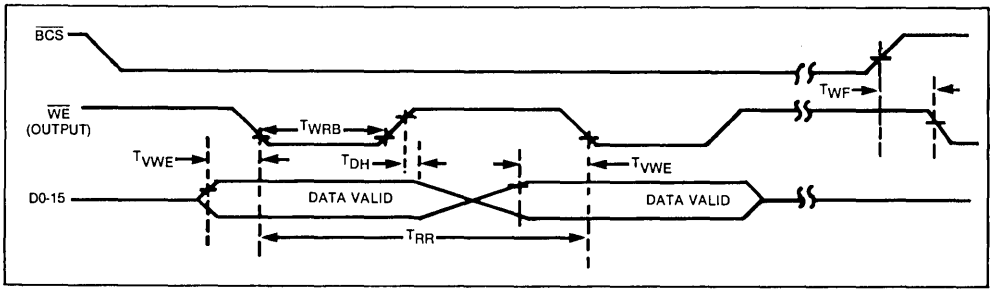
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
$^tSET\ 1$	ADDR, Set up to $\overline{RE}$	80		nsec	
$^tSET\ 2$	$\overline{CS}$ Set up to $\overline{RE}$	0		nsec	
^tDACC	Data Valid from $\overline{RE}$		375	nsec	C_L = 100pF
^tRC	Read Enable Pulse Width	.375	5.0	μsec	
^tDOH	Data Hold from $\overline{RE}$		150	nsec	
^tHLD	ADDR. $\overline{CS}$, Hold from $\overline{RE}$	0		nsec	
^tRDR	Read Recovery Time	500		nsec	



HOST WRITE TIMING

HOST WRITE TIMING

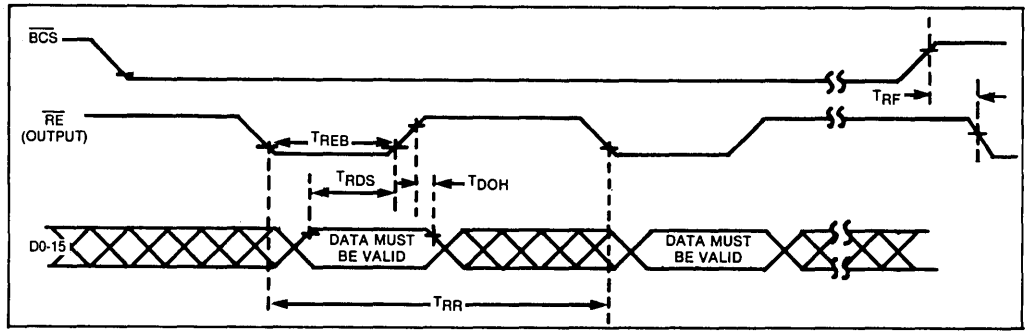
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
$^tSET_1$	ADDR, Set up to $\overline{WE}$	80		nsec	
$^tSET_2$	$\overline{CS}$ Set up to $\overline{WE}$	0		nsec	
^tDS	Data Bus Setup to $\overline{WE}$	100		nsec	
^tWE	Write Enable Pulse Width	200		nsec	
^tDH	Data Bus Hold from $\overline{We}$	80		nsec	
$^tHLD_1$	$\overline{CS}$ Hold from $\overline{WE}$	0		nsec	
$^tHLD_2$	ADDR Hold from $\overline{WE}$	30		nsec	
^tWER	Write Recovery Time	1.0		μsec	



BUFFER WRITE TIMING

BUFFER WRITE TIMING (READ SECTOR CMD)

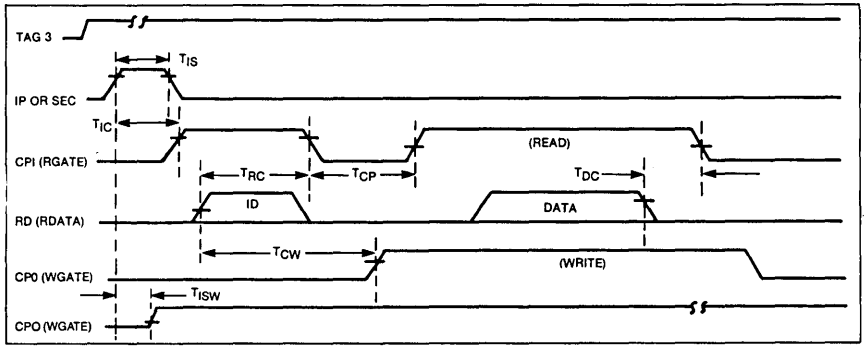
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
^tWRB	$\overline{WE}$ Output Pulse Width		4		SC	See Note 2
^tVWE	Data Set up to $\overline{WE}$		4		SC	See Note 2
^tDH	Data Hold from $\overline{WE}$		4		SC	See Note 2
^tRR	$\overline{WE}$ Repetition Rate		16		SC	See Note 2
^tWF	$\overline{WE}$ Float from $\overline{BCS}$			0	nsec	



BUFFER READ TIMING

BUFFER READ TIMING (WRITE SECTOR CMD)

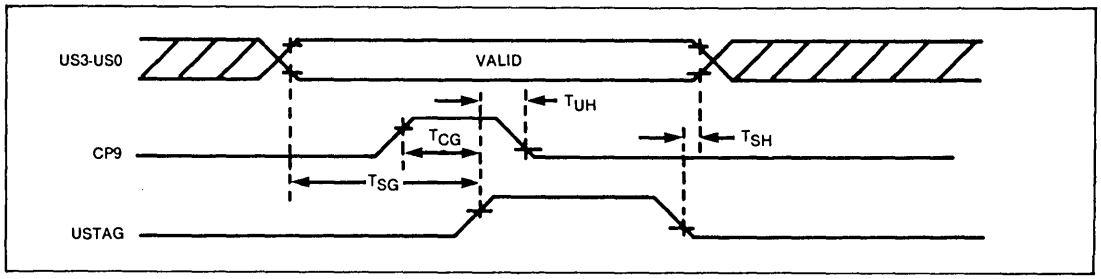
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
tREB	$\overline{RE}$ output Pulse Width		4		SC	See Note 2
tRDS	Data Setup to $\overline{RE}$	140			nsec	
tRR	$\overline{RE}$ Repetition Rate		16		SC	See Note 2*
tDOH	Data Hold From $\overline{RE}$	80			nsec	
tRF	$\overline{RE}$ Float from $\overline{BCS}$			0	nsec	



DISK R/W CONTROL TIMING

DISK R/W CONTROL TIMING (SCLK = 9.677 MHZ)

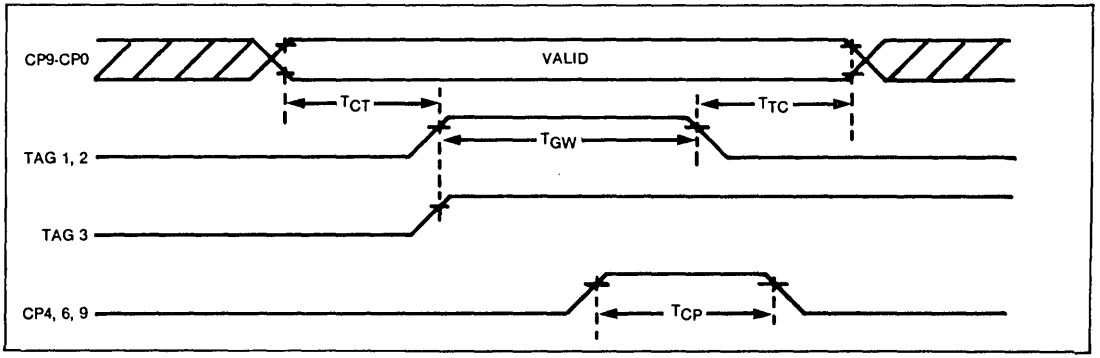
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
tIS	Index/Sector Pulse Width	.2	1.25	3.0	μsec	
tIC	Index/Sector to CP1 High		60		SC	See Note 3
tRC	CP1 Low from Read Data		56		SC	See Note 3
tCP	CP1 Low to CP1 High		12		SC	See Note 3
tDC	Last Read Data to CP1 Low		16		SC	See Note 3
tCW	CP0 High from Read Data		60		SC	See Note 3
tSW	Index/Sector High to CP0 High on FORMAT			250	nsec	



UNIT SELECT TIMING

UNIT SELECT TIMING (SCLK = 9.677 MHZ)

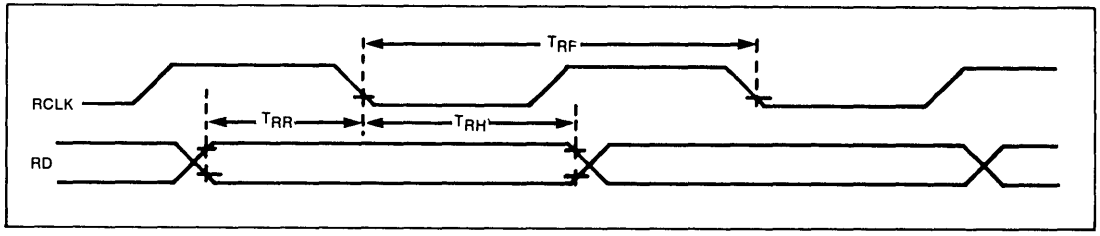
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
tSG	US3-US0 Setup to USTAG	1.0			μsec	
tCG	CP9 Setup to USTAG		4		CLK	See Note 4
tUH	CP9 Hold Time from USTAG		4		CLK	See Note 4
tSH	US3-US0 Hold Time from USTAG	1.0			μsec	



CP TAG TIMING

CP TAG TIMING 9SCLK = 9.677 MHZ)

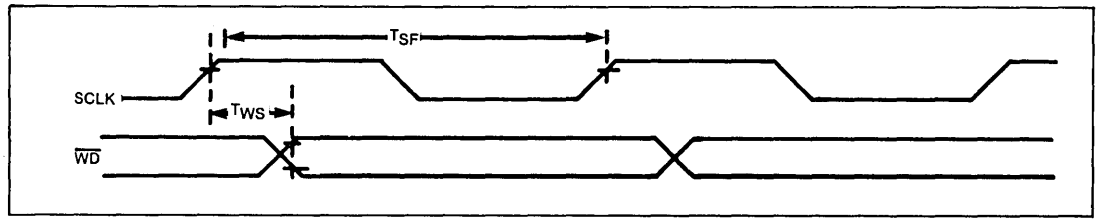
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
tCT	CP9-CP0 Set up to TAGS 1, 2, or 3		5		CLK	See Note 4
t6GW	TAGS 1 & 2 Pulse Width		4		CLK	See Note 4
tTC	CP9-CP0 Hold Time from TAG 1, 2 Low		2		CLK	See Note 4
tCP	CP4, 6, 9 Pulse Width During TAG 3 True		4		CLK	See Note 4



READ DATA TIMING

READ DATA TIMING

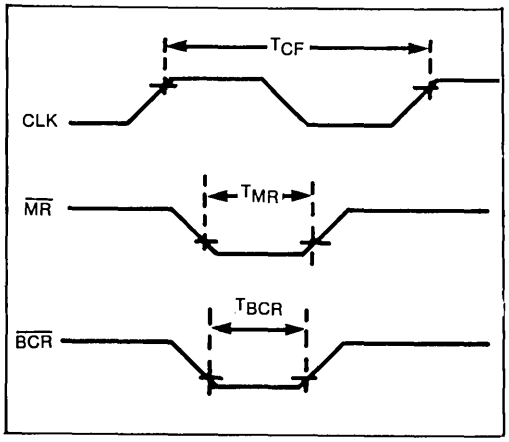
SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITIONS
^tRF	RCLK Frequency	1.0	9.677	10.1	MHZ	
^tRR	Read Data Setup to RCLK Low	35			nsec	
^tRH	Read Data Hold Time from RCLK Low	0			nsec	



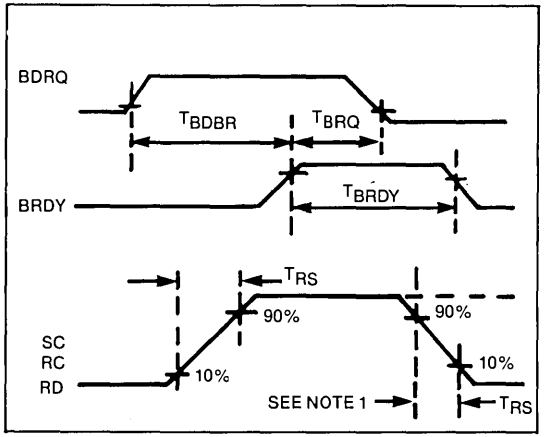
WRITE DATA TIMING

WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
^tSF	Servo Clock Frequency	1.0	9.677	10.1	MHZ	
^tWS	WD Valid from Servo Clock High			85	nsec	C_L = 15 pf. See Note 5



MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
$_tCF$	Master Clock Frequency		2.0	2.5	MHZ	50% Duty Cycle
$_tMR$	Master Reset Pulse Width	12			μsec	CLK Active
$_tBCR$	$\overline{BCR}$ Pulse Width		4		CLK	See Notes 4&7
$_tBRQ$	BDRQ Reset from BRDY	50		600	nsec	
$_tRS$	Rise of Fall Time			15	nsec	See Note 1
$_tBDBR$	BRDY High from BDRQ High	4				See Note 8
$_tBRDY$	BRDY Pulse Width	4				See Note 8

NOTES:

1. It is recommended to buffer the line receiver stage with a TTL or Schottky TTL stage on pins 27, 28 and 29. A current sink capability of 48 mA with a 100 ohm pull-up resistor will provide both the required rise and fall times and also the required voltage swing. It is recommended to locate these buffers physically near the WD 1050 to minimize inductive ringing.
2. Timing is a function of the Servo Clock (SCLK) frequency. The number of negative SCLK transitions plus 400 nsec. SCLK periods is specified. (Disregard "TYP" in this case).
3. Timing is a function of the Servo Clock (SCLK) frequency. The number of negative SCLK transitions plus 400 nsec. max. is specified. (Disregard the "TYP" in this case).
4. Timing is a function of the Master Clock (CLK) frequency. The number of CLK periods is specified. (Disregard the "TYP" in this case).
5. WD is an open drain output and requires an external 1K ohm pull-up to V_{CC}. This pin is inverted relative to the SMD interface cable. It is recommended that this output go to the 'D' input of a 74S74 flip-flop that is clocked by the SCLK buffer described in Note 1. The 74S74 Q output may then connect to the interface line driver. It is recommended that the 74S74 be located physically near the Wd1050.
6. All AC timing is measured at V_{OL} = 0.8 V, V_{OH} = 2.0V.
7. Certain occurrences of BCR can have variable pulse widths. Deactivation of $\overline{BCR}$ is dependent upon the next occurance of INDX or SCTR for these instances.
8. Timing is a function of the Master Clock (CLK) frequency. The number of CLK periods, plus 100 nsec. min. is specified.

WD1050 SMD Controller/Formatter Application Notes

INTRODUCTION

Prior to the introduction of 5¼ and 8 inch Winchester disks drives in the late 1970's, minicomputers and mainframes were the only systems that utilized rigid disks. These drives were relatively expensive; sometimes as high as $200 per megabyte. They offered the minicomputer designer a fixed or removable drive with capacities from 10 to 300 megabytes. Initially, there was no need for interface standards. IBM Corporation was the predominant leader in the marketplace, and anyone else who decided to build drives were IBM compatible units. But as competition increased, more and more companies began producing lower cost units with increased capacity. Minicomputer companies were being formed, offering complete systems that were non-IBM compatible. The disk drive race was on.

In order to standardize a common interface and to prevent product obsolescence, Control Data Corporation developed an intelligent interface called the Storage Module Device or SMD. This interface allowed a variety of drives to use the same hardware signals, even though their capacities and physical sizes differed. Variations of the SMD were also introduced. Some of these are the CMD (Cartridge Module Drive) and the MMD (Memory Module Drive). The SMD interface began to gain acceptance in the marketplace as competitive manufacturers offered "SMD-compatible" drives as well. The SMD was well on its way to becoming a defacto standard in the industry. Its longevity has been proved by over 10 years worth of product based on this "intelligent" interface.

With today's smaller diameter low cost drives, where does SMD stand? Oddly enough, the higher capacity 5¼ and 8 inch Winchesters are reviving the SMD protocol. Because the SMD interface offers several advantages over the ST506 type interface in the high capacity arena (such as parallel seek instead of serial step pulses), several manufacturers are planning to offer the SMD on their traditional small system disk drives. The SMD, however, is not a trivial interface when it comes down to designing a controller.

A LOOK AT THE SMD

Figure 1 illustrates the electrical signals of the SMD. Two separate cables are used: one for control and one for data. The control cable (commonly referred to as the "A" cable) is responsible for all head movement, status reportings and issuing commands. The data cable (or "B" cable) is used for reading and writing NRZ data to a particular sector on the drive. Note that all lines on both cables are differential signals; they require a differential driver/receiver at both ends.

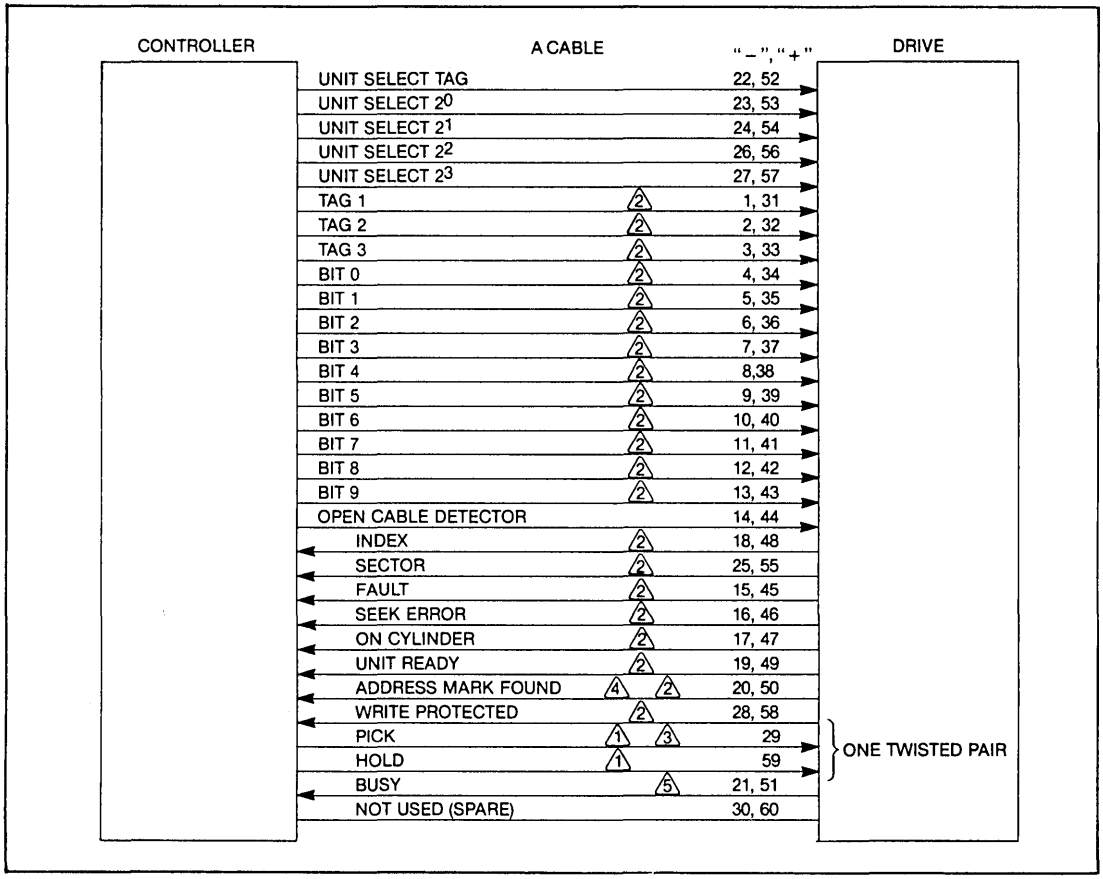
Primary control over the "A" cable is based upon a 10 bit bus called the Tag Bus. These 10 lines send particular information to the driver and initiate a command. Three Tag lines (Tag 1-3) are used to tell the drive what the bus contains during the strobing of the Tags. For example, Tag 1 tells the drive that the Tag bus contains a cylinder number that the head assemblies should be moved to for reading or writing. Tag 2 tells the drive the Head/Volume to select, while Tag 3 is used to initiate read or write commands and to perform special recovery routines.

Drives are selected by separate UNIT SELECT lines on the "A" cable, which have their own strobe line called Unit Select Tag. Other signals on the "A" cable serve status reporting type functions. SEEK ERROR and ON CYLINDER are examples of status lines.

The "B" cable is used to transmit serial, NRZ data to and from the drive. Associated with the R/W lines are clocks: Write Clock for write recovery and Read Clock for read recovery. Additional signals aid in determining the status of each drive on the bus.

In a multiple drive configuration, the two cables are connected as shown in Figure 2. The "A" cable is daisy-chained; each drive is tied together in parallel with termination resistors on the last drive. The "B" cable is radial-connected; a separate cable from each drive connects to the controller.

It is probably obvious by now that a great deal of control is necessary to perform even a simple Read or Write operation on the SMD Bus. The drive controller must perform simultaneous operations on both cables, as well as monitoring status signals to determine successful execution of operation. A typical SMD controller can consist of 150 SSI/MSI Integrated Circuits and a local microprocessor or bit-slice to perform the necessary functions. SMD controller designers of today can take advantage of a new LSI chip that will reduce the number of I.C.'s to well under 40.



NOTE: 60 Position
30 Twisted pair-straight flat cable
Maximum Length-100 ft. (30.48 meters)

1 Special signal, not a balanced transmission signal
2 Gated by unit selected
3 Not interpreted, is Daisy chained, no driver connection within the LMD
4 Not activated, is Daisy chained, always a logic zero output if unit is selected
5 Not generated, is Daisy chained, no driver connection within the LMD

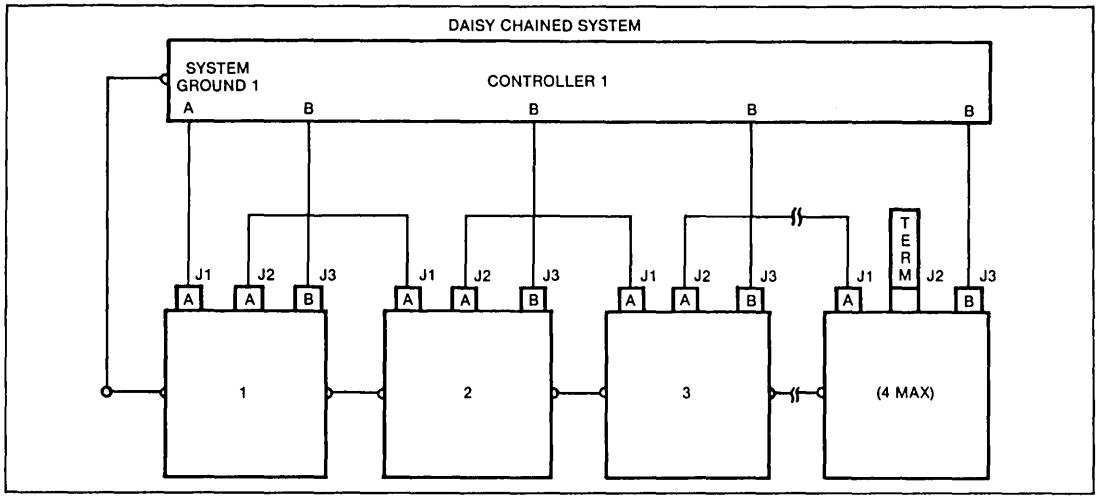
Figure 1(A). Tag Bus I / O Interface ("A" Cable)

CONTROLLER	"B" CABLE	"−","+"	DRIVE
	WRITE DATA	8, 20	
	GROUND	7	
	WRITE CLOCK	6, 19	
	GROUND	18	
	SERVO CLOCK	2, 14	
	GROUND	1	
	READ DATA	3, 16	
	GROUND	15	
	READ CLOCK	5, 17	
	GROUND	4	
	SEEK END	10, 23	
	UNIT SELECTED	22, 9	
	GROUND	21	
	INDEX	12, 24	
	GROUND	11	
	SECTOR	13, 26	
	GROUND	25	

NOTES:
1. 26 conductor flat cable.
   Maximum Length–50 ft. (15.24 meters)
2. No signals gated by "A" cable unit select

Figure 1 (B). "B" Cable Interface

NOTES:
1. Maximum individual A cable lenghts = 100 feet (30.48 meters)
2. Maximum individual B cable lenghts = 50 feet (15.24 meters)



NOTES:
1. Termination of "A" cable lines are required at controller and the last unit of the Daisy chain or each unit in a radial configuration.
2. Termination of "B" cable receiver lines are required at the controller and are on the unit' receiver cards.
3. Maximum cumulative "A" cable length per controller = 100 feet (30.48 meters) maximum individual "B" cable lenght = 50 feet (15.24 meters).

Figure 2. Daisy Chained System

WD1050 SMD CONTROLLER CHIP

Western Digital Corporation offers an LSI controller chip for the SMD protocol. This device, called the WD1050, has been designed to interface an SMD rigid disk drive to a 16-bit Host processor. A set of macrocommands allows the Host to request a specific operation such as seek, read, etc., in which all Tag and control lines on the drive interface perform their appropriate signaling. By using this device, the designer is free to concentrate on operating system software intervention, rather than meeting electrical requirements of the drive protocol. Figure 3 shows the Block Diagram of the WD1050. Data or commands are entered in 16-bits through the Data I/O Buffers. This information is stored in the Task File and tells the device parameters about a specific command. This could be a cylinder address, a sector number to search for, a particular drive that should be selected, etc. After this information is loaded, a command is issued. The Control Unit instructs the various pins on the drive interface to generate their proper signals. Upon completion of a command, the WD1050 interrupts the Host and reports via the status register if any errors were encountered. The device is then ready for the next command.

Figure 4 illustrates the Task File and its contents. The Host processor generates the three address lines shown, then performs a read or write operation to the selected 16-bit register. All registers can be read or written to with the exception of the Command/Status Register. Since both of these registers share a common address location, a "write" will cause a command to execute, while a "read" will cause the status to be fetched from the device. This memory mapped architecture allows the Host to randomly access any location in the Task File without disrupting or reloading the data in other registers.

The Instruction Set of the WD1050 is shown in Figure 5. Return to Zero, and Seek Cylinder commands are used for head movement, while the remaining commands are responsible for reading or writing data. Each Read/Write command also contains an "Implied Seek" feature. This allows the Host processor to issue a read or a write function even though the heads are sitting over the wrong cylinder. The WD1050 will perform an automatic seek operation

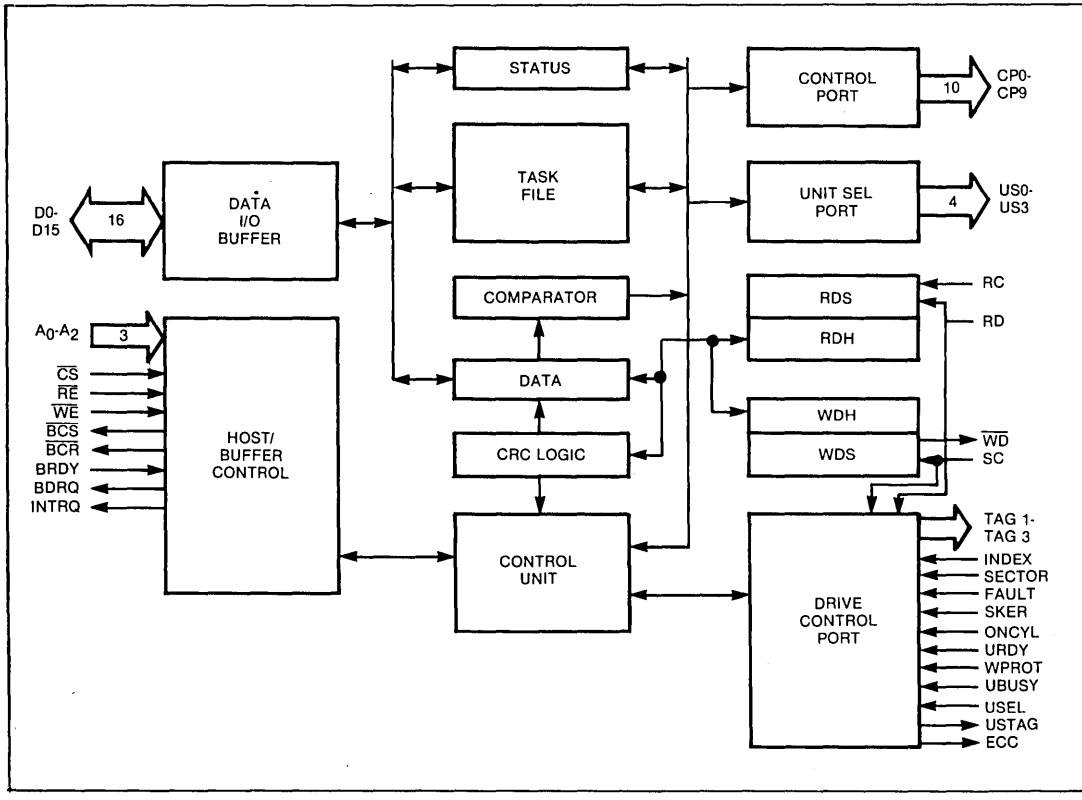


FIGURE 3. WD1050 BLOCK DIAGRAM

before the actual read or write. Because of this, the head movement commands (Return to Zero and Seek Cylinders) are usually restricted for use in overlap seeks. This is the ability to perform seek operations on several drives simultaneously.

After a command has finished execution, the WD1050 will report to the Host through its Status Register (shown in Figure 6) how successful a command execution was. Many commands will not execute if certain conditions are not met. For example, a FAULT condition, shown by status bit 6, will prevent all commands except Fault Clear from executing. Read / Write commands will not execute if the "On Cylinder" bit is false, either. In summary, the Host must examine the various bits to determine what action to take next.

HOST SECTOR BUFFER

Because of the high data rates used on the SMD protocol (9.677 Mbits / sec.), even a fast micro- processor will have trouble keeping up in a Programmed I / O environment. For this reason, the WD1050 has been designed to use a sector buffer.

Figure 7 shows a Host Interface to the device using a low cost Static RAM and a binary counter. Since the WD1050 will be transferring data directly to the RAM, a transceiver will be needed to isolate the Host from the RAM / WD1050 logic. This transceiver, as shown in Figure 7, is disabled by Buffer Chip Select (BCS). Whenever BCS is active, the WD1050 is reading or writing to the RAM. During this condition, the Host cannot read status or any other registers. When the data transfer is over, the device disables BCS and enables Buffer Data Request (BDRQ). This tells the Host that the buffer is now available for use. If a read command had been issued, the sector buffer would have filled the data requested.

During this process, the WD1050 takes control over Write Enable ($\overline{WE}$) by making it an output. It places its first data word on the bus and strobes $\overline{WE}$. This causes a write operation to the RAM and increments the binary counter that is tied to the RAM's address lines. Another $\overline{WE}$ strobe then occurs, increments the counter again, and the process continues until the sector is transferred. If a single sector operation was requested, the WD1050's use of the sector buffer is completed. However, multiple sectors may be transferred as an option within the command. In this case, the Buffer Ready (BRDY) input to the device is examined. If false, the WD1050 assumes there is more RAM available and transfers the next sector of data. The BRDY signal is normally generated by a "carry" or overflow out of the binary counter. If BRDY has gone active but the device still has more sectors to transfer, BDRQ will be made active to allow the Host to unload the data in the RAM, making room for the additional sectors. The WD1050 will then resume its operation of finding a sector and writing the data to the buffer. After all the data has been transferred, the command will terminate. To complete the scheme, a signal called Buffer Counter Reset (BCR) is used to zero the counters before the Host or device starts a transfer. A BCR pulse is generated whenever BCS makes a transition.

By using this buffer scheme, the designer has the ability with one command to transfer the maximum number of sectors specified by the Sector Counter in the SDH Register.

CONCLUSION

Using the WD1050 as the basis for an SMD controller design, can reduce the complexity of the design effort considerably. However, challenges still remain in interfacing the device to maximize the efficiency of the interface. The buffer control signals, for example, can be changed to accomodate a DMA controller for higher throughput. ECC can be appended to the buffer for data correction purposes. A local microprocessor dedicated on the SMD controller board could even be used to emulate existing SMD / Host software routines.

Regardless of the application, the WD1050 signifies a trend in the semiconductor industry to not only replace logic in a discrete design, but to offer complete functions in large scale integration. This device is certainly not the first to offer an LSI functional building block, and will not be the last.

A2	A1	A0	REGISTER SELECTED
0	0	0	Head Number/Sector Address
0	1	0	Sector Count/Length/Unit Address
1	0	0	16 Bit Cylinder Register
1	1	0	Command Register (Write Only)
1	1	1	Status Register (Read Only)

Figure 4. WD1050 Task File

COMMAND	LSB				COMMAND REGISTER BITS											MSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fault Clear	1	0	0	0	0	0	0	I	0	0	0	0	U	S	E	L
Return to Zero	1	0	0	1	V	L	O	I	0	0	0	M	U	S	E	L
Seek Cylinder	1	0	1	0	V	L	O	I	Z	C	H	M	U	S	E	L
Read ID Field	1	0	1	1	R	L	O	I	Z	C	H	M	U	S	E	L
Read Sector	1	1	0	0	R	L	O	I	Z	C	H	M	U	S	E	L
Write Sector	1	1	0	1	R	L	O	I	Z	C	H	M	U	S	E	L
Format	1	1	1	0	R	P	O	I	Z	C	H	M	U	S	E	L
Verify	1	1	1	1	R	P	O	I	Z	C	H	M	U	S	E	L

FLAG SUMMARY	
V = Verify	I = Interrupt Enable
R = CRC Enable	Z = Volume/Head change
L = Logical Sectoring	C = Cylinder Address
P = Programmable Sectors	H = Head Selection
O = On Cylinder	M = Marginal Data Recovery
E = Priority Release/Early	U = Unit Sel/Servo Minus
L = Unit Deselect/Late	S = Priority Sel/Servo Plus

Figure 5. WD1050 Instruction Set

BIT	NAME	DESCRIPTION
0	ID Field Not Found (ID/NF)	Set if the sync character preceding the ID Field or ID Field contents read from the disk do not match the respective Task File contents.
1	ID CRC Error (IDCE)	Set if the CRC calculation on the ID Field read from the disk is in error.
2	Data Field Not Found (DFNF)	Set if the Data Field sync pattern following the ID Field does not match the sync character.
3	Data Field CRC Error (DFCE)	Set if the CRC Calculation on the Data Field read from the disk is in error.
4	Not Used	This bit is not used; it is forced to a zero.
5	Buffer Data Request (BDRQ)	Reflects the Buffer Data Request output.
6	Fault (FLT)	Reflects the status of the Fault (FLT) input.
7	Buffer Chip Select (BCS)	This bit is an inverted copy of the Buffer Chip Select ($\overline{BCS}$) output.
8	Seek Error (SKER)	Reflects the status of the Seek Error (SKER) input.
9	On Cylinder (OCYL)	Reflects the status of the On Cylinder (OCYL) input.
10	Unit Ready (URDY)	Reflects the status of the Unit Ready (URDY) input.
11	Write Protect (WPRT)	Reflects the status of the Write Protect (WPRT).
12	Unit Selected (USEL)	Reflects the status of the Unit Selected (USEL) input.
13	Unit Busy (UBSY)	Reflects the status of the Unit Busy (UBSY) input.
14	CIP	Set when a command is in progress.
15	Buffer Chip Select (BCS)	This bit is an inverted copy of the Buffer Chip Select ($\overline{BCS}$) output. This bit also appears in STATUS Bit 7.

Figure 6. WD1050 Status Register

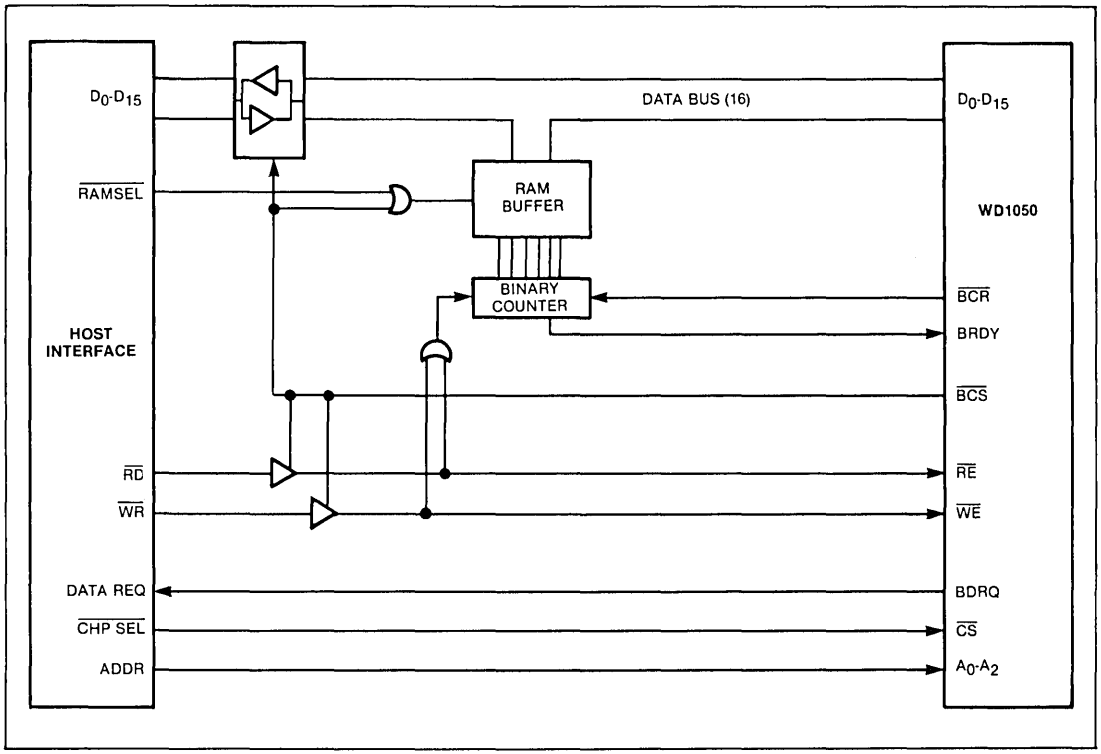


Figure 7. WD1050 Host Interface

WD1100 Series Winchester Controller Chips

DESCRIPTION

The WD1100 Chip series provides a low cost alternative for developing a Winchester Controller. These devices have been designed to read and convert an MFM data stream into 8-bit parallel bytes. During a write operation, parallel data is converted back into MFM to be written on the disk. Address Marks are generated and detected while CRC bytes can be appended and checked on the data stream. The WD1100 is fabricated in N-channel silicon gate technology and is available in a 20-pin Dual-In-Line package.

- WD1100-01 SER/PARALLEL CONVERTER
- WD1100-02 MFM GENERATOR
- WD1100-12 IMPROVED MFM GENERATOR
- WD1100-03 AM DETECTOR
- WD1100-04 CRC GENERATOR/CHECKER
- WD1100-05 PAR/SERIAL CONVERTER
- WD1100-06 ECC/CRC LOGIC
- WD1100-07 HOST INTERFACE LOGIC
- WD1100-09 DATA SEPARATION SUPPORT LOGIC

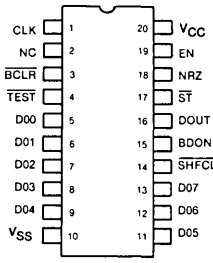
FEATURES

- SA1000/ST506 COMPATIBLE
- SINGLE 5V SUPPLY
- TRI-STATE DATA LINES
- 5 MBITS/SEC TRANSFER RATE
- SIMPLIFIED INTERCONNECT

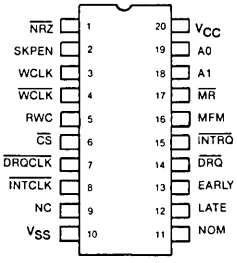
APPLICATIONS

Winchester Controllers for:

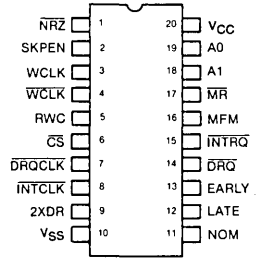
- SHUGART ASSOCIATES
- SEAGATE TECHNOLOGY
- QUANTUM CORP.
- TANDON MAGNETICS
- MINISCRIBE
- RMS
- CMI . . . AND OTHERS



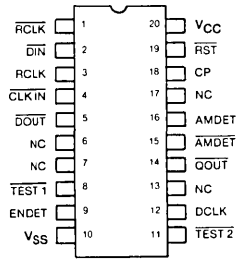
WD1100-01
SERIAL/PARALLEL CONVERTOR



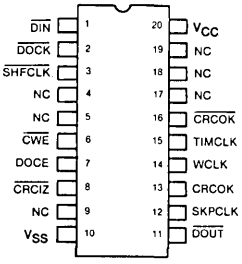
WD1100-02
MFM GENERATOR



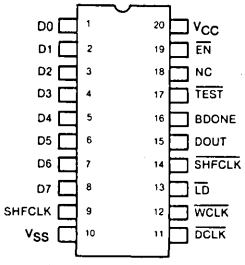
WD1100-12
IMPROVED MFM GENERATOR



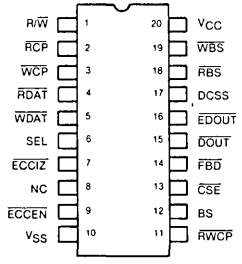
WD1100-03
AM DETECTOR



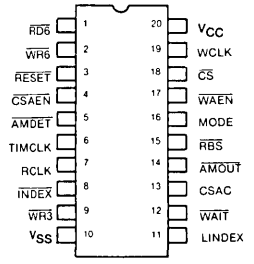
WD1100-04
CRC GENERATOR/CHECKER



WD1100-05
PARALLEL/SERIAL CONVERTER



WD1100-06
ECC/CRC LOGIC



WD1100-07
HOST INTERFACE LOGIC

WD1100-01 Serial/Parallel Converter

DESCRIPTION

The WD1100-01 Serial/Parallel Converter allows the user to convert NRZ (non-return to zero) data from a Winchester disk drive into 8-bit parallel form. Additional inputs are provided to signal the start of the parallel process, as well as Byte Strobes to signify the end of the conversion. The device contains two sets of 8-bit registers; one register may be read (in parallel), while data is being shifted into the other register. This double-buffering allows the Host to read data from the disk drive at one-eighth the actual data rate.

The WD1100-01 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5MBITS/SEC SHIFT RATE
- SERIAL IN/SERIAL-PARALLEL OUT
- 20 PIN DIP PACKAGE

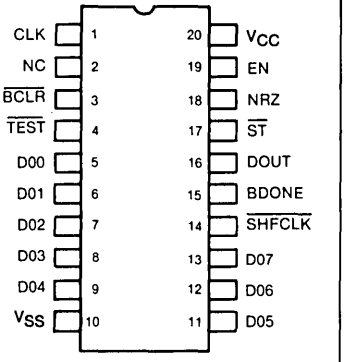


Figure 1.
WD1100-01 Pin Connections

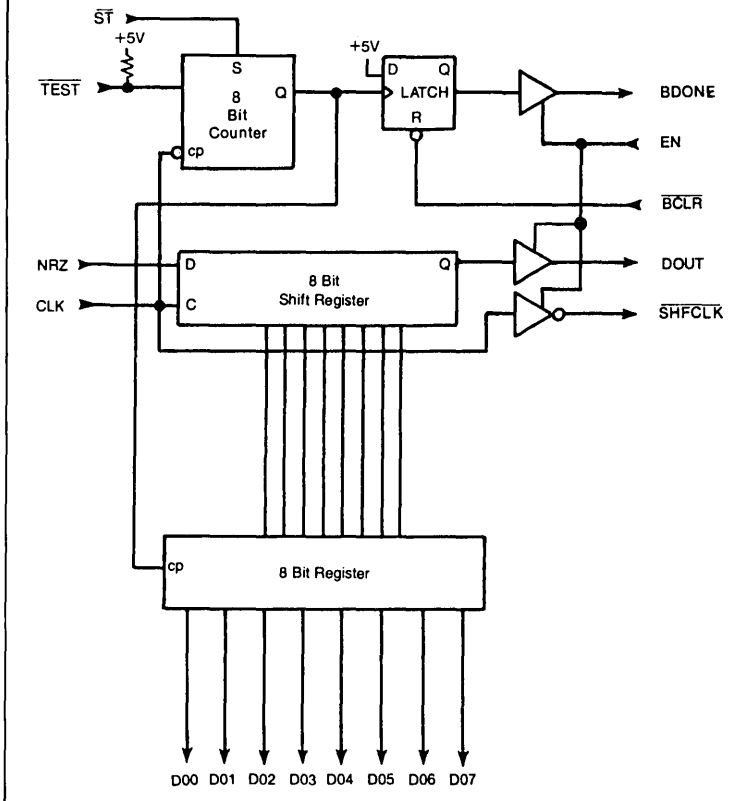


Figure 2.
WD1100-01 Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	CLK	CLOCK	NRZ data is entered into the 8-bit shift register on the low-to-high transition of clock.
2	NC	NO CONNECTION	No connection. This pin is to be left open by the user.
3	$\overline{BCLR}$	$\overline{BYTE\ CLEAR}$	When this line is at a logic 0, the BDONE (Pin 15) line is held reset.
4	$\overline{TEST}$	$\overline{TEST\ INPUT}$	This pin must be left open by the user.
5-9 11-13	D00-D07	DATA0-DATA 7	8 bit parallel data outputs.
10	V_{SS}	GROUND	Ground.
14	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	Inverted copy of CLOCK (pin 1) which is active when EN (pin 19) is at a logic 1.
15	BDONE	BYTE DONE	This signal is forced to a logic 1 signifying 8 bits of data have been assembled. BDONE remains in a logic 1 state until reset by a logic 0 on the BCLR (pin 3) line.
16	DOUT	DATA OUT	Serial Data Output from the 8th stage of the internal shift register. DOUT is in a high impedance state whenever EN (pin 19) is at a logic 0.
17	$\overline{ST}$	$\overline{START}$	This line enables the byte counter and is used for synchronization. It must be held to a logic 1 prior to first data bit on the NRZ (pin 18) line.
18	NRZ	NRZ DATA	NRZ serial data is entered on this pin and clocked by the low to high transition of CLK (pin 1).
19	EN	ENABLE	When this signal is at a logic 0, DOUT, $\overline{SHFCLK}$, and BDONE outputs are in a high impedance state.
20	V_{CC}	V_{CC}	$+5V \pm 10\%$ power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the WD1100-01 must be synchronized to the data stream. The $\overline{ST}$ line (Pin 17 high) is used to hold the internal bit counter in a cleared state until valid data (NRZ) and clocks (CLK) are entered. The $\overline{ST}$ line is a synchronous input and therefore requires one full cycle of the CLK line (Pin 1) to occur in order to accept a $\overline{ST}$ condition. After this happens, the device is ready to perform serial to parallel conversions.

Data is entered on the NRZ line and clocked into the 8-bit shift register on the low-to-high transition of CLK. The $\overline{ST}$ line must be set low during the low time of CLK. Data is accepted on low-to-high transition of the clock while the high-to-low transition of CLK increments the bit counter. After 8 data bits have been entered the final high-to-low transition of CLK sets an internal latch tied to the BDONE line (Pin 15). At the same time, the contents of the shift register are parallel loaded into an 8 bit register making the parallel data available on the D00-D07 outputs. BDONE will remain in a latched state until the $\overline{BCLR}$ is set to a logic 0, clearing off the BDONE signal. $\overline{BCLR}$ is a level triggered input and must be set back to a logic 1 before the next 8 bits are shifted through the register. $\overline{BCLR}$ has no effect on the serial shifting process. When the next 8 bits are received, BDONE will again be set and the operation continues.

When interfacing to a microprocessor, BDONE is used to indicate a parallel byte is ready to be read. As the processor reads the data out of the D00-D07 lines, the $\overline{BCLR}$ line should be strobed to clear of BDONE in anticipation of the next assembled byte. An address decode signal generated at the host may be used for this purpose. During a power-up condition, the state of BDONE is indeterminant. It is recommended that $\overline{BCLR}$ be strobed low after power-up to insure that BDONE is cleared.

The serial output line from the last stage of the shift register is available on the DOUT pin. An inverted copy of CLK is available on the $\overline{SHFCLK}$ pin. Both DOUT (Pin 16) and $\overline{SHFCLK}$ (Pin 14) can be used to drive another shift register external to the device.

The three signals BDONE, DOUT, and $\overline{SHFCLK}$ can be placed in a high impedance state by setting EN (Pin 19) to a logic 0. Likewise, EN must be at a logic 1 in order for these signals to be active.

The $\overline{TEST}$ pin is internally OR'ed with the $\overline{ST}$ line to inhibit the bit counter. It is recommended that $\overline{TEST}$ be left open by the user. An internal pull-up resistor is tied to this pin to satisfy the appropriate logic level required internally for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias .....0°C (32°F) to 50°C (122°F)
Voltage on any pin
with respect to V_{SS} .....−0.2V to +7.0V
Power Dissipation.....1 Watt
STORAGE TEMPERATURE
PLASTIC ...−55°C (−67°F) to +125°C (257°F)
CERAMIC ..−55°C (−67°F) to +150°C (302°F)

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = + 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_O	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All Outputs Open
I_{IH}	Input High			<10	μA	V_{IN} = .4 to V_{CC}
I_{IL}	Input Low			<10	μA	V_{IN} = .4 to V_{CC}

AC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F), V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
f_{CL}	CLK FREQUENCY	0		5.25	MHZ	
t_{LS}	↓CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{HS}	↑CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{DS}	Data set-up to ↑ CLK	15			nsec	
t_{VB}	BDONE valid from ↓ CLK	65		140	nsec	EN = 1
t_{RS}	BDONE reset from $\overline{BCLR}$			135	nsec	EN = 1
t_{BW}	$\overline{BCLR}$ Pulse Width	50			nsec	EN = 1
t_{SC}	↑ CLK to ↓ $\overline{SHFCLK}$			90	nsec	EN = 1
t_{CS}	↓ CLK to ↑ $\overline{SHFCLK}$			90	nsec	EN = 1
t_{SD}	Data delay from ↑ $\overline{SHFCLK}$			55	nsec	EN = 1
t_{FO}	Enable to DOUT ACTIVE			90	nsec	
t_{DH}	Data Hold w.r.t. ↑ CLK	45			nsec	
t_{CD}	↑ CLK to DOUT ACTIVE			145	nsec	
t_{OF}	Enable to DOUT disable			90	nsec	

NOTE: 1. Typical Values are for T_A = 25°C (77°F) and V_{CC} = +5V ± 10%

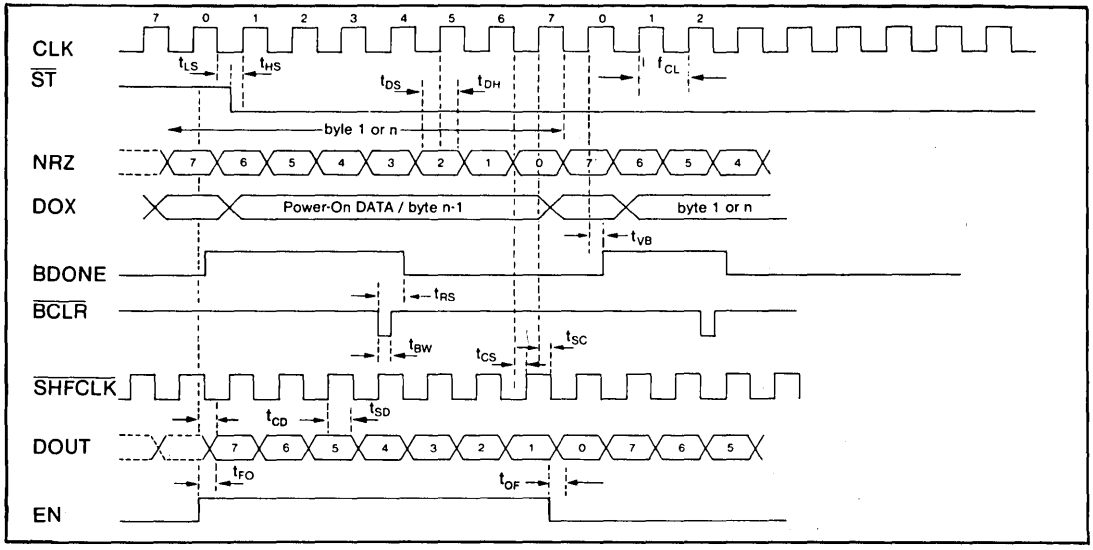


FIGURE 3. WD1100-01 FUNCTIONAL TIMING

WD1100-03 AM Detector

DESCRIPTION

The WD1100-03 Address Mark Detector provides an efficient means of detecting Address Mark Fields in an MFM (NRZ) data stream. MFM (NRZ) clocks and data are fed to the device along with a window clock generated by an external data separator. The WD1100-03 searches the data stream for a DATA = A1, CLK = 0A pattern and produces an AM DET signal when the pattern has been found. NRZ data is an output from the device, which can be used to drive a serial/parallel converter. An uncommitted latch is also provided for by the data separator circuitry, if required.

The WD1100-03 Address Mark Detector is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- 5 MBITS/SEC DATA RATE
- DECODES $A1_{16}$ $0A_{16}$
- SYNCHRONOUS CLOCK/DATA OUTPUTS
- 20 PIN DIP PACKAGE

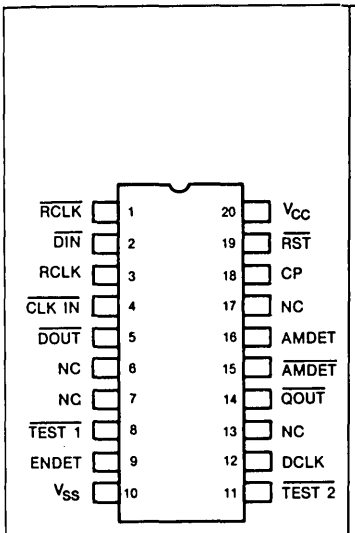


Figure 1.
WD1100-03 Pin Connections

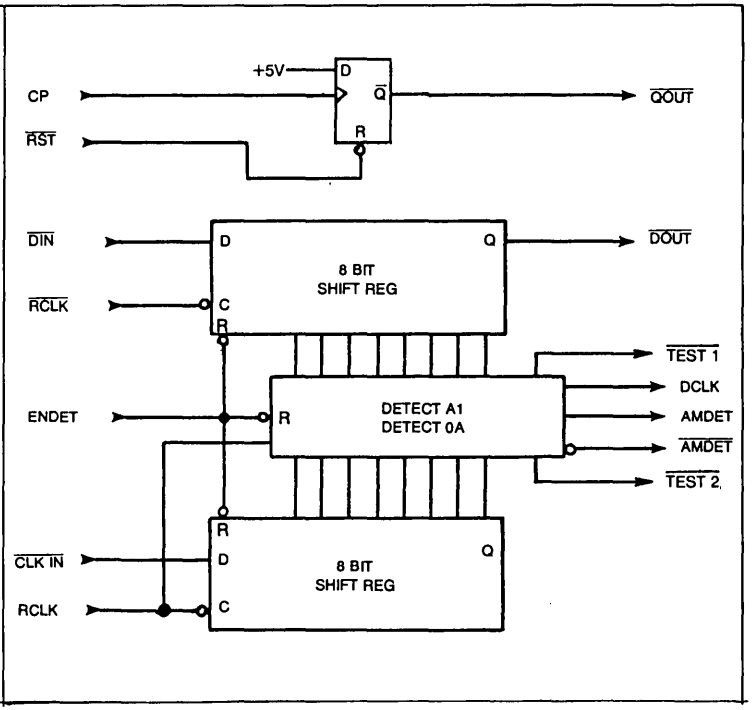


Figure 2.
WD1100-03 Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1 3	$\overline{RCLK}$ RCLK	$\overline{READ\ CLOCK}$ READ CLOCK	Complimentary clock inputs used to clock DIN and $\overline{CLK\ IN}$ into the AM detector.
2	$\overline{DIN}$	$\overline{DATA\ INPUT}$	MFM data pulses from the external Data Separator are connected on this line.
4	$\overline{CLK\ IN}$	$\overline{CLOCK\ INPUT}$	MFM clock pulses from the external Data Separator are connected on this line.
5	$\overline{DOUT}$	$\overline{DATA\ OUTPUT}$	Data Output from the internal Data Shift register, synchronized with DCLK.
6,7,13,17	NC	No Connection	To be left open by the user.
8 11	$\overline{TEST\ 1}$ $\overline{TEST\ 2}$	$\overline{TEST\ 1}$ $\overline{TEST\ 2}$	To be left open by the user.
9	ENDET	ENABLE DETECTION	A logic 1 on this line enables the detection logic to search or a data $A1_{16}$ and clock.
10	V_{SS}	V_{SS}	Ground.
12	DCLK	DATA CLOCK	Clock output that is synchronized with $\overline{DATA\ OUT}$ (Pin 5).
14	$\overline{QOUT}$	$\overline{LATCH\ OUTPUT}$	Signal output from the uncommitted latch.
15 16	$\overline{AMDET}$ AMDET	$\overline{ADDRESS\ MARK\ DETECT}$ ADDRESS MARK DETECT	Complimentary Address Mark Detector output. These signals will go active when a Data = $A1_{16}$ Clock = $0A_{16}$ pattern is detected in the data stream.
18	CP	CLOCK PULSE	A low-to-high transition on this line will cause the $\overline{QOUT}$ (Pin 14) to be latched at a logic 0.
19	$\overline{RST}$	$\overline{RESET}$	A logic 0 on this line will cause the $\overline{QOUT}$ (Pin 14) signal to be set at a logic 1.
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the internal logic must be initialized. While the ENDET (Pin 9) line is at a logic 0, shifting of data will be inhibited and $\overline{AMDET}$, AMDET, $\overline{CLK}$, and $\overline{DATA\ OUT}$ will remain inactive.

When ENDET is at a logic 1, shifting is enabled. NRZ data is entered on the $\overline{DIN}$ line (Pin 2) and shifted on the high-to-low transition of $\overline{RCLK}$ (Pin 1). NRZ clocks are entered on the $\overline{CLK}$ IN line, and shifted on the high-to-low transition of RCLK (Pin 3). The $\overline{DOUT}$ line (Pin 5) is tied to the last stage of the internal Data Shift register and will reflect information clocked into the $\overline{DIN}$ line delayed by 8 bits.

While each bit is being shifted, a 16 bit comparator is continuously checking the parallel contents of the shift registers for the DATA = $A1_{16}$, CLK = $0A_{16}$ pattern. When this pattern is detected, $\overline{AMDET}$ will be set to a logic 0 and AMDET will be set to a logic 1. $\overline{AMDET}$ and AMDET will remain latched until the device is reinitialized by forcing ENDET to a logic 0.

When an AM is detected, DCLK will begin to toggle. Data present on the $\overline{DOUT}$ line may then be clocked into an external serial / parallel converter. DCLK will remain inactive when ENDET is held at a logic 0.

An uncommitted edge-triggered flip / flop has been provided to facilitate the detection of high frequency by the data separator, but may be used for any purpose. The low-to-high transition of CP (Pin 18) will set the $\overline{QOUT}$ (Pin 14) to a logic 0. $\overline{QOUT}$ may be reset back to a logic 1 by a low level on the $\overline{RST}$ line (Pin 19).

$\overline{TEST\ 1}$ and $\overline{TEST\ 2}$ are output lines. $\overline{TEST\ 1}$ is an active low pulse when an $A1_{16}$ is detected, and $\overline{TEST\ 2}$ is active low pulse when a $0A_{16}$ is detected. These signals are used for test points and therefore should be left open by the user if not required.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias ..... 0°C (32°F) to 50°C (122°F)
Voltage on any pin with respect to V_{SS} ..... -0.2 to +7.0V
Power Dissipation ..... 1 Watt

STORAGE TEMPERATURE
PLASTIC ..... -55°C to +125°C
CERAMIC ..... -55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F), V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	-0.2		0.7	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -200 A
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All Outputs Open
I_{IH}	Current Input High			10	uA	V_{IN} = .4 to V_{CC}
I_{IL}	Current Input Low			10	uA	V_W = .4 to V_{CC}

AC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F), V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
f_{RC}	RCLK FREQUENCY			5.25	MHz	
t_{ST}	Data, CLKIN, RCLK Setup Time	40			nsec	
t_{HT}	Data, CLKIN, RCLK Hold Time	40			nsec	
t_{RD}	↓ $\overline{RCLK}$ to ↑ DCLK			140	nsec	
t_{EM}	ENDET set to AMDET, DOUT, DCLK			100	nsec	
t_{RA}	↓ $\overline{RCLK}$ to ↑ $\underline{AMDET}$			115	nsec	
t_{RM}	↓ $\overline{RCLK}$ to ↓ $\underline{AMDET}$			125	nsec	
t_{RO}	↓ $\overline{RCLK}$ to $\overline{DOUT}$			135	nsec	
t_{EA}	↓ $\underline{ENDET}$ to AMDET, DOUT, DCLK			190	nsec	
t_{RQ}	↓ $\overline{RST}$ to ↑ $\overline{QOUT}$			110	nsec	
t_{RW}	Pulse width of $\overline{RST}$	50			nsec	
t_{CW}	CP Pulse $\underline{width}$	90			nsec	
t_{CQ}	↑ CP to ↓ $\overline{QOUT}$			120	nsec	

NOTE: 1. Typical Values are for T_A = 25°C and V_{CC} = +5V.

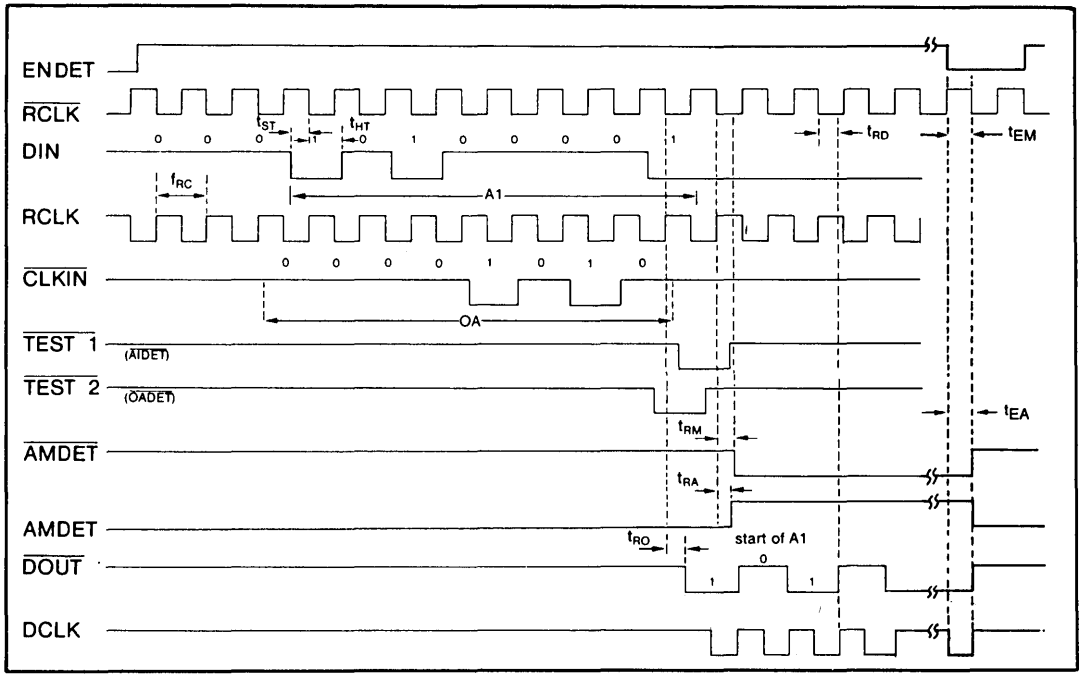


Figure 3. WD1100-03 Functional Timing

WD1100-04 CRC Generator/Checker

DESCRIPTION

The WD1100-04 CRC Generator / Checker is designed to generate a Cyclic Redundancy Checkword from a serial data stream, and to check a data stream against a known CRC word. Complimentary latched "CRCOK" outputs are provided to indicate CRC errors in check mode. Additional logic has been included to shift the CRC checkword out of the device by signals generated on other WD1100 family devices.

The WD1100-04 is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- GENERATES / CHECKS CRC
- SINGLE +5V SUPPLY
- LATCHED ERROR OUTPUTS
- $X^{16} + X^{12} + X^5$ 1(CCITT-16)
- AUTOMATIC RESET
- 20 PIN DIP PACKAGE

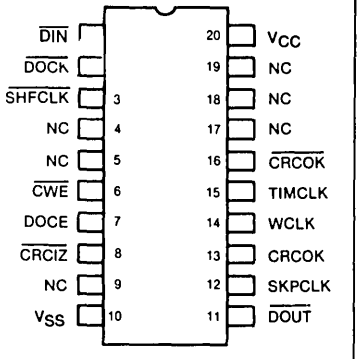


Figure 1.
WD1100-04 Pin Connections

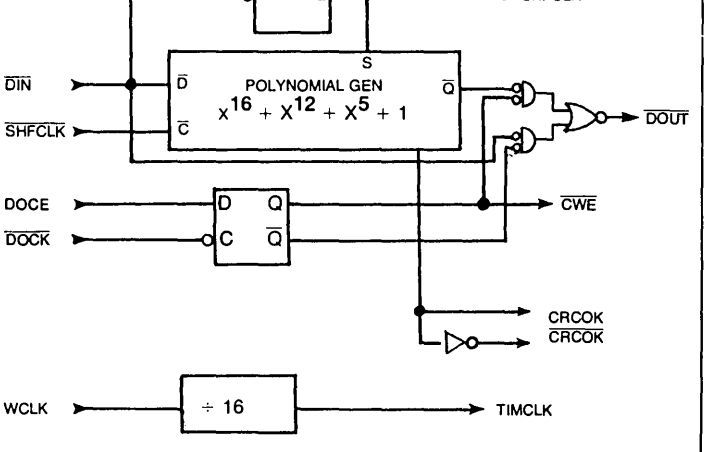


Figure 2.
WD1100-04 Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{DIN}$	$\overline{DATA\ INPUT}$	Active low serial input data stream is used to generate/check the 2 byte CRC word.
2	$\overline{DOCK}$	$\overline{DATA\ OR\ CRC\ WORD\ CLOCK}$	After a byte of data has been transferred in, this input signal is used to latch the state of DOCE in an internal D flop with a high to low transition.
3	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	The falling edge shifts data bits into the CRC generator/checker. It also transfers the CRC check word to $\overline{DOUT}$ in the write mode ($\overline{DDCE}$ = LOW). The rising edge also activates the $\overline{CRCOK}$ lines in the read mode when no error is found.
4,5	N.C.	NO CONNECTION	
6	$\overline{CWE}$	$\overline{CHECK\ WORD\ ENABLE}$	This active low output indicates that the CRC checkword is being output on the $\overline{DOUT}$ line. When $\overline{CWE}$ is high, data is being output on $\overline{DOUT}$.
7	DOCE	DATA OR CRC ENABLE	Initially, this input line is held high to direct input data (pin 1) to the output data (pin 11). After the next to the last BYTE is transmitted but before the last BYTE occurs DOCE must be low to direct the 2 CRC check bytes to DOUT (pin 11). DOCE must be maintained low for a minimum of 2 byte times. DOCE is used only in the write mode.
8	$\overline{CRCIZ}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ INITIALIZE}$	When this line is at a logic 0, the SKPCLK output line is held high and the CRC generator is held preset to hex "FFFF."
9	N.C.	NO CONNECTION	
10	V_{SS}	GROUND	GROUND.
11	$\overline{DOUT}$	$\overline{DATA\ OUTPUT}$	In the write mode, this line outputs the unmodified data stream along with the 2 byte CRC word appended to the end of the stream.
12	SKPCLK	SKIP CLOCK	The first high-to-low transition on $\overline{DIN}$ (pin 1) resets SKPCLK low and enables the CRC to either generate or check the CRC word.
13	CRCOK	CYCLIC REDUNDANCY CHECK OKAY	In the read mode, after the 2 byte CRC word is entered on $\overline{DIN}$ and no error has been detected, this line is set high to indicate no errors have occurred. This line will then remain high as long as $\overline{DIN}$ is maintained high.
14	WCLK	WRITE CLOCK	This input clock is divided by 16 to produce TIMCLK (pin 15) and has no effect on the rest of the internal circuitry.
15	TIMCLK	TIMING CLOCK	See WCLK (pin 14).
16	$\overline{CRCOK}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ OKAY}$	Complementary output version of CRCOK (pin 13).
17-19	N.C.	NO CONNECTION	
20	V_{CC}	Power Supply	+5v ± 10% power supply.

DEVICE DESCRIPTION

Prior to shifting data through the device (either in the read or write modes) the CRC generator/checker is initialized by strobing the CRCIZ (pin 8) low. This forces the SKPCLK (pin 12) line to the high state. The first low going transition on DIN (pin 1), namely the most significant bit of an address mark, resets the SKPCLK line. The WD1100-04 has now been properly initialized and is ready to generate/check the CRC bytes. The CRCOK and CRCOK lines should be set to their inactive states.

In the write mode, initially the DOCE (pin 7) is held high and pseudo DOCK is produced by supplying a string of zeros before the address mark. This ensures the proper state of the internal D flip flop to gate input data to the output line DOUT (pin 11). As shown in the block diagram the CWE (pin 6) will be set high. Sometime between the next to the last and the last DOCK that indicates the end of the data stream, DOCE (pin 7) is lowered to ensure the smooth transition of the 2 byte CRC checkword to the output line DOUT (pin 11).

DOCE must be maintained low for a minimum of 2 byte times. After the CRC word is generated, DOUT will produce a string of zeroes (i.e., held high). This portion of the circuitry is dormant in the read mode. After proper initialization, input data is entered on DIN (pin 1) along with the 2 byte CRC word for the read mode of operation. At the end of the data stream, if no errors were detected the CRCOK (pin 13) is set high. Accordingly the complimentary output (pin 16) is set low. These output states will be maintained as long as DIN is held high and CRCIZ (pin 8) is not strobed. If the CRCOK lines do not become active, an error has been detected and a retry is in order. If successive re-tries fail, an error flag may be set to determine a further course of action as desired by the user.

WCLK is divided by 16 to produce TIMCLK which may be used as a buffered step clock for SA1000 compatible drives.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under
Bias . . . . . 0°C (32°F) to 50°C (122°F)
Voltage on any pin
with respect to V_{SS} . . . . . -0.2V to +7.0V
Power Dissipation . . . . . 1 Watt

STORAGE TEMPERATURE
PLASTIC . . . . . -55°C (-67°F) to + 125°C (257°F)
CERAMIC . . . . -55°C (-67°F) to + 150°C (302°F)

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITIONS
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{0H} = -200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All Outputs Open
I_{IH}	Current Input High			<10	uA	V_{IN} = .4 to V_{CC}
I_{IL}	Current Input Low			<10	uA	V_{IN} = .4 to V_{CC}

AC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN.	TYP[1]	MAX.	UNITS	CONDITION
t_{WT}	↑ WCLK to ↓ TIMCLK			140	nsec	
t_{ZS}	CRCIZ ↓ to ↑ SKPCLK			120	nsec	
t_{ZK}	CRCIZ pulse width	90			nsec	
t_{BS}	DOCE set up time w.r.t. ↓ DOCK	20			nsec	
t_{BH}	DOCE hold time w.r.t. ↓ DOCK	40			nsec	
t_{DD}	DIN to DOUT delay			105	nsec	CWE set high

SYMBOL	PARAMETER	MIN.	TYP[1]	MAX.	UNITS	CONDITION
t_{DK}	↓ $\overline{DIN}$ to ↓ SKPCLK			120	nsec	
t_{DW}	$\overline{DIN}$ P.W. to reset SKPCLK	50			nsec	
t_{IC}	↓ $\overline{DOCK}$ to ↑ $\overline{CWE}$			120	nsec	
t_{SD}	SHFCLK to $\overline{DOUT}$			150	nsec	
t_{BC}	↓$\overline{DOCK}$ to ↑$\overline{CWE}$			120	nsec	
f_{SC}	$\overline{SHFCLK}$ frequency			5.25	MHz	
t_{SR}	↑ $\overline{SHFCLK}$ to ↑ $\overline{CRCOK}$			85	nsec	
t_{SC}	↑$\overline{SHFCLK}$ to ↓ $\overline{CRCOK}$			90	nsec	
t_{IN}	↓ $\overline{DOCK}$ to ↓ $\overline{DIN}$			90	nsec	

NOTE: 1. Typical Values are for T_A = 25°C (77°F) and V_{CC} = +5.0V

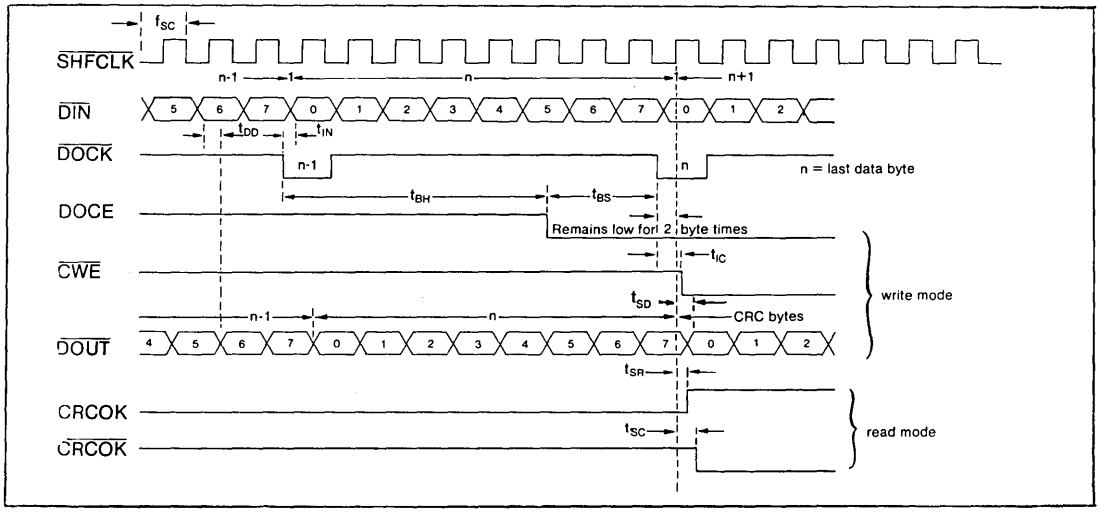


Figure 3.
WD1100-04 Write Mode

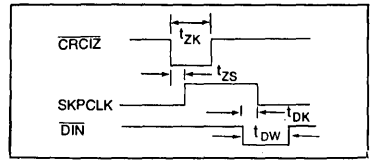


Figure 4.
WD1100-04 Initialize

WD1100-05 Parallel/Serial Converter

DESCRIPTION

The WD1100-05 Parallel/Serial Converter allows the user to convert a byte of data to a serial stream when writing to a disk or any serial device. Parallel data is entered via the D0-D7 lines on the rising edge of $\overline{DCLK}$. A synchronous BYTE counter is used to signify that 8-bits of data have been shifted out and that the 8-bit latch is ready to be reloaded. The double buffering of the data permits another byte to be loaded while the previous byte is in the process of being shifted.

The WD1100-05 is implemented in NMOS silicon gate technology and is available in a 20-pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5 M BITS/SEC SHIFT RATE
- TRI-STATE OUTPUT CONTROL
- PARALLEL IN/SERIAL OUT
- 20 PIN DIP PACKAGE

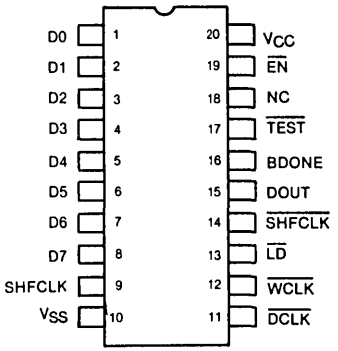


Figure 1.
WD1100-05 Pin Connections

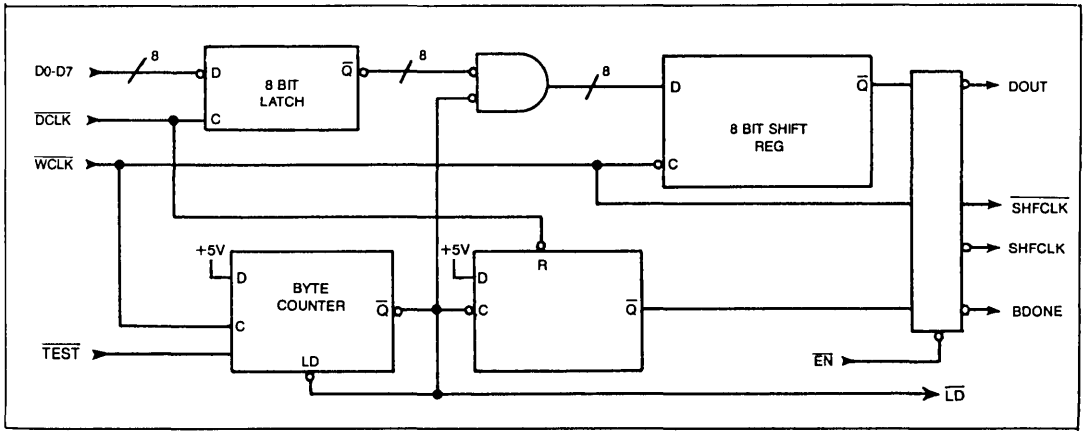


Figure 2.
WD1100-05 Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1-8	D0-D7	DATA 0-DATA 7	8-bit parallel data inputs (bit 7 = MSB).
9	SHFCLK	SHIFT CLOCK	Inverted copy of $\overline{\text{WCLK}}$ (pin 12) which is active when ENABLE (pin 19) is at a logic 0.
10	V_{SS}	GROUND	GROUND.
11	$\overline{\text{DCLK}}$	$\overline{\text{DATA CLOCK}}$	Active low input signal resets the BDONE (pin 16) latch. The low-to-high (trailing edge) clocks the input data into the internal 8-bit latch.
12	$\overline{\text{WCLK}}$	$\overline{\text{WRITE CLOCK}}$	The high-to-low (↓) edge of this clock signal is used to shift the data out serially. The low-to-high (↑) edge is used to update the internal byte counter (module 8).
13	$\overline{\text{LD}}$	$\overline{\text{LOAD}}$	This active low signal indicates that the Byte Counter is being preset to 1. Normally left open by the user.
14	$\overline{\text{SHFCLK}}$	$\overline{\text{SHIFT CLOCK}}$	Delayed copy of $\overline{\text{WCLK}}$ (pin 12) which is active when EN (pin 19) is at a logic 0.
15	DOUT	DATA OUT	Serial data output enabled by EN (pin 19).
16	BDONE	BYTE DONE	This output signal is forced to a logic 1 whenever 8 bits of data have been shifted out. BDONE remains in this state unless reset by the loading of another byte of data.
17	$\overline{\text{TEST}}$	$\overline{\text{TEST INPUT}}$	This pin must be left open by the user.
18	NC	No Connection	
19	$\overline{\text{EN}}$	$\overline{\text{ENABLE}}$	This active low signal enables DOUT, $\overline{\text{SHFCLK}}$, SHFCLK, and BDONE outputs. When high, these output signals are in a high impedance state.
20	V_{CC}	V_{CC}	+5 ± 10% power supply input.

DEVICE DESCRIPTION

Prior to loading the WD1100-05, it is recommended that 00H (or FF) be loaded into the input buffers to ensure that DOUT is at a fixed level. $\overline{\text{EN}}$ (pin 19) is set to a logic 0 to enable the device outputs.

Data is entered on the D0-D7 input lines and is strobed into the data latches on the rising edge of DCLK (pin 11). DCLK also resets BDONE (pin 16). The first BDONE that comes up simply means that the WD1100-05 is ready to accept another byte of data and that the previous byte entered is in the process of being shifted out. If the BDONE is serviced prior to every 8th WRITE CLOCK pulse the output data will represent a contiguous block of the bytes entered. Due to the asynchronous nature of the WD1100-05, the input data will be available in serial form at the output anywhere from 8 to 16 write clock cycles later.

Data is shifted out on the high-to-low (↓) transition of the $\overline{\text{WCLK}}$ (pin 12). The low-to-high (↑) transition of WCLK increments a byte counter which in turn sets the BDONE signal high after 8 bits of data have been shifted out. The low-to-high transition of BDONE also causes the loading of the data buffer into the shift register. The data buffer is now ready to be reloaded with the next byte.

The loading of the next byte automatically clears the BDONE signal. The entire process as outlined above is repeated. BDONE always needs to be serviced within 8 WCLK cycles unless the next byte to be transmitted is the same as the previous byte.

Four signals, BDONE, DOUT, $\overline{\text{SHFCLK}}$, and SHFCLK, can be placed in a high impedance state by setting $\overline{\text{EN}}$ (pin 19) to a logic 1. Likewise, $\overline{\text{EN}}$ must be at a logic 0 in order for these signals to drive any external device.

The $\overline{\text{TEST}}$ pin is internally OR'ed with the counter output to produce the LD (pin 13) signal. This is used to inhibit the bit counter by external means for test purposes. It is recommended that $\overline{\text{TEST}}$ be left open by the user. An internal pull-up resistor is tied to this pin to satisfy the appropriate logic level required for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias .....0°C (32°F) to 50°C (122°F)
Voltage on any pin
with respect to V_{SS}.....-0.2V to +7.0V
Power Dissipation .....1 Watt
STORAGE TEMPERATURE
PLASTIC .....-55°C (-67°F) to + 125°C (257°F)
CERAMICS .....-55°C (-67°F) to + 150°C (302°F)

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics: T_A = 0°C (32°F) to 50°C (122°F), V_{CC} = ±5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 200 μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All Ouputs Open
I_{IH}	Current Input High			<10	μA	V_{IN} = .4 to V_{CC}
I_{IL}	Current Input Low			<10	μA	V_{IN} = .4 to V_{CC}

AC Electrical Characteristics: T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = + 5 ± 10% V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
^fWC	WCLK frequency			5.25	MHZ	50% duty cycle
^tDW	DCLK pulse width	50			nsec	
^tDS	Data set-up w.r.t. ↑ DCLK	30			nsec	
^tDH	Data hold time w.r.t. ↑ DCLK	50			nsec	
^tDB	↓ DCLK to ↓ BDONE			160	nsec	EN = 0
^tDO	↓ WCLK to DOUT			130	nsec	EN = 0
^tSH	↓ WCLK to ↓ SHFCLK			75	nsec	EN = 0
^tHS	↑ WCLK to ↑ SHFCLK			70	nsec	EN = 0
^tWB	↑ WCLK to ↑ BDONE			180	nsec	EN = 0
^tES	↓ $\overline{EN}$ to BDONE, DOUT SHFCLK ACTIVE			90	nsec	
^tCL	↑ $\overline{WCLK}$ to ↓ $\overline{LD}$			150	nsec	

NOTES: 1. Typical Values are for T_A = 25°C (77°F) and V_{CC} = + 5.0V

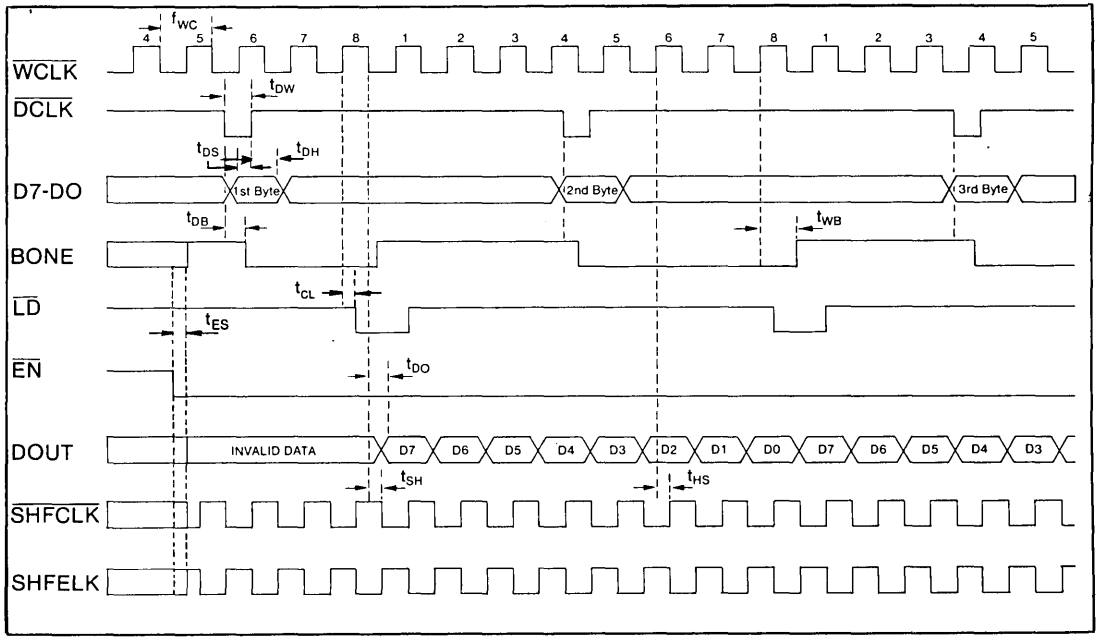


Figure 3.
WD1100-05 Functional Timing Diagram

WD1100-06 ECC/CRC Logic

FEATURES

- 32-BIT COMPUTER SELECTED POLYNOMIAL
- SINGLE BURST CORRECTION TO 8 BITS
- MULTIPLE BURST DETECTION
- PROGRAMMABLE CORRECTION/DETECTION SPAN
- CRC OR ECC SOFTWARE SELECTABLE
- DATA TRANSFER RATES TO 5.25 MBITS/SEC
- SERIAL CHECK/SYNDROME BIT PROCESSING
- 128, 256, 512 BYTE SECTOR SIZES
- SINGLE +5V SUPPLY
- TTL, MOS COMPATIBLE
- 20 PIN DIP PACKAGE

DESCRIPTION

The WD1100-06 ECC/CRC logic chip gives the user of the WD1100 series of chips easy ECC or CRC implementation. With proper software, it will provide single burst correction up to 8 bits and double burst detection. The computer selected polynomial has been optimized for Winchester 5 1/4" and 8" drives with sector sizes up to 512 bytes.

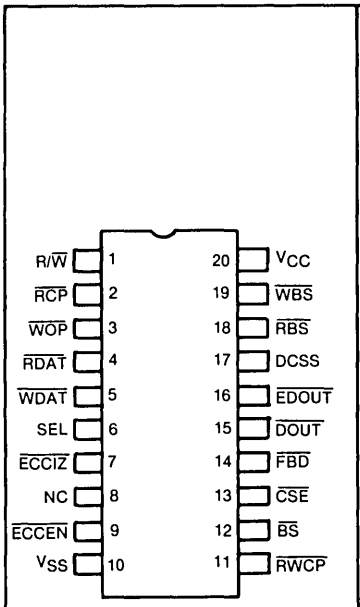


Figure 1.
WD1100-06 CONNECTIONS

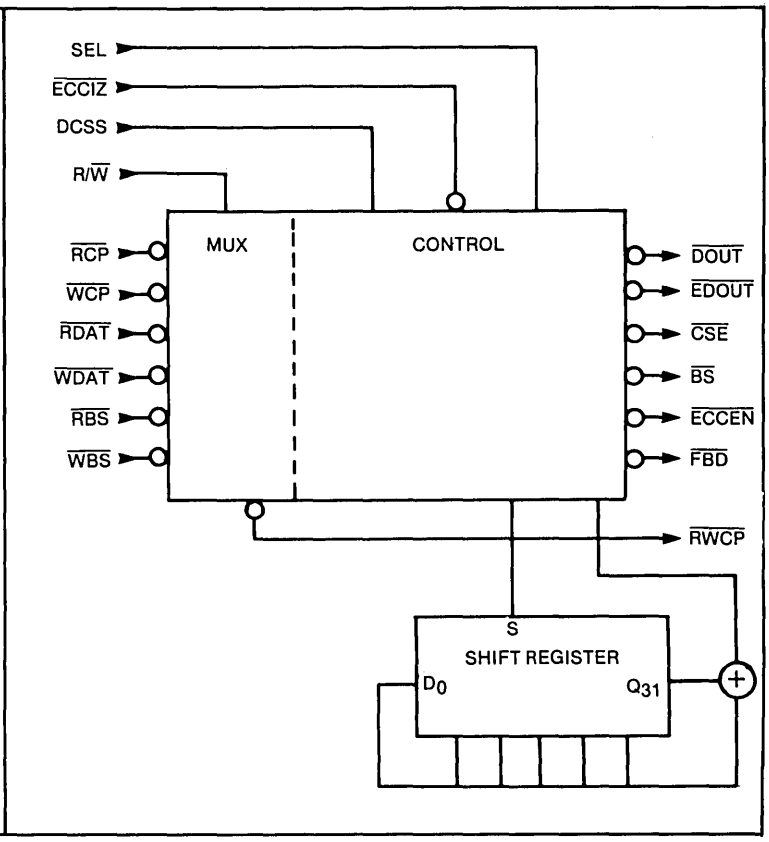


Figure 2.
WD1100-06 BLOCK DIAGRAM

WD1100-06 ECC/CRC DEVICE PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	READ/WRITE	R/W	Input line used to select the data, clock and CRC/ECC strobe during read/write operations. When low input signals WDAT, WCP, and WBS are selected. When high input signals RDAT, RCP, and RBS are selected.
2	READ CLOCK PULSE	$\overline{RCP}$	Input pulse used by the internal shift registers to compute the 4 syndrome bytes.
3	WRITE CLOCK PULSE	$\overline{WCP}$	Input pulse used by the internal shift registers to compute the 4 check bytes.
4	READ DATA	$\overline{RDAT}$	Serial data input during a read operation.
5	WRITE DATA	$\overline{WDAT}$	Serial data input during a write operation.
6	SELECT	SEL	This input is used to select either the CRC or the ECC polynomial for error detection/correction. SEL = 0 ECC polynomial selected. SEL = 1 CRC polynomial selected.
7	ECC INITIALIZE	$\overline{ECCIZ}$	Input used to preset all the internal shift registers. Output lines FBD, EDOUT, DOUT, and CSE will be in their inactive high states. The first low going edge of either RDAT or WDAT signals the activation of all internal circuitry.
8	NO CONNECTION	N/C	No connection.
9	ECC ENABLE	$\overline{ECCEN}$	When low, the ECC/CRC process is enabled. When high, this output signal indicates that the process is disabled.
10	GROUND	V_{SS}	Ground.
11	READ/WRITE CLOCK PULSE	$\overline{RWCP}$	Output clock pulse during read or write operations. The input clock pulses RCP and WCP are multiplexed on this output line for use by any support logic.
12	BYTE SYNC	$\overline{BS}$	The input signals RBS and WBS are gated with the appropriate clocks and multiplexed as an output on the byte sync line. Normally not used by the user.
13	CLOCK SELECT ENABLE	$\overline{CSE}$	When high, this output indicates that the device is in the process of computing the check/syndrome bytes and that EDOUT and DOUT lines contain data information. When low, the device puts CRC or ECC check/syndrome bits on the output data lines.
14	FEEDBACK	$\overline{FBD}$	The feedback line to the shift registers is brought out as an output line for test purposes. Normally left open by the user.
15	DATA OUTPUT	$\overline{DOUT}$	Output data line carries data or CRC/ECC information depending upon the state of DCSS.
16	EARLY DATA	$\overline{EDOUT}$	Unlatched output data line available 1 clock period earlier than DOUT.

WD1100-06 ECC/CRC PIN DESCRIPTION (CONTINUED)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
17	DATA/CHECK SYNDROME SELECT	DCSS	Data or check/syndrome select input line. When high, data is output on the data lines; when low, CRC or check syndrome bits are output depending upon which polynomial selected. DCSS goes low sometime between the last and the next to the last data byte transferred to/from the disk provided all set-up and hold-times have been met. DCSS must stay low for at least 2-byte times when the CRC polynomial selected and it must stay low for at least 4 byte times if the ECC polynomial is selected.
18	$\overline{\text{READ BYTE}}$	$\overline{\text{RBS}}$	Input used to latch the state of DCSS during the read mode.
19	$\overline{\text{WRITE BYTE}}$	$\overline{\text{WBS}}$	Input used to latch the state of DCSS during the write mode.
20	+5V	V_{CC}	+5V ± 10%

DEVICE DESCRIPTION

To ensure correct operation of the WD1100-06 device, the ECCIZ line is strobed to preset the polynomial generator shift register, and reset the Data/Check-Syndrome select flip-flop. The 32-bit shift register string is preset to avoid all zero check bytes. The DCSS line is held high and appropriate signals are then applied to the rest of the inputs. Since most disk media use an Address mark of A1 (or M.S.B. set), advantage is taken of this feature to start off the ECC/CRC calculation on the data/ID fields automatically. The first active low going edge on the input data lines releases the internal SET Flip-Flop. The ECCEN output line is set low indicating that the internal circuitry is ready to begin the computation of the ECC/CRC bytes. Immediately following the Address mark, data is supplied in a serial fashion.

Sometime before the last byte of data and after the next to the last byte of data is transferred through this device, the DCSS line is set low. Since data is generally serialized/deserialized before/after processing by the WD1100-06 device, the byte-sync pulses can be easily obtained from those devices marking the byte boundaries. The byte-sync pulses are internally ANDED with the RWCP line to ensure the smooth transition of checks/syndrome bytes on the DOUT output line only after the last bit of data has been entered into the device. A one bit time delay through a D Flip-Flop has been added on the DOUT line to deglitch this output line.

During a WRITE operation, the input data stream is divided by the polynomial $X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^2 + 1$ and the 32-bit remainder obtained is used as the 4 check syndrome bytes. If the syndrome is zero, no errors occurred. Otherwise, the non-zero syndrome is used by a software algorithm to compute the displacement and the error vector within the bad sector. To protect the integrity of the ID field only a CRC check should be performed over this field. No attempt ought to be made to correct data in the ID field. The CRC polynomial implemented is the standard CCITT ($X^{16} + X^{12} + X^5 + 1$.) Although either polynomial may be used for both fields, the use of the CRC polynomial for the ID fields is recommended since it only requires 2 bytes instead of 4.

POLYNOMIAL SELECTION

For disk media, polynomial selection has a significant influence on data accuracy. Fire code polynomials have been widely used on OEM disk controllers, but provide less accuracy than properly selected computer generated codes.

For fixed, guaranteed correction and detection spans, data accuracy may be highly dependent on polynomial selection. Some polynomials, fire codes for example, are particularly susceptible to miscorrection on common disk type errors, while others, computer generated polynomials for example, can be selected to be less susceptible. Computer generated codes do not have the pattern sensitivity of the fire code and the miscorrection patterns are more random in nature.

More than 20,000 computer generated random polynomials of degree 32, each with 8 feedback terms, were evaluated in order to find the polynomial described in this specification.

SELECTING THE CORRECTION SPAN

The code described in this document can be used to correct up to 8-bits.

Any correction span from 1 to 8 may be selected. However, for best data accuracy, the lowest correction span should be used that meets the correction requirements for the disk drives supported.

For most Winchester media, a 5-bit correction span is adequate.

The correction span may have to be longer if the drive uses a read/write modulation method that maps a single media bit in error into several decoded bits in error. Examples of read/write modulation methods of this type would be GCR and 2,7 code.

PROPERTIES OF THE POLYNOMIAL

The following polynomial was computer selected for insensitivity to short double bursts, good detection span and 8 feedback terms.

Forward polynomial is:
$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^{6} + X^{2} + 0$.

Reciprocal polynomial is:
$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^{6} + X^{4} + X^{0}$.

Properties*

1. Maximum record length (r) = 526x8-bits (including check bits)
2. Maximum correction span (b) = 8-bits
3. Degree of polynomial (m) = 32
4. Single burst detection span without correction = 32 bits.(Detection span when the code is used for detection only)
5. Single burst detection span with correction (d) - (Detection span when the code is used for correction)
   = 19 bits for b = 5 and r = 526x8
   = 14 bits for b = 8 and r = 526x8
   = 20 bits for b = 5 and r = 270x8
   = 14 bits for b = 8 and r + 270x8
6. Double burst detection span without correction - (Double burst detection span when code is used for correction)
   = 3 bits for b = 5 and r = 526x8
   = 2 bits for b = 8 and r = 526x8
   = 4 bits for b = 5 and r = 270x8
   = 2 bits for b = 8 and r = 270x8
7. Non-detection probability = 2.3E-10.
8. Miscorrection probability -
   = 1.57 E-5 for b = 5 and r = 526x8
   = 1.25 E-4 for b = 8 and r = 526x8
   = 8.00 E-6 for b = 5 and r = 270x8
   = 6.40 E-5 for b = 8 and r = 270x8

NOTE:*
You should not use this polynomial for a record length of correction span beyond the maximum specific above.

SOFTWARE REQUIREMENTS

The software algorithm, developed by the user, uses the syndrome to detect an error, generate a correction pattern and a displacement vector or to determine if uncorrectable. In the correction algorithm, a simulated shift register is used to implement the reciprocal polynomial. The simulated shift register is loaded with the syndrome and shifted until a correctable pattern is found or the error is determined to be uncorrectable. Both forward and reverse displacements are computed.

Either the serial or the parallel algorithm may be implemented by the user. In almost all cases the serial software algorithm is the most applicable. Additionally, 1K of table space is required if the parallel software algorithm is selected. It is assumed that the highest order bit of a byte is serialized and deserialized first.

CORRECTION TIME PERFORMANCE

All real time operations are performed with error correction hardware. The software algorithms used get involved only after an error has been detected.

The following correction times are for a serial type algorithm such as that used on the WD1001:
a) Standard microprocessor = 30 to 60 milliseconds
b) Bit slice = 6 to 12 milliseconds
c) 8X300 (used on WD1001) = 15 to 30 milliseconds

DATA ACCURACY

ERP (Error Recovery Procedure) strategies have a significant influence on data accuracy. An ERP strategy requires data to be re-read before applying correction and results in much better data accuracy. The WD1001 employs such a strategy. This strategy reduces the possibility of passing undetected erroneous data by rereading until the error goes away, or until there has been a consistant error syndrome over two previous rereads.

Another technique that can be used to give data a higher probability of recovery is write check: read back after write. Since write check affects performance, it should be optional. Alternate sector assignment and defect skipping are some of the other techniques that may be implemented by the user if so desired.

SELF-CHECKING WITH MICROCODE

Periodic microcode and/or software checking is another approach that can be used to limit the amount of undetected erroneous data transferred in case of an ECC circuit failure. Microcode or software diagnostics could be run on subsystem power up and during idle times. These diagnostics would force ECC errors and check for the proper syndrome and proper decoding of the syndrome by the correction routine of the operational microcode.

To do this, simply use a long bit in the READ and WRITE commands to the disk. This bit can then be used to suppress the transfer of check/syndrome bytes on the output data line by letting the DCSS line stay high during ECC TIME. The complete procedure is summarized below.

1. WRITE: Pass all data to the disk and generate 4 check bytes at the end of the data field.

2. READLONG: Do not generate the syndrome, instead copy the 4 check bytes as data and pass them unaltered to the Host. Now the Host may induce errors anywhere in the data stream as long as the induced error does not exceed the correction span of the polynomial generator.

3. WRITELONG: Write the data and check bytes supplied by the Host to the disk. Prevent WD1100-06 from generating check bits by not asserting DCSS during transfer. No check bytes will be recorded.

4. READ: Read data and generate the syndrome in a normal manner. The software algorithm can now be invoked to correct the induced error.

To aid in detection of certain hardware failures, it is desirable to have non-zero check bytes for an all zeros record. This feature has been incorporated into the circuit defined in this specification.

Ambient Temperature under Bias . . . . 0°C (32°F) to 50°C (122°F)
Voltage on any pin with respect to V_{SS} . . . . . -0.2V to +7.0V
Power Dissipation . . . . . 1 Watt
Storage Temperature
Plastic . . . . . -55°C (-67°F) to +125°C (257°F)
Ceramic . . . . . -55°C (-67°F) to +150°C (302°F)

SPECIFICATIONS

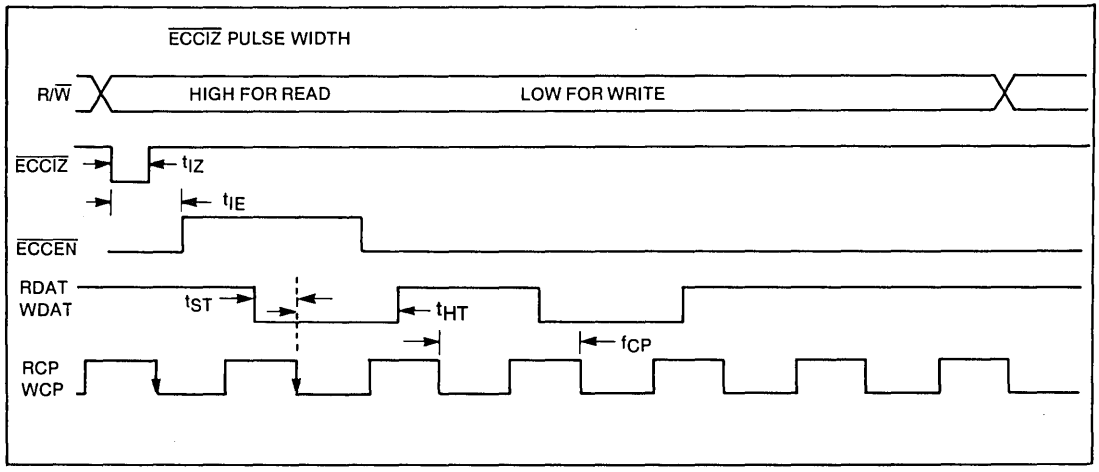
ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias....0°C (32°F) to 50°C (122°F)
Voltage on any pin with respect to V_{SS} .....-0.2V to +7.0V
Power Dissipation .....1 Watt
Storage Temperature
Plastic .....-55°C (-67°F) to +125°C (257°F)
Ceramic .....-55°C (-67°F) to +150°C (302°F)

NOTE:
Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

DC Operating Characteristics T_A = 0°C (32°F)to 50°C (122°F), V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITIONS
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{0H} = -200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		75	150	mA	All Outputs Open
I_{IH}	Current Input High			<10	uA	V_{IN} = .4 to V_{CC}
I_{IL}	Current Input Low			<10	uA	V_{IN} = .4 to V_{CC}



AC Electrical Characteristics T_A = 0°C (32°F) to 50°C(122°F), V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITIONS
f_{CP}	Clock Frequency			5.25	MHz	
t_{IZ}	ECCIZ Pulse Width	100			nsec	
t_{IE}	ECCIZ↓ to ECCEN ↑			100	nsec	
t_{ST}	R/WDAT Setup Time	100		1 Clock Period	nsec	
t_{HT}	R/WDAT Hold Time	0			nsec	

WD1100-07 Host Interface Logic

FEATURES

- SINGLE +5V SUPPLY
- WAIT SIGNAL GENERATION
- TIMING CLOCK GENERATION
- INDEX PROPAGATION
- CARD ACCESS CONTROL
- COMPLIMENTS ECC ARCHITECTURE
- 20 PIN DIP PACKAGE

DESCRIPTION

The WD1100-07 Host Interface Logic chip simplifies the design of a Winchester Hard Disk Controller using the WD1100 chip series. It does this by performing logic functions that would otherwise require considerable discrete logic. Additionally, there are signals provided for ECC implementation.

The WD1100-07 is implemented in NMOS silicon gate technology and is available in a 20-pin plastic or ceramic Dual-in-Line package.

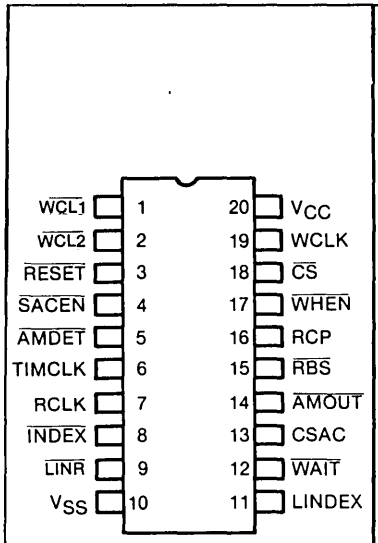


Figure 1.
WD1100-07 PIN CONNECTIONS

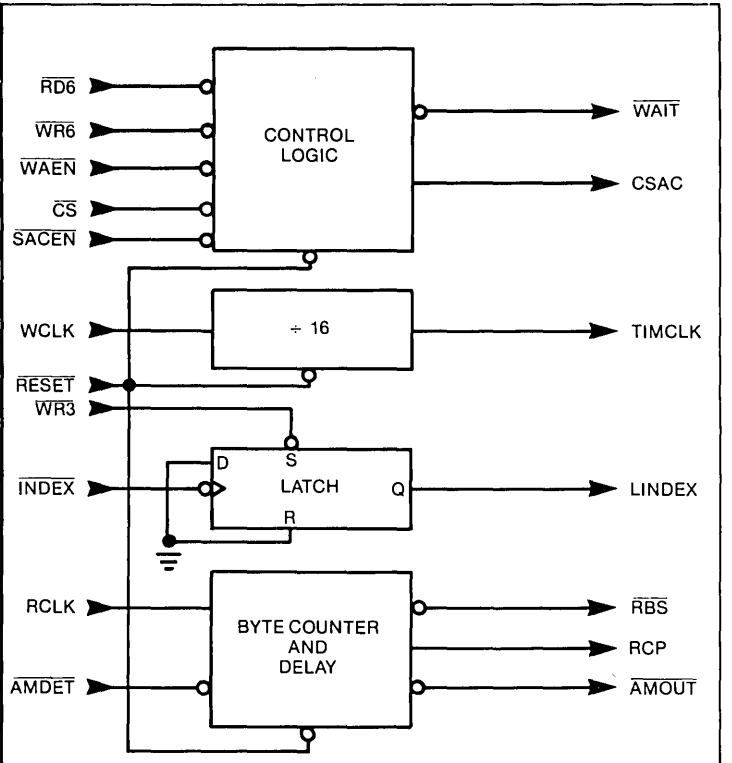


Figure 2.
WD1100-07 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	WAIT CLEAR 1	WCL1	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
2	WAIT CLEAR 2	WCL2	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
3	RESET	RESET	An input used to set TIMCLK & reset WAIT, AMOUT and RBS.
4	SELECT ADDRESS ENABLE	SACEN	This is an input signal that is used to enable card select for host access.
5	ADDRESS MARK DETECT	AMDET	An input that must go active when a DATA = A1(HEX) or clock = 0A(HEX) pattern is detected in the data stream.
6	TIMING CLOCK	TIMCLK	An output used to provide reference timing signals to SA100 type drives.
7	READ CLOCK	RCLK	This input, the same as used to clock in data and clocks to the AM detector, is used to produce AMOUT.
8	INDEX PULSE	INDEX	This input is provided by the drive once each revolution of the disk.
9	LINDEX RESET	LINR	An input used to reset LINDEX.
10	GROUND	V_{SS}	Ground.
11	LATCHED INDEX	LINDEX	An output that is INDEX delayed by one clock time.
12	WAIT	WAIT	This output goes true when controller is internally accessing data or has not accepted data from the host during a WRITE.
13	CARD SELECT ADDRESS	CSAC	An output that is the result of CS qualified with SACEN.
14	ADDRESS MARK DELAYED OUTPUT	AMOUT	This output is a delayed version of AMDET.
15	READ BYTE STROBE	RBS	This output strobes once for each byte of READ data. Initialized by AMDET.
16	READ CLOCK PULSE	RCP	This output is delayed from RCLK through propagation. Not normally used.
17	WAIT ENABLE	WAEN	An input that is used to enable the internal WAIT circuitry.
18	CARD SELECT	CS	An input from host that selects controller.
19	WRITE CLOCK	WCLK	This input is used to produce TIMCLK on low to high transitions.
20	+5VDC	V_{CC}	+5V ± 10%.

DEVICE DESCRIPTION

Upon power up or reset, WAIT, AMOUT, and RBS are reset and TIMCLK is set. This is the only interactive signal between the four sections of the chip. Each section will be described separately.

Control Logic

This section provides WAIT (pin 12) and CSAC (pin 13). WAIT is set in its active low state when WAEN (pin 17) is active low by the falling edge of CS (pin 18). WAIT is reset by the falling edge of either WCL1 or WCL2 depending on whether in a read or write mode. CSAC (pin 13) is enabled by setting SACEN (pin 4) low after WAIT has been enabled. CSAC is reset by WCL1 or WCL2.

Timing Clock

TIMCLK (pin 6) is a divided by sixteen version of WCLK (pin 19). It is used with SA1000 type drives.

Index Pulse

Lindex (pin 11) is a delayed version of INDEX (pin 8). It remains high until reset by LINR (pin 9).

Read Byte Sync

$\overline{RBS}$ (pin 15) will go true on the eighth negative going transition of RCLK (pin 7) after $\overline{AMDET}$ (pin 5) goes true. $\overline{RBS}$ will remain true for one clock cycle.

Read Clock Pulse

RCP (pin 16) is a delayed version of RCLK and is normally left open by the user.

Address Mark Delayed Output

$\overline{AMOUT}$ (pin 14) is the same as $\overline{AMDET}$ delayed by two clock times.

These circuits were developed to work with the other chips in the WD1100 series. They are used on the WD1001 the timing relationships must be observed.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias .....0°C (32°F) to 50°C (122°F)
Voltage on any pin
with respect to V_{SS}.....-0.2V to +7.0V
Power Dissipation.....1 Watt
Storage Temperature
Plastic ....-55°C (-67°F) to +125°C (257°F)
Ceramic ...-55°C (-67°F) to +150°C (302°F)

NOTE:

Maximum ratings indicate operation where permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

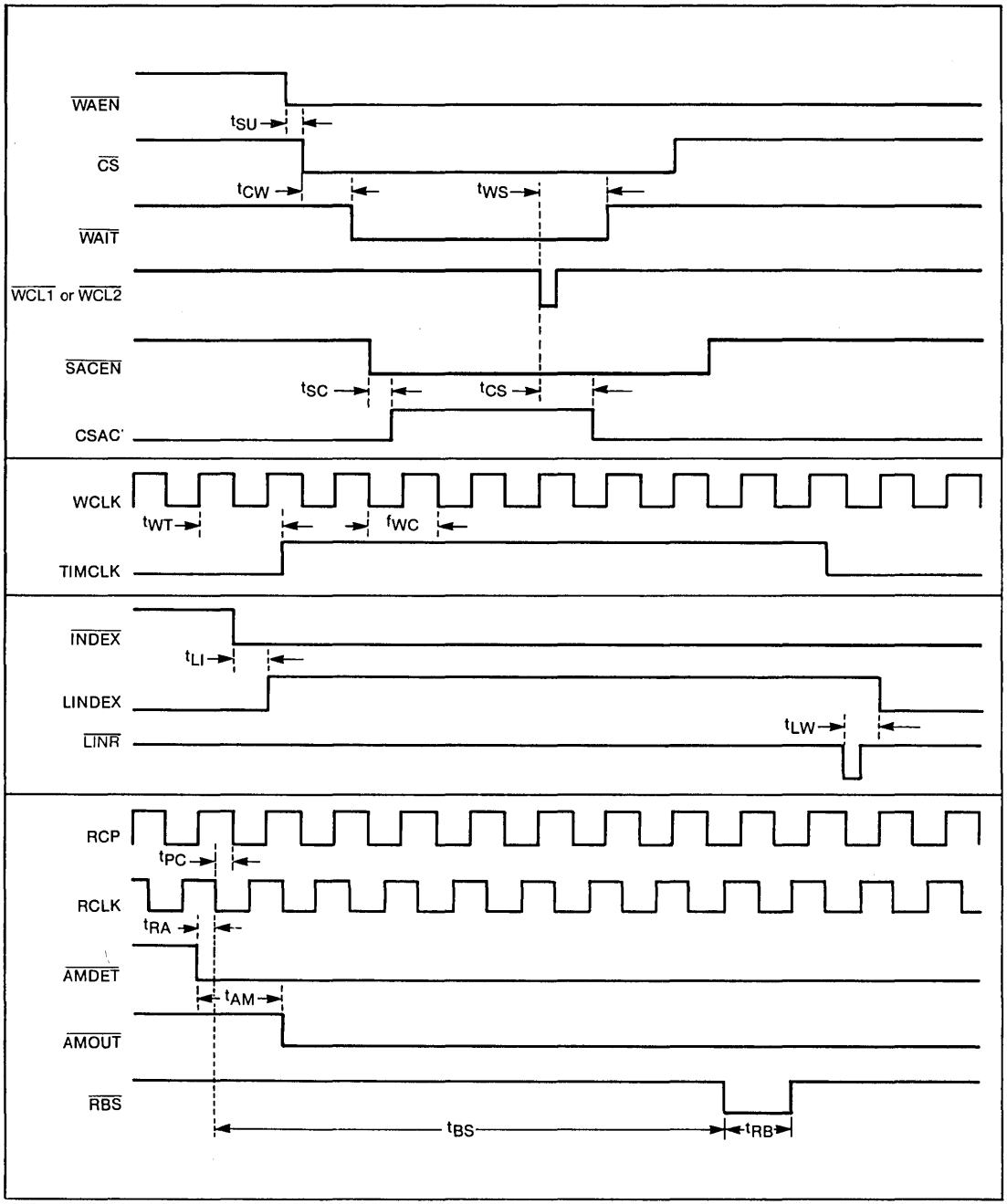
DC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = +5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITIONS
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All Outputs Open
I_{IH}	Current Input High			<10	uA	V_{IN} = .4 to V_{CC}
I_{IL}	Current Input Low			<10	uA	V_{IN} = .4 to V_{CC}

AC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = 5V ±10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITIONS
f_{WC}	WCLK FREQUENCY			5.25	MHz	
t_{CW}	$\overline{CS}$↓ to $\overline{WAIT}$↓		50	160	nsec	
t_{WS}	$\overline{WCL1}$↓ or $\overline{WCL2}$↓ to $\overline{WAIT}$↑		170	195	nsec	
t_{SU}	$\overline{WAEN}$ Setup Time	50			nsec	
t_{SC}	$\overline{SACEN}$↓ to $\overline{CSAC}$↑		5	70	nsec	$\overline{WAIT}$ TRUE
t_{CS}	$\overline{WCL1}$↓ or $\overline{WCL2}$↓ CSAC↓		45	155	nsec	$\overline{WAIT}$ TRUE
t_{WT}	$\overline{WCLK}$↑ to TIMCLK↑			250	nsec	
t_{LI}	$\overline{INDEX}$↓ to LINDEX↑		50	100	nsec	
t_{LW}	$\overline{LINR}$↓ to LINDEX↓		30	100	nsec	
t_{PC}	$\overline{RCLK}$↓ to RCP↓		30	75	nsec	
t_{RA}	$\overline{AMDET}$ Setup Time		30	50	nsec	
t_{AM}	$\overline{AMDET}$↓ to $\overline{AMOUT}$↓		2 CLOCK CYCLES +45 8 CLOCK CYCLES	2 CLOCK CYCLES +45 8 CLOCK CYCLES	nsec	
t_{BS}	$\overline{RCLK}$↓ to $\overline{RBS}$↓		+165	90	nsec	
t_{RB}	$\overline{RBS}$ Period		1 CLOCK CYCLE			

[1]NOTE: Typical Values are for T_A = 25°C (77°F) and V_{CC} = +5V


WAEN
tSU
CS
tCW
tWS
WAIT
WCL1 or WCL2
SACEN
tSC
tCS
CSAC'
WCLK
tWT
tWC
TIMCLK
INDEX
tLI
LINDEX
tLW
LINR
RCP
tPC
RCLK
tRA
AMDET
tAM
AMOUT
RBS
tBS
tRB

WD1100-09 Data Separator Support Logic

GENERAL DESCRIPTION

The WD1100-9 Data Separator Support Logic, when used with the other chips in the WD1100 series, greatly reduces the external discrete logic required to design a Winchester hard disk data separator. The chip provides the pump signals to an external error amplifier, control signals to an internal bus and a special drive selection signal also to an internal bus.

The WD1100-09 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic package.

FEATURES

- SINGLE +5V SUPPLY
- DRUN GENERATION
- DATA SEPARATION CONTROL SIGNALS
- 20 PIN DIP PACKAGE

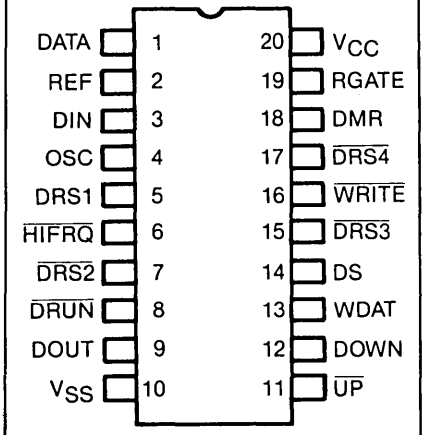


Figure 1.
WD1100-09 Pin Connections

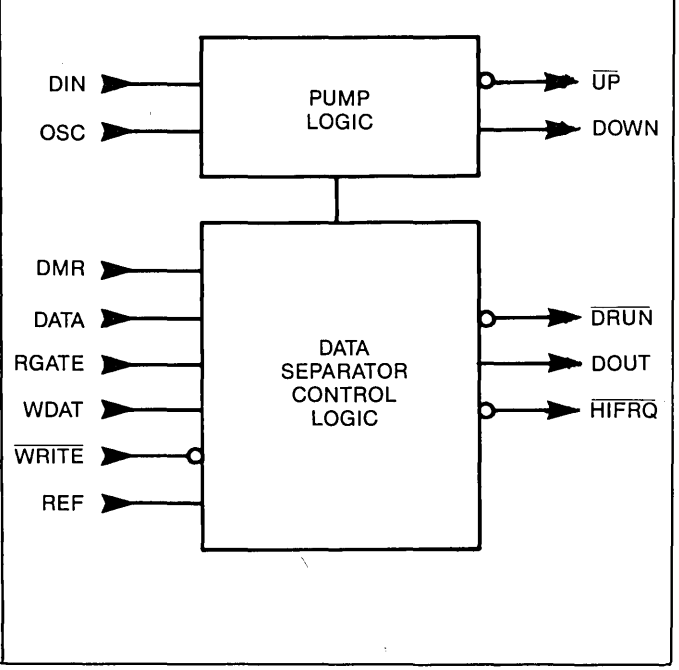


Figure 2.
WD1100-09 Block Diagram

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	READ DATA	DATA	Input that is used in $\overline{\text{DRUN}}$ generation.
2	REFERENCE	REF	An input that is 2 times the data rate that keeps the VCO on center frequency during non-read times.
3	DELAYED DATA IN	DIN	This input is a delayed version of DOUT. An external delay line is used. The signals are compared to provide pumps.
4	OSCILLATOR	OSC	An input from the external VCO that is used in pump development.
5,7, 15,17	$\overline{\text{DRIVE SELECT}}$ 1- $\overline{\text{DRIVE SELECT}}$ 4	$\overline{\text{DRS1}}$- $\overline{\text{DRS4}}$	Input signals indicating which drive has been selected.
6	$\overline{\text{HIGH FREQUENCY}}$	$\overline{\text{HIFRQ}}$	Output to controller microprocessor that indicates 16 ones or zeroes have been entered on the DATA line.
8	$\overline{\text{DATA RUNNING}}$	$\overline{\text{DRUN}}$	Output that indicates to the controller microprocessor the completion of 16 ones or zeroes on the data line. Used to switch from REF to DATA via firmware.
9	DATA OUT	DOUT	Output data line. Can be REF or DATA or WDATA depending on the condition of $\overline{\text{WRITE}}$, DME and RGATE.
10	GROUND	V_{SS}	Ground.
11	$\overline{\text{UP PUMP}}$	$\overline{\text{UP}}$	An output that indicates REF is leading DATA. Goes to error amp. Open collector.
12	DOWN PUMP	DOWN	An output that indicates DATA is leading REF. Goes to error amp. Open collector.
13	WRITE DATA	WDATA	MFM Write data input. Output appears at DOUT.
14	DRIVE SELECTED	DS	An output that indicates that one of four drives have been selected.
16	$\overline{\text{WRITE MODE}}$	$\overline{\text{WRITE}}$	This input is active during a write operation and enables WDAT.
18	DATA MASTER RESET	DMR	This input is used to provide time-out for $\overline{\text{DRUN}}$ and $\overline{\text{HIFRQ}}$ in the event that 16 ones or zeroes are not present.
19	READ GATE	RGATE	This input, usually provided by the controller microprocessor, places chip in read mode.
20	+5V DC	V_{CC}	+5VDC = 10%.

DEVICE DESCRIPTION

The WD1100-09 is divided into three sections. Each section will be described separately.

Drive Select Logic

DS (pin 14) will go active high if any input $\overline{\text{DSR1}}$ through $\overline{\text{DRS4}}$ (pins, 5, 7, 15, 17) are active low.

Pump Logic

Internal logic causes the $\overline{\text{UP}}$ (pin 11) and the DOWN (pin 12) to be set, initially to their inactive states. DIN (pin 3) is the delayed data developed by passing DOUT through a delay line. OSC (pin 4) is the output of the data separator VCO. Whichever reaches the pump logic first will determine whether UP PUMP or DOWN PUMP is produced. These signals are then sent to an external error amplifier and used for VCO correction. During a write, the DIN must be locked to a crystal oscillator clock and will hold the VCO on frequency.

Data Separator Control Logic

Read Mode

In order to prevent the external VCO from locking onto a harmonic of its operating frequency, REF (pin 2) is provided with a signal twice the data rate that is crystal controlled. With $\overline{\text{WRITE}}$ (pin 6) and RGATE (pin 19) inactive, this signal will appear at DOUT (pin 9). This signal is applied to the pump logic (see above).

The switching function is initiated immediately after RGATE goes true. DMR (pin 18) will be set active as a result of high frequency pulses applied to an external one shot whose pulse width is such that its output is a single stretched pulse. The high frequency pulses are applied to the DATA (pin 1) line and after 16 consecutive pulses, $\overline{\text{DRUN}}$ (pin 8) and $\overline{\text{HIFRQ}}$

(pin 6) go true. At this point REF is switched out and the DATA stream is switched in and appears at DOUT. DRUN is reset when RGATE goes inactive and HIFRQ goes inactive when DMR goes inactive.

WRITE MODE

When WRITE (pin 16) goes active, REF is switched out and WDAT (pin 13) will appear at DOUT. Since WDAT is a crystal controlled signal (usually the MFM write data); the VCO is held locked and will not drift.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias .....0°C (32°F) to 50°C (122°F)
Voltage on any pin with
respect to V_{SS} .....-0.2V to +7.0V
Power Dissipation .....1 Watt
STORAGE TEMPERATURE

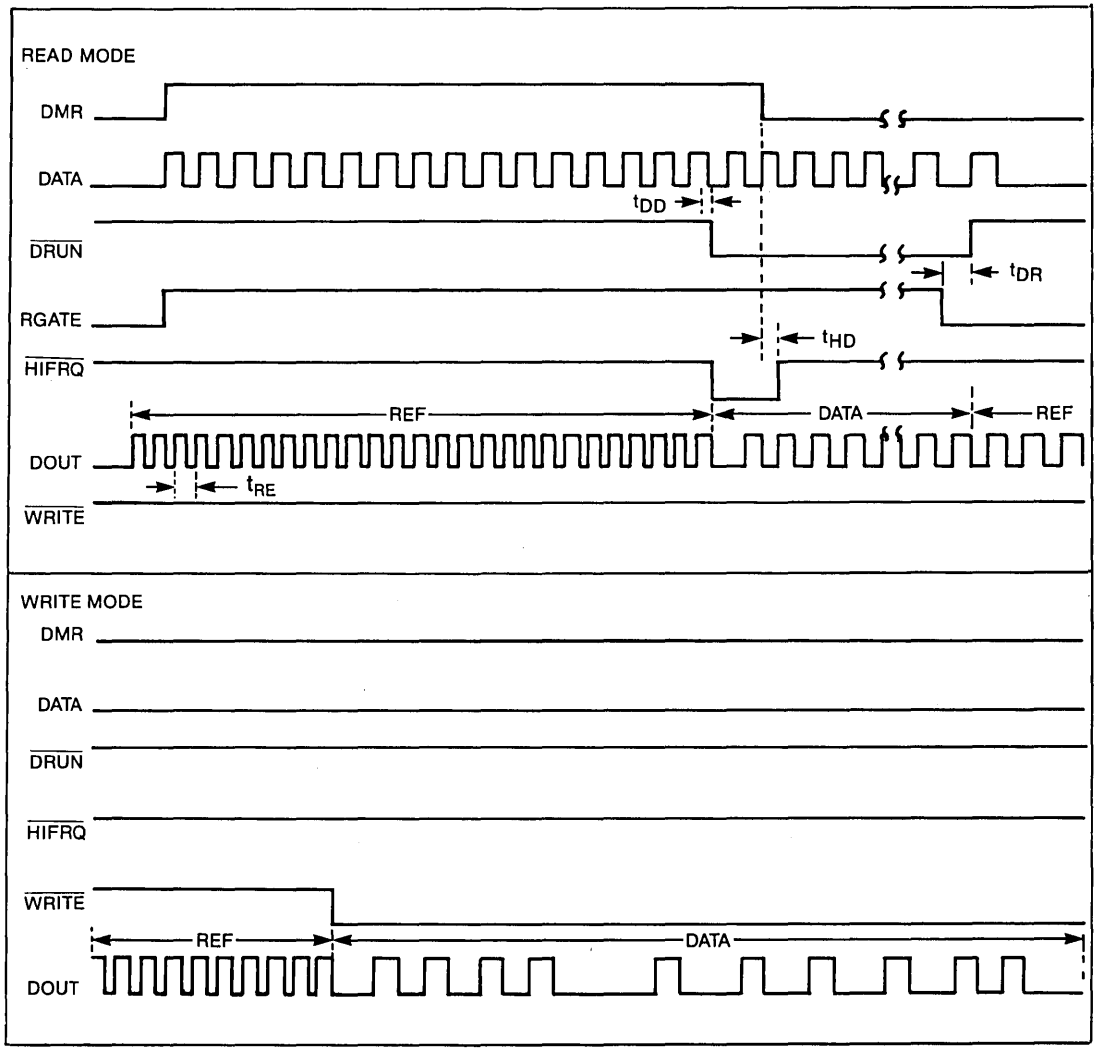
Plastic .....-55°C (-67°F) to + 125°C (257°F)
Ceramic .....-55°C (-67°F) to + 150°C (302°F)

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Operating Characteristics T_A = 0°C (32°F) to 50°C (122°F), V_{CC} = +5V 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All Outputs Open
I_{IH}	Current Input High			<10	μA	V_{IN} = .4 to V_{CC}
I_{IL}	Current Input Low			<10	μA	V_{IN} = .4 to V_{CC}

NOTE: UP and DOWN are open collector outputs and provide 12mA I_{OL} @ .5V.



AC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = 5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{DD}	DATA to $\overline{DRUN}$			170	nsec	
t_{DR}	RGATE to $\overline{DRUN}$			90	nsec	
t_{HD}	DMR to HIFRQ			90	nsec	
t_{RE}	REF frequency		2 TIMES DATA RATE	10	MHz	

WD1100-12 Improved MFM Generator

DESCRIPTION

The WD1100-12 Improved MFM Generator converts NRZ data into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal containing both clocks and data can then be used to record information on a Winchester Disk Drive utilizing this recording technique. In addition to an MFM output, the device generates first level Write Precompensation signals for use with inner track densities. A unique feature of the WD1100-12 is the ability to delete a clock pulse in the outgoing MFM stream in order to record Address Marks.

The WD1100-12 is fabricated in NMOS silicon gate technology and is available in a 20-pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- 5M BIT/SEC DATA RATE
- WRITE PRECOMPENSATION
- ADDRESS MARK GENERATION

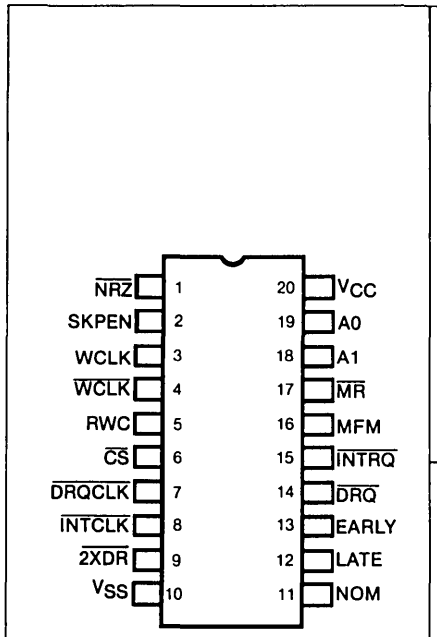
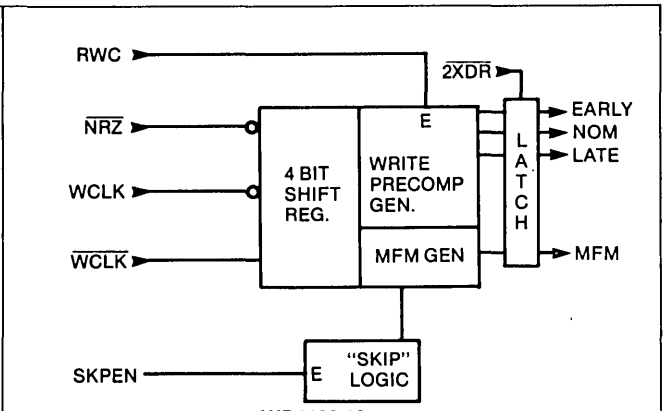


Figure 1.
WD1100-12 Pin Connections



WD1100-12
Figure 2. Block Diagram MFM Generator

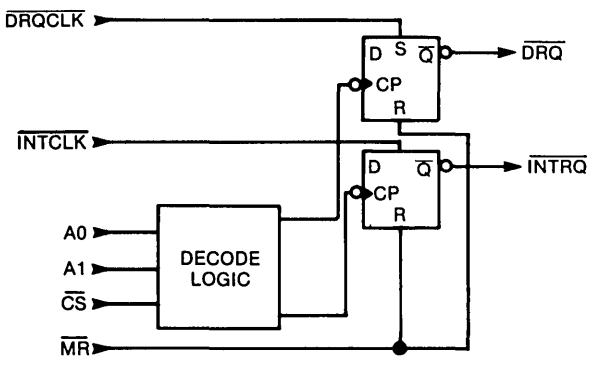


Figure 3.
WD1100-12 Block Diagram Interrupt Control Logic

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	NON-RETURN-TO ZERO	NRZ data input that is strobed into the MFM generator by WCLK(↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. NRZ data is clocked into the MFM Generator on the high-to-low transition of WCLK
4	$\overline{WCLK}$	WRITE CLOCK	(pin 3).
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	$\overline{2XDR}$	2 TIMES DATA RATE	This input is used to latch EARLY, LATE, NOM and MFM outputs.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompenstion Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the NRZ (pin 1) line.
6	$\overline{CS}$	CHIP SELECT	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	INTERRUPT REQUEST CLOCK	A low on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	DATA REQUEST CLOCK	A low on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	INTERRUPT REQUEST	This output is latched at a logic 0 when INTCLK (pin 8) goes/ is low.
14	$\overline{DRQ}$	DATA REQUEST	This output is latched at a logic 0 when DRQCLK (pin 7) goes/ is low.
17	$\overline{MR}$	MASTER RESET	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18,19	A_0,A_1	ADDRESS 0,1	When CS is low and the address lines go high, INTRQ is cleared; if the address lines go low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V ² 10% power supply input.

DEVICE DESCRIPTION

The WD1100-12 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic is used specifically on the WD1000 Winchester Controller Board and may be used in similar designs to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the NRZ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1.

LAST DATA SENT		SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X	1	1	0	H	L	L
X	0	1	1	L	H	L
0	0	0	1	H	L	L
1	0	0	0	L	H	L
ANY OTHER PATTERN				L	L	H

DEVICE DESCRIPTION (CONTINUED)

The SKPEN signal is used to record a unique data / clock pattern as an Address Mark, using AI_{16} data with OA_{16} clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the NRZ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the $A1_{16}$ the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data paterns may be used, the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests ($\overline{INTRQ}$) by selecting $\overline{CS}$ (pin 6) in combination with A_0 and A_1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INRQ}$ simultaneously.

MR	A_1	A_0	CS	DRQ	INTRQ
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q

X = Don't care

Q_N = remains at previous state

$\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only by a low level or $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A_1, and A_0.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias.....0°C (32°F) to 50°C (122°F)
Voltage on any pin
with respect to V_{SS}.....-0.2V to +7.0V
Power Dissipation.....1 Watt

STORAGE TEMPERATURE:
PLASTIC.....-55°C (-67°F) to +125°C (257°F)
CERAMIC....-55°C (-67°F) to +150°C (302°F)

NOTE: Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = +5V ±10%; V_{SS} = OV

SYMBOL	PARAMTER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All outputs open
I_{IH}	Current Input High			<10	μA	V_{IN}= .4 to V_{CC}
I_{IL}	Current Input Low			<10	μA	V_{IN}= .4 to V_{CC}

AC Electrical Characteristics T_A= 0°C (32°F) to 50°C (122°F); V_{CC} = +5V ±10%; V_{SS} = OV

SYMBOL	PARAMTER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{FR}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t.↓WCLK	10			nsec	"Per Figure 4"
t_{DH}	Data hold w.r.t.↓WCLK	25			nsec	"Per Figure 4"
t_{TM}	↑2XDR to ↑ MFM			115	nsec	"Per Figure 4"
t_{MR}	Master reset pulse width	50			nsec	"Per Figure 5"
t_{MD}	↓$\overline{MR}$ to ↑$\overline{DRQ}$			150	nsec	"Per Figure 5"

SYMBOL	PARAMTER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{MI}	↓MR to ↑INTRQ			150	nsec	"Per Figure 5"
t_{DQ}	DRQCLK pulse width	50			nsec	"Per Figure 7"
t_{IQ}	INTCLK pulse width	50			nsec	"Per Figure 8"
t_{DD}	↓DRQCLK to DRQ			120	nsec	"Per Figure 7"
t_{II}	↓INTCLK to INTRQ			120	nsec	"Per Figure 8"
t_{AD}	↓AX to ↑DRQ			145	nsec	"Per Figure 6"
t_{AI}	↑ AX to ↑INTRQ			160	nsec	
t_{CD}	↓CS to ↑DRQ			145	nsec	"Per Figure 6"
t_{CI}	↓CS to ↑INTRQ			180	nsec	"Per Figure 6"
t_{RN}	↑RWC to ↓NOM			145	nsec	"Per Figure 4"
t_{TE}	↑2XDR to ↑EARLY			115	nsec	"Per Figure 4"
t_{TN}	↑2XDR to ↑ NOM			115	nsec	"Per Figure 4"
t_{TL}	↑2XDR to ↑ LATE			115	nsec	"Per Figure 4"

NOTES: 1. Typical Values are for $T_A = 25°C$ (77°F) and $V_{CC} = +5.0V$.

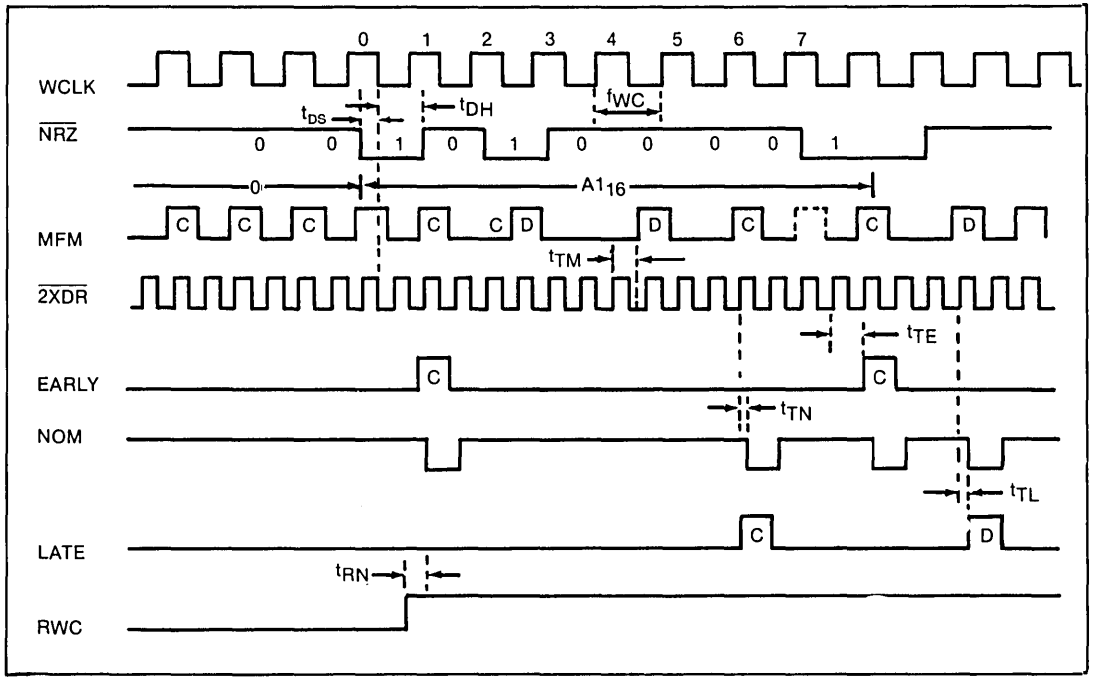


Figure 4. WD1100-12 MFM GENERATOR TIMING

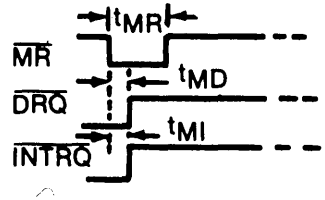


Figure 5

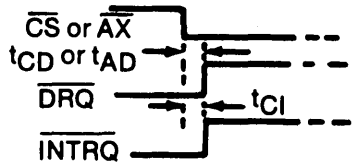


Figure 6

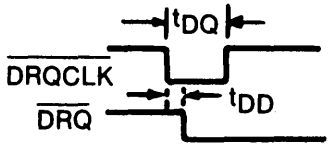


Figure 7

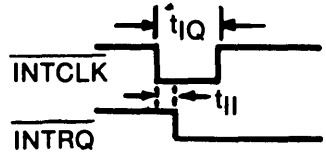


Figure 8

WD2010-05 Winchester Disk Controller

FEATURES

- COMPATIBLE WITH MOST MICROPROCESSORS VIA AN 8-BIT DATA BUS
- DATA RATE OF 5 MBS
- MULTIPLE SECTOR READ AND WRITE COMMANDS
- FORMATTING AND SECTOR INTERLEAVE CAPABILITY
- SEEK COMBINED WITH READ AND WRITE COMMANDS
- SINGLE OR MULTIPLE SECTOR BUFFER USING FIFO OR RAM/COUNTER
- BUFFER ACCESS VIA PROGRAMMED I/O OR DMA
- 32-BIT ECC OR 16-BIT CRC SELECTED BY SOFTWARE
- SECTOR LENGTH OF 128, 256, 512, 1024 BYTES SELECTED BY SOFTWARE
- PROGRAMMABLE RETRY ALGORITHM
- CAPABLE OF CORRECTING ERRORS WHEN A SECTOR BUFFER IS USED
- 5 OR 11 BIT CORRECTION SPAN SELECTED BY PROGRAM

DESCRIPTION

The WD2010 Winchester Disk Controller is a single chip device designed for use with the Shugart Associates SA1000 and Seagate Technology ST506 8" and 5.25" disk drives. The WD2010-05 is software compatible with the WD1010-05 and reads or writes at a rate of 5 Mbits.

The WD2010 operates with an external buffer such as WD1510 128X9 FIFO memory or a combination of a 256X8 static RAM and an 8-bit resettable counter, or a DMA controller. Data bytes are transferred to and from the buffer every 1.6 μsec. Transfers from the buffer to the CPU are made via programmed I/O or DMA.

The WD2010 generates counter control signals to minimize external gating, and hand shake signals to control DMA operation for multiple sector transfers.

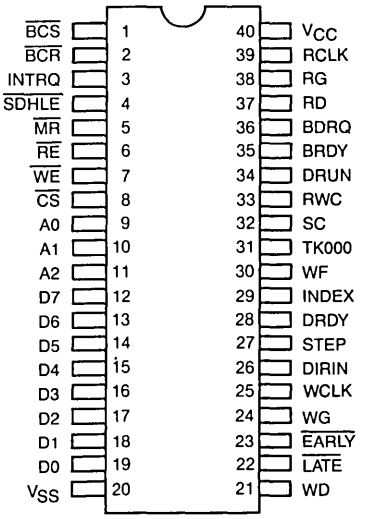
A 32-bit ECC (Error Correction Code) polynomial or a 16-bit CRC are selectable.

The WD2010 has three possible alternatives in handling an error during a Read operation:

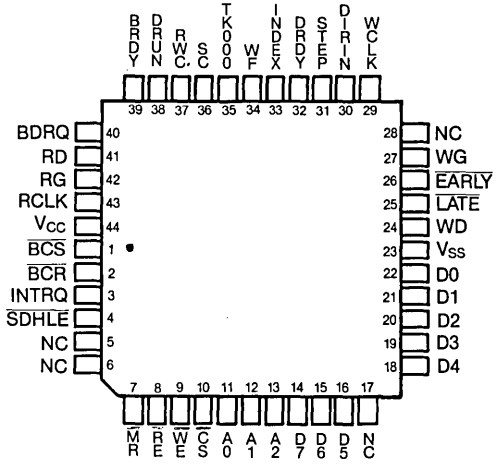
A. It may be directed to correct the data in the Sector Buffer automatically, providing the Host with good data.

B. Supply the Host with the error location and pattern, allowing the Host to correct the error.

C. Take no action other than setting the error flag and letting the Host do the entire error correction process.



DIP PIN DESIGNATION



QUAD PIN DESIGNATION

The WD2010 is a TTL compatible 40 pin DIP or 44 pin QUAD NMOS device requiring a single +5V supply.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	$\overline{BCS}$	$\overline{BUFFER}$ CHIP SELECT	O	When asserted it enables reading or writing the external Sector Buffer as well as controlling bus switching.
2	$\overline{BCR}$	$\overline{BUFFER}$ $\overline{COUNTER\ RESET}$	O	$\overline{BCR}$ is asserted prior to read and write functions and at the completion of a command. $\overline{BCR}$ is not used if the Sector Buffer is a FIFO.
3	INTRQ	INTERRUPT REQUEST	O	INTRQ is asserted upon completion of a command and remains that way until the Status Register is read or a new command is written into the Command Register. This signal may be programmed by a Read Command to occur with BDRQ and DRQ.
4	$\overline{SDHLE}$	$\overline{SDH\ LATCH\ ENABLE}$	O	$\overline{SDHLE}$ is asserted when the $\overline{SDH}$ Register is to be written into by the Host. (See Figure 3.)
5	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	When asserted $\overline{MR}$ initializes all internal logic except Task File.
6	$\overline{RE}$	$\overline{READ\ ENABLE}$	I/O	Tri-state, bi-directional signal. $\overline{RE}$ is an input when reading the Task File, and an output when reading the Sector Buffer.
7	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	I/O	Tri-state, bi-directional signal. Used as an input when writing to the WD2010 Task File. Used as an output when the WD2010 is writing to the Sector Buffer.
8	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	$\overline{CS}$ must be asserted to read from or write to the WD2010 Task File.
9 thru 11	A0 thru A2	ADDRESS 0 thru ADDRESS 2	I	Provide the address of the register within the Task File that is to transmit or receive on the data bus.
12 thru 19	D7 thru D0	DATA 7 thru DATA 0	I/O	8-bit, tri-state, bi-directional bus used for the transfer of commands, status, and data.
20	V_{SS}	GROUND		Ground
21	WD	WRITE DATA	O	WD is the MFM data to be written to the disk. The frequency is controlled internally by WCLK and should be stabilized further externally by a D flip flop clocked at twice the WCLK frequency. The output has an active pullup and pulldown that can sink 6.0ma.
22	$\overline{LATE}$	$\overline{LATE}$	O	This signal is used in the Write Precompensation circuitry along with $\overline{EARLY}$ to control the delay of WD.
23	$\overline{EARLY}$	$\overline{EARLY}$	O	This signal is used in the Write Precompensation circuitry along with $\overline{LATE}$ to control the delay of WD.
24	WG	WRITE GATE	O	WG is asserted when valid data is to be written. It enables write current to the head and is immediately de-asserted if a Write Fault (WF) is detected.
25	WCLK	WRITE CLOCK	I	A 5 MHz clock used internally to control WD.
26	DIRIN	DIRECTION IN	O	This signal determines the direction of the read/write heads when stepped. Asserted moves them in; de-asserted, out.

PIN DESCRIPTION (cont.)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
27	STEP	STEP PULSE	O	This signal is used for pulsing the stepping motor. (See Stepping Rate Description.)
28	DRDY	DRIVE READY	I	DRDY must be asserted to execute any drive related commands.
29	INDEX	INDEX PULSE	I	The leading edge of this signal indicates that the index mark has been detected.
30	WF	WRITE FAULT	I	When asserted, indicates a write error at the drive. This halts all write, read, and stepping commands.
31	TK000	TRACK000	I	This signal is asserted when the read/write heads are positioned over track 0 (cyl.000). It is used to verify proper completion of a restore command.
32	SC	SEEK COMPLETE	I	The leading edge of SC indicates that the drive has settled down after stepping. It is static tested if the rising edge has not been received within 10 revolutions after the stepping pulses.
33	RWC	REDUCE WRITE CURRENT	O	RWC can be programmed to reduce the write current starting at a selected cylinder. (See Write Precomp Cylinder Register.)
34	DRUN	DATA RUN	I	DRUN informs the WD2010 when a field of all ones or zeros has been detected. (See Drive Interface.)
35	BRDY	BUFFER READY	I	When asserted, the Sector Buffer is full or empty.
36	BDRQ	BUFFER DATA REQUEST	O	BDRQ represents the same state as DRQ (bit 3 of the Status Register). This signal is asserted when the Sector Buffer is to be read from or written to by the Host. BDRQ can be used for DMA or Programmed I/O. If DRQ is used it must be polled by the Host during Programmed I/O.
37	RD	READ DATA	I	MFM data and clocks are received from the drive. The clocks and data are separated internally.
38	RG	READ GATE	O	RG is asserted when a search for an address mark is initiated. It remains asserted until the end of the ID or data field. (See Drive Interface.)
39	RCLK	READ CLOCK	I	This clock is generated by a VCO, phase locked to data read from the disk.
40	V_{CC}	+5V		+5 Volts

·ARCHITECTURE

The WD2010 provides the necessary interface control between the Host processor and a 5.25" or 8" Winchester disk drive. The controller is made up of seven major building blocks connected to the processor via a Host interface on one side and a drive interface on the other. Figure 1 illustrates the major sections and how they relate to each other.

The WD2010 timing is controlled by two clock input signals, RCLK and WCLK. RCLK is used for MFM decoding and is a 5 Mbit/sec data rate. WCLK is used for MFM encoding at the same rate as reading, PLA Controller, Host Interface, and Buffer Control.

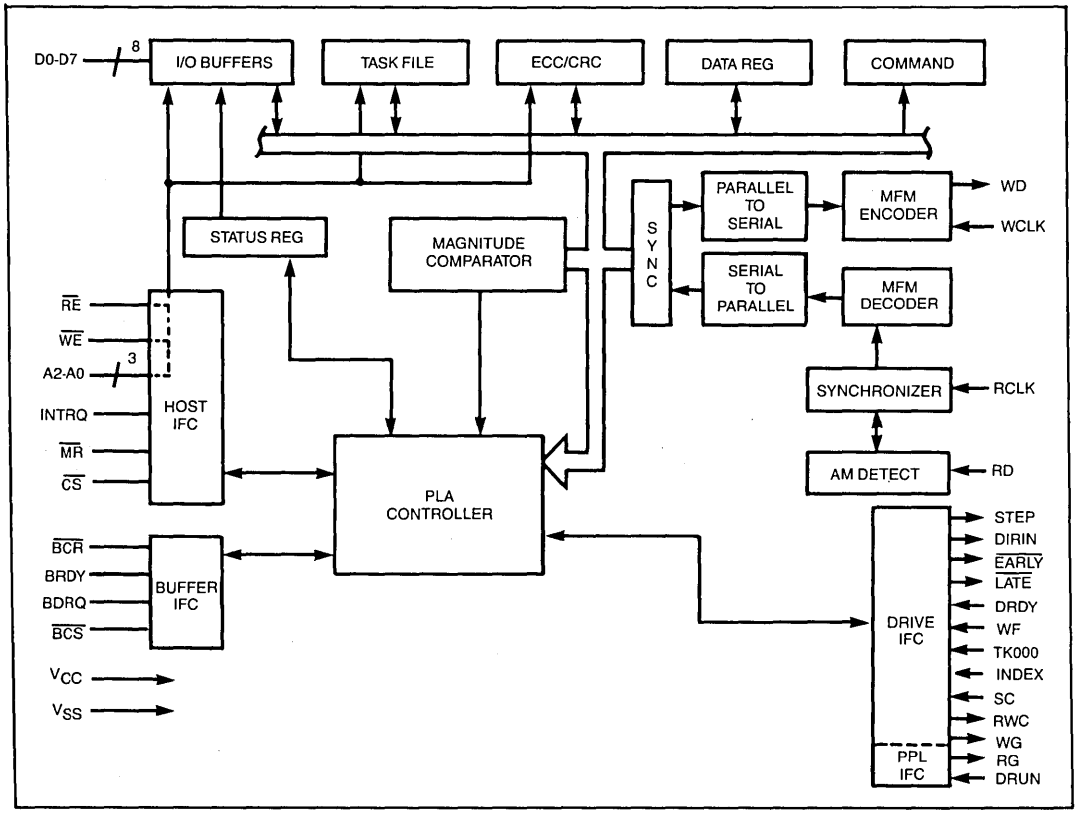


FIGURE 1. WD2010 BLOCK DIAGRAM

Programmable Logic Array (PLA) Controller

The Command Register, is the last of the Task File Registers to be written into, and starts the PLA control. The PLA controller, synchronized by WCLK, interprets the command, generates control signals, and operates in a hand shake mode when communicating with the MFM encoding block.

Magnitude Comparator

The magnitude (number of steps) and direction required to move the heads from their present cylinder to their desired cylinder is performed by an 11-bit comparator. It compares the cylinder number recorded in the Task File (it's desired location) with the Present Cylinder Position Register recorded internally. From this, the direction and number of steps that must be performed to place the head on the desired track is calculated.

A separate high speed equivalence comparator is used to compare ID field bytes when searching for a sector ID field.

CRC and ECC Generator and Checker.

The CRC mode of the operation, defined by the SDH (Sector Size, Head, drive select) Register (Bit 7 = 0), provides a means of verifying the accuracy of the data read from the disk but does not attempt to correct it.

The CRC generator computes and checks cyclic redundancy check characters that are to be written to, and read from the disk following the ID and data fields. The polynomial used is $X^{16}+X^{12}+X^5+1$. The CRC Register is preset to all one's before computation starts.

The ID field always has a 2-byte CRC character appended to it, while the data field may have either a 2-byte CRC (SDH 7 = 0) or a 4-byte ECC character (SDH 7 = 1).

If the CRC character being generated while reading the data does not equal the one previously written, an error exists. If there is a CRC failure in the ID field, an ID not found is indicated by bit 4 of the Error Register being set. If the failure is in the data field, bit 6 of the Error Register is set.

The ECC mode of operation (SDH 7 = 1) is only applicable to the data field. This feature built into the WD2010 provides the user with the ability to detect and correct errors in the data field automatically.

A summary of the parameters to be considered when ECC is desired are:

1. SDH Register bit 7.
2. Read Command bit 0 (T).
3. Read and Write Command bit 1 (L).
4. Compute Correction Command.
5. Set Parameter Command.
6. Error correction successful, bit 2 of the Status Register.
7. Error occurred, bit 0 of the Status Register.
8. Uncorrectable error, bit 6 of the Error Register.

The SDH register bit 7 must be equal to one to change from the CRC mode to the ECC mode.

The T bit (bit 0) within the Read Command controls whether or not error correction is to be attempted.

When T = 0 and an error is detected, the WD2010 tries up to 10 times to correct the error. If successful, bit 2 of the Status Register is set. The Host can interrogate the Status Register and detect that a problem does exist, but was corrected. If the error is not correctable, bit 6 of the Error Register is set. The Host can read the data, even though errors do exist.

When T = 1, and an error is detected, no attempt is made to correct it and bit 0 of the Status Register and bit 6 of the Error Register is set. The user now has two choices:

1. Ignore the error and make no attempt to correct it.
2. Use the Compute Correction Command to determine the pattern and location of the error, and correct it within the user's program.

When the Compute Correction Command is implemented, it should be done before executing any command that can alter the content of the ECC Register. The Read, Write, Scan, and Format commands alter the syndrome and correction is impossible. The Compute Correction Command determines that the error is uncorrectable, at which point the error bits in the Status Register and Error Register are set.

Although ECC generation starts with the first bit of the F8 byte in the data ID field, the actual ECC bytes produced for the sector are the same as if the A1 byte was included.

The ECC polynomial used is,

$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1.$

For auto correction the external data buffer must be implemented with a static RAM and counter, not a FIFO memory.

The Set Parameter Command is used to select a 5 or 11-bit correction span.

Read and Write Commands, with the L bit (bit 1) equal to one, are referred to as Readlong and Writelong Commands. With these commands, no ECC or CRC characters are generated or checked by the WD2010. In effect, the 4 ECC bytes are handled as an additional 4 bytes of data which pass through the data buffer.

With proper use of the Write, Readlong, Writelong, and Read commands, a diagnostic routine may be developed to test the accuracy of the error correction process.

MFM Encoding and Decoding

The MFM encoder receives its data one byte at a time from an 8-Bit parallel-to-serial register, and with the frequency of WCLK, develops the MFM WD. Depending on the bit pattern of the data, $\overline{\text{EARLY}}$ or $\overline{\text{LATE}}$ may be asserted. External circuitry uses these signals to compensate for the shift caused by the influence one bit has over another. The WD2010 examines three bits, the last one written, the one being written, and the next one to be written. From this, $\overline{\text{EARLY}}$ or $\overline{\text{LATE}}$ is asserted. Since the bit leaving the WD2010 has already occurred, it is too late to make it early, therefore the external delay circuit must be as follows.

$\overline{\text{EARLY}}$ (asserted) and $\overline{\text{LATE}}$ (de-asserted) = no delay

$\overline{\text{EARLY}}$ (de-asserted) and $\overline{\text{LATE}}$ (de-asserted) = one unit delay

$\overline{\text{EARLY}}$ (de-asserted) and $\overline{\text{LATE}}$ (asserted) = two units delay

These signals are not dependent upon the Write Precomp Cylinder register (RWC). Figure 6 illustrates one method of using these signals.

The MFM decode operates from RCLK, a bit rate clock generated from the external Data Separator. RCLK and WCLK need not be synchronized.

Address Mark (AM) Detection

An address mark is comprised of two unique bytes preceding both the ID field and the data field. The first byte is used for resynchronization. The second byte indicates whether it is an ID field or a data field.

The first byte, A1 hex, normally has a clock pattern of OE hex. However, one clock pulse has been suppressed, making it QA hex. With this pattern, the detector knows it is looking at an address mark. It now examines the next byte to determine if it is an ID or data field. If bits 7 thru 2 are 1111X1XX, it is an ID field (bits 3, 1, and 0 are the high order cyl.#bits). If the second byte is F8, it is a data field.

Host Interface

The primary interface between the Host processor and the WD2010 is an 8-bit bi-directional bus. This bus is used to transmit and receive data for both the WD2010 and the Sector Buffer. The Sector Buffer consists of either a FIFO memory, or a static RAM and counter. Since the WD2010 makes the bus active when accessing the Sector Buffer, a transceiver must be used to isolate the Host during this time. Figure 2 illustrates a typical interface with a Sector Buffer, implemented with a RAM memory. Whenever the WD2010-05 is not using the Sector Buffer,it turns control of the Sector Buffer and data bus over to the Host by de-asserting its output term, $\overline{\text{BCS}}$. This de-selects the Sector Buffer and switches the data bus transceivers.

When the Host wants to access the Sector Buffer it produces an address of zero (A0 thru A2 ≠ 0). A decoder recognizing A0 thru A2 ≠ 0 asserts a $\overline{BCS}$ of its own. The Host then asserts $\overline{WE}$ or $\overline{RE}$ for the counter, at the leading edge, the location within the Sector Buffer addressed by the counter is accessed, at the trailing edge the counter advances to the next count. The decoder asserts $\overline{CS}$ to the WD2010 any time the address does not equal zero (A0 thru A2 ≠ 0).

During Write Sector commands the Host sets up data in the Task File and issues the command. The WD2010 asserts $\overline{BCR}$ to zero the counter. It then generates a status to inform the Host it can load the Sector Buffer with the data to be written. When the counter reaches its maximum count, BRDY is asserted by the carry out of the counter, informing the WD2010 that the Sector Buffer is full. (BRDY is asserted with a rising edge and is ignored if asserted before the WD2010 asserts $\overline{BCR}$.) $\overline{BCS}$ is then asserted, disconnecting the Host through the transceivers, and $\overline{RE}$ and $\overline{WE}$ become outputs from the WD2010 to allow access to the Sector Buffer. When the WD2010 is done using the Sector Buffer, it de-asserts $\overline{BCS}$ which again allows the Host to access this local bus.

The Read Sector Command operates in a similar manner, except that the Sector Buffer is loaded by the WD2010 instead of the Host.

When BDRQ is used, it can either be connected to a DMA controller or used for programmed I/O. In either case it signals that the WD2010 is ready to receive or transmit data. DRQ status bit, if used, must be polled by the Host, therefore is limited to programmed I/O.

When INTRQ is asserted, the Host is signaled that a command has terminated (either a normal termination or an aborted command). In the case of the Read Command, INTRQ can be programmed by bit 3 to be asserted upon termination as the other commands, or at the same time BDRQ is asserted. In either case, INTRQ remains asserted until the Host reads the Status Register to determine the result of the termination, or writes a new command into the Command Register.

The WD2010 asserts $\overline{SDHLE}$ to the Host whenever the SDH register is being written into. This makes it possible to store the same information in an external register for decoding. Figure 3 illustrates one method.

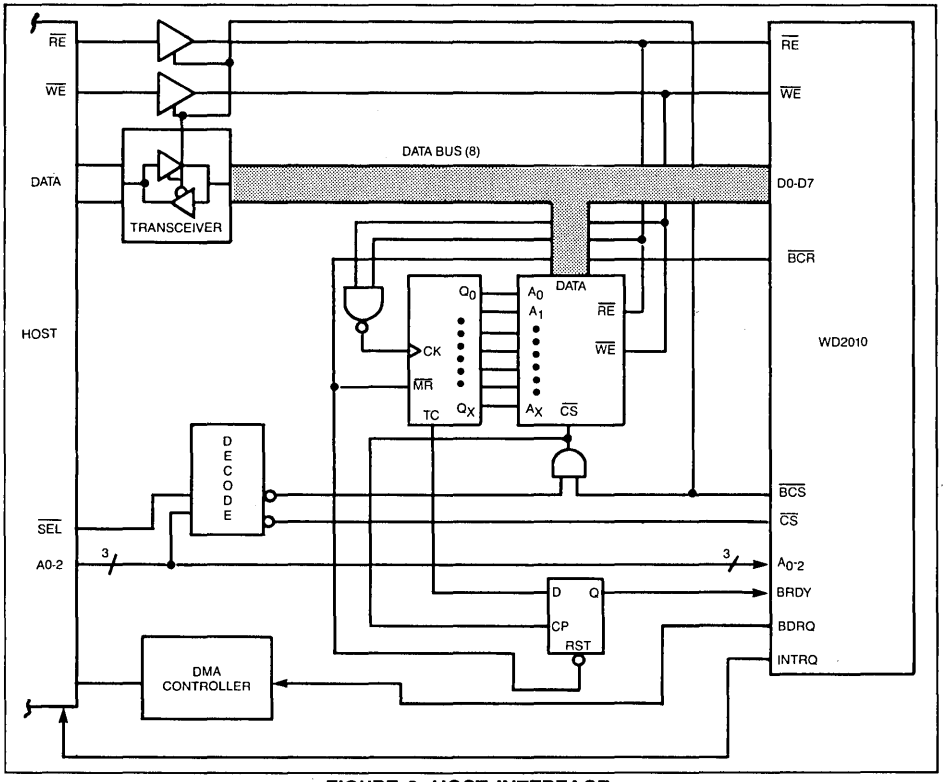


FIGURE 2. HOST INTERFACE

Drive Interface

The drive side of the WD2010 controller requires three sections of external logic. These are interface/ Sector Buffers, data separator, and write precompensation. Figure 3A illustrates the drive interface.

The control lines are buffered, single-ended, and resistor terminated at TTL levels. The data lines to and from the drive also require buffering, and are terminated with RS-422 drivers. The interface specification for the drive can be found in the manufacturer's OEM manual. The WD2010 supplies TTL compatible signals, and interfaces with most driver devices.

When the SDH Register is written into, the Head and Drive select signals are latched externally by the latch enable signal $\overline{\text{SDHLE}}$. See Figure 3B.

The data recovery circuits consist of a phase lock loop, data separator, and associated components. The WD2010 interacts with the data separator through DRUN and RG. The block diagram of the data separator circuit is illustrated in Figure 4. Data read from the drive is presented to the RD input of the WD2010, the reference multiplexor, and a retriggerable one shot. The RG is de-asserted when the WD2010 is not inspecting data. The PLL at this time should remain locked to the reference clock.

When any Read or Write Command is initiated and a search for an address mark begins, DRUN is examined. The DRUN one-shot is set slightly longer than one bit time, allowing it to retrigger constantly on a field of all ones or all zeros. An internal counter times out to see that DRUN is asserted for 2 byte times. RG is asserted by the WD2010 switching the data separator to lock onto the incoming data stream. If DRUN is de-asserted prior to 7 byte times, RG is de-asserted and the process is repeated. RG remains asserted until a non-zero, address mark is detected. It then de-asserts RG for two byte times (to allow the PLL to lock back on the reference clock) and starts the DRUN search over again. If an address mark is

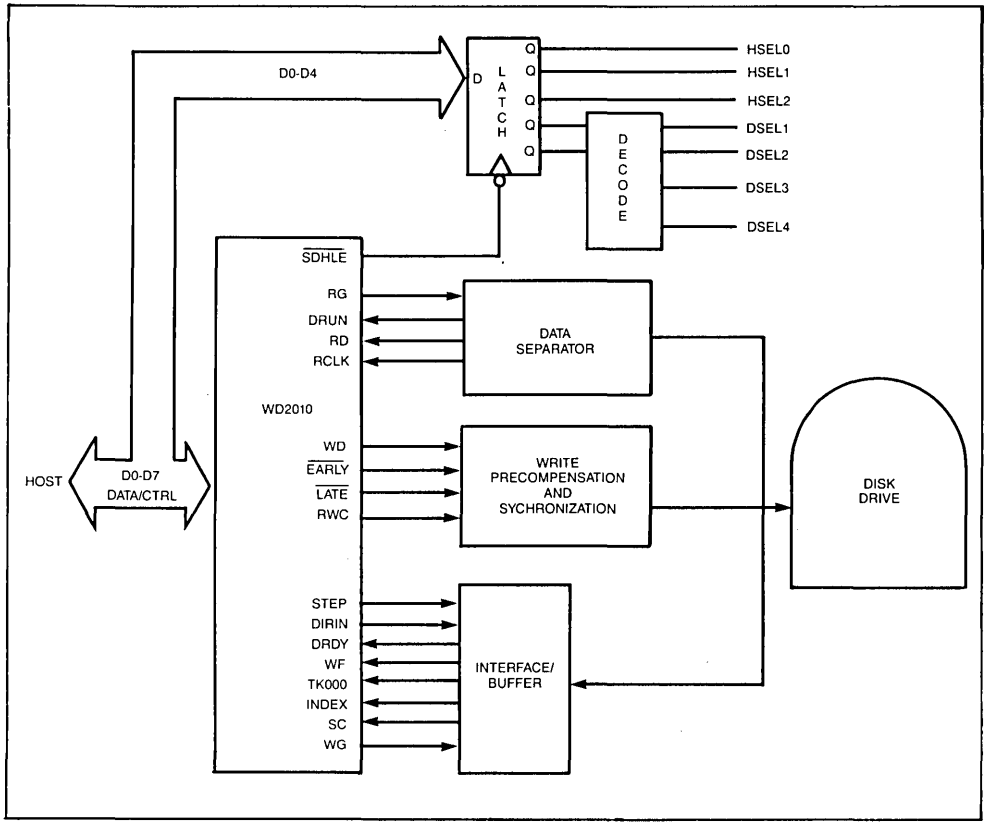


FIGURE 3A. DRIVE INTERFACE BLOCK DIAGRAM

detected, RG remains asserted and the command continues searching for the proper ID field. This sequence is illustrated in Figure 5.

The Write Precompensation circuitry is designed to reduce the shift in the data caused by the effect one bit has over another. The Write precompensation logic is divided into two areas: RWC and Early or Late writing of the bits. A block diagram of the Write Precomp circuit is illustrated in Figure 6.

RWC is controlled by the Write Precomp Cylinder Register in the Task File. This register is written into by the Host. When a cylinder is called for that is equal to, or greater than the content of this register, the write current will be reduced, thus lessening the effect one bit can have over another.

Shift may also be caused by the bit pattern. With certain combinations of ones and zeros some of the bits can drift far enough apart to become difficult to read without error. This phenomenon can be minimized by using EARLY and LATE as described under MFM Encoder.

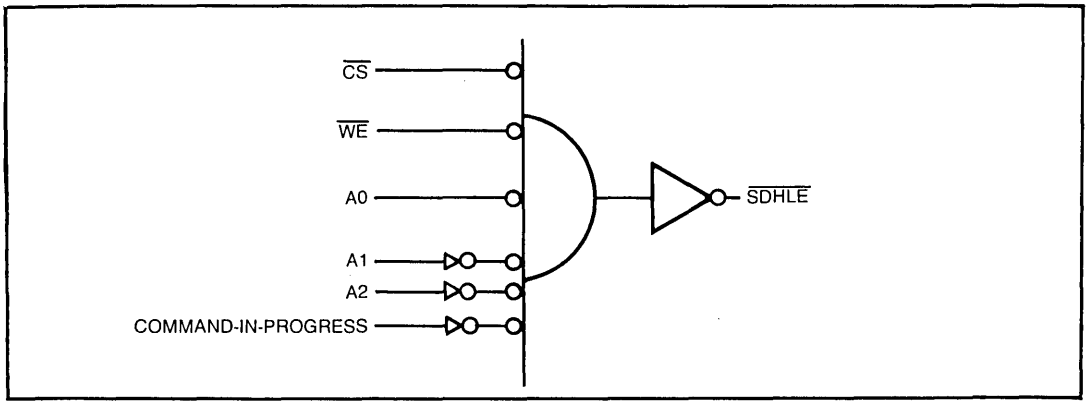


FIGURE 3B. LATCH ENABLE SIGNAL

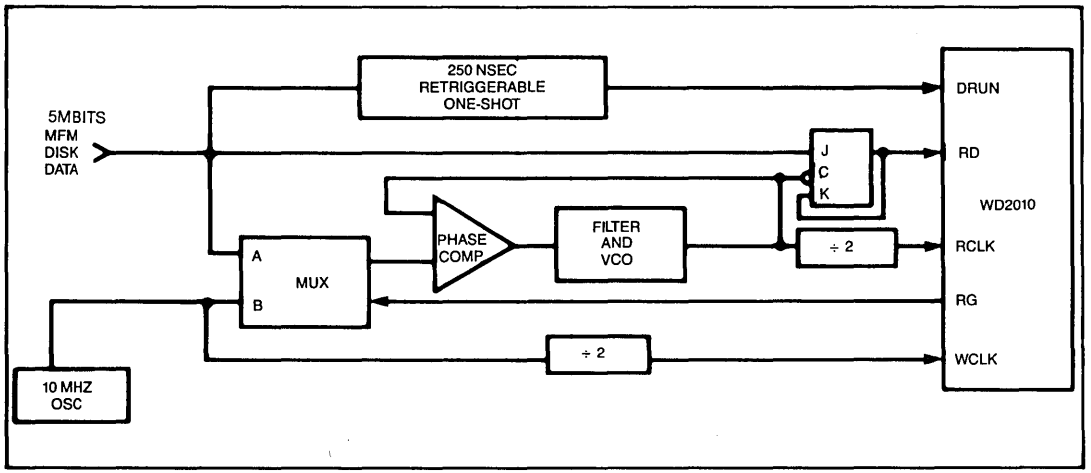


FIGURE 4. DATA SEPARATOR CIRCUIT

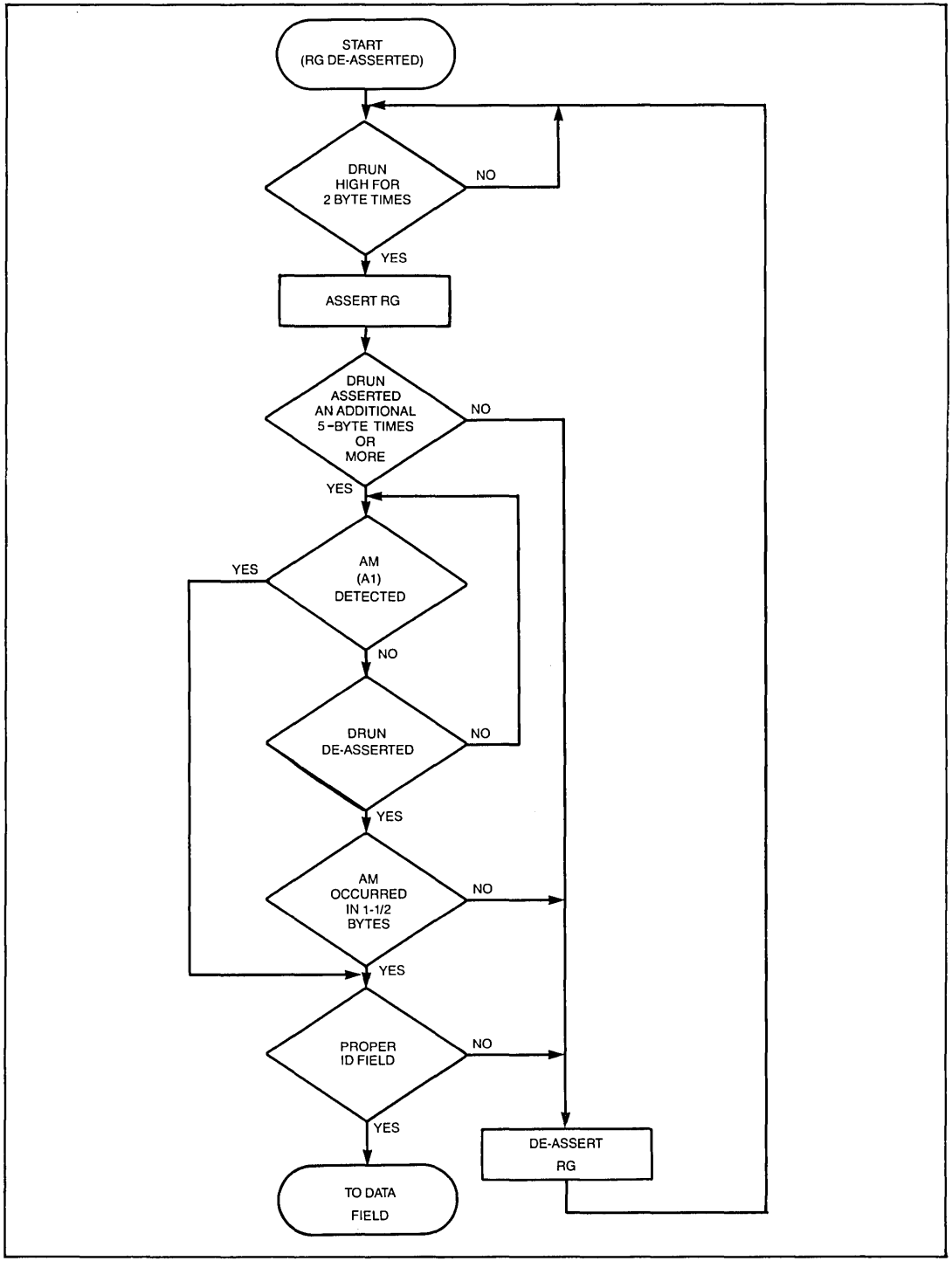


FIGURE 5. PLL CONTROL SEQUENCE FOR ID FIELD

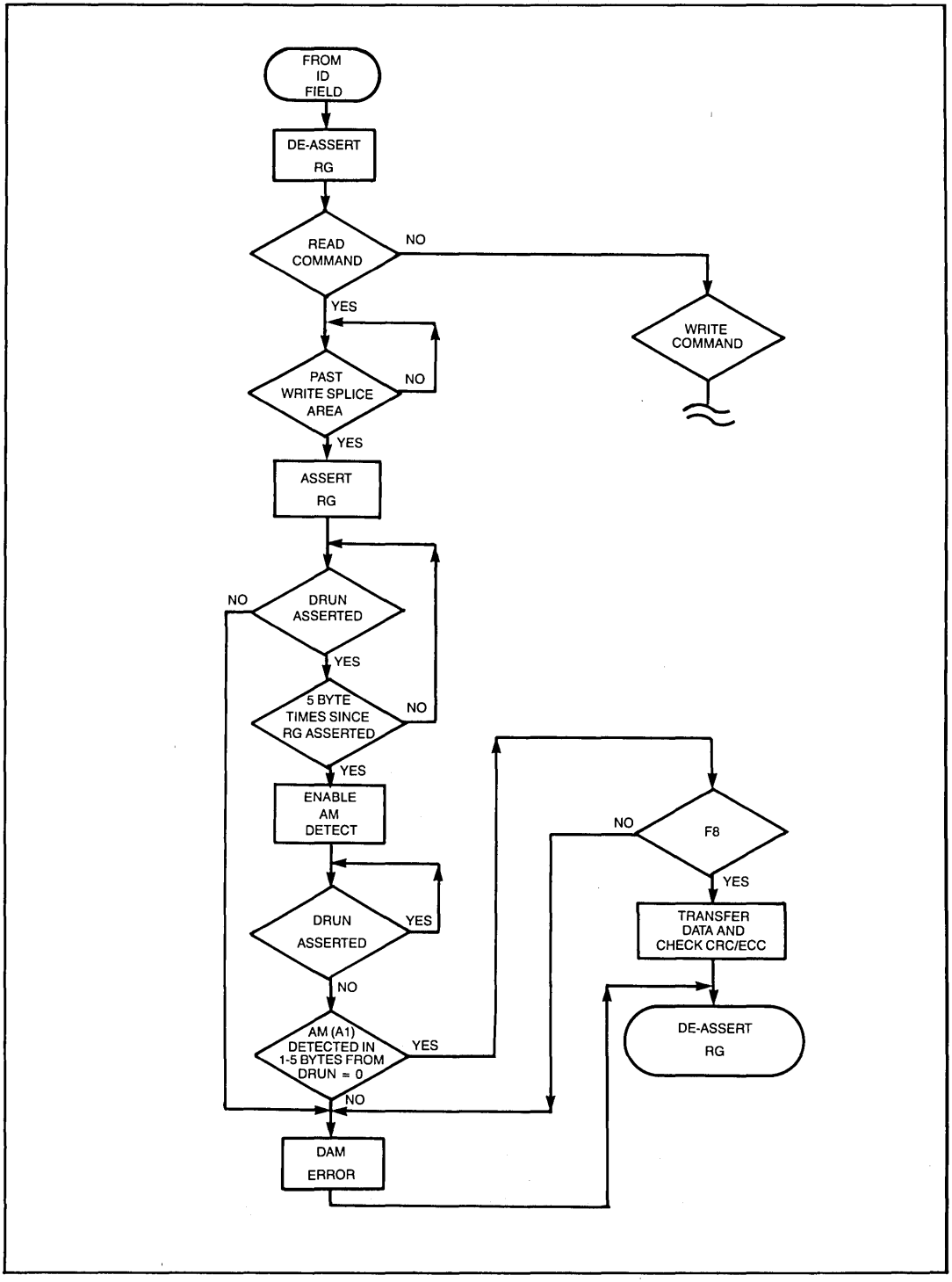


FIGURE 5A. PLL CONTROL SEQUENCE FOR DATA FIELD

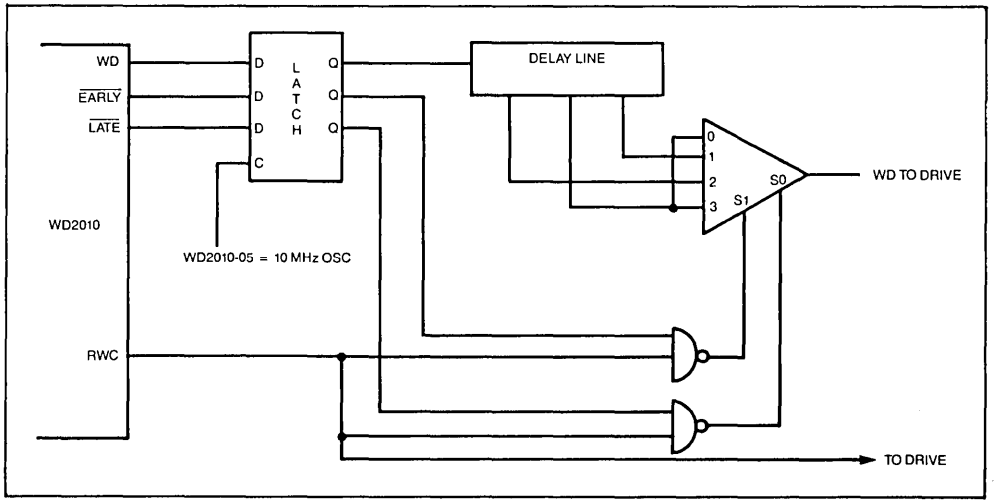


FIGURE 6. WRITE PRECOMPENSATION CIRCUIT

TASK FILE

The Task File is a bank of nine, 8-bit registers used to hold status information indicating the success or failure of an operation, as well as the parameters under which the drive is to operate. They are addressed by A0 through A2 lines. A0 through A2 = 0 is unused by the WD2010 and when received, puts its bus in the tri-stated condition isolating it from the bus.

ERROR REGISTER (A2 thru A0 = 1 READ)

This register contains specific error status pertaining to the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC/ECC	0	ID	0	AC	TK	DM

BIT 7 - BAD BLOCK DETECT

This bit is set when an ID field has been encountered that contains a Bad Block Mark. It is used for bad sector mapping.

BIT 6 - CRC/ECC DATA FIELD ERROR

CRC mode of operation (SDH 7 = 0): this bit is set when a CRC error occurs in the data field. When Retry is enabled, ten more attempts are made to read the sector correctly. If none of these attempts are successful, bit zero in the Status Register is set also. If one of the attempts is successful, this bit remains set to inform the Host that a marginal condition exists. However, the zero status bit is not set. No attempt is made to correct the error.

ADDRESS			TASK FILE	
A2	A1	A0	READ ONLY	WRITE ONLY
0	0	0	**BUS TRI-STATED**	
0	0	1	Error Register	Write Precomp Cylinder
0	1	0	Sector Count	
0	1	1	Sector Number	
1	0	0	Cylinder Low	
1	0	1	Cylinder High	
1	1	0	SDH Register	
1	1	1	Status Register	Command Register

NOTE: These registers are not cleared by $\overline{MR}$ being asserted

ECC mode of operation (SDH 7 = 1). This bit is set when the first non-zero syndrome is detected. When Retry is enabled, up to ten attempts are made to correct the error. If successful, this bit remains on. However, bit 2 of the Status Register is set to inform the Host that the error has been corrected. If unsuccessful, this bit remains on and bit zero of the Status Register is set also. When Retry is disabled no attempt is made to correct the error.

The data may be read even if errors do exist.

Note: If the Long Mode bit is set in the Read or Write command, no error checking is performed.

Bit 5–Reserved

Not used, forced to zero.

Bit 4–ID Not Found

This bit is set to indicate that the correct cylinder, head, sector, or size parameter could not be found, or a CRC error occurred on the ID field. This bit is set on the first failure and remains set even if the error is recovered on a retry. When recovery is unsuccessful, the Error Status bit is set also.

For a Scan ID Command with retry enabled (T = 0), the Error Status bit is set after ten unsuccessful attempts have been made to find the correct ID. With Retry disabled (T = 1) only two attempts are made before setting the Error Status.

For a Read and Write Command with Retry enabled (T = 0), ten attempts are made to find the correct ID field. If there is still an error on the tenth try, an auto-scan and auto-seek are performed. Then, ten more tries are made before setting the Error Status. When the Retry is disabled (T = 1) only two tries are made, and no auto-scan or auto-seek operations are performed.

Bit 3–Reserved

Not used, forced to zero.

Bit 2–Aborted Command

The command is aborted and this bit set if, DRDY has not been asserted, WF is asserted, or the command issued had an undefined command code.

Bit 1–Track Zero Error

This bit is set during a Restore Command when TK000 input has not indicated that the head has reached track zero by 2047 steps.

Bit 0– Data Address Mark Not Found

This bit is set during a Read Sector Command if the Data Address Mark is not found following the proper sector ID.

WRITE PRECOMP CYLINDER (A2 thru A0 = 1 write)

This register is used to define the cylinder number where the RWC output signal is to be asserted.

7	6	5	4	3	2	1	0
CYLINDER NUMBER ÷ 4							

The value 00-FF loaded into this register is internally multiplied by four to specify the actual cylinder where RWC is to be asserted. Thus a value of 9C Hex causes the RWC to be asserted on cylinder 270 Hex, 9D Hex on cylinder 274 Hex, etc. RWC is asserted when the present cylinder is equal to, or greater than the value of this register. For example, the ST506 requires precomp 80 Hex (128 dec.) and above. Therefore, the write precomp cylinder should be loaded with 20 Hex (32 dec.).

A value of FF Hex causes RWC to remain de-asserted, regardless of the cylinder number values.

SECTOR COUNT (A2 thru A0 = 2)

In a muliple sector operation, this register contains the number of sectors involved with Read Seector, Write Sector, and Format commands.

7	6	5	4	3	2	1	0
NUMBER OF SECTORS							

The value written into this register is decremented by one after each sector is transferred to or from the Sector Buffer. A zero represents a 256 sector transfer, a 1 = one sector, etc. This register is disregarded when a single sector command is specified.

SECTOR NUMBER (A2 thru A0 = 3)

This reigister holds the number of the desired sector.

7	6	5	4	3	2	1	0
SECTOR NUMBER							

This is the starting sector in a multiple sector command. It is incremented by one after each sector has been transferred to or form the Sector Buffer. The register can contain any value from 0 to 255.

This register also specifies the minimum GAP 3 length, minus 3, during a Format Command.

CYLINDER NUMBER LOW (A2 thru A0 = 4)

This register holds the least significant 8 bits of the desired cylinder number.

7	6	5	4	3	2	1	0
LS BYTE OF CYL. NUMBER							

It is used in conjunction with the Cylinder Number High Register to specify a range of 0 to 2047.

CYLINDER NUMBER HIGH (A2 thru A0 = 5)

This register contains the three most significant bits of the desired cylinder number.

7	6	5	4	3	2	1	0
X	X	X	X	X	#	#	#

These registers determine where the R/W heads are to be positioned. The Host writes the desired cylinder number into these registers. Internal to the WD2010 is another pair of registers pointing to where the heads are presently located. When any command, other than a Restore, is executed these registers are compared. The difference between them results in DIRIN and STEP signaling the drive how many cylinders to move the heads and in which direction.

The Present Cylinder Position Register is updated to equal the cylinder Number Register at the completion of the seek.

When a Restore Command is executed, the Present Cylinder Position Register is reset to zero, while DIRIN and STEP move the heads to track zero.

SDH REGISTER (A2 thru A0 = 6)

This register contains the desired sector size, drive number, and head number parameters.

7	6 5	4 3	2 1 0
EXT	SIZE	DRIVE	HEAD

6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL1
0	1	DSEL2
1	0	DSEL3
1	1	DSEL4

2	1	0	HEAD #
0	0	0	HSEL0
0	0	1	HSEL1
0	1	0	HSEL2
0	1	1	HSEL3
1	0	0	HSEL4
1	0	1	HSEL5
1	1	0	HSEL6
1	1	1	HSEL7

NOTE:

Drive select and head select lines must be generated externally. Figure 3 represents one method of achieving this.

As shown below, the SDH byte written in the ID field during the Format Command is not the same as the contents of the SDH Register.

Bit 7 – One selects the ECC mode for the data field. Zero selects the CRC mode for the data field.

7	6 5	4 3	2 1 0
BAD B.	SIZE	0 0	HEAD

STATUS REGISTER (A2 thru A0 = 7 READ)

The Status Register is used to inform the Host of certain events performed by the WD2010 as well as reporting status from the drive control lines. Reading the Status Register de-asserts INTRQ.

A SCAN ID Command reads the cylinder number from the track on which the heads are presently located, and writes this into the Present Cylinder Position Register.

When a different drive is selected just prior to a Read, Format, Write, or Seek command, the WD2010 issues an auto-scan ID command. This updates the Present Cylinder Position Register to reflect the position of the heads on this drive.

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	DWC	CIP	ERR

Bit 7 - Busy

BUSY is asserted when a command is written into the Command Register and, except for the Read Command, it is de-asserted at the end of the comand. When executing a Read Sector Command, BUSY is de-asserted when the Sector Buffer is full. Commands should not be loaded into the Command Register when this bit is set. When the BUSY bit is set, no other bits in the Status or Error Register are valid.

Bit 6 - Ready

This bit reflects the status of DRDY. When this bit equals zero, the command is aborted and the status of this bit is latched.

Bit 5 - Write Fault

This bit reflects the status of WF. When this bit equals one, the command is aborted, INTRQ is asserted, and the status of this bit is latched.

Bit 4 - Seek Complete

This bit reflects the status of SC. When a seek or implied seek has been initiated by a command, it pauses until the seek is complete, This bit is latched after an "aborted command" error.

Bit 3 - Data Request

DRQ reflects the same status as BDRQ. It is asserted when the data Sector Buffer must be written into, or read from. DRQ and BDRQ remain asserted until BRDY indicates that the Sector Buffer has been filled or emptied, depending upon the command. DRQ is used during Program Interrrupt and must be interrogated by the Host to determine that the WD2010 is ready. BDRQ operates through a DMA controller for data transfers.

Bit 2 - Data Was Corrected

When a one, this bit indicates an error has been detected during the ECC mode of operation and the data in the Sector Buffer has been corrected. This provides the user with an indication that there may be a marginal condition within the drive before the errors become uncorrectable. This bit is forced to zero when not in the ECC mode of operation.

Bit 1 - Command in Progress (CIP)

When this bit is set, a command is being excuted and a new command should not be loaded. Although a command is being executed the Sector Buffer is still available for access by the Host. When WD2010 is no longer busy, (bit 7 = 0) the Status Register can be read. An attempt to read the other registers results in reading the status.

Bit 0 - Error

This bit indicates that a non-recoverable error has occurred. When the Host reads the status and finds this bit set, it must then read the Error Register to determine what type of error it was.

COMMAND REGISTER (A2 thru A0 = 7 write)

The command to be executed is written into this register.

7	6	5	4	3	2	1	0
COMMAND							

The command asserts BUSY and CIP, and begins to execute as soon as it is written into this register. Therefore, all necessary information should be loaded into the Task File prior to entering the command. Any attempt to write into these registers is ignored until the command has terminated, as indicated by the CIP status. INTRQ is de-asserted if it is still active at the time the command is written.

COMMAND SUMMARY:

	BIT							
COMMAND	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESTORE	0	0	0	1	R3	R2	R1	R0
SEEK	0	1	1	1	R3	R2	R1	R0
READ SECTOR	0	0	1	0	I	M	L	T
WRITE SECTOR	0	0	1	1	0	M	L	T
SCAN ID	0	1	0	0	0	0	0	T
WRITE FORMAT	0	1	0	1	0	0	0	0
COMPUTE CORRECTION	0	0	0	0	1	0	0	0
SET PARAMETER	0	0	0	0	0	0	0	S

Stepping Rate Field R3-R0

For 5 MHz WCLK:

R3-R0 = 0000-35μsec
0001-.5msec
0010-1.0msec
0011-1.5nsec
0100-2.0msec
0101-2.5msec
0110-3.0msec
0111-3.5msec
1000-4.0msec
1001-4.5msec
1010-5.0msec
1011-5.5msec
1100-6.0msec
1101-6.5msec
1110-3.2μsec
1111-16μsec

STEP PULSE WIDTH =
1.6μsec at 3.2μsec rate
8.0μsec at all others.

I - Interrupt Control

I = 0 INTRQ occurs with BDRQ/DRQ indicating the Sector Buffer is full (valid only when M = 0).

I = 1 INTRQ occurs when the command is completed and the Host has read the Sector Buffer.

M - Multiple Sector Flag

M = 0 Transfer one sector (the sector count is ignored)

M = 1 Transfers multiple sectors

L - Long Mode

L = 0 Normal mode, normal CRC or ECC functions are performed.

L = 1 Long mode, no CRC or ECC bytes are developed or error checking performed on the data field. The WD2010 appends the four additional bytes supplied by the Host or disk to the data field.

T - Retry Flag

T = 0 Enable Retry

T = 1 Disable Retry

S - Error Correction Span

S = 0 5-bit span

S = 1 11-bit span

RESTORE COMMAND

The Restore command is used to position the read/write heads over track zero. It is usually issued by the Host when a drive has just been turned on.

The stepping rate used for the restore is determined by SC. The WD2010 issues a Step pulse and then waits for the leading edge of SC before starting another step. If the leading edge of SC is not seen within 10 revolutions (index pulses) the WD2010 switches to sensing the level of SC. If after 2047 Stepping pulses TK000 is not asserted, the WD2010 sets the Track Zero error bit, asserts INTRQ and terminates the operation. An interrupt also occurs if WRITE FAULT is asserted or DRDY is de-asserted during execution.

The stepping rate field is stored in an internal register for future use by commands with implied seeks.

SEEK COMMAND

By not testing SC, the Seek Command is capable of overlapping seeks on multiple drives. R3 through R0 controls the stepping rate, as well as being written into an internal register for use by those commands with implied seek capability.

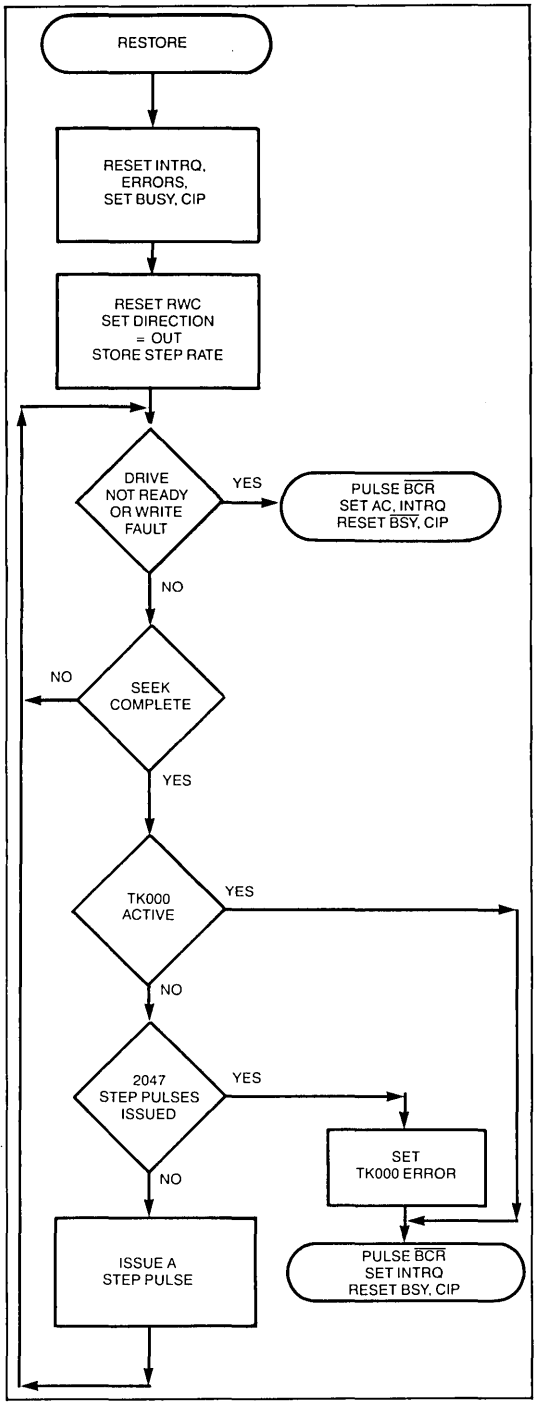


FIGURE 7. RESTORE COMMAND

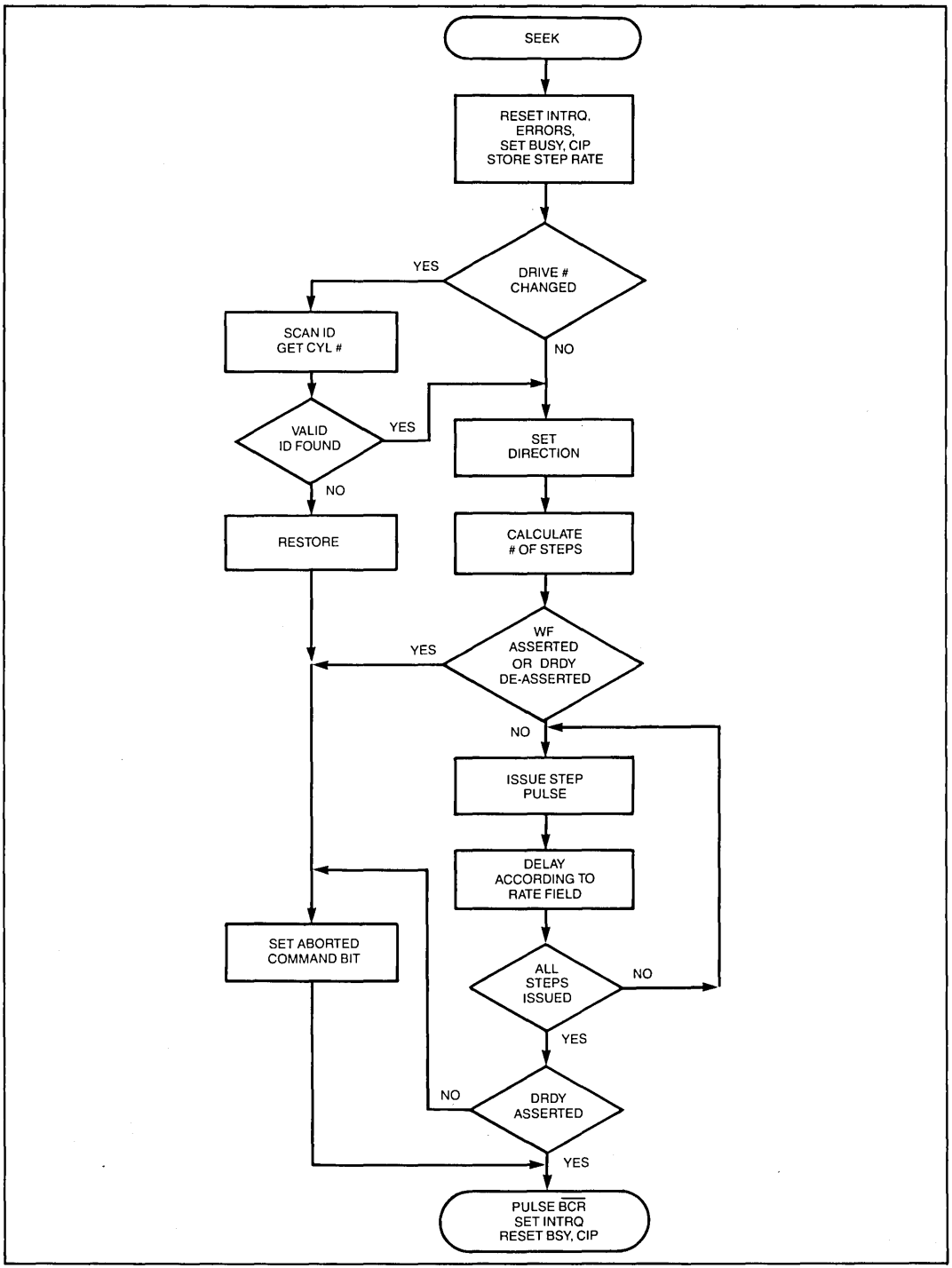


FIGURE 8. SEEK COMMAND

The direction and number of step pulses needed are calculated by comparing the contents of the cylinder number in the Task File to the present cylinder position number stored internally. After all the steps have been issued, the present position cylinder number is updated, INTRQ asserted and the command terminated. if DRDY is de-asserted or WF is asserted during the execution of the command, INTRQ is asserted, and the command aborts setting the AC error.

If an implied seek is performed, the stepping rate for all but the last step is controlled by R3 through R0. On the last step the seek continues until the leading edge of SC is detected.

READ SECTOR

The Read Sector command is used to transfer one or more sectors of data from the disk to the Sector Buffer. Upon receipt of this command, the WD2010 compares the cylinder number in the Task File with the Present Cylinder Position Register. From this, the direction and number of steps required for the seek are calculated. As stated in the Seek Command, if an implied seek is performed, the stepping rate for all but the last step is controlled by R3 through R0. On the last step the seek continues until the leading edge of SC is detected.

If the WD2010 detects a change in the drive number since the last Read Command, an Auto Scan ID is performed. This updates the Present Cylinder Position Register to reflect the current drive before the seek begins.

After the WD2010 senses SC (with or without an implied seek) it must find an ID field with the correct cylinder, head, sector size, and CRC. With Retry enabled (T = 0), ten attempts are made to find the correct ID field. If there is still an error on the tenth try, an auto-scan and auto-seek are performed. Then, ten more tries are made before setting the ID Not Found Error. When Retry is disabled (T = 1) only two tries are made, and no auto-scan or auto-seek operations are performed.

When the Data Address Mark is found the WD2010 is ready to transfer data into the Sector Buffer (if after successfully reading the correct ID field the Data Address Mark is not found a DAM error is set). When the disk has filled the Sector Buffer, the WD2010 asserts BDRQ and DRQ and then checks the I flag. If the flag is 0, INTRQ is asserted also, signaling the Host to read the content of the Sector Buffer. If the I flag is 1, INTRQ occurs after the Host has read the Sector Buffer and terminated the command.

An optional M flag can be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD2010 decrements the sector count and increments the sector number. The next logical sector is transferred, regardless of the interleave. Sectors are numberd by a byte in the ID field during the Format Command.

For the WD2010 to make multiple sector transfers to the Sector Buffer, the BRDY signal must toggle from low to high for each sector. The sector transfers continue until the sector count equals zero. If the sector count is not zero (indication more sectors are to be read) and the Sector Buffer is full, BDRQ is asserted and the Host must unload the Sector Buffer. Once this occurs, the Sector Buffer is free to accept the next sector.

WF and DRDY are monitored throughout the command. If WF becomes asserted, or DRDY de-asserted, the command terminates and the AC error flag is set. For a description of the error checking procedure on the data field see the explanation under CRC and ECC Generator and Checker. Both the Read and Write commands feature a simulated completion to ease programming. BDRQ, DRQ, and INTRQ are generated in a normal manner upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command.

When M = 0 (Single Sector Read)

(1)	Host:	Sets up parameters; issues Read Sector command.
(2)	2010:	Finds sector specified; asserts BCR and BCS. Sector Buffer data transfer via WE.
(3)	2010:	Asserts BCR de-asserts $\overline{BCS}$.
(4)	2010:	Asserts BDRQ and DRQ flag.
(5)	2010:	If 1 bit = 0 then (8).
(6)	Host:	Reads contents of Sector Buffer (by asserting RE).
(7)	2010:	Waits for BRDY the asserts INTRQ; End.
(8)	2010:	Asserts INTRQ.
(9)	Host:	Reads contents of Sector Buffer (by asserting RE);End.

When M = 1 (Multiple Sector Read)

(1)	Host:	Sets up parameters; issues Read Sector command.
(2)	2010:	Finds sector specified; asserts BCR and BCS. Sector Buffer data transfer via WE.
(3)	2010:	Asserts BCR; de-asserts $\overline{BCS}$.
(4)	2010:	Asserts BDRQ and DRQ flag.
(5)	Host:	Reads contents of Sector Buffer (by asserting RE).
(6)	Sector Buffer:	Indicates data has been transferred by asserting BRDY.
(7)	2010:	When BRDY is asserted, decrements sector count; increments sector number, go to (9) if sector count = 0.
(8)	2010:	Go to Step (2).
(9)	2010:	Asserts INTRQ; End.

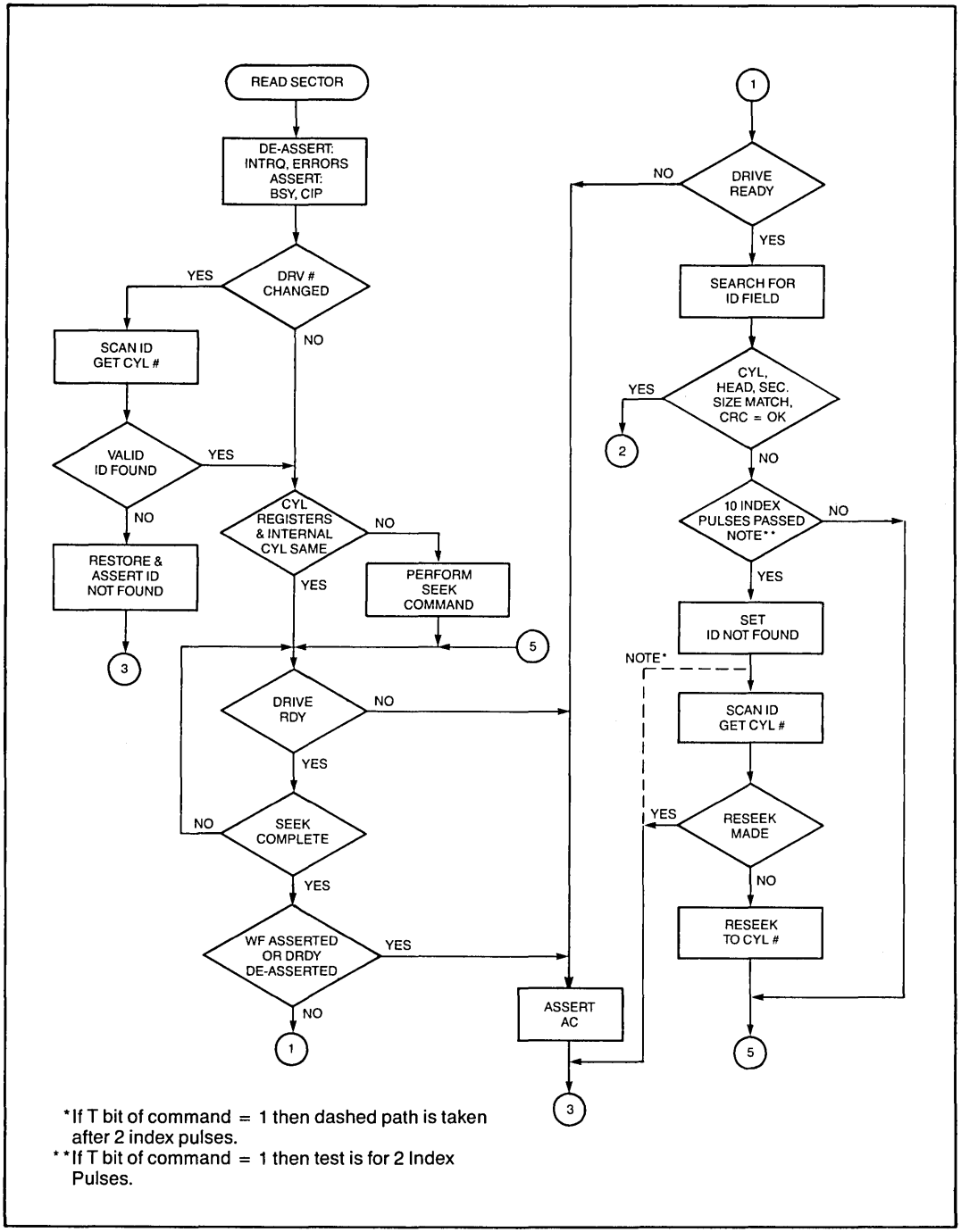


FIGURE 9. READ COMMAND

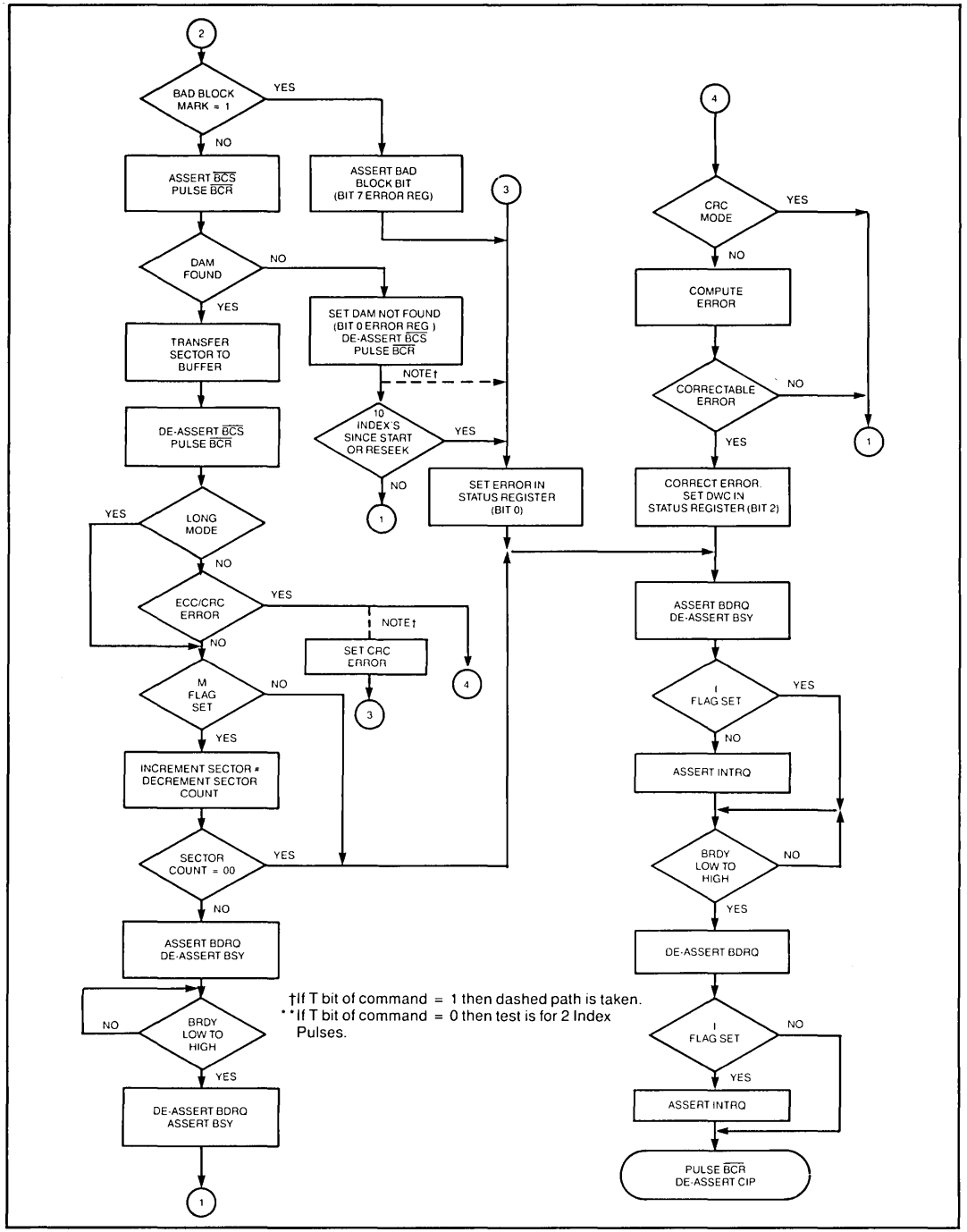


FIGURE 9. READ COMMAND (Continued)

WRITE SECTOR

The Write Sector Command is used to write one or more sectors of data from the Sector Buffer to the disk. Upon receipt of this command, the WD2010 compares the cylinder number in the Task File with the present position cylinder number. From this, the direction and number of steps required for the seek are calculated. As stated in the Seek Command, if an implied seek is performed, the stepping rate is controlled by R3 through R0. After the last step the WD2010 waits until the leading edge of SC is received.

If the WD2010 detects a change in the drive number since the last Write Command, an auto-Scan ID takes place. This updates the Present Cylinder Position Register to reflect the current drive before the seek begins.

After the WD2010 senses SC (with or without an implied seek), BDRQ and DRQ signals are asserted and the Host proceeds filling the Sector Buffer. When BRDY is asserted, a search for an ID with the specified cylinder, head, sector size, and CRC is initiated. If the ID is not found and Retry is enabled (T = 0), ten attempts are made to find the correct ID field. If there is still an error on the tenth try, an auto-scan and auto-seek is performed. Then ten more tries are made before setting the Error Status bit. (The ID Not Found error is set on the first failure). When Retry is disabled (T = 1). Only two tries are made and no auto-scan or auto-seek operations are performed.

When the correct ID is found, WG is asserted and data is written to the disk. When SDH 7 bit is zero, WD2010 generates a two byte CRC character to be appended to the data. When SDH 7 bit is one, four ECC bytes replaces the CRC character. When the L bit within the Write Command is one, the polynomial generation of the data is inhibited, and neither CRC or ECC bytes are generated. Instead, four bytes of data supplied by the Host is written.

During a multiple sector write operation (M flag = 1), the sector number is incremented and sector count decremented. If BRDY is asserted after the first sector is read from the Sector Buffer, WD2010 continues to read data from the Sector Buffer for the next sector. If BRDY is de- asserted, WD2010 asserts BDRQ and waits for the Host to place data in the Sector Buffer.

Summary of a write sector operation:

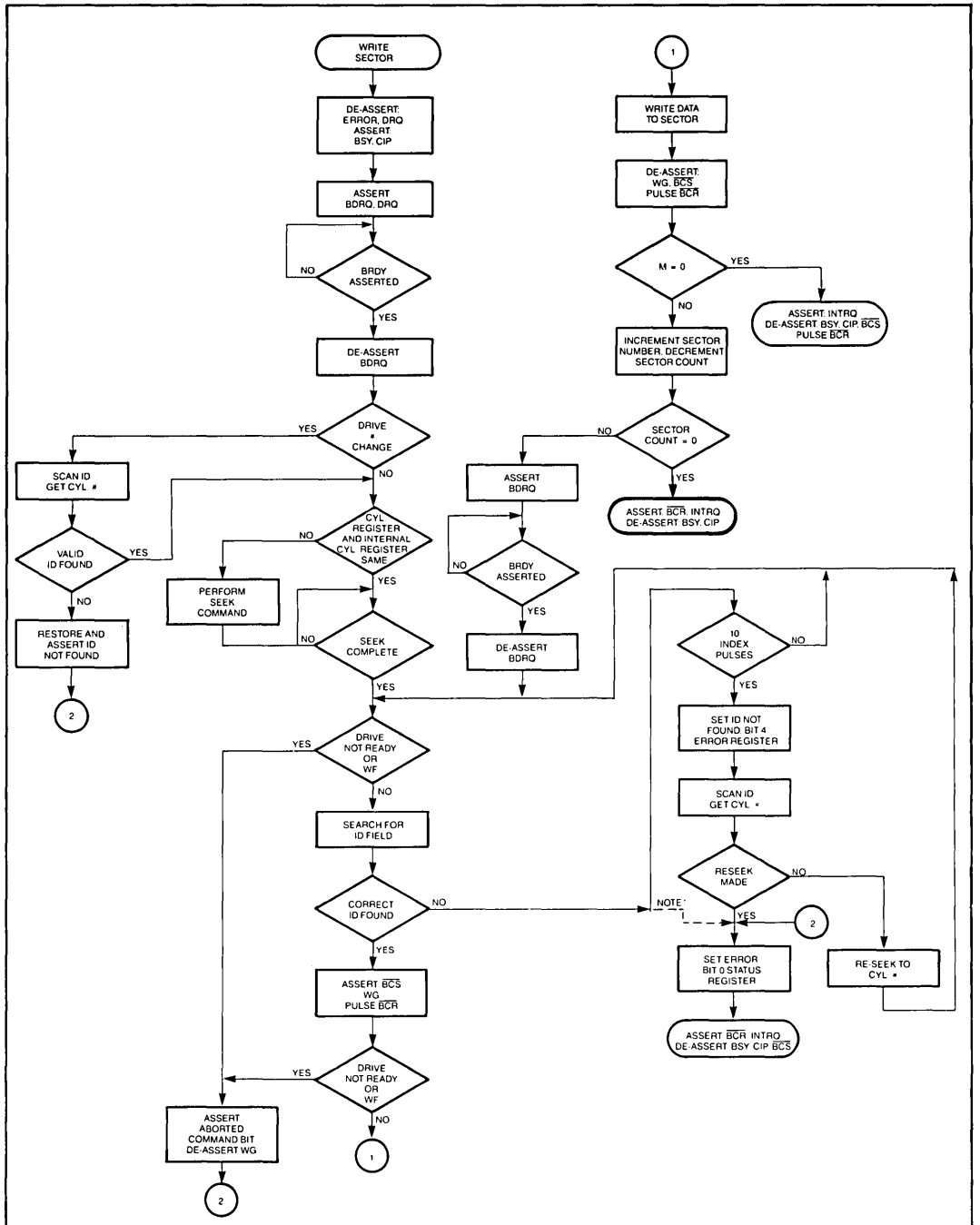
(1) Host: Sets up parameters; issues write sector command.
(2) 2010: Asserts BDRQ and DRQ.
(3) Host: Loads Sector Buffer with data (by asserting $\overline{WE}$).
(4) 2010: Waits for leading edge of BRDY.
(5) 2010: Finds specified ID field, write to sector.
(6) 2010: If M = 0, assert INTRQ; End.
(7) 2010: Increments sector number, decrements sector count.
(8) 2010: If sector count = 0, assert INTRQ; End.
(9) 2010: Go to (2).

SCAN ID

The Scan ID Command is used to update the head, sector size, sector number, and cylinder registers.

When the first ID field is encountered, the ID information is loaded into the SDH cylinder, and sector number registers in the Task File. The Present Position Cylinder Register is also updated. If this is an Auto- Scan caused by a change in drive numbers, only the present position cylinder number is altered.

If the ID field is not found and Retry is enabled (T = 0), ten attempts are made to read it. If Retry is disabled (T = 1), only two tries are made. There is no implied seek in this command and the Sector Buffer remains unchanged. When DRDY is de-asserted or WF asserted the command aborts and the appropriate error flags are asserted.



*If retries disabled then dashed path is taken after 2 Index Pulses.

FIGURE 10. WRITE COMMAND

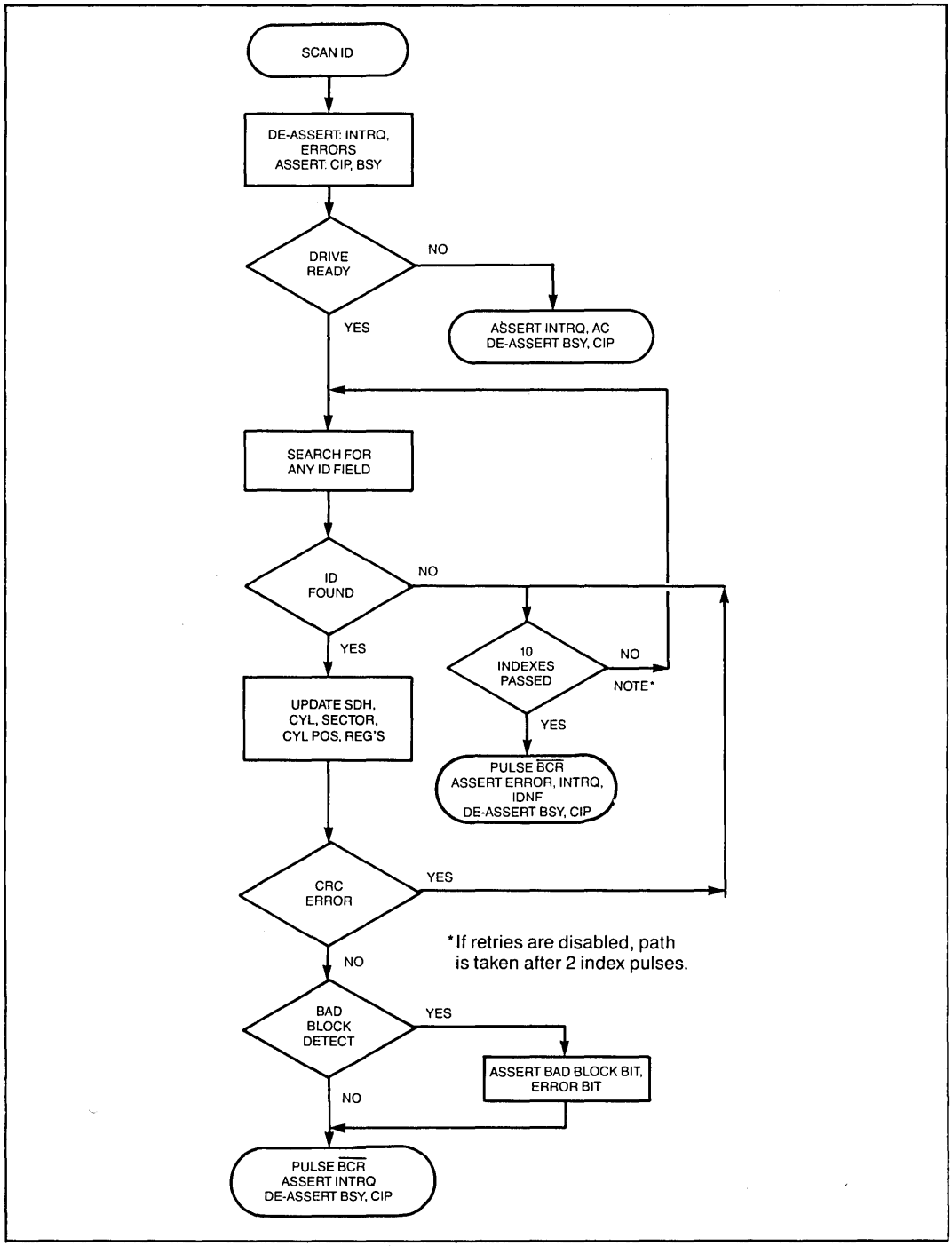


FIGURE 11. SCAN ID COMMAND

FORMAT

The Format Command is used to format one track using the Task File and Sector Buffer. During this command the Sector Buffer contains additional parameter information instead of data. Figure 12 shows the contents of the Sector Buffer for a 32 sector track format with an interleave factor of two.

Each sector requires a two byte sequence. The first byte designates if a Bad Block Mark is to be recorded in the ID field. A 00 is normal; an 80 Hex is a Bad Block Mark. In the example of Figure 12, sector 04 gets a Bad Block Mark recorded. The second byte indicates the logical sector number to be recorded. Using this scheme, sectors can be recorded in any interleave factor desired. The rest of the Sector Buffer is filled with any value, BRDY is asserted, and the WD2010 begins formatting the track.

The Sector Count Register holds the total number of sectors to be formatted, while the Sector Number Register holds the number of bytes, minus three, to be used for Gap 1 and Gap 3. For instance, if the Sector Count value is 2 and the Sector Number value is 3, then 2 sectors are written and 6 bytes of 4E Hex are written for Gap 1 and Gap 3. The data fields are filled with FF Hex, and the CRC or ECC is generated as specified by the related coding.

The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining the minimum Gap 3 is:

$$\text{Gap 3} = 2 \times M \times S + K$$

M = motor speed variation (e.g. .03 for ± 3%)
S = sector length in bytes
K = 18 for an interleave factor of 1
K = 0 for any other interleave factor

When WF is asserted or DRDY de-asserted the command terminates and the AC error is asserted. Figure 13 shows the format that is written on the disk.

	DATA							
ADDR	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
				.				
				.				
FO	FF	FF	FF	FF	FF	FF	FF	FF

FIGURE 12. FORMAT COMMAND BUFFER CONTENTS

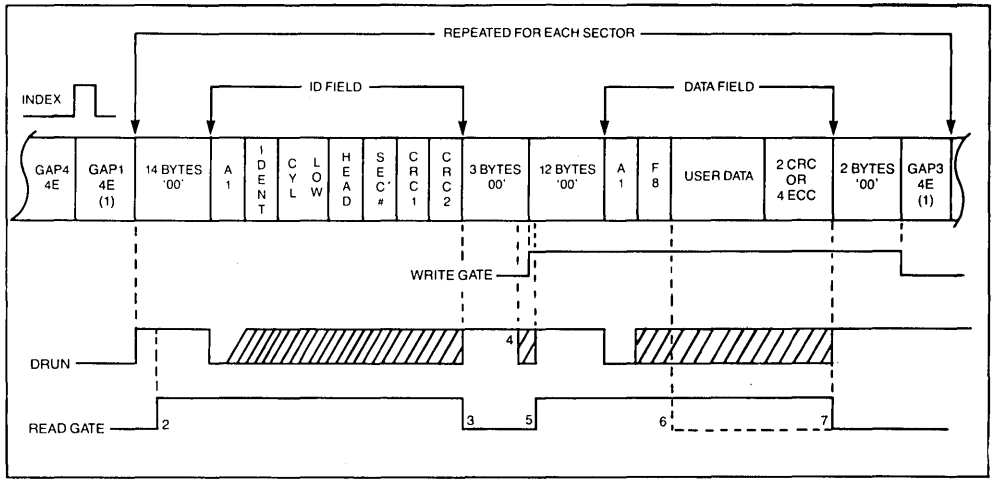


FIGURE 13. FORMAT

ID FIELD

A1 = A1 Hex with OA Hex clock

IDENT = Bits 3,1,0 = Cylinder High
- FE = 0-255 Cylinders
- FF = 256-511 Cylinders
- FC = 512-767 Cylinders
- FD = 768-1023 Cylinders
- F6 = 1024-1279 Cylinders
- F7 = 1280-1535 Cylinders
- F4 = 1536-1791 Cylinders
- F5 = 1792-2047 Cylinders

HEAD = Bits 0,1,2 = Head Number
- Bits 3,4 = 0
- Bits 5,6 = Sector Size
  - 00 = 256
  - 01 = 512
  - 10 = 1024
  - 11 = 128
- Bit 7 = Bad Block Mark

Sec# = Logical Sector Number

DATA FIELD

A1 = A1 hex with 0A hex clock

F8 = Data Address Mark; Normal Clock

USER = Data Field 128 to 1024 Bytes

NOTES:

1. GAP 1 and 3 length determined by Sector Number Register contents during formatting.
2. The decision to assert RG is made 2 bytes after the start of DRUN.
3. RG de-asserted:
   - If DRUN does not last until A1
   - When any part of ID does not match the one expected.
   - After CRC if correct ID has been read.
4. Write splice recorded on disk by asserting WG.
5. RG is suppressed until after write splice.
6. Not a proper A1 or F8, set DAM error.
7. Sector size as stated in ID field, plus two for CRC or 4 for ECC.

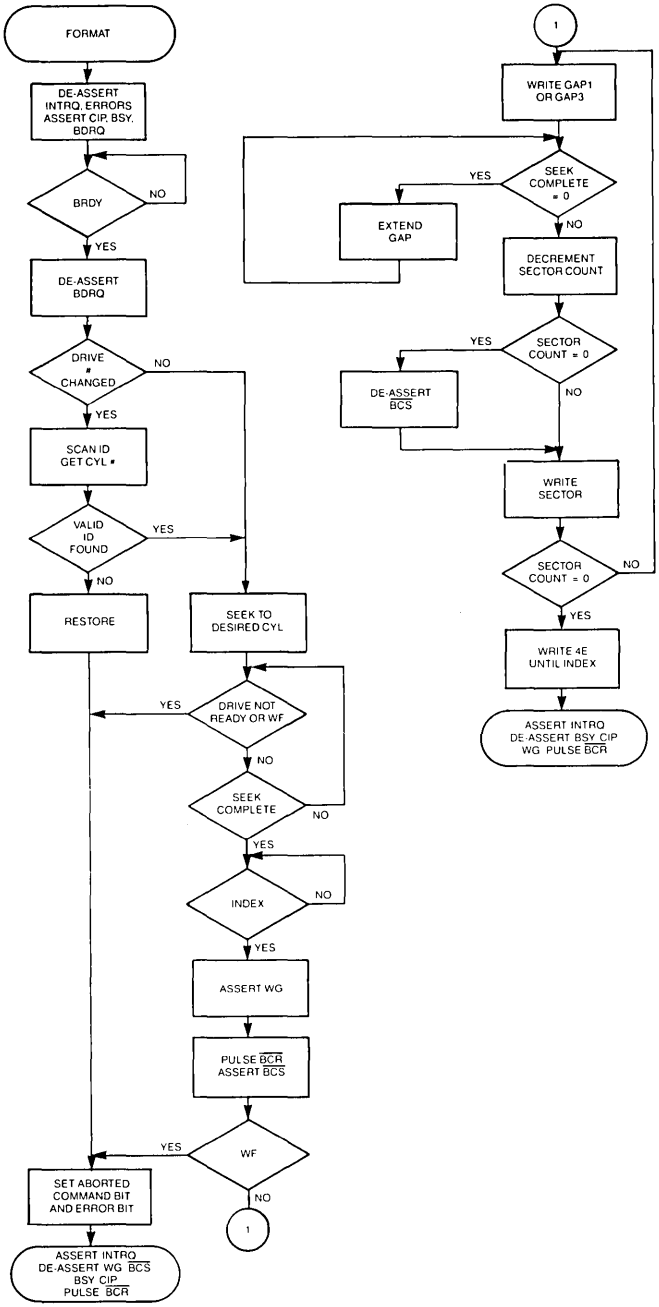


FIGURE 14. FORMAT COMMAND

COMPUTE CORRECTION

The Compute Correction Command determines the location and pattern of a single burst error, but does not correct it. The Host, using the data provided by the WD2010, must perform the actual correction. The Compute Correction Command is used following a data field ECC Error. The command initiating the read operation must specify no Retry. (T = 1).

The Compute Correction Command first writes the four syndrome bytes from the internal ECC Register to the Sector Buffer then the ECC Register is clocked. With each clock, a counter is incremented and the pattern examined. If the pattern is correctable, the procedure is stopped and the count and patten are written to the Sector Buffer, following the syndrome. The process is also stopped if the count exceeds the sector size before a correctable pattern is found.

When the command terminates the Sector Buffer contains the following data:

Syndrome	MSB
Syndrome	
Syndrome	
Syndrome	
Error Pattern Offset	
Error Pattern Offset	
Error Pattern	
Error Pattern	
Error Pattern	LSB

As an example, when the Error Pattern Offset is zero the following procedure may correct the error. The first data byte of the sector is eclusive OR'ed with the MSB of the Error Pattern. , the second byte of data with the second byte of the Error Pattern, and the third byte of data with the LSB of the Error Pattern.

If the Sector Buffer count exceeds the sector size, or the burst is greater than that selected buy the Set Parameter Command, the ECC/CRC error (bit 6) and the Error Status bit (bit 0) is set.

The WD2010 defaults to a 5-bit correction span if a Set Parameter Command has not been executed since the last $\overline{MR}$.

SET PARAMETER

This command selects the correction span to be used by the error correction process. A 5-bit span is selected when bit zero of the command equals 0, and 11-bit span when 1. The WD2010 defaults to a five bit span following a Master Reset.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground).....+7V
Max Voltage on any Pin with
respect to V_{SS}.....-0.5V to +7V
Operating Temperature. .0°C(32°F) to 70 °C(158 °F)
Storage Temperature. .-55°C(-67 °F) to + 125 °C (257°F)

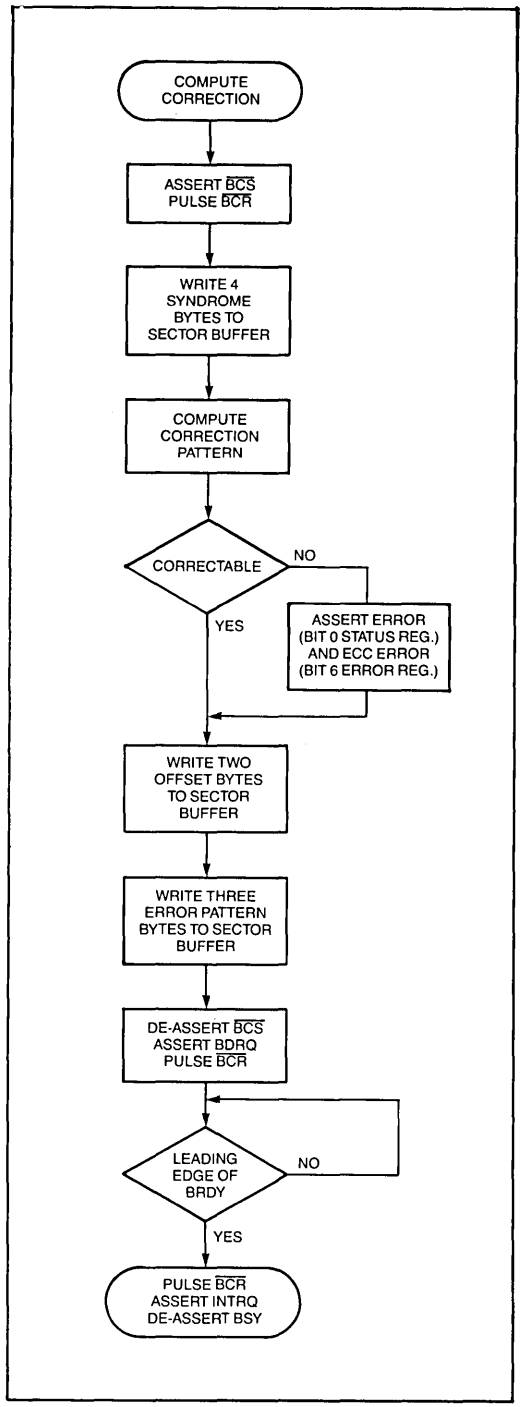
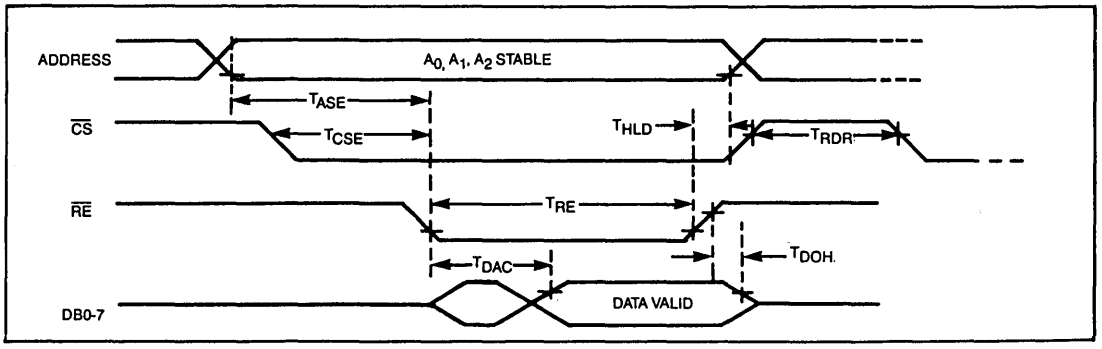


FIGURE 15. COMPUTE CORRECTION COMMAND

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating characteristics.

DC Operating Characteristics TA = 0 °C (32°F) to 70°C(158°F); V_{SS} = 0V, V_{CC} = +5V ±.25V

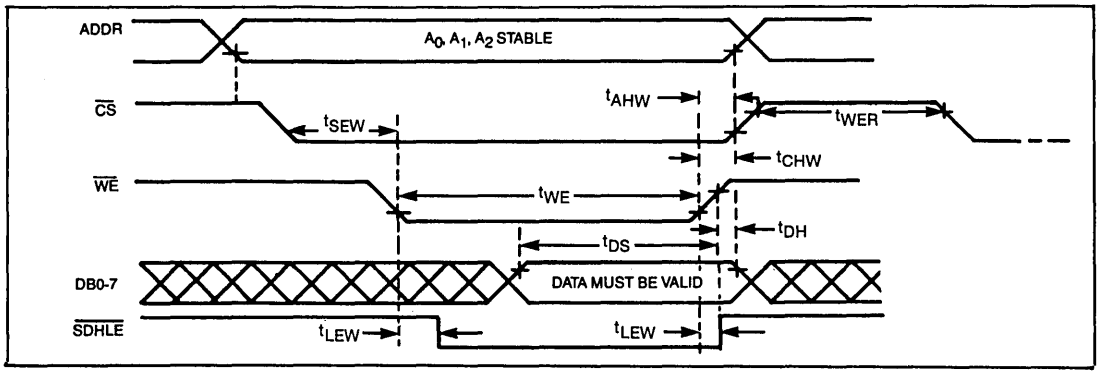
SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITION
I_{IL}	Input Leakage		± 10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Drain)		± 10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_O = −100μA
V_{OL}	Output Low Voltage		0.4	V	I_O = 1.6mA
V_{OL}	Output Low Voltage (Pins 21-23)		0.45	V	I_O = 6.0mA See Note 10
I_{CC}	Supply Current		220	mA	All Outputs Open
	For Pins 25, 34, 37, 39:				
V_{IH}	Input High Voltage	4.6		V	
VIL	Input Low Voltage		0.5	V	
TRS	Rise and Fall Time		30	nsec	.9V to 4.2V
CIN	Input Capacitance		15	pF	



HOST READ TIMING

HOST READ TIMING WD2010-05 WC = 5 MHz

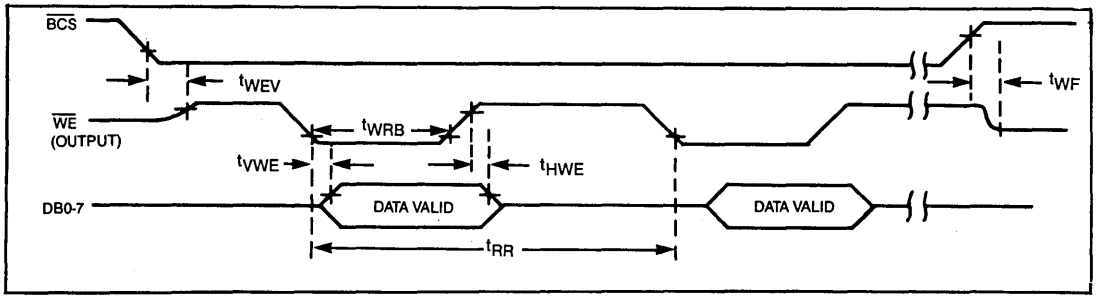
SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITION
t_{ASE}	Address Setup to $\overline{RE}$	100		nsec	
t_{DAC}	Data Valid from $\overline{RE}$		350	nsec	
t_{RE}	Read Enable Pulse Width	.4	10	μsec	
t_{DOH}	Data Hold from $\overline{RE}$	20	200	nsec	
t_{HLD}	Address $\overline{CS}$ hold from $\overline{RE}$	0		nsec	
t_{RDR}	Read Recovery time	300		nsec	
t_{CSE}	$\overline{CS}$ Setup to $\overline{RE}$	0		nsec	See Note 8



HOST WRITE TIMING

HOST WRITE TIMING WD2010-05

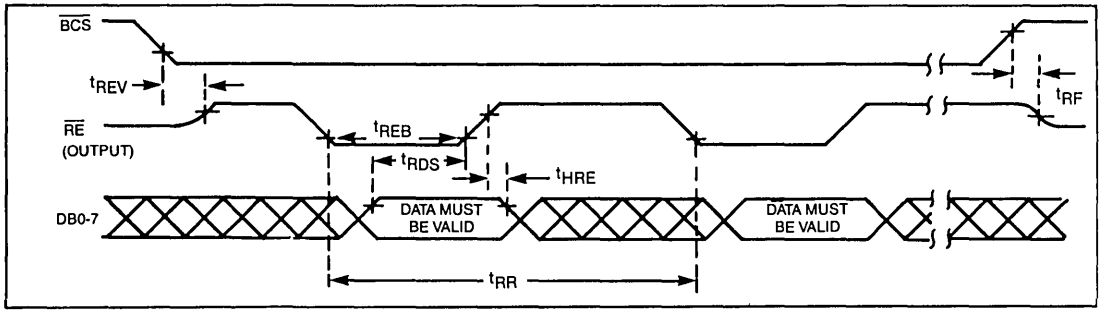
SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITION
t_{SEW}	Address $\overline{CS}$ Setup to $\overline{WE}$	0	10	μsec	
t_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	μsec	
t_{WE}	Write Enable Pulse Width	.2	10	μsec	
t_{DH}	Data Bus Hold from $\overline{WE}$	10		nsec	
t_{AHW}	Address Hold from $\overline{WE}$	30		nsec	
t_{WER}	Write Recovery Time	1.0		μsec	See Note 1
t_{CHW}	$\overline{CS}$ Hold Time from $\overline{WE}$	0			See Note 9
t_{LEW}	$\overline{SDHLE}$ Propagation Delay	20	150	nsec	



BUFFER WRITE TIMING

BUFFER WRITE TIMING (READ SECTOR CMD) WD2010-05 WC = 5MHz

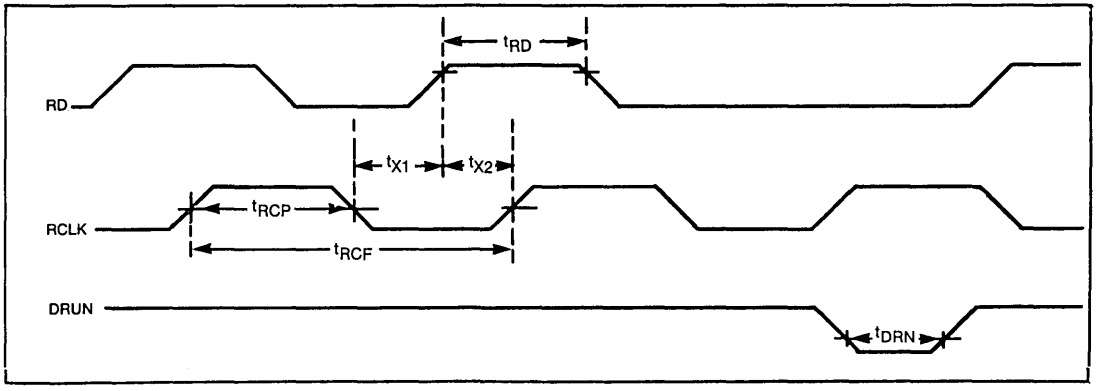
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{WEV}	$\overline{WE}$ float to $\overline{WE}$ Valid	0		100	nsec	C_L = 50 pf
t_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	nsec	See Note 4
t_{VWE}	Data Valid from $\overline{WE}$			150	nsec	
t_{HWE}	Data Hold from $\overline{WE}$	60		200	nsec	
t_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	μsec	
t_{WF}	$\overline{WE}$ Float from $\overline{BCS}$	0		100	nsec	C_L = 50 pf



BUFFER READ TIMING

BUFFER READ TIMING (WRITE SECTOR CMD) WD2010-05 WC = 5MHz

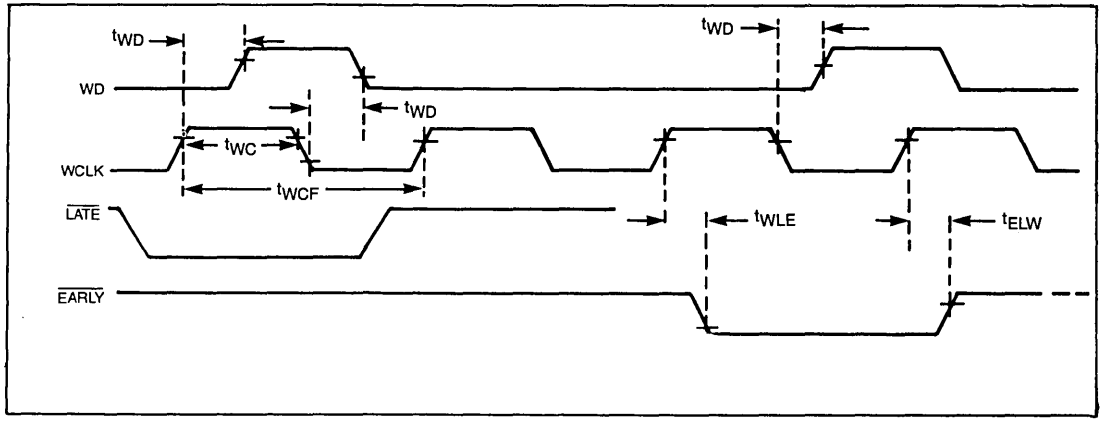
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{REV}	$\overline{RE}$ float to $\overline{RE}$ Valid	0		100	nsec	C_L = 50 pf
t_{REB}	$\overline{RE}$ Output Pulse Width	300	400	500	nsec	See Note 4
t_{RDS}	Data Setup to $\overline{RE}$	140			nsec	
t_{RR}	$\overline{RE}$ Repetition Rate	1.2	1.6	2.0	μsec	
t_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	nsec	C_L = 50 pf
t_{HRE}	Data Hold from $\overline{RE}$	0			nsec	



READ DATA TIMING

READ DATA TIMING WD2010-05WC = 5 MHz

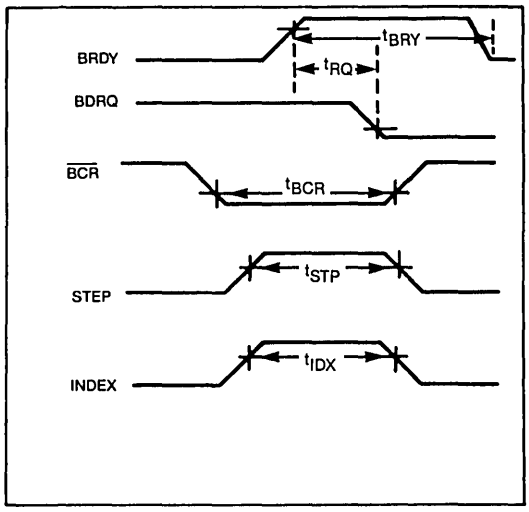
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{RCP}	RCLK Pulse Width	95		2000	nsec	50% Duty Cycle
t_{X1}	RD from RCLK Transition	0		t_{RCP}	nsec	
t_{X2}	RD to RCLK Transition	20		t_{RCP}	nsec	
t_{RD}	RD Pulse Width	40		t_{RCP}	nsec	
t_{DRN}	DRUN Pulse Width	30			nsec	
t_{RCF}	RCLK Frequency	.250	5	5.25	MHz	See Note 6



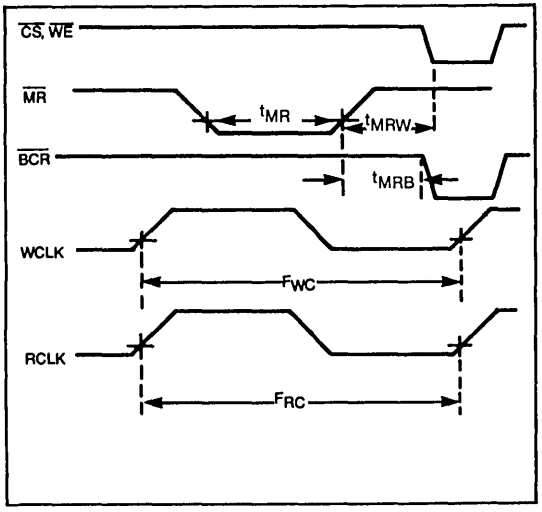
WRITE DATA TIMING

WRITE DATA TIMING WD2010-05WC = 5 MHz

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{WC}	WCLK Pulse Width	95		2000	nsec	50% Duty Cycle
t_{WD}	Propagation Delay WCLK to WD	10		65	nsec	
t_{WLE}	WCLK to Leading $\overline{\text{EARLY/LATE}}$	10		65	nsec	
t_{ELW}	WCLK to Trailing $\overline{\text{EARLY/LATE}}$	10		65	nsec	
t_{WCF}	WCLK Frequency	.250	5	5.25	MHz	See Note 6



MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING WD2010-05

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{RQ}	BDRQ Reset from BRDY	20		200	nsec	
t_{BCR}	$\overline{\text{Buffer}}$ $\overline{\text{Counter}}$ $\overline{\text{Reset}}$ Pulse Width	1.4	1.6	1.8	μsec	
t_{STP}	Step Pulse Width	1.4 7.8	1.6 8.0	8.2 8.2	μsec	See Note 2
t_{IDX}	Index Pulse Width	500			nsec	
t_{MR}	Master Reset Pulse	24			WC	See Note 3
t_{BRY}	BRDY Pulse Width	400			nsec	See Note 5
t_{MRB}	$\overline{\text{MR}}$ Trailing to $\overline{\text{BCR}}$	0	3.2	6.4	μsec	
t_{MRW}	$\overline{\text{MR}}$ Trailing to Host Write	6.4			μsec	

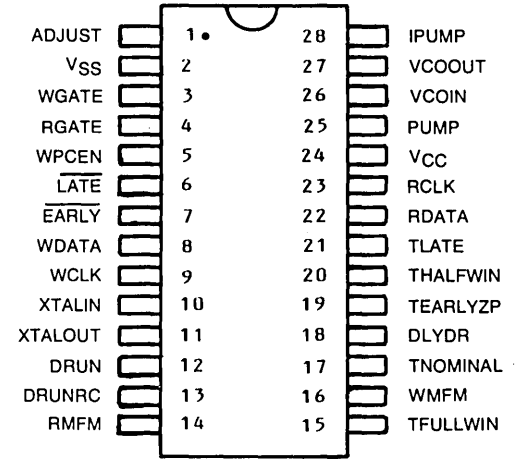
NOTES:

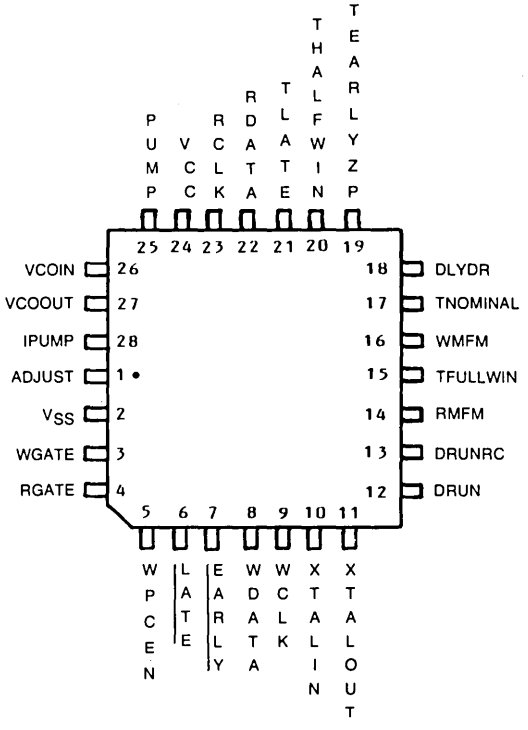
1. AC timing measured at V_{OH} = 2.0V, V_{OL} = 0.8V, C_L = 50 pf.
2. 1.6 μsec. is typical pulse for a step rate of 32 μsec/step. 8.0 μsec typical pulse for all other step rates. Last step pulse at 3.2 μsec/step rate up to 8.2 μsec.
3. 24 WCLK periods (4.8 μsec at 5.0 MHz)
4. 2 WCLK ± 100 ns.
5. The true to false transition of BRDY should not come sooner than 2 WCLK from true to false transition of BDRQ.
6. $t_{RCF} = t_{WCF} \pm 15\%$.
7. 2 WCLK ± 50 ns.
8. $\overline{\text{RE}}$ may precede $\overline{\text{CS}}$ if $\overline{\text{CS}}$ plus $\overline{\text{RE}}$ meets the t_{RE} width.
9. $\overline{\text{WE}}$ may precede $\overline{\text{CS}}$ if $\overline{\text{CS}}$ plus $\overline{\text{RE}}$ meets the t_{WE} width.
10. It may be desirable to connect a 1 K Ω pullup resistor to pins 21-23.

WD10C20-05 Self-Adjusting Data Separator

FEATURES

- PROCESSES ALL SENSITIVE READ/WRITE DATA SIGNALS
- CMOS TECHNOLOGY
- DESIGNED FOR ST506/ST412 AND WD1010/ WD2010 INTERFACE
- HIGHLY STABLE LC TYPE VOLTAGE CONTROLLED OSCILLATOR
- SELF ADJUSTING VCO COMPENSATES FOR COMPONENT, TEMPERATURE, VOLTAGE, AND AGING VARIATIONS
- FREQUENCY DETECTION ON CRYSTAL REFERENCE AND DATA SYNCHRONIZATION FIELD, ELIMINATES 180 DEGREE LOCK DUE TO DRIVE ASYMMETRY, AND ELIMINATES HARMONIC LOCK FROM WRITE SPLICES
- ZERO PHASE STARTUP PROVIDES FASTER, MORE PREDICATABLE LOCK ACQUISITION
- LOCKS TO CRYSTAL REFERENCE WHILE IDLE
- DUAL GAIN: HIGH FOR FASTER ACQUISITION
  LOW FOR MORE JITTER
  REJECTION WHILE TRACKING
- EXTERNAL PUMP CURRENT CONTROL
- AVAILABLE IN 28-PIN DIP OR QSM PACKAGE
- INTEGRATED CRYSTAL OSCILLATOR
- ACCOMMODATES OTHER DATA RATES THROUGH SELECTION OF EXTERNAL COMPONENTS





PIN DESIGNATION

DESCRIPTION

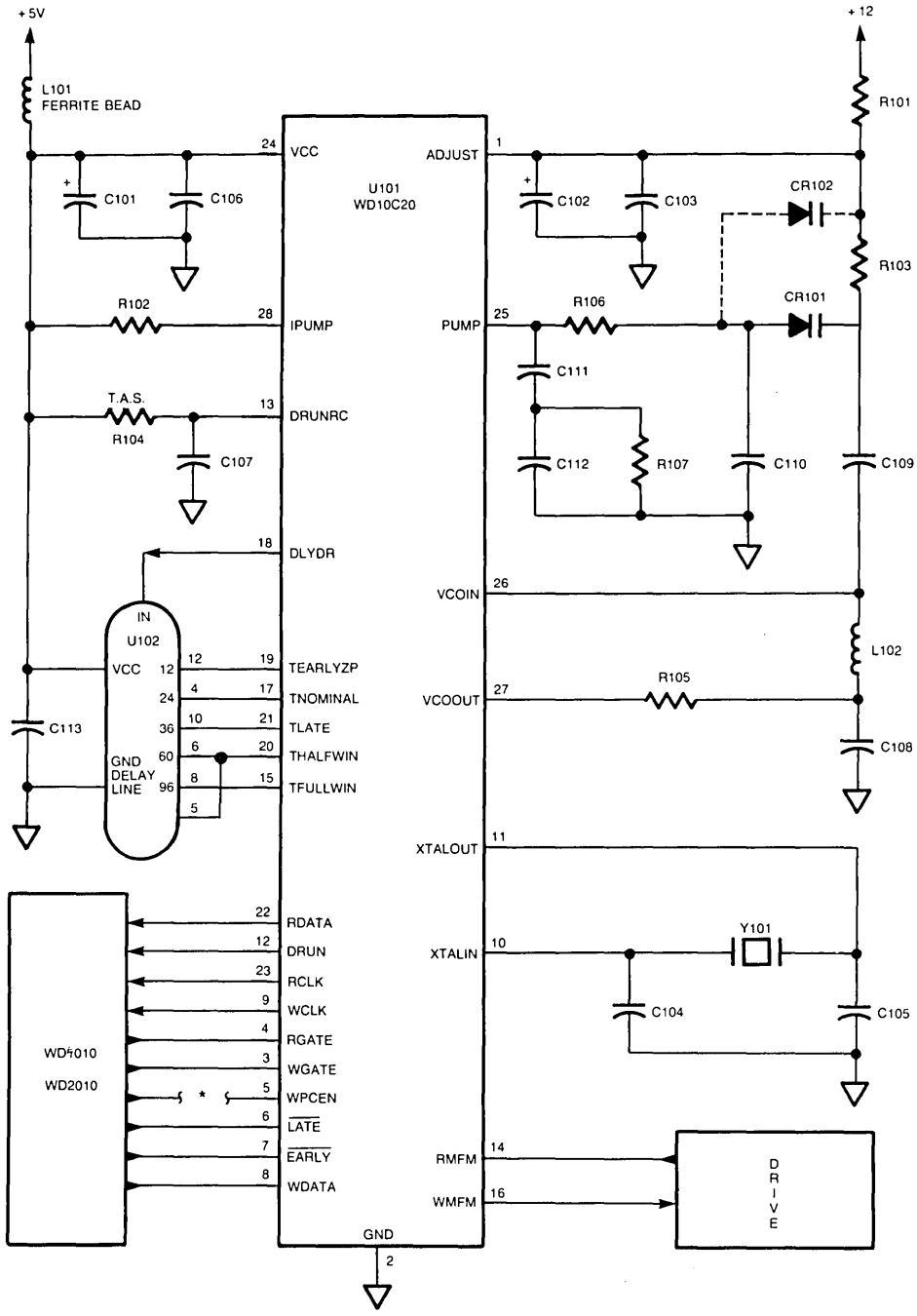
The WD10C20-05 is an LSI device implemented in 3 micron high-speed CMOS, designed to be compatible with the WD1010 and WD2010 Winchester Disk Controllers and ST506/ST412 disk drives. In a typical application, it handles all sensitive read/write signals between a WD1010/WD2010 and the data drivers/receivers. Read data corresponds to previous write data, with added phase, frequency, and write splice noise. The WD10C20-05 removes these sources of noise and presents a clean, digital read signal to the WD1010/WD2010.

While reading, the WD10C20-05 performs phase-locked loop data synchronization on data read from the drive. An on-board Sync Field detector automatically switches the PLL from the stable crystal reference to the read data. Zero-phase start-up results when the VCO is halted and restarted in phase with the data to eliminate initial acquisition in the wrong frequency direction. Frequency-phase detection is used at the beginning of the Sync Field to quickly and reliably acquire lock to the data. Use of this technique eliminates susceptibility to harmonics and asymmetry. The WD10C20-05 then switches to phase-only detection to complete the phase acquisition before the end of the Synch Field and to enable tracking of random MFM read data. When switching to phase detection, the WD10C20-05 reduces the error amplifier gain for better rejection of drive jitter. A precisely aligned detector samples the data at twice the underlying data rate to remove the phase jitter. The regenerated signal, along with a fixed-phase synchronous clock, are output to the WD1010/WD2010 digital circuits.

While writing, the WD10C20-05 conditions the write data to the drive. MFM data from the WD1010/WD2010 is precisely clocked, with a signal at twice the data frequency, to minimize digital phase noise. If precompensation is enabled, early, nominal, and late taps on an external delay line are multiplexed through matched delay paths to produce synchronized, precompensated write data, which is sent directly to the drive's write circuits.

The WD10C20-05 is designed to work at the 5 Mbit/sec data rate of the ST506/ST412 interface. Other data rates may be accommodated through the proper selection of external components.

NOTE: To assure reliable operation of the WD10C20-05, it is recommended that the WD10C20-05 KIT, number 77-000014 be used. If the user elects to not use the kit, the external components as shown in Figure 1, must be selected from the parts listed in the WD10C20-05 Application Note. The placement of these components must conform to the layout illustrated in the Application Note. (The Application Note is available through your Western Digital field representative.)



*RWC CONNNECTS TO WPCEN IF REDUCED WRITE CURRENT IS TO START AT THE SAME TIME AS WRITE PRECOMP. THE WD1002S-WX2 USES LS/DIR/WPC.

FIGURE 1. EXTERNAL COMPONENTS

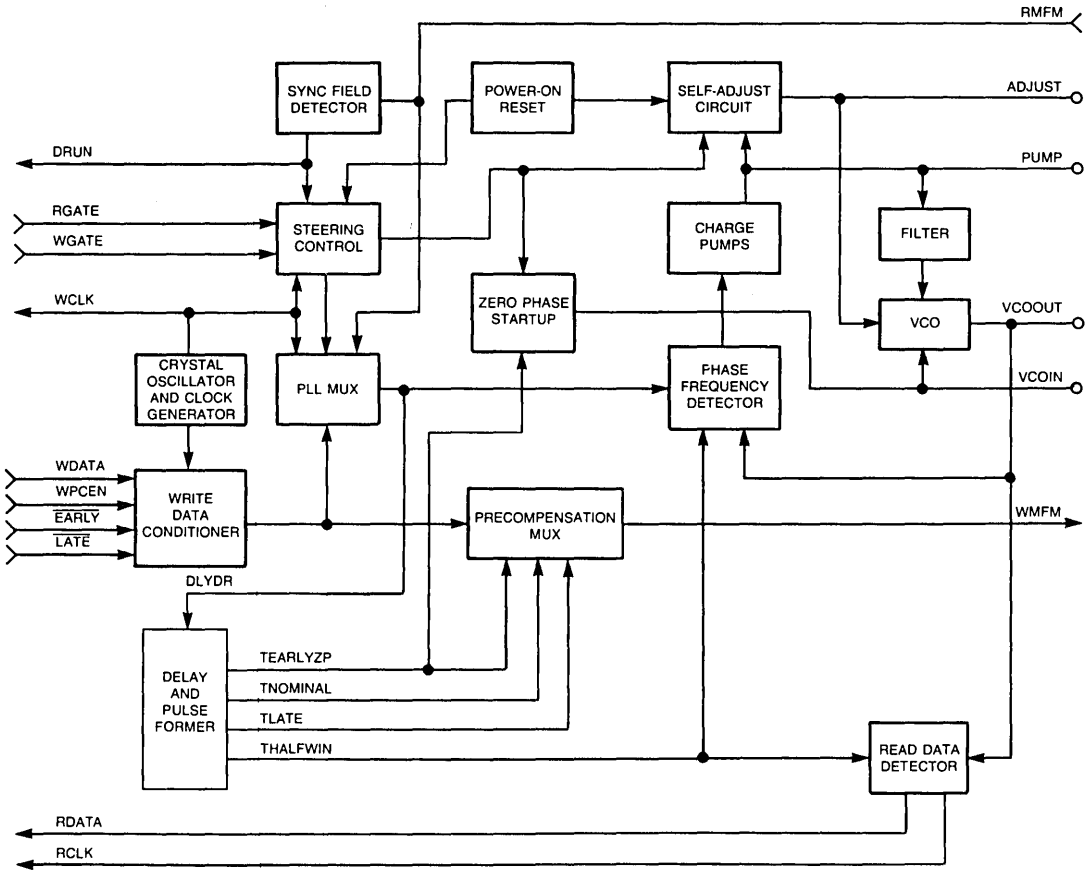


FIGURE 2. WD10C20 BLOCK DIAGRAM

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	ADJUST	ADJUST	O	Provides self calibration of the PLL.
2	VSS	GROUND		
3	WGATE	WRITE GATE	I	WGATE is asserted when the controller writes on the disk.
4	RGATE	READ GATE	I	RGATE is asserted when the controller intends to read from the disk. RGATE causes the WD10C20-05 to remain locked onto the incoming data stream.
5	WPCEN	WRITE PRECOMP ENABLE	I	WPCEN is asserted to enable the $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ signals from the controller. WPCEN may be connected to the Reduce Write Current (RWC) available from the WD1010/WD2010 if Write Precomp is to occur at the same time as the Reduced Write Current, or to an independent source if they start at different times.
6	$\overline{\text{LATE}}$	$\overline{\text{LATE}}$	I	Asserted by the Controller to delay the writing of a bit to the disk.
7	$\overline{\text{EARLY}}$	$\overline{\text{EARLY}}$	I	Asserted by the Controller to advance the writing of a bit to the disk.
8	WDATA	WRITE DATA	I	Non-Synchronized and Non-Precompensated MFM data from the controller to be written on the disk via WMFM.
9	WCLK	WRITE CLOCK	O	WCLK is equal to XTALIN ÷ 2 and is used by the controller to generate the data to be written.
10	XTALIN	XTALIN	I	XTALIN is a crystal controlled oscillator input used by a number of internal control functions. Divided by 2 it develops WCLK. XTALIN may also be driven by an external driver in which case XTALOUT is left open. The input level of this pin is not TTL and must be guaranteed by the clock source.
11	XTALOUT	XTALOUT	O	XTALOUT is the crystal controlled oscillator output. When an external frequency source is used, this pin is left open.
12	DRUN	DATA RUN	O	DRUN is a signal that discriminates between frequencies on RMFM. It goes low for low frequencies and high for high frequencies. Its nominal threshold is set to 1-3/8 bit times using DRUNRC. DRUN remains asserted for a continuous stream of one's or zero's. ie: Sync Field.
13	DRUNRC	DRUNRC	I	Connected to an external RC circuit for the generation of DRUN.
14	RMFM	READ MFM DATA	I	MFM Data received from the drive. A nominal 4K ohm internal pullup resistor allows tri-state multiplexing of the driver's data receivers.
15	TFULLWIN	TFULLWINDOW	I	Delay line tap for generating full window RMFM pulses.
16	WMFM	WRITE MFM DATA	O	Preconditioned WDATA ready to be written on the disk. WMFM is held low when WGATE is low.
17	TNOMINAL	TNOMINAL	I	Delay line tap for uncompensated write data.

PIN DESCRIPTION (Continued)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
18	DYLDR	DELAY LINE DRIVER	O	Drives an external delay line.
19	TEARLYZP	TEARLY ZERO PHASE TIMING	I	Delay line tap for early precompensated write data and for zero phase startup of the VCO.
20	THALFWIN	THALFWINDOW	I	Delay line tap for generating the enable phase delay when in phase detection mode.
21	TLATE	TLATE	I	Delay line tap for late precompensated write data.
22	RDATA	READ DATA	O	RDATA is RMFM synchronized to RCLK. The clock is removed from the RMFM by the controller.
23	RCLK	READ CLOCK	O	RCLK is equal to one half of VCO and is synchronized to RDATA during a read operation and to WCLK while in an idle state.
24	VCC	POWER SUPPLY	I	+5V Power Supply.
25	PUMP	PUMP	I/O	Charge PUMP to the PLL filter. Also a voltage input to the self-adjust sensing circuitry.
26	VCOIN	VOLTAGE CONTROL OSCILLATOR INPUT	I	Input to the VCO gain stage. VCOIN is clamped low, and then released during zero phase startup.
27	VCOOUT	VOLTAGE CONTROL OSCILLATOR OUTPUT	O	Output from the VCO gain stage.
28	IPUMP	IPUMP	I	An external resistor connected to IPUMP establishes the magnitude of the charge pump current and ADJUST current.

ARCHITECTURE

The WD10C20-05, with the necessay external components, provides the data interface between the WD1010 or WD2010 and an ST506/ST412 compatible drive. There are eight major functional sections within the WD10C20-05:

- Synchronized Field Detector
- Steering Control
- Phase-locked Loop (PLL)
  - Phase-frequency Detector
  - Charge Pumps
  - Filter
  - Voltage Controller Oscillator (VCO)
  - Zero Phase Startup Circuit
  - Self Adjustment Circuit
- Read Data Detector
- Crystal Oscillator
- Write Data Conditioner
- Delay And Pulse Former
- Power-on Reset

SYNCHRONIZATION FIELD DETECTOR

The Synchronization Field Detector discriminates between the 00's of a Synchronization Field and the low frequency data immediately preceding these fields. The criterion used is pulse period discrimination on the RMFM data. The external resistor and capacitor connected to DRUNRC sets the nominal detection threshold of 1-3/8 bit times. DRUN goes low for long periods and high for short periods.

STEERING CONTROL

This logic controls the sequencing of events when the WD10C20-05 is switching between read, write and idle modes. When switching, the Steering Control disables the Phase-Frequency Detector and Charge Pumps, switches the MUX source, invokes zero-phase startup, selects the velocity lock mode of the Phase-Frequency Detector, and high gain on the Charge Pump. After the zero-phase startup is complete, the Phase-Frequency Detector and Charge pumps are enabled. If the device is in read or write mode, after four byte times the Steering Control switches to phase detection, and the charge pumps are set to low gain.

PHASE-LOCKED LOOP

Phase-Frequency Detector

The Phase-Frequency Detector operates in one of two modes: velocity lock mode or phase-only detection.

Velocity lock mode is used for acquisition when the PLL is switched to read or write data or when the PLL is following the reference crystal oscillator.

The Steering Control logic switches to the Phase-only mode when frequency and phase acquisition is nearly complete. Internal delay paths have been carefully matched to minimize introduction of a phase error due to switching. The phase-only mode must be used to lock to the MFM following the Sync Field, since that contains the three MFM frequencies.

In either mode, the Phase-Frequency detector converts a phase difference between the VCO and the input to a pulse width equal to the phase difference. The polarity of the phase error determines whether a signal is directed to the pump up or pump down circuitry in the Charge Pump section.

Charge Pumps

The Charge Pump circuit converts the widths received from the Phase-Frequency Detector to proportional amounts of charge, into or out of the filter. The gain of the Charge Pumps is set by the input current of the IPUMP signal. This current is set by an external resistor connected to the VCC.

Filter

The Filter converts the current pulses from the Charge Pumps to a voltage ouptut to the VCO. It also peforms the sample-and-hold function necessary for an edge locked PLL, and is also necessary during the zero phase startup period. As shown in Figure 1, one of the filter's capacitors (C110) is also part of the VCO's series resonant oscillator.

The filter must meet the specific requirements of acquisition time, capture range, and jitter ejection, and within the context of its effect on VCO operation. The filter functions to block high frequency signals due to RMFM read data jitter, and passes the low frequency signals of the RMFM.

Voltage Controlled Oscillator

The VCO is a series resonant LC oscillator. The active gain element that provides the energy to sustain oscillation is within the WD10C20-05, between the VCOIN and VCOOUT pins. An inexpensive varactor controls and tunes the VCO. The filter connects to the anode of the varactor and provides the voltage for loop operation of the PLL. Higher voltages at the VCO input correspond to lower frequencies, and lower voltages correspond to higher frequencies. The self-adjustment circuit connects to the cathode of the varactor. The voltage bias at this point determines the location of the VCO's V-F characteristic curve, and is set for a favorable VCO input voltage at the nominal frequency of the VCO.

Zero Phase Startup Circuit

The VCOIN connects to the Zero Phase Startup Circuit, which contains the logic necessary to turn a clamp on or off. This clamp, in turn, enables or disables the VCO gain stage. When the WD10C20-05 changes the PLL input signal, the clamp is turned on for a minimum of one input data period. This stops the VCO gain and removes the AC energy from the passive VCO components. The VCO is now in a known state, and the time between the release of the clamp and the time the first edge of the VCO reaches the Phase Frequency Detector can be predicted. This event is made to coincide with the arrival of a data pulse by the delay between TEARLYZP and THALFWIN.

Self Adjustment Circuit

The Self Adjustment Circuit (SAC) serves to slowly maintain the VCO's input voltage near the sense level. It performs compensation for component variations in much the same way as manual adjustments, as well as dynamic variations such as temperature, voltage and aging. Another advantage of this circuit is the heavy RC filtering of the + 12 volt supply. The SAC tunes the VCO so that its nominal output frequency of twice the data rate corresponds to an input voltage favorable to the Charge Pumps. This voltage is approximately half of the VCC, and centers the capture range. The PUMP signal connects to an internal comparator and senses the VCO input voltage to determine whether it is above or below the threshold voltage (VSENSE).

The comparator is sampled at a low frequency derived from the crystal. The output is used as the up / down control to a six-bit counter. At power-on, this counter is set to half scale. The least significant two bits are for noise immunity only. The most significant four bits connect to a digital-to-analog converter (DAC) that controls the current-sinking ability of the ADJUST signal. To convert the ADJUST signal current to a voltage, it is connected externally through a resistor to the + 12V. To filter the DAC steps and transients, the ADJUST is connected to two capacitors. A resistor from the ADJUST signal to the cathode of the VCO varactor completes the circuit. Refer to Figure 1.

READ DATA DETECTOR

The Read Data Detector produces RCLK and RDATA. RCLK is a square wave equal to one half of the VCO frequency. During data tracking, RCLK mirrors the slowly varying frequency of the RMFM. RDATA is a regenerated form of the RMFM, with the jitter removed and one-half bit-time pulse widths, and is exactly synchronous with RCLK. RCLK edges occur nominally in the center of RDATA to allow sufficient setup and hold time for the digital circuits in the WD1010 / WD2010 using these signals.

CRYSTAL OSCILLATOR

The Crystal Oscillator is designed to operate in the parallel resonant mode, with an external crystal and two capacitors. It generates the WCLK signal used externally. Internally, various divisions of it are used by the Write Data Conditioner, PLL, and SAC.

When an externally generated clock is desired, the crystal and capacitors are omitted. The XTALIN pin is connected to the clock source, and XTALOUT is left disconnected. The input levels of XTALIN are not TTL and must be guaranteed by the clock source.

WRITE DATA CONDITIONER

The Write Data Conditioner samples and precisely synchronizes WDATA, EARLY, and LATE on the leading and trailing edges of WCLK. When WGATE is asserted, the DLYDR signal is a direct derivative of WDATA and is connected to the input of the delay line. It returns to the WD10C20-05 via the TEARLYZP, TNOMINAL, and TLATE input signals. When WPCEN is de- asserted, WMFM follows the TNOMINAL signal. When WPCEN is asserted, the EARLY and LATE signals select the TEARLYZP and TLATE inputs, respectively. The differential delay between TEARLYZP and TNOMINAL at the delay line defines the amount of early precompensation, and similarly, the differential delay between TNOMINAL to TLATE defines the amount of late precompensation.

When WGATE is asserted, one of the initial MFM pulses is suppressed to create an interval of two bit times. This ensures that DRUN will go low at the beginning of a Sync Field preceding a data field, so that zero phase startup and velocity lock are executed properly. When WGATE is de-asserted. WMFM is held low.

DELAY AND PULSE FORMER

The Delay And Pulse Former includes the external delay line as well as logic internal to the WD10C20-05. In response to rising edges, it produces positive pulses slightly longer than one detection window, which is half of one bit time. The taps are also used for write precompensation, zero-phase startup, and defining the enable window for phase detection. Depending on the mode of operation, its input is either RMFM, synchronized WDATA, or WCLK.

POWER-ON RESET

This integrated function is used to reliably set flip-flops to a predictable state during the application of the VCC. It is used by the Steering Control and SAC sections.

DATA SEPARATOR CIRCUIT PERFORMANCE SPECIFICATIONS

The following specifications apply when the external components are selected as specified and operate within the following ranges:

$V_{CC} = +5V \pm .25V$ with $\leq$ 100 mV ripple, 0 to 30 KHz
$+12V = +12V \pm 1.2V$ with $\leq$ 200 mV ripple, 0 to 30 KHz
Temperature = 0° to 70°C (32° to 158°F)

PHASE-LOCKED LOOP:

• Acquisition Time	< 12.8 usec (16 usec from DRUN high)	
• Capture Range	> ± 2.2% (± 1% drive ± .1% crystal Osc.)	
• Jitter Rejection	>40 db at 2.5 MHz	
• Damping Factor	min .7 typ. 1 max 1.4	Velocity Lock
	min .5 typ. .7 max 1.1	Phase Detection
• KD Error Amplifier Gain	min 2 mA	Velocity Lock Operating Range VSENSE ± 1060 mv
	typ 6 mA	
	max 10 mA	
	min 1 mA	Phase Detection Operating Range VSENSE ± 950 mV
	typ 4.3 mA	
	max 6.8 mA	
• Error Amplifier Balance Ratio	max 2:1	Phase Detection Operating Range VSENSE ± 950 mV Phase: ± 5 to ± 40 nsec
• Ko VCO Gain	min 4.5% per volt	
	typ 5% per volt	
	max 7.5% per volt	

FREQUENCY DETECTOR

DRUN must be high in response to RMFM rising edge to rising edge periods less than 250 nsec. DRUN must be low for periods greater than 300 nsec.

CRYSTAL OSCILLATOR

The operational frequency must be within ± .1% of 10 MHz.

PHASE DETECTOR/CHARGE PUMPS

Phase Decision Points

While in the phase detection mode, the phase difference from null (zero pump current) to the decision points must be no less than ± 40 nsec.

VCO GAIN

Over the VCO input voltage range, VSENSE nominal ± 1060 mV, the VCO gain must be within the range of 4.5% to 7.5% per volt. There must be no interruptions in its characteristic V-F curve over the input voltage range.

WD10C20-05 ELECTRICAL CHARCTERISTICS

MAXIMUM RATINGS

V_{CC} with respect to V_{SS} ..... +5.5 Volts
Max Voltage range on any pin ..... -0.5V to 0.5V > V_{CC}
(except ADJUST) with respect to V_{SS}
Max Voltage Range on ADJUST with respect to V_{SS} ..... -0.5V to +13.2V
Operating Temperature ..... 0°C(32°F) to 70°C(158°F)
Storage Temperature ..... -65°C(-85°F) to 150°C(302°F)

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics

DC OPERATING CHARACTERISTICS
T_A = 0°C (32°F) to 70°C (158°F)
V_{CC} = +5V ±.25V

Input signals:
TEARLYZP, TNOMINAL, TLATE, THALFWIN, TFULLWIN, RGATE, WGATE, WPCEN, WDATA, $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$, RMFM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_{IH}	Voltage Input High	3.0			V	
V_{IL}	Voltage Input Low			.8	V	

Input signals:
TEARLYZP, TNOMINAL, TLATE, THALFWIN, TFULLWIN, RGATE, WGATE, XTALIN, VCOIN (Clamp off)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
I_{IN}	Input leakage			±10	μA	V_{IN} = GND to V_{CC}

Input signals: WDATA, $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
I_{IH}	Current Input High			+10	μA	V_{IH} = 3.4 V*
I_{IL}	Current Input Low			-4	mA	V_{IL} = .45 V*

Input signal: WPCEN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
I_{IH}	Current Input High			+10	μA	V_{IH} = 3.4 V*
I_{IL}	Current Input Low			-2	mA	V_{IL} = .4 V*

*These inputs may or may not have an internal pullup resistor.
In either case, if I_{IH} and I_{IL} meet these specs, the inputs will be driven correctly.

Input signal: RMFM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
I_{IH}	Current Input High			0	mA	V_{IH} = 3.4 V
I_{IL}	Current Input Low			−2.5	mA	V_{IL} = .4 V Internal pullup resistor

Input signal: XTALIN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_{IH}	Voltage Input High	3.6			V	
V_{IL}	Voltage Input Low			.6	V	

Output signals: WCLK**, WMFM, DLYDR

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_{OH}	Voltage Output High	2.4			V	I_{OH} = −1 mA
V_{OL}	Voltage Output Low			.4	V	I_{OL} = 4 mA
T_{RISE}	Rise Time .8 to 2.0 V			10	nsec	CL = 30 pf
T_{FALL}	Fall Time 2.0 to .8 V			10	nsec	CL = 30 pf

Output signal: WCLK**

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_{OH}	Voltage Output High	4.6			V	I_{OH} = −100 μA
V_{OL}	Voltage Output Low			.2	V	I_{OL} = 1 mA
T_{RISE}	Rise Time .9 to 4.2 V			30	nsec	CL = 30 pf
T_{FALL}	Fall Time 4.2 to .9 V			30	nsec	CL = 30 pf

**WCLK has two requirements. It must be able to drive special WD1010 / WD2010 inputs, as well as a buffer at TTL levels. In any application, the total capacitance of the WD1010 / WD2010, buffer, and PC board, must not be more than 30 pf. The total input current of the WD1010 / WD2010 and buffer at the different input voltages must not exceed the above specification.

Output signals: RCLK, RDATA, DRUN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_{OH}	Voltage Output High	4.65			V	I_{OH} = −20 μA
V_{OL}	Voltage Output Low			.2	V	I_{OL} = 20 μA
T_{RISE}	Rise Time .9 to 4.2 V			30	nsec	CL = 20 pf
T_{FALL}	Fall Time 4.2 to .9 V			30	nsec	CL = 20 pf

Self Adjust, Pump, and Power

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_S	VSENSE Threshold		2.4		V	
I_A	ACQUISITION PUMP Current		±6		mA	3.57K on IPUMP***
I_T	TRACKING PUMP Current		±4.5		mA	3.57K on IPUMP***
I_{JMX}	ADJUST Max Current	.4	.6	1.0	mA	3.57K on IPUMP***
I_{JMN}	ADJUST Min Current			±10	μA	
I_{CC}	Power Supply Current		40		mA	3.57K on IPUMP, 5MHz

***Depending upon the application, there are specific requirements upon the pump currents and their relationship to VSENSE. This document is written for 5 Mbit/sec, WD1010/WD2010, ST506/ST412 drive.

AC OPERATING CHARACTERISTICS

Timing on signals RDATA, RCLK, WCLK, and DRUN are measured at the voltage halfway between the WD1010/WD2010's VIH and VIL: 2.55 Volts. All other signals are measured from the I.4 volt transition. All timing is measured with the load capacitance, CL = 50 pf.

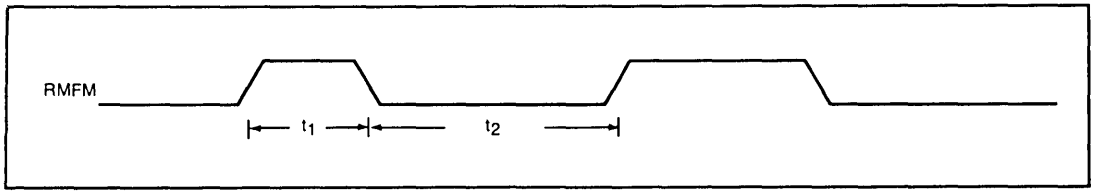


FIGURE 3. DISK DRIVE READ DATA, PULSE FORMING

TABLE 1. DISK DRIVE READ DATA, PULSE FORMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_1	RMFM Pulse Width High	20		150	nsec	
t_2	RMFM Pulse Width Low	25			nsec	

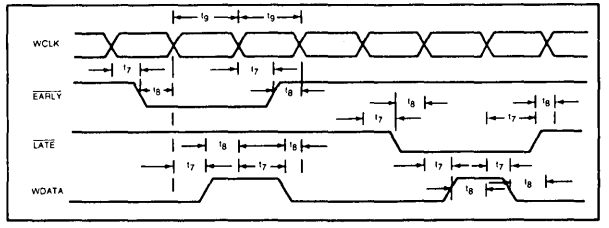


FIGURE 4. WRITE SETUP/OLD

TABLE 2. WRITE SETUP/HOLD

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_7	Hold Time	5			nsec	
t_8	Setup Time	20			nsec	
t_9	WCLK Pulse Width	95		105	nsec	

Setup and Hold time is independent of the application of the WD10C20-05.

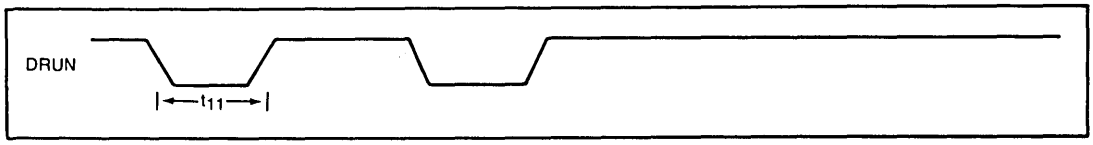


FIGURE 5. DRUN

TABLE 3. DRUN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{11}	DRUN Low Pulse Width	30			nsec	*

*No requirement on DRUN pulse width high.

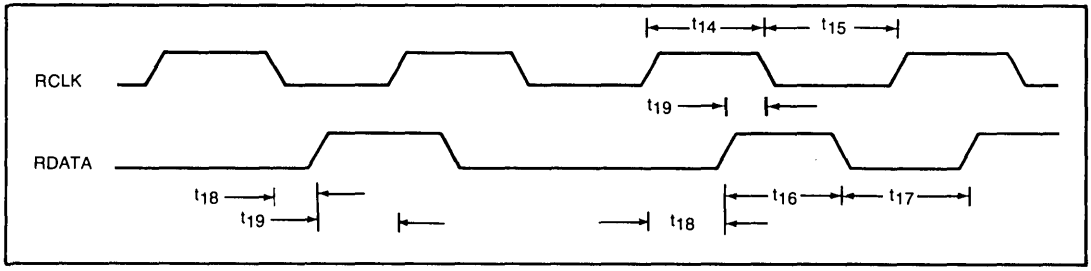


FIGURE 6. RCLK, RDATA TIMING

TABLE 4. RCLK, RDATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{14}	RCLK High Pulse Width	93		108	nsec	
t_{15}	RCLK Low Pulse Width	93		108	nsec	
t_{16}	RDATA High Pulse Width	93		108	nsec	
t_{17}	RDATA Low Pulse Width	93		108	nsec	
t_{18}	RCLK Edge to RDATA Rising Edge	30			nsec	Max is implicit in t_{19}min
t_{19}	RDATA Rising Edge To RCLK Edge	30			nsec	Max is implicit in t_{18}min

t_{14} and t_{15} each define an MFM detection window. The rising edge of RDATA must occur within the window. $t_{14} + t_{15}$ = the current bit cell time.

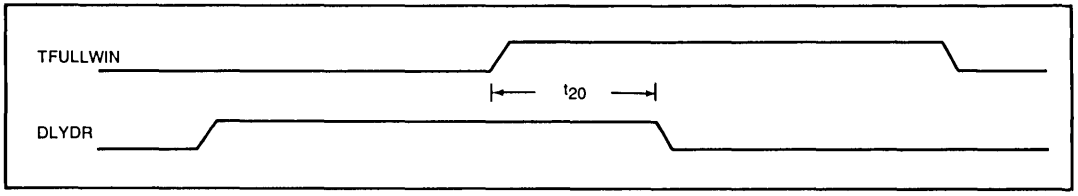
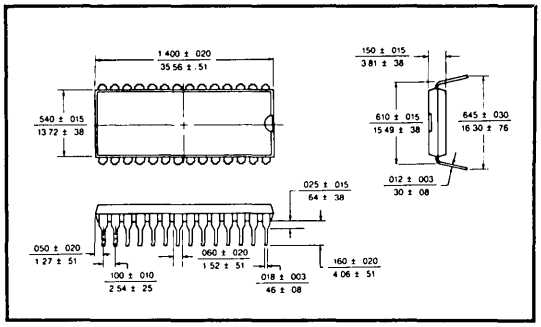


FIGURE 7. DLYDR, TFULLWIN TIMING

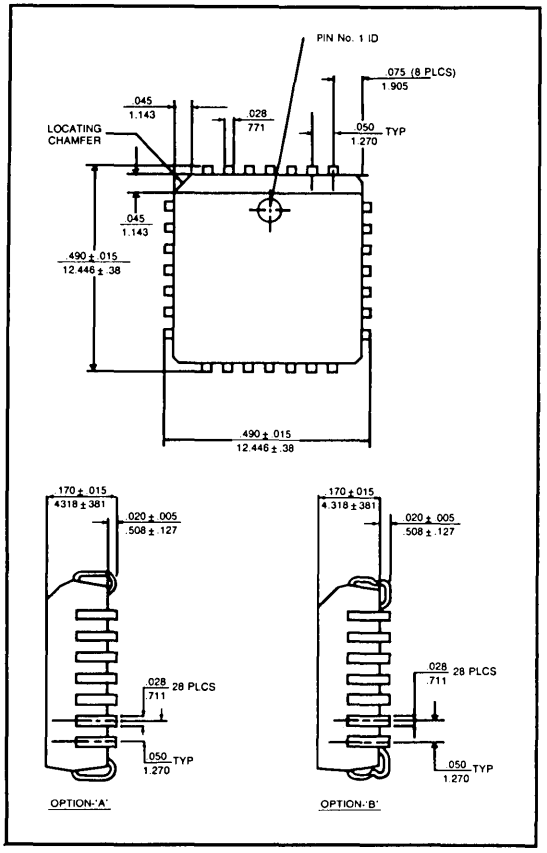
TABLE 5. DLYDR, TFULLWIN TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{20}	DLYDR Shutoff Time	12		36	nsec	

PACKAGE DIAGRAMS



28 LEAD PLASTIC PH

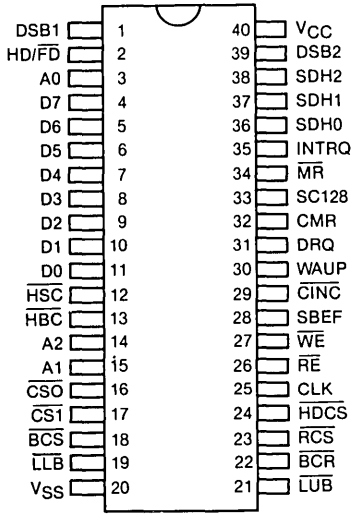


28 LEAD PLASTIC QUAD JH

WD1014 Error Detection/Support Logic Device

FEATURES

- 32-BIT ECC POLYNOMIAL
- BURST CORRECTION TO 11-BITS
- MULTIPLE ERROR BURST DETECTION
- DATA TRANSFER RATE OF 5-MBITS/SECOND
- PROCESSES CHECK/SYNDROME BITS IN 2-BIT SERIAL FASHION
- SECTOR SIZES = 128, 256, 512, & 1024 BYTE DATA FIELDS
- SUPPORT READ/WRITE SHORT/LONG FEATURES
- ON-CHIP STORAGE OF SYNDROME/CHECK BYTES
- 8-BIT I/O DATA BUS
- SOFTWARE ADDRESSABLE REGISTERS & LATCHES
- ON-CHIP LOGIC FOR EXTERNAL BUFFER CONTROL
- 40 PIN, DUAL-IN-LINE, N-MOS DEVICE
- TTL, MOS COMPATABILITY
- SINGLE SOURCE +5 VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1014 EDS logic chip provides the WD1002-05 Winchester Floppy Disk Controller (WFC) board with ECC and support logic. The EDS chip is a single chip device specifically designed to add error correction capabilities to a 5.25" and 8" Winchester disk drive. It also contains three 8-bit registers, three counters, and several latches that enhance the capability of the WFC on-board Control Processor (CP) chip WD1015 for control functions in real time operation. The EDS 40-pin device replaces approximately 35 standard TTL packages consisting of shift registers, flip-flops, and logic gates.

The ECC polynomial selected is the same as the one implemented in the WD1100-06 ECC/CRC logic except that the current design is a 2-bit serial implementation of the polynomial for faster operation. The ECC polynomial selected is a computer generated code optimized for sector sizes of 128, 256, 512, and 1024 byte data fields. The four ECC bytes appended by this chip enable corection of a single burst of up to 11 bits. It can also simultaneously detect a single burst of up to 20 bits and a double burst of up to 4 bits. The computer generated code has been selected over a comparable fire code since the fire codes suffer from pattern sensitivity problem.

The WD1014 EDS device is fabricated using N-channel silicone gate technology, and is available in a 40-pin, ceramic, dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	PIN NAME	FUNCTION
1	DSB1	DRIVE SELECT BIT 1	This output is encoded with DSB2 to select one of three Winchester Drives or one of four floppy drives depending upon the state of HD / $\overline{FD}$.
2	HD / $\overline{FD}$	HARD OR $\overline{\text{FLOPPY}}$ DISK SELECT	When high, hard disk drives are selected and when low, floppy disk drives are selected.
3	A0	ADDRESS BIT 0	This input along with $\overline{CS0}$ = 1 and $\overline{CS1}$ = 0 is used to address the WD 1014 registers.
4 Thru 11	D7 thru D0	DATA 7 thru DATA 0	8-bit bi-directional data bus. Data is output only when the check / syndrome register or the command register is read.
12	$\overline{HSC}$	$\overline{\text{HOST STATUS}}$ CONTROL	This output when low, enables the WFC status onto the data lines making them available to the Host processor, if WAUP = 0.
13	$\overline{HBC}$	$\overline{\text{HOST BUS CONTROL}}$	This output when low, enables the Host to communicate to the WFC and set up all task files, if WAUP = 0 and $\overline{HSC}$ = 1.
14	A2	ADDRESS BIT 2	These 2 inputs along with $\overline{CS0}$ = 1 and $\overline{CS1}$ = 0 are used to address the WD1014 registers.
15	A1	ADDRESS BIT 1	
16	$\overline{CS0}$	$\overline{\text{CHIP SELECT BIT 0}}$	$\overline{CS0}$ = 1 and $\overline{CS1}$ = 0 selects the WD1014, for other combinations see the chart under task files.
17	$\overline{CS1}$	$\overline{\text{CHIP SELECT BIT 1}}$	
18	$\overline{BCS}$	$\overline{\text{BUFFER CHIP SELECT}}$	This input line indicates that an external device wants to access the buffer. The ECC check / syndrome computation is also enabled at this time.
19	$\overline{LLB}$	$\overline{\text{LOAD LOWER BYTE}}$	The rising edge of this output line is used to load the lower byte of address into the external buffer counter.
20	V_{SS}	GROUND	Ground.
21	$\overline{LUB}$	$\overline{\text{LOAD UPPER BYTE}}$	The rising edge of this output line is used to load the upper byte of address into the external buffer counter.
22	$\overline{BCR}$	$\overline{\text{BUFFER COUNTER RESET}}$	This input indicates that an external device wants to reset the external buffer counters. The internal overflow counters are also cleared.
23	$\overline{RCS}$	$\overline{\text{RAM CHIP SELECT}}$	This output line is used to select external RAM when $\overline{BCS}$ is active low or when the CP or the Host is accessing the RAM. This output is disabled when SBEF = 1.
24	$\overline{HDCS}$	$\overline{\text{HARD DISK CHIP SELECT}}$	This output line is used to enable the WD1010 when the Host is accessing its task files except the Error, Status and Command registers.
25	CLK	CLOCK	The rising edge of CLK is used to shift the ECC polynomial and the falling edge is used to count exactly 4 shifts.
26	$\overline{RE}$	$\overline{\text{READ ENABLE}}$	Strobes used in conjunction with $\overline{CS0}$ = 1, $\overline{CS1}$ = 0, A2-A0 to access registers.
27	$\overline{WE}$	$\overline{\text{WRITE ENABLE}}$	
28	SBEF	SECTOR BUFFER EMPTY OR FULL	Output signal used to indicate the sector buffer has been filled or emptied.
29	$\overline{CINC}$	$\overline{\text{COUNTER INCREMENT}}$	The rising edge of this output signal increments an external address counter. This output is enabled only if the RAM is being accessed and SBEF = 0.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	PIN NAME	FUNCTION
30	WAUP	WAKEUP	This output signal is made active by the Host issuing a command and filling the sector buffer. It indicates that a command is being executed by the CP on the WFC board. The Host now cannot communicate with the WFC until the command has been completed. $\overline{MR}$ also sets WAUP.
31	DRQ	DATA REQUEST	The data request line is activated whenever the sector buffer contains data to be read by the Host, or is awaiting data to be loaded by the Host. This line is reset whenever the sector buffer has been filled or emptied.
32	CMR	COUNTER MASTER RESET	This output signal resets the external address counters whenever a $\overline{MR}$ or a command has been issued by the Host, or when $\overline{BCS}$ is asserted.
33	SC128	SECTOR COUNT OF 128 BYTES	This input signal is used in conjunction with the SDH register to indicate that the buffer has overflowed.
34	$\overline{MR}$	MASTER RESET	Used to initialize internal logic. All internal buffer overflow counters are reset, the DRQ and INTRQ flip-flops are cleared and BUSY is set.
35	INTRQ	INTERRUPT REQUEST	This output line is activated whenever a command has been completed. It is reset to the inactive state when the status register is read, or a new command is loaded via the DAL lines, or $\overline{MR}$ is asserted.
36 37 38	SDH2 SDH1 SDSH2	DRIVE SELECT, AND HEAD SELECT BITS	The 3 least significant bits of the internal SDH register are available as outputs. The SDH register is updated whenever the Host writes to it.
39	DSB2	DRIVE SELECT BIT 2	This output is encoded with DSB1 to select one of three Winchester Drives or one of four floppy drives depending upon the state of HD/$\overline{FD}$.
40	V_{CC}	POWER SUPPLY	+5V Power Source

TASK FILES

WAKE UP, $\overline{CS1}$, $\overline{CS0}$, A2-A0, $\overline{RE}$ and $\overline{WE}$ are used to select various registers as shown below:

WAKE UP	$\overline{CS1}$	$\overline{CS0}$	A2-A0	EFFECT
X	1	1	X	Idle – Nothing selected.
0	1	0	X	Host to WFC and WD1010 files.
1	1	0	X	CP to WD1010+ RAM access.
1	0	1	X	CP to WD1014.
X	0	0	X	Illegal condition.

A2	A1	A0	WD1014 REGISTERS		WD1010 REGISTERS	
			$\overline{RE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WE}$
0	0	0	0+CHECK/ SYN bytes*	0 + CHECK bytes*	RAM	RAM
0	0	1		Set ECC	Error Req.**	Write Precomp
0	1	0	SLEEP	0+LLB[2]	Sector Count	Sector Count
0	1	1	Clear OVF/CNTRS	0+LUB[2]	Sector Number	Sector Number
1	0	0		Set DRQ	Cylinder Low	Cylinder Low
1	0	1		Set Read Latch	Cylinder High	Cylinder High
1	1	0	Clear Mult Mode	Set Mult Mode	S.D.H.	S.D.H.
1	1	1	0+Command*	0+Error Reg.*	Status Reg.**	Command Reg.**

*Data bus contains valid information. Except as indicated in ** the Host and onboard CP(WD1015) can access the registers in the WD1010. The registers in the WD1014 can only be accessed by the WD1015. For the registers not referred to in *, the data bus need not contain valid information.

**The Host does not access these registers in the WD1010 (or WD2797). The content of these registers must be off loaded to an intermediate register for access by the Host.

COMMAND	BITS 7	6	5	4	3	2	1	0
READ	0	0	1	0	I	M	L	0
WRITE	0	0	1	1	0	M	L	0
FORMAT	0	1	0	1	0	0	0	0

COMMAND CODES

For the implementation of parts of the controls, the following command codes are pertinent:

The control logic only decodes bits 7-4 and uses bit 1 (long bit) in its internal logic. The rest of the command codes and bits are not used by the WD1014.

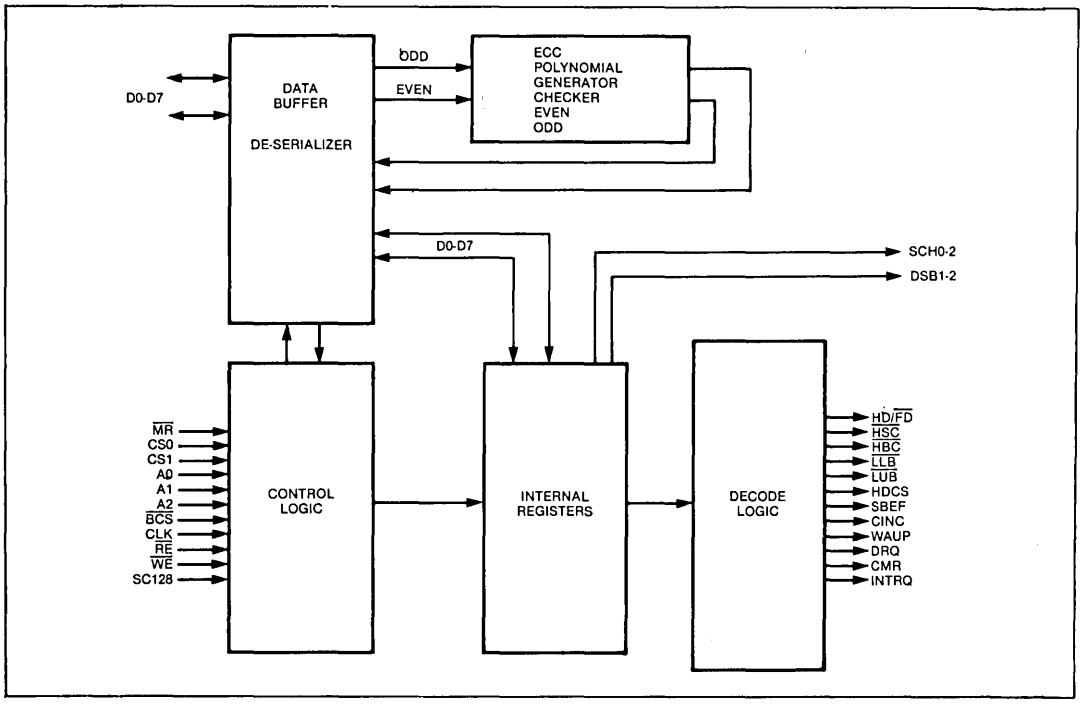
For a complete description of the commands or the task files refer to the WD1002-05 WFC data sheet.

WD1014 ARCHITECTURE

The WD1014 Chip was specifically designed for the WFC board to extend the capabilities of the Control Processor (WD1015) to handle real time functions. As designed, the WD1014 is not a stand alone general purpose device unless, of course, almost all of the protocol described can be used in any new designs.

The WD1014 consists of a 2 bit serial polynomial generator (that produces 4 bytes of check/syndrome) an 8 bit data buffer and deserializer, two 8 bit registers, namely a Command/Error register and a SDH register, and control logic consisting of 3 counters, 6 latches, and a host of combinatorial logic. The addressable registers and latches are accessed as shown in the block diagram below.

Each major functional block will be described essentially independent of one another. Some overlap and references to the WFC board are unavoidable and, in fact, they aid in presenting a clearer picture of the device.



WD1014 BLOCK DIAGRAM

THE ECC POLYNOMIAL GENERATOR

The 4 byte check / syndrome generator consists of two 16 bit shift registers each of which has 8 feedback terms implemented with XOR gates, and control gates for the feedback and data paths.

The leading two bytes of the data field are not recognized by the WD1014. Therefore, in order to maintain compatibility with the devices that do, the polynomial is preset to what would have been calculated if the AIF8 had been read.(B517894A)

ECC computations are made whenever the external sector buffer is being accessed. The data present on the system data bus is accepted by the input data buffer and processed along with the gated data from the last stages of the shift register strings. The direction of shift within the ECC polynomial is from the LS.B. to the M.S.B. After the last byte of data has been accessed from the sector buffer, the internal counter overflow register is set. This in turn sets a feedback inhibit register after the last byte has been processed by the ECC polynomial. At this point, the feedback terms are forced to zero and only the data path to the LS.B. is enabled. This feature is convenient to store the 4 check / syndrome bytes internally so that RLONG and WLONG commands can be supported without the use of an external buffer.

During a write operation, the input data stream is divided by the polynomial and the 32 bit remainder obtained after buffer overflow is used as the 4 check bytes. The 4 check bytes are gated out of the WD1014 even though $\overline{RCS}$ = 1 since the internal $\overline{RBCS}$ is still active. In a READ operation, the check bytes are recomputed and compared to the recorded check bytes to generate the 4 syndrome bytes. The syndrome bytes are stored internally in the shift registers until the CP is ready to use them. Otherwise, the non-zero syndrome is used by the software algorithm to compute the displacement and the error vector within the bad sector.

To support RLONG and WLONG (L = 1) features of the WD1002-05, shift register strings are used as storage elements. After the last byte of data, the Host can write or read the 4 additional bytes which serve as check bytes for the data transmitted to the buffer. In this mode the feedback terms and the outputs from M.S.B. of the shift registers are disabled so that only data is accepted and stored. This enables the user to alter the check bits / or data to verify the operation of the Error detection logic.

SDH REGISTER

This register can be written into by either the Host or WD1015. The bits are decoded as follows.

BIT	7	6 5	4 3	2 1 0
FUNCTION	CRC + ECC	SECTOR SIZE	DRIVE SELECT	HEAD/DRIVE SELECT

Bit 7 should be set to a 1 whenever a Winchester disk is selected "and" ECC is to be utilized. It must be set to 0 for floppy disks.

Bit 6-5 as shown below specify the sector size.

SDH6	SDH5	SECTOR SIZE IN BYTES
1	1	128
0	0	256
0	1	512
1	0	1024

The decoded bits are used in conjunction with a 3 bit counter which has SC128 as its clock. The falling edge of this input is used to set a counter overflow latch for sector sizes 256, 512 and 1024. The rising edge of this input sets counter overflow latch when the sector size is 128. The counter overflow is available on the output as SBEF and is used internally to set the buffer overflow latch and various other control logic as required by system operation. This counter and associated logic is cleared upon $\overline{MR}$, any new command, or can be directly cleared by CLROVF.

Bits 4-0 are used for drive and head selection and are decoded in the following manner.

Winchester
HD/$\overline{FD}$ = 1 = $\overline{SDH4} + \overline{SDH3} + \overline{SDH4}\cdot\overline{SDH3}$
DSB1 = 1 = SDH3 decoded off chip for one of three
DSB2 = 1 = SDH4 drives.
SDH2-0 = SDH2-0 decoded off chip for one of eight heads.

Floppy
HD/$\overline{FD}$ = 0 = SDH4·SDH3
DSB1 = 1 = SDH1 decoded off chip for one of four
DSB2 = 1 = SDH2 drives.
SDH2-0 = Not used.
Side select is controlled by the WD1015 via the WD2797.

COMMAND/ERROR REGISTER

This 8 bit register intercepts and holds the command issued by the Host. When a command is issued:

(a) the sector counter and associated overflow latches are cleared.
(b) the external counters are cleared via CMR
(c) the read command latch is cleared
(d) INTRQ is reset
(e) bit 1 (the long bit) is used by the ECC polynomial to implement the READLONG and WRITELONG command. The CP can also read this latch so that it can execute the command.
(f) WAKEUP is set immediately if the command is a RESTORE, SEEK, or READ. For a WRITE or a FORMAT command, WAUP is set after counter overflow (COVF) occurs or an additional four RAM accesses have occured (SYN4), depending upon the long bit L = 0 or L = 1.

At the completion of a command, this register is reused to hold error information that can be read by the Host. This is necessary since error information from two sources has to be manipulated by the CP and reported to the Host in real time when requested to do so.

ERROR DETECTION LOGIC

The error detection logic consists of an input data buffer and deserializer, two 16-bit shift registers to generate the ECC bytes, and associated control logic consisting of two 3-bit counters and integrated logic.

INPUT DATA BUFFER AND DESERIALIZER

This section is designed to accept a byte of data on the rising edge of $\overline{RE}$ or $\overline{WE}$ under the following conditions:

1. The ECC polynomial is selected as implied by SDH7 = 1.
2. A valid $\overline{RBCS}$ is generated regardless of the counter overflow
3. If the syndrome is to be read by the C.P. after an overflow condition has occurred (i.e., the syndrome is not saved after it has been read by the C.P.).

Valid data presented to the WD1014 device is accepted by the data buffer and the ECC shift registers on the rising edge of $\overline{RE}$ or $\overline{WE}$ input strobes. These strobes are synchronized internally by the falling edge of the input clock so that shifting can begin on the rising edge of the clock. Data is serialized and shifted in a 2-bit parallel mode until the internal bit counter reaches the count of 3. This process is repeated for every byte of data until the counter overflow occurs plus an additional 4 bytes have been processed. Under the worst case conditions, a byte of data will be processed within 4 clock cycles after the $\overline{RE}$ or $\overline{WE}$ strobes are terminated.

MULTIPLEXER

The multiplexer is used to channel data to the I/O pins D7-D0 when one of the following conditions occur.

1. The command register is read
2. The error register is read
3. The check bytes are read
4. The syndrome bytes are read

The $\overline{RE}$ strobe gating with the above control signals is designed to keep the hold time on the output data bus to less than 100 n.s. and the data access time to be no more than 200 n.s.

WAKEUP

This signal alerts the external CP that a command has been received and is internally referred to as the busy signal.

WAUP will go high when $\overline{MR}$ is asserted or a command other than WRITE or FORMAT has been received. In the case of a WRITE or FORMAT command WAUP will go high when SBEF = 1 and L = 0, or when an additional four bytes have been accepted by the WD1014 when L = 1.

For proper operation, the READ command latch must be set by the CP whenever that command has been received. Also the Multiple Mode latch is set by the CP in order to execute the same command a multiple number of times. This latch must be reset if executing a READ or a WRITE command only once, or if the last sector of a multiple sector transfer is being processed.

WAKEUP can only be reset by asserting SLEEP.

DATA REQUEST

The true condition of the DRQ latch can oly be sampled by external circuitry if WAUP = 0.

This latch can be set by either the CP, or whenever a WRITE or FORMAT command is written into the WD1014. It is reset by COVF = 1 (SBEF) when L = 0, or until an additional 4 bytes have been accepted by the WD1014 when L = 1.

INTERRUPT REQUEST

Two latches are provided to handle interrupts. The programmed I/O interrupt (PINT) latch is set whenever an interrupt is desired at the start of data transmission to the Host. The DMA interrupt (DINT) latch is set whenever an interrupt is desired at the end of data transmission to the Host.

Both latches are reset when:

1. A $\overline{MR}$ occurs
2. Any command is received
3. The output signal $\overline{HCS}$ is activated.

As in the case of DRQ, the true condition of INTRQ can only be sampled by external circuitry if WAUP = 0.

MISCELLANEOUS CONTROL SIGNALS

The rest of the output signals are purely combinatorial in nature and are best described by Boolean expressions.

1. $\overline{HSC} = \overline{\overline{BUSY}.\overline{CSO}}.A2.A1.A0.\overline{RE}$
2. $\overline{HBC} = \overline{\overline{BUSY}.\overline{CSO}}.HSC$
3. $\overline{LUB} = \overline{CS1}.\overline{A2}.A1.A0.\overline{WE}$
4. $\overline{LLB} = \overline{CS1}.\overline{A2}.A1.\overline{A0}.\overline{WE}$
5. $\overline{RCS} = \overline{COVF}(\overline{CSO}.\overline{A2}.\overline{A1}.\overline{A0} + \overline{BCS})$
6. $\overline{HDCS} = (\overline{\overline{BUSY}}.A2.A1.A0. + \overline{\overline{BUSY}}..\overline{A2}.\overline{A1}.\overline{RE} + \overline{CSO})$

$\overline{HDCS}$ is active only if the Host is not accessing the error, status or the command registers of the WD1010 device, and $\overline{CSO}$ is asserted.

7. $\overline{CINC} = \overline{COVF}.\overline{RSC}(\overline{WE} + \overline{RE})$
8. CMR = $\overline{MR}$ + CST where CST = $\overline{\overline{BUSY}.\overline{CSO}}$ .A2.A1.A0.$\overline{WE}$(Any cmd written)
9. SBEF = COVF

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Ambient Temperatures
under bias . . . . . 0°C (32°F) to 70°C (158°F)

Voltage on any pin
with respect to V_{SS} . . . . . -0.2V to + 7.0V
Power dissipation . . . . . 1.5 Watt

STORAGE TEMPERATURE

Plastic . . . . . -55°C(-67°F) to + 125°C(257°F)
Ceramic . . . . . -55°C(-67°F) to + 150°C(302°F)

NOTE:

Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

TABLE 1. DC Electrical Characteristics T_A = 0°C (32°F) to 70°C (158°F), V_{CC} = +5V ±.25V, V_{SS} = 0V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
VIL	Input Low Voltage	-0.2		0.8	V	
VIH	Input High Voltage	2.0			V	
VOL	Output Low Voltage			.04	V	I_{OL} = 1.6 mA
VOH	Output High Voltage	2.4			V	I_{OH} = -100 mA
VCC	Supply Voltage	4.75	5.0	5.25	V	
ICC	Supply Current		200	250	mA	All outputs open

TIMING PARAMETERS

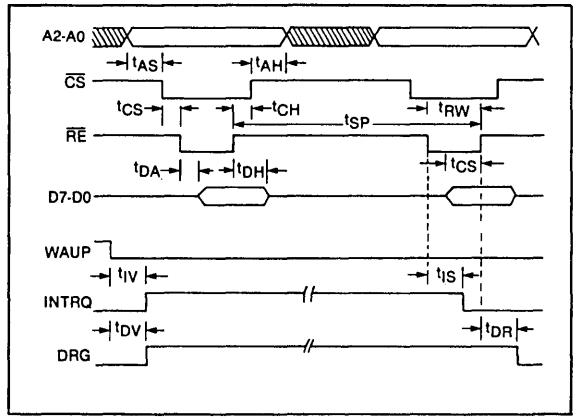


FIGURE 1. DATA READ CYCLE

TABLE 2. DATA READ CYCLE TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
f_{CP}	Input Clock Freq.		6.0	5.0	MHZ	
t_{AS}	Address Setup to $\overline{CS}$	100	70		nS	
t_{AH}	Address Hold from $\overline{CS}$	50	20		nS	
t_{CS}	Chip Selects Setup to $\overline{RE}$	100	70		nS	
t_{CH}	Chip Selects Hold from $\overline{RE}$	50	20		nS	
t_{RE}	$\overline{RE}$ pulsewidth	150	120		nS	
t_{SP}	$\overline{RE}$ Strobes period (rising edge)	4			CP	
t_{DA}	Data Access after $\overline{RE}$ active		100	150	nS	
t_{DH}	Data Hold after $\overline{RE}$ inactive		50	100	nS	reading
t_{DS}	Data Setup to $\overline{RE}$ inactive	50	10		nS	
t_{IV}	Interrupt Request valid		50 200	100 250	nS nS	Prog. I/O INT DMA INT
t_{IS}	INTRQ Reset		100	200	nS	
t_{DV}	Data Request Valid		50	100	nS	
t_{DR}	DRQ Reset		100	200	nS	

AC ELECTRICAL CHARACTERISTICS

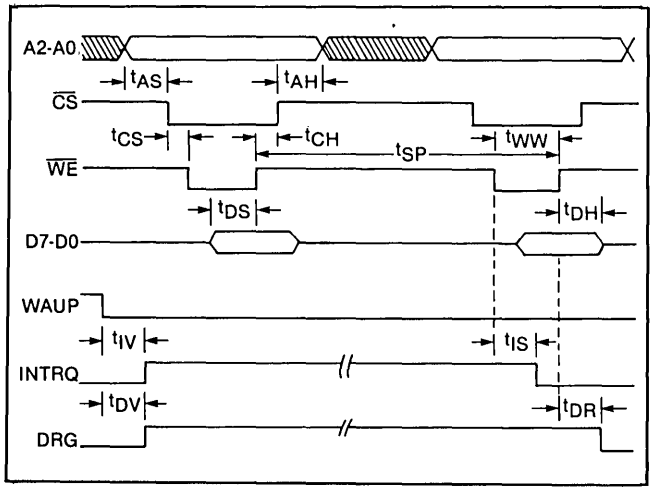


FIGURE 2. DATA WRITE CYCLE

TABLE 3. DATA WRITE CYCLE TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
f_{CP}	Input Clock Freq.		6.0	5.0	MHZ	
t_{AS}	Address Setup to $\overline{CS}$	100	70		nS	
t_{AH}	Address Hold from $\overline{CS}$	50	20		nS	
t_{CS}	Chip Selects Setup to $\overline{WE}$	100	70		nS	
t_{CH}	Chip Selects Hold from $\overline{WE}$	50	20		nS	
t_{WE}	$\overline{WE}$ pulsewidth	150	120		nS	
t_{SP}	$\overline{WE}$ Strobes period (rising edge)	4			CP	
t_{DHW}	Data Hold after $\overline{WE}$ inactive	0	30		nS	writing
t_{DS}	Data Setup to $\overline{WE}$ inactive	50	10		nS	
t_{IV}	Interrupt Request valid		50	100	nS	Prog. I/O INT
		50	200	250	nS	DMA INT
t_{IS}	INTRQ Reset		100	200	nS	
t_{DV}	Data Request Valid		50	100	nS	
t_{DR}	DRQ Reset		100	200	nS	

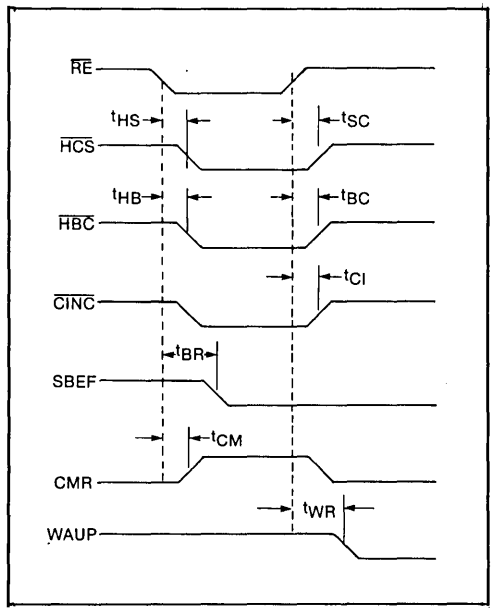


FIGURE 3. OUTPUT SIGNALS W.R.T. $\overline{RE}$

TABLE 4. OUTPUT SIGNAL (W.R.T.) $\overline{RE}$ TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{CI}	$\overline{RE}$ to Count Increm.		50	100	nS	rising edges
t_{HS}	$\overline{RE}$ to Status Strobe		130	200	nS	
t_{SC}	$\overline{RE}$ to $\overline{HSC}$ inactive		130	200	nS	
t_{HB}	$\overline{CS0}$ to Host bus str		70	200	nS	active if $\overline{HSC}$ off
t_{BC}	$\overline{CS0}$ to $\overline{HBC}$ inact.		80	200	nS	active if $\overline{HSC}$ off
t_{BR}	$\overline{RE}$ to cir SBEF		250	300	nS	using CLROVF strobe
t_{CM}	$\overline{RE}$ to counter reset		200	300	nS	using CLROVF strobe
t_{WR}	$\overline{RE}$ to WAUP reset		100	200	nS	using SLEEP strobe

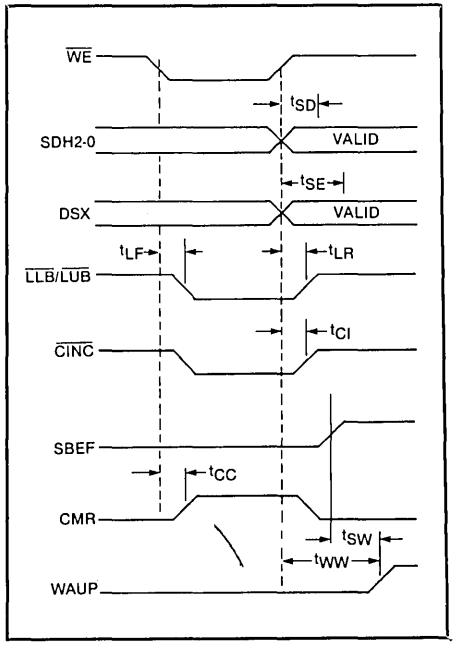


FIGURE 4. OUTPUT SIGNALS W.R.T. $\overline{WE}$

TABLE 5. OUTPUT SIGNAL (W.R.T.) $\overline{WE}$ TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{SD}	$\overline{WE}$ Inactive to SDHX output		150	200	nS	
t_{SE}	$\overline{WE}$ Inactive to DSX output		175	200	nS	
t_{LF}	$\overline{WE}$ to $\overline{LLB}/\overline{LUB}$		70	150	nS	falling edges
t_{LR}	$\overline{WE}$ to $\overline{LLB}/\overline{LUB}$		80	150	nS	rising edges
t_{CI}	$\overline{WE}$ to Count Increm.		50	100	nS	rising edges
t_{CC}	$\overline{WE}$ to Counter Reset		150	200	nS	
t_{SW}	SBEF to WAUP set		50	200	nS	
t_{WW}	$\overline{WE}$ to WAUP set		175	200	nS	Command written

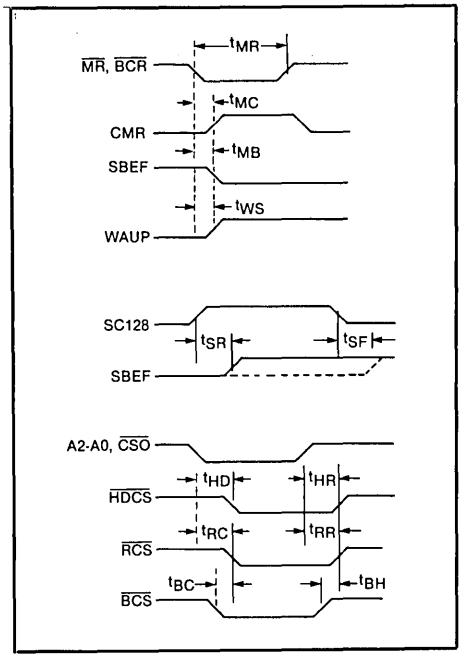


FIGURE 5. MISCELLANEOUS TIMINGS

TABLE 6. MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{MR}	Master reset/Buffer counter reset width	100	50		nS	
t_{MC}	$\overline{MR}/\overline{BCR}$ to counter reset		60	100	nS	
t_{MB}	$\overline{MR}/\overline{BCR}$ to SBEF rst		130	200	nS	
t_{WS}	$\overline{MR}$ to WAUP reset		100	200	nS	$\overline{BCR}$ has no effect
t_{SR}	Rising Edge of SC128 to SBEF		100	200	nS	128 byte sector
t_{SF}	Falling Edge of SC128 to SBEF		150	200	nS	all other sectors
t_{HD}	$\overline{CS0}$ to $\overline{HDCS}$		70	150	nS	(or address lines)
t_{HR}	$\overline{CS0}$ to $\overline{HDCS}$ rising to $\overline{CMR}$		80	150	nS	
t_{RC}	$\overline{CS0}$ to $\overline{RCS}$ active		90	150	nS	(or address lines)
t_{RR}	$\overline{CS0}$ to $\overline{RCS}$ high		100	150	nS	
t_{BC}	$\overline{BCS}$ to $\overline{RCS}$ active		50	100	nS	
t_{BH}	$\overline{BCS}$ to $\overline{RCS}$ high		60	100	nS	

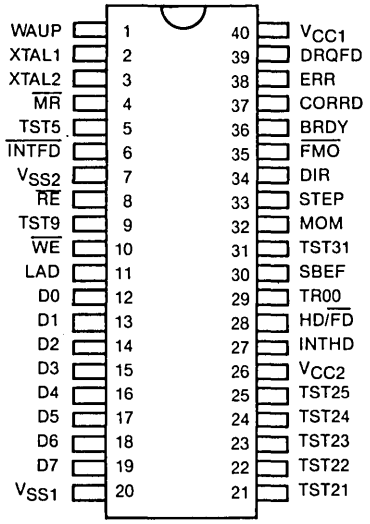
WD1015 Buffer Manager Control Processor

FEATURES

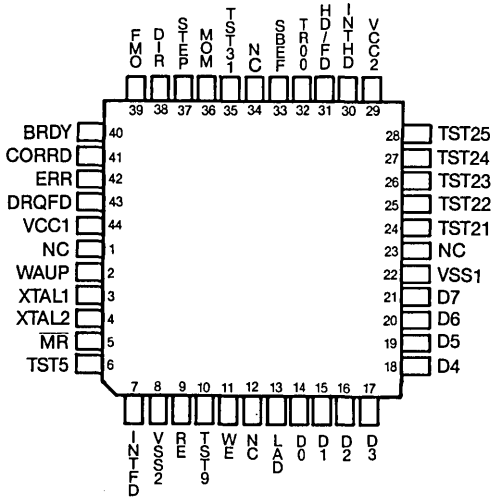
- SINGLE +5V POWER SUPPLY
- COMPLETE BUFFER MANAGER
- PROGRAMMABLE SECTOR SIZES - 128, 256, 512, or 1024 BYTES
- ECC BURST ERROR CORRECTION UP TO 5 BITS ON HARD DISK DATA
- 8-BIT MULTIPLEXED ADDRESS/DATA I/O BUS
- FLOPPY DISK COMMAND TRANSLATION
- SUPPORTS MOTOR ON OR HEAD LOAD DRIVES
- SUPPORTS 250 OR 500 KBS FLOPPIES
- BUFFERED SEEKS WITH FLOPPIES AND WINCHESTERS
- 16 POPULAR STEPPING RATES AVAILABLE
- AUTOMATIC RETRIES ON ALL ERRORS WITH SIMULATED COMPLETION
- POWER-ON DIAGNOSTICS INCLUDED
- 10 MHZ CLOCK RATE
- 40 PIN DIP PACKAGE
- 44 PIN QSM PACKAGE

DESCRIPTION

The WD1015 is a complete Control Processor (CP) that is used to handle all aspects of buffer management, in conjunction with the EDS (WD1014) device, for the Winchester/Floppy Controller board (WD1002-05). It executes all of the commands used by the WD1002-05 and does all of the control required except for real time processing, which is done by the WD1014. Throughout this specification this device will be referred to as the WD1015, or BMAC (buffer manager and controller), or simply as the CP (control processor). The WD1015 is programmed to control the transfer of information within the WFC and it maintains the necessary copies of the task files (TSF) found on both drives. Host access to the WFC causes the CP to access task file information in the TSF after a command is issued. Depending on the command, the CP will make the buffer accessible to the host or the WD1010 or 2797 controllers. The CP also controls the operation of the Error Correcting logic. During the transfer of data from the Host to the WD1010, the EDS monitors the data bus, if so enabled, to compute a 4 byte ECC which is appended to the data transferred to the WD1010 and recorded on the disk. During data transfers from the WD1010 to the host the CP uses the ECC to validate the data. If data is corrupted the CP envokes recovery techniques such as retries and correction. A maximum of 8 retries are attempted if two consecutive syndroms do not match. Correction is attempted only if two consecutive syndromes match. If the error is uncorrectable, the operation is terminated. The CP is also used to handle data transfers from or to the SF for the



PIN DESIGNATION



QSM DESIGNATION

floppy disk controller, which only uses CRC check bytes for its data fields. Two commands, RESTORE and SEEK, are directly executed by the CP rather than the WD2797 floppy disk controller. During status reads by the Host, the CP consolidates the normal completion status from the WD1010, the WD2797 and the current EDS status into a form consistant with established WD1010 error reporting. This consolidated status is then presented to the Host. The WD1015 is fabricated using HMOS technology and is available in a 40 pin DIP package and 44 pin QSM package.

PIN DESCRIPTION

PIN NUMBER	SIGNAL NAME	MNEMONIC	FUNCTION
1	WAKEUP	WAUP	This input is used by the BMAC to poll a command from the Host. The BUSY status bit is set immeditately execpt in case of a WRITE/FORMAT command. In that case, WAUP and BUSY, are set only after the sector buffer has been filled by the Host. WAUP is reset when the command has been executed.
2	CRYSTAL 1	XTAL1	One side of crystal input for internal oscillator. Also input for external source.
3	CRYSTAL 2	XTAL2	Other side of crystal/external source input. Frequency should be 10 MHz.
4	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	This input is used to initialize the internal logic of the processor.
5	TEST 5	TST5	This input is to be left open by the user. Internal pull-up 300K ohm.
6	$\overline{\text{FLOPPY DISK INTERRUPT}}$	$\overline{\text{INTFD}}$	Initiates an interrupt if interrupt is enabled; disabled on reset.
7	V_{SS2}	V_{SS2}	This input is to be left open by the user. Internal pull-up 10M ohm.
8	READ ENABALE	$\overline{\text{RE}}$	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
9	$\overline{\text{TEST 9}}$	$\overline{\text{TST9}}$	This output is left open by the user.
10	$\overline{\text{WRITE}}$	$\overline{\text{WE}}$	Output strobe during a BUS write. Used as write strobe to an external device. Signifies that valid data has been put on the BUS.
11	ADDRESS LATCH	LAD	This output signal occurs once during each instruction cycle. The negative edge of LAD strobes address into an external latch, used to communicate to the WD1010, WD2797, and the WD1014 chips.
12-19	DATA BUS	D7-D0	True I/O bi-directional BUS which can be written to or read synchronously using $\overline{\text{RE}}$, $\overline{\text{WE}}$, strobes. Also contains the address and data during an external access to or from port devices, under control of LAD, $\overline{\text{RE}}$, and $\overline{\text{WE}}$.
20	GROUND	V_{SS1}	Ground.
21-25	TEST 21-25	TST21-25	Unused pins to be left open by the user.
26	V_{CC2}	V_{CC2}	+5V during operation.
27	HARD DISK INTERRUPT	INTHD	This input is polled to sense an interrupt from the WD1010, indicating completion of command issued to it by the BMAC.
28	$\overline{\text{HARD DISK/FLOPPY DISK}}$	HD/$\overline{\text{FD}}$	This input is used to sense hard disk operation when high, and floppy disk operation when low.
29	TRACK 00	TR00	This input indicates that the R/$\overline{\text{W}}$ heads of the selected floppy drive are positioned over the outermost cylinder.
30	SECTOR BUFFER EMPTY/FULL	SBEF	This input to the BMAC is set high whenever a sector of data has been written to or read from the Sector Buffer.
31	TEST 31	TST31	Normally left open by the user.

PIN DESCRIPTION (cont.)

PIN NUMBER	SIGNAL NAME	MNEMONIC	FUNCTION
32	MOTOR MODE	MOM	Input used to select motor-on or head load timings for floppies. This line should be left open for motor-on type drives such as the mini floppies. A delay of 1 second will be observed before FMO is activated. For head load type drives like the standard floppies, this input should be grounded. A delay of 40 mS, will be observed before FMO is activated, thereby improving the overall performance when accessing the floppies.
33	STEP	STEP	The STEP output is pulsed once for each cylinder to be stepped on the floppies. The step pulse period is normally determined by the stepping rate selected. On a RESTORE for the floppies, however, a stepping rate of 8 mS, is used if the specified stepping rate is faster than 8 mS.
34	DIRECTION	DIR	This output is used by the floppy drive to determine the direction of a seek operation. A low defines direction as out and a high specifies direction as in.
35	$\overline{\text{FLOPPY MOTOR-ON}}$	$\overline{\text{FMO}}$	This output is used to turn the motor on, on all floppy drives supported by the WD1002 WFC board. The drives must be configured such that the heads are loaded when this signal is activated. When the floppies are being accessed for the first time, a delay as determined by MOM, is observed before activating FMO. Motor on is turned off after - 3 seconds, if no further floppy accesses are made.
36	BUFFER READY	BRDY	This output signal indicates the sector buffer is ready to be accessed by an external device such as the WD1010.
37	CORRECTED DATA	CORRD	This output status indicates to the Host that the BMAC has successfully corrected a data error in the data buffer, at least once. To determine if more than one correction has taken place during a multisector read, each sector specified must be reread by the Host on an individual basis.
38	ERROR	ERR	Output status bit indicates that the BMAC encountered an error during the execution of a command.The error reg, on the WFC board must be read by the Host to determine the type of error that occurred.
39	DATA REQUEST	DRQFD	This input indicates to the BMAC that the WD2797 has a byte of data available to be read from the disk, or requires a byte of data to be written to the floppy disk.
40	V_{CC1}	V_{CC1}	Main power supply. +5V ±5%

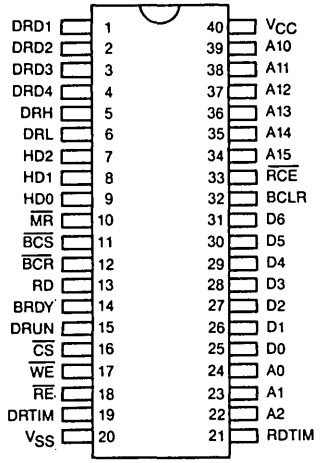
WD1100-21 Buffer Manager Support Device

FEATURES

- 6-BIT AUTO-INCREMENTING ADDRESS BUS
- 128, 256, 512, OR 1024 BYTES PER SECTOR DETECTOR
- SELECTS UP TO 4 DISK DRIVES
- SELECTS UP TO 8 HEADS PER DRIVE
- PROVIDES A RAM CHIP ENABLE AND READY SIGNAL
- TTL, MOS COMPATIBLE
- 40 PIN DIP PACKAGE
- NMOS TECHNOLOGY
- SINGLE + 5 VDC SUPPLY

DESCRIPTION

The WD1100-21 Buffer Manager Support Device is designed to interface up to four disk drives and eight heads per drive, to a WD1010-05 and Sector Buffer. The WD1100-21 accepts the SDH Register information (Sector Size, Drive, Head) and selects the appropriate drive and head. It receives the data from the disk and develops RD and DRUN (Read Data and Data Run) suitable for the WD1010-05. The WD1100-21 also selects the Sector Buffer and provides six of the address lines. The other four address lines must be implemented externally. The WD1100-21 signals BRDY (Buffer Ready) when the buffer counter reaches the value stored in the SDH Register.



PIN DESIGNATION

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	PIN NAME	I/O	FUNCTION
1	DRD1	READ DATA 1	I	This signal is data read from disk drive 1. It is shaped and placed on output pin 13.
2	DRD2	READ DATA 2	I	This signal is data read from disk drive 2. It is shaped and placed on output pin 13.
3	DRD3	READ DATA 3	I	This signal is data read from disk drive 3. It is shaped and placed on output pin 13.
4	DRD4	READ DATA 4	I	This signal is data read from disk drive 4. It is shaped and placed on output pin 13.
5	DRH	DRIVE SELECT HIGH	I	Most significant bit of the drive select number. Must be encoded externally.
6	DRL	DRIVE SELECT LOW	I	Least significant bit of drive select number. Must be encoded externally.
7	HD2	HEAD SELECT 2	I	Bit 2 of the head select number. Must be encoded externally.
8	HD1	HEAD SELECT 1	I	Bit 1 of the head select number. Must be encoded externally.
9	HD0	HEAD SELECT 0	I	Bit 0 of the head select number. Must be encoded externally.
10	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	Asserted, it initializes all internal logic including the SDH Register.
11	$\overline{BCS}$	$\overline{BUFFER\ CHIP\ SELECT}$	I	Asserted, this signal asserts RCE.
12	$\overline{BCR}$	$\overline{BUFFER\ COUNTER\ RESET}$	I	This signal resets the buffer address counter to zero making A10 thru A15 = 0.
13	RD	READ DATA	0	This is the MFM data read from the disk, shaped and made compatible with the WD1010-05.
14	BRDY	BUFFER READY	0	This signal is asserted when the buffer counter (A10 thru A15) has reached the sector size specified in the SDH Register, 128, 256, 512, or 1024.
15	DRUN	DATA RUN	0	This signal is asserted when a field of ones or zeroes has been detected.
16	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	Must be asserted to write into the SDH Register, increment the Buffer Address Counter, and assert RCE.
17	$\overline{WE}$	$\overline{READ\ ENABLE}$	I	Must be asserted to write into the SDH Register. WE or RE must be asserted to increment the Buffer Address Counter.
18	$\overline{RE}$	$\overline{READ\ ENABLE}$	I	$\overline{RE}$ or $\overline{WE}$ must be asserted to increment the Buffer Address Counter.
19	DRTIM	DRUN TIMING	I	An external load used to adjust DRUN to nominal pulse width of 250 nsec.
20	V_{SS}	GROUND	I	Ground.
21	RDTIM	RD TIMING	I	An external load for adjusting the pulse width of RD. 1K ohms creates approx. 90 nsec.
22 thru 24	A2 thru A0	ADDRESS 2 thru ADDRESS 0	I	A2 thru A0 are used to address the SDH Register (A2-A0 = 6) and increment the Buffer Address Counter (A2-A0 = 0).

PIN DESCRIPTION (Continued)

PIN NUMBER	MNEMONIC	PIN NAME	I/O	FUNCTION
25 thru 31	DO thru D6	DATA 0 thru DATA 6	I	7-Bit data bus used to write into the SDH Register.
32	BCLR	BUFFER CLEAR	O	Asserted, this signal indicates that the Buffer Address Counter has been cleared.
33	$\overline{RCE}$	$\overline{RAM\ CHIP\ ENABLE}$	O	Asserted by BCS, or CS and A0 thru A2 equal to zero. Used to enable access to the data buffer.
34 thru 39	A10 thru A15	BUFFER ADDRESS 10 thru 15	O	Buffer Address Counter. Used to address the Data Buffer.
40	V_{CC}	POWER SOURCE		+5V Power Supply

ARCHITECTURE

The WD1100-21 is composed of a 7-Bit SDH Register (the extension bit, bit 7 is not included), 11-Bit Sector Buffer Counter, and miscellaneous control signals. The content of the SDH Register is used to select the drive and head, and limit the Sector Buffer Counter to the size decoded by bits 5 and 6.

Figure 1 is a block diagram illustrating the relationship of the timing and control signals with the SDH Register and Sector Buffer Counter.

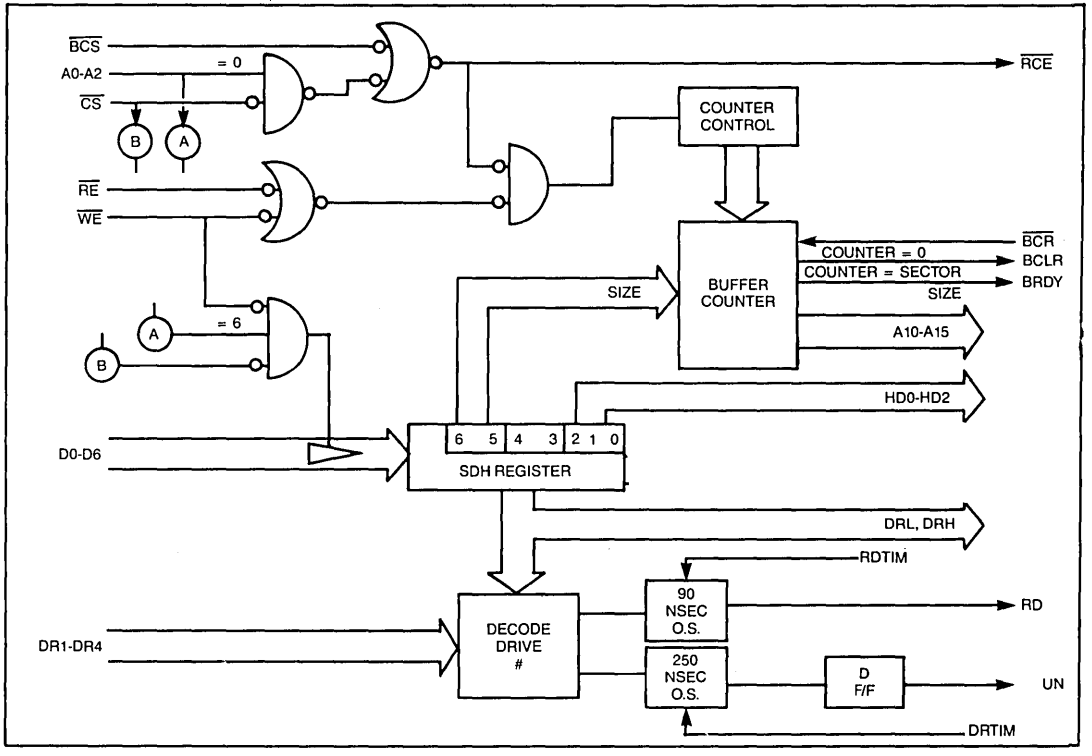


FIGURE 1. WD1100-21 BLOCK DIAGRAM

OPERATIONAL DESCRIPTION

The Host, to write to the SDH Register asserts $\overline{CS}$ and $\overline{WE}$, and places an address of zero on A0 thru A2.

6 5	4 3	2 1 0
SIZE	DRIVE	HEAD

SDH bits 2-1-0 make up signals HD2 HD1 and HD0 and are encoded externally to select one of eight heads. SDH bits 4 and 3 make up signals DRH and DRL, and they are encoded externally to select one of four drives. Bits 4 and 3 are also used internally to enable the appropriate input signal DRD1 thru DRD4 from the drive reading data. Bits 6 and 5 are encoded as follows and asserts BRDY (Buffer Ready) when the Sector Buffer Counter reaches the designated amount.

SDH6	SDH5	SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

Sector Buffer Counter is an 11-bit binary counter used to address the Sector Buffer and generate the BCLR and BRDY signals. Only address bits A10 thru A15 are supplied by the counter, the other five bits must be implemented externally. $\overline{BCR}$ asserted by the WD1010-05 resets the counter to zero. The counter in turn, asserts BCLR which is used to reset the five remaining address bits. The Sector Buffer may be written into and Read from by the Host and Disk.

The Host, to access the Sector Buffer, must place an address of zero on A0 thru A2, assert $\overline{CS}$ to select the WD1100-21, $\overline{WE}$ to write, or $\overline{RE}$ to read. This is done for each byte written to, or read from the Sector Buffer. In turn the WD1100-21 asserts $\overline{RCE}$ enabling the Sector Buffer, and increments the Sector Buffer Counter by one. when the count specified by SDH6 and SDH5 is reached, BRDY is asserted indicating the end of the Sector Buffer.

Reading or writing to the Sector Buffer from the disk is done in much the same manner. The difference is, that the WD1010-05 supplies the $\overline{WE}$ and $\overline{RE}$ instead of the Host. The WD1010-05 also replaces the $\overline{CS}$ with $\overline{BCS}$.

The drive selected by DRL and DRH, inputs its Read Data on one of the DRD1 thru DRD4 lines. SDH4 and SDH3 enables the appropriate signal and passes it on to an O.S. to be shaped and widened for use by a WD1010-05. The DRUN signal is produced by gating the selected DRD signal to an O.S. followed by a D flip flop.

ADJUSTMENTS

RD pulse width is established by the load placed on RDTIM. See Table 2 and Note 1.

DRUN is controlled by the resistance placed on DRTIM. Select DRD1 with the SDH Register. Then place a 5 MHz signal on DRD1 while monitoring DRUN on pin 15. It should be high. Then a 2.5 MHz signal is placed on the DRD1 input. DRUN should be low. The resistance chosen should be midway between DRUN just going high at 5 MHz. See Table 2 and Note 2.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Ambient Temperature under bias .....0°C (32°F) to 50°C (122°F).
Voltage on any pin with respect to V_{SS} ....-0.2V to 7.0V
Power dissipation .....1.5 Watts

STORAGE TEMPERATURE

Plastic .....-55°C(-67°F) to 125°C (257°F)
Ceramic.....-55°C(-67°F) to 150°C (302°F)

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

TABLE 1. DC OPERATING CHARACTERISTICS

T_A = 0°C (32°F) to 70°C (158°F), V_{CC} = +5V ± .25V, V_{SS} = 0V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{IL}	Input Leakage			-10	A	Pins 1-4, 25-31
I_{OL}	Output Leakage			10	A	Pins 1-4, 25-31
I_{IP}	Input Pullup	0.1		1.6	mA	Pins 10-12, 16-18, 22-24
V_{IH}	Voltage Input High	2.0			V	
V_{IL}	Voltage Input Low	-0.2		0.8	V	
V_{OH}	Voltage Output High	2.4			V	I_{OH} = -100μA
V_{OL}	Voltage Output Low			0.4	V	I_{OL} = 1.6mA
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
I_{CC}	Supply Current		200	250	mA	Outputs Open

AC TIMING CHARACTERISTICS

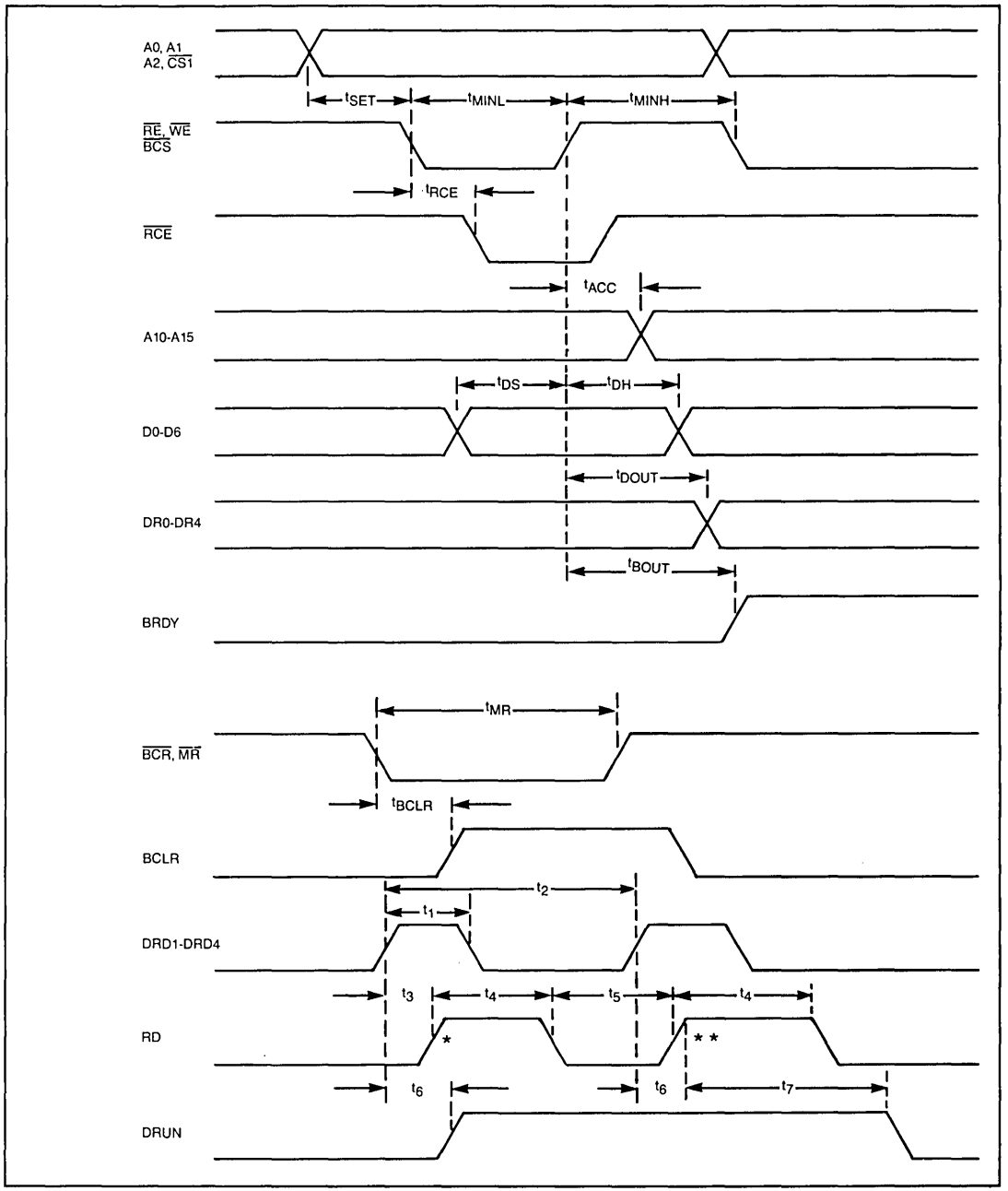


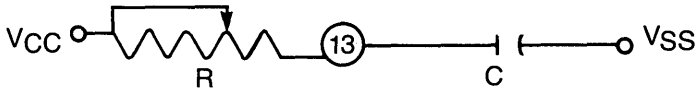
FIGURE 2. AC TIMING

*Trigger DRUN
**Retrigger DRUN

TABLE 2. TIMING CHARACTERISTICS **All units in nsec.**

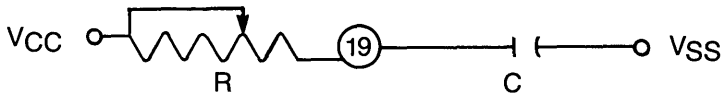
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	CONDITIONS
t_{SET}	A0 thru A2 and $\overline{CS}$ setup	0			
t_{MINL}	$\overline{RE}$, $\overline{WE}$, and $\overline{BCS}$ low	200			
t_{MINH}	$\overline{RE}$, $\overline{WE}$, and $\overline{BCS}$ high	100			
t_{RCE}	$\overline{RCE}$ delay from $\overline{BCS}$ or $\overline{CS}$			100	C = 50 pf
t_{ACC}	A10 thru A15 delay from $\overline{RE}$ or $\overline{WE}$			200	C = 50 pf
t_{DS}	D0 thru D6 setup time	50			
t_{DH}	D0 thru D6 hold time	100			
t_{DOUT}	DR1 thru DR4 delay			170	C = 50 pf
t_{BOUT}	$\overline{BRDY}$ delay			250	C = 50 pf
t_{MR}	$\overline{MR}$ and $\overline{BCR}$ pulse width	150			
t_{BCLR}	BCLR delay from $\overline{MR}$ or $\overline{BCR}$			200	C = 50 pf
t_1	DRD1 thru DRD 4 width	25			
t_2	DRD1 thru DRD4 cycle time		200		
t_3	RD delay from DRD1 thru DRD4			200	C = 50 pf
t_4	RD high	90	100	110	Note 1
t_5	RD low				$t_2 - t_4$
t_6	DRUN delay from DRD1 thru DRD4			200	Note 2
t_7	DRUN	225	250	275	

NOTE 1.



TYP - R = 10 Kohms, C = 150 pf
Adjust R to meet characteristics for t_4. Typical values for t_4 and t_5 are for 5MHz data rate.

NOTE 2.

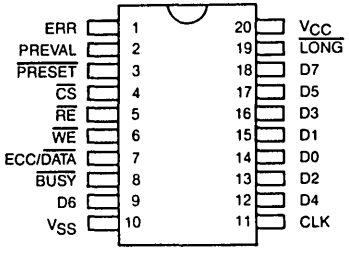


R = 10 Kohms, C = 150 pf
Adjust R to meet characteristics for t_7.

WD11C00-13 ECC Support Device

FEATURES

- 32-BIT COMPUTER SELECTED POLYNOMIAL
- PARALLEL INPUT AND OUTPUT
- DATA TRANSFER RATES UP TO 5 MBITS/SEC
- RECORD LENGTH UP TO 1038 BYTES INCLUDING CHECK BYTES
- TTL, MOS COMPATIBLE
- 20 PIN DIP PACKAGE
- CMOS TECHNOLOGY
- SINGLE + 5 VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD11C00-13 ECC Support Device is designed to provide ECC capabilities for Winchester Disk Controllers and accommodates data transfer rates up to 5 Mbits/sec. Data is transferred into and out of the WD11C00-13 via an 8-bit, bi- directional parallel data port.

The WD11C00-13 performs several operations including ECC byte generation, error detection, and error syndrome generation. Additionally, the WD11C00-13 supports user diagnostics by allowing transparent ECC byte transfers between the Host and disk medium.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	ERR	ERROR	O	This signal is valid only when the Byte Counter reaches the end of the syndrome bytes. Asserted indicates a non-zero syndrome, or the syndrome has not yet been generated. In the Long mode, ERR will be de-asserted at the completion of each ECC byte, but is of no meaning.
2	PREVAL	PRESET VALUE	I	PREVAL asserted presets the ECC accumulator to FFFFFFFF, and when de-asserted, presets the accumulator to B517894A. It is an asynchronous signal and enabled when $\overline{\text{PRESET}}$ is asserted and $\overline{\text{LONG}}$ de-asserted.
3	$\overline{\text{PRESET}}$	$\overline{\text{PRESET}}$	I	$\overline{\text{PRESET}}$ asserted and $\overline{\text{LONG}}$ de-asserted enables PREVAL.
4	$\overline{\text{CS}}$	$\overline{\text{CHIP SELECT}}$	I	$\overline{\text{CS}}$ asserted enables $\overline{\text{WE}}$ or $\overline{\text{RE}}$.
5	$\overline{\text{RE}}$	$\overline{\text{READ ENABLE}}$	I	When asserted, data is written to or ECC and Syndrome bytes read from the accumulator.
6	$\overline{\text{WE}}$	$\overline{\text{WRITE ENABLE}}$	I	When asserted, data and ECC bytes are written to the accumulator.
7	ECC/$\overline{\text{D}}$	ECC/$\overline{\text{DATA}}$	I	When $\overline{\text{DATA}}$ is asserted, data is written to the accumulator and ECC bytes are generated. When ECC is asserted, polynomial control logic is inhibited. ECC and syndrome bytes are transferred to or from the accumulator.
8	$\overline{\text{BUSY}}$	$\overline{\text{BUSY}}$	O	WD11C00-13 asserts $\overline{\text{BUSY}}$ while performing any function other than $\overline{\text{PRESET}}$.
9	D6	DATA BIT 6	I/O	This signal is bit 6 of an 8-bit, bi-directional, data bus.
10	V_{SS}	GROUND		Ground.
11	CLK	CLOCK	I	5 MHZ clock used for internal timing (see text for additional explanation).
12	D4	DATA BIT 4	I/O	This signal is bit 4 of an 8-bit, bi-directional data bus.
13	D2	DATA BIT 2	I/O	This signal is bit 2 of an 8-bit, bi-directional data bus.
14	D0	DATA BIT 0	I/O	This signal is bit 0 (LSB) of an 8-bit, bi-directional data bus.
15	D1	DATA BIT 1	I/O	This signal is bit 1 of an 8-bit, bi-directional data bus.
16	D3	DATA BIT 3	I/O	This signal is bit 3 of an 8-bit, bi-directional data bus.
17	D5	DATA BIT 5	I/O	This signal is bit 5 of an 8-bit, bi-directional data bus.
18	D7	DATA BIT 7	I/O	This signal is bit 7 (MSB) of an 8-bit, bi-directional data bus.
19	$\overline{\text{LONG}}$	$\overline{\text{LONG}}$	I	$\overline{\text{LONG}}$ is asserted when Long Mode is selected. This signal inhibits $\overline{\text{PRESET}}$, as well as ECC and Syndrome byte generation.
20	V_{CC}	POWER SUPPLY		+5V Power Supply

ARCHITECTURE

The WD11C00-13 is composed of an accumulator and necessary timing and control logic, to generate four ECC or Syndrome bytes. The generation process can be inhibited, allowing the WD11C00-13 to appear transparent to the four additional bytes that follow the end of data written to or read from the disk during READLONG or WRITELONG operations. The major blocks of the WD11C00-13 are shown in Figure 1.

Accumulator

The accumulator consists of a 32-bit serial, ring shift register. Access to this register is byte serial via the most significant byte. Due to the configuration of the register, an 8-bit byte requires only four clocks to shift to the next byte position.

The WD11C00-13 operates as a destructive read out. As each ECC or Syndrome byte is read out, it is replaced with zeros. Hence, as the last ECC or Syndrome byte is read, the accumulator is reset.

The content of the WD11C00-13 is altered by any of the following events:

1. Presetting to FFFFFFFF or B517894A with the $\overline{\text{PRESET}}$ and PREVAL input signals.
2. Passing data through the device to produce four ECC bytes (i.e. writing data to the disk).
3. Passing data and ECC bytes through the device to produce and hold a syndrome (i.e. reading data from the disk).
4. Writing only the ECC bytes into the device with no data (i.e. WRITELONG to, or READLONG from the disk, create a transparent effect on the ECC character).

Polynomial Control

The polynomial $X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$ is the same as that used in other Western Digital devices. ECC and Syndrome generation is initiated during data transfer by asserting $\overline{\text{DATA}}$ (ECC/$\overline{\text{DATA}}$). Polynomial logic is inhibited as the ECC and Syndrome bytes are read by asserting ECC (ECC/$\overline{\text{DATA}}$).

Preset Generator

$\overline{\text{PRESET}}$ and PREVAL are asynchronous inputs which do not require $\overline{\text{CS}}$ or Clock asserted. They provide a means of presetting the ECC register to FFFFFFFF or B517894A. When $\overline{\text{WE}}$ is asserted before the address mark (A 1F8) is read. $\overline{\text{PRESET}}$ and PREVAL are asserted prior to the device being selected. This presets the ECC register to FFFFFFFF. As the first data byte is reached, the polynomial control logic will have generated ECC bytes B517894A.

When an application calls for not passing the address mark (A 1F8) through the WD11C00-13, $\overline{\text{PRESET}}$ is asserted and PREVAL de-asserted before the device is selected. This presets the ECC register to B517894A, the same configuration that is reached when the address mark is read. In this manner, compatibility between drives is maintained.

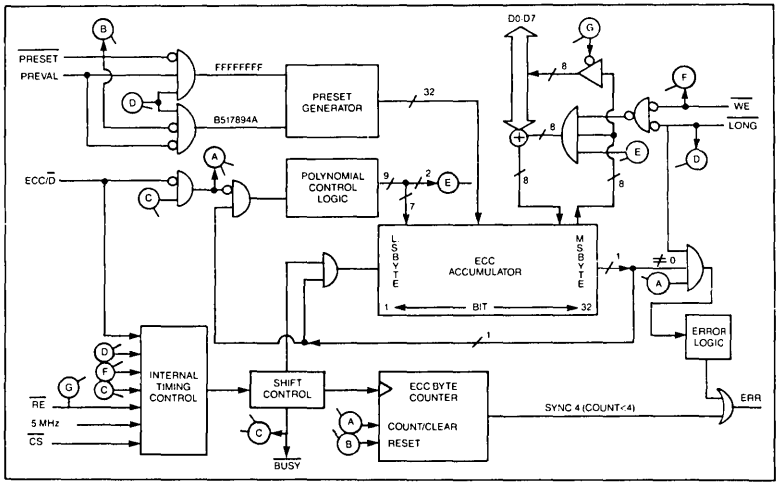


FIGURE 1. WD11C00-13 FUNCTIONAL BLOCK DIAGRAM

Byte Counter

As the ECC or Syndrome bytes are written into or read out of the accumulator, ECC (ECC/DATA) is asserted. This initiates the Byte Counter. The counter is incremented once for each byte and used internally to indicate when all 4 bytes (Sync 4) have been written or read. It is also used to control ERR timing and WE. The counter is reset synchronously during data transfer or asynchronously by asserting PRESET.

Error Logic

ERR is de-asserted only when the Byte Counter has reached the count of four (SYNC 4) and the Syndrome is equal to zero, or the device is in the long mode.

Internal Timing

With the exception of PRESET and PREVAL functions all operations are performed under control of the external 5 MHz clock. The internal timing is initiated by the following signals:

CS BUSY RE WE ECC/DATA LONG SYNC 4

When the device is selected for either a Read or Write function in the normal mode, the clocks function throughout the entire data transfer. When the WD11C00-13 is selected during WRITELONG mode, the clocks do not start until the ECC bytes from the Host or disk is reached (indicated by ECC/DATA). The clocks stop when the fourth byte has been counted.

When the WD11C00-13 is selected during READLONG mode, the clocks do not start until the ECC bytes previously loaded are sent to the Host or disk. The clocks continue as long as Read functions are requested, even if more than four ECC bytes have been called for.

LONG MODE COMMANDS

When in the Long Mode, PRESET can not be asserted, thus protecting the contents of the Accumulator from being altered by anything other than ECC bytes.

For diagnostic purposes, it is not desirable to generate ECC or Syndrome bytes on the data being passed between the Host and disk. Instead, the WD11C00-13 allows the ECC bytes to pass through unaltered. To accomplish this, READLONG and WRITELONG commands are provided. The three significant inputs used to accomplish this are LONG, WE and ECC/DATA, with LONG being the primary control.

While in the Long Mode with data on the bus, no internal clocks can be generated. Therefore, no data can be written into the Accumulator or ECC bytes produced. The content on the Accumulator remains unchanged from its Preset Value.

When the first of the ECC bytes is placed on the data bus, ECC (ECC/DATA) is asserted. With LONG inhibiting the polynomial control logic from functioning, the clocks are initiated and this byte, along with the next three, are written into the Accumulator unchanged. As stated in the clock description, after the fourth byte is written into the WD11C00-13 the clocks stop, preventing the destruction of the ECC bytes by additional Write functions.

Reading the ECC bytes from the WD11C00-13 is much the same as in WRITELONG, with the following exception: as each byte is read out, its location is reset to zero and the clock continues to run as long as RE is asserted.

SUMMARY

When writing to the WD11C00-13 during Long Mode, the polynomial and preset functions are inhibited and the clocks cannot run after the fourth byte. This protects the ECC bytes, making the device appear transparent.

When reading from the WD11C00-13 during Long Mode, ECC generation and preset functions are inhibited. The clocks can continue to run after the fourth byte, making it possible to supply the Host or disk with as many zeros as needed to fill the allotted space. This decision is controlled by the Host.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATING

V_{CC} with respect to V_{SS} (ground) . . . . . + 7V

Voltage on any pin with respect to V_{SS} . . . . . -0.3 to V_{CC} + 0.3 volts

Operating temperature . . 0°C (32°F) to 70°C (185°F)

Storage Temperature . . . . -65°C (-85°F) to 150°C (302°F)

NOTE:

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

TABLE 1. DC OPERATING CHARACTERISTICS

T_A = 0°C (32°F) to 70°C (158°F); V_{SS} = OV, V_{CC} = +5V ± .25V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100uA
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
I_{CC}	Supply Current			10	mA	In active state
				100	μA	In rest state

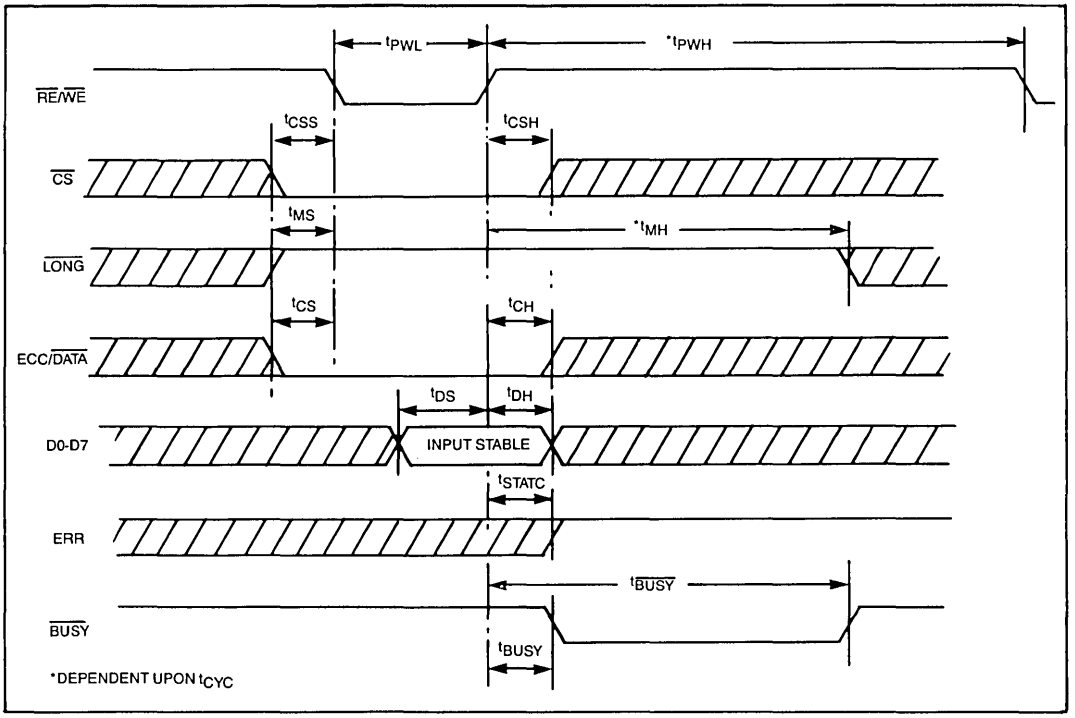


FIGURE 2. DATA INPUT TIMING

TABLE 2. DATA INPUT TIMING

All Units in nsec.

SYMBOL	CHARACTERISTIC	MIN	MAX	TYP
t_{PWL}	$\overline{RE}/\overline{WE}$ Pulse Width Low	124		
t_{PWH}	$\overline{RE}/\overline{WE}$ Pulse Width High	4T + 235*		
t_{CSS}	$\overline{CS}$ Setup to Leading Edge of $\overline{RE}/\overline{WE}$	10		
t_{CSH}	$\overline{CS}$ Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	0		
t_{MS}	Mode Input Setup to Leading Edge of $\overline{RE}/\overline{WE}$	14		
t_{MH}	Mode Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	4T +115*		
t_{CS}	Control Input Setup to Leading Edge of $\overline{RE}/\overline{WE}$	33		
t_{CH}	Control Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	37		
t_{DS}	Data Input Setup to Trailing Edge of $\overline{RE}/\overline{WE}$	40		
t_{DH}	Data Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	20		
t_{STATC}	Accumulator ≠ 0 to High Level After Trailing Edge of $\overline{RE}/\overline{WE}$		40	
$t_{\overline{BUSY}}$	$\overline{BUSY}$ Output to High Level After Trailing Edge of $\overline{RE}/\overline{WE}$		4T + 165*	
t_{BUSY}	$\overline{BUSY}$ to Low Level After Trailing Edge of $\overline{RE}/\overline{WE}$		85	
t_{CYC}	Clock Cycle Period	180		

*T = t_{CYC}

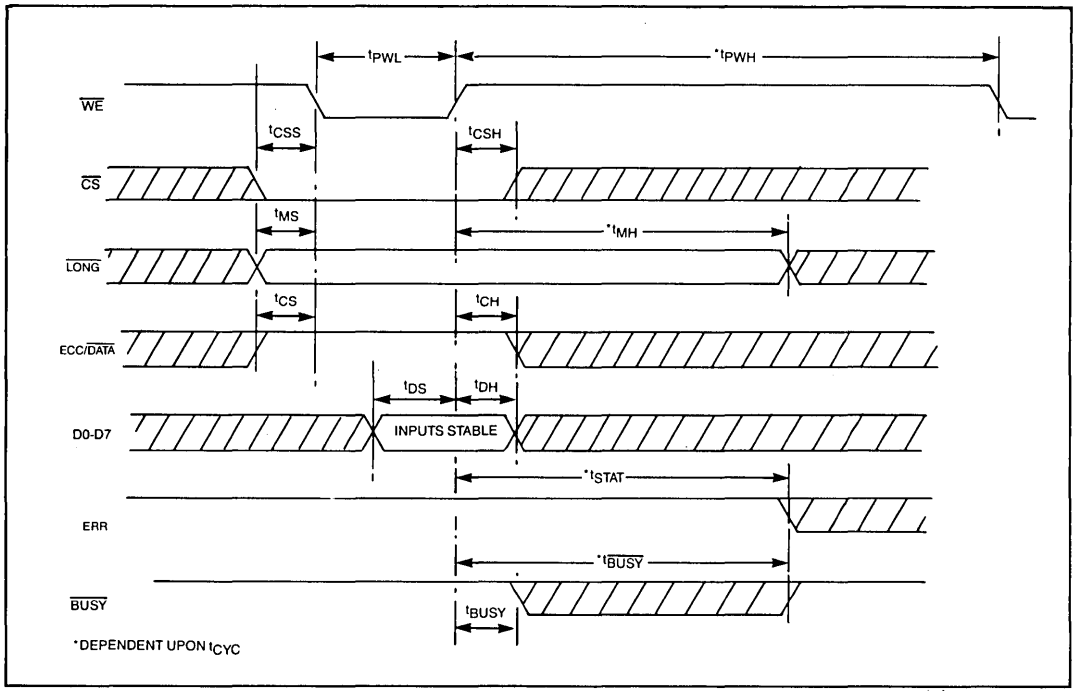


FIGURE 3. ECC BYTE INPUT TIMING

TABLE 3. ECC INPUT TIMING All Units in nsec.

SYMBOL	CHARACTERISTIC	MIN	MAX	TYP
^tPWL	$\overline{RE}/\overline{WE}$ Pulse Width Low	124		
^tPWH	$\overline{RE}/\overline{WE}$ Pulse Width High	4T + 235*		
^tCSS	$\overline{CS}$ Setup to Leading Edge of $\overline{RE}/\overline{WE}$	10		
^tCSH	$\overline{CS}$ Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	0		
^tMS	Mode Input Setup to Leading Edge of $\overline{RE}/\overline{WE}$	14		
^tMH	Mode Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	4T + 115*		
^tCS	Control Input Setup to Leading Edge of $\overline{RE}/\overline{WE}$	33		
^tCH	Control Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	37		
^tDS	Data Input Setup to Trailing Edge of $\overline{RE}/\overline{WE}$	40		
^tDH	Data Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	20		
^tSTAT	Accumulator ≠ 0 to Low Level After Trailing Edge of $\overline{RE}/\overline{WE}$		4T + 165*	
$^t\overline{BUSY}$	$\overline{BUSY}$ Output to High Level After Trailing Edge of $\overline{RE}/\overline{WE}$		4T + 165*	
^tBUSY	$\overline{BUSY}$ to Low Level After Trailing Edge of $\overline{RE}/\overline{WE}$		50	
^tCYC	Clock Cycle Period	180		

*T = ^tCYC

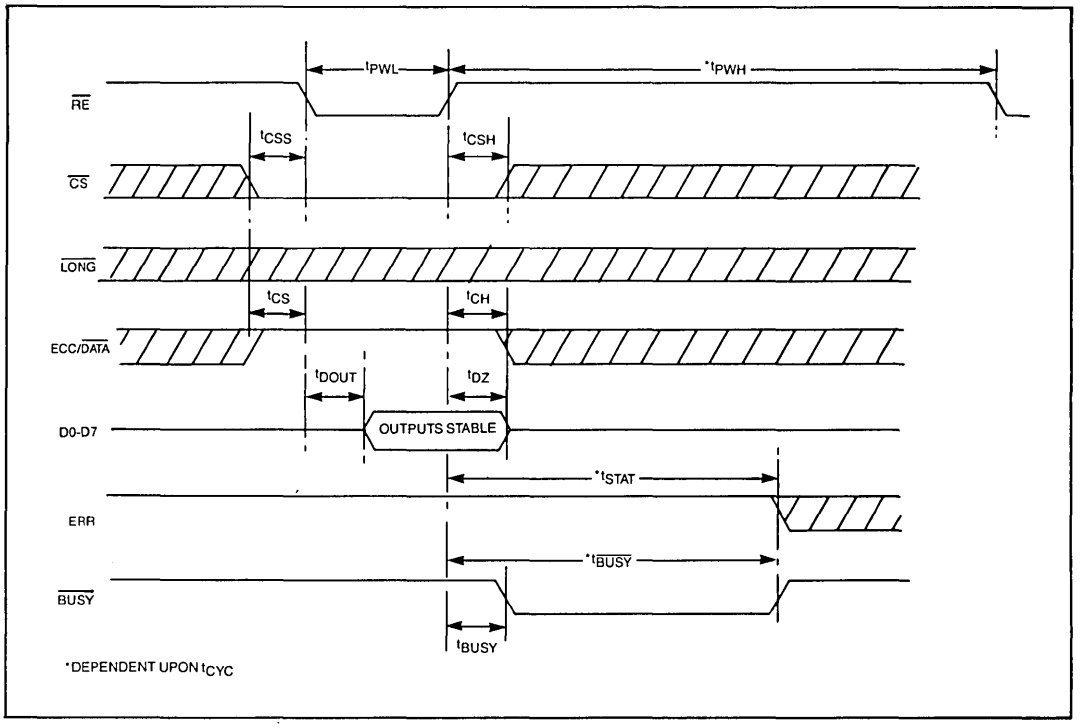


FIGURE 4. DEVICE OUTPUT TIMING

TABLE 4. DEVICE OUTPUT TIMING All Units in nsec.

SYMBOL	CHARACTERISTICS	MIN	MAX	TYP
t_{PWL}	$\overline{RE}/\overline{WE}$ Pulse Width Low	124		
t_{PWH}	$\overline{RE}/\overline{WE}$ Pulse Width High	4T + 235*		
t_{CSS}	$\overline{CS}$ Setup to Leading Edge of $\overline{RE}/\overline{WE}$	10		
t_{CSH}	$\overline{CS}$ Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	0		
t_{CS}	Control Input Setup to Leading Edge of $\overline{RE}/\overline{WE}$	33		
t_{CH}	Control Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	37		
t_{DOUT}	Data Output Valid After Leading Edge of $\overline{RE}$		50	
t_{DZ}	Data Bus Float After Trailing Edge of $\overline{RE}$		60	
t_{STAT}	Accumulator ≠ 0 to Low Level After Trailing Edge of $\overline{RE}/\overline{WE}$		4T + 165*	
$t_{\overline{BUSY}}$	$\overline{BUSY}$ Output to High Level After Trailing Edge of $\overline{RE}/\overline{WE}$		4T + 165*	
t_{BUSY}	$\overline{BUSY}$ to Low Level After Trailing Edge of $\overline{RE}/\overline{WE}$		50	
t_{CYC}	Clock Cycle Period	180		

*T = t_{CYC}

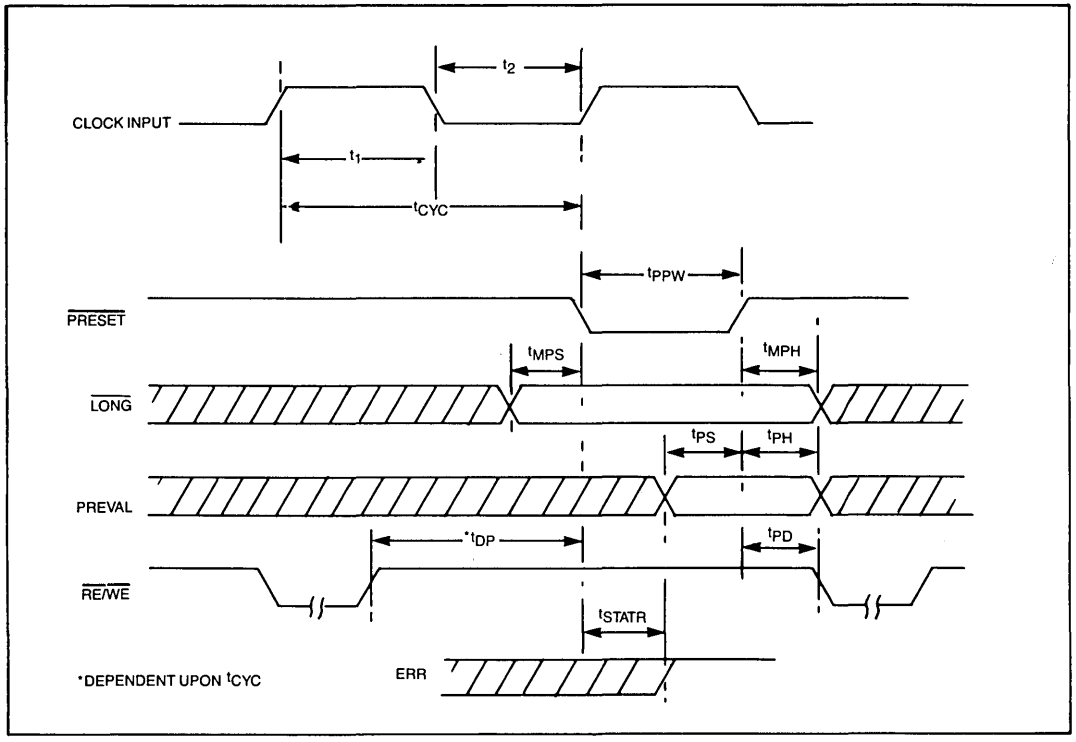


FIGURE 5. MISCELLANEOUS TIMING

TABLE 5. MISCELLANEOUS TIMING All Units in nsec.

SYMBOL	CHARACTERISTICS	MIN	MAX	TYP
t_1	Clock High Period	90		
t_2	Clock Low Period	90		
t_{CYC}	Clock Cycle Period	180		
t_{PPW}	$\overline{\text{PRESET}}$ Input Pulse Width Low	109		
t_{MPS}	Mode Setup to Leading Edge of $\overline{\text{PRESET}}$	23		
t_{MPH}	Mode Hold After Trailing Edge of $\overline{\text{PRESET}}$	0		
t_{PS}	SSC Input Setup to Trailing Edge of $\overline{\text{PRESET}}$	103		
t_{PH}	SSC Input Hold After Trailing Edge of $\overline{\text{PRESET}}$	9		
t_{DP}	Delay from Trailing Edge of $\overline{\text{RE}}/\overline{\text{WE}}$ to Trailing Edge of $\overline{\text{PRESET}}$	4T + 375*		
t_{PD}	Delay from Trailing Edge of $\overline{\text{PRESET}}$ to Leading Edge of $\overline{\text{RE}}/\overline{\text{WE}}$	0		
t_{STATR}	Accumulator ≠ 0 to High Level After Leading Edge of $\overline{\text{PRESET}}$	91		

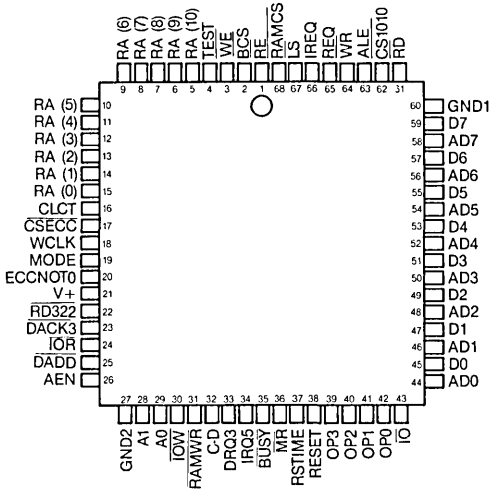
*T = t_{CYC}

WESTERN DIGITAL
CORPORATION

WD11C00-17
PC/XT Host Interface Logic Device

FEATURES

- 8-BIT HOST INTERFACE
- 3 MICRON CMOS TECHNOLOGY
- COMBINES RANDOM LOGIC AND SPECIALIZED CIRCUITS
- FAST SWITCHING SPEEDS
- LOW POWER DISSIPATION
- STATIC PROTECTION ON ALL I/Os
- PROPAGATION DELAYS OF 1.4 NANOSECONDS
- 68 PIN SURFACE MOUNTABLE PACKAGE
- SINGLE +5 VOLT POWER SUPPLY
- HIGH CURRENT BUS DRIVERS
- INTERFACE LOGIC CONTROL FOR PC BUS



PIN DESIGNATION

DESCRIPTION

The WD11C00-17 PC/XT Host Interface Logic Device combines the necessary random logic and specialized circuitry to interface the Western Digital chip set to the IBM PC/XT interface for Winchester Disk control. The chip contains integrated: Status Ports, Read/Write Ports, Sector Buffer Control, ECC Generation and Detection Logic, Reset Timing Logic, and Host Interface Logic. These features greatly simplify hardware requirements for the design engineer when using the WD chip set consisting of the: WD1015, WD1010A-05, and WD10C20-A. With appropriate decode logic, the WD11C00-17 appears to the Host as four contiguous I/O locations XX0-XX3. The 32-bit ECC Generation and Detection circuitry allows for realtime ECC check byte generation and error checking; ECC correction is via the WD1015. The WD11C00-17 also contains all the handshaking logic required for polled I/O and DMA transfers with the Host.

HOST INTERFACE

The WD11C00-17 PC/XT Host Interface Logic Device interfaces directly to the Host Data Bus via bi-directional high current bus drivers on the DO-D7 pins and high current dirvers on the DRQ3 and DRQ5 pins.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature ..... 0°C (32°F) to 55°C (131°F)

Voltage on any pin with respect to Ground (Vss) ..... -0.5 to 7.0V

Power Dissipation 1W

Storage Temperature Plastic ..... -55°C (-67°F) to + 125°C (257°F)

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the AC/DC Electrical Characteristics.

AC/DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITON
V_{IL}	TTL Low Level Input Voltage			0.8	V	Pins:1,2,3,4,16,17,18,19,25,32,39,40 ,41,42,43,44,46,48,50,52,54,56,58,61 ,63,64,66,67
V_{IH}	TTL High Level Input Voltage	2.4			V	Pins: Same as V_{IL}
V_{TL}	Schmitt Threshold Voltage Low	0.9			V	Pins:23,24,26,28,29,30,37,38,45,47, 49,51,53,55,57,59
V_{TH}	Schmitt Treshold (High)			2.4	V	Pins:Same as V_{TL}
V_{HY}	Hysteresis	0.35			V	Pins: Same as V_{TL}
I_{OL}	Low Level Output Current Single Buffer	5.0			mA	V_{DL} = 0.4V Pins:5,6,7,8,9,10,11,12,13,14,15,20, 22,31,35,62,65,68
	Tri-State, Single Buffer	5.0			mA	Pins:44,46,48,50,52,54,56,58
	Tri-State, Double Buffer	10.0			mA	Pins:1,3,33,34,45,47,49,51,53,55
	Open Drain N-Channel	5.0			mA	Pins:36,37
I_{OH}	High Level Output Current Single Buffer	-5.0			mA	V_{OH} = 2.4V Pins: Same as I_{OL}
	Tri-State, Single Buffer	-5.0			mA	Pins: Same as I_{OL}
	Tri-State, Double Buffer	-10.0			mA	Pins: Same as I_{OL}
I_{DD}	Supply Current			15	mA	Pins: Same as I_{OL}
I_I	Input Leakage	-10.0		10	uA	Vin = 0 or 5.5V
I_Z	Tri-State Leakage	-10.0		10	uA	Vo = 0 or 5.5V

PIN DESCRIPTIONS

Pin descriptions are listed in Table 1.

TABLE 1. PIN DESCRIPTIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	Read Enable	$\overline{RE}$	Input when $\overline{BCS}$ is low. Read strobe is bi-directional for Sector Buffer Address. Output when BCS is high, follows RD Pin 61.
2	Buffer Chip Select	$\overline{BCS}$	Controls direction of bi-directional $\overline{RE}$, $\overline{WE}$ lines. Enables RAMCS for WD1010 access.
3	Write Enable	$\overline{WE}$	Input when $\overline{BCS}$ is low. Write strobe is bi-directional for Sector Buffer Address. Output when BCS is high, follows $\overline{WR}$ Pin 64.
4	Test	TEST	Input active high, used for test only, controls state of internal RA10 (end of data) during ECC test. TEST = LOW DATA TEST = HIGH END OF DATA
5-15	RAM Address	$\overline{RA10}$ RAO	Outputs active high, address Sector Buffer RAM and WD1010.
16	Clear Count	CLCT	Input active high clears lower RAM address counter outputs RA - RA7.
17	Chip Select ECC	$\overline{CSECC}$	Input active low enables the ECC function.
18	Write Clock	WCLK	Input 5 MHz clock for the ECC function.
19	Mode	MODE	Input when high selects normal mode of the ECC function (i.e., check bytes are generated after end of data). When low selects long mode and inhibits preset function of ECC logic (i.e., check bytes are not generated after end of data and logic passes check bytes transparently from Host to disk).
20	ECC Not Zero	ECC NOT 0	Output active high indicates to WD1015 that an error has been detected while comparing check bytes at end of data stream with check bytes generated internally.

TABLE 1. PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
21	+5 VDC	VCC	Input supply voltage.
22	Read Port 322	RD322	Output active low when Host reads status Port 322.
23	DMA Acknowledge 3	DACK3	Input active low acknowledges DMA request 3 (DRQ3).
24	I/O Read	IOR	Input active low enables data onto D0-D7 outputs when Host wants to read data or status.
25	Device Address Code	DADD	Input active low when address 320 thru 323 is present on the Host Address Bus.
26	Address Enable	AEN	Input active high indicates that DMA Controller (Host) has control over the address, control, and data buses. Used to enable Host to disk I/O functions.
27	Ground	GND	Ground.
28	Address Bit 1	A1	Input active when Host asserts A1 to high state. Used to enable Host to disk I/O functions.
29	Address Bit 0	A0	Input active high when Host asserts A0 to high state. Used to enable Host to disk I/O functions.
30	I/O Write	IOW	Input active low strobes data from the Data Bus into internal devices or into the Sector Buffer RAM when Host performs a write function.
31	RAM Write	RAMWR	Output active low when either Host, WD1010 or WD1015 wants to write to Sector Buffer RAM.
32	Control/Data	C/D	Input when low indicates that Controller expects either a command or status block transfer. When high, indicates that Controller expects a data block transfer. Used to enable a data block transfer. Used to enable disk I/O control section.
33	DMA Request 3	DRQ3	Output active high requests DMA service from the Host. Remains high until DACK 3- goes low. Asserted when the Controller is ready to accept data or data is ready to be read.
34	Interrupt Request 5	IRQ5	Output active high signals to Host that service is required. Remains high until Host interrupt service routine resets it. Activated when the Controller has completed disk operation.
35	Busy	BUSY	Output active low indicates Host has selected controller and is about to perform an I/O operation.
36	Master Reset	MR	Bi-directional input active low when external Power UP Reset detects dropping VCO level. Clears all internal registers. Output active low when Host either performs a soft reset, or handshake reset from the bus is detected via the RESET Pin 38.
37	Reset Time	RSTIME	Input threshold adjust for the duration of the MR Pin 36 active low time during soft Reset.
38	Reset	RESET	Input active high when Host performs a bus reset. Clears all internal registers and active MR Pin 36 to active low.
39-42	Option 0,1,2,3	OPO 1,2,3	Inputs normally high via internal pull up resistors. Can be activated low by applying GND to the input. Disk configuration readable on Data Bus by Host via status read to Port 322. OPO - DO, OP1 - D1, OP2 - D2, OP3 - D3.
43	Input/Output	I/O	Input controls direction on Internal Data Bus Buffer form Host's point of view. High = input to Host. The ADX Bus is driven onto the DX Bus. Low = output from Host. DX Bus is received and driven to the ADX Bus.

TABLE 1. PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
44,46 48,50 52,54 56,58	Address/Data Bus	AD0-AD7	Bi-directional Bus carries address information to Internal RAM Address Counter and control de-multiplexer. Carries data to and from the internal ECC function and the external Sector Buffer RAM.
45	Data Bus 0	D0	Bi-directional Bus interfaces Controller to Host Data Bus.(D0 through D7).
47	Data Bus 1	D1	
49	Data Bus 2	D2	
51	Data Bus 3	D3	
53	Data Bus 4	D4	
55	Data Bus 5	D5	
57	Data Bus 6	D6	
59	Data Bus 7	D7	
60	Ground	GND	Ground.
61	Read	RD	Input active low when WD1015 performs a read operation.
62	Chip Select 1010	CS1010	Output active low when WD1015 performs a read or write operation to the WD1010.
63	Address Latch Enable	ALE	Input active high when WD1015 asserts ALE. Used internally to select and latch the control demultiplexer.
64	Write	WR	Input active low when WD1015 performs a write operation.
65	Request	REQ	Output active high indicates to the Host that Controller is ready to accept data from or transfer data to the Host. Handshake signal for transfers between Host and Controller. The state of this output is read on DO by the Host via a status read to Port 321.
66	Interrupt Request	IREQ	Input when asserted enables REQ. When low, it indicates to the Host that the operation is complete.
67	Long/Short	LS	Input signal is high during a Host Controller transfer. The Controller is in the long mode (Data Transfer) when high. When this signal is low during Host Controller transfer, the Controller is in the short mode (Command Transfer).
68	RAM Chip Select	RAMCS	Output active low enables the external Sector Buffer RAM for read/write operations by the Host, WD1015 or WD1010.

FUNCTIONAL DESCRIPTION

The WD11C00-17 PC/XT Host Interface Logic Device combines random logic and specialized circuits into one device. The internal architecture of the WD11C00-17 is shown in block diagram format and illustrated in Figure 1.

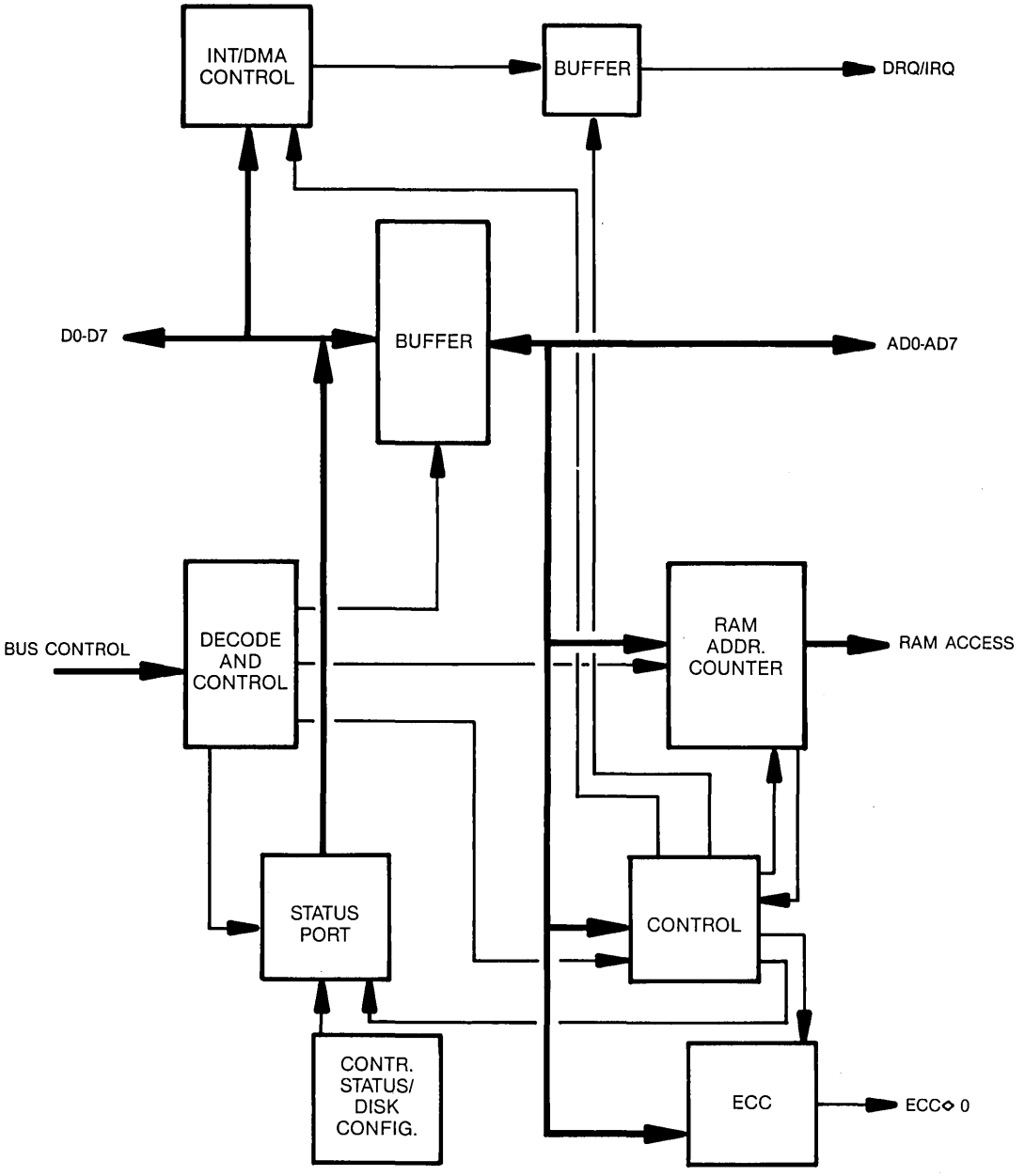


FIGURE 1. WD11C00-17 PC/XT HOST INTERFACE LOGIC DEVICE BLOCK DIAGRAM

STATUS PORTS

All port address decoding is done internally in the WD11C00-17. This is done via the AO and A1, and DADD inputs. The board's hardware status register and INT/DRQ latches are contained within the WD11C00-17. The board's hardware status is available to the Host via a read to Port 321. This is a read only function. The bits are defined as follows:

Bit 7 - Unused

Bit 6 - Unused

Bit 5 - Interrupt Request (IRQ)

Bit 4 - Data Request (DRQ)

Bit 3 - Busy (BUSY)

Bit 2 - Command/Data (C/$\overline{D}$)

Bit 1 - Input/Output (I/$\overline{O}$)

Bit 0 - Request (REQ)

The four lower order bits (OPO-OP3) of the drive configuration information are readable on the Data Bus by the Host via read operation to Port 322. This is a read function only. OPO-OP3 are input signals to the WD11C00-17, and are normally high due to internal pull-up resistors. OP0-OP3 are written directly to the Data Bus via DO-D3 outputs from the WD11C00-17.

RD322 output is generated by the WD11C00-17 so that external 74LS244 can be used to read the four high order bits (OP4-OP7) of the drive configuration information. These bits are pulled up by external 4.7K pull-up resistors.

Port 323 contains two bits which enable or disable the interrupt and DMA request lines to the Host. This is a write function only. The bits are defined as follows:

Bits 7-2 - Unused

Bit 1 - Interrupt Request Enable

Bit 0 - DMA Request Enable

READ/WRITE PORTS

All port address decoding is done internally in the WD11C00-17. This is done via the AO and A1, and DADD inputs. A complete port summary is defined in Table 2.

TABLE 2. READ/WRITE PORTS

ADDRESS	READ FUNCTION	WRITE FUNCTION
320/324	Read Data, Board to Host	Write Data, Host to Board
321/325	Read Board Hardware Status	Board Software Reset
322/326	Read Drive Configuration Information	Board Select
323/327	Not Used	Set/Reset DMA, IRQ Masks

All reads and writes to Port 320 result in data being transferred from the Sector Buffer and the Sector Buffer Counter being incremented.

Write to Port 321 results in a software reset. This has the same effect as a hardware reset.

Write to Port 322 results in a board selection. This must be done prior to each command.

SECTOR BUFFER CONTROL

The WD11C00-17 contains all the necessary Sector Buffer address counters and generates Sector Buffer chip select and Sector Buffer read/write signals.

The RAO through RA9 outputs are used to control the Sector Buffer. A 2K by 8 RAM is used but only 1K of it is necessary so only the lower 1K is used. This 1K is divided into four 256 byte pages.

The RA8-RA10 outputs are rsetable by the WD1015. This allows the WD1010 to access the WD1010 tasks files.

The RA10 putput is used to de-assert DRQ3, informing the Host that the Sector Buffer is either empty or full, and signals the end of the data field or the start of the ECC field to the ECC logic in the WD11C00-17.

The lower two pages of the Sector Buffer are used to store the 512 bytes of sector data. The lower page is also used to store command information prior to passing it along to the WD1015 and, to store ECC bytes.

The $\overline{RAMCS}$ and $\overline{RAMWR}$ outputs are used to select the Sector Buffer and Read/Write to the RAM.

The WD1015 outputs the $\overline{CLCT}$ signal to the WD11C00-17. This results in the Address Counter outputs RAO-RA7 to be cleared.

DISK, HOST, AND WD1015 I/O CONTROL

The WD11C00-17 is used in conjunction with the WD1015 and the Sector Buffer in controlling the WD1010 and performing Host transfers.

Commands are transferred by the Host into the first 256 byte page within the Sector Buffer. The WD1015

then reads these commands and loads the WD1010's task file registers with the appropiate information.

The WD1010's task file registers are selected via the RA8-RA10 outputs together with the CS1010-output.

The WD11C00-17 inputs $\overline{BCS}$, $\overline{RE}$, and $\overline{WE}$, are asserted by the WD1010 when it wants to read the Sector Buffer. A read or write by the WD1015 to the WD1010's task file registers results in the $\overline{RE}$ or $\overline{WE}$ outputs to be asserted. The $\overline{RE}$ and $\overline{WE}$ line are bi-directional and are inputs when $\overline{BCS}$ is low.

The WD11C00-17 inputs $\overline{RD}$ and $\overline{WR}$ are used by the WD1015 when it wants to read or write either the Sector Buffer or the WD1010.

The Host Data Bus (DO-D7) interfaces directly to the WD11C00-17 and is driven via bi-directional high current bus drivers to the chip.

The bus signals DRQ3 and IRQ5 are driven by internal high current drivers.

The AO, A1, $\overline{DACK3}$, $\overline{IOR}$, $\overline{IOW}$ and $\overline{RESET}$ inputs to the WD11C00-17 all feature Schmitt trigger inputs to ensure noise immunity.

The WD1015 outputs the $\overline{CLCT}$ signal to the WD11C00-17. This results in the Address Counter outputs RAO-RA7 to be cleared.

The $\overline{DADD}$ input to the WD11C00-17 is generated by the external address decode logic. The WD11C00-17 will decode which of the four ports is being selected, but the external circuitry must decode the proper port address range of 320 through 323.

The AEN input to the WD11C00-17 is asserted when the DMA controller has control over the bus. AEN's assertion de-gates the Host Processor and other devices from the I/O channel.

The $\overline{BUSY}$, $\overline{CD}$, and I/O inputs to the WD11C00-17 are all generated by the WD1015 and passed to the WD11C00-17 so that they may be read in the board's hardware status register.

ECC GENERATION AND DETECTION

The WD11C00-17 generates and appends the four byte ECC to the data stream. Proper placement of the ECC requires determination of the end of the data stream. Assertion of RA10 by the WD11C00-17 Address Counter indicates RAM overflow and the end of the data stream. After writing the four ECC bytes to the disk, the WD11C00-17 ECC circuitry supplies all zero bytes to the AD0 through AD7 Bus as long as the ECC function is selected.

During a read operation, the ECC circuitry recomputes the ECC. Comparison of the previously written ECC and computed ECC occurs at the end of the data stream. The ECC circuitry records the results of the comparison. Any additional writes to the Sector Buffer are ignored. If the results of the comparison is non-zero, then the WD11C00-17 asserts a ECC NOT 0 signal. Assertion of ECC NOT 0 enables the disk controller to attempt error correction.

During Writelong and Readlong commands, the ECC generations and checking is disabled. A Writelong command caused the WD11C00-17 to accept any four bytes from the Host, and stores them internally. These bytes are written to the disk unaltered.

A Readlong command causes the WD11C00-17 to accept the four bytes written on the disk. These bytes are passed to the Host unaltered. This allows the Host to induce errors anywhere in the data stream and check for predictable results.

The ECC circuitry requires a 5 MHz input clock.

The polynomial $X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$ is the same as that used in other Western Digital devices.

RESET TIMING

When asserted, RST places the board in its intitial power-up condition, setting the internal parameters and initializing on- board circuitry properly. The WD11C00-17 has an internal one-shot that handles the reset pulse width. The input RSTIME controls the duration of the active low reset pulse that originates from the MR- output.

The RESET input is hard wired to the bus interface reset input. A reset on this pin clears all internal registers and forces the $\overline{MR}$ output low.

The $\overline{MR}$ pin is bi-directional and acts as an input when the exteranl VCC detect circuit forces the board into a reset conditon. When this occurs, the internal registers are reset.

Figure 2 illustrates the WD11C00-17 PC/XT Host Interface Logic Device incorporated into the WD1002S-WX2 Winchester Disk Controller Board's architecture.

Figure 2 illustrates the WD11C00-17 PC/XT Host Interface Logic Device incorporated into the WD1002S-WX2 Winchester Disk Controller Board's architecture.

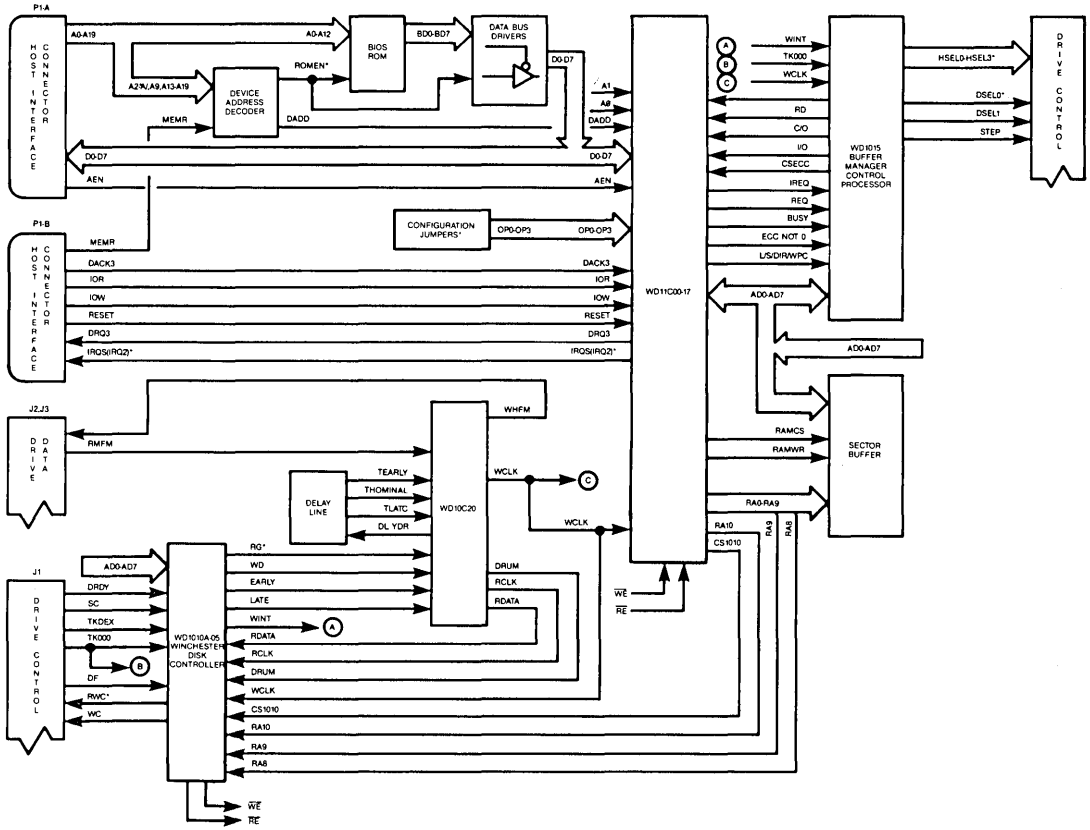


FIGURE 2. WD1002S-WX2 WINCHESTER DISK CONTROLLER ARCHITECTURE

WD33C93
SCSI-Bus Interface Controller

FEATURES

- IMPLEMENTS FULL SCSI BUS FEATURES: ARBITRATION, DISCONNECT, RECONNECT, PARITY, AND SYNCHRONOUS DATA TRANSFERS
- COMPATIBLE WITH MOST MICROPROCESSORS THROUGH AN 8-BIT DATA BUS; SUPPORTS BOTH MULTIPLEXED AND NON-MULTIPLEXED ADDRESS/DATA BUS SYSTEMS
- CAN BE USED AS HOST ADAPTER OR PERIPHERAL ADAPTER
- PROGRAMMED I/O OR DMA TRANSFERS
- INCLUDES 48-MA DRIVERS FOR DIRECT CONNECTION TO THE SCSI BUS
- INTERNAL 24-BIT TRANSFER COUNTER
- PROGRAMMABLE TIMEOUTS FOR SELECTION AND RESELECTION
- "COMBINATION" COMMANDS GREATLY REDUCE INTERRUPT-HANDLING RESPONSIBILITIES
- SPECIAL "TRANSLATE ADDRESS" COMMAND PERFORMS THE LOGICAL-TO-PHYSICAL ADDRESS TRANSLATION
- SINGLE +5V SUPPLY
- AVAILABLE IN 44-PIN CHIP CARRIER OR 40-PIN DIP
- LOW POWER CMOS DESIGN

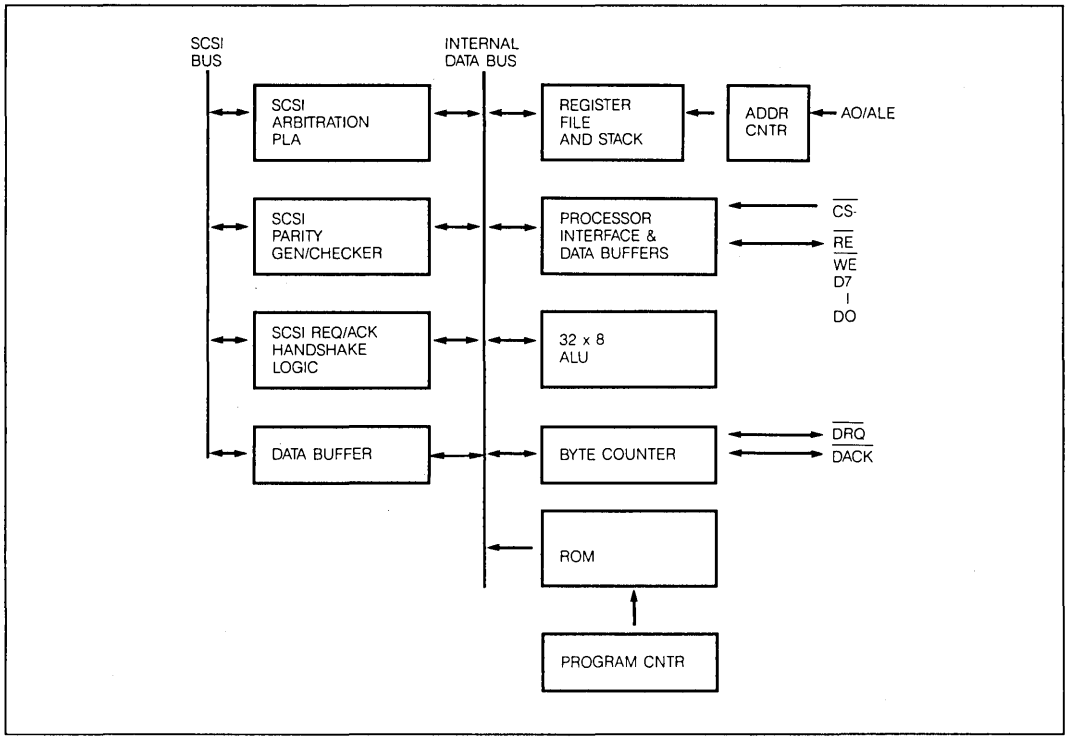
DESCRIPTION

The WD33C93 is a MOS/VLSI device which is implemented in the WD CMOS-3, 3-micron gate process. It operates from a single 5 volt supply and is available in either a 44-pin chip carrier or a 40-pin dual-in-line package. All inputs and outputs are TTL-compatible.

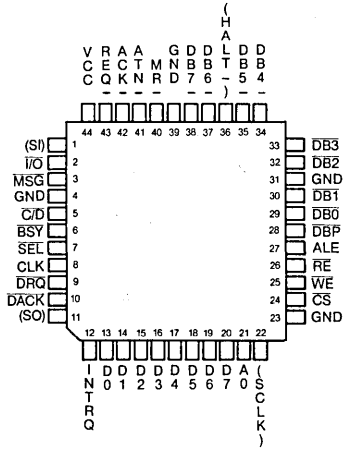
The WD33C93 is intended for use in Host or peripheral systems which interface to the SCSI (Small Computer Standard Interface) Bus. When used in the Host system, the WD33C93 interfaces both to the Host bus (8086/8088 type) and to the SCSI Bus. It waits for the Host to give it a command to select the desired unit. The WD33C93 then arbitrates for the SCSI Bus and selects the peripheral unit. If it fails to get the bus because of a higher priority Host, it continues trying, notifying the Host when it has succeeded by generating an interrupt. When the peripheral requests a command byte from the Host, the WD33C93 receives the request and generates an interrupt to the Host. The Host responds to the interrupt by giving a "Transfer Info" command and a peripheral command byte to the WD33C93. The WD33C93 sends the command byte to the peripheral, and the process continues until all command, data, and status bytes have been transferred.

When the WD33C93 is used in a peripheral system, it can communicate to the local processor and the SCSI Bus just as it does when used as a Host adapter. The WD33C93 has the additional capability of interfacing with the WD Bus. This means that in the data transfer phase, rather than interfacing to an external DMA controller, it can issue read and write enables in order to access the Sector Buffer.

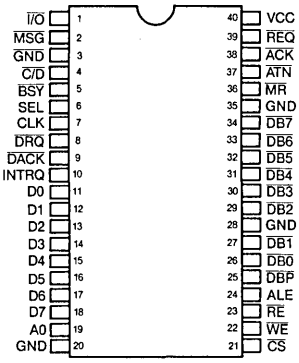
The WD33C93 implements the full SCSI physical path definition for use with the single-ended interfacing option. Arbitration, parity, and synchronous transfers will be implemented along with the standard SCSI physical path signaling.



WD33C93 BLOCK DIAGRAM



44 PIN CHIP CARRIER



40 PIN DIP

Note: Pins in parentheses are for test purposes only, and should be left unconnected for normal chip operation.

WD1002-05 Winchester/Floppy Controller

FEATURES

- CONTROL FOR UP TO 3 WINCHESTER AND 4 FLOPPY DRIVES.
- ON BOARD DATA SEPARATOR AND WRITE PRECOMPENSATION
- 128, 256, 512, AND 1024 BYTE SECTOR SIZES.
- PROGRAMMABLE SECTOR SIZES TO 1K.
- AUTOMATIC TRACK FORMATTING ON HARD AND FLOPPY DISKS.
- MULTIPLE SECTOR OPERATIONS.
- 5-BIT SINGLE BURST ERROR CORRECTION ON WINCHESTER.
- 5-MBIT DATA TRANSFER RATE.
- ECC DIAGNOSTIC COMMANDS (READ LONG & WRITE LONG).
- SINGLE + 5V POWER SUPPLY.

DESCRIPTION

The WD1002-05 Winchester-Floppy Controller (WFC) is a stand-alone general purpose board designed to interface up to three 5 1/4" Winchester hard disks and up to four 5 1/4" floppy disk drives. The WFC implements all the logic required for a variable length sector (to 1K bytes), ECC correction, data separation and Host interface circuitry. The Winchester interface is based on the Seagate ST506 and the floppy interface on the Shugart SA450. All necessary buffers and drivers/receivers are on board.

Communication to and from the Host is made via a separate computer access port. This port consists mainly of an 8-bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macrocommands are transferred via this 8-bit bus. An on-board Sector Buffer allows data transfers to the Host computer at a rate independent of the drive transfer rate.

The WD1002-05 Controller board is based on the WD1014 EDS device and WD1015 Buffer Controller device, as well as the WD2797 Floppy Disk Controller and WD1010 Winchester Disk Controller chips. It is form factor compatible with most 5 1/4" Winchesters and may be directly mounted on the drive.

ARCHITECTURE

The Block Diagram of the WD1002-05 is shown in Figure 1. The heart of the system is the WD1015 Buffer/Controller, which generates and processes all data and control lines, along with the WD1014 EDS that generates all control signals that cannot be handled in real time by the WD1015.

Commands, parameters, and data are entered via the Host Interface Logic. The WD1015 accepts both floppy and Winchester commands in identical format, converting these parameters to the WD1797/WD1010 protocol. Data is read from the selected drive and transferred to the Sector Buffer. If an error in the data field has been encountered, the WD1015 instructs the controllers to perform retries automatically. On a Winchester drive, the WD1014 ECC device is enabled and error correction procedures invoked. Error Correction may be disabled via software from the Host to allow "CRC-only" formatted Winchester drives to be used in the system. Data Separation and Write Precompensation Logic is onboard for Winchester transfers, while the WD2797 Floppy Controller provides an integrated Data Separator and adjustable write precomp. After the Sector Buffer is full, the WD1015 informs the Host Interface Logic that data may be read by the Host. The use of an on-board Sector Buffer provides both transparent error correction and data transfers to the Host that are independent of drive transfer rates.

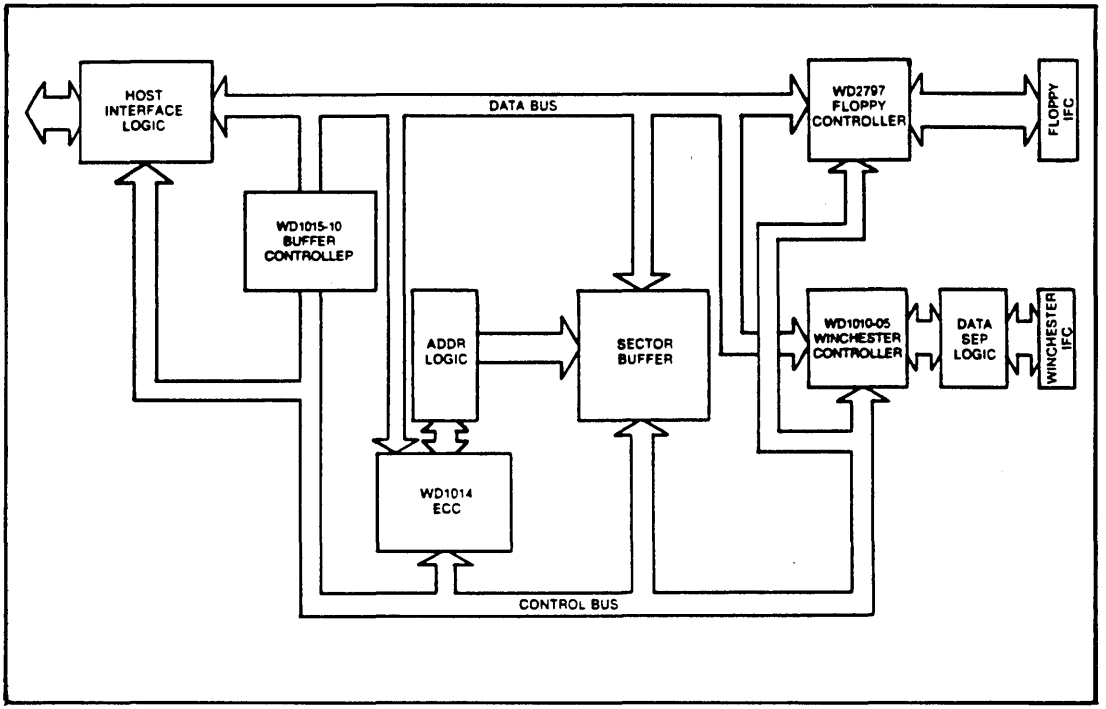


Figure 1. WD1002-05 BLOCK DIAGRAM

HOST INTERFACE

The WD1002-05 has been designed to interface with a Host processor via a parallel port or CPU bus configurations. The specific signals are compatible with the Western Digital WD1000/WD1001 series of Winchester-only controller boards. With the inclusion of the WD1015, the previous WAIT signal is no longer necessary but has been provided for compatiability; status information is always availabale to the Host for monitoring command progress. When the Busy bit is set, no other status bits are valid.

The Host Interface connector (J5) consists of an 8-bit bi-directional bus, three address lines, and read and write signals. All functions within the WD1002-05 are initiated by the Host Interface.

SIG PIN	SIG GND	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
1 3 5 7 9 11 13 15	2 4 6 8 10 12 14 16	DAL 0 thru DAL 7	DATA 0 thru DATA 7	I/0	8-bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the $\overline{CS}$ line is de-asserted.
17 19 21	18 20 22	A0 A1 A2	ADDRESS 0 ADDRESS 1 ADDRESS 2	I	These three Address Lines are used to select one of nine registers in the Task File or the Sector Buffer. They must remain stable during all read and write operations.
23	24	$\overline{CS}$	$\overline{CARD\ SELECT}$	I	When $\overline{Card\ Select}$ is active along with $\overline{RE}$ or $\overline{WE}$, data is read or written via the DAL bus. $\overline{CS}$ must make a transition for each byte read from or written to the Task File.
25	26	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	I	When $\overline{Write\ Enable}$ is active along with $\overline{CS}$, the Host may write data to a selected register of the WD1002-05.
27	28	$\overline{RE}$	$\overline{READ\ ENABLE}$	I	When $\overline{Read\ Enable}$ is active along with $\overline{CS}$, the Host may read data from a selected register of the WD1002-05.
29	30	Pull-up (PUP)			Used only when replacing WD1000 or WD1001 with WD1002-05. Tied to a pull-up resistor.
31	32	Not Connected			
33	34	Not Connected			
35	36	INTRQ	INTERRUPT REQUEST	0	The Intererupt Request Line is asserted whenever a command has been completed. It is de-asserted when the Status Register is read, or a new command is loaded via the DAL lines.
37	38	DRQ	DATA REQUEST	0	The Data Request line is asserted whenever the Sector Buffer contains data to be read by the Host, or is awaiting data to be loaded by the Host. This line is de-asserted whenever the buffer has been exhausted or filed by the Host.
39	40	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	The $\overline{Master\ Reset}$ line initializes all internal logic on the WD1002-05. Sector Number, Cylinder number and SDH are cleared, stepping rate for Winchester devices are set to 7.5mS, stepping rate for floppies is set to 40 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRDQ and INTRQ signals are de-asserted.

Note: All even numbered pins (2 through 40) are to be used as signal grounds. Power ground is available on J6, pin 1.

DRIVE CONNECTORS

Six connectors are provided for connection of up to three Winchester and four Floppy drives. All applicable drivers and receivers have been included on the board to allow direct connections to the drives. All signals to the Floppies are daisy-chained and require the last (or only) drive to contain termination resistors.

The Winchester control cable is daisy-chained and requires resistors on the last drive termination. Most Floppy/Winchester drives can be configured to provide this. The data cables on the Winchester are radially connected to each drive. Three data cable connectors are included on the board.

FLOPPY DRIVE CONTROL/DATA CONNECTOR J8

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2		NC
3	4		NC
5	6	0	Drive Select 1
7	8	I	Index/Sector
9	10	0	Drive Select 2
11	12	0	Drive Select 3
13	14	0	Drive Select 4
15	16	0	Motor On
17	18	0	Direction In
19	20	0	Step
21	22	0	Write Date
23	24	0	Write Gate
25	26	I	Track 00
27	28	I	Write Protect
29	30	I	Read Data
31	32	0	Side Select
33	34		NC

34-PIN WINCHESTER DRIVE CONTROL CONNECTOR J7

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	0	RWC
3	4	0	Head Select 2
5	6	0	Write Gate
7	8	I	Seek Complete
9	10	I	TRACK 000
11	12	I	Write Fault
13	14	0	Head Select 0
15	16		NC
17	18	0	Head Select
19	20	I	Index
21	22	I	Ready
23	24	0	Step
25	26	0	Drive Select 1
27	28	0	Drive Select 2
29	30	0	Drive Select 3
31	32		NC
33	34	0	Direction In

WINCHESTER DRIVE DATA CONNECTOR J1-J3

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1		NC
4	3		NC
6	5		NC
8	7		NC
10	9		NC
11			GND
12			GND
	13	0	+MFM Write Data
	14	0	-MFM Write Data
15			GND
16			GND
	17	I	+MFM Read Data
	18	I	-MFM Read Data
19			GND
20			GND

POWER CONNECTOR J6

PIN	SIGNAL NAME
1	NC
2	GROUND
3	GROUND
4	+5V REGULALTED

COMMANDS

The WD1002-05 executes five macrocommands. Most commands feature automatic 'implied' seek, which means the Host system need not tell the WD1002-05 where the R/W heads of each drive are or when to move them. The controller automatically performs all needed retries on all errors encountered including data ECC errors. If the R/W head mispositions, the WD1002-05 automatically performs a restore and a re-seek. If the error is uncoverable, the WD1002-05 simulates a normal completion to simplify the Host system's software.

Commands are executed by loading the command byte into the Command Resister while the controller is not busy. (Controller is not busy if it has completed the previous command). The Task File must be loaded prior to issuing a command. On Write/Format operations, the Sector buffer must be filled with the required data before the command can be executed by the WD1002-05. On Winchester drives no command executes if the Seek Complete or Ready Signal are de-asserted or if the Write Fault signal is asserted. Normally it is not necessary to poll these signals before issuing a command. If the WD1002-05 receives a command that is not defined in the following table, undefined results occur.

For ease of discussion, commands are divided into three types:

TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Test	1	0	0	1	0	0	0	0
I	Restore	0	0	0	1	r3	r2	r1	r0
I	Seek	0	1	1	1	r3	r2	r1	r0
II	Read Sector	0	0	1	0	I	M	L	0
II	Write Sector	0	0	1	1	0	M	L	0
III	Format Track	0	1	0	1	0	0	0	0

r3 - r0 = STEPPING RATES

r3-r0	Winchester Disk Drives	Floppy Disk Drives
0000	~35 μs	~15 μs
0001	0.5 ms	1.0 ms
0010	1.0 ms	2.0 ms
0011	1.5 ms	3.0 ms
0100	2.0 ms	4.0 ms
0101	2.5 ms	5.0 ms
0110	3.0 ms	6.0 ms
0111	3.5 ms	8.0 ms
1000	4.0 ms	10 ms
1001	4.5 ms	12 ms
1010	5.0 ms	14 ms
1011	5.5 ms	16 ms
1100	6.0 ms	18 ms
1101	6.5 ms	20 ms
1110	7.0 ms	25 ms
1111	7.5 ms	40 ms

I = DMA Read Mode
I = 0, Programmed I/O Mode
I = 1, DMA Mode
L = Read/Write Long
L = 0, Normal R/W Transfer
L = 1, R/W ECC Bytes from Host
M = Multiple Sector
M = 0, Single Sector R/W
M = 1, Multiple Sector R/W

I, L, M FLAGS

The 'I' Flag allows the Interrupt line (INTRQ) to be activated when the data is available. The Data Request signal is always activated when the WD1002-05 either needs data (in the case of the Write commands) or has data available for the Host. If the 'I' Flag is not set, then the INTRQ is activated before the start of data transfer. If set, then INTRQ is set after the last byte of the last sector has been transferred to the Host.

The 'L' Flag allows the Host to Read the ECC bytes as data. The ECC generator is inhibited. This function may be used for diagnostic and performance purposes by allowing the Host to compute and check ECC operation. Since the floppy disk format does not allow ECC, the 'L' Flag is a "don't care" bit in this case.

The 'M' Flag allows multiple sectors to be transferred via one command. The Sector Count Register in the Task File is used to specify the number of sectors to be transferred from a track. Retries and ECC correction (if applicable) are performed on each sector.

TYPE I COMMANDS

These commands simply position the R/W heads of the selected drive or run Diagnostics, Restore and Seek Commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate.

Test

The Test Command is used to run internal diagnostics for checking WD1002-05 board function. It is mainly employed to isolate faults in the board logic. This command is always executed when $\overline{MR}$ is asserted. Any faults are reported as error codes.

Restore

The Restore Command is used to move the R/W heads to the Track 0 position. It is usually performed after a power-up operation. When restoring a Winchester drive, the specified stepping rate is not used; the actual Restore rate is handshaked with the Seek Complete. When Restoring a floppy drive, the R3-R0 rate is used when the rate is equal to or slower than 8 msec. On rates faster than 8 msec., the restore stepping rate defaults to 8 msec. On both floppy and Winchester, the rate is stored for subsequent implied Seeks for Read/Write Commands.

Seek

The Seek Command is used to position the Read/Write to a specified location. Since the Read and Write Commands feature implied Seek, this command is normally used to perform simultaneous (overlap Seek) operations on multiple drives. The specified stepping rate is used for Track to Track access time.

The desired location is loaded into the cylinder registers prior to issuing the command. On Winchester drive, the Write Fault, Seek Complete, and Ready lines must be true for the command to execute. The Seek Complete line is not checked after all stepping pulses have been issued. A Seek operation on a floppy drive will be performed regardless of the state of Write Protect on the Drive Interface.

TYPE II COMMANDS

This type of command is characterized by a transfer of a block of data from the WD1002-05 buffer to the Host. This command has an implicit stepping rate as set by the last Restore or Seek command.

Read Sector

The Read Sector Command is used to transfer a specified sector from any drive to the Host buffer. The stepping rate, specified in an earlier Restore or Seek command, is used to automatically perform a Seek prior to execution of the Read. After the Task File has been loaded with the desired parameter, the on-board Sector Buffer is filled with the data from the disk. The Host may then read this data by accessing the Sector Buffer repeatedly.

The option flags I, L, M are also available and work exactly as described in the I, L, M FLAG description.

Write Sector

The Write Sector Command is used to transfer a block of data from the on-board buffer to a specified sector. After the command is issued, the WD1002-05 generates a DRQ and the Host proceeds to fill the buffer. Once filled, the desired sector is searched for. This may include an implied Seek. After the ID field is found the Write Gate signal is activated and the data is MFM encoded and written serially to the selected drive. The Write Precompensation Register in the Task File specifies the starting cylinder on a Winchester drive where precomp is to be enabled. The WFC is configured with no precompensation when writing to the floppies. The user may cut the etch on WD2797 pin 1 so that precomp is always enabled or jumper it to pin 29 so that precomp is enabled for tracks greater than 43.

The option Flags 'L' and 'M' are also available and work exactly as described in the I, L, M FLAG description.

TYPE III COMMAND

Format Track

This command is used to format a drive prior to reading or writing it causes ID fields, gaps and all information to be written to a selected Track for initialization. The on-board Sector Buffer serves a different purpose for this command; it contains the Bad Block Flag and the physical numbers of the sectors to be recorded. Since the actual sector numbers are now taken from the buffer, unlimited Interleaving is allowed. The Sector Count Register in the Task File, normally used during a multiple sector R/W, now specifies the number of sectors to be formatted. The Format Track Command also features the implied Seek option, so that the entire drive can be formatted by incrementing the cylinder number after each execution.

SETTING UP TASK FILES

Before any of the five commands may be executed, a set of parameter registers called the Task File must be set up. For most commands, this informs the WD1002-05 of the exact location on the disk that the transfer should take place. For a normal read or write sector operation, the Sector Number, the Size/Drive/Head, Cylinder Number, and Command registers (usually in that order) are written.

Note that most of these registers can be read as well as written. These registers normally are not read from, but this feature is provided so that error reporting routines can determine physically where an error occurred without recalculating the sector, head and cylinder parameters.

Since the WD1002-05 can recall all the Task File parameters sent to it, it is recommended that Task File parameters be stored in the WD1002-05 as they are calculated. This saves the programmer a few instructions by not maintaining two copies of the same information.

REGISTER SELECTION ARRAY

CS	A2	A1	A0	RE	WE
1	X	X	X	Deselected	Deselected
0	0	0	0	Sector Buffer	Sector Buffer
0	0	0	1	Error Register	Write Precomp*
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High**	Cylinder High**
0	1	1	1	Size/Drive/Head	Size/Drive/Head
0	1	1	1	Status Register	Command Register

*Not used on Floppy

**When LSB = 1, permits 48 t.p.i. Floppy disk to be used on 96 t.p.i. Floppy disk system, for all commands used.

SDH REGISTER								
BIT	7	6	5	4	3	2	1	0
Function	Sec Ext	Sec Size		Drive Select		Head/ Drive Select		

BIT 7	SECTOR EXTENSION (WINCHESTER ONLY)
0	Selects CRC for data field
1	Selects ECC for data field

BIT 6	BIT 5	SECTOR SIZE
0	0	256 Bytes
0	1	515 Bytes
1	0	1024 Bytes
1	1	128 Bytes

BIT 4	BIT 3	DRIVE SELECTION
0	0	Winchester Drive Sel 1
0	1	Winchester Drive Sel 2
1	0	Winchester Drive Sel 3
1	1	Floppy Drive Sel

BIT 2	BIT 1	BIT0	WIN-CHESTER HEAD NR	FLOPPY DRIVE & HEAD NRS.
0	0	0	0	DR1 HD0
0	0	1	1	DR1 HD1
0	1	0	2	DR2 HD0
0	1	1	3	DR2 HD1
1	0	0	4	DR3 HD0
1	0	1	5	DR3 HD1
1	1	0	6	DR4 HD0
1	1	1	7	DR4 HD1

Since most hard disk drives contain more than one head per position, it is more efficient to step the R/W head assemblies of most disk drives by, cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessible by all the heads on a positioner before stepping to a new cylinder.

STATUS & ERROR REGISTERS

The Status Register is used to monitor command flow and to supply the Host with specific information about the drive. A bit called "Busy" (Bit 7) indicates that the WD1002-05 is executing a current command and register access is prohibited. This bit can be read at any time by the Host but all other bits are invalid when this status bit is set.

The Error Register is used to report different types of errors caused by execution of the last command. To ease programming, the LSB of the Status Register is set if any of the bits in the Error Register are also set.

STATUS REGISTER BITS

BIT	STATUS REGISTER
7	Busy
6	Ready
5	Write Fault
4	Seek Complete
3	Data Request
2	Corrected Date
1	—
0	Error

ERROR REGISTER BITS

Bit	Normal Operation Status Reg. Bit 0 = 1	Diagnostic Operation Status Reg. Bit 0 = 0
7	Bad Block Detect	
6	Uncorrectable Error	
5	CRC Error ID Field	WD1015 Error
4	ID Not Found	WD1014 Error
3	-	Sector Buffer Error
2	Aborted Command	WD1010 Error
1	TK000 Error	WD2797 Error
0	DAM not found	Pass WD1002 is Functional

SPECIFICATIONS:

	HARD DISK	FLOPPY DISK
Encoding method:	MFM	MFM
Cylinders per Head:	Up to 1024	Up to 245
Sectors per Track:	Up to 64	Up to 64
Heads:	8	2
Drive Selects:	3 (ST506)	4 (SA450)
Step Rate:	35 usec. to 7.5 msec. (0.5 msec. increments)	0-40 msec. (1 of 16 rates in this range)
Data Transfer Rate:	5.0 Mbits/sec	250 Kbits/sec
Write Precomp Time:	12 nsec	100-300 nsec adj.

Sectoring:	Soft
Host Interface:	8-Bit bi-directional bus
Drive Cable Length:	10 ft (3M) max.
Host Cable Length:	3 ft (1M) max.
Power Requirements:	+5V ±5%, 3.0A Max.
Ambient Operating Temperature	0°C to 50° C (32° F to 122° F)
Relative Humidity:	20% to 80%
Air Flow	100 linear ft. per minute at .5" from component surface
MTBF:	10,000 POH
MTTR:	30 minutes
Length:	8.00 in
Width:	5.75 in
Height:	0.75 in
Mounting Centers:	7.50 X 5.250 in

WD1002-HDO Winchester Controller

FEATURES

- CONTROL FOR UP TO 3 WINCHESTER DRIVES
- ON BOARD DATA SEPARATOR AND WRITE PRECOMPENSATION
- 128, 256, 512, AND 1024 BYTE SECTOR SIZES
- PROGRAMMABLE SECTOR SIZES TO 1K
- AUTOMATIC TRACK FORMATTING ON HARD DISKS
- MULTIPLE SECTOR OPERATIONS
- 5-BIT SINGLE BURST ERROR CORRECTION ON WINCHESTER
- CRC GENERATION/VERIFICATION ON ID FIELDS
- 5-MBIT DATA TRANSFER RATE
- ECC DIAGNOSTIC COMMANDS (READ LONG & WRITE LONG)
- SINGLE +5V POWER SUPPLY

DESCRIPTION

The WD1002-HDO Winchester Controller is a stand-alone general purpose board designed to interface up to three 5 1 / 4" Winchester hard disks. The Winchester Controller implements all the logic required for a variable length sector (to 1K bytes). ECC correction, data separation and Host interface circuitry. The Winchester interface is based on the Seagate ST506. All necessary buffers and drivers / receivers are on board.

Communication to and from the Host is made via a separate computer access port. This port consists mainly of an 8-bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro commands are transferred via this 8-bit bus. An on-board Sector Buffer allows data transfers to the Host computer at a rate independent of the drive transfer rate.

The WD1002-HDO Controller board is based on the WD1014 EDS device and WD1015 Buffer Controller device, as well as the WD1010 Winchester Disk Controller chips. It is form factor compatible with most 5 1 / 4" Winchesters and may be directly mounted on the drive.

ARCHITECTURE

The Block Diagram of the WD1002-HDO is shown in Figure 1. The heart of the system is the WD1015 Buffer / Controller, which generates and processes all data and control lines, along with the WD1014 EDS that generates all control signals that cannot be handled in real time by the WD1015.

Commands, parameters, and data are entered via the Host Interface Logic. Data is read from the selected drive and transferred to the Sector Buffer. If an error in the data field has been encountered, the WD1015 instructs the controller to perform retries automatically.

On a Winchester drive, the WD1014 ECC device is enabled and error correction procedures invoked. Error Correction may be disabled via software from the Host to allow CRC-only formatted Winchester drives to be used in the system. The WD1002-HDO provides Data Separation and Write Precompensation Logic for data transfers. After the Sector Buffer is full, the WD1015 informs the Host Interface Logic that data may be read by the Host. The use of an on-board Sector Buffer provides both transparent error correction and data transfers to the Host that are independent of drive transfer rates.

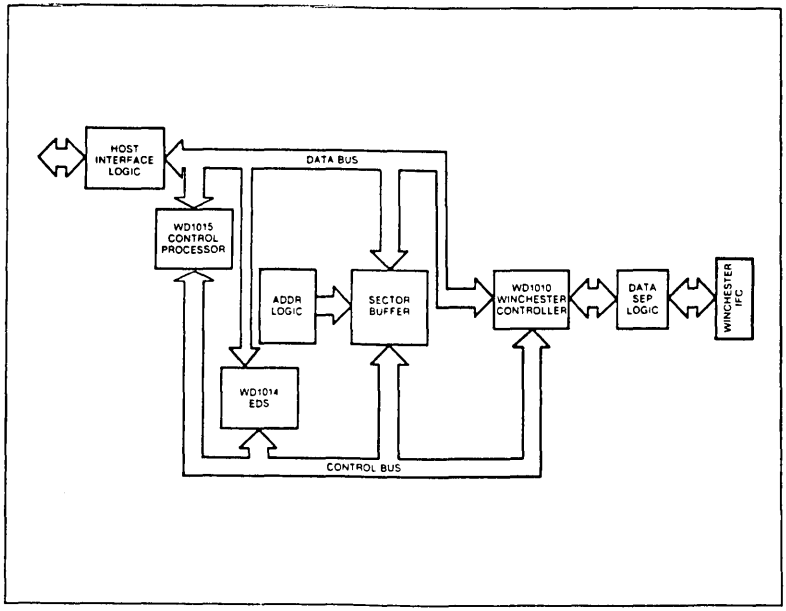


FIGURE 1. WD1002-HDO BLOCK DIAGRAM

HOST INTERFACE

The WD 1002-HDO is designed to interface to a Host processor via a parallel port or CPU bus configurations. The specific signals are compatible with the Western Digital WD1000/WD1001 series of Winchester-only controller boards. With the inclusion of the WD1015, the previous WAIT signal is no longer necessary but has been provided for compatibility; status information is always available to the Host for monitoring command progress. When the Busy bit is set, no other status bits are valid.

The Host interface connector (J5) consists of an 8-bit bi-directional bus, three address lines, and read and write signals. All functions within the WD1002-HDO are initiated by the Host interface.

HOST INTERFACE CONNECTOR J5

SIG. PIN	SIG. GND.	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1 3 5 7 9 11 13 15	2 4 6 8 10 12 14 16	DAL 0 thru DAL 7	DATA ACCESS LINE 0 thru DATA ACCESS LINE 7	I/O	8-bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the CS line is de-asserted
17 19 21	18 20 22	A0 A1 A2	ADDRESS 0 ADDRESS 1 ADDRESS 2	I	These three Address Lines are used to select one of nine registers in the Task File or the Sector Buffer. They must remain stable during all read and write operations.
23	24	$\overline{CS}$	$\overline{CARD\ SELECT}$	I	When $\overline{Card\ Select}$ is active along with $\overline{RE}$ or $\overline{WE}$, data is read or written via the DAL bus. $\overline{CS}$ must make a transition for each byte read or written to the Task File.
25	26	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	I	When $\overline{Write\ Enable}$ is active along with $\overline{CS}$, the Host may read data to a selected register of the WD1002-HDO.
27	28	$\overline{RE}$	$\overline{READ\ ENABLE}$	I	When $\overline{Read\ Enable}$ is active along with $\overline{CS}$, the Host may read data from a selected register of the WD1002-HDO.
29	30	Pull-up (PUP)			Used only when replacing WD1000 or WD1001 with WD1002-HDO. Tied to a pull-up register.
31	32	NOT CONNECTED			
33	34	NOT CONNECTED			
35	36	INTRQ	INTERRUPT REQUEST	O	The Interrupt Request Line is asserted whenever a command has been completed. It is de-asserted when the Status Register is read, or a new command is loaded via the DAL lines.
37	38	DRQ	DATA REQUEST	O	The Data Request line is asserted whenever the Sector Buffer contains data to be read by the Host, or is awaiting data to be loaded by the Host. This line is de-asserted whenever the buffer has been exhausted or filled by the Host.
39	40	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	The $\overline{Master\ Reset}$ line initializes all internal logic on the WD1002-HDO Sector Number, Cylinder Number and SDH are cleared, stepping rate for Winchester devices are set to 7.5 msec, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ INTRQ signals are de-asserted.
Note: Grounds					All even numbered pins (2 through 40) are to be used as signal grounds. Power ground is available on J6, pin 1.

DRIVE CONNECTORS

Five connectors are provided for connection of up to three Winchester drives. All applicable drivers and receivers have been included on the board to allow direct connections to the drives.

The Winchester control cable is daisy-chained and requires termination resistors on the last drive. Most Winchester drives can be configured to provide this. The data cables are radially connected to each drive. Three data cable connectors are included on the board.

34-PIN WINCHESTER DRIVE CONTROL CONNECTOR J7

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	RWC
3	4	O	Head Select 2
5	6	O	Write Gate
7	8	I	Seek Complete
9	10	I	TRACK 000
11	12	I	Write Fault
13	14	O	Head Select 0
15	16		NC
17	18	O	Head Select 1
19	20	I	Index
21	22	I	Ready
23	24	O	Step
25	26	O	Drive Select 1
27	28	O	Drive Select 2
29	30	O	Drive Select 3
31	32		NC
33	34	O	Direction In.

WINCHESTER DRIVE DATA CONNECTIONS AND DESCRIPTIONS J1-J3

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1		NC
4	3		NC
6	5		NC
8	7		NC
10	9		NC
11			GND
12			GND
	13	O	+MFM Write Data
	14	O	-MFM Write Data
15			GND
16			GND
	17	I	+MFM Read Data
	18	I	-MFM Read Data
19			GND
20			GND

POWER CONNECTOR

A four pin AMP connector is used for power input to the WD1002-HDO. The pin-outs are as shown:

POWER CONNECTOR J6

PIN	SIGNAL NAME
1	NC
2	GROUND
3	GROUND
4	+5V REGULATED

COMMANDS

The WD1002-HDO executes five macro commands. Most commands feature automatic 'implied' seek, which means the Host system need not tell the WD1002-HDO where to R/W heads of each drive are or when to move them. The controller automatically performs all needed retries on all errors encountered including data ECC errors. If the R/W head mispositions, the WD1002-HDO automatically performs a restore and re-seek. If the error is unrecoverable, the WD1002-HDO simulates a normal completion to simplify the Host system's software.

Commands are executed by loading the command byte into the Command Register while the controller is not busy. (Controller is not busy if it has completed the previous command). The Task File must be loaded prior to issuing a command. On Write/Format operations, the Sector Buffer must be filled with the required data before the command can be executed by the WD1002-HDO. On Winchester drives no command executes if the Seek Complete or Ready signals are de-asserted or if the Write Fault signal is asserted. Normally, it is not necessary to poll these signals before issuing a command. If the WD1002-HDO receives a command that is not defined in the following table, undefined results occur.

The Restore Command is used to move the R/W heads to the Track 0 position. It is usually performed after a power-up operation. The Restore Command does not use the specified stepping rate, instead the rate is determined by two handshakes with the Seek Complete signal. The specified rate is stored for use by the Read and Write Commands.

For ease of discussion, commands are divided into three types:

TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Test	1	0	0	1	0	0	0	0
I	Restore	0	0	0	1	r3	r2	r1	r0
I	Seek	0	1	1	1	r3	r2	r1	r0
II	Read Sector	0	0	1	0	I	M	L	0
III	Write Sector	0	0	1	1	0	M	L	0
III	Format Track	0	1	0	1	0	0	0	0

r3-r0 = STEPPING RATES

r3-r0	Winchester Disk Drives
0000	~35 μsec
0001	0.5 msec
0010	1.0 msec
0011	1.5 msec
0100	2.0 msec
0101	2.5 msec
0110	3.0 msec
0111	3.5 msec
1000	4.0 msec
1001	4.5 msec
1010	5.0 msec
1011	5.5 msec
1100	6.0 msec
1101	6.5 msec
1110	7.0 msec
1111	7.5 msec

I = DMA Read Mode

I = 0, Programmed I / O Mode
I = 1, DMA Mode

L = Read / Write Long

L = 0, Normal R / W Transfer
L = 1, R / W ECC Bytes from Host

M = Multiple Sector

M = 0, Single Sector R / W
M = 1, Multiple Sector R / W

TYPE I COMMANDS

These commands simply position the R / W heads of the selected drive or run Diagnostics. Restore and Seek Commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate.

Test

Bit code: 1 0 0 1 0 0 0 0

The Test Command is used to run internal diagnostics for checking WD1002-HDO board function. It is mainly employed to isolate faults in the board logic. This command is always executed when MR is asserted. Any faults are reported as error codes.

Restore

The Restore Command is used to move the R/W heads to the Track 0 position. It is usually performed after a power-up operation. The Restore Command does not use the specified stepping rate, instead the rate is determined by two handshakes with the Seek Complete signal. The specified rate is stored for use by the Read and Write Commands.

Seek

The Seek Command is used to position the Read/Write to a specified location. Since the Read and Write Commands feature implied Seek, this command is normally used to perform simultaneous (overlap Seek) operations on multiple drives. The specified stepping rate is used for Track to Track access time.

The desired location is loaded into the cylinder registers prior to issuing the command. On Winchester drive, the Write Fault, Seek Complete, and Ready lines must be true for the command to execute. The Seek Complete line is not checked after all stepping pulses have been issued.

TYPE II COMMAND

This type of command is characterized by a transfer of a block of data from the WD1002-HDO buffer to the Host. This command has an implicit stepping rate as set by the last Restore or Seek command.

Read Sector

The Read Sector Command is used to transfer a specified sector from any drive to the Host buffer. The stepping rate, specified in an earlier Restore or Seek command, is used to automatically perform a Seek prior to execution of the Read. After the Task File has been loaded with the desired parameter, the on-board Sector Buffer is filled with the data from the disk. The Host may then read this data by accessing the Sector Buffer repeatedly.

Sector Buffer

The 'I' Flag allows the Interrupt line (INTRQ) to be activated when the data is available. The Data Request signal is always activated when the WD1002-HDO either needs data (in the case of the Write commands) or has data available for the Host. If the 'I' Flag is not set, then the INTRQ is activated before the start of data transfer. If set, then INTRQ is set after the last byte of the last sector has been transferred to the Host.

The 'L' Flag allows the Host to Read the ECC bytes as data. The ECC generator is inhibited. This function may be used for diagnostic and performance purposes by allowing the Host to compute and check ECC operation.

The 'M' Flag allows multiple sectors to be transferred via one command. The Sector Count Register in the Task File is used to specify the number of sectors to be transferred from a track. Retries and ECC correction (if applicable) are performed on each sector.

TYPE III COMMANDS

Write Sector

The Write Sector Command is used to transfer a block of data from the on-board buffer to a specified sector. After the command is issued, the WD1002-HDO generates a DRQ and the Host proceeds to fill the buffer. Once filled, the desired sector is searched for. This may include an implied Seek. After the ID field is found, the Write Gate signal is activated and the data is MFM encoded and written serially to the selected drive. The Write Precompensation Register in the Task File specifies the starting cylinder on a Winchester drive where precomp is to be enabled.

The option Flags 'L' and 'M' are also available and work exactly as described in the Read Sector command.

Format Track

This command is used to format a drive prior to reading or writing. It causes ID fields, gaps, and all information to be written to a selected Track for initialization. The on-board Sector Buffer serves a different purpose for this command; it contains the Bad Track Flag and the physical numbers of the sectors to be recorded. Since the actual sector numbers are now taken from the buffer, unlimited Interleaving is allowed. The Sector Count Register in the Task File, normally used during a multiple sector R/W, now specifies the number of sectors to be formatted. The Format Track Command also features the implied Seek option, so that the entire drive can be formatted by incrementing the cylinder number after each execution.

SETTING UP TASK FILES

Before any of the five commands may be executed, a set of parameter registers called the Task File must be set up. For most commands, this informs the WD1002-HDO of the exact location on the disk that the transfer should take place. For a normal read or write sector operation, the Sector Number, the Size/Drive/Head, Cylinder Number, and Command registers (usually in that order) are written.

Note that most of these registers can be read as well as written. These registers normally are not read from, but this feature is provided so that error reporting routines can determine physically where an error occurred without recalculating the sector, head and cylinder parameters.

Since the WD1002-HDO can recall all the Task File parameters sent to it, it is recommended that Task File parameters be stored in the WD1002-HDO as they are calculated. This saves the programmer a few instructions by not maintaining two copies of the same information.

REGISTER SELECTION ARRAY

CS	A2	A1	A0	RE	WE
1	x	x	x	De-selected	De-selected
0	0	0	0	Sector Buffer	Sector Buffer
0	0	0	1	Error Register	Write Precomp
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High	Cylinder High
0	1	1	0	Size/Drive/Head	Size/Drive/Head
0	1	1	1	Status Register	Command Register

SDH REGISTER								
BIT	7		6	5	4	3	2 1	0
Function	Sec Ext		Sec Size		Drive Select		Head Select	

BIT 7	SECTOR EXTENSION
0	Selects CRC for data field
1	Selects ECC for data field

BIT 6	BIT 5	SECTOR SIZE
0	0	256 Bytes
0	1	512 Bytes
1	0	1024 Bytes
1	1	128 Bytes

BIT 4	BIT 3	DRIVE SELECTED
0	0	Winchester Drive Sel 1
0	1	Winchester Drive Sel 2
1	0	Winchester Drive Sel 3
1	1	

BIT 2	BIT 1	BIT 0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Since most hard disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessible by all the heads on a positioner before stepping to a new cylinder.

STATUS & ERROR REGISTERS

The Status Register is used to monitor command flow and to supply the Host with specific information about the drive. "Busy" (Bit 7) indicates that the WD1002-HDO is executing a current command and register access is prohibited. This bit can be read at any time by the Host but all other bits are invalid when this status bit is set.

The Error Register is used to report different types of errors caused by execution of the last command. To ease programming, the LSB of the STATUS Register is set if any of the bits in the Error Register are also set.

STATUS REGISTER BITS

BIT	STATUS REGISTER
7	Busy
6	Ready
5	Write Fault
4	Seek Complete
3	Data Request
2	Corrected Data
1	–
0	Error

ERROR REGISTER BITS

Bit	Normal Operation Status Reg.Bit 0 = 1	Diagnostic Operation Status Reg.Bit 0 = 0
7	Bad Block Detect	
6	Uncorrectable Error	
5	CRC Error ID Field	WD1015 Error
4	ID Not Found	WD1014 Error
3	–	Sector Buffer Error
2	Aborted Command	WD1010 Error
1	TK000 Error	
0	DAM not found	Pass WD1002 is Functional

SPECIFICATIONS:

	HARD DISK
Encoding method:	MFM
Cylinders per Head:	Up to 1024
Sectors per Track:	Up to 64
Heads:	8
Drive Selects:	3 (ST506)
Step Rate:	35 μsec to 7.5 msec. (0.5 msec. increments)
Data Transfer Rate:	5.0 Mbits / sec
Write Precomp Time:	12 nsec
Sectoring:	Soft
Host Interface:	8-bit bi-directional bus
Drive Cable Length:	10 ft (3M) max.
Host Cable Length:	3 ft (1M) max.
Power Requirements:	+5V 5%, 3.0A Max.
Ambient Operating Temperature:	0°C to 50°C (32°F to 122°F)
Relative Humidity:	20% to 80%
Air Flow:	100 linear ft per minute at .5" from component surface.
MTBF:	10,000 POH
MTTR:	30 minutes
Length:	8.00 in
Width:	5.75 in
Height:	0.75 in
Mounting Centers:	7.50 X 5.250 in

WD1002-SHD Winchester Disk Controller

FEATURES

- SINGLE + 5V SUPPLY
- SASI™ HOST INTERFACE
- CONTROL FOR UP TO 2 WINCHESTER DRIVES, UP TO 8 R/W HEADS EACH
- 32-BIT ECC FOR WINCHESTER DATA CORRECTION
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- BAD TRACK MAPPING CAPABILITY
- AUTOMATIC FORMATTING
- 256 OR 512 BYTES PER SECOND
- SELECTABLE INTERLEAVE
- MULTIPLE SECTOR READS AND WRITES
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- IMPLIED SEEKS
- OVERLAPPED SEEKS

DESCRIPTION

The WD1002-SHD is a stand alone, general purpose Winchester Controller Board designed to interface up to two Winchester Disk Drives to a Host Processor. The Winchester Drive signals are based upon the Floppy look-alike interface available on the Seagate Technology ST506 and other compatible drives. All necessary receivers and drivers are included on the board to allow direct connection to the drive.

Communications to and from the Host Computer are made via a separate computer access port. This port conforms to the popular Shugart Associates System Interface (SASI). It consists of control signals and an 8-bit, bi-directional bus. All data to be written to or read from the disk, status information, and command parameters are transferred via this bus. An on-board Sector Buffer allows bus transfers to be executed independently of the actual data transfer of the drive.

The WD1002-SHD is based upon the WD1015-02, WD1010, and WD1100-13, specifically designed for Winchester disk drive control.

SASI ™ is a trademark of Shugart Assoc.

ARCHITECTURE

The WD1002-SHD has five on-board interface connectors. Other connectors are for test only and should not be used.

The five connectors consist of a Power Connector, Host Interface Connector, Winchester Drive Control Connector and two Winchester Data Cable Connectors.

The Winchester Drive Control Cable is daisy-chained to the drive. The Drive Data Connectors carry differential signals and are radially connected.

The Host Interface Connector provides a path to the Host thru a SASI Bus. Other SASI-compatible controllers may also be connected to the same bus.

SPECIFICATIONS:

DRIVE INTERFACES

Encoding Method	MFM
Cylinders per Drive	Programmable
Bytes per Sector	Selectable, 256 or 512
Sectors per Track	32 (256 bytes/sector) 17 (512 bytes/sector)
Head Selects	8
Drive Selects	2
Stepping Rates/Algorithms	Programmable
Data Transfer Rate	5 Mbits/sec
Write Precomp Time	12 nsec
Sectoring	Soft
Max Cable Length	
Control (Total Daisy Chain)	6M (20ft.)
Data (Radial - each)	6M (20ft.)

HOST INTERFACE

Type	SASI
Max Cable Length (Total Daisy Chain)	4.5M (15 ft.)
Termination	Socketed 220/330 pack
Addressing	Jumperable, 0 to 7 (factory default = 0)

POWER

Voltage	5V + 5%
Current	2.0A Max, 1.5A TYP
Ripple	0.1 volts max, 0.1 to 25 MHz

MECHANICAL

Length	8.0 inches
Width	5.75 inches
Height (Max incl leads, board, & components	0.75 inches

ENVIRONMENTAL - OPERATING

Ambient Temperature	0°C (32°F) to 55°C (131°F)
Relaltive Humidity	10% to 90% non-condensing
Altitude	0 to 3000M (10,000ft.)

CONNECTORS

MECHANICAL INFORMATION

Table 1 defines the connectors and a source for the mating connectors on the associated cables.

Table 1. CONNECTORS

REFERENCE DESIGNATION	INTERFACE FUNCTION	EQUIVALENT MATING CONNECTOR
P1	Power	AMP1-480424-0 (Housing) AMP350078-4 (Pins)
P2	SASI Bus	AMP88379-8
J1	Winchester Control (Daisy-Chain)	AMP88373-3
J2,J3	Winchester Data (Radial)	AMP88377-4
J4	Test - do not use	

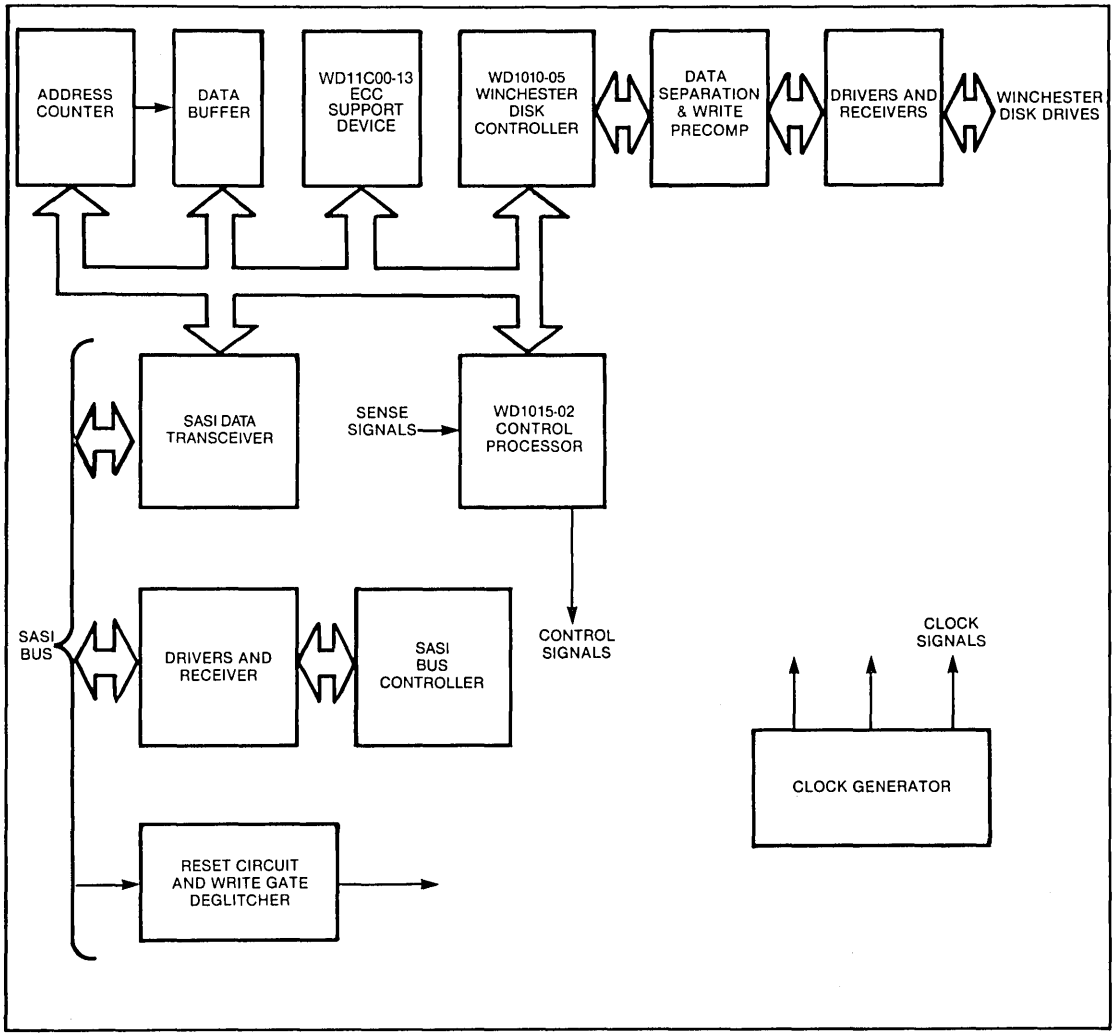


Figure 1. WD1002-SHD BLOCK DIAGRAM

HOST INTERFACING

The WD1002-SHD Controller has been designed to interface to the Shugart Associates System Interface (SASI) bus. All interfacing is done through the SASI connector (P2). Up to eight SASI compatible devices (including the Host) may be connected to this bus. The cable terminating resistor pack is socketed on the last controller in the daisy-chain to aid flexibility in daisy-chaining bus devices.

The controller is shipped from the factory configured to respond to SASI device address 0. This may be changed by the user to any SASI address (0 through 7).

HOST INTERFACE CONNECTOR

The host interface connector is a 50 pin vertical header. The connector pin-outs are as follows:

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
1	2	$\overline{\text{DATA 0}}$ (LSB)	Bi-directional bytewide bus bits $\overline{\text{D0-D7}}$.
3	4	$\overline{\text{DATA 1}}$	
5	6	$\overline{\text{DATA 2}}$	
7	8	$\overline{\text{DATA 3}}$	
9	10	$\overline{\text{DATA 4}}$	
11	12	$\overline{\text{DATA 5}}$	
13	14	$\overline{\text{DATA 6}}$	
15	16	DATA 7 (MSB)	
17	18	SPARE	
19	20	SPARE	
21	22	SPARE	
23	24	SPARE	
25	26	SPARE	
27	28	SPARE	
29	30	SPARE	
31	32	SPARE	
33	34	SPARE	
35	36	BUSY	Controller-to-host signal whose falling edge acknowledges receipt of $\overline{\text{SEL}}$ and own address. Rising edge indicates transaction complete.
37	38	$\overline{\text{ACK}}$	Host-to controller handshake for byte transfers (both edges used).
39	40	$\overline{\text{RST}}$	100 nsec low level initiate host-to controller.
41	42	$\overline{\text{MSG}}$	Controller-to-host $\overline{\text{MESSAGE}}$ signal to indicate type of bus transfer (see INFORMATION TRANSFER PHASE).
43	44	$\overline{\text{SEL}}$	Host-to-controller low level signal gives control of bus to the addressed target.
45	46	$\overline{\text{C/D}}$	Controller-to-host $\overline{\text{COMMAND}}$/DATA signal used to indicate type of bus transfer (see INFORMATION TRANSFER PHASE).
47	48	$\overline{\text{REQ}}$	Controller-to-host handshake for byte transfers (both edges used).
49	50	$\overline{\text{I/O}}$	0 = Input to host. 1 = Output from host. (see INFOMATION TRANSFER PHASE)

WINCHESTER DRIVE CONTROL CONNECTOR

The drive control connector is a 34-pin PC card edge connector that provides a low speed bus that is daisy chained to each of the Winchster drives in the system. To properly terminate the open collector outputs from the WD1002-SHD, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. No other drives should have this termination. The drive control signals and pinouts are as follows:

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME I/O	DESCRIPTION
1	2	RWC (O)	When the Reduce Write Current (RWC) line is activated by Write Gate (WG), a lower write current is used to compensate for a greater bit packing density on the inner cylinders. RWC is only valid when WG is low.
3	4	HS2 (O)	Head Select lines are used by the WD1002-SHD to select a specific R/W head on the drive.
13	14	HS0 (O)	
17	18	HS1 (O)	
5	6	WG (O)	Write Gate (WG) enables data to be written on the disk. Special circuitry has been included to ensure that this signal will not "glitch" at power-on. This enables the disk drive to remain powered while the WD1002-SHD power is being cycled.
7	8	SC (I)	Seek Complete (SC) informs the WD1002-SHD that the head of a selected drive has stabilized.
9	10	TR000 (I)	Track 000 (TR000) indicates that the R/W heads are positioned on the outermost cylinder.
11	12	WF (I)	Write Fault (WF) informs the WD1002-SHD that some fault has been detected by the selected drive.
15	16		NC
19	20	IND (I)	Index (IND) indicates the index point for synchronization during formatting. IND is also used as a time-out mechanism for retries. IND should pulse once for each disk rotation.
21	22	RDY (I)	Ready (RDY) informs the WD1002-SHD that the desired drive is selected and its motor is up to speed.
23	24	STEP (O)	STEP is pulsed for each desired step. The direction of the step is determined by the DIRIN line.
25	26	DS0	The Drive Select bits (DS0-DS1) are used to select either drive 1 or drive 2.
27	28	DS1	
29	30		NC
31	32		NC
33	34	DIRIN	Direction in (DIRIN) determines the direction of movement of the R/W heads when STEP is pulsed: DIRIN = 1 = direction out DIRIN = 0 = direction in

WINCHESTER DRIVE DATA CONNECTOR

Two data connectors are provided for data transfer between the controller and each drive. All lines associated with the transfer of data between the drive and the controller are differential in nature and may not be multiplexed. The data connectors are 20-pin vertical headers on tenth-inch centers. The cable pinouts are as follows:

SIGNAL GROUND	SIGNAL PIN	(I/O)	SIGNAL NAME
2	1	I	Drive Selected
4	3	-	NC
6	5	-	NC
8	7	-	NC
10	9	-	NC
12	11	-	GND
	13	O	+MFM Write Data
	14	O	-MFM Write Data
16	15	-	GND
	17	I	+MFM READ DATA
	18	I	-MFM READ DATA
20	19	-	GND

POWER CONNECTOR

A four pin AMP connector is provided for power input to the board. The pinouts are as follows:

PIN	SIGNAL
1	NC
2	GROUND
36	GROUND
4	+5V regulated

HOST INTERFACE DETAILED BUS OPERATION

With regard to bus operations, time can be partitioned into the following mutually exclusive phases:

1. Reset
2. Bus Free
3. Target Selection
4. Information Transfer
5. Bus Release

Bus Phase Sequencing

A Reset Phase may occur at any time. It is followed by the Bus Free Phase. In the absence of a Reset Phase, the bus alternates between the Bus Free Phase and one Transaction.

A Transaction always consists of the following sequence:

1. one Target Selection Phase
2. one or more Information Transfer Phases
3. one Bus Release Phase

The five bus phases are described below. The Information Transfer Phase is broken down into its mutually exclusive categories, which are also called phases.

1. RESET PHASE

Defined as the time $\overline{\text{RESET}}$ is low. It is used by a Host to force the controller(s) on the bus to the same state as that following a power on condition. Power-on-Reset is 110msec. Master Reset from Host is 100μsec.

2. BUS FREE PHASE

Defined as the time between the Reset Phase or completion (Bus Release Phase) of one Transaction and initiation (Target Selection Phase) of the next Transaction. It can also be thought of as the time during which no unit has control of the bus. All eight control lines are high. The Data Lines are in an undefined state.

3. TARGET SELECTION PHASE

This phase begins when the host places a target address on the bus. The Host then brings $\overline{\text{SEL}}$ low. The phase ends when the target corresponding to that address responds by bringing $\overline{\text{BUSY}}$ low. Note: the Host must bring $\overline{\text{SEL}}$ high before completion of the current Transaction (end of next Bus Release Phase).

The target address consists of one of $\overline{\text{D0}}$ through $\overline{\text{D7}}$ low and the other seven high. The controller's default address corresponds to $\overline{\text{D0}}$ low. It may be changed to any address by jumpering. Two controllers may not have the same address.

4. INFORMATION TRANSFER PHASE

This phase is used to transfer one or more bytes over the bus. It begins when the currently selected controller sets $\overline{\text{I/O}}$, $\overline{\text{C/D}}$, and $\overline{\text{MSG}}$ to one of the five legal combinations in the following table. This indicates to the Host the type of byte transfer(s) which will follow.

$\overline{\text{I/O}}$	$\overline{\text{C/D}}$	$\overline{\text{MSG}}$	TYPE OF TRANSFER PHASE	NUMBER OF BYTES
1	0	1	Command Block (from Host)	6
1	1	1	Data Block (from Host)	3, 8, 256, 260, 512 or 516
0	1	1	Data Block (to Host)	1, 4, 256, 260, 512 or 516
0	0	1	Status Byte (to Host)	1
0	0	0	Message Byte (to Host)	1

For each byte transferred, the following operations must occur in sequence to perform the asynchronous handshake.

1. The controller brings REQ low
2. The host brings ACK low
3. The controller brings REQ high
4. The host brings ACK high

For controller to host transfers, the eight bits are valid on the bus at least 125 nsec before REQ goes low. For host to controller transfers, they must be valid on the bus no later than 375 nsec after ACK goes low. Note: for debugging, it is useful to know that bytes are valid on the bus at the rising edge of REQ during any transfer.

The Command Block Transfer Phase is used to send a block of parameters to the controller. This block specifies the operation to be performed (e.g. Format Disk).

The Data Transfer Phase is primarily used to send one or more sectors of data (with or without ECC) in either direction. It is also used to send an extra block of parameters to the controller or to send byte(s) of controller operational information to the host.

During the Status Transfer Phase, a byte is sent to the Host. They are encoded to indicate whether an error has been detected, and if so, which drive.

During the Message Byte Transfer Phase, one byte of all zeroes is sent to the host. This is necessary to satisfy the protocol.

BUS RELEASE PHASE

This phase is simply the low-to-high transition of BUSY. This event signifies to the host that the current Transaction has terminated and the associated target is no longer controlling the bus.

SUMMARY

Now in more detail, a transaction always consists of the following sequence:

a. One Target Selection Phase
b. One Command Block Transfer Phase
c. Zero or more Data Block Transfer Phase(s) (type and number determined by the preceding Command Block parameters)
d. One Status Byte Transfer Phase
e. One Message Byte Transfer Phase
f. One Bus Release Phase

During a transaction, all Data Block Transfer Phases are in the same direction and of the same size.

COMMAND BLOCKS

A transaction is initiated by the host to instruct the controller to execute a command. During the Command Block Transfer Phase, six bytes of information specifying the command are transferred to the controller. There is a specific fomat for these bytes, shown in figure below.

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	Command Class			OP Code				
1	Logical Unit Number			Logical Sector Address (high)				
2	Logical Sector Address (Middle)							
3	Logical Sector Address (Low)							
4	Interleave or Block Count							
5	Control Byte							

Byte 0 is transferred first. Byte 0 must be specified for all commands. Each command has exactly one Byte 0 value associated with it.

Depending on the value of Byte 0, each parameter in Bytes 1 through 5 may require specification. Table 2 specifies the supported commands and their parameters. It also includes information in data transfers required during execution. All other commands are reserved.

LOGICAL UNIT NUMBER (LUN)

This is contained in the upper three bits of Byte 1. The allowed values are 0,1. The designators in the Command Table are:

Drive 0 (LUN 0) or 1 (LUN 1)

LOGICAL SECTOR ADDRESS (L)

This is a 21-bit field contained in Bytes 1, 2, and 3. It is computed from the Cylinder address (C), Head address (H), and Sector address (S), as well as the drive parameters, heads per drive (HD) and Sectors per track (ST):

$$L = (((C*Hd) + H) * ST) + S$$

C,H, and S can be derived from L, HD, and ST as follows:

$$S = L \text{Modulo } ST$$
$$H = ((L-S)/ST) \text{ Modulo } HD$$
$$C = (((L-S)/ST)-H)/HD$$

This field specifies a sector (or a beginning sector) for the Read and Write Drive commands. It specifies a track for the Format and Seek commands (marked with a * in the table). When only a track specification is required, the sector number implied by the Logical Sector Address is ignored.

INTERLEAVE OR BLOCK COUNT

This field makes up Byte 4. The Interleave Ratio (I) is specified in the Five Format commands. The maximum ratio is the sectors-per-track minus 1.

The Block Count (B) is specified in the Read, Write, Read Long, and Write Long commands. It specifies the number of Logical Sectors to be transferred.

Both Interleave Ratio and Block Count use all 8-bits to specify the parameters.

Table 2. WD1002-SHD SUPPORTED COMMAND SUMMARY

COMMAND NAME	CLASS + OP CODE	LUN	LOGICAL SECTOR ADDRESS	INTER-LEAVE OR BLOCK COUNT	CON-TROL BYTE OPTIONS	# OF SASI DATA BLOCK TRANSFERS	DATA BLOCK SIZE	DIRECTION
Test Drive Ready	0,0	W	-	-	-	0	-	-
Restore to track 0	0,1	W	-	-		0	-	-
Request Status	0,3	W	-	-	-	1	4	To Host
Format Drive	0,4	W	L*	I	R,P,S	0	-	-
Check Track Format	0,5	W	L*	I	R,S	0	-	-
Format Track	0,6	W	L*	I	R,P,S	0	-	-
Format Bad Track	0,7	W	L*	I	R,P,S	0	-	-
Read Drive	0,8	W	L	B	R,A,S	B	Sector	To Host
Write Drive	0,A	W	L	B	R,S	B	Sector	To CTLR
Seek	0,B	W	L*	-	R,S	0	-	-
Winchester Parameters	0,C	W	-	-	-	1	8	To CTLR
Return Burst Error Length	0,D	W	-	-	-	1	1	To Host
Format Alternate Track	0,E	W	L*	I	R,P,S	1	3	To CTLR
Write Sector Buffer	0,F	-	-	-	-	1	- Sector	To CTLR
Read Sector Buffer	0,10	-	-	-	-	1	- Sector	To Host
Perform RAM Diagnostics	7,0	-	-	-	-	0	-	-
Perform Drive Diagnostics	7,3	W	-	-	R,S	0	-	-
Perform Controller Diagnostics	7,4	-	-	-	-	0	-	-
Read Drive Long	7,5	W	L	B	R,S	B	- Sector +4	To Host
Write Drive Long	7,6	W	L	B	R,S	B	- Sector +4	To CTLR

LEGEND

W Winchester
L* Logical sector Address used only to specify track
I Interleave
B Block count
R Retry enable/disable
A Attempt immediate error correction enable/disable
S Stepping algorithm
P Used with format commands for determining data field pattern

CONTROL BYTE

This Byte is broken into the following fields:

FIELD	BIT(s)	FUNCTION
S (STEP)	0-3	Used in all commands which may cause a seek. Contains a code corresponding to a seek stepping algorithm. See Device Control Block (Fast Step Options).
U	4	Reserved. Unused.
P (FORMAT)	5	Used in the format commands. If 0, fill data fields with hex 6C. If 1, fill with the pattern in the sector buffer.
A (REREAD)	6	Used in the Read Drive command with LUN indicating Winchester. Normally 0. If 1, do not reread before attempting error correction.
R (RETRY)	7	Used in all commands which will cause an ID field to be read. Normally 0. If 1, Disable retries.

NOTE:

If one or more of the above fields are required to be specified for a command, then all the other fields in that control byte must be set to zero. If none are required, all eight bits are interpreted as "don't cares."

If retries are required then, a maximum of 8 are performed. If a Read problem still exists, a Reseek is issued and a maximum of eight more retries are performed.

WD1002-SHD DEVICE CONTROL BLOCK

FAST STEP OPTIONS

The fast step option field contains an unsigned 3-bit integer. These integers correspond to the following fast step algorithms:

OPTION	
0	Default: 3msec/step
1	Half-step for Seagate drives
2	3 msec
3	Half-step for TI drives
4	200 μsec/step. This is appropriate for buffered steps on drives made by Computer Memories Inc. and Rotating Memories Inc.
5	70 μsec/step.
6	30 μsec/step.
7	15 μsec/step.
8	2 msec/step.
9	3 msec
B-F	Spare (3 msec)

COMMAND STATUS BYTE

BITS	
0	0
1	Error flag: 0 -= no error 1 -= error
2	0
3	0
4	0
5-7	Logical unit number

At the completion of execution of each command, a command status byte is sent by the WD1002-SHD to the host to indicate to the host whether or not the command was successful.

The logical unit number returned is simply the contents of the logical unit field in the drive control block. For those commands that do not take a logical unit number as an input parameter, the logical unit number returned in the command status byte is not meaningful.

COMMAND COMPLETION BYTE

The command completion byte is an all zero byte sent by the WD1002-SHD to the host immediately following each command status byte. It indicates to the host that the Wd1002-SHD has freed the SASI bus.

COMMANDS

Each command is briefly described below.

1. TEST DRIVE READY (CLASS 0, OPCODE 0)

BYTE		CONTENTS
0	Bits 5-7 = Command class	0
	Bits 0-4 = Operation code	0
1	Bits 5-7 = Logical unit number	
	Bits 0-4	don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error, no seek complete, drive not ready, write fault.

Action

Select the drive and determine whether or not it is ready.

For a Winchester drive, read its status register and test the ready bit and busy bit. For Winchester drives supporting buffered seeks, this command is useful for determining the first drive to reach its target track.

2. RESTORE TO TRACK 0 (CLASS 0, OPCODE 1)

BYTE		CONTENTS
0	Bits 5-7 = Command class	0
	Bits 0-4 = Operation code	1
1	Bits 5-7 = Logical unit number Bits 0-4	don't care
2		don't care
2		don't care
4		don't care
5	Control Field	don't care
	Bit 7	
	Bit 6 - Immediate ECC:0→no Immediate correction	0
	Bit 4 - Reserved for future use. Must be zero.	0
	Bit 5 - Format data	0
	Bits 0-3	don't care

Possible Error Codes

No error, invalid command, Track 0 not found, drive not ready, write fault.

Action

Position the heads to cylinder 0.

3. REQUEST STATUS (CLASS 0, OPCODE 3)

BYTE		CONTENTS
0	Bits 5-7 = Command class	0
	Bits 0-4 = Operation code	3
1	Bits 5-7 = Logical unit number Bits 0-4	don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error, invalid command.

Action

Send the Host 4 bytes, the error byte and a 3-byte logical sector address for the specified drive.

The following non-drive error codes are treated as drive 0 errors: RAM failure (30.), ROM failure (31), ECC failure (32.). Hence, if command RAM diagnostic or command controller diagnostic detects an error, then status for drive 0 should be requested.

Error Byte 0

BITS	
7	Logical sector address flag: 0 = sector address not valid 1 = sector address valid
6	Not used. Set to 0
0-5	Error codes

Logical Sector Address

BYTE	
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21
2	Logical sector address bits 8-15
3	Logical sector address bits 0-7

If the most recent non-request-status command to the specified drive required a logical sector address, then the logical sector address flag is 1; else, it is 0. If the logical sector address flag is 0, then the logical sector address is not meaningful.

If there was an error on the immediately preceding command and the logical sector address flag is 1, then the logical sector address indicates the sector or track on which the error occured. If the command was a format type command, then the logical sector address indicates the track; else, it indicates the sector.

If there was no error on the immediately preceding command and the command was a format type command, then the logical sector address indicates the track one beyond the last track accessed.

If there was no error and the command was not a format type command, then the logical sector address indicates the last sector accessed.

3A. ERROR CODES

Disk Drive Error Codes

0 No error
1 No index pulses
2 No seek complete
3 Write fault
4 Drive not ready
6 Track 0 not found

Controller Error Codes

10/14 Not used because WD1010 combines CRC with several other errors in an I.D. field as errors not found.
11 Uncorrectable data error
12 Address mark not found
15 Seek error
18 Error burst corrected
19 Bad track

1A Format error
1C Illegal (direct) access to an alternate track
1D Alternate track already used
1E Alternate track not marked as alternate
1F Alternate track equals bad track

Command Error Codes

20 Invalid command
21 Invalid sector address

Miscellaneous Error Codes

30 RAM failure
31 ROM failure
32 ECC hardware failure

3B. ERROR CODE DESCRIPTIONS

No Seek Complete (2)

This error code is only returned by the Test Drive Ready command when the target drive is a Winchester that supports buffered seeks. It indicates the drive is busy doing a buffered seek.

Write Fault (3)

Indicates that there was write current to the head when the write gate was disabled. This is a very serious problem and should be fixed immediately.

Track 0 Not Found (6)

This error code is only returned by the recalibrate command. It indicates that the track 0 status from the drive did not become active after the maximum necessary steps towards cylinder 0.

Uncorrectable Data Error (11)

For a Winchester drive this error code indicates one or more error bursts in the data field were beyond the error correction code's ability to correct. The sector data for the sector in error is not sent to the Host.

Address Mark Not Found (12)

Indicates that the header for the target sector was found, but its address mark was not detected.

Error Burst Corrected (18)

Indicates that the error correction code (ECC) was used to successfully correct an error. The corrected sector data is sent to the Host. This is the only error condition for which sector data is sent to the Host.

Bad Track (19)

This usually indicates access of a track that was formatted as a bad track. However, there is a very small chance that it indicates that a track formatted as a bad track with alternate is so faulty that none of the multiple, duplicate pointers to the alternate track can be read.

Format Error (1A)

This error code is returned by the check track format command. It indicates that the track is not formatted with the specified interleave factor, or at least one sector header is unreadable.

This error code is returned by drive diagnostic to indicate that a bad-track-with-alternate does not contain a valid pointer to the alternate track.

Alternate Track Already Used (1D)

This error code is only returned by the format alternate track command. It indicates that the specified alternate track is already an alternate or bad track.

Alternate Track Not Marked as an Alternate (1E)

This error code indicates that access of a bad-track with-alternate caused access to an alternate track which was not marked as an alternate track.

Alternate Track Equals Bad Track (1F)

This error code is only returned by the format alternate track command. It indicates that the same track was specified as the bad track and the alternate track.

Invalid Command (20)

This error code indicates that the command class, command code, interleave factor, or fast step number were invalid.

RAM Failure (31)

This error code indicates one of the following conditions: (1) The program memory RAM checksum does not match the calculated checksum. (2) The RAM in the microprocessor failed. (3) The microprocessor CPU failed.

ECC Hardware Failure (32)

This error code indicates that the ECC Support Device failed during internal diagnostics.

4. FORMAT DRIVE (CLASS 0, OPCODE 4)

BYTE		CONTENTS
0	Bits 5-7 = Command class	0
	Bits 0-4 = Operation code	4
1	Bits 5-7 = Logical unit number	
	Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 - Retry disable:	
	0 = no disable	
	1 = disable	
	Bit 6 - Immediate ECC:	
	0 = no immediate correction	0
	Bit 5 - Format Data:	
	0 = Hex 6C	
	1 = contents of sector buffer	
	Bit 4 - Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, write fault.

Action

Format from the specified track to the end of the disk. The previous contents of the formatted tracks are ignored.

5. CHECK TRACK FORMAT (CLASS 0, OPCODE 5)

BYTE		CONTENTS
0	Bits 5-7 = Command class	0
	Bits 0-4 = Operation code	5
1	Bits 5-7 = Logical unit number	
	Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 - Retry disable:	
	0 = no disable	
	1 = disable	
	Bit 6 Immediate ECC:	
	0 = no immediate correction	0

5. CHECK TRACK FORMAT (Continued)

BYTE		CONTENTS
	Bit 5 - Format data	0
	Bit 4 - Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option Integer	

Possible Error Codes

No error, invalid command, invalid sector address, seek error, format error, drive not ready, write fault.

Action

Verify that the specified track is formatted with the specified interleave factor. Do not read the sector data fields.

6. FORMAT TRACK (CLASS 0, OPCODE 6)

BYTE		CONTENTS
0	Bits 5-7 = Command class	0
	Bits 0-4 = Operation code	6
1	Bits 5-7 = Logical unit number	
	Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 - Retry disable:	
	0 = no disable	
	1 = disable	
	Bit 6 - Immediate ECC:	
	0 = no immediate correction	0
	Bit 5 - Format data:	
	0 = Hex 6C	
	1 = contents of sector buffer	
	Bit 4 - Reserved for future use. Must be zero	0
	Bits 0-3 = Fast step option Integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek, error, write fault.

Action

Format the specified track. The current contents of the specified track are ignored.

WD1002-SAS Winchester/Floppy Disk Controller

FEATURES

- XSASI 8-BIT BI-DIRECTIONAL BUS HOST INTERFACE
- CONTROLS UP TO 2 WINCHESTER DRIVES (UP TO 8 R/W HEADS EACH)
- CONTROLS UP TO 2 FLOPPY DRIVES (DOUBLE-SIDED, DOUBLE DENSITY, SA450)
- USER-SELECTABLE 5 1/4" WINCHESTER AND FLOPPY OPERATION
- 32-BIT ECC FOR WINCHESTER DATA ERROR DETECTION AND CORRECTION
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- BAD TRACK MAPPING CAPABILITY FOR WINCHESTER
- AUTOMATIC FORMATTING
- 256 OR 512 BYTES PER SECTOR FOR WINCHESTER
- PROGRAMMABLE SECTOR SIZES (128,256,512,1024 BYTES) FOR FLOPPY
- PROGRAMMABLE INTERLEAVE CAPABILITY FOR WINCHESTER
- MULTIPLE SECTOR READS AND WRITES
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- OVERLAPPED SEEK CAPABILITY ON BUFFERED STEP DRIVES
- SUPPORTS IMPLIED SEEKS ON ALL COMMANDS
- SINGLE + 5V POWER SUPPLY

DESCRIPTION

The WD1002-SAS is a stand-alone, general-purpose Winchester and Floppy Controller Board designed to interface up to two Winchester disk drives and up to two Floppy disk drives to a Host Processor.The Winchester drive signals are based on the Floppy look-alike interface available on the Seagate Technology ST506 and other compatible drives. All necessary receivers and drivers are included on the board, allowing direct connection to the drive.

A separate computer access port enables communications between the Host Computer and Controller. This port conforms to XSASI and consists of an 8-bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and command parameters are transferred via this bus. An on-board data buffer allows bus transfers to be executed independently of the drive's data transfer.

The WD1002-SAS is based on a proprietary chip set consisting of the WD1010-05, WD1770, WD11C00-13, and WD1015-06 designed specifically for Winchester and Floppy control.

ARCHITECTURE

The WD1002-SAS consists of six on-board interface connectors:

- Power Connector (P1)
- Host interface connector (J1)
- Winchester drive control connector (P2)
- Two Winchester data cable connectors (J2,J3)
- Floppy control and data connector (J4)

The J5 connector is used for test only. The WD1002-SAS architecture is illustrated in Figure 1.

The WD1002-SAS accommodates up to two Winchester and up to two Floppy drives. The Winchester drive control cable is daisy-chained to each of two drives, and the drive data connectors, which carry differential signals, are radially connected. The drive control and data connector is daisy-chained to each of two drives. Table 1 defines the WD1002-SAS connectors and a source for the mating connectors on the associated cables.

TABLE 1. WD1002-SAS INTERFACE CONNECTORS

CONNECTOR	INTERFACE FUNCTION	EQUIVALENT MATING CONNECTOR
P1	Power	AMP1-480424-0 (Housing) AMP350078-4 (Pins)
J1	Host Interface (XSASI Bus)	AMP88379-8
P2	Winchester Control (Daisy-chained)	AMP88373-3
J2,J3	Winchester Data (Radially connected)	AMP88377-4
J4	Floppy Control and Data (Daisy-chained)	AMP88379-6
J5	Test (Do not use)	

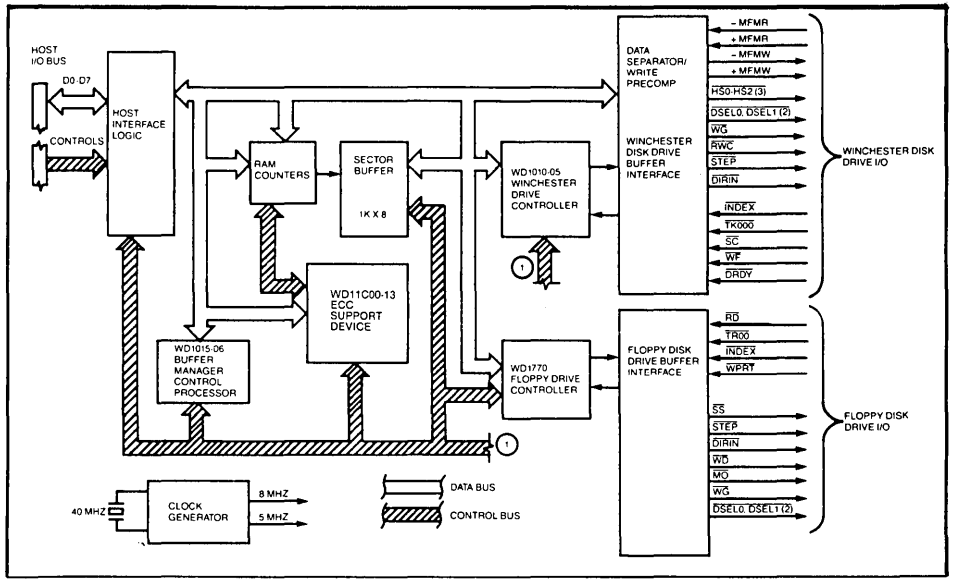


FIGURE 1. WD1002-SAS FUNCTIONAL BLOCK DIAGRAM

SPECIFICATIONS

HOST INTERFACE

Type	XSASI
Cable length (Daisy-chained)	15 ft (4.6 m) max.
Termination	Socketed 220/330 ohm resistor pack
Addressing	Jumper selectable (0 to 7)

DRIVE INTERFACES

	WINCHESTER	FLOPPY
Encoding method	MFM	MFM
Cylinders per drive	Programmable up to 1024	Programmable up to 245
Bytes per sector	Programmable 256 or 512	Programmable (128, 256, 512, or 1024)
Sectors per track	17, 32 for 256, 512 bytes/sector, respectively	26, 16, 9, 5 for 128, 256, 512, 1024 bytes/sector, respectively
Heads	8	2
Drives	2	2
Stepping rates/algorithm	Programmable	Programmable
Data transfer rate	5 Mbps	250 Kbps
Write precompensation time	12 nsec	125 nsec
Sectoring	Soft	Soft
CRC polynomial	$X^{16} + X^{12} + X^5 + 1$	
ECC polynomial	$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$	
Reciprocal ECC polynomial	$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^6 + X^4 + 1$	
Drive cable length:		
Control (Daisy-chained)	10 ft (3 m) max.	10 ft (3 m) max. for control and data combined
Data (Radially connected)	10 ft (3 m) max.	

DATA SEPARATOR

Aquisition Time	$\leq 6.4\mu$sec.
Capture Range	$\pm 5\%$
Bit Jitter Tolerance	± 36 nsec.
Asymmetry Tolerance	20 nsec. as measured over constant RCLK pattern.
f_o Stability	$\leq 2\%$

POWER

Voltage	$+5V \pm 5\%$
Current	2.0 amps max., 1.5 amps typ.
Ripple	0.1V max.

DIMENSIONS

Length	8 inches (20.3 cm)
Width	5.75 inches (14.6 cm)
Heigt (max. including board, components, & leads)	0.75 inches (1.9 cm)

ENVIRONMENTAL

Ambient temperature	0°C (32°F) to 55°C (131°F)
Relative humidity	10% to 90% non-condensing
Altitude	0 to 10,000 ft (3048 m)
Air Flow	100 linear ft/min. at 0.5 inches (0.13 cm) from component
MTBF	surfaces
MTTR	10,000 POH
	30 minutes

HOST INTERFACE

The WD1002-SAS Controller interfaces to the XSASI bus.Interfacing is accomplished through the J1 connector, connecting up to eight XSASI-compatible devices. The controller is shipped from the factory already configured to respond to device address 0. This preset address may be changed to any address from 0 through 7 by jumpering via the resistor pack at location RN2.

HOST INTERFACE CONNECTOR

The Host interface connector (J1) is a 50-pin vertical header. Table 2 provides the connector pin description and its bus signals. The cable terminating 220/330 ohm resistor pack is socketed onto the controller to provide flexibility in daisy-chaining the bus devices.

TABLE 2. HOST INTERFACE CONNECTOR (J1) PIN DESCRIPTION

SIG. GND	SIG. PIN	SIGNAL MNEMONIC	SIGNAL NAME	I/O*	FUNCTION
1 3 5 7 9 11 13 15	2 4 6 8 10 12 14 16	DO thru D7	DATA 0 thru DATA 7	I/O	An 8-bit bi-directional bus used to transfer commands, status, and data.
17 thru 34			NOT CONNECTED		
35	36	BSY	BUSY	O	Indicates to the Host that the WD1002-SAS is busy executing a command and is unable to accept another command. When BSY is asserted, it acknowledges receipt of SEL and its own address. De-asserting indicates transaction is completed.
37	38	ACK	ACKNOWLEDGE	I	Indicates to the controller that the Host has accepted the byte for data transfer.
39	40	RST	RESET	I	When asserted, RST places the WD1002-SAS into its initial power-up state. When asserted for >100 nsec, RST initializes the controller.
41	42	MSG	MESSAGE	O	Used with I/O, C/D, and REQ to indicate type of transfer. For example, during the Message Byte Transfer Phase, one byte of zeros is sent to the Host to indicate the command is complete.
43	44	SEL	SELECT	I	An asserted signal gives control of the bus to the address (0 through 7) which is selected by jumpering at location RN2.
45	46	C/D	CONTROL/DATA	O	Used with I/O, MSG, and REQ to indicate type of transfer.
47	48	REQ	REQUEST	O	Indicates to the Host that the controller is ready for data transfer.
49	50	I/O	INPUT/OUTPUT	O	Identifies the direction of transfers between the Host and WD1002-SAS. I asserted = input to Host; O asserted = output to controller.

*The I/O column is in relation to the WD1002-SAS and not the Host.

HOST INTERFACE BUS OPERATION

The timing sequence for bus operations includes five phases:

1. **Reset Phase.** Occurs when RESET is asserted. Used by the Host to force the controller(s) on the bus to the same state it was in following a power on condition.

2. **Bus Free Phase.** Occurs between the completion of one transaction (Bus Release Phase) and the initiation of the next transaction (Target Selection Phase). Also occurs during the time in which no unit has control of the bus. All eight control lines and eight data lines are de-asserted.
3. **Target Selection Phase.** Occurs when the Host places a target address on the bus and asserts SEL, and the addressed controller asserts BSY. The Host then de-asserts SEL before completing the phase.

   The target address consists of one asserted and seven de-asserted DO through D7 signals. The controller's default address of O corresponds to an asserted DO, which may be changed to any address by jumpering. Two controllers may not use the same address.
4. **Information Transfer Phase.** Used to transfer one or more bytes on the bus. The type of transfer is determined by the I/O, C/D, and MSG signal codes on the lines (providing five valid combinations) as shown in Table 3, and as qualified by request. A valid combination indicates to the Host the types of byte transfers that are to follow.

The following are used to transfer information:

- **Command Block Transfer Phase.** Used to send a block of command bytes from the Host to the controller, specifying the operation to be performed (e.g. Format Disk).
- **Data Block Transfer Phase.** Used primarily to send one or more sectors of data either from or to the Host. Also used to send a block of parameters to the controller or to the Host.
- **Status Byte Transfer Phase.** During this phase, one byte is sent to the Host indicating the status of the operation.
- **Message Byte Transfer Phase.** One byte of zeros is sent to the Host to indicate the command is complete.

For each byte transferred, the following operations occur in sequence to perform the asynchronous handshake:

- Controller asserts $\overline{REQ}$
- Host asserts $\overline{ACK}$
- Controller de-asserts $\overline{REQ}$
- Host de-asserts $\overline{ACK}$

  For controller-to-Host transfers, the eight bits are valid on the bus at least 100 nsec before $\overline{REQ}$ is asserted. Host-to-controller transfers are valid on the bus no later than 250 nsec after $\overline{ACK}$ is asserted. It is recommended that before asserting $\overline{ACK}$, make sure the data is valid. (Note: For debugging, bytes are valid on the bus when $\overline{REQ}$ is de-asserted during any transfer.)

5. **Bus Release Phase.** Occurs when $\overline{BSY}$ is de-asserted. This phase signals the Host that the current transaction has terminated and the associated selected target is no longer controlling the bus.

BUS PHASE SEQUENCING

A Reset Phase may occur any time and is followed by the Bus Free Phase. In the absence of a Reset Phase, the bus alternates between the Bus Free Phase and one transaction. A transaction always consists of the following:

1. One Target Selection Phase
2. One Command Block Transfer Phase
3. Zero or more Data Block Transfer Phase(s) - Type and number determined by the preceding Command Block Transfer Phase
4. One Status Byte Transfer Phase
5. One Message Byte Transfer Phase
6. One Bus Release Phase

During a transaction, all Data Block Transfer Phases are the same size and are sent in the same direction.

DRIVE INTERFACES

WINCHESTER DRIVE CONTROL CONNECTOR

The Winchester drive control connector, a 34 pin printed circuit card edge connector, is a low- speed bus daisy-chained to each Winchester drive in the system. To terminate the control signals on the WD1002-SAS properly, the last drive in the daisy-chain must have a 220/330 ohm resistor pack installed. The pin description and control signals are provided in Table 4.

TABLE 3. INFORMATION TRANSFER PHASE

SIGNAL MNEMONIC			TRANSFER TYPE	NUMBER OF BYTES
$\overline{I/O}$	$\overline{C/D}$	$\overline{MSG}$		
1	0	1	Command Block	6
1	1	1	Data Out Block	3, 8, 128, 256, 260, 512, 516, or 1024
0	1	1	Data In Block	1, 4, 128, 256, 260, 512, 516, or 1024
0	0	1	Status Byte	1
0	0	0	Message Byte	1

TABLE 4. WINCHESTER DRIVE CONTROL CONNECTOR (P2) PIN DESCRIPTION

SIG. GND	SIG. PIN	SIGNAL MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	2	RWC	REDUCE WRITE CURRENT	O	RWC is asserted when the cylinder specified by the Set Parameters Command is reached.
3	4	HS2	HEAD SELECT 2	O	HS2 is one of three Head Select signals decoded by the drive to select one of eight R/W heads.
5	6	WG	WRITE GATE	O	WG is asserted when valid data is to be written on disk. WD1002-SAS de-asserts this signal when a WF is detected. Special circuitry is included to ensure the output does not glitch during power on.
7	8	SC	SEEK COMPLETE	I	SC informs the WD1002-SAS the head of a selected drive reached the desired cylinder and has stabilized.
9	10	TKOOO	TRACK OOO	I	The drive asserts this signal when the R/W heads are positioned over the outermost cylinder, cylinder O.
11	12	WF	WRITE FAULT	I	WF is asserted by the selected drive when a write error occurs. The command in progress aborts and no other disk command can be executed while this signal is asserted.
13	14	HSO	HEAD SELECT O	O	HSO is one of three Head Select signals decoded by the drive to select one of eight R/W heads.
15	16		NOT CONNECTED		
17	18	HS1	HEAD SELECT 1	O	HS1 is one of three Head Select signals decoded by the drive to select one of eight R/W heads.
19	20	INDEX	INDEX PULSE	I	This signal indicates the start of a track. It is used as a synchronization point during formatting and as a time-out mechanism for retries. This signal pulses once for each disk revolution.
21	22	DRDY	DRIVE READY	I	Informs the controller that the drive motor is up to speed.
23	24	STEP	STEP PULSE	O	STEP, together with DIRIN, positions the heads to the desired cylinder. STEP pulses once for each step. DIRIN determines the step direction.
25	26	DSEL0	DRIVE SELECT 0	O	DSEL0 is used to select drive 0.
27	28	DSEL1	DRIVE SELECT 1	O	DSEL1 is used to select drive 1.
29 thru 32			NOT CONNECTED		
33	34	DIRIN	DIRECTION IN	O	DIRIN determines the direction the R/W heads take when the step line is pulsed. De-asserted = out; asserted = in.

WINCHESTER DRIVE DATA CONNECTORS

Connectors J2 and J3 allow data transfer between the controller and each drive. The data lines are differential in nature and must be connected to each drive with its own cable, i.e., drive O to J2 and drive 1 to J3. Each drive is radially connected with a maximum cable length of 10 feet. Each data connector is a 20-pin vertical header on 0.1 inch center. Data connector pin descriptions and signals are given in Table 5.

FLOPPY DRIVE CONTROL AND DATA CONNECTOR

The Floppy drive control signals function in a manner similar to the Winchester except both the control and data signals are transmitted on the same connector. The connector is daisy-chained to each drive. To properly terminate each TTL level output signal from the WD1002-SAS, the last drive in the daisy-chain must have line terminations installed as specified by the drive manufacturer. A flat ribbon cable, or twisted-pair, of less than 10 feet should be used. The connector is a 34-pin vertical header on 0.1 inch center. Pin description and signals are given in Table 6.

TABLE 5.
WINCHESTER DRIVE DATA CONNECTOR - J2,J3

SIG. GND	SIG. PIN	I/O	SIGNAL NAME
	1		NC
2			GND
	3		NC
4			GND
	5		NC
6			GND
	7		NC
8			GND
	9		NC
	10		NC
11			GND
12			GND
	13	O	+MFM Write Data
	14	O	-MFM Write Data
15			GND
16			GND
	17	I	+MFM Read Data
	18	I	-MFM Read Data
19			GND
20			GND

TABLE 6. FLOPPY DRIVE CONTROL AND DATA CONNECTOR (J4) PIN DESCRIPTION

SIG. GND	SIG. PIN	SIGNAL MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1 thru 4			NOT CONNECTED		
5	6	$\overline{\text{DSELO}}$	DRIVE SELECT O	O	$\overline{\text{DSELO}}$ is used to select drive O. (Note: On an SA450, this is drive 4.)
7	8	$\overline{\text{INDEX}}$	INDEX PULSE	I	This signal indicates the start of a track. It is used as a synchronization point during formatting and as a time-out mechanism for retries. This signal pulses once for each disk revolution.
9	10	$\overline{\text{DSEL1}}$	DRIVE SELECT 1	O	$\overline{\text{DSEL1}}$ is used to select drive 1.
11 thru 14			NOT CONNECTED		
15	16	$\overline{\text{MO}}$	MOTOR ON	O	Directly controls the Floppy drive's power-on of the spindle motor. A 1-second delay occurs after the motor is on.
17	18	$\overline{\text{DIRIN}}$	DIRECTION IN	O	$\overline{\text{DIRIN}}$ determines the direction the R/W heads take when the step line is pulsed. De-asserted = out; asserted = in.
19	20	$\overline{\text{STEP}}$	STEP PULSE	O	$\overline{\text{STEP}}$, together with $\overline{\text{DIRIN}}$, positions the heads to the desired cylinder. $\overline{\text{STEP}}$ pulses once for each step. $\overline{\text{DIRIN}}$ determines the step direction.
21	22	$\overline{\text{WD}}$	WRITE DATA	O	Provides data to be written on the diskette and is enabled by $\overline{\text{WG}}$ asserted.
23	24	$\overline{\text{WG}}$	WRITE GATE	O	$\overline{\text{WG}}$ is asserted when valid data is to be written on disk. It is used by the drive to enable the write current to the head.

TABLE 6. FLOPPY DRIVE CONTROL AND DATA CONNECTOR (J4) PIN DESCRIPTION (CONTINUED)

SIG GND	SIG PIN	SIGNAL MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
25	26	$\overline{\text{TROO}}$	$\overline{\text{TRACK OO}}$	I	The drive asserts this signal when the R/W heads are positioned over the outermost cylinder.
27	28	$\overline{\text{WPRT}}$	$\overline{\text{WRITE PROTECT}}$	I	Indicates to the controller a write-protected diskette is installed. When $\overline{\text{WPRT}}$ is asserted, no data is written to the diskette.
29	30	$\overline{\text{RD}}$	$\overline{\text{READ DATA}}$	I	Provides raw data (clock and data combined) as detected by the drive circuitry.
31	32	$\overline{\text{SS}}$	$\overline{\text{SIDE SELECT}}$	O	$\overline{\text{SS}}$ determines the side of the diskette to be used. Asserted = select side O; de-asserted = select side 1.
33	34		NOT CONNECTED		

POWER CONNECTOR

A 4-pin amp connector P1 provides power input to the WD1002-SAS:

SIG GND	SIG. PIN	SIGNAL NAME
	1	NOT CONNECTED
2		GND
3		GND
	4	+5V Regulated

WD1002-SAS COMMAND BLOCK

A transaction is initiated by the Host, instructing the controller to execute a command. During the Command Block Transfer Phase, six bytes of information specifying the command are transferred to the controller. Figure 2 defines the contents of each byte in the Command Block. These parameters are sent to the WD1002-SAS by the Host to perform specific transactions.

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	COMMAND CLASS			OP CODE				
1	LOGICAL UNIT NUMBER			LOGICAL SECTOR ADDRESS (BITS 20 THRU 16)				
2	LOGICAL SECTOR ADDRESS (BITS 15 THRU 8)							
3	LOGICAL SECTOR ADDRESS (BITS 7 THRU 0)							
4	INTERLEAVE OR BLOCK COUNT							
5	CONTROL BYTE							

FIGURE 2. COMMAND BLOCK DESCRIPTION

Command Class

Designates whether the command is used in operation (class 0) or for diagnostic (class 7). Command classes 1 through 6 are reserved for future use.

OP Code

An operation code is used in each command class to identify the function of the commands, e.g., read and write.

Logical Unit Number

There are 8 logical unit numbers. For example, logical unit numbers 0 and 1, respectively. The Floppy logical unit numbers are 4 and 5.

Logical Sector Address

This address is a 21-bit unsigned integer specifying a unique physical sector. The following equation shows the one-to-one ratio between the set of logical sector addresses and the set of physical sectors:

Logical Sector Address = (((Cylinder Number* Number of Heads) + Head Number)* Number of Sectors per Track) + Sector Number

Each format command begins operation at the beginning of the track containing the specified sector.

Interleave or Block Count

The interleave factor is used by format commands. The 3:1 ratio is the minimum operational interleave; however, the disk also may be formatted at a 1:1 ratio. The maximum interleave is equal to the sectors-per-track minus one. Block count specifies the number of sectors to be used for each data transfer command. The block count is an unsigned, no-zero integer. A block count of all zeros equals 256 sectors.

Control Byte

The descriptions and contents of the Control Byte for both the Winchester and Floppy drives are shown in Table 7.

TABLE 7. CONTROL BYTE DESCRIPTION

BIT	WINCHESTER CONTENTS	FLOPPY CONTENTS
0 thru 3	Step Option. Unsigned 4-bit integers corresponding to stepping rates in Table 8.	Step Option. Unsigned 4-bit integers corresponding to stepping rates in Table 8.
4	Reserved for future use. Must be 0.	MSB Bit 5 / LSB Bit 4 / Sector Size: 0 0 — 128 bytes/sector 0 1 — 256 bytes/sector 1 0 — 512 bytes/sector 1 1 — 1024 bytes/sector
5	Format Data: 0 = 6C Hex 1 = Contents of Sector Buffer (Data is provided by the Write Sector Buffer Command)	
6	Error Correction: 0 = Correction After Two Identical Syndromes 1 = Correction After One Syndrome	Not used. Must be 0.
7	Error Retry: 0 = Enable Retry 1 = Disable Retry	Not used. Must be 0.

TABLE 8. STEP OPTIONS

OPTION	WINCHESTER STEP RATE*	FLOPPY STEP RATE
0	3 msec per step**	15 μsec
1	Half-step for Seagate ST506 (MLC2); fast step for Texas Instruments drives	1 msec
2	3 msec per step	2 msec
3	Half-step for Seagate ST506 (MLC2); fast-step for Texas Instruments drives	3 msec
4	200 μsec per step (appropriate for buffered-steps on drives manufactured by Computer Memories Inc. and Rotating Memories Inc.)	4 msec
5	70 μsec per step	5 msec
6	3 μsec per step	6 msec
7	15 μsec per step	8 msec
8	2 msec per step for Olivetti-561	10 msec
9	3 msec per step	12 msec
A	3 msec per step	14 msec
B	3 msec per step	16 msec
C	3 msec per step	18 msec
D	3 msec per step	20 msec
E	3 msec per step	25 msec
F	3 msec per step	40 msec

*For the Seek Command, buffered-seeks(Options 4 through 7) do not wait for seek completion. All other seeks wait for seek completion.

**This is the preferred 3 msec step rate.

COMMAND DESCRIPTIONS

The WD1002-SAS commands are summarized in Table 9. Each command is listed with its Command Block contents.

TABLE 9. SUMMARY OF COMMANDS

COMMAND	CLASS	OP CODE	LUN (W/F)	LSA	INT/BLK	CONTROL BYTE					
						R	C	F	MSB SS	LSB SS	STEP
TEST DRIVE READY	0	00	V(W)	n	n	n	n	n	n	n	n
RECALI-BRATE	0	01	V(W) V(F)	n n	n n	V n	V n	n n	n n	n n	V V
REQUEST STATUS	0	03	V(W/F)	n	n	n	n	n	n	n	n
FORMAT DRIVE	0	04	V(W)	V*	V(INT)	V	V	V	n	n	V
CHECK TRACK FORMAT	0	05	V(W)	V*	V(INT)	V	V	V	n	n	V
FORMAT TRACK	0	06	V(W) V(F)	V* V*	V(INT) V(INT)	V n	V n	V n	n V	n V	V V
FORMAT BAD TRACK	0	07	V(W)	V*	V(INT)	V	V	V	n	n	V
READ SECTOR	0	08	V(W) V(F)	V V	V(BLK) V(BLK)	V n	V n	V n	n V	n V	V V
WRITE SECTOR	0	OA	V(W) V(F)	V V	V(BLK) V(BLK)	V n	V n	V n	n V	n V	V V
SEEK	0	OB	V(W) V(F)	V* V*	n n	V n	V n	V n	n V	n V	V V
SET PARAMETERS	0	OC	V(W/F)	n	n	n	n	n	n	n	n
RETURN LAST CORRECTED BURST LENGTH	0	OD	V(W)	n	n	n	n	n	n	n	n
FORMAT ALTERNATE TRACK	0	OE	V(W)	V*	V(INT)	V	V	V	n	n	V
WRITE SECTOR BUFFER	0	OF	n(W)	n	n	n	n	n	n	n	n
READ SECTOR BUFFER	0	10	n(W)	n	n	n	n	n	n	n	n
RAM DIAGNOSTIC	7	OO	n(W/F)	n	n	n	n	n	n	n	n
DRIVE DIAGNOSTIC	7	O3	V(W)	n	n	V	V	V	n	n	V
CONTROLLER DIAGNOSTIC	7	O4	n(W/F)	n	n	n	n	n	n	n	n
READ LONG	7	O5	V(W)	V	V(BLK)	V	V	V	n	n	V
WRITE LONG	7	O6	V(W)	V	V(BLK)	V	V	V	n	n	V

LEGEND:

V	Must be a valid parameter
n	Not used (should be 0 for future compatibility).
LUN(W/F)	Logical Unit Number of Winchester drives
INT	Interleave factor.
BLK	Block Count.
R	Error Retry. Bit 7 of the Control Byte for Winchester drives.
C	Error Correction. Bit 6 of the Control Byte for Winchester drives.
F	Format Dat6a. Bit 5 of the Control Byte for Winchester Drives.
MSB SS	Most Significant Bit Sector Size. Bit 5 of the Control Byte for Floppy drives.
LSB SS	Least Significant Bit Sector Size. Bit 4 of the Control Byte for Floppy drives.
STEP	Stepping Rate. Bits 0 through 3 of the Control Byte as defined in Table 8 for Winchester and Floppy drives.

Each Wd1002-SAS command is described briefly in the following paragraphs. Refer to Table 9 for their parameter contents.

1. TEST DRIVE READY (CLASS 0, OP CODE 00)

This command reads the drive's status. For Winchester drives supporting buffered-seeks, this command is useful for determining the first drive to reach its selected track.

This command is not used for the Floppy drives.

Possible Error Codes

00	No Error
03	Write Fault
04	Drive Not Ready
08	Buffered-Seek in Progress
32	Invalid Command

2. RECALIBRATE (CLASS 0. OP CODE 01)

This command positions the R/W heads over the outer most cylinder, cylinder 0.

Possible Error Codes

00	No Error
03	Write Fault
04	Drive Not Ready
06	Track 0 Not Found
32	Invalid Command

3. REQUEST STATUS (CLASS 0, OP CODE 03)

This command sends the Host four status bytes of error information (as shown in Figure 3) for the specified drive.

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	AVF	0	ERROR CODE					
1	LOGICAL UNIT NUMBER		LOGICAL SECTOR ADDRESS (BITS 20 THRU 16)					
2	LOGICAL SECTOR ADDRESS (BITS 15 THRU 8)							
3	LOGICAL SECTOR ADDRESS (BITS 7 THRU 0)							

AVF

Address valid flag. Indicates that the Logical Sector Address fields are valid.

FIGURE 3. FOUR STATUS BYTES

The information sent by the controller to the Host via the Request Status Command includes these conditions:

- % If the most recent non-Request-Status Command to the specified drive requires a logical sector address, then the address valid flag is 1.
- % If an error has occurred on the preceding command and the address valid flag is 1, then the logical sector address indicates the record on which the error occurred.
- % If no error has occurred on the preceding command to format the track, format the drive, or format the alternate track, then the logical sector address indicates one track beyond the last track accessed.
- % If no error has occurred and the command is to check the track format, format the bad track, or is not a format command, then the logical sector address indicates the last track or sector

Possible Error Codes

00 No Error
32 Invalid Command

The WD1002-SAS error code descriptions are summarized in Table 10.

TABLE 10. ERROR CODE DESCRIPTIONS

ERROR CODE	ERROR NAME	TYPE OF ERROR	DESCRIPTION
00	No Error	Disk Drive	No error has occurred.
03	Write Fault	Disk Drive	Indicates write current occurred when $\overline{WG}$ is de-asserted, or a $\overline{SC}$ is not asserted and a drive is selected while WG is asserted.
04	Drive Not Ready	Disk Drive	The selected drive's $\overline{DRDY}$ is de-asserted. Indicates the motor of the selected drive is not up to speed.
06	Track 0 Not Found	Disk Drive	This code is returned by the Recalibrate Command. Indicates the $\overline{TKOOO}$ or $\overline{TROO}$ from the selected drive was not asserted after the maximum number of steps (up to 1024 for the Winchester; up to 256 for the Floppy) toward cylinder 0.
08	Buffered-Seek in Progress	Disk Drive	This code is returned by the Test Drive Ready Command, indicating the selected drive (Winchester supporting buffered-seeks) is busy performing a buffered-seek.
10	Write Protected	Controller	This code is returned by Floppy drives when write-protect tab is detected on the diskette.
11	CRC Error	Controller	Indicates a CRC error in the data field is detected during a Floppy command execution after eight retries.
12	Address Mark Not found	Controller	This code is returned when address is not found during Floppy command execution after eight retries.
17	Uncorrectable Data Error	Controller	For a Floppy drive, this code indicates a CRC error in the data field. For a Winchester drive, this code indicates one or more error bursts in the data field are beyond the ECC's ability to correct. Data for the sector in error is not sent to the Host.
18	Data Address Mark Not Found	Controller	This code is returned by Winchester drives. Indicates the selected sector's header is found, but its Address Mark is not detected.
21	Seek Error	Controller	Indicates the controller cannot locate the specified address on the disk.
24	Error Burst Corrected	Controller	A code returned by Winchester drives. Indicates the ECC successfully corrected an error. The corrected sector data is sent to the Host (Note: This is the only error condition in which sector data is sent to the Host.)
25	Bad Track	Controller	Usually indicates access of a formatted bad track. Also indicates a formatted Bad-Track-With-Alternate is faulty and multiple, duplicate pointers to the Alternate Track cannot be read.
26	Format Error	Controller	This code is returned by the Check Track Format Command. Indicates a track is not formatted, a track is not formatted with the specified interleave factor, or at least one sector header is unreadable. This code is also returned by the drive diagnostic, indicating a Bad-Track-With-Alternate does not contain a valid pointer to the Alternate Track.
28	Illegal (Direct) Access to an Alternate Track	Controller	The specified address is not a valid address for an Alternate Track.

TABLE 10. ERROR CODE DESCRIPTIONS (CONTINUED)

ERROR CODE	ERROR NAME	TYPE OF ERROR	DESCRIPTION
29	Alternate Track Already Used	Controller	This code is returned by the Format Alternate Track Command. Indicates the specified Alternate Track is already an alternate or bad track.
30	Alternate Track Not Marked as Alternate	Controller	Indicates access of a Bad-Track-With-Alternate caused access to an Alternate Track not marked as an Alternate Track.
31	Alternate Track Equals Bad Track	Controller	This code is returned by the Format Alternate Track Command. Indicates the same track is specified as the Bad Track and the Alternate Track.
32	Invalid Command	Command	Indicates an invalid command class, operation code, logical unit number, interleave factor, or step number.
33	Invalid Sector Address	Command	Indicates the specified address has reached the file device's given range, exceeding capacity.
48	RAM Failure	Miscellaneous	Indicates the external RAM failed.
49	ROM Failure	Miscellaneous	Indicates ROM checksum does not match the calculated checksum.

4. FORMAT DRIVE (CLASS 0, OP CODE 04)

This command formats from the specified track to the end of the disk. The previous contents of the formatted tracks are ignored.

This command is not used for the Floppy drives.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
21 Seek Error
32 Invalid Command
33 Invalid Sector Address

5. CHECK TRACK FORMAT (CLASS 0, OP CODE 05)

This command verifies whether the specified track is formatted with the specified interleave factor. It does not read the sector data fields.

This command is not used for the Floppy drives.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
21 Seek Error
26 Format Error
32 Invalid Command
33 Invalid Sector Address

6. FORMAT TRACK (CLASS 0, OP CODE 06)

This command formats the specified track, ignoring the current contents. For Floppy drives, 5E Hex is written in the data field.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
21 Seek Error
32 Invalid Command
33 Invalid Sector Address

7. FORMAT BAD TRACK (CLASS 0, OP CODE 07)

This command formats the specified track with a Bad Block Mark in each sector header, ignoring the previous contents. The contents of a bad track are not accessible.

This command is not used for the Floppy drives.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
32 Invalid Command
33 Invalid Sector Address

8. READ SECTORS (CLASS 0, OP CODE 08)

Beginning with the specified sector, this command reads the specified number of consecutive sectors.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
11 CRC Error
12 Record Not Found
17 Uncorrectable Data Error
18 Address Mark Not Found
21 Seek Error
24 Error Burst Corrected
25 Bad Track
28 Illegal (Direct) Access to an Alternate Track
30 Alternate Track Not Marked as Alternate
32 Invalid Command
33 Invalid Sector Address

9. WRITE SECTORS (CLASS 0, OP CODE 0A)

Beginning with the specified sector, this command writes the specified number of consecutive sectors.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
10 Write-Protected
12 Record Not Found
18 Address Mark Not Found
21 Seek Error
25 Bad Track
28 Illegal (Direct) Access to an Alternate Track
30 Alternate Track Not Marked as Alternate
32 Invalid Command
33 Invalid Sector Address

10. SEEK (CLASS O, OP CODE OB)

This command moves the read/write head to the specified cylinder. It does not read any sector header to verify start or end position.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
32 Invalid Command
33 Invalid Sector Address

11. SET PARAMETERS (CLASS 0, OP CODE OC)

For Winchester Drives, the following parameters are set to their respective default values upon power up or reset:

PARAMETER	DEFAULT VALUE
Number of Cylinders	153
Number of Heads	4
Starting RWC Cylinder: The specified number for this parameter is rounded down to the nearest integer in multiples of four. For example, 0,4,8,12,. . . . . .,. . .,1020.	128
Starting Write Precomp Cylinder	64
Maximum Length of Error Burst To Be Corrected: For most applications, the maximum length of error burst to be corrected should be approximately 5 because correcting longer bursts increases the chance of miscorrecting.	11

Winchester Parameter Block

The parameters sent by the Host to the WD1002-SAS in the following format replace the default values shown above:

BYTE	DESCRIPTION
0	Number of Cylinders MSByte
1	Number of Cylinders LSByte
2	Bits 4 thru 7 = Must be 0 Bits 0 thru 3 = Numbers of Heads
3	Start RWC Cylinder Number MSByte
4	Start RWC Cylinder Number LSByte
5	Start Write Precomp Cylinder Number MSByte
6	Start Write Precomp Cylinder Number LSByte
7	Bits 4 thru 7 = Must be 0 Bits 0 thru 3 = Maximum Length of Error Burst To Be Corrected

For Floppy Drives, power up or reset sets the parameters to the following defaults:

PARAMETER	DEFAULT VALUE
Number of Cylinders	40
Number of Heads	2
Tracks Per Inch Flag for 96 tpi Diskette	0

Floppy Parameter Block

The parameters sent by the Host to the WD1002-SAS in the following format replace the default values shown above:

BYTE	DESCRIPTION
0	Number of Cylinders MSByte
1	Number of Cylinders LSByte
2	Bits 4 thru 7 = Must be 0 Bits 0 thru 3 = Number of Heads
3	If 48 or 96 Tracks Per Inch diskette is used in a drive with the same TPI = O If 48 Tracks Per Inch diskette is used in a 96 TPI drive = 1
4	Zeros
5	Zeros
6	Zeros
7	Zeros

Possible Error Codes

00 No Error
32 Invalid Command

12. RETURN LAST CORRECTED BURST LENGTH (CLASS 0, OP CODE OD)

This command sends the Host one byte of data containing the length of the most recently corrected error burst. If no error burst has been corrected since the last power-up or reset, then Error Burst Length Block of zero is sent to the Host.

This command is not used for the Floppy drives.

Possible Error Codes

00 No Error

13 FORMAT ALTERNATE TRACK (CLASS O, OP CODE OE)

This command formats the specified track as a Bad-Track-With-Alternate. Then it formats the specified Alternate Track with the specified interleave factor. The alternate Track is specified by the Host by sending the following Alternate Sector Address Block to the WD1002-SAS after the device Control Byte :

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	0			LOGICAL SECTOR ADDRESS (BITS 20 THRU 16)				
1	LOGICAL SECTOR ADDRESS (BITS 15 THRU 8)							
2	LOGICAL SECTOR ADDRESS (BITS 7 THRU 0)							

This command is not used for the Floppy drives.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
21 Seek Error
29 Alternate Track Already Used
31 Alternate Track Equals Bad Track
32 Invalid Command
33 Invalid Sector Address

14. WRITE SECTOR BUFFER (CLASS O,OP CODE OF)

This command writes data from the Host to the WD1002-SAS Sector Buffer. The Host sends as many bytes as there are in a sector on Logical Unit 0. This data is not written to any disk. The Write Sector Buffer Command provides the data used by format commands having bit 5 of the Control Byte = 1.

This command is not used for the Floppy drives.

Possible Error Codes

00 No Error

15. READ SECTOR BUFFER (CLASS O, OP CODE 10)

This command sends current contents of the WD1002- SAS Sector Buffer the Host. The Host accepts as many bytes as there are in a sector on Logical Unit 0.

This command is not used for the Floppy drives.

Possible Error Codes

00 No Error

16. RAM DIAGNOSTIC (CLASS 7,OP CODE 00)

This command writes and reads various patterns into the Sector Buffer to test. This command also destroys the previous contents of the Sector Buffer.

Possible Error Codes

00 no Error
48 RAM Failure

17. DRIVE DIAGNOSTIC (CLASS 7,OP CODE 03)

This command recalibrates the selected drive, then scans the ID on each track. This command does not write to the disk or send any sector data to the Host.

The drive diagnostic is used to verify that at least one sector header can be read on each track. When a track formatted as bad Track, Bad-Track- With-Alternate, or Alternate Track is encountered, an error is not reported. However, an error is reported when a Bad-Track-With-Alternate is encountered with the Alternate Track Not Marked as an Alternate. If no pointer to the Alternate Track can be read from a Bad-Track-With-Alternate then a Bad Track error is reported.

This command is not used for the Floppy drives.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
21 Seek Error
25 Bad Track
30 Alternate Track Not Marked as Alternate
32 Invalid Command

18. CONTROLLER DIAGNOSTIC (CLASS 7,OP CODE 04)

This command calculates a checksum for the ROM program, and tests the microprocessor and Sector Buffer. This command does not access any disk drive but destroys the previous contents of the Sector Buffer.

Possible Error Codes

00 No Error
48 RAM Failure
49 ROM Failure

19. READ LONG (CLASS 7,OP CODE 05)

Beginning with the specified sector, this command reads the specified number of consecutive sectors and an additional four ECC data bytes per sector provided by the controller.

This command is not used for the Floppy drives.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
18 Address Mark Not Found
21 Seek Error
25 Bad Track
28 Illegal (Direct) Access to an Alternate Track
30 Alternate Track Not Marked as Alternate
32 Invalid Command
33 Invalid Sector Address

20. WRITE LONG (CLASS 7,OP CODE 06)

Beginning with the specified sector, this command writes the specified number of consecutive sectors. Following each sector, the Host sends the WD1002-SAS an additional four ECC data bytes (unaltered by the controller) which are written to the disk as ECC bytes for the sector. This command is useful for diagnostic purposes.

This command is not used for the Floppy drives.

Possible Error Codes

00 No Error
03 Write Fault
04 Drive Not Ready
18 Address Mark Not Found
21 Seek Error
25 Bad Track
28 Illegal (Direct) Access to an Alternate Track
30 Alternate Track Not Marked as Alternate
32 Invalid Command
33 Invalid Sector Address

COMMAND STATUS BYTE

After each command is executed, the WD1002-SAS sends a Command Status Byte to the Host to determine whether the command is completed successfully. The logical unit number returned represents the contents of the logical unit field in the drive control block.

BITS							
7	6	5	4	3	2	1	0
LUN			0	0	0	E	0

LUN Logical Unit Number
E Error Flag:
0 = No Error
1 = Error

COMMAND COMPLETION BYTE

Immediately following each Command Status Byte, the WD1002-SAS sends a Command Completion Byte containing all zeros to the Host while $\overline{\text{MSG}}$ is asserted. This byte indicates to the Host that $\overline{\text{BSY}}$ will be de-asserted, the bus is available for the next command.

HOST INTERFACE TIMING

Timing diagrams are shown in Figures 4 through 6 and their values are given in Tables 11 and 12.

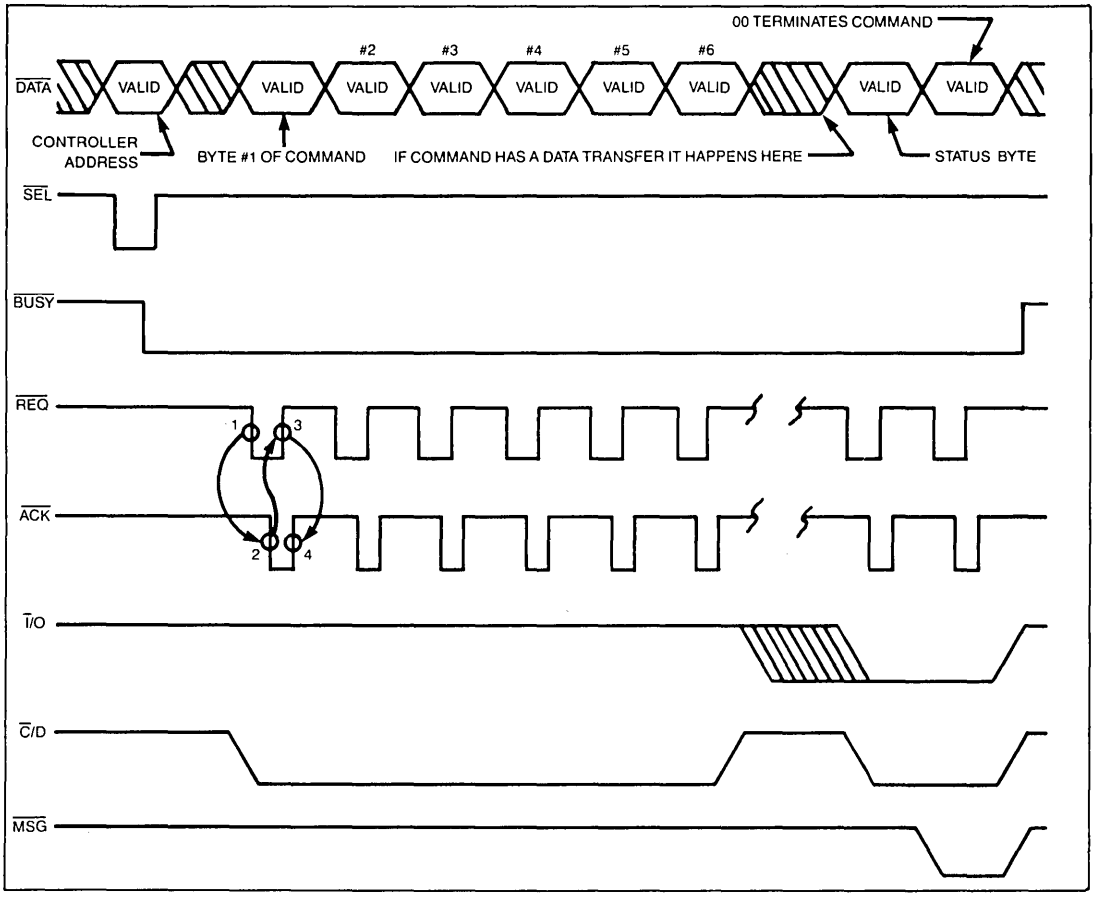


FIGURE 4. TYPICAL HOST-CONTROLLER BUS TRANSFER TIMING

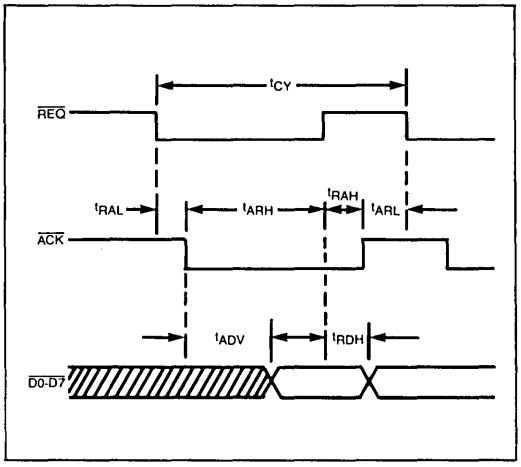


FIGURE 5: HOST-TO-CONTROLLER TIMING

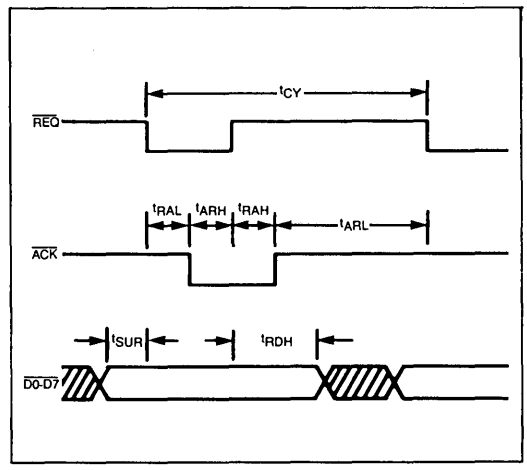


FIGURE 6: CONTROLLER-TO-HOST TIMING

TABLE 11.
HOST-TO-CONTROLLER TIMING PARAMETERS

t_{XX}	MIN(nsec)	MAX(nsec)
t_{CY}*	1152	
t_{RAL}†	0	
t_{ARH}	600	840
t_{RAH}††	0	
t_{ARL}	200	488
t_{ADV}		375
T_{RDH}	0	

*If conditions in † and †† are met, then t_{CY} (typ) = 1200 nsec and t_{CY} max = 1248 nsec.
†If $t_{RAL} \leq 89$ nsec, then no wait states are inserted.
††If $t_{RAH} \leq 97$ nsec, then no wait states are inserted.
One wait state = 200 nsec.

TABLE 12.
CONTROLLER-TO-HOST TIMING PARAMETERS

t_{XX}	MIN(nsec)	MAX(nsec)
t_{CY}*	1152	
t_{RAL}†	0	
t_{ARH}	200	448
t_{RAH}††	0	
t_{ARL}	200	848
t_{SUR}	125	
t_{RDH}	152	

*If conditions in † and †† are met, then t_{CY}(typ) = 1200 nsec and t_{CY} max = 1248 nsec.
†If $t_{RAL} \leq 497$ nsec, then no wait states are inserted.
††If $t_{RAH} \leq 200$ nsec, then no wait states are inserted.

WD1002-WX1 Winchester Disk Controller

FEATURES

- 4.95" x 3.85" HALF-SLOT FORM FACTOR
- IBM XT WINCHESTER CONTROLLER EMULATION, IBM PC HOST INTERFACE
- WD10C20 SELF-ADJUSTING DATA SEPARATOR
- DATA RATES UP TO 5 MBITS/SEC
- CONTROLS UP TO 2 DRIVES USING SEAGATE TECHNOLOGY ST506
- SUPPORTS DRIVES OF ANY CONFIGURATION UP TO 1024 CYLINDERS AND 16 R/W HEADS
- 32-BIT ECC POLYNOMIAL FOR ERROR DETECTION AND CORRECTION
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- AUTOMATIC FORMATTING
- 512 BYTES PER SECTOR
- SECTOR INTERLEAVE CAPABILITY
- MULTIPLE SECTOR READS AND WRITES
- INTERNAL DIAGNOSTICS
- DMA TRANSFER CAPABILITY
- AUTO-CONFIGURABLE BIOS ROM
- COMPATIBLE WITH WD1002S-WX2

DESCRIPTION

The WD1002-WX1 Winchester Controller is a half-slot sized IBM XT compatible board designed to interface up to two hard disk drives. The drive interface is based upon the Seagate Technology ST506. The drives need not be of the same capacity or configuration. All necessary receivers and drivers are included on the board to allow direct connection to the drive(s).

The WD1002-WX1 interfaces directly with the Host I/O bus via several interface buses. Data transfer to or from the Controller can be either programmed I/O or DMA.

The WD1002-WX1 is based on the WD1010A-05 Winchester Controller/Formatter, the WD1015 Control Processor, the WD110C0-17 Logic Array, and WD10C20 Data Separator.

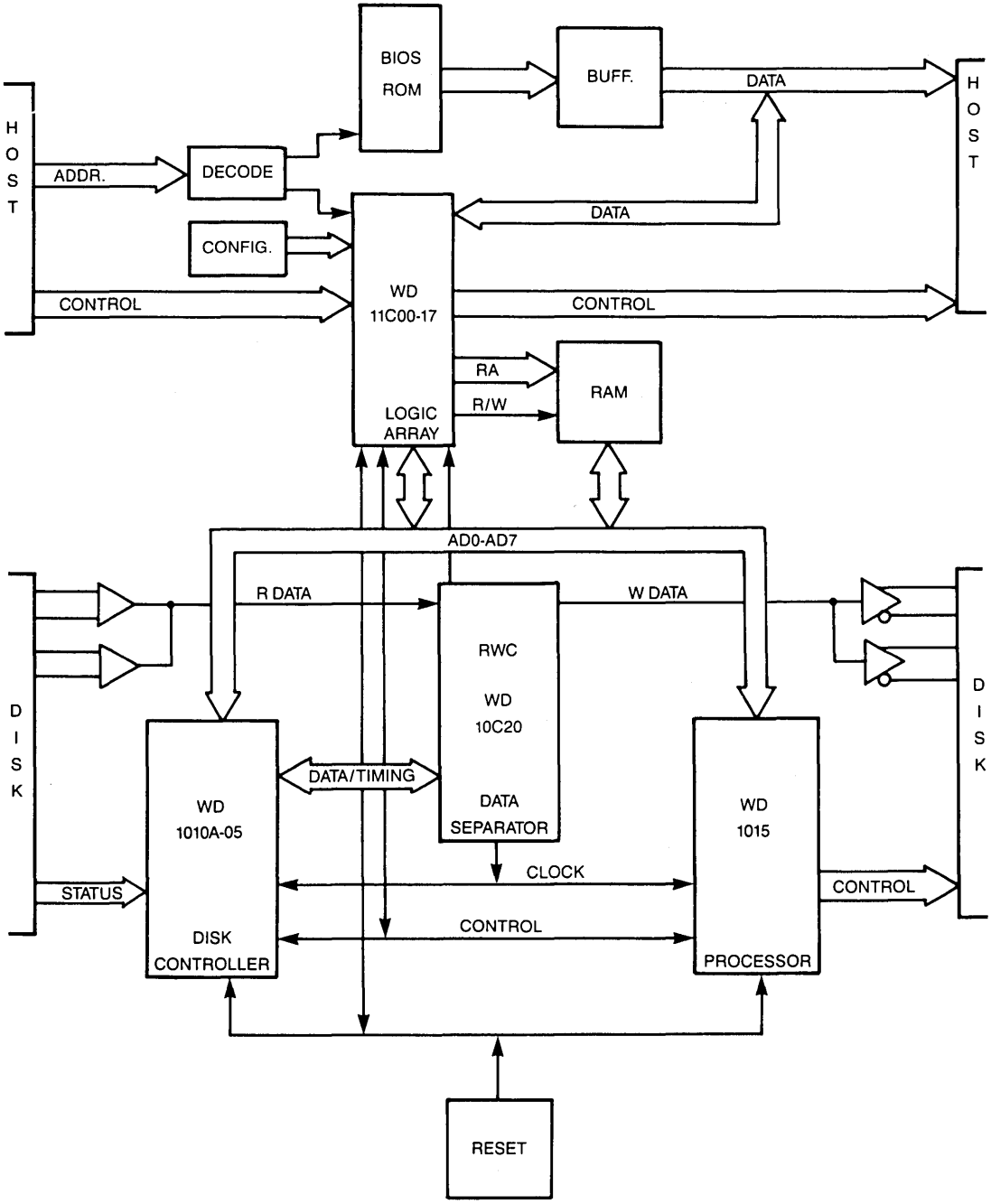
Monitoring of the disk drive status lines is a major function of the WD1010A-05. The WD1010A-05 also controls passage of read and write data between the WD10C20 Data Separator and the other major components of the WD1002-WX1.

The WD1015 controls and coordinates the activity of the disk drive, WD1010A-05, and WD11C00-17. The WD1002-WX1 receives and sends commands or status information over the 8-bit multiplexed address/data bus, AD0 through AD7. Drive control signals select the proper drive and head when enabled by the WD1015.

The WD11C00-17 Logic Array incorporates several functions in a single package. Implementation of these functions occurs by combining random logic and specialized circuits. The WD11C00-17 contains the following circuits

Status ports
Read and write ports
Sector Buffer RAM addressing and control
Disk I/O Control
ECC
Reset Timing

The WD10C20 is a monolithic CMOS Data Separator. This component interfaces the WD1010A-05 to a Winchester disk drive.



WD1002-WX1 BLOCK DIAGRAM

WD1002S-SHD Winchester Disk Controller

FEATURES

- SASI HOST INTERFACE
- BAD TRACK MAPPING CAPABILITY
- MULTIPLE SECTOR READS AND WRITES
- SUPPORTS REMOVABLE MEDIA DRIVES
- AUTOMATIC FORMATTING
- ADJUSTMENT FREE DATA SEPARATOR
- IMPLIED SEEKS
- OVERLAPPED SEEKS
- 3 1/2 INCH FORM FACTOR
- 32-BIT ECC FOR WINCHESTER DATA CORRECTION
- 256 OR 512 BYTES PER SECTOR
- CONTROL FOR EITHER ONE OR TWO WINCHESTER DRIVES, WITH UP TO SIXTEEN READ/WRITE HEADS EACH
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- SELECTABLE INTERLEAVE
- BUILT-IN WRITE PRECOMPENSTION
- SUPPORTS UP TO 16 HEADS

DESCRIPTION

The WD1002S-SHD is a stand alone, general purpose Winchester Disk Controller Board, incorporating the latest state-of-the-art surface mount technology and designed to interface up to two Winchester Disk Drives to a Host Processor. The Winchester Drive signals are based upon the Seagate Technology ST506 interface and other compatible drives. All necessary receivers and drivers are included on the board to allow direct connection to the drive.

Communication to and from the Host are made via a separate computer access port. This port conforms to the Shugart Associates System Interface (SASI) and consists of control signals and an 8-bit, bi-directional bus. All data to be written to or read from the disk, status information, and command parameters are transferred via this bus. An on-board Sector Buffer allows bus transfers to be executed independently of the actual data transfer of the drive.

ARCHITECTURE

The WD1002S-SHD Winchester Disk Controller is based upon a Western Digital proprietary chip set consisting of a: WD1010A-05, WD10C20, WD1015, and the WD11C00-16, all specifically designed for Winchester disk control.

TABLE 1. WD1002S-SHD INTERFACE CONNECTORS

REFERENCE DESIGNATION	INTERFACE FUNCTION	MATING CONNECTOR
P1	POWER	AMP1-480424-0 (Housing) AMP350078-4 4-pin connector
J1	HOST (SASI BUS)	AMP88379-8 50-pin vertical header
J2-J3	DRIVE DATA	AMP88377-4 20-pin vertical header
J4	DRIVE CONTROL	AMP88373-3 34-pin PC card edge connector

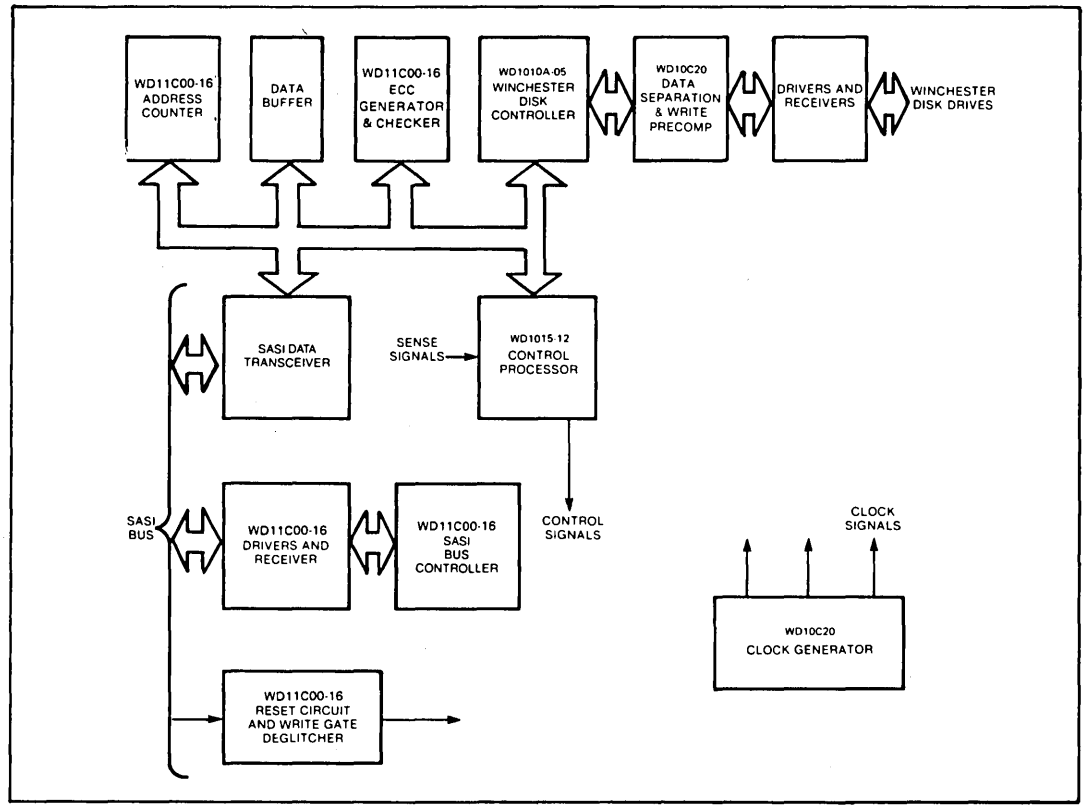


FIGURE 1. WD1002S-SHD WINCHESTER DISK CONTROLLER BLOCK DIAGRAM

SPECIFICATIONS

HOST INTERFACE

Type	SASI
Max Cable Length (Total Daisy Chain)	4.5 meters (15 ft.)
Termination	Socketed 220/330 ohm resistor pack
Addressing	Jumper selectable 0 to 7

DRIVE INTERFACES

Encoding Method	MFM
Cylinders per Track	Programmable
Bytes per Sector	Jumper selectable (256 or 512)
Sectors per Track	32 (256 bytes/sector) 17 (512 bytes/sector)
Max Heads	16
Drive Selects	2
Stepping Rates/Algorythms	Programmable
Data Transfer Rate	5 Mbits/sec
Write Precomp Time	12 nsec
Max Cable Length:	
Control (Total Daisy-Chain)	6 Meters (20 ft.)
Data (Radial-each)	6 Meters (20 ft.)

POWER

Voltage	+5 VDC ± 5% and +12 VDC ± 5%
Current	800 ma typical (1.0 amps max)
Ripple	0.1 to 25 mv (0.1 VDC max)

DATA SEPARATOR

Read Margin	± 16 nsec
Asymmetry	30 nsec measured over 5 MHZ Raw MFM periods of 185, 215, nsec

PHYSICAL

Length	5.75 inches
Width	4.00 inches
Height (max. including board, components & leads)	0.75 inches
MTBF	10,000 POH
MTTR	30 Minutes

ENVIRONMENTAL

Ambient Temperature	0°C (32°) to 55°C (131°F)
Relative Humidity	10% to 90% non-condensing
Altitude	0 to 10,000 Feet (3,048 meters)
Air Flow	150 linear feet per minute at 1/4 inch from compotent surfaces.

HOST INTERFACE

The WD1002S-SHD Winchester Disk Controller is designed to interface with the Shugart Associates System Interface (SASI) Bus. All interfacing is done through the SASI connector (J1). The Host and seven other SASI compatible devices can be daisy-chained to this bus. The last device in the daisy-chain must be terminated with a standard 220/330 ohm resistor pack.

TABLE 2. HOST INTERFACE CONNECTOR (J1) PIN DESCRIPTIONS

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	2	$\overline{DO}$	$\overline{DATA\ 0}$	I/O	8-Bit, bi-directional bus used for the transfer of commands, status and data
3	4	thru	thru		
5	6	$\overline{D7}$	$\overline{DATA\ 7}$		
7	8				
9	10				
11	12				
13	14				
15	16				
17 thru	34	Spare			
35	36	$\overline{BSY}$	$\overline{BUSY}$	O	Falling edge acknowledges receipt of $\overline{SEL}$ and address. Rising edge indicates transaction complete.
37	38	$\overline{ACK}$	$\overline{ACKNOWLEDGE}$	I	Handshake for byte transfers (both edges used).
39	40	$\overline{RST}$	$\overline{RESET}$	I	Asserted for 100 nsec.
41	42	$\overline{MSG}$	$\overline{MESSAGE}$	O	Indicates type of bus transfer (see information Transfer Phase).
43	44	$\overline{SEL}$	$\overline{SELECT}$	I	Asserted, gives control of bus to addressed target.
45	46	$\overline{C}/D$	$\overline{CONTROL}/DATA$	O	Indicates type of bus transfer (see information Transfer Phase).
47	48	$\overline{REQ}$	$\overline{REQUEST}$	O	Handshake for byte transfers (both edges used).
49	50	$\overline{I}/O$	$\overline{IN}/OUT$	I/O	L = Input to the Host H = Output from Host (See information Transfer Phase)

DRIVE CONTROL INTERFACE

The control signals are common to both drives and are daisy chained from a single 34-pin PC card edge connector (J4). To terminate the control signals properly, the last drive in the daisy-chain must not be more than 20 feet from the controller, and have a 220/330 ohm resistor pack installed.

TABLE 3. DRIVE CONTROL CONNECTOR (J4) PIN DESCRIPTIONS

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	2	RWC HS3 CHANGE CART	REDUCE WRITE CURRENT	O	RWC is asserted when the Present Cylinder Number Register is equal to or greater than the content programmed in the Write Precomp Register. It is used by the drive to reduce drift caused by greater bit density on the inner cylinders.
			HEAD SELECT 3	O	HS3 is an optional Head Select line that allows the selection of eight additional heads.
			CHANGECART	O	CHANGECART when activated, will stop the spindle motor. (Removable Media Drives only)
3	4	HS2	HEAD SELECT 2	O	HS2 is one of three Head Select signals encoded by the drive to select one of eight R/W heads.
5	6	WG	WRITE GATE	O	WG is asserted when valid data is to be written. It is used by the drive to enable the write current to the head. WD1002S-SHD de-asserts this signal when WF is asserted. WD1002S-SHD prevents WG from being asserted at power up, allowing the drive to remain ON while cycling the Controller ON or OFF.
7	8	SC	SEEK COMPLETE	I	SC, when asserted, informs the WD1002S-SHD that the selected head has reached the desired cylinder and has stabilized.
9	10	TK000	TRACK 000	I	The drive asserts TK000 when the heads are positioned over the outermost cylinder (Track 0).
11	12	WF	WRITE FAULT	I	WF is asserted by the drive when a write error occurs.
13	14	HSO	HEAD SELECT	O	HSO is one of three Head Select signals encoded by the drive to select one of eight R/W heads.
15	16	RECOVER	RECOVERY MODE		Not Used.
17	18	HS1 WRTSERVO	HEAD SELECT 1	O	HS1 is one of three Head Select signals encoded by the drive to select on of eight R/W heads.
			WRITE SERVO	O	WRTSERVO is used to write servo information on a new cartridge.

TABLE 3. DRIVE CONTROL CONNECTOR (J4) PIN DESCRIPTIONS (CONT'D.)

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
19	20	$\overline{\text{INDEX}}$	$\overline{\text{INDEX PULSE}}$	I	This signal indicates start of a track. It is used as a synchronization point during formatting and as a time out mechanism for retries. This signal pulses once for each revolution of the disk.
21	22	$\overline{\text{DRDY}}$	$\overline{\text{DRIVE READY}}$	I	The drive asserts $\overline{\text{DRDY}}$ when selected and the motor is up to speed.
23	24	$\overline{\text{STEP}}$	$\overline{\text{STEP PULSE}}$	O	$\overline{\text{STEP}}$, with $\overline{\text{DIRIN}}$, positions the heads to the desired cylinder.
25	26	$\overline{\text{DSELO}}$	$\overline{\text{DRIVE SELECT 0}}$	O	$\overline{\text{DSELO}}$ is used to select drive 1.
27	28	$\overline{\text{DSEL1}}$	$\overline{\text{DRIVE SELECT 1}}$	O	$\overline{\text{DSEL1}}$ is used to select drive 2.
29	30	NC	Not Connected		
31	32	NC	Not Connected		
33	34	$\overline{\text{DIRIN}}$	$\overline{\text{DIRECTION IN}}$	O	$\overline{\text{DIRIN}}$ determines the direction the R/W heads take when stepped. Asserted = IN. De-asserted = OUT.

DRIVE DATA INTERFACE

The data is differential and must be connected to each drive with its own cable (J2, J3). It should be a flat ribbon cable, or twisted pair, less than 20 feet long. The connector is a 20-pin vertical header on a 0.1" center.

TABLE 4. DRIVE DATA CONNECTORS (J2,J3) PINS

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
-	1		Not Connected
2	-		Ground
-	3	O	Reinitialize
4	-		Ground
-	5	I	$\overline{\text{Write Protected}}$
6	-		Ground
-	7		Not Connected
8	-		Ground
-	9	I	$\overline{\text{Cartridge Changed}}$
-	10	I	$\overline{\text{Cartridge In}}$
11	-		Ground
12	-		Ground
-	13	O	+ MFM Write Data
-	14	O	- MFM Write Data
15	-		Ground
16	-		Ground
-	17	I	+ MFM Read Data
-	18	I	- MFM Read Data
19	-		Ground
20	-		Ground

POWER CONNECTOR

A 4-pin AMP connector (P1) provides power input to the WD1002S- SHD Controller.

TABLE 5. POWER CONNECTOR (P1) PIN DESCRIPTIONS

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME
	1	+12 Volts (regulated)
2		Ground
3		Ground
	4	+5 Volts (regulated)

DISK DRIVE CONFIGURATION PARAMETERS

Table 6 lists the variable parameters for the major drives supported by the WD1002S-SHD Winchester Disk Controller.

TABLE 6. DISK DRIVE CONFIGURATION PARAMETER VARIATIOINS

MFGR	MODEL #	CYLINDERS	HEADS	REDUCED WRITE CURRENT CYL.	WRITE PRECOMPENSATION CYLINDER
CMI	CM-5205	256 (100)	2	56 (100)	256 (100)
CMI	CM-5410	256 (100)	4	256 (100)	256 (100)
CMI	CM-5616	256 (100)	6	256 (100)	256 (100)
OLI	HD561	180 (B4)	2	128 (80)	180 (84)
OLI	HD562	180 (B4)	2	128 (80)	180 (84)
RMS	503	153 (99)	2	77 (4B)	77 (4B)
RMS	506	153 (99)	4	77 (4B)	77 (4B)
RMS	512	153 (99)	8	77 (4B)	77 (4B)
SEA	ST506	153 (99)	4	128 (80)	64 (40)
SEA	ST412	306 (132)	4	128 (80)	64 (40)
TAN	TM602S	153 (99)	4	128 (80)	153 (99)
TAN	TM603S	153 (99)	6	128 (80)	153 (99)
TAN	TM603SE	230 (E6)	6	128 (80)	128 (80)
TI	5 1/4+	153 (99)	4	64 (40)	64 (40)
RO	101	192 (CO)	2	96 (60)	0 (0)
RO	102	192 (CO)	4	96 (60)	0 (0)
RO	103	192 (CO)	6	96 (60)	0 (0)
RO	104	192 (CO)	8	96 (60)	0 (0)
RO	201	321 (141)	2	132 (84)	0 (0)
RO	202	321 (141)	4	132 (84)	0 (0)
RO	203	321 (141)	6	132 (84)	0 (0)
RO	204	321 (141)	8	132 (84)	0 (0)
MS	1-006	306 (132)	2	153 (99)	0 (0)
MS	1-012	306 (132)	4	153 (99)	0 (0)
DMA	360	306 (132)	2	153 (99)	0 (0)
SYQ	312RO	306 (132)	2	153 (99)	0 (0)

DRIVE MANUFACTURES ABBREVIATIONS:

CMI	Computer Memories Inc.
OLI	Oliveti
RMS	Rotating Memory Systems Inc.
SEA	Seagate Technology Inc.
TAN	Tandon Inc.
TI	Texas Instruments
RO	Rodime Ltd.
MS	Miniscribe
DMA	DMA Systems
SYQ	Syquest Corp.

COMMANDS

The WD1002S-SHD Winchester Disk Controller Board supports 26 different SASI commands; 21 operation commands and 5 diagnostic commands. Table 7 is a summary of the supported commands and their parameters. It also includes information about data transfers required during execution. All other SASI command codes are reserved.

TABLE 7. WD1002S-SHD SUPPORTED COMMAND SUMMARY

COMMAND NAME	CLASS, OPCODE	LUN	LOGICAL SECTOR ADDRESS	INTERLEAV OR BLOCK COUNT	CONTROL BYTE OPTIONS	#SASI DATA BLOCK TRNSFRS	D.B. SIZE	DIREC-TION
Test Drive Ready	0,00	W	- -	- -	- -	0	- -	- -
Restore to Track 0	0,01	W	- -	- -	- -	0	- -	- -
Req. Status	0,03	W	- -	- -	- -	1	4	To Host
Frmt Drive	0,04	W	L*	I	R,P,S,Z	0	- -	- -
Chk Tr Frmt	0,05	W	L*	I	R,S	0	- -	- -
Format Track	0,06	W	L*	I	R,P,S,Z	0	- -	- -
Frmt Bad Trk	0,07	W	L*	I	R,P,S,Z	0	- -	- -
Read	0,08	W	L	B	R,A,S	B	SCTR	To Host
Stop Drive	0,13	W	- -	- -	- -	0	- -	- -
Write	0,0A	W	L	B	R,S	B	SCTR	To CTLR
Seek	0,0B	W	L*	- -	R,S	0	- -	- -
Set Parameters	0,0C	W	- -	- -	- -	1	8	To CTLR
Last Corrected Burst Length	0,0D	W	- -	- -	- -	1	1	To Host
Frmt Alt Trk	0,0E	W	L*	I	R,P,S,Z	1	3	To CTLR
Wr Sct Bfr	0,0F	-	- -	- -	- -	1	SCTR	To CTLR
Rd Sct Bfr	0,10	-	- -	- -	- -	1	SCTR	To Host
Write Servo	6,00	W	- -	- -	- -	0	- -	- -

TABLE 7. WD1002S-SHD SUPPORTED COMMAND SUMMARY (CONT'D)

COMMAND NAME	CLASS, OPCODE	LUN	LOGICAL SECTOR ADDRESS	INTERLEAV OR BLOCK COUNT	CONTROL BYTE OPTIONS	#SASI DATA BLOCK TRNSFRS	D.B. SIZE	DIREC-TION
Reinitialize Cartridge	6,02	W	- -	- -	- -	0	- -	- -
RAM Diag	7,00	-	- -	- -	- -	0	- -	- -
Drive Diag	7,03	W	- -	- -	R,S	0	- -	- -
CTLR Diag	7,04	-	- -	- -	- -	0	- -	- -
RD Long	7,05	W	L	B	R,S	B	SECT +4	To Host
WR Long	7,06	W	L	B	R,S	B	SECT +4	To CTLR

W Winchester
L* Logical sector address used only to specify track
L Logical sector address
I Interleave
B Block count
R Retry enable/disable
A Attempt immediate ECC enable/disable
S Stepping algorithm
P Used with Format commands for determining data field patterns function should be performed.
Z Used with Format commands for determining if a Write Servo function should be performed.

COMMAND BLOCKS

A transaction is initiated by the Host to instruct the WD1002S- SHD Winchester Disk Controller to execute a given command. During the Command Block Transfer Phase, six bytes of information specifying the command are transferred to the WD1002S-SHD Winchester Disk Controller. This is the Command Block and is illustrated in Figure 2.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class			Operation Code				
1	Logical Unit Num			Logical Sector Address(High)				
2	Logical Sector Address (Middle)							
3	Logical Sector Address (Low)							
4	Interleave or Block Count							
5	Control Byte							

FIGURE 2. COMMAND BLOCK FORMAT

Byte 0 is transferred first and must be specified for all commands. Depending upon the value of Byte 0, each parameter in bytes 1 through 5 may require specification.

LOGICAL UNIT NUMBER (LUN)

The LUN is contained in the three MSBits of Byte 1. The allowed values are 0 and 1. The designators in the command table are: Drive 0 (LUN = 0) or Drive 1 (LUN = 1).

LOGICAL SECTOR ADDRESS

The Logical Sector Address (High, Middle, and Low) is a 21-bit field contained in Bytes 1, 2, and 3. It is computed from the Cylinder Addres (C), Head Address (H), and Sector Address (S), as well as the drive parameters Heads per Cylinder (HC) and Sectors per Track (ST):

$$L = ([(C \times HC) + H] \times ST) + S$$

C, H, and S can be derived from L, HC and ST as follows:

$$S = L \text{ Modulo } ST$$
$$H = [(L-S)/ST] \text{ Modulo } HC$$
$$C = ([(L-S/ST] - H)/HC$$

This field specifies a sector (or beginning sector) for the Read and Write drive commands. It specifies a track for the Format and Seek commands (indicated by L* in Table 7). When only a track specification is required, the sector number implied by the Logical Sector Address is ignored.

INTERLEAVE OR BLOCK COUNT

The Interleave or Block Count comprise Byte 4. The Interleave ratio (I in Table 7) is specified in the five Format commands. The maximum ratio is equal to the Sector-per-Track minus 1.

The Block Count (B in Table 7) is specified in the Read, Write, Read Long, and Write Long commands. B specifies the number of Logical Sectors to be transferred.

Both Interleave ratio and Block Count use all 8-bits to specify their respective parameters.

CONTROL BYTES

Table 8 defines the Control Byte fields:

TABLE 8. CONTROL BYTE FIELDS

FIELD	BIT (S)	FUNCTION
STEP	0-3	Used in all commands that contain code corresponding to seek stepping algorithm. See Fast Step Options.
Z	4	Write Servo Information
P	5	Format Data (P) is used in the Format commands. If P=O, the WD1002S-SHD fills the data field with 6C Hex. If P=1, data field is filled with the pattern in the Sector Buffer.
A	6	Immediate ECC (A) is used in the Read command. If A=O, no immediate ECC is performed. If A=1, immediate ECC is performed.
R	7	Retry (R) is used in all commands that read the ID field. If R=0, (normal), a maximum of 3 non-restore retries are performed, then Restore, Seek, and 1 more read is performed. If R=1 Retry is disabled then no retries are performed.

NOTE

If one or more of the above fields are required for a command, then all other fields in that Control Byte must be set to 0. If none of the above are required, all bits in the Control Byte are interpreted as 'don't care' bits (X).

FAST STEP OPTIONS

The Fast Step Option field contains an unsigned 3-bit integer. These integers correspond to the Fast Step Algorithms listed in Table 9.

TABLE 9. FAST STEP OPTION ALGORITHMS

OPTION	ALGORITHM
0	Default: 3 msec. per step
1	Reserved
2	Reserved
3	Reserved
4	200 usec. per step. This is appropriate for buffered steps on drives made by Computer Memories Inc. and Rotating Memories Inc.
5	70 usec. per step
6	30 usec. per step
7	15 usec. per step
8	12μ's per step
9-F	Spare (3 msec. per step)

COMMAND STATUS BYTE

At the completion of any command execution, a Command Status Byte is sent by the WD1002S-SHD to the Host, whether the command was successful or aborted. The LUN returned is the contents of the LUN field in the drive control block. For those commands that do not use LUN as an input parameter, the LUN returned in the Command Status Byte is meaningless. Figure 3 illustrates the contents of the Command Status Byte.

BITS

7	6	5	4	3	2	1	0
LUN			0	0	P	EF	CC

EF (Error Flag): 0 = no error
1 = error
P (Write Protected) = 1
(Removable Media Only)
CC (Cartridge Changed) = 1
0 = Default
1 = CC

FIGURE 3. COMMAND STATUS BYTE

COMMAND COMPLETION BYTE

The Command Completion Byte is an all zero byte sent by the WD1002S-SHD Winchester Disk Controller to the Host immediately following each Command Status Byte. It indicates to the Host that the WD1002S-SHD has freed the SASI Bus.

TEST DRIVE READY (CLASS 0,OP CODE 00)

This command selects a drive and verifies that it is ready. The following is the Test Drive Ready command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 00				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes — No Error, Invalid Command, No Seek Complete, Drive Not Ready, or Write Fault.

Action — Select the drive and determine if it is ready. For a Winchester drive, read its status register and test the ready bit and the busy bit. For Winchester drives supporting buffered seeks, this command is useful for determining the first drive to reach its target track.

RESTORE TO TRACK 0
(CLASS 0, OPCODE 01)

This command positions the read/write heads to Track 0.

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 01				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	0	0	0	X	X	X	X

Possible Error Codes — No Error, Invalid Command,Track 0 Not Found, Drive Not Found, or write Fault.

Action — Position the read/write heads to track 0.

REQUEST STATUS
(CLASS 0, OPCODE 03)

The Host must send this command immediately after it detects an error. The command causes the WD1002S-SHD Winchester Disk Controller to return four bytes of drive and Controller status. When an error occurs during a multiple sector data transfer (read or write), the Request Status command returns the Logical Sector Address of the failing sector in bytes 1, 2, and 3. If the Request Status command is issued after any of the format commands of the Check Track Format command, then the Logical Sector Address points to one sector beyond the last track formatted or checked if there was no error. If there was an error, then the Logical Address returned points to the track in error. The following is the Request Status command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 03				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes — No Error or Invalid Command.

Action — Send the Host 4 bytes; the error byte and a 3-byte Logical Sector Address for the specified drive.

ERROR/STATUS RESPONSE TO HOST

The following non-drive error codes are treated as Drive 0 errors: RAM Failure (30); ROM Failure (31), ECC Hardware Failure (33). If the RAM Diagnostic command or Controller Diagnostic command detects an error, then status for Drive 0 should be requested.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	LSA	0	Error Codes					
1	LUN		Logical Sector Address Bits 16-20					
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							

ERROR CODES

A. DISK DRIVE ERROR CODES

00 = No Error
03 = Write Fault
04 = Drive Not Ready
06 = Track 0 Not Found
07 = Write Protected
09 = Function Not Supported By Drive

B. CONTROLLER ERROR CODES

01, 02, 10/14 = Not used because the WD1010A-05 groups CRC with other errors in ID field as ID not found. During implied seeks, these are called SEEK errors, Code 15.
11 = Uncorrectable Data Error
12 = Address Mark Not Found
15 = Seek Error
18 = Error Burst Corrected
19 = Bad Track
1A = Format Error
1C = Illegal (Direct) Access to an Alternate Track
1D = Alternate Track Already Used
1E = Alternate Track Not Marked as Alternate
1F = Alternate Track Equals Bad Track

C. COMMAND ERROR CODES

0A = Controller Not Initialized
20 = Invalid Command
21 = Invalid Sector Address
22 = Illegal Parameter

D. MISCELLANEOUS ERROR CODES

30 = RAM Failure
31 = ROM Failure
32 = ECC Hardware Failure

If the most recent non-request-status command to the specified drive required a Logical Sector Address, then the LSA flag is 1; otherwise it is 0 and the Logical Sector Address is meaningless.

ERROR CODE DESCRIPTIONS

No Error (00)

No error detected during the previous operation.

Write Fault (03)

Indicates that there is Write Current to the head when WG is deasserted. This is a very serious problem and should be remedied immediately.

Drive Not Ready (04)

The drive does not respond with a Drive Ready signal after being selected by the WD1002S-SHD.

Track 0 Not Found (06)

This error is only returned by the Restore To Track 0 command. It indicates that Track 0 status from the drive was not asserted within the maximum number of steps towards cylinder 0.

Write Protected (07)

Function Not Supported By Drive (09)

Controller Not Initialized (0A)

This occurs when user fails to issue Initialize Format command before issuing any command that accesses the drive.

Uncorrectable Data Error (11)

This error indicates that one or more error bursts within the data field (Winchester) were beyond the Error Correction capabilities of the WD1002S-SHD. The sector data for this sector is not sent to the Host.

Address Mark Not Found (12)

This error indicates that the header for the Target Sector was found, but its Address Mark was not detected.

Seek Error (15)

The WD1002S-SHD detects an incorrect cylinder or track, or both.

Error Burst Corrected (18)

Indicates that ECC was used to successfully correct an error.The corrected sector data is sent to the Host.

Bad Track (19)

This error usually indicates access of a track that was formatted as a bad track. However, there is a very small chance that it indicates that a track formatted as a bad track with alternate is so faulty that none of the multiple, duplicate pointers to the alternate track can be read.

Format Error (1A)

This error code is returned by the Check Track Format command. It indicates that the track is not formatted with the specified interleave factor, or at least one sector header is unreadable. This error code is returned by the Drive Diagnostic command to indicate that bad-track-with-alternate does not contain valid pointer to the alternate track.

Illegal (Direct) Access to an Alternate Track (1C)

Alternate Track Already Used (1D)

This error code is only returned by the Format Alternate Track command. It indicates that the specified alternate track is already an alternate, or bad track.

Alternate Track Not Marked as an Alternate (1E)

This error code indicates that access of a bad-track-with-alternate caused access to an alternate track that was not marked as an alternate.

Alternate Track Equals Bad Track (1F)

This error code is returned only by the Format Alternate Track command. It indicates that the same track was specified as the bad track and the alternate track.

Invalid Command (20)

This error code indicates that the Command Code, Interleave Factor, or Fast Step Option was invalid.

Invalid Sector Address (21)

This error code indicates that the WD1002S-SHD detected a sector address beyond the maximum range.

Illegal Parameter (22)

When Controller detects an invalid parameter or invalid combination of parameters.

RAM Failure (30)

This error code indicates one of the following conditions:

1. The program memory RAM checksum does not match the calculated checksum.
2. The RAM in the Control Processor failed.
3. The Control Processor CPU failed.

ROM Failure (31)

This error code indicates that a ROM checksum error occurred during internal diagnostics.

ECC Hardware Failure (32)

This error code indicates that the ECC Support Device failed during internal diagnostics.

FORMAT DRIVE
(CLASS 0, OPCODE 04)

This command formats all sectors with ID and data fields according to the selected interleave factor. This command also writes 6C Hex into the data fields. The starting address is passed into the Control Byte which is read by the WD1002S-SHD Winchester Disk Controller. The Controller then formats from this address to the end of the disk. The following is the Format Drive command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 04				
1	LUN			Logical Sector Address Bits 16-20				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							
4	Interleave Factor							
5	R	O	P	Z	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

P Format Data: 0 = 6C Hex
1 = Contents of Sector Buffer

Z Write Servo: 0 = Do Not Write Servo
1 = Write Servo Information

NOTE

This is used only for removable media drives that implement the Write Servo function.

Possible Error Codes

No Error, Invalid Command, Invalid Sector Address, Drive Not Ready, Seek Error, or Write Fault.

Action

Format from the specified track to the end of the disk. The previous contents of the formatted tracks are ignored.

CHECK TRACK FORMAT
(CLASS 0,OPCODE 05)

This command checks the format on the specified track for correct ID and interleave. The command does not read the data field. The following is the Check Track Format command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 05				
1	LUN			Logical Sector Address Bits 16-20				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							
4	Interleave Factor							
5	R	O	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Possible Error Codes

No Error, Invalid Command, Invalid Sector Address, Seek Error,Format Error, Drive Not Ready, or Write Fault.

Action

Verify that the specified track is formatted with the specified interleave factor. Do not read the sector data fields.

FORMAT TRACK
(CLASS 0, OPCODE 06)

This comand formats a specified track and can be used to clear bad-sector flags in all sectors on the specified track that was previously formatted with the Format Bad Track command. The command writes 6C Hex into all data fields specified. The following is the Format Track command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 06				
1	LUN			Logical Sector Address Bits 16-20				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							
4	Interleave Factor							
5	R	O	P	Z	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

P Format Data: 0 = 6C Hex
1 = Contents of Sector Buffer

Z Write Servo: 0 = Do not Write Servo
1 = Write Servo Information

Possible Error Codes

No Error, Invalid Command, Invalid Sector Address, Drive Not Ready, Seek Error, or Write Fault.

Action

Format the specified track, ignoring the previous contents.

FORMAT BAD TRACK
(CLASS 0, OPCODE 07)

This command formats the specified track and sets the bad-sector flag in the ID fields. It does not write to the data fields. The following illustrates the Bad Track command block format.

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 07				
1	LUN			Logical Sector Address Bits 16-20				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							
4	Interleave Factor							
5	R	0	0	Z	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Z Write Servo: 0 = Do not Write Servo
1 = Write Servo Information

Possible Error Codes

No Error, Invalid Command, Invalid Sector Address, Drive Not Ready, or Write Fault.

Action

Format the specified track with a bad block mark in each sector header, ignoring the previous contents. The contents of a bad track are not accessible.

READ
(CLASS 0, OPCODE 08)

This command reads the specified number of sectors, starting with the initial Sector Address contained in the Control Byte. The following is the Read command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 08				
1	LUN			Logical Sector Address Bits 16-20				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							
4	Interleave Factor							
5	R	A	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

A Attempt ECC 0 = No Immediate Correction
1 = Immediate ECC

Possible Error Codes

No Error, Invalid Command, Invalid Sector Address, Drive Not Ready, Seek Error, Bad Track, Illegal (direct) Access To Alternate Track, Alternate Track Not Marked As Alternate, Address Mark Not Found, Error Burst Corrected, Uncorrectable Data Error, or Write Fault.

Action

Read the specified number of consecutive sectors beginning with the specified Sector Address contained in the Control Byte.

WRITE
(CLASS 0, OPCODE 0A)

This command writes the specified number of sectors, beginning with the initial sector address contained in the Control Byte. The following is the Write command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 0A				
1	LUN			Logical Sector Address Bits 16-20				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							
4	Interleave Factor							
5	R	0	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Possible Error Codes

No Error, Invalid Command, Invalid Sector Address, Drive Not Ready, Seek Error, Bad Track, Illegal (direct) Access to Alternate Track, Alternate Track Not Marked As Alternate, Address Mark Not Found, or Write Fault.

Action

Write the specified number of sectors beginning with the specified Sector Address contained in the Control Byte.

SEEK
(CLASS 0, OPCODE 0B)

This command initiates a seek to the track specified in the Control Byte. The drive must be formatted.

The following is the Seek command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 0B				
1	LUN			Logical Sector Address Bits 16-20				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							
4	X	X	X	X	X	X	X	X
5	R	0	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Possible Error Codes

No Error, Invalid Command, Invalid Sector Address, Drive Not Ready, or Write Fault.

Action

Move the read/write head to the specified cylinder. Do not read any sector header to verify start or end position.

SET PARAMETERS
(CLASS 0, OPCODE 0C)

This command enables the Host to configure the WD1002S-SHD Winchester Disk Controller to work with drives that have different capacities and characteristics. However, both Drive 0 and Drive 1 must be of the same manufacturer and model number. The following is the Set Parameters command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 0C				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

If parameters are out of range, an Invalid Command error will be set.

Action

Set the following parameters for both Winchester drives (LUN 0 and 1): Number of cylinders, Number of heads; Starting Reduced Write Current cylinder, Starting Write Precompensation cylinder, and the maximum length of an error burst to be corrected. These parameters are sent by the Host to the WD1002S-SHD Winchester Disk Controller in a parameter block with the following format:

PARAMETER BLOCK

After the Host sends the Set Parameters command block to the WD1002S-SHD Winchester Disk Controller, it then sends an 8-byte block of data that contains the required drive parameters. Some parameters occupy two bytes; all two-byte parameters are transferred with the Most Significant Byte first. The following is the 8-byte Parameter block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	MSByte of Number of Cylinders							
1	LSByte of Number of Cylinders							
2	0	0	0	0	Number of Heads			
3	MSByte of Starting RWC Cylinder							
4	LSByte of Starting RWC Cylinder							
5	MSByte of Starting Write Precomp Cylinder							
6	LSByte of Starting Write Precomp Cylinder							
7	0	0	0	RD	Max ERR Burst Corrected			

RD (Removable Media Drive) 0 = Fixed
1 = Removable

The following parameter defaults are set by Power-UP and Reset:

Number of cylinders = 153
Number of heads = 4
Starting Reduced Write Current Cylinder = 128
Starting Write Precompensation Cylinder = 64
Maximum length of an error burst to be corrected = 11

The acceptable ranges of the following parameters are as follows:

Number of cylinders = 1 - 1024
Number of heads = 1 - 16
Starting Reduced Write Current Cylinder = 1 - 1023
Starting Write Precompensation Cylinder = 0 - 1023
Maximum length of an error burst to be corrected = 1 - 11

If one of the parameters is out of range, then all parameters up to, but not including the parameter in error, are set for Drive 0 and no parameteres are set for Drive 1. The error code for this error is Invalid Command.

Starting Reduced Write Current Cylinder

The specified starting Reduced Write Current cylinder number is reduced to the nearest integer multiple of four (i.e., 0, 4, 8, 12,. . .1020).

Maximum Length of Error Burst To Be Corrected

For practically all applications,the maximum length of the error burst to be corrected should be five. Correcting longer burst greatly increases the chance of miscorrecting.

LAST CORRECTED BURST LENGTH (CLASS 0, OPCODE 0D)

This command transfers one byte to the Host containing the values of the ECC burst length detected by the WD1002S-SHD during the last Read command. This byte is valid only after a correctable ECC error (18).

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 0D				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No Error.

Action

Send the Host one byte of data containing the length of the most recently corrected error burst. If no error burst has been corrected since the last Power-UP or Reset, then a byte of zeros is sent to the Host.

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Number of bits in Last Corrected Error Burst							

FIGURE 4. ERROR BURST LENGTH BLOCK

FORMAT ALTERNATE TRACK (CLASS 0, OPCODE 0E)

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 0E				
1	LUN			Logical Sector Address Bits 16-20				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							
4	Interleave Factor							
5	R	0	P	Z	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

P Format Data: 0 = 6C Hex
1 = Contents of Sector Buffer

Z Write Servo: 0 = Do not Write Servo
1 = Write Servo Information

Possible Error Codes

No Error, Invalid Command, Invalid Sector Address, Drive Not Ready, Seek Error, Alternate Track Already Used, Alternate Track Equals Bad Track, or Write Fault.

Action

Format the specified track as a bad-track-with-alternate. Format the specified alternate track with the specified interleave factor. The Bad Block Mark is written in each sector header with the alternate address block written into each sector data field. This is done to all sectors of the track. It is not known to the user which sector of the track might be bad. The alternate track is specified by the Host by sending an alternate sector address block to the WD1002S-SHD after the command block. The alternate track is formatted after the bad track-with-alternate is formatted. Once the alternate is formatted, the bad track to alternate seeking is transparent to the user.

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	Logical Sector Address Bits 16-20				
1	Logical Sector Address Bits 8-15							
2	Logical Sector Address Bits 0-07							

FIGURE 5. ALTERNATE SECTOR ADDRESS BLOCK

WRITE SECTOR BUFFER (CLASS 0, OPCODE 0F)

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 0F				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No Errors.

Action

Write data from the Host to the WD1002S-SHD Winchester Disk Controller Sector Buffer. The Host must send as many bytes as there are in a sector on Drive 0. These data are not written to any drive. This command is used to initialize the format data optionally used by the Format commands.

READ SECTOR BUFFER (CLASS 0, OPCODE 10)

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 10				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No Error.

Action

Send the Host the present contents of the WD1002S-SHD Winchester Disk Controller Sector Buffer. The Host must accept as many bytes as there are in a sector on Drive 0.

STOP DRIVE
(CLASS 0, OPCODE 13)

This command causes a removable cartridge disk drive to spin down and stop so the user can change the cartridge. After the cartridge is changed, the drive must be started by external means. Software can check for completion of the cartridge change by using the Test Drive Ready command. The format for the Stop Drive command is as follows:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 0			Operation Code 13				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes
Function Not Supported By Drive.

Action
Spins down drive to allow user to change removable cartridge.

WRITE SERVO
(CLASS 6, OPCODE 00)

The Write Servo command completely erases the existing servo information and all other data on the disk, then rewrites the servo information. This provides optimum alignment between cartridge and drive (and may enhance seek performance) as each cartridge can be servo written by the drive in which it is to be used.

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 6			Operation Code 00				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes
Function Not Supported By Drive.

REINITIALIZE CARTRIDGE
(CLASS 6, OPCODE 02)

This command provides a servo reinitialization cycle wherin track location and disk runout information are reprogrammed in the drive microprocessor. This function may be employed by the Host system to improve Seek error rate, and is automatically provided on a power-UP sequence or after a cartridge change.

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 6			Operation Code 02				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

Function Not Supported By Drive.

RAM DIAGNOSTIC
(CLASS 7, OPCODE 00)

This command performs a data pattern test on the Sector Buffer. The Host does not preserve the contents of the Sector Buffer.The following is the RAM Diagnostic command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 7			Operation Code 00				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No Error or RAM failure.

Action

Test the Sector Buffer by writing and reading various patterns into it.

DRIVE DIAGNOSTIC
(CLASS 7, OPCODE 03)

This command tests both the drive and the drive-to-Controller interface. The WD1002S-SHD Winchester Disk Controller sends Restore to Track 0 and Seek commands to the selected drive and verifies Sector 0 of all tracks on the disk. The WD1002S-SHD Winchester Disk Controller does not perform any write operations during this command; the disk is understood to be previoulsy formatted. The following is the Drive Diagnostic command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 7			Operation Code 03				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	R	0	0	0	Fast Step Option			

Possible Error Codes

No Error, Invalid Command, Drive Not Ready, Seek Error, Format Error, or Write Fault.

Action

Recalibrate the target drive, then scan ID on each track. This command does not write to the disk, nor does it send any sector data to the Host. The effect of the Drive Diagnostic command is to verify that at least one sector header can be read on each track. It does not report an error when it encounters a track that has been formatted as a 'Bad Track', 'Bad-Track-With-Alternate', or 'Alternate Track'.

CONTROLLER DIAGNOSTIC
(CLASS 7, OPCODE 04)

This command initiates the WD1002S-SHD self-test diagnostic routine. The WD1002S-SHD tests its Control Processor, Sector Buffer, ECC circuitry, Winchester Controller/Formatter, and the checksum of the Program Memory. The WD1002S-SHD does not access the drive during this command. The following is the Controller Diagnostic command block format.

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 7			Operation Code 04				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No Error, ROM Failure, RAM Failure, or ECC Hardware Failure.

Action

Calculate a checksum for the program ROM, test the Control Processor, test the Sector Buffer, and test the ECC hardware. This command does not access any disk drive.

READ LONG
(CLASS 7, OPCODE 05)

This command transfers the target sector and four bytes of data ECC to the Host. If an ECC error occurs during Read, the WD1002S- SHD does not attempt to correct the data field. The command is useful in recovering data from a sector that contains an uncorrectable ECC error. It is also useful during diagnostic operations.

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 7			Operation Code 05				
1	LUN			Logical Sector Address Bits 16-20				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							
4	Sector Count							
5	R	0	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Possible Error Codes

No Error, Invalid Command, Invalid Sector Address, Drive Not Ready, Seek Error, Bad Track, Illegal (direct) Access To An Alternate Track, Alternate Track Not Marked As Alternate, Address Mark Not Found, or Write Fault.

Action

Read the specified number of consecutive sectors and their ECC bytes beginning with the specified sector contained in the Control Byte. There are four ECC bytes per sector. This command is only useful for diagnostic purposes.

WRITE LONG
(CLASS 7, OPCODE 06)

This command transfers a sector of data and four appended ECC bytes to the disk drive. During this write operation, the Host supplies the four ECC bytes instead of the usual hardware generated ECC bytes.

This command is useful only for diagnostic routines. The following is the Write Long command block format:

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 7			Operation Code 06				
1	LUN			Logical Sector Address Bits 16-20				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-07							
4	Sector Count							
5	R	0	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Possible Error Codes

No Error, Invalid Command, Invalid Sector Address, Drive Not Ready, Seek Error, Bad Track Illegal (direct) Access To Alternate Track, Alternate Track Not Marked As Alternate, Address Mark Not Found, or Write Fault.

Action

Write the specified number of consecutive sectors beginning with the specified sector. Following each sector, the Host sends four ECC bytes to the WD1002S-SHD Winchester Disk Controller to be written to the disk as the ECC bytes for the sector. This command is useful for diagnostic purposes. It allows the generation of a sector containing a correctable ECC error.

TIMING

Figure 6 illustrates a typical Host-Controller bus transfer, complete with Controller selection.

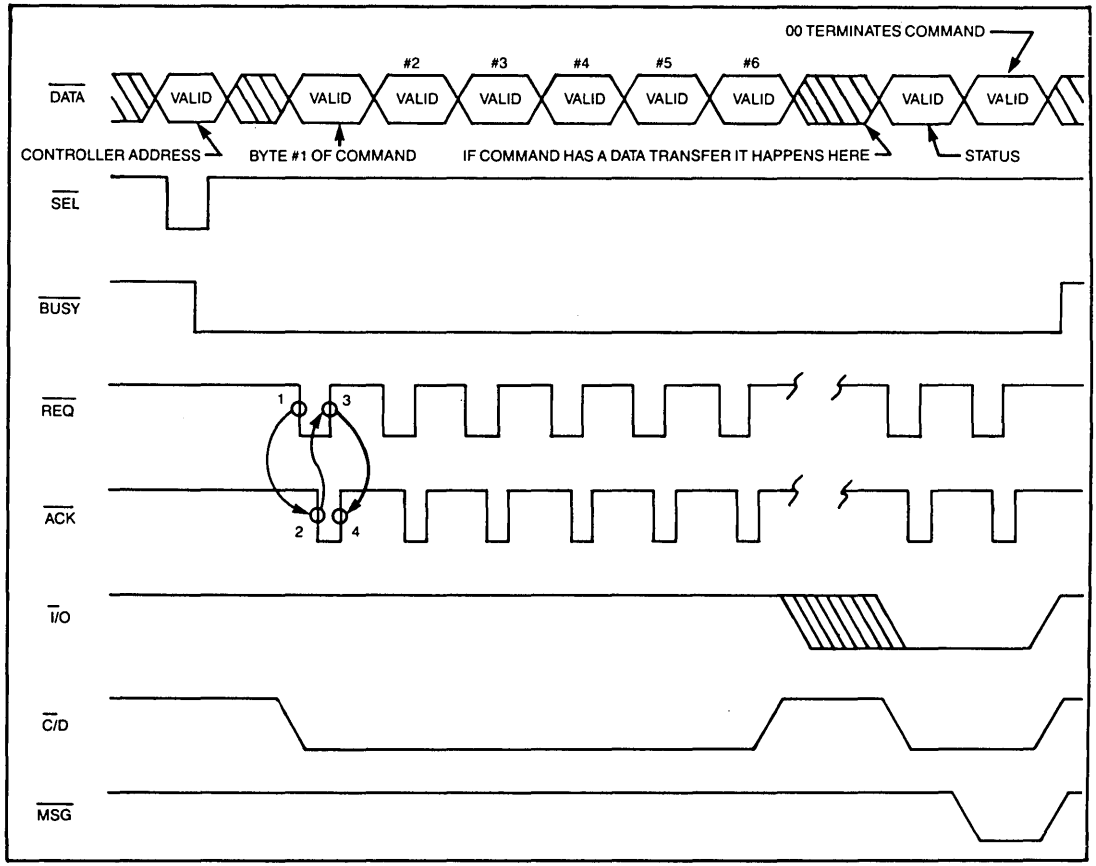


FIGURE 6. TYPICAL HOST-CONTROLLER BUS TRANSFER TIMING

HOST/CONTROLLER SELECTION TIMING

Prior to either command or data transfer, the Host must perform a handshake operation in selecting the Controller. The Host first asserts $\overline{SEL}$ and places the Controller address bit on the bus (the address bit is preset to DB0 at the factory but can be any bit from DB0 to DB7 in a multiple-Controller environment).

After the controller recognizes its address bit and $\overline{SEL}$ being asserted, it then asserts $\overline{BUSY}$. During this selection phase, the Host takes full control of the data bus by asserting O (I/O). Once the Controller has asserted $\overline{BUSY}$, the selection process is complete. $\overline{SEL}$ must be de-asserted by the Host at or before the first Command byte to the Controller. Figure 7 illustrates the Controller Select Timing. Figure 8 illustrates the Controller Select Timing Flow.

NOTE

No restriction on sequence of $\overline{SEL}$ and $\overline{DADR}$ falling edges. Both must be low to ensure controller selection.

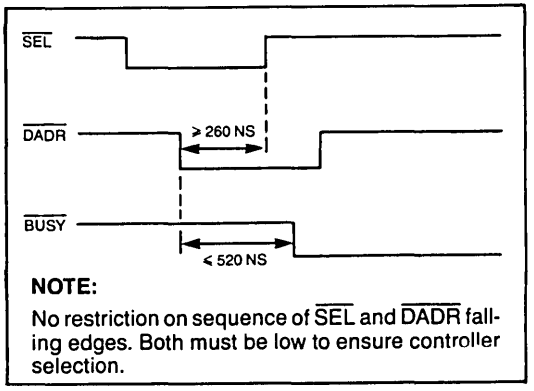


FIGURE 7. CONTROLLER SELECT TIMING

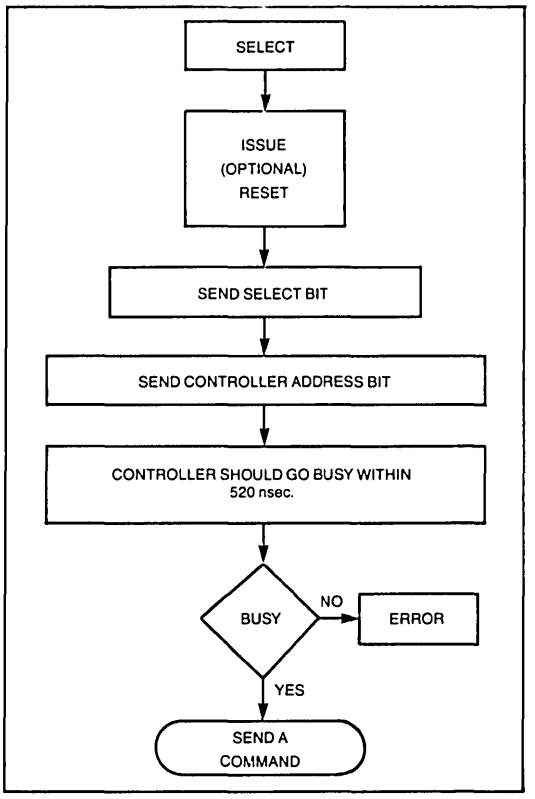


FIGURE 8.
CONTROLLER SELECT FLOW DIAGRAM

COMMAND MODE

After Controller selection, the Host can transmit its first command. The Controller receives a command form the Host using a sequence of handshake recognition signals. The Controller asserts C (C/D) to notify the Host that it is ready to receive a command and assets O (I/O) to indicate that the direction is from the Host to the Controller. At this time, MSG is in the de-asserted state.

The Controller asserts REQ within 10 usec. After asserting O (I/O), C (C/D), and MSG is in the de-asserted state. The Host then answers by asserting ACK when it is ready to send a command byte to the Controller. The command byte must be stable on the bus within 250 nsec. of ACK being asserted and remain stable until the Controller de-asserts REQ. After the Controller de-asserts REQ, the Host de-asserts ACK completing the handshake sequence for the first command byte. The complete handshake sequence must be repeated for each successive command byte from the Host. Table 9 lists the relationships of I/O, C/D, and MSG.

TABLE 9. HOST BUS SIGNAL STATUS

I/O	C/D	MSG	BUS STATUS
1	0	1	The Controller receives a command from the Host.
1	1	1	The Controller receives data from the Host.
0	1	1	The Controller sends data to the Host.
0	0	1	The Controller sends an error status byte to the Host.
0	0	0	The Controller informs the Host that it has completed the command in process.

DATA TRANSFER

Figures 9 and 10 illustrate the required timing for Host-to-Controller and Controller-to-Host data transfers respectively. These diagrams include the required handshake signals. Tables 10 and 11 provide the timing parameters for these diagrams.

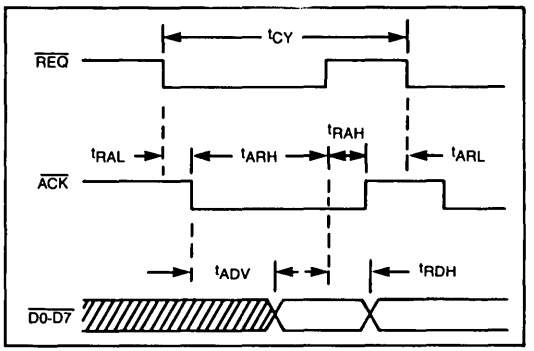


FIGURE 9.
HOST-TO-CONTROLLER
DATA TRANSFER TIMING

TABLE 10.
HOST-TO-CONTROLLER
TIMING PARAMETERS

PARAMETER	MIN*	MAX*
t_{CY}**	1152	
t_{RAL}†	0	
t_{ARH}	600	840
t_{RAH}††	0	
t_{ARL}	200	448
t_{ADV}		375
t_{RDH}	0	

LEGEND:

* nsec

** If conditions in † and †† are met, then $t_{CY}t_{YP}$ = 1200 nsec and t_{CY} max = 1248 nssec.

† If $t_{RAL} < 89$ nsec, then no wait states are inserted.

†† If $t_{RAH} < 97$ nsec, then no wait states are inserted.

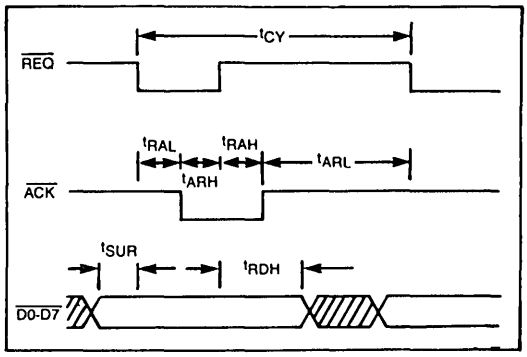


FIGURE 10.
CONTROLLER-TO-HOST
DATA TRANSFER TIMING

TABLE 11.
CONTROLLER-TO-HOST
TIMING PARAMETERS

PARAMETER	MIN*	MAX*
t_{CY}**	1152	
t_{RAL}†	0	
t_{ARH}	200	448
t_{RAH}††	0	
t_{RAL}	200	848
t_{SUR}	125	
t_{RDH}	152	

LEGEND:

* nsec

** If conditions in † and †† are met, then $t_{CY}t_{YP}$ = 120 nsec and t_{CY} max = 1248 nsec.

† If t_{RAL} < 497 nsec, then no wait states are inserted.

†† If t_{RAH} < 200 nsec, then no wait states are inserted.

STATUS BYTES

After every command, the Controller sends two status bytes to the Host. The first byte of information contains the error status code for that command and the second byte contains all zeros, indicating that the command has been completed. Figure 11 illustrates the timing sequence for Command Termination. Figure 12 illustrates the timing flow for sending and terminating a command, and Figure 13 illustrates Status Request Timing Flow.

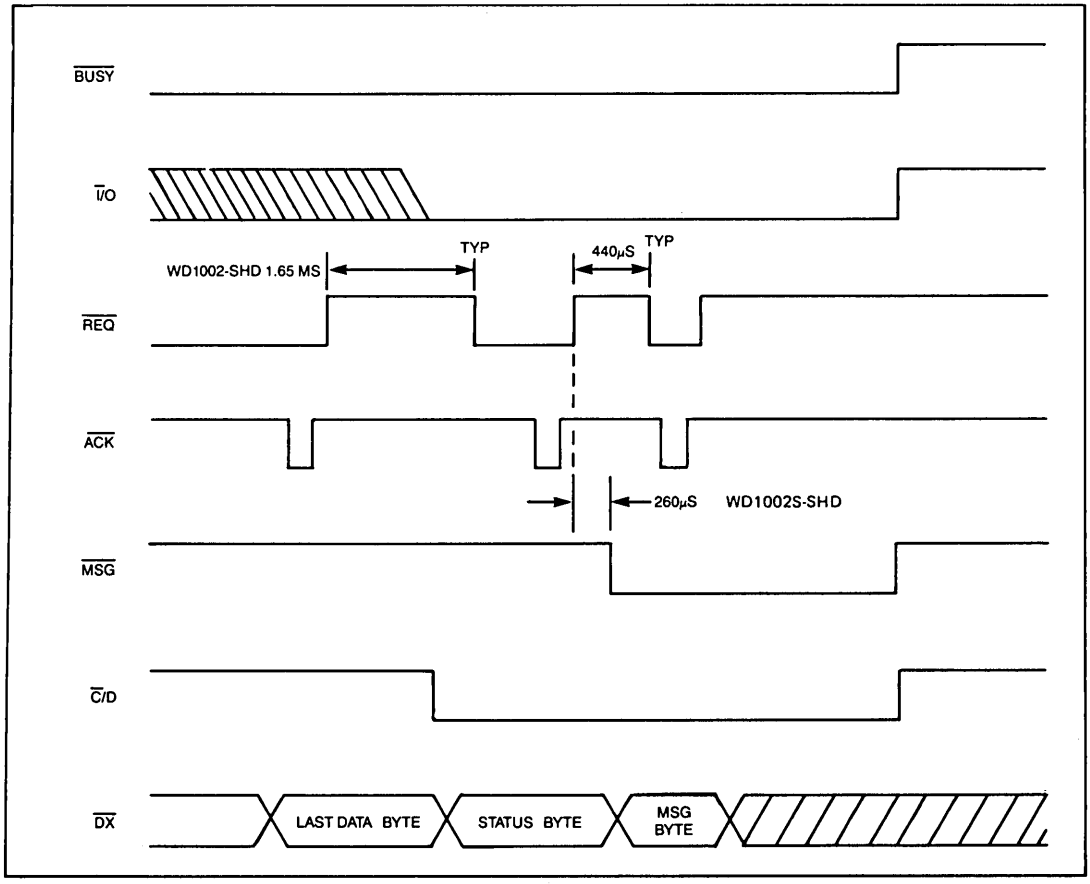


FIGURE 11. COMMAND TERMINATION TIMING

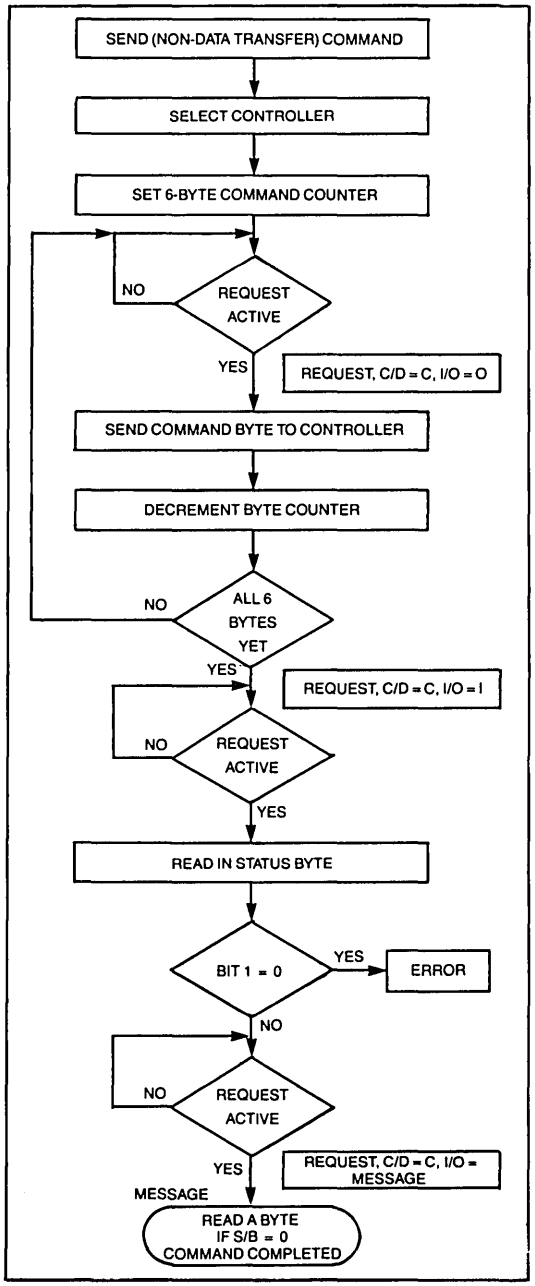


FIGURE 12.
COMMAND SEQUENCE
TIMING FLOW DIAGRAM

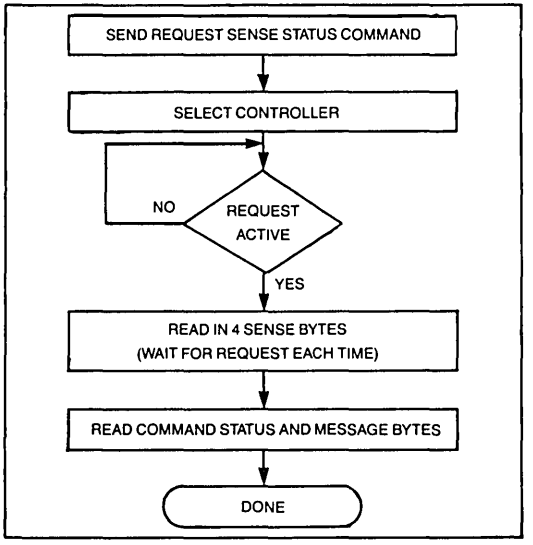


FIGURE 13.
REQUEST STATUS COMMAND
TIMING FLOW DIAGRAM

MISCELLANEOUS TIMING

The following is a list of specific timing parameters that must be met for proper operation of the WD1002S-SHD:

A. **CONTROLLER RESET** – Power-On-Reset (POR) is less than 120 msec. and Reset ($\overline{RST}$) is less than 120 usec. During either of these periods, the Host is inhibited from selecting the Controller. If selection is attempted, the Controller does not assert BUSY.

B. **SELECT TO $\overline{C}$/D** – After $\overline{RST}$ or POR, the Controller runs its internal diagnostic routines until it is selected by the Host, at which point the Controller exits the diagnostic routine being run. While in the diagnostic loop, the controller can take as long as 340 msec. After it asserts $\overline{BUSY}$, before asserting $\overline{C}$ ($\overline{C}$/D). However, once the Controller has left the diagnostic loop, no more than 80 usec. is required for the Controller to assert $\overline{C}$ ($\overline{C}$/D) after $\overline{BUSY}$ is asserted.

C. **$\overline{C}$/D TO FIRST $\overline{REQ}$ TIMING PULSE** – When the Controller first asserts $\overline{C}$ ($\overline{C}$/D) until the first $\overline{REQ}$ pulse is asserted is typically 120 usec.

D. **WAIT STATE** – One wait state equals 200 nsec.

NOTE

All $\overline{SASI}$ protocol must be adhered to (i.e., a $\overline{RE}$/$\overline{ACK}$ handshake must precede every byte transferred).

WD1002C-WX2
Winchester Controller Board

FEATURES

- IBM XT WINCHESTER CONTROLLER EMULATION, IBM PC HOST INTERFACE.
- EITHER 50 PIN EXTERNAL CONNECTOR OR 62 PIN EXTERNAL CONNECTOR.
- SUPPORTS MULTIPLE STEPPING RATES, INCLUDING 18 USEC.
- DYNAMICALLY CONFIGURABLE BIOS ROM
- SUPPORTS TWO ST506 TYPE DRIVES WITH UP TO 1024 CYLINDERS AND 16 R/W HEADS.
- ERROR DETECTION AND CORRECTION ON DATA FIELD USING 32-BIT ECC POLYNOMIAL
- AUTOMATIC FORMATTING.
- WD10C20-05 SELF-ADJUSTING LSI DATA SEPARATOR.
- SECTOR INTERLEAVE CAPABILITY.
- OVERLAPPED SEEK CAPABILITY ON BUFFERED-STEP DRIVES.
- SUPPORTS IMPLIED SEEKS ON ALL COMMANDS.
- DMA TRANSFER CAPABILITY.

DESCRIPTION

The WD1002C-WX2 is an IBM XT compatible Winchester controller board based on the design of the WD1002S-WX2. The WD1002C-WX2 is a 10 inch x 3.90 inch board and includes either a 50 pin external connector or a 62 pin external connector. The connector allows the user to configure a system easily with external Winchester drives. The board contains one internal connector and one external connector and a maximum of 2 drives can be attached. The 50-pin external connector will control one external drive configured as Drive 0 or Drive 1. The 62 pin connector carries all the signals required to control up to two external drives. In either case, the maximum number of drives supported is two, so if the 62 pin connector has 2 drives attached, no drive may be attached to the internal connector.

The WD1002C-WX2 supports drives with up to 16 heads and supports the following stepping rates: 3 msec, 18 μsec, 30 μsec, 45 μsec, 60 μsec, 75 μsec and 210 μsec.

The WD1002C-WX2 interfaces directly to the Host I/O via the IBM PC bus. Data transfer to and from the controller can be either programmed I/O or DMA.

The BIOS is dynamically configurable at the time of formatting the drive. The user has two options: to use a resident set of drive tables, or to define through the keyboard a new set of customized tables.

WD1002S-WX2 Winchester Disk Controller

FEATURES

- 8-BIT BI-DIRECTIONAL BUS HOST INTERFACE.
- IBM XT WINCHESTER CONTROLLER EMULATION, IBM PC HOST INTERFACE
- WD10C20 WINCHESTER DATA SEPARATOR AND WRITE PRECOMPENSATION DEVICE
- WD11C00-17 LOGIC ARRAY
- DATA RATES UP TO 5 MBITS/SEC
- CONTROLS UP TO 2 DRIVES USING SEAGATE TECHNOLOGY ST506/ST412
- SUPPORTS DRIVES OF ANY CONFIGURATION UP TO 1024 CYLINDERS AND 16 R/W HEADS WITH THE WD1015-24 OR 8 R/W HEADS WITH THE WD1015-14
- THE CONTROLLED DRIVES NEED NOT BE OF THE SAME CAPACITY OR CONFIGURATION
- ERROR CORRECTION ON DATA FIELD ERRORS, CRC ID FIELD VERIFICATION
- 32-BIT ECC POLYNOMIAL FOR ERROR DETECTION AND CORRECTION
- READ AND WRITE LONG COMMANDS FOR CHECKING ERROR CORRECTION CIRCUITRY
- SELECTABLE AUTOMATIC RETRIES ON ALL ERRORS
- AUTOMATIC RESTORE AND RE-SEEK ON ALL SEEK ERRORS
- AUTOMATIC FORMATTING
- 512 BYTES PER SECTOR
- SECTOR INTERLEAVE CAPABILITY
- MULTIPLE SECTOR READS AND WRITES
- OVERLAPPED SEEK CAPABILITY ON BUFFERED-STEP DRIVES
- SUPPORTS IMPLIED SEEKS ON ALL COMMANDS
- INTERNAL DIAGNOSTICS
- DMA TRANSFER CAPABILITY
- SUPPORTS INTERRUPTS, INTERRUPT REQUESTS, AND DMA REQUEST SHARING
- INCLUDES SOCKET FOR USER SUPPLIED 2716, 2732, OR 2764 ROM
- BIOS AVAILABLE

DESCRIPTION

The WD1002S-WX2 is a stand-alone, general purpose Winchester Disk Controller. The WD1002S-WX2 interfaces up to two Winchester disk drives and a Host Processor, e.g. an IBM XT.

The Winchester interface conforms to the Seagate Technology ST506/ST412 interface. All necessary receivers and drivers are included on the board, allowing direct connection to the disk drive(s).

A separate computer access port enables communications between the Host and disk controller. An 8-bit bi-directional bus and appropriate control signals comprise this port. Disk read or write data, status information, and command parameters are transferred via this bus. An on-board data buffer allows bus transfers to be executed independently of the drive's data transfer.

ARCHITECTURE

The WD1002S-WX2 architecture is based on a proprietary chip set consisting of the WD11C00-17, WD1010A-05, WD10C20, and WD1015. As illustrated in Figure 1, the WD1002S-WX2 consists of the following components:

Bi-directional Control/Data Bus
Address Decoding Logic
Configuration Switches
Basic Input/Output System (BIOS) ROM
WD11C00-17
WD10C20
Sector Buffer RAM
WD1010A-05
WD1015
Reset Logic

BI-DIRECTIONAL CONTROL/DATA BUS

The 8-bit, bi-directional bus transmits addresses, commands, data, and status information. This bus links the WD1002S-WX2 to the Host. Specifically, this bus transmits data between the Host and Sector Buffer RAM.

ADDRESS DECODING LOGIC

The purpose of this logic is to decode a valid device address from the Host.

CONFIGURATION JUMPERS

These jumpers configure the WD1002S-WX2 for different disk drive capacities.

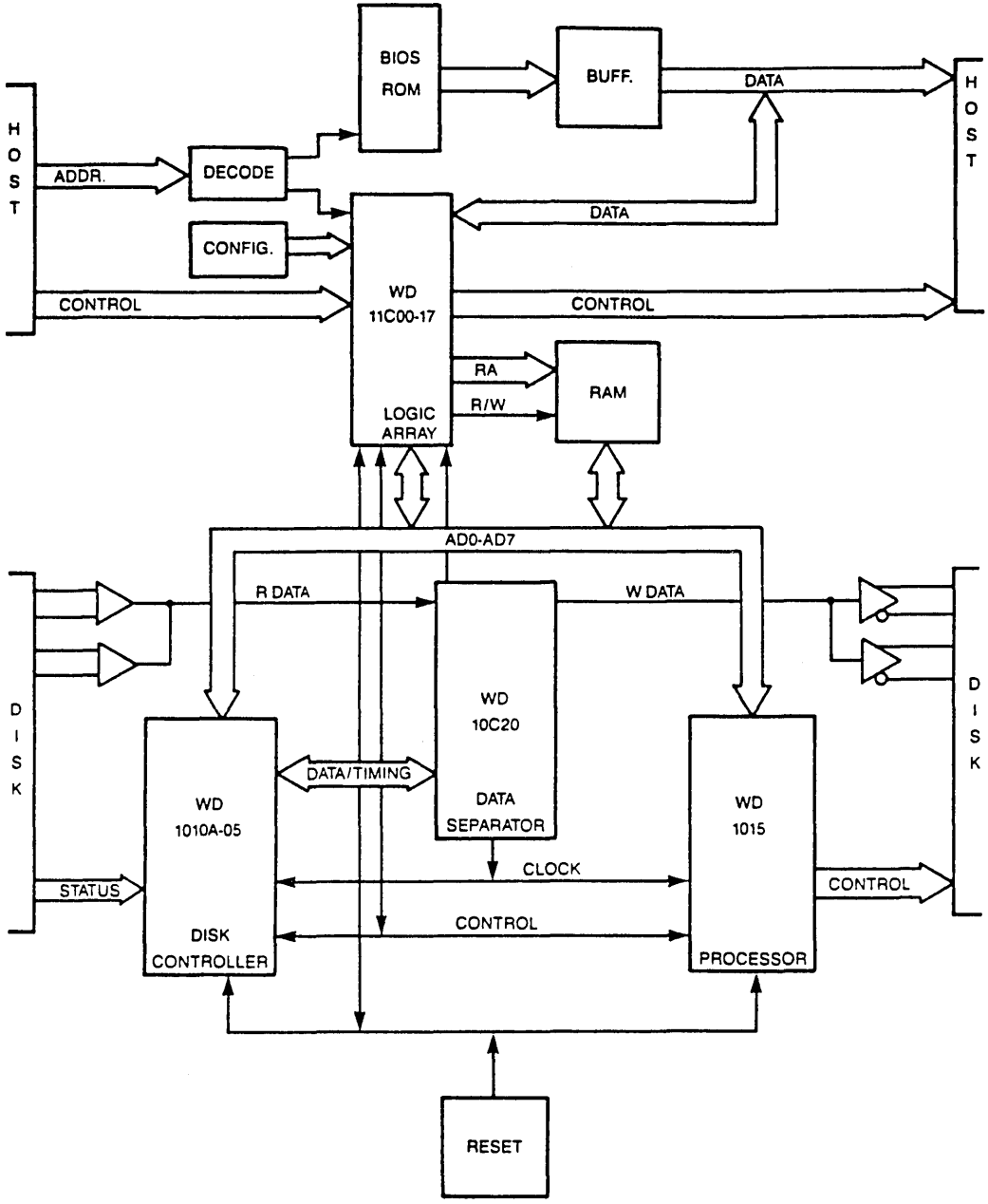


FIGURE 1. WD1002S-WX2 FUNCTIONAL BLOCK DIAGRAM

BIOS ROM

The Host, after powering up, interrogates its ports to determine what devices are connected. The Host uses information supplied by the BIOS ROM to perform an install operation. Then, during normal operation, the BIOS operates much like a driver that is resident in the Host's memory space. The BIOS ROM is addressed at Host memory locations C8000 - C8FFF. The BIOS is addressed by the A0 through A19 bus. Outputs to the Host are via the Intraboard Command/Status bus (BD0 through BD7) and Host Interface Data/Command bus (D0 through D7).

WD11C00-17

The WD11C00-17 incorporates several functions in a single package. Implementation of these functions occurs by combining random logic and specialized circuits. The WD11C00-17 contains the following circuits:

Status ports
Read and write ports
Sector Buffer RAM addressing and control
ECC
Reset timing

The WD11C00-17 connects directly to the Host Interface Data/Command and Intraboard Command/Data (AD0-AD7) buses.

WD10C20

The WD10C20 performs phase-locked loop data synchronization on read data from the Winchester drives. This device also conditions write data to be recorded on the disk. The WD10C20 includes both frequency and phase detection. Zero phase error start-up circuitry eliminates problems due to asymmetry. The WD10C20 requires no adjustments and contains all data synchronization and write precompensation circuitry in a single device.

SECTOR BUFFER RAM

The Sector Buffer RAM is a 2K x 8 RAM. The Sector Buffer allows Host data transfers independent of the actual drive data transfer rate. The Sector Buffer temporarily stores the following information:

Sector data during Read and Write Commands
Disk format information during a Format Command
Drive characteristics during a Set Parameters Command

WD1010A-05

The primary function of the WD1010A-05 is to control data transfers between the disk and the Sector Buffer. Data transfers take place after the WD1015 Buffer Manager Control Processor positions the selected head over the desired track. The WD1010A-05 receives the parameters and commands from the WD1015 via the AD0 through AD7 bus. The WD1010A-05 interprets the parameter or command, determines which sectors are involved, and whether a read, write, or format function is required.

WD1015

The WD1015 manages and controls all commands and communications between the Host and WD1010A-05. The WD1015 controls ECC and CRC functions.

There are two versions of the WD1015. Table 1 describes the differences between the two versions of the WD1015. The acronym WD1015 refers to both versions. When a specific reference is made to a specific version, the appropriate acronym is used.

Table 1. WD1015 DESCRIPTION

FUNCTION	WD1015-14	WD1015-24	REMARKS
Execution of automatic self-test after Reset command or power-up	Yes	No	
Supports 16 heads	No	Yes	The WD1015-14 supports up to eight heads. The WD1015-14 uses the REDUCED WRITE CURRENT (RWC) signal. The WD1015-24 supports up to 16 heads. The WD1015-24 uses the RWC pin on J1 as HEAD SELECT 3 (HS3). Refer to Table 10 for further details.
3.5 seconds time-out on single track steps	No	Yes	3.5 time-out allows removable/servo drives time to create servo map. WD1015-14 allows 1 second.
Bit 4 of opcode in Command Control	Valid	Don't care	Refer to Figure 2 for further details.
Step rates			Refer to Table 8 for further details.
Format Bad Track			Refer to Command Section for further details.

RESET LOGIC

The Reset Logic initializes the internal circuitry of the WD1002S-WX2 during the power-up process or a low voltage condition. The Reset Logic also disables the WRITE GATE signal. Disabling WRITE GATE prevents writing spurious data to the disk drive during power up, power down or a low voltage conditon.

INTERFACE CONNECTIONS

The WD1002S-WX2 has four on-board connectors for user application.

P1 Host interface: 62-pin IBM PC compatible card edge connector.

J1 Drive control: 34-pin dual row header connector daisy-chained to two drives. The control signals at the second drive from the WD1002S-WX2 (no more than a total length of 10 feet or 3 meters) are terminated with a 220 ohm resistor to +5V and a 330 ohm resistor to ground.

J2,J3 Drive data: 20-pin dual row header connectors, radially connected each to its own drive.

HOST INTERFACE

Connector P1 pins A1 through A31 are on the component side of the board and B1 through B31 are on the artwork side. Table 2 describes the Host interface Connector, P1.

TABLE 2. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
A1		NOT CONNCECTED		
A2 thru A9	D7 thru D0	DATA 7 thru DATA 0	I/O	8-Bit, tri-state, bi-directional bus. It is used to transmit data between the Host and Sector Buffer, and Command Block to the WD1015, status and drive configuration to the Host. The BIOS transmits parameter information and commands to the Host via this bus.
A10		NOT CONNECTED		
A11	AEN	ADDRESS ENABLE	I	AEN is asserted during a DMA mode of operation making the I/O ports 320 hex thru 323 hex inaccessible to the Host. Data transfers and intrabus control is initiated by asserting DACK3. The BIOS ROM can still be addressed via A0-A19.
A12 thru A31	A19 thru A0	ADDRESS BUS A19 thru A0	I	A0 thru A9 are used during programmed I/O mode of operation to address ports 320 hex thru 323 hex. They are inhibited during DMA by AEN. A0 thru A19 addresses the BIOS ROM regardless of the state of AEN.
B1	GND	GROUND		
B2	RST	RESET	I	When asserted, RST places the WD1002S-WX2 into its initial power-up state.
B3	+5VDC	+5VDC		+5VDC
B4	IRQ2	INTERRUPT REQUEST LEVEL 2	O	The WD1002S-WX2 asserts IRQ2 to interrupt the Host upon the completion of a command. Use of IRQ2 is jumper selectable. Use of IRQ5 is standard. Refer to Table 10 for further details on jumper selectable options.
B5 thru B8		NOT CONNECTED		
B9	+12VDC	+12VDC		+12VDC
B10	GND	GROUND		
B11		NOT CONNECTED		

TABLE 2. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION (CONT'D.)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
B12	$\overline{\text{MEMR}}$	$\overline{\text{MEMORY READ}}$	I	The Host, to read the BIOS ROM places the address on A0 thru A19, asserts $\overline{\text{MEMR}}$ and receives the data via D0 thru D7 data bus.
B13	$\overline{\text{IOW}}$	$\overline{\text{I/O WRITE}}$	I	The Host or DMA controller asserts $\overline{\text{IOW}}$ when a data byte is to be written to the WD1002S-WX2.
B14	$\overline{\text{IOR}}$	$\overline{\text{I/O READ}}$	I	The Host or DMA controller asserts $\overline{\text{IOR}}$ when a data or status byte is to be read from the WD1002S-WX2.
B15	$\overline{\text{DACK3}}$	$\overline{\text{DMA ACKNOWLEDGE CHANNEL 3}}$	I	The DMA controller asserts $\overline{\text{DACK3}}$ in response to DRQ3 sent by the WD1002S-WX2. $\overline{\text{DACK3}}$ enables DMA data transfer, bypassing port 320 which was disabled by AEN.
B16	DRQ3	DMA REQUEST CHANNEL 3	O	WD1002S-WX2 asserts DRQ3 to inform the DMA controller that data is available for transfer.
B17 thru B22		NOT CONNECTED		
B23	IRQ5	INTERRUPT REQUEST LEVEL 5	O	The WD1002S-WX2 asserts IRQ5 to interrupt the Host upon the completion of a command.
B24 thru B28		NOT CONNECTED		
B29	+5VDC	+5VDC		+5VDC
B30		NOT CONNECTED		
B31	GND	GROUND		

DRIVE INTERFACE

DRIVE CONTROL

Control signals are common to all drives and are daisy-chained to the drives from a single connector, J1. To terminate the control signals properly, the last drive in the daisy-chain must have a 220/330 ohm resistor pack installed. Table 3 describes the drive control connector, J1.

TABLE 3. DRIVE CONTROL CONNECTOR (J1) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
1	2	RWC/HS3	REDUCE WRITE CURRENT/HEAD SELECT 3	O	The WD1015-14 allows this pin to be used as the RWC pin. The WD1015-24 uses this pin as HS3. Refer to Table 10 for further details. RWC is used by the drive to reduce the write current on the inner cylinders. This lessens the bit shift caused by the greater bit density on these cylinders. RWC is asserted when the specified cylinder is reached. HS3 is one of four Head Select signals decoded by the drive to select one of 16 R/W heads.
3	4	HS2	HEAD SELECT 2	O	HS2 is one of three (or four) Head Select signals decoded by the drive to select one of eight (or 16) R/W heads.
5	6	WG	WRITE GATE	O	WG is asserted when valid data is to be written. It is used by the drive to enable the write current to the head. WD1002S-WX2 de-asserts this signal when a WF is detected. Circuitry is included to ensure the output does not glitch during power on, power down or power failure.
7	8	SC	SEEK COMPLETE	I	SC informs the WD1002S-WX2 that the selected head has reached the desired cylinder and has stabilized. Since SC is not checked after a Seek Command, overlapped seeks are allowed.
9	10	TK000	TRACK 000	I	The drive asserts this signal when the heads are positioned over the outermost cylinder, cylinder 0.
11	12	WF	WRITE FAULT	I	WF is asserted by the drive when a write error occurs. The command in progress aborts and no other comand can be executed while this signal is asserted.
13	14	HS0	HEAD SELECT 0	O	HS0 is one of three (or four) Head Select signals decoded by the drive to select one of eight (or 16) R/W heads.
15		GND	GROUND		
	16		NOT CONNECTED		
17	18	HS1	HEAD SELECT 1	O	HS1 is one of three (or four) Head Select signals decoded by the drive to select one of eight (or 16) R/W heads.
19	20	INDEX	INDEX PULSE	I	This signal indicates the start of a track. It is used as a sychronization point during formatting and as a time out mechanism for retries. This signal pulses once for each revolution of the disk.
21	22	DRDY	DRIVE READY	I	The drive asserts this signal when the motor is up to speed. No Read or Write commands can be performed if this signal is not asserted.

TABLE 3. DRIVE CONTROL CONNECTOR (J1) PIN DESCRIPTION (CONT'D.)

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
23	24	$\overline{\text{STEP}}$	$\overline{\text{STEP PULSE}}$	O	$\overline{\text{STEP}}$ along with $\overline{\text{DIRIN}}$ positions the heads to the desired cylinder. $\overline{\text{STEP}}$ pulses the stepping motor at the rate specified by the SP bits in the Command Block and is controlled by the WD1015. $\overline{\text{DIRIN}}$ specifies the direction.
25	26	$\overline{\text{DSEL 0}}$	$\overline{\text{DRIVE SELECT 0}}$	O	$\overline{\text{DSEL 0}}$ is the decoded output of the SDH Register within the WD1010A-05, latched and sent to the drive by the WD1015 to select drive 0.
27	28	$\overline{\text{DSEL 1}}$	$\overline{\text{DRIVE SELECT 1}}$	O	$\overline{\text{DSEL 1}}$ is the decoded output of the SDH Register within the WD1010A-05, latched and sent to the drive by the WD1015 to select drive 1.
29, 31	30, 32		NOT CONNECTED		
33	34	$\overline{\text{DIRIN}}$	$\overline{\text{DIRECTION IN}}$	O	$\overline{\text{DIRIN}}$ determines the direction the R/W heads take when stepped. Asserted = in, de-asserted = out.

DRIVE DATA CONNECTOR

The data is differential in nature and must be connected to each drive with its own cable, drive 0 to J2 and drive 1 to J3. It should be a flat ribbon cable, or twisted pair, less than 3 meters (10 feet) in length. The connector is a 20-pin vertical header on 0.25 centimeter (0.1 inch) center. Table 4 describes the drive data connectors, J2 and J3.

TABLE 4. DRIVE DATA CONNECTORS – J2, J3

SIG. GND.	SIG. PIN	I/O	SIGNAL NAME
	1		NC
2			GND
	3		NC
4			GND
	5		NC
6			GND
	7		NC
8			GND
	9		NC
	10		NC
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	– MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	– MFM Read Data
19			GND
20			GND

COMMAND DESCRIPTION

This section provides a detailed description of the Command Block format and function of the 19 commands supported by the WD1002S-WX2. Fourteen of the commands are operational and five are diagnostic. Table 5 lists a summary of the commands.

TABLE 5. COMMAND SUMMARY

COMMAND	PARAMETERS (Refer to Figure 2)								
	OP CODE	DRV	HD	CYL	SEC	BLK/INT	R1	R2	STEP
TEST DRIVE READY	00	V	n	n	n	n	n	n	n
RECALIBRATE	01	V	n	n	n	n	V	n	n
READ STATUS OF LAST OPERATION	03	V	n	n	n	n	n	n	n
FORMAT DRIVE	04	V	V	V	DR	V(INT)	V	n	V
VERIFY SECTORS	05	V	V	V	V	V(BLK)	V	V	V
FORMAT TRACK	06	V	V	V	DR	V(INT)	V	n	V
FORMAT BAD TRACK	07	V	V	V	DR	V(INT)	V	n	V
READ SECTOR	08	V	V	V	V	V(BLK)	V	V	V
WRITE SECTORS	0A	V	V	V	V	V(BLK)	V	n	V
SEEK	0B	V	V	V	DR	n	V	n	V
INITIALIZE DRIVE PARAMETERS	0C	V	n	n	n	n	n	n	n
READ ECC BURST ERROR LENGTH	0D	V	n	n	n	n	n	n	n
READ SECTOR BUFFER	0E	n	n	n	n	n	n	n	n
WRITE SECTOR BUFFER	0F	n	n	n	n	n	n	n	n
EXECUTE SECTOR BUFFER DIAGNOSTIC	E0	n	n	n	n	n	n	n	n
EXECUTE DRIVE DIAGNOSTIC	E3	V	n	n	n	n	V	n	V
EXECUTE CONTROLLER DIAGNOSTIC	E4	n	n	n	n	n	n	n	n
READ LONG	E5	V	V	V	V	V(BLK)	V	n	V
WRITE LONG	E6	V	V	V	V	V(BLK)	V	n	V

LEGEND:

V Must be a valid parameter
DR Not used but must be within a valid parameter range
n Not used (should be 0 for future compatibility)
INT Interleave
BLK Block Count

I/O PORT DESCRIPTION

There are four contiguous I/O ports addressed 320 hexidecimal through 323 hexidecimal. Each port is bi-directional. The functions of the I/O ports are listed in Table 6. These ports are used for all communication between the Host and Controller.

TABLE 6. I/O PORT DESCRIPTIONS

ADDRESS	READ PORT FUNCTION	WRITE PORT FUNCTION
320	READ DATA	WRITE DATA
321	READ WD1002S-WX2 HRDWR STATUS	WD1002S-WX2 RESET*
322	READ DRIVE CONFIGURATION INFO	WD1002S-WX2 SELECT
323	Not Used	WRITE DMA AND INTERRUPT MASK REGISTER

***NOTE**

The WD1015-14 automatically executes self-tests after either a Reset command or upon power-up. The WD1015-24 DOES NOT automatically execute self-test after either a Reset command or upon power-up. A WD BIOS performs an Execute Controller Diagnostic command as part of the install sequence after power-up regardless of the version of WD1015 on-board. If the Host software interrogates WD1015-24 after a Reset; the WD1015-24 returns good status. The Host must issue an Execute Controller Diagnostic command to perform the WD1015-24 self-test.

PORT 320

This is a bi-directional path over which data, commands, parameters, and status are passed.

PORT 321

The Host reads this port to interrogate the hardware status. This status byte can be read at any time, including command execution. The status bits are identified in Table 7.

TABLE 7. HARDWARE STATUS

BIT							
7	6	5	4	3	2	1	0
d	d	IRQ	DRQ	BSY	C/D	I/O	REQ

d Not used

IRQ Interrupt Request. Assertion (set to 1) signifies that an interrupt is pending.

DRQ DMA request bit. Assertion (set to 1) signals the Host that the WD1002S-WX2 is ready for a DMA transfer to take place. The direction of the transfer is defined by the I/O bit.

BSY Busy bit. Assertion (set to 1) signals the Host that the WD1002S-WX2 is busy executing a command and is unable to accept another command.

C/D Control/Data. Tells the Host which type of transfer the WD1002S-WX2 is expecting. 1 = command or status byte. 0 = data.

I/O Input/Output. Identifies the direction of transfers between the Host and WD1002S-WX2. The terms input and output are relative to the Host. 1 = input, 0 = output.

REQ Request bit. A handshake signal for data transfers between the Host and WD1002S-WX2. The WD1002S-WX2 asserts (sets to 1) this bit when it is ready for data to be transferred between it and the Host. **REQ must be valid for every byte transferred to the Host.**

The Host writes to this port to generate a MR (Master Reset) on the WD1002S-WX2. When writing to this port, the data byte is ignored.

Resetting a WD1002S-WX2 with a WD1015-14 causes automatic execution of a self-test. Automatic execution of self-test does not occur with the WD1015-24. If the Host software interrogates WD1015-24 after a Reset; the WD1015-24 returns good status. The Host must issue an Execute Controller Diagnostic command to perform the WD1015-24 self-test.

PORT 322

Reading Port 322 returns a 4-bit drive configuration code in bits 0 through 3. The two least significant bits correspond to drive 0, the two most significant bits to drive 1. The configuration of these bits is established with jumpers on the controller at SW1. Western Digital sets the configuration jumpers to one. Table 11 shows how to set them up for a specific drive.

The two bits associated with each drive is capable of addressing one of four different configuration tables. Both drives can address the same or different tables. The table required by the drive is determined by its formatted capacity. Table 0 = 5MB, 1 = 24MB, 2 = 15MB, 3 = 10MB (default table) with 62-000042-01 and 62-000042-11 WD BIOS. Table 0 = 20MB, Table 1 = 10MB, Table 2 = 20MB, Table 3 = 10MB with 62-000042-12 WD BIOS.

The parameters established by these tables are:

Number Of Cylinders
Number Of Heads
The Starting Cylinder For RWC (Reduced Write Current).
The Starting Cylinder For Write Precomp
Maximum Correctable Error Burst Length
Retries Allowed, Stable or Immediate ECC Correction, Step Rate

Writing to port 322 selects the WD1002S-WX2, sets the Busy bit in the Status Register and prepares it to receive a command. When writing to port 322, the data byte is ignored.

PORT 323

Reading this port has no function.

Writing to this port controls the enabling of the interrupt and DMA request signals to the Host. The bits in this port are defined as follows:

BIT							
7	6	5	4	3	2	1	0
d	d	d	d	d	d	IRQEN	DRQEN

IRQEN Interrupt Request Enable. When asserted (set to one), enables interrupts to the Host.

DRQEN DMA Request Enable. When asserted (set to one), enables DMA requests to the Host.

COMMAND BLOCK

The Host first selects the WD1002S-WX2 by asserting I/OW while at the same time addressing port 322 with the A0 through A19 address bus. The WD1002S-WX2 then asserts the BSY (BUSY) bit in the Status Register. The Host by asserting I/OR and addressing port 321 reads the status, finding REQ asserted transmits the first byte of the six byte Command Block to the WD1015. REQ is de-asserted at the end of the first byte transfer. REQ must be re-asserted for the second byte of the Command Block transfer. Assertion and de-assertion of REQ must occur for each byte transferred. Figure 2 defines the bytes within the Command Block.

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	OP CODE							
1	0	0	D	0	HEAD NUMBER			
2	CYL NUMBER MSB		0	SECTOR NUMBER				
3	CYLINDER NUMBER LSB							
4	BLOCK COUNT OR INTERLEAVE							
5	R1	R2	0	0	0	SP	SP	SP

FIGURE 2. COMMAND BLOCK DESCRIPTION

OP Code: Operation Code identifies the type and function of the command. Bits 7, 6, and 5 designate whether the command is operational (0) or diagnostic (5). Bits 4 through 0 select the function of the command, i.e. Read, Write, etc.

NOTE

The WD1015-24 firmware ignores bit four of byte 0 (op code).

D — Drive number, selects one of two drives zero or one.

Head Number — Designates the head to be used on the selected drive. 0 through 15. Selection of heads 8 through 15 requires WD1015-24.

Cylinder Number MSB and LSB — Designates the cylinder containing the sector(s) to be used by the command. 0 through 1024.

Sector Number — Specifies the starting sector used by the command.

Block Count or Interleave — Block count specifies the number of sectors to be used by a Read, Write, Read Long, or Write Long command. A block count of zero equals 256 sectors. Interleave is used by the Format commands. The maximum interleave is equal to the sectors-per-track minus one.

R1 — General disk error retry disable bit. R1 controls the retry for all errors except a Data ECC error. With R1 asserted, the WD1002S-WX2 makes no attempt to retry an error operation. Instead, it aborts the command and sets the appropriate status in the Status Register. Because the disk is soft sectored, an ID field error may cause the WD1002S-WX2 to perform two retries. With R1 de-asserted, the WD1002S-WX2 retries the operation approximately ten times before aborting the command and setting the status bit. In the case of an ID Not Found Error, the WD1002S-WX2 does a restore to track zero and seeks back to the desired track after the first ten tries and then makes ten more tries before aborting and setting the error status.

R2 — ECC Error retry bit. With R2 = 1, an attempt is made to correct the error on the first syndrome. R2 = 0 there must be two consecutive like syndromes before an attempt is made to correct the error.

SP — The Step Code is used to select the rate at which step pulses are issued to the drive. Table 8 defines the rates corresponding to each step pulse code.

TABLE 8. STEPPING RATE CODES

BITS			STEPPING RATES	
2	1	0	WD1015-14	WD1015-24
0	0	0	3 msec. per step*	3 msec. per step*
0	0	1	3 msec. per step	45 μsec. per step
0	1	0	3 msec. per step	60 μsec. per step
0	1	1	3 msec. per step	18 μsec. per step
1	0	0	200 μsec. per step	210 μsec. per step
1	0	1	70 μsec. per step	75 μsec. per step
1	1	0	3 msec. per step	30 μsec. per step
1	1	1	3 msec. per step	18 μsec. per step

*This is the preferred 3 msec. step code.

TEST DRIVE READY (OP CODE 00)

This command selects the drive specified by the DRV bit in the Command Block and interrogates the $\overline{DRDY}$, $\overline{WF}$, and $\overline{SC}$ signals returned by that drive. If $\overline{WF}$ and $\overline{SC}$ are de-asserted and DRDY asserted, the command returns an error code of 00 No Error Detected.

POSSIBLE ERROR CODES

03 Write Fault
04 Drive Not Ready
08 Drive Still Seeking

RECALIBRATE (OP CODE 01)

This command moves the Read/Write heads to track 0. The $\overline{SC}$ signal from the drive controls the stepping rate of this command. Therefore, this command is slower than commands that implement the implied seek and make use of the stepping rate designated by the SP bits in the Command Block.

NOTE

Timeout on each step during a Recalibrate command is 1 second with a WD1015-14. Timeout on each step during a Recalibrate is 3.5 seconds with a WD1015-24. The 3.5 second timeout supports removable Winchesters.

POSSIBLE ERROR CODES

03 Write Fault
04 Drive Not Ready
06 Track Zero Not Found

READ STATUS OF LAST OPERATION (OP CODE 03)

Upon termination of a command the WD1002S-WX2 develops a Command Completion Byte, de-asserts the BSY bit, if IRQEN had been enabled, asserts IRQ5. If IRQEN had not been asserted, it is the responsibility of the Host to read port 321 to determine that a WD1002S-WX2 is no longer busy. Once the Host determines that a command has terminated, it must read the Command Completion Byte to learn which drive has terminated and whether an error had occurred. To do this, the Host reads port 320. The format of the Command Completion Byte is as follows:

BIT							
7	6	5	4	3	2	1	0
0	0	D	0	0	0	E	0

D = Number of the drive terminating. 0 = drive 0. 1 = drive 1
E = 1 if an error occurred

If the Command Completion Byte indicates the occurence of an error, issue a Read Status command for the drive indicating the error. Preformance of a Read Status command before any other command execution prevents loss of the error status. When a Read Status of the last operation is written to port 320, the WD1002S-WX2 responds with four bytes of status as shown in Figure 3.

BYTE	BITS							
	7	6	5	4	3	2	1	0
0	AV	0	ERROR CODE					
1	0	0	D	0	HEAD NUMBER			
2	CYL NUMBER MSB		0	SECTOR NUMBER				
3	CYLINDER NUMBER LSB							

AV Address valid bit. Indicates that the Head, Cylinder, and Sector fields are valid.
Error Codes are shown in Table 9
All other bits are the same as those defined in the Command Block definitions.

FIGURE 3. FOUR STATUS BYTES

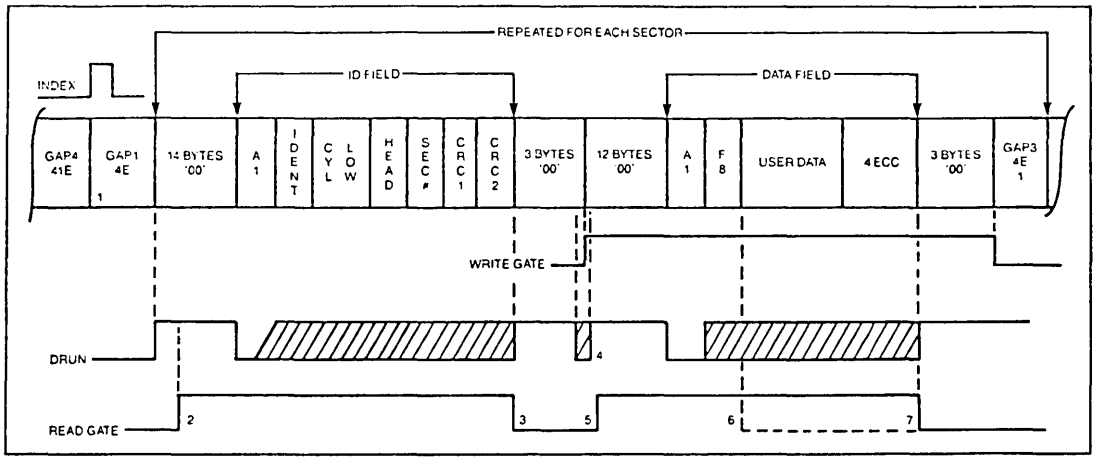
When an error occurs during a multiple sector data transfer (read or write), this command returns the address of the failing sector. If the Read Status command is issued after any of the format commands or the Verify Desired Sectors command, the address returned by the WD1002S-WX2 points one sector beyond the last track formatted or blocked, if there was no error. If there was an error, then the address returned points to the track in error.

TABLE 9. CONTROLLER RETURNED ERROR CODES

HEX CODE	DEFINITION
00	No error detected.
02	No $\overline{SC}$ signal from the drive. The WD1002S-WX2 has not received a SC from the drive within one second (3.5 seconds with WD1015-24) following the last step pulse of a non-buffered seek operation.
03	Write Fault signal received from the drive. This error is reported when the WD1002S-WX2 detects $\overline{WF}$ asserted by a drive either at the completion of a Sector Data Transfer or after initially selecting a drive and the drive indicates ready.
04	Drive Not Ready. The WD1002S-WX2 reports this error when $\overline{DRDY}$ is not received from the drive at the time selection is attempted, or is de-asserted after the drive has been selected.
06	Track 0 Not Found. This error is reported during a Recalibrate command if $\overline{TK000}$ is not received from the drive before stepping the Read/Write Heads 1024 steps.
08	Drive Still Seeking. This status is returned in response to a Test Drive Ready command when a drive performing a buffered seek has not yet asserted $\overline{SC}$.
11	Uncorrectable Data Error. The ECC logic detected an error burst greater than its correction capabilities. The data in the Sector Buffer is not sent to the Host.
12	Data Address Mark Not Found. The proper Sector ID was read by the drive but failed to detect the Data Address Mark.
15	Seek Error. The desired Sector ID field could not be found on the selected track, or a CRC error occurred on the ID field.
18	Correctable Data Error. An error occurred in the data field that was within the tolerance of the ECC logic and was corrected. The data in the Sector Buffer is transmitted to the Host. This status is set as a warning to the Host that a marginal condition may exist.
19	Track Is Flagged Bad. A sector had been encountered that has the Bad Block Mark set in the ID Field. The Format Bad Track command records this bit in all sectors of the designated flagging them all as bad. No retries are attempted in response to this error.
20	Invalid Command. The WD1002S-WX2 has received a command with an invalid class or Op code, Interleave Factor.
21	Illegal Sector Address. This error is asserted when a command attempts to address a sector beyond the capacity of the drive. This could be at the time the command is issued, or in the case of a multiple sector transfer, after the last available sector has been used.
30	Sector Buffer Error. An error occurred while preforming Sector Buffer Diagnostics (Command Code E0 and E4). A disk drive is not involved in this test.
31	Controller ROM Checksum Error. A ROM checksum error was detected during the Controller Diagnostic command (E4).
32	ECC Polynomial Error. During the Controller Diagnostic command (E4), the hardware ECC generator (WD11C00-17) failed its test.

FORMAT DRIVE STARTING AT DESIRED TRACK (OP CODE 04)

The WD1002S-WX2 first positions the Read/Write heads to track zero. Using the parameters specified in the Command Block, the WD1002S-WX2 positions the heads to the desired track. Formatting always starts with the first sector of the track, regardless of the value of SEC. Even so, SEC must be within the allowable limits. A sample of what is recorded in each sector is shown in Figure 4. The data recorded in the Data Field is defaulted to whatever is in the Sector Buffer at the time. The logical sector numbering is specified by the interleave value (INT) included in the Command Block. If a hard error occurs while formatting a track, the WD1002S-WX2 stops the format operation and returns an error code.



ID FIELD

A1 = A1 Hex with 0A Hex clock

IDENT = Bits 1,0 = Cylinder High
FE = 0-255 Cylinders
FF = 256-511 Cylinders
FC = 512=767 Cylinders
FD = 768-1023 Cylinders

HEAD = Bits 0,1,2 = Head Number
Bits 3,4, = 00
Bits 5,6, = Sector Size (10)
Bit 7 = Bad Block Mark

Sec# = Logical Sector Number

DATA FIELD

A1 = A1 Hex with 0A Hex clock

F8 = Data Address Mark; Normal Clock

USER = Data Field 512 Bytes

NOTES:

1. GAP 1 and 3 length equals 22 bytes.
2. The decision to assert RG is made 2 bytes after the start of DRUN.
3. RG de-asserted:
   - If DRUN does not last until A1
   - When any part of ID does not match the one expected.
   - After CRC if correct ID has been read.
4. Write splice recorded on disk by asserting WG.
5. RG is suppressed until after write splice.
6. Not a proper A1 or F8, set DAM error.
7. Sector size as stated in ID field, plus four for ECC.

FIGURE 4. FORMAT

INTERLEAVING

When physically sequential sectors on the disk are to be read, each sector reaches the read/write head before a read or write operation can be set up. The disk must then make a complete rotation to pick up the next sector. When an attempt is made to read all 17 sectors on a particular track, 17 rotations or approximately one fourth of a second per 8K bytes are required. This performance can be significantly improved by interleaving, a technique that allows the system to read or write more than one sector per rotation.

For a system requiring less than two sector times to proccess the data it has read and to set up for the next read operation, the second logical sector is physically placed three sectors away from the first. The controller can now read the second sector with minimal delay. This three-to-one interleave factor allows a potential reading of the entire track in less than three rotations. In the example given, the throughput is increased by a factor of 5.6.

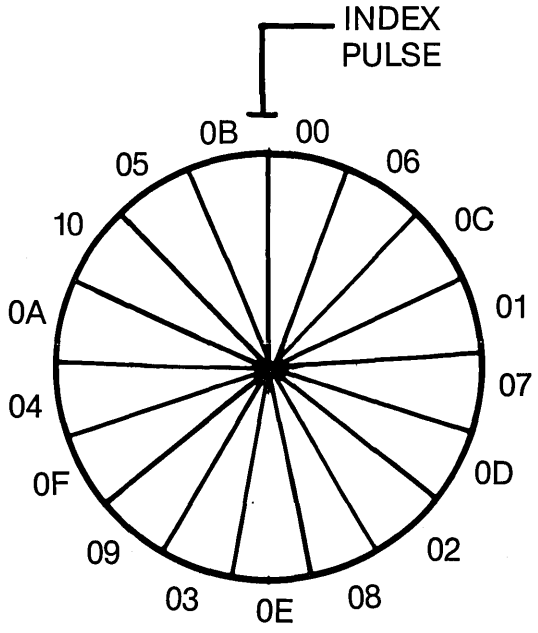


FIGURE 5. 17 SECTORS WITH A 3:1 INTERLEAVE

The simplest way to determine the optimum interleave for any particular system is through experimentation. If the system maintains its directories or virtual memory-swapping areas in a certain place of the disk, it sometimes makes sense to have more than one interleave.

To simplify driver software, the WD1002S-WX2 automatically writes the logical sector number of each sector in its ID field. Figure 5 is an example of an interleave table for a 17-sector track with 3:1 interleave. The WD1002S-WX2 accepts any interleave value between zero and one less than the number of sectors per track. An interleave of zero is automatically converted to one, and a value out of range results in an error code 20, Invalid Command Error.

VERIFY SECTORS (OP CODE 05)

This command reads from 1 to 256 sectors, as specified by BLK in the Command Block, beginning at the sector specified by HD CYL and SEC. If an error occurs during a multiple sector read, the heads remain positioned at the track containing the error. The Host then issues a Read Status of Last Disk Operation command to determine the error code. To continue the operation, the Host calculates the difference between the number of sectors desired and the number of sectors completed and issues another Seek command to access the remaining sectors.

POSSIBLE ERROR CODES

02 No Seek Complete
03 Write Fault
04 Drive Not Ready
06 Track Zero Not Found
12 Data Address Mark Not Found
15 Seek Error
19 Track Flagged Bad
21 Illegal Disk Address

FORMAT TRACK (OP CODE 06)

This command is identical to the Format Drive command, except that only the track specified by the command is formatted. This command can be used to clear the Bad Track Flag, or reformat individual tracks.

FORMAT BAD TRACK (OP CODE 07)

This command is the same as the Format Track command, except that the Bad Track Flag is set in the ID field.

READ SECTORS (OP CODE 08)

This command reads from 1 to 256 sectors as specified by BLK in the Command Block, beginning at the sector defined by CYL SEC and Head. An uncorrectable error during a multiple sector read causes the operation to terminate at the error sector. The Host then issues a Read Status of Last Disk Operation command to determine the type of error. To continue the operation, the Host calculates the difference between the number of sectors desired and the number of sectors completed, then issues another Read commend to access the remaining sectors. Error code 06 can only be asserted if the R1 bit = 0 and ten consecutive attempts have failed to read the ID Field. This causes the WD1002S-WX2 to recalibrate the heads and seek back to the desired track. If track zero is not detected within 1024 steps, Error Code 06 is set. If R1 = 1, the WD1002S-WX2 aborts the command after a maximum of two tries to read the ID field. Therefore no attempt is made to position the heads to track zero.

POSSIBLE ERROR CODES

02 No Seek Complete
03 Write Fault
04 Drive Not Ready
06 Track Zero Not Found
11 Uncorrectable ECC Error
12 Data Address Mark Not Found
15 Seek Error
18 Correctable ECC Error
19 Track Flagged Bad
21 Illegal Sector Address

WRITE SECTORS (OP CODE 0A)

This command writes from 1 to 256 sectors as specified by BLK in the Command Block. The multiple sector transfer scheme works the same as the Read command. Error code 06 can only be asserted if the R1 bit is 0 and ten consecutive attempts have failed to read the ID Field. This causes the WD1002S-WX2 to recalibrate the heads and seek back to the desired track. If track zero is not detected within 1024 steps, Error Code 06 is set. If R1 is 1, the WD1002S-WX2 aborts the command on the first failure to read an ID Field. Therefore, no attempt to position the heads to track zero is made.

POSSIBLE ERROR CODES

02 No Seek Complete
03 Write Fault
04 Drive Not Ready
06 Track Zero Not Found
12 Data Address Mark Not Found
15 Seek Error
19 Track Flagged Bad
21 Illegal Disk Address

SEEK (OP CODE 0B)

This command selects the head and initiates a seek to the track specified by HD and CYL in the Command Block. The $\overline{SC}$ signal line is sampled to allow buffered seeks. The cylinder must be in range. The drive must be formatted. Drives employing buffered steps can be issued step pulses at a high speed, freeing the WD1002S-WX2 for other operations. The WD1002S-WX2 does not wait for the drive to complete the seek to return a Command Completion Status. If the return status shows no error, the seek was issued correctly. If there is an error, the seek was not issued. After transferring the status, another command can be issued to either drive. If the WD1002S-WX2 receives a command other than Test Drive Ready for a drive that is still seeking, it asserts BSY and waits for $\overline{SC}$ to be asserted before executing the command. If the command is a Test Drive Ready, it executes and returns an 08 Drive Still Seeking Error. The time-out for non-buffered seeks is 1 second for a WD1002S-WX2 with a WD1015-14. A WD1002S-WX2 with a WD1015-24 times out for 3.5 seconds for non-buffered seeks. For buffered seeks, the WD1015 checks $\overline{SC}$ before a Read or Write (next command).

The rate at which the Step Pulses are issued to the drive is controlled by the SP bits in the Command Block. The drive buffers these pulses and steps at its own rate. This allows the WD1002S-WX2 to continue about its own business, possibly starting the other drive seeking to a new track, without having to wait for the $\overline{SC}$ from the first drive. Refer to Table 8 for the available stepping rates.

POSSIBLE ERROR CODES

03 Write Fault
04 Drive Not Ready
15 Seek Error

INITIALIZE DRIVE PARAMETERS (OP CODE 0C)

The WD1002S-WX2 is capable of controlling two drives with different formatted capacity. The BIOS contains four Winchester parameter tables. The configuration jumpers address the proper Winchester parameter table during the BIOS install cycle at power up. Refer to Table 11 for details on these jumper settings. When the Host reads port 322 and discovers a change in drives, it issues this command, followed by the 8-byte block of drive parameters listed below:

Maximum Number of Cylinders (2 bytes, 1024 max.)
Maximum Number of Heads (1 byte, 8 or 16 heads)
Starting Reduced Write Current Cylinder (2 bytes, 1024 max.)
Starting Write Precompensation Cylinder (2 bytes, 1024 max.)
Maximum ECC Data Burst Length (I byte, max.)

A typical set of parameters for a 10MB drive is as follows:

306 cylinders
4 heads
RWC at cylinder 153
Write Precomp at cylinder 153
11-bit burst error length (Western Digital Corp. recommends using a maximum ECC burst length of five or less to ensure optimum integrity of data recovered).

For the exact parameters, it is necessary to refer to the specifications for the BIOS in use on the specified board.

READ ECC BURST ERROR LENGTH (OP CODE 0D)

This command is only valid following a correctable ECC error. It transfers one byte indicating the length of the error. The error length is determined by counting the first through last bit in the error.

READ SECTOR BUFFER (OP CODE 0E)

This command transfers the 512 bytes of data currently residing in the Sector Buffer to the Host.

WRITE SECTOR BUFFER (OP CODE 0F)

This command writes 512 bytes of data from the Host into the WD1002S-WX2 Sector Buffer.

EXECUTE SECTOR BUFFER DIAGNOSTIC (OP CODE E0)

This command executes a 9-pass test that uses a 0-byte pattern (0, 1, 2, 4, 8, 10, 20, 40, and 80 hex) that is written to the Sector Buffer, then read back. After each successful completion, the whole pattern is shifted one byte postition and repeated.

NOTE

The WD Format Drive Utility in the WD BIOS executes this command before physical formatting of the drive. Thus, the data fields are formatted with this 0, 1, 2, 4, 8, 10, 20, 40, and 80 hex pattern.

POSSIBLE ERROR CODES

30 Data error

EXECUTE DRIVE DIAGNOSTIC (OP CODE E3)

This command tests both the drive and the drive-to-WD1002S-WX2 interface. The WD1002S-WX2 sends Recalibrate and Seek commands to the selected drive and reads sector zero of each track verifying both ID and data fields. The WD1002S-WX2 does not perform any write operations.

5.19.1 POSSIBLE ERROR CODES

02 No Seek Complete
03 Write Fault
04 Drive Not Ready
06 Track Zero Not Found
12 Data Address Mark Not Found
15 Seek Error

EXECUTE CONTROLLER DIAGNOSTICS (OP CODE E4)

Regardless of the version of the WD1015 on the WD1002S-WX2, the WD1002S-WX2 executes this command when the Host issues a command code of E4 hex to the CCB. The WD1015-14 automatically executes this command after system Reset (RST on connector P1 B2 asserted), write to port 321 Hex, or power-up. The WD1015-24 only automatically executes this command when an on-board WD BIOS performs an install sequence after power-up.

Once started, this command continues to run until an error occurs, or the Host selects the WD1002S-WX2 by writing to port 322. If an error occurs when this command has been started at power up, an error code is output at pins 27, 28, and 29 of the WD1015. These are the Head Select 0, 1, and 2 signals and can be monitored at the Drive Control Connector J1 pins 14, 18, and 4. The error codes generated under this condition are not the same as those reported by a Read Status command.

1 - WD1010A-05 Error
2 - WD11C00-17 ECC Error
3 - Sector Buffer Error
4 - WD1015 RAM Error
5 - WD1015 ROM Error

WD1010A-05 TEST

A pattern is written to and read from the WD1010A-05's Sector Count and Sector Number Registers.

WD11C00-17 ECC TEST

The WD11C00-17 is enabled during the read portion of the Sector Buffer Test. After the contents of the Sector Buffer have been read, the ERR (pin 1) of the WD11C00-17 is monitored, it should be asserted indicating non-zero Check Bytes. The internal check pattern is then fed back into the chip and pin 1 monitored again. This time it should not be asserted, indicating a Check Byte pattern of zero.

SECTOR BUFFER TEST

The hex pattern 00, 01, 02, 04, 08, 10, 20, 40, 80 is written throughout the entire Sector Buffer and then read to make sure it is correct. The entire contents of the Sector Buffer is then shifted one byte position and read again. This procedure is repeated nine times verifying that every bit in the Sector Buffer can be set and reset.

The WD11C00-17 is enabled during the read functions to verify the operability of that device.

WD1015 RAM TEST

This tests the 100 bytes of internal RAM in the same manner as the Sector Buffer test.

WD1015 ROM TEST

This test verifies the ability to address and read all 2K bytes of internal ROM, using an add and rotate algorithm to generate a single byte result. This result is then compared with the Sumcheck located in the last page of memory.

POSSIBLE ERROR CODES

30 Sector Buffer Error
31 ROM Sumcheck Error
3 ECC Error

READ LONG (OP CODE E5)

The Host first performs a normal Write command, writing known data, that produces a predictable ECC character, then performs a Read Long command. This command reads the data from the disk without generating a ECC bytes of its own. Instead, it reads the four ECC bytes from the disk, as though reading data, resulting in 512 plus 4 for a total of 516 bytes of data. The Host, knowing what the data and ECC bytes are supposed to be, can now determine whether any errors that have occurred are a result of a data or ECC failure.

POSSIBLE ERROR CODES

02 No Seek Complete
03 Write Fault
04 Drive Not Ready
06 Track Zero Not Found
12 Data Address Mark Not Found
15 Seek Error
19 Track Flagged Bad
21 Illegal Disk Address

WRITE LONG (OP CODE E6)

After performing the Write normal/Read Long routine to determine that the WD1002S-WX2 is able to write data and generate correct ECC bytes, the Host can execute a Write Long and Read normal routine. This verifies the ability of the WD1002S-WX2 to read the data correctly and generate 4-zero ECC bytes or if an error was forced, correct it. The Write Long command does not generate ECC bytes, instead the Host supplies them along with a known data pattern. Then, performing a normal Read command, the Host can determine whether non-zero ECC bytes are caused by a Read failure or ECC generation failure. (This procedure could be performed prior to the Write normal/Read Long).

POSSIBLE ERROR CODES

02 No Seek Complete
03 Write Fault
04 Drive Not Ready
06 Track Zero Not Found
12 Data Address Mark Not Found
15 Seek Error
19 Track Flagged Bad
21 Illegal Disk Address

INSTALLATION

HARDWARE AND SOFTWARE INSTALLATION

This section briefly describes installation of the WD1002S-WX2 in an IBM PC or IBM-compatible computer.

1. Ensure system power is off.
2. Insert WD1002S-WX2 in computer chassis and connect drive cables.
   (J1 = control cable, J2 = drive 0 cable, J3 = drive 1 cable)
3. Power up the system.
4. Insert IBM PCDOS 2.0 or IBM PCDOS 2.1 diskette.

CAUTION

Performing steps 5 through 9 destroys any data presently on the disk.

5. Load DEBUG utility by typing "debug" and ENTER after the DOS prompt.
6. Initiate the WX2FMT (format) program by typing the following command line: g = c800:5
7. Press "y" to begin formatting drive 0 (logical drive C.)
8. To format drive 1 or second drive in a daisy chain, reload DEBUG utility. Type "RAX" and ENTER. Prompt returns "AX 0000". Type "0103", ENTER which defines relative drive number and interleave factor (01 = relative drive number; 03 = interleave factor). Type "G = C800:5", ENTER, and type "y" to begin formatting drive 1 (logical drive D).
9. Run standard DOS utilities, FDISK and FORMAT.

JUMPER INSTALLATION AND LOCATIONS

The WD1002S-WX2 is configured for the standard IBM PC XT with jumper plugs installed at W3, W4, and W6. No jumpers are required at W5 and W7. To change the configuration, a jumper plug can be installed in the appropriate block. Installation of jumpers on W5 and W7 requires carefully cutting an etch and placing a jumper plug onto the Jumpered position. To restore the standard setting, move the jumper plug to the Standard position. Table 10 describes these jumpers and options. Table 11 describes the drive configuration jumpers and an INTERRUPT REQUEST (IRQ) jumper in SW1. Figure 6 illustrates the locations of W1 through W7 and SW1.

TABLE 10 JUMPER SELECTABLE OPTIONS (W1 THROUGH W5)

JUMPER	FUNCTION	PIN	DESCRIPTION
W1,W2			For Western Digital Manufacturing use only.
W3	Standard:	1-2	Closed by etch or jumper. Enables BIOS ROM
		1-2	Open. Disables BIOS ROM.
W4	Standard:	2-3	Selects primary port 320 Hex.
	Jumpered:	1-2	Selects secondary port 324 Hex. Requires custom BIOS. **NOTE** The WD1002S-WX2 provides two sets of I/O ports. The primary port addresses are 320 through 323 Hex. The secondary port addresses are 324 through 327 Hex. However, secondary ports on the WD1002S-WX2 are *NOT* supported by many versions of DOS.
W5	Standard:	1-2	Selects 2732 or 2764 BIOS ROM size.
	Jumpered:	2-3	Selects 2716 BIOS ROM size. W5 pin 1-2 etch must be cut.
W6	Standard:	2-3	8 head configuration, RWC used.
	Jumpered:	1-2	16 head configuration, RWC not used, requires custom BIOS ROM and WD1015-24.
W7	Standard:	1-2	Selects IRQ5.
	Jumpered:	2-3	Selects IRQ2. SW1 position 5 must also be jumpered (closed) and W7 pin 1-2 etch must be cut.

TABLE 11 SW1 JUMPER BLOCK DESCRIPTION

WD BIOS 62-000042-01 (ROM) or 62-000042-11 (EPROM)

BIOS TABLE	FORMATTED CAPACITY	POSITION 1 2 DRIVE 1	POSITION 3 4 DRIVE 0	DRIVE TYPE	HEADS	NUMBER OF CYLINDERS	PRE-COMP RWC
3	10MB	1 1	1 1	ST412 Seagate	4	306	0 None
2	15MB	0 1	0 1	ST419 Seagate	6	306	256 RWC = 128
1	26MB	1 0	1 0	5820 Evotek	8	375	0 None
0	5MB	0 0	0 0	ST506 Seagate	2	306	0 None
		WD BIOS 62-000042-12 (EPROM)					
3	10MB	1 1	1 1	ST412 Seagate	4	306	0 None
2	20MB	0 1	0 1	ST225 Seagate	4	612	128 None
1	10MB	1 0	1 0	3012 MiniScribe	2	612	128 RWC = 128
0	20MB	0 0	0 0	HH725 Microscience	4	612	None None

Factory sets jumper for BIOS Table 3. Position 5 of SW1 select IRQ5 (factory setting) or IRQ2. 1 = IRQ5. 0 = IRQ2. Positions 6, 7, and 8 of SW1 are reserved.

LEGEND: 1 = no jumper installed, ties input to +5vdc. 0 = jumper installed, ties input to ground.

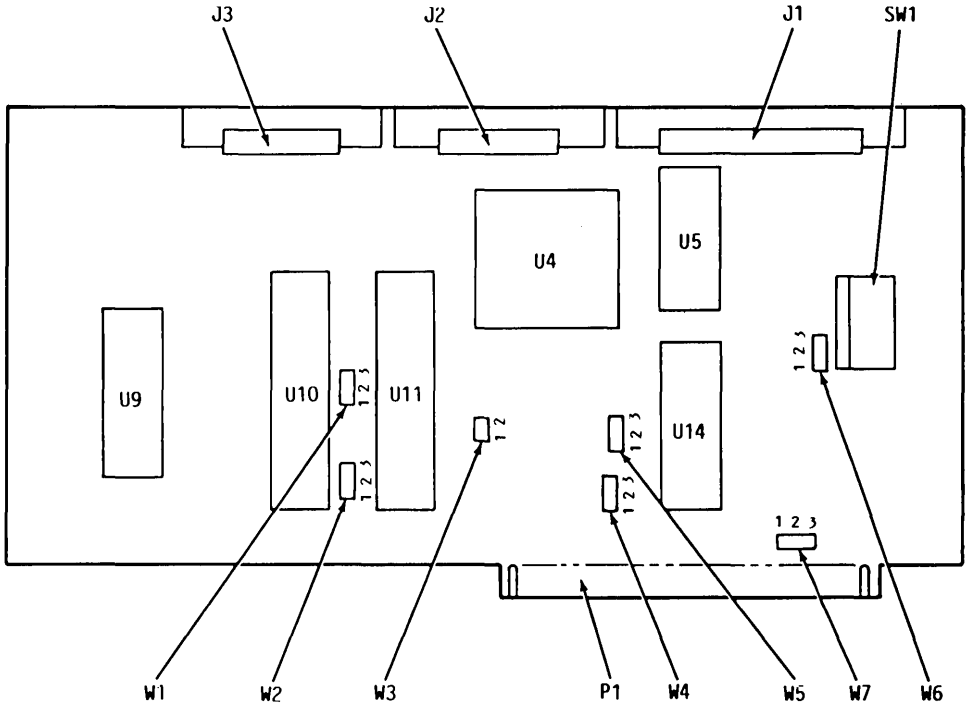


FIGURE 6. JUMPER LOCATIONS

7.3 BIOS ROM INSTALLATION

The WD1002S-WX2 firmware driver routines, supplied by Western Digital Corporation, reside in a 4KB x 8 bit EPROM. This BIOS ROM is available in three sizes as follows:

2716 2KB x 8 bit
2732 4KB x 8 bit (standard from the factory)
2764 8KB x 8 bit

The WD1002S-WX2 provides a 28 pin DIP socket for the BIOS ROM. This socket accomodates a 2732 or 2764 JEDEC EPROM. Figure 7 illustrates the standard connections for the 2732 or 2764. These connections can be modified to support a 2716. Perform the following steps to modify the standard connections:

1. Cut the etch between pads 1 and 2 on W5
2. Jumper pad 3 to pad 2
3. Wire pin 20 and 26 as shown.
4. Plug BIOS in the socket. Pin 1 of the 2716 BIOS should be in position 3 of the socket.

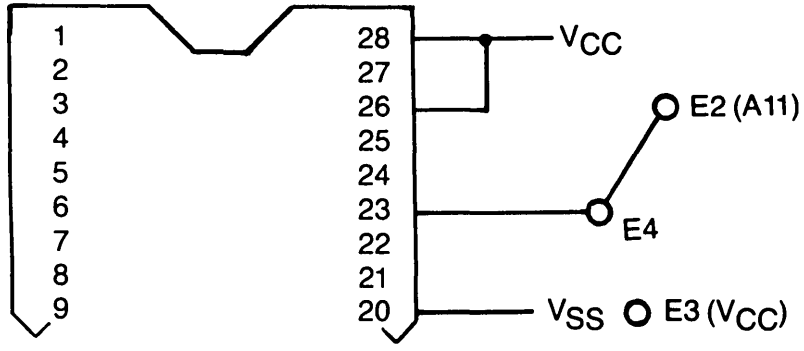


FIGURE 7. BIOS ROM SOCKET CONNECTIONS

SPECIFICATIONS

This section contains the overall specifications for the WD1002S-WX2 Winchester Disk Controller.

ELECTRICAL

HOST INTERFACE

Type	IBM PC
Host Interface Connector	P1 connects directly to Host motherboard with a 62-pin card edge connector

DRIVE INTERFACE

Encoding Method	MFM
Cylinders per Drive	Up to 1024
Sectors per Track	17
Bytes per Sector	512
Heads	8 with WD1015-14 16 with WD1015-24
Drive Selects	2
Stepping Rates	70 μsec, 200 μsec, 3 msec (WD1015-14) 18 μsec, 30 μsec, 45 μsec, 60 μsec, 75 μsec, 2l0 μsec, 3 msec (WD1015-24)
Data Transfer Rate	5 Mbits/sec (ST506)
Write Precomp Time	12 nsec
Sectoring	Soft
CRC Polynomial	$x^{16} + x^{12} + x^5 + 1$
ECC Polynomial	$x^{32} + x^{28} + x^{26} + x^{19} +$ $x^{17} + x^{10} + x^6 + x^2 + 1$
Reciprocal ECC Polynomial	$x^{32} + x^{30} + x^{26} + x^{22} +$ $x^{15} + x^{13} + x^6 + x^4 + 1$
Miscorrection Prob.	5-bit correction = <1.6 E- 5
Non-detection Prob.	<2.3 E-10
Correction Span	Up to ll-bit burst
Max Cable Length:	
Control (Total Daisy 3 Meters (10 ft.) Chain)	3 Meters (10 ft.)
Data (Radial-each)	3 Meters (10 ft.)

WD10C20

Acquisition Time	< or = 12. 8 μs
Capture Range	± 2.2% to 1ns after 12.8 μs acquisition
Bit Jitter Tolerance	± -34ns (min. of 40 db after acquisition)
Asymmetry Tolerance	± -34ns (write precompensation turned off; as measured over constant RCLK pattern)

POWER

Voltage	5V ±5%
Current	0.8 amps max.
Ripple	0.1 volts max., 25 mV typical
Voltage	+12 ±10%
Current	10 mA. max.

PHYSICAL

Form factor	IBM PC
Length	20.6 centimeters (8.1 inches)
Width	9.78 centimeters (3.85 inches)
Height (max including board, components, & leads)	1.27 centimeters (0.50 inches)

ENVIRONMENTAL

Ambient Temperature	0°C (32°F) to 55°C (131°F)
Relative Humidity	10% to 95% non-condensing
Altitude	0 to 3000 meters (10,000 ft)
Air Flow	100 lin ft/min. at 0.5" from component surfaces.
MTBF	10,000 POH
MTTR	30 Minutes

INTERFACE TIMING

Timing diagrams are shown in Figures 8 through 11 and their values are listed in Tables 12 through 15 respectively. Since the Controller I/O ports can be accessed by either the Host system DMA Controller or the Host processor, timing is given for both cases. The processor executes I/O and memory reads from the ports and the on-board BIOS ROM, and writes to the ports. The DMA is used for data transfers between the data I/O port and the Host RAM.

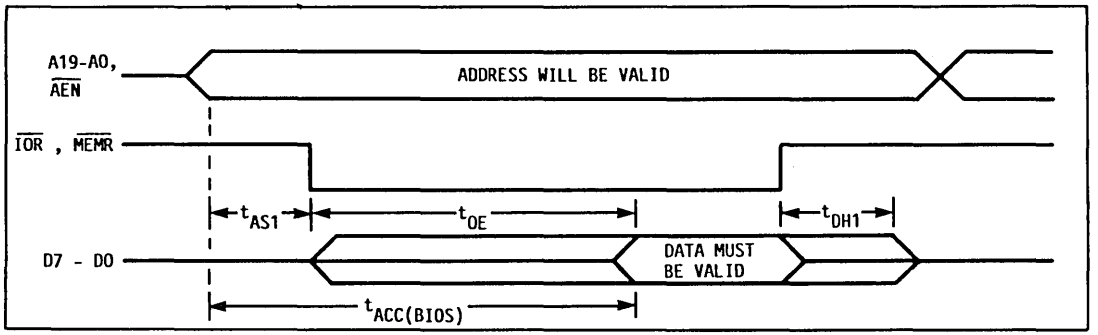


FIGURE 8. HOST I/O OR BIOS READ TIMING

TABLE 12. HOST I/O OR BIOS READ TIMING

UNITS IN NSEC.

SYMBOL	CHARACTERISTIC	MIN	MAX
t_{AS1}	Address Setup Time	50	
t_{ACC}	Address Access Time		250
t_{OE}	Output Enable Time		175
t_{DH1}	Data Hold Time	0	

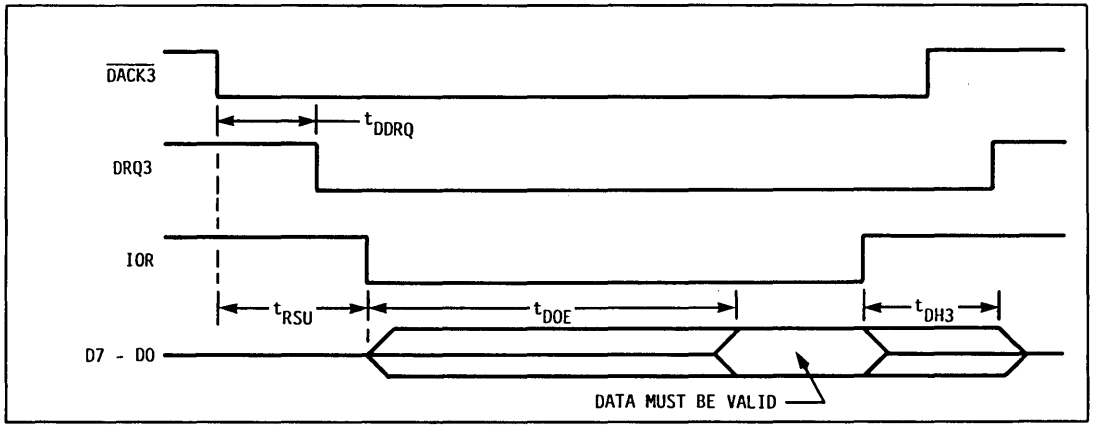


FIGURE 9. DMA I/O READ TIMING

TABLE 13. DMA I/O READ TIMING

UNITS IN NSEC.

SYMBOL	CHARACTERISTIC	MIN.	MAX.
t_{DDRQ}	DRQ3 De-assert Delay	20	45
t_{RSU}	Read Setup Time	7	
t_{DOE}	Data Output Enable		175
t_{DH3}	Data Hold Time	0	

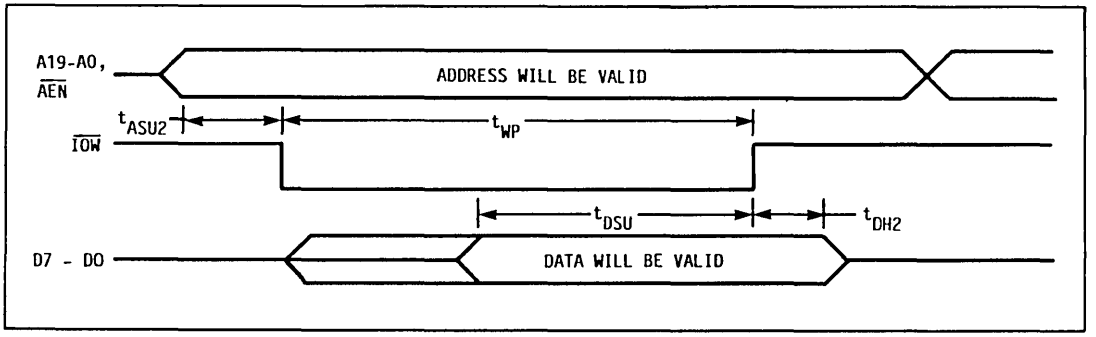


FIGURE 10. HOST I/O WRITE TIMING

TABLE 14. HOST I/O WRITE TIMING

UNITS IN NSEC.

SYMBOL	CHARACTERISTIC	MIN.
t_{ASU2}	Address Setup Time	50
t_{WP}	Write Pulse Time (I/O)	100
t_{DSU}	Data Setup Time	50
t_{DH2}	Data Hold Time	0

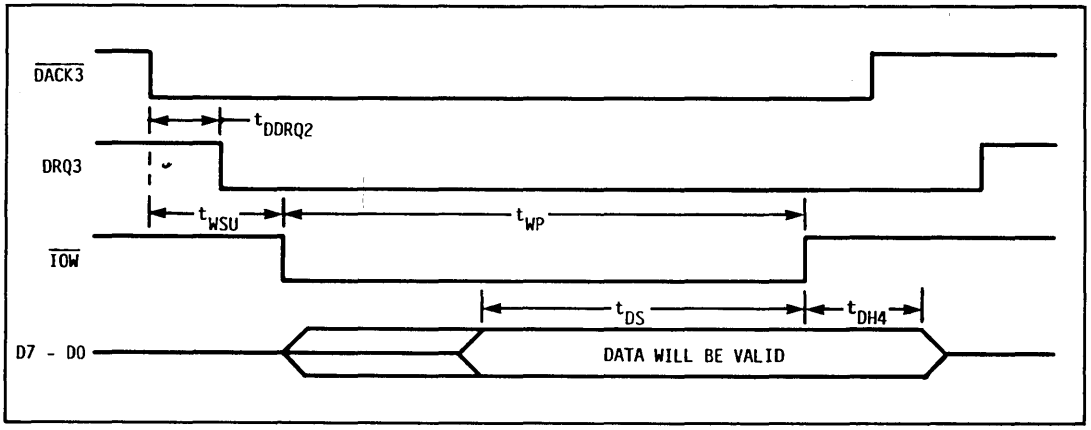


FIGURE 11. DMA I/O WRITE TIMING

TABLE 15. DMA I/O WRITE TIMING

UNITS IN NSEC.

SYMBOL	CHARACTERISTIC	MIN.	MAX.
t_{DDRQ}	DRQ3 De-assert Delay	20	45
t_{WSU}	Write Setup Time	7	
t_{WP}	Write Pulse Width	100	
t_{DS}	Data Setup Time	50	
t_{DH4}	Data Hold Time	0	

WD1002-WAH WINCHESTER DISK CONTROLLER

FEATURES

- PC AT COMPATIBLE WINCHESTER CONTROLLER
- CONTROLS UP TO TWO WINCHESTER DRIVES (16 R/W HEADS EACH)
- HARDWARE DESIGN ALLOWS TWO WD1002-WAH CONTROLLERS IN ONE SYSTEM
- 8-BIT, BI-DIRECTIONAL BUS HOST INTERFACE (FOR CONTROL AND STATUS TRANSFERS)
- 16-BIT, HIGH-SPEED PIO DATA TRANSFERS
- 32-BIT ECC FOR WINCHESTER ERROR DETECTION AND CORRECTION
- MULTIPLE SECTOR READ/WRITE COMMANDS (MAY CROSS HEAD AND CYLINDER BOUNDARIES)
- IMPLIED AND BUFFERED SEEK COMMANDS
- READ/WRITE DIAGNOSTIC AND VERIFY COMMANDS
- PROGRAMMABLE FORMAT AND ERROR RECOVERY ALGORITHMS
- WD10C20 SINGLE CHIP DATA SEPARATOR

DESCRIPTION

The WD1002-WAH is an IBM PC AT bus compatible Winchester controller board designed to interface up to two drives. The drive interface is based upon the Seagate Technology ST506. The drives need not be of the same capacity or configuration. All necessary receivers and drivers are included on the board to allow direct connection to the drive(s).

ARCHITECTURE

The WD1002-WAH is based on the WD1014-01 Error Detection/Support Logic device, WD1015-03 Buffer Manager Control Processor, WD1010A-05 Winchester Disk Controller, and WD10C20 Data Separator. The WD1002-WAH also uses two 2K x 8 static RAM memory devices as a Sector Buffer.

The WD1014-01 provides error correction for the WD1002-WAH. The WD1014-01 generates four ECC bytes and appends these bytes to the sector data field. The maximum error correction span is 5-bits. The WD1014-01 sets the error correction span. The WD1014-01 also selects the proper drive and head.

The WD1015-03 is an 8-bit microprocessor that controls and coordinates the activity of the disk drives, WD1010A-05, and WD1014-01. The WD1015-03 receives and sends command or status information over the internal WD1002-WAH multiplexed address/data bus, HD0 through HD7. Controlling firmware resides in the WD1015-03's 2K internal ROM.

The WD1010A-05 controls all data transfers between the Sector Buffer and the drives. The WD1010A-05 performs multiple sector Read/Write, Implied and Buffered Seek commands. The WD1010A-05 also executes programmable format and error recovery algorithms. All commands are executed through the seven Task Files of the WD1010A-05 after limited intervention by the WD1015-03 and WD1014-01.

The WD10C20 performs phase-locked loop data synchronization on read data from the Winchester drives. This device also conditions write data to be recorded on the disk. The WD10C20 includes both frequency and phase detection. Zero phase error start-up circuitry eliminates problems due to asymmetry. The WD10C20 requires no adjustments and contains all data separation circuitry in a single device.

The Sector Buffer is two 2KB x 8 RAMs. Since the WD1010A-05, WD1014-01, and WD1015-03 are 8-bit devices, two RAMs are used because the Host provides data in 16-bit words. An onboard PAL selects the proper RAM. The Sector Buffer RAMs never contain more than 512 bytes.

Figure 1 is a block diagram of the WD1002-WAH.

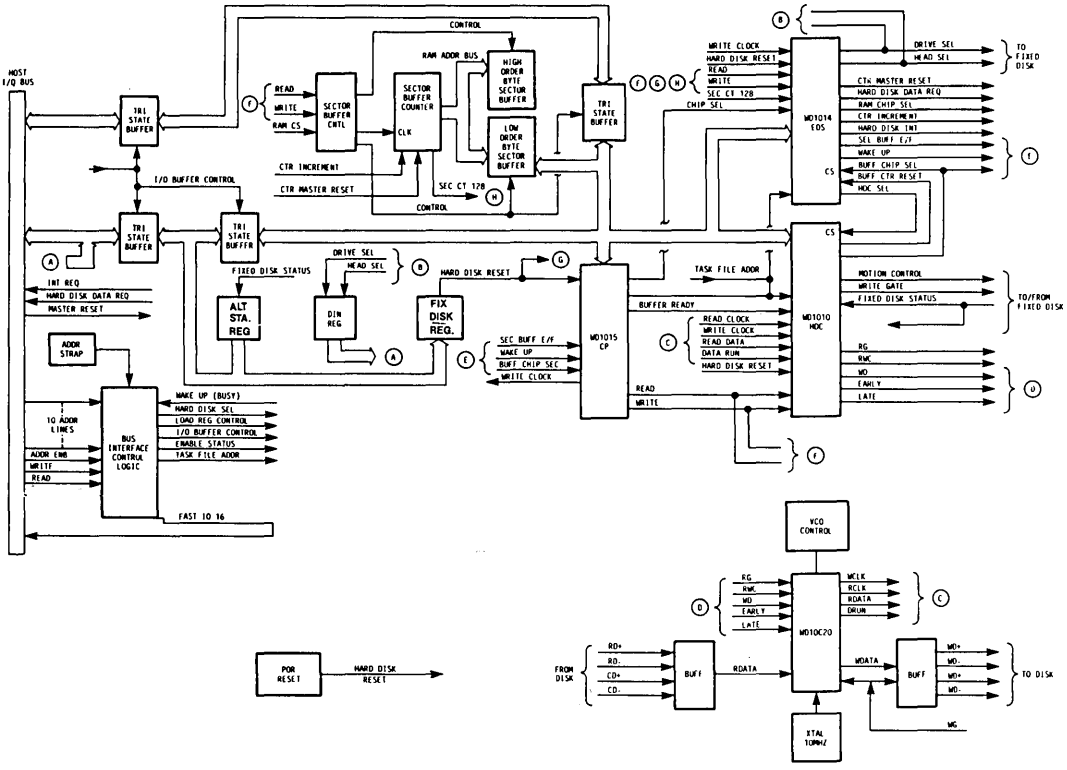


FIGURE 1. WD1002-WAH BLOCK DIAGRAM

INTERFACE CONNECTORS

The WD1002-WAH has five interface connectors:

P1-62-pin card edge connector
Component side -Pins A1 through A31
Conductor side -Pins B1 through B31

P2-36-pin card edge connector
Component side -Pins C1 through C18
Conductor side -Pins D1 through D18

J1- control cable connector

J2- drive 0 data cable connector

J3- drive 1 data cable connector

The pin description of the connectors are given in Tables 1 through 4.

HOST INTERFACE CONNECTORS

The WD1002-WAH Controller interfaces with the 16-bit, bi-directional data bus by means of the two card edge connectors P1 and P2. The pin descriptions for P1 are given in Table 1 and for P2, in Table 2.

TABLE 1. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
A1,A10, A12 thru A21	NC			
A2 thru A9	SD7 thru SD0	DATA BIT 7 thru DATA BIT 0	I/O	Bi-directional, 8-bit data bus for data and status communication between the controller and the Host.
A11	AEN	ADDRESS ENABLE	I	When AEN is asserted, the DMA controller assumes control of the Host address bus, control bus, and data bus. I/O port addresses are no longer generated for I/O port access.
A22 thru A31	SA9 thru SA0	ADDRESS BITS A9 thru A0	I	A 10-bit address bus for I/O addressing by the Host.
B1,B10 B31	GND	Ground		
B2	RST	RESET	I	When asserted, RST forces the WD1002-WAH board into the initial power-up state.
B3,B29	+5VDC	+5VDC		+5VDC
B9	+12VDC	+12VDC		+12VDC
B4 thru B8,B11, B12	NC			
B13	$\overline{\text{IOW}}$	$\overline{\text{I/O WRITE}}$	I	Assertion causes the WD1002-WAH to read a data, status or control byte from the Host data bus.
B14	$\overline{\text{IOR}}$	$\overline{\text{I/O READ}}$	I	Assertion causes the WD1002-WAH to drive data unto the Host data bus.
B15 thru B27,B30	NC			
B28	ALE	ADDRESS LATCH ENABLE	I	Assertion enables the WD1002-WAH to latch a valid board address from the Host address bus.

TABLE 2. HOST INTERFACE CONNECTOR (P2) PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
C1 thru C10	NC			
C11 thru C18	D8 thru D0	DATA BIT 8 thru DATA BIT 15	I/O	Bi-directional, 8-bit data bus for data tranfers only between the controller and the Host.
D1	NC			
D2	I/OCS16	I/O 16 BIT CHIP SELECT	I	Assertion signals the system board that the current data transfer is a 1 wait-state, 16-bit I/O cycle, derived from an address decode.
D3 thru D6	NC			
D7	IRQ14	INTERRUPT REQUEST 14	O	Assertion indicates that the WD1002-WAH request execution of the Host interrupt service routine.
D8 thru D18	NC			

DRIVE CONTROL CONNECTOR J1

The drive control connector is a 34-pin printed circuit card edge connector daisy-chained to each drive in the system. To terminate the control signals on the WD1002-WAH properly, the last drive on the daisy chain must have a 220/330 ohm resistor pack installed. Pin descriptions and control signals for the drive control connector J1 are given in Table 3.

TABLE 3. DRIVE CONTROL CONNECTOR (J1) PIN DESCRIPTION

SIGNAL				I/O	FUNCTION
GND.	PIN	MNEMONIC	NAME		
1	2	HS3/RWC	HEAD SELECT 3 REDUCE WRITE CURRENT	O	The WD1002-WAH uses HS3 to select one of 16 R/W heads. RWC is not used with 16 head drives. RWC is used by drives with 8 R/W heads. RWC reduces the write current on the inner cylinders. This lessens the bit shift caused by greater density on these cylinders.
3	4	HS2	HEAD SELECT 2	O	HS2 is one of the head select signals decoded by the drive to select one of eight (or 16) R/W heads.
5	6	WG	WRITE GATE	O	WG is asserted when valid data is to be written on disk. The WD1002-WAH de-asserts WG when WF is detected. Special circuitry is included to ensure the system output is free of glitches during power-on.
7	8	SC	SEEK COMPLETE	I	SC informs the WD1002-WAH that the head of a selected drive has reached the desired cylinder and has stabilized.

TABLE 3. DRIVE CONTROL CONNECTOR (J1) PIN DESCRIPTION (cont'd)

SIGNAL				I/O	FUNCTION
GND.	PIN	MNEMONIC	NAME		
9	10	TK000	TRACK 000		TK000 is asserted when the R/W heads are positioned over the outermost cylinder.
11	12	WF	WRITE FAULT		WF is asserted by the selected drive when a write error occurs. While this signal is being asserted, the command in progress aborts and no other disk command can be executed.
13	14	HS0	HEAD SELECT 0	O	HS0 is one of the head select signals decoded by the drive to select one of eight (or 16) R/W heads.
15		GND			
	16	NC			
17	18	HS1	HEAD SELECT 1	O	HS1 is one of the head select signals decoded by the drive to select one of eight (or 16) R/W heads.
19	20	INDEX	INDEX PULSE	I	INDEX indicates the start of a track. Used as a synchronization point during formatting and as a time-out mechanism for retries. Pulses once each disk revolution.
21	22	DRDY	DRIVE READY	I	DRDY informs the controller that the drive motor is up to speed.
23	24	STEP	STEP PULSE	O	STEP, with DIRIN, positions the heads to the desired cylinder. STEP pulses once for each step. DIRIN determines the step direction.
25	26	DS0	DRIVE SELECT 0	O	DS0 is used to select drive 0.
27	28	DS1	DRIVE SELECT 1	O	DS1 is used to select drive 1.
29, 31, 33		GND			
	30, 32	NC			
33	34	DIRIN	DIRECTION IN	O	DIRIN determines the direction in which the R/W heads move when the step line is pulsed. De-asserted = out; asserted = in.

DATA CONNECTORS

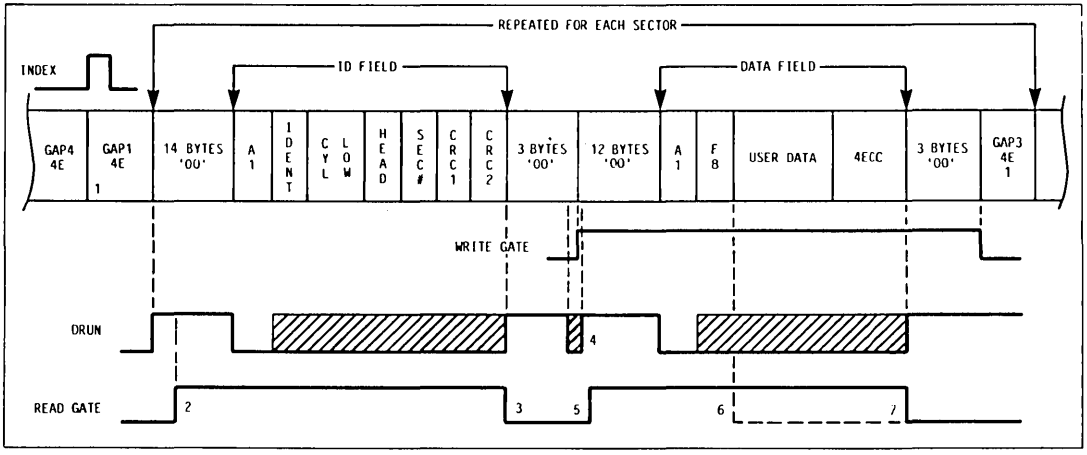
The data lines between the WD1002-WAH and the two disk drives are connected to J2 and J3. As the data lines are not identical, J2 must be connected to the cable from drive 0, and J3 to the cable from drive 1. Each drive is radially connected with a maximum cable length of 3 meters (10 feet). Each data connector is a 20-pin vertical header on 0.25mm (0.01 inch) center. Data connector pin descriptions and signals are listed in Table 4.

TABLE 4. DRIVE DATA CONNECTORS (J2,J3) PIN DESCRIPTION

SIGNAL			
GND	PIN	I/O	SIGNAL NAME
	1		NC
2			GND
	3		NC
4			GND
	5		NC
6			GND
7		NC	
8			GND
	9		NC
	10		NC
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	-MFM Write Data
15			GND
16			GND
	17		+ MFM Read Data
	18		-MFM Read Data
19			GND
20			GND

FORMAT

The format used for Winchester disk track formatting is shown in Figure 2. The ID and data fields on any disk are initialized by the Format command.



NOTES

1. GAP 1 and 3 length equals 22 bytes.
2. Decision to assert RG is made two bytes after the start of DRUN.
3. RG is de-asserted:
   - If DRUN does not last until A1.
   - When any part of the ID does not match the one that is expected.
   - After CRC, if correct ID has been read.
4. Write splice recorded on disk by asserting WG.
5. RG is suppressed until after write splice.
6. Not a proper A1 or F8, set DAM error.
7. Sector size as stated in ID field, plus four for ECC.

ID FIELD

A1 = A1 hex with OA hex clock

IDENT = Bits 1,0 = Cylinder High

FE = 0-255 Cylinders
FF = 256-511 Cylinders
FC = 512-767 Cylinders
FD = 768-1023 Cylinders

HEAD = Bits 0, 1, 2 = Head Number
Bits 3,4 = 0
Bits 5, 6 = Sector Size
Bit 7 = Bad Block Mark

Sec # = Logical Sector Number

DATA FIELD

A1 = A1 hex with 01 hex clock
F8 = Data Address Mark; Normal Clock
USER = Data Field 512 Bytes

FIGURE 2. WINCHESTER DISK FORMAT

REGISTER ADDRESS MAP

The WD1002-WAH contains seven Read/Write task file registers in the WD1010A-05 and three hardware registers external to the WD1010A-05. These registers are mapped into either a primary of secondary I/O address. All data, control, and status information pass between the task files and the Host.

All data transfers are word transfers except ECC bytes in Read Longs and Write Longs. These ECC bytes are transferred in byte mode. Control and status bytes are also transferred between the Host in byte mode. The 7 task file registers are multiplexed with $\overline{IOR}$ and $\overline{IOW}$ to give 14 possible parts. Five of the eight task file registers are bi-directional. Two of the task file registers have different definitions for read and write operation. Jumpers select the primary and secondary address. This allows two controllers in the same Host system. However, secondary ports on the WD1002-WAH are not supported by any version of DOS.

Table 5 summarizes the WD1002-WAH I/O port address map. Figure 3 summarizes the WD1010A-05 task file registers and bit assignments. Figure 4 summarizes the other three I/O registers and bit assignments for the WD1002-WAH. Bit assignments are with respect to the Host lower byte bus terms, SD7 through SDO. The fixed size/drive/head (SDH) and status registers in the WD1010A-05 desciptions slightly differ from the standard descriptions in the WD1010-05 data sheet. Please note that the SDH register is set for the ECC option mode and 512 bytes per track. The SDH register also limits the number of heads to 16. Bit 2 of the WD1010A-05 status register is designated as the Corrected Data bit. Assertion (setting to 1) of this bit indicates the sector read from the drive resulted in a correctable ECC error. Soft errors do not end multiple sector transfers. Bit 1 of the WD1010A-05 status register is designated as the Index bit. Assertion of this bit occurs each revolution of the currently selected drive. Refer to the WD1010-05 data sheet for a complete description of all other WD1010A-05 bit assignments. Table 6 describes the bit assignments for the other WD1002-WAH control and status registers.

NOTE

Where differences exist, the values and descriptions for Figure 3 take precedence over the WD1010-05 data sheet.

TABLE 5. WD1002-WAH REGISTER ADDRESS MAP

I/O ADDRESS			
PRIMARY	**SECONDARY**	**READ**	**WRITE**
WD1010A-05 TASK FILE REGISTERS			
1F1	171	ERROR REGISTER	WRITE PRE-COMP
1F2	172	SECTOR COUNT	SECTOR COUNT
1F3	173	SECTOR NUMBER	SECTOR NUMBER
1F4	174	CYLINDER NUMBER (low byte)	CYLINDER NUMBER (low byte)
1F5	175	CYLINDER NUMBER (high byte)	CYLINDER NUMBER (high byte)
1F6	176	SDH REGISTER	SDH REGISTER
1F7	177	STATUS REGISTER	COMMAND REGISTER
CONTROL AND STATUS REGISTERS EXTERNAL TO THE WD1010A-05			
1F0	170	DATA REGISTER (16 bits)	DATA REGISTER (16 bits)
3F6	376		FIXED DISK REGISTER
3F6	376	ALTERNATE STATUS REGISTER	
3F7	377	DIGITAL INPUT REGISTER	

REGISTER	7	6	5	4	3	2	1	0
WRITE PRE-COMP	CYLINDER NUMBER DIVIDED BY 4							
ERROR	BB	ECC	0	ID	0	AC	TK	DM
SECTOR COUNT	NUMBER OF SECTORS							
SECTOR NUMBER	SECTOR NUMBER							
CYLINDER NO.	CYLINDER NUMBER (LOW BYTE)							
CYLINDER NO.	0	0	0	0	0	0	CYL. NO. MSB	
SDH	1	0	1	DS	HS3	HS2	HS1	HS0
COMMAND	COMMAND							
STATUS	BSY	RDY	WF	SC	DRQ	CRD	IDX	ERR

FIGURE 3. WD1010A-05 TASK FILE REGISTER BIT ASSIGNMENT

REGISTER	7	6	5	4	3	2	1	0
ALTERNATE STATUS	BSY	RDY	WF	SC	DRQ	CRD	IDX	ERR
DIGITAL INPUT	X	$\overline{WTG}$	$\overline{HS3}$/ $\overline{RWC}$	$\overline{HS2}$	$\overline{HS1}$	$\overline{HS0}$	$\overline{DS2}$	$\overline{DS1}$
FIXED DISK	0	0	0	0	HS3EN	RST	IEN	0

FIGURE 4. WD1002-WAH CONTROL AND STATUS REGISTERS

TABLE 6. WD1002-WAH CONTROL AND STATUS REGISTER BIT DEFINITIONS

REGISTER	BIT MNEMONIC	BIT NAME
ALTERNATE STATUS	BSY	Controller Busy Flag
	RDY	Ready from selected drive
	WFT	Write Fault from selected drive
	SKC	Seek Complete from selected drive
	DRQ	Data Transfer Request Flag
	CRD	Corrected Data Flag from WD1015-03
	IDX	Index pulse from selected drive
	ERR	Error Flag from WD1015-03
DIGITAL INPUT	X	Reserved. System bus signal SDO7 tri-stated
	$\overline{WTG}$	Write Gate on
	HS3 (RWC) through HS0	Drive head select or RWC (bit 5) for drives using RWC
	$\overline{DS2}$, $\overline{DS1}$	Drive select
FIXED DISK	HS3EN	Set to 1: Enables $\overline{HS3}$ Set to 0: Enables $\overline{RWC}$
	RST	Reset. Program controlled reset to board. This bit maintains the WD1002-WAH logic reset as long as this is on. This bit must be on for a minimum of 5.0 μsec. After the bit is on for the minimum time, the bit must be turned off to complete reset function.
	$\overline{IEN}$	Interrupt Enable. Enables or disables IRQ14. This bit does not clear the interrupt level in the disabled state. A pending interrupt would occur when the interrupt is enabled again. A system master reset clears the interrupt but leaves the interrupt enabled.

COMMANDS

The WD1002-WAH command set contains eight commands. Five commands (Restore, Seek, Read Sector, Write Sector, and Format Track) are executed through the WD1010A-05 command register. (A sixth WD1010A-05 command, Scan ID is not directly available to the Host. Scan ID may be executed by the WD1015-03 transparently to the Host.) The three remaining commands (Read Verify, Diagnose, and Set Parameters) are executed through the WD1015-03.

Table 7 describes the eight WD1002-WAH commands and their bit assignments. The next section describes a typical command sequence. Each command is described following the command sequence.

TABLE 7. COMMANDS AND COMMAND CODES

COMMAND	BITS							
Restore	0	0	0	1	R3	R2	R1	R0
Seek	0	1	1	1	R3	R2	R1	R0
Read Sector	0	0	1	0	0	0	L	T
Write Sector	0	0	1	1	0	0	L	T
Format Track	0	1	0	1	0	0	0	0
Read Verify	0	1	0	0	0	0	0	T
Diagnose	1	0	0	1	0	0	0	0
Set Parameters	1	0	0	1	0	0	0	1

LEGEND

R3 through R0	Step rate selection bits. Refer to Table 8 for more detailed information.
L	Read or Write Long bit. Set to 1 enables Read or Write Long mode.
T	Retry bit. Set to 1 disables retries.

The stepping rates for the commands that perform implied seeks are set in the least significant nibble of the last executed RESTORE or SEEK command. The stepping rate is given in Table 8.

TABLE 8. STEPPING RATE

R3	R2	R1	R0	STEPPING RATE	R3	R2	R1	R0	STEPPING RATE
0	0	0	0	35 μsec	1	0	0	0	4.0 msec
0	0	0	1	0.5 msec	1	0	0	1	4.5 msec
0	0	1	0	1.0 msec	1	0	1	0	5.0 msec
0	0	1	1	1.5 msec	1	0	1	1	5.5 msec
0	1	0	0	2.0 msec	1	1	0	0	6.0 msec
0	1	0	1	2.5 msec	1	1	0	1	6.5 msec
0	1	1	0	3.0 msec	1	1	1	0	7.0 msec
0	1	1	1	3.5 msec	1	1	1	1	7.5 msec
Note: After Diagnose or reset, stepping rate defaults to 7.5 msec									

COMMAND SEQUENCE DESCRIPTION

This section describes a typical command execution sequence. This description illustrates the relationship beween Host and the major components of the WD1002-WAH during command execution.

In the idle state: the WD1010A-05 drive control signals are off. The controller status indicates ready. Drive status is valid. Controller interrupt is enabled but not asserted. The WD1015-03 is idle and is monitoring the WAKEUP signal input.

The Host outputs the command parameters to the WD1010A-05 task file, the operation command (Seek, Read or Write) and the command attributes (Long mode, retry control, etc.). For write operations, the Host also outputs the sector or format data.

The command byte is intercepted by the WD1014-01 and is held for later interpretation by the WD1015-03.

A Read command output sets the module Wakeup latch that causes the controller status to indicate Busy and the WD1015-03 WAKEUP signal to be asserted. Write and Format commands first set the data request status signal DRQ. This initiates the Host data transfer. Completion of the data transfer (512 or 516 bytes) sets the WD1015-03 WAKEUP signal and Busy status.

The WD1015-03 examines the command, verifies command parameters, and passes the command to the WD1010A-05 for execution.

The WD1010A-05 executes the command providing drive positioning, data transfer control, error monitoring and completion status. The WD10C20 provides drive read and write data control for commands that require data transfers.

On command completion, the WD1010A-05 interrupts the WD1015-03. The WD1015-03 examines the command, status, etc. for any additional requirements. If completion is indicated, the WD1015-03 sets the controller status to indicate ready and interrupts the Host.

The WD1002-WAH returns to the idle state and the Host may examine drive and controller status, read input data, etc., as required to complete the operation.

COMMAND DESCRIPTION

Restore

The Restore command is used to move the R/W heads to the Track 000 position. The controller issues step pulses to the drive until the Track 000 indicator from the drive is asserted. If Track 000 is not asserted within 1023 steps, the Error bit in the Status Register is set and a Track 000 error is posted in the Error Register. The implied seek step rate may be set up according to Table 8 by the Restore command. The restore step rate is established by the seek complete signal from the drive, i.e., each step pulse is issued only after seek complete is asserted by the drive from the previous step. If the $\overline{\text{DRIVE READY}}$ signal is de-asserted or $\overline{\text{WRITE FAULT}}$ is asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

Seek

This command moves the R/W heads to the cylinder specified in the task file cylinder specified in the task file cylinder high and low registers. The implied seek step rate is also set by this command. The lower order four bits of the command are used to select one of 16 available step rates. An interrupt is generated at the completion of the command. If the DRIVE READY signal is de-asserted or WRITE FAULT is asserted, this command is terminated with the error bit set in the status register and the error register reports an aborted command.

Read Sector

A number of sectors (1 - 256) can be read from the selected drive with this command. The sector count register in the task file determines the number of sectors to be transferred. Multiple sector reads may cross head and cylinder boundaries.

If the Read command is issued prior to initializing a step rate, the default value of 7.5 msec is selected and a Recalibrate is performed prior to the Read.

If the R/W heads are not positioned over the target track, the controller performs an implied seek to the proper cylinder. The stepping rate used during the implied seek is the value specified during the previous Seek or Restore command.

The optional long bit (L set to 1 enables Read Long.) informs the WD1002-WAH whether or not to include the four ECC bytes. These four ECC bytes are transferred as individual bytes, not words, as is the data field information. The data request bit in the status register must be valid before each byte transferred and at least 2 μsec will pass between each byte transferred.

Data errors up to 5 bits in length will be automatically corrected on normal Read commands. If an uncorrectable error occurs, the data transfer will still take place, a multi- sector read, however, will terminate after the sector in error is read by the system.

The optional retry bit (T set to 1 disables retries.) disables or enables retries. The WD1010A-05 automatically retries for ten disk revolutions when the retry bit is enabled. The WD1010A-05 properly sets the error and status registers if the retries are unsuccessful. Disabling retries allows only two disk revolutions before the WD1010A-05 sets the error and status registers.

For ECC errors, eight retries are made at reading before a soft uncorrectable error is reported. A retry results in the reissuing of the WD1010A-05 Read Sector command. The WD1010A-05 Read Sector command attempts to verify the sector ten times, if T is set to 1, before returning an error. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. If the error is an uncorrectable error or an error is reported by the WD1010A-05, the command terminates.

Interrupts occur as each sector is ready to be read by the system. No interrupt is generated at the end of the command. If the DRIVE READY signal is de-asserted or WRITE FAULT asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

Write Sector

A number of sectors (1 - 256) can be written to the selected drive. The sector count register in the task file determines the number of sectors to be transferred. Multiple sector writes may cross head and cylinder boundaries.

If the Write command is issued prior to initializing a step rate, the default value of 7.5 msec is selected and a Recalibrate is performed prior to the Write.

If the heads are not positioned at the cylinder specified in the cylinder high and low registers, the controller performs an implied seek. The step rate used is determined by the step rate field of the most recently executed Restore or Seek command.

The optional long bit (L set to 1 enables Write Long.) informs the WD1002-WAH whether or not to append the Host supplied ECC bytes. These four bytes are transferred as individual bytes, not words, as is data field information. The data request bit in the status register must be valid before each byte transferred and at least 2 μsec will pass between each byte transferred.

The optional retry bit (Tset to 1 disables retries.) disables or enables retries. The WD1010A-05 automatically retries for ten disk revolutions when the retry bit is enabled. The WD1010A-05 properly sets the error and status registers if the retries are unsuccessful. Disabling retries allows only two disk revolutions before the WD1010A-05 sets the error and status registers.

The WD1002-WAH interrupt is generated as the data for each sector is required to be transferred into the Sector Buffer (except the first sector) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and the data request status is set. If the DRIVE READY signal is de-asserted or WRITE FAULT is asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

Format Track

The track specified by the task file is formatted with ID and data fields according to the interleave table transferred to the buffer. The interleave table, consists of two bytes per sector as follows:

00 PHYSICAL SECTOR 1
00 PHYSICAL SECTOR 2
00 PHYSICAL SECTOR 3
"
"
"
00 PHYSICAL SECTOR 17

The data transfer must be 512 bytes even though the table may be only 34 bytes. The sector count register must be loaded with the number of sectors per track before each Format Track command. The Format Track command supports on error reporting. A bad block may be specified by replacing a 00 table entry with and 80 Hex. When switching between drives, a Restore command must be executed prior to attempting a format. Command completion will leave all data fields initialized to zeroes. The completion interrupt is generated after each track has been formatted.

Read Verify

This command funtions similarly to a normal Read command except that data is not output to the Host. One of 256 sectors may be verified at one time. The generated ECC bytes are compared with the recorded ECC bytes for data verification. A single interrupt is generated upon completion of the command or in the event of an error.

If the Read Verify command is issued prior to initializing a step rate, the default value of 7.5 msec is selected and a recalibrate is performed prior to the Read Verify.

For ECC errors, eight retries are made at reading before a soft uncorrectable error is reported.

A retry results in the reissuing of the WD1010A-05 Read Sector command. The WD1010A-05 Read Sector command attempts to verify the sector ten times, if T is set to 1, before returning an error. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. If the error is an uncorrectable error or an error is reported by the WD1010A-05, the command terminates. The WRITE FAULT and DRIVE READY inputs are checked throughout the command's execution.

Diagnose

The Diagnose command causes the Controller to perform an onboard diagnostic and to report the result in the Error Register. An interrupt is performed upon completion of the command.

The Diagnose command performs tests on the WD1015-03's internal ROM and RAM, the WD1014-01, WD1010A-05, and the Sector Buffer. If any component fails, the appropriate error code is loaded into the error register. Error codes are as follows:

01	No errors
02	WD1010A-05 register access error
03	Sector Buffer RAM data error
04	WD1014-01 register access error
05	WD1015-03 ROM checksum or RAM data error
00,06-FF	Not used. Undefined.

In addition, the Diagnose command sets the write precomp task file register to 32. This causes write precompensation to begin at cylinder 128. (Since the write pre-comp register holds the desired value divided by four.) The sector count register is reset to one while the cylinder high, cylinder low, and SDH registers are all set to zero.

Set Parameters

This command sets up the drive parameters regarding the maximum number of heads and sectors per track. The WD1002- WAH uses these two paramenters when performing multiple sector operations. The SDH task file register specifies the drive affected. The sector count and SDH registers must be set up before this command is issued. An interrupt is set at the completion of the command.

This command must be issued before any multiple sector operations are undertaken. By setting the SDH register for each of the two possible drives, this command allows the WD1002-WAH to support two drives with different characteristics.

JUMPER OPTIONS

The WD1002-WAH does not provide configuration switches for drive parameters, interrupt selection, or drive selection. The attached drive or drives must be configured for drive select 1 or 2. The available jumper options are as follows:

W1: Primary and secondary I/O address jumper allows two controllers in one chassis. Jumpering positions 1-2 selects base primary address 1FO. Jumpering positions 2-3 selects base secondary address 170.

W2: LATCHED status register jumper. L = latched. In this mode, the WD1002-WAH diagnostics registers located at I/O address BASE + 7, 3F6 Hex, and 3F7 Hex present latched status to the Host. This mode is IBM PC AT compatible. Drive select line is semi-static.

NON-LATCHED NL = non-latched. This has certain timing implications for the disk drives. DRIVE SELECT low to status valid is 355 nsec as measured at the drive interface. The drive select lines are activated only when the controller is executing a command, or reading status at 3F6 or 3F7 Hex.

Figure 5 illustrates the location of W1 and W2.

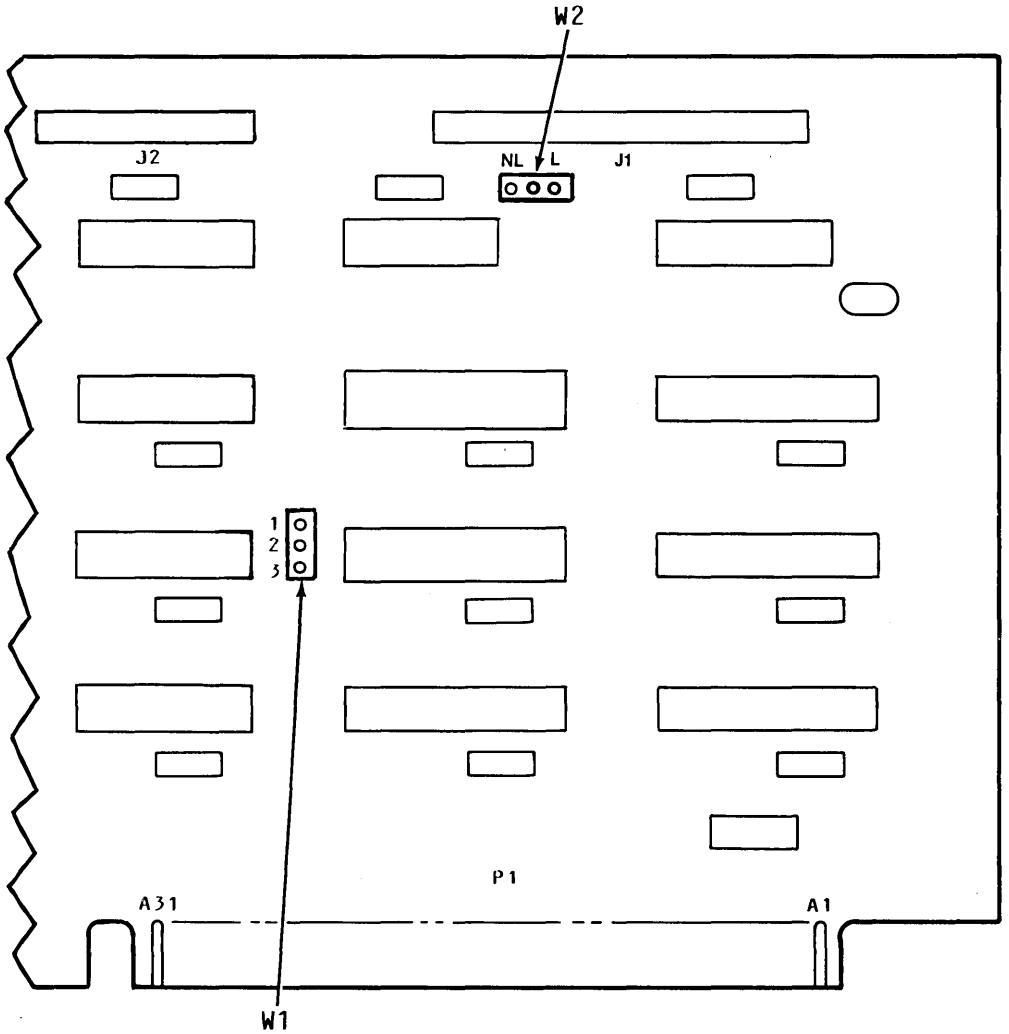


FIGURE 5. WD1002-WAH JUMPER LOCATIONS

SPECIFICATIONS

PHYSICAL

Form factor	IBM PC
Length	20.6 centimeters (8.1 inches)
Width	10.7 centimeters (4.2 inches)
Height (maximum including board, components, and leads)	1.27 centimeters (0.05 inches)

POWER AND ENVIRONMENT

Power	Current
+5V ± 5%	1.5A
+12V ± 10%	0.5mA

ENVIRONMENTAL

Temperature	
Operating	0°C (32°F) to 55°C (131°F)
Non-operating	-40°C (-40°F) to 60°C (140°F)
Humidity	
Operating	8% to 85% non-condensing
Non-operating	5% to 95% non-condensing
Shock and Vibration	
Shock	35G/20MS square wave maximum
Vibration	1G/0-600 Hz, dwell not to exceed 30 seconds at any resonance
Altitude	
Operating	0 to 3000 meters maximum (10,000 Ft)
Non-operating	0 to 5000 meters maximum (15,000 Ft)

RECORDING SPECIFICATIONS

Encoding method	MFM
Data rate	5.0Mbs
Sector format	512 bytes/sector 17 sectors/track (sectors number 01 through 17) track soft sectored format
Interleave	2:1
Drives supported	2 maximum
Heads supported	16 maximum
Tracks supported	1024 maximum
Hard error rate	less than 1 per 10(E12) bits read
Soft error rate	less than 1 per 10(E10) bits read
Seek error rate	less than 1 per 10(E06) seeks

READ/WRITE CONTROL SPECIFICATIONS

Maximum acquisition time	12.8 us @ 5.0Mbs
Capture range	> ± 2.2%
Drive Margin	± 16 ns (with pre-comp off)
Asymmetry tolerance	30nsec

ERROR CORRECTION SPECIFICATIONS

Method	Polynomial division
Degree	32
Forward polynomial	$X^{32}+X^{28}+X^{26}+X^{19}+X^{17}+X^{10}+X^{06}+X^{02}+1$
Reciprocal polynomial	$X^{32}+X^{30}+X^{26}+X^{22}+X^{15}+X^{13}+X^{06}+X^{04}+1$
Record length (r)	516 by 8 bits maximum
Correction span (b)	5 bits
Single burst detection span	r = 516 by 8 bits
with b = 0	32 bits
with b = 5	19 bits
Single burst detection span	r = 516 by 8 bits
with b = 0	> 3 bits
with b = 5	3 bits
Non-detection probability	2.3 (E-10), r = 516 by 8, b = 5
Miscorrection probability	1.57 (E-5), r = 516 by 8, b = 5

TIMING

Timing diagrams are shown in Figures 6 through 8, and the timing values are given in Table 9.

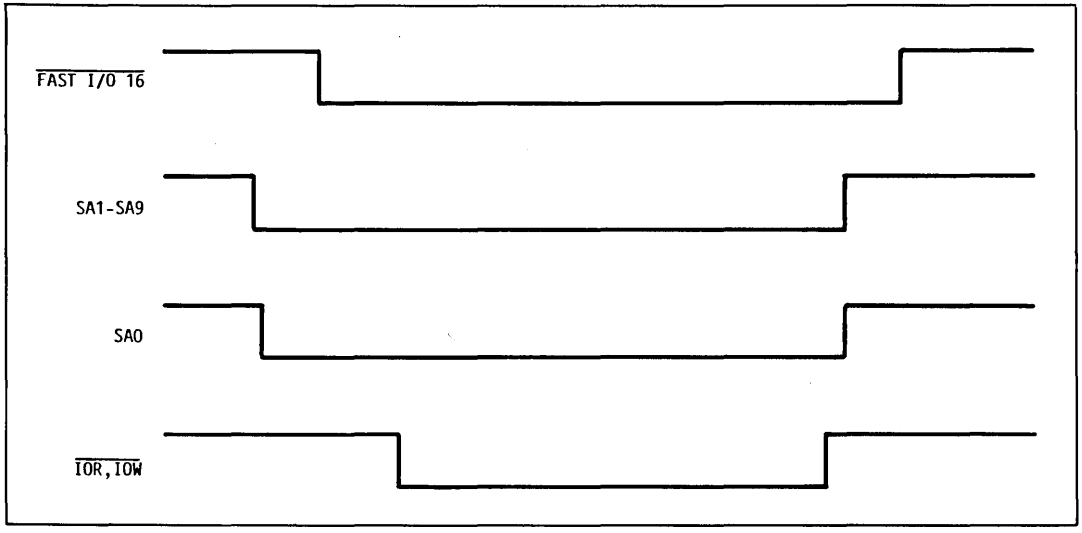


FIGURE 6. I/O CHANNEL TIMING

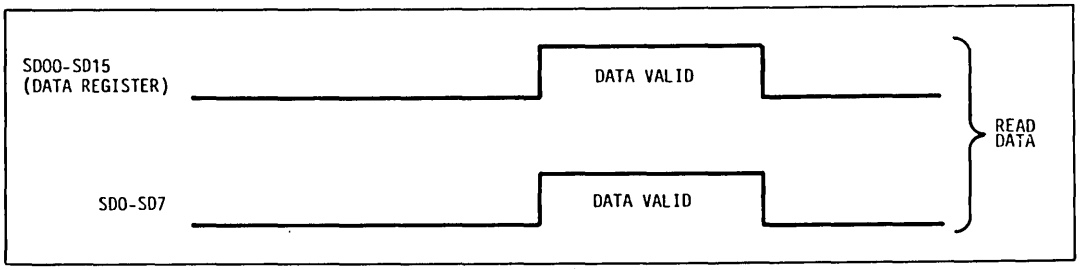


FIGURE 7. DATA REGISTER READ DATA I/O TIMING

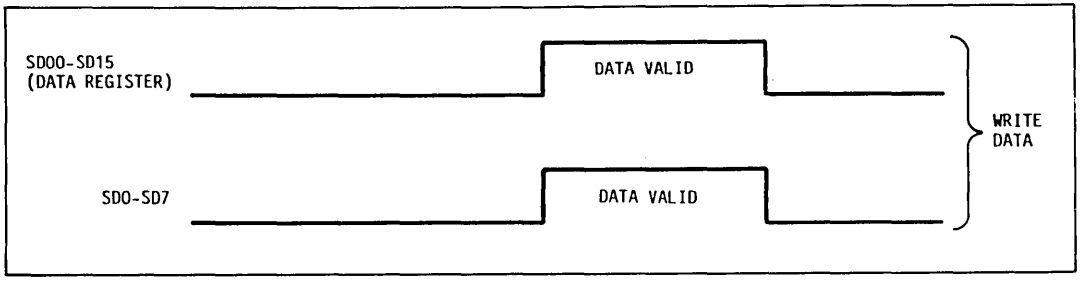


FIGURE 8. DATA REGISTER WRITE DATA I/O TIMING

TABLE 9. TIMING

DEFINITION	I/O	
	16 BIT	8 BIT
SA1-SA9 -> $\overline{\text{Fast I/O 16}}$	93 nsec max	N/A
SA0 -> $\overline{\text{Fast I/O 16}}$	73 nsec max	N/A
SA1-SA9 -> $\overline{\text{IOR}}$/$\overline{\text{IOW}}$	97 nsec min	97 nsec min
SA0-> $\overline{\text{IOR}}$/$\overline{\text{IOW}}$	77 nsec min	77 nsec min
$\overline{\text{IOR}}$/$\overline{\text{IOW}}$ Pulse Width	167 nsec min	542 nsec min
IOR/IOW -> Fast I/O 16	93 nsec max	N/A
$\overline{\text{IOR}}$ -> Data Valid	132 nsec max	498 nsec max
Data Valid -> I/OW	71 nsec min	491 nsec min
Data Hold from IOW	54 nsec min	46 nsec min
Addr Hold from IOR/IOR	47 nsec min	47 nsec min
IOR/IOW -> $\overline{\text{IOR}}$/$\overline{\text{IOW}}$	375 nsec min	375 nsec min

WD1002-WA2 Winchester/Floppy Disk Controller

FEATURES

- AT COMPATIBLE WINCHESTER AND FLOPPY CONTROLLER
- CONTROLS UP TO TWO WINCHESTER DRIVES (ST506/ST412, 16 R/W HEADS EACH)
- CONTROLS UP TO TWO FLOPPY DISK DRIVES
  DOUBLE-SIDED
  DOUBLE DENSITY (360kB, 250kbs, MFM)
  QUAD DENSITY (1.2MB, 500kbs, MFM)
  FOUR DATA RATES (500kbs, 300kbs, 250kbs, and 125kbs)
  SUPPORTS 360 AND 300 RPM SPINDLE SPEEDS
- BASED ON INDUSTRY STANDARD WD1010A-05 WINCHESTER DISK CONTROLLER
- 8-BIT, BI-DIRECTIONAL BUS HOST INTERFACE FOR CONTROL AND STATUS TRANSFERS
- HIGH-SPEED, 16-BIT PIO DATA TRANSFERS
- 32-BIT ECC FOR WINCHESTER ERROR DETECTION AND CORRECTION, CRC FOR ID FIELDS
- DIAGNOSTIC MODE FOR ERROR CHECKING
- WRITE PRECOMPENSATION LOGIC
- SINGLE CHIP WINCHESTER DATA SEPARATOR (WD10C20)
- ALLOWS CONCURRENT OPERATION OF ONE FLOPPY AND ONE WINCHESTER DRIVE

DESCRIPTION

The WD1002-WA2 is an AT bus compatible Winchester/Floppy disk controller designed to interface up to two Winchester and up to two floppy disk drives. The board permits the concurrent operation of one floppy and one fixed disk drive. The Winchester drive interface is compatible to the Seagate Technology ST506 standard interface for 5Mbs hard disk drives. The floppy disk drive interface supports 1.2MB, 360 RPM drives as well as 360kB (SA450) drives. The WD1002-WA2 includes all necessary receivers and drivers to allow direct connection to the drive(s).

ARCHITECTURE

The WD1002-WA2 is based on the WD1014-01 Error Detection/Support Logic device, WD1015-03 Buffer Manager Control Processor, WD1010A-05 Winchester Disk Controller, WD2293-07 Floppy Data Separator Control Device, WD2293-08 Floppy Clock and Support Device, and WD10C20 Winchester Data Separator and Write Precompensation Device. The WD1002-WA2 also uses two 2K x 8 static RAM devices as a 16-bit wide Sector Buffer, an analog data separator with dual VCOs for four floppy data rates, and an NEC μPD765A Floppy Disk Controller.

The WD1014-01 provides error correction for the WD1002-WA2's Winchester control circuitry. The WD1014-01 generates four ECC bytes and appends these bytes to the sector data field. The maximum error correction span is 5-bits. The WD1014-01 also selects the proper drive and head.

The WD1015-03 is an 8 bit microprocessor that controls and coordinates the activity of the Winchester disk drives, WD1010A-05, and WD1014-01. The WD1015-03 receives and sends commands or status information over the internal WD1002-WA2 multiplexed address/data bus, HD0 through HD7. Controlling firmware resides in the WD1015-03's 2K internal ROM.

The WD1010A-05 controls all data transfers between the Sector Buffer and the drives. The WD1010A-05 performs multiple sector Read/Write, Implied and Buffered Seek commands. The WD1010A-05 also executes programmable format and error recovery algorithms. All Winchester commands are executed through the seven Task Files of the WD1010A-05 after limited intervention by the WD1015-03 and WD1014-01.

The Sector Buffer is two 2KB x 8 RAMS. Since the WD1010A-05, WD1014-01, and WD1015-03 are 8-bit devices, two RAMs are used because the Host provides data in 16-bit words. An on board PAL selects the proper RAM. The Sector Buffer RAMs never contain more than 512 bytes.

The WD10C20 performs phase-locked loop data synchronization on read data from the Winchester drives. This device also conditions write data to be recorded on the disk. The WD10C20 includes both frequency and phase detection. Zero phase error start-up circuitry eliminates problems due to asymmetry. The WD10C20 requires no adjustments and contains all data separation circuitry in a single device.

The NEC μPD765A is a floppy disk controller. Host control over the NEC μPD765A is complete. No on-board processor controls the floppy controller. Floppy transfers are made in DMA mode. All floppy commands are supported.

NOTE

Refer to the NEC Microcomputer Division Catalog for more detailed information on this device. Where differences exist, the values and descriptions in this data sheet take precedence over the NEC documentation. For example, the sector size is set at 512 bytes per sector by the AT BIOS even though the NEC controller allows programmable sector sizes.

The WD2293-07 enables the analog floppy data separator to switch to one of four possible data rates. System Data Bits 0 and 1 select the floppy data transfer rate. The WD2293-07 also controls the data separator phase locked loop (PLL) and voltage controlled oscillator (VCO).

The WD2293-08 controls timing of the data rate and floppy DMA requests. Write precompensation is also provided by the WD2293-08. Write precompensation time for floppy data transfers is 125 nsec.

The analog data separator for the floppy disk controller consists of a phase detector, amplifier gain control, a bandpass filter and dual VCOs. Detection of phase error between read data and VCO input is provided by the phase detector. Amplifier gain control throttles the speed of the VCO i.e., increases the VCO speed if VCO lags the data and decreases the VCO speed if VCO leads the data. The bandpass filter adjusts the bandwidth of the data's frequency. Dual VCOs are used for different data rates.

Figure 1 is a functional block diagram of the WD1002-WA2 board.

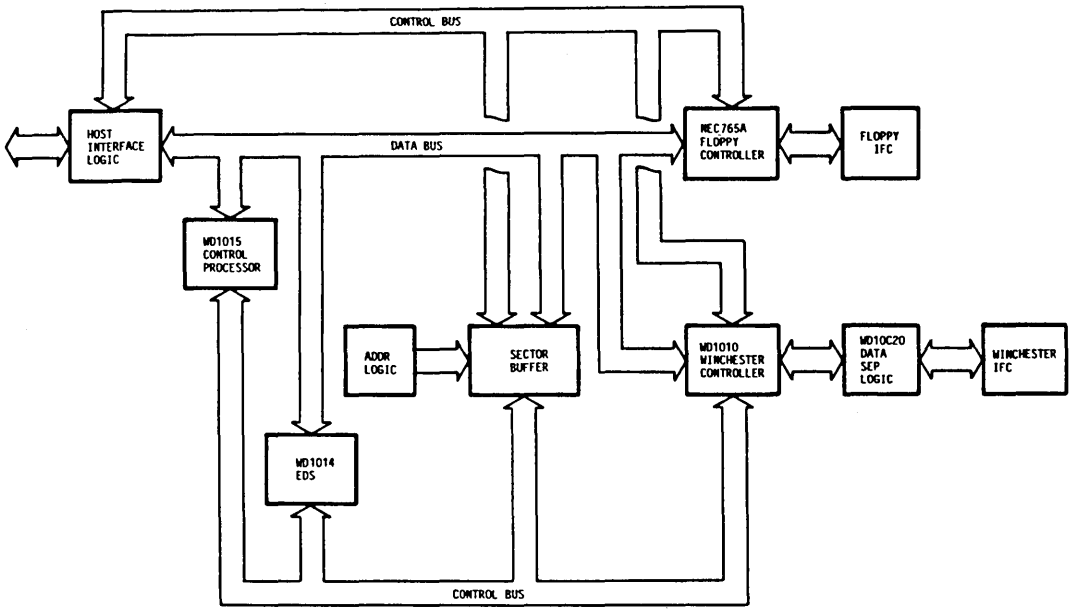


FIGURE 1. WD1002-WA2 BLOCK DIAGRAM

INTERFACE CONNECTORS

The WD1002-WA2 has seven interface connectors:

- P1 – 62-pin card edge connector
  Component side – Pins A1 through A31
  Conductor side – Pins B1 through B31
- P1' – 36-pin card edge connector
  Component side – Pins C1 through C18
  Conductor side – Pins D1 through D18
- J 5 – Winchester control cable connector
- J 4 – Winchester drive 1 data cable connector
- J 3 – Winchester drive 2 data cable connector
- J 1 – Floppy control and data cable connector (daisy-chained)
- J 6 – LED Winchester drive connector

The pin descriptions of the connectors are given in Tables 1 through 5.

HOST INTERFACE CONNECTORS

The WD1002-WA2 Controller interfaces with the 16-bit, bi-directional data bus by means of the two card edge connectors P1 and P1'. The pin descriptions for P1 are given in Table 1 and P1', in Table 2.

TABLE 1. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
A1,A10, A12 thru A21	NC			
A2 thru A9	SD7 thru SD0	DATA BUS BITS 7 THRU 0	I/O	Bi-directional, lower 8-bit data bus for data and status communication between the controller and the Host.
All	AEN	ADDRESS ENABLE	I	When AEN is asserted, the DMA controller assumes control of the Host address bus, control bus, and data bus. I/O port addresses are no longer generated for I/O port access. In this mode, the I/O port is selected by asserting $\overline{\text{DACK2}}$.
A22 thru A31	A9 thru A0	ADDRESS BUS BITS 9 thru 0	I	A 10-bit address bus for I/O port addressing by the Host.
B1,B10 B31	GND	GROUND		
B2	RST	RESET	I	When asserted, RST forces the WD1002-WA2 board into the initial power-up state.
B3,B29	+5VDC	+5VDC		+5VDC
B6	DRQ2	DMA REQUEST CHANNEL 2		DRQ2 is asserted whenever data are available for transfer to or from the WD1002-WA2 under DMA control. Applies to floppy controller only.
B7	-12VDC	-12VDC		-12VDC
B9	+12VDC	+12VDC		+12VDC

TABLE 1. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION (CONT'D)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
B4,B5, B8,B11, B12	NC			
B13	$\overline{IOW}$	$\overline{I/O\ WRITE}$	I	$\overline{IOW}$ is asserted when the DMA Controller or Host writes a data, status, or control byte to the WD1002-WA2.
B14	$\overline{IOR}$	$\overline{I/O\ READ}$	I	$\overline{IOR}$ is asserted when the DMA controller or Host reads a data from the WD1002-WA2.
B15 thru B21	NC			
B22	IRQ6	INTERRUPT REQUEST 6	O	IRQ6 is asserted to interrupt the Host upon completion of a command. Applies to floppy controller only.
B23,B24				
B25	NC			
B26	$\overline{DACK2}$	$\overline{DMA\ ACKNOWLEDGE\ CHANNEL\ 2}$	0	$\overline{DACK2}$ is asserted in response to DMA request channel 2.
B27	T/C	TERMINAL COUNT	I	Indicates sending of the last byte in a floppy disk transfer.
B28	ALE	ADDRESS LATCH ENABLE	I	Indicates board address is available.
B29	+5V	+5V		
B30	NC			

TABLE 2. HOST INTERFACE CONNECTOR (P1') PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
C1 thru C10	NC			
C11 thru C18	SD8 thru SD15	DATA BIT 8 thru DATA BIT 15	I/O	Bi-directional, upper 8-bit data bus for data transfers only between the controller and the Host.
D1	NC			
D2	$\overline{\text{I/O CS 16}}$	$\overline{\text{I/O 16-BIT CHIP SELECT}}$	I	$\overline{\text{I/O CS 16}}$ signals the system board that the current data transfer is a 1 wait-state, 16-bit I/O cycle, derived from an address decode.
D3 thru D6	NC			
D7	IRQ14	INTERRUPT REQUEST 14		IRQ14 signals the Host that the Winchester controller needs attention. IRQ is generated when the IRQ line goes from low to high.
D8 thru D15,D17	NC			
D16	+5VDC	+5VDC		+5VDC
D18	GND	GROUND		

WINCHESTER DRIVE CONTROL CONNECTOR J5

The Winchester drive control cable connector is a 34-pin printed circuit card edge connector daisy-chained to each drive in the system. To terminate the control signals on the WD1002-WA2 properly, the last drive on the daisy chain must have a 220/330 ohm resistor pack installed. Pin descriptions and control signals for the drive control connector J5 are given in Table 3.

TABLE 3. WINCHESTER DRIVE CONTROL CONNECTOR (J5) PIN DESCRIPTION

SIGNAL				I/O	FUNCTION
GND	PIN	MNEMONIC	NAME		
1	2	HS3/RWC	HEAD SELECT3/ REDUCE WRITE CURRENT	O	The WD1002-WA2 uses HS3 to select one of 16 R/W heads. RWC is not used by drives with 16 head drives. RWC is used by drives with 8 R/W heads. RWC reduces the write current on the inner cylinders. This lessens the bit shift caused by greater bit density on these cylinders.
3	4	HS2	HEAD SELECT2	O	HS2 is one of the head select signals decoded by the drive to select one of eight (or 16) R/W heads.
5	6	WG	WRITE GATE	O	WG is asserted when valid data is to be written on disk. The WD1002-WA2 de-asserts WG when WF is detected. Special circuitry is included to ensure the system output is free of glitches during power-on.
7	8	SC	SEEK COMPLETE	I	SC informs the WD1002-WA2 that the head of a selected drive has reached the desired cylinder and has stabilized.
9	10	TK000	TRACK000		TK000 is asserted when the R/W heads are positioned over the outermost cylinder.
11	12	WF	WRITE FAULT		WF is asserted by the selected drive when a write error occurs. While this signal is being asserted, the command in progress aborts and no other disk command can be executed.
13	14	HS0	HEAD SELECT0	O	HS0 is one of the head select signals decoded by the drive to select one of eight (or 16) R/W heads.
15*	16	NC			
17	18	HS1	HEAD SELECT1	O	HS1 is one of the head select signals decoded by the drive to select one of eight (or 16) R/W heads.
19	20	INDEX	INDEX PULSE	I	INDEX indicates the start of a track. Used as a synchronization point during formatting and as a time-out mechanism for retries. Pulses once each disk revolution.
21	22	DRDY	DRIVE READY	I	DRDY informs the controller that the drive motor is up to speed.
23	24	STEP	STEP PULSE	O	STEP, with DIRIN, positions the heads to the desired cylinder. STEP pulses once for each step. DIRIN determines the step direction.
25	26	DS0	DRIVE SELECT0	O	DS0 is used to select drive 0.
27	28	DS1	DRIVE SELECT1	O	DS1 is used to select drive 1.
29, 31		GND			
	30, 32	NC			
33	34	DIRIN	DIRECTION IN	O	DIRIN determines the direction in which the R/W heads move when the step line is pulsed. De-asserted = out; asserted = in.

*Pin 15 is reserved to polarize the connector.

WINCHESTER DATA CONNECTORS J4, J3

The data lines between the Controller and the two Winchester disk drives are connected to J4 and J3. As the data lines are not identical, J4 must be connected to the cable from Winchester drive 1 and J3, to the cable from Winchester drive 2. Each drive is radially connected with a maximum cable length of 3 meters (10 feet). Each data connector is a 20-pin vertical header on 0.25 mm (0.01 inch) center. Data connector pin descriptions and signals are listed in Table 4.

TABLE 4.
WINCHESTER DRIVE DATA CONNECTORS (J3, J4)
PIN DESCRIPTION

SIGNAL			
GND	PIN	I/O	SIGNAL NAME
	1		NC
2			GND
	3		NC
4			GND
	5		NC
6			GND
	7		NC
8*			
	9		NC
	10		NC
11			GND
12			GND
	13	O	+MFMD Write Data
	14	O	-MFMD Write Data
15			GND
16			GND
	17	I	+MFMRD Read Data
	18	I	-MFMRD Read Data
19			GND
20			GND

*Pin 8 is reserved to polarize the connector

TABLE 5. FLOPPY DRIVE CONTROL AND DATA CONNECTOR (J1) PIN DESCRIPTION

SIG GND	SIG PIN	SIGNAL MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	2	WCCNTRL-	WRITE-CURRENT-CONTROL-	0	Inverted Form of SDO for read data. Selection of 300kbs data rate asserts WCCNTRL.
1	4	NC			
5					Pin 5 is reserved to polarize the connector.
	6	NC			
7	8	INDEX-	INDEX-	I	Assertion indicates start of a track
9	10	MOTEN1-	MOTOR-ENABLE1-	O	MOTEN1- (MOTEN2-) turns on the floppy disk drive spindle.
15	16	MOTEN2-	MOTOR-ENABLE2-	O	MOTEN1- (MOTEN2-) and the appropriate drive select signal must be asserted at the same time.
11	12	DS2-	DRIVE-SELECT2-	0	Assertion selects drive 2. MOTEN2- must be asserted at the same time as DS2-.
13	14	DS1	DRIVE-SELECT1-	O	Assertion selects drive 1. MOTEN1- must be asserted at the same time as DS1-.
17	18	DIR	DIRECTION	O	Assertion moves the selected read/write head inward. De-assertion moves the selected read/rite head outward.
19	20	STEP-	STEP-PULSE-	O	Assertion moves the read/write head one track at a time. The head moves in direction determined by the DIR- signal.
21	22	WRT DATA-	WRITE-DATA-	O	MFM data.
23	24	WRT EN-	WRITE-DATA-	O	Assertion enables the writing of data on an unprotected diskette.
25	26	$\overline{\text{TRK0}}$	$\overline{\text{TRACK0}}$	I	Assertion indicates that the read/write head is over the outermost track.
27	28	$\overline{\text{WRT PROT}}$	$\overline{\text{WRITE PROTECT}}$	I	Assertion indicates a write protected diskette.
29	30	$\overline{\text{READ DATA}}$	$\overline{\text{READ DATA}}$	I	MFM Read Data.
31	32	$\overline{\text{HS1}}$	$\overline{\text{HEAD}}$	O	Assertion selects head 1.
33	34	$\overline{\text{DISKETTE CHG}}$	$\overline{\text{DISKETTE CHANGE}}$	I	Assertion indicates drive is not ready i.e., drive door open, no diskette in drive, or improper assertion of motor enable or drive select signals.

WINCHESTER FORMAT

The format used for Winchester disk track formatting is shown in Figure 2. The ID and data fields on any disk are initialized by the Format command.

NOTES

1. GAP 1 and 3 length equals 22 bytes
2. Decision to assert RG is made two bytes after the start of DRUN
3. RG is de-asserted:
   - If DRUN does not last until A1
   - When any part of the ID does not match the one that is expected
   - After CRC, if correct ID has been read.
4. Write splice recorded on disk by asserting WG.
5. RG is suppressed until after write splice.
6. Not a proper A1 or F8, set DAM error.
7. Sector size as stated in ID field, plus four for ECC.

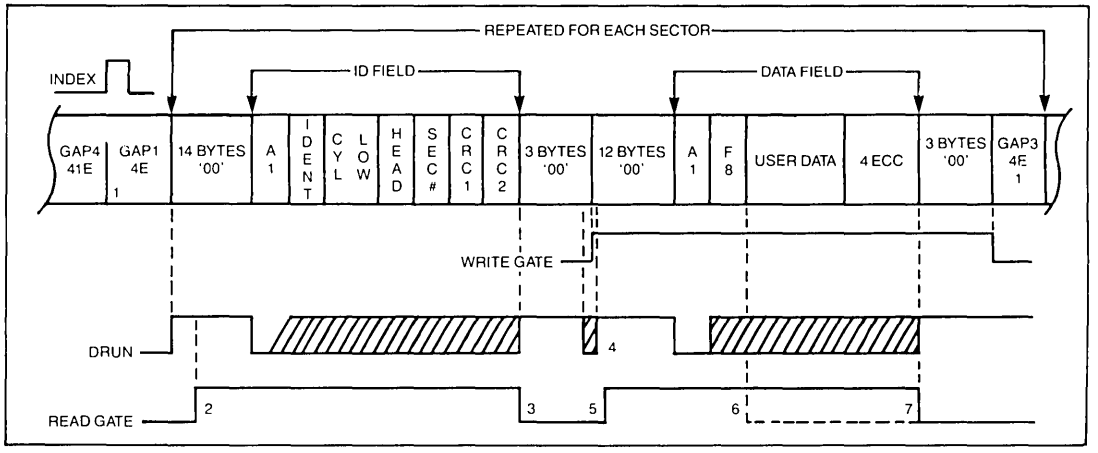
ID FIELD

A1 = A1 Hex with 0A Hex clock
IDENT = Bits 1,0 = Cylinder High
FE = 0-255 Cylinders
FF = 256-511 Cylinders
FC = 512-767 Cylinders
FD = 768-1023 Cylinders
HEAD = Bits 0,1,2 = Head Number
Bits 3,4 = 0
Bits 5,6 = Sector Size
Bit 7 = Bad Block Mark
Sec # = Logical Sector Number

DATA FIELD

A1 = A1 Hex with 01 Hex clock
F8 = Data Address Mark: Normal Clock
USER = Data Field 512 Bytes

FIGURE 2. WINCHESTER DISK FORMAT



REGISTER ADDRESS MAP

The WD1002-WA2 contains seven Read/Write task file registers in the WD1010A-05, a 16-bit Data Register, Digital Output and Input Registers, Alternate Fixed Disk Status Register and fixed Disk Register. The WD2293-07 and WD2293-08 contain a 2-bit Floppy Control Register in each device. Main Floppy Status and Data Registers are in the NEC „PD765A. These registers are mapped into either a primary or secondary I/O address. All Winchester data, control, and status information pass between the task files or Data Register and the Host. All floppy data, control, and status information pass between the floppy registers. All Winchester data transfers between the Host and Data Register are word transfers except ECC bytes in Read Longs and Write Longs. These ECC bytes are transferred in byte mode. Control and status bytes are also transferred between the Host in byte mode. The task file registers are multiplexed with IOR- and IOW- to give 14 possible ports. Five of the eight task file registers are bi-directional. Two of the task file registers have different definitions for read and write operation. Jumpers select the primary and secondary address. This allows two controllers in the same Host system. However, secondary ports on the WD1002-WA2 are NOT supported by any version of DOS.

Table 6 summarizes the WD1002-WA2 I/O port address map. Figure 3 summarizes the WD1010A-05 task file registers and bit assignments. Figure 4 summarizes the other I/O registers and bit assignments for the WD1002-WA2. Bit assignments are with respect to the Host lower byte bus terms, SD7 through SD0. The fixed size/drive/head (SDH) and status registers in the WD1010A-05 descriptions slightly differ from the standard descriptions in the WD1010-05 data sheet. Please note that the SDH register is set for the ECC option mode and 512 bytes per track. The SDH register also limits the number of drives to two and the number of heads to 16. Bit 2 of the WD1010A-05 status register is designated as the Corrected Data bit. Assertion (setting to 1) of this bit indicates the sector read from the drive resulted in a correctable ECC error. Soft errors do not end multiple sector transfers. Bit 1 of the WD1010A-05 status register is designated as the Index bit. Assertion of this bit occurs each revolution of the currently selected drive. Refer to the WD1010-05 data sheet for a complete description of all other WD1010A-05 bit assignments. Table 7 describes the bit assignments for the other WD1002-WA2 control and status registers.

NOTE

Where differences exist, the values and descriptions for Figure 3 take precedence over the WD1010-05 data sheet.

TABLE 6. WD1002-WA2 REGISTER ADDRESS MAP

I/O ADDRESS		READ	WRITE
PRIMARY	SECONDARY		
DATA REGISTER			
1FO	170	DATA REGISTER (16 bits)	DATA REGISTER (16 bits)
WD1010A-05 TASK REGISTERS			
1F1	171	ERROR REGISTER	WRITE PRE-COMP
1F2	172	SECTOR COUNT	SECTOR COUNT
1F3	173	SECTOR NUMBER	SECTOR NUMBER
1F4	174	CYLINDER NUMBER (low byte)	CYLINDER NUMBER (low byte)
1F5	175	CYLINDER NUMBER (high byte)	CYLINDER NUMBER (high byte)
1F6	176	SDH REGISTER	SDH REGISTER
1F7	177	STATUS REGISTER	COMMAND REGISTER
CONTROL AND STATUS REGISTERS			
3F2	372		DIGITAL OUTPUT REGISTER
3F4	374	MAIN FLOPPY STATUS REGISTER (NEC uPD765A)	MAIN FLOPPY STATUS REGISTER NEC uPD765A)
3F5	375	FLOPPY DATA REGISTER NEC u765A)	FLOPPY DATA REGISTER (NEC u765A)
3F6	376	ALTERNATE FIXED STATUS REGISTER	FIXED DISK
3F7	377	DIGITAL INPUT REGISTER	FLOPPY CONTROL REGISTER (WD2293-07 and -08)

NOTE

All addresses in Table 6 are in Hex. A Read or Write to I/O address 1FO Hex (170 Hex) is a Read or Write for the Sector Buffer. Therefore, the hardware for the 16-bit Data Register is the Sector Buffer.

REGISTER	7	6	5	4	3	2	1	0
WRITE PRE-COMP	CYLINDER NUMBER DIVIDED BY 4							
ERROR	BB	ECC	0	ID	0	AC	TK	DM
SECTOR COUNT	NUMBER OF SECTORS							
SECTOR NUMBER	SECTOR NUMBER							
CYLINDER NO.	CYLINDER NUMBER (LOW BYTE)							
CYLINDER NO.	0	0	0	0	0	0	CYL.	NO. MSB
SDH	1	0	1	DS	HS3	HS2	HS1	HS0
COMMAND	COMMAND							
STATUS	BSY	RDY	WF	SC	DRQ	CRD	IDX	ERR

FIGURE 3. WD1010A-05 TASK FILE REGISTER BIT ASSIGNMENT

REGISTER	7	6	5	4	3	2	1	0
DIGITAL OUTPUT	X	X	MOEN2	MOEN1	FDMAEN	FRST	X	FDSEL
MAIN FLOPPY STATUS	RQM	DIO	EXM	CB	X	X	D1B	D0B
ALTERNATE STATUS	BSY	RDY	WF	SC	DRQ	CRD	IDX	ERR
FIXED DISK	0	0	0	0	HS3EN	RST	IEN-	0
DIGITAL INPUT	DCHG	WTG-	HS3-/RWC-		HS2-	HS1-	HS0-	DS2-	DS1-
FLOPPY CONTROL	TWO BIT REGISTERS IN WD2293-07 AND -08						SDB1	SDB0

FIGURE 4. WD1002-WA2 CONTROL AND STATUS REGISTER

TABLE 7. WD1002-WA2 CONTROL AND STATUS REGISTER BIT DEFINITIONS

REGISTER	BIT MNEMONIC	BIT NAME
DIGITAL OUTPUT	X	Reserved
	MOEN2 MOEN1	MOTOR ENABLE 2 and MOTOR ENABLE1. Controls floppy drive motors. Setting this bit to 0 turns off the associated drive and drive selection can not occur.
	FDMAEN	FLOPPY DISK INTERRUPT and DMA ENABLE. Setting this bit to 1 gates floppy disk DMA and interrupt requests to the I/O interface. Setting to 0 disables the DMA and interrupt request drivers.
	FRST	Setting to 0 resets floppy controller. Floppy reset time is 3.5 usec. Set to 1 by Host software enables the floppy controller.
	FDSEL	FLOPPY DISK SELECT. Set to 0 selects drive A. Set to 1 selects drive B. Appropriate MOTOR ENABLE bit must be set.
MAIN FLOPPY STATUS	X	Reserved
	RQM	REQUEST FOR MASTER. Set to 1 to indicate that the floppy data register is ready for a data transfer. Used with DIO bit.
	DIO	DATA INPUT/OUTPUT. Controls data transfer direction. Set to 0 to indicate data transfer is from Host to floppy controller. Set to 1 to indicate data transfer is to Host from floppy controller.
	EXM	EXECUTION MODE. Set to 1 only during the execution phase in non DMA mode.
	CB	Set to 1 to indicate a Read or Write command in process.
	D1B	Set to 1 when floppy drive B is in Seek mode.
	D0B	Set to 1 when floppy drive A is in Seek mode.

TABLE 7 WD1002-WA2 CONTROL AND STATUS REGISTER BIT DEFINITIONS

REGISTER	BIT MNEMONIC	BIT NAME
ALTERNATE FIXED DISK STATUS	BSY	Controller Busy Flag Ready from selected drive Write Fault from selected drive.
	RDY	
	WF	Seek Complete from selected drive.
	SC	Data Transfer Request Flag Corrected Data Flag from WD1015-03 Index pulse from selected drive.
	DRQ	
	CRD	Error Flag from WD1015-03 Index pulse from selected drive.
	IDX	
	ERR	Error Flag from WD1015-03 Set to 1: Enables HS3–.
FIXED DISK	HS3EN	Set to 0: Enables RWC–.
	RST	Reset. Program Controlled reset to board. This bit maintains the WD1002-WA2 logic reset as long as this is on. This bit must be on for a minimum of 5.0usec. After the bit is on for the minimum time, the bit must be turned off to complete reset function.
	IEN–	Interrupt Enable. Enables or disables IRQ14. This bit does not clear the interrupt level in the disabled state. A pending interrupt would occur when the interrupt is enabled again. A system master reset clears the interrupt but leaves the interrupt enabled.
DIGITAL INPUT	DCHG	DISKETTE CHANGE. Set to 1 if no diskette is in the drive, drive door is open, or the drive is not ready.
	WTG-	Write Gate on
	HS3- (RWC-) through HS0-	Drive head select or RWC- (bit 5) for drives using RWC- DS2-, DS1- Drive select
FLOPPY CONTROL	SDB1, SDB0	The WD2293-07 and WD2293-08 each contain a two bit Floppy Control register. These registers control the data transfer rate between the controller and drive and the data encoding format. The Floppy control registers bit definitions are as follows: SDB1 SDB0 0 0 500kbs MFM* 0 1 300kbs MFM 1 0 250kbs MFM 1 1 125kbs FM**

* Default data rate after Reset.

** International exchange standard for 5 1/4 inch floppy diskettes.

WINCHESTER COMMANDS

The WD1002-WA2 Winchester command set contains eight commands. Five commands (Restore, Seek, Read Sector, Write Sector, and Format Track) are executed through the WD1010A-05 commmand register. (A sixth WD1010A-05 command, Scan ID is not directly available to the Host. Scan ID may be executed by the WD1015-03 transparently to the Host.) The three remaining commands (Read Verify, Diagnose, and Set Parameters) are executed through the WD1015-03.

Table 8 describes the eight WD1002-WA2 Winchester commands and their bit assignments. The next section describes a typical Winchester command sequence. Each Winchester command is described following the command sequence.

TABLE 8. COMMANDS AND COMMAND CODES

COMMAND	BITS							
Restore	0	0	0	1	R3	R2	R1	R0
Seek	0	1	1	1	R3	R2	R1	R0
Read Sector	0	0	1	0	0	0	L	T
Write Sector	0	0	1	1	0	0	L	T
Format Track	0	1	0	1	0	0	0	0
Read Verify	0	1	0	0	0	0	0	T
Diagnose	1	0	0	1	0	0	0	0
Set Parameters	1	0	0	1	0	0	0	1

LEGEND

R3 through R0 Step rate selection bits. Refer to Table 8 for more detailed information.

L Read or Write Long bit. Set to 1 enables Read or Write Long mode.

T Retry bit. Set to 1 disables retries.

The stepping rates for the commands that perform implied seeks are set in the least significant nibble of the last executed RESTORE or SEEK command. Table 9 describes the Winchester step rates.

TABLE 9. STEPPING RATE

R3	R2	R1	R0	STEPPING RATE	R3	R2	R1	R0	STEPPING RATE
0	0	0	0	35usec	1	0	0	0	4.0msec
0	0	0	1	0.5msec	1	0	0	1	4.5msec
0	0	1	0	1.0msec	1	0	1	0	5.0msec
0	0	1	1	1.5msec	1	0	1	1	5.5msec
0	1	0	0	2.0msec	1	1	0	0	6.0msec
0	1	0	1	2.5msec	1	1	0	1	6.5msec
0	1	1	0	3.0msec	1	1	1	0	7.0msec
0	1	1	1	3.5msec	1	1	1	1	7.5msec

Note: After Diagnose or reset, stepping rate defaults to 7.5 msec

WINCHESTER COMMAND SEQUENCE DESCRIPTION

This section secribes a typical Winchester command execution sequence. The description illustrates the relationship between Host and the major components of the WD1002-WA2 during command execution.

In the idle state: the WD1010A-05 drive control signals are off. The controller status indicates ready. Drive status is valid. Controller interrupt is enabled but not asserted. The WD1015-03 is idle and is monitoring the WAKEUP signal input.

The Host outputs the command parameters to the WD1010A-05 task file, the operation command (Seek, Read or Write) and the command attributes (Long mode, retry control, etc.). For write operations, the Host also outputs the sector or format data.

The command byte is intercepted by the WD1014-01 and is held for later interpretation by the WD1015-03.

A Read command output sets the module Wakeup latch that causes the controller status to indicate Busy and the WD1015-03 WAKEUP signal to be asserted. Write and Format commands first set the data request status signal DRQ. This initiates the Host data transfer. Completion of the data transfer (512 or 516 bytes) sets the WD1015-03 WAKEUP signal and Busy status.

The WD1015-03 examines the command, verifies command parameters, and passes the command to the WD1010A-05 for execution.

The WD1010A-05 executes the command providing drive positioning, data transfer control, error monitoring and completion status. The WD10C20 provides drive read and write data control for commands that require data transfers.

On command completion, the WD1010A-05 interrupts the WD1015-03. The WD1015-03 examines the command, status etc. for any additional requirements. If completion is indicated, the WD1015-03 sets the controller status to indicate ready and interrupts the Host.

The WD1002-WA2 returns to the idle state and the Host may examine drive and controller status, read input data, etc. as required to complete the operation.

WINCHESTER COMMAND DESCRIPTION

RESTORE

The Restore command is used to move the R / W heads to the Track 000 position. The controller issues step pulses to the drive until the Track 000 indicator from the drive is asserted. If Track 000 is not asserted within 1023 steps, the Error Error bit in the Status Register is set and a Track 000 error is posted in the Error Register. The implied seek step rate may be set up according to Table 8 by the Restore command. The restore step rate is established by the seek complete signal from the drive, i.e., each step pulse is issued only after seek complete is asserted by the drive from the previous step. If the DRIVE READY- signal is de-asserted or WRITE FAULT- is asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

SEEK

This command moves the R / W heads to the cylinder specified in the task file cylinder high and low registers. The implied seek step rate is also set by this command. The lower order four bits of the command are used to select one of 16 available step rates. An interrupt is generated at the completion of the command. If the DRIVE READY- signal is de-asserted or WRITE FAULT- is asserted, this command is terminated with the error bit set in the status register and the error register reports an aborted command.

READ SECTOR

A number of sectors (1 - 256) can be read from the selected drive with this command. The sector count register in the task file determines the number of sectors to be transferred. Multiple sector reads may cross head and cylinder boundaries.

If the Read command is issued prior to initializing a step rate, the default value of 7.5msec is selected and a Recalibrate is performed prior to the Read.

If the R / W heads are not positioned over the target track, the controller performs an implied seek to the proper cylinder. The stepping rate used during the implied seek is the value specified during the previous Seek or Restore command.

The optional long bit (L set to 1 enables Read Long.) informs the WD1002-WA2 whether or not to include the four ECC bytes. These four ECC bytes are transferred as individual bytes, not words, as is the data field information. The data request bit in the status register must be valid before each byte transferred and at least 2usec will pass between each byte transferred.

Data errors up to 5 bits in length will be automatically corrected on normal Read commands. If an uncorrectable error occurs, the data transfer will still take place, a multi-sector read, however, will terminate after the sector in error is read by the system.

The optional retry bit (T set to 1 disables retries.) disables or enables retries. The WD1010A-05 automatically retries for ten disk revolutions when the retry bit is enabled. The WD1010A-05 properly sets the error and status registers if the retries are unsuccessful. Disabling retries allows only two disk revolutions for automatic retries before the WD1010A-05 sets the error and status registers.

For ECC errors, eight Read retries are made at reading before a soft uncorrectable error is reported. A Read retry results in the reissuing of the WD1010A-05 Read Sector command. The WD1010A-05 Read Sector command attempts to verify the sector ten times, if T is set to 1, before returning an error. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. If the error is an uncorrectable error or an error is reported by the WD1010A-05, the command terminates.

Interrupts occur as each sector is ready to be read by the system. No interrupt is generated at the end of the command. If the DRIVE READY- signal is de-asserted or WRITE FAULT- asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

WRITE SECTOR

A number of sectors (1 - 256) can be written to the selected drive. The sector count register in the task file determines the number of sectors to be transferred. Multiple sector writes may cross head and cylinder boundaries.

If the Write command is issued prior to initializing a step rate, the default value of 7.5msec is selected and a Recalibrate is performed prior to the Write.

If the heads are not positioned at the cylinder specified in the cylinder high and low registers, the controller performs an implied seek. The step rate used is determined by the step rate field of the most recently executed Restore or Seek command.

The optional long bit (L set to 1 enables Write Long.) informs the WD1002-WA2 whether or not to append the Host supplied ECC bytes. These four bytes are transferred as individual bytes, not words, as is data field information. The data request bit in the status register must be valid before each byte transferred and at least 2usec will pass between each byte transferred.

The optional retry bit (T set to 1 desables retries.) disables or enables retries. The WD1010A-05 performs up to ten automatic retries when the retry bit is enabled. The WD1010A-05 properly sets the error and status registers if the retries are unsuccessful. Disabling retries allows only two automatic retries before the WD1010A-05 sets the error and status registers.

The WD1002-WA2 interrupt is generated as the data for each sector is required to be transferred into the Sector Buffer (except the first sector) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and the data request status is set. If DRIVE

READY- signal is de-asserted or WRITE FAULT- is asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

FORMAT TRACK

The track specified by the task file is formatted with ID and data fields according to the interleave table transferred to the buffer. The interleave table, consists of two bytes per sector as follows:

00 PHYSICAL SECTOR 1
00 PHYSICAL SECTOR 2
00 PHYSICAL SECTOR 3
.
.
.
00 PHYSICAL SECTOR 17

The data transfer must be 512 bytes even though the table may be only 34 bytes. The sector count register must be loaded with the number of sectors per track before each Format Track command. The Format Track sommand supports no error reporting. A bad block may be specified by replacing a 00 table entry with an 80 hex. When switching between drives, a Restore command must be executed prior to attempting a format. Command completion will leave all data fields initialized to zeroes. The completion interrupt is generated after each track has been formatted.

READ VERIFY

This command functions similarly to a normal Read command except that data is not output to the Host. One to 256 sectors may be verfied at one time. The generated ECC bytes are compared with the recorded ECC bytes for data verification. A single interrupt is generated upon completion of the command or in the event of an error.

If the Read Verify command is issued prior to initializing a step rate, the default value of 7.5msec is selected and a recalibrate is performed prior to the Read Verify.

For ECC errors, eight Read retries are made at reading before a soft uncorrectable error is reported. A Read retry results in the reissuing of the WD1010A-05 Read Sector command. The WD1010A-05 Read Sector command attempts to verify the sector ten times, if T is set to 1, before returning an error. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. If the error is an uncorrectable error or an error is reported by the WD1010A-05, the command terminates. The WRITE FAULT- and DRIVE READY- inputs are checked throughout the command's execution.

DIAGNOSE

The Diagnose command causes the Controller to perform an on-board diagnostic and to report the result in the Error Register. An interrupt is performed upon completion of the command.

The Diagnose command performs tests on the WD1015-03's internal ROM and RAM, the WD1014-05, and the Sector Buffer. If any component fails, the appropriate error code is loaded into the error register. Error codes are as follows:

01	No errors
02	WD1010A-05 register access error
03	Sector Buffer RAM data error
04	WD1014-01 register access error
05	WD1015-03 ROM checksum or RAM data error
00, 06-FF	Not used. Undefined.

In addition, the Diagnose command sets the write precomp task file register to 32. This causes write precompensation to begin at cylinder 128. (Since the write pre-comp register holds the desired value divided by four.) The sector count register is reset to one while the cylinder high, cylinder low, and SDH registers are all set to zero.

SET PARAMETERS

This command sets up the drive parameters regarding the maximum number of heads and sectors per track. The WD1002-WA2 uses these two parameters when performing multiple sector operations. The SDH task file register specifies the drive affected. The sector count and SDH registers must be set up before this command is issued. An interrupt is set at the completion of the command.

This command must be issued before any multiple sector operations are undertaken. By setting the SDH register for each of the two possible drives, this command allows the WD1002-WA2 to support two drives with different characteristics.

FLOPPY COMMANDS AND FLOPPY COMMAND SEQUENCE

The WD1002-WA2 supports all NEC uPD765A commands. Table 10 lists the NEC uPD765A commands and command codes. Refer to the NEC Microcomputer Division Catalog for further descriptions of the floppy disk controller commands, command protocols and command sequence.

TABLE 10. COMMAND CODE DESCRIPTION

COMMAND	COMMAND CODES							
	SDB7	SDB6	SDB5	SDB4	SDB3	SDB2	SDB1	SDB0
READ DATA*	MT	MF	SK	0	0	1	1	0
READ DELETED DATA*	MT	MF	SK	0	1	1	0	0
WRITE DATA*	MT	MF	0	0	0	1	0	1
WRITE DELETED DATA*	MT	MF	0	0	1	0	0	1
READ TRACK*	0	MF	SK	0	0	0	1	0
READ ID*	0	MF	0	0	1	0	1	0
FORMAT TRACK*	0	MF	0	0	1	1	0	1
SCAN EQUAL*	MT	MF	SK	1	0	0	0	1
SCAN LOW OR EQUAL*	MT	MF	SK	1	1	0	0	1
SCAN HIGH OR EQUAL*	MT	MF	SK	1	1	1	0	1
SENSE DRIVE STATUS*	0	0	0	0	0	1	0	0
SEEK*	0	0	0	0	1	1	1	1
RECALIBRATE**	0	0	0	0	0	1	1	1
SENSE INTERRUPT STATUS	0	0	0	0	1	0	0	0
SPECIFY	0	0	0	0	0	0	1	1
			SRT			HUT		
				HLT				ND
INVALID	Invalid command codes: No operation - floppy controller enters standby state.							

*Second byte of command code for these commands is as follows:
SDB7 through SDB3: Set to zero. SDB2: HD. SDB1: 0. SDB0: 0
**Second byte of command code for Recalibrate is as follows:
SDB7 through SDB0: Set to zero.

LEGEND

MT	Multi-track	Set to one for multi-track operation. If set to one after execution of Read / Write operation on side 0, floppy controller automatically searches for sector 1, side 1.
MF	FM / MFM mode	Set to zero for FM. Set to one for MFM:
SK	Skip	Set to one to skip deleted data address mark.
HD	Head	Set to one for head 1. Set to zero for head 0.
SRT	Step Rate Time	1 to 16 msec in 1msec increments (0hex = 16msec, 1hex = 15msec . . . Ehex = 2msec, Fhex = 1msec. Step rates apply to both drives.
HUT	Head Unload Time	16 to 240msec in 16msec increments.
HLT	Head Load Time	2 to 254msec in 2msec increments.
ND	Non-DMA Mode	Set to one for non-DMA mode.

SUPPORT OF 1.2MB AND 360KB DRIVES

The WD1002-WA2 supports 1.2MB and 360kB drives. Diskettes written on 1.2MB drives with the 360kB density may not be readable on 360kB drives due to a difference in track widths. High capacity drives (1.2MB) require special media to support a recording density of 9646 bits per inch. This special media requires much higher write currents than 360kB drives can produce. Thus, the special media is incompatible with the high capacity drives.

High capacity drives rotate at 360 RPM instead of 300 RPM. A new data transfer rate of 300kbs is used to enable the Host system to read diskettes written on 360kB media. This means that a diskette recorded at 250kbs on the 300 RPM drives reads at a 300kbs rate in the 360 RPM drives.

Recorded track width is determined by the read / write head. The 1.2MB drives write tracks at a 0.16mm (0.00063 inch) width instead of the 0.33mm (0.0130inch) track width for 360kB drives. This can cause some incompatibilities when exchanging media written on the high density drive at the low density rate. This type of interchange is best supported by addition of a 360kB drive to the Host system. Floppy write precompensation is 125 nsec at all transfer rates over all tracks. Floppy write precompensation cannot be disabled or programmed.

Other features for the high capacity drives include 3msec track to track access time vs. 6 msec and a motor start time of 750msec vs. 250msec. The WD1002-WA2 supports only two drives. Data transfers are performed over the DMA channel.

INSTALLATION

This section briefly describes the installation of the WD1002-WA2 board in IBM PC-AT compatible computers.

1. Ensure that system power is off.
2. Insert the WD1002-WA2 board into the computer chassis and connect the drive cables. (J1 = floppy drives 1 and 2 cable, J5 = Winchester control cable, J4 = Winchester drive 1 cable, J3 = Winchester drive 2 cable)

The WD1002-WA2 board is configured for IBM PC-AT compatible computers. Jumper plugs are installed at E1 / E6 and E7 / E8. Figure 5 illustrates the WD1002-WA2 jumper locations. The following jumper options are available:

Standard:	E2-E3	Selects primary addresses 3F2, 3F4 / 3F7 hex for the floppy disk drives.
	E5-E6	Selects primary addresses 1F0 / 1F7 hex for the Winchester disk drives
Jumpered:	E1-E2	Selects secondary addresses 372, 374 / 377 hex for the floppy disk drives
	E4-E5	Selects secondary addresses 170 / 177 hex for the Winchester disk drives
Standard:	E7-E8	Jumper installed. Must be left jumpered at all times.

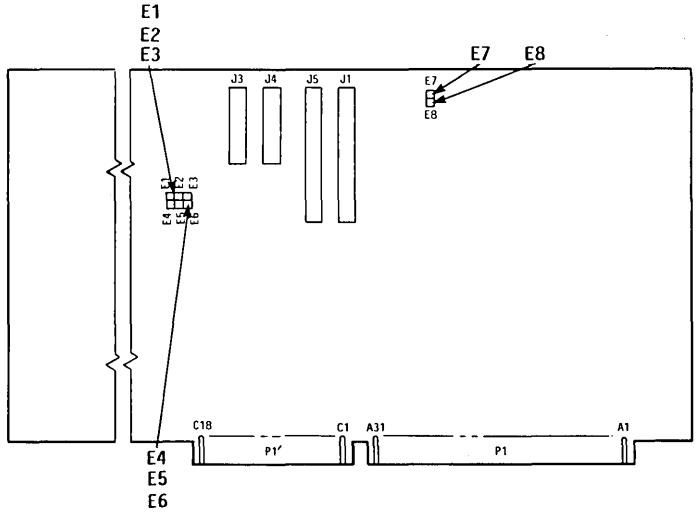


FIGURE 5. WD1002-WA2 Jumper Locations

SPECIFICATIONS

	Hard Disk	Floppy Disk
Encoding Method:	MFM	FM and MFM
Data Rate:	5Mbs	125kbs, 250kbs, 300kbs, 500kbs
Format:	IBM XT compatible	IBM PC-XT compatible
Sectoring:	Soft, 512 byte by 17 per track (Numbered 1 through 17)	Soft, up to 15 by 512 byte sectors per track
Cylinders:	1024	77 max
Heads:	16 max	2 max
Drives:	2	2
Soft Error Rate:	1 in 10E10 bits read	1 in 10E09 bits read
Head Error Rate:	1 in 10E12 bits read	1 in 10E12 bits read
Seek Error Rate:	1 in 10E6 seeks	1 in 10E6 seeks
Precompensation:	+ / - 12 nsec, single-level MFM	+ / - 125 nsec write pre-compensation for all data rates
Interleave Factor:	2 to 1 min	
CRC Polynomial:	x^16 + x^12 + x^5 + 1 \	
ECC Polynomial:	x^32 + x^28 + x^26 + x^19 + x^17 + x^10 + x^6 + x^2 + 1	
ECC Polynomial Reciprocal:	x^32 + x^30 + x^26 + x^22 + x^15 + x^13 + x^6 + x^4 + 1	
ID Field CRC Polynomial:		x^16 + x^12 + x^05 + 1
Data Field CRC Polynomial:		x^16 + x^12 + x^05 + 1
DATA SEPARATOR:		
Type:	WD10C20 self-adjusting VCO	Analog with dual R-C VCO
Features:	reference clock, o phase startup, read pulse extension, DRUN generation write precompensation	single adjustment for each VCO, automatic of adjustment
Acquisition Time:	Less than 8 bytes	Less than 8 byte times
Capture Range:	+ / -3% min	+ / -8.5% min
Phase Error:		+ / -10 deg
POWER:		
Logic Supply:	+5V + / -5%, 2.5 A max	
Supply Ripple:	+ / -100mV, p-p	
Analog Supply 1:	+12V + / -10%, 0.150 A max	
Supply Ripple:	+ / -100 mV, p-p	
Analog Supply 2:	-12V + / -10%, 0.01 A max	
Supply Ripple:	+ / -100 mV, p-p	
ENVIRONMENTAL:		
Temperature		
Operating Non-operating	0°C to 50°C -40°C to 60°C (32°F to 122°F) (-40°F to 140°F)	
Air Flow	100 LFM min constant unidirectional, measured on a plane 1 / 4 in. equidistant from PCB surface.	

	Hard Disk	Floppy Disk
Humidity		
Operating	8% to 80% non-condensing	
Non-operating	5% to 95% non-condensing	
Altitude		
Operating	0 to 3000 meters (0 to 10000 feet)	
Non-operating	0 to 5000 meters (0 to 16000 feet)	
Vibration		
Operating	6 to 600 Hz at 1.0 G	
PHYSICAL:		
Length	33.3 centimeters (13.1 inches)	
Width	12.2 centimeters (4.80 inches)	
Height	1.90 centimeters (0.75 inches)	

HOST INTERFACE TIMING

Timing diagrams are shown in Figure 6. the timing values are given in Table 11.

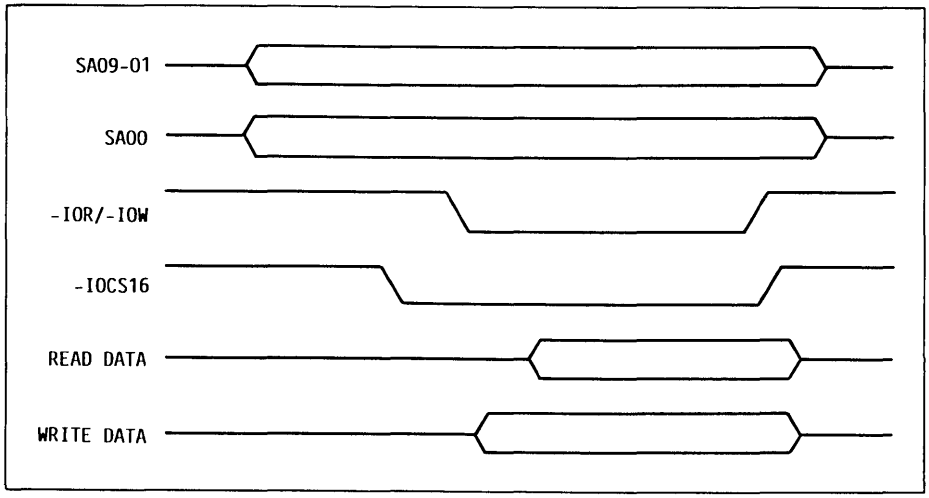


FIGURE 6. I / O CHANNEL TIMING

TABLE 11. TIMING

CHARACTERISTIC	TIMING (nsec)	
	min	max
-IOCS16 from SA09-01		93
-IOCS16 from SA00		73
+IOCS16 from +IOR / +IOW		93
SD15-00 from -IOR(16 bit I / O)		132
SD07-00 from -IOR (8 bit I / O)		498
SD15-00 to +IOW (16 bit I / O)	71	
6D07-00 to +IOW (8 bit I / O)	491	
+IOW to SD15-00 HIZ (16 bit I / O)	54	
+IOW to SD07-00 HIZ (8 bit I / O)	46	
-IOR / -IOW Pulse Width (16 bit I / O)	160	
-IOR / -IOW Pulse Width (8 bit I / O)	540	
+IOR / +IOW to -IOR / -IOW	375	
ADDR HOLD from +IOR / +IOW	47	
SA09-01 to -IOR / -IOW	97	

WD1003-SCS Winchester Disk Controller

FEATURES

- SCSI COMPATIBLE BUS HOST INTERFACE
- CONTROLS UP TO TWO ST506 COMPATIBLE DRIVES
- ALLOWS OVERLAPPED SEEKS
- UP TO 16 HEADS AND 2,048 CYLINDERS
- PROGRAMMABLE SECTOR SIZES (128, 256, 512, AND 1024 BYTES PER SECTOR)
- PROGRAMMABLE STEPPING RATES (3 MSEC/STEP MINIMUM)
- PROGRAMMABLE GAP SIZES
- USER-SELECTABLE DEVICE ADDRESS
- PROGRAMMABLE 1:1 INTERLEAVE
- FULLY SUSTAINED, SEQUENTIAL READ/WRITE OPERATIONS
- SELF-TEST DIAGNOSTICS
- 32-BIT ECC FOR WINCHESTER DATA ERROR DETECTION AND CORRECTION
- COMMAND QUEUING
- LOGICAL UNIT ADDRESSING
- SCSI BUS PARITY OPTION
- FULL HARDWARE COMPLIANCE WITH ANSI SCSI X3T9.2 SPECIFICATIONS
- SUPPORTS DISCONNECT/RECONNECT OPERATIONS
- OPTIONALLY SUPPORTS RESELECTION TIME-OUT
- SUPPORTS ALL STANDARD AND EXTENDED COMMANDS, AND WESTERN DIGITAL'S UNIQUE COMMANDS
- SINGLE-BYTE MESSAGES
- SENSE AND EXTENDED-SENSE CAPABILITY
- RESERVATONS SUPPORTED TO LOGICAL UNIT NUMBER LEVEL
- SECTOR LEVEL BAD BLOCK MAPPING CAPABILITY

DOCUMENT SCOPE

This document is intended to provide the reader with an overview of the WD1003-SCS. For a detailed understanding it will be necessary to refer to the following documents:

- WD1003-SCS Winchester Disk Controller OEM Manual Doc. 79-000025
- SCSI Specification ANSI X3T9.2 August 1984
- ST-506 Winchester Disk Controller
  ST506 S.M.
  Seagate Technology,
  Scotts Valley, Cal.
- ST-506 Electrical Interface Specification
  Seagate Technology,
  Scotts Valley, Cal.
- WD2010-05 Winchester Controller Data Sheet
- WD10C20 Self-Adjusting Data Separator Data Sheet

DESCRIPTION

The WD1003-SCS is a single-board Winchester Disk Controller designed to support up to two ST506 compatible disk drives and to interface to the Small Computer System Interface (SCSI) bus. Bus operation is in compliance with the ANSI X3T9.2 SCSI Specifications.

Commands directed to the drives are executed by the WD1003-SCS and all communications and data transfers to and from the Host take place via the SCSI bus in accordance with SCSI protocol.

The WD1003-SCS functions only as a Target device in the SCSI environment. Because the WD1003-SCS supports disconnect/reconnect operations, full arbitration capability is provided. In addition, the WD1003-SCS Controller board supports one-to-one disk interleave, i.e., fully sustained operations on sequential read access.

The WD1003-SCS is based on a proprietary chip set consisting of the WD2010-05, WD11C00-19 and WD10C20 LSI devices, designed specifically for Winchester/SCSI interface. Extensive error detection and correction, as well as data recovery techniques for disk errors, are incorporated within the controller's design. This circuitry resides in the WD2010-05. The WD11C00-19 is used to control all communications and data transfer.

ARCHITECTURE

The WD1003-SCS architecture allows an optimum amount of design functions to reside within the board. This is accomplished by creating a unified internal bus structure, whereby all major LSI devices share the same buses.

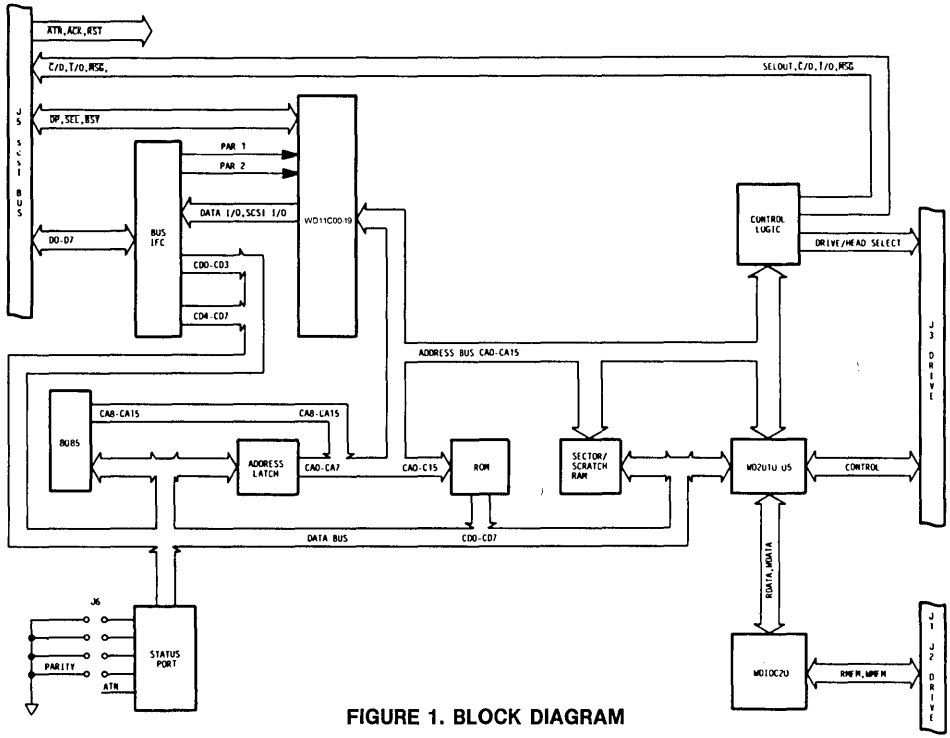


FIGURE 1. BLOCK DIAGRAM

As illustrated in Figure 1, the WD1003-SCS contains four major VLSI devices:

- 8085 microprocessor
- WD2010-05 Winchester Controller
- WD10C20 Self-Adjusting Data Separator
- WD11C00-19 SCSI Protocol Support Device

Control Processor

The Control Processor is an 8085 microprocessor used for the main board control, and is supported by a 2764 (8K X 8) EPROM and a (2K X 8) 2016 static RAM device. The WD1003-SCS Controller's unique architecture facilitates two major functions:

- Support of the SCSI bus application
- 1:1 interleave capability

WD2010-05 Winchester Disk Controller

The primary function of the WD2010-05 is to control data transfer between the disk and the Sector Buffer after the on-board control processor has positioned the selected head over the desired track. The WD2010-05 receives the parameters and commands from the control processor via the CD0 through CD7 bus.

In addition, built-in Error Checking and Correction (ECC) capability in the WD2010-05 enables error detection and correction on all data transfers from the disk. A set of check bits are calculated and appended to the data field when data is written to the disk.

WD10C20 Self-Adjusting Data Separator

The WD10C20 is an LSI device implemented in the 3-micron, high-speed CMOS as a read/write channel. It performs all sensitive read/write signal operations between the Winchester Disk Controller and data drivers and receivers. The device performs both phase-locked loop data synchronization on read data from the drive and conditioning write data to the drive.

WD11C00-19 SCSI Protocol Support Device

The WD11C00-19 is a 40-pin LSI device designed to provide four major support functions:

- Address generation
- Data Transfer (read/write) control
- Arbitration
- Parity checker/generator

All SCSI commands are read, format converted, and then issued to the WD2010-05 for execution.

SPECIFICATIONS

HOST INTERFACE

Type	SCSI
Cable length	20 ft. (6 m) max.
Termination all signals	Socketed 220/330 ohm resistor pack 220 ohms to +5 Volts, 330 ohms to ground
Addressing	Jumper selectable (0 through 7) Default = 0

DRIVE INTERFACE

Encoding method	MFM
Cylinders per drive	Programmable up to 2048
Bytes per sector	Programmable (128, 256, 512, 1024)
Sectors per track	Programmable
Heads per cylinder	Programmable up to 16
Drives	2
Stepping rates/algorithm	Programmable (3 usec/step min.)
Data transfer rate	5 Mbps
Write precompensation	12 nsec
Sectoring	Soft
CRC polynomial	$X^{16}+X^{12}+X^{5}+1$
ECC polynomial	$X^{32}+X^{28}+X^{26}+X^{19}+X^{17}+X^{10}+X^{6}+X^{2}+1$
Cable length:	
Control (daisy-chained)	10 ft. (3 m) max.
Data (radially connected)	10 ft. (3 m) max.
Termination:	all signals 220 ohms to +5 Volts, 330 ohms to ground
Control	on last drive in chain
Data	on WD1003-SCS

DATA SEPARATOR

The operational parameter limits of the Data Separator circuitry on the WD1003-SCS provided here are related only to ST506 Winchester disk operations. For the WD1003-SCS to function properly, the hard disk drive mechanism must perform within the following specifications:

Drive margin	±16 nsec min
Drive Asymmetry	30 nsec. measured over 5 Mhz RAWMFM periods of 185 nsec, 215 nsec, 185 nsec.

ELECTRICAL

Voltage and Current	+5 Vdc±5% @ 1.5 amps nominal 2 amps max +12 Vdc±10% @ 0.25 amps nominal

SCSI electrical description

When measured at the SCSI bus device connection, each signal driven by an SCSI device has the following output characteristics:

Signal assertion = 0 to 0.5 Vdc
Minimum driver output capability = 48mA(sinking) @ 0.5 Vdc

Measured at the connector, each signal has the following input characteristics:

Signal Asserted	0 to 0.8 Vdc
Maximum total input load	-0.4 mA @ 0.4 Vdc
Signal de-asserted	2.0 to 5.25 Vdc

PHYSICAL DIMENSIONS

Length	8 inches (20.3 cm)
Width	5.75 inches (14.6 cm)
Height (including board, components and leads)	0.75 inches (1.9 cm)

ENVIRONMENTAL

Temperature:	
Operating range	0°C (32°F) to 55°C (131°F)
Storage range	-40°C (-40°F) to 60°C (140°F)
Relative Humidity	
Operating range	8% to 80% non-condensing
Storage range	5% to 95% non-condensing
Maximum wet bulb	24° C (75° F)
Altitude	
Operating range	0 to 10,000 ft. (3048 m)
Airflow	150 linear ft/min @ 0.25 inches from component surfaces

Corrosion

Connectors, exposed contacts, and conductors are protected to resist corrosion under all conditions of storage and operating life.

INTERFACE ORGANIZATION

The WD1003-SCS is designed to be mounted directly onto a 5.25" Winchester-type hard disk drive. It contains four vertical-header connectors, and one power connector located along the peripheral edges of the board:

- Two Winchester drive data connectors J1, J2
- Winchester drive control connector J3
- Power connector J4
- Host interface connector J5

The WD1003-SCS accommodates up to two Winchester hard disk drives. The control cable is daisy-chained to each of the two drives; and the drive data cables, which carry differential signals, are radially connected. Table 1 defines the WD1003-SCS connectors and a source for the mating connectors on the associated cables.

TABLE 1.

CONNECTOR	INTERFACE FUNCTION	EQUIVALENT MATING CONNECTOR
J1,J2	Drive Data (Radially-connected)	Burndy #FRS20BS
J3	Drive Control (Daisy-chained)	Brundy #FRS34BS
J4	Power	AMP 1-4840424-0
J5	Host Interface (SCSI Bus)	Burndy #FRS50BS

HOST INTERFACE CONNECTOR

The WD1003-SCS interfaces to the Host via J5, a 50-pin vertical header connector mounted on 0.1 inch centers. The cable used should be a flat ribbon or twisted pair cable of not more than 20 feet in length. Cable termination is via 220/330 ohm resistor packs in position Z1 and Z3. Each signal is terminated to +5 volts via 220 ohms and 330 ohms to ground. Table 2 provides the connector pin descriptions and its bus signals.

TABLE 2. HOST INTERFACE CONNECTOR (J5) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O *	FUNCTION
1 thru 17	2 thru 18	DBO thru DB7 and DBP	DATA BUS 0 thru DATA BUS 7 DATA BUS PARITY	I/O	These signals comprise the SCSI tri-state, bi-directional data bus used to transfer commands, status and data. DBO through DB7 are used for Target device selection and arbitration. DBP is odd parity for DBO through DB7 and is not valid during the arbitration process.
19 thru 25	26	GROUND N.C.	Not Connected		
27 thru 30		GROUND			
31	32	ATN	ATTENTION	I	Asserted by the Host to indicate a message is ready for the WD1003-SCS. This message is read by the WD1003-SCS at its convenience by performing a Message Out Phase.
33	34	GROUND			
35	36	BSY	BUSY	I/O	Indicates to the Host that the SCSI bus is busy executing a command and is unable to accept another. When asserted, BSY acknowledges receipt of SEL and its own address. De-asserted indicates the transfer is completed.
37	38	ACK	ACKNOWLEDGE	I	Acknowledgement for a REQ/ACK data transfer handshake, acknowledges to the WD1003-SCS that the Host has accepted the byte for data transfer.
39	40	RST	RESET	I	When asserted at least 25 usec, RST places the WD1003-SCS into its initial power-up state.
41	42	MSG	MESSAGE	O	Asserted during the Message Byte Transfer Phase. Used with I/O and C/D to indicate the type of transfer.
43	44	SEL	SELECT	I/O	Used by the Host to select the WD1003-SCS, or by the WD1003-SCS to reselect the Host. When asserted, gives control of the bus to the DBO through DB7 address selected by the J6 jumper.

TABLE 2. HOST INTERFACE CONNECTOR (J5) PIN DESCRIPTION (cont.)

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O *	FUNCTION
45	46	C/D	CONTROL/ DATA	O	C/D along with I/O and MSG indicates to the Host whether control or data is on the bus. C/D - 0 = Control - 1 = Data Control is defined as a: command, status, or message.
47	48	REQ	REQUEST	O	A request for a REQ/ACK data transfer handshake. Indicates to the Host that the WD1003-SCS is ready for data transfer.
49	50	I/O	INPUT/ OUTPUT	O	Indicates direction of transfer between the Host and the WD1003-SCS. I/O - 0 = Input to the Host - 1 = Output from the Host

* The I/O column is in relation to the WD1003-SCS and not the Host.

WINCHESTER DRIVE CONTROL CONNECTOR

The WD1003-SCS supports the Seagate Technology ST506 drive control protocol. The control connector is a 34-pin vertical header mounted on a 0.1 inch center. Control signals are common to both drives and are daisy-chained on a single connector J3. The cable used should be a flat ribbon or twisted-pair not more than 10 feet in length.

The control signals are to be terminated at the last drive in the daisy-chain with a 220/330 ohm resistor pack. Each control signal is connected to +5 volts with the 220 ohm resistor and to ground with 330 ohms.

The drive control connector J3 pin description is provided in Table 3.

TABLE 3. DRIVE CONTROL (J3) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O *	FUNCTION
1	2	HS3 or RWC	HEAD SELECT 3 or REDUCE WRITE CURRENT	O	HS3 is one of four Head Select signals decoded by the drive to select one of 16 R/W heads. RWC is asserted when the cylinder specified by the Inquiry Data Format command is reached. An asserted RWC allows the 8085 to initiate RWC on succeeding cylinders.
3	4	HS2	HEAD SELECT 2	O	One of four Head Select signals decoded by the drive to select one of 16 R/W heads.
5	6	WG	WRITE GATE	O	WG is asserted when valid data is to be written on the disk. WD1003-SCS de-asserts this signal when a WF is detected.
7	8	SC	SEEK COMPLETE	I	SC is asserted by the selected drive when the head has reached the desired cylinder and stabilized.
9	10	TK000	TRACK 000	I	The drive asserts this signal when the R/W heads are positioned over the outermost cylinder, cylinder zero.

TABLE 3. DRIVE CONTROL (J3) PIN DESCRIPTION (cont.)

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
11	12	$\overline{WF}$	$\overline{WRITE\ FAULT}$	I	$\overline{WF}$ is asserted by the selected drive when a write error occurs. The command in progress aborts and no other disk command can be executed while this signal is asserted.
13	14	$\overline{HSO}$	$\overline{HEAD\ SELECT\ 0}$	O	One of four Head Select signals decoded by the drive to select one of 16 R/W heads.
15	16	N.C.	Not Connected		
17	18	$\overline{HS1}$	$\overline{HEAD\ SELECT\ 1}$	O	One of four Head Select signals decoded by the drive to select one of 16 R/W heads.
19	20	$\overline{INDEX}$	$\overline{INDEX\ PULSE}$	I	Indicates the start of a track and is used both as a synchronization point during formatting and a time-out mechanism for retries. This signal pulses once for each disk revolution.
21	22	$\overline{DRDY}$	$\overline{DRIVE\ READY}$	I	Informs the WD1003-SCS that the drive motor is up to speed.
23	24	$\overline{STEP}$	$\overline{STEP\ PULSE}$	O	$\overline{STEP}$, together with $\overline{DIRIN}$, positions the heads to the desired cylinder. $\overline{STEP}$ pulses once for each cylinder. $\overline{DIRIN}$ determines the direction.
25	26	$\overline{DSEL\ 0}$	$\overline{DRIVE\ SELECT\ 0}$	O	$\overline{DSEL0}$ is used to select drive 0.
27	28	$\overline{DSEL\ 1}$	$\overline{DRIVE\ SELECT\ 1}$	O	$\overline{DSEL\ 1}$ is used to select drive 1.
29	30	N.C.	Not Connected		
31	32	N.C.	Not Connected		
33	34	$\overline{DIRIN}$	$\overline{DIRECTION\ IN}$	O	$\overline{DIRIN}$ determines the direction the R/W heads take when the Step signal is pulsed. 0 = in, 1 = out.

WINCHESTER DRIVE DATA CONNECTOR

The data is differential in nature and must be radially connected to each drive with its own cable, drive 0 to J1 and drive 1 to J2. It should be a flat ribbon cable, or twisted pair, not more than 10 ft. in length. The connecter is a 20-pin vertical header on 0.1 inch center.

TABLE 4. DRIVE DATA CONNECTORS - J2, J3

SIG. GND.	SIG. PIN	I/O	SIGNAL NAME
	1		NC
2			GND
	3		NC
4			GND
	5		NC
6			GND
	7		NC
8			GND
	9		NC
	10		NC
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	-MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	-MFM Read Data
19			GND
20			GND

POWER CONNECTOR

A 4-pin, neoprene-type connector (J4) is provided for power input to the WD1003-SCS board.

PIN	VOLTAGE
1	+ 12V
2	GND.
3	GND.
4	+ 5V

COMMAND DESCRIPTION

The WD1003-SCS supports 22 commands. These commands are separated into three Groups: 15 standard commands in group 0, 4 extended commands in group 1, and 3 diagnostic commands in group 7. A summary of these commands, along with their Command Description Block is illustrated in the tables that follow.

TABLE 5. SUMMARY OF GROUP 0 AND 7 COMMANDS

COMMAND	OP CODE	LUN	LBA / FD,CL,DLF	INT	NOB/RSB/ NB / PLL	ERTY
TEST DRIVE READY	00	V	n	n	n	n
REZERO UNIT	01	V	n	n	n	n
REQUEST SENSE	03	V	n	n	V(RSB)	n
FORMAT UNIT	04	V	V(FD,CL,DLF)	V	n	n
REASSIGN BLOCKS	07	V	n	n	n	n
READ	08	V	V(LBA)	n	V(NOB)	V
WRITE	0A	V	V(LBA)	n	V(NOB)	V
SEEK	0B	V	V(LBA)	n	n	n
INQUIRY DATA FORMAT	12		V(LBA)	n	V(NB)	n
MODE SELECT	15	V	n	n	V(PLL)	n
RESERVE UNIT	16	V	n	n	n	n
RELEASE UNIT	17	V	n	n	n	n
MODE SENSE	1A	V	n	n	V(PLL)	n
RECEIVE DIAGNOSTIC	1C	V	n	n	n	n
SEND DIAGNOSTIC	1D	V	n	n	n	n
READ LONG	E5	V	V(LBA)	n	V(NOB)	V
WRITE LONG	E6	V	V(LBA)	n	V(NOB)	V
READ DIF	E7	V	n	n	n	n

LEGEND:

V Must be a valid parameter.
n Not used (should be 0 for future compatibility).
LUN Logical Unit Number of drives. 0 or 1 for WD1003-SCS.
LBA Logical Block Address.
FD Format Data bit.
CL Complete List bit.
DLF Defect List Format bits.
INT Interleave factor.
NOB Number Of Blocks.
RSB Requested Sense Bytes.
NB Number of Bytes.
PLL Parameter Length List.
ERTY Error Retry bit.

GROUP 0 AND 7 COMMAND DESCRIPTION BLOCK

The Command Description Block format used by the 15 Group 0 and 3 Group 7 commands is provided in Figure 2.

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	OPERATION CODE							
1	LUN			LOGICAL BLOCK ADDRESS (MSB) OR FORMAT DATA/COMPLETE LIST/DEFECT LIST FORMAT				
2	LOGICAL BLOCK ADDRESS							
3	LOGICAL BLOCK ADDRESS (LSB) OR INTERLEAVE (MSB)							
4	NUMBER OF BLOCKS, REQUESTED SENSE BYTES, NUMBER OF BYTES, INTERLEAVE (LSB), OR PARAMETER LIST LENGTH							
5	ERTY	0	0	0	0	0	0	0

FIGURE 2. GROUP 0 AND 7 COMMAND DESCRIPTION BLOCK

Operation Code

Bits 7-5 designates that the command is used in a Group 0 or 7 operation.

Bits 4-0 identify the function of a command, e.g., Read or Write, to be performed within Command Group 0 or 7.

LUN

Specifies the Logical Unit Number of the attached drive. Must be 0 or 1.

Logical Block Address

Specifies the Logical Block Address where an operation is to begin.

Format Data, Complete List, Defect List Format

Used in conjunction with the Reassign Blocks and Format Commands:
- Format Data. Bit 4 of byte 1.
- Complete List. Bit 3 of byte 1.
- Defect List. Bits 2, 1, and 0 of byte 1.

Interleave (MSB) and (LSB)

The interleave factor is used by format commands. The disk may be formatted at a 1:1 ratio. And the maximum interleave is equal to the sectors-per-track minus one.

Byte 3 or 4 can be any interleave number from 0 through 28. If an interleave factor of 0 is used, the WD1003-SCS uses a default interleave of 2.

Number of Blocks

Indicates the number of contiguous logical data blocks to be transferred by an operation. When zero, 256 blocks are transferred. Any other value indicates the number of blocks to be transferred.

Requested Sense Bytes

The number of bytes indicates the length of data allocated by the Host for the returned sense information. The count also determines the format of the returned sense data. Sense data can be returned in one of two supported sense byte formats: (1) standard Non-Extended Sense Byte format, and (2) Extended Sense Byte format. A requested sense byte count of zero results in a data transfer of four. The requested count, but never more than eight sense bytes, are sent on all other requested values.

Parameter List Length

The only valid length for proper operation is 30 (decimal). Zero represents a No-Operation condition.

Number of Bytes

Indicates the data length allocated by the Host for the Returned Sense data.

ERTY

Disk error retry bit. When set, indicates a request for a retry operation. (Used if retries are supported by a specific command.)

TABLE 6. SUMMARY OF GROUP 1 COMMANDS

COMMAND	OP CODE	LUN	LBA	NOB	PMI	ERTY
READ CAPACITY	25	V	V	n	V	n
READ EXTENDED	28	V	V	V	n	V
WRITE EXTENDED	2A	V	V	V	n	V
SEEK EXTENDED	2B	V	V	n	n	V

LEGEND:

V	Must be a valid parameter.	NOB	Number Of Blocks.
n	Not used (should be 0 for future compatibility).	PMI	Partial Medium Indicator bit.
LUN	Logical Unit Number of drives 0 and 1.	ERTY	Error Retry bit.
LBA	Logical Block Address.		

GROUP 1 COMMAND DESCRIPTION BLOCK

The Command Description Block format used by the four Group 1 commands is provided in Figure 3.

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	OPERATION CODE							
1	LUN			0	0	0	0	0
2	LOGICAL BLOCK ADDRESS (MSB)							
3	LOGICAL BLOCK ADDRESS							
4	LOGICAL BLOCK ADDRESS							
5	LOGICAL BLOCK ADDRESS (LSB)							
6	0	0	0	0	0	0	0	0
7	NUMBER OF BLOCKS (MSB)							
8	NUMBER OF BLOCKS (LSB) OR PMI							
9	ERTY	0	0	0	0	0	0	0

FIGURE 3. GROUP 1 COMMAND DESCRIPTION BLOCK FORMAT

Operation Code

Bits 7-5 designates that the command is used in a Group 1 operation.

Bits 4-0 identify the function of a command e.g., Read Extended, Write Extended, or Seek Extended to be performed within Command Group 1.

LUN

Specifies the Logical Unit Number of the attached drive. Must be a 0 or 1.

Logical Block Address

Specifies the Logical Block Address where an operation is to begin.

Number of Blocks

Indicates the number of contiguous logical data blocks to be transferred by an operation. When zero, 256 blocks are to be transferred. Any other value indicates the number of blocks to be transferred.

PMI

Partial Medium Indicator. Bit 0 of byte 8 used in the Read Capacity Command. Setting this bit to:

0 = Controller returns address of the last block on the LUN device.

1 = Controller returns the last block prior to a cylinder boundary that follows the Block Address given by the Host. For example, Block Address 0 results in the controller returning Block Address 67 on a device with four heads and is formatted with 17 sectors per track (512 bytes per sector).

RETRY

Disk error retry bit. When set, indicates an error condition and a request for a retry operation. (Used if retries are supported by a specific command.)

TABLE 7. POSSIBLE COMMAND ERROR CODES

COMMAND	ERROR CODE
TEST DRIVE READY	00,03,04,1C,22
REZERO UNIT	00,03,04,06,0A,1C,21,22
REQUEST SENSE	NONE
FORMAT UNIT	00,03,04,1A,1B,1C,1D,1E,22
REASSIGN BLOCKS	00,03,04,1A,1B,1C,1D,1E,22
READ	00,03,04,06,0A,10,11,13,18,1C,21,22,80
WRITE	00,03,04,06,0A,10,19,1C,21,22,80
SEEK	00,03,04,0A,1C,21,22
INQUIRY DATA	00,22
FORMAT	
MODE SELECT	00,20,21,22
RESERVE UNIT	00,03,04,22
RELEASE UNIT	00,03,04,22
MODE SENSE	00,20,21,22
RECEIVE DIAGNOSTIC	00,1C,22,30,31,32,33,34,37
SEND DIAGNOSTIC	00,1C,22,30,31,32,33,34,37
READ CAPACITY	00,20,21,22
READ EXTENDED	00,03,04,06,0A,10,11,13,18,19,1C,21,22,80
WRITE EXTENDED	00,03,04,06,0A,10,18,19,1C,21,22,80
SEEK EXTENDED	00,03,04,06,0A,1C,21,22,80
READ LONG	00,03,04,06,0A,10,13,19,1C,21,22,80
WRITE LONG	00,03,04,06,0A,10,13,19,1C,21,22,80
READ DIF	1C,22

TABLE 8. ERROR CODE DESCRIPTION

ERROR CODE* (HEX)	ERROR NAME	TYPE OF ERROR	DESCRIPTION
00	No Sense		Indicates that there is no specific Sense Key information to report for a designated LUN. No error is detected and the command is completed successfully.
03	Write Fault	Disk Drive	Indicates write current had not occurred when $\overline{WG}$ is de-asserted, or an $\overline{SC}$ is not asserted and a drive is selected while $\overline{WG}$ is asserted.
04	Drive Not Ready	Disk Drive	Indicates the LUN address cannot be accessed. The selected drive's $\overline{DRDY}$ is de-asserted. The motor of the selected drive is not up to speed.
06	Track 0 Not Found	Disk Drive	This code is returned by the Rezero Unit Command. Indicates $\overline{TK000}$ from the selected drive was not asserted after the maximum number of steps (up to 1024) toward cylinder 0.
0A	Disk Full	Operational	Insufficient medium (hard disk) capacity. Indicates the specified address reached the file device's given range.
10	ID Error	Disk Drive	An ID CRC error.
11	Uncorrectable Data Error	Disk Drive	Indicates an error in the data field is beyond the ECC's correction capability. Data for the block in error is not sent to the Host.
13	Data Address Mark Not Found	Disk Drive	Indicates header of a selected block is found, but its Data Address Mark is not detected.
18	Correctable Data Error	Disk Drive	Indicates an error in the data field is within the ECC's correction capability and is corrected. The data block is sent to the Host. This status serves as a warning to the Host that a marginal condition may exist.
19	Bad Block	Operational	Indicates a formatted bad block is encountered.
1A	Bad DIF	Operational or Disk Drive	The Drive Information File cannot be read by the Reassign Blocks or Format command with the Add To DIF option selected.
1B	Cannot Read Alternate Track Information	Media	On all attempts to read the alternate address from the bad track a read error occurred.
1C	Disk Not Formatted Correctly	Operational	This error can only occur on the first disk access after an initial power up or a reset. Sector zero track zero was read and found not to contain a Drive Information File.
1D	Address Of The Defective Block Too Large	Operational	Defective block address exceeds the size of the disk.
1E	No Alternates Left	Operational	1. No alternate tracks were allocated and format has been requested with Bad Track Mapping option only. 2. Not enough alternate tracks allocated to accommodate the number of bad blocks specified in the Drive Information List. 3. No unused alternate tracks available for use during a Reassign Blocks command.

TABLE 8. ERROR CODE DESCRIPTION (cont.)

ERROR CODE* (HEX)	ERROR NAME	TYPE OF ERROR	DESCRIPTION
20	Bad Command	Command	Indicates an invalid Command Group, OP. Code,LUN, Logic Block Address, ID, Interleave, Block Length, or Partial Medium Indicator.
21	Illegal Block Address	Operational	Not a valid address for a Logical Block or Parameter.
22	Unit Attention		Occurs only once after reset. Indicates the removable medium (hard disk) may have been changed or the WD1003-SCS has been reset (by a Bus Device Reset message or a "hard" Reset condition) since the last command was issued to the LUN. When the error condition is detected, the requested command is not performed. The Unit Attention Sense Key is reported to all Initiators that subsequently issue a command to the LUN. This Sense Key is cleared for the next command from the same Initiator.
30	Bad ROM	Diagnostics	Indicates the ROM checksum does not match the calculated checksum.
31	Bad RAM	Diagnostics	Indicates the external RAM failed.
32	Bad Winchester	Diagnostics	Indicates the WD2010-05 Disk Controller failed.
33	Bad Address Generation	Diagnostics	Address generation has failed. Indicates a WD1100-19 error.
34	Bad Instruction Set	Diagnostics	Indicates an invalid instruction set from the 8085 microprocessor.
36	Good Pass Of Diagnostics	Diagnostics	Diagnostics completed successfully.
37	Bad Bus	Diagnostics	Indicates an internal bus hardware error.
+80	Valid Address		A valid address bit, indicating the Block Address fields contain valid information.

*Error codes returned reflect only one error although multiple errors may exist. In this case, the error considered to most severe will be reported.

+80 is ORed with the error code: e.g. 37 = B7

WESTERN DIGITAL
CORPORATION

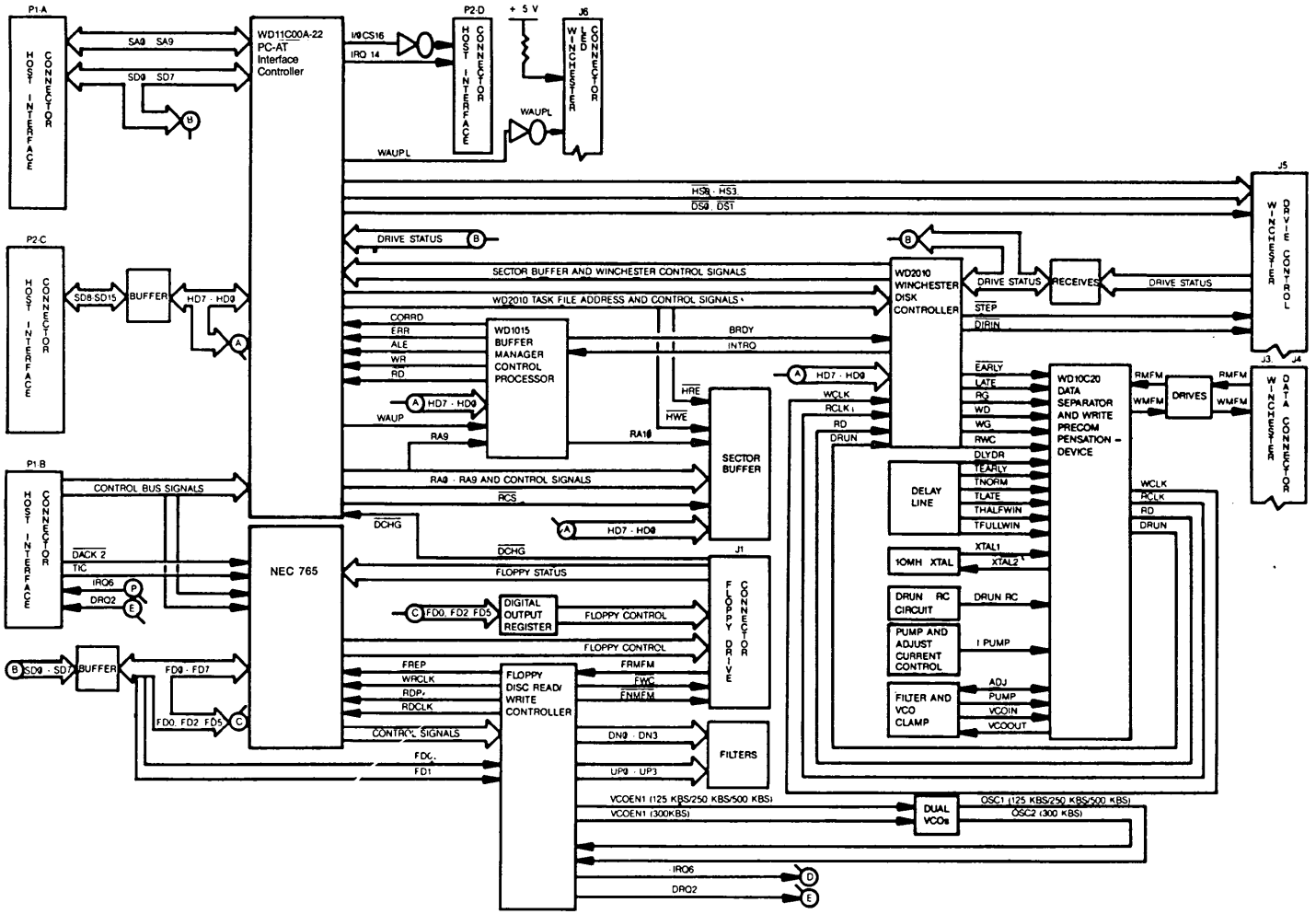
WD1003-WA2 Winchester/Floppy Disk Controller
ADVANCED INFORMATION

FEATURES

- AT COMPATIBLE WINCHESTER AND FLOPPY CONTROLLER
- CONTROLS UP TO TWO WINCHESTER DRIVES (ST506/ST412, 16 R/W HEADS EACH, 2048 CYLINDERS)
- CONTROLS UP TO TWO FLOPPY DISK DRIVES:
  - DOUBLE-SIDED
  - DOUBLE DENSITY (360kB, 250kbs, MFM)
  - QUAD DENSITY (1.2MB, 500kbs, MFM)
  - FOUR DATA RATES (500kbs, 300kbs, 250kbs, and 125kbs)
  - SUPPORTS 360 AND 300 RPM SPINDLE SPEED
- WD2010A-05 WINCHESTER DISK CONTROLLER
- 8-BIT, BI-DIRECTIONAL BUS HOST INTERFACE FOR CONTROL AND STATUS TRANSFERS
- HIGH-SPEED, 16-BIT PIO DATA TRANSFERS
- 32-BIT ECC OR WINCHESTER ERROR DETECTION AND CORRECTION, CRC FOR ID FIELDS
- DIAGNOSTIC MODE FOR ERROR CHECKING
- WRITE PRECOMPENSATION LOGIC
- WD10C20 DATA SEPARATOR AND WRITE PRECOMPENSATION DEVICE
- WD11C00A-22 (RMAC) AND WD16C92 FLOPPY DISK READ/WRITE CONTROLLER (FRWC) REDUCE POWER CONSUMPTION AND COMPONENT COUNT
- ALLOWS CONCURRENT OPERATION OF ONE FLOPPY AND ONE WINCHESTER DRIVE

DESCRIPTION

The WD1003-WA2 is a cost reduced version of the WD1002-WA2. The WD1003-WA2 is an IBM Personnal Computer AT bus compatible Winchester/Floppy disk controller designed to interface up to two Winchester and up to two floppy disk drives. The board permits the concurrent operation of one floppy and one fixed disk drive. The Winchester drive interface is compatible to the Seagate Technology ST506 standard interface for 5Mbs hard disk drives. The floppy disk drive interface supports 1.2MB, 360 RPM drives as well as 360kB (SA450) drives. The WD1003-WA2 includes all necessary receivers and drivers to allow direct connection to the drive(s).



WD1003-WA2 BLOCK DIAGRAM

WESTERN DIGITAL
CORPORATION

WD1003-WAH Winchester Disk Controller
ADVANCED INFORMATION

FEATURES

- AT COMPATIBLE WINCHESTER CONTROLLER
- CONTROLS UP TO TWO WINCHESTER DRIVES (ST506 / ST412, 16 R / W HEADS EACH, 2048 CYLINDERS)
- 8-BIT, BI-DIRECTIONAL BUS HOST INTERFACE
- 16-BIT, HIGH SPEED PIO DATA TRANSFERS
- 32-BIT ECC FOR WINCHESTER ERROR DETECTION AND CORRECTION
- MULTIPLE SECTOR READ/WRITE COMMANDS (MAY CROSS HEAD AND CYLINDER BOUNDARIES
- IMPLIED AND BUFFERED SEEK COMMANDS
- READ/WRITE DIAGNOSTIC AND VERIFY COMMANDS
- PROGRAMMABLE FORMAT AND ERROR RECOVERY ALGORITHMS
- WD10C20 DATA SEPARATOR AND WRITE PRECOMPENSATION
- WD2010A-05 WINCHESTER DISK CONTROLLER

DESCRIPTION

The WD1003-WAH is a cost reduced version of the WD1002-WAH. The WD1003-WAH is an IBM Personal Computer AT bus compatible Winchester controller board designed to interface up to two drives. The drive interface is based upon the Seagate Technology ST506. The drives need not be of the same capacity or configuration. All necessary receivers and drivers are included on the board to allow direct connection to the drive(s).

WD1003-WAH BLOCK DIAGRAM

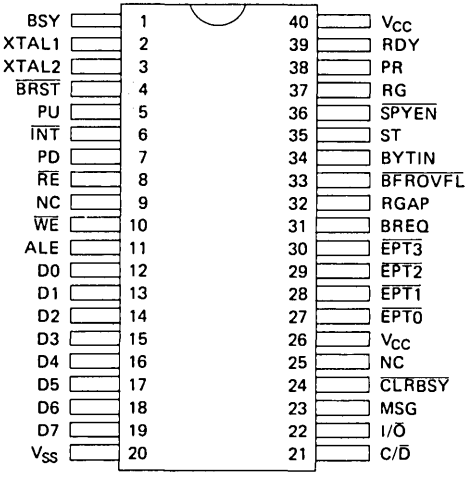
WD2401 Buffer Management Tape Controller

FEATURES

- 40-PIN DIP
- NMOS TECHNOLOGY
- SINGLE +5V POWER SUPPLY
- 6 MHZ CLOCK RATE
- SUPPORTS 1/4" STREAMING TAPE UNITS
- SASI HOST INTERFACE
- CONTROLS TAPE MOTION
- STREAMING TAPE COMMAND TRANSLATION
- SELF TEST DIAGNOSTICS
- AUTOMATIC RETRIES ON ALL ERRORS

DESCRIPTION

The WD2401 Buffer Management Tape Controller (BMTC) is a complete control processor for streaming tape controllers. This device executes all basic functions for 1/4" streaming tape backup of disk images or logical files. WD2401 firmware programs handle all aspects of SASI Host command interpretation, tape motion control, and buffer management of the WD24C02 Read/Write Formatter. Execution of error recovery routines provide complete backup with minimal Host intervention. The error recovery routines attempt a maximum of 16 retries to recover most error conditions.



PIN DESIGNATION

PIN DESCRIPTION

SIG. PIN	SIGNAL MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	BSY	BUSY	I	Indicates start of SASI Command phase.
2	XTAL1	CRYSTAL1	I	External crystal for timing purposes.
3	XTAL2	CRYSTAL2	I	External crystal for timing purposes.
4	$\overline{BRST}$	$\overline{RESET}$	I	Initializes the internal logic of the BMTC. Starts execution of diagnostic TEST routine.
5	PU	PULL UP	I	Tied to external one ohm pull-up resistor.
6	$\overline{INT}$	$\overline{INTERRUPT}$	I	Indicates the WD24C02 has started to read or write a gap.
7	PD	PULL DOWN	I	Tied to external 330 ohm pull-down resistor.
8	$\overline{RE}$	$\overline{READ\ ENABLE}$	O	Asserted to read data from the Host or WD24C02.
9		NOT USED	O	Left open.
10	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	O	Indicates valid data during bus write.
11	ALE	ADDRESS LATCH ENABLE	O	Strobes address into external device. Occurs once each instruction cycle.
12 thru 19	D0 thru D7	DATA 0 thru DATA 7	I/O	8-bit, tri-state, bi-directional bus. D0 is the least significant bit (LSB). D7 is the most significant bit (MSB). Data is written on or read from the bus using $\overline{WE}$ or $\overline{RE}$ strobes, respectively. Also contains the address and data during an external access to or from port devices. ALE, $\overline{RE}$, and $\overline{WE}$ controls the external access.
20	V_{SS}	GROUND		GROUND
21	C/$\overline{D}$	CONTROL/$\overline{DATA}$	O	Indicates whether the current byte on the SASI bus is a control or data byte.
22	I/$\overline{O}$	INPUT/$\overline{OUTPUT}$	O	Indicates the direction of the current byte on the SASI bus.
23	MSG	MESSAGE	O	Indicates a Data Message Out phase on the SASI bus.
24	$\overline{CLRBSY}$	$\overline{CLEAR\ BUSY}$	O	Indicates release of SASI bus.
25	NC	Not Connected		

PIN DESCRIPTION (CONT'D.)

SIG. PIN	SIGNAL MNEMONIC	SIGNAL NAME	I/O	FUNCTION
26	V_{CC}	+5V		+5V power supply.
27	$\overline{EPTO}$	ENABLE PORT 0	O	Strobes output data to an external latch when $\overline{O}$ ($I/\overline{O}$) is asserted. Enables external latch to input data to the WD2401 when I ($I/\overline{O}$) is asserted.
28	$\overline{EPT1}$	ENABLE PORT 1	O	Strobes drive control data from the WD2401 into an external register. Refer to Table 1 for the definitions of these control data bits.
29	$\overline{EPT2}$	ENABLE PORT 2	O	Strobes drive control data from the WD2401 into an external register. Refer to Table 2 for the definitions of these control data bits.
30	$\overline{EPT3}$	ENABLE PORT 3	O	Assertion of this signal enables sending of the tape drive status to the WD2401. Refer to Table 3 for the definitions of these status bits.
31	BREQ	BUS REQUEST	O	Assertion of this signal allows the WD2401 to request use of external bus. The WD2401 controls external bus when RDY is asserted.
32	RGAP	RAW GAP	I	Assertion of this signal indicates the occurance of the gap in the incoming data stream.
33	$\overline{BFROVFL}$	$\overline{BUFFER\ OVERFLOW}$	I	Assertion indicates completion of a transfer of a block of data between the Host and WD24C02.
34	BYTIN	BYTE IN	I	Assertion of this signal indicates the Host port on the tape controller board is ready to transfer a byte.
35	ST	START HOST DATA TRANSFER	O	Asserted for Host data transfers.
36	$\overline{SPYEN}$	$\overline{ENABLE\ SPY\ MODE}$	O	Asserted for spying on the SASI bus. (Currently not implemented.)
37	RG	READ GATE	O	Asserted to switch external data separator from reference to the incoming data bits.
38	PR	PRIME	O	Assertion of this signal initializes the WD24C02 for data transfers to the Host.
39	RDY	READY	I	Assertion of this signal indicates the WD2401 controls external bus.
40	V_{CC}	+5V		+5V power supply.

TABLE 1. DRIVE CONTROL BIT DEFINITIONS ($\overline{EPT1}$)

BIT	FUNCTION
0	Track bit 0 (LSB)
1	Track bit 1
2	Track bit 2
3	Track bit 3 (MSB)
4	Head Current
5	Prime spy mode
6	Spare
7	Spare

NOTE: This device specifies up to 16 tracks (Track bits 0-3)

TABLE 2. DRIVE CONTROL BITS ($\overline{EPT2}$)

BIT	FUNCTION
0	Write enable
1	Erase enable
2	Reverse direction
3	Start tape motion
4	Drive select 0
5	Threshold
6	Spare
7	SASI enable

TABLE 3. TAPE DRIVE STATUS BIT DEFINITIONS ($\overline{EPT3}$)

BIT	FUNCTION
0	Upper tape hole
1	Lower tape hole
2	Drive selected
3	Cartridge inserted
4	Tape write enabled
5	Tachometer pulses
6	Abort command (From Host)
7	No data on tape

ARCHITECTURE

The WD2401 consists of the I/O interface, control logic, 4KB ROM, 256 bytes RAM, clock, and program counter. Figure 1 illustrates the architecture of the WD2401.

Transmission and reception of data, control, and status is the responsibility of the I/O interface.

The control logic receives, decodes, and executes instructions received from the I/O interface or other internal logic.

The 4KB ROM contains firmware programs. These programs enable the control logic to handle all aspects of SASI Host command interpretation, tape motion control, and buffer management of WD24C02.

The 256 bytes of internal RAM serve as a scratch-pad memory for the WD2401.

The 8-bit CPU follows the standard architecture of most popular CPUs.

Timing signals for the WD2401 internal logic are derived from the clock circuitry. The WD24C02 clock requires connection to an external crystal with a fundamental frequency of 6 MHz.

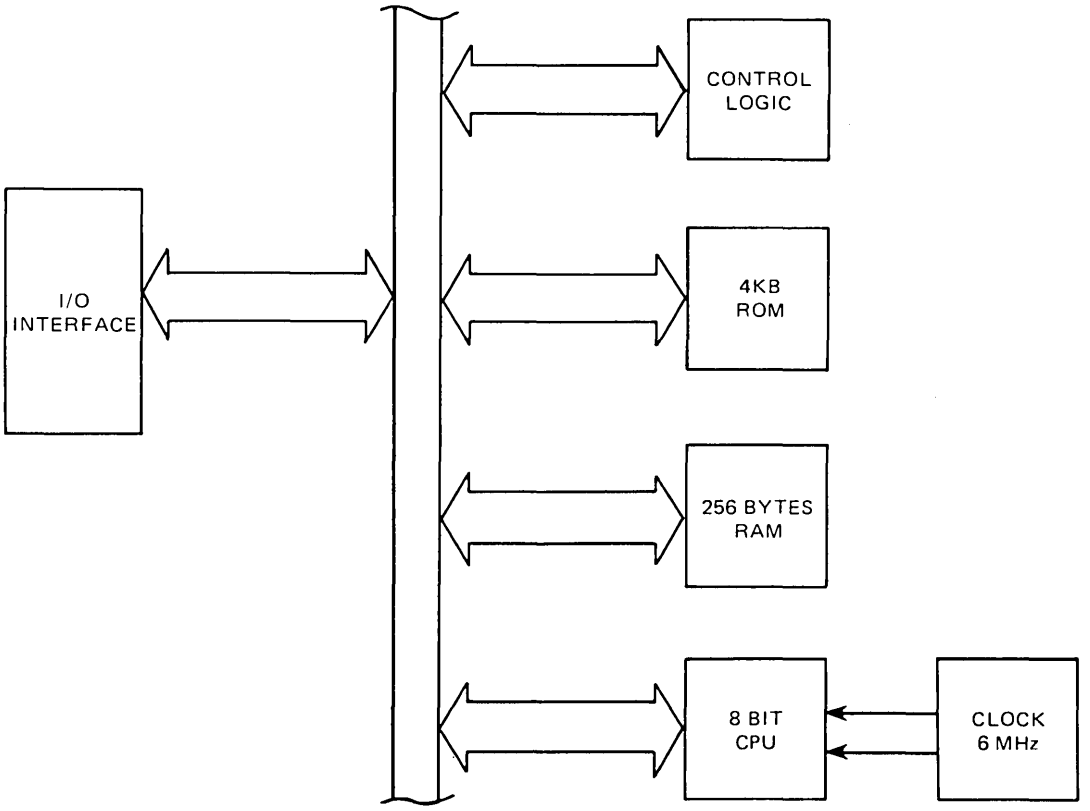


FIGURE 1. WD2401 BUFFER MANAGEMENT TAPE CONTROLLER SIMPLIFIED BLOCK DIAGRAM

WD2401 COMMAND SET

The WD2401 command set implements all the basic functions to backup Winchester disk images or logical files. WD2401 commands control the basic functions of tape positioning, data transfer, and operational modes.

Command protocol follows the SASI standard. Command descriptor blocks (CDB) consist of six bytes and contain the following information:

Byte 0 contains the command group in bits 7 through 5 and the command op code in bits 4 through 0.
Byte 1 contains the tape drive's Logical Unit Number (LUN bits 7 through 5), and the five high order bits of the Tape Block Number (HIGH bits 4 through 0).
HIGH along with Byte 2 (MIDDLE) and Byte 3 (LOW) make up the Tape Block Number used only by the Read Tape Block command.
Byte 4 contains the COUNT field used by the Read File Mark and Write File Mark commands.
Byte 5 contains the option bits.

Figure 2 illustrates the CDB format. Tables 4 and 5 summarizes command parameters and option bits, respectively. Table 6 lists error codes and their definitions.

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0				OPCODE				
1	LUN			HIGH				
2	MIDDLE							
3	LOW							
4	COUNT							
5	OPTION BITS See Table 5							

FIGURE 2. COMMAND DESCRIPTOR BLOCK FORMAT

TABLE 4. COMMAND SUMMARY

COMMAND	COMMAND TYPE	OP CODE	LUN	HIGH	MIDDLE	LOW	COUNT	OPTIONS
REWIND TO BEGINNING OF TAPE	TAPE POSITION	11	D	0	0	0	0	0
READ FILE MARKS	TAPE POSITION	24	D	0	0	0	V	T
ERASE TAPE	TAPE POSITION	26	D	0	0	0	0	0
RETENSION TAPE	TAPE POSITION	27	D	0	0	0	0	0
FIND END OF DATA	TAPE POSITION	28	D	0	0	0	0	0
TEST DRIVE READY	OPERATION MODE	00	D	0	0	0	0	0
READ SENSE BYTES	DATA TRANSFER	03	D	0	0	0	0	C
READ BLOCK BUFFER	DATA TRANSFER	10	0	0	0	0	0	P
WRITE BLOCK BUFFER	DATA TRANSFER	0F	0	0	0	0	0	P
READ TAPE BLOCKS	DATA TRANSFER	21	D	V	V	V	V	R,T,F
WRITE TAPE BLOCKS	DATA TRANSFER	22	D	0	0	0	V	T,U,H
WRITE FILE MARK	DATA TRANSFER	23	D	0	0	0	V	T,H
READ EXTENDED STATUS	DATA TRANSFER	25	D	0	0	0	0	C
BACKUP DISK IMAGE	OPERATION MODE	40	D	0	0	0	0	T,U,H
PERFORM CONTROLLER DIAGNOSTICS	OPERATION MODE	E4	0	0	0	0	0	0
DEFINE TAPE PARAMETERS	OPERATION MODE	0C	D	0	0	0	0	0
EXIT SPY MODE	OPERATION MODE	41	D	0	0	0	0	U

LEGEND

D Target drive number
V Valid parameter
T Threshold
C Clear internal counters
P Page number. External block buffer contains sixteen pages of memory. Each page of memeory is 512 bytes.
R Reposition option
F Flush bit
U Underrun
H High current
O Must be O

TABLE 5. OPTION BITS SUMMARY

COMMAND	BITS							
	7	6	5	4	3	2	1	0
WRITE BLOCK BUFFER	0	0	0	0	P	P	P	P
READ BLOCK BUFFER	0	0	0	0	P	P	P	P
READ TAPE BLOCKS	R	F	T	0	0	0	0	0
READ FILE MARKS	0	0	T	0	0	0	0	0
WRITE TAPE BLOCKS	0	0	T	H	U	0	0	0
WRITE FILE MARKS	0	0	T	H	0	0	0	0
FIND END OF DATA	0	0	T	0	0	0	0	0
READ EXTENDED STATUS	0	0	0	0	0	C	0	0
READ SENSE BYTES	0	0	0	0	0	C	0	0

NOTE: Bits 0 through 7 in byte 5 of command block are set to zero for all other commands.

LEGEND

P Page number. External block buffer contains sixteen pages of memory. Each page of memory is 512 bytes.
R Reposition. 0 = disable. 1 = enable repositioning. Enabling repositioning requires a tape block address in the HIGH, MIDDLE, and LOW bit positions and starts a flush.
F Flush. 1 = flush data blocks in the buffers before reading more blocks. 0 = disable flushing.
T Threshold. 0 = disable. 1 = enables threshold at read head. Eliminates data of questionable quality.
H High current. 0 = disable. 1 = enables increased write current for high coercivity tape, e.g. DC600A.
U Underrun. 0 = stop tape motion on an underrun. 1 = maintain streaming on an underrun.
C Clear internal Read CRC, Write CRC, and Underrun/Overrun counters when set to 1.

TABLE 6. ERROR CODES

HEX CODE	DEFINITION
04	Drive not ready. Drive could not be selected.
20	Illegal command in CDB.
30	WD2401 RAM failure.
31	ROM checksum error.
35	Maximum number of retries exceeded.
36	End of tape.
37	Addressed tape block not found.
38	Write protected.
39	File mark not detected.
3A	End of physical media.
3B	End of recorded data.
3C	Illegal tape structure. Missing blocks.

TAPE POSITIONING COMMANDS

Tape positioning commands (Rewind to Beginning of Tape, Erase and Retension only) issued to the BMTC are completed immediately, i.e., the Host issues the command, the WD2401 stores the command in internal RAM, then the WD2401 releases the SASI bus. The WD2401 remains connected to the SASI bus until completion of the Read File Marks command. The Host issues a Test Drive Ready command to the WD2401 to determine if the positioning command has been completed. An error condition is generated for an uncompleted drive positioning command. Normal completion of a drive positioning command is assumed if no error is presented.

REWIND TO BEGINNING OF TAPE (OP CODE 11)

This command causes the tape drive to rewind the tape from the tape's current position to the beginning of tape (BOT) position.

READ FILE MARKS (OP CODE 24)

The Read File Marks command moves the tape forward to a specified file marker. This command allows processing of multiple disk images or logical files as individual data sets.

ERASE TAPE (OP CODE 26)

This command erases and retensions the entire tape.

RETENSION TAPE (OP CODE 27)

This command causes the tape drive to rewind the tape to the BOT positon. Next, the tape drive winds the tape to the end of tape (EOT) position and rewinds to the BOT position.

FIND END OF DATA (OP CODE 28)

This command searches for the last recorded block on tape.

DATA TRANSFER COMMANDS

READ SENSE BYTES
(OP CODE 03)

This command returns one status byte. The block number with the error follows the status byte. A no error condition returns the block number of the last read or written block of data. The WD2401 returns four bytes of data to the Host. These bytes are:

	7	6	5	4	3	2	1	0
BYTE 0	B	0	T	T	E	E	E	E
BYTE 1	D	D	D	HIGH				
BYTE 2	MIDDLE							
BYTE 3	LOW							

NOTE: B represents the block address valid bit.
1 = block address is valid. 0 = invalid.
T represents the error type.
E represents the error code.
D represents the drive number in error.

WRITE BLOCK BUFFER
(OP CODE 0F)

This command allows the Host to perform memory diagnostics on the internal RAM. The controller must be in an idle state before this command is issued.

READ BLOCK BUFFER
(OP CODE 10)

This command allows the Host to perform memory diagnostics on the internal RAM. The controller must be in an idle state before this command can be issued.

READ TAPE BLOCKS
(OP CODE 21)

The Read Tape Blocks command restores the data from a streaming backup tape cartridge. This command restores both disk images and logical files. All read data transfers must pass the data into the Host memory.

WRITE TAPE BLOCKS
(OP CODE 22)

The Write Tape Blocks command writes data to tape from Host memory.

WRITE FILE MARK
(OP CODE 23)

This command writes a file mark block at the current tape postion. A file mark denotes the end of a complete disk image data set or the end of a logical file.

READ EXTENDED STATUS
(OP CODE 25)

The Read Extended Status command allows the user access to extensive error status information. This command sends 20 bytes of data to the Host.

The contents of these bytes are:

	7	6	5	4	3	2	1
BYTES 1 - 0	NUMBER OF REPOSITIONS						
BYTES 2 - 3	NUMBER OF UNDERRUNS						
BYTES 4 - 5	NUMBER OF OVERRUNS						
BYTES 6 - 7	NUMBER OF READ CRC ERRORS						
BYTES 8 - 9	NUMBER OF WRITE CRC ERRORS						
BYTE 10	MOST RECENT ERROR CODE						
BYTES 11 - 13	MOST RECENT ERROR BLOCK						
BYTES 14 - 16	NEXT BLOCK TO BE READ OR WRITTEN						
BYTE 17	NUMBER OF BLOCKS BUFFERED IN EXTERNAL RAM						
BYTE 18	MAJOR VERSION OF FIRMWARE						
BYTE 19	MINOR VERSION OF FIRMWARE						

OPERATIONAL MODE COMMANDS

DEFINE TAPE PARAMETERS (OP CODE 0C)

The Host issues this command to pass hardware parameters to the WD24C02. The Buffer Management Tape Controller passes these parameters to the WD24C02 in three bytes. These bytes are:

	7	6	5	4	3	2	1	0
BYTE 0	NUMBER OF TRACKS PER DRIVE							
BYTE 1	NUMBER OF RETRIES PER COMMAND							
BYTE 2	BLOCKS TO BUFFER BEFORE STARTING TAPE							

EXIT SPY MODE (OP CODE 41)

This command ends spy mode operation for short and long terms. Normal completion of a disk image dump or catastrophic errors require that streaming operations stop. Short term spy exits allow the Host to intermix disk operations with other disks.

TEST DRIVE READY (OP CODE 00)

The user issues this command to determine completion of a tape motion command. Completion of this command with no error indicates normal execution of the previously issued tape motion command. Simultaneous execution of this command and a tape motion command results in an error condition. Issuing a Read Sense Byte determines the exact state of the tape motion command or the cause of the error conditon.

BACKUP DISK IMAGE (OP CODE 40)

This command arms the tape controller and slaves it to the disk controller. The WD24C02 Read/Write Formatter intercepts data on the SASI Bus and writes the data to the tape. Interception of the data on the SASI Bus is the spy mode. The WD24C02 Read/Write Formatter throttles the disk controller by regulating the ACK signal from the Host.

PERFORM CONTROLLER DIAGNOSTICS (OP CODE E4)

This command causes the WD2401 to execute diagnostics and to detect errors. The user determines the exact error code by issuing the Read Sense Command.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C (32°F) to 70°C (158°F)
Storage Temperature ..... -65°C (-85°F) to + 150°C (302°F)
Volatage on any Pin with respect to ground ..... -0.5V to +7V
Power Dissipation ..... 1.5 Watts

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

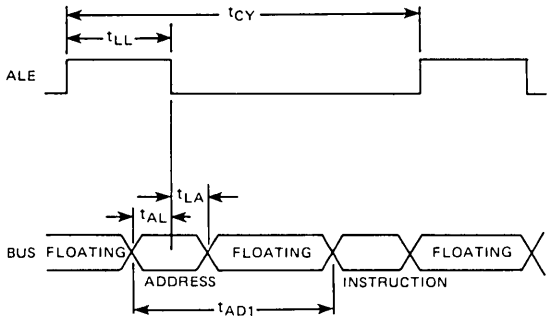
DC Operating Characteristics T_A = 0°C (32°F) to 70°C (158°F); V_{SS} = 0V, V_{CC} = 5V + 10%

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage (All except $\overline{BRST}$, XTAL1, and XTAL2)	-0.5	0.8	V	
V_{IL1}	Input Low Voltage ($\overline{BRST}$, XTAL1, and XTAL2)	-0.5	0.6	V	
V_{IH}	Input High Voltage (All except $\overline{BRST}$, XTAL1, and XTAL2)	2.0	5.0	V	
V_{IH1}	Input High Voltage ($\overline{BRST}$, XTAL1, and XTAL2)	3.8	5.0	V	
V_{OL}	Output Low Voltage (Bus)		0.45	V	I_{OL} = 2.0 mA
V_{OL1}	Output Low Voltage ($\overline{RE}$,$\overline{WE}$, ALE)		0.45	V	I_{OL} = 1.8 mA
V_{OL2}	Output Low Voltage (All other Outputs)		0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage (Bus)	2.4		V	I_{OH} = -400 μA
V_{OH1}	Output High Voltage ($\overline{RE}$,$\overline{WE}$,and ALE)	2.4		V	I_{OH} = -100 μA
V_{OH2}	Output High Voltage (All other Outputs)	2.4		V	I_{OH} = -40 μA

DC Electrical Characteristics (Cont'd.) T_A = 0°C (32°F) to 70°C (158°F); V_{CC} = 5V ±10%; V_{SS} = OV

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage Current (RDY and $\overline{INT}$)		±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{IL1}	Input Leakage Current (Pins 21 through 38)		-500	μA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current (Bus – High Impedance State, BSY)		±10	μA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
V_{CC}	Total Supply Current		80	mA	

AC CHARACTERISTICS T_A = 0°C (32°F) to 70°C (158°F); V_{SS} = 0V, V_{CC} = +5V + 10%

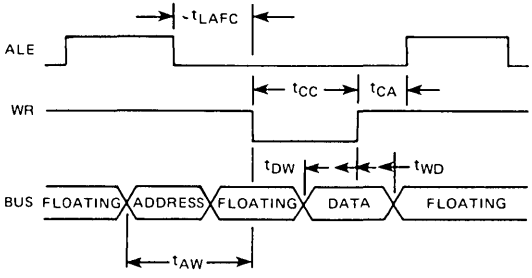


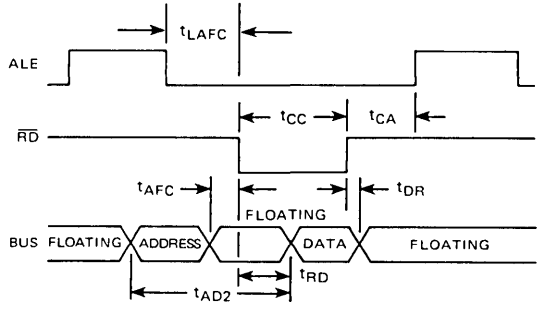
INSTRUCTION FETCH FROM EXTERNAL MEMORY TIMING

INSTRUCTION FETCH FROM EXTERNAL MEMORY TIMING

SYMBOL	CHARACTERISTICS	TYP	UNITS	CONDITIONS (NOTE 1)
t_{CY}	Cycle Time	2.5	μsec	NOTE 2
t_{LL}	ALE Pulse Width	413	nsec	
t_{LA}	Address Hold from ALE	126	nsec	
t_{AL}	Address Setup to ALE	223	nsec	NOTE 3
t_{AD1}	Address Setup to Data	1030	nsec	

NOTES: 1. Control output load capacitance equals 80 pF. Bus load capacitance equals 150 pF.
2. Assumes 50% duty cycle on XTAL1 and XTAL2.
3. Bus high impedance load equals 20 pF.





WRITE TO EXTERNAL DATA MEMORY

SYMBOL	CHARACTERISTICS	TYP	MIN
t_{LAFC}	ALE to Control ($\overline{WE}$, $\overline{RE}$)	425	nsec
t_{CC}	Control Pulse Width ($\overline{WE}$, $\overline{RE}$)	1050	nsec
t_{CA}	Control ($\overline{WE}$, $\overline{RE}$) to ALE	126	nsec
t_{DW}	Data Setup before $\overline{WE}$	883	nsec
t_{WD}	Data Hold after $\overline{WE}$	116	nsec
t_{AW}	Address Setup to $\overline{WE}$	683	nsec

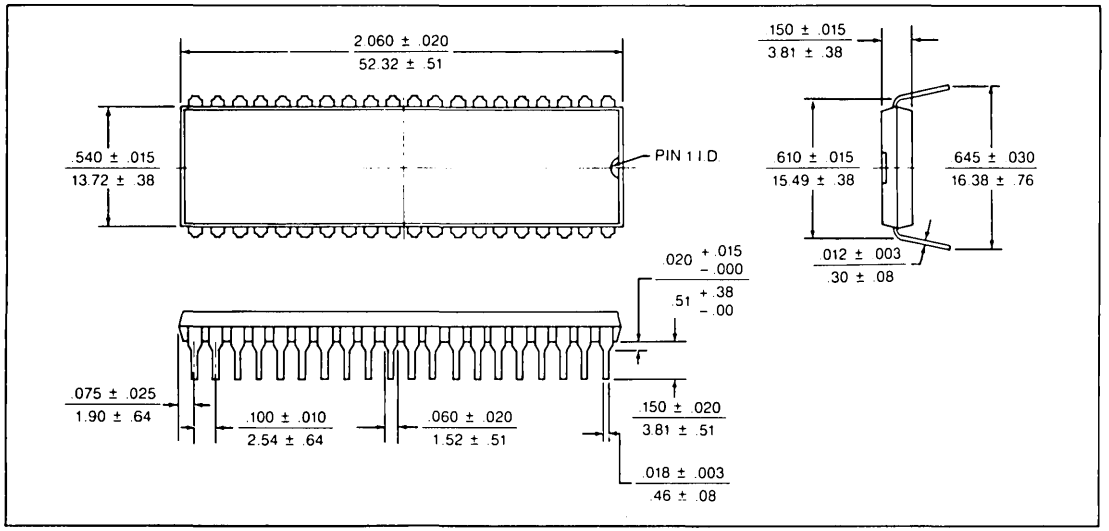
NOTE: Control output load capacitance equals 80 pF. Bus output load capacitance equals 150 pF.

READ FROM EXTERNAL DATA MEMORY

SYMBOL	CHARACTERISTICS	TYP	MIN
t_{LAFC}	ALE to Control ($\overline{RE}$, $\overline{WE}$)	425	nsec
t_{CC}	Control Pulse Width ($\overline{RE}$, $\overline{WE}$)	1050	nsec
t_{CA}	Control to ALE ($\overline{RE}$, $\overline{WE}$)	126	nsec
t_{AFC}	Address float to $\overline{RE}$	293	nsec
t_{DR}	Data Hold $\overline{RE}$	220	nsec
t_{RD}	$\overline{RD}$ to Data In	746	nsec
t_{AD2}	Address setup to read data	1530	nsec

NOTE: Control output load capacitance equals 80 pF. Bus output load capacitance equals 150 pF.

PACKAGE DIAGRAM



40 LEAD PLASTIC PL

WESTERN DIGITAL
CORPORATION

WD2404-DSM
Tape Data Separator Module

FEATURES

- FABRICATED USING STATE-OF-THE-ART SURFACE MOUNT TECHNOLOGY
- SMALL FORM FACTOR (2" X 2.5")
- INDUSTRY STANDARD QIC-36 INTERFACE
- CONFORMS TO QIC-36 ISV, BIT JITTER AND ASYMMETRY SPECIFICATIONS
- COMPLETELY SELF-ADJUSTING
- ±10% CAPTURE RANGE
- +5V and +12V OPERATIONS

DESCRIPTION

The WD2404-DSM is a completely self-contained, self adjusting, state-of-the-art design implemented in Surface Mount Technology. The tape data separator module provides a generic interface to a tape controller implementing a QIC-36 drive interface and QIC-24 recording format for ¼" streaming tape.

It requires a high speed 14.4 MHz clock and provides 7.2 MHz and 3.6 MHz clocks for system interface.

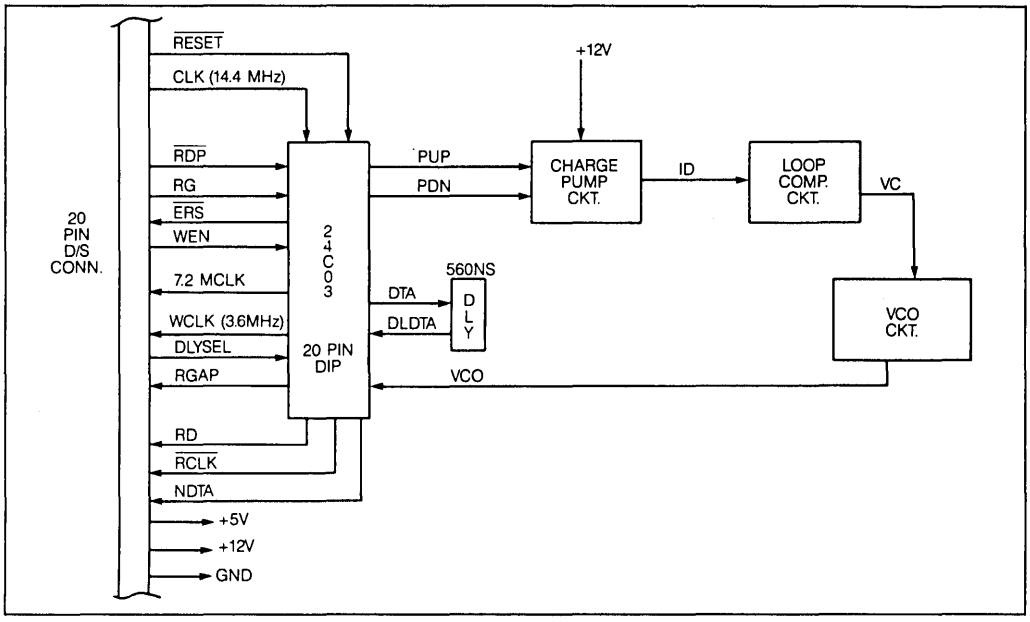
The tape data separator module consists of the following basic functional blocks.

- DATA SEPARATION LOGIC
- CHARGE PUMP CIRCUITS
- LOOP COMPENSATION CIRCUIT
- VCO CIRCUITS

An optional delay line is included on the module which can be disabled by the user.

There are absolutely no adjustments on the WD2404-DSM. The module looks at Raw Data Pulse (RDP) from the drive at Read Gate (RG) time and generates Expect to Receive Sync (ERS) and Read Gap (RGAP). It separates data and clock and generates RCLK and RD signals. It also detects the absence of data (Erased Tape) by asserting signal NDTA. The WD2404-DSM also has the capability to narrow the bit cell window during Read After Write (RAW) operation for additional data integrity.

The module is easy to integrate and is fabricated using Surface Mount Technology for high reliability. The module requires +5V and +12V supply.



TAPE DATA SEPARATOR BLOCK DIAGRAM

PIN NO.	SIGNAL	SIGNAL FUNCTION	I/O
1	RG	READ GATE	I
2	CLK	14.4 MHz CLOCK	I
3	7.2 MCLK	7.2 MHz CLOCK	O
4	RDP	RAW DATA PULSE	I
5	DLYSEL	DELAY SELECT 0–EXTERNAL 1–INTERNAL	I
6	RGAP	READ GAP	O
7	WCLK	WRITE CLOCK 3.6 MHz	O
8	DTA	DATA FOR DELAY LINE APPLICATION	O
9	RESET	RESET	I
10	DLDTA	EXTERNAL DELAYED DATA	I
11	ERS	EXPECT TO RECEIVE SYNC	O
12	N/C	RESERVED	
13	NDTA	NO DATA DETECTED	O
14	RD	READ DATA (SYNCHRONIZED)	O
15	WEN	WRITE ENABLE	I
16	RCLK	READ CLOCK (FOR CLOCKING RD)	O
17,19	GND	DC GROUND	
18	VCC	+5V DC	
20	+12V	+12V DC	

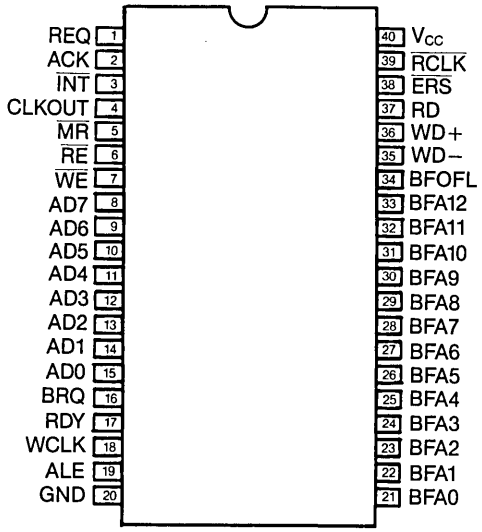
SIGNAL	FUNCTIONAL	DESCRIPTION
RG	READ GATE	Asserted whenever the tape controller is ready to read data from the drive also asserted during tape write for read after write function.
CLK	CLOCK	14.4 MHz TTL clock all tape related timings are derived from this high speed clock.
7.2 MCLK	7.2 MCLK	Divide by two clock for WD3600 tape controller.
$\overline{RDP}$	RAW DATA PULSE	Incoming data pulse from QIC-36 drive after 220/330Ω termination. This signal should meet the min/max pulse width/period requirements of QIC-36 specs.
DLYSEL	DELAY SELECT	This signal selects the internal 24C03 digital delay or external delay thru delay line default (line floating) state is digital delay connected to GND for delay line selection.
RGAP	READ GAP	Whenever a consecutive string of recorded one's (1's) are detected (min 32) this line is asserted and will stay asserted during the entire gap time minimum QIC-24 gap is 125 bits.
WCLK	WRITE CLOCK	This clock is four times the bit rate of tape data transfer (divide by four clock for WD24C02).
DTA	DATA	Data for delay line application (not to be used externally).
$\overline{RESET}$	RESET	Master reset used to synchronize internal circuits or WD24C03.
DLDTA	EXTERNAL DELAYED DATA	Data from delay line. (Not to be used externally).
$\overline{ERS}$	EXPECT TO RECEIVE SYNC	This signal is asserted by the module when a valid QIC-24 gap is verified and the data separator is locked in a phase mode assertion of this indicates the imminent occurence of sync mark shortly.
NDTA	NO DATA	This signal is asserted when illegal GCR pattern is encountered erased tape will constitute illegal GCR pattern.
RD	READ DATA	True vinary data separated from clock read data is synchronized with read clock (RCLK).
WEN	WRITE ENABLE	If asserted during a write operation this narrows the bit cell window for read after write operation providing additional data integrity.
$\overline{RCLK}$	READ CLOCK	Read Clock synchronized with seperated data. Data to be clocked with rising edge of the clock.
GND	GROUND	Power supply ground +5V & 12V return.
VCC	VCC	+5V from power supply.
+12V	+12V	+12V from power supply.

WESTERN DIGITAL
CORPORATION

WD24C02 Read/Write Formatter
Advance Information

FEATURES

- 40-PIN DUAL IN-LINE PACKAGE GATE ARRAY DEVICE
- SINGLE +5V POWER SUPPLY
- SUPPORTS QIC-24 REV. D TAPE FORMAT
- READ-AFTER-WRITE VERIFICATION
- SUPPORTS AN EXTERNAL 8 KB (16 BLOCKS) BLOCK BUFFER
- INTERFACES TO AN EXTERNAL BUFFER MANAGER (E.G., WD2401)
- DIRECT INTERFACE TO DATA SEPARATOR LOGIC
- HANDLES DMA REQUEST AND ACKNOWLEDGE HANDSHAKE FOR HOST DATA TRANSFERS
- BUS CONTROL AND A MULIPLEXED ADDRESS AND DATA BUS FOR MICROPROCESSOR INTERFACE
- COMMAND AND STATUS REGISTERS



PIN DESIGNATION

DESCRIPTION

The WD24C02 is a multifunctional gate array device. This device performs QIC-24 read and write formatting with read-after-write verification. (QIC is an acronym for Quarter-Inch Compatibility). The WD24C02 is controller by a Buffer Management Tape Controller (WD2401) or other external microprocessor programmed for buffer management of tape data.

The WD24C02 DMA request and acknowledge signals control the transfer of read and write data between the Host and an external block buffer. (The block buffer is an external 8K byte random access memory.This memory is divided into 16 pages. Each page is 512 bytes in length.) These signals throttle the SASI bus, when required, to compensate for disk latencies. The WD2402 also maintains the buffer addresses (lower 9 bits) for Host or device access.

The Status Register represnts the current status of the WD24C02 and is read by the buffer manager. All read and write functions are selected by writing a command in the Command Register.

The WD24C02 runs at a 3.6 MHz clock rate and provides a real time clock of 90 KHz for the tape drive interface. External data separator logic directly interfaces with the WD24C02.

SIG. PIN	SIGNAL MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
1	REQ	DMA REQUEST	I	Assertion of this signal indicates the Host is ready to access the external block buffer for a read or write.
2	ACK	DMA ACKNOWLEDGE	O	Assertion of this signal indicates to the requesting device that the address is available to the external block buffer for a read or write cycle.
3	$\overline{INT}$	$\overline{INTERRUPT}$	0	Assertion of this signal indicates to the Host the start of a read or write gap.
4	CLKOUT	OUTPUT CLOCK	0	Real time clock for external circuitry.
5	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	Assertion initializes the WD24C02.
* 6	$\overline{RE}$	$\overline{READ\ ENABLE}$	I/O	Bi-directional, tri-state line. Assertion as an input writes data into the WD24C02 internal register. Assertion as an output indicates the WD24C02 is writing data to the external block buffer.
* 7	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	I/O	Bi-directional, tri-state line. Assertion as an input writes data into the WD24C02 internal registers. Assertion as an output indicates the WD24C02 is writing data to the external block buffer.
8 thru 15	AD7 thru AD0	MULTIPLEXED ADDRESS AND DATA BUS	I/O	Eight-bit, bi-directional, multiplexed data and address bus. Addresses are input only. The bi-directional data lines transfer command and status information.
16	BRQ	BUS REQUEST	I	Assertion indicates a request for access to the WD24C02 internal registers.
17	RDY	READY	O	Assertion indicates to the requesting device that the bus is available. At least one access can be made every 11.1 μsec. DMA requests are not acknowledged during this time.
18	WCLK	WRITE CLOCK	I	Internal clock for write data transfers and other internal timing purposes.
19	ALE	ADDRESS LATCH ENABLE	I	Assertion of this signal latches the address from the multiplexed address and data bus.
20	GND	GROUND		Ground.
21 thru 33	BFA0 thru BFA12	BUFFER ADDRESS BUS	O	Address bus for external buffer RAM. BFA0 is the least significant bit (LSB).
34	BF0FL	BUFFER OVERFLOW	O	Assertion of this signal indicates to the BMTC that the 512 byte external RAM buffer is full. The page pointer requires updating for the next data transfer.
35	WD–	TAPE WRITE DATA –	O	Run length limited (RLL) encoded data.
36	WD +	TAPE WRITE DATA +	O	Complementary data.

SIG. PIN	SIGNAL MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
37	RD	TAPE READ DATA	I	RLL encoded data (from Data Separator).
38	$\overline{ERS}$	$\overline{EXPECT\ TO\ RECEIVE\ SYNCHRONIZATION}$	I	Assertion of this signal indicates to the read sequencer the imminent occurrence of the synchronization character.
39	$\overline{RCLK}$	$\overline{READ\ CLOCK}$	I	Extracted clock from RAW DATA PULSE (RDP).
40	V_{CC}	V_{CC}		+5V + 5% power supply.

WD1036R-SHD Streaming Tape Controller

FEATURES

- SASI 8-BIT BI-DIRECTIONAL BUS HOST INTERFACE
- QIC-36 1/4-INCH STREAMING TAPE DRIVE
- CONFORMS TO QIC-24 FORMAT SPECIFICATIONS
- READ-AFTER-WRITE VERIFICATION
- EXTENSIVE ERROR RECOVERY ABILITY
- ON-BOARD 8K BYTE BUFFER
- SUPPORTS TAPE DRIVES WITH A 720-K BIT DATA TRANSFER RATE
- 90-IPS TAPE SPEED
- START/STOP OR STREAMING OPERATION
- 5.5 IN. X 8 IN. PCB FORM FACTOR
- ADJUSTMENT FREE DATA SEPARATOR

DOCUMENT SCOPE

This document is intended to provide the reader with an overview of the WD1036R-SHD, for a detailed understanding it will be necessary to refer to the following documents:

SASI™
QIC-24, QIC-36
WD1036R-SHD OEM manual document number 79-000028
WD2401 BMTC Data sheet
WD24C02 R/W Formatter Data sheet

SASI is a trademark of Shugart Inc.

DESCRIPTION

The WD1036R-SHD is a stand-alone Streaming Tape Controller board that interfaces to a single 1/4-inch QIC-36 streaming tape drive. The WD1036R-SHD uses industry standard QIC-24 Read/Write formatting.

The WD1036R-SHD communicates with the Winchester disk drive controller (possibly a WD1002-SHD) through the Host controlled SASI bus. All data, status information, and commands are transferred via this bus.

Figure 1 shows a typical system configuration.

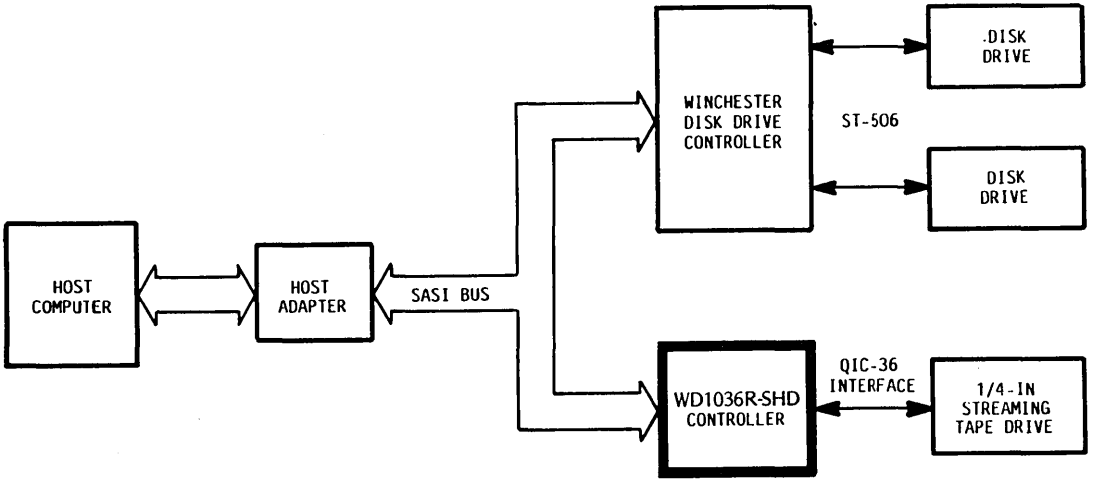


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

ARCHITECTURE

The WD1036R-SHD has three on-board connectors, the power connector P1, Host connector J1, and tape drive connector J2. Figure 2 is a block diagram illustrating the major areas of the WD1036R-SHD. These sections consist of a WD2401 Buffer Manager/Tape Controller, WD24C02 Read/Write Formatter, an 8K byte RAM, Data Separator, SASI interface, tape drive interface, and misc. buffers and latches.

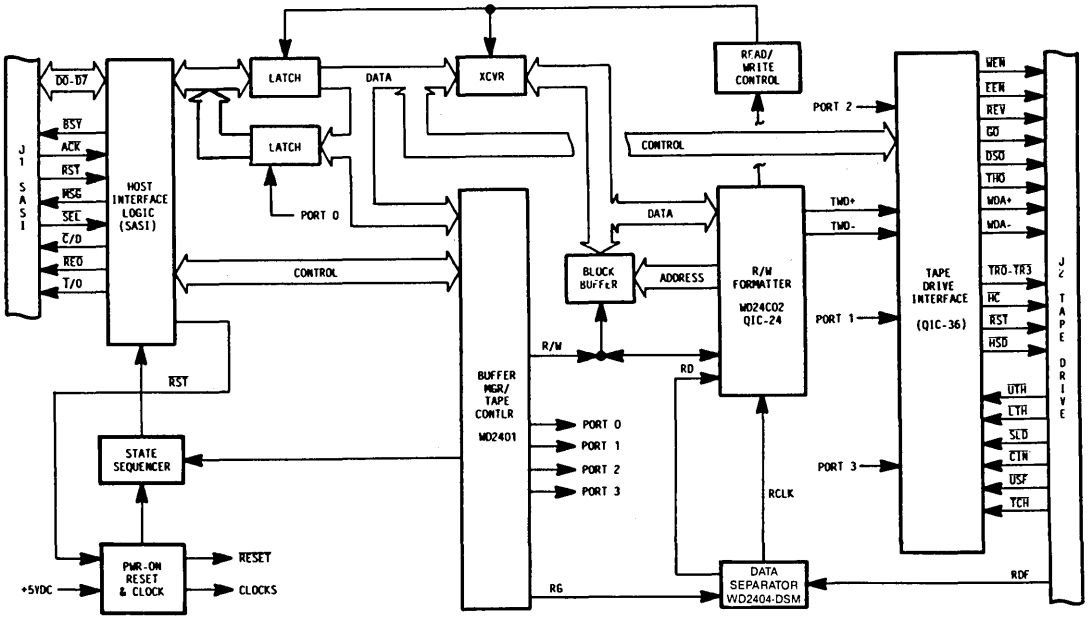


FIGURE 2. WD1036R-SHD STREAMING TAPE CONTROLLER, BLOCK DIAGRAM

WD2401 BMTC

The WD2401-BMTC consists of an 8-bit microcontroller, 4K bytes of ROM, containing Western Digital proprietary firmware, and 256 bytes of RAM. The WD2401-BMTC is responsible for performing the following functions:

- Receive an interpret SASI commands and pass certain commands to the WD24C02 Read/Write Formatter.
- Act as the handshake controller with both SASI interface hardware and the tape drive, and control all tape drive motion.
- Periodically poll the status and sense signals from the tape drive, then determine and initiate the appropriate action.
- Manage the RAM buffer and furnish the four high-order address bits (page number) to the WD24C02.
- Initialize the Page Pointer and Command Registers in the WD24C02 following a power up reset, or a reset (RST) from the initiator.
- Perform a diagnostic routine to test the microprocessor, RAM, and ROM at power-up or reset from the initiator.
- Perform error handling and maintain an error log in it's internal RAM.

WD24C02 R/W Formatter

Write formatter logic in the WD24C02 reads data from the RAM buffer, formats it to QIC-24 requirements, and serializes the data to be written on the tape.

Read formatter logic accepts serial data from Data Separator logic, deserializes it, decodes GCR-coded data, and transfers data to the RAM Buffer. This logic also detects File Marks, strips out the gap, sync characters, and block address, and performs the CRC Check, generating a CRC error flag when an error occurs. Read formatter logic also performs the Read Check during a write operation.

The WD24C02 detects error status and passes it on to the WD2401, which maintains an error log in its internal RAM.

The WD24C02 maintains the nine low-order address bits at the RAM Buffer for either Host or drive access. The four high-order address bits - block select - are maintained by the WD2401 but supplied to the RAM by the WD24C02.

Buffer arbitration is managed so that the Host does not run over a restricted block buffer. A bad block is not transferred to the Host during a restore operation.

Buffer RAM

The 8K-byte RAM is treated as 16 blocks of 512 bytes each, which correspond to the block size on tape. The four high-order address lines select the block. Bi-directional data lines are connected to SASI Bus latches and to the WD24C02 data lines. The buffer is addressed by the WD24C02 while the WD2401 controls the reading and writing of the buffer.

Data Separator

The Data Separator recognizes the data as it is read from the tape, removes the clock pulses, and transfers the data (RD) to the WD24C02. Handshaking with the WD2401 is through RG and RGAP signals which define the beginning of data. The WD2404-DSM is initialized at power-up or by the initiator issuing $\overline{\text{RST}}$.

The WD2404-DSM is a self contained module requiring no adjustments. It is installed as a piggy-back card by mating the rear entry connector J1 on the module to J3 on the WD1036R-SHD.

SPECIFICATIONS

HOST INTERFACE

Type	SASI
Cable length (Daisy Chained)	15 ft. (4.6m) max.
Cable connector	50 pin Berg 65610-150 or Molex 10-89-1501
Termination	Socketed 220/330 ohm resistor pack
Addressing	Jumper selectable (1 through 8) Default = 2

DRIVE INTERFACE

Type	QIC-36 Rev. B Standard
Cable length	10 ft. (3 m) max.
Cable connector	50 pin Berg 65610-150 or Molex 10-89-1501
Termination	220 ohms to +5 volts 330 ohms to ground
Recording method	QIC-24, NRZI, GCR (0,2) at 10,000 frpi.
CRC polynomial	$X^{16} + X^{12} + X^5 + 1$
Cartridge Capacity	1/4 in. 9 track DC300A = 30 MByte DC300XL = 45 MByte DC600A = 60 MByte

DATA SEPARATOR

Acquisition time	<64 bit times
Capture range	±25%
Bit jitter tolerance	See Figure 3
Asymmetry tolerance	See Figure 3

POWER

Cable connector	4 pin, right angle Molex 15-24-4041 AMP 641737-1
Voltage	+5 VDC ±5% +12 VDC ±5%
Current	1.5A max. 1.2A typ. @ 5 volts 50ma max. 20ma typ. @ 12 volts
Ripple	0.1 volt

DIMENSIONS

Length	8 inches
Width	5.50 inches
Height (max. including board, components, and leads)	0.5 inch

ENVIRONMENTAL

Ambient temperature	0°C (32°F) to 55°C (131°F)
Relative humidity	10% to 90% non-condensing
Altitude	0 to 10,000 ft (3048 m)
Air flow	150 linear ft/min @ 0.25 inches from the component surface
MTBF	10,000 hrs.
MTTR	30 min.

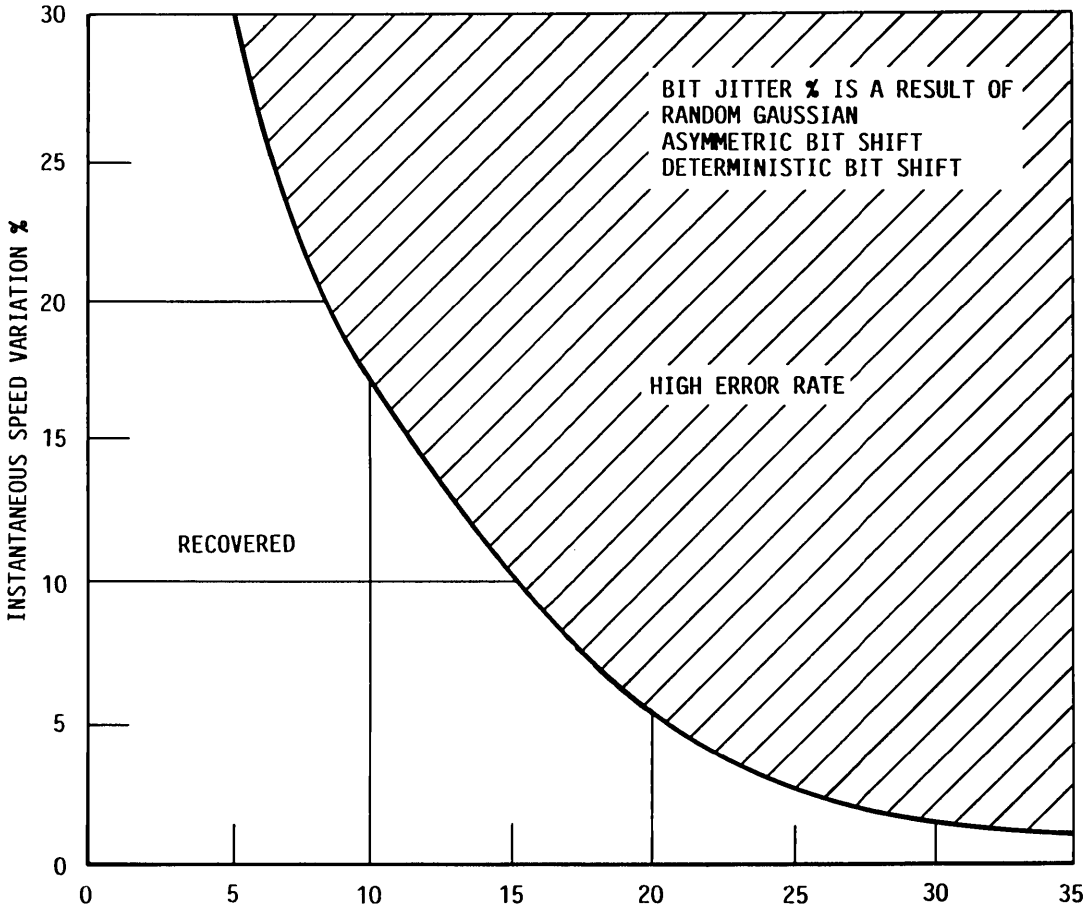


FIGURE 3. BIT JITTER (%)

HOST INTERFACE

The SASI interface is a daisy-chained bus interconnecting the Host computer, the WD1036R-SHD, Winchester drive controller, and other peripheral or peripheral controllers up to a total of eight. The WD1036R-SHD is connected to the bus through a 50-pin flat cable which may be as long as 15 feet. The connector on the WD1036R-SHD is a Berg 65610-150 or Molex 10-89-1501.

The bus is terminated at the WD1036R-SHD using a socketed resistor pack to facilitate daisy-chaining. The WD1036R-SHD is strapped at the factory to respond to SASI address 2 but may be changed by moving a jumper to the desired address.

TABLE 1. HOST INTERFACE CONNECTOR (J1) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1 thru 15	2 thru 16	$\overline{D0}$ thru $\overline{D7}$	$\overline{DATA\ 0}$ thru $\overline{DATA\ 7}$	I/O	Eight-bit, bi-directional, tri-state, bus used to transfer commands, status, and data between the Host and Controller and other devices on the bus.
17 thru 33	18 thru 34	$\overline{ABORT}$	$\overline{ABORT}$	I	Optional hardware $\overline{ABORT}$ signal. Pin selected by movable jumper. Allows the Host to reset the WD1036R-SHD without effecting other devices on the bus.
35	36	$\overline{BSY}$	$\overline{BUSY}$	O	Indicates to the Host that the WD1036R-SHD is busy executing a command and is unable to accept another command. The trailing edge acknowledges receipt of $\overline{SEL}$ and indicates that the transaction is completed.
37	38	$\overline{ACK}$	$\overline{ACKNOWLEDGE}$	I	$\overline{ACK}$ is an input signal when used with $\overline{REQ}$ as a handshake signal for byte transfer. Both leading and trailing edges are used.
39	40	$\overline{RST}$	$\overline{RESET}$	I	When asserted for at least 100 nsec, $\overline{RST}$ places the WD1036R-SHD in its initial power-up state.
41	42	$\overline{MSG}$	$\overline{MESSAGE}$	O	Indicates the end of the present transaction.
43	44	$\overline{SEL}$	$\overline{SELECT}$	I	When asserted, gives control of the bus to the selected device address.
45	46	$\overline{C}$/D	$\overline{CONTROL}$/ DATA	O	As an output signal, $\overline{C}$/D along with $\overline{I}$/O and $\overline{MSG}$ signals the Host the type of bus transfer that is expected by the WD1036R-SHD. $\overline{C}$/D - 0 = Control - 1 = Data Control is defined as a: command, status or message.
47	48	$\overline{REQ}$	$\overline{REQUEST}$	O	$\overline{REQ}$ is an output signal when used with $\overline{ACK}$ as a handshake signal for data transfer between the Host and WD1036R-SHD. Both leading and trailing edges are used.
49	50	$\overline{I}$/O	$\overline{INPUT}$/ OUTPUT	O	As an output singal $\overline{I}$/O defines the direction of the transfer: 1 = output from the Host 0 = input to the Host

TAPE DRIVE INTERFACE

The WD1036R-SHD interfaces to the tape drive through a 50-pin flat cable no more than 10 feet in length. The interface comprises 25 lines, three of which are reserved for future use. The 50-pin edge connector on the WD1036R-SHD mates with a Berg 65610-150, Molex 10-89-1501, or equivalent.

The lines are terminated with 220 ohms to +5 volts and 330 ohms to ground. All signals to the WD1036R-SHD are terminated at the WD1036R-SHD and must be able to drive two TTL loads plus the termination.

TABLE 2. TAPE DRIVE INTERFACE CONNECTOR (J2) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	2	$\overline{GO}$	$\overline{GO}$	O	$\overline{GO}$ controls the capstan servo. $\overline{GO}$ starts the tape motion sequences in the direction specified by $\overline{REV}$.
3	4	$\overline{REV}$	$\overline{REVERSE}$	O	$\overline{REV}$ controls the direction of the capstan servo. When asserted with $\overline{GO}$, the tape motion is in the reverse direction.
5	6	$\overline{TR3}$	$\overline{TRACK\ SELECT\ 3}$	O	Track Select bit 3. $\overline{TR3}$ through $\overline{TR0}$ is the binary coded track number used by the drive to select a designated track. (MSB)
7	8	$\overline{TR2}$	$\overline{TRACK\ SELECT\ 2}$	O	Track Select bit 2. $\overline{TR3}$ through $\overline{TR0}$ is the binary coded track number used by the drive to select a designated track.
9	10	$\overline{TR1}$	$\overline{TRACK\ SELECT\ 1}$	O	Track Select bit 1. $\overline{TR3}$ through $\overline{TR0}$ is the binary coded track number used by the drive to select a designated track.
11	12	$\overline{TR0}$	$\overline{TRACK\ SELECT\ 0}$	O	Track Select bit 0. $\overline{TR3}$ through $\overline{TR0}$ is the binary coded track number used by the drive to select a designated track. (LSB)
13	14	$\overline{RST}$	$\overline{RESET}$	O	$\overline{RST}$ is a minimum pulse of 13 usec. It starts the initialization routine and recalibration of the head to its reference position.
15	16		RESERVED		
17	18		RESERVED		
19	20		RESERVED		
21	22	$\overline{DS0}$	$\overline{DRIVE\ SELECT\ 0}$	O	When asserted $\overline{DS0}$ permits basic tape drive operations to proceed. $\overline{DS0}$ enables the transfer of control signals: RDP CIN USF TCH EEN. The drive acknowledges receipt of $\overline{DS0}$ by sending $\overline{SLD}$.
23	24	$\overline{HC}$	$\overline{HIGH\ CURRENT}$	O	When asserted, enables operation with DC 600A tape cartridges. Refer to ANSC Project 671 Unrecorded Magnetic Tape Cartridge for Information Interchange, 0.250 inch (6.30mm) 6400-10000 flux-reversals per inch (252-394 frpmm).
25	26	$\overline{RDP}$	$\overline{READ\ DATA\ PULSE}$	I	Serial-bit data read from tape to the WD1036R-SHD. $\overline{RDP}$ is present when data passes the read head and $\overline{DS0}$ is asserted.

TABLE 2. TAPE DRIVE INTERFACE CONNECTOR (J2) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
27	28	$\overline{\text{UTH}}$	$\overline{\text{UPPER TAPE POSITION HOLE}}$	I	$\overline{\text{UTH}}$ and $\overline{\text{LTH}}$ encode information having to do with tape position as follows:
29	30	$\overline{\text{LTH}}$	$\overline{\text{LOWER TAPE POSITION HOLE}}$	I	$\overline{\text{UTH}}$ $\overline{\text{LTH}}$ MEANING 1 1 Beginning of Tape 0 1 End of Tape 1 0 Warning Zone 0 0 Recording Zone The Recording Zone is between the Load Point and the Early Warning hole if BOT or EOT has been detected since the last cartridge insertion ($\overline{\text{CIN}}$). Otherwise 0 0 means the tape position is not known.
31	32	$\overline{\text{SLD}}$	$\overline{\text{DRIVE SELECTED}}$	I	Tape drive acknowledgement to the WD1036R-SHD or receipt of the $\overline{\text{DS0}}$.
33	34	$\overline{\text{CIN}}$	$\overline{\text{CARTRIDGE IN}}$	I	$\overline{\text{CIN}}$ is asserted when a tape cartridge is in place and the WD1036R-SHD asserts $\overline{\text{DS0}}$, and GO.
35	36	$\overline{\text{USF}}$	$\overline{\text{UNSAFE}}$	I	The drive asserts $\overline{\text{USF}}$ when the File Protect Plug is not in the safe position on the cartridge and the WD1036R-SHD asserts $\overline{\text{DS0}}$. This state permits data to be written and erased.
37	38	$\overline{\text{TCH}}$	$\overline{\text{TACH PULSE}}$	I	$\overline{\text{TCH}}$ is present while tape is moving.
39	40	WDA-	WRITE DATA-	O	Data to be written on tape, enabled while $\overline{\text{WEN}}$ is asserted. System is optimized to record GCR data at a nominal density of 10,000 frpi.
41	42	WDA+	WRITE DATA+	O	The inverse of WDA-.
43	44	$\overline{\text{THD}}$	$\overline{\text{THRESHOLD}}$	O	Sets a percentage-qualifying voltage threshold for Read Data. Eliminates data of marginal quality read from tape.
45	46	$\overline{\text{HSD}}$	$\overline{\text{HIGH SPEED}}$	O	Asserted = 90 ips tape speed. WD1036R-SHD never de-asserts $\overline{\text{HSD}}$.
47	48	$\overline{\text{WEN}}$	$\overline{\text{WRITE ENABLE}}$	O	When asserted, enables drive to write data.
49	50	$\overline{\text{EEN}}$	$\overline{\text{ERASE ENABLE}}$	O	Tape is erased the full width of the erase head when the WD1036R-SHD selects track 0, and asserts $\overline{\text{DS0}}$ and $\overline{\text{EEN}}$.

WD1036R-SHD COMMANDS

To facilitate intergration of the WD1036R-SHD into the system, the protocol and command structure is the same as that of the WD1002-SHD Disk Controller.

The commands can be classified into three groups: Tape positioning, data transfer and control mode. Each command is characterized by a 6-byte Command Description Block. Table 3 is a summary of the commands and Table 4 represents the Command Description Block.

TABLE 3. COMMAND SUMMARY

COMMAND	OP CODE	LUN	BLOCK NO.	COUNT	OPTIONS
Tape Position					
Rewind To BOT	11	D	0	0	0
Read File Marks	24	D	0	V	T
Erase Tape	26	D	0	0	0
Retension Tape	27	D	0	0	0
Find End of Data	28	D	0	0	T
Data Transfer					
Read Sense Bytes	03	D	0	0	C
Write Block Buffer	0F	0	0	0	P
Read Block Buffer	10	0	0	0	P
Read Tape Blocks	21	D	V	V	R T F
Write Tapes Blocks	22	D	0	V	U T H
Write File Mark	23	D	0	V	T H
Read Extended Status	25	D	0	0	C
Operation Mode					
Test Drive Ready	00	D	0	0	0
Define Tape Parameters	0C	D	0	0	0
Diagnostics	E4	0	0	0	0

TABLE 4. COMMAND DESCRIPTION BLOCK

	BIT							
BYTE	7	6	5	4	3	2	1	0
0	OPERATION CODE							
1	LOGICAL UNIT NUMBER			BITS 20 THRU 16 OF TAPE BLOCK ADDRESS				
2	BITS 15 THRU 8 OF TAPE BLOCK ADDRESS							
3	BITS 7 THRU 0 OF TAPE BLOCK ADDRESS							
4	COUNT FIELD							
5	OPTION BITS (see table 5.)							

Operation Code	Bits 7-5 designates a command class of 0, 1, 2, or 7. Bits 4-0 identifies the function of the command, e.g., Erase, Rentension, etc.
Logical Unit No.	Logical unit number of the target tape drive.
Tape Block Address	Used by the Read Tape Block command to locate the first block to be read within a file.
Count Field	Used by the Read File Mark command to locate the file that is to be read by a Read Tape Block command. Used by a Write File Mark command to control the number of File Marks to be written. Used by a Read/Write Tape Blocks command to control the number of blocks to be read or written.
Option Bits	See Table 5.

TABLE 5. OPTION BITS

COMMAND	BIT 7	6	5	4	3	2	1	0
Read Sense Bytes	0	0	0	0	0	C	0	0
Find End of Data	0	0	T	0	0	0	0	0
Write Block Buffer	0	0	0	0	P	P	P	P
Read Block Buffer	0	0	0	0	P	P	P	P
Read Tape Blocks	R	F	T	0	0	0	0	0
Read File Marks	0	0	T	0	0	0	0	0
Write Tape Blocks	0	0	T	H	U	0	0	0
Write File Marks	0	0	T	H	0	0	0	0
Read Extended Status	0	0	0	0	0	C	0	0
All other commands	0	0	0	0	0	0	0	0

LEGEND:

P - Page Number. External block number contains sixteen 512-byte pages of memory.

R - Reposition.
0 = Disable
1 = Enable. Reading starts at the tape block specified in the Command Description Block. The Reposition option also initiates a Flush option.

F - Flush.
0 = Disable
1 = Flush data blocks from buffers before reading more blocks.

U - Underrun.
0 = Stop tape motion on underrun.
1 = Continue streaming on underrun.

T - Threshold
0 = Disable
1 = Enable threshold at Read Head.

H - High Current
0 = Disable
1 = Increase Write Current for high-coercivity tape. e.g., DC600A

C - Clear Inernal Counters
0 = Disable
1 = Clear Read/Write CRC errors and Under/Overrun counter.

WD1036S-WX2 Streaming Tape Controller

FEATURES

- 3.9 X 8.1" IBM PC/XT/AT FORM FACTOR
- SUPPORTS ONE 1/4" BASIC TAPE DRIVE (QIC-36)
- INDUSTRY STANDARD QIC-24 RECORDING FORMAT
- ON BOARD WD24CO2 READ/WRITE FORMATTER CHIP
- READ-AFTER-WRITE VERIFICATION
- EXTENSIVE ERROR RECOVERY WITH AUTOMATIC RETRIES
- DMA TRANSFER CAPABILITY
- SUPPORTS 90 IPS STREAMING OPERATION
- APPLICATION SOFTWARE TO RUN UNDER IBM PC DOS 2.0 TO EMULATE IBM'S BACKUP/RESTORE COMMANDS
- FILE-BY-FILE BACKUP/RESTORE CAPABILITY

DESCRIPTION

The WD1036S-WX2 is a single board streaming tape controller for IBM PC/AT/XT and compatible computers. This controller supports one 1/4" cartridge tape drive with QIC-36 interface. (QIC is an acronym for Quarter-Inch Compatibility).

The two utilities TBACKUP and TRESTORE provided with the controller enable file backup and restore from Winchester to tape and vice versa on the IBM system bus. These utilities require a minimum of 128KB of memory, but achieve a higher performance with 256KB or more. The memory size determines the maximum number of blocks that can be transferred by a single command during backup and restore operations. The command set also allows searching of records on tape.

The recording format conforms to the QIC-24 standard. The WD1036S-WX2 performs read-after-write verification and rewrites the data block, as required, in case of an error. Similarly, it repositions and rereads a record for read errors. A 16-bit cyclical redundancy check (CRC) ensures detection of an error. The WD1036S-WX2 automatically attempts to reread or rewrite data up to 16 times on errors.

Application software is supplied which emulates selective file backup and restore functions provided by IBM PC DOS 2.0.

HARDWARE ARCHITECTURE

The WD1036S-WX2 is based on the WD24C02 Read/Write Formatter device. There are three support modules to the WD24C02. One module buffers Host bus signals, decodes and translates Host bus commands into board control signals, and builds WD24C02 commands. Another module separates the drive data into clocks and read data and provides signals that indicate tape data gap times. The last module is responsible for the drive status and control. Figure 1 is a hardware block diagram of the WD1036S-WX2.

The PC interface and Buffer module contains bus transceivers, address decoding circuitry, control signal receivers, and the WD1100-18 gate array. The WD1100-18 translates Host bus commands and generates control signals for the WD24C02. The WD1100-18 also serves as a two byte DMA buffer between the Host and WD24C02.

The Data Separation module uses a phase lock loop that tracks incoming data pulses, generates a read clock and read data.

The Drive Control and Status module contains a set of registers that are loaded via Host bus commands. These registers transmit control bits to the drive through high current drivers. This module also buffers status lines from the drive. Issuing a Read Status command to the WD1036S-WX2 places the status information including the cartridge-in status unto the Host bus.

SOFTWARE ARCHITECTURE

The two stand-alone utilities TBACKUP and TRESTORE are designed to run under IBM PC DOS version 2.0 or later. These utilities will operate with a 128KB memory system. But a higher performance is achieved with 256KB or larger memory systems.

Figure 2 illustrates the architecture of the TBACKUP and TRESTORE programs. The Application Level is written to interface with a common module called Core. The Core is a high level interface between the application code and the Tape Access Module. The Core isolates the application program from the low level operations of tape positioning, tape drive interface timing characteristics, and data formatting considerations. Thus, an application program is simplified by not dealing with these low level operations.

The Core module contains two functional components, a Command Processor and a Buffer Manager. These components are compatible with machines that differ from the IBM PC. Compatibility is achieved by coding these functions in C and performing no hardware or operating system dependent operations in the Core.

The Application level module uses the high level command set described in the section titled Software Commands.

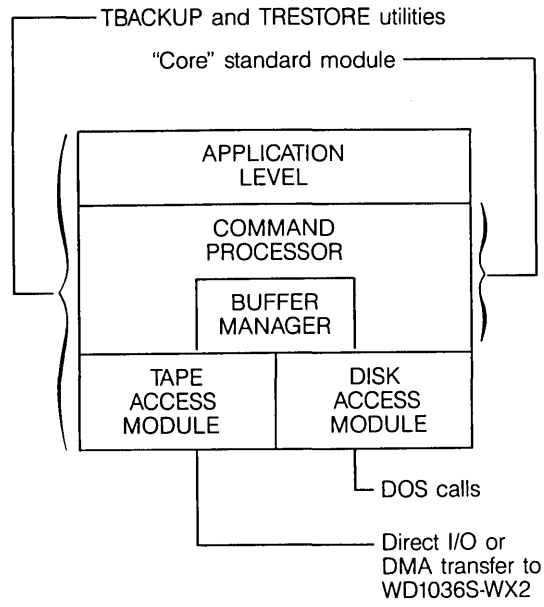


FIGURE 2.
WD1036S-WX2 SOFTWARE BLOCK DIAGRAM

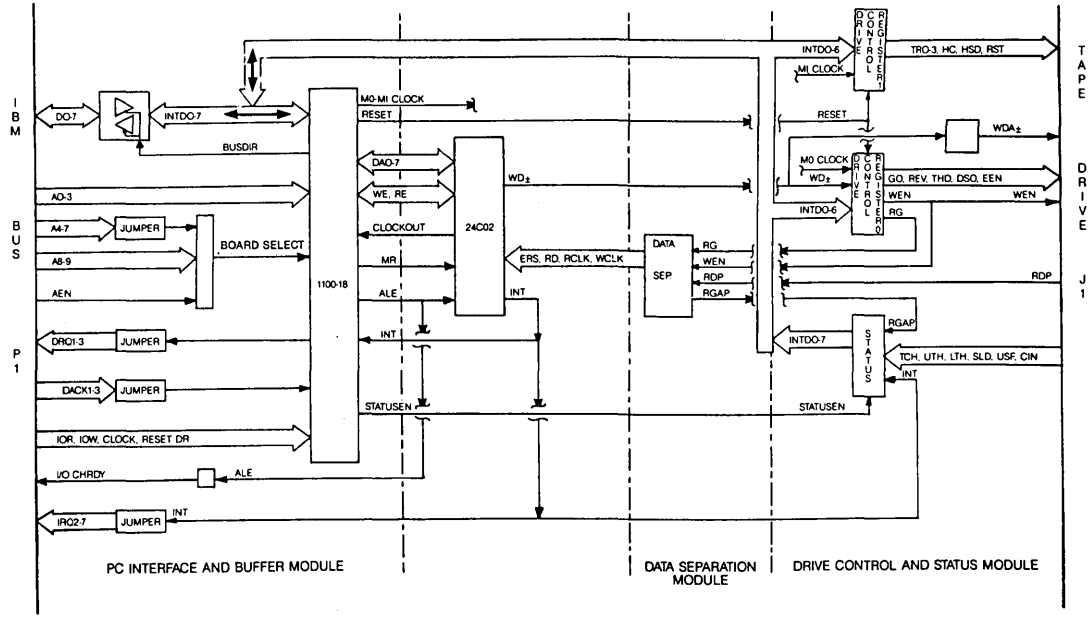


Figure 1. WD1036S-WX2 HARDWARE BLOCK DIAGRAM

SPECIFICATIONS

HOST INTERFACE

Type	IBM PC/AT, PC/XT
Cable length	Connects directly to the Host mother board with a 62-Pin card edge connector.
Addressing	Jumper selectable (300 through 3F0) Default = 330
Interrupt Channel	Jumper selectable (IRQ2 through IRQ7) Default IRQ3
DMA Channel Request	Jumper selectable (DRQ1,2 and 3) Default DRQ1.
Memory Requirements	128K Bytes min. 256K bytes or more are recommended.

DRIVE INTERFACE

Type	QIC-36 Rev. B Standard
Cable length	10 ft. (3 m) max.
Cable connector	50 pin 3 M 3425-6050 at the WD1036S-WX2 3 M 3415-001 at the drive
Termination	220 ohms to +5 volts 330 ohms to ground
Recording method	QIC-24, NRZI, GCR (0,2) at 10,000 frpi.
CRC polynomial	x16 + x12 + x5 + 1
Cartridge Capacity	1/4 in. 9 track DC300A = 30 MByte DC300XL = 45 MByte DC600A = 60 MByte
Tape speed	90 inches per second

DATA SEPARATOR

Acquisition time	< 64 Bit times.
Capture range	±25%
Bit jitter tolerance	See Figure 3
Asymmetry tolerance	See Figure 3

POWER

Voltage	+5 VDC ±5% +12 VDC ±5%
Current	1A max. 800ma typ. @ 5 volts 30 ma max. 20ma typ. @12 volts
Ripple	0.1 volt

DIMENSIONS

Length	8.1 inches
Width	3.9 inches
Height (max including board, components, and leads).	0.5 inch

ENVIRONMENTAL

Ambient temperature	0°C (32°F) TO 55°C (131°F)
Relative humidity	10% to 90% non-condensing
Altitude	0 to 10,000 ft (3048 m)
Air flow	150 linear ft/min @ 0.25 inches from the component surface
MTBF	10,000 Hrs.
MTTR	30 min.

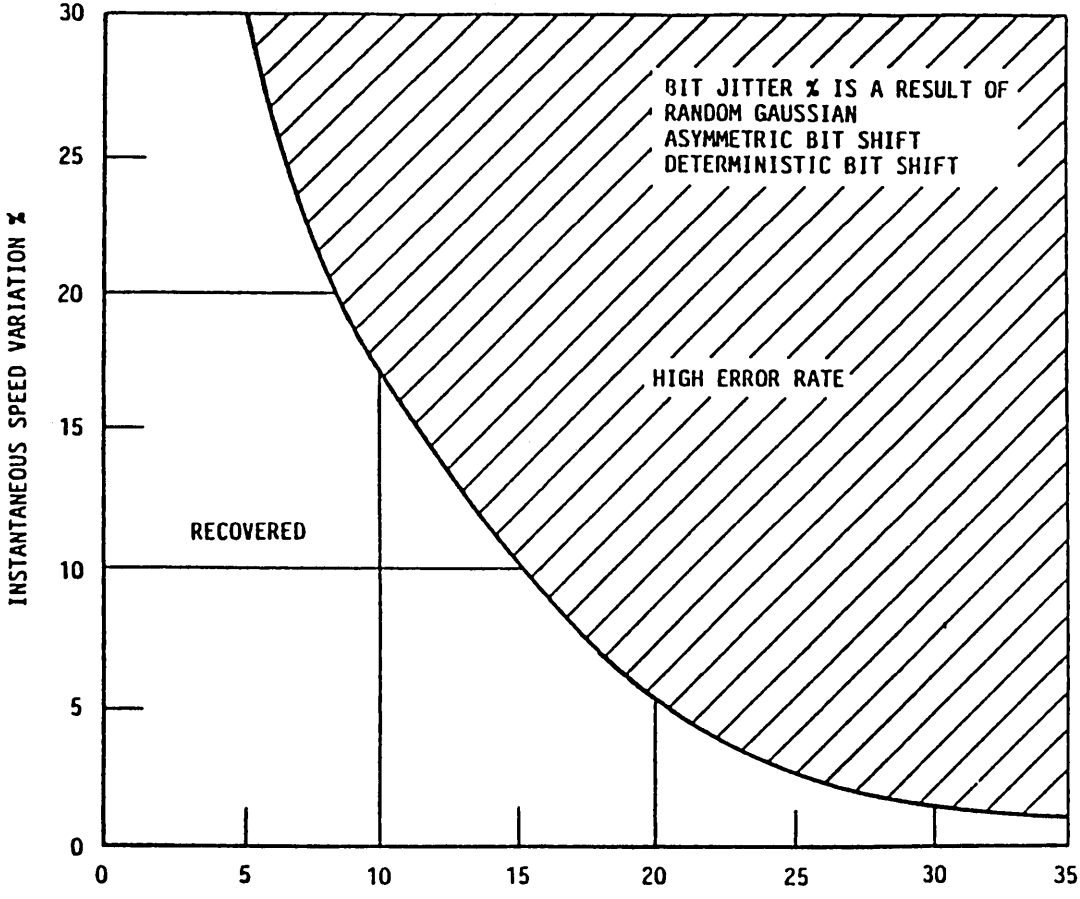


FIGURE 3. BIT JITTER %

CONNECTORS

The WD1036S-WX2 has two on-board connectors for interfacing to an IBM PC/AT/XT or compatible Host and one 1/4" QIC-36 cartridge tape drive.

P1 - The Host connects to this 62-pin card edge connector. Pins A1 through A31 are on the component side of the board and pins B1 through B31 are on the artwork side. The signals applied to this connector are described in Table 1.

J1 - The Tape Drive connects to this 50-pin connector via a cable of no more than 10 feet (3m) in length. All incoming signals are terminated with a 220 ohm resistor to +5V and 330 ohm resistor to ground. The signals applied to this connector are described in Table 2.

TABLE 1. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
A1		NOT CONNECTED		
A2 thru A9	D7 thru D0	DATA 7 thru DATA 0	I/O	8-Bit, tri-state, bi-directional bus for data and status communication between the WD1036S-WX2 and Host.
A10	I/O CH RDY	I/O CHANNEL READY	I	This tri-state signal adds one Wait State to allow for WD24C02 related commands.
A11	AEN	ADDRESS ENABLE	I	AEN is asserted by the Host DMA controller. Asserted, the DMA Controller has control of the address, control, and data buses. Only memory I/O operations can occur during assertion of AEN.
A12 thru A21		NOT CONNECTED		
A22 thru A31	A9 thru A0	ADDRESS BIT 9 thru ADDRESS BIT 0	I	Address bus.
B1	GND	GROUND		
B2	RST	RESET DRV	I	Initializes the WD1036S-WX2 during power-up or low line voltage condition.
B3	+5V	+5 VOLTS		
B4	IRQ2	INTERRUPT REQUEST LEVEL 2	O	The WD1036S-WX2 asserts IRQ2 to interrupt the Host upon the completion of a block operation. IRQ2 through IRQ7 is jumper selectable.
B5		NOT CONNECTED		
B6	DRQ2	DMA REQUEST CHANNEL 2	O	WD1036S-WX2 asserts DRQ2 to inform the DMA Controller that data is available for transfer in either direction. DRQ1,2 and 3 are jumper selectable.
B7 B8		NOT CONNECTED		
B9	+12V	+12 VOLTS		
B10	GND	GROUND		
B11 B12		NOT CONNECTED		

TABLE 1. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION (cont.)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
B13	$\overline{IOW}$	$\overline{I/O\ WRITE}$	I	The Host or DMA controller asserts $\overline{IOW}$ when a data or control byte is to be written to the WD1036S-WX2.
B14	$\overline{IOR}$	$\overline{I/O\ READ}$	I	The Host or DMA controller asserts $\overline{IOR}$ when a data or status byte is to be read from the WD1036S-WX2.
B15	$\overline{DACK3}$	$\overline{DMA\ ACKNOWLEDGE\ CHANNEL\ 3}$	I	The DMA Controller asserts $\overline{DACK3}$ in response to DRQ3 sent by the WD1036S-WX2. $\overline{DACK1}$, $\overline{2}$ and $\overline{3}$ are jumper selectable.
B16	DRQ3	DMA REQUEST CHANNEL 3	O	WD1036S-WX2 asserts DRQ3 to inform the DMA Controller that data is available for transfer in either direction. DRQ1,2 and 3 are jumper selectable.
B17	$\overline{DACK1}$	$\overline{DMA\ ACKNOWLEDGE\ CHANNEL\ 1}$	I	The DMA controller asserts $\overline{DACK1}$ in response to DRQ1 sent by the WD1036S-WX2. $\overline{DACK1}$,$\overline{2}$ and $\overline{3}$ are jumper selectable.
B18	DRQ1	DMA REQUEST CHANNEL 1	O	WD1036S-WX2 asserts DRQ1 to inform the DMA controller that data is available for transfer in either direction. DRQ1, 2 and 3 are jumper selectable.
B19		NOT CONNECTED		
B20	CLK	SYSTEM CLOCK	I	System clock with a period of 210 nsec and 33% duty cycle.
B21	IRQ7	INTERRUPT REQUEST LEVEL 7	O	The WD1036S-WX2 asserts IRQ7 to interrupt the Host upon the completion of a block. IRQ2 through IRQ7 is jumper selectable.
B22	IRQ6	INTERRUPT REQUEST LEVEL 6	O	The WD1036S-WX2 asserts IRQ6 to interrupt the Host upon the completion of a block. IRQ2 through IRQ7 is jumper selectable.
B23	IRQ5	INTERRUPT REQUEST LEVEL 5	O	The WD1036S-WX2 asserts IRQ5 to interrupt the Host upon the completion of a block. IRQ2 through IRQ7 is jumper selectable.
B24	IRQ4	INTERRUPT REQUEST LEVEL 4	O	The WD1036S-WX2 asserts IRQ4 to interrupt the Host upon the completion of a block. IRQ2 through IRQ7 is jumper selectable.
B25	IRQ3	INTERRUPT REQUEST LEVEL 3	O	The WD1036S-WX2 asserts IRQ3 to interrupt the Host upon the completion of a block. IRQ2 through IRQ7 is jumper selectable.
B26	$\overline{DACK2}$	$\overline{DMA\ ACKNOWLEDGE\ CHANNEL\ 2}$	I	The DMA controller asserts $\overline{DACK2}$ in response to DRQ1 sent by the WD1036S-WX2. $\overline{DACK1}$, $\overline{2}$ and $\overline{3}$ are jumper selectable.
B27 B28		NOT CONNECTED		
B29	+5V	+5VOLTS		
B30		NOT CONNECTED		
B31	GND	GROUND		

TABLE 2. DRIVE CONNECTOR (J1) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	2	$\overline{GO}$	$\overline{GO}$	O	Assertion starts tape motion. The state of $\overline{REV}$ determines the direction of tape motion.
3	4	$\overline{REV}$	$\overline{REVERSE}$	O	Assertion causes the tape drive to move tape in the reverse direction. De-assertion causes the tape drive to move tape in the forward direction. The WD1036S-WX2 must assert $\overline{GO}$ to enable $\overline{REV}$.
5	6	$\overline{TR3}$	$\overline{TRACK\ SELECT\ 3}$	O	Track Select bit 3. $\overline{TR3}$ through $\overline{TR0}$ is the binary coded track number used by the drive to select a designated track. (MSB).
7	8	$\overline{TR2}$	$\overline{TRACK\ SELECT\ 2}$	O	Track Select bit 2. $\overline{TR3}$ through $\overline{TR0}$ is the binary coded track number used by the drive to select a designated track.
9	10	$\overline{TR1}$	$\overline{TRACK\ SELECT\ 1}$	O	Track Select bit 1. $\overline{TR3}$ through $\overline{TR0}$ is the binary coded track number used by the drive to select a designated track.
11	12	$\overline{TR0}$	$\overline{TRACK\ SELECT\ 0}$	O	Track Select bit 0. $\overline{TR3}$ through $\overline{TR0}$ is the binary coded track number used by the drive to select a designated track. (LSB).
13	14	$\overline{RST}$	$\overline{RESET}$	O	$\overline{RST}$ is a minimum pulse of 13 usec. It starts the initialization routine and recalibration of the head to its reference position.
15	16		RESERVED		
17	18		RESERVED		
19	20		RESERVED		
21	22	$\overline{DSO}$	$\overline{DRIVE\ SELECT\ 0}$	O	When asserted $\overline{DSO}$ permits basic tape drive operations to proceed. $\overline{DSO}$ enables the transfer of control signals: RDP $\overline{CIN}$ $\overline{USF}$ $\overline{TCH}$ EEN. The drive acknowledges receipt of $\overline{DSO}$ by sending SLD.
23	24	$\overline{HC}$	$\overline{HIGH\ CURRENT}$	O	When asserted, enables operation with DC 600A tape cartridges. Refer to ANSC Project 671 Unrecorded Magnetic Tape Cartridge for Information Interchange, 0.250 inch (6.30mm)6400-10000 flux-reversals per inch (252-394 frpmm).
25	26	$\overline{RDP}$	$\overline{READ\ DATA\ PULSE}$	I	Serial-bit data read from tape to the WD1036S-WX2. RDP is present when data passes the read head and $\overline{DSO}$ is asserted.
27	28	$\overline{UTH}$	$\overline{UPPER\ TAPE\ POSITION\ HOLE}$	I	$\overline{UTH}$ and $\overline{LTH}$ encode information having to do with tape position as follows:
29	30	$\overline{LTH}$	$\overline{LOWER\ TAPE\ POSITION\ HOLE}$	I	$\overline{UTH}$ $\overline{LTH}$ MEANING 1 1 Beginning of Tape 0 1 End of Tape 1 0 Warning Zone 0 0 Recording Zone The Recording Zone is between the Load Point and the Early Warning hole if BOT or EOT has been detected since the last cartridge insertion ($\overline{CIN}$). If that is not the case 0 0 means the tape position is not known.

TABLE 2. DRIVE CONNECTOR (J1) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
31	32	$\overline{SLD}$	$\overline{DRIVE\ SELECTED}$	I	Tape drive acknowledgment to the WD1036S-WX2 of receipt of the $\overline{DSO}$.
33	34	$\overline{CIN}$	$\overline{CARTRIDGE\ IN}$	I	$\overline{CIN}$ is asserted when a tape cartridge is in place and the WD1036S-WX2 asserts $\overline{DSO}$ and GO.
35	36	$\overline{USF}$	$\overline{UNSAFE}$	I	The drive asserts $\overline{USF}$ when the File Protect Plug is not in the safe position on the cartridge and the WD1036S-WX2 asserts $\overline{DSO}$. This state permits data to be written and erased.
37	38	$\overline{TCH}$	$\overline{TACH\ PULSE}$	I	$\overline{TCH}$ is present while tape is moving. It is not looked at or used by the WD1036S-WX2.
39	40	WDA -	WRITE DATA -	O	Data to be written on tape, enabled while $\overline{WEN}$ is asserted. System is optimized to record GCR data at a nominal density of 10,000 frpi.
41	42	WDA +	WRITE DATA +	O	The inverse of WDA-
43	44	$\overline{THD}$	$\overline{THRESHOLD}$	O	Sets a percentage-qualifying voltage threshold for Read Data. Eliminates data of marginal quality read from tape.
45	46	$\overline{HSD}$	$\overline{HIGH\ SPEED}$	O	Asserted = 90-ips tape speed. Utilities supplied by Western Digital always asserts $\overline{HSD}$.
47	48	$\overline{WEN}$	$\overline{WRITE\ ENABLE}$	O	When asserted, enables drive to write data.
49	50	$\overline{EEN}$	$\overline{ERASE\ ENABLE}$	O	Tape is erased the full width of the tape when the WD1036S-WX2 asserts $\overline{DSO}$ and $\overline{EEN}$.

COMMAND SUMMARY

The commands associated with the WD1036S-WX2 fall into one of two categories. Hardware commands, those low level commands that communicate directly with the WD1036S-WX2 and are implemented by the WD1100-18 and WD24C02, and high level software commands, those commands within the application level module that interface between the application program and Core.

HARDWARE COMMANDS

There are a total of 16 commands recognized by the WD1036S-WX2. Ten of these commands are the direct responsibility of the WD1100-18 and six are performed by the WD24C02. The WD1036S-WX2 occupies sixteen I/O addresses, O through F Hex. The base address is jumper selectable at the time of installation to start at one of sixteen locations from 300 Hex through 3F0 Hex.

Following is a brief summary of the hardware commands. For a more indepth description, refer to the OEM manual, DOC. number 79–000037.

TABLE 3. HARDWARE COMMAND SUMMARY

OFFSET	I/O	COMMAND NAME	DESCRIPTION
0	IOR	READ STATUS	Returns a status byte representing the state of the following signals: Bit 7 = RGAP Bit 3 = SLD Bit 6 = TCH Bit 2 = LTH Bit 5 = USF Bit 1 = UTH Bit 4 = CIN Bit 0 = INT
4	IOR	START DMA PIPELINE	Two DRQ $\overline{\text{DACK}}$ handshakes are completed. This writes two data bytes into a DMA buffer in the WD1100-18. A Write Tape command can now be started.
8	IOR	CONTROLLER RESET	Resets all WD1100-18 internal logic, both Drive Control registers and de-asserts $\overline{\text{MR}}$ to the WD24C02.
C	IOR	READ WD24C02 STATUS REGISTER	Returns to the Host the state of the following signals: Bit 7 = CBK Bit 2 = FMD Bit 6-4 not used Bit 1 = WGP Bit 3 = RGP Bit 0 = CER
F	IOR	READ BLOCK ADDRESS	Returns to the Host the block address of the last data block read. The block address is four bytes in length. Therefore, four consecutive Read Block Address commands must be issued. The MSB is returned first.
0	IOW	SET CONTROL FLIP-FLOPS	This command establishes the state of the DMA enable and Repeat Flip/Flops. Bit 0 = Set DMA Enable Bit 1 = Set Repeat Write Data Command. Bit 2 = Reset Repeat F/F
4	IOW	SET DRIVE CONTROL REGISTER 0	Drive Control Register 0 controls the following signals: Bit 7 not used Bit 3 = Drive Select Bit 6 = Read Gate Enable Bit 2 = Threshold Bit 5 = Write Enable Bit 1 = Reverse Bit 4 = Erase Enable Bit 0 = Go
8	IOW	SET DRIVE CONTROL REGISTER 1	Drive Control Register 1 controls the following signals: Bit 7 not used Bit 3 = Track Select 3 Bit 6 = Reset Drive Bit 2 = Track Select 2 Bit 5 = High Speed Bit 1 = Track Select 1 Bit 4 = High Current Bit 0 = Track Select 0
C	IOW	LOAD COMMAND REGISTER	A byte representing one of six possible commands is written into the Command Register in the WD24C02. Bit 7 = Abort Bit 2 = Read Scan Bit 6 = Write File Mark Bit 1 = Write Data Bit 5, 4 not used Bit 0 = Read Data Bit 3 = Write Gap
F	IOW	WRITE BLOCK ADDRESS REGISTER	The Block Address Register is four bytes in length, therefore this command must be issued consecutively four times. The MSB is written first.

SOFTWARE COMMANDS

The commands that comprise the Application-to-Core Module can be divided into four categories: Tape Access commands, Disk Access commands, Host Buffer Manager commands and Mode commands.

Following is a brief summary of the Application-to-Core command set. For a more indepth description, refer to the OEM manual, DOC. number 79-000037.

Command Format

OP. CODE	OPTION	
PARAMETER 2		BYTE 3 - 4
PARAMETER 3		BYTE 5 - 6

Status Format

Returned upon completion of a command

OP. CODE	STATUS	
STATUS 2		BYTE 3 - 4
STATUS 3		BYTE 5 - 6

TABLE 4. SOFTWARE COMMAND SUMMARY

COMMAND	OP CODE	OPTION	PARAMETERS
Tape Commands			
Retension	01	00 Do not erase 01 Erase	— — — —
Read Tape	02	00 Start reading at the beginning of the tape. 01 Start reading following the last block read by a Read Command or found with a Find Command	— — — —
Write Tape	03	00 Start writing at the beginning of the present track. 01 Start writing at the end of recorded data.	— — — —
Find Tape Block	04	00 Find Data Block "n". 01 Find Control Block "n". 02 Find File Mark Block "n". 03 Find Block Address "addr". 04 Find beginning of track "n".	n = Parm 2 n = Parm 2 n = Parm 2 addr = Parm 2 and 3 n = Parm 2
Stop Tape	05	00 No options	— —
Disk Commands			
Set Disk Mode	06	00 Disk Image 01 File Image	— — — —
Read Disk	07	00 No Options	— —
Write Disk	08	00 No Options	— —

TABLE 4. SOFTWARE COMMAND SUMMARY (cont.)

COMMAND	OP CODE	OPTION	PARAMETERS
Host Buffer Commands			
Read Buffer	09	00 Read previous page	— —
		01 Read current page	— —
		02 Read next page	— —
		03 Skip one page	— —
		04 Skip to next data block	— —
		05 Skip to next control block	— —
		06 Skip to next File Mark	— —
Write Buffer	0A	00 Write a data block	— —
		01 Write a control block	— —
		02 Write a File Mark block	— —
	0B	Reserved	
Mode Commands			
Write Configuration	0C	00 Miscellaneous Status. 01 Maximum number of tracks. 02 Number of pages in buffer. 03 Seg. of buffers' first page 04 Offset of first page. 0E Write CRC error counter. 0F Pointer to local buffer. 10 Pointer to word containing expected tape block address 11 Pointer to word containing last tape block address. 12 Pointer to word containing current tape track. 13 Reposition counter.	Data to be written in Parm 2
Read Configuration	0D	00 Miscellaneous Status. 01 Maximum number of tracks. 02 Number of pages in buffer. 03 Seg. of buffers' first page 04 Offset of first page. 0D Read CRC error counter. 0F Pointer to local buffer. 10 Pointer to word containing expected tape block address 11 Pointer to word containing last tape block address. 12 Pointer to word containing current tape track. 13 Reposition counter.	Data read is returned in Stat 2
Initialize	0E	00 All (options 01 - 05) 01 Tape portion 02 Core variables 03 Buffer Manager 04 Cartridge status 05 Controller reset	

WD8206 Error Detection and Correction Unit

FEATURES

- DETECTS AND CORRECTS ALL SINGLE BIT ERRORS
- DETECTS ALL DOUBLE BIT AND MOST MULTIPLE BIT ERRORS
- 52 NSEC MAXIMUM FOR DETECTION; 67 NSEC MAXIMUM FOR CORRECTION (16-BIT SYSTEM)
- EXPANDABLE TO HANDLE 80-BIT MEMORIES
- SYNDROME INPUT AND OUTPUT BUSSES – NO TIMING STROBES REQUIRED
- SUPPORTS READS WITH AND WITHOUT CORRECTION, WRITES, PARTIAL (BYTE) WRITES, AND READ-MODIFY-WRITES
- HMOS TECHNOLOGY FOR LOW POWER
- 68-PIN LEADLESS JEDEC PACKAGE
- SINGLE +5V SUPPLY

GENERAL DESCRIPTION

The HMOS 8206 Error Detection and Correction Unit is a high-speed device that provides error detection and correction for memory systems (static and dynamic) requiring high reliability and performance. Each WD8206 handles 8 or 16 data bits and up to 8 check bits. WD8206's can be cascaded to provide correction and detection for up to 80-bits of data. Other WD8206 features include the ability to handle byte writes, memory initialization, and error logging.

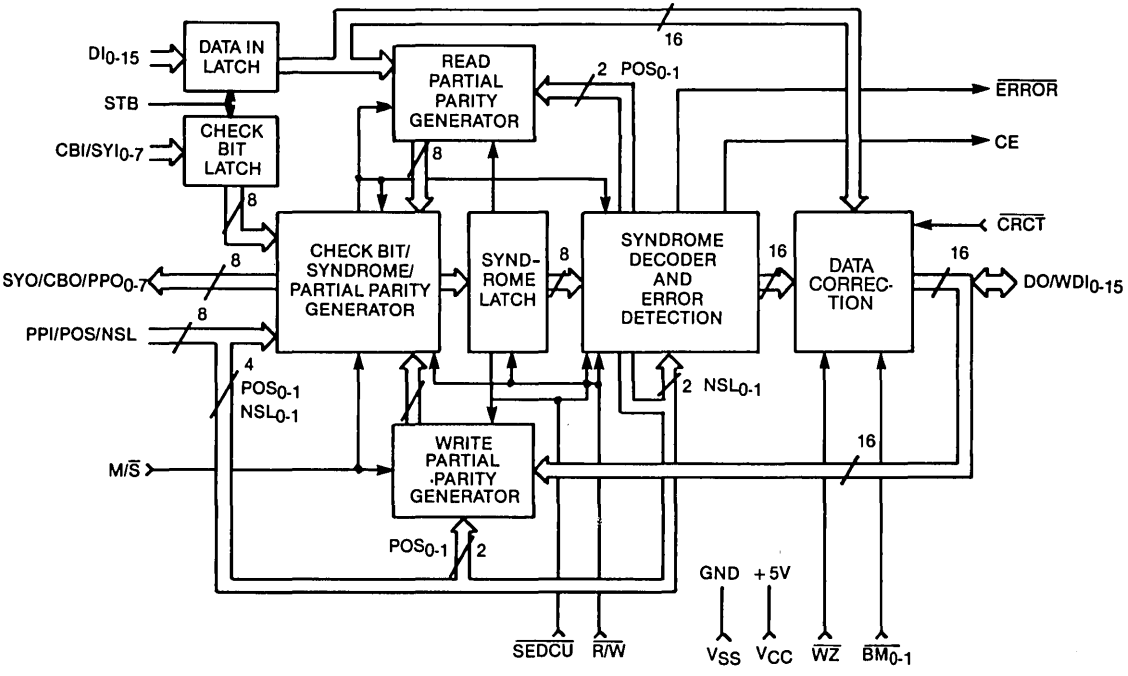


FIGURE 1. WD8206 BLOCK DIAGRAM

TABLE 1. PIN DESCRIPTION

PIN NUMBER	SYMBOL	I/O	NAME AND FUNCTION
1,68-61, 59-53	DI_{0-15}	I	**Data In:** These inputs accept a 16-bit word from RAM for error detection and/or correction.
5 6 7 8 9 10 11 12	CBI/SYI_0 CBI/SYI_1 CBI/SYI_2 CBI/SYI_3 CBI/SYI_4 CBI/SYI_5 CBI/SYI_6 CBI/SYI_7	I I I I I I I I	**Check Bits In/Syndrome In:** In a single WD8206 system, or in the master in a multi-WD8206 system, these inputs accept the check bits (5 to 8) from the RAM. In a single WD8206 16 bit system, CBI_{0-5} are used. In slave WD8206's, these inputs accept the syndrome from the master.
51 50 49 48 47 46 45 44 42 41 40 39 38 37 36 35	DO/WDI_0 DO/WDI_1 DO/WDI_2 DO/WDI_3 DO/WDI_4 DO/WDI_5 DO/WDI_6 DO/WDI_7 DO/WDI_8 DO/WDI_9 DO/WDI_{10} DO/WDI_{11} DO/WDI_{12} DO/WDI_{13} DO/WDI_{14} DO/WDI_{15}	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	**Data Out/Write Data In:** In a read cycle, data accepted by DI_{0-15} appears at these outputs corrected if CRCT is low, or uncorrected if CRCT is high. The IBM inputs must be high to enable the output buffers during the read cycle. In a write cycle, data to be written into the RAM is accepted by these inputs for computing the write check bits. In a partial-write cycle, the byte not to be modified appears at either DO_{0-7} if BM_0 is high, or DO_{8-15} if BM_1 is high, for writing to the RAM. When WZ is active, it causes the WD8206 to output all zeros at DO_{0-15}, with the proper write check bits on CBO.
23 24 25 27 28 29 30 31	$SYO/CBO/PPO_0$ $SYO/CBO/PPO_1$ $SYO/CBO/PPO_2$ $SYO/CBO/PPO_3$ $SYO/CBO/PPO_4$ $SYO/CBO/PPO_5$ $SYO/CBO/PPO_6$ $SYO/CBO/PPO_7$	O O O O O O O O	**Syndrome Out/Check Bits Out/Partial Parity Out:** In a single WD8206 system, or in the master in a multi-WD8206 system, the syndrome appears at these outputs during a read. During a write, the write check bits appear. In slave WD8206's, the partial parity bits used by the master appear at these outputs. The syndrome is latched (during read-modify-writes) by R/W going low.
13 14	PPI_0/POS_0 PPI_1/POS_1	I I	**Partial Parity In/Position:** In the master in the multi-WD8206 system, these inputs accept partial parity bits O and 1 from the slaves. In a slave WD8206, these inputs inform it of its position within the system (1 to 4). Not used in a single WD8206 system.
15 16	PPI_2/NSL_0 PPI_3/NSL_1	I I	**Partial Parity In/Number of Slaves:** In the master in a multi-WD8206 system, these inputs accept partial parity bits 2 and 3 from the slaves. In a multi-WD8206 system, these inputs are used in slave number 1 to tell it the total number of slaves in the system (1 to 4). Not used in other slaves or in a single WD8206 system.
17	PPI_4/CE	I/O	**Partial Parity In/Correctable Error:** In the master in a multi-WD8206 system, this pin accepts partial parity bit 4. In slave number 1 only, or in a single WD8206 system, this pin outputs the correctable error flag. CE is latched by R/W going low. Not used in other slaves.
18 19 20	PPI_5 PPI_6 PPI_7	I I I	**Partial Parity In:** In the master in a multi-WD8206 system, these pins accept partial parity bits 5 to 7. The number of partial parity bits equals the number of check bits. Not used in single WD8206 systems or in slaves.

TABLE 1. PIN DESCRIPTION (CONTINUED)

PIN NUMBER	SYMBOL	I/O	NAME AND FUNCTION
22	ERROR	O	**Error:** This pin outputs the error flag in a single WD8206 system or in the master of a multi-WD8206 system. It is latched by R/W going low. Not used in slaves.
52	CRCT	I	**Correct:** When low, this pin causes data correction during a read or read-modify-write cycle. When high, it causes error correction to be disabled, although error checking is still enabled.
2	STB	I	**Strobe:** STB is an input control used to strobe data at the DI inputs and check-bits at the CBI/SYI inputs. The signal is active high to admit the inputs. The signals are latched by the high-to-low transition of STB.
33 32	BM_0 BM_1	I I	**Byte Marks:** When high, the Data Out pins are enabled for a read cycle. When low, the Data Out buffers are tristated for a write cycle. BM_0 controls DO_{0-7}, while BM_1 controls DO_{8-15}. In partial (bytes) writes, the byte mark input is low for the new byte to be written.
21	R/W	I	**Read/Write:** When high, this pin causes the WD8206 to perform detection and correction (if CRCT is low). When low, it causes the WD8206 to generate check bits. On the high-to-low transition, the syndrome is latched internally for read-modify-write cycles.
34	WZ	I	**Write Zero:** When low, this input overrides the BM_{0-1} and R/W inputs to cause the WD8206 to output all zeros at DO_{0-15} with the corresponding check bits at CBO_{0-7}. Used for memory initialization.
4	M/S	I	**Master/Slave:** Input tells the WD8206 whether it is a master (high) or a slave (low).
3	SEDCU	I	**Single EDC Unit:** Input tells the master whether it is operating as a single WD8206 (low) or as the master in a multi-WD8206 system (high). Not used in slaves.
60	V_{CC}	I	**Power Supply:** +5V
26	V_{SS}	I	**Logic Ground**
43	V_{SS}	I	**Output Driver Ground**

FUNCTIONAL DESCRIPTION

The WD8206 Error Detection and Correction Unit provides greater memory system reliability through its ability to detect and correct memory errors. It is a single chip device that can detect and correct all single bit errors and detect all double bit and some higher multiple bit errors. Some other odd multiple bit errors (e.g., 5 bits in error) are interpreted as single bit errors, and the CE flag is raised. While some even multiple bit errors (e.g., 4 bits in eror) are interpreted as no error, most are detected as double bit errors. This error handling is a function of the number of check bits used by the WD8206 (see Figure 2) and the specific Hamming code used. Errors in check bits are not distinguished from errors in a word.

A single WD8206 handles 8 or 16 bits of data, and up to 5 WD8206's can be cascaded in order to handle data paths for 80 bits. For a single WD8206 8-bit system, the DI_{8-15}, DO/WDI_{8-15} and BM_1 inputs are grounded. See the Multi-Chip systems section for information on 24-80-bit systems.

The WD8206 has a "flow through" architecture. It supports two kinds of error correction architecture: 1) Flow-through, or correct-always; and 2) Parallel, or check-only. There are two separate 16-pin busses, one to accept data from the RAM (DI) and the other to deliver corrected data to the system bus (DO/WDI). The logic is entirely combinatorial during a read cycle.

This is in contrast to an architecture with only one bus, with bi-directional bus drivers that must first read the data and then be turned around to output the corrected data. The latter architecture typically requires additional hardware (latches and/or transceivers) and may be slower in a system due to timing skews of control signals.

DATA WORD BITS	CHECK BITS
8	5
16	6
24	6
32	7
40	7
48	8
56	8
64	8
72	8
80	8

FIGURE 2. NUMBER OF CHECK BITS USED BY WD8206

READ CYCLE

With the R/W pin high, data is received from the RAM outputs into the DI pins where it is optionally latched by the STB signal. Check bits are generated from the data bits and compared to the check bits read from the RAM into the CBI pins. If an error is detected, the ERROR flag is activated and the correctable error flag (CE) is used to inform the system whether the error is correctable or not. With the BM inputs high, the word appears corrected at the DO pins if the error is correctable, or unmodified if the error was uncorrectable.

If more than one WD8206 is being used, then the check bits are read by the master. The slaves generate a partial parity output (PPO) and pass it to the master. The master WD8206 then generates and returns the syndrome to the slaves (SYO) for correction of the data.

The WD8206 may alternatively be used in a "check-only" mode with the CRCT pin left high. With the correction facility turned off, the propagation delay from memory outputs to WD8206 outputs is significantly shortened. In this mode, the WD8206 issues an ERROR flag to the CPU, which can then perform one of several options: lengthen the current cycle for correction, restart the instruction, perform a diagnostic routine, etc.

A syndrome word, five to eight bits in length and containing all necessary information about the existence and location of an error, is made available to the system at the $SYO_{0\text{-}7}$ pins. Error logging may be accomplished by latching the syndrome and the memory address of the word in error.

WRITE CYCLE

For a full write, in which an entire word is written to memory, the data is written directly to the RAM, bypassing the WD8206. The same data enters the WD8206 through the WDI pins where check bits are generated. The Byte Mark inputs must be low to tri-state the DO drivers. The check bits, 5 to 8 in number, are then written to the RAM through the CBO pins for storage along with the data word. In a multi-chip system, the master writes the check bits using partial parity information from the slaves.

In a partial write, part of the data word is overwritten and part is retained in memory. This is accomplished by performing a read-modify-write cycle. The complete old word is read into the WD8206 and corrected, with the syndrome internally latched by R/W going low. Only that part of the word not to be modified is output onto the DO pins, as controlled by the Byte Mark inputs. That portion of the word to be overwritten is supplied by the system bus. The WD8206 then calculates check bits for the new word, using the byte from the previous read and the new byte from the system bus, and writes them to the memory.

READ-MODIFY-WRITE CYCLES

Upon detection of an error, the WD8206 may be used to correct the bit in error in memory. This reduces the probability of getting multiple-bit errors in subsequent read cycles. This correction is handled by executing read-modify-write cycles.

The read-modify-write cycle is controlled by the R/W input. After (during) the read cycle, the system dynamic RAM controller or CPU examines the WD8206 ERROR and CE outputs to determine if a correctable error occurred. If it did, the dynamic RAM controller or CPU forces R/W low, telling the WD8206 to latch the generated syndrome and drive the corrected check bits onto the CBO outputs. The corrected data is available on the DO pins. The DRAM controller then writes the corrected data and corresponding check bits into memory.

The WD8206 may be used to perform read-modify-writes in one or two RAM cycles. If it is done in two cycles, the WD8206 latches are used to hold the data and check bits from the read cycle to be used in the following write cycle. The WD8207 Advanced Dynamic RAM controller allows read-modify-write cycles in one memory cycle. See the System Environment section.

INITIALIZATION

A memory system operating with ECC requires some form of initialization at system power-up in order to set valid data and check bit information in memory. The WD8206 supports memory initialization by the write zero function. By activating the WZ pin, the WD8206 will write a data pattern of zeros and the associated check bits in the current write cycle. By thus writing to all memory at power-up, a controller can set memory to valid data and check bits. Massive memory failure, as signified by both data and check bits all ones or zeros, will be detected as an uncorrectable error.

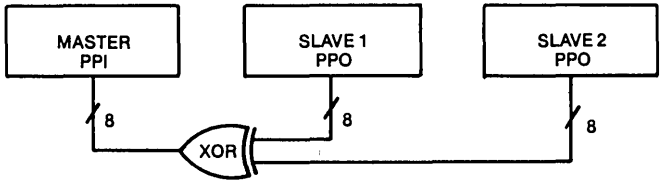
MULTI-CHIP SYSTEMS

A single WD8206 handles 8 or 16 bits of data and 5 or 6 check bits, respectively. Up to 5 WD8206's can be cascaded for 80-bit memories with 8 check bits.

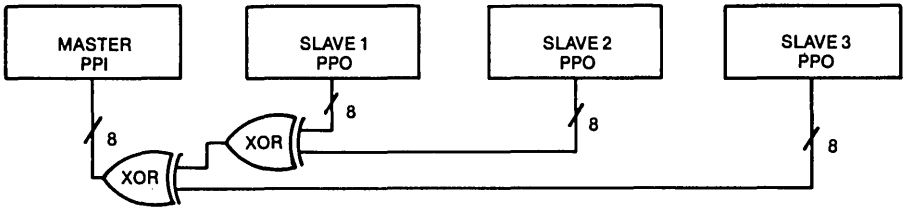
When cascaded, one WD8206 operates as a master, and all others as slaves. As an example, during a read cycle in a 32-bit system with one master and one slave, the slave calculates parity on its portion of the word – "partial parity" – and presents it to the master through the PPO pins. The master combines the partial parity from the slave with the parity it calculated from its own portion of the word to generate a syndrome. The syndrome is then returned by the master to the slave for error correction. In systems with more than one slave, the above description continues to apply, except that the partial parity outputs of the slaves must be XORed externally. Figure 3 shows the necessary external logic for multi-chip systems. Write and read-modify-write cycles are carried out analogously. See the System Operation section for multi-chip wiring diagrams.

There are several pins used to define whether the WD8206 will operate as a master or a slave. Tables 2 and 3 illustrate how these pins are tied.

3a. 48-Bit System



3b. 64-Bit System



3c. 80-Bit System

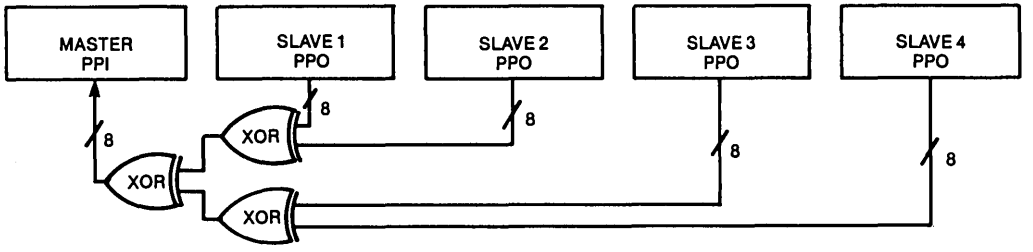


FIGURE 3. EXTERNAL LOGIC FOR MULTI-CHIP SYSTEMS

TABLE 2. MASTER/SLAVE PIN ASSIGNMENTS

PIN NO.	PIN NAME	MASTER	SLAVE1	SLAVE2	SLAVE3	SLAVE4
4	M/S	+5V	Gnd	Gnd	Gnd	Gnd
3	SEDCU	+5V	+5V	+5V	+5V	+5V
13	PPI_0/POS_0	PPI	Gnd	+5V	Gnd	+5V
14	PPI_1/POS_1	PPI	Gnd	Gnd	+5V	+5V
15	PPI_2/NSL_0	PPI	*	+5V	+5V	+5V
16	PPI_3/NSL_1	PPI	*	+5V	+5V	+5V

*See Table 3.

NOTE:

Pins 13, 14, 15, and 16 have internal pull-up resistors and may be left as N.C. where specified as connecting to +5V.

TABLE 3. NSL PIN ASSIGNMENTS FOR SLAVE 1

	NUMBER OF SLAVES			
PIN	1	2	3	4
PPI_2/NSL_0	Gnd	+5V	Gnd	+5V
PPI_3/NSL_1	Gnd	Gnd	+5V	+5V

The timing specifications for multi-chip systems must be calculated to take account of the external XOR gating in 3,4, and 5-chip systems. Let tXOR be the delay for a single external TTL XOR gate. Then the following equations show how to calculate the relevant timing parameters for 2-chip (n = 0), 3- chip (n = 1), 4-chip (n = 2), and 5-chip (n = 2) systems:

Data-in to corrected data-out (read cycle) =
TDVSV + TPVSV + TSVQV + ntXOR

Data-in to error flag (read cycle) =
TDVSV + TPVEV + ntXOR

Data-in to correctable error flag (read cycle) =
TDVSV + TPVSV + TSVCV + ntXOR

Write data to check-bits valid (read-mod-write cycle) =
TQVQV + TPVSV + ntXOR

Data-in to check-bits valid (read-mod-write cycle) =
TDVSV + TPVSV + TSVQV + TQVQV + TPVSV + 2ntXOR

Data-in to check-bits valid (non-correcting read-modify-write cycle) =
TDVQU + TQVQV + TPVSV + ntXOR

HAMMING CODE

The WD8206 uses a modified Hamming code which was optimized for multi-chip EDCU systems. The code is such that partial parity is computed by all WD8206's in parallel. No WD8206 requires more time for propagation through logic levels than any other one, and hence no one device becomes a bottleneck in the parity operation. However, one or two levels of external TTL XOR gates are required in systems with three to five chips. The code appears in Table 4. The check bits are derived from the table by XORing or XNORing together the bits indicated by 'X's in each row corresponding to a check bit. For example, check bit 0 in the MASTER for data word 1000110101101011 will be "0." It should be noted that the WD8206 will detect the gross error condition of all lows or all highs.

Error correction is accomplished by identifying the bad bit and inverting it. Table 4 can also be used as an error syndrome table by replacing the 'X's with '1's. Each column then represents a different syndrome word, and by locating the column corresponding to a particular syndrome the bit to be corrected may be identified. If the syndrome cannot be located, then the error cannot be corrected. For example, if the syndrome word is 00110111, the bit to be corrected is bit 5 in the slave one data word (bit 21).

The syndrome decoding is also summarized in Table 5, which can be used for error logging. By finding the appropriate syndrome word (starting with bit zero, the least significant bit), the result is either: 1) no error; 2) an identified (correctable) single bit error; 3) a double bit error; or 4) a multi-bit uncorrectable error.

TABLE 4. MODIFIED HAMMING CODE CHECK BIT GENERATION

Check bits are generated by XOR'ing (except for the CB0 and CB1 data bits, which are XNOR'ed in Master) the data bits in the rows corresponding to the check bits. Note there are 6 check bits in a 16-bit system, 7 in a 32-bit system, and 8 in 48-or-more-bit systems.

BYTE NUMBER	0								1								OPERATION
BIT NUMBER	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
CB0 =	X	X	—	X	—	X	X	—	X	—	—	X	—	X	—	—	XNOR
CB1 =	X	—	X	—	—	X	—	X	—	X	—	X	X	—	X	—	XNOR
CHECK CB2 =	—	X	X	—	X	—	X	X	—	—	X	—	X	—	—	X	XOR
CB3 =	X	X	X	X	X	—	—	—	X	X	X	—	—	—	—	—	XOR
BITS CB4 =	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	XOR
CB5 =	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
CB6 =	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
CB7 =	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
DATA BITS	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	
	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	

16 BIT OR MASTER

	2								3								OPERATION
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
	—	X	X	X	—	X	X	—	—	X	X	—	—	X	—	—	XOR
	X	X	X	—	—	X	—	X	X	X	—	—	—	—	—	X	XOR
	—	X	X	X	—	X	X	X	—	—	X	X	—	—	—	—	XOR
	X	X	—	—	X	—	X	X	X	—	—	X	X	—	—	—	XOR
	X	X	—	—	X	X	X	X	—	—	—	—	X	—	X	—	XOR
	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	XOR
	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3	
	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	

SLAVE #1

BYTE NUMBER	4								5								6								7								8								9								OPERATION
BIT NUMBER	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
CB0 =	X	X	—	X	—	X	X	—	X	—	—	X	—	X	—	—	X	—	X	X	—	—	X	—	—	X	X	X	—	X	X	—	—	X	X	—	—	X	—	—	XOR
CB1 =	X	—	X	—	—	X	—	X	—	X	—	X	X	—	X	—	X	X	—	—	—	X	—	—	—	X	X	—	X	X	X	—	—	X	X	—	X	X	X	—	—	X	X	—	—	—	—	—	XOR
CHECK CB2 =	—	X	X	—	X	—	X	X	—	—	X	—	X	—	—	X	—	X	X	X	—	X	X	—	X	—	—	X	—	X	X	—	—	X	X	—	—	X	—	X	—	X	X	—	X	—	—	X	XOR
CB3 =	X	X	X	X	X	—	—	—	X	X	X	—	—	—	—	—	X	—	—	X	X	—	—	—	—	X	X	X	—	—	—	X	X	X	—	—	X	X	—	—	X	X	—	—	X	—	—	—	XOR
BITS CB4 =	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	—	—	—	—	—	X	X	X	—	X	X	—	—	—	—	X	—	X	X	—	—	—	—	X	X	X	—	—	X	—	—	—	XOR
CB5 =	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	X	—	X	X	X	X	—	X	—	—	—	X	—	—	—	X	XOR
CB6 =	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	—	—	X	X	X	—	—	—	—	X	—	X	—	—	XOR
CB7 =	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
DATA BITS	3	3	3	3	3	3	3	3	4	4	4	4	4	4	4	4	4	4	5	5	5	5	5	5	5	5	5	5	6	6	6	6	6	6	6	7	7	7	7	7	7	7	7	7	7	7	7	7	
	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	

SLAVE #2 | SLAVE #3 | SLAVE #4

TABLE 5. SYNDROME DECODING

Syndrome Bits				0 0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				1 0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				2 0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
7	6	5	4	3 0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	N	CB0	CB1	D	CB2	D	D	18	CB3	D	D	0	D	1	2	D
0	0	0	1	CB4	D	D	5	D	6	7	D	D	3	16	D	4	D	D	17
0	0	1	0	CB5	D	D	11	D	19	12	D	D	8	9	D	10	D	D	67
0	0	1	1	D	13	14	D	15	D	D	21	20	D	D	66	D	22	23	D
0	1	0	0	CB6	D	D	25	D	26	49	D	D	48	24	D	27	D	D	50
0	1	0	1	D	52	55	D	51	D	D	70	28	D	D	65	D	53	54	D
0	1	1	0	D	29	31	D	64	D	D	69	68	D	D	32	D	33	34	D
0	1	1	1	30	D	D	37	D	38	39	D	D	35	71	D	36	D	D	U
1	0	0	0	CB7	D	D	43	D	77	44	D	D	40	41	D	42	D	D	U
1	0	0	1	D	45	46	D	47	D	D	74	72	D	D	U	D	73	U	D
1	0	1	0	D	59	75	D	79	D	D	58	60	D	D	56	D	U	57	D
1	0	1	1	63	D	D	62	D	U	U	D	D	U	U	D	61	D	D	U
1	1	0	0	D	U	U	D	U	D	D	U	76	D	D	U	D	U	U	D
1	1	0	1	78	D	D	U	D	U	U	D	D	U	U	D	U	D	D	U
1	1	1	0	U	D	D	U	D	U	U	D	D	U	U	D	U	D	D	U
1	1	1	1	D	U	U	D	U	D	D	U	U	D	D	U	D	U	U	D

N = No Error
CBX = Error in Check Bit X
X = Error in Data Bit X
D = Double Bit Error
U = Uncorrectable Multi-Bit Error

SYSTEM ENVIRONMENT

The WD8206 interface to a typical 32-bit memory system is illustrated in Figure 4. For larger systems, the partial parity bits from slaves two to four must be XOR'ed externally, which calls for one level of XOR gating for three WD8206's and two levels for four or five WD8206's.

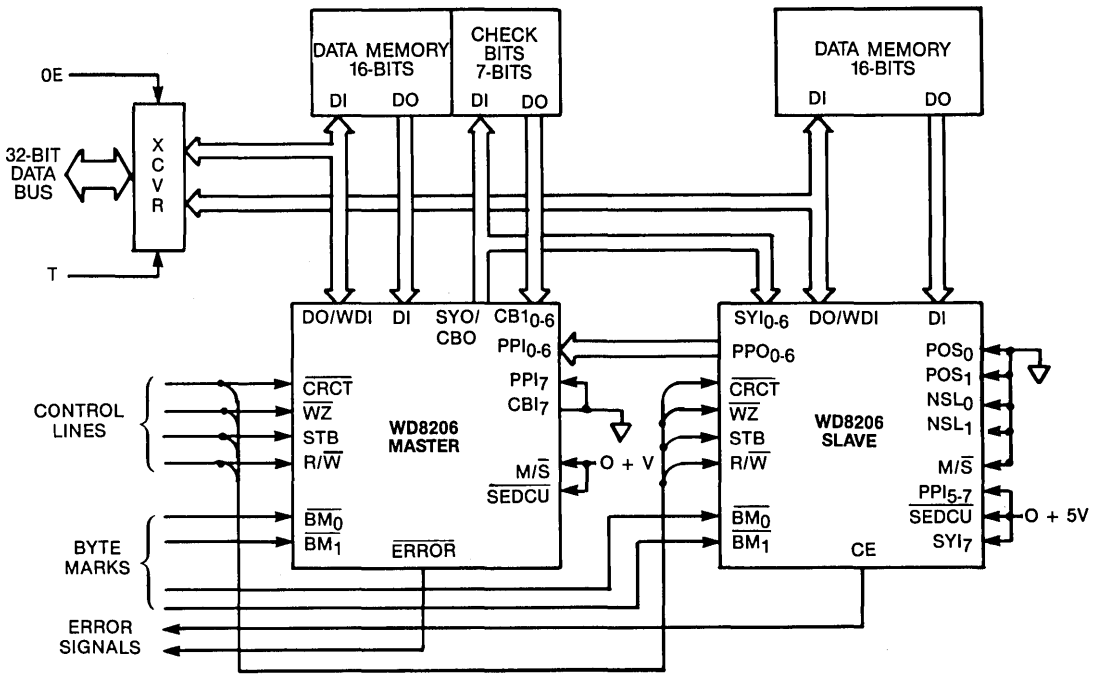


FIGURE 4. 32-BIT WD8206 SYSTEM INTERFACE

The WD8206 is designed for direct connection to the WD8207 Advanced Dynamic RAM Controller. The WD8207 has the ability to perform dual port memory control and Figure 5 illustrates a highly integrated dual port RAM implementation using the WD8206 and WD8207. The WD8206/WD8207 combination permits such features as automatic scrubbing (correcting errors in memory during refresh), extending RAS and CAS timings for Read-Modify-Writes in single memory cycles, and automatic memory initialization upon reset. Together, these two chips provide a complete dual-port, error-corrected dynamic RAM subsystem.

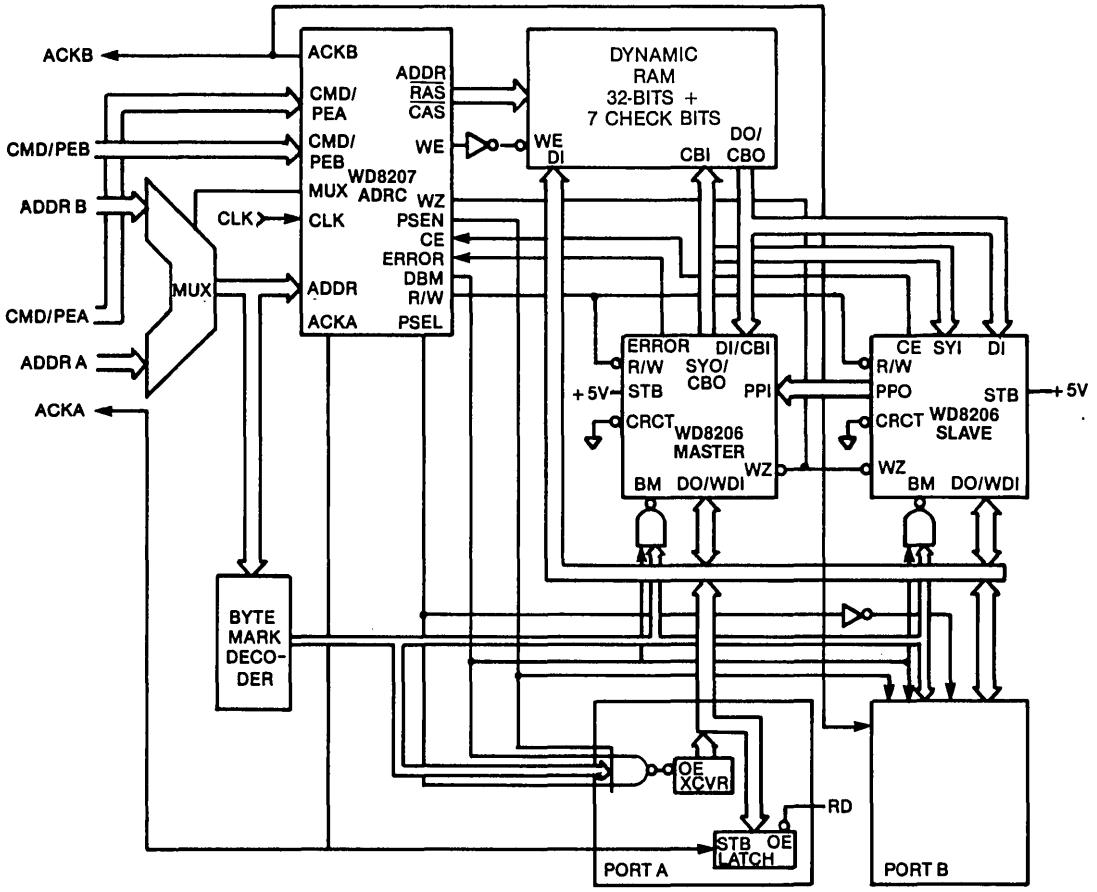


FIGURE 5. DUAL PORT RAM SUBSYSTEM WITH WD8206/WD8207 (32-BIT BUS)

MEMORY BOARD TESTING

The WD8206 lends itself to straightforward memory board testing with a minimum of hardware overhead. The following is a description of four common test modes and their implementation.

Mode 0 –Read and write with error correction.
Implementation: This mode is the normal WD8206 operating mode.

Mode 1 –Read and write data with error correction disabled to allow test of data memory.
Implementation: This mode is performed with CRCT deactivated.

Mode 2 –Read and write check bits with error correction disabled to allow test of check bits memory.
Implementation: Any pattern may be written into the check bits memory by judiciously choosing the proper data word to generate the desired check bits, through the use of the WD8206 Hamming code. To read out the check bits, it is first necessary to fill the data memory with all zeroes, which may be done by activating WZ and incrementing memory addresses with WE to the check bits memory held inactive, and then performing ordinary reads. The check bits will then appear directly at the SYO outputs, with bits CB0 and CB1 inverted.

Mode 3 –Write data, without altering or writing check bits, to allow the storage of bit combinations to cause error correction and detection.
Implementation: This mode is implemented by writing the desired word to memory with WE to the check bits array held inactive.

PACKAGE

The WD8206 is packaged in a 68-pin, leadless JEDEC type A hermetic chip carrier. Figure 6 illustrates the package, and Figure 7 is the pinout.

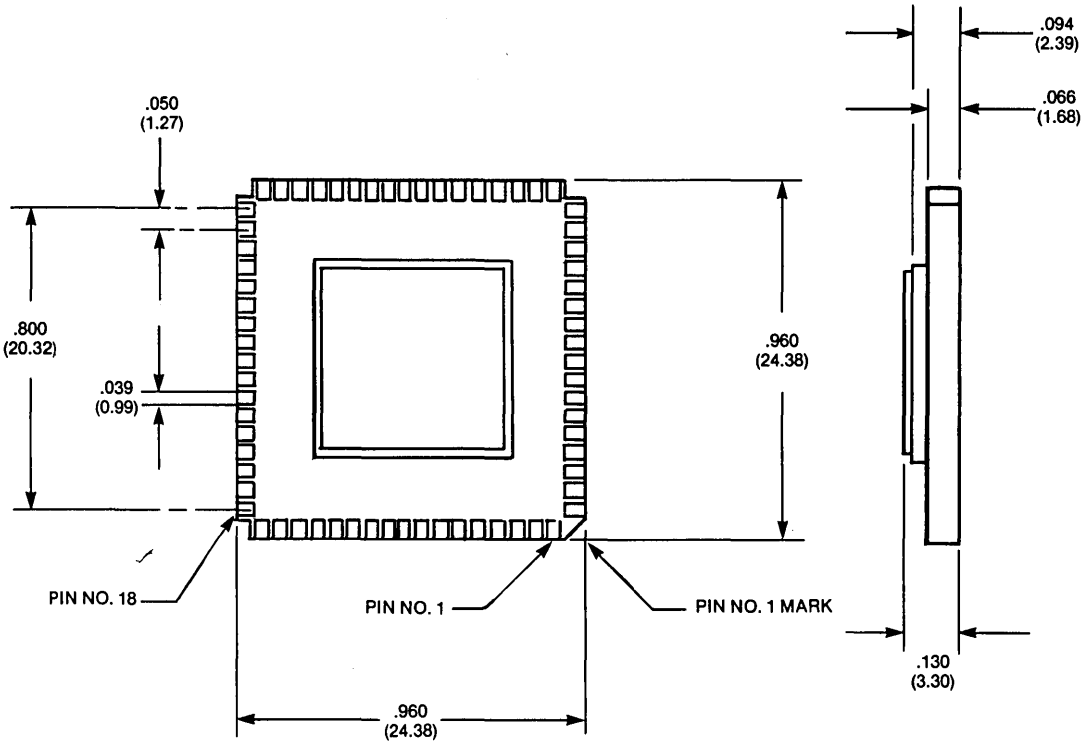


FIGURE 6. WD8206 JEDEC TYPE A PACKAGE

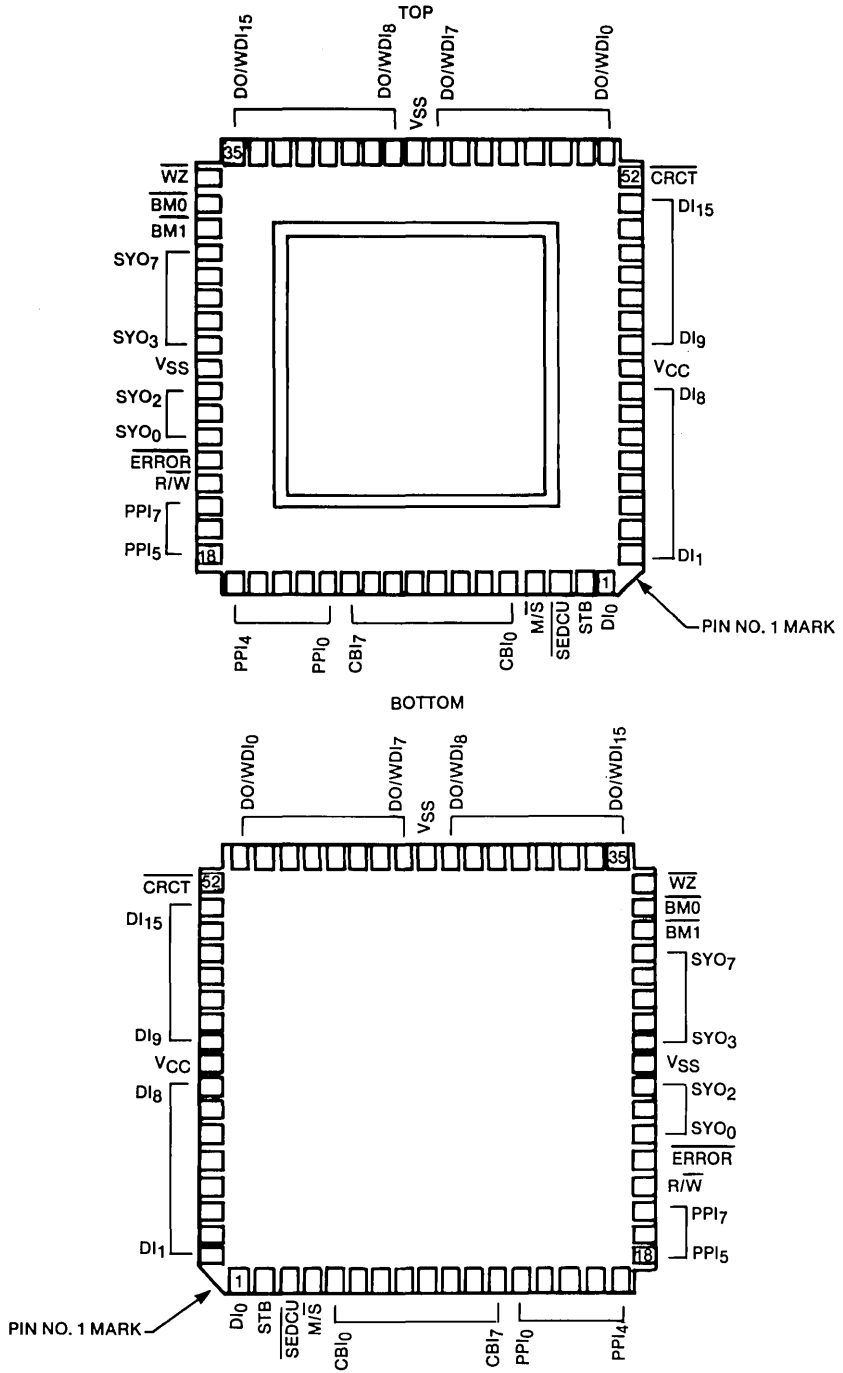


FIGURE 7. WD8206 PINOUT DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to + 150°C
Voltage On Any Pin
With Respect to Ground ..... -0.5V to + 7V
Power Dissipation ..... 2.5 Watts

*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

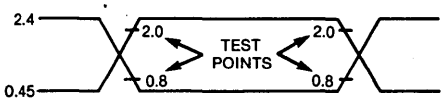
DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ±10%, V_{SS} = GND)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{CC}	Power Supply Current				
	- Single WD8206 or Slave #1		270	mA	
	- Master in Multi-Chip or Slaves #2, 3, 4		230	mA	
V_{IL}[1]	Input Low Voltage	-0.5	0.8	V	
V_{IH}[1]	Input High Voltage	2.0	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage				
	- DO		0.4	V	I_{OL} = 8mA
	- All Others		0.4	V	I_{OL} = 2.0mA
V_{OL}	Output Low Voltage				
	- DO	2.6		V	I_{OH} = -2mA
	- All Others	2.4		V	I_{OH} = 0.4mA
I_{LO}	I/O Leakage Current				
	-PPI_4/CE		±20	μA	0.45V $V_{I/O}$ V_{CC}
	-DO/WDI_{0-15}		±10	μA	
I_{LI}	Input Leakage Current				
	- $PPI_{0-3, 5-7}$, CBI_{6-7}, SEDCU[2]		±20	μA	0V V_{IN} V_{CC}
	- All Other Input Only Pins		±10	μA	

NOTES:

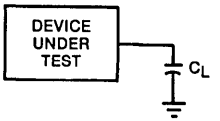
1. SEDCU (pin 3) and M/S (pin 4) are device strapping options and should be tied to V_{CC} or GND. V_{IH} min = V_{CC} - 0.5V and V_{IL} max = 0.5V.
2. PPI_{0-7} (pins 13-20) and CBI_{6-7} (pins 11, 12) have internal pull-up resistors and if left unconnected will be pulled to V_{CC}.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1 and 0.45V FOR A LOGIC 0. TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC 1 AND 0.8V FOR A LOGIC 0.

A.C. TESTING LOAD CIRCUIT



C_L INCLUDES JIG CAPACITANCE

AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±10%, V_{SS} = 0V, C_L = 100pF; all times are in nsec.)

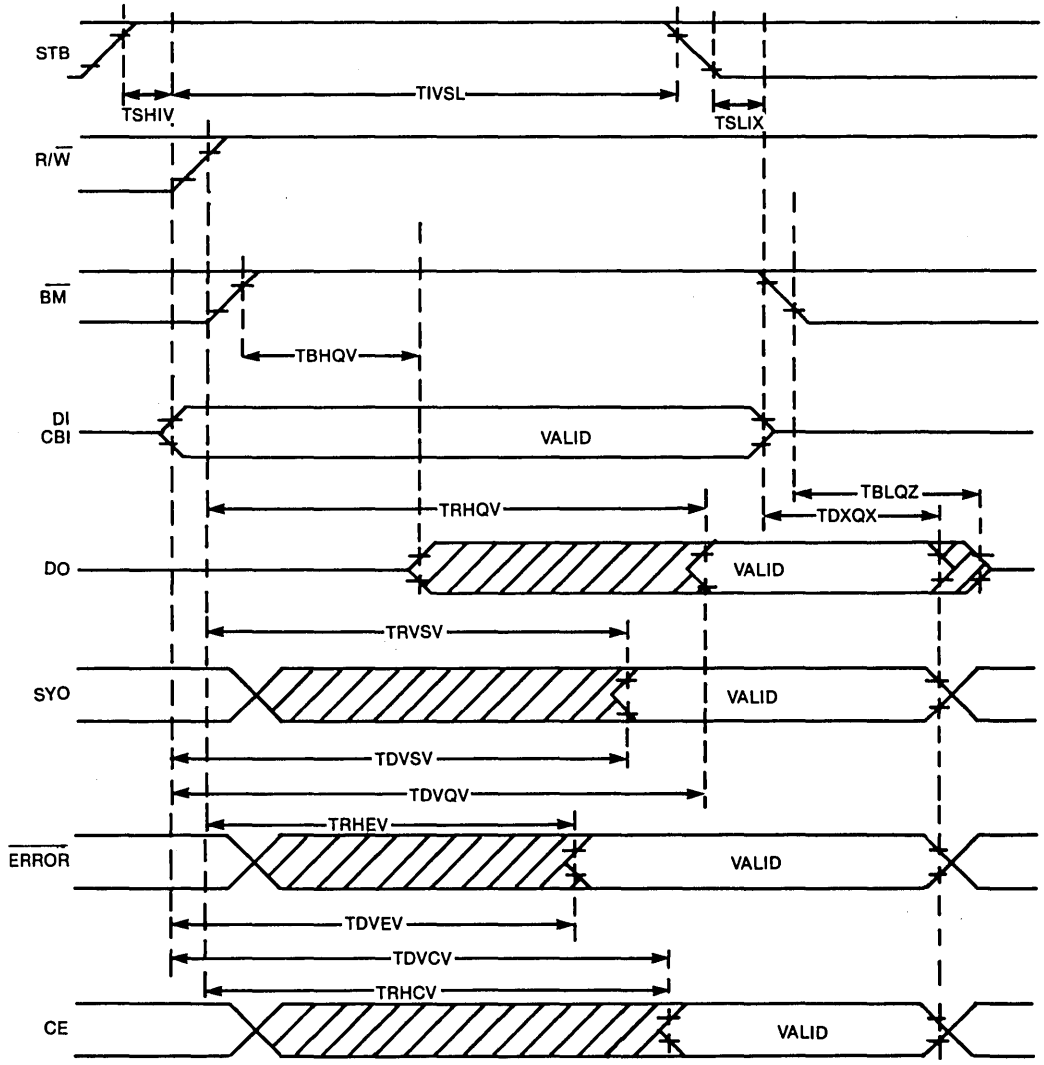
		WD8206		WD8206-8		
SYMBOL	**PARAMETER**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**NOTES**
TRHEV	ERROR Valid from R/W		25		34	
TRHCV	CE Valid from R/W (Single WD8206)		44		59	
TRHQV	Corrected Data Valid from R/W		54		66	1
TRVSV	SYO/CBO/PPO Valid from R/W		42		56	1
TDVEV	ERROR Valid from Data/Check Bits In		52		70	
TDVCV	CE Valid from Data/Check Bits In		70		96	
TDVQV	Corrected Data Valid from Data/Check Bits In		67		90	
TDVSV	SYO/PPO Valid from Data/Check Bits In		55		74	
TBHQV	Corrected Data Access Time		37		43	
TDXQX	Hold Time from Data/Check Bits In	0		0		1
TBLQZ	Corrected Data Float Delay	0	28	0	38	1
TSHIV	STB High to Data/Check Bits In Valid	30		40		2
TIVSL	Data/Check Bits In to STB Set-up	5		5		
TSLIX	Data/Check Bits In from STB Hold	25		30		
TPVEV	ERROR Valid from Partial Parity In		30		40	
TPVQV	Corrected Data (Master) from Partial Parity In		61		76	1
TPVSV	Syndrome/Check Bits Out from Partial Parity In		43		51	1
TSVQV	Corrected Data (Slave) Valid from Syndrome		51		69	
TSVCV	CE Valid from Syndrome (Slave number 1)		48		65	
TQVQV	Check Bits/Partial Parity Out from Write Data In		64		80	1
TRHSX	Check Bits/Partial Parity Out from R/W, WZ Hold	0		0		1
TRLSX	Syndrome Out from R/W Hold	0		0		
TQXQX	Hold Time from Write Data In	0		0		1
TSVRL	Syndrome Out to R/W Set-up	17		22		
TDVRL	Data/Check Bits In to R/W Set-up	39		46		1
TDVQU	Uncorrected Data Out from Data In		32		43	
TTVQV	Corrected Data Out from CRCT		30		40	
TWLQL	WZ to Zero Out		30		40	
TWHQX	Zero Out from WZ Hold	0		0		

NOTES:

1. A.C. Test Levels for CBO and DO are 2.4V AND 0.8V.
2. T_{SHIV} is required to guarantee output delay timings: T_{DVEV}, T_{DVCV}, T_{DVSV}, T_{SHIV} + T_{IVSL} guarantees a min STB pulse width of 35 nsec (45 nsec for the WD8206-8).

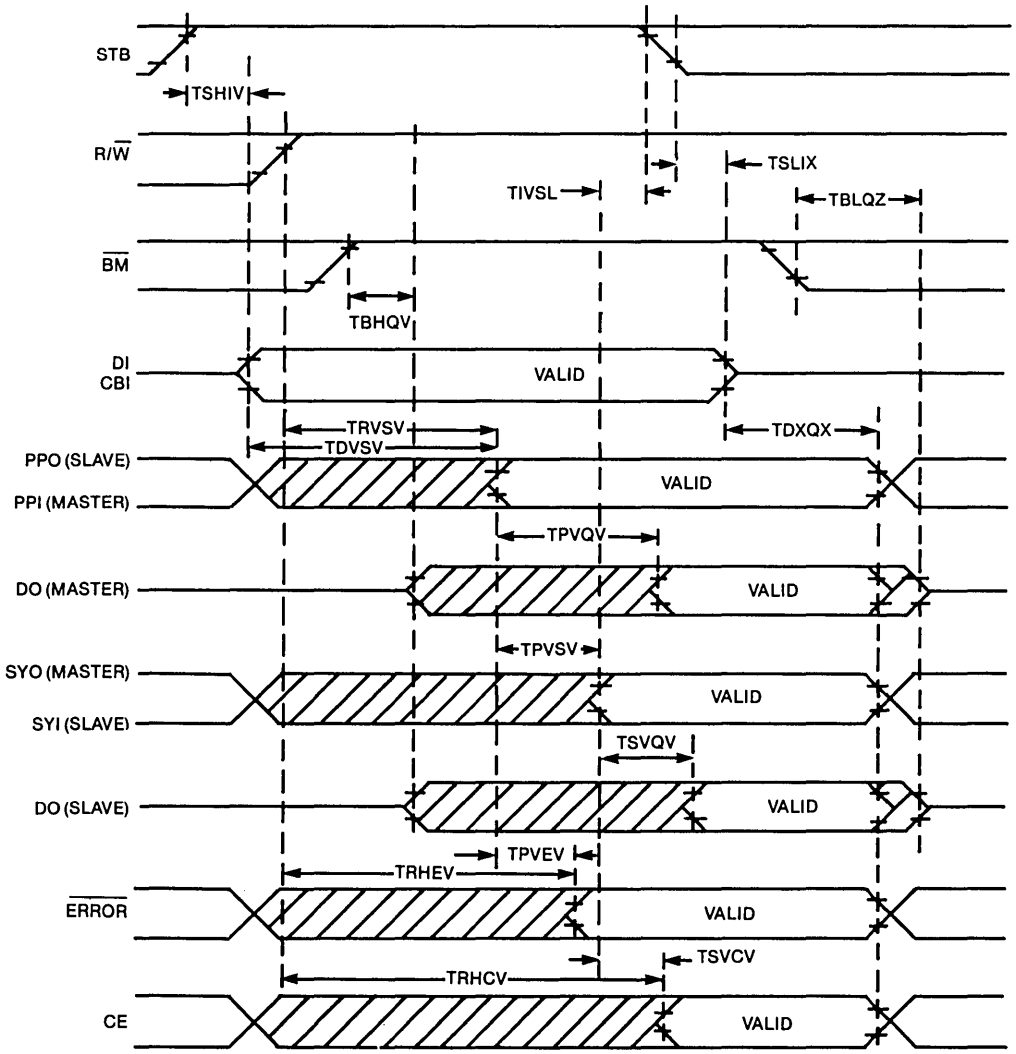
WAVEFORMS

READ – 16-BIT ONLY



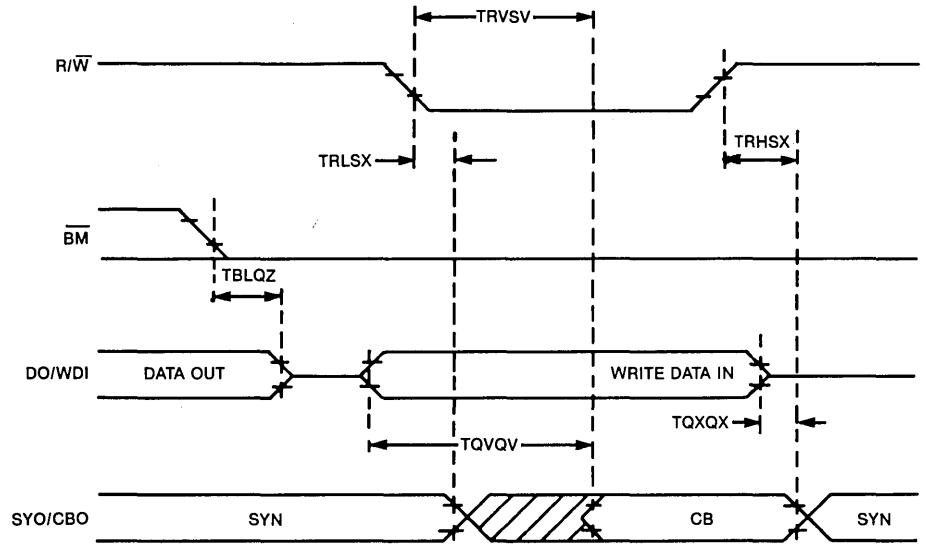
WAVEFORMS (Continued)

READ – MASTER / SLAVE

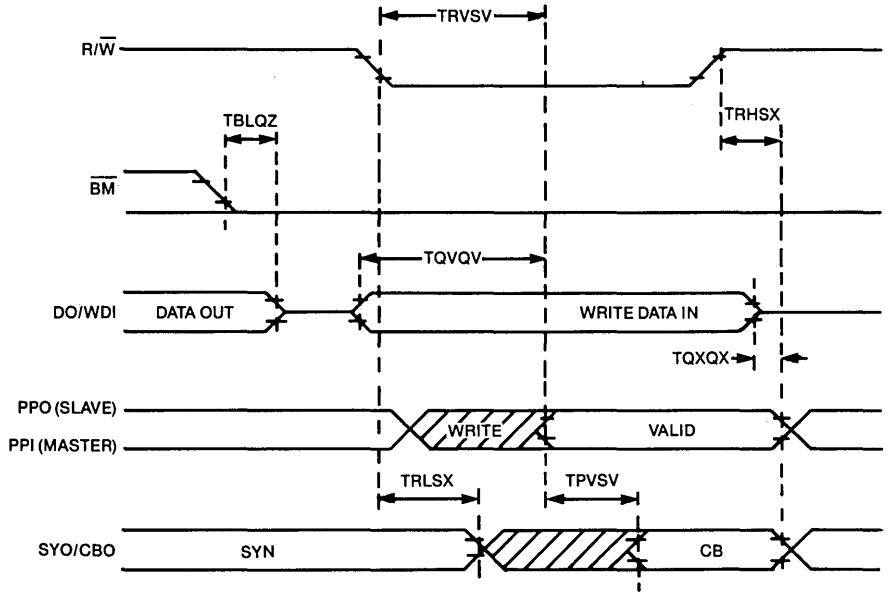


WAVEFORMS (Continued)

FULL WRITE – 16-BIT ONLY

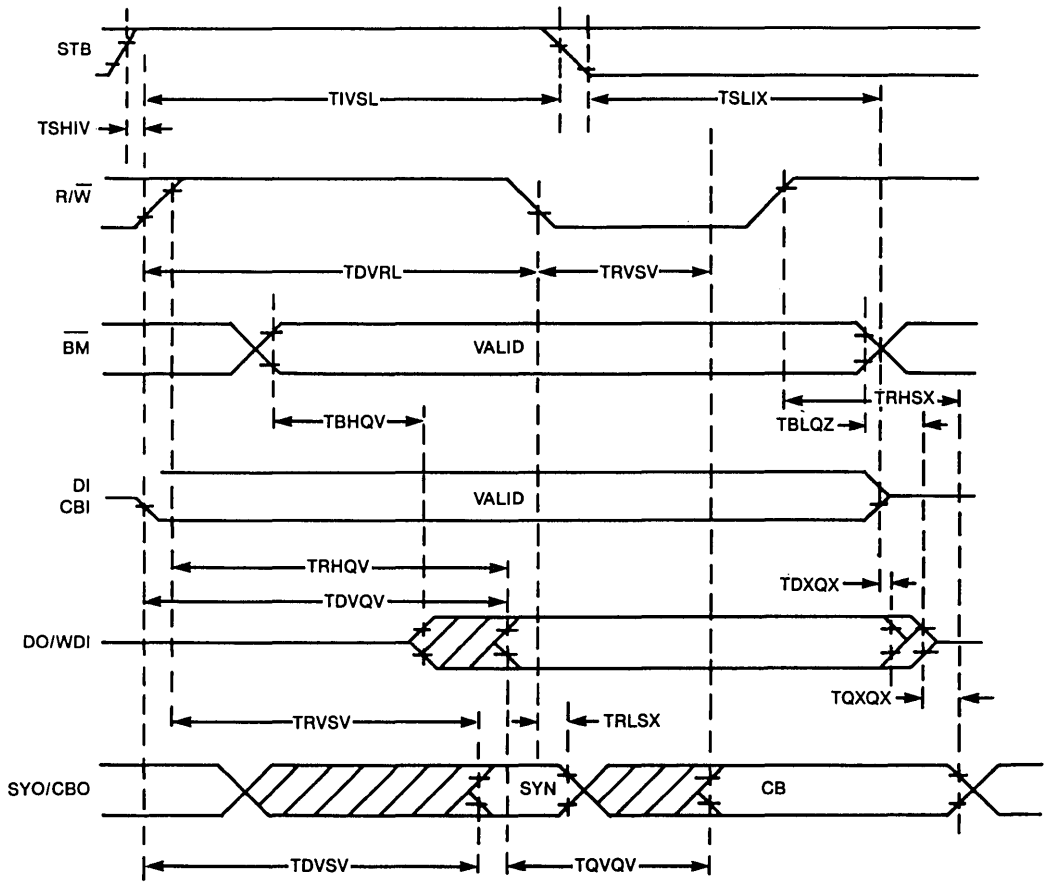


FULL WRITE — MASTER/SLAVE



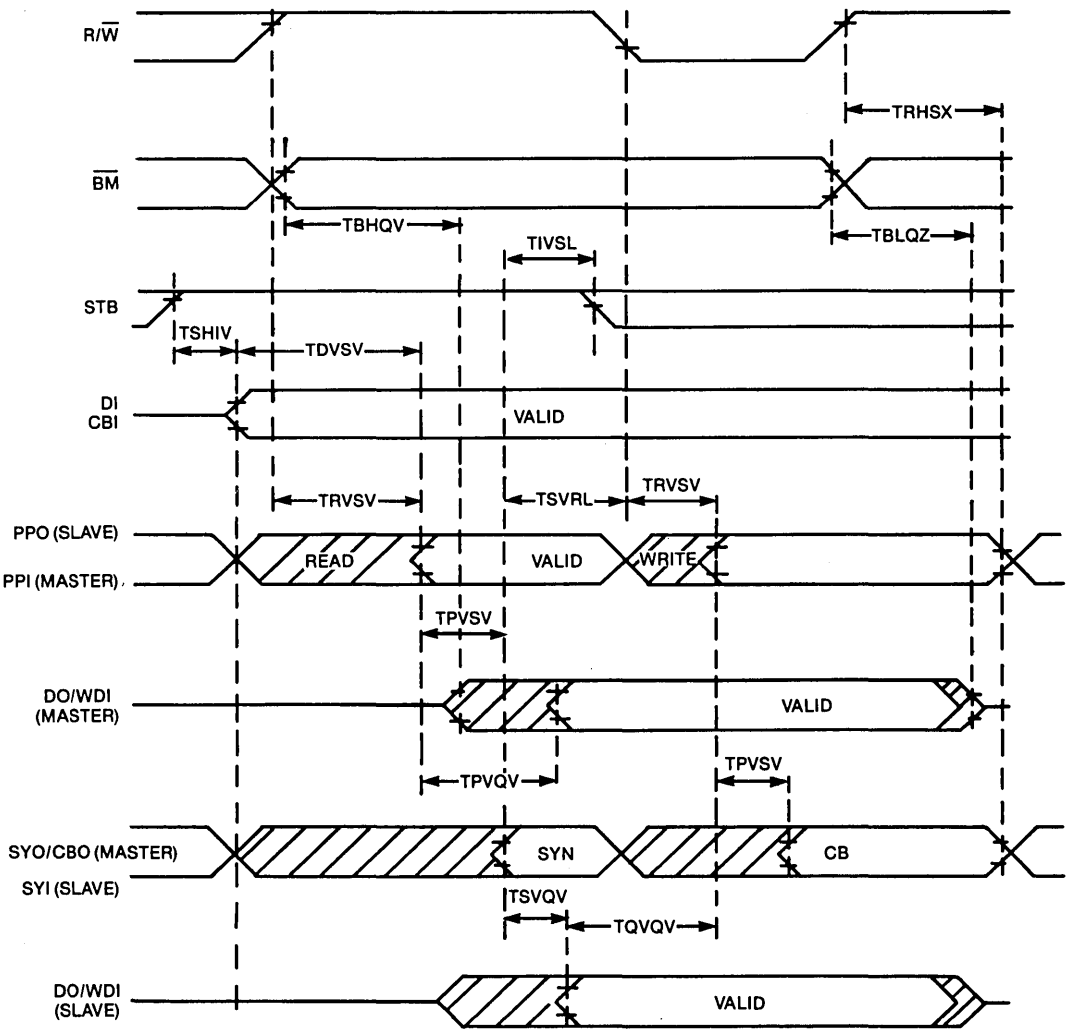
WAVEFORMS (Continued)

READ MODIFY WRITE – 16-BIT ONLY



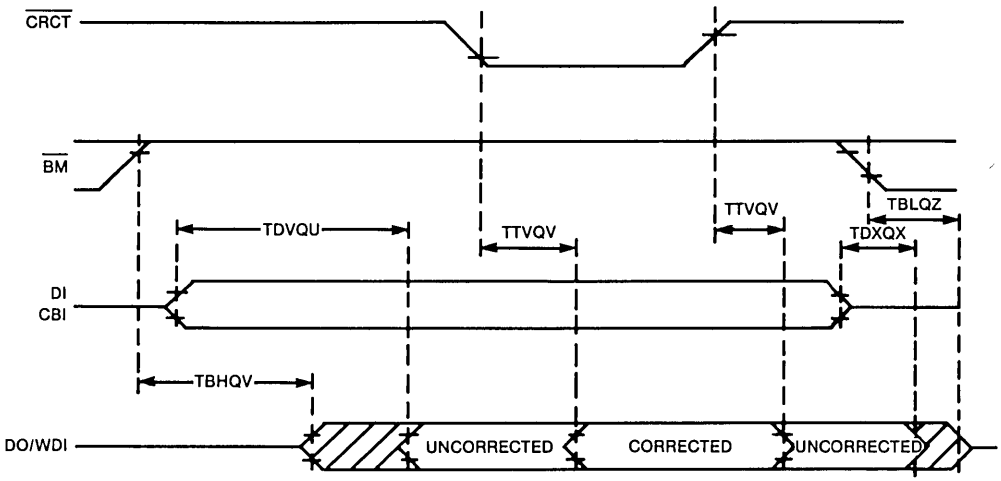
WAVEFORMS (Continued)

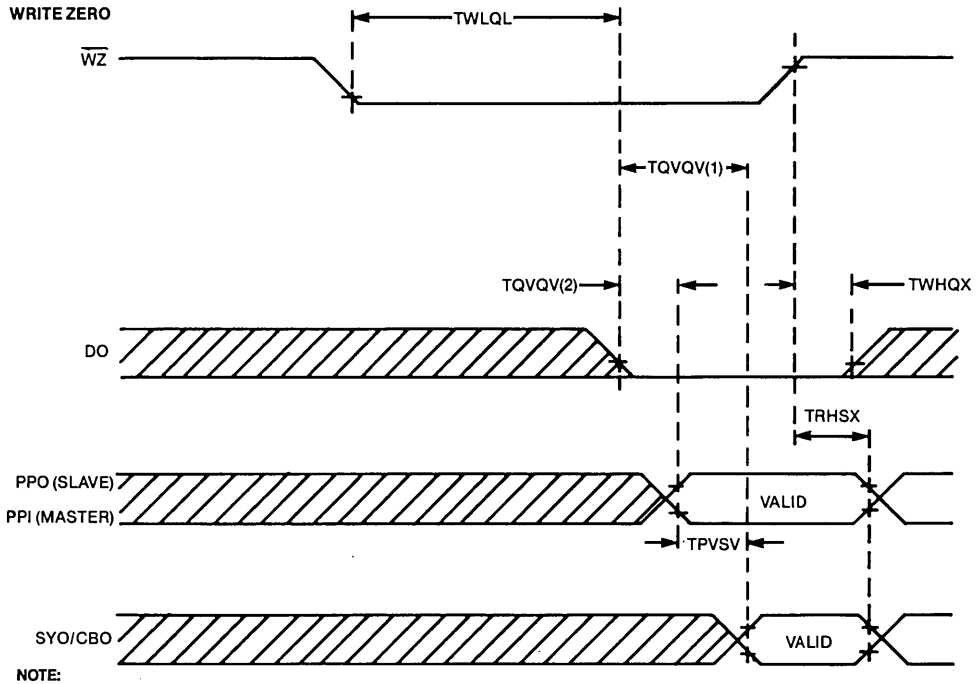
READ MODIFY WRITE – MASTER/SLAVE



WAVEFORMS (Continued)

NON-CORRECTING READ





NOTE:
(1): 16-BIT ONLY
(2): MASTER/SLAVE

WD93020 Integrated Drives

WD93020 INTEGRATED DRIVES

Western Digital's initial peripheral subsystem offering, the WD93020 series of integrated disk drives, adds all disk controller functions to a 20 megabyte Winchester disk drive. Eliminating the requirement for a separate controller card, the subsystem's small size and attractive price make it economically feasible to use Winchester disk drive technology into applications like portable personal computers or low cost home computers. Western Digital Integrated Drive models are configured with a popular selection of host computer plug compatible interfaces: SCSI, IBM PC-XT, and IBM PC-AT.

BASIC DRIVE FEATURES:

- TWO-PLATTER, 3.5-INCH, FIXED MEDIA DISK DRIVE.
- A FORMATTED DATA CAPACITY OF 20 MEGABYTES.
- A SINGLE PRINTED CIRCUIT BOARD ASSEMBLY.
- AN AVERAGE ACCESS TIME OF 85 MILISECONDS.
- POWER DISSIPATION OF LESS THAN 12 WATTS.
- UP TO 850 TRACKS PER INCH.

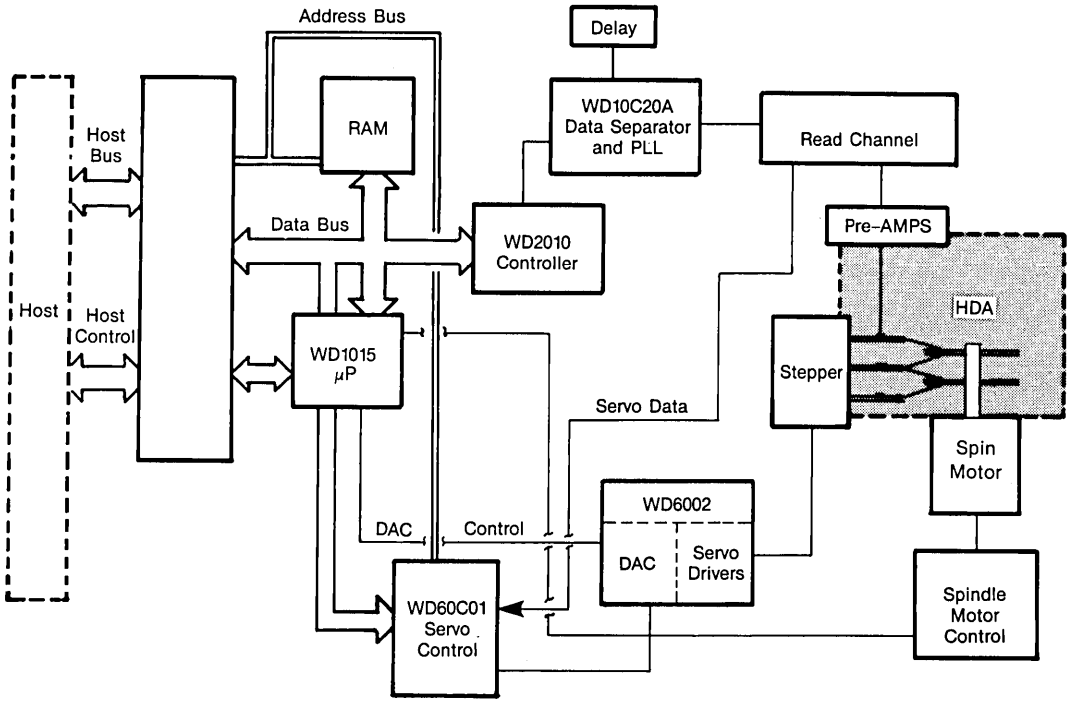
BASIC CONTROLLER FEATURES:

- PLUG COMPATIBLE INTERFACES: SCSI, IBM PC-XT, AND IBM PC-AT.
- MODIFIED FREQUENCY MODULATION (MFM) ENCODING
- PROGRAMMABLE SECTOR INTERLEAVE FOR CONSECUTIVE SECTOR TRANSFERS: 2:1 INTERLEAVE ON PC INTERFACES; 1:1 INTERLEAVE ON SCSI INTERFACES.
- BUILT-IN SELF-TEST AND DIAGNOSTIC CAPABILITIES COVERING BOTH DRIVE AND CONTROLLER OPERATION.
- IMPROVES DATA RELIABILITY BY INCORPORATING ONBOARD DATA SEPARATION.
- AUTOMATIC WRITE PRECOMPENSATION.
- AT/XT - SUPPORTS MULTIPLE TRACK/CYLINDER READ/WRITE.
- SCSI - SUPPORTS BLOCK MODE TRANSFER.
- ERROR DETECTION AND CORRECTION CAPABILITY USING A 32-BIT POLYNOMIAL.
- THE SCSI INTERFACE HAS FULL IMPLEMENTATION OF THE SCSI PROTOCOL INCLUDING DISCONNECT/RECONNECT.
- A 40-PIN, SINGLE CABLE CONNECTION FOR THE IBM PC MODELS.

INTEGRATED DRIVE SPECIFICATIONS

TECHNOLOGICAL CHARACTERISTICS	
CAPACITY - Formatted	20.0 Megabytes
- Unformatted	25.5 Megabytes
CYLINDERS	612
TRACK CAPACITY	10,416 Bytes
NUMBER OF DISKS	2
MEDIA	Ferrous Oxide or Thin Film
RECORDING SURFACES	4
READ/WRITE HEADS	4
HEAD POSITIONER	Stepper Motor
ENCODING METHOD	Modified-frequency Modulation
PERFORMANCE CHARACTERISTICS	
SEEK - Track to Track	15 Milliseconds
- Average	85 Milliseconds
- Maximum	150 Milliseconds
ROTATIONAL LATENCY	8.6 Milliseconds
HEAD SETTLING	Included in Seek Times
TRANSFER RATE	5.0 Megabits per Second
RELIABILITY	
CORRECTED ERROR RATES - Hard	1 in 10^{-13}
Read retries and - Soft	1 in 10^{-11}
ECC Enabled - Seek	N/A
RAW ERROR RATES - Hard Errors	1 in 10^{-12}
- Soft Errors	1 in 10^{-10}
- Seek Errors	1 in 10^{-6}
MTBF	15,000 Power-On-Hours
PREVENTIVE MAINTENANCE	None
SERVICE LIFE	5 Years
MTTR	30 Minutes
PHYSICAL CHARACTERISTICS	
SIZE - Height	41.0 mm. (1.614 in.)
- Width	101.0 mm. (3.976 in.)
- Depth	129.5 mm. (5.100 in.)
WEIGHT	1.2 Lbs.
DC POWER - Input Voltage	+5 VDC ± 5% @0.8 Amps Typ. +12 VDC ± 5% @ 0.7 Amps Typ.
- Maximum Start	2 Amps @ +5 VDC 1 Amp @ +12 VDC
HEAT DISSIPATION	12 Watts Average
ENVIRONMENTAL CHARACTERISTICS	
TEMPERATURE - Operating	4°-50°C (40°-122°F)
- Non-operating	-40°-60°C (-40°-140°F)
- Gradient	± 10°C/Hour (± 18°F/Hour)
RELATIVE HUMIDITY	8 - 90% No Condensation
MAXIMUM WET BULB	76°F Non-condensing
SHOCK - Operating	10 G 10 ms Half Sine Wave
- Non-operating	50 G 10 ms Half Sine Wave
VIBRATION - Operating	2 - 10 Hz 0.1 in. Dbl Amplitude 10 - 500 Hz 0.5 G (O-P)
- Non-operating	2 - 10 Hz 0.4in. Dbl Amplitude 10 - 500 Hz 2.0 G (O-P)
ALTITUDE - Operating	-1,000 - 10,000 Feet
- Non-operating	-1,000 - 50,000 Feet

Specifications and features are subject to change without notice.



WD93020 INTEGRATED DRIVE ELECTRONICS (TYPICAL)

ORDERING INFORMATION

OBSOLETE PACKAGE DESIGNATIONS

A 40 Lead DIP-Ceramic
B 40 Lead DIP-Relpak
C 24 Lead DIP-Ceramic
E 28 Lead DIP-Ceramic
F 28 Lead DIP-Relpak
J 16 Lead DIP-Ceramic
K 16 Lead DIP-Plastic (Totally Encapsulated)
L 18 Lead DIP-Ceramic
M 18 Lead DIP-Plastic (Totally Encapsulated)
P 40 Lead DIP-Plastic (Totally Encapsulated)
R 28 Lead DIP-Plastic (Totally Encapsulated)
T 48 Lead DIP-Ceramic
U 20 Lead DIP-Ceramic
V 20 Lead DIP-Plastic (Totally Encapsulated)
X 20 Ceramic KIT
Y 20 Plastic KIT

CURRENT PACKAGE DESIGNATIONS

PACKAGE TYPE:		LEAD COUNT:	
A	Ceramic DIP	A	<14 Lead
P	Plastic DIP	D	18 Lead
C	Cerdip DIP	E	20 Lead
D	Ceramic QUAD	F	22 Lead
J	Plastic QUAD	H	28 Lead
		L	40 Lead
		M	44 Lead
		N	48 Lead
		T	68 Lead

Example of obsolete method:
WD1943M00 Where M = Single Digit
Package Designator (M = 18 Lead Plastic)

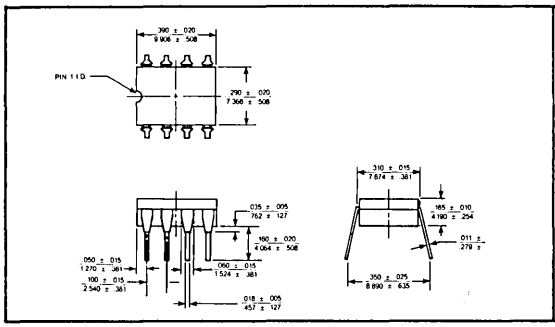
Example of current method:
WD1943PD00 Where PD = Double Digit
Package Designator (P = Plastic and D = 18 Lead)

The following listing indicates the available packages for each product.

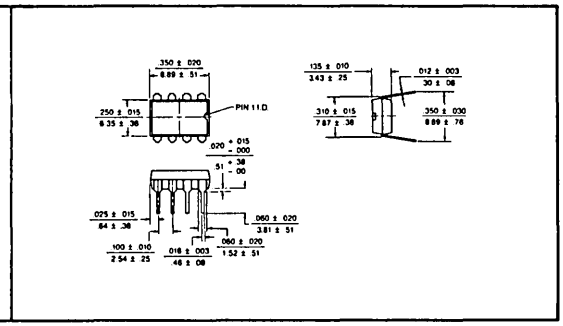
PRODUCT	DIP DUAL IN-LINE PACK.	QSM QUAD SURFACE MOUNT
WD1010-05	PL, AL	DM, JM
WD1014-00	PL, AL	
WD1015-02,10,24	PL, AL	DM, JM
WD10C20	PH, AH	DH, JH
WD1050-00		DT
WD1100-01	PE, AE	
WD1100-03	PE, AE	
WD1100-04	PE, AE	
WD1100-05	PE, AE	
WD1100-06	PE, AE	
WD1100-07	PE, AE	
WD1100-09	PE, AE	
WD1100-12	PE, AE	
WD11C00-13	PE, AE	DH, JH
WD1100-21	AL	
WD11C00-17		DT
WD1691-00	PE, AE, CE	
WD16C92	PL, AL	
WD1770,72,73	PH, AH	DH, JH
WD1771-01	PL, AL	

PRODUCT	DIP DUAL IN-LINE PACK.	QSM QUAD SURFACE MOUNT
FD179X-02	PL, AL	
WD2010-05	PL, AL	DM, JM
WD2143-03	PD, AD, CD	
WD2401	PL, AL	
WD24C02	PL, AL	
WD279X-02	PL, AL	
WD33C92	PN, AN	DM, JM
WD33C93	PL, AL	DM, JM
WD8206-00,02		DT
WD8207-02,05		DT
WD9216-00,01	PA, CA	
WD92C32-00	PA, AA	

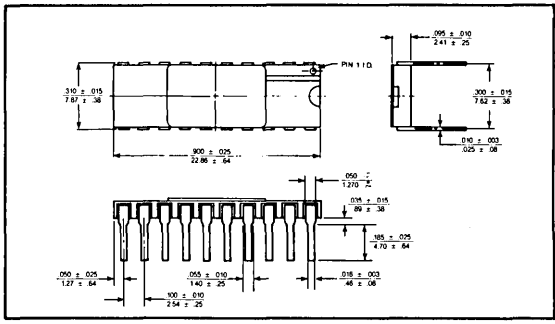
Package Diagrams



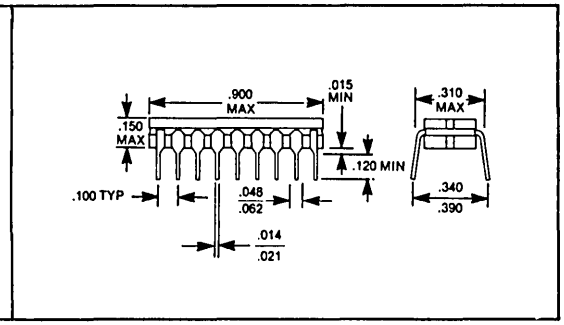
8 LEAD CERDIP "CA"



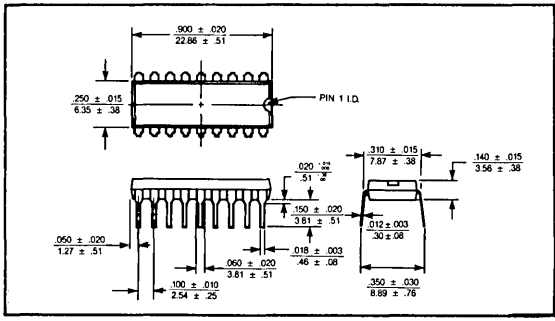
8 LEAD PLASTIC "PA"



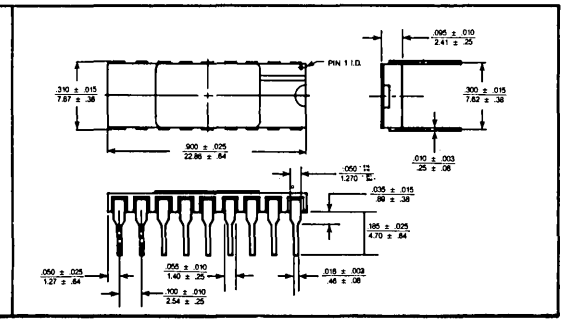
18 LEAD CERAMIC "AD"



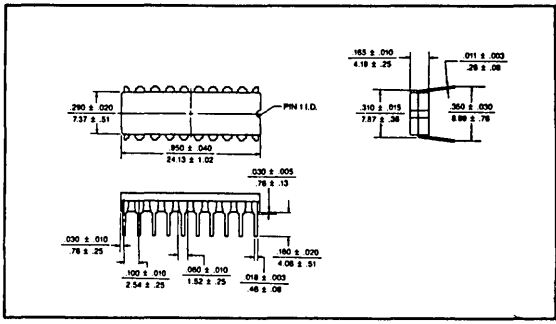
18 LEAD CERDIP "CD"



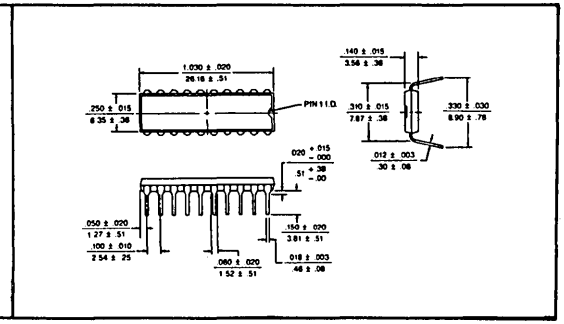
18 LEAD PLASTIC "PD"



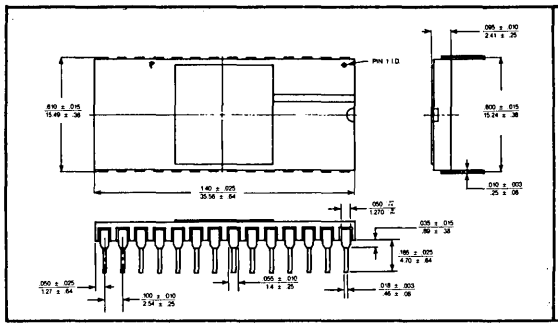
20 LEAD CERAMIC "AE"



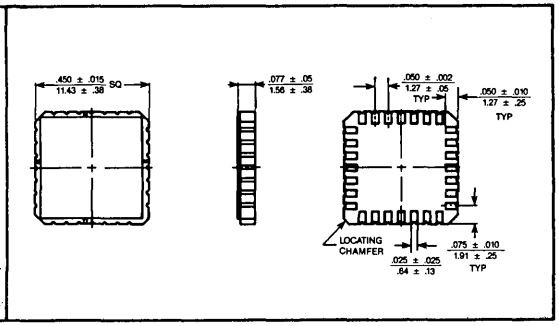
20 LEAD CERDIP "CE"



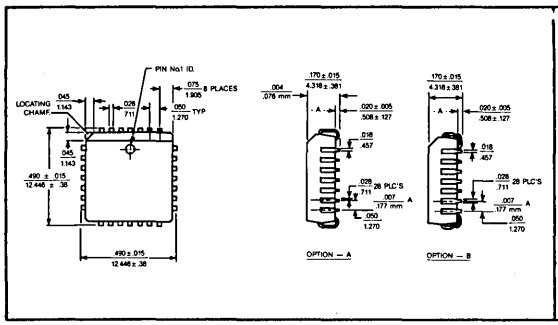
20 LEAD PLASTIC "PE"



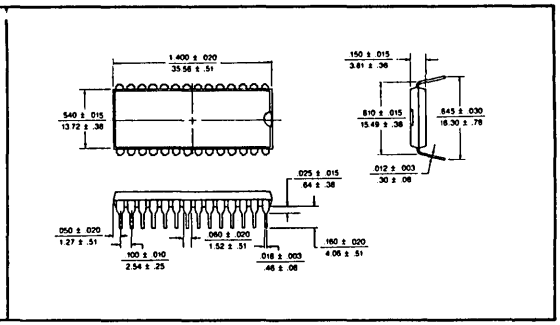
28 LEAD CERAMIC "AH"



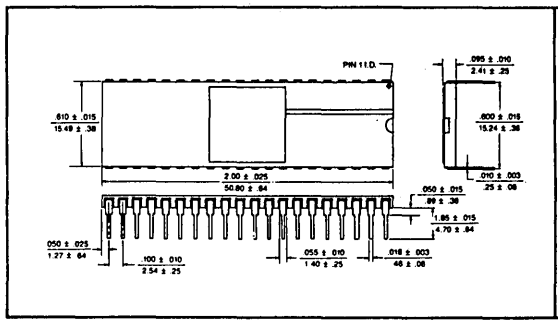
28 LEAD CERAMIC "DH"



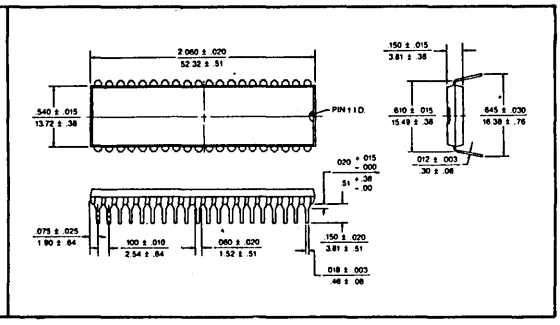
28 LEAD PLASTIC "JH"



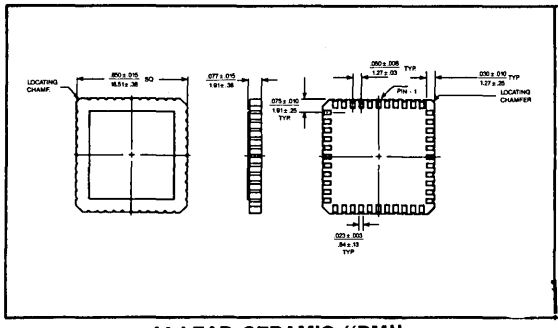
28 LEAD PLASTIC "PH"



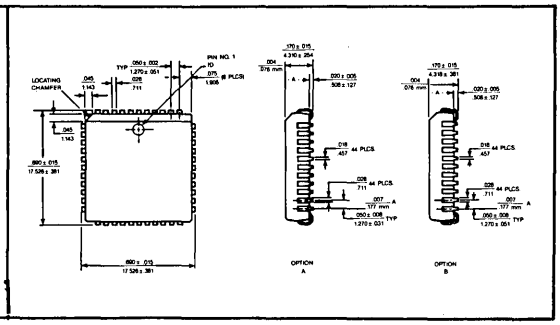
40 LEAD CERAMIC "AL"



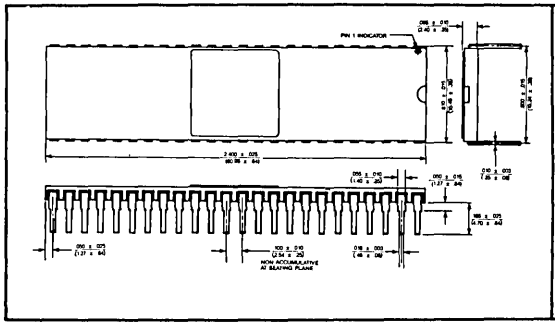
40 LEAD PLASTIC "PL"



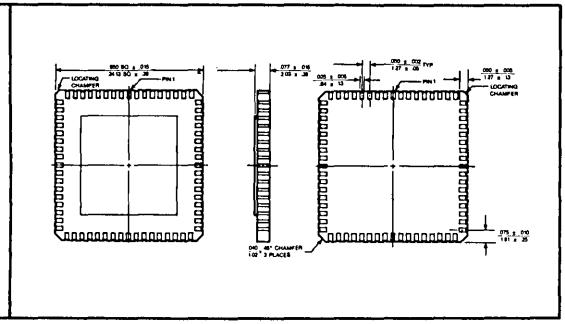
44 LEAD CERAMIC "DM"



44 LEAD PLASTIC "JM"



48 LEAD CERAMIC "AN"



68 LEAD CERAMIC "DT"

Component Products
Terms and Conditions

1. **ACCEPTANCE:** Unless otherwise provided, it is agreed that sales are made on the terms, conditions and warranties contained herein and that to the extent of any conflict, the same take precedence over any terms or conditions which may appear on Buyer's order form. Seller shall not be bound by Buyer's terms and conditions unless expressly agreed to in writing. In the absence of written acceptance of these terms, acceptance of or payment for any of the articles covered hereby shall constitute an acceptance of these terms and conditions.

2. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer and Seller's liability as to delivery ceases upon making delivery of articles purchased hereunder to carrier at shipping point in good condition; the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Unless specific instructions from Buyer specify which method of shipment is to be used, the Seller will exercise his own discretion.

3. **DELIVERY:** Shipping dates are approximate only. Seller shall not be liable for any loss or expense (consequential or otherwise) incurred by Buyer if Seller fails to meet the specified delivery schedule because of unavoidable production or other delays. Seller may deliver the articles in installments, Seller shall not be liable for any delay in delivery or for non-delivery, in whole or in part, caused by the occurrence of any contingency beyond the control either of Seller or Seller's suppliers, including, by way of illustration but not limitation, war (whether an actual declaration thereof is made or not), sabotage, insurrection, riot or other act of civil disobedience, act of public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof, judicial action, labor dispute, accident, fire, explosion, flood, storm or other act of God, shortage of labor, fuel, raw material or machinery or technical failure where Seller has exercised ordinary care in the prevention thereof. If any contingency occurs, Seller may allocate production and deliveries among Seller's customers.

4. **TERMS AND METHODS OF PAYMENT:** Where seller has extended credit to Buyer, terms of payment shall be net thirty (30) days from date of invoice. The amount of credit or terms of payment may be changed or credit withdrawn by Seller at any time. If the articles are delivered in installments, Buyer shall pay for each installment in accordance with the terms hereof. Payment shall be made for the articles without regard to whether Buyer has made or may make any inspection of the articles. If shipments are delayed by Buyer, payments are due from the date when Seller has prepared to make shipments. Articles held for Buyer are at Buyer's sole risk and expense.

5. **TAXES:** All prices are exclusive of all federal, state and local excise, sales, use, and similar taxes; when applicable to this sale or to the articles sold, will appear as separate additional items on the invoice unless Seller receives a properly executed exemption certificate from Buyer prior to shipment.

6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents or trademarks arising from compliance with Buyer's designs or specifications or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements. Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information and assistance (at the Seller's expense) for the defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is in such suit held to constitute infringement and the use of said product or part is enjoined, the Seller, shall at its own expense, either procure for the Buyer the right to continue using said product or part, or replace same with non-infringing product, or modify it so it becomes non- infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof.

7. **ASSIGNMENT:** The Buyer shall not assign his order or any interest therein or any rights thereunder without the prior written consent of Seller.

8. **WARRANTY:** Seller warrants articles of its manufacture against materials or workmanship for a period of one year from date on which Seller delivers said articles. The liability of Seller under this warranty is limited at Seller's option, solely to repair, replacement with equivalent articles, or an appropriate credit adjustment not to exceed the original sales price of articles returned to the Seller provided that (a) Seller is promptly notified in writing by Buyer upon discovery of defects, (b) the defective article is returned to Seller, transportation charges prepaid by Buyer, and (c) Seller's examination of such article disclosed to its satisfaction that defects were not caused by negligence, misuse, improper installation, accident, or unauthorized repair or alteration by the Buyer. In the case of equipment articles, this warranty does not include mechanical parts failing from normal usage nor does it cover limited life electrical components which deteriorate with age. In the case of accessories, not manufactured by Seller, but which are furnished with the Seller's equipment, Seller's liability is limited to whatever warranty is extended by the manufacturers thereof and transferable to the Buyer. This Warranty is expressed in lieu of all other Warranties, expressed or implied, including the implied Warranty of fitness for a particular purpose, and of all other obligations or liabilities on the Seller's part, and it neither assumes nor authorizes any other person to assume for the Seller any other liabilities. This Warranty should not be confused with or construed to imply free preventative or remedial maintenance, calibration or other service required for normal operation of the equipment articles. These Warranty provisions do not extend the original Warranty period of any article which has either been repaired or replaced by Seller. In no event will Seller be liable for any incidental or consequential damages.

9. **TERMINATION:** Buyer may terminate this contract in whole or from time to time in part upon 60 days written notice to Seller. In such event Buyer shall be liable for termination charges which shall include a price adjustment based on the quantity of articles actually delivered, and all costs, direct and indirect, incurred and committed for this contract together with a reasonable allowance for pro-rated expenses and profits. Any termination or back off in scheduling will not be allowed on shipments scheduled for the month in which the request is made and for the month following.

10. **GOVERNMENT CONTRACTS:** If the articles to be furnished under this contract are to be used in the performance of a Government contract or subcontract and a Government contract number shall appear on Buyer's purchase order, those clauses of the applicable Government procurement regulation which are mandatorialy required by Federal Statute to be included in Government subcontracts shall be incorporated herein by reference.

11. **ORIGIN OF ARTICLES:** Seller engages in off-shore production, assembly and / or processing and makes no warranty or representation, expressed or implied, that the articles delivered hereunder are United States articles or of U.S. origin for the purpose of any statute, law, rule, regulation or case thereunder. If Buyer ships the articles hereunder out of the U.S. for assembly, then at Buyer's request in writing, Seller shall provide information applicable to identification of any articles not of U.S. origin.

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2445 McCabe Way, Irvine, CA 92714
(714) 863-0102 • TWX 910-595-1139