IMAGING

WD90C10

(PVGA1M) Enhanced

VGA Controller

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1.0   INTRODUCTION

Western Digital Imaging WD90C10 is a 1.25 micron CMOS VLSI device that allows the design of a VGA graphics subsystem to interface with the PC/XT/AT bus, as well as the IBM Micro Channel Bus, while maintaining backwards compatibility with previous video standards such as MDA, EGA, CGA, Hercules and AT&T 6300. The enhancements include Western Digital registers for EGA register level compatibility for PS/2 and TTL monitors, 1024 by 768 color graphics support, and integrated Micro Channel and AT interface. A major advantage of the WD90C10 is that designs implementing this graphics controller will be able to run applications requiring VGA hardware and BIOS compatibility, and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode. The WD90C10 supports two 256 Kbyte by 4 DRAMs for operation.

This data book supplies sales order information, a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package mechanical information, and a list of associated references.
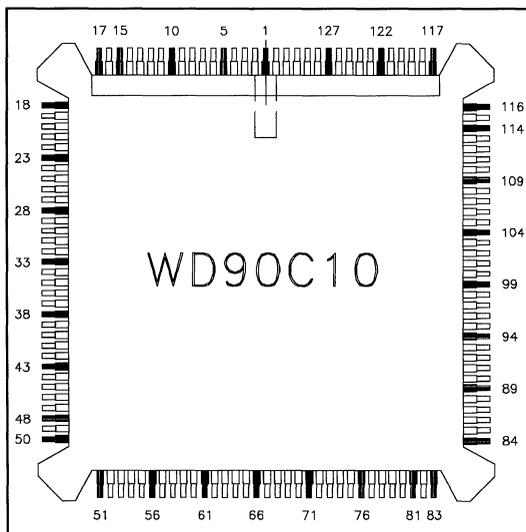
FIGURE 1. WD90C10 PIN DIAGRAM

Ordering Information: WD90C10 Part Number: WD90C10LR00 02.

1.1   FEATURES

* Provides single Chip Video Graphics Solution for IBM PC, XT, AT, and PS/2 compatible systems.
* Supports two 256 Kbyte by 4 DRAMs, providing high performance, high resolution, and 256 colors.
* Pin compatible with the WD90C11 and WD90C12.
* 100% hardware compatible with IBM's VGA and EGA with hidden register support.
* 100% CGA, MDA, Hercules Graphics, and AT&T Model 6300 compatible.
* With two 256K by 4 DRAMs will support 1024 by 768 by 2/4 colors, 800 by 600 by 16 colors, 132 column text.
* Write cache for improved CPU write performance.
* 8- or 16-bit data bus for I/O and memory. True 16-bit CPU to video memory transfer for all modes.
* Up to 65 MHz maximum video clock rate.
* Up to 42 MHz maximum memory clock rate.
* Up to four simultaneous displayable fonts.
* 6, 7, 8, and 9 pixel wide fonts.
* Up to 16 fonts can be loaded.
* Provides adapter video BIOS ROM decoding.
* Total of 18 address bits for cursor location and start address.
* Special double scanning and underline.
* Special display enable or blanking output signal.
* Special border disable.
* Lockable palette, RAMDAC, and overscan registers.
* Special register locking for flat panel applications.
* Supports 16-bit I/O register transfer to index/data register pairs.
* Adjustable internal FIFO and fast page memory interface.
* 132-pin Plastic Flat Pack (PFP) JEDEC package.
* Integrated Feature connector interface and external RAMDAC support.

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	A14	34	D8	67	MD14	100	VID0
2	A15	35	D7	68	MD13	101	VID1
3	A16	36	D6	69	MD12	102	VID2
4	A17	37	D5	70	MD11	103	VID3
5	A18	38	D4	71	MD10	104	VID4
6	A19	39	D3	72	MD9	105	VID5
7	A20	40	D2	73	MD8	106	VID6
8	A21	41	D1	74	MD7	107	VID7
9	A22	42	D0	75	MD6	108	+5VDC
10	A23	43	[$\overline{WE1}$]	76	MD5	109	$\overline{EXVID}$
11	$\overline{BHE}$	44	GND	77	GND	110	GND
12	EMEM	45	$\overline{MRD}$ (M/$\overline{IO}$)	78	MD4	111	VREF
13	$\overline{EIO}$ (3C3D0)	46	$\overline{MWR}$ ($\overline{S0}$)	79	MD3	112	MDET [FSADJ]
14	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	47	$\overline{IOR}$ ($\overline{S1}$)	80	MD2	113	[GND-Analog]
15	GND	48	$\overline{IOW}$ ($\overline{CMD}$)	81	MD1	114	B
16	IRQ ($\overline{IRQ}$)	49	RSET	82	MD0	115	G
17	+5VDC	50	+5VDC	83	+5VDC	116	R
18	$\overline{EBROM}$	51	GND	84	$\overline{EXPCLK}$	117	A0
19	DIR	52	MA0	85	GND	118	A1
20	RDY	53	MA1	86	USR1	119	A2
21	$\overline{MEMCS16}$ ($\overline{CDDS16}$)	54	MA2	87	USR0	120	A3
22	$\overline{EDBUFH}$	55	MA3	88	PCLK	121	A4
23	$\overline{EDBUFL}$	56	MA4	89	$\overline{BLNK}$	122	A5
24	$\overline{ROM16}$ ($\overline{CSFB}$)	57	MA5	90	VSYNC	123	[+5 VDC-Analog]
25	$\overline{HTL}$	58	MA6	91	HSYNC	124	A6
26	D15	59	MA7	92	$\overline{RPLT}$	125	A7
27	D14	60	MA8	93	$\overline{WPLT}$	126	A8
28	GND	61	GND	94	VCLK2	127	A9
29	D13	62	$\overline{RAS}$	95	+5VDC	128	A10
30	D12	63	$\overline{CAS}$	96	VCLK1	129	A11
31	D11	64	$\overline{WE0}$	97	VCLK0	130	A12
32	D10	65	$\overline{OE}$	98	MCLK	131	GND
33	D9	66	MD15	99	GND	132	A13

TABLE 1. WD90C10 PIN ASSIGNMENTS

NOTE:
(   ) Micro Channel only.
[   ] Reserved for WD90C11 and WD90C12 option.

2.0 WD90C10 ARCHITECTURE

The WD90C10 contains four major internal modules, the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The WD90C10 also has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface, and the Clock interface.

The WD90C10 controls the interfacing between the system microprocessor and video memory. Since the WD90C10 arbitrates video memory between the system microprocessor and the CRT Controller contained within the WD90C10, all data passes through the WD90C10 when the system microprocessor writes to or reads from the video memory.

A FIFO is used internally to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles, using only two 256K by 4 DRAMs.

2.1 WD90C10 MODULES

The CRT Controller module maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The CRT Controller module also generates horizontal sync (HSYNC), vertical sync (VSYNC), and blanking signal for the display monitor.

The Sequencer functions as a timing generator for the AT bus or Micro Channel interface, in I/O or memory cycles. It also provides the character clock in the alphanumeric mode, and the dot clock in the graphics mode, for the CRT, Graphics, and Attribute Controllers.

The Graphics Controller manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the Sequencer.

The Attribute Controller modifies the CRT display data stream in graphics and character modes. It controls blinking, underlining, cursor, pixel panning, reverse video, and background or foreground color in all display modes.
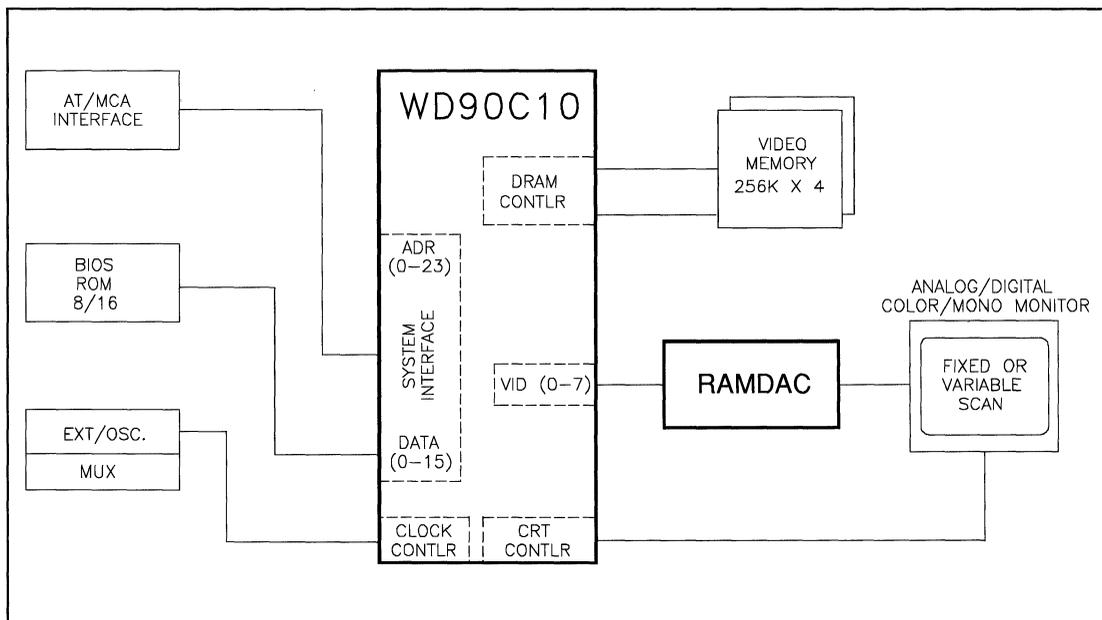

FIGURE 2. SYSTEM BLOCK DIAGRAM

3.0 WD90C10 INTERFACES

3.1 CPU AND BIOS ROM INTERFACE

The WD90C10 is designed to operate in both the PC/XT/AT Bus and the PS/2 Micro Channel Bus architecture configurations. The selection of the mode depends on the setting of a configuration register bit CNF(2), which is determined upon power-up/reset, and is described in the WD90C10 Configuration Bits section of this data book.

Whether configured for either AT or Micro Channel operation, the WD90C10 operates functionally in a manner conducive to PC/XT/AT or Micro Channel interfacing respectively. The signal pins, memory maps and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C10 provides all the signals, and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus, in 8 or 16 bit data path modes. WD90C10 also provides the necessary decoding of the adapter video BIOS ROM. Using the provided signals, the customer can implement designs which operate in 8- or 16-bit mode and control an 8 or 16 bit BIOS ROM.

The I/O data path can be programmed to be either 16- or 8-bit. The CPU to display buffer data path can also be eight or sixteen bits wide for all modes. $\overline{\text{ROM16}}$, $\overline{\text{IOCS16}}$, and $\overline{\text{MEMCS16}}$ signals are generated by the WD90C10.

The WD90C10 has a display memory write cache which holds the CPU write data until it can be transferred to the display memory, allowing the CPU to continue. This feature greatly reduces CPU wait states while writing to the video memory.

The WD90C10 will provide the necessary wait states for CPU accesses to the video memory if necessary. Wait states for I/O accesses and BIOS ROM accesses are not generated.

Special I/O ports such as 46E8H for the AT for setup, and 102H for VGA enable, have been implemented internally in the WD90C10.

3.2 DRAM INTERFACE

The WD90C10 optimizes its interface to the video memory display buffer. The video memory DRAMs are organized as four planes to support all modes from only two 256K by 4 DRAMs by making use of its Fast Page Access of memory. Each plane can be configured as 64 KBytes (128 or 256 Kbyte total).

For display refresh cycles, the WD90C10 will perform page mode read operations on the video memory in graphics modes. In alpha modes, a choice of page video memory read operation is also provided. For video memory write operations during graphics or alpha modes, the WD90C10 will generate standard RAS/CAS cycles as needed. The WD90C10 will also refresh the DRAMs with 3 or 5 (CAS before RAS) refresh cycles after every horizontal scan line.

Two or four 256K by 4, 80 ns DRAMs and a 37.5 MHz MCLK are required for all modes. 70 ns DRAMs can be used with 42 MHz MCLK.

3.3 VIDEO INTERFACE

The WD90C10 is optimized to connect to an analog CRT monitor through a RAMDAC, but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the WD90C10 provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C10 can be programmed to directly generate all the CRT signals for up to 8 bits/pixel (256 color) displays.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected directly to the WD90C10. The WD90C10 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

FIGURE 3. WD90C10 BLOCK DIAGRAM
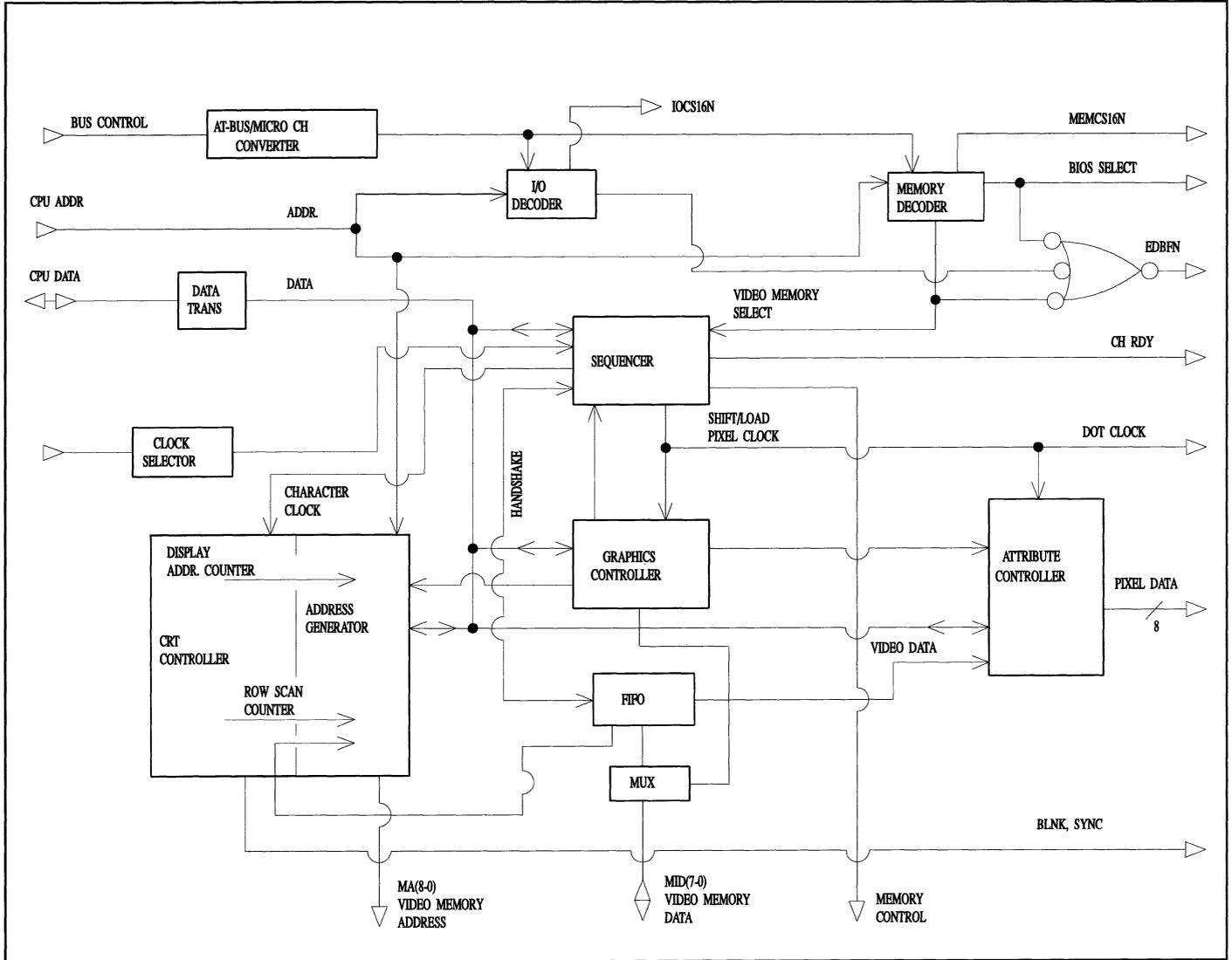
3.4   CLOCK INTERFACE

The WD90C10 has four clock input signal pins; the separate memory clock, MCLK, which drives the DRAM and bus interface timing; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. VCK1 and VCK2 can also be programmed as outputs to provide the option to externally control a multiplexer that supplies the video clock. The MCLK can also be selected as a memory clock or video dot clock .

3.5   WD90C10 POWER-UP CONFIGURA-TION

The WD90C10 uses the memory data pins to configure an internal configuration register upon power- up/reset. CNF(2) will determine whether the WD90C10 will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by the WD90C10 at power-up/reset are used as status bits, or for clock source control.   For more information on WD90C10 power-up configuration, refer to the Configuration Bits section of this data book.

4.0   PIN DESCRIPTION

The following table provides pin definitions for the   mnemonics are used.
132-pin   WD90C10   package.   The   WD90C10

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
POWER ON			
49	RSET	I	RESET: This signal input will reset the WD90C10. MCLK and VCLK0 should be connected to WD90C10 in order for the WD90C10 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the MD15-0 bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
CLOCK SELECTION			
98	MCLK	I	MEMORY CLOCK: This clock signal determines the VGA DRAM timing as well as system interface control timing. MCLK should be a minimum 37.5 MHz for 80 ns DRAMS.
97	VCLK0	I	VIDEO CLOCK 0: This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK is 25.175 MHz to display 640 pixels per horizontal display line. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
96	VCLK1	I/O	VIDEO CLOCK 1: This pin can be a second video display clock input or an output to external clock selection module. Pin direction is determined on Reset by a pull-up/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H (or it reflects the contents of 03C2, Miscellaneous Register, bit 2). Refer to the Configuration Register and PR15 Register, bit 5 description.
94	VCLK2	I/O	VIDEO CLOCK 2: A third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. Acts as a user-defined external clock input, or an output reflecting the content of bit PR2(1) (or it reflects the contents of 03C2, Miscellaneous Register, bit 3) if CNF (3) is set to 1. See the Configuration Register and PR15 Register, bit 5 description.

TABLE 2. PIN DESCRIPTION

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
HOST INTERFACE			
10 9 8 7	A23 A22 A21 A20	I I I I	ADDRESS BUS (A23 - A20): These address bits should be connected to address bus SA23 - 20 in Micro Channel mode. In AT mode, if CNF(11) = 1, then A23-20 should be connected to LA23-20 of the AT address bus. If CNF(11) = 0, then A22-20 should be connected to LA19 - 17 of the AT address bus, and A23 should be connected to an externally decoded ($\overline{LA23}$ x $\overline{LA22}$ x $\overline{LA21}$ x $\overline{LA20}$) = 1 from the AT address bus. CNF(11) = 0 when MD8 is pulled down with a 4.7 Kohm resistor.
6 5 4 3 2 1 132 130 129 128 127 126 125 124 122 121 120 119 118 117	A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	I I I I I I I I I I I I I I I I I	ADDRESS BUS (SA19-SA0): These inputs are directly connected to the system address bus (SA19 - SA0). Latched address. A19 - A17 can be connected to LA19 - LA17 in 386 systems when CNF (11) = 1. Refer to CNF(11) definition.
26 27 29 30 31 32 33 34 35 36 37 38 39 40 41 42	D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	DATA BUS (SD15 - SD0): These bidirectional signals either may be connected directly to a local data bus requiring less than 8 mA of source/sink, or may be connected through two external bus buffers controlled by $\overline{EDBUFH}$, $\overline{EDBUFL}$, and DIR.

TABLE 2. PIN DESCRIPTION (CONT)

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
20	RDY	O	READY: An active high output which signals to the system processor that a memory access is completed, and is used to add wait states to the CPU bus cycles during video memory accesses. It may be pulled inactive by the WD90C10 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.
16	IRQ/($\overline{\text{IRQ}}$)	O	INTERRUPT REQUEST: Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of Vertical Display occurs, this signal will transition active, causing the interrupt. It will stay latched until CRTC11 bit 4 clears it. In an AT system IRQ is usually not connected, but may be connected if desired. $\overline{\text{IRQ}}$ is used to generate interrupt, usually in the Micro Channel mode.
21	$\overline{\text{MEMCS16}}$ ($\overline{\text{CDDS16}}$)	O	MEMORY CHIP SELECT 16 BITS: In AT mode, this line is used to respond the host to enable 16-bit video memory data transfer. In Micro Channel mode, this line is used to indicate 16-bit video memory or I/O access.
13	$\overline{\text{EIO}}$ (3C3D0)	I	ENABLE I/O: In AT mode, this active low signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, this line is from I/O port 3C3 bit 0 to enable video subsystem memory and I/O address decoding. ("1" = enable)
18	$\overline{\text{EBROM}}$	O	ENABLE BIOS ROM: In AT mode, this is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). A WRITE to WD90C10 internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
25	$\overline{\text{HTL}}$	O	ENABLE HIGH-TO-LOW: (for 16-bit BIOS) If only an 8-bit CPU interface is used, this output enables a data buffer to allow reading the upper byte of ROM data on the lower data bus when 2 ROMs (16-bit) are supported.
12	EMEM	I	ENABLE MEMORY: This signal enables memory decoding when high. It is normally connected to the signal -Refresh.

TABLE 2. PIN DESCRIPTIONS (CONT)

NOTE:
(   ) Micro Channel only.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
11	$\overline{BHE}$	I	BYTE HIGH ENABLE: If SA0 is "0", this signal enables 16-bit data transfer mode when $\overline{BHE}$ is "0". With SA0, this signal is also used to select high byte data (SD[15:8]) or low byte data (SD[7:0]). An internal pullup is on this input.
45	$\overline{MRD}$/(M/$\overline{IO}$)	I	MEMORY READ: In AT mode, this signal is called $\overline{MRD}$ and is an active low memory read strobe. In Micro Channel mode, the signal is called M/$\overline{IO}$. It distinguishes between memory and I/O cycles. When (M/$\overline{IO}$) is high, a memory cycle is in process. A low on (M/$\overline{IO}$) shows that an I/O cycle is in process.
46	$\overline{MWR}$/($\overline{S0}$)	I	MEMORY WRITE: The Active low memory write strobe in AT mode. In Micro Channel mode, it becomes $\overline{S0}$ and is the channel status signal which indicates the start and type of a channel cycle. Along with $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ signals, it is decoded to interpret I/O and memory commands.
47	$\overline{IOR}$/($\overline{S1}$)	I	I/O READ: Active low I/O read strobe in AT mode. In Micro Channel mode, it becomes $\overline{S1}$ and is the channel status signal which indicates the start and type of a channel cycle.
48	$\overline{IOW}$/($\overline{CMD}$)	I	I/O WRITE: Active low strobe. In AT mode, the strobe signals an I/O write. In Micro Channel mode it is the bus data strobe $\overline{CMD}$; address bus validity is signaled by $\overline{CMD}$ going low while the rising edge of $\overline{CMD}$ indicates the end of a Micro Channel bus cycle.
14	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	I/O	I/O CHIP SELECT 16 BITS: In AT mode, used to respond to the host to allow 16-bit I/O access. In Micro Channel mode, is driven by the host to individually select channel connector slots during system configuration.
19	DIR	O	DIRECTION CONTROL: Active high Direction Control for external bus buffers in AT and MCA implementation. The default state is low until a read cycle occurs. The WD90C10 will then drive DIR high to change the direction of the data buffers.
22	$\overline{EDBUFH}$	O	ENABLE DATA BUFFER HIGH: Active low signal allows control of an external data buffer for data bits D8 - D15.
23	$\overline{EDBUFL}$	O	ENABLE DATA BUFFER LOW: Active low signal allows control of an external data buffer for data bits D0 - D7.

TABLE 2. PIN DESCRIPTIONS (CONT)

NOTE:
(   ) Micro Channel only.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
24	$\overline{ROM16}$/ $\overline{(CSFB)}$	O	BIOS ROM SELECT 16 BITS: This signal decodes the ROM address space C0000 - DFFFF. It may be combined with SA15 and SA16 to control $\overline{MEMCS16}$ for the address space C0000 - C7FFF. This is an active low, totem-pole output. CARD SELECT FEEDBACK: (Micro Channel mode) This signal is used as Card Selected Feedback to provide positive acknowledgement of its presence at the host's addresses specified. This is an active low output.
DISPLAY MEMORY INTERFACE			
63	$\overline{CAS}$	O	COLUMN ADDRESS STROBE: Active low CAS output signal (for both two and four DRAM configurations).
62	$\overline{RAS}$	O	ROW ADDRESS STROBE: Active low RAS output signal (for both two and four DRAM configurations).
65	$\overline{OE}$	O	OUTPUT ENABLE: Active low DRAM output enable signal (for both two and four DRAM configurations).
64	$\overline{WE0}$	O	WRITE ENABLE: Active low write enable signal for first two DRAMs.
43	$\overline{[WE1]}$	O	Reserved for WD90C11 and WD90C12.
PROGRAMMABLE OUTPUTS			
87	USR0	O	May be used to control special card or system features.
86	USR1	O	May be used to control special card or system features.

TABLE 2. PIN DESCRIPTION (CONT)

NOTE:
[   ] Reserved for WD90C11 and WD90C12.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
VIDEO MEMORY DATA			
66	MD15	I/O	DISPLAY MEMORY DATA (MD15 - 0): These
67	MD14	I/O	lines are the data bus to the video display
68	MD13	I/O	DRAMS. The MD15-MD8 data lines are for
69	MD12	I/O	use with 4-DRAM configurations of the
70	MD11	I/O	WD90C10 or WD90C12 part. Data lines MD0-
71	MD10	I/O	15 are pulled up by internal 50K ohm resistors
72	MD9	I/O	or may be pulled down by external 4.7K ohm
73	MD8	I/O	resistors to provide setup information on power-
74	MD7	I/O	up (reset) as follows:
75	MD6	I/O	
76	MD5	I/O	**MD** **POWER-UP** **REGISTER**
78	MD4	I/O	**FUNCTION** **(BIT)**
79	MD3	I/O	15 EGA SW4 PR11(7) +
80	MD2	I/O	14 EGA SW3 PR11(6) +
81	MD1	I/O	13 EGA SW2 PR11(5) +
82	MD0	I/O	12 EGA SW1 PR11(4) +
			11 Analog/TTL Display CNF(8) *
			10 8- or 16-bit ROMs PR1 (1) *
			9 3C3 or 46E8 I/O Port
			for Setup CNF(9) +
			8 A23 - 20 Connection
			Select CNF(11) +
			7 General Purpose CNF(7) *
			6 General Purpose CNF(6) *
			5 General Purpose CNF(5) *
			4 General Purpose CNF(4) *
			3 VCLK1,2 Input/Output CNF(3) +
			2 AT/Micro Channel Mode CNF(2) +
			1 1 or 2 ROMs CNF(1) *
			0 BIOS ROM Mapping PR1(0) *
			NOTES:
			"*" Pulldown resistor sets these bits to logic 1.
			"+" Pulldown resistor sets these bits to logic 0.
			For more details refer to PR and Configuration
			Registers.
VIDEO MEMORY ADDRESS			
60	MA8	O	MEMORY ADDRESS (MA0 - MA8): Display
59	MA7	O	memory DRAM address. For testing purposes,
58	MA6	O	these pins can be tri-stated by setting Paradise
57	MA5	O	Register PR4(4)=1.
56	MA4	O	
55	MA3	O	
54	MA2	O	
53	MA1	O	
52	MA0	O	

TABLE 2. PIN DESCRIPTIONS

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
RAMDAC INTERFACE			
107	VID7	O	VIDEO (VD0-VD7): Pixel video data output to
106	VID6	O	DAC and to Feature Connector. These lines
105	VID5	O	can drive up to a 8 mA load.
104	VID4	O	
013	VID3	O	
102	VID2	O	
101	VID1	O	
100	VID0	O	
92	$\overline{RPLT}$	O	READ PALETTE: Video DAC register and color palette read signal for an external RAM-DAC. Active low during an I/O read of addresses 3C6H, 3C8H, and 3C9H.
93	$\overline{WPLT}$	O	WRITE PALETTE: Video DAC register and color palette write signal for an external RAM-DAC. Active low during an I/O write to addresses 3C6H-3C9H.
88	PCLK	O	PIXEL CLOCK: Video pixel clock output used by the DAC to latch video signals VID0-7. Its source is one of the video clock inputs: VCLK0, VCLK1 or VCLK2 as determined by the Miscellaneous Output register.
CRT CONTROL			
89	$\overline{BLNK}$	O	BLANK: Active low display monitor blank pulse to external RAMDAC.
91	HSYNC	O	HORIZONTAL SYNC: Display monitor horizontal synchronization pulse. Active high or low depending on the Miscellaneous Output Register programming.
90	VSYNC	O	VERTICAL SYNC: Display monitor vertical synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.
112	MDET [FSADJ]	I	MONITOR DETECT: This pin is used when the RAMDAC is external. It is used to determine the monitor type and can be read at port 3C2H bit 4.
		I	[FULL SCALE ADJUST]: This pin is used when the RAMDAC is internal (WD90C12). It is used to control the RED, GREEN and BLUE's full scale output current.

TABLE 2. PIN DESCRIPTIONS (CONT)

NOTE:
[   ] Reserved for WD90C12.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
INTERNAL RAMDAC [WD90C12]			
116	[RED]	O	RED CURRENT OUTPUT: Used with the WD90C12 - Internal RAMDAC RS170 output from RED DAC to drive an analog monitor.
115	[GREEN]	O	GREEN CURRENT OUTPUT: Used with the WD90C12 - Internal RAMDAC RS170 output from GREEN DAC to drive an analog monitor.
114	[BLUE]	O	BLUE CURRENT OUTPUT: Used with the WD90C12 - Internal RAMDAC RS170 output from BLUE DAC to drive an analog monitor.
111	[VREF]	I	VOLTAGE REFERENCE INPUT: Used with the WD90C12 - Internal RAMDAC input used to set the reference voltage for the RAMDAC.
FEATURE CONNECTOR SUPPORT			
109	EXVID	I	ENABLE EXTERNAL VIDEO DATA: A Feature Connector input. A low tri-states the video data lines VID7:0. An internal pullup resistor is provided. In the WD90C12 the VID7:0 lines become inputs to the internal RAMDAC.
84	EXPCLK	I	ENABLE EXTERNAL PIXEL CLOCK: A Feature Connector input. A low tri-states the PCKL output. An internal pullup resistor is provided.
POWER AND GROUND			
123	[VCC]	-----	[+5VDC - ANALOG for WD90C12]
113	[GND]	-----	[Ground - ANALOG for WD90C12]
17	VCC	-----	+5VDC
50	VCC	-----	+5VDC
83	VCC	-----	+5VDC
95	VCC	-----	+5VDC
108	VCC	-----	+5VDC
15	GND	-----	Ground
28	GND	-----	Ground
44	GND	-----	Ground
51	GND	-----	Ground
61	GND	-----	Ground
77	GND	-----	Ground
85	GND	-----	Ground
99	GND	-----	Ground
110	GND	-----	Ground
131	GND	-----	Ground

TABLE 2. PIN DESCRIPTIONS

NOTE:
[   ] Reserved for WD90C12.

5.0   ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to V_{SS}	-0.3 to 7 Volts
Power Dissipation	1.0 Watt

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

5.1   STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0° to 70°C
Power Supply Voltage	4.75 to 5.25 Volts

5.2   D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS
V(IL)	Input Low Voltage	-0.3	0.8	V	VCC=5V±5%
V(IH)	Input High Voltage	2.0	VCC+0.3	V	VCC=5V±5%
I(IL)	Input Low Current	--	±10	uA	VIN=0.0V
I(IH)	Input High Current	--	±10	uA	VIN=VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +2.0mA[1]
V(OH)	Output High Voltage	2.4	--	V	IOH=-2.0mA[1]
I(OZ)	High Impedance Leakage Current	-10.0	10.0	uA	OV<VOUT<VCC
C(IN)	Input Capacitance	--	10	pF	FC=1 MHz
C(OUT)	Output Capacitance	--	10	pF	FC=1 MHz

TABLE 3. DC CHARACTERISTICS

NOTE:

The WD90C10 outputs have 2.0 mA maximum source and sink capability except as follows:

IRQ, RDY= 4.0 mA source and 24.0 mA sink.

$\overline{\text{MEMCS16}}$, $\overline{\text{IOCS16}}$ = 20 mA sink.

D15:0, PCLK, VID7:0, $\overline{\text{ROM16}}$ = 8.0 mA source/sink.

$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE0}}$, $\overline{\text{WE1}}$, $\overline{\text{OE}}$, MA8:0, MD15:0 = 1.0 mA source/sink.

6.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters
presented in this section:

All units are in nanoseconds
$C_L = 20$ pF unless otherwise noted

NUMBER	PARAMETER	MIN	MAX	NOTES
	RESET TIMING			
1	Reset Pulse Width	10t		t = 1/MCLK
2	MD Setup to RSET low	50		
3	MD Hold from RSET low	30		
4	RSET low to first IOW	10t		
	CLOCK TIMING			
1	VCLK Period	t		t = 1/VCLK
2	VCLK high	0.4t	0.6t	@1.4V
3	VCLK low	0.4t	0.6t	@1.4V
4*	Clock Rise Time		3	0.8V - 2.0V
5*	Clock Fall Time		3	0.8V - 2.0V
6	VCLK to PCLK Delay	8	30	45 ns @ 120 pF load up to 30MHz
7a	VCLK to Hsync Delay	8	35	
7b	VCLK to Vsync Delay	8	35	
7c	VCLK to BLNK Delay	8	30	
7d	VCLK to VID(7:0) Delay	8	30	45 ns @ 120 pF load up to 30 MHz
8	MCLK period	24	27	
9	MCLK high	10	17	@ 1.4V
10	MCLK low	10	17	@ 1.4V
11	VID (7:0) setup to PCLK	3		
12	VID (7:0) hold from PCLK	3		

TABLE 4. AC TIMING CHARACTERISTICS

* Apply to both VCLK and MCLK.

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE AT MODE TIMING			
1	EMEM setup to $\overline{MRD}$, $\overline{MWR}$ low	20		
2	EMEM hold from $\overline{MRD}$,$\overline{MWR}$ high	15		
3a	A(23:0) setup to $\overline{MRD}$,$\overline{MWR}$ low	20		
3b	A(15:0) setup to $\overline{IOR}$,$\overline{IOW}$ low	20		
3c	$\overline{BHE}$ setup to $\overline{MRD}$,$\overline{MWR}$,$\overline{IOR}$,$\overline{IOW}$ low	20		
4a	A(23:0) hold from $\overline{MRD}$, $\overline{MWR}$ low	15		
4b	A(15:0) hold from $\overline{IOR}$, $\overline{IOW}$ low	15		
4c	$\overline{BHE}$ hold from $\overline{MRD}$,$\overline{MWR}$,$\overline{IOR}$,$\overline{IOW}$ low	15		
5	$\overline{EIO}$ setup to $\overline{IOR}$/$\overline{IOW}$ low	20		
6	$\overline{EIO}$ hold from $\overline{IOR}$/$\overline{IOW}$ high	15		
7	EDBUFxN low from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ low		38	
8	EDBUFxN high from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ high		38	
9	DIR high from $\overline{IOR}$,$\overline{MRD}$ low		38	
10	DIR hold from $\overline{IOR}$ and $\overline{MRD}$ high		38	
11	D(15:0) write data setup to $\overline{IOW}$ & $\overline{MWR}$ high	30		
12a	D(15:0) read data hold from $\overline{IOR}$ high		30	
12b	D(15:0) read data hold from $\overline{MRD}$ high		30	
12c	D(15:0) write data hold from $\overline{IOW}$ high	15		
12d	D(15:0) write data hold from $\overline{MWR}$ high	15		
13a	D(15:0) read data valid from $\overline{IOR}$ low		90	C_L = 70 pF
13b	D(15:0) write data valid after $\overline{MWR}$ low		2t	t= 1/MCLK
14	RDY high from $\overline{MWR}$/$\overline{MRD}$ low *(max is for standard VGA modes)*	10	2.45 µs	
15*	Memory read data valid from RDY high		40	C_L = 70 pF
16	RDY low from $\overline{MWR}$/$\overline{MRD}$ low	10	30	C_L = 100 pF
17	RDY tristate from $\overline{MWR}$/$\overline{MRD}$ high	10	30	C_L = 100 pF
18	$\overline{EBROM}$ low from valid A(23:15)		40	
19	$\overline{EBROM}$ hold from $\overline{MRD}$ high		40	
20a	$\overline{WPLT}$ low from $\overline{IOW}$ low		30	
20b	$\overline{RPLT}$ low from $\overline{IOR}$ low		30	
21a	$\overline{WPLT}$ high from $\overline{IOW}$ high		30	
21b	$\overline{RPLT}$ high from $\overline{IOR}$ high		30	
22	$\overline{EBROM}$ low from $\overline{IOW}$ low (46E8H port)		40	
23	$\overline{EBROM}$ high from $\overline{IOW}$ high (46E8H port)		40	
24	VCLK1 low from $\overline{IOW}$ low (3C2 port)		30	
25	VCLK1 high from $\overline{IOW}$ high (3C2 port)		30	
26	A(15:0) valid to $\overline{IOCS16}$ low		40	C_L = 100 pF
27	$\overline{IOCS16}$ hold from $\overline{IOW}$ high		40	C_L = 100 pF
28	A(23:17) valid to $\overline{MEMCS16}$ low		40	C_L = 100 pF
29	$\overline{MEMCS16}$ hold after valid A(23:17)		40	C_L = 100 pF

TABLE 4. AC TIMING CHARACTERISTICS (CONT)

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE MICRO CHANNEL MODE TIMING			
1	A(23:0),EMEM,$\overline{\text{BHE}}$ setup to $\overline{\text{CMD}}$ low	20		
2	A(23:0),EMEM,$\overline{\text{BHE}}$ hold from $\overline{\text{CMD}}$ low	15		
3	$\overline{\text{CDSETUP}}$,EIO setup to $\overline{\text{CMD}}$ low	20		
4	$\overline{\text{CDSETUP}}$,EIO hold from $\overline{\text{CMD}}$ low	15		
5	STATUS setup to $\overline{\text{CMD}}$ low	20		
6	STATUS hold from $\overline{\text{CMD}}$ low	15		
7	$\overline{\text{EDBUFH}}$, $\overline{\text{EDBUFL}}$ low from $\overline{\text{CMD}}$ low		38	
8	$\overline{\text{EDBUFH}}$, $\overline{\text{EDBUFL}}$ high from $\overline{\text{CMD}}$ high		38	
9	DIR active from $\overline{\text{CMD}}$ low		38	
10	DIR inactive from $\overline{\text{CMD}}$ high		38	
11	$\overline{\text{CSFB}}$ delay from valid address/status		40	CL = 100 pF
12	$\overline{\text{CSFB}}$ hold from $\overline{\text{CMD}}$ high (I/O cycle)		30	CL = 100 pF
13	$\overline{\text{CSFB}}$ hold from invalid address (memory cycle)		30	CL = 100 pF
14	$\overline{\text{CDDS16}}$ delay from valid address		40	
15	$\overline{\text{CDDS16}}$ hold from invalid address		30	
16	D(15:0) I/O write data setup to $\overline{\text{CMD}}$ high		30	
17a	D(15:0) I/O Write data hold after $\overline{\text{CMD}}$ high	15		
17b	D(15:0) Memory Write data hold after $\overline{\text{CMD}}$ high	0		
17c	D(15:0) I/O Read data hold from $\overline{\text{CMD}}$ high	5	20	CL = 70 pF
17d	D(15:0) Memory Read data hold from $\overline{\text{CMD}}$ high	5	20	C_L = 70 pF
18a	D(15:0) Memory Write data valid after $\overline{\text{CMD}}$ low		50	
18b	D(15:0) I/O Read data valid from $\overline{\text{CMD}}$ low		90	C_L = 70 pF
19	RDY high delay from $\overline{\text{CMD}}$ low	0	2.45µs	
20*	D(15:0) Memory Read Data valid from RDY high		40	C_L = 70 pF
21	$\overline{\text{CMD}}$ high (inactive)	2t+15		
22	RDY low delay from valid address/status	10	30	
23	$\overline{\text{EBROM}}$ low from valid address		40	
24	$\overline{\text{EBROM}}$ high from $\overline{\text{CMD}}$ high		30	
25	$\overline{\text{WPLT}}$/$\overline{\text{RPLT}}$ low from $\overline{\text{CMD}}$ low		30	
26	$\overline{\text{WPLT}}$/$\overline{\text{RPLT}}$ high from $\overline{\text{CMD}}$ high		30	
27	VCLK1 low from $\overline{\text{CMD}}$ low (3C2 port)		30	
28	VCLK1 high from $\overline{\text{CMD}}$ high (3C2 port)		30	

TABLE 4. AC TIMING CHARACTERISTICS (CONT)

* Depends on setting of 3C5, Index 11, bit 4, 3.

0 0   max 40 ns
0 1   max 40 ns + 1t
1 0   max 40 ns + 1t
1 1   max 40 ns - 1t

(t = 1/MCLK)

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM TIMING			
1	$\overline{RAS}$ cycle time	6t	See Note	
2	$\overline{RAS}$ pulse width low	3.5t-6	See Note	
3	$\overline{RAS}$ high time (precharge)	2.5t+6		
4	$\overline{RAS}$ low to $\overline{CAS}$ low	2.5t-9	2.5t -6	
5	$\overline{CAS}$ cycle time	2t	2t	
6	$\overline{CAS}$ pulse width low	1t	1t	
7	$\overline{CAS}$ high time (precharge)	1t	1t	
8	Row address setup to $\overline{RAS}$ low	1.5t-10	1t	
9	Row address hold time from $\overline{RAS}$ low	1t-6	1t+10	
10	Column address setup to $\overline{CAS}$ low	1t-10	1 t	
11	Column address hold from $\overline{CAS}$ low	1t	1t+10	
12	Read Data valid before $\overline{CAS}$ high	2		
13	Read data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t-21	1.5t	
15	Write Data hold after $\overline{CAS}$ low	1t-5	1t	
16	$\overline{WE0}$ low setup $\overline{CAS}$ low	1t-5	1t+5	
17	$\overline{WE0}$ low hold after $\overline{CAS}$ high	0	10	
18	$\overline{OE}$ high before $\overline{WE0}$ low	2t-5	2t+5	
19	$\overline{OE}$ low after $\overline{WE0}$ high	1t-5	1t+5	

MCLK edge to $\overline{RAS}$,$\overline{CAS}$, MA(8:0) edge delay may be up to 40 ns

Notes:
Page-mode CRT reads may be 4-32 $\overline{CAS}$ cycles.
CPU writes use 1-4 $\overline{CAS}$ cycles in Page-mode.
CPU reads use 4 $\overline{CAS}$ cycles in Page-mode.

t = 1/MCLK
It is recommended that MCLK = 37.5 MHz for 80 ns DRAM with longer RAS precharge. MCLK = 40 MHz for 80 ns DRAM with shorter RAS precharge. This can be accomplished with selected DRAMs.

TABLE 4. AC TIMING CHARACTERISTICS (CONT)

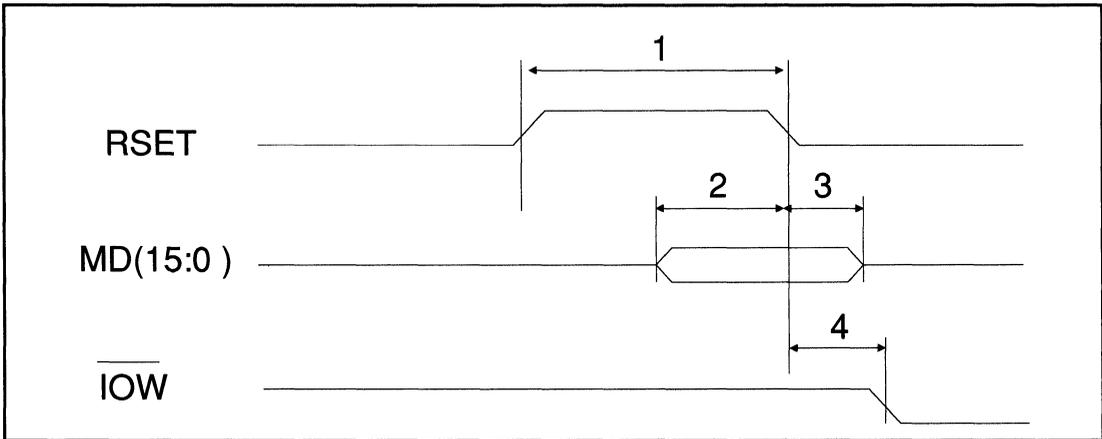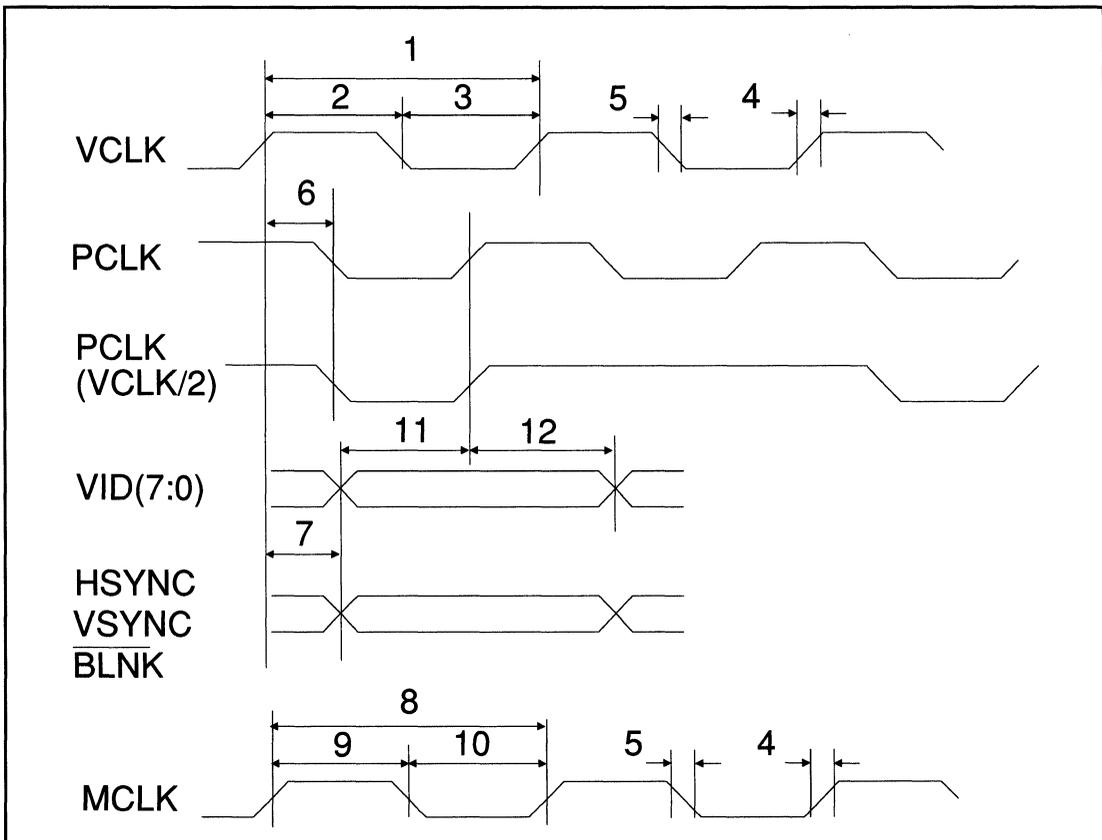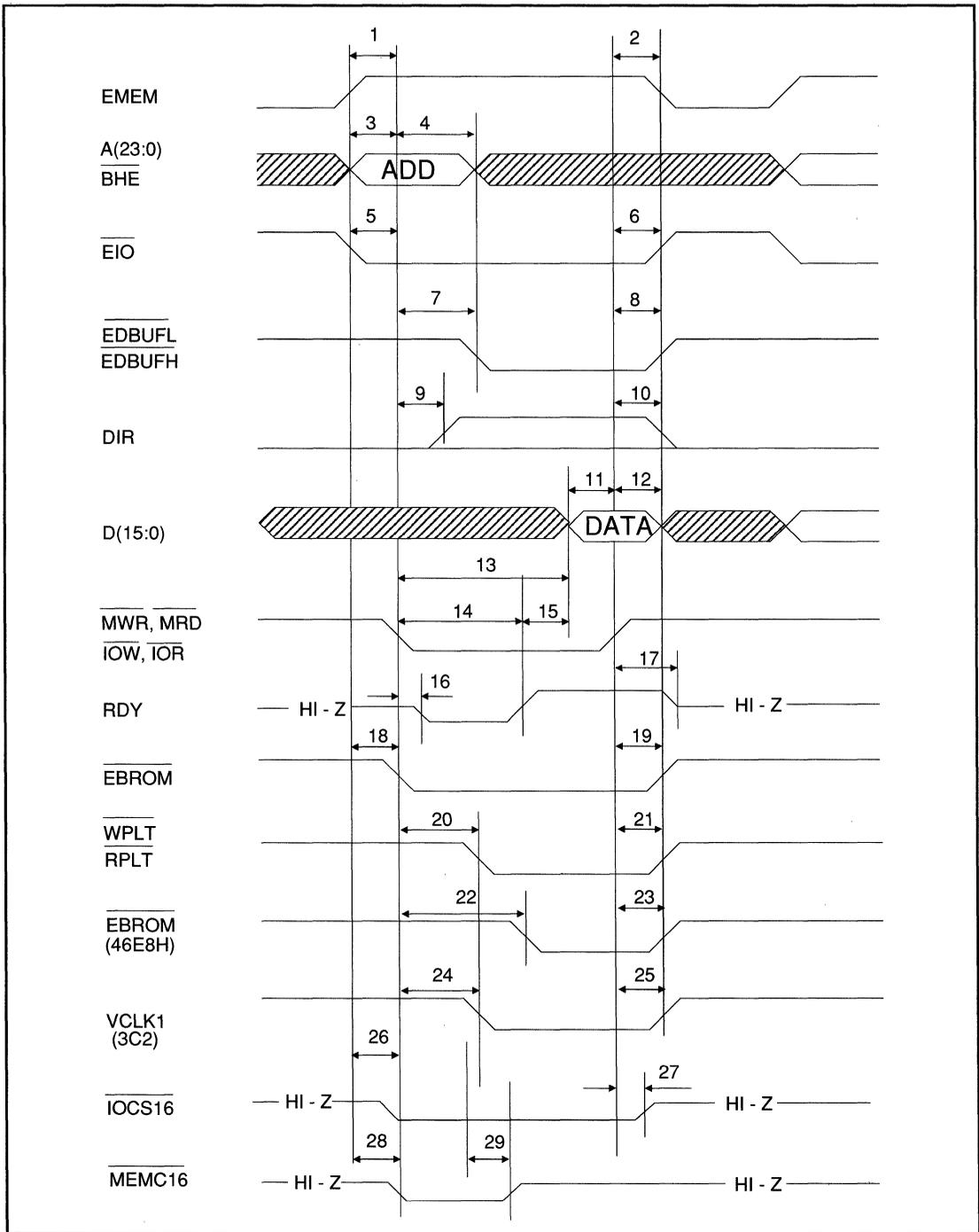**FIGURE 4. RESET TIMING**

FIGURE 5. CLOCK AND VIDEO TIMING

FIGURE 6. AT MODE BUS TIMING
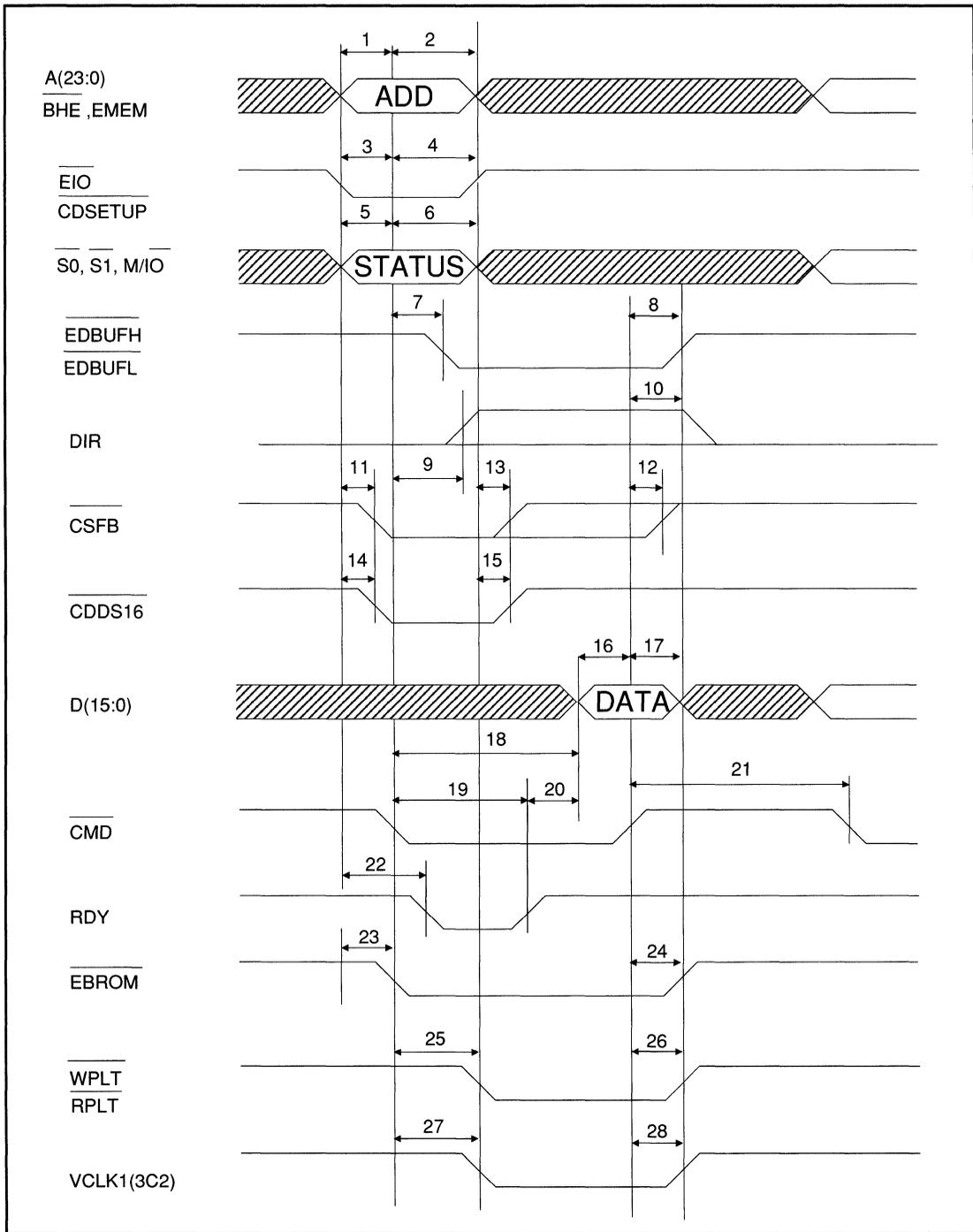
FIGURE 7. MICRO CHANNEL MODE BUS TIMING

ADVANCE INFORMATION 10/26/90
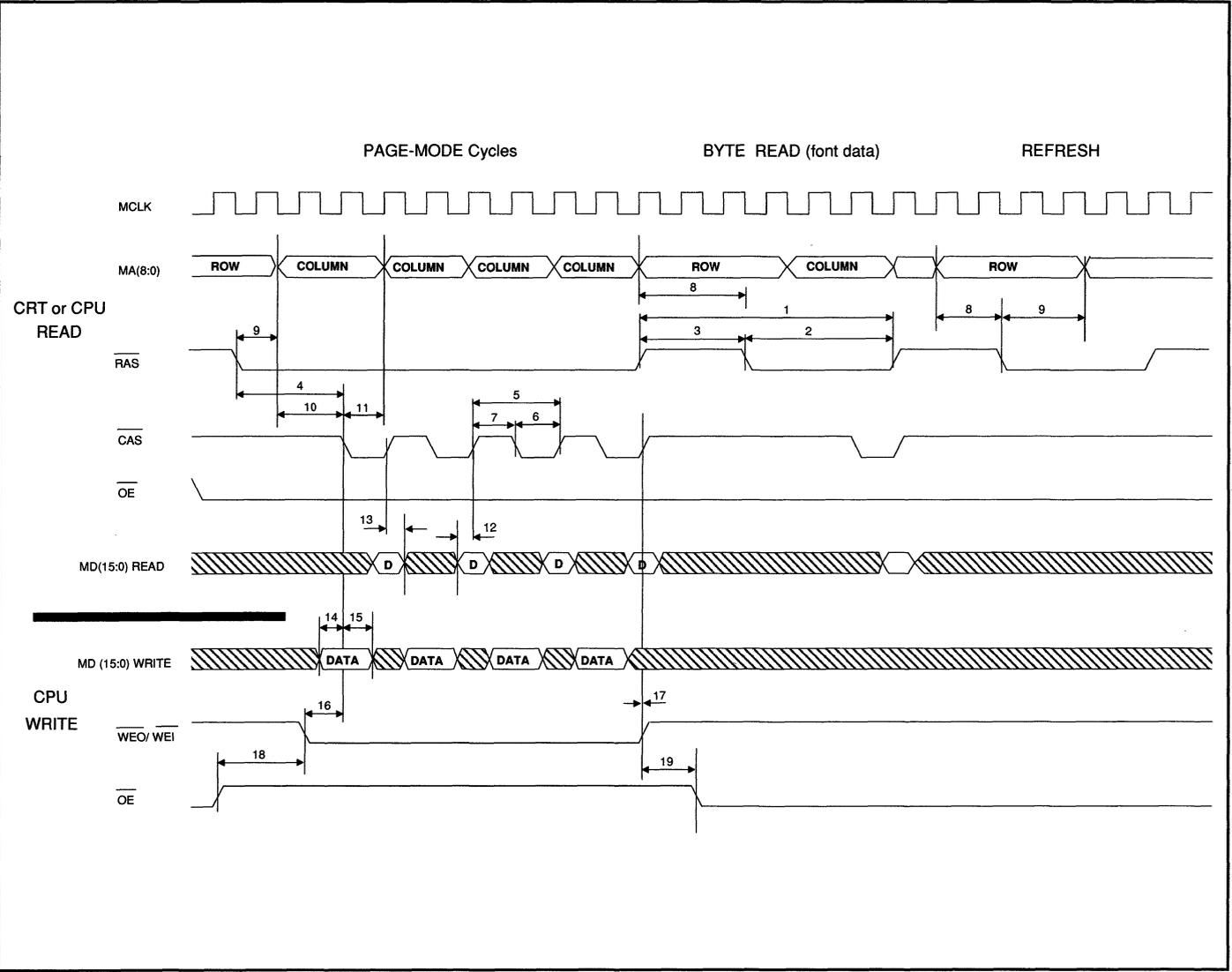
FIGURE 8. DRAM TIMING

7.0   WD90C10 REGISTERS

All the standard IBM registers incorporated inside the WD90C10 are functionally equivalent to the VGA implementation while additional Western Digital registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA registers in greater detail, followed by the VGA/EGA difference section and PR registers description. For more information, refer to the reference literature.

7.1   VGA REGISTERS SUMMARY

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
*Video Subsystem Enable	RW			3C3
AT Mode Setup and Enable	W			46E8
Setup Video Enable	RW			102
* I/O Port 3C3 can be used to replace 46E8 (if CNF (9) = 0) for setup in AT mode. In Micro Channel mode, writes to 3C3, bit 0 = 1 enables memory and I/O address decoding.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Read Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

1. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.
2. All Register addresses are in hex.

TABLE 5. VGA REGISTERS SUMMARY

7.2   PR REGISTERS SUMMARY

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3X5.31- 3X5.3F	RW	3B5.31 - 3B5.3F	3D5.31 - 3D5.3F
** CNF Configuration	-----	-----	-----
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21 Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR30 Memory Interface and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12

NOTE:

All of the PR Registers may be read/write protected. Refer to the PR Registers' description for more details.

7.3   COMPATIBILITY REGISTERS
       SUMMARY

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers.
4. ** = This register is loaded during power on.

7.4   VGA REGISTERS

Throughout this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

7.5   GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:

1. Reserved bits should be set to zero.

2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

> 0 = B in Monochrome Modes

> 1 = D in Color Modes

7.5.1   Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0= Positive vertical sync polarity.
1= Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0= Positive horizontal sync polarity.
1= Negative horizontal sync polarity.

NOTE:

*These bits determined the vertical size of the frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0-5, one memory page is selected from the two 64KB pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection.
Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0= CRTC and status addresses for MDA mode (3BX).
1= CRTC and status addresses for CGA mode (3DX).

**7.5.2 Input Status Register 0,
Read Only Port = 3C2**

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode. MDET monitor status (pin 112) is sampled and can be read from this bit.

Bit(3:0)

Reserved.

7.5.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0= Vertical frame is displayed.
1= Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

7.5.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control:
0: Vsync output enabled
1: Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved

7.6 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to zero.

7.6.1   Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

7.6.2   Reset Register, Read/Write Port = 3C5, Index = 00

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

7.6.3   Clocking Mode Register, Read/Write Port = 3C5, Index = 01

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on bit 2.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

Bit 3

Dot Clock Selection
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2

Shift Load. Effective only if bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.

Commands Sequencer to generate 8 or 9 dot wide character clock.

0 = 9 dot wide character clock.

1 = 8 dot wide character clock.

7.6.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing To Memory Maps (0-3) respectively.

0 = Writing to maps (0-3) disallowed.

1 = Maps (0-3) accessible.

7.6.5 Character Map Select Register Read/Write Port = 3C5, Index = 03

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text modes is redefined to control switching between character sets. A 0 selects character map B. A 1 selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.

The Most Significant Bit (MSB) of character map A along with bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit 4

Character Map B MSB Select.
The MSB of character map B along with bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit(3:2)

Character Map Select A.
Refer to bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to bit 4 table.

**7.6.6   Memory Mode Register,
            Read/Write Port = 3C5, Index = 04**

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.
0 = 64 KB of video memory.
1 = Greater than 64KB of memory for VGA/EGA modes.

Bit 0

Reserved.

7.7   CRT CONTROLLER REGISTERS

PORT	INDEX	VGA REGISTER NAME	*6845 REG NAME
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	+
3?5	03	End Horizontal Blanking	+
3?5	04	Start Horizontal Retrace	+
3?5	05	End Horizontal Retrace	+
3?5	06	Vertical Total	+Vert. Disp.
3?5	07	Overflow	+
3?5	08	Preset Row Scan	+
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	+
3?5	14	Underline Location	+
3?5	15	Start Vertical Blank	+
3?5	16	End Vertical Blank	+
3?5	17	CRTC Mode Control	+
3?5	18	Line Compare	+

TABLE 6. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0=B in Monochrome Modes and
1=D in Color Modes

2. "*" 6845 Mode Registers are defined and explained in greater in the reference literature.

3. "+" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

7.7.1 CRT Address Register Read/Write Port = 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

7.7.2 Horizontal Total Register Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

Bit(7:0)

Count Plus Retrace Less 5.

In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

7.7.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

The total displayed characters less one are programmed in this register. This register is locked if PR3(5) = 1 or the Vertical Retrace End Register bit 7= 1.

7.7.4 Start Horizontal Blanking Register Read/Write Port = 3?5, Index = 02H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

7.7.5 End Horizontal Blanking Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

Bit 7

Reserved

Bit(6:5)

Display Enable Signal Skew Control.
They define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

End Horizontal Blanking.

End Horizontal Blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the most significant bit is the End Horizontal Retrace Register (Index 05H) bit 7.

7.7.6   Start Horizontal Retrace Pulse Register Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.

Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

7.7.7   End Horizontal Retrace Register Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit 7

MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit(6:5)

Horizontal Retrace Delay.

These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace Pulse Width "W".

Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

7.7.8   Vertical Total Register Read/Write Port = 3?5, Index = 06H

BIT	FUNCTION
7 - 0	Vertical Total Scan Lines

Bit(7:0)

Raster Scan Line Total Less 2.

The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5 respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 - bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register bit 7 = 1.

7.7.9 Overflow Vertical Register
Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vert. Ret. Start Bit 9
6	Vert. Display Enable End Bit 9
5	Vert. Total Bit 9
4	Line Compare Bit 8
3	Start Vert. Blank Bit 8
2	Vert. Ret. Start Bit 8
1	Vert. Display Enable End Bit 8
0	Vert. Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (index = 10H).

**Bit 6

Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5

Vertical Total Bit 9 (index = 06H).

Bit 4

Line Compare Bit 8 (index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (index =15H).

++Bit 2

Vertical Retrace Start Bit 8 (index = 10H).

**Bit 1

Vertical Display Enable End Bit 8 (index = 12)

++ Bit 0

Vertical Total Bit 8 (index = 06H)

NOTES:

+ This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register bit 7 = 1.

7.7.10 Preset Row Scan Register
Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7

Reserved.

Bit(6:5)

Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit(4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

7.7.11   Maximum Scan Line Register Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare bit 9
5	Start Vertical Blank bit 9
4 - 0	Maximum Scan Line

Bit 7

200 To 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

7.7.12   Cursor Start Register Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0=Cursor on.
1=Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

7.7.13   Cursor End Register Read/Write Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7
Reserved.

Bit(6:5)

Cursor Skew Bits.

Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

Cursor End Scanline

These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

7.7.14 Start Address High Register
Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits.

Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0DH. The PR Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 & 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

7.7.15 Start Address Low Register
Read/Write Port = 3?5H,
Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

9.7.16 Cursor Location High Register
Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.

The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

7.7.17 Cursor Location Low Register
Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.

The lower order eight bits of the 16 bit video memory address in VGA or 6845 mode.

7.7.18 Vertical Retrace Start Register Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 - 0 as the light pen read back value, and bits 6 an 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

7.7.19 Vertical Retrace End Register Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) and internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

7.7.20 Vertical Display Enable End Register Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower eight bits)

Bit(7:0)

Vertical Display Enable End Lower Eight Bits.
The eight lower bits of ten bit register that defines where the active display frame ends.
The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6 respectively.

7.7.21 Offset Register Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

7.7.22 Underline Location Register Read/Write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

7.7.23 Start Vertical Blank Register
Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

7.7.24 End Vertical Blank Register
Read/Write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank inactive Count.
End Vertical Blank is an 8 bit value calculated as follows:
8 Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

7.7.25 CRT Mode Control Register
Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:

* See bit 5, defining address wrap. This table is only applicable when PR Register PR1 bits 7 and 6 equal zero, or PR16 bit 1 equals one.

The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.

0 = In word address mode, this bit enables bit 13 to appear at MA0, otherwise bit 0 appears on MA0.

1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2

0 = Character clock increments memory address counter.

1 = Character clock divided by 2 increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select For Vertical Timing Counter.
0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.
0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller compatibility mode support for CGA operation.
0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

7.7.26 Line Compare Register
Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower Eight Bits.
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

7.8   GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE:
1. Reserved bits should be set to zero.

7.8.1   Graphics Index Register, Read/Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

7.8.2 Set/Reset Register, Read/Write Port 3CF, Index = 00

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:
0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE:
*The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

7.8.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

7.8.4 Color Compare Register, Read/Write PORT 3CF, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

7.8.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data un-modified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

7.8.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.
These bits select memory map in system read operations. It has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 & 1 or value 10b or 11 to select the chained maps 2 & 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

7.8.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.
0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.
1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.
0 = Map 0 - Map 3 data is placed into shift registers for normal operations.
1 = For CGA graphics mode compatibility, even numbered bits from all of the maps are shifted out of even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.

0 = normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.

The following table defines the four write modes.

BIT 1	BIT 0	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

7.8.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A) is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

7.8.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.

0 = Disable color compare operation.
1 = Enable color compare operation.

7.8.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

7.9 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:
1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as shown below.

0 = B in Monochrome Modes and
1 = D in Color Modes

7.9.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits

NOTE:
The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read thru address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0, but does not toggle for reads to address 3C1.

7.9.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table
below.

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

7.9.3 Attribute Mode Control Register Read Port 3C1/Write Port 3C0, Index = 10

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select
0 = VID5 and VID4 palette register outputs are
selected.
1 = Color Select Register (index 14H) bits 1 and 0
are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width
0 = Disable 256 color mode pixel width. The
PCLK output is the same as the internal dot clock
rate.

1 = Enable pixel width for 256 color mode. The
PCLK output is the internal dot clock divided by
two.

Bit 5

PEL Panning Compatibility
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL
Panning Register.
1 = Allows a successful line compare to disable
the PEL Panning Register and also bits 5 and 6 of
the CRT Controller Register 08 until VSYNC oc-
curs. Allows pixel panning of a selected portion of
the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of
the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not
utilize line graphics character codes.
0 = Forces ninth dot to be the same color as
background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth
dot character is forced to be identical to the eighth
character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

7.9.4 Overscan Color Register
Read Port 3C1/Write Port 3C0,
Index = 11

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)
Overscan/Border Color.
They determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

7.9.5 Color Plane Enable Register
Read Port 3C1/Write Port 3C0,
Index = 12

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)
Reserved.

Bit(5:4)
Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)
Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

7.9.6 Horizontal Pel Panning Register Read Port 3C1/Write Port 3C0, Index = 13

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7.9.7 Color Select Register Read Port 3C1/Write Port 3CO, Index = 14

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

7.10 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes

7.10.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable Blinking
1 = Enable Blinking

Bit 4

Reserved.

Bit 3

Video enable.
0 = Video Disable
1 = Video activated

Bit 2

Reserved.

Bit 1

Port 3BFH enable.
0 = Prevents setting of Port 3BF bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode. Should be 1.
0 = High resolution disabled.
1 = High resolution is enabled.

7.10.2 Hercules Registers

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BF. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8 overrides the write port 3BF functions defined by its bits 0 and 1. The associated details are shown below.

7.10.3 Enable Mode Register 3B8

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit (6:2,0)

Not Applicable.

Bit 1

Port 3BF Bit 0 Override.
0 = Prevents setting of Port 3BF bit 0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BF bit 0 to switch for the alpha or graphics mode selection.

7.10.4 Hercules Compatibility Register Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) bit 7 selects the displayed memory page address in the graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

7.10.5 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 2

B/W or Color Display Mode.
0 = Color Mode Selected.
1 = B/W Mode Selected.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

7.10.6 CGA Color Select Register Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 2

Red Border/Background
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

7.10.7 CRT Status Register MDA Operation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

7.10.8 CRT Status Register CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

7.10.9 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 KB length).
1 = Display memory address starts at BC00:0H (16 KB length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode.
A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

7.11 WD90C10 PR REGISTERS

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3X5.31- 3X5.3F	RW	3B5.31 - 3B5.3F	3D5.31 - 3D5.3F
CNF Configuration (loaded during power-on)	-----	-----	-----
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21 Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR30 Memory Interface and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12

NOTE:
All of the PR Registers may be read/write protected.

TABLE 7. PR REGISTERS SUMMARY

The WD90C10 has additional features that enhance the performance and functions of the Western Digital Imaging PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C10 architecture is optimized with additional I/O registers.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES:

1. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.

2. PR register notation - XXX.YY where XXX is the data port address and YY is the register index e.g. 3CF.0F implies 0F--3CEH (Select Index register) followed by (Data byte) -- 3CF (Data Port).

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101; a register remains unlocked until any other value is written to the unlocked register.   Registers PR0 through PR5 are readable only if PR4 bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17 load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power on reset except where noted.

7.11.1 Address Offset Registers PROA & PROB

PROA - Address Offset Register A
Read/Write Port = 3CF, Index = 09

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PROB - Address Offset Register B
Read/Write Port = 3CF, Index = 0A

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C10 can control up to 512 Kbytes of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000H and ends at BFFFFH. To help VGA to reach the memory beyond this range, the WD90C10 has two CPU address offset registers PROA and PROB which can be used to support more than 128 Kbytes of linear display memory address space.

The contents of PROA (bit 6:0) or PROB (bit 6:0) are always added to the CPU address A(18:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture, PROA and PROB will then provide 4 Kbyte segmentation of the display memory. (Increment PROA or PROB by one of its equivalents to jump from a 4 Kbyte segment to another 4 Kbyte segment of the display memory.)

PROA and PROB are all set to zero value at power on reset. There are two ways to control whether PROA or PROB get added into CPU address.

- **Sequencer Extension Register 3C5 (index 11) bit 7 = 0.**

PROA is the primary offset register being added with the CPU address. PR1, bit 3 enables PROB which becomes the secondary offset register. If PR1, bit 3 = 1 and Graphics Controller index 6, bits 3:2 = 00b, A000:0 for 128K, then PROA will offset the CPU address from B000:0H to BFFF:FH while PROB offsets the CPU address from A000:0H to AFFF:FH. If PR1, bit 3 = 1 and Graphics Controller index 6, bits 3:2 = 01(A000:0H for 64K), then PROA will offset the CPU address from A800:0H to AFFF:FH while PROB offsets the CPU address from A000:0H - A7FF:FH.

- **Sequencer extension register 3C5 (index 11) bit 7 = 1.**

Both PROA and PROB are enabled. A CPU memory write will select PROB as the offset register. Otherwise, PROA is selected as the offset register.

7.11.2 PR1 - Memory Size, Read/Write Port = 3CF, Index = 0B

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Reserved
3	Enable Alternate Address Offset Register PR0B
2	16-Bit Video Memory
1	ROM Data Width
0	BIOS ROM Map Out

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(10), MD(0) using either pull-up or pull-down external resistors. Pull-up resistors on MD(10), MD(0) cause PR1(1:0) bits to be latched low.

Bits 7, 6

Memory Size.

These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits in conjunction with PR0A, PR0B, PR16 (1) select the way memory is mapped into the CPU address space. IF PR16 (1) is set to 1, the memory mapping will be set identical to the IBM VGA regardless of PR1 (7), PR1 (6).

The WD90C10 supports 512 Kbytes (four 256K by 4 DRAM) display memory. This makes it possible to support some extended graphics modes such as 640 by 480 by 256 colors and 800 by 600 by 256 colors.

The setting of these two bits will be overwritten by PR16 (1). When PR16(1) is set to 1, memory mapping will be identical to the IBM VGA (equivalent to PR1 (7,6) = 00).

The following tables list the different settings on these two bits for different memory organizations.

GRAPHICS MODE RAM ADDRESSING:

PR1(7)   PR1(6)

0   0   256K TOTAL;64K/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	CRT	WORD CPU	CRT	DBL WORD CPU	CRT
MA(17)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(16)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(4)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(3)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(2)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)
MA(1)	See note, page 61					
MA(0)	See note, page 61					

PR1(7)   **PR1(6)**

0   1   256K TOTAL;64K/PLANE; WD90C10 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	CRT	WORD CPU	CRT	DBL WORD CPU	CRT
MA(17)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(16)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(4)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(3)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(2)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

PR1(7)   **PR1(6)**

1   1   RESERVED

1   0   RESERVED

NOTES:

1. A(19:0) are WD90C10 internally modified system Addresses.

2. CA(17:0) are CRT Controller Character Address Counter Bits.

3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(2) if Graphics Register 6 bit 3 or bit 2 = 1.

4. CA(13) is selected as MA(2) if CRTC Mode Register 17 bit 5 = 0.

5. For two 256K x 4 DRAMs, MA(1) and MA(0) are used as memory plane select for 256 Kbytes.

MA(1), MA(0) =   00 select plane 0
                  01 select plane 1
                  10 select plane 2
                  11 select plane 3

Bits 5, 4

Reserved

Bit 3

Enable Alternate Address Offset Register PROB

Bit 2

Enable 16 bit bus for Video Memory
When set to 1, $\overline{MEMCS16}$ will be active low for all of the video memory cycles.

Bit 1

When set to 1 and bit 0=0, the BIOS ROM has a 16 bit data path from C000:0 - DFFF:FH ($\overline{ROM16}$ will respond to ROM access). Otherwise, the BIOS ROM has an 8 bit data path.

A pull down resistor on MD(10) will set this bit to 1 after power-on reset. This bit can also be set to 1 by an I/O write to PR1 register if the CNF(1) = 1 (2 ROMs).

Bit 0

If set to 1 the BIOS ROM is mapped out. Pull-up resistor latches 0 after power up. A pull-up on MD(0) sets this bit to 0 at power on reset.

7.11.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0C

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register & mode

Bit 6

0: VGA or EGA mode
1: Non-VGA (6845) mode

Bit 5

Character Map Select. The following functions are overridden by setting PR15(2). This bit in conjunction with PR2(2) and bit 3 of the attribute code, enables character maps from planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE:
Setting PR15(2) = 1 i.e. selecting page mode addressing overrides plane selected table shown above.

Bit(4:3)

Character clock period control

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character text mode only)
1	0	6 dots (for text modes only)
1	1	6 dots (for text modes only)

NOTE:

The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and character map select. Setting this bit to 1 enables underline for all odd values of attribute codes, e.g. Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, it locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.
Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

7.11.4 PR3 - CRT Lock Control Register Read/Write Port=3CF, Index = 0D

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

7.11.5 WD90C10 CRT Controller Register Locking

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). 11 When bit 7 is 1, CRT controller registers (R0-7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the sections below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT controller register 00 --Horizontal Total Characters per scan
CRT controller register 01 --Horizontal Display Enable End
CRT controller register 02 --Start Horizontal Blanking
CRT controller register 03 --End Horizontal Blanking
CRT controller register 04 --Start Horizontal Retrace
CRT controller register 05 --End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT controller register 07(Bit6) - Vert. Display Enable End bit 9
CRT controller register 07(Bit1) - Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT controller register 06 --- Vertical Total
CRT controller register 07(Bit7) ---Vertical Retrace Start bit 9
CRT controller register 07(Bit5) ---Vertical Total bit 9
CRT controller register 07(Bit3) ---Start Vertical Blank bit 8
CRT controller register 07(Bit2) ---Vertical Retrace Start bit 8
CRT controller register 07(Bit0) ---Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1
CRT controller register 09(Bit5) ---Start Vertical Blank bit 9
CRT controller register 10 ---Vertical Retrace Start
CRT controller register 11 [Bits(3:0)] ---Vertical Retrace End
CRT controller register 15 ---Start Vertical Blanking
CRT controller register 16 ---End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1
CRTC mode control register 17(Bit2) ---Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6

Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5

Lock horizontal timing.
Locks CRTC registers of Group 0 and 4.
Prevents attempt by applications software to un-lock Group 0 registers by setting 3?5.11 bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address registers values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 bit 7=1.

Bit 0

Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 bit 7=0.

7.11.6 PR4- Video Control Register Read/Write Port=3CF, Index = 0E

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAM-DAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$. Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15(1).

Bit 6

Select PCLK equal to VCLK.
0=PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1=PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

Bit 4

Tri-state the memory control outputs. The memory address bus MA(8:0), and all DRAM control signals are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" bit 3 of mode register 3D8, only in 80 x 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3C0/3C1 change to write-only mode if the EGA compatibility bit is set. In VGA mode (PR(4) bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, per the Attribute Controller registers definitions.

Bit 0

Extended Shift Register Control.
This register should only be used with 4 DRAMs to configure the video shift register for extended 256 color modes.

7.11.7 PR5 - General Purpose Status Bits
Read/Write Port=3CF, Index = 0F

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PRO-PR4 Unlock
1	PRO-PR4 Unlock
0	PRO-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 - PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register bits 4 through 8. Setting PR(4) bit 1 to 1, read protects registers PR0 - PR5.

Bit 7	CNF(7) [READ ONLY]
Bit 6	CNF(6) [READ ONLY]
Bit 5	CNF(5) [READ ONLY]
Bit 4	CNF(4) [READ ONLY]
Bit 3	CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits and cleared to 0 by reset. They control writing to PR registers PR0-PR4 as follows:

2 1 0	PR0-PR4
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected

7.11.8 PR10 Unlock PR11-PR17
Read/Write Port = 3?5, Index = 29

This register is READ/WRITE and cleared to 0 by reset.   PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX.   Bits (7,3), Bits(6:4), and Bits (2:0) control access to PR registers PR10-PR17. Bits 7 and 3 enable register read operation for PR10 - PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 - PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test.

7.11.9 PR11 EGA Switches Read/Write
Port = 3?5, Index = 2a

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA CONFIGURATION SWITCHES SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of the bit to be read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller as well as the Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during reads.

7.11.10 PR12 Scratch Pad Read/Write Port = 3?5, Index = 2b

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power up.

7.11.11 PR13 Interlace H/2 Start Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE:
In the above expression, HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

7.11.12 PR14 Interlace H/2 End Read/Write Port = 3?5, Index = 2d

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in MICRO CHANNEL operation.

Bit 6

Vertical double scan. This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is:

N=2(n+1)

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced mode.
Setting this bit to 1 selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.
Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 end bits (4:0). Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

7.11.13 PR15 Miscellaneous Control 1 Read/Write Port = 3?5, Index = 2e

BIT	FUNCTION
7	Read 46E8 Enable
6	Reserved
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable reading port 46E8H. This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

Bit 6

Reserved.

Bit 5

Latched VCLK1 and VCLK2. This bit is used only if CNF(3) = 1 which configures the VCLK1 and VCLK2 pins as outputs. Setting This bit to 1 causes outputs VCLK1 and VCLK2 to equal bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H respectively.

Bit 4

Select MCLK as video clock. Setting this bit to causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.

Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30-40%. Set this bit to 1 of 132 character mode

timing is selected (see description of PR2). Setting this bit to any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register while the map selection is determined by the bits (4:3). A pair of adjacent 8K character maps in planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.

The Character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

Note:

The above Character Map Select functions override the functions override the functions of PR2(5) and PR2(2).

This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select. This bit is used to select between two types of Display Enable timings available at output pin BLNKN if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0=BLNKN supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable border. Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

7.11.14 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2f

BIT	FUNCTION
7	External reg. 46E8H lock
6	CRTC Address count Width bit 1
5	CRTC Address Count Width bit 0
4	CRTC Address Counter Offset bit 1
3	CRTC Address Counter Offset bit 0
2	Enable Odd/Even Page bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H register.

Setting this bit to 1 causes $\overline{EBROM}$ output to be forced high (Inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.

Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64 K locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256KB
0	1	128K
1	X	64K

Bit (4:3)

CRTC Address Counter Offset
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

Bit 1

VGA Memory Mapping

Setting this bit to 1, selects 256KB IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC write strobe (3C6H - 3C9H) Programming this bit to 1 causes output WPLTN to be forced to 1 disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C10 is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

7.11.15 PR17 Miscellaneous Control 3
        Read/Write Port = 3?5, Index = 30

BIT	FUNCTION
7 - 4	Reserved
3	Map out 4K of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map out 2K of BIOS ROM

Bit (7:4)

Reserved.

Bit (3)

Map out 4K of BIOS ROM.

Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C6FF:FH. Power on reset sets this bit to 0.

Bit (2)

Enable 64K BIOS ROM.

Setting this bit to 1 enables access of the BIOS ROM in the system address range C000:0H - CFFF:FH. Power on reset sets this bit to 0.

Bit (1)

Setting this bit to a 1 locks Hercules compatibility register (I/O port 3BF). Power on reset sets this bit to 0.

Bit (0)

Map out 2K of BIOS ROM.

Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C67F:FH.

Power on reset sets this bit to 0.

7.11.16 PR20 3C5 Index 6: Unlock Sequencer Extended Registers
        (Reset State = Locked)

A value of X1X01XXXX (48H) must be loaded to allow R/W of the Sequencer Extended Registers. When the extended registers are locked, then the Sequencer index will be readable as three bits only. When unlocked, the Sequencer index reads as a full eight bits.

7.11.17 PR21 3C5 Index 7: Display Configuration Status and Scratch Pad Bits

This register provides a convenient location for determining the current VGA configuration state. This information is needed for many of the BIOS calls.

BIT	FUNCTION
7 - 4	Scratch Pad Bits
3	Status of 3C2 bit 0
2	Status of PR2 bit 6
1	Status of PR4 bit 1
0	Status of PR5 bit 3

Bits 7:4

Read/write scratch pad for any BIOS status data that may need to be saved. Reset state is 1111.

Bit 3

Reflects the setting of the I/O address select bit in the Miscellaneous Output Register.

A 1 means CGA (3Dx) addresses have been selected by this read-only bit, while a 0 means MDA (3Bx) addresses have been selected.

Bit 2

Reflects the setting of the VGA/6845 select bit in PR2 (3CF index C).

A 1 means 6845 compatibility has been selected by this read-only bit, while a 0 means VGA or EGA compatibility has been selected.

Bit 1

Reflects the setting of the VGA/EGA select bit in PR4 (3CF index E).

A 1 means EGA compatibility has been selected by this read-only bit, while a 0 means VGA was selected.

Bit 0

Reflects the setting of the Analog/TTL status bit in PR5 (3CF index F).

The video BIOS may define this as a 0 meaning an an analog monitor was selected by this read-only bit, while a 1 means a TTL-type monitor was selected.

7.11.18 PR30 3C5 Index 10
Memory Interface and FIFO Control
Register (See Note)

This register controls display memory data width and its bandwidth. All of the bits are reset to zero at power on reset.

BIT	FUNCTION
7, 6	Reserved
5	8- or 16-bit Memory data path
4	Disable 16-bit CPU interface
3	Enable write buffer extension
2	4 or 8 level FIFO
1, 0	Display memory bandwidth

Bits (7,6)

Reserved

Bit 5

This bit must be set to zero. This bit is reserved for the WD90C11 and WD90C12.

Bit 4

When set to 1, the 16-bit CPU interface is un-chained mode is disabled. This is for debug only and should be set to 0 under normal conditions.

Bit 3

When set to 1 enables the write buffer extension. This will make the write buffer effectively two deep. Should be set to 1 under normal conditions.

Bit 2

When set to 1, will set the internal FIFO to 4 levels deep. Otherwise the FIFO is 8 levels deep. In general, when 16-bits display memory is enabled (bit 1 of this register is set to 1), then the 4 level deep FIFO is recommended. In "Super VGA" mode (800 by 600 by 256 color) an 8 level deep FIFO will be required.

Bit 1, 0

These two bits can be used to adjust the display memory bandwidth. In general it is recommended that these two bits be set to 01 to accommodate most applications. These bits have no effect in any text mode. They are locked into 00 internally when a text mode is set.

00	FIFO requests for memory cycle when FIFO is:	one level empty
01	FIFO requests for memory cycle when FIFO is:	two levels empty
10	FIFO requests for memory cycle when FIFO is:	three levels empty
11	FIFO requests for memory cycle when FIFO is:	four levels empty

NOTE:
PR30 is reserved for next generation WD90C10.

7.11.19 PR31 3C5 Index 11: System Inter-
face Control (Reset State = 00H)

This register provides the control bits for the system interface. This register should be set during the Post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 will be used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY release Control 1
3	CPU Read RDY release Control 0
2	Enable Write Buffer
1	Enable 16-bit I/O Operation on Attribute Controller
0	Enable 16-bit I/O Operation on CRTC, Sequencer and Graphics Controller

Bit 7

When set to 1, the offset register PR0-A will be added to the CPU address for read cycles, while PR0-B will be added for write cycles. When cleared to 0, the offset registers operate the same as in the PVGA1B. Refer to PR0A and PR0B definitions.

Bit 6

When set to 1, system performace is improved by 10% by removing extra memory cycles on blank lines.

Bit 5

When set to 1, text mode performance will be improved.

Bit 4:3

These two bits set the CPU's RDY timing to be optimized for different system timing. For slower systems, the RDY line may be released earlier because it will take longer for the read cycle to be completed.

00 =   Power on reset condition. RDY is inserted at the end of a CPU memory cycle

01, 10 = RDY is inserted 1MCK before the end of a CPU memory cycle.

11 =   RDY is inserted 1MCK after the end of a CPU read memory cycle. RDY is inserted at the end of a memory write cycle.

For 10 MHz or slower systems, the 01 setting is recommended. For 12 MHz or faster systems, the 11 setting is recommended.

Bit 2

When set to 1, a single-level , 16-bit write buffer is enabled. This willl greatly reduce the number of wait states for CPU writes to display memory.

Bit 1

If this bit and bit 0 are both set to 1, then the Attribute Controller (3C0/3C1) is configured for 16-bit access. The index is at 3C0, while the data is at 3C1, and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for 8-bit cycles. $\overline{IOCS16}$ is asserted for all cycles to 3C0 or 3C1.

Bit 0

When set to 1, this bit enables 16-bit access to the CRTC (3?4/3?5), Sequencer (3C4/3C5), and Graphics Controller (3CE/3CF). The output $\overline{IOCS16}$ will be active for any I/O read or write to these addresses. When set at 0, the VGA I/O is all 8-bit.

7.11.20 PR32 3C5 Index 12: Miscellaneous Control 4 (Reset State = 00H)

This register provides control for several different features. Some of these features help to support Genlock of the PVGA1M to another display controller for overlay.

BIT	FUNCTION
7	Enable External Sync Mode
6	Disable Cursor Blink
5	USR1 Function Select
4	USR1 Control
3	USR0 Function Select
2	USR0 Control
1	Allow readback in backward compatible modes
0	Force standard CPU addressing in 132-column mode

Bit 7

When set to 1, $\overline{\text{EXVID}}$ is configured to input external Horizontal Sync, and $\overline{\text{EXPCLK}}$ inputs external Vertical Sync. The external HSYNC signal also synchronizes the character clock timing. In this configuration, $\overline{\text{EXVID}}$ and $\overline{\text{EXPCLK}}$ do not control the VID7:0 and PCLK output buffers. A 0 setting places this bit into its normal operation mode.

Bit 6

When set to 1, the text cursor blink will be disabled, and the cursor will remain on. This option can be used if cursor blink is not desired.

Bit 5

A 1 setting causes the USR1 output to indicate when the WD90C10 is reading font data in text mode (FONTCYC). A 0 causes the USR1 output to reflect the state of bit 4, which can be used to control new features that the system board designer may wish to add.

Bit 4

Controls the USR1 output when selected by bit 5.

Bit 3

A 1 setting causes the USR0 output to indicate that the WD90C10 is reading both the character and the attribute data from the DRAMs in text mode (TEXTCYC). USR0 will be high during the RAS cycles for character/attribute read. The DRAM data may be sampled when USR0 is high. A 0 setting causes the USR0 output to reflect the state of bit 2, which can be used to control new features that the system board designer may wish to add.

Bit 2

Controls the USR0 output when selected by bit 3.

Bit 1

When set to 1, this bit allows reading the registers that are not readable in backward compatibility modes. This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0

When set to 1, the special CPU address mapping for page mode font access in 132-column text is set for standard mapping without disturbing the display. This will be used only for special virtual VGA applications.

7.12   INTERNAL I/O PORTS

7.12.1   AT Mode Setup, Enable Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused

Bit 4

Setup
Puts WD90C10 into setup mode where only I/O port 102H is accessible.

Bit 3

Enable I/O and Memory Accesses

Bit(2:0)

Unused Internally
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0. The WD90C10 also provides an alternative port 3C3H instead of port 46E8H. If a pull down resistor is connected to MD(9) during power on reset (CNF9 = 0), then port 3C3H will be decoded instead of port 46E8H to support the same functions described above. Otherwise, port 46E8H is selected and decoded.

7.12.2   Setup Mode Video Enable (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C10 must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C10 after power on in the MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H.   In MCA mode, when the VGASETUP (EION) signal pin is active low, the WD90C10 is in setup mode and port 102H can be accessed.

7.13   VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C10. However, the $\overline{WPLT}$ and $\overline{RPLT}$ signals required by the RAMDAC are provided by the WD90C10. Setting PR(16) bit 0 to a 1 forces $\overline{WPLT}$ to a high level disabling I/O writes to the RAMDAC. Normally, the $\overline{WPLT}$ and $\overline{RPLT}$ signals to the RAMDAC are generated when the following I/O ports are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL address port (write)	Read/write port
3C7H	PEL address port (read)	Write only port
*3C7H	*DAC state (read only)	*If bits 0/1 =1, DAC in read operation. When bits 0/1=0,DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL mask (read/write)	Not to be written by application code or color look up table will be changed.
3C9H	PEL data register (read/write)	Three successive read/write bytes.

* This port is internal to the WD90C10.

7.14 CONFIGURATION BITS

Memory Data lines 15:0 are used to input configuration data at power-on reset (RST) by pullup or pulldown resistors. This configuration data then sets the bits in internal registers. Some of these bits can then be changed by software, while some are in non-writable registers. The non-writable bits set features such as bus type which are not changed after power-on.

BIT	FUNCTION
15 - 12	EGA Switches
11	A23 - A20 Connection Select
10	16-bit BIOS
9	46E8/3C3 Select
8	Display Status
7 - 4	General Purpose Status
3	Video Clock Source Control
2	Bus Architecture Select
1	ROM Configuration
0	Map out BIOS

7.14.1 WD90C10 Configuration Register Bits CNF(15:0)

CNF(15:12)

EGA CONFIGURATION SWITCHES SW4-SW1. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. PULLING DOWN MD(15:12) causes these bits to be latched LOW. PR11(7:4) are writable bits. These bits can be read as bit 4 of port 3C2H (as on a standard EGA) if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of which bit is read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE		READ
3c2 bit 3	3C2 bit 2	3C2 bit 4
0	0	PR11(7) [= EGA SW4]
0	1	PR11(6) [= EGA SW3]
1	0	PR11(5) [= EGA SW2]
1	1	PR11(4) [= EGA SW1]

CNF (11) (Refer to Figure 12)

A 4.7K pull down resistor on the pin MD 8 will set CNF(11) = 0. The pins A(22:20) should then be connected to the AT bus signals LA(19:17), unlatched CPU address. The pin A23 should be connected to the NOR of AT bus signals LA(23:20). The pins A(19:17) should be connected to AT bus SA(19:17), latched CPU address. This will allow the WD90C10 to directly drive MEMCS16 in AT bus which requires decoding of the early unlatched address LA(23:17). An external NOR is required to decode LA(23:20).

If there is no pull down resistor on MD8, the CNF(11) will be set to 1 by the internal pull up. Pins A(23:17) should be connected to AT bus signals LA(23:17). In most 80286 systems, the early address LA(23:17) is not latched during a bus operation. CNF(11) = 0 is required to ensure proper decoding of MEMCS16 without many external components. In most 80386 systems, the early address LA(23:17) is latched during a bus operation. CNF(11) = 1 is recommended for design simplification. In Micro Channel applications, CNF(11) should be set to 1.

CNF (10)

A 4.7K pull down on pin MD10 will set CNF(10) = PR1(1). Upon power-up, the pin ROM16 is enabled for 16-bit BIOS ROM decoding. Otherwise the internal pull up will set CNF(10) = PR1=0. To enable the 16-bit BIOS, PR1 must be set to 1 by writing to port 3CF (index 0B) and the CNF (1) must be 1. This bit is read/write at PR1(1).

CNF (9)

A 4.7K pull down on pin MD9 will set CNF(9) = 0. Then port 03C3 will be selected as the VGA setup and enable register instead of port 46E8 in the AT interface. Otherwise, the internal pull up will set CNF(9) = 1. Port 46E8 will be selected as VGA setup and enable register. This bit has no effect in Micro Channel applications.

CNF (8)

ANALOG/TTL DISPLAY STATUS BIT.
Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F). Suggested implementation is:

0 = Analog (VGA - compatible) display is attached
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

GENERAL PURPOSE STATUS BITS.
Bits CNF (7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched high.

CNF (3)

VIDEO CLOCK SOURCE CONTROL.
This bit cannot be written or read as I/O port pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C10 pins VCLK1 and VCLK2 as inputs or outputs.

0=For inputs.
1=For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip, during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK1 and VCLK2 outputs equal to bits 2 and 3 of the Miscellaneous output register at 3C2H respectively when PR15 bit 5 is set to 1.

CNF (2)

BUS ARCHITECTURE SELECT.
This bit cannot be written or read as I/O. Pulling down MD(2) causes CNF(2) to be latched low.

0:   Micro Channel architecture

1:   AT BUS architecture

Select CNF(2) will change PINOUT definition between AT BUS and Micro Channel bus (see PINOUT description).

PC AT BUS	I/O	Micro Channel	I/O
MEMCS16	OUT	$\overline{CDDS16}$	OUT
$\overline{ROM16}$	OUT	$\overline{CSFB}$	OUT
$\overline{EIO}$	IN	3C3D0	IN
$\overline{MRD}$	IN	M/$\overline{IO}$	IN
$\overline{MWR}$	IN	$\overline{S0}$	IN
$\overline{IOR}$	IN	$\overline{S1}$	IN
$\overline{IOW}$	IN	CMD	IN
IRQ	OUT	$\overline{IRQ}$	OUT
$\overline{IOCS16}$	OUT	CDSETUP	OUT

CNF (1)

ROM CONFIGURATION.
When set to 0, the WD90C10's data bus buffer controls are configured for 1 ROM (8 bits). An internal pullup on MD (1) sets this bit to 0 at power-on reset.
When set to 1, the WD90C10's data bus buffer controls are configured for 16-bits (as with two ROMs).
If CNF (1) = 0, then PR1(1) can not be set high. This bit can not be written or read.

CNF (0)

BIOS ROM MAPPING.
If set to 1, the BIOS ROM is mapped out. An internal pullup resistor on MD(0) sets this bit to 0 at power-on reset. An external 4.7 K ohm pulldown resistor may be used to set this bit to 1 on power-on (reset).
This bit is read/write at PR1(0).

APPENDIX

A.1   EGA MODE

For the register definitions that have not changed from the VGA modes, refer to the VGA description. Only the differences between the VGA and EGA registers are briefly described in this section. Also, refer to the prior section for VGA mode details. Not Used bits should be set to 0 unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are not covered in this procedure. These steps are briefly defined to outline the EGA mode entry.

- Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pull-up or pull-down resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.
- Unlock all the PR registers.
- Program PR2(6) to 0 for EGA mode.
- Set PR4 bit 1 to logic 1 for EGA compatibility.
- Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on pins MD(15:12). (Pull-up resistor causes logic 1 to be latched after power on reset.)
- The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 bit 4.

- If EGA is to be emulated on the IBM PS/2 type analog display, follow the suggested steps listed below:
  Initialize all the registers.
  Lock CRT controller registers.
  Force Clock Control rate of the CRT controller.
  - Set EGA emulation mode by programming:
    PR11(3)=1; Set EGA emulation on PS/2 type display
    PR14(6)=1; Vertical double scan
    PR11(2)=1; Lock clock select
    PR11(0)=1; Lock 8/9 dot timing.
    PR14(7)=1; Enable IRQ (optional)
  - Lock the PR registers PRO-PR5 and PR10-PR17.
  - Read protect PR registers.

- When EGA is required on a TTL monitor, the suggested steps are:
  - Initialize all the registers.
  - Set EGA TTL mode by programming:
    PR11(3)=0;EGA TTL
    PR14(7)=1;Enable IRQ
    PR15(6)=1;Set Low Clock
    PR14(7)=1;Enable IRQ
  - Lock PR registers PRO-PR5 and PR10-PR17
  - Read protect PR registers.

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlight all the EGA mode registers.

A1.1 EGA Registers Summary

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3?4
CRT Controller Data Reg Except the following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
Light Pen High, (Index=10)	R	3?5
Light Pen Low, (Index=11)	R	3?5
Graphics Controller Registers:		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3CO*
Attribute Controller Data Reg	WO	3CO*

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All Register addresses are in hex.
3. "?" = "B" in Monochrome modes or "D" in Color modes.
4. "*" = Identical responses from I/O ports 3C0 and 3C1.

TABLE 8. EGA REGISTERS SUMMARY

A.2   GENERAL REGISTERS

Only the general registers and the bit definitions that differ between the VGA and EGA are addressed.   Their EGA mode bit definitions are provided.

A.2.1   Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Not used.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 Mhz clock (VCLK0) is selected.
0	1	16.257 Mhz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

A.2.2   Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not used

Bit 4

EGA: The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not used = 1

A.2.3   Input Status Register 1 (READ PORT 3?A)

Bit (7)

EGA: Not used

Bit 6

EGA: Not used = 1

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: Not used = 1

Bit 1

EGA: Unused

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

A.2.4 Feature Control Register (Write Port 3?A)

Bits (7:0)

EGA: Not used

A.3 SEQUENCER REGISTERS (PORT 3C5)

A.3.1 Clocking Mode register (Index = 01)

Bits (7:4)

EGA: Not Used

Bits (3,2)

EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1

EGA: Set to zero

Bit (0)

EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

A.3.2 Character Map Select Register (Index 03)

Bits (7:4)

EGA: Not Used

Bits (3:2)

EGA: Character Map Select A

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

Bits (1:0)

EGA: Character Map Select B

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

NOTE:

1. Character Map selection from Plane 2 is determined by bit 3 of the attribute code.

A.3.3 Memory Mode Register (Index = 04)

Bits (7:3)

EGA: Not Used

Bits (2:1)

EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0

EGA: Alpha mode bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha modes and enables non-Alpha modes.

A.4   CRT CONTROLLER REGISTERS (PORT 3?5)

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. Also, "?" implies that a register is mapped into either 3B5 or 3D5, for Monochrome or Color display modes, respectively.

A.4.1   Index Register (Port = 3?4)

Bits (7:5)
EGA: Not Used.

Bits (4:0)
EGA: Five bits point to the CRT Registers Address index where the data is to be written.

A.4.2   Horizontal Total Register (Index = 00)

Bits (7:0)
EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

A.4.3   End Horizontal Blanking Register (Index = 03)

Bits (7)
EGA: Not Used.

Bits (6:5)
EGA: They define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)
EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

A.4.4   End Horizontal Retrace Register (Index = 05)

Bit 7
EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)
EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

A.4.5   Vertical Total Register (Index = 06)

Bits (7:0)
EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

A.4.6   CRT Controller Overflow Register (Index = 07)

Bits (7:5)
EGA: Not used.

Bits (4:0)
Identical to CRT Controller Overflow Register Bits (4:0) definitions in the VGA section.

A.4.7   Preset Row Scan Register (Index = 08)

Bits (7:5)
EGA: Not used.

Bits (4:0)
EGA: Same as Preset Row Scan Register Bits (4:0) definition in the VGA section.

A.4.8 Maximum Scan Line Register (Index = 09)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as maximum Scan Line Register Bits (4:0) definition in the VGA section.

A.4.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

A.4.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

A.4.11 Vertical Retrace Start Register (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

A.4.12 Vertical Retrace End Register (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not used

Bit 5

EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

A.4.13 Underline Location Register (Index = 14)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

A.4.14 End Vertical Blanking Register (Index = 16)

Bits (7:5)
EGA: Not used.

Bits (4:0)
EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

A.4.15 Mode Control Register (Index = 17)

Bits (7:5)
EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4
EGA: Not used.

Bits (3:0)
EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.5 GRAPHICS CONTROLLER REGISTERS (PORT 3CF)

A.5.1 Read Map Select Register (Index = 04)

Bits (7:3)
EGA: Not Used.

Bits (2:0)
EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

A.5.2 Mode Register (Index = 05)

Bit (7:6)
EGA: Not Used

Bits (5:2)
EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)
EGA: Binary coded write bits define the write modes per table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to VGA section
0	1	Write mode 1 - Refer to VGA section
1	0	Write mode 2 - Refer to VGA section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

A.6 ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0/3C1)

A.6.1 Palette Registers (Index = 00 through 0F)

BIT	FUNCTION
7 - 6	Not used
5 - 0	Dynamic color selection

Bits (7:6)
EGA: Not Used.

Bits (5:0)
EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

A.6.2   Mode Control Register (Index = 10)

BIT	FUNCTION
7 - 4	Not used
3 - 0	Same as Mode Control in VGA section

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.6.3   Overscan Color Register (Index = 11)

BIT	FUNCTION
7 - 6	Not used
5 - 0	Overscan color for border

Bits (7:6)

EGA: Not Used

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

A.6.4   Color Plane Enable Register (Index = 12)

BIT	FUNCTION
7 - 6	Same as Color Plane Enable - VGA
5 - 4	Video Status Multiplexer
3 - 0	Same as Color Plane Enable - VGA

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer per the table listed:

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2(Red)	VID 0 (Blue)
0	1	VID 5(SRed)	VID 4 (SGreen)
1	0	VID 3(SBlue)	VID 1 (Green)
1	1	VID 5(SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

A.6.5   Horizontal PEL Panning Register (Index = 13)

BIT	FUNCTION
7 - 4	Not used
3 - 0	Horizontal left shift of the video data in number of pixels.

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, (9 dots/character) image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

A.7   APPLICATIONS

The WD90C10 applications section is divided into various interfaces such as processor (AT or Micro Channel mode), video memory, RAMDAC, monitor, and clock.   The description and block diagrams are generic.   No attempt is made to present schematic level details.   Currently available application notes, technical briefs, and refer-enced literature at the end of the data sheet should supplement the information provided in this section.   The Figures 9 through 17 are shown along with their brief description on the subsequent pages.

Figure 9 highlights the various WD90C10 Processor, memory, and I/0 interfaces.
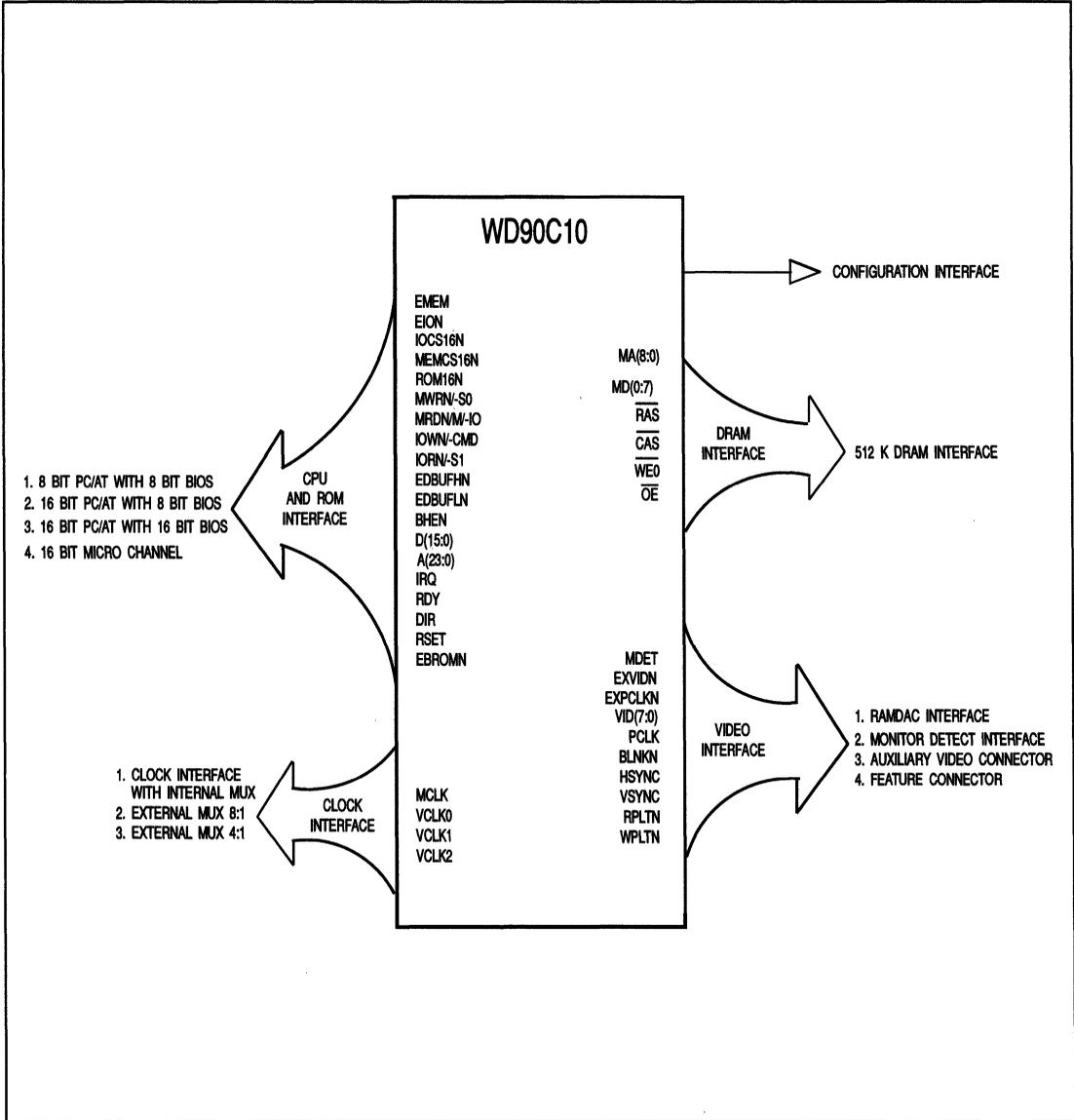
FIGURE 9. WD90C10 INTERFACES

Figure 10 shows a block diagram of the WD90C10 with 8 bit PC/AT interface using 8 bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM.
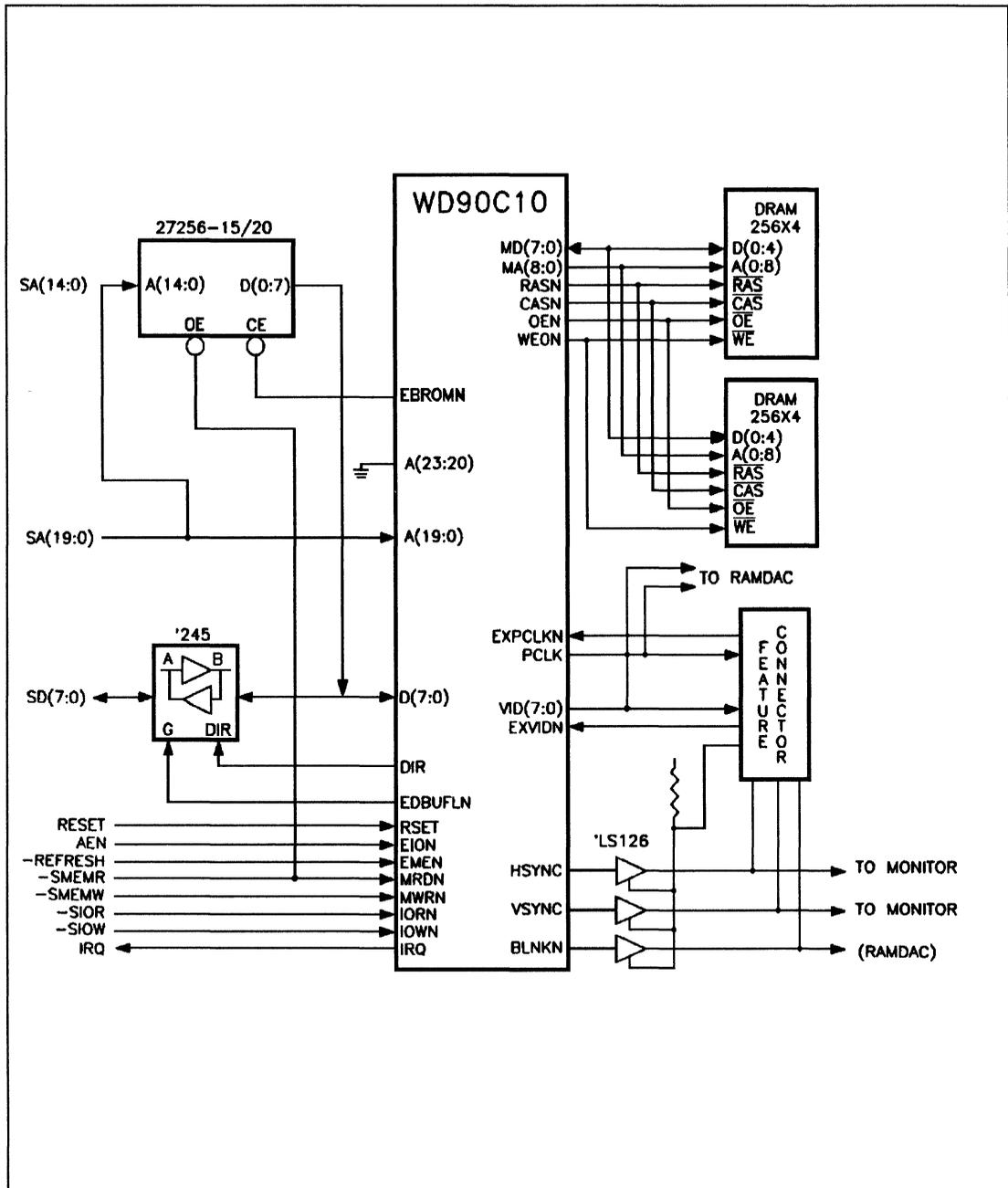

FIGURE 10. 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 11 illustrates 16-bit PC/AT interface with 8-bit BIOS using WD90C10. For 386 systems, the processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers and BIOS ROM are also shown in it.
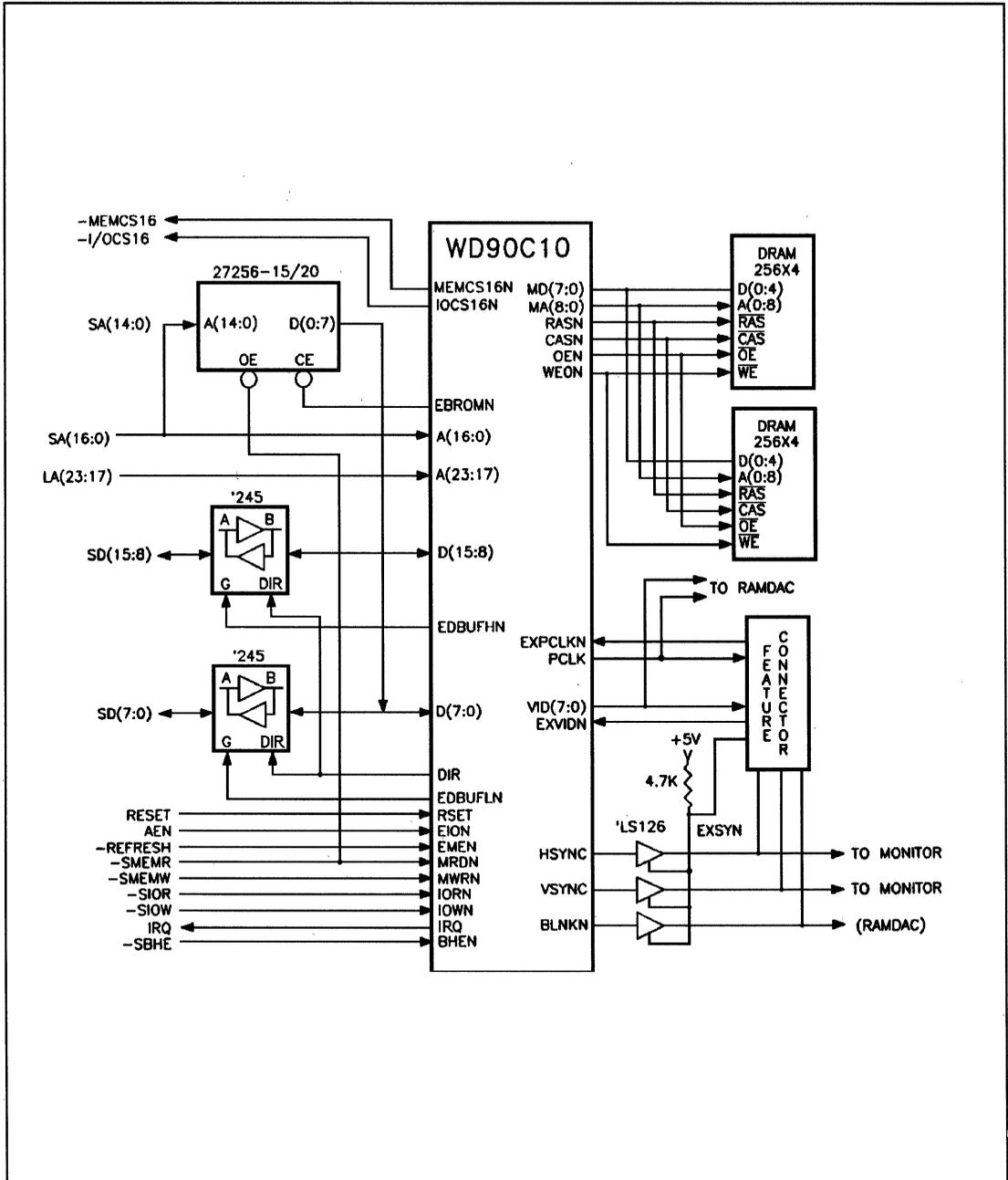

FIGURE 11. 16-BIT BIOS PC AT INTERFACE WITH 8-BIT BIOS

For 286 and some 386 systems, there may not be enough address hold time after SMEMRD or SMEMWR to generate $\overline{MEMC16}$ and $\overline{ROM16}$. Therefore, to allow continuous 16-bit memory and 16-bit BIOS access capability, configure the WD90C10 as illustrated in configuration 1. Configuration 2 can also be used, but it has some limitations.

CONFIGURATION 1:

This configuration uses a PAL to generate the $\overline{MEMC16}$ signal. This ensures 16-bit BIOS and 16-bit memory access capability at all times.

USR0 = 1   enables 16-bit memory accesses
USR1 = 1   enables 16-bit BIOS accesses

The BIOS initializes the USR outputs. The user must also set PR1, bit 1 and PR1, bit 2 to the values that correspond to the USR1 and USR0 settings, respectively.   Refer to PR register descriptions.

PAL EQUATIONS

$\overline{Y1}$= USR0 * LA17 * $\overline{LA18}$ * LA19 * $\overline{LA20}$ * $\overline{LA21}$ * $\overline{LA22}$ * $\overline{LA23}$ + USR1 * $\overline{LA17}$ * LA18 * LA19 * LA20 * $\overline{LA21}$ * $\overline{LA22}$ * $\overline{LA23}$ * SA[15] * $\overline{SA[16]}$

Y2=0
Y2 * TRST=Y1 (Output enabled when $\overline{Y1}$=0)

The first term of Y1 decodes the video region A0000 - BFFFF. The second term decodes the BIOS region C0000 - C7FFF.

CONFIGURATION 2:

Use of a PAL to generate $\overline{MEMC16}$ and discrete logic to decode the BIOS and provide 16-bit ROM accesses. USR0=1 enables 16-bit memory accesses.

This 16-bit BIOS implementation is limited with high bus speeds because ROM16 is delayed 40 ns from address valid (refer to timing information). For high bus speeds, 16-bit ROM accesses may not always occur in AT bus environments.

PAL has tri-state outputs.

Set the PR1, bits 1 and 2 to correspond to the USR0 setting and ROM data path respectively.

PAL EQUATIONS:

$\overline{Y1}$ = USR0 * LA17 * $\overline{LA18}$ * LA19 * $\overline{LA20}$ * $\overline{LA21}$ * $\overline{LA22}$ * $\overline{LA23}$ (A0000 - BFFFF)
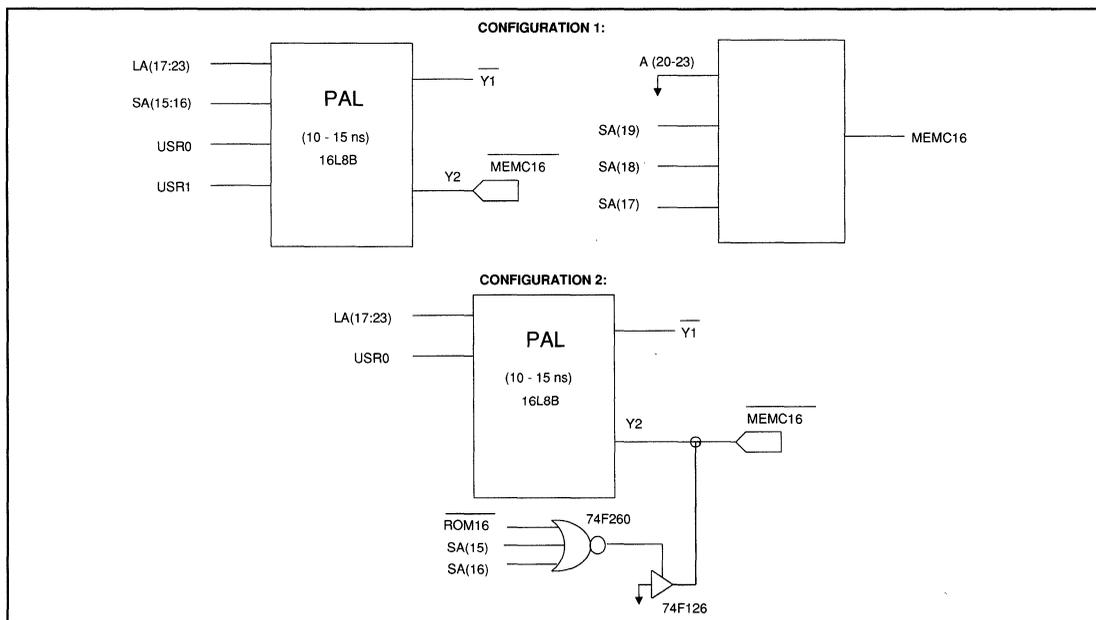
Y2 = 0,Y2 * TRST = Y1

FIGURE 12. WD90C10 INTERFACE FOR 286 OR 386-BASED SYSTEMS

Figure 13 describes a 16-bit PC/AT interface with 16-bit BIOS ROM implementation using the WD90C10. The system data bus SD(15:0), address and data bus buffers are presented. Also, $\overline{\text{MEMCS16}}$ implementation is limited to certain bus speeds as SA15 and SA16 are used for the 16-bit BIOS. Refer to Figure 12 for 286-based systems.

FIGURE 13. 16-BIT PC AT INTERFACE WITH 16-BIT BIOS
(WITH OPTIONAL 512 KBYTES: 4- 256K BY 4 DRAM)

Figure 14 illustrates the WD90C10 and 16-bit
Micro Channel interface. 3C3.D0 is output of port
3C3H bit 0 VGA Subsystem Enable Register.
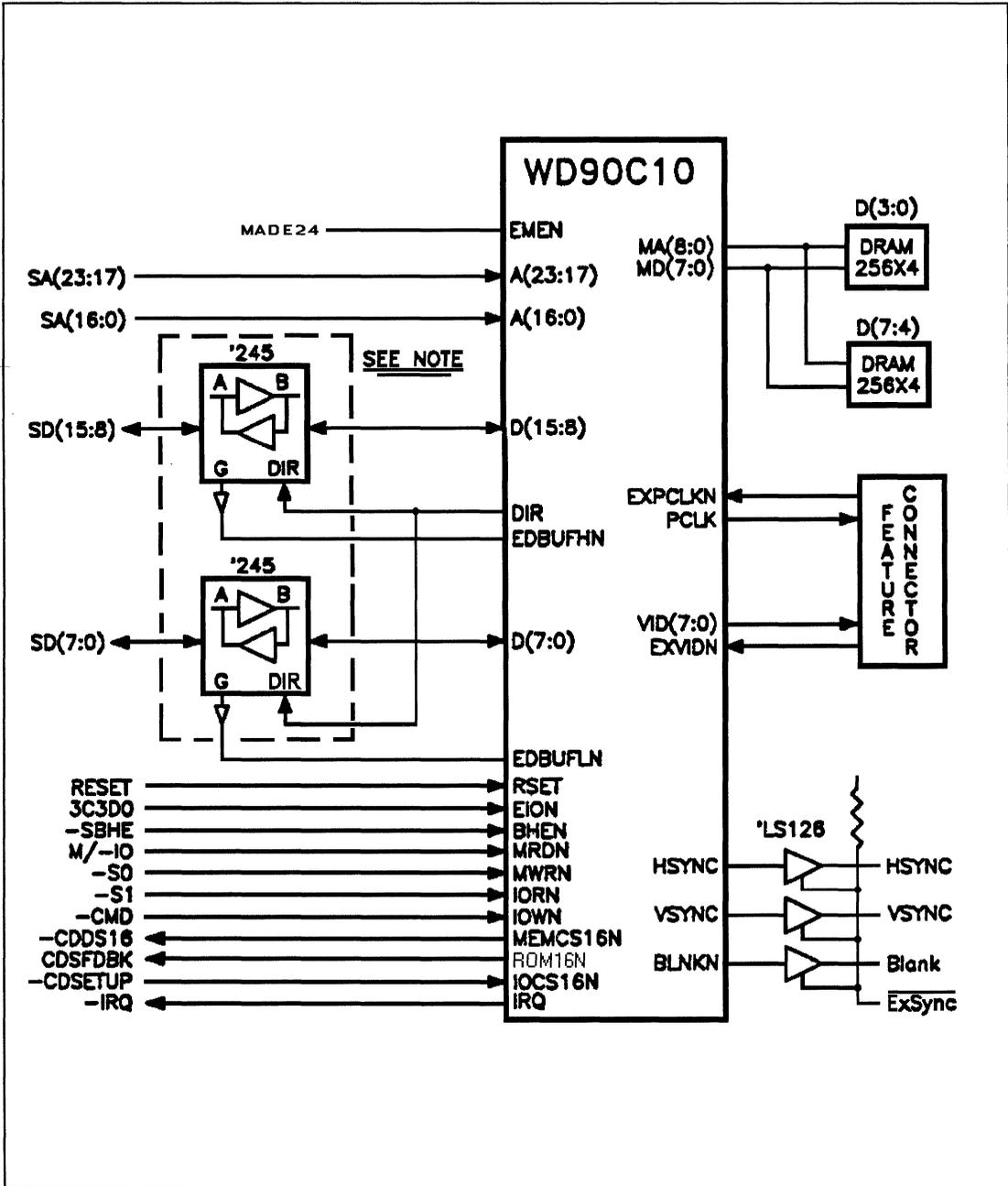
FIGURE 14. 16-BIT MICRO CHANNEL INTERFACE

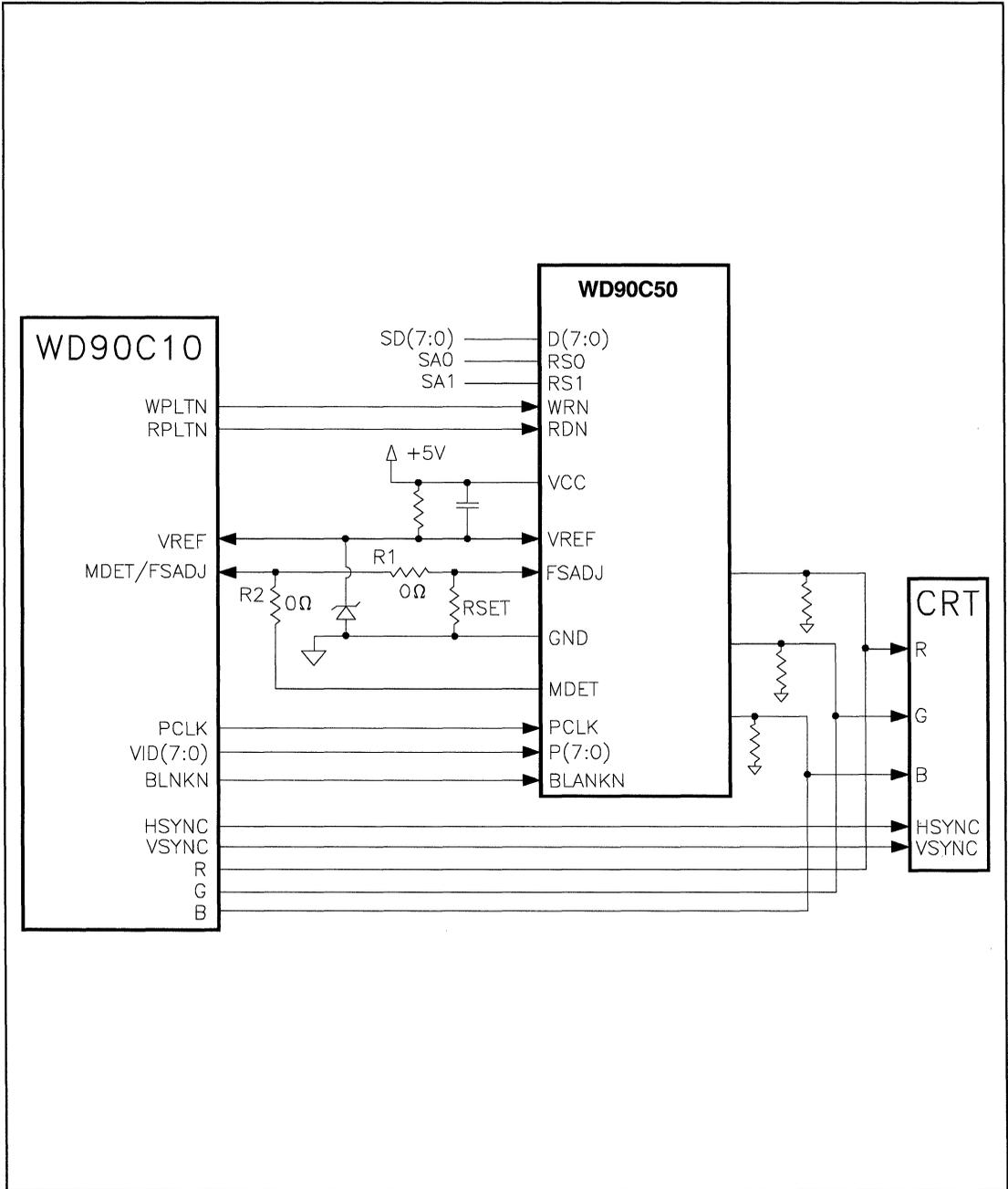Figure 15 illustrates the WD90C10 and RAMDAC (WD90C50) interface block diagram for analog monitors.

FIGURE 15. WD90C10 WITH RAMDAC INTERFACE

Figure 16 illustrates the WD90C10 and TTL monitor connections.

NOTE:

1. VGA/TTL switch may be used to disable HSYNC and VSYNC for Analog or TTL Video connector.

2. MD(15:12) may also be connected as the EGAswitches if desired. See PR register and Pin out sections for more details.

3. For AT applications using the WD90C10, install the IRQ9 resistor.

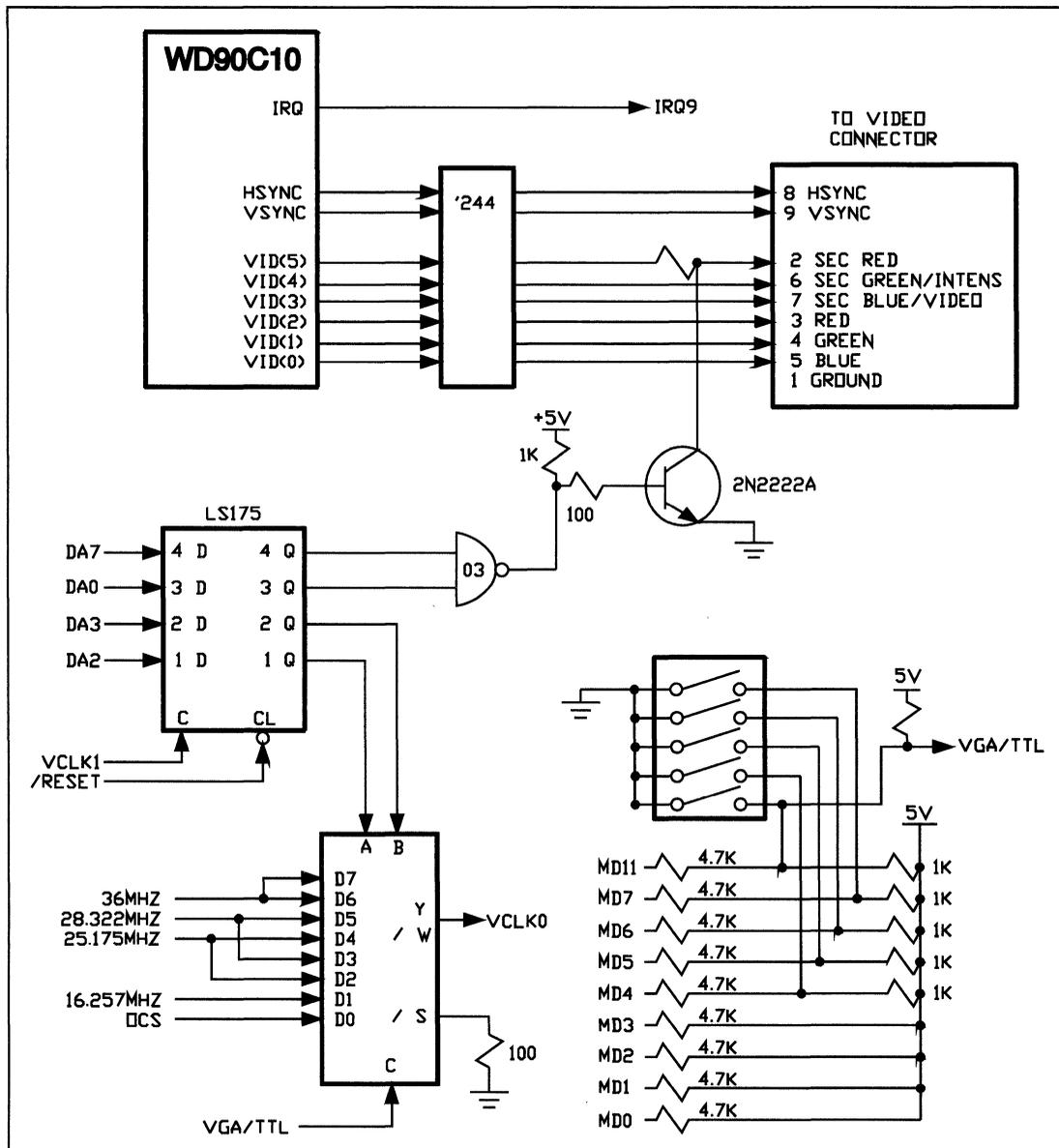4. Transistor 2N2222A is used to emulate a Monochrome and a Color Display connection.

FIGURE 16. WD90C10 AND TTL MONITOR CONNECTIONS

Figure 17 illustrates the WD90C10 with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H bit 3 and bit 2. It is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C10 signal pins (VCLK1, VCLK2) inputs.
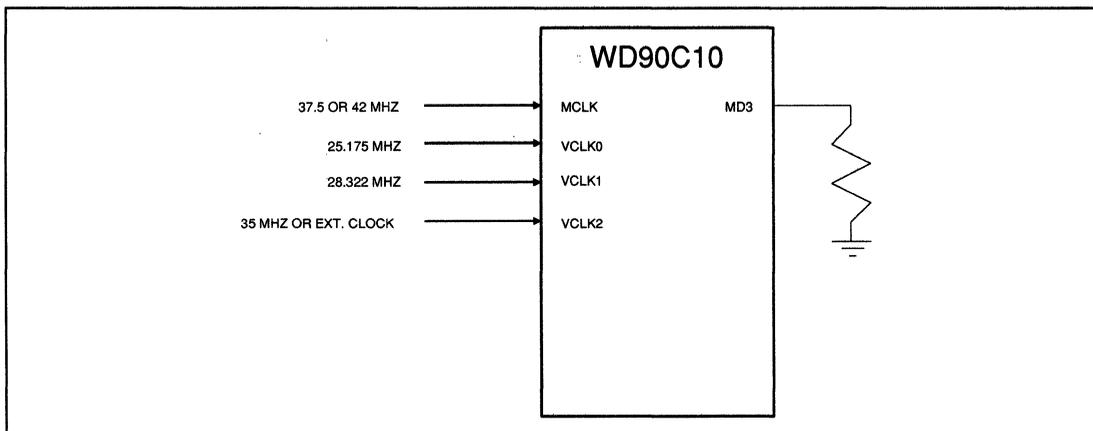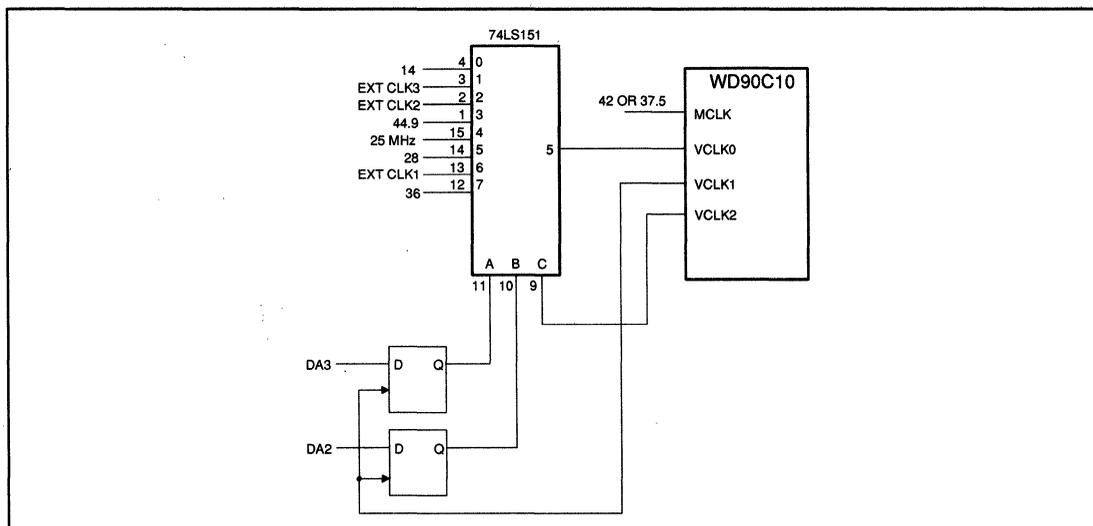

FIGURE 17. CLOCK INTERFACE

FIGURE 18. EXTERNAL VIDEO CLOCK MULTIPLEXING

A.8 REFERENCES

A list of references for generating the WD90C10 data book is shown below:

- IBM Personal Computer Hardware User Guide (IBM # 6322510)
- IBM Personal Computer XT Hardware User Guide (IBM # 6322511)
- IBM Personal Computer AT hardware User Guide (IBM # 6280066)
- IBM Personal System 2 Model 30 Hardware User Guide (IBM # 68x2230)
- IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)

- IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 68x2201)
- IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)
- IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)
- Personal Computer Reference Manual (IBM # 6025005)
- AT&T Video Display Controller VDC 750 / VDC 600 Installation Guide
- Hercules Graphics Card Owner's Manual
- Paradise OEM Technical Publication Manual

The customers are urged to refer to the manuals listed above and supplement their knowledge from other books and literature available.
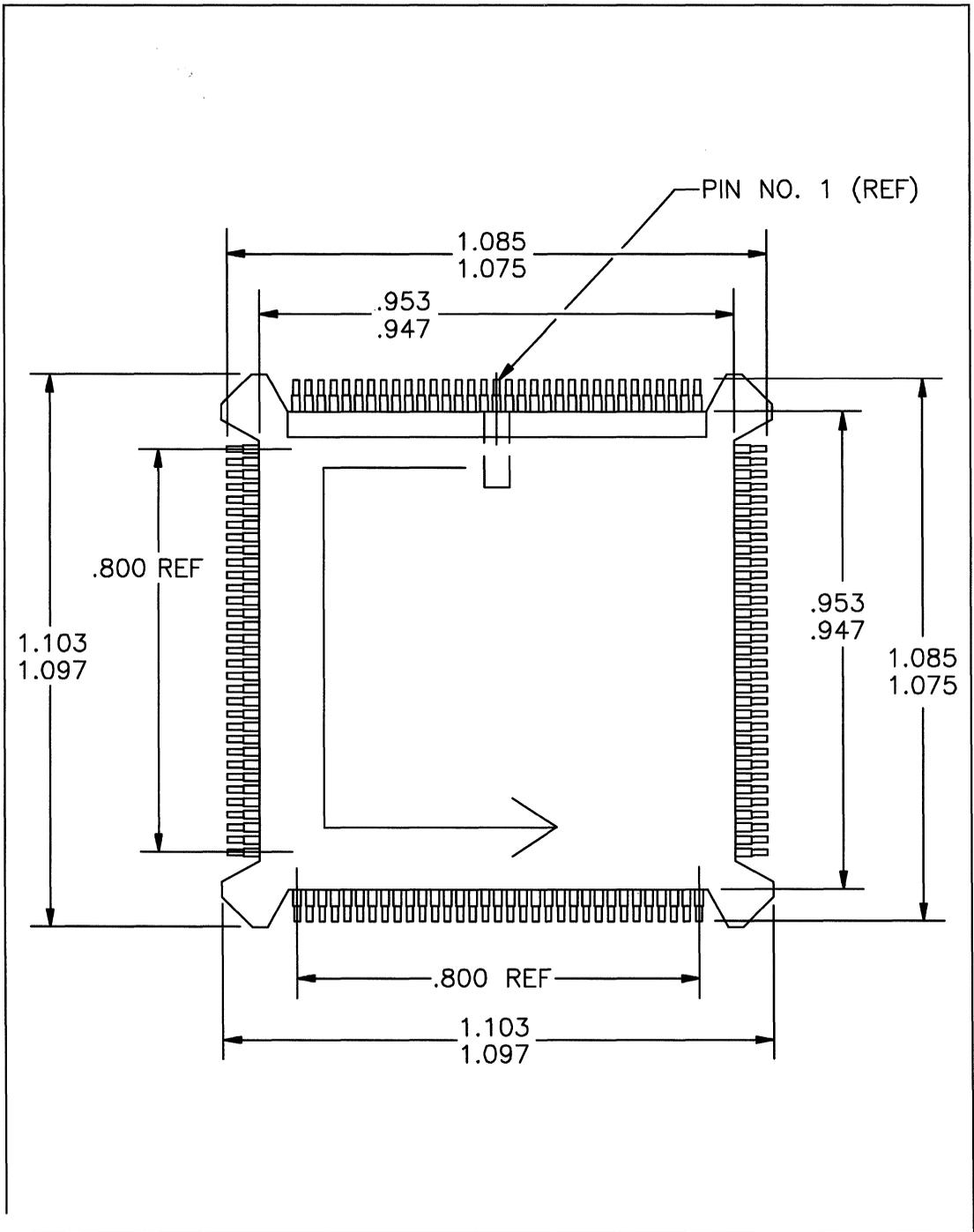
FIGURE 19. 132-PIN JEDEC PLASTIC FLAT PACKAGE (PFP) 1 OF 2

ADVANCE INFORMATION 10-26-90

SEATING PLANE

8°–0°

.180
.160

.030
.020

0.078

0.035

0.061

0.078

0.035

32.4 DEG
TYP

.025

.016
.008

.012
.008

.025 MIN.
(OPTIONAL)

.040
.020

0.017

0.005

0.045
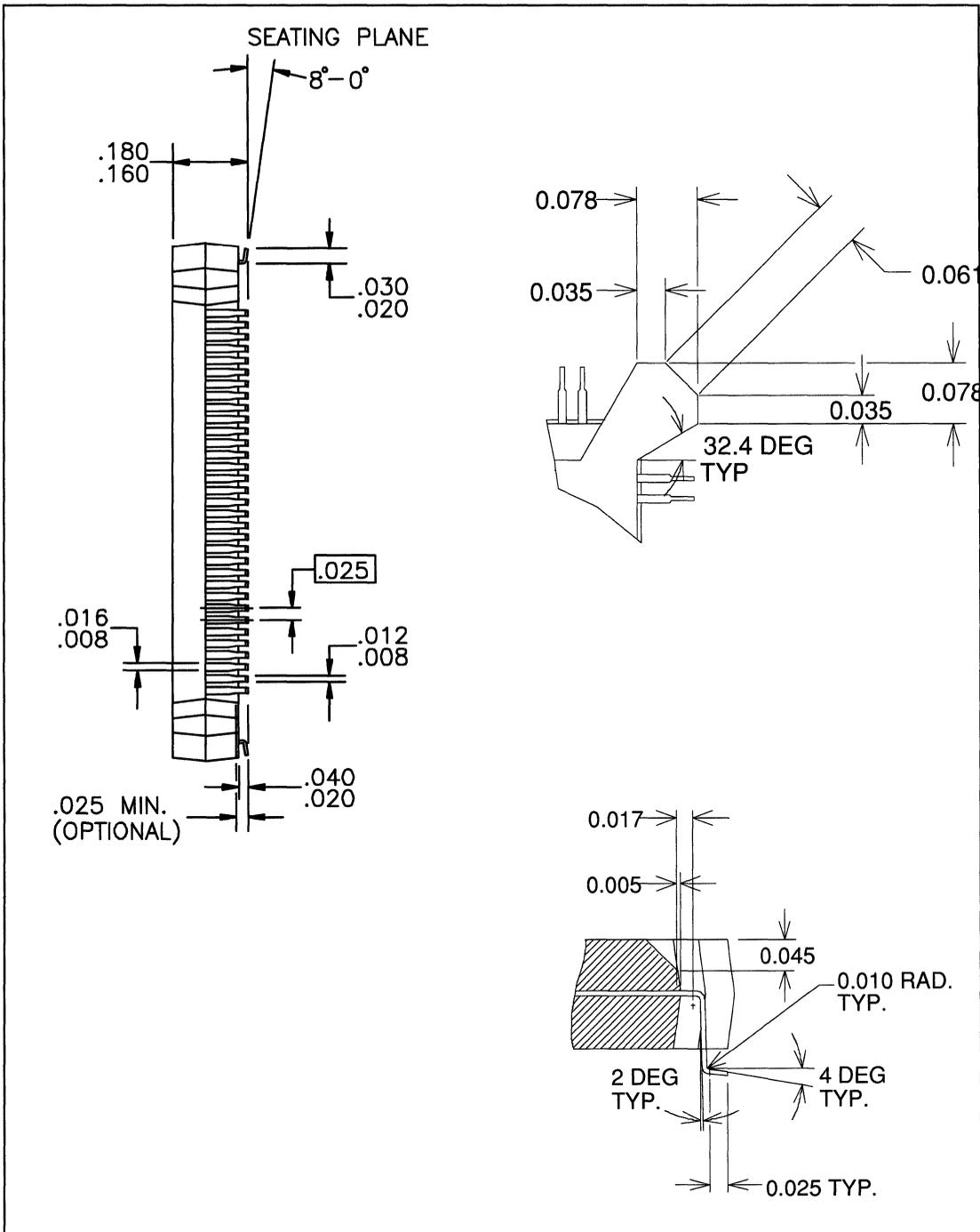
0.010 RAD.
TYP.

2 DEG
TYP.

4 DEG
TYP.

0.025 TYP.

FIGURE 19. 132-PIN JEDEC PLASTIC FLAT PACKAGE (PFP) 2 OF 2