19

WD90C55

VGA LCD

Interface

WESTERN DIGITAL

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1.0 INTRODUCTION

The WD90C55 color interface chip provides the RGB data exchange interface between the WD90C2X family of VGA/LCD controller chips and a number of color panels. The WD90C55 also acts as a pass-through buffer for LCD monochrome data.

This section provides an introduction to the WD90C55 as well as a list of features.

1.1 GENERAL DESCRIPTION

The WD90C55 has been designed to fit the needs of the fast-growing laptop computer market and color-LCD panel technologies. This device interfaces with the following VGA laptop controllers to provide a complete solution in designing laptop computers with both mono- and color-LCD interfaces listed below:

- 90C20
- 90C22
- 90C20A
- 90C26

The WD90C55 drives color LCD panels directly, without requiring additional buffers. It can also be used to drive mono-LCD panels as output buffers.

Using a combination of the WD90C55 and WD90C2X product lines, both mono- and color-LCD panel applications are possible for laptop computers. OEM customers can upgrade their flat-panels as easily as upgrading their CRT displays.

Tables 1-1 and 1-2 show color LCD implementations and number of colors available for each type.

1.2 FEATURES

The major features of the WD90C55 are listed below.

- Direct interface with WD90C20, WD90C22, WD90C20A and WD90C26
- Power down mode control to reduce power consumption
- I/O pin mapping to improve board level testability
- 8-bit (2 and 2/3 pixels) STN color LCD interface
- 16-bit (5 and 1/3 pixels) STN color LCD interface
- Timing adjustment for TFT color LCD panel
- 44-pin PQFP or 48-pin VQFP package

PRODUCT NAME PANEL TYPE	WD90C20	WD90C22	WD90C20A	WD90C26
STN Color LCD	with WD90C55	with WD90C55	with WD90C55	with WD90C55
Hitachi TFT	with WD90C55	with WD90C55	direct	direct
Sharp TFT	N/A	direct	direct	direct

TABLE 1-1 COLOR LCD IMPLEMENTATION

PRODUCT NAME PANEL TYPE	WD90C20	WD90C22	WD90C20A	WD90C26
STN Color LCD	512	4K or 256K	4K	4K or 256K
TFT Color LCD	512	512	512	512 or 27K

TABLE 1-2 COLOR CAPABILITY

2.0 ARCHITECTURE

The WD90C55 color interface chip provides the RGB data exchange interface between the WD90C2X family of VGA/LCD controller chips and a number of color LCD panels, TFT color panels and STN 8-bit/16-bit LCD color panels. It acts as a pass-through buffer for LCD monochrome data, buffering LCD monochrome data from the WD90C2X family, and passing it, along with control signals, to LCD monochrome panels. These interface functions are provided for by the following five modes:

- STN 8-bit Color LCD mode
- STN 16-bit Color LCD mode
- TFT Color LCD for WD90C20
- TFT Color LCD mode for WD90C22
- LCD Monochrome mode

The following additional modes are also provided:

- Pin scan mode
- Output tri-state mode

The WD90C55 turns off any unnecessary logic not selected by SEL[2:0] inputs.

Described in the following subsections are the eight major functional modules of the WD90C55:

- Sequencer (SEQ)
- Data Conversion Control (DCC)
- Bi-Phase Clock Generator (BCG)
- Power Down Control (PDC)
- I/O Pin Mapping Control (IOMP)
- TFT Timing Control (TTC) Interface
- Color Panel Interface (CPI)
- Monochrome LCD Interface

These modules are illustrated in the functional block diagram provided in this section.

2.1 SEQUENCER - STN INTERFACE

The sequencer provides the key timing control from the WD90C2X product to the color LCD panel. In STN color-LCD mode, the WD90C2X sends out 6-bits (2-pixels) every shift clock. The shift clock (XSCLK) is not free-running but toggling. It toggles only when the video data is valid. "WGT-CLK" is used to qualify the valid data and to start the state machine in the sequencer.

2.2 DATA CONVERSION CONTROL - STN INTERFACE

The DCC block provides both 6-bit to 8-bit and 6-bit to 16-bit data conversion.

Only one type of color LCD panel is enabled during the operation.

Unused logic is automatically turned off.

2.3 BI-PHASE CLOCK GENERATOR - STN INTERFACE

The BCG block is used to generate the bi-phase clock outputs XUCLK and XLCLK. These outputs are used in the 8-bit STN color LCD interface.

Eight-bit data is latched on the falling edges of XUCLK and XLCLK. Sixteen-bit data is latched on the falling edge of XLCLK.

2.4 POWER DOWN CONTROL

The PDC block generates the control signals to turn off the WD90C55 when the system goes to power down mode.

The output data bus is driven "Low".

The output clocks are turned off and stay "Low" when the "$\overline{\text{PDOWN}}$" is active low.

2.5 I/O PINS MAPPING/PIN SCAN TEST MODE

This is a unique test mode provided by the WD90C55. When the SEL[2:0] = 000, test mode is enabled.

Test mode allows input pins to be logically connected to the outputs. During In-Circuit Test, test pads can be connected to the pins on a PCB, and a simple "opens and shorts" test verifies that there are no defects.

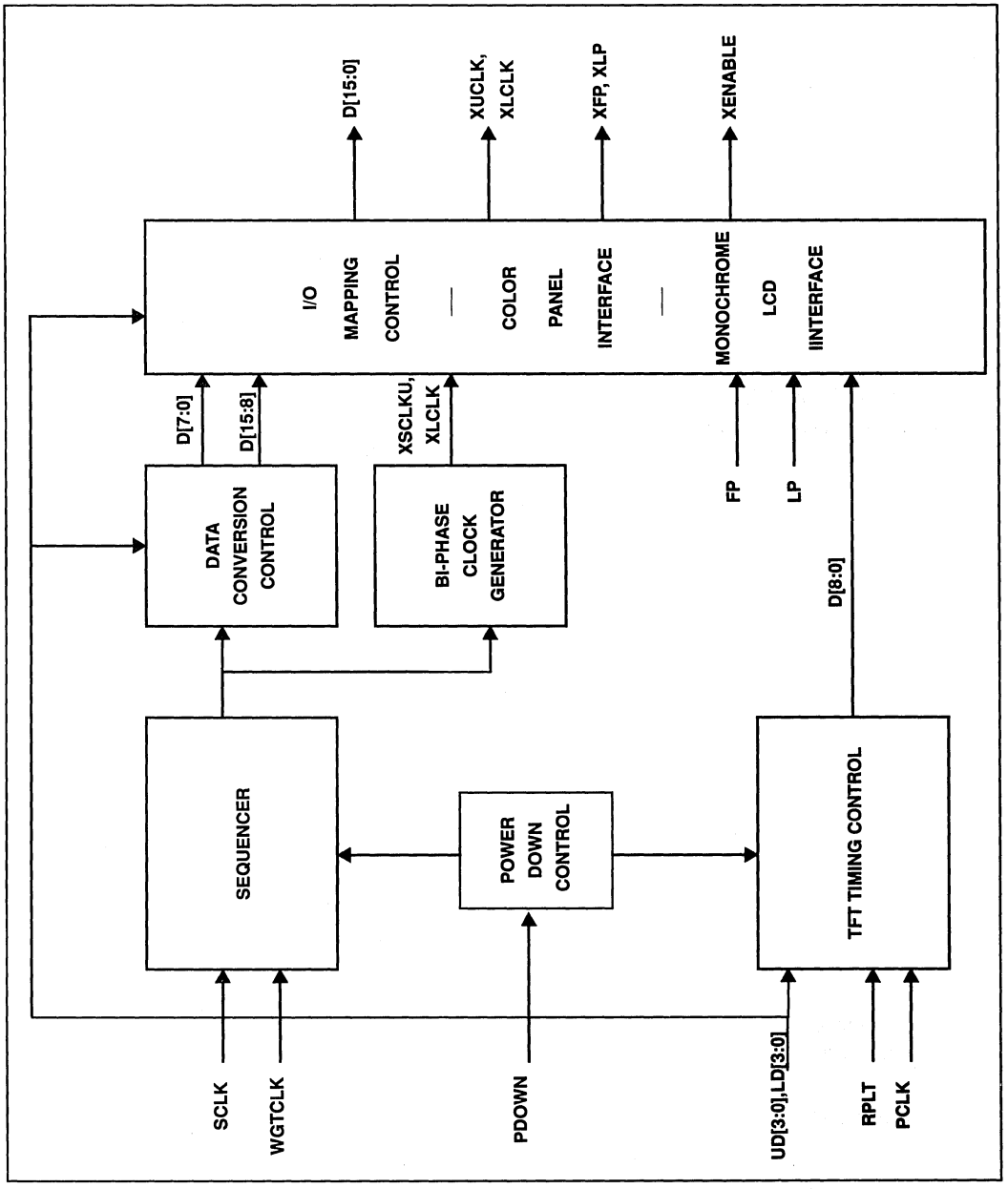

FIGURE 2-1 COLOR LCD FUNCTIONAL BLOCK DIAGRAM

2.6 TFT TIMING CONTROL - TFT INTERFACE

The WD90C20 and WD90C22 require different timing. It is the function of the TTC Block to adjust the timing specification for the Hitachi TFT Color LCD Panel. This adjustment consists of a 7 PCLK delay and 2 PCLK delay for the WD90C20 and WD90C22, respectively.

The WD90C22, WD90C20A and WD90C26 can drive the Sharp TFT color LCD panel directly.

The WD90C20A and WD90C26 can also drive the Hitachi TFT color LCD directly, without a WD90C55 interface.

2.7 COLOR PANEL INTERFACE

The color panel interface block contains the logic to multiplex 8-bit STN data onto the external data bus (D0-D7), or 16-bit STN data onto D0-D15. Nine-bit TFT data (R0-2, G0-2, B0-2) are multiplexed onto D0-DX8, and 8-bit monochrome LCD data is muxed onto D0-D7 via this block.

2.8 MONOCHROME LCD INTERFACE

In Monochrome LCD mode, input data UD[3:0] LD[3:0] and control signals for FP, LP, and SCLK, are multiplexed onto the color interface bus. These input data and control signals are simply buffered and passed through the WD90C55. See the following figure for input data to pixel mapping information.

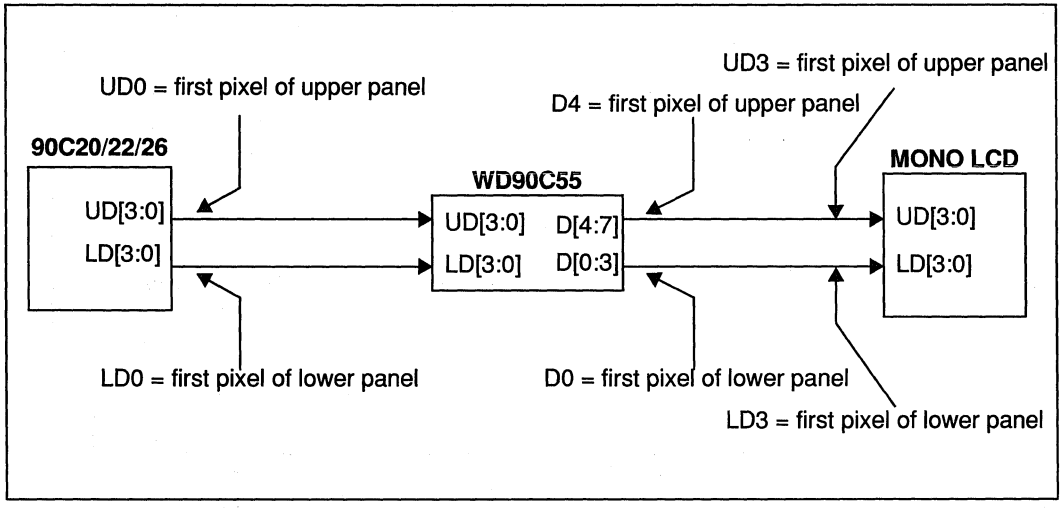

FIGURE 2-2 WD90C55 MONO LCD INTERFACE BLOCK DIAGRAM

3.0 SIGNAL DESCRIPTION

This section contains pin information for both the 44- and 48-pin WD90C55 products. Pin assignment tables and pin diagrams of both are provided.

Section 4.1 describes the 44-pin product and section 4.2 describes the 48-pin device.

3.1 44-PIN WD90C55 PINOUT

This section contains the following information:

- Pinout diagram
- Pin list
- Pin package definitions
- Pin description
- Bus definition
- LCD panel pinout spec

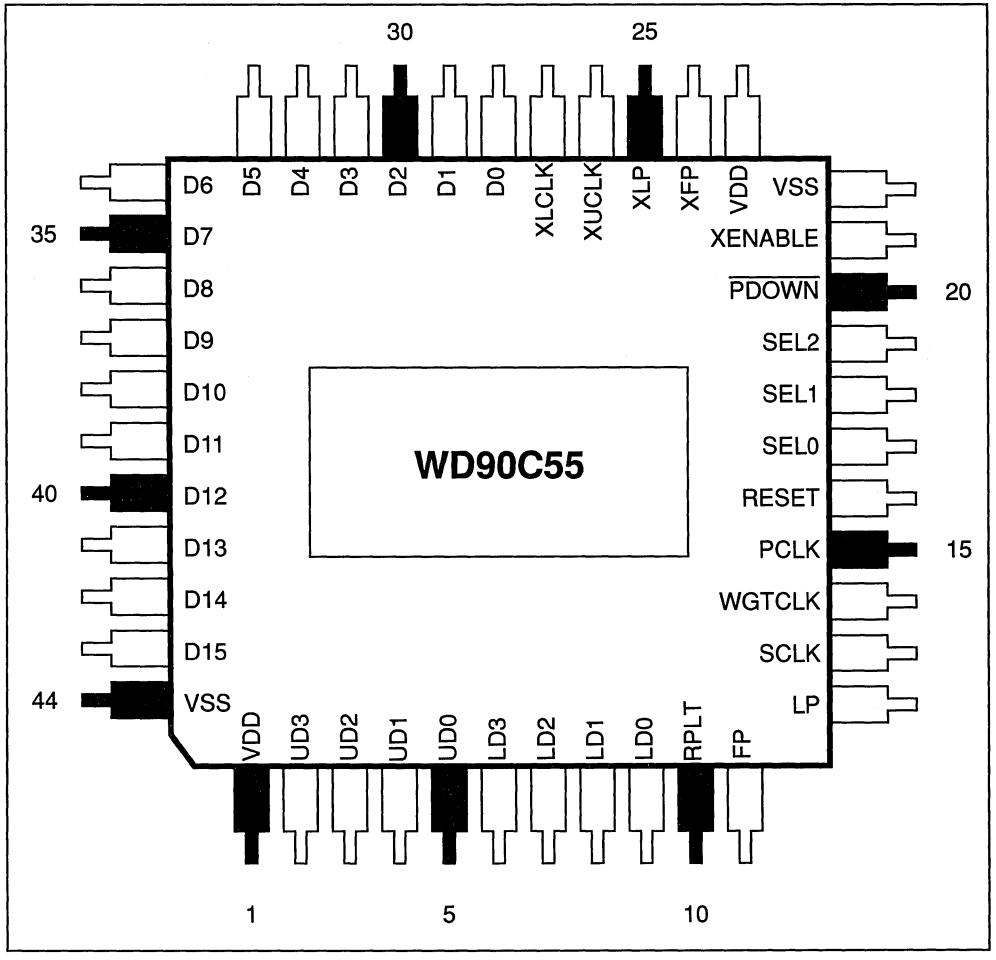

FIGURE 3-1 44-PIN WD90C55 PINOUT DIAGRAM

NAME	PIN#	NAME	PIN#	NAME	PIN#
VDD	1	RESET	16	D3	31
UD3	2	SEL0	17	D4	32
UD2	3	SEL1	18	D5	33
UD1	4	SEL2	19	D6	34
UD0	5	$\overline{\text{PDOWN}}$	20	D7	35
LD3	6	XENABLE	21	D8	36
LD2	7	VSS	22	D9	37
LD1	8	VDD	23	D10	38
LD0	9	XFP	24	D11	39
RPLT	10	XLP	25	D12	40
FP	11	XUCLK	26	D13	41
LP	12	XLCLK	27	D14	42
SCLK	13	D0	28	D15	43
WGTCLK	14	D1	29	VSS	44
PCLK	15	D2	30		

TABLE 3-1 44-PIN PACKAGE PIN LIST

PIN #	SIGNAL NAME	I/O	DESCRIPTION
1,22,23,44	VSS, VDD	I	Power
2-5	UD[3:0]	I	Upper Panel Output data
6-9	LD[3:0]	I	Lower Panel Output data
10	RPLT	I	Data bit which is used for TFT interface
11	FP	I	Frame pulse
12	LP	I	Line Pulse
13	SCLK	I	Shift Clock
14	WGTCLK	I	Data enable
15	PCLK	I	Pixel Clock (free running)
16	RESET	I	System Reset
17-19	SEL[0:2]	I	WD90C55 Selection Bus, bit 0 to bit 2
20	$\overline{\text{PDOWN}}$	I	Power Down Mode Control, active low
21	XENABLE	O	Data Enable
24	XFP	O	Frame Pulse
25	XLP	O	Line Pulse
26	XUCLK	O	Upper Data Shift Clock
27	XLCLK	O	Lower Data Shift Clock
28-43	D[15:0]	O	LCD Panel Data Output

TABLE 3-2 44-PIN PACKAGE PIN DESCRIPTIONS

SEL[2:0]	DESCRIPTION
0 0 0	Test Mode 1 I/O pin mapping, ICT test
0 0 1	8-Bit STN Panels (Sharp, Seiko)
0 1 0	16-Bit STN Panels (Sanyo)
1 0 0	Monochrome LCD Panels
1 0 1	Hitachi TFT Color Panel (WD90C20)
1 1 0	Hitachi TFT Color Panel (WD90C22)
1 1 1	Test Mode 2, Output buffer tristate test

TABLE 3-3 44-PIN PACKAGE SEL[2:0] BUS DEFINITION

NOTE

The WD90C22 can drive the Sharp TFT color LCD directly without WD90C55.

WD90C55	MONO LCD	8-BIT STN (Seiko)	8-BIT STN (Sharp)	16-BIT STN	9-BIT TFT
XFP	FP	DIN	YD	FLM	VSYNC
XLP	LP	LP	LP	CL1	HSYNC
XENABLE	UNUSED	UNUSED	UNUSED	UNUSED	DEN
FR	FR	UNUSED	UNUSED	M	UNUSED
XUCLK	XSCLK	XSCLU	XCKL	UNUSED	CLK
XLCLK	UNUSED	XCKLL	XCKU	CL2	UNUSED
D15	UNUSED	UNUSED	UNUSED	UD7	UNUSED
D14	UNUSED	UNUSED	UNUSED	UD6	UNUSED
D13	UNUSED	UNUSED	UNUSED	UD5	UNUSED
D12	UNUSED	UNUSED	UNUSED	UD4	UNUSED
D11	UNUSED	UNUSED	UNUSED	UD3	UNUSED
D10	UNUSED	UNUSED	UNUSED	UD2	UNUSED
D9	UNUSED	UNUSED	UNUSED	UD1	UNUSED
D8	UNUSED	UNUSED	UNUSED	UD0	B0
D7	UD3	D7	D0	LD7	R2
D6	UD2	D6	D1	LD6	R1
D5	UD1	D5	D2	LD5	R0
D4	UD0	D4	D3	LD4	G2
D3	LD3	D3	D4	LD3	G1
D2	LD2	D2	D5	LD2	G0
D1	LD1	D1	D6	LD1	B2
D0	LD0	D0	D7	LD0	B1

TABLE 3-4 44-PIN PACKAGE LCD PANEL PINOUT SPEC

3.2 48-PIN WD90C55 PINOUT

This subsection contains the following information:

- Pinout diagram of the 48-pin WD90C55
- 48-Pin Package List

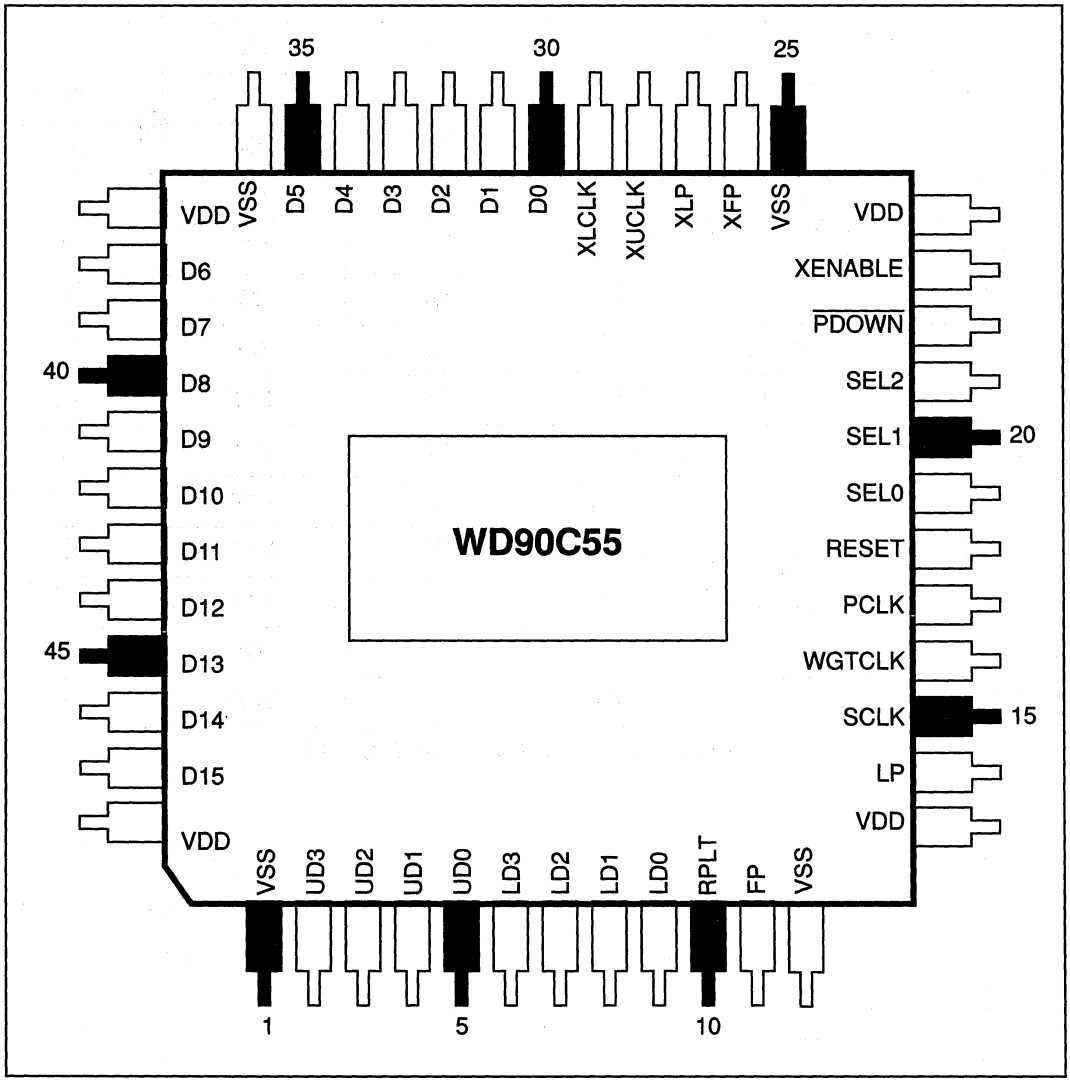

FIGURE 3-2 48-PIN PACKAGE PINOUT DIAGRAM

NAME	PIN #	NAME	PIN #	NAME	PIN #
VSS	1	PCLK	17	D3	33
UD3	2	RESET	18	D4	34
UD2	3	SEL0	19	D5	35
UD1	4	SEL1	20	VSS	36
UD0	5	SEL2	21	VDD	37
LD3	6	$\overline{\text{PDOWN}}$	22	D6	38
LD2	7	XENABLE	23	D7	39
LD1	8	VDD	24	D8	40
LD0	9	VSS	25	D9	41
RPLT	10	XFP	26	D10	42
FP	11	XLP	27	D11	43
VSS	12	XUCLK	28	D12	44
VDD	13	XLCLK	29	D13	45
LP	14	D0	30	D14	46
SCLK	15	D1	31	D15	47
WGTCLK	16	D2	32	VDD	48

TABLE 3-5 48-PIN PACKAGE PIN LIST

PIN #	SIGNAL NAME	I/O	DESCRIPTION
1,22,23,44	VSS, VDD	I	Power
2-5	UD[3:0]	I	Upper Panel Output data
6-9	LD[3:0]	I	Lower Panel Output data
10	RPLT	I	Data bit which is used for TFT interface
11	FP	I	Frame pulse
12	LP	I	Line Pulse
13	SCLK	I	Shift Clock
14	WGTCLK	I	Data enable
15	PCLK	I	Pixel Clock (free running)
16	RESET	I	System Reset
17-19	SEL[0:2]	I	WD90C55 Selection Bus, bit 0 to bit 2
20	$\overline{\text{PDOWN}}$	I	Power Down Mode Control, active low
21	XENABLE	O	Data Enable
24	XFP	O	Frame Pulse
25	XLP	O	Line Pulse
26	XUCLK	O	Upper Data Shift Clock
27	XLCLK	O	Lower Data Shift Clock
28-43	D[15:0]	O	LCD Panel Data Output

TABLE 3-6 48-PIN PACKAGE PIN DESCRIPTIONS

SEL[2:0]	DESCRIPTION
0 0 0	Test Mode 1 I/O pin mapping, ICT test
0 0 1	8 Bit STN Panels (Sharp, Seiko)
0 1 0	16 Bit STN Panels (Sanyo)
1 0 0	Monochrome LCD Panels
1 0 1	Hitachi TFT Color Panel (WD90C20)
1 1 0	Hitachi TFT Color Panel (WD90C22)
1 1 1	Test Mode 2, Output buffer tristate test

TABLE 3-7 48-PIN PACKAGE SEL[2:0] BUS DEFINITION

NOTE

The WD90C22 can drive the Sharp TFT color LCD directly without WD90C55.

WD90C55	MONO LCD	8-BIT STN (Seiko)	8-BIT STN (Sharp)	16-BIT STN	9-BIT TFT
XFP	FP	DIN	YD	FLM	VSYNC
XLP	LP	LP	LP	CL1	HSYNC
XENABLE	UNUSED	UNUSED	UNUSED	UNUSED	DEN
FR	FR	UNUSED	UNUSED	M	UNUSED
XUCLK	XSCLK	XSCLU	XCKL	UNUSED	CLK
XLCLK	UNUSED	XCKLL	XCKU	CL2	UNUSED
D15	UNUSED	UNUSED	UNUSED	UD7	UNUSED
D14	UNUSED	UNUSED	UNUSED	UD6	UNUSED
D13	UNUSED	UNUSED	UNUSED	UD5	UNUSED
D12	UNUSED	UNUSED	UNUSED	UD4	UNUSED
D11	UNUSED	UNUSED	UNUSED	UD3	UNUSED
D10	UNUSED	UNUSED	UNUSED	UD2	UNUSED
D9	UNUSED	UNUSED	UNUSED	UD1	UNUSED
D8	UNUSED	UNUSED	UNUSED	UD0	B0
D7	UD3	D7	D0	LD7	R2
D6	UD2	D6	D1	LD6	R1
D5	UD1	D5	D2	LD5	R0
D4	UD0	D4	D3	LD4	G2
D3	LD3	D3	D4	LD3	G1
D2	LD2	D2	D5	LD2	G0
D1	LD1	D1	D6	LD1	B2
D0	LD0	D0	D7	LD0	B1

TABLE 3-8 48-PIN PACKAGE LCD PANEL PINOUT SPEC

4.0 DC ELECTRICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0° C to 70° C
Storage temperature	-40° C to 125° C
Voltage on all inputs and outputs with respect to Vss	-0.3 to 7 Volts
Power dissipation	0.85 watt

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

4.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to Vss (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0° to 70° C
Power Supply Voltage	4.75 to 5.25 Volts

4.3 SUPPLY PINS

PARAMETER	MIN	MAX	CONDITIONS
VDD	4.75V	5.25V	Pins 1, 23 (44 pin package), Pin 8, 48 (48 pin package)

4.4 INPUT PINS

PARAMETER	MIN	MAX	CONDITIONS
VIL	-0.5V	0.8V	
VIH	2.0V	VCC +0.5V	
IIL	-10µA	-10 µA	VIH = VCC, VIL = 0V
IDDS		100 µA	VIN = VCC or VSS, IOH = IOL = 0mA

FP, LP, SCLK, WGTCLK,PCLK,UD[3:0], LD[3:0], RESET, RPLT, $\overline{\text{PDOWN}}$, SEL[2:0]

4.5 OUTPUT PINS

PARAMETER	MIN	MAX	CONDITIONS
VOL		0.4V	IOL = 6mA
VOH	2.4V		IOH = -2mA
IOZ	-50 µA	50 µA	VOUT = VCC or VSS
C_{out}		100pf	

XFP, XLP, XENABLE, XUCLK, XLCLK, D[15:0]

5.0 AC OPERATING CHARACTERISTICS

Timing is provided for the following:

- STN Color LCD Mode - Input Timing
- STN Color LCD Mode - 8-bit interface
- STN Color LCD Mode - 16-bit interface
- TFT Color LCD Mode - 9-bit interface
- Mono LCD Mode

ITEM	DESCRIPTION	MIN	MAX
1	Rise/Fall Time (Inputs: PCLK SCLK FP LP WGTCLK		5 ns 10 ns 10 ns 10 ns 10 ns
2	UD[3:1], LD[3,1] setup to ↓ SCLK	18 ns	
3	UD[3:1], LD[3,1] hold from ↓ SCLK	18 ns	
4	UD[3:1], LD[3,1] valid from ↑ WGTCLK	10 ns	
5	UD[3:1], LD[3,1] invalid from ↓ WGTCLK	-10 ns	
6	SCLK period	62.5 ns (PCLK = 32 MHz)	80 ns (PCLK = 25 MHz)
7	FP ⇑ to LP ⇓ SETUP time	1LP	
8	FP ⇓ to LP ⇓ HOLD time		0

TABLE 5-1 STN COLOR LCD MODE - INPUT TIMING

Refer to the following figure for timing diagram.

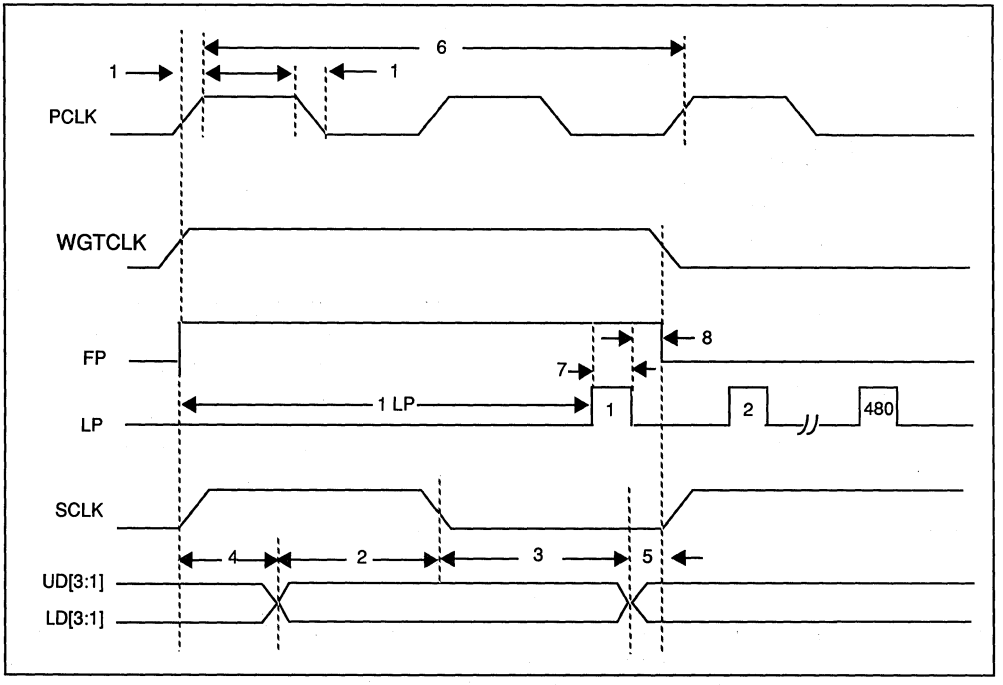

FIGURE 5-1 STN COLOR LCD MODE - INPUT TIMING DIAGRAM

NOTE

$LP = 1/_{PCLK} * 800$

ITEM	DESCRIPTION	MIN	MAX
1	XFP to XLP- Hold time	24PCLK	32 PCLK
2	XFP to XLP- Setup time		1LP
3	↑ SCLK to ↑ XUCLK		240 ns
4	↑ SCLK to ↑ XLCLK		345 ns
5	D[7:0] (even byte) setup to ↓ XUCLK, ↓ XLCLK	30 @ t=32MHz 35 @ t=28MHz 40 @ t=25MHz	
6	D[7:0] (odd byte) hold from ↓ XUCLK, ↓ XLCLK	30 @ t=32MHz 35 @ t=28MHz 40 @ t=25MHz	
7	XUCLK cycle time	163 ns	218 ns
8	XLCLK cycle time	165 ns	205 ns

TABLE 5-2 STN COLOR LCD MODE - 8-BIT INTERFACE

Refer to the figure on the next page for timing diagram.

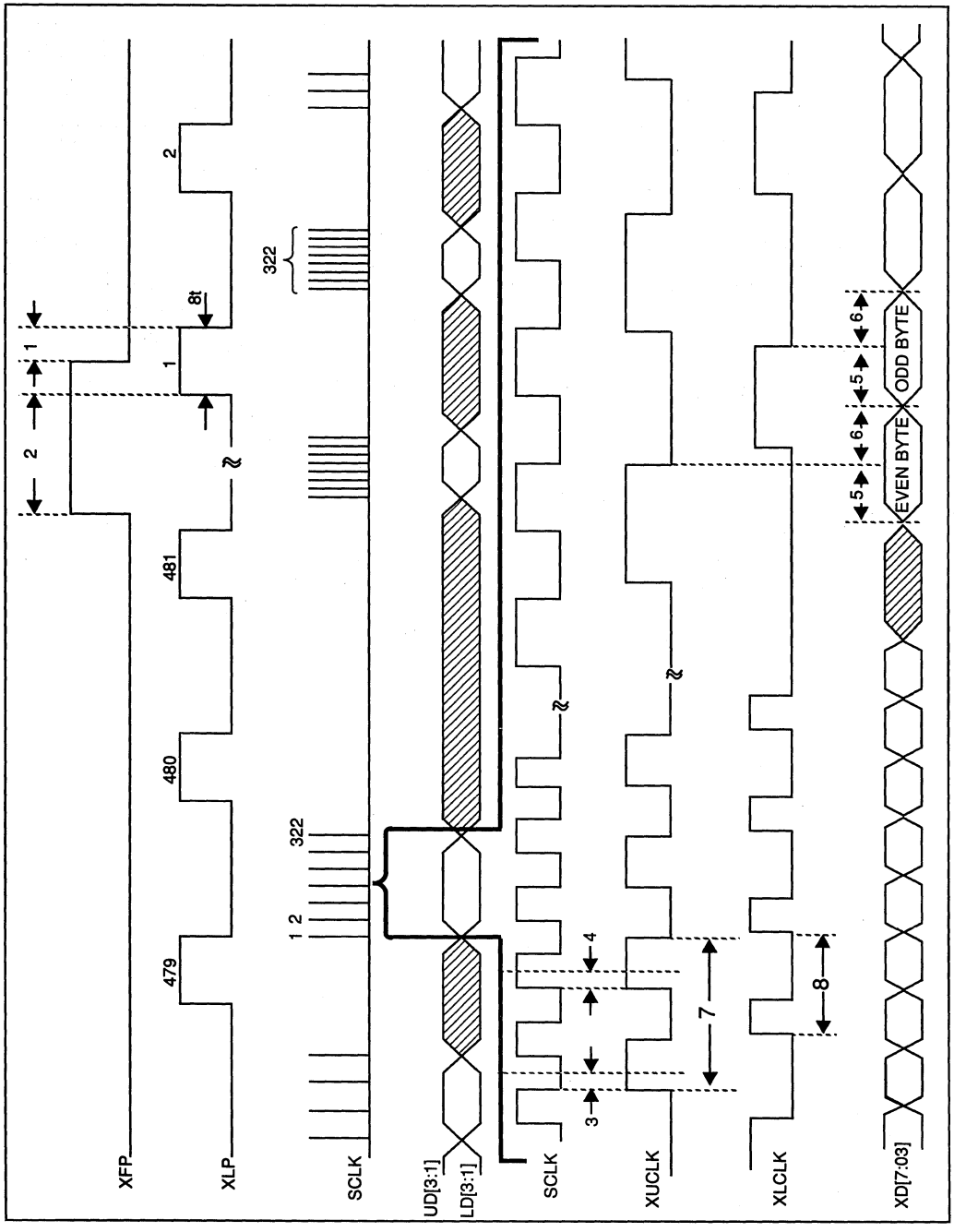

FIGURE 5-2 STN COLOR LCD 8-BIT INTERFACE MODE TIMING DIAGRAM

ITEM	DESCRIPTION	MIN	MAX
1	XFP to XLP- Hold time	24PCLK	32 PCLK
2	XFP to XLP- Setup time		1LP
3	↑ SCLK to ↑ XUCLK		240 ns
4	↑ SCLK to ↑ XLCLK		345 ns
5	D[7:0] (even byte) setup to ↓ XUCLK, ↓ XLCLK	30 @ t=32MHz 35 @ t=28MHz 40 @ t=25MHz	

TABLE 5-3 STN COLOR LCD MODE - 8-BIT INTERFACE

Refer to the figure on the next page for timing diagram.

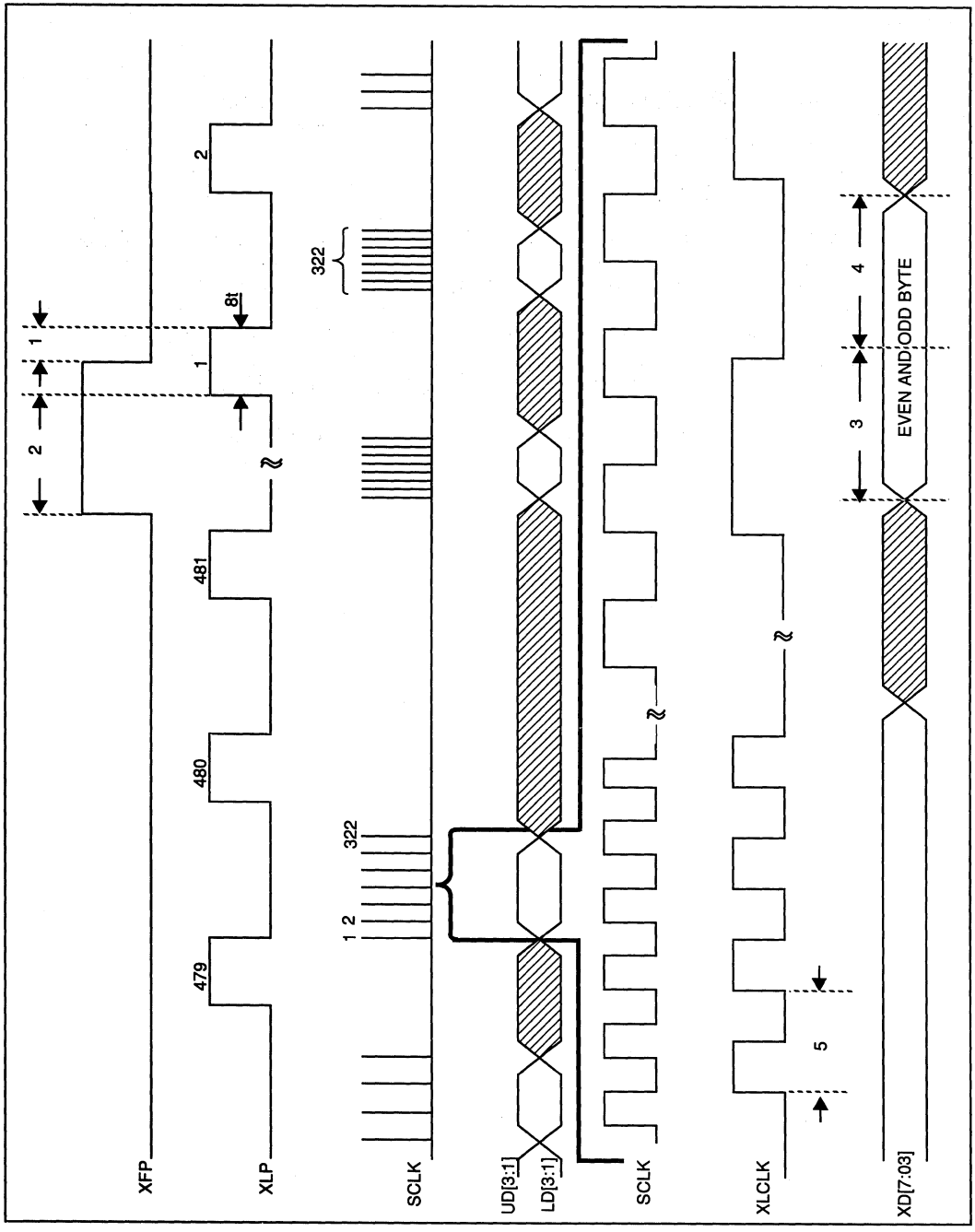

FIGURE 5-3 STN COLOR LCD 16-BIT INTERFACE MODE TIMING DIAGRAM

ITEM	DESCRIPTION	MIN	MAX
1	Data IN [8:0] setup to PCLK ↓	10 ns	
2	Data IN [8:0] hold from PCLK ↓	10 ns	
3	D[8:0] setup to XUCLK ↓ (WD90C22) PCLK=25MHz	10 ns	
4	D[8:0] hold from XUCLK ↓ (WD90C22) PCLK=25MHz	10 ns	
5	D[8:0] setup to XUCLK ↓ (WD90C20) PCLK=25MHz	10 ns	
6	D[8:0] hold from XUCLK ↓ (WD90C20) PCLK=25MHz	10 ns	

TABLE 5-4 TFT COLOR LCD MODE - 9-BIT INTERFACE

Refer to the following figure for timing diagram.

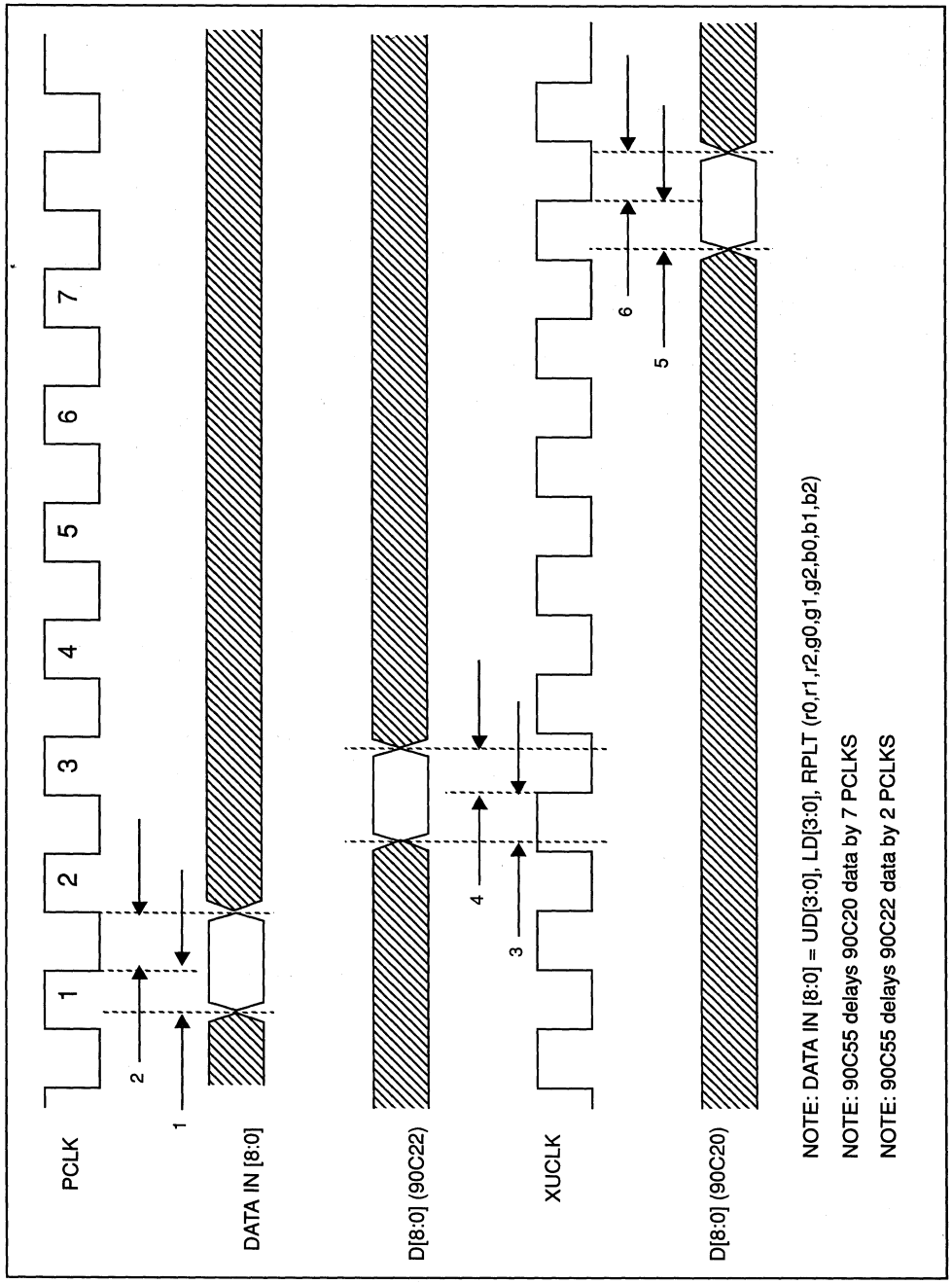

FIGURE 5-4 TFT COLOR LCD 9-BIT INTERFACE MODE TIMING DIAGRAM

6.0 IMPLEMENTATION

This section provides block diagrams of the WD90C55 in each implementation:

- 90C20 Implementation
- 90C20A Implementation
- 90C22 Implementation
- 90C26 Implementation

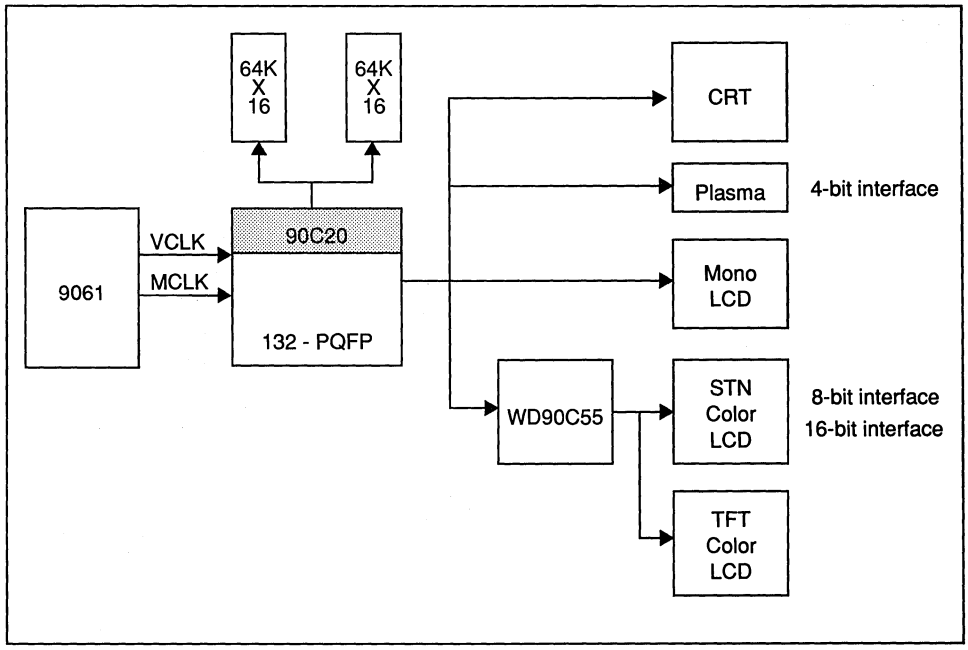

FIGURE 6-1 WD90C55 WITH WD90C20 IMPLEMENTATION

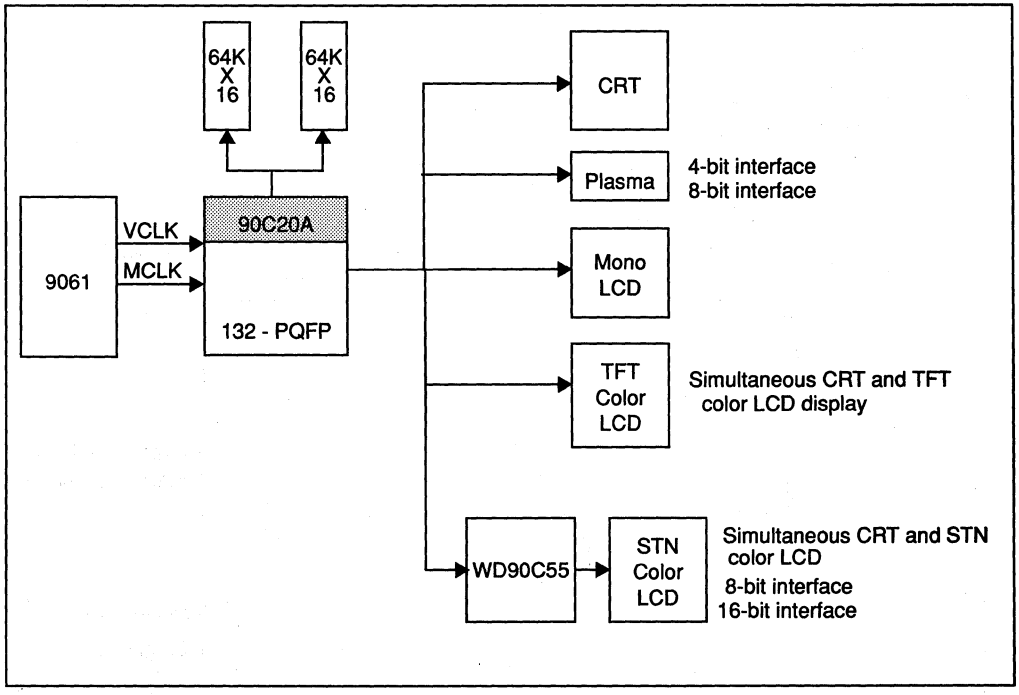

FIGURE 6-2 WD90C55 WITH WD90C20A IMPLEMENTATION

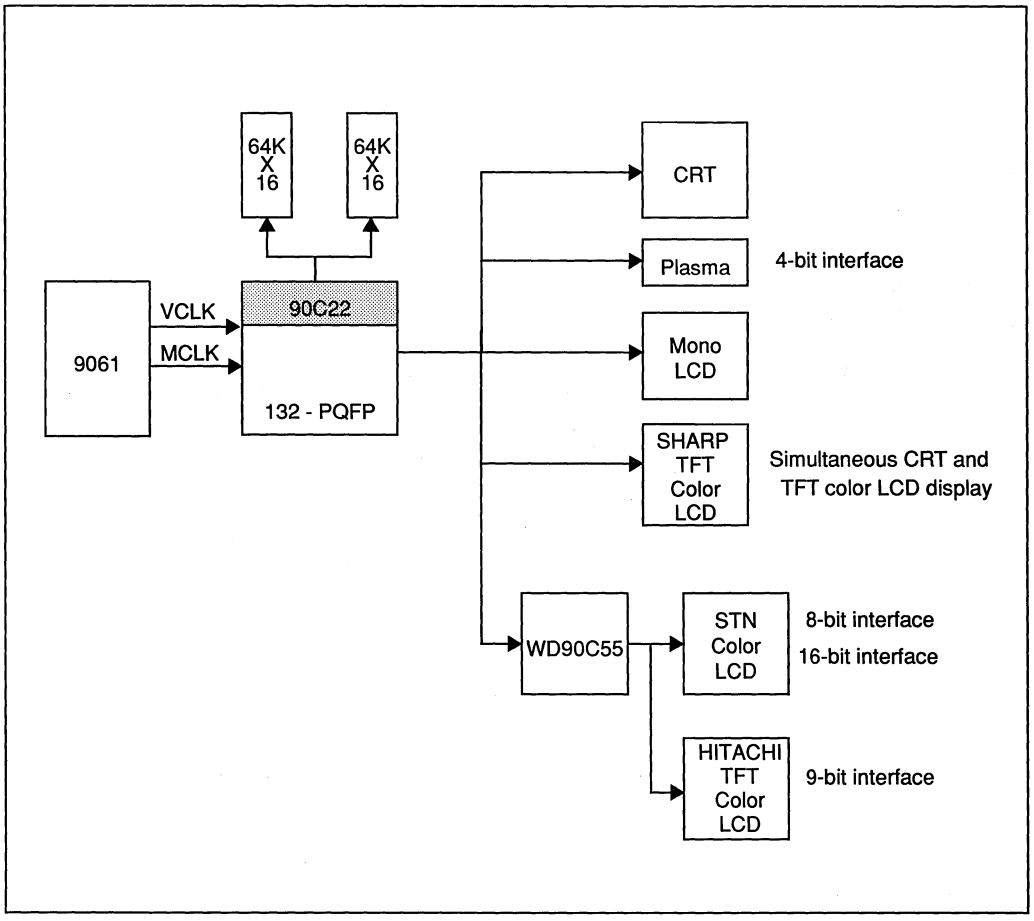

FIGURE 6-3 WD90C55 WITH WD90C22 IMPLEMENTATION

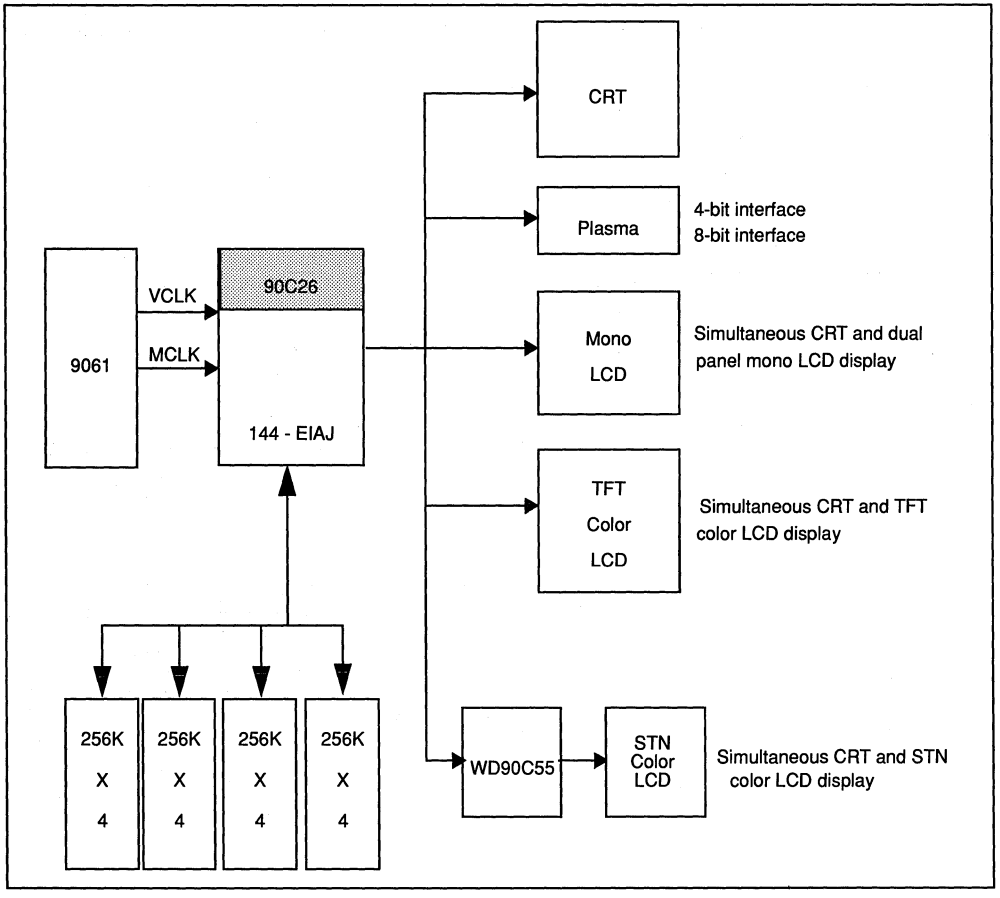

FIGURE 6-4 WD90C55 WITH WD90C26 IMPLEMENTATION

7.0 MECHANICAL SPECIFICATIONS

Figures 7-1 and 7-2 contain the mechanical specifications for WD90C55 44- and 48-pin packages.

7.1 44-PIN PACKAGE

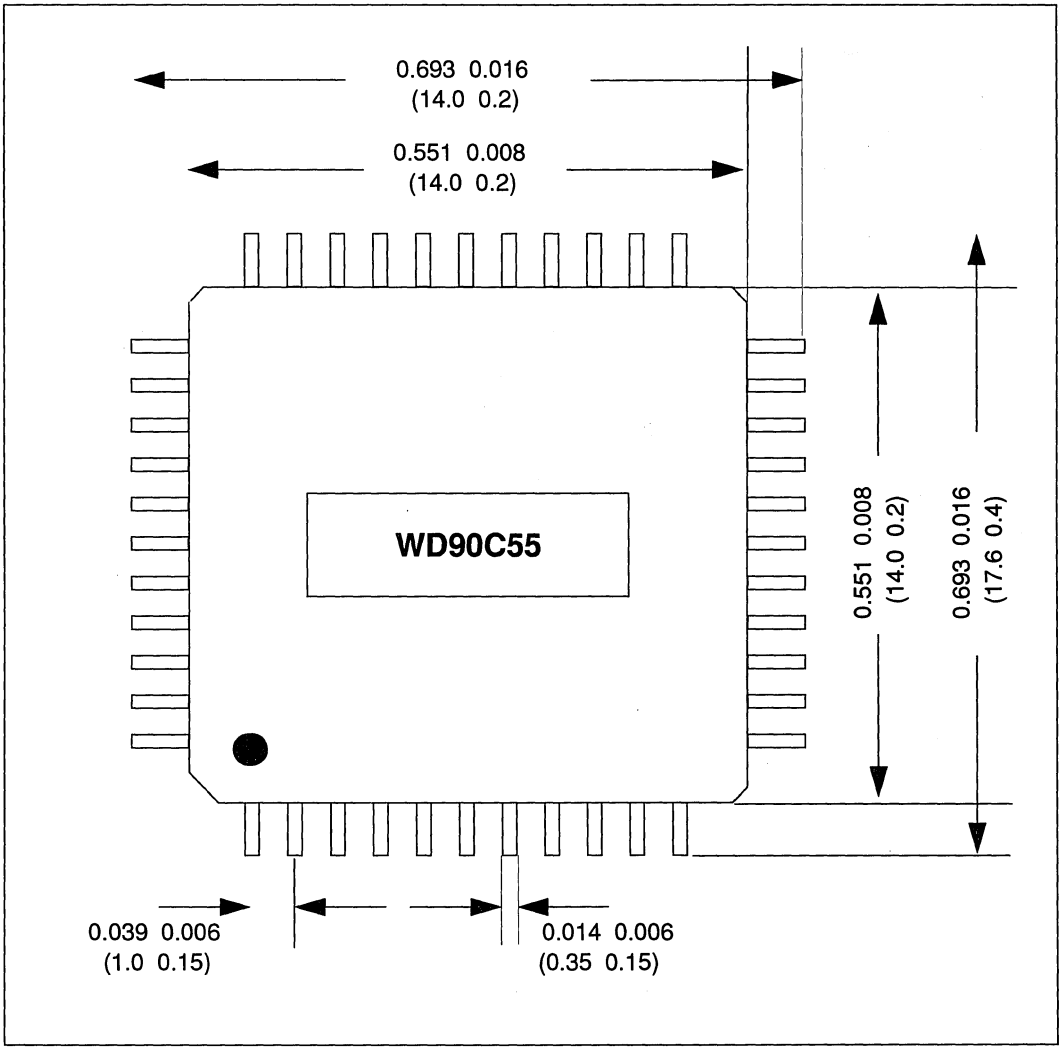

FIGURE 7-1 44-PIN LAYOUT MECHANICAL SPECIFICATION

7.2 48-PIN PACKAGE

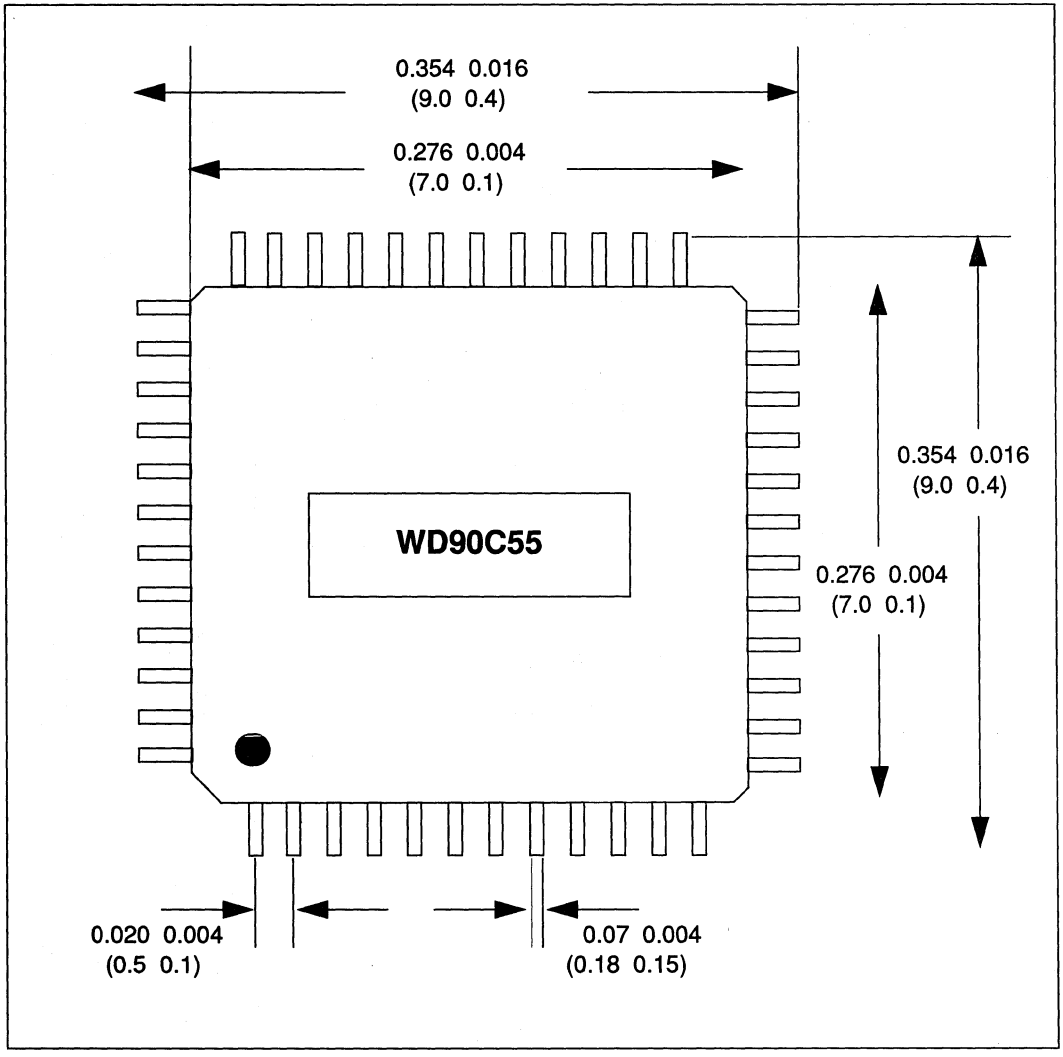

FIGURE 7-2 48-PIN LAYOUT MECHANICAL SPECIFICATION