WD10C22B
Self-Adjusting Data Separator

FEATURES

- Designed specifically for the industry standard WD42C22/WD50C12 Hard Disk Controllers and ST506/412 type Winchester disk drives
- Provides pin-selectable MFM(5 Mbits/sec) or RLL (to 10 Mbits/sec)
- Provides all processing of the sensitive read/write data signals
- Precision internal self-adjusting delay line tracks operating frequency
- Highly stable LC type Voltage Controlled Oscillator
- Precision self-adjusting VCO compensates for component, temperature, voltage, and aging variations
- Uses phase-frequency detection (velocity lock) on crystal reference and on the data synchronization field to eliminate 180 degree lock due to drive asymmetry, and to eliminate harmonic lock due to write splices and other transients
- Zero Phase Startup for faster, more predictable lock acquisition
- Data detector is precisely centered in the window, independently of data frequency
- Window size is automatically optimized as frequency changes
- Write data precompensation automatically set as frequency changes
- "Window shift" allows use of precompensation timing to reduce the read data window for test and error recovery purposes
- Locks to crystal reference while idle
- Dual gain:
  - high for faster acquisition
  - low for more jitter rejection while tracking
- External programmable pump current control
- Precision current reference provides highly accurate pump currents
- Integrated crystal oscillator, with special power-on startup circuitry
- Inexpensive external components
- Will accommodate a variety of data rates through selection of external components
- Available in 28-pin DIP or 28-pin QSM leaded surface mount chip carrier
- Low power, low noise CMOS design
- Special circuitry designed in for unusually good testability
- No inaccurate RC type one shots
- No noisy fast edge bipolar technology circuits

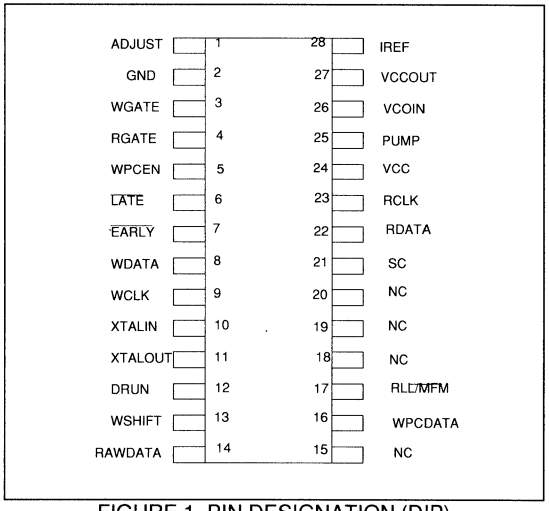


FIGURE 1. PIN DESIGNATION (DIP)

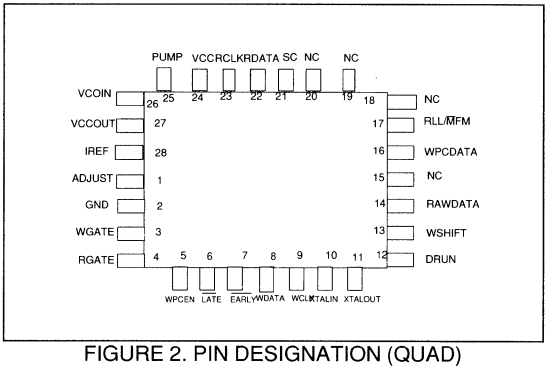


FIGURE 2. PIN DESIGNATION (QUAD)

DESCRIPTION

The WD10C22B Read/Write Channel is an LSI device implemented in 3 micron high-speed CMOS. It is specifically designed to be compatible with the Western Digital WD42C22/WD50C12 series of Hard Disk Controllers, and with disk drives conforming to the popular ST506/412 interface standard and recent speed-enhanced versions. In a typical application, it performs all of the handling of the sensitive read/write signals between a Hard Disk Controller and data drivers and receivers. Read data corresponds to previous write data, with added phase, frequency, and write splice noise. The fundamental purpose of the WD10C22B is to remove these sources of noise, and present a clean digital read signal to the Hard Disk Controller.

The WD10C22B performs phase-locked loop data synchronization on read data from the drive. An on-board synch field detector automatically switches the PLL from the stable crystal reference to the read data. The VCO is halted and restarted in phase with the data to eliminate initial acquisition in the wrong frequency direction. Phase-frequency detection (velocity lock) is used at the beginning of the synch field to quickly and reliably acquire lock to the data. Use of this technique eliminates susceptibility to harmonics and asymmetry. The WD10C22B then switches to phase-only detection to complete the phase acquisition before the end of the synch field, and to enable tracking of random read data. The phase jump at the switchover due to multiplexing, seen in other circuits, is avoided through the use of a proprietary zero phase jump design. When switching to phase detection, the WD10C22B reduces the error amplifier gain for better rejection of drive jitter. A precisely centered detector samples the data at twice the underlying data rate to remove the phase jitter. Another proprietary technique adjusts the window width to the current data rate, providing greater phase margin. The regenerated signal, along with a fixed-phase synchronous clock, are output for the Hard Disk Controller's digital circuits.

The WD10C22B performs conditioning on write data to the drive. Data from the Hard Disk Controller is precisely clocked with a signal at twice the data frequency to minimize digital phase noise. If precompensation is enabled, early, nominal, and late taps on an internal delay line are multiplexed through matched delay paths to produce synchronized, precompensated write data, which is sent directly to the drive's write circuits. The taps are also used to provide a window shift feature so as to enable more stringent and flexible testing of the drive/controller subsystem.

A key feature of the 10C22B is the internal delay line, which is set automatically by the XTALIN frequency.

The device has been designed to work at the 5 Mbit/sec data rate using MFM encoding or up to 10 Mbits/sec data rate using RLL encoding. Other data rates may be accomodated through selection of external components.

The schematic and parts list shown on the following pages reflect an implementation proven out over millions of Western Digital controllers. Complete part specifications including recommended vendors, in both thru-hole and surface mount layouts, are available. Contact your local Western Digital sales representative for more information.

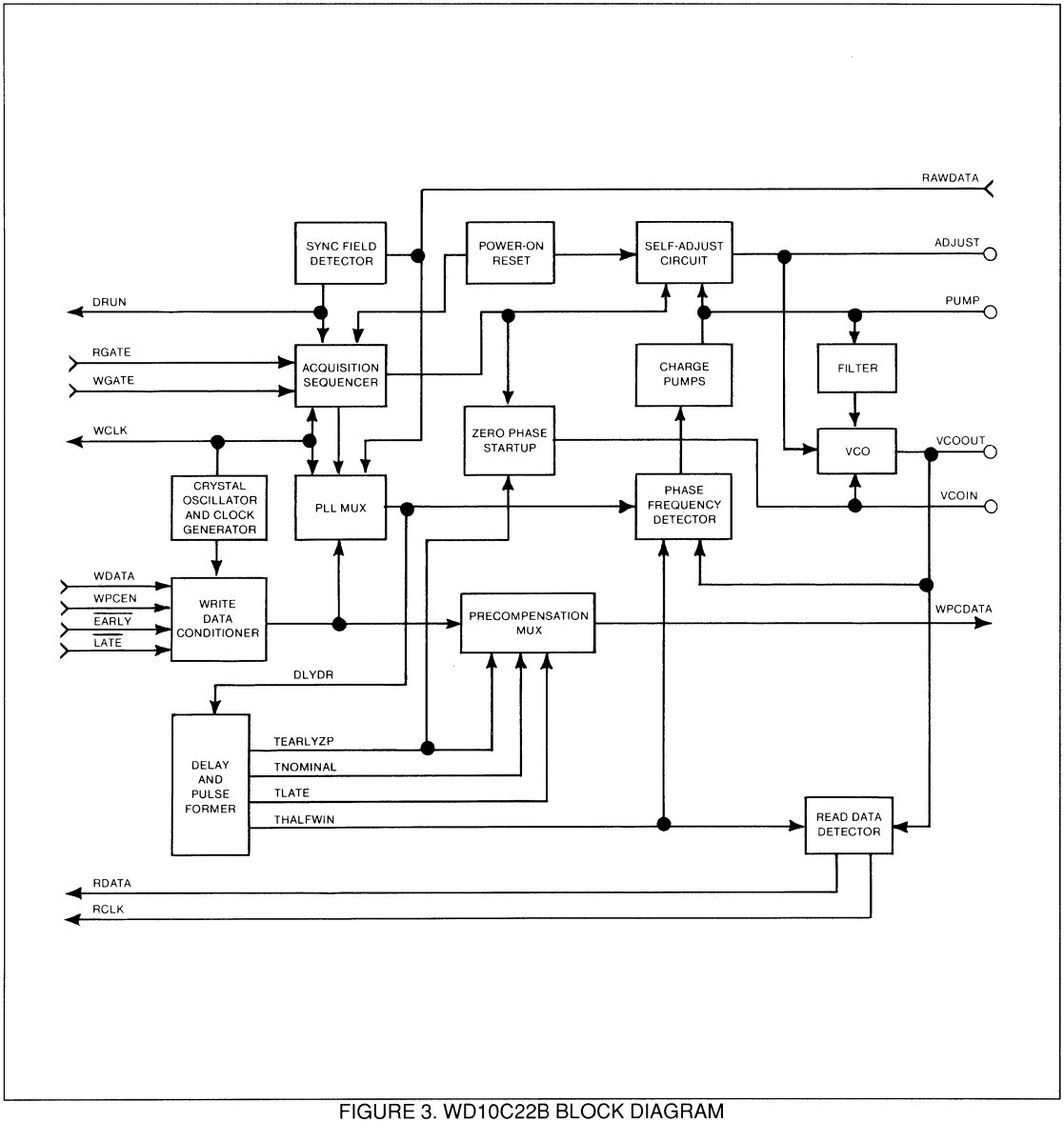


FIGURE 3. WD10C22B BLOCK DIAGRAM

EXTERNAL COMPONENTS PARTS LIST

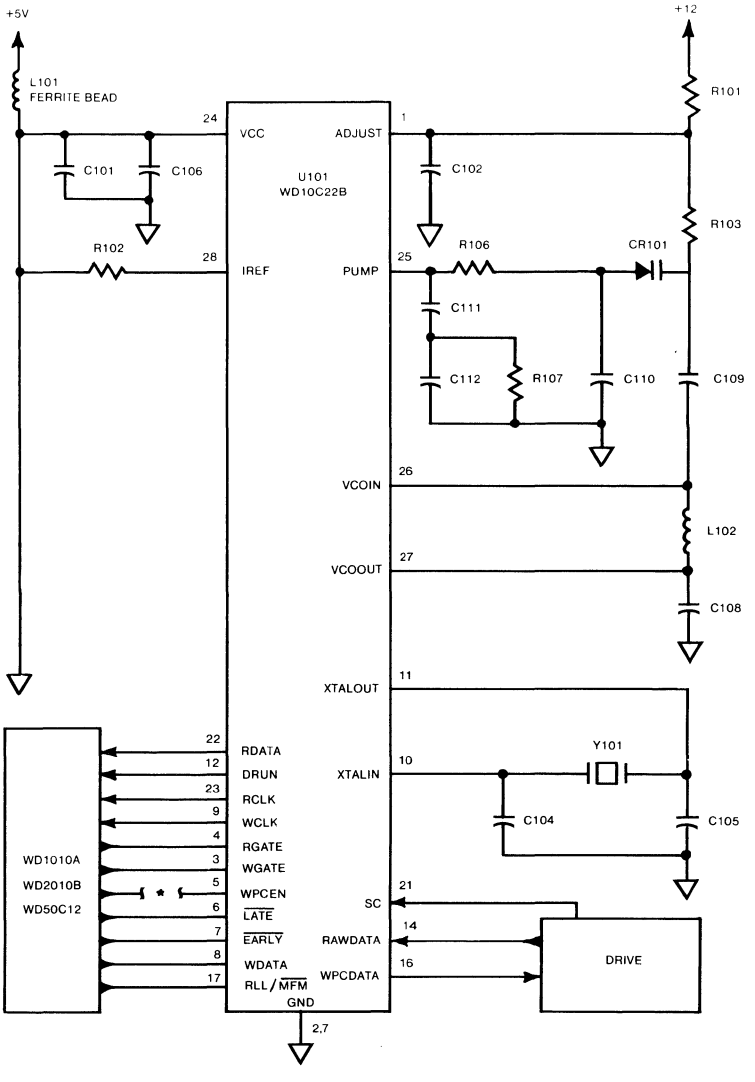
The parts list shown below gives typical component values for 5 Mbit/sec MFM and 7.5 Mbit/sec RLL data rates.

See the diagram on the opposite page for the location of each component.

Contact your local Western Digital sales representative for more information on how to changes these values, to accommodate different data rates.

10C22B EXTERNAL COMPONENTS for 5Mbits/sec (MFM) and 7.5Mbits/sec (RLL)

PART #	MFM	RLL	SPECIFICATIONS
L101	---	---	ferrite bead
C101	0.1 µF	0.1 µF	cer., +80-20%,50V, z5u
C106	1000 pF	1000 pF	cer., ±20%, 50V, x7R
R102	10.0K	10.0K	MF 1%, 1/8 w, 100 ppm
R101	36.5K	36.5 K	MF 1%, 1/8 w, 100 ppm
R103	100K	100 K	CF 5%, 1/4 w
C102	0.1 µF	0.1 µF	TANT ±20%, 25V
L102	4.7 µH	2.2 µH	1%
C108	180 pF	150 pF	cer., 5%,50V, npo
C109	1000 pF	1000 pF	cer., +5%, 50V, npo
C110	180 pF	150 PF	cer., 5%,50V, npo
CR101	---	---	varactor MVAM 109
R106	1.50K	1.50K	MF 1%, 1/8 w, 100 ppm
R107	590 ohm	590 ohm	MF 1%, 1/8, 100 ppm
C111	4700 pF	4700 pF	cer., 5%, 50V, npo
C112	150 pF	150 pF	cer. , 5%, 50V, npo
Y101	10.0 MHz	15.0 MHz	crystal .01%, 0-70C paral
C104	68 pF	33 pF	cer., 5%, 50V, npo
C105	47 pF	22 pF	cer. , 5%, 50V, npo



*RWC CONNECTS TO WPCEN IF REDUCED WRITE CURRENT IS TO START AT THE SAME TIME AS WRITE PRECOMP.

FIGURE 4. EXTERNAL COMPONENTS

Pin Descriptions

Signals have the same pin numbers for both packages.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
14	RAWDATA	RAW DATA	I	Data received from the drive read circuits. Includes an internal pullup resistor to allow tri-state multiplexing of the drives' data receivers.
22	RDATA	READ DATA	O	Detected and regenerated version of RAWDATA. Jitter has been removed and pulses have been synchronized with RCLK.
23	RCLK	READ CLOCK	O	VCOIN divided to half frequency. Tracks the base frequency of RAWDATA during a read operation; otherwise tracks the crystal frequency.
12	DRUN	DATA RUN	O	The output of a frequency detector connected to RAWDATA. Short, high frequency periods cause it to go high; long, low frequency periods cause it to go low.
13	WSHIFT	WINDOW SHIFT	I	Tri-state input. Used during reads to shift the data detection window when testing or performing error recovery. When high, it shifts the data late; when low, it shifts the data early; and when floating, it does no shifting.
4	RGATE	READ GATE	I	Read gate. Set high when the Controller intends to read.
3	WGATE	WRITE GATE	I	Write gate. Set high when recording onto the disk.
8	WDATA	WRITE DATA	I	Write data to be conditioned and sent out through WPCDATA to be written onto the disk.
7	$\overline{\text{EARLY}}$	EARLY	I	Negative true inputs used to advance write data for write precompensation.
6	$\overline{\text{LATE}}$	LATE	I	Negative true inputs used to delay write data for write precompensation.
5	WPCEN	WRITE PRECOMP ENABLE	I	Write precompensation enable. When high, it enables $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$.
16	WPCDATA	WRITE PRECOMP DATA	O	Write data sent to the drive write circuits. Low when WGATE is low.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
10	XTALIN	XTALIN	I	Input pins for a crystal oscillator circuit. If an external frequency source is desired, XTALIN can be driven and XTALOUT left open.
11	XTALOUT	XTALOUT	O	Output pins for a crystal oscillator circuit.
9	WCLK	WRITE CLOCK	O	Clock signal at one half the XTALIN frequency.
19	NC	NO CONNECT	--	Not used. Must leave open.
18	NC	NO CONNECT	--	Not used Must leave open.
20	NC	NO CONNECT	--	Not used. Must leave open.
17	RLL/$\overline{\text{MFM}}$	RLL/$\overline{\text{MFM}}$ SELECT	I	When high, selects RLL (2,7) mode. When low, selects MFM (1,3) mode.
21	SC	SEEK COMPLETE	I	When low, keeps VCO referenced to XTALIN. In an application, it should be connected to the SC (Seek Complete) pin of the Hard Disk Controller.
15	NC	NO CONNECT	--	Not used. Must leave open.
25	PUMP	PUMP	I/O	Charge pump output to the PLL filter. Also a voltage input to the self adjust sensing (VSENSE) circuitry.
26	VCOIN	VCO INPUT	I/O	Input/output of the VCO gain stage. VCOIN is clamped high and then released during Zero Phase Startup.
27	VCOOUT	VCO OUTPUT	O	Output of the VCO gain stage.
1	ADJUST	ADJUST	O	Output pin for self calibration of the PLL.
28	IREF	IREF	I/O	An external resistor connected to this pin sets the magnitude of the charge pump current.
2	GND	GROUND	I	GROUND
24	V_{CC}	POWER SUPPLY	I	+5 Volts. Power supply input.

PIN NUMBER	NAME	TYPE	DIODE CLAMP	PULL-UP PULL-DOWN	COMMENTS
1	ADJUST	O	NEG	----	Open NFET drain
2	GND	I	----	---	----
3	WGATE	I	NEG	----	TTL
4	RGATE	I	NEG	----	TTL
5	WPCEN	I	NEG	----	TTL
6	LATE	I	NEG/POS	PU	TTL
7	EARLY	I	NEG/POS	PU	TTL
8	WDATA	I	NEG/POS	PU	TTL
9	WCLK	I/O	NEG/POS	----	TTL/MOS
10	XTALIN	I/O	NEG/POS	---	TTL/MOS,Analog,Float. PFET
11	XTALOUT	O	NEG/POS	---	3V PFET clamp
12	DRUN	O	NEG/POS	---	MOS, Float. PFET/NFET
13	WSHIFT	I	NEG/POS	PU/PD	Trinary receiver
14	RAWDATA	I	NEG/POS	PU	TTL
15	NC	--	----	---	----
16	WPCDATA	O	NEG	---	TTL
17	RLL/MFM	I	NEG/POS	PU	TTL
18	NC	--	----	---	----
19	NC	--	----	---	----
20	NC	--	----	---	----
21	SC	I	NEG/POS	PU	TTL
22	RDATA	O	NEG/POS	---	MOS, Float. PFET/NFET
23	RCLK	O	NEG/POS	---	MOS, Float. PFET/NFET
24	V_{CC}	I	---	---	---
25	PUMP	I/O	NEG/POS	---	Analog
26	VCOIN	I/O	POS	----	Analog, Float. PFET protection
27	VCOOUT	O	NEG/POS	----	3V PFET clamp
28	IREF	I/O	NEG	----	Float. NFET protection

ARCHITECTURE

The WD10C22B, with the necessary external components, provides the data interface between the WD42C22, or the WD50C12 and an ST506/ST412 compatible drive. There are nine major functional sections within the WD10C22B:

- Synchronization Field Detector
- Acquisition Sequencer
- Phase-locked Loop (PLL)
  - Phase-Frequency Detector
  - Charge Pumps
  - Filter
  - Voltage Controller Oscillator (VCO)
  - Zero Phase Startup Circuit
- Self Adjustment Circuit
- Read Data Detector
- Crystal Oscillator
- Write Data Conditioner
- Delay and Pulse Former
- Power-on Reset

SYNCHRONIZATION FIELD DETECTOR

The purpose of this circuit is to reliability discriminate between the high frequency of a PLL synchronization field and the lower frequencies immediately preceding it. The criterion used is pulse period discrimination on RAWDATA. If the period between consecutive rising edges of RAWDATA is short with respect to the threshold, then DRUN will go high; if long, then DRUN will go low.The pulses in the synchronization field have the shortest period in the format. The optimum discrimination threshold is set using an internal delay line.

ACQUISITION SEQUENCER

The Acquisition Sequencer sends sequencing control signals to the Synchronization Field Detector, Zero Phase Startup, Charge Pump, VCO, Read Data Detector, and Phase-Frequency Detector circuits when the WD10C22B is switching between the read, write, and idle modes. In addition, it controls a MUX which steers either read data, write data, or crystal divided by two to the delay line, and selects either the delayed read data, delayed crystal divided by two, or an undelayed crystal divided by two as the source for the Phase-Frequency Detector's data input.

When switching from the idle to the read mode, the Acquisition Sequencer invokes the Zero Phase Startup Circuit, which in turn disables the Phase-Frequency Detector and Charge Pumps. It switches the MUX source from crystal divided by two, to delayed read data, and selects the velocity lock mode of the Phase-Frequency Detector.After the Zero Phase Startup is complete, the Phase-Frequency Detector and Charge Pumps are enabled. In velocity lock mode, the Charge Pumps are set to high gain and the VCO frequency, internally divided by two (MFM) or three (RLL) is passed to the Phase-Frequency Detector's clock input. Velocity lock remains for six byte times, after which the Acquisition Sequencer selects the phase lock mode of the Phase-Frequency Detector, passing the VCO frequency without division, sets the Charge Pumps to low gain, and puts the Synchronization Field Detector to sleep.

When switching from the read to the idle mode, the Acquisition Sequencer invokes the Zero Phase Startup Circuit, disabling the Phase-Frequency Detector and Charge Pumps. It switches the MUX source from delayed read data to delayed crystal divided by two, selects the velocity lock mode of the Phase-Frequency Detector, and enables the Synchronization Field Detector. After the Zero Phase Startup is complete, the Phase-Frequency Detector and Charge Pumps are enabled.

When switching from the idle to the write mode, the Acquisition Sequencer switches the MUX source to undelayed crystal divided by two, freeing the delay line taps for utilization by the Write Data Conditioner's precompensation function. The velocity lock mode of the Phase-Frequency Detector is maintained, and the Synchronization Field Detector is put to sleep.

When switching from the write to the idle mode, the Acquisition Sequencer maintains as the MUX source, undelayed crystal divided by two, maintains the velocity lock mode of the Phase-Frequency Detector, and enables the Synchronization Field Detector.

PHASE-LOCKED LOOP (PLL)

Phase-Frequency Detector

The Phase-Frequency Detector can be operated in two modes. The velocity lock mode is used for acquisition when the PLL is switched to read data, and is always used when the PLL is following the reference crystal oscillator. Whenever the device is not reading, the PLL is locked to XTALIN. The second mode, phase lock, is standard phase-only detection. The Acquisition Sequencer switches to this mode when frequency acquisition is essentially complete on data, and phase acquisition is nearly complete as well. A proprietary technique has been employed to guarantee zero phase off set due to switching from the reference crystal to data. Phase-only mode must, of course, be used to lock to the data following the synch field, since that will contain the three frequencies inherent in MFM or the six frequencies inherent in RLL mode.

In either mode, the Phase-Frequency detector converts a phase difference between the VCO and input to a pulse width equal to the phase difference. The polarity of the phase error determines whether a signal will be routed to the pump up or pump down circuitry in the Charge Pump section.

Charge Pumps

This circuit converts the pulse widths received from the Phase-Frequency Detector to proportional amounts of charge into or out of the Filter. The gain of the Charge Pumps is proportional to the input current on the IREF pin. This current is set by an external resistor connected to VCC. When in velocity lock mode, the pumps are set approximately 40 IREF. When in phase lock, the gain is reduced by half.

Filter

The Filter converts the current pulses from the Charge Pumps to a voltage output to the VCO.

The Filter must be carefully designed to the specific requirements of damping factor, acquisition time, capture range, and jitter rejection; and within the context of its effect on VCO operation. Roughly speaking, it functions to filter out high frequency signals due to RAWDATA read data jitter, while passing the low frequency signals associated with the more slowly varying underlying frequency of RAWDATA, and handling a step change in input frequency when switching between drive data and crystal.

Voltage Controlled Oscillator(VCO)

The VCO is a series resonant LC oscillator. The active gain element provides the energy to sustain the oscillation between the VCOIN and the VCOOUT pins within the WD10C22B. The VCO is controlled and tuned with an inexpensive varactor. The filter is connected to the anode of the varactor, providing the voltage for loop operation of the PLL. Note that higher voltages at the VCO input correspond to lower frequencies, and vice-versa. The cathode of the varactor is connected to the Self-Adjustment Circuit. The voltage bias on the cathode determines the location on the VCO's V-F characteristic curve. The voltage bias is set for a voltage favorable to the charge pumps at the nominal frequency of the VCO.

Zero Phase Startup Circuit

The Zero Phase Startup circuit is a set of logic and a clamp on the VCOIN pin. When the Acquisition Sequencer switches the PLL input signal upon transitions into or out of the read mode, the logic turns on the clamp for a minimum of one input data period (typical duration is three input data periods). The clamp stops the operation of the VCO oscillator gain stage and removes the AC energy from the passive VCO components. This puts the VCO into a known state, so there is a predictable time from release of the clamp until the first VCO edge reaches the Phase-Frequency Detector.

Self Adjustment Circuit

The Self Adjustment Circuit tunes the VCO so that its nominal output frequency of twice the data rate will correspond to an input voltage favorable to the Charge Pumps. This voltage is one half of VCC, and centers the capture range. An internal comparator connected to the PUMP pin detects whether the voltage into the VCO is above or below this threshold voltage, called VSENSE.The comparator drives a current sink connected to the ADJUST pin. Externally, a resistor to +12 volts is connected to the ADJUST pin to convert the current to a voltage. A large capacitor is also connected to the ADJUST pin to heavily filter transients. A large value resistor from the ADJUST pin to the cathode of the VCO varactor completes the circuit. The Self Adjustment Circuit functions to slowly keep the VCO's input voltage near the VSENSE level. It not only performs compensation for component variations in the same way that a manual adjustment would, but it also compen-

sates for dynamic variations such as voltage, temperature, and aging. Another beneficial characteristic of this circuit is heavy RC filtering of the +12 volt supply. The Self Adjustment Circuit is disabled during acquisition to read data, to guard against unfavorable high gain responses to high frequency non-synch data patterns.

READ DATA DETECTOR

This circuit produces the signals RCLK and RDATA. RCLK is a square wave at one half the VCO frequency. During data tracking, the frequency of RCLK mirrors the slowly varying frequency of the RAWDATA read data. RDATA is a regenerated form of RAWDATA, with all jitter removed and positive pulses one window wide. It is synchronous with RCLK. RCLK edges occur nominally in the center of RDATA pulses to allow sufficient setup and hold time for the digital circuits in the Hard Disk Controller that use these signals. RDATA is DC low during velocity lock, and is activated by the Acquisition Sequencer approximately at the transition to phase lock.

CRYSTAL OSCILLATOR

The Crystal Oscillator is designed to operate in the parallel resonant mode, with an external crystal and two capacitors. It generates the WCLK signal used externally. Internally, various divisions of it are used by the Acquisition Sequencer, Write Data Conditioner, Phase Locked Loop, and Delay Line circuits.

When an externally generated clock is desired, the crystal and capacitors are omitted. The XTALIN pin is connected to the clock source, with XTALOUT left unconnected.

The oscillator circuit includes a special (patent pending) implementation to better ensure startup and to startup more quickly. A low value resistor is connected across the gain stage during the internal power-on reset. This quickly charges the external capacitors to the threshold value. As the resistor is disconnected, capacitive coupling induces a transient into the circuit, which helps to quickly achieve oscillation. A high value resistor is always present.

The oscillator should not be connected to any external circuits.

WRITE DATA CONDITIONER

The Write Data Conditioner samples and precisely synchronizes WDATA, EARLY, and LATE on the rising and falling edges of WCLK. They are immediately pipelined into flip-flops that are sampled on one edge of the XTALIN frequency (twice WCLK) to remove all jitter due to differential rise and fall times of WCLK. When WGATE is active, the synchronized WDATA is channeled through the MUX and passes through internal delay stages. If WPCEN is low, then the nominal delay is selected and passed to the WPCDATA output pin. If WPCEN is high, then the EARLY and LATE signals will select the early or late delays, respectively. If both EARLY and LATE are inactive, or in the illegal case when they are simultaneously active, the nominal delay will be selected. The differential delay between the early WPCDATA and nominal WPCDATA defines the amount of early precompensation, and similary, nominal WPCDATA to late WPCDATA defines the amount of late precompensation. The value is nominally 12.5ns at 5MHz MFM or 8.3 nsec at 7.5 MHz RLL, inversely proportional to frequency.

In MFM mode (RLL/MFM pin low) when WGATE goes high, one of the initial pulses is suppressed to create an interval of two bit times. This ensures that DRUN will go low at the beginning of a data synch field, initializing the Acquisition Sequencer. When WGATE goes low, WPCDATA will be held low.

DELAY LINE AND PULSE FORMER

This section includes the integrated delay lines and RAWDATA pulse forming logic of the WD10C22B.

Pulse forming on RAWDATA is utilized to provide internal pulses suitable for use by the Synchronization Field Detector and Delay Line. In response to input rising edges on RAWDATA, it produces internal positive pulses terminated by a

Delay Line tap. Their widths are slightly longer than half the detection window.

Delay Line taps are also used for the following: write precompensation; window shifting; data frequency discrimination; and the Phase-Frequency Detector's early/late windows (phase-lock mode).

POWER-ON RESET

This integrated function is used to reliably initialize the flip-flops to a predictable state during the application of VCC. It is also used by the Crystal Oscillator startup circuit.

SYNCHRONIZATION FIELD DETECTOR

This circuit reliably detects high and low frequencies or RAWDATA. Pulse period discrimination is used to cause DRUN to stay true during synch fields and to not remain true in the gaps preceding the synch field. Discrimination requires the sync field to be the highest frequency in the encoding scheme [2 windows for MFM (1,3) and 3 windows for RLL (2,7)].

PHASE-LOCKED LOOP:

When used in a 5Mbit/sec application with the recommended Western Digital components (see page 4), the following system performance can be achieved.

PHASE-LOCKED LOOP:

Acquisition Time	<12.8 µsec (16 µsec from DRUN high)		
Capture Range	>±2.2% (±1% drive ±.1% crystal osc.)		
Jitter Rejection	>40db at 2.5 MHz		
Damping Factor (Velocity Lock)	min .7	typ 1	max 1.4
Damping Factor (Phase Lock)	min.5	typ .7	max 1.1
Ko VCO Gain (per volt)	min 4.5%	typ 6%	max 7.5%

DC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{CC} with respect to GROUND:	+5.5 volts
Max voltage on any pin with respect to GROUND, (except ADJUST, XTALIN, and VCOIN):	-0.5 to V_{CC}+0.5 volts
Max voltage on ADJUST with respect to GROUND:	-0.5 to +13.2 volts
Max voltage on XTALIN and VCOIN with respect to GROUND:	-5.0 to V_{CC}+0.5 volts
DC Operating Characteristics over:	T_a = 0 to 70 deg. C;
	V_{CC}=+5.0V±5%

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the above.

Digital Signals

Input Signals: RGATE, WGATE, SC, WPCEN, WDATA, $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$, RAWDATA, RLL/$\overline{\text{MFM}}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	2.5			V	
V_{IL}	Voltage input low			0.8	V	

Input Signals: XTALIN (TTL)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	2.4			V	
V_{IL}	Voltage input low			0.4	V	

Input Signals: RGATE,WGATE,WPCEN,VCOIN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{IN}	Input leakage current			±10	µA	V_{IN}=GND to V_{CC}

For the case of VCOIN, leakage is measured with the Zero Phase Startup Clamp off.

Input Signals: WDATA, $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{IH}	Input high current	-0.5			mA	V_{IH}= 2.4 V*
I_{IL}	Input low currrent			-4	mA	V_{IL}=0.45 V*

* Internal pullup resistor.

Input Signals: RAWDATA, SC, RLL/$\overline{\text{MFM}}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{IH}	Input high current	-0.1			mA	V_{IH}=2.4 V*
I_{IL}	Input low current			-1.0	mA	V_{IL}=0.4 V*

* Internal pullup resistor.

Input Signal: WSHIFT

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	$0.8V_{CC}$			V	
V_{IT}	Voltage input 3-st volt	$0.4V_{CC}$		$0.6V_{CC}$	V	
V_{IZ}	Voltage input high Z	$.47V_{CC}$		$.53V_{CC}$	V	I_{IN}=0
V_{IL}	Voltage input low			$0.2V_{CC}$	V	
I_{IH}	Input high current	0.2		0.7	mA	V_{IH}=4.4 V, *
I_{IZ}	Input high Z current	±50.0			µA	$V_{IN}\leq.4V_{CC}$; $V_{IN}\geq.6V_{CC}$, *
I_{IL}	Input low current	-0.2		-0.7	mA	V_{IL}=0.6 V, *

* Internal pullup and pulldown resistors

Power Supply Currents

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CCA}	5v active current		40	75	mA	10Kohm on IREF
I_{CCS}	5v static current		2	15	mA	**

** Static I_{CC} is measured with XTALIN and VCOIN held high; WGATE, RGATE, WPCEN, ADJUST, and IREF held low; and the remaining pins open.

Outputs:WPCDATA

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output high volt	2.4			V	I_{OH}=-0.4mA
V_{OL}	Output low volt			0.4	V	I_{OL}=+2.0mA
t_{RISE}	Rise time			7	nsec	0.8 to 2.0 V, LOAD=L1; See Note
t_{FALL}	Fall time			3	nsec	2.0 to 0.8 V; LOAD=L2; See Note

Outputs: DRUN† (non-TTL)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output high volt	4.65			V	I_{OH}=-20 µA
V_{OL}	Output low volt			0.2	V	I_{OL}=+20 µA
t_{RISE}	Rise time			28	nsec	0.9 to 4.2 V; Load=L3; See Note
t_{FALL}	Fall time			19	nsec	4.2 to 0.9 V; Load=L3; See Note

Outputs: DRUN† (TTL)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output high volt	2.4			V	I_{OH}=-20 µA
V_{OL}	Output low volt			0.4	V	I_{OL}=+20 µA
t_{RISE}	Rise time			7	nsec	0.8 to 2.0 V; Load=L3; See Note
t_{FALL}	Fall time			8	nsec	2.0 to 0.8 V; Load=L3; See Note

Output: RCLK†, RDATA†, WCLK‡ (non-TTL)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output high volt	4.65			V	I_{OH}= -0.1mA
V_{OL}	Output low volt			0.2	V	I_{OL}= +1.0mA
t_{RISE}	Rise time			29	nsec	0.9 to 4.2 V; Load=L4; See Note
t_{FALL}	Fall time			15	nsec	4.2 to 0.9 V; Load=L5; See Note

Output: RCLK†, RDATA†, WCLK‡ (TTL)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output high volt	2.0			V	I_{OH}=-1 mA
V_{OL}	Output low volt			0.4	V	I_{OL}=+4 mA
t_{RISE}	Rise time			7	nsec	0.8 to 2.0 V; Load=L4; See Note
t_{FALL}	Fall time			8	nsec	2.0 to 0.8 V; Load=L5; See Note

† The DRUN, RCLK, and RDATA signals each have two output requirements. The 5 Mbit WD1010/2010 input signals DRUN, RCLK and RDATA require wide voltage swings. The WD42C22/50C12 requires TTL levels. These two output requirements are listed separately.

‡ WCLK has two output requirements. WCLK must be able to drive the wide voltage swings of the 5Mbit WD1010/2010's, and simultaneously drive one TTL clock buffer device. These two output requirements are listed separately. The two loads are combined.

Note: Load circuits

Applies to the previous conditions where the total load is listed as L1, L2, L3, L4, or L5.

LOAD	C to GND	R to GND	R to V_{CC}
L1	20 pf	20 K	---
L2	20 pf	--	2 K
L3	20 pf	--	--
L4	30 pf	20 K	---
L5	30 pf	--	2 K

Analog Signals

Input: XTALIN (non-TTL)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LKX}	Input leakage currents			±100	nA	V_{IN},V_{OUT}=V_{IBIAS}

Leakage measured after the internal Power-On Reset has timed out.

Output: XTALOUT

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{OLS}	Short circuit sink current	8		65	mA	V_{CC}=+5; XTALIN,XTALOUT=+2.5V
I_{OHS}	Short circuit source current	-1.5		-9.0	mA	V_{CC}=+5; XTALIN,XTALOUT=GND
V_{CLMP}	V_{OH} clamp voltage	2.3		3.7	V	XTALIN=-1V;V_{CC}=+5V
R_{BO}	Operating bias resistance	1.0		9.5	Mohm	*
R_{BP}	Power on reset bias resistance	15		100	Kohm	**
V_{IBIAS}	Input bias volt	0.8		1.8	V	XTALOUT floating; I_{IL},I_{IH}=0µA

* R_{BO} is computed as a parallel resistance to the leakage resistance R_{LKX} = V_{IBIAS}/I_{LKX}. With XTALIN=V_{CC}, XTALOUT=GND, the measured current on XTALIN is given by $V_{CC}(1/R_{BO}+1/R_{LKX})$.

** R_{BP} is the parallel combination of R_{BO} and an additional resistor activated during power on reset. R_{BP} is computed by measuring the XTALIN current with XTALIN = V_{CC}, XTALOUT = GND during t_{POT} (see the section Timing Characteristics describing Power-on Reset).

Output: VCOOUT

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{OLS}	Short circuit sink current	8		25	mA	V_{CC}=+5; VCOIN,VCOOUT=+2.5V
I_{OHS}	Short circuit source current	-1.5		-9.0	mA	V_{CC}=+5: VCOIN,VCOOUT=GND
V_{CLMP}	V_{OH} clamp voltage	2.3		3.7	V	VCOIN=-1V;V_{CC}=+5V
R_{SO}	Series output resistance	70		165	ohms	
V_{IBIAS}	Input bias volt	0.75		1.6	V	2 Megohms across VCOIN and VCOOUT; VCOOUT floating; I_{IL},I_{IH}=0 µA

Input/Output: IREF

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	
V_{IREF}	IREF voltage	0.42V_{CC}		0.58V_{CC}	V	10Kohm±1% resistor connected between IREF and V_{CC}

POWER-ON Reset Voltages

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	
V_{RON}	Reset min V_{CC} on		3		V	Min. V_{CC} voltage required to meet the requirements of the timing t_{CUP}
V_{ROFF}	Reset V_{CC} off		3		V	V_{CC} voltage at which the device activates its internal power-on reset signal

Output: ADJUST

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{SH}	ADJUST max threshold	.48V_{CC}		.63V_{CC}	V	V_{PUMP} at V_{ADJ} =+6V,200µA
V_{SL}	ADJUST min. threshold	.47V_{CC}		.57V_{CC}	V	V_{PUMP} at V_{ADJ} =+10V,20µA
V_{SD}	V_{SENSE} delta			300	mV	V_{SH}-V_{SL}
V_{ADJ}	ADJUST voltage range	0		13.2	V	*
I_{AJMX}	ADJUST maximum current			2.5	mA	Measured with PUMP voltage forced to VCC and ADJUST voltage forced to +10V
I_{LKA}	ADJUST off leakage			±10	µA	V_{ADJ} = GND to 13.2V; V_{PUMP} = GND

* This parameter defines what voltages may appear on the ADJUST pin in operation. 13.2 volts could be on the ADJUST pin if the +12V supply is on when V_{CC} is off.

Input/Output: PUMP

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS*
I_{LKP}	Tristate leakage			±10	µA	V_{PUMP} = GND to V_{CC}
I_{PHUN}	Nom higain pump up	-8.25		-11.75	mA	V_{PUMP} =V_{SH},V_{SL}
I_{PHDN}	Nom higain pump dn	8.25		11.75	mA	V_{PUMP} =V_{SH},V_{SL}
I_{PLUN}	Nom lowgain pump up	-3.75		-6.25	mA	V_{PUMP} =V_{SH},V_{SL}
I_{PLDN}	Nom lowgain pump dn	3.75		6.25	mA	V_{PUMP} =V_{SH},V_{SL}
I_{PHU}	Higain pump up	-7.00		-13.00	mA	V_{PMP} = V_{SH} + L+M; V_{PMP} = V_{SL}-K-L-M
I_{PHD}	Higain pump down	7.00		13.00	mA	V_{PMP} = V_{SH} +L+M; V_{PMP} = V_{SL}-K-L-M
I_{PLU}	Lowgain pump up	-3.00		-7.00	mA	V_{PMP} = V_{SH} + L; V_{PMP} = V_{SL}-K-L
I_{PLD}	Lowgain pump down	3.00		7.00	mA	V_{PMP} = V_{SH} +L; V_{PMP} = V_{SL}-K-L
R_{BALA}	ErrAmp bal ratio acquisition	0.8		1.2		V_{SL} -K-L-M ≤ V_{PMP} ≤ V_{SH} +L+M
R_{BALT}	ErrAmp bal ratio tracking	0.8		1.2		V_{SL} - K-L ≤ V_{PMP} ≤ V_{SH} +L
R_{KD}	ErrAmp gain ratio	1.8		2.2		V_{SL} -K- L ≤ V_{PMP} ≤ V_{SH} +L

* Pump currents are specified over V_{CC}±5%, ADJUST supply 12v±10%, IREF resistor 10Kohm±1%, ADJUST resistor 36.5Kohm±1%, worst case process variations, temperature, and the measured V_{SH} and V_{SL} values with K = 50mV, L = 550mV, and M = 110mV. Balance ratios are specified as up:down for R_{BAL}, and acquisition:tracking for R_{KD}.

Timing Characteristics

The following are timings that are independent of the application of the device, and have been, where applicable, expressed in terms of the data frequency by W(indow) = 1/(2x NRZ data frequency), for data frequencies in the range of 1 to 15MBit/sec.

Several timings are referenced using a phase relationship of input signals called NULL. When the PLL is acquiring data in velocity lock mode, for a given set of conditions there is one phase of RAWDATA with respect to VCOIN which results in zero net current on PUMP. This phase is called NULLV. The equivalent phase relationship found when the PLL is tracking data in phase detection mode is called NULLP. When the PLL is tracking the crystal, the corresponding NULL, NULLX, refers to the equivalent phase between XTALIN and VCOIN.

Timing on signals WCLK, RDATA, and RCLK, unlike the earlier 10C2x devices, is measured from the 1.4 V transitions. While these timings have not been specified for the voltage halfway between the WD1010/2010's V_{IH} and V_{IL} of 2.55 Volts, the WD10C22B's performance is compatible with those parts at 5Mbits/sec MFM data rates.

Disk Drive Read Data

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{RDH}	RAWDATA pulse width high	20			nsec	
t_{RDL}	RAWDATA pulse width low	20			nsec	
t_{RDT}	RAWDATA period	100			nsec	Min time required between two consecutive RAWDATA pulses*

* The limiting factor is one of the following:

a. Phase detector recycle time

b. Delay line minimum pulse width low propagation

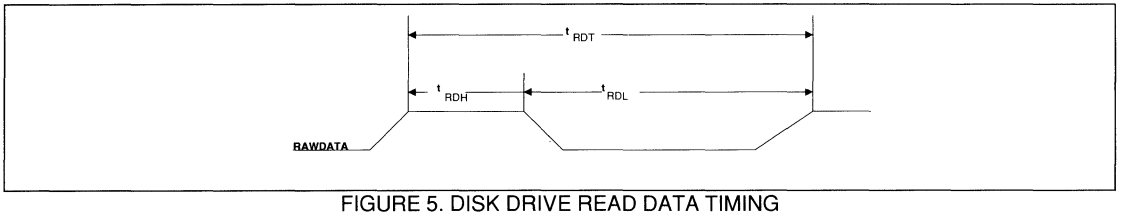


FIGURE 5. DISK DRIVE READ DATA TIMING

Read Data Conditioner

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS*
t_{RDP}	RDATA pulse width	W-5	W	W+10	nsec	*
t_{RCP}	RCLK pulse width	W-5	W	W+5	nsec	*
t_{X1}	RCLK transition to RDATA rising	W/2-15	W/2	---	nsec	*
t_{X2}	RDATA rising to RCLK transition	W/2-5	W/2	---	nsec	*

* Measured under either of the following conditions for VCOIN:

a. VCOIN generated from external components, conforming to WD application specifications

b. VCOIN's $V_{IH/L}$ at $V_{IBIAS} \pm 1.5v$, and with a 50% duty cycle measured at the V_{IBIAS} crossings (i.e. $t_{VCL}=t_{VCH}$)

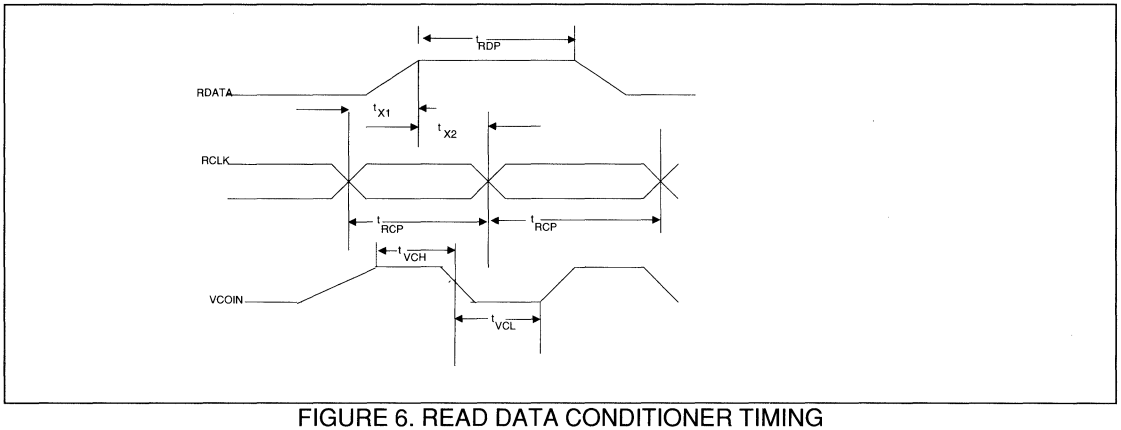


FIGURE 6. READ DATA CONDITIONER TIMING

Read Data Detector

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS*
t_{DDW}	Data Detect Window	W-2	W	W+2	nsec	WSHIFT floating,**
t_{DWE}	DDET Early Window	W/2-5	W/2	W/2+5	nsec	WSHIFT floating
t_{DWL}	DDET Late Window	W/2-5	W/2	W/2+5	nsec	WSHIFT floating
t_{DSE}	DDET Shift Early Window	W/8-5	W/8	W/8+5	nsec	WSHIFT active low
t_{DSL}	DDET Shift Late Window	W/8-5	W/8	W/8+5	nsec	WSHIFT active high

* Using the NULLP phase as a reference, input data is shifted incrementally to the minimum phase offset at which output data, seen on RDATA, is incorrect. Measured under either of the following conditions for VCOIN:

a. VCOIN generated from external components which conform to WD application specifications

b. VCOIN's $V_{IH/L}$ at $V_{IBIAS} \pm 1.5v$, and with a 50% duty cycle measured at the V_{IBIAS} crossings (i.e. $t_{VCL} = t_{VCH}$). For this case, t_{DWE} and t_{DWL} should be offset from their measured values by +2.5ns and -2.5ns respectively, to compensate for measurement technique error.

** The data detection window maximum is specified as greater than W only to allow for tester inaccuracy and/or statistical error in the measurement. For a statistically significant sample, if one were to plot the probability of successful decode of a bit versus time, the data detection window must be W when defined as the time between the points for which the probability function is 0.5.

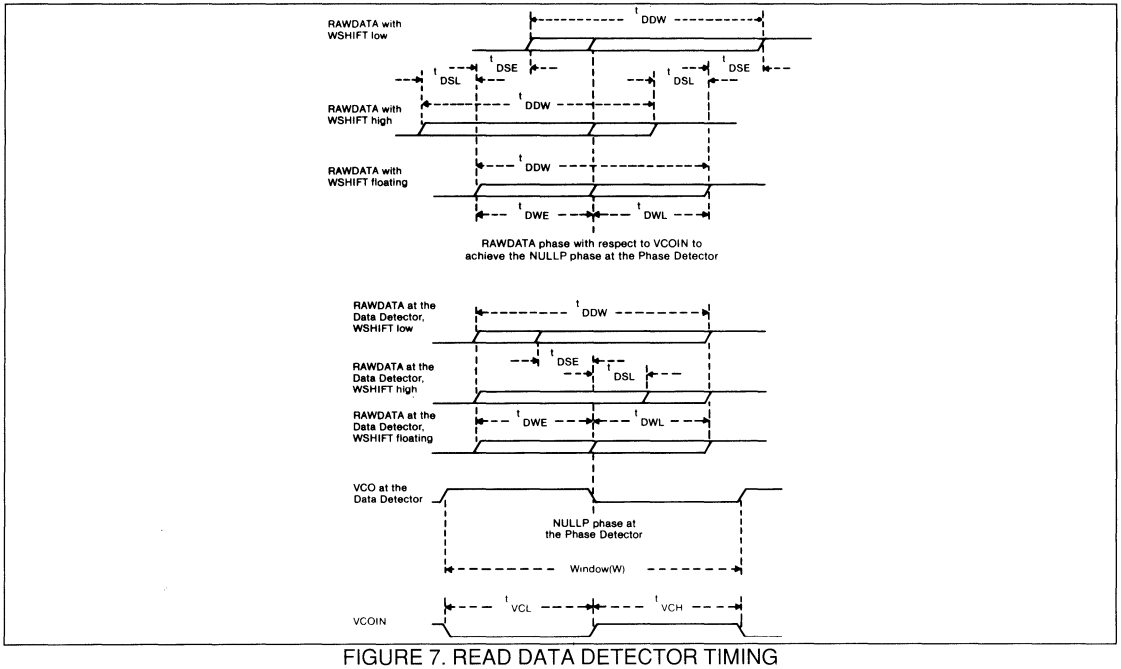


FIGURE 7. READ DATA DETECTOR TIMING

Read Data Frequency Detector (MFM)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS*
t_{DRH}	DRUN high freq	$1/\{(2.625/f_{XTL}) - 0.015\}$		MHz	Min. RAWDATA freq for DRUN high
t_{DRL}	DRUN low freq		$1/\{(2.625/f_{XTL}) + 0.01\}$	MHz	Max. RAWDATA freq for DRUN to go low on every RAWDATA period

* f_{XTL} is the XTALIN frequency specified in MHz (i.e. 10 for 10MHz)

Read Data Frequency Detector (RLL)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS*
t_{DRH}	DRUN high freq	$1/\{(3.500/f_{XTL}) - 0.02\}$		MHz	Min. RAWDATA freq for DRUN high
t_{DRL}	DRUN low freq		$1/\{(3.500/f_{XTL}) + 0.01\}$	MHz	Max. RAWDATA freq for DRUN to go low on every RAWDATA period

* f_{XTL} is the XTALIN frequency specified in MHz (i.e. 10 for 10MHz)

Phase-Frequency Detector

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{NPV}	NULLP-NULLV		±1		nsec	
t_{WPV}	NULLPW - NULLVW		±1		nsec	
t_{PWS}	NULLP - NULLPW	-3	±1	1	nsec	
t_{VWS}	NULLV - NULLVW		±1		nsec	

Phase Detection Mode

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS*†
t_{PDW}	Phase Detect Window	W-2	W	W+2	nsec	**
t_{PWE}	PDET Early window	W/2-5	W/2	W/2+5	nsec	
t_{PWL}	PDET Late window	W/2-5	W/2	W/2+5	nsec	

* Measured in phase detection mode only

** Because of the periodic nature of t_{PDW}, this must be exactly equal to W, as defined by the inverse of the VCOIN frequency. t_{PDW}, in addition to checking for obscure defects on the device, checks the device tester's accuracy.

† The end points of each of these phase timings corresponds to zero average current on the PUMP pin. The "vertical"lines shown at the PUMP up/down decision points have a significant finite slope.

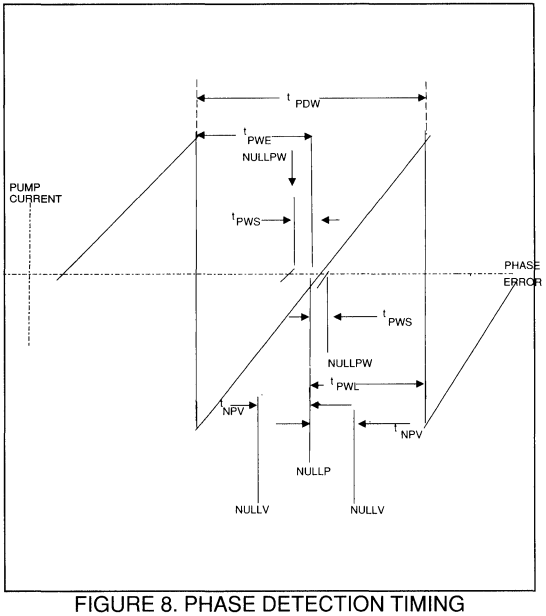


FIGURE 8. PHASE DETECTION TIMING

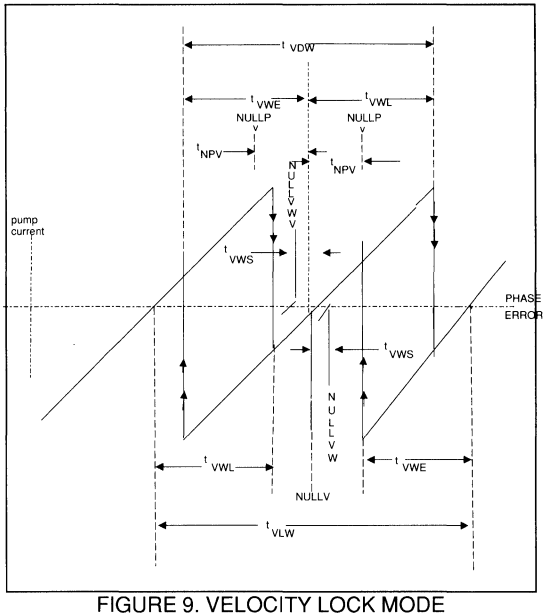


FIGURE 9. VELOCITY LOCK MODE

Velocity Lock Mode (MFM)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{VLW}	Velocity Lock Window		4W		nsec	*
t_{VDW}	Vlock Detect Window		4W		nsec	RAWDATA or XTALIN
t_{VWE}	Vlock Early Window		2W		nsec	RAWDATA or XTALIN
t_{VWL}	Vlock Late Window		2W		nsec	RAWDATA or XTALIN

* Because of the periodic nature of t_{VLW}, this must equal 4W, where W is the inverse of the VCOIN frequency. t_{VLW}, in addition to checking for obscure defects on the device, checks the device tester's accuracy.

Velocity Lock Mode (RLL)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{VLW}	Velocity Lock Window		6W		nsec	*
t_{VDW}	Vlock Detect Window		6W		nsec	RAWDATA or XTALIN
t_{VWE}	Vlock Early Window		3W		nsec	RAWDATA or XTALIN
t_{VWL}	Vlock Late Window		3W		nsec	RAWDATA or XTALIN

* Because of the periodic nature of t_{VLW}, this must equal 6W, where W is the inverse of the VCOIN frequency. t_{VLW}, in addition to checking for obscure defects on the device, checks the device tester's accuracy.

Write Precompensation

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{WCS}	Setup time of either edge of EARLY, LATE, or WDATA to any edge of WCLK	15			nsec	
t_{WCH}	Hold time of either edge of EARLY, LATE, or WDATA from any edge of WCLK	5			nsec	
t_{PCE}	Early precomp	W/8-1.5	W/8	W/8+1.5	nsec	Precomp.WPCDATA minus non-precompensatedWPCDATA
t_{PCL}	Late precomp	W/8-1.5	W/8	W/8+1.5	nsec	Precomp.WPCDATA minus non-precompensatedWPCDATA
t_{PCP}	WPCDATA pulse width	W-20	W-10	W	nsec	Early and late precompensation cases

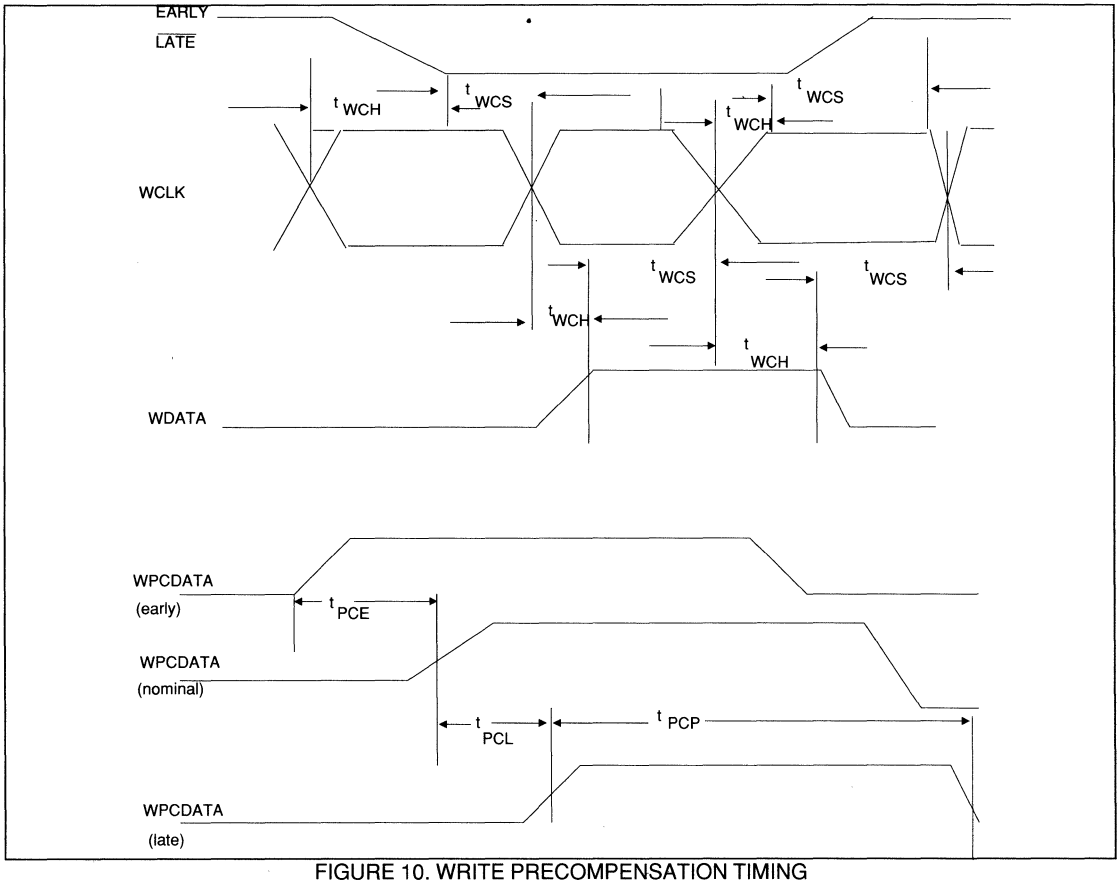


FIGURE 10. WRITE PRECOMPENSATION TIMING

TTL XTALIN Input Clock

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{XCP}	TTL XTALIN Clock Pulse Width	20			nsec	
t_{XP}	XTALIN max freq	23.5			MHz	47/53% Duty Cycle

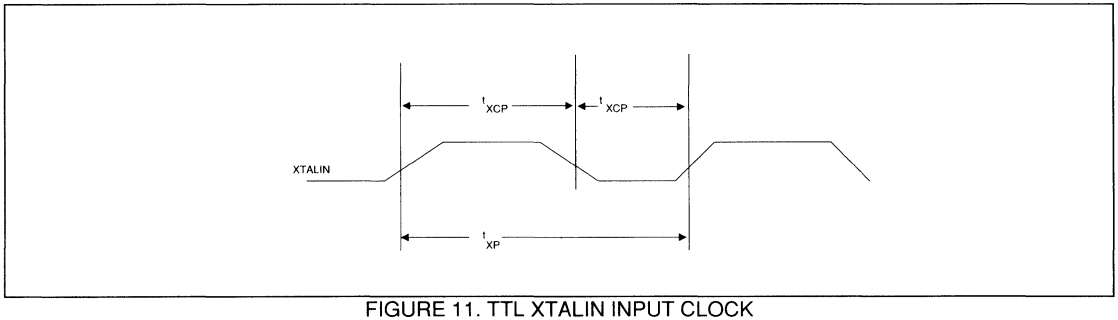


FIGURE 11. TTL XTALIN INPUT CLOCK

Power On Reset

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{CUP}	V_{CC} to Controller Up		100		µsec	V_{CC} rise time 200nsec, 10% to 90%

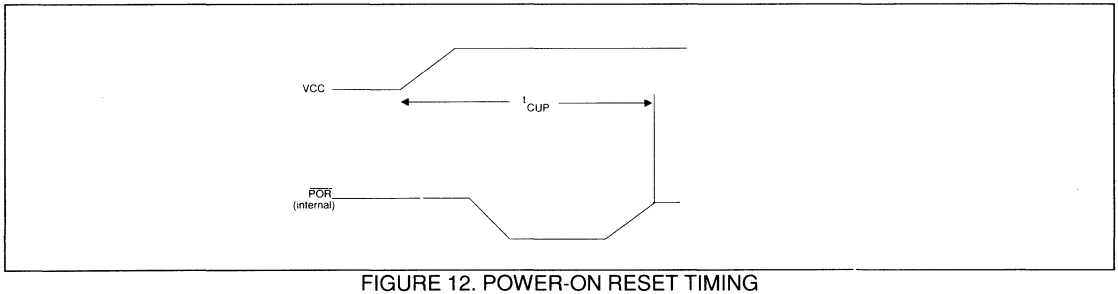


FIGURE 12. POWER-ON RESET TIMING

Delay Line

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DRC}	Delay-Locked Loop Time Constant		3		msec	

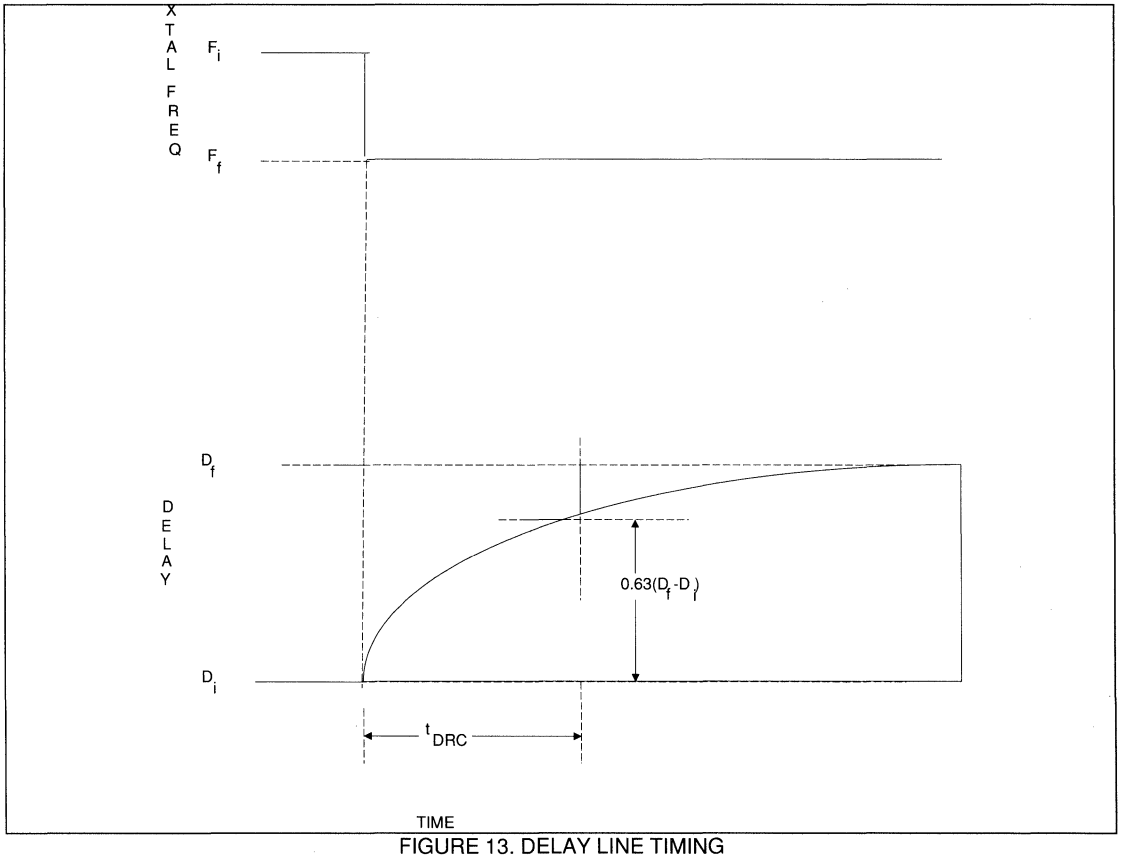
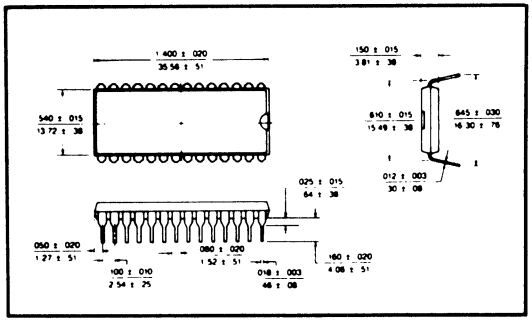
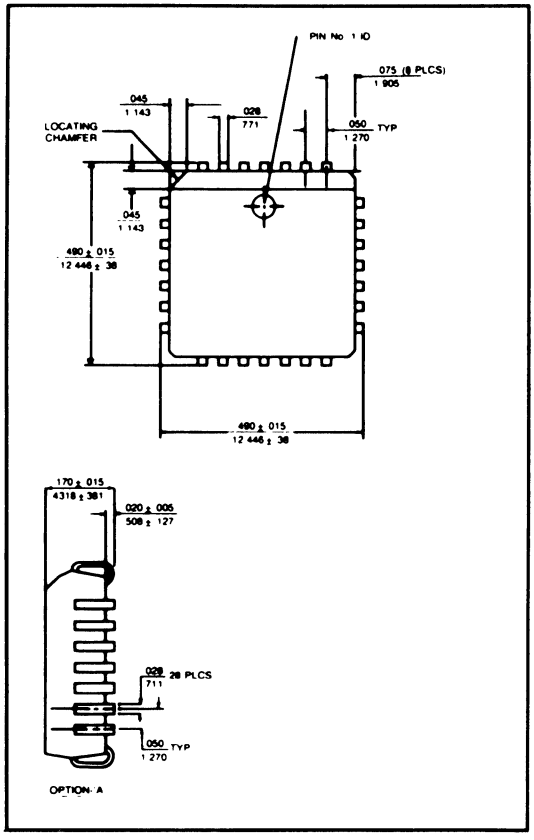


FIGURE 13. DELAY LINE TIMING

PACKAGE DIAGRAMS



28 LEAD PLASTIC PH



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