WD90C30

High Performance

Video Controller

WESTERN DIGITAL

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ADDITIONAL REFERENCES

IBM Personal Computer Hardware User Guide (IBM # 6322510)
IBM Personal Computer XT Hardware User Guide (IBM # 6322511)
IBM Personal Computer AT Hardware User Guide (IBM # 6280066)
IBM Personal System 2 Model 30 Hardware User Guide (IBM # 68x2230)
IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)
IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 68x2201)
IBM PC Options and Adapters Technical Reference Manual (IBM # 6322509)
IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)
Personal Computer Reference Manual (IBM # 6025005)

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1.0 INTRODUCTION

The Western Digital Imaging WD90C30 is a 0.9 micron CMOS VLSI device that allows the design of a VGA graphics subsystem to interface with the PC/XT/AT bus, as well as the IBM Micro Channel bus, while maintaining backwards compatibility with previous video standards such as MDA, EGA, CGA, Hercules and AT&T 6300. A major advantage of the WD90C30 is that designs implementing this graphics controller will be able to run applications requiring VGA hardware and BIOS compatibility, and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode. The WD90C30 supports high resolution graphics with 1024 by 768 dot resolution and 256 colors. The WD90C30 also supports 132-column text mode and 6-16 pixel fonts.

This data book supplies a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package information, and associated references.

1.1 FEATURES

- Provides single chip video graphics solution for IBM PC, XT, AT, and PS/2 compatible systems.
- Supports two, four or eight 64 Kbyte by 16 DRAMs; four or eight 256 Kbyte by 4 DRAMs; and one or two 256 Kbyte by 16 DRAMs.
- Pin compatible with the WD90C31.
- 100% hardware compatible with IBM's VGA and EGA with hidden register support.
- 100% CGA, MDA, Hercules Graphics, and AT&T Model 6300 compatible.
- Supports all IBM VGA modes with two 64K by 16 DRAMs or only one 256K by 16 DRAM.
- With more DRAMS installed it can support 256 colors at the following resolutions: 640 by 400, 640 by 480, 800 by 600, and 1024 by 768.
- Supports 132-column text.
- Write buffer for zero wait state CPU write performance.
- 8-bit or 16-bit data bus for I/O and memory. True 16-bit CPU to video memory transfer for all modes.
- Provides 16-bit or 32-bit memory interface with fast page operations.
- Up to 80 MHz maximum video clock rate.
- Up to 50 MHz maximum memory clock rate.
- Up to four simultaneous displayable fonts.
- 6-16 pixel-wide fonts.
- A maximum of 16 fonts can be loaded.
- Provides adapter video BIOS ROM decoding.
- Eleven-bit vertical counter to support scan resolution of up to 2048 scan lines.
- Special double scanning and underline.
- Special display enable or blanking output signal.
- Special border disable.
- Lockable palette, RAMDAC, and overscan registers.
- Special CRTC shadow registers for support of non-standard monitors.
- Special register locking for flat panel applications.
- Supports 16-bit I/O register transfer to index/data register pairs.
- Adjustable internal FIFO and fast page memory interface.
- 132-pin JEDEC (Joint Electronic Device Engineering Council) PQFP (Plastic Quad Flat Package).
- 144-pin EIAJ (Electrical Industry Association of Japan) PQPF.
- Integrated Feature connector interface and external RAMDAC support.
- Integrated bus interface for PC/XT/AT, and Micro Channel with minimum external component support.
- Programmable memory mapping register to map WD90C30 into any CPU memory address space.
- Eight-bit CPU address offset register to support 1 Mbyte memory segmentation.

2.0 WD90C30 ARCHITECTURE

The WD90C30 contains four major internal modules, the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The WD90C30 also has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface, and the Clock interface.

An internal four-level write buffer is used to achieve fast memory write. A zero wait state may be achieved with a 32-bit video memory interface for most memory write operations.

An internal FIFO is used to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles.

The CRT Controller module maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The CRT Controller module also generates horizontal sync (HSYNC), vertical sync (VSYNC), and blanking signal for the display monitor.

The Sequencer functions as a timing generator for the display memory cycles. It provides the character clock in the alphanumeric mode, and the dot clock in the graphics mode. The sequencer arbitrates between video display refresh, memory refresh and CPU access of the video memory. The sequencer also provides write buffer control.

The Graphics Controller manipulates the data flow between the CPU and the video memory for both CPU write and CPU read cycles.

The Attribute Controller serializes the video memory data into video data stream, according to different display formats. It controls blinking, underlining, cursor, pixel panning, reverse video, and background or foreground color in all display modes.

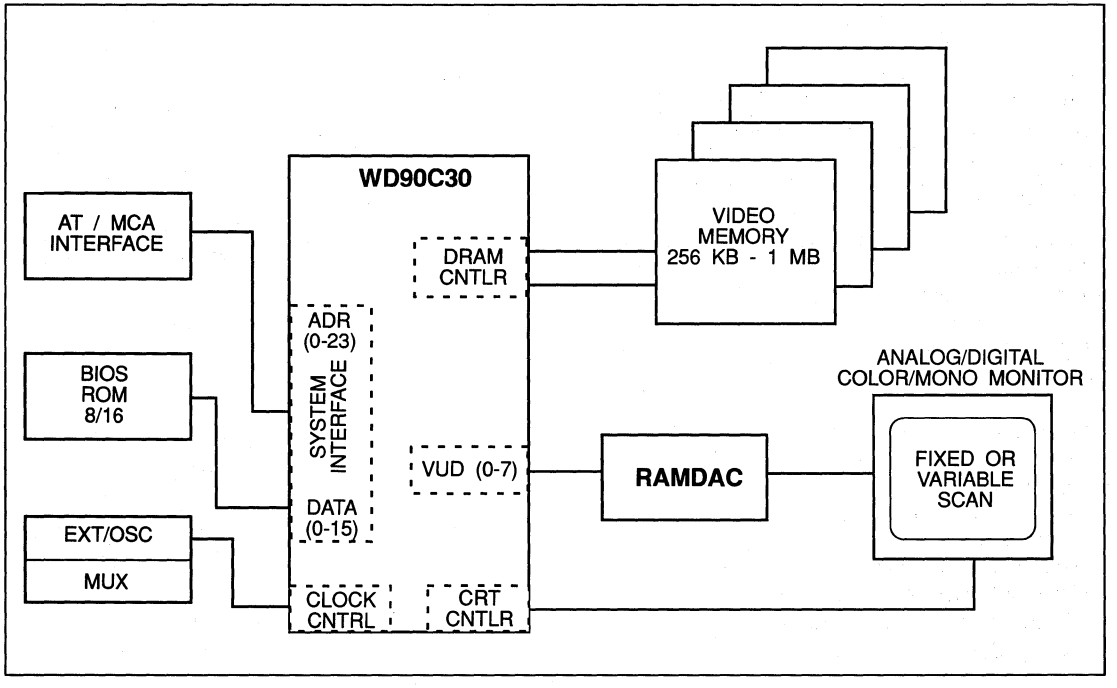

FIGURE 1. SYSTEM BLOCK DIAGRAM

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3.0 WD90C30 INTERFACES

3.1 CPU AND BIOS ROM INTERFACE

The WD90C30 is designed to operate in both the PC/XT/AT Bus and the PS/2 Micro Channel Bus architecture configurations. The selection of the mode depends on the setting of a configuration register bit CNF(2), which is determined upon power-up/reset, and is described in the WD90C30 Configuration Bits section of this data book.

Whether configured for either AT or Micro Channel operation, the WD90C30 operates functionally in a manner conducive to PC/XT/AT or Micro Channel interfacing. The signal pins, memory maps, and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C30 provides all the signals, and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus, in 8-bit or 16-bit data path modes. WD90C30 also provides the necessary decoding of the adapter video BIOS ROM. Using the provided signals, the customer can implement designs which operate in 8-bit or 16-bit mode and control an 8-bit or 16-bit BIOS ROM.

The I/O data path can be programmed to be either 16-bit or 8-bit. The CPU to display buffer data path can also be eight or sixteen bits wide for all modes. $\overline{\text{ROM16}}$, $\overline{\text{IOCS16}}$, and $\overline{\text{MEMCS16}}$ signals are generated by the WD90C30.

The WD90C30 has a display memory write buffer which holds the CPU write data until it can be transferred to the display memory, allowing the CPU to continue. This feature greatly reduces CPU wait states while writing to the video memory.

The WD90C30 provides the necessary wait states for CPU accesses to the video memory, if necessary. Wait states for I/O accesses and BIOS ROM accesses are not generated.

Special I/O ports such as 46E8H for the AT (or 03C3H for Micro Channel) for setup, and 102H for VGA enable, have been implemented internally in the WD90C30.

3.2 DRAM INTERFACE

The WD90C30 has a very flexible DRAM interface. It can work with two, four, or eight 64Kbyte by 16 DRAMs with a 32-bit memory interface. It can also work with four 256 Kbyte by 4 DRAMs and one 256 Kbyte by 16 DRAM with a 16-bit memory interface. Other possible configurations are eight 256 Kbyte by 4 DRAMS or two 256Kbyte by 16 DRAMS with a 32-bit memory interface. In all cases the WD90C30 uses the DRAM fast page mode to optimize performance.

The WD90C30 can support all standard IBM VGA modes with only two 64K by 16 DRAMs. Because it uses a 32-bit memory interface and has internal write buffer, the WD90C30 can update the video memory without inserting wait states to the AT bus for most standard IBM VGA modes.

When additional DRAMs are installed, the WD90C30 is capable of supporting high resolution video modes (1024 by 768 with 256 colors, non-interlaced at 72 Hz vertical refresh rate).

The WD90C30 is designed to support DRAM (60 ns, 70 ns, 80 ns, and 100 ns) with the dedicated MCLOCK which can operate from 32 MHz to 50 MHz maximum.

The WD90C30 generates fast page DRAM timing for all the CPU accesses, graphics display and text display (a choice of page mode and non-page mode operation is provided to access fonts in text modes).

The WD90C30 also generates CAS before RAS DRAM refresh for the display memory.

3.3 VIDEO INTERFACE

The WD90C30 is optimized to connect to an analog CRT monitor through a RAMDAC, but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the WD90C30 provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and

depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C30 can be programmed to directly generate all the CRT signals for up to eight bits/pixel (256 color) displays.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected directly to the WD90C30. The WD90C30 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.4 CLOCK INTERFACE

The WD90C30 has four clock input signal pins; the separate memory clock, MCLK, which drives the DRAM and bus interface timing; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. VCLK1 and VCLK2 can also be programmed as outputs to provide the option to externally control a multiplexer that supplies the video clock. The MCLK can also be selected as a memory clock or video dot clock.

3.5 WD90C30 POWER-UP CONFIGURATION

The WD90C30 uses the memory data pins to configure an internal configuration register upon power-up-reset. CNF(2) determines whether the WD90C30 will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by the WD90C30 at power-up-reset are used as status bits or for clock source control. For more information on WD90C30 power-up configuration, refer to Section 7.10, Configuration Bits.

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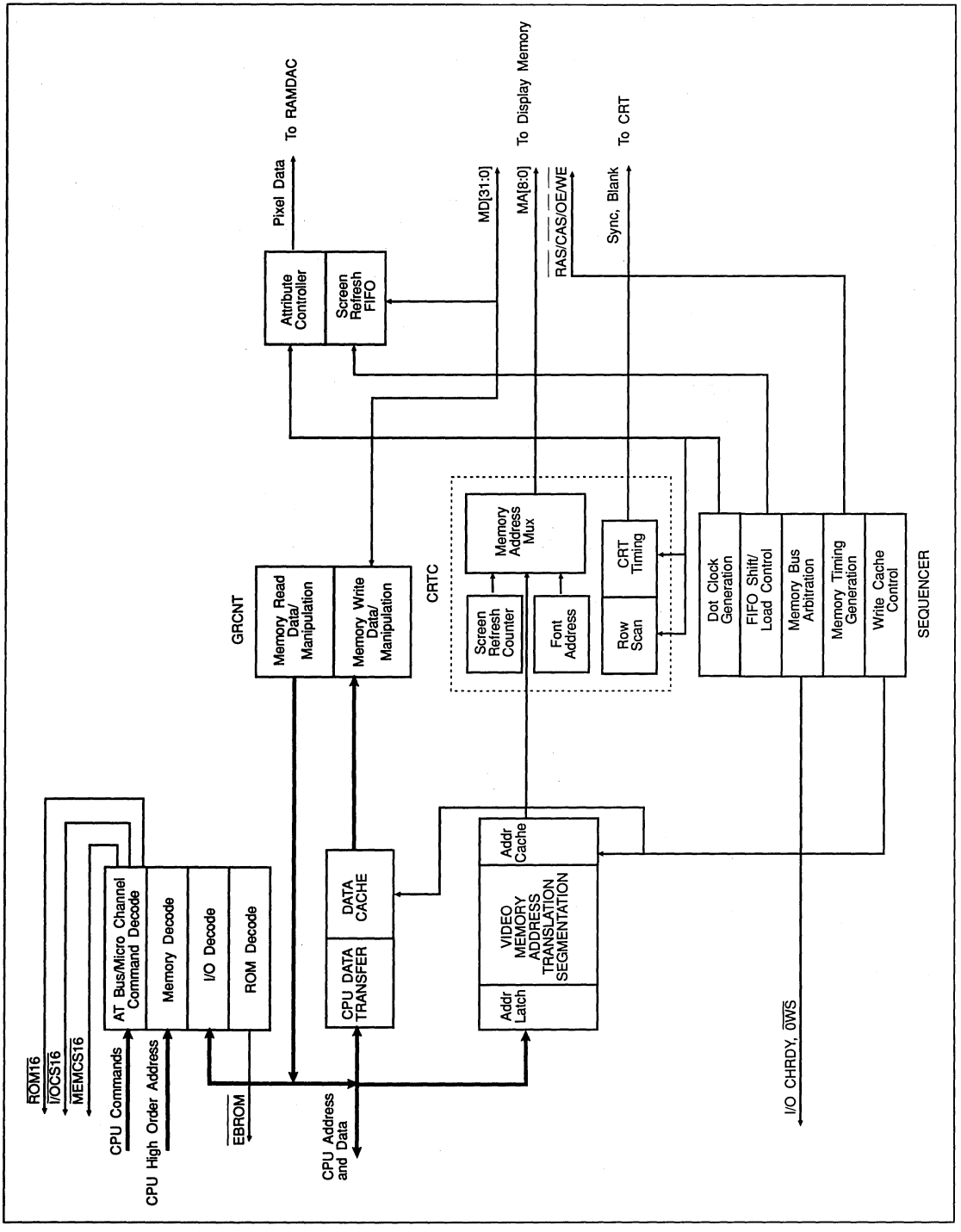

FIGURE 2. WD90C30 BLOCK DIAGRAM

4.0 SIGNAL DESCRIPTION

Table 1 provides a list of pin assignments for the 132-pin JEDEC package. Table 2 provides a list of pin assignments for the 144-pin EIAJ package. Table 3 provides a description of the signals controlled by the WD90C30, and both the JEDEC and EIAJ pins are identified. The WD90C30 mnemonics are used.

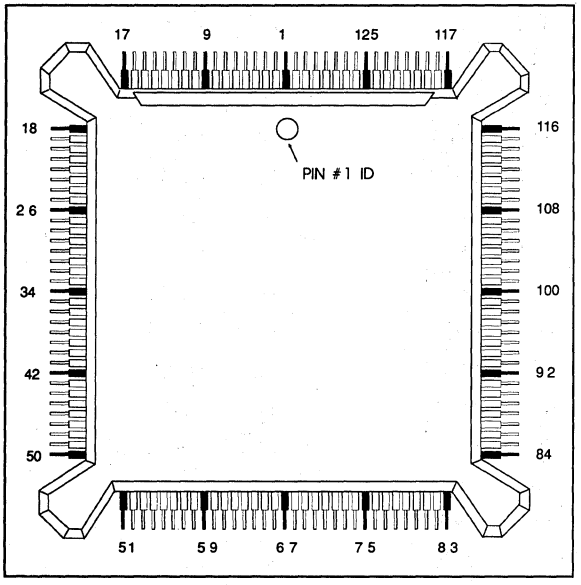

FIGURE 3. 132-PIN JEDEC PACKAGE

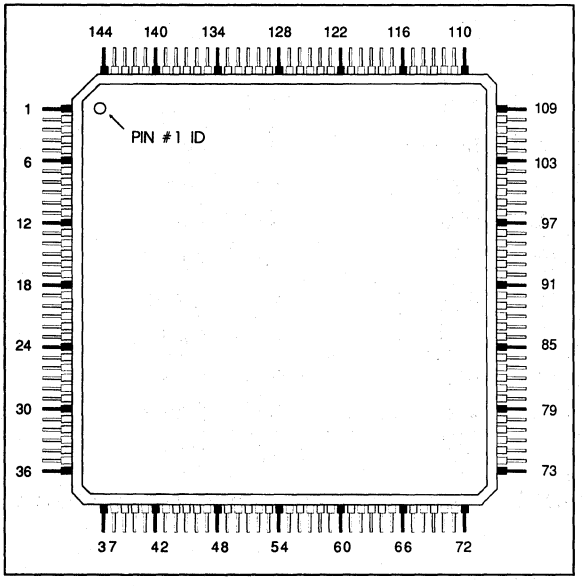

FIGURE 4. 144-PIN EIAJ PACKAGE

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PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	MDET	34	MD12	67	VSS	100	DIR
2	USR1	35	MD11	68	A22	101	DA7
3	USR0	36	MD10	69	A23	102	DA6
4	MCLK	37	MD9	70	$\overline{\text{IOCS16}}$	103	DA5
5	VSS	38	MD8	71	$\overline{\text{MEMCS16}}$	104	DA4
6	$\overline{\text{OE}}$	39	$\overline{\text{RAS}}$	72	$\overline{\text{BHE}}$	105	DA3
7	$\overline{\text{WE3}}$	40	VSS	73	ALE	106	DA2
8	MD31	41	$\overline{\text{CAS}}$	74	IRQ	107	DA1
9	MD30	42	MD7	75	EMEM	108	DA0
10	MD29	43	MD6	76	$\overline{\text{IOR}}$	109	$\overline{\text{EDBUFL}}$
11	MD28	44	MD5	77	$\overline{\text{IOW}}$	110	VSYNC
12	MD27	45	MD4	78	$\overline{\text{MRD}}$	111	HSYNC
13	MD26	46	MD3	79	$\overline{\text{MWR}}$	112	$\overline{\text{BLANK}}$
14	MD25	47	MD2	80	RESET	113	$\overline{\text{HTL}}$
15	MD24	48	MD1	81	$\overline{\text{0WS}}$	114	$\overline{\text{WPLT}}$
16	$\overline{\text{WE2}}$	49	MD0	82	IOCHRDY	115	$\overline{\text{RPLT}}$
17	VSS	50	VCC	83	VSS	116	VCC
18	VCC	51	VSS	84	VCC	117	VSS
19	MD23	52	$\overline{\text{WE0}}$	85	$\overline{\text{EIO}}$	118	PCLK
20	MD22	53	MA0	86	$\overline{\text{ROM16}}$	119	VID0
21	MD21	54	MA1	87	$\overline{\text{EBROM}}$	120	VID1
22	MD20	55	MA2	88	$\overline{\text{EDBUFH}}$	121	VID2
23	MD19	56	MA3	89	A16	122	VID3
24	MD18	57	MA4	90	DA15	123	VID4
25	MD17	58	MA5	91	DA14	124	VID5
26	MD16	59	MA6	92	DA13	125	VID6
27	$\overline{\text{RAS4}}$	60	MA7	93	DA12	126	VID7
28	$\overline{\text{RAS3}}$	61	MA8	94	DA11	127	VSS
29	VSS	62	A17	95	DA10	128	VCLK0
30	$\overline{\text{WE1}}$	63	A18	96	DA9	129	VCLK1
31	MD15	64	A19	97	DA8	130	VCLK2
32	MD14	65	A20	98	$\overline{\text{EABUF}}$	131	$\overline{\text{EXPCLK}}$
33	MD13	66	A21	99	VSS	132	$\overline{\text{EXVID}}$

TABLE 1. WD90C30 132-PIN JEDEC ASSIGNMENTS

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	N.C.	37	N.C.	73	N.C.	109	N.C.
2	VCC	38	VSS	74	VCC	110	VSS
3	MD23	39	$\overline{WE0}$	75	$\overline{EIO}$	111	PCLK
4	MD22	40	MA0	76	$\overline{ROM16}$	112	VID0
5	MD21	41	MA1	77	$\overline{EBROM}$	113	VID1
6	MD20	42	MA2	78	$\overline{EDBUFH}$	114	VID2
7	MD19	43	MA3	79	A16	115	VID3
8	MD18	44	MA4	80	DA15	116	VID4
9	MD17	45	MA5	81	DA14	117	VID5
10	MD16	46	MA6	82	DA13	118	VID6
11	$\overline{RAS4}$	47	MA7	83	DA12	119	VID7
12	$\overline{RAS3}$	48	MA8	84	DA11	120	VSS
13	VSS	49	A17	85	DA10	121	VCLK0
14	$\overline{WE1}$	50	A18	86	DA9	122	VCLK1
15	MD15	51	A19	87	DA8	123	VCLK2
16	MD14	52	A20	88	$\overline{EABUF}$	124	$\overline{EXPCLK}$
17	MD13	53	A21	89	VSS	125	$\overline{EXVID}$
18	N.C.	54	N.C.	90	N.C.	126	N.C.
19	MD12	55	VSS	91	DIR	127	MDET
20	MD11	56	A22	92	DA7	128	USR1
21	MD10	57	A23	93	DA6	129	USR0
22	MD9	58	$\overline{IOCS16}$	94	DA5	130	MCLK
23	MD8	59	$\overline{MEMCS16}$	95	DA4	131	VSS
24	RAS	60	$\overline{BHE}$	96	DA3	132	$\overline{OE}$
25	VSS	61	ALE	97	DA2	133	$\overline{WE3}$
26	$\overline{CAS}$	62	IRQ	98	DA1	134	MD31
27	MD7	63	EMEM	99	DA0	135	MD30
28	MD6	64	$\overline{IOR}$	100	$\overline{EDBUFL}$	136	MD29
29	MD5	65	$\overline{IOW}$	101	VSYNC	137	MD28
30	MD4	66	$\overline{MRD}$	102	HSYNC	138	MD27
31	MD3	67	$\overline{MWR}$	103	$\overline{BLANK}$	139	MD26
32	MD2	68	RESET	104	$\overline{HTL}$	140	MD25
33	MD1	69	$\overline{OWS}$	105	$\overline{WPLT}$	141	MD24
34	MD0	70	IOCHRDY	106	$\overline{RPLT}$	142	$\overline{WE2}$
35	VCC	71	VSS	107	VCC	143	VSS
36	N.C.	72	N.C.	108	N.C.	144	N.C.

TABLE 2. WD90C30 144-PIN EIAJ ASSIGNMENTS

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
			POWER ON
80 - 68	RESET	I	**RESET:** This signal input resets the WD90C30. MCLK and VCLK0 should be connected to WD90C30 in order for the WD90C30 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the MD15-0 bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
			CLOCK SELECTION
4 - 130	MCLK	I	**MEMORY CLOCK:** This clock signal determines the VGA DRAM timing as well as system interface control timing. MCLK should be a minimum 37.5 MHz for 80 ns DRAMS.
128 - 121	VCLK0	I	**VIDEO CLOCK 0:** This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK is 25.175 MHz to display 640 pixels per horizontal display line. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
129 - 122	VCLK1	I/O	**VIDEO CLOCK 1:** This pin can be a second video display clock input or an output to external clock selection module. Pin direction is determined on Reset by a pull-up/down resistor on Pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H (or it reflects the contents of 03C2, Miscellaneous Register, Bit 2). Refer to the Configuration Register and PR15 Register, Bit 5 description.
130 - 123	VCLK2	I/O	**VIDEO CLOCK 2:** A third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. Acts as a user-defined external clock input, or an output reflecting the content of Bit PR2(1) (or it reflects the contents of 03C2H, Miscellaneous Register, Bit 3) if CNF(3) is set to "1". See the Configuration Register and PR15 Register, Bit 5 description.

TABLE 3. SIGNAL DESCRIPTION

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
HOST INTERFACE			
69 - 57 68 - 56 66 - 53 65 - 52 64 - 51 63 - 50 62 - 49	A23 A22 A21 A20 A19 A18 A17	I I I I I I I	**ADDRESS BUS (A23 - A17):** These address bits should be connected to address bus SA23 - 17 in Micro Channel mode. In AT mode A23-17 should be connected to A23-17 of the AT address bus.
89 - 79	A16	I	**ADDRESS BUS (A16):** Bit SA16 of CPU address bus
73 - 61	ALE	I	**ADDRESS LATCH ENABLE:** In AT mode, A23-17 are latched internally at the falling edge of the ALE. In Micro Channel mode, ALE should not be used and should be connected to VSS.
90 - 80 91 - 81 92 - 82 93 - 83 94 - 84 95 - 85 96 - 86 97 - 87 101 - 92 102 - 93 103 - 94 104 - 95 105 - 96 106 - 97 107 - 98 108 - 99	DA15 DA14 DA13 DA12 DA11 DA10 DA9 DA8 DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	**ADDRESS /DATA BUS:** This is the multiplexed CPU address and data bus. $\overline{EABUF}$ = 0: Enables the external address buffer. $\overline{EDBUFL}$ = 0 or $\overline{EDBUFH}$ = 0: Enables the external bi-directional data buffers. DIR controls the data flow for the data buffer.
82 - 70	IOCHRDY	O	**READY**: This active high output signal indicates to the system processor that a memory access is completed. It is used to add wait states to the CPU bus cycles during video memory accesses. It may be pulled inactive by the WD90C30 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.

TABLE 3. SIGNAL DESCRIPTION (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
74 - 62	IRQ/(IRQ)	O	**INTERRUPT REQUEST:** Programmable processor interrupt request. It is enabled via Bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of Vertical Display occurs, this signal will be active, causing the interrupt. It will stay active until CRTC11 Bit 4 clears it. In an AT system IRQ is usually not connected, but may be connected if desired. IRQ is used to generate interrupt, usually in the Micro Channel mode.
71 - 59	MEMCS16/ (CDDS16)	O	**MEMORY CHIP SELECT 16 BITS:** In AT mode, this line is used to respond the host to enable 16-bit video memory data transfer. In Micro Channel mode, this line is used to indicate 16-bit video memory or I/O access.
85 - 75	EIO (3C3D0)	I	**ENABLE I/O:** In AT mode, this active low signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, this line comes from I/O port 3C3H Bit 0 to enable video subsystem memory and I/O address decoding. ("1" = enable)
87 - 77	EBROM	O	**ENABLE BIOS ROM:** This is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). A write to WD90C30 internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
113 - 104	HTL	O	**ENABLE HIGH-TO-LOW:** (for 16-bit BIOS) If only an eight-bit CPU interface is used, this output enables a data buffer to allow reading of the upper byte of ROM data on the lower data bus when two ROMs (16-bit) are supported.
75 - 63	EMEM	I	**ENABLE MEMORY:** This signal enables memory decoding when high. It is normally connected to the Refresh signal.
72 - 60	BHE	I	**BYTE HIGH ENABLE:** BHE should be connected to BHE of the AT or Micro Channel bus. BHE, SA0 = 00 - Word transfer = 01 - High byte transfer = 10 - Low byte transfer = 11 - Illegal

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

NOTE:
( ) Micro Channel only.

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
81 - 69	$\overline{0WS}$	O	**ZERO WAIT STATE:** This active low signal can be used to generate zero wait states to the AT bus. This signal can be programmed by the PR33 register, bits 7 and 6 in the following ways: $\overline{0WS}$ = 0 if write cache is not full. $\overline{0WS}$ = 0 if valid memory address decode AND write cache is not full. In this case $\overline{0WS}$ = 0 should be ANDed externally with $\overline{MWR}$ to generate zero wait state strobe. $\overline{0WS}$ = 0 if valid memory address decode AND write cache is not full AND $\overline{MWR}$ is active. $\overline{0WS}$ = 0 if valid memory address decode AND write cache is not full and $\overline{MWR}$ is active; OR if valid I/O address decode and $\overline{IOW}$ is active.
78 - 66	$\overline{MRD}$/(M/$\overline{IO}$)	I	**MEMORY READ:** In AT mode, this signal is called $\overline{MRD}$ and is an active low memory read strobe. In Micro Channel mode, the signal is called M/$\overline{IO}$. It distinguishes between memory and I/O cycles. When (M/$\overline{IO}$) is high, a memory cycle is in process. A low on (M/$\overline{IO}$) shows that an I/O cycle is in process.
79 - 67	$\overline{MWR}$/($\overline{S0}$)	I	**MEMORY WRITE:** The Active low memory write strobe in AT mode. In Micro Channel mode, it becomes $\overline{S0}$ and is the channel status signal which indicates the start and type of a channel cycle. Along with $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ signals, it is decoded to interpret I/O and memory commands.
76 - 64	$\overline{IOR}$/($\overline{S1}$)	I	**I/O READ:** Active low I/O read strobe in AT mode. In Micro Channel mode, it becomes $\overline{S1}$ and is the channel status signal which indicates the start and type of a channel cycle.
77 - 65	$\overline{IOW}$/($\overline{CMD}$)	I	**I/O WRITE:** Active low strobe. In AT mode, the strobe signals an I/O write. In Micro Channel mode it is the bus data strobe $\overline{CMD}$. Address bus validity is signaled by $\overline{CMD}$ going low while the rising edge of $\overline{CMD}$ indicates the end of a Micro Channel bus cycle.
70 - 58	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	I/O	**I/O CHIP SELECT 16 BITS:** In AT mode, this signal is used to respond to the host to allow 16-bit I/O access. In Micro Channel mode, this signal is driven by the host to individually select channel connector slots during system configuration.

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

NOTE:
( ) Micro Channel only.

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
100 - 91	DIR	O	**DIRECTION CONTROL:** Active high Direction Control for external bus buffers in AT and MCA implementation. The default state is low until a read cycle occurs. The WD90C30 will then drive DIR high to change the direction of the data buffers.
88 - 78	$\overline{\text{EDBUFH}}$	O	**ENABLE DATA BUFFER HIGH:** Active low signal that allows control of an external data buffer for data bits D8 through D15.
109 - 100	$\overline{\text{EDBUFL}}$	O	**ENABLE DATA BUFFER LOW:** Active low signal that allows control of an external data buffer for data bits D0 through D7.
98 - 88	$\overline{\text{EABUF}}$	O	**ENABLE ADDRESS BUFFER:** Active low signal that allows control of an external address buffer.
86 - 76	$\overline{\text{ROM16}}$/($\overline{\text{CSFB}}$)/ $\overline{\text{EXBLANK}}$	I/O	**BIOS ROM SELECT 16 BITS:** (AT Mode) Active low output. This signal decodes the ROM address LA(23-17) for space 0C0000 - 0DFFFF. It may be combined with SA15 and SA16 externally to control $\overline{\text{MCS16}}$ for the address space C0000 - C7FFF. If CNF(17) is set to 0 at power up reset, the ROM16 address decoding is disabled. ROM16 then reflects the status of PR1_1 bit. **CARD SELECT FEEDBACK:** (Micro Channel mode) Active low output. This signal is used as Card Selected Feedback to provide positive acknowledgement of its presence at the host's addresses specified. **EXTERNAL BLANK:** (AT or Micro Channel Mode) If CNF (18) is set to zero (MD18 = 0 at power-up reset), this signal becomes an active low input. $\overline{\text{EXBLANK}}$ = 1: enables BLANK, VSYNC, and HSYNC output. $\overline{\text{EXBLANK}}$ = 0: tri-state BLANK, VSYNC, and HSYNC output.

TABLE 3. SIGNAL DESCRIPTION (Continued)

NOTE:
( ) Micro Channel only.

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
DISPLAY MEMORY INTERFACE			
41 - 26	$\overline{CAS}$	O	**COLUMN ADDRESS STROBE:** Active low CAS output signal (for both two, four and eight DRAM configurations).
39 - 24	$\overline{RAS}$	O	**ROW ADDRESS STROBE:** This active low RAS output signal is the strobe for the 256 Kbyte by 4 or 256 Kbyte by 16 DRAM interface. If 64 Kbyte by 16 DRAMS are used, then this signal is the RAS strobe for the first 256 Kbyte memory bank.
28 - 12	$\overline{RAS3}$	O	**ROW ADDRESS STROBE:** This active low RAS strobe is used only if eight 64 Kbyte by 16 DRAMs are used. It controls the third 256 Kbyte memory bank.
27 - 11	$\overline{RAS4}$	O	**ROW ADDRESS STROBE:** This active low RAS strobe is used only if eight 64 Kbyte by 16 DRAMs are used. It controls the fourth 256 Kbyte memory bank.
6 - 132	$\overline{OE}$	O	**OUTPUT ENABLE:** Active low DRAM output enable signal (for both two, four and eight DRAM configurations).
52 - 39	$\overline{WE0}$	O	**WRITE ENABLE:** Active low write enable signal for MD7 through 0.
30 - 14	$\overline{WE1}$	O	**WRITE ENABLE:** Active low write enable signal for MD15 through 8.
16 - 142	$\overline{WE2}$	O	**WRITE ENABLE:** Active low write enable signal for MD23 through 16.
7 - 133	$\overline{WE3}$	O	**WRITE ENABLE:** Active low write enable signal for MD31 through 24.
PROGRAMMABLE OUTPUTS			
3 - 129	USR0	O	May be used to control special card or system features (see PR32 register).
2 - 128	USR1	O	May be used to control special card or system features (see PR32 register).

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
VIDEO MEMORY DATA			
31 - 15	MD15	I/O	**DISPLAY MEMORY DATA (MD15 through 0):**
32 - 16	MD14	I/O	These lines are the data bus to the video display
33 - 17	MD13	I/O	DRAMS. The MD0-18 data lines are pulled up by in-
34 - 19	MD12	I/O	ternal 50K ohm resistors or may be pulled down by
35 - 20	MD11	I/O	external 4.7 Kohm resistors to provide setup informa-
36 - 21	MD10	I/O	tion on power-up (reset) as follows:
37 - 22	MD9	I/O	
38 - 23	MD8	I/O	**MD POWER-UP FUNCTION REGISTER (BIT)**
42 - 27	MD7	I/O	18 Enable $\overline{\text{ROM16}}$ as $\overline{\text{EXBLANK}}$ CNF(18)+
43 - 28	MD6	I/O	16 64K by 16 or 256K by 4 DRAM Select CNF(16)+
44 - 29	MD5	I/O	15 EGA SW4/General Purpose PR11 (7) +
45 - 30	MD4	I/O	14 EGA SW3/General Purpose PR11 (6)+
46 - 31	MD3	I/O	13 EGA SW2/General Purpose PR11 (5) +
47 - 32	MD2	I/O	12 EGA SW1/General Purpose PR11 (4) +
48 - 33	MD1	I/O	11 ANALOG/TTL Display CNF(8) *
49 - 34	MD0	I/O	10 Set 16-bit ROM [CNF(10)]*
8 - 134	MD31	I/O	9 3C3H or 46E8H I/O port for wake up [CNF(9)] +
9 - 135	MD30	I/O	8 A23-A20 connection [CNF(11)]+
10 - 136	MD29	I/O	7 General Purpose CNF(7) *
11 - 137	MD28	I/O	6 General Purpose CNF(6) *
12 - 138	MD27	I/O	5 General Purpose CNF(5) *
13 - 139	MD26	I/O	4 General Purpose CNF(4) *
14 - 140	MD25	I/O	3 VCLK1,2 I/O CNF(3) +
15 - 141	MD24	I/O	2 AT/Micro Channel Mode CNF(2)+
19 - 3	MD23	I/O	1 1 or 2 ROMs CNF(1) *
20 - 4	MD22	I/O	0 BIOS ROM Mapping PR1(0) *
21 - 5	MD21	I/O	NOTES:
22 - 6	MD20	I/O	"*" Pulldown resistor sets these bits to logic 1.
23 - 7	MD19	I/O	"+" Pulldown resistor sets these bits to logic 0.
24 - 8	MD18	I/O	For more details refer to PR and Configuration
25 - 9	MD17	I/O	Registers.
26 - 10	MD16	I/O	

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
VIDEO MEMORY ADDRESS			
61 - 48 60 - 47 59 - 46 58 - 45 57 - 44 56 - 43 55 - 42 54 - 41 53 - 40	MA8/$\overline{RAS2}$ MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0	O O O O O O O O O	**MEMORY ADDRESS (MA0 through MA8):** Display memory DRAM address. For testing purposes, these pins can be tri-stated by setting Register PR4(4)=1. MA8/$\overline{RAS2}$ is an active low RAS strobe for the second 256 Kbyte memory bank if four 64K by 16 DRAMs are used.
RAMDAC INTERFACE			
126 - 119 125 - 118 124 - 117 123 - 116 122 - 115 121 - 114 120 - 113 119 - 112	VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0	O O O O O O O O	**VIDEO (VD0-VD7):** Pixel video data output to DAC and to Feature Connector. These lines can drive up to a 8 mA load.
115 - 106	$\overline{RPLT}$	O	**READ PALETTE:** Video DAC register and color palette read signal for an external RAMDAC. Active low during an I/O read of addresses 3C6H, 3C8H, and 3C9H.
114 - 105	$\overline{WPLT}$	O	**WRITE PALETTE:** Video DAC register and color palette write signal for an external RAMDAC. Active low during an I/O write to addresses 3C6H through 3C9H.
118 - 111	PCLK	O	**PIXEL CLOCK:** Video pixel clock output used by the DAC to latch video signals VID0 through 7. Its source is one of the video clock inputs: VCLK0, VCLK1 or VCLK2 as determined by the Miscellaneous Output Register.
CRT CONTROL			
112 - 103	$\overline{BLANK}$	O	**BLANK:** Active low display monitor blank pulse to external RAMDAC.
111 - 102	HSYNC	O	**HORIZONTAL SYNC:** Display monitor horizontal synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.
110 - 101	VSYNC	O	**VERTICAL SYNC:** Display monitor vertical synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
1 - 127	MDET	I	**MONITOR DETECT:** This pin is used when the RAM-DAC is external. It is used to determine the monitor type and can be read at port 3C2H Bit 4.
FEATURE CONNECTOR SUPPORT			
132 - 125	$\overline{\text{EXVID}}$	I	**ENABLE EXTERNAL VIDEO DATA:** A Feature Connector input. A low tri-states the video data lines VID7:0. An internal pullup resistor is provided.
131 - 124	$\overline{\text{EXPCLK}}$	I	**ENABLE EXTERNAL PIXEL CLOCK:** A Feature Connector input. A low tri-states the PCLK output. An internal pullup resistor is provided.
POWER AND GROUND			
18 - 2	VCC	-----	+5VDC
50 - 35	VCC	-----	+5VDC
84 - 74	VCC	-----	+5VDC
116 - 107	VCC	-----	+5VDC
5 - 13	VSS	-----	Ground
17 - 25	VSS	-----	Ground
29 - 38	VSS	-----	Ground
40 - 55	VSS	-----	Ground
51 - 71	VSS	-----	Ground
67 - 89	VSS	-----	Ground
83 - 110	VSS	-----	Ground
99 - 120	VSS	-----	Ground
117 - 131	VSS	-----	Ground
127 - 143	VSS	-----	Ground
- 1 - 18 - 36 - 37 - 54 - 72 - 73 - 90 - 108 - 109 - 126 - 144			These pins are not connected in the 144-pin EIAJ package

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to V_{SS}	-0.3 to 7 Volts

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

5.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0° to 70°C
Power Supply Voltage	4.75 to 5.25 Volts
Power Dissipation	140 mA

5.2 DC CHARACTERISTICS

The WD90C30 outputs have 4.0 mA maximum source and sink capability (see Table 4), except as follows:

IRQ, IOCHRDY, $\overline{0WS}$,
$\overline{MEMCS16}$, $\overline{IOCS16}$ = 24 mA sink.

PCLK, VID7:0, $\overline{BLANK}$ = 10 mA source/sink.

DRAM Interface = 4 mA source/sink
(RAS, CAS, $\overline{WE}$, $\overline{OE}$, MA, MD)

HSYNC, VSYNC, DA15:0 = 6 mA sink.

$\overline{ROM16}$ = 16 mA SINK.

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS
V(IL)	Input Low Voltage	-0.3	0.8	V	VCC=5V±5%
V(IH)	Input High Voltage	2.0	VCC+0.3	V	VCC=5V±5%
I(IL)	Input Low Current	--	±10	uA	VIN=0.0V
I(IH)	Input High Current	--	±10	uA	VIN=VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +2.0mA
V(OH)	Output High Voltage	2.4	--	V	IOH=-2.0mA
I(OZ)	High Impedance Leakage Current	-10.0	10.0	uA	OV<VOUT<VCC
C(IN)	Input Capacitance	--	10	pF	FC=1 MHz
C(OUT)	Output Capacitance	--	10	pF	FC=1 MHz
CI/O	I/O Pin Capacitance	--	12	pF	FC=1 MHz

TABLE 4. DC CHARACTERISTICS

6.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section:

- All units are in nanoseconds.
- C_L = 30 pF unless otherwise noted.
- nt implies n X t, (n times the period t). e.g. 1t, 2t etc.
- #n refers to the spec number in column 1 of the same table.

NUMBER	PARAMETER	MIN	MAX	NOTES
	RESET TIMING			
1	Reset Pulse Width	10t		t = 1/MCLK (For configuration at power up.)
2	MD Setup to RSET low	50		
3	MD Hold from RSET low	30		
4	RSET low to first $\overline{IOW}$	10t		
	CLOCK TIMING			
1 *	VCLK Period	12.5	72.0	
2	VCLK high	5		@ 1/2 VDD
3	VCLK low	5		@ 1/2 VDD
4 *	Clock Rise Time		2	1V - (VDD - 1V)
5 *	Clock Fall Time		2	1V - (VDD - 1V)
6	VCLK to PCLK Delay	8	20	45 ns @ 120 pF load
7a	VCLK to HSYNC Delay	8	25	
7b	VCLK to VSYNC Delay	8	25	
7c	VCLK to $\overline{BLANK}$ Delay	8	20	
7d	VCLK to VID(7:0) Delay	8	20	45 ns @ 120 pF load up to 30 MHz
8 **	MCLK period	20	30	Max 50 MHz, min 33.3 MHz
9	MCLK high	8		@ 1/2 VDD
10	MCLK low	8		@ 1/2 VDD
11	VID (7:0) setup to PCLK	3		
12	VID (7:0) hold from PCLK	3		

TABLE 5. AC TIMING CHARACTERISTICS

* Apply to both VCLK and MCLK.

** VCLK0 and MCLK use CMOS level input buffers. $V(IL)_{max}$ = 1.5V, $V(IH)_{min}$ = VDD - 1.5V

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE AT MODE TIMING			
1	EMEM setup to $\overline{MRD}$, $\overline{MWR}$ low	20		
2	EMEM hold from $\overline{MRD}$,$\overline{MWR}$ high	10		
3a	A(23:17) setup to ALE low	20		
3b	$\overline{BHE}$, DA(15:0) setup to $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	18		
4a	A(23:17) hold from ALE low	10		
4b	DA(15:0) hold from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	10		
5	$\overline{EIO}$ setup to $\overline{IOR}$/$\overline{IOW}$ low	20		
6	$\overline{EIO}$ hold from $\overline{IOR}$/$\overline{IOW}$ high	10		
7a	$\overline{EABUF}$ high from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ low	9	25	
7b	$\overline{EDBUF}$ low from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ low	13.5	35	
7c	$\overline{HTL}$ low from $\overline{MRD}$ low		25	
8a	$\overline{EABUF}$ low from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ high	14.5	35	
8b	$\overline{EDBUF}$ high from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ high	8.5	25	
8c	$\overline{HTL}$ high from $\overline{MRD}$ high		25	
9	DIR high from $\overline{IOR}$,$\overline{MRD}$ low		20	
10	DIR hold from $\overline{IOR}$ and $\overline{MRD}$ high		20	
11	DA(15:0) write data setup to $\overline{IOW}$, $\overline{MWR}$ high	20		
12a	DA(15:0) read data hold from $\overline{IOR}$ high or $\overline{MRD}$ high	10		
12b	DA(15:0) write data hold from $\overline{IOW}$, $\overline{MWR}$ high	10		
13	DA(15:0) read data valid after $\overline{IOR}$ low		70	
14	RDY high from $\overline{MWR}$/$\overline{MRD}$ low *(max is for standard VGA modes)*	10	2.45 µs	
15	Memory read data valid from RDY high		40	Note 1
16	RDY low from $\overline{MWR}$/$\overline{MRD}$ low	10	20	C_L = 100 pF
17	RDY tristate from $\overline{MWR}$/$\overline{MRD}$ high	10	30	C_L = 100 pF
18	$\overline{EBROM}$ low from valid A(23:15)		40	
19	$\overline{EBROM}$ hold from $\overline{MRD}$ high		40	
20a	$\overline{WPLT}$ low from $\overline{IOW}$ low		37	
20b	RPLT low from $\overline{IOR}$ low		30	
21a	$\overline{WPLT}$ high from $\overline{IOW}$ high	9	15	
21b	$\overline{RPLT}$ high from $\overline{IOR}$ high	9	20	
22	$\overline{EBROM}$ low from $\overline{IOW}$ low (46E8H Port)		1t + 20	
23	$\overline{EBROM}$ high from $\overline{IOW}$ high (46E8H Port)		25	
24	VCLK1 low from $\overline{IOW}$ low (3C2H Port)		1t + 24	

TABLE 5. AC TIMING CHARACTERISTICS (Continued)

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE AT MODE TIMING			
25	VCLK1 high from $\overline{IOW}$ high (3C2H Port)		15	
26	A(15:0) valid to $\overline{IOCS16}$ low		35	C_L = 100pF
27	$\overline{IOCS16}$ hold from $\overline{IOW}$ high		20	C_L = 100pF
28	A(23:17) valid to $\overline{MEMCS16}$ or $\overline{ROM16}$ low		39	C_L = 100pF
29	$\overline{MEMCS16}$ tristate from the next active ALE		39	C_L = 100pF
30a	$\overline{IOR}$, $\overline{IOW}$, $\overline{MWR}$, $\overline{MRD}$ high	2t + 15		t = ^{1}/MCLOCK Note 2
30b	$\overline{IOR}$, $\overline{IOW}$, $\overline{MWR}$, $\overline{MRD}$ low	2t		t = ^{1}/MCLOCK (Note 3)
30c	ALE pulse width	30		
31	$\overline{OWS}$, low from $\overline{IOW}$, $\overline{MWR}$ low		15	C_L = 100pF

Note 1: Depends on setting of PR31 (3C5H, index 11H) bits 4, 3. t = ^{1}/MCLOCK
00 - Max 40
01 - Max 40 + 1t
10 - Max 40 + 2t
11 - Max 40 - 1t

Note 2: Minimum of #30a should be the greater of 2t + 15 or (#8a + #3b + delay on the external address buffer)

Note 3: Minimum of #30b should be the greater of 2t or (#7b + #11 + delay on the external data buffer)

TABLE 5. AC TIMING CHARACTERISTICS (Continued)

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE MICRO CHANNEL MODE TIMING			
1	A(23:0),EMEM,$\overline{BHE}$ setup to $\overline{CMD}$ low	20		
2	A(23:0),EMEM,$\overline{BHE}$ hold from $\overline{CMD}$ low	10		
3	$\overline{CDSETUP}$,$\overline{EIO}$ setup to $\overline{CMD}$ low	20		
4	$\overline{CDSETUP}$,$\overline{EIO}$ hold from $\overline{CMD}$ low	15		
5	STATUS setup to $\overline{CMD}$ low	20		
6	STATUS hold from $\overline{CMD}$ low	15		
7a	$\overline{EDBUFH}$, $\overline{EDBUFL}$ low from $\overline{CMD}$ low	13.5	35	
7b	$\overline{EABUF}$ high from $\overline{CMD}$ low	9	25	
8a	$\overline{EDBUFH}$, $\overline{EDBUFL}$ high from $\overline{CMD}$ high	8.5	25	
8b	$\overline{EABUF}$ low from $\overline{CMD}$ high	14.5	35	
9	DIR active from $\overline{CMD}$ low		20	
10	DIR inactive from $\overline{CMD}$ high		20	
11	$\overline{CSFB}$ delay from valid address/status		30	C_L = 100 pF
12	$\overline{CSFB}$ hold from $\overline{CMD}$ high (I/O cycle)		30	C_L = 100 pF
13	$\overline{CSFB}$ hold from invalid address (memory cycle)		30	C_L = 100 pF
14	$\overline{CDDS16}$ delay from valid address		40	
15	$\overline{CDDS16}$ hold from invalid address		30	
16	DA(15:0) write data setup to $\overline{CMD}$ high	20		
17	DA(15:0) Write data hold after $\overline{CMD}$ high	10		
18	DA(15:0) I/O Read data valid from $\overline{CMD}$ low		70	
19	RDY high delay from $\overline{CMD}$ low	0	2.45 µs	
20	DA(15:0) Memory Read Data valid from RDY high		40	Note 1
21a	$\overline{CMD}$ high (inactive)	2t + 15		Note 2
21b	$\overline{CMD}$ low	2t		Note 3
22	RDY low delay from valid address/status		30	
23	$\overline{EBROM}$ low from valid address		40	
24	$\overline{EBROM}$ high from $\overline{CMD}$ high		30	
25	$\overline{WPLT}$ /$\overline{RPLT}$ low from $\overline{CMD}$ low	9	20	
26	$\overline{WPLT}$ /$\overline{RPLT}$ high from $\overline{CMD}$ high	9	20	
27	VCLK1 low from $\overline{CMD}$ low (3C2H Port)		1t + 30	
28	VCLK1 high from $\overline{CMD}$ high (3C2H Port)		25	

Note 1: Depends on setting of PR31 (3C5H, Index 11H) bits 4, 3. t = ^{1}/MCLK
00 max 40 ns
01 max 40 ns + 1t
10 max 40 ns + 2t
11 max 40 ns - 1t

Note 2: Minimum of #21a is the greater of 2t + 5 or (#8b + #1 + delay on external address buffer)

Note 3: Minimum of #21b is the greater of 2t or (#7a + #16 + delay on external data buffer)

TABLE 5. AC TIMING CHARACTERISTICS (Continued)

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM TIMING (256K by 4, 256K by 16)			
1	$\overline{RAS}$ cycle time	*6t		
2	$\overline{RAS}$ pulse width low	*3.5t - d		
3	$\overline{RAS}$ high time (precharge)	*2.5t + d		
4	$\overline{RAS}$ low to $\overline{CAS}$ low	*2.5t - 9	2.5t - d	
5	$\overline{CAS}$ cycle time	2t		
6	$\overline{CAS}$ pulse width low	*1t + d		
7	$\overline{CAS}$ high time (precharge)	*1t - d		
8	Row address setup to $\overline{RAS}$ low	1t - 10		
9	Row address hold time from $\overline{RAS}$ low	1t		
10	Column address setup to $\overline{CAS}$ low	1t - 10		
11	Column address hold from $\overline{CAS}$ low	1t		
12	Read Data valid before $\overline{CAS}$ high	3		
13	Read Data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t - 15		
15	Write Data hold after $\overline{CAS}$ low	1t - 5		
16	$\overline{WE}$ low setup $\overline{CAS}$ low	1t- 5	1t + 5	
17	$\overline{WE}$ low hold after $\overline{CAS}$ high	Same as $\overline{CAS}$ low		
18	$\overline{OE}$ high before $\overline{WE}$ low	2t - 10		
19	$\overline{OE}$ low after $\overline{WE}$ high	1t - 10		
20	$\overline{CAS}$ high for $\overline{CAS}$ before $\overline{RAS}$ refresh	1t - 10		
21	$\overline{RAS}$ low from $\overline{CAS}$ low for $\overline{CAS}$ before $\overline{RAS}$ refresh	1.5t + 10		

Notes:
The timing is the result of setting PR33 (3C5H, Index = 13H) = XXX00000
* Timings are adjustable by PR33.
Memory write uses fast page early write, while keeping $\overline{OE}$ = 1.
Memory read uses fast page read, while keeping $\overline{OE}$ = 1.
t = ^{1}/MCLK
(MCLK = 37.5 MHz for 80 ns DRAM)
(MCLK = 40 MHz for some faster 80 ns DRAM)
(MCLK = 44.4 MHz for 70 ns DRAM)
(MCLK = 49.5 MHz for 60 ns DRAM)
} Maximum MCLK frequency
d = Delay with a min of 4 ns and a max of 7 ns.

TABLE 5. AC TIMING CHARACTERISTICS (Continued)

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM TIMING (64K by 16)			
1	$\overline{RAS}$ cycle time	*5t		
2	$\overline{RAS}$ pulse width low	*3t		
3	$\overline{RAS}$ high time (precharge)	*2t		
4	$\overline{RAS}$ low to $\overline{CAS}$ low	*1.5t	1.5t	
5	$\overline{CAS}$ cycle time	2t	2t	
6	$\overline{CAS}$ pulse width low	* 1t + 2d		
7	$\overline{CAS}$ high time (precharge)	* 1t - 2d		
8	Row address setup to $\overline{RAS}$ low	1t		
9	Row address hold time from $\overline{RAS}$ low	1/2t		
10	Column adress setup to $\overline{CAS}$ low	1t - 10		
11	Column address hold from $\overline{CAS}$ low	1t		
12	Read Data valid before $\overline{CAS}$ high	2		
13	Read Data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t - 15		
15	Write Data hold after $\overline{CAS}$ low	1t - 5		
16	$\overline{WE}$ low setup before $\overline{CAS}$ low	1t - 10		
17	$\overline{WE}$ low hold after $\overline{CAS}$ high	Same as $\overline{CAS}$ low		
18	$\overline{OE}$ high before $\overline{WE}$ low	1t + 2		
19	$\overline{OE}$ low after $\overline{WE}$ high	1t - 10		
20	$\overline{CAS}$ high for $\overline{CAS}$ before $\overline{RAS}$ refresh	0.5t		
21	$\overline{RAS}$ low from $\overline{CAS}$ low for $\overline{CAS}$ before $\overline{RAS}$ refresh	1.5t		

MCLK edge to $\overline{RAS}$, $\overline{CAS}$, MA(8:0) edge delay may be up to 40 ns.

NOTES:
The timing is the result of setting PR33 (3C5H, Index = 13H) = xxx01110
* Timings are adjustable by PR33
Memory write uses fast page early write, while keeping $\overline{OE}$ = 1.
Memory read uses fast page read, while keeping $\overline{OE}$ = 0.
t = ^{1}/MCLK (MCLK = 36 MHz for 80 ns, 64K by 16 DRAM)
d = Delay with a min of 4 ns and a max of 7 ns.

TABLE 5. AC TIMING CHARACTERISTICS (Continued)

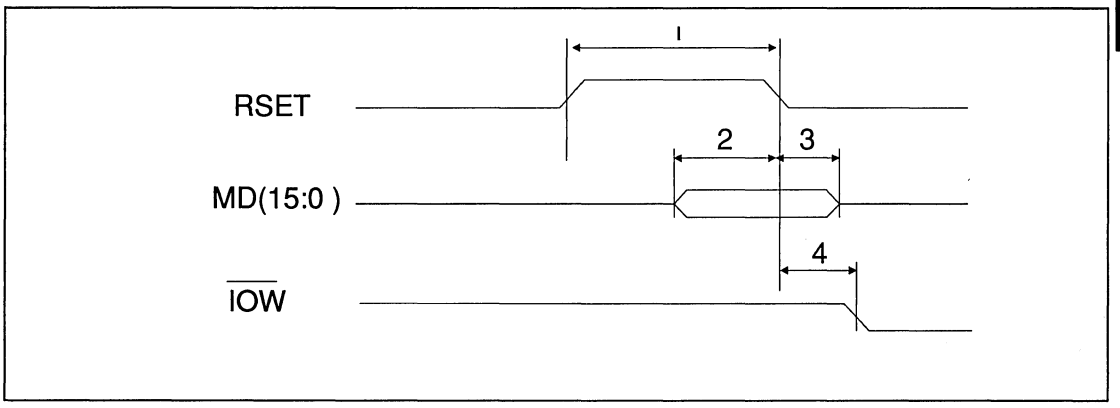

FIGURE 5. RESET TIMING

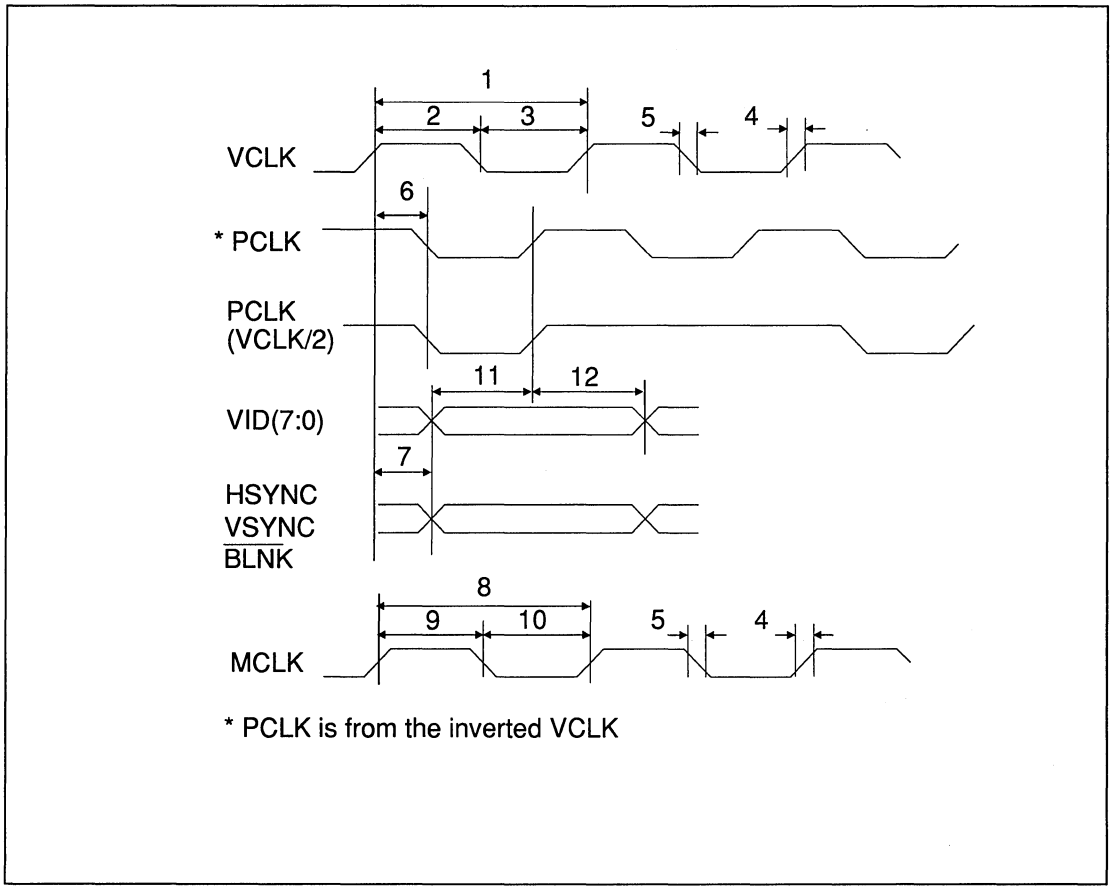

FIGURE 6. CLOCK AND VIDEO TIMING

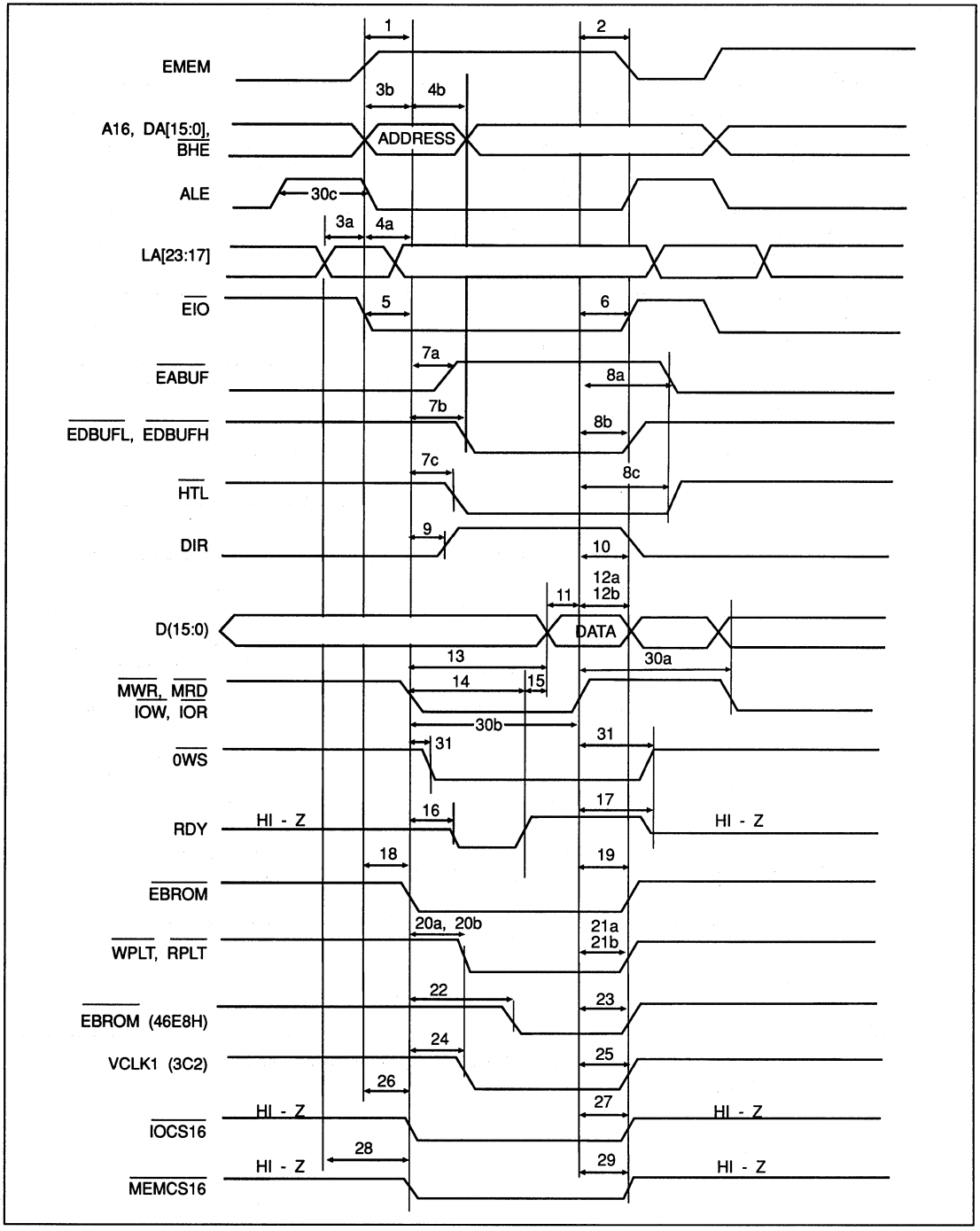

FIGURE 7. AT MODE BUS TIMING

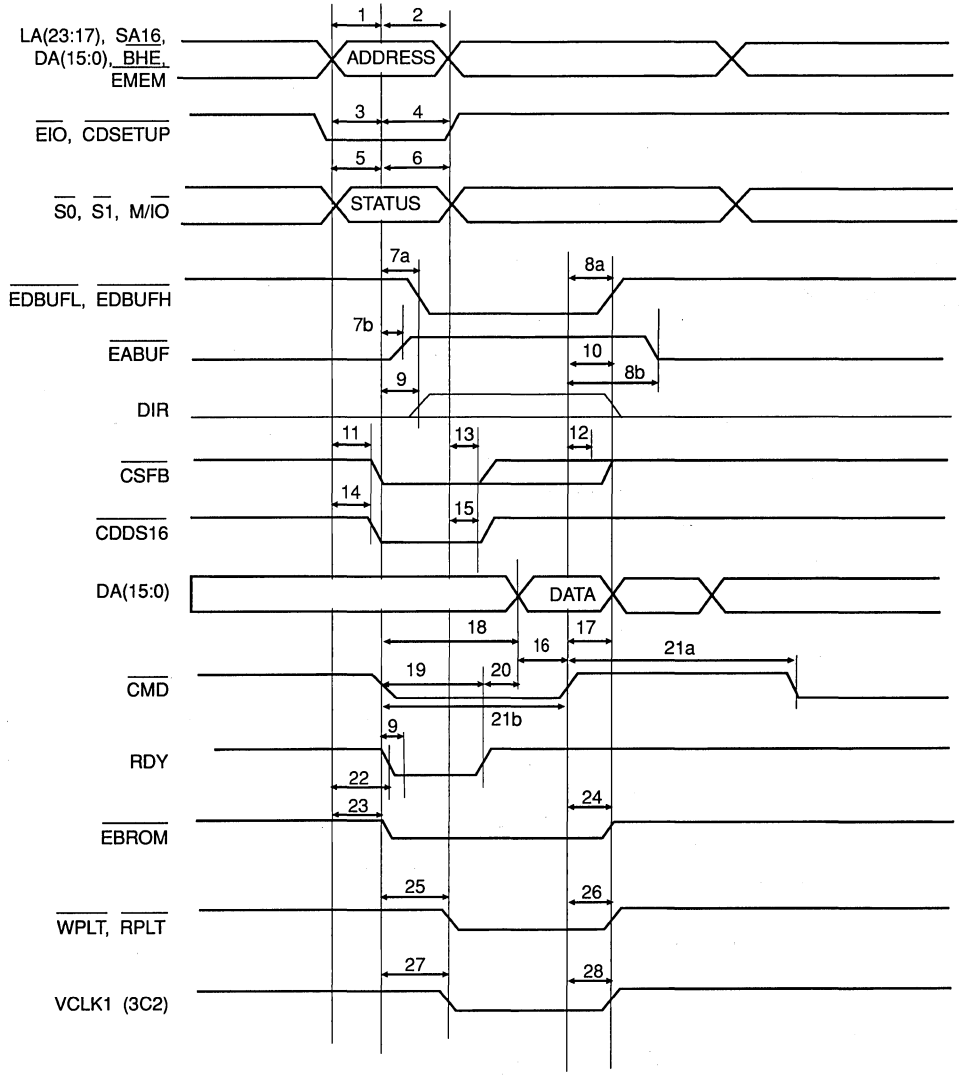

FIGURE 8. MICRO CHANNEL MODE BUS TIMING

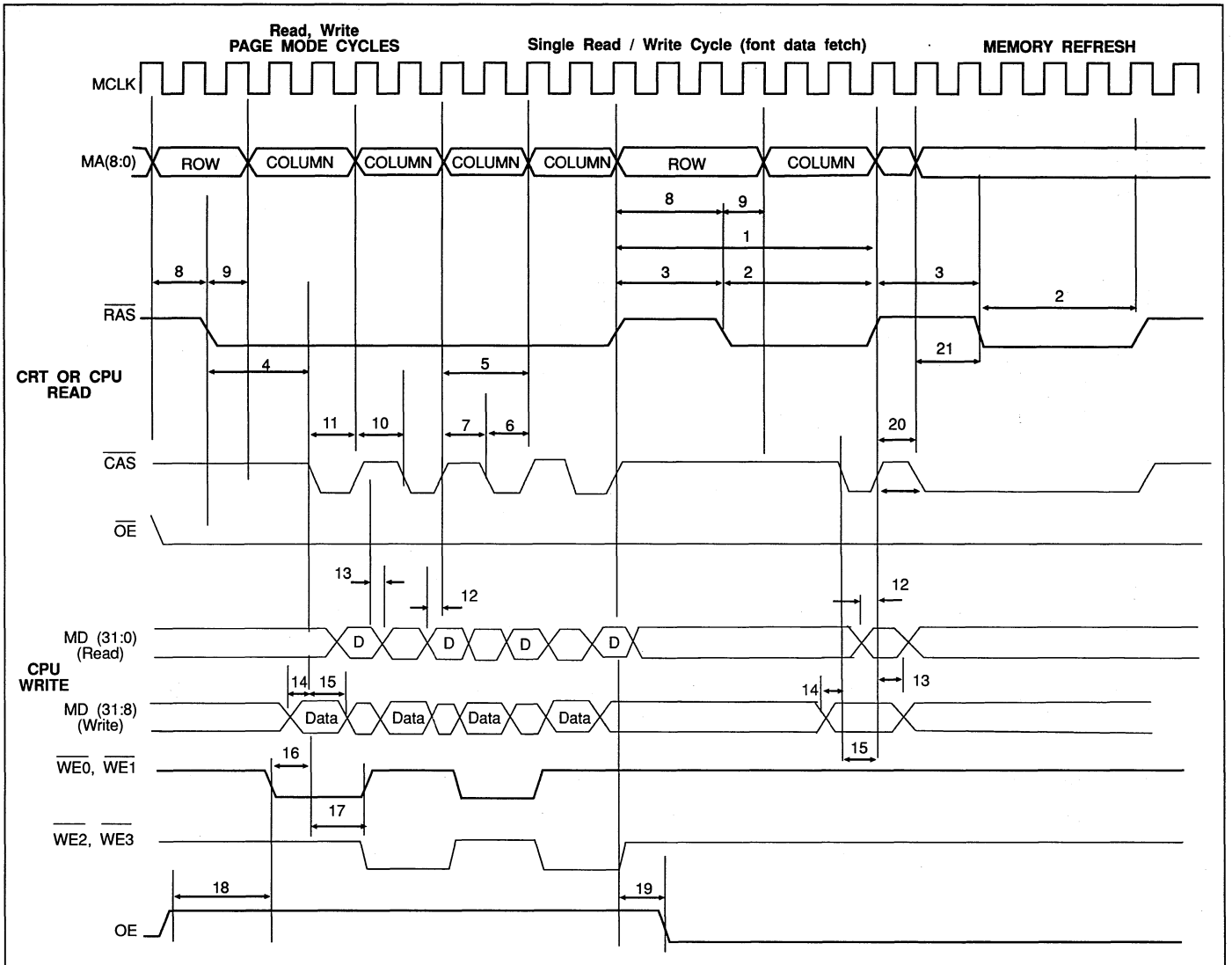

FIGURE 9. DRAM TIMING

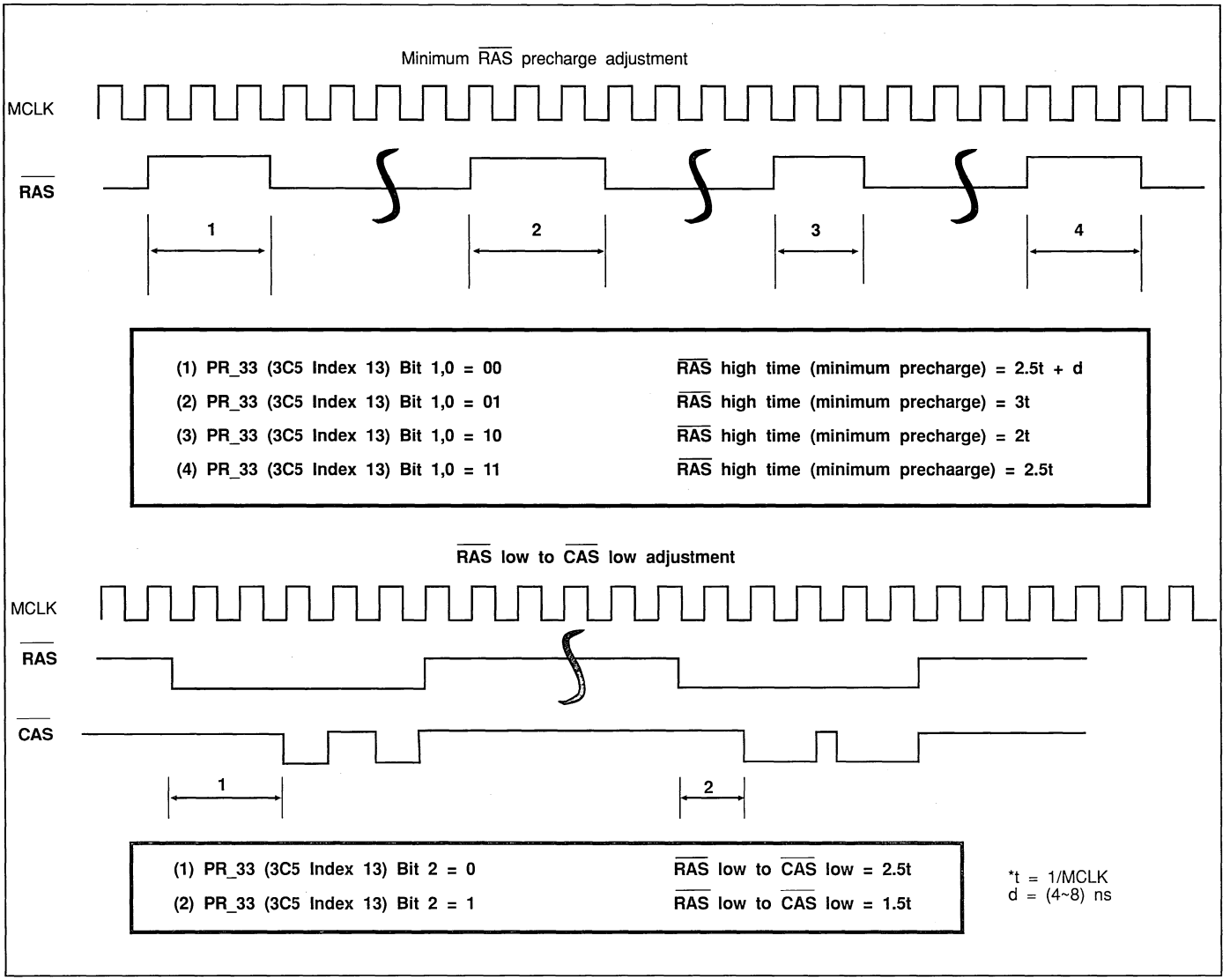

FIGURE 10. DRAM TIMING ADJUSTMENT

DRAM Timing Adjustment: The $\overline{RAS}$, $\overline{CAS}$ timing can be adjusted by register PR33 (3C5H, Index 3H) bits 4 through 0. Only the following timing may be affected: (See Figures 9 and 10).

3 $\overline{RAS}$ high time (precharge)
4 $\overline{RAS}$ low to CAS low
6 $\overline{CAS}$ pulse width

$\overline{CAS}$ pulse width adjustment: $\overline{CAS}$ cycle time is always equal to 2t {t = 1/MCLK}, {d = (4~ 8) ns}.

PR33 (Bits 4 through 3) =
00, $\overline{CAS}$ low = 1t + d; $\overline{CAS}$ high = 1t - d
01, $\overline{CAS}$ low = 1t + 2d; $\overline{CAS}$ high = 1t - 2d
1X, $\overline{CAS}$ low = 1.5t; $\overline{CAS}$ high = $^1/2$t

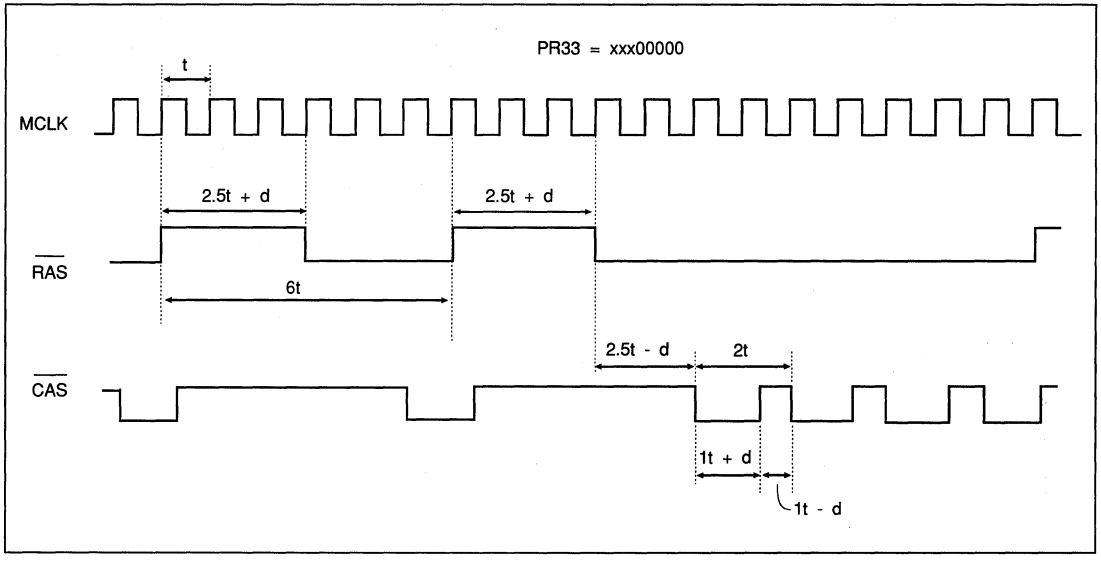

FIGURE 11. 256K BY 4 DRAM TIMING

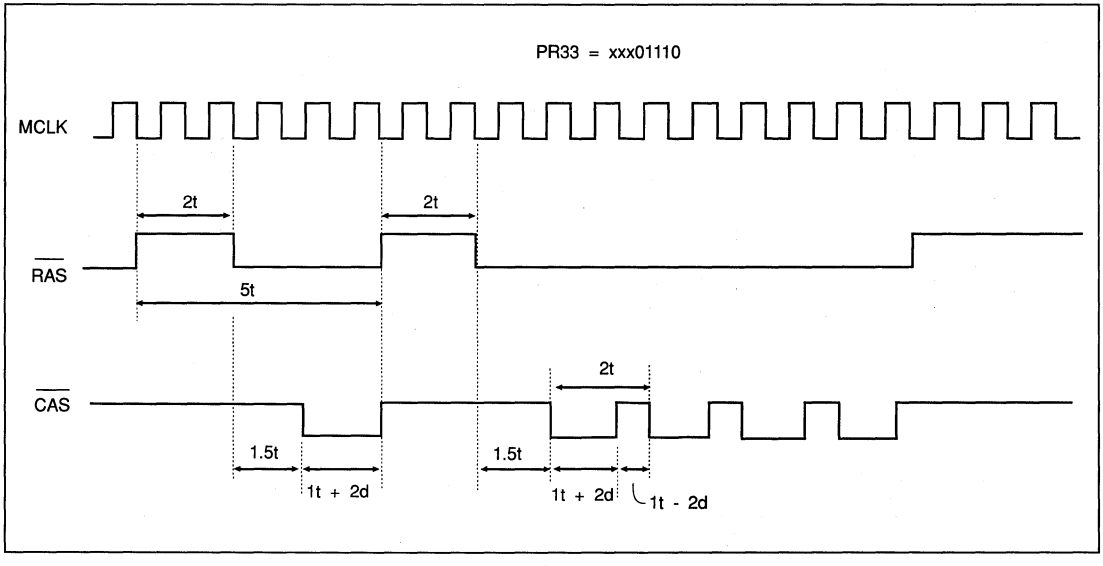

FIGURE 12. 64K BY 16 DRAM TIMING

7.0 WD90C30 REGISTERS

All the standard IBM registers incorporated inside the WD90C30 are functionally equivalent to the VGA implementation while additional Western Digital registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA registers in greater detail, followed by the VGA/EGA difference section and PR registers description. For more information, refer to the reference literature.

Throughout this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Register	W			3C2
	R			3CC
Input Status Register 0	RO			3C2
Input Status Register 1	RO	3BA	3DA	
Feature Control Register	W	3BA	3DA	
	R			3CA
*Video Subsystem Enable Register	RW			3C3
* I/O Port 3C3H can be used to replace 46E8H [if CNF(9) = 0] for setup in AT mode. In Micro Channel mode, writes to 3C3H, Bit 0 = 1 enables memory and I/O address decoding.				
SEQUENCER REGISTERS				
Sequencer Index Register	RW			3C4
Sequencer Data Register	RW			3C5
CRT CONTROLLER REGISTERS				
Index Register	RW	3B4	3D4	
CRT Controller Data Register	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Register	RW			3CE
Other Graphics Registers	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Register	RW			3C0
Attribute Controller Data Register	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Read Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

1. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.
2. All Register addresses are in hexidecimal

TABLE 6. VGA REGISTERS SUMMARY

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
PR18 CRTC Vertical Timing Overflow	RW	3B5.3E	3B5.3E
PR19 Signature Analyzer Control	RW	3B5.3F	3D5.3F
Reserved 3X5.31- 3X5.3C	RW	3B5.31 - 3B5.3C	3D5.31 - 3D5.3C
PR1A CRTC Shadow Register Control	RW	3B5.3D	3D5.3D
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21 Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR22 Scratch Pad	RW	3C5.8	3C5.8
PR23 Scratch Pad	RW	3C5.9	3C5.9
PR30 Memory Interface write buffer and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12
PR33 DRAM Timing and Zero Wait State Control Registers	RW	3C5.13	3C5.13
PR34 Video Memory Mapping Register	RW	3C5.14	3C5.14
PR35 USR0, USR1 Output Select Register	RW	3C5.15	3C5.15

NOTE:
All of the PR Registers may be read/write protected. Refer to the PR Registers description for more details.

TABLE 7. PR REGISTERS SUMMARY

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Register	WO	3B8	3D8	3D8	3B8
Color Select Register	WO		3D9	3D9	
Status Register	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Register	WO			3DE	
Hercules Register	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers.
4. ** = This register is loaded during power on.

TABLE 8. COMPATIBILITY REGISTERS SUMMARY

7.1 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:

1. Reserved bits should be set to zero.

2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes

   1 = D in Color Modes

7.1.1 Miscellaneous Output Register, Read Port = 3CCH, Write Port = 3C2H

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0 = Positive vertical sync polarity.
1 = Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0 = Positive horizontal sync polarity.
1 = Negative horizontal sync polarity.

NOTE:

*These bits determined the vertical size of the frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0 through 5, one memory page is selected from the two 64 Kbyte pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bits (3:2)

Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register Bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register Bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register Bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4H and 3B5H), or Color (3D4H and 3D5H) mode. Bit 0 also maps Input Status Register 1 at MDA (3BAH) or CGA (3DAH).

0 = CRTC and status addresses for MDA mode (3BX).
1 = CRTC and status addresses for CGA mode (3DX).

7.1.2 Input Status Register 0, Read Only Port = 3C2H

BIT	FUNCTION
7	CRT Interrupt
6:5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3:0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bits (6:5)

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode.
DA15 monitor status (Pin 20) is sampled and can be read from this bit.

Bits (3:0)

Reserved.

7.1.3 Input Status Register 1, Read Only Port = 3?AH

BIT	FUNCTION
7:6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2:1	Reserved
0	Display Enable

Bits (7:6)

Reserved.

Bits (5:4)

Color Plane Diagnostics.
These bits allow the processor to select two of eight colors by activating the Attribute Controller's Color Plane Enable Register Bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bits (2:1)

Reserved.

Bit 0

Display Enable Status.

0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

7.1.4 Feature Control Register, Read Port = 3CAH, Write Port = 3?AH

BIT	FUNCTION
7:4	Reserved
3	Vertical Sync Control
2:0	Reserved

Bits (7:4)

Reserved

Bit 3

Vertical Sync Control.

0 = VSYNC output enabled.
1 = VSYNC output is logical "OR" of VSYNC and Vertical Display Enable.

Bits (2:0)

Reserved

7.2 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to zero.

7.2.1 Sequencer Index Register, Read/Write Port = 3C4H

BIT	FUNCTION
7:5	Reserved
4:0	Sequencer Address/Index Bits

Bits (7:5)

Reserved.

Bits (4:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer Register to be accessed. Sequencer extension registers are also indexed by this register.

7.2.2 Reset Register, Read/Write Port = 3C5H, Index = 00H

BIT	FUNCTION
7:2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bits (7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

7.2.3 Clocking Mode Register, Read/Write Port = 3C5H, Index = 01H

BIT	FUNCTION
7:6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bits (7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on Bit 2.
1 = Serial shift registers loaded every 4th character clock (32-bit fetches).

Bit 3

Dot Clock Selection
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2

Shift Load. Effective only if Bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate an 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

7.2.4 Map Mask Register, Read/Write Port = 3C5H, Index = 02H

BIT	FUNCTION
7:4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bits (7:4)

Reserved.

Bits (3:0)

Controls Writing to Memory Maps (3-0), respectively.
0 = Writing to maps (3-0) disallowed.
1 = Maps (3-0) accessible.

7.2.5 Character Map Select Register, Read/Write Port = 3C5H, Index = 03H

BIT	FUNCTION
7:6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4, Bit 1 = 1, then the attribute byte Bit 3 in text modes is redefined to control switching between character sets. A "0" selects Character Map B. A "1" selects character map A. Character Map selection from either Plane 2 or Plane 3 is determined by PR2(2), PR2(5) and Bit 4 of the attribute code.

Bits (7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of Character Map A along with Bits 3 and 2, select the location of Character Map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit 4

Character Map B MSB Select.
The MSB of Character Map B along with Bits 1 and 0, select the location of Character Map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bits (3:2)

Character Map Select A.
Refer to Bit 5 table.

Bits (1:0)

Character Map Select B.
Refer to Bit 4 table.

7.2.6 Memory Mode Register, Read/Write Port = 3C5H, Index = 04H

BIT	FUNCTION
7:4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bits (7:4)

Reserved.

Bit 3

Chains Four Maps.

0 = Processor sequentially accesses data using map mask register.

1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.

0 = Even processor addresses to access Maps 0 and 2. Odd processor addresses to access Maps 1 and 3.

1 = Sequential processor access as defined by Map Mask Register.

Bit 1

Extended Video Memory.

0 = 64 KB of video memory.

1 = Greater than 64 KB of memory for VGA/EGA modes.

Bit 0

Reserved.

PORT	INDEX	VGA REGISTER NAME	*6845 REGISTER NAME
3?4	---	CRT Controller Address Register	CRTC Address Register
3?5	00	Horizontal Total	HorizontalTotal
3?5	01	Horizontal Display Enable End	Horizontal Display
3?5	02	Start Horizontal Blanking	+
3?5	03	End Horizontal Blanking	+
3?5	04	Start Horizontal Retrace	+
3?5	05	End Horizontal Retrace	+
3?5	06	Vertical Total	+Vert. Display
3?5	07	Overflow	+
3?5	08	Preset Row Scan	+
3?5	09	Maximum Scan Line/Others	Maximum Scan Line Address
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Address High
3?5	0D	Start Address Low	Start Address Low
3?5	0E	Cursor Location High	Cursor Location High
3?5	0F	Cursor Location Low	Cursor Location Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	+
3?5	14	Underline Location	+
3?5	15	Start Vertical Blank	+
3?5	16	End Vertical Blank	+
3?5	17	CRTC Mode Control	+
3?5	18	Line Compare	+

TEXT = 1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes
2. "*" 6845 Mode Registers are defined and explained in greater detail in the reference literature.
3. "+" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.
4. Reserved bits should be set to zero.
5. Port addresses are in hex.

TABLE 9. CRT CONTROLLER REGISTERS

7.3 CRT CONTROLLER REGISTERS

7.3.1 CRT Address Register, Read/Write Port = 3?4H

BIT	FUNCTION
7:5	Reserved
4:0	Index bits

Bits (7:5)

Reserved.

Bits (4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed in hexidecimal.

7.3.2 Horizontal Total Register, Read/Write Port = 3?5H, Index = 00H

BIT	FUNCTION
7:0	Horizontal Total Period

Bits (7:0)

Count Plus Retrace Less Five.
In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

7.3.3 Horizontal Display Enable End Register, Read/Write Port = 3?5H, Index 01H

BIT	FUNCTION
7:0	Displayed Characters per Scan Line

Bits (7:0)

This register contains the total number of displayed characters less one. This register is locked if PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.4 Start Horizontal Blanking Register, Read/Write Port = 3?5H, Index = 02H

BIT	FUNCTION
7:0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.5 End Horizontal Blanking Read/Write Port = 3?5H, Index = 03H

BIT	FUNCTION
7	Reserved
6:5	Display Enable Signal Skew Control
4:0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

Bit 7

Reserved

Bits (6:5)

Display Enable Signal Skew Control.
These bits define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

End Horizontal Blanking.
Start blanking register plus the width of the horizontal blank in character clocks. The least significant five bits are programmed in this register,

while the most significant bit is the End Horizontal Retrace Register (Index 05H) Bit 7. When the least significant five bits of the horizontal character counter matches these six bits, the horizontal blanking ends.

7.3.6 Start Horizontal Retrace Pulse Register, Read/Write Port = 3?5H, Index = 04H

BIT	FUNCTION
7:0	Start Horizontal Retrace Character Count

Bits (7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.7 End Horizontal Retrace Register, Read/Write Port = 3?5H, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6:5	Horizontal Retrace Delay
4:0	End Horizontal Retrace

This register is locked if the PR Register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

Bit 7

MSB (Sixth Bit) of End Horizontal Blanking Register.

Bits (6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace.
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

7.3.8 Vertical Total Register, Read/Write Port = 3?5H, Index = 06H

BIT	FUNCTION
7:0	Vertical Total Scan Lines

Bits (7:0)

Raster Scan Line Total Less 2.
The least significant eight bits of an eleven bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus two. Time for vertical retrace, and vertical sync are also included. The eighth and nineth bits of this count are loaded into the Vertical Overflow Register (Index = 07H) as Bit 0 and Bit 5, respectively. Bit 10 of this count is in the 3?5H, index 3EH, bit 0. In 6845 modes, total vertical display time in rows is programmed into Bit 6 - Bit 0, while Bit 7 is reserved. Scan count reduction is not necessary. The number of scan lines in a row is determined by the maximum Scan Line Register (Index 09H Bits 4 through 0). This register is locked if the PR Register PR3(0) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.9 Overflow Vertical Register, Read/Write Port = 3?5H, Index = 07H

BIT	FUNCTION
7	Vertical Retrace Start Bit 9
6	Vertical Display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical Display Enable End Bit 8
0	Vertical Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (Index = 10H).

****Bit 6**

Vertical Display Enable End Bit 9 (Index = 12H).

++Bit 5

Vertical Total Bit 9 (Index = 06H).

Bit 4

Line Compare Bit 8 (Index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (Index =15H).

++Bit 2

Start Vertical Retrace Start Bit 8 (Index = 10H).

++ Bit 1

Vertical Total Bit 8 (Index = 06H)

NOTES:

+ This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register Bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

7.3.10 Preset Row Scan Register, Read/Write Port = 3?5H, Index = 08H

BIT	FUNCTION
7	Reserved
6:5	Byte Panning Control
4:0	Preset Row Scan Count

Bit 7

Reserved.

Bits (6:5)

Byte Panning Control.
These bits allow up to three bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 Byte Left Shift
1	0	2 Bytes Left Shift
1	1	3 Bytes Left Shift

Bits (4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

7.3.11 Maximum Scan Line Register, Read/Write Port = 3?5H, Index = 09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4:0	Maximum Scan Line

Bit 7

200 to 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is Bit 9 of the Line Compare Register (Index = 18H).

Bit 5

Start Vertical Blank.
This is Bit 9 of the Start Vertical Blank Register (Index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bits (4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus one. In 6845 mode, Bits 5 through 7 are reserved, and Bits 4 through 0 are programmed with the maximum scan line count less one for non-interlace mode. Interlaced mode is not supported.

7.3.12 Cursor Start Register, Read/Write Port = 3?5H, Index = 0AH

BIT	FUNCTION
7:6	Reserved
5	Cursor Control
4:0	Cursor Start Scan Line

Bits (7:6)

Reserved.

Bit 5

Cursor Control.
0=Cursor on.
1=Cursor off.

Bits (4:0)

Cursor Start Scan Line.
These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less one. If this value is programmed with a value greater than the Cursor End Register (Index = 0BH), no cursor is generated. For 6845 modes, Bit 7 is reserved. Bit 5 controls the cursor operation and Bits 4 through 0 contain the cursor start value. Bit 6 is not used.

7.3.13 Cursor End Register, Read/Write Port = 3?5H, Index = 0BH

BIT	FUNCTION
7	Reserved
6:5	Cursor Skew
4:0	Cursor End Scan Line

Bit 7

Reserved.

Bits (6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks, e.g., one character clock skew moves the cursor right by one position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

Cursor End Scanline.
These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, Bits 7 through 5 are reserved and Bits 4 through 0 contain row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode, i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

7.3.14 Start Address High Register, Read/Write Port = 3?5H, Index = 0CH

BIT	FUNCTION
7:0	Start Address High Byte

Bits (7:0)

Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16-bit video memory address, used for screen refresh. The low order 8-bit register is at Index 0DH. The PR Register PR3 Bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes Bits 6 and 7 are forced to "0", regardless of this register's contents, while the lower order eight bits are at Index register 0DH.

7.3.15 Start Address Low Register, Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7:0	Start Address Low Byte

Bits (7:0)

Start Address Low Byte.
The lower order eight bits of the 16-bit video memory address in VGA or 6845 modes.

7.3.16 Cursor Location High Register, Read/Write Port = 3?5H, Index = 0EH

BIT	FUNCTION
7:0	Cursor Location High Byte

Bits (7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of the 16-bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at Index 0FH. In VGA mode, the PR Register PR3 Bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, Bits 6 and 7 are reserved, while Bits 5 through 0 are the high order bits of the cursor.

7.3.17 Cursor Location Low Register, Read/Write Port = 3?5H, Index = 0FH

BIT	FUNCTION
7:0	Cursor Location Low Byte

Bits (7:0)

Cursor Address Lower Byte Bits.
The lower order eight bits of the 16-bit video memory address in VGA or 6845 mode.

7.3.18 Vertical Retrace Start Register, Read/Write Port = 3?5H, Index = 10H

BIT	FUNCTION
7:0	Vertical Retrace Start (Lower eight bits)

Bits (7:0)

Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the 11-bit Vertical Retrace Start Register. Bits 8 and 9 are located in the Overflow Register (Index = 07H). Bit 10 is located in 3?5H, Index 3EH, bit 2. In 6845 compatible mode, this register shows the high order six bits in positions 5 through 0 as the light pen read back value, and Bits 6 and 7 are reserved. The lower order eight bits of the Light Pen Read Back Register are at the Index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3(0) = 1.

7.3.19 Vertical Retrace End Register, Read/Write Port = 3?5H, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3:0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller Index registers in the range of index 00H-07H. Line Compare Bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates three refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates five DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enable vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a "0" to) an internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bits (3:0)

Vertical Retrace End.
Specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The four-bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

7.3.20 Vertical Display Enable End Register, Read/Write Port = 3?5H, Index = 12H

BIT	FUNCTION
7:0	Vertical Display Enable End (Lower eight bits)

Bits (7:0)

Vertical Display Enable End Lower Eight Bits.
The eight lower bits of this 11-bit register defines where the active display frame ends. The programmed count is in scan lines minus one. Bits 8 and 9 are in the Overflow Register (Index 07H) at positions 1 and 6, respectively. Bit 10 is in 3?5H, Index 3EH, Bit 10

7.3.21 Offset Register, Read/Write Port = 3?5H, Index = 13H

BIT	FUNCTION
7:0	Logical Line Screen Width

Bits (7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K = 2 in byte mode and K = 4 in word mode.

7.3.22 Underline Location Register, Read/Write Port = 3?5H, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4:0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count by Four for Double Word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by four.

Bits (4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where underline is to be displayed. Load a value one less than the desired scan line number.

7.3.23 Start Vertical Blank Register, Read/Write Port = 3?5H, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7:0	Start Vertical Blank (Lower eight bits)

Bits (7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the 11-bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (Index = 07H) and Bit 9 is in the Maximum Scan Line Register (Index = 09H). Bit 10 is 3?5H; Index 3EH, Bit 3. The eleventh bit value is reduced by one from the desired scan line count where the vertical blanking signal starts.

7.3.24 End Vertical Blank Register, Read/Write Port = 3?5H, Index = 16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7:0	End Vertical Blank

Bits (7:0)

Vertical Blank Inactive Count.
End Vertical Blank is an eight-bit value calculated as follows:
Eight-bit End Vertical Blank value = (value of Start Vertical Blank minus one) + (value of Vertical Blank signal width in scan lines).

7.3.25 CRT Mode Control Register, Read/Write Port = 3?5H, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by one bit and the MSB of the address counter appears on the LSB. See the Table 10.
1 = Byte address mode.

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.
0 = In word address mode, this bit enables Bit 13 to appear at MA0, otherwise Bit 0 appears on MAO.
1 = Select MA15 for odd/even mode when 256 Kbytes of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2
0 = Character clock increments memory address counter.
1 = Character clock divided by two increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select for Vertical Timing Counter.
0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by two.

Bit 1

Select Row Scan Counter.
0 = Selects row scan counter Bit 1 as output at MA14 address pin.
1 = Selects Bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller Compatibility Mode Support for CGA Operation.
0 = Row scan address Bit 0 is substituted for memory address Bit 13 at MA13 output pin during active display time.
1 = Enable memory address Pin 13 to be output at MA13 address pin.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLE WORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:
* See Bit 5, defining address wrap. This table is only applicable when PR Register PR1 Bits 7 and 6 equal zero, or PR16 Bit 1 equals one.

The CRT Underline Location Register (Index = 14H) Bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (Index 17H) Bit 6 controls addressing.

TABLE 10. WORD OR BYTE MODE

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7.3.26 Line Compare Register, Read/Write Port = 3?5H, Index = 18H

BIT	FUNCTION
7:0	Line Compare (lower eight bits)

Bits (7:0)

Line Compare Lower Eight Bits.
Lower eight bits of the ten-bit Scan Line Compare Register. Bit 8 is in the Overflow Register (Index = 07H) and Bit 9 is in the Maximum Scan Line Register (Index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

7.4 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE:
1. Reserved bits should be set to zero.

7.4.1 Graphics Index Register, Read/Write Port = 3CEH

BIT	FUNCTION
7:4	Reserved
3:0	Graphics Address Bits

Bits (7:4)

Reserved.

Bits (3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

7.4.2 Set/Reset Register, Read/Write Port = 3CFH, Index = 00H

BIT	FUNCTION
7:4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bits (7:4)

Reserved.

Bits (3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (Index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight-bit fill operation. The map designations are defined below:

0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE:
*The selection of Write Mode 0 is determined by the Graphics Mode Register (Index = 05H) Bit 1 and Bit 0.

7.4.3 Enable Set/Reset Register, Read/Write Port = 3CFH, Index = 01H

BIT	FUNCTION
7:4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bits (7:4)

Reserved.

Bits (3:0)

Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, these bits, set to "0", disable the Set/Reset Register (Index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.

1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (Index = 00H), and the respective memory map is written with the Set/Reset Register value.

7.4.4 Color Compare Register, Read/Write Port = 3CFH, Index = 02H

BIT	FUNCTION
7:4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bits (7:4)

Reserved.

Bits (3:0)

Color Compare.

The color compare bit contains the value to which all eight bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a "1" is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with Bit 3 = 0 for the Graphics Mode Register (Index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

7.4.5 Data Rotate Register, Read/Write Port = 3CFH, Index = 03H

BIT	FUNCTION
7:5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count Bit 2
1	Rotate Count Bit 1
0	Rotate Count Bit 0

Bits (7:5)

Reserved.

Bits (4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (Index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches
Note: "Data" refers to CPU data that has gone through data rotation. The latches contain the data from the last memory read operation.		

Bits (2:0)

Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (Index = 05H).

7.4.6 Read Map Select Register, Read/Write Port = 3CFH, Index = 04H

BIT	FUNCTION
7:2	Reserved
1	Map Select 1
0	Map Select 0

Bits (7:2)

Reserved.

Bits (1:0)

Map Select.
These bits select memory map in memory read operations. It has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained Maps 0 and 1 or value 10b or 11b to select the chained Maps 2 and 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

7.4.7 Graphics Mode Register, Read/Write Port = 3CFH, Index = 05H

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.

0 = Enables Bit 5 of this register to control loading of the shift registers. Four-bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by Bits 2 and 3 of the Color Select Register located at Index = 14H within the Attribute Controller.

1 = Load video shift registers to support 256-color mode.

Bit 5

Shift Register.

Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.

0 = Map 0 through Map 3 data is placed into shift registers for normal operations.

1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.

0 = Normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by Bit 2 of the Sequencer Memory Mode Register (Index = 04H). Even system addresses access Maps 0 or 2 and odd system addresses access Maps 1 or 3.

Bit 3

Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register (Index 04H). This setting will have no effect if Bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bits (1:0)

Write Mode.

Table 11 defines the four write modes.

BIT 1	BIT 0	WRITE MODE
0	0	**Write Mode 0.** If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is rotated right by the number of bits defined in the Data Rotate Register (with the old LSB now the new MSB).
0	1	**Write Mode 1.** This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	**Write Mode 2.** Memory maps (3:0) are filled with the eight-bit value of the corresponding CPU data bits (3:0). The 32-bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	**Write Mode 3.** Eight bits of the value contained in the Set/Reset Register (Index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (Index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an eight-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

TABLE 11. WRITE MODES

7.4.8 Miscellaneous Register, Read/Write Port = 3CFH, Index = 06H

BIT	FUNCTION
7:4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bits (7:4)

Reserved.

Bits (3:2)

Memory Map 1, 0.
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1

Odd/Even Mode.
0 = CPU address Bit A0 is the memory address Bit MA0.
1 = CPU address Bit A is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects Map 0 or 2, while A0 = 1 selects Map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode.
This bit is programmed the same way as Bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

7.4.9 Color Don't Care Register, Read/Write Port = 3CFH, Index = 07H

BIT	FUNCTION
7:4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bits (7:4)

Reserved.

Bits (3:0)

Memory Map Color Compare Operation.
0 = Disable color compare operation.
1 = Enable color compare operation.

7.4.10 Bit Mask Register, Read/Write Port = 3CFH, Index = 08H

BIT	FUNCTION
7:0	Bit Mask

Bits (7:0)

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.
0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

7.5 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:

1. The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (Port = 3?AH) clears the flip-flop and selects the Address Register, which is read through address 3C1H and written at address 3C0H. Once the Address Register has been loaded with an index, the next write operation to 3C0H will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0H, but does not toggle for reads to address 3C1H.
2. Attribute register data is written at 3C0H and register data is read from address 3C1H.
3. Reserved bits should be set to zero.

7.5.1 Attribute Index Register, Read/Write Port = 3C0H

BIT	FUNCTION
7:6	Reserved
5	Palette Address Source
4:0	Attribute Address Bits

Bits (7:6)

Reserved.

Bit 5

Palette Address Source.

0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (Index 00 - 0FH).

1 = Enable internal color palette and normal video translation.

Bits (4:0)

Attribute Controller Index Register Address Bits.

7.5.2 Palette Registers 00-0FH, Read Port = 3C1H/Write Port = 3C0H

BIT	FUNCTION
7:6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bits (7:6)

Reserved.

Bits (5:0)

Palette Pixel Colors.

They are defined as follows:

0 = Current pixel color deselected.

1 = Enable corresponding pixel color per the table below.

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

7.5.3 Attribute Mode Control Register, Read Port = 3C1H/Write Port = 3C0H, Index = 10H

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select.

0 = VID5 and VID4 palette register outputs are selected.

1 = Color Select Register (Index 14H) Bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width.

0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.

1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility.
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also Bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

7.5.4 Overscan Color Register, Read Port = 3C1H/Write Port = 3C0H, Index = 11H

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bits (7:0)

Overscan/Border Color.
They determine the overscan or border color. For monochrome display, this register is set to "0". Border colors are set as shown above.

7.5.5 Color Plane Enable Register, Read Port = 3C1H/Write Port = 3C0H, Index = 12H

BIT	FUNCTION
7:6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3:0	Enable Color Plane

Bits (7:6)

Reserved.

Bits (5:4)

Video Status Control.
These bits select two out of eight color outputs which can be read by the Input Status Register 1 (Port = 03?AH) Bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bits (3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

7.5.6 Horizontal Pel Panning Register, Read Port = 3C1H/Write Port = 3C0H, Index = 13H

BIT	FUNCTION
7:4	Reserved
3:0	Horizontal PEL Panning

Bits (7:4)

Reserved.

Bits (3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For nine dots/character modes, up to eight pixels can be shifted horizontally to the left. Likewise, for eight dots/character up to seven pixels can be shifted horizontally to the left. For 256 color, up to three position pixel shifts can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7.5.7 Color Select Register, Read Port = 3C1H/Write Port = 3COH, Index = 14H

BIT	FUNCTION
7:4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bits (7:4)

Reserved.

Bits (3:2)

Color Value MSB.
Two most two significant bits of the eight-digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bits (1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight-bit color value. They are selected by the Attribute Controller Mode Control Register (Index = 10H).

7.6 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
   0 = B in Monochrome Modes
   1 = D in Color Modes

7.6.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode.
If Bit 1=1 and Port 3BFH Bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable Blinking
1 = Enable Blinking

Bit 4

Reserved.

Bit 3

Video Enable.
0 = Video Disabled
1 = Video Activated

Bit 2

Reserved.

Bit 1

Port 3BFH Enabled.
0 = Prevents setting of Port 3BFH Bits 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFH Bits 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode.
Should be set to "1".
0 = High resolution disabled.
1 = High resolution is enabled.

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7.6.2 Hercules Registers

The Hercules Mode Register is a two-bit write only register located at I/O port address 3BFH. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8H overrides the write Port 3BFH functions defined by its Bits 0 and 1. The associated details are shown below.

7.6.3 Enable Mode Register 3B8H

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bits (6:2,0)

Reserved.

Bit 1

Port 3BFH Bit 0 Override.
0 = Prevents setting of Port 3BFH Bit 0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFH Bit 0 to switch for the alpha or graphics mode selection.

7.6.4 Hercules Compatibility Register, Write Only Port = 3BFH

BIT	FUNCTION
7:2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8H) Bit 7 selects the displayed memory page address in the graphics mode. When it is reset, Bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8H) Bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

7.6.5 Color CGA Operation Register, Write Only Port = 3D8H

BIT	FUNCTION
7:6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bits (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 2

B/W or Color Display Mode.
0 = Color Mode Selected.
1 = B/W Mode Selected.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

7.6.6 CGA Color Select Register, Write Only Port = 3D9H

BIT	FUNCTION
7:6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bits (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA (two bits per pixel).
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 2

Red Border/Background
Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

7.6.7 CRT Status Register, MDA Operation, Read Only Port = 3BAH

BIT	FUNCTION
7	VSYNC Inactive
6:4	Reserved
3	B/W Video Enabled
2:1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BXH).

Bits (6:4)

Reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bits (2:1)

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

7.6.8 CRT Status Register, CGA Operation, Read Only Port = 3DAH

BIT	FUNCTION
7:4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bits (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

7.6.9 AT&T/M24 Register, Write Only Port = 3DEH

This is a write only, eight-bit register located at address 3DEH. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting Bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5:4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in-color text modes.
1 = Underline attribute selects white underlined foreground.

Bits (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 Kbyte length).
1 = Display memory address starts at BC00:0H (16 Kbyte length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode, 400-line mode.
A 400-line monitor is required for this mode.
0 = 200-line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400-line graphics.

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
PR18 CRTC Vertical Timing Overflow	RW	3B5.3E	3B5.3E
PR19 Signature Analyzer Control	RW	3B5.3F	3D5.3F
Reserved 3X5.31- 3X5.3C	RW	3B5.31 - 3B5.3C	3D5.31 - 3B5.3C
PR1A CRTC Shadow Register Control	RW	3B5.3D	3D5.3D
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21 Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR22 Scratch Pad	RW	3C5.8	3C5.8
PR23 Scratch Pad	RW	3C5.9	3C5.9
PR30 Memory Interface write buffer and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12
PR33 DRAM Timing and zero Wait State Control Registers	RW	3C5.13	3C5.13
PR34 Video Memory Mapping Register	RW	3C5.14	3C5.14
PR35 USR0, USR1 Output Select Register	RW	3C5.15	3C5.15

NOTE:
All of the PR Registers may be read/write protected.

TABLE 12. PR REGISTERS SUMMARY

7.7 WD90C30 PR REGISTERS

The WD90C30 has additional features that enhance the performance and functions of the Western Digital Imaging PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C30 architecture is optimized with additional I/O registers.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES:

1. The designation 3?5H means that the register is mapped into either 3B5H in monochrome mode or 3D5H in color modes.
2. PR register notation - XXX.YY where XXX is the data port address and YY is the register index, e.g., 3CF.0F implies 0F → 3CEH (Select Index register) followed by (Data byte) → 3CFH (Data Port).

Registers PR0 through PR4 and PR11 through PR1A are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101. A register remains unlocked until another value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 Bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17 load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 Bit 1 to "1" does not read protect registers PR10 through PR17. PR21-PR23 and PR30-PR35 are R/W protected by PR20. PR20 must be loaded with 48H to make it possible to read or write to PR21-PR23 and PR30-PR35. All PR registers are set to "0" at power on reset except where noted.

7.7.1 Address Offset Registers PROA And PROB

PROA - Address Offset Register A, Read/Write Port = 3CFH, Index = 09H

BIT	FUNCTION
7:0	Primary Address Offset Bits

PROB - Address Offset Register B, Read/Write Port = 3CFH, Index = 0AH

BIT	FUNCTION
7:0	Alternate Address Offset Bits

The WD90C30 can control up to 1 Mbyte of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000H and ends at BFFFFH. To help VGA to reach the memory beyond this range, the WD90C30 has two CPU address offset registers PROA and PROB which can be used to support more than 128 Kbytes of linear display memory address space.

The contents of PROA (Bits 6:0) or PROB (Bits 6:0) are always added to the CPU address A(19:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture. PROA and PROB will then provide four Kbyte segmentation of the display memory. (Increment PROA or PROB by one of its equivalents to jump from a four Kbyte segment to another four Kbyte segment of the display memory.)

PROA and PROB are all set to zero at power-on-reset. There are two ways to control whether PROA or PROB get added into CPU address.

- **Sequencer Extension Register 3C5H, Index = 11H, Bit 7 = 0.**

  When PR1-3 = 0, then PR0A is always selected as the CPU address offset register.

  When PR1-3 = 1 and if the display memory is mapped into A000 - BFFFF (128 Kbytes), PR0A offset CPU address range is B0000 - BFFFF; the PR0B offset CPU address range is A0000 - AFFFF. (If CPU address bit A16 = 1, select PR0A. Otherwise PR0B is selected.)

  When PR1-3 = 1 and if the display memory is mapped into A0000 - AFFFF (64 Kbytes) or B0000 - B7FFF or B800 - BFFFF (32 Kbytes), then PR0B offset CPU address range is A0000 - A7FFF or B0000 - B7FFF. PR0A offset CPU address range is A8000 - AFFFF or B8000 - BFFFF. (If CPU address bit A15 = 1, select PR0A. Otherwise PR0B is selected.)

- **Sequencer Extension Register 3C5H, Index = 11H, Bit 7 = 1.**

  Both PR0A and PR0B are enabled. A CPU memory write will select PR0B as the offset register. Otherwise, PR0A is selected as the offset register.

7.7.2 PR1 - Memory Size, Read/Write Port = 3CFH, Index = 0BH

BIT	FUNCTION
7:6	Memory Size Select
5:4	Memory Mapping
3	Enable Alternate Address Offset Register PR0B
2	16-Bit System Interface
1	16-bit BIOS ROM
0	BIOS ROM Map Out

This register is eight bits wide. Bits PR1(1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(10), MD(0) using either pull-up or pull-down external resistors. Pull-up resistors on MD(10), MD(0) cause PR1(1:0) bits to be latched low.

Bits (7:6)

Memory Size.
These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits in conjunction with PR0A, PR0B, PR16(1) select the way memory is mapped into the CPU address space. IF PR16(1) is set to "1", the memory mapping will be set identical to the IBM VGA, regardless of PR1(7), PR1(6).

Tables 13 through 16 list the different settings on these two bits for different memory organizations.

PR1(7) = 0 PR1(6) = 0 256K TOTAL; IBM VGA MEMORY ORGANIZATION						
VIDEO RAM ADDR BIT	**BYTE CPU**	**CRT**	**WORD CPU**	**CRT**	**DBL WORD CPU**	**CRT**
MA(17)	PA	PA	PA	PA	PA	PA
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(14) or(3) XRN(5)	CA(15) or(4) CA(14)	A(14)	CA(12)

TABLE 13. IBM COMPATIBLE MEMORY ORGANIZATION

PR1 (7) = 0 PR1 (6) = 1 256K TOTAL; 64K/PLANE; WD90C30 MEMORY ORGANIZATION						
VIDEO RAM ADDR BIT	**BYTE CPU**	**CRT**	**WORD CPU**	**CRT**	**DBL WORD CPU**	**CRT**
MA(17)	PA	PA	PA	PA	PA	PA
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
----	----	----	----	----	----	----
----	----	----	----	----	----	----
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16) or(3) XRN(5)	CA(15)	A(16)	CA(14)

TABLE 14. WD90C30 MEMORY ORGANIZATION - 256 KBYTES

PR1(7) = 1, PR1(6) = 0 512K TOTAL;128K/PLANE; WD90C30 MEMORY ORGANIZATION						
VIDEO RAM ADDR BIT	**BYTE CPU**	**CRT**	**WORD CPU**	**CRT**	**DBL WORD CPU**	**CRT**
MA(17)	PA	PA	PA	PA	PA	PA
MA(16)	A(16)	CA(16)	A(17)	CA(16)	A(18)	CA(16)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16) or[3] XRN (5)	CA(15)	A(16)	CA(14)

TABLE 15. WD90C30 MEMORY ORGANIZATION - 512 KBYTES

PR1 (7), PR1 (6) = 1 1M TOTAL; 256K PLANE; WD90C30 MEMORY ORGANIZATION						
VIDEO RAM ADDR BIT	**BYTE CPU**	**CRT**	**WORD CPU**	**CRT**	**DBL WORD CPU**	**CRT**
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16)	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
MA(13)	A(13)	CA(13)	A(13)	CA(12)	A(13)	CA(11)
----	----	----	----	----	----	----
----	----	----	----	----	----	----
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(16) or[3] XRN (5)	CA(15)	A(18)	CA(16)

TABLE 16. WD90C30 MEMORY ORGANIZATION - 1 MBYTE

NOTES:

1. A(19:0) are WD90C30 internally modified system Addresses (CPU address + offset address).
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted Bit 5. XRN(5) can be used to replace CPU address bits in order to select memory pages in word mode. In IBM compatible memory mapping, 3C5.4, Bit 1 = 1 will select XRN(5) to replace CPU address bits. In other memory mapping schemes (PR1(7,6) ≠ 00, 3C5.4H, Bit 1 = 1 and PR16_2 = 1 will select XRN(5) to replace address bits.
4. CA(15) is selected as MA(0) if CRTC Mode Register 17, Bit 5 = 1 in word addressing modes.
5. PA is the memory plane select bit when DRAM interface is set for 16 bits.
   PA = 0 selects Plane 1,0
   PA = 1 selects Plane 2,3
6. MA 17-0 are divided into $\overline{RAS}$, $\overline{CAS}$ addresses as follows:

For 2256K by 4 DRAM or 256K by 16 DRAM	MA(16) - MA (8) ⇒ MA(17), M(7) - MA(0) ⇒	$\overline{RAS}$(8) - $\overline{RAS}$(0) $\overline{CAS}$(8) - $\overline{CAS}$(0)
For 64K by 16 DRAM	MA(15) - MA(8) ⇒ MA(7) - MA(0) ⇒	$\overline{RAS}$(7) - $\overline{RAS}$(0) $\overline{CAS}$(7) - $\overline{CAS}$(0)
MA(17,16) = 00 01 10 11	Select 1st 64K bank Select 2nd 64K bank Select 3rd 64K bank Select 4th 64K bank	

Bits (5:4)

PRI(5,4) Memory Map Select.

0	0	IBM VGA mapping. CPU addresses are decoded from 0A0000H - 0BFFFFH from the lowest 1 Mbyte CPU address space (depending on 3CF.06H bits 2 and 3).
0	1	First 256 Kbyte in any 1 Mbyte CPU addressing space (X00000H - X3FFFFH)
1	0	First 512 Kbyte in any 1 Mbyte CPU addressing space (X00000H - X7FFFFH)
1	1	In any 1Mbyte CPU address space (X00000H - XFFFFFH)

*PR34(3C5.14H) Bits 3-0 control to which 1 Mbyte of CPU address space the WD90C30 is mapped.

Bit 3

Enable Alternate Address Offset Register PROB.

Bit 2

Enable 16 bit system interface bus.
When set to "1", $\overline{MEMCS16}$ will be active low for all of the video memory cycles.

Bit 1

16-bit BIOS ROM.
When set to "1", the BIOS ROM has a 16 bit data path ($\overline{ROM16}$ will respond to ROM access). Otherwise, the BIOS ROM has an eight-bit data path.

A pull-down resistor on MD(10) will set this bit to "1" after power-on reset. This bit can also be set to "1" by an I/O write cycle only if the CNF(1) = 1.

Bit 0

BIOS ROM Map Out.
If set to "1", the BIOS ROM is mapped out. A pull-down resistor on MD(0) sets this bit to "1" at power-on-reset.

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7.7.3 PR2-Video Select Register, Read/Write Port = 3CFH, Index = 0CH

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4:3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register and Mode.

Bit 6

6845 Compatibility.
0: VGA or EGA mode
1: Non-VGA (6845) mode

Bit 5

Character Map Select.
The following functions are overridden by setting PR15(2). This bit in conjunction with PR2(2) and Bit 3 of the attribute code, enables character maps from Planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE:
Setting PR15(2) = 1, i.e., selecting page mode addressing overrides plane selected table shown above.

Bits (4:3)

Character clock period control.

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132-character text mode only)
1	0	9 dots
1	1	6 dots if PR17(5) = 0; 10 dots if PR17(5) = 1.

NOTE:
The character clock period control functions have no effect in graphics modes (Graphics Mode always uses eight dots).

Bit 2

Underline and character map select.
Setting this bit to "1" enables underline for all odd values of attribute codes, e.g., programming "1" gives blue underline. It overrides the background color function of the attribute code Bit 3, which is forced to "0". Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

Third Clock Select Line.
This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to "1". When CNF(3) is set to "0", it locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.
Uses VCLK when Sequencer Register 1, Bit 3, is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

7.7.4 PR3 - CRT Lock Control Register, Read/Write Port = 3CFH, Index = 0DH

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Bit 7

Lock VSYNC polarity as programmed at 3C2H Bit 7.

Bit 6

Lock HSYNC polarity as programmed at 3C2H Bit 6.

Bit 5

Lock Horizontal Timing.
Locks CRTC registers of Group 0 and 4. Prevents attempts by applications software to unlock Group 0 registers by setting 3?5.11H Bit 7 = 0.

Bit 4

Bit 9 Control.
Bit 9 of CRT Controller Start Memory Adress High Register 3?5.0CH and Bit 9 of Cursor Location High 3?5.0EH. This bit corresponds to Character Address CA(17).

Bit 3

Bit 8 Control.
Bit 8 of CRT Controller Start Memory Address High Register 3?5.0CH and Bit 8 of Cursor Location High 3?5.0EH. This bit corresponds to Character Address CA(16).

Bit 2

Cursor Control.
Cursor Start, Stop, Preset Row Scan, and Maximum Scan Line Address registers values multiplied by two.

Bit 1

Lock Prevention.
Bit 1 = 1 prevents attempts by applications software to lock registers of Group 1 by setting 3?5.11H, Bit 7 = 1.

Bit 0

Lock vertical timing.
Bit 0 = 1 locks CRTC registers of Groups 2 and 3. Overrides attempts by applications software to unlock Group 2 registers by setting 3?5.11H, Bit 7 = 0.

7.7.5 WD90C30 CRT Controller Register Locking

Register locking is controlled by four bits. They are PR3 (5,1,0) and 3?5.11H(7) (i.e. IBM Vertical Retrace End Register Bit 7 controlled by Index register 11). When 3?5.11H Bit 7 is "1", CRT controller registers (R0-7) are write-protected per VGA definition. For more information on the five groups and their locking schemes, refer to the following sections.

All Port and Index addresses are in hex.

- **Group 0**

  These registers are locked if PR3(5) = 1 OR 3?5.11(7) = 1.

  3?5 Index 00 - Horizontal Total Characters per scan

  3?5 Index 01 - Horizontal Display Enable End

  3?5 Index 02 - Start Horizontal Blanking

  3?5 Index 03 - End Horizontal Blanking

  3?5 Index 04 - Start Horizontal Retrace

  3?5 Index 05 - End Horizontal Retrace

- **Group 1**

  These registers are locked if PR3(1) = 0 AND 3?5.11(7) = 1.

  3?5 Index 07 (Bit 6) - Vertical Display Enable End Bit 9

3?5 Index 07 (Bit 1) - Vertical Display Enable End Bit 8

3?5 Index 0E (Bit 1) - Vertical Display Enable End Bit 10

- **Group 2**

  These registers are locked if PR3(0) = 1 OR 3?5.11(7) = 1.

  3?5 Index 06 - Vertical Total

  3?5 Index 07 (Bit 7) - Vertical Retrace Start Bit 9

  3?5 Index 07 (Bit 5) - Vertical Total Bit 9

  3?5 Index 07 (Bit 3) - Start Vertical Blank Bit 8

  3?5 Index 07 (Bit 2) - Vertical Retrace Start Bit 8

  3?5 Index 07 (Bit 0) - Vertical Total Bit 8

  3?5 Index 09 (Bit 5) - Start Vertical Blank Bit 9

  3?5 Index 3E (Bit 0) - Vertical Total Bit 10

  3?5 Index 3E (Bit 2) - Vertical Retrace Start Bit 10

  3?5 Index 3E (Bit 3) - Start Vertical Blank Bit 10

- **Group 3**

  These registers are locked if PR3(0) = 1.

  3?5 Index 10 - Vertical Retrace Start

  3?5 Index 11 [Bits(3:0)] - Vertical Retrace End

  3?5 Index 15 - Start Vertical Blanking

  3?5 Index 16 - End Vertical Blanking

- **Group 4**

  This register is locked if PR3(5) = 1.

  CRTC mode control register 17(Bit 2) - Selects divide-by-two vertical timing.

7.7.6 PR4 - Video Control Register, Read/Write Port = 3CFH, Index = 0EH

The video monitor output control register (PR4) can be programmed to tristate the CRT display control outputs as well as video data for the RAM-DAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLANK}}$ / Display Enable
6	PCLK=VCLK
5	Tristate Video Outputs
4	Tristate Memory Control Outputs
3	Override CGA Enable Video Bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Extended 256-color Shift Register Control

Bit 7

$\overline{\text{BLANK}}$ / Display Enable.
This bit controls the output signal $\overline{\text{BLANK}}$. Normally in the VGA mode, $\overline{\text{BLANK}}$ is used by the external video DAC to generate blanking. If this Bit = 1, the $\overline{\text{BLANK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15(1).

Bit 6

Select PCLK equal to VCLK.
0 = PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1 = PCLK is always the non-inverted VCLK input clock.

Bit 5

Tristate outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLANK}}$.

Bit 4

Tri-state memory control outputs.
The memory address bus MA(8:0), and all ten DRAM control signals are tri-stated when this bit is set to "1".

Bit 3

Override CGA Enable Video Bit.
Overrides the CGA "enable video" Bit 3 of mode register 3D8H, only in 80 by 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to "1". Power-on-reset causes no override.

Bit 2

Set to 1 to lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode.
It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3COH/3C1H change to write-only mode if the EGA compatibility bit is set. Setting this bit to "1" also disables reading PR0 through PR5. In VGA mode [PR(4) Bit 1 is zero] 3C0 register is read/write while 3C1H register is read only, per the Attribute Controller Register's definitions.

Bit 0

Extended Shift Register Control.
This bit should be set to "1" to select for extended 256-color modes (IBM Mode 13 is not included).

7.7.7 PR5 - General Purpose Status Bits, Read/Write Port = 3CFH, Index = 0FH

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PR0-PR4 Unlock
1	PR0-PR4 Unlock
0	PR0-PR4 Unlock

Bits (2:0) are read/write bits and cleared to zero by reset. They provide lock or unlock capability for PR registers PR0 through PR4. The PR0 through PR4 registers are unlocked when "X5H" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register Bits 4 through 8. Setting PR(4) Bit 1 to "1", read protects registers PR0 through PR5.

Bit 7	CNF(7) [READ ONLY]
Bit 6	CNF(6) [READ ONLY]
Bit 5	CNF(5) [READ ONLY]
Bit 4	CNF(4) [READ ONLY]
Bit 3	CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits and cleared to zero by reset. They control writing to PR registers PR0 through PR4 as follows:

2 1 0	PR0-PR4
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected
1 0 1	Write enabled

7.7.8 PR10 Unlock PR11-PR1A Read/Write Port = 3?5H, Index = 29H

This register is read/write and cleared to zero by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits (6:4), and Bits (2:0) control access to PR registers PR10-PR1A. Bits 7 and 3 enable register read operation for PR10 - PR1A. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 through PR1A.

BIT	FUNCTION
7	PR10-PR1A - Read Enable Bit 1
6:4	PR10(6:4) - Scratch Pad
3	PR10-PR1A - Read Enable Bit 0
2:0	PR11-PR1A - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test.

7.7.9 PR11 EGA Switches, Read/Write Port = 3?5H, Index = 2AH

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4/General Purpose
6	EGASW3/General Purpose
5	EGASW2/General Purpose
4	EGASW1/General Purpose
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA Configuration Switches SW4-SW1.
These read/write bits from corresponding memory data bus pins MD(15:12) are latched internally at power-on-reset with either pull-up or pull-down external resistors. Pulling-up MD(15:12) causes PR11(7:4) to be latched high. These bits can be read as Bit 4 of Port 3C2H if the EGA compatibility bit [PR4(1)] has been set to "1". Selection of the bit to be read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2H, as follows. These bits can be used as General Purpose scratch bits.

WRITE		READ
3C2 bit 3	3C2 bit 2	3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are read/write and cleared to zero at power-on-reset.

Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select.
This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer Screen Control.
Setting PR11(1) to "1" prevents modification of the following bits in the Graphics Controller as well as the Sequencer:

Graphics Controller	3CF.05H bits (6:5)
Sequencer	3C5.01H bits (5:2)
Sequencer	3C5.03H bits (5:0)

Although the internal functions selected by the graphics controller and sequencer bits are locked by setting PR11 Bit 1 to "1", they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 Dots.
Setting this bit to "1" prevents modification of the Clocking Mode Sequencer Register 3C5.01H, Bit 0. Although eight or nine character timing is locked by setting PR11 Bit 0 to "1", the 3C5.01H Bit 0 appears unlocked to the system processor during read operations.

7.7.10 PR12 Scratch Pad, Read/Write Port = 3?5H, Index = 2BH

BIT	FUNCTION
7:0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power-up.

7.7.11 PR13 Interlace H/2 Start, Read/Write Port = 3?5H, Index = 2CH

BIT	FUNCTION
7:0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power-up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to "1". All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04H) and Horizontal Total Register (3?5.00H):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE:
In the above expression, HRD = Horizontal Retrace Delay, determined by Bits 6 and 5 of the Horizontal Retrace End Register (3?5.05H).

7.7.12 PR14 Interlace H/2 End, Read/Write Port = 3?5H, Index = 2DH

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to "0" by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4:0	Interlaced H/2 End

Bit 7

Enable IRQ.
This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to "0". This bit should not be set to "1" in MICRO CHANNEL operation.

Bit 6

Vertical Double Scan.
This bit should be set to "1" when emulating EGA on PS/2 display. Setting this bit to "1" causes the CRTC's Vertical Displayed Line Counter and Row Scan Counter to be clocked by divide-by-two horizontal timing, if vertical sync polarity (3C2H Bit 7=0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is: N=2(n+1).

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced Mode.
Setting this bit to "1" selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09H] = 0XX00000. Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 End Bits (4:0).
Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

7.7.13 PR15 Miscellaneous Control 1, Read/Write Port = 3?5H, Index = 2EH

BIT	FUNCTION
7	Read 46E8 Enable
6	High VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable Reading Port 46E8H.
This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to "1" enables I/O Port 46E8H to be read, regardless of the state of its own Bits 3 and 4 and of Port 102H, Bit 0 (sleep bit). Only Bits (4:0) of Port 46E8H are readable; Bits (7:5) are "0".

Bit 6

High VCLK.
Setting this bit to "1" adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much higher than the memory clock (MCLK) frequency. This bit should be set to "1" if: (MCLK in MHz / VCLK in MHz) equal to 1.5. This bit also should be set to "1" in all extended 256-color modes.

Bit 5

Latched VCLK1 and VCLK2.
This bit is used only if CNF(3) = 1 which configures the VCLK1 and VCLK2 pins as outputs. Setting This bit to "1" causes outputs VCLK1 and VCLK2 to equal Bits 2 and 3 of I/O write register (Miscellaneous Output Register) at 3C2H, respectively.

Bit 4

Select MCLK as Video Clock.
Setting this bit to "1" causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility.
This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to "1" if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to "1" causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing. Setting this bit to "1" also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing.
Setting this bit to "1" forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30-40%. Set this bit to "1" if 132 character mode timing is selected (see description of PR2). Setting this bit to "1" in any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to "1", it redefines the Character Map Select Register (3C5.03H). One of eight 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by Bits (2:0) of this register while the map selection is determined by the Bits (4:3). A pair of adjacent 8K character maps in Planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by Bit 3 of the attribute code.
The character attribute, Bit 3, in conjunction with Bits 3 and 4 of the Character Map Select Register (3C5.03H), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

NOTE:
The above Character Map Select functions override the functions of PR2(5) and PR2(2).

This bit must be set to "1" before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to "1" internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select.
This bit is used to select between two types of display enable timings available at output pin $\overline{\text{BLANK}}$ if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0 = $\overline{\text{BLANK}}$ supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = $\overline{\text{BLANK}}$ supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable Border.
Setting this bit to "1" forces the video outputs to "0" during the interval when border (overscan) color would be active.

7.7.14 PR16 Miscellaneous Control 2, Read/Write Port = 3?5H, Index = 2FH

BIT	FUNCTION
7	External Register 46E8H Lock
6	CRTC Address Count Width Bit 1
5	CRTC Address Count Width Bit 0
4	CRTC Address Counter Offset Bit 1
3	CRTC Address Counter Offset Bit 0
2	Enable Odd/Even Page Bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit 7

Lock External 46E8H Register.
Setting this bit to "1" causes $\overline{\text{EBROM}}$ output to be forced high (Inactive) during I/O writes to port 46E8H.

Bits (6:5)

CRTC Address Counter Width.
Power on reset clears these bits to "0". These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set "1" to ensure VGA and EGA compatible operation of the address counter, limited to 64K locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256KB
0	1	128K
1	X	64K

Bits (4:3)

CRTC Address Counter Offset.
Bits 4 and 3 are summed with the CRT Controller's Address Counter Bits CA(17) and CA(16), respectively, and the two-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even.
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06H(1) to "1", setting 3C5.04H(1) to "1", selecting extended memory, and setting 3C5.04H(3) to "0" to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2H(5)] to select between two pages of memory, by controlling video RAM address "0", regardless of the Memory Size Bits PR1(7:6).

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Bit 1

VGA Memory Mapping.
Setting this bit to "1", selects 256 Kbyte IBM VGA Mapping, regardless of the Memory Size Bits PR1(7:6).

Bit 0

Lock RAMDAC Write Strobe (3C6H - 3C9H).
0 = Normal operation.
1 = Output $\overline{WPLT}$ to be forced to "1", disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C30, is also protected from the modification, but may still be read at the Port 3C7H.

7.7.15 PR17 Miscellaneous Control 3, Read/Write Port = 3?5H, Index = 30H

BIT	FUNCTION
7:6	Reserved
5	Character Clock Period Select
4	PCLK = $^{VCLK}/_{2}$
3	Map out 4K of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map out 2K of BIOS ROM

Bits (7:6)

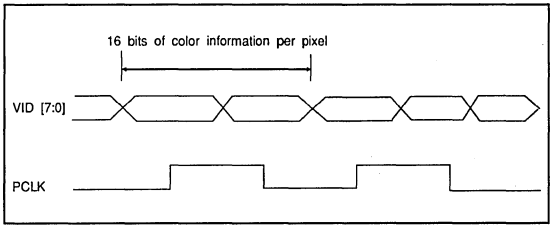
Reserved.

Bit 5:

Character Clock Period Select.
When PR2 (3CF.0CH), Bits 4:3 = "11", then setting this bit to "0" selects the six-dot font. Setting this bit to "1" selects the ten-dot font. Otherwise, this bit has no effect.

Bit 4

PCLK = $^{VCLK}/_{2}$.
Setting this bit to "1" forces PCLK = $^{VCLK}/_{2}$. This control is useful for interface with high color RAM-DAC as follows:



Bit 3

Map Out 4K of BIOS ROM.
Setting this bit to "1" disables access of the BIOS ROM in the system address range C600:0H through C6FF:FH. Power on reset sets this bit to "0".

Bit 2

Enable 64K BIOS ROM.
Setting this bit to "1" enables access of the BIOS ROM in the system address range C000:0H through CFFF:FH. Power on reset sets this bit to "0".

Bit 1

Hercules Compatibility.
Setting this bit to a "1" locks Hercules compatibility register (I/O Port 3BFH). Power on reset sets this bit to "0".

Bit 0

Map Out 2K of BIOS ROM.
Setting this bit to "1" disables access of the BIOS ROM in the system address range C600:0H through C67F:FH. Power-on-reset sets this bit to "0".

7.7.16 PR18 CRTC Vertical Timing Overflow, Read/Write Port = 3?5H, Index = 3EH

These bits combined with other vertical timing overflow bits in CRTC constitutes an 11-bit vertical timing control. These bits are set to zero at power-on-reset.

BIT	FUNCTION
7:5	Reserved
4	Line compare Bit 10
++3	Start vertical blank Bit 10
++2	Start vertical retrace Bit 10
**1	Vertical display enable end Bit 10
++0	Vertical total Bit 10
Note: ++ The bit is locked if PR3(0) = 1 OR the 3?5H Index 11H Bit 7 = 1 ** The bit is locked if PR3(1) = 0 AND the 3?5H Index 11H Bit 7 = 1	

7.7.17 PR19 Video Signature Analyzer Control Read/Write Port = 3?5H, Index = 3FH

BIT	FUNCTION
7:4	Reserved
3	Signature read enable
2	Enable video input
1	Preload control
0	Enable/Status bits

Bits (7:4)

Reserved

Bit 3

Signature Read Enable.
Set this bit to "1" in order to read signature analyzer results from 3?5H, Index 20H and 21H.

Bit 2

Enable Video Input.
This bit is used for self-test. Set this bit to "1" for self-testing. The video input to the signature analyzer is disabled. Set this bit to "0" to enable video input for signature analyzer.

Bit 1

Preload Control.
Setting this bit to "0" will preload the Signature Analyzer Result Register (3?5H, Index 20H and 21H) with 0001H. Set this bit to "1" for normal operation.

Bit 0

Enable/Status Bits.
Setting this bit to "1" will enable the signature analyzer to collect signature on video input. This bit indicates the status when read back.
0 = Finished (or not enabled)
1 = Busy

7.7.18 PR1A Shadow Register Control, Read/Write Port = 3?5H, Index = 3DH

Bits (7:4)

Reserved.

Bits 3

I/O Read Select.
0 = Select actual CRTC registers for read
1 = Select shadow CRTC registers for read

Bits (2:0)

Shadow Lock.
Setting Bits 2:0 = "101" will lock all the shadowed register bits. This lock overrides any locks. Please refer to the shadow register description for details.

7.7.19 PR20 Unlock Sequencer Extended Registers, Read/Write Port 3C5H, Index = 6H, (Reset State = Locked)

A value of X1X01XXXX (48H) must be loaded to allow R/W of the Sequencer Extended Registers. When the extended registers are locked, then the Sequencer index will be readable as three bits only. When unlocked, the Sequencer Index reads as six bits.

7.7.20 PR21 Display Configuration Status and Scratch Pad Bits Register, Bits 7:4 Read/Write Bits 3:0 Read Only, Port 3C5H, Index = 7H

This register provides a convenient location for determining the current VGA configuration state. This information is needed for many of the BIOS calls.

BIT	FUNCTION
7:4	Scratch Pad Bits
3	Status of 3C2H Bit 0
2	Status of PR2 Bit 6
1	Status of PR4 Bit 1
0	Status of PR5 Bit 3

Bits (7:4)

Scratch Pad Bits.
Read/write scratch pad for any BIOS status data that may need to be saved. Reset state is "1111".

Bit 3

Status of 3C2H Bit 0.
Reflects the setting of the I/O address select bit in the Miscellaneous Output Register. A "1" indicates CGA (3Dx) addresses have been selected by this read-only bit, while a "0" indicates MDA (3Bx) addresses have been selected.

Bit 2

Status of PR2 Bit 6.
Reflects the setting of the VGA/6845 select bit in PR2 (3CFH Index CH). A "1" indicates 6845 compatibility has been selected by this read-only bit, while a "0" indicates VGA or EGA compatibility has been selected.

Bit 1

Status of PR4 Bit 1.
Reflects the setting of the VGA/EGA select bit in PR4 (3CFH Index EH). A "1" indicates EGA compatibility has been selected by this read-only bit, while a "0" indicates VGA was selected.

Bit 0

Status of PR5 Bit 3.
Reflects the setting of the Analog/TTL status bit in PR5 (3CFH Index FH). A "0" indicates an analog monitor was selected by this read-only bit, while a "1" indicates a TTL-type monitor was selected.

7.7.21 PR22 Scratch Pad Register, Read/Write Port = 3C5H, Index = 8H

Bits (7:0)

Scratch pad bits.

7.7.22 PR23 Scratch Pad Register, Read/Write Port = 3C5H, Index = 9H

Bits (7:0)

Scratch pad bits.

7.7.23 PR30 Memory Interface, Write Buffer and FIFO Control Register, Read/Write Port = 3C4H, Index 10H

This register controls display memory data width and its bandwidth. All of the bits are reset to zero at power on reset.

BIT	FUNCTION
7:6	Write Buffer Control
5	32-bit or 16-bit Memory Data Path
4	Disable 16-bit CPU Interface for Unchain Mode
3	Two-level FIFO
2	Four or Eight-level FIFO
1:0	Display FIFO control

Bits (7:6)

Write Buffer Control.
Bits 6 and 7 determine the depth of the write buffer. PR31 Bit 2 must be set to "1" for these two bits to have any effect.

BITS 7 6	FUNCTION
00	Write buffer is one level deep
01	Write buffer is two levels deep
10	Write buffer is three levels deep
11	Write buffer is four levels deep

Bit 5

Memory Data Path.
When set to "1", the display memory data path becomes 16-bits wide. Otherwise, the data path is 32-bits wide.

Bit 4

0 = Normal conditions
1 = 16-bit interface, unchained mode is disabled. This is for debug only.

Bit 3

Two-level FIFO.
0 = The FIFO is four or eight levels deep, depending on Bit 2 of this register.
1 = The FIFO is two levels deep, regardless of Bit 2.

Bit 2

Four or Eight-Level FIFO.
0 = FIFO set to eight levels deep.
1 = FIFO set to four levels deep.

Bits (1:0)

Display FIFO Control
These two bits can be used to adjust the display memory bandwidth. In general it is recommended that these two bits be set to "01" to accommodate most applications. These bits have no effect in any text mode. They are locked into "00" internally when a text mode is set.

BIT	FUNCTION	
00	FIFO requests for memory cycle when FIFO is:	one level empty
01	FIFO requests for memory cycle when FIFO is:	two levels empty
10	FIFO requests for memory cycle when FIFO is:	three levels empty
11	FIFO requests for memory cycle when FIFO is:	four levels empty

7.7.24 PR31 System Interface Control, Read/Write Port = 3C5H, Index = 11H, Reset State = 00

This register provides the control bits for the system interface. This register should be set during the post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 will be used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY Release Control 1
3	CPU Read RDY Release Control 0
2	Enable Write Buffer
1	Enable 16-bit I/O Attribute Controller
0	Enable 16-bit I/O Operation on CRTC, Sequencer and Graphics Controller

Bit 7

Read/Write Offset Enable.
0 = Normal (Refer to PR0A and PR0B definitions).
1 = The offset register PR0-A will be added to CPU address for read cycles, while PR0-B will be added for write cycles.

Bit 6

Turbo Mode for Blanked Lines.
1 = System performance is improved by 10% by removing extra screen refresh memory cycles on vertical blank.
0 = Normal.

Bit 5

Turbo Mode for Text.
1 = For improved text mode performance.
0 = Normal.

Bits (4:3)

CPU Read RDY Release Controls 1,0.
These two bits set the CPU's RDY timing to be optimized for different system timing. For slower systems, the RDY line may be released earlier because it takes longer to complete the read cycle.

00 = Power on reset condition. RDY is inserted at the end of a CPU memory cycle
01 = RDY is inserted 1MCLK before the end of a CPU memory cycle.
10 = RDY is inserted 2MCLK before the end of a CPU memory cycle.
11 = RDY is inserted 1MCLK after the end of a CPU memory cycle.

For 10 MHz or slower systems, the "01" setting is recommended. For 12 MHz or faster systems, the "11" setting is recommended.

Bit 2

Enable Write Buffer.
1 = Write buffer is enabled. This will greatly reduce the number of wait states for CPU writes to display memory.
0 = Write buffer disabled.

Bit 1

Enable 16-bit I/O Attribute Controller.
If Bit 1 and Bit 0 are both set to "1", then the Attribute Controller (3C0H/3C1H) is configured for 16-bit access. The index is at 3C0H, while the data is at 3C1H, and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for eight-bit cycles. $\overline{IOCS16}$ is asserted for all cycles to 3C0H or 3C1H.

Bit 0

Enable 16-bit I/O Operations.
1 = Enables 16-bit access to the CRTC (3?4H/3?5H), Sequencer (3C4H/3C5H), and Graphics Controller (3CEH/3CFH). The output $\overline{IOCS16}$ will be active for any I/O read or write to these addresses.
0 = The VGA I/O is eight-bits.

7.7.25 PR32 Miscellaneous Control 4, Read/Write Port = 3C5H, 3C5H Index = 12H, Reset State = 00

This register provides control for several different features. Some of these features help to support Genlock of the WD90C30 to another display controller for overlay.

BIT	FUNCTION
7	Enable External Sync Mode
6	Disable Cursor Blink
5	USR1 Function Select
4	USR1 Control
3	USR0 Function Select
2	USR0 Control
1	Allow Read Back in Backward compatible Modes
0	Force Standard CPU Addressing in 132-column Mode

Bit 7

Enable External Sync Mode.
0 = Normal operation mode.
1 = $\overline{EXVID}$ is configured to input external Horizontal Sync, and $\overline{EXPCLK}$ inputs external Vertical Sync. The external $\overline{HSYNC}$ signal also synchronizes the character clock timing. In this configuration, $\overline{EXVID}$ and $\overline{EXPCLK}$ do not control the VID 7:0 and PCLK output buffers, but they are used to genlock the WD90C30 to another display controller.

Bit 6

Disable Cursor Blink.
0 = Blink enabled
1 = The text cursor blink will be disabled, and the cursor will remain on. This option can be used if cursor blink is not desired.

Bit 5

USR1 Function Select.
0 = Causes the USR1 output to reflect the state of Bit 4, which can be used to control new features that the system board designer may wish to add.
1 = The USR1 output is slected by PR35 Bits 5, 4, and 3. See PR35 description.

Bit 4

USR1 Control.
Controls the USR1 output when selected by Bit 5.

Bit 3

USR0 Function Select.
0 = Causes the USR0 output to reflect the state of Bit 2, which can be used to control new features that the system board designer may wish to add.
1 = The USR0 output is selected by PR35 Bits 2, 1, and 0. See PR35 description.

Bit 2

USR0 Control.
Controls the USR0 output when selected by Bit 3.

Bit 1

Read Backward in Compatible Modes.
When set to "1", this bit allows reading of those registers that are not readable in backward compatibility modes. This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0

132-Column Mode.
When set to "1", the special CPU address mapping for page mode font access in 132-column text is set for standard mapping without disturbing the display. This will be used only for special virtual VGA applications.

7.7.26 PR33 DRAM Timing and Zero Wait State Control Register, Read/Write Port = 3C5H, Index = 13H

Bits (7:6)

These two bits control the operation of the $\overline{0WS}$ output pin. $\overline{OWS}$ is disabled if PR31 bit 2 = 0 (Write Buffer is off).

BIT 7	BIT 6	FUNCTION
0	0	$\overline{0WS}$ = 0 if the internal write is buffer-ready.
0	1	$\overline{0WS}$ = 0 if the internal write buffer is ready AND the memory address is decoded.
1	0	$\overline{0WS}$ = 0 if the internal write buffer is ready AND memory address is decoded AND $\overline{MWR}$ = 0.
1	1	$\overline{0WS}$ = 0 if the condition "10" is true OR I/O write to the WD90C30 is occurring.

Bit 5

Reserved

Bits (4:3)

These two bits control the $\overline{CAS}$ timing.

BIT	VALUE	FUNCTION
4-3	00	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1 Mclock + (4-7) ns. $\overline{CAS}$ high is 1 Mclock - (4-7) ns.
4-3	01	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1 Mclock + (8-14) ns. $\overline{CAS}$ high is 1 Mclock - (8-14) ns.
4-3	10	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1.5 Mclocks. $\overline{CAS}$ high is 0.5 Mclocks.
4-3	11	Reserved.

Bit 2

BIT	VALUE	FUNCTION
2	0	$\overline{CAS}$ cycle starts 2.5 Mclocks after $\overline{RAS}$ low.
2	1	$\overline{CAS}$ cycle starts 1.5 Mclocks after $\overline{RAS}$ low.

Bits (1:0)

These two bits control $\overline{RAS}$ precharge. Refer to DRAM timing adjustments in Section 6.0.

BIT	VALUE	FUNCTION
1-0	00	$\overline{RAS}$ high is 2-1/2 mclocks plus a 4-7 ns. delay.
1-0	01	$\overline{RAS}$ high is 3 Mclocks wide.
1-0	10	$\overline{RAS}$ high is 2 Mclocks wide.
1-0	11	$\overline{RAS}$ high is 2-1/2 Mclocks.

7.7.27 PR34 Video Memory Mapping Register, Read/Write Port = 3C5H, Index = 14H

Bits (7:0)

BITS	FUNCTION
7-4	Reserved.
3-0	These four bits are compared with the CPU address A_[23:20] as part of the video memory address decoding. This allows the VGA to be mapped into any 1 Mbyte CPU memory space. This register will not affect the $\overline{EBROM}$ and $\overline{ROM16}$ decoding. $\overline{EBROM}$ and $\overline{ROM16}$ will still decode at A_[23:20] = 0H. Used with the correct setting of PR1, Bits 5 and 4, this register supports virtual VGA applications. These four bits are set to "0" at power-on reset.

7.7.28 PR35 USR0, USR1 Output Select Register, Read/Write Port = 3C5H, Index = 15H

This register determines which internal signals can be observed through USR0 and USR1 output pins. This is for debug purposes and may be useful for using internal signals to control external functions. PR35, Bits 5 and 3, must be set to "1" for this register to have any effect.

Bits (7:6)

Reserved.

Bits (5:3)

5, 4, 3	USR1 =
0 0 0	"1", if WD90C30 is fetching fonts from DRAM
0 0 1	"1", if WD90C30 is fetching graphics data from DRAM
0 1 0	"1", if the internal write buffer is ready
0 1 1	"1", if a CPU write cycle is occurring
1 0 0	"0", if a CPU write cycle is not caused by write buffer
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

Bits (2:0)

2, 1, 0	USR0 =
0 0 0	"1", if I/O address is decoded
0 0 1	"1", if WD90C30 is fetching character attributes from DRAM
0 1 0	"0", if the internal write buffer is not empty
0 1 1	"1", if CPU read cycle is occurring
1 0 0	"0", if a write buffer cycle is occurring
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

7.8 INTERNAL I/O PORTS

7.8.1 AT Mode Setup, Enable Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7:5	Unused
4	Setup
3	Enable I/O and Memory
2:0	External BIOS ROM Page Select

Bits (7:5)

Unused.

Bit 4

Setup.
Puts WD90C30 into setup mode where only I/O Port 102H is accessible.

Bit 3

Enable I/O and Memory Accesses.

Bits (2:0)

BIOS ROM Page Select.
On I/O accesses to 46E8H, $\overline{\text{EBROM}}$ becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0. The WD90C30 also provides an alternative Port 3C3H instead of Port 46E8H. If a pull-down resistor is connected to MD(9) during power on reset (CNF9 = 0), then Port 3C3H will be decoded instead of Port 46E8H to support the same functions described above. Otherwise, Port 46E8H is selected and decoded.

7.8.2 Setup Mode Video Enable (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7:1	Unused
0	Wakeup VGA

Bits (7:1)

Unused.

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower three address bits are decoded for this port and WD90C30 must be in Setup mode. VGA Enable Sleep bit or Programmable Option Select (POS) Register 102H Bit 0 is used to awaken the WD90C30 after power on in the MCA and AT mode. To enter the set up mode in AT bus applications, Bit 4 of the partially decoded internal I/O Port 46E8H is set to "1" before accessing the I/O Port 102H. In MCA mode, when the VGASETUP ($\overline{\text{EIO}}$) signal pin is active low, the WD90C30 is in setup mode and Port 102H can be accessed.

7.9 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C30. However, the $\overline{\text{WPLT}}$ and $\overline{\text{RPLT}}$ signals required by the RAMDAC are provided by the WD90C30. Setting PR(16) Bit 0 to a "1" forces $\overline{\text{WPLT}}$ to a high level disabling I/O writes to the RAMDAC. Normally, the $\overline{\text{WPLT}}$ and $\overline{\text{RPLT}}$ signals to the RAMDAC are generated when the following I/O ports are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL Address Port (Write)	Read/Write Port
3C7H	PEL Address Port (Read)	Read Only Port
*3C7H	*DAC State (Read Only)	* If Bits 0/1 = 1, DAC in read operation. When Bits 0/1 = 0, DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL Mask (Read/Write)	Not to be written by application code or color look-up table will be changed.
3C9H	PEL Data Register (Read/Write)	Three successive read/write bytes.

* This port is internal to the WD90C30.

TABLE 17. VIDEO RAMDAC PORTS

7.10 WD90C30 CONFIGURATION REGISTER BITS CNF(18:0)

Memory Data Lines (18:0) are used to input configuration data at power-on reset (RST) by pull-up or pull-down resistors. This configuration data then sets the bits in internal registers. Some of these bits can then be changed by software, while some are in non-writable registers. The non-writable bits set features such as bus type which are not changed after power-on. All MD(18:0) are internally pulled up by 50 ohm resistors. The following table lists the non-writable configuration bits.

BIT	FUNCTION
18	Enable $\overline{\text{ROM16}}$ as $\overline{\text{EXBLANK}}$ input
17	
16	64K by 16 or 256 K by 4 DRAM select
15 -12	EGA Switches
11	A23 - A20 Connection Select
9	46E8H/3C3H Select
8	Display Status
7 - 4	General Purpose Status
3	Video Clock Source Control
2	AT/MCA Bus Select

CNF(18)

A 4.7K pull-down resistor on Pin MD(18) sets CNF(18) = 0. Otherwise the internal pull-up will set CNF(18) = 1.

0 = $\overline{\text{ROM16}}$ configured as $\overline{\text{EXBLANK}}$ input.

1 = Normal $\overline{\text{ROM16}}$ operation. $\overline{\text{ROM16}}$ is an output.

CNF(16)

A 4.7K pull-down resistor on pin MD(16) sets CNF(16) = 0. Otherwise, the internal pull-up will set CNF(16) = 1.

0 = WD90C30 is interfacing with a 64K by 16 DRAM.

1 = WD90C30 is interfacing with a 256K by 4 or 256K by 16 DRAM.

CNF(15:12)

EGA configuration switches SW4-SW1.
Pulling up MD(15:12) causes PR11(7:4) to be latched high. Pulling down MD(15:12) causes these bits to be latched LOW. PR11(7:4) are writable bits. These bits can be read as Bit 4 of Port 3C2H (as on a standard EGA) if the EGA compatibility bit [PR4(1)] has been set to "1". Selection of which bit to read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2H, as follows.

WRITE		READ
3C2 Bit 3	3C2 Bit 2	3C2 Bit 4
0	0	PR11(7) [= EGA SW4]
0	1	PR11(6) [= EGA SW3]
1	0	PR11(5) [= EGA SW2]
1	1	PR11(4) [= EGA SW1]

CNF(11)

A 4.7K pull-down resistor on the Pin MD8 sets CNF(11) = 0. The pins A(22:20) should then be connected to the AT bus signals LA(19:17), unlatched CPU address. The pin A23 should be connected to the NOR of AT bus signals LA(23:20). The pins A(19:17) should be connected to AT bus SA(19:17), latched CPU address. This will allow the WD90C30 to directly drive MEMCS16 in AT bus which requires decoding of the early unlatched address LA(23:17). An external NOR is required to decode LA(23:20).

If there is no pull-down resistor on MD8, the CNF(11) will be set to "1" by the internal pull-up. Pins A(23:17) should be connected to AT bus signals LA(23:17). LA(23:17) are internally latched by ALE signal.

CNF(10)

A 4.7K pull-down on Pin MD10 sets CNF(10) = PR1(1) = 1. Upon power-up, the pin ROM16 is enabled for 16-bit BIOS ROM decoding. Otherwise, the internal pull-up will set CNF(10) = PR1(1) = 0. To enable the 16-bit BIOS, PR1(1) must be set to "1" by writing to Port 3CFH (Index 0BH) bit 1 and at the same time the CNF(1) must be "1". This bit is read/write at PR1(1).

CNF(9)

A 4.7K pull-down on Pin MD9 sets CNF(9) = 0. Then Port 03C3H will be selected as the VGA setup and enable register instead of Port 46E8H in the AT interface. Otherwise, the internal pull-up will set CNF(9) = 1. Port 46E8H will be selected as VGA setup and enable register. This bit has no effect in Micro Channel applications.

CNF(8)

Analog/TTL Display Status Bit.
Bit CNF(8) is latched internally at power-on-reset from memory data bus Pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as Bit 3 of PR5 (3CF.0FH). Also, CNF(8) is unaffected by writing to PR5 (3CF.0FH). Suggested implementation is:

0 = Analog (VGA - compatible) display is attached
1 = TTL (EGA-compatible) display is attached.

CNF(7:4)

General Purpose Status Bits.
Bits CNF(7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD(7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0FH) positions (7:4). These bits are unaffected by writing to PR5(3CF.0FH). Pulling down MD(7:4) causes CNF(7:4) to be latched high.

CNF(3)

Video Clock Source Control.
This bit cannot be written or read as I/O port. Pulling up MD(3) causes CNF(3) to be latched high. It configures WD90C30 pins VCLK1 and VCLK2 as inputs or outputs.

0 = For inputs.
1 = For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip, during I/O writes to Port 3C2H. This load pulse may be inhibited by setting PR11(2) = 1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK1 and VCLK2 outputs are equal to Bits 2 and 3 of the Miscellaneous Output Register at 3C2H when PR15 Bit 5 is set to "1".

CNF (2)

Bus Architecture Select.
This bit cannot be written or read as I/O. Pulling down MD(2) causes CNF(2) to be latched low.

0 = Micro Channel architecture
1 = AT BUS architecture

Selecting CNF(2) will change pinout definition between AT BUS and Micro Channel bus. (See Signal Description.)

PC-AT BUS	I/O	MICRO CHANNEL	I/O
MEMCS16	OUT	$\overline{\text{CDDS16}}$	OUT
$\overline{\text{ROM16}}$	OUT	$\overline{\text{CSFB}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0H	IN
$\overline{\text{MRD}}$	IN	M/$\overline{\text{IO}}$	IN
$\overline{\text{MWR}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	$\overline{\text{CMD}}$	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
$\overline{\text{IOCS16}}$	OUT	$\overline{\text{CDSETUP}}$	OUT

CNF (1)

ROM Configuration.
When set to "0", the WD90C30's data bus buffer controls are configured for one ROM (eight bits). An internal pull-up on MD(1) sets this bit to "0" at power-on-reset.

0 = PR1(1) can not be set high. This bit can not be written or read.

1 = The WD90C30's data bus buffer controls are configured for 16-bits (as with two ROMs). Setting CNF(1) to 1 enables the $\overline{\text{HTL}}$ output pin. With an 8-bit system interface, address bit A(0) = 0, selects the even ROM and A(0)=1 selects the odd ROM. With a 16-bit system interface, CNF(1) and PR1(1) must be set to one to enable $\overline{\text{ROM16}}$.

CNF (0)

BIOS ROM Mapping.
If set to "1", the BIOS ROM is mapped out. An internal pullup resistor on MD(0) sets this bit to 0 at power-on reset. An external 4.7 Kohm pull-down resistor may be used to set this bit to "1" on power-on-reset.

This bit is read/write at PR1(0).

A.0 APPENDIX A - EGA MODE

A.1 EGA MODE ENTRY

For the register definitions that have not changed from the VGA modes, refer to the VGA description. Only the differences between the VGA and EGA registers are briefly described in this section. Also, refer to the prior section for VGA mode details. "Not Used" bits should be set to "0" unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are not covered in this procedure. These steps are briefly defined to outline the EGA mode entry.

- Load Configuration register Bit 8. Select logic "0" for a VGA-compatible PS/2 display or logic "1" for an EGA-compatible TTL monitor by using the appropriate pull-up or pull-down resistor on MD(11). (A pull-up resistor on MD11 causes CNF(8) to be latched with logic "0" for analog PS/2 compatible displays.) This status information signifies the type of monitor attached to the system and is available to the BIOS or application.
- Unlock all the PR registers.
- Program PR2(6) to "0" for EGA mode.
- Set PR4 Bit 1 to logic "1" for EGA compatibility.
- Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on Pins MD(15:12). (A pull-up resistor causes logic "1" to be latched after power-on-reset.)
- The EGA switch setting may then be read from PR11(7:4) at I/O Port 3C2H Bit 4.
- If EGA mode is to be emulated on an IBM PS/2 analog display, follow the suggested steps listed below:
  Initialize all the registers.
  Lock CRT controller registers.
  Force clock control rate of the CRT controller.
  - Set EGA emulation mode by programming:
    PR11(3)=1; Set EGA emulation on PS/2 type display
    PR14(6)=1; Vertical double scan
    PR11(2)=1; Lock clock select
    PR11(0)=1; Lock 8/9 dot timing.
    PR14(7)=1; Enable IRQ (optional).
  - Lock the PR registers PRO through PR5 and PR10 through PR17.
  - Read protect PR registers.
- When EGA is required on a TTL monitor, the suggested steps are:
  - Initialize all the registers.
  - Set EGA TTL mode by programming:
    PR11(3)=0; EGA TTL
    PR14(7)=1; Enable IRQ
    PR15(6)=1; Set Low Clock
    PR14(7)=1; Enable IRQ
  - Lock PR registers PRO through PR5 and PR10 through PR17.
  - Read protect PR registers.

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlight all the EGA mode registers.

A.2 GENERAL REGISTERS

Only the general registers and the bit definitions that differ between the VGA and EGA are addressed. Their EGA mode bit definitions are provided.

A.2.1 Miscellaneous Output Register Write, Port = 3C2H

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Not used.

REGISTERS	EGA	I/O PORT HEX
General Registers:		
Miscellaneous Output Register	WO	3C2
Input Status Register 0	RO	3C2
Input Status Register 1	RO	3?A
Feature Control Register	WO	3?A
Sequencer Registers:		
Sequencer Index Register	WO	3C4
Sequencer Data Register	WO	3C5
CRT Controller Registers:		
Index Register	WO	3?4
CRT Controller Data Register, except the following:	WO	3?5
Start Address High (Index=0CH)	RW	3?5
Start Address Low (Index=0DH)	RW	3?5
Cursor Location High (Index=0EH)	RW	3?5
Cursor Location Low (Index=0FH)	RW	3?5
Light Pen High, (Index=10H)	R	3?5
Light Pen Low, (Index=11H)	R	3?5
Graphics Controller Registers:		
Index Register	WO	3CE
Other Graphics Register	WO	3CF
Attribute Controller Registers:		
Index Register	WO	3CO*
Attribute Controller Data Register	WO	3CO*

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All Register addresses are in hex.
3. "?" = "B" in Monochrome modes or "D" in Color modes.

TABLE 18. EGA REGISTERS SUMMARY

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 MHz clock (VCLK0) is selected.
0	1	16.257 MHz clock (VCLK1) is selected if Configuration Register Bit 3 is "0".
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is "0".
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is "0".

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

A.2.2 Input Status Register 0, Read Port = 3C2H

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not used.

Bit 4

EGA: The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to "1".

Bits (3:0)

EGA: Not used = 1.

A.2.3 Input Status Register 1, Read Port = 3?AH

Bit 7

EGA: Not used.

Bit 6

EGA: Not used = 1.

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: Not used = 1.

Bit 1

EGA: Not used.

Bit 0

EGA: Same as Input Status Register 1 Bit 0 definition in the VGA section.

A.2.4 Feature Control Register, Write Port = 3?AH

Bits (7:0)

EGA: Not used.

A.3 SEQUENCER REGISTERS, PORT = 3C5H

A.3.1 Clocking Mode Register, Index = 01H

Bits (7:4)

EGA: Not Used.

Bits (3:2)

EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1

EGA: Set to zero.

Bit 0

EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

A.3.2 Character Map Select Register, Index = 03H

Bits (7:4)

EGA: Not used.

Bits (3:2)

EGA: Character Map Select A.

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

Bits (1:0)

EGA: Character Map Select B.

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

NOTE:
Character Map selection from Plane 2 is determined by Bit 3 of the attribute code.

A.3.3 Memory Mode Register, Index = 04H

Bits (7:3)

EGA: Not used.

Bits (2:1)

EGA: Identical to Memory Mode Register Bits (2:1) definition in the VGA section.

Bit 0

EGA: Alpha Mode Bit.
A logic "1" shows that Alpha mode is active and character map selection is enabled. A logic "0" disables Alpha modes and enables non-Alpha modes.

A.4 CRT CONTROLLER REGISTERS, PORT = 3?5H

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. Also, "?" implies that a register is mapped into either 3B5H or 3D5H, for Monochrome or Color display modes, respectively.

A.4.1 Index Register, Port = 3?4H

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Five bits point to the CRT Registers Address Index where the data is to be written.

A.4.2 Horizontal Total Register, Index = 00H

Bits (7:0)

EGA: Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

A.4.3 End Horizontal Blanking Register, Index = 03H

Bit 7

EGA: Not used.

Bits (6:5)

EGA: They define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

A.4.4 End Horizontal Retrace Register, Index = 05H

Bit 7

EGA: This bit defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

A.4.5 Vertical Total Register, Index = 06H

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

A.4.6 CRT Controller Overflow Register, Index = 08H

Bits (7:5)

EGA: Not used.

Bits (4:0)

Identical to CRT Controller Overflow Register Bits (4:0) definitions in the VGA section.

A.4.7 Maximum Scan Line Register, Index = 09H

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as maximum Scan Line Register Bits (4:0) definition in the VGA section.

A.4.8 Cursor Start Register, Index = 0AH

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

A.4.9 Cursor End Register, Index = 0BH

Bit 7

EGA: Not used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

A.4.10 Vertical Retrace Start Register, Index = 10H - Write

(Light Pen High register, Index = 10H - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

A.4.11 Vertical Retrace End Register, Index = 11H - Write

(Light Pen Low register, Index = 11H - Read)

Bits (7:6)

EGA: Not used.

Bit 5

EGA: This bit enables the IRQ output buffer control if logic "0" is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic "1", the IRQ buffer is switched to a high impedance state.

Bit 4

EGA: When programmed to logic "0", the IRQ latch is reset and cleared to "0" if Bit 5 = 0. If it is logic '1", the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

A.4.12 Underline Location Register, Index = 14H

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

A.4.13 End Vertical Blanking Register, Index = 16H

Bits (7:5)
EGA: Not used.

Bits (4:0)

EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

A.4.14 Mode Control Register, Index = 17H

Bits (7:5)

EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4

EGA: Not used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.5 GRAPHICS CONTROLLER REGISTERS, PORT = 3CFH

A.5.1 Read Map Select Register, Index = 04H

Bits (7:3)

EGA: Not Used.

Bits (2:0)

EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

BIT 2	BIT 1	BIT 0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

A.5.2 Mode Register, Index = 05H

Bit (7:6)

EGA: Not used.

Bits (5:2)

EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)

EGA: Binary coded write bits define the write modes per table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to VGA section
0	1	Write mode 1 - Refer to VGA section
1	0	Write mode 2 - Refer to VGA section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

A.6 ATTRIBUTE CONTROLLER REGISTERS, PORTS = 3C0H/3C1H

A.6.1 Palette Registers, Index = 00H through 0FH

BIT	FUNCTION
7:6	Not used
5:0	Dynamic color selection

Bits (7:6)

EGA: Not used.

Bits (5:0)

EGA: Dynamic color selection. Logic "0" = Color deselection, and Logic "1" = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

A.6.2 Mode Control Register, Index = 10H

BIT	FUNCTION
7:4	Not used
3:0	Same as Mode Control in VGA section

Bits (7:4)

EGA: Not used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.6.3 Overscan Color Register, Index = 11H

BIT	FUNCTION
7:6	Not used
5:0	Overscan color for border

Bits (7:6)

EGA: Not used.

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic "0". The border color is defined by the color table for the Palette registers shown above.

A.6.4 Color Plane Enable Register, Index = 12H

BIT	FUNCTION
7:6	Same as Color Plane Enable - VGA
5:4	Video Status Multiplexer
3:0	Same as Color Plane Enable - VGA

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer as shown below:

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2(Red)	VID 0 (Blue)
0	1	VID 5(SRed)	VID 4 (SGreen)
1	0	VID 3(SBlue)	VID 1 (Green)
1	1	VID 5(SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

A.6.5 Horizontal PEL Panning Register, Index = 13H

BIT	FUNCTION
7:4	Not used
3:0	Horizontal left shift of the video data in number of pixels.

Bits (7:4)

EGA: Not Used.

Bits (3:0)

EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, (nine dots/character) image can be shifted by nine pixels. For all other graphics or alpha numeric modes, a maximum left shift of eight pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

B .0 APPENDIX B - WD90C30 INTERFACES

The WD90C30 applications section is divided into various interfaces: processor (AT or Micro Channel mode), video memory, RAMDAC, monitor, and clock. The description and block diagrams are generic. No attempt is made to present schematic level details. Currently available application notes and technical briefs at the end of this data book will supplement the information provided in this section.

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B.1 WD90C30 INTERFACES

Figure 13 highlights the WD90C30 interfaces.

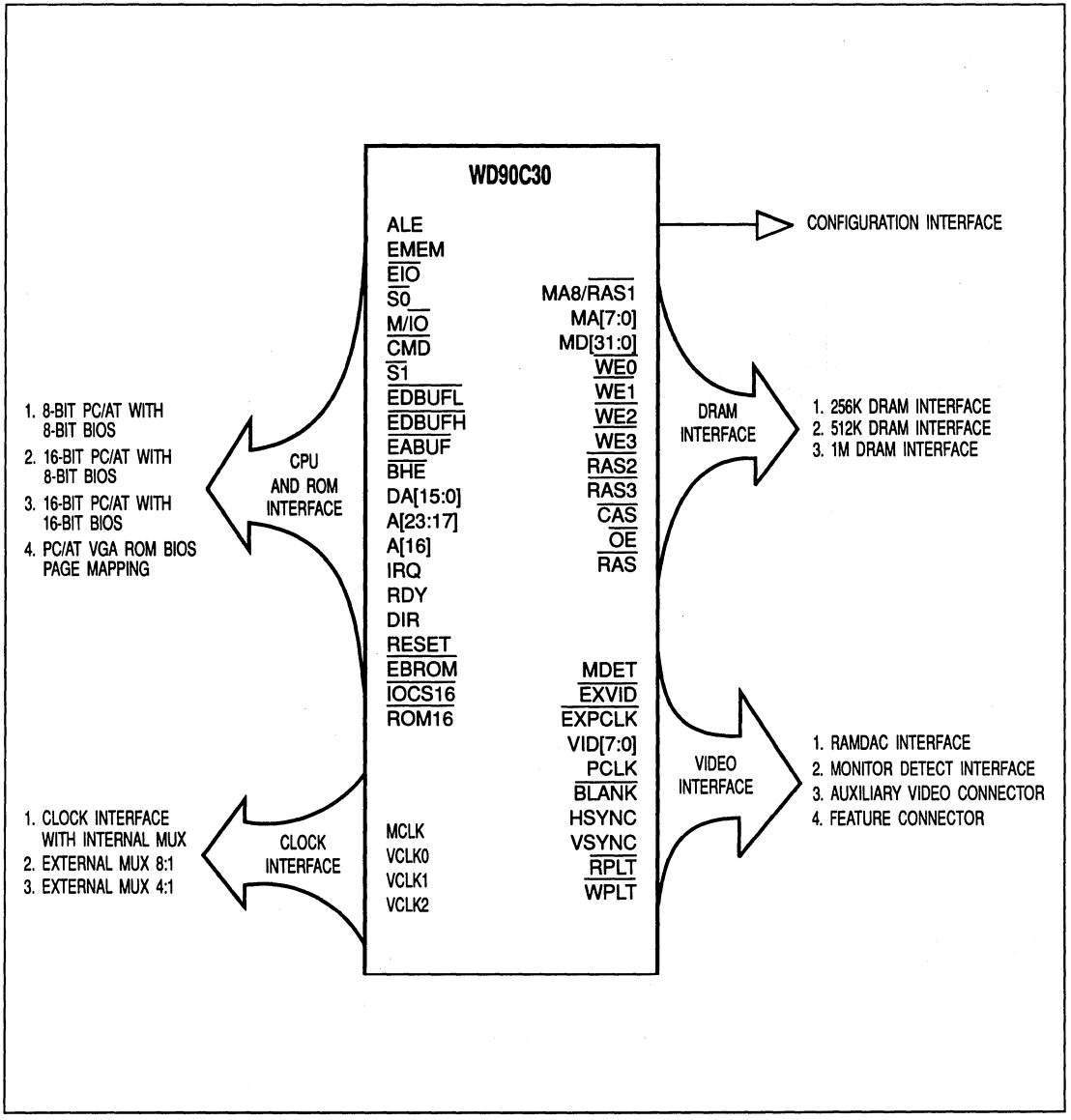

FIGURE 13. WD90C30 INTERFACES

B.2 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 14 shows a block diagram of the WD90C30 with eight-bit PC/AT interface using eight-bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM.

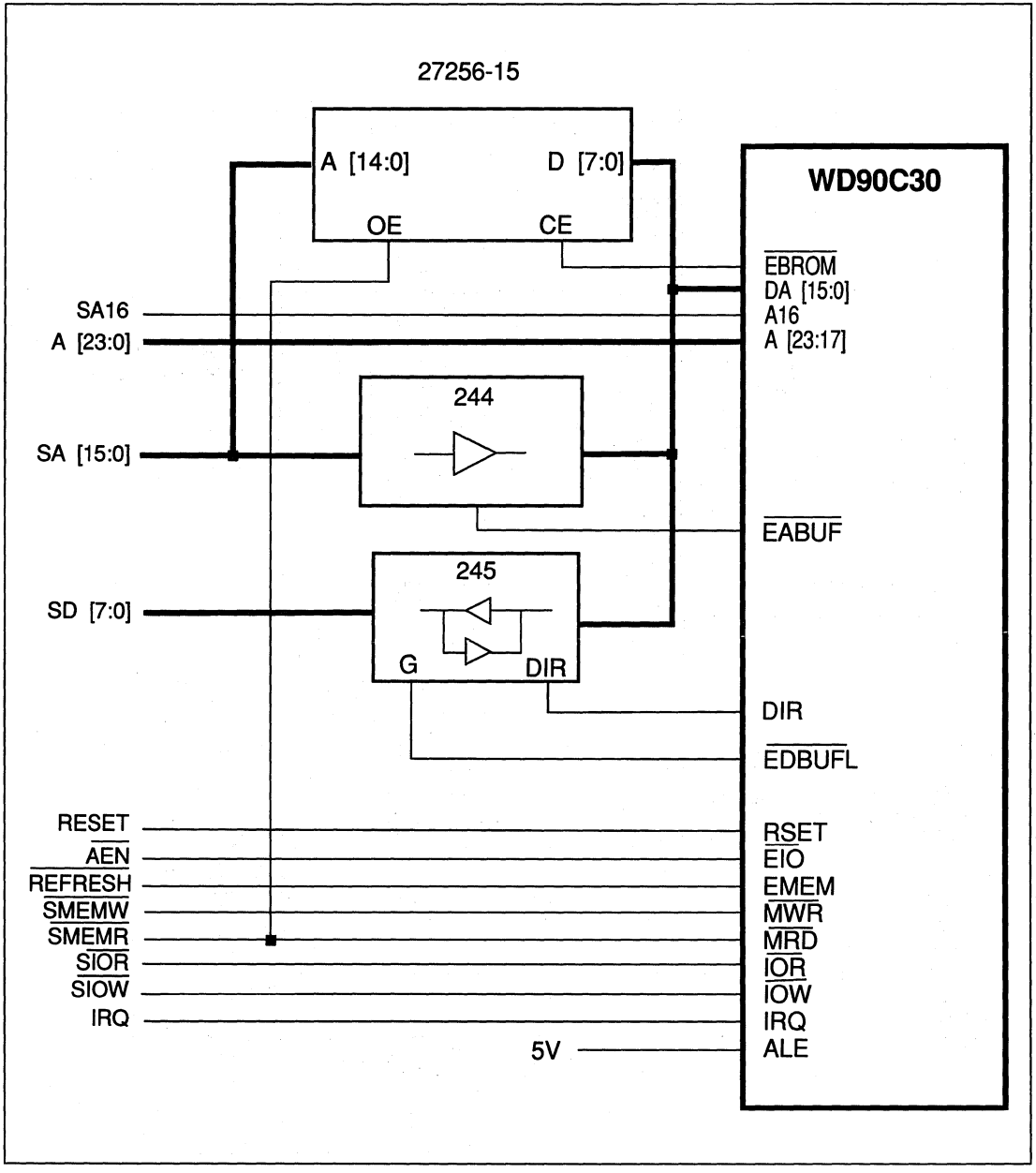

FIGURE 14. 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

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B.3 16-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 15 illustrates 16-bit PC/AT interface with an eight-bit BIOS using WD90C30. For 386 systems, the processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers and BIOS ROM are also shown.

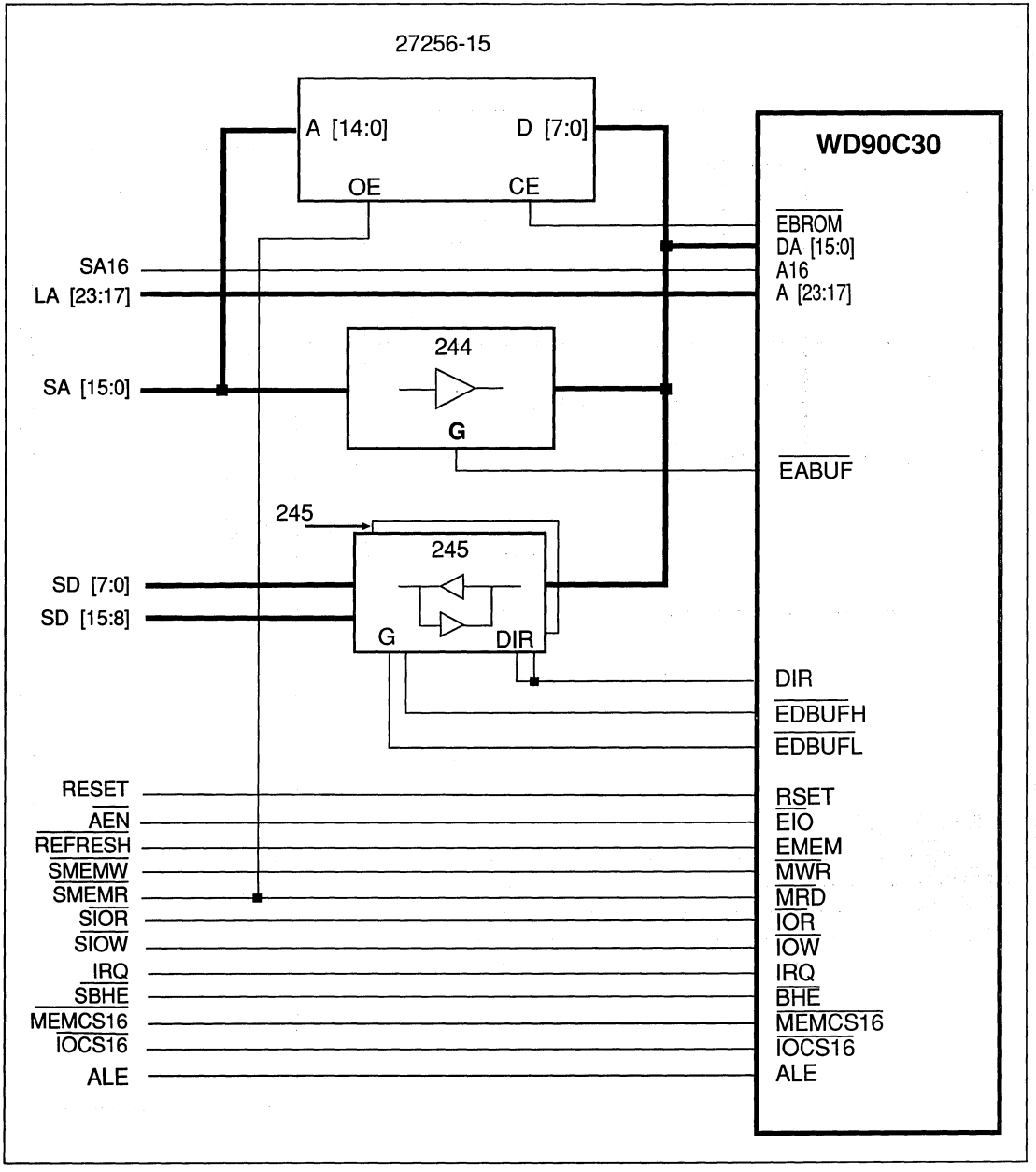

FIGURE 15. 16-BIT PC AT INTERFACE WITH 8-BIT BIOS

B.4 16-BIT PC AT INTERFACE WITH 16-BIT BIOS

Figure 16 describes a 16-bit PC/AT interface with 16-bit BIOS ROM implementation using the WD90C30. The system data bus SD(15:0), address and data bus buffers are presented. Also, MEMCS16 implementation is limited to certain bus speeds since SA15 and SA16 are used for the 16-bit BIOS. Refer to Figure 18 for 286-based systems.

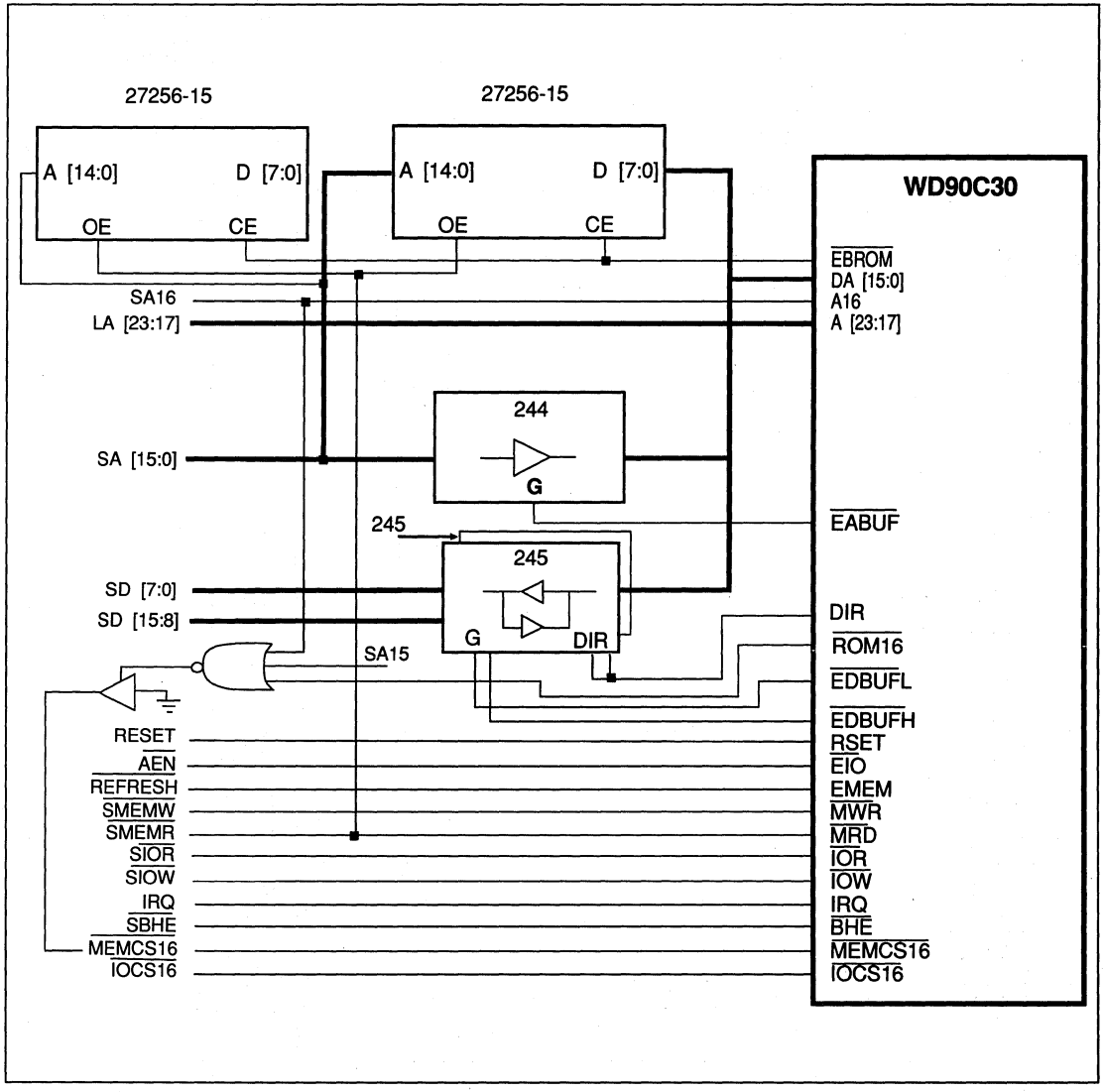

FIGURE 16. 16-BIT PC AT INTERFACE WITH 16-BIT BIOS

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B.5 16-BIT MICRO CHANNEL

Figure 17 illustrates the WD90C30 and 16-bit Micro Channel interface. 3C3.D0H is output of Port 3C3H Bit 0 VGA Subsystem Enable Register.

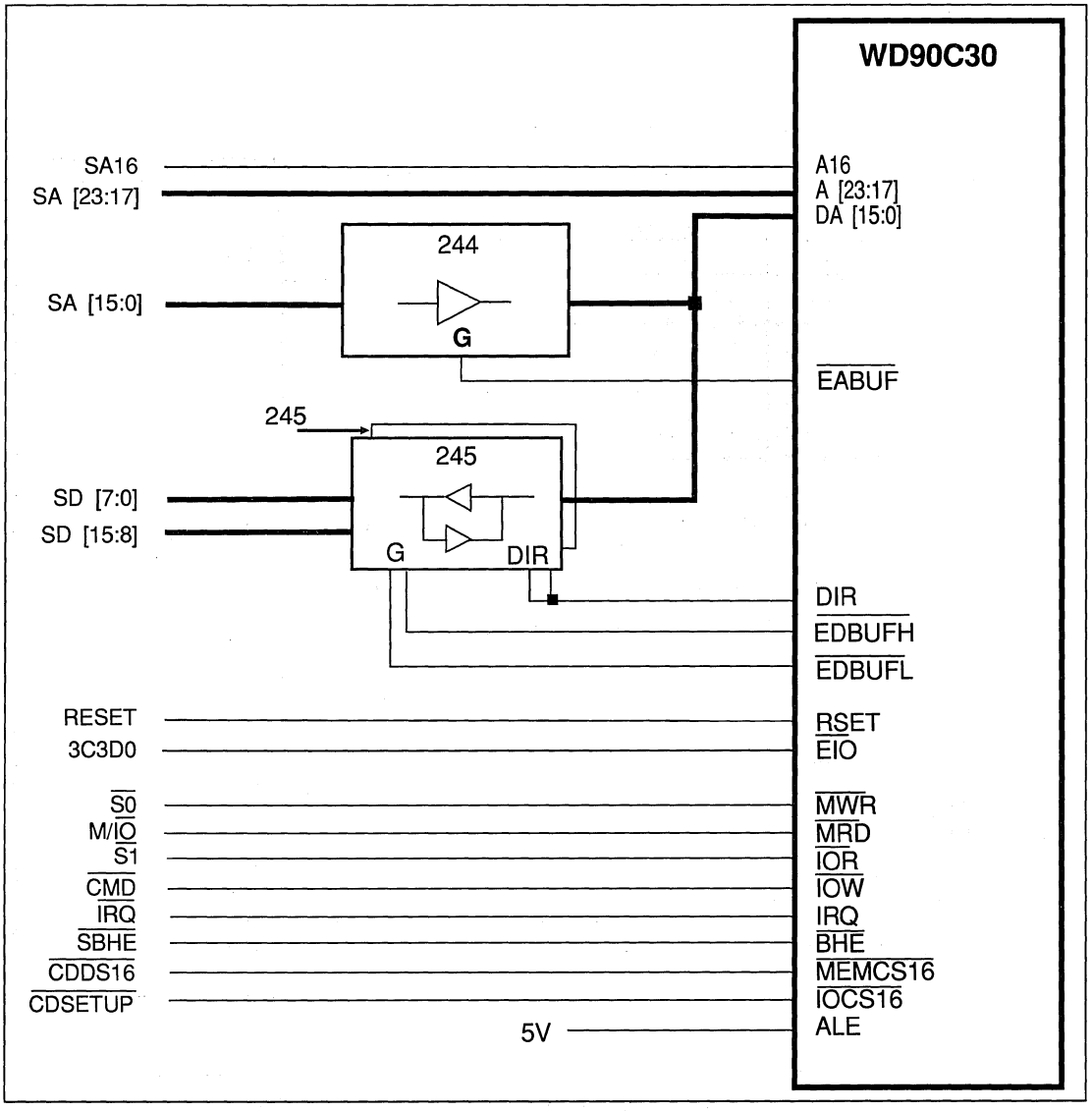
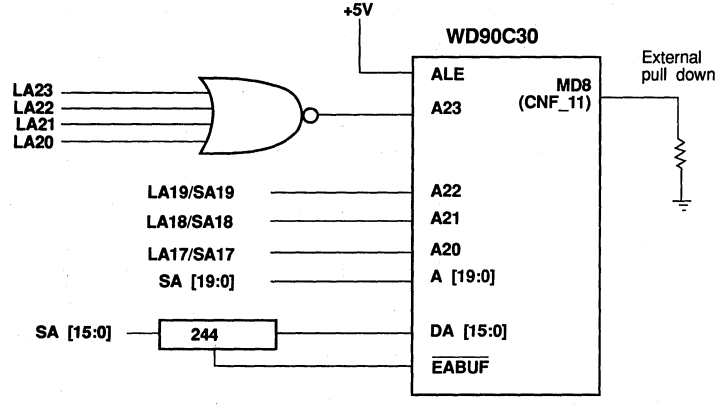


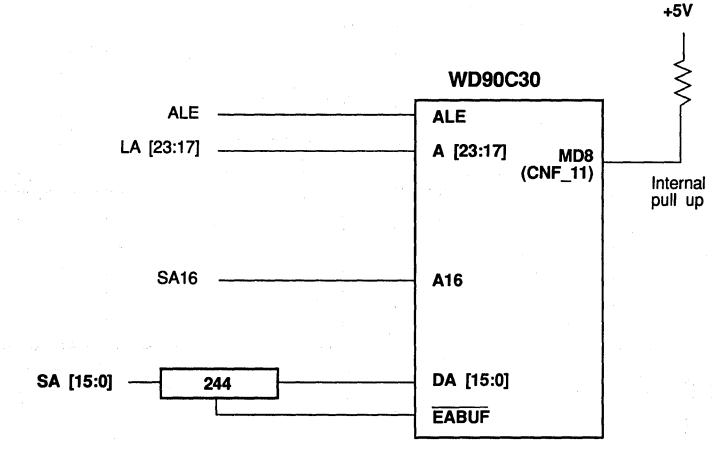
FIGURE 17. 16-BIT MICRO CHANNEL INTERFACE

B.6 WD90C30 INTERFACE FOR 286 OR 386 BASED SYSTEMS

For systems that do not meet the hold time of LA address valid from the falling edge of MEMR or MEMW, pull MD8 down and connect LA addresses and SA addresses as shown in the upper half of Figure 18. This applies to most 286 systems. Otherwise, connect LA addresses and SA addresses as shown in the lower half of Figure 18. This applies to most 386 systems.



Note: MD8 (CNF_11 is pulled down at power-on-reset. This configuration is recommended for interfacing with 8-bit and 16-bit AT buses. For an 8-bit interface, A23 should be connected to SA [19:17] on the AT bus. For a 16-bit interface, LA [23:17] must be connected to generate MEMCS16.



Note: MD8 (CNF_11) is pulled up internally at power-on-reset. This configuration is recommended for interface with a 16-bit AT bus only. LA [23:17] is internally latched by ALE.

FIGURE 18. WD90C30 INTERFACE FOR 286 OR 386-BASED SYSTEMS

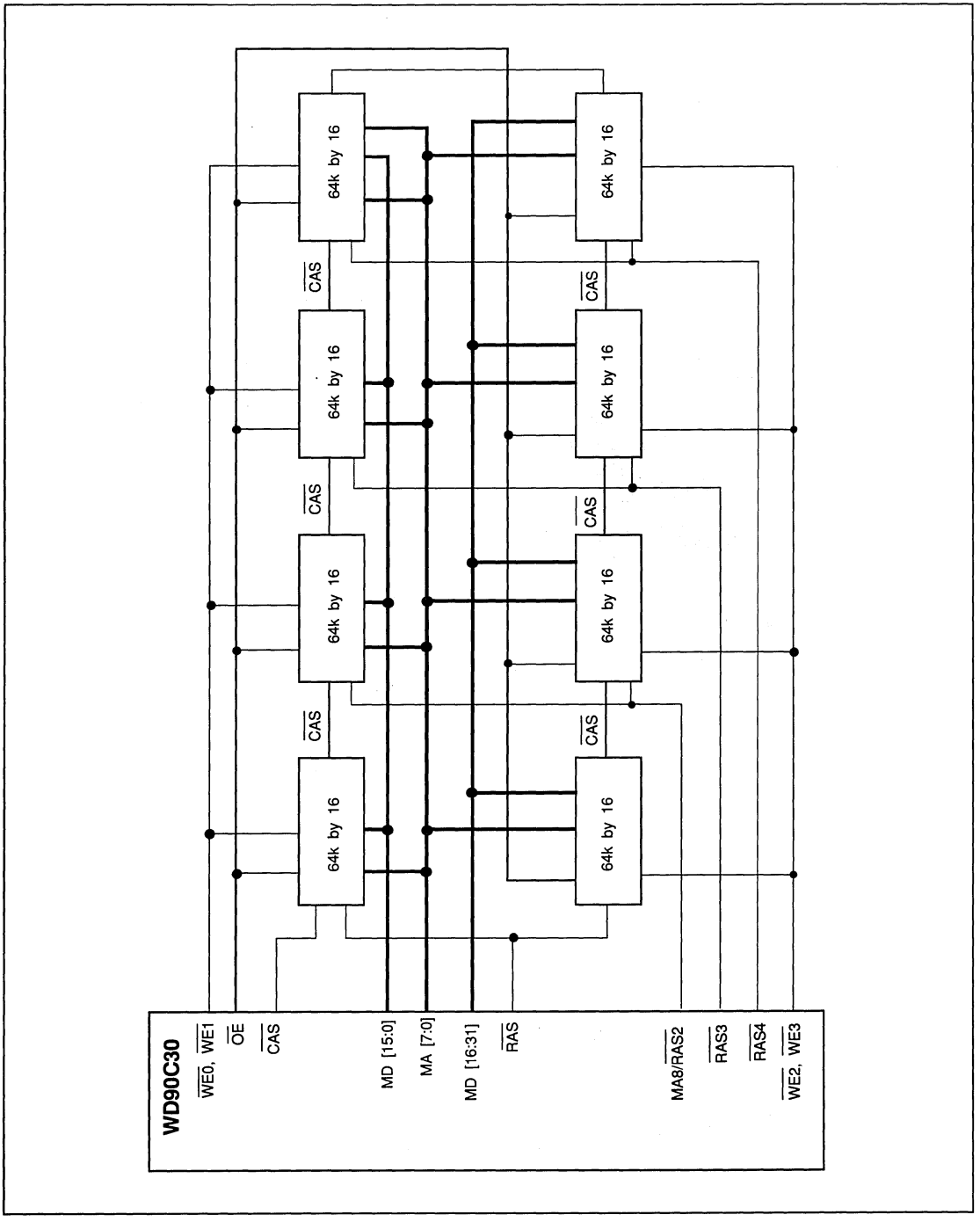
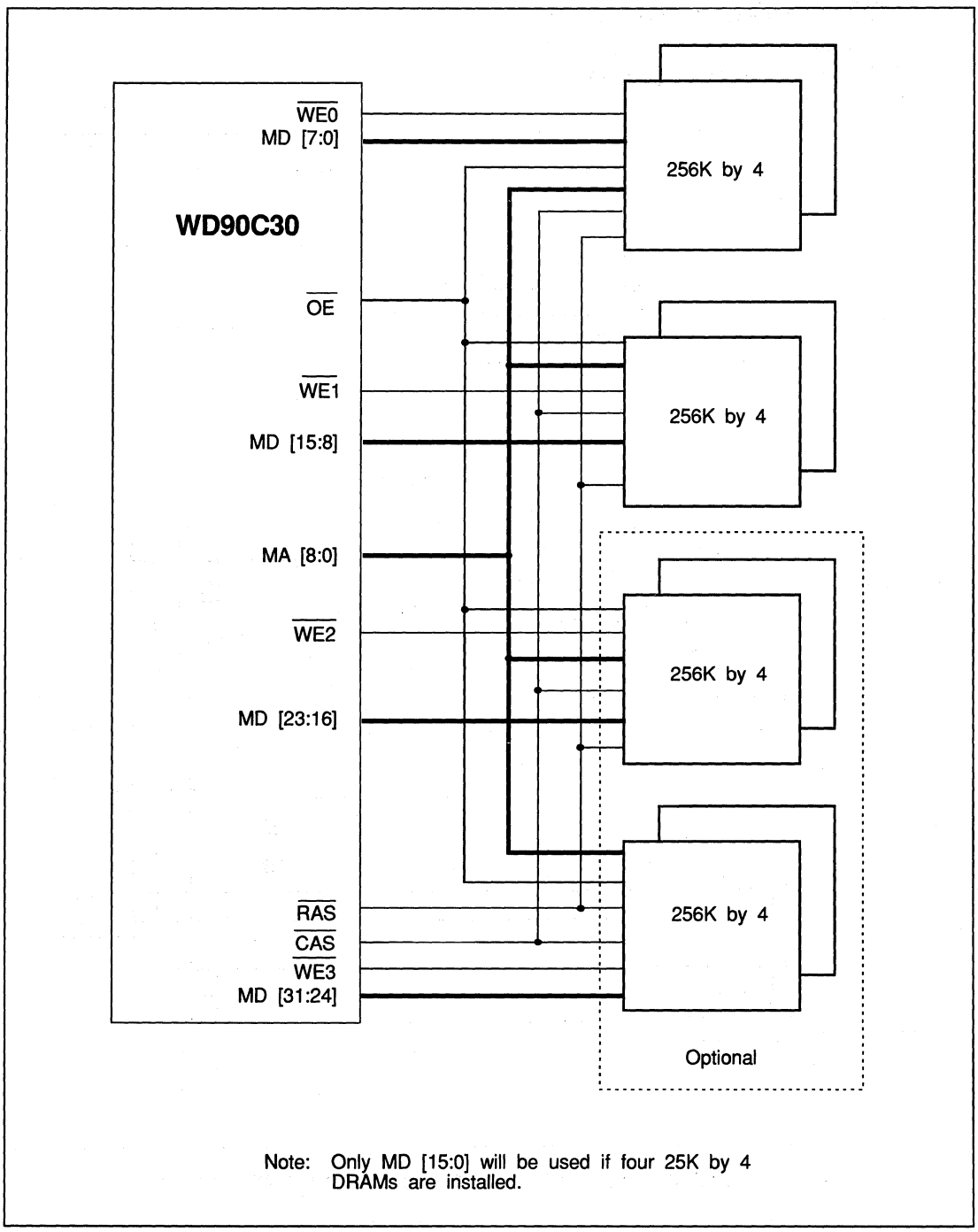


FIGURE 19. TWO, FOUR OR EIGHT 64K BY 16 DRAM INTERFACE



Note: Only MD [15:0] will be used if four 25K by 4 DRAMs are installed.

FIGURE 20. FOUR OR EIGHT 256K BY 4 DRAM INTERFACE

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B.7 WD90C30 WITH RAMDAC INTERFACE

Figure 21 illustrates the WD90C30 and RAMDAC (WD90C50) interface block diagram for analog monitors.

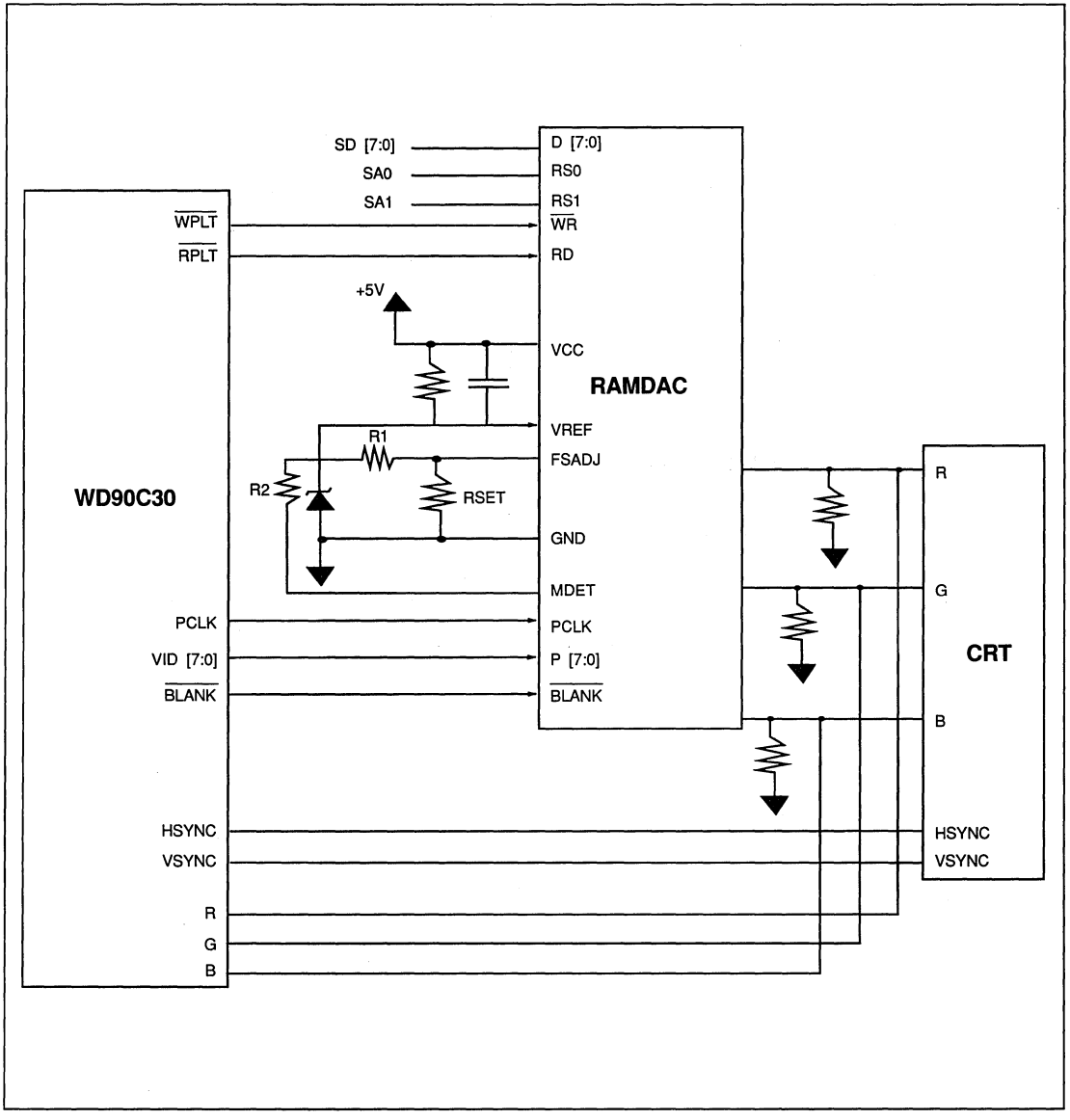

FIGURE 21. WD90C30 WITH RAMDAC INTERFACE

B.8 WD90C30 AND TTL MONITOR CONNECTIONS

Figure 22 illustrates the WD90C30 and TTL monitor connections

NOTE:

- VGA/TTL switch may be used to disable HSYNC and VSYNC for analog or TTL Video connector.
- MD(15:12) may also be connected as the EGA switches if desired. See PR Register and Pinout sections for more detail.
- For AT applications using the WD90C30, install the IRQ9 resistor.
- Transistor 2N2222A is used to emulate a monochrome and color display connection.

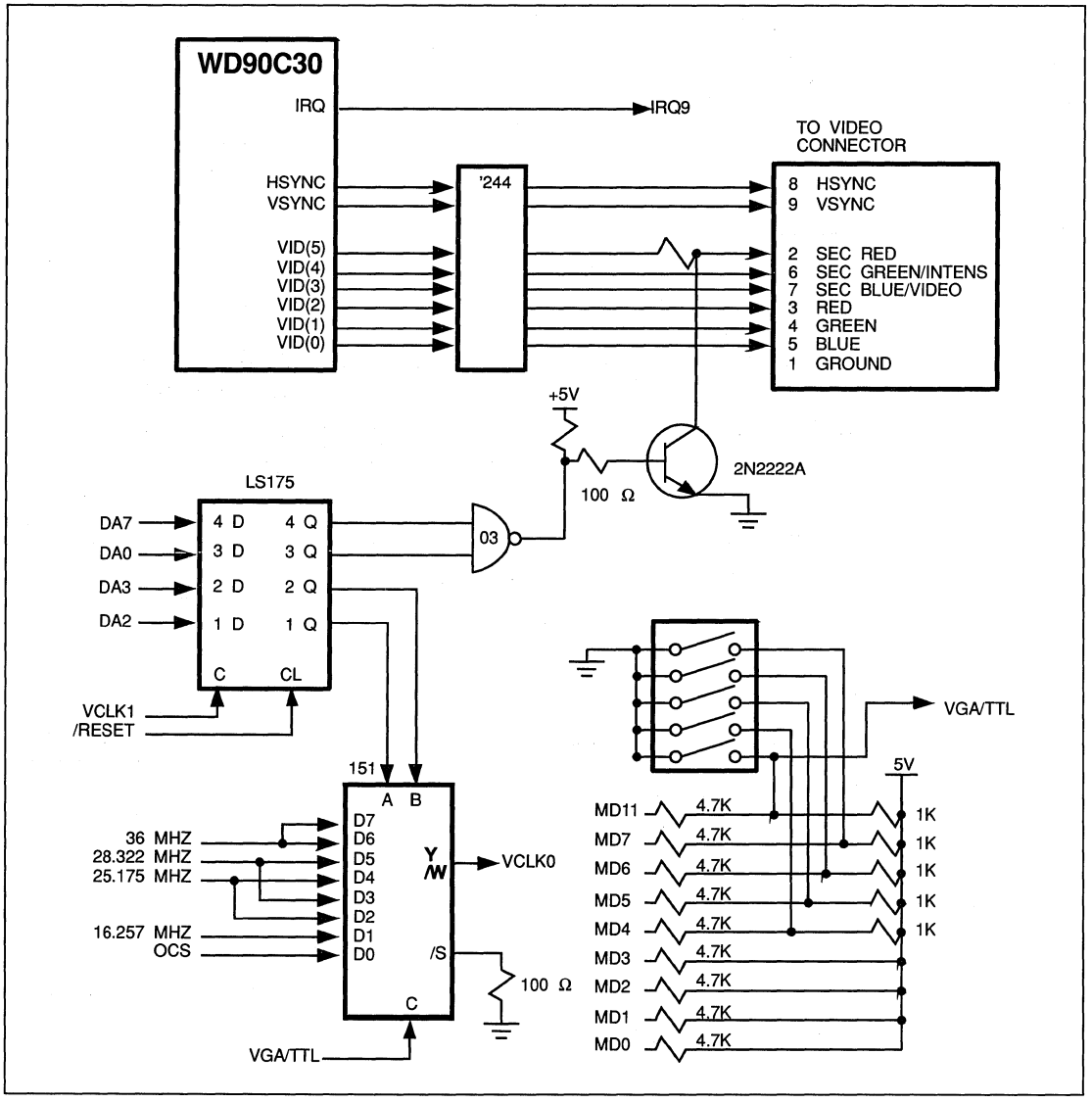

FIGURE 22. WD90C30 AND TTL MONITOR CONNECTIONS

B.9 CLOCK INTERFACE

Figure 23 illustrates the WD90C30 with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H Bit 3 and Bit 2 and is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C30 signal pins (VCLK1, VCLK2) inputs.

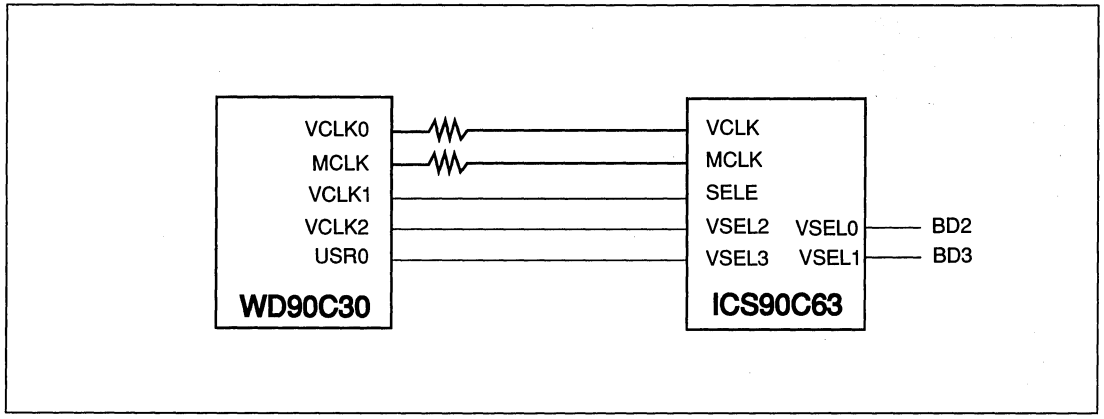

FIGURE 23. CLOCK INTERFACE

C.0 APPENDIX C - SHADOW REGISTER IMPLEMENTATION

The Shadow Register has been implemented on some of the CRTC registers. The purpose of using the shadow register is to have one CRTC register that is writable and readable all the time by application programs without actually changing CRTC timing. The actual CRTC timing registers are initialized and locked while using the shadow register for compatibility.

Registers are added to the following CRTC registers. The shadowed registers can be locked by writing "XXXXX101" to PR1A(3?5.3DH). This lock overrides any other locks. Then by setting PR1A Bit 3 = 1, this will select the shadow register for read.

HORIZONTAL TIMING			
ADDRESS	**BITS**	**LOCK**	**DESCRIPTION**
3?5.00	7:0	Group 0	Horizontal Total
3?5.02	7:0	Group 0	Start Horizontal Blanking
3?5.03	4:0	Group 0	End Horizontal Blanking
3?5.05	7	Group 0	Bit 6 of EHB
3?5.04	7:0	Group 0	Start Horizontal Retrace
3?5.05	4:0	Group 0	End Horizontal Retrace
3?5.03	6:5	Group 0	Display Enable Skew
3?5.05	6:5	Group 0	Horizontal Retrace Skew
VERTICAL TIMING			
ADDRESS	**BITS**	**LOCK**	**DESCRIPTION**
3?5.06	7:0	Group 2	Vertical Total
3?5.07	5,0	Group 2	Bits 9, 8 of VT
3?5.10	7:0	Group 3	Vertical Retrace Start
3?5.07	7,2	Group 2	Bits 9, 8 of VRS
3?5.11	3:0	Group 3	Vertical Retrace Start
3?5.15	7:0	Group 3	Start Vertical Blank
3?5.07	3	Group 2	Bit 8 of SVB
3?5.09	5	Group 2	Bit 9 of SVB
3?5.16	7:0	Group 3	End Vertical Blank

Note:
Group 0: Registers will be locked if PR3(5) = 1 or 3?5.11H bit 7 = 1
Group 2: Registers will be locked if PR3(0) = 1 or 3?5.11H bit 7 = 1
Group 3: Registers will be locked if PR3(0) = 1
Group 0, 2, 3 registers listed above will be locked if PR1A = "xxxxx101", regardless of the contents of PR3.
The Horizontal Display End and the Vertical Display End registers are not shadowed.

TABLE 19. SHADOW REGISTER IMPLEMENTATION

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D.0 APPENDIX D - SIGNATURE ANALYZER

A signature analyzer was designed for use in the WD90C30. The primary purpose of the signature analyzer is to aid in IC test and board level test. The signature analyzer allows the video output path to be included in diagnostics. Signature analysis is a method of compressing large amounts of data to be compared. Each video frame (video data and mode dependent) has a unique signature capable of detecting single bit errors.

D.1 DESCRIPTION

The basis of the signature analyzer is a linear feedback shift register (LFSR). The inputs to the LFSR tap onto the VID_[0:7] output of the IC. The signal path of the video outputs is not modified by adding the signature analyzer. A block diagram is shown below. The primary variables in designing a signature analyzer are length of the shift register and the feedback terms to be used. The length will affect the probability of masking an error. The chance of masking an error is approximately $1/2^n$, where n is the length of the shift register. A 16-bit signature register is used on the WD90C30. Selection of an optimal feedback polynomial will depend on the type of errors expected. The CRC-CCITT polynomial ($x^{16} + x^{12} + x^5 + 1$) has been implemented on the WD90C30. It was modified for multiple inputs as shown in the block diagram.

D.2 OPERATION

The signature analyzer was designed to collect signature of the VID_[0:7] outputs over one vertical frame. The signal path of the VID_[0:7] has not been altered. The signature analyzer register (LFSR) is enabled at the falling edge of the internal VSYNC (before polarity selection) if the start bit is high. The following rising edge of the VSYNC signal will disable the LFSR. In the case of interlaced operation, signature is collected from the beginning of the even field to the end of the odd field. The signature analyzer contains a 4-bit control register PR19 (address 3?5.3FH). Power-up-reset clears this register to 00H. This register has both read and write locks. The read lock originates from PR10 Bits 7 and 3. The write lock originates from PR10 Bits 2 through 0. PR10 also serves as the lock for other registers.

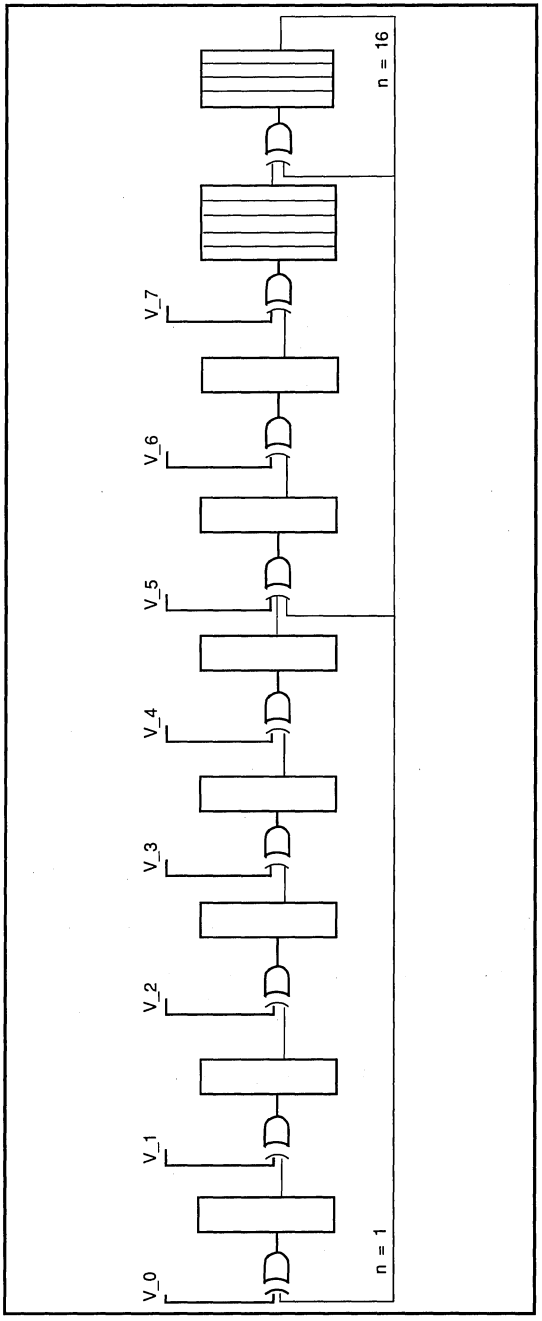

FIGURE 24. LINEAR FEEDBACK SHIFT REGISTER

BIT	FUNCTION	READ/WRITE	DESCRIPTION
BIT 0	Start/status	R/W	Writing "1" to this bit position enables the signature analyzer to collect a signature at the falling edge of the next vertical sync pulse. This bit may be read to check status if the read lock is disabled. 1: Busy 0: Finished or not enabled
BIT 1	Clear	R/W	Writing "0" to this bit position preloads the LFSR with 0001H. This bit must be set to operate the signaure analyzer. 1: Normal operation 0: Preload LFSR
BIT 2	Disable Video input	R/W	This bit is used in a self-test mode. A fixed signature will be generated for any given mode (independent of video memory data). 1: Disable video inputs 0: Enable video inputs
BIT 3	Lock Read Port	R/W	This bit must be set in order to read the signature and status. 1: Enable read of LFSR (addresses 3?5.20H and 3?5.21H). 0: Disable reads of LFSR

TABLE 20. CONTROL REGISTER PR19

The following programming steps highlight the sequence that will setup, check, and read the signature.

Step 1) 85H-> 3?5.29H; release control register (PR10) read and write lock

Step 2) 00H-> 3?5.3FH; clear signaure analyzer

Step 3) 03H-> 3?5.3FH; enable signature analyzer to collect signature

Step 4) read 3?5.3FH; check status for busy
if LSB = 1 repeat step 4
if LSB = 0 signature is collected, proceed to step 5

Step 5) OAH-> 3?5.3FH; enable signature analyzer read port

Step 6) read 3?5.20H; read low byte of signature

Step 7) read 3?5.21H; read high byte of signature

Step 8) 00H-> 3?5.3FH; clear signaure analyzer and lock read port.

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E.0 APPENDIX E - I/O MAPPING

E.1 INTRODUCTION

The I/O Mapping was designed for use in the WD90C30 to isolate board level solder defects. The I/O Mapping allows the IC to enter a test mode where all of pins in the IC are divided into various groups as inputs and output. The path from PCB trace through inputs, IC, output and PCB trace can be treated as a simple path. With test points on board, test for opens and shorts can be performed quickly.

E.2 TEST MODE

There are four requirements to meet for the WD90C30 to enter the I/O mapping test mode .

- $\overline{\text{MWR}}$ is LOW
- $\overline{\text{IOR}}$ is LOW
- CONFIGURATION SWITCH 2 is HIGH (MD2 is pulled high)
- RESET is HIGH

If both $\overline{\text{MWR}}$ and $\overline{\text{IOR}}$ are low at the same time, it becomes an illegal condition in AT machines and a reserved condition in the PS/2 machines. Configuration switch 2 high will ensure that WD90C30 is in AT mode. Reset controls a transparent latch as shown in Figure 25. Reset can be dropped low to latch the test mode. All the bidirectional pins are forced to input mode when in the test mode.

E.3 PIN GROUPINGS

The following pin groupings are done to minimize routing overhead of I/O pin mapping. Multiple input pins in a row are ORed together to the output shown in the following table. The input column lists the input pin number(s) along with the signal name(s). The output column lists the output pin number along with the pin name that corresponds to the input pin(s).

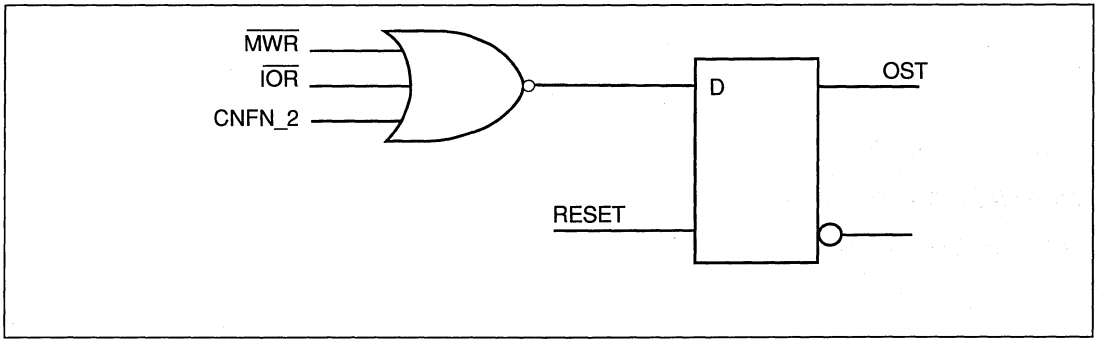

FIGURE 25. TEST MODE CIRCUIT

INPUT PINS		OUTPUT PINS	
PIN	**NAME**	**PIN**	**NAME**
P1	MDET	P123	VID4
P4	MCLK	P124	VID5
P8	MD31	P125	VID6
P9	MD30	P126	VID7
P10 + P13	MD29 + MD26	P2	USR1
P11 + P14	MD28 + MD25	P3	USR0
P12	MD27	P7	$\overline{WE3}$
P15	MD24	P6	$\overline{OE}$
P19 + P24 + P31	MD23 + MD18 + MD15	P27	$\overline{RAS4}$
P20	MD22	P16	$\overline{WE2}$
P21 + P25 + P32	MD21 + MD17 + MD14	P28	$\overline{RAS3}$
P22 + P26 + P33	MD20 + MD16 + MD13	P30	$\overline{WE1}$
P23 + P34 + P43	MD19 + MD12 + MD6	P39	$\overline{RAS}$
P35 + P38	MD11 + MD8	P52	$\overline{WE0}$
P36 + P41	MD10 + $\overline{CAS}$	P53	MA0
P37 + P42 +P46	MD9 + MD7 + MD3	P54	MA1
P44 + P47	MD5 + MD2	P55	MA2
P45 + P49	MD4 + MD0	P56	MA3
P48 + P62	MD1 + A17	P57	MA4
P63 + P68	A18 + A22	P59	MA6
P64 + P69 + P72	A19 + A23 + $\overline{BHE}$	P58	MA5
P65	A20	P60	MA7
P66 + P73 + P86	A21 + ALE + $\overline{ROM16}$	P61	MA8
P70 + P77 + P80	$\overline{IOCS16}$ + $\overline{IOW}$ + RESET	P74	IRQ
P90 + P93 + P95 P79 + P89	DA15 + DA12 + DA10 + $\overline{MWR}$ + A16	P71	$\overline{MEMCS16}$
P75 + P78 + P88	EMEM + $\overline{MRD}$ + $\overline{EDBUFH}$	P82	IOCHRDY
P85 + P92	$\overline{EIO}$ + DA13	P81	$\overline{0WS}$
P91 + P94	DA14 + DA11	P87	$\overline{EBROM}$
P76 + P77	$\overline{IOR}$ + $\overline{IOW}$	P100	DIR**
P96 + P101	DA9 + DA7	P115	$\overline{RPLT}$
P97 + P102	DA8 + DA6	P114	$\overline{WPLT}$
P98 + P103	$\overline{EABUF}$ + DA5	P113	$\overline{HTL}$
P104 + P109	DA4 + $\overline{EDBUFL}$	P112	$\overline{BLANK}$
P105 + P107	DA3 + DA1	P110	VSYNC
P106 + P108	DA2 + DA0	P111	HSYNC

Note:
A "+" in the input column indicates an OR function for the test input pins only.
** This mapping for DIR output is valid only during RESET HIGH.

TABLE 21. WD90C30 PIN SCAN MAP FOR 132-PIN PACKAGE

INPUT PINS		OUTPUT PINS	
PIN	NAME	PIN	NAME
P128	VCLK0	P118	PLCK
P129	VCLK1	P119	VID0
P130	VCLK2	P120	VID1
P131	$\overline{\text{EXPCLK}}$	P121	VID2
P132	$\overline{\text{EXVID}}$	P122	VID3

TABLE 21. WD90C30 PIN SCAN MAP FOR 132-PIN PACKAGE (Cont.)

Refer to Table 3 for the comparable pin number for a 144-pin package.

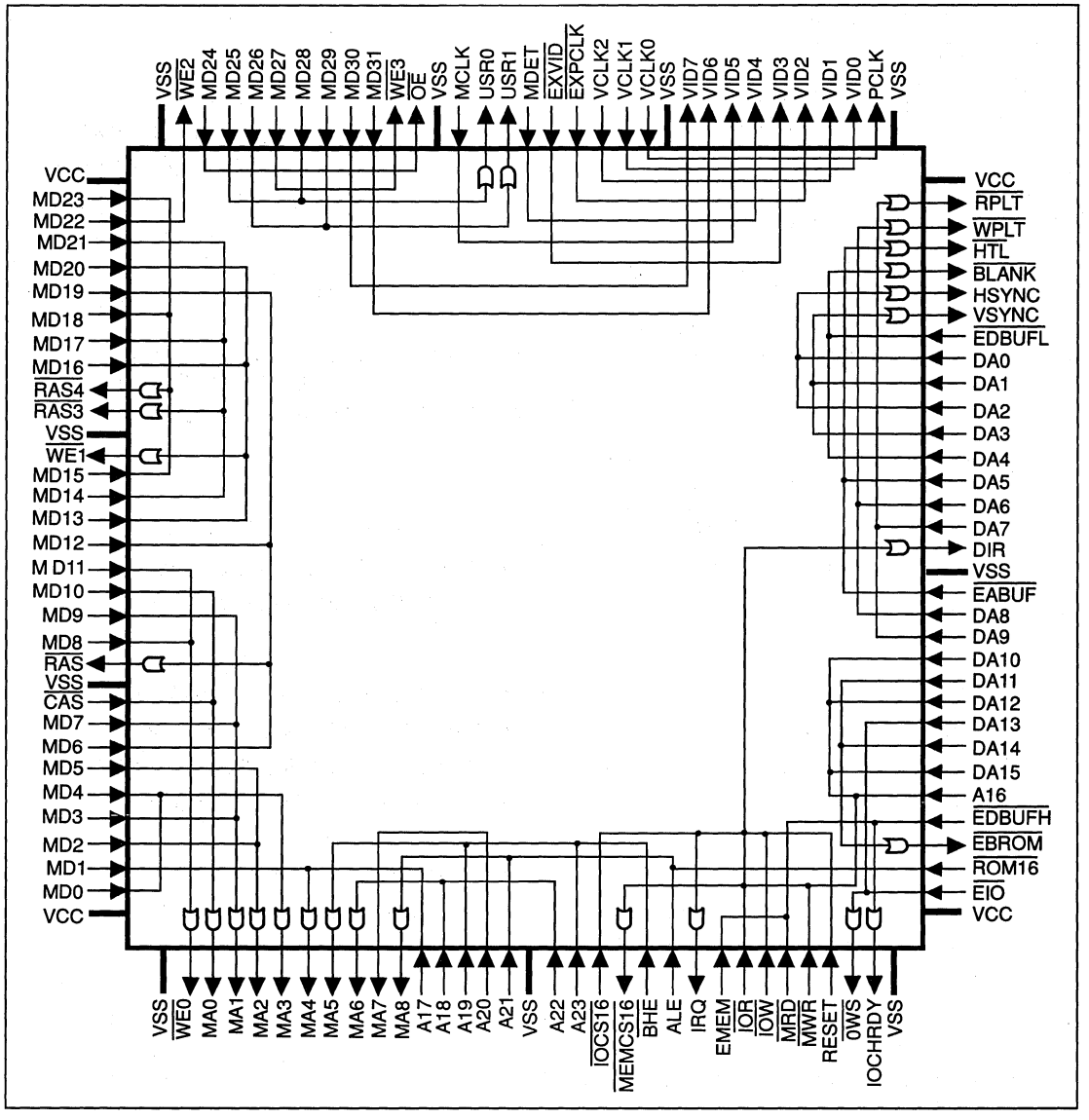

FIGURE 26. WD90C30 PIN SCAN MAP FOR A 132-PIN PACKAGE

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F.0 APPENDIX - F

The WD90C30 design is based on the popular WD90C11 design. Please refer to the WD90C11 data sheet for more informaton. This appendix highlights the major differences between the two devices.

F.1 REGISTER DIFFERENCES BETWEEN WD90C30 AND WD90C11

PR30 Write Buffer and FIFO Control Register, Read/Write Port = 3C5H, Index = 10H

The register also exists in WD90C11. In the WD90C30 chip, the definition of this register is the same except for Bits 7, 6, 5, and 3. All bits are reset to zero at Power-On-Reset (POR).

Bit (7:6)

BIT	VALUE	FUNCTION
7-6	00	One-level write buffer
7-6	01	Two-level write buffer
7-6	10	Three-level write buffer
7-6	11	Four-level write buffer

NOTE: Write buffer is turned on by setting PR31 (3C5H INDEX 11H) Bit 2 = 1. Otherwise, these two bits have no effect.

WD90C30 - FEATURES	WD90C11 - FEATURES
• Multiplexed CPU address and data	• Separated CPU address and data buses.
• Programmable CPU address decoding to map VGA anywhere in the CPU address space.	• Fixed CPU address decoding (0A000 - 0BFFF)
• 16-bit or 32-bit video memory interface	• 8 or 16-bit video memory interface
• Support for 1 Mbyte of memory	• Support for 512 Kbytes of memory
• Support for four or eight 256K by 4 DRAM	• Support for two or four 256K by 4 DRAMs
• 1024 by 768 resolution in 256 colors	• 800 by 600 resolution in 256 colors
• Four levels of CPU write cache	• One level of CPU write cache
• 11-bit vertical counter	• 10-bit vertical counter
• Support for 6 to 16 pixel-wide fonts	• Support for 6 to 8 pixel-wide fonts
• Support for two, four or eight 64K by 16 DRAMs	
• Zero wait state generation	
• CRTC shadow registers	
• Video output signature and pin mapping for system level testing	

TABLE 22. WD90C30 FEATURES / WD90C11 FEATURES

Bit 5

BIT	VALUE	FUNCTION
5	0	32-bit display memory interface.
5	1	16-bit display memory interface.

Bit 4

BIT	VALUE	FUNCTION
4	0	Enable word transfer in planar modes.
4	1	Disable word transfer in planar modes.

Bit 3

BIT	VALUE	FUNCTION
3	0	8-Level or 4-level screen refresh FIFO, depending on Bit 2.
3	1	2-level screen refresh FIFO regardless of bit 2.

Bit 2

BIT	VALUE	FUNCTION
2	0	8-level screen refresh FIFO.
2	1	4-level screen refresh FIFO.

Bits (1:0)

BIT	VALUE	FUNCTION
1-0	00	Generate FIFO request when FIFO is one level empty.
1-0	01	Generate FIFO request when FIFO is two levels empty.
1-0	10	Generate FIFO request when FIFO is three levels empty.
1-0	11	Generate FIFO request when FIFO is four levels empty.

F.2 PR33 DRAM TIMING AND ZERO WAIT STATE CONTROL REGISTER, READ/ WRITE PORT = 3C5H, INDEX = 13H

This is a new register in the WD90C30.

Bits (7:6)

BIT 7	BIT 6	FUNCTION
0	0	$\overline{0WS}$ = 0 if the internal write cache is ready.
0	1	$\overline{0WS}$ = 0 if the internal write cache is ready AND memory address is decoded.
1	0	$\overline{0WS}$ = 0 if the internal write buffer is ready AND memory address is decoded AND MWR = 0.
1	1	$\overline{0WS}$ = 0 if the condition "1, 0" is true OR I/O address is decoded.

Bit 5

Reserved

Bits (4:3)

BIT	VALUE	FUNCTION
4-3	00	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1 Mclock + (4-7) ns. $\overline{CAS}$ high is 1 Mclock - (4-7) ns.
4-3	01	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1 Mclock + (8-14) ns. $\overline{CAS}$ high is 1 Mclock - (8-14) ns.
4-3	10	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1.5 Mclocks. $\overline{CAS}$ high is 0.5 Mclocks.
4-3	11	Reserved.

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Bit 2

BIT	VALUE	FUNCTION
2	0	$\overline{CAS}$ cycle starts 3 Mclocks after $\overline{RAS}$ low.
2	1	$\overline{CAS}$ cycle starts 2 Mclocks after $\overline{RAS}$ low.

Bits (1:0)

BIT	VALUE	FUNCTION
1-0	00	$\overline{RAS}$ high is two and half Mclocks plus a 4-7 ns delay.
1-0	01	$\overline{RAS}$ high is three Mclocks wide.
1-0	10	$\overline{RAS}$ high is two Mclocks wide.
1-0	11	$\overline{RAS}$ high is two and a half Mclocks.

F.3 PR34 VIDEO MEMORY MAPPING REGISTER, READ/WRITE PORT = 3C5H, INDEX = 14H

Bits (7:0)

BITS	FUNCTION
7-4	Reserved.
3-0	The contents of these four bits are compared with the CPU address A_[23:20] as part of the video memory address decoding. This will allow the VGA to be mapped out of the lowest 1Mbyte of CPU memory space. This register will not affect the $\overline{ROM16}$ decoding. $\overline{ROM16}$ will still decode at A_[23:20] = 0H.

F.4 PR1 MEMORY SIZE REGISTER, READ/WRITE PORT = 3CFH, INDEX = 0BH

Bits (7:6)

BIT	VALUE	FUNCTION
7-6	00	Same as 1C.IBM 256 Kbyte VGA.
7-6	01	Same as 1C.256 Kbyte Paradise VGA.
7-6	10	Same as 1C.512 Kbyte Paradise VGA.
7-6	11	1024 Kbyte Paradise VGA.

Bits (5:4)

BIT	VALUE	FUNCTION
5-4	00	IBM memory mapping. Decode memory address range is from A0000H - BFFFFH depending on register Bits 3 and 2 (3CFH Index 06H).
5-4	01	Decode memory address range from 00000H - 3FFFFH (256K total).
5-4	10	Decode memory address range from 0000H - 7FFFFH (512K total).
5-4	11	Decode memory address range from 00000H - FFFFFH (1 M total).

Bits (3:0)

BITS	FUNCTION
3	Enable Alternate Address Offset Register PROB.
2	16-Bit Video Memory.
1	ROM Data Width.
0	BIOS ROM Map Out.

Bit 3

Enable Alternate address Offset Register PROB

Bit 2

Enable 16-bit bus for Video Memory. When set to 1, $\overline{\text{MEMCS16}}$ is asserted for all video memory cycles.

Bit 1

0 = BIOS ROM has an 8-bit data path.

1 = BIOS ROM has a 16-bit data path from C000:0H - DFFF:FH, if bit 0 = 0. ($\overline{\text{ROM16}}$ responds to ROM access).

A pull-down resistor on MD(10) sets this bit to 1 after power-on-reset. This bit can also be set to 1 by an I/O write to PR1 register if CNF(1) = 1 (2 ROMs).

Bit 0

If set to 1 the BIOS ROM is mapped out. Pull-up resistor latches bit 0 after power-up. A pull-up on MD(0) sets this bit to 0 at power-on-reset.

F.5 PR22 SCRATCH PAD REGISTER, READ/WRITE PORT = 3C5H, INDEX = 8H

This is a new register in the WD90C30.

Bits (7:0)

Scratch Bits

F.6 PR23 SCRATCH PAD REGISTER, READ/WRITE PORT = 3C5H, INDEX = 9H

This is a new register in the WD90C30.

Bits (7:0)

Scratch Bits

F.7 PROA AND PROB ADDRESS OFFSET REGISTERS, READ/WRITE PORT = 3CFH, INDEX = 09H AND 0AH

Bit 7

This bit is the 7th memory address offset bit.

Bits (6:0)

Primary/Alternate Address Offset Bits.

The WD90C30 is capable of controlling up to 512 Kbytes of display memory. However, DOS only assigns 128 Kbytes of total memory space for the display memory, starting at A0000H and ending at BFFFFH. For VGA to reach the memory beyond this range, the WD90C30 has two CPU address offset registers, PROA and PROB. These registers can be used to support more than 128 Kbytes of linear display memory address space.

The Contents of PROA (bits 6:0) or PROB (bits 6:0) are always added to the CPU address A(18:12) before they are translated to display memory address. This is similar to the segment registers DS and ES in the 8088/80X86 architecture. PROA and PROB provide a 4 Kbyte segmentation of the display memory. Increment PROA or PROB by one of its equivalents to jump a 4 Kbyte segment to another 4 Kbyte segment of the display memory.

Both PROA and PROB are set to zero at power-on-reset.

There are two ways to control whether PROA or PROB get added into the CPU address.

1. Sequencer Extention Register 3C5H Index 11H bit 7 = 0.

PROA is the primary offset register being added to the CPU address. PR1, bit 3 enables PROB which becomes the secondary offset register.

If Graphics Controller Index 6H bits 3:2 = 00, A000:0H for 128K, and PR1 bit 3 = 1, then PROA offsets the CPU address from B000:0H to BFFF:FH while PROB offsets the CPU address from A000:0H to AFFF:FH.

If Graphics Controller Index 6H, bits 3:2 = 01 (A000:0H for 64K), and PR1 bit 3 = 1, then PROA offsets the CPU address from A800:0H to AFFF:FH, while PROB offsets the CPU address from A000:0H - A7FF:FH.

2. Sequencer Extention Register 3C5H Index 11H bit 7 = 1.

Both PROA and PROB are enabled. PROA is selected as the offset register unless a CPU memory write selects PROB as the offset register.

F.8 PR17 MISCELLANEOUS CONTROL REGISTER, READ/WRITE PORT = 3?5H, INDEX = 30H

Bits (7:6)

Reserved.

Bit 5

BIT	VALUE	FUNCTION
5	0	No effect.
5	1	In text mode, if PR2 Bits 2 and 3 = 11, then the 10-dot font is selected. Otherwise, it has no effect.

Bit 4

BIT	VALUE	FUNCTION
4	0	No effect.
4	1	PCLK is divided by two.

Bits (3:0)

BITS	FUNCTION
3	Map Out 4K BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map Out 2K of BIOS ROM.

Bit 3

Map out 4K of BIOS ROM.

Setting this bit to 1 disables access to the BIOS ROM in the system address range C600:0H - C6FF:FH.

Power on reset sets this bit to 0.

Bit 2

Enable 64K BIOS ROM.

Setting this bit to 1 enables access to the BIOS ROM in the system range C000:0H - CFFF:FH.

Power on reset sets this bit to 0.

Bit 1

Setting this bit to 1 locks Hercules compatibility register (I/O Port 3BFH).

Power on reset sets this bit to 0.

Bit 0

Map out 2K of BIOS ROM.

Setting this bit to 1 disables access to the BIOS ROM in the system address range C600:0H - C67F:FH.

Power on reset sets this bit to 0.

F.9 PR18 VERTICAL TIMING OVERFLOW REGISTER, READ/WRITE PORT = 3?5H, INDEX = 3EH

Bits (7:0)

BITS	FUNCTION
7:5	Reserved
4	Line compare Bit 10.
3	Start vertical blank Bit 10.
2	Start vertical retrace Bit 10.
1	Vertical display enable end Bit 10.
0	Vertical total Bit 10.

F.10 WD90C30 - NEW CONFIGURATION BITS

The WD90C30 provides three new bits in addition to the configuration bits that are standard with the WD90C11. The following configuration bits are set during power-on-reset. A pull-down resistor on the corresponding MD bits will cause a configuration bit to be set low. Otherwise, configuration bits are high.

Configuration Bit 18

0 = The $\overline{\text{ROM16}}$ pin is an input. $\overline{\text{ROM16}}$ becomes EXBLANK.

1 = The $\overline{\text{ROM16}}$ pin is an output pin.

Configuration Bit 16

0 = 64K by 16 DRAM

1 = 256K by 4 or 256K by 16 DRAM

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G.0 PACKAGE DIMENSIONS

Figure 27 illustrates the 132-pin JEDEC package showing the dimensions in inches. Figure 28 illustraes the 144-pin EIAJ package showing the dimensions in millimeteres and inches.

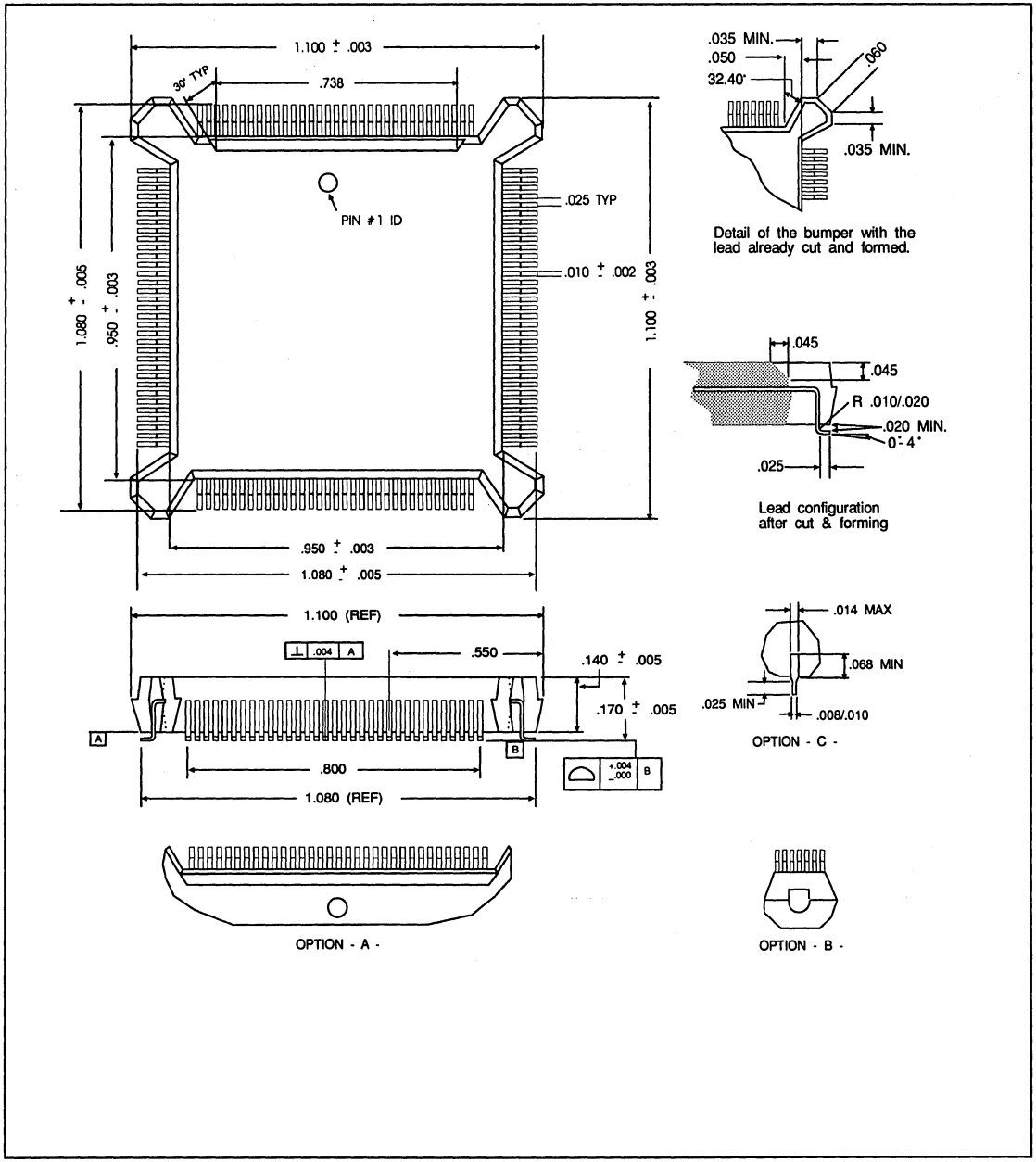

FIGURE 27. 132-PIN JEDEC PACKAGE

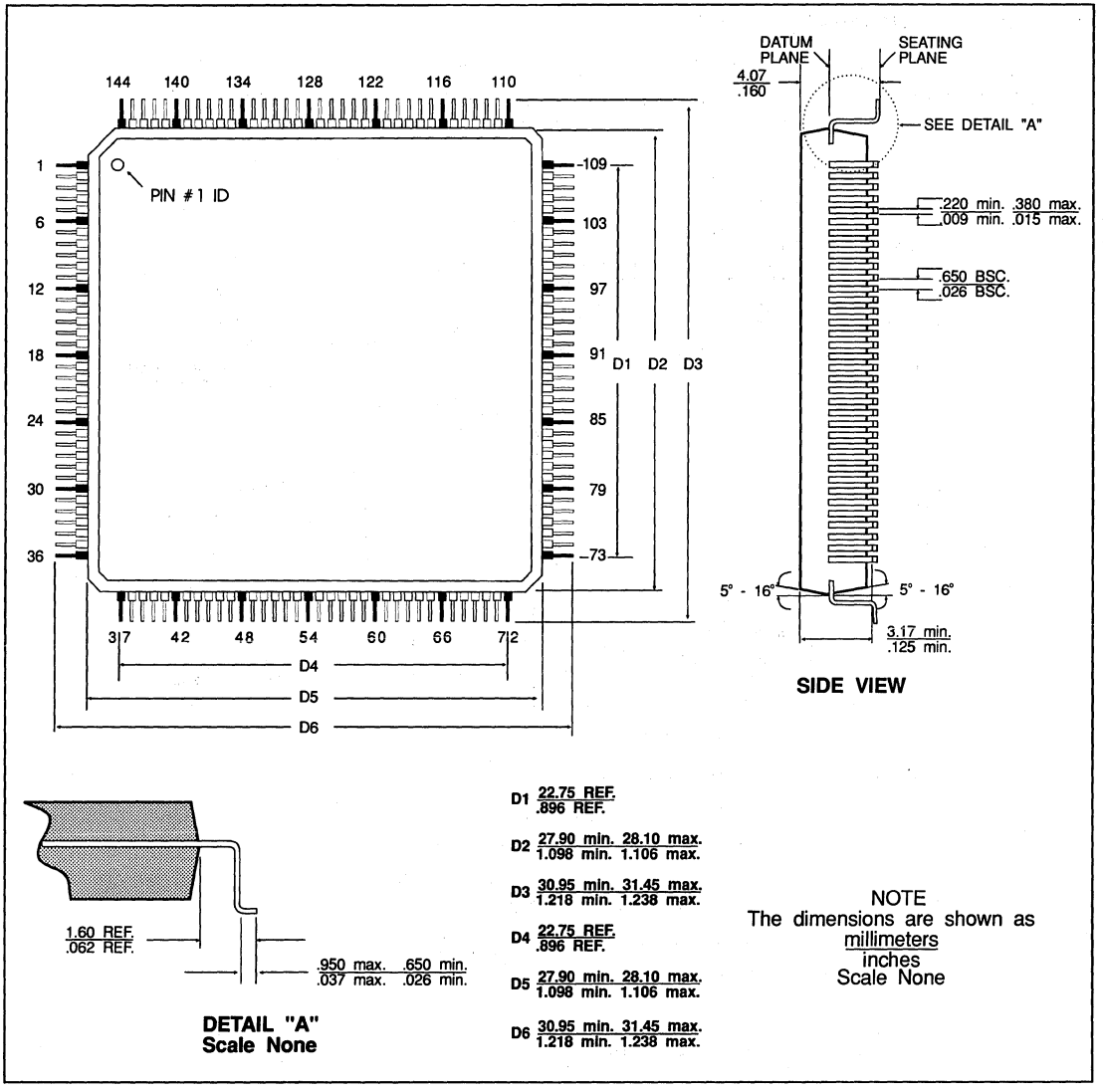

FIGURE 28. 144-PIN EIAJ PACKAGE