W83194BR-645
Data Sheet

WINBOND
CLOCK GENERATOR
FOR
SIS 645/650 CHIPSET

Publication Release Date: April 13, 2005

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1. GENERAL DESCRIPTION

The W83194BR-645 is a Clock Synthesizer for SiS645/650 chipset. W83194BR-645 provides all clocks required for high-speed Intel Pentium 4, and also provides 32 different frequencies of CPU clocks frequency setting. All clocks are externally selectable with smooth transitions. The W83194BR-645 makes SDRAM in synchronous or asynchronous frequency with CPU clocks.

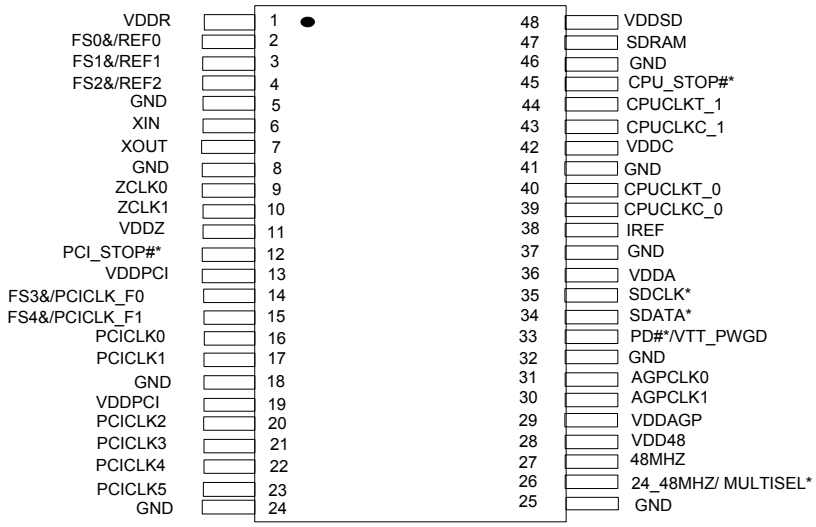
The W83194BR-645 provides step-less frequency programming by controlling the VCO freq. and the programmable AGP, PCI clock output divisor ratio. A watchdog timer is quipped and when time out, register9 bit5 will be set to 1 for warning. Spread spectrum built in at ±0.5% or ±0.25% to reduce EMI. Programmable stopping individual clock outputs and frequency selection through I^2C interface

The W83194BR-645 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1V /nS slew rate into 30 pF loads. The fixed frequency outputs as REF, 24 MHz, and 48 MHz provide better than 0.5V /nS slew rate.

2. FEATURES

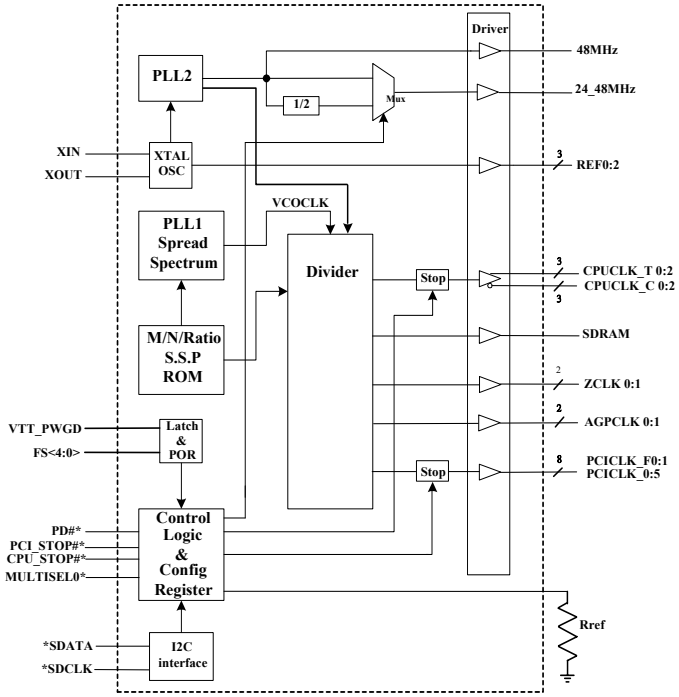
- Supports Intel Pentium 4 CPU with I^2C.
- 2 pairs of differential CPU clocks
- 2 ZCLK for SiS 645/650 chipset
- 2 AGP clocks
- 1 SDRAM output clock for chipset
- 8 PCI synchronous clocks
- 1 24/48 MHz, 1 48 MHz
- 3 REF clocks
- Skew --- CPU to SDRAM < 1 nS, PCI to PCI < 500 pS, AGP to AGP < 175 pS
- Smooth frequency switch with selections from 66 to 200 MHz
- I^2C 2-Wire serial interface and I^2C read back
- Flexible spread spectrum to reduce EMI
- Programmable registers to enable/stop each output and select modes (Mode as Tri-state or Normal)
- Packaged in 48-pin SSOP

3. PIN CONFIGURATION



&: pull-down 120K
*** : pull-up 120K**
 # :input active low

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{tp120k}	Latched input at power up, internal 120 KΩ pull up.
IN_{td120k}	Latched input at power up, internal 120 KΩ pull down.
OUT	Output
OD	Open Drain
I/O	Bi-directional Pin
I/OD	Bi-directional Pin, Open Drain.
#	Active Low
*	Internal 120 KΩ pull-up
&	Internal 120 KΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
6	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
7	XOUT	OUT	Crystal output at 14.318 MHz nominally with internal loading capacitors (18pF).

5.2 CPU, ZCLK, SDRAM, PCI Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
40, 39, 44, 43	CPUCLKT_0 CPUCLKC_0, CPUCLKT_1 CPUCLKC_1,	OUT	True CPU clock output and Complementary CPU clock output. This pin will be stopped by CPU_STOP#
47	SDRAM	OUT	SDRAM clock output, which have syn. or asyn. Frequencies as CPU clocks. The clock phase is the same as CPUCLKT_0 and CPUCLKT_1.
14	PCICLK_F0	OUT	PCI free running clock during normal operation.
	FS3&	IN_{td120k}	Latched input for FS3 at initial power up for H/W selecting the output frequency. Internal 120KΩ pull-down
15	PCICLK_F1	OUT	PCI free running clock during normal operation.
	FS4&	IN_{td120k}	Latched input for FS4 at initial power up for H/W selecting the output frequency. Internal 120KΩ pull-down
16, 17, 20, 21, 22, 23	PCICLK [0:5]	OUT	Low skew (< 500pS) PCI clock outputs.

31, 30	AGPCLK [0:1]	OUT	AGP clock outputs for AGP.
9, 10	ZCLK [0:1]	OUT	Z clock outputs for chipset.

5.3 I2C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
34	SDATA*	I/O	Serial data of I^2C 2-wire control interface, Internal 120kΩ pull-up.
35	SDCLK*	IN	Serial clock of I^2C 2-wire control interface, Internal 120kΩ pull-up.

5.4 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
38	IREF	IN	Deciding the reference current for the CPUCLK pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current. There are two modes to select different current via power on trapping the Pin 26 (MULTISEL0). The table is show as follows.
2	REF0	OUT	3.3V, 14.318 MHz reference clock output.
	FS0&	IN_{td120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency. Internal 120KΩ pull-down.
3	REF1	OUT	3.3V, 14.318 MHz reference clock output.
	FS1&	IN_{td120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency, Internal 120KΩ pull-down.
4	REF2	OUT	3.3V, 14.318 MHz reference clock output.
	FS2&	IN_{td120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency. Internal 120KΩ pull-down.
26	24_48 MHz	OUT	24 MHz or 48 MHz selected by Register.
	MULTISEL0*	IN_{tp120k}	MULTISEL0 at initial power up for H/W selecting the current multiplier for CPU outputs. Internal 120KΩ pull-up.
27	48 MHz	OUT	48 MHz output for USB.

5.5 Power Management Pins

PIN	PIN NAME	TYPE	DESCRIPTION
33	PD#*	IN	Power Down pin, if PD# = 0, all clocks are stopped.
	VTT_PWGD	IN	Power good input signal comes from ACPI with high active. This 3.3V input is level sensitive strobe used to determine FS [4:0] and MULTISEL input are valid and is ready to sample. This pin is high active.
45	CPU_STOP#*	IN	CPU clock stop control pin, This pin is low active. Internal 120KΩ pull-up.
12	PCI_STOP#*	IN	PCI clock stop control pin, This pin is low active. Internal 120KΩ pull-up.

5.6 Power Pins

PIN	PIN NAME	DESCRIPTION
1	VDDR	Power supply for REF0: 2 3.3V.
11	VDDZ	Power supply for ZCLK 3.3V.
36	VDDA	Power supply for core logic. 3.3V
42	VDDC	Power supply for CPUCLK 3.3V.
29	VDDAGP	Power supply for AGP outputs.
13,19	VDDPCI	Power supply for PCI outputs.
48	VDDSD	Power supply for SDRAM 3.3V.
28	VDD48	Power supply for 48/24 MHz outputs.
5, 8, 18, 24, 25, 32, 37, 41, 46	GND	Circuit Ground.

Hardware MULTSEL [1:0] Selects Function

Multsel1 Byte 8 bit 0	Multsel0 Pin 26	Board Target trace/Term Z	Reference R, IREF = VDD/(3*Rr)	Output Current	Voh @ Z
0	0	50 Ω	Rr = 221 1% IREF = 5.00 mA	Ioh = 4*IREF	1.0V @ 50
0	0	60 Ω	Rr = 221 1% IREF = 5.00 mA	Ioh = 4*IREF	1.2V @ 60
0	1	50 Ω	Rr = 221 1% IREF = 5.00 mA	Ioh = 5*IREF	1.25V @ 50
0	1	60 Ω	Rr = 221 1% IREF = 5.00 mA	Ioh = 5*IREF	1.5V @ 60
1	0	50 Ω	Rr = 221 1% IREF = 5.00 mA	Ioh = 6*IREF	1.5V @ 50
1	0	60 Ω	Rr = 221 1% IREF = 5.00 mA	Ioh = 6*IREF	1.8V @ 60
1	1	50 Ω	Rr = 221 1% IREF = 5.00 mA	Ioh = 7*IREF	1.75V @ 50
1	1	60 Ω	Rr = 221 1% IREF = 5.00 mA	Ioh = 7*IREF	2.1V @ 50
0	0	50 Ω	Rr = 475 1% IREF = 2.32 mA	Ioh = 4*IREF	0.47V @ 50
0	0	60 Ω	Rr = 475 1% IREF = 2.32 mA	Ioh = 4*IREF	0.56V @ 50
0	1	50 Ω	Rr = 475 1% IREF = 2.32 mA	Ioh = 5*IREF	0.58V @ 50
0	1	60 Ω	Rr = 475 1% IREF = 2.32 mA	Ioh = 5*IREF	0.7V @ 60
1	0	50 Ω	Rr = 475 1% IREF = 2.32 mA	Ioh = 6*IREF	0.7V @ 50
1	0	60 Ω	Rr = 475 1% IREF = 2.32 mA	Ioh = 6*IREF	0.84V @ 60
1	1	50 Ω	Rr = 475 1% IREF = 2.32 mA	Ioh = 7*IREF	0.81V @ 50
1	0	60 Ω	Rr = 475 1% IREF = 2.32 mA	Ioh = 6*IREF	0.97V @ 60

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 4 bit 4 ~ 7, 2).

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)

0	0	0	0	0	66.67	66.67	66.67	66.67	33.33
0	0	0	0	1	100.00	100.00	66.67	66.67	33.33
0	0	0	1	0	100.00	200.00	66.67	66.67	33.33
0	0	0	1	1	100.00	133.33	66.67	66.67	33.33
0	0	1	0	0	100.00	150.00	60.00	60.00	30.00
0	0	1	0	1	100.00	125.00	62.50	62.50	31.25
0	0	1	1	0	108.00	162.1	64.8	64.8	32.4
0	0	1	1	1	100.00	133.33	80.00	66.67	33.33
0	1	0	0	0	100.00	200.00	66.67	66.67	33.33
0	1	0	0	1	100.00	166.67	62.50	62.50	31.25
0	1	0	1	0	100.00	166.67	71.43	83.33	41.67
0	1	0	1	1	80.00	133.33	66.67	66.67	33.33
0	1	1	0	0	80.00	133.33	66.67	66.67	33.33
0	1	1	0	1	95.00	95.00	63.33	63.33	31.67
0	1	1	1	0	95.00	126.67	63.33	63.33	31.67
0	1	1	1	1	66.67	66.67	50.00	50.00	25.00
1	0	0	0	0	105.00	140.00	70.00	70.00	35.00
1	0	0	0	1	100.90	100.90	67.27	67.27	33.63
1	0	0	1	0	108.00	144.00	72.00	72.00	36.00
1	0	0	1	1	100.90	134.53	67.27	67.27	33.63
1	0	1	0	0	112.00	149.33	74.67	74.67	37.33
1	0	1	0	1	133.33	100.00	66.67	66.67	33.33
1	0	1	1	0	133.33	133.33	66.67	66.67	33.33
1	0	1	1	1	133.33	166.67	66.67	66.67	33.33
1	1	0	0	0	100.00	133.00	80.00	66.67	33.33
1	1	0	0	1	100.00	100.00	80.00	66.67	33.33
1	1	0	1	0	100.00	166.67	83.33	62.50	31.25
1	1	0	1	1	133.33	166.67	83.33	66.67	33.33
1	1	1	0	0	100.00	133.00	100.00	66.67	33.33
1	1	1	0	1	100.00	100.00	100.00	66.67	33.33
1	1	1	1	0	100.00	166.67	100.00	62.50	31.25
1	1	1	1	1	130.4	163.0	93.2	65.2	32.6

7. I²C CONTROL AND STATUS REGISTERS

The Register 0~3 are reserved for external clock buffer

(The register No. Is increased by 1 if use byte data read/write protocol)

7.1 Register 4: Frequency Select Register (default = 0)

BIT	NAME	PWD	DESCRIPTION
7	SSEL [3]	0	Frequency selection by software via I²C
6	SSEL [2]	0	
5	SSEL [1]	0	
4	SSEL [0]	0	
3	EN_SSEL	0	Enable software program FS [4:0]. 0 = Select frequency by hardware. 1= Select frequency by software I²C - Bit 4: 7, 2.
2	SSEL [4]	0	Frequency selection bit 4
1	EN_SPSP	0	Enable Spread Spectrum in the frequency table. 0 = Normal 1 = Spread Spectrum enabled
0	EN_SAFE_FREQ	0	Enable reload safe frequency when the watchdog is timeout. 0 = reload the FS [4:0] latched pins when watchdog time out. 1 = reload the safe frequency bit defined at Register 9 bit 4~0.

7.2 Register 5: CPU, SDRAM Clock Register (1 = Enable, 0 = Stopped)

BIT	PIN NO.	PWD	DESCRIPTION
7	47	1	SDRAM
6	44, 43	1	CPUCLKT/C1
5	40, 39	1	CPUCLKT/C0
4	15	X	FS [4] Read back.
3	14	X	FS [3] Read back
2	4	X	FS [2] Read back
1	3	X	FS [1] Read back
0	2	X	FS [0] Read back

7.3 Register 6 PCI Clock Register (1 = Enable, 0 = Stopped)

BIT	PIN NO.	PWD	DESCRIPTION
7	15	1	PCICLK_F1
6	14	1	PCICLK_F0
5	23	1	PCICLK 5
4	22	1	PCICLK 4
3	21	1	PCICLK 3
2	20	1	PCICLK 2
1	17	1	PCICLK 1
0	16	1	PCICLK 0

7.4 Register 7 48 MHz, ZCLK, REF Clock Register (1 = Enable, 0 = Stopped)

BIT	PIN NO.	PWD	DESCRIPTION
7	27	1	48 MHz
6	26	1	24_48 MHz
5	SEL_24	1	24/48 MHz frequency control 1: 24 MHz. 0: 48 MHz.
4	10	1	ZCLK1
3	9	1	ZCLK0
2	4	1	REF2
1	3	1	REF1
0	2	1	REF0

7.5 Register 8: AGP Control Register (1 = Enable, 0 = Stopped)

BIT	PIN NO.	PWD	DESCRIPTION
7		1	CPUCLKT/C0 Stop control: 0: CPUCLK0 free run 1: CPUCLK0 can stopped by CPU_STOP#
6		1	CPUCLKT/C1 Stop control: 0: CPUCLK1 free run 1: CPUCLK1 can stopped by CPU_STOP#
5		0	PCI_F0 Stop control: 0: PCI_F0 free run

			1: PCI_F0 can stopped by PCI_STOP#

Register 8: AGP Control Register (1 = Enable, 0 = Stopped), continued

BIT	PIN NO.	PWD	DESCRIPTION
4		0	PCI_F1 Stop control: 0: PCI_F1 free run 1: PCI_F1 can stopped by PCI_STOP#
3	30	1	AGP_1
2	31	1	AGP_0
1	MULTISEL0	1	MULTISEL0 trapping pin data read back
0	MULTISEL1	0	MULTISEL1 (IREF output control)

7.6 Register 9: Watchdog Control Register

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	EN_WD	0	Enable Watchdog Timer if set to 1. Set to 0, disable watchdog timer. Read this bit will return a counting state. If timer continues down count, this bit will return 1. Otherwise, this bit will return 0.
5	WD_TIMEOUT	0	Watchdog Timeout Status. If the watchdog is started and timer down counts to zero, this bit will be set to 1. Clear this bit to logic 0, If set to 1, when the watchdog is restart in the next time. This bit is Read Only.
4	SAF_FREQ [4]	0	Watchdog safe frequency bits. These bits will be reloaded into FS [4:0], if the watchdog is timeout and enable reload safe frequency bits.
3	SAF_FREQ [3]	0	
2	SAF_FREQ [2]	0	
1	SAF_FREQ [1]	0	
0	SAF_FREQ [0]	0	

7.7 Register 10: Watchdog Timer Register

BIT	NAME	PWD	DESCRIPTION
7	WD_TIME [7]	0	Watchdog timeout time. The bit resolution is 250 mS. The default time is 8*250 mS = 2.0 seconds. If the watchdog timer is start, this register will be down count. Read this register will return a down count value.
6	WD_TIME [6]	0	
5	WD_TIME [5]	0	
4	WD_TIME [4]	0	
3	WD_TIME [3]	1	
2	WD_TIME [2]	0	
1	WD_TIME [1]	0	

0	WD_TIME [0]	0	

7.8 Register 11: M/N Program Register

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [8]	1	Programmable N divisor value. Bit 7~0 are defined in the Register 12.
6	TEST2	0	Test bit 2. Winbond test bit, do not change them.
5	TEST1	1	Test bit 1. Winbond test bit, do not change them.
4	M_DIV [4]	0	Programmable M divisor value.
3	M_DIV [3]	1	
2	M_DIV [2]	0	
1	M_DIV [1]	1	
0	M_DIV [0]	1	

7.9 Register 12: M/N Program Register

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [7]	0	Programmable N divisor value bit 7~0. The bit 8 is defined in Register 11.
6	N_DIV [6]	0	
5	N_DIV [5]	1	
4	N_DIV [4]	0	
3	N_DIV [3]	1	
2	N_DIV [2]	1	
1	N_DIV [1]	1	
0	N_DIV [0]	1	

7.10 Register 13: Spread Spectrum Programming Register

BIT	NAME	PWD	DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3.
6	SP_UP [2]	0	Spread Spectrum Up Counter bit 2.
5	SP_UP [1]	0	Spread Spectrum Up Counter bit 1.
4	SP_UP [0]	1	Spread Spectrum Up Counter bit 0
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3
2	SP_DOWN [2]	1	Spread Spectrum Down Counter bit 2
1	SP_DOWN [1]	1	Spread Spectrum Down Counter bit 1

0	SP_DOWN [0]	1	Spread Spectrum Down Counter bit 0

7.11 Register 14: Divisor and Step-less Enable Control Register

BIT	NAME	PWD	DESCRIPTION
7	EN_MN_PROG	0	0: use frequency table 1: use M/N register to program frequency The equation is **VCO freq. = 14.318MHz * (N+4)/ M**. When the watchdog timer is timeout, this will be clear. In this time, the frequency is set to hardware default latched or safe frequency set by EN_SFAE_FREQ (Register 9 bit 0).
6	RATIO_SEL [4]	1	CPU, PCI, AGP, SDRAM, and ZCLK ratio selection. The ratio is shown as following table.
5	RATIO_SEL [3]	0	
4	RATIO_SEL [2]	0	
3	RATIO_SEL [1]	1	
2	RATIO_SEL [0]	1	
1	TEST0	0	Test bit 0. Winbond test bit, do not change them.
0	Reserved	0	

7.12 Register 15: CPU_ZCLK Skew Control Register

BIT	NAME	PWD	DESCRIPTION
7	CPU_ZCLK_SKEW [2]	1	CPU to ZCLK SKEW control
6	Reserved	0	Reserved
5	Reserved	1	Reserved
4	Reserved	0	
3	Reserved	0	
2	Reserved	1	
1	Reserved	1	
0	Reserved	1	

7.13 Register 16: CPU_AGP_SKEW

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved for Winbond internal use, do not change them
6	Reserved	0	
5	Reserved	0	Reserved for Winbond internal use, do not change them
4	CPU_STOP	1	CPU_STOP pin read back

3	PCI_STOP	1	CPU_STOP pin read back
2	CPU_AGP_SKEW [2]	1	CPU to AGP skew.
1	CPU_AGP_SKEW [1]	0	
0	CPU_AGP_SKEW [0]	0	

7.14 Register 17: Skew Control Register

BIT	NAME	PWD	DESCRIPTION
7	CPU_ZCLK_SKEW [1]	0	CPU to AGP skew
6	CPU_ZCLK_SKEW [0]	0	
5	CPU_SDRAM_SKEW [2]	1	CPU to SDRAM skew
4	CPU_SDRAM_SKEW [1]	0	
3	CPU_SDRAM_SKEW [0]	0	
2	CPU_PCI_SKEW [2]	1	CPU to PCI skew
1	CPU_PCI_SKEW [1]	0	
0	CPU_PCI_SKEW [0]	0	

7.15 Register 18: Winbond Chip ID Register (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83194BR-645 is 0x77.
6	CHPI_ID [6]	1	Winbond Chip ID.
5	CHPI_ID [5]	1	Winbond Chip ID.
4	CHPI_ID [4]	1	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	1	Winbond Chip ID.
1	CHPI_ID [1]	1	Winbond Chip ID.
0	CHPI_ID [0]	1	Winbond Chip ID.

7.16 Register 19: Winbond Chip ID Register (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	SUB_ID [3]	0	Winbond Sub-Chip ID. The sub-chip ID of W83194BR-645 is defined as 0001b.
6	SUB_ID [2]	0	Winbond Sub-Chip ID.
5	SUB_ID [1]	0	Winbond Sub-Chip ID.
4	SUB_ID [0]	1	Winbond Sub-Chip ID.

3	VER_ID [3]	0	Winbond Version ID. The Version ID of W83194BR-645 is 0001b.
2	VER_ID [2]	0	Winbond Version ID.
1	VER_ID [1]	0	Winbond Version ID.
0	VER_ID [0]	1	Winbond Version ID.

7.17 Ratio Selection Table

Table of CPU, PCI, AGP, SDRAM, and ZCLK clock selection.

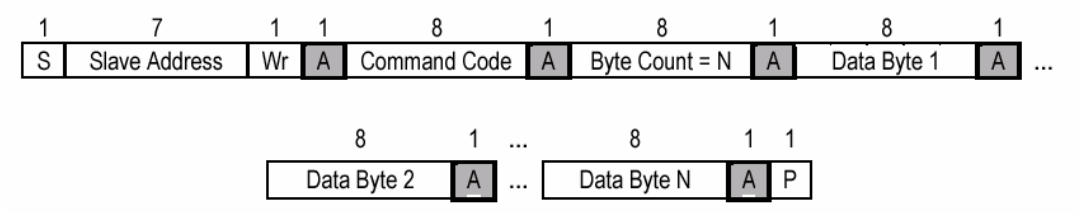
Reg14 Bit6	Reg14 Bit5	Reg14 Bit4	Reg14 Bit3	Reg14 Bit2	CPU	SDRAM	ZCLK	AGP	PCI
SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	Ratio	Ratio	Ratio	Ratio	Ratio
0	0	0	0	0	3	3	6	6	12
0	0	0	0	1	3	4	6	6	12
0	0	0	1	0	4	2	6	6	12
0	0	0	1	1	4	3	4	6	12
0	0	1	0	0	4	3	5	6	12
0	0	1	0	1	4	3	6	6	12
0	0	1	1	0	4	4	4	6	12
0	0	1	1	1	4	4	5	6	12
0	1	0	0	0	4	4	6	6	12
0	1	0	0	1	5	3	5	8	16
0	1	0	1	0	5	3	6	8	16
0	1	0	1	1	5	3	6	6	12
0	1	1	0	0	5	3	7	6	12
0	1	1	0	1	5	3	8	8	16
0	1	1	1	0	5	4	7	10	20
0	1	1	1	1	5	4	8	8	16
1	0	0	0	0	5	4	8	10	20
1	0	0	0	1	5	4	10	10	20
1	0	0	1	0	6	4	10	10	20
1	0	0	1	1	6	6	6	6	12
1	0	1	0	0	6	6	8	8	16

8. ACCESS INTERFACE

The W83194BR-645 provides I^2C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-645 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^2C address is defined at 0xD2.

Block Read and Block Write Protocol

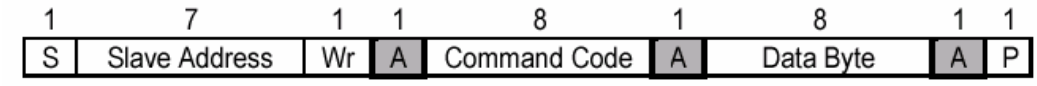
8.1 Block Write Protocol



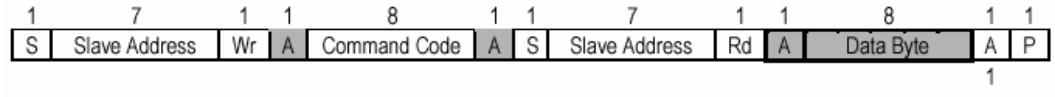
8.2 Block Read Protocol

In block mode, the command code must filled 8'h00

8.3 Byte Write Protocol



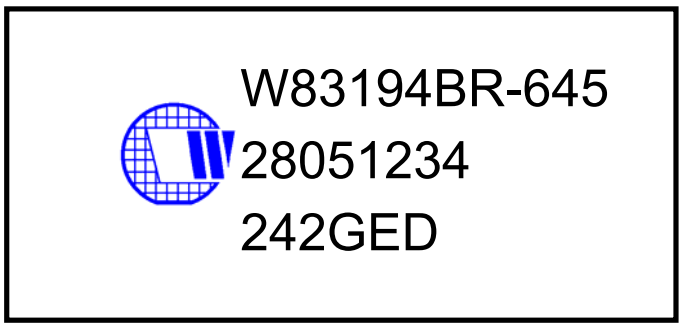
8.4 Byte Read Protocol



9. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83194BR-645	48-pin SSOP	Commercial, 0°C to +70°C

10. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-645

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 942 G E D

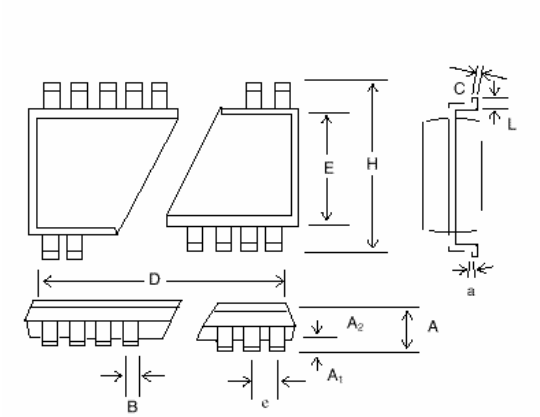
242: packages made in '2002, week 42

G: assembly house ID; O means OSE, G means GR

E: Internal use code

D: IC revision

11. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
		n.a.	All of the versions before 0.50 are for internal use.
1.0	01/08/02	n.a.	Change version and version on web site to 1.0
2.0	02/24/03	All	Update new form
2.1	4/13/2005	22	Add disclaimer

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

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