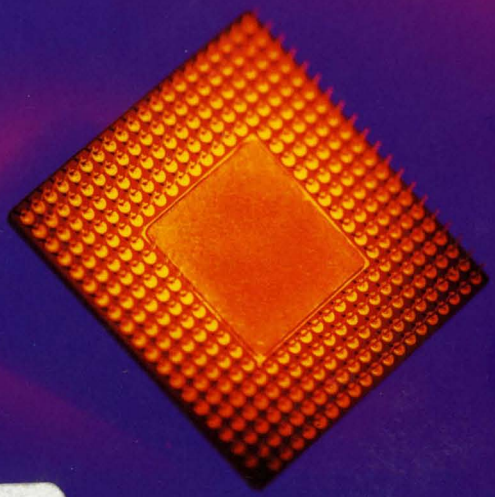
The Programmable Logic Data Book

Data Book



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The Programmable Logic Data Book

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On behalf of the employees of Xilinx, our sales representatives, our distributors, and our manufacturing partners, welcome to our 1996 Data Book, and thank you for your interest in Xilinx products and services.

As the inventor of Field Programmable Gate Array technology and the world's leading supplier of programmable logic, we would like to pledge our continuing commitment to providing you, our users, with the best possible integrated circuit components, development systems, and technical and sales support.

Over the past year, we have substantially broadened our product line with the introduction of the XC4000E, XC4000EX, XC5000, and XC6000 series of FPGAs and the XC9500 family of CPLDs. The recently-introduced XACTstep v6 and Foundation series products have set a new standard for functionality and ease-of-use in programmable logic development systems. You can expect this pace of innovation to continue, and even increase, as we maintain our leadership role in bringing leading-edge programmable logic solutions to the market.

We look forward to satisfying all of your programmable logic needs.

Sincerely,

Wim Roelandts

Chief Executive Officer

XILINX®

Section Titles

XILINX®

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An Introduction to Xilinx Products

About this Book

This Data Book provides a "snapshot in time" in its listing of IC devices and development system software available from Xilinx as of early 1996. New devices, speed grades, package types and development system products are continually being added to the Xilinx product portfolio. Users are encouraged to contact their local Xilinx sales representative and consult the WebLINX World Wide Web site (http://www.xilinx.com) and the quarterly XCELL newsletter for the latest information regarding new product availability.

The product specifications for several older Xilinx FPGA families are not included in this Data Book. This does not imply that these products are no longer available. However, for new designs, users are encouraged to use the newer products described in this book, which offer better performance at lower cost than the older technologies. Product specifications for the older products are available at WebLINX, the Xilinx site on the World Wide Web, or through your local Xilinx sales representative. These products include the following FPGA families: the XC2000, XC3000, XC3100, XC4000, XC4000A, XC4000D, and XC4000H families.

Data Sheet Categories

In order to provide the most up-to-date information, some component products included in this book may not have been fully characterized at the time of publication. In these cases, the AC and DC characteristics included in the data sheets will be marked as *Advance* or *Preliminary* information. (Not withstanding the definitions of such terms, all specifications are subject to change without notice.) These designations have the following meaning:

- **Advance** — Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, but not for final production.
- **Preliminary** — Based on preliminary characterization. Changes are possible, but not expected.
- **Final (unmarked)** — Specifications not identified as either Advance or Preliminary are to be considered final.

Data Book Contents

Chapter 1 is a general overview of the Xilinx product line, and is recommended reading for designers who are new to the field of high-density programmable logic.

Chapter 2 contains a discussion of the overall design methodology when using Xilinx programmable logic and descriptions of Xilinx development system products. This chapter is placed at the beginning of the book since these development tools are needed to design with any of the Xilinx programmable logic devices.

Chapter 3 contains the product descriptions for the Xilinx Complex Programmable Logic Device (CPLD) products, including the XC7000 and XC9000 series.

Chapter 4 includes the product descriptions for the Xilinx static-memory-based Field Programmable Gate Array (FPGA) products, including the XC3000, XC4000, XC5000, and XC6000 series.

Chapter 5 holds the product descriptions for the XC1700 family of Serial PROM devices. These Serial PROMs provide a convenient, low-cost means of storing configuration programs for the SRAM-based FPGAs described in Chapter 4.

Chapter 6 is an overview of Xilinx components appropriate for 3.3 V and mixed-voltage systems. This chapter will refer you back to the appropriate product descriptions in the earlier chapters.

Chapter 7 contains a brief overview of the HardWire product line. Detailed product specifications are available in separate Xilinx data sheets.

Chapter 8 is an overview of Xilinx High-Reliability/Military products. Detailed product specifications are available in separate Xilinx data sheets.

Chapter 9 describes the HW130 device programmer for the XC1700 series of Serial PROMs and the XC7000 and XC9000 series of CPLDs.

Chapter 10 contains a description of all the physical packages for the various IC products, including information about the thermal characteristics of those packages.

Chapter 11 discusses the testing, quality, and reliability of Xilinx component products.

Chapter 12 includes a listing of all the technical support facilities provided by Xilinx.

Chapter 13 contains additional information about Xilinx components that is not provided in the product specifications of the earlier chapters. This includes some additional electrical parameters that are not in the product specifications because they are not part of the manufacturing test program for the particular device, but may be of interest to the user. Also included in this chapter is a discussion of the

JTAG boundary test scan logic found in several Xilinx component families.

The final two sections contain an index to the topics included in this Data Book and a listing of Xilinx sales offices, sales representatives, and distributors.

About the Company

Xilinx, Inc., offers the industry's broadest selection of programmable logic devices. With 1995 revenues of over $500 million, Xilinx is the world's largest supplier of programmable logic, and the market leader in Field Programmable Gate Arrays (FPGAs).

Xilinx was founded in 1984, based on the revolutionary idea of combining the logic density and versatility of gate arrays with the time-to-market advantages and convenience of user-programmable standard parts. One year later, Xilinx introduced the world's first Field Programmable Gate Array. Since then, through a combination of architectural and manufacturing process improvements, the company has continually increased device performance, in terms of capacity, speed, and ease-of-use, while lowering costs.

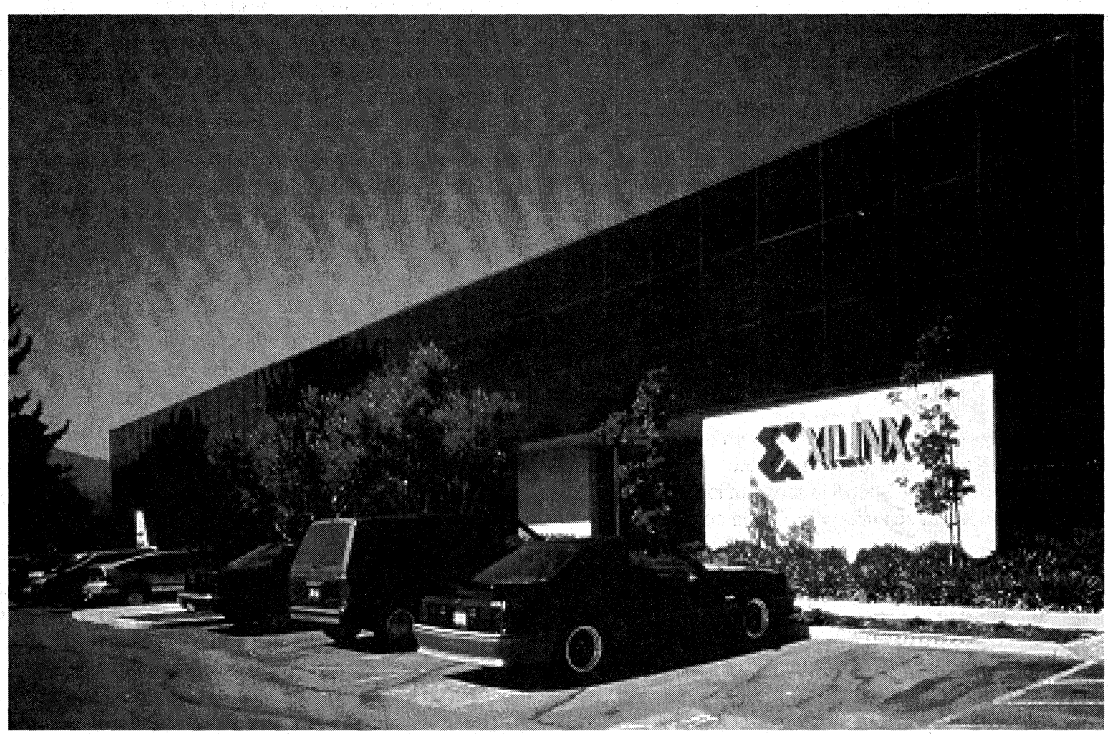
In 1992, Xilinx expanded its product line to include advanced Complex Programmable Logic Devices (CPLDs, also known as EPLDs). For the user, CPLDs are an attractive complement to FPGAs, offering simpler design software and more predictable timing.

As the market leader in one of the fastest growing segments of the semiconductor industry, Xilinx strategy is to focus its resources on creating new ICs and development system software, providing world-class technical support, developing markets, and building a diverse customer base across a broad range of geographic and end-use application segments. The company has avoided the large capital commitment and overhead burden associated with sole ownership and operation of a wafer fabrication facility. Instead, Xilinx has established alliances with several high-volume, state-of-the-art CMOS IC manufacturers. Using standard, high-volume processes assures low manufacturing costs, produces programmable logic devices with well-established reliability, and provides for early access to advances in CMOS processing technology.

Xilinx headquarters are located in San Jose, California. The company markets its products worldwide through a network of direct sales offices, manufacturers' representatives, and distributors (as listed in the back of this book). The company has representatives and distributors in over 38 countries.

Product Line Overview

Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs) can be used in virtually any digital logic system. Over 35 million Xilinx components have been used in a wide variety of end-equipment applications, ranging from supercomputers to hand-held



instruments, from central office switches to centrifuges, and from missile guidance systems to guitar synthesizers.

Xilinx achieved its leading position through a continuing commitment to provide a complete product solution. This encompasses a focus on all three critical areas of the high-density programmable solution "triangle": components (silicon), software, and service (Figure 1).

Programmable Logic vs. Gate Arrays

Xilinx programmable logic devices provide the benefits of high integration levels without the risks or expenses of semi-custom and custom IC development. Some of the benefits of programmable logic as versus mask-programmed gate arrays are briefly discussed below.

Faster Design and Verification

Xilinx FPGAs and CPLDs can be designed and verified quickly while the same process requires several weeks with gate arrays. There are no non-recurring engineering (NRE) costs, no test vectors to generate, and no delay while waiting for prototypes to be manufactured.

Design Changes without Penalty

Because the devices are software-configured and user-programmed, modifications are much less risky and can be made anytime - in a manner of minutes or hours, as opposed to the weeks it would take with a gate array. This results in significant cost savings in design and production.

Shortest Time-to-Market

When designing with Xilinx programmable logic, time-to-market is measured in days or a few weeks, not the months often required when using gate arrays. A study by market research firm McKinsey & Co. concluded that a six-month delay in getting to market can cost a product one-third of its lifetime potential profit. With mask-programmed gate arrays, design iterations can easily add that much time, and more, to a product schedule.

Once the decision has been made to use Xilinx programmable logic, a choice must be made from a number of product families, device options, and product types. The information in the product selection matrices that follow can help guide that selection; detailed product specifications are available in subsequent chapters of this book. Since many component products are available in common packages with common footprints, designs often can be migrated to higher or lower density devices, or even across some product families, without any printed circuit board changes. Design ideas, represented in text or schematic format, are converted into a configuration data file for an FPGA or CPLD device using the Xilinx XACT*step* development software running on a PC or workstation.

Component Products

Xilinx offers the broadest line of programmable logic devices available today, with hundreds of products featuring various combinations of architectures, logic densities, package types, and speed grades in commercial, industrial, and military grades. This breadth of product offerings allows the selection of the programmable logic device that is best suited for the target application.

Xilinx programmable logic offerings include several families of reprogrammable FPGAs, one-time-programmable FPGAs, EPROM-based CPLDs, and FLASH-memory-based CPLDs (Figure 2). HardWire devices are mask-programmed versions of the reprogrammable FPGAs, and provide a transparent, no-risk migration path to lower-cost devices for high-volume, stable designs. Additionally, a family of Serial PROM devices is available to store configuration programs for the reprogrammable FPGA devices.

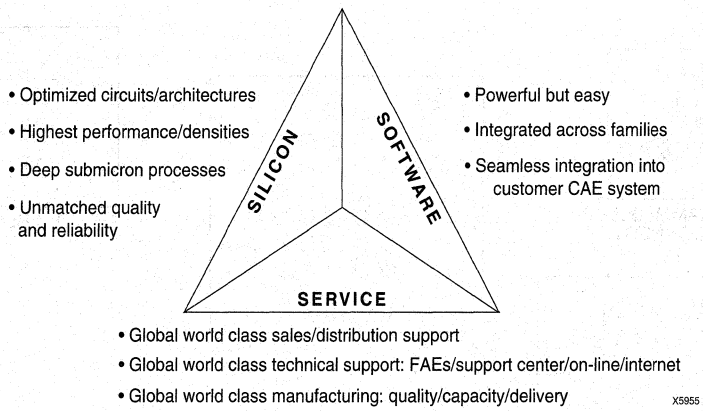


Figure 1: The Xilinx Programmable Solution Triangle

Many devices are available in military temperature range and/or MIL-STD-883B versions, for high-reliability and military applications.

Field Programmable Gate Arrays (FPGAs)

FPGA devices feature a gate-array-like architecture, with a matrix of logic cells surrounded by a periphery of I/O cells, as diagrammed in Figure 3. Segments of metal interconnect can be linked in an arbitrary manner by programmable switches to form the desired signal nets between the cells.

FPGAs combine an abundance of logic gates, registers, and I/Os with fast system speed. Xilinx offers several families of reprogrammable, static-memory-based (SRAM-based) FPGAs, including the XC2000, XC3000, XC4000, XC5000, and XC6000 series.

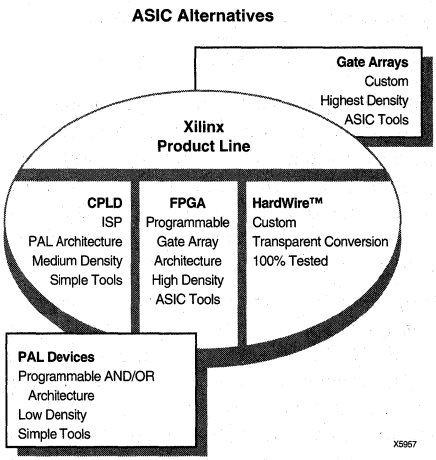


Figure 2: Application-Specific IC Products

Complex Programmable Logic Devices (CPLDs)

Designers more comfortable with the speed, design simplicity, and predictability of PALs may prefer CPLD devices. Conceptually, CPLDs consist of multiple PAL-like function blocks that can be interconnected through a switch matrix (Figure 4). The Xilinx XC7000 CPLD series is based on EPROM technology. The new XC9000 CPLD series features 5V in-system programmable FLASH technology, and, like most of the FPGA families, includes built-in JTAG boundary scan test logic.

HardWire devices

HardWire devices are masked-programmed versions of the SRAM-based FPGAs. The HardWire products provide an easy, transparent migration path to a cost-reduced device without the engineering burden associated with conventional gate array re-design. The HardWire gate array is architecturally identical to its FPGA counterpart, but the programmable elements in the FPGA are replaced with fixed metal connections. The resulting die is considerably smaller, with a correspondingly lower cost. Using proprietary automatic test vector generation software and patented test logic, Xilinx guarantees over 95% fault coverage, while eliminating the need for user-generated test vectors. The mask and test programs are generated automatically by Xilinx from the user's existing FPGA design file.

Serial PROMs

The XC1700 family features one-time programmable serial PROMs ranging in density from about 18,000 bits to over 260,000 bits. These serial PROMs are an easy-to-use, cost-effective method for storing configuration data for the SRAM-based FPGAs.

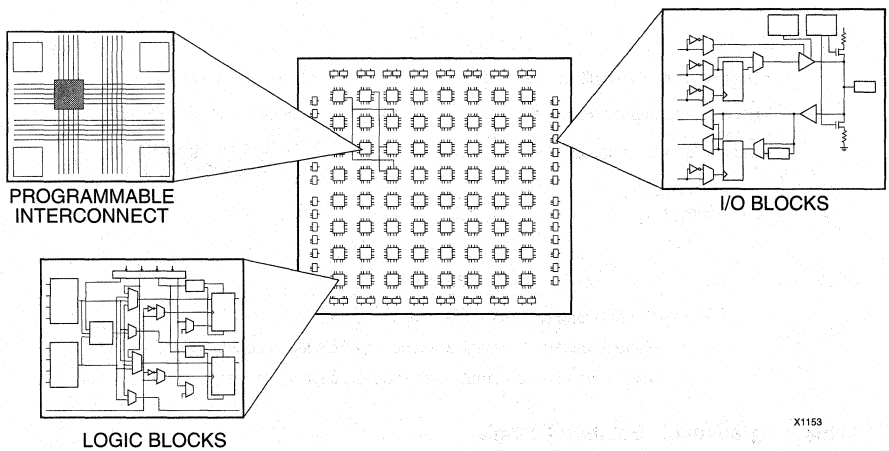


Figure 3: FPGA Architecture

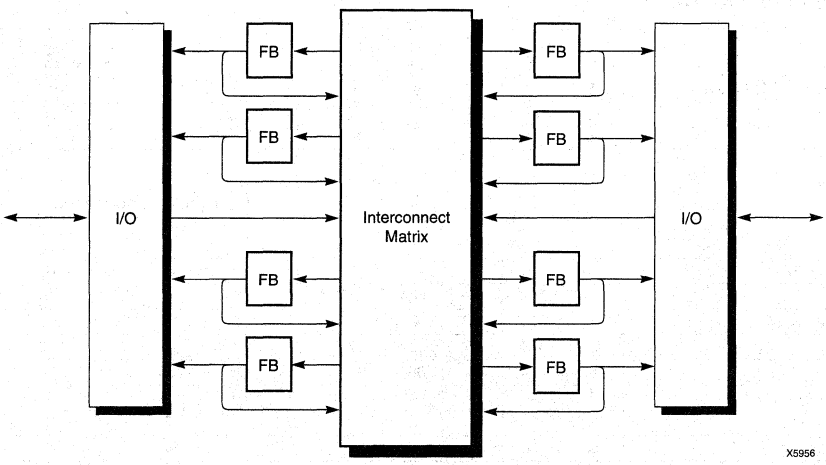


Figure 4: CPLD Architecture

High-Reliability Devices

Xilinx was the first company to offer high-reliability FPGAs by introducing MIL-STD-883B qualified XC2000 and XC3000 series devices in 1989. MIL-STD-883B members of the XC4000 FPGA series also are available, and qualified versions of additional Xilinx families are in development. The product line also includes Standard Microcircuit Drawing (SMD) versions of several families. Some Xilinx devices are available in tested die form through arrangements with manufacturing partners.

Development System Products

Xilinx offers a complete software environment for the implementation of logic designs in Xilinx programmable logic devices. This environment, called XACT*step*, combines powerful technology with a flexible, easy-to-use graphical interface to help users achieve the best possible designs, regardless of experience level. The user has a wide range of choices between a fully-automatic implementation and detailed involvement in the layout process. The XACT*step* system provides all the implementation tools required to design with Xilinx logic devices, including the following:

- libraries and interfaces for popular schematic editors, logic synthesis tools, and simulators
- design manager/flow engine
- module generator
- map, place, and route compilation software
- graphical floorplanner
- static timing analyzer
- hardware debugger

Xilinx is committed to an "open system" approach to front-end design creation, synthesis, and verification. Xilinx devices are supported by the broadest number of EDA vendors and synthesis vendors in the industry. Supported platforms include the ubiquitous PC and several popular workstations.

Service

Providing global, world-class manufacturing, technical support, and sales/distribution support is an essential foundation of the Xilinx product strategy. Xilinx manufacturing facilities have earned ISO9002 certification, and Xilinx quality and reliability achievements are among the world's best - not just for programmable logic suppliers, but among all semiconductor companies. Comprehensive technical support facilities include training courses, extensive product documentation and application notes, a quarterly technical newsletter, automated document servers, a technical bulletin board, the WebLINX World Wide Web site, technical support hotlines, and a cadre of Field Application Engineers. Sales support is provided by a worldwide network of representatives and distributors.

FPGA Product Selection Matrix

	DEVICES	XC3000 Series	XC3020A/L	XC3030A/L	XC3042A/L	XC3064A/L	XC3090A/L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC3142L	XC3190L
	KEY FEATURES		Low Cost/ Low Power					Highest Performance						Low Voltage (3.3 V) Highest Performance	
DENSITY		Max Logic Gates (K)	1.5	2	3	5	6	1.5	2	3	5	6	8	3	6
		Max RAM Bits	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
		Typical Gate Range (K)	1-1.5	1.5-2	2-3	4-5	5-6	1-1.5	1-2	2-3	4-5	5-6	7-8	2-3	5-6
		CLBs	64	100	144	224	320	64	100	144	224	320	484	144	320
		Flip-Flops	256	360	480	688	928	256	360	480	688	928	1320	480	928
FEATURES		Output Drive (mA)	4	4	4	4	4	8	8	8	8	8	8	4	4
		JTAG (IEEE 1149.1)	N	N	N	N	N	N	N	N	N	N	N	N	N
		Dedicated Arithmetic	N	N	N	N	N	N	N	N	N	N	N	N	N
		Quiescent Current (mA)	0.5/ 0.02	0.5/ 0.02	0.5/ 0.02	0.5/ 0.02	0.5/ 0.02	8	8	8	8	8	8	1.5	1.5
PERFORMANCE		Fastest Speed Grade	-6/-8	-6/-8	-6/-8	-6/-8	-6/-8	-09	-09	-09	-09	-09	-09	-2	-2
		Shift Register (MHz)	124/69	124/69	124/69	124/69	124/69	312	312	312	312	312	312	256	256
		Small State Machine (MHz)	42/23	42/23	42/23	42/23	42/23	112	112	112	112	112	112	68	68
		Large State Machine (MHz)	21/14	21/14	21/14	21/14	21/14	55	55	55	55	55	55	33	33
		4-Bit Multiply-Accumulator (MHz)	20/12	20/12	20/12	20/12	20/12	51	51	51	51	51	51	33	33
		16-Bit Accumulator (MHz)	25/15	25/15	25/15	25/15	25/15	58	58	58	58	58	58	41	41
		Address Map Decoder (MHz)	52/27	52/27	52/27	52/27	52/27	127	127	127	127	127	127	84	84
		Data Path (MHz)	147/86	147/86	147/86	147/86	147/86	335	335	335	335	335	335	84	84
		Counter Timer (MHz)	37/23	37/23	37/23	37/23	37/23	81	81	81	81	81	81	56	56
		16-Bit Non Loadable Counter (MHz)	135/81	135/81	135/81	135/81	135/81	370	370	370	370	370	370	323	323
		16-Bit Loadable Binary Up Counter (MHz)	39/25	39/25	39/25	39/25	39/25	91	91	91	91	91	91	63	63
		16-Bit Loadable Prescaled Counter (MHz)	100/59	100/59	100/59	100/59	100/59	228	228	228	228	228	228	154	154
		RAM Read Modify Write (MHz)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
		Pad to Setup (ns)	14/12	14/12	14/12	14/12	14/12	2.5	2.5	2.5	2.5	2.5	2.5	4	4
		Clock to Pad (ns)	7/18	7/18	7/18	7/18	7/18	4	4	4	4	4	4	5	5
		Combinatorial Pad to Pad (ns)	14/25	14/25	14/25	14/25	14/25	6	6	6	6	6	6	8	8

FPGA Product Selection Matrix (continued)

DEVICES	XC4000 Series	XC4003E*	XC4005E*	XC4006E*	XC4008E*	XC4010E*	XC4013E*	XC4020E*	XC4025E*	XC4028EX	XC4036EX	XC4044EX	XC4052XL	XC4062XL	XC4003H	XC4005H	XC4005L	XC4010L	XC4013L
KEY FEATURES		High Density High Performance Select-RAM™ Memory													High I/O		Low Voltage (3 V)		
DENSITY	Max Logic Gates, (no RAM) (K)	3	5	6	8	10	13	20	25	28	36	44	52	62	3	5	5	10	13
	Max RAM Bits (no Logic)	3200	6272	8192	10368	12800	18342	25088	32768	32768	41472	51200	61952	73728	3200	6272	6272	12800	18432
	Typical Gate Range (Logic and RAM) (K)	2-5	3-9	4-12	6-15	7-20	10-30	13-40	15-45	18-50	22-65	27-80	33-100	40-130	2-5	3-9	3-9	7-20	10-30
	CLBs	100	196	256	324	400	576	784	1024	1024	1296	1600	1936	2304	100	196	196	400	576
	Flip-Flops	360	616	768	936	1120	1536	2016	2560	2560	3168	3840	4576	5376	200	392	616	1120	1536
FEATURES	Output Drive (mA)	12	12	12	12	12	12	12	12	12	12	12	12	12	24	24	4	4	4
	JTAG (IEEE 1149.1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	Dedicated Arithmetic	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	Quiescent Current (mA)	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	0.05	0.05	0.05
PERFORMANCE	Fastest Speed Grade	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-5	-5	CONTACT FACTORY		
	Shift Register (MHz)	190	190	190	190	190	190	190	190	190	190	190	190	190	105	105			
	Small State Machine (MHz)	69	69	69	69	69	69	69	69	69	69	69	69	69	48	48			
	Large State Machine (MHz)	43	43	43	43	43	43	43	43	43	43	43	43	43	37	37			
	4-Bit Multiply-Accumulator (MHz)	39	39	39	39	39	39	39	39	39	39	39	39	39	20	20			
	16-Bit Accumulator (MHz)	65	65	65	65	65	65	65	65	65	65	65	65	65	36	36			
	Address Map Decoder (MHz)	71	71	71	71	71	71	71	71	71	71	71	71	71	43	43			
	Data Path (MHz)	156	156	156	156	156	156	156	156	156	156	156	156	156	105	105			
	Counter Timer (MHz)	117	117	117	117	117	117	117	117	117	117	117	117	117	58	58			
	16-Bit Non Loadable Counter (MHz)	180	180	180	180	180	180	180	180	180	180	180	180	180	95	95			
	16-Bit Loadable Binary Up Counter (MHz)	87	87	87	87	87	87	87	87	87	87	87	87	87	42	42			
	16-Bit Loadable Prescaled Counter (MHz)	115	115	115	115	115	115	115	115	115	115	115	115	115	63	63			
	RAM Read Modify Write (MHz)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	50	50			
	Pad to Setup (ns)	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	7	7			
	Clock to Pad (ns)	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	10	10			
	Combinatorial Pad to Pad (ns)	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	5	5			

*Usable gates assume 20% of CLBs used as RAM

DEVICES	XC5000, XC6000 Series	XC5202	XC5204	XC5206	XC5210	XC5215	XC6209	XC6216	XC6236	XC6264
KEY FEATURES		High Density Low Cost					µP Interface Fast Configuration			
DENSITY	Max Logic Gates (K)	3	6	10	16	23	13	24	55	100
	Max RAM Bits	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	Typical Gate Range (K)	2-3	4-6	6-10	10-16	15-23	9-13	16-24	36-55	64-100
	CLBs/Logic Cells	64	120	196	324	484	2304	4096	9216	16384
	Flip-Flops	256	480	784	1296	1936	2304	4096	9216	16384
FEATURES	Output Drive (mA)	8	8	8	8	8	8	8	8	8
	JTAG (IEEE 1149.1)	Y	Y	Y	Y	Y	N	N	N	N
	Dedicated Arithmetic	Y	Y	Y	Y	Y	N	N	N	N
	Quiescent Current (mA)	15	15	15	15	15	–	–	–	–
PERFORMANCE	Fastest Speed Grade	-4	-4	-4	-4	-4	CONTACT FACTORY			
	Shift Register (MHz)	83	83	83	83	83				
	Small State Machine (MHz)	50	50	50	50	50				
	Large State Machine (MHz)	35	35	35	35	35				
	4-Bit Multiply-Accumulator (MHz)	24	24	24	24	24				
	16-Bit Accumulator (MHz)	60	60	60	60	60				
	Address Map Decoder (MHz)	69	69	69	69	69				
	Data Path (MHz)	83	83	83	83	83				
	Counter Timer (MHz)	59	59	59	59	59				
	16-Bit Non Loadable Counter (MHz)	N/A	N/A	N/A	N/A	N/A				
	16-Bit Loadable Binary Up Counter (MHz)	58	58	58	58	58				
	16-Bit Loadable Prescaled Counter (MHz)	83	83	83	83	83				
	RAM Read Modify Write (MHz)	N/A	N/A	N/A	N/A	N/A				
	Pad to Setup (ns)	6.6	6.6	6.6	6.6	6.6				
	Clock to Pad (ns)	14.2	14.2	14.2	14.2	14.2				
	Combinatorial Pad to Pad (ns)	15	15	15	15	15				

*Usable gates assume 20% of CLBs used as RAM

CPLD Product Selection Matrix

	CPLD Families	XC7318	XC7336	XC7336Q	XC7354	XC7372	XC73108	XC73144	XC9536	XC9572	XC95108	XC95144	XC95180	XC95216	XC95288	XC95432	XC95576
DEVICES																	
KEY FEATURES		100% Routable 100% Utilization 5 ns T_{PD}							JTAG 5 V ISP 3 V or 5 V I/O								
DENSITY	Gates (K)	0.4	0.8	0.8	1.5	1.9	3.0	3.8	0.8	1.6	2.4	3.2	4.0	4.8	6.4	9.6	12.8
	Macrocells	18	36	36	54	72	108	144	36	72	108	144	180	216	288	432	576
	Flip-Flops	18	36	36	108	126	198	234	36	72	108	144	180	216	288	432	576
FEATURES	Output Drive (mA)	24	24	24	24	24	24	24	24	24	24	24	24	24	24	24	24
	JTAG (IEEE 1149.1)	N	N	N	N	N	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y
	Dedicated Arithmetic	N	N	N	Y	Y	Y	Y	N	N	N	N	N	N	N	N	N
	Quiescent Current (mA)	90	126	50	140	187	227	250	–	–	140	–	–	–	–	–	–
PERFORMANCE	Fastest Speed Grade	-5	-5	-10	-7	-7	-7	-7	-5	-7	-7	-7	-10	-10	-10	–	–
	Shift Register (MHz)	125	125		95	95	95	95	CONTACT FACTORY								
	Small State Machine (MHz)	108	108		95	95	95	95									
	Large State Machine (MHz)	102	102		95	95	95	95									
	4-Bit Multiply-Accumulator (MHz)	46	46		52	52	52	52									
	16-Bit Accumulator (MHz)	40	40		63	63	63	63									
	Address Map Decoder (MHz)	108	108		95	95	95	95									
	Data Path (MHz)	125	125		95	95	95	95									
	Counter Timer (MHz)	94	94		47	47	47	47									
	16-Bit Non Loadable Counter (MHz)	125	125		95	95	95	95									
	16-Bit Loadable Binary Up Counter (MHz)	125	125		95	95	95	95									
	16-Bit Loadable Prescaled Counter (MHz)	125	125		95	95	95	95									
	RAM Read Modify Write (MHz)	N/A	N/A		N/A	N/A	N/A	N/A									
	Pad to Setup (ns)	3.5	3.5		4	4	4	4									
	Clock to Pad (ns)	4.5	4.5		7	7	7	7									
	Combinatorial Pad to Pad (ns)	5	5		7	7	7	7									

		Number of Pins																
PACKAGE OPTIONS AND USER I/O	MAX I/O		38	38	38	58	84	120	156	34	72	108	133	168	168	192	232	232
Package (Code)	PLCC (PC)	44	38	38	38	38				34								
	PQFP (PQ)	44	38	38	38					34								
	CLCC (WC)	44		38	38	38												
	VQFP (VQ)	44			38													
	PLCC (PC)	68				58	57											
	CLCC (WC)	68				58	57											
	PLCC (PC)	84					72	72			69	69						
	CLCC (WC)	84					72	72										
	PGC (PG)	84																
	PQFP (PQ)	100					84	84			72	81	81					
	TQFP (TQ)	100									72	81						
	PGA (PG)	144						120										
	PQFP (PQ)	160						120	136			108	133	133	133			
	HQFP (HQ)	208												168	168	168		
	BGA (BG)	225						120	156									
	HQFP (HQ)	304														192	232	232

Development System Products
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Development Systems Products Overview

Bundled Packages Product Descriptions

Individual Product Descriptions

XACT*step:* Accelerating Your Productivity

The newest version of the XACT development system, XACT*step*, started shipping in the fourth quarter of 1995.

XACT*step* software features a revolutionary combination of power and ease-of-use to provide accelerated learning curves, short implementation cycles, and faster design debug. This high-productivity environment contains six new productivity tools that are easily accessible through graphical tool bars, icons and pop-up menus. They support the complete spectrum of programmable logic design methodology from fully automatic to hand-crafted.

All the tools in XACT*step* feature a new graphical user interface (GUI). On the PC, the GUI is fully Microsoft Windows compliant.

With this new GUI, all programs are executed from tool bars and icons. Tool tips provide instant descriptions and on-line help is available for more in-depth information. Report browsers present message files with plain English titles and allow simultaneous viewing of multiple documents.

Six Powerful New Tools

- The new Design Manager provides a complete project management environment for a wide range of families. It provides version control, device re-targeting and design re-use.
- The configurable Flow Engine lets designers choose the amount of control they want over the implementation process. They can choose a fully automatic flow or set break points that allow analysis and optimization of results before proceeding to the next step.
- XACT*step* contains the industry's first graphically-based hierarchical Floorplanner. This tool provides techniques that have proven to be extremely valuable to gate array and custom silicon designers. Using floorplanning, it is easy to achieve hand-crafted levels of performance and density without resorting to low-level manual techniques. Floorplanning is valuable for any design that has a high degree of structure or a large number of gates. It also allows optimization of specialized structures like Xilinx unique high-speed distributed RAM and three-state internal bus features.
- The new interactive Timing Analyzer makes it easy to quickly determine a design's performance by generating custom timing reports. Using pop-up menus, it is quickly configured to show the delay along a specific path or group of paths. It also shows the delay along all paths of a certain type or those associated with a specific clock signal. In addition, the Timing Analyzer automatically compares the design's actual performance to XACT-Performance goals and shows the estimated maximum frequency for each clock in the design.
- The Hardware Debugger allows verification of configuration data and viewing of internal signal activity. It takes advantage of the reprogrammability of SRAM-based devices by configuring the FPGA in-circuit using a cable connected to a host PC or workstation. After configuring the device, bitstream data is read back through the cable for automatic verification.
  While the device is running, an unlimited number of internal nodes can be probed and displayed in a waveform window.
- The new PROM Formatter in XACT*step* assists the designer in creating PROM programming files. This tool chooses the best PROM size or automatically splits the data into multiple files if multiple PROMs are required. It supports serial and byte-wide PROMs in four different formats. If the target system uses the daisy chain capability of the Xilinx FPGA, the PROM formatter graphically creates the load order and verifies the load sequence.

The Xilinx Design Manager—Simplifies the Design Flow

- Source and revision control
- Permits running all Xilinx software from menus
- Automates design translation via XMake facility
- Provides on-line help for all menus, programs and options

Flow Engine

- Automatically invokes all implementation programs as required to compile a design into an FPGA or CPLD
- Supports hierarchically-structured designs

Extensive On-line Help

- The Design Manager contains on-line Help for
  Every menu
  Every program
  Every program option
  Design-flow suggestions

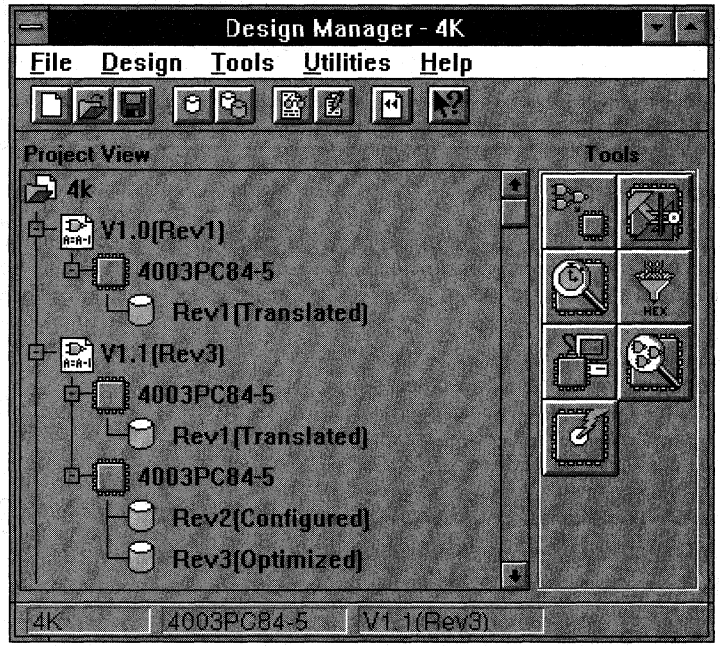


Figure 1: Design Manager Main Window

Design Flow Overview

This section describes the Xilinx Automated CAE Tools (XACT) design environment for Xilinx FPGA and CPLD devices.

High-density programmable logic has created unique requirements for CAE software; the tools must deliver the ease-of-design and fast time-to-market benefits that have popularized FPGA and CPLD technologies, must be capable of implementing high-density logic designs on an engineer's desktop system, and must be easy-to-use and compatible with the user's existing design environment.

In order to meet those needs, Xilinx offers a variety of development system products optimized to support the Xilinx FPGA and CPLD architectures. Available products include state-of-the-art design implementation software, libraries and interfaces to popular schematic editors, synthesis and timing simulators, and behavioral-based design entry tools. All Xilinx development system software is integrated under the Xilinx Design Manager, providing designers with a common user interface regardless of their choice of device architecture and tools.

As with other logic technologies, the basic methodology for FPGA design consists of three interrelated steps: entry, implementation, and verification. (Figure 2 - Figure 4). The design process is iterative, returning to the design entry phase for correction and optimization. Popular generic tools are used for entry and simulation (for example, Viewlogic System's PROcapture schematic editor and PROsim simulator), but architecture-specific tools are needed for implementation.

Design Entry

Schematic editors and synthesis are the most-popular methodologies for design entry. FPGA/CPLD symbol libraries and netlist interfaces are available for schematic editors from vendors such as Viewlogic, OrCAD, Mentor Graphics, and Cadence. These libraries reflect the wide variety of logic functions that can be implemented in FPGA/CPLD devices.

Behavioral-oriented design entry methods, including Boolean equations and state-machine descriptions, are supported by the Xilinx ABEL and LogiBloxs products, as well as a number of products from CAE vendors such as Data I/O, Logical Devices, MINC, and ISDATA.

As the density and complexity of FPGA and CPLD designs increase to 10,000 gates and beyond, gate-level entry tools often are cumbersome, and the use of logic synthesis and high-level description languages (HDLs), such as VHDL and Verilog, can raise designer productivity. The use of HDLs requires synthesis tools that effectively compile designs for the target architecture. Xilinx offers interfaces for synthesis tools from Synopsys. Other CAE vendors, such as Mentor Graphics, Cadence Design Systems, Viewlogic, and Exemplar Logic, also offer synthesis tools tailored for the Xilinx device architectures.

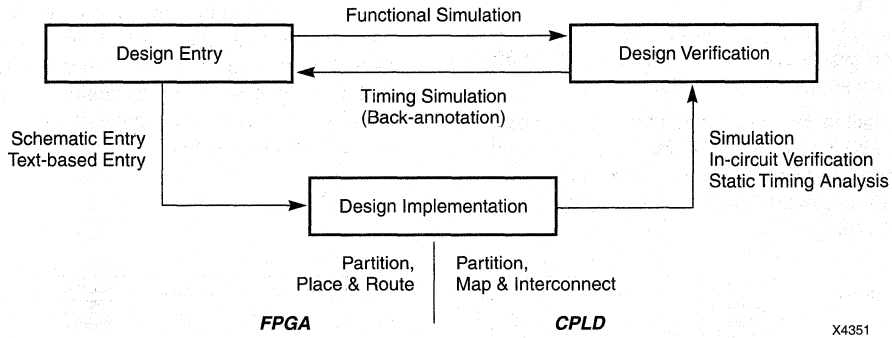


Figure 2: FPGA/CPLD Design Flow

Many engineers prefer visually oriented design-entry techniques over text-based HDLs. The benefits of HDLs are provided to these designers with tools that provide high-level design constructs in a symbolic format compatible with graphics-based schematic editors. X-BLOX is a graphics-based high-level language that allows designers to use a schematic editor to enter designs as a set of generic modules. The X-BLOX compiler optimizes the modules for the target device architecture, automatically choosing the appropriate architectural resources for each function.

The XACT*step* design environment supports hierarchical design entry, with top-level drawings defining the major functional blocks, and lower-level descriptions defining the logic in each block. The implementation tools automatically combine the hierarchical elements of a design. Different hierarchical elements can be specified with different design entry tools, allowing the use of the most convenient entry method for each portion of the design. In this type of 'mixed-mode' design entry, designers can intermix schematic, text, gate-level and behavioral-level design, permitting the re-use of previously designed modules and easing the transition to higher-level design methodologies.

Design Implementation

After the design is entered, implementation tools map the logic into the resources of the target device architecture, determine an optimal placement of the logic, and select the routing channels that connect the logic and I/O blocks. Xilinx design implementation tools apply a very high degree of automation to these tasks. A design compilation utility automatically retrieves the design's input files and performs all the necessary steps to create the CPLD or FPGA configuration program.

For demanding applications, the user can exercise various degrees of control over the automated implementation process using auto-interactive tools and techniques. Optionally, user-designated partitioning, placement, and routing information can be specified as part of the design entry process (typically, right on the schematic). The implementation of highly structured designs can greatly benefit from the basic floorplanning techniques familiar to designers of large gate arrays.

For Xilinx FPGAs, the automatic tools are complemented by an interactive, graphics-based editor that allows users to view and manipulate a model of the logic and routing resources inside the FPGA device, providing the user with visibility into the implementation of the design.

Design Verification

Verification of FPGA/CPLD designs typically involves a combination of in-circuit testing, simulation, and static timing analysis. The user-programmable nature of these devices allows designs to be tested immediately in the target application. For Xilinx FPGAs and in-system-programmable CPLDs, download cables are provided that allow for the direct downloading of a bitstream from a PC or workstation to an FPGA or CPLD device on a target board. Demonstration/prototyping boards are also available. The implementation tools include back-annotation to provide post-layout timing of implemented designs to support timing simulation. A static timing analyzer can be used to examine a design's logic and timing to calculate the performance along signal paths, identify possible race conditions, and detect set-up and hold-time violations. Timing analyzers do not require the user to generate input stimulus patterns or test vectors.

Xilinx software is available both in bundled packages containing front end implementation tools and with integrated kits to enable plug and play with 3rd party EDA environments. New enhancements are constantly being developed, and update services are available to ensure timely access to the latest versions.

Xilinx Software on CD-ROM

Xilinx software and updates are now delivered on CD-ROM for the PC and workstations (Sun, HP700 and RS6000 Series). Here are some of the benefits:

- Faster Installation: No more wasted time, feeding floppy after floppy into the PC. No more waiting for workstation tapes to spin, looking for the proper data. Installing or updating Xilinx software is as easy as popping in one CD-ROM disk.
- Software Compatibility: New install utilities monitor the software configuration, ensure executable version compatibility, and update only the necessary files to keep the software up-to-date. Archiving old versions of XACT software is as easy as storing one CD-ROM disk.
- On-line documentation, tutorials, application notes, and product demonstrations.

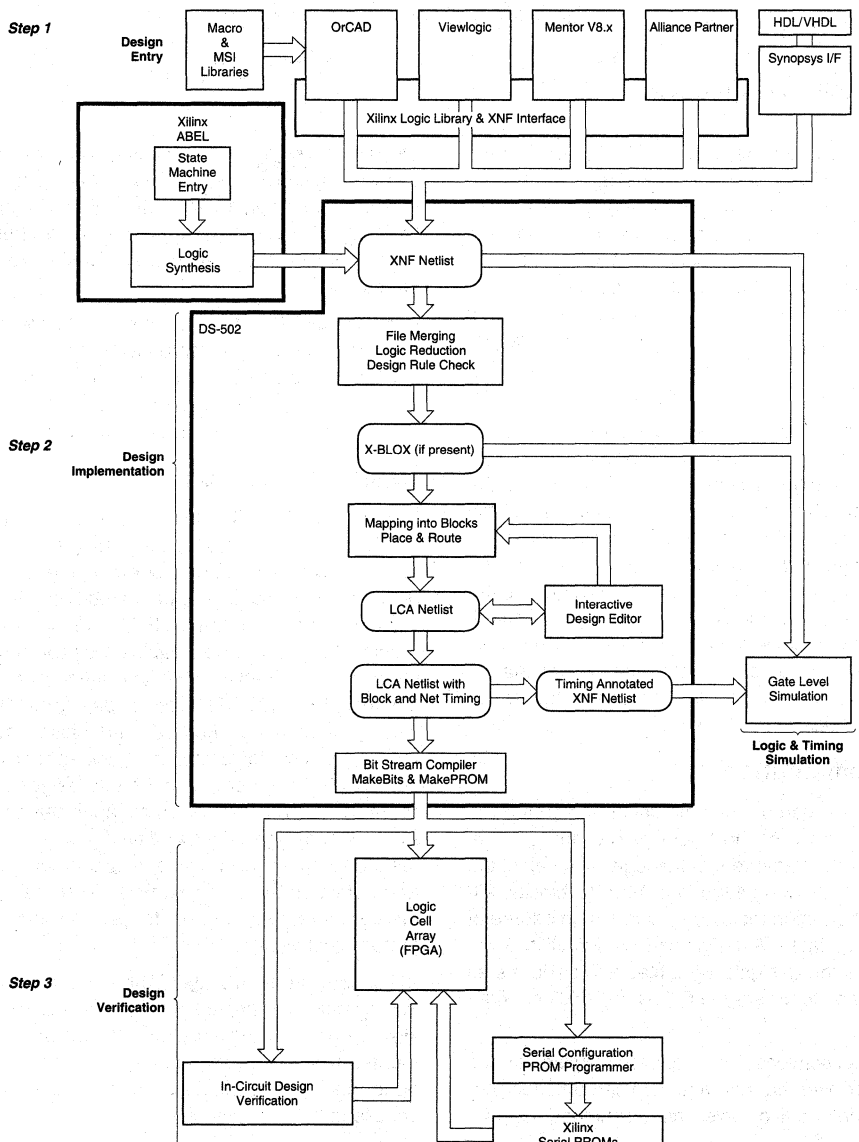


Figure 3: Detailed FPGA Design Flow

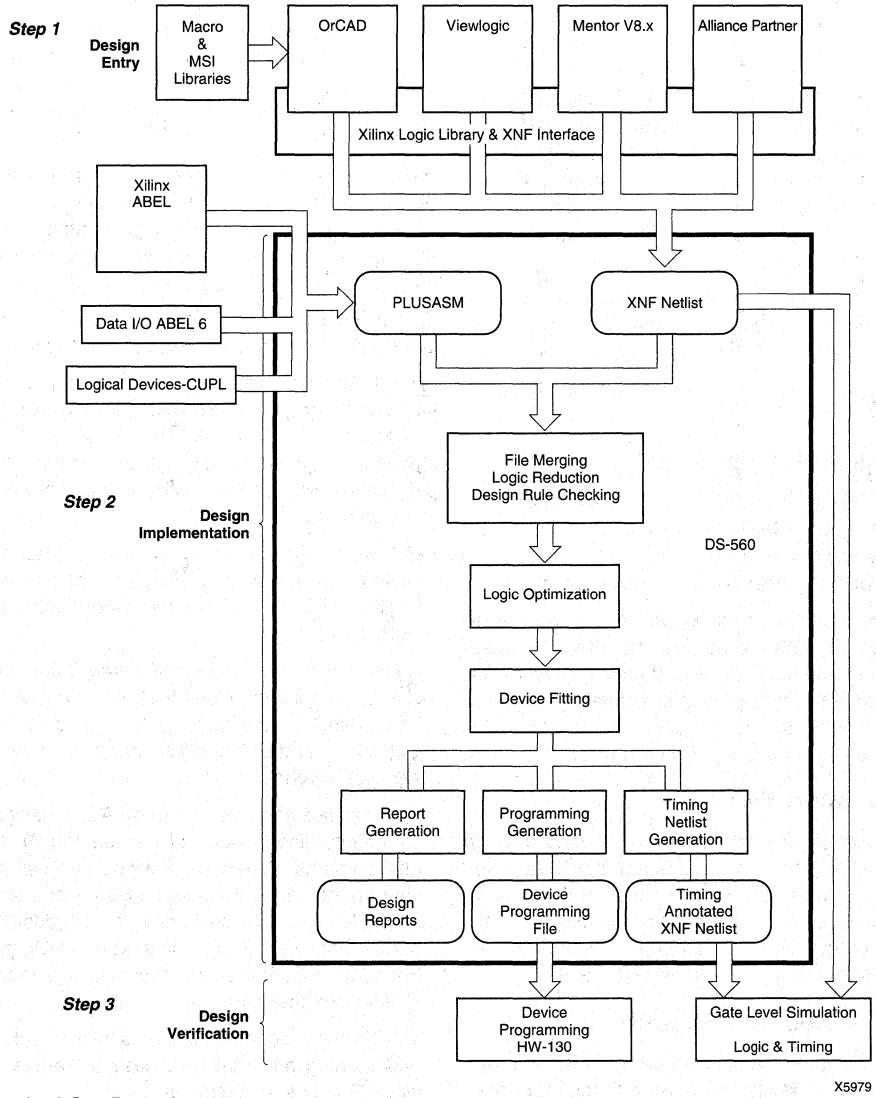


Figure 4: Detailed CPLD Design Flow

Support and Update Services

Software Updates

A major focus of Xilinx engineering is continual improvement of the Xact*step* Development System Software. This is accomplished by developing new features to improve your design productivity, and adding new technologies to give you access to the latest Xilinx products. If you are on maintenance, you will receive new revisions containing enhancements to the software products you have licensed from Xilinx.

Base Product Updates

The Xact*step* Base packages do not come with a standard one-year update contract. When Xilinx releases a new version of software, customers will be notified and may purchase the new version update at the listed price.

Online Documentation

Xilinx continually updates documentation to reflect changes to the Development System Software. As part of the update service, you receive new online documentation with each update.

Technical Support Hotline

The Technical Telephone Support Hotline provides you with toll-free telephone access to trained software technical support engineers. (See Chapter 13.) Expertise provided includes most major third-party interfaces including Viewlogic, OrCAD, Mentor Graphics, Xilinx ABEL, Synopsys, and Cadence. Additionally, Xilinx core expertise is available for both FPGA and CPLD product lines covering place and route, X-BLOX, XACT Performance, XDelay, configuration and component issues.

This support service for problem resolution assistance is available between 8:00 am and 5:00 pm Pacific Standard Time, Monday through Friday (except holidays).

For service outside USA, please contact your local representative.

Xilinx Technical Bulletin Board

The Xilinx Technical Bulletin Board allows electronic exchange of information with technical support engineers. With this service you can upload your design data making it available to support engineers during problem resolution.

You can use the Technical Bulletin Board download capability to obtain various software utilities, the latest released revisions of speed and package files, detailed solutions for commonly encountered problems, and marketing updates. The Technical Bulletin Board number is 1-408-559-9327 and it is available 24 hours a day, 7 days a week.

Customer Support FAX

The technical support engineers can be reached directly via facsimile by using the "Technical Support only" fax line. This service is available to supply information to the support engineers to resolve a specific inquiry. Additionally, this service may be used in lieu of, or together with, the Technical Support Hotline. The fax number is 1-408-879-4442.

Internet Electronic Mail Support

Another alternative for technical support is via the Internet E-Mail address, hotline@xilinx.com. As with the other previously described methods, electronic mail allows full access to Xilinx Technical Support engineers.

Software Series Overview

The Xilinx Xact*step* Software Series provides powerful, easy to use design tools for FPGA and CPLD devices. Three different series with several choices of configurations lets designers choose the exact system for their needs.

- Foundation Series — Complete shrink-wrapped design solutions
- Alliance Series — Powerful systems that integrate into existing EDA environments
- SLI Series — Value added options that enable system level integration.

The Foundation Series provides entry-level designers with a complete solution in a shrink-wrapped, easy-to-use environment. This fully integrated set of tools, which is perfect for users that are new to PLD design, includes design entry simulation, VHDL synthesis, and design implementation tools.

The Xilinx Alliance Series is for designers who want to integrate into their existing EDA tool environment. It supports the complete spectrum of design techniques with interfaces to over 45 EDA vendors and 80 different design tools.

Optional Viewlogic front-end products are part of the Alliance Series. This is ideal for users who want a complete system that is extensible to board and system level design.

The Foundation and Alliance Series support the industry's broadest array of PLD solutions including the XC2000, XC3000A, XC3100A, XC4000/E, XC5000, XC7300 and XC9500 families. This gives designers technology independence by letting them choose target devices late in the design cycle.

Both series include the powerful XACT*step* implementation system containing the popular Design Manager, Flow Engine, PROM File Formatter, Floorplanner and Hardware Debugger.

All products in the Xilinx XACT*step* Series use standards-based design techniques that maximize design portability and reuse. EDA design tools that support EDIF, ABEL, Verilog, VHDL and LPM formats interface easily into the Xilinx design environment.

PLD designs can use integrated ABEL design and synthesis or interfaces to any of the leading PLD design tools environments. Schematic designs can use the integrated capture tool in the Foundation Series or choose interfaces to any leading EDA environment. HDL designs enjoy standards-based design using integrated VHDL synthesis in the Foundation Series or interfaces to any leading VHDL or Verilog synthesis tool.

This flexibility protects the user's investment in design tools and training and makes it easy to re-use designs even when EDA systems change.

Foundation Series

The Foundation Series provides everything required to design a programmable logic device in an easy-to-use, fully-integrated environment. This fully integrated solution makes PLD design easy by providing push button design flows, on-line training and the XACT*step* windows-based graphical user interface.

This series features broad support for standards based HDL design. All configurations interface with the popular ABEL language and fitters optimized for each target architecture. VHDL configurations include integrated VHDL synthesis with tutorials and wizards to turn new users into experts quickly and easily.

Easy to Learn and Use

The Foundation Series is a fully integrated tool set allowing users to access design entry, implementation and verification tools from a single graphical user interface. Every step in the design process is accomplished using graphical tool bars, icons and pop-up menus supported by interactive tutorials and comprehensive on-line help.

VHDL Synthesis

VHDL configurations of the Foundation Series contain integrated VHDL synthesis and wizards with the following features.

- On-line tutorial teaches the art of VHDL design.
- Intelligent HDL editor with color coding, syntax checking and single click error navigation makes it easy to read and debug VHDL designs.
- HDL Language Assistant provides libraries of common functions with optimized VHDL code.
- FPGA specific synthesis tools produce high-density, high-performance results.

ABEL-HDL Synthesis

ABEL™ configurations of the Foundation Series contain integrated synthesis and wizards with the following features.

- Intelligent HDL editor with color coding, syntax checking and single click error navigation makes it easy to read and debug ABEL designs.
- HDL Language Assistant provides libraries of common functions with optimized ABEL code.
- FPGA/CPLD specific synthesis tools produce high-density, high-performance results.

Alliance Series

The Alliance Series is for users who want powerful design tools that integrate into their existing EDA environment. With this series, designers can choose from a wide range of design techniques including schematic capture, module-based design and HDL from over 45 EDA vendors. With standards based design interfaces including EDIF, ABEL, Verilog and VHDL, this series provides maximum flexibility, portability and design reuse.

Advanced integration with Cadence, Mentor, OrCAD, Synopsys and Viewlogic provide tightly-coupled environments that make it easy to move through the design process.

Other EDA vendors are supported through the Xilinx Alliance Program, insuring high quality tools and accurate results. Information on these vendors can be found on the Xilinx Alliance CD or through WebLINX on the world wide web at www.xilinx.com.

The Alliance Series includes the complete XACT*step* implementation tool set supporting the complete spectrum of design methodologies from fully-automatic to hand-crafted.

Viewlogic Standalone products are part of the Alliance Series and are for those users who want the integration of a complete solution with the power to access board and system level design tools. These products include Viewlogic Workview Office schematic capture, simulation and synthesis tools.

Configurations

The Xilinx Software Series are available in 3 configurations giving designers a cost effective way to match their tools to the gate densities they require.

CPLD configurations provide support for Xilinx's XC9500 and XC7300 CPLD families.

Base configurations provides push-button design flows and support designs up to 5,000 gates.

Standard configurations combine push-button flows with powerful auto-interactive tools. These tools give designers more influence and control over implementation while maintaining the benefits of design automation. Standard configurations support designs up to 20,000 gates.

Optional LogiCores give designers access to large fully verified functions that simplify design entry and provide dramatic savings in engineering resources. The initial LogiCore product set includes a complete PCI interface module.

Migration Paths

All tools in the Xilinx XACT*step* Series use standards-based design to protect the user's investment as design requirements change.

For example, designers can use Foundation products to learn ABEL or VHDL and produce code optimized for device resources. If future requirements force the use of different design tools, users can upgrade to the Xilinx Alliance Series and reuse their code while gaining access to powerful system-level tools.

The Foundation and Alliance Series use the same core implementation tools eliminating the need to re-learn the design process after an upgrade.

Unified libraries and standard design file formats allow schematic designers to enjoy the same migration capabilities.

Individual Products

Libraries and Interface – Contains schematic symbols or HDL libraries, simulation models with timing information, and translators to the XNF file format.

Core Implementation – Provides the software necessary to process an XNF file into a file which can be used to program a Xilinx FPGA or CPLD device. Includes tools for logic reduction, design rule checking, mapping, automatic placement and routing, bitstream generation and PROM file generation.

X-BLOX Module Generator & Optimizer – Allows design entry as block diagrams using a familiar schematic editor. Using built-in expert knowledge, X-BLOX software automatically optimizes your design to take full advantage of the unique features of the XC3000A, XC3100A, XC4000, and XC5000 FPGA families.

Xilinx ABEL – Supports CPLD and FPGA text-based design entry and netlist translation using ABEL high level description language. ABEL supports different design styles including Boolean equations, truth tables and encoded or symbolic state machines.

XChecker™ Cable – Supports downloading of bitstream and PROM files, and readback of configuration data and internal node values. This cable uses the serial port of IBM PCs & compatibles and supported workstations.

FPGA Demoboard – Provides demonstration or prototype capability for XC2000, XC3000, XC3000A, XC3100, XC3100A devices in 68-pin PLCC packages, and XC4000 family devices in 84-pin PLCC. This board is designed to offer flexibility for learning and prototyping.

Order Codes

Order codes for Development Systems products consist of a multiple-field part number. The first field indicates the product category. Additional fields indicate the third-party CAE vendor for interface tools, the package name or individual product number and the platform.

For example, the following order code indicates the category as Development System, the interface CAE vendor as Viewlogic, the package as Standard, the platform as IBM PC or compatible, and the media as CD-ROM.

DS-VL-STD-PC1-C

The following table shows valid product category, CAE vendor, package type, platform and media type codes.

Product Category	Code
Development System	DS
Support and Updates	SC
Base Update	BU
Re-instate Updates	SR
Product Upgrade	DX
Hardware	HW
Training Course	TC

Interface Vendor	Code
OrCAD	OR
Viewlogic	VL
Viewlogic *Stand-alone*	VLS
Mentor, version 8	MN8
Synopsys	SY
Cadence	CDN
Foundation	FND

Package Type	Code
Base System	BAS
Standard System	STD
Extended System	EXT
Advanced System	ADV

Platform	Code
IBM PC compatible	PC1
Sun-4	SN2
HP700	HP7
IBM RS6000	RS6

Media Type	Code
CD-ROM	C

Development Systems: Bundled Packages Product Descriptions

June 1, 1996 (Version 1.0)

This section describes the following products:

Foundation Series

- Foundation Base System (PC)
- Foundation Base System with VHDL Synthesis (PC)
- Foundation Standard System (PC)
- Foundation Standard System with VHDL Synthesis (PC)

Alliance Series

- OrCAD – Base System (PC)
- OrCAD – Standard System (PC)
- Viewlogic – Base System (PC)
- Viewlogic – Standard System (PC)
- Viewlogic Stand-alone – Base System (PC)
- Viewlogic Stand-alone – Standard System (PC)
- Viewlogic Stand-alone – Extended System (PC)
- Viewlogic – Standard System (Workstation)
- Mentor – Standard System (Workstation)
- Synopsys – Standard System (Workstation)
- Cadence Standard System (Workstation)
- Third-Party Alliance – Standard System (PC and Workstation)

Foundation Series: Foundation Base System (PC)

Base System Includes

- Schematic editor with library support for XC2000, XC3000/A, XC3100/A, XC4000/E, XC5200 FPGAs and XC7300 and XC9500 CPLDs
- Functional and Timing Simulator
- Core implementation software for FPGAs with device support for XC2000, XC3000/A & XC3100/A up to XC3x42/A, XC4000/E up to XC4003/E, and XC5200 up to XC5204
- Core implementation software for CPLDs with device support for XC7300 and XC9500
- XChecker Diagnostic Cable

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx bulletin board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation

Required Hardware Environment

- Fully compatible PC386/486/Pentium
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 70 MB hard disk space
- ISO 9660 type CD ROM drive
- VGA display
- One parallel and two serial ports
- 16 MB of RAM

Package Features - Foundation Base (PC)

Feature	FND Base	FND Std.	FND BaseV	FND Std. V
Libraries and Interface	√	√	√	√
Schematic Editor	√	√	√	√
Simulator (Unlimited)	√	√	√	√
CPLD Devices	√	√	√	√
FPGA Limited[1]	√		√	
FPGA 2K, 3K, 4K, 5K		√		√
Core Implementation	√[2]	√	√[2]	√
Synthesis Tools			√	√
X-BLOX		√		√
XChecker Cable	√	√	√	√
Hotline Support	√	√	√	√

Notes: 1. XC2000, XC3000, up to XC3042/XC3142; XC4000/E up to XC4003/E; XC5200 up to XC5204
2. XDE Design Editor and Floorplanner not included

Foundation Series: Foundation Base System with VHDL Synthesis (PC)

Base System Includes

- Schematic editor with library support for XC2000, XC3000/A, XC3100/A, XC4000/E, XC5200 FPGAs and XC7300 and XC9500 CPLDs
- Functional and Timing Simulator
- VHDL Synthesis capability with HDL
- Wizard that makes HDL design entry easier and faster with Xilinx specific templates
- VHDL multimedia tutorial
- Core implementation software for FPGAs with device support for XC2000, XC3000/A & XC3100/A up to XC3x42/A, XC4000/E up to XC4003/E, and XC5200 up to XC5204
- Core implementation software for CPLDs with device support for XC7300 and XC9500
- XChecker Diagnostic Cable

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx bulletin board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation

Required Hardware Environment

- Fully compatible PC386/486/Pentium
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 70 MB hard disk space
- ISO 9660 type CD ROM drive
- VGA display
- One parallel and two serial ports
- 16 MB of RAM

Package Features - Foundation (PC)

Feature	FND Base	FND Std.	FND BaseV	FND Std. V
Libraries and Interface	√	√	√	√
Schematic Editor	√	√	√	√
Simulator (Unlimited)	√	√	√	√
CPLD Devices	√	√	√	√
FPGA Limited[1]	√		√	
FPGA 2K, 3K, 4K, 5K		√		√
Core Implementation	√[2]	√	√[2]	√
Synthesis Tools			√	√
X-BLOX		√		√
XChecker Cable	√	√	√	√
Hotline Support	√	√	√	√

Notes: 1. XC2000, XC3000, up to XC3042/XC3142; XC4000/E up to XC4003/E; XC5200 up to XC5204
2. XDE Design Editor and Floorplanner not included

Foundation Series: Foundation Standard System (PC)

Standard System Includes

- Schematic editor with library support for XC2000, XC3000/A, XC3100/A, XC4000/E, XC5200 FPGAs and XC7300 and XC9500 CPLDs
- Functional and Timing Simulator (unlimited gates)
- Core implementation software for FPGAs with device support for XC2000, XC3000/A & XC3100/A, XC4000/E and XC5200
- Core implementation software for CPLDs with device support for XC7300 and XC9500
- XChecker Diagnostic Cable

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx bulletin board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation

Required Hardware Environment

- Fully compatible PC386/486/Pentium
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 70 MB hard disk space
- ISO 9660 type CD ROM drive
- VGA display
- One parallel and two serial ports
- 16 MB of RAM

Package Features - Foundation (PC)

Feature	FND Base	FND Std.	FND BaseV	FND Std. V
Libraries and Interface	√	√	√	√
Schematic Editor	√	√	√	√
Simulator (Unlimited)	√	√	√	√
CPLD Devices	√	√	√	√
FPGA Limited	√		√	
FPGA 2K, 3K, 4K, 5K		√		√
Core Implementation	√	√	√	√
Synthesis Tools			√	√
X-BLOX		√		√
XChecker Cable	√	√	√	√
Hotline Support	√	√	√	√

Foundation Series: Foundation Standard System with VHDL (PC)

Standard System Includes

- Schematic editor with library support for XC2000, XC3000/A, XC3100/A, XC4000/E, XC5200 FPGAs and XC7300 and XC9500 CPLDs
- Functional and Timing Simulator (unlimited gates)
- VHDL Syntheses capability with HDL Wizard that makes HDL design entry easier and faster with Xilinx specific templates
- VHDL multimedia tutorial
- Core implementation software for FPGAs with device support for XC2000, XC3000/A & XC3100/A, XC4000/E and XC5200
- Core implementation software for CPLDs with device support for XC7300 and XC9500
- XChecker Diagnostic Cable

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx bulletin board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation

Required Hardware Environment

- Fully compatible PC386/486/Pentium
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 70 MB hard disk space
- ISO 9660 type CD ROM drive
- VGA display
- One parallel and two serial ports
- 16 MB of RAM

Package Features - Foundation (PC)

Feature	FND Base	FND Std.	FND BaseV	FND Std. V
Libraries and Interface	√	√	√	√
Schematic Editor	√	√	√	√
Simulator (Unlimited)	√	√	√	√
CPLD Devices	√	√	√	√
FPGA Limited	√		√	
FPGA 2K, 3K, 4K, 5K		√		√
Core Implementation	√	√	√	√
Synthesis Tools			√	√
X-BLOX		√		√
XChecker Cable		√		√
Hotline Support	√	√	√	√

Alliance Series: OrCAD – Base System (PC)

Base System Includes

- Schematic Interface for OrCAD SDT386+ with library support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E and XC5200 FPGAs and XC7000 and XC9500 Series CPLDs
- Functional and Timing Simulation Interface for OrCAD VST386+
- Core Implementation Software for CPLDs and FPGAs with device support for XC2000, XC3000, XC3000A and XC3100, XC3100A up to XC3x42, XC3x42A, XC4000/E up to XC4003/E, XC5200 up to XC5204, XC7300, and XC9500

Note:

- This package does not include the OrCAD SDT schematic capture or VST simulation tools. They must be purchased separately from OrCAD.
- XDE-Xilinx Design Editor is not included.
- This Base Package does not come with a standard one year update contract. Instead, when Xilinx releases a new version of software, customers will be notified and may purchase the Base Update at the listed price.
- The Base Update is only available to licensees of the DS-OR-BAS-PC1 on a one-for-one basis.

Revision Updates Include

- Latest version software and online documentation
- Only available to customers who have purchased a Base product before.

Required Hardware Environment

- Fully IBM compatible PC386/486/Pentium
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 60 Mbyte hard-disk space
- One 3.5" High-Density floppy disk drive
- VGA display
- One parallel and two serial ports
- 16 Mbytes of RAM for all supported XC3000A and XC4000/E FPGAs
- Mouse

Package Features - OrCAD PC

Feature	Base	Std.
Libraries and Interface	√	√
Schematic Editor		
Simulator (Limited)		
Simulator (Unlimited)		
EPLD Devices	√	√
FPGA Limited[1]	√	
FPGA 2K, 3K, 4K, 5K		√
Core Implementation	√[2]	√
Synthesis Tools		
X-BLOX		√
XChecker Cable	√	√
Hotline Support	√	√

Notes: 1. XC2000, XC3000, up to XC3042/XC3142; XC4000/E up to XC4003/E; XC5200 up to XC5204
2. XDE Design Editor and Floorplanner not included

Alliance Series: OrCAD – Standard System (PC)

Standard System Includes

- Schematic Interface for OrCAD SDT386+ with library support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E FPGAs and XC7000 and XC9500 Series CPLDs
- Functional and Timing Simulation Interface for OrCAD VST386+
- X-BLOX Module Generator and Optimizer
- Core Implementation Software for CPLDs and FPGAs with device support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200, XC7300, and XC9500
- Software Support and Updates for first year

Note:

- This package does not include the OrCAD SDT schematic capture or VST simulation tools. They must be purchased separately from OrCAD.

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Required Hardware Environment

- Fully IBM compatible PC386/486/Pentium
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 80 Mbyte hard-disk space
- One ISO 9660 compatible CD-ROM drive
- VGA display
- One parallel and two serial ports
- 16 Mbytes of RAM up to XC4008
- 24 Mbytes of RAM for XC3195, XC3195A, XC4010
- 32 Mbytes of RAM for XC4013
- Mouse

Package Features - OrCAD PC

Feature	Base	Std.
Libraries and Interface	√	√
Schematic Editor		
Simulator (Limited)		
Simulator (Unlimited)		
EPLD Devices	√	√
FPGA Limited	√	
FPGA 2K, 3K, 4K, 5K		√
Core Implementation	√	√
Synthesis Tools		
X-BLOX		√
XChecker Cable	√	√
Hotline Support	√	√

Alliance Series: Viewlogic – Base System (PC)

Base System Includes

- Viewlogic Schematic Interface library support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200 FPGAs, and XC7000 and XC9500 CPLDs
- Viewlogic Functional and Timing Simulation Interface
- Core Implementation Software for CPLDs and FPGAs with device support for XC2000, XC3000, XC3000A, XC3100, XC3100A up to XC3x42/A, XC4000/E up to XC4003/E, XC5200 up to XC5204, XC7300, and XC9500

Note:

- This package does not include Viewlogic schematic capture or simulation tools. They must be purchased separately from Viewlogic or Xilinx (see Stand-alone packages).
- Interface and libraries support Workview 6.1, Workview PRO and Office Series.
- XDE-Xilinx Design Editor - not included
- This Base Package does not come with a standard one-year update contract. Instead, when Xilinx releases a new version of software, customers will be notified and may purchase the Base Update at the listed price.
- The Base Update is only available to licensees of the DS-VL-BAS-PC1 on a one-for-one basis.

Revision Updates Include

- Latest version software and online documentation
- Only available to customers who have purchased a base product before.

Required Hardware Environment

- Fully IBM compatible PC386/486/Pentium
- MS-Windows version 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 60 Mbytes disk space
- One CD-ROM drive
- VGA display
- 3-Button Serial Mouse
- One parallel and two serial ports
- 16 Mbytes of RAM

Package Features - Viewlogic PC

Feature	VL Base	VL Std.	VLS Base	VLS Std.	VLS Ext.
Libraries and Interface	√	√	√	√	√
Schematic Editor			√	√	√
Simulator (Limited)			√		
Simulator (Unlimited)				√	√
EPLD Devices	√	√	√	√	√
FPGA Limited[1]	√		√		
FPGA 2K, 3K, 4K, 5K		√		√	√
Core Implementation	√[2]	√	√[2]	√	√
Synthesis Tools					√
X-BLOX		√		√	√
XChecker Cable	√	√	√	√	√
Hotline Support	√	√	√	√	√

1. XC2000, XC3000, up to XC3042/XC3142; XC4000/E up to XC4003/E; XC5200 up to XC5204
2. XDE Design Editor and Floorplanner not included

Alliance Series: Viewlogic – Standard System (PC)

Standard System Includes

- Viewlogic Schematic Interface with library support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200 FPGAs and XC7000 and XC9500 CPLDs
- Viewlogic Functional and Timing Simulation Interface
- Core Implementation Software for CPLDs and FPGAs with device support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200, XC7300, and XC9500
- X-BLOX Module Generator and Optimizer
- Software Support and Updates for the first year

Note:

- This package does not include Viewlogic schematic capture or simulation tools. They must be purchased separately from Viewlogic or Xilinx (see Stand-alone packages).
- Interface and libraries support Workview PRO and Office Series.

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Required Hardware Environment

- Fully IBM compatible PC386/486/Pentium
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 90 Mbytes hard-disk space
- One ISO 9660 compatible CD-ROM drive
- VGA display
- 3-Button Serial Mouse
- One parallel and two serial ports
- 16 Mbytes of RAM for devices up to XC4008
- 24 Mbytes of RAM for XC3195, XC4010
- 32 Mbytes of RAM for XC4013

Package Features - Viewlogic PC

Feature	VL Base	VL Std.	VLS Base	VLS Std.	VLS Ext.
Libraries and Interface	√	√	√	√	√
Schematic Editor			√	√	√
Simulator (Limited)			√		
Simulator (Unlimited)				√	√
EPLD Devices	√	√	√	√	√
FPGA Limited	√		√		
FPGA 2K, 3K, 4K, 5K		√		√	√
Core Implementation	√	√	√	√	√
Synthesis Tools					√
X-BLOX		√		√	√
XChecker Cable	√	√	√	√	√
Hotline Support	√	√	√	√	√

Alliance Series: Viewlogic *Stand-alone* – Base System (PC)

Stand-alone Standard System Includes

- Workview Office Schematic Editor with library support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200 FPGAs and XC7000 and XC9500 CPLDs
- Workview Office Functional and Timing Simulation for designs (limited gates)
- Core Implementation Software for CPLDs and FPGAs with device support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200, XC7300, and XC9500

Note:

- XDE-Xilinx Design Editor - not included
- This Base Package does not come with a standard one-year update contract. Instead, when Xilinx releases a new version of software, customers will be notified and may purchase the Base Update at the listed price.
- The Base Update is only available to licensees on a one-for-one basis.

Revision Updates Include

- Latest version software and online documentation
- Only available to customers who have purchased a base product before.

Required Hardware Environment

- Fully IBM compatible PC386/486/Pentium
- MS-Windows version 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 60 Mbytes disk space
- One CD-ROM drive
- VGA display
- 3-Button Serial Mouse
- One parallel and two serial ports
- 16 Mbytes of RAM

Package Features - Viewlogic PC

Feature	VL Base	VL Std.	VLS Base	VLS Std.	VLS Ext.
Libraries and Interface	√	√	√	√	√
Schematic Editor			√	√	√
Simulator (Limited)			√		
Simulator (Unlimited)				√	√
EPLD Devices	√	√	√	√	√
FPGA Limited[1]	√		√		
FPGA 2K, 3K, 4K, 5K		√		√	√
Core Implementation	√[2]	√	√[2]	√	√
Synthesis Tools					√
X-BLOX		√		√	√
XChecker Cable	√	√	√	√	√
Hotline Support	√	√	√	√	√

Notes: VL = Viewlogic, VLS = Viewlogic *Stand-alone*
1. XC2000, XC3000, up to XC3042/XC3142; XC4000/E up to XC4003/E; XC5200 up to XC5204
2. XDE Design Editor and Floorplanner not included

Alliance Series: Viewlogic *Stand-alone* – Standard System (PC)

***Stand-alone* Standard System Includes**

- Workview Office Schematic editor with library support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200 FPGAs and XC7000 and XC9500 CPLDs
- Workview Office Functional and Timing Simulation for designs (unlimited gates)
- Core Implementation Software for CPLDs and FPGAs with device support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200, XC7300, and XC9500
- X-BLOX Module Generator and Optimizer
- Software Support and Updates for the first year

Support and Updates Include

- Hotline Telephone support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Required Hardware Environment

- Fully IBM compatible PC386/486/Pentium
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 90 Mbytes hard-disk space
- One ISO 9660 compatible CD-ROM drive
- VGA display
- 3-Button SP Mouse
- One parallel and two serial ports
- 16 Mbytes of RAM for devices up to XC4008
- 24 Mbytes of RAM for XC3195, XC4010
- 32 Mbytes of RAM for XC4013

Package Features - Viewlogic PC

Feature	VL Base	VL Std.	VLS Base	VLS Std.	VLS Ext.
Libraries and Interface	√	√	√	√	√
Schematic Editor			√	√	√
Simulator (Limited)			√		
Simulator (Unlimited)				√	√
EPLD Devices	√	√	√	√	√
FPGA Limited	√		√		
FPGA 2K, 3K, 4K, 5K		√		√	√
Core Implementation	√	√	√	√	√
Synthesis Tools					√
X-BLOX		√		√	√
XChecker Cable	√	√	√	√	√
Hotline Support	√	√	√	√	√

Alliance Series: Viewlogic *Stand-alone* – Extended System (PC)

Extended *Stand-alone* System Includes

- Workview Office Schematic editor with library support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200 FPGAs and XC7000 and XC9500 CPLDs
- Workview Office Functional, Timing, and VHDL Simulation (unlimited gates)
- ViewSynthesis – VHDL synthesis with X-BLOX integration and library synthesis support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E and XC5200 FPGAs
- X-BLOX Module Generator and Optimizer
- Core Implementation Software for CPLDs and FPGAs with device support for XC2000, XC3000/ XC3100, XC4000/E, XC5200, XC7300, and XC9500
- Software Support and Updates if on maintenance

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Required Hardware Environment

- Fully IBM compatible PC386/486/Pentium
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 90 Mbytes hard-disk space
- One ISO 9660 compatible CD-ROM drive
- VGA display
- 3-Button Serial Mouse
- One parallel and two serial ports
- 16 Mbytes of RAM for devices up to XC4008
- 24 Mbytes of RAM for XC3195, XC4010
- 32 Mbytes of RAM for XC4013

Package Features - Viewlogic PC

Feature	VL Base	VL Std.	VLS Base	VLS Std.	VLS Ext.
Libraries and Interface	√	√	√	√	√
Schematic Editor			√	√	√
Simulator (Limited)			√		
Simulator (Unlimited)				√	√
EPLD Devices	√	√	√	√	√
FPGA Limited	√		√		
FPGA 2K, 3K, 4K, 5K		√		√	√
Core Implementation	√	√	√	√	√
Synthesis Tools					√
X-BLOX		√		√	√
XChecker Cable	√	√	√	√	√
Hotline Support	√	√	√	√	√

Alliance Series: Viewlogic – Standard System (Workstation)

Standard System Includes

- Schematic Interface for Draw with library support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200 FPGAs and XC7000 and XC9500 CPLDs
- Functional and Timing Simulation Interface for ViewSim
- Core Implementation Software for CPLDs and FPGAs with device support for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200, XC7300, and XC9500
- X-BLOX Module Generator and Optimizer
- Software Support and Updates if on maintenance

Note:

- This package does not include schematic capture or simulation tools. They must be purchased separately.
- Interface supports Workview Office and PRO Series

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Required Hardware Environment

- 50 to 200 MB hard disk space allocated Xilinx designs.
- 32 MB of RAM (minimum)
- Color Monitor
- Swap Space: 140 MB (minimum)
- TCP/IP Software
- CD ROM Drive

Sun-4 Sparcstation Series

- Sun OS 4.1.X
- X-Windows (R3 or R4)
- Open Windows or Motif

HP700 Series

- HPUX 9.0/9.1
- X-Windows (R5)
- HP_VUE 3.0

Recommended Hardware Environment

- Additional RAM to increase performance

Package Features - Viewlogic W/S

Feature	Std.
Libraries and Interface	√
Schematic Editor	
Simulator (Limited)	
Simulator (Unlimited)	
EPLD Devices	√
FPGA Limited	
FPGA 2K, 3K, 4K, 5K	√
Core Implementation	√
Synthesis Tools	
X-BLOX	√
XChecker Cable	√
Hotline Support	√

Alliance Series: Mentor V8 – Standard System (Workstation)

Standard System Includes

- Mentor V8 Interface (Mentor Design Architect/QuickSim II Libraries and Interface)
- Core Implementation Software for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200 FPGAs and XC7300 and XC9500 CPLDs
- X-BLOX Module Generator and Optimizer
- Software Support and Updates if on maintenance

Note:

- This package does not include Design Architect schematic capture, or QuickSim II simulation tools. Contact your local Mentor Graphics sales office to purchase these tools.
- AutoLogic synthesis program, libraries and interface are available from Mentor Graphics.

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Required Hardware Environment

- 50 to 200 MB hard disk space allocated Xilinx designs.
- 32 MB of RAM (minimum)
- Color Monitor
- Swap Space: 140 MB (minimum)
- TCP/IP Software
- CD ROM Drive

Sun-4 Sparcstation Series

- Sun OS 4.1.X
- X-Windows (R3 or R4)
- Open Windows or Motif

HP700 Series

- HPUX 9.0/9.1
- X-Windows (R5)
- HP_VUE 3.0

Recommended Hardware Environment

- Additional RAM to increase performance

Package Features - Mentor W/S

Feature	Std.
Libraries and Interface	√
Schematic Editor	
Simulator (Limited)	
Simulator (Unlimited)	
EPLD Devices	√
FPGA Limited	
FPGA 2K, 3K, 4K, 5K	√
Core Implementation	√
Synthesis Tools	
X-BLOX	√
XChecker Cable	√
Hotline Support	√

Alliance Series: Synopsys – Standard System (Workstation)

Standard System Includes

- XC3000, XC3000A, XC3100, XC3100A, XC4000/E and XC5200 synthesis library
- Core Implementation Software for XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200 FPGAs, and XC7300 and XC9500 CPLDs
- X-BLOX Module Generator and Optimizer
- Works with Synopsys Design Compiler and FPGA Compiler
- Translator from Synopsys to Xilinx XNF
- Software Support and Updates if on maintenance

Note:

- This package does not include Synopsys Design Compiler or FPGA Compiler. These must be purchased separately from Synopsys.

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Required Hardware Environment

- 50 to 200 MB hard disk space allocated Xilinx designs.
- 32 MB of RAM (minimum)
- Color Monitor
- Swap Space: 140 MB (minimum)
- TCP/IP Software
- CD ROM Drive

Sun-4 Sparcstation Series

- Sun OS 4.1.X
- X-Windows (R3 or R4)
- Open Windows or Motif

HP700 Series

- HPUX 9.0/9.1
- X-Windows (R5)
- HP_VUE 3.0

Recommended Hardware Environment

- Additional RAM to increase performance

Package Features - Synopsys W/S

Feature	Std.
Libraries and Interface	√
Schematic Editor	
Simulator (Limited)	
Simulator (Unlimited)	
EPLD Devices	√
FPGA Limited	
FPGA 2K, 3K, 4K, 5K	√
Core Implementation	√
Synthesis Tools	
X-BLOX	√
XChecker Cable	√
Hotline Support	√

Alliance Series: Cadence – Standard System (Workstation)

Standard System Includes

- Cadence Interface (Composer and Concept Schematic Libraries and Verilog and RapidSim simulation models and interfaces)
- Core Implementation Software for XC2000, XC3000/A, XC3100/A, XC4000/E, XC5200 FPGAs, and XC7300 and XC9500 CPLDs
- LogiBlox Module Generator and Optimizer
- Software Support and Updates if on maintenance

Note:

- This package does not include Composer/Concept schematic capture, or Verilog/RapidSim simulation tools. Contact your local Cadence sales office to purchase these tools
- FPGA designer (Synergy based top-down FPGA design tool) is available from Cadence.

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Required Hardware Environment

- 50 to 200 MB hard disk space allocated Xilinx designs.
- 32 MB of RAM (minimum)
- Color Monitor
- Swap Space: 140 MB (minimum)
- TCP/IP Software
- CD ROM Drive

Sun-4 Sparcstation Series

- Sun OS 4.1.X
- X-Windows (R3 or R4)
- Open Windows or Motif

HP700 Series

- HPUX 9.0/9.1
- X-Windows (R5)
- HP_VUE 3.0

Recommended Hardware Environment

- Additional RAM to increase performance

Package Features - Synopsys W/S

Feature	Std.
Libraries and Interface	√
Schematic Editor	
Simulator (Limited)	
Simulator (Unlimited)	
EPLD Devices	√
FPGA Limited	
FPGA 2K, 3K, 4K, 5K	√
Core Implementation	√
Synthesis Tools	
X-BLOX	√
XChecker Cable	√
Hotline Support	√

Alliance Series: Third Party Alliance – Standard System

Standard System Includes

- X-BLOX Module Generator & Optimizer
- Core Implementation Software for CPLDs and FPGAs with device support for XC2000, XC3000/A, XC3100/A, XC4000/E, XC7300, and XC9500
- Software Support and Updates for the first year

Note:

- Purchase schematic and simulation tools and interfaces and libraries from a Xilinx 3rd-Party Alliance Partner

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Required Hardware Environment (PC)

- Fully compatible PC386/486/Pentium
- MS-DOS version 5.0 (minimum)
- MS-Windows 3.1 (minimum)
- Minimum 80 MB hard disk space
- One ISO 9660-type CD-ROM drive
- VGA display (higher resolutions supported)
- One parallel and two serial ports
- 16 MB of RAM for devices up to XC4008
- 24 MB of RAM for XC3195A, XC4010
- 32 MB of RAM for XC4013
- Mouse

Required Hardware Environment (Workstation)

- 50 to 200 MB hard disk space allocated Xilinx designs.
- 32 MB of RAM (minimum)
- Color Monitor
- Swap Space: 140 MB (minimum)
- TCP/IP Software
- CD-ROM Drive

Sun-4 Sparcstation Series

- Sun OS 4.1.X
- X-Windows (R3 or R4)
- Open Windows or Motif

HP700 Series

- HPUX 9.0/9.1
- X-Windows (R5)
- HP_VUE 3.0

IBM RS6000

- AIX 3.2
- X-Windows Support

Package Features - Third Party Alliance

Feature	Std.
Libraries and Interface	√
Schematic Editor	
Simulator (Limited)	
Simulator (Unlimited)	
EPLD Devices	√
FPGA Limited[1]	
FPGA 2K, 3K, 4K, 5K	√
Core Implementation	√
Synthesis Tools	
X-BLOX	√
XChecker Cable	√
Hotline Support	√

This section describes the following products:

- FPGA Core Implementation – DS-502
- CPLD Core Implementation – DS-560
- Schematic and Simulator Interfaces
- X-BLOX – DS-380
- Xilinx ABEL Design Entry – DS-371
- Xilinx ABEL Design Entry – DS-571
- Xilinx-Synopsys Interface (XSI) – DS401
- XChecker Cables
- Demonstration Boards

FPGA Core Implementation – DS-502

Core Implementation Includes

- Software to process an XNF file for an XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200 device into a BIT or PROM file that can be downloaded
- Automatic or interactive implementation
- XACT Performance™ system-level timing-driven mapping, placement, and routing
- Fast incremental design capability
- Advanced logic reduction algorithms
- Comprehensive design rule checker
- Powerful design editor
- Static timing analyzer
- Bitstream and PROM file generators
- Original hierarchical netlist-based back-annotation
- Software Support and Updates if on maintenance

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Hardware Requirements

PC

- Fully compatible PC386/486
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 50 Mbytes hard-disk space for Xilinx software
- One 3.5" High-Density floppy disk drive or ISO 9660 type CD-ROM drive
- VGA display
- One parallel and two serial ports
- 16 Mbytes of RAM for devices up to XC4008
- 32 Mbytes of RAM for XC3195, XC4010, and XC4013
- Mouse

Workstations

- 65 Mbytes hard-disk drive space for Xilinx software
- Other hardware requirements are same as for the Standard package

CPLD Core Implementation – DS-560

CPLD Core Implementation Includes

- Fitter software to process XC7000 and XC9500 family designs
- Automatic optimization and mapping
- Automatic use of UIM resources
- Automatic arithmetic functions
- Complete optimization and collapsing
- High speed compilation

Support and Updates Include:

- Documentation Updates
- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX

XACT-CPLD provides a complete, user-friendly, multi-platform design environment for implementing behavioral or schematic designs. XACT-CPLD allows users to easily create, verify, and implement logic designs targeting the entire range of Xilinx XC7000 and XC9500 series devices.

Automatic Logic Mapping and Optimization

The automatic partitioning and mapping capabilities of XACT-CPLD allow the designer to concentrate on design functionality without concern for physical implementation; all device resources are automatically mapped and interconnected with no user intervention required. In addition, automatic logic optimization insures the highest performance and the most efficient usage of device resources. Because of these automatic features, the user does not need a detailed knowledge of the device architecture. However, XACT-CPLD also allows the designer to fully control the physical mapping of logic and I/O resources when necessary.

Required Hardware Environment

- Fully compatible PC 486/Pentium
- MS-Windows 3.1
- MS-DOS version 5.0 (minimum)
- Minimum 26 MB hard disk space
- ISO 9660 type CD ROM drive
- VGA display
- One parallel port for EZTag download cable
- One serial port for Windows compatible mouse
- 16 MB of RAM

Feature Summary

- Advanced XACT*step* v6.0 XC7000 implementation software with fully automatic device selection, multiple pass optimization, partitioning and mapping, and timing driven fitting.
- XC9500 implementation software with advanced pinlocking capability.
- EZTag download software supporting the programming of multiple Xilinx CPLDs anywhere in a JTAG chain.
- Includes XC9500 Synopsys, Viewlogic, and OrCAD interfaces.
- On-line tutorials and documentation
- Static timing report
- Schematic Design Entry — XACT-CPLD, coupled with the appropriate external interface, provides a schematic library that includes familiar TTL and PAL components for use with industry-standard schematic editors such as those available from OrCAD, ViewLogic, Mentor Graphics, and Cadence Design Systems.
- Simulation Support — XACT-CPLD supports various third-party simulators such as ViewLogic PROsim, OrCAD VST, Mentor QuickSim, Cadence Verilog, and Cadence RapidSim. Both functional and timing simulation are supported.
- Board-Level Simulation Support — XACT-CPLD device models are available from Logic Modeling Corporation for board-level simulation on a variety of platforms.
- High-Speed Compilation — Design iterations are easily performed and the results are quickly reported.
- Predictable Design Performance — The PAL-like architecture of the Xilinx CPLDs provides fixed predictable delays independent of physical placement, routing, or device utilization.
- Automatic Mapping and Logic Optimization — Device resources are automatically mapped for optimal efficiency and high performance. Users can focus on design functionality without concern for the physical implementation in the device.
- Complete Design Control — Users have the option to override the automatic features of XACT-CPLD and selectively control any or all device resources.
- Multiple Platform Support — XACT-CPLD runs on Sun, HP, and PC (DOS) platforms

Schematic and Simulator Interfaces

Interfaces and libraries for several popular schematic editors and timing simulators are available as individual products, for users that already own an editor and simulator. For designers looking for a design entry tool, Xilinx offers Xilinx-specific versions of Viewlogic's schematic editor, simulator, and ViewSynthesis VHDL synthesizer and VHDL simulator.

The following products are available for the platforms noted in parentheses:

DS-390 Viewlogic schematic editor with Xilinx libraries and interface (PC)

DS-290 Viewlogic simulator with Xilinx libraries and interface (PC)

DS-391 Libraries and interfaces that support Viewlogic's Workview Office Series, PRO Series, and Powerview design entry and simulation tools (PC, Sun, HP700)

DS-344 Libraries and interfaces for Mentor Graphics Design Architect schematic editor and QuickSim II simulator (HP700, Sun)

DS-35 Libraries and interfaces for OrCAD 386+ schematic editor and VST 386+ simulator (PC)

Features

- Complete set of primitive and macro libraries for all FPGA and CPLD products
- Full simulation models provides for accurate post-layout timing analysis
- Unified libraries allow easy migration between all Xilinx architectures, including CPLDs
- Converts schematic drawings to Xilinx Netlist Format (XNF) output
- Converts XNF files to format compatible with logic and timing simulators
- Supports unlimited levels of hierarchy
- Includes one year of support and updates
- All above products can be purchased with core implementation tools as a package, offering easier upgrading and reduced cost.

X-BLOX – DS-380

X-BLOX Includes

- Parameter-based schematic and function-generation tool. Allows block-diagram design entry using generic function modules.
- Works with many Schematic Entry Interfaces (Viewlogic, Mentor, OrCAD, Cadence and other Alliance Partners)
- Expert system that automatically utilizes the advanced features of the XC5200 family, XC4000/E family and XC3000A and XC3100A families
- Schematic library with more than 30 frequently-used generic modules (adders, counters, decoders, registers, MUXes, etc.)
- Software Support and Updates for first year

Note:

- XC5200, XC4000/E and XC3000A, XC3100A families are supported. XC2000, XC3000, and XC3100 are not supported.
- Additional Requirements:
  Five Mbytes hard-disk space for program and design files

Xilinx ABEL Design Entry – DS-371

The Xilinx ABEL system gives designers the ability to enter Xilinx designs using the industry standard ABEL Hardware Description Language (ABEL-HDL). Designers can describe circuits with Boolean equations, state machines and truth tables. State machine and logic optimization software automatically generates efficient logic for Xilinx devices.

Many designs contain portions of logic that are best described in a text-based format; some designs can be completely described in this way. In the Xilinx ABEL system, Xilinx designs can be created with Boolean equations, state machines, and truth tables. The ABEL HDL makes designing quick and simple. Intelligent state machine and logic optimization software automatically creates efficient, fast state machines. The ABEL simulator allows functional simulation of ABEL-HDL designs.

CPLD designs may be entered entirely with ABEL-HDL. FPGA designs should be entered via a combination of XABEL and a schematic editor to take optimal advantage of the Xilinx architectures. The recommended design flow is to enter designs schematically with functional blocks that refer to logic described in ABEL-HDL. From inside the Xilinx ABEL environment, designers create and compile the logic in these functional blocks. The Xilinx XMake program then compiles the complete design to a bitstream that can be downloaded to a Xilinx device. XMake automatically calls the software that merges the various design files (schematics and ABEL-HDL), partitions, places and routes the design and creates the final bitstream. The design can then be verified with a simulator and a timing analyzer, as well as verified in-circuit.

One-Hot Encoding

For the flop-flop rich, fan-in limited Xilinx FPGA architecture, One-Hot Encoding (OHE) is the preferred technique for implementing high-performance state machines. OHE is also know as state-per-bit encoding, since it uses one flip-flop per state. OHE takes advantage of the abundance of flip-flops in Xilinx FPGAs to reduce the levels of logic required to implement a state machine. This implementation significantly increases performance over fully encoded state machines, the traditional technique used in PLDs. Xilinx ABEL automatically uses OHE on symbolic state machines created in ABEL-HDL for FPGAs.

Features

- State machine and Boolean equation entry via DATA I/O's ABEL language
- ABEL Functional Simulator
- Xilinx-specific ABEL environment, compiler, and optimizer for FPGAs
- Automatic symbolic One-Hot encoding or fully encoded state-machine implementation
- Ability to integrate ABEL designs with other schematic elements
- Software Support and Updates for the first year

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Additional Requirements

- 10 Mbytes hard-disk space for program and design files

Xilinx ABEL Design Entry – DS-571

XABEL-CPLD is the new Xilinx development system designed for PAL and CPLD users. With this completely self contained system, customers can quickly and easily integrate their logic into Xilinx CPLDs using the industry-standard ABEL hardware description language.

XABEL-CPLD Includes

- Familiar Data I/O ABEL, Windows based environment for design entry, simulation and fitting
- Hierarchical design entry and JEDEC file conversion
- Functional simulation with graphical waveform viewer
- Static timing report
- Advanced XACT*step* v6.0 XC7000 and XC9500 fitters with fully automatic device selection, multiple pass optimization, partitioning and mapping, and timing driven fitting
- EZTag download software and cable
- Online tutorial and online help reduces learning curve

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Online tutorial and help

Required Hardware Environment

- Fully compatible PC 486/Pentium
- MS-Windows 3.1
- MS-DOS version 5.0 (minimum)
- Minimum 45 MB hard disk space
- ISO 9660 type CD ROM drive
- VGA display
- One parallel port for EZTag download cable
- One serial port for Windows compatible mouse
- 16 MB of RAM

Feature Summary

- Familiar Data I/O ABEL, Windows based environment for design entry, simulation and fitting provides a simple, single push button design flow
- Industry-standard ABEL-HDL supports state machines, high level logic descriptions, truth tables and equation entry
- Hierarchical design entry and JEDEC file conversion enables reuse of existing PAL codes, simplifying PAL integration into Xilinx CPLDs
- Functional simulation with graphical waveform viewer and static timing reports facilitate rapid design verification
- Advanced XACT*step* v6.0 fitter's architecture specific knowledge let's the user focus on design functionality
- Online tutorial leads users through the entire design process in minutes
- Extensive online help system places all documentation just a mouse-click away

Xilinx-Synopsys Interface (XSI) – DS-401

This interface and library product supports VHDL and Verilog/HDL synthesis using either the Synopsys Design Compiler or FPGA Compiler products

Features

- Synthesis libraries for:
  XC3000/XC3100, XC4000/E and XC5000 family FPGAs
  XC7000 and XC9500 family CPLDs
- X-BLOX synthetic library
- Translator from Synopsys to Xilinx XNF
- Ability to integrate models with other design
- Available for Sun-4, and HP700, platforms

DS-401 (XSI) lets the Synopsys FPGA Compiler and Design Compiler target the XC3000, XC3100, XC4000/E, and XC5000 FPGA families and XC7500 and XC9500 CPLD families. XSI consists of synthesis libraries, a translator from Synopsys to XNF, and a library of X-BLOX functions implemented using Synopsys DesignWare.

Language Support

Either VHDL or Verilog/HDL entry is supported through the use of the appropriate Synopsys language compiler.

Compiler Support

FPGA Compiler is highly recommended for XC4000/E and XC5200 designs due to its specific XC4000/E algorithms. Design Compiler is sufficient for XC3000 and XC3100 designs.

Simulation Support

Behavioral simulation before compilation using Synopsys VHDL System Simulator (VSS) is supported. In the future, gate-level simulation of designs after layout will be supported as well.

Support and Updates

- Software updates for one year
- Documentation updates
- Hotline Telephone Support for the first six months
- Access to Xilinx bulletin board
- Apps FAX

Notes

- This product does not support the Synopsys Test Compiler
- A Synopsys Standard package is available which combines XSI (DS-401) and FPGA core implementation tools (DS-502) in one product. Packages offer reduced prices over modules purchased separately.
- The X-BLOX library allows Synopsys software to automatically insert certain X-BLOX functions (adders, subtracters, and comparators) where possible for maximum performance. In-warranty XSI customer receive X-BLOX as an automatic upgrade.

XChecker Cables

XChecker Cable Package Includes

- XChecker cable
- Flying wire jumper
- Flat header jumper
- XChecker diagnostics fixture

XChecker Cable Features

- Provides bitstream and PROM-file download capability to FPGAs
- Provides readback capability
- Works with serial ports on IBM 386/486/Pentium and compatibles
- Compatible with XACT XChecker diagnostics software and the XACT Probe utility
- Flying-wire and flat-header jumpers provide easy access during prototyping

Demonstration Board – FPGA

FPGA Demo Board Includes

- Three 7-segment displays (one for XC3000, XC3000A and two for XC4000/E)
- Two, octal DIP switches for inputs to LCA devices (one for XC3000 and one for XC4000/E)
- Test pins for access to all LCA I/O
- XC4003A in 84-pin PLCC package
- XC3020A in 68-pin PLCC package
- Two 8-segment bar displays (one for XC3000A and one for XC4000/E)
- Program, Reset, and Spare momentary contact switches

FPGA Demo Board Features

- Operates from a 5-V power supply
- Compatible with XChecker and parallel download cables
- Supports Master-Serial configuration mode for interface to Xilinx serial PROMs
- Two sockets, one can be used for any XC2000, XC3000 or XC3100 device in a 68-pin PLCC package, the other can be used for any XC4000/E device in an 84 pin PLCC package
- Provides sockets for up to three daisy-chained serial PROMs
- Includes 3 inch by 3 inch prototyping area
- Daisy-chain configuration capability (XC4000/E must be first in the chain)

CPLD Products

XC9500 In-System Programmable CPLD Family

XC9536 In-System Programmable CPLD

XC9572 In-System Programmable CPLD

XC95108 In-System Programmable CPLD

XC95144 In-System Programmable CPLD

XC95180 In-System Programmable CPLD

XC95216 In-System Programmable CPLD

XC95288 In-System Programmable CPLD

XC95432 In-System Programmable CPLD

XC95576 In-System Programmable CPLD

XC9500 In-System Programmable CPLD Family

August 1, 1996 (Version 1.1)

Preliminary Product Information

Features

- High-performance
  - 5 ns pin-to-pin logic delays on all pins
  - f_{CNT} to 125 MHz
- Large density range
  - 36 to 576 macrocells with 800 to12,800 usable gates
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-5, -7, -10 speed grades)
- Advanced 0.6µm CMOS 5V FastFLASH technology

Description

The XC9500 CPLD family provides advanced in-system programming and test capabilities for high performance, general purpose logic integration. All devices are in-system programmable for a minimum of 10,000 program/erase cycles. Extensive IEEE 1149.1 (JTAG) boundary-scan support is also included on all family members.

As shown in Table 1, the nine devices of the XC9500 family range in logic density from 800 to over 12,800 usable gates with 36 to 576 registers, respectively. Multiple package options and associated I/O capacity are shown in Table 2. The XC9500 family is fully pin-compatible allowing easy design migration across multiple density options in a given package footprint.

The XC9500 architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. An expanded JTAG instruction set allows version control of programming patterns and in-system debugging. In-system programming throughout the full device operating range and a minimum of 10,000 program/erase cycles provide worry-free reconfigurations and system field upgrades.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. I/Os may be configured for 3.3 V or 5 V operation. All outputs provide 24 mA drive.

Architecture Description

Each XC9500 device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the FastCONNECT switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with 36 inputs and 18 outputs. The FastCONNECT switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, 12 to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. See Figure 1.

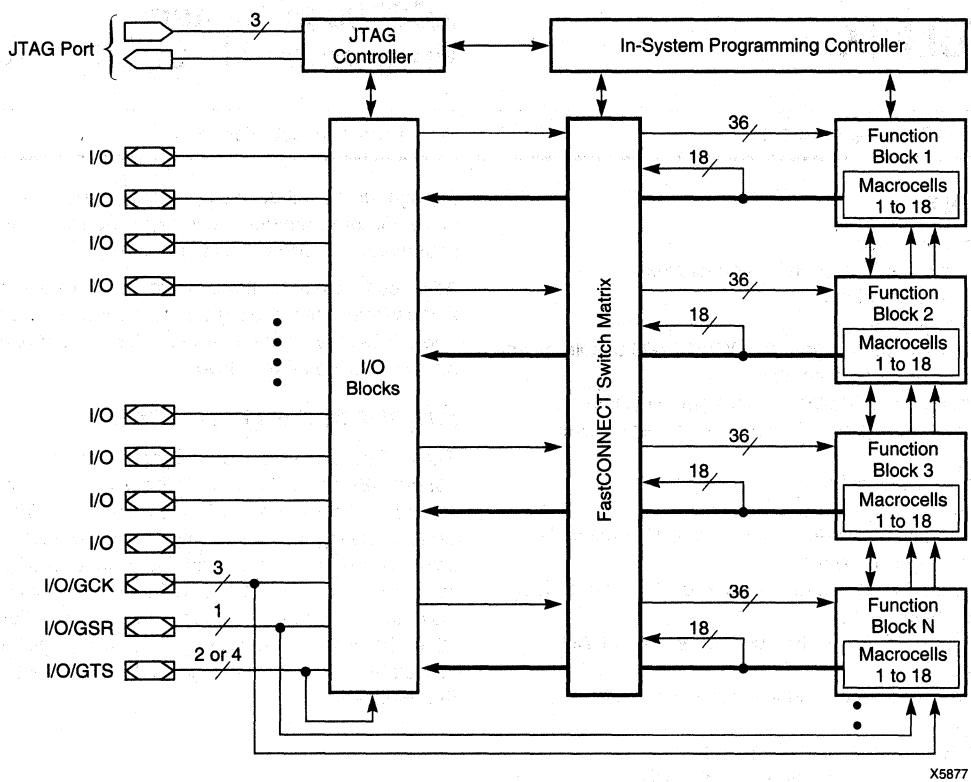


Figure 1: XC9500 Architecture

Table 1: XC9500 Device Family

	XC9536	XC9572	XC95108	XC95144	XC95180	XC95216	XC95288	XC95432	XC95576
Macrocells	36	72	108	144	180	216	288	432	576
Usable Gates	800	1,600	2,400	3,200	4,000	4,800	6,400	9600	12,800
Registers	36	72	108	144	180	216	288	432	576
t_{PD} (ns)	5	7.5	7.5	7.5	10	10	10	10	12
t_{SU} (ns)	4.5	5.5	5.5	5.5	6.5	6.5	6.5	6.5	9.5
t_{CO} (ns)	4.5	5.5	5.5	5.5	6.5	6.5	6.5	6.5	9.5
f_{CNT} (MHz)	125	125	125	125	111	111	111	111	100
f_{SYSTEM} (MHz)	100	83	83	83	67	67	67	67	67
Preliminary									

Note: f_{CNT} = Operating frequency for 16-bit counters
f_{SYSTEM} = Internal operating frequency for general purpose system designs spanning multiple FBs.

Table 2: Available Packages and Device I/O Pins

	XC9536	XC9572	XC95108	XC95144	XC95180	XC95216	XC95288	XC95432	XC95576
44-Pin PLCC	34								
44-Pin VQFP	34								
84-Pin PLCC		69	69						
100-Pin PQFP		72	81	81					
100-Pin TQFP		72	81						
160-Pin PQFP			108	133	133	133			
208-Pin HQFP					166	166	168		
304-Pin HQFP							192	232	232

Note: Does not include the dedicated JTAG pins.

Function Block

Each Function Block, as shown in Figure 2, is comprised of 18 independent macrocells, each capable of implementing a combinatorial or registered function. The FB also receives global clock, output enable, and set/reset signals. The FB generates 18 outputs that drive the FastCONNECT switch matrix. These 18 outputs and their corresponding output enable signals also drive the IOB.

Logic within the FB is implemented using a sum-of-products representation. Thirty-six inputs provide 72 true and complement signals into the programmable AND-array to form 90 product terms. Any number of these product terms, up to the 90 available, can be allocated to each macrocell by the product term allocator.

Each FB supports local feedback paths that allow any number of FB outputs to drive into its own programmable AND-array without going outside the FB.

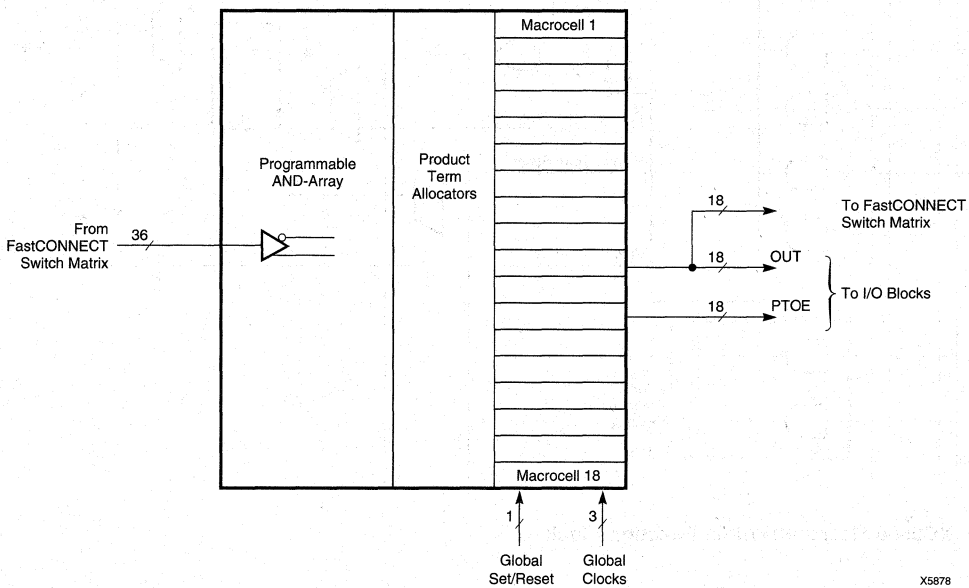


Figure 2: XC9500 Function Block

Macrocell

Each XC9500 macrocell may be individually configured for a combinatorial or registered function. The macrocell and associated FB logic is shown in Figure 3.

Five direct product terms from the AND-array are available for use as primary data inputs (to the OR and XOR gates) to implement combinatorial functions, or as control inputs including clock, set/reset, and output enable. The product term allocator associated with each macrocell selects how the five direct terms are used.

The macrocell register can be configured as a D-type or T-type flip-flop, or it may be bypassed for combinatorial operation. Each register supports both asynchronous set and reset operations. During power-up, all user registers are initialized to the user-defined preload state (default to 0 if unspecified).

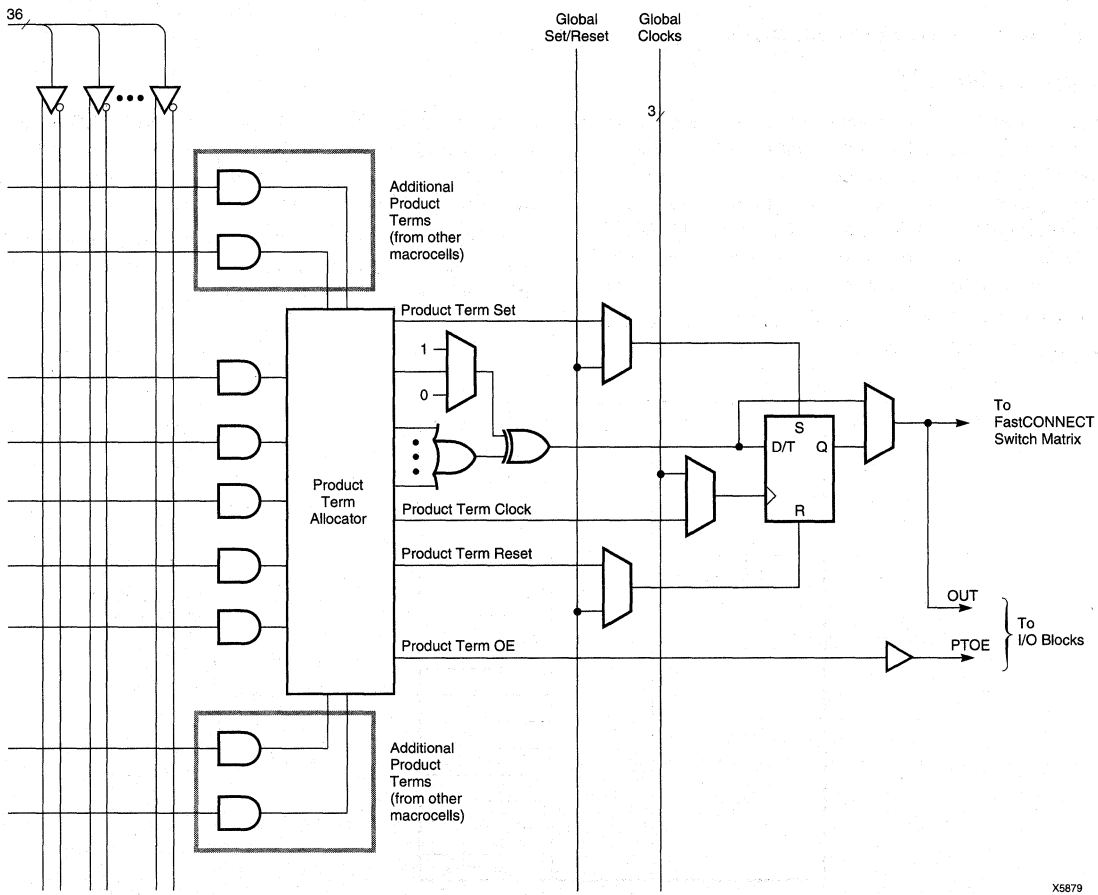


Figure 3: XC9500 Macrocell Within Function Block

All global control signals are available to each individual macrocell, including clock, set/reset, and output enable signals. As shown in Figure 4, the macrocell register clock originates from either of three global clocks or a product term clock. Both true and complement polarities of a GCK pin can be used within the device. A GSR input is also provided to allow user registers to be set to a user-defined state.

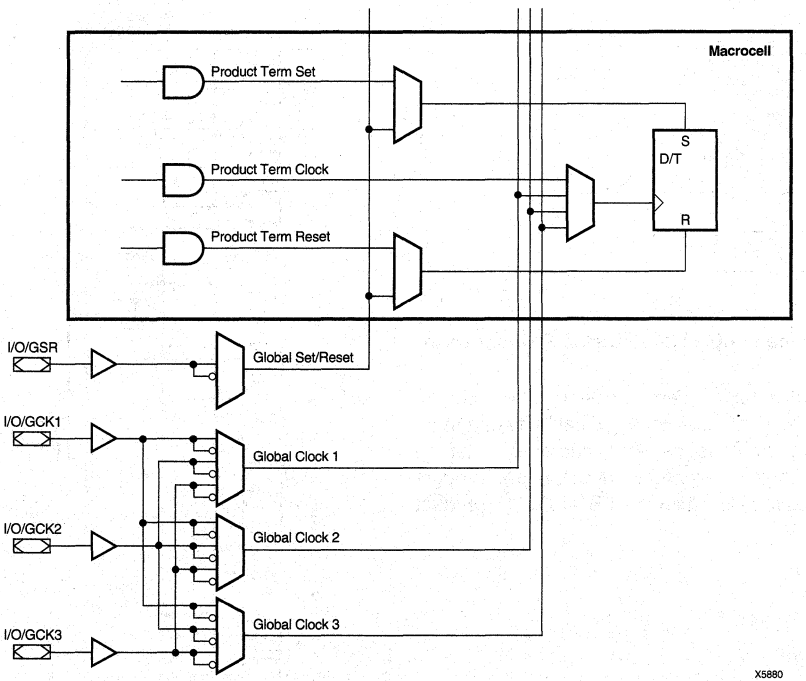


Figure 4: Macrocell Clock and Set/Reset Capability

Product Term Allocator

The product term allocator controls how the five direct product terms are assigned to each macrocell. For example, all five direct terms can drive the OR function as shown in Figure 5.

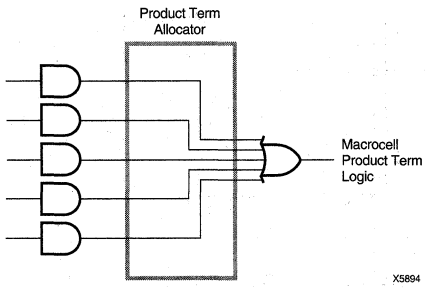


Figure 5: Macrocell Logic Using Direct Product Term

The product term allocator can re-assign other product terms within the FB to increase the logic capacity of a macrocell beyond five direct terms. Any macrocell requiring additional product terms can access uncommitted product terms in other macrocells within the FB. Up to 15 product terms can be available to a single macrocell with only a small incremental delay of t_{PTA}, as shown in Figure 6.

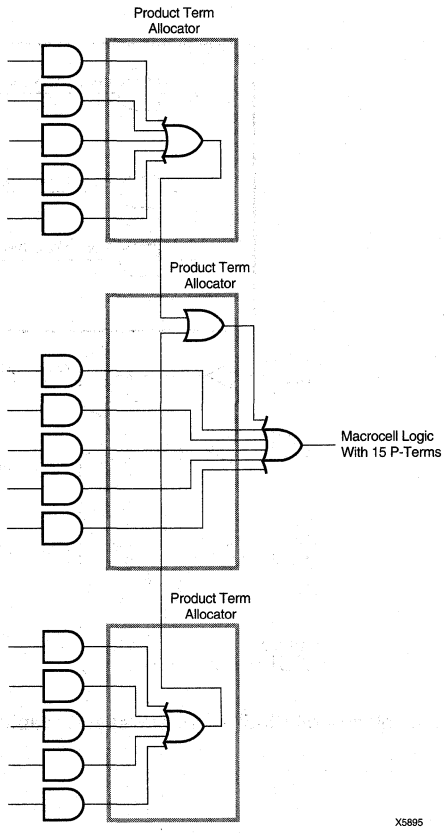


Figure 6: Product Term Allocation With 15 Product Terms

The product term allocator can re-assign product terms from any macrocell within the FB by combining partial sums of products over several macrocells, as shown in Figure 7.

In this example, the incremental delay is only $2*t_{PTA}$. All 90 product terms are available to any macrocell, with a maximum incremental delay of $8*t_{PTA}$.

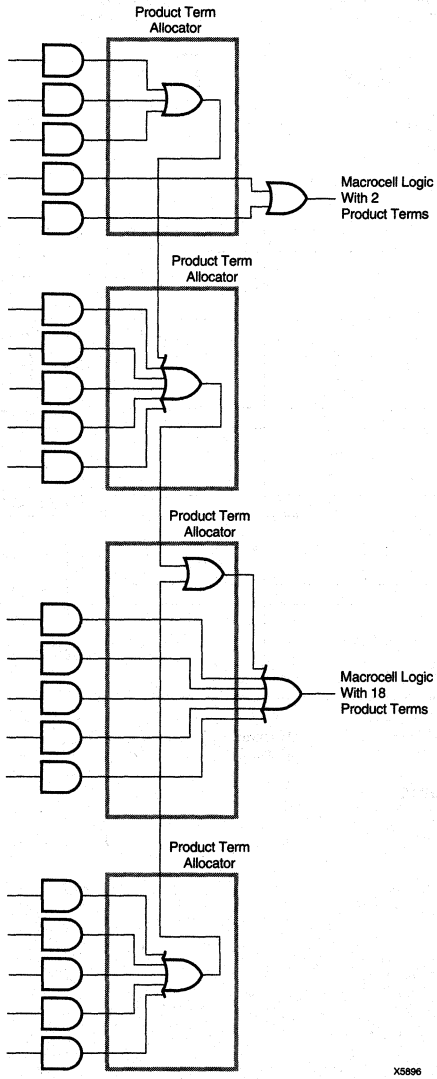


Figure 7: Product Term Allocation Over Several Macrocells

The internal logic of the product term allocator is shown in Figure 8.

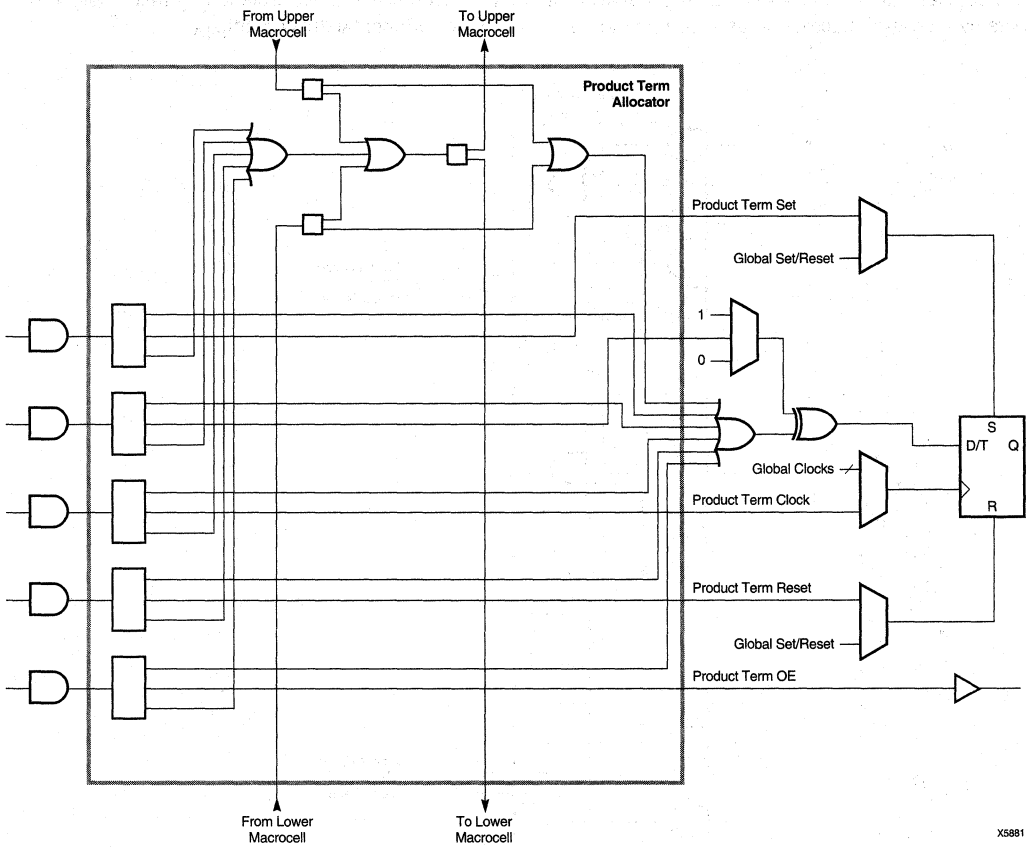


Figure 8: Product Term Allocator Logic

FastCONNECT Switch Matrix

The FastCONNECT switch matrix connects signals to the FB inputs, as shown in Figure 9. All IOB outputs (corresponding to user pin inputs) and all FB outputs drive the FastCONNECT matrix. Any of these (up to a FB fan-in limit of 36) may be programmably selected to drive each FB with a uniform delay.

The FastCONNECT switch matrix is capable of combining multiple internal connections into a single wired-AND output before driving the destination FB. This provides additional logic capability and increases the effective logic fan-in of the destination FB without any additional timing delay. This capability is available for internal connections originating from FB outputs only. It is automatically invoked by the development software where applicable.

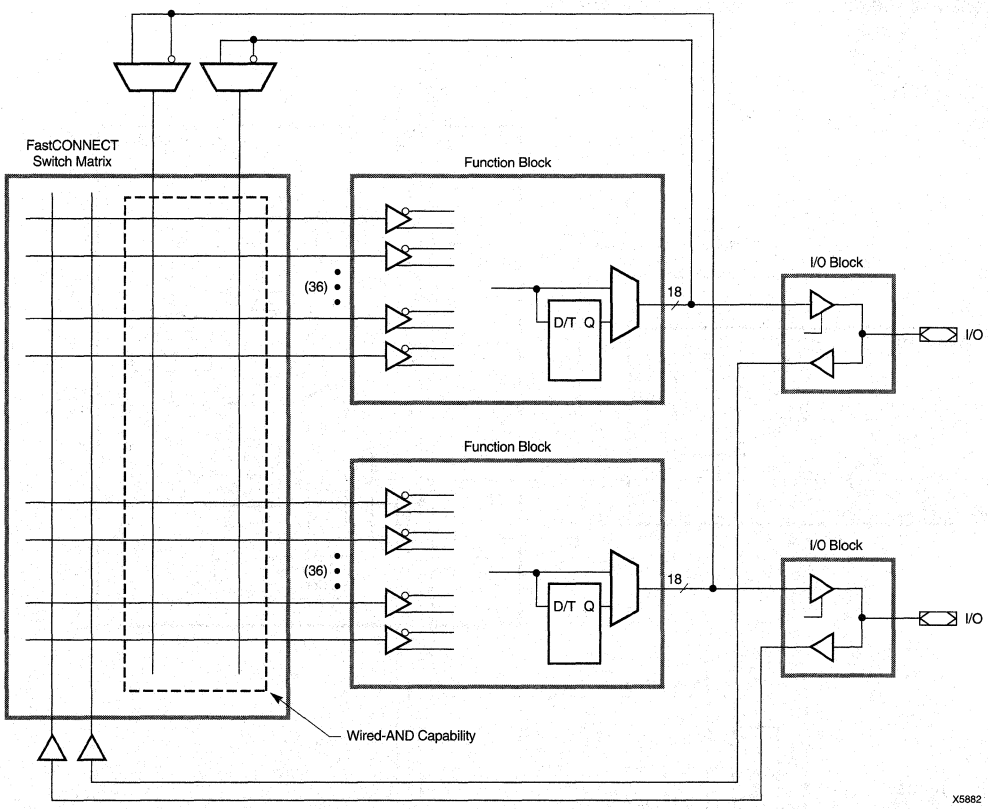


Figure 9: FastCONNECT Switch Matrix

I/O Block

The I/O Block (IOB) interfaces between the internal logic and the device user I/O pins. Each IOB includes an input buffer, output driver, output enable selection multiplexer, and user programmable ground control. See Figure 10 for details.

The input buffer is compatible with standard 5 V CMOS, 5 V TTL and 3.3 V signal levels. The input buffer uses the internal 5 V voltage supply (V_{CCINT}) to ensure that the input thresholds are constant and do not vary with the V_{CCIO} voltage.

The output enable may be generated from one of four options: a product term signal from the macrocell, any of the global OE signals, always "1", or always "0". There are two global output enables for devices with up to 144 macrocells, and four global output enables for devices with 180 or more macrocells. Both polarities of any of the global 3-state control (GTS) pins may be used within the device.

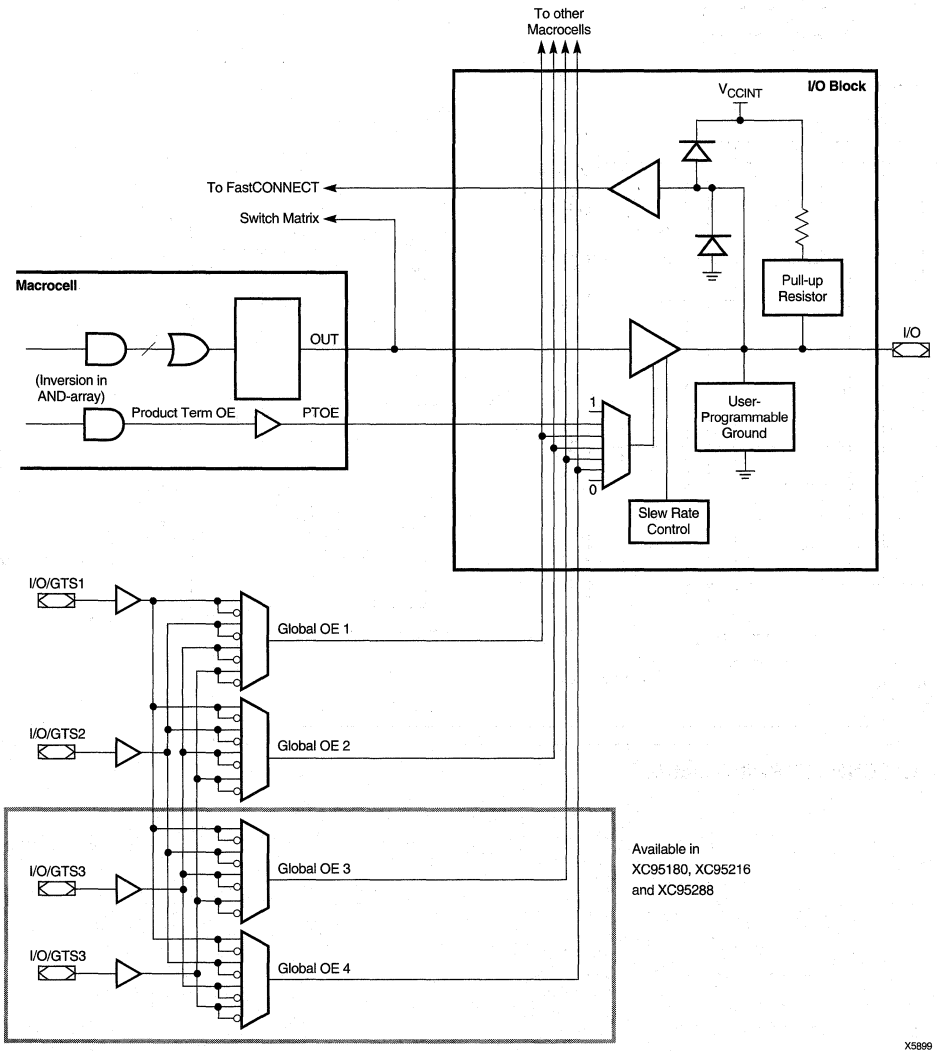


Figure 10: I/O Block and Output Enable Capability

Each output has independent slew rate control. Output edge rates may be programmably slowed down to reduce system noise (with an additional time delay of t_{SLEW}). See Figure 11.

Each IOB provides user programmable ground pin capability. This allows device I/O pins to be configured as additional ground pins. By tying strategically located programmable ground pins to the external ground connection, system noise generated from large numbers of simultaneous switching outputs may be reduced.

A control pull-up resistor (typically 10K ohms) is attached to each device I/O pin to prevent device pins from floating when the device is not in normal user operation. This resistor is active during device programming mode and system power-up. It is also activated for an erased device. The resistor is deactivated during normal operation.

The output driver is capable of supplying 24 mA output drive. All output drivers in the device may be configured for either 5 V TTL levels or 3.3 V levels by connecting the device output voltage supply (V_{CCIO}) to a 5 V or 3.3 V voltage supply. Figure 12 shows how the XC9500 device can be used in 5 V only and mixed 3.3 V/5 V systems.

Pin-Locking Capability

The capability to lock the user defined pin assignments during design changes depends on the ability of the architecture to adapt to unexpected changes. The XC9500 devices have architectural features that enhance the ability to accept design changes while maintaining the same pinout.

The XC9500 provides 100% routing within the FastCONNECT switch matrix, and incorporates a flexible Function Block that allows block-wide allocation of available p-terms. This provides a high level of confidence of maintaining both input and output pin assignments for unexpected design changes.

For extensive design changes requiring higher logic capacity than is available in the initially chosen device, the new design may be able to fit into a larger pin-compatible device using the same pin assignments.

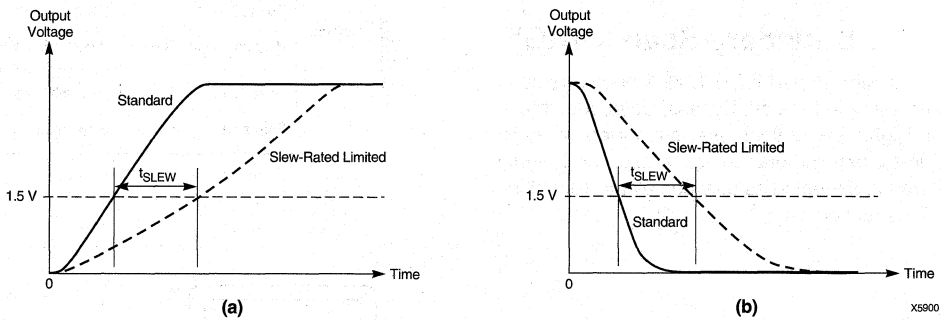


Figure 11: Output Slew-Rate Control For (a) Rising and (b) Falling Outputs

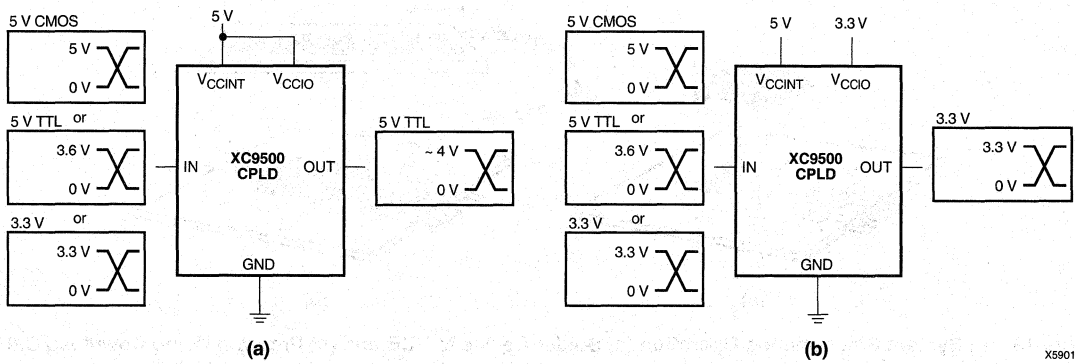


Figure 12: XC9500 Devices in (a) 5 V Systems and (b) Mixed 3.3 V/5 V Systems

In-System Programming

XC9500 devices are programmed in-system via a standard 4-pin JTAG protocol, as shown in Figure 13. In-system programming offers quick and efficient design iterations and eliminates package handling. The Xilinx development system provides the programming data sequence using a download cable, a third-party JTAG development system, JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence.

The system designer must ensure that the system is well-behaved before the XC9500 device is programmed with a user pattern. During XC9500 programming, all I/Os are tri-stated and pulled-up.

XC9500 devices also can be programmed by third-party device programmers.

Endurance

All XC9500 CPLDs provide a minimum endurance level of 10,000 in-system program/erase cycles. Each device meets all functional, performance, and data retention specifications within this endurance limit.

IEEE 1149.1 Boundary-Scan (JTAG)

XC9500 devices fully support IEEE 1149.1 boundary-scan (JTAG). Extest, Sample/Preload, Bypass, Usercode, Intest, Idcode, and Highz instructions are supported in each device. All in-system programming, erase, and verify instructions are implemented as fully compliant extensions of the 1149.1 instruction set.

Refer to the application note on the XC9500 JTAG instruction set for additional information.

Design Security

XC9500 devices incorporate advanced data security features which fully protect the programming data against unauthorized reading or inadvertent device erasure/reprogramming. Table 3 shows the four different security settings available.

The read security bits can be set by the user to prevent the internal programming pattern from being read or copied. Erasing the entire device is the only way to reset the read security bit.

The write security bits provide added protection against accidental device erasure or reprogramming by the user. Once set, the write-protection may be deactivated when the device needs to be reprogrammed with a valid pattern.

Table 3: Data Security Options

Write Security	Read Security: Default	Read Security: Set
Default	Read Allowed Program/Erase Allowed	Read Inhibited Program/Erase Allowed
Set	Read Allowed Program/Erase Inhibited	Read Inhibited Program/Erase Inhibited

X5905

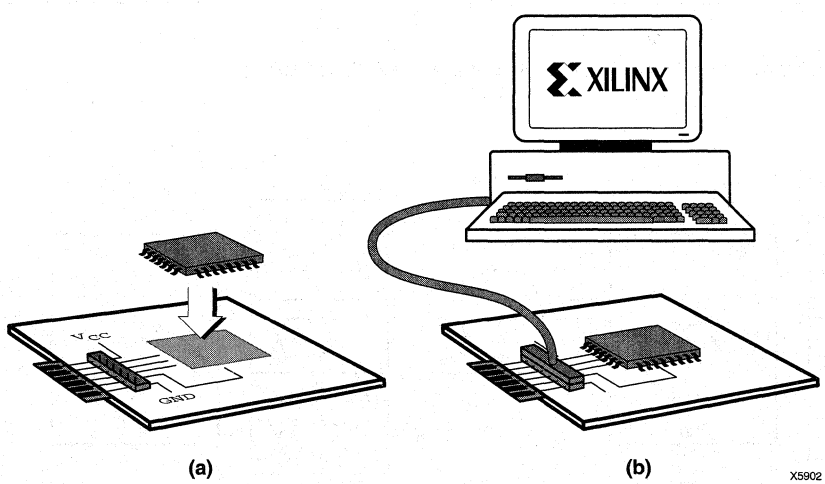


Figure 13: In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable

Low Power Mode

All XC9500 devices offer a low-power mode for individual macrocells or across all macrocells. This feature allows the device power to be significantly reduced.

Each individual macrocell may be programmed in low-power mode by the user. Performance-critical parts of the application can remain in standard power mode, while other parts of the application may be programmed for low-power operation to reduce the overall power dissipation. Macrocells programmed for low-power mode incur additional delay (t_{LP}) in pin-to-pin combinatorial delay as well as register setup time. Product term clock to output and product term output enable delays are unaffected by the macrocell power-setting.

Timing Model

The uniformity of the XC9500 architecture allows a simplified timing model for the entire device. The basic timing model is shown in Figure 14. Detailed timing information on a design, including secondary parameters, can be easily obtained from the timing report in the XACT*step* development system.

The basic timing model is valid for macrocell functions that use the direct product terms only, with standard power setting, and standard slew rate setting. Table 4 shows how each of the key timing parameters is affected by the product term allocator (if needed), low-power setting, and slew-limited setting.

The product term allocation time depends on the logic span of the macrocell function, which is defined as one less than the maximum number of allocators in the product term path. If only direct product terms are used, then the logic span is 0. The Figure 6 example shows that up to 15 product terms are available with a span of 1. In the case of Figure 7, the 18 product term function has a span of 2.

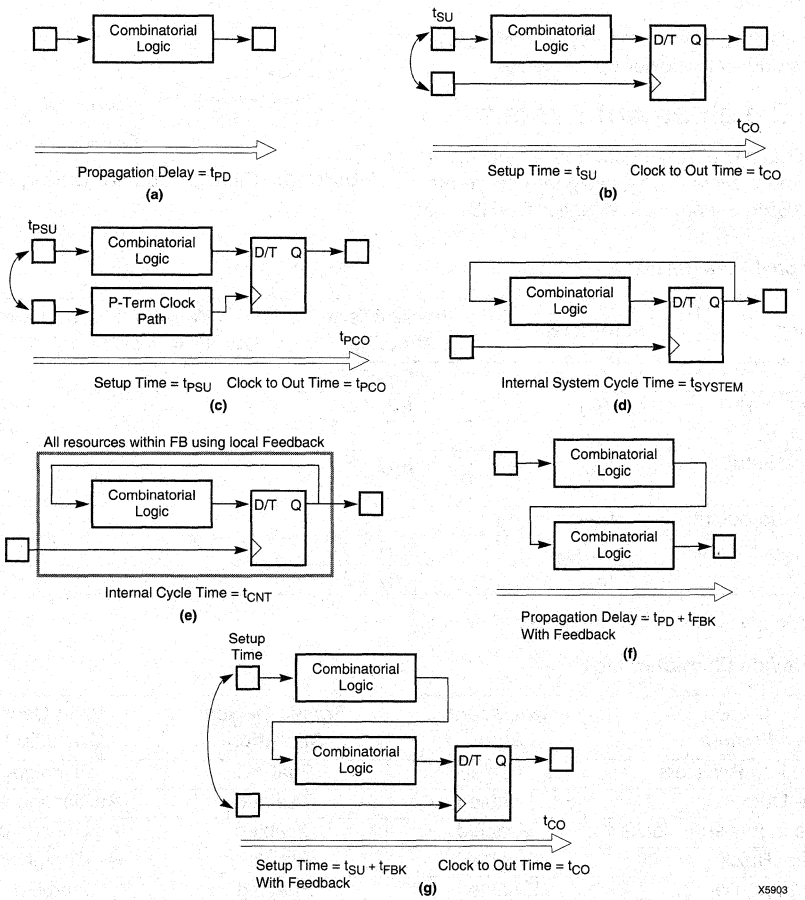


Figure 14: Basic Timing Model

Power-Up Characteristics

The XC9500 devices are well behaved under all operating conditions. During power-up each XC9500 device employs internal circuitry which keeps the device in the quiescent state until V_{CCINT} supply voltage is at a safe level (approximately 3.8 V). During this time, all device pins and JTAG pins are disabled, and all device outputs are disabled with the IOB pull-up resistors (~ 10K ohms) enabled. See Table 5. When the supply voltage reaches a safe level, all user registers become initialized (within 100 µs typical), and the device is immediately available for operation, as shown in Figure 15.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with the IOB pull-up resistors enabled. The JTAG pins are enabled to allow the device to be programmed at any time.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

In mixed 3.3 V/5 V systems, it is recommended that $V_{CCINT} \geq V_{CCIO}$ at all times during the power-up sequence.

XACT*step*™ Development System

The XC9500 CPLD family is fully supported by the Xilinx XACT*step* development system. The designer can create the design using ABEL, schematics, equations, VHDL or other HDL languages in a variety of software front-end-tools. The XACT*step* development system can be used to implement the design and generate a JEDEC bitmap which can be used to program the XC9500 device. The XACT*step* development system includes JTAG download software that can be used to program the devices via a download cable.

FastFLASH Technology

An advanced 0.6 µm CMOS Flash process is used to fabricate all XC9500 devices. Specifically developed for Xilinx in-system programmable CPLDs, the process provides high performance logic capability and endurance of 10,000 program/erase cycles.

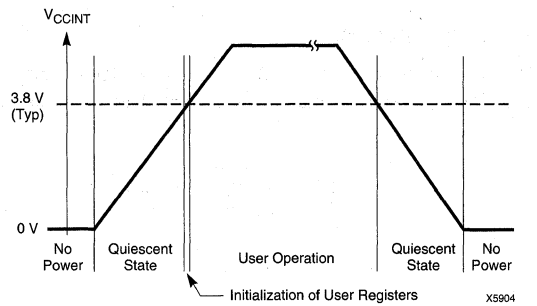


Figure 15: Device Behavior During Power-up

Table 4: Timing Model Parameters

Description	Parameter	Product Term Allocator[1]	Macrocell Low-Power Setting	Output Slew-Limited Setting
Propagation Delay	t_{PD}	+ t_{PTA} * S	+ t_{LP}	+ t_{SLEW}
Global Clock Setup Time	t_{SU}	+ t_{PTA} * S	+ t_{LP}	–
Global Clock-to-output	t_{CO}	–	–	+ t_{SLEW}
Product Term Clock Setup Time	t_{PSU}	+ t_{PTA} * S	+ t_{LP}	–
Product Term Clock-to-output	t_{PCO}	–	–	+ t_{SLEW}
Internal System Cycle Period	t_{SYSTEM}	+ t_{PTA} * S	+ t_{LP}	–
Feedback Time	t_{FBK}	+ t_{PTA} * S	+ t_{LP}	–

Note: 1. S = the logic span of the function, as defined in the text.

Table 5: XC9500 Device Characteristics

Device Feature	Quiescent State	Erased Device Operation	Valid User Operation
IOB Pull-up Resistors	Enabled	Enabled	Disabled
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

XC9536 In-System Programmable CPLD

June 1, 1996 (Version 1.0)

Preliminary Product Specification

Features

- 5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 125 MHz
- 36 macrocells with 800 usable gates
- Up to 34 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-5, -7, -10 speed grades)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 44-pin PLCC and 44-pin VQFP packages

Description

The XC9536 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of two 36V18 Function Blocks, providing 800 usable gates with propagation delays of 5 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC9536 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC9536 device.

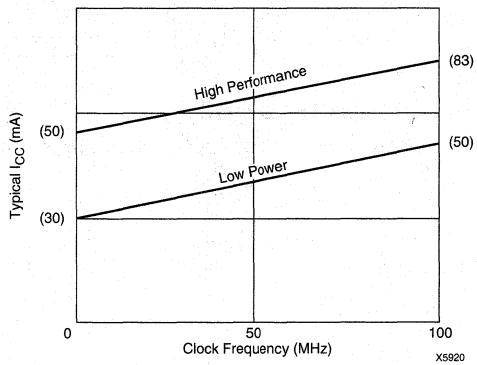


Figure 1: Typical I_{CC} vs. Frequency For XC9536

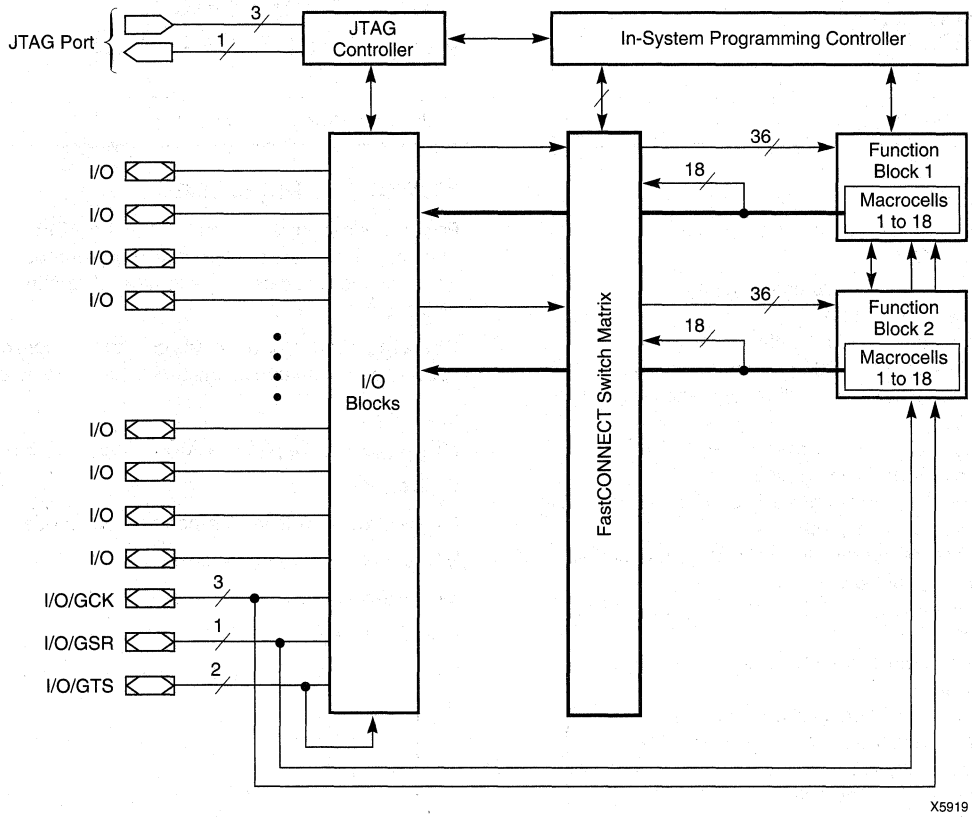


Figure 2: XC9536 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 ns @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions[1]

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	V_{CCINT} +0.5	V
V_O	Output voltage	0	V_{CCINT} + 0.5	V
T_{IN}	Input signal transition time		50	ns

Note 1. Numbers in parenthesis are for industrial-temperature range versions.

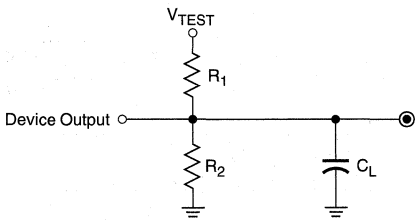
DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5 V operation	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	Output low voltage for 5 V operation	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	30 mA Typ		

AC Characteristics

Symbol	Parameter	XC9536-5		XC9536-7		XC9536-10		XC9536-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	I/O to output valid		5.0		7.5		10		15	ns
t_{SU}	I/O setup time before GCK	4.5		5.5		6.5		8.0		ns
t_{H}	I/O hold time after GCK	0		0		0		0		ns
t_{CO}	GCK to output valid		4.5		5.5		6.5		8.0	ns
f_{CNT}	16-bit counter frequency	125		125		111.0		95.0		MHz
f_{SYSTEM} [1]	Multiple FB Internal Operating Frequency	100		83.0		67.0		55.0		MHz
t_{PSU}	I/O setup time before p-term clock input	0.5		0.5		1.0		2.0		ns
t_{PH}	I/O hold time after p-term clock input	4.0		5.0		5.5		6.0		ns
t_{PCO}	P-term clock to output valid		7.5		10.5		12.0		14.0	ns
t_{OE}	GTS to output valid		6.0		7.0		10.0		15.0	ns
t_{OD}	GTS to output disable		6.0		7.0		10.0		15.0	ns
t_{POE}	Product term OE to output valid		10.5		13.0		15.5		18.0	ns
t_{POD}	Product term OE to output disable		10.5		13.0		15.5		18.0	ns
t_{PTA}	Product term allocator delay		1.5		1.5		2.0		2.0	ns
t_{FBK}	Internal combinatorial feedback delay		NA		8.5		12.0		17.0	ns
t_{WLH}	GCK pulse width (High or Low)	4.0		4.0		4.5		5.0		ns
f_{TOG}	Export Control Max. flip-flop toggle rate		125		125		111		100	MHz
t_{SLEW}	Slew rate time delay		3.5		4.0		4.5		5.5	ns
t_{LP}	Low power time delay adder		8.0		8.0		8.5		8.5	ns
		Preliminary								

Note: 1. f_{SYSTEM} = internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

Figure 3: AC Load Circuit

XC9536 I/O Pins

Function Block	Macrocell	PC44	VQ44	BScan Order	Notes
1	1	2	40	105	
1	2	3	41	102	
1	3	5	43	99	[1]
1	4	4	42	96	
1	5	6	44	93	[1]
1	6	8	2	90	
1	7	7	1	87	[1]
1	8	9	3	84	
1	9	11	5	81	
1	10	12	6	78	
1	11	13	7	75	
1	12	14	8	72	
1	13	18	12	69	
1	14	19	13	66	
1	15	20	14	63	
1	16	22	16	60	
1	17	24	18	57	
1	18	–	–	54	

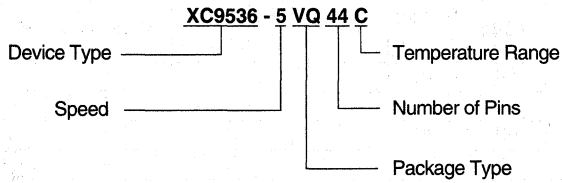
Function Block	Macrocell	PC44	VQ44	BScan Order	Notes
2	1	1	39	51	
2	2	44	38	48	
2	3	42	36	45	[1]
2	4	43	37	42	
2	5	40	34	39	[1]
2	6	39	33	36	[1]
2	7	38	32	33	
2	8	37	31	30	
2	9	36	30	27	
2	10	35	29	24	
2	11	34	28	21	
2	12	33	27	18	
2	13	29	23	15	
2	14	28	22	12	
2	15	27	21	9	
2	16	26	20	6	
2	17	25	19	3	
2	18	–	–	0	

Note: [1] Global control pin

XC9536 Global, JTAG and Power Pins

Pin Type	PC44	VQ44
I/O/GCK1	5	43
I/O/GCK2	6	44
I/O/GCK3	7	1
I/O/GTS1	42	36
I/O/GTS2	40	34
I/O/GSR	39	33
TCK	17	11
TDI	15	9
TDO	30	24
TMS	16	10
V_{CCINT} 5 V	21,41	15,35
V_{CCIO} 3.3 V/5 V	32	26
GND	23,10,31	17,4,25
No Connects	—	—

Ordering Information



Speed Options

-15	15 ns pin-to-pin delay
-10	10 ns pin-to-pin delay
-7	7.5 ns pin-to-pin delay
-5	5 ns pin-to-pin delay

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C

Packaging Options

PC44	44-Pin Plastic Leaded Chip Carrier (PLCC)
VQ44	44-Pin Very Thin Quad Flat Pack (VQFP)

X5952

Component Availability

Pins		44		84	100		160	208
Type		Plastic PLCC	Plastic VQFP	Plastic PLCC	Plastic PQFP	Plastic TQFP	Plastic PQFP	Power QFP
Code		PC44	VQ44	PC84	PQ100	TQ100	PQ160	HQ208
XC9536	-15	C(I)	C(I)					
	-10	C(I)	C(I)					
	-7	C	C					
	-5	C	C					

X5907

XC9572 In-System Programmable CPLD

June 1, 1996 (Version 1.0)

Advance Product Specification

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 125 MHz
- 72 macrocells with 1,600 usable gates
- Up to 72 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 84-pin PLCC, 100-pin PQFP and 100-pin TQFP packages

Description

The XC9572 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of four 36V18 Function Blocks, providing 1,600 usable gates with propagation delays of 7.5 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC9572 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

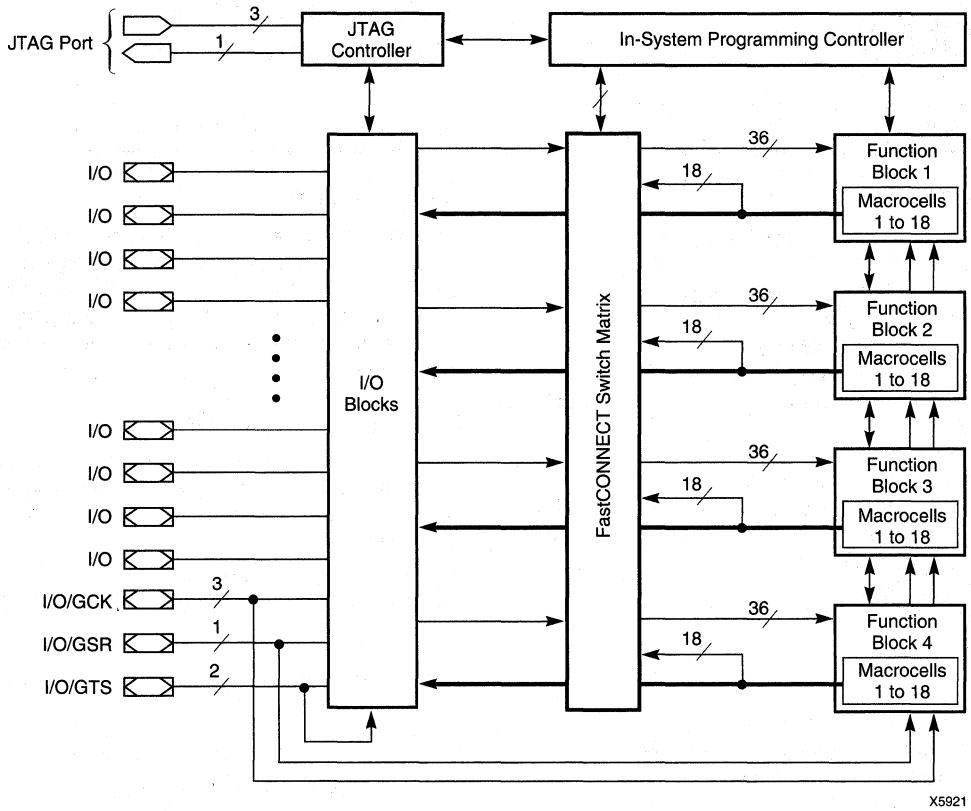


Figure 1: XC9572 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

XC9572 I/O Pins

Function Block	Macrocell	PC84	PQ100	TQ100	BScan Order	Notes
1	1	4	18	16	213	
1	2	1	15	13	210	
1	3	6	20	18	207	
1	4	7	22	20	204	
1	5	2	16	14	201	
1	6	3	17	15	198	
1	7	11	27	25	195	
1	8	5	19	17	192	
1	9	9	24	22	189	[1]
1	10	13	30	28	186	
1	11	10	25	23	183	[1]
1	12	18	35	33	180	
1	13	20	38	36	177	
1	14	12	29	27	174	[1]
1	15	14	31	29	171	
1	16	23	41	39	168	
1	17	15	32	30	165	
1	18	24	42	40	162	
2	1	63	89	87	159	
2	2	69	96	94	156	
2	3	67	93	91	153	
2	4	68	95	93	150	
2	5	70	97	95	147	
2	6	71	98	96	144	
2	7	76	5	3	141	[1]
2	8	72	99	97	138	
2	9	74	1	99	135	[1]
2	10	75	3	1	132	
2	11	77	6	4	129	[1]
2	12	79	8	6	126	
2	13	80	10	8	123	
2	14	81	11	9	120	
2	15	83	13	11	117	
2	16	82	12	10	114	
2	17	84	14	12	111	
2	18	–	94	92	108	
3	1	25	43	41	105	
3	2	17	34	32	102	
3	3	31	51	49	99	
3	4	32	52	50	96	
3	5	19	37	35	93	
3	6	34	55	53	90	
3	7	35	56	54	87	
3	8	21	39	37	84	
3	9	26	44	42	81	
3	10	40	62	60	78	
3	11	33	54	52	75	
3	12	41	63	61	72	
3	13	43	65	63	69	
3	14	36	57	55	66	
3	15	37	58	56	63	
3	16	45	67	65	60	
3	17	39	60	58	57	
3	18	–	61	59	54	
4	1	46	68	66	51	
4	2	44	66	64	48	
4	3	51	73	71	45	
4	4	52	74	72	42	
4	5	47	69	67	39	
4	6	54	78	76	36	
4	7	55	79	77	33	
4	8	48	70	68	30	
4	9	50	72	70	27	
4	10	57	83	81	24	
4	11	53	76	74	21	
4	12	58	84	82	18	
4	13	61	87	85	15	
4	14	56	80	78	12	
4	15	65	91	89	9	
4	16	62	88	86	6	
4	17	66	92	90	3	
4	18	–	81	79	0	

Notes: [1] Global control pin

XC9572 Global, JTAG and Power Pins

Pin Type	PC84	PQ100	TQ100
I/O/GCK1	9	24	22
I/O/GCK2	10	25	23
I/O/GCK3	12	29	27
I/O/GTS1	76	5	3
I/O/GTS2	77	6	4
I/O/GSR	74	1	99
TCK	30	50	48
TDI	28	47	45
TDO	59	85	83
TMS	29	49	47
V_{CCINT} 5 V	38,73,78	7,59,100	5,57,98
V_{CCIO} 3.3 V/5 V	22,64	28,40,53,90	26,38,51,88
GND	8,16,27,42,49,60	2,23,33,46,64,71,77,86	100,21,31,44,62,69,75,84
No Connects	—	4,9,21,26,36,45,48,75,82	2,7,19,24,34,43,46,73,80

XC95108 In-System Programmable CPLD

June 1, 1996 (Version 1.0)

Preliminary Product Specification

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 125 MHz
- 108 macrocells with 2400 usable gates
- Up to 108 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 84-pin PLCC, 100-pin PQFP, 100-pin TQFP and 160-pin PQFP packages

Description

The XC95108 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of six 36V18 Function Blocks, providing 2,400 usable gates with propagation delays of 7.5 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95108 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC95108 device.

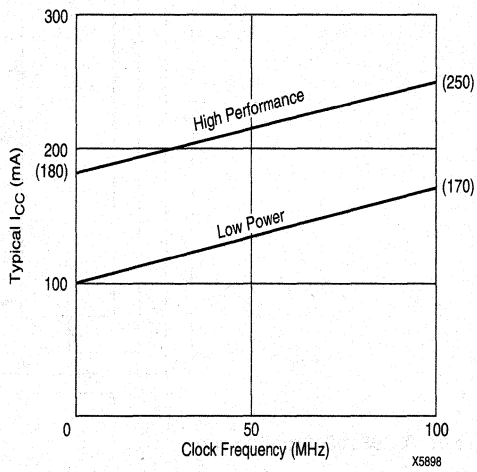


Figure 1: Typical I_{CC} vs. Frequency for XC95108

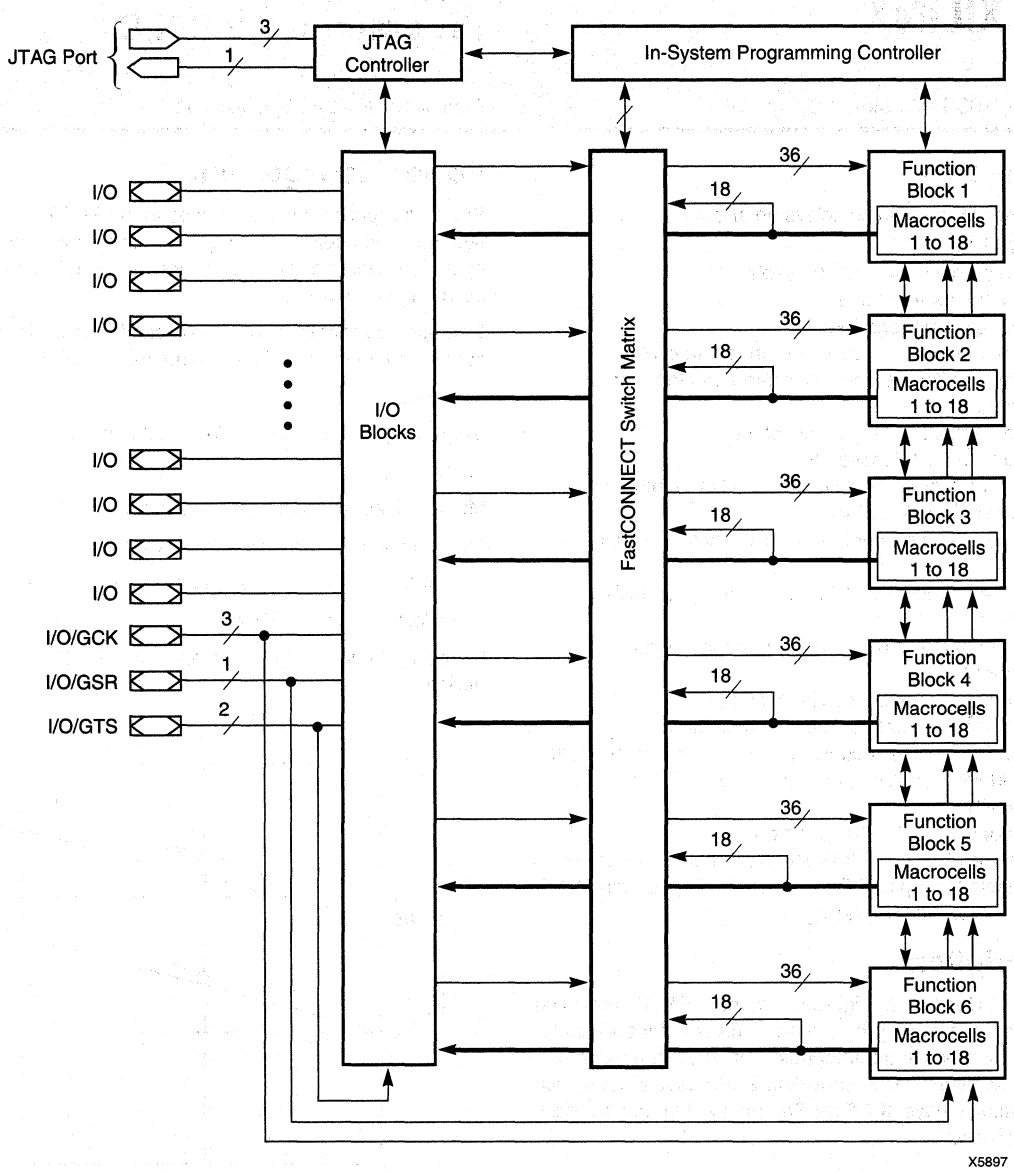


Figure 2: XC95108 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 ns @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions[1]

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	V_{CCINT} +0.5	V
V_O	Output voltage	0	V_{CCINT} + 0.5	V
T_{IN}	Input signal transition time		50	ns

Note: 1. Numbers in parenthesis are for industrial-temperature range versions.

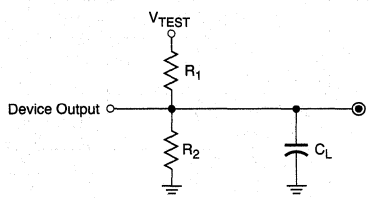
DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5 V operation	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	Output low voltage for 5 V operation	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	100 mA Typ		

AC Characteristics

Symbol	Parameter	XC95108-7		XC95108-10		XC95108-15		XC95108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	I/O to output valid		7.5		10		15		20	ns
t_{SU}	I/O setup time before GCK	5.5		6.5		8.0		10.0		ns
t_{H}	I/O hold time after GCK	0		0		0		0		ns
t_{CO}	GCK to output valid		5.5		6.5		8.0		10.0	ns
f_{CNT}	16-bit counter frequency	125		111		95.0		83.0		MHz
f_{SYSTEM} [1]	Multiple FB Internal Operating Frequency	83.0		67.0		55.0		50.0		MHz
t_{PSU}	I/O setup time before p-term clock input	0.5		1.0		2.0		4.0		ns
t_{PH}	I/O hold time after p-term clock input	5.0		5.5		6.0		6.0		ns
t_{PCO}	P-term clock to output valid		10.5		12.0		14.0		16.0	ns
t_{OE}	GTS to output valid		7.0		10.0		15.0		20.0	ns
t_{OD}	GTS to output disable		7.0		10.0		15.0		20.0	ns
t_{POE}	Product term OE to output valid		13.0		15.5		18.0		22.0	ns
t_{POD}	Product term OE to output disable		13.0		15.5		18.0		22.0	ns
t_{PTA}	Product term allocator delay		1.5		2.0		2.0		2.0	ns
t_{FBK}	Internal combinatorial feedback delay		8.5		12.0		17.0		20.0	ns
t_{WLH}	GCK pulse width (High or Low)	4.0		4.5		5.0		6.0		ns
f_{TOG}	Export Control Max. flip-flop toggle rate		125		111		100		83	MHz
t_{SLEW}	Slew rate time delay		4.0		4.5		5.0		5.5	ns
t_{LP}	Low power time delay adder		8.0		8.5		8.5		8.5	ns
		Preliminary								

Note: 1. f_{SYSTEM} = internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

Figure 3: AC Load Circuit

XC95108 I/O Pins

Function Block	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes	Function Block	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes
1	1	–	–	–	25	321		3	1	–	–	–	45	213	
1	2	1	15	13	21	318		3	2	14	31	29	47	210	
1	3	2	16	14	22	315		3	3	15	32	30	49	207	
1	4	–	21	19	29	312		3	4	–	36	34	57	204	
1	5	3	17	15	23	309		3	5	17	34	32	54	201	
1	6	4	18	16	24	306		3	6	18	35	33	56	198	
1	7	–	–	–	27	303		3	7	–	–	–	50	195	
1	8	5	19	17	26	300		3	8	19	37	35	58	192	
1	9	6	20	18	28	297		3	9	20	38	36	59	189	
1	10	–	26	24	36	294		3	10	–	45	43	69	186	
1	11	7	22	20	30	291		3	11	21	39	37	60	183	
1	12	9	24	22	33	288	[1]	3	12	23	41	39	62	180	
1	13	–	–	–	34	285		3	13	–	–	–	52	177	
1	14	10	25	23	35	282	[1]	3	14	24	42	40	63	174	
1	15	11	27	25	37	279		3	15	25	43	41	64	171	
1	16	12	29	27	42	276	[1]	3	16	26	44	42	68	168	
1	17	13	30	28	44	273		3	17	31	51	49	77	165	
1	18	–	–	–	43	270		3	18	–	–	–	74	162	
2	1	–	–	–	158	267		4	1	–	–	–	123	159	
2	2	71	98	96	154	264		4	2	57	83	81	134	156	
2	3	72	99	97	156	261		4	3	58	84	82	135	153	
2	4	–	4	2	4	258		4	4	–	82	80	133	150	
2	5	74	1	99	159	255	[1]	4	5	61	87	85	138	147	
2	6	75	3	1	2	252		4	6	62	88	86	139	144	
2	7	–	–	–	9	249		4	7	–	–	–	128	141	
2	8	76	5	3	6	246	[1]	4	8	63	89	87	140	138	
2	9	77	6	4	8	243	[1]	4	9	65	91	89	142	135	
2	10	–	9	7	12	240		4	10	–	–	–	147	132	
2	11	79	8	6	11	237		4	11	66	92	90	143	129	
2	12	80	10	8	13	234		4	12	67	93	91	144	126	
2	13	–	–	–	14	231		4	13	–	–	–	153	123	
2	14	81	11	9	15	228		4	14	68	95	93	146	120	
2	15	82	12	10	17	225		4	15	69	96	94	148	117	
2	16	83	13	11	18	222		4	16	–	94	92	145	114	
2	17	84	14	12	19	219		4	17	70	97	95	152	111	
2	18	–	–	–	16	216		4	18	–	–	–	155	108	

Notes: [1] Global control pin

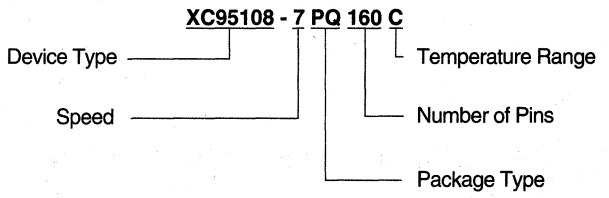
XC95108 I/O Pins (continued)

Function Block	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes	Function Block	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes
5	1	–	–	–	76	105		6	1	–	–	–	91	51	
5	2	32	52	50	79	102		6	2	45	67	65	103	48	
5	3	33	54	52	82	99		6	3	46	68	66	104	45	
5	4	–	48	46	72	96		6	4	–	75	73	116	42	
5	5	34	55	53	86	93		6	5	47	69	67	106	39	
5	6	35	56	54	88	90		6	6	48	70	68	108	36	
5	7	–	–	–	78	87		6	7	–	–	–	105	33	
5	8	36	57	55	90	84		6	8	50	72	70	111	30	
5	9	37	58	56	92	81		6	9	51	73	71	113	27	
5	10	–	–	–	84	78		6	10	–	–	–	107	24	
5	11	39	60	58	95	75		6	11	52	74	72	115	21	
5	12	40	62	60	97	72		6	12	53	76	74	117	18	
5	13	–	–	–	87	69		6	13	–	–	–	112	15	
5	14	41	63	61	98	66		6	14	54	78	76	122	12	
5	15	43	65	63	101	63		6	15	55	79	77	124	9	
5	16	–	61	59	96	60		6	16	–	81	79	129	6	
5	17	44	66	64	102	57		6	17	56	80	78	126	3	
5	18	–	–	–	89	54		6	18	–	–	–	114	0	

XC95108 Global, JTAG and Power Pins

Pin Type	PC84	PQ100	TQ100	PQ160
I/O/GCK1	9	24	22	33
I/O/GCK2	10	25	23	35
I/O/GCK3	12	29	27	42
I/O/GTS1	76	5	3	6
I/O/GTS2	77	6	4	8
I/O/GSR	74	1	99	159
TCK	30	50	48	75
TDI	28	47	45	71
TDO	59	85	83	136
TMS	29	49	47	73
V_{CCINT} 5 V	38,73,78	7,59,100	5,57,98	10,46,94,157
V_{CCIO} 3.3 V/5 V	22,64	28,40,53,90	26,38,51,88	1,41,61,81,121,141
GND	8,16,27,42,49,60	2,23,33,46,64,71,77,86	100,21,31,44,62,69,75,84	20,31,40,51,70,80,99
GND	–	–	–	100,110,120,127,137
GND	–	–	–	160

Ordering Information



Speed Options

-20	20 ns pin-to-pin delay
-15	15 ns pin-to-pin delay
-10	10 ns pin-to-pin delay
-7	7 ns pin-to-pin delay

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C

Packaging Options

PC84	84-Pin Plastic Leaded Chip Carrier (PLCC)
PQ100	100-Pin Plastic Quad Flat Pack (PQFP)
TQ100	100-Pin Thin Quad Flat Pack (TQFP)
PQ160	160-Pin Plastic Quad Flat Pack (PQFP)

X5953

Component Availability

Pins	44		84	100		160	208
Type	Plastic PLCC	Plastic VQFP	Plastic PLCC	Plastic PQFP	Plastic TQFP	Plastic PQFP	Power QFP
Code	PC44	VQ44	PC84	PQ100	TQ100	PQ160	HQ208
XC95108 -20			C(I)	C(I)	C(I)	C(I)	
XC95108 -15			C(I)	C(I)	C(I)	C(I)	
XC95108 -10			C(I)	C(I)	C(I)	C(I)	
XC95108 -7			C	C	C	C	

X5941

XC95144 In-System Programmable CPLD

June 1, 1996 (Version 1.0)

Advance Product Specification

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 144 macrocells with 3,200 usable gates
- Up to 133 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 100-pin PQFP, and 160-pin PQFP packages

Description

The XC95144 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of eight 36V18 Function Blocks, providing 3,200 usable gates with propagation delays of 7.5 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95144 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

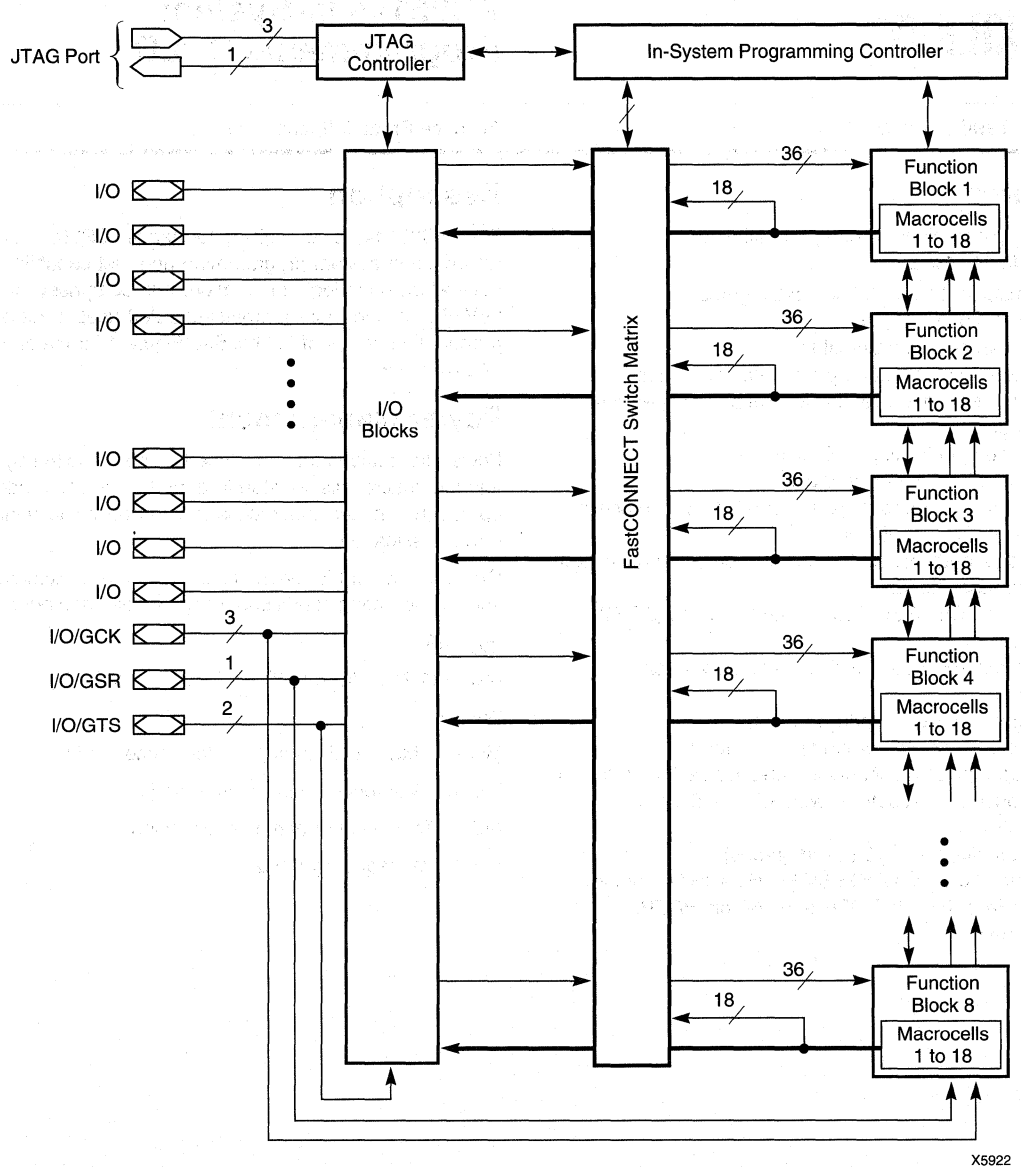


Figure 1: XC95144 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

XC95144 I/O Pins

Function Block	Macrocell	PQ100	PQ160	BScan Order	Notes
1	1	–	38	429	
1	2	15	21	426	
1	3	16	22	423	
1	4	–	25	420	
1	5	17	23	417	
1	6	18	24	414	
1	7	–	32	411	
1	8	19	26	408	
1	9	20	28	405	
1	10	–	74	402	
1	11	21	29	399	
1	12	22	30	396	
1	13	–	39	393	
1	14	24	33	390	[1]
1	15	25	35	387	[1]
1	16	–	78	384	
1	17	26	36	381	
1	18	–	–	378	
2	1	–	3	375	
2	2	4	4	372	[1]
2	3	–	147	369	
2	4	–	158	366	
2	5	5	6	363	[1]
2	6	6	8	360	[1]
2	7	–	7	357	
2	8	8	11	354	
2	9	9	12	351	
2	10	–	155	348	
2	11	10	13	345	
2	12	11	15	342	
2	13	–	5	339	
2	14	12	17	336	
2	15	13	18	333	
2	16	–	105	330	
2	17	14	19	327	
2	18	–	–	324	

Function Block	Macrocell	PQ100	PQ160	BScan Order	Notes
3	1	–	53	321	
3	2	27	37	318	
3	3	–	84	315	
3	4	–	45	312	
3	5	29	42	309	[1]
3	6	30	44	306	
3	7	–	48	303	
3	8	31	47	300	
3	9	32	49	297	
3	10	–	89	294	
3	11	34	54	291	
3	12	35	56	288	
3	13	–	55	285	
3	14	36	57	282	
3	15	37	58	279	
3	16	–	34	276	
3	17	38	59	273	
3	18	–	–	270	
4	1	–	149	267	
4	2	92	143	264	
4	3	–	107	261	
4	4	–	123	258	
4	5	93	144	255	
4	6	94	145	252	
4	7	–	151	249	
4	8	95	146	246	
4	9	96	148	243	
4	10	–	114	240	
4	11	97	152	237	
4	12	98	154	234	
4	13	–	150	231	
4	14	99	156	228	
4	15	1	159	225	[1]
4	16	–	14	222	
4	17	3	2	219	[1]
4	18	–	–	216	

Notes: [1] Global control pin

Macrocell outputs to package pins subject to change, contact factory for latest information. Power, GND, JTAG and Global Signals are fixed.

XC95144 I/O Pins (continued)

Function Block	Macrocell	PQ100	PQ160	BScan Order	Notes
5	1	–	65	213	
5	2	39	60	210	
5	3	–	27	207	
5	4	–	76	204	
5	5	41	62	201	
5	6	42	63	198	
5	7	–	67	195	
5	8	43	64	192	
5	9	44	68	189	
5	10	–	93	186	
5	11	45	69	183	
5	12	48	72	180	
5	13	–	66	177	
5	14	51	77	174	
5	15	52	79	171	
5	16	–	52	168	
5	17	54	82	165	
5	18	–	–	162	
6	1	–	–	159	
6	2	79	124	156	
6	3	–	9	153	
6	4	–	91	150	
6	5	80	126	147	
6	6	81	129	144	
6	7	–	131	141	
6	8	82	133	138	
6	9	83	134	135	
6	10	–	130	132	
6	11	84	135	129	
6	12	87	138	126	
6	13	–	132	123	
6	14	88	139	120	
6	15	89	140	117	
6	16	–	153	114	
6	17	91	142	111	
6	18	–	–	108	

Function Block	Macrocell	PQ100	PQ160	BScan Order	Notes
7	1	–	–	105	
7	2	55	86	102	
7	3	–	50	99	
7	4	–	43	96	
7	5	56	88	93	
7	6	57	90	90	
7	7	–	83	87	
7	8	58	92	84	
7	9	60	95	81	
7	10	–	109	78	
7	11	61	96	75	
7	12	62	97	72	
7	13	–	85	69	
7	14	63	98	66	
7	15	65	101	63	
7	16	–	87	60	
7	17	66	102	57	
7	18	–	–	54	
8	1	–	–	51	
8	2	67	103	48	
8	3	–	128	45	
8	4	–	16	42	
8	5	68	104	39	
8	6	69	106	36	
8	7	–	118	33	
8	8	70	108	30	
8	9	72	111	27	
8	10	–	125	24	
8	11	73	113	21	
8	12	74	115	18	
8	13	–	119	15	
8	14	75	116	12	
8	15	76	117	9	
8	16	–	112	6	
8	17	78	122	3	
8	18	–	–	0	

XC95144 Global, JTAG and Power Pins

Pin Type	PQ100	PQ160
I/O/GCK1	24	33
I/O/GCK2	25	35
I/O/GCK3	29	42
I/O/GTS1	5	6
I/O/GTS2	6	8
I/O/GTS3	3	2
I/O/GTS4	4	4
I/O/GSR	1	159
TCK	50	75
TDI	47	71
TDO	85	136
TMS	49	73
V_{CCINT} 5 V	7,59,100	10,46,94,157
V_{CCIO} 3.3 V/5 V	28,40,53,90	1,41,61,81,121,141
GND	2,23,33,46,64,71, 77,86	20,31,40,51,70,80, 99,100,110,120,127, 137,160
No Connects	–	–

XC95180 In-System Programmable CPLD

August 1, 1996 (Version 1.1)

Advance Product Specification

Features

- 10 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 180 macrocells with 4,000 usable gates
- Up to 166 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-10 speed grade)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 160-pin PQFP, and 208-pin HQFP packages

Description

The XC95180 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of ten 36V18 Function Blocks, providing 4,000 usable gates with propagation delays of 10 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95180 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

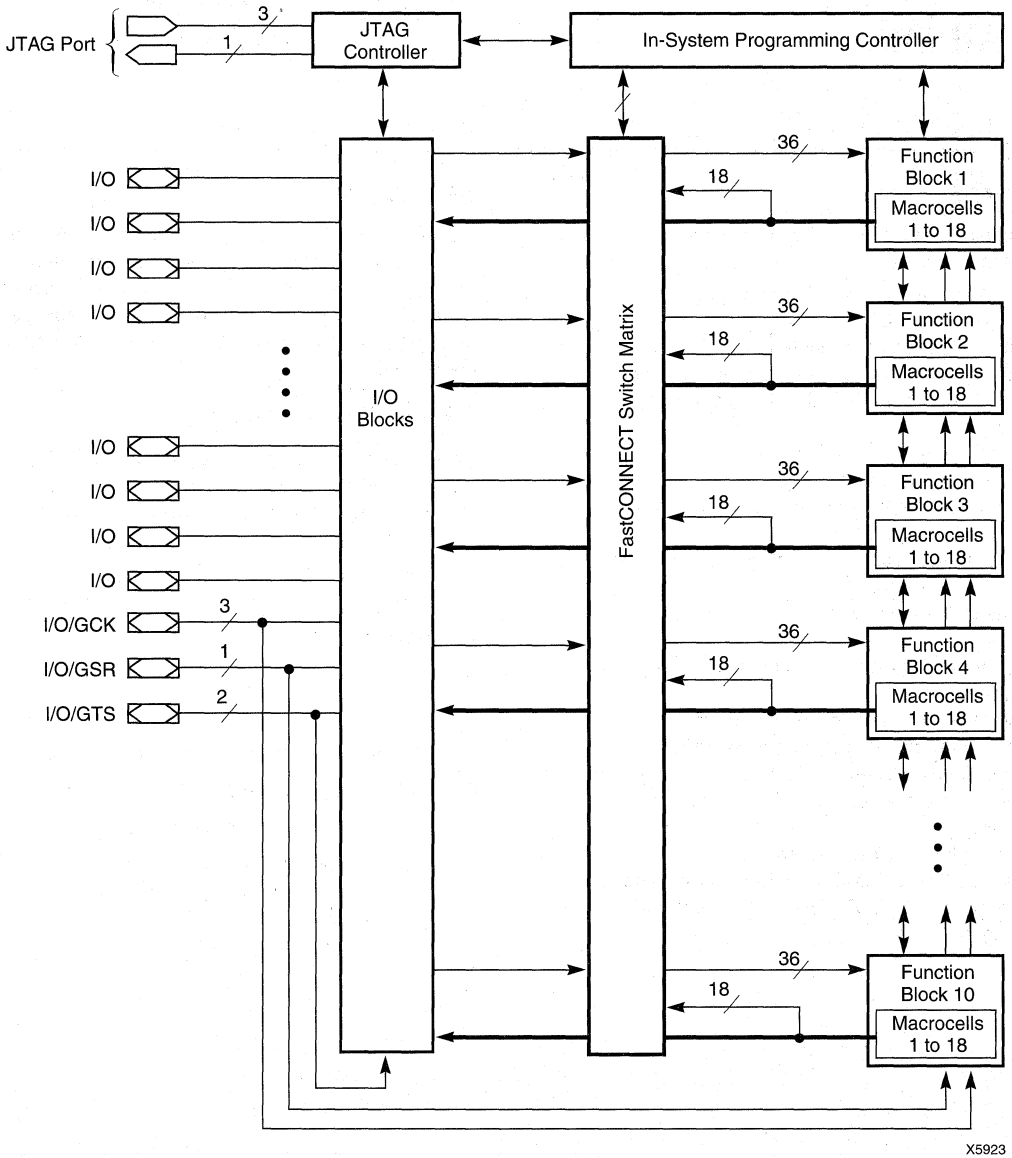


Figure 1: XC95180 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

XC95180 I/O Pins

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
1	1	–	39	537	
1	2	22	30	534	
1	3	23	31	531	
1	4	24	32	528	
1	5	25	33	525	
1	6	26	34	522	
1	7	–	40	519	
1	8	27	35	516	
1	9	28	36	513	
1	10	29	37	510	
1	11	30	38	507	
1	12	32	43	504	
1	13	–	41	501	
1	14	33	44	498	[1]
1	15	34	45	495	
1	16	35	46	492	[1]
1	17	36	47	489	
1	18	–	–	486	
2	1	–	14	483	
2	2	6	7	480	[1]
2	3	7	8	477	
2	4	8	9	474	[1]
2	5	9	10	471	
2	6	11	15	468	
2	7	–	28	465	
2	8	12	16	462	
2	9	13	17	459	
2	10	14	18	456	
2	11	15	19	453	
2	12	16	20	450	
2	13	–	29	447	
2	14	17	21	444	
2	15	18	22	441	
2	16	19	23	438	
2	17	21	25	435	
2	18	–	–	432	
3	1	–	48	429	
3	2	37	49	426	
3	3	38	50	423	
3	4	39	51	420	
3	5	42	55	417	[1]
3	6	43	56	414	
3	7	–	54	411	
3	8	44	57	408	
3	9	45	58	405	
3	10	47	60	402	
3	11	48	61	399	
3	12	49	63	396	
3	13	–	62	393	
3	14	50	64	390	
3	15	52	70	387	
3	16	53	71	384	
3	17	56	74	381	
3	18	–	–	387	
4	1	–	196	375	
4	2	150	194	372	
4	3	151	197	369	
4	4	152	198	366	
4	5	153	199	363	
4	6	154	200	360	
4	7	–	203	357	
4	8	155	201	354	
4	9	156	202	351	
4	10	–	208	348	
4	11	158	205	345	
4	12	159	206	342	[1]
4	13	–	12	339	
4	14	2	3	336	[1]
4	15	3	4	333	
4	16	4	5	330	[1]
4	17	5	6	327	
4	18	–	–	324	

Notes: [1] Global control pin
Macrocell outputs to package pins subject to change, contact factory for latest information. Power, GND, JTAG and Global Signals are fixed.

XC95180 I/O Pins (continued)

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
5	1	–	–	321	
5	2	54	72	318	
5	3	55	73	315	
5	4	57	75	312	
5	5	58	76	309	
5	6	59	77	306	
5	7	–	67	303	
5	8	60	78	300	
5	9	62	82	297	
5	10	–	–	294	
5	11	63	83	291	
5	12	64	84	288	
5	13	–	80	285	
5	14	65	85	282	
5	15	66	86	279	
5	16	67	87	276	
5	17	68	88	273	
5	18	–	–	270	
6	1	–	169	267	
6	2	134	174	264	
6	3	135	175	261	
6	4	138	178	258	
6	5	139	179	255	
6	6	140	180	252	
6	7	–	183	249	
6	8	142	182	246	
6	9	143	185	243	
6	10	–	189	240	
6	11	144	186	237	
6	12	145	187	234	
6	13	–	195	231	
6	14	146	188	228	
6	15	147	191	225	
6	16	148	192	222	
6	17	149	193	219	
6	18	–	–	216	
7	1	–	90	213	
7	2	69	89	210	
7	3	72	95	207	
7	4	74	97	204	
7	5	76	99	201	
7	6	77	100	198	
7	7	–	91	195	
7	8	78	102	192	
7	9	79	103	189	
7	10	–	101	186	
7	11	82	110	183	
7	12	83	111	180	
7	13	–	106	177	
7	14	84	112	174	
7	15	85	113	171	
7	16	86	114	168	
7	17	87	115	165	
7	18	–	–	162	
8	1	–	144	159	
8	2	118	154	156	
8	3	119	155	153	
8	4	122	158	150	
8	5	123	159	147	
8	6	124	160	144	
8	7	–	151	141	
8	8	125	161	138	
8	9	126	162	135	
8	10	–	165	132	
8	11	128	164	129	
8	12	129	166	126	
8	13	–	168	123	
8	14	130	167	120	
8	15	131	170	117	
8	16	132	171	114	
8	17	133	173	111	
8	18	–	–	108	

XC95180 I/O Pins (continued)

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes	Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
9	1	–	–	105		10	1	–	–	51	
9	2	88	116	102		10	2	104	135	48	
9	3	89	117	99		10	3	105	136	45	
9	4	90	118	96		10	4	106	137	42	
9	5	91	121	93		10	5	107	138	39	
9	6	92	122	90		10	6	108	139	36	
9	7	–	107	87		10	7	–	120	33	
9	8	93	123	84		10	8	109	140	30	
9	9	95	125	81		10	9	111	145	27	
9	10	–	109	78		10	10	–	142	24	
9	11	96	126	75		10	11	112	146	21	
9	12	97	127	72		10	12	113	147	18	
9	13	–	119	69		10	13	–	143	15	
9	14	98	128	66		10	14	114	148	12	
9	15	101	131	63		10	15	115	149	9	
9	16	102	133	60		10	16	116	150	6	
9	17	103	134	57		10	17	117	152	3	
9	18	–	–	54		10	18	–	–	0	

XC95180 Global, JTAG and Power Pins

Pin Type	PQ160	HQ208
I/O/GCK1	33	44
I/O/GCK2	35	46
I/O/GCK3	42	55
I/O/GTS1	6	7
I/O/GTS2	8	9
I/O/GTS3	2	3
I/O/GTS4	4	5
I/O/GSR	159	206
TCK	75	98
TDI	71	94
TDO	136	176
TMS	73	96
V_{CCINT} 5 V	10, 46, 94, 157	11, 59, 124, 153, 204
V_{CCIO} 3.3 V/5 V	1, 41, 61, 81, 121, 141	1, 26, 53, 65, 79, 92, 105, 132, 157, 172, 181, 184
GND	20 ,31, 40, 51, 70, 80, 99, 100, 110, 120, 127, 137, 160	2, 13, 24, 27, 42, 52, 66, 68, 69, 81, 93, 104, 108, 129, 130, 141, 156, 163, 177, 190, 207
No Connects	–	–

XC95216 In-System Programmable CPLD

August 1, 1996 (Version 1.1)

Preliminary Product Specification

Features

- 10 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 216 macrocells with 4800 usable gates
- Up to 166 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-10 speed grade)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 160-pin PQFP and 208-pin HQFP packages

Description

The XC95216 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of twelve 36V18 Function Blocks, providing 4,800 usable gates with propagation delays of 10 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95216 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC95216 device.

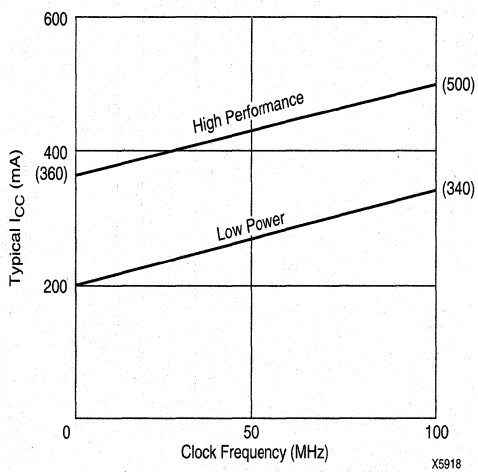


Figure 1: Typical I_{CC} vs. Frequency For XC95216

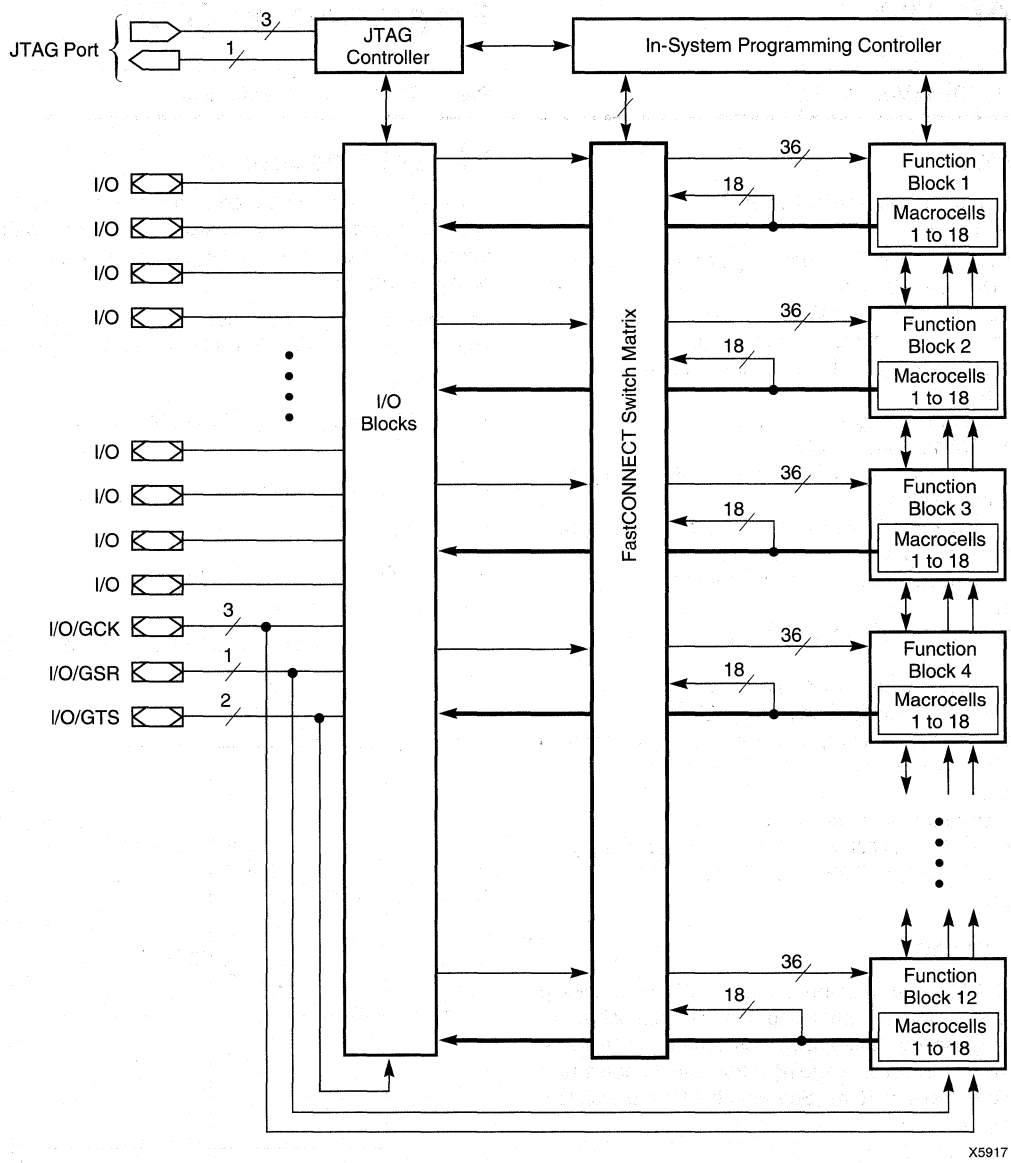


Figure 2: XC95216 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 ns @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions[1]

Symbol	Parameter	Min	Max
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6
V_{IL}	Low-level input voltage	0	0.80
V_{IH}	High-level input voltage	2.0	V_{CCINT} +0.5
V_O	Output voltage	0	V_{CCINT} + 0.5
T_{IN}	Input signal transition time		50

Note: 1. Numbers in parenthesis are for industrial-temperature range versions.

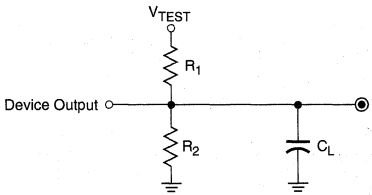
DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5 V operation	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	Output low voltage for 5 V operation	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	200 mA		

AC Characteristics

Symbol	Parameter	XC95216-10		XC95216-15		XC95216-20		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	I/O to output valid		10		15		20	ns
t_{SU}	I/O setup time before GCK	6.5		8.0		10.0		ns
t_{H}	I/O hold time after GCK	0		0		0		ns
t_{CO}	GCK to output valid		6.5		8.0		10.0	ns
f_{CNT}	16-bit counter frequency	111		95.0		83.0		MHz
f_{SYSTEM} [1]	Multiple FB Internal Operating Frequency	67.0		55.0		50.0		MHz
t_{PSU}	I/O setup time before p-term clock input	1.0		2.0		4.0		ns
t_{PH}	I/O hold time after p-term clock input	5.5		6.0		6.0		ns
t_{PCO}	P-term clock to output valid		12.0		14.0		16.0	ns
t_{OE}	GTS to output valid		10.0		15.0		20.0	ns
t_{OD}	GTS to output disable		10.0		15.0		20.0	ns
t_{POE}	Product term OE to output valid		15.5		18.0		22.0	ns
t_{POD}	Product term OE to output disable		15.5		18.0		22.0	ns
t_{PTA}	Product term allocator delay		2.0		2.0		2.0	ns
t_{FBK}	Internal combinatorial feedback delay		12.0		17.0		20.0	ns
t_{WLH}	GCK pulse width (High or Low)	4.5		5.0		6.0		ns
f_{TOG}	Export Control Max. flip-flop toggle rate		111		100		83	MHz
t_{SLEW}	Slew rate time delay		4.5		5.0		5.5	ns
		Preliminary						

Note: 1. f_{SYSTEM} = internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

Figure 3: AC Load Circuit

XC95216 I/O Pins

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
1	1	–	–	645	
1	2	18	22	642	
1	3	19	23	639	
1	4	–	28	636	
1	5	21	25	633	
1	6	22	30	630	
1	7	–	–	627	
1	8	23	31	624	
1	9	24	32	621	
1	10	–	12	618	
1	11	25	33	615	
1	12	26	34	612	
1	13	–	–	609	
1	14	27	35	606	
1	15	28	36	603	
1	16	29	37	600	
1	17	30	38	597	
1	18	–	–	594	
2	1	–	–	591	
2	2	6	7	588	[1]
2	3	7	8	585	
2	4	–	29	582	
2	5	8	9	579	[1]
2	6	9	10	576	
2	7	–	–	573	
2	8	11	15	570	
2	9	12	16	567	
2	10	–	–	564	
2	11	13	17	561	
2	12	14	18	558	
2	13	–	–	555	
2	14	15	19	552	
2	15	16	20	549	
2	16	–	14	546	
2	17	17	21	543	
2	18	–	–	540	

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
3	1	–	–	537	
3	2	32	43	534	
3	3	33	44	531	[1]
3	4	–	39	528	
3	5	34	45	525	
3	6	35	46	522	[1]
3	7	–	–	519	
3	8	36	47	516	
3	9	37	49	513	
3	10	–	67	510	
3	11	38	50	507	
3	12	39	51	504	
3	13	–	–	501	
3	14	42	55	498	[1]
3	15	43	56	495	
3	16	–	80	492	
3	17	44	57	489	
3	18	–	–	486	
4	1	–	–	483	
4	2	152	198	480	
4	3	153	199	477	
4	4	–	196	474	
4	5	154	200	471	
4	6	155	201	468	
4	7	–	–	465	
4	8	156	202	462	
4	9	158	205	459	
4	10	–	–	456	
4	11	159	206	453	[1]
4	12	2	3	450	[1]
4	13	–	–	447	
4	14	3	4	444	
4	15	4	5	441	[1]
4	16	–	203	438	
4	17	5	6	435	
4	18	–	–	432	

XC95216 I/O Pins (continued)

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
5	1	–	–	429	
5	2	45	58	426	
5	3	47	60	423	
5	4	–	41	420	
5	5	48	61	417	
5	6	49	63	414	
5	7	–	–	411	
5	8	50	64	408	
5	9	52	70	405	
5	10	–	109	402	
5	11	53	71	399	
5	12	54	72	396	
5	13	–	–	393	
5	14	55	73	390	
5	15	56	74	387	
5	16	–	40	384	
5	17	57	75	381	
5	18	–	–	378	
6	1	–	–	375	
6	2	140	180	372	
6	3	142	182	369	
6	4	–	208	366	
6	5	143	185	363	
6	6	144	186	360	
6	7	–	–	357	
6	8	145	187	354	
6	9	146	188	351	
6	10	–	183	348	
6	11	147	191	345	
6	12	148	192	342	
6	13	–	–	339	
6	14	149	193	336	
6	15	150	194	333	
6	16	–	169	330	
6	17	151	197	327	
6	18	–	–	324	

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
7	1	–	–	321	
7	2	58	76	318	
7	3	59	77	315	
7	4	–	54	312	
7	5	60	78	309	
7	6	62	82	306	
7	7	–	–	303	
7	8	63	83	300	
7	9	64	84	297	
7	10	–	91	294	
7	11	65	85	291	
7	12	66	86	288	
7	13	–	–	285	
7	14	67	87	282	
7	15	68	88	279	
7	16	–	48	276	
7	17	69	89	273	
7	18	–	–	270	
8	1	–	–	267	
8	2	126	162	264	
8	3	128	164	261	
8	4	–	143	258	
8	5	129	166	255	
8	6	130	167	252	
8	7	–	–	249	
8	8	131	170	246	
8	9	132	171	243	
8	10	–	195	240	
8	11	133	173	237	
8	12	134	174	234	
8	13	–	–	231	
8	14	135	175	228	
8	15	138	178	225	
8	16	–	189	222	
8	17	139	179	219	
8	18	–	–	216	

XC95216 I/O Pins (continued)

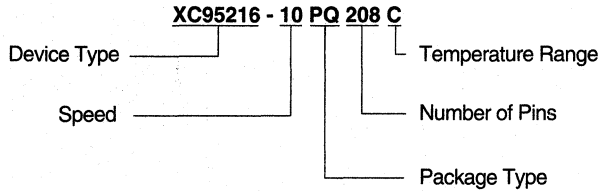
Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
9	1	–	–	213	
9	2	72	95	210	
9	3	74	97	207	
9	4	–	101	204	
9	5	76	99	201	
9	6	77	100	198	
9	7	–	–	195	
9	8	78	102	192	
9	9	79	103	189	
9	10	–	90	186	
9	11	82	110	183	
9	12	83	111	180	
9	13	–	–	177	
9	14	84	112	174	
9	15	85	113	171	
9	16	–	62	168	
9	17	86	114	165	
9	18	–	–	162	
10	1	–	–	159	
10	2	113	147	156	
10	3	114	148	153	
10	4	–	144	150	
10	5	115	149	147	
10	6	116	150	144	
10	7	–	–	141	
10	8	117	152	138	
10	9	118	154	135	
10	10	–	168	132	
10	11	119	155	129	
10	12	122	158	126	
10	13	–	–	123	
10	14	123	159	120	
10	15	124	160	117	
10	16	–	165	114	
10	17	125	161	111	
10	18	–	–	108	

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
11	1	–	–	105	
11	2	87	115	102	
11	3	88	116	99	
11	4	–	119	96	
11	5	89	117	93	
11	6	90	118	90	
11	7	–	–	87	
11	8	91	121	84	
11	9	92	122	81	
11	10	–	107	78	
11	11	93	123	75	
11	12	95	125	72	
11	13	–	–	69	
11	14	96	126	66	
11	15	97	127	63	
11	16	–	120	60	
11	17	98	128	57	
11	18	–	–	54	
12	1	–	–	51	
12	2	101	131	48	
12	3	102	133	45	
12	4	–	106	42	
12	5	103	134	39	
12	6	104	135	36	
12	7	–	–	33	
12	8	105	136	30	
12	9	106	137	27	
12	10	–	151	24	
12	11	107	138	21	
12	12	108	139	18	
12	13	–	–	15	
12	14	109	140	12	
12	15	111	145	9	
12	16	–	142	6	
12	17	112	146	3	
12	18	–	–	0	

XC95216 Global, JTAG and Power Pins

Pin Type	PQ160	HQ208
I/O/GCK1	33	44
I/O/GCK2	35	46
I/O/GCK3	42	55
I/O/GTS1	6	7
I/O/GTS2	8	9
I/O/GTS3	2	3
I/O/GTS4	4	5
I/O/GSR	159	206
TCK	75	98
TDI	71	94
TDO	136	176
TMS	73	96
V_{CCINT} 5 V	10,46,94,157	11, 59, 124, 153, 204
V_{CCIO} 3.3 V/5 V	1,41,61,81,121,141	1, 26, 53, 65, 79, 92, 105, 132, 157, 172, 181, 184
GND	20, 31, 40, 51, 70, 80, 99, 100, 110, 120, 127, 137, 160	2, 13, 24, 27, 42, 52, 66, 68, 69, 81, 93, 104, 108, 129, 130, 141, 156, 163, 177, 190, 207
No Connects	–	–

Ordering Information



Speed Options

-20	20 ns pin-to-pin delay
-15	15 ns pin-to-pin delay
-10	10 ns pin-to-pin delay

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C

Packaging Options

PQ160	160-Pin Plastic Quad Flat Pack (PQFP)
HQ208	208-Pin Power Quad Flat Pack (HQFP)

X5088

Component Availability

Pins		44		84	100		160	208
Type		Plastic PLCC	Plastic VQFP	Plastic PLCC	Plastic PQFP	Plastic TQFP	Plastic PQFP	Power QFP
Code		PC44	VQ44	PC84	PQ100	TQ100	PQ160	HQ208
XC95216	-20						C(I)	C(I)
	-15						C	C
	-10						C	C

X5089

XC95288 In-System Programmable CPLD

June 1, 1996 (Version 1.0)

Advance Product Specification

Features

- 10 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 288 macrocells with 6,400 usable gates
- Up to 292 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-10 speed grade)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in a 208-pin and 304-pin HQFP packages

Description

The XC95288 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of sixteen 36V18 Function Blocks, providing 6,400 usable gates with propagation delays of 10 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95288 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

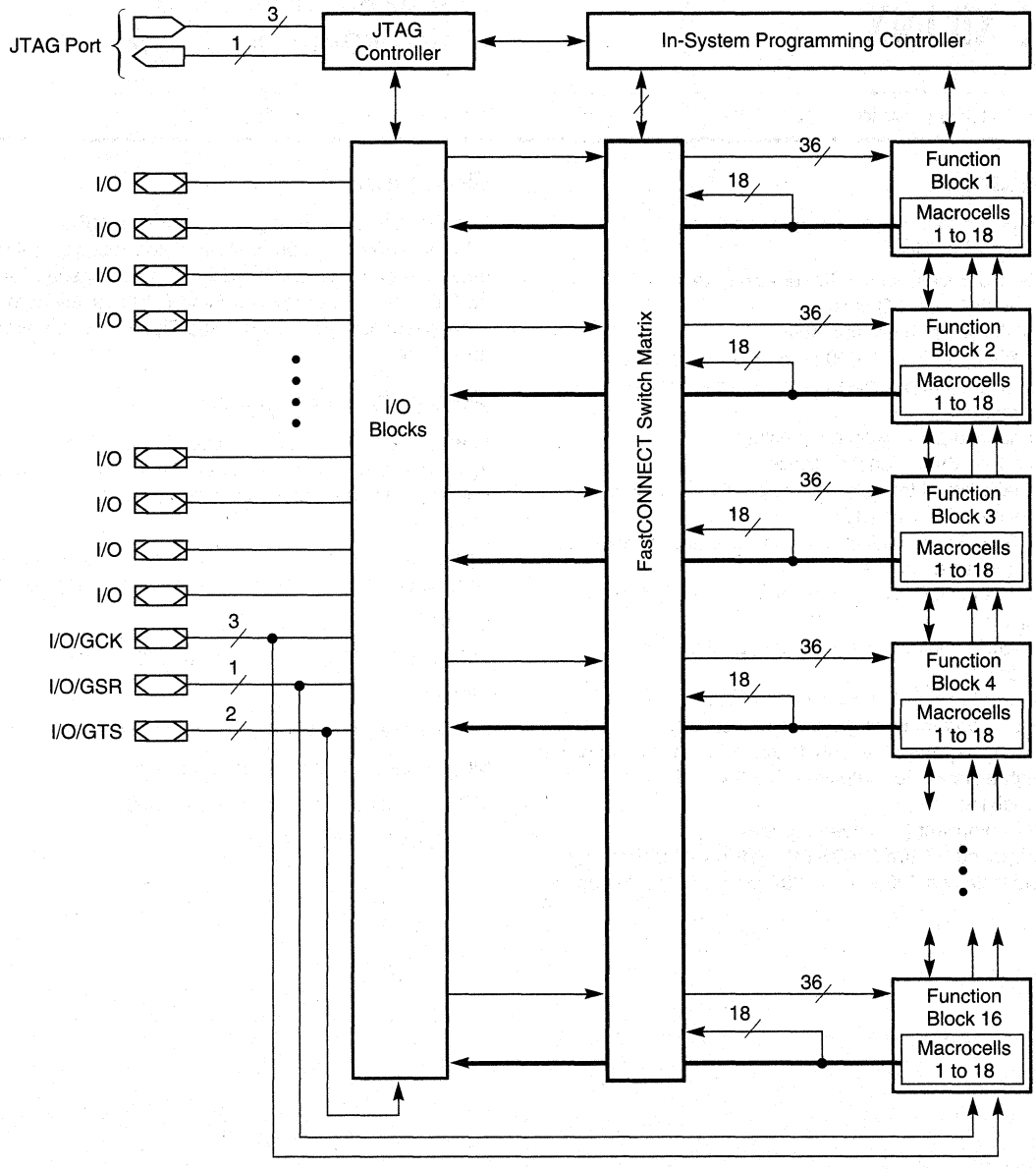


Figure 1: XC95288 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

XC95288 I/O Pins

Function Block	Macrocell	HQ208	BScan Order	Notes
1	1	–	861	
1	2	28	858	
1	3	29	855	
1	4	–	852	
1	5	30	849	
1	6	31	846	
1	7	–	843	
1	8	32	840	
1	9	–	837	
1	10	33	834	
1	11	–	831	
1	12	34	828	
1	13	–	825	
1	14	35	822	
1	15	36	819	
1	16	–	816	
1	17	37	813	
1	18	–	810	
2	1	–	807	
2	2	15	804	
2	3	16	801	
2	4	–	798	
2	5	17	795	
2	6	18	792	
2	7	–	789	
2	8	19	786	
2	9	–	783	
2	10	20	780	
2	11	–	777	
2	12	21	774	
2	13	–	771	
2	14	22	768	
2	15	23	765	
2	16	–	762	
2	17	25	759	
2	18	–	756	

Function Block	Macrocell	HQ208	BScan Order	Notes
3	1	–	753	
3	2	38	750	
3	3	39	747	
3	4	–	744	
3	5	40	741	
3	6	41	738	
3	7	–	735	
3	8	43	732	
3	9	–	729	
3	10	44	726	[1]
3	11	–	723	
3	12	45	720	
3	13	–	717	
3	14	46	714	[1]
3	15	47	711	
3	16	–	708	
3	17	48	705	
3	18	–	702	
4	1	–	699	
4	2	3	696	[1]
4	3	4	693	
4	4	–	690	
4	5	5	687	[1]
4	6	6	684	
4	7	–	681	
4	8	7	678	[1]
4	9	–	675	
4	10	8	672	
4	11	–	669	
4	12	9	666	[1]
4	13	–	663	
4	14	10	660	
4	15	12	657	
4	16	–	654	
4	17	14	651	
4	18	–	648	

Notes: [1] Global control pin
Macrocell outputs to package pins subject to change, contact factory for latest information. Power, GND, JTAG and Global Signals are fixed.
Consult factory for HQ304 pinouts.

XC95288 I/O Pins (continued)

Function Block	Macrocell	HQ208	BScan Order	Notes
5	1	–	645	
5	2	49	642	
5	3	50	639	
5	4	–	636	
5	5	51	633	
5	6	54	630	
5	7	–	627	
5	8	55	624	[1]
5	9	–	621	
5	10	56	618	
5	11	–	615	
5	12	57	612	
5	13	–	609	
5	14	58	606	
5	15	60	603	
5	16	–	600	
5	17	61	597	
5	18	–	594	
6	1	–	591	
6	2	197	588	
6	3	198	585	
6	4	–	582	
6	5	199	579	
6	6	200	576	
6	7	–	573	
6	8	201	570	
6	9	–	567	
6	10	202	564	
6	11	–	561	
6	12	203	558	
6	13	–	555	
6	14	205	552	
6	15	206	549	[1]
6	16	–	546	
6	17	208	543	
6	18	–	540	

Function Block	Macrocell	HQ208	BScan Order	Notes
7	1	–	537	
7	2	62	534	
7	3	63	531	
7	4	–	528	
7	5	64	525	
7	6	66	522	
7	7	–	519	
7	8	67	516	
7	9	–	513	
7	10	69	510	
7	11	–	507	
7	12	70	504	
7	13	–	501	
7	14	71	498	
7	15	72	495	
7	16	–	492	
7	17	73	489	
7	18	–	486	
8	1	–	483	
8	2	186	480	
8	3	187	477	
8	4	–	474	
8	5	188	471	
8	6	189	468	
8	7	–	465	
8	8	191	462	
8	9	–	459	
8	10	192	456	
8	11	–	453	
8	12	193	450	
8	13	–	447	
8	14	194	444	
8	15	195	441	
8	16	–	438	
8	17	196	435	
8	18	–	432	

Note: [1] Global control pin

XC95288 I/O Pins (continued)

Function Block	Macrocell	HQ208	BScan Order	Notes
9	1	–	429	
9	2	74	426	
9	3	75	423	
9	4	–	420	
9	5	76	417	
9	6	77	414	
9	7	–	411	
9	8	78	408	
9	9	–	405	
9	10	80	402	
9	11	82	399	
9	12	83	396	
9	13	–	393	
9	14	84	390	
9	15	85	387	
9	16	–	384	
9	17	86	381	
9	18	–	378	
10	1	–	375	
10	2	170	372	
10	3	171	369	
10	4	–	366	
10	5	173	363	
10	6	174	360	
10	7	–	357	
10	8	175	354	
10	9	–	351	
10	10	178	348	
10	11	179	345	
10	12	180	342	
10	13	–	339	
10	14	182	336	
10	15	183	333	
10	16	–	330	
10	17	185	327	
10	18	–	324	

Function Block	Macrocell	HQ208	BScan Order	Notes
11	1	–	321	
11	2	87	318	
11	3	88	315	
11	4	–	312	
11	5	89	309	
11	6	90	306	
11	7	–	303	
11	8	91	300	
11	9	–	297	
11	10	95	294	
11	11	97	291	
11	12	99	288	
11	13	–	285	
11	14	100	282	
11	15	101	279	
11	16	–	276	
11	17	102	273	
11	18	–	270	
12	1	–	267	
12	2	158	264	
12	3	159	261	
12	4	–	258	
12	5	160	255	
12	6	161	252	
12	7	–	249	
12	8	162	246	
12	9	–	243	
12	10	164	240	
12	11	165	237	
12	12	166	234	
12	13	–	231	
12	14	167	228	
12	15	168	225	
12	16	–	222	
12	17	169	219	
12	18	–	216	

XC95288 I/O Pins (continued)

Function Block	Macrocell	HQ208	BScan Order	Notes
13	1	–	213	
13	2	103	210	
13	3	106	207	
13	4	–	204	
13	5	107	201	
13	6	109	198	
13	7	–	195	
13	8	110	192	
13	9	–	189	
13	10	111	186	
13	11	112	183	
13	12	113	180	
13	13	–	177	
13	14	114	174	
13	15	115	171	
13	16	–	168	
13	17	116	165	
13	18	–	162	
14	1	–	159	
14	2	144	156	
14	3	145	153	
14	4	–	150	
14	5	146	147	
14	6	147	144	
14	7	–	141	
14	8	148	138	
14	9	–	135	
14	10	149	132	
14	11	150	129	
14	12	151	126	
14	13	–	123	
14	14	152	120	
14	15	154	117	
14	16	–	114	
14	17	155	111	
14	18	–	108	

Function Block	Macrocell	HQ208	BScan Order	Notes
15	1	–	105	
15	2	117	102	
15	3	118	99	
15	4	–	96	
15	5	119	93	
15	6	120	90	
15	7	–	87	
15	8	121	84	
15	9	–	81	
15	10	122	78	
15	11	123	75	
15	12	125	72	
15	13	–	69	
15	14	126	66	
15	15	127	63	
15	16	–	60	
15	17	128	57	
15	18	–	54	
16	1	–	51	
16	2	131	48	
16	3	133	45	
16	4	–	42	
16	5	134	39	
16	6	135	36	
16	7	–	33	
16	8	136	30	
16	9	–	27	
16	10	137	24	
16	11	138	21	
16	12	139	18	
16	13	–	15	
16	14	140	12	
16	15	142	9	
16	16	–	6	
16	17	143	3	
16	18	–	0	

XC95288 Global, JTAG and Power Pins

Pin Type	HQ208
I/O/GCK1	44
I/O/GCK2	46
I/O/GCK3	55
I/O/GTS1	7
I/O/GTS2	9
I/O/GTS3	3
I/O/GTS4	5
I/O/GSR	206
TCK	98
TDI	94
TDO	176
TMS	96
V_{CCINT} 5 V	11,59,124,153,204
V_{CCIO} 3.3 V/5 V	1,26,53,65,79,92,105, 132,157,172,181,184
GND	2,13,24,27,42,52,68,81, 93,104,108,129,130, 141,156,163,177, 190,207
No Connects	–

XC95432 In-System Programmable CPLD

June 1, 1996 (Version 1.0)

Advance Product Specification

Features

- 10 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 432 macrocells with 9,600 usable gates
- Up to 232 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in a 304-pin HQFP package

Description

The XC95432 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of twenty-four 36V18 Function Blocks, providing 9,600 usable gates with propagation delays of 10 ns.

XC95576 In-System Programmable CPLD

June 1, 1996 (Version 1.0)

Advance Product Specification

Features

- 12 ns pin-to-pin logic delays on all pins
- f_{CNT} to 100 MHz
- 576 macrocells with 12,800 usable gates
- Up to 232 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in a 304-pin HQFP package

Description

The XC95576 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of thirty-two 36V18 Function Blocks, providing 12,800 usable gates with propagation delays of 12 ns.

XC7300 CMOS CPLD Family

XC7318 18-Macrocell CMOS CPLD

XC7336/XC7336Q 36-Macrocell CMOS CPLD

XC7354 54-Macrocell CMOS CPLD

XC7372 72-Macrocell CMOS CPLD

XC73108 108-Macrocell CMOS CPLD

XC73144 144-Macrocell CMOS CPLD

XC7300 Characterization Data

XC7300 CMOS CPLD Family

June 1, 1996 (Version 1.0) Product Specification

Features

- High-performance Complex Programmable Logic Devices (CPLDs)
  - 5 / 7.5 ns pin-to-pin speeds on all fast inputs
  - Up to 167 MHz maximum clock frequency
- 100% PCI compliant
- High-drive 24 mA output
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 43 to 61 MHz 18-bit accumulators
- Multiple independent clocks
- Each input programmable as direct, latched, or registered
- Power management options
- Multiple security bits for design protection
- Supported by industry standard design and verification tools
- Advanced Dual-Block architecture
  - Fast Function Blocks
  - High-Density Function Blocks (XC7354, XC7372, XC73108, XC73144)
- 0.8 µ CMOS EPROM technology

Description

The XC7300 family employs a unique Dual-Block architecture that provides high speed operations via Fast Function Blocks and/or high density capability via High Density Function Blocks.

Fast Function Blocks (FFBs) provide fast, pin-to-pin speed and logic throughput for critical decoding and ultra-fast state machine applications. High-Density Function Blocks (FBs) provide maximum logic density and system-level features to implement complex functions with predictable timing for adders and accumulators, wide functions and state machines requiring large numbers of product terms, and other forms of complex logic. See Figure 1.

In addition, the XC7300 architecture employs the Universal Interconnect Matrix (UIM) which guarantees 100% interconnect of all internal functions. This interconnect scheme provides constant, short interconnect delays for all routing paths through the UIM. Constant interconnect delays simplify device timing and guarantee design performance, regardless of logic placement within the chip.

The UIM provides an intrinsic wire-AND capability called SMARTswitch. Transferring functions into the UIM conserves macrocell logic. This increases the total logic capacity of the device. The wire-AND capability also significantly increases the signal fan-in of each function block. All Xilinx-supported CPLD design tools automatically implement SMARTswitch.

The XC7300 Family

	XC7318	XC7336	XC7354	XC7372	XC73108	XC73144
Typical 22V10 Equivalent	1.5 – 2	3 – 4	6	8	12	16
Number of Macrocells	18	36	54	72	108	144
Number of Function Blocks	2	4	6	8	12	16
Number of Flip-Flops	18	36	108	126	198	276
Number of Fast Inputs	12	12	12	12	12	12
Number of Signal Pins	38	38	58	84	120	156

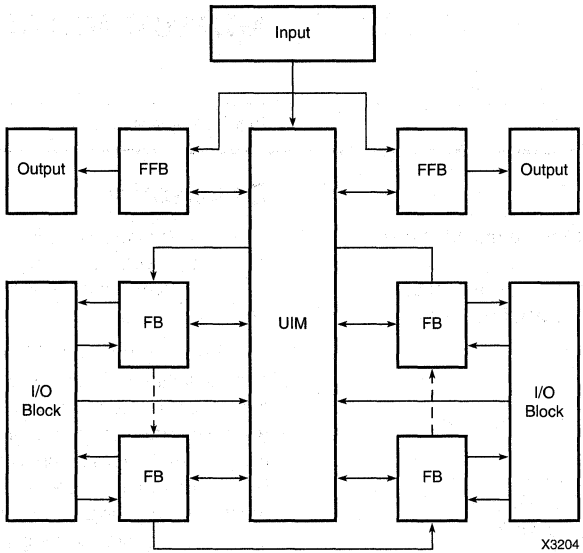


Figure 1: XC7300 Device Block Diagram

All XC7300 Dual-Block CPLDs include programmable power management features to specify high-performance or low-power operation on an individual macrocell-by-macrocell basis. Unused macrocells are automatically turned off to minimize power dissipation. Designers can operate speed-critical paths at maximum performance, while non-critical paths dissipate less power.

Fast Function Blocks

The FFB has 24 inputs that can be individually selected from the UIM, 12 fast input pins, or the nine macrocell feedbacks from the FFB. The programmable AND array in each FFB generates 45 product terms to drive the nine macrocells in each FFB. Each macrocell can be configured for registered or combinatorial logic. See Figure 2.

Five product terms from the programmable AND array are allocated to each macrocell. Four of these product terms are ORed together and may be optionally inverted before driving the input of a programmable D-type flip-flop. The fifth product term drives the asynchronous active-High programmable Reset or Set Input to the macrocell flip-flop. The flip-flop can be configured as a D-type or Toggle flip-flop, or transparent for combinatorial outputs.

Two FFB macrocell differences exist between the XC7318/XC7336/XC73144 and the XC7354/XC7372/XC73108.

In the XC7318, XC7336 and XC73144, five product terms from the programmable AND array are allocated to each macrocell. Four of these product terms are OR'd together and may be optionally inverted before driving the input of a programmable D-type flip-flop. The fifth product term drives the asynchronous active High programmable Set or Reset input to the macrocell flip-flop. The flip-flop can be configured as a D-type or Toggle flip-flop, or transparent for combinatorial outputs. See Figure 2.

In the XC7354, XC7372 and XC73108, five product terms from the programmable AND array are allocated to each macrocell. Four of these product terms are OR'd together, inverted and drive the input of a programmable D-type flip-flop. The fifth product term drives the asynchronous active High programmable Set input to the macrocell flip-flop. The flip-flop can be configured as a D-type flip-flop or transparent for combinatorial outputs. See Figure 3.

The programmable clock source is one of two global Fast-Clock signals (FCLK0 or FCLK1) that are distributed with short delay and minimal skew over the entire chip.

The FFB macrocells drive chip outputs directly through 3-state output buffers. Each output buffer can be individually controlled by one of two dedicated Fast Output Enable inputs or permanently enabled or disabled. The macrocell output can also be routed back as an input to the FFB and the UIM.

Each FFB output is capable of sinking 24 mA when V_{CCIO} = 5 volts. These include all outputs on the XC7318 and XC7336 devices and all Fast Outputs (FOs) on the XC7354, XC7372, XC73108, and XC73144 devices.

Unlike other I/Os, the FFB inputs do not have an input register.

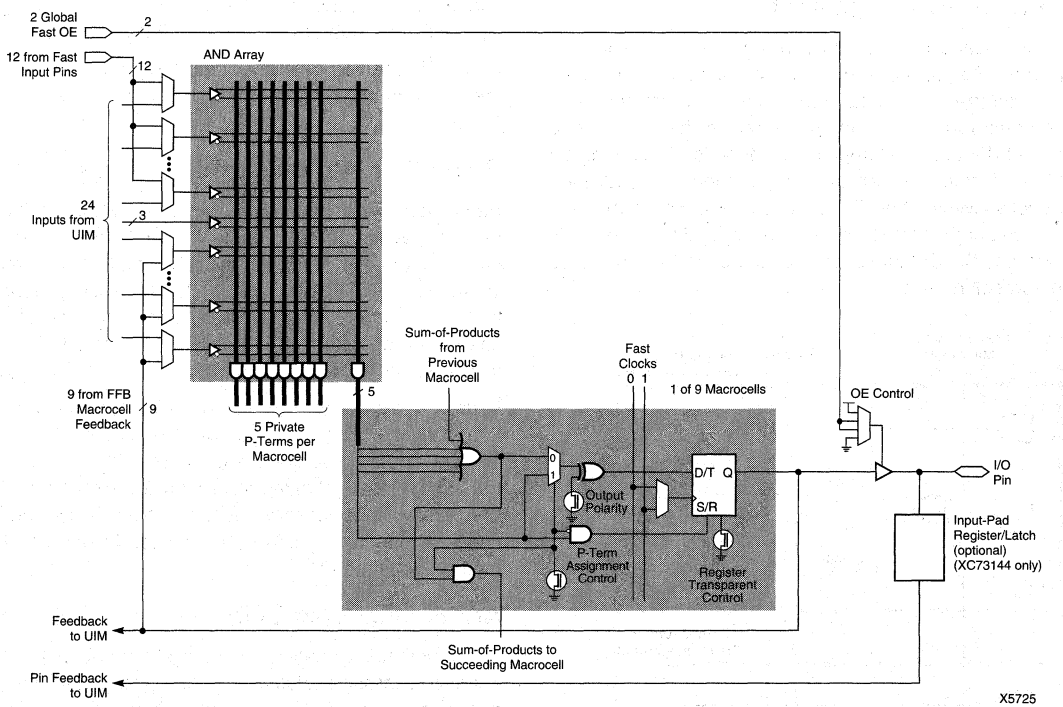


Figure 2: Fast Function Block and Macrocell Schematic for the XC7318, XC7336, and XC73144

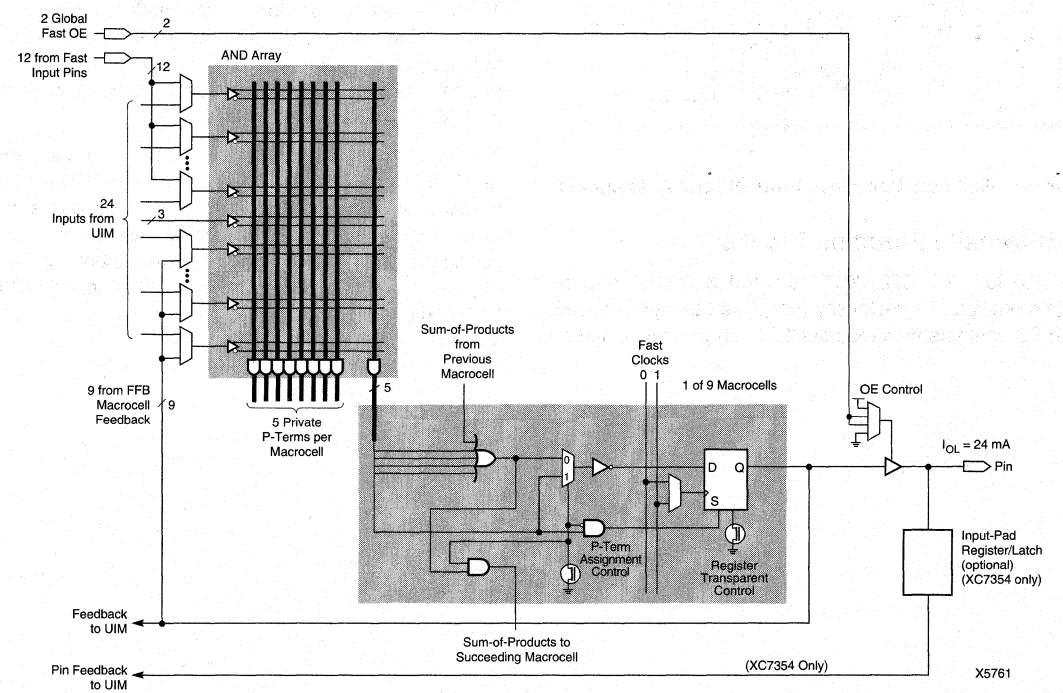


Figure 3: Fast Function Block and Macrocell Schematic for the XC7354, XC7372, and XC73108

Product Term Assignment

Each macrocell sum-of-product OR gates can be expanded using the FFB product term assignment scheme. Product term assignment transfers product terms in increments of four product terms from one macrocell to the neighboring macrocell (Figure 4). Complex logic functions requiring up to 36 product terms can be implemented using all nine macrocells within the FFB. When product terms are assigned to adjacent macrocells, the product term normally dedicated to the Set or Reset function becomes the input to the macrocell register.

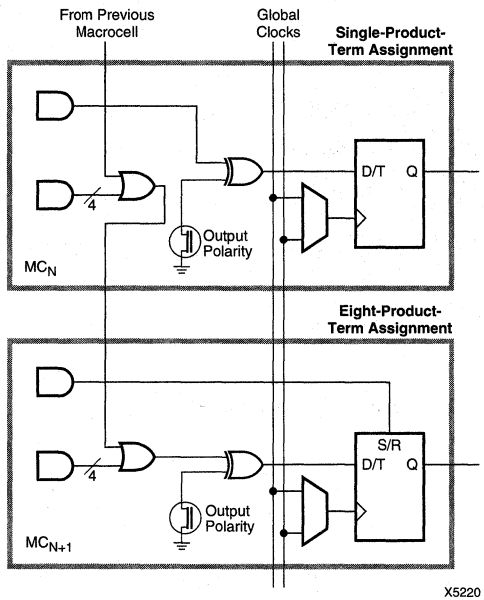


Figure 4: Fast Function Block Product Term Assignment

High-Density Function Blocks

The XC7354, XC7372, XC73108 and XC73144 devices contain multiple, High-Density FBs linked though the UIM. Each FB contains nine macrocells. Each macrocell can be configured for either registered or combinatorial logic. A detailed block diagram of the FB is shown in Figure 5.

Each FB receives 21 signals and their complements from the UIM and an additional three inputs from the Fast Input (FI) pins.

Shared and Private Product Terms

Each macrocell contains five private product terms that can be used as the primary inputs for combinatorial functions implemented in the Arithmetic Logic Unit (ALU), or as individual Reset, Set, Output-Enable, and Clock logic functions for the flip-flop. Each FB also provides an additional 12 shared product terms, which are uncommitted product terms available for any of the nine macrocells within the FB.

Four private product terms can be ORed together with up to four shared product terms to drive the D1 input to the ALU. The D2 input is driven by the OR of the fifth private product term and up to eight of the remaining shared product terms. The shared product terms add no logic delay, and each shared product term can be connected to one or all nine macrocells in the FB.

Arithmetic Logic Unit

The functional versatility of each macrocell in the FB is enhanced through additional gating and control functions available in the ALU. A detailed block diagram of the XC7300 ALU is shown in Figure 6.

The ALU has two programmable modes; *logic* and *arithmetic*. In logic mode, the ALU functions as a 2-input function generator using a 4-bit look-up table that can be programmed to generate any Boolean function of its D1 and D2 inputs as illustrated in Table 1.

The function generator can OR its inputs, widening the OR function to a maximum of 17 inputs. It can AND them, which means that one sum-of-products can be used to mask the other. It can also XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted, and either or both can be ignored.

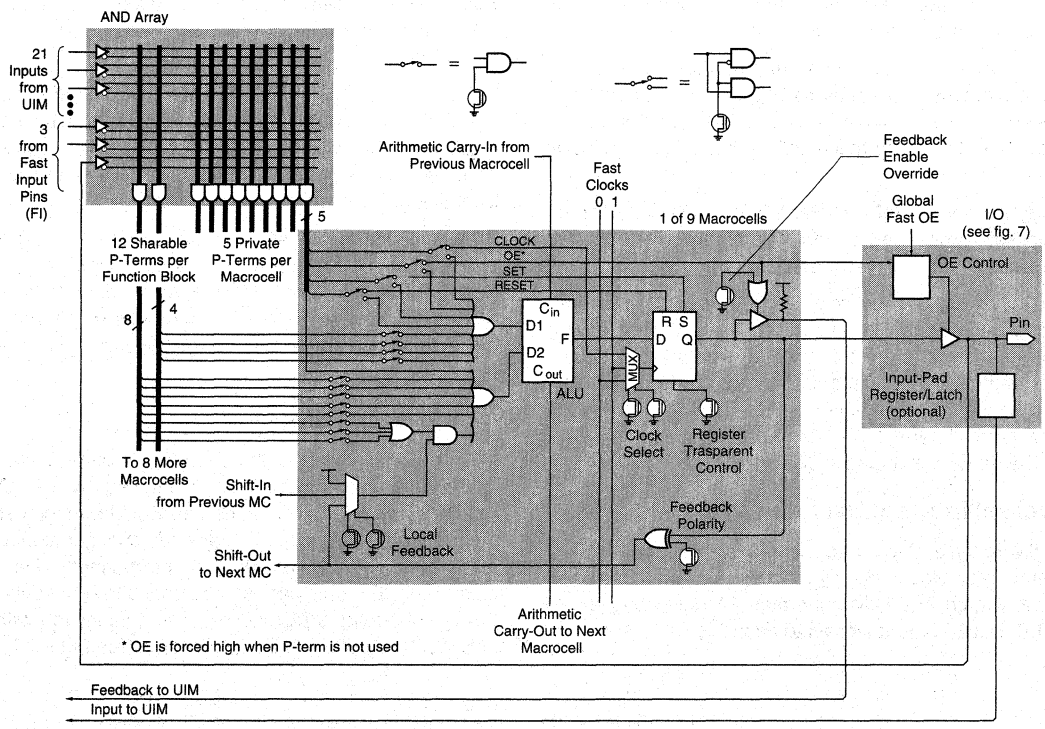


Figure 5: High-Density Function Block and Macrocell Schematic

Table 1: Function Generator Logic Operations

Function	
D1:+: D2	$\overline{D1}$:+: $\overline{D2}$
D1 * D2	$\overline{D1}$ * $\overline{D2}$
D1 + D2	$\overline{D1}$ + $\overline{D2}$
D1	D2
D1	D2
D1 * $\overline{D2}$	$\overline{D1}$ * D2
D1 + $\overline{D2}$	$\overline{D1}$ + D2

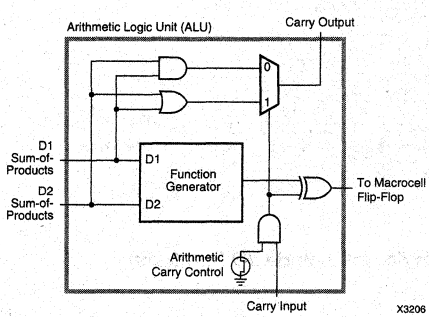


Figure 6: ALU Schematic

Therefore, the ALU can implement one additional layer of logic without any speed penalty.

In arithmetic mode, the ALU block can be programmed to generate the arithmetic sum or difference of the D1 and D2 inputs. Combined with the carry input from the next lower macrocell, the ALU operates as a 1-bit full adder generating a carry output to the next higher macrocell. The carry chain propagates between adjacent macrocells and also crosses the boundaries between FBs. This dedicated carry chain overcomes the inherent speed and density problems of the traditional CPLD architecture when trying to perform arithmetic functions.

Carry Lookahead

Each FB provides a carry lookahead generator capable of anticipating the carry across all nine macrocells. The carry lookahead generator reduces the ripple-carry delay of wide arithmetic functions such as add, subtract, and magnitude compare to that of the first nine bits, plus the carry lookahead delay of the higher-order FBs.

Macrocell Flip-Flop

The ALU block output drives the input of a programmable D-type flip-flop. The flip-flop is triggered by the rising edge of the clock input, but it can be configured as transparent,

making the Q output identical to the D input, independent of the clock, or as a conventional flip-flop.

The macrocell clock source is programmable and can be one of the private product terms or one of two global FastCLK signals (FCLK0 and FCLK1). Global FastCLK signals are distributed to every macrocell flip-flop with short delay and minimal skew.

The asynchronous Set and Reset product terms override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set.

In addition to driving the chip output buffer, the macrocell output is routed back as an input to the UIM. One private product term can be configured to control the Output Enable of the output buffer and/or the feedback to the UIM. If it is configured to control UIM feedback, the Output Enable product term forces the UIM feedback line High when the macrocell output is disabled.

Universal Interconnect Matrix

The UIM receives inputs from each macrocell output, I/O pin, and dedicated input pin. Acting as fully connected crossbar switch, the UIM generates 21 output signals to each FB and 24 output signals to each FFB.

Each UIM input can be connected to any UIM output. The UIM delay is constant, regardless of the routing distance, fan-out, or fan-in.

When multiple UIM inputs are connected to the same output, their wire-AND is formed by using internally available inversions. This AND logic can also be used to implement wide NAND, OR or NOR functions. This offers an additional level of logic without any speed penalty.

A macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Programming several such macrocell outputs onto the same UIM output emulates a 3-state bus line. If one of the macrocell outputs is enabled, the UIM output assumes the enabled output's level.

Input/Output Blocks

Macrocells drive chip outputs directly through 3-state output buffers, each individually controlled by the Output Enable product term mentioned above. The macrocell output can be inverted. An additional configuration option allows the output to be disabled permanently. Two dedicated FastOE inputs can also be configured to control any of the chip outputs instead of, or in conjunction with, the individual Output Enable product term. See Figure 7.

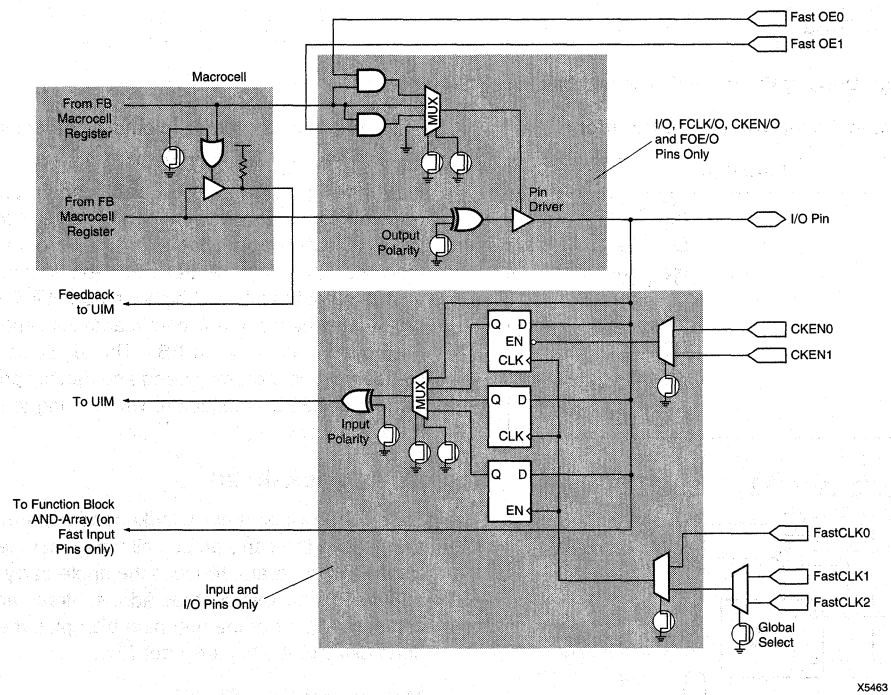


Figure 7: Input/Output Schematic (except XC7318/XC7336 which do not include I/O flip-flops)

Output buffers, except those connected to FFBs, can sink 12 mA when V_{CCIO} = 5 V. FFB outputs can sink 24 mA when V_{CCIO} = 5 V.

Each signal input to the chip is connected to a programmable input structure that can be configured as direct, latched, or registered. The latch and flip-flop can use one of two FastCLK signals as latch enable or clock. The two FastCLK signals are FCLK0 and a global choice of either FCLK1 or FCLK2. Latches are transparent when FastCLK is High, and flip-flops clock on the rising edge of FastCLK. The flip-flop includes an active-low clock enable, which when High, holds the present state of the flip-flop and inhibits response to the input signal. The clock enable source is one of two global Clock Enable signals ($\overline{CE0}$ and $\overline{CE1}$). An additional configuration option is polarity inversion for each input signal.

3.3 V or 5 V Interface Configuration

XC7300 devices can be used in systems with two different supply voltages: 3.3 V and 5 V. Each XC7300 device has separate V_{CC} connections to the internal logic and input buffers (V_{CCINT}) and to the I/O drivers (V_{CCIO}). V_{CCINT} must always be connected to a nominal 5 V supply, while V_{CCIO} may be connected to either 3.3 V or 5 V, depending on the output interface requirement.

When V_{CCIO} is connected to 5 V, the input thresholds are TTL levels, compatible with 3.3 V and 5 V logic. The output High levels are also TTL compatible. When V_{CCIO} is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V rail. This makes the XC7300 family ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed so the I/O can also safely interface to a mixed 3.3 V and 5 V bus.

Power-On Characteristics/Master Reset

Each XC7300 device undergoes a short internal initialization sequence upon device powerup. During this time (t_{RESET}), the outputs remain 3-stated while the device is configured from its internal EPROM array and all registers are initialized. If the $\overline{MR}$ pin is tied to V_{CCINT}, the initialization sequence is completely transparent to the user and is completed in t_{RESET} after V_{CCINT} has reached 4.75 V. If $\overline{MR}$ is held low while the device is powering up, the internal initialization sequence begins and outputs will remain 3-stated until the sequence is complete and $\overline{MR}$ is brought High. V_{CC} rise must be monotonic to ensure the initialization sequence is performed correctly.

For additional flexibility, the $\overline{MR}$ pin is provided so the device can be reinitialized after power is applied. On the falling edge of $\overline{MR}$, all outputs become 3-stated and the initialization sequence begins. The outputs remain 3-stated until the internal initialization sequence is complete and $\overline{MR}$ is brought High. The minimum $\overline{MR}$ pulse with is t_{WMR}. If $\overline{MR}$ is brought high after t_{WMR}, but before t_{RESET}, the outputs will become active after t_{RESET}. It is essential that the $\overline{MR}$ pin remain static during power on reset (t_{RESET}).

During the initialization sequence, all input registers or latches are preloaded High and all FB and FFB macrocell registers are preloaded to a known state. For FFB macrocell registers where the Set/Reset product term is defined, the preload is accomplished by asserting the product term shortly before the end of the initialization sequence. When the Set/Reset product term is configured as Reset, the register preload value is Low. When the Set/Reset product term is configured as Set, the register preload value is High. For FFB macrocell registers where the Set/Reset product term is not used, the register preload value is High.

For FB macrocell registers, the preload value is defined by a separate preload configuration bit, independent of the Set and Reset product terms. The value of this preload configuration bit may be determined by the user. If unspecified, the register preload value is Low.

Power Management

The XC7300 family features a power-management scheme permitting non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a small portion is speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To further reduce power dissipation, unused FBs are turned off and unused macrocells in used FBs are configured for low power operation.

Erasure Characteristics

In windowed packages, the EPROM array can be erased by exposure to UV light with wavelengths of approximately 4000 Å. The recommended erasure time is approximately 1 hr. when the device is placed within 1 in. of an UV lamp with 12,000 $\mu W/cm^2$ power rating. To prevent unintentional exposure, place opaque labels over the device window.

When the device is exposed to high intensity UV light for much longer periods, permanent damage can occur. The maximum integrated dose the XC7300 CPLDs can be exposed to without damage is 7000 W • s/cm^2, or approximately one week at 12,000 $\mu W/cm^2$.

Design Recommendations

For proper operation, all unused input and I/O pins must be connected to a valid logic level (High or Low). The recommended decoupling for all V_{CC} pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.

Use electrostatic discharge (ESD) handling procedures with the XC7300 CPLDs to prevent damage to the device during programming, assembly, and test.

Design Security

Each member of the XC7300 family has a multibit security system that controls access to the configuration programmed into the device. This security scheme uses multiple EPROM bits at various locations within the EPROM array to offer a higher degree of design security than other EPROM and fused-based devices. Programmed data within EPROM cells is invisible–even when examined under a microscope–and cannot be selectively erased. The EPROM security bits, and the device configuration data, reset when the device is erased.

High-Volume Production Programming

The XC7300 family is available as a factory programmed product. For factory programming procedures, contact your local Xilinx representative.

XACT*step* Development System

The XC7300 CPLD family is fully supported by the Xilinx XACT*step* development system. The designer can create the design using ABEL, schematics, equations, VHDL or other HDL languages in a variety of software front-end tools. The XACT*step* development system can be used to implement the design and generate a bitmap which can be used to program the XC7300 devices.

Timing Model

Timing within the XC7300 family is accurately determined using external timing parameters from the device data sheet, a variety of CAE simulators, or with the timing model shown in Figure 8.

The timing model is based on the fixed internal delays of the XC7300 architecture which consists of four basic parts: I/O Blocks, the UIM, FFBs and FBs. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can calculate the timing information for a particular device.

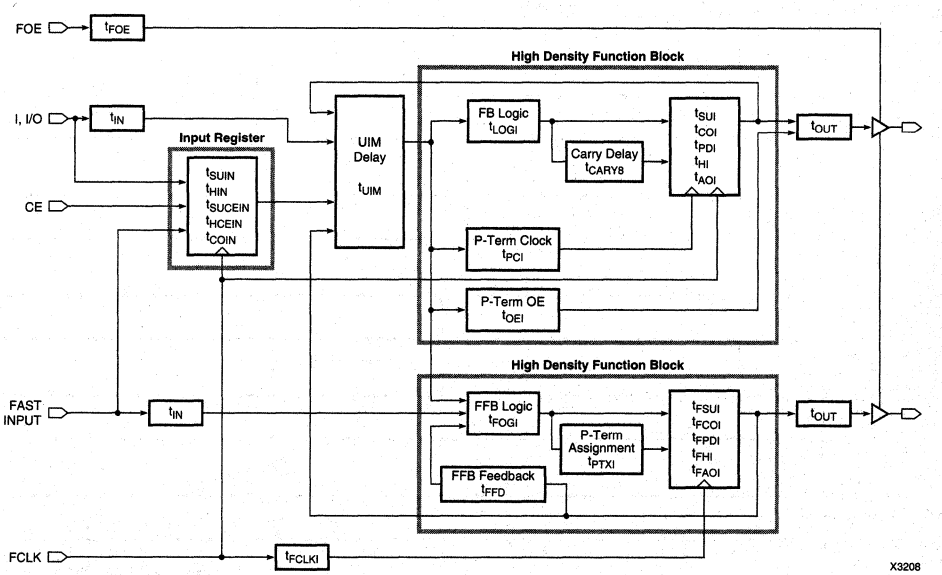
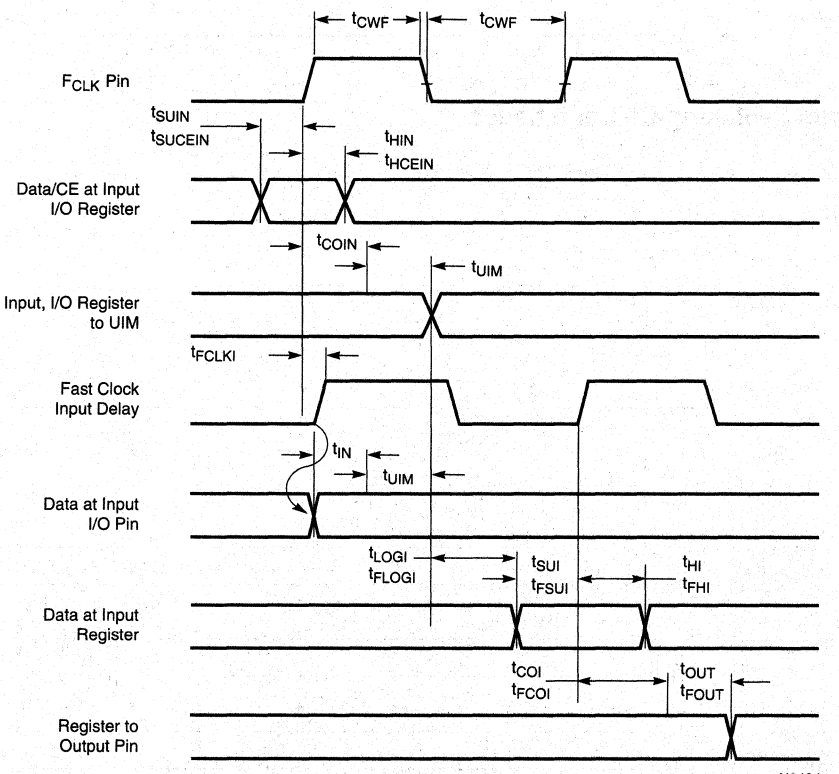
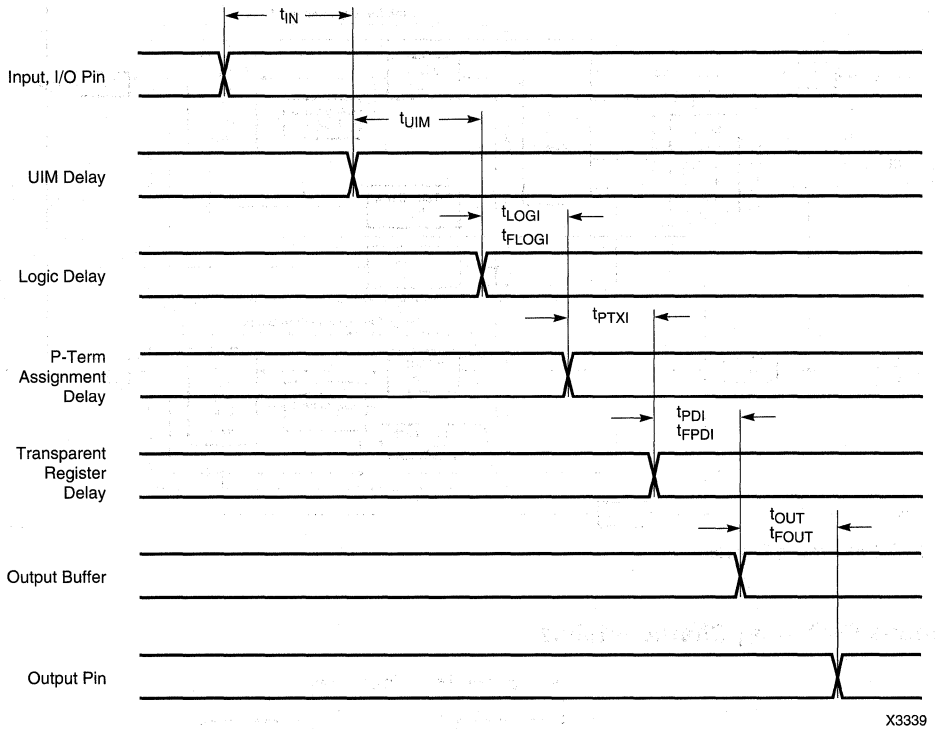


Figure 8: XC7300 Timing Model

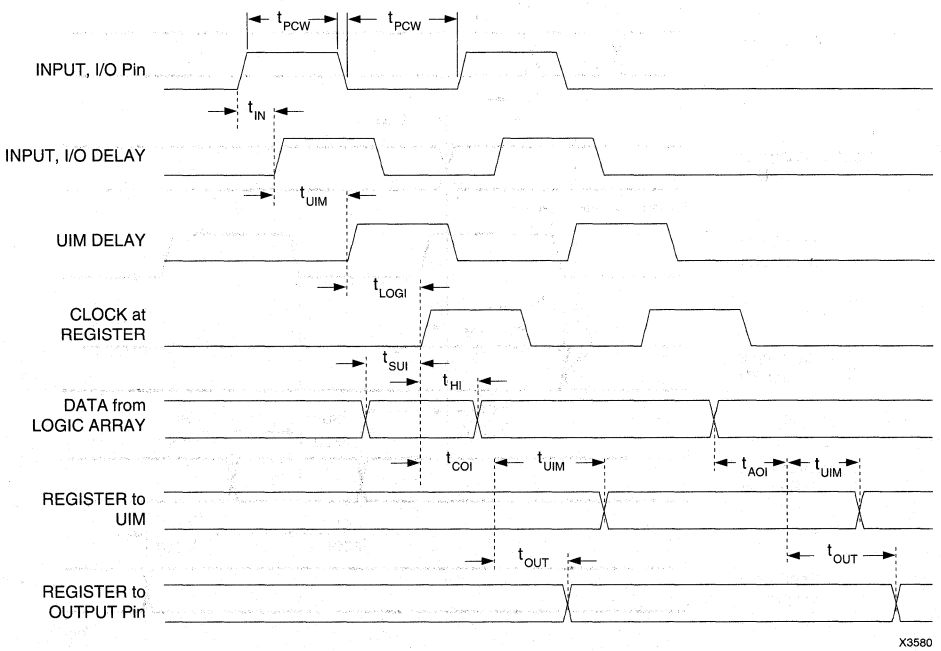
Synchronous Switching Characteristics



Combinational Switching Characteristics



Asynchronous Switching Characteristics



XC7318
18-Macrocell CMOS CPLD

June 1, 1996 (Version 1.0)

Product Specification

Features

- Ultra high-performance Complex Programmable Logic Devices (CPLDs)
  - 5 ns pin-to-pin speeds on all fast inputs
  - Up to 167 MHz maximum clock frequency
- 100% PCI compliant
- High-drive 24 mA output
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- Multiple security bits for design protection
- Incorporates two PAL-like 24V9 Fast Function Blocks
- 0.8 µ CMOS EPROM technology
- Available in 44-pin PQFP and PLCC packages

General Description

The XC7318 is a high performance CPLD providing general purpose logic integration. It consists of two PAL-like 24V9 Fast Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™). See Figure 1 for the architecture overview.

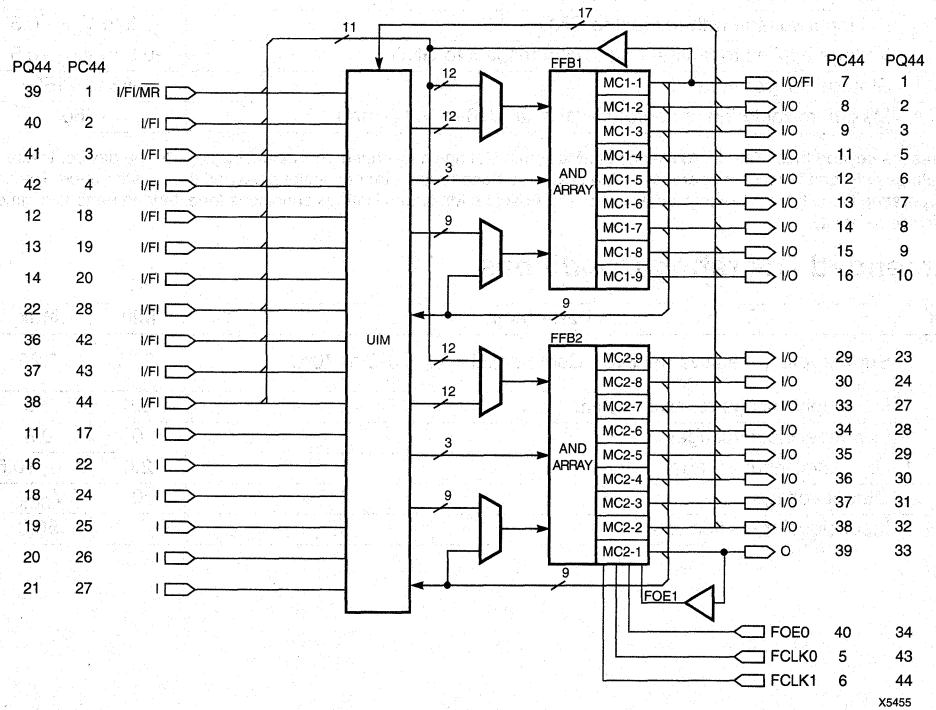


Figure 1: XC7318 Architecture

Power Estimation

Figure 2 shows a typical power estimation for the XC7318 device, programmed as a 16-bit counter and operating at the indicated clock frequency.

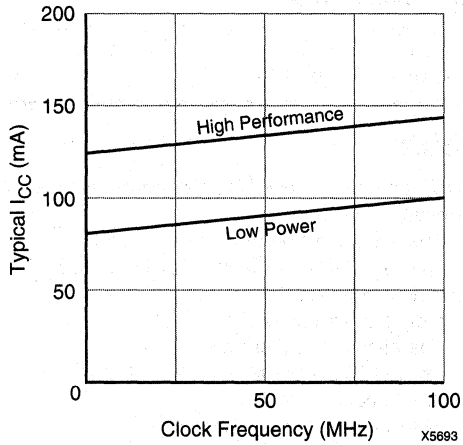


Figure 2: Typical I_{CC} vs. Frequency for XC7318

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT} V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
V_{CCIO}	I/O supply voltage relative to GND	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V
T_{IN}	Input signal transition time		50.0	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 24 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		6.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{OUT}[1]	Output capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}[2]	Supply current	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5V f = 1.0 MHz @ 25°C	90 Typ		mA

Notes: 1. Sample tested.
2. Measured with device programmed as a 16-bit counter.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

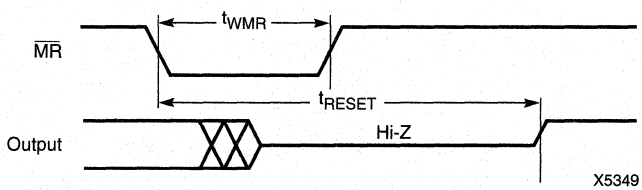


Figure 3: Global Reset Waveform

Fast Function Block (FFB) External AC Characteristics [1]

Symbol	Parameter	XC7318-5		XC7318-7		Units
		Min	Max	Min	Max	
t_{PD}	Fast input to output valid [2]		5.0		7.5	ns
	I/O or input to output valid [2]		8.5		12.0	ns
t_{SU}	Fast input setup time before FCLK	4.5		5.0		ns
	I/O or input setup time before FCLK	7.0		8.5		ns
t_H	Fast, I/O or input hold time after FCLK	0		0		ns
t_{CO}	FCLK input to output valid		4.5		4.5	ns
t_{FOE}	FOE input to output valid		7.0		7.5	ns
t_{FOD}	FOE input to output disable		7.0		7.5	ns
f_{MAX}	Max count frequency [2, 3]	167.0		125.0		MHz
t_{WLH}	Fast Clock pulse width (High or Low)	3.0		4.0		ns

Notes: 1. All appropriate ac specifications tested using Figure 5 as test load circuit.
2. Assumes four product terms per output.
3. Export Control Max. flip-flop toggle rate.

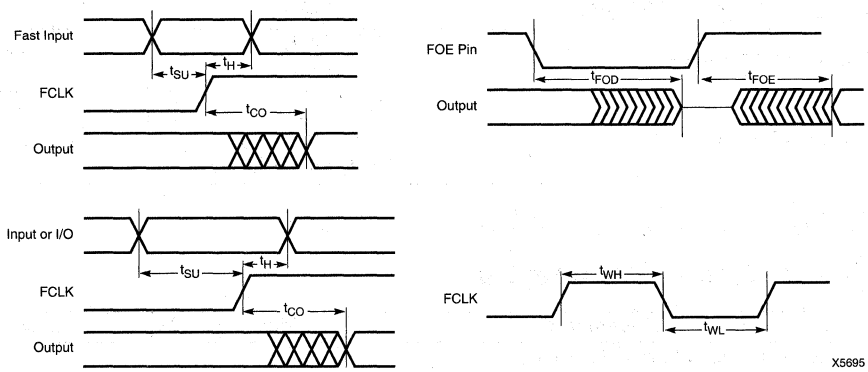
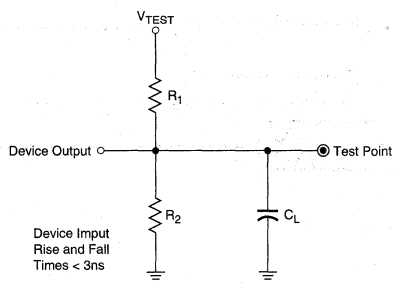


Figure 4: Switching Waveform



V_{CCIO} Level	V_{TEST}	R_1	R_1	C_L
5 V	5.0 V	160 Ω	120 Ω	35 pF
3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5222

Figure 5: AC Load Circuit

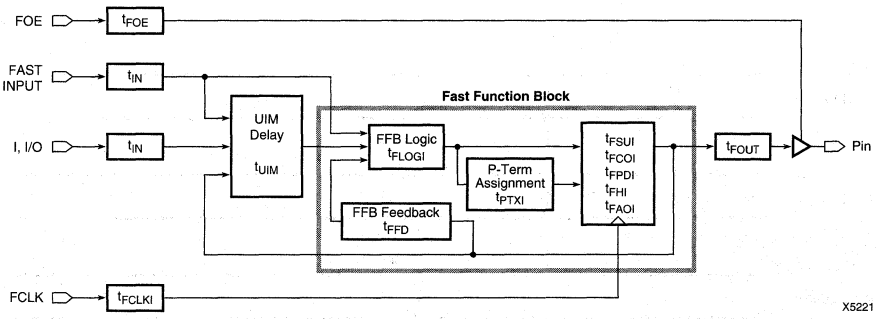


Figure 6: XC7318 Timing Model

Timing Model

Timing within the XC7318 is accurately determined using external timing parameters from the device data sheet, using a variety of CAE simulators, or with the timing model shown in Figure 6.

The timing model is based on the fixed internal delays of the XC7318 architecture that consists of three basic parts: I/O Blocks, the UIM and Fast Function Blocks. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can easily calculate the timing information for the XC7318.

Fast Function Block (FFB) Internal AC Characteristics

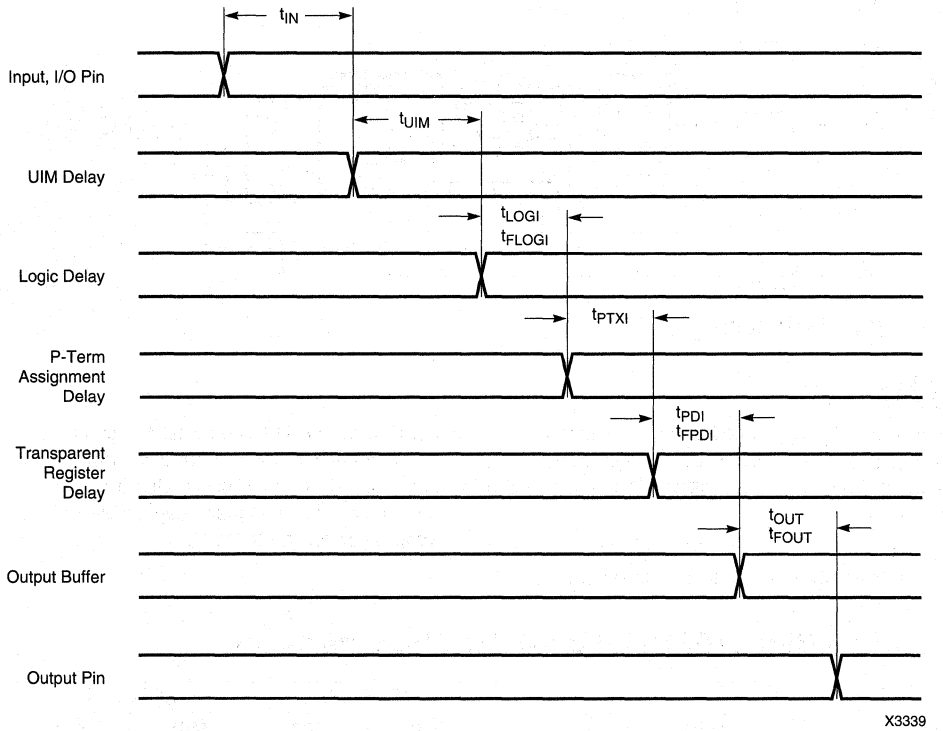
Symbol	Parameter	XC7318-5		XC7318-7		Units
		Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [1]		1.0		1.5	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [1]		2.0		3.5	ns
t_{FSUI}	FFB register setup time	2.5		1.5		ns
t_{FHI}	FFB register hold time	1.0		2.5		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5	ns
t_{FAOI}	FFB register async. set delay		2.0		2.0	ns
t_{PTXI}	FFB p-term assignment delay		0.6		0.8	ns
t_{FFD}	FFB feedback delay		0.5		4.0	ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

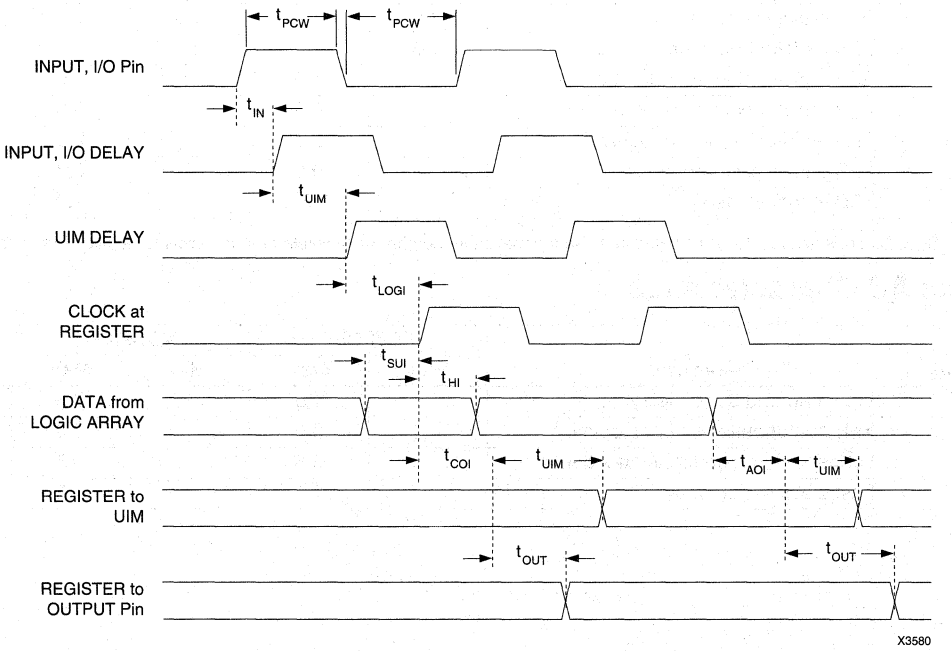
Internal AC Characteristics

Symbol	Parameter	XC7318-5		XC7318-7		Units
		Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		1.5		2.5	ns
t_{FOUT}	FFB output buffer and pad delay		2.0		3.0	ns
t_{UIM}	Universal Interconnect Matrix delay		3.5		4.5	ns
t_{FCLKI}	Fast clock buffer delay		1.5		1.5	ns

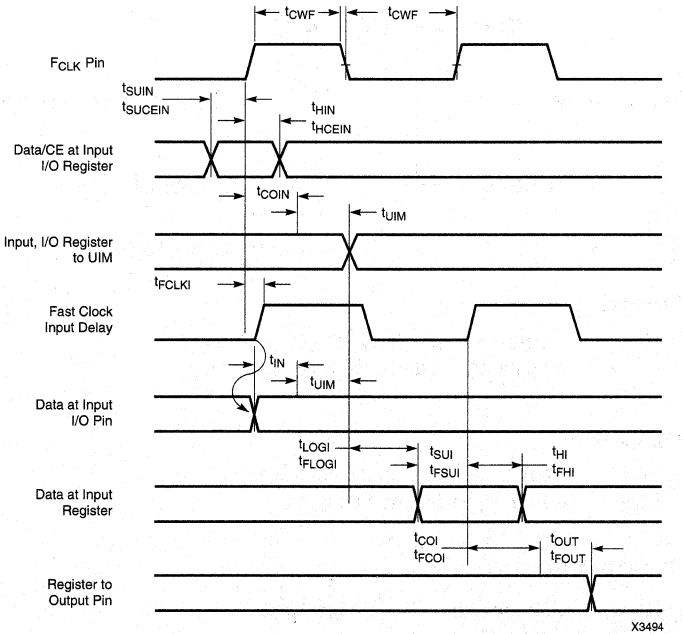
Combinational Switching Characteristics



Asynchronous Switching Characteristics



Synchronous Switching Characteristics

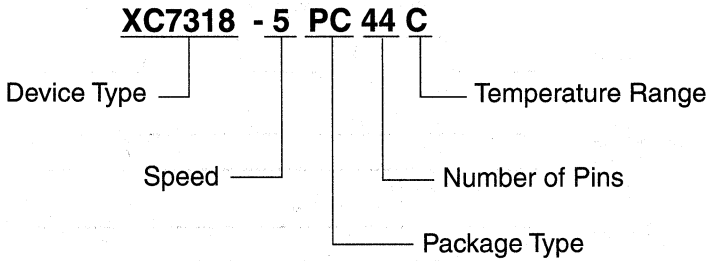


XC7318 Pinouts

PQ44	PC44	Input	XC7318	Output
39	1	I/FI	$\overline{MR}$	
40	2	I/FI		
41	3	I/FI		
42	4	I/FI		
43	5	FCLK0		
44	6	FCLK1		
1	7	I/FO/FI		MC1-1
2	8	I/FO		MC1-2
3	9	I/FO		MC1-3
4	10		**GND**	
5	11	I/FO		MC1-4
6	12	I/FO		MC1-5
7	13	I/FO		MC1-6
8	14	I/FO		MC1-7
9	15	I/FO		MC1-8
10	16	I/FO		MC1-9
11	17	I		
12	18	I/FI		
13	19	I/FI		
14	20	I/FI		
15	21		V_{CCINT}	
16	22	I		

PQ44	PC44	Input	XC7318	Output
17	23		**GND**	
18	24	I		
19	25	I		
20	26	I		
21	27	I		
22	28	I/FI		
23	29	I/FO		MC2-9
24	30	I/FO		MC2-8
25	31		**GND**	
26	32		V_{CCIO}	
27	33	I/FO		MC2-7
28	34	I/FO		MC2-6
29	35	I/FO		MC2-5
30	36	I/FO		MC2-4
31	37	I/FO		MC2-3
32	38	I/FO		MC2-2
33	39	FOE1/FO		MC2-1
34	40	FOE0		
35	41		V_{CCINT}/V_{PP}	
36	42	I/FI		
37	43	I/FI		
38	44	I/FI		

Ordering Information



Speed Options

-7	7.5 ns pin-to-pin delay (commercial only)
-5	5 ns pin-to-pin delay (commercial only)

Packaging Options

PC44	44-Pin Plastic Leaded Chip Carrier
PQ44	44-Pin Plastic Quad Flat Pack

Temperature Options

C	Commercial	0^{o}C to 70^{o}C

Component Availability

Pins		44	
Type		Plastic PLCC	Plastic PQFP
Code		PC44	PQ44
XC7318	–7	C	C
	–5	C	C

C = Commercial = 0° to +70°C

XC7336/XC7336Q
36-Macrocell CMOS CPLD

June 1, 1996 (Version 1.0) | Product Specification

Features

- Ultra high-performance Complex Programmable Logic Devices (CPLDs)
  - 5 ns pin-to-pin speeds on all fast inputs
  - Up to 167 MHz maximum clock frequency
- New low power XC7336Q
- 100% PCI compliant
- High-drive 24 mA output
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- Multiple security bits for design protection
- Incorporates four PAL-like 24V9 Fast Function Blocks
- 0.8 µ CMOS EPROM technology
- Available in 44-pin VQFP, PQFP and PLCC/CLCC packages

General Description

The XC7336 is a high performance CPLD providing general purpose logic integration. It consists of four PAL-like 24V9 Fast Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™). See Figure 1 for the architecture overview.

The XC7336 is designed in 0.8 µ CMOS EPROM technology, in speed grades ranging from 5 to 15 ns. The XC7336Q is also available now, providing lower power consumption in -10, -12 and -15 ns speed grades.

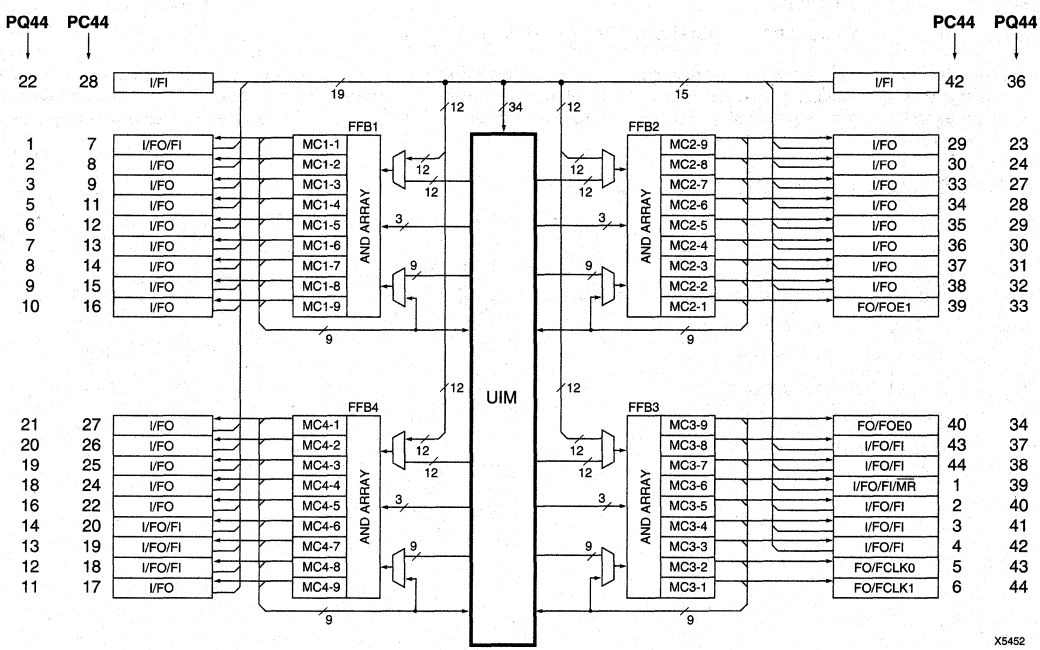


Figure 1: XC7336 Architecture

Power Estimation

Figure 2 shows a typical power estimation for the XC7336 and the XC7336Q device, programmed as two 16-bit counters and operating at the indicated clock frequency.

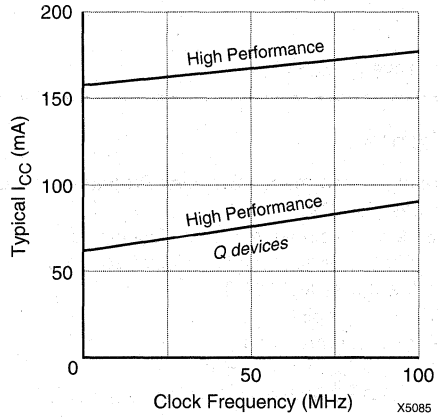


Figure 2: Typical I_{CC} vs. Frequency for XC7336

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+250	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
V_{CCIO}	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.50	5.50	V
V_{CCIO}	I/O supply voltage relative to GND	3.0	3.60	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V
T_{IN}	Input signal transition time		50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter		Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage		I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage		I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage		I_{OL} = 24 mA V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage		I_{OL} = 24 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current		V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current		V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins		V_{IN} = GND f = 1.0 MHz		6.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FOE0, FOE1)		V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for Fast Inputs		V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT}[1]	Output capacitance		V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}[2]	Supply current	(Non Q)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5V f = 1.0 MHz @ 25°C	126 Typ		mA
		(Q)		55 Typ		

Notes: 1. Sample tested.
2. Measured with device programmed as two 16-bit counters.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

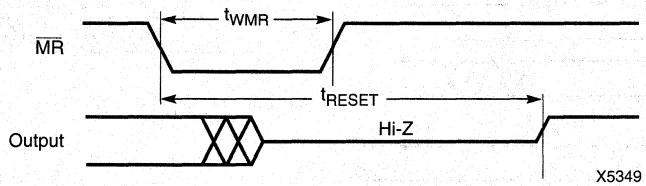


Figure 3: Global Reset Waveform

Fast Function Block (FFB) External AC Characteristics [1]

Symbol	Parameter	XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Fast input to output valid [2]		5.0		7.5		10.0		12.0		15.0	ns
	I/O or input to output valid [2]		8.5		12.0		15.0		19.0		23.0	ns
t_{SU}	Fast input setup time before FCLK	4.5		5.0		5.0		6.0		7.0		ns
	I/O or input setup time before FCLK	7.0		8.5		10.0		13.0		15.0		ns
t_H	Fast, I/O or input hold time after FCLK	0		0		0		0		0		ns
t_{CO}	FCLK input to output valid		4.5		4.5		8.0		9.0		12.0	ns
t_{FOE}	FOE input to output valid		7.0		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.0		7.5		10.0		12.0		15.0	ns
f_{MAX}	Max count frequency [2, 3]	167.0		125.0		100.0		80.0		66.7		MHz
t_{WLH}	Fast Clock pulse width (High or Low)	3.0		4.0		5.0		5.5		6.0		ns

Symbol	Parameter	XC7336Q-10		XC7336Q-12		XC7336Q-15		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Fast input to output valid [2]		10.0		12.0		15.0	ns
	I/O or input to output valid [2]		15.0		19.0		23.0	ns
t_{SU}	Fast input setup time before FCLK	6.5		6.5		7.0		ns
	I/O or input setup time before FCLK	11.5		13.5		15.0		ns
t_H	Fast, I/O or input hold time after FCLK	0		0		0		ns
t_{CO}	FCLK input to output valid		6.5		8.5		12.0	ns
t_{FOE}	FOE input to output valid		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		10.0		12.0		15.0	ns
f_{MAX}	Max count frequency [2, 3]	100.0		80.0		66.7		MHz
t_{WLH}	Fast Clock pulse width (High or Low)	5.0		5.5		6.0		ns

Notes: 1. All appropriate ac specifications tested using Figure 5 as test load circuit.
2. Assumes four product terms per output.
3. Export Control Max. flip-flop toggle rate.

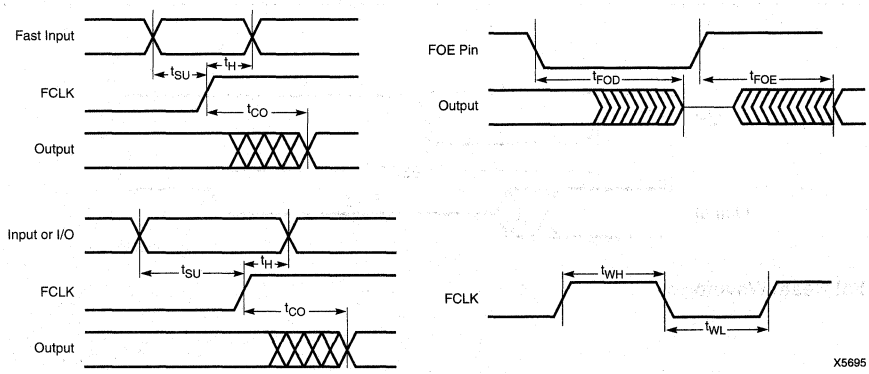
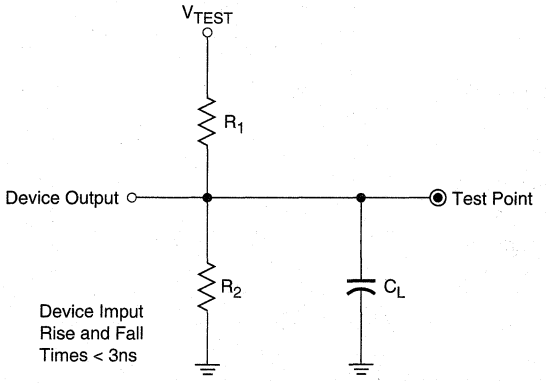


Figure 4: Switching Waveform



V_{CCIO} Level	V_{TEST}	R_1	R_1	C_L
5 V	5.0 V	160 Ω	120 Ω	35 pF
3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5222

Figure 5: AC Load Circuit

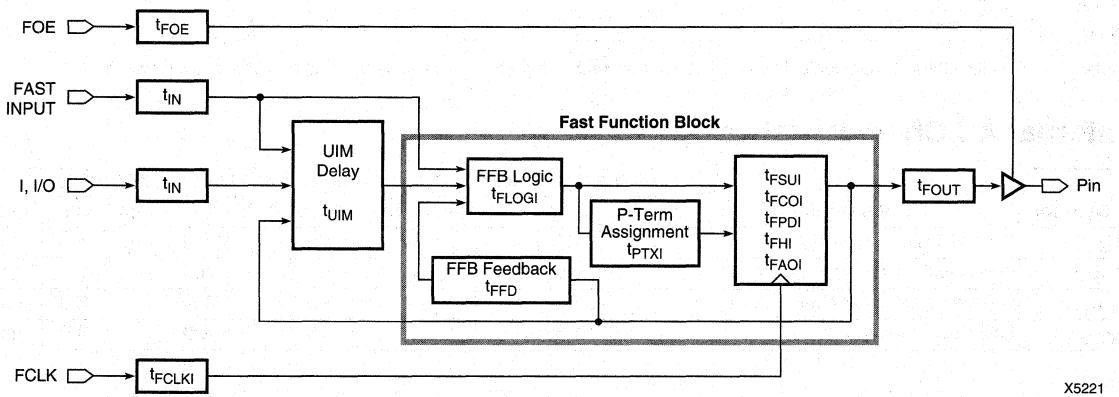


Figure 6: XC7336 Timing Model

Timing Model

Timing within the XC7336 is accurately determined using external timing parameters from the device data sheet, using a variety of CAE simulators, or with the timing model shown in Figure 6.

The timing model is based on the fixed internal delays of the XC7336 architecture that consists of three basic parts: I/O Blocks, the UIM and Fast Function Blocks. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can easily calculate the timing information for the XC7336.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [1]		1.0		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [1]		2.0		3.5		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	2.5		1.5		2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	1.0		2.5		2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.0		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		0.6		0.8		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		0.5		4.0		5.0		6.5		8.0	ns

Symbol	Parameter	XC7336Q-10		XC7336Q-12		XC7336Q-15		Units
		Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [1]		3.0		3.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [1]		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		5.0		6.5		8.0	ns

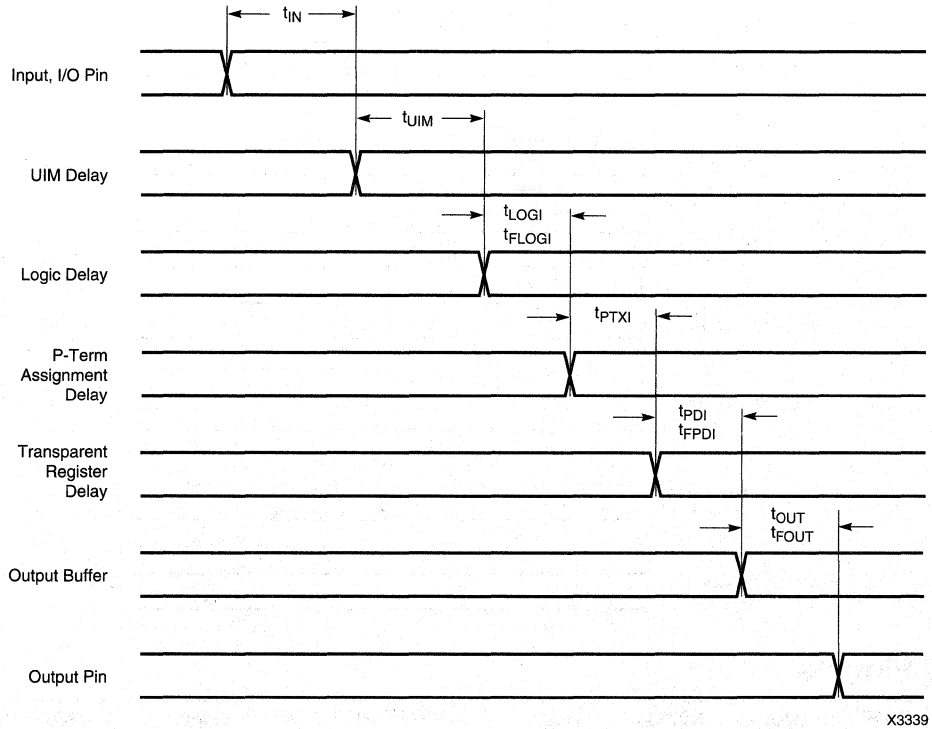
Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Internal AC Characteristics

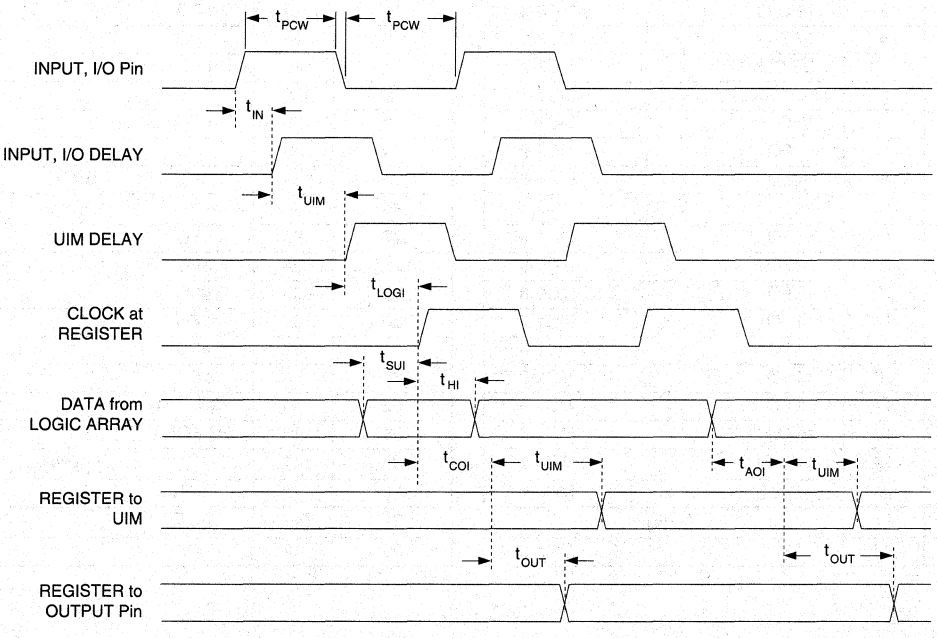
Symbol	Parameter	XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		1.5		2.5		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		2.0		3.0		4.5		5.0		7.0	ns
t_{UIM}	Universal Interconnect Matrix delay		3.5		4.5		5.0		7.0		8.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		1.5		2.5		3.0		4.0	ns

Symbol	Parameter	XC7336Q-10		XC7336Q-12		XC7336Q-15		Units
		Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		7.0	ns
t_{UIM}	Universal Interconnect Matrix delay		5.0		7.0		8.0	ns
t_{FCLKI}	Fast clock buffer delay		2.5		3.0		4.0	ns

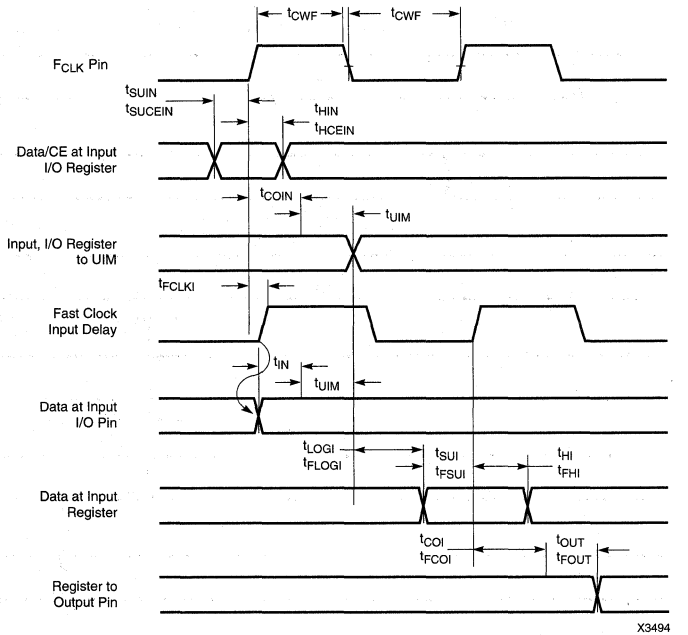
Combinational Switching Characteristics



Asynchronous Switching Characteristics



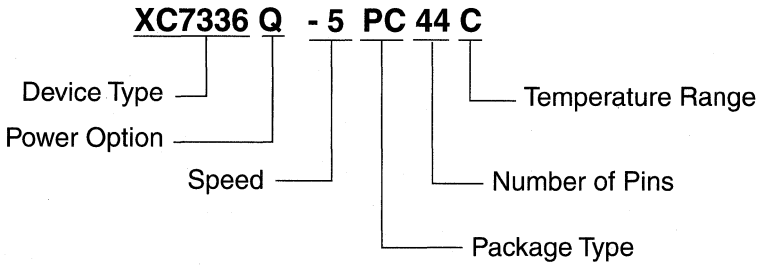
Synchronous Switching Characteristics



XC7336 Pinouts

VQ44/PQ44	PC44	Input	XC7336	Output
39	1	I/FO/FI	$\overline{MR}$	MC3-6
40	2	I/FO/FI		MC3-5
41	3	I/FO/FI		MC3-4
42	4	I/FO/FI		MC3-3
43	5	FO/FCLK0		MC3-2
44	6	FO/FCLK1		MC3-1
1	7	I/FO/FI		MC1-1
2	8	I/FO		MC1-2
3	9	I/FO		MC1-3
4	10		**GND**	
5	11	I/FO		MC1-4
6	12	I/FO		MC1-5
7	13	I/FO		MC1-6
8	14	I/FO		MC1-7
9	15	I/FO		MC1-8
10	16	I/FO		MC1-9
11	17	I/FO		MC4-9
12	18	I/FO/FI		MC4-8
13	19	I/FO/FI		MC4-7
14	20	I/FO/FI		MC4-6
15	21		V_{CCINT}	
16	22	I/FO		MC4-5
17	23		**GND**	
18	24	I/FO		MC4-4
19	25	I/FO		MC4-3
20	26	I/FO		MC4-2
21	27	I/FO		MC4-1
22	28	I/FI		
23	29	I/FO		MC2-9
24	30	I/FO		MC2-8
25	31		**GND**	
26	32		V_{CCIO}	
27	33	I/FO		MC2-7
28	34	I/FO		MC2-6
29	35	I/FO		MC2-5
30	36	I/FO		MC2-4
31	37	I/FO		MC2-3
32	38	I/FO		MC2-2
33	39	FO/FOE1		MC2-1
34	40	FO/FOE0		MC3-9
35	41		V_{CCINT}/V_{PP}	
36	42	I/FI		
37	43	I/FO/FI		MC3-8
38	44	I/FO/FI		MC3-7

Ordering Information



Power Options

Q Low Power -10, -12, -15 speeds

Speed Options

-15 15 ns pin-to-pin delay
-12 12 ns pin-to-pin delay
-10 10 ns pin-to-pin delay
-7 7.5 ns pin-to-pin delay (commercial only)
-5 5 ns pin-to-pin delay (commercial only)

Packaging Options

PC44 44-Pin Plastic Leaded Chip Carrier
WC44 44-Pin Windowed Ceramic Leaded Chip Carrier
PQ44 44-Pin Plastic Quad Flat Pack
VQ44 44-Pin Thin Quad Pack

Temperature Options

C Commercial0°C to 70°C
I Industrial–40°C to 85°C

Component Availability

Pins		44			
Type		Plastic PLCC	Ceramic CLCC	Plastic PQFP	Plastic VQFP
Code		PC44	WC44	PQ44	VQ44
XC7336	–15	CI	CI	CI	
	–12	CI	CI	C	
	–10	CI	CI	C	
	–7	C	C	C	
	–5	C	C	C	
XC7336Q	–15	CI	CI	C	C
	–12	CI	CI	C	C
	–10	C	C	C	C

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C

XC7354
54-Macrocell CMOS CPLD

June 1, 1996 (Version 1.0) | Product Specification

Features

- High-performance Complex Programmable Logic Devices (CPLDs)
  - 7.5 ns pin-to-pin speeds on all fast inputs
  - Up to 125 MHz maximum clock frequency
- 100% PCI compliant
- 18 outputs with 24 mA drive
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 61 MHz 18-bit accumulators
- Multiple independent clocks
- Up to 54 inputs programmable as direct, latched, or registered
- Power management options
- Multiple security bits for design protection
- 54 macrocells with programmable I/O architecture
- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - 4 High-Density Function Blocks
- 0.8 µ CMOS EPROM technology
- Available in 44-pin and 68-pin PLCC and CLCC packages

General Description

The XC7354 is a high performance CPLD providing general purpose logic integration. It consists of two PAL-like 24V9 Fast Function Blocks and four High Density Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™).

Power Management

The XC7354 features a power-management scheme that permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC}\ (mA) = MC_{HP}\ (3.0) + MC_{LP}\ (2.6) + MC\ (0.006\ mA/MHz)\ f$$

Where:

MC_{HP} = Macrocells in high-performance mode
MC_{LP} = Macrocells in low-power mode
MC = Total number of macrocells used
f = Clock frequency (MHz)

Figure 1 shows a typical power calculation for the XC7354 device, programmed as three 16-bit counters and operating at the indicated clock frequency.

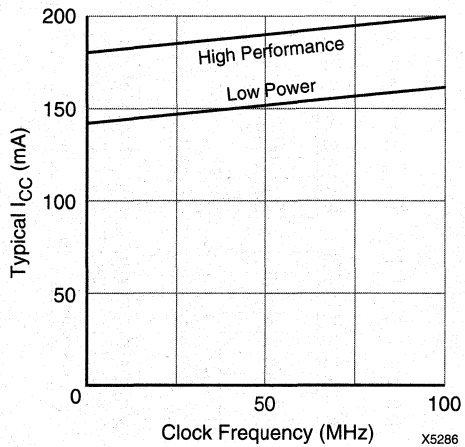


Figure 1: Typical I_{CC} vs. Frequency for XC7354

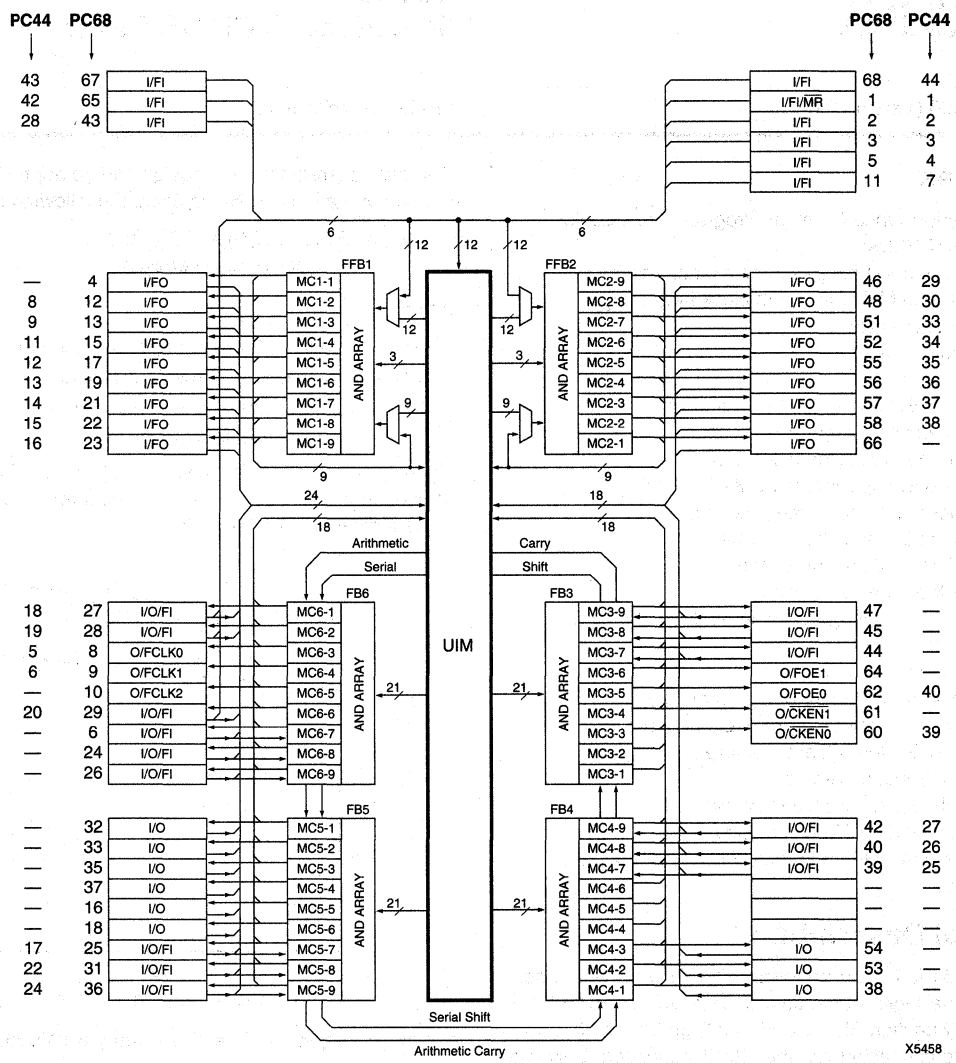


Figure 2: XC7354 Architecture

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT} V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_A = –55°C to T_C + 125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V
T_{IN}	Input signal transition time		50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage	I_{OL} = 24 mA (FO) I_{OL} = 12 mA (I/O) V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT}[1]	Output capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}[2]	Supply current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5V f = 1.0 MHz @ 25°C	140 Typ		mA

Notes: 1. Sample tested.
2. Measured with device programmed as three 16-bit counters.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Fast Function Block (FFB) External AC Characteristics[3]

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency [1, 2, 4]	125.0		100.0		80.0		66.7		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		8.0		9.0		12.0	ns
t_{PDFO}	Fast input to output valid [1, 2]		7.5		10.0		12.0		15.0	ns
t_{PDFU}	I/O to output valid [1, 2]		12.0		16.0		19.0		23.0	ns
t_{CWF}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
3. All appropriate AC specifications tested using Figure 3 as the test load circuit.
4. Export Control Max. flip-flop toggle rate.

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_C	Max count frequency [1, 2]	95.2		76.9		66.7		55.6		MHz
t_{SU}	I/O setup time before FCLK ↑ [1, 2]	10.5		13.0		15.0		18.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		10.0		12.0		15.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	4.0		6.0		7.0		9.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		13.5		17.0		20.0		24.0	ns
t_{PD}	I/O to output valid [1, 2]		16.5		22.0		27.0		32.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [1]		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [1]		3.5		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0	ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [1]		3.5		3.5		4.0		5.0	ns
t_{LOGILP}	Low power FB logic delay [1]		7.0		7.5		9.0		11.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	13.5		16.0		18.0		21.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0	ns
t_{CARY8}	ALU carry delay within 1 FB [2]		5.0		6.0		8.0		12.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [2]		1.0		1.5		2.0		3.0	ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for adder with registered outputs.

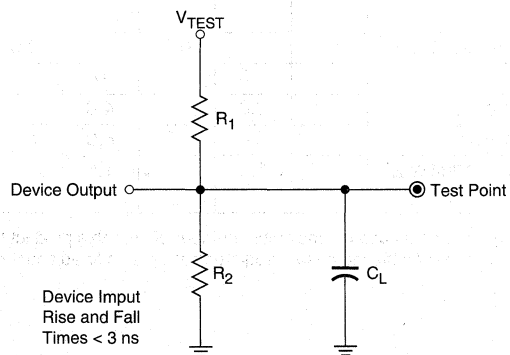
I/O Block External AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) [1]	95.2		76.9		66.7		55.6		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Internal AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0	ns
t_{UIM}	Universal Interconnect Matrix delay		4.5		6.0		7.0		8.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3491

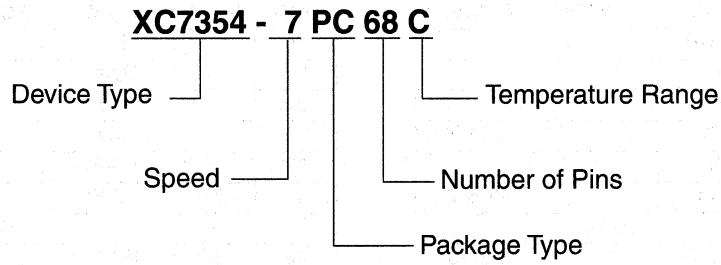
Figure 3: AC Load Circuit

XC7354 Pinouts

PC68	PC44	Input	XC7354	Output
1	1	I/FI/ $\overline{MR}$		
2	2	I/FI		
3	3	I/FI		
4	–	I/FO		MC1-1
5	4	I/FI		
6	–	I/O/FI		MC6-7
7	–		**GND**	
8	5	O/FCLK0		MC6-3
9	6	O/FCLK1		MC6-4
10	–	O/FCLK2		MC6-5
11	7	I/FI		
12	8	I/FO		MC1-2
13	9	I/FO		MC1-3
14	10		**GND**	
15	11	I/FO		MC1-4
16	–	I/O		MC5-5
17	12	I/FO		MC1-5
18	–	I/O		MC5-6
19	13	I/FO		MC1-6
20	–		V_{CCIO}	
21	14	I/FO		MC1-7
22	15	I/FO		MC1-8
23	16	I/FO		MC1-9
24	–	I/O/FI		MC6-8
25	17	I/O/FI		MC5-7
26	–	I/O/FI		MC6-9
27	18	I/O/FI		MC6-1
28	19	I/O/FI		MC6-2
29	20	I/O/FI		MC6-6
30	21		V_{CCINT}	
31	22	I/O/FI		MC5-8
32	–	I/O		MC5-1
33	–	I/O		MC5-2
34	23		**GND**	

PC68	PC44	Input	XC7354	Output
35	–	I/O		MC5-3
36	24	I/O/FI		MC5-9
37	–	I/O		MC5-4
38	–	I/O		MC4-1
39	25	I/O/FI		MC4-7
40	26	I/O/FI		MC4-8
41	–		**GND**	
42	27	I/O/FI		MC4-9
43	28	I/FI		
44	–	I/O/FI		MC3-7
45	–	I/O/FI		MC3-8
46	29	I/FO		MC2-9
47	–	I/O/FI		MC3-9
48	30	I/FO		MC2-8
49	31		**GND**	
50	32		V_{CCIO}	
51	33	I/FO		MC2-7
52	34	I/FO		MC2-6
53	–	I/O		MC4-2
54	–	I/O		MC4-3
55	35	I/FO		MC2-5
56	36	I/FO		MC2-4
57	37	I/FO		MC2-3
58	38	I/FO		MC2-2
59	–		V_{CCINT}	
60	39	O/$\overline{CKEN0}$		MC3-3
61	–	O/$\overline{CKEN1}$		MC3-4
62	40	O/FOE0		MC3-5
63	41		V_{CCINT}/V_{PP}	
64	–	O/FOE1		MC3-6
65	42	I/FI		
66	–	I/FO		MC2-1
67	43	I/FI		
68	44	I/FI		

Ordering Information



Speed Options

-15	15 ns pin-to-pin delay
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay (commercial and industrial only)
-7	7.5 ns pin-to-pin delay (commercial only)

Packaging Options

PC44	44-Pin Plastic Leaded Chip Carrier
WC44	44-Pin Windowed Ceramic Leaded Chip Carrier
PC68	68-Pin Plastic Leaded Chip Carrier
WC68	68-Pin Windowed Ceramic Leaded Chip Carrier

Temperature Options

C	Commercial0°C to 70°C
I	Industrial -40°C to 85°C
M	Military -55°C (Ambient) to 125°C (Case)

Component Availability

Pins		44		68	
Type		Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC
Code		PC44	WC44	PC68	WC68
XC7354	–15	CI	CI	CI	CIM
	–12	CI	CI	CI	CIM
	–10	CI	CI	CI	CI
	–7	C	C	C	C

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C M = Military = –55°C(A) to 125°C (C)

Features

- High-performance Complex Programmable Logic Devices (CPLDs)
  - 7.5 ns pin-to-pin speeds on all fast inputs
  - Up to 125 MHz maximum clock frequency
- 100% PCI compliant
- 18 outputs with 24 mA drive
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 61 MHz 18-bit accumulators
- Multiple independent clocks
- Up to 84 inputs programmable as direct, latched, or registered
- Power management options
- Multiple security bits for design protection
- 72 macrocells with programmable I/O architecture
- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - 6 High-Density Function Blocks
- 0.8 µ CMOS EPROM technology
- Available in 68-pin and 84-pin PLCC/CLCC and 100-pin PQFP packages

General Description

The XC7372 is a high performance CPLD providing general purpose logic integration. It consists of two PAL-like 24V9 Fast Function Blocks and six High Density Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™). See Figure 2 for the architecture overview.

Power Management

The XC7372 features a power-management scheme that permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC}\ (mA) = MC_{HP}\ (3.1) + MC_{LP}\ (2.6) + MC\ (0.012\ mA/MHz)\ f$$

Where:

MC_{HP} = Macrocells in high-performance mode
MC_{LP} = Macrocells in low-power mode
MC = Total number of macrocells used
f = Clock frequency (MHz)

Figure 1 shows a typical power calculation for the XC7372 device, programmed as four 16-bit counters and operating at the indicated clock frequency.

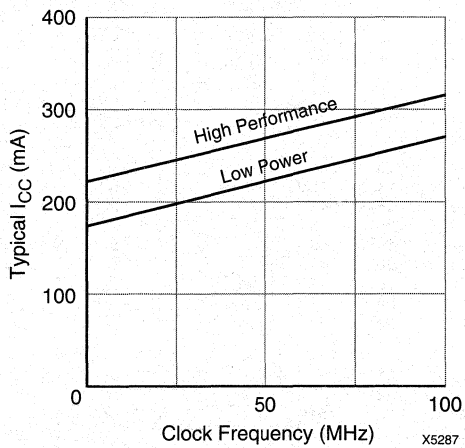


Figure 1: Typical I_{CC} vs. Frequency for XC7372

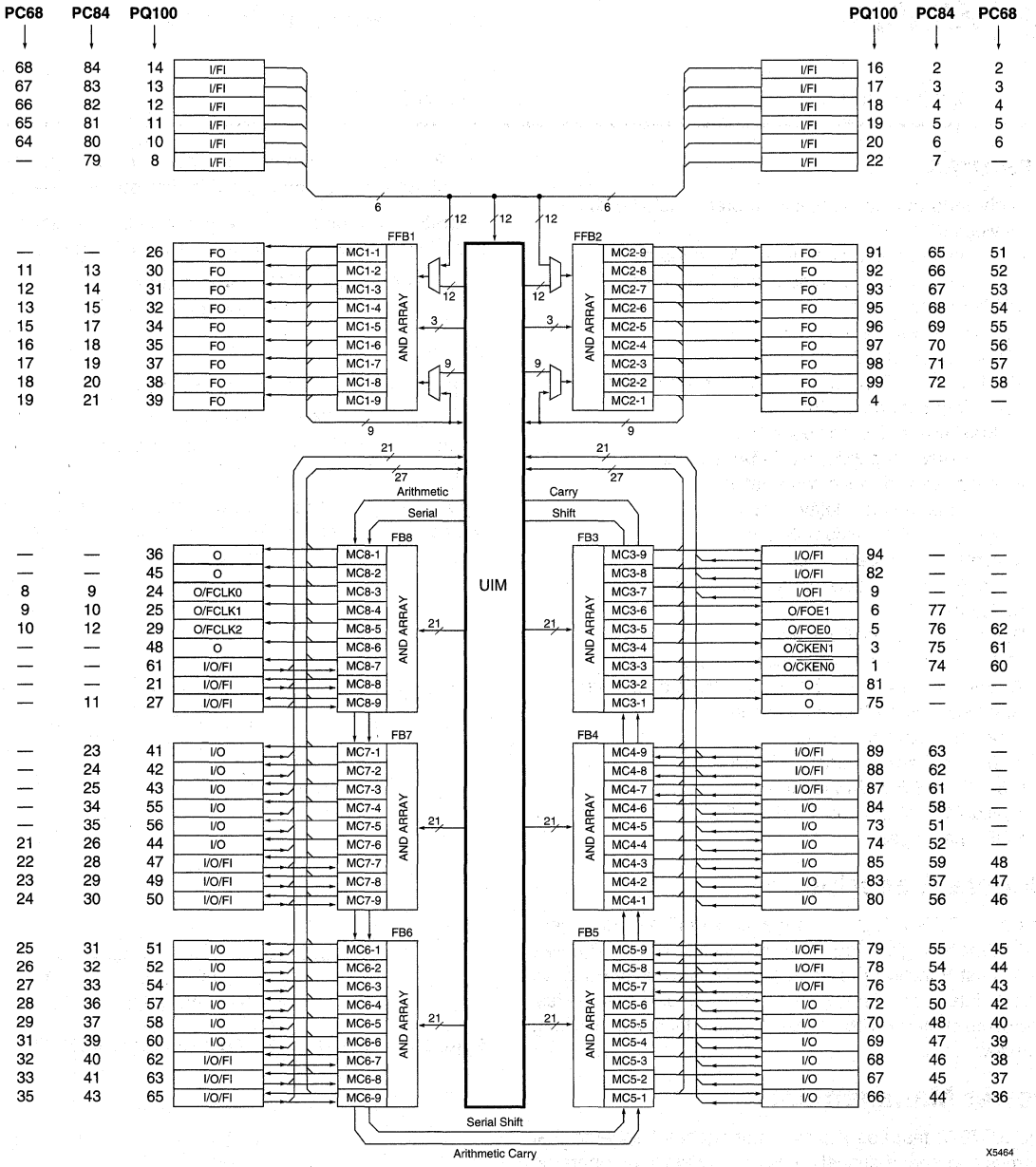


Figure 2: XC7372 Architecture

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}/ V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_A = –55°C to T_C + 125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V
T_{IN}	Input signal transition time		50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage	I_{OL} = 24 mA (FO) I_{OL} = 12 mA (I/O) V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT}[1]	Output capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}[2]	Supply current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5V f = 1.0 MHz @ 25°C	187 Typ		mA

Notes: 1. Sample tested.
2. Measured with device programmed as four 16-bit counters.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Fast Function Block (FFB) External AC Characteristics[3]

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency [1, 2, 4]	125.0		100.0		80.0		66.7		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		8.0		9.0		12.0	ns
t_{PDFO}	Fast input to output valid [1, 2]		7.5		10.0		12.0		15.0	ns
t_{PDFU}	I/O to output valid [1, 2]		14.0		17.0		20.0		24.0	ns
t_{CWF}	Fast clock pulse width (High or Low)	4.0		5.0		5.5		6.0		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
3. All appropriate specifications tested using Figure 3 as the test load circuit.
4. Export Control Max. flip-flop toggle rate.

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_C	Max count frequency [1, 2]	95.2		71.4		62.5		52.6		MHz
t_{SU}	I/O setup time before FCLK ↑ [1, 2]	12.5		14.0		16.0		19.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		10.0		12.0		15.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	6.0		6.0		7.0		9.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		13.5		18.0		21.0		25.0	ns
t_{PD}	I/O to output valid [1, 2]		18.5		23.0		28.0		33.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [1]		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [1]		3.5		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0	ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [1]		3.5		3.5		4.0		5.0	ns
t_{LOGILP}	Low power FB logic delay [1]		7.0		7.5		9.0		11.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	13.5		17.0		19.0		22.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0	ns
t_{CARY8}	ALU carry delay within 1 FB [2]		5.0		6.0		8.0		12.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [2]		1.0		1.5		2.0		3.0	ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for adder with registered outputs.

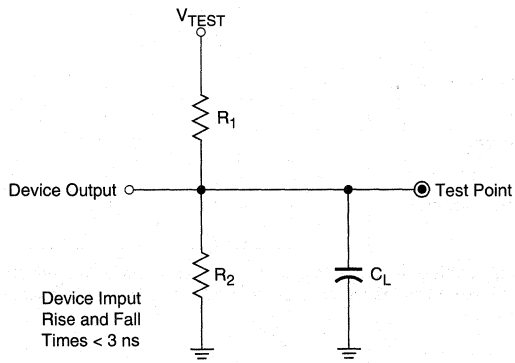
I/O Block External AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) [1]	95.2		71.4		62.5		52.6		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Internal AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0	ns
t_{UIM}	Universal Interconnect Matrix delay		6.5		7.0		8.0		9.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

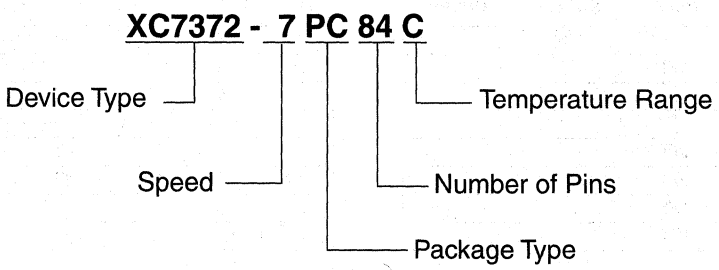
X3491

Figure 3: AC Load Circuit

XC7372 Pinouts

PQ100	PC84	PC68	Input	XC7372	Output
15	1	1		$\overline{MR}$	
16	2	2	I/FI		
17	3	3	I/FI		
18	4	4	I/FI		
19	5	5	I/FI		
20	6	6	I/FI		
21	–	–	I/O/FI		MC8-8
22	7	–	I/FI		
23	8	7		**GND**	
24	9	8	O/FCLK0		MC8-3
25	10	9	O/FCLK1		MC8-4
26	–	–	FO		MC1-1
27	11	–	I/O/FI		MC8-9
28	–	–		V_{CCIO}	
29	12	10	O/FCLK2		MC8-5
30	13	11	FO		MC1-2
31	14	12	FO		MC1-3
32	15	13	FO		MC1-4
33	16	14		**GND**	
34	17	15	FO		MC1-5
35	18	16	FO		MC1-6
36	–	–	O		MC8-1
37	19	17	FO		MC1-7
38	20	18	FO		MC1-8
39	21	19	FO		MC1-9
40	22	20		V_{CCIO}	
41	23	–	I/O		MC7-1
42	24	–	I/O		MC7-2
43	25	–	I/O		MC7-3
44	26	21	I/O		MC7-6
45	–	–	O		MC8-2
46	27	–		**GND**	
47	28	22	I/O/FI		MC7-7
48	–	–	O		MC8-6
49	29	23	I/O/FI		MC7-8
50	30	24	I/O/FI		MC7-9
51	31	25	I/O		MC6-1
52	32	26	I/O		MC6-2
53	–	–		V_{CCIO}	
54	33	27	I/O		MC6-3
55	34	–	I/O		MC7-4
56	35	–	I/O		MC7-5
57	36	28	I/O		MC6-4
58	37	29	I/O		MC6-5
59	38	30		V_{CCINT}	
60	39	31	I/O		MC6-6
61	–	–	I/O/FI		MC8-7
62	40	32	I/O/FI		MC6-7
63	41	33	I/O/FI		MC6-8
64	42	34		**GND**	
65	43	35	I/O/FI		MC6-9
66	44	36	I/O		MC5-1
67	45	37	I/O		MC5-2
68	46	38	I/O		MC5-3
69	47	39	I/O		MC5-4
70	48	40	I/O		MC5-5
71	49	41		**GND**	
72	50	42	I/O		MC5-6
73	51	–	I/O		MC4-5
74	52	–	I/O		MC4-4
75	–	–	O		MC3-1
76	53	43	I/O/FI		MC5-7
77	–	–		**GND**	
78	54	44	I/O/FI		MC5-8
79	55	45	I/O/FI		MC5-9
80	56	46	I/O		MC4-1
81	–	–	O		MC3-2
82	–	–	I/O/FI		MC3-8
83	57	47	I/O		MC4-2
84	58	–	I/O		MC4-6
85	59	48	I/O		MC4-3
86	60	49		**GND**	
87	61	–	I/O/FI		MC4-7
88	62	–	I/O/FI		MC4-8
89	63	–	I/O/FI		MC4-9
90	64	50		V_{CCIO}	
91	65	51	FO		MC2-9
92	66	52	FO		MC2-8
93	67	53	FO		MC2-7
94	–	–	I/O/FI		MC3-9
95	68	54	FO		MC2-6
96	69	55	FO		MC2-5
97	70	56	FO		MC2-4
98	71	57	FO		MC2-3
99	72	58	FO		MC2-2
100	73	59		V_{CCINT}	
1	74	60	O/$\overline{CKEN0}$		MC3-3
2	–	–		**GND**	
3	75	61	O/$\overline{CKEN1}$		MC3-4
4	–	–	FO		MC2-1
5	76	62	O/FOE0		MC3-5
6	77	–	O/FOE1		MC3-6
7	78	63		V_{CCINT}/ V_{PP}	
8	79	–	I/FI		
9	–	–	I/O/FI		MC3-7
10	80	64	I/FI		
11	81	65	I/FI		
12	82	66	I/FI		
13	83	67	I/FI		
14	84	68	I/FI		

Ordering Information



Speed Options

-15	15 ns pin-to-pin delay
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay (commercial and industrial only)
-7	7.5 ns pin-to-pin delay (commercial only)

Packaging Options

PC68	68-Pin Plastic Leaded Chip Carrier
WC68	68-Pin Windowed Ceramic Leaded Chip Carrier
PC84	84-Pin Plastic Leaded Chip Carrier
WC84	84-Pin Windowed Ceramic Leaded Chip Carrier
PQ100	100-Pin Plastic Quad Flat Pack

Temperature Options

C	Commercial0°C to 70°C
I	Industrial -40°C to 85°C
M	Military -55°C (Ambient) to 125°C (Case)

Component Availability

Pins		68		84		100
Type		Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PQFP
Code		PC68	WC68	PC84	WC84	PQ100
XC7372	–15	CI	CIM	CI	CIM	CI
	–12	CI	CIM	CI	CI	CI
	–10	CI	CI	CI	CI	CI
	–7	C	C	C	C	C

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C M = Military = –55°C(A) to 125°C (C)

XC73108
108-Macrocell CMOS CPLD

June 1, 1996 (Version 1.0) | Product Specification

Features

- High-performance Complex Programmable Logic Devices (CPLDs)
  - 7.5 ns pin-to-pin speeds on all fast inputs
  - Up to 125 MHz maximum clock frequency
- 100% PCI compliant
- 18 outputs with 24 mA drive
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 56 MHz 18-bit accumulators
- Multiple independent clocks
- Up to 120 inputs programmable as direct, latched, or registered
- Power management options
- Multiple security bits for design protection
- 108 macrocells with programmable I/O architecture
- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - 10 High-Density Function Blocks
- 0.8 µ CMOS EPROM technology
- Available in 84-pin and 84-pin PLCC/CLCC, 144-pin PGA, 100-pin and 160-pin PQFP, and 225-pin BGA packages

General Description

The XC73108 is a high performance CPLD providing general purpose logic integration. It consists of two PAL-like 24V9 Fast Function Blocks and ten High Density Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™).

Power Management

The XC73108 features a power-management scheme that permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC}\ (mA) = MC_{HP}\ (2.4) + MC_{LP}\ (2.1) + MC\ (0.015\ mA/MHz)\ f$$

Where:

MC_{HP} = Macrocells in high-performance mode
MC_{LP} = Macrocells in low-power mode
MC = Total number of macrocells used
f = Clock frequency (MHz)

Figure 1 shows a typical power calculation for the XC73108 device, programmed as six 16-bit counters and operating at the indicated clock frequency.

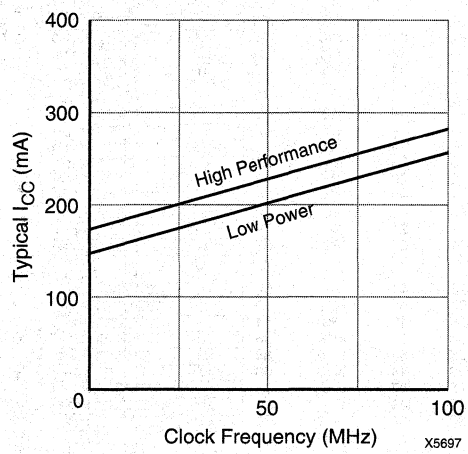


Figure 1: Typical I_{CC} vs. Frequency for XC73108

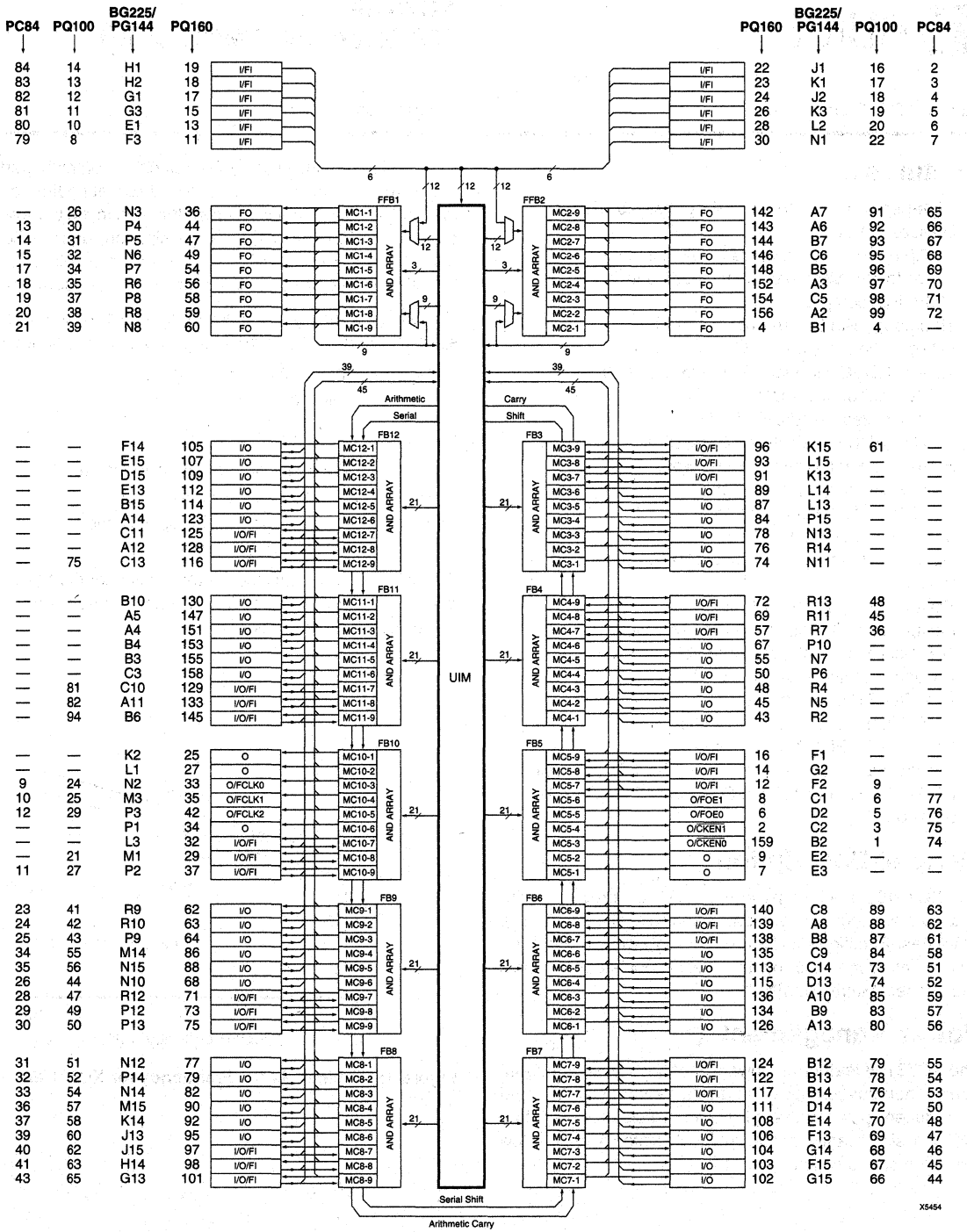


Figure 2: XC73108 Architecture

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT} V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_A = –55°C to T_C + 125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V
T_{IN}	Input signal transition time		50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage	I_{OL} = 24 mA (FO) I_{OL} = 12 mA (I/O) V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT}[1]	Output capacitance	V_{IN} = GND f = 1.0 MHz		20.0	pF
I_{CC}[2]	Supply current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5V f = 1.0 MHz @ 25°C	227 Typ		mA

Notes: 1. Sample tested.
2. Measured with device programmed as six 16-bit counters.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Fast Function Block (FFB) External AC Characteristics[3]

		XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
f_{CF}	Max count frequency [1, 2, 4]	125.0		100.0		80.0		66.7		50.0		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		10.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		8.0		9.0		12.0		15.0	ns
t_{PDFO}	Fast input to output valid [1, 2]		7.5		10.0		12.0		15.0		20.0	ns
t_{PDFU}	I/O to output valid [1, 2]		13.5		19.0		22.0		27.0		35.0	ns
t_{CWF}	Fast clock pulse width (High or Low)	4.0		5.0		5.5		6.0		6.0		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
3. All appropriate AC specifications tested using Figure 3 as the test load circuit.
4. Export Control Max. flip-flop toggle rate.

High-Density Function Block (FB) External AC Characteristics

		XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
f_C	Max count frequency [1, 2]	83.3		62.5		55.6		45.5		35.7		MHz
t_{SU}	I/O setup time before FCLK ↑ [1, 2]	12.0		16.0		18.0		22.0		28.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		10.0		12.0		15.0		20.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	4.0		6.0		7.0		9.0		12.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		15.0		20.0		23.0		28.0		36.0	ns
t_{PD}	I/O to output valid [1, 2]		18.0		25.0		30.0		36.0		45.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		12.0		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [1]		1.5		1.5		2.0		2.0		3.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [1]		3.5		5.5		7.0		8.0		11.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		6.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		4.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0		2.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0		6.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5		2.0	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0		10.0	ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [1]		3.5		3.5		4.0		5.0		6.0	ns
t_{LOGILP}	Low power FB logic delay [1]		7.0		7.5		9.0		11.0		14.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		6.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		6.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0		7.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	15.0		19.0		21.0		25.0		31.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		20.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		12.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0		9.0	ns
t_{CARY8}	ALU carry delay within 1 FB [2]		5.0		6.0		8.0		12.0		15.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [2]		1.0		1.5		2.0		3.0		4.0	ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for adder with registered outputs.

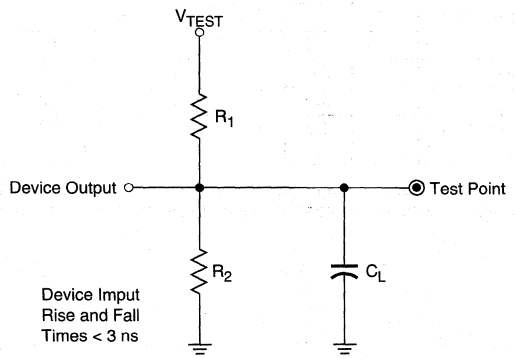
I/O Block External AC Characteristics

Symbol	Parameter	XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) [1]	83.3		62.5		55.6		45.5		35.7		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		10.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0		6.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		12.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		6.0		ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Internal AC Characteristics

Symbol	Parameter	XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0		6.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0		9.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0		14.0	ns
t_{UIM}	Universal Interconnect Matrix delay		6.0		9.0		10.0		12.0		15.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0		20.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0		20.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0		5.0	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3491

Figure 3: AC Load Circuit

XC73108 Pinouts

PQ160	PG144 BG225	PQ100	PC84	Input	XC73108	Output
1	D3	–	–		V_{CCIO}	
2	C2	3	75	O/CKEN1		MC5-4
3	–	–	–		N/C	
4	B1	4	–	FO		MC2-1
5	–	–	–		N/C	
6	D2	5	76	O/FOE0		MC5-5
7	E3	–	–	O		MC5-1
8	C1	6	77	O/FOE1		MC5-6
9	E2	–	–	O		MC5-2
10	D1	7	78		V_{CCINT}/V_{PP}	
11	F3	8	79	I/FI		
12	F2	9	–	I/O/FI		MC5-7
13	E1	10	80	I/FI		
14	G2	–	–	I/O/FI		MC5-8
15	G3	11	81	I/FI		
16	F1	–	–	I/O/FI		MC5-9
17	G1	12	82	I/FI		
18	H2	13	83	I/FI		
19	H1	14	84	I/FI		
20	H3	–	–		**GND**	
21	J3	15	1		MR	
22	J1	16	2	I/FI		
23	K1	17	3	I/FI		
24	J2	18	4	I/FI		
25	K2	–	–	O		MC10-1
26	K3	19	5	I/FI		
27	L1	–	-	O		MC10-2
28	L2	20	6	I/FI		
29	M1	21	–	I/O/FI		MC10-8
30	N1	22	7	I/FI		
31	M2	23	8		**GND**	
32	L3	–	–	I/O/FI		MC10-7
33	N2	24	9	O/FCLK0		MC10-3
34	P1	–	–	O		MC10-6
35	M3	25	10	O/FCLK1		MC10-4
36	N3	26	–	FO		MC1-1
37	P2	27	11	I/O/FI		MC10-9
38	–	–	–		N/C	
39	–	–	–		N/C	
40	R1	–	–		**GND**	

PQ160	PG144 BG225	PQ100	PC84	Input	XC73108	Output
41	N4	28	–		V_{CCIO}	
42	P3	29	12	O/FCLK2		MC10-5
43	R2	–	–	I/O		MC4-1
44	P4	30	13	FO		MC1-2
45	N5	–	–	I/O		MC4-2
46	R3	–	–		V_{CCINT}	
47	P5	31	14	FO		MC1-3
48	R4	–	–	I/O		MC4-3
49	N6	32	15	FO		MC1-4
50	P6	–	–	I/O		MC4-4
51	R5	33	16		**GND**	
52	–	–	–		N/C	
53	–	–	–		N/C	
54	P7	34	17	FO		MC1-5
55	N7	–	–	I/O		MC4-5
56	R6	35	18	FO		MC1-6
57	R7	36	–	I/O/FI		MC4-7
58	P8	37	19	FO		MC1-7
59	R8	38	20	FO		MC1-8
60	N8	39	21	FO		MC1-9
61	N9	40	22		V_{CCIO}	
62	R9	41	23	I/O		MC9-1
63	R10	42	24	I/O		MC9-2
64	P9	43	25	I/O		MC9-3
65	–	–	–		N/C	
66	–	–	–		N/C	
67	P10	–	–	I/O		MC4-6
68	N10	44	26	I/O		MC9-6
69	R11	45	–	I/O/FI		MC4-8
70	P11	46	27		**GND**	
71	R12	47	28	I/O/FI		MC9-7
72	R13	48	–	I/O/FI		MC4-9
73	P12	49	29	I/O/FI		MC9-8
74	N11		–	I/O		MC3-1
75	P13	50	30	I/O/FI		MC9-9
76	R14	–	–	I/O		MC3-2
77	N12	51	31	I/O		MC8-1
78	N13	–	–	I/O		MC3-3
79	P14	52	32	I/O		MC8-2
80	R15	–	–		**GND**	

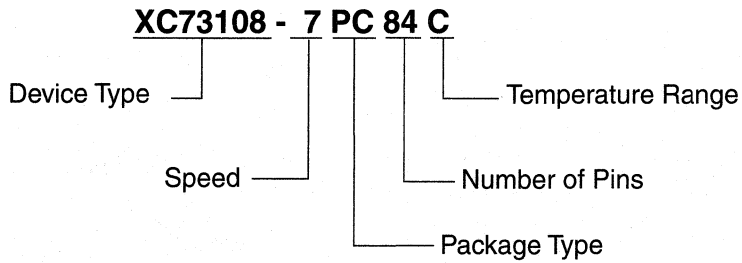
Note: With the XC73108 in the 225-pin ball grid array package, only 144 of the solder balls are connected, the remaining solder balls should be left unconnected.

XC73108 Pinouts (continued)

PQ160	PG144 BG225	PQ100	PC84	Input	XC73108	Output
81	M13	53	–		V_{CCIO}	
82	N14	54	33	I/O		MC8-3
83	–	–	–		N/C	
84	P15	–	–	I/O		MC3-4
85	–	–	–		N/C	
86	M14	55	34	I/O		MC9-4
87	L13	–	–	I/O		MC3-5
88	N15	56	35	I/O		MC9-5
89	L14	–	–	I/O		MC3-6
90	M15	57	36	I/O		MC8-4
91	K13	–	–	I/O/FI		MC3-7
92	K14	58	37	I/O		MC8-5
93	L15	–	–	I/O/FI		MC3-8
94	J14	59	38		V_{CCINT}	
95	J13	60	39	I/O		MC8-6
96	K15	61	–	I/O/FI		MC3-9
97	J15	62	40	I/O/FI		MC8-7
98	H14	63	41	I/O/FI		MC8-8
99	H15	–	–		**GND**	
100	H13	64	42		**GND**	
101	G13	65	43	I/O/FI		MC8-9
102	G15	66	44	I/O		MC7-1
103	F15	67	45	I/O		MC7-2
104	G14	68	46	I/O		MC7-3
105	F14	–	–	I/O		MC12-1
106	F13	69	47	I/O		MC7-4
107	E15	–	–	I/O		MC12-2
108	E14	70	48	I/O		MC7-5
109	D15	–	–	I/O		MC12-3
110	C15	71	49		**GND**	
111	D14	72	50	I/O		MC7-6
112	E13	–	–	I/O		MC12-4
113	C14	73	51	I/O		MC6-5
114	B15	–	–	I/O		MC12-5
115	D13	74	52	I/O		MC6-4
116	C13	75	–	I/O/FI		MC12-9
117	B14	76	53	I/O/FI		MC7-7
118	–	–	–		N/C	
119	–	–	–		N/C	
120	A15	77	–		**GND**	

PQ160	PG144 BG225	PQ100	PC84	Input	XC73108	Output
121	C12	–	–		V_{CCIO}	
122	B13	78	54	I/O/FI		MC7-8
123	A14	–	–	I/O		MC12-6
124	B12	79	55	I/O/FI		MC7-9
125	C11	–	–	I/O/FI		MC12-7
126	A13	80	56	I/O		MC6-1
127	B11	–	–		**GND**	
128	A12	–	–	I/O/FI		MC12-8
129	C10	81	–	I/O/FI		MC11-7
130	B10	–	–	I/O		MC11-1
131	–	–	–		N/C	
132	–	–	–		N/C	
133	A11	82	–	I/O/FI		MC11-8
134	B9	83	57	I/O		MC6-2
135	C9	84	58	I/O		MC6-6
136	A10	85	59	I/O		MC6-3
137	A9	86	60		**GND**	
138	B8	87	61	I/O/FI		MC6-7
139	A8	88	62	I/O/FI		MC6-8
140	C8	89	63	I/O/FI		MC6-9
141	C7	90	64		V_{CCIO}	
142	A7	91	65	FO		MC2-9
143	A6	92	66	FO		MC2-8
144	B7	93	67	FO		MC2-7
145	B6	94	–	I/O/FI		MC11-9
146	C6	95	68	FO		MC2-6
147	A5	–	–	I/O		MC11-2
148	B5	96	69	FO		MC2-5
149	–	–	–		N/C	
150	–	–	–		N/C	
151	A4	–	–	I/O		MC11-3
152	A3	97	70	FO		MC2-4
153	B4	–	–	I/O		MC11-4
154	C5	98	71	FO		MC2-3
155	B3	–	–	I/O		MC11-5
156	A2	99	72	FO		MC2-2
157	C4	100	73		V_{CCINT}	
158	C3	–	–	I/O		MC11-6
159	B2	1	74	O/CKEN0		MC5-3
160	A1	2	–		**GND**	

Ordering Information



Speed Options

-20	20 ns pin-to-pin delay
-15	15 ns pin-to-pin delay
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay (commercial and industrial only)
-7	7.5 ns pin-to-pin delay (commercial only)

Packaging Options

PC84	84-Pin Plastic Leaded Chip Carrier
WC84	84-Pin Windowed Ceramic Leaded Chip Carrier
PQ100	100-Pin Plastic Quad Flat Pack
PG144	144-Pin Windowed Pin-Grid-Array
PQ160	160-Pin Plastic Quad Flat Pack
BG225	225-Pin Plastic Ball-Grid-Array

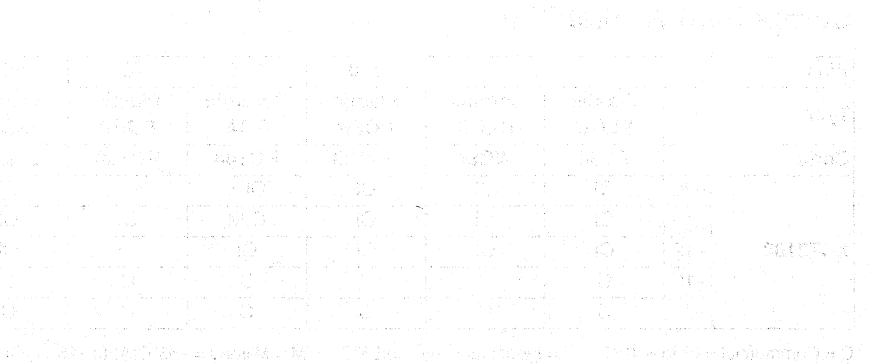
Temperature Options

C	Commercial0°C to 70°C
I	Industrial -40°C to 85°C
M	Military -55°C (Ambient) to 125°C (Case)

Component Availability

Pins		84		100	144	160	225
Type		Plastic PLCC	Ceramic CLCC	Plastic PQFP	Ceramic PGA	Plastic PQFP	Plastic BGA
Code		PC84	WC84	PQ100	PG144	PQ160	BG225
XC73108	-20	CI	CI	CI	CIM	CI	CI
	-15	CI	CI	CI	CIM	CI	CI
	-12	CI	CI	CI	CI	CI	CI
	-10	C	C	C	C	C	C
	-7	C	C	C	C	C	C

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C M = Military = –55°C(A) to 125°C (C)



Features

- High-performance Complex Programmable Logic Devices (CPLDs)
  - 7.5 ns pin-to-pin speeds on all fast inputs
  - Up to 100 MHz maximum clock frequency
- 100% PCI compliant
- 18 outputs with 24 mA drive
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 43 MHz 16-bit accumulators
- Multiple independent clocks
- Up to 132 inputs programmable as direct, latched, or registered
- Power management options
- Multiple security bits for design protection
- 144 macrocells with programmable I/O architecture
- Advanced Dual-Block architecture
  - 4 Fast Function Blocks
  - 12 High-Density Function Blocks
- Programmable slew rate
- Programmable ground control
- 0.8 µ CMOS EPROM technology
- Available in 84-pin and 84-pin PLCC/CLCC, 144-pin PGA, 100-pin and 160-pin PQFP, and 225 BGA packages

General Description

The XC73144 is a high performance CPLD providing general purpose logic integration. It consists of four PAL-like 24V9 Fast Function Blocks and twelve High Density Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™).

Power Management

The XC73144 features a power-management scheme that permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC}\ (mA) = MC_{HP}\ (2.4) + MC_{LP}\ (2.1) + MC\ (0.015\ mA/MHz)\ f$$

Where:

MC_{HP} = Macrocells in high-performance mode
MC_{LP} = Macrocells in low-power mode
MC = Total number of macrocells used
f = Clock frequency (MHz)

Figure 1 shows a typical power calculation for the XC73144 device, programmed as eight 16-bit counters and operating at the indicated clock frequency.

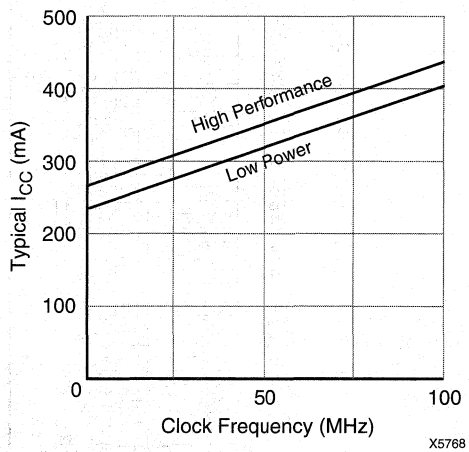


Figure 1: Typical I_{CC} vs. Frequency for XC73144

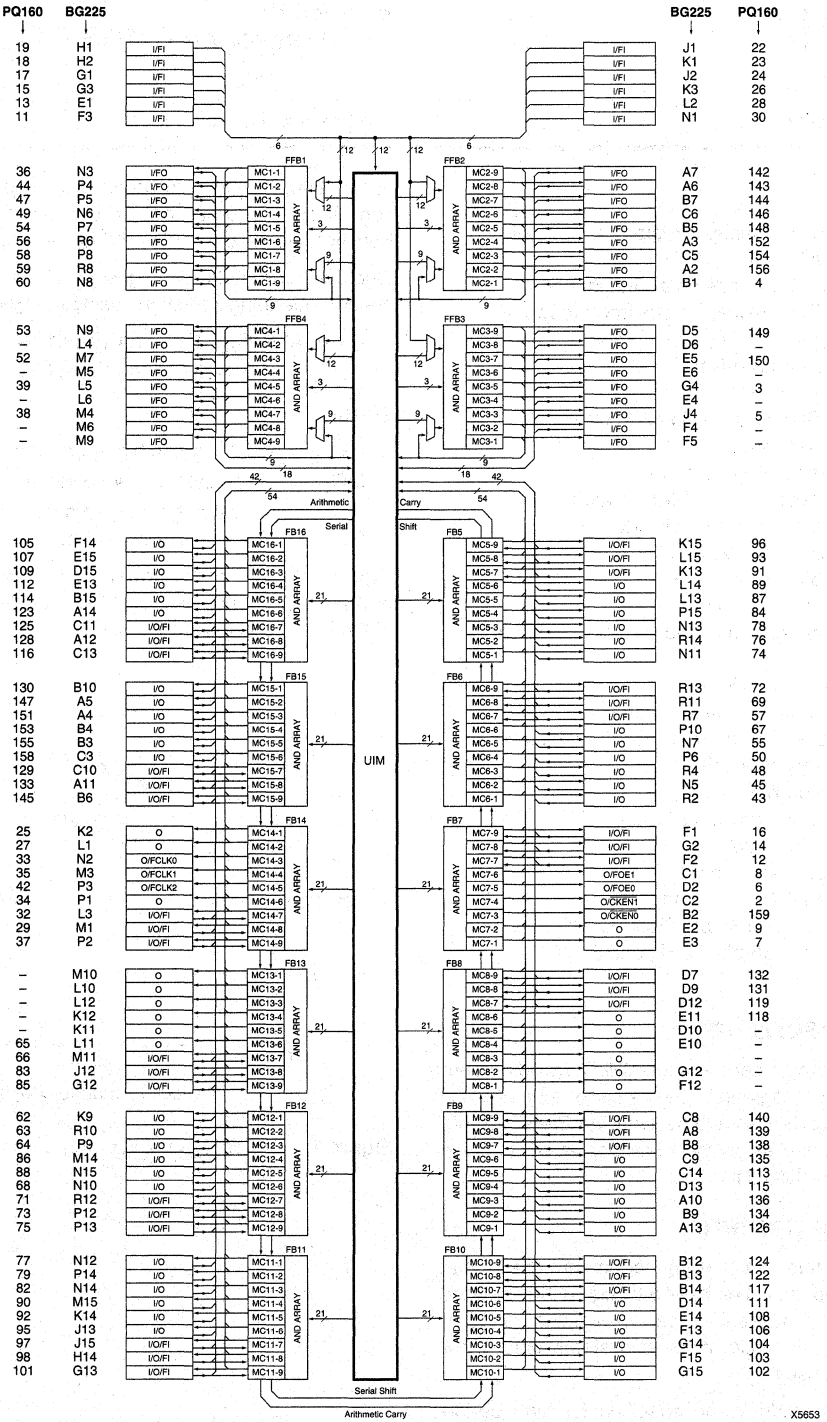


Figure 2: XC73144 Architecture

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT} V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_A = –55°C to T_C + 125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V
T_{IN}	Input signal transition time		50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT}[1]	Output capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}[2]	Supply current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5V f = 1.0 MHz @ 25°C	250 Typ		mA

Notes: 1. Sample tested.
2. Measured with device programmed as eight 16-bit counters.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Slew Rate and Programmable Ground Control

Due to the large number of high current drivers available on the XC73144, two programmable signal management features have been included – slew rate control (SRC) and ground control (GC). Slew rate control is primarily for external system benefit, to reduce ringing and other coupling phenomenon. SRC permits designers to select either 1 V/ns or 1.5 V/ns slew rate on a pin-by-pin basis for any output or I/O signal. This can be done with PLUSASM or schematically, as needed. The default slew rate is 1 V/ns. To assign the pins with equations (PLUSASM), the designer needs to only declare them as follows:

FAST ON <signal name list>

This will assign the signals in the list to have a 1.5 V/ns slew rate. Omitting the signal name list will globally set all signals to be 1.5 V/ns. Specific signals therefore can be declared with 1 V/ns slew rate as follows:

FAST OFF <signal name list>

Schematic control of SRC is also straightforward. Again, the default is 1 V/ns, but to assign specific pins fast, the designer need only attach the "FAST" attribute to the I/O or output buffer or the corresponding pin.

Programmable ground control is useful for internal chip signal management. The output buffers of the Fast Function Blocks have an impedance of approximately 7 Ω when switching high to low, where the High Density Function Blocks impedance is around 14 Ω. Since this low impedance is negligible compared to the impedance of the pin inductance when output current transients occur, a reasonable ground connection can be made by driving unused output pins low and physically attaching them to external ground. The XC73144 architecture permits the automatic assignment of external ground signals to all macrocells that are not declared as primary outputs or I/Os. Note that the logical function of the buried macrocell is fully preserved, while its output driver is driving low and physically attached to ground. Should designers not wish to employ programmable ground control, they need only declare all such pins as primary I/Os whether they will be attached externally or not.

Fast Function Block (FFB) External AC Characteristics[3]

		XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units
f_{CF}	Max count frequency [1, 2, 4]	105.0		100.0		80.0		66.7		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		7.0		9.0		12.0	ns
t_{PDFO}	Fast input to output valid [1, 2]		7.5		9.0		12.0		15.0	ns
t_{PDFU}	I/O to output valid [1, 2]		13.5		17.0		22.0		27.0	ns
t_{CWF}	Fast clock pulse width (High or Low)	4.0		5.0		5.5		6.0		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
3. All appropriate AC specifications tested using Figure 3 as the test load circuit.
4. Export Control Max. flip-flop toggle rate.

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_C	Max count frequency [1, 2]	83.3		62.5		55.6		45.5		MHz
t_{SU}	I/O setup time before FCLK ↑ [1, 2]	12.0		13.5		18.0		22.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		9.0		12.0		15.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	4.0		6.0		7.0		9.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		15.0		19.0		23.0		28.0	ns
t_{PD}	I/O to output valid [1, 2]		18.0		22.0		30.0		36.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [1]		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [1]		3.5		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0	ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [1]		3.5		3.5		4.0		5.0	ns
t_{LOGILP}	Low power FB logic delay [1]		7.0		7.5		9.0		11.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	15.0		19.0		21.0		25.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0	ns
t_{CARY8}	ALU carry delay within 1 FB [2]		5.0		6.0		8.0		12.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [2]		1.0		1.5		2.0		3.0	ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for adder with registered outputs.

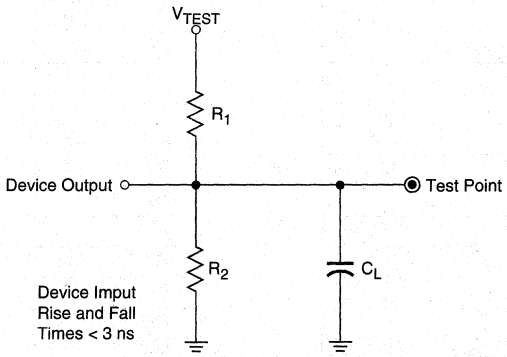
I/O Block External AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) [1]	83.3		62.5		55.6		45.5		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Internal AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0	ns
t_{UIM}	Universal Interconnect Matrix delay		6.0		9.0		10.0		12.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3491

Figure 3: AC Load Circuit

XC73144 Pinouts

BG225	PQ160	Input	XC73144	Output
D3	1		V_{CCIO}	
E4	-	I/FO		MC3-4
F4	-	I/FO		MC3-2
C2	2	O/CKEN1		MC7-4
F5	-	I/FO		MC3-1
G4	3	I/FO		MC3-5
B1	4	I/FO		MC2-1
J4	5	I/FO		MC3-3
D2	6	O/FOE0		MC7-5
E3	7	O		MC7-1
C1	8	O/FOE1		MC7-6
E2	9	O		MC7-2
D1	10		V_{CCINT}/V_{PP}	
F3	11	I/FI		
F2	12	I/O/FI		MC7-7
E1	13	I/FI		
G2	14	I/O/FI		MC7-8
G3	15	I/FI		
F1	16	I/O/FI		MC7-9
G1	17	I/FI		
H2	18	I/FI		
H1	19	I/FI		
H3	20		**GND**	
J3	21	I/FI	**MR**	
K5	-		V_{CCIO}	
J1	22	I/FI		
K1	23	I/FI		
J2	24	I/FI		
K2	25	O		MC14-1
K3	26	I/FI		
L1	27	O		MC14-2
L2	28	I/FI		
M1	29	I/O/FI		MC14-8
N1	30	I/FI		
M2	31		**GND**	
L3	32	I/O/FI		MC14-7
N2	33	O/FCLK0		MC14-3
P1	34	O		MC14-6
M3	35	O/FCLK1		MC14-4
N3	36	I/FO		MC1-1
K4	-	I/FO		MC4-1
L4	-	I/FO		MC4-2
P2	37	I/O/FI		MC14-9
M4	38	I/FO		MC4-3
L5	39	I/FO		MC4-5
R1	40		**GND**	

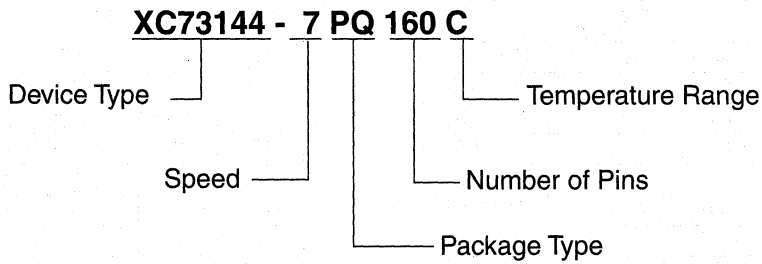
BG225	PQ160	Input	XC73144	Output
N4	41		V_{CCIO}	
P3	42	O/FCLK2		MC14-5
R2	43	I/O		MC6-1
P4	44	I/FO		MC1-2
N5	45	I/O		MC6-2
R3	46		V_{CCINT}	
M5	-	I/FO		MC4-4
P5	47	I/FO		MC1-3
R4	48	I/O		MC6-3
L6	-	I/FO		MC4-6
M6	-	I/FO		MC4-8
N6	49	I/FO		MC1-4
P6	50	I/O		MC6-4
R5	51		**GND**	
M7	52	I/FO		MC4-7
M9	53	I/FO		MC4-9
P7	54	I/FO		MC1-5
N7	55	I/O		MC6-5
R6	56	I/FO		MC1-6
R7	57	I/O/FI		MC6-7
P8	58	I/FO		MC1-7
R8	59	I/FO		MC1-8
N8	60	I/FO		MC1-9
N9	61		V_{CCIO}	
M10	-	O		MC13-1
L10	-	O		MC13-2
R9	62	I/O		MC12-1
R10	63	I/O		MC12-2
P9	64	I/O		MC12-3
L11	65	O		MC13-6
M11	66	I/O/FI		MC13-7
M12	-		**GND**	
P10	67	I/O		MC6-6
N10	68	I/O		MC12-6
R11	69	I/O/FI		MC6-8
P11	70		**GND**	
R12	71	I/O/FI		MC12-7
R13	72	I/O/FI		MC6-9
P12	73	I/O/FI		MC12-8
N11	74	I/O		MC5-1
P13	75	I/O/FI		MC12-9
R14	76	I/O		MC5-2
N12	77	I/O		MC11-1
N13	78	I/O		MC5-3
P14	79	I/O		MC11-2
R15	80		**GND**	

XC73144 Pinouts (continued)

BG225	PQ160	Input	XC73144	Output
M13	81		V_{CCIO}	
L12	-	O		MC13-3
K12	-	O		MC13-4
N14	82	I/O		MC11-3
K11	-	O		MC13-5
J12	83	I/O/FI		MC13-8
P15	84	I/O		MC5-4
G12	85	I/O/FI		MC13-9
M14	86	I/O		MC12-4
L13	87	I/O		MC5-5
N15	88	I/O		MC12-5
L14	89	I/O		MC5-6
M15	90	I/O		MC11-4
K13	91	I/O/FI		MC5-7
K14	92	I/O		MC11-5
L15	93	I/O/FI		MC5-8
J14	94		V_{CCINT}	
J13	95	I/O		MC11-6
K15	96	I/O/FI		MC5-9
J15	97	I/O/FI		MC11-7
H14	98	I/O/FI		MC11-8
H15	99		**GND**	
H13	100		**GND**	
F11	-		V_{CCINT}	
G13	101	I/O		MC11-9
G15	102	I/O		MC10-1
F15	103	I/O		MC10-2
G14	104	I/O		MC10-3
F14	105	I/O		MC16-1
F13	106	I/O		MC10-4
E15	107	I/O		MC16-2
E14	108	I/O		MC10-5
D15	109	I/O		MC16-3
C15	110		**GND**	
D14	111	I/O		MC10-6
E13	112	I/O		MC16-4
C14	113	I/O		MC9-5
B15	114	I/O		MC16-5
D13	115	I/O		MC9-4
C13	116	I/OFI		MC16-9
F12	-	O		MC8-1
E12	-	O		MC8-2
B14	117	I/O/FI		MC10-7
E11	118	O		MC8-6
D12	119	I/O/FI		MC8-7
A15	120		**GND**	

BG225	PQ160	Input	XC73144	Output
C12	121		V_{CCIO}	
B13	122	I/O/FI		MC10-8
A14	123	I/O		MC16-6
B12	124	I/O/FI		MC10-9
C11	125	I/O/FI		MC16-7
A13	126	I/O		MC9-1
D11	-	O		MC8-3
B11	127		**GND**	
A12	128	I/O/FI		MC16-8
E10	-	O		MC8-4
D10	-	O		MC8-5
C10	129	I/O/FI		MC15-7
B10	130	I/O		MC15-1
D9	131	I/O/FI		MC8-8
D7	132	I/O/FI		MC8-9
A11	133	I/O/FI		MC15-8
B9	134	I/O		MC9-2
C9	135	I/O		MC9-6
A10	136	I/O		MC9-3
A9	137		**GND**	
B8	138	I/O/FI		MC9-7
A8	139	I/O/FI		MC9-8
C8	140	I/O/FI		MC9-9
C7	141		V_{CCIO}	
A7	142	I/FO		MC2-9
A6	143	I/FO		MC2-8
B7	144	I/FO		MC2-7
B6	145	I/O/FI		MC15-9
C6	146	I/FO		MC2-6
D6	-	I/FO		MC3-8
E6	-	I/FO		MC3-6
A5	147	I/O		MC15-2
B5	148	I/FO		MC2-5
D5	149	I/FO		MC3-9
E5	150	I/FO		MC3-7
A4	151	I/O		MC15-3
A3	152	I/FO		MC2-4
B4	153	I/O		MC15-4
C5	154	I/FO		MC2-3
D4	-		**GND**	
B3	155	I/O		MC15-5
A2	156	I/FO		MC2-2
C4	157		V_{CCINT}	
C3	158	I/O		MC15-6
B2	159	O/CKEN0		MC7-3
A1	160		**GND**	

Ordering Information



Speed Options

-15	15 ns pin-to-pin delay
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay (commercial and industrial only)
-7	7.5 ns pin-to-pin delay (commercial only)

Packaging Options

PQ160	160-Pin Plastic Quad Flat Pack
BG225	225-Pin Plastic Ball-Grid-Array

Temperature Options

C	Commercial 0°C to 70°C
I	Industrial -40°C to 85°C

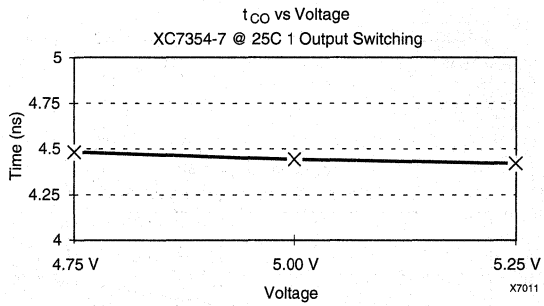
Component Availability

Pins		160	225
Type		Plastic PQFP	Plastic BGA
Code		PQ160	BG225
XC73144	–15	CI	CI
	–12	CI	CI
	–10	C	C
	–7	C	C

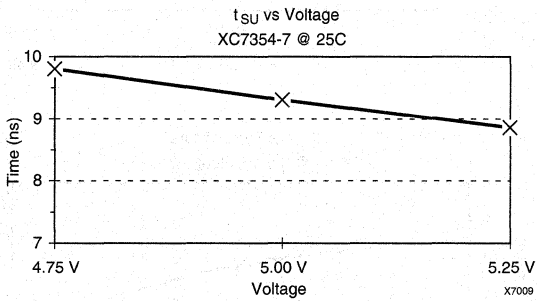
C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C

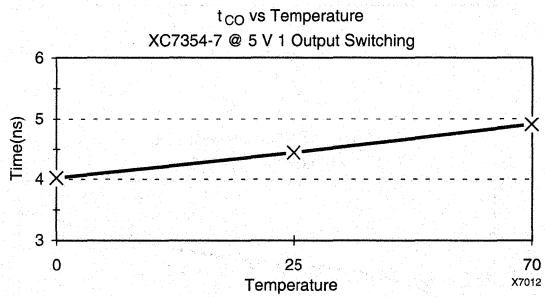
The following section includes typical characterization data for the XC7354, XC7372 and XC73108. Frequently consulted timing parameters were characterized under variations in temperature, voltage and number of simultaneously switching outputs. As demonstrated by the graphical data presented, all products are well within published data sheet limits for commercial temperature and voltage ranges.

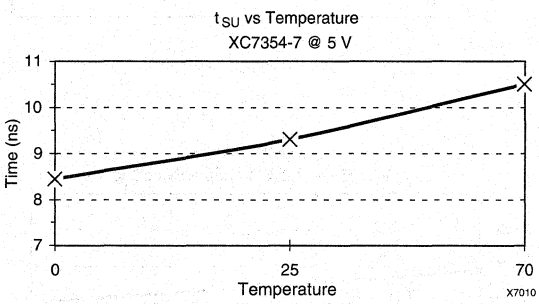
Though this set of characterization data does not include explicit information on the XC7318, XC7336 and XC73144, all XC7300 products are designed using the same circuit configurations, design rules and process technology. Therefore, the XC7318, XC7336 and XC73144 timing parameters are also safely guardbanded with respect to their published data sheet limits.

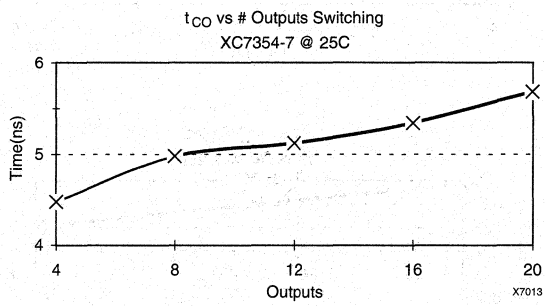


XC7354



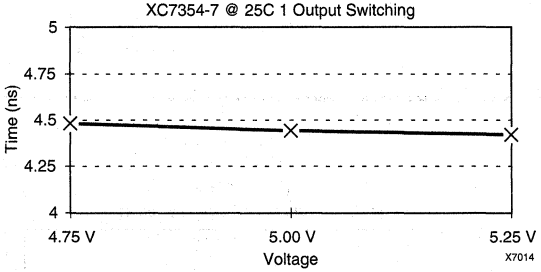




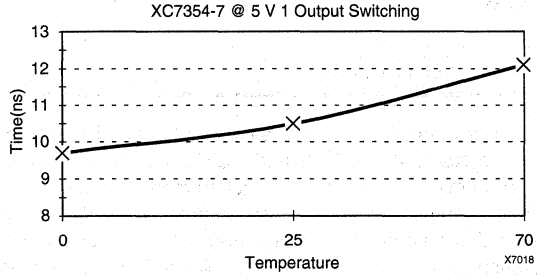


XC7354 (continued)

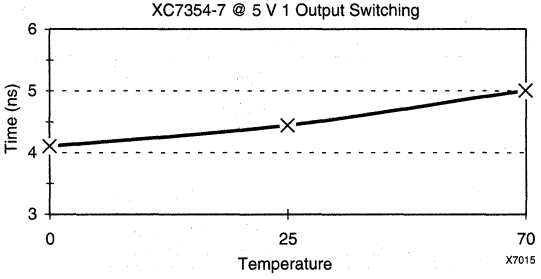
t_{COF} vs Voltage
XC7354-7 @ 25C 1 Output Switching



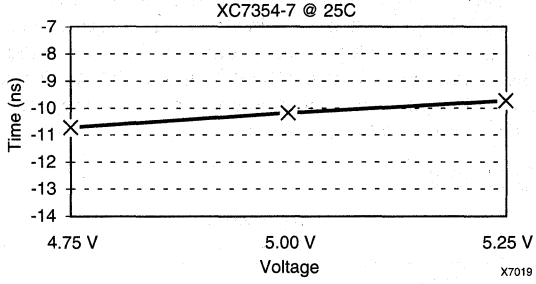
t_{RA} vs Temperature
XC7354-7 @ 5 V 1 Output Switching



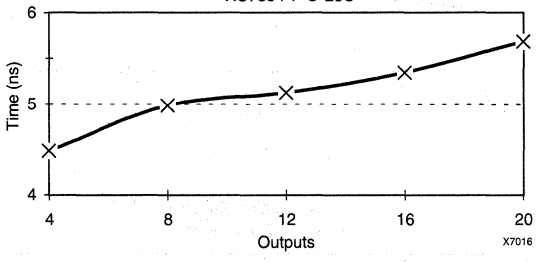
t_{COF} vs Temperature
XC7354-7 @ 5 V 1 Output Switching



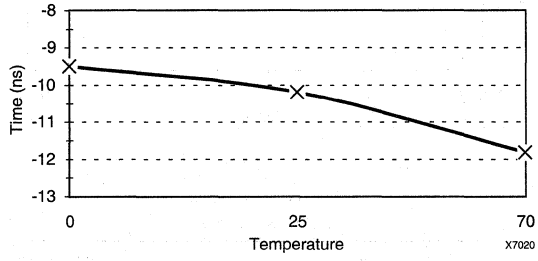
t_{HA} vs Voltage
XC7354-7 @ 25C



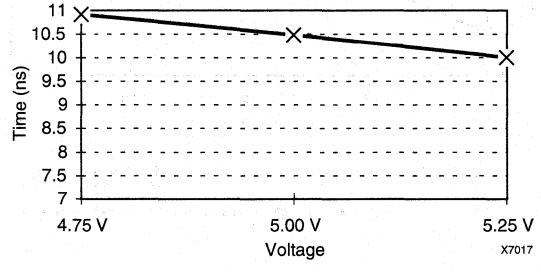
t_{COF} vs # Outputs Switching
XC7354-7 @ 25C



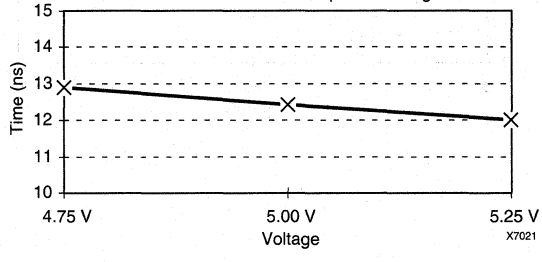
t_{HA} vs Temperature
XC7354 @ 5 V 1 Output Switching



t_{RA} vs Voltage
XC7354-7 @ 25C

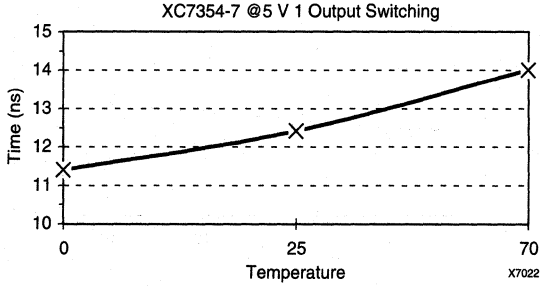


t_{PD} vs Voltage
XC7354-7 @25C 1 Output Switching

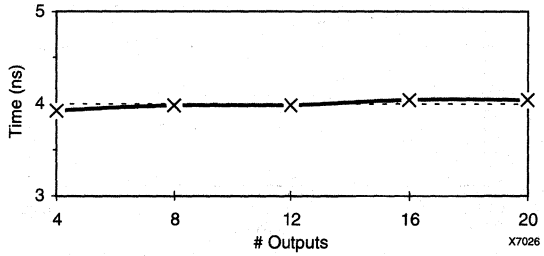


XC7354 (continued)

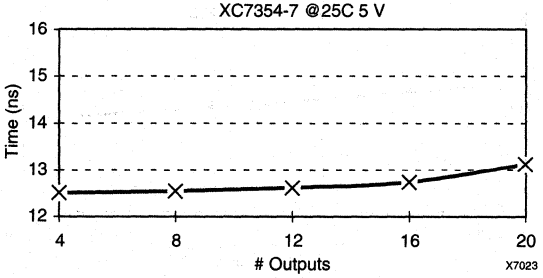
t_{PD} vs Temperature
XC7354-7 @5 V 1 Output Switching



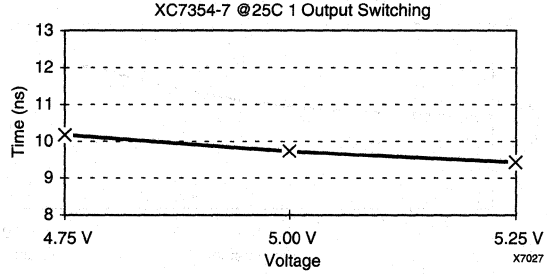
t_{PDFO} vs # Outputs Switching
XC7354-7 @25C 5 V



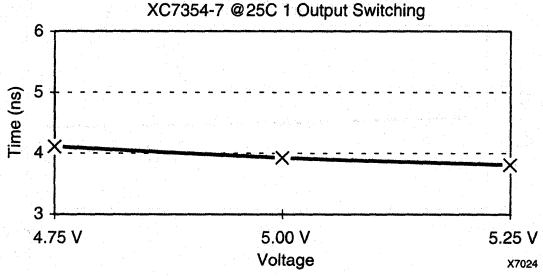
t_{PD} vs # Outputs Switching
XC7354-7 @25C 5 V



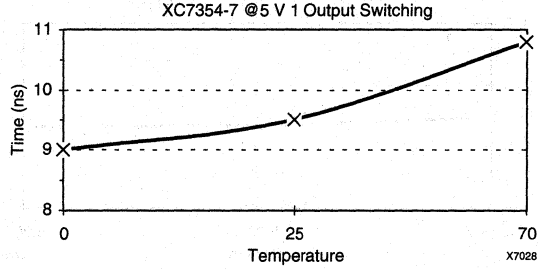
t_{PDFU} vs Voltage
XC7354-7 @25C 1 Output Switching



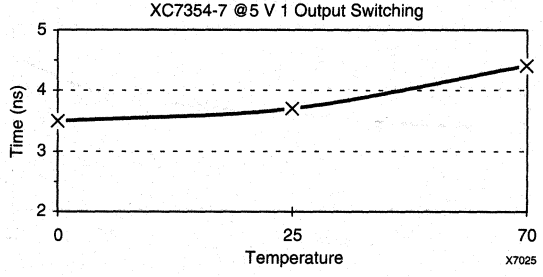
t_{PDFO} vs Voltage
XC7354-7 @25C 1 Output Switching



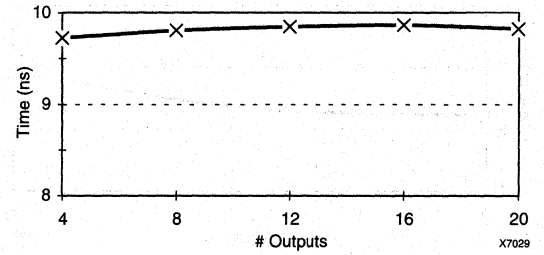
t_{PDFU} vs Temperature
XC7354-7 @5 V 1 Output Switching



t_{PDFO} vs Temperature
XC7354-7 @5 V 1 Output Switching

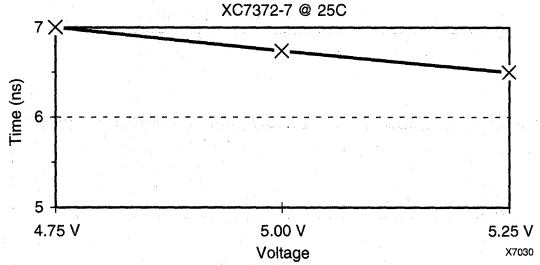


t_{PDFU} vs # Outputs Switching
XC7354-7 @25C 5 V

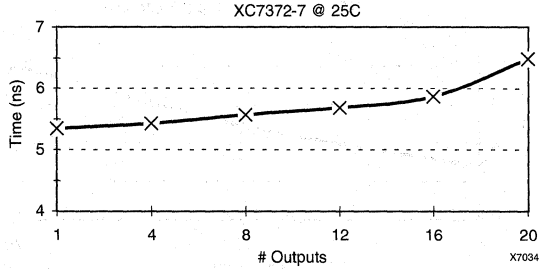


XC7372

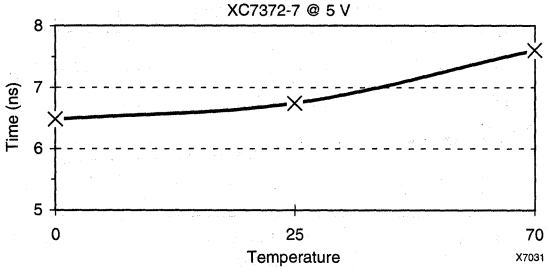
t_{SU} vs Voltage
XC7372-7 @ 25C



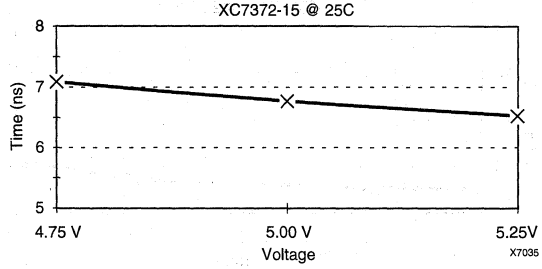
t_{CO} vs #Outputs Switching
XC7372-7 @ 25C



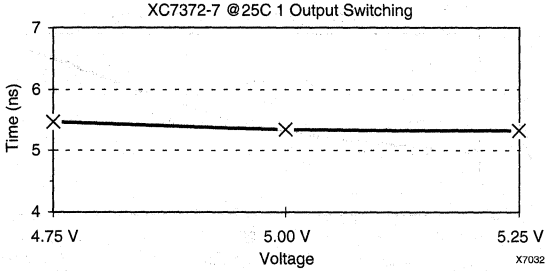
t_{SU} vs Temperature
XC7372-7 @ 5 V



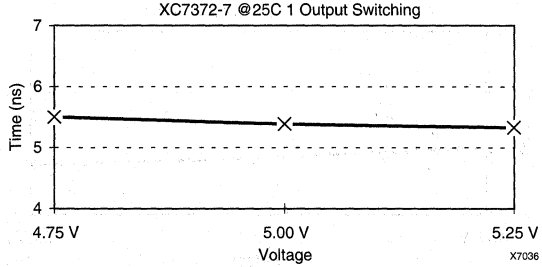
t_{SUF} vs Voltage
XC7372-15 @ 25C



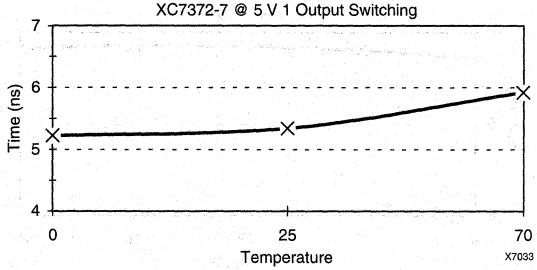
t_{CO} vs Voltage
XC7372-7 @25C 1 Output Switching



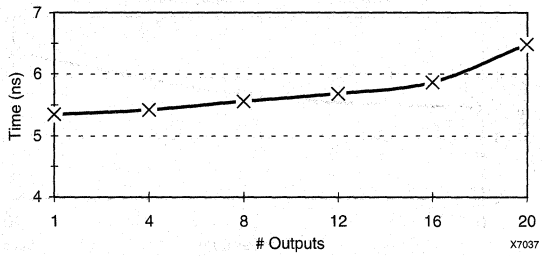
t_{COF} vs Voltage
XC7372-7 @25C 1 Output Switching



t_{CO} vs Temperature
XC7372-7 @ 5 V 1 Output Switching

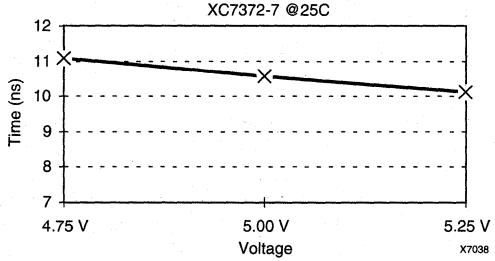


t_{COF} vs #Outputs Switching
XC7372-7 @ 25C

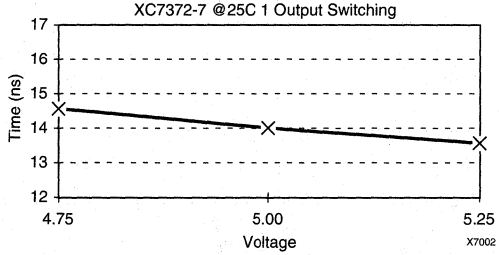


XC7372 (continued)

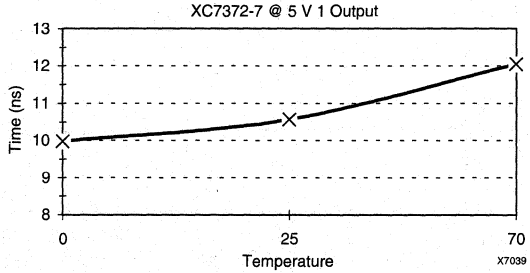
t_{RA} vs Voltage
XC7372-7 @25C



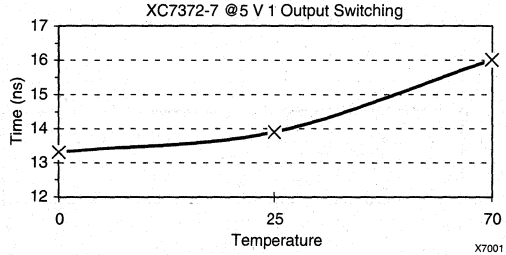
t_{PD} vs Voltage
XC7372-7 @25C 1 Output Switching



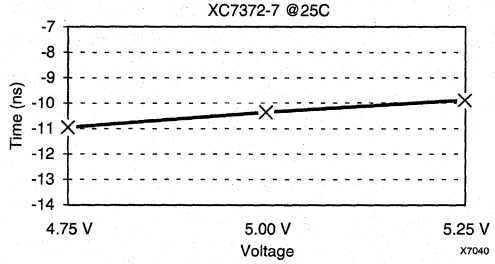
t_{RA} vs Temperature
XC7372-7 @ 5 V 1 Output



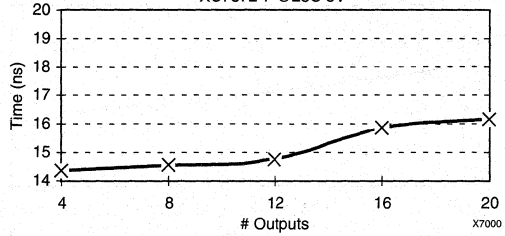
t_{PD} vs Temperature
XC7372-7 @5 V 1 Output Switching



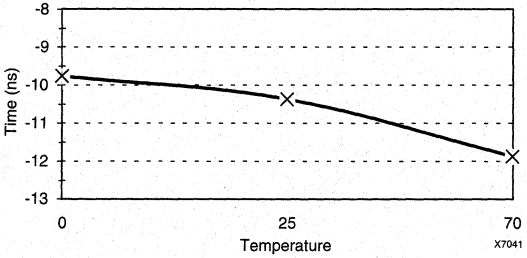
t_{HA} vs Voltage
XC7372-7 @25C



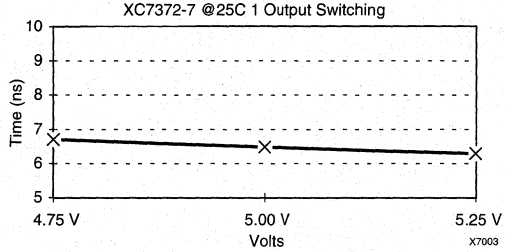
t_{PD} vs # Outputs
XC7372-7 @25C 5V



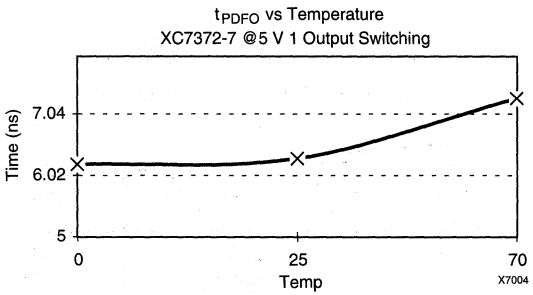
t_{HA} vs Temperature
XC7372-7 @ 5V 1 Output Switching

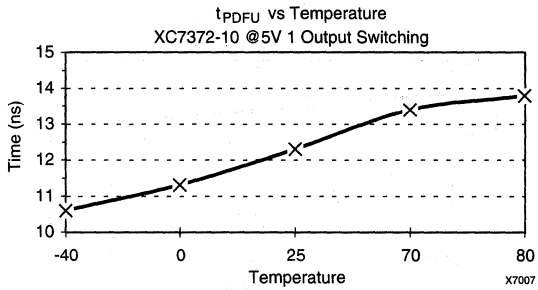


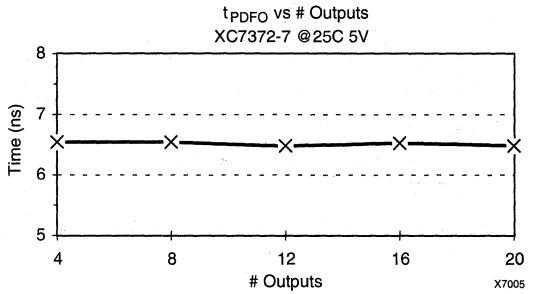
t_{PDFO} vs Voltage
XC7372-7 @25C 1 Output Switching

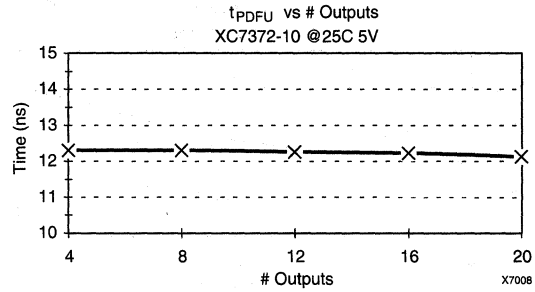


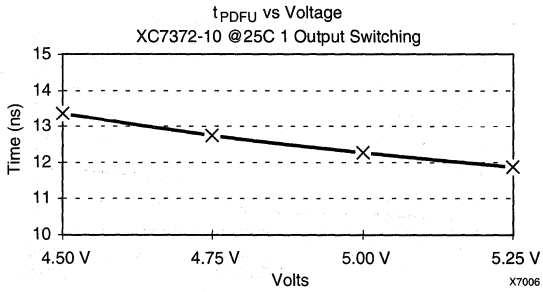
XC7372 (continued)





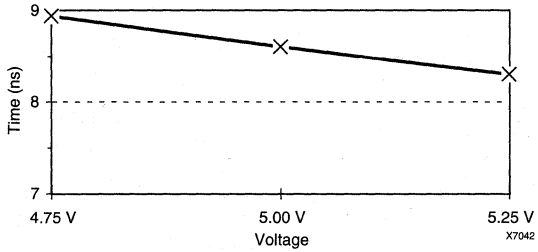




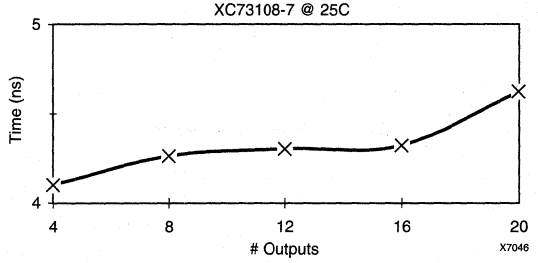


XC73108

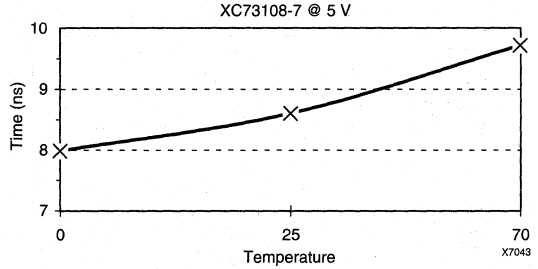
t_{SU} vs Voltage
XC73108-7 @ 25C



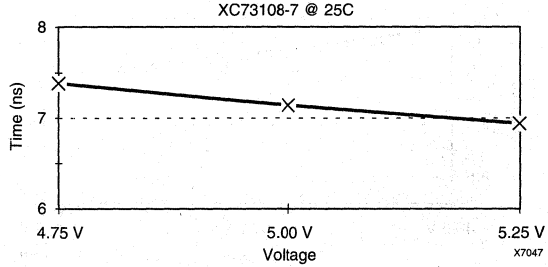
t_{CO} vs #Outputs Switching
XC73108-7 @ 25C



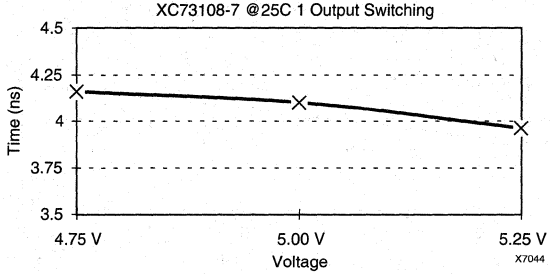
t_{SU} vs Temperature
XC73108-7 @ 5 V



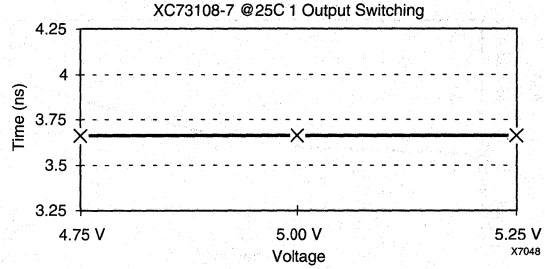
t_{SUF} vs Voltage
XC73108-7 @ 25C



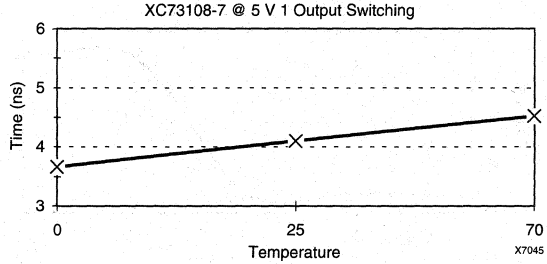
t_{CO} vs Voltage
XC73108-7 @25C 1 Output Switching



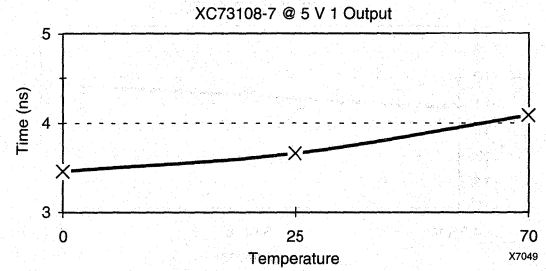
t_{COF} vs Voltage
XC73108-7 @25C 1 Output Switching



t_{CO} vs Temperature
XC73108-7 @ 5 V 1 Output Switching

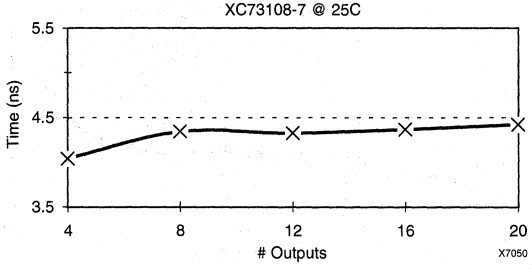


t_{COF} vs Temperature
XC73108-7 @ 5 V 1 Output

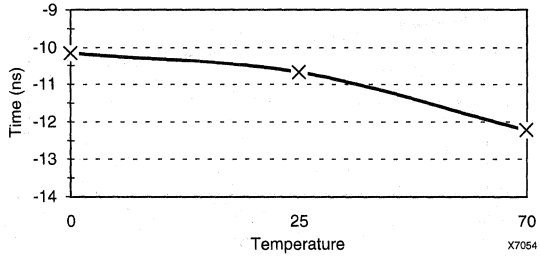


XC73108 (continued)

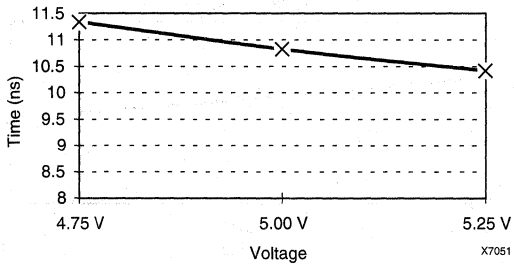
t_{COF} vs #Outputs Switching
XC73108-7 @ 25C



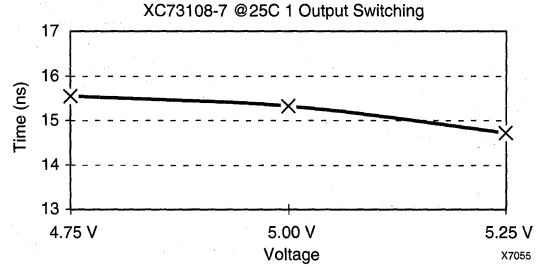
t_{HA} vs Temperature
XC73108-7 @ 5 V 1 Output Switching



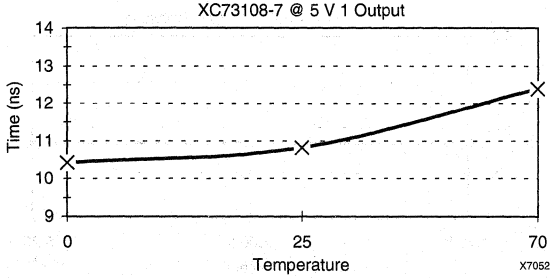
t_{RA} vs Voltage
XC73108-7 @25C



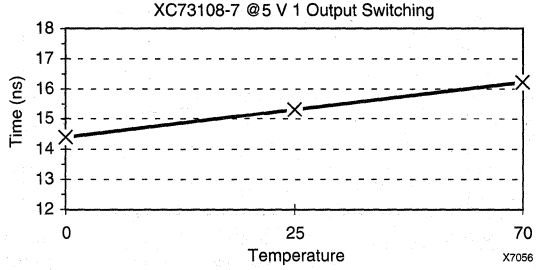
t_{PD} vs Voltage
XC73108-7 @25C 1 Output Switching



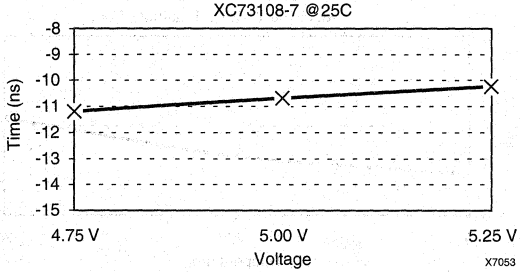
t_{RA} vs Temperature
XC73108-7 @ 5 V 1 Output



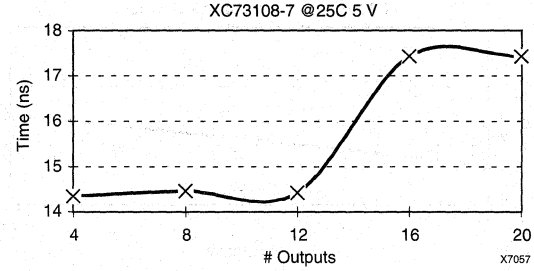
t_{PD} vs Temperature
XC73108-7 @5 V 1 Output Switching



t_{HA} vs Voltage
XC73108-7 @25C

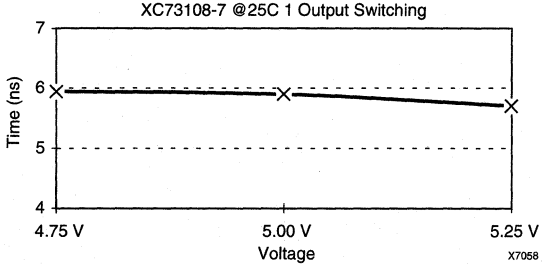


t_{PD} vs # Outputs
XC73108-7 @25C 5 V

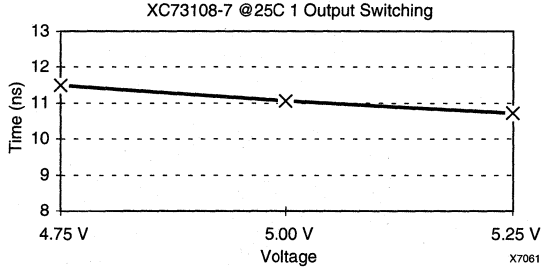


XC73108 (continued)

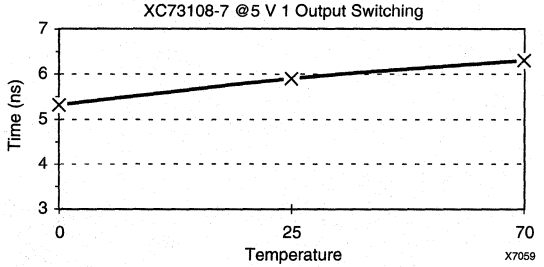
t_{PDFO} vs Voltage
XC73108-7 @25C 1 Output Switching



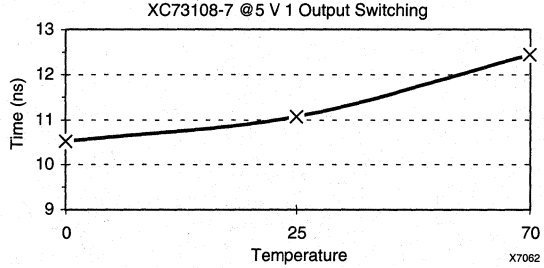
t_{PDFU} vs Voltage
XC73108-7 @25C 1 Output Switching



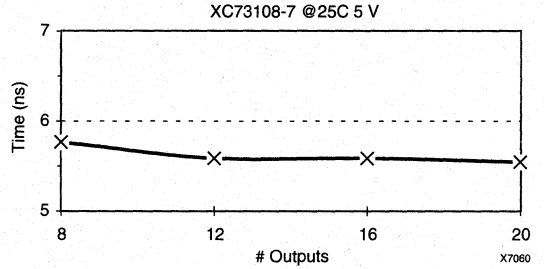
t_{PDFO} vs Temperature
XC73108-7 @5 V 1 Output Switching



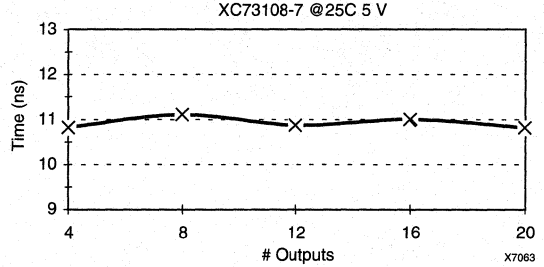
t_{PDFU} vs Temperature
XC73108-7 @5 V 1 Output Switching



t_{PDFO} vs # Outputs
XC73108-7 @25C 5 V



t_{PDFU} vs # Outputs Switching
XC73108-7 @25C 5 V



XC7236A 36-Macrocell CMOS CPLD

XC7272A 72-Macrocell CMOS CPLD

XC7236A
36-Macrocell CMOS CPLD

June 1, 1996 (Version 1.0) | Product Specification

Features

- Second-Generation High Density Programmable Logic Device
- UV-erasable CMOS EPROM technology
- 36 macrocells, grouped into four Function Blocks(FBs), interconnected by a programmable Universal Interconnect Matrix
- Each FB contains a programmable AND-array with 24 complementary inputs, providing up to 17 product terms per macrocell
- Enhanced logic features:
  - 2-input Arithmetic Logic Unit in each macrocell
  - Dedicated fast carry network between macrocells
  - Wide AND capability in the Universal Interconnect Matrix
- Identical timing for all interconnect paths and for all macrocell logic paths
- 36 signal pins
  - 30 I/Os, 2 inputs, 4 outputs
- Each input is programmable
  - Direct, latched, or registered
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ± 0.3 V
- Three high-speed, low-skew global clock inputs
- Available in 44-pin PLCC and CLCC packages

General Description

The XC7236A combines the classical features of the PAL-like CPLD architecture with innovative systems-oriented logic enhancements. This favors the implementation of fast state machines, large synchronous counters and fast arithmetic, as well as multi-level general-purpose logic. Performance, measured in achievable system clock rate and critical delays, is not only predictable, but independent of physical logic mapping, interconnect routing, and resource utilization. Performance, therefore, remains invariant between design iterations. The propagation delay through interconnect and logic is constant for any function implemented in any one of the output macrocells.

The functional versatility of the traditional programmable logic array architecture is enhanced through additional gating and control functions available in an Arithmetic Logic Unit (ALU) in each macrocell. Dedicated fast arithmetic carry lines running directly between adjacent macrocells and FBs support fast adders, subtractors and comparators of any length up to 36 bits.

This additional ALU in each macrocell can generate any combinatorial function of two sums of products, and it can generate and propagate arithmetic-carry signals between adjacent macrocells and FBs.

The Universal Interconnect Matrix (UIM) facilitates unrestricted, fixed-delay interconnects from all device inputs and macrocell outputs to any FB AND-array input. The UIM can also perform a logical AND across any number of its incoming signals on the way to any FB, adding another level of logic without additional delay. This supports bidirectional loadable synchronous counters of any size up to 36 bits, operating at the specified maximum device frequency

As a result of these logic enhancements, the XC7236A can deliver high performance even in designs that combine large numbers of product terms per output, or need more layers of logic than AND-OR, or need a wide AND function in some of the product terms, or perform wide arithmetic functions.

Architectural Overview

Figure 1 shows the XC7236A structure. Four Function Blocks(FBs) are all interconnected by a central UIM. Each FB receives 21 signals from the UIM and each FB produces nine signals back into the UIM. All device inputs are also routed via the UIM to all FBs. Each FB contains nine output macrocells that draw from a programmable AND array driven by the 21 signals from the UIM. Most macrocells drive a 3-state chip output. All feed back into the UIM.

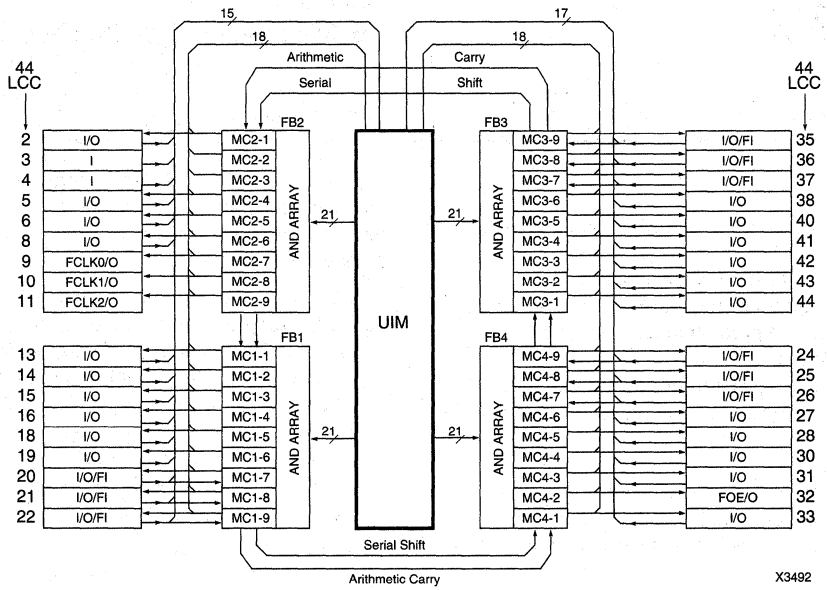


Figure 1: XC7236A Architecture

FBs and macrocells

The XC7236A contains 36 macrocells with identical structure, grouped into four FBs of nine macrocells each. Figure 2 shows the macrocell structure. Each macrocell is driven by product terms derived from a programmable AND array in the FB. The AND array in each FB receives 21 signals and their complements from the UIM. In three FBs, the AND array receives three additional inputs and their complements directly from FastInput (FI) pins, thus offering faster logic paths.

Five product terms are private to each macrocell; an additional 12 product terms are shared among the nine macrocells in each FB. Four of the private product terms can be selectively ORed together with up to four of the shared product terms, and drive the D1 input to the ALU. The other input, D2, to the ALU is driven by the OR of the fifth private product term and up to eight of the remaining shared product terms.

As a programmable option, four of the private product terms can be used for other purposes. One of the private product terms can be used as a dedicated clock for the flip-flop in the macrocell. (See the subsequent description of other clocking options.) Another one of the private product terms can be the asynchronous active-High Reset of the macrocell flip-flop, another one can be the asynchronous active-High Set of the macrocell flip-flop, and another one can be the Output Enable signal.

As a configuration option, the macrocell output can be fed back and ORed into the D2 input to the ALU after being ANDed with three of the shared product terms to implement counters and toggle flip-flops.

The ALU has two programmable modes. In the logic mode, it is a 2-input function generator, a 4-bit look-up table, that can be programmed to generate any Boolean function of its two inputs. It can OR them, widening the OR function to 17 inputs; it can AND them, which means that one sum of products can be used to mask the other; it can XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted and either or both can be ignored. The ALU can implement one additional layer of logic without any speed penalty.

In the arithmetic mode, the ALU block in each macrocell can be programmed to generate the arithmetic sum or difference of two operands, combined with a carry signal coming from the next lower macrocell. It also feeds a carry output to the next higher macrocell. This carry propagation chain crosses the boundaries between FBs. This dedicated carry chain overcomes the inherent speed and density problems of the traditional CPLD architecture when trying to perform arithmetic functions.

The ALU output drives the D input of the macrocell flip-flop. Each flip-flop has several programmable options. One option is to eliminate the flip-flop by making it transparent, which makes the Q output identical with the D input, independent of the clock. Otherwise, the flip-flop operates in the

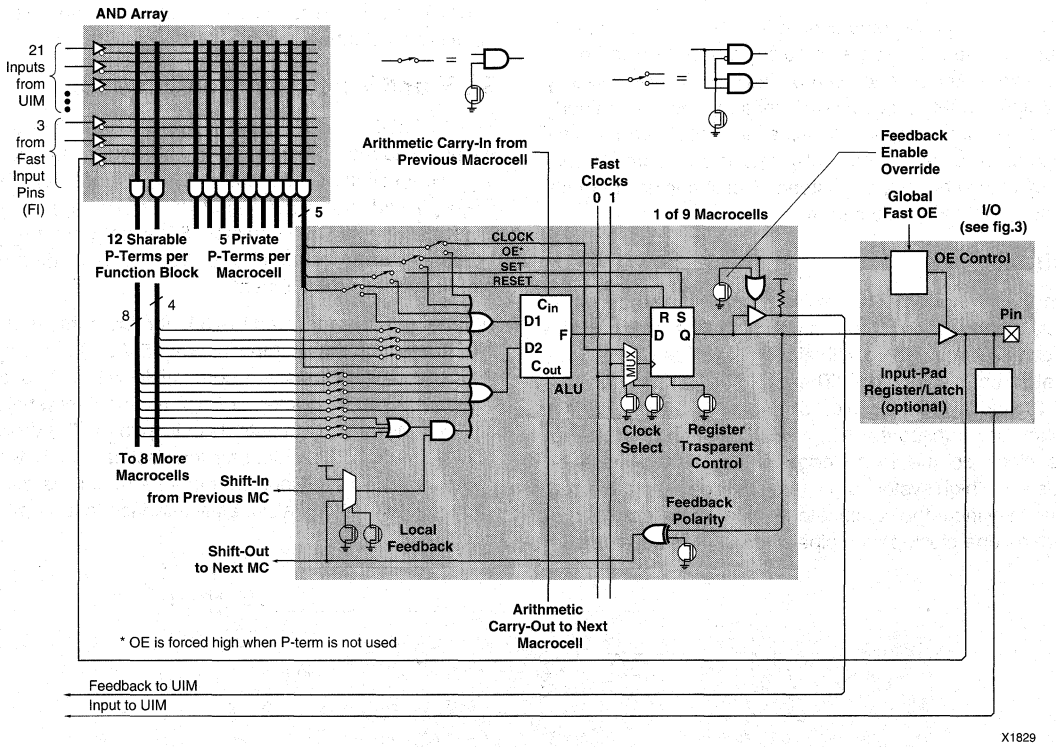


Figure 2: FB and macrocell Schematic

conventional manner, triggered by the rising edge on its clock input.

The clock source is programmable and is either the dedicated product term mentioned earlier, or one of two global FastCLK signals (FLCK0 or FLCK1) that are distributed with short delay and minimal skew over the whole chip.

The asynchronous Set and Reset (Clear) inputs override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set. Upon power-up, each macrocell flip-flop can be preloaded with either 0 or 1.

In addition to driving a chip output pin, the macrocell output is also routed back as an input to the UIM. One private product term can be configured to control the Output Enable of the output pin driver and/or the feedback to the UIM. If configured to control UIM feedback, when the OE product-term is de-asserted, the UIM feedback line is forced High and thus disabled.

Universal Interconnect Matrix

The UIM receives 68 inputs: 36 from the macrocell feedbacks, 30 from bidirectional I/O pins, and 2 from dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 84 output signals, 21 to each FB.

Any one of the 68 inputs can be programmed to be connected to any number of the 84 outputs. The delay through the array is constant, independent of the apparent routing distance, the fan-out, fan-in, or routing complexity.

Routability is not an issue in that any UIM input can drive any UIM output or multiple outputs without additional delay.

When multiple inputs are programmed to be connected to the same output, this output becomes the AND of the input signals if the levels are interpreted as active High. By choosing the appropriate signal inversion at the input pin, macrocell outputs and FB AND-array input, this AND-logic can also be used to implement a NAND, OR, or NOR function. This offers an additional level of logic without any speed penalty.

A macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Several such macrocell outputs programmed onto the same UIM output emulate a 3-state bus line. If one of the macrocell outputs is enabled, the UIM output assumes that same level.

Outputs

Thirty-four of the 36 macrocell drive chip outputs directly through individually programmable inverters followed by 3-state output buffers; each can be individually controlled by the Output Enable product term mentioned above. An additional configuration option disables the output permanently. One dedicated FastOE input also can be configured to control any of the chip outputs instead of, or in conjunction with, the individual OE product term.

Inputs

Each signal input to the chip is programmable as either direct, latched, or registered in a flip flop. The latch and flip-flop can be programmed with either of two FastCLK signals as latch enable or clock. The two FastCLK signals are FCLK0 and a global choice of either FCLK1 or FCLK2. Latches are transparent when FastCLK is High, and flip-flops clock on the rising edge of FastCLK. Registered inputs allow high system clock rates by pipelining the inputs before they incur the combinatorial delay in the device, provided the one-clock-period pipeline latency is acceptable.

The direct, latched, or registered inputs then drive the UIM. There is no propagation-delay difference between pure inputs and I/O inputs.

3.3 V or 5 V Interface configuration

The XC7236A can be used in systems with two different supply voltages, 5 V and 3.3 V. The device has separate V_{CC} connections to the internal logic and input buffers (V_{CCINT}) and to the I/O output drivers (V_{CCIO}). V_{CCINT} is always connected to a nominal +5 V supply, but V_{CCIO} may be connected to either +5 V or +3.3 V, depending on the output interface requirement.

When V_{CCIO} is connected to +5 V, the input thresholds are TTL levels, and thus compatible with 5 V or 3.3 V logic, and the output high levels are compatible with 5 V systems. When V_{CCIO} is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V rail. This makes the XC7236A ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed such that the I/O can also safely interface to a mixed 3.3-V and 5-V bus.

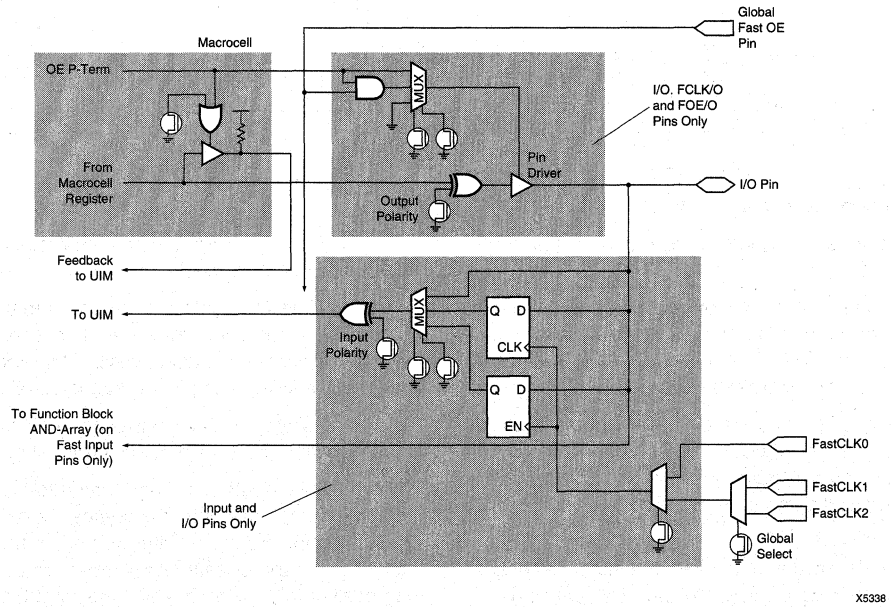


Figure 3: Input/Output Schematic

Programming and Using the XC7236A

The features and capabilities described above are used by the Xilinx development software to program the device according to the specification given either through schematic entry, or through a behavioral description expressed in Boolean equations.

The user can specify a security bit that prevents any reading of the programming bit map after the device has been programmed and verified.

The device is programmed in a manner similar to an EPROM (ultra-violet light erasable read-only memory) using the Intel Hex format. Programming support is available from a number of programmer manufacturers. The UIM connections and FB AND-array connections are made directly by non-volatile EPROM cells. Other control bits are read out of the EPROM array and stored into latches just after power-up. This method, common among EPLD devices, requires application of a master-reset signal delayed at least until V_{CC} has reached the required operating voltage. This can be achieved using a simple capacitor and pull-up resistor on the MR pin (the RC product should be larger than twice the V_{CC} rise time). The power-up or reset signal initiates a self-timed configuration period lasting about 350 µs (t_{RESET}), during which all device outputs remain disabled and programmed preload state values are loaded into the macrocell registers.

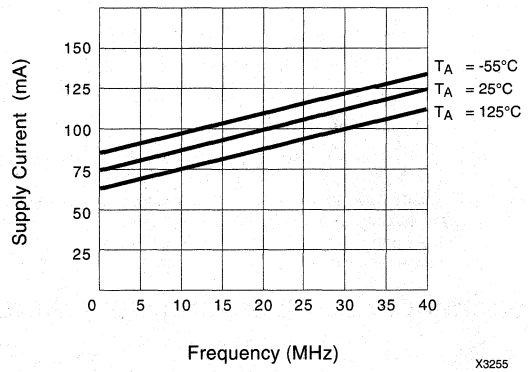


Figure 4: Typical I_{CC} vs. Frequency for XC7236A configured as sixteen 4-bit counters
(V_{CC} = +5.0 V, V_{IN} = V_{CC} or GND, all outputs open)

Unused input and I/O pins should be tied to ground or Vcc or some valid logic level. This is common practice for all CMOS devices to avoid dissipating excess current through the input pad circuitry.

The recommended decoupling capacitance on the three V_{CC} pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}/ V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_A = –55°C to T_C + 125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage 3.3 V	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 24 mA V_{CC} = Min		0.4	V
I_{CC}	Supply current	V_{IN} = 0 V V_{CC} = Max f = 0 MHz	126 Typ		mA
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}	-10	+10	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}	-100	+100	µA
C_{IN}	Input capacitance (sample tested)	V_{IN} = GND f = 1.0 MHz		10	pF

AC Timing Requirements

Symbol	Parameter	Fig.	XC7236A-25		XC7236A-20		XC7236A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
f_{CYC} (Note 1)	Max sequential toggle frequency (with feedback) using FastCLK	6	40		50		60		MHz
f_{CYC1} (Note 1)	Max sequential toggle frequency (with feedback) using a Product-Term Clock	6	40		50		60		MHz
f_{CYC4} (Note 2)	Max macrocell toggle frequency using local feedback and FastCLK		50		50		60		MHz
f_{CLK} (Note 2)	Max macrocell register transmission frequency (without feedback) using FastCLK		45		50		60		MHz
f_{CLK1} (Note 2)	Max macrocell register transmission frequency (without feedback) using a Product-Term Clock		42		50		60		MHz
f_{CLK2} (Note 2)	Max input register transmission frequency (without feedback) using FastCLK		50		50		60		MHz
f_{CLK3} (Note 1)	Max input register to macrocell register pipeline frequency using FastCLK	7	33		40		60		MHz
t_W	FastCLK pulse width (HIgh/Low)	11	10		8		6		ns
f_{TOG}	Export Control Max. flip-flop toggle rate			50		62		83	MHz
t_{W1}	Product-term clock pulse width (active/inactive)	11	12		9		7		ns
t_{SU}	Input to macrocell register set-up time before FastCLK	9	29		24		18		ns
t_H	Input to macrocell register hold time after FastCLK	9	-7		-4		-4		ns
t_{SU1} (Note 1)	Input to macrocell register set-up time before Product-term clock	8	16		14		10		ns
t_{H1}	Input to macrocell register hold time after Product-term clock	8	0		0		0		ns
t_{SU2}	Input to register/latch set-up time before FastLCK	10	8		8		6		ns
t_{H2}	Input to register/latch hold time after FastLCK	10	0		0		0		ns
t_{SU5}	FastInput to macrocell register set-up time before FastCLK		20		18		15		ns
t_{H5}	FastInput to macrocell register hold time after FastCLK		0		0		0		ns
t_{WA}	Set/Reset pulse width (active)	11	12		12		10		ns
t_{RA}	Set/Reset input recovery set-up time before FastCLK	11	30		25		20		ns
t_{HA}	Set/Reset input hold time after FastCLK	11	-5		0		0		ns
t_{RA1}	Set/Reset input recovery set-up time before Product-term clock	11	15		15		12		ns
t_{HA1}	Set/Reset input hold time after Product-term clock	11	9		9		8		ns
t_{HRS}	Product-term clock width (active/inactive)		10		10		8		ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms and the ALU.
2. Not tested but derived from appropriate pulse-widths, set-up time and hold-time measurements.

Propagation Delays

Symbol	Parameter	Fig.	XC7236A-25		XC7236A-20		XC7236A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
t_{CO}	FastCLK input to registered output delay	11	5	14	3	13	3	10	ns
t_{CO1}	P-term clock input to registered output delay	11	10	30	5	24	5	20	ns
t_{AO}	Set/Reset input to registered output delay	11	10	40	5	32	5	25	ns
t_{PD} (Note 1)	Input to non-registered output delay	11	10	40	5	32	5	25	ns
t_{OE}	Input to output enable	11	10	32	5	25	5	20	ns
t_{OD}	Input to output disable	11	10	32	5	25	5	20	ns
t_{PD5}	FastInput to non-registered macrocell output delay		10	31	5	25	5	20	ns
t_{OE5}	FastInput to output enable		5	23	3	20	3	15	ns
t_{OD5}	FastInput to output disable		5	23	3	20	3	15	ns
t_{FOE}	FOE input to output enable		5	15	3	14	3	12	ns
t_{FOD}	FOD input to output disable		5	15	3	14	3	12	ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms and the ALU.

Incremental Parameters

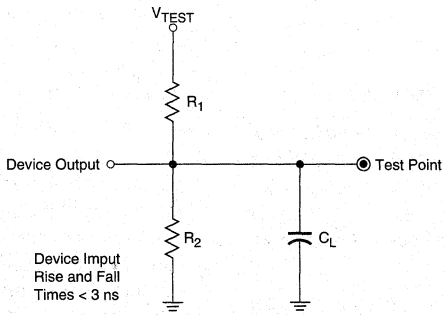
Symbol	Parameter	Fig.	XC7236A-25		XC7236A-20		XC7236A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
t_{PDT1} (Note 2)	Arithmetic carry delay between adjacent macrocells	12		1.2		1.2		1	ns
t_{PDT8} (Note 2)	Arithmetic carry delay through 9 adjacent macrocells in a FB	12		6		5		3	ns
t_{PDT9} (Note 2)	Arithmetic carry delay through 10 macrocells from macrocell #n to macrocell #n in next FB	12		9		6		4	ns
t_{COF1}	Incremental delay from UIM-input (for P-term clock) to registered macrocell feedback	13		12		7		5	ns
t_{COF2} (Note 3)	Incremental delay from FastCLK net to latched/registered UIM-input	13		1		1		1	ns
t_{PDF} (Note 1)	Incremental delay from UIM-input to non-registered macrocell feedback	13		22		14		10	ns
t_{AOF}	Incremental delay from UIM-input (Set/Reset) to registered macrocell feedback	13		22		14		10	ns
t_{OEF} t_{ODF}	Incremental delay from UIM-input (used as output-enable/disable) to macrocell feedback	13		14		7		5	ns
$t_{IN} + t_{OUT}$ (Note 4)	Propagation delay through unregistered input pad (to UIM) plus output pad driver (from macrocell)	13		18		18		15	ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms and the ALU.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for an adder with registered outputs.
3. Parameter t_{COF2} is derived as the difference between the clock period for pipelining input-to-macrocell registers ($1/f_{CLK3}$) and the non-registered input set-up time (t_{SU}).
4. Parameter t_{IN} represents the delay from an input or I/O pin to a UIM-input (or from a FastCLK pin to the Fast CLK net); t_{OUT} represents the delay from a macrocell output (feedback point) to an output or I/O pin. Only the sum of $t_{IN} + t_{OUT}$ can be derived from measurements, e.g., $t_{IN} + t_{OUT} = t_{SU} + t_{CO} - 1/f_{CYC}$.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{rVCC}	V_{CC} rise time (if MR not used for power-up)			5	µs
t_{RESET}	Configuration completion time (to outputs operational)		350	1000	µs

Note: Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, V_{CC} rise *must be* monotonic. Following reset, the Clock, Reset and Set inputs must not be asserted until all applicable input and feedback set-up times are met.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
O	5.0 V	5.0 V	310 Ω	195 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3489

Figure 5: AC Load Circuit

Timing and Delay Path Specifications

The delay path consists of three blocks that can be connected in series:

- Input Buffer and associated latch or register
- Logic Resource (UIM, AND-array and macrocell)
- Three-state Output Buffer

All inputs have the same delay, regardless of fan-out or location. All logic resources have the same delay, regardless of logic complexity, interconnect topology or location on the chip. All outputs have the same delay. The achievable clock rate is, therefore, determined only by the input method (direct, latched or registered) and the number of times a signal passes through the combinatorial logic.

Timing and Delay Path Descriptions

Figure 6 defines the maximum clock frequency (with feedback). Any macrocell output can be fed back to the UIM as an input for the next clock cycle. Figure 6 shows the relevant delay path. The parameters f_{CYC} and f_{CYC1} specify the maximum operating frequency for FastCLK and product-term clock operation respectively.

Figure 7 specifies the max operating frequency (f_{CLK3}) for pipelined operation between the input registers and the macrocell registers, using FastCLK.

Figure 8 defines the set-up and hold times from the data inputs to the product-term clock used by the output register.

Figure 9 defines the set-up and hold times from the data inputs to the FastCLK used by the output register.

Figure 10 defines the set-up and hold times from the data input to the FastCLK used in an input register.

Figure 11 shows the waveforms for the macrocell and control paths

Figure 12 defines the carry propagation delays between macrocells and between FBs. The parameters describe the delay from the C_{IN}, D1 and D2 inputs of a macrocell ALU to the C_{IN} input of the adjacent macrocell ALU. These delays must be added to the standard macrocell delay path (t_{PD} or t_{SU}) to determine the performance of an arithmetic function.

Figure 13 defines the incremental parameters for the standard macrocell logic paths. These incremental parameters are used in conjunction with pin-to-pin parameters when calculating compound logic path timing. Incremental parameters are derived indirectly from other pin-to-pin measurement.

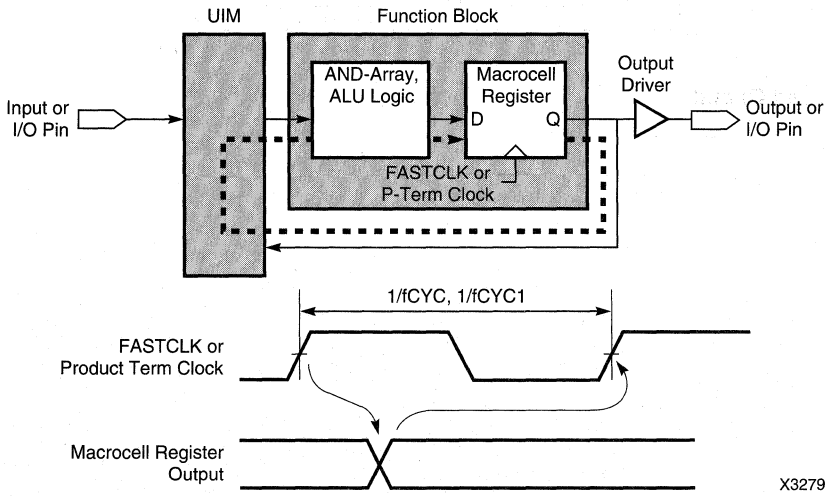


Figure 6: Delay Path Specification for f_{CYC} and f_{CYC1}

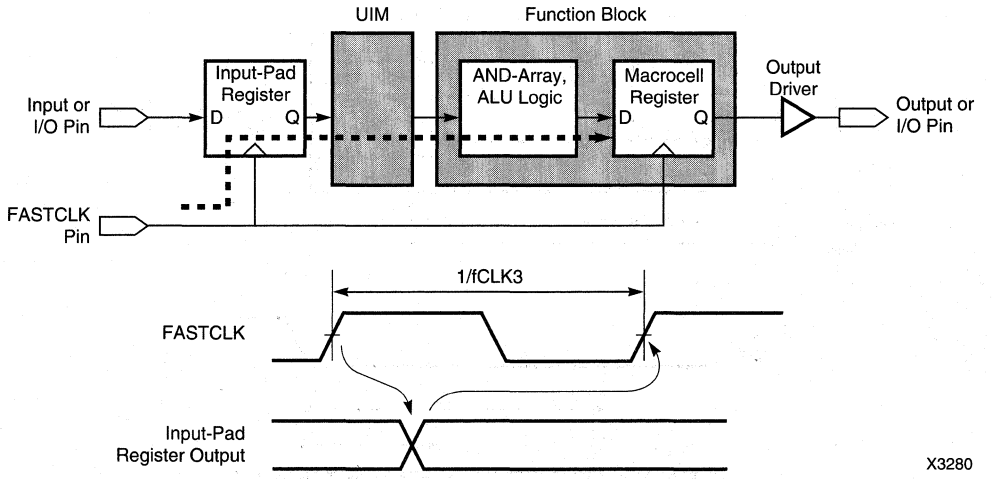


Figure 7: Delay Path Specification for f_{CLK3}

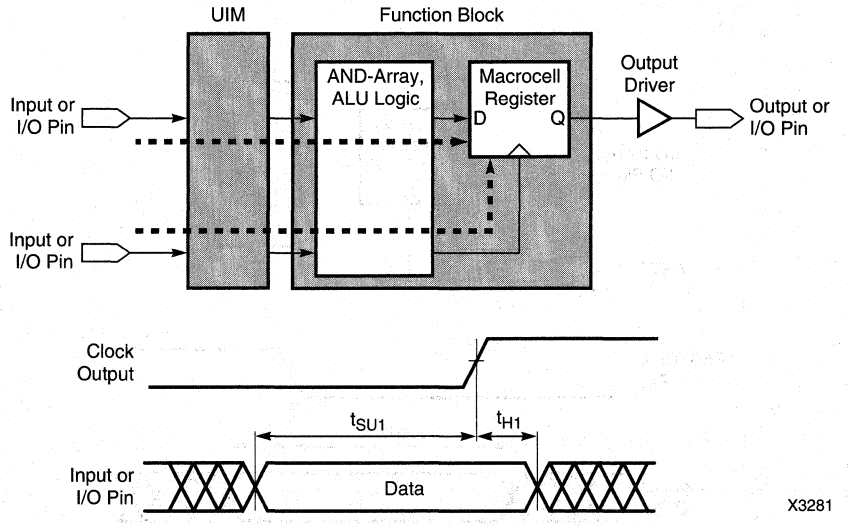


Figure 8: Delay Path Specification for f_{SU1} and f_{H1}

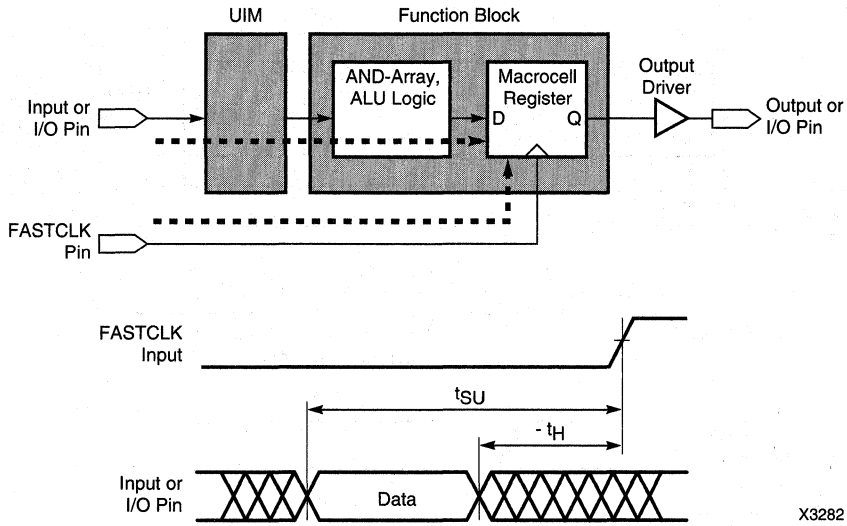


Figure 9: Delay Path Specification for f_{SU} and f_H

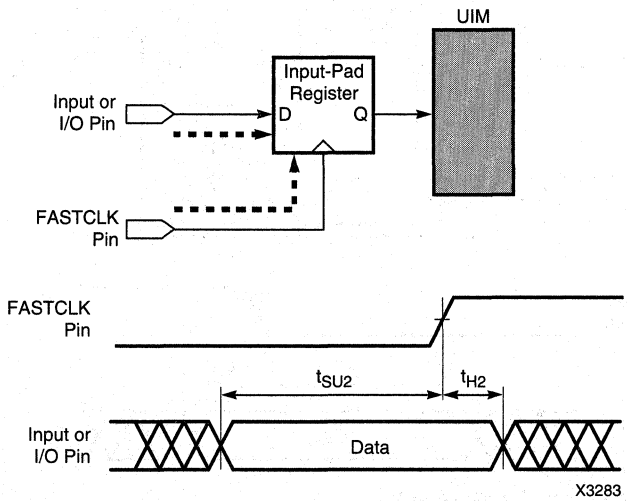


Figure 10: Delay Path Specification for f_{SU2} and f_{H2}

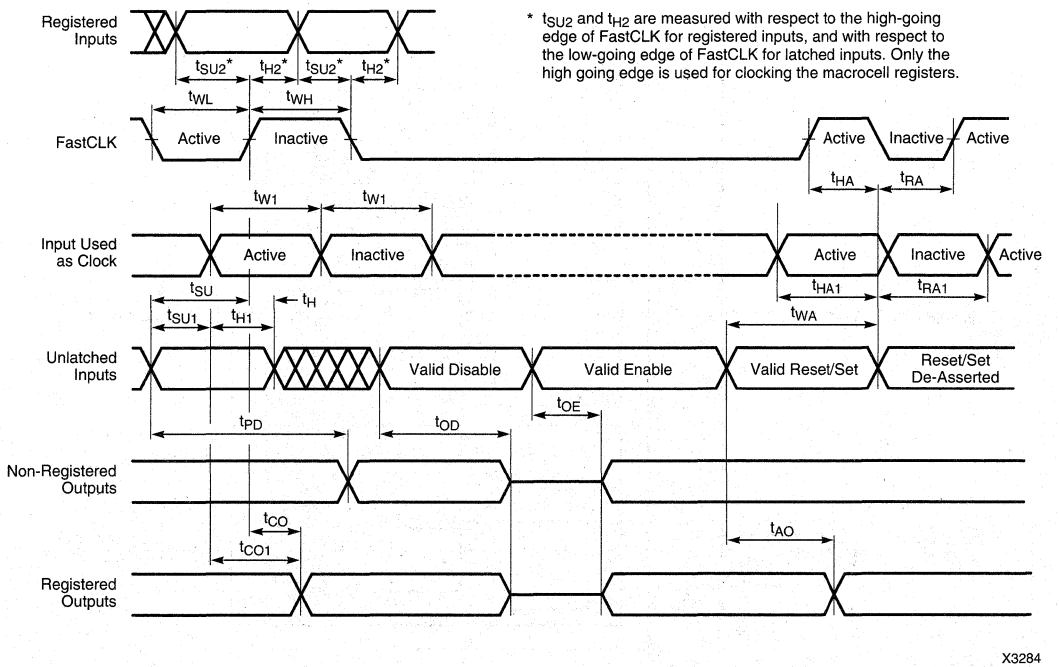


Figure 11: Principal Pin-to-Pin Measurements

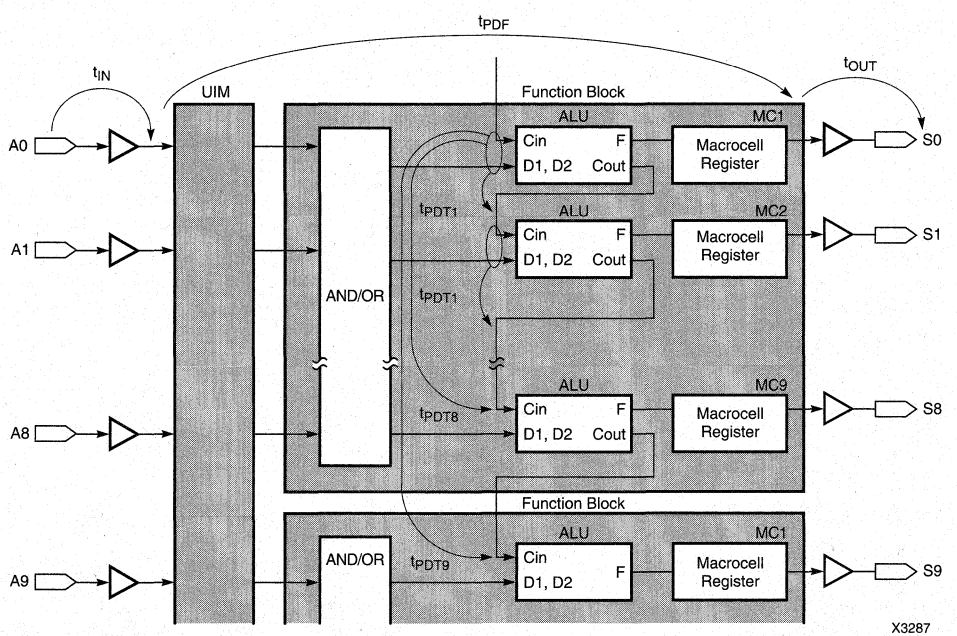


Figure 12: Arithmetic Timing Parameters

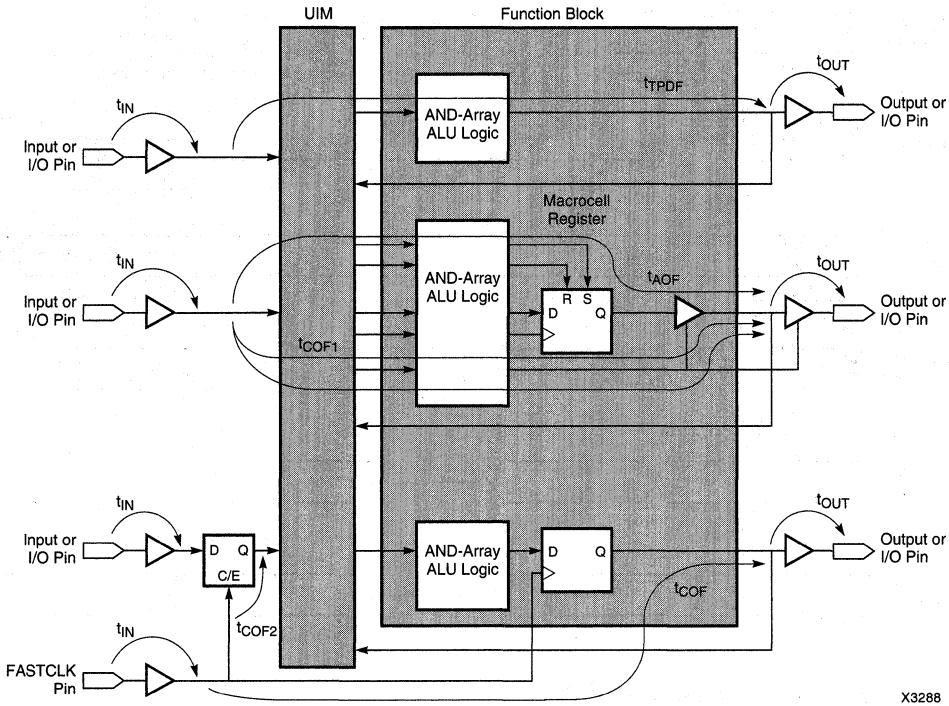


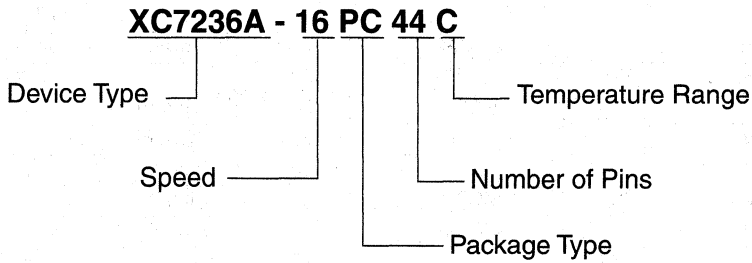
Figure 13: Incremental Timing Parameters

XC7372 Pinouts

Pin #	Input		Output
1	Master Reset	VPP	
2	Input		MC2-1
3	Input		
4	Input		
5	Input		MC2-4
6	Input		MC2-5
7		GND	
8	Input		MC2-6
9	FastCLK0		MC2-7
10	FastCLK1		MC2-8
11	FastCLK2		MC2-9
12		VCCIO	
13	Input		MC1-1
14	Input		MC1-2
15	Input		MC1-3
16	Input		MC1-4
17		GND	
18	Input		MC1-5
19	Input		MC1-6
20	Input/FI		MC1-7
21	Input/FI		MC1-8
22	Input/FI		MC1-9

Pin #	Input		Output
23		VCCIO	
24	Input/FI		MC4-9
25	Input/FI		MC4-8
26	Input/FI		MC4-7
27	Input		MC4-6
28	Input		MC4-5
29		GND	
30	Input		MC4-4
31	Input		MC4-3
32	FastOE		MC4-2
33	Input		MC4-1
34		VCCINT	
35	Input/FI		MC3-9
36	Input/FI		MC3-8
37	Input/FI		MC3-7
38	Input		MC3-6
39		GND	
40	Input		MC3-5
41	Input		MC3-4
42	Input		MC3-3
43	Input		MC3-2
44	Input		MC3-1

Ordering Information



Speed Options

-25	25 ns (40 MHz) sequential cycle time
-20	20 ns (50 MHz) sequential cycle time
-16	16 ns (60 MHz) sequential cycle time (commercial/industrial only)

Packaging Options

PC44	44-Pin Plastic Leaded Chip Carrier
WC44	44-Pin Windowed Ceramic Leaded Chip Carrier

Temperature Options

C	Commercial0°C to 70°C
I	Industrial -40°C to 85°C
M	Military -55°C (Ambient) to 125°C (Case)

Component Availability

Pins		**44**	
Type		**Plastic PLCC**	**Ceramic CLCC**
Code		**PC44**	**WC44**
XC7236A	–25	CI	CIM
	–20	CI	CIM
	–16	CI	CI

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C M = Military = –55°C(A) to 125°C (C)

XC7272A
72-Macrocell CMOS CPLD

June 1, 1996 (Version 1.0) | Product Specification

Features

- Second-Generation High Density Programmable Logic Device
- UV-erasable CMOS EPROM technology
- 72 macrocells, grouped into eight Function Blocks (FBs), interconnected by a programmable Universal Interconnect Matrix
- Each FB contains a programmable AND-array with 21 complementary inputs, providing up to 16 product terms per macrocell
- Enhanced logic features:
  - 2-input Arithmetic Logic Unit in each macrocell
  - Dedicated fast carry network between macrocells
  - Wide AND capability in the Universal Interconnect Matrix
- Identical timing for all interconnect paths and for all macrocell logic paths
- 72 signal pins in the 84-pin packages
  - 42 I/Os, 12 inputs, 18 outputs
- Each input is programmable
  - Direct, latched, or registered
- I/O-pin is usable as input when macrocell is buried
- Two high-speed, low-skew global clock inputs
- Available in 68-pin and 84-pin PLCC/CLCC, 84-pin PGA packages

General Description

The XC7272A combines the classical features of the PAL-like CPLD architecture with innovative systems-oriented logic enhancements. This favors the implementation of fast state machines, large synchronous counters and fast arithmetic, as well as multi-level general-purpose logic. Performance, measured in achievable system clock rate and critical delays, is not only predictable, but independent of physical logic mapping, interconnect routing, and resource utilization. Performance, therefore, remains invariant between design iterations. The propagation delay through interconnect and logic is constant for any function implemented in any one of the output macrocells.

The functional versatility of the traditional programmable logic array architecture is enhanced through additional gating and control functions available in an Arithmetic Logic Unit (ALU) in each macrocell. Dedicated fast arithmetic carry lines running directly between adjacent macrocells and FBs support fast adders, subtractors and comparators of any length up to 72 bits.

This additional ALU in each macrocell can generate any combinatorial function of two sums of products, and it can generate and propagate arithmetic-carry signals between adjacent macrocells and Functional Blocks.

The Universal Interconnect Matrix (UIM) facilitates unrestricted, fixed-delay interconnects from all device inputs and macrocell outputs to any Function Block AND-array input. The UIM can also perform a logical AND across any number of its incoming signals on the way to any Functional Block, adding another level of logic without additional delay. This supports bidirectional loadable synchronous counters of any size up to 72 bits, operating at the specified maximum device frequency

As a result of these logic enhancements, the XC7272A can deliver high performance even in designs that combine large numbers of product terms per output, or need more layers of logic than AND-OR, or need a wide AND function in some of the product terms, or perform wide arithmetic functions.

Architectural Overview

Figure 1 shows the XC7272A structure. Eight Function Blocks(FBs) are all interconnected by a central UIM. Each FB receives 21 signals from the UIM and each FB produces nine signals back into the UIM. All device inputs are also routed via the UIM to all FBs. Each FB contains nine output macrocells that draw from a programmable AND array driven by the 21 signals from the UIM. Most Macro-cells drive a 3-state chip output. All feed back into the UIM.

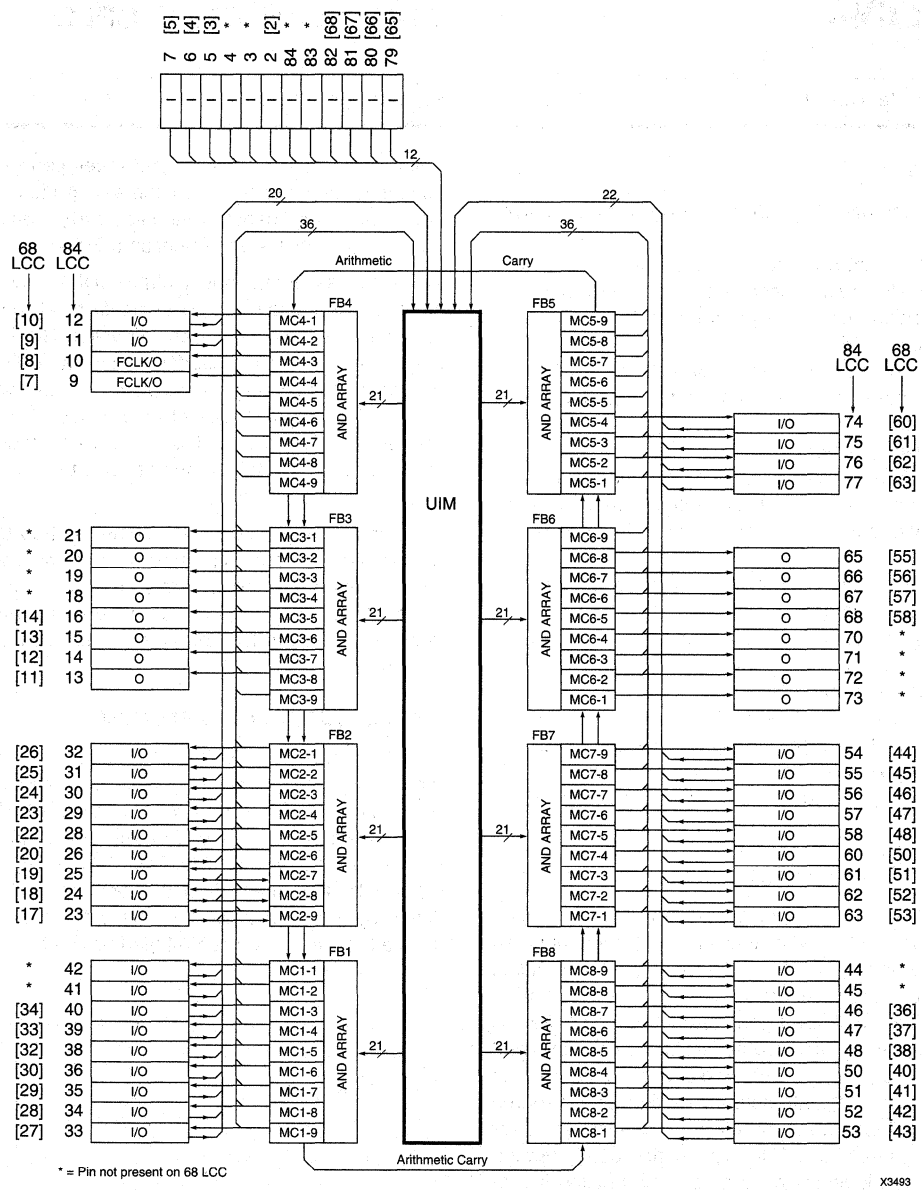


Figure 1: XC7272A Architecture

Function Blocks and Macrocells

The XC7272A contains 72 identical macrocells, grouped into eight FBs of nine macrocells each. Each macrocell is driven by product terms derived from the 21 inputs from the UIM into the Function Block. Figure 2 shows the macrocell structure.

Five product terms are private to each macrocell; an additional 12 product terms are shared among the nine macrocells in any Function Block. One private product term is a dedicated clock for the flip-flop in the macrocell.

The remaining four private product terms can be selectively ORed together with up to three of the shared product terms, to drive one input to an Arithmetic Logic Unit (ALU). The other input to the ALU is driven by the OR of up-to-nine product terms from the remaining shared product terms.

As a programmable option, two of the private product terms can be used for other purposes. One is the asynchronous active-High Reset of the macrocell flip-flop, the other can be either an asynchronous active-High Set of the macrocell flip-flop, or provide an active-High Output-Enable signal from any one of the Function Block inputs.

The ALU has two programmable modes. In the *logic mode,* it is a 2-input function generator, a 4-bit look-up table, that can be programmed to generate any Boolean function of its two inputs. It can OR them, widening the OR function to 16 inputs; it can AND them, which means that one sum of products can be used to mask the other; it can XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted, and either or both can be ignored. The ALU can implement one additional layer of logic without any speed penalty.

In the *arithmetic mode,* the ALU block can be programmed to generate the arithmetic sum or difference of two operands, combined with a carry signal coming from the lower macrocell; it also feeds a carry output to the next higher macrocell. This carry propagation chain crosses the boundaries between FBs, but it can also be configured as a 0 or 1 when it enters a Function Block.

This dedicated carry chain overcomes the inherent speed and density problems of the traditional CPLD architecture, when trying to perform arithmetic functions like add, subtract, and magnitude compare.

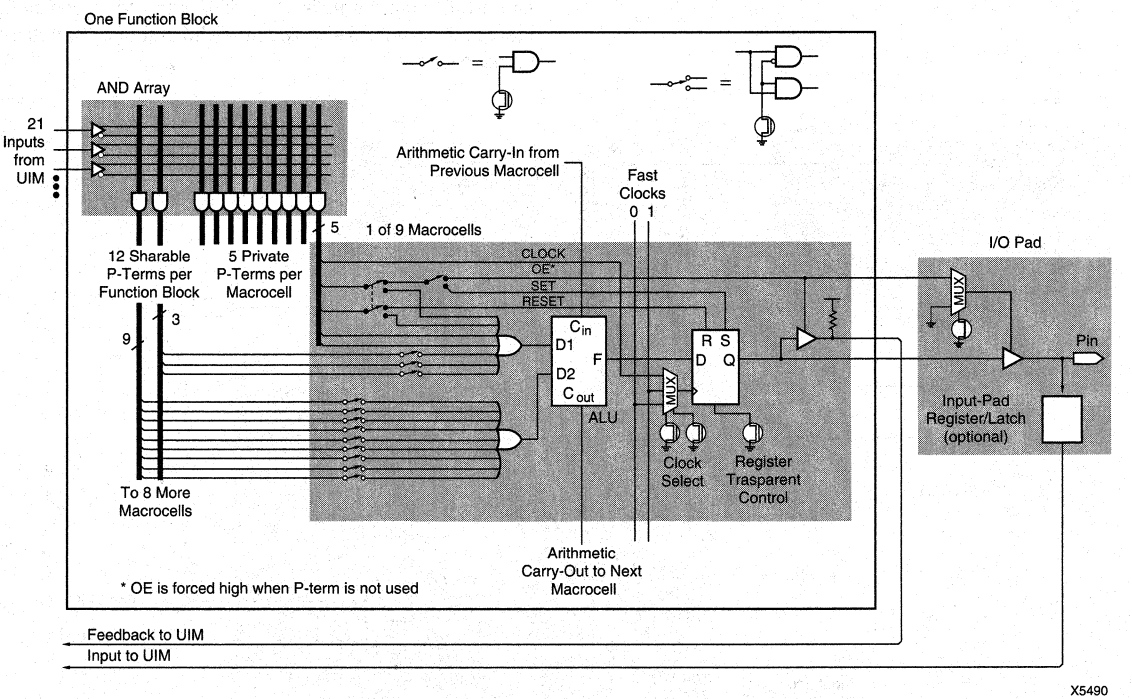


Figure 2: Function Block and Macrocell Schematic

The ALU output drives the D input of the macrocell flip-flop.

Each flip-flop has several programmable options:

One option is to eliminate the flip-flop by making it transparent, which makes the Q output identical with the D input, independent of the clock.

If this option is *not* programmed, the flip-flop operates in the conventional manner, triggered by the rising edge on its clock input.

The clock source is programmable: It is either the dedicated product term mentioned above, or it is one of the two global FastCLK signals that are distributed with short delay and minimal skew over the whole chip.

The asynchronous Set and Reset (Clear) inputs override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set. Upon power-up, each macrocell flip-flop can be preloaded with either 0 or 1.

In addition to driving the chip output buffer, the macrocell output is also routed back as an input to the UIM. When the Output Enable product term mentioned above is not active, this feedback line is forced High and thus disabled.

Universal Interconnect Matrix

The UIM receives 126 inputs: 72 from the 72 macrocells, 42 from bidirectional I/O pins, and 12 from dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 168 output signals, 21 to each Function Block.

Any one of the 126 inputs can be programmed to be connected to any number of the 168 outputs. The delay through the array is constant, independent of the apparent routing distance, the fan-out, fan-in, or routing complexity. Routability is not an issue: Any UIM input can drive any UIM output, even multiple outputs, and the delay is constant.

When multiple inputs are programmed to be connected to the same output, this output becomes the AND of the input signals if the levels are interpreted as active High. By choosing the appropriate signal inversion in the macrocell outputs and the Function Block AND-array input, this AND-logic can also be used to implement a NAND, OR, or NOR function, thus offering an additional level of logic without any speed penalty.

A macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Several such macrocell outputs programmed onto the same UIM output emulate a 3-state bus line. If one of the macrocell outputs is enabled, the UIM output assumes that same level.

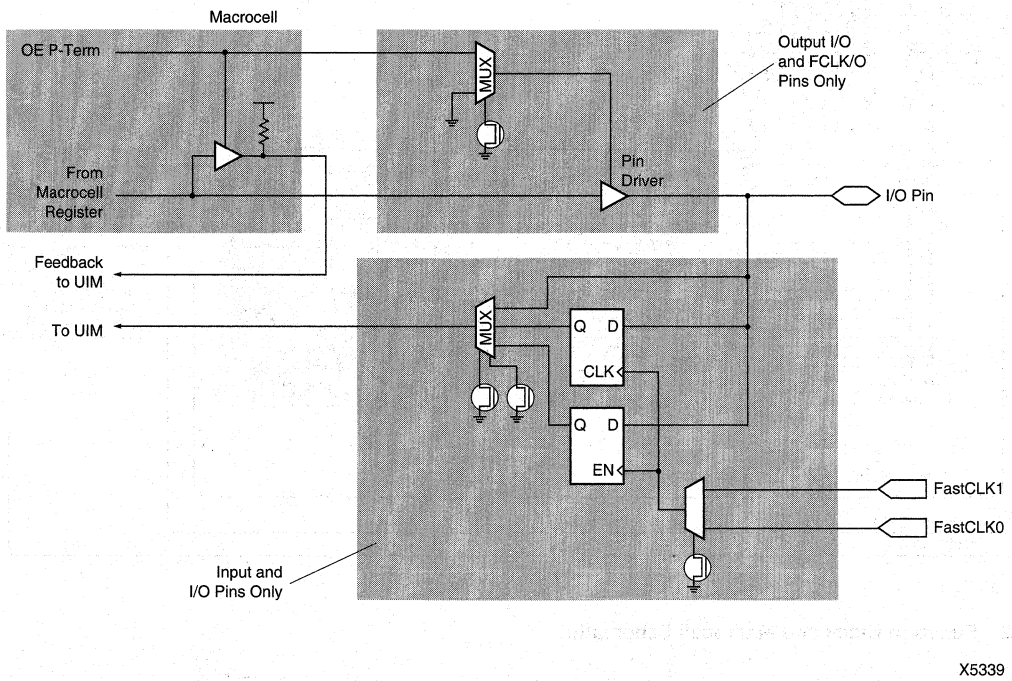


Figure 3: Input/Output Schematic

Outputs

Sixty of the 72 macrocells drive chip outputs directly through 3-state output buffers, each individually controlled by the Output Enable product term mentioned above. For bidirectional I/O pins, an additional programmable cell can optionally disable the output permanently. The buried flip-flop is then still available for internal feedback, and the pin can still be used as a separate input

Inputs

Each signal input to the chip is programmable as either direct, latched, or registered in a flip-flop. The latch and flip-flop can be programmed with either of the two FastCLK signals as latch enable or clock. The latch is transparent when FastCLK is High, and the flip-flop clocks on the rising edge of FastCLK. Registered inputs allow high system clock rates by pipelining the inputs before they incur the combinatorial delay in the device, in cases where a pipeline cycle is acceptable.

The direct, latched, or registered inputs then drive the UIM. There is no propagation-delay difference between pure inputs and I/O inputs.

Programming and Using the XC7272A

The features and capabilities described above are used by the Xilinx XACT*step* development software to program the device according to the specification given either through schematic entry, or through a behavioral description expressed in Boolean equations.

The user can specify a security bit that prevents any reading of the programming bit map after the device has been programmed and verified.

The device is programmed in a manner similar to an EPROM (ultra-violet light erasable read-only memory) using the Intel Hex or JEDEC format. Programming support is available from a number of programmer manufacturers. The UIM connections and Function Block AND-array connections are made directly by non-volatile EPROM cells. Other control bits are read out of the EPROM array and stored into latches just after power-up. This method, common among CPLD devices, requires either a very fast V_{CC} rise time (<5 µs) or the application of a master-reset signal delayed at least until V_{CC} has reached the required operating voltage. The latter can be achieved using a simple capacitor and pull-up resistor on the MR pin (the RC product should be larger than twice the V_{CC} rise time). The power-up or reset signal initiates a self-timed configuration period lasting about 350 µs (t_{RESET}), during which all device outputs remain disabled and programmed preload state values are loaded into the macrocell registers.

Unused input and I/O pins should be tied to ground or Vcc or some valid logic level. This is common practice for all CMOS devices to avoid dissipating excess current through the input-pad circuitry.

The recommended decoupling capacitance on the three V_{CC} pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.

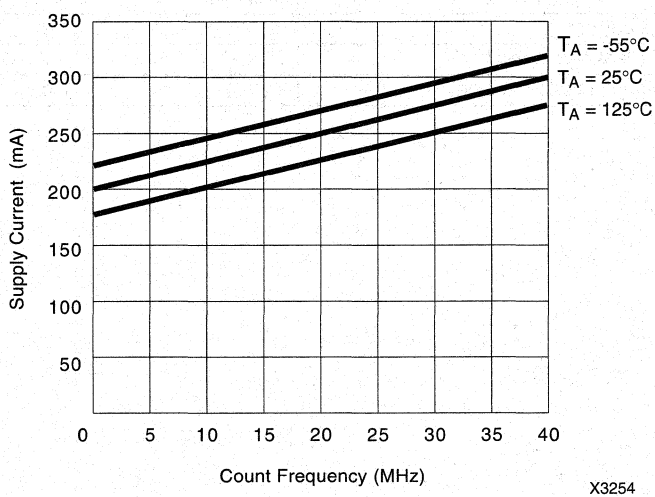


Figure 4: Typical I_{CC} vs. Frequency for XC7272A configured as sixteen 4-bit counters
(V_{CC} = +5.0 V, V_{IN} = V_{CC} or GND, all outputs open)

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to 7.0	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}/ V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_A = –55°C to T_C + 125°C	4.5	5.5	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_{IL}	Low-level input voltage	0	0.8	V

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
V_{OL}	TTL Low-level output voltage	I_{OL} = 8 mA V_{CC} = Min		0.5	V
I_{CC}	Supply current	V_{IN} = 0 V V_{CC} = Max f = 0 MHz	222 Typ		mA
I_{IL}	Input leakage current		-10	+10	µA
I_{OZ}	Output high-Z leakage current		-100	+100	µA
C_{IN}	Input capacitance (sample tested)			10	pF

AC Timing Requirements

Symbol	Parameter	Fig.	XC7272A-25		XC7272A-20		XC7272A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
f_{CYC} (Note 1)	Max sequential toggle frequency (with feedback) using FastCLK		40		50		55		MHz
f_{CYC1} (Note 1)	Max sequential toggle frequency (with feedback) using a Product-Term Clock		40		50		55		MHz
f_{CLK} (Note 2)	Max macrocell register transmission frequency (without feedback) using FastCLK		40		50		55		MHz
f_{CLK1} (Note 2)	Max macrocell register transmission frequency (without feedback) using a Product-Term Clock		40		50		55		MHz
f_{CLK2} (Note 2)	Max input register transmission frequency (without feedback) using FastCLK		67		67		67		MHz
f_{CLK3} (Note 1)	Max input register to macrocell register pipeline frequency using FastCLK	7	40		50		60		MHz
t_{WL}	FastCLK Low pulse width	11	7.5		7.5		6		ns
t_{WH}	FastCLK High pulse width	11	7.5		7.5		6		ns
f_{TOG}	Export Control Max. flip-flop toggle rate			67		67		83	MHz
t_{W1}	Product-term clock pulse width (active/inactive)	11	10		9		7		ns
t_{SU}	Input to macrocell register set-up time before FastCLK	9	24		19		15		ns
t_H	Input to macrocell register hold time after FastCLK	9	-7		-4		-4		ns
t_{SU1} (Note 1)	Input to macrocell register set-up time before Product-term clock	8	10		8		6		ns
t_{H1}	Input to macrocell register hold time after Product-term clock	8	0		0		0		ns
t_{SU2}	Input to register/latch set-up time before FastLCK	10	8		8		6		ns
t_{H2}	Input to register/latch hold time after FastLCK	10	0		0		0		ns
t_{WA}	Set/Reset pulse width	11	12		10		8		ns
t_{RA}	Set/Reset input recovery set-up time before FastCLK	11	20		20		16		ns
t_{HA}	Set/Reset input hold time after FastCLK	11	-5		-3		-3		ns
t_{RA1}	Set/Reset input recovery set-up time before Product-term clock	11	6		5		4		ns
t_{HA1}	Set/Reset input hold time after Product-term clock	11	9		8		6		ns
t_{HRS}	Set/Reset input hold time after Reset/Set inactive		10		8		6		ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms and the ALU.
2. Not tested but derived from appropriate pulse-widths, set-up time and hold-time measurements.

Propagation Delays

Symbol	Parameter	Fig.	XC7272A-25		XC7272A-20		XC7272A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
t_{CO}	FastCLK input to registered output delay	11	5	16	3	14	3	12	ns
t_{CO1}	P-term clock input to registered output delay	11	10	30	6	25	6	21	ns
t_{AO}	Set/Reset input to registered output delay	11	13	40	8	32	8	25	ns
t_{PDD} (Note 1)	Input to non-registered output delay	11	13	40	8	32	8	25	ns
t_{OE}	Input to output enable	11	11	32	7	25	7	22	ns
t_{OD}	Input to output disable		11	32	7	25	7	22	ns

Note: 1. Specifications account for logic paths which use the maximum number of available product terms and the ALU.

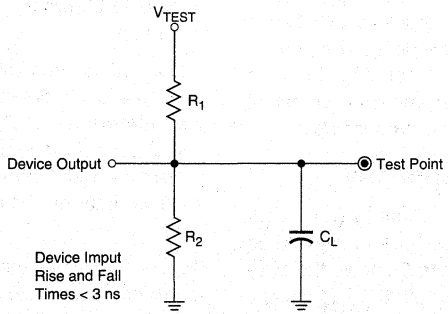
Incremental Parameters

Symbol	Parameter	Fig.	XC7272A-25		XC7272A-20		XC7272A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
t_{PDT1} (Note 2)	Arithmetic carry delay between adjacent macrocells	12		1.6		1.2		1	ns
t_{PDT8} (Note 2)	Arithmetic carry delay through 9 adjacent macrocells in a FB	12		10		8		6	ns
t_{PDT9} (Note 2)	Arithmetic carry delay through 10 macrocells from macrocell #n to macrocell #n in next FB	12		14		12		10	ns
t_{COF}	Incremental delay from FastCLK net to registered output feedback	13		1		1		1	ns
t_{COF1}	Incremental delay from UIM-input (for P-term clock) to registered macrocell feedback	13		1.5		12		10	ns
t_{COF2} (Note 3)	Incremental delay from FastCLK net to latched/registered UIM-input	13		1		1		1	ns
t_{PDF} (Note 1)	Incremental delay from UIM-input to non-registered macrocell feedback	13		25		19		14	ns
t_{AOF}	Incremental delay from UIM-input (Set/Reset) to registered macrocell feedback	13		25		19		14	ns
t_{OEF} t_{ODF}	Incremental delay from UIM-input (used as output-enable/disable) to macrocell feedback	13		17		12		11	ns
$t_{IN} + t_{OUT}$ (Note 4)	Propagation delay through unregistered input pad (to UIM) plus output pad driver (from macrocell)	13		15		13		11	ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms and the ALU.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for an adder with registered outputs.
3. Parameter t_{COF2} is derived as the difference between the clock period for pipelining input-to-macrocell registers ($1/f_{CLK3}$) and the non-registered input set-up time (t_{SU}).
4. Parameter t_{IN} represents the delay from an input or I/O pin to a UIM-input (or from a FastCLK pin to the Fast CLK net); t_{OUT} represents the delay from a macrocell output (feedback point) to an output or I/O pin. Only the sum of $t_{IN} + t_{OUT}$ can be derived from measurements, e.g., $t_{IN} + t_{OUT} = t_{SU} + t_{CO} - 1/f_{CYC}$.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{rVCC}	V_{CC} rise time (if MR not used for power-up)			5	µs
t_{RESET}	Configuration completion time (to outputs operational)		350	1000	µs



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
O	5.0 V	5.0 V	450 Ω	245 Ω	35 pF

X3490

Figure 5: AC Load Circuit

Timing and Delay Path Specifications

The delay path consists of three blocks that can be connected in series:

- Input Buffer and associated latch or register
- Logic Resource (UIM, AND-array and macrocell)
- Three-state Output Buffer

All inputs have the same delay, regardless of fan-out or location. All logic resources have the same delay, regardless of logic complexity, interconnect topology or location on the chip. All outputs have the same delay. The achievable clock rate is, therefore, determined only by the input method (direct, latched or registered) and the number of times a signal passes through the combinatorial logic.

Timing and Delay Path Descriptions

Figure 6 defines the maximum clock frequency (with feedback). Any macrocell output can be fed back to the UIM as an input for the next clock cycle. Figure 6 shows the relevant delay path. The parameters f_{CYC} and f_{CYC1} specify the maximum operating frequency for FastCLK and product-term clock operation respectively.

Figure 7 specifies the max operating frequency (f_{CLK3}) for pipelined operation between the input registers and the macrocell registers, using FastCLK.

Figure 8 defines the set-up and hold times from the data inputs to the product-term clock used by the output register.

Figure 9 defines the set-up and hold times from the data inputs to the FastCLK used by the output register.

Figure 10 defines the set-up and hold times from the data input to the FastCLK used in an input register.

Figure 11 shows the waveforms for the macrocell and control paths

Figure 12 defines the carry propagation delays between macrocells and between FBs. The parameters describe the delay from the C_{IN}, D1 and D2 inputs of a macrocell ALU to the C_{IN} input of the adjacent macrocell ALU. These delays must be added to the standard macrocell delay path (t_{PD} or t_{SU}) to determine the performance of an arithmetic function.

Figure 13 defines the incremental parameters for the standard macrocell logic paths. These incremental parameters are used in conjunction with pin-to-pin parameters when calculating compound logic path timing. Incremental parameters are derived indirectly from other pin-to-pin measurement.

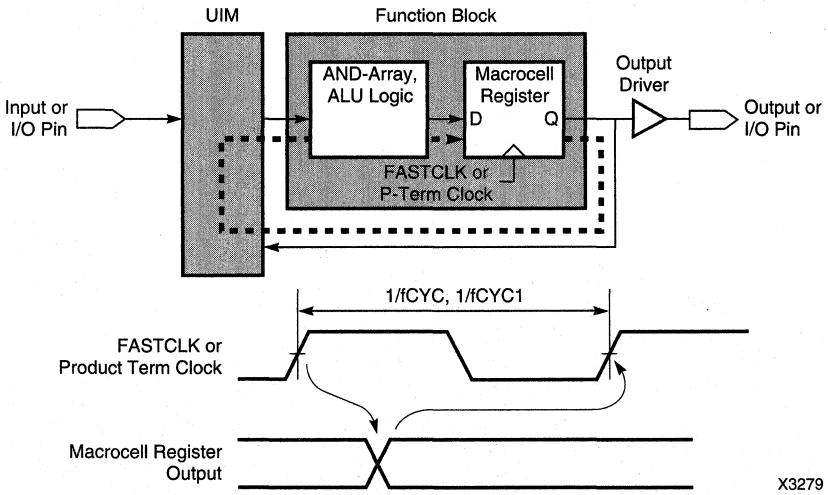


Figure 6: Delay Path Specification for f_{CYC} and f_{CYC1}

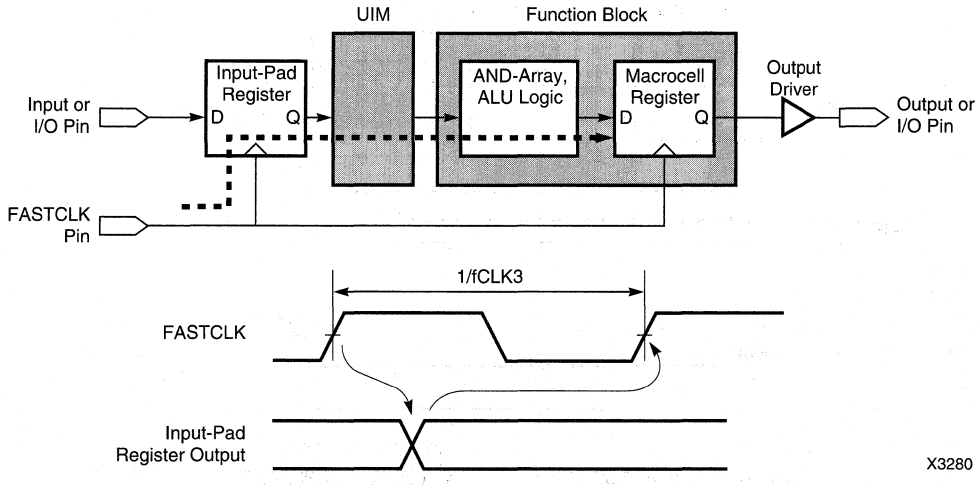


Figure 7: Delay Path Specification for f_{CLK3}

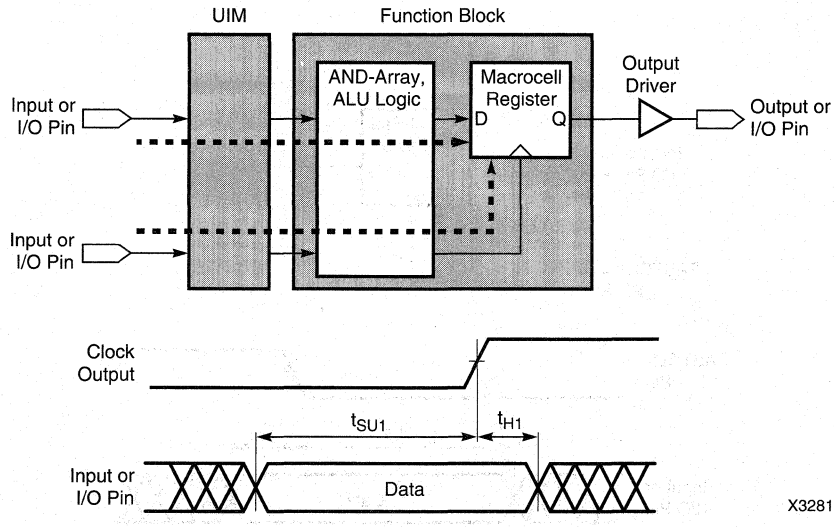


Figure 8: Delay Path Specification for f_{SU1} and f_{H1}

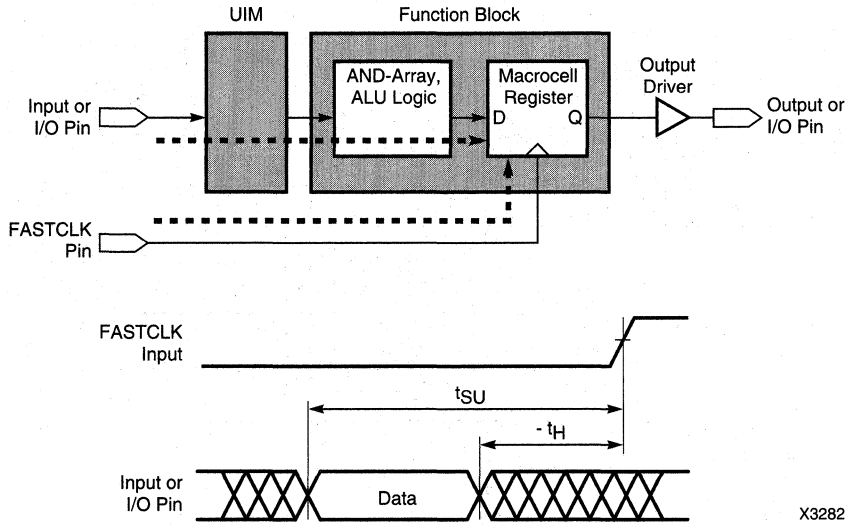


Figure 9: Delay Path Specification for f_{SU} and f_H

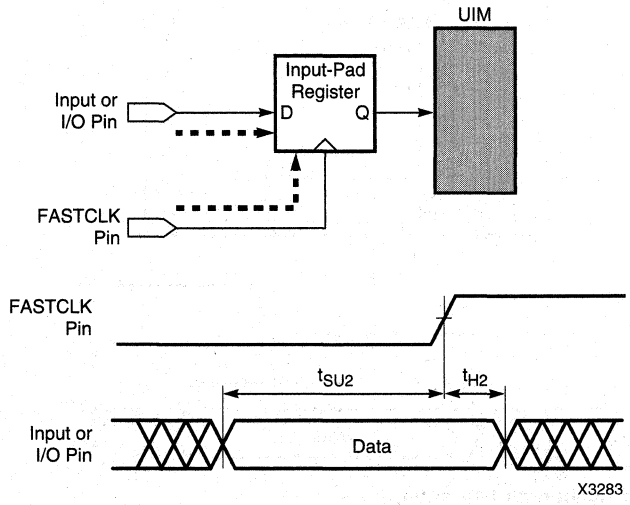


Figure 10: Delay Path Specification for f_{SU2} and f_{H2}

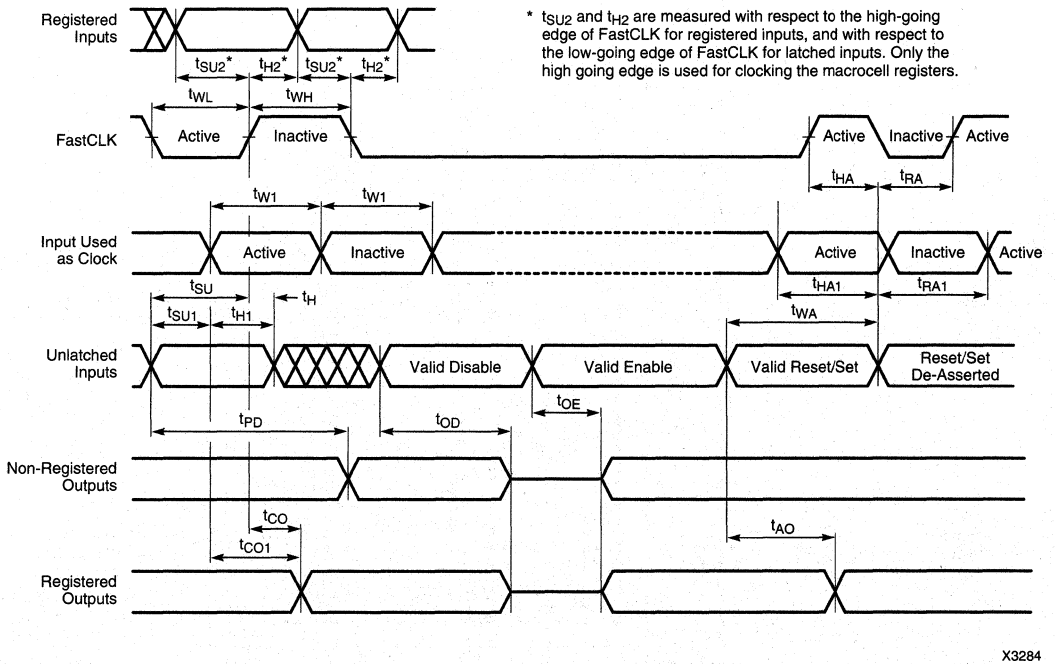


Figure 11: Principal Pin-to-Pin Measurements

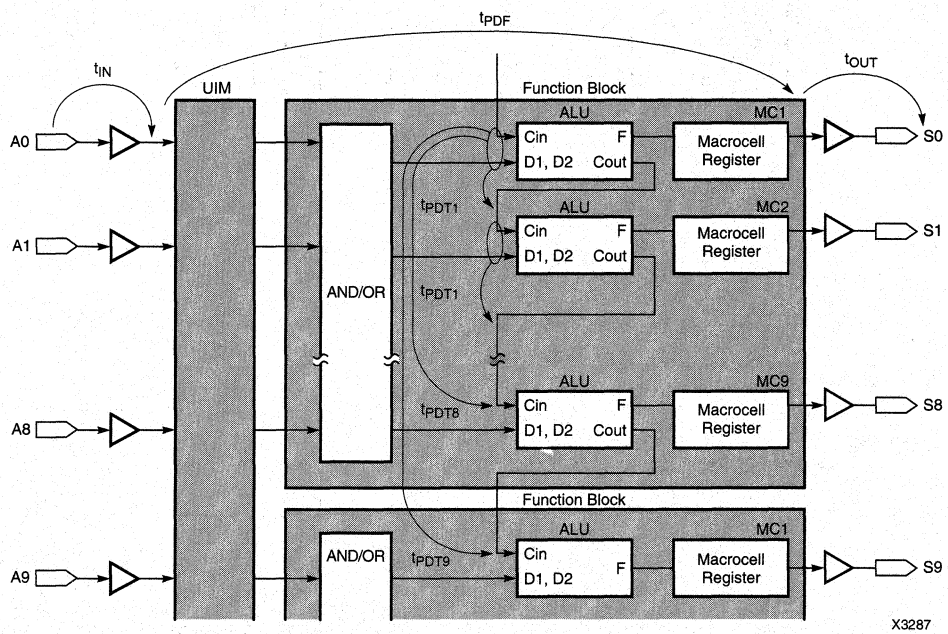


Figure 12: Arithmetic Timing Parameters

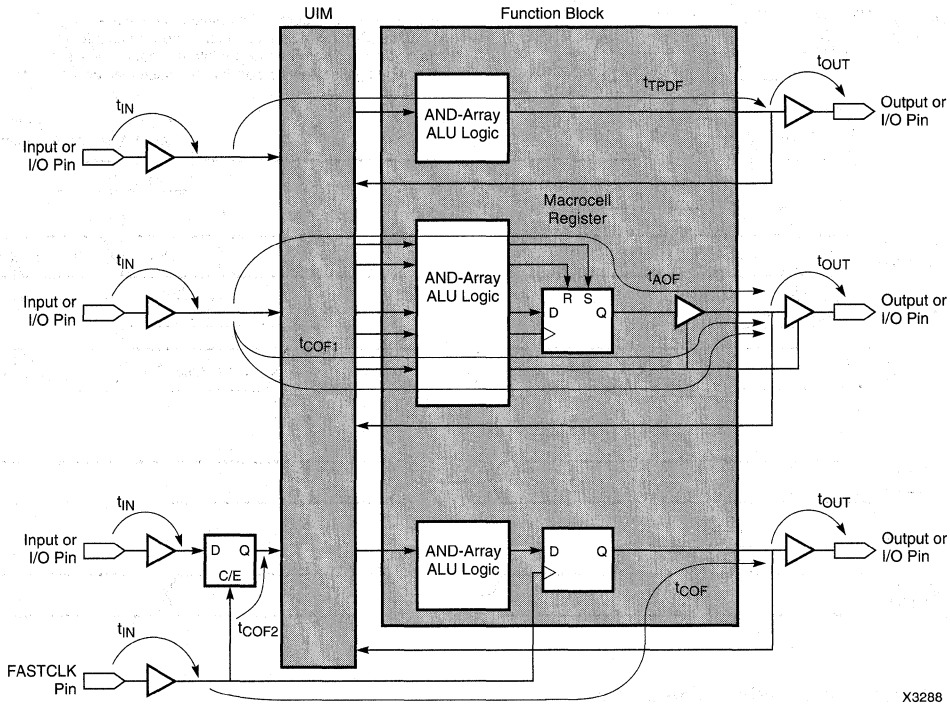


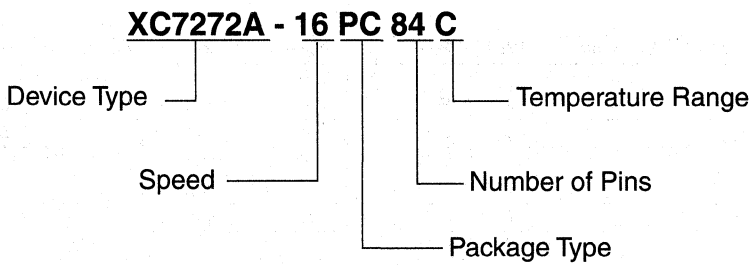
Figure 13: Incremental Timing Parameters

XC7372 Pinouts

PC68	in	XC7272A	out	PC84	PG84
1	Master Reset			1	F-9
2	Input			2	F-11
-	Input			3	E-11
-	Input			4	E-10
3	Input			5	E-9
4	Input			6	D-11
5	Input			7	D-10
6		**GND**		8	C-11
7	Fast CLK0		MC4-4	9	B-11
8	Fast CLK1		MC4-3	10	C-10
9	Input		MC4-2	11	A-11
10	Input		MC4-1	12	B-10
11			MC3-8	13	B-9
12			MC3-7	14	A-10
13			MC3-6	15	A-9
14			MC3-5	16	B-8
15		**GND**		17	A-8
-			MC3-4	18	B-6
-			MC3-3	19	B-7
-			MC3-2	20	A-7
-			MC3-1	21	C-7
16		**Vcc**		22	C-6
17	Input		MC2-9	23	A-6
18	Input		MC2-8	24	A-5
19	Input		MC2-7	25	B-5
20	Input		MC2-6	26	C-5
21		**GND**		27	A-4
22	Input		MC2-5	28	B-4
23	Input		MC2-4	29	A-3
24	Input		MC2-3	30	A-2
25	Input		MC2-2	31	B-3
26	Input		MC2-1	32	A-1
27	Input		MC1-9	33	B-2
28	Input		MC1-8	34	C-2
29	Input		MC1-7	35	B-1
30	Input		MC1-6	36	C-1
31		**GND**		37	D-2
32	Input		MC1-5	38	D-1
33	Input		MC1-4	39	E-3
34	Input		MC1-3	40	E-2
-	Input		MC1-2	41	E-1
-	Input		MC1-1	42	F-2

PC68	in	XC7272A	out	PC84	PG84
35		**Vcc**		43	F-3
-	Input		MC8-9	44	G-3
-	Input		MC8-8	45	G-1
36	Input		MC8-7	46	G-2
37	Input		MC8-6	47	F-1
38	Input		MC8-5	48	H-1
39		**GND**		49	H-2
40	Input		MC8-4	50	J-1
41	Input		MC8-3	51	K-1
42	Input		MC8-2	52	J-2
43	Input		MC8-1	53	L-1
44	Input		MC7-9	54	K-2
45	Input		MC7-8	55	K-3
46	Input		MC7-7	56	L-2
47	Input		MC7-6	57	L-3
48	Input		MC7-5	58	K-4
49		**GND**		59	L-4
50	Input		MC7-4	60	J-5
51	Input		MC7-3	61	K-5
52	Input		MC7-2	62	L-5
53	Input		MC7-1	63	K-6
54		**Vcc**		64	J-6
55			MC6-8	65	J-7
56			MC6-7	66	L-7
57			MC6-6	67	K-7
58			MC6-5	68	L-6
59		**GND**		69	L-8
-			MC6-4	70	K-8
-			MC6-3	71	L-9
-			MC6-2	72	L-10
-			MC6-1	73	K-9
60	Input		MC5-4	74	L-11
61	Input		MC5-3	75	K-10
62	Input		MC5-2	76	J-10
63	Input		MC5-1	77	K-11
64		**GND**		78	J-11
65	Input			79	H-10
66	Input			80	H-11
67	Input			81	F-10
68	Input			82	G-10
-	Input			83	G-11
-	Input			84	G-9

Ordering Information



Speed Options

-25	25 ns (40 MHz) sequential cycle time
-20	20 ns (50 MHz) sequential cycle time
-16	16 ns (60 MHz) sequential cycle time (commercial/industrial only)

Packaging Options

PC68	68-Pin Plastic Leaded Chip Carrier
WC68	68-Pin Windowed Ceramic Leaded Chip Carrier
PC84	84-Pin Plastic Leaded Chip Carrier
WC84	84-Pin Windowed Ceramic Leaded Chip Carrier
PG84	84-Pin Ceramic Windowed Pin Grid Array

Temperature Options

C	Commercial0°C to 70°C
I	Industrial -40°C to 85°C
M	Military -55°C (Ambient) to 125°C (Case)

Component Availability

Pins		68		84		
Type		Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Ceramic PGA
Code		PC68	WC68	PC84	WC84	PG84
XC7272A	-25	CI	CI	CI	CIM	CI
	-20	CI	CI	CI	CIM	CI
	-16	CI	CI	CI	CI	CI

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C M = Military = –55°C(A) to 125°C (C)

SRAM-Based FPGA Products Table of Contents

SRAM-Based FPGA Products

XC4000 Series Field Programmable Gate Arrays

XILINX®

XC4000 Series
Field Programmable Gate Arrays

July 30, 1996 (Version 1.03)

Product Specification

XC4000-Series Features

Note: XC4000-Series devices described in this data sheet include the XC4000E, XC4000EX, XC4000L, and XC4000XL. This information does not apply to the older Xilinx families: XC4000, XC4000A, XC4000D or XC4000H. For information on these devices, see the Xilinx WEBLINX at http://www.xilinx.com.

- Third Generation Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Fully PCI compliant (speed grades -3 and faster)
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance to 66 MHz
- Flexible Array Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per XC4000E output (4 mA per XC4000L output)
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
- Backward Compatible with XC4000 Devices
- XACT*step* Development System runs on '386/'486/ Pentium-type PC, Sun-4, and Hewlett-Packard 700 series
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
  - RAM/ROM compiler

Low-Voltage Versions Available

- Low-Voltage Devices Function at 3.0 - 3.6 Volts
- XC4000L: Low-Voltage Versions of XC4000E devices
- XC4000XL: Low-Voltage Versions of XC4000EX devices

Additional XC4000EX/XL Features

- Highest Capacity — Over 130,000 Usable Gates
- Additional Routing Over XC4000E
  - almost twice the routing capacity for high-density designs
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
- Flexible New High-Speed Clock Network
  - 8 additional Early Buffers for shorter clock delays
  - 4 additional FastCLK™ buffers for fastest clock input
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- High-Speed Parallel Express™ Configuration Mode
- Improved I/O Setup and Clock-to-Output with FastCLK and Global Early Buffers
- 4 Additional Address Bits in Master Parallel Configuration Mode

Introduction

XC4000-Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of eleven years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

The XC4000 Series currently has 19 members, as shown in Table 1.

Table 1: XC4000-Series Field Programmable Gate Arrays

Device	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total Logic Blocks	Number of Flip-Flops	Max. Decode Inputs per side	Max. User I/O
XC4003E	3,000	3,200	2,000 - 5,000	10 x 10	100	360	30	80
XC4005E/L	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112
XC4006E	6,000	8,192	4,000 - 12,000	16 x 16	256	768	48	128
XC4008E	8,000	10,368	6,000 - 15,000	18 x 18	324	936	54	144
XC4010E/L	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160
XC4013E/L	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	72	192
XC4020E	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	84	224
XC4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	96	256
XC4028EX/XL	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	96	256
XC4036EX/XL	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	108	288
XC4044EX/XL	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	120	320
XC4052XL	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	132	352
XC4062XL	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	144	384
	Larger Devices Available in the First Half of 1997							

* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

Note: *Throughout the functional descriptions in this document, references to the XC4000E device family include the XC4000L, and references to the XC4000EX device family include the XC4000XL, unless explicitly stated otherwise. References to the XC4000 Series include the XC4000E, XC4000EX, XC4000L, and XC4000XL families. All functionality in low-voltage families is the same as in the corresponding 5-Volt family, except where numerical references are made to timing, power, or current-sinking capability.*

Description

XC4000-Series devices are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave, peripheral and Express modes).

XC4000-Series FPGAs are supported by powerful and sophisticated software, covering every aspect of design from schematic or behavioral entry, floorplanning, simulation, automatic block placement and routing of interconnects, to the creation, downloading, and readback of the configuration bit stream.

Because Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 5,000 systems per month. For lowest high-volume unit cost, a design can first be implemented in the XC4000E or XC4000EX, then migrated to one of Xilinx' compatible HardWire mask-programmed devices.

Table 2 shows density and performance for a few common circuit functions that can be implemented in XC4000-Series devices.

Table 2: Density and Performance for Several Common Circuit Functions in XC4000E[1]

Design Class	Function	CLBs Used	XC4000E-3	XC4000E-2	Units
Memory	256 x 8 Single Port (read/modify/write)	72	63	80	MHz
	32 x 16 bit FIFO				
	simultaneous read/write	48	63	80	MHz
	MUXed read/write	32	63	80	MHz
Logic	9 bit Shift Register (with enable)	5	170	200	MHz
	16 bit Pre-Scaled Counter	8	142	170	MHz
	16 bit Loadable Counter	8	65	76	MHz
	16 bit Accumulator	9	65	76	MHz
	8 bit, 16 tap FIR Filter sample rate				
	parallel	400	55	65	MHz
	serial	68	8.1	10	MHz
	8 x 8 Parallel Multiplier				
	single stage, register to register	73	37	30	ns
	16 bit Address Decoder (internal decode)	3	4.7	3.9	ns
	9 bit Parity Checker	1	4.3	2.7	ns

Note: 1. Most functions are faster in XC4000EX due to faster carry logic, direct connects, and other additional interconnect.

Taking Advantage of Reconfiguration

FPGA devices can be reconfigured to change logic function while resident in the system. This capability gives the system designer a new degree of freedom not available with any other type of logic.

Hardware can be changed as easily as software. Design updates or modifications are easy, and can be made to products already in the field. An FPGA can even be reconfigured dynamically to perform different functions at different times.

Reconfigurable logic can be used to implement system self-diagnostics, create systems capable of being reconfigured for different environments or operations, or implement multi-purpose hardware for a given application. As an added benefit, using reconfigurable FPGA devices simplifies hardware design and debugging and shortens product time-to-market.

XC4000E and XC4000EX Families Compared to the XC4000

For readers already familiar with the XC4000 family of Xilinx Field Programmable Gate Arrays, the major new features in the XC4000-Series devices are listed in this section. The biggest advantages of XC4000E and XC4000EX devices are significantly increased system speed, greater capacity, and new architectural features, particularly Select-RAM memory. The XC4000EX devices also offer many new routing features, including special high-speed clock buffers that can be used to capture input data with minimal delay.

Any XC4000E device is pinout- and bitstream-compatible with the corresponding XC4000 device. An existing XC4000 bitstream can be used to program an XC4000E device. However, since the XC4000E includes many new features, an XC4000E bitstream cannot be loaded into an XC4000 device.

Most XC4000EX devices have no corresponding XC4000 devices, because of the larger CLB arrays. The XC4028EX has the same array size as the XC4025 and XC4025E, but is not bitstream-compatible. However, the XC4025, XC4025E, and XC4028EX are all pinout-compatible.

Improvements in XC4000E and XC4000EX

Increased System Speed

Delays in FPGA-based designs are layout dependent. There is a rule of thumb designers can consider—the system clock rate should not exceed one third to one half of the specified toggle rate. Critical portions of a design, such as shift registers and simple counters, can run faster—approximately two thirds of the specified toggle rate.

XC4000E and XC4000EX devices can run at synchronous system clock rates of up to 66 MHz, and internal performance can exceed 150 MHz. This increase in performance over the previous families stems from improvements in both device processing and system architecture. XC4000-Series devices use a sub-micron triple-layer metal process. In addition, many architectural improvements have been made, as described below.

PCI Compliance

XC4000-Series -3 and faster speed grades are fully PCI compliant. XC4000E and XC4000EX devices can be used to implement a one-chip PCI solution.

Carry Logic

The speed of the carry logic chain has increased dramatically. Some parameters, such as the delay on the carry chain through a single CLB (TBYP), have improved by as much as 50% from XC4000 values. See "Fast Carry Logic" on page 21 for more information.

Select-RAM Memory: Edge-Triggered, Synchronous RAM Modes

The RAM in any CLB can be configured for synchronous, edge-triggered, write operation. The read operation is not affected by this change to an edge-triggered write.

Dual-Port RAM

A separate option converts the 16x2 RAM in any CLB into a 16x1 dual-port RAM with simultaneous Read/Write.

The function generators in each CLB can be configured as either level-sensitive (asynchronous) single-port RAM, edge-triggered (synchronous) single-port RAM, edge-triggered (synchronous) dual-port RAM, or as combinatorial logic.

Configurable RAM Content

The RAM content can now be loaded at configuration time, so that the RAM starts up with user-defined data.

H Function Generator

In XC4000-Series devices, the H function generator is more versatile than in the XC4000. Its inputs can come not only from the F and G function generators but also from up to three of the four control input lines. The H function generator can thus be totally or partially independent of the other two function generators, increasing the maximum capacity of the device.

IOB Clock Enable

The two flip-flops in each IOB have a common clock enable input, which through configuration can be activated individually for the input or output flip-flop or both. This clock enable operates exactly like the EC pin on the XC4000 CLB. This new feature makes the IOBs more versatile, and avoids the need for clock gating.

Output Drivers

The output pull-up structure defaults to a TTL-like totem-pole. This driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc, just like the XC4000 outputs. Alternatively, XC4000-Series devices can be globally configured with CMOS outputs, with p-channel pull-up transistors pulling to Vcc. Also, the configurable pull-up resistor in the XC4000 Series is a p-channel transistor that pulls to Vcc, whereas in the XC4000 it is an n-channel transistor that pulls to a voltage one transistor threshold below Vcc.

Input Thresholds

The input thresholds can be globally configured for either TTL (1.2 V threshold) or CMOS (2.5 V threshold), just like XC2000 and XC3000 inputs. The two global adjustments of input threshold and output level are independent of each other.

Global Signal Access to Logic

There is additional access from global clocks to the F and G function generator inputs.

Configuration Pin Pull-Up Resistors

During configuration, the three mode pins, M0, M1, and M2, have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected.

The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors after configuration.

The $\overline{\text{PROGRAM}}$ input pin has a permanent weak pull-up.

Soft Start-up

Like the XC3000A, XC4000-Series devices have "Soft Start-up." When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. This feature avoids potential ground bounce when all outputs are turned on simultaneously. Immediately after start-up, the slew rate of the individual outputs is, as in the XC4000 family, determined by the individual configuration option.

XC4000 and XC4000A Compatibility

Existing XC4000 bitstreams can be used to configure an XC4000E device. XC4000A bitstreams must be recompiled for use with the XC4000E due to improved routing resources, although the devices are pin-for-pin compatible.

Additional Improvements in XC4000EX Only

Increased Routing

New interconnect in the XC4000EX includes twenty-two additional vertical lines in each column of CLBs and twelve new horizontal lines in each row of CLBs. The twelve "Quad Lines" in each CLB row and column include optional repowering buffers for maximum speed. Additional high-performance routing near the IOBs enhances pin flexibility.

Faster Input and Output

A fast, dedicated early clock sourced by global clock buffers is available for the IOBs. To ensure synchronization with the regular global clocks, a Fast Capture latch driven by the early clock is available. The input data can be initially loaded into the Fast Capture latch with the early clock, then transferred to the input flip-flop or latch with the low-skew global clock. A programmable delay on the input can be used to avoid hold-time requirements. See "IOB Input Signals" on page 24 for more information.

Latch Capability in CLBs

Storage elements in the XC4000EX CLB can be configured as either flip-flops or latches. This capability makes the FPGA highly synthesis-compatible.

IOB Output MUX From Output Clock

A multiplexer in the IOB allows the output clock to select either the output data or the IOB clock enable as the output to the pad. Thus, two different data signals can share a single output pad, effectively doubling the number of device outputs without requiring a larger, more expensive package. This multiplexer can also be configured as an AND-gate to implement a very fast pin-to-pin path. See "IOB Output Signals" on page 27 for more information.

Express Configuration Mode

A new slave configuration mode accepts parallel data input. Data is processed in parallel, rather than serialized internally. Therefore, the data rate is eight times that of the six conventional configuration modes.

Additional Address Bits

Larger devices require more bits of configuration data. A daisy chain of several large XC4000EX devices may require a PROM that cannot be addressed by the eighteen address bits supported in the XC4000E. The XC4000EX family therefore extends the addressing in Master Parallel configuration mode to 22 bits.

Table 3: CLB Count of Selected XC4000-Series Soft Macros

7400 Equivalents	CLBs
'138	5
'139	2
'147	5
'148	6
'150	5
'151	3
'152	3
'153	2
'154	16
'157	2
'158	2
'160	5
'161	6
'162	8
'163	8
'164	4
'165s	9
'166	5
'168	7
'174	3
'194	5
'195	3
'280	3
'283	8
'298	2
'352	2
'390	3
'518	3
'521	3
Explanation of RAM nomenclature	
s = single-port edge-triggered	
d = dual-port edge-triggered	
no extension = level-sensitive	

Barrel Shifters	CLBs
brlshft4	4
brlshft8	13
4-Bit Counters	
cd4cd	3
cd4cle	5
cd4rle	6
cb4ce	3
cb4cle	6
cb4re	5
8- and 16-Bit Counters	
cb8ce	6
cb8re	10
cc16ce	9
cc16cle	9
cc16cled	21
Identity Comparators	
comp4	1
comp8	2
comp16	5
Magnitude Comparators	
compm4	4
compm8	9
compm16	20
RAMs	
ram16x4	2
ram16x4s	2
ram16x4d	4

Multiplexers	CLBs
m2-1e	1
m4-1e	1
m8-1e	3
m16-1e	5
Registers	
rd4r	2
rd8r	4
rd16r	8
Shift Registers	
sr8ce	4
sr16re	8
Decoders	
d2-4e	2
d3-8e	4
d4-16e	16

Explanation of counter nomenclature
- cb = binary counter
- cd = BCD counter
- cc = cascadable binary counter
- d = bidirectional
- l = loadable
- e = clock enable
- r = synchronous reset
- c = asynchronous clear

Detailed Functional Description

XC4000-Series devices achieve high speed through advanced semiconductor technology and improved architecture. The XC4000E and XC4000EX support system clock rates of up to 66 MHz and internal performance in excess of 150 MHz. Compared to older Xilinx FPGA families, XC4000-Series devices are more powerful. They offer on-chip edge-triggered and dual-port RAM, clock enables on I/O flip-flops, and wide-input decoders. They are more versatile in many applications, especially those involving RAM. Design cycles are faster due to a combination of increased routing resources and more sophisticated software.

Basic Building Blocks

Xilinx user-programmable gate arrays include two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.

Three other types of circuits are also available:

- 3-State buffers (TBUFs) driving horizontal longlines are associated with each CLB.
- Wide edge decoders are available around the periphery of each device.
- An on-chip oscillator is provided.

Programmable interconnect resources provide routing paths to connect the inputs and outputs of these configurable elements to the appropriate networks.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Each of these available circuits is described in this section.

Configurable Logic Blocks (CLBs)

Configurable Logic Blocks implement most of the logic in an FPGA. The principal CLB elements are shown in Figure 1. The number of CLBs needed to implement selected soft macros is shown in Table 3.

Two 4-input function generators (F and G) offer unrestricted versatility. Most combinatorial logic functions need four or fewer inputs. However, a third function generator (H) is provided. The H function generator has three inputs. Either zero, one, or both of these inputs can be the outputs of F and G; the other input(s) are from outside the CLB. The CLB can, therefore, implement certain functions of up to nine variables, like parity check or expandable-identity comparison of two sets of four inputs.

Each CLB contains two storage elements that can be used to store the function generator outputs. However, the storage elements and function generators can also be used independently. These storage elements can be configured as flip-flops in both XC4000E and XC4000EX devices; in the XC4000EX they can optionally be configured as latches. DIN can be used as a direct input to either of the two storage elements. H1 can drive the other through the H function generator. Function generator outputs can also drive two outputs independent of the storage element outputs. This versatility increases logic capacity and simplifies routing.

Thirteen CLB inputs and four CLB outputs provide access to the function generators and storage elements. These inputs and outputs connect to the programmable interconnect resources outside the block.

Function Generators

Four independent inputs are provided to each of two function generators (F1 - F4 and G1 - G4). These function generators, with outputs labeled F' and G', are each capable of implementing any arbitrarily defined Boolean function of four inputs. The function generators are implemented as memory look-up tables. The propagation delay is therefore independent of the function implemented.

A third function generator, labeled H', can implement any Boolean function of its three inputs. Two of these inputs can optionally be the F' and G' functional generator outputs. Alternatively, one or both of these inputs can come from outside the CLB (H2, H0). The third input must come from outside the block (H1).

Signals from the function generators can exit the CLB on two outputs. F' or H' can be connected to the X output. G' or H' can be connected to the Y output.

A CLB can be used to implement any of the following functions:

- any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables[1]
- any single function of five variables
- any function of four variables together with some functions of six variables
- some functions of up to nine variables.

1. When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

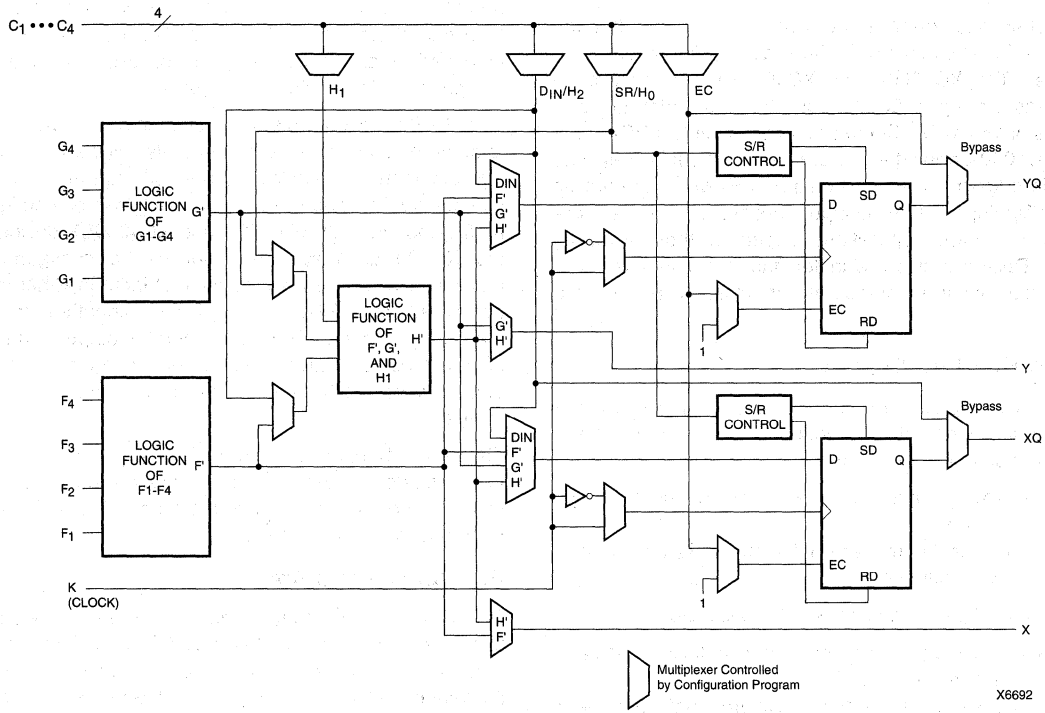


Figure 1: Simplified Block Diagram of XC4000-Series CLB (RAM and Carry Logic functions not shown)

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

Flip-Flops

The CLB can pass the combinatorial output(s) to the interconnect network, but can also store the combinatorial results or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well.

The two edge-triggered D-type flip-flops have common clock (K) and clock enable (EC) inputs. Either or both clock inputs can also be permanently enabled. Storage element functionality is described in Table 4.

Latches (XC4000EX only)

The CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Storage element functionality is described in Table 4.

Table 4: CLB Storage Element Functionality (active rising edge is shown)

Mode	K	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop	X	X	1	X	SR
	↑	1*	0*	D	D
	0	X	0*	X	Q
Latch	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

X	Don't care
↑	Rising edge
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The clock pin is shared by both storage elements. However, the clock is individually invertible for each storage element. Any inverter placed on the clock input is automatically absorbed into the CLB.

Clock Enable

The clock enable signal (EC) is active High. The EC pin is shared by both storage elements. If left unconnected for either, the clock enable for that storage element defaults to the active state. EC is not invertible within the CLB.

Set/Reset

An asynchronous storage element input (SR) can be configured as either set or reset. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a Global Set/Reset pulse during normal operation, and the effect of a pulse on the SR pin of the CLB. All three set/reset functions for any single flip-flop are controlled by the same configuration data bit.

The set/reset state can be independently specified for each flip-flop. This input can also be independently disabled for either flip-flop.

The set/reset state is specified by using the INIT attribute, or by placing the appropriate set or reset flip-flop library symbol.

SR is active High. It is not invertible within the CLB.

Global Set/Reset

A separate Global Set/Reset line (not shown in Figure 1) sets or clears each storage element during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, a reset flip-flop is reset by both SR and GSR.

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 2.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global Set/Reset signal.

Alternatively, GSR can be driven from any internal node.

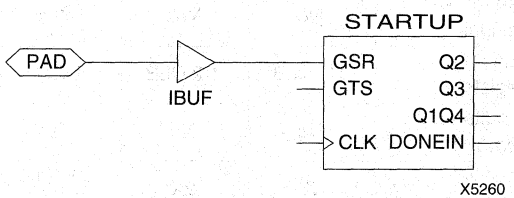


Figure 2: Schematic Symbols for Global Set/Reset

Data Inputs and Outputs

The source of a storage element data input is programmable. It is driven by any of the functions F', G', and H', or by the Direct In (DIN) block input. The flip-flops or latches drive the XQ and YQ CLB outputs.

Two fast feed-through paths are available, as shown in Figure 1. A two-to-one multiplexer on each of the XQ and YQ outputs selects between a storage element output and any of the control inputs. This bypass is sometimes used by the automated router to repower internal signals.

Control Signals

Multiplexers in the CLB map the four control inputs (C1 - C4 in Figure 1) into the four internal control signals (H1, DIN/H2, SR/H0, and EC). Any of these inputs can drive any of the four internal control signals.

When the logic function is enabled, the four inputs are:

- EC — Enable Clock
- SR/H0 — Asynchronous Set/Reset or H function generator Input 0
- DIN/H2 — Direct In or H function generator Input 2
- H1 — H function generator Input 1.

When the memory function is enabled, the four inputs are:

- EC — Enable Clock
- WE — Write Enable
- D0 — Data Input to F and/or G function generator
- D1 — Data input to G function generator (16x1 and 16x2 modes) or 5th Address bit (32x1 mode).

Using FPGA Flip-Flops and Latches

The abundance of flip-flops in the XC4000 Series invites pipelined designs. This is a powerful way of increasing performance by breaking the function into smaller subfunctions and executing them in parallel, passing on the results through pipeline flip-flops. This method should be seriously considered wherever throughput is more important than latency.

To include a CLB flip-flop, place the appropriate library symbol. For example, FDCE is a D-type flip-flop with clock enable and asynchronous clear. The corresponding latch symbol (for the XC4000EX only) is called LDCE.

In XC4000-Series devices, the flip flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated task. This ability increases the functional capacity of the devices.

The CLB setup time is specified between the function generator inputs and the clock input K. Therefore, the specified CLB flip-flop setup time includes the delay through the function generator.

Using Function Generators as RAM

Optional modes for each CLB make the memory look-up tables in the F' and G' function generators usable as an array of Read/Write memory cells. Available modes are level-sensitive (similar to the XC4000/A/H families), edge-triggered, and dual-port edge-triggered. Depending on the selected mode, a single CLB can be configured as either a 16x2, 32x1, or 16x1 bit array.

Supported CLB memory configurations and timing modes for single- and dual-port modes are shown in Table 5.

XC4000-Series devices are the first programmable logic devices with edge-triggered (synchronous) and dual-port RAM accessible to the user. Edge-triggered RAM simplifies system timing. Dual-port RAM doubles the effective throughput of FIFO applications. These features can be individually programmed in any XC4000-Series CLB.

Advantages of On-Chip and Edge-Triggered RAM

The on-chip RAM is extremely fast. The read access time is the same as the logic delay. The write access time is slightly slower. Both access times are much faster than any off-chip solution, because they avoid I/O delays.

Edge-triggered RAM, also called synchronous RAM, is a feature never before available in a Field Programmable Gate Array. The simplicity of designing with edge-triggered RAM, and the markedly higher achievable performance, add up to a significant improvement over existing devices with on-chip RAM.

Three application notes are available from Xilinx that discuss edge-triggered RAM: "*XC4000E Edge-Triggered and Dual-Port RAM Capability*," "*Implementing FIFOs in XC4000E RAM*," and "*Synchronous and Asynchronous FIFO Designs*." All three application notes apply to both XC4000E and XC4000EX RAM.

Table 5: Supported RAM Modes

	16 x 1	16 x 2	32 x 1	Edge-Triggered Timing	Level-Sensitive Timing
Single-Port	√	√	√	√	√
Dual-Port	√			√	

RAM Configuration Options

The function generators in any CLB can be configured as RAM arrays in the following sizes:

- Two 16x1 RAMs: two data inputs and two data outputs with identical or, if preferred, different addressing for each RAM
- One 32x1 RAM: one data input and one data output.

One F or G function generator can be configured as a 16x1 RAM while the other function generators are used to implement any function of up to 5 inputs.

Additionally, the XC4000-Series RAM may have either of two timing modes:

- Edge-Triggered (Synchronous): data written by the designated edge of the CLB clock. WE acts as a true clock enable.
- Level-Sensitive (Asynchronous): an external WE signal acts as the write strobe.

The selected timing mode applies to both function generators within a CLB when both are configured as RAM.

The number of read ports is also programmable:

- Single Port: each function generator has a common read and write port
- Dual Port: both function generators are configured together as a single 16x1 dual-port RAM with one write port and two read ports. Simultaneous read and write operations to the same or different addresses are supported.

RAM configuration options are selected by placing the appropriate library symbol.

Choosing a RAM Configuration Mode

The appropriate choice of RAM mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Recommended usage is shown in Table 6.

The difference between level-sensitive, edge-triggered, and dual-port RAM is only in the write operation. Read operation and timing is identical for all modes of operation.

Table 6: RAM Mode Selection

	Level-Sensitive	Edge-Triggered	Dual-Port Edge-Triggered
Use for New Designs?	No	Yes	Yes
Size (16x1, Registered)	1/2 CLB	1/2 CLB	1 CLB
Simultaneous Read/Write	No	No	Yes
Relative Performance	X	2X	2X (4X effective)

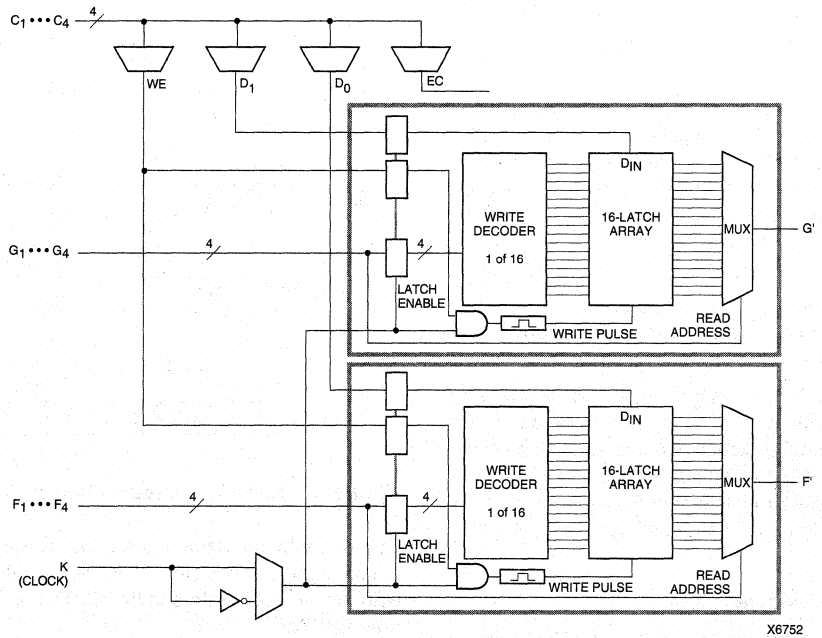


Figure 3: 16x2 (or 16x1) Edge-Triggered Single-Port RAM

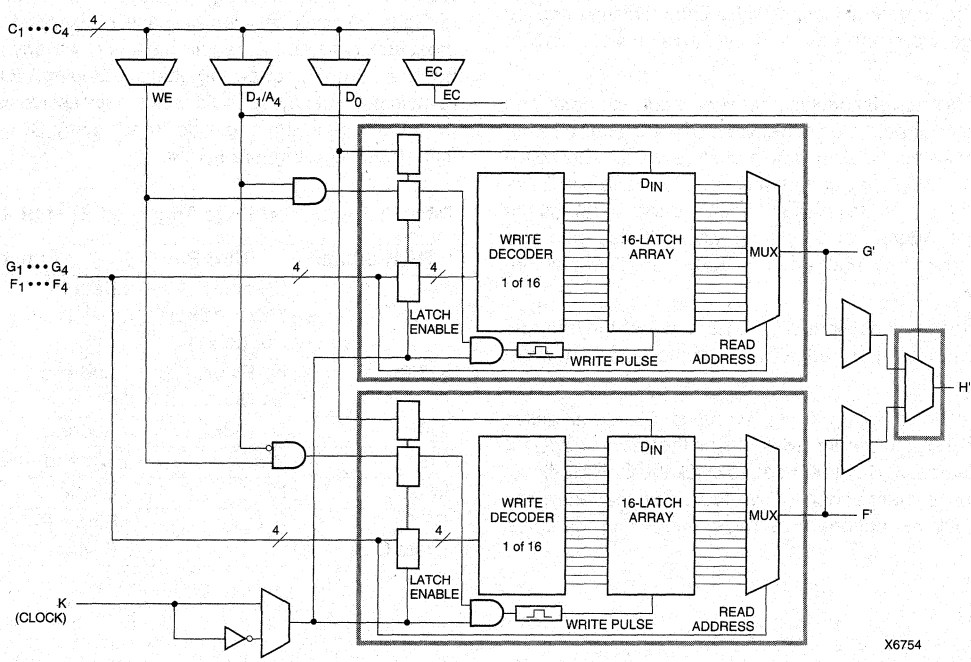


Figure 4: 32x1 Edge-Triggered Single-Port RAM (F and G addresses are identical)

RAM Inputs and Outputs

The F1-F4 and G1-G4 inputs to the function generators act as address lines, selecting a particular memory cell in each look-up table.

The functionality of the CLB control signals changes when the function generators are configured as RAM. The DIN/H2, H1, and SR/H0 lines become the two data inputs (D0, D1) and the Write Enable (WE) input for the 16x2 memory. When the 32x1 configuration is selected, D1 acts as the fifth address bit and D0 is the data input.

The contents of the memory cell(s) being addressed are available at the F' and G' function-generator outputs. They can exit the CLB through its X and Y outputs, or can be captured in the CLB flip-flop(s).

Configuring the CLB function generators as Read/Write memory does not affect the functionality of the other portions of the CLB, with the exception of the redefinition of the control signals. In 16x2 and 16x1 modes, the H' function generator can be used to implement Boolean functions of F', G', and D1, and the D flip-flops can latch the F', G', H', or D0 signals.

Single-Port Edge-Triggered Mode

Edge-triggered (synchronous) RAM simplifies timing requirements. XC4000-Series edge-triggered RAM timing operates like writing to a data register. Data and address are presented. The register is enabled for writing by a logic High on the write enable input, WE. Then a rising or falling clock edge loads the data into the register, as shown in Figure 5.

Complex timing relationships between address, data, and write enable signals are not required, and the external write enable pulse becomes a simple clock enable. The active edge of WCLK latches the address, input data, and WE signals. An internal write pulse is generated that performs the write. See Figure 3 and Figure 4 for block diagrams of a CLB configured as 16x2 and 32x1 edge-triggered, single-port RAM.

The relationships between CLB pins and RAM inputs and outputs for single-port, edge-triggered mode are shown in Table 7.

The Write Clock input (WCLK) can be configured as active on either the rising edge (default) or the falling edge. It uses the same CLB pin (K) used to clock the CLB flip-flops, but it can be independently inverted. Consequently, the RAM output can optionally be registered within the same

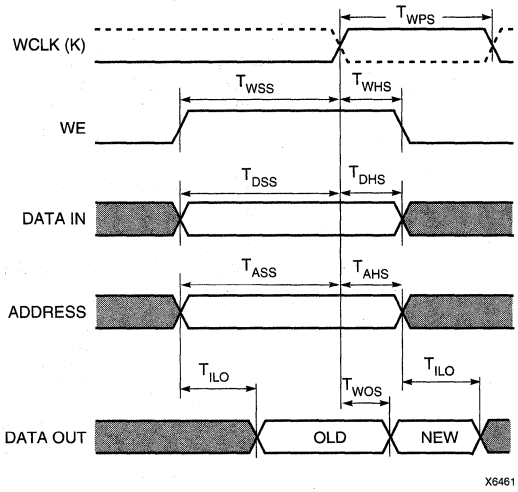


Figure 5: Edge-Triggered RAM Write Timing

CLB either by the same clock edge as the RAM, or by the opposite edge of this clock. The sense of WCLK applies to both function generators in the CLB when both are configured as RAM.

The WE pin is active-High and is not invertible within the CLB.

Note: The pulse following the active edge of WCLK (T_{WPS} in Figure 5) must be less than one millisecond wide. For most applications, this requirement is not overly restrictive; however, it must not be forgotten. Stopping WCLK at this point in the write cycle could result in excessive current and even damage to the larger devices if many CLBs are configured as edge-triggered RAM.

Table 7: Single-Port Edge-Triggered RAM Signals

RAM Signal	CLB Pin	Function
D	D0 or D1 (16x2, 16x1) D0 (32x1)	Data In
A[3:0]	F1-F4 or G1-G4	Address
A[4]	D1 (32x1)	Address
WE	WE	Write Enable
WCLK	K	Clock
SPO (Data Out)	F' or G'	Single Port Out (Data Out)

Dual-Port Edge-Triggered Mode

In dual-port mode, both the F and G function generators are used to create a single 16x1 RAM array with one write port and two read ports. The resulting RAM array can be read and written simultaneously at two independent addresses. Simultaneous read and write operations at the same address are also supported.

Dual-port mode always has edge-triggered write timing, as shown in Figure 5.

Figure 6 shows a simple model of an XC4000-Series CLB configured as dual-port RAM. One address port, labeled A[3:0], supplies both the read and write address for the F function generator. This function generator behaves the same as a 16x1 single-port edge-triggered RAM array. The RAM output, Single Port Out (SPO), appears at the F function generator output. SPO, therefore, reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the G function generator. The write address for the G function generator, however, comes from the address A[3:0]. The output from this 16x1 RAM array, Dual Port Out (DPO), appears at the G function generator output. DPO, therefore, reflects the data at address DPRA[3:0].

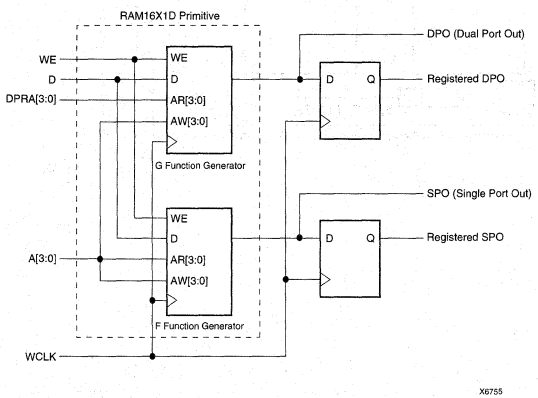


Figure 6: XC4000-Series Dual-Port RAM, Simple Model

Therefore, by using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. Simultaneous access doubles the effective throughput of the FIFO.

The relationships between CLB pins and RAM inputs and outputs for dual-port, edge-triggered mode are shown in Table 8. See Figure 7 for a block diagram of a CLB configured in this mode.

Note: The pulse following the active edge of WCLK (T_{WPS} in Figure 5) must be less than one millisecond wide. For most applications, this requirement is not overly restrictive; however, it must not be forgotten. Stopping WCLK at this point in the write cycle could result in excessive current and even damage to the larger devices if many CLBs are configured as edge-triggered RAM.

Table 8: Dual-Port Edge-Triggered RAM Signals

RAM Signal	CLB Pin	Function
D	D0	Data In
A[3:0]	F1-F4	Read Address for F, Write Address for F and G
DPRA[3:0]	G1-G4	Read Address for G
WE	WE	Write Enable
WCLK	K	Clock
SPO	F'	Single Port Out (addressed by A[3:0])
DPO	G'	Dual Port Out (addressed by DPRA[3:0])

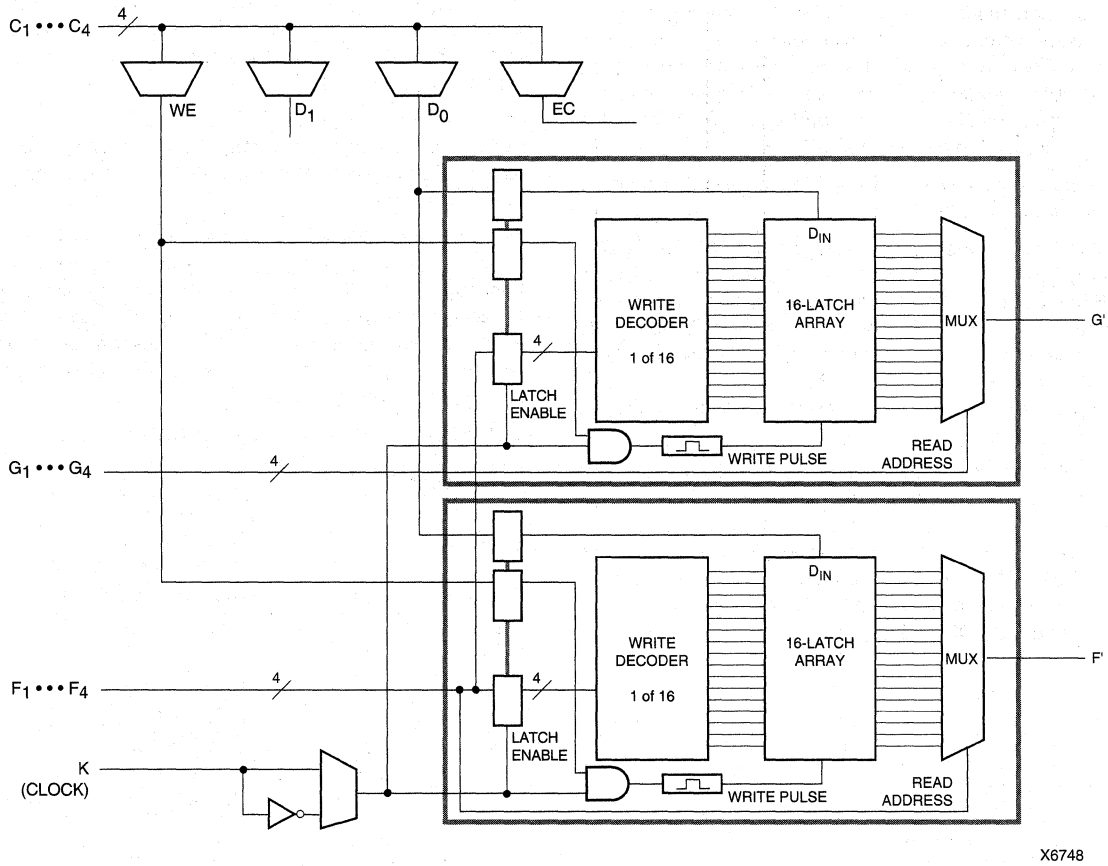


Figure 7: 16x1 Edge-Triggered Dual-Port RAM

Single-Port Level-Sensitive Timing Mode

Note: Edge-triggered mode is recommended for all new designs. Level-sensitive mode, also called asynchronous mode, is still supported for XC4000-Series backward-compatibility with the XC4000 family.

Level-sensitive RAM timing is simple in concept but can be complicated in execution. Data and address signals are presented, then a positive pulse on the write enable pin (WE) performs a write into the RAM at the designated address. As indicated by the "level-sensitive" label, this RAM acts like a latch. During the WE High pulse, changing the data lines results in new data written to the old address. Changing the address lines while WE is High results in spurious data written to the new address—and possibly at other addresses as well, as the address lines inevitably do not all change simultaneously.

The user must generate a carefully timed WE signal. The delay on the WE signal and the address lines must be carefully verified to ensure that WE does not become active until after the address lines have settled, and that WE goes inactive before the address lines change again. The data must be stable before and after the falling edge of WE.

In practical terms, WE is usually generated by a 2X clock. If a 2X clock is not available, the falling edge of the system clock can be used. However, there are inherent risks in this approach, since the WE pulse must be guaranteed inactive before the next rising edge of the system clock. Several older application notes are available from Xilinx that discuss the design of level-sensitive RAMs. These application notes include XAPP031, "*Using the XC4000 RAM Capability*," and XAPP042, "*High-Speed RAM Design in XC4000*."

However, the edge-triggered RAM available in the XC4000 Series is superior to level-sensitive RAM for almost every application.

Figure 8 shows the write timing for level-sensitive, single-port RAM.

The relationships between CLB pins and RAM inputs and outputs for single-port level-sensitive mode are shown in Table 9.

Figure 9 and Figure 10 show block diagrams of a CLB configured as 16x2 and 32x1 level-sensitive, single-port RAM.

Initializing RAM at Configuration

Both RAM and ROM implementations of the XC4000-Series devices are initialized during configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the schematic library guide.

If not defined, all RAM contents are initialized to all zeros, by default.

RAM initialization occurs only during configuration. The RAM content is not affected by Global Set/Reset.

Table 9: Single-Port Level-Sensitive RAM Signals

RAM Signal	CLB Pin	Function
D	D0 or D1	Data In
A[3:0]	F1-F4 or G1-G4	Address
WE	WE	Write Enable
O	F' or G'	Data Out

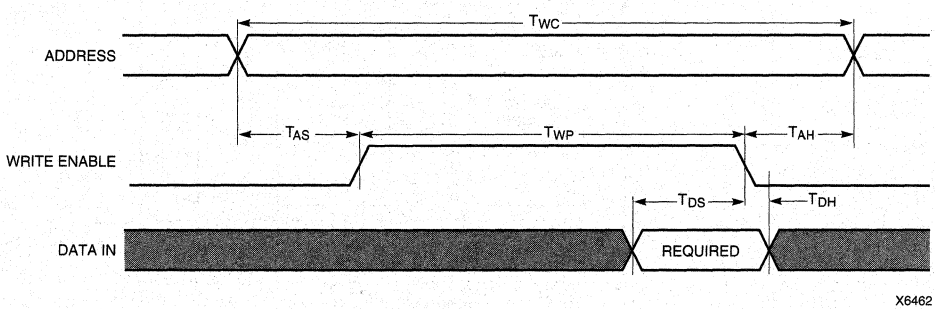


Figure 8: Level-Sensitive RAM Write Timing

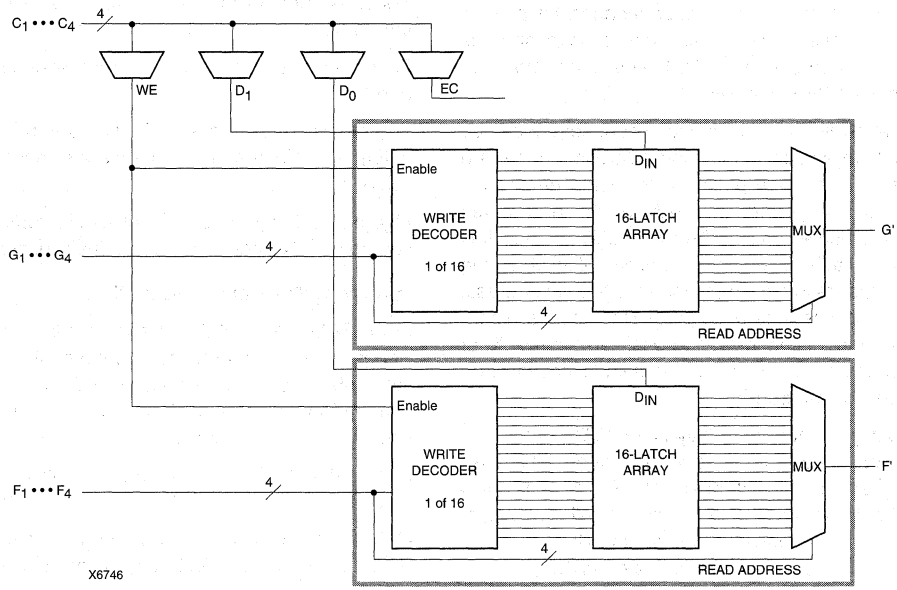


Figure 9: 16x2 (or 16x1) Level-Sensitive Single-Port RAM

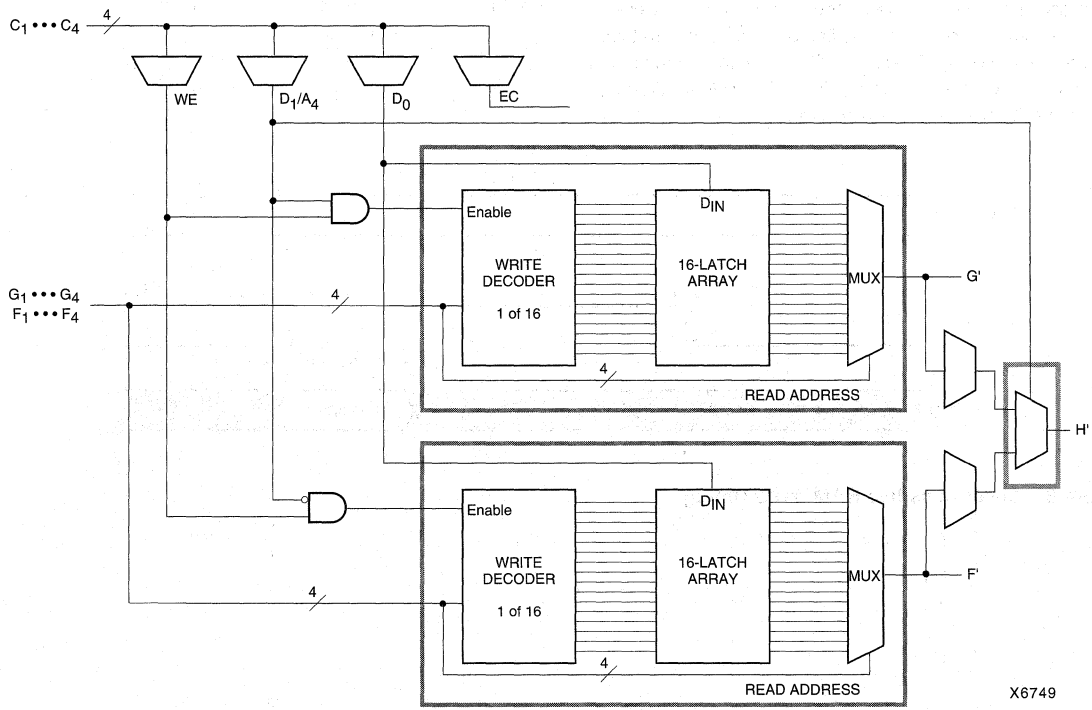


Figure 10: 32x1 Level-Sensitive Single-Port RAM (F and G addresses are identical)

Fast Carry Logic

Each CLB F and G function generator contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources.

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level.

This fast carry logic is one of the more significant features of the XC4000 Series, speeding up arithmetic and counting into the 70 MHz range.

The carry chain in XC4000E devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. (See Figure 11.) In order to improve speed in the high-capacity XC4000EX devices, which can potentially have very long carry chains, the carry chain travels upward only, as shown in Figure 12. This restriction should have little impact, because the smallest XC4000EX device, the XC4028EX, can accommodate a 64-bit carry chain in a single column. Additionally, standard interconnect can be used to route a carry signal in the downward direction.

Figure 13 on page 22 shows an XC4000E CLB with dedicated fast carry logic. The carry logic in the XC4000EX is similar, except that COUT exits at the top only, and the signal CINDOWN does not exist. As shown in Figure 13, the carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 14 and Figure 15 on page 23 show the details of the carry logic for the XC4000E and the XC4000EX respectively. These diagrams show the contents of the box labeled "CARRY LOGIC" in Figure 13. As shown, the XC4000EX carry logic eliminated a multiplexer to reduce delay on the pass-through carry chain. Additionally, the multiplexer on the G4 path now has a memory-programmable input, which permits G4 to directly connect to COUT. G4 thus becomes an additional high-speed initialization path for carry-in.

The dedicated carry logic is discussed in detail in Xilinx document XAPP 013: "*Using the Dedicated Carry Logic in XC4000*." This discussion also applies to XC4000E devices, and to XC4000EX devices when the minor logic changes are taken into account.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

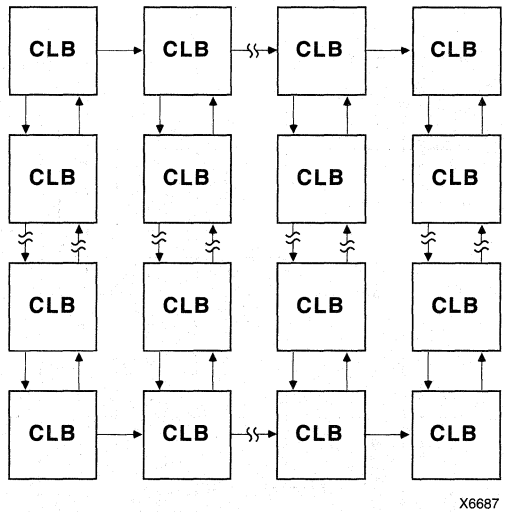


Figure 11: Available XC4000E Carry Propagation Paths

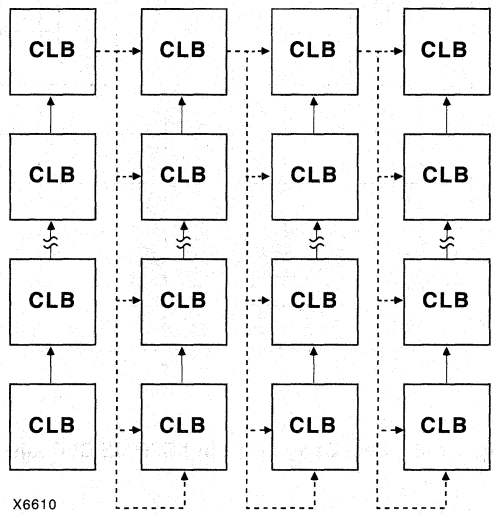


Figure 12: Available XC4000EX Carry Propagation Paths (dotted lines use general interconnect)

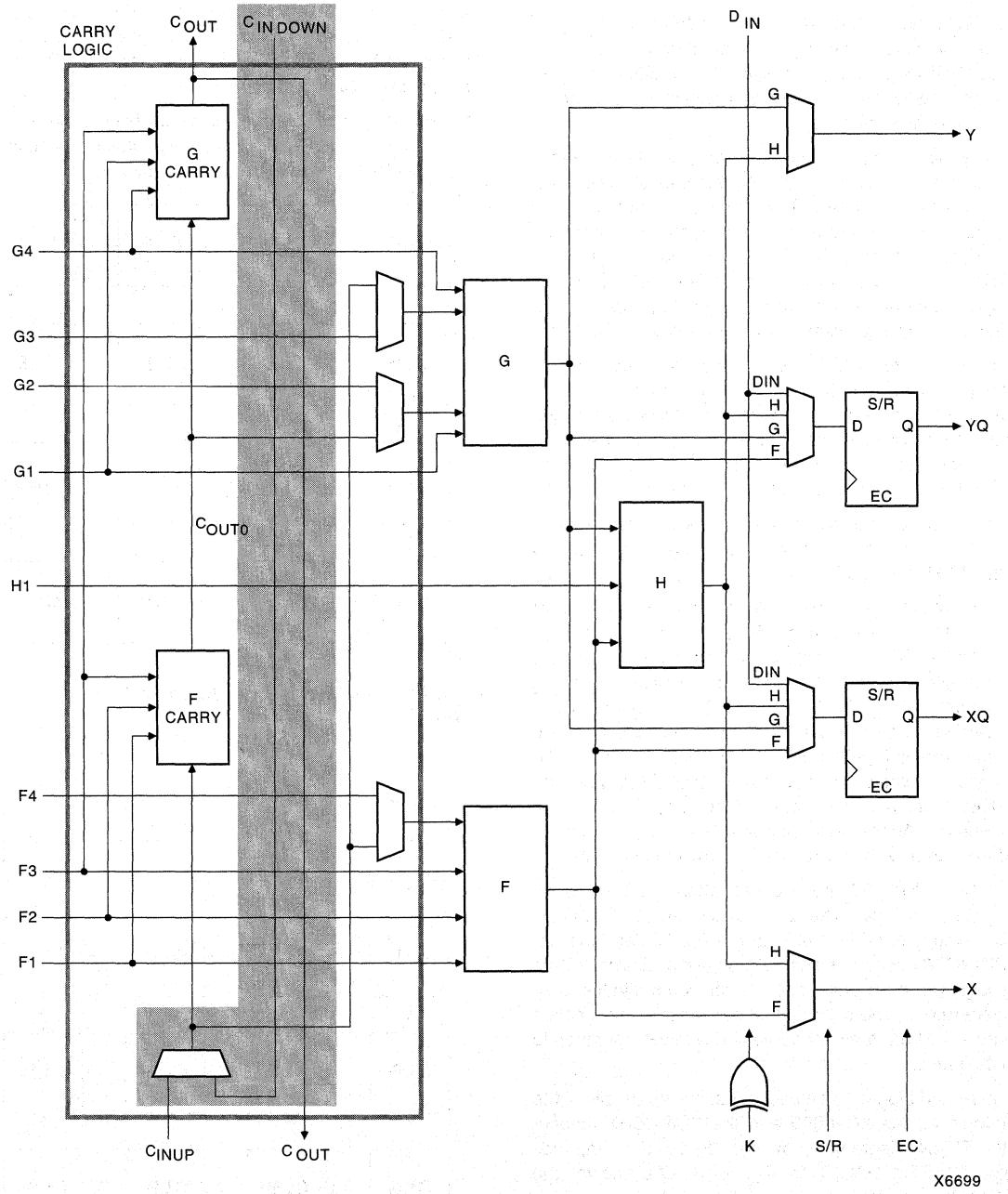


Figure 13: Fast Carry Logic in XC4000E CLB (shaded area not present in XC4000EX)

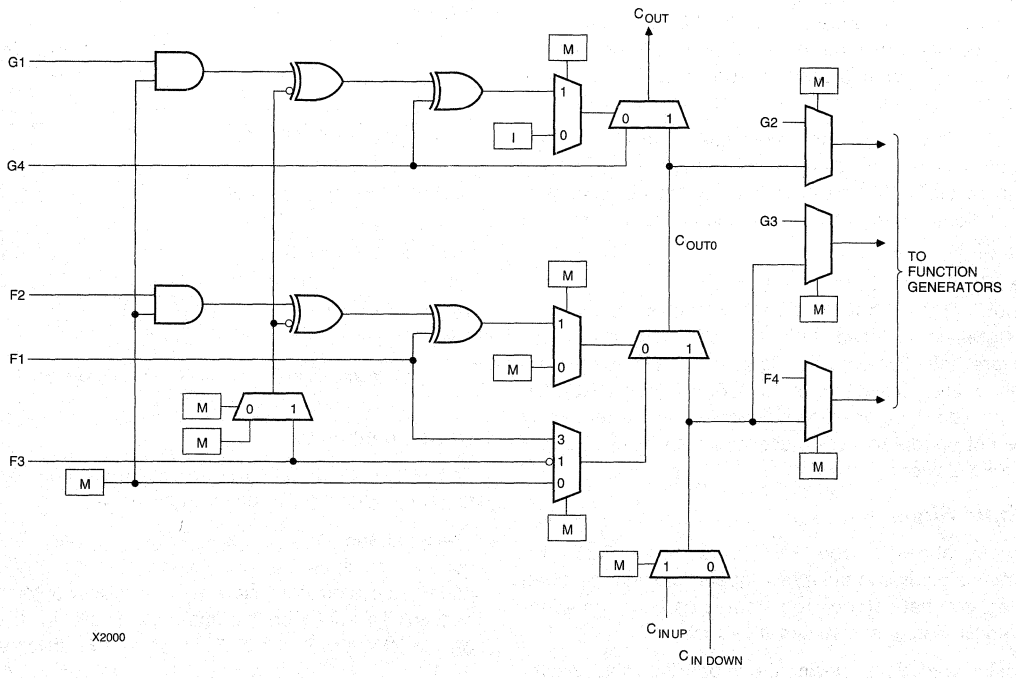


Figure 14: Detail of XC4000E Dedicated Carry Logic

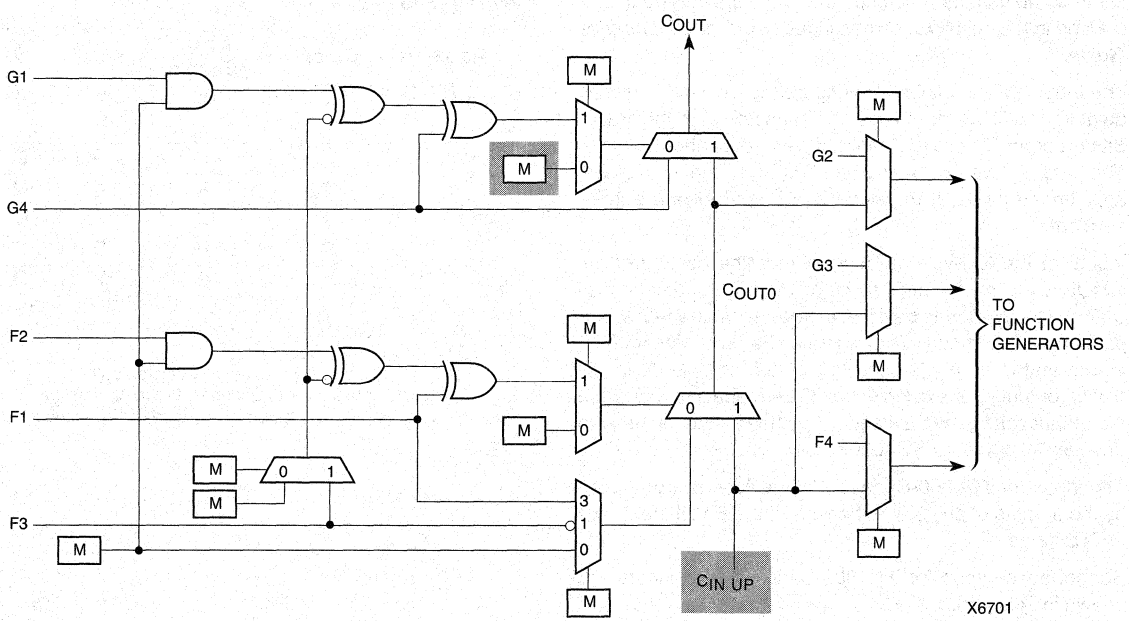


Figure 15: Detail of XC4000EX Dedicated Carry Logic (shaded areas show differences from XC4000E carry logic)

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

Figure 16 shows a simplified block diagram of the XC4000E IOB. A more complete diagram of the XC4000E IOB can be found in Figure 42 on page 51, in the "Boundary Scan" section. Figure 42 includes the boundary scan logic in the IOB.

Figure 17 shows a simplified block diagram of the XC4000EX IOB. The XC4000EX IOB contains some special features not included in the XC4000E IOB. These features are highlighted in Figure 17, and discussed throughout this section. When XC4000EX special features are discussed, they are clearly identified in the text. Any feature not so identified is present in both XC4000E and XC4000EX devices.

IOB Input Signals

Two paths, labeled I1 and I2 in Figure 16 and Figure 17, bring input signals into the array. Inputs also connect to an input register that can be programmed as either an edge-triggered flip-flop or a level-sensitive latch.

The choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are available, and some combinations of latches and flip-flops can be implemented in a single IOB, as described in the *XACT Libraries Guide*.

The inputs can be globally configured for either TTL (1.2V, default) or CMOS thresholds, using an option in the MakeBits program. There is a slight hysteresis of about 300mV. The output levels are also configurable; the two global adjustments of input threshold and output level are independent.

Inputs of the low-voltage devices *must* be configured as CMOS at all times. They can be driven by the outputs of all 5-Volt XC4000-Series devices, provided that the 5-Volt outputs are in TTL mode. They can also be driven by any TTL output that does not exceed 3.7 V. 5-Volt XC3000-family device outputs, for example, are TTL-compatible, but since the output voltage can exceed 3.7 V, they cannot be used to drive an XC4000L or XC4000XL input.

The inputs of XC4000-Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC4000-Series device inputs are shown in Table 10.

Table 10: Supported Sources for XC4000-Series Device Inputs

Source	XC4000-Series Inputs		
	3.3 V, CMOS	5 V, TTL	5 V, CMOS
Any device, Vcc = 3.3 V, CMOS outputs	√	√	Unreliable Data
XC4000-Series, Vcc = 5 V, TTL outputs	√	√	
Any device, Vcc = 5 V, TTL outputs (Voh ≤ 3.7 V)	√	√	
Any device, Vcc = 5 V, CMOS outputs	Danger[1]	√	√

1. Acceptable for XC4000XL if the designated 5-Volt supply pad (V_{TT}) is tied to 5V.

Registered Inputs

The I1 and I2 signals that exit the block can each carry either the direct or registered input signal.

The input and output storage elements in each IOB have a common clock enable input, which, through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC pin on the XC4000-Series CLB. It cannot be inverted within the IOB.

The storage element behavior is shown in Table 11.

Table 11: Input Register Functionality (active rising edge is shown)

Mode	Clock	Clock Enable	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop	_/‾	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

X	Don't care
_/‾	Rising edge
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

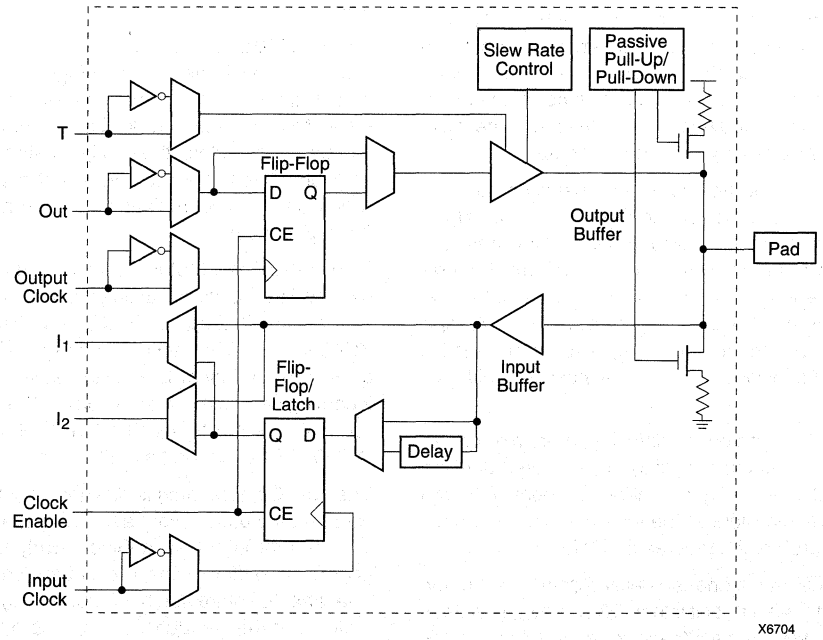


Figure 16: Simplified Block Diagram of XC4000E IOB

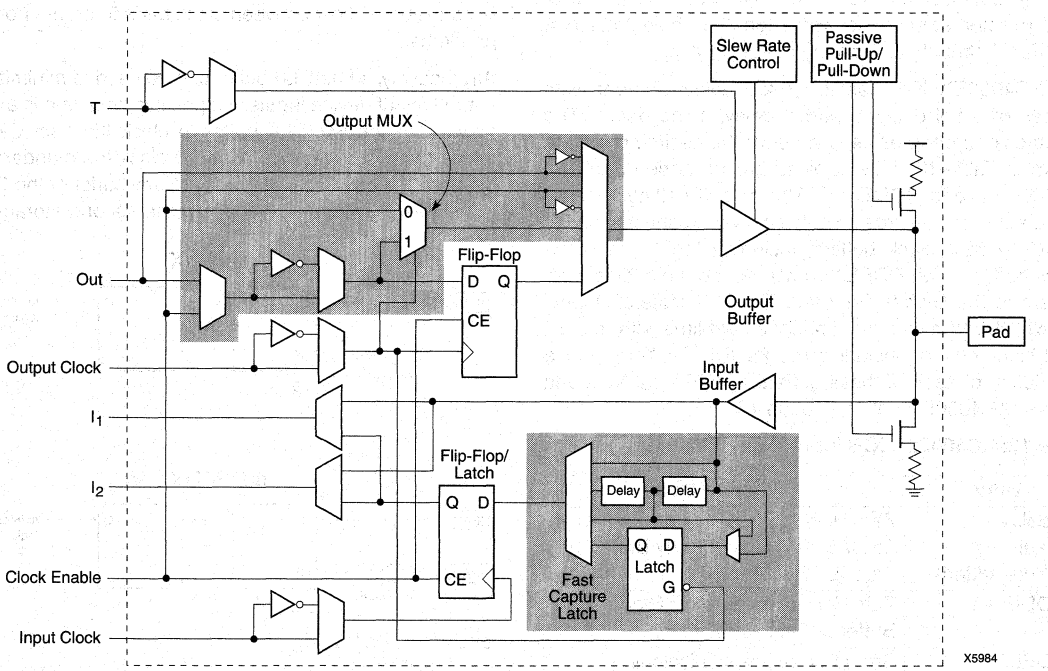


Figure 17: Simplified Block Diagram of XC4000EX IOB (shaded areas indicate differences from XC4000E)

Optional Delay Guarantees Zero Hold Time

The data input to the register can optionally be delayed by several nanoseconds. With the delay enabled, the setup time of the input flip-flop is increased so that normal clock routing does not result in a positive hold-time requirement. A positive hold time requirement can lead to unreliable, temperature- or processing-dependent operation.

The input flip-flop setup time is defined between the data measured at the device I/O pin and the clock input at the IOB (not at the clock pin). Any routing delay from the device clock pin to the clock input of the IOB must, therefore, be subtracted from this setup time to arrive at the real setup time requirement relative to the device pins. A short specified setup time might, therefore, result in a negative setup time at the device pins, i.e., a positive hold-time requirement.

When a delay is inserted on the data line, more clock delay can be tolerated without causing a positive hold-time requirement. Sufficient delay eliminates the possibility of a data hold-time requirement at the external pin. The maximum delay is therefore inserted as the default.

The XC4000E IOB has a one-tap delay element: either the delay is inserted (default), or it is not. The delay guarantees a zero hold time with respect to clocks routed through any of the XC4000E global clock buffers. (See "Global Nets and Buffers (XC4000E only)" on page 41 for a description of the global clock buffers in the XC4000E.) For a shorter input register setup time, with non-zero hold, attach a NODELAY attribute or property to the flip-flop.

The XC4000EX IOB has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The attributes or properties used to select the desired delay are shown in Table 12. The choices are no added attribute, MEDDELAY, and NODELAY. The default setting, with no added attribute, ensures no hold time with respect to any of the XC4000EX clock buffers, including the Global Low-Skew buffers. MEDDELAY ensures no hold time with respect to the Global Early and FastCLK buffers. Inputs with NODELAY may have a positive hold time with respect to all clock buffers, including the FastCLK buffers. For a description of each of these buffers, see "Global Nets and Buffers (XC4000EX only)" on page 43.

Table 12: XC4000EX IOB Input Delay Element

Value	When to Use
full delay (default, no attribute added)	Zero Hold with respect to Global Low-Skew Buffer, Global Early Buffer, or FastCLK Buffer
MEDDELAY	Zero Hold with respect to Global Early Buffer or FastCLK Buffer
NODELAY	Short Setup, positive Hold time

Additional Input Latch for Fast Capture (XC4000EX only)

The XC4000EX IOB has an additional optional latch on the input. This latch, as shown in Figure 17, is clocked by the output clock — the clock used for the output flip-flop — rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the very fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To use this Fast Capture technique, drive the output clock pin (the Fast Capture latching signal) from the output of one of the Global Early or FastCLK buffers supplied in the XC4000EX. The second storage element should be clocked by a Global Low-Skew buffer, to synchronize the incoming data to the internal logic. (See Figure 18.) These special buffers are described in "Global Nets and Buffers (XC4000EX only)" on page 43.

The Fast Capture latch is designed primarily for use with a Global Early buffer. For Fast Capture, a single clock signal is routed through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) The Fast Capture latch is clocked by the Global Early buffer, and the standard IOB flip-flop or latch is clocked by the Global Low-Skew buffer. This mode is the safest way to use the Fast Capture latch, because the clock buffers on both storage elements are driven by the same pad. There is no external skew between clock pads to create potential problems.

Alternatively, a FastCLK buffer can be used to minimize the setup time of device inputs, if a positive hold time is acceptable. Use the FastCLK buffer to clock the Fast Capture latch, and a slower clock buffer to clock the standard IOB flip-flop or latch. Either the Global Early buffer or the Global Low-Skew buffer can be used for the second storage ele-

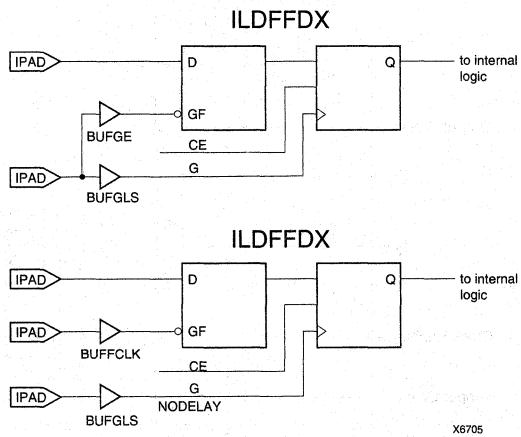


Figure 18: Examples Using XC4000EX Fast Capture Latch

ment, but whichever one is used should be the same clock as the related internal logic. Since the FastCLK pads are different from the Global Early and Global Low-Skew pads, care must be taken to ensure that skew external to the device does not create internal timing difficulties.

To place the Fast Capture latch in a design, use one of the special library symbols, ILDFFDX or ILDFLDX. ILDFFDX is a transparent-Low Fast Capture latch followed by an active-High input flip-flop. ILDFLDX is a transparent-Low Fast Capture latch followed by a transparent-High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB. If a single BUFG output is used to drive both clock inputs, the software automatically runs the clock through both a Global Low-Skew buffer and a Global Early buffer, and clocks the Fast Capture latch appropriately.

Figure 17 on page 25 also shows a two-tap delay on the input. By default, if the Fast Capture latch is used, the Xilinx software assumes a Global Early buffer is driving the clock, and selects MEDDELAY to ensure a zero hold time. This default can be overridden to remove the delay, if FastClk is used, by attaching a NODELAY attribute or property to the ILDFFD or ILDFLD latch. Select the desired delay based on the discussion in the previous subsection.

IOB Output Signals

Output signals can be optionally inverted within the IOB, and can pass directly to the pad or be stored in an edge-triggered flip-flop. The functionality of this flip-flop is shown in Table 13.

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB.

The 4-mA maximum output current specification of many FPGAs often forces the user to add external buffers, which are especially cumbersome on bidirectional I/O lines. The XC4000E and XC4000EX devices solve many of these problems by providing a guaranteed output sink current of 12 mA. Two adjacent outputs can be interconnected externally to sink up to 24 mA. (XC4000L and XC4000XL outputs can sink up to 4 mA, and two adjacent XC4000L and XC4000XL outputs can sink up to 8 mA.) The XC4000E and XC4000EX FPGAs can thus directly drive buses on a printed circuit board.

Table 13: Output Flip-Flop Functionality (active rising edge is shown)

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	_/‾	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
_/‾	Rising edge
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

By default, the output pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc. Alternatively, the outputs can be globally configured as CMOS drivers, with p-channel pull-up transistors pulling to Vcc. This MakeBits option applies to all outputs on the device. It is not individually programmable.

Outputs of low-voltage devices *must* be configured as CMOS at all times. They can drive the inputs of any 5-Volt device with TTL-compatible thresholds.

Any XC4000-Series 5-Volt device with its outputs configured in TTL mode can drive the inputs of any typical 3.3-Volt device. (For a detailed discussion of how to interface between 5 V and 3.3 V devices, see the 3V Products section of *The Programmable Logic Data Book*.)

Supported destinations for XC4000-Series device outputs are shown in Table 14.

Table 14: Supported Destinations for XC4000-Series Outputs

Destination	XC4000-Series Outputs		
	3.3 V, CMOS	5 V, TTL	5 V, CMOS
Any typical device, Vcc = 3.3 V, CMOS-threshold inputs	√	√	some[1]
Any device, Vcc = 5 V, TTL-threshold inputs	√	√	√
Any device, Vcc = 5 V, CMOS-threshold inputs	Unreliable Data		√

1. Only if destination device has 5-V tolerant inputs

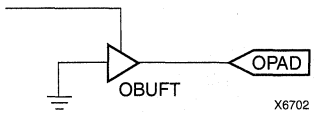


Figure 19: Open-Drain Output

An output can be configured as open-drain (open-collector) by placing an OBUFT symbol in a schematic or HDL code, then tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground. (See Figure 19.)

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

For XC4000E devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is 200 pF for all package pins between each Power/Ground pin pair. For XC4000EX devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce. Therefore, the maximum total capacitive load is 300 pF between each external Power/Ground pin pair. Maximum loading may vary for the low-voltage devices.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC4000E devices and 600 pF for XC4000EX devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC4000 Series.

XC4000-Series devices have a feature called "Soft Start-up," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Global Three-State

A separate Global 3-State line (not shown in Figure 16 or Figure 17) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. This global net (GTS) does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Using GTS is similar to GSR. See Figure 2 on page 13 for details.

Alternatively, GTS can be driven from any internal node.

Output Multiplexer/2-Input Function Generator (XC4000EX only)

As shown in Figure 17 on page 25, the output path in the XC4000EX IOB contains an additional multiplexer not available in the XC4000E IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass-gate, AND-gate, OR-gate, or XOR-gate, with 0, 1, or 2 inverted inputs. The logic used to implement these functions is shown in the upper gray area of Figure 17.

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad; effectively doubling the number of device outputs without requiring a larger, more expensive package.

When the MUX is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with either a FastCLK or Global Early buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe driven by a FastCLK buffer, as shown in Figure 20. The critical-path pin-to-pin delay of this circuit is less than 6 nanoseconds. (This value may not be achievable in XC4000XL devices.)

As shown in Figure 17, the IOB input pins Out, Output Clock, and Clock Enable have different delays and different flexibilities regarding polarity. Additionally, Output Clock sources are more limited than the other inputs. Therefore, the Xilinx software does not move logic into the IOB function generators unless explicitly directed to do so.

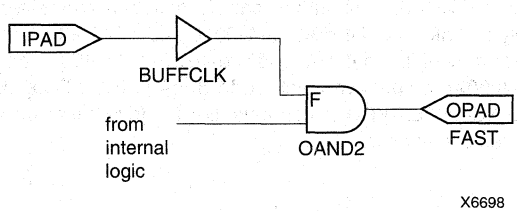


Figure 20: Fast Pin-to-Pin Path in XC4000E

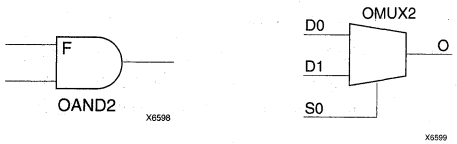


Figure 21: Output AND and MUX Symbols in XC4000EX IOB

The user can specify that the IOB function generator be used, by placing special library symbols beginning with the letter "O." For example, a 2-input AND-gate in the IOB function generator is called OAND2. Use the symbol input pin labelled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in Figure 21.

Other IOB Options

There are a number of other programmable options in the XC4000-Series IOB.

Pull-up and Pull-down Resistors

Programmable pull-up and pull-down resistors are useful for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to Vcc. The configurable pull-down resistor is an n-channel transistor that pulls to Ground.

The value of these resistors is 50 kΩ – 100 kΩ. This high value makes them unsuitable as wired-AND pull-up resistors.

The pull-up resistors for most user-programmable IOBs are active during the configuration process. See Table 24 on page 78 for a list of pins with pull-ups active before and during configuration.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

Independent Clocks

Separate clock signals are provided for the input and output flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent, except that in the XC4000EX, the Fast Capture latch shares an IOB input with the output clock pin.

Early Clock for IOBs (XC4000EX only)

Special early clocks are available for IOBs. These clocks are sourced by the same sources as the Global Low-Skew buffers, but are separately buffered. They have fewer loads and therefore less delay. The early clock can drive either the IOB output clock or the IOB input clock, or both. The early clock allows fast capture of input data, and fast clock-to-output on output data. The Global Early buffers that drive these clocks are described in "Global Nets and Buffers (XC4000EX only)" on page 43.

Fast Clock for IOBs (XC4000EX only)

Very fast clocks driven by FastCLK buffers are also available for IOBs. These clocks are sourced by semi-dedicated pads—the pads can be used as general I/O if not used to drive FastCLK buffers. There are two FastCLK buffers on the left edge, and two on the right edge of the device. They provide the fastest method of reaching the IOB clock pins. The FastCLK buffer can drive either the IOB output clock or the IOB input clock, or both. These buffers allow the fastest possible setup times and clock-to-output times. The FastCLK buffers are described in "Global Nets and Buffers (XC4000EX only)" on page 43.

Global Set/Reset

As with the CLB registers, the Global Set/Reset signal (GSR) can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops. The choice of set or clear applies to both the initial state of the flip-flop and the response to the Global Set/Reset pulse. See "Global Set/Reset" on page 13 for a description of how to use GSR.

JTAG Support

Embedded logic attached to the IOBs contains test structures compatible with IEEE Standard 1149.1 for boundary scan testing, permitting easy chip and board-level testing. More information is provided in "Boundary Scan" on page 50.

Three-State Buffers

A pair of 3-state buffers is associated with each CLB in the array. (See Figure 27 on page 34.) These 3-state buffers can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources. Programmable pull-up resistors attached to these longlines help to implement a wide wired-AND function.

The buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in Table 15.

Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array. (See Figure 33 on page 39.)

The horizontal longlines driven by the 3-state buffers have a weak keeper at each end. This circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Special longlines running along the perimeter of the array can be used to wire-AND signals coming from nearby IOBs or from internal longlines. These longlines form the wide edge decoders discussed in "Wide Edge Decoders" on page 31.

Three-State Buffer Modes

The 3-state buffers can be configured in three modes:

- Standard 3-state buffer
- Wired-AND with input on the I pin
- Wired OR-AND

Standard 3-State Buffer

All three pins are used. Place the library element BUFT. Connect the input to the I pin and the output to the O pin. The T pin is an active-High 3-state (i.e. an active-Low enable). Tie the T pin to Ground to implement a standard buffer.

Wired-AND with Input on the I Pin

The buffer can be used as a Wired-AND. Use the WAND1 library symbol, which is essentially an open-drain buffer. WAND4, WAND8, and WAND16 are also available. See the *XACT Libraries Guide* for further information.

The T pin is internally tied to the I pin. Connect the input to the I pin and the output to the O pin. Connect the outputs of all the WAND1s together and attach a PULLUP symbol.

Wired OR-AND

The buffer can be configured as a Wired OR-AND. A High level on either input turns off the output. Use the WOR2AND library symbol, which is essentially an open-drain 2-input OR gate. The two input pins are functionally equivalent. Attach the two inputs to the I0 and I1 pins and tie the output to the O pin. Tie the outputs of all the WOR2ANDs together and attach a PULLUP symbol.

Three-State Buffer Examples

Figure 22 shows how to use the 3-state buffers to implement a wired-AND function. When all the buffer inputs are High, the pull-up resistor(s) provide the High output.

Figure 23 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active-High 3-state (T) is identical to an active-Low output enable, as shown in Table 15.

Table 15: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN

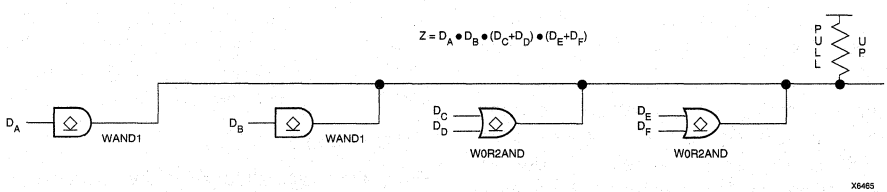


Figure 22: Open-Drain Buffers Implement a Wired-AND Function

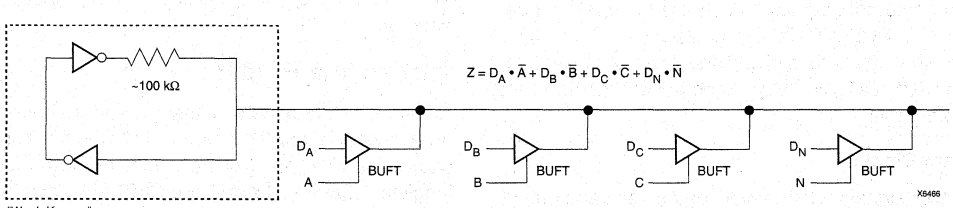


Figure 23: 3-State Buffers Implement a Multiplexer

Wide Edge Decoders

Dedicated decoder circuitry boosts the performance of wide decoding functions. When the address or data field is wider than the function generator inputs, FPGAs need multi-level decoding and are thus slower than PALs. XC4000-Series CLBs have nine inputs. Any decoder of up to nine inputs is, therefore, compact and fast. However, there is also a need for much wider decoders, especially for address decoding in large microprocessor systems.

An XC4000-Series FPGA has four programmable decoders located on each edge of the device. The inputs to each decoder are any of the IOB I1 signals on that edge plus one local interconnect per CLB row or column. Each row or column of CLBs provides up to three variables or their compliments., as shown in Figure 24. Each decoder generates a High output (resistor pull-up) when the AND condition of the selected inputs, or their complements, is true. This is analogous to a product term in typical PAL devices.

Each of these wired-AND gates is capable of accepting up to 42 inputs on the XC4005E and 72 on the XC4013E. There are up to 96 inputs for each decoder on the XC4028EX and 132 on the XC4052EX. The decoders may also be split in two when a larger number of narrower decoders are required, for a maximum of 32 decoders per device.

The decoder outputs can drive CLB inputs, so they can be combined with other logic to form a PAL-like AND/OR structure. The decoder outputs can also be routed directly to the chip outputs. For fastest speed, the output should be on the same chip edge as the decoder. Very large PALs can be emulated by ORing the decoder outputs in a CLB. This decoding feature covers what has long been considered a weakness of older FPGAs. Users often resorted to external PALs for simple but fast decoding functions. Now, the dedicated decoders in the XC4000-Series device can implement these functions fast and efficiently.

To use the wide edge decoders, place one or more of the WAND library symbols (WAND1, WAND4, WAND8, WAND16). Attach a DECODE attribute or property to each WAND symbol. Tie the outputs together and attach a PULLUP symbol. Location attributes or properties such as L (left edge) or TR (right half of top edge) should also be used to ensure the correct placement of the decoder inputs.

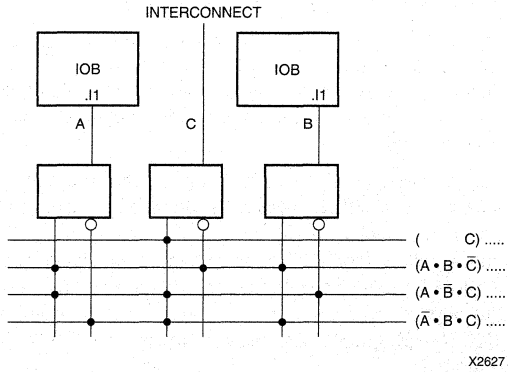


Figure 24: XC4000-Series Edge Decoding Example

On-Chip Oscillator

XC4000-Series devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration modes. The oscillator runs at a nominal 8 MHz frequency that varies with process, Vcc, and temperature. The output frequency falls between 4 and 10 MHz. (The oscillator operates more slowly at lower voltages. The output frequency may be reduced by as much as 10% for low-voltage devices.)

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8 MHz clock, plus any two of 500 kHz, 16kHz, 490Hz and 15Hz (up to 10% lower for low-voltage devices). These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code (see Figure 25).

The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

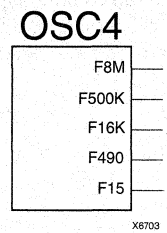


Figure 25: XC4000-Series Oscillator Symbol

Programmable Interconnect

All internal connections are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing resources is provided to achieve efficient automated routing.

The XC4000E and XC4000EX share a basic interconnect structure. XC4000EX devices, however, have additional routing not available in the XC4000E. The extra routing resources allow high utilization in high-capacity devices. All XC4000EX-specific routing resources are clearly identified throughout this section. Any resources not identified as XC4000EX-specific are present in all XC4000-Series devices.

This section describes the varied routing resources available in XC4000-Series devices. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design.

Interconnect Overview

There are several types of interconnect.

- CLB routing is associated with each row and column of the CLB array.
- IOB routing forms a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the internal logic blocks.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

Five interconnect types are distinguished by the relative length of their segments: single-length lines, double-length lines, quad and octal lines (XC4000EX only), and longlines. In the XC4000EX, direct connects allow fast data flow between adjacent CLBs, and between IOBs and CLBs.

Extra routing is included in the IOB pad ring. The XC4000EX also includes a ring of octal interconnect lines near the IOBs to improve pin-swapping and routing to locked pins.

XC4000E devices include two types of global buffers, while XC4000EX devices have three different types. These global buffers have different properties, and are intended for different purposes. They are discussed in detail later in this section.

CLB Routing Connections

A high-level diagram of the routing resources associated with one CLB is shown in Figure 26. The shaded arrows represent routing present only in XC4000EX devices.

Table 16 shows how much routing of each type is available in XC4000E and XC4000EX CLB arrays. Clearly, very large designs, or designs with a great deal of interconnect, will route more easily in the XC4000EX. Smaller XC4000E designs, typically requiring significantly less interconnect, do not require the additional routing.

Figure 27 on page 34 is a detailed diagram of both the XC4000E and the XC4000EX CLB, with associated routing. The shaded square is the programmable switch matrix, present in both the XC4000E and the XC4000EX. The L-shaped shaded area is present only in XC4000EX devices. As shown in the figure, the XC4000EX block is essentially an XC4000E block with additional routing.

CLB inputs and outputs are distributed on all four sides, providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation.

Table 16: Routing per CLB in XC4000-Series Devices

	XC4000E		XC4000EX	
	Vertical	**Horizontal**	**Vertical**	**Horizontal**
Singles	8	8	8	8
Doubles	4	4	4	4
Quads	0	0	12	12
Longlines	6	6	10	6
Direct Connects	0	0	2	2
Globals	4	0	8	0
Carry Logic	2	0	1	0
Total	24	18	45	32

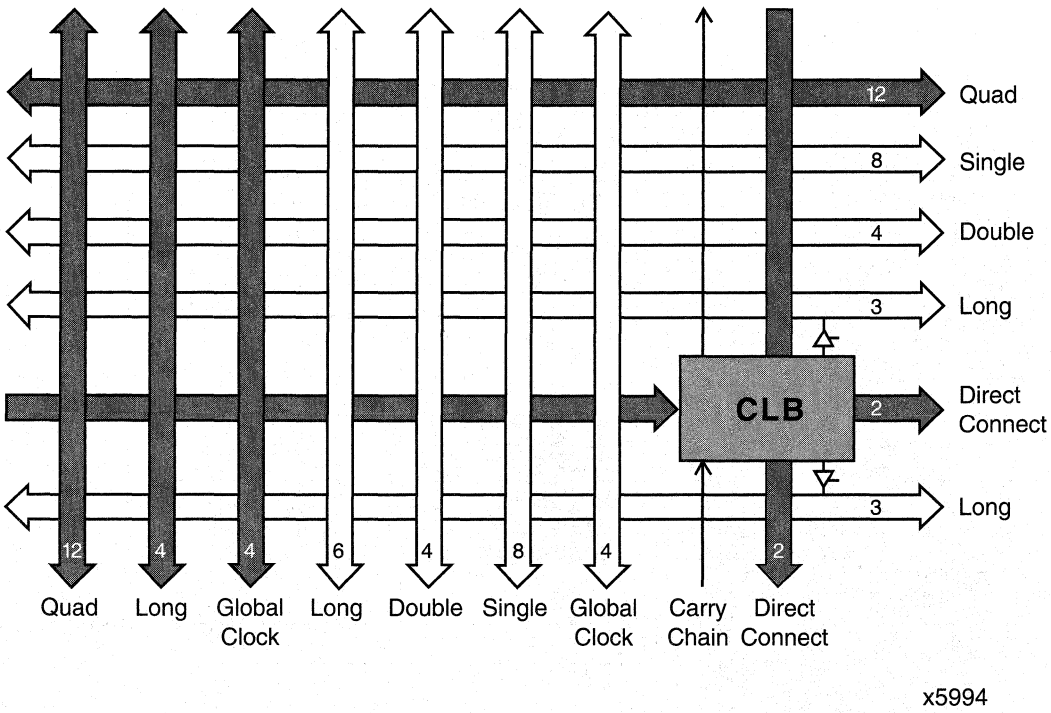


Figure 26: High-Level Routing Diagram of XC4000-Series CLB (shaded arrows indicate XC4000EX only)

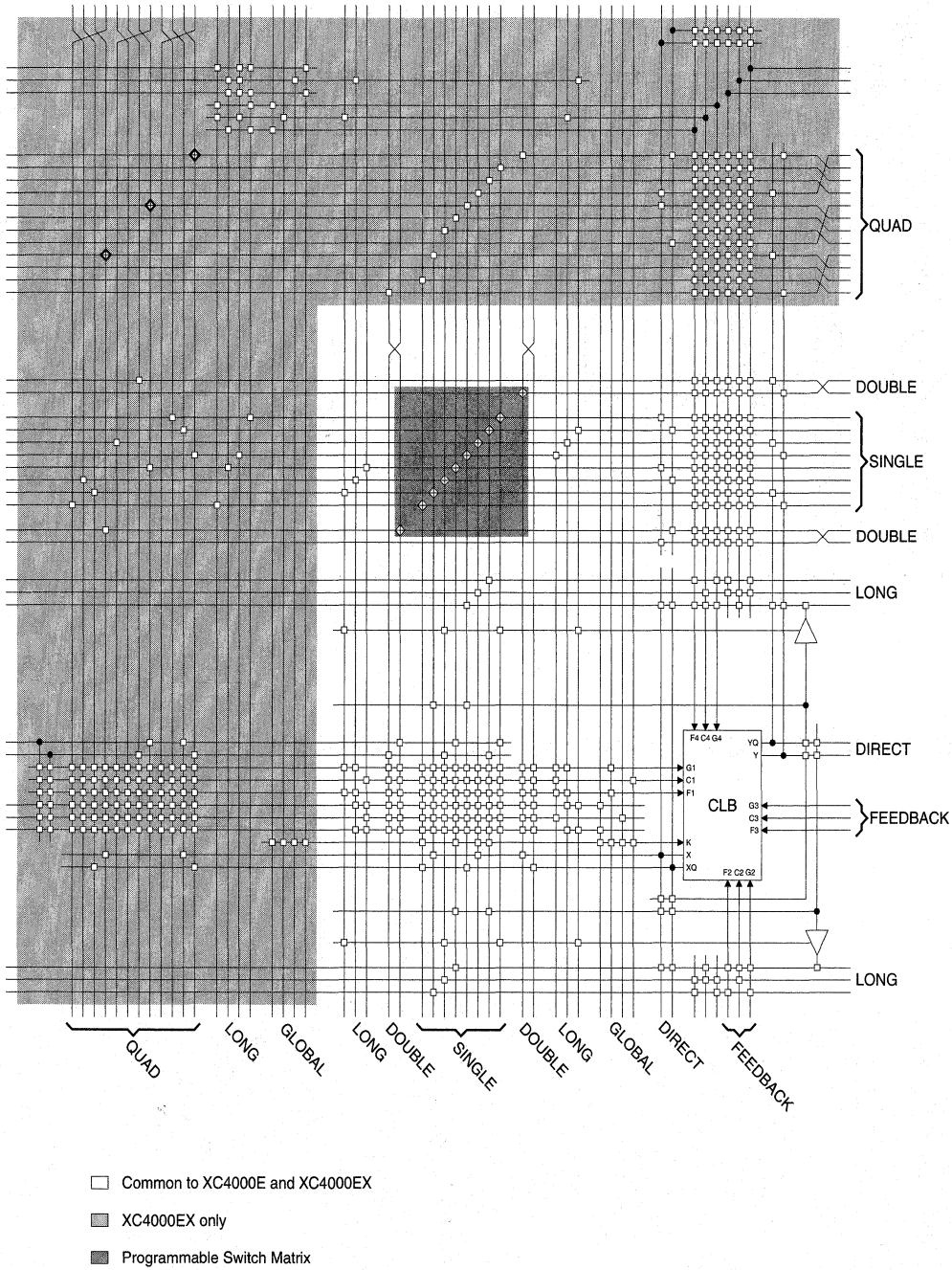


Figure 27: Detail of Programmable Interconnect Associated with XC4000-Series CLB

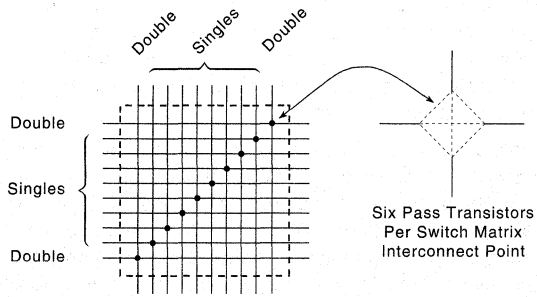


Figure 28: Programmable Switch Matrix (PSM)

Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each switch matrix consists of programmable pass transistors used to establish connections between the lines (see Figure 28).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and a column of CLBs.

Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 29. Routing connectivity is shown in Figure 27.

Single-length lines incur a delay whenever they go through a switching matrix. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a switch matrix. Double-length lines are grouped in pairs with the switch matrices staggered, so that each line goes through a switch matrix at every other row or column of CLBs (see Figure 29).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility. Double-length lines are connected by way of the programmable switch matrices. Routing connectivity is shown in Figure 27.

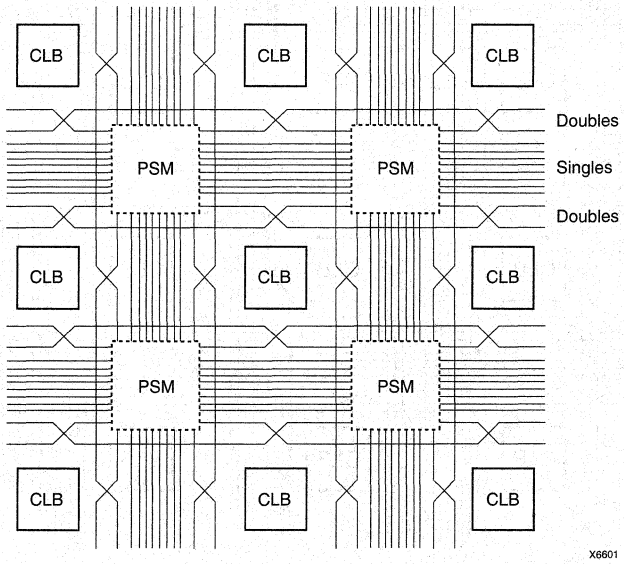


Figure 29: Single- and Double-Length Lines, with Programmable Switch Matrices (PSMs)

Quad Lines (XC4000EX only)

XC4000EX devices also include twelve vertical and twelve horizontal quad lines per CLB row and column. Quad lines are four times as long as the single-length lines. They are interconnected via buffered switch matrices (shown as diamonds in Figure 27 on page 34). Quad lines run past four CLBs before entering a buffered switch matrix. They are grouped in fours, with the buffered switch matrices staggered, so that each line goes through a buffered switch matrix at every fourth CLB location in that row or column. (See Figure 30.)

The buffered switch matrixes have four pins, one on each edge. All of the pins are bidirectional. Any pin can drive any or all of the other pins.

Each buffered switch matrix contains one buffer and six pass transistors. It resembles the programmable switch matrix shown in Figure 28, with the addition of a programmable buffer. There can be up to two independent inputs and up to two independent outputs. Only one of the independent inputs can be buffered.

The place and route software automatically uses the timing requirements of the design to determine whether or not a quad line signal should be buffered. A heavily loaded signal is typically buffered, while a lightly loaded one is not. One scenario is to alternate buffers and pass transistors. This allows both vertical and horizontal quad lines to be buffered at alternating buffered switch matrices.

Due to the buffered switch matrices, quad lines are very fast. They provide the fastest available method of routing heavily loaded signals for long distances across the device.

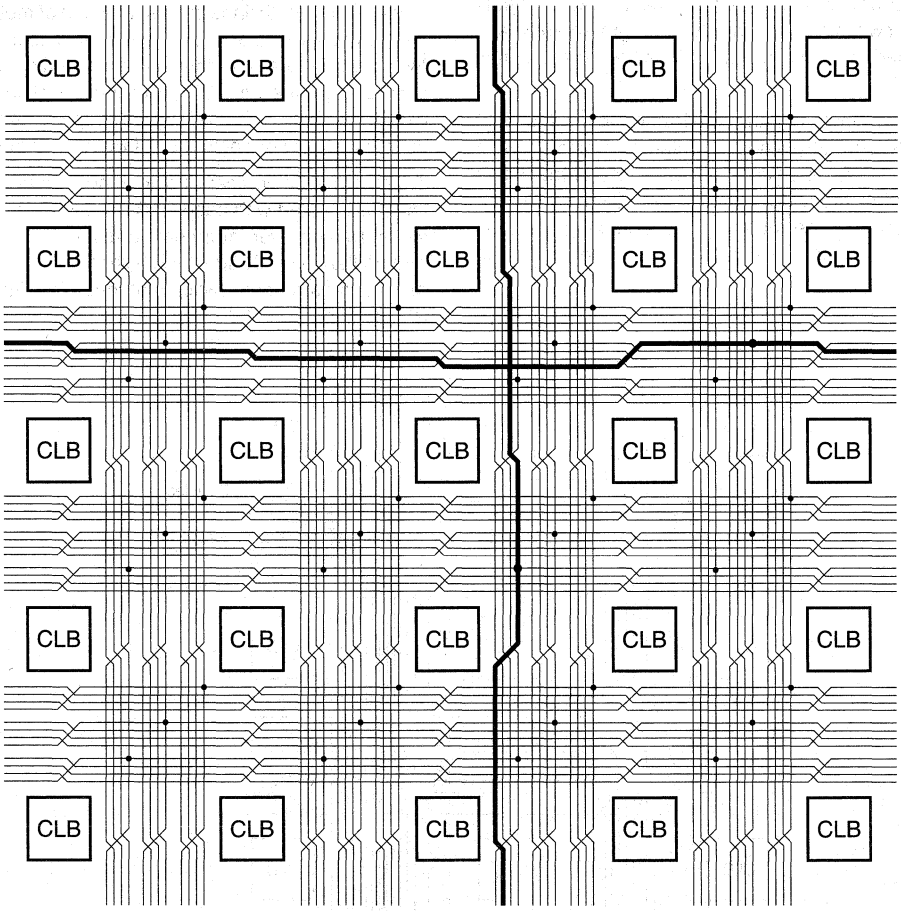


Figure 30: Quad Lines (XC4000EX only)

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances. In XC4000EX devices, quad lines are preferred for critical nets, because the buffered switch matrices make them faster for high fan-out nets.

Two horizontal longlines per CLB can be driven by 3-state or open-drain drivers (TBUFs). They can therefore implement unidirectional or bidirectional buses, wide multiplexers, or wired-AND functions. (See "Three-State Buffers" on page 29 for more details.)

Each horizontal longline driven by TBUFs has either two (XC4000E) or eight (XC4000EX) pull-up resistors. To activate these resistors, attach a PULLUP symbol to the longline net. The software automatically activates the appropriate number of pull-ups. There is also a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Each XC4000E longline has a programmable splitter switch at its center, as does each XC4000EX longline driven by TBUFs. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Each XC4000EX longline not driven by TBUFs has a buffered programmable splitter switch at the 1/4, 1/2, and 3/4 points of the array. Due to the buffering, XC4000EX longline performance does not deteriorate with the larger array sizes. If the longline is split, the resulting partial longlines are independent.

Routing connectivity of the longlines is shown in Figure 27 on page 34.

Direct Interconnect (XC4000EX only)

The XC4000EX offers two direct, efficient and fast connections between adjacent CLBs. These nets facilitate a data flow from the left to the right side of the device, or from the top to the bottom, as shown in Figure 31. Signals routed on the direct interconnect exhibit minimum interconnect propagation delay and use no general routing resources.

The direct interconnect is also present between CLBs and adjacent IOBs. Each IOB on the left and top device edges has a direct path to the nearest CLB. Each CLB on the right and bottom edges of the array has a direct path to the nearest two IOBs, since there are two IOBs for each row or column of CLBs.

The place and route software uses direct interconnect whenever possible, to maximize routing resources and minimize interconnect delays.

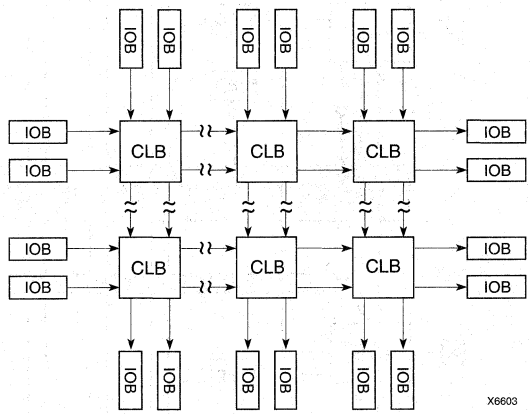


Figure 31: XC4000EX Direct Interconnect

I/O Routing

XC4000-Series devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines spanning two CLBs (four IOBs), and four longlines. Global lines and Wide Edge Decoder lines are provided. XC4000EX devices also include eight octal lines.

A high-level diagram of the VersaRing is shown in Figure 32. The shaded arrows represent routing present only in XC4000EX devices.

Figure 33 is a detailed diagram of the XC4000E and XC4000EX VersaRing. The area shown includes two IOBs. There are two IOBs per CLB row or column, therefore this diagram corresponds to the CLB routing diagram shown in Figure 27 on page 34. The shaded areas represent routing and routing connections present only in XC4000EX devices.

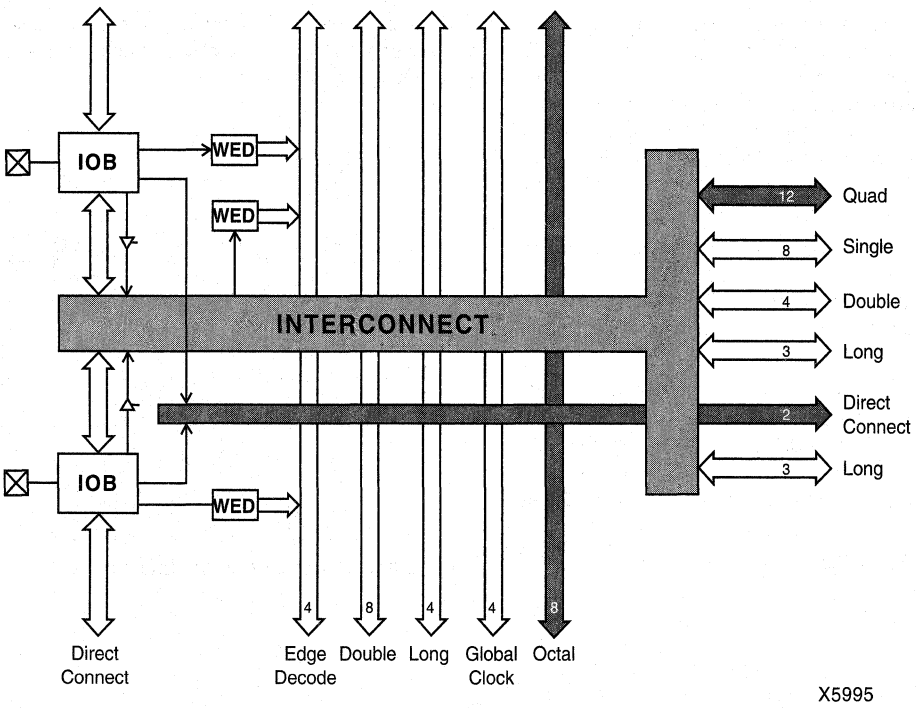


Figure 32: High-Level Routing Diagram of XC4000-Series VersaRing (Left Edge)
WED = Wide Edge Decoder, IOB = I/O Block (shaded arrows indicate XC4000EX only)

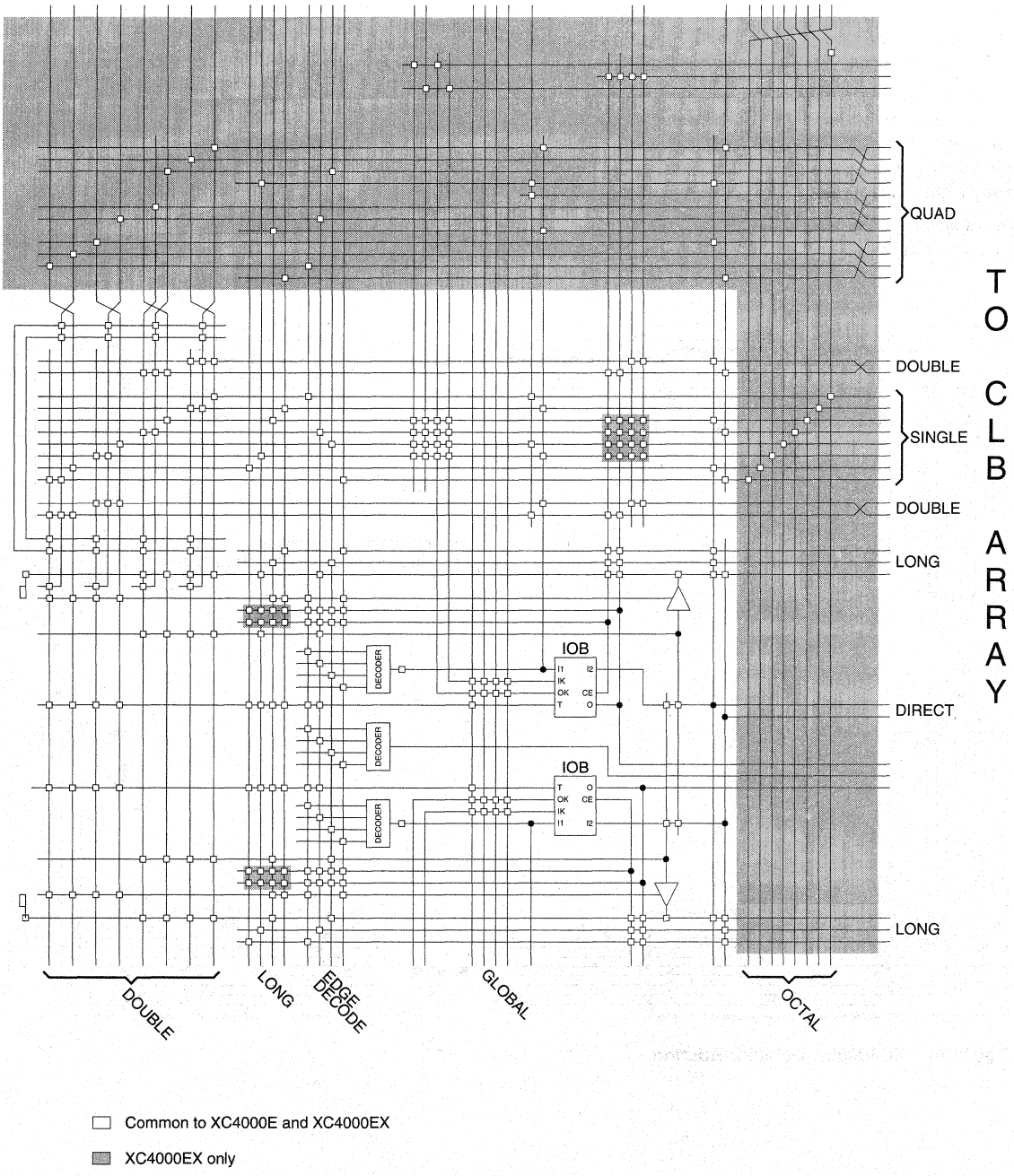


Figure 33: Detail of Programmable Interconnect Associated with XC4000-Series IOB (Left Edge)

Octal I/O Routing (XC4000EX only)

Between the XC4000EX CLB array and the pad ring, eight interconnect tracks provide for versatility in pin assignment and fixed pinout flexibility. (See Figure 34.)

These routing tracks are called octals, because they can be broken every eight CLBs (sixteen IOBs) by a programmable buffer that also functions as a splitter switch. The buffers are staggered, so each line goes through a buffer at every eighth CLB location around the device edge.

The octal lines bend around the corners of the device. The lines cross at the corners in such a way that the segment most recently buffered before the turn has the farthest distance to travel before the next buffer, as shown in Figure 34.

IOB inputs and outputs interface with the octal lines via the single-length interconnect lines. Single-length lines are also used for communication between the octals and double-length lines, quads, and longlines within the CLB array.

Segmentation into buffered octals was found to be optimal for distributing signals over long distances around the device.

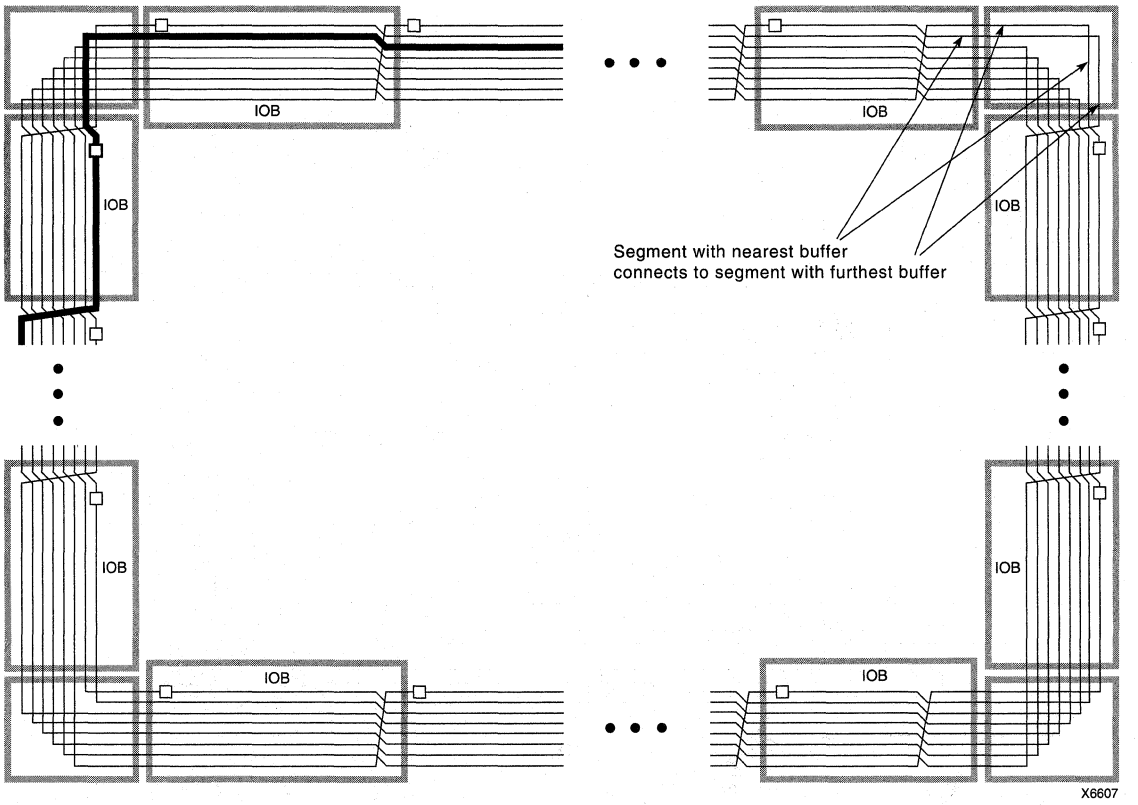


Figure 34: XC4000EX Octal I/O Routing

Global Nets and Buffers

Both the XC4000E and the XC4000EX have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew. The global buffers are described in detail in the following sections. The text descriptions and diagrams are summarized in Table 17. The table shows which CLB and IOB clock pins can be sourced by which global buffers.

In both XC4000E and XC4000EX devices, placement of a library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. The detailed information in these sections is included only for reference.

Global Nets and Buffers (XC4000E only)

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The four global lines can be driven by either of two types of global buffers. The clock pins of every CLB and IOB can also be sourced from local interconnect.

Two different types of clock buffers are available in the XC4000E:

- Primary Global Buffers (BUFGP)
- Secondary Global Buffers (BUFGS)

Four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs.

The Primary Global buffers must be driven by the semi-dedicated pads. The Secondary Global buffers can be sourced by either semi-dedicated pads or internal nets.

Each CLB column has four dedicated vertical Global lines. Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 35. Each corner of the device has one Primary buffer and one Secondary buffer.

IOBs along the left and right edges have four vertical global longlines. Top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), or BUFG (either primary or secondary buffer) element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=L attribute or property to a BUFGS symbol to direct that a buffer be placed in one of the two Secondary Global buffers on the left edge of the device, or a LOC=BL to indicate the Secondary Global buffer on the bottom edge of the device, on the left.

Table 17: Clock Pin Access

	XC4000E		XC4000EX				Local Interconnect
	BUFGP	BUFGS	BUFGLS	L & R BUFGE	T & B BUFGE	BUFFCLK	
All CLBs in Quadrant	√	√	√	√	√		√
All CLBs in Device	√	√	√				√
IOBs on Adjacent Vertical Half Edge	√	√	√	√	√	√	√
IOBs on Adjacent Vertical Full Edge	√	√	√	√			√
IOBs on Adjacent Horizontal Half Edge (Direct)				√			√
IOBs on Adjacent Horizontal Half Edge (through CLB globals)	√	√	√	√	√		√
IOBs on Adjacent Horizontal Full Edge (through CLB globals)	√	√	√				√

L = Left, R = Right, T = Top, B = Bottom

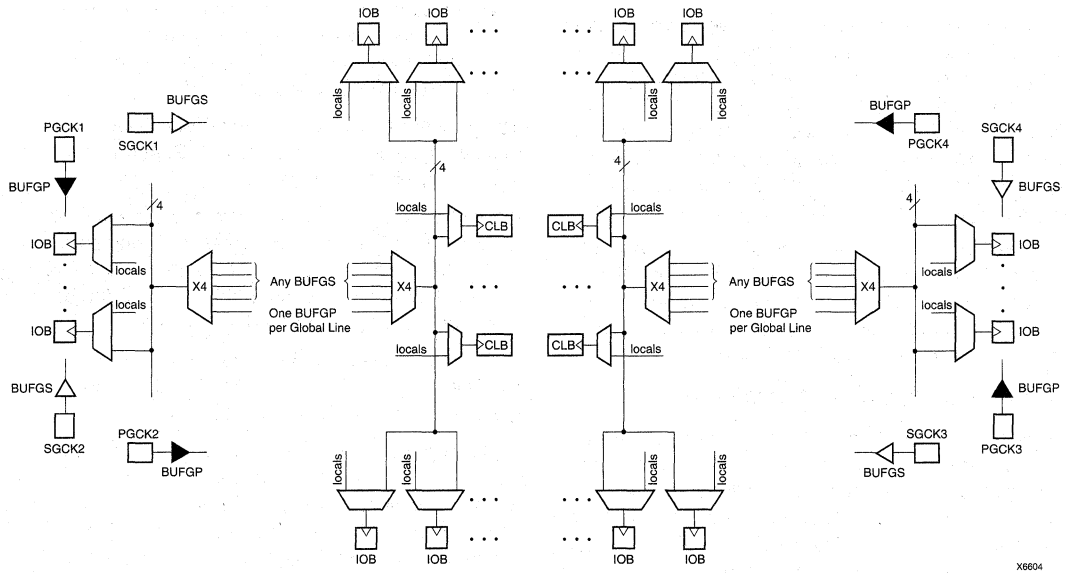


Figure 35: XC4000E Global Net Distribution

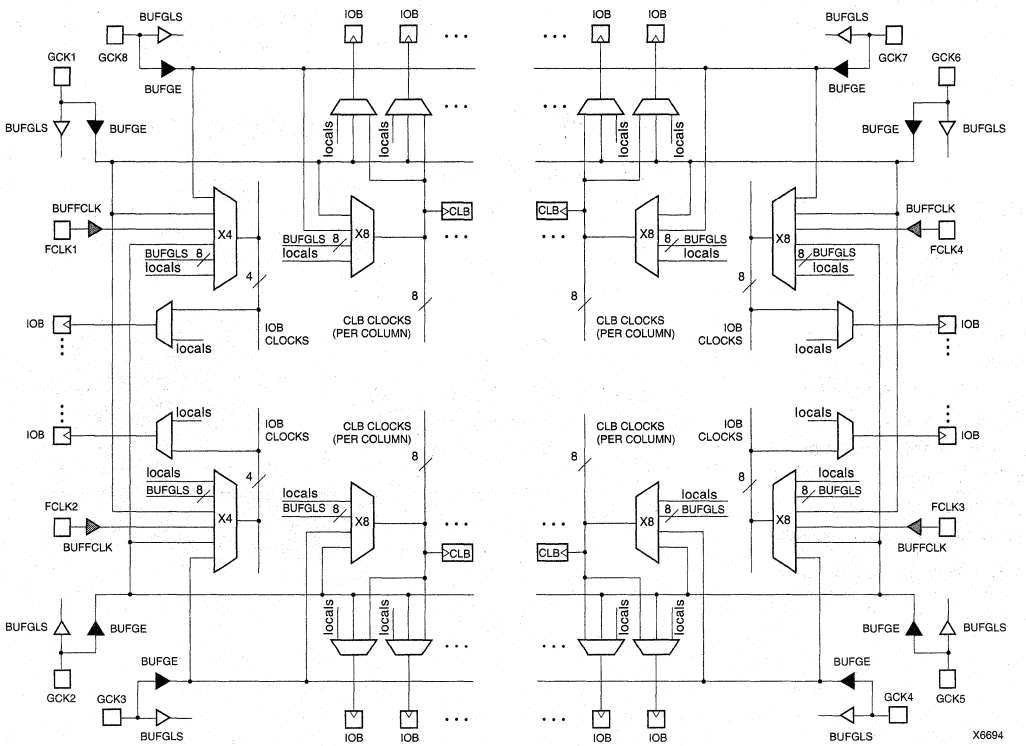


Figure 36: XC4000EX Global Net Distribution

Global Nets and Buffers (XC4000EX only)

Eight vertical longlines in each CLB column are driven by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The global lines are broken in the center of the array, to allow faster distribution and to minimize skew across the whole array. Each half-column global line has its own buffered multiplexer, as shown in Figure 36. The top and bottom global lines cannot be connected across the center of the device, as this connection might introduce unacceptable skew. The top and bottom halves of the global lines must be separately driven — although they can be driven by the same global buffer.

The eight global lines in each CLB column can be driven by either of two types of global buffers. They can also be driven by internal logic, because they can be accessed by single, double, and quad lines at the top, bottom, half, and quarter points. Consequently, the number of different clocks that can be used simultaneously in an XC4000EX device is very large.

There are four global lines feeding the IOBs at the left edge of the device. IOBs along the right edge have eight global lines. There is a single global line along the top and bottom edges with access to the IOBs. All IOB global lines are broken at the center. They cannot be connected across the center of the device, as this connection might introduce unacceptable skew.

IOB global lines can be driven from any of three types of global buffers, or from local interconnect. Alternatively, top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

Three different types of clock buffers are available in the XC4000EX:

- Global Low-Skew Buffers (BUFGLS)
- Global Early Buffers (BUFGE)
- FastCLK Buffers (BUFFCLK)

Global Low-Skew Buffers are the standard clock buffers. They should be used for most internal clocking, whenever a large portion of the device must be driven.

Global Early Buffers are designed to provide a faster clock access, but CLB access is limited to one-fourth of the device. They also facilitate a faster I/O interface.

FastCLK buffers are specifically designed to provide the fastest possible I/O clock. They have only the standard input access to CLBs, through local interconnect.

Figure 36 is a conceptual diagram of the global net structure in the XC4000EX.

Global Early buffers and Global Low-Skew buffers share a single pad. Therefore, the same IPAD symbol can drive one buffer of each type, in parallel. This configuration is particularly useful when using the Fast Capture latches, as described in "IOB Input Signals" on page 24. Paired Global Early and Global Low-Skew buffers share a common input; they cannot be driven by two different signals.

Choosing an XC4000EX Clock Buffer

The clocking structure of the XC4000EX provides a large variety of features. However, it can be simple to use, without understanding all the details. The software automatically handles clocks, along with all other routing, when the appropriate clock buffer is placed in the design. In fact, if a buffer symbol called BUFG is placed, rather than a specific type of buffer, the software even chooses the buffer most appropriate for the design. The detailed information in this section is provided for those users who want a finer level of control over their designs.

If fine control is desired, use the following summary and Table 17 on page 41 to choose an appropriate clock buffer.

- The simplest thing to do is to use a Global Low-Skew buffer.
- If a faster clock path is needed, try a BUFG. The software will first try to use a Global Low-Skew Buffer. If timing requirements are not met, a faster buffer will automatically be used.
- If a single quadrant of the chip is sufficient for the clocked logic, and the timing requires a faster clock than the Global Low-Skew buffer, use a Global Early buffer.
- In special cases, where both external and internal timing have been carefully studied, a FastCLK buffer can be used, for the fastest possible I/O clock path.

Global Low-Skew Buffers

Each corner of the XC4000EX device has two Global Low-Skew buffers. Any of the eight Global Low-Skew buffers can drive any of the eight vertical Global lines in a column of CLBs. In addition, any of the buffers can drive any of the four vertical lines accessing the IOBs on the left edge of the device, and any of the eight vertical lines accessing the IOBs on the right edge of the device. (See Figure 37 on page 44.)

IOBs at the top and bottom edges of the device are accessed through the vertical Global lines in the CLB array, as in the XC4000E. Any Global Low-Skew buffer can, therefore, access every IOB and CLB in the device.

The Global Low-Skew buffers can be driven by either semi-dedicated pads or internal logic.

To use a Global Low-Skew buffer, place a BUFGLS element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGLS be placed in one of the two Global Low-Skew buffers on the top edge of the device, or a LOC=TR to indicate the Global Low-Skew buffer on the top edge of the device, on the right.

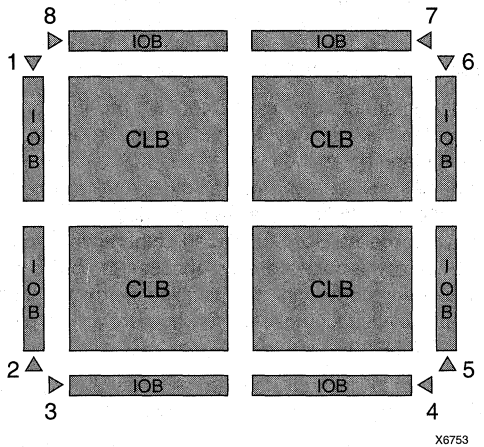


Figure 37: Any BUFGLS (GCK1 - GCK8) Can Drive Any or All Clock Inputs on the Device

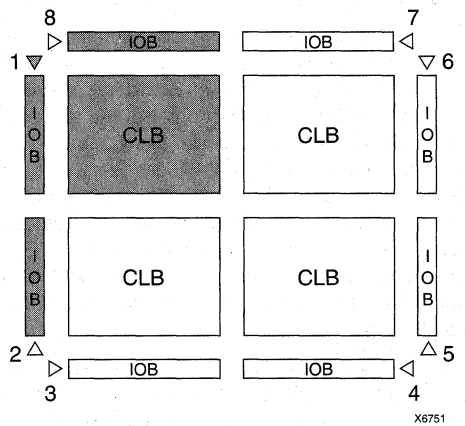


Figure 38: Left and Right BUFGEs Can Drive Any or All Clock Inputs in Same Quadrant or Edge (GCK1 is shown. GCK2, GCK5 and GCK6 are similar.)

Global Early Buffers

Each corner of the XC4000EX device has two Global Early buffers. The primary purpose of the Global Early buffers is to provide an earlier clock access than the potentially heavily-loaded Global Low-Skew buffers. A clock source applied to both buffers will result in the Global Early clock edge occurring several nanoseconds earlier than the Global Low-Skew buffer clock edge, due to the lighter loading.

Global Early buffers also facilitate the fast capture of device inputs, using the Fast Capture latches described in "IOB Input Signals" on page 24. For Fast Capture, take a single clock signal, and route it through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) Use the Global Early buffer to clock the Fast Capture latch, and the Global Low-Skew buffer to clock the normal input flip-flop or latch, as shown in Figure 18 on page 26.

The Global Early buffers can also be used to provide a fast Clock-to-Out on device output pins. However, an early clock in the output flip-flop IOB must be taken into consideration when calculating the internal clock speed for the design.

The Global Early buffers at the left and right edges of the chip have slightly different capabilities than the ones at the top and bottom. Refer to Figure 38, Figure 39, and Figure 36 on page 42 while reading the following explanation.

Each Global Early buffer can access the eight vertical Global lines for all CLBs in the quadrant. Therefore, only one-fourth of the CLB clock pins can be accessed. This restriction is in large part responsible for the faster speed of the buffers, relative to the Global Low-Skew buffers.

The left-side Global Early buffers can each drive two of the four vertical lines accessing the IOBs on the entire left edge of the device. The right-side Global Early buffers can each drive two of the eight vertical lines accessing the IOBs on the entire right edge of the device. (See Figure 38.)

Each left and right Global Early buffer can also drive half of the IOBs along either the top or bottom edge of the device, using a dedicated line that can only be accessed through the Global Early buffers.

The top and bottom Global Early buffers can drive half of the IOBs along either the left or right edge of the device, as shown in Figure 39. They can only access the top and bottom IOBs via the CLB global lines.

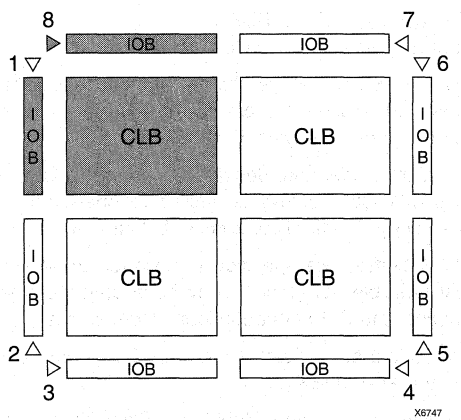


Figure 39: Top and Bottom BUFGEs Can Drive Any or All Clock Inputs in Same Quadrant (GCK8 is shown. GCK3, GCK4 and GCK7 are similar.)

The Global Early buffers can be driven by either semi-dedicated pads or internal logic. They share pads with the Global Low-Skew buffers, so a single net can drive both global buffers, as described above.

To use a Global Early buffer, place a BUFGE element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGE be placed in one of the two Global Early buffers on the top edge of the device, or a LOC=TR to indicate the Global Early buffer on the top edge of the device, on the right.

FastCLK Buffers

The fastest way to bring a clock into the XC4000EX device is through a FastCLK buffer. Two FastCLK buffers are present on the left edge, and two on the right edge, of the XC4000EX die. There are no FastCLK buffers on the top or bottom edges.

One purpose of the FastCLK buffers is to create a very fast pin-to-pin path by using the IOB 2-input function generator in conjunction with the FastCLK. Drive the F input of the IOB function generator with the FastCLK buffer output, as described in "IOB Output Signals" on page 27.

Alternatively, a FastCLK buffer can be used to minimize the setup time of device inputs, if a positive hold time is acceptable. Use the FastCLK buffer to clock the Fast Capture latch, and a slower clock buffer to clock the standard IOB flip-flop or latch. Either the Global Early buffer or the Global Low-Skew buffer can be used for the second storage element, but whichever one is used should be the same clock as the related internal logic. Since the FastCLK pads are different from the Global Early and Global Low-Skew pads, care must be taken to ensure that skew external to the device does not create internal timing difficulties.

The FastCLK buffers can also be used to provide a fast Clock-to-Out on device output pins. However, a fast clock in the output flip-flop IOB must be taken into consideration when calculating the internal clock speed for the design.

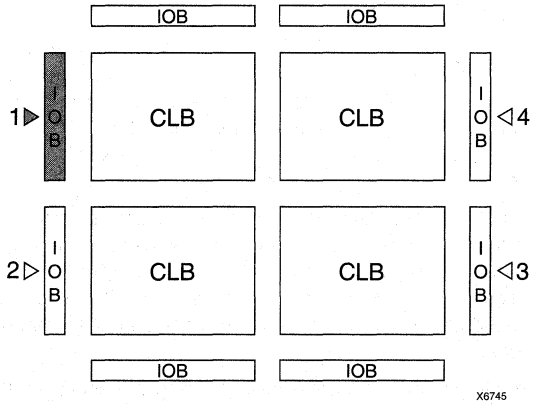


Figure 40: Each BUFFCLK Can Drive Any or All Clock Inputs in Same Half-Edge (FCLK1 is shown. FCLK2, FCLK3 and FCLK4 are similar.)

The FastCLK buffers are limited to accessing IOBs on one-half of the die edge only, as shown in Figure 40 and Figure 36 on page 42. They can each drive two of the four vertical lines accessing the IOBs on the left edge of the device, or two of the eight vertical lines accessing the IOBs on the right edge of the device. They can only access the CLB array through single- and double-length lines.

The FastCLK buffers must be driven by the semi-dedicated IOBs. They are not accessible from internal nets. Other than the FastCLK feature, these IOBs are identical to all other IOBs.

To use a FastCLK buffer, place a BUFFCLK element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=LB attribute or property to direct that a BUFFCLK be placed on the left edge of the device at the bottom, or use LOC=L to indicate either of the buffers on the left edge.

The input to the BUFFCLK symbol must be driven by a input pad symbol, such as IPAD, or by an input flip-flop or latch, such as INFF, ILD, ILDFFDX, or ILDFLDX.

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated Vcc and Ground ring surrounding the logic array provides power to the I/O drivers, as shown in Figure 41. An independent matrix of Vcc and Ground lines supplies the interior logic of the device.

This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically, a 0.1 µF capacitor connected near the Vcc and Ground pins of the package will provide adequate decoupling.

Output buffers capable of driving/sinking the specified 12 mA (XC4000E) or 24 mA (XC4000EX) loads under specified worst-case conditions may be capable of driving/sinking up to 10 times as much current under best case conditions.

Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the Ground pads. The I/O Block output buffers have a slew-rate limited mode (default) which should be used where output rise and fall times are not speed-critical.

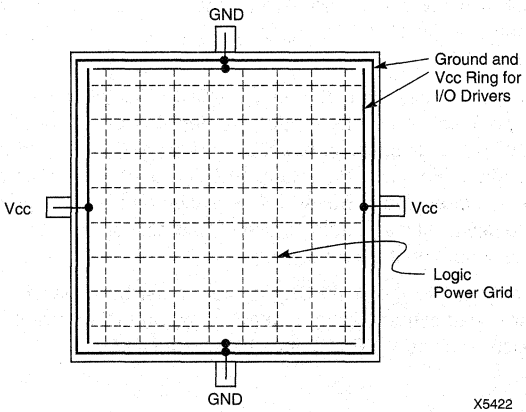


Figure 41: XC4000-Series Power Distribution

Pin Descriptions

There are three types of pins in the XC4000-Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with a 50 kΩ - 100 kΩ pull-up resistor.

After configuration, if an IOB is unused it is configured as an input with a 50 kΩ - 100 kΩ pull-up resistor.

XC4000-Series devices have no dedicated Reset input. Any user I/O can be configured to drive the Global Set/Reset net, GSR. See "Global Set/Reset" on page 13 for more information on GSR.

XC4000-Series devices have no Powerdown control input, as the XC3000 and XC2000 families do. The XC3000/XC2000 Powerdown control also 3-stated all of the device I/O pins. For XC4000-Series devices, use the global 3-state net, GTS, instead. This net 3-states all outputs, but does not place the device in low-power mode. See "IOB Output Signals" on page 27 for more information on GTS.

Device pins for XC4000-Series devices are described in Table 18. Pin functions during configuration for each of the seven configuration modes are summarized in Table 24 on page 78, in the "Configuration Timing" section.

Table 18: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
VCC	I	I	Eight or more (depending on package) connections to the nominal +5 V supply voltage (+3.3 V for low-voltage devices). All must be connected, and each must be decoupled with a 0.01 - 0.1 µF capacitor to Ground.
GND	I	I	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master modes or Asynchronous Peripheral mode, but is an input in Slave mode, Synchronous Peripheral mode, and Express mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High time restriction on XC4000-Series devices, except during Readback. See "Violating the Maximum High and Low Time Specification for the Readback Clock" on page 65 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in MakeBits, the XACT*step* program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to Vcc.
User I/O Pins That Can Have Special Functions			
RDY/$\overline{\text{BUSY}}$	O	I/O	During Peripheral mode configuration, this pin indicates when it is appropriate to write another byte of data into the FPGA. The same status is also available on D7 in Asynchronous Peripheral mode, if a read operation is performed when the device is selected. After configuration, RDY/$\overline{\text{BUSY}}$ is a user-programmable I/O pin. RDY/$\overline{\text{BUSY}}$ is pulled High with a high-impedance pull-up prior to $\overline{\text{INIT}}$ going High.
$\overline{\text{RCLK}}$	O	I/O	During Master Parallel configuration, each change on the A0-A17 outputs (A0 - A21 for XC4000EX) is preceded by a rising edge on $\overline{\text{RCLK}}$, a redundant output signal. $\overline{\text{RCLK}}$ is useful for clocked PROMs. It is rarely used during configuration. After configuration, $\overline{\text{RCLK}}$ is a user-programmable I/O pin.
M0, M1, M2	I	I (M0), O (M1), I (M2)	As Mode inputs, these pins are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. After configuration, M0 and M2 can be used as inputs, and M1 can be used as a 3-state output. These three pins have no associated input or output registers. During configuration, these pins have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected. The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors. A pull-down resistor value of 4.7 kΩ is recommended. These pins can only be used as inputs or outputs when called out by special schematic definitions. To use these pins, place the library components MD0, MD1, and MD2 instead of the usual pad symbols. Input or output buffers must still be used.

Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special schematic definitions. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 kΩ - 10 kΩ external pull-up resistor is recommended. As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.
SGCK1 - SGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (XC4000EX only)	Weak Pull-up	I or I/O	Eight inputs can each drive a Global Low-Skew buffer. In addition, each can drive a Global Early buffer. Each pair of global buffers can also be driven from internal logic, but must share an input signal. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFGLS or BUFGE symbol is automatically placed on one of these pins.
FCLK1 - FCLK4 (XC4000EX only)	Weak Pull-up	I or I/O	Four FCLK inputs can each drive a FastCLK buffer. The FastCLK buffers cannot be driven from internal logic. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFFCLK symbol is automatically placed on one of these pins.

Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
$\overline{CS0}$, CS1, $\overline{WS}$, $\overline{RS}$	I	I/O	These four inputs are used in Asynchronous Peripheral mode. The chip is selected when $\overline{CS0}$ is Low and CS1 is High. While the chip is selected, a Low on Write Strobe ($\overline{WS}$) loads the data present on the D0 - D7 inputs into the internal data buffer. A Low on Read Strobe ($\overline{RS}$) changes D7 into a status output — High if Ready, Low if Busy — and drives D0 - D6 High. In Express mode, CS1 is used as a serial-enable signal for daisy-chaining. $\overline{WS}$ and $\overline{RS}$ should be mutually exclusive, but if both are Low simultaneously, the Write Strobe overrides. After configuration, these are user-programmable I/O pins.
A0 - A17	O	I/O	During Master Parallel configuration, these 18 output pins address the configuration EPROM. After configuration, they are user-programmable I/O pins.
A18 - A21 (XC4000EX only)	O	I/O	During Master Parallel configuration with an XC4000EX master, these 4 output pins add 4 more bits to address the configuration EPROM. After configuration, they are user-programmable I/O pins.
D0 - D7	I	I/O	During Master Parallel and Peripheral configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. During Parallel configuration, DIN is the D0 input. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During configuration in any mode but Express mode, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor (50 kΩ - 100 kΩ) that defines the logic level as High.

Boundary Scan

The 'bed of nails' has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan-compatible IC. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The XC4000 Series implements IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in Xilinx devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note XAPP 017: "*Boundary Scan in XC4000 Devices.*"

Figure 42 shows a simplified block diagram of the XC4000E Input/Output Block with boundary scan implemented. XC4000EX boundary scan logic is identical.

Figure 43 on page 52 is a diagram of the XC4000-Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

XC4000-Series devices can also be configured through the boundary scan logic. See "Configuration Through the Boundary Scan Pins" on page 64.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-State Control. Non-IOB pins have appropriate partial bit population for In or Out only. $\overline{\text{PROGRAM}}$, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The XC4000-Series boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 19.

Table 19: Boundary Scan Instructions

Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	Reserved	—	—
1	1	1	BYPASS	Bypass Register	—

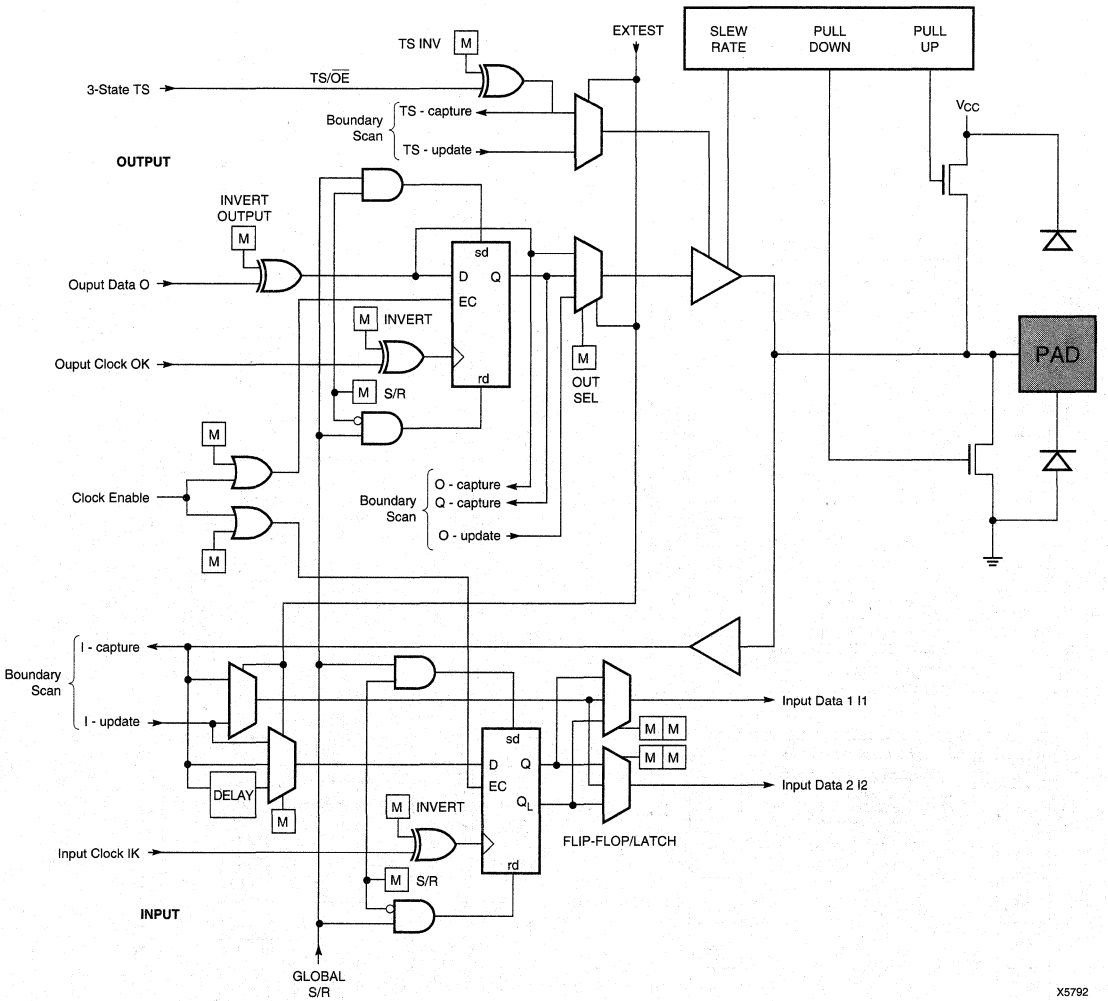


Figure 42: Block Diagram of XC4000E IOB with Boundary Scan (some details not shown). XC4000EX Boundary Scan Logic is Identical.

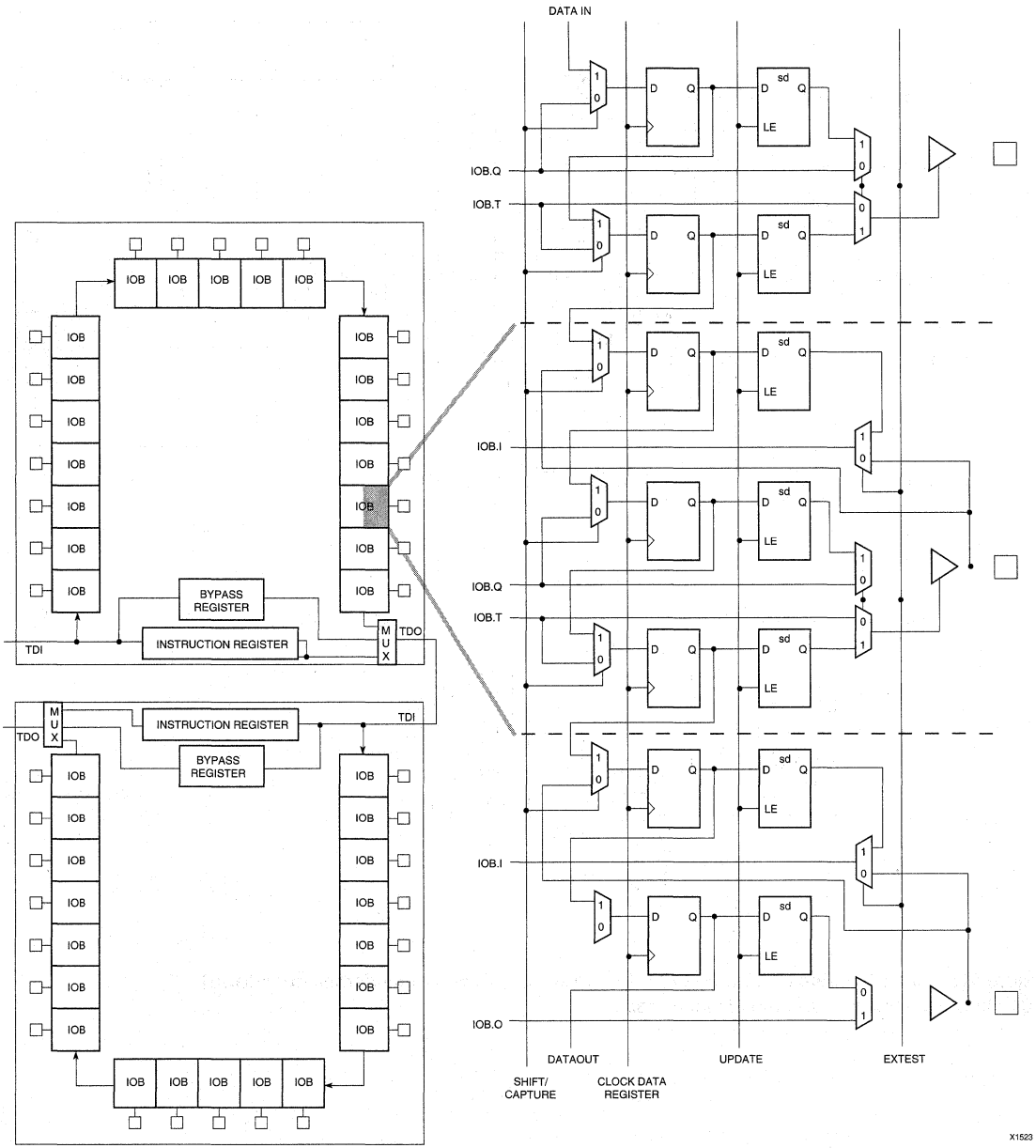


Figure 43: XC4000-Series Boundary Scan Logic

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only M0 and M2 mode pins contribute only the In bit to the boundary scan I/O data register, while the output-only M1 pin contributes all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in XDE or Epic), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 44. The device-specific pinout tables for the XC4000 Series include the boundary scan locations for each IOB pin.

BSDL (Boundary Scan Description Language) files for XC4000-Series devices are available on the Xilinx BBS.

Including Boundary Scan in a Schematic

If boundary scan is only to be used during configuration, no special schematic elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 45.

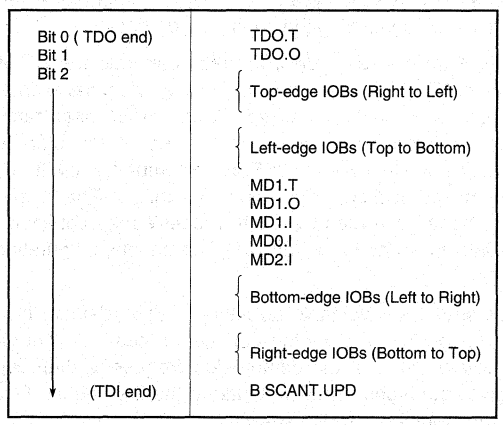


Figure 44: Boundary Scan Bit Sequence

Even if the boundary scan symbol is used in a schematic, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Avoiding Inadvertent Boundary Scan Activation

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state
- TCK: Tie High or Low—don't toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note XAPP 017.001, "*Boundary Scan in XC4000E Devices.*"

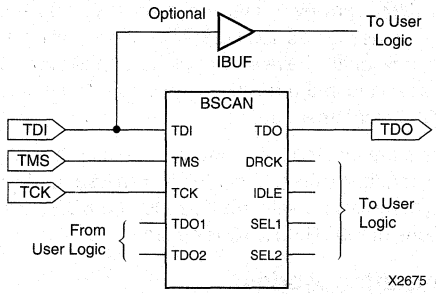


Figure 45: Boundary Scan Schematic Example

Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. XC4000-Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The XACT*step* development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Special Purpose Pins

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary connections. M2 and M0 can be used as inputs, and M1 can be used as an output. The XACT*step* development system does not use these resources unless they are explicitly specified in the design entry. This is done by placing a special pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In XC4000-Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the mode pins can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ.) After configuration, these pins can individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of 4.7 kΩ is recommended.

These pins are located in the lower left chip corner and are near the readback nets. This location allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

Configuration Modes

XC4000E devices have six configuration modes. XC4000EX devices have the same six modes, plus an additional configuration mode. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for daisy-chained devices. The seventh mode, called Express mode, is an additional slave mode that allows high-speed parallel configuration of the high-capacity XC4000EX devices. The coding for mode selection is shown in Table 20.

Table 20: Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Express (XC4000EX only)	0	1	0	input	Byte-Wide
Reserved	0	0	1	—	—

Note: * Peripheral Synchronous can be considered byte-wide Slave Parallel

A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in Table 24 on page 78.

Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, for compatibility with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as either 1 MHz (default) or 8 MHz (up to 10% lower for low-voltage devices). Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

Peripheral Modes

The two Peripheral modes accept byte-wide data from a bus. A RDY/$\overline{\text{BUSY}}$ status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the syn-

chronous mode, an externally supplied clock input to CCLK serializes the data.

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 55 on page 68. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received. Figure 49 on page 61 shows the start-up timing for an XC4000-Series device.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The MakePROM program must be used to combine the bitstreams for a daisy-chained configuration.

Multi-Family Daisy Chain

All Xilinx FPGAs of the XC2000, XC3000, and XC4000 Series use a compatible bitstream format and can, therefore, be connected in a daisy chain in an arbitrary sequence. There is, however, one limitation. The lead device must belong to the highest family in the chain. If the chain contains XC4000-Series devices, the master normally cannot be an XC2000 or XC3000 device.

The reason for this rule is shown in Figure 49 on page 61. Since all devices in the chain store the same length count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge, as indicated on the left edge of Figure 49. The master device then generates additional CCLK pulses until it reaches its finish point F. The different families generate or require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device does not really finish its configuration, although DONE may have gone High, the outputs became active, and the internal reset was released. For the XC4000-Series device, not reaching F means that readback cannot be initiated and most boundary scan instructions cannot be used.

The user has some control over the relative timing of these events and can, therefore, make sure that they occur at the proper time and the finish point F is reached. Timing is controlled using MakeBits options.

XC3000 Master with an XC4000-Series Slave

Some designers want to use an inexpensive lead device in peripheral mode and have the more precious I/O pins of the XC4000-Series devices all available for user I/O. Figure 46 provides a solution for that case.

This solution requires one CLB, one IOB and pin, and an internal oscillator with a frequency of up to 5 MHz as a clock source. The XC3000 master device must be configured with late Internal Reset, which is the default option.

One CLB and one IOB in the lead XC3000-family device are used to generate the additional CCLK pulse required by the XC4000-Series devices. When the lead device removes the internal RESET signal, the 2-bit shift register responds to its clock input and generates an active Low output signal for the duration of the subsequent clock period. An external connection between this output and CCLK thus creates the extra CCLK pulse.

Express Mode (XC4000EX only)

Express mode is similar to Slave Serial mode, except the data is presented in parallel format, and is clocked into the target device a byte at a time rather than a bit at a time. The data is loaded in parallel into eight different columns: it is not internally serialized. Eight bits of configuration data are loaded with every CCLK cycle, therefore this configuration

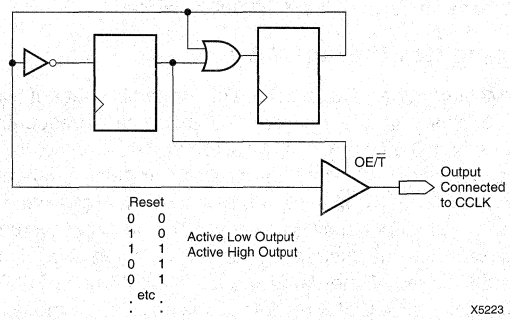


Figure 46: CCLK Generation for XC3000 Master Driving an XC4000-Series Slave

mode runs at eight times the data rate of the other six modes. A length count is not used in Express mode.

Express mode must be specified as an option to the MakeBits program, which generates the bitstream. The Express mode bitstream is not compatible with the other six configuration modes.

Multiple slave devices with identical configurations can be wired with parallel D0-D7 inputs. In this way, multiple devices can be configured simultaneously.

Pseudo Daisy Chain

Multiple devices with different configurations can be connected together in a pseudo daisy chain, provided that all of the devices are in Express mode. A single combined bitstream is used to configure the chain of Express mode devices, but the input data bus must drive D0-D7 of each device. Tie High the CS1 pin of the first device to be configured. Connect the DOUT pin of each FPGA to the CS1 pin of the next device in the chain. The D0-D7 inputs are wired to each device in parallel. The DONE pins are wired together, with one or more internal DONE pull-ups activated. Alternatively, a 4.7 kΩ external resistor can be used, if desired. (See Figure 63 on page 76.)

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All XC4000EX devices in Express mode are synchronized to the DONE pin. User I/O for each device become active after the DONE pin for that device goes High. (The exact timing is determined by MakeBits options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle.

Because only XC4000EX and XC5200 devices support Express mode, only these devices can be used to form an Express mode daisy chain. XC5200 devices used in a combined daisy chain with XC4000EX devices should be configured as synchronized to DONE (MakeBits option CCLK_SYNC or UCLK_SYNC), and their DONE pins wired together with those of the XC4000EX devices.

Setting CCLK Frequency

For Master modes, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz (up to 10% lower for low-voltage devices). In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz (up to 10% lower for low-voltage devices). The frequency is selected by an option when running MakeBits, the bitstream generation software tool. If an XC4000-Series Master is driving an XC3000- or XC2000-family slave, slow CCLK mode must be used. Slow mode is the default.

Data Stream Format

The data stream ("bitstream") format is identical for all configuration modes, with the exception of Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode.

The data stream formats are shown in Table 21. Express mode data is shown with D0 at the left and D7 at the right. For all other modes, bit-serial data is read from left to right, and byte-parallel data is effectively assembled from this serial bitstream, with the first bit in each byte assigned to D0.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 22 and Table 23). Each frame begins with a start field and ends with an error check. In all modes except Express mode, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

Table 21: XC4000-Series Data Stream Formats

Data Type	Express Mode (D0-D7)	All Other Modes (D0...)
Fill Byte	11111111b	11111111b
Preamble Code	11110010b	0010b
Length Count	FFFFFFh	COUNT(23:0)
Fill Bits	—	1111b
Start Field	11010010b	0b
Data Frame	DATA(n-1:0)	DATA(n-1:0)
CRC or Constant Field Check	11010010b	xxxx (CRC) or 0110b
Extend Write Cycle	FFFFFFFFFFh	—
Postamble	—	01111111b
Start-Up Bytes	xxxxxxxxh	xxh

LEGEND:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Table 22: XC4000E Program Data

Device	XC4003E	XC4005E/L	XC4006E	XC4008E	XC4010E/L	XC4013E/L	XC4020E	XC4025E
Max Logic Gates	3,000	5,000	6,000	8,000	10,000	13,000	20,000	25,000
CLBs (Row x Col.)	100 (10 x 10)	196 (14 x 14)	256 (16 x 16)	324 (18 x 18)	400 (20 x 20)	576 (24 x 24)	784 (28 x 28)	1,024 (32 x 32)
IOBs	80	112	128	144	160	192	224	256
Flip-Flops	360	616	768	936	1,120	1,536	2,016	2,560
Horizontal Longlines	20	28	32	36	40	48	56	64
TBUFs per Longline	12	16	18	20	22	26	30	34
Bits per Frame	126	166	186	206	226	266	306	346
Frames	428	572	644	716	788	932	1,076	1,220
Program Data	53,936	94,960	119,792	147,504	178,096	247,920	329,264	422,128
PROM Size (bits)	53,984	95,008	119,840	147,552	178,144	247,968	329,312	422,176

Notes: 1. Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits
Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1
Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
PROM Size = Program Data + 40
2. The user can add more "one" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.

The MakeBits software creates the configuration bitstream. In Express mode, only non-CRC error checking is supported. In all other modes, MakeBits allows a selection of CRC or non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, MakeBits calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the $\overline{\text{INIT}}$ pin. In Master modes, CCLK and address signals continue to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin Low or cycling Vcc.

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 21. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 47. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Read Capture MakeBits option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

Table 23: XC4000EX Program Data

Device	XC4028EX/XL	XC4036EX/XL	XC4044EX/XL	XC4052XL	XC4062XL
Max Logic Gates	28,000	36,000	44,000	52,000	62,000
CLBs (Row x Col.)	1,024 (32 x 32)	1,296 (36 x 36)	1,600 (40 x 40)	1,936 (44 x 44)	2,304 (48 x 48)
IOBs	256	288	320	352	384
Flip-Flops	2,560	3,168	3,840	4,576	5,376
Horizontal Longlines	192	216	240	264	288
TBUFs per Longline	34	38	42	46	50
Bits per Frame	421	469	517	565	613
Frames	1587	1775	1963	2151	2,339
Program Data	668,127	832,483	1,014,879	1,215,323	1,433,807
PROM Size (bits)	668,167	832,523	1,014,919	1,215,363	1,433,847

Notes: 1. Bits per Frame = (12 x number of rows) + 8 for the top + 16 for the bottom + 8 + 1 start bit + 4 error check bits
Number of Frames = (47 x number of columns) + 27 for the left edge + 52 for the right edge + 4
Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
PROM Size = Program Data + 40
2. The user can add more "one" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.
3. Express mode bitfiles are slightly larger (see Table 21).

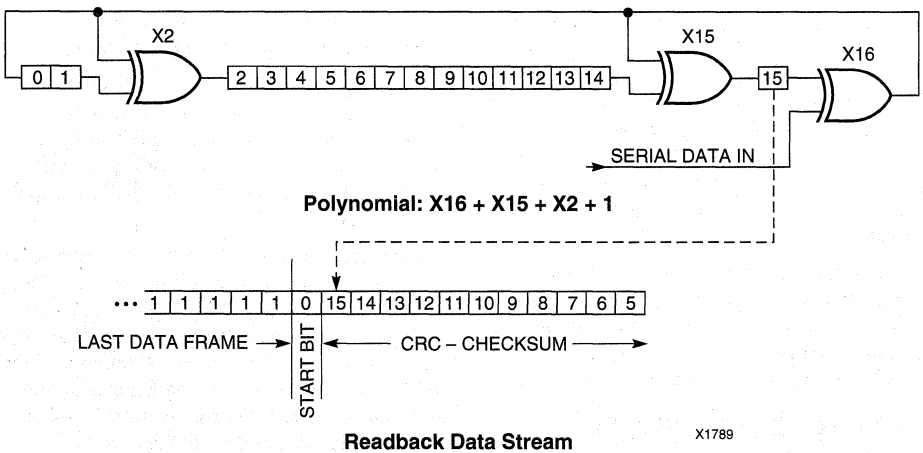


Figure 47: Circuit for Generating CRC-16

Configuration Sequence

There are four major steps in the XC4000-Series power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-Up

The full process is illustrated in Figure 48.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When Vcc reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms, and up to 10% longer in the low-voltage devices. The delay is four times as long when in Master Modes (M0 Low), to allow ample time for all slaves to reach a stable Vcc. When all $\overline{INIT}$ pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin Low. During this time delay, or as long as the $\overline{PROGRAM}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{PROGRAM}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the $\overline{INIT}$ input.

Initialization

During initialization and configuration, user pins HDC, $\overline{LDC}$, $\overline{INIT}$ and DONE provide status outputs for the system interface. The outputs $\overline{LDC}$, $\overline{INIT}$ and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain $\overline{INIT}$ pin is released after the final initialization pass through the frame addresses. There is a deliberate delay of 50 to 250 µs (up to 10% longer for low-voltage devices) before a Master-mode device recognizes an inactive $\overline{INIT}$. Two internal clocks after the $\overline{INIT}$ pin is recognized as High, the FPGA samples the three mode lines to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

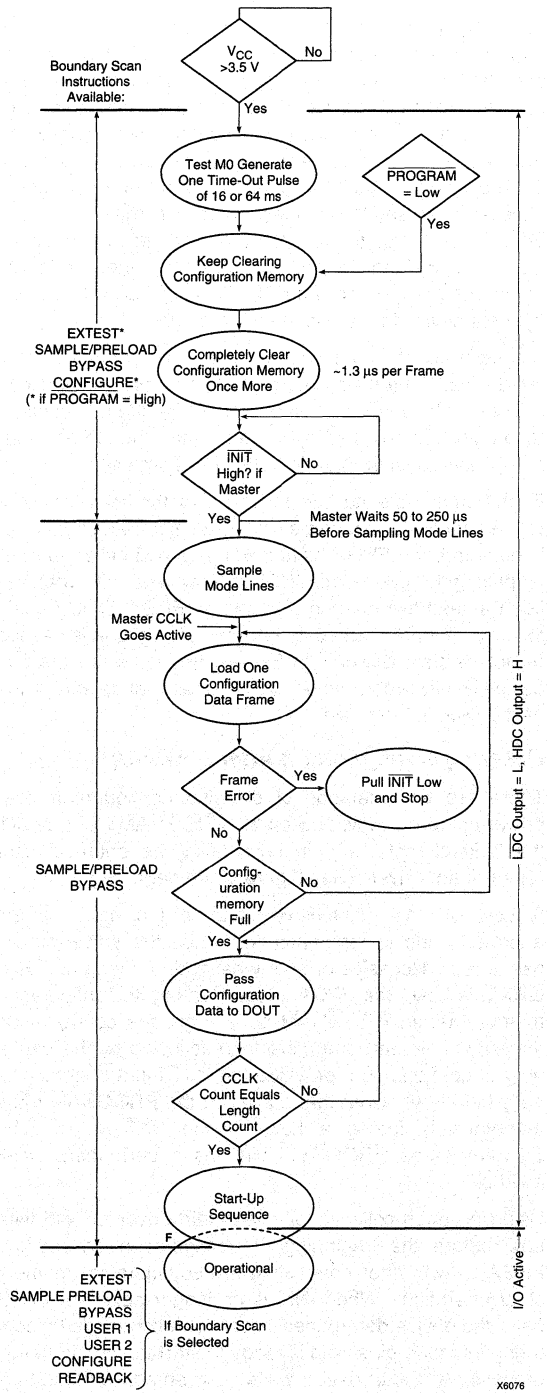


Figure 48: Power-up Configuration Sequence

Configuration

The 0010 preamble code, included for all modes except Express mode, indicates that the following 24 bits represent the length count. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to all devices in the daisy chain, DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain $\overline{\text{INIT}}$ pin Low. After all configuration frames have been loaded into an FPGA, DOUT again follows the input data so that the remaining data is passed on to the next device. In Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the $\overline{\text{PROGRAM}}$ input, or pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See Figure 48 on page 59.)

A Low on the $\overline{\text{PROGRAM}}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{\text{PROGRAM}}$ is Low, the FPGA keeps clearing its configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the $\overline{\text{INIT}}$ input is not externally held Low. Note that a Low on the $\overline{\text{PROGRAM}}$ input automatically forces a Low on the $\overline{\text{INIT}}$ output. The XC4000-Series $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up.

Using an open-collector or open-drain driver to hold $\overline{\text{INIT}}$ Low before the beginning of configuration causes the FPGA to wait after completing the configuration memory clear operation. When $\overline{\text{INIT}}$ is no longer held Low externally, the device determines its configuration mode by capturing its mode pins, and is ready to start the configuration process. A master device waits up to an additional 250 µs to make sure that any slaves in the optional daisy chain have seen that $\overline{\text{INIT}}$ is High.

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset or Set at the right time.

Figure 49 describes start-up timing for the three Xilinx families in detail. Express mode configuration always uses either CCLK_SYNC or UCLK_SYNC timing, the other configuration modes can use any of the four timing sequences.

To access the internal start-up signals, place the STARTUP library symbol.

Start-up Timing

Different FPGA families have different start-up sequences.

The XC2000 family goes through a fixed sequence. DONE goes High and the internal global Reset is de-activated one CCLK period after the I/O become active.

The XC3000A family offers some flexibility. DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The XC4000 Series offers additional flexibility. The three events — DONE going High, the internal Set/Reset being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. Each of them can occur one CCLK period before or after, or simultaneous with, any of the others. This relative timing is selected by means of software options in MakeBits, the bitstream generation software.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset/Set is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 49, but the designer can modify it to meet particular requirements.

Normally, the start-up sequence is controlled by the internal device oscillator output (CCLK), which is asynchronous to the system clock.

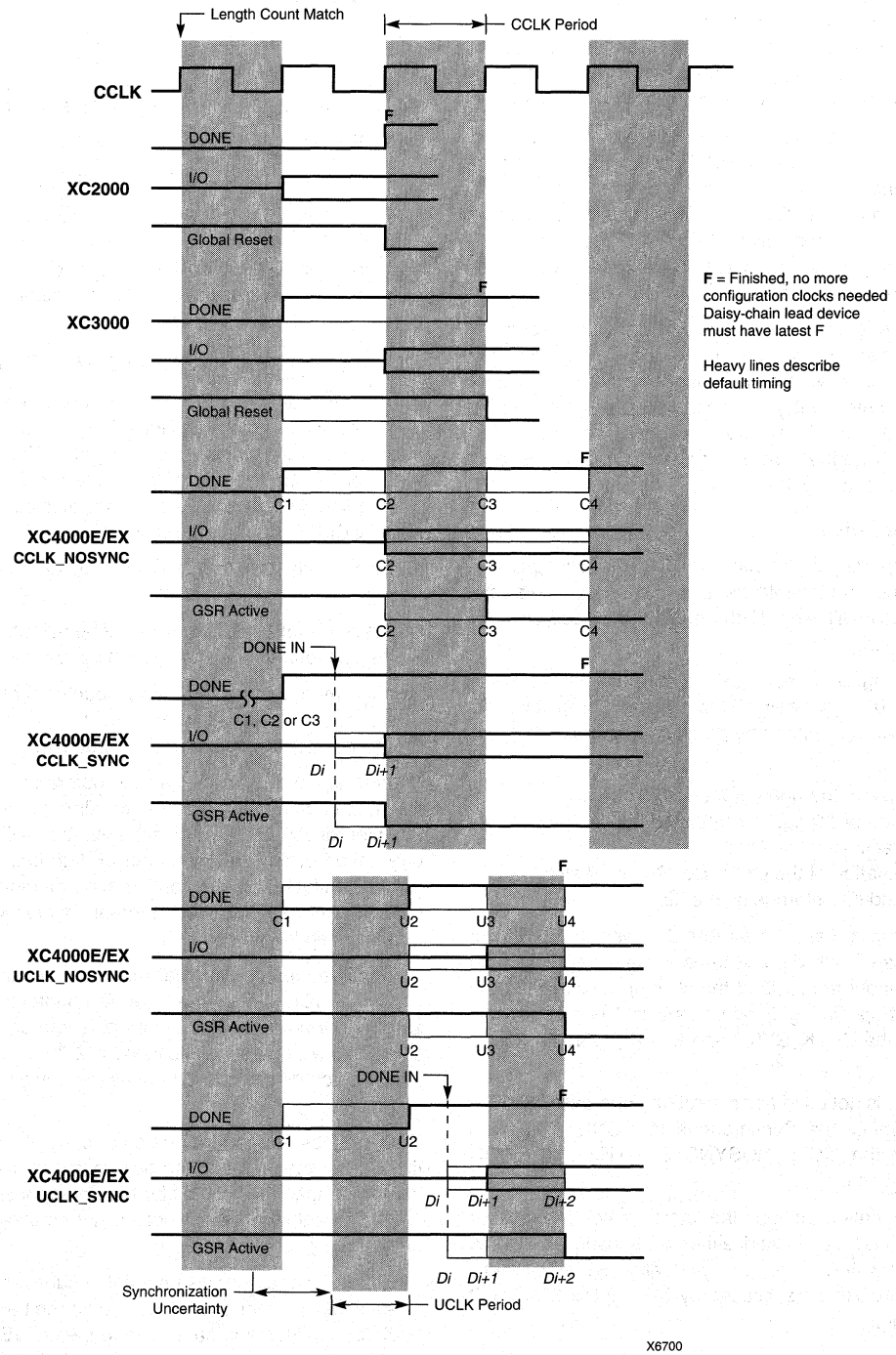


Figure 49: Start-up Timing

The XC4000 Series offers another start-up clocking option, UCLK_NOSYNC. The three events described above need not be triggered by CCLK. They can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

If either of these two options is selected, and no user clock is specified in the design or attached to the device, the chip could reach a point where the configuration of the device is complete and the Done pin is asserted, but the outputs do not become active. The solution is either to recreate the bitstream specifying the start-up clock as CCLK, or to supply the appropriate user clock.

Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks received since $\overline{INIT}$ went High equals the loaded value of the length count.

The next rising clock edge sets a flip-flop Q0, shown in Figure 50. Q0 is the leading bit of a 5-bit shift register. The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called "Start-up Timing Synchronous to Done In" and is selected by the CCLK_SYNC and UCLK_SYNC MakeBits options.

When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by the CCLK_NOSYNC and UCLK_NOSYNC MakeBits options.

As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK. These signals can be accessed by placing the STARTUP library symbol.

Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in Figure 49 show the default timing, which is compatible with XC2000 and XC3000 devices using early DONE and late Reset. The thin lines indicate all other possible timing options.

Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

DONE Goes High to Signal End of Configuration

In all configuration modes except Express mode, XC4000-Series devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

Two conditions have to be met in order for the DONE pin to go high:

- the chip's internal memory must be full, and
- the configuration length count must be met, *exactly.*

This is important because the counter that determines when the length count is met begins with the very first CCLK, not the first one after the preamble.

Therefore, if a stray bit is inserted before the preamble, or the data source is not ready at the time of the first CCLK, the internal counter that holds the number of CCLKs will be one ahead of the actual number of data bits read. At the end of configuration, the configuration memory will be full, but the number of bits in the internal counter will not match the expected length count.

As a consequence, a Master mode device will continue to send out CCLKs until the internal counter turns over to zero, and then reaches the correct length count a second time. This will take several seconds [2^{24} * CCLK period] — which is sometimes interpreted as the device not configuring at all.

If it is not possible to have the data ready at the time of the first CCLK, the problem can be avoided by increasing the number in the length count by the appropriate value. The *XACT User Guide* includes detailed information about manually altering the length count.

In Express mode, there is no length count. The DONE pin for each device goes High when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

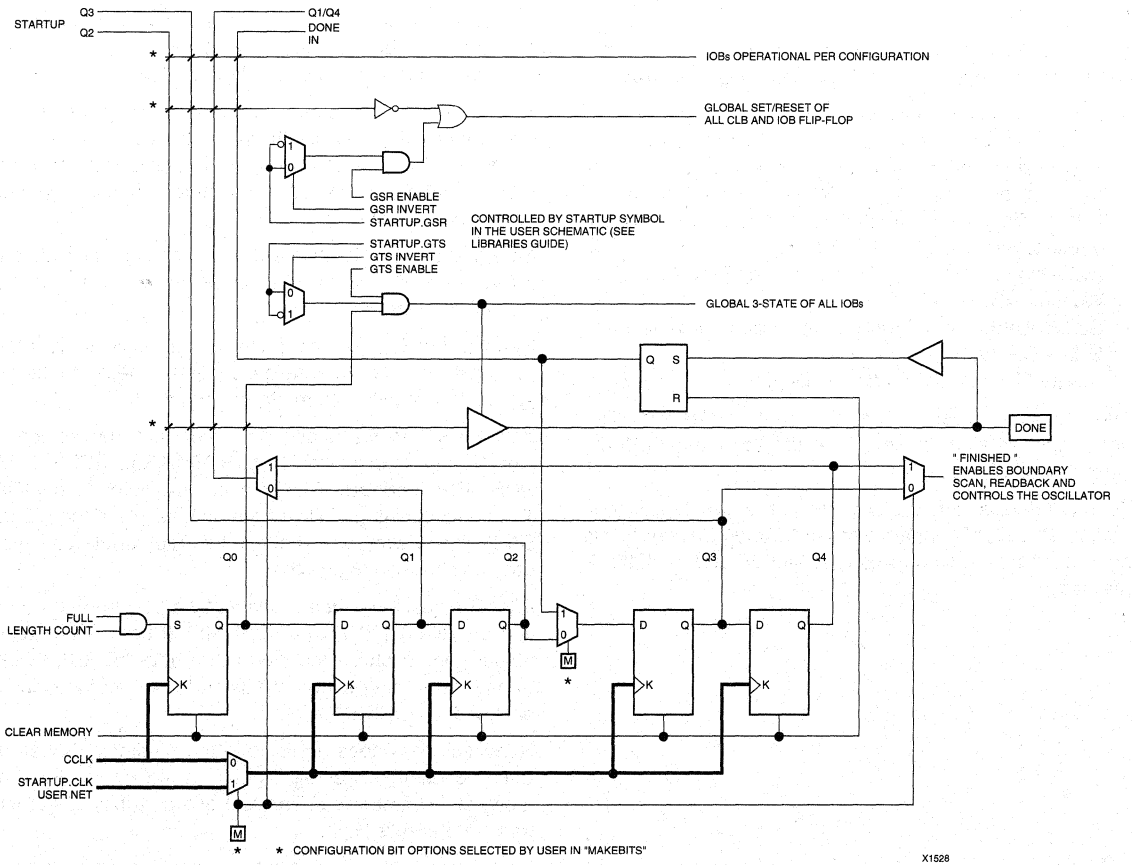


Figure 50: Start-up Logic

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by MakeBits, the bitstream generation software.

Release of User I/O After DONE Goes High

By default, the user I/O are released one CCLK cycle after the DONE pin goes High. If CCLK is not clocked after DONE goes High, the outputs remain in their initial state — 3-stated, with a 50 kΩ - 100 kΩ pull-up. The delay from DONE High to active user I/O is controlled by a MakeBits option.

Release of Global Set/Reset After DONE Goes High

By default, Global Set/Reset (GSR) is released two CCLK cycles after the DONE pin goes High. If CCLK is not clocked twice after DONE goes High, all flip-flops are held in their initial set or reset state. The delay from DONE High to GSR inactive is controlled by a MakeBits option.

Configuration Complete After DONE Goes High

Three full CCLK cycles are required after the DONE pin goes High, as shown in Figure 49 on page 61. If CCLK is not clocked three times after DONE goes High, readback cannot be initiated and most boundary scan instructions cannot be used.

Configuration Through the Boundary Scan Pins

XC4000-Series devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input
- Wait for $\overline{\text{INIT}}$ to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note XAPP017, "*Boundary Scan in XC4000 Devices*." This application note also applies to XC4000E and XC4000EX devices.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Note that in XC4000-Series devices, configuration data is *not* inverted with respect to configuration as it is in XC2000 and XC3000 families.

Readback of Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

XC4000-Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, place the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 51.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

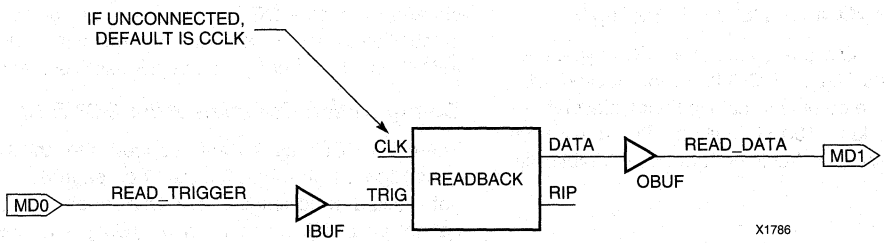


Figure 51: Readback Schematic Example

Readback Options

Readback options are: Read Capture, Read Abort, and Clock Select. They are set with MakeBits, the bitstream generation software.

Read Capture

When the Read Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted.

When the Read Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations.

If the RAM capability of the CLBs is used, RAM data are available in readback, since they directly overwrite the F and G function-table configuration of the CLB.

RDBK.TRIG is located in the lower-left corner of the device, as shown in Figure 52.

Read Abort

When the Read Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger.

After an aborted readback, additional clocks (up to one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If readback must be inhibited for security reasons, the readback control nets are simply not connected.

RDBK.CLK is located in the lower right chip corner, as shown in Figure 52.

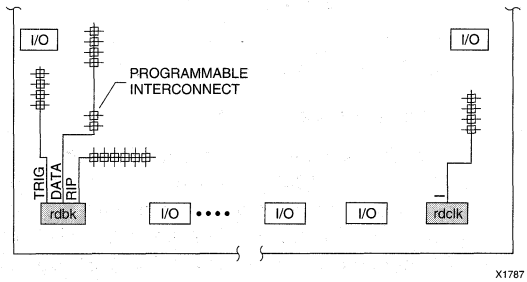


Figure 52: READBACK Symbol in Graphical Editor

Violating the Maximum High and Low Time Specification for the Readback Clock

The readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 21, Table 22 and Table 23.

Readback with the XChecker Cable

The XChecker Universal Download/Readback Cable and Logic Probe uses the readback feature for bitstream verification. It can also display selected internal signals on the PC or workstation screen, functioning as a low-cost in-circuit emulator.

Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In MakeBits, the user can specify Fast ConfigRate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. The value increases from between 0.5 and 1.25 MHz, to a value between 4 and 10 MHz. (For low-voltage devices, the frequency can be up to 10% lower.) Be sure that the serial PROM and slaves are fast enough to support this data rate. XC2000, XC3000/A, and XC3100A devices do not support the Fast ConfigRate option.

The SPROM CE input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).

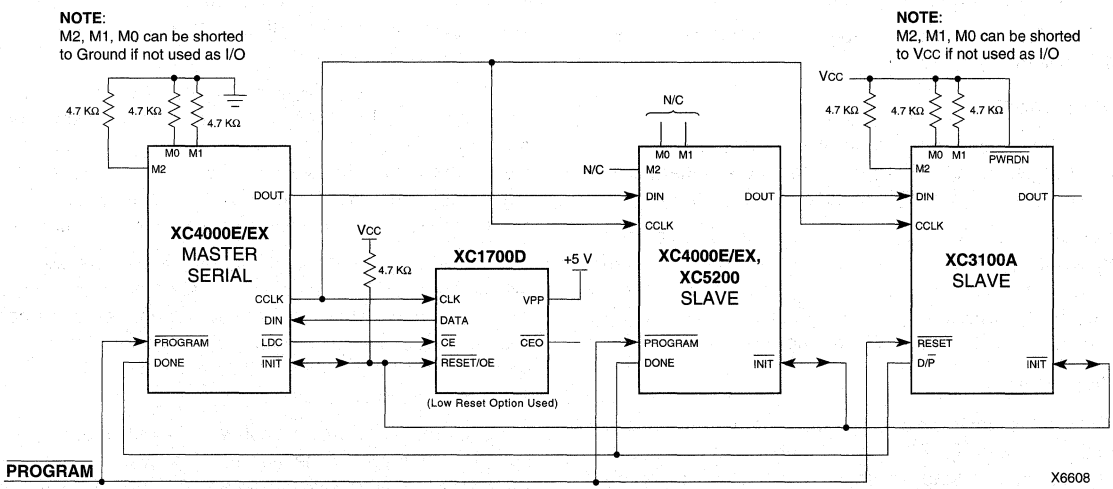
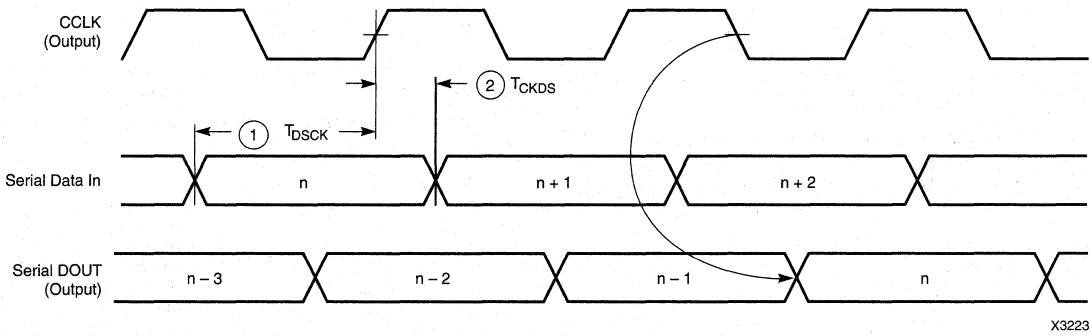


Figure 53: Master Serial Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DSCK}	20		ns
	DIN hold	2	T_{CKDS}	0		ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until Vcc is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 54: Master Serial Mode Programming Switching Characteristics

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resistors during configuration.

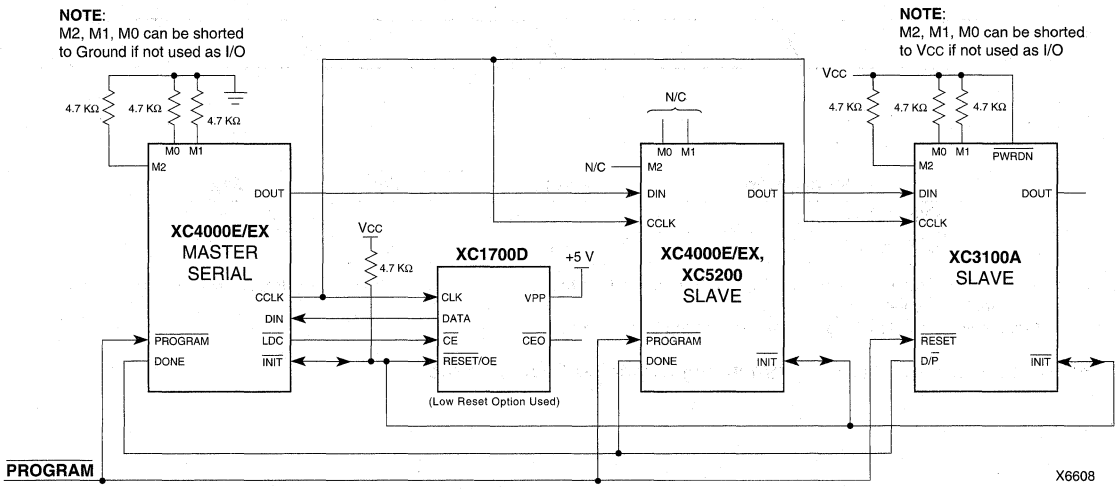
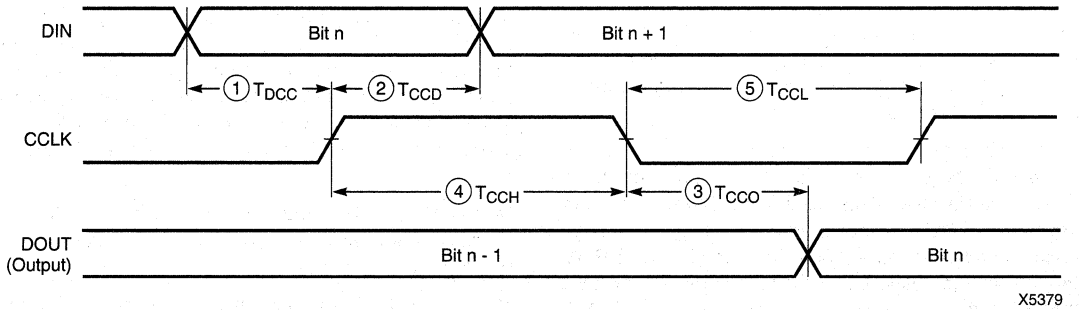


Figure 55: Slave Serial Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DCC}	20		ns
	DIN hold	2	T_{CCD}	0		ns
	DIN to DOUT	3	T_{CCO}		30	ns
	High time	4	T_{CCH}	45		ns
	Low time	5	T_{CCL}	45		ns
	Frequency		F_{CC}		10	MHz

Note: Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Figure 56: Slave Serial Mode Programming Switching Characteristics

Master Parallel Modes

In the two Master Parallel modes, the lead FPGA directly addresses an industry-standard byte-wide EPROM, and accepts eight data bits just before incrementing or decrementing the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data (and also changes the EPROM address) until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

The PROM address pins can be incremented or decremented, depending on the mode pin settings. This option allows the FPGA to share the PROM with a wide variety of microprocessors and microcontrollers. Some processors must boot from the bottom of memory (all zeros) while others must boot from the top. The FPGA is flexible and can load its configuration bitstream from either end of the memory.

Master Parallel Up mode is selected by a <100> on the mode pins (M2, M1, M0). The EPROM addresses start at 00000 and increment.

Master Parallel Down mode is selected by a <110> on the mode pins. The EPROM addresses start at 3FFFF and decrement.

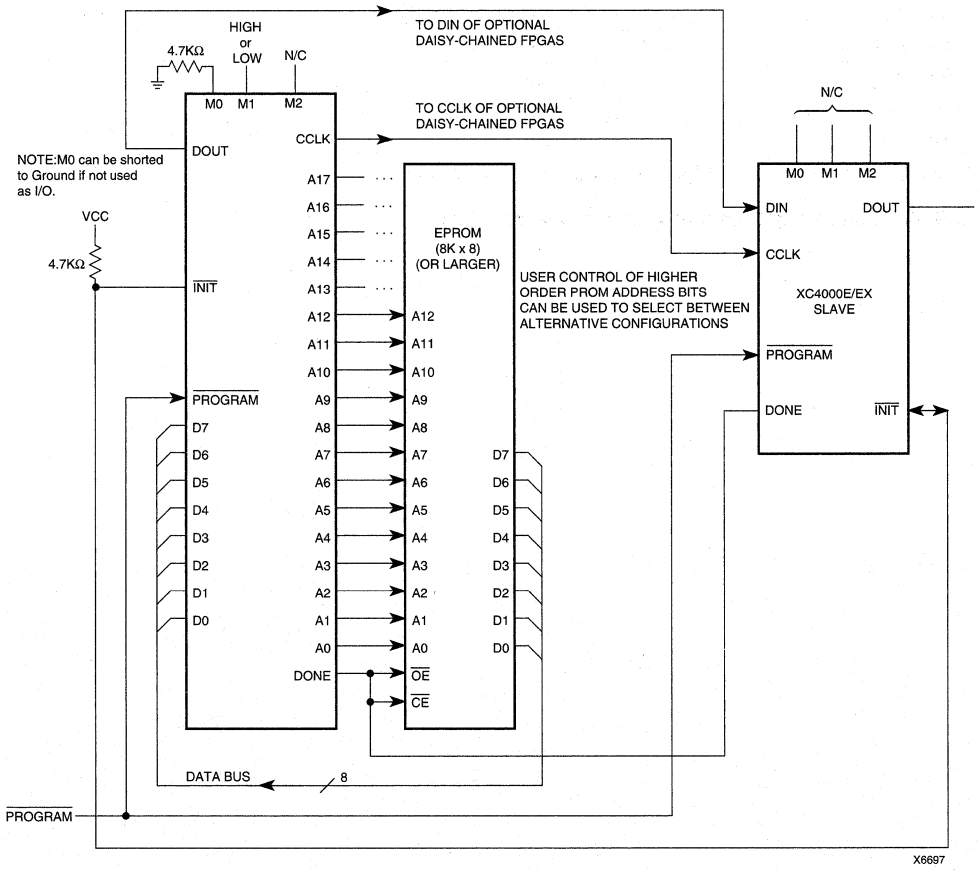
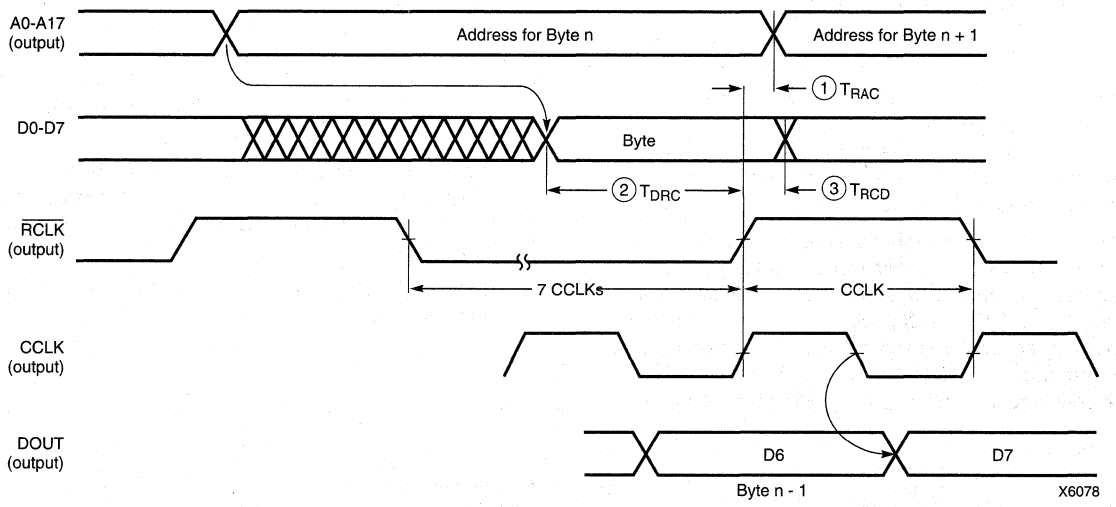


Figure 57: Master Parallel Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
RCLK	Delay to Address valid	1	T_{RAC}	0	200	ns
	Data setup time	2	T_{DRC}	60		ns
	Data hold time	3	T_{RCD}	0		ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until Vcc is valid.
2. The first Data byte is loaded and CCLK starts at the end of the first $\overline{\text{RCLK}}$ active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

Figure 58: Master Parallel Mode Programming Switching Characteristics

Synchronous Peripheral Mode

Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/$\overline{\text{BUSY}}$ output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal for test purposes. Note that RDY/$\overline{\text{BUSY}}$ is pulled High with a high-impedance pullup prior to $\overline{\text{INIT}}$ going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).

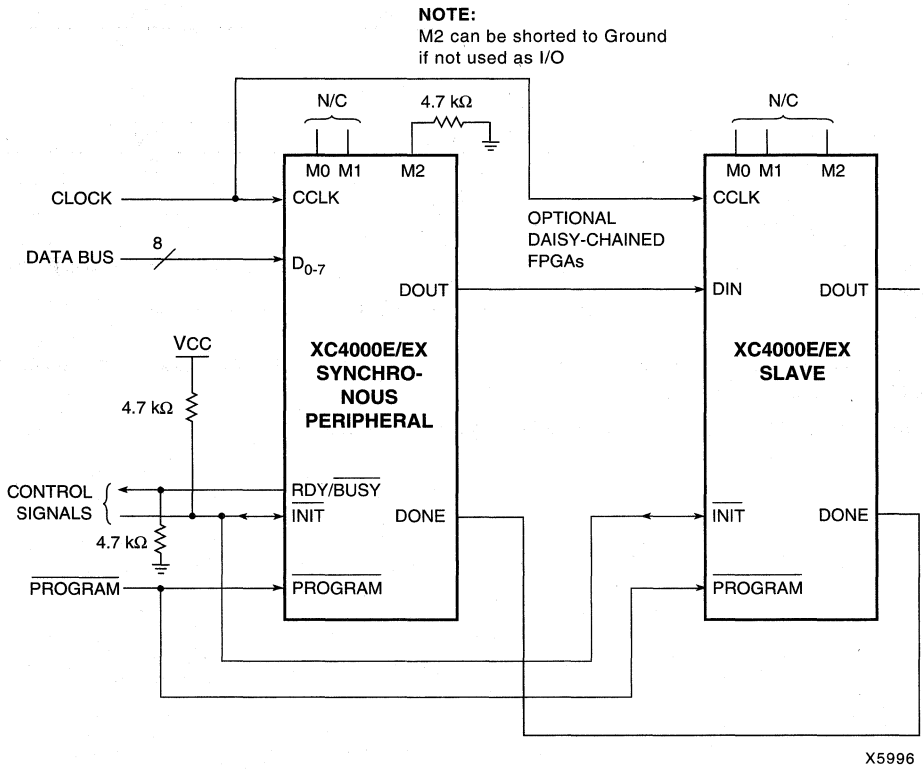
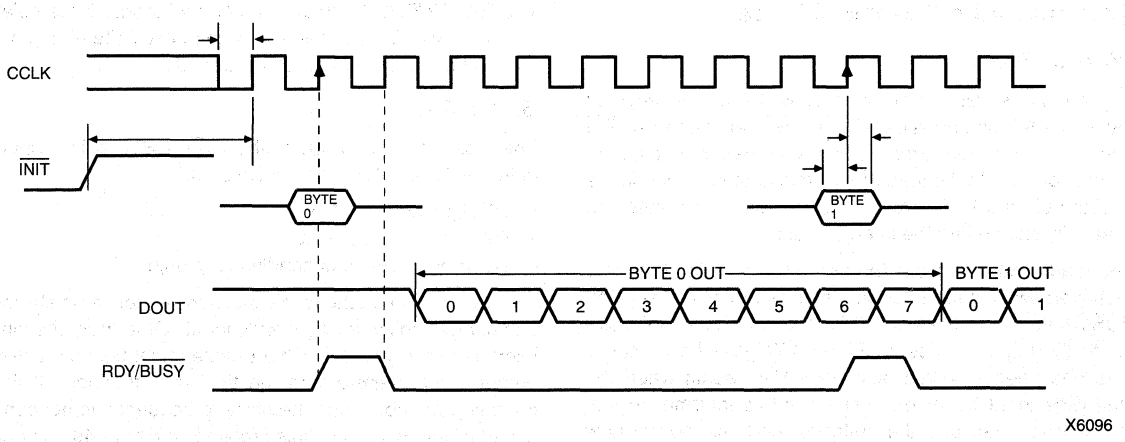


Figure 59: Synchronous Peripheral Mode Circuit Diagram



	Description	Symbol	Min	Max	Units
CCLK	INIT (High) setup time	T_{IC}	5		µs
	D0 - D7 setup time	T_{DC}	60		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	50		ns
	CCLK Low time	T_{CCL}	60		ns
	CCLK Frequency	F_{CC}		8	MHz

Notes:
1. Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after INIT goes High. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.
2. The RDY/BUSY line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.
3. The pin name RDY/BUSY is a misnomer. In Synchronous Peripheral mode this is really an ACKNOWLEDGE signal.
4. Note that data starts to shift out serially on the DOUT pin 0.5 CCLK periods after it was loaded in parallel. Therefore, additional CCLK pulses are clearly required after the last byte has been loaded.

Figure 60: Synchronous Peripheral Mode Programming Switching Characteristics

Asynchronous Peripheral Mode

Write to FPGA

Asynchronous Peripheral mode uses the trailing edge of the logic AND condition of $\overline{WS}$ and $\overline{CS0}$ being Low and $\overline{RS}$ and CS1 being High to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic.

The lead FPGA presents the preamble data (and all data that overflows the lead device) on its DOUT pin. The RDY/$\overline{BUSY}$ output from the lead FPGA acts as a handshake signal to the microprocessor. RDY/$\overline{BUSY}$ goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. A new write may be started immediately, as soon as the RDY/$\overline{BUSY}$ output has gone Low, acknowledging receipt of the previous data. Write may not be terminated until RDY/$\overline{BUSY}$ is High again for one CCLK period. Note that RDY/$\overline{BUSY}$ is pulled High with a high-impedance pull-up prior to $\overline{INIT}$ going High.

The length of the $\overline{BUSY}$ signal depends on the activity in the UART. If the shift register was empty when the new byte was received, the $\overline{BUSY}$ signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the $\overline{BUSY}$ signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

The READY/$\overline{BUSY}$ handshake can be ignored if the delay from any one Write to the end of the next Write is guaranteed to be longer than 10 CCLK periods.

Status Read

The logic AND condition of the $\overline{CS0}$, CS1and $\overline{RS}$ inputs puts the device status on the Data bus.

- D7 High indicates Ready
- D7 Low indicates Busy
- D0 through D6 go unconditionally High

It is mandatory that the whole start-up sequence be started and completed by one byte-wide input. Otherwise, the pins used as Write Strobe or Chip Enable might become active outputs and interfere with the final byte transfer. If this transfer does not occur, the start-up sequence is not completed all the way to the finish (point F in Figure 49 on page 61).

In this case, at worst, the internal reset is not released. At best, Readback and Boundary Scan are inhibited. The length-count value, as generated by MakeBits and MakePROM, ensures that these problems never occur.

Although RDY/$\overline{BUSY}$ is brought out as a separate signal, microprocessors can more easily read this information on one of the data lines. For this purpose, D7 represents the RDY/$\overline{BUSY}$ status when $\overline{RS}$ is Low, $\overline{WS}$ is High, and the two chip select lines are both active.

Asynchronous Peripheral mode is selected by a <101> on the mode pins (M2, M1, M0).

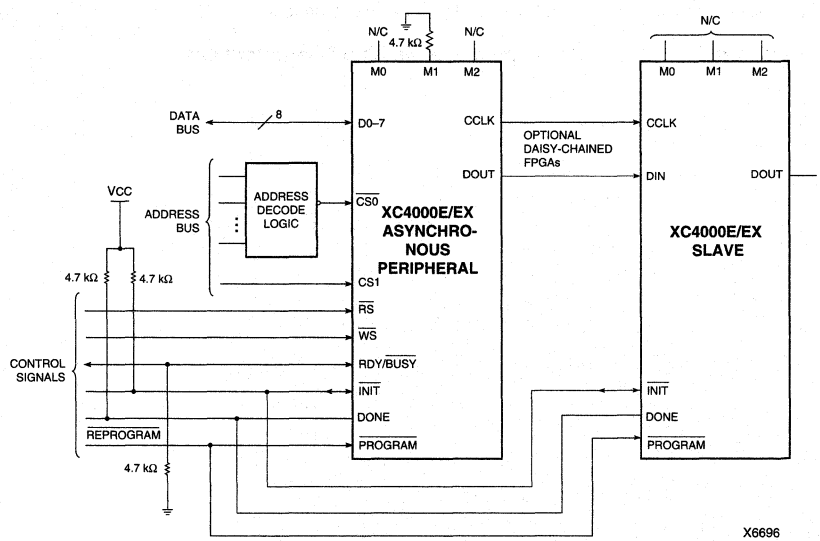
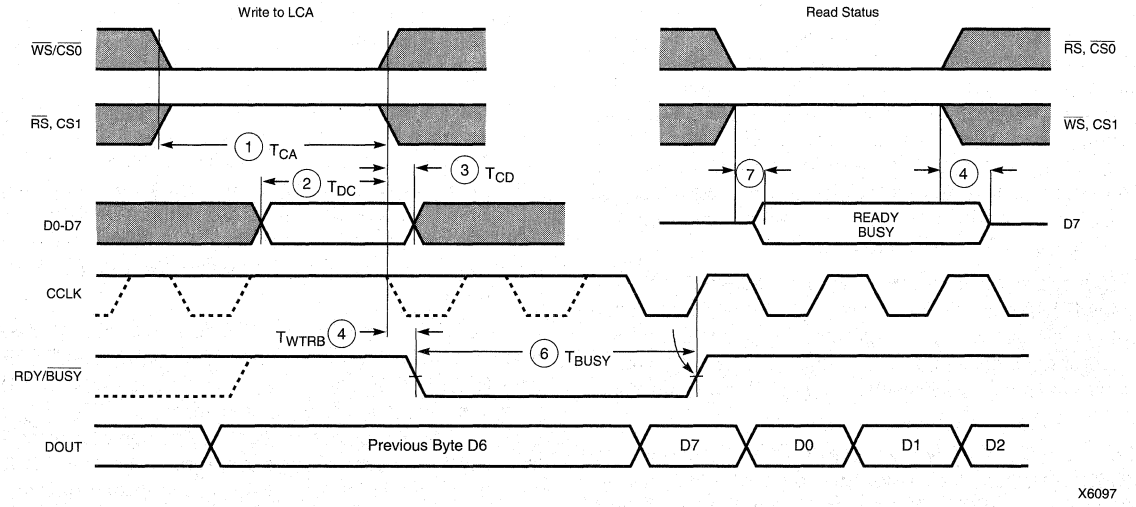


Figure 61: Asynchronous Peripheral Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
Write	Effective Write time ($\overline{CS0}$, $\overline{WS}$=Low; $\overline{RS}$, CS1=High)	1	T_{CA}	100		ns
	DIN setup time	2	T_{DC}	60		ns
	DIN hold time	3	T_{CD}	0		ns
RDY	RDY/$\overline{BUSY}$ delay after end of Write or Read	4	T_{WTRB}		60	ns
	RDY/$\overline{BUSY}$ active after beginning of Read	7			60	ns
	RDY/$\overline{BUSY}$ Low output (Note 4)	6	T_{BUSY}	2	9	CCLK periods

Notes:
1. Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.
2. The time from the end of $\overline{WS}$ to CCLK cycle for the new byte of data depends on the completion of previous byte processing and the phase of the internal timing generator for CCLK.
3. CCLK and DOUT timing is tested in slave mode.
4. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T_{BUSY} occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements. Data need not be held beyond the rising edge of $\overline{WS}$. RDY/$\overline{BUSY}$ will go active within 60 ns after the end of $\overline{WS}$. A new write may be asserted immediately after RDY/$\overline{BUSY}$ goes Low, but write may not be terminated until RDY/$\overline{BUSY}$ has been High for one CCLK period.

Figure 62: Asynchronous Peripheral Mode Programming Switching Characteristics

Express Mode (XC4000EX only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers. A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking.

In Express mode, an external signal drives the CCLK input of the FPGA device. The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge.

Express mode is only supported by the XC4000EX and XC5200 families. It may not be used, therefore, when an XC4000EX or XC5200 device is daisy-chained with devices from other Xilinx families.

If the first device is configured in Express mode, additional devices may be daisy-chained only if every device in the chain is also configured in Express mode. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pullup). Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The status pin DOUT is pulled Low two internal-oscillator cycles after $\overline{INIT}$ is recognized as High, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a MakeBits option.

XC4000EX devices in Express mode are always synchronized to DONE. The device becomes active after DONE goes High. DONE is an open-drain output. With the DONE pins tied together, therefore, the external DONE signal stays low until all devices are configured, then all devices in the daisy chain become active simultaneously. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. XC5200 devices in the chain should be configured as synchronized to DONE (MakeBits option CCLK_SYNC or UCLK_SYNC), and their DONE pins wired together with those of the XC4000EX devices.

Express mode must be specified as an option to the MakeBits program, which generates the bitstream. The Express mode bitstream is not compatible with the other six configuration modes.

Express mode is selected by a <010> on the mode pins (M2, M1, M0).

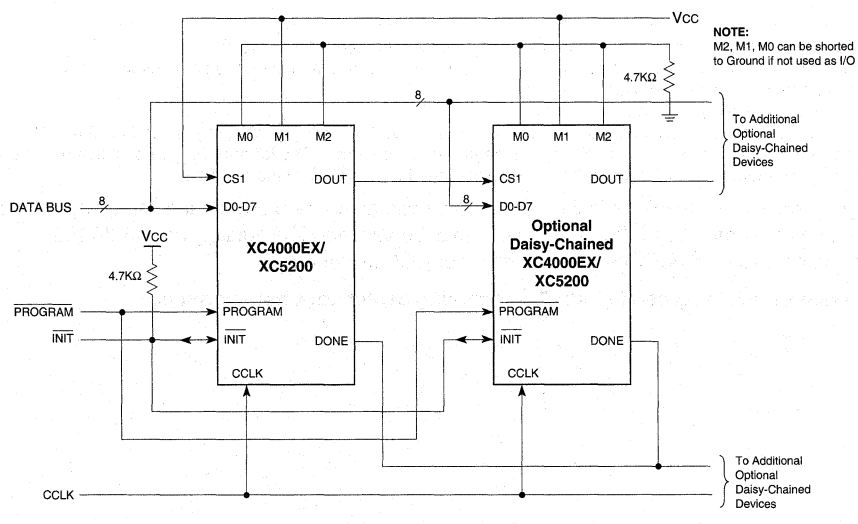
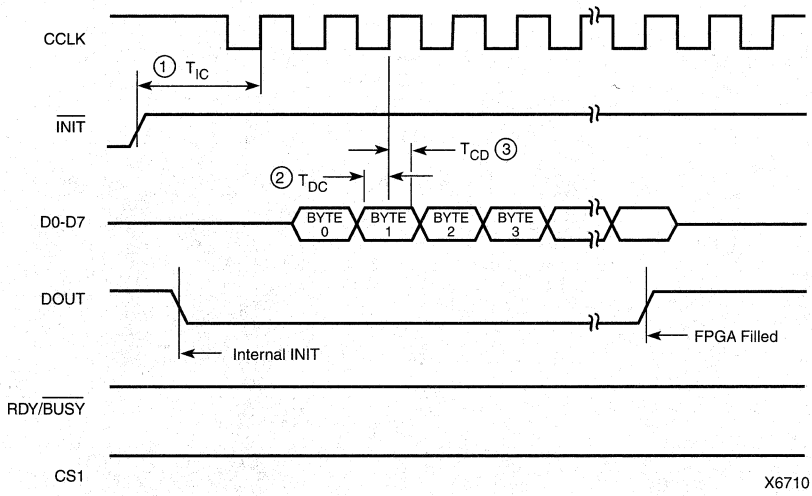


Figure 63: Express Mode Circuit Diagram

	Description	Symbol	Min	Max	Units
CCLK	$\overline{INIT}$ (High) setup time	T_{IC}	-		µs
	D0 - D7 setup time	T_{DC}	-		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	-		ns
	CCLK Low time	T_{CCL}	-		ns
	CCLK Frequency	F_{CC}		-	MHz
			Preliminary		



Note: If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 64: Express Mode Programming Switching Characteristics

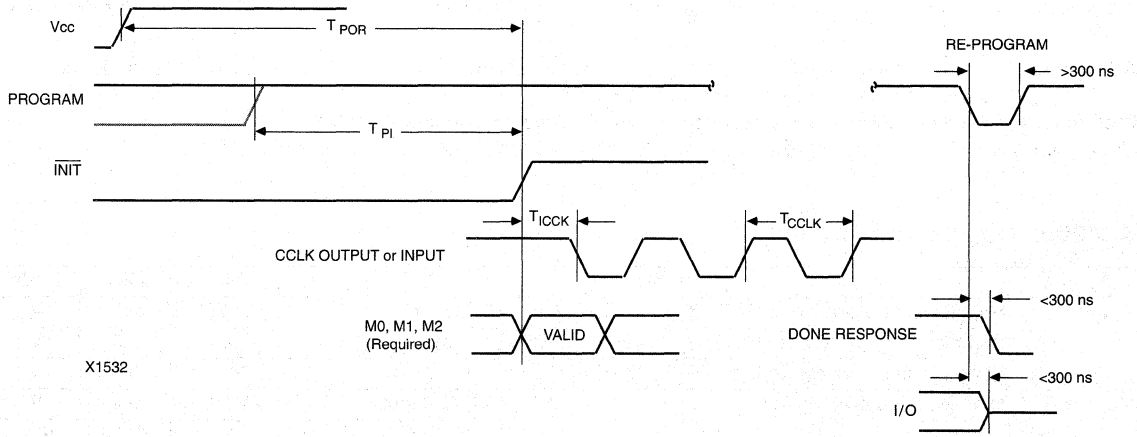
Table 24: Pin Functions During Configuration

CONFIGURATION MODE <M2:M1:M0>							
SLAVE SERIAL <1:1:1>	**MASTER SERIAL <0:0:0>**	**SYNCH. PERIPH-ERAL <0:1:1>**	**ASYNCH. PERIPH-ERAL <1:0:1>**	**MASTER PARALLEL DOWN <1:1:0>**	**MASTER PARALLEL UP <1:0:0>**	**EXPRESS <0:1:0>**	**USER OPERATION**
M2(HIGH) (I)	M2(LOW) (I)	M2(LOW) (I)	M2(HIGH) (I)	M2(HIGH) (I)	M2(HIGH) (I)	M2(LOW) (I)	(I)
M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	(O)
M0(HIGH) (I)	M0(LOW) (I)	M0(HIGH) (I)	M0(HIGH) (I)	M0(LOW) (I)	M0(LOW) (I)	M0(HIGH) (I)	(I)
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (I)	CCLK (I)
		RDY/$\overline{\text{BUSY}}$ (O)	RDY/$\overline{\text{BUSY}}$ (O)	$\overline{\text{RCLK}}$ (O)	$\overline{\text{RCLK}}$ (O)		I/O
			$\overline{\text{RS}}$ (I)				I/O
			$\overline{\text{CS0}}$ (I)				I/O
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	SGCK4-GCK5-I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO	TDO	TDO	TDO	TDO-(O)
			$\overline{\text{WS}}$ (I)	A0	A0		I/O
				A1	A1		PGCK4-GCK6-I/O
			CS1	A2	A2		I/O
				A3	A3		I/O
				A4	A4		I/O
				A5	A5		I/O
				A6	A6		I/O
				A7	A7		I/O
				A8	A8		I/O
				A9	A9		I/O
				A10	A10		I/O
				A11	A11		I/O
				A12	A12		I/O
				A13	A13		I/O
				A14	A14		I/O
				A15	A15		SGCK1-GCK7-I/O
				A16	A16		PGCK1-GCK8-I/O
				A17	A17		I/O
				A18*	A18*		I/O
				A19*	A19*		I/O
				A20*	A20*		I/O
				A21*	A21*		I/O
							ALL OTHERS

* XC4000EX only

Notes 1. A shaded table cell represents a 50 kΩ - 100 kΩ pull-up before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Configuration Switching Characteristics



Master Modes

Description		Symbol	Min	Max	Units
Power-On Reset	M0 = High	T_{POR}	10	40	ms
	M0 = Low	T_{POR}	40	130	ms
Program Latency		T_{PI}	30	200	µs per CLB column
CCLK (output) Delay		T_{ICCK}	40	250	µs
CCLK (output) Period, slow		T_{CCLK}	640	2000	ns
CCLK (output) Period, fast		T_{CCLK}	80	250	ns

Slave and Peripheral Modes

Description	Symbol	Min	Max	Units
Power-On Reset	T_{POR}	10	33	ms
Program Latency	T_{PI}	30	200	µs per CLB column
CCLK (input) Delay (required)	T_{ICCK}	4		µs
CCLK (input) Period (required)	T_{CCLK}	100		ns

XC4000E Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.[1]

XC4000E Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = -0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	4.5	5.5	V
	Supply voltage relative to GND, T_C = -55°C to +125°C	Military	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time (Note 2)			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Note 2: Typical value only. Not tested or characterized.
Note 3: Input and output measurement thresholds for TTL are 1.5 V. Input and output measurement thresholds for CMOS are 2.5 V.

XC4000E DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0mA, V_{CC} min	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)	TTL input levels		10	mA
		CMOS input levels		1	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	PQFP and MQFP packages		10	pF
		Other packages		16	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with a MakeBits Tie option.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

XC4000E Absolute Maximum Ratings

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

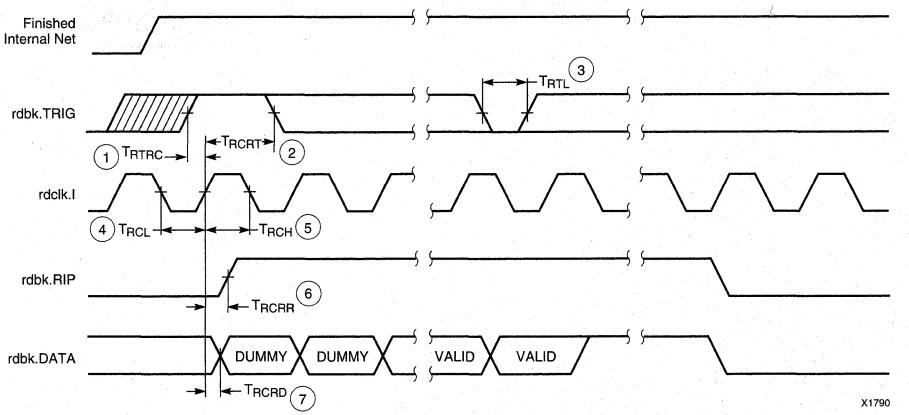
Note 1: Maximum DC overshoot or undershoot above Vcc or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000E Program Readback Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements.

The following guidelines reflect worst-case values over the recommended operating conditions.



	Description	Symbol		Min	Max	Units
rdbk.TRIG	rdbk.TRIG setup	1	T_{RTRC}	200	-	ns
	rdbk.TRIG hold	2	T_{RCRT}	50	-	ns
	rdbk.TRIG Low to abort Readback	3	T_{RTL}	100	-	ns
rdclk.1	rdbk.DATA delay	7	T_{RCRD}	-	250	ns
	rdbk.RIP delay	6	T_{RCRR}	-	250	ns
	High time	5	T_{RCH}	250	500	ns
	Low time	4	T_{RCL}	250	500	ns

Note 1: Timing parameters apply to all speed grades.

Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

XC4000E Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2		
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**		**Units**
From pad through Primary buffer, to any clock K	T_{PG}	XC4003E	7.0	4.7	4.0		ns
		XC4005E	7.0	4.7	4.0		ns
		XC4006E	7.5	5.3	4.5		ns
		XC4008E	8.0	6.1	5.2		ns
		XC4010E	11.0	6.3	5.4		ns
		XC4013E	11.5	6.8	5.8		ns
		XC4020E	12.0	7.0	6.2		ns
		XC4025E	12.5	7.2	6.3		ns
From pad through Secondary buffer, to any clock K	T_{SG}	XC4003E	7.5	5.2	4.4		ns
		XC4005E	7.5	5.2	4.4		ns
		XC4006E	8.0	5.8	4.9		ns
		XC4008E	8.5	6.6	5.6		ns
		XC4010E	11.5	6.8	5.8		ns
		XC4013E	12.0	7.3	6.2		ns
		XC4020E	12.5	7.5	6.6		ns
		XC4025E	13.0	7.7	6.8		ns
					ADVANCE		

XC4000E Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2		
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**		**Units**
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4003E	9.2	5.0	4.3		ns
		XC4005E	9.5	6.0	5.1		ns
		XC4006E	12.0	7.0	6.2		ns
		XC4008E	12.5	8.0	7.0		ns
		XC4010E	15.0	9.0	8.1		ns
		XC4013E	16.0	11.0	9.9		ns
		XC4020E	17.0	13.9	12.5		ns
		XC4025E	18.0	16.9	15.2		ns
Full length, both pull-ups, inputs from internal logic	T_{WAFL}	XC4003E	12.0	7.0	6.0		ns
		XC4005E	12.5	8.0	6.8		ns
		XC4006E	14.0	9.0	7.9		ns
		XC4008E	16.0	10.0	8.8		ns
		XC4010E	18.0	11.0	9.7		ns
		XC4013E	19.0	13.0	11.7		ns
		XC4020E	20.0	15.5	14.0		ns
		XC4025E	21.0	18.9	17.0		ns
Half length, one pull-up, inputs from IOB I-pins	T_{WAO}	XC4003E	10.5	6.0	5.1		ns
		XC4005E	10.5	7.0	6.0		ns
		XC4006E	13.5	8.0	6.8		ns
		XC4008E	14.0	9.0	7.9		ns
		XC4010E	16.0	10.0	8.8		ns
		XC4013E	17.0	12.0	10.8		ns
		XC4020E	18.0	15.0	13.5		ns
		XC4025E	19.0	17.6	15.8		ns
Half length, one pull-up, inputs from internal logic	T_{WAOL}	XC4003E	12.0	8.0	6.8		ns
		XC4005E	12.5	9.0	7.7		ns
		XC4006E	14.0	10.0	8.5		ns
		XC4008E	16.0	11.0	9.4		ns
		XC4010E	18.0	12.0	10.2		ns
		XC4013E	19.0	14.0	11.9		ns
		XC4020E	20.0	16.8	14.3		ns
		XC4025E	21.0	19.6	16.7		ns
					ADVANCE		

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPF} or T_{OPS}), as listed under "IOB Switching Characteristic Guidelines."

XC4000E Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (LL): I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T_{IO1}	XC4003E	5.0	4.2	3.4	ns
		XC4005E	5.0	5.0	4.0	ns
		XC4006E	6.0	5.9	4.7	ns
		XC4008E	7.0	6.3	5.0	ns
		XC4010E	8.0	6.4	5.1	ns
		XC4013E	9.0	7.2	5.7	ns
		XC4020E	10.0	8.2	6.6	ns
		XC4025E	11.0	9.1	7.3	ns
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T_{IO2}	XC4003E	5.0	4.2	3.6	ns
		XC4005E	6.0	5.3	4.5	ns
		XC4006E	7.8	6.4	5.4	ns
		XC4008E	8.1	6.8	5.8	ns
		XC4010E	10.5	6.9	5.9	ns
		XC4013E	11.0	7.7	6.5	ns
		XC4020E	12.0	8.7	7.4	ns
		XC4025E	12.0	9.6	8.2	ns
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T_{ON}	XC4003E	5.5	4.6	3.9	ns
		XC4005E	7.0	6.0	5.4	ns
		XC4006E	7.5	6.7	5.7	ns
		XC4008E	8.0	7.1	6.0	ns
		XC4010E	8.5	7.3	6.2	ns
		XC4013E	8.7	7.5	6.4	ns
		XC4020E	11.0	8.4	7.1	ns
		XC4025E	11.0	8.4	7.1	ns
T going High to TBUF going inactive, not driving LL	T_{OFF}	All devices	1.8	1.5	1.3	ns
T going High to LL going from Low to High, pulled up by a single resistor. (Note 2)	T_{PUS}	XC4003E	20.0	14.0	11.9	ns
		XC4005E	23.0	16.0	13.6	ns
		XC4006E	25.0	18.0	15.3	ns
		XC4008E	27.0	20.0	17.0	ns
		XC4010E	29.0	22.0	18.7	ns
		XC4013E	32.0	26.0	22.1	ns
		XC4020E	35.0	32.5	27.6	ns
		XC4025E	42.0	39.1	33.2	ns
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T_{PUF}	XC4003E	9.0	7.0	6.0	ns
		XC4005E	10.0	8.0	6.8	ns
		XC4006E	11.5	9.0	7.7	ns
		XC4008E	12.5	10.0	8.5	ns
		XC4010E	13.5	11.0	9.4	ns
		XC4013E	15.0	13.0	11.0	ns
		XC4020E	16.0	14.8	12.6	ns
		XC4025E	18.0	16.5	14.0	ns
					ADVANCE	

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: This value includes a minimum load. The value reported by LCA2XNF -S is increased to allow for potentially heavy loading, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

XC4000E CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Combinatorial Delays									
F/G inputs to X/Y outputs	T_{ILO}		2.7		2.0		1.6		
F/G inputs via H' to X/Y outputs	T_{IHO}		4.7		4.3		2.7		
C inputs via SR through H' to X/Y outputs	T_{HH0O}		4.1		3.3		2.4		
C inputs via H' to X/Y outputs	T_{HH1O}		3.7		3.6		2.2		
C inputs via DIN through H' to X/Y outputs	T_{HH2O}		4.5		3.6		2.6		
CLB Fast Carry Logic									
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		3.2		2.6		2.1		
Add/Subtract input (F3) to COUT	T_{ASCY}		5.5		4.4		3.7		
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.7		1.7		1.4		
CIN through function generators to X/Y outputs	T_{SUM}		3.8		3.3		2.6		
CIN to COUT, bypass function generators	T_{BYP}		1.0		0.7		0.6		
Sequential Delays									
Clock K to outputs Q	T_{CKO}		3.7		2.8		2.8		
Setup Time before Clock K									
F/G inputs	T_{ICK}	4.0		3.0		2.4			
F/G inputs via H'	T_{IHCK}	6.1		4.6		3.9			
C inputs via H0 through H'	T_{HH0CK}	4.5		3.6		3.5			
C inputs via H1 through H'	T_{HH1CK}	5.0		4.1		3.3			
C inputs via H2 through H'	T_{HH2CK}	4.8		3.8		3.7			
C inputs via DIN	T_{DICK}	3.0		2.4		2.0			
C inputs via EC	T_{ECCK}	4.0		3.0		2.6			
C inputs via S/R, going Low (inactive)	T_{RCK}	4.2		4.0		4.0			
C_{IN} input via F'/G'	T_{CCK}								
C_{IN} input via F'/G' and H'	T_{CHCK}								
						ADVANCE			

XC4000E CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Hold Time after Clock K									
F/G inputs	T_{CKI}	0		0		0			
F/G inputs via H'	T_{CKIH}	0		0		0			
C inputs via H0 through H'	T_{CKHH0}	0		0		0			
C inputs via H1 through H'	T_{CKHH1}	0		0		0			
C inputs via H2 through H'	T_{CKHH2}	0		0		0			
C inputs via DIN	T_{CKDI}	0		0		0			
C inputs via EC	T_{CKEC}	0		0		0			
C inputs via SR, going Low (inactive)	T_{CKR}	0		0		0			
Clock									
Clock High time	T_{CH}	4.5		4.0		4.0			
Clock Low time	T_{CL}	4.5		4.0		4.0			
Set/Reset Direct									
Width (High)	T_{RPW}	5.5		4.0		4.0			
Delay from C inputs via S/R, going High to Q	T_{RIO}		6.5		4.0		4.0		
Master Set/Reset (Note 1)									
Width (High or Low)	T_{MRW}	13.0		11.5		11.5			
Delay from Global Set/Reset net to Q	T_{MRQ}		23.0		18.7		17.4		
Global Set/Reset inactive to first active clock K edge	T_{MRK}								
Toggle Frequency[2] (MHz) (Note 2)	F_{TOG}		111		125		125		
						ADVANCE			

Note 1: Timing is based on the XC4005E. For other devices see the XACT timing calculator.
Note 2: Export Control Max. flip-flop toggle rate.

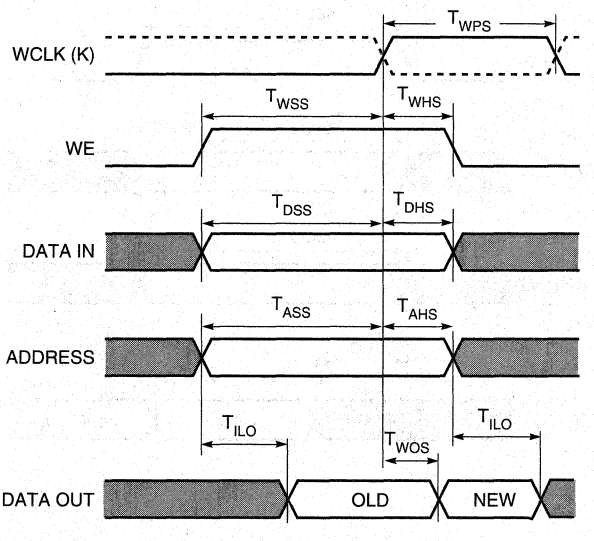
XC4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2	
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Write Operation								
Address write cycle time	16x2	T_{WCS}	15.0		14.4		11.6	
(clock K period)	32x1	T_{WCTS}	15.0		14.4		11.6	
Clock K pulse width	16x2	T_{WPS}	7.5	1 ms	7.2	1 ms	5.8	1 ms
(active edge)	32x1	T_{WPTS}	7.5	1 ms	7.2	1 ms	5.8	1 ms
Address setup time	16x2	T_{ASS}	2.8		2.4		2.0	
before clock K	32x1	T_{ASTS}	2.8		2.4		2.0	
Address hold time	16x2	T_{AHS}	0		0		0	
after clock K	32x1	T_{AHTS}	0		0		0	
DIN setup time	16x2	T_{DSS}	3.5		3.2		2.7	
before clock K	32x1	T_{DSTS}	2.5		1.9		1.7	
DIN hold time	16x2	T_{DHS}	0		0		0	
after clock K	32x1	T_{DHTS}	0		0		0	
WE setup time	16x2	T_{WSS}	2.2		2.0		1.6	
before clock K	32x1	T_{WSTS}	2.2		2.0		1.6	
WE hold time	16x2	T_{WHS}	0		0		0	
after clock K	32x1	T_{WHTS}	0		0		0	
Data valid	16x2	T_{WOS}		10.3		8.8		6.3
after clock K	32x1	T_{WOTS}		11.6		10.3		7.4
							ADVANCE	

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.



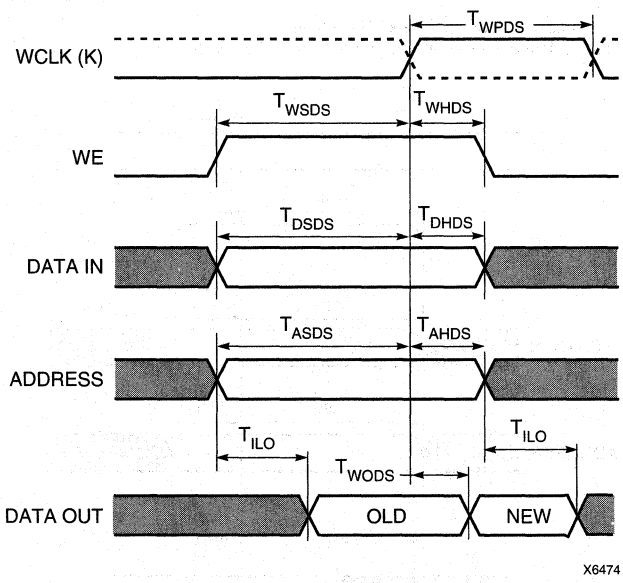
XC4000E CLB Edge-Triggered (Synchronous) Dual-Port RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2	
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Write Operation								
Address write cycle time (clock K period)	16x1	T_{WCDS}	15.0		14.4		11.6	
Clock K pulse width (active edge)	16x1	T_{WPDS}	7.5	1 ms	7.2	1 ms	5.8	1 ms
Address setup time before clock K	16x1	T_{ASDS}	2.8		2.5		2.1	
Address hold time after clock K	16x1	T_{AHDS}	0		0		0	
DIN setup time before clock K	16x1	T_{DSDS}	2.2		1.9		1.6	
DIN hold time after clock K	16x1	T_{DHDS}	0		0		0	
WE setup time before clock K	16x1	T_{WSDS}	2.2		2.0		1.6	
WE hold time after clock K	16x1	T_{WHDS}	0.3		0		0	
Data valid after clock K	16x1	T_{WODS}		10.0		7.8		6.2
							ADVANCE	

Note: Applicable Read timing specifications are identical to16x2 Level-Sensitive Read timing.



XC4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

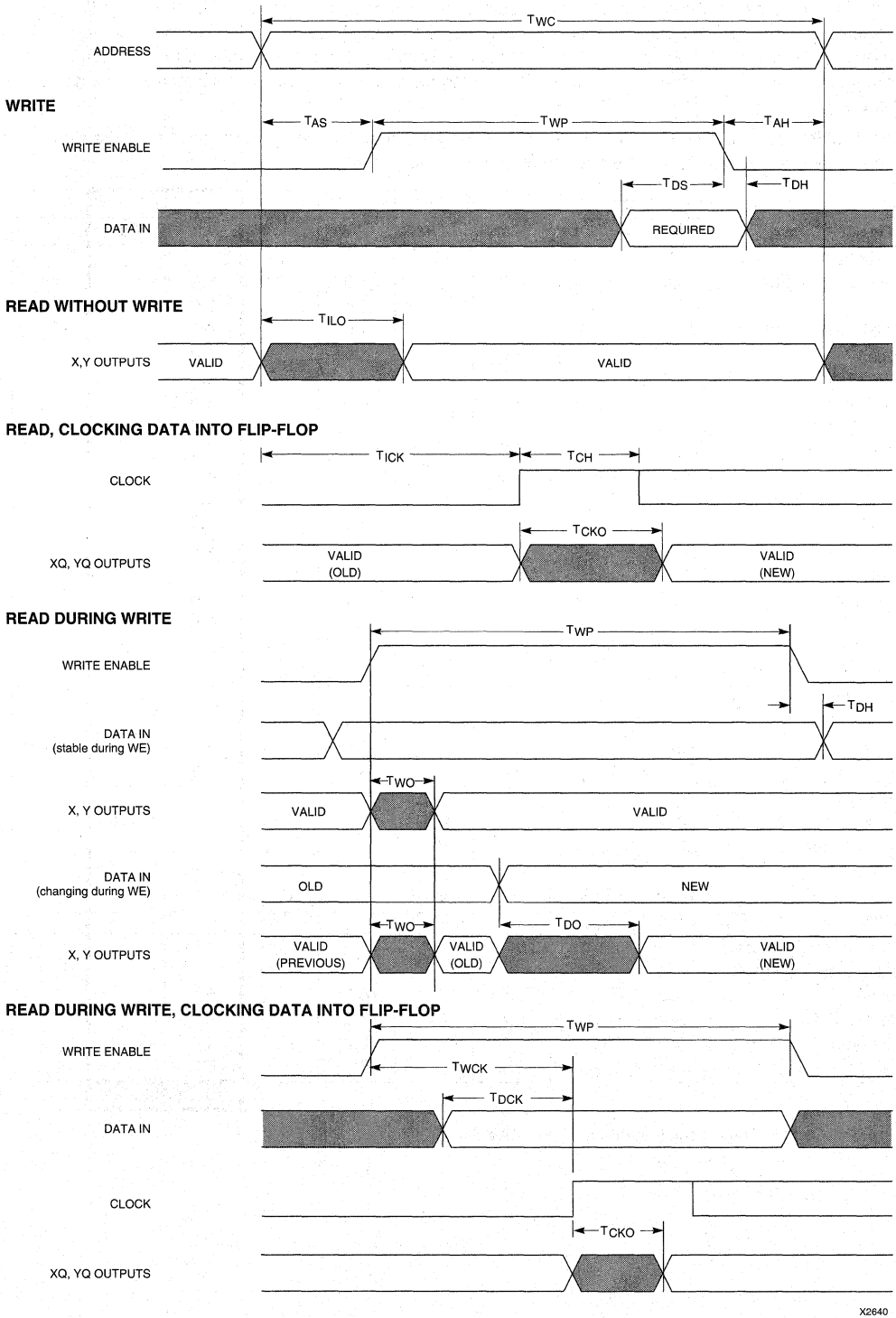
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2			
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Write Operation										
Address write cycle time	16x2	T_{WC}	8.0		8.0		8.0			
	32x1	T_{WCT}	8.0		8.0		8.0			
Write Enable pulse width	16x2	T_{WP}	4.0		4.0		4.0			
(High)	32x1	T_{WPT}	4.0		4.0		4.0			
Address setup time	16x2	T_{AS}	2.0		2.0		2.0			
before WE	32x1	T_{AST}	2.0		2.0		2.0			
Address hold time	16x2	T_{AH}	2.5		2.0		2.0			
after end of WE	32x1	T_{AHT}	2.0		2.0		2.0			
DIN setup time	16x2	T_{DS}	4.0		2.2		0.8			
before end of WE	32x1	T_{DST}	5.0		2.2		0.8			
DIN hold time	16x2	T_{DH}	2.0		2.0		2.0			
after end of WE	32x1	T_{DHT}	2.0		2.0		2.0			
Read Operation										
Address read cycle time	16x2	T_{RC}	4.5		3.1		2.6			
	32x1	T_{RCT}	6.5		5.5		3.8			
Data valid after address	16x2	T_{ILO}		2.7		2.0		1.6		
change (no Write Enable)	32x1	T_{IHO}		4.7		4.3		2.7		
Read Operation, Clocking Data into Flip-Flop										
Address setup time	16x2	T_{ICK}	4.0		3.0		2.4			
before clock K	32x1	T_{IHCK}	6.1		4.6		3.9			
Read During Write										
Data valid after WE goes	16x2	T_{WO}		10.0		6.0		4.9		
active (DIN stable	32x1	T_{WOT}		12.0		7.3		5.6		
before WE)										
Data valid after DIN	16x2	T_{DO}		9.0		6.6		5.8		
(DIN changes during WE)	32x1	T_{DOT}		11.0		7.6		6.2		
Read During Write, Clocking Data into Flip-Flop										
WE setup time	16x2	T_{WCK}	8.0		6.0		5.1			
before clock K	32x1	T_{WCKT}	9.6		6.8		5.8			
Data setup time	16x2	T_{DCK}	7.0		5.2		4.4			
before clock K	32x1	T_{DCKT}	8.0		6.2		5.3			
							ADVANCE			

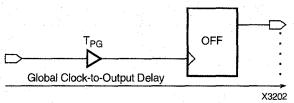
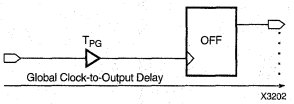
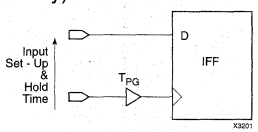
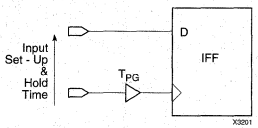
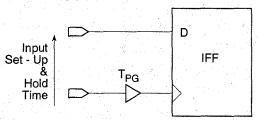
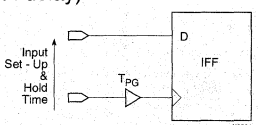
Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XC4000E CLB Level-Sensitive RAM Timing Characteristics



XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between the two methods, the values listed below should be used, and the derived values must be ignored. All values are expressed in units of nanoseconds.

		Speed Grade	-4	-3	-2
Description	**Symbol**	**Device**			
Global Clock to Output (fast) using OFF 	T_{ICKOF} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	12.5 14.0 14.5 15.0 16.0 16.5 17.0 17.0	10.2 10.7 10.7 10.8 10.9 11.0 11.0 12.6	8.7 9.1 9.1 9.2 9.3 9.4 9.4 10.7
Global Clock to Output (slew-limited) using OFF 	T_{ICKO} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	16.5 18.0 18.5 19.0 20.0 20.5 21.0 21.0	14.0 14.7 14.7 14.8 14.9 15.0 15.1 15.3	11.5 12.0 12.0 12.1 12.2 12.8 12.8 13.0
Input Setup Time, using IFF (no delay) 	T_{PSUF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	2.5 2.0 1.9 1.4 1.0 0.5 0 0	2.3 1.2 1.0 0.6 0.2 0 0 0	2.3 1.2 1.0 0.6 0.2 0 0 0
Input Hold Time, using IFF (no delay) 	T_{PHF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	4.0 4.6 5.0 6.0 6.0 7.0 7.5 8.0	4.0 4.5 4.7 5.1 5.5 6.5 6.7 7.0	4.0 4.5 4.7 5.1 5.5 5.5 5.7 5.9
Input Setup Time, using IFF (with delay) 	T_{PSU} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	8.5 8.5 8.5 8.5 8.5 8.5 9.5 9.5	7.0 7.0 7.0 7.0 7.0 7.0 7.0 7.6	6.0 6.0 6.0 6.0 6.0 6.0 6.0 6.5
Input Hold Time, using IFF (with delay) 	T_{PH} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	0 0 0 0 0 0 υ 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

OFF = Output Flip-Flop IFF = Input Flip-Flop or Latch

ADVANCE

XC4000E IOB Input Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2	
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Propagation Delays								
(TTL Inputs)								
Pad to I1, I2	T_{PID}	All devices		3.0		2.5		2.0
Pad to I1, I2 via transparent								
latch, no delay	T_{PLI}	All devices		4.8		3.6		3.6
with delay	T_{PDLI}	XC4003E		10.4		9.3		7.0
		XC4005E		10.8		9.6		7.3
		XC4006E		10.8		10.2		7.8
		XC4008E		10.8		10.6		8.1
		XC4010E		11.0		10.8		8.2
		XC4013E		11.4		11.2		8.5
		XC4020E		13.8		12.4		9.5
		XC4025E		13.8		13.7		9.5
(CMOS Inputs)								
Pad to I1, I2	T_{PIDC}	All devices		5.5		4.1		3.7
Pad to I1, I2 via transparent								
latch, no delay	T_{PLIC}	All devices		8.8		6.8		6.2
with delay	T_{PDLIC}	XC4003E		16.5		12.4		11.0
		XC4005E		16.5		13.2		11.9
		XC4006E		16.8		13.4		12.1
		XC4008E		17.3		13.8		12.4
		XC4010E		17.5		14.0		12.6
		XC4013E		18.0		14.4		13.0
		XC4020E		20.8		15.6		14.0
		XC4025E		20.8		15.6		14.0
(TTL or CMOS)								
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		5.6		2.8		2.8
Clock (IK) to I1, I2								
(latch enable, active Low)	T_{IKLI}	All devices		6.2		4.0		3.9
Hold Times (Note 1)								
Pad to Clock (IK), no delay	T_{IKPI}	All devices	0		0		0	
with delay	T_{IKPID}	All devices	0		0		0	
Clock Enable (EC) to Clock (IK),								
no delay	T_{IKEC}	All devices	1.5		1.5		0.9	
with delay	T_{IKECD}	All devices	0		0		0	
							ADVANCE	

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Input Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2	
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Setup Times (TTL Inputs)								
Pad to Clock (IK), no delay	T_{PICK}	All devices	4.0		2.6		1.7	
with delay	T_{PICKD}	XC4003E	10.9		8.2		5.5	
		XC4005E	10.9		8.7		5.5	
		XC4006E	10.9		9.2		6.6	
		XC4008E	11.1		9.6		6.9	
		XC4010E	11.3		9.8		7.0	
		XC4013E	11.8		10.2		7.3	
		XC4020E	14.0		11.4		8.2	
		XC4025E	14.0		11.4		8.2	
(CMOS Inputs)								
Pad to Clock (IK), no delay	T_{PICKC}	All devices	6.0		3.3		2.4	
with delay	T_{PICKDC}	XC4003E	12.0		8.8		6.2	
		XC4005E	12.0		9.7		6.2	
		XC4006E	12.3		9.9		7.3	
		XC4008E	12.8		10.3		7.6	
		XC4010E	13.0		10.5		7.7	
		XC4013E	13.5		10.9		8.0	
		XC4020E	16.0		12.1		8.9	
		XC4025E	16.0		12.1		8.9	
(TTL or CMOS)								
Clock Enable (EC) to Clock (IK), no delay	T_{ECIK}	All devices	3.5		2.5		2.0	
with delay	T_{ECIKD}	XC4003E	10.4		8.1		5.6	
		XC4005E	10.4		8.5		5.6	
		XC4006E	10.4		9.1		6.9	
		XC4008E	10.4		9.5		7.2	
		XC4010E	10.7		9.7		7.3	
		XC4013E	11.1		10.1		7.6	
		XC4020E	14.0		11.3		8.5	
		XC4025E	14.0		11.3		8.5	
Global Set/Reset (Note 3)								
Delay from GSR net through Q to I1, I2	T_{RRI}			12.0		7.8		6.8
GSR width	T_{MRW}		13.0		11.5		11.5	
GSR inactive to first active Clock (IK) edge	T_{MRI}							

ADVANCE

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E IOB Output Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Propagation Delays (TTL Output Levels)							
Clock (OK) to Pad, fast	T_{OKPOF}		7.5		6.5		4.5
slew-rate limited	T_{OKPOS}		11.5		9.5		7.0
Output (O) to Pad, fast	T_{OPF}		8.0		5.5		4.8
slew-rate limited	T_{OPS}		12.0		8.5		7.3
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		5.0		4.2		3.8
3-state to Pad active and valid, fast	T_{TSONF}		9.7		8.1		7.3
slew-rate limited	T_{TSONS}		13.7		11.1		9.8
Propagation Delays (CMOS Output Levels)							
Clock (OK) to Pad, fast	T_{OKPOFC}		9.5		7.8		7.0
slew-rate limited	T_{OKPOSC}		13.5		11.6		10.4
Output (O) to Pad, fast	T_{OPFC}		10.0		9.7		8.7
slew-rate limited	T_{OPSC}		14.0		13.4		12.1
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZC}		5.2		4.3		3.9
3-state to Pad active and valid, fast	T_{TSONFC}		9.1		7.6		6.8
slew-rate limited	T_{TSONSC}		13.1		11.4		10.2
						ADVANCE	

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Output Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Setup and Hold									
Output (O) to clock (OK) setup time	T_{OOK}	5.0		4.6		3.8			
Output (O) to clock (OK) hold time	T_{OKO}	0		0		0			
Clock Enable (EC) to clock (OK) setup	T_{ECOK}	4.8		3.5		2.5			
Clock Enable (EC) to clock (OK) hold	T_{OKEC}	1.2		1.2		0.5			
Clock									
Clock High	T_{CH}	4.5		4.0		4.0			
Clock Low	T_{CL}	4.5		4.0		4.0			
Global Set/Reset (Note 3)									
Delay from GSR net to Pad	T_{RPO}		15.0		11.8		8.7		
GSR width	T_{MRW}	13.0		11.5		11.5			
GSR inactive to first active clock (OK) edge	T_{MRO}								
						ADVANCE			

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Setup and Hold									
Input (TDI) to clock (TCK) setup time	T_{TDITCK}								
Input (TDI) to clock (TCK) hold time	T_{TCKTDI}								
Input (TMS) to clock (TCK) setup time	T_{TMSTCK}								
Input (TMS) to clock (TCK) hold time	T_{TCKTMS}								
Propagation Delay									
Clock (TCK) to Pad (TDO)	T_{TCKPO}								
Clock									
Clock (TCK) High	T_{TCKH}								
Clock (TCK) Low	T_{TCKL}								
Power-On Reset									
JTAG operation after valid Vcc	T_{RJTAG}								
						ADVANCE			

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000L Switching Characteristics

XC4000L timing parameters were not available at the time this document was released. See the Xilinx WEBLINX at http://www.xilinx.com for the latest available information.

XC4000EX Switching Characteristics

XC4000EX timing parameters were not available at the time this document was released. See the Xilinx WEBLINX at http://www.xilinx.com for the latest available information.

XC4000XL Switching Characteristics

XC4000XL timing parameters were not available at the time this document was released. See the Xilinx WEBLINX at http://www.xilinx.com for the latest available information.

Device-Specific Pinout Tables

Pin Locations for XC4003E Devices

XC4003E Pad Name	PC 84	PQ 100	VQ 100	PG 120	Bndry Scan
VCC	P2	P92	P89	G3	-
I/O (A8)	P3	P93	P90	G1	32
I/O (A9)	P4	P94	P91	F1	35
I/O	-	P95	P92	E1	38
I/O	-	P96	P93	F2	41
I/O (A10)	P5	P97	P94	F3	44
I/O (A11)	P6	P98	P95	D1	47
I/O (A12)	P7	P99	P96	C1	50
I/O (A13)	P8	P100	P97	D2	53
I/O (A14)	P9	P1	P98	C2	56
I/O, SGCK1 (A15)	P10	P2	P99	D3	59
VCC	P11	P3	P100	C3	-
GND	P12	P4	P1	C4	-
I/O, PGCK1 (A16)	P13	P5	P2	B2	62
I/O (A17)	P14	P6	P3	B3	65
I/O, TDI	P15	P7	P4	C5	68
I/O, TCK	P16	P8	P5	B4	71
I/O, TMS	P17	P9	P6	B5	74
I/O	P18	P10	P7	A4	77
I/O	-	-	-	C6	80
I/O	-	P11	P8	A5	83
I/O	P19	P12	P9	B6	86
I/O	P20	P13	P10	A6	89
GND	P21	P14	P11	B7	-
VCC	P22	P15	P12	C7	-
I/O	P23	P16	P13	A7	92
I/O	P24	P17	P14	A8	95
I/O	-	P18	P15	A9	98
I/O	-	-	-	B8	101
I/O	P25	P19	P16	C8	104
I/O	P26	P20	P17	A10	107
I/O	P27	P21	P18	B9	110
I/O	-	P22	P19	A11	113
I/O	P28	P23	P20	C9	116
I/O, SCGK2	P29	P24	P21	A12	119
O (M1)	P30	P25	P22	B11	122
GND	P31	P26	P23	C10	-
I (M0)	P32	P27	P24	C11	125
VCC	P33	P28	P25	D11	-
I (M2)	P34	P29	P26	B12	126
I/O, PGCK2	P35	P30	P27	C12	127
I/O (HDC)	P36	P31	P28	A13	130
I/O	-	P32	P29	D12	133
I/O ($\overline{\text{LDC}}$)	P37	P33	P30	C13	136
I/O	P38	P34	P31	E12	139
I/O	P39	P35	P32	D13	142
I/O	-	P36	P33	F11	145
I/O	-	P37	P34	E13	148
I/O	P40	P38	P35	F12	151
I/O ($\overline{\text{INIT}}$)	P41	P39	P36	F13	154
VCC	P42	P40	P37	G12	-
GND	P43	P41	P38	G11	-
I/O	P44	P42	P39	G13	157
I/O	P45	P43	P40	H13	160
I/O	-	P44	P41	J13	163
I/O	-	P45	P42	H12	166
I/O	P46	P46	P43	H11	169
I/O	P47	P47	P44	K13	172
I/O	P48	P48	P45	J12	175
I/O	P49	P49	P46	L13	178
I/O	P50	P50	P47	M13	181
I/O, SGCK3	P51	P51	P48	L12	184
GND	P52	P52	P49	K11	-
DONE	P53	P53	P50	L11	-
VCC	P54	P54	P51	L10	-
$\overline{\text{PROGRAM}}$	P55	P55	P52	M12	-
I/O (D7)	P56	P56	P53	M11	187
I/O, PGCK3	P57	P57	P54	N13	190
I/O (D6)	P58	P58	P55	M10	193
I/O	-	P59	P56	N11	196
I/O (D5)	P59	P60	P57	M9	199
I/O ($\overline{\text{CS0}}$)	P60	P61	P58	N10	202
I/O	-	P62	P59	L8	205
I/O	-	P63	P60	N9	208
I/O (D4)	P61	P64	P61	M8	211
I/O	P62	P65	P62	N8	214
VCC	P63	P66	P63	M7	-
GND	P64	P67	P64	L7	-
I/O (D3)	P65	P68	P65	N7	217
I/O ($\overline{\text{RS}}$)	P66	P69	P66	N6	220
I/O	-	P70	P67	N5	223
I/O	-	-	-	M6	226
I/O (D2)	P67	P71	P68	L6	229
I/O	P68	P72	P69	N4	232
I/O (D1)	P69	P73	P70	M5	235
I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	P70	P74	P71	N3	238
I/O (D0, DIN)	P71	P75	P72	N2	241
I/O, SGCK4 (DOUT)	P72	P76	P73	M3	244
CCLK	P73	P77	P74	L4	-
VCC	P74	P78	P75	L3	-
O, TDO	P75	P79	P76	M2	0
GND	P76	P80	P77	K3	-
I/O (A0, $\overline{\text{WS}}$)	P77	P81	P78	L2	2
I/O, PGCK4 (A1)	P78	P82	P79	N1	5
I/O (CS1, A2)	P79	P83	P80	K2	8
I/O (A3)	P80	P84	P81	L1	11
I/O (A4)	P81	P85	P82	J2	14
I/O (A5)	P82	P86	P83	K1	17
I/O	-	P87	P84	H3	20
I/O	-	P88	P85	J1	23
I/O (A6)	P83	P89	P86	H2	26
I/O (A7)	P84	P90	P87	H1	29
GND	P1	P91	P88	G2	-

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Additional No Connect (N.C.) Connections on PG120 Package

PG120	PG120	PG120	PG120
A1	B13	J11	M4
A2	E2	K12	N12
A3	E3	L5	
B1	E11	L9	
B10	J3	M1	

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Pin Locations for XC4005E/L Devices

XC4005 E/L Pad Name	PC 84	PQ 100	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
VCC	P2	P92	P128	H3	P142	P183	-
I/O (A8)	P3	P93	P129	H1	P143	P184	44
I/O (A9)	P4	P94	P130	G1	P144	P185	47
I/O	-	P95	P131	G2	P145	P186	50
I/O	-	P96	P132	G3	P146	P187	53
I/O (A10)	P5	P97	P133	F1	P147	P190	56
I/O (A11)	P6	P98	P134	F2	P148	P191	59
I/O	-	-	P135	E1	P149	P192	62
I/O	-	-	P136	E2	P150	P193	65
GND	-	-	P137	F3	P151	P194	-
I/O (A12)	P7	P99	P138	E3	P154	P199	68
I/O (A13)	P8	P100	P139	C1	P155	P200	71
I/O	-	-	P140	C2	P156	P201	74
I/O	-	-	P141	D3	P157	P202	77
I/O (A14)	P9	P1	P142	B1	P158	P203	80
I/O, SGCK1 (A15)	P10	P2	P143	B2	P159	P204	83
VCC	P11	P3	P144	C3	P160	P205	-
GND	P12	P4	P1	C4	P1	P2	-
I/O, PGCK1 (A16)	P13	P5	P2	B3	P2	P4	86
I/O (A17)	P14	P6	P3	A1	P3	P5	89
I/O	-	-	P4	A2	P4	P6	92
I/O	-	-	P5	C5	P5	P7	95
I/O, TDI	P15	P7	P6	B4	P6	P8	98
I/O, TCK	P16	P8	P7	A3	P7	P9	101
GND	-	-	P8	C6	P10	P14	-
I/O	-	-	P9	B5	P11	P15	104
I/O	-	-	P10	B6	P12	P16	107
I/O, TMS	P17	P9	P11	A5	P13	P17	110
I/O	P18	P10	P12	C7	P14	P18	113
I/O	-	-	P13	B7	P15	P21	116
I/O	-	P11	P14	A6	P16	P22	119
I/O	P19	P12	P15	A7	P17	P23	122
I/O	P20	P13	P16	A8	P18	P24	125
GND	P21	P14	P17	C8	P19	P25	-
VCC	P22	P15	P18	B8	P20	P26	-
I/O	P23	P16	P19	C9	P21	P27	128
I/O	P24	P17	P20	B9	P22	P28	131
I/O	-	P18	P21	A9	P23	P29	134
I/O	-	-	P22	B10	P24	P30	137
I/O	P25	P19	P23	C10	P25	P33	140
I/O	P26	P20	P24	A10	P26	P34	143
I/O	-	-	P25	A11	P27	P35	146
I/O	-	-	P26	B11	P28	P36	149

XC4005 E/L Pad Name	PC 84	PQ 100	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
GND	-	-	P27	C11	P29	P37	-
I/O	P27	P21	P28	B12	P32	P42	152
I/O	-	P22	P29	A13	P33	P43	155
I/O	-	-	P30	A14	P34	P44	158
I/O	-	-	P31	C12	P35	P45	161
I/O	P28	P23	P32	B13	P36	P46	164
I/O, SCGK2	P29	P24	P33	B14	P37	P47	167
O (M1)	P30	P25	P34	A15	P38	P48	170
GND	P31	P26	P35	C13	P39	P49	-
I (M0)	P32	P27	P36	A16	P40	P50	173
VCC	P33	P28	P37	C14	P41	P55	-
I (M2)	P34	P29	P38	B15	P42	P56	174
I/O, PGCK2	P35	P30	P39	B16	P43	P57	175
I/O (HDC)	P36	P31	P40	D14	P44	P58	178
I/O	-	-	P41	C15	P45	P59	181
I/O	-	-	P42	D15	P46	P60	184
I/O	-	P32	P43	E14	P47	P61	187
I/O ($\overline{\text{LDC}}$)	P37	P33	P44	C16	P48	P62	190
GND	-	-	P45	F14	P51	P67	-
I/O	-	-	P46	F15	P52	P68	193
I/O	-	-	P47	E16	P53	P69	196
I/O	P38	P34	P48	F16	P54	P70	199
I/O	P39	P35	P49	G14	P55	P71	202
I/O	-	P36	P50	G15	P56	P74	205
I/O	-	P37	P51	G16	P57	P75	208
I/O	P40	P38	P52	H16	P58	P76	211
I/O ($\overline{\text{INIT}}$)	P41	P39	P53	H15	P59	P77	214
VCC	P42	P40	P54	H14	P60	P78	-
GND	P43	P41	P55	J14	P61	P79	-
I/O	P44	P42	P56	J15	P62	P80	217
I/O	P45	P43	P57	J16	P63	P81	220
I/O	-	P44	P58	K16	P64	P82	223
I/O	-	P45	P59	K15	P65	P83	226
I/O	P46	P46	P60	K14	P66	P86	229
I/O	P47	P47	P61	L16	P67	P87	232
I/O	-	-	P62	M16	P68	P88	235
I/O	-	-	P63	L15	P69	P89	238
GND	-	-	P64	L14	P70	P90	-
I/O	P48	P48	P65	P16	P73	P95	241
I/O	P49	P49	P66	M14	P74	P96	244
I/O	-	-	P67	N15	P75	P97	247
I/O	-	-	P68	P15	P76	P98	250
I/O	P50	P50	P69	N14	P77	P99	253
I/O, SGCK3	P51	P51	P70	R16	P78	P100	256
GND	P52	P52	P71	P14	P79	P101	-

XC4005 E/L Pad Name	PC 84	PQ 100	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
DONE	P53	P53	P72	R15	P80	P103	-
VCC	P54	P54	P73	P13	P81	P106	-
$\overline{\text{PRO-GRAM}}$	P55	P55	P74	R14	P82	P108	-
I/O (D7)	P56	P56	P75	T16	P83	P109	259
I/O, PGCK3	P57	P57	P76	T15	P84	P110	262
I/O	-	-	P77	R13	P85	P111	265
I/O	-	-	P78	P12	P86	P112	268
I/O (D6)	P58	P58	P79	T14	P87	P113	271
I/O	-	P59	P80	T13	P88	P114	274
GND	-	-	P81	P11	P91	P119	-
I/O	-	-	P82	R11	P92	P120	277
I/O	-	-	P83	T11	P93	P121	280
I/O (D5)	P59	P60	P84	T10	P94	P122	283
I/O ($\overline{\text{CS0}}$)	P60	P61	P85	P10	P95	P123	286
I/O	-	P62	P86	R10	P96	P126	289
I/O	-	P63	P87	T9	P97	P127	292
I/O (D4)	P61	P64	P88	R9	P98	P128	295
I/O	P62	P65	P89	P9	P99	P129	298
VCC	P63	P66	P90	R8	P100	P130	-
GND	P64	P67	P91	P8	P101	P131	-
I/O (D3)	P65	P68	P92	T8	P102	P132	301
I/O ($\overline{\text{RS}}$)	P66	P69	P93	T7	P103	P133	304
I/O	-	P70	P94	T6	P104	P134	307
I/O	-	-	P95	R7	P105	P135	310
I/O (D2)	P67	P71	P96	P7	P106	P138	313
I/O	P68	P72	P97	T5	P107	P139	316
I/O	-	-	P98	R6	P108	P140	319
I/O	-	-	P99	T4	P109	P141	322
GND	-	-	P100	P6	P110	P142	-
I/O (D1)	P69	P73	P101	T3	P113	P147	325
I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	P70	P74	P102	P5	P114	P148	328
I/O	-	-	P103	R4	P115	P149	331
I/O	-	-	P104	R3	P116	P150	334
I/O (D0, DIN)	P71	P75	P105	P4	P117	P151	337
I/O, SGCK4 (DOUT)	P72	P76	P106	T2	P118	P152	340
CCLK	P73	P77	P107	R2	P119	P153	-
VCC	P74	P78	P108	P3	P120	P154	-
O, TDO	P75	P79	P109	T1	P121	P159	0
GND	P76	P80	P110	N3	P122	P160	-
I/O (A0, $\overline{\text{WS}}$)	P77	P81	P111	R1	P123	P161	2
I/O, PGCK4 (A1)	P78	P82	P112	P2	P124	P162	5
I/O	-	-	P113	N2	P125	P163	8
I/O	-	-	P114	M3	P126	P164	11
I/O (CS1, A2)	P79	P83	P115	P1	P127	P165	14
I/O (A3)	P80	P84	P116	N1	P128	P166	17
GND	-	-	P118	L3	P131	P171	-
I/O	-	-	P119	L2	P132	P172	20
I/O	-	-	P120	L1	P133	P173	23
I/O (A4)	P81	P85	P121	K3	P134	P174	26
I/O (A5)	P82	P86	P122	K2	P135	P175	29
I/O	-	P87	P123	K1	P137	P178	32
I/O	-	P88	P124	J1	P138	P179	35
I/O (A6)	P83	P89	P125	J2	P139	P180	38
I/O (A7)	P84	P90	P126	J3	P140	P181	41
GND	P1	P91	P127	H2	P141	P182	-

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Additional No Connect (N.C.) Connections on TQ144, PG156, PQ160 & PQ208 Packages

TQ144	PG156	PQ160	PQ208
P117	A4	P8	P1
	A12	P9	P3
	D1	P30	P10-P13
	D2	P31	P19-P20
	D16	P49	P31-P32
	E15	P50	P38-P41
	M1	P71	P51-P54
	M2	P72	P63-P66
	M15	P89	P72-P73
	N16	P90	P84-P85
	R5	P111	P91-P94
	R12	P112	P102
	T12	P129	P104-P105
		P130	P107
		P136	P115-P118
		P152	P124-P125
		P153	P136-P137
			P143-P146
			P155-P158
			P167-P170
			P176-P177
			P188-P189
			P195-P198
			P206-P208

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Pin Locations for XC4006E Devices

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
VCC	P2	P128	H3	P142	P183	-
I/O (A8)	P3	P129	H1	P143	P184	50
I/O (A9)	P4	P130	G1	P144	P185	53
I/O	-	P131	G2	P145	P186	56
I/O	-	P132	G3	P146	P187	59
I/O (A10)	P5	P133	F1	P147	P190	62
I/O (A11)	P6	P134	F2	P148	P191	65
I/O	-	P135	E1	P149	P192	68
I/O	-	P136	E2	P150	P193	71
GND	-	P137	F3	P151	P194	-
I/O	-	-	D1	P152	P197	74
I/O	-	-	D2	P153	P198	77
I/O (A12)	P7	P138	E3	P154	P199	80
I/O (A13)	P8	P139	C1	P155	P200	83
I/O	-	P140	C2	P156	P201	86
I/O	-	P141	D3	P157	P202	89
I/O (A14)	P9	P142	B1	P158	P203	92
I/O, SGCK1 (A15)	P10	P143	B2	P159	P204	95
VCC	P11	P144	C3	P160	P205	-
GND	P12	P1	C4	P1	P2	-
I/O, PGCK1 (A16)	P13	P2	B3	P2	P4	98
I/O (A17)	P14	P3	A1	P3	P5	101
I/O	-	P4	A2	P4	P6	104
I/O	-	P5	C5	P5	P7	107
I/O, TDI	P15	P6	B4	P6	P8	110
I/O, TCK	P16	P7	A3	P7	P9	113
I/O	-	-	A4	P8	P10	116
I/O	-	-	-	P9	P11	119
GND	-	P8	C6	P10	P14	-
I/O	-	P9	B5	P11	P15	122
I/O	-	P10	B6	P12	P16	125
I/O, TMS	P17	P11	A5	P13	P17	128
I/O	P18	P12	C7	P14	P18	131
I/O	-	P13	B7	P15	P21	134
I/O	-	P14	A6	P16	P22	137
I/O	P19	P15	A7	P17	P23	140
I/O	P20	P16	A8	P18	P24	143
GND	P21	P17	C8	P19	P25	-
VCC	P22	P18	B8	P20	P26	-
I/O	P23	P19	C9	P21	P27	146
I/O	P24	P20	B9	P22	P28	149
I/O	-	P21	A9	P23	P29	152
I/O	-	P22	B10	P24	P30	155
I/O	P25	P23	C10	P25	P33	158
I/O	P26	P24	A10	P26	P34	161
I/O	-	P25	A11	P27	P35	164
I/O	-	P26	B11	P28	P36	167
GND	-	P27	C11	P29	P37	-
I/O	-	-	A12	P30	P40	170
I/O	-	-	-	P31	P41	173
I/O	P27	P28	B12	P32	P42	176
I/O	-	P29	A13	P33	P43	179
I/O	-	P30	A14	P34	P44	182
I/O	-	P31	C12	P35	P45	185
I/O	P28	P32	B13	P36	P46	188
I/O, SCGK2	P29	P33	B14	P37	P47	191
O (M1)	P30	P34	A15	P38	P48	194
GND	P31	P35	C13	P39	P49	-
I (M0)	P32	P36	A16	P40	P50	197
VCC	P33	P37	C14	P41	P55	-
I (M2)	P34	P38	B15	P42	P56	198
I/O, PGCK2	P35	P39	B16	P43	P57	199
I/O (HDC)	P36	P40	D14	P44	P58	202
I/O	-	P41	C15	P45	P59	205
I/O	-	P42	D15	P46	P60	208
I/O	-	P43	E14	P47	P61	211
I/O ($\overline{\text{LDC}}$)	P37	P44	C16	P48	P62	214
I/O	-	-	E15	P49	P63	217
I/O	-	-	D16	P50	P64	220
GND	-	P45	F14	P51	P67	-
I/O	-	P46	F15	P52	P68	223
I/O	-	P47	E16	P53	P69	226
I/O	P38	P48	F16	P54	P70	229
I/O	P39	P49	G14	P55	P71	232
I/O	-	P50	G15	P56	P74	235
I/O	-	P51	G16	P57	P75	238
I/O	P40	P52	H16	P58	P76	241
I/O ($\overline{\text{INIT}}$)	P41	P53	H15	P59	P77	244
VCC	P42	P54	H14	P60	P78	-
GND	P43	P55	J14	P61	P79	-
I/O	P44	P56	J15	P62	P80	247
I/O	P45	P57	J16	P63	P81	250
I/O	-	P58	K16	P64	P82	253
I/O	-	P59	K15	P65	P83	256
I/O	P46	P60	K14	P66	P86	259
I/O	P47	P61	L16	P67	P87	262
I/O	-	P62	M16	P68	P88	265
I/O	-	P63	L15	P69	P89	268
GND	-	P64	L14	P70	P90	-
I/O	-	-	N16	P71	P93	271
I/O	-	-	M15	P72	P94	274
I/O	P48	P65	P16	P73	P95	277
I/O	P49	P66	M14	P74	P96	280
I/O	-	P67	N15	P75	P97	283
I/O	-	P68	P15	P76	P98	286
I/O	P50	P69	N14	P77	P99	289
I/O, SGCK3	P51	P70	R16	P78	P100	292
GND	P52	P71	P14	P79	P101	-
DONE	P53	P72	R15	P80	P103	-
VCC	P54	P73	P13	P81	P106	-
$\overline{\text{PROGRAM}}$	P55	P74	R14	P82	P108	-

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
I/O (D7)	P56	P75	T16	P83	P109	295
I/O, PGCK3	P57	P76	T15	P84	P110	298
I/O	-	P77	R13	P85	P111	301
I/O	-	P78	P12	P86	P112	304
I/O (D6)	P58	P79	T14	P87	P113	307
I/O	-	P80	T13	P88	P114	310
I/O	-	-	R12	P89	P115	313
I/O	-	-	T12	P90	P116	316
GND	-	P81	P11	P91	P119	-
I/O	-	P82	R11	P92	P120	319
I/O	-	P83	T11	P93	P121	322
I/O (D5)	P59	P84	T10	P94	P122	325
I/O ($\overline{CS0}$)	P60	P85	P10	P95	P123	328
I/O	-	P86	R10	P96	P126	331
I/O	-	P87	T9	P97	P127	334
I/O (D4)	P61	P88	R9	P98	P128	337
I/O	P62	P89	P9	P99	P129	340
VCC	P63	P90	R8	P100	P130	-
GND	P64	P91	P8	P101	P131	-
I/O (D3)	P65	P92	T8	P102	P132	343
I/O ($\overline{RS}$)	P66	P93	T7	P103	P133	346
I/O	-	P94	T6	P104	P134	349
I/O	-	P95	R7	P105	P135	352
I/O (D2)	P67	P96	P7	P106	P138	355
I/O	P68	P97	T5	P107	P139	358
I/O	-	P98	R6	P108	P140	361
I/O	-	P99	T4	P109	P141	364
GND	-	P100	P6	P110	P142	-
I/O	-	-	R5	P111	P145	367
I/O	-	-	-	P112	P146	370
I/O (D1)	P69	P101	T3	P113	P147	373
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P70	P102	P5	P114	P148	376
I/O	-	P103	R4	P115	P149	379
I/O	-	P104	R3	P116	P150	382
I/O (D0, DIN)	P71	P105	P4	P117	P151	385
I/O, SGCK4 (DOUT)	P72	P106	T2	P118	P152	388
CCLK	P73	P107	R2	P119	P153	-
VCC	P74	P108	P3	P120	P154	-
O, TDO	P75	P109	T1	P121	P159	0
GND	P76	P110	N3	P122	P160	-
I/O (A0, $\overline{WS}$)	P77	P111	R1	P123	P161	2
I/O, PGCK4 (A1)	P78	P112	P2	P124	P162	5
I/O	-	P113	N2	P125	P163	8
I/O	-	P114	M3	P126	P164	11
I/O (CS1, A2)	P79	P115	P1	P127	P165	14
I/O (A3)	P80	P116	N1	P128	P166	17
I/O	-	P117	M2	P129	P167	20
I/O	-	-	M1	P130	P168	23
GND	-	P118	L3	P131	P171	-
I/O	-	P119	L2	P132	P172	26
I/O	-	P120	L1	P133	P173	29
I/O (A4)	P81	P121	K3	P134	P174	32
I/O (A5)	P82	P122	K2	P135	P175	35
I/O	-	P123	K1	P137	P178	38
I/O	-	P124	J1	P138	P179	41
I/O (A6)	P83	P125	J2	P139	P180	44
I/O (A7)	P84	P126	J3	P140	P181	47
GND	P1	P127	H2	P141	P182	-

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Additional No Connect (N.C.) Connections on PQ160 & PQ208 Packages

PQ160	PQ208
P136	P1
	P3
	P12-P13
	P19-20
	P31-P32
	P38-P39
	P51-P54
	P65-P66
	P72-P73
	P84-P85
	P91-P92
	P102
	P104-P105
	P107
	P117-P118
	P124-P125
	P136-P137
	P143-P144
	P155-P158
	P169-P170
	P176-P177
	P188-P189
	P195-P196
	P206-P208

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Pin Locations for XC4008E Devices

XC4008E Pad Name	PC 84	PQ 160	PG 191	PQ 208	Bndry Scan
VCC	P2	P142	J4	P183	-
I/O (A8)	P3	P143	J3	P184	56
I/O (A9)	P4	P144	J2	P185	59
I/O	-	P145	J1	P186	62
I/O	-	P146	H1	P187	65
I/O	-	-	H2	P188	68
I/O	-	-	H3	P189	71
I/O (A10)	P5	P147	G1	P190	74
I/O (A11)	P6	P148	G2	P191	77
I/O	-	P149	F1	P192	80
I/O	-	P150	E1	P193	83
GND	-	P151	G3	P194	-
I/O	-	P152	C1	P197	86
I/O	-	P153	E2	P198	89
I/O (A12)	P7	P154	F3	P199	92
I/O (A13)	P8	P155	D2	P200	95
I/O	-	P156	B1	P201	98
I/O	-	P157	E3	P202	101
I/O (A14)	P9	P158	C2	P203	104
I/O, SGCK1 (A15)	P10	P159	B2	P204	107
VCC	P11	P160	D3	P205	-
GND	P12	P1	D4	P2	-
I/O, PGCK1 (A16)	P13	P2	C3	P4	110
I/O (A17)	P14	P3	C4	P5	113
I/O	-	P4	B3	P6	116
I/O	-	P5	C5	P7	119
I/O, TDI	P15	P6	A2	P8	122
I/O, TCK	P16	P7	B4	P9	125
I/O	-	P8	C6	P10	128
I/O	-	P9	A3	P11	131
GND	-	P10	C7	P14	-
I/O	-	P11	A4	P15	134
I/O	-	P12	A5	P16	137
I/O, TMS	P17	P13	B7	P17	140
I/O	P18	P14	A6	P18	143
I/O	-	-	C8	P19	146
I/O	-	-	A7	P20	149
I/O	-	P15	B8	P21	152
I/O	-	P16	A8	P22	155
I/O	P19	P17	B9	P23	158
I/O	P20	P18	C9	P24	161
GND	P21	P19	D9	P25	-
VCC	P22	P20	D10	P26	-
I/O	P23	P21	C10	P27	164
I/O	P24	P22	B10	P28	167
I/O	-	P23	A9	P29	170
I/O	-	P24	A10	P30	173
I/O	-	-	A11	P31	176
I/O	-	-	C11	P32	179
I/O	P25	P25	B11	P33	182
I/O	P26	P26	A12	P34	185
I/O	-	P27	B12	P35	188
I/O	-	P28	A13	P36	191
GND	-	P29	C12	P37	-
I/O	-	P30	A15	P40	194
I/O	-	P31	C13	P41	197
I/O	P27	P32	B14	P42	200
I/O	-	P33	A16	P43	203
I/O	-	P34	B15	P44	206
I/O	-	P35	C14	P45	209
I/O	P28	P36	A17	P46	212
I/O, SCGK2	P29	P37	B16	P47	215
O (M1)	P30	P38	C15	P48	218
GND	P31	P39	D15	P49	-
I (M0)	P32	P40	A18	P50	221
VCC	P33	P41	D16	P55	-
I (M2)	P34	P42	C16	P56	222
I/O, PGCK2	P35	P43	B17	P57	223
I/O (HDC)	P36	P44	E16	P58	226
I/O	-	P45	C17	P59	229
I/O	-	P46	D17	P60	232
I/O	-	P47	B18	P61	235
I/O ($\overline{\text{LDC}}$)	P37	P48	E17	P62	238
I/O	-	P49	F16	P63	241
I/O	-	P50	C18	P64	244
GND	-	P51	G16	P67	-
I/O	-	P52	E18	P68	247
I/O	-	P53	F18	P69	250
I/O	P38	P54	G17	P70	253
I/O	P39	P55	G18	P71	256
I/O	-	-	H16	P72	259
I/O	-	-	H17	P73	262
I/O	-	P56	H18	P74	265
I/O	-	P57	J18	P75	268
I/O	P40	P58	J17	P76	271
I/O ($\overline{\text{INIT}}$)	P41	P59	J16	P77	274
VCC	P42	P60	J15	P78	-
GND	P43	P61	K15	P79	-
I/O	P44	P62	K16	P80	277
I/O	P45	P63	K17	P81	280
I/O	-	P64	K18	P82	283
I/O	-	P65	L18	P83	286
I/O	-	-	L17	P84	289
I/O	-	-	L16	P85	292
I/O	P46	P66	M18	P86	295
I/O	P47	P67	M17	P87	298
I/O	-	P68	N18	P88	301
I/O	-	P69	P18	P89	304
GND	-	P70	M16	P90	-
I/O	-	P71	T18	P93	307
I/O	-	P72	P17	P94	310
I/O	P48	P73	N16	P95	313

XC4008E Pad Name	PC 84	PQ 160	PG 191	PQ 208	Bndry Scan
I/O	P49	P74	T17	P96	316
I/O	-	P75	R17	P97	319
I/O	-	P76	P16	P98	322
I/O	P50	P77	U18	P99	325
I/O, SGCK3	P51	P78	T16	P100	328
GND	P52	P79	R16	P101	-
DONE	P53	P80	U17	P103	-
VCC	P54	P81	R15	P106	-
$\overline{\text{PROGRAM}}$	P55	P82	V18	P108	-
I/O (D7)	P56	P83	T15	P109	331
I/O, PGCK3	P57	P84	U16	P110	334
I/O	-	P85	T14	P111	337
I/O	-	P86	U15	P112	340
I/O (D6)	P58	P87	V17	P113	343
I/O	-	P88	V16	P114	346
I/O	-	P89	T13	P115	349
I/O	-	P90	U14	P116	352
GND	-	P91	T12	P119	-
I/O	-	P92	U13	P120	355
I/O	-	P93	V13	P121	358
I/O (D5)	P59	P94	U12	P122	361
I/O ($\overline{\text{CS0}}$)	P60	P95	V12	P123	364
I/O	-	-	T11	P124	367
I/O	-	-	U11	P125	370
I/O	-	P96	V11	P126	373
I/O	-	P97	V10	P127	376
I/O (D4)	P61	P98	U10	P128	379
I/O	P62	P99	T10	P129	382
VCC	P63	P100	R10	P130	-
GND	P64	P101	R9	P131	-
I/O (D3)	P65	P102	T9	P132	385
I/O ($\overline{\text{RS}}$)	P66	P103	U9	P133	388
I/O	-	P104	V9	P134	391
I/O	-	P105	V8	P135	394
I/O	-	-	U8	P136	397
I/O	-	-	T8	P137	400
I/O (D2)	P67	P106	V7	P138	403
I/O	P68	P107	U7	P139	406
I/O	-	P108	V6	P140	409
I/O	-	P109	U6	P141	412
GND	-	P110	T7	P142	-
I/O	-	P111	U5	P145	415
I/O	-	P112	T6	P146	418
I/O (D1)	P69	P113	V3	P147	421
I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	P70	P114	V2	P148	424
I/O	-	P115	U4	P149	427
I/O	-	P116	T5	P150	430
I/O (D0, DIN)	P71	P117	U3	P151	433
I/O, SGCK4 (DOUT)	P72	P118	T4	P152	436
CCLK	P73	P119	V1	P153	-
VCC	P74	P120	R4	P154	-

XC4008E Pad Name	PC 84	PQ 160	PG 191	PQ 208	Bndry Scan
O, TDO	P75	P121	U2	P159	0
GND	P76	P122	R3	P160	-
I/O (A0, $\overline{\text{WS}}$)	P77	P123	T3	P161	2
I/O, PGCK4 (A1)	P78	P124	U1	P162	5
I/O	-	P125	P3	P163	8
I/O	-	P126	R2	P164	11
I/O (CS1, A2)	P79	P127	T2	P165	14
I/O (A3)	P80	P128	N3	P166	17
I/O	-	P129	P2	P167	20
I/O	-	P130	T1	P168	23
GND	-	P131	M3	P171	-
I/O	-	P132	P1	P172	26
I/O	-	P133	N1	P173	29
I/O (A4)	P81	P134	M2	P174	32
I/O (A5)	P82	P135	M1	P175	35
I/O	-	-	L3	P176	38
I/O	-	P136	L2	P177	41
I/O	-	P137	L1	P178	44
I/O	-	P138	K1	P179	47
I/O (A6)	P83	P139	K2	P180	50
I/O (A7)	P84	P140	K3	P181	53
GND	P1	P141	K4	P182	-

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Additional No Connect (N.C.) Connections on PG191 & PQ208 Packages

PG191	PQ208	PQ208
A14	P1	P107
B5	P3	P117
B6	P12	P118
B13	P13	P143
D1	P38	P144
D18	P39	P155
F2	P51	P156
F17	P52	P157
N2	P53	P158
N17	P54	P169
R1	P65	P170
R18	P66	P195
V4	P91	P196
V5	P92	P206
V14	P102	P207
V15	P104	P208
	P105	

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Pin Locations for XC4010E/L Devices

XC4010E/L Pad Name	PC 84	PQ 160	TQ 176	PG 191	PQ/ HQ 208	BG 225	Bndry Scan
VCC	P2	P142	P155	J4	P183	D8	-
I/O (A8)	P3	P143	P156	J3	P184	E8	62
I/O (A9)	P4	P144	P157	J2	P185	B7	65
I/O	-	P145	P158	J1	P186	A7	68
I/O	-	P146	P159	H1	P187	C7	71
I/O	-	-	P160	H2	P188	D7	74
I/O	-	-	P161	H3	P189	E7	77
I/O (A10)	P5	P147	P162	G1	P190	A6	80
I/O (A11)	P6	P148	P163	G2	P191	B6	83
I/O	-	P149	P164	F1	P192	A5	86
I/O	-	P150	P165	E1	P193	B5	89
GND	-	P151	P166	G3	P194	GND*	-
I/O	-	-	-	F2	P195	D6	92
I/O	-	-	P167	D1	P196	C5	95
I/O	-	P152	P168	C1	P197	A4	98
I/O	-	P153	P169	E2	P198	E6	101
I/O (A12)	P7	P154	P170	F3	P199	B4	104
I/O (A13)	P8	P155	P171	D2	P200	D5	107
I/O	-	P156	P172	B1	P201	B3	110
I/O	-	P157	P173	E3	P202	F6	113
I/O (A14)	P9	P158	P174	C2	P203	A2	116
I/O, SGCK1 (A15)	P10	P159	P175	B2	P204	C3	119
VCC	P11	P160	P176	D3	P205	B2	-
GND	P12	P1	P1	D4	P2	A1	-
I/O, PGCK1 (A16)	P13	P2	P2	C3	P4	D4	122
I/O (A17)	P14	P3	P3	C4	P5	B1	125
I/O	-	P4	P4	B3	P6	C2	128
I/O	-	P5	P5	C5	P7	E5	131
I/O, TDI	P15	P6	P6	A2	P8	D3	134
I/O, TCK	P16	P7	P7	B4	P9	C1	137
I/O	-	P8	P8	C6	P10	D2	140
I/O	-	P9	P9	A3	P11	G6	143
I/O	-	-	-	B5	P12	E4	146
I/O	-	-	-	B6	P13	D1	149
GND	-	P10	P10	C7	P14	GND*	-
I/O	-	P11	P11	A4	P15	F5	152
I/O	-	P12	P12	A5	P16	E1	155
I/O, TMS	P17	P13	P13	B7	P17	F4	158
I/O	P18	P14	P14	A6	P18	F3	161
I/O	-	-	P15	C8	P19	G4	164
I/O	-	-	P16	A7	P20	G3	167
I/O	-	P15	P17	B8	P21	G2	170
I/O	-	P16	P18	A8	P22	G1	173
I/O	P19	P17	P19	B9	P23	G5	176
I/O	P20	P18	P20	C9	P24	H3	179
GND	P21	P19	P21	D9	P25	H2	-
VCC	P22	P20	P22	D10	P26	H1	-
I/O	P23	P21	P23	C10	P27	H4	182
I/O	P24	P22	P24	B10	P28	H5	185
I/O	-	P23	P25	A9	P29	J2	188
I/O	-	P24	P26	A10	P30	J1	191
I/O	-	-	P27	A11	P31	J3	194
I/O	-	-	P28	C11	P32	J4	197
I/O	P25	P25	P29	B11	P33	K2	200
I/O	P26	P26	P30	A12	P34	K3	203
I/O	-	P27	P31	B12	P35	J6	206
I/O	-	P28	P32	A13	P36	L1	209
GND	-	P29	P33	C12	P37	GND*	-
I/O	-	-	-	B13	P38	L3	212
I/O	-	-	-	A14	P39	M1	215
I/O	-	P30	P34	A15	P40	K5	218
I/O	-	P31	P35	C13	P41	M2	221
I/O	P27	P32	P36	B14	P42	L4	224
I/O	-	P33	P37	A16	P43	N1	227
I/O	-	P34	P38	B15	P44	M3	230
I/O	-	P35	P39	C14	P45	N2	233
I/O	P28	P36	P40	A17	P46	K6	236
I/O, SCGK2	P29	P37	P41	B16	P47	P1	239
O (M1)	P30	P38	P42	C15	P48	N3	242
GND	P31	P39	P43	D15	P49	GND*	-
I (M0)	P32	P40	P44	A18	P50	P2	245
VCC	P33	P41	P45	D16	P55	R1	-
I (M2)	P34	P42	P46	C16	P56	M4	246
I/O, PGCK2	P35	P43	P47	B17	P57	R2	247
I/O (HDC)	P36	P44	P48	E16	P58	P3	250
I/O	-	P45	P49	C17	P59	L5	253
I/O	-	P46	P50	D17	P60	N4	256
I/O	-	P47	P51	B18	P61	R3	259
I/O ($\overline{\text{LDC}}$)	P37	P48	P52	E17	P62	P4	262
I/O	-	P49	P53	F16	P63	K7	265
I/O	-	P50	P54	C18	P64	M5	268
I/O	-	-	-	D18	P65	R4	271
I/O	-	-	-	F17	P66	N5	274
GND	-	P51	P55	G16	P67	GND*	-
I/O	-	P52	P56	E18	P68	R5	277
I/O	-	P53	P57	F18	P69	M6	280
I/O	P38	P54	P58	G17	P70	N6	283
I/O	P39	P55	P59	G18	P71	P6	286
I/O	-	-	P60	H16	P72	R6	289

XC4010E/L Pad Name	PC 84	PQ 160	TQ 176	PG 191	PQ/ HQ 208	BG 225	Bndry Scan
I/O	-	-	P61	H17	P73	M7	292
I/O	-	P56	P62	H18	P74	R7	295
I/O	-	P57	P63	J18	P75	L7	298
I/O	P40	P58	P64	J17	P76	N8	301
I/O ($\overline{INIT}$)	P41	P59	P65	J16	P77	P8	304
VCC	P42	P60	P66	J15	P78	R8	-
GND	P43	P61	P67	K15	P79	M8	-
I/O	P44	P62	P68	K16	P80	L8	307
I/O	P45	P63	P69	K17	P81	P9	310
I/O	-	P64	P70	K18	P82	R9	313
I/O	-	P65	P71	L18	P83	N9	316
I/O	-	-	P72	L17	P84	M9	319
I/O	-	-	P73	L16	P85	L9	322
I/O	P46	P66	P74	M18	P86	N10	325
I/O	P47	P67	P75	M17	P87	K9	328
I/O	-	P68	P76	N18	P88	R11	331
I/O	-	P69	P77	P18	P89	P11	334
GND	-	P70	P78	M16	P90	GND*	-
I/O	-	-	-	N17	P91	R12	337
I/O	-	-	-	R18	P92	L10	340
I/O	-	P71	P79	T18	P93	P12	343
I/O	-	P72	P80	P17	P94	M11	346
I/O	P48	P73	P81	N16	P95	R13	349
I/O	P49	P74	P82	T17	P96	N12	352
I/O	-	P75	P83	R17	P97	P13	355
I/O	-	P76	P84	P16	P98	K10	358
I/O	P50	P77	P85	U18	P99	R14	361
I/O, SGCK3	P51	P78	P86	T16	P100	N13	364
GND	P52	P79	P87	R16	P101	GND*	-
DONE	P53	P80	P88	U17	P103	P14	-
VCC	P54	P81	P89	R15	P106	R15	-
$\overline{PROGRAM}$	P55	P82	P90	V18	P108	M12	-
I/O (D7)	P56	P83	P91	T15	P109	P15	367
I/O, PGCK3	P57	P84	P92	U16	P110	N14	370
I/O	-	P85	P93	T14	P111	L11	373
I/O	-	P86	P94	U15	P112	M13	376
I/O (D6)	P58	P87	P95	V17	P113	J10	379
I/O	-	P88	P96	V16	P114	L12	382
I/O	-	P89	P97	T13	P115	M15	385
I/O	-	P90	P98	U14	P116	L13	388
I/O	-	-	-	V15	P117	L14	391
I/O	-	-	-	V14	P118	K11	394
GND	-	P91	P99	T12	P119	GND*	-
I/O	-	P92	P100	U13	P120	K13	397
I/O	-	P93	P101	V13	P121	K14	400
I/O (D5)	P59	P94	P102	U12	P122	K15	403

XC4010E/L Pad Name	PC 84	PQ 160	TQ 176	PG 191	PQ/ HQ 208	BG 225	Bndry Scan
I/O ($\overline{CS0}$)	P60	P95	P103	V12	P123	J12	406
I/O	-	-	P104	T11	P124	J13	409
I/O	-	-	P105	U11	P125	J14	412
I/O	-	P96	P106	V11	P126	J15	415
I/O	-	P97	P107	V10	P127	J11	418
I/O (D4)	P61	P98	P108	U10	P128	H13	421
I/O	P62	P99	P109	T10	P129	H14	424
VCC	P63	P100	P110	R10	P130	H15	-
GND	P64	P101	P111	R9	P131	GND*	-
I/O (D3)	P65	P102	P112	T9	P132	H12	427
I/O ($\overline{RS}$)	P66	P103	P113	U9	P133	H11	430
I/O	-	P104	P114	V9	P134	G14	433
I/O	-	P105	P115	V8	P135	G15	436
I/O	-	-	P116	U8	P136	G13	439
I/O	-	-	P117	T8	P137	G12	442
I/O (D2)	P67	P106	P118	V7	P138	G11	445
I/O	P68	P107	P119	U7	P139	F15	448
I/O	-	P108	P120	V6	P140	F14	451
I/O	-	P109	P121	U6	P141	F13	454
GND	-	P110	P122	T7	P142	GND*	-
I/O	-	-	-	V5	P143	E13	457
I/O	-	-	-	V4	P144	D15	460
I/O	-	P111	P123	U5	P145	F11	463
I/O	-	P112	P124	T6	P146	D14	466
I/O (D1)	P69	P113	P125	V3	P147	E12	469
I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	P70	P114	P126	V2	P148	C15	472
I/O	-	P115	P127	U4	P149	D13	475
I/O	-	P116	P128	T5	P150	C14	478
I/O (D0, DIN)	P71	P117	P129	U3	P151	F10	481
I/O, SGCK4 (DOUT)	P72	P118	P130	T4	P152	B15	484
CCLK	P73	P119	P131	V1	P153	C13	-
VCC	P74	P120	P132	R4	P154	B14	-
O, TDO	P75	P121	P133	U2	P159	A15	0
GND	P76	P122	P134	R3	P160	D12	-
I/O (A0, $\overline{WS}$)	P77	P123	P135	T3	P161	A14	2
I/O, PGCK4 (A1)	P78	P124	P136	U1	P162	B13	5
I/O	-	P125	P137	P3	P163	E11	8
I/O	-	P126	P138	R2	P164	C12	11
I/O (CS1, A2)	P79	P127	P139	T2	P165	A13	14
I/O (A3)	P80	P128	P140	N3	P166	B12	17

XC4010E/L Pad Name	PC 84	PQ 160	TQ 176	PG 191	PQ/ HQ 208	BG 225	Bndry Scan
I/O	-	P129	P141	P2	P167	A12	20
I/O	-	P130	P142	T1	P168	C11	23
I/O	-	-	-	R1	P169	B11	26
I/O	-	-	-	N2	P170	E10	29
GND	-	P131	P143	M3	P171	GND*	-
I/O	-	P132	P144	P1	P172	A11	32
I/O	-	P133	P145	N1	P173	D10	35
I/O (A4)	P81	P134	P146	M2	P174	A10	38
I/O (A5)	P82	P135	P147	M1	P175	D9	41
I/O	-	-	P148	L3	P176	C9	44
I/O	-	P136	P149	L2	P177	B9	47
I/O	-	P137	P150	L1	P178	A9	50
I/O	-	P138	P151	K1	P179	E9	53
I/O (A6)	P83	P139	P152	K2	P180	C8	56
I/O (A7)	P84	P140	P153	K3	P181	B8	59
GND	P1	P141	P154	K4	P182	A8	-

4/2/96

* Pads labelled GND* are internally bonded to a Ground plane within the BG225 package. They have no direct connection to any package pin.

Additional Ground (GND) Connections on BG225 Package

GND
F8
G7
G8
G9
H6
H7
H8
H9
H10
J7
J8
J9
K8

2/28/96

Note: The package pins in this table are bonded to an internal Ground plane within the BG225 package. They should all be externally connected to Ground.

Additional No Connect (N.C.) Connections on PQ/HQ208 & BG225 Packages

PQ/HQ208	BG225
P1	A3
P3	B10
P51	C4
P52	C6
P53	C10
P54	D11
P102	E2
P104	E3
P105	E14
P107	E15
P155	F1
P156	F2
P157	F7
P158	F9
P206	F12
P207	G10
P208	J5
	K1
	K4
	K12
	L2
	L6
	L15
	M10
	M14
	N7
	N11
	N15
	P5
	P7
	P10
	R10

3/12/96

Pin Locations for XC4013E/L Devices

XC4013E/L Pad Name	PQ 160	PQ/ HQ 208	PG 223	BG 225	PQ/ HQ 240	Bndry Scan
VCC	P142	P183	J4	D8	P212	-
I/O (A8)	P143	P184	J3	E8	P213	74
I/O (A9)	P144	P185	J2	B7	P214	77
I/O	P145	P186	J1	A7	P215	80
I/O	P146	P187	H1	C7	P216	83
I/O	-	P188	H2	D7	P217	86
I/O	-	P189	H3	E7	P218	89
I/O (A10)	P147	P190	G1	A6	P220	92
I/O (A11)	P148	P191	G2	B6	P221	95
VCC	-	-	-	VCC*	P222	-
I/O	-	-	H4	C6	P223	98
I/O	-	-	G4	F7	P224	101
I/O	P149	P192	F1	A5	P225	104
I/O	P150	P193	E1	B5	P226	107
GND	P151	P194	G3	GND*	P227	-
I/O	-	P195	F2	D6	P228	110
I/O	-	P196	D1	C5	P229	113
I/O	P152	P197	C1	A4	P230	116
I/O	P153	P198	E2	E6	P231	119
I/O (A12)	P154	P199	F3	B4	P232	122
I/O (A13)	P155	P200	D2	D5	P233	125
I/O	-	-	F4	A3	P234	128
I/O	-	-	E4	C4	P235	131
I/O	P156	P201	B1	B3	P236	134
I/O	P157	P202	E3	F6	P237	137
I/O (A14)	P158	P203	C2	A2	P238	140
I/O, SGCK1 (A15)	P159	P204	B2	C3	P239	143
VCC	P160	P205	D3	B2	P240	-
GND	P1	P2	D4	A1	P1	-
I/O, PGCK1 (A16)	P2	P4	C3	D4	P2	146
I/O (A17)	P3	P5	C4	B1	P3	149
I/O	P4	P6	B3	C2	P4	152
I/O	P5	P7	C5	E5	P5	155
I/O, TDI	P6	P8	A2	D3	P6	158
I/O, TCK	P7	P9	B4	C1	P7	161
I/O	P8	P10	C6	D2	P8	164
I/O	P9	P11	A3	G6	P9	167
I/O	-	P12	B5	E4	P10	170
I/O	-	P13	B6	D1	P11	173
I/O	-	-	D5	E3	P12	176
I/O	-	-	D6	E2	P13	179
GND	P10	P14	C7	GND*	P14	-
I/O	P11	P15	A4	F5	P15	182
I/O	P12	P16	A5	E1	P16	185
I/O, TMS	P13	P17	B7	F4	P17	188
I/O	P14	P18	A6	F3	P18	191
VCC	-	-	-	VCC*	P19	-
I/O	-	-	D7	F2	P20	194
I/O	-	-	D8	F1	P21	197
I/O	-	P19	C8	G4	P23	200
I/O	-	P20	A7	G3	P24	203
I/O	P15	P21	B8	G2	P25	206
I/O	P16	P22	A8	G1	P26	209
I/O	P17	P23	B9	G5	P27	212
I/O	P18	P24	C9	H3	P28	215
GND	P19	P25	D9	H2	P29	-
VCC	P20	P26	D10	H1	P30	-
I/O	P21	P27	C10	H4	P31	218
I/O	P22	P28	B10	H5	P32	221
I/O	P23	P29	A9	J2	P33	224
I/O	P24	P30	A10	J1	P34	227
I/O	-	P31	A11	J3	P35	230
I/O	-	P32	C11	J4	P36	233
I/O	-	-	D11	J5	P38	236
I/O	-	-	D12	K1	P39	239
VCC	-	-	-	VCC*	P40	-
I/O	P25	P33	B11	K2	P41	242
I/O	P26	P34	A12	K3	P42	245
I/O	P27	P35	B12	J6	P43	248
I/O	P28	P36	A13	L1	P44	251
GND	P29	P37	C12	GND*	P45	-
I/O	-	-	D13	L2	P46	254
I/O	-	-	D14	K4	P47	257
I/O	-	P38	B13	L3	P48	260
I/O	-	P39	A14	M1	P49	263
I/O	P30	P40	A15	K5	P50	266
I/O	P31	P41	C13	M2	P51	269
I/O	P32	P42	B14	L4	P52	272
I/O	P33	P43	A16	N1	P53	275
I/O	P34	P44	B15	M3	P54	278
I/O	P35	P45	C14	N2	P55	281
I/O	P36	P46	A17	K6	P56	284
I/O, SCGK2	P37	P47	B16	P1	P57	287
O (M1)	P38	P48	C15	N3	P58	290
GND	P39	P49	D15	GND*	P59	-
I (M0)	P40	P50	A18	P2	P60	293
VCC	P41	P55	D16	R1	P61	-
I (M2)	P42	P56	C16	M4	P62	294
I/O, PGCK2	P43	P57	B17	R2	P63	295
I/O (HDC)	P44	P58	E16	P3	P64	298
I/O	P45	P59	C17	L5	P65	301
I/O	P46	P60	D17	N4	P66	304
I/O	P47	P61	B18	R3	P67	307
I/O ($\overline{\text{LDC}}$)	P48	P62	E17	P4	P68	310
I/O	P49	P63	F16	K7	P69	313
I/O	P50	P64	C18	M5	P70	316
I/O	-	P65	D18	R4	P71	319

XC4013E/L Pad Name	PQ 160	PQ/ HQ 208	PG 223	BG 225	PQ/ HQ 240	Bndry Scan
I/O	-	P66	F17	N5	P72	322
I/O	-	-	E15	P5	P73	325
I/O	-	-	F15	L6	P74	328
GND	P51	P67	G16	GND*	P75	-
I/O	P52	P68	E18	R5	P76	331
I/O	P53	P69	F18	M6	P77	334
I/O	P54	P70	G17	N6	P78	337
I/O	P55	P71	G18	P6	P79	340
VCC	-	-	-	VCC*	P80	-
I/O	-	P72	H16	R6	P81	343
I/O	-	P73	H17	M7	P82	346
I/O	-	-	G15	N7	P84	349
I/O	-	-	H15	P7	P85	352
I/O	P56	P74	H18	R7	P86	355
I/O	P57	P75	J18	L7	P87	358
I/O	P58	P76	J17	N8	P88	361
I/O ($\overline{INIT}$)	P59	P77	J16	P8	P89	364
VCC	P60	P78	J15	R8	P90	-
GND	P61	P79	K15	M8	P91	-
I/O	P62	P80	K16	L8	P92	367
I/O	P63	P81	K17	P9	P93	370
I/O	P64	P82	K18	R9	P94	373
I/O	P65	P83	L18	N9	P95	376
I/O	-	P84	L17	M9	P96	379
I/O	-	P85	L16	L9	P97	382
I/O	-	-	L15	R10	P99	385
I/O	-	-	M15	P10	P100	388
VCC	-	-	-	VCC*	P101	-
I/O	P66	P86	M18	N10	P102	391
I/O	P67	P87	M17	K9	P103	394
I/O	P68	P88	N18	R11	P104	397
I/O	P69	P89	P18	P11	P105	400
GND	P70	P90	M16	GND*	P106	-
I/O	-	-	N15	M10	P107	403
I/O	-	-	P15	N11	P108	406
I/O	-	P91	N17	R12	P109	409
I/O	-	P92	R18	L10	P110	412
I/O	P71	P93	T18	P12	P111	415
I/O	P72	P94	P17	M11	P112	418
I/O	P73	P95	N16	R13	P113	421
I/O	P74	P96	T17	N12	P114	424
I/O	P75	P97	R17	P13	P115	427
I/O	P76	P98	P16	K10	P116	430
I/O	P77	P99	U18	R14	P117	433
I/O, SGCK3	P78	P100	T16	N13	P118	436
GND	P79	P101	R16	GND*	P119	-
DONE	P80	P103	U17	P14	P120	-
VCC	P81	P106	R15	R15	P121	-
$\overline{PROGRAM}$	P82	P108	V18	M12	P122	-
I/O (D7)	P83	P109	T15	P15	P123	439

XC4013E/L Pad Name	PQ 160	PQ/ HQ 208	PG 223	BG 225	PQ/ HQ 240	Bndry Scan
I/O, PGCK3	P84	P110	U16	N14	P124	442
I/O	P85	P111	T14	L11	P125	445
I/O	P86	P112	U15	M13	P126	448
I/O	-	-	R14	N15	P127	451
I/O	-	-	R13	M14	P128	454
I/O (D6)	P87	P113	V17	J10	P129	457
I/O	P88	P114	V16	L12	P130	460
I/O	P89	P115	T13	M15	P131	463
I/O	P90	P116	U14	L13	P132	466
I/O	-	P117	V15	L14	P133	469
I/O	-	P118	V14	K11	P134	472
GND	P91	P119	T12	GND*	P135	-
I/O	-	-	R12	L15	P136	475
I/O	-	-	R11	K12	P137	478
I/O	P92	P120	U13	K13	P138	481
I/O	P93	P121	V13	K14	P139	484
VCC	-	-	-	VCC*	P140	-
I/O (D5)	P94	P122	U12	K15	P141	487
I/O ($\overline{CS0}$)	P95	P123	V12	J12	P142	490
I/O	-	P124	T11	J13	P144	493
I/O	-	P125	U11	J14	P145	496
I/O	P96	P126	V11	J15	P146	499
I/O	P97	P127	V10	J11	P147	502
I/O (D4)	P98	P128	U10	H13	P148	505
I/O	P99	P129	T10	H14	P149	508
VCC	P100	P130	R10	H15	P150	-
GND	P101	P131	R9	GND*	P151	-
I/O (D3)	P102	P132	T9	H12	P152	511
I/O ($\overline{RS}$)	P103	P133	U9	H11	P153	514
I/O	P104	P134	V9	G14	P154	517
I/O	P105	P135	V8	G15	P155	520
I/O	-	P136	U8	G13	P156	523
I/O	-	P137	T8	G12	P157	526
I/O (D2)	P106	P138	V7	G11	P159	529
I/O	P107	P139	U7	F15	P160	532
VCC	-	-	-	VCC*	P161	-
I/O	P108	P140	V6	F14	P162	535
I/O	P109	P141	U6	F13	P163	538
I/O	-	-	R8	G10	P164	541
I/O	-	-	R7	E15	P165	544
GND	P110	P142	T7	GND*	P166	-
I/O	-	-	R6	E14	P167	547
I/O	-	-	R5	F12	P168	550
I/O	-	P143	V5	E13	P169	553
I/O	-	P144	V4	D15	P170	556
I/O	P111	P145	U5	F11	P171	559
I/O	P112	P146	T6	D14	P172	562
I/O (D1)	P113	P147	V3	E12	P173	565
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P114	P148	V2	C15	P174	568
I/O	P115	P149	U4	D13	P175	571

XC4013E/L Pad Name	PQ 160	PQ/ HQ 208	PG 223	BG 225	PQ/ HQ 240	Bndry Scan
I/O	P116	P150	T5	C14	P176	574
I/O (D0, DIN)	P117	P151	U3	F10	P177	577
I/O, SGCK4 (DOUT)	P118	P152	T4	B15	P178	580
CCLK	P119	P153	V1	C13	P179	-
VCC	P120	P154	R4	B14	P180	-
O, TDO	P121	P159	U2	A15	P181	0
GND	P122	P160	R3	D12	P182	-
I/O (A0, $\overline{WS}$)	P123	P161	T3	A14	P183	2
I/O, PGCK4 (A1)	P124	P162	U1	B13	P184	5
I/O	P125	P163	P3	E11	P185	8
I/O	P126	P164	R2	C12	P186	11
I/O (CS1, A2)	P127	P165	T2	A13	P187	14
I/O (A3)	P128	P166	N3	B12	P188	17
I/O	-	-	P4	F9	P189	20
I/O	-	-	N4	D11	P190	23
I/O	P129	P167	P2	A12	P191	26
I/O	P130	P168	T1	C11	P192	29
I/O	-	P169	R1	B11	P193	32
I/O	-	P170	N2	E10	P194	35
GND	P131	P171	M3	GND*	P196	-
I/O	P132	P172	P1	A11	P197	38
I/O	P133	P173	N1	D10	P198	41
I/O	-	-	M4	C10	P199	44
I/O	-	-	L4	B10	P200	47
VCC	-	-	-	VCC*	P201	-
I/O (A4)	P134	P174	M2	A10	P202	50
I/O (A5)	P135	P175	M1	D9	P203	53
I/O	-	P176	L3	C9	P205	56
I/O	P136	P177	L2	B9	P206	59
I/O	P137	P178	L1	A9	P207	62
I/O	P138	P179	K1	E9	P208	65
I/O (A6)	P139	P180	K2	C8	P209	68
I/O (A7)	P140	P181	K3	B8	P210	71
GND	P141	P182	K4	A8	P211	-

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Pads labelled GND* are internally bonded to a Ground plane within the BG225 package. They have no direct connection to any package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the BG225 package. They have no direct connection to any package pin.

Additional Ground (GND) Connections on BG225 Packages

BG225	BG225
K8	H9
J7	H10
J8	G7
J9	G8
H6	G9
H7	F8
H8	

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The BG225 package pins in this table are bonded to an internal Ground plane on the XC4013E/L die. They must all be externally connected to Ground.

Additional No Connect (N.C.) Connections on PQ/HQ208 & PQ/HQ240 Packages

PQ/HQ208	PQ/HQ240
P1	P22 ‡
P3	P37 ‡
P51	P83 ‡
P52	P98 ‡
P53	P143 ‡
P54	P158 ‡
P102	P195
P104	P204 ‡
P105	P219 ‡
P107	
P155	
P156	
P157	
P158	
P206	
P207	
P208	

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‡ Pins marked with this symbol are reserved for Ground connections on future revisions of the device. These pins do not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

Pin Locations for XC4020E Devices

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
VCC	P183	J4	P212	-
I/O (A8)	P184	J3	P213	86
I/O (A9)	P185	J2	P214	89
I/O	P186	J1	P215	92
I/O	P187	H1	P216	95
I/O	P188	H2	P217	98
I/O	P189	H3	P218	101
I/O (A10)	P190	G1	P220	104
I/O (A11)	P191	G2	P221	107
I/O	-	-	-	110
I/O	-	-	-	113
VCC	-	-	P222	-
I/O	-	H4	P223	116
I/O	-	G4	P224	119
I/O	P192	F1	P225	122
I/O	P193	E1	P226	125
GND	P194	G3	P227	-
I/O	P195	F2	P228	128
I/O	P196	D1	P229	131
I/O	P197	C1	P230	134
I/O	P198	E2	P231	137
I/O (A12)	P199	F3	P232	140
I/O (A13)	P200	D2	P233	143
I/O	-	-	-	146
I/O	-	-	-	149
I/O	-	F4	P234	152
I/O	-	E4	P235	155
I/O	P201	B1	P236	158
I/O	P202	E3	P237	161
I/O (A14)	P203	C2	P238	164
I/O, SGCK1 (A15)	P204	B2	P239	167
VCC	P205	D3	P240	-
GND	P2	D4	P1	-
I/O, PGCK1 (A16)	P4	C3	P2	170
I/O (A17)	P5	C4	P3	173
I/O	P6	B3	P4	176
I/O	P7	C5	P5	179
I/O, TDI	P8	A2	P6	182
I/O, TCK	P9	B4	P7	185
I/O	-	-	-	188
I/O	-	-	-	191
I/O	P10	C6	P8	194
I/O	P11	A3	P9	197
I/O	P12	B5	P10	200
I/O	P13	B6	P11	203
I/O	-	D5	P12	206
I/O	-	D6	P13	209
GND	P14	C7	P14	-
I/O	P15	A4	P15	212
I/O	P16	A5	P16	215
I/O, TMS	P17	B7	P17	218
I/O	P18	A6	P18	221
VCC	-	-	P19	-
I/O	-	D7	P20	224
I/O	-	D8	P21	227
I/O	-	-	-	230
I/O	-	-	-	233
I/O	P19	C8	P23	236
I/O	P20	A7	P24	239
I/O	P21	B8	P25	242
I/O	P22	A8	P26	245
I/O	P23	B9	P27	248
I/O	P24	C9	P28	251
GND	P25	D9	P29	-
VCC	P26	D10	P30	-
I/O	P27	C10	P31	254
I/O	P28	B10	P32	257
I/O	P29	A9	P33	260
I/O	P30	A10	P34	263
I/O	P31	A11	P35	266
I/O	P32	C11	P36	269
I/O	-	-	-	272
I/O	-	-	-	275
I/O	-	D11	P38	278
I/O	-	D12	P39	281
VCC	-	-	P40	-
I/O	P33	B11	P41	284
I/O	P34	A12	P42	287
I/O	P35	B12	P43	290
I/O	P36	A13	P44	293
GND	P37	C12	P45	-
I/O	-	D13	P46	296
I/O	-	D14	P47	299
I/O	P38	B13	P48	302
I/O	P39	A14	P49	305
I/O	P40	A15	P50	308
I/O	P41	C13	P51	311
I/O	-	-	-	314
I/O	-	-	-	317
I/O	P42	B14	P52	320
I/O	P43	A16	P53	323
I/O	P44	B15	P54	326
I/O	P45	C14	P55	329
I/O	P46	A17	P56	332
I/O, SCGK2	P47	B16	P57	335
O (M1)	P48	C15	P58	338
GND	P49	D15	P59	-
I (M0)	P50	A18	P60	341
VCC	P55	D16	P61	-
I (M2)	P56	C16	P62	342
I/O, PGCK2	P57	B17	P63	343
I/O (HDC)	P58	E16	P64	346

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
I/O	P59	C17	P65	349
I/O	P60	D17	P66	352
I/O	P61	B18	P67	355
I/O ($\overline{LDC}$)	P62	E17	P68	358
I/O	-	-	-	361
I/O	-	-	-	364
I/O	P63	F16	P69	367
I/O	P64	C18	P70	370
I/O	P65	D18	P71	373
I/O	P66	F17	P72	376
I/O	-	E15	P73	379
I/O	-	F15	P74	382
GND	P67	G16	P75	-
I/O	P68	E18	P76	385
I/O	P69	F18	P77	388
I/O	P70	G17	P78	391
I/O	P71	G18	P79	394
VCC	-	-	P80	-
I/O	P72	H16	P81	397
I/O	P73	H17	P82	400
I/O	-	-	-	403
I/O	-	-	-	406
I/O	-	G15	P84	409
I/O	-	H15	P85	412
I/O	P74	H18	P86	415
I/O	P75	J18	P87	418
I/O	P76	J17	P88	421
I/O ($\overline{INIT}$)	P77	J16	P89	424
VCC	P78	J15	P90	-
GND	P79	K15	P91	-
I/O	P80	K16	P92	427
I/O	P81	K17	P93	430
I/O	P82	K18	P94	433
I/O	P83	L18	P95	436
I/O	P84	L17	P96	439
I/O	P85	L16	P97	442
I/O	-	-	-	445
I/O	-	-	-	448
I/O	-	L15	P99	451
I/O	-	M15	P100	454
VCC	-	-	P101	-
I/O	P86	M18	P102	457
I/O	P87	M17	P103	460
I/O	P88	N18	P104	463
I/O	P89	P18	P105	466
GND	P90	M16	P106	-
I/O	-	N15	P107	469
I/O	-	P15	P108	472
I/O	P91	N17	P109	475
I/O	P92	R18	P110	478
I/O	P93	T18	P111	481
I/O	P94	P17	P112	484

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
I/O	-	-	-	487
I/O	-	-	-	490
I/O	P95	N16	P113	493
I/O	P96	T17	P114	496
I/O	P97	R17	P115	499
I/O	P98	P16	P116	502
I/O	P99	U18	P117	505
I/O, SGCK3	P100	T16	P118	508
GND	P101	R16	P119	-
DONE	P103	U17	P120	-
VCC	P106	R15	P121	-
$\overline{PROGRAM}$	P108	V18	P122	-
I/O (D7)	P109	T15	P123	511
I/O, PGCK3	P110	U16	P124	514
I/O	P111	T14	P125	517
I/O	P112	U15	P126	520
I/O	-	R14	P127	523
I/O	-	R13	P128	526
I/O	-	-	-	529
I/O	-	-	-	532
I/O (D6)	P113	V17	P129	535
I/O	P114	V16	P130	538
I/O	P115	T13	P131	541
I/O	P116	U14	P132	544
I/O	P117	V15	P133	547
I/O	P118	V14	P134	550
GND	P119	T12	P135	-
I/O	-	R12	P136	553
I/O	-	R11	P137	556
I/O	P120	U13	P138	559
I/O	P121	V13	P139	562
VCC	-	-	P140	-
I/O (D5)	P122	U12	P141	565
I/O ($\overline{CS0}$)	P123	V12	P142	568
I/O	-	-	-	571
I/O	-	-	-	574
I/O	P124	T11	P144	577
I/O	P125	U11	P145	580
I/O	P126	V11	P146	583
I/O	P127	V10	P147	586
I/O (D4)	P128	U10	P148	589
I/O	P129	T10	P149	592
VCC	P130	R10	P150	-
GND	P131	R9	P151	-
I/O (D3)	P132	T9	P152	595
I/O ($\overline{RS}$)	P133	U9	P153	598
I/O	P134	V9	P154	601
I/O	P135	V8	P155	604
I/O	P136	U8	P156	607
I/O	P137	T8	P157	610
I/O	-	-	-	613
I/O	-	-	-	616

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
I/O (D2)	P138	V7	P159	619
I/O	P139	U7	P160	622
VCC	-	-	P161	-
I/O	P140	V6	P162	625
I/O	P141	U6	P163	628
I/O	-	R8	P164	631
I/O	-	R7	P165	634
GND	P142	T7	P166	-
I/O	-	R6	P167	637
I/O	-	R5	P168	640
I/O	P143	V5	P169	643
I/O	P144	V4	P170	646
I/O	P145	U5	P171	649
I/O	P146	T6	P172	652
I/O (D1)	P147	V3	P173	655
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P148	V2	P174	658
I/O	-	-	-	661
I/O	-	-	-	664
I/O	P149	U4	P175	667
I/O	P150	T5	P176	670
I/O (D0, DIN)	P151	U3	P177	673
I/O, SGCK4 (DOUT)	P152	T4	P178	676
CCLK	P153	V1	P179	-
VCC	P154	R4	P180	-
O, TDO	P159	U2	P181	0
GND	P160	R3	P182	-
I/O (A0, $\overline{WS}$)	P161	T3	P183	2
I/O, PGCK4 (A1)	P162	U1	P184	5
I/O	P163	P3	P185	8
I/O	P164	R2	P186	11
I/O (CS1, A2)	P165	T2	P187	14
I/O (A3)	P166	N3	P188	17
I/O	-	-	-	20
I/O	-	-	-	23
I/O	-	P4	P189	26
I/O	-	N4	P190	29
I/O	P167	P2	P191	32
I/O	P168	T1	P192	35
I/O	P169	R1	P193	38
I/O	P170	N2	P194	41
GND	P171	M3	P196	-
I/O	P172	P1	P197	44
I/O	P173	N1	P198	47
I/O	-	M4	P199	50
I/O	-	L4	P200	53
VCC	-	-	P201	-
I/O	-	-	-	56
I/O	-	-	-	59
I/O (A4)	P174	M2	P202	62
I/O (A5)	P175	M1	P203	65
I/O	P176	L3	P205	68
I/O	P177	L2	P206	71
I/O	P178	L1	P207	74
I/O	P179	K1	P208	77
I/O (A6)	P180	K2	P209	80
I/O (A7)	P181	K3	P210	83
GND	P182	K4	P211	-

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Additional No Connect (N.C.) Connections on HQ208 & HQ240 Packages

HQ208	HQ240
P1	P22 ‡
P3	P37 ‡
P51	P83 ‡
P52	P98 ‡
P53	P143 ‡
P54	P158 ‡
P102	P195
P104	P204 ‡
P105	P219 ‡
P107	
P155	
P156	
P157	
P158	
P206	
P207	
P208	

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‡ Pins marked with this symbol are reserved for Ground connections on future revisions of the device. These pins do not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

Pin Locations for XC4025E, XC4028EX, & XC4028XL Devices

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
VCC	P183	J4	P212	K1	P38	VCC*	-
I/O (A8)	P184	J3	P213	K2	P37	D14	98
I/O (A9)	P185	J2	P214	K3	P36	C14	101
I/O (A19)	P186	J1	P215	K5	P35	A15	104
I/O (A18)	P187	H1	P216	K4	P34	B15	107
I/O	P188	H2	P217	J1	P33	C15	110
I/O	P189	H3	P218	J2	P32	D15	113
I/O (A10)	P190	G1	P220	H1	P31	A16	116
I/O (A11)	P191	G2	P221	J3	P30	B16	119
GND	-	-	-	-	-	GND*	-
I/O	-	-	-	J4	P29	C16	122
I/O	-	-	-	J5	P28	B17	125
I/O	-	-	-	H2	P27	C17	128
I/O	-	-	-	G1	P26	B18	131
VCC	-	-	P222	E1	P25	VCC*	-
I/O	-	H4	P223	H3	P23	C18	134
I/O	-	G4	P224	G2	P22	D17	137
I/O	P192	F1	P225	H4	P21	A20	140
I/O	P193	E1	P226	F2	P20	B19	143
GND	P194	G3	P227	F1	P19	GND*	-
I/O	-	-	-	H5	P18	C19	146
I/O	-	-	-	G3	P17	D18	149
I/O	P195	F2	P228	D1	P16	A21	152
I/O	P196	D1	P229	G4	P15	B20	155
I/O	P197	C1	P230	E2	P14	C20	158
I/O	P198	E2	P231	F3	P13	B21	161
I/O (A12)	P199	F3	P232	G5	P12	B22	164
I/O (A13)	P200	D2	P233	C1	P10	C21	167
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O	-	-	-	F4	P9	D20	170
I/O	-	-	-	E3	P8	A23	173
I/O	-	F4	P234	D2	P7	D21	176
I/O	-	E4	P235	C2	P6	C22	179
I/O	P201	B1	P236	F5	P5	B24	182
I/O	P202	E3	P237	E4	P4	C23	185
I/O (A14)	P203	C2	P238	D3	P3	D22	188
I/O, SGCK1, GCK8 (A15)	P204	B2	P239	C3	P2	C24	191
VCC	P205	D3	P240	A2	P1	VCC*	-
GND	P2	D4	P1	B1	P304	GND*	-
I/O, PGCK1, GCK1 (A16)	P4	C3	P2	D4	P303	D23	194
I/O (A17)	P5	C4	P3	B2	P302	C25	197
I/O	P6	B3	P4	B3	P301	D24	200
I/O	P7	C5	P5	E6	P300	E23	203
I/O, TDI	P8	A2	P6	D5	P299	C26	206
I/O, TCK	P9	B4	P7	C4	P298	E24	209
I/O	-	-	-	A3	P297	F24	212

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	-	-	-	D6	P296	E25	215
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O	P10	C6	P8	E7	P295	D26	218
I/O	P11	A3	P9	B4	P294	G24	221
I/O	P12	B5	P10	C5	P293	F25	224
I/O	P13	B6	P11	A4	P292	F26	227
I/O	-	D5	P12	D7	P291	H23	230
I/O	-	D6	P13	C6	P290	H24	233
I/O	-	-	-	E8	P289	G25	236
I/O	-	-	-	B5	P288	G26	239
GND	P14	C7	P14	A5	P287	GND*	-
I/O, FCLK1	P15	A4	P15	B6	P286	J23	242
I/O	P16	A5	P16	D8	P285	J24	245
I/O, TMS	P17	B7	P17	C7	P284	H25	248
I/O	P18	A6	P18	B7	P283	K23	251
VCC	-	-	P19	A6	P282	VCC*	-
I/O	-	D7	P20	C8	P280	K24	254
I/O	-	D8	P21	E9	P279	J25	257
I/O	-	-	-	A7	P278	L24	260
I/O	-	-	-	D9	P277	K25	263
GND‡	-	-	P22	-	-	GND*	-
I/O	-	-	-	B8	P276	L25	266
I/O	-	-	-	A8	P275	L26	269
I/O	P19	C8	P23	C9	P274	M23	272
I/O	P20	A7	P24	B9	P273	M24	275
I/O	P21	B8	P25	E10	P272	M25	278
I/O	P22	A8	P26	A9	P271	M26	281
I/O	P23	B9	P27	D10	P270	N24	284
I/O	P24	C9	P28	C10	P269	N25	287
GND	P25	D9	P29	A10	P268	GND*	-
VCC	P26	D10	P30	A11	P267	VCC*	-
I/O	P27	C10	P31	B10	P266	N26	290
I/O	P28	B10	P32	B11	P265	P25	293
I/O	P29	A9	P33	C11	P264	P23	296
I/O	P30	A10	P34	E11	P263	P24	299
I/O	P31	A11	P35	D11	P262	R26	302
I/O	P32	C11	P36	A12	P261	R25	305
I/O	-	-	-	B12	P260	R24	308
I/O	-	-	-	A13	P259	R23	311
GND‡	-	-	P37	-	-	GND*	-
I/O	-	-	-	C12	P258	T26	314
I/O	-	-	-	D12	P257	T25	317
I/O	-	D11	P38	E12	P256	T23	320
I/O	-	D12	P39	B13	P255	V26	323
VCC	-	-	P40	A16	P253	VCC*	-
I/O	P33	B11	P41	A14	P252	U24	326
I/O	P34	A12	P42	C13	P251	V25	329
I/O	P35	B12	P43	B14	P250	V24	332
I/O, FCLK2	P36	A13	P44	D13	P249	U23	335
GND	P37	C12	P45	A15	P248	GND*	-

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	-	-	-	B15	P247	Y26	338
I/O	-	-	-	E13	P246	W25	341
I/O	-	D13	P46	C14	P245	W24	344
I/O	-	D14	P47	A17	P244	V23	347
I/O	P38	B13	P48	D14	P243	AA26	350
I/O	P39	A14	P49	B16	P242	Y25	353
I/O	P40	A15	P50	C15	P241	Y24	356
I/O	P41	C13	P51	E14	P240	AA25	359
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O	-	-	-	A18	P239	AB25	362
I/O	-	-	-	D15	P238	AA24	365
I/O	P42	B14	P52	C16	P237	Y23	368
I/O	P43	A16	P53	B17	P236	AC26	371
I/O	P44	B15	P54	B18	P235	AA23	374
I/O	P45	C14	P55	E15	P234	AB24	377
I/O	P46	A17	P56	D16	P233	AD25	380
I/O, SGCK2, GCK2	P47	B16	P57	C17	P232	AC24	383
O (M1)	P48	C15	P58	A20	P231	AB23	386
GND	P49	D15	P59	A19	P230	GND*	-
I (M0)	P50	A18	P60	C18	P229	AD24	389
VCC	P55	D16	P61	B20	P228	VCC*	-
I (M2)	P56	C16	P62	D17	P227	AC23	390
I/O, PGCK2, GCK3	P57	B17	P63	B19	P226	AE24	391
I/O (HDC)	P58	E16	P64	C19	P225	AD23	394
I/O	P59	C17	P65	F16	P224	AC22	397
I/O	P60	D17	P66	E17	P223	AF24	400
I/O	P61	B18	P67	D18	P222	AD22	403
I/O ($\overline{\text{LDC}}$)	P62	E17	P68	C20	P221	AE23	406
I/O	-	-	-	F17	P220	AE22	409
I/O	-	-	-	G16	P219	AF23	412
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O	P63	F16	P69	D19	P218	AD20	415
I/O	P64	C18	P70	E18	P217	AE21	418
I/O	P65	D18	P71	D20	P216	AF21	421
I/O	P66	F17	P72	G17	P215	AC19	424
I/O	-	E15	P73	F18	P214	AD19	427
I/O	-	F15	P74	H16	P213	AE20	430
I/O	-	-	-	E19	P212	AF20	433
I/O	-	-	-	F19	P211	AC18	436
GND	P67	G16	P75	E20	P210	GND*	-
I/O	P68	E18	P76	H17	P209	AD18	439
I/O	P69	F18	P77	G18	P208	AE19	442
I/O	P70	G17	P78	G19	P207	AC17	445
I/O	P71	G18	P79	H18	P206	AD17	448
VCC	-	-	P80	F20	P204	VCC*	-
I/O	P72	H16	P81	J16	P203	AE18	451
I/O	P73	H17	P82	G20	P202	AF18	454

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	-	-	-	J17	P201	AE17	457
I/O	-	-	-	H19	P200	AE16	460
GND‡	-	-	P83	-	-	GND*	-
I/O	-	-	-	H20	P199	AF16	463
I/O	-	-	-	J18	P198	AC15	466
I/O	-	G15	P84	J19	P197	AD15	469
I/O	-	H15	P85	K16	P196	AE15	472
I/O	P74	H18	P86	J20	P195	AF15	475
I/O	P75	J18	P87	K17	P194	AD14	478
I/O	P76	J17	P88	K18	P193	AE14	481
I/O ($\overline{\text{INIT}}$)	P77	J16	P89	K19	P192	AF14	484
VCC	P78	J15	P90	L20	P191	VCC*	-
GND	P79	K15	P91	K20	P190	GND*	-
I/O	P80	K16	P92	L19	P189	AE13	487
I/O	P81	K17	P93	L18	P188	AC13	490
I/O	P82	K18	P94	L16	P187	AD13	493
I/O	P83	L18	P95	L17	P186	AF12	496
I/O	P84	L17	P96	M20	P185	AE12	499
I/O	P85	L16	P97	M19	P184	AD12	502
I/O	-	-	-	N20	P183	AC12	505
I/O	-	-	-	M18	P182	AF11	508
GND‡	-	-	P98	-	-	GND*	-
I/O	-	-	-	M17	P181	AE11	511
I/O	-	-	-	M16	P180	AD11	514
I/O	-	L15	P99	N19	P179	AF9	517
I/O	-	M15	P100	P20	P178	AD10	520
VCC	-	-	P101	T20	P177	VCC*	-
I/O	P86	M18	P102	N18	P175	AE9	523
I/O	P87	M17	P103	P19	P174	AD9	526
I/O	P88	N18	P104	N17	P173	AC10	529
I/O	P89	P18	P105	R19	P172	AF7	532
GND	P90	M16	P106	R20	P171	GND*	-
I/O	-	-	-	N16	P170	AE8	535
I/O	-	-	-	P18	P169	AD8	538
I/O	-	N15	P107	U20	P168	AC9	541
I/O	-	P15	P108	P17	P167	AF6	544
I/O	P91	N17	P109	T19	P166	AE7	547
I/O	P92	R18	P110	R18	P165	AD7	550
I/O	P93	T18	P111	P16	P164	AE6	553
I/O	P94	P17	P112	V20	P163	AE5	556
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O	-	-	-	R17	P162	AD6	559
I/O	-	-	-	T18	P161	AC7	562
I/O	P95	N16	P113	U19	P160	AF4	565
I/O	P96	T17	P114	V19	P159	AF3	568
I/O	P97	R17	P115	R16	P158	AD5	571
I/O	P98	P16	P116	T17	P157	AE3	574
I/O	P99	U18	P117	U18	P156	AD4	577
I/O, SGCK3, GCK4	P100	T16	P118	X20	P155	AC5	580

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
GND	P101	R16	P119	W20	P154	GND*	-
DONE	P103	U17	P120	V18	P153	AD3	-
VCC	P106	R15	P121	X19	P152	VCC*	-
PROGRAM	P108	V18	P122	U17	P151	AC4	-
I/O (D7)	P109	T15	P123	W19	P150	AD2	583
I/O, PGCK3, GCK5	P110	U16	P124	W18	P149	AC3	586
I/O	P111	T14	P125	T15	P148	AB4	589
I/O	P112	U15	P126	U16	P147	AD1	592
I/O	-	R14	P127	V17	P146	AA4	595
I/O	-	R13	P128	X18	P145	AA3	598
I/O	-	-	-	U15	P144	AB2	601
I/O	-	-	-	T14	P143	AC1	604
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O (D6)	P113	V17	P129	W17	P142	Y3	607
I/O	P114	V16	P130	V16	P141	AA2	610
I/O	P115	T13	P131	X17	P140	AA1	613
I/O	P116	U14	P132	U14	P139	W4	616
I/O	P117	V15	P133	V15	P138	W3	619
I/O	P118	V14	P134	T13	P137	Y2	622
I/O	-	-	-	W16	P136	Y1	625
I/O	-	-	-	W15	P135	V4	628
GND	P119	T12	P135	X16	P134	GND*	-
I/O	-	R12	P136	U13	P133	V3	631
I/O	-	R11	P137	V14	P132	W2	634
I/O, FCLK3	P120	U13	P138	W14	P131	U4	637
I/O	P121	V13	P139	V13	P130	U3	640
VCC	-	-	P140	X15	P129	VCC*	-
I/O (D5)	P122	U12	P141	T12	P127	V2	643
I/O ($\overline{CS0}$)	P123	V12	P142	X14	P126	V1	646
GND‡	-	-	P143	-	-	-	-
I/O	-	-	-	U12	P125	U2	649
I/O	-	-	-	W13	P124	T2	652
GND	-	-	-	-	-	GND*	-
I/O	-	-	-	X13	P123	T1	655
I/O	-	-	-	V12	P122	R4	658
I/O	P124	T11	P144	W12	P121	R3	661
I/O	P125	U11	P145	T11	P120	R2	664
I/O	P126	V11	P146	X12	P119	R1	667
I/O	P127	V10	P147	U11	P118	P3	670
I/O (D4)	P128	U10	P148	V11	P117	P2	673
I/O	P129	T10	P149	W11	P116	P1	676
VCC	P130	R10	P150	X10	P115	VCC*	-
GND	P131	R9	P151	X11	P114	GND*	-
I/O (D3)	P132	T9	P152	W10	P113	N2	679
I/O ($\overline{RS}$)	P133	U9	P153	V10	P112	N4	682
I/O	P134	V9	P154	T10	P111	N3	685
I/O	P135	V8	P155	U10	P110	M1	688
I/O	P136	U8	P156	X9	P109	M2	691
I/O	P137	T8	P157	W9	P108	M3	694

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	-	-	-	X8	P107	M4	697
I/O	-	-	-	V9	P106	L1	700
GND‡	-	-	P158	-	-	GND*	-
I/O	-	-	-	U9	P105	L2	703
I/O	-	-	-	T9	P104	L3	706
I/O (D2)	P138	V7	P159	W8	P103	J1	709
I/O	P139	U7	P160	X7	P102	K3	712
VCC	-	-	P161	X5	P101	VCC*	-
I/O	P140	V6	P162	V8	P99	J2	715
I/O, FCLK4	P141	U6	P163	W7	P98	J3	718
I/O	-	R8	P164	U8	P97	K4	721
I/O	-	R7	P165	W6	P96	G1	724
GND	P142	T7	P166	X6	P95	GND*	-
I/O	-	-	-	T8	P94	H2	727
I/O	-	-	-	V7	P93	H3	730
I/O	-	R6	P167	X4	P92	J4	733
I/O	-	R5	P168	U7	P91	F1	736
I/O	P143	V5	P169	W5	P90	G2	739
I/O	P144	V4	P170	V6	P89	G3	742
I/O	P145	U5	P171	T7	P88	F2	745
I/O	P146	T6	P172	X3	P87	E2	748
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O (D1)	P147	V3	P173	U6	P86	F3	751
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P148	V2	P174	V5	P85	G4	754
I/O	-	-	-	W4	P84	D2	757
I/O	-	-	-	W3	P83	F4	760
I/O	P149	U4	P175	T6	P82	E3	763
I/O	P150	T5	P176	U5	P81	C2	766
I/O (D0, DIN)	P151	U3	P177	V4	P80	D3	769
I/O, SGCK4, GCK6 (DOUT)	P152	T4	P178	X1	P79	E4	772
CCLK	P153	V1	P179	V3	P78	C3	-
VCC	P154	R4	P180	W1	P77	VCC*	-
O, TDO	P159	U2	P181	U4	P76	D4	0
GND	P160	R3	P182	X2	P75	GND*	-
I/O (A0, $\overline{WS}$)	P161	T3	P183	W2	P74	B3	2
I/O, PGCK4, GCK7 (A1)	P162	U1	P184	V2	P73	C4	5
I/O	P163	P3	P185	R5	P72	D5	8
I/O	P164	R2	P186	T4	P71	A3	11
I/O (CS1, A2)	P165	T2	P187	U3	P70	D6	14
I/O (A3)	P166	N3	P188	V1	P69	C6	17
I/O	-	-	-	R4	P68	B5	20
I/O	-	-	-	P5	P67	A4	23
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O	-	P4	P189	U2	P66	C7	26

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	-	N4	P190	T3	P65	B6	29
I/O	P167	P2	P191	U1	P64	A6	32
I/O	P168	T1	P192	P4	P63	D8	35
I/O	P169	R1	P193	R3	P62	B7	38
I/O	P170	N2	P194	N5	P61	A7	41
I/O	-	-	P195	T2	P60	D9	44
I/O	-	-	-	R2	P59	C9	47
GND	P171	M3	P196	T1	P58	GND*	-
I/O	P172	P1	P197	N4	P57	B8	50
I/O	P173	N1	P198	P3	P56	D10	53
I/O	-	M4	P199	P2	P55	C10	56
I/O	-	L4	P200	N3	P54	B9	59
VCC	-	-	P201	R1	P52	VCC*	-
I/O	-	-	-	M5	P51	A9	62
I/O	-	-	-	P1	P50	D11	65
I/O	-	-	-	M4	P49	B11	68
I/O	-	-	-	N2	P48	A11	71
GND	-	-	-	-	-	GND*	-
I/O (A4)	P174	M2	P202	N1	P47	D12	74
I/O (A5)	P175	M1	P203	M3	P46	C12	77
I/O	P176	L3	P205	M2	P45	B12	80
I/O	P177	L2	P206	L5	P44	A12	83
I/O (A21)	P178	L1	P207	M1	P43	C13	86
I/O (A20)	P179	K1	P208	L4	P42	B13	89
I/O (A6)	P180	K2	P209	L3	P41	A13	92
I/O (A7)	P181	K3	P210	L2	P40	B14	95
GND	P182	K4	P211	L1	P39	GND*	-

4/2/96

Pads labelled GND* are internally bonded to a Ground plane within the BG352 package. They have no direct connection to any package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the BG352 package. They have no direct connection to any package pin.

Pads labelled GND‡ should be connected to Ground if possible; however, they can be left unconnected if necessary for compatibility with other devices.

Additional No Connect (N.C.) Connections on HQ208 Package

N.C.	N.C.
P1	P107
P3	P155
P51	P156
P52	P157
P53	P158
P54	P206
P102	P207
P104	P208
P105	

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Additional Ground (GND) Connections on HQ240 Package

GND
P204
P219

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The Ground (GND) package pins in the above table should be externally connected to Ground if possible; however, they can be left unconnected if necessary for compatibility with other devices.

Additional No Connect (N.C.) Connections on HQ304 Package

N.C.
P11
P24
P53
P100
P128
P176
P205
P254
P281

3/21/96

Note: In XC4025 (no extension) devices in the HQ304 package, P101 is a No Connect (N.C.) pin. P101 is Vcc in XC4025E/L and XC4028EX/XL devices. Where necessary for compatibility, this pin can be left unconnected.

Additional No Connect, Vcc & Ground Connections on BG352 Package

N.C.	VCC	GND
A18	A10	A1
A24	A17	A2
B4	B2	A5
B10	B25	A8
B23	D7	A14
C1	D13	A19
C5	D19	A22
C8	G23	A25
C11	H4	A26
D1	K1	B1
D16	K26	B26
D25	N23	E1
F23	P4	E26
J26	U1	H1
K2	U26	H26
L4	W23	N1
L23	Y4	P26
T3	AC8	W1
T4	AC14	W26
T24	AC20	AB1
U25	AE2	AB26
AB3	AE25	AE1
AC2	AF10	AE26
AC6	AF17	AF1
AC11		AF2
AC16		AF5
AC21		AF8
AC25		AF13
AD16		AF19
AD21		AF22
AD26		AF25
AE4		AF26
AE10		

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Pin Locations for XC4036EX/XL Devices

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
GND	P304	GND*	GND*	-
I/O, GCK1 (A16)	P303	H8	D29	218
I/O (A17)	P302	F6	C30	221
I/O	P301	B4	E28	224
I/O	P300	D4	E29	227
I/O, TDI	P299	B2	D30	230
I/O, TCK	P298	G9	D31	233
I/O	-	F8	E30	236
I/O	-	C5	E31	239
I/O	P297	A7	G28	242
I/O	P296	A5	G29	245
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P295	B8	H28	248
I/O	P294	C9	H29	251
I/O	P293	E9	G30	254
I/O	P292	F12	H30	257
I/O	P291	D10	J28	260
I/O	P290	B10	J29	263
I/O	P289	F10	H31	266
I/O	P288	F14	J30	269
GND	P287	GND*	GND*	-
I/O, FCLK1	P286	C11	K28	272
I/O	P285	B12	K29	275
I/O, TMS	P284	E11	K30	278
I/O	P283	E15	K31	281
VCC	P282	VCC*	VCC*	-
I/O	P280	F16	L29	284
I/O	P279	C13	L30	287
I/O	-	B14	M29	290
I/O	-	E17	M31	293
I/O	P278	E13	N31	296
I/O	P277	A15	N28	299
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P276	B16	P30	302
I/O	P275	D16	P28	305
I/O	P274	D18	P29	308
I/O	P273	A17	R31	311
I/O	P272	E19	R30	314
I/O	P271	B18	R28	317
I/O	P270	C17	R29	320
I/O	P269	C19	T31	323
GND	P268	GND*	GND*	-
VCC	P267	VCC*	VCC*	-
I/O	P266	F20	T30	326
I/O	P265	B20	T29	329
I/O	P264	C21	U31	332
I/O	P263	B22	U30	335
I/O	P262	E21	U28	338
I/O	P261	D22	U29	341
I/O	P260	A23	V30	344
I/O	P259	B24	V29	347
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P258	A25	W30	350
I/O	P257	D24	W29	353
I/O	-	B26	Y30	356
I/O	-	A27	Y29	359
I/O	P256	C27	Y28	362
I/O	P255	F24	AA30	365
VCC	P253	VCC*	VCC*	-
I/O	P252	E25	AA29	368
I/O	P251	E27	AB31	371
I/O	P250	B28	AB30	374
I/O, FCLK2	P249	C29	AB29	377
GND	P248	GND*	GND*	-
I/O	P247	F26	AB28	380
I/O	P246	D28	AC30	383
I/O	P245	B30	AC29	386
I/O	P244	E29	AC28	389
I/O	P243	F28	AD29	392
I/O	P242	F30	AD28	395
I/O	P241	C31	AE30	398
I/O	P240	E31	AE29	401
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P239	B32	AF31	404
I/O	P238	A33	AE28	407
I/O	P237	A35	AG31	410
I/O	P236	F32	AF28	413
I/O	-	C35	AG30	416
I/O	-	B38	AG29	419
I/O	P235	E33	AH31	422
I/O	P234	G31	AG28	425
I/O	P233	H32	AH30	428
I/O, GCK2	P232	B36	AJ30	431
O (M1)	P231	A39	AH29	434
GND	P230	GND*	GND*	-
I (M0)	P229	E35	AH28	437
VCC	P228	VCC*	VCC*	-
I (M2)	P227	G33	AJ28	438

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O, GCK3	P226	D36	AK29	439
I/O (HDC)	P225	C37	AH27	442
I/O	P224	F34	AK28	445
I/O	P223	J33	AJ27	448
I/O	P222	D38	AL28	451
I/O ($\overline{LDC}$)	P221	G35	AH26	454
I/O	-	E39	AL27	457
I/O	-	K34	AH25	460
I/O	P220	F38	AK26	463
I/O	P219	G37	AL26	466
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P218	H38	AH24	469
I/O	P217	J37	AJ25	472
I/O	P216	G39	AK25	475
I/O	P215	M34	AJ24	478
I/O	P214	N35	AL24	481
I/O	P213	P34	AH22	484
I/O	P212	J35	AJ23	487
I/O	P211	L37	AK23	490
GND	P210	GND*	GND*	-
I/O	P209	M38	AJ22	493
I/O	P208	R35	AK22	496
I/O	P207	H36	AL22	499
I/O	P206	T34	AJ21	502
VCC	P204	VCC*	VCC*	-
I/O	P203	N37	AH20	505
I/O	P202	N39	AK21	508
I/O	-	U35	AK20	511
I/O	-	R39	AJ19	514
I/O	P201	M36	AL20	517
I/O	P200	V34	AH18	520
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P199	R37	AK19	523
I/O	P198	T38	AJ18	526
I/O	P197	T36	AL19	529
I/O	P196	V36	AK18	532
I/O	P195	U37	AH17	535
I/O	P194	U39	AJ17	538
I/O	P193	V38	AJ16	541
I/O ($\overline{INIT}$)	P192	W37	AK16	544
VCC	P191	VCC*	VCC*	-
GND	P190	GND*	GND*	-
I/O	P189	Y34	AL16	547
I/O	P188	AC37	AH15	550
I/O	P187	AB38	AK15	553

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O	P186	AD36	AJ14	556
I/O	P185	AA35	AH14	559
I/O	P184	AE37	AK14	562
I/O	P183	AB36	AL13	565
I/O	P182	AD38	AK13	568
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P181	AB34	AJ13	571
I/O	P180	AE39	AH13	574
I/O	-	AM36	AL12	577
I/O	-	AC35	AK12	580
I/O	P179	AG39	AH12	583
I/O	P178	AG37	AJ11	586
VCC	P177	VCC*	VCC*	-
I/O	P175	AD34	AL10	589
I/O	P174	AN39	AK10	592
I/O	P173	AE35	AJ10	595
I/O	P172	AH38	AK9	598
GND	P171	GND*	GND*	-
I/O	P170	AJ37	AL8	601
I/O	P169	AG35	AH10	604
I/O	P168	AF34	AJ9	607
I/O	P167	AH36	AK8	610
I/O	P166	AK36	AK7	613
I/O	P165	AM34	AL6	616
I/O	P164	AH34	AJ7	619
I/O	P163	AJ35	AH8	622
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P162	AL37	AK6	625
I/O	P161	AT38	AL5	628
I/O	P160	AM38	AH7	631
I/O	P159	AN37	AJ6	634
I/O	-	AK34	AK5	637
I/O	-	AR39	AL4	640
I/O	P158	AN35	AK4	643
I/O	P157	AL33	AH5	646
I/O	P156	AV38	AK3	649
I/O, GCK4	P155	AT36	AJ4	652
GND	P154	GND*	GND*	-
DONE	P153	AR35	AH4	-
VCC	P152	VCC*	VCC*	-
$\overline{PROGRAM}$	P151	AN33	AH3	-
I/O (D7)	P150	AM32	AJ2	655
I/O, GCK5	P149	AP34	AG4	658
I/O	P148	AW39	AG3	661
I/O	P147	AN31	AH2	664

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O	-	AV36	AH1	667
I/O	-	AR33	AF4	670
I/O	P146	AP32	AF3	673
I/O	P145	AU35	AG2	676
I/O	P144	AW33	AE3	679
I/O	P143	AU33	AF2	682
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O (D6)	P142	AV32	AF1	685
I/O	P141	AU31	AD4	688
I/O	P140	AR31	AD3	691
I/O	P139	AP28	AE2	694
I/O	P138	AT32	AC3	697
I/O	P137	AV30	AD1	700
I/O	P136	AR29	AC2	703
I/O	P135	AP26	AB4	706
GND	P134	GND*	GND*	-
I/O	P133	AU29	AB3	709
I/O	P132	AV28	AB2	712
I/O, FCLK3	P131	AT28	AB1	715
I/O	P130	AR25	AA3	718
VCC	P129	VCC*	VCC*	-
I/O (D5)	P127	AP24	AA2	721
I/O ($\overline{CS0}$)	P126	AU27	Y2	724
I/O	-	AR27	Y4	727
I/O	-	AW27	Y3	730
I/O	P125	AT24	W4	733
I/O	P124	AR23	W3	736
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P123	AP22	V4	739
I/O	P122	AV24	V3	742
I/O	P121	AU23	U1	745
I/O	P120	AT22	U2	748
I/O	P119	AR21	U4	751
I/O	P118	AV22	U3	754
I/O (D4)	P117	AP20	T1	757
I/O	P116	AU21	T2	760
VCC	P115	VCC*	VCC*	-
GND	P114	GND*	GND*	-
I/O (D3)	P113	AU19	T3	763
I/O ($\overline{RS}$)	P112	AV20	R1	766
I/O	P111	AV18	R2	769
I/O	P110	AR19	R4	772
I/O	P109	AT18	R3	775
I/O	P108	AW17	P2	778
I/O	P107	AV16	P3	781

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O	P106	AP18	P4	784
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P105	AR17	N3	787
I/O	P104	AT16	N4	790
I/O	-	AV14	M1	793
I/O	-	AW13	M2	796
I/O (D2)	P103	AR15	L2	799
I/O	P102	AP16	L3	802
VCC	P101	VCC*	VCC*	-
I/O	P99	AV12	K1	805
I/O, FCLK4	P98	AR13	K2	808
I/O	P97	AU11	K3	811
I/O	P96	AT12	K4	814
GND	P95	GND*	GND*	-
I/O	P94	AP14	J2	817
I/O	P93	AR11	J3	820
I/O	P92	AV10	J4	823
I/O	P91	AT8	H1	826
I/O	P90	AT10	H2	829
I/O	P89	AP10	H3	832
I/O	P88	AP12	H4	835
I/O	P87	AR9	G2	838
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O (D1)	P86	AU7	G4	841
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P85	AW7	F2	844
I/O	-	AW5	F3	847
I/O	-	AV6	E1	850
I/O	P84	AR7	E3	853
I/O	P83	AV4	D1	856
I/O	P82	AN9	E4	859
I/O	P81	AW1	D2	862
I/O (D0, DIN)	P80	AP6	C2	865
I/O, GCK6 (DOUT)	P79	AU3	D3	868
CCLK	P78	AR5	D4	-
VCC	P77	VCC*	VCC*	-
O, TDO	P76	AN7	C4	0
GND	P75	GND*	GND*	-
I/O (A0, $\overline{WS}$)	P74	AT4	B3	2
I/O, GCK7 (A1)	P73	AV2	D5	5
I/O	P72	AM8	B4	8
I/O	P71	AL7	C5	11
I/O	-	AR3	B5	14
I/O	-	AR1	C6	17
I/O (CS1, A2)	P70	AK6	A5	20

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O (A3)	P69	AN3	D7	23
I/O	P68	AM6	B6	26
I/O	P67	AM2	A6	29
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P66	AL3	D8	32
I/O	P65	AH6	C7	35
I/O	P64	AP2	B7	38
I/O	P63	AK4	D9	41
I/O	P62	AG5	D10	44
I/O	P61	AF6	C9	47
I/O	P60	AL5	B9	50
I/O	P59	AJ3	C10	53
GND	P58	GND*	GND*	-
I/O	P57	AH2	B10	56
I/O	P56	AE5	A10	59
I/O	P55	AM4	C11	62
I/O	P54	AD6	D12	65
VCC	P52	VCC*	VCC*	-
I/O	P51	AG3	B11	68
I/O	P50	AG1	C12	71
I/O	-	AC5	C13	74
I/O	-	AE1	A12	77
I/O	P49	AH4	D14	80
I/O	P48	AB6	B13	83
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O (A4)	P47	AD2	C14	86
I/O (A5)	P46	AB4	A13	89
I/O	P45	AE3	B14	92
I/O	P44	AC1	D15	95
I/O (A21)	P43	AD4	C15	98
I/O (A20)	P42	AA5	B15	101
I/O (A6)	P41	AA3	B16	104
I/O (A7)	P40	Y6	A16	107
GND	P39	GND*	GND*	-
VCC	P38	VCC*	VCC*	-
I/O (A8)	P37	W3	D17	110
I/O (A9)	P36	Y2	A17	113
I/O (A19)	P35	V4	C18	116
I/O (A18)	P34	T2	D18	119
I/O	P33	U1	B18	122
I/O	P32	V6	A19	125
I/O (A10)	P31	U3	B19	128
I/O (A11)	P30	R1	C19	131
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O	P29	U5	D19	134
I/O	P28	T4	A20	137
I/O	-	P2	B20	140
I/O	-	N1	C20	143
I/O	P27	R5	C21	146
I/O	P26	M2	A22	149
VCC	P25	VCC*	VCC*	-
I/O	P23	L3	B22	152
I/O	P22	T6	C22	155
I/O	P21	N5	B23	158
I/O	P20	M4	A24	161
GND	P19	GND*	GND*	-
I/O	P18	K2	D22	164
I/O	P17	K4	C23	167
I/O	P16	P6	B24	170
I/O	P15	M6	C24	173
I/O	P14	J3	A26	176
I/O	P13	H2	C25	179
I/O (A12)	P12	H4	D24	182
I/O (A13)	P10	G3	B26	185
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P9	K6	A27	188
I/O	P8	G1	D25	191
I/O	-	E1	C26	194
I/O	-	E3	B27	197
I/O	P7	J7	C27	200
I/O	P6	H6	B28	203
I/O	P5	C3	D27	206
I/O	P4	D2	B29	209
I/O (A14)	P3	E5	C28	212
I/O, GCK8 (A15)	P2	G7	D28	215
VCC	P1	VCC*	VCC*	-

4/2/96

Pads labelled GND* are internally bonded to a Ground plane within the associated package. They have no direct connection to any package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the associated package. They have no direct connection to any package pin.

Additional No Connect (N.C.) Connections on HQ304 Package

N.C.	N.C.
P11	P176
P24	P205
P53	P254
P100	P281
P128	

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Additional No Connect, Vcc & Ground Connections on PG411 Package

N.C.	N.C.	VCC	GND
A13	AA37	A3	A9
B6	AB2	A11	A19
B34	AC3	A21	A29
C7	AC39	A31	A37
C15	AF2	C39	C1
C23	AF38	D6	D14
C25	AJ5	F36	D20
C33	AK2	J1	D26
D8	AK38	L39	D34
D12	AL35	W1	F4
D30	AN1	AA39	J39
D32	AN5	AJ1	L1
E7	AP8	AL39	P4
E23	AP30	AP4	P36
E37	AP38	AT34	W39
F2	AR37	AU1	Y4
F18	AT2	AW9	Y36
F22	AT30	AW19	AA1
G5	AU5	AW29	AF4
H34	AU9	AW37	AF36
J5	AU13		AJ39
K36	AU15		AL1
K38	AU17		AP36
L5	AU25		AT6
L35	AU37		AT14
N3	AV8		AT20
P38	AV26		AT26
R3	AV34		AU39
V2	AW15		AW3
W5	AW23		AW11
W35	AW25		AW21
Y38	AW35		AW31

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Additional No Connect, Vcc & Ground Connections on BG432 Package

N.C.	N.C.	VCC	GND
A4	AG1	A1	A2
A8	AH6	A11	A3
A15	AH9	A21	A7
A28	AH19	A31	A9
B8	AH23	C3	A14
B12	AJ5	C29	A18
B17	AJ8	D11	A23
B21	AJ12	D21	A25
B25	AJ15	L1	A29
C8	AJ20	L4	A30
C16	AJ26	L28	B1
C17	AK11	L31	B2
D6	AK17	AA1	B30
D13	AK24	AA4	B31
D20	AK27	AA28	C1
D23	AL15	AA31	C31
D26	AL17	AH11	D16
E2		AH21	G1
F1		AJ3	G31
F4		AJ29	J1
F28		AL1	J31
F29		AL11	P1
F30		AL21	P31
F31		AL31	T4
G3			T28
M3			V1
M4			V31
M28			AC1
M30			AC31
N1			AE1
N2			AE31
N29			AH16
N30			AJ1
V2			AJ31
V28			AK1
W1			AK2
W2			AK30
W28			AK31
W31			AL2
Y1			AL3
Y31			AL7
AC4			AL9
AD2			AL14
AD30			AL18
AD31			AL23
AE4			AL25
AF29			AL29
AF30			AL30

3/22/96

Pin Locations for XC4044EX/XL Devices

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
GND	GND*	GND*	-
I/O, GCK1 (A16)	H8	D29	242
I/O (A17)	F6	C30	245
I/O	B4	E28	248
I/O	D4	E29	251
I/O, TDI	B2	D30	254
I/O, TCK	G9	D31	257
I/O	F8	E30	260
I/O	C5	E31	263
I/O	A7	G28	266
I/O	A5	G29	269
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	C7	F30	272
I/O	D8	F31	275
I/O	B8	H28	278
I/O	C9	H29	281
I/O	E9	G30	284
I/O	F12	H30	287
I/O	D10	J28	290
I/O	B10	J29	293
I/O	F10	H31	296
I/O	F14	J30	299
GND	GND*	GND*	-
I/O, FCLK1	C11	K28	302
I/O	B12	K29	305
I/O, TMS	E11	K30	308
I/O	E15	K31	311
VCC	VCC*	VCC*	-
I/O	F16	L29	314
I/O	C13	L30	317
I/O	B14	M29	320
I/O	E17	M31	323
I/O	E13	N31	326
I/O	A15	N28	329
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	F18	N29	332
I/O	C15	N30	335
I/O	B16	P30	338
I/O	D16	P28	341
I/O	D18	P29	344
I/O	A17	R31	347
I/O	E19	R30	350
I/O	B18	R28	353
I/O	C17	R29	356
I/O	C19	T31	359
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	F20	T30	362

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	B20	T29	365
I/O	C21	U31	368
I/O	B22	U30	371
I/O	E21	U28	374
I/O	D22	U29	377
I/O	A23	V30	380
I/O	B24	V29	383
I/O	C23	V28	386
I/O	F22	W31	389
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	A25	W30	392
I/O	D24	W29	395
I/O	B26	Y30	398
I/O	A27	Y29	401
I/O	C27	Y28	404
I/O	F24	AA30	407
VCC	VCC*	VCC*	-
I/O	E25	AA29	410
I/O	E27	AB31	413
I/O	B28	AB30	416
I/O, FCLK2	C29	AB29	419
GND	GND*	GND*	-
I/O	F26	AB28	422
I/O	D28	AC30	425
I/O	B30	AC29	428
I/O	E29	AC28	431
I/O	D30	AD31	434
I/O	D32	AD30	437
I/O	F28	AD29	440
I/O	F30	AD28	443
I/O	C31	AE30	446
I/O	E31	AE29	449
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	B32	AF31	452
I/O	A33	AE28	455
I/O	A35	AG31	458
I/O	F32	AF28	461
I/O	C35	AG30	464
I/O	B38	AG29	467
I/O	E33	AH31	470
I/O	G31	AG28	473
I/O	H32	AH30	476
I/O, GCK2	B36	AJ30	479
O (M1)	A39	AH29	482
GND	GND*	GND*	-
I (M0)	E35	AH28	485
VCC	VCC*	VCC*	-
I (M2)	G33	AJ28	486
I/O, GCK3	D36	AK29	487
I/O (HDC)	C37	AH27	490

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	F34	AK28	493
I/O	J33	AJ27	496
I/O	D38	AL28	499
I/O ($\overline{LDC}$)	G35	AH26	502
I/O	E39	AL27	505
I/O	K34	AH25	508
I/O	F38	AK26	511
I/O	G37	AL26	514
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	H38	AH24	517
I/O	J37	AJ25	520
I/O	G39	AK25	523
I/O	M34	AJ24	526
I/O	K36	AH23	529
I/O	K38	AK24	532
I/O	N35	AL24	535
I/O	P34	AH22	538
I/O	J35	AJ23	541
I/O	L37	AK23	544
GND	GND*	GND*	-
I/O	M38	AJ22	547
I/O	R35	AK22	550
I/O	H36	AL22	553
I/O	T34	AJ21	556
VCC	VCC*	VCC*	-
I/O	N37	AH20	559
I/O	N39	AK21	562
I/O	U35	AK20	565
I/O	R39	AJ19	568
I/O	M36	AL20	571
I/O	V34	AH18	574
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	R37	AK19	577
I/O	T38	AJ18	580
I/O	T36	AL19	583
I/O	V36	AK18	586
I/O	U37	AH17	589
I/O	U39	AJ17	592
I/O	W35	AK17	595
I/O	AC39	AL17	598
I/O	V38	AJ16	601
I/O ($\overline{INIT}$)	W37	AK16	604
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	Y34	AL16	607
I/O	AC37	AH15	610
I/O	Y38	AL15	613
I/O	AA37	AJ15	616
I/O	AB38	AK15	619
I/O	AD36	AJ14	622

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	AA35	AH14	625
I/O	AE37	AK14	628
I/O	AB36	AL13	631
I/O	AD38	AK13	634
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	AB34	AJ13	637
I/O	AE39	AH13	640
I/O	AM36	AL12	643
I/O	AC35	AK12	646
I/O	AG39	AH12	649
I/O	AG37	AJ11	652
VCC	VCC*	VCC*	-
I/O	AD34	AL10	655
I/O	AN39	AK10	658
I/O	AE35	AJ10	661
I/O	AH38	AK9	664
GND	GND*	GND*	-
I/O	AJ37	AL8	667
I/O	AG35	AH10	670
I/O	AF34	AJ9	673
I/O	AH36	AK8	676
I/O	AK38	AJ8	679
I/O	AP38	AH9	682
I/O	AK36	AK7	685
I/O	AM34	AL6	688
I/O	AH34	AJ7	691
I/O	AJ35	AH8	694
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	AL37	AK6	697
I/O	AT38	AL5	700
I/O	AM38	AH7	703
I/O	AN37	AJ6	706
I/O	AK34	AK5	709
I/O	AR39	AL4	712
I/O	AN35	AK4	715
I/O	AL33	AH5	718
I/O	AV38	AK3	721
I/O, GCK4	AT36	AJ4	724
GND	GND*	GND*	-
DONE	AR35	AH4	-
VCC	VCC*	VCC*	-
$\overline{PROGRAM}$	AN33	AH3	-
I/O (D7)	AM32	AJ2	727
I/O, GCK5	AP34	AG4	730
I/O	AW39	AG3	733
I/O	AN31	AH2	736
I/O	AV36	AH1	739
I/O	AR33	AF4	742
I/O	AP32	AF3	745
I/O	AU35	AG2	748

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	AW33	AE3	751
I/O	AU33	AF2	754
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O (D6)	AV32	AF1	757
I/O	AU31	AD4	760
I/O	AR31	AD3	763
I/O	AP28	AE2	766
I/O	AP30	AD2	769
I/O	AT30	AC4	772
I/O	AT32	AC3	775
I/O	AV30	AD1	778
I/O	AR29	AC2	781
I/O	AP26	AB4	784
GND	GND*	GND*	-
I/O	AU29	AB3	787
I/O	AV28	AB2	790
I/O, FCLK3	AT28	AB1	793
I/O	AR25	AA3	796
VCC	VCC*	VCC*	-
I/O (D5)	AP24	AA2	799
I/O ($\overline{CS0}$)	AU27	Y2	802
I/O	AR27	Y4	805
I/O	AW27	Y3	808
I/O	AT24	W4	811
I/O	AR23	W3	814
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	AW25	W2	817
I/O	AW23	V2	820
I/O	AP22	V4	823
I/O	AV24	V3	826
I/O	AU23	U1	829
I/O	AT22	U2	832
I/O	AR21	U4	835
I/O	AV22	U3	838
I/O (D4)	AP20	T1	841
I/O	AU21	T2	844
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O (D3)	AU19	T3	847
I/O ($\overline{RS}$)	AV20	R1	850
I/O	AV18	R2	853
I/O	AR19	R4	856
I/O	AT18	R3	859
I/O	AW17	P2	862
I/O	AV16	P3	865
I/O	AP18	P4	868
I/O	AU17	N1	871
I/O	AW15	N2	874
VCC	VCC*	VCC*	-
GND	GND*	GND*	-

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	AR17	N3	877
I/O	AT16	N4	880
I/O	AV14	M1	883
I/O	AW13	M2	886
I/O (D2)	AR15	L2	889
I/O	AP16	L3	892
VCC	VCC*	VCC*	-
I/O	AV12	K1	895
I/O, FCLK4	AR13	K2	898
I/O	AU11	K3	901
I/O	AT12	K4	904
GND	GND*	GND*	-
I/O	AP14	J2	907
I/O	AR11	J3	910
I/O	AV10	J4	913
I/O	AT8	H1	916
I/O	AT10	H2	919
I/O	AP10	H3	922
I/O	AP12	H4	925
I/O	AR9	G2	928
I/O	AU9	G3	931
I/O	AV8	F1	934
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O (D1)	AU7	G4	937
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	AW7	F2	940
I/O	AW5	F3	943
I/O	AV6	E1	946
I/O	AR7	E3	949
I/O	AV4	D1	952
I/O	AN9	E4	955
I/O	AW1	D2	958
I/O (D0, DIN)	AP6	C2	961
I/O, GCK6 (DOUT)	AU3	D3	964
CCLK	AR5	D4	-
VCC	VCC*	VCC*	-
O, TDO	AN7	C4	0
GND	GND*	GND*	-
I/O (A0, $\overline{WS}$)	AT4	B3	2
I/O, GCK7 (A1)	AV2	D5	5
I/O	AM8	B4	8
I/O	AL7	C5	11
I/O	AR3	B5	14
I/O	AR1	C6	17
I/O (CS1, A2)	AK6	A5	20
I/O (A3)	AN3	D7	23
I/O	AM6	B6	26
I/O	AM2	A6	29
VCC	VCC*	VCC*	-
GND	GND*	GND*	-

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	AL3	D8	32
I/O	AH6	C7	35
I/O	AP2	B7	38
I/O	AK4	D9	41
I/O	AN1	B8	44
I/O	AK2	A8	47
I/O	AG5	D10	50
I/O	AF6	C9	53
I/O	AL5	B9	56
I/O	AJ3	C10	59
GND	GND*	GND*	-
I/O	AH2	B10	62
I/O	AE5	A10	65
I/O	AM4	C11	68
I/O	AD6	D12	71
VCC	VCC*	VCC*	-
I/O	AG3	B11	74
I/O	AG1	C12	77
I/O	AC5	C13	80
I/O	AE1	A12	83
I/O	AH4	D14	86
I/O	AB6	B13	89
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O (A4)	AD2	C14	92
I/O (A5)	AB4	A13	95
I/O	AE3	B14	98
I/O	AC1	D15	101
I/O (A21)	AD4	C15	104
I/O (A20)	AA5	B15	107
I/O	AB2	A15	110
I/O	AC3	C16	113
I/O (A6)	AA3	B16	116
I/O (A7)	Y6	A16	119
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O (A8)	W3	D17	122
I/O (A9)	Y2	A17	125
I/O	V2	C17	128
I/O	W5	B17	131
I/O (A19)	V4	C18	134
I/O (A18)	T2	D18	137
I/O	U1	B18	140
I/O	V6	A19	143
I/O (A10)	U3	B19	146
I/O (A11)	R1	C19	149
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	U5	D19	152
I/O	T4	A20	155
I/O	P2	B20	158
I/O	N1	C20	161

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	R5	C21	164
I/O	M2	A22	167
VCC	VCC*	VCC*	-
I/O	L3	B22	170
I/O	T6	C22	173
I/O	N5	B23	176
I/O	M4	A24	179
GND	GND*	GND*	-
I/O	K2	D22	182
I/O	K4	C23	185
I/O	P6	B24	188
I/O	M6	C24	191
I/O	L5	D23	194
I/O	J5	B25	197
I/O	J3	A26	200
I/O	H2	C25	203
I/O (A12)	H4	D24	206
I/O (A13)	G3	B26	209
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	K6	A27	212
I/O	G1	D25	215
I/O	E1	C26	218
I/O	E3	B27	221
I/O	J7	C27	224
I/O	H6	B28	227
I/O	C3	D27	230
I/O	D2	B29	233
I/O (A14)	E5	C28	236
I/O, GCK8 (A15)	G7	D28	239
VCC	VCC*	VCC*	-

4/2/96

Pads labelled GND* are internally bonded to a Ground plane within the associated package. They have no direct connection to any package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the associated package. They have no direct connection to any package pin.

Additional No Connect, Vcc & Ground Connections on PG411 Package

N.C.	VCC	GND
A13	A3	A9
B6	A11	A19
B34	A21	A29
C25	A31	A37
C33	C39	C1
D12	D6	D14
E7	F36	D20
E23	J1	D26
E37	L39	D34
F2	W1	F4
G5	AA39	J39
H34	AJ1	L1
L35	AL39	P4
N3	AP4	P36
P38	AT34	W39
R3	AU1	Y4
AF2	AW9	Y36
AF38	AW19	AA1
AJ5	AW29	AF4
AL35	AW37	AF36
AN5		AJ39
AP8		AL1
AR37		AP36
AT2		AT6
AU5		AT14
AU13		AT20
AU15		AT26
AU25		AU39
AU37		AW3
AV26		AW11
AV34		AW21
AW35		AW31

3/22/96

Additional No Connect, Vcc & Ground Connections on BG432 Package

N.C.	VCC	GND
A4	A1	A2
A28	A11	A3
B12	A21	A7
B21	A31	A9
C8	C3	A14
D6	C29	A18
D13	D11	A23
D20	D21	A25
D26	L1	A29
E2	L4	A30
F4	L28	B1
F28	L31	B2
F29	AA1	B30
M3	AA4	B31
M4	AA28	C1
M28	AA31	C31
M30	AH11	D16
W1	AH21	G1
W28	AJ3	G31
Y1	AJ29	J1
Y31	AL1	J31
AE4	AL11	P1
AF29	AL21	P31
AF30	AL31	T4
AG1		T28
AH6		V1
AH19		V31
AJ5		AC1
AJ12		AC31
AJ20		AE1
AJ26		AE31
AK11		AH16
AK27		AJ1
		AJ31
		AK1
		AK2
		AK30
		AK31
		AL2
		AL3
		AL7
		AL9
		AL14
		AL18
		AL23
		AL25
		AL29
		AL30

3/26/96

Pin Locations for XC4052XL Devices

XC4052XL Pad Name	BG432	Bndry Scan
GND	GND*	-
I/O, GCK1 (A16)	D29	266
I/O (A17)	C30	269
I/O	E28	272
I/O	E29	275
I/O, TDI	D30	278
I/O, TCK	D31	281
GND	GND*	-
I/O	F28	284
I/O	F29	287
I/O	E30	290
I/O	E31	293
I/O	G28	296
I/O	G29	299
VCC	VCC*	-
GND	GND*	-
I/O	F30	302
I/O	F31	305
I/O	H28	308
I/O	H29	311
I/O	G30	314
I/O	H30	317
GND	GND*	-
I/O	J28	320
I/O	J29	323
I/O	H31	326
I/O	J30	329
GND	GND*	-
I/O, FCLK1	K28	332
I/O	K29	335
I/O, TMS	K30	338
I/O	K31	341
VCC	VCC*	-
I/O	L29	344
I/O	L30	347
GND	GND*	-
I/O	M30	350
I/O	M28	353
I/O	M29	356
I/O	M31	359
I/O	N31	362
I/O	N28	365
GND	GND*	-
VCC	VCC*	-
I/O	N29	368
I/O	N30	371
I/O	P30	374
I/O	P28	377
I/O	P29	380
I/O	R31	383
GND	GND*	-
I/O	R30	386
I/O	R28	389
I/O	R29	392
I/O	T31	395
GND	GND*	-
VCC	VCC*	-
I/O	T30	398
I/O	T29	401
I/O	U31	404
I/O	U30	407
GND	GND*	-
I/O	U28	410
I/O	U29	413
I/O	V30	416
I/O	V29	419
I/O	V28	422
I/O	W31	425
VCC	VCC*	-
GND	GND*	-
I/O	W30	428
I/O	W29	431
I/O	W28	434
I/O	Y31	437
I/O	Y30	440
I/O	Y29	443
GND	GND*	-
I/O	Y28	446
I/O	AA30	449
VCC	VCC*	-
I/O	AA29	452
I/O	AB31	455
I/O	AB30	458
I/O, FCLK2	AB29	461
GND	GND*	-
I/O	AB28	464
I/O	AC30	467
I/O	AC29	470
I/O	AC28	473
GND	GND*	-
I/O	AD31	476
I/O	AD30	479
I/O	AD29	482
I/O	AD28	485
I/O	AE30	488
I/O	AE29	491
GND	GND*	-
VCC	VCC*	-
I/O	AF31	494
I/O	AE28	497
I/O	AF30	500
I/O	AF29	503
I/O	AG31	506

XC4052XL Pad Name	BG432	Bndry Scan
I/O	AF28	509
GND	GND*	-
I/O	AG30	512
I/O	AG29	515
I/O	AH31	518
I/O	AG28	521
I/O	AH30	524
I/O, GCK2	AJ30	527
O (M1)	AH29	530
GND	GND*	-
I (M0)	AH28	533
VCC	VCC*	-
I (M2)	AJ28	534
I/O, GCK3	AK29	535
I/O (HDC)	AH27	538
I/O	AK28	541
I/O	AJ27	544
I/O	AL28	547
I/O ($\overline{\text{LDC}}$)	AH26	550
GND	GND*	-
I/O	AK27	553
I/O	AJ26	556
I/O	AL27	559
I/O	AH25	562
I/O	AK26	565
I/O	AL26	568
VCC	VCC*	-
GND	GND*	-
I/O	AH24	571
I/O	AJ25	574
I/O	AK25	577
I/O	AJ24	580
I/O	AH23	583
I/O	AK24	586
GND	GND*	-
I/O	AL24	589
I/O	AH22	592
I/O	AJ23	595
I/O	AK23	598
GND	GND*	-
I/O	AJ22	601
I/O	AK22	604
I/O	AL22	607
I/O	AJ21	610
VCC	VCC*	-
I/O	AH20	613
I/O	AK21	616
GND	GND*	-
I/O	AJ20	619
I/O	AH19	622
I/O	AK20	625
I/O	AJ19	628

XC4052XL Pad Name	BG432	Bndry Scan
I/O	AL20	631
I/O	AH18	634
GND	GND*	-
VCC	VCC*	-
I/O	AK19	637
I/O	AJ18	640
I/O	AL19	643
I/O	AK18	646
I/O	AH17	649
I/O	AJ17	652
GND	GND*	-
I/O	AK17	655
I/O	AL17	658
I/O	AJ16	661
I/O ($\overline{\text{INIT}}$)	AK16	664
VCC	VCC*	-
GND	GND*	-
I/O	AL16	667
I/O	AH15	670
I/O	AL15	673
I/O	AJ15	676
GND	GND*	-
I/O	AK15	679
I/O	AJ14	682
I/O	AH14	685
I/O	AK14	688
I/O	AL13	691
I/O	AK13	694
VCC	VCC*	-
GND	GND*	697
I/O	AJ13	700
I/O	AH13	703
I/O	AL12	706
I/O	AK12	709
I/O	AJ12	712
I/O	AK11	715
GND	GND*	-
I/O	AH12	718
I/O	AJ11	721
VCC	VCC*	-
I/O	AL10	724
I/O	AK10	727
I/O	AJ10	730
I/O	AK9	733
GND	GND*	-
I/O	AL8	736
I/O	AH10	739
I/O	AJ9	742
I/O	AK8	745
GND	GND*	-
I/O	AJ8	748
I/O	AH9	751

XC4052XL Pad Name	BG432	Bndry Scan
I/O	AK7	754
I/O	AL6	757
I/O	AJ7	760
I/O	AH8	763
GND	GND*	-
VCC	VCC*	-
I/O	AK6	766
I/O	AL5	769
I/O	AH7	772
I/O	AJ6	775
I/O	AK5	778
I/O	AL4	781
GND	GND*	-
I/O	AH6	784
I/O	AJ5	787
I/O	AK4	790
I/O	AH5	793
I/O	AK3	796
I/O, GCK4	AJ4	799
GND	GND*	-
DONE	AH4	-
VCC	VCC*	-
$\overline{\text{PROGRAM}}$	AH3	-
I/O (D7)	AJ2	802
I/O, GCK5	AG4	805
I/O	AG3	808
I/O	AH2	811
I/O	AH1	814
I/O	AF4	817
GND	GND*	-
I/O	AF3	820
I/O	AG2	823
I/O	AG1	826
I/O	AE4	829
I/O	AE3	832
I/O	AF2	835
VCC	VCC*	-
GND	GND*	-
I/O (D6)	AF1	838
I/O	AD4	841
I/O	AD3	844
I/O	AE2	847
I/O	AD2	850
I/O	AC4	853
GND	GND*	-
I/O	AC3	856
I/O	AD1	859
I/O	AC2	862
I/O	AB4	865
GND	GND*	-
I/O	AB3	868
I/O	AB2	871

XC4052XL Pad Name	BG432	Bndry Scan
I/O, FCLK3	AB1	874
I/O	AA3	877
VCC	VCC*	-
I/O (D5)	AA2	880
I/O ($\overline{\text{CS0}}$)	Y2	883
GND	GND*	-
I/O	Y4	886
I/O	Y3	889
I/O	Y1	892
I/O	W1	895
I/O	W4	898
I/O	W3	901
GND	GND*	-
VCC	VCC*	-
I/O	W2	904
I/O	V2	907
I/O	V4	910
I/O	V3	913
I/O	U1	916
I/O	U2	919
GND	GND*	-
I/O	U4	922
I/O	U3	925
I/O (D4)	T1	928
I/O	T2	931
VCC	VCC*	-
GND	GND*	-
I/O (D3)	T3	934
I/O ($\overline{\text{RS}}$)	R1	937
I/O	R2	940
I/O	R4	943
GND	GND*	-
I/O	R3	946
I/O	P2	949
I/O	P3	952
I/O	P4	955
I/O	N1	958
I/O	N2	961
VCC	VCC*	-
GND	GND*	-
I/O	N3	964
I/O	N4	967
I/O	M1	970
I/O	M2	973
I/O	M3	976
I/O	M4	979
GND	GND*	-
I/O (D2)	L2	982
I/O	L3	985
VCC	VCC*	-
I/O	K1	988
I/O, FCLK4	K2	991

XC4052XL Pad Name	BG432	Bndry Scan
I/O	K3	994
I/O	K4	997
GND	GND*	-
I/O	J2	1000
I/O	J3	1003
I/O	J4	1006
I/O	H1	1009
GND	GND*	-
I/O	H2	1012
I/O	H3	1015
I/O	H4	1018
I/O	G2	1021
I/O	G3	1024
I/O	F1	1027
GND	GND*	-
VCC	VCC*	-
I/O (D1)	G4	1030
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	F2	1033
I/O	F3	1036
I/O	E1	1039
I/O	F4	1042
I/O	E2	1045
GND	GND*	-
I/O	E3	1048
I/O	D1	1051
I/O	E4	1054
I/O	D2	1057
I/O (D0, DIN)	C2	1060
I/O, GCK6 (DOUT)	D3	1063
CCLK	D4	-
VCC	VCC*	-
O, TDO	C4	0
GND	GND*	-
I/O (A0, $\overline{WS}$)	B3	2
I/O, GCK7 (A1)	D5	5
I/O	B4	8
I/O	C5	11
I/O	A4	14
I/O	D6	17
GND	GND*	-
I/O	B5	20
I/O	C6	23
I/O (CS1, A2)	A5	26
I/O (A3)	D7	29
I/O	B6	32
I/O	A6	35
VCC	VCC*	-
GND	GND*	-
I/O	D8	38
I/O	C7	41
I/O	B7	44
I/O	D9	47

XC4052XL Pad Name	BG432	Bndry Scan
I/O	B8	50
I/O	A8	53
GND	GND*	-
I/O	D10	56
I/O	C9	59
I/O	B9	62
I/O	C10	65
GND	GND*	-
I/O	B10	68
I/O	A10	71
I/O	C11	74
I/O	D12	77
VCC	VCC*	-
I/O	B11	80
I/O	C12	83
GND	GND*	-
I/O	D13	86
I/O	B12	89
I/O	C13	92
I/O	A12	95
I/O	D14	98
I/O	B13	101
GND	GND*	-
VCC	VCC*	-
I/O (A4)	C14	104
I/O (A5)	A13	107
I/O	B14	110
I/O	D15	113
I/O (A21)	C15	116
I/O (A20)	B15	119
GND	GND*	-
I/O	A15	122
I/O	C16	125
I/O (A6)	B16	128
I/O (A7)	A16	131
GND	GND*	-
VCC	VCC*	-
I/O (A8)	D17	134
I/O (A9)	A17	137
I/O	C17	140
I/O	B17	143
GND	GND*	-
I/O (A19)	C18	146
I/O (A18)	D18	149
I/O	B18	152
I/O	A19	155
I/O (A10)	B19	158
I/O (A11)	C19	161
VCC	VCC*	-
GND	GND*	-
I/O	D19	164
I/O	A20	167

XC4052XL Pad Name	BG432	Bndry Scan
I/O	B20	170
I/O	C20	173
I/O	B21	176
I/O	D20	179
GND	GND*	-
I/O	C21	182
I/O	A22	185
VCC	VCC*	-
I/O	B22	188
I/O	C22	191
I/O	B23	194
I/O	A24	197
GND	GND*	-
I/O	D22	200
I/O	C23	203
I/O	B24	206
I/O	C24	209
GND	GND*	-
I/O	D23	212
I/O	B25	215
I/O	A26	218
I/O	C25	221
I/O (A12)	D24	224
I/O (A13)	B26	227
GND	GND*	-
VCC	VCC*	-
I/O	A27	230
I/O	D25	233
I/O	C26	236
I/O	B27	239
I/O	A28	242
I/O	D26	245
GND	GND*	-
I/O	C27	248
I/O	B28	251
I/O	D27	254
I/O	B29	257
I/O (A14)	C28	260
I/O, GCK8 (A15)	D28	263
VCC	VCC*	-

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Pads labelled GND* are internally bonded to a Ground plane within the associated package. They have no direct connection to any package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the associated package. They have no direct connection to any package pin.

Additional No Connect, Vcc & Ground Connections on BG432 Package

N.C.	VCC	GND
C8	A1	A2
	A11	A3
	A21	A7
	A31	A9
	C3	A14
	C29	A18
	D11	A23
	D21	A25
	L1	A29
	L4	A30
	L28	B1
	L31	B2
	AA1	B30
	AA4	B31
	AA28	C1
	AA31	C31
	AH11	D16
	AH21	G1
	AJ3	G31
	AJ29	J1
	AL1	J31
	AL11	P1
	AL21	P31
	AL31	T4
		T28
		V1
		V31
		AC1
		AC31
		AE1
		AE31
		AH16
		AJ1
		AJ31
		AK1
		AK2
		AK30
		AK31
		AL2
		AL3
		AL7
		AL9
		AL14
		AL18
		AL23
		AL25
		AL29
		AL30

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Package-Specific Pinout Tables

PC84 Package Pinouts

Pin	XC4003E	XC4005E XC4005L	XC4006E	XC4008E	XC4010E XC4010L
P1	GND	GND	GND	GND	GND
P2	VCC	VCC	VCC	VCC	VCC
P3	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
P4	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
P5	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
P6	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
P7	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
P8	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
P9	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
P10	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P11	VCC	VCC	VCC	VCC	VCC
P12	GND	GND	GND	GND	GND
P13	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P14	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P15	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P16	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P17	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P18	I/O	I/O	I/O	I/O	I/O
P19	I/O	I/O	I/O	I/O	I/O
P20	I/O	I/O	I/O	I/O	I/O
P21	GND	GND	GND	GND	GND
P22	VCC	VCC	VCC	VCC	VCC
P23	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O	I/O
P26	I/O	I/O	I/O	I/O	I/O
P27	I/O	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O	I/O
P29	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2
P30	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
P31	GND	GND	GND	GND	GND
P32	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)
P33	VCC	VCC	VCC	VCC	VCC
P34	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)
P35	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2
P36	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P37	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P38	I/O	I/O	I/O	I/O	I/O
P39	I/O	I/O	I/O	I/O	I/O
P40	I/O	I/O	I/O	I/O	I/O
P41	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P42	VCC	VCC	VCC	VCC	VCC
P43	GND	GND	GND	GND	GND
P44	I/O	I/O	I/O	I/O	I/O
P45	I/O	I/O	I/O	I/O	I/O
P46	I/O	I/O	I/O	I/O	I/O
P47	I/O	I/O	I/O	I/O	I/O
P48	I/O	I/O	I/O	I/O	I/O
P49	I/O	I/O	I/O	I/O	I/O
P50	I/O	I/O	I/O	I/O	I/O
P51	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3
P52	GND	GND	GND	GND	GND
P53	DONE	DONE	DONE	DONE	DONE
P54	VCC	VCC	VCC	VCC	VCC
P55	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$
P56	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P57	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3
P58	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P59	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P60	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P61	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P62	I/O	I/O	I/O	I/O	I/O
P63	VCC	VCC	VCC	VCC	VCC
P64	GND	GND	GND	GND	GND
P65	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P66	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P67	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P68	I/O	I/O	I/O	I/O	I/O
P69	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P70	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)
P71	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P72	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P73	CCLK	CCLK	CCLK	CCLK	CCLK
P74	VCC	VCC	VCC	VCC	VCC
P75	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
P76	GND	GND	GND	GND	GND
P77	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
P78	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P79	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P80	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P81	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
P82	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
P83	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
P84	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)

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PQ100 Package Pinouts

PQ100 Pin	XC4003E	XC4005E
P1	I/O (A14)	I/O (A14)
P2	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P3	VCC	VCC
P4	GND	GND
P5	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P6	I/O (A17)	I/O (A17)
P7	I/O, TDI	I/O, TDI
P8	I/O, TCK	I/O, TCK
P9	I/O, TMS	I/O, TMS
P10	I/O	I/O
P11	I/O	I/O
P12	I/O	I/O
P13	I/O	I/O
P14	GND	GND
P15	VCC	VCC
P16	I/O	I/O
P17	I/O	I/O
P18	I/O	I/O
P19	I/O	I/O
P20	I/O	I/O
P21	I/O	I/O
P22	I/O	I/O
P23	I/O	I/O
P24	I/O, SCGK2	I/O, SCGK2
P25	O (M1)	O (M1)
P26	GND	GND
P27	I (M0)	I (M0)
P28	VCC	VCC
P29	I (M2)	I (M2)
P30	I/O, PGCK2	I/O, PGCK2
P31	I/O (HDC)	I/O (HDC)
P32	I/O	I/O
P33	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P34	I/O	I/O
P35	I/O	I/O
P36	I/O	I/O
P37	I/O	I/O
P38	I/O	I/O
P39	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P40	VCC	VCC
P41	GND	GND
P42	I/O	I/O
P43	I/O	I/O
P44	I/O	I/O
P45	I/O	I/O
P46	I/O	I/O
P47	I/O	I/O
P48	I/O	I/O
P49	I/O	I/O
P50	I/O	I/O
P51	I/O, SGCK3	I/O, SGCK3
P52	GND	GND
P53	DONE	DONE
P54	VCC	VCC
P55	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
P56	I/O (D7)	I/O (D7)
P57	I/O, PGCK3	I/O, PGCK3
P58	I/O (D6)	I/O (D6)
P59	I/O	I/O
P60	I/O (D5)	I/O (D5)
P61	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P62	I/O	I/O
P63	I/O	I/O
P64	I/O (D4)	I/O (D4)
P65	I/O	I/O
P66	VCC	VCC
P67	GND	GND
P68	I/O (D3)	I/O (D3)
P69	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P70	I/O	I/O
P71	I/O (D2)	I/O (D2)
P72	I/O	I/O
P73	I/O (D1)	I/O (D1)
P74	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)
P75	I/O (D0, DIN)	I/O (D0, DIN)
P76	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P77	CCLK	CCLK
P78	VCC	VCC
P79	O, TDO	O, TDO
P80	GND	GND
P81	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
P82	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P83	I/O (CS1, A2)	I/O (CS1, A2)
P84	I/O (A3)	I/O (A3)
P85	I/O (A4)	I/O (A4)
P86	I/O (A5)	I/O (A5)
P87	I/O	I/O
P88	I/O	I/O
P89	I/O (A6)	I/O (A6)
P90	I/O (A7)	I/O (A7)
P91	GND	GND
P92	VCC	VCC
P93	I/O (A8)	I/O (A8)
P94	I/O (A9)	I/O (A9)
P95	I/O	I/O
P96	I/O	I/O
P97	I/O (A10)	I/O (A10)
P98	I/O (A11)	I/O (A11)
P99	I/O (A12)	I/O (A12)
P100	I/O (A13)	I/O (A13)

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VQ100 Package Pinouts

VQ100 Pin	XC4003E
P1	GND
P2	I/O, PGCK1 (A16)
P3	I/O (A17)
P4	I/O, TDI
P5	I/O, TCK
P6	I/O, TMS
P7	I/O
P8	I/O
P9	I/O
P10	I/O
P11	GND
P12	VCC
P13	I/O
P14	I/O
P15	I/O
P16	I/O
P17	I/O
P18	I/O
P19	I/O
P20	I/O
P21	I/O, SCGK2
P22	O (M1)
P23	GND
P24	I (M0)
P25	VCC
P26	I (M2)
P27	I/O, PGCK2
P28	I/O (HDC)
P29	I/O
P30	I/O ($\overline{\text{LDC}}$)
P31	I/O
P32	I/O
P33	I/O
P34	I/O
P35	I/O
P36	I/O ($\overline{\text{INIT}}$)
P37	VCC
P38	GND
P39	I/O
P40	I/O
P41	I/O
P42	I/O
P43	I/O
P44	I/O
P45	I/O
P46	I/O
P47	I/O
P48	I/O, SGCK3
P49	GND
P50	DONE
P51	VCC
P52	$\overline{\text{PROGRAM}}$
P53	I/O (D7)
P54	I/O, PGCK3
P55	I/O (D6)
P56	I/O
P57	I/O (D5)
P58	I/O ($\overline{\text{CS0}}$)
P59	I/O
P60	I/O
P61	I/O (D4)
P62	I/O
P63	VCC
P64	GND
P65	I/O (D3)
P66	I/O ($\overline{\text{RS}}$)
P67	I/O
P68	I/O (D2)
P69	I/O
P70	I/O (D1)
P71	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)
P72	I/O (D0, DIN)
P73	I/O, SGCK4 (DOUT)
P74	CCLK
P75	VCC
P76	O, TDO
P77	GND
P78	I/O (A0, $\overline{\text{WS}}$)
P79	I/O, PGCK4 (A1)
P80	I/O (CS1, A2)
P81	I/O (A3)
P82	I/O (A4)
P83	I/O (A5)
P84	I/O
P85	I/O
P86	I/O (A6)
P87	I/O (A7)
P88	GND
P89	VCC
P90	I/O (A8)
P91	I/O (A9)
P92	I/O
P93	I/O
P94	I/O (A10)
P95	I/O (A11)
P96	I/O (A12)
P97	I/O (A13)
P98	I/O (A14)
P99	I/O, SGCK1 (A15)
P100	VCC

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PG120 Package Pinouts

PG120 Pin	XC4003E
N13	I/O, PGCK3
N12	N.C.
N11	I/O
N10	I/O ($\overline{CS0}$)
N9	I/O
N8	I/O
N7	I/O (D3)
N6	I/O ($\overline{RS}$)
N5	I/O
N4	I/O
N3	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
N2	I/O (D0, DIN)
N1	I/O, PGCK4 (A1)
M13	I/O
M12	$\overline{PROGRAM}$
M11	I/O (D7)
M10	I/O (D6)
M9	I/O (D5)
M8	I/O (D4)
M7	VCC
M6	I/O
M5	I/O (D1)
M4	N.C.
M3	I/O, SGCK4 (DOUT)
M2	O, TDO
M1	N.C.
L13	I/O
L12	I/O, SGCK3
L11	DONE
L10	VCC
L9	N.C.
L8	I/O
L7	GND
L6	I/O (D2)
L5	N.C.
L4	CCLK
L3	VCC
L2	I/O (A0, $\overline{WS}$)
L1	I/O (A3)
K13	I/O
K12	N.C.
K11	GND
K3	GND
K2	I/O (CS1, A2)
K1	I/O (A5)
J13	I/O
J12	I/O
J11	N.C.
J3	N.C.
J2	I/O (A4)
J1	I/O
H13	I/O
H12	I/O
H11	I/O
H3	I/O
H2	I/O (A6)
H1	I/O (A7)
G13	I/O
G12	VCC
G11	GND
G3	VCC
G2	GND
G1	I/O (A8)
F13	I/O ($\overline{INIT}$)
F12	I/O
F11	I/O
F3	I/O (A10)
F2	I/O
F1	I/O (A9)
E13	I/O
E12	I/O
E11	N.C.
E3	N.C.
E2	N.C.
E1	I/O
D13	I/O
D12	I/O
D11	VCC
D3	I/O, SGCK1 (A15)
D2	I/O (A13)
D1	I/O (A11)
C13	I/O ($\overline{LDC}$)
C12	I/O, PGCK2
C11	I (M0)
C10	GND
C9	I/O
C8	I/O
C7	VCC
C6	I/O
C5	I/O, TDI
C4	GND
C3	VCC
C2	I/O (A14)
C1	I/O (A12)

PG120 Pin	XC4003E
B13	N.C.
B12	I (M2)
B11	O (M1)
B10	N.C.
B9	I/O
B8	I/O
B7	GND
B6	I/O
B5	I/O, TMS
B4	I/O, TCK
B3	I/O (A17)
B2	I/O, PGCK1 (A16)
B1	N.C.
A13	I/O (HDC)
A12	I/O, SCGK2
A11	I/O
A10	I/O
A9	I/O
A8	I/O
A7	I/O
A6	I/O
A5	I/O
A4	I/O
A3	N.C.
A2	N.C.
A1	N.C.

3/13/96

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

TQ144 Package Pinouts

TQ144 Pin	XC4005E	XC4006E
P1	GND	GND
P2	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P3	I/O (A17)	I/O (A17)
P4	I/O	I/O
P5	I/O	I/O
P6	I/O, TDI	I/O, TDI
P7	I/O, TCK	I/O, TCK
P8	GND	GND
P9	I/O	I/O
P10	I/O	I/O
P11	I/O, TMS	I/O, TMS
P12	I/O	I/O
P13	I/O	I/O
P14	I/O	I/O
P15	I/O	I/O
P16	I/O	I/O
P17	GND	GND
P18	VCC	VCC
P19	I/O	I/O
P20	I/O	I/O
P21	I/O	I/O
P22	I/O	I/O
P23	I/O	I/O
P24	I/O	I/O
P25	I/O	I/O
P26	I/O	I/O
P27	GND	GND
P28	I/O	I/O
P29	I/O	I/O
P30	I/O	I/O
P31	I/O	I/O
P32	I/O	I/O
P33	I/O, SCGK2	I/O, SCGK2
P34	O (M1)	O (M1)
P35	GND	GND
P36	I (M0)	I (M0)
P37	VCC	VCC
P38	I (M2)	I (M2)
P39	I/O, PGCK2	I/O, PGCK2
P40	I/O (HDC)	I/O (HDC)
P41	I/O	I/O
P42	I/O	I/O
P43	I/O	I/O
P44	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P45	GND	GND
P46	I/O	I/O
P47	I/O	I/O
P48	I/O	I/O
P49	I/O	I/O
P50	I/O	I/O
P51	I/O	I/O
P52	I/O	I/O
P53	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P54	VCC	VCC
P55	GND	GND
P56	I/O	I/O
P57	I/O	I/O
P58	I/O	I/O
P59	I/O	I/O
P60	I/O	I/O
P61	I/O	I/O
P62	I/O	I/O
P63	I/O	I/O
P64	GND	GND
P65	I/O	I/O
P66	I/O	I/O
P67	I/O	I/O
P68	I/O	I/O
P69	I/O	I/O
P70	I/O, SGCK3	I/O, SGCK3
P71	GND	GND
P72	DONE	DONE
P73	VCC	VCC
P74	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
P75	I/O (D7)	I/O (D7)
P76	I/O, PGCK3	I/O, PGCK3
P77	I/O	I/O
P78	I/O	I/O
P79	I/O (D6)	I/O (D6)
P80	I/O	I/O
P81	GND	GND
P82	I/O	I/O
P83	I/O	I/O
P84	I/O (D5)	I/O (D5)
P85	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P86	I/O	I/O
P87	I/O	I/O
P88	I/O (D4)	I/O (D4)
P89	I/O	I/O
P90	VCC	VCC
P91	GND	GND
P92	I/O (D3)	I/O (D3)
P93	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P94	I/O	I/O

TQ144 Pin	XC4005E	XC4006E
P95	I/O	I/O
P96	I/O (D2)	I/O (D2)
P97	I/O	I/O
P98	I/O	I/O
P99	I/O	I/O
P100	GND	GND
P101	I/O (D1)	I/O (D1)
P102	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)
P103	I/O	I/O
P104	I/O	I/O
P105	I/O (D0, DIN)	I/O (D0, DIN)
P106	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P107	CCLK	CCLK
P108	VCC	VCC
P109	O, TDO	O, TDO
P110	GND	GND
P111	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
P112	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P113	I/O	I/O
P114	I/O	I/O
P115	I/O (CS1, A2)	I/O (CS1, A2)
P116	I/O (A3)	I/O (A3)
P117	N.C.	I/O
P118	GND	GND
P119	I/O	I/O
P120	I/O	I/O
P121	I/O (A4)	I/O (A4)
P122	I/O (A5)	I/O (A5)
P123	I/O	I/O
P124	I/O	I/O
P125	I/O (A6)	I/O (A6)
P126	I/O (A7)	I/O (A7)
P127	GND	GND
P128	VCC	VCC
P129	I/O (A8)	I/O (A8)
P130	I/O (A9)	I/O (A9)
P131	I/O	I/O
P132	I/O	I/O
P133	I/O (A10)	I/O (A10)
P134	I/O (A11)	I/O (A11)
P135	I/O	I/O
P136	I/O	I/O
P137	GND	GND
P138	I/O (A12)	I/O (A12)
P139	I/O (A13)	I/O (A13)
P140	I/O	I/O
P141	I/O	I/O
P142	I/O (A14)	I/O (A14)
P143	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P144	VCC	VCC

2/28/96

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

PG156 Package Pinouts

PG156 Pin	XC4005E	XC4006E
T1	O, TDO	O, TDO
T2	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
T3	I/O (D1)	I/O (D1)
T4	I/O	I/O
T5	I/O	I/O
T6	I/O	I/O
T7	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
T8	I/O (D3)	I/O (D3)
T9	I/O	I/O
T10	I/O (D5)	I/O (D5)
T11	I/O	I/O
T12	N.C.	I/O
T13	I/O	I/O
T14	I/O (D6)	I/O (D6)
T15	I/O, PGCK3	I/O, PGCK3
T16	I/O (D7)	I/O (D7)
R1	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
R2	CCLK	CCLK
R3	I/O	I/O
R4	I/O	I/O
R5	N.C.	I/O
R6	I/O	I/O
R7	I/O	I/O
R8	VCC	VCC
R9	I/O (D4)	I/O (D4)
R10	I/O	I/O
R11	I/O	I/O
R12	N.C.	I/O
R13	I/O	I/O
R14	$\overline{PROGRAM}$	$\overline{PROGRAM}$
R15	DONE	DONE
R16	I/O, SGCK3	I/O, SGCK3
P1	I/O (CS1, A2)	I/O (CS1, A2)
P2	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P3	VCC	VCC
P4	I/O (D0, DIN)	I/O (D0, DIN)
P5	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
P6	GND	GND
P7	I/O (D2)	I/O (D2)
P8	GND	GND
P9	I/O	I/O
P10	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
P11	GND	GND
P12	I/O	I/O
P13	VCC	VCC
P14	GND	GND
P15	I/O	I/O
P16	I/O	I/O
N1	I/O (A3)	I/O (A3)
N2	I/O	I/O
N3	GND	GND
N14	I/O	I/O
N15	I/O	I/O
N16	N.C.	I/O
M1	N.C.	I/O
M2	N.C.	I/O
M3	I/O	I/O
M14	I/O	I/O
M15	N.C.	I/O
M16	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O
L3	GND	GND
L14	GND	GND
L15	I/O	I/O
L16	I/O	I/O
K1	I/O	I/O
K2	I/O (A5)	I/O (A5)
K3	I/O (A4)	I/O (A4)
K14	I/O	I/O
K15	I/O	I/O
K16	I/O	I/O
J1	I/O	I/O
J2	I/O (A6)	I/O (A6)
J3	I/O (A7)	I/O (A7)
J14	GND	GND
J15	I/O	I/O
J16	I/O	I/O
H1	I/O (A8)	I/O (A8)
H2	GND	GND
H3	VCC	VCC
H14	VCC	VCC
H15	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
H16	I/O	I/O
G1	I/O (A9)	I/O (A9)
G2	I/O	I/O
G3	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
G16	I/O	I/O
F1	I/O (A10)	I/O (A10)
F2	I/O (A11)	I/O (A11)
F3	GND	GND

PG156 Pin	XC4005E	XC4006E
F14	GND	GND
F15	I/O	I/O
F16	I/O	I/O
E1	I/O	I/O
E2	I/O	I/O
E3	I/O (A12)	I/O (A12)
E14	I/O	I/O
E15	N.C.	I/O
E16	I/O	I/O
D1	N.C.	I/O
D2	N.C.	I/O
D3	I/O	I/O
D14	I/O (HDC)	I/O (HDC)
D15	I/O	I/O
D16	N.C.	I/O
C1	I/O (A13)	I/O (A13)
C2	I/O	I/O
C3	VCC	VCC
C4	GND	GND
C5	I/O	I/O
C6	GND	GND
C7	I/O	I/O
C8	GND	GND
C9	I/O	I/O
C10	I/O	I/O
C11	GND	GND
C12	I/O	I/O
C13	GND	GND
C14	VCC	VCC
C15	I/O	I/O
C16	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
B1	I/O (A14)	I/O (A14)
B2	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
B3	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
B4	I/O, TDI	I/O, TDI
B5	I/O	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	VCC	VCC
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O, SCGK2	I/O, SCGK2
B15	I (M2)	I (M2)
B16	I/O, PGCK2	I/O, PGCK2
A1	I/O (A17)	I/O (A17)
A2	I/O	I/O
A3	I/O, TCK	I/O, TCK
A4	N.C.	I/O
A5	I/O, TMS	I/O, TMS
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	N.C.	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	O (M1)	O (M1)
A16	I (M0)	I (M0)

2/28/96

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

PQ160 Package Pinouts

PQ 160 Pin	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E
P1	GND	GND	GND	GND	GND
P2	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P3	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P4	I/O	I/O	I/O	I/O	I/O
P5	I/O	I/O	I/O	I/O	I/O
P6	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P7	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P8	N.C.	I/O	I/O	I/O	I/O
P9	N.C.	I/O	I/O	I/O	I/O
P10	GND	GND	GND	GND	GND
P11	I/O	I/O	I/O	I/O	I/O
P12	I/O	I/O	I/O	I/O	I/O
P13	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P14	I/O	I/O	I/O	I/O	I/O
P15	I/O	I/O	I/O	I/O	I/O
P16	I/O	I/O	I/O	I/O	I/O
P17	I/O	I/O	I/O	I/O	I/O
P18	I/O	I/O	I/O	I/O	I/O
P19	GND	GND	GND	GND	GND
P20	VCC	VCC	VCC	VCC	VCC
P21	I/O	I/O	I/O	I/O	I/O
P22	I/O	I/O	I/O	I/O	I/O
P23	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O	I/O
P26	I/O	I/O	I/O	I/O	I/O
P27	I/O	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O	I/O
P29	GND	GND	GND	GND	GND
P30	N.C.	I/O	I/O	I/O	I/O
P31	N.C.	I/O	I/O	I/O	I/O
P32	I/O	I/O	I/O	I/O	I/O
P33	I/O	I/O	I/O	I/O	I/O
P34	I/O	I/O	I/O	I/O	I/O
P35	I/O	I/O	I/O	I/O	I/O
P36	I/O	I/O	I/O	I/O	I/O
P37	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2
P38	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
P39	GND	GND	GND	GND	GND
P40	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)
P41	VCC	VCC	VCC	VCC	VCC
P42	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)
P43	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2
P44	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P45	I/O	I/O	I/O	I/O	I/O
P46	I/O	I/O	I/O	I/O	I/O
P47	I/O	I/O	I/O	I/O	I/O
P48	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P49	N.C.	I/O	I/O	I/O	I/O
P50	N.C.	I/O	I/O	I/O	I/O
P51	GND	GND	GND	GND	GND
P52	I/O	I/O	I/O	I/O	I/O
P53	I/O	I/O	I/O	I/O	I/O
P54	I/O	I/O	I/O	I/O	I/O
P55	I/O	I/O	I/O	I/O	I/O
P56	I/O	I/O	I/O	I/O	I/O
P57	I/O	I/O	I/O	I/O	I/O
P58	I/O	I/O	I/O	I/O	I/O
P59	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P60	VCC	VCC	VCC	VCC	VCC
P61	GND	GND	GND	GND	GND
P62	I/O	I/O	I/O	I/O	I/O
P63	I/O	I/O	I/O	I/O	I/O
P64	I/O	I/O	I/O	I/O	I/O
P65	I/O	I/O	I/O	I/O	I/O
P66	I/O	I/O	I/O	I/O	I/O
P67	I/O	I/O	I/O	I/O	I/O
P68	I/O	I/O	I/O	I/O	I/O
P69	I/O	I/O	I/O	I/O	I/O
P70	GND	GND	GND	GND	GND
P71	N.C.	I/O	I/O	I/O	I/O
P72	N.C.	I/O	I/O	I/O	I/O
P73	I/O	I/O	I/O	I/O	I/O
P74	I/O	I/O	I/O	I/O	I/O
P75	I/O	I/O	I/O	I/O	I/O
P76	I/O	I/O	I/O	I/O	I/O
P77	I/O	I/O	I/O	I/O	I/O
P78	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3
P79	GND	GND	GND	GND	GND
P80	DONE	DONE	DONE	DONE	DONE
P81	VCC	VCC	VCC	VCC	VCC
P82	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$
P83	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P84	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3
P85	I/O	I/O	I/O	I/O	I/O
P86	I/O	I/O	I/O	I/O	I/O
P87	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P88	I/O	I/O	I/O	I/O	I/O
P89	N.C.	I/O	I/O	I/O	I/O
P90	N.C.	I/O	I/O	I/O	I/O
P91	GND	GND	GND	GND	GND
P92	I/O	I/O	I/O	I/O	I/O
P93	I/O	I/O	I/O	I/O	I/O
P94	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P95	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)

PQ 160 Pin	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E
P96	I/O	I/O	I/O	I/O	I/O
P97	I/O	I/O	I/O	I/O	I/O
P98	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P99	I/O	I/O	I/O	I/O	I/O
P100	VCC	VCC	VCC	VCC	VCC
P101	GND	GND	GND	GND	GND
P102	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P103	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
P104	I/O	I/O	I/O	I/O	I/O
P105	I/O	I/O	I/O	I/O	I/O
P106	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P107	I/O	I/O	I/O	I/O	I/O
P108	I/O	I/O	I/O	I/O	I/O
P109	I/O	I/O	I/O	I/O	I/O
P110	GND	GND	GND	GND	GND
P111	N.C.	I/O	I/O	I/O	I/O
P112	N.C.	I/O	I/O	I/O	I/O
P113	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P114	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)
P115	I/O	I/O	I/O	I/O	I/O
P116	I/O	I/O	I/O	I/O	I/O
P117	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P118	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P119	CCLK	CCLK	CCLK	CCLK	CCLK
P120	VCC	VCC	VCC	VCC	VCC
P121	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
P122	GND	GND	GND	GND	GND
P123	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
P124	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P125	I/O	I/O	I/O	I/O	I/O
P126	I/O	I/O	I/O	I/O	I/O
P127	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P128	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P129	N.C.	I/O	I/O	I/O	I/O
P130	N.C.	I/O	I/O	I/O	I/O
P131	GND	GND	GND	GND	GND
P132	I/O	I/O	I/O	I/O	I/O
P133	I/O	I/O	I/O	I/O	I/O
P134	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
P135	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
P136	N.C.	N.C.	I/O	I/O	I/O
P137	I/O	I/O	I/O	I/O	I/O
P138	I/O	I/O	I/O	I/O	I/O
P139	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
P140	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)
P141	GND	GND	GND	GND	GND
P142	VCC	VCC	VCC	VCC	VCC
P143	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
P144	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
P145	I/O	I/O	I/O	I/O	I/O
P146	I/O	I/O	I/O	I/O	I/O
P147	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
P148	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
P149	I/O	I/O	I/O	I/O	I/O
P150	I/O	I/O	I/O	I/O	I/O
P151	GND	GND	GND	GND	GND
P152	N.C.	I/O	I/O	I/O	I/O
P153	N.C.	I/O	I/O	I/O	I/O
P154	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
P155	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
P156	I/O	I/O	I/O	I/O	I/O
P157	I/O	I/O	I/O	I/O	I/O
P158	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
P159	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P160	VCC	VCC	VCC	VCC	VCC

2/28/96

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

TQ176 Package Pinouts

TQ176 Pin	XC4010L
P1	GND
P2	I/O, PGCK1 (A16)
P3	I/O (A17)
P4	I/O
P5	I/O
P6	I/O, TDI
P7	I/O, TCK
P8	I/O
P9	I/O
P10	GND
P11	I/O
P12	I/O
P13	I/O, TMS
P14	I/O
P15	I/O
P16	I/O
P17	I/O
P18	I/O
P19	I/O
P20	I/O
P21	GND
P22	VCC
P23	I/O
P24	I/O
P25	I/O
P26	I/O
P27	I/O
P28	I/O
P29	I/O
P30	I/O
P31	I/O
P32	I/O
P33	GND
P34	I/O
P35	I/O
P36	I/O
P37	I/O
P38	I/O
P39	I/O
P40	I/O
P41	I/O, SCGK2
P42	O (M1)
P43	GND
P44	I (M0)
P45	VCC
P46	I (M2)
P47	I/O, PGCK2
P48	I/O (HDC)
P49	I/O
P50	I/O
P51	I/O
P52	I/O ($\overline{\text{LDC}}$)
P53	I/O
P54	I/O
P55	GND
P56	I/O
P57	I/O
P58	I/O
P59	I/O
P60	I/O
P61	I/O
P62	I/O
P63	I/O
P64	I/O
P65	I/O ($\overline{\text{INIT}}$)
P66	VCC
P67	GND
P68	I/O
P69	I/O
P70	I/O
P71	I/O
P72	I/O
P73	I/O
P74	I/O
P75	I/O
P76	I/O
P77	I/O
P78	GND
P79	I/O
P80	I/O
P81	I/O
P82	I/O
P83	I/O
P84	I/O
P85	I/O
P86	I/O, SGCK3
P87	GND
P88	DONE
P89	VCC
P90	$\overline{\text{PROGRAM}}$
P91	I/O (D7)
P92	I/O, PGCK3
P93	I/O
P94	I/O

TQ176 Pin	XC4010L
P95	I/O (D6)
P96	I/O
P97	I/O
P98	I/O
P99	GND
P100	I/O
P101	I/O
P102	I/O (D5)
P103	I/O ($\overline{CS0}$)
P104	I/O
P105	I/O
P106	I/O
P107	I/O
P108	I/O (D4)
P109	I/O
P110	VCC
P111	GND
P112	I/O (D3)
P113	I/O ($\overline{RS}$)
P114	I/O
P115	I/O
P116	I/O
P117	I/O
P118	I/O (D2)
P119	I/O
P120	I/O
P121	I/O
P122	GND
P123	I/O
P124	I/O
P125	I/O (D1)
P126	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
P127	I/O
P128	I/O
P129	I/O (D0, DIN)
P130	I/O, SGCK4 (DOUT)
P131	CCLK
P132	VCC
P133	O, TDO
P134	GND
P135	I/O (A0, $\overline{WS}$)
P136	I/O, PGCK4 (A1)
P137	I/O
P138	I/O
P139	I/O (CS1, A2)
P140	I/O (A3)
P141	I/O
P142	I/O
P143	GND
P144	I/O
P145	I/O
P146	I/O (A4)
P147	I/O (A5)
P148	I/O
P149	I/O
P150	I/O
P151	I/O
P152	I/O (A6)
P153	I/O (A7)
P154	GND
P155	VCC
P156	I/O (A8)
P157	I/O (A9)
P158	I/O
P159	I/O
P160	I/O
P161	I/O
P162	I/O (A10)
P163	I/O (A11)
P164	I/O
P165	I/O
P166	GND
P167	I/O
P168	I/O
P169	I/O
P170	I/O (A12)
P171	I/O (A13)
P172	I/O
P173	I/O
P174	I/O (A14)
P175	I/O, SGCK1 (A15)
P176	VCC

3/15/96

PG191 Package Pinouts (see PG223)

The PG191 package pinout has been combined with the PG223 in a single table, because of their physical compatibility. The PG191 has the same dimensions as the PG223, but has 32 fewer pins on the inner ring.

PQ208, HQ208 Package Pinouts

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P1	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P2	GND	GND	GND	GND	GND	GND	GND
P3	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P4	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, GCK1 (A16)
P5	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P6	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P7	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P8	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P9	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P10	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P11	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P12	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P13	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P14	GND	GND	GND	GND	GND	GND	GND
P15	I/O	I/O	I/O	I/O	I/O	I/O	I/O, FCLK1
P16	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P17	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P18	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P19	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P20	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P21	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P22	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P23	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P25	GND	GND	GND	GND	GND	GND	GND
P26	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P27	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P29	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P30	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P31	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P32	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P33	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P34	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P35	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P36	I/O	I/O	I/O	I/O	I/O	I/O	I/O, FCLK2
P37	GND	GND	GND	GND	GND	GND	GND
P38	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P39	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P40	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P41	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P42	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P43	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P44	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P45	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P46	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P47	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, GCK2
P48	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
P49	GND	GND	GND	GND	GND	GND	GND
P50	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)
P51	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P52	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P53	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P54	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P55	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P56	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)
P57	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, GCK3
P58	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P59	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P60	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P61	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P62	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P63	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P64	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P65	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P66	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P67	GND	GND	GND	GND	GND	GND	GND
P68	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P69	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P70	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P71	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P72	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P73	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P74	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P75	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P76	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P77	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P78	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P79	GND	GND	GND	GND	GND	GND	GND
P80	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P81	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P82	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P83	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P84	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P85	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P86	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P87	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P88	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P89	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P90	GND	GND	GND	GND	GND	GND	GND
P91	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P92	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P93	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P94	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P95	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P96	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P97	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P98	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P99	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P100	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, GCK4
P101	GND	GND	GND	GND	GND	GND	GND
P102	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P103	DONE	DONE	DONE	DONE	DONE	DONE	DONE
P104	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P105	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P106	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P107	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P108	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$
P109	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P110	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, GCK5
P111	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P112	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P113	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P114	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P115	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P116	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P117	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P118	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P119	GND	GND	GND	GND	GND	GND	GND
P120	I/O	I/O	I/O	I/O	I/O	I/O	I/O, FCLK3
P121	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P122	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P123	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P124	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P125	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P126	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P127	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P128	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P129	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P130	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P131	GND	GND	GND	GND	GND	GND	GND
P132	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P133	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P134	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P135	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P136	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P137	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P138	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P139	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P140	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P141	I/O	I/O	I/O	I/O	I/O	I/O	I/O, FCLK4
P142	GND	GND	GND	GND	GND	GND	GND
P143	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P144	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P145	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P146	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P147	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P148	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)
P149	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P150	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P151	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P152	I/O, SGCK (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)
P153	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK
P154	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P155	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P156	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P157	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P158	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P159	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
P160	GND	GND	GND	GND	GND	GND	GND
P161	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
P162	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, GCK7 (A1)
P163	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P164	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P165	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P166	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P167	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P168	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P169	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P170	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P171	GND	GND	GND	GND	GND	GND	GND
P172	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P173	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P174	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
P175	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
P176	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P177	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P178	I/O	I/O	I/O	I/O	I/O	I/O	I/O (A21)
P179	I/O	I/O	I/O	I/O	I/O	I/O	I/O (A20)
P180	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
P181	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)
P182	GND	GND	GND	GND	GND	GND	GND
P183	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P184	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
P185	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
P186	I/O	I/O	I/O	I/O	I/O	I/O	I/O (A19)
P187	I/O	I/O	I/O	I/O	I/O	I/O	I/O (A18)
P188	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P189	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P190	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
P191	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
P192	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P193	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P194	GND	GND	GND	GND	GND	GND	GND
P195	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P196	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P197	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P198	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P199	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
P200	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
P201	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P202	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P203	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
P204	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, GCK8 (A15)
P205	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P206	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P207	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P208	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

PG223 and PG191 Package Pinouts

These two packages have been combined into a single table because of their physical compatibility. The PG191 has the same dimensions as the PG223, but has 32 fewer pins on the inner ring.

PG 223 Pin	PG 191 Pin	XC4008E PG191	XC4010E PG191	XC4013E PG223	XC4020E PG223	XC4025E PG223
V1	V1	CCLK	CCLK	CCLK	CCLK	CCLK
V2	V2	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)
V3	V3	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
V4	V4	N.C.	I/O	I/O	I/O	I/O
V5	V5	N.C.	I/O	I/O	I/O	I/O
V6	V6	I/O	I/O	I/O	I/O	I/O
V7	V7	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
V8	V8	I/O	I/O	I/O	I/O	I/O
V9	V9	I/O	I/O	I/O	I/O	I/O
V10	V10	I/O	I/O	I/O	I/O	I/O
V11	V11	I/O	I/O	I/O	I/O	I/O
V12	V12	I/O (CS0)	I/O (CS0)	I/O (CS0)	I/O (CS0)	I/O (CS0)
V13	V13	I/O	I/O	I/O	I/O	I/O
V14	V14	N.C.	I/O	I/O	I/O	I/O
V15	V15	N.C.	I/O	I/O	I/O	I/O
V16	V16	I/O	I/O	I/O	I/O	I/O
V17	V17	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
V18	V18	PRO-GRAM	PRO-GRAM	PRO-GRAM	PRO-GRAM	PRO-GRAM
U1	U1	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
U2	U2	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
U3	U3	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
U4	U4	I/O	I/O	I/O	I/O	I/O
U5	U5	I/O	I/O	I/O	I/O	I/O
U6	U6	I/O	I/O	I/O	I/O	I/O
U7	U7	I/O	I/O	I/O	I/O	I/O
U8	U8	I/O	I/O	I/O	I/O	I/O
U9	U9	I/O (RS)	I/O (RS)	I/O (RS)	I/O (RS)	I/O (RS)
U10	U10	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
U11	U11	I/O	I/O	I/O	I/O	I/O
U12	U12	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
U13	U13	I/O	I/O	I/O	I/O	I/O
U14	U14	I/O	I/O	I/O	I/O	I/O
U15	U15	I/O	I/O	I/O	I/O	I/O
U16	U16	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3
U17	U17	DONE	DONE	DONE	DONE	DONE
U18	U18	I/O	I/O	I/O	I/O	I/O
T1	T1	I/O	I/O	I/O	I/O	I/O
T2	T2	I/O (CS1,A2)	I/O (CS1,A2)	I/O (CS1,A2)	I/O (CS1,A2)	I/O (CS1,A2)
T3	T3	I/O (A0, WS)	I/O (A0, WS)	I/O (A0, WS)	I/O (A0, WS)	I/O (A0, WS)
T4	T4	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
T5	T5	I/O	I/O	I/O	I/O	I/O
T6	T6	I/O	I/O	I/O	I/O	I/O
T7	T7	GND	GND	GND	GND	GND
T8	T8	I/O	I/O	I/O	I/O	I/O
T9	T9	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
T10	T10	I/O	I/O	I/O	I/O	I/O
T11	T11	I/O	I/O	I/O	I/O	I/O
T12	T12	GND	GND	GND	GND	GND
T13	T13	I/O	I/O	I/O	I/O	I/O
T14	T14	I/O	I/O	I/O	I/O	I/O
T15	T15	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
T16	T16	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3
T17	T17	I/O	I/O	I/O	I/O	I/O
T18	T18	I/O	I/O	I/O	I/O	I/O
R1	R1	N.C.	I/O	I/O	I/O	I/O
R2	R2	I/O	I/O	I/O	I/O	I/O
R3	R3	GND	GND	GND	GND	GND
R4	R4	VCC	VCC	VCC	VCC	VCC
R5				I/O	I/O	I/O
R6				I/O	I/O	I/O
R7				I/O	I/O	I/O
R8				I/O	I/O	I/O
R9	R9	GND	GND	GND	GND	GND
R10	R10	VCC	VCC	VCC	VCC	VCC
R11				I/O	I/O	I/O
R12				I/O	I/O	I/O
R13				I/O	I/O	I/O
R14				I/O	I/O	I/O
R15	R15	VCC	VCC	VCC	VCC	VCC
R16	R16	GND	GND	GND	GND	GND
R17	R17	I/O	I/O	I/O	I/O	I/O
R18	R18	N.C.	I/O	I/O	I/O	I/O
P1	P1	I/O	I/O	I/O	I/O	I/O
P2	P2	I/O	I/O	I/O	I/O	I/O
P3	P3	I/O	I/O	I/O	I/O	I/O
P4				I/O	I/O	I/O
P15				I/O	I/O	I/O
P16	P16	I/O	I/O	I/O	I/O	I/O
P17	P17	I/O	I/O	I/O	I/O	I/O
P18	P18	I/O	I/O	I/O	I/O	I/O
N1	N1	I/O	I/O	I/O	I/O	I/O
N2	N2	N.C.	I/O	I/O	I/O	I/O
N3	N3	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
N4				I/O	I/O	I/O
N15				I/O	I/O	I/O
N16	N16	I/O	I/O	I/O	I/O	I/O

PG 223 Pin	PG 191 Pin	XC4008E PG191	XC4010E PG191	XC4013E PG223	XC4020E PG223	XC4025E PG223
N17	N17	N.C.	I/O	I/O	I/O	I/O
N18	N18	I/O	I/O	I/O	I/O	I/O
M1	M1	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
M2	M2	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
M3	M3	GND	GND	GND	GND	GND
M4				I/O	I/O	I/O
M15				I/O	I/O	I/O
M16	M16	GND	GND	GND	GND	GND
M17	M17	I/O	I/O	I/O	I/O	I/O
M18	M18	I/O	I/O	I/O	I/O	I/O
L1	L1	I/O	I/O	I/O	I/O	I/O
L2	L2	I/O	I/O	I/O	I/O	I/O
L3	L3	I/O	I/O	I/O	I/O	I/O
L4				I/O	I/O	I/O
L15				I/O	I/O	I/O
L16	L16	I/O	I/O	I/O	I/O	I/O
L17	L17	I/O	I/O	I/O	I/O	I/O
L18	L18	I/O	I/O	I/O	I/O	I/O
K1	K1	I/O	I/O	I/O	I/O	I/O
K2	K2	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
K3	K3	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)
K4	K4	GND	GND	GND	GND	GND
K15	K15	GND	GND	GND	GND	GND
K16	K16	I/O	I/O	I/O	I/O	I/O
K17	K17	I/O	I/O	I/O	I/O	I/O
K18	K18	I/O	I/O	I/O	I/O	I/O
J1	J1	I/O	I/O	I/O	I/O	I/O
J2	J2	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
J3	J3	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
J4	J4	VCC	VCC	VCC	VCC	VCC
J15	J15	VCC	VCC	VCC	VCC	VCC
J16	J16	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
J17	J17	I/O	I/O	I/O	I/O	I/O
J18	J18	I/O	I/O	I/O	I/O	I/O
H1	H1	I/O	I/O	I/O	I/O	I/O
H2	H2	I/O	I/O	I/O	I/O	I/O
H3	H3	I/O	I/O	I/O	I/O	I/O
H4				I/O	I/O	I/O
H15				I/O	I/O	I/O
H16	H16	I/O	I/O	I/O	I/O	I/O
H17	H17	I/O	I/O	I/O	I/O	I/O
H18	H18	I/O	I/O	I/O	I/O	I/O
G1	G1	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
G2	G2	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
G3	G3	GND	GND	GND	GND	GND
G4				I/O	I/O	I/O
G15				I/O	I/O	I/O
G16	G16	GND	GND	GND	GND	GND
G17	G17	I/O	I/O	I/O	I/O	I/O
G18	G18	I/O	I/O	I/O	I/O	I/O
F1	F1	I/O	I/O	I/O	I/O	I/O

PG 223 Pin	PG 191 Pin	XC4008E PG191	XC4010E PG191	XC4013E PG223	XC4020E PG223	XC4025E PG223
F2	F2	N.C.	I/O	I/O	I/O	I/O
F3	F3	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
F4				I/O	I/O	I/O
F15				I/O	I/O	I/O
F16	F16	I/O	I/O	I/O	I/O	I/O
F17	F17	N.C.	I/O	I/O	I/O	I/O
F18	F18	I/O	I/O	I/O	I/O	I/O
E1	E1	I/O	I/O	I/O	I/O	I/O
E2	E2	I/O	I/O	I/O	I/O	I/O
E3	E3	I/O	I/O	I/O	I/O	I/O
E4				I/O	I/O	I/O
E15				I/O	I/O	I/O
E16	E16	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
E17	E17	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
E18	E18	I/O	I/O	I/O	I/O	I/O
D1	D1	N.C.	I/O	I/O	I/O	I/O
D2	D2	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
D3	D3	VCC	VCC	VCC	VCC	VCC
D4	D4	GND	GND	GND	GND	GND
D5				I/O	I/O	I/O
D6				I/O	I/O	I/O
D7				I/O	I/O	I/O
D8				I/O	I/O	I/O
D9	D9	GND	GND	GND	GND	GND
D10	D10	VCC	VCC	VCC	VCC	VCC
D11				I/O	I/O	I/O
D12				I/O	I/O	I/O
D13				I/O	I/O	I/O
D14				I/O	I/O	I/O
D15	D15	GND	GND	GND	GND	GND
D16	D16	VCC	VCC	VCC	VCC	VCC
D17	D17	I/O	I/O	I/O	I/O	I/O
D18	D18	N.C.	I/O	I/O	I/O	I/O
C1	C1	I/O	I/O	I/O	I/O	I/O
C2	C2	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
C3	C3	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
C4	C4	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
C5	C5	I/O	I/O	I/O	I/O	I/O
C6	C6	I/O	I/O	I/O	I/O	I/O
C7	C7	GND	GND	GND	GND	GND
C8	C8	I/O	I/O	I/O	I/O	I/O
C9	C9	I/O	I/O	I/O	I/O	I/O
C10	C10	I/O	I/O	I/O	I/O	I/O
C11	C11	I/O	I/O	I/O	I/O	I/O
C12	C12	GND	GND	GND	GND	GND
C13	C13	I/O	I/O	I/O	I/O	I/O
C14	C14	I/O	I/O	I/O	I/O	I/O
C15	C15	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
C16	C16	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)

PG 223 Pin	PG 191 Pin	XC4008E PG191	XC4010E PG191	XC4013E PG223	XC4020E PG223	XC4025E PG223
C17	C17	I/O	I/O	I/O	I/O	I/O
C18	C18	I/O	I/O	I/O	I/O	I/O
B1	B1	I/O	I/O	I/O	I/O	I/O
B2	B2	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
B3	B3	I/O	I/O	I/O	I/O	I/O
B4	B4	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
B5	B5	N.C.	I/O	I/O	I/O	I/O
B6	B6	N.C.	I/O	I/O	I/O	I/O
B7	B7	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
B8	B8	I/O	I/O	I/O	I/O	I/O
B9	B9	I/O	I/O	I/O	I/O	I/O
B10	B10	I/O	I/O	I/O	I/O	I/O
B11	B11	I/O	I/O	I/O	I/O	I/O
B12	B12	I/O	I/O	I/O	I/O	I/O
B13	B13	N.C.	I/O	I/O	I/O	I/O
B14	B14	I/O	I/O	I/O	I/O	I/O
B15	B15	I/O	I/O	I/O	I/O	I/O
B16	B16	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2
B17	B17	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2
B18	B18	I/O	I/O	I/O	I/O	I/O
A2	A2	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
A3	A3	I/O	I/O	I/O	I/O	I/O
A4	A4	I/O	I/O	I/O	I/O	I/O
A5	A5	I/O	I/O	I/O	I/O	I/O
A6	A6	I/O	I/O	I/O	I/O	I/O
A7	A7	I/O	I/O	I/O	I/O	I/O
A8	A8	I/O	I/O	I/O	I/O	I/O
A9	A9	I/O	I/O	I/O	I/O	I/O
A10	A10	I/O	I/O	I/O	I/O	I/O
A11	A11	I/O	I/O	I/O	I/O	I/O
A12	A12	I/O	I/O	I/O	I/O	I/O
A13	A13	I/O	I/O	I/O	I/O	I/O
A14	A14	N.C.	I/O	I/O	I/O	I/O
A15	A15	I/O	I/O	I/O	I/O	I/O
A16	A16	I/O	I/O	I/O	I/O	I/O
A17	A17	I/O	I/O	I/O	I/O	I/O
A18	A18	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

BG225 Package Pinouts

BG225 Pin	XC4010E	XC4013E/L
R1	VCC	VCC
R2	I/O, PGCK2	I/O, PGCK2
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	I/O	I/O
R8	VCC	VCC
R9	I/O	I/O
R10	N.C.	I/O
R11	I/O	I/O
R12	I/O	I/O
R13	I/O	I/O
R14	I/O	I/O
R15	VCC	VCC
P1	I/O, SCGK2	I/O, SCGK2
P2	I (M0)	I (M0)
P3	I/O (HDC)	I/O (HDC)
P4	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P5	N.C.	I/O
P6	I/O	I/O
P7	N.C.	I/O
P8	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P9	I/O	I/O
P10	N.C.	I/O
P11	I/O	I/O
P12	I/O	I/O
P13	I/O	I/O
P14	DONE	DONE
P15	I/O (D7)	I/O (D7)
N1	I/O	I/O
N2	I/O	I/O
N3	O (M1)	O (M1)
N4	I/O	I/O
N5	I/O	I/O
N6	I/O	I/O
N7	N.C.	I/O
N8	I/O	I/O
N9	I/O	I/O
N10	I/O	I/O
N11	N.C.	I/O
N12	I/O	I/O
N13	I/O, SGCK3	I/O, SGCK3
N14	I/O, PGCK3	I/O, PGCK3
N15	N.C.	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	I (M2)	I (M2)
M5	I/O	I/O
M6	I/O	I/O
M7	I/O	I/O
M8	GND	GND
M9	I/O	I/O
M10	N.C.	I/O
M11	I/O	I/O
M12	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
M13	I/O	I/O
M14	N.C.	I/O
M15	I/O	I/O
L1	I/O	I/O
L2	N.C.	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	N.C.	I/O
L7	I/O	I/O
L8	I/O	I/O
L9	I/O	I/O
L10	I/O	I/O
L11	I/O	I/O
L12	I/O	I/O
L13	I/O	I/O
L14	I/O	I/O
L15	N.C.	I/O
K1	N.C.	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	N.C.	I/O
K5	I/O	I/O
K6	I/O	I/O
K7	I/O	I/O
K8	GND	GND
K9	I/O	I/O
K10	I/O	I/O
K11	I/O	I/O
K12	N.C.	I/O
K13	I/O	I/O
K14	I/O	I/O
K15	I/O (D5)	I/O (D5)
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	N.C.	I/O
J6	I/O	I/O
J7	GND	GND
J8	GND	GND
J9	GND	GND
J10	I/O (D6)	I/O (D6)
J11	I/O	I/O
J12	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
J13	I/O	I/O
J14	I/O	I/O
J15	I/O	I/O
H1	VCC	VCC
H2	GND	GND
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H6	GND	GND
H7	GND	GND
H8	GND	GND
H9	GND	GND
H10	GND	GND
H11	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
H12	I/O (D3)	I/O (D3)
H13	I/O (D4)	I/O (D4)

BG225 Pin	XC4010E	XC4013E/L
H14	I/O	I/O
H15	VCC	VCC
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O	I/O
G6	I/O	I/O
G7	GND	GND
G8	GND	GND
G9	GND	GND
G10	N.C.	I/O
G11	I/O (D2)	I/O (D2)
G12	I/O	I/O
G13	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
F1	N.C.	I/O
F2	N.C.	I/O
F3	I/O	I/O
F4	I/O, TMS	I/O, TMS
F5	I/O	I/O
F6	I/O	I/O
F7	N.C.	I/O
F8	GND	GND
F9	N.C.	I/O
F10	I/O (D0, DIN)	I/O (D0, DIN)
F11	I/O	I/O
F12	N.C.	I/O
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
E1	I/O	I/O
E2	N.C.	I/O
E3	N.C.	I/O
E4	I/O	I/O
E5	I/O	I/O
E6	I/O	I/O
E7	I/O	I/O
E8	I/O (A8)	I/O (A8)
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O (D1)	I/O (D1)
E13	I/O	I/O
E14	N.C.	I/O
E15	N.C.	I/O
D1	I/O	I/O
D2	I/O	I/O
D3	I/O, TDI	I/O, TDI
D4	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
D5	I/O (A13)	I/O (A13)
D6	I/O	I/O
D7	I/O	I/O
D8	VCC	VCC
D9	I/O (A5)	I/O (A5)
D10	I/O	I/O
D11	N.C.	I/O
D12	GND	GND
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
C1	I/O, TCK	I/O, TCK
C2	I/O	I/O
C3	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
C4	N.C.	I/O
C5	I/O	I/O
C6	N.C.	I/O
C7	I/O	I/O
C8	I/O (A6)	I/O (A6)
C9	I/O	I/O
C10	N.C.	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	CCLK	CCLK
C14	I/O	I/O
C15	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)
B1	I/O (A17)	I/O (A17)
B2	VCC	VCC
B3	I/O	I/O
B4	I/O (A12)	I/O (A12)
B5	I/O	I/O
B6	I/O (A11)	I/O (A11)
B7	I/O (A9)	I/O (A9)
B8	I/O (A7)	I/O (A7)
B9	I/O	I/O
B10	N.C.	I/O
B11	I/O	I/O
B12	I/O (A3)	I/O (A3)
B13	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
B14	VCC	VCC
B15	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
A1	GND	GND
A2	I/O (A14)	I/O (A14)
A3	N.C.	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O (A10)	I/O (A10)
A7	I/O	I/O
A8	GND	GND
A9	I/O	I/O
A10	I/O (A4)	I/O (A4)
A11	I/O	I/O
A12	I/O	I/O
A13	I/O (CS1, A2)	I/O (CS1, A2)
A14	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
A15	O, TDO	O, TDO

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PQ240, HQ240 Package Pinouts

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P1	GND	GND	GND	GND
P2	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, GCK1 (A16)
P3	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P4	I/O	I/O	I/O	I/O
P5	I/O	I/O	I/O	I/O
P6	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P7	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P8	I/O	I/O	I/O	I/O
P9	I/O	I/O	I/O	I/O
P10	I/O	I/O	I/O	I/O
P11	I/O	I/O	I/O	I/O
P12	I/O	I/O	I/O	I/O
P13	I/O	I/O	I/O	I/O
P14	GND	GND	GND	GND
P15	I/O	I/O	I/O	I/O, FCLK1
P16	I/O	I/O	I/O	I/O
P17	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P18	I/O	I/O	I/O	I/O
P19	VCC	VCC	VCC	VCC
P20	I/O	I/O	I/O	I/O
P21	I/O	I/O	I/O	I/O
P22	N.C.‡	N.C.‡	N.C.‡	GND‡
P23	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O
P26	I/O	I/O	I/O	I/O
P27	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O
P29	GND	GND	GND	GND
P30	VCC	VCC	VCC	VCC
P31	I/O	I/O	I/O	I/O
P32	I/O	I/O	I/O	I/O
P33	I/O	I/O	I/O	I/O
P34	I/O	I/O	I/O	I/O
P35	I/O	I/O	I/O	I/O
P36	I/O	I/O	I/O	I/O
P37	N.C.‡	N.C.‡	N.C.‡	GND‡
P38	I/O	I/O	I/O	I/O
P39	I/O	I/O	I/O	I/O
P40	VCC	VCC	VCC	VCC
P41	I/O	I/O	I/O	I/O
P42	I/O	I/O	I/O	I/O
P43	I/O	I/O	I/O	I/O
P44	I/O	I/O	I/O	I/O, FCLK2
P45	GND	GND	GND	GND
P46	I/O	I/O	I/O	I/O
P47	I/O	I/O	I/O	I/O
P48	I/O	I/O	I/O	I/O
P49	I/O	I/O	I/O	I/O
P50	I/O	I/O	I/O	I/O
P51	I/O	I/O	I/O	I/O
P52	I/O	I/O	I/O	I/O
P53	I/O	I/O	I/O	I/O
P54	I/O	I/O	I/O	I/O
P55	I/O	I/O	I/O	I/O
P56	I/O	I/O	I/O	I/O
P57	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, GCK2
P58	O (M1)	O (M1)	O (M1)	O (M1)
P59	GND	GND	GND	GND
P60	I (M0)	I (M0)	I (M0)	I (M0)
P61	VCC	VCC	VCC	VCC
P62	I (M2)	I (M2)	I (M2)	I (M2)
P63	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, GCK3
P64	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P65	I/O	I/O	I/O	I/O
P66	I/O	I/O	I/O	I/O
P67	I/O	I/O	I/O	I/O
P68	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P69	I/O	I/O	I/O	I/O
P70	I/O	I/O	I/O	I/O
P71	I/O	I/O	I/O	I/O
P72	I/O	I/O	I/O	I/O
P73	I/O	I/O	I/O	I/O
P74	I/O	I/O	I/O	I/O
P75	GND	GND	GND	GND
P76	I/O	I/O	I/O	I/O
P77	I/O	I/O	I/O	I/O
P78	I/O	I/O	I/O	I/O
P79	I/O	I/O	I/O	I/O
P80	VCC	VCC	VCC	VCC
P81	I/O	I/O	I/O	I/O
P82	I/O	I/O	I/O	I/O
P83	N.C.‡	N.C.‡	N.C.‡	GND‡
P84	I/O	I/O	I/O	I/O
P85	I/O	I/O	I/O	I/O
P86	I/O	I/O	I/O	I/O
P87	I/O	I/O	I/O	I/O
P88	I/O	I/O	I/O	I/O
P89	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P90	VCC	VCC	VCC	VCC
P91	GND	GND	GND	GND
P92	I/O	I/O	I/O	I/O
P93	I/O	I/O	I/O	I/O
P94	I/O	I/O	I/O	I/O
P95	I/O	I/O	I/O	I/O
P96	I/O	I/O	I/O	I/O
P97	I/O	I/O	I/O	I/O
P98	N.C.‡	N.C.‡	N.C.‡	GND‡
P99	I/O	I/O	I/O	I/O
P100	I/O	I/O	I/O	I/O
P101	VCC	VCC	VCC	VCC
P102	I/O	I/O	I/O	I/O
P103	I/O	I/O	I/O	I/O
P104	I/O	I/O	I/O	I/O
P105	I/O	I/O	I/O	I/O
P106	GND	GND	GND	GND
P107	I/O	I/O	I/O	I/O
P108	I/O	I/O	I/O	I/O
P109	I/O	I/O	I/O	I/O
P110	I/O	I/O	I/O	I/O
P111	I/O	I/O	I/O	I/O
P112	I/O	I/O	I/O	I/O
P113	I/O	I/O	I/O	I/O
P114	I/O	I/O	I/O	I/O
P115	I/O	I/O	I/O	I/O
P116	I/O	I/O	I/O	I/O
P117	I/O	I/O	I/O	I/O
P118	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, GCK4
P119	GND	GND	GND	GND
P120	DONE	DONE	DONE	DONE
P121	VCC	VCC	VCC	VCC
P122	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$
P123	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P124	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, GCK5
P125	I/O	I/O	I/O	I/O
P126	I/O	I/O	I/O	I/O
P127	I/O	I/O	I/O	I/O
P128	I/O	I/O	I/O	I/O
P129	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P130	I/O	I/O	I/O	I/O
P131	I/O	I/O	I/O	I/O
P132	I/O	I/O	I/O	I/O
P133	I/O	I/O	I/O	I/O

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P134	I/O	I/O	I/O	I/O
P135	GND	GND	GND	GND
P136	I/O	I/O	I/O	I/O
P137	I/O	I/O	I/O	I/O
P138	I/O	I/O	I/O	I/O, FCLK3
P139	I/O	I/O	I/O	I/O
P140	VCC	VCC	VCC	VCC
P141	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P142	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P143	N.C.‡	N.C.‡	N.C.‡	GND‡
P144	I/O	I/O	I/O	I/O
P145	I/O	I/O	I/O	I/O
P146	I/O	I/O	I/O	I/O
P147	I/O	I/O	I/O	I/O
P148	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P149	I/O	I/O	I/O	I/O
P150	VCC	VCC	VCC	VCC
P151	GND	GND	GND	GND
P152	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P153	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P154	I/O	I/O	I/O	I/O
P155	I/O	I/O	I/O	I/O
P156	I/O	I/O	I/O	I/O
P157	I/O	I/O	I/O	I/O
P158	N.C.‡	N.C.‡	N.C.‡	GND‡
P159	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P160	I/O	I/O	I/O	I/O
P161	VCC	VCC	VCC	VCC
P162	I/O	I/O	I/O	I/O
P163	I/O	I/O	I/O	I/O, FCLK4
P164	I/O	I/O	I/O	I/O
P165	I/O	I/O	I/O	I/O
P166	GND	GND	GND	GND
P167	I/O	I/O	I/O	I/O
P168	I/O	I/O	I/O	I/O
P169	I/O	I/O	I/O	I/O
P170	I/O	I/O	I/O	I/O
P171	I/O	I/O	I/O	I/O
P172	I/O	I/O	I/O	I/O
P173	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P174	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)
P175	I/O	I/O	I/O	I/O
P176	I/O	I/O	I/O	I/O

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P177	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P178	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)
P179	CCLK	CCLK	CCLK	CCLK
P180	VCC	VCC	VCC	VCC
P181	O, TDO	O, TDO	O, TDO	O, TDO
P182	GND	GND	GND	GND
P183	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
P184	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, GCK7 (A1)
P185	I/O	I/O	I/O	I/O
P186	I/O	I/O	I/O	I/O
P187	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P188	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P189	I/O	I/O	I/O	I/O
P190	I/O	I/O	I/O	I/O
P191	I/O	I/O	I/O	I/O
P192	I/O	I/O	I/O	I/O
P193	I/O	I/O	I/O	I/O
P194	I/O	I/O	I/O	I/O
P195	N.C.	N.C.	I/O	I/O
P196	GND	GND	GND	GND
P197	I/O	I/O	I/O	I/O
P198	I/O	I/O	I/O	I/O
P199	I/O	I/O	I/O	I/O
P200	I/O	I/O	I/O	I/O
P201	VCC	VCC	VCC	VCC
P202	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
P203	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
P204	N.C.‡	N.C.‡	N.C.‡	GND‡
P205	I/O	I/O	I/O	I/O
P206	I/O	I/O	I/O	I/O
P207	I/O	I/O	I/O	I/O (A21)
P208	I/O	I/O	I/O	I/O (A20)
P209	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
P210	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)
P211	GND	GND	GND	GND
P212	VCC	VCC	VCC	VCC
P213	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
P214	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
P215	I/O	I/O	I/O	I/O (A19)
P216	I/O	I/O	I/O	I/O (A18)
P217	I/O	I/O	I/O	I/O
P218	I/O	I/O	I/O	I/O
P219	N.C.‡	N.C.‡	N.C.‡	GND‡
P220	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
P221	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
P222	VCC	VCC	VCC	VCC
P223	I/O	I/O	I/O	I/O
P224	I/O	I/O	I/O	I/O
P225	I/O	I/O	I/O	I/O
P226	I/O	I/O	I/O	I/O
P227	GND	GND	GND	GND
P228	I/O	I/O	I/O	I/O
P229	I/O	I/O	I/O	I/O
P230	I/O	I/O	I/O	I/O
P231	I/O	I/O	I/O	I/O
P232	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
P233	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
P234	I/O	I/O	I/O	I/O
P235	I/O	I/O	I/O	I/O
P236	I/O	I/O	I/O	I/O
P237	I/O	I/O	I/O	I/O
P238	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
P239	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, GCK8 (A15)
P240	VCC	VCC	VCC	VCC

3/11/96

‡ Pins labelled GND‡ should be connected to Ground if possible; however, they can be left unconnected if necessary for compatibility with other devices. Pins labelled N.C.‡ are reserved for Ground connections on future revisions of the device. These pins do not physically connect to anything on the current device revision. However, they should be externally connected to Ground if possible.

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

PG299 Package Pinouts

PG299 Pin	XC4025E	XC4028EX/XL
X1	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)
X2	GND	GND
X3	I/O	I/O
X4	I/O	I/O
X5	VCC	VCC
X6	GND	GND
X7	I/O	I/O
X8	I/O	I/O
X9	I/O	I/O
X10	VCC	VCC
X11	GND	GND
X12	I/O	I/O
X13	I/O	I/O
X14	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
X15	VCC	VCC
X16	GND	GND
X17	I/O	I/O
X18	I/O	I/O
X19	VCC	VCC
X20	I/O, SGCK3	I/O, GCK4
W1	VCC	VCC
W2	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O
W7	I/O	I/O, FCLK4
W8	I/O (D2)	I/O (D2)
W9	I/O	I/O
W10	I/O (D3)	I/O (D3)
W11	I/O	I/O
W12	I/O	I/O
W13	I/O	I/O
W14	I/O	I/O, FCLK3
W15	I/O	I/O
W16	I/O	I/O
W17	I/O (D6)	I/O (D6)
W18	I/O, PGCK3	I/O, GCK5
W19	I/O (D7)	I/O (D7)
W20	GND	GND
V1	I/O (A3)	I/O (A3)
V2	I/O, PGCK4 (A1)	I/O, GCK7 (A1)
V3	CCLK	CCLK
V4	I/O (D0, DIN)	I/O (D0, DIN)
V5	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
V6	I/O	I/O
V7	I/O	I/O
V8	I/O	I/O
V9	I/O	I/O
V10	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
V11	I/O (D4)	I/O (D4)
V12	I/O	I/O
V13	I/O	I/O
V14	I/O	I/O
V15	I/O	I/O
V16	I/O	I/O
V17	I/O	I/O
V18	DONE	DONE
V19	I/O	I/O
V20	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O (CS1, A2)	I/O (CS1, A2)
U4	O, TDO	O, TDO
U5	I/O	I/O
U6	I/O (D1)	I/O (D1)
U7	I/O	I/O
U8	I/O	I/O
U9	I/O	I/O
U10	I/O	I/O
U11	I/O	I/O
U12	I/O	I/O
U13	I/O	I/O
U14	I/O	I/O
U15	I/O	I/O
U16	I/O	I/O
U17	$\overline{PROGRAM}$	$\overline{PROGRAM}$
U18	I/O	I/O
U19	I/O	I/O
U20	I/O	I/O
T1	GND	GND
T2	I/O	I/O
T3	I/O	I/O
T4	I/O	I/O
T5	GND	GND
T6	I/O	I/O
T7	I/O	I/O
T8	I/O	I/O
T9	I/O	I/O
T10	I/O	I/O
T11	I/O	I/O
T12	I/O (D5)	I/O (D5)
T13	I/O	I/O
T14	I/O	I/O
T15	I/O	I/O
T16	VCC	VCC
T17	I/O	I/O
T18	I/O	I/O
T19	I/O	I/O
T20	VCC	VCC
R1	VCC	VCC
R2	I/O	I/O

PG299 Pin	XC4025E	XC4028EX/XL
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R16	I/O	I/O
R17	I/O	I/O
R18	I/O	I/O
R19	I/O	I/O
R20	GND	GND
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	I/O	I/O
P5	I/O	I/O
P16	I/O	I/O
P17	I/O	I/O
P18	I/O	I/O
P19	I/O	I/O
P20	I/O	I/O
N1	I/O (A4)	I/O (A4)
N2	I/O	I/O
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N16	I/O	I/O
N17	I/O	I/O
N18	I/O	I/O
N19	I/O	I/O
N20	I/O	I/O
M1	I/O	I/O (A21)
M2	I/O	I/O
M3	I/O (A5)	I/O (A5)
M4	I/O	I/O
M5	I/O	I/O
M16	I/O	I/O
M17	I/O	I/O
M18	I/O	I/O
M19	I/O	I/O
M20	I/O	I/O
L1	GND	GND
L2	I/O (A7)	I/O (A7)
L3	I/O (A6)	I/O (A6)
L4	I/O	I/O (A20)
L5	I/O	I/O
L16	I/O	I/O
L17	I/O	I/O
L18	I/O	I/O
L19	I/O	I/O
L20	VCC	VCC
K1	VCC	VCC
K2	I/O (A8)	I/O (A8)
K3	I/O (A9)	I/O (A9)
K4	I/O	I/O (A18)

PG299 Pin	XC4025E	XC4028EX/XL
K5	I/O	I/O (A19)
K16	I/O	I/O
K17	I/O	I/O
K18	I/O	I/O
K19	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
K20	GND	GND
J1	I/O	I/O
J2	I/O	I/O
J3	I/O (A11)	I/O (A11)
J4	I/O	I/O
J5	I/O	I/O
J16	I/O	I/O
J17	I/O	I/O
J18	I/O	I/O
J19	I/O	I/O
J20	I/O	I/O
H1	I/O (A10)	I/O (A10)
H2	I/O	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H16	I/O	I/O
H17	I/O	I/O
H18	I/O	I/O
H19	I/O	I/O
H20	I/O	I/O
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O (A12)	I/O (A12)
G16	I/O	I/O
G17	I/O	I/O
G18	I/O	I/O
G19	I/O	I/O
G20	I/O	I/O
F1	GND	GND
F2	I/O	I/O
F3	I/O	I/O
F4	I/O	I/O
F5	I/O	I/O
F16	I/O	I/O
F17	I/O	I/O
F18	I/O	I/O
F19	I/O	I/O
F20	VCC	VCC
E1	VCC	VCC
E2	I/O	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	VCC	VCC
E6	I/O	I/O

PG299 Pin	XC4025E	XC4028EX/XL
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	I/O	I/O
E14	I/O	I/O
E15	I/O	I/O
E16	GND	GND
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	GND	GND
D1	I/O	I/O
D2	I/O	I/O
D3	I/O (A14)	I/O (A14)
D4	I/O, PGCK1 (A16)	I/O, GCK1 (A16)
D5	I/O, TDI	I/O, TDI
D6	I/O	I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	I/O
D13	I/O	I/O, FCLK2
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I (M2)	I (M2)
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
C1	I/O (A13)	I/O (A13)
C2	I/O	I/O
C3	I/O, SGCK1 (A15)	I/O, GCK8 (A15)
C4	I/O, TCK	I/O, TCK
C5	I/O	I/O
C6	I/O	I/O
C7	I/O, TMS	I/O, TMS
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O, SGCK2	I/O, GCK2
C18	I (M0)	I (M0)

PG299 Pin	XC4025E	XC4028EX/XL
C19	I/O (HDC)	I/O (HDC)
C20	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
B1	GND	GND
B2	I/O (A17)	I/O (A17)
B3	I/O	I/O
B4	I/O	I/O
B5	I/O	I/O
B6	I/O	I/O, FCLK1
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O, PGCK2	I/O, GCK3
B20	VCC	VCC
A2	VCC	VCC
A3	I/O	I/O
A4	I/O	I/O
A5	GND	GND
A6	VCC	VCC
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	GND	GND
A11	VCC	VCC
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	GND	GND
A16	VCC	VCC
A17	I/O	I/O
A18	I/O	I/O
A19	GND	GND
A20	O (M1)	O (M1)

3/18/96

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

HQ304 Package Pinouts

HQ304 Pin	XC4025E	XC4028EX XC4028XL	XC4036EX XC4036XL
P1	VCC	VCC	VCC
P2	I/O, SGCK1 (A15)	I/O, GCK8 (A15)	I/O, GCK8 (A15)
P3	I/O (A14)	I/O (A14)	I/O (A14)
P4	I/O	I/O	I/O
P5	I/O	I/O	I/O
P6	I/O	I/O	I/O
P7	I/O	I/O	I/O
P8	I/O	I/O	I/O
P9	I/O	I/O	I/O
P10	I/O (A13)	I/O (A13)	I/O (A13)
P11	N.C.	N.C.	N.C.
P12	I/O (A12)	I/O (A12)	I/O (A12)
P13	I/O	I/O	I/O
P14	I/O	I/O	I/O
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
P17	I/O	I/O	I/O
P18	I/O	I/O	I/O
P19	GND	GND	GND
P20	I/O	I/O	I/O
P21	I/O	I/O	I/O
P22	I/O	I/O	I/O
P23	I/O	I/O	I/O
P24	N.C.	N.C.	N.C.
P25	VCC	VCC	VCC
P26	I/O	I/O	I/O
P27	I/O	I/O	I/O
P28	I/O	I/O	I/O
P29	I/O	I/O	I/O
P30	I/O (A11)	I/O (A11)	I/O (A11)
P31	I/O (A10)	I/O (A10)	I/O (A10)
P32	I/O	I/O	I/O
P33	I/O	I/O	I/O
P34	I/O	I/O (A18)	I/O (A18)
P35	I/O	I/O (A19)	I/O (A19)
P36	I/O (A9)	I/O (A9)	I/O (A9)
P37	I/O (A8)	I/O (A8)	I/O (A8)
P38	VCC	VCC	VCC
P39	GND	GND	GND
P40	I/O (A7)	I/O (A7)	I/O (A7)
P41	I/O (A6)	I/O (A6)	I/O (A6)
P42	I/O	I/O (A20)	I/O (A20)
P43	I/O	I/O (A21)	I/O (A21)
P44	I/O	I/O	I/O
P45	I/O	I/O	I/O
P46	I/O (A5)	I/O (A5)	I/O (A5)
P47	I/O (A4)	I/O (A4)	I/O (A4)
P48	I/O	I/O	I/O
P49	I/O	I/O	I/O
P50	I/O	I/O	I/O
P51	I/O	I/O	I/O
P52	VCC	VCC	VCC
P53	N.C.	N.C.	N.C.
P54	I/O	I/O	I/O
P55	I/O	I/O	I/O
P56	I/O	I/O	I/O
P57	I/O	I/O	I/O
P58	GND	GND	GND
P59	I/O	I/O	I/O
P60	I/O	I/O	I/O
P61	I/O	I/O	I/O
P62	I/O	I/O	I/O
P63	I/O	I/O	I/O
P64	I/O	I/O	I/O
P65	I/O	I/O	I/O
P66	I/O	I/O	I/O
P67	I/O	I/O	I/O
P68	I/O	I/O	I/O
P69	I/O (A3)	I/O (A3)	I/O (A3)
P70	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P71	I/O	I/O	I/O
P72	I/O	I/O	I/O
P73	I/O, PGCK4 (A1)	I/O, GCK7 (A1)	I/O, GCK7 (A1)
P74	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
P75	GND	GND	GND
P76	O, TDO	O, TDO	O, TDO
P77	VCC	VCC	VCC
P78	CCLK	CCLK	CCLK
P79	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)	I/O, GCK6 (DOUT)
P80	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P81	I/O	I/O	I/O
P82	I/O	I/O	I/O
P83	I/O	I/O	I/O
P84	I/O	I/O	I/O
P85	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
P86	I/O (D1)	I/O (D1)	I/O (D1)
P87	I/O	I/O	I/O
P88	I/O	I/O	I/O
P89	I/O	I/O	I/O
P90	I/O	I/O	I/O
P91	I/O	I/O	I/O
P92	I/O	I/O	I/O
P93	I/O	I/O	I/O
P94	I/O	I/O	I/O
P95	GND	GND	GND
P96	I/O	I/O	I/O
P97	I/O	I/O	I/O
P98	I/O	I/O, FCLK4	I/O, FCLK4
P99	I/O	I/O	I/O
P100	N.C.	N.C.	N.C.
P101	VCC	VCC	VCC

HQ304 Pin	XC4025E	XC4028EX XC4028XL	XC4036EX XC4036XL
P102	I/O	I/O	I/O
P103	I/O (D2)	I/O (D2)	I/O (D2)
P104	I/O	I/O	I/O
P105	I/O	I/O	I/O
P106	I/O	I/O	I/O
P107	I/O	I/O	I/O
P108	I/O	I/O	I/O
P109	I/O	I/O	I/O
P110	I/O	I/O	I/O
P111	I/O	I/O	I/O
P112	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
P113	I/O (D3)	I/O (D3)	I/O (D3)
P114	GND	GND	GND
P115	VCC	VCC	VCC
P116	I/O	I/O	I/O
P117	I/O (D4)	I/O (D4)	I/O (D4)
P118	I/O	I/O	I/O
P119	I/O	I/O	I/O
P120	I/O	I/O	I/O
P121	I/O	I/O	I/O
P122	I/O	I/O	I/O
P123	I/O	I/O	I/O
P124	I/O	I/O	I/O
P125	I/O	I/O	I/O
P126	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
P127	I/O (D5)	I/O (D5)	I/O (D5)
P128	N.C.	N.C.	N.C.
P129	VCC	VCC	VCC
P130	I/O	I/O	I/O
P131	I/O	I/O, FCLK3	I/O, FCLK3
P132	I/O	I/O	I/O
P133	I/O	I/O	I/O
P134	GND	GND	GND
P135	I/O	I/O	I/O
P136	I/O	I/O	I/O
P137	I/O	I/O	I/O
P138	I/O	I/O	I/O
P139	I/O	I/O	I/O
P140	I/O	I/O	I/O
P141	I/O	I/O	I/O
P142	I/O (D6)	I/O (D6)	I/O (D6)
P143	I/O	I/O	I/O
P144	I/O	I/O	I/O
P145	I/O	I/O	I/O
P146	I/O	I/O	I/O
P147	I/O	I/O	I/O
P148	I/O	I/O	I/O
P149	I/O, PGCK3	I/O, GCK5	I/O, GCK5
P150	I/O (D7)	I/O (D7)	I/O (D7)
P151	$\overline{PROGRAM}$	$\overline{PROGRAM}$	$\overline{PROGRAM}$
P152	VCC	VCC	VCC
P153	DONE	DONE	DONE
P154	GND	GND	GND

HQ304 Pin	XC4025E	XC4028EX XC4028XL	XC4036EX XC4036XL
P155	I/O, SGCK3	I/O, GCK4	I/O, GCK4
P156	I/O	I/O	I/O
P157	I/O	I/O	I/O
P158	I/O	I/O	I/O
P159	I/O	I/O	I/O
P160	I/O	I/O	I/O
P161	I/O	I/O	I/O
P162	I/O	I/O	I/O
P163	I/O	I/O	I/O
P164	I/O	I/O	I/O
P165	I/O	I/O	I/O
P166	I/O	I/O	I/O
P167	I/O	I/O	I/O
P168	I/O	I/O	I/O
P169	I/O	I/O	I/O
P170	I/O	I/O	I/O
P171	GND	GND	GND
P172	I/O	I/O	I/O
P173	I/O	I/O	I/O
P174	I/O	I/O	I/O
P175	I/O	I/O	I/O
P176	N.C.	N.C.	N.C.
P177	VCC	VCC	VCC
P178	I/O	I/O	I/O
P179	I/O	I/O	I/O
P180	I/O	I/O	I/O
P181	I/O	I/O	I/O
P182	I/O	I/O	I/O
P183	I/O	I/O	I/O
P184	I/O	I/O	I/O
P185	I/O	I/O	I/O
P186	I/O	I/O	I/O
P187	I/O	I/O	I/O
P188	I/O	I/O	I/O
P189	I/O	I/O	I/O
P190	GND	GND	GND
P191	VCC	VCC	VCC
P192	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
P193	I/O	I/O	I/O
P194	I/O	I/O	I/O
P195	I/O	I/O	I/O
P196	I/O	I/O	I/O
P197	I/O	I/O	I/O
P198	I/O	I/O	I/O
P199	I/O	I/O	I/O
P200	I/O	I/O	I/O
P201	I/O	I/O	I/O
P202	I/O	I/O	I/O
P203	I/O	I/O	I/O
P204	VCC	VCC	VCC
P205	N.C.	N.C.	N.C.
P206	I/O	I/O	I/O
P207	I/O	I/O	I/O

HQ304 Pin	XC4025E	XC4028EX XC4028XL	XC4036EX XC4036XL
P208	I/O	I/O	I/O
P209	I/O	I/O	I/O
P210	GND	GND	GND
P211	I/O	I/O	I/O
P212	I/O	I/O	I/O
P213	I/O	I/O	I/O
P214	I/O	I/O	I/O
P215	I/O	I/O	I/O
P216	I/O	I/O	I/O
P217	I/O	I/O	I/O
P218	I/O	I/O	I/O
P219	I/O	I/O	I/O
P220	I/O	I/O	I/O
P221	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P222	I/O	I/O	I/O
P223	I/O	I/O	I/O
P224	I/O	I/O	I/O
P225	I/O (HDC)	I/O (HDC)	I/O (HDC)
P226	I/O, PGCK2	I/O, GCK3	I/O, GCK3
P227	I (M2)	I (M2)	I (M2)
P228	VCC	VCC	VCC
P229	I (M0)	I (M0)	I (M0)
P230	GND	GND	GND
P231	O (M1)	O (M1)	O (M1)
P232	I/O, SGCK2	I/O, GCK2	I/O, GCK2
P233	I/O	I/O	I/O
P234	I/O	I/O	I/O
P235	I/O	I/O	I/O
P236	I/O	I/O	I/O
P237	I/O	I/O	I/O
P238	I/O	I/O	I/O
P239	I/O	I/O	I/O
P240	I/O	I/O	I/O
P241	I/O	I/O	I/O
P242	I/O	I/O	I/O
P243	I/O	I/O	I/O
P244	I/O	I/O	I/O
P245	I/O	I/O	I/O
P246	I/O	I/O	I/O
P247	I/O	I/O	I/O
P248	GND	GND	GND
P249	I/O	I/O, FCLK2	I/O, FCLK2
P250	I/O	I/O	I/O
P251	I/O	I/O	I/O
P252	I/O	I/O	I/O
P253	VCC	VCC	VCC
P254	N.C.	N.C.	N.C.
P255	I/O	I/O	I/O
P256	I/O	I/O	I/O
P257	I/O	I/O	I/O
P258	I/O	I/O	I/O
P259	I/O	I/O	I/O
P260	I/O	I/O	I/O
P261	I/O	I/O	I/O
P262	I/O	I/O	I/O
P263	I/O	I/O	I/O
P264	I/O	I/O	I/O
P265	I/O	I/O	I/O
P266	I/O	I/O	I/O
P267	VCC	VCC	VCC
P268	GND	GND	GND
P269	I/O	I/O	I/O
P270	I/O	I/O	I/O
P271	I/O	I/O	I/O
P272	I/O	I/O	I/O
P273	I/O	I/O	I/O
P274	I/O	I/O	I/O
P275	I/O	I/O	I/O
P276	I/O	I/O	I/O
P277	I/O	I/O	I/O
P278	I/O	I/O	I/O
P279	I/O	I/O	I/O
P280	I/O	I/O	I/O
P281	N.C.	N.C.	N.C.
P282	VCC	VCC	VCC
P283	I/O	I/O	I/O
P284	I/O, TMS	I/O, TMS	I/O, TMS
P285	I/O	I/O	I/O
P286	I/O	I/O, FCLK1	I/O, FCLK1
P287	GND	GND	GND
P288	I/O	I/O	I/O
P289	I/O	I/O	I/O
P290	I/O	I/O	I/O
P291	I/O	I/O	I/O
P292	I/O	I/O	I/O
P293	I/O	I/O	I/O
P294	I/O	I/O	I/O
P295	I/O	I/O	I/O
P296	I/O	I/O	I/O
P297	I/O	I/O	I/O
P298	I/O, TCK	I/O, TCK	I/O, TCK
P299	I/O, TDI	I/O, TDI	I/O, TDI
P300	I/O	I/O	I/O
P301	I/O	I/O	I/O
P302	I/O (A17)	I/O (A17)	I/O (A17)
P303	I/O, PGCK1 (A16)	I/O, GCK1 (A16)	I/O, GCK1 (A16)
P304	GND	GND	GND

3/20/96

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

BG352 Package Pinouts

BG352 Pin	XC4028EX/XL
AF1	GND
AF2	GND
AF3	I/O
AF4	I/O
AF5	GND
AF6	I/O
AF7	I/O
AF8	GND
AF9	I/O
AF10	VCC
AF11	I/O
AF12	I/O
AF13	GND
AF14	I/O ($\overline{\text{INIT}}$)
AF15	I/O
AF16	I/O
AF17	VCC
AF18	I/O
AF19	GND
AF20	I/O
AF21	I/O
AF22	GND
AF23	I/O
AF24	I/O
AF25	GND
AF26	GND
AE1	GND
AE2	VCC
AE3	I/O
AE4	N.C.
AE5	I/O
AE6	I/O
AE7	I/O
AE8	I/O
AE9	I/O
AE10	N.C.
AE11	I/O
AE12	I/O
AE13	I/O
AE14	I/O
AE15	I/O
AE16	I/O
AE17	I/O
AE18	I/O
AE19	I/O
AE20	I/O
AE21	I/O
AE22	I/O
AE23	I/O ($\overline{\text{LDC}}$)
AE24	I/O, GCK3
AE25	VCC
AE26	GND
AD1	I/O
AD2	I/O (D7)
AD3	DONE
AD4	I/O
AD5	I/O
AD6	I/O
AD7	I/O
AD8	I/O
AD9	I/O
AD10	I/O
AD11	I/O
AD12	I/O
AD13	I/O
AD14	I/O
AD15	I/O
AD16	N.C.
AD17	I/O
AD18	I/O
AD19	I/O
AD20	I/O
AD21	N.C.
AD22	I/O
AD23	I/O (HDC)
AD24	I (M0)
AD25	I/O
AD26	N.C.
AC1	I/O
AC2	N.C.
AC3	I/O, GCK5
AC4	$\overline{\text{PROGRAM}}$
AC5	I/O, GCK4
AC6	N.C.
AC7	I/O
AC8	VCC
AC9	I/O
AC10	I/O
AC11	N.C.
AC12	I/O
AC13	I/O
AC14	VCC
AC15	I/O
AC16	N.C.
AC17	I/O
AC18	I/O
AC19	I/O
AC20	VCC
AC21	N.C.
AC22	I/O
AC23	I (M2)
AC24	I/O, GCK2
AC25	N.C.
AC26	I/O
AB1	GND
AB2	I/O
AB3	N.C.
AB4	I/O
AB23	O (M1)
AB24	I/O
AB25	I/O
AB26	GND
AA1	I/O
AA2	I/O
AA3	I/O
AA4	I/O
AA23	I/O
AA24	I/O

BG352 Pin	XC4028EX/XL
AA25	I/O
AA26	I/O
Y1	I/O
Y2	I/O
Y3	I/O (D6)
Y4	VCC
Y23	I/O
Y24	I/O
Y25	I/O
Y26	I/O
W1	GND
W2	I/O
W3	I/O
W4	I/O
W23	VCC
W24	I/O
W25	I/O
W26	GND
V1	I/O ($\overline{CS0}$)
V2	I/O (D5)
V3	I/O
V4	I/O
V23	I/O
V24	I/O
V25	I/O
V26	I/O
U1	VCC
U2	I/O
U3	I/O
U4	I/O, FCLK3
U23	I/O, FCLK2
U24	I/O
U25	N.C.
U26	VCC
T1	I/O
T2	I/O
T3	N.C.
T4	N.C.
T23	I/O
T24	N.C.
T25	I/O
T26	I/O
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R23	I/O
R24	I/O
R25	I/O
R26	I/O
P1	I/O
P2	I/O (D4)
P3	I/O
P4	VCC
P23	I/O
P24	I/O
P25	I/O
P26	GND
N1	GND
N2	I/O (D3)

BG352 Pin	XC4028EX/XL
N3	I/O
N4	I/O ($\overline{RS}$)
N23	VCC
N24	I/O
N25	I/O
N26	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M23	I/O
M24	I/O
M25	I/O
M26	I/O
L1	I/O
L2	I/O
L3	I/O
L4	N.C.
L23	N.C.
L24	I/O
L25	I/O
L26	I/O
K1	VCC
K2	N.C.
K3	I/O
K4	I/O
K23	I/O
K24	I/O
K25	I/O
K26	VCC
J1	I/O (D2)
J2	I/O
J3	I/O, FCLK4
J4	I/O
J23	I/O, FCLK1
J24	I/O
J25	I/O
J26	N.C.
H1	GND
H2	I/O
H3	I/O
H4	VCC
H23	I/O
H24	I/O
H25	I/O, TMS
H26	GND
G1	I/O
G2	I/O
G3	I/O
G4	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
G23	VCC
G24	I/O
G25	I/O
G26	I/O
F1	I/O
F2	I/O
F3	I/O (D1)
F4	I/O
F23	N.C.
F24	I/O

BG352 Pin	XC4028EX/XL
F25	I/O
F26	I/O
E1	GND
E2	I/O
E3	I/O
E4	I/O, GCK6 (DOUT)
E23	I/O
E24	I/O, TCK
E25	I/O
E26	GND
D1	N.C.
D2	I/O
D3	I/O (D0, DIN)
D4	O (TDO)
D5	I/O
D6	I/O (CS1, A2)
D7	VCC
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	I/O (A4)
D13	VCC
D14	I/O (A8)
D15	I/O
D16	N.C.
D17	I/O
D18	I/O
D19	VCC
D20	I/O
D21	I/O
D22	I/O (A14)
D23	I/O, GCK1 (A16)
D24	I/O
D25	N.C.
D26	I/O
C1	N.C.
C2	I/O
C3	CCLK
C4	I/O, GCK7 (A1)
C5	N.C.
C6	I/O (A3)
C7	I/O
C8	N.C.
C9	I/O
C10	I/O
C11	N.C.
C12	I/O (A5)
C13	I/O (A21)
C14	I/O (A9)
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O
C21	I/O (A13)
C22	I/O
C23	I/O
C24	I/O, GCK8 (A15)

BG352 Pin	XC4028EX/XL
C25	I/O (A17)
C26	I/O, TDI
B1	GND
B2	VCC
B3	I/O (A0, $\overline{WS}$)
B4	N.C.
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	N.C.
B11	I/O
B12	I/O
B13	I/O (A20)
B14	I/O (A7)
B15	I/O (A18)
B16	I/O (A11)
B17	I/O
B18	I/O
B19	I/O
B20	I/O
B21	I/O
B22	I/O (A12)
B23	N.C.
B24	I/O
B25	VCC
B26	GND
A1	GND
A2	GND
A3	I/O
A4	I/O
A5	GND
A6	I/O
A7	I/O
A8	GND
A9	I/O
A10	VCC
A11	I/O
A12	I/O
A13	I/O (A6)
A14	GND
A15	I/O (A19)
A16	I/O (A10)
A17	VCC
A18	N.C.
A19	GND
A20	I/O
A21	I/O
A22	GND
A23	I/O
A24	N.C.
A25	GND
A26	GND

2/28/96

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

PG411 Package Pinouts

PG411 Pin	XC4036EX/XL	XC4044EX/XL
AW1	I/O	I/O
AW3	GND	GND
AW5	I/O	I/O
AW7	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
AW9	VCC	VCC
AW11	GND	GND
AW13	I/O	I/O
AW15	N.C.	I/O
AW17	I/O	I/O
AW19	VCC	VCC
AW21	GND	GND
AW23	N.C.	I/O
AW25	N.C.	I/O
AW27	I/O	I/O
AW29	VCC	VCC
AW31	GND	GND
AW33	I/O	I/O
AW35	N.C.	N.C.
AW37	VCC	VCC
AW39	I/O	I/O
AV2	I/O, GCK7 (A1)	I/O, GCK7 (A1)
AV4	I/O	I/O
AV6	I/O	I/O
AV8	N.C.	I/O
AV10	I/O	I/O
AV12	I/O	I/O
AV14	I/O	I/O
AV16	I/O	I/O
AV18	I/O	I/O
AV20	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
AV22	I/O	I/O
AV24	I/O	I/O
AV26	N.C.	N.C.
AV28	I/O	I/O
AV30	I/O	I/O
AV32	I/O (D6)	I/O (D6)
AV34	N.C.	N.C.
AV36	I/O	I/O
AV38	I/O	I/O
AU1	VCC	VCC
AU3	I/O, GCK6 (DOUT)	I/O, GCK6 (DOUT)
AU5	N.C.	N.C.
AU7	I/O (D1)	I/O (D1)
AU9	N.C.	I/O
AU11	I/O	I/O
AU13	N.C.	N.C.
AU15	N.C.	N.C.
AU17	N.C.	I/O
AU19	I/O (D3)	I/O (D3)
AU21	I/O	I/O
AU23	I/O	I/O
AU25	N.C.	N.C.
AU27	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
AU29	I/O	I/O
AU31	I/O	I/O
AU33	I/O	I/O
AU35	I/O	I/O
AU37	N.C.	N.C.
AU39	GND	GND
AT2	N.C.	N.C.
AT4	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
AT6	GND	GND
AT8	I/O	I/O
AT10	I/O	I/O
AT12	I/O	I/O
AT14	GND	GND
AT16	I/O	I/O
AT18	I/O	I/O
AT20	GND	GND
AT22	I/O	I/O
AT24	I/O	I/O
AT26	GND	GND
AT28	I/O, FCLK3	I/O, FCLK3
AT30	N.C.	I/O
AT32	I/O	I/O
AT34	VCC	VCC
AT36	I/O, GCK4	I/O, GCK4
AT38	I/O	I/O
AR1	I/O	I/O
AR3	I/O	I/O
AR5	CCLK	CCLK
AR7	I/O	I/O
AR9	I/O	I/O
AR11	I/O	I/O
AR13	I/O, FCLK4	I/O, FCLK4
AR15	I/O (D2)	I/O (D2)
AR17	I/O	I/O
AR19	I/O	I/O
AR21	I/O	I/O
AR23	I/O	I/O
AR25	I/O	I/O
AR27	I/O	I/O
AR29	I/O	I/O
AR31	I/O	I/O
AR33	I/O	I/O
AR35	DONE	DONE
AR37	N.C.	N.C.
AR39	I/O	I/O
AP2	I/O	I/O
AP4	VCC	VCC
AP6	I/O (D0, DIN)	I/O (D0, DIN)
AP8	N.C.	N.C.
AP10	I/O	I/O
AP12	I/O	I/O

PG411 Pin	XC4036EX/XL	XC4044EX/XL
AP14	I/O	I/O
AP16	I/O	I/O
AP18	I/O	I/O
AP20	I/O (D4)	I/O (D4)
AP22	I/O	I/O
AP24	I/O (D5)	I/O (D5)
AP26	I/O	I/O
AP28	I/O	I/O
AP30	N.C.	I/O
AP32	I/O	I/O
AP34	I/O, GCK5	I/O, GCK5
AP36	GND	GND
AP38	N.C.	I/O
AN1	N.C.	I/O
AN3	I/O (A3)	I/O (A3)
AN5	N.C.	N.C.
AN7	O, TDO	O, TDO
AN9	I/O	I/O
AN31	I/O	I/O
AN33	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
AN35	I/O	I/O
AN37	I/O	I/O
AN39	I/O	I/O
AM2	I/O	I/O
AM4	I/O	I/O
AM6	I/O	I/O
AM8	I/O	I/O
AM32	I/O (D7)	I/O (D7)
AM34	I/O	I/O
AM36	I/O	I/O
AM38	I/O	I/O
AL1	GND	GND
AL3	I/O	I/O
AL5	I/O	I/O
AL7	I/O	I/O
AL33	I/O	I/O
AL35	N.C.	N.C.
AL37	I/O	I/O
AL39	VCC	VCC
AK2	N.C.	I/O
AK4	I/O	I/O
AK6	I/O (CS1, A2)	I/O (CS1, A2)
AK34	I/O	I/O
AK36	I/O	I/O
AK38	N.C.	I/O
AJ1	VCC	VCC
AJ3	I/O	I/O
AJ5	N.C.	N.C.
AJ35	I/O	I/O
AJ37	I/O	I/O
AJ39	GND	GND
AH2	I/O	I/O
AH4	I/O	I/O

PG411 Pin	XC4036EX/XL	XC4044EX/XL
AH6	I/O	I/O
AH34	I/O	I/O
AH36	I/O	I/O
AH38	I/O	I/O
AG1	I/O	I/O
AG3	I/O	I/O
AG5	I/O	I/O
AG35	I/O	I/O
AG37	I/O	I/O
AG39	I/O	I/O
AF2	N.C.	N.C.
AF4	GND	GND
AF6	I/O	I/O
AF34	I/O	I/O
AF36	GND	GND
AF38	N.C.	N.C.
AE1	I/O	I/O
AE3	I/O	I/O
AE5	I/O	I/O
AE35	I/O	I/O
AE37	I/O	I/O
AE39	I/O	I/O
AD2	I/O (A4)	I/O (A4)
AD4	I/O (A21)	I/O (A21)
AD6	I/O	I/O
AD34	I/O	I/O
AD36	I/O	I/O
AD38	I/O	I/O
AC1	I/O	I/O
AC3	N.C.	I/O
AC5	I/O	I/O
AC35	I/O	I/O
AC37	I/O	I/O
AC39	N.C.	I/O
AB2	N.C.	I/O
AB4	I/O (A5)	I/O (A5)
AB6	I/O	I/O
AB34	I/O	I/O
AB36	I/O	I/O
AB38	I/O	I/O
AA1	GND	GND
AA3	I/O (A6)	I/O (A6)
AA5	I/O (A20)	I/O (A20)
AA35	I/O	I/O
AA37	N.C.	I/O
AA39	VCC	VCC
Y2	I/O (A9)	I/O (A9)
Y4	GND	GND
Y6	I/O (A7)	I/O (A7)
Y34	I/O	I/O
Y36	GND	GND
Y38	N.C.	I/O
W1	VCC	VCC

PG411 Pin	XC4036EX/XL	XC4044EX/XL
W3	I/O (A8)	I/O (A8)
W5	N.C.	I/O
W35	N.C.	I/O
W37	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
W39	GND	GND
V2	N.C.	I/O
V4	I/O (A19)	I/O (A19)
V6	I/O	I/O
V34	I/O	I/O
V36	I/O	I/O
V38	I/O	I/O
U1	I/O	I/O
U3	I/O (A10)	I/O (A10)
U5	I/O	I/O
U35	I/O	I/O
U37	I/O	I/O
U39	I/O	I/O
T2	I/O (A18)	I/O (A18)
T4	I/O	I/O
T6	I/O	I/O
T34	I/O	I/O
T36	I/O	I/O
T38	I/O	I/O
R1	I/O (A11)	I/O (A11)
R3	N.C.	N.C.
R5	I/O	I/O
R35	I/O	I/O
R37	I/O	I/O
R39	I/O	I/O
P2	I/O	I/O
P4	GND	GND
P6	I/O	I/O
P34	I/O	I/O
P36	GND	GND
P38	N.C.	N.C.
N1	I/O	I/O
N3	N.C.	N.C.
N5	I/O	I/O
N35	I/O	I/O
N37	I/O	I/O
N39	I/O	I/O
M2	I/O	I/O
M4	I/O	I/O
M6	I/O	I/O
M34	I/O	I/O
M36	I/O	I/O
M38	I/O	I/O
L1	GND	GND
L3	I/O	I/O
L5	N.C.	I/O
L35	N.C.	N.C.
L37	I/O	I/O
L39	VCC	VCC

PG411 Pin	XC4036EX/XL	XC4044EX/XL
K2	I/O	I/O
K4	I/O	I/O
K6	I/O	I/O
K34	I/O	I/O
K36	N.C.	I/O
K38	N.C.	I/O
J1	VCC	VCC
J3	I/O	I/O
J5	N.C.	I/O
J7	I/O	I/O
J33	I/O	I/O
J35	I/O	I/O
J37	I/O	I/O
J39	GND	GND
H2	I/O	I/O
H4	I/O (A12)	I/O (A12)
H6	I/O	I/O
H8	I/O, GCK1 (A16)	I/O, GCK1 (A16)
H32	I/O	I/O
H34	N.C.	N.C.
H36	I/O	I/O
H38	I/O	I/O
G1	I/O	I/O
G3	I/O (A13)	I/O (A13)
G5	N.C.	N.C.
G7	I/O, GCK8 (A15)	I/O, GCK8 (A15)
G9	I/O, TCK	I/O, TCK
G31	I/O	I/O
G33	I (M2)	I (M2)
G35	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
G37	I/O	I/O
G39	I/O	I/O
F2	N.C.	N.C.
F4	GND	GND
F6	I/O (A17)	i/O (A17)
F8	I/O	I/O
F10	I/O	I/O
F12	I/O	I/O
F14	I/O	I/O
F16	I/O	I/O
F18	N.C.	I/O
F20	I/O	I/O
F22	N.C.	I/O
F24	I/O	I/O
F26	I/O	I/O
F28	I/O	I/O
F30	I/O	I/O
F32	I/O	I/O
F34	I/O	I/O
F36	VCC	VCC
F38	I/O	I/O
E1	I/O	I/O
E3	I/O	I/O

PG411 Pin	XC4036EX/XL	XC4044EX/XL
E5	I/O (A14)	I/O (A14)
E7	N.C.	N.C.
E9	I/O	I/O
E11	I/O, TMS	I/O, TMS
E13	I/O	I/O
E15	I/O	I/O
E17	I/O	I/O
E19	I/O	I/O
E21	I/O	I/O
E23	N.C.	N.C.
E25	I/O	I/O
E27	I/O	I/O
E29	I/O	I/O
E31	I/O	I/O
E33	I/O	I/O
E35	I (M0)	I (M0)
E37	N.C.	N.C.
E39	I/O	I/O
D2	I/O	I/O
D4	I/O	I/O
D6	VCC	VCC
D8	N.C.	I/O
D10	I/O	I/O
D12	N.C.	N.C.
D14	GND	GND
D16	I/O	I/O
D18	I/O	I/O
D20	GND	GND
D22	I/O	I/O
D24	I/O	I/O
D26	GND	GND
D28	I/O	I/O
D30	N.C.	I/O
D32	N.C.	I/O
D34	GND	GND
D36	I/O, GCK3	I/O, GCK3
D38	I/O	I/O
C1	GND	GND
C3	I/O	I/O
C5	I/O	I/O
C7	N.C.	I/O
C9	I/O	I/O
C11	I/O, FCLK1	I/O, FCLK1
C13	I/O	I/O
C15	N.C.	I/O
C17	I/O	I/O
C19	I/O	I/O
C21	I/O	I/O
C23	N.C.	I/O
C25	N.C.	N.C.
C27	I/O	I/O
C29	I/O, FCLK2	I/O, FCLK2
C31	I/O	I/O

PG411 Pin	XC4036EX/XL	XC4044EX/XL
C33	N.C.	N.C.
C35	I/O	I/O
C37	I/O (HDC)	I/O (HDC)
C39	VCC	VCC
B2	I/O, TDI	I/O, TDI
B4	I/O	I/O
B6	N.C.	N.C.
B8	I/O	I/O
B10	I/O	I/O
B12	I/O	I/O
B14	I/O	I/O
B16	I/O	I/O
B18	I/O	I/O
B20	I/O	I/O
B22	I/O	I/O
B24	I/O	I/O
B26	I/O	I/O
B28	I/O	I/O
B30	I/O	I/O
B32	I/O	I/O
B34	N.C.	N.C.
B36	I/O, GCK2	I/O, GCK2
B38	I/O	I/O
A3	VCC	VCC
A5	I/O	I/O
A7	I/O	I/O
A9	GND	GND
A11	VCC	VCC
A13	N.C.	N.C.
A15	I/O	I/O
A17	I/O	I/O
A19	GND	GND
A21	VCC	VCC
A23	I/O	I/O
A25	I/O	I/O
A27	I/O	I/O
A29	GND	GND
A31	VCC	VCC
A33	I/O	I/O
A35	I/O	I/O
A37	GND	GND
A39	O (M1)	O (M1)

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

BG432 Package Pinouts

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
AL1	VCC	VCC	VCC
AL2	GND	GND	GND
AL3	GND	GND	GND
AL4	I/O	I/O	I/O
AL5	I/O	I/O	I/O
AL6	I/O	I/O	I/O
AL7	GND	GND	GND
AL8	I/O	I/O	I/O
AL9	GND	GND	GND
AL10	I/O	I/O	I/O
AL11	VCC	VCC	VCC
AL12	I/O	I/O	I/O
AL13	I/O	I/O	I/O
AL14	GND	GND	GND
AL15	N.C.	I/O	I/O
AL16	I/O	I/O	I/O
AL17	N.C.	I/O	I/O
AL18	GND	GND	GND
AL19	I/O	I/O	I/O
AL20	I/O	I/O	I/O
AL21	VCC	VCC	VCC
AL22	I/O	I/O	I/O
AL23	GND	GND	GND
AL24	I/O	I/O	I/O
AL25	GND	GND	GND
AL26	I/O	I/O	I/O
AL27	I/O	I/O	I/O
AL28	I/O	I/O	I/O
AL29	GND	GND	GND
AL30	GND	GND	GND
AL31	VCC	VCC	VCC
AK1	GND	GND	GND
AK2	GND	GND	GND
AK3	I/O	I/O	I/O
AK4	I/O	I/O	I/O
AK5	I/O	I/O	I/O
AK6	I/O	I/O	I/O
AK7	I/O	I/O	I/O
AK8	I/O	I/O	I/O
AK9	I/O	I/O	I/O
AK10	I/O	I/O	I/O
AK11	N.C.	N.C.	I/O
AK12	I/O	I/O	I/O
AK13	I/O	I/O	I/O
AK14	I/0	I/O	I/O
AK15	I/O	I/O	I/O
AK16	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
AK17	N.C.	I/O	I/O
AK18	I/O	I/O	I/O
AK19	I/O	I/O	I/O
AK20	I/O	I/O	I/O
AK21	I/O	I/O	I/O
AK22	I/O	I/O	I/O
AK23	I/O	I/O	I/O
AK24	N.C.	I/O	I/O
AK25	I/O	I/O	I/O
AK26	I/O	I/O	I/O
AK27	N.C.	N.C.	I/O
AK28	I/O	I/O	I/O
AK29	I/O, GCK3	I/O, GCK3	I/O, GCK3
AK30	GND	GND	GND
AK31	GND	GND	GND
AJ1	GND	GND	GND
AJ2	I/O (D7)	I/O (D7)	I/O (D7)
AJ3	VCC	VCC	VCC
AJ4	I/O, GCK4	I/O, GCK4	I/O, GCK4
AJ5	N.C.	N.C.	I/O
AJ6	I/O	I/O	I/O
AJ7	I/O	I/O	I/O
AJ8	N.C.	I/O	I/O
AJ9	I/O	I/O	I/O
AJ10	I/O	I/O	I/O
AJ11	I/O	I/O	I/O
AJ12	N.C.	N.C.	I/O
AJ13	I/O	I/O	I/O
AJ14	I/O	I/O	I/O
AJ15	N.C.	I/O	I/O
AJ16	I/O	I/O	I/O
AJ17	I/O	I/O	I/O
AJ18	I/O	I/O	I/O
AJ19	I/O	I/O	I/O
AJ20	N.C.	N.C.	I/O
AJ21	I/O	I/O	I/O
AJ22	I/O	I/O	I/O
AJ23	I/O	I/O	I/O
AJ24	I/O	I/O	I/O
AJ25	I/O	I/O	I/O
AJ26	N.C.	N.C.	I/O
AJ27	I/O	I/O	I/O
AJ28	I (M2)	I (M2)	I (M2)
AJ29	VCC	VCC	VCC
AJ30	I/O, GCK2	I/O, GCK2	I/O, GCK2
AJ31	GND	GND	GND
AH1	I/O	I/O	I/O
AH2	I/O	I/O	I/O
AH3	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
AH4	DONE	DONE	DONE
AH5	I/O	I/O	I/O
AH6	N.C.	N.C.	I/O
AH7	I/O	I/O	I/O
AH8	I/O	I/O	I/O
AH9	N.C.	I/O	I/O
AH10	I/O	I/O	I/O
AH11	VCC	VCC	VCC
AH12	I/O	I/O	I/O
AH13	I/O	I/O	I/O
AH14	I/O	I/O	I/O
AH15	I/O	I/O	I/O
AH16	GND	GND	GND
AH17	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
AH18	I/O	I/O	I/O
AH19	N.C.	N.C.	I/O
AH20	I/O	I/O	I/O
AH21	VCC	VCC	VCC
AH22	I/O	I/O	I/O
AH23	N.C.	I/O	I/O
AH24	I/O	I/O	I/O
AH25	I/O	I/O	I/O
AH26	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
AH27	I/O (HDC)	I/O (HDC)	I/O (HDC)
AH28	I (M0)	I (M0)	I (M0)
AH29	O (M1)	O (M1)	O (M1)
AH30	I/O	I/O	I/O
AH31	I/O	I/O	I/O
AG1	N.C.	N.C.	I/O
AG2	I/O	I/O	I/O
AG3	I/O	I/O	I/O
AG4	I/O, GCK5	I/O, GCK5	I/O, GCK5
AG28	I/O	I/O	I/O
AG29	I/O	I/O	I/O
AG30	I/O	I/O	I/O
AG31	I/O	I/O	I/O
AF1	I/O (D6)	I/O (D6)	I/O (D6)
AF2	I/O	I/O	I/O
AF3	I/O	I/O	I/O
AF4	I/O	I/O	I/O
AF28	I/O	I/O	I/O
AF29	N.C.	N.C.	I/O
AF30	N.C.	N.C.	I/O
AF31	I/O	I/O	I/O
AE1	GND	GND	GND
AE2	I/O	I/O	I/O
AE3	I/O	I/O	I/O
AE4	N.C.	N.C.	I/O
AE28	I/O	I/O	I/O
AE29	I/O	I/O	I/O
AE30	I/O	I/O	I/O
AE31	GND	GND	GND
AD1	I/O	I/O	I/O
AD2	N.C.	I/O	I/O
AD3	I/O	I/O	I/O
AD4	I/O	I/O	I/O
AD28	I/O	I/O	I/O
AD29	I/O	I/O	I/O
AD30	N.C.	I/O	I/O
AD31	N.C.	I/O	I/O
AC1	GND	GND	GND
AC2	I/O	I/O	I/O
AC3	I/O	I/O	I/O
AC4	N.C.	I/O	I/O
AC28	I/O	I/O	I/O
AC29	I/O	I/O	I/O
AC30	I/O	I/O	I/O
AC31	GND	GND	GND
AB1	I/O, FCLK3	I/O, FCLK3	I/O, FCLK3
AB2	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
AB3	I/O	I/O	I/O
AB4	I/O	I/O	I/O
AB28	I/O	I/O	I/O
AB29	I/O, FCLK2	I/O, FCLK2	I/O, FCLK2
AB30	I/O	I/O	I/O
AB31	I/O	I/O	I/O
AA1	VCC	VCC	VCC
AA2	I/O (D5)	I/O (D5)	I/O (D5)
AA3	I/O	I/O	I/O
AA4	VCC	VCC	VCC
AA28	VCC	VCC	VCC
AA29	I/O	I/O	I/O
AA30	I/O	I/O	I/O
AA31	VCC	VCC	VCC
Y1	N.C.	N.C.	I/O
Y2	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
Y3	I/O	I/O	I/O
Y4	I/O	I/O	I/O
Y28	I/O	I/O	I/O
Y29	I/O	I/O	I/O
Y30	I/O	I/O	I/O
Y31	N.C.	N.C.	I/O
W1	N.C.	N.C.	I/O
W2	N.C.	I/O	I/O
W3	I/O	I/O	I/O
W4	I/O	I/O	I/O
W28	N.C.	N.C.	I/O
W29	I/O	I/O	I/O
W30	I/O	I/O	I/O
W31	N.C.	I/O	I/O
V1	GND	GND	GND
V2	N.C.	I/O	I/O
V3	I/O	I/O	I/O
V4	I/O	I/O	I/O
V28	N.C.	I/O	I/O
V29	I/O	I/O	I/O
V30	I/O	I/O	I/O
V31	GND	GND	GND
U1	I/O	I/O	I/O
U2	I/O	I/O	I/O
U3	I/O	I/O	I/O
U4	I/O	I/O	I/O
U28	I/O	I/O	I/O
U29	I/O	I/O	I/O
U30	I/O	I/O	I/O
U31	I/O	I/O	I/O
T1	I/O (D4)	I/O (D4)	I/O (D4)
T2	I/O	I/O	I/O
T3	I/O (D3)	I/O (D3)	I/O (D3)
T4	GND	GND	GND
T28	GND	GND	GND
T29	I/O	I/O	I/O
T30	I/O	I/O	I/O
T31	I/O	I/O	I/O
R1	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
R2	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
R3	I/O	I/O	I/O
R4	I/O	I/O	I/O
R28	I/O	I/O	I/O
R29	I/O	I/O	I/O
R30	I/O	I/O	I/O
R31	I/O	I/O	I/O
P1	GND	GND	GND
P2	I/O	I/O	I/O
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P28	I/O	I/O	I/O
P29	I/O	I/O	I/O
P30	I/O	I/O	I/O
P31	GND	GND	GND
N1	N.C.	I/O	I/O
N2	N.C.	I/O	I/O
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N28	I/O	I/O	I/O
N29	N.C.	I/O	I/O
N30	N.C.	I/O	I/O
N31	I/O	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	N.C.	N.C.	I/O
M4	N.C.	N.C.	I/O
M28	N.C.	N.C.	I/O
M29	I/O	I/O	I/O
M30	N.C.	N.C.	I/O
M31	I/O	I/O	I/O
L1	VCC	VCC	VCC
L2	I/O (D2)	I/O (D2)	I/O (D2)
L3	I/O	I/O	I/O
L4	VCC	VCC	VCC
L28	VCC	VCC	VCC
L29	I/O	I/O	I/O
L30	I/O	I/O	I/O
L31	VCC	VCC	VCC
K1	I/O	I/O	I/O
K2	I/O, FCLK4	I/O, FCLK4	I/O, FCLK4
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K28	I/O, FCLK1	I/O, FCLK1	I/O, FCLK1
K29	I/O	I/O	I/O
K30	I/O, TMS	I/O, TMS	I/O, TMS
K31	I/O	I/O	I/O
J1	GND	GND	GND
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J28	I/O	I/O	I/O
J29	I/O	I/O	I/O
J30	I/O	I/O	I/O
J31	GND	GND	GND
H1	I/O	I/O	I/O
H2	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H28	I/O	I/O	I/O
H29	I/O	I/O	I/O
H30	I/O	I/O	I/O
H31	I/O	I/O	I/O
G1	GND	GND	GND
G2	I/O	I/O	I/O
G3	N.C.	I/O	I/O
G4	I/O (D1)	I/O (D1)	I/O (D1)
G28	I/O	I/O	I/O
G29	I/O	I/O	I/O
G30	I/O	I/O	I/O
G31	GND	GND	GND
F1	N.C.	I/O	I/O
F2	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)
F3	I/O	I/O	I/O
F4	N.C.	N.C.	I/O
F28	N.C.	N.C.	I/O
F29	N.C.	N.C.	I/O
F30	N.C.	I/O	I/O
F31	N.C.	I/O	I/O
E1	I/O	I/O	I/O
E2	N.C.	N.C.	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E28	I/O	I/O	I/O
E29	I/O	I/O	I/O
E30	I/O	I/O	I/O
E31	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O, GCK6 (DOUT)	I/O, GCK6 (DOUT)	I/O, GCK6 (DOUT)
D4	CCLK	CCLK	CCLK
D5	I/O, GCK7 (A1)	I/O, GCK7 (A1)	I/O, GCK7 (A1)
D6	N.C.	N.C.	I/O
D7	I/O (A3)	I/O (A3)	I/O (A3)
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	VCC	VCC	VCC
D12	I/O	I/O	I/O
D13	N.C.	N.C.	I/O
D14	I/O	I/O	I/O
D15	I/O	I/O	I/O
D16	GND	GND	GND
D17	I/O (A8)	I/O (A8)	I/O (A8)
D18	I/O (A18)	I/O (A18)	I/O (A18)
D19	I/O	I/O	I/O
D20	N.C.	N.C.	I/O
D21	VCC	VCC	VCC
D22	I/O	I/O	I/O
D23	N.C.	I/O	I/O
D24	I/O (A12)	I/O (A12)	I/O (A12)

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
D25	I/O	I/O	I/O
D26	N.C.	N.C.	I/O
D27	I/O	I/O	I/O
D28	I/O, GCK8 (A15)	I/O, GCK8 (A15)	I/O, GCK8 (A15)
D29	I/O, GCK1 (A16)	I/O, GCK1 (A16)	I/O, GCK1 (A16)
D30	I/O, TDI	I/O, TDI	I/O, TDI
D31	I/O, TCK	I/O, TCK	I/O, TCK
C1	GND	GND	GND
C2	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
C3	VCC	VCC	VCC
C4	O, TDO	O, TDO	O, TDO
C5	I/O	I/O	I/O
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	N.C.	N.C.	N.C.
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O
C14	I/O (A4)	I/O (A4)	I/O (A4)
C15	I/O (A21)	I/O (A21)	I/O (A21)
C16	N.C.	I/O	I/O
C17	N.C.	I/O	I/O
C18	I/O (A19)	I/O (A19)	I/O (A19)
C19	I/O (A11)	I/O (A11)	I/O (A11)
C20	I/O	I/O	I/O
C21	I/O	I/O	I/O
C22	I/O	I/O	I/O
C23	I/O	I/O	I/O
C24	I/O	I/O	I/O
C25	I/O	I/O	I/O
C26	I/O	I/O	I/O
C27	I/O	I/O	I/O
C28	I/O (A14)	I/O (A14)	I/O (A14)
C29	VCC	VCC	VCC
C30	I/O (A17)	I/O (A17)	I/O (A17)
C31	GND	GND	GND
B1	GND	GND	GND
B2	GND	GND	GND
B3	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	I/O	I/O	I/O
B8	N.C.	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	I/O	I/O	I/O
B12	N.C.	N.C.	I/O
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	I/O (A20)	I/O (A20)	I/O (A20)
B16	I/O (A6)	I/O (A6)	I/O (A6)
B17	N.C.	I/O	I/O
B18	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
B19	I/O (A10)	I/O (A10)	I/O (A10)
B20	I/O	I/O	I/O
B21	N.C.	N.C.	I/O
B22	I/O	I/O	I/O
B23	I/O	I/O	I/O
B24	I/O	I/O	I/O
B25	N.C.	I/O	I/O
B26	I/O (A13)	I/O (A13)	I/O (A13)
B27	I/O	I/O	I/O
B28	I/O	I/O	I/O
B29	I/O	I/O	I/O
B30	GND	GND	GND
B31	GND	GND	GND
A1	VCC	VCC	VCC
A2	GND	GND	GND
A3	GND	GND	GND
A4	N.C.	N.C.	I/O
A5	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
A6	I/O	I/O	I/O
A7	GND	GND	GND
A8	N.C.	I/O	I/O
A9	GND	GND	GND
A10	I/O	I/O	I/O
A11	VCC	VCC	VCC
A12	I/O	I/O	I/O
A13	I/O (A5)	I/O (A5)	I/O (A5)
A14	GND	GND	GND
A15	N.C.	I/O	I/O
A16	I/O (A7)	I/O (A7)	I/O (A7)
A17	I/O (A9)	I/O (A9)	I/O (A9)
A18	GND	GND	GND
A19	I/O	I/O	I/O
A20	I/O	I/O	I/O
A21	VCC	VCC	VCC
A22	I/O	I/O	I/O
A23	GND	GND	GND
A24	I/O	I/O	I/O
A25	GND	GND	GND
A26	I/O	I/O	I/O
A27	I/O	I/O	I/O
A28	N.C.	N.C.	I/O
A29	GND	GND	GND
A30	GND	GND	GND
A31	VCC	VCC	VCC

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

Product Availability

Table 25 - Table 27 show the planned packages and speed grades for XC4000-Series devices. Call your local sales office for the latest availability information, or see the Xilinx WEBLINX at http://www.xilinx.com for the latest revision of the specifications.

Table 25: Component Availability Chart for XC4000E FPGAs

	Speed Grade	PC 84	PQ 100	VQ 100	PG 120	TQ 144	PG 156	PQ 160	CB 164	PG 191	CB 196	PQ 208	HQ 208	PG 223	BG 225	CB 228	PQ 240	HQ 240	PG 299	HQ 304
XC 4003E	-4	C I	C I	C I	C I															
	-3	C I	C I	C I	C I															
	-2	C	C	C	C															
XC 4005E	-4	C I	C I			C I	C I M B	C I	M B			C I								
	-3	C I	C I			C I	C I	C I				C I								
	-2	C	C			C	C	C				C								
XC 4006E	-4	C I				C I	C I	C I				C I								
	-3	C I				C I	C I	C I				C I								
	-2	C				C	C	C				C								
XC 4008E	-4	C I						C I		C I		C I								
	-3	C I						C I		C I		C I								
	-2	C						C		C		C								
XC 4010E	-4	C I						C I		C I MB	MB	C I	C I		C I					
	-3	C I						C I		C I		C I	C I		C I					
	-2	C						C		C		C	C		C					
XC 4013E	-4							C I				C I	C I	C I M B	C I	M B	C I	C I		
	-3							C I				C I	C I	C I	C I		C I	C I		
	-2							C				C	C	C	C		C	C		
XC 4020E	-4												C I	C I				C I		
	-3												C I	C I				C I		
	-2												C	C				C		
XC 4025E	-4													C I		M B		C I	C I M B	C I
	-3													C I				C I	C I	C I
	-2													C				C	C	C

C = Commercial, T_J = 0° to +85° C
I = Industrial, T_J = -40° to +100° C
M = Mil Temp, T_C = -55° to +125° C
B = MIL-STD-883C Class B, T_C = -55° to +125° C
Shaded device/package combinations are not supported.

Table 26: Component Availability Chart for XC4000EX FPGAs

	Speed Grade	HQ208	HQ240	PG299	HQ304	BG352	PG411	BG432
XC4028EX	-4	C I	C I	C I	C I	C I		
	-3	C	C	C	C	C		
XC4036EX	-4				C I		C I	C I
	-3				C		C	C
XC4044EX	-4						C I	C I
	-3						C	C

C = Commercial, T_J = 0° to +85° C
I = Industrial, T_J = -40° to +100° C
M = Mil Temp, T_C = -55° to +125° C
B = MIL-STD-883C Class B, T_C = -55° to +125° C
Shaded device/package combinations are not supported.

Table 27: Component Availability Chart for XC4000L and XC4000XL FPGAs

	Speed Grade	PC 84	TQ 176	PQ 208	HQ 208	BG 225	PQ 240	HQ 240	PG 299	HQ 304	BG 352	PG 411	BG 432	PG 475
XC4005L	-6	C		C										
	-5	C		C										
	-4													
XC4010L	-6	C	C	C										
	-5	C	C	C										
	-4													
XC4013L	-6			C		C	C							
	-5			C		C	C							
	-4													
XC4028XL					C			C	C	C	C			
XC4036XL										C		C	C	
XC4044XL												C	C	
XC4052XL												C	C	
XC4062XL														C

C = Commercial, T_J = 0° to +85° C
I = Industrial, T_J = -40° to +100° C
M = Mil Temp, T_C = -55° to +125° C
B = MIL-STD-883C Class B, T_C = -55° to +125° C
Shaded device/package combinations are not supported.
Speed grades for the XC4000XL have not yet been determined.

User I/O Per Package

Maximum available user I/O for each device/package combination is shown in Table 28 - Table 30.

Pinout tables for XC4000-Series devices follow. Pinout data is offered in two forms, as device-specific and package-specific tables. Device-specific tables include all packages for each XC4000-Series device. They follow the pad locations around the die, and include boundary scan register locations. Package-specific tables include all XC4000-Series devices available in a given package. These tables are especially useful in determining which pads should be avoided, in case of a future transition to a different device in the same package.

All pinouts defined at the time of publication are included in these tables. Additional information may be available. Call your local sales office or see the Xilinx WEBLINX at http://www.xilinx.com for the latest information.

Table 28: Maximum User I/O for XC4000E Device/Package Combinations

No. of Pins	Package (Code)	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E
Maximum User I/O		**80**	**112**	**128**	**144**	**160**	**192**	**224**	**256**
84	PLCC (PC)	61	61	61	61	61			
100	PQFP (PQ)	77	77						
	VQFP (VQ)	77							
120	PGA (PG)	80							
144	TQFP (TQ)		112	113					
156	PGA (PG)		112	125					
160	PQFP (PQ)		112	128	129	129	129		
164	CBFP (CB)		112						
191	PGA (PG)				144	160			
196	CBFP (CB)					160			
208	PQFP (PQ)		112	128	144	160	160		
	HQFP (HQ)					160	160	160	
223	PGA (PG)						192	192	192
225	BGA (BG)					160	192		
228	CBFP (CB)						192		192
240	PQFP (PQ)						192		
	HQFP (HQ)						192	193	193
299	PGA (PG)								256
304	HQFP (HQ)								256

Note: This table includes standard user-programmable I/O. It also includes the TDI, TCK, and TMS pins, which can function as user-programmable I/O if not used for boundary scan. In addition to the I/O listed in this table, the M0 and M2 pins can be used as inputs only; the M1 and TDO pins can be used as outputs only. All of these pins must be called out using special library symbols. The XACT software does not use them by default. (See Table 18 on page 47.)

Table 29: Maximum User I/O for XC4000EX Device/Package Combinations

No. of Pins	Package (Code)	XC4028EX	XC4036EX	XC4044EX
Maximum User I/O		**256**	**288**	**320**
208	HQFP (HQ)	160		
240	HQFP (HQ)	193		
299	PGA (PG)	256		
304	HQFP (HQ)	256	256	
352	BGA (BG)	256		
411	PGA (PG)		288	320
432	BGA (BG)		288	320

Note: This table includes standard user-programmable I/O. It also includes the TDI, TCK, and TMS pins, which can function as user-programmable I/O if not used for boundary scan. In addition to the I/O listed in this table, the M0 and M2 pins can be used as inputs only; the M1 and TDO pins can be used as outputs only. All of these pins must be called out using special library symbols. The XACT software does not use them by default. (See Table 18 on page 47.)

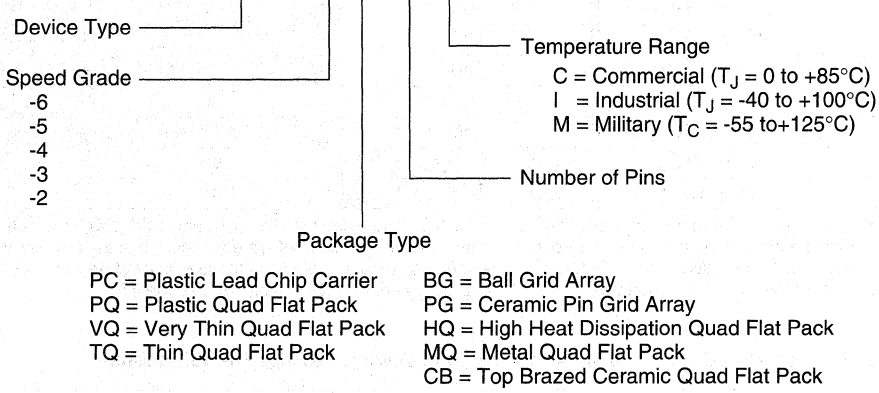
Table 30: Maximum User I/O for XC4000L and XC4000XL Device/Package Combinations

No. of Pins	Package (Code)	XC4005L	XC4010L	XC4013L	XC4028XL	XC4036XL	XC4044XL	XC4052XL	XC4062XL
Maximum User I/O		**112**	**160**	**192**	**256**	**288**	**320**	**352**	**384**
84	PLCC (PC)	61	61						
176	TQFP (TQ)		153						
208	PQFP (PQ)	112	160	160					
208	HQFP (HQ)				160				
225	BGA (BG)			192					
240	PQFP (PQ)			192					
240	HQFP (HQ)				193				
299	PGA (PG)				256				
304	HQFP (HQ)				256	256			
352	BGA (BG)				256				
411	PGA (PG)					288	320	352	
432	BGA (BG)					288	320	352	
475	PGA (PG)								384

Note: This table includes standard user-programmable I/O. It also includes the TDI, TCK, and TMS pins, which can function as user-programmable I/O if not used for boundary scan. In addition to the I/O listed in this table, the M0 and M2 pins can be used as inputs only; the M1 and TDO pins can be used as outputs only. All of these pins must be called out using special library symbols. The XACT software does not use them by default. (See Table 18 on page 47.)

Ordering Information

Example: XC4013E-3HQ240C



X6750

XC5200 Field Programmable Gate Arrays

XC5200L Field Programmable Gate Arrays

XC5200
Field Programmable Gate Arrays

August 6, 1996 (Version 4.01) — Preliminary Product Specification

Features

- High-density family of Field-Programmable Gate Arrays (FPGAs)
- Design- and process-optimized for low cost
  - 0.6-µm three-layer metal (TLM) process
- System performance up to 50 MHz
- SRAM-based, in-system reprogrammable architecture
- Flexible architecture with abundant routing resources
  - VersaBlock™ logic module
  - VersaRing™ I/O interface
  - Dedicated cell-feedthrough path
  - Hierarchical interconnect structure
  - Extensive registers/latches
  - Dedicated carry logic for arithmetic functions
  - Cascade chain for wide input functions
  - Dedicated IEEE 1149.1 boundary-scan logic
  - Internal 3-state bussing capability
  - Four global low-skew clock or signal distribution nets
  - Globally selectable CMOS or TTL input thresholds
  - Output slew-rate control
  - 8-mA sink current per output
- Configured by loading binary file
  - Unlimited reprogrammability
  - Seven programming modes, including high-speed Express™ mode
- 100% factory tested
- 100% footprint compatibility for common packages
- Fully supported by XACT*step*™ Development System
  - Includes complete support for XACT-Performance™, X-BLOX™, Unified Libraries, Relationally Placed Macros (RPMs), XDelay, and XChecker™
  - Wide selection of PC and workstation platforms
  - Interfaces to more than 100 third-party CAE tools

Description

The XC5200 Field-Programmable Gate Array Family is engineered to deliver the lowest cost of any FPGA family. By optimizing the new XC5200 architecture for three-layer metal (TLM) technology and a 0.6-µm CMOS SRAM process, dramatic advances have been made in silicon efficiency. These advances position the XC5200 family as a cost-effective, high-volume alternative to gate arrays.

Building on experiences gained with three previous successful SRAM FPGA families, the XC5200 family brings a robust feature set to high-density programmable logic design. The VersaBlock logic module, the VersaRing I/O interface, and a rich hierarchy of interconnect resources combine to enhance design flexibility and reduce time-to-market.

Complete support for the XC5200 family is delivered through the familiar XACT*step* software environment. The XC5200 family is fully supported on popular workstation and PC platforms. Popular design entry methods are fully supported, including ABEL, schematic capture, and synthesis. Designers utilizing logic synthesis can use their existing tools to design with the XC5200 devices.

Table 1: Initial XC5200 Field-Programmable Gate Array Family Members

Device	XC5202	XC5204	XC5206	XC5210	XC5215
Max Logic Gates	3,000	6,000	10,000	16,000	23,000
Typical Gate Range	2,000 - 3,000	4,000 - 6,000	6,000 - 10,000	10,000 - 16,000	15,000 - 23,000
VersaBlock Array	8 x 8	10 x 12	14 x 14	18 x 18	22 x 22
Number of CLBs	64	120	196	324	484
Number of Flip-Flops	256	480	784	1,296	1,936
Number of I/Os	84	124	148	196	244
TBUFs per Horizontal Longline	10	14	16	20	24

XC5200 Family Compared to XC4000 and XC3000 Series

For readers already familiar with the XC4000 and XC3000 gate array series, this section describes significant differences between them and the XC5200 family. Unless otherwise indicated, comparisons refer to both XC4000 and XC3000 devices.

Configurable Logic Block (CLB) Resources

Each XC5200 CLB contains four independent 4-input function generators and four registers, which are configured as four independent Logic Cells™ (LCs). The output from the function generator in each LC can be brought out as a CLB output and/or drive the D input of the register. A pair of LCs can be combined to form a 5-input function generator.

There are four direct feedthrough paths for each XC5200 CLB, one per LC. These paths provide extra data input lines or serve as additional local routes without consuming any logic resources.

The registers in each XC5200 LC are optionally configurable as edge-triggered D-type flip-flops or as transparent level-sensitive latches.

The XC5200 CLB includes dedicated carry logic that provides fast arithmetic carry capability. The dedicated carry logic may also be used to cascade function generators for implementing wide arithmetic functions.

XC4000 family: XC5200 devices have no wide edge decoders.

XC4000 family: XC5200 dedicated carry logic differs from that of the XC4000 family in that the sum is generated in an additional function generator in the adjacent column. An XC5200 device thus uses twice as many function generators for adders, subtracters, accumulators, and some counters. Note, however, that a loadable up/down counter requires the same number of function generators in both families.

XC4000 family: XC5200 lookup tables cannot be used as RAM.

Table 2: Four Generations of Xilinx Field-Programmable Gate Array Families

Parameter	XC5200	XC4000	XC3000A/XC3100A	XC2000
Function generators per CLB	4	3	2	2
Logic inputs per CLB	20	9	5	4
Logic outputs per CLB	12	4	2	2
Low-skew global buffers	4	8	2	2
Single-length lines	10	8	5	4
Double-length lines	4	4	0	0
Longlines	8	6	3	2
Direct connects	8	0	2	2
VersaRing	yes	no	no	no
User RAM	no	yes	no	no
Dedicated decoders	no	yes	no	no
Cascade chain	yes	no	no	no
Fast carry logic	yes	yes	no	no
Internal 3-state drivers	yes	yes	yes	no
IEEE boundary scan	yes	yes	no	no
Output slew-rate control	yes	yes	yes	no
Power-down option	no	no	yes	yes
Crystal oscillator circuit	no	no	yes	yes

Input/Output Block (IOB) Resources

The XC5200 family maintains footprint compatibility with the XC4000 family, but not with the XC3000 family.

The XC5200 IOB does not include flip-flops or latches. The XC5200 family provides direct connections from each IOB to the registers in the adjacent CLB in order to emulate IOB registers.

The XC5200 IOB provides a programmable delay element to control input set-up time. This element can be used to avoid potential hold-time problems.

Each XC5200 IOB is capable of 8-mA source and sink currents.

IEEE 1149.1-type boundary scan is supported in each XC5200 IOB.

XC3000 family: Each XC5200 IOB has access to tristatable Longlines by means of its own 3-state buffer (TBUF).

Routing Resources

The XC5200 family provides a flexible coupling of logic and local routing resources called the VersaBlock. The XC5200 VersaBlock element includes the CLB, a Local Interconnect Matrix (LIM), and direct connects to neighboring VersaBlocks.

Each XC5200 VersaBlock element has complete intra-CLB routing, the LIM, and offers four direct routing connections to each of the four neighboring CLBs. Any function generator or flip-flop thus has unrestricted connectivity to 19 other function generators or flip-flops: three in its own CLB, and 16 in the adjacent CLBs. These direct connects do not compete with the general routing resources (see Table 2).

There is a special routing resource, the VersaRing, between the outer edge of the core CLB array and the ring of IOBs, providing added routability to the I/O. This feature is particularly important for designs that require a fixed pinout prior to completion.

The XC5200 provides four global buffers for clocking or high-fanout control signals. Each buffer may be sourced by means of its dedicated pad or from any internal source.

Each XC5200 TBUF can drive up to two horizontal Longlines.

There are no internal pull-ups for XC5200 Longlines.

Configuration and Readback

XC4000 family: The XC5200 family provides a global reset but not a global set.

XC5200 devices use a different configuration process than that of the XC3000 family, but use the same process as the XC4000 family. The rest of this discussion compares XC5200 features with those of the XC3000 family only.

Although their configuration processes differ, XC5200 devices may be used in daisy chains with XC3000 devices.

The XC5200 PROGRAM pin is a single-function input pin that overrides all other inputs.

The XC5200 INIT pin also acts as a Configuration Error output.

XC5200 devices support two additional programming modes: Peripheral Synchronous and the new high-speed Express mode.

XC5200 start-up can be synchronized to any user clock by means of a configuration option.

The XC5200 family does not support Power-down, but offers a Global 3-state input that does not reset any flip-flops.

The XC5200 family does not provide an on-chip crystal oscillator amplifier, but it does provide an internal oscillator from which a variety of frequencies up to 16 MHz are available.

Readback in the XC5200 family either ignores the flip-flop content, thereby avoiding the need for masking, or it takes a snapshot of all flip-flops at the start of Readback.

Readback in the XC5200 family has the same polarity as Configuration, and can be aborted.

Architectural Overview

Figure 1 presents a simplified, conceptual overview of the XC5200 architecture. Similar to conventional FPGAs, the XC5200 family consists of programmable IOBs, programmable logic blocks, and programmable interconnect. Unlike other FPGAs, however, the logic and local routing resources of the XC5200 family are combined in flexible VersaBlocks. General-purpose routing connects to the VersaBlock through the General Routing Matrix (GRM).

VersaBlock: Abundant Local Routing Plus Versatile Logic

The basic logic element in each VersaBlock structure is the Logic Cell, shown in Figure 2. Each LC contains a 4-input function generator (F), a storage device (FD), and control logic. There are five independent inputs and three outputs to each LC. The independence of the inputs and outputs allows the software to maximize the resource utilization within each LC. Each Logic Cell also contains a direct feedthrough path that does not sacrifice the use of either the function generator or the register; this feature is a first for FPGAs. The storage device is configurable as either a D flip-flop or a latch. The control logic consists of carry logic for fast implementation of arithmetic functions, which can also be configured as a cascade chain allowing decode of very wide input functions.

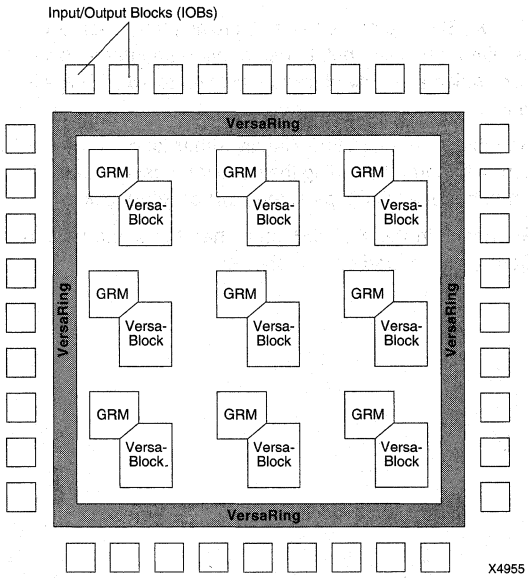


Figure 1: XC5200 Architectural Overview

The XC5200 CLB consists of four LCs, as shown in Figure 3. Each CLB has 20 independent inputs and 12 independent outputs. The top and bottom pairs of LCs can be configured to implement 5-input functions. The challenge of FPGA implementation software has always been to maximize the usage of logic resources. The XC5200 family addresses this issue by surrounding each CLB with two types of local interconnect — the Local Interconnect Matrix (LIM) and direct connects. These two interconnect resources, combined with the CLB, form the VersaBlock, represented in Figure 4.

The LIM provides 100% connectivity of the inputs and outputs of each LC in a given CLB. The benefit of the LIM is that no general routing resources are required to connect feedback paths within a CLB. The LIM connects to the GRM via 24 bidirectional nodes.

The direct connects allow immediate connections to neighboring CLBs, once again without using any of the general interconnect. These two layers of local routing resource improve the granularity of the architecture, effectively making the XC5200 family a "sea of logic cells." Each VersaBlock has four 3-state buffers that share a common enable line and directly drive horizontal Longlines, creating robust on-chip bussing capability. The VersaBlock allows fast, local implementation of logic functions, effectively implementing user designs in a hierarchical fashion. These resources also minimize local routing congestion and improve the efficiency of the general interconnect, which is used for connecting larger groups of logic. It is this combination of both fine-grain and coarse-grain architecture attributes that maximize logic utilization in the XC5200 family. This symmetrical structure takes full advantage of the third metal layer, freeing the placement software to pack user logic optimally with minimal routing restrictions.

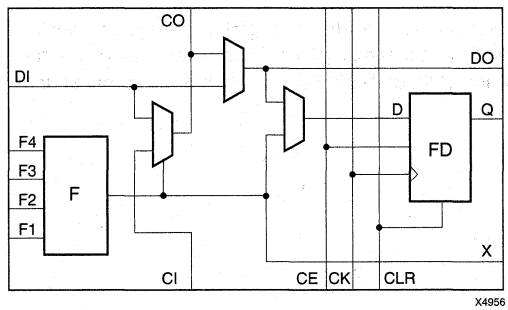


Figure 2: XC5200 Logic Cell (Four LCs per CLB)

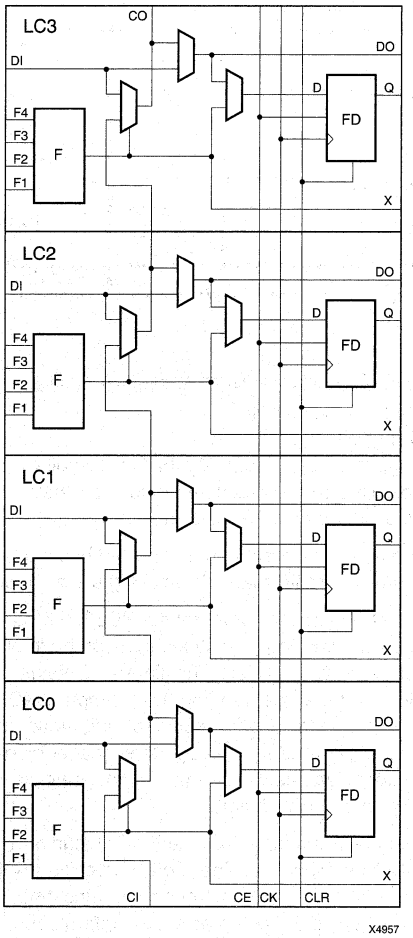


Figure 3: Configurable Logic Block

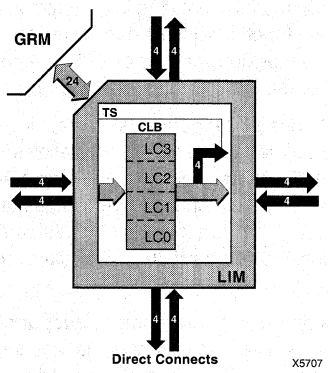


Figure 4: VersaBlock

VersaRing I/O Interface

The interface between the IOBs and core logic has been redesigned in the XC5200 family. The IOBs are completely decoupled from the core logic. The XC5200 IOBs contain dedicated boundary-scan logic for added board-level testability, but do not include input or output registers. This approach allows a maximum number of IOBs to be placed around the device, improving the I/O-to-gate ratio and decreasing the cost per I/O. A "freeway" of interconnect cells surrounding the device forms the VersaRing, which provides connections from the IOBs to the internal logic These incremental routing resources provide abundant connections from each IOB to the nearest VersaBlock, in addition to Longline connections surrounding the device. The VersaRing eliminates the historic trade-off between high logic utilization and pin placement flexibility. These incremental edge resources give users increased flexibility in preassigning (i.e., locking) I/O pins before completing their logic designs. This ability accelerates time-to-market, since PCBs and other system components can be manufactured concurrent with the logic design.

General Routing Matrix

The GRM is functionally similar to the switch matrices found in other architectures, but it is novel in its tight coupling to the logic resources contained in the VersaBlocks. Advanced simulation tools were used during the development of the XC5200 architecture to determine the optimal level of routing resources required. The XC5200 family contains six levels of interconnect hierarchy — a series of single-length lines, double-length lines, and Longlines all routed through the GRM. The direct connects, LIM, and logic-cell feedthrough are contained within each VersaBlock. Throughout the XC5200 interconnect, an efficient multiplexing scheme, in combination with three layer metal (TLM), was used to improve the overall efficiency of silicon usage.

Performance Overview

The XC5200 family has been benchmarked with many designs running synchronous clock rates up to 50 MHz. The performance of any design depends on the circuit to be implemented, and the delay through the combinatorial and sequential logic elements, plus the delay in the interconnect routing. Table 3 shows some performance numbers for representative circuits. A rough estimate of timing can be made by assuming 6 ns per logic level, which includes direct-connect routing delays. More accurate estimations can be made using the information in the Switching Characteristic Guideline section.

Table 3: Performance for Several Common Circuit Functions

Function	XC5200 Speed Grade			
	-6	-5	-4	-3
16-bit Decoder from Input Pad	9 ns	8 ns	7 ns	6 ns
24-bit Accumulator	32 MHz	39 MHz	45 MHz	50 MHz
16-to-1 Multiplexer	16 ns	13 ns	11 ns	9 ns
16-bit Unidirectional Loadable Counter	40 MHz	50 MHz	59 MHz	65 MHz
16-bit U/D Counter	40 MHz	50 MHz	59 MHz	65 MHz
16-bit Adder	24 ns	20 ns	17 ns	15 ns
24-bit Loadable U/D Counter	36 MHz	42 MHz	48 MHz	52 MHz
	Preliminary			Advance

Development System

The powerful features of the XC5200 device family require an equally powerful, yet easy-to-use, set of development tools. Xilinx provides an enhanced version of the Xilinx Automatic CAE Tools (XACT*step*), optimized for the XC5200 family.

As with other logic technologies, the basic methodology for XC5200 FPGA design consists of three interrelated steps: design entry, implementation, and verification. Popular generic tools are used for entry and simulation (for example, Viewlogic Systems's Viewdraw schematic editor and Viewsim simulator), but architecture-specific tools are needed for implementation.

Several advanced features of the XACT*step* system facilitate XC5200 FPGA design. RPMs — schematic-based macros with relative location constraints to guide their placement within the FPGA — help to ensure an optimized implementation for common logic functions. An abundance of local routing permits RPMs to be contained within a single VersaBlock or to span across multiple VersaBlocks. XACT-Performance allows designers to enter the exact performance requirements during design entry, at the schematic level, to guide PPR.

Design Entry

Designs can be entered graphically, using schematic-capture software, or in any of several text-based formats (such as Boolean equations, state-machine descriptions, and high-level design languages).

Xilinx and third-party CAE vendors have developed library and interface products compatible with a wide variety of design-entry and simulation environments. A standard interface-file specification, Xilinx Netlist File (XNF), is provided to simplify file transfers into and out of the XACT*step* development system.

Xilinx offers XACT*step* development system interfaces to the following design environments:

- Xilinx Foundation Series
- Viewlogic Systems (Viewdraw, Viewsim)
- Mentor Graphics V8 (NETED, QuickSim, Design Architect, QuickSim II)
- OrCAD (SDT, VST)
- Synopsys (Design Compiler, FPGA Compiler)
- Xilinx-ABEL (State Machine module generator)
- X-BLOX (Graphical Mode Generator)

Many other environments are supported by third-party vendors. Currently, more than 100 packages are supported.

The unified schematic library for the XC5200 FPGA reflects the wide variety of logic functions that can be implemented in these versatile devices. The library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

Designing with macros is as easy as designing with standard SSI/MSI functions. The "soft macro" library contains detailed descriptions of common logic functions, but does not contain any partitioning or routing information. The performance of these macros depends, therefore, on how the PPR software processes the design. RPMs, on the other hand, do contain predetermined partitioning and relative placement information, resulting in an optimized implementation for these functions. Users can create their own library elements — either soft macros or RPMs — based on the macros and primitives of the standard library.

The X-BLOX design language is a graphics-based high-level description language (HDL) that allows designers to use a schematic editor to enter designs as a set of generic modules. The X-BLOX compiler synthesizes and optimizes the modules for the target device architecture, automatically choosing the appropriate architectural resources for each function.

The XACT*step* design environment supports hierarchical design entry, with top-level drawings defining the major functional blocks, and lower-level descriptions defining the logic in each block. The implementation tools automatically combine the hierarchical elements of a design. Different

hierarchical elements can be specified with different design entry tools, allowing the use of the most convenient entry method for each portion of the design.

Design Implementation

The design implementation tools satisfy the requirements for an automated design process. Logic partitioning, block placement, and signal routing are performed by the PPR program. The partitioner takes the logic from the entered design and maps the logic into the architectural resources of the FPGA (such as the logic blocks, I/O blocks, and 3-state buffers). The placer then determines the best locations for the blocks, depending on their connectivity and the required performance. The router finally connects the placed blocks together.

The PPR algorithms support fully automatic implementation of most designs. However, for demanding applications, the user may exercise various degrees of control over the automated implementation process. Optionally, user-designated partitioning, placement, and routing information can be specified as part of the design-entry process. The implementation of highly structured designs can benefit greatly from the basic floorplanning techniques familiar to designers of large gate arrays.

The PPR program includes XACT-Performance, a feature that allows designers to specify the timing requirements along entire paths during design entry. Timing path analysis routines in PPR then recognize and accommodate the user-specified requirements. Timing requirements can be entered on the schematic in a form directly relating to the system requirements (such as the targeted minimum clock frequency, or the maximum allowable delay on the data path between two registers). So, while the timing of each individual net is not predictable, the overall performance of the system along entire signal paths is automatically tailored to match user-generated specifications.

Design Verification

The high development cost associated with common mask-programmed gate arrays necessitates extensive simulation to verify a design. Due to the custom nature of masked gate arrays, mistakes or last-minute design changes cannot be tolerated. A gate-array designer must simulate and test all logic using simulation software. Simulation describes what happens in a system under worst-case situations. However, simulation can be tedious and slow, and simulation vectors must be generated. A few seconds of system time can take weeks to simulate.

Programmable-gate-array users, however, can use in-circuit debugging techniques in addition to simulation. Because Xilinx devices are reprogrammable, designs can be verified in real time without the need for extensive simulation vectors.

The XACT*step* development system supports both simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database. This data can then be sent to the simulator to verify timing-critical portions of the design database using XDELAY, the Xilinx static timing analyzer tool. Back-annotation — the process of mapping the timing information back into the signal names and symbols of the schematic — eases the debugging effort.

For in-circuit debugging, the XACT*step* development system includes a serial download and readback cable (XChecker) that connects the FPGA in the system to the PC or workstation through an RS232 serial port. The engineer can download a design or a design revision into the system for testing. The designer can also single-step the logic, read the contents of the numerous flip-flops on the device, and observe internal logic levels. Simple modifications can be downloaded into the system in a matter of minutes.

Detailed Functional Description

CLB Logic

Figure 3 shows the logic in the XC5200 CLB, which consists of four Logic Cells (LC[3:0]). Each Logic Cell consists of an independent 4-input Lookup Table (LUT), and a D-Type flip-flop or latch with common clock, clock enable, and clear, but individually selectable clock polarity. Additional logic features provided in the CLB are:

- High-speed carry propagate logic.
- High-speed pattern decoding.
- High-speed direct connection to flip-flop D-inputs.
- Each flip-flop can be programmed individually as either a transparent, level-sensitive latch or a D flip-flop.
- Four 3-state buffers with a shared Output Enable.
- Two 4-input LUTs can be combined to form an independent 5-input LUT.

5-Input Functions

Figure 5 illustrates how the outputs from the LUTs from LC0 and LC1 can be combined with a 2:1 multiplexer (F5_MUX) to provide a 5-input function. The outputs from the LUTs of LC2 and LC3 can be similarly combined.

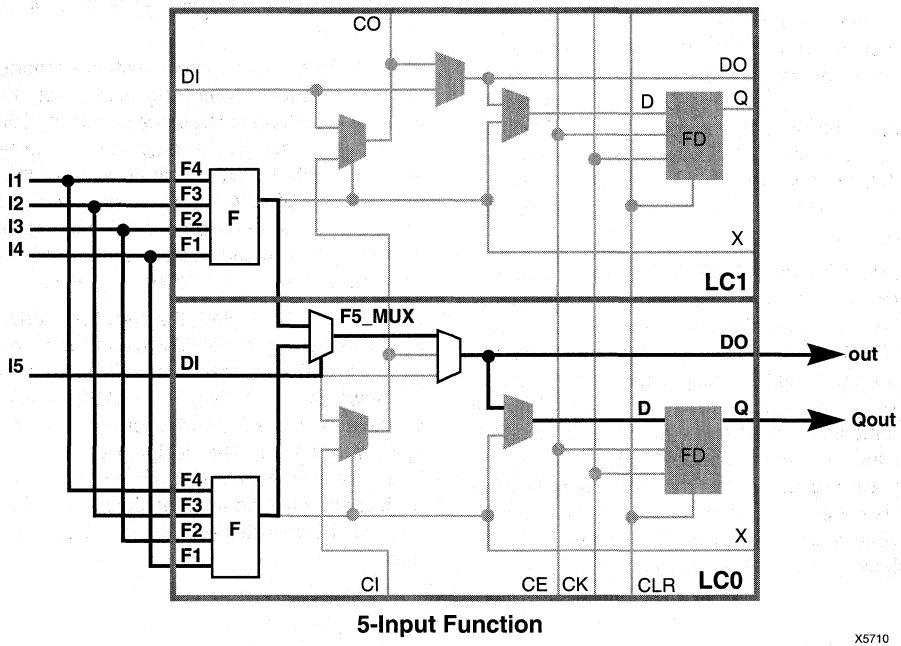


Figure 5: Two LUTs in Parallel Combined to Create a 5-input Function

Carry Function

The XC5200 family supports a carry-logic feature that enhances the performance of arithmetic functions such as counters, adders, etc. A carry multiplexer (CY_MUX) symbol on a schematic is used to indicate the XC5200 carry logic. This symbol represents the dedicated 2:1 multiplexer in each LC that performs the one-bit high-speed carry propagate per logic cell (four bits per CLB).

While the carry propagate is performed inside the LC, an adjacent LC must be used to complete the arithmetic function. Figure 6 represents an example of an adder function. The carry propagate is performed on the CLB shown, which also generates the half-sum for the four-bit adder. An adjacent CLB is responsible for XORing the half-sum with the corresponding carry-out. Thus an adder or counter requires two LCs per bit. Notice that the carry chain requires an initialization stage, which the XC5200 family accomplishes using the carry initialize (CY_INIT) macro and one additional LC.

The XC5200 library contains a set of RPMs and arithmetic functions designed to take advantage of the dedicated carry logic. Using and modifying these macros makes it much easier to implement customized RPMs, freeing the designer from the need to become an expert on architectures.

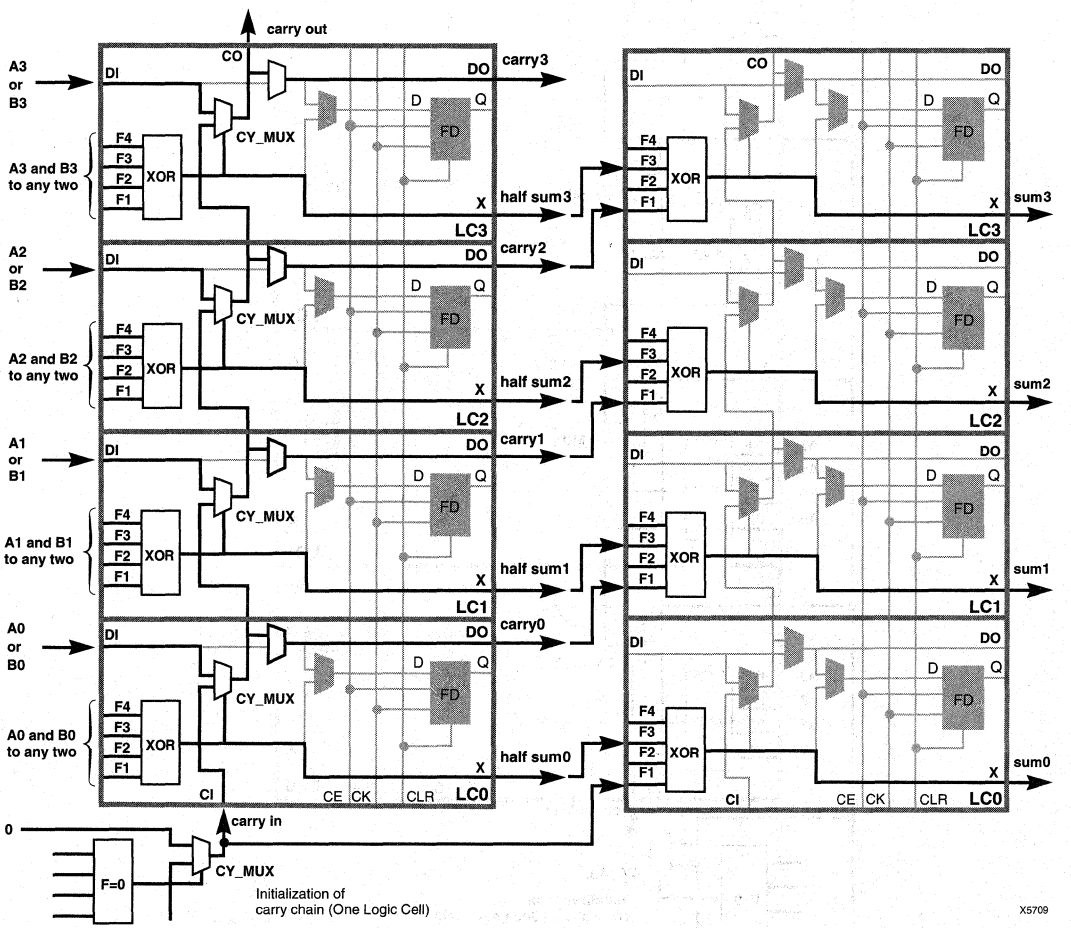


Figure 6: XC5200 CY_MUX Used for Adder Carry Propagate

Cascade Function

Each CY_MUX can be connected to the CY_MUX in the adjacent LC to provide cascadable decode logic. Figure 7 illustrates how the 4-input function generators can be configured to take advantage of these four cascaded CY_MUXes. Note that AND and OR cascading are specific cases of a general decode. In AND cascading all bits are decoded equal to logic one, while in OR cascading all bits are decoded equal to logic zero. The flexibility of the LUT achieves this result.

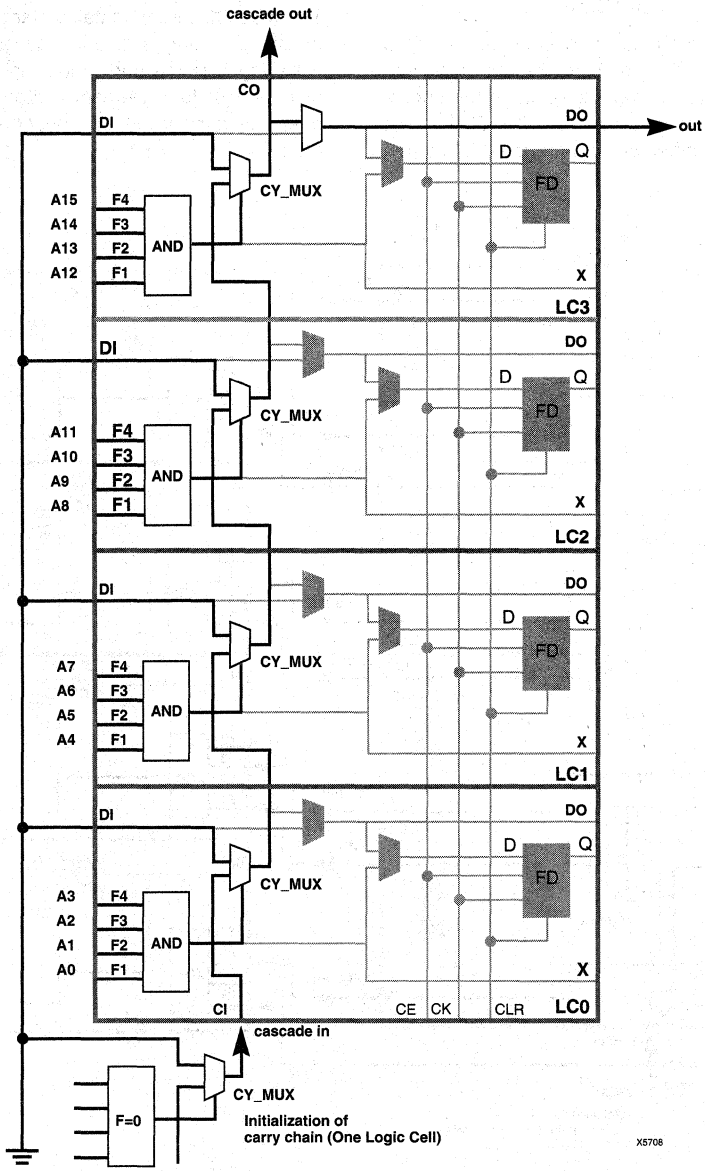


Figure 7: XC5200 CY_MUX Used for Decoder Cascade Logic

3-State Buffers

The XC5200 family has four dedicated TBUFs per CLB. The four buffers are individually configurable through four configuration bits to operate as simple non-inverting buffers or in 3-state mode. When in 3-state mode the CLB's output enable (TS) control signal drives the enable to all four buffers (see Figure 8). Each TBUF can drive up to two horizontal Longlines.

Oscillator

The XC5200 oscillator (OSC52) divides the internal 16-MHz clock or a user clock that is connected to the "C" pin. The user then has the choice of dividing by 4, 16, 64, or 256 for the "OSC1" output and dividing by 2, 8, 32, 128, 1024, 4096, 16384, or 65536 for the "OSC2" output. The division is specified via a "DIVIDEn_BY=x" attribute on the symbol, where n=1 for OSC1, or n=2 for OSC2. The OSC5 macro is used where an internal oscillator is required. The CK_DIV macro is applicable when a user clock input is specified (see Figure 9).

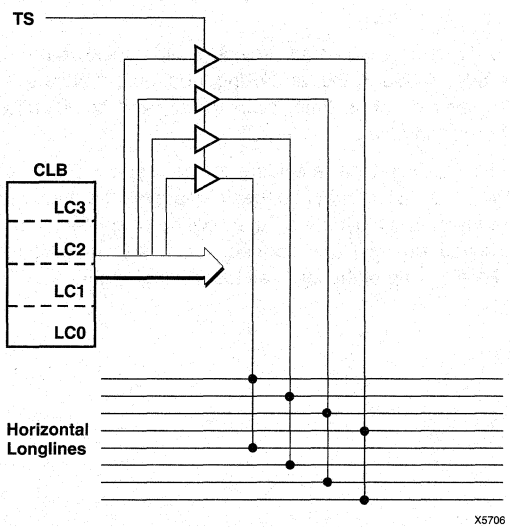


Figure 8: XC5200 3-State Buffer

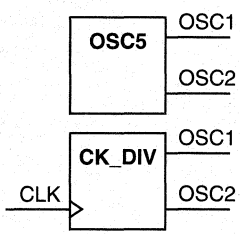


Figure 9: XC5200 Oscillator Macros

Global Reset (GR)

On start-up, all XC5200 internal flip-flops are reset, using a global reset (GR) signal. The user can assign the pin location for the GR signal and use it to reset asynchronously all of the flip-flops in the design without using general routing resources. The user can also assign a positive or negative polarity to GR.

Boundary Scan

XC5200 devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP can also support two USERCODE instructions.

Boundary-scan operation is independent of individual IOB configuration and package type. All IOBs are treated as independently controlled bidirectional pins, including any unbonded IOBs. Retaining the bidirectional test capability after configuration provides flexibility for interconnect testing.

Also, internal signals can be captured during EXTEST by connecting them to unbonded IOBs, or to the unused outputs in IOBs used as unidirectional input pins. This technique partially compensates for the lack of INTEST support.

The public boundary-scan instructions are always available prior to configuration. After configuration, the public instructions and any USERCODE instructions are only available if specified in the design. While SAMPLE and BYPASS are available during configuration, it is recommended that boundary-scan operations not be performed during this transitory period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA device, and to read back the configuration data.

All of the XC4000 boundary-scan modes are supported in the XC5200 family. Three additional outputs for the User Register are provided (Reset, Update, and Shift), representing the decoding of the corresponding state of the boundary-scan internal state machine.

VersaBlock Routing

Local Interconnect Matrix

The GRM connects to the VersaBlock via 24 bidirectional ports (M0-M23). Excluding direct connections, global nets, and 3-statable Longlines, all VersaBlock inputs and outputs connect to the GRM via these 24 ports. Four 3-statable unidirectional signals (TQ0-TQ3) drive out of the VersaBlock directly onto the horizontal Longlines. Two horizontal global nets (GH0 and GH1) and two vertical global nets (GV0 and GV1) connect directly to every CLB clock pin; they can connect to other CLB inputs via the GRM. Each CLB also has four unidirectional direct connects to each of its four neighboring CLBs. These direct connects can also feed directly back to the CLB (see Figure 10).

In addition, each CLB has 16 direct inputs, four direct connections from each of the neighboring CLBs. These direct connections provide high-speed local routing that bypasses the GRM.

The 13 CLB outputs (12 LC outputs plus a V_{CC}/GND signal) connect to the eight VersaBlock outputs via the output multiplexers, which consist of eight fully populated 13-to-1 multiplexers. Of the eight VersaBlock outputs, four signals drive each neighboring CLB directly, and provide a direct feedback path to the input multiplexers. The four remaining multiplexer outputs can drive the GRM through four TBUFs (TQ0-TQ3). All eight multiplexer outputs can connect to the GRM through the bidirectional M0-M23 signals. All eight signals also connect to the input multiplexers and are potential inputs to that CLB.

CLB inputs have several possible sources: the 24 signals from the GRM, 16 direct connections from neighboring VersaBlocks, four signals from global, low-skew buffers (GH0, GH1, GV0, and GV1), and the four signals from the CLB output multiplexers. Unlike the output multiplexers, the input multiplexers are not fully populated; i.e., only a subset of the available signals can be connected to a given CLB input. The flexibility of LUT input swapping and LUT mapping compensates for this limitation. For example, if a 2-input NAND gate is required, it can be mapped into any of the four LUTs, and use any two of the four inputs to the LUT.

Direct Connects

The unidirectional direct-connect segments are connected to the logic input/output pins through the CLB's input and output multiplexer array, and thus bypass the programmable routing matrix altogether. These lines are intended to increase the routing channel utilization where possible, while simultaneously reducing the delay incurred in speed-critical connections.

The direct connects also provide a high-speed path from the edge CLBs to the VersaRing input/output buffers, and thus reduce set-up time, clock-to-out, and combinational propagation delay.

The direct connects are ideal for developing customized RPM cells. Using direct connects improves the macro performance, and leaves the other routing channels intact for improved routing. Direct connects can also route through a CLB using one of the four cell-feedthrough paths.

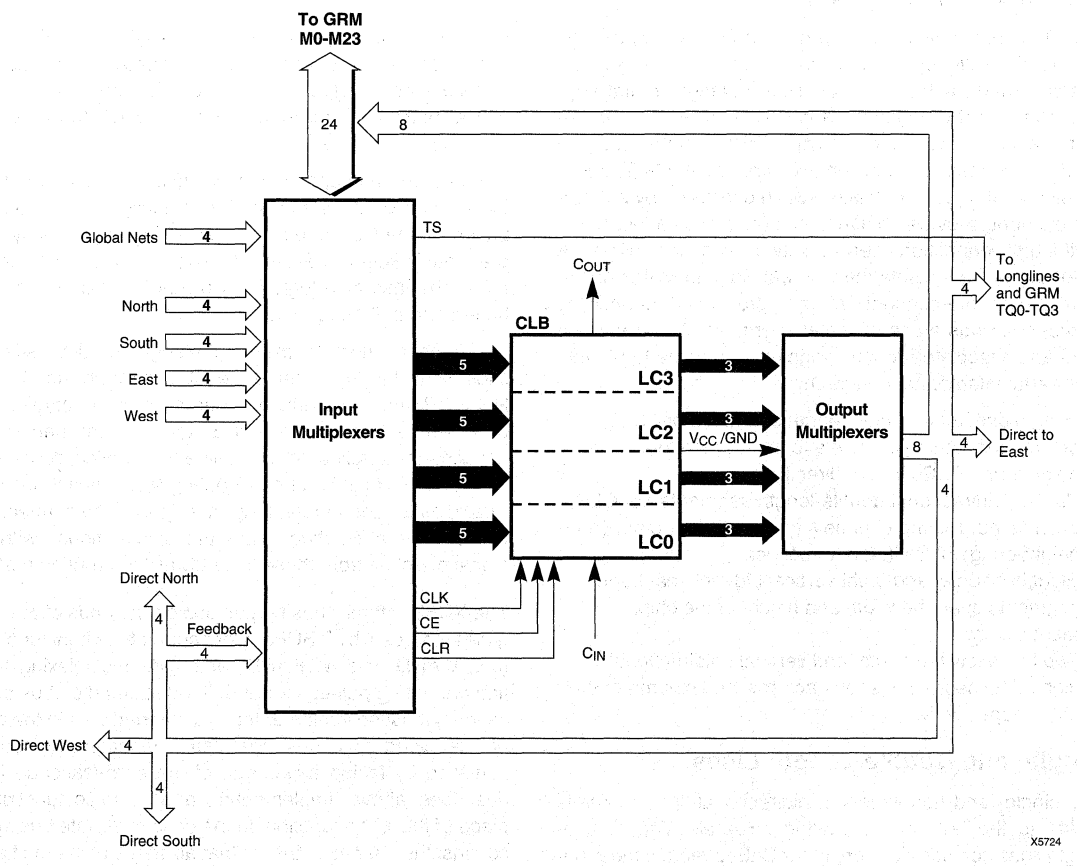


Figure 10: VersaBlock Details

General Routing Matrix

The General Routing Matrix, shown in Figure 11, provides flexible bidirectional connections to the Local Interconnect Matrix through a hierarchy of different-length metal segments in both the horizontal and vertical directions. A programmable interconnect point (PIP) establishes an electrical connection between two wire segments. The PIP, consisting of a pass transistor switch controlled by a memory element, provides bidirectional (in some cases, unidirectional) connection between two adjoining wires. A collection of PIPs inside the General Routing Matrix and in the Local Interconnect Matrix provides connectivity between various types of metal segments. A hierarchy of PIPs and associated routing segments combine to provide a powerful interconnect hierarchy:

- Forty bidirectional single-length segments per CLB provide ten routing channels to each of the four neighboring CLBs in four directions.
- Sixteen bidirectional double-length segments per CLB provide four routing channels to each of four other (non-neighboring) CLBs in four directions.
- Eight horizontal and eight vertical bidirectional Longline segments span the width and height of the chip, respectively.
- Two low-skew horizontal and vertical unidirectional global-line segments span each row and column of the chip, respectively.

Single- and Double-Length Lines

The single- and double-length bidirectional line segments make up the bulk of the routing channels. The double-length lines hop across every other CLB to reduce the propagation delays in speed-critical nets. Regenerating the signal strength is recommended after traversing three or four such segments. XACT*step* place-and-route software automatically connects buffers in the path of the signal as necessary. Single- and double-length lines cannot drive onto Longlines and global lines; Longlines and global lines can, however, drive onto single- and double-length lines. As a general rule, Longline and global-line connections to the programmable routing matrix are unidirectional, with the signal direction from these lines toward the routing matrix.

Longlines

Longlines are used for high-fan-out signals, 3-state busses, low-skew nets, and faraway destinations. Row and column splitter PIPs in the middle of the array effectively double the total number of Longlines by electrically dividing them into two separated half-lines. The horizontal Longlines are driven by the 3-state buffers in each CLB, and are driven by similar buffers at the periphery of the array from the VersaRing I/O Interface.

Bus-oriented microprocessor designs are accommodated by using horizontal Longlines in conjunction with the 3-state buffers in the CLB and in the VersaRing. Additionally, programmable keeper cells at the periphery can be enabled to retain the last valid logic level on the Longlines when all buffers are in 3-state mode.

Longlines connect to the single-length or double-length lines, or to the logic inside the CLB, through the General Routing Matrix. The only manner in which a Longline can be driven is through the four 3-state buffers; therefore, a Longline-to-Longline or single-line-to-Longline connection through PIPs in the General Routing Matrix is not possible. Again, as a general rule, long- and global-line connections to the General Routing Matrix are unidirectional, with the signal direction from these lines toward the routing matrix.

The XC5200 family has no pull-ups on the ends of the Longlines sourced by TBUFs. Consequently, wired functions (i.e., WAND and WORAND) and wide multiplexing functions requiring pull-ups for undefined states (i.e., bus applications) must be implemented in a different way. In the case of the wired functions, the same functionality can be achieved by taking advantage of the carry/cascade logic described above, implementing a wide logic function in place of the wired function. In the case of 3-state bus applications, the user must insure that all states of the multiplexing function are defined. This process is as simple as adding an additional TBUF to drive the bus High when the previously undefined states are activated.

Global Lines

Global buffers in Xilinx FPGAs are special buffers that drive a dedicated routing network called Global Lines, as shown in Figure 12. This network is intended for high-fan-out clocks or other control signals, to maximize speed and minimize skewing while distributing the signal to many loads.

The XC5200 family has a total of four global buffers (BUFG symbol in the library), each with its own dedicated routing channel. Two are distributed vertically and two horizontally throughout the FPGA.

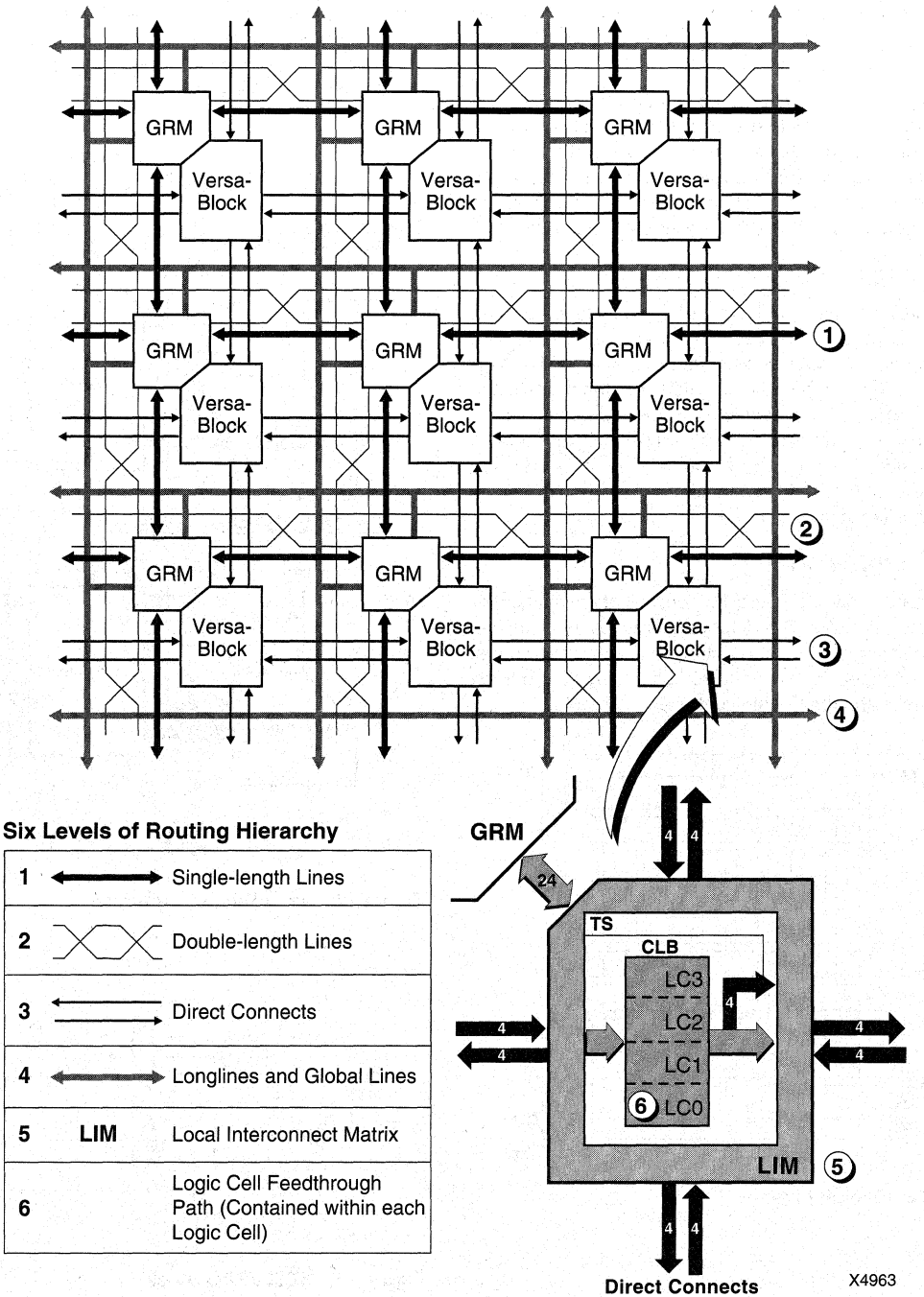


Figure 11: XC5200 Interconnect Structure

The global lines provide direct input only to the CLB clock pins. The global lines also connect to the General Routing Matrix to provide access from these lines to the function generators and other control signals.

Four clock input pads at the corners of the chip, as shown in Figure 12, provide a high-speed, low-skew clock network to each of the four global-line buffers. In addition to the dedicated pad, the global lines can be sourced by internal logic. PIPs from several routing channels within the VersaRing can also be configured to drive the global-line buffers.

VersaRing Input/Output Interface

The VersaRing, shown in Figure 13, is positioned between the core logic and the pad ring; it has all the routing resources of a VersaBlock without the CLB logic. The VersaRing decouples the pad ring's pitch from the core's pitch. Each VersaRing Cell provides up to four pad-cell connections on one side, and connects directly to the CLB ports on the other side. Depending on placement and pad-cell pitch, any number of pad cells to a maximum of four can be connected to a VersaRing cell.

Input/Output Pad

The I/O pad, shown in Figure 14, consists of an input buffer and an output buffer. The output driver is an 8-mA full-rail CMOS buffer with 3-state control. Two slew-rate control modes are supported to minimize bus transients. Both the output buffer and the 3-state control are invertible.

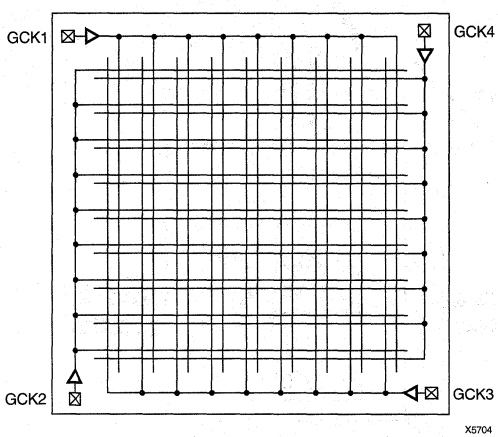


Figure 12: Global Lines

The input buffer has globally selected CMOS and TTL input thresholds. The input buffer is invertible and also provides a programmable delay line to assure reliable chip-to-chip set-up and hold times. Minimum ESD protection is 3 KV using the Human Body Model.

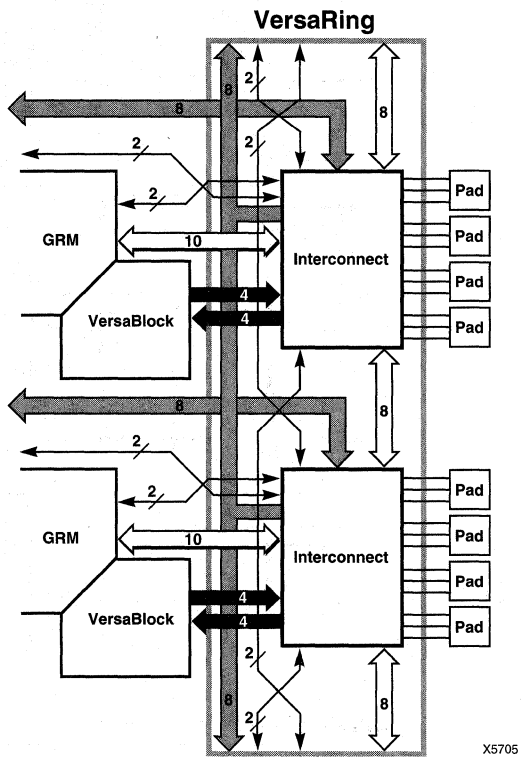


Figure 13: VersaRing I/O Interface

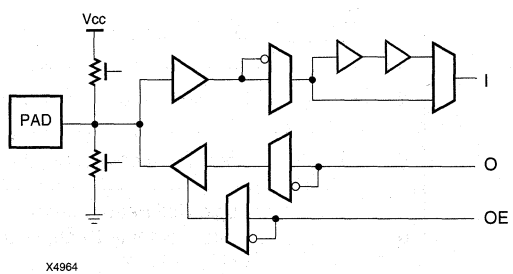


Figure 14: XC5200 I/O Block

Pin Descriptions

Permanently Dedicated Pins

V_{cc}

Eight or more (depending on package type) connections to the nominal +5-V supply voltage. All must be connected.

GND

Eight or more (depending on package type) connections to ground. All must be connected.

CCLK

During configuration, Configuration Clock is an output of the FPGA in master modes or Asynchronous Peripheral mode, but is an input to the FPGA in Slave Serial mode, Synchronous Peripheral mode, and Express mode.

After configuration, CCLK has a weak pull-up resistor and can be selected as Readback Clock.

DONE

This is a bidirectional signal with optional pull-up resistor.

As an output, it indicates the completion of the configuration process. The configuration program determines the exact timing, the clock source for the Low-to-High transition, and enable of the pull-up resistor.

As an input, a Low level on DONE can be configured to delay the global logic initialization or the enabling of outputs.

$\overline{\text{PROGRAM}}$

This is an active-Low input, held Low during configuration, that forces the FPGA to clear its configuration memory.

When $\overline{\text{PROGRAM}}$ goes High, the FPGA executes a complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. After configuration, it has an optional pull-up resistor.

User I/O Pins That Can Have Special Functions

RDY/$\overline{\text{BUSY}}$

During peripheral modes, this pin indicates when it is appropriate to write another byte of data into the FPGA device. The same status is also available on D7 in Asynchronous Peripheral mode, if a read operation is performed when the device is selected. After configuration, this is a user-programmable I/O pin.

$\overline{\text{RCLK}}$

During Master Parallel configuration, each change on the A0-17 outputs is preceded by a rising edge on $\overline{\text{RCLK}}$, a redundant output signal. After configuration, this is a user-programmable I/O pin.

M0, M1, M2

As mode inputs, these pins are sampled before the start of configuration to determine the configuration mode to be used.

After configuration, M0, M1, and M2 become user-programmable I/O.

TDO

If boundary scan is used, this is the Test Data Output.

If boundary scan is not used, this pin becomes user-programmable I/O.

TDI, TCK, TMS

If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs, respectively, coming directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed.

If the boundary scan option is not selected, all boundary scan functions are inhibited once configuration is completed. These pins become user-programmable I/O.

HDC

High During Configuration is driven High until configuration is completed. It is available as a control output indicating that configuration is not yet completed. After configuration, this is a user-programmable I/O pin.

$\overline{\text{LDC}}$

Low During Configuration is driven Low until configuration completes. It is available as a control output indicating that configuration is not yet completed. After configuration, this is a user-programmable I/O pin.

$\overline{\text{INIT}}$

Before and during configuration, this is a bidirectional signal. An external pull-up resistor is recommended.

As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA device in the internal WAIT state before the start of configuration. Master-mode devices stay in a WAIT state an additional 50 to 250 µs after $\overline{\text{INIT}}$ has gone High.

During configuration, a Low on this output indicates that a configuration data error has occurred. After configuration, this is a user-programmable I/O pin.

GCK1 - GCK4

Four Global Inputs each drive a dedicated internal global net with short delay and minimal skew. If not used for this purpose, any of these pins is a user-programmable I/O pin.

$\overline{CS0}$, CS1, $\overline{WS}$, $\overline{RS}$

These four inputs are used in peripheral modes. The chip is selected when $\overline{CS0}$ is Low and CS1 is High. While the chip is selected, a Low on Write Strobe ($\overline{WS}$) loads the data present on the D0 - D7 inputs into the internal data buffer; a Low on Read Strobe ($\overline{RS}$) changes D7 into a status output: High if Ready, Low if Busy, and D0...D6 are active High. $\overline{WS}$ and $\overline{RS}$ should be mutually exclusive, but if both are Low simultaneously, the Write Strobe overrides. After configuration, these are user-programmable I/O pins. In Express mode, CS1 is also used as a serial-enable signal for daisy chaining.

A0 - A17

During Master Parallel mode, these 18 output pins address the configuration EPROM. After configuration, these are user-programmable I/O pins.

D0 - D7

During Master Parallel, peripheral, and Express configuration modes, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.

DIN

During Slave Serial or Master Serial configuration modes, this is the serial configuration data input receiving data on the rising edge of CCLK.

During parallel configuration modes, this is the D0 input. After configuration, DIN is a user-programmable I/O pin.

DOUT

During configuration in any non-Express mode, this is the serial configuration data output that can drive the DIN of daisy-chained slave FPGA devices. DOUT data changes on the falling edge of CCLK. After configuration, DOUT is a user-programmable I/O pin.

In Express mode, this is the enable output that can drive CS1 of daisy-chained FPGA devices.

Unrestricted User-Programmable I/O Pins

I/O

A pin that can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-impedance pull-up resistor that defines the logical level as High.

Configuration

Configuration is the process of loading design-specific programming data into one or more FPGA devices to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Each configuration bit defines the state of a static memory cell that controls either a function LUT bit, a multiplexer input, or an interconnect pass transistor. The XACT*step* development system translates the design into a netlist file. It automatically partitions, places, and routes the logic and generates the configuration data in PROM format.

Modes

The XC5200 family has seven modes of configuration, selected by a 3-bit input code applied to the FPGA mode pins (M0, M1, and M2). There are three self-clocking Master modes, two Peripheral modes, a Slave serial mode, and a new high-speed Slave parallel mode called the Express. See Table 4.

Brief descriptions of the seven modes are provided below.

Master Modes

The Master modes use an internal oscillator to generate CCLK for driving potential slave devices, and to generate address and timing for external PROM(s) containing the configuration data. Master Parallel (up or down) modes generate the CCLK signal and PROM addresses, and receive byte parallel data, which is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, to be compatible with different microprocessor addressing conventions. The Master Serial Mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

Peripheral Modes

The two Peripheral modes accept byte-wide data from a bus. A READY/BUSY status is available as a handshake signal. In the asynchronous mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. In the synchronous mode, an externally supplied clock input to CCLK serializes the data.

Slave Serial Mode

In the Slave Serial mode, the FPGA device receives serial-configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK. Multiple slave devices with identical configurations can be wired with parallel DIN inputs so that the devices can be configured simultaneously.

Daisy Chaining

Multiple devices may be daisy-chained together so that they may be programmed using a single bitstream. The first device in the chain may be set to operate in any mode; all other devices in the chain must be set to operate in Slave Serial mode. Express-mode daisy chains are the only exception: every device in such a chain must be set to operate in Express mode.

All CCLK pins are tied together, and the data chain passes from DOUT to DIN of successive devices along the chain.

Table 4: Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel up	1	0	0	output	Byte-Wide, 00000 ↑
Master Parallel down	1	1	0	output	Byte-Wide, 3FFFF ↓
Peripheral Synchronous *	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Express	0	1	0	input	Byte-Wide
Reserved	0	0	1	—	—

* Peripheral Synchronous can be considered byte-wide Slave Parallel

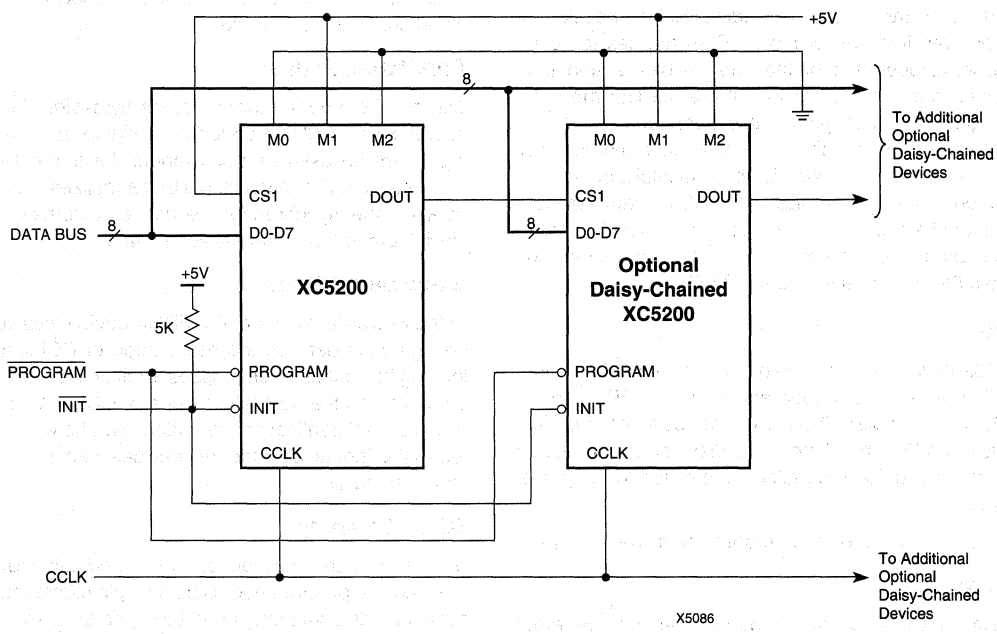


Figure 15: Express Mode

Express Mode

The Express mode (see Figure 15) is similar to the Slave serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK while byte-wide data is loaded directly into the configuration data shift registers. In this mode the XC5200 family is capable of supporting a CCLK frequency of 10 MHz, which is equivalent to an 80-MHz serial rate, because eight bits of configuration data are being loaded per CCLK cycle. An XC5210 in the Express mode, for instance, can be configured in about 2 ms. The Express mode does not support CRC error checking, but does support constant-field error checking.

In the Express configuration mode, an external signal drives the CCLK input(s) of the FPGA device(s). The first byte of parallel configuration data must be available at the D inputs of the FPGA devices a short set-up time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge. See Figure 16.

Bitstream generation currently generates a bitstream sufficient to program in all configuration modes except Express. Extra CCLK cycles are necessary to complete the configuration, since in this mode data is read at a rate of eight bits per CCLK cycle instead of one bit per cycle. Normally the entire start-up sequence requires a number of bits that is equal to the number of CCLK cycles needed. An additional five CCLKs (equivalent to 40 extra bits) will guarantee completion of configuration, regardless of the start-up options chosen.

The Express mode is supported by the XC5200 and XC4000EX families. It may be used, if XC5200 and XC4000EX devices are daisy-chained.

If the first device is configured in the Express mode, additional devices may be daisy-chained only if every device in the chain is also configured in the Express mode. CCLK pins are tied together and D7-D0 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled LOW two internal-oscillator cycles (nominally 1 MHz) after $\overline{\text{INIT}}$ is recognized as High, and remains Low until the device's configuration memory is full. Then DOUT is pulled High to signal the next device in the chain to accept the configuration data on the D7-D0 bus. All devices receive and recognize the six bytes of preamble and length count, irrespective of the level on CS1; but subsequent frame data is accepted only when CS1 is High and the device's configuration memory is not already full.

Format

Table 5 describes the XC5200 configuration data stream. Table 6 describes the internal configuration data structure.

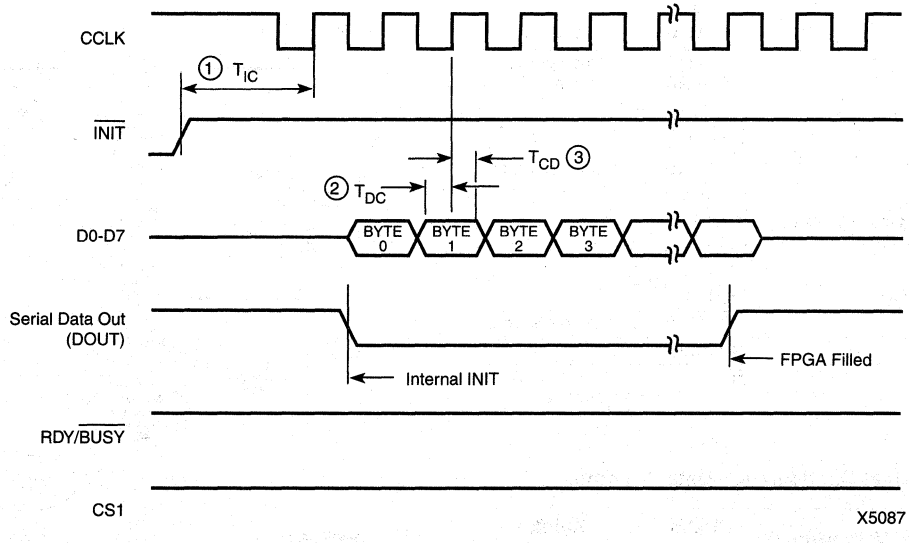


Figure 16: Express Mode Programming Switching Characteristics

	Description	Symbol		Min	Max	Units
CCLK	$\overline{INIT}$ (High) Setup time required	1	T_{IC}	5		µs
	DIN Setup time required	2	T_{DC}	30		ns
	DIN Hold time required	3	T_{CD}	0		ns
	CCLK High time		T_{CCH}	30		ns
	CCLK Low time		T_{CCL}	30		ns
	CCLK Frequency		F_{CC}		10	MHz

Table 5: XC5200 Bitstream Format

Data Type	Value	Occurrences
Fill Byte	11111111	Once per bit-stream
Preamble	11110010	
Length Counter	COUNT(23:0)	
Fill Byte	11111111	
Start Byte	11111110	Once per data frame
Data Frame *	DATA(N-1:0)	
Cyclic Redundancy Check or Constant Field Check	CRC(3:0) or 0110	
Fill Nibble	1111	
Extend Write Cycle	FFFFFF	
Postamble	11111110	Once per de-vice
Fill Bytes (30)	FFFF...FF	
Start-Up Byte	FF	Once per bit-stream

Table 6: Internal Configuration Data Structure

Device	VersaBlock Array	PROM Size (bits)	Xilinx Serial Prom Needed
XC5202	8 x 8	42,416	XC1765D
XC5204	10 x 12	70,704	XC17128D
XC5206	14 x 14	106,288	XC17128D
XC5210	18 x 18	165,488	XC17256D
XC5215	22 x 22	237,744	XC17256D

Bits per Frame = (34 x number of Rows) + 28 for the top + 28 for the bottom + 4 splitter bits + 8 start bits + 4 error check bits + 4 fill bits * + 24 extended write bits
= (34 x number of Rows) + 100
* In the XC5202 (8 x 8), there are 8 fill bits per frame, not 4

Number of Frames = (12 x number of Columns) + 7 for the left edge + 8 for the right edge + 1 splitter bit
= (12 x number of Columns) + 16

Program Data = (Bits per Frame x Number of Frames) + 48 header bits + 8 postamble bits + 240 fill bits + 8 start-up bits
= (Bits per Frame x Number of Frames) + 304

PROM Size = Program Data

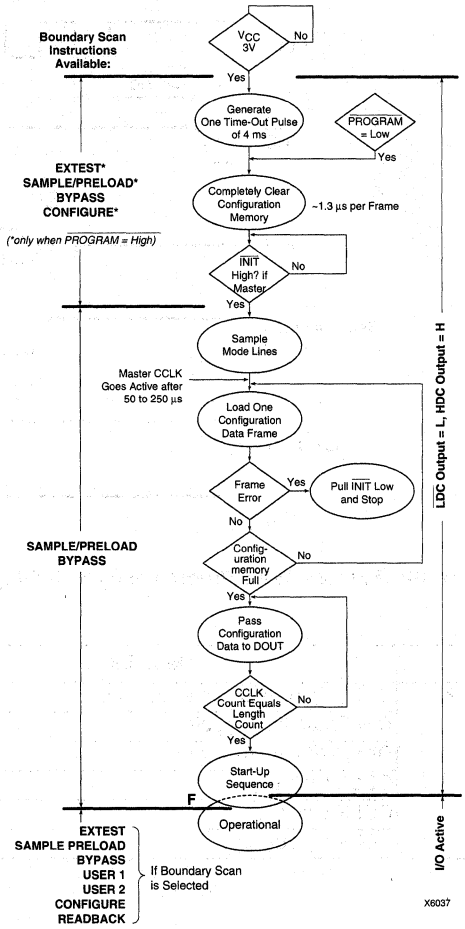


Figure 17: Configuration Sequence

Configuration Sequence

Figure 17 illustrates the XC5200 configuration sequence. This section describes the configuration sequence in detail.

Power-On Time-Out

An internal power-on reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the FPGA begin to operate (i.e., performs a write-and-read test of a sample pair of configuration memory bits), the programmable I/O buffers are 3-stated with active high-impedance pull-up resistors. A time-out delay — nominally 4 ms — is initiated to allow the power-supply voltage to stabilize. For correct operation the power supply must reach V_{CC}(min) by the end of the time-out, and must not dip below it thereafter.

There is no distinction between master and slave modes with regard to the time-out delay. Instead, the $\overline{\text{INIT}}$ line is used to ensure that all daisy-chained devices have completed initialization. Since XC2000 devices do not have this signal, extra care must be taken to guarantee proper operation when daisy-chaining them with XC5200 devices. For proper operation with XC3000 devices, the $\overline{\text{RESET}}$ signal, which is used in XC3000 to delay configuration, should be connected to $\overline{\text{INIT}}$.

If the time-out delay is insufficient, configuration should be delayed by holding the $\overline{\text{INIT}}$ pin Low until the power supply has reached operating levels.

During all three phases — Power-on, Initialization, and Configuration — DONE is held Low; HDC, $\overline{\text{LDC}}$, and $\overline{\text{INIT}}$ are active; DOUT is driven; and all I/O buffers are disabled.

Initialization

This phase clears the configuration memory and establishes the configuration mode.

The configuration memory is cleared at the rate of one frame per internal clock cycle (nominally 1 MHz). An open-drain bidirectional signal, $\overline{\text{INIT}}$, is released when the configuration memory is completely cleared. The device then tests for the absence of an external active-low level on $\overline{\text{INIT}}$. The mode lines are sampled two internal clock cycles later (nominally 2 µs).

The master device waits an additional 32 µs to 256 µs (nominally 64-128 µs) to provide adequate time for all of the slave devices to recognize the release of $\overline{\text{INIT}}$ as well. Then the master device enters the Configuration phase.

Configuration

The length counter begins counting immediately upon entry into the configuration state. In slave-mode operation it is important to wait at least two cycles of the internal 1-MHz clock oscillator after $\overline{\text{INIT}}$ is recognized before toggling CCLK and feeding the serial bitstream. Configuration will not begin until the internal configuration logic reset is released, which happens two cycles after $\overline{\text{INIT}}$ goes High. A master device's configuration is delayed from 32 to 256 µs to ensure proper operation with any slave devices driven by the master device.

A preamble field at the beginning of the configuration data stream indicates that the next 24 bits represent the length count. The length count equals the total number of configuration bits needed to load the complete configuration data to all daisy-chained devices. Once the preamble and length-count values have been passed through to the next device in the daisy-chain, DOUT is held High to prevent start bits from reaching any daisy-chained devices. After fully configuring itself, the device passes serial data to downstream daisy-chained devices via DOUT until the full length count is reached.

Errors in the configuration bitstream are checked at the end of a frame of data. The device does not check the preamble or length count for errors. In a daisy-chained configuration, configuration data for downstream devices are not checked for errors. If an error is detected after reading a frame, the $\overline{\text{ERR}}$ pin (also known as $\overline{\text{INIT}}$) is immediately pulled Low and all configuration activity ceases. However, a master or Peripheral Asynchronous device will continue outputting a configuration clock and incrementing the PROM address indefinitely even though it will never complete configuration. A reprogram or power-on must be applied to remove the device from this state.

Start-Up and Operation

The XC5200 start-up sequence is identical to that of the XC4000 family. Each of these events may occur in any order: (a) DONE is pulled High; and/or (b) user I/Os become active; and/or (c) Internal Reset is deactivated. As a configuration option, the three events may be triggered by a user clock rather than by CCLK, or the start-up sequence may be delayed by externally holding the DONE pin Low.

In any mode, the clock cycles of the start-up sequence are not included in the length count. The length of the bitstream is greater than the length count.

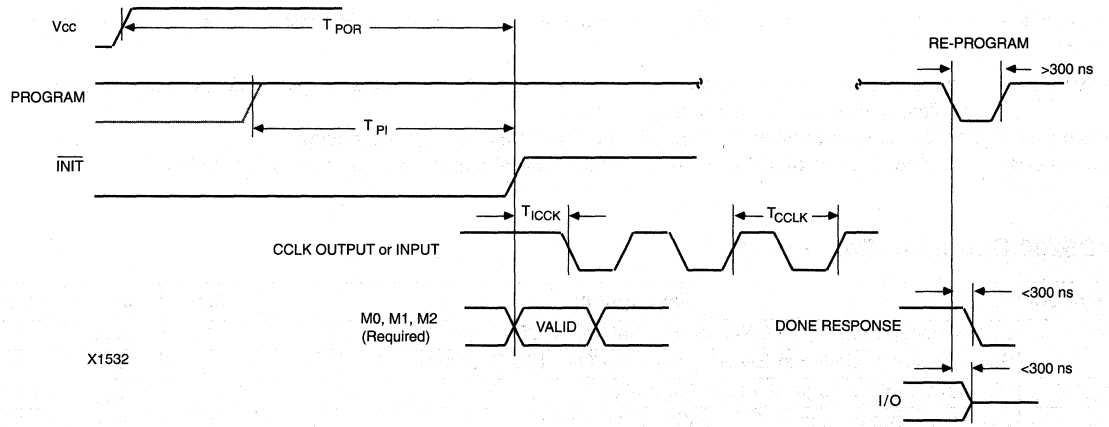
Pin Functions During Configuration

CONFIGURATION MODE: <M2:M1:M0>							USER OPERATION
SLAVE <1:1:1>	MASTER-SER <0:0:0>	SYN.PERIPH <0:1:1>	ASYN.PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	EXPRESS <0:1:0>	
				A16	A16		GCK1-I/O
				A17	A17		I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
							I/O
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	I/O
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	M0 (LOW) (I)	I/O
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (LOW) (I)	I/O
							GCK2-I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O
$\overline{\text{INIT}}$-ERROR *	$\overline{\text{INIT}}$-ERROR *	$\overline{\text{INIT}}$-ERROR *	$\overline{\text{INIT}}$-ERROR *	$\overline{\text{INIT}}$-ERROR *	$\overline{\text{INIT}}$-ERROR *	$\overline{\text{INIT}}$-ERROR *	I/O
							I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
							GCK3-I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
			$\overline{\text{CSO}}$ (I)				I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
			$\overline{\text{RS}}$ (I)				I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	I/O
		RDY/$\overline{\text{BUSY}}$	RDY/$\overline{\text{BUSY}}$	RCLK	RCLK		I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	I/O
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (I)	CCLK (I)
TDO	TDO	TDO	TDO	TDO	TDO	TDO	TDO-I/O
			$\overline{\text{WS}}$ (I)	A0	A0		I/O
				A1	A1		GCK4-I/O
			CS1 (I)	A2	A2	CS1 (I)	I/O
				A3	A3		I/O
				A4	A4		I/O
				A5	A5		I/O
				A6	A6		I/O
				A7	A7		I/O
				A8	A8		I/O
				A9	A9		I/O
				A10	A10		I/O
				A11	A11		I/O
				A12	A12		I/O
				A13	A13		I/O
				A14	A14		I/O
				A15	A15		I/O
							ALL OTHERS

* INIT is an open-drain output during configuration (I) Represents an input (O) Represents an output

Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50-kΩ to 100-kΩ pull-up resistor.

Configuration Switching Characteristics



Master Modes

Description	Symbol	Min	Max	Units
Power-On-Reset	T_{POR}	2	15	ms
Program Latency	T_{PI}	6	70	µs per CLB column
CCLK (output) Delay	T_{ICCK}	40	375	µs
period (slow)	T_{CCLK}	640	3000	ns
period (fast)	T_{CCLK}	100	375	ns

Slave and Peripheral Modes

Description	Symbol	Min	Max	Units
Power-On-Reset	T_{POR}	2	15	ms
Program Latency	T_{PI}	6	70	µs per CLB column
CCLK (input) Delay (required)	T_{ICCK}	5		µs
period (required)	T_{CCLK}	100		ns

Note: At power-up, V_{CC} must rise from 2.0 to V_{CC} min in less than 15 ms, otherwise delay configuration using $\overline{PROGRAM}$ until V_{CC} is valid.

XC5200 Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.[1]

XC5200 Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GNDCommercial:0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GNDIndustrial:-40°C to 100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

XC5200 DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -8.0 mA, V_{CC} min	3.86		V
V_{OL}	Low-level output voltage @ I_{OL} = 8.0 mA, V_{CC} max (Note 1)		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 1)		15	mA
I_{IL}	Leakage current	-10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.25	mA

Note: 1. With no output current loads, all package pins at Vcc or GND, either TTL or CMOS inputs, and the FPGA configured with a MakeBits tie option.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

XC5200 Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature in plastic packages	+125	°C
	Junction temperature in ceramic packages	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC5200 Global Buffer Switching Characteristic Guidelines

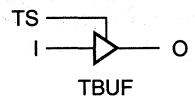
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT*step* timing calculator and used in the simulator.

		Speed Grade	-6	-5	-4	-3
Description	**Symbol**	**Device**	**Max (ns)**	**Max (ns)**	**Max (ns)**	**Max (ns)**
Global Signal Distribution						
From pad through global buffer, to any clock (CK)	T_{BUFG}	XC5202	9.1	8.5		
		XC5204	9.3	8.7		
		XC5206	9.4	8.8		
		XC5210	9.4	8.8	8.5	8.3
		XC5215	10.5	9.9		
			PRELIMINARY			ADVANCE

Note: 1. Die-size-dependent parameters are based upon XC5210 characterization. Production specifications will vary with array size.

XC5200 Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT*step* timing calculator and used in the simulator.

			-6	-5	-4	-3
Description	**Symbol**	**Device**	**Max (ns)**	**Max (ns)**	**Max (ns)**	**Max (ns)**
TBUF driving a Longline  						
I to Longline, while TS is Low; i.e., buffer is constantly active	T_{IO}	XC5202	6.0	3.8		
		XC5204	6.4	4.1		
		XC5206	6.6	4.2		
		XC5210	6.6	4.2	3.3	3.2
		XC5215	7.3	4.6		
TS going Low to Longline going from floating High or Low to active Low or High	T_{ON}	XC5202	7.8	5.6		
		XC5204	8.3	5.9		
		XC5206	8.4	6.0		
		XC5210	8.4	6.0	5.0	4.7
		XC5215	8.9	6.3		
TS going High to TBUF going inactive, not driving Longline	T_{OFF}	XC52xx	3.0	2.8		
			PRELIMINARY			ADVANCE

Note: 1. Die-size-dependent parameters are based upon XC5210 characterization. Production specifications will vary with array size.

XC5200 CLB Switching Characteristic Guidelines

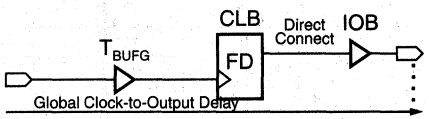
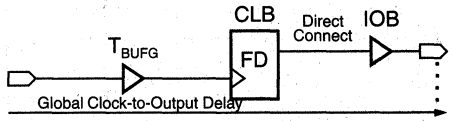
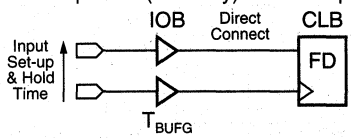
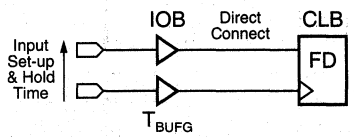
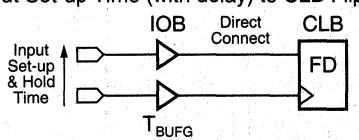
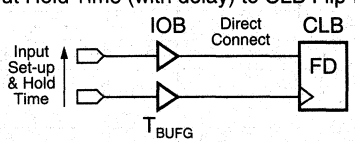
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT*step* timing calculator and used in the simulator.

Description	Symbol	-6 Min (ns)	-6 Max (ns)	-5 Min (ns)	-5 Max (ns)	-4 Min (ns)	-4 Max (ns)	-3 Min (ns)	-3 Max (ns)
Combinatorial Delays									
F inputs to X output	T_{ILO}		5.6		4.6		3.8		3.0
DI inputs to DO output (Logic-Cell Feedthrough)	T_{IDO}		4.3		3.5		2.8		2.2
F inputs via F5_MUX to DO output	T_{IMO}		7.2		5.8		5.0		4.2
Carry Delays									
Incremental delay per bit	T_{CY}		0.7		0.6		0.5		0.5
Carry-in overhead from DI	T_{CYDI}		1.8		1.6		1.5		1.3
Carry-in overhead from F	T_{CYL}		3.7		3.2		2.9		2.3
Carry-out overhead to DO	T_{CYO}		4.0		3.2		2.5		2.0
Sequential Delays									
Clock (CK) to out (Q) (Flip-Flop)	T_{CKO}		5.8		4.9		4.0		3.5
Gate (Latch enable) going active to out (Q)	T_{GO}		9.2		7.4		5.9		4.7
Set-up Time Before Clock (CK)									
F inputs	T_{ICK}	2.3		1.8		1.4		1.0	
F inputs via F5_MUX	T_{MICK}	3.8		3.0		2.5		2.1	
DI input	T_{DICK}	0.8		0.5		0.4		0.3	
CE input	T_{EICK}	1.6		1.2		0.9		0.7	
Hold Times After Clock (CK)									
F inputs	T_{CKI}	0		0		0		0	
F inputs via F5_MUX	T_{CKMI}	0		0		0		0	
DI input	T_{CKDI}	0		0		0		0	
CE input	T_{CKEI}	0		0		0		0	
Clock Widths									
Clock High Time	T_{CH}	6.0		6.0		6.0		6.0	
Clock Low Time	T_{CL}	6.0		6.0		6.0		6.0	
Export Control Max. flip-flop toggle rate (MHz)	F_{TOG}		83		83		83		83
Reset Delays									
Width (High)	T_{CLRW}	6.0		6.0		6.0		6.0	
Delay from CLR to Q (Flip-Flop)	T_{CLR}		7.7		6.3		5.1		4.0
Delay from CLR to Q (Latch)	T_{CLRL}		6.5		5.2		4.2		3.2
Global Reset Delays (see Note 2)									
Width (High)	T_{GCLRW}	6.0		6.0		6.0			6.0
Delay from internal GCLR to Q	T_{GCLR}		14.7		12.1		9.1		8.0
		PRELIMINARY						ADVANCE	

Note: 1. The CLB K to Q output delay (T_{CKO}) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold-time requirement (T_{CKDI}) of any CLB on the same die.
2. Timing is based upon the XC5215 device. For other devices, see XACT*step* Timing Calculator.

XC5200 Guaranteed Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the Global Buffer specifications. The XACT*step* delay calculator uses this indirect method, and may overestimate because of worst-case assumptions. When there is a discrepancy between these two methods, the values listed below should be used, and the derived values should be considered conservative overestimates.

			Speed Grade	-6	-5	-4	-3
Description		**Symbol**	**Device**	**Max (ns)**	**Max (ns)**	**Max (ns)**	**Max (ns)**
Global Clock to Output Pad (fast) 		T_{ICKOF} (Max)	XC5202	16.9	15.1		
			XC5204	17.1	15.3		
			XC5206	17.2	15.4		
			XC5210	17.2	15.4	14.2	13.0
			XC5215	19.0	17.0		
Global Clock to Output Pad (slew-limited) 		T_{ICKO} (Max)	XC5202	21.4	18.7		
			XC5204	21.6	18.9		
			XC5206	21.7	19.0		
			XC5210	21.7	19.0	17.3	17.0
			XC5215	24.3	21.2		
Input Set-up Time (no delay) to CLB Flip-Flop 		T_{PSUF} (Min)	XC5202	2.5	1.8		
			XC5204	2.3	1.6		
			XC5206	2.2	1.5		
			XC5210	2.2	1.5	1.2	0.8
			XC5215	0.5	0		
Input Hold Time (no delay) to CLB Flip-Flop 		T_{PHF} (Min)	XC5202	3.2	2.7		
			XC5204	3.4	2.9		
			XC5206	3.5	3.0		
			XC5210	3.5	3.0	2.8	2.6
			XC5215	4.4	3.9		
Input Set-up Time (with delay) to CLB Flip-Flop 		T_{PSU} (Min)	XC5202	8.8	7.7		
			XC5204	8.6	7.5		
			XC5206	8.5	7.4		
			XC5210	8.5	7.4	6.0	5.0
			XC5215	6.8	5.7		
Input Hold Time (with delay) to CLB Flip-Flop 		T_{PH} (Min)	XC52xx	0	0	0	0
				PRELIMINARY			ADVANCE

Note: 1. These measurements assume that the flip-flop has a direct connect to or from the IOB. XACT-Performance can be used to assure that direct connects are used.
2. When testing outputs (fast or slew-limited), half of the outputs on one side of the device are switching.
3. Die-size-dependent parameters are based upon XC5210 characterization. Production specifications will vary with array size.

XC5200 IOB Switching Characteristic Guidelines

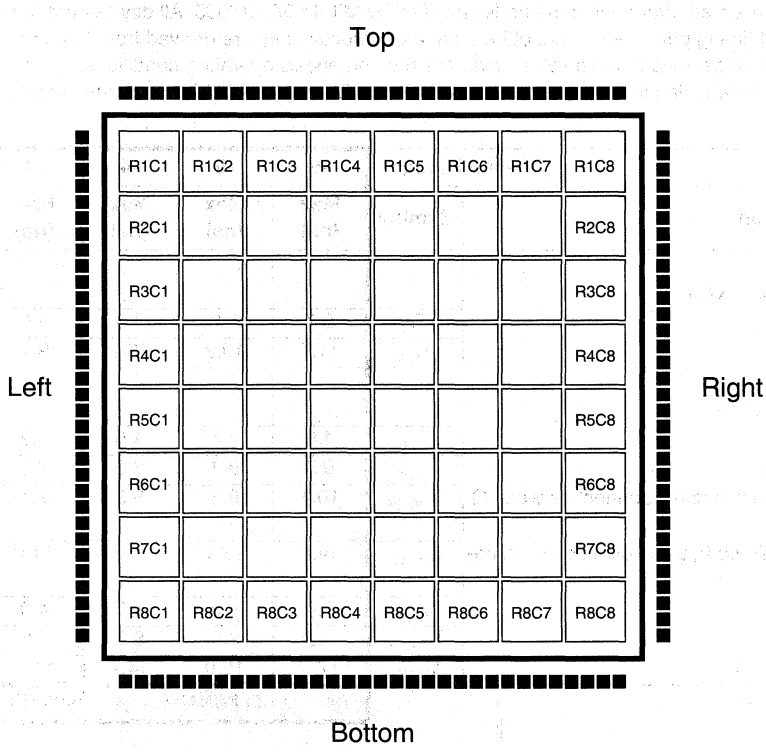
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT*step* timing calculator and used in the simulator.

Speed Grade		-6	-5	-4	-3
Description	**Symbol**	**Max (ns)**	**Max (ns)**	**Max (ns)**	**Max (ns)**
Input					
Propagation Delays from CMOS or TTL Levels					
Pad to I (no delay)	T_{PI}	5.7	5.0	4.8	4.0
Pad to I (with delay)	T_{PID}	11.4	10.2	10.2	9.4
Output					
Propagation Delays to CMOS or TTL Levels					
Output (O) to Pad (fast)	T_{OPF}	4.6	4.5	4.5	4.2
Output (O) to Pad (slew-limited)	T_{OPS}	9.5	8.4	8.0	7.5
From clock (CK) to output pad (fast), using direct connect between Q and output (O)	T_{OKPOF}	10.1	9.3	8.3	7.1
From clock (CK) to output pad (slew-limited), using direct connect between Q and output (O)	T_{OKPOS}	14.9	13.1	11.8	11.0
3-state to Pad active (fast)	T_{TSONF}	5.6	5.2	4.9	4.0
3-state to Pad active (slew-limited)	T_{TSONS}	10.4	9.0	8.3	7.8
Internal GTS to Pad active (see Note 3)	T_{GTS}	17.7	15.9	14.7	14.0
		PRELIMINARY			ADVANCE

Note: 1. Timing is measured at pin threshold, with 50-pF external capacitance loads. **Slew-limited** output rise/fall times are approximately two times longer than **fast** output rise/fall times. For the effect of capacitive loads on ground bounce, see "XC4000 Series Technical Information" in "Section 13, Product Technical Information" in the 1996 Xilinx *Programmable Logic Data Book.*

2. Unused and unbonded IOBs are configured by default as inputs with internal pull-up resistors.
3. Timing is based upon the XC5210 device. For other devices, see XACT*step* Timing Calculator.

XC5200 CLB-to-Pad Diagrams

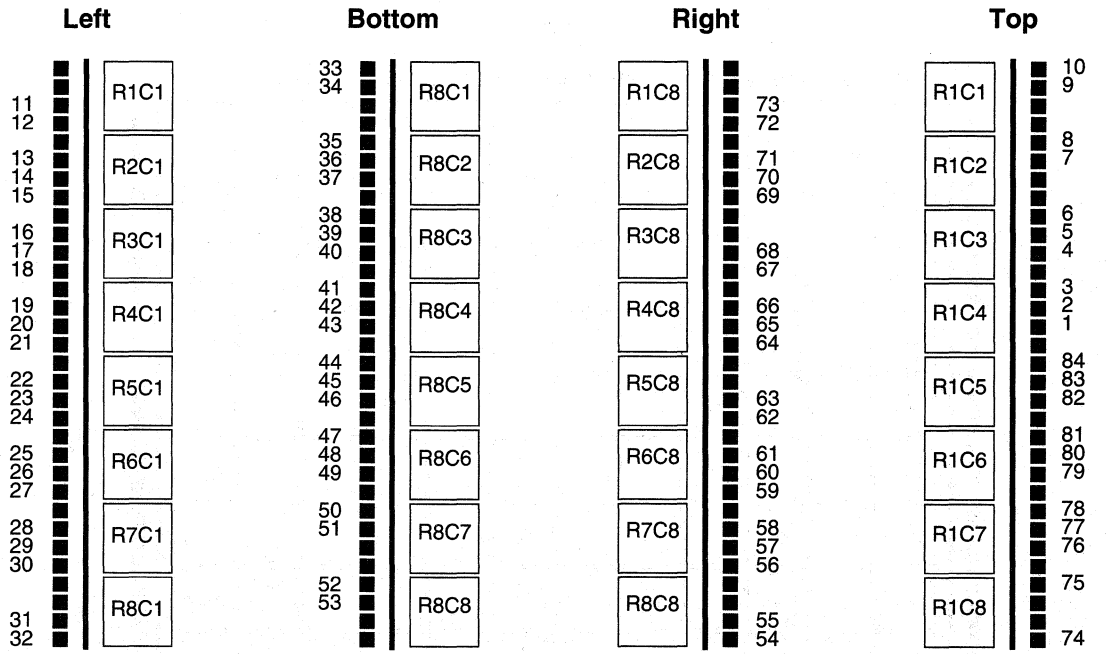


KEY:

■ I/O Pad

R#C# CLB, identified by R#C# = row and column numbers

Figure 18: XC5202 CLB-to-Pad Relationship



Note: Pad numbers (1, 2, ..., 84) refer to die pads, not external device pins.
See the XC5202 pinout table beginning on page 223.

Figure 19: XC5202 CLB-to-Pad Relationship (Detail)

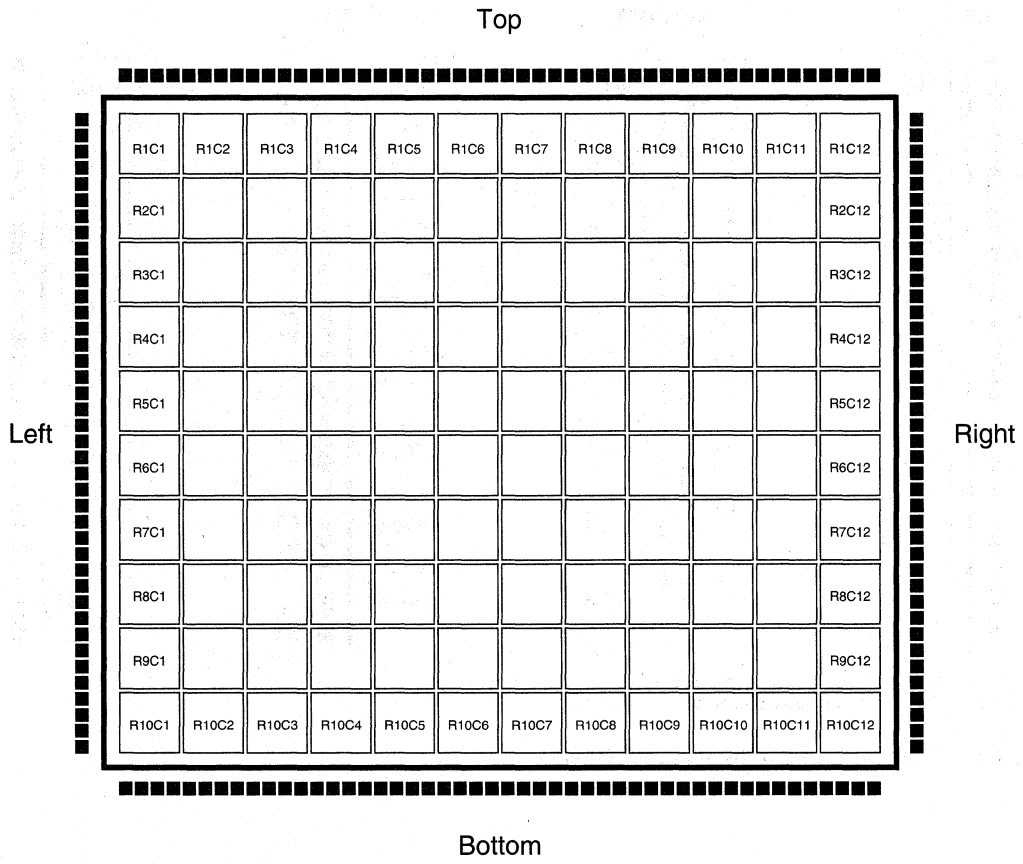
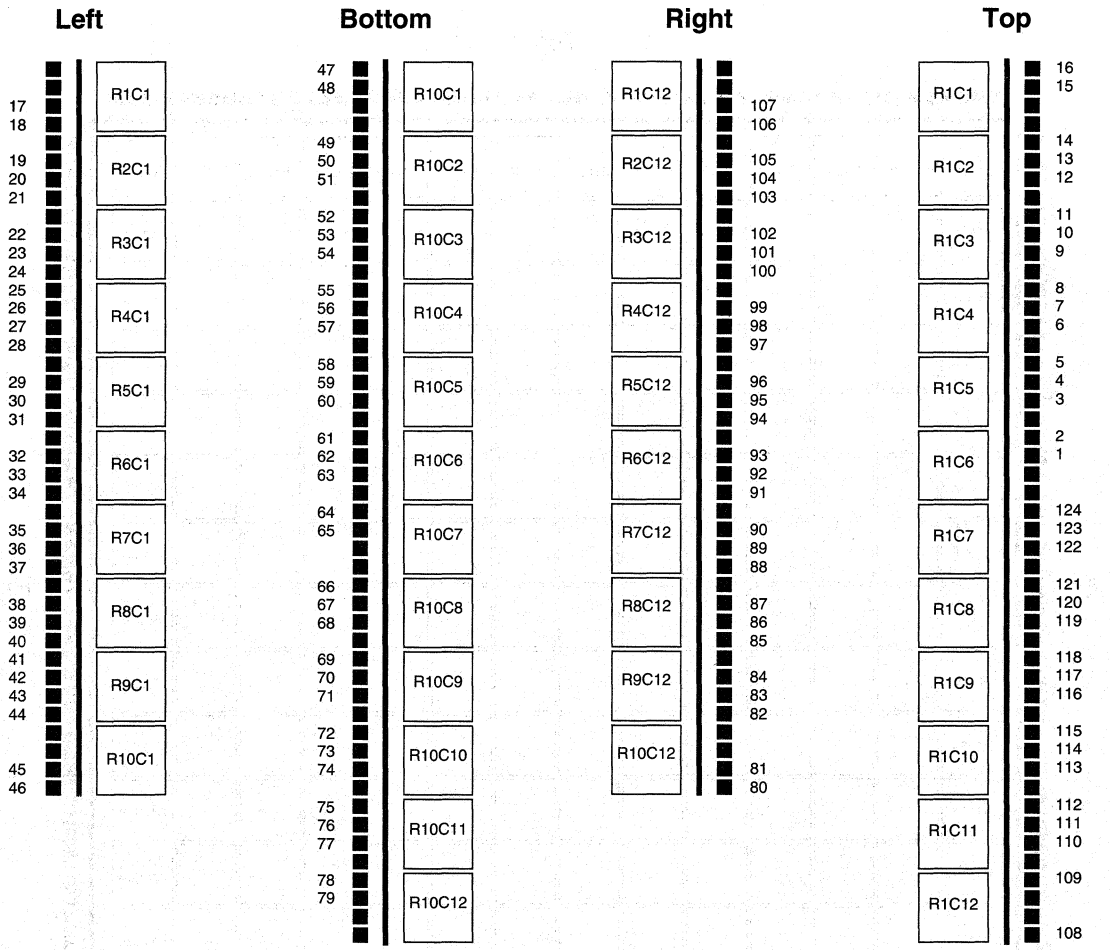


Figure 20: XC5204 CLB-to-Pad Relationship



Note: Pad numbers (1, 2, ..., 124) refer to die pads, not external device pins.
See the XC5204 pinout table beginning on page 226.

Figure 21: XC5204 CLB-to-Pad Relationship (Detail)

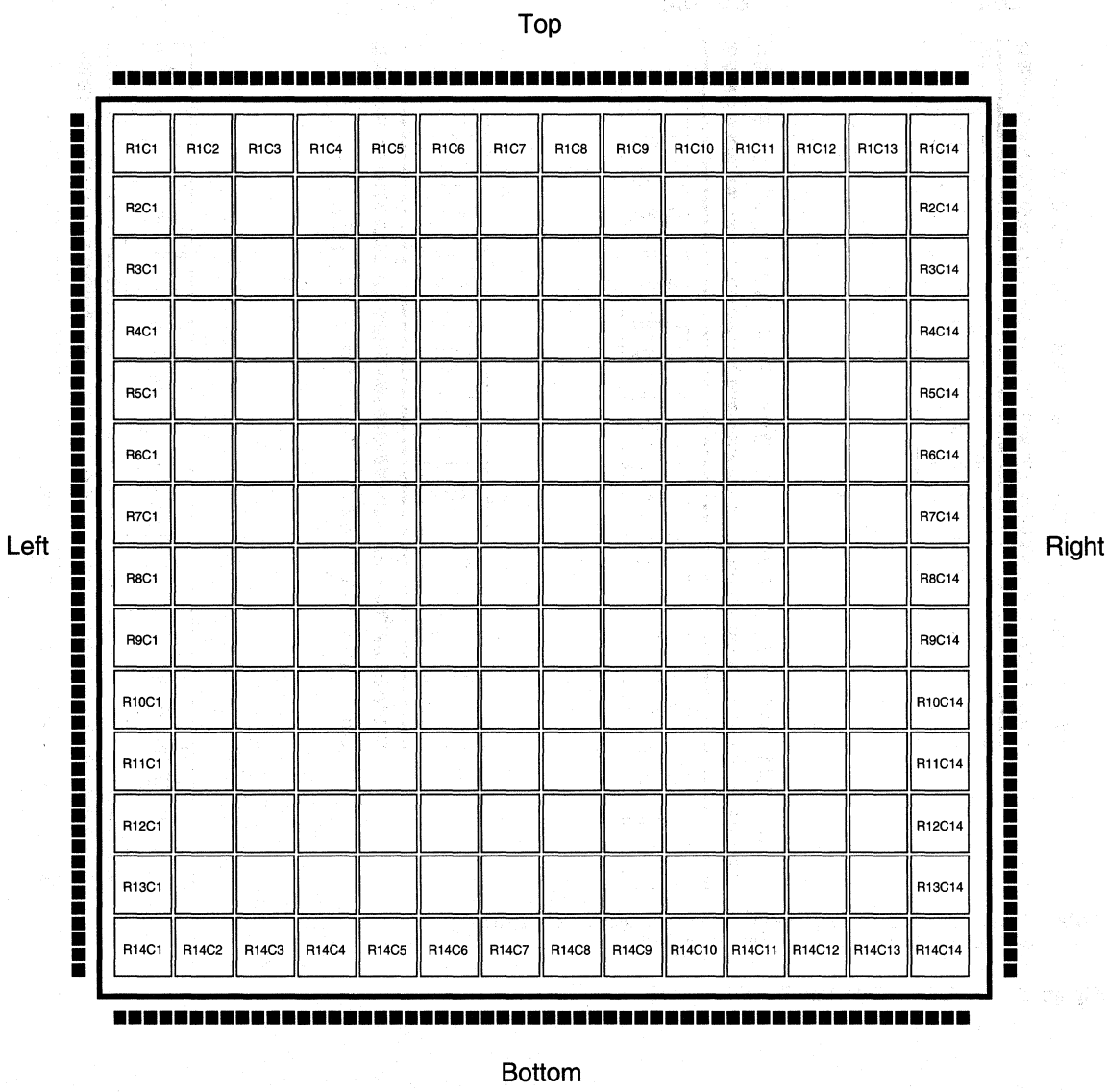
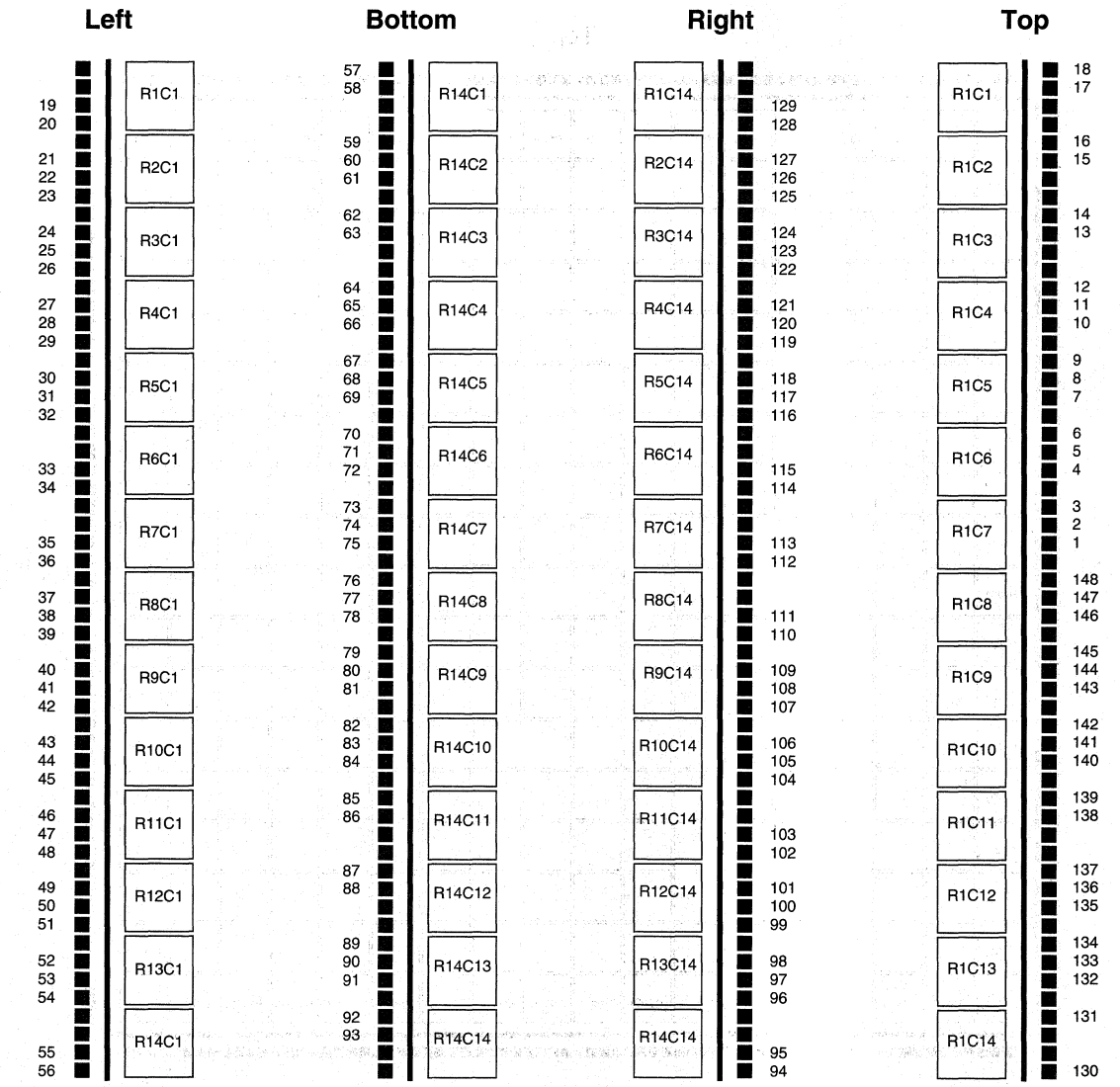
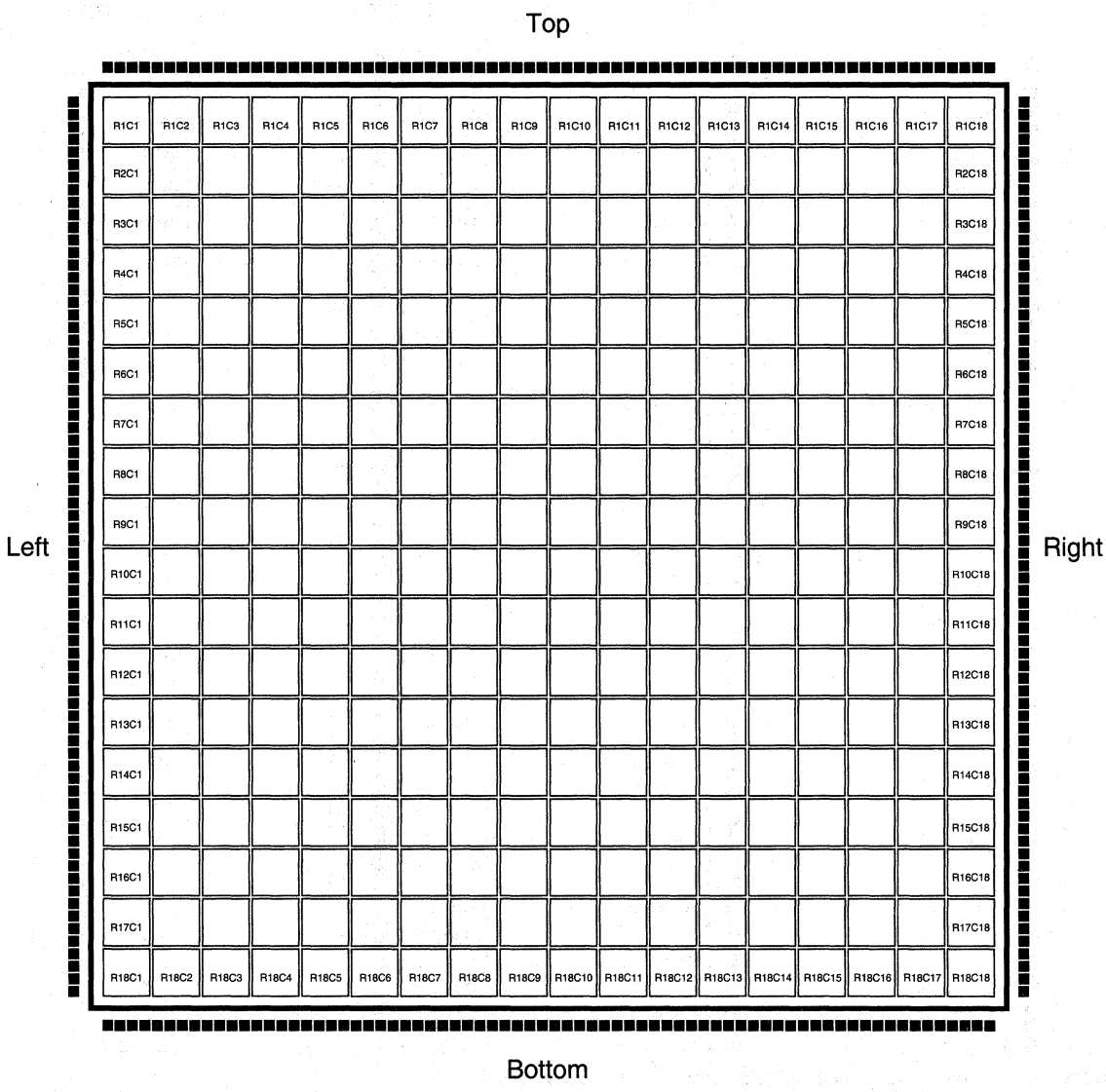


Figure 22: XC5206 CLB-to-Pad Relationship



Note: Pad numbers (1, 2, ..., 148) refer to die pads, not external device pins.
See the XC5206 pinout table beginning on page 230.

Figure 23: XC5206 CLB-to-Pad Relationship (Detail)

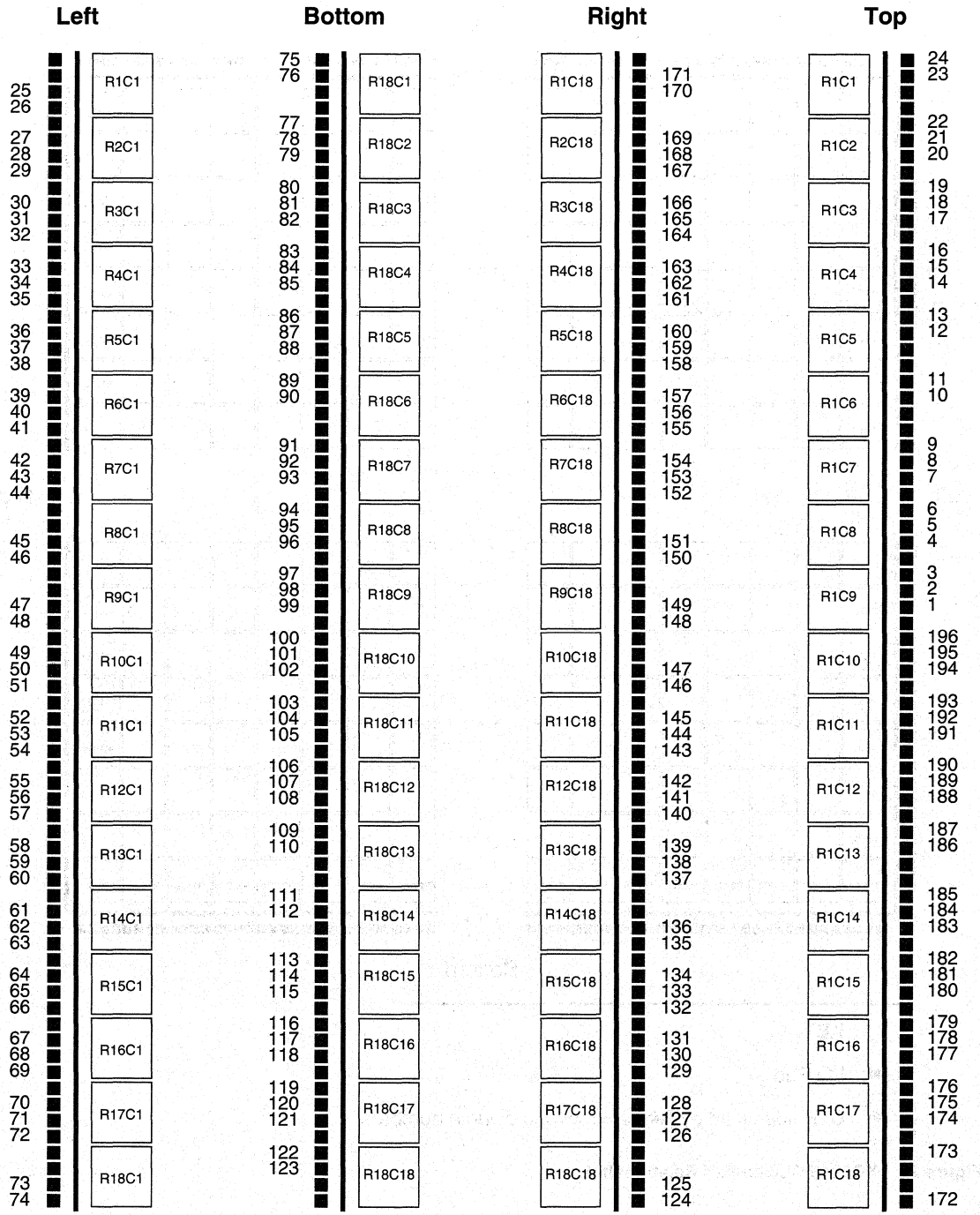


KEY:

- I/O Pad

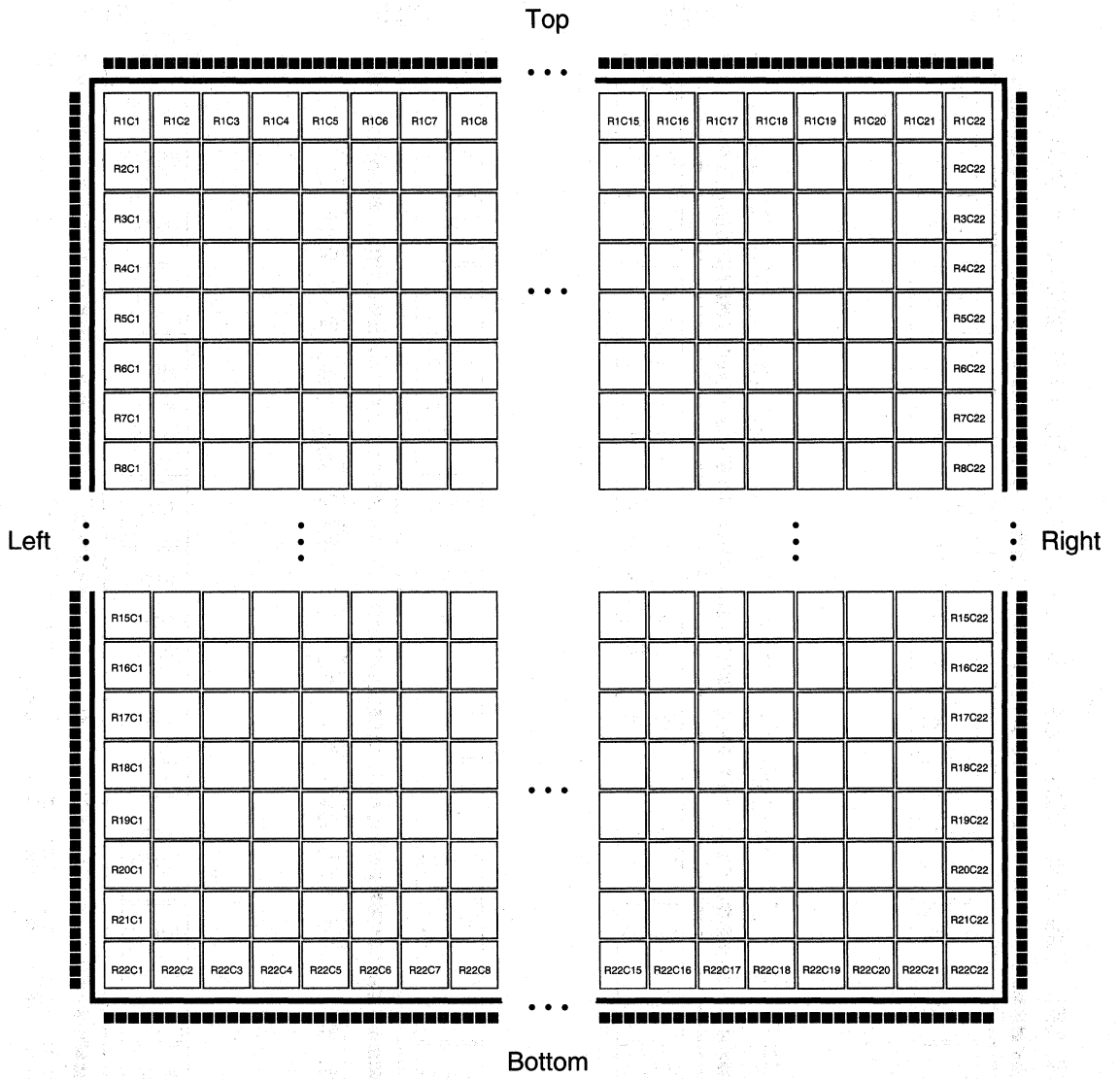
R#C# CLB, identified by R#C# = row and column numbers

Figure 24: XC5210 CLB-to-Pad Relationship



Note: Pad numbers (1, 2, ..., 196) refer to die pads, not external device pins.
See the XC5210 pinout table beginning on page 235.

Figure 25: XC5210 CLB-to-Pad Relationship (Detail)

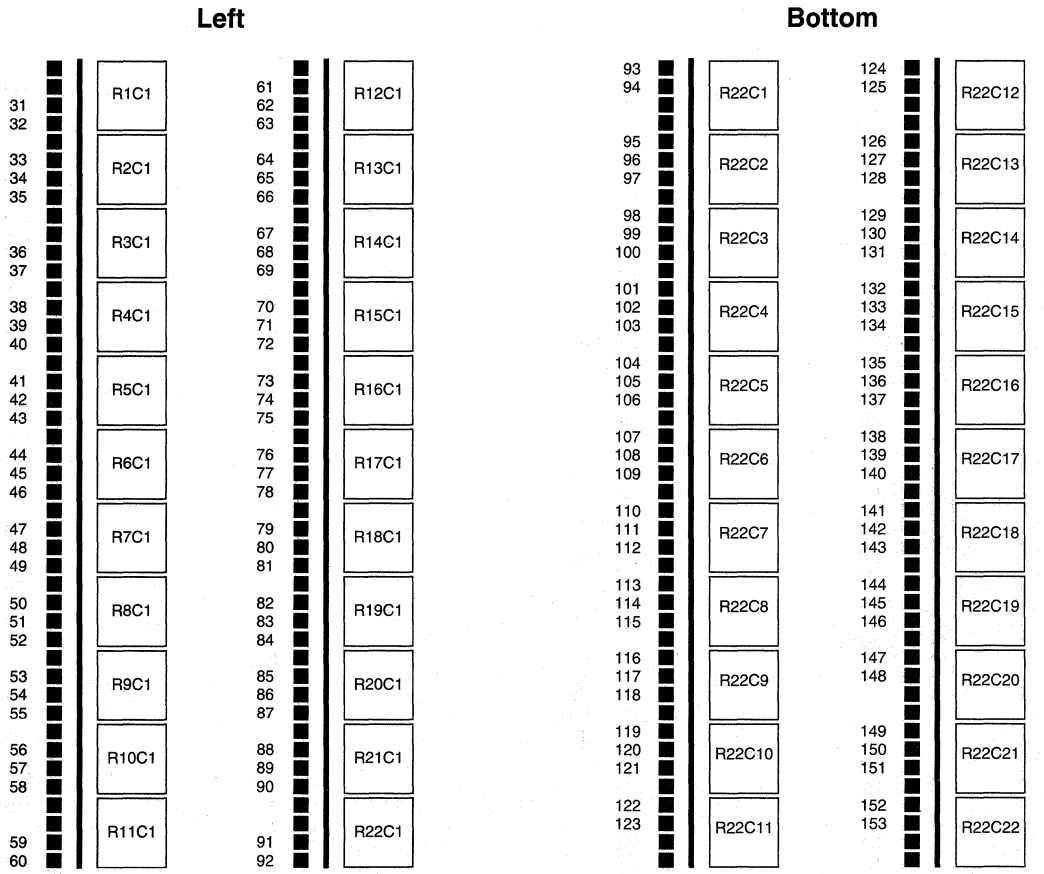


KEY:

- I/O Pad

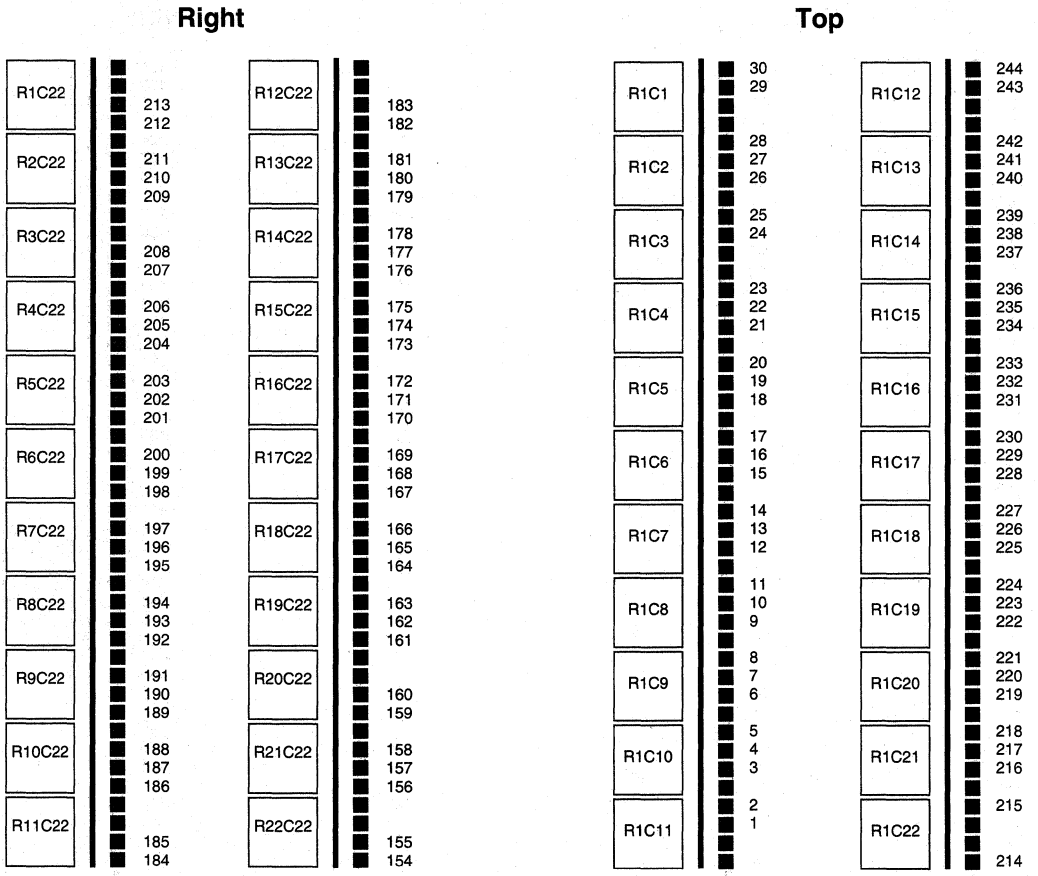
R#C# CLB, identified by R#C# = row and column numbers

Figure 26: XC5215 CLB-to-Pad Relationship



Note: Pad numbers (31, 32, ..., 153) refer to die pads, not external device pins. See the XC5215 pinout table beginning on page 241.

Figure 27: XC5215 CLB-to-Pad Relationship (Left/Bottom Detail)



Note: Pad numbers (1, 2, ..., 244) refer to die pads, not external device pins. See the XC5215 pinout table beginning on page 241.

Figure 28: XC5215 CLB-to-Pad Relationship (Right/Top Detail)

Device-Specific Pinout Tables

Pin Locations for XC5202 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
	VCC	2	92	89	128	H3	-
1.	I/O (A8)	3	93	90	129	H1	51
2.	I/O (A9)	4	94	91	130	G1	54
3.	I/O	-	95	92	131	G2	57
4.	I/O	-	96	93	132	G3	63
5.	I/O (A10)	5	97	94	133	F1	66
6.	I/O (A11)	6	98	95	134	F2	69
	-	-	-	-	135*	-	-
	-	-	-	-	136*	-	-
	GND	-	-	-	137	F3	-
7.	I/O (A12)	7	99	96	138	E3	78
8.	I/O (A13)	8	100	97	139	C1	81
	-	-	-	-	140*	-	-
	-	-	-	-	141*	-	-
9.	I/O (A14)	9	1	98	142	B1	90
10.	I/O (A15)	10	2	99	143	B2	93
	VCC	11	3	100	144	C3	-
	GND	12	4	1	1	C4	-
11.	GCK1 (A16, I/O)	13	5	2	2	B3	102
12.	I/O (A17)	14	6	3	3	A1	105
	-	-	-	-	4*	-	-
	-	-	-	-	5*	-	-
13.	I/O (TDI)	15	7	4	6	B4	111
14.	I/O (TCK)	16	8	5	7	A3	114
	GND	-	-	-	8	C6	-
	-	-	-	-	9*	-	-
	-	-	-	-	10*	-	-
15.	I/O (TMS)	17	9	6	11	A5	117
16.	I/O	18	10	7	12	C7	123
17.	I/O	-	-	-	13	B7	126
18.	I/O	-	11	8	14	A6	129
19.	I/O	19	12	9	15	A7	135
20.	I/O	20	13	10	16	A8	138
	GND	21	14	11	17	C8	-
	VCC	22	15	12	18	B8	-
21.	I/O	23	16	13	19	C9	141
22.	I/O	24	17	14	20	B9	147
23.	I/O	-	18	15	21	A9	150
24.	I/O	-	-	-	22	B10	153
25.	I/O	25	19	16	23	C10	159
26.	I/O	26	20	17	24	A10	162
	-	-	-	-	25*	-	-
	-	-	-	-	26*	-	-
	GND	-	-	-	27	C11	-
27.	I/O	27	21	18	28	B12	165
28.	I/O	-	22	19	29	A13	171
	-	-	-	-	30*	-	-
	-	-	-	-	31*	-	-
29.	I/O	28	23	20	32	B13	174

Pin Locations for XC5202 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
30.	I/O	29	24	21	33	B14	177
31.	M1 (I/O)	30	25	22	34	A15	186
	GND	31	26	23	35	C13	-
32.	M0 (I/O)	32	27	24	36	A16	189
	VCC	33	28	25	37	C14	-
33.	M2 (I/O)	34	29	26	38	B15	192
34.	GCK2 (I/O)	35	30	27	39	B16	195
35.	I/O (HDC)	36	31	28	40	D14	204
	-	-	-	-	41*	-	-
	-	-	-	-	42*	-	-
36.	I/O	-	32	29	43	E14	207
37.	I/O (LDC)	37	33	30	44	C16	210
	GND	-	-	-	45	F14	-
	-	-	-	-	46*	-	-
	-	-	-	-	47*	-	-
38.	I/O	38	34	31	48	F16	216
39.	I/O	39	35	32	49	G14	219
40.	I/O	-	36	33	50	G15	222
41.	I/O	-	37	34	51	G16	228
42.	I/O	40	38	35	52	H16	231
43.	I/O ($\overline{ERR}$, $\overline{INIT}$)	41	39	36	53	H15	234
	VCC	42	40	37	54	H14	-
	GND	43	41	38	55	J14	-
44.	I/O	44	42	39	56	J15	240
45.	I/O	45	43	40	57	J16	243
46.	I/O	-	44	41	58	K16	246
47.	I/O	-	45	42	59	K15	252
48.	I/O	46	46	43	60	K14	255
49.	I/O	47	47	44	61	L16	258
	-	-	-	-	62*	-	-
	-	-	-	-	63*	-	-
	GND	-	-	-	64	L14	-
50.	I/O	48	48	45	65	P16	264
51.	I/O	49	49	46	66	M14	267
	-	-	-	-	67*	-	-
	-	-	-	-	68*	-	-
52.	I/O	50	50	47	69	N14	276
53.	I/O	51	51	48	70	R16	279
	GND	52	52	49	71	P14	-
	DONE	53	53	50	72	R15	-
	VCC	54	54	51	73	P13	-
	PROG	55	55	52	74	R14	-
54.	I/O (D7)	56	56	53	75	T16	288
55.	GCK3 (I/O)	57	57	54	76	T15	291
	-	-	-	-	77*	-	-
	-	-	-	-	78*	-	-
56.	I/O (D6)	58	58	55	79	T14	300
57.	I/O	-	59	56	80	T13	303
	GND	-	-	-	81	P11	-
	-	-	-	-	82*	-	-

Pin Locations for XC5202 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
	-	-	-	-	83*	-	-
58.	I/O (D5)	59	60	57	84	T10	306
59.	I/O ($\overline{CS0}$)	60	61	58	85	P10	312
60.	I/O	-	62	59	86	R10	315
61.	I/O	-	63	60	87	T9	318
62.	I/O (D4)	61	64	61	88	R9	324
63.	I/O	62	65	62	89	P9	327
	VCC	63	66	63	90	R8	-
	GND	64	67	64	91	P8	-
64.	I/O (D3)	65	68	65	92	T8	336
65.	I/O ($\overline{RS}$)	66	69	66	93	T7	339
66.	I/O	-	70	67	94	T6	342
67.	I/O	-	-	-	95	R7	348
68.	I/O (D2)	67	71	68	96	P7	351
69.	I/O	68	72	69	97	T5	360
	-	-	-	-	98*	-	-
	-	-	-	-	99*	-	-
	GND	-	-	-	100	P6	-
70.	I/O (D1)	69	73	70	101	T3	363
71.	I/O ($\overline{RCLK}$-$\overline{BUSY}$/ RDY)	70	74	71	102	P5	366
	-	-	-	-	103*	-	-
	-	-	-	-	104*	-	-
72.	I/O (D0, DIN)	71	75	72	105	P4	372
73.	I/O (DOUT)	72	76	73	106	T2	375
	CCLK	73	77	74	107	R2	-
	VCC	74	78	75	108	P3	-
74.	I/O (TDO)	75	79	76	109	T1	0
	GND	76	80	77	110	N3	-
75.	I/O (A0, $\overline{WS}$)	77	81	78	111	R1	9
76.	GCK4 (A1, I/O)	78	82	79	112	P2	15
	-	-	-	-	113*	-	-
	-	-	-	-	114*	-	-
77.	I/O (A2, CS1)	79	83	80	115	P1	18
78.	I/O (A3)	80	84	81	116	N1	21
	-	-	-	-	117*	-	-
	GND	-	-	-	118	L3	-
	-	-	-	-	119*	-	-
	-	-	-	-	120*	-	-
79.	I/O (A4)	81	85	82	121	K3	27
80.	I/O (A5)	82	86	83	122	K2	30
81.	I/O	-	87	84	123	K1	33
82.	I/O	-	88	85	124	J1	39
83.	I/O (A6)	83	89	86	125	J2	42
84.	I/O (A7)	84	90	87	126	J3	45
	GND	1	91	88	127	H2	-

Notes: * Indicates unconnected package pins.
† leading numbers refer to bonded pad, shown in Figure 18 or Figure 19.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD

Pin Locations for XC5204 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
	VCC	2	92	89	128	H3	142	-
1.	I/O (A8)	3	93	90	129	H1	143	78
2.	I/O (A9)	4	94	91	130	G1	144	81
3.	I/O	-	95	92	131	G2	145	87
4.	I/O	-	96	93	132	G3	146	90
5.	I/O (A10)	5	97	94	133	F1	147	93
6.	I/O (A11)	6	98	95	134	F2	148	99
7.	I/O	-	-	-	135	E1	149	102
8.	I/O	-	-	-	136	E2	150	105
	GND	-	-	-	137	F3	151	-
9.	I/O	-	-	-	-	D1	152	111
10.	I/O	-	-	-	-	D2	153	114
11.	I/O (A12)	7	99	96	138	E3	154	117
12.	I/O (A13)	8	100	97	139	C1	155	123
13.	I/O	-	-	-	140	C2	156	126
14.	I/O	-	-	-	141	D3	157	129
15.	I/O (A14)	9	1	98	142	B1	158	138
16.	I/O (A15)	10	2	99	143	B2	159	141
	VCC	11	3	100	144	C3	160	-
	GND	12	4	1	1	C4	1	-
17.	GCK1 (A16, I/O)	13	5	2	2	B3	2	150
18.	I/O (A17)	14	6	3	3	A1	3	153
19.	I/O	-	-	-	4	A2	4	159
20.	I/O	-	-	-	5	C5	5	162
21.	I/O (TDI)	15	7	4	6	B4	6	165
22.	I/O (TCK)	16	8	5	7	A3	7	171
	-	-	-	-	-	-	8*	-
	-	-	-	-	-	-	9*	-
	GND	-	-	-	8	C6	10	-
23.	I/O	-	-	-	9	B5	11	174
24.	I/O	-	-	-	10	B6	12	177
25.	I/O (TMS)	17	9	6	11	A5	13	180
26.	I/O	18	10	7	12	C7	14	183
27.	I/O	-	-	-	13	B7	15	186
28.	I/O	-	11	8	14	A6	16	189
29.	I/O	19	12	9	15	A7	17	195
30.	I/O	20	13	10	16	A8	18	198
	GND	21	14	11	17	C8	19	-
	VCC	22	15	12	18	B8	20	-
31.	I/O	23	16	13	19	C9	21	201
32.	I/O	24	17	14	20	B9	22	207
33.	I/O	-	18	15	21	A9	23	210
34.	I/O	-	-	-	22	B10	24	213
35.	I/O	25	19	16	23	C10	25	219
36.	I/O	26	20	17	24	A10	26	222
37.	I/O	-	-	-	25	A11	27	225
38.	I/O	-	-	-	26	B11	28	231
	GND	-	-	-	27	C11	29	-
	-	-	-	-	-	-	30*	-
	-	-	-	-	-	-	31*	-

Pin Locations for XC5204 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
39.	I/O	27	21	18	28	B12	32	234
40.	I/O	-	22	19	29	A13	33	237
41.	I/O	-	-	-	30	A14	34	240
42.	I/O	-	-	-	31	C12	35	243
43.	I/O	28	23	20	32	B13	36	246
44.	I/O	29	24	21	33	B14	37	249
45.	M1 (I/O)	30	25	22	34	A15	38	258
	GND	31	26	23	35	C13	39	-
46.	M0 (I/O)	32	27	24	36	A16	40	261
	VCC	33	28	25	37	C14	41	-
47.	M2 (I/O)	34	29	26	38	B15	42	264
48.	GCK2 (I/O)	35	30	27	39	B16	43	267
49.	I/O (HDC)	36	31	28	40	D14	44	276
50.	I/O	-	-	-	41	C15	45	279
51.	I/O	-	-	-	42	D15	46	282
52.	I/O	-	32	29	43	E14	47	288
53.	I/O (LDC)	37	33	30	44	C16	48	291
54.	I/O	-	-	-	-	E15	49	294
55.	I/O	-	-	-	-	D16	50	300
	GND	-	-	-	45	F14	51	-
56.	I/O	-	-	-	46	F15	52	303
57.	I/O	-	-	-	47	E16	53	306
58.	I/O	38	34	31	48	F16	54	312
59.	I/O	39	35	32	49	G14	55	315
60.	I/O	-	36	33	50	G15	56	318
61.	I/O	-	37	34	51	G16	57	324
62.	I/O	40	38	35	52	H16	58	327
63.	I/O ($\overline{ERR}$, $\overline{INIT}$)	41	39	36	53	H15	59	330
	VCC	42	40	37	54	H14	60	-
	GND	43	41	38	55	J14	61	-
64.	I/O	44	42	39	56	J15	62	336
65.	I/O	45	43	40	57	J16	63	339
66.	I/O	-	44	41	58	K16	64	348
67.	I/O	-	45	42	59	K15	65	351
68.	I/O	46	46	43	60	K14	66	354
69.	I/O	47	47	44	61	L16	67	360
70.	I/O	-	-	-	62	M16	68	363
71.	I/O	-	-	-	63	L15	69	366
	GND	-	-	-	64	L14	70	-
72.	I/O	-	-	-	-	N16	71	372
73.	I/O	-	-	-	-	M15	72	375
74.	I/O	48	48	45	65	P16	73	378
75.	I/O	49	49	46	66	M14	74	384
76.	I/O	-	-	-	67	N15	75	387
77.	I/O	-	-	-	68	P15	76	390
78.	I/O	50	50	47	69	N14	77	396
79.	I/O	51	51	48	70	R16	78	399
	GND	52	52	49	71	P14	79	-
	DONE	53	53	50	72	R15	80	-
	VCC	54	54	51	73	P13	81	-
	PROG	55	55	52	74	R14	82	-

Pin Locations for XC5204 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
80.	I/O (D7)	56	56	53	75	T16	83	408
81.	GCK3 (I/O)	57	57	54	76	T15	84	411
82.	I/O	-	-	-	77	R13	85	420
83.	I/O	-	-	-	78	P12	86	423
84.	I/O (D6)	58	58	55	79	T14	87	426
85.	I/O	-	59	56	80	T13	88	432
	-	-	-	-	-	-	89*	-
	-	-	-	-	-	-	90*	-
	GND	-	-	-	81	P11	91	-
86.	I/O	-	-	-	82	R11	92	435
87.	I/O	-	-	-	83	T11	93	438
88.	I/O (D5)	59	60	57	84	T10	94	444
89.	I/O ($\overline{CS0}$)	60	61	58	85	P10	95	447
90.	I/O	-	62	59	86	R10	96	450
91.	I/O	-	63	60	87	T9	97	456
92.	I/O (D4)	61	64	61	88	R9	98	459
93.	I/O	62	65	62	89	P9	99	462
	VCC	63	66	63	90	R8	100	-
	GND	64	67	64	91	P8	101	-
94.	I/O (D3)	65	68	65	92	T8	102	468
95.	I/O ($\overline{RS}$)	66	69	66	93	T7	103	471
96.	I/O	-	70	67	94	T6	104	474
97.	I/O	-	-	-	95	R7	105	480
98.	I/O (D2)	67	71	68	96	P7	106	483
99.	I/O	68	72	69	97	T5	107	486
100.	I/O	-	-	-	98	R6	108	492
101.	I/O	-	-	-	99	T4	109	495
	GND	-	-	-	100	P6	110	-
	-	-	-	-	-	-	111*	-
	-	-	-	-	-	-	112*	-
102.	I/O (D1)	69	73	70	101	T3	113	498
103.	I/O ($\overline{RCLK}$-BUSY/RDY)	70	74	71	102	P5	114	504
104.	I/O	-	-	-	103	R4	115	507
105.	I/O	-	-	-	104	R3	116	510
106.	I/O (D0, DIN)	71	75	72	105	P4	117	516
107.	I/O (DOUT)	72	76	73	106	T2	118	519
	CCLK	73	77	74	107	R2	119	-
	VCC	74	78	75	108	P3	120	-
108.	I/O (TDO)	75	79	76	109	T1	121	0
	GND	76	80	77	110	N3	122	-
109.	I/O (A0, $\overline{WS}$)	77	81	78	111	R1	123	9
110.	GCK4 (A1, I/O)	78	82	79	112	P2	124	15
111.	I/O	-	-	-	113	N2	125	18
112.	I/O	-	-	-	114	M3	126	21
113.	I/O (A2, CS1)	79	83	80	115	P1	127	27
114.	I/O (A3)	80	84	81	116	N1	128	30
115.	I/O	-	-	-	117	M2	129	33
116.	I/O	-	-	-	-	M1	130	39
	GND	-	-	-	118	L3	131	-
117.	I/O	-	-	-	119	L2	132	42
118.	I/O	-	-	-	120	L1	133	45

Pin Locations for XC5204 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
119.	I/O (A4)	81	85	82	121	K3	134	51
120.	I/O (A5)	82	86	83	122	K2	135	54
	-	-	-	-	-	-	136*	-
121.	I/O	-	87	84	123	K1	137	57
122.	I/O	-	88	85	124	J1	138	63
123.	I/O (A6)	83	89	86	125	J2	139	66
124.	I/O (A7)	84	90	87	126	J3	140	69
	GND	1	91	88	127	H2	141	-

Notes: * Indicates unconnected package pins.
† leading numbers refer to bonded pad, shown in Figure 20 or Figure 21.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD

Pin Locations for XC5206 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
	VCC	2	92	89	128	142	155	J4	183	-
1.	I/O (A8)	3	93	90	129	143	156	J3	184	87
2.	I/O (A9)	4	94	91	130	144	157	J2	185	90
3.	I/O	-	95	92	131	145	158	J1	186	93
4.	I/O	-	96	93	132	146	159	H1	187	99
5.	I/O	-	-	-	-	-	160	H2	188	102
6.	I/O	-	-	-	-	-	161	H3	189	105
7.	I/O (A10)	5	97	94	133	147	162	G1	190	111
8.	I/O (A11)	6	98	95	134	148	163	G2	191	114
9.	I/O	-	-	-	135	149	164	F1	192	117
10.	I/O	-	-	-	136	150	165	E1	193	123
	GND	-	-	-	137	151	166	G3	194	-
	-	-	-	-	-	-	-	-	195*	-
	-	-	-	-	-	-	167*	-	196*	-
11.	I/O	-	-	-	-	152	168	C1	197	126
12.	I/O	-	-	-	-	153	169	E2	198	129
13.	I/O (A12)	7	99	96	138	154	170	F3	199	138
14.	I/O (A13)	8	100	97	139	155	171	D2	200	141
15.	I/O	-	-	-	140	156	172	B1	201	150
16.	I/O	-	-	-	141	157	173	E3	202	153
17.	I/O (A14)	9	1	98	142	158	174	C2	203	162
18.	I/O (A15)	10	2	99	143	159	175	B2	204	165
	VCC	11	3	100	144	160	176	D3	205	-
	-	-	-	-	-	-	-	-	206*	-
	-	-	-	-	-	-	-	-	207*	-
	-	-	-	-	-	-	-	-	208*	-
	-	-	-	-	-	-	-	-	1*	-
	GND	12	4	1	1	1	1	D4	2	-
	-	-	-	-	-	-	-	-	3*	-
19.	GCK1 (A16, I/O)	13	5	2	2	2	2	C3	4	174
20.	I/O (A17)	14	6	3	3	3	3	C4	5	177
21.	I/O	-	-	-	4	4	4	B3	6	183
22.	I/O	-	-	-	5	5	5	C5	7	186
23.	I/O (TDI)	15	7	4	6	6	6	A2	8	189
24.	I/O (TCK)	16	8	5	7	7	7	B4	9	195
25.	I/O	-	-	-	-	8	8	C6	10	198
26.	I/O	-	-	-	-	9	9	A3	11	201
	-	-	-	-	-	-	-	-	12*	-
	-	-	-	-	-	-	-	-	13*	-
	GND	-	-	-	8	10	10	C7	14	-
27.	I/O	-	-	-	9	11	11	A4	15	207
28.	I/O	-	-	-	10	12	12	A5	16	210
29.	I/O (TMS)	17	9	6	11	13	13	B7	17	213
30.	I/O	18	10	7	12	14	14	A6	18	219
31.	I/O	-	-	-	-	-	15	C8	19	222
32.	I/O	-	-	-	-	-	16	A7	20	225
33.	I/O	-	-	-	13	15	17	B8	21	234
34.	I/O	-	11	8	14	16	18	A8	22	237
35.	I/O	19	12	9	15	17	19	B9	23	246
36.	I/O	20	13	10	16	18	20	C9	24	249

Pin Locations for XC5206 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
	GND	21	14	11	17	19	21	D9	25	-
	VCC	22	15	12	18	20	22	D10	26	-
37.	I/O	23	16	13	19	21	23	C10	27	255
38.	I/O	24	17	14	20	22	24	B10	28	258
39.	I/O	-	18	15	21	23	25	A9	29	261
40.	I/O	-	-	-	22	24	26	A10	30	267
41.	I/O	-	-	-	-	-	27	A11	31	270
42.	I/O	-	-	-	-	-	28	C11	32	273
43.	I/O	25	19	16	23	25	29	B11	33	279
44.	I/O	26	20	17	24	26	30	A12	34	282
45.	I/O	-	-	-	25	27	31	B12	35	285
46.	I/O	-	-	-	26	28	32	A13	36	291
	GND	-	-	-	27	29	33	C12	37	-
	-	-	-	-	-	-	-	-	38*	-
	-	-	-	-	-	-	-	-	39*	-
47.	I/O	-	-	-	-	30	34	A15	40	294
48.	I/O	-	-	-	-	31	35	C13	41	297
49.	I/O	27	21	18	28	32	36	B14	42	303
50.	I/O	-	22	19	29	33	37	A16	43	306
51.	I/O	-	-	-	30	34	38	B15	44	309
52.	I/O	-	-	-	31	35	39	C14	45	315
53.	I/O	28	23	20	32	36	40	A17	46	318
54.	I/O	29	24	21	33	37	41	B16	47	321
55.	M1 (I/O)	30	25	22	34	38	42	C15	48	330
	GND	31	26	23	35	39	43	D15	49	-
56.	M0 (I/O)	32	27	24	36	40	44	A18	50	333
	-	-	-	-	-	-	-	-	51*	-
	-	-	-	-	-	-	-	-	52*	-
	-	-	-	-	-	-	-	-	53*	-
	-	-	-	-	-	-	-	-	54*	-
	VCC	33	28	25	37	41	45	D16	55	-
57.	M2 (I/O)	34	29	26	38	42	46	C16	56	336
58.	GCK2 (I/O)	35	30	27	39	43	47	B17	57	339
59.	I/O (HDC)	36	31	28	40	44	48	E16	58	348
60.	I/O	-	-	-	41	45	49	C17	59	351
61.	I/O	-	-	-	42	46	50	D17	60	354
62.	I/O	-	32	29	43	47	51	B18	61	360
63.	I/O (LDC)	37	33	30	44	48	52	E17	62	363
64.	I/O	-	-	-	-	49	53	F16	63	372
65.	I/O	-	-	-	-	50	54	C18	64	375
	-	-	-	-	-	-	-	-	65*	-
	-	-	-	-	-	-	-	-	66*	-
	GND	-	-	-	45	51	55	G16	67	-
66.	I/O	-	-	-	46	52	56	E18	68	378
67.	I/O	-	-	-	47	53	57	F18	69	384
68.	I/O	38	34	31	48	54	58	G17	70	387
69.	I/O	39	35	32	49	55	59	G18	71	390
70.	I/O	-	-	-	-	-	60	H16	72	396
71.	I/O	-	-	-	-	-	61	H17	73	399
72.	I/O	-	36	33	50	56	62	H18	74	402
73.	I/O	-	37	34	51	57	63	J18	75	408

Pin Locations for XC5206 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
74.	I/O	40	38	35	52	58	64	J17	76	411
75.	I/O ($\overline{ERR}$, $\overline{INIT}$)	41	39	36	53	59	65	J16	77	414
	VCC	42	40	37	54	60	66	J15	78	-
	GND	43	41	38	55	61	67	K15	79	-
76.	I/O	44	42	39	56	62	68	K16	80	420
77.	I/O	45	43	40	57	63	69	K17	81	423
78.	I/O	-	44	41	58	64	70	K18	82	426
79.	I/O	-	45	42	59	65	71	L18	83	432
80.	I/O	-	-	-	-	-	72	L17	84	435
81.	I/O	-	-	-	-	-	73	L16	85	438
82.	I/O	46	46	43	60	66	74	M18	86	444
83.	I/O	47	47	44	61	67	75	M17	87	447
84.	I/O	-	-	-	62	68	76	N18	88	450
85.	I/O	-	-	-	63	69	77	P18	89	456
	GND	-	-	-	64	70	78	M16	90	-
	-	-	-	-	-	-	-	-	91*	-
	-	-	-	-	-	-	-	-	92*	-
86.	I/O	-	-	-	-	71	79	T18	93	459
87.	I/O	-	-	-	-	72	80	P17	94	468
88.	I/O	48	48	45	65	73	81	N16	95	471
89.	I/O	49	49	46	66	74	82	T17	96	480
90.	I/O	-	-	-	67	75	83	R17	97	483
91.	I/O	-	-	-	68	76	84	P16	98	486
92.	I/O	50	50	47	69	77	85	U18	99	492
93.	I/O	51	51	48	70	78	86	T16	100	495
	GND	52	52	49	71	79	87	R16	101	-
	-	-	-	-	-	-	-	-	102*	-
	DONE	53	53	50	72	80	88	U17	103	-
	-	-	-	-	-	-	-	-	104*	-
	-	-	-	-	-	-	-	-	105*	-
	VCC	54	54	51	73	81	89	R15	106	-
	-	-	-	-	-	-	-	-	107*	-
	PROG	55	55	52	74	82	90	V18	108	-
94.	I/O (D7)	56	56	53	75	83	91	T15	109	504
95.	GCK3 (I/O)	57	57	54	76	84	92	U16	110	507
96.	I/O	-	-	-	77	85	93	T14	111	516
97.	I/O	-	-	-	78	86	94	U15	112	519
98.	I/O (D6)	58	58	55	79	87	95	V17	113	522
99.	I/O	-	59	56	80	88	96	V16	114	528
100.	I/O	-	-	-	-	89	97	T13	115	531
101.	I/O	-	-	-	-	90	98	U14	116	534
	-	-	-	-	-	-	-	-	117*	-
	-	-	-	-	-	-	-	-	118*	-
	GND	-	-	-	81	91	99	T12	119	-
102.	I/O	-	-	-	82	92	100	U13	120	540
103.	I/O	-	-	-	83	93	101	V13	121	543
104.	I/O (D5)	59	60	57	84	94	102	U12	122	552
105.	I/O ($\overline{CS0}$)	60	61	58	85	95	103	V12	123	555
106.	I/O	-	-	-	-	-	104	T11	124	558
107.	I/O	-	-	-	-	-	105	U11	125	564
108.	I/O	-	62	59	86	96	106	V11	126	567

Pin Locations for XC5206 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
109.	I/O	-	63	60	87	97	107	V10	127	570
110.	I/O (D4)	61	64	61	88	98	108	U10	128	576
111.	I/O	62	65	62	89	99	109	T10	129	579
	VCC	63	66	63	90	100	110	R10	130	-
	GND	64	67	64	91	101	111	R9	131	-
112.	I/O (D3)	65	68	65	92	102	112	T9	132	588
113.	I/O ($\overline{RS}$)	66	69	66	93	103	113	U9	133	591
114.	I/O	-	70	67	94	104	114	V9	134	600
115.	I/O	-	-	-	95	105	115	V8	135	603
116.	I/O	-	-	-	-	-	116	U8	136	612
117.	I/O	-	-	-	-	-	117	T8	137	615
118.	I/O (D2)	67	71	68	96	106	118	V7	138	618
119.	I/O	68	72	69	97	107	119	U7	139	624
120.	I/O	-	-	-	98	108	120	V6	140	627
121.	I/O	-	-	-	99	109	121	U6	141	630
	GND	-	-	-	100	110	122	T7	142	-
	-	-	-	-	-	-	-	-	143*	-
	-	-	-	-	-	-	-	-	144*	-
122.	I/O	-	-	-	-	111	123	U5	145	636
123.	I/O	-	-	-	-	112	124	T6	146	639
124.	I/O (D1)	69	73	70	101	113	125	V3	147	642
125.	I/O ($\overline{RCLK}$-$\overline{BUSY}$/RDY)	70	74	71	102	114	126	V2	148	648
126.	I/O	-	-	-	103	115	127	U4	149	651
127.	I/O	-	-	-	104	116	128	T5	150	654
128.	I/O (D0, DIN)	71	75	72	105	117	129	U3	151	660
129.	I/O (DOUT)	72	76	73	106	118	130	T4	152	663
	CCLK	73	77	74	107	119	131	V1	153	-
	VCC	74	78	75	108	120	132	R4	154	-
	-	-	-	-	-	-	-	-	155*	-
	-	-	-	-	-	-	-	-	156*	-
	-	-	-	-	-	-	-	-	157*	-
	-	-	-	-	-	-	-	-	158*	-
130.	I/O (TDO)	75	79	76	109	121	133	U2	159	-
	GND	76	80	77	110	122	134	R3	160	-
131.	I/O (A0, $\overline{WS}$)	77	81	78	111	123	135	T3	161	9
132.	GCK4 (A1, I/O)	78	82	79	112	124	136	U1	162	15
133.	I/O	-	-	-	113	125	137	P3	163	18
134.	I/O	-	-	-	114	126	138	R2	164	21
135.	I/O (A2, CS1)	79	83	80	115	127	139	T2	165	27
136.	I/O (A3)	80	84	81	116	128	140	N3	166	30
137.	I/O	-	-	-	117	129	141	P2	167	33
138.	I/O	-	-	-	-	130	142	T1	168	42
	-	-	-	-	-	-	-	-	169*	-
	-	-	-	-	-	-	-	-	170*	-
	GND	-	-	-	118	131	143	M3	171	-
139.	I/O	-	-	-	119	132	144	P1	172	45
140.	I/O	-	-	-	120	133	145	N1	173	51
141.	I/O (A4)	81	85	82	121	134	146	M2	174	54
142.	I/O (A5)	82	86	83	122	135	147	M1	175	57
143.	I/O	-	-	-	-	-	148	L3	176	63

Pin Locations for XC5206 Devices

Pin	Description †	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
144.	I/O	-	-	-	-	136	149	L2	177	66
145.	I/O	-	87	84	123	137	150	L1	178	69
146.	I/O	-	88	85	124	138	151	K1	179	75
147.	I/O (A6)	83	89	86	125	139	152	K2	180	78
148.	I/O (A7)	84	90	87	126	140	153	K3	181	81
	GND	1	91	88	127	141	154	K4	182	-

Notes: * Indicates unconnected package pins.
† leading numbers refer to bonded pad, shown in Figure 22 or Figure 23.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD

Pin Locations for XC5210 Devices

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
	VCC	2	128	142	155	183	J4	VCC**	212	-
1.	I/O (A8)	3	129	143	156	184	J3	E8	213	111
2.	I/O (A9)	4	130	144	157	185	J2	B7	214	114
3.	I/O	-	131	145	158	186	J1	A7	215	117
4.	I/O	-	132	146	159	187	H1	C7	216	123
5.	I/O	-	-	-	160	188	H2	D7	217	126
6.	I/O	-	-	-	161	189	H3	E7	218	129
	-	-	-	-	-	-	-	-	219*	-
7.	I/O (A10)	5	133	147	162	190	G1	A6	220	135
8.	I/O (A11)	6	134	148	163	191	G2	B6	221	138
	VCC	-	-	-	-	-	-	VCC**	222	-
9.	I/O	-	-	-	-	-	H4	C6	223	141
10.	I/O	-	-	-	-	-	G4	F7	224	150
11.	I/O	-	135	149	164	192	F1	A5	225	153
12.	I/O	-	136	150	165	193	E1	B5	226	162
	GND	-	137	151	166	194	G3	GND**	227	-
13.	I/O	-	-	-	-	195	F2	D6	228	165
14.	I/O	-	-	-	167	196	D1	C5	229	171
15.	I/O	-	-	152	168	197	C1	A4	230	174
16.	I/O	-	-	153	169	198	E2	E6	231	177
17.	I/O (A12)	7	138	154	170	199	F3	B4	232	183
18.	I/O (A13)	8	139	155	171	200	D2	D5	233	186
19.	I/O	-	-	-	-	-	F4	A3	234	189
20.	I/O	-	-	-	-	-	E4	C4	235	195
21.	I/O	-	140	156	172	201	B1	B3	236	198
22.	I/O	-	141	157	173	202	E3	F6	237	201
23.	I/O (A14)	9	142	158	174	203	C2	A2	238	210
24.	I/O (A15)	10	143	159	175	204	B2	C3	239	213
	VCC	11	144	160	176	205	D3	VCC**	240	-
	-	-	-	-	-	206*	-	-	-	-
	-	-	-	-	-	207*	-	-	-	-
	-	-	-	-	-	208*	-	-	-	-
	-	-	-	-	-	1*	-	-	-	-
	GND	12	1	1	1	2	D4	GND**	1	-
	-	-	-	-	-	3*	-	-	-	-
25.	GCK1 (A16, I/O)	13	2	2	2	4	C3	D4	2	222
26.	I/O (A17)	14	3	3	3	5	C4	B1	3	225
27.	I/O	-	4	4	4	6	B3	C2	4	231
28.	I/O	-	5	5	5	7	C5	E5	5	234
29.	I/O (TDI)	15	6	6	6	8	A2	D3	6	237
30.	I/O (TCK)	16	7	7	7	9	B4	C1	7	243
31.	I/O	-	-	8	8	10	C6	D2	8	246
32.	I/O	-	-	9	9	11	A3	G6	9	249
33.	I/O	-	-	-	-	12	B5	E4	10	255
34.	I/O	-	-	-	-	13	B6	D1	11	258
35.	I/O	-	-	-	-	-	D5	E3	12	261
36.	I/O	-	-	-	-	-	D6	E2	13	267
	GND	-	8	10	10	14	C7	GND**	14	-
37.	I/O	-	9	11	11	15	A4	F5	15	270

Pin Locations for XC5210 Devices

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
38.	I/O	-	10	12	12	16	A5	E1	16	273
39.	I/O (TMS)	17	11	13	13	17	B7	F4	17	279
40.	I/O	18	12	14	14	18	A6	F3	18	282
	VCC	-	-	-	-	-	-	VCC**	19	-
41.	I/O	-	-	-	-	-	D7	F2	20	285
42.	I/O	-	-	-	-	-	D8	F1	21	291
	-	-	-	-	-	-	-	-	22*	-
43.	I/O	-	-	-	15	19	C8	G4	23	294
44.	I/O	-	-	-	16	20	A7	G3	24	297
45.	I/O	-	13	15	17	21	B8	G2	25	306
46.	I/O	-	14	16	18	22	A8	G1	26	309
47.	I/O	19	15	17	19	23	B9	G5	27	318
48.	I/O	20	16	18	20	24	C9	H3	28	321
	GND	21	17	19	21	25	D9	GND**	29	-
	VCC	22	18	20	22	26	D10	VCC**	30	-
49.	I/O	23	19	21	23	27	C10	H4	31	327
50.	I/O	24	20	22	24	28	B10	H5	32	330
51.	I/O	-	21	23	25	29	A9	J2	33	333
52.	I/O	-	22	24	26	30	A10	J1	34	339
53.	I/O	-	-	-	27	31	A11	J3	35	342
54.	I/O	-	-	-	28	32	C11	J4	36	345
	-	-	-	-	-	-	-	-	37*	-
55.	I/O	-	-	-	-	-	D11	J5	38	351
56.	I/O	-	-	-	-	-	D12	K1	39	354
	VCC	-	-	-	-	-	-	VCC**	40	-
57.	I/O	25	23	25	29	33	B11	K2	41	357
58.	I/O	26	24	26	30	34	A12	K3	42	363
59.	I/O	-	25	27	31	35	B12	J6	43	366
60.	I/O	-	26	28	32	36	A13	L1	44	369
	GND	-	27	29	33	37	C12	GND**	45	-
61.	I/O	-	-	-	-	-	D13	L2	46	375
62.	I/O	-	-	-	-	-	D14	K4	47	378
63.	I/O	-	-	-	-	38	B13	L3	48	381
64.	I/O	-	-	-	-	39	A14	M1	49	387
65.	I/O	-	-	30	34	40	A15	K5	50	390
66.	I/O	-	-	31	35	41	C13	M2	51	393
67.	I/O	27	28	32	36	42	B14	L4	52	399
68.	I/O	-	29	33	37	43	A16	N1	53	402
69.	I/O	-	30	34	38	44	B15	M3	54	405
70.	I/O	-	31	35	39	45	C14	N2	55	411
71.	I/O	28	32	36	40	46	A17	K6	56	414
72.	I/O	29	33	37	41	47	B16	P1	57	417
73.	M1 (I/O)	30	34	38	42	48	C15	N3	58	426
	GND	31	35	39	43	49	D15	GND**	59	-
74.	M0 (I/O)	32	36	40	44	50	A18	P2	60	429
	-	-	-	-	-	51*	-	-	-	-
	-	-	-	-	-	52*	-	-	-	-
	-	-	-	-	-	53*	-	-	-	-
	-	-	-	-	-	54*	-	-	-	-
	VCC	33	37	41	45	55	D16	VCC**	61	-

Pin Locations for XC5210 Devices

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
75.	M2 (I/O)	34	38	42	46	56	C16	M4	62	432
76.	GCK2 (I/O)	35	39	43	47	57	B17	R2	63	435
77.	I/O (HDC)	36	40	44	48	58	E16	P3	64	444
78.	I/O	-	41	45	49	59	C17	L5	65	447
79.	I/O	-	42	46	50	60	D17	N4	66	450
80.	I/O	-	43	47	51	61	B18	R3	67	456
81.	I/O (LDC)	37	44	48	52	62	E17	P4	68	459
82.	I/O	-	-	49	53	63	F16	K7	69	462
83.	I/O	-	-	50	54	64	C18	M5	70	468
84.	I/O	-	-	-	-	65	D18	R4	71	471
85.	I/O	-	-	-	-	66	F17	N5	72	474
86.	I/O	-	-	-	-	-	E15	P5	73	480
87.	I/O	-	-	-	-	-	F15	L6	74	483
	GND	-	45	51	55	67	G16	GND**	75	-
88.	I/O	-	46	52	56	68	E18	R5	76	486
89.	I/O	-	47	53	57	69	F18	M6	77	492
90.	I/O	38	48	54	58	70	G17	N6	78	495
91.	I/O	39	49	55	59	71	G18	P6	79	504
	VCC	-	-	-	-	-	-	VCC**	80	-
92.	I/O	-	-	-	60	72	H16	R6	81	507
93.	I/O	-	-	-	61	73	H17	M7	82	510
	-	-	-	-	-	-	-	-	83*	-
94.	I/O	-	-	-	-	-	G15	N7	84	516
95.	I/O	-	-	-	-	-	H15	P7	85	519
96.	I/O	-	50	56	62	74	H18	R7	86	522
97.	I/O	-	51	57	63	75	J18	L7	87	528
98.	I/O	40	52	58	64	76	J17	N8	88	531
99.	I/O ($\overline{ERR}$, $\overline{INIT}$)	41	53	59	65	77	J16	P8	89	534
	VCC	42	54	60	66	78	J15	VCC**	90	-
	GND	43	55	61	67	79	K15	GND**	91	-
100.	I/O	44	56	62	68	80	K16	L8	92	540
101.	I/O	45	57	63	69	81	K17	P9	93	543
102.	I/O	-	58	64	70	82	K18	R9	94	546
103.	I/O	-	59	65	71	83	L18	N9	95	552
104.	I/O	-	-	-	72	84	L17	M9	96	555
105.	I/O	-	-	-	73	85	L16	L9	97	558
	-	-	-	-	-	-	-	-	98*	-
106.	I/O	-	-	-	-	-	L15	R10	99	564
107.	I/O	-	-	-	-	-	M15	P10	100	567
	VCC	-	-	-	-	-	-	VCC**	101	-
108.	I/O	46	60	66	74	86	M18	N10	102	570
109.	I/O	47	61	67	75	87	M17	K9	103	576
110.	I/O	-	62	68	76	88	N18	R11	104	579
111.	I/O	-	63	69	77	89	P18	P11	105	588
	GND	-	64	70	78	90	M16	GND**	106	-
112.	I/O	-	-	-	-	-	N15	M10	107	591
113.	I/O	-	-	-	-	-	P15	N11	108	600
114.	I/O	-	-	-	-	91	N17	R12	109	603
115.	I/O	-	-	-	-	92	R18	L10	110	606
116.	I/O	-	-	71	79	93	T18	P12	111	612

Pin Locations for XC5210 Devices

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
117.	I/O	-	-	72	80	94	P17	M11	112	615
118.	I/O	48	65	73	81	95	N16	R13	113	618
119.	I/O	49	66	74	82	96	T17	N12	114	624
120.	I/O	-	67	75	83	97	R17	P13	115	627
121.	I/O	-	68	76	84	98	P16	K10	116	630
122.	I/O	50	69	77	85	99	U18	R14	117	636
123.	I/O	51	70	78	86	100	T16	N13	118	639
	GND	52	71	79	87	101	R16	GND**	119	-
	-	-	-	-	-	102*	-	-	-	-
	DONE	53	72	80	88	103	U17	P14	120	-
	-	-	-	-	-	104*	-	-	-	-
	-	-	-	-	-	105*	-	-	-	-
	VCC	54	73	81	89	106	R15	VCC**	121	-
	-	-	-	-	-	107*	-	-	-	-
	PROG	55	74	82	90	108	V18	M12	122	-
124.	I/O (D7)	56	75	83	91	109	T15	P15	123	648
125.	GCK3 (I/O)	57	76	84	92	110	U16	N14	124	651
126.	I/O	-	77	85	93	111	T14	L11	125	660
127.	I/O	-	78	86	94	112	U15	M13	126	663
128.	I/O	-	-	-	-	-	R14	N15	127	666
129.	I/O	-	-	-	-	-	R13	M14	128	672
130.	I/O (D6)	58	79	87	95	113	V17	J10	129	675
131.	I/O	-	80	88	96	114	V16	L12	130	678
132.	I/O	-	-	89	97	115	T13	M15	131	684
133.	I/O	-	-	90	98	116	U14	L13	132	687
134.	I/O	-	-	-	-	117	V15	L14	133	690
135.	I/O	-	-	-	-	118	V14	K11	134	696
	GND	-	81	91	99	119	T12	GND**	135	-
136.	I/O	-	-	-	-	-	R12	L15	136	699
137.	I/O	-	-	-	-	-	R11	K12	137	708
138.	I/O	-	82	92	100	120	U13	K13	138	711
139.	I/O	-	83	93	101	121	V13	K14	139	714
	VCC	-	-	-	-	-	-	VCC**	140	-
140.	I/O (D5)	59	84	94	102	122	U12	K15	141	720
141.	I/O ($\overline{CS0}$)	60	85	95	103	123	V12	J12	142	723
	-	-	-	-	-	-	-	-	143*	-
142.	I/O	-	-	-	104	124	T11	J13	144	726
143.	I/O	-	-	-	105	125	U11	J14	145	732
144.	I/O	-	86	96	106	126	V11	J15	146	735
145.	I/O	-	87	97	107	127	V10	J11	147	738
146.	I/O (D4)	61	88	98	108	128	U10	H13	148	744
147.	I/O	62	89	99	109	129	T10	H14	149	747
	VCC	63	90	100	110	130	R10	VCC**	150	-
	GND	64	91	101	111	131	R9	GND**	151	-
148.	I/O (D3)	65	92	102	112	132	T9	H12	152	756
149.	I/O ($\overline{RS}$)	66	93	103	113	133	U9	H11	153	759
150.	I/O	-	94	104	114	134	V9	G14	154	768
151.	I/O	-	95	105	115	135	V8	G15	155	771
152.	I/O	-	-	-	116	136	U8	G13	156	780
153.	I/O	-	-	-	117	137	T8	G12	157	783

Pin Locations for XC5210 Devices

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
	-	-	-	-	-	-	-	-	158*	-
154.	I/O (D2)	67	96	106	118	138	V7	G11	159	786
155.	I/O	68	97	107	119	139	U7	F15	160	792
	VCC	-	-	-	-	-	-	VCC**	161	-
156.	I/O	-	98	108	120	140	V6	F14	162	795
157.	I/O	-	99	109	121	141	U6	F13	163	798
158.	I/O	-	-	-	-	-	R8	G10	164	804
159.	I/O	-	-	-	-	-	R7	E15	165	807
	GND	-	100	110	122	142	T7	GND**	166	-
160.	I/O	-	-	-	-	-	R6	E14	167	810
161.	I/O	-	-	-	-	-	R5	F12	168	816
162.	I/O	-	-	-	-	143	V5	E13	169	819
163.	I/O	-	-	-	-	144	V4	D15	170	822
164.	I/O	-	-	111	123	145	U5	F11	171	828
165.	I/O	-	-	112	124	146	T6	D14	172	831
166.	I/O (D1)	69	101	113	125	147	V3	E12	173	834
167.	I/O ($\overline{\text{RCLK}}$-BUSY/RDY)	70	102	114	126	148	V2	C15	174	840
168.	I/O	-	103	115	127	149	U4	D13	175	843
169.	I/O	-	104	116	128	150	T5	C14	176	846
170.	I/O (D0, DIN)	71	105	117	129	151	U3	F10	177	855
171.	I/O (DOUT)	72	106	118	130	152	T4	B15	178	858
	CCLK	73	107	119	131	153	V1	C13	179	-
	VCC	74	108	120	132	154	R4	VCC**	180	-
	-	-	-	-	-	155*	-	-	-	-
	-	-	-	-	-	156*	-	-	-	-
	-	-	-	-	-	157*	-	-	-	-
	-	-	-	-	-	158*	-	-	-	-
172.	I/O (TDO)	75	109	121	133	159	U2	A15	181	-
	GND	76	110	122	134	160	R3	GND**	182	-
173.	I/O (A0, $\overline{\text{WS}}$)	77	111	123	135	161	T3	A14	183	9
174.	GCK4 (A1, I/O)	78	112	124	136	162	U1	B13	184	15
175.	I/O	-	113	125	137	163	P3	E11	185	18
176.	I/O	-	114	126	138	164	R2	C12	186	21
177.	I/O (CS1, A2)	79	115	127	139	165	T2	A13	187	27
178.	I/O (A3)	80	116	128	140	166	N3	B12	188	30
179.	I/O	-	-	-	-	-	P4	F9	189	33
180.	I/O	-	-	-	-	-	N4	D11	190	39
181.	I/O	-	117	129	141	167	P2	A12	191	42
182.	I/O	-	-	130	142	168	T1	C11	192	45
183.	I/O	-	-	-	-	169	R1	B11	193	51
184.	I/O	-	-	-	-	170	N2	E10	194	54
	-	-	-	-	-	-	-	GND**	195*	-
	GND	-	118	131	143	171	M3	-	196	-
185.	I/O	-	119	132	144	172	P1	A11	197	57
186.	I/O	-	120	133	145	173	N1	D10	198	66
187.	I/O	-	-	-	-	-	M4	C10	199	69
188.	I/O	-	-	-	-	-	L4	B10	200	75
	VCC	-	-	-	-	-	-	VCC**	201	-
189.	I/O (A4)	81	121	134	146	174	M2	A10	202	78
190.	I/O (A5)	82	122	135	147	175	M1	D9	203	81

Pin Locations for XC5210 Devices

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
	-	-	-	-	-	-	-	-	204*	-
191.	I/O	-	-	-	148	176	L3	C9	205	87
192.	I/O	-	-	136	149	177	L2	B9	206	90
193.	I/O	-	123	137	150	178	L1	A9	207	93
194.	I/O	-	124	138	151	179	K1	E9	208	99
195.	I/O (A6)	83	125	139	152	180	K2	C8	209	102
196.	I/O (A7)	84	126	140	153	181	K3	B8	210	105
	GND	1	127	141	154	182	K4	GND**	211	-

Notes: * Indicates unconnected package pins.

† leading numbers refer to bonded pad, shown in Figure 24 or Figure 25.

** Pins labeled VCC** are internally bonded to a VCC plane within the BG225 package. The external pins are: B2, D8, H15, R8, B14, R1, H1, and R15.

Pins labeled GND** are internally bonded to a ground plane within the BG225 package. The external pins are: A1, D12, G7, G9, H9, H8, H10, J8, K8, A8, F8, G8, H2, H7, H9, J7, J9, M8.

Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1 = TDO.O

Boundary Scan Bit 1056 = BSCAN.UPD

Pin Locations for XC5215 Devices

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
	VCC	142	183	212	K1	38	VCC**	VCC**	-
1.	I/O (A8)	143	184	213	K2	37	E8	D14	138
2.	I/O (A9)	144	185	214	K3	36	B7	C14	141
3.	I/O	145	186	215	K5	35	A7	A15	147
4.	I/O	146	187	216	K4	34	C7	B15	150
5.	I/O	-	188	217	J1	33	D7	C15	153
6.	I/O	-	189	218	J2	32	E7	D15	159
	-	-	-	219*	-	-	-	-	-
7.	I/O (A10)	147	190	220	H1	31	A6	A16	162
8.	I/O (A11)	148	191	221	J3	30	B6	B16	165
	-	-	-	-	-	29*	-	-	-
	-	-	-	-	-	28*	-	-	-
9.	I/O	-	-	-	H2	27	-	C17	171
10.	I/O	-	-	-	G1	26	-	B18	174
	VCC	-	-	222	E1	25	VCC**	VCC**	-
	-	-	-	-	-	24*	-	-	-
11.	I/O	-	-	223	H3	23	C6	C18	177
12.	I/O	-	-	224	G2	22	F7	D17	183
13.	I/O	149	192	225	H4	21	A5	A20	186
14.	I/O	150	193	226	F2	20	B5	B19	189
	GND	151	194	227	F1	19	GND**	GND**	-
15.	I/O	-	-	-	H5	18	-	C19	195
16.	I/O	-	-	-	G3	17	-	D18	198
17.	I/O	-	195	228	D1	16	D6	A21	201
18.	I/O	-	196	229	G4	15	C5	B20	207
19.	I/O	152	197	230	E2	14	A4	C20	210
20.	I/O	153	198	231	F3	13	E6	B21	213
21.	I/O (A12)	154	199	232	G5	12	B4	B22	219
	-	-	-	-	-	11*	-	-	-
22.	I/O (A13)	155	200	233	C1	10	D5	C21	222
23.	I/O	-	-	-	F4	9	-	D20	225
24.	I/O	-	-	-	E3	8	-	A23	234
25.	I/O	-	-	234	D2	7	A3	D21	237
26.	I/O	-	-	235	C2	6	C4	C22	243
27.	I/O	156	201	236	F5	5	B3	B24	246
28.	I/O	157	202	237	E4	4	F6	C23	249
29.	I/O (A14)	158	203	238	D3	3	A2	D22	258
30.	I/O (A15)	159	204	239	C3	2	C3	C24	261
	VCC	160	205	240	A2	1	VCC**	VCC**	-
	-	-	206*	-	-	-	-	-	-
	-	-	207*	-	-	-	-	-	-
	-	-	208*	-	-	-	-	-	-
	-	-	1*	-	-	-	-	-	-
	GND	1	2	1	B1	304	GND**	GND**	-
	-	-	3*	-	-	-	-	-	-
31.	GCK1 (A16, I/O)	2	4	2	D4	303	D4	D23	270
32.	I/O (A17)	3	5	3	B2	302	B1	C25	273
33.	I/O	4	6	4	B3	301	C2	D24	279
34.	I/O	5	7	5	E6	300	E5	E23	282
35.	I/O (TDI)	6	8	6	D5	299	D3	C26	285

Pin Locations for XC5215 Devices

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
36.	I/O (TCK)	7	9	7	C4	298	C1	E24	294
37.	I/O	-	-	-	A3	297	-	F24	297
38.	I/O	-	-	-	D6	296	-	E25	303
39.	I/O	8	10	8	E7	295	D2	D26	306
40.	I/O	9	11	9	B4	294	G6	G24	309
41.	I/O	-	12	10	C5	293	E4	F25	315
42.	I/O	-	13	11	A4	292	D1	F26	318
43.	I/O	-	-	12	D7	291	E3	H23	321
44.	I/O	-	-	13	C6	290	E2	H24	327
45.	I/O	-	-	-	E8	289	-	G25	330
46.	I/O	-	-	-	B5	288	-	G26	333
	GND	10	14	14	A5	287	GND**	GND**	-
47.	I/O	11	15	15	B6	286	F5	J23	339
48.	I/O	12	16	16	D8	285	E1	J24	342
49.	I/O (TMS)	13	17	17	C7	284	F4	H25	345
50.	I/O	14	18	18	B7	283	F3	K23	351
	VCC	-	-	19	A6	282	VCC**	VCC**	-
	-	-	-	-	-	281*	-	-	-
51.	I/O	-	-	20	C8	280	F2	L24	354
52.	I/O	-	-	21	E9	279	F1	K25	357
	-	-	-	22*	-	-	-	-	-
	-	-	-	-	-	278*	-	-	-
	-	-	-	-	-	277*	-	-	-
53.	I/O	-	-	-	B8	276	-	L25	363
54.	I/O	-	-	-	A8	275	-	L26	366
55.	I/O	-	19	23	C9	274	G4	M23	369
56.	I/O	-	20	24	B9	273	G3	M24	375
57.	I/O	15	21	25	E10	272	G2	M25	378
58.	I/O	16	22	26	A9	271	G1	M26	381
59.	I/O	17	23	27	D10	270	G5	N24	390
60.	I/O	18	24	28	C10	269	H3	N25	393
	GND	19	25	29	A10	268	GND**	GND**	-
	VCC	20	26	30	A11	267	VCC**	VCC**	-
61.	I/O	21	27	31	B10	266	H4	N26	399
62.	I/O	22	28	32	B11	265	H5	P25	402
63.	I/O	23	29	33	C11	264	J2	P23	405
64.	I/O	24	30	34	E11	263	J1	P24	411
65.	I/O	-	31	35	D11	262	J3	R26	414
66.	I/O	-	32	36	A12	261	J4	R25	417
67.	I/O	-	-	-	B12	260	-	R24	423
68.	I/O	-	-	-	A13	259	-	R23	426
	-	-	-	37*	-	-	-	-	-
	-	-	-	-	-	258*	-	-	-
	-	-	-	-	-	257*	-	-	-
69.	I/O	-	-	38	E12	256	J5	T26	429
70.	I/O	-	-	39	B13	255	K1	T25	435
	-	-	-	-	-	254*	-	-	-
	VCC	-	-	40	A16	253	VCC**	VCC**	-
71.	I/O	25	33	41	A14	252	K2	U24	438
72.	I/O	26	34	42	C13	251	K3	V25	441
73.	I/O	27	35	43	B14	250	J6	V24	447

Pin Locations for XC5215 Devices

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
74.	I/O	28	36	44	D13	249	L1	U23	450
	GND	29	37	45	A15	248	GND**	GND**	-
75.	I/O	-	-	-	B15	247	-	Y26	453
76.	I/O	-	-	-	E13	246	-	W25	459
77.	I/O	-	-	46	C14	245	L2	W24	462
78.	I/O	-	-	47	A17	244	K4	V23	465
79.	I/O	-	38	48	D14	243	L3	AA26	471
80.	I/O	-	39	49	B16	242	M1	Y25	474
81.	I/O	30	40	50	C15	241	K5	Y24	477
82.	I/O	31	41	51	E14	240	M2	AA25	483
83.	I/O	-	-	-	A18	239	-	AB25	486
84.	I/O	-	-	-	D15	238	-	AA24	489
85.	I/O	32	42	52	C16	237	L4	Y23	495
86.	I/O	33	43	53	B17	236	N1	AC26	498
87.	I/O	34	44	54	B18	235	M3	AA23	501
88.	I/O	35	45	55	E15	234	N2	AB24	507
89.	I/O	36	46	56	D16	233	K6	AD25	510
90.	I/O	37	47	57	C17	232	P1	AC24	513
91.	M1 (I/O)	38	48	58	A20	231	N3	AB23	522
	GND	39	49	59	A19	230	GND**	GND**	-
92.	M0 (I/O)	40	50	60	C18	229	P2	AD24	525
	-	-	51*	-	-	-	-	-	-
	-	-	52*	-	-	-	-	-	-
	-	-	53*	-	-	-	-	-	-
	-	-	54*	-	-	-	-	-	-
	VCC	41	55	61	B20	228	VCC**	VCC**	-
93.	M2 (I/O)	42	56	62	D17	227	M4	AC23	528
94.	GCK2 (I/O)	43	57	63	B19	226	R2	AE24	531
95.	I/O (HDC)	44	58	64	C19	225	P3	AD23	540
96.	I/O	45	59	65	F16	224	L5	AC22	543
97.	I/O	46	60	66	E17	223	N4	AF24	546
98.	I/O	47	61	67	D18	222	R3	AD22	552
99.	I/O (LDC)	48	62	68	C20	221	P4	AE23	555
100.	I/O	-	-	-	F17	220	-	AE22	558
101.	I/O	-	-	-	G16	219	-	AF23	564
102.	I/O	49	63	69	D19	218	K7	AD20	567
103.	I/O	50	64	70	E18	217	M5	AE21	570
104.	I/O	-	65	71	D20	216	R4	AF21	576
105.	I/O	-	66	72	G17	215	N5	AC19	579
106.	I/O	-	-	73	F18	214	P5	AD19	582
107.	I/O	-	-	74	H16	213	L6	AE20	588
108.	I/O	-	-	-	E19	212	-	AF20	591
109.	I/O	-	-	-	F19	211	-	AC18	594
	GND	51	67	75	E20	210	GND**	GND**	-
110.	I/O	52	68	76	H17	209	R5	AD18	600
111.	I/O	53	69	77	G18	208	M6	AE19	603
112.	I/O	54	70	78	G19	207	N6	AC17	606
113.	I/O	55	71	79	H18	206	P6	AD17	612
	-	-	-	-	-	205*	-	-	-
	VCC	-	-	80	F20	204	VCC**	VCC**	-
114.	I/O	-	72	81	J16	203	R6	AE17	615

Pin Locations for XC5215 Devices

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
115.	I/O	-	73	82	G20	202	M7	AE16	618
	-	-	-	83*	-	-	-	-	-
	-	-	-	-	-	201*	-	-	-
	-	-	-	-	-	200*	-	-	-
116.	I/O	-	-	-	H20	199	-	AF16	624
117.	I/O	-	-	-	J18	198	-	AC15	627
118.	I/O	-	-	84	J19	197	N7	AD15	630
119.	I/O	-	-	85	K16	196	P7	AE15	636
120.	I/O	56	74	86	J20	195	R7	AF15	639
121.	I/O	57	75	87	K17	194	L7	AD14	642
122.	I/O	58	76	88	K18	193	N8	AE14	648
123.	I/O ($\overline{ERR}$, $\overline{INIT}$)	59	77	89	K19	192	P8	AF14	651
	VCC	60	78	90	L20	191	VCC**	VCC**	-
	GND	61	79	91	K20	190	GND**	GND**	-
124.	I/O	62	80	92	L19	189	L8	AE13	660
125.	I/O	63	81	93	L18	188	P9	AC13	663
126.	I/O	64	82	94	L16	187	R9	AD13	672
127.	I/O	65	83	95	L17	186	N9	AF12	675
128.	I/O	-	84	96	M20	185	M9	AE12	678
129.	I/O	-	85	97	M19	184	L9	AD12	684
130.	I/O	-	-	-	N20	183	-	AC12	687
131.	I/O	-	-	-	M18	182	-	AF11	690
	-	-	-	98*	-	-	-	-	-
	-	-	-	-	-	181*	-	-	-
	-	-	-	-	-	180*	-	-	-
132.	I/O	-	-	99	N19	179	R10	AE11	696
133.	I/O	-	-	100	P20	178	P10	AD11	699
	VCC	-	-	101	T20	177	VCC**	VCC**	-
	-	-	-	-	-	176*	-	-	-
134.	I/O	66	86	102	N18	175	N10	AE9	702
135.	I/O	67	87	103	P19	174	K9	AD9	708
136.	I/O	68	88	104	N17	173	R11	AC10	711
137.	I/O	69	89	105	R19	172	P11	AF7	714
	GND	70	90	106	R20	171	GND**	GND**	-
138.	I/O	-	-	-	N16	170	-	AE8	720
139.	I/O	-	-	-	P18	169	-	AD8	723
140.	I/O	-	-	107	U20	168	M10	AC9	726
141.	I/O	-	-	108	P17	167	N11	AF6	732
142.	I/O	-	91	109	T19	166	R12	AE7	735
143.	I/O	-	92	110	R18	165	L10	AD7	738
144.	I/O	71	93	111	P16	164	P12	AE6	744
145.	I/O	72	94	112	V20	163	M11	AE5	747
146.	I/O	-	-	-	R17	162	-	AD6	750
147.	I/O	-	-	-	T18	161	-	AC7	756
148.	I/O	73	95	113	U19	160	R13	AF4	759
149.	I/O	74	96	114	V19	159	N12	AF3	768
150.	I/O	75	97	115	R16	158	P13	AD5	771
151.	I/O	76	98	116	T17	157	K10	AE3	774
152.	I/O	77	99	117	U18	156	R14	AD4	780
153.	I/O	78	100	118	X20	155	N13	AC5	783
	GND	79	101	119	W20	154	GND**	GND**	-

Pin Locations for XC5215 Devices

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
	-	-	102*	-	-	-	-	-	-
	DONE	80	103	120	V18	153	P14	AD3	-
	-	-	104*	-	-	-	-	-	-
	-	-	105*	-	-	-	-	-	-
	VCC	81	106	121	X19	152	VCC**	VCC**	-
	-	-	107*	-	-	-	-	-	-
	PROG	82	108	122	U17	151	M12	AC4	-
154.	I/O (D7)	83	109	123	W19	150	P15	AD2	792
155.	GCK3 (I/O)	84	110	124	W18	149	N14	AC3	795
156.	I/O	85	111	125	T15	148	L11	AB4	804
157.	I/O	86	112	126	U16	147	M13	AD1	807
158.	I/O	-	-	127	V17	146	N15	AA4	810
159.	I/O	-	-	128	X18	145	M14	AA3	816
160.	I/O	-	-	-	U15	144	-	AB2	819
161.	I/O	-	-	-	T14	143	-	AC1	828
162.	I/O (D6)	87	113	129	W17	142	J10	Y3	831
163.	I/O	88	114	130	V16	141	L12	AA2	834
164.	I/O	89	115	131	X17	140	M15	AA1	840
165.	I/O	90	116	132	U14	139	L13	W4	843
166.	I/O	-	117	133	V15	138	L14	W3	846
167.	I/O	-	118	134	T13	137	K11	Y2	852
168.	I/O	-	-	-	W16	136	-	Y1	855
169.	I/O	-	-	-	W15	135	-	V4	858
	GND	91	119	135	X16	134	GND**	GND**	-
170.	I/O	-	-	136	U13	133	L15	V3	864
171.	I/O	-	-	137	V14	132	K12	W2	867
172.	I/O	92	120	138	W14	131	K13	U4	870
173.	I/O	93	121	139	V13	130	K14	U3	876
	VCC	-	-	140	X15	129	VCC**	VCC**	-
	-	-	-	-	-	128*	-	-	-
174.	I/O (D5)	94	122	141	T12	127	K15	V2	879
175.	I/O ($\overline{CS0}$)	95	123	142	X14	126	J12	V1	882
	-	-	-	143*	-	-	-	-	-
	-	-	-	-	-	125*	-	-	-
	-	-	-	-	-	124*	-	-	-
176.	I/O	-	-	-	X13	123	-	T1	888
177.	I/O	-	-	-	V12	122	-	R4	891
178.	I/O	-	124	144	W12	121	J13	R3	894
179.	I/O	-	125	145	T11	120	J14	R2	900
180.	I/O	96	126	146	X12	119	J15	R1	903
181.	I/O	97	127	147	U11	118	J11	P3	906
182.	I/O (D4)	98	128	148	V11	117	H13	P2	912
183.	I/O	99	129	149	W11	116	H14	P1	915
	VCC	100	130	150	X10	115	VCC**	VCC**	-
	GND	101	131	151	X11	114	GND**	GND**	-
184.	I/O (D3)	102	132	152	W10	113	H12	N2	924
185.	I/O ($\overline{RS}$)	103	133	153	V10	112	H11	N4	927
186.	I/O	104	134	154	T10	111	G14	N3	936
187.	I/O	105	135	155	U10	110	G15	M1	939
188.	I/O	-	136	156	X9	109	G13	M2	942
189.	I/O	-	137	157	W9	108	G12	M3	948

Pin Locations for XC5215 Devices

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
190.	I/O	-	-	-	X8	107	-	M4	951
191.	I/O	-	-	-	V9	106	-	L1	954
	-	-	-	158*	-	-	-	-	-
	-	-	-	-	-	105*	-	-	-
	-	-	-	-	-	104*	-	-	-
192.	I/O (D2)	106	138	159	W8	103	G11	J1	960
193.	I/O	107	139	160	X7	102	F15	K3	963
	VCC	-	-	161	X5	101	VCC**	VCC**	
	-	-	-	-	-	100*	-	-	
194.	I/O	108	140	162	V8	99	F14	J2	966
195.	I/O	109	141	163	W7	98	F13	J3	972
196.	I/O	-	-	164	U8	97	G10	K4	975
197.	I/O	-	-	165	W6	96	E15	G1	978
	GND	110	142	166	X6	95	GND**	GND**	
198.	I/O	-	-	-	T8	94	-	H2	984
199.	I/O	-	-	-	V7	93	-	H3	987
200.	I/O	-	-	167	X4	92	E14	J4	990
201.	I/O	-	-	168	U7	91	F12	F1	996
202.	I/O	-	143	169	W5	90	E13	G2	999
203.	I/O	-	144	170	V6	89	D15	G3	1002
204.	I/O	111	145	171	T7	88	F11	F2	1008
205.	I/O	112	146	172	X3	87	D14	E2	1011
206.	I/O (D1)	113	147	173	U6	86	E12	F3	1014
207.	I/O ($\overline{\text{RCLK}}$-BUSY/RDY)	114	148	174	V5	85	C15	G4	1020
208.	I/O	-	-	-	W4	84	-	D2	1023
209.	I/O	-	-	-	W3	83	-	F4	1032
210.	I/O	115	149	175	T6	82	D13	E3	1035
211.	I/O	116	150	176	U5	81	C14	C2	1038
212.	I/O (D0, DIN)	117	151	177	V4	80	F10	D3	1044
213.	I/O (DOUT)	118	152	178	X1	79	B15	E4	1047
	CCLK	119	153	179	V3	78	C13	C3	-
	VCC	120	154	180	W1	77	VCC**	VCC**	-
	-	-	155*	-	-	-	-	-	-
	-	-	156*	-	-	-	-	-	-
	-	-	157*	-	-	-	-	-	-
	-	-	158*	-	-	-	-	-	-
214.	I/O (TDO)	121	159	181	U4	76	A15	D4	0
	GND	122	160	182	X2	75	GND**	GND**	-
215.	I/O (A0, $\overline{\text{WS}}$)	123	161	183	W2	74	A14	B3	9
216.	GCK4 (A1, I/O)	124	162	184	V2	73	B13	C4	15
217.	I/O	125	163	185	R5	72	E11	D5	18
218.	I/O	126	164	186	T4	71	C12	A3	21
219.	I/O (A2, CS1)	127	165	187	U3	70	A13	D6	27
220.	I/O (A3)	128	166	188	V1	69	B12	C6	30
221.	I/O	-	-	-	R4	68	-	B5	33
222.	I/O	-	-	-	P5	67	-	A4	39
223.	I/O	-	-	189	U2	66	F9	C7	42
224.	I/O	-	-	190	T3	65	D11	B6	45
225.	I/O	129	167	191	U1	64	A12	A6	51
226.	I/O	130	168	192	P4	63	C11	D8	54
227.	I/O	-	169	193	R3	62	B11	B7	57

Pin Locations for XC5215 Devices

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
228.	I/O	-	170	194	N5	61	E10	A7	63
229.	I/O	-	-	195	T2	60	-	D9	66
230.	I/O	-	-	-	R2	59	-	C9	69
	GND	131	171	196	T1	58	GND**	GND**	-
231.	I/O	132	172	197	N4	57	A11	B8	75
232.	I/O	133	173	198	P3	56	D10	D10	78
233.	I/O	-	-	199	P2	55	C10	C10	81
234.	I/O	-	-	200	N3	54	B10	B9	87
	-	-	-	-	-	53*	-	-	-
	VCC	-	-	201	R1	52	VCC**	VCC**	-
235.	I/O	-	-	-	M5	51	-	B11	90
236.	I/O	-	-	-	P1	50	-	A11	93
	-	-	-	-	-	49*	-	-	-
	-	-	-	-	-	48*	-	-	-
237.	I/O (A4)	134	174	202	N1	47	A10	D12	99
238.	I/O (A5)	135	175	203	M3	46	D9	C12	102
	-	-	-	204*	-	-	-	-	-
239.	I/O	-	176	205	M2	45	C9	B12	105
240.	I/O	136	177	206	L5	44	B9	A12	111
241.	I/O	137	178	207	M1	43	A9	C13	114
242.	I/O	138	179	208	L4	42	E9	B13	117
243.	I/O (A6)	139	180	209	L3	41	C8	A13	126
244.	I/O (A7)	140	181	210	L2	40	B8	B14	129
	GND	141	182	211	L1	39	GND**	GND**	-

Notes: * Indicates unconnected package pins.

† leading numbers refer to bonded pad, shown in Figure 26, Figure 27 or Figure 28.

** Pins labeled VCC** are internally bonded to a VCC plane within the BG225 and BG352 packages. The external pins for the BG225 are: B2, D8, H15, R8, B14, E1, and R15. The external pins for the BG352 are: A10, A17, B2, B25, D13, D19, D7, G23, H4, K1, K26, N23, P4, U1, U26, W23, Y4, AC14, AC20, AC8, AE2, AE25, AF10, and AF17.
Pins labeled GND** are internally bonded to a ground plane within the BG225 and BG352 packages. The external pins for the BG225 are: A1, D12, G7, G9, H9, H8, H10, J8, K8, A8, F8, G8, H2, H7, H9, J7, J9, M8. The external pins for the BG352 are: A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF13, AF19, AF2, AF22, AF25, AF26, AF5, AF8.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD

Product Availability

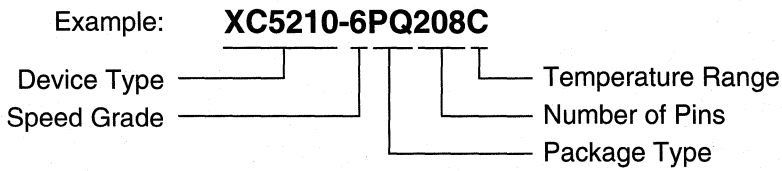
PINS		84	100	100	144	156	160	176	191	208	208	223	225	240	240	299	304	352
TYPE		Plast. PLCC	Plast. PQFP	Plast. VQFP	Plast. TQFP	Ceram. PGA	Plast. PQFP	Plast. TQFP	Ceram. PGA	High-Perf. QFP	Plast. PQFP	Ceram. PGA	Plast. BGA	High-Perf. QFP	Plast. PQFP	Ceram. PGA	High-Perf. QFP	Plast. BGA
CODE		PC84	PQ100	VQ100	TQ144	PG156	PQ160	TQ176	PG191	HQ208	PQ208	PG223	BG225	HQ240	PQ240	PG299	HQ304	BG352
XC5202	-6	CI	CI	CI	CI	CI												
	-5	CI	CI	CI	CI	CI												
	-4	(CI)	(CI)	(CI)	(CI)	(CI)												
	-3	(CI)	(CI)	(CI)	(CI)	(CI)												
XC5204	-6	CI	CI	CI	CI	CI	CI											
	-5	CI	CI	CI	CI	CI	CI											
	-4	(CI)	(CI)	(CI)	(CI)	(CI)	(CI)											
	-3	(CI)	(CI)	(CI)	(CI)	(CI)	(CI)											
XC5206	-6	CI	CI	CI	CI		CI	CI	CI		CI							
	-5	CI	CI	CI	CI		CI	CI	CI		CI							
	-4	(CI)	(CI)	(CI)	(CI)		(CI)	(CI)	(CI)		(CI)							
	-3	(CI)	(CI)	(CI)	(CI)		(CI)	(CI)	(CI)		(CI)							
XC5210	-6	CI			CI		CI	CI			CI	CI	CI		CI			
	-5	CI			CI		CI	CI			CI	CI	CI		CI			
	-4	(CI)			(CI)		(CI)	(CI)			(CI)	(CI)	(CI)		(CI)			
	-3	(CI)			(CI)		(CI)	(CI)			(CI)	(CI)	(CI)		(CI)			
XC5215	-6						CI			CI			CI	CI		CI	CI	CI
	-5						CI			CI			CI	CI		CI	CI	CI
	-4						(CI)			(C)			(CI)	(CI)		(CI)	(CI)	(CI)
	-3						(CI)			(C)			(CI)	(CI)		(CI)	(CI)	(CI)

Notes: Parentheses indicate future product plans C = Commercial T_J = 0° to +85°C I= Industrial T_J = -40°C to +100°C

User I/O Per Package

Device	Max I/O	Package Type																
		PC84	PQ100	VQ100	TQ144	PG156	PQ160	TQ176	PG191	HQ208	PQ208	PG223	BG225	HQ240	PQ240	PG299	HQ304	BG352
XC5202	84	65	81	81	84	84												
XC5204	124	65	81	81	117	124	124											
XC5206	148	65	81	81	117		133	148	148		148							
XC5210	196	65			117		133	149			164	196	196		196			
XC5215	244						133			164			196	197		244	244	244

Ordering Information



XC5200L
Field Programmable Gate Arrays

June 1, 1996 (Version 1.0)

Advance Product Specification

Features

- High-density family of Field-Programmable Gate Arrays (FPGAs)
- JEDEC-compliant 3.3 V version of XC5200 FPGA family
- Design- and process-optimized for low cost
  - 0.5-µm three-layer metal (TLM) process
- SRAM-based, in-system reprogrammable architecture
- Flexible architecture with abundant routing resources
  - VersaBlock™ logic module
  - VersaRing™ I/O interface
  - Dedicated cell-feedthrough path
  - Hierarchical interconnect structure
  - Extensive registers/latches
  - Dedicated carry logic for arithmetic functions
  - Cascade chain for wide input functions
  - Dedicated IEEE 1149.1 boundary-scan logic
  - Internal 3-state bussing capability
  - Four global low-skew clock or signal distribution nets
  - Output slew-rate control
  - 4-mA sink current per output
- Configured by loading binary file
  - Unlimited reprogrammability
  - Seven programming modes, including high-speed Express™ mode
- 100% factory tested
- 100% architecture, pin-out and bit-stream compatible with XC5200 families
- 100% footprint compatibility for common packages
- 5 V tolerant inputs
- Fully supported by XACT*step*™ Development System
  - Includes complete support for XACT-Performance™, X-BLOX™, Unified Libraries, Relationally Placed Macros (RPMs), XDelay, and XChecker™
  - Wide selection of PC and workstation platforms
  - Interfaces to more than 100 third-party CAE tools

Description

The XC5200L Field-Programmable Gate Array Family is engineered to deliver the lowest cost of any FPGA family. By optimizing the new XC5200L architecture for three-layer metal technology and 0.5-µm CMOS SRAM process, dramatic advances have been made in silicon efficiency. These advances position the XC5200L family as a cost-effective, high-volume alternative to gate arrays.

Building on experiences gained with three previous successful SRAM FPGA families, the XC5200L family brings a robust feature set to high-density programmable logic design. The VersaBlock logic module, the VersaRing I/O interface, and a rich hierarchy of interconnect resources combine to enhance design flexibility and reduce time-to-market.

Complete support for the XC5200L family is delivered through the familiar XACT*step* software environment. The XC5200L family is fully supported on popular workstation and PC platforms. Popular design entry methods are fully supported, including ABEL, schematic capture, and synthesis. Designers utilizing logic synthesis can use their existing Synopsys, Viewlogic, Mentor, and Exemplar tools to design with the XC5200L devices.

Table 1: Initial XC5200L Field-Programmable Gate Array Family Members

Device	XC5202L	XC5206L	XC5215L
Max Logic Gates	3,000	10,000	23,000
Typical Gate Range	2,000 - 3,000	6,000 - 10,000	15,000 - 23,000
VersaBlock Array	8 x 8	14 x 14	22 x 22
Number of CLBs	64	196	484
Number of Flip-Flops	256	784	1,936
Number of I/Os	84	148	244
TBUFs per Horizontal Longline	10	16	24

XC5200L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC5200L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial: T_J=0°C to 85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage—CMOS configuration	2.0	5.0	V
V_{IL}	Low-level input voltage—CMOS configuration	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

XC5200L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4 mA, V_{CC} min	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 4 mA, V_{CC} max (Note 1)		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)		N/A	mA
I_{IL}	Leakage current	-10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.25	mA

Notes: 1. With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
2. With no output current loads, all package pins at Vcc or GND, either TTL or CMOS inputs, and the FPGA configured with a MakeBits tie option.

XC5200L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature in plastic packages	+125	°C
	Junction temperature in ceramic packages	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC6200 Field Programmable Gate Arrays

XC6200
Field Programmable Gate Arrays

June 1, 1996 (Version 1.0) — Advance Product Specification

Features

- Advanced Processor-Compatible Architecture
  - FastMAP™ interface allows direct processor read/write access to all internal registers in user design with no logic overhead
  - All user registers and SRAM control store memory mapped onto processor address space
  - Programmable data bus width (8, 16, 32-bits)
  - Easily interfaced to most microcontrollers and microprocessors
- High-Performance Sea-of-Gates FPGA
  - Up to 16K configurable cells
  - Abundant registers, gates and routing resources
  - Extremely high gate count for structured logic or datapath designs
- High Capacity Distributed RAM
  - High speed SRAM control store
  - 2 bytes of synchronous RAM per cell
- High Speed Flexible Interconnect Architecture
  - Low delay hierarchical routing scheme gives large number of fast 'longlines' (Fastlanes)
  - Any cell can be connected to any other
  - Suited to both structured synchronous cell data path type designs or irregular random logic
  - Completely flexible clocks and clears for registers
  - 4 Global low-skew signals
- >110MHz flip-flop toggle rates
- Extremely Flexible Cell Architecture
  - Over 50 distinct logic functions per cell
  - One register and gate/multiplexer possible for *every* cell
- Advanced Dynamic Reconfiguration Capability
  - High speed reconfiguration via parallel CPU interface
  - Unlimited reprogrammability
  - Full or partial reconfiguration/context switching possible
  - Ideal for custom computing applications
- Flexible Pin Configuration
  - All User I/O's programmable as in, out, bidirect, tri-state or open drain.
  - Configurable pull-up/down resistors
  - CMOS or TTL logic levels
  - 8, 16, 32-bit CPU interface
- Testability
  - Pre-tested volume part
  - JTAG capability with library macrocells
- XACT*step* Series 6000 Development System
  - Implement designs using familiar tools like Viewlogic and Synopsys
  - Use PC or Unix workstation platforms
  - Fully automatic mapping, placement and routing
  - Interactive Physical Editor for design optimization
  - Large Xilinx parts library for schematic capture
  - VHDL synthesis

Table 1: The XC6200 Family of Field-Programmable Gate Arrays

Device	XC6209 [1]	XC6216	XC6236 [1]	XC6264 [1]
Max Logic Gates	13,000	24,000	55,000	100,000
Typical Gate Range	9,000 - 13,000	16,000 - 24,000	36,000 - 55,000	64,000 - 100,000
Number of Cells	2304	4096	9216	16384
Max. No. Registers	2304	4096	9216	16384
Number IOB's	192	256	384	512
Cell Rows x Columns	48x48	64x64	96x96	128x128
Max. RAM (bits)	36K	65K	147K	262K

Notes: 1. Planned Product

Description

The XC6200 family is a new type of high performance Field Programmable Gate Array (FPGA) from Xilinx.

The XC6200 series is a family of fine-grain, sea-of-gates FPGAs. These devices are designed to operate in close co-operation with a microprocessor or microcontroller to provide an implementation of functions normally placed on an ASIC. These include interfaces to external hardware and peripherals, glue logic and custom coprocessors, including bit level and systolic operations unsuited for standard processors.

XC6200 FPGAs can provide extremely high gate counts for data path or regular array type designs. In these cases the actual gate count may be considerably higher than those given in Table 1.

An XC6200 part is composed of a large array of simple, configurable cells. Each basic cell contains a computation unit capable of simultaneously implementing one of a set of logic level functions *and* a routing area through which inter-cell communication can take place. The structure is simple, symmetrical, hierarchical and regular, allowing novice users to quickly make efficient use of the resources available.

The nearest-neighbor interconnect of the cells is supplemented with wires of length 4, 16 and chip-length (CL) cells, called FastLane-4, 16 and CL respectively, which provide low-delay paths for longer connections. In addition there are four global input signals which provide a low-skew distribution path for critical high-fan-out nets such as clocks and initialization signals.

An XC6200 part is configured by the content of an integral, highly stable six-transistor SRAM control store. This allows XC6200 parts to be quickly reconfigured an unlimited number of times. The SRAM control store can be mapped into the address space of a host processor and additional support logic is provided to allow rapid reconfiguration of all or part of the device. In addition, the outputs of function units within the device can be read by a processor through the RAM interface. A host processor can read or write registers within logic implemented on the device. Data transfers can be 8, 16 or 32 bits wide, even when register bits are distributed over a column of cells. These capabilities allow XC6200 FPGAs to support virtualised hardware in which circuits running on the FPGA can be saved (`swapped out') to allow the FPGA resources to be assigned to a different task, then restored (`swapped in') at a later time with the correct internal state in their registers. Sections of the device can be reconfigured without disturbing circuits running in other sections. Thus an XC6200 FPGA in a coprocessor application can be time-shared by several processes running on the host computer.

Design entry and verification are carried out with Xilinx XACT*step* Series 6000 software using industry-standard schematic capture, synthesis and simulation packages such as Viewlogic, Synopsys and Mentor Graphics. A comprehensive library of parts, ranging from simple gate primitives to complex macro-functions, exists to make this an easy task.

Below the top level design tools, the XC6200 product family is supported by a number of CAD tools ranging from simple symbolic editors to sophisticated cell-compilation tools. These tools will ensure that the captured design is laid out efficiently with no user intervention. Node delays can then be back-annotated to the top level logic simulator. The tools also allow for manual intervention in the layout process, if desired. Incremental design is also supported: if a design is laid out and subsequently changed, only the modified block has to be re-laid out.

The functions available within each cell provide a good target for logic synthesis programs. The simple cell architecture allows arbitrary user logic designs to be mapped onto a number of cells, rather than having to split the design up into medium-complexity mini-functions for mapping to a larger configurable logic block. Because each cell can be configured as a register, designs containing far more registers than would be possible with a larger configurable block are achievable.

Detailed Functional Description

Logical and Physical Organization

The XC6200 architecture may be viewed as a hierarchy. At the lowest level lies a large array of basic cells (Figure 1). This is the 'sea-of-gates'. Each cell is individually programmable to implement a D-type register and a 2-input logic function such as a multiplexer or gate. Any cell may also be configured to implement a purely combinatorial function, with no register. This is illustrated in Figure 7.

Cells, Blocks and Tiles

First generation fine-grain architectures implemented only nearest-neighbor interconnection and had no hierarchical routing (Figure 1). The XC6200 architecture is a second generation fine-grain architecture, employing a hierarchical cellular array structure. Neighbor-connected cells are grouped into Blocks of 4x4 cells (Figure 2) that themselves form a cellular array, communicating with neighboring 4x4 cell Blocks. A 4x4 array of these 4x4 Blocks forms a 16x16 cell Tile (Figure 3). In the XC6216 part, a 4x4 array of these 16x16 Tiles forms the central 64x64 cell array which is then surrounded by I/O pads (Figure 4).

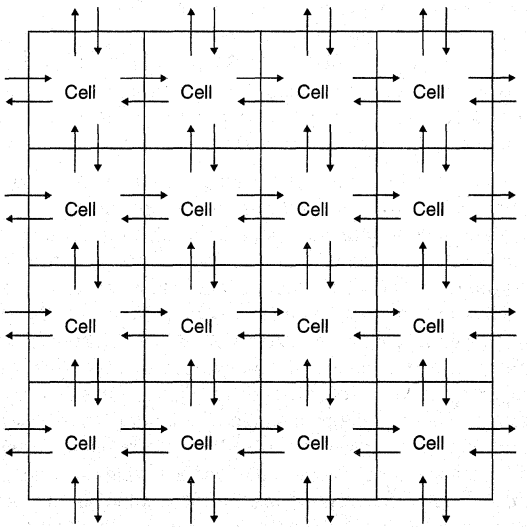


Figure 1: Nearest-Neighbor Interconnect Array Structure

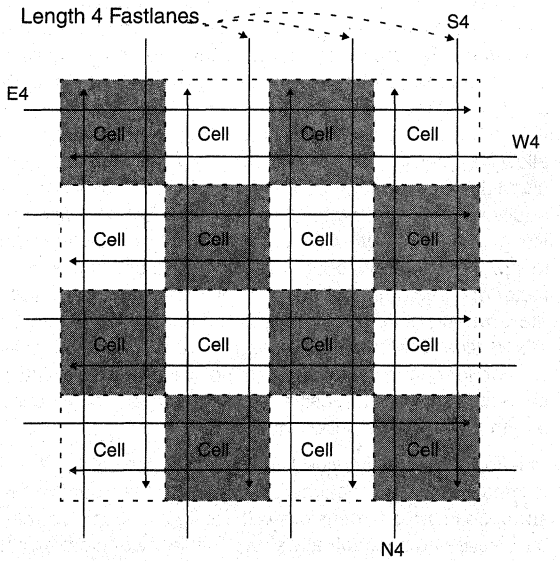


Figure 2: XC6200 4x4 Cell Block

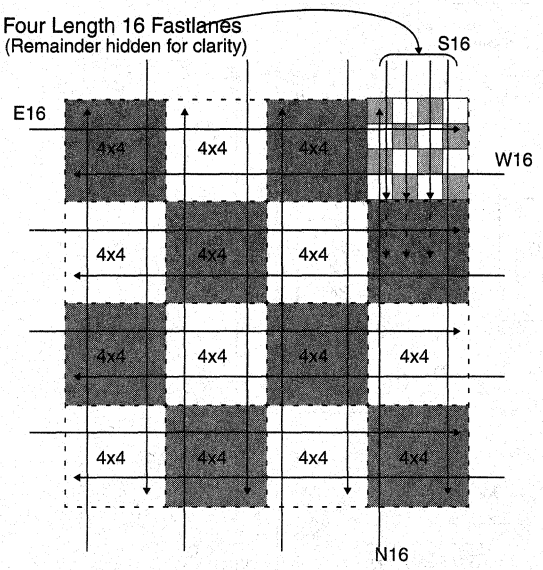


Figure 3: XC6200 16x16 Cell Tile

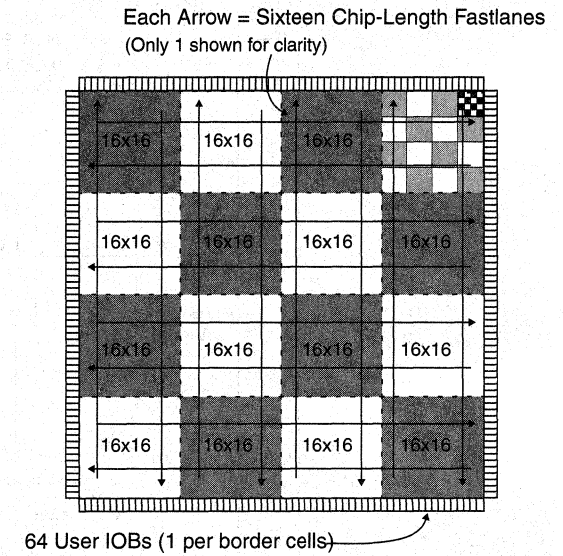


Figure 4: XC6216 Device

Routing Resources

Each level of hierarchy (basic cells, 4x4 cell Blocks, 16x16 cell Tiles, 64x64, etc.) has its own associated routing resources. Basic cells can route to their nearest neighbors or through the neighbor cell to its neighbor. Note that cells used for interconnect in this manner can still be used to provide a logic function. Wires of length four are provided to allow 4x4 cell blocks to route across themselves without using basic cell resources. Similarly 16x16 cell tiles provide additional wires of length 16 cells and the 64x64 array provides wires of length 64. Larger XC6200 products extend this process to 256x256 cell blocks and so on, scaling by a factor of 4 at each hierarchical level as required. Intermediate array sizes (e.g. 96x96) are created by adding more 16x16 tiles. Switches at the edge of the blocks and tiles provide for connections between the various levels of interconnect at the same position in the array (e.g. connecting length 4 wires to neighbor wires).

The longer wires provided at each hierarchical level are termed 'Fastlanes' because it is convenient to visualize the structure in three dimensions with routing at each hierarchical level being conceptually above that in lower hierarchical levels, with the cellular array as the base layer. The length-4 Fastlanes are driven by special routing multiplexers within the cells at 4x4 block boundaries. All routing wires are directional. They are always labelled according to the signal travel direction. For example, S4 is a length-4 Fastlane heading from North to South. In Figures 2, 3 and 4 each individual cell has a length 4, 16 and CL Fastlane above it. However only a small number are shown for clarity.

The benefit of the additional wiring resources provided at each level of the hierarchy is that wiring delays in the XC6200 architecture scale logarithmically with distance in cell units rather than linearly as is the case with the first generation neighbor interconnect architectures. Since 4x4 cell block boundaries lie on unit cell boundaries, the switching function provided at 4x4 cell boundaries is a superset of that provided at unit cell boundaries. i.e it provides for neighbor interconnect between the adjacent cells as well as additional switching options using the length 4 wires. Similarly, the switching unit on 16x16 cell tile boundaries provides a superset of the permutations available from that on the 4x4 cell block boundaries. Further switching units are also provided on the 64x64 cell boundaries to provide the length CL Fastlanes.

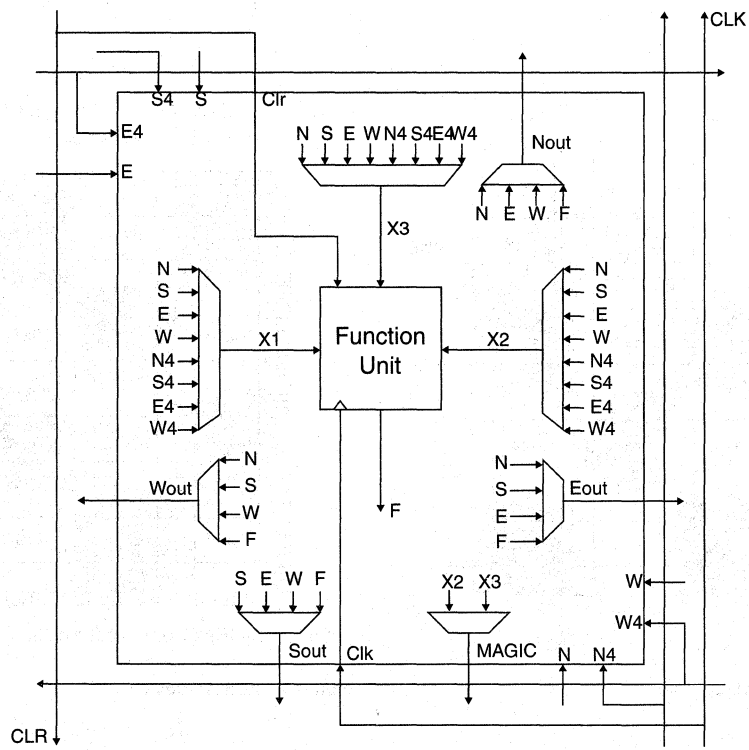


Figure 5: XC6200 Basic Cell

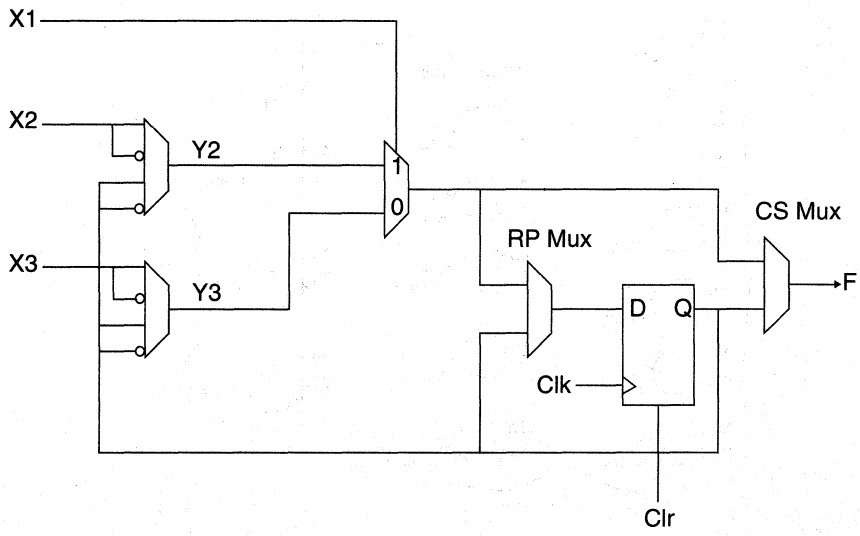


Figure 6: XC6200 Function Unit

Magic Wires

The majority of interconnections are routed using the nearest-neighbor and Fastlane wires described above. Each cell has a further output (labelled 'Magic') which provides an additional routing resource. A cell's Magic output is not always available for routing. Its availability is dependent on the logic function implemented inside the cell. More information on the physical nature of the Magic wires is given in the section "Function Unit" on page 257.

Each cell's Magic output is routed to two distinct 4x4 block boundary switches. The Magic wire can be driven by N, S, E or W from adjacent cells or from the N4, S4, E4 or W4 Fastlanes passing over the cell. This makes it particularly useful for corner-turning (all other routing resources are straight).

The Magic wires are illustrated in Figure 8.

Global Wires

The XC6200 architecture permits registers within a user design to be clocked by different clocks and cleared by different asynchronous clears. Clocks and Clears may be provided by any user I/O pin or generated from user logic internally. In line with good synchronous digital design practices, it is recommended that a single global Clock and Clear are used. This minimizes the likelihood of timing problems and gives more reliable simulations.

Four Global wires (G1, G2, GClk and GClr) are provided for low skew, low delay signals. These wires are intended for global Clock and Clear or other high fan-out signals and are distributed throughout the array in a low skew pattern. A global signal can reach the function block inputs of any cell on the array passing through very few routing switches. The four Globals are very similar. It would be possible to use GClk as a global Clear signal, however for minimum delay, it is recommended that GClk be used for global clocks and GClr for global clears. GClk and GClr can reach the inputs of any register in the array, passing through only a single routing switch. G1 and G2 may be used for secondary global clocks or clears. G1 and G2 have a slightly larger delay than GClk and GClr.

Function Unit

Figure 5 shows the basic XC6200 cell in detail. The inputs from neighboring cells are labelled N, S, E, W and those from length 4 wires N4, S4, E4, W4 according to their signal direction. Additional inputs include Clock and Asynchronous Clear for the Function Unit D-type register. The output from the cell function unit, which implements the gates and registers required by the user's design, is labelled F. The Magic output is used for routing as described earlier. The multiplexers within the cell are controlled by bits within the configuration memory. As can be seen from Figure 5, the basic cells in the array have inputs from the length 4 wires associated with 4x4 cell blocks as well as their nearest neighbor cells. The function unit design allows the cells to efficiently support D-type registers with Asynchronous Clear and 2:1 multiplexers, as well as all Boolean functions of two variables (*A* and *B*) chosen from the inputs to the cell (N,S,E,W,N4,S4,E4,W4) (Table 2). Figure 7 shows the schematic representations of the basic cell functions possible. The Magic routing output can only be used if the signal to be routed can be placed on X2 or X3.

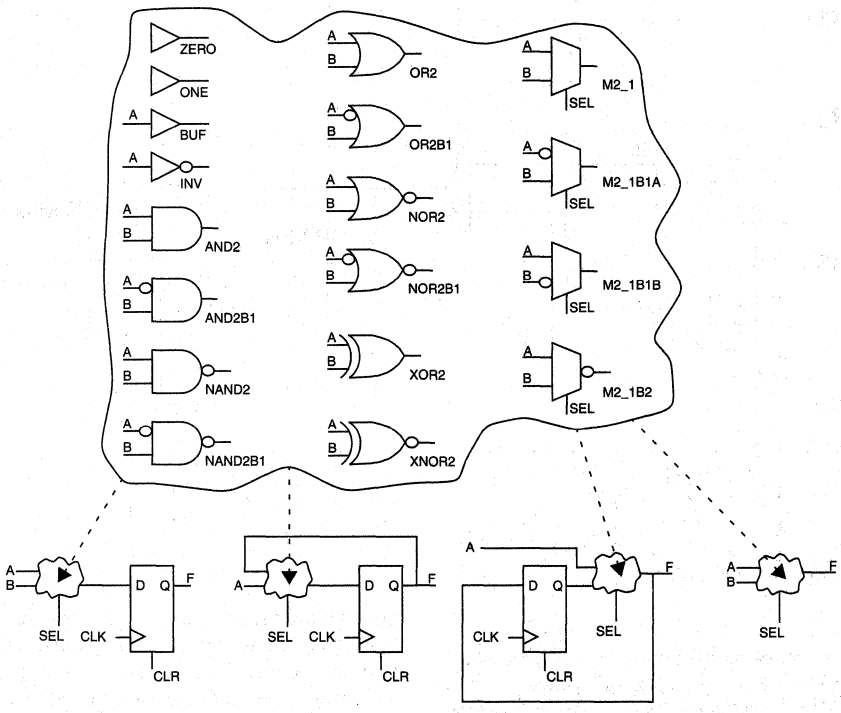


Figure 7: Cell Logic Functions

Figure 6 shows the implementation of the XC6200 function unit. The design uses the fact that any function of two Boolean variables can be computed by a 2:1 multiplexer if suitable values chosen from the input variables and their complements are placed on its inputs. The Y2 and Y3 multiplexers provide for this conditional inversion of the inputs. The CS multiplexer selects a combinatorial or sequential output. The RP multiplexer allows the contents of the register to be 'protected'. If register protection is enabled then only the programming interface can write to the register. It will not change when the X inputs to the function unit change, *even if it is clocked or cleared.* This feature is useful in designs containing control registers which are only to be written by an external microprocessor. The control inputs of all the multiplexers, except the one switched by X1, come from configuration memory bits.

Cell Logic Functions

Each cell can be configured as any two-input gate function, any flavor of 2:1 multiplexer, constant 0 or 1, single input functions (buffer or inverter) or any of these in addition to a D-type register. This is illustrated in Figure 7. The gate names given correspond to standard Xilinx library part names for these primitives. Although three inputs are shown entering the combinatorial 'cloud', dual and single input functions are also possible (e.g. inverter + register or register alone.) The buffer symbol is available in the CAD libraries, however the place and route software will generally optimize this out as there is no requirement for the designer to buffer signals with this architecture. This is because signals are regularly buffered by routing multiplexers. Symmetrical functions are also possible but not shown in Figure 7; e.g. $\overline{A}\bullet B$ (AND2B1) is shown but $A\bullet\overline{B}$ (AND2B2) is not. This is because *A* and *B* are assigned to user signals by the logic mapping software to provide the required function. Thus, a multiplexer with inversion on the SEL input is unnecessary because the mapping software can simply swap the signal assignments for *A* and *B*.

The sources of the X1, X2 and X3 input multiplexers are set automatically by CAD software during the logic mapping phase. Table 2 shows the assignments for all the cell multiplexers to compute the various logic gate functions. A NAND2B1 is equivalent to an OR2B1 with the inputs swapped and a NOR2B1 is equivalent to an AND2B1 with the inputs swapped; therefore, these gates are not listed in Table 2.

If the register within a cell is not used in the design then a special 'fast' version of most gates can be configured, using the register to provide a constant 1 or 0. For example a fast AND gate ($A\bullet B$) can be configured by setting the register to 0 during configuration and assigning Q to Y3. *A* is routed to X1 and *B* to X2. X2 is assigned to Y2. When *A* changes to

Table 2: Function Derivation

Function	X1	X2	X3	Y2	Y3	RP	CS	Q
0 (Fast)	X	X	X	X	X	Q	S	0
0	A	A	A	$\overline{X2}$	X3	X	C	X
1 (Fast)	X	X	X	X	X	Q	S	1
1	A	A	A	X2	$\overline{X3}$	X	C	X
BUF (Fast)	A	X	X	Q	$\overline{Q}$	Q	C	1
BUF	X	A	A	X2	X3	X	C	X
INV (Fast)	A	X	X	Q	$\overline{Q}$	Q	C	0
INV	X	A	A	$\overline{X2}$	$\overline{X3}$	X	C	X
A•B (Fast)	A	B	X	X2	Q	Q	C	0
A•B	A	B	A	X2	X3	X	C	X
$\overline{A}$•B (Fast)	A	X	B	Q	X3	Q	C	0
$\overline{A}$•B	A	A	B	$\overline{X2}$	X3	X	C	X
$\overline{A}$•$\overline{B}$ (Fast)	A	B	X	$\overline{X2}$	Q	Q	C	1
$\overline{A}$•$\overline{B}$	A	B	A	$\overline{X2}$	$\overline{X3}$	X	C	X
A+B (Fast)	A	X	B	Q	X3	Q	C	1
A+B	A	A	B	X2	X3	X	C	X
$\overline{A}$+B (Fast)	A	B	X	X2	Q	Q	C	1
$\overline{A}$+B	A	B	A	X2	$\overline{X3}$	X	C	X
$\overline{A}$+$\overline{B}$ (Fast)	A	X	B	Q	$\overline{X3}$	Q	C	0
$\overline{A}$+$\overline{B}$	A	A	B	$\overline{X2}$	$\overline{X3}$	X	C	X
A⊕B	A	B	B	$\overline{X2}$	X3	X	C	X
$\overline{A⊕B}$	A	B	B	X2	$\overline{X3}$	X	C	X
M2_1	SEL	A	B	X2	X3	X	C	X
M2_1B1A	SEL	A	B	X2	X3	X	C	X
M2_1B1B	SEL	A	B	X2	$\overline{X3}$	X	C	X
M2_1B2	SEL	A	B	$\overline{X2}$	$\overline{X3}$	X	C	X

0, Y3 is selected and F is forced low as soon as the X1-controlled multiplexer switches. In the normal AND gate, there would be an additional delay as *A* propagated through the Y3 multiplexer. Fast or normal gates may be specified by the designer but, for optimal layout density, this is best left to the logic mapping software.

The multiplexer functions have a straightforward mapping with fixed assignments to X1,X2 and X3, and Y2 and Y3 providing input inversions as required.

Routing Switches

As described earlier, each cell within a 4x4 block is able to drive its output to its nearest neighbors to the N,S,E and W. In addition to this, cells at 4x4 block boundaries are also able to drive their outputs onto length-4 Fastlanes. Special switch units are provided around each 4x4 block boundary to facilitate these connections. This is illustrated in Figure 8. These switches also allow higher levels of hierarchical routing (e.g. length – 16 and CL Fastlanes) to be connected to length-4 Fastlanes.

Figure 8 also shows the connections for each cell's Magic output. Each Magic output is routed to two destinations for increased routing flexibility. The two connections are labelled M and MA. The Magic wires allow cell outputs to jump to the edge of the 4x4 block and hence onto Fastlanes or into the next 4x4 block. They are also a particularly efficient way of making large busses turn corners.

N,S,E and W switches are similar, however the N switches contain additional multiplexers to drive the register Clock lines. The contents of the boundary switches are shown in Figure 9 through Figure 12. The multiplexers driving the NOut, SOut, EOut and WOut lines are actually implemented within the cell adjacent to the switch. These multiplexers take the place of the neighbor multiplexers found in the basic cell (see Figure 5). Boundary cells contain additional RAM bits to control the larger multiplexers. An additional output is available from these multiplexers. This output reflects the output that would have come from the cell's neighbor multiplexer had it been a basic non-boundary cell. To distinguish this from the output of the boundary switch (NOut, SOut, EOut or WOut), it is suffixed with a 'C' (Cell); e.g. NC for an Nswitch. NC will be one of NIn, E, W,

or F depending on the least-significant two bits of the NOut multiplexer select lines. Hence NC will be identical to NOut if NOut is one of F, NIn, E or W. If NOut is one of N4In, N16, PS4 or MN then NC will be one of F, NIn, E or W depending on which signal is routed to NOut. The 'C' signal will be one of the upper four inputs to the 8:1 multiplexers shown in Figure 9 through Figure 12, the actual value being selected by the two least-significant multiplexer select lines. Similar 'C' signals are generated in the Sswitch, Eswitch, and WSwitch.

The S4 input to the NOut multiplexer in the Nswitch is actually the S4 *input* to the adjacent Sswitch in the 4x4 block immediately to the North of this block. This should not be confused with the S4Out signal from that block's Sswitch. This is also true of some of the other inputs to the multiplexers in other boundary switches. To avoid confusion, these inputs are prefixed with the letter 'P' (for Previous). e.g. PS4. This feature allows Fastlane wires to perform U-turns.

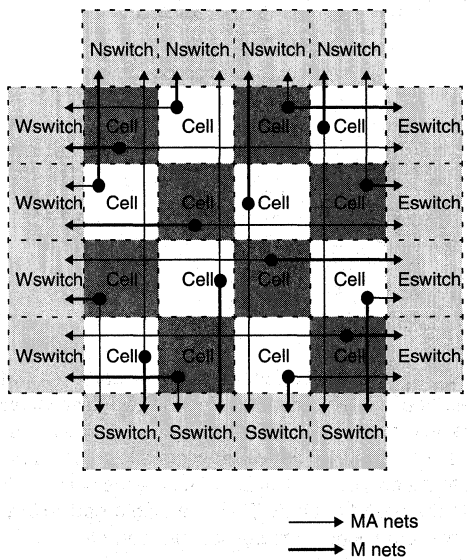


Figure 8: Routing Switches at 4x4 Block Boundary

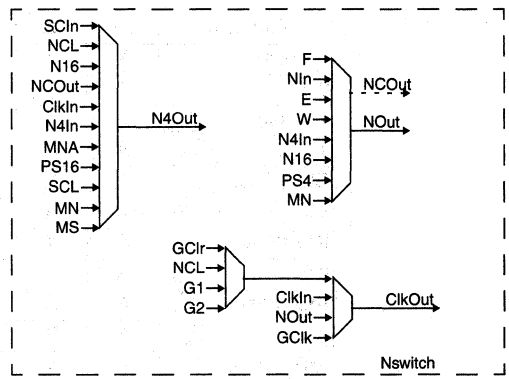


Figure 9: Contents of Nswitch

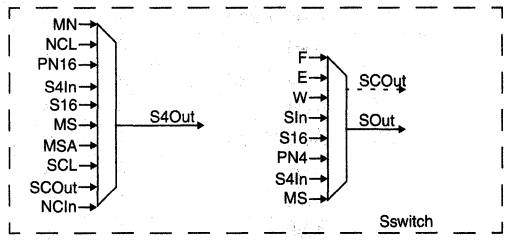


Figure 10: Contents of Sswitch

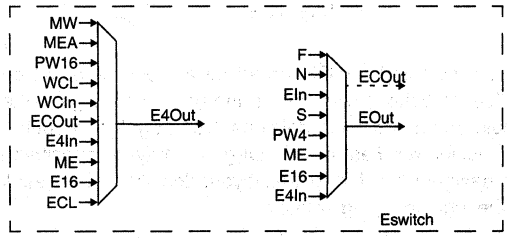


Figure 11: Contents of Eswitch

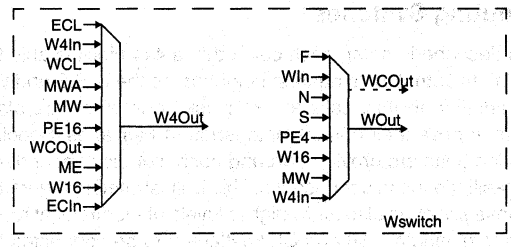


Figure 12: Contents of Wswitch

Clock Distribution

As described previously, register clock inputs may be driven from any source but it is recommended that the GClk signal is used. GClk also has the advantage that it can be stopped by writing to the Device Configuration Register. The Global wires enter the part through dedicated input pins and are distributed in a special low-skew 'H' pattern (Figure 13). Each vertically aligned (South to North) group

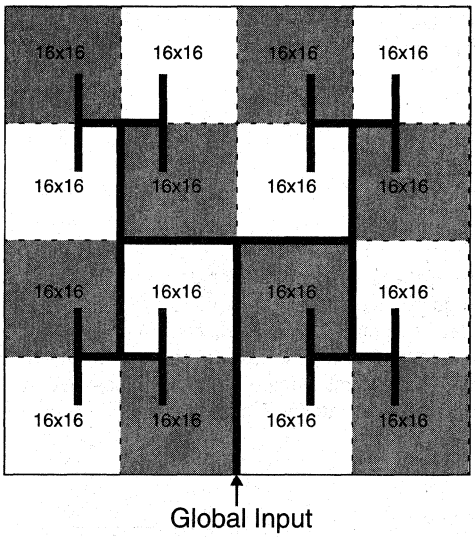


Figure 13: Low Skew 'H' Distribution Of Global Signals (XC6216)

of four cells within a 4x4 block is clocked by its own clock source. This is driven from a multiplexer in the Nswitch immediately to the South of the group of cells. The connections for this multiplexer are shown in Figure 9. ClkOut drives the Clk inputs to each of the four cells in the group. As can be seen from Figure 9, the register clock for each group of four cells can be driven by ClkIn, NOut, GClk, GClr, G1, G2 or NCL. ClkIn is the ClkOut from the 4x4 block to the South, allowing vertical daisy-chaining of clock signals. NOut is the N output from the cell associated with the Nswitch. This can be used to provide local user-generated or gated clock signals if required. GClk is the Global Clock signal direct from the device GClk input. Clearly this signal only has to pass through one 4:1 multiplexer whereas GClr, G1 and G2 have to pass through two. This is one reason why there is less delay on GClk.

It is also possible to route North chip-length Fastlanes onto the Clock lines. This allows up to 64 (for a XC6216 device) locally used clocks to be provided that can still run the entire length of the chip with minimal skew. These local clock signals may be generated internally (e.g. by dividing a faster clock) or sourced directly from the device programmable I/O pins.

Where a fast clock is required by only a small fraction of the logic on the device it may be preferable to employ user interconnect resources rather than a Global or Chip-Length Fastlane, since limiting fast clock distribution to the area of the device where it is required will reduce power consumption.

Clear Distribution

Register Clear inputs are routed in a similar manner to Clock inputs. In this case vertical groups of 16 cells, within a 16x16 tile, share a common Clear. Clear lines run in a Southerly direction and are sourced from the Sswitch unit of 4x4 blocks which also lie on a 16x16 boundary. All of the boundary switches at 16x16 boundaries contain additional switching multiplexers. These are illustrated in Figure 14.

ClrOut drives the Clr inputs to each of the sixteen cells in the group. The S and SCL connections allow the output of a cell to provide a user-generated local Clear signal.

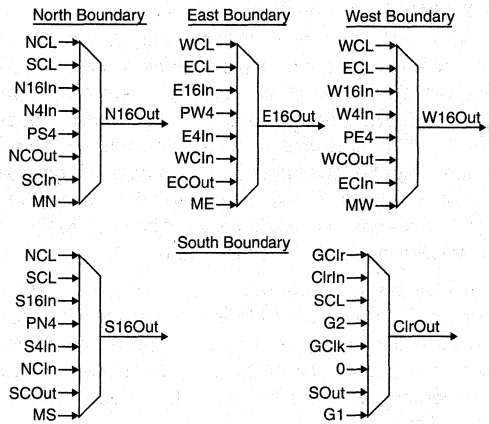


Figure 14: Additional Switches at 16x16 Boundaries

Input/Output Blocks (IOBs)

User-configurable Input/Output Blocks (IOBs) provide the interface between external package pins and the internal logic.

One IOB is provided for every cell position around the array border. IOBs are connected to fixed pad locations. There are more IOBs than available pads, hence some IOBs are 'padless'. However it is still possible to route signals from padless IOBs to device pins.

Figure 15 is a simplified diagram of an IOB and its associated IO pad. The IOB is located at the array border and the pad is located close to its device pin. The pad may be located some distance from its associated IOB. The map-

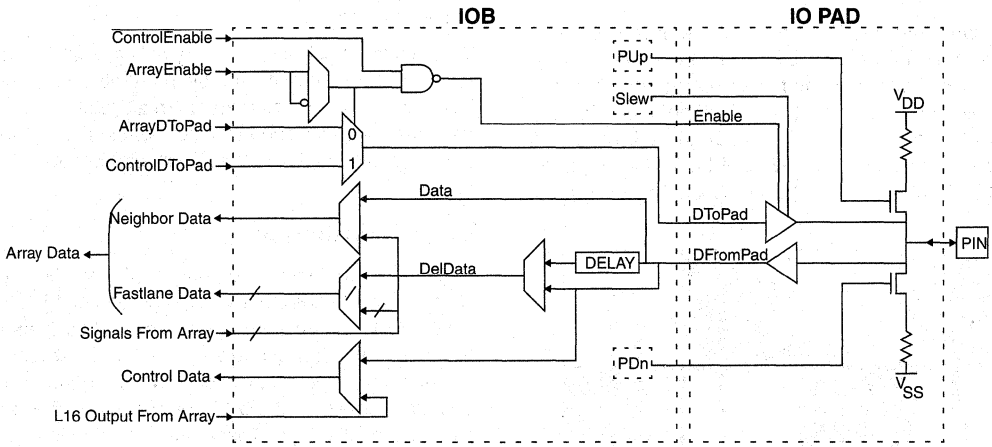


Figure 15: Input/Output Architecture

ping of IOBs to device pins is given in the pinout tables starting on page 282.

The XC6200 IOB architecture incorporates a novel and very powerful feature: every IOB has the capability of routing either an array signal or a control logic signal to/from the device pin. Every signal, including all the control signals (e.g. $\overline{CS}$, Rd$\overline{Wr}$, Address Bus, Data Bus, etc.), passes through an IOB. This means that all the control signals can be routed into the logic array for use in user designs. Similarly, user logic can control the XC6200 internal control circuitry. For example a user signal could be used to drive the internal $\overline{CS}$ signal rather than the $\overline{CS}$ pin.

As an example of the power of this feature, an XC6200 design could include an address decoder which decoded microprocessor read/write cycles and produced appropriately retimed signals for all the parts on a board *including itself*, thereby removing the need for address decoding PAL's or discrete logic.

Each IOB has an array data input and a control data input, labelled ArrayDToPad and ControlDToPad in Figure 15. Associated with these inputs are two enable signals - ArrayEnable and ControlEnable. These signals control whether the pad associated with this IOB is in the input or output mode. Each IOB also supplies ArrayData and ControlData when acting as an input.

The 'Control' signals are routed to the internal XC6200 control circuitry. If control signals are not required all the time then these IOBs can be used to route other user signals into the array. For example if only eight data bus bits were continuously required, the remaining twenty-four IOBs associated with the data bus could be used to route user signals to/from the array. ControlEnable comes either from the internal XC6200 control circuitry if there is a bidirectional control signal or output signal on that IOB, or it is tied inactive.

There are less real control signals than IOBs, hence the three control signals on some IOBs are not connected to the device control logic. These spare control signals are used to route data to and from the padless IOBs mentioned above. The control signals on the padless IOB are not used. This is illustrated in Figure 16.

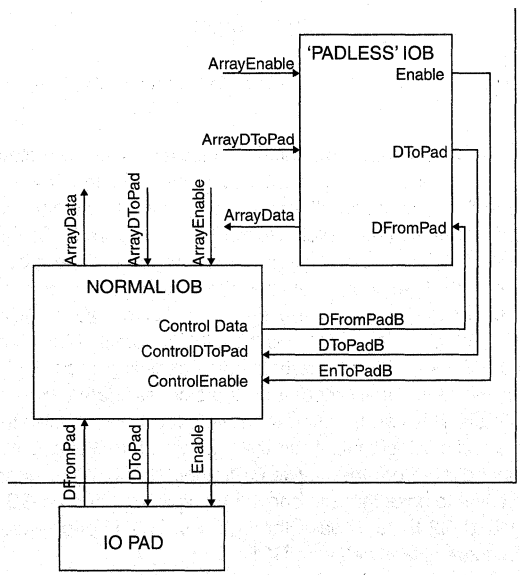


Figure 16: 'Padless' IOB Configuration

The 'Control' signals are also referred to as 'B' signals later in this data sheet. ControlDToPad = DToPadB, ControlEnable = EnToPadB and Control Data = DFromPadB. Also the L16 output from the array, which can be routed onto Control Data, is referred to as DForPadB.

Three configuration RAM bits within each IOB control the programmable aspects of its IO pad. These RAM bits have no effect for padless IOBs. 'PUp' and 'PDn' enable the pull-up and pull-down resistors. The resistors may be used to tie floating logic inputs to a known value. 'Slew' slows the output transition time to reduce supply noise and ground-bounce. The default condition is pull-up off, pull-down off and slew on.

The Array Enable, Array Data and Control Data multiplexers are also controlled by configuration RAM bits. A fixed delay may be optionally applied to Array Data inputs. This allows the input data hold time specification to be removed.

The ArrayEnable and ArrayDToPad signals can be configured to constant 0 or 1 values within the logic array. The constant values are particularly useful for the enable signal when the pin is to function as an input or output rather than a bidirectional pin. Constant values on the data signal and a computed value on the enable signal produce open drain pull-up (DToPad=1) or pull-down (DToPad=0) pins.

During reset, all the output drivers are disabled and the pull-up resistors are enabled. The pull-up and pull-down RAM control bits have no effect. After a reset the output drivers remain in this state. For the output drivers to be enabled, the global $\overline{OE}$ signal must be asserted (low) and a valid configuration must be present in the device ID register. The ID register is usually the last thing to be written during configuration and acts as a check that the programming interface is operating correctly. More details of this are given in the 'Programming' section on page 268. The $\overline{OE}$ signal provides a quick way of disabling all the output drivers and may be activated at any time. Only when $\overline{OE}$ is active and there is a valid ID pattern in the ID register, do the pull-up and pull-down RAM control bits determine the IO-pad resistor configuration.

I/O Routing

The array signals to and from the IOBs are generally just the signals which would have passed between two cells in the array. The ArrayDToPad signal in Figure 15 is actually the neighbor output from the border cell associated with the IOB. The Array Enable signal is the length-4 Fastlane output from the same cell.

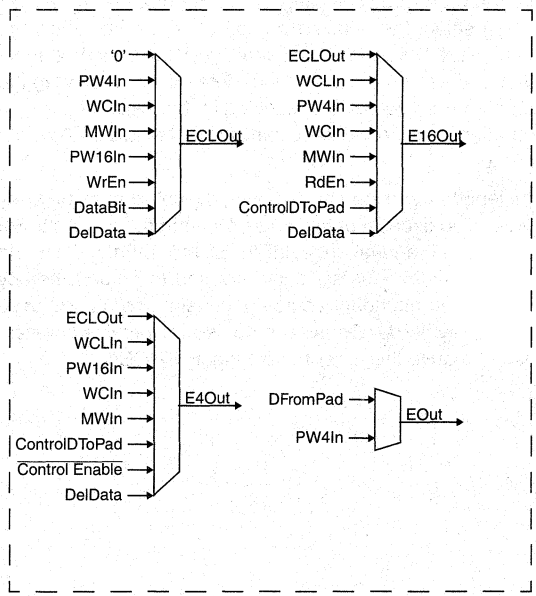


Figure 17: Array Data Sources In West IOBs

The Array Data multiplexer in Figure 15 is actually a collection of multiplexers that source the neighbor, length-4, length-16 and chip-length wires into the array. South IOBs (IOBs at the South edge of the array) also source the local clock signals into the array. North IOBs source the local clear signals. This is illustrated for a West IOB in Figure 17. These multiplexers also allow a number of other internal control signals to be routed into the array: WrEn and RdEn are signals which are active during state register accesses. 'DataBit' is the state register output value for this row during a state access. Details of the timing of these signals are given in the "Parallel Programming Interface" on page 268. Note that in order to provide a minimal delay signal path into the core array, the neighbor data output from the IOB cannot select the delayed version of DFromPad. Only the un-delayed DFromPad and the Previous Length-4 Input can be routed onto the neighbor data output. Therefore the neighbor data output is unaffected by the value of the configuration memory which controls the DelData multiplexer in Figure 15.

The length-4 and length-16 routing multiplexers at the array border also expect some inputs which are not available. For example at the West edge, MEIn, ECIn, PE4In and PE16In are non-existent. These inputs are tied to ground thereby providing an abundant source of constant zeros and ones at the array border. These can be used to provide constant values to drive the Array Enable inputs to IOBs.

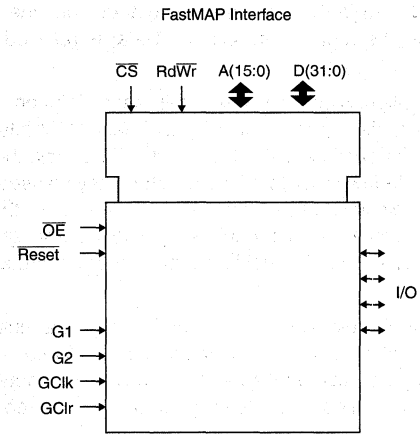


Figure 18: XC6216 Logic Symbol

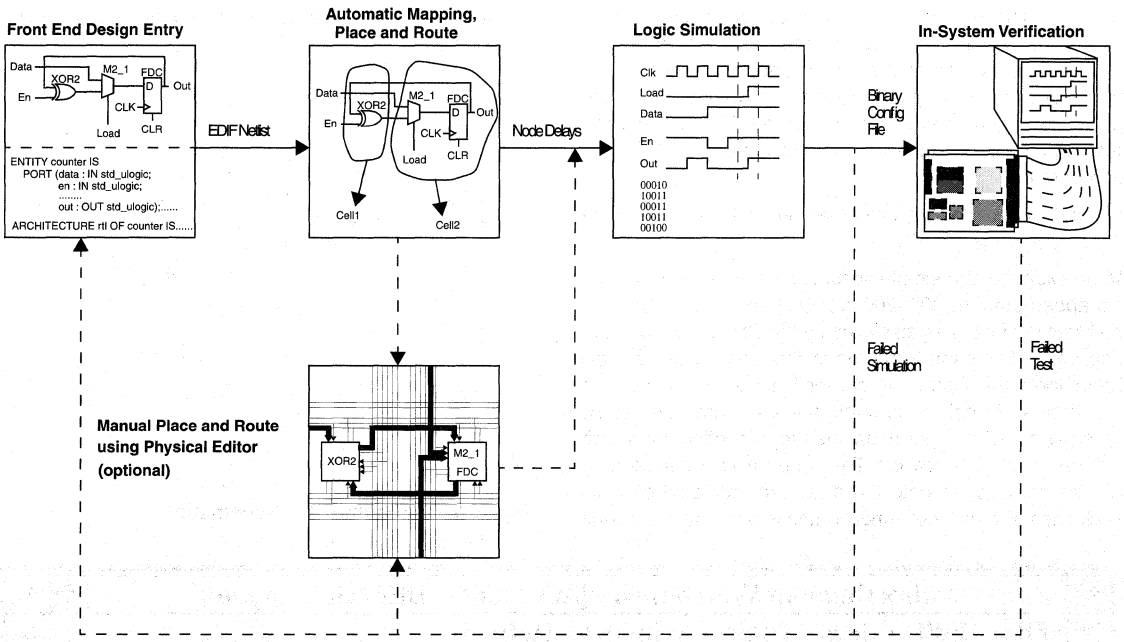


Figure 19: XC6200 Logic Design Flow

Designing with XC6200

The designing of XC6200 FPGAs into systems may be partitioned into three distinct activities: board design, logic design, and software design.

Board Design with XC6200

An XC6200 part may be used on a board design as a microprocessor peripheral part, as an ASIC-type device or as both. In the first instance the XC6200 part will have conventional SRAM data, address and control signals. In other cases, it may only require the user defined I/O signals of an ASIC. Packaging information for the part is shown in Table 6. The number of user I/O signals will depend on the exact package used.

Several XC6200 devices may be tiled together on a board to form a larger array. The regular array structure of XC6200 devices makes this particularly easy.

The configuration RAM bits in the IOBs allow for a number of different programmable options to make interfacing to other ICs easier.

Logic Design with XC6200

This can be approached as an ASIC type design using the function and routing architecture defined in the previous sections. An example design flow is illustrated in Figure 19. The design may be carried out in a variety of different ways. Hardware description languages such as VHDL may be used with the synthesized design targeted to the XC6200 architecture. Alternatively, schematic capture, using the extensive Xilinx Unified Library, with commonly used front end design tools (e.g. ViewLogic PROcapture/ViewDraw) may be used. These tools produce an EDIF netlist which is subsequently passed to the underlying XC6200 place and route software. This automatically maps the user's design to the XC6200 architecture in an efficient way and provides individual node delays which can be passed back to the high level simulation tools such as Viewlogic PROsim/ ViewSim for accurate simulation. Simulation may be carried out prior to placement to check the logical correctness of the design using nominal delays. The place and route software also has optimization capability to carry out tasks such as redundant gate removal. A binary configuration file that can be written to the XC6200 device via the programming interface is also produced automatically. The underlying CAD software is highly integrated with the high level CAD tools, providing user-friendly pull-down menus and dialog boxes to carry out all tasks.

These methods allow designers with little or no knowledge of the XC6200 architecture to quickly produce large and complex designs. Some designers may wish to carry out detailed hand placement and routing to produce ultra-optimized very high-speed/small area sections in their designs. Others may wish to generate large regular structures such as systolic arrays or perform floor-planning for extra efficiency. For these cases, a sophisticated physical editor is available that allows designers to graphically modify the

automatic placement of gates/registers into cells and modify the routing as much as required. Alternatively this software may simply be used to see how the automatic placement and routing software has optimized a design. If a modification is subsequently made, then only the modified part of the design needs to be re-laid out. This incremental design process provides a very rapid change cycle during debugging.

All the design tasks may be carried out on PC or Unix workstation platforms.

As an example, the simple accumulator circuit of Figure 20 is mapped onto the XC6200 architecture. Figure 21 shows the resulting layout as displayed by the Physical Editor running under Microsoft Windows in this case. The Physical Editor tools are also available for Unix workstations. The boundaries of basic cells within the array are denoted by the squares, with larger rectangles representing the switch units on 4 cell boundaries. The wiring resources used by the design mapped onto the array are indicated by solid black lines. When a cell function unit is used by the design it is annotated with the instance names of the mapped primitives. The primary inputs and outputs are not shown in this example.

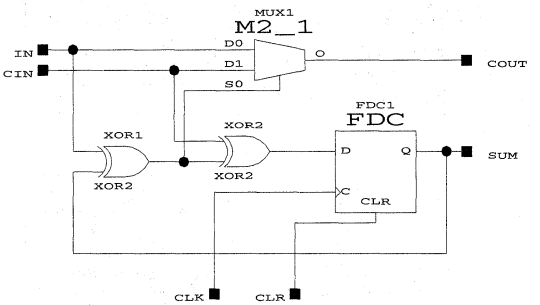


Figure 20: Accumulator Schematic

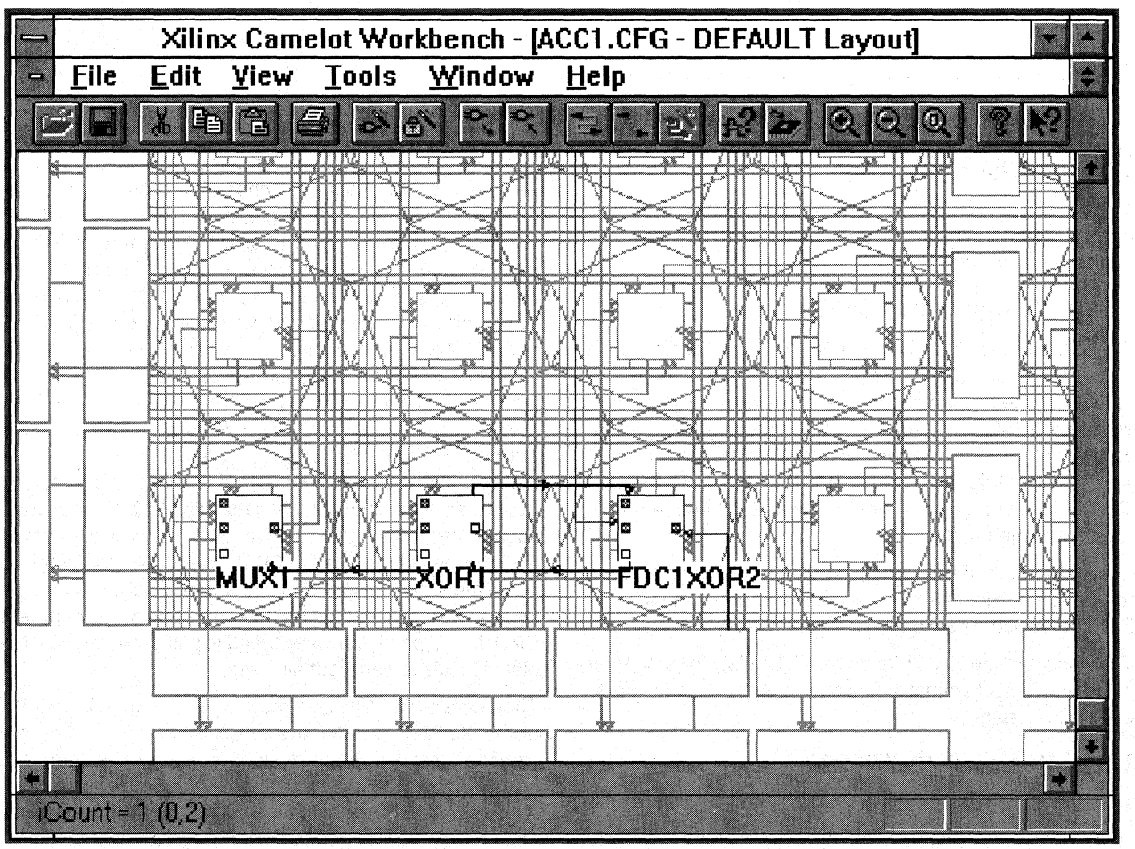


Figure 21: Accumulator Physical Editor View

The inputs and outputs to the function unit are connected to the edges of the cell box. The CAD plot shows all the routing resources available. To the left of each cell the six wires running in a Southerly direction are: SCL, S16, Clr, S4, Magic and S. The signal direction is indicated with arrow heads. S, S4 and Clr are shown entering the cells on the left edge of the cell boxes. The two outputs on the left edge of the cell box are Magic and SOut. The inputs and outputs on the remaining three cell box edges follow a similar pattern. The Clk input on the right hand cell box edge is denoted with a clock '<' symbol.

The Physical Editor allows cells to be selected and moved. The inter-cell routing rubber-bands and adapts automatically to the new placement. The routing may also be manually modified if desired.

Software Design with XC6200

This is the design of a program for the host processor which interacts with a design running on the XC6200 FPGA. Here various registers within the XC6200 design appear as locations within the processor's memory map. In addition, the configuration memory of the device appears within the memory map and portions of the device can be reconfigured as required. Predefined device drivers and an efficient run-time library are available to make optimal use of the high speed reconfiguration capabilities with minimal development time.

Register Access

The XC6200 architecture supports direct accesses from the processor to nodes within the user's circuit: the output of any cell's function unit can be read and the flip-flop within any cell can be written. During state reads a number of cell outputs are routed onto the CPU data bus. The signal which is actually read is the inverse of F in Figure 6 (= Q or $\overline{D}$).

These accesses are carried out through the control store interface and involve no additional wiring within the user's design. The CPU interface signals involved in addressing the cell state can be routed into the configurable array so that user circuits can detect that an access has been made and take appropriate action: for example, calculate a new value for an output register or process a value placed in an input register.

In many applications this access to internal nodes will be the main path through which data is transferred to the processor and in some coprocessor type applications it may be the only external I/O method: user programmable I/O pads may not be required at all.

To allow high bandwidth transfers between the processor and internal nodes it is necessary to be able to transfer a complete processor data word of up to 32 bits in one memory cycle. For this reason, access bits are mapped into a separate region of the device address space from configuration bits so that all the bits in a word contain access bits.

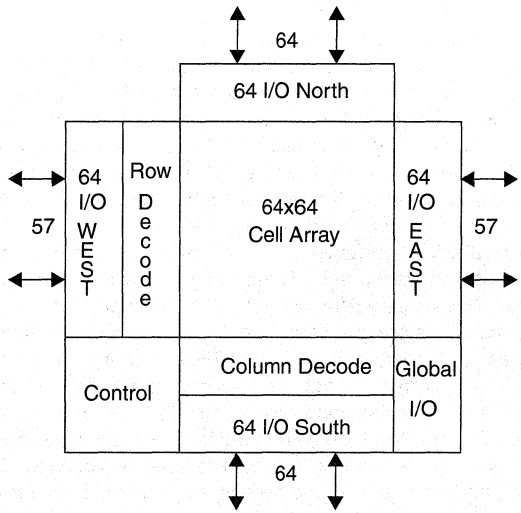


Figure 22: XC6216 Block Diagram

Figure 22 is a block diagram of the XC6216 part, showing the row and column address decoders. Figure 23 shows the mapping of this area of the address space: there are 64 I/O signals from each column of cells and a 6-bit column address selects a particular column of cells to access. This row and column addressing scheme puts a constraint on the placement of registers within the user's design that are to be accessed word-wide: they must be on the same column of cells within the array.

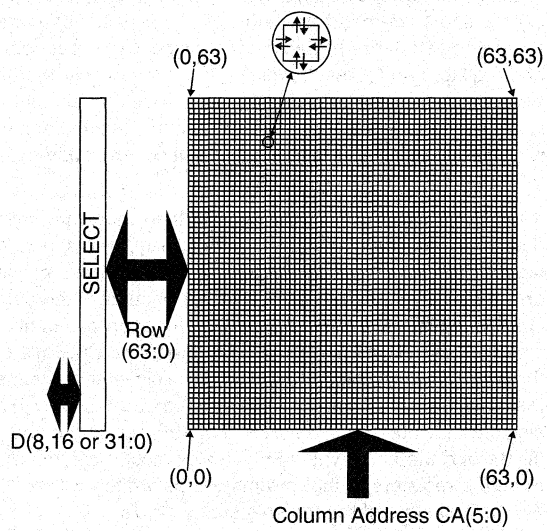


Figure 23: Memory Mapped I/O

Map Register

The XC6200 architecture also provides a mechanism for mapping the 64 possible cell outputs onto the 8,16 or 32-bit external data bus, selecting only those cells that implement bits of the register to be accessed. Without this unit the processor would have to implement a complex sequence of shift and mask operations to discard those bits corresponding to cells not within the register, or the user would have to constrain the layout so that the register bits were in adjacent cells. The mechanism provided takes the form of a 64-bit **map register**, one bit for each row I/O signal from the array. This map register can be read and written through the control store interface and is set up prior to state accesses. A logic 0 in the map register indicates that the cell in the corresponding row is part of the register to be accessed. The unit maps rows from the cell array onto external data lines starting with the least significant bit: thus the first row with a 0 in the map register will connect to external data bus bit 0, the second row with a 0 in the map register to data bus bit 1 and so on.

This technique puts a further constraint on the user's layout: the cells implementing the bits of the register must be ordered so that less significant bits occur below more significant bits. However, there are no constraints about the relative separations of the cells. In practice these two placement constraints: cells occurring in the same column and in order vertically are easy to meet in datapath type designs.

Normally, the map register will be set once to indicate the placement of the user I/O register that will then be accessed many times. Therefore the two write operations required with a 32-bit bus to set up the map register represent a small overhead. In data path type designs where several registers are required, for example two input operand registers and a result register, it is easy to ensure that the corresponding bits of the registers occur on the same row but different columns of the array so that the same map register value can be used with different column addresses to access the various registers.

If more '0's exist in the map register than there are valid data bus bits then a form of wildcarding occurs during writes. The data bus bits are allocated to the rows of the array with a '0' in their map register bit. Once all of the data bus bits have been allocated, Bit 0 of the data bus is allocated to the next row whose map register bit is a '0', Bit 1 of the data bus to the next row and so on. This feature means that an entire column of state registers can be written with a single 8-bit write. For example, if the map register contains all '0's and the CPU writes FFh to a particular column. All the state registers in that column will be written with a '1'. The default state of the map register is all '0's.

During reads, if there are more '0' bits in the map register than data bus bits, the first rows with '0' bits are mapped onto the bus.

If there are less '0's in the map register than data bus bits, the upper data bus bits, which are not mapped, will be read as '1's during CPU reads and ignored during CPU writes.

An example of map register operation is shown in Figure 24. The position of the user-defined register within the cell array is defined by the '0's in the 64-bit map register. Similar registers could be defined for every column in the array if desired.

There is a delay after a write to the map register before the change takes effect. No state accesses should be carried out during this time.

Mask Register

A mask unit controlled by a 32-bit register is placed between the external data bus and the internal data connections. When the external data bus is 8 or 16 bits wide only the bottom 8 or 16 bits of this register are significant. A logic '1' in a bit of this register indicates that the corresponding bit of the internal data bus is *not* relevant. Bit locations corresponding to '1's in the Mask Register will retain their values when written. On a write operation the corresponding bit line will not be enabled and the state information for that bit will not be changed. When the device is reset the Mask Register will contain all logic 0's corresponding to all data bus bits valid.

During CPU reads, valid register bits which are disabled will be read as '0'. Invalid bits (bits which do not physically exist for the register being read) may be read as '0' or '1'.

The mask register does not affect state register accesses. In this case the map register can be used to prevent certain bits being modified.

Programming

The binary data for configuring an XC6200 device, generated by CAD software from the textual description of a user design, must be downloaded into the part itself. This may be performed in several ways. Generally, the fastest and most efficient way is by writing directly to the control store, mapped into the address space of a host processor. If a microprocessor or other parallel data source is not available, then the serial programming interface may be used.

Parallel Programming Interface

The XC6200 FPGA has a conventional programming interface for static RAM, based on Chip Select ($\overline{CS}$) and Read/Write (Rd$\overline{Wr}$) control signals. The $\overline{CS}$ signal can be used to address a single part within an array of devices and allows data to be read or written. Timing for these signals is illustrated in Figures 28 and 29. These figures show that the programming interface is synchronous. The GClk input is used to sample all the interface signals. GClk is also used when accessing user registers as illustrated in Figure 24. This is an important point, as only registers clocked directly by GClk can be reliably read or written using this method.

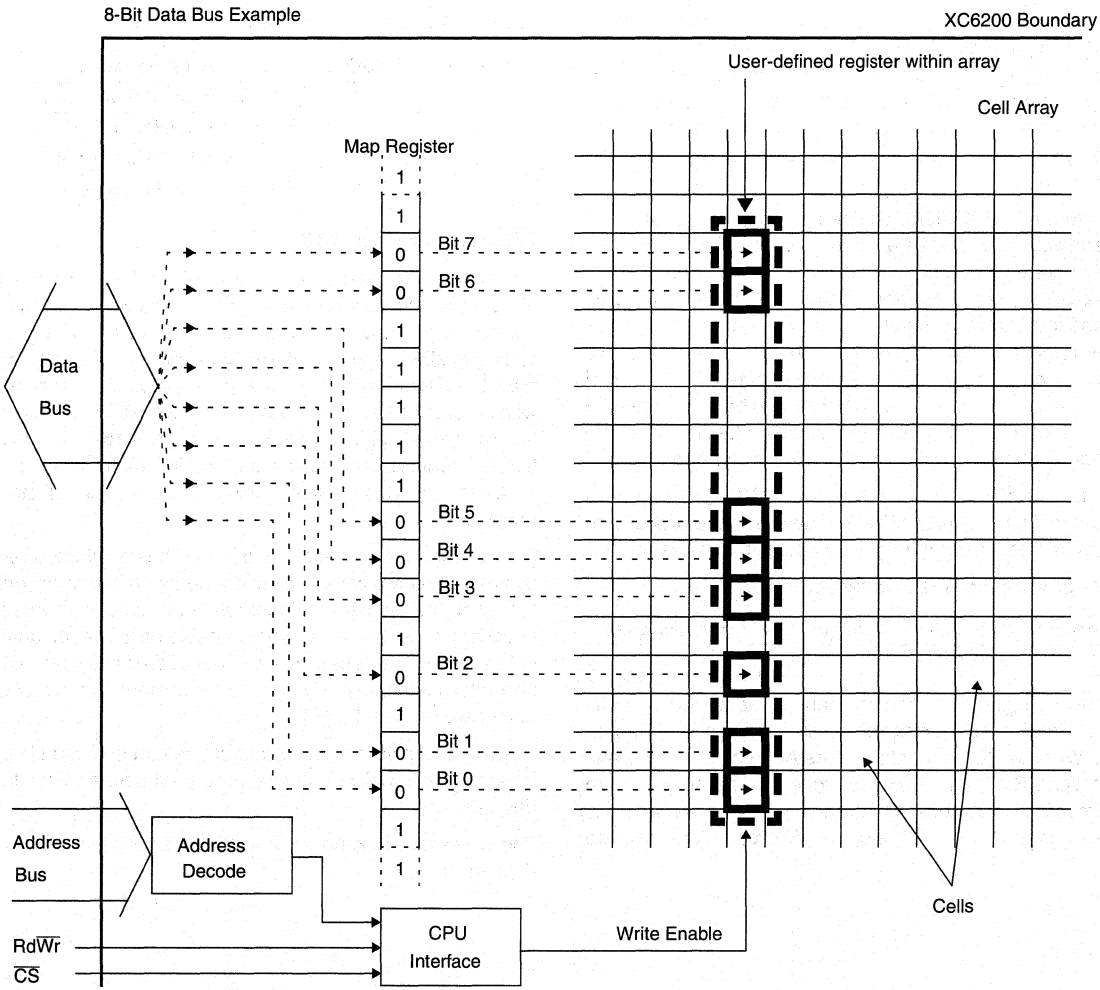


Figure 24: Internal Register Access

Figure 29 shows two separate read cycles - a normal cycle immediately followed by an extended cycle. In the normal read cycle $\overline{CS}$ is sampled low on the first rising GClk edge (t_1) and high on the next (t_2). The data bus is then driven until the next rising GClk edge (t_3). In cases where this is not long enough, the read cycle can be extended by keeping $\overline{CS}$ asserted beyond t_2. This is equivalent to adding wait states. In this case the data bus is driven until $\overline{CS}$ is deasserted. $\overline{CS}$ should not be allowed to go high and low again. This would cause another cycle to begin. $\overline{CS}$ is sampled on every rising GClk edge. Other CPU interface signals such as Rd$\overline{Wr}$ and the Address Bus are only sampled on the first GClk edge of the cycle (t_1 for the first cycle and t_3 for the second in the figure examples).

Extended write cycles are also possible, however these are functionally no different to normal write cycles, the data and address busses still being sampled on the first rising GClk edge of the cycle (t_3 in Figure 28).

$\overline{CS}$ must always be sampled as a '1' before the next cycle can begin. In Figure 29 the extended read cycle starts immediately after the normal read cycle at time t_3. A write cycle could not start until the *next* rising GClk edge as the data from the read cycle is still on the data bus.

The SRAM programming interface is supplemented by additional hardware resources designed to minimize the number of processor cycles required for reconfiguration.

These resources are initially inactive after a reset so the device looks like an SRAM.

The control store layout is designed to minimize the overhead of computations required for dynamic access while maintaining adequate density to minimize the external storage required for device configurations. When an external processor is used to configure the device it may be convenient to use a compressed format of the configuration information.

A feature of the XC6200 architecture is that a rectangular area of cells specified as a hierarchical block within a user's design corresponds directly with a rectangular area within the configuration memory of the XC6200 device. This means that a block within the user's design can be dynamically replaced with another block by the host processor, reconfiguring only the corresponding area of the control store. The binary data for both blocks can be pre-calculated from the cellular design and the actual replacement can be carried out very rapidly using a block transfer operation.

The format of the address bus to the XC6216 device is shown in Table 3. Larger XC6200 devices have proportionally more bits allocated to row and column addresses.

Table 3: Address Bus Format (XC6216)

Mode(1:0)	Column(5:0)	Column Offset<1:0>	Row(5:0)
15:14	13:8	7:6	5:0

All the configuration memory can be accessed as 8-bit bytes. When a 16-bit transfer occurs Address<0> is irrelevant. When a 32-bit transfer occurs Address<1:0> is irrelevant. Data Bus bits <7:0> are written to the address with Address<1:0>=00, bits <15:8> are written to the address with Address<1:0> = 01, etc. The Address Mode bits are used to determine which area of the control store is to be accessed according to Table 4.

Table 4: Address Mode Selection

Mode1	Mode0	Area Selected
0	0	Cell Configuration and State
0	1	East/West Switch or IOB
1	0	North/South Switch or IOB
1	1	Device Control Registers

Wildcard Registers

The wildcard register allows many cell configuration memories within the same column of cells to be written simultaneously with the same data. This is used during device testing to allow regular patterns to be loaded efficiently into the control memory but is more generally useful, especially with regular bit sliced designs, since it allows many cells to be changed simultaneously. For example, a 16-bit 2:1 multiplexer could be built using cell routing multiplexers and switched between sources using a single control store access.

Similarly, the column address decoder has a wildcard register which allows several cells on the same row to be written with the same configuration. The column address decoder drives the word lines to enable particular columns of RAM cells. In this case the number of columns which can be written simultaneously is limited to 32: that is at most five don't care bits can be set.

The row and column wildcard registers can be used simultaneously to rapidly configure regular structures onto the device.

The address decoding for the XC6216 FPGA is summarized in Table 5.

Table 5: XC6216 Memory Map

Address Bus	Decode	
A[15:14] (Mode[1:0])	00	Cells
	01	East/West Switch or IOB
	10	North/South Switch or IOB
	11	Control Registers
A[13:8] (Column[5:0])	Cell Mode - Cell column	
	North/South Mode - Switch column	
	East/West Mode - Column[5:2] = 4x4 block number Column[1:0] decoded as:	
	00	West Switch
	01	West IOB (Column[5:2]=0000)
	10	East IOB (Column[5:2]=1111)
	11	East Switch
A[7:6] (Column Offset[1:0])	Cell Mode	
	00	Neighbor Routing
	01	Function Input Routing
	10	Function
	11	State Access (Cell Registers)
	North/South Switch Mode	
	00	N/S Switch or N/S IOB Reg 0
	01	N/S Switch or N/S IOB Reg 1
	10	N/S Switch or N/S IOB Reg 2
	11	N/S Secondary Clock Mux (Column[1:0] = 00 or 11)
	East/West Switch Mode	
	00	E/W Switch or E/W IOB Reg 0
	01	E/W IOB Reg 1
A[5:0] (Row[5:0])	Cell Mode - Cell row	
	East/West Mode - Switch row	
	North/South Mode - Row[5:2] = 4x4 block number Row[1:0] decoded as:	
	00	South Switch
	01	South IOB (Row[5:2]=0000)
	10	North IOB (Row[5:2]=1111)
	11	North Switch

Serial Programming Interface

All the memory mapped locations in an XC6200 device may be written in parallel or serial mode. All the operations which can be carried out with the parallel interface may also be done serially. The serial interface gives random access to all the XC6200 memory locations. The serial interface is designed to operate with any Xilinx serial PROM. A single serial PROM may be used to configure several FPGAs. In this case one of the FPGAs acts as a 'Master' and the others as 'Slaves'. The Master controls the serial PROM and the Slaves. This is illustrated in Figure 25.

The serial PROM interface consists of 6 dedicated I/O pins:

$\overline{Serial}$ Input that controls transitions between states in serial mode state machine.

0 => serial mode, 1 => parallel mode

Wait Input that controls transitions between states in serial mode state machine.

0 => continue loading, 1 => pause until *Wait* deasserted

SEReset Output from Master FPGA that resets serial PROM address counter.

$\overline{SECE}$ Output from Master FPGA that enables serial PROM output.

SEClk Output from Master FPGA that clocks serial PROM and slave FPGAs. *SEData* is clocked into the FPGAs on the rising edge of *SEClk*.

SEData Serial data input to FPGA. This is sampled in the FPGA by *SEClk* and retimed by the FPGA's own GClk.

In a multi-FPGA configuration a user I/O also will have to be available to provide the Wait input to the next device in the chain.

On Reset each FPGA examines its $\overline{Serial}$ and Wait inputs. Any FPGA that sees both these signals low at this time assumes it is the master and drives SEReset, $\overline{SECE}$ and SEClk. All User I/Os are held in a high-impedance state (with pull-up) until a valid configuration is loaded. In Figure 25, the User I/Os will be pulled high on Reset, hence the Wait input to the Slaves will be high and they will configure as Slaves. A valid configuration is assumed when the device ID register is loaded with the correct ID. Programmable I/Os can only be enabled when this is present.

Serial data is loaded in address/data pairs. Once an address/data pair has been shifted into the FPGA, the data word is parallel written to the corresponding address inside the FPGA just as though a parallel CPU write had occurred. This means it is possible to do all the things which can be accomplished with the parallel interface, e.g. use of the mask register, writes to cell state registers, etc.

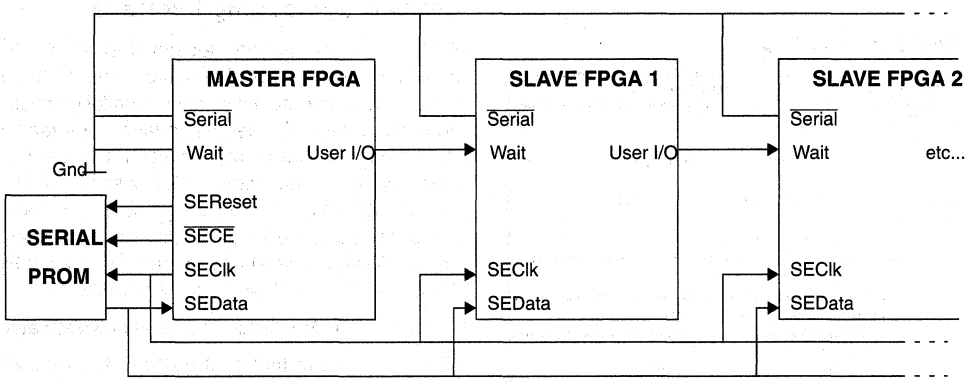


Figure 25: Master-Slave Serial Configuration

The write operation is pipelined so there need be no interruption in the serial data stream. The first address/data pair must be preceded by a Synchronization Byte = 1111_1110. There are no start/stop bits, checksums or error check/correction bits.

The address and data are shifted in MSB first. The address is always 16-bits. The data word is initially 8-bits but may be increased to 16 or 32 bits by loading the device configuration register with the appropriate code. The bits are shifted in on the rising edge of SEClk. The SEClk rate may also be increased by writing the appropriate code to the device configuration register. Initially SEClk is 1/16 GClk frequency. It can also be set to 1/8, 1/4 or 1/2 GClk.

An example is shown in Figure 25. Data1 is loaded into Addr1 after the address lsb has been shifted in. In this example the first write was to the device configuration register and the data bus width was changed from 8 to 32 bits. Data word 2 starts immediately after Addr1 has been shifted in. Due to the new data bus width, 32 data bits will be shifted in. If the width had not been changed data word 2 would also have been 8 bits. Data will continue to be loaded until $\overline{\text{Serial}}$ goes high or Wait goes low.

Reset And Initialization

When the XC6200 FPGA is powered up or after a reset, all configuration memory is cleared and the cell state registers are cleared. The $\overline{\text{Reset}}$ pin is not required to be active during or after power-up to initialize the FPGA. To avoid potential high current random configurations, the power-up reset is carried out automatically. The automatic power-up initialization takes 2.5 µs. All the XC6200 I/O pads are disabled during this time and it is impossible to access the device. The XC6200 may be re-initialized at any time by asserting the $\overline{\text{Reset}}$ input for a minimum of 20 ns. This acts as a signal to the chip to initialize itself. This initialization occurs after $\overline{\text{Reset}}$ has been deasserted. Therefore there is a 1.0 µs (typ.) reset recovery time when no device accesses are possible.

Pin Descriptions

The pins are labelled as follows:

V_{DD}

Connections to the nominal +5V supply. All must be connected.

GND

Connections to ground. All must be connected.

$\overline{CS}$

Chip Select enables the programming circuitry and initiates address decoding. When $\overline{CS}$ is low, data can be read from or written to the control memory. This signal is intended to be used in conjunction with address decoding circuitry to select one part within a larger array for programming.

D<d:0>

(d+1)-bit bidirectional data bus. Used for device configuration and direct cell register access.

A<a:0>

Address bus for CPU access of internal registers and configuration memory. 'a' varies between family members.

Rd$\overline{Wr}$

When $\overline{CS}$ is low this signal determines whether data is read from or written to the control memory. If Rd$\overline{Wr}$ is high then a read cycle takes place. If Rd$\overline{Wr}$ is low, then a write cycle takes place.

GClk, GClr, G1, G2

Global signals. GClk should be used for global user clocks, GClr for global user clears and G1 and G2 for other global, low-skew signals. The GClk pin is *always* configured as an input and cannot be used as a fully flexible User I/O like the majority of other control signals.

$\overline{Reset}$

When $\overline{Reset}$ is taken low the programming registers (mask unit and address wildcard unit) are re-initialized, resulting in the XC6200 device appearing as a conventional SRAM. The control store of the cell array is initialized into a low power consumption configuration. All programmable output pad enable signals are forced inactive. All the IO-pad pull-up resistors are also enabled. This signal should be taken low immediately after power up to initialize the device. This pin is *always* configured as an input and cannot be used as a fully flexible User I/O like the majority of other control signals.

$\overline{OE}$

When this signal is low the outputs of all programmable I/O pads are forced into a high impedance state (independent of the contents of the control store). All the IO-pad pull-up resistors are also enabled. This pin is *always* configured as an input and cannot be used as a fully flexible User I/O like the majority of other control signals.

$\overline{Serial}$

Input which controls transitions between states in serial mode state machine.

Wait

Input which controls transitions between states in serial mode state machine.

0 => continue loading, 1 => pause until Wait deasserted

SEReset

Output from Master FPGA which resets serial PROM address counter.

$\overline{SECE}$

Output from Master FPGA which enables serial PROM output.

SEClk

Output from Master FPGA which clocks serial PROM and slave FPGAs.

SEData

Serial data input to FPGA. This is sampled in the FPGA by SEClk and retimed by the FPGA's own GClk.

ConfigOK

Signal is active (high) when a valid pattern is present in the ID register and inactive when the pattern is invalid.

N_x

North I/Os. Connections to I/O Blocks on the north of the array.

S_x

South I/Os. Connections to I/O Blocks on the south of the array.

E_x

East I/Os. Connections to I/O Blocks on the east of the array.

W_x

West I/Os. Connections to I/O Blocks on the west of the array

Electrical Parameters

The XC6200 series is fabricated in 0.65 micron triple metal n-well CMOS. Foundry sources for this part have been chosen to meet or exceed relevant military standards and industry practice.

As with all CMOS devices, care must be exercised when handling this part as it can be damaged by static discharge, although standard circuit design procedures have been adopted to minimize this risk.

The power consumption of a XC6200 device can vary from a few tens to several hundreds of milliamps depending on its configuration and the data applied to it. The most significant sources of power consumption are I/O blocks and dynamic dissipation within the array, both of which are largely under user control. Dynamic power dissipation is of most concern where the XC6200 device is used to implement highly concurrent computations. Power dissipation must be considered carefully, not only because excessive dissipation could result in device failure but also because operating speed is reduced at high temperature.

A 0.22µF decoupling capacitor across V_{CC} and *GND* per part is recommended. Surface mounted, radial, plastic or ceramic capacitors are suitable.

Where possible, user designs that could result in many output pads making a simultaneous transition in the same direction should be avoided. This is especially important on heavily loaded connections to non-XC6200 parts. To minimize power dissipation, redundant connections in user designs (which may arise in hierarchical design styles to promote sub-block re-use) should be deleted by CAD programs prior to programming XC6200 devices. As a general guideline, users should attempt to minimize the number of cell resources used. Where buffers must drive heavy external loads it may be helpful to choose I/O blocks near *GND* pads.

XC6200 parts automatically reset themselves after power up, since the random values in the control store at this time could correspond to a relatively high power dissipation configuration.

The XC6200 part distributes power using a redundant scheme which ensures minimal voltage drop between pads and internal circuitry. Power for pads is distributed on a separate power and ground ring.

The maximum power consumption of the XC6200 is limited by two factors: the metal conductors supplying the part and heat dissipation. The metal conductors can handle up to 100mA each. Heat dissipation is generally a much more serious consideration: a full discussion of thermal characteristics for the different package options is given in section 4 of this data book.

XC6200 Switching Characteristics

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest sheet before finalizing a design.

XC6200 Operating Conditions

Symbol	Parameter			Min	Max	Units
V_{CC}	Supply voltage relative to GND	Commercial	T_J = 0° C to 85° C junction	4.75	5.25	V
	Supply voltage relative to GND	Industrial	T_J = -40° C to 100° C junction	4.50	5.50	V
V_{ILT}	Low-level input voltage – TTL configuration			0	0.80	V
V_{IHT}	High-level input voltage – TTL configuration			2.0	V_{CC}	V
V_{ILC}	Low-level input voltage – CMOS configuration			0	20%	V
V_{IHC}	High-level input voltage – CMOS configuration			70%	100%	V
T_{IN}	Input signal transition time				250	ns

XC6200 DC Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	High-level output voltage	I_{OH} = -8.0 mA V_{DD} = Min	3.86		V
V_{OL}	Low-level output voltage	I_{OL} = 8mA V_{DD} = Min		0.4	V
I_{IL}	Input leakage current	V_{DD} = Max V_{IN} = GND or V_{CC}	10	10	µA
I_{OZ}	Output high-Z leakage current	V_{DD} = Max V_O = GND or V_{CC}		TBA	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		15	pF
I_{CC}[2]	Quiescent Supply Current	V_{IN} = V_{CC} or GND V_{DD} = 5 V f = 1.0 MHz @ 25°C		TBA	mA

Notes: 1. Sample tested.
2. Measured with no output loads, no active input pull-up resistors and all package pins at V_{CC} or GND.

XC6200 Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC}+0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC}+0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: *Stresses beyond those listed under XC6200 Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under XC6200 Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.*

XC6200 Power-on/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
T_{WMR}	Master Reset input Low pulse width		20		ns
T_{MRR}	Recovery time after Master Reset deasserted		1		µs
T_{PRR}	Recovery time after power up		2.5		µs
			Advance		

XC6200 Serial Configuration Timing

	Description	Symbol		Min	Max	Units
SEClk	SEData setup	1	T_{DC}	TBA	-	ns
	SEData hold	2	T_{CD}	TBA	-	ns
	Setup before GClk	3	T_{CG}	TBA	-	ns
	Hold after GClk	4	T_{GC}	TBA	-	ns
				Advance		

XC6200 Global Buffer Switching Characteristic Guidelines

	Speed Grade:	-2		
Symbol	Parameter	Min	Max	Units
T_{PGClk}	From pad through **GClk** buffer to any register clock		12	ns
T_{PG}	From pad through **G1,G2,GClr** buffers to any register clock		12	ns
T_{PClr}	From pad through **global** buffers to any register clear		11	ns
T_{PCkS}	Skew between any pair of register clocks using the same **global**		0.9	ns
T_{PClS}	Skew between any pair of register clears using the same **global**		0.9	ns
		Advance		

Note: Typical loading values are used.

XC6200 Cell Switching Characteristic Guidelines

	Speed Grade:	-2		
Symbol	Parameter	Min	Max	Units
T_{ILO1}	X1 change to Function Output(1)		2	ns
T_{ILO23}	X2/X3 change to Function Output(2)		3	ns
T_{ICK1}	Internal Register Set-Up Time @ X1(1)	3.5		ns
T_{ICK23}	Internal Register Set-Up Time @ X2/X3(2)	4		ns
T_{IHCK1}	Internal Register Hold Time @ X1(1)	-1.5		ns
T_{IHCK23}	Internal Register Hold Time @ X2/3(2)	-2		ns
T_{CH}	Clock High Time(3)	4.5		ns
T_{CL}	Clock Low Time(3)	4.5		ns
f_{TOG}	Export Control Max. flip-flop toggle rate		111	MHz
T_{CLW}	Clear Pulse Width(3)	1		ns
T_{CKO}	Clock to Function Output		2	ns
T_{CKLO}	Clock to Function Output via X2/X3 feedback mux's		3	ns
		Advance		

Notes: 1.Data input measured at input to X1 routing multiplexer. Clock input measured at register.
2.Data input measured at input to X2/X3 routing multiplexers. Clock input measured at register.
3.Measured at the actual register in the cell.
4.Typical loading values are used.

XC6200 Guaranteed Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly and guaranteed over all the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The delay calculator software uses this indirect method. When there is a discrepancy between these two methods, the directly tested values listed below should be used and the derived values should be ignored.

Speed Grade:		-2				
		Best I/O		Worst I/O		
Symbol	Parameter	Min	Max	Min	Max	Units
T_{ICKOF}	Global Clock (GClk) to Output (fast)				19	ns
T_{ICKO}	Global Clock (GClk) to Output (slew limited)				22.6	ns
T_{PSUF}	Input Set-up Time (fast)			-4		ns
T_{PSU}	Input Set-up Time with delay			5		ns
T_{PHF}	Input Hold Time (fast)			6.5		ns
T_{PH}	Input Hold Time with delay			-2.5		ns
		Advance				

Notes: All appropriate AC specifications tested using Figure 27 as test load circuit.
These parameters are tested directly and guaranteed over the operating conditions.
As the parameters vary between I/Os, values are given for best and worst I/Os. The parameters for other I/Os will be somewhere between these two extremes. The delay calculator software will calculate the correct value for each I/O used.
All parameters assume the cell register is the closest one to the IOB.

XC6200 IOB Switching Characteristic Guidelines

Speed Grade:		-2				
Symbol	Parameter	Best I/O		Worst I/O		Units
		Min	Max	Min	Max	
	INPUT					
T_{PID}	Pad to Neighbor data				4	ns
T_{PID4}	Pad to L4 Fastlane				5	ns
T_{PDID4}	Pad to L4 Fastlane with delay				13	ns
	OUTPUT					
T_{OPF}	Neighbor data to Output (fast)				4	ns
T_{OPS}	Neighbor data to Output (slew rate limited)				8	ns
T_{TSHZ}	3-state to Pad begin hi-Z (slew rate independent)				5	ns
T_{TSONF}	3-state to Pad active and valid (fast)				5.2	ns
T_{TSONS}	3-state to Pad active and valid (slew rate limited)				9	ns
		Advance				

Notes: As the parameters vary between I/Os, values are given for best and worst I/Os. The parameters for other I/Os will be somewhere between these two extremes. The delay calculator software will calculate the correct value for each I/O used.
Typical loading values are used.

XC6200 Internal Routing Delays

Symbol	Parameter	Speed Grade: -2 Min	Max	Units
T_{FN}	Function Output to Neighbor		1	ns
T_{NN}	Route Neighbor In to Neighbor Out		1.5	ns
T_{Magic}	Route X2/X3 to Magic Out		2.5	ns
T_{L4}	Length-4 Fastlane delay		2	ns
T_{L16}	Length-16 Fastlane delay		2.5	ns
T_{L64}	Chip-Length Fastlane delay		5	ns
		Advance		

Notes: Delays vary depending on direction. Worst case figures are given here. The delay calculator software will calculate the correct delay for each direction.
Typical loading values are used.

XC6200 CPU Interface Timing

	Symbol	Parameter	Speed Grade: -2 Min	Max	Units
1	$T_{su\overline{CS}}$	$\overline{CS}$ set up before Clock[1]	6		ns
2	$T_{h\overline{CS}}$	$\overline{CS}$ hold after Clock[1]	0		ns
3	$T_{suRd\overline{Wr}}$	Rd$\overline{Wr}$ set up before Clock	6		ns
4	$T_{hRd\overline{Wr}}$	Rd$\overline{Wr}$ hold after Clock	0		ns
5	T_{suA}	Address Bus set up before Clock	6		ns
6	T_{hA}	Address Bus hold after Clock	0		ns
7	T_{suD}	Data Bus set up before Clock	6		ns
8	T_{hD}	Data Bus hold after Clock	0		ns
9	T_{WC}	Write cycle time[2]	40		ns
10	T_{RC}	Read cycle time[2]	40		ns
11	T_{CKD}	Clock to Valid Data		8	ns
12	T_{CKDZ}	Clock to Data high impedance[3]		9	ns
13	$T_{\overline{CS}DZ}$	$\overline{CS}$ to Data high impedance[3]		9	ns
			Advance		

Notes:
1. $\overline{CS}$ must be correctly sampled as a '0' at the start of the cycle (t_1) and sampled as a '1' at the end of the cycle (t_2). Other signals only require to be correctly sampled at t_1.
2. The minimum time for a read or write cycle is two CPU clock periods, although the cycles shown do not start and finish at the start of a clock period.
3. Data is removed from the bus T_{CKDZ} after t_3 unless $\overline{CS}$ is still asserted at this time. In this case, data is removed from the bus asynchronously $T_{\overline{CS}DZ}$ after $\overline{CS}$ goes high.

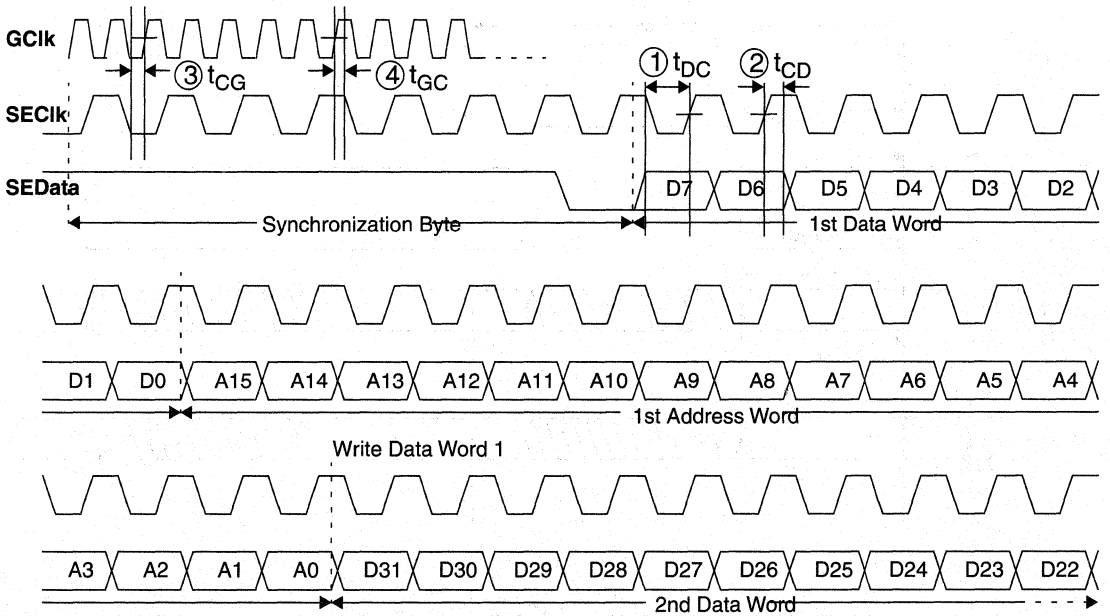


Figure 26: Serial Configuration Timing

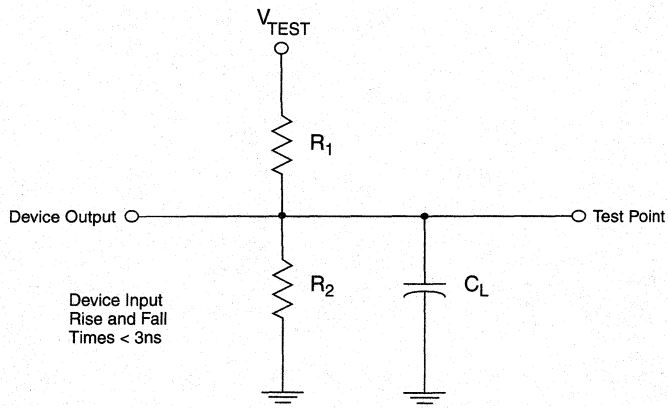


Figure 27: AC Load Circuit

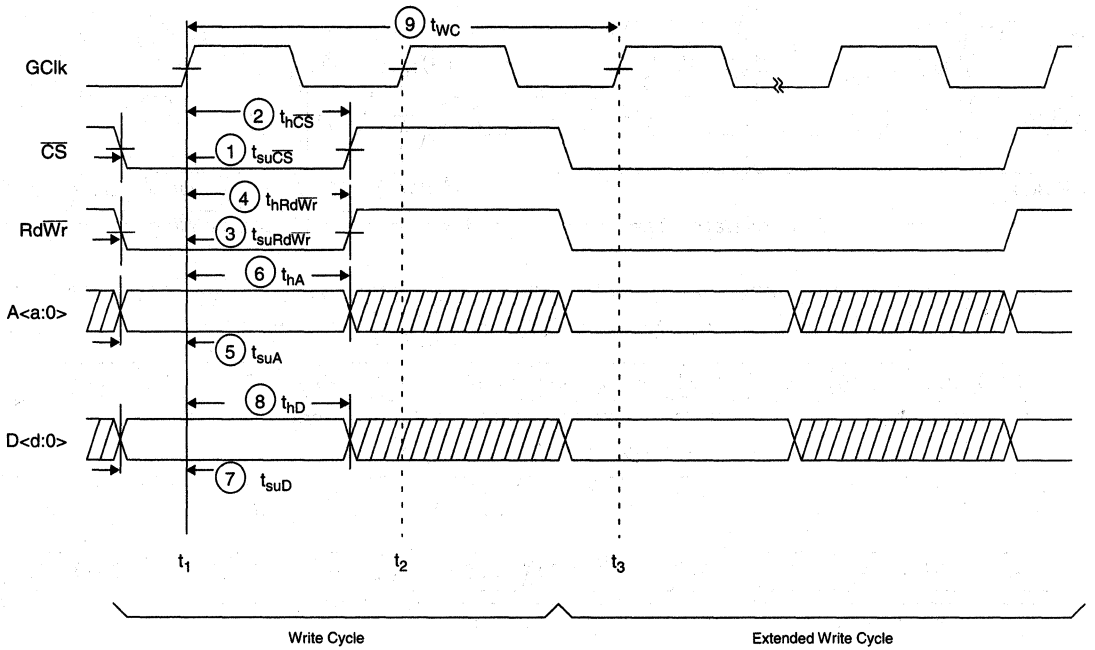


Figure 28: Configuration Memory Write Cycles

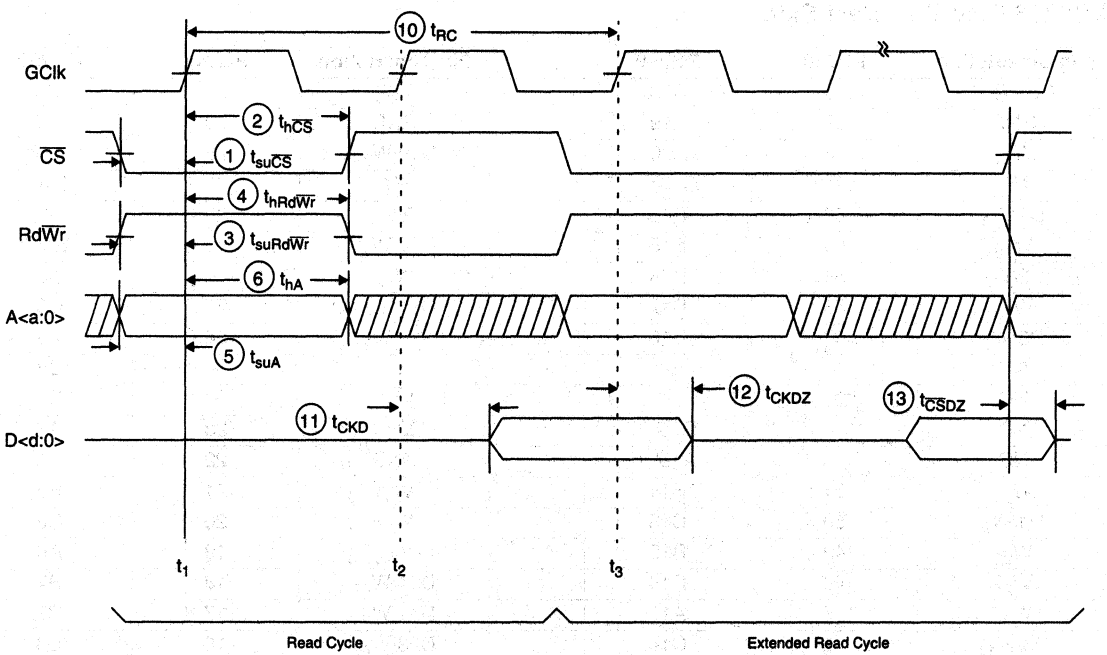


Figure 29: Configuration Memory Read Cycles

XC6200 Pinout Tables

XC6216 Pinouts - West Side

Pin Description	PQ240	PG299		Pin Description	PQ240	PG299
$D0/W_1$[2]	60	C18		V_{CC}	30	A11
GND	59	A19		GND	29	A10
W_{14}	58	A20		$D19/W_{39}$	28	C10
NC	57[1]	C17[1]		W_{40}	-	D10
$D1/W_3$	56	D16		$D9/W_{19}$	27	A9
W_{16}	55	E15		$D20/W_{41}$	26	E10
$D2/W_5$	54	B18		W_{42}	-	B9
W_{18}	53	B17		$D21/W_{43}$	25	C9
$D3/W_7$	52	C16		$D10/W_{21}$	24	A8
NC	-	-		W_{44}	-	B8
NC	-	-		W_{46}	-	D9
NC	-	D15[1]		$D22/W_{45}$	23	A7
NC	-	A18[1]		GND	22	-
W_{20}	51	E14		W_{48}	21	E9
$D4/W_9$	50	C15		W_{50}	20	C8
W_{22}	49	B16		V_{CC}	19	A6
W_{24}	48	D14		$D24/W_{49}$	18	B7
W_{26}	47	A17		$D11/W_{23}$	17	C7
$D5/W_{11}$	46	C14		$D23/W_{47}$	16	D8
NC	-	E13[1]		$D25/W_{51}$	15	B6
NC	-	B15[1]		GND	14	A5
GND	45	A15		W_{52}	-	B5
W_{28}	44	D13		W_{54}	-	E8
W_{30}	43	B14		W_{56}	13	C6
W_{32}	42	C13		$D12/W_{25}$	12	D7
$D6/W_{13}$	41	A14		W_{58}	11	A4
V_{CC}	40	A16		$D26/W_{53}$	10	C5
$D16/W_{33}$	39	B13		$D27/W_{55}$	9	B4
W_{34}	38	E12		$D13/W_{27}$	8	E7
GND	37	-		W_{60}	-	D6
NC	-	D12[1]		W_{62}	-	A3
NC	-	C12[1]		NC	-	-
NC	-	A13[1]		NC	-	-
NC	-	B12[1]		$D28/W_{57}$	7	C4
$D7/W_{15}$	36	A12		$D14/W_{29}$	6	D5
$D17/W_{35}$	35	D11		$D29/W_{59}$	5	E6
W_{36}	34	E11		$D15/W_{31}$	4	B3
$D18/W_{37}$	33	C11		$D30/W_{61}$	3	B2
$D8/W_{17}$	32	B11		$D31/W_{63}$	2	D4
W_{38}	31	B10		GND	1	B1

Notes: 1. Pin not connected.
2. Pins with a dual function have the 'Control' signal shown first. See section "Input/Output Blocks (IOBs)" on page 261 for details.

XC6216 Pinouts - South Side

Pin Description	PQ240	PG299		Pin Description	PQ240	PG299
V_{CC}	61	B20		GND	91	K20
$RdWr/S_1$	62	D17		$G1/S_{17}$	92	L19
CS/S_3	63	B19		$G2/S_{19}$	93	L18
W_{12}/S_0	64	C19		S_{42}	94	L16
$\overline{OE}/S_5$	65	F16		S_{41}	95	L17
W_{10}/S_2	66	E17		S_{44}	-	M20
$\overline{Reset}/S_7$	67	D18		S_{43}	-	M19
W_8/S_4	68	C20		S_{46}	-	N20
NC	-	-		S_{48}	-	M18
NC	-	-		E_0/S_{50}	96	M17
W_6/S_6	69	F17		E_2/S_{52}	97	M16
W_4/S_8	70	G16		GND	98	-
W_2/S_{10}	71	D19		E_4/S_{54}	99	N19
W_0/S_{12}	72	E18		S_{45}	100	P20
S_{14}	73	D20		V_{CC}	101	T20
S_{16}	74	G17		S_{21}	102	N18
S_{18}	-	F18		$SEData/S_{23}$	103	P19
S_{20}	-	H16		E_6/S_{56}	104	N17
S_{22}	-	E19		S_{47}	105	R19
S_{24}	-	F19		GND	106	R20
GND	75	E20		NC	-	N16[1]
S_{26}	76	H17		NC	-	P18[1]
S_{33}	77	G18		E_8/S_{58}	107	U20
$\overline{Serial}/S_9$	78	G19		S_{49}	108	P17
$Wait/S_{11}$	79	H18		S_{51}	109	T19
V_{CC}	80	F20		S_{53}	110	R18
S_{28}	81	J16		S_{55}	-	P16
S_{35}	82	G20		S_{57}	-	V20
GND	83	-		E_{10}/S_{60}	111	R17
S_{30}	-	J17		E_{12}/S_{62}	112	T18
S_{32}	-	H19		NC	-	-
S_{34}	-	H20		NC	-	-
S_{36}	-	J18		$\overline{SECE}/S_{25}$	113	U19
$GClk/S_{13}$	84	J19		$SEReset/S_{27}$	114	V19
S_{38}	85	K16		S_{59}	115	R16
$GClr/S_{15}$	86	J20		S_{61}	116	T17
S_{37}	87	K17		$SEClk/S_{29}$	117	U18
S_{40}	88	K18		$ConfigOK/S_{31}$	118	X20
S_{39}	89	K19		GND	119	W20
V_{CC}	90	L20		S_{63}	120	V18

Note: 1. Pin not connected.

XC6216 Pinouts - East Side

Pin Description	PQ240	PG299		Pin Description	PQ240	PG299
V_{CC}	121	X19		GND	151	X11
E_{14}	122	U17		$A8/E_{17}$	152	W10
$A0/E_{1}$	123	W19		E_{40}	153	V10
E_{16}	124	W18		$A9/E_{19}$	154	T10
$A1/E_{3}$	125	T15		E_{41}	155	U10
E_{18}	126	U16		E_{42}	156	X9
$A2/E_{5}$	127	V17		E_{43}	157	W9
E_{20}	128	X18		NC	-	X8[1]
NC	-	U15[1]		E_{44}	-	V9
NC	-	T14[1]		E_{46}	-	U9
NC	-	-		E_{48}	-	T9
NC	-	-		GND	158	-
$A3/E_{7}$	129	W17		$A10/E_{21}$	159	W8
E_{22}	130	V16		E_{50}	160	X7
E_{24}	131	X17		V_{CC}	161	X5
E_{26}	132	U14		E_{45}	162	V8
$A4/E_{9}$	133	V15		E_{52}	163	W7
E_{28}	134	T13		$A11/E_{23}$	164	U8
NC	-	W16[1]		E_{47}	165	W6
NC	-	W15[1]		GND	166	X6
GND	135	X16		E_{54}	-	T8
E_{30}	136	U13		E_{56}	-	V7
E_{32}	137	V14		E_{58}	167	X4
$A5/E_{11}$	138	W14		E_{49}	168	U7
E_{33}	139	V13		$A12/E_{25}$	169	W5
V_{CC}	140	X15		E_{51}	170	V6
E_{34}	141	T12		E_{53}	171	T7
E_{35}	142	X14		E_{55}	172	X3
GND	143	-		NC	-	-
NC	-	U12		NC	-	-
NC	-	W13		$A13/E_{27}$	173	U6
NC	-	X13		E_{57}	174	V5
NC	-	V12		E_{60}	-	W4
$A6/E_{13}$	144	W12		E_{62}	-	W3
E_{36}	145	T11		$A14/E_{29}$	175	T6
E_{37}	146	X12		E_{59}	176	U5
E_{38}	147	U11		$A15/E_{31}$	177	V4
$A7/E_{15}$	148	V11		E_{61}	178	X1
E_{39}	149	W11		E_{63}	179	V3
V_{CC}	150	X10		V_{CC}	180	W1

Note: 1. Pin not connected.

XC6216 Pinouts - North Side

Pin Description	PQ240	PG299		Pin Description	PQ240	PG299
V_{CC}	240	A2		GND	211	L1
NC	-	-		N_{15}	210	L2
N_1	239	C3		N_{17}	209	L3
N_3	238	D3		N_{19}	208	L4
N_0	237	E4		N_{42}	207	M1
N_2	236	F5		N_{41}	206	L5
N_4	235	C2		N_{44}	205	M2
N_6	234	D2		GND	204	-
N_8	-	E3		N_{43}	203	M3
N_{10}	-	F4		N_{21}	202	N1
NC	-	-		N_{46}	-	N2
NC	-	-		N_{48}	-	M4
N_5	233	C1		N_{50}	-	P1
N_7	232	G5		N_{52}	-	M5
N_{12}	231	F3		V_{CC}	201	R1
N_{14}	230	E2		N_{23}	200	N3
N_{16}	229	G4		N_{54}	199	P2
N_{18}	228	D1		N_{45}	198	P3
N_{20}	-	G3		N_{56}	197	N4
N_{22}	-	H5		GND	196	T1
GND	227	F1		NC	-	R2[1]
N_{24}	226	F2		N_{47}	195	T2
N_{26}	225	H4		N_{58}	194	N5
N_{33}	224	G2		N_{49}	193	R3
N_{28}	223	H3		N_{51}	192	P4
V_{CC}	222	E1		N_{53}	191	U1
N_{30}	-	G1		N_{55}	190	T3
N_{32}	-	H2		N_{57}	189	U2
N_{34}	-	J5		N_{60}	-	P5
N_{36}	-	J4		N_{62}	-	R4
N_{35}	221	J3		NC	-	-
N_9	220	H1		NC	-	-
GND	219	-		N_{59}	188	V1
N_{11}	218	J2		N_{25}	187	U3
N_{38}	217	J1		N_{27}	186	T4
N_{37}	216	K4		N_{61}	185	R5
N_{40}	215	K5		N_{63}	184	V2
N_{39}	214	K3		N_{29}	183	W2
N_{13}	213	K2		GND	182	X2
V_{CC}	212	K1		N_{31}	181	U4

Note: 1. Pin not connected.

Product Availability

Devices are available in small and large packages. The small packages are useful where board area is at a premium and the design can make use of the wireless I/O parallel CPU interface to determine the state of internal nodes. The large package options give a very high user programmable I/O count where this is a prime requirement. The available packaging options for the XC6216 are summarized in Table 6. (These options are advance information and subject to change. Please confirm availability with Xilinx.

Signal pins are all the non-supply pins that drive into the array or control circuitry. Some of these pins are shared between control signals and user I/O. The un-shared user I/Os do not share a pin with a control signal. The number of user I/Os available will be somewhere between the number of signal pins and the number of un-shared I/Os, depending on how many of the FPGA control signals are actually required. For example, if only an 8-bit data bus and no serial interface were required, the number of user I/Os would go up by 24+6=30 in a PGA299 package.

Table 6: XC6216 Package Options

Package	Pins	Signal Pins	Max Data Bus Pins	Unshared User I/O
PLCC	84	68	16	22
PQFP	240	199	32	137
PGA	299	242	32	180

XC3000 Series Field Programmable Gate Arrays

XC3000A Field Programmable Gate Arrays

XC3000L Field Programmable Gate Arrays

XC3100A Field Programmable Gate Arrays

XC3100L Field Programmable Gate Arrays

XC3000 Series
Field Programmable Gate Arrays

June 1, 1996 (Version 2.0)

Product Description

Features

- Complete line of four related Field Programmable Gate Array product families
  - XC3000A, XC3000L, XC3100A, XC3100L
- Ideal for a wide range of custom VLSI design tasks
  - Replaces TTL, MSI, and other PLD logic
  - Integrates complete sub-systems into a single package
  - Avoids the NRE, time delay, and risk of conventional masked gate arrays
- High-performance CMOS static memory technology
  - Guaranteed toggle rates of 70 to 370 MHz, logic delays from 9 to 1.5 ns
  - System clock speeds over 80 MHz
  - Low quiescent and active power consumption
- Flexible FPGA architecture
  - Compatible arrays ranging from 1,000 to 7,500 gate complexity
  - Extensive register, combinatorial, and I/O capabilities
  - High fan-out signal distribution, low-skew clock nets
  - Internal 3-state bus capabilities
  - TTL or CMOS input thresholds
  - On-chip crystal oscillator amplifier
- Unlimited reprogrammability
  - Easy design iteration
  - In-system logic changes
- Extensive packaging options
  - Over 20 different packages
  - Plastic and ceramic surface-mount and pin-grid-array packages
  - Thin and Very Thin Quad Flat Pack (TQFP and VQFP) options
- Ready for volume production
  - Standard, off-the-shelf product availability
  - 100% factory pre-tested devices
  - Excellent reliability record
- Complete XACT*step* Development System
  - Schematic capture, automatic place and route
  - Logic and timing simulation
  - Interactive design editor for design optimization
  - Timing calculator
  - Interfaces to popular design environments like Viewlogic, Cadence, Mentor Graphics, and others

Description

XC3000-Series Field Programmable Gate Arrays (FPGAs) provide a group of high-performance, high-density, digital integrated circuits. Their regular, extendable, flexible, user-programmable array architecture is composed of a configuration program store plus three types of configurable elements: a perimeter of I/O Blocks (IOBs), a core array of Configurable Logic Bocks (CLBs) and resources for interconnection. The general structure of an FPGA is shown in Figure 2. The XACT*step* development system provides schematic capture and auto place-and-route for design entry. Logic and timing simulation, and in-circuit emulation are available as design verification alternatives. The design editor is used for interactive design optimization, and to compile the data pattern that represents the configuration program.

The FPGA user logic functions and interconnections are determined by the configuration program data stored in internal static memory cells. The program can be loaded in any of several modes to accommodate various system requirements. The program data resides externally in an EEPROM, EPROM or ROM on the application circuit board, or on a floppy disk or hard disk. On-chip initialization logic provides for optional automatic loading of program data at power-up. The companion XC17XX Serial Configuration PROMs provide a very simple serial configuration program storage in a one-time programmable package.

The XC3000 Field Programmable Gate Array families provide a variety of logic capacities, package styles, temperature ranges and speed grades.

Device	Max Logic Gates	Typical Gate Range	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3020A, 3020L, 3120A	1,500	1,000 - 1,500	64	8 x 8	64	256	16	14,779
XC3030A, 3030L, 3130A	2,000	1,500 - 2,000	100	10 x 10	80	360	20	22,176
XC3042A, 3042L, 3142A, 3142L	3,000	2,000 - 3,000	144	12 x 12	96	480	24	30,784
XC3064A, 3064L, 3164A	4,500	3,500 - 4,500	224	16 x 14	120	688	32	46,064
XC3090A, 3090L, 3190A, 3190L	6,000	5,000 - 6,000	320	16 x 20	144	928	40	64,160
XC3195A	7,500	6,500 - 7,500	484	22 x 22	176	1,320	44	94,984

XC3000 Series Overview

Introduced in 1987/88, the XC3000 series is the industry's most successful family of FPGAs, with over 10 million devices shipped. In 1992/93, Xilinx introduced three additional families, offering more speed, functionality, and a new supply-voltage option.

There are now four distinct family groupings within the XC3000 Series of FPGA devices, with emphasis on those listed below:

- XC3000A Family
- XC3000L Family
- XC3100A Family
- XC3100L Family

All six families share a common architecture, development software, design and programming methodology, and also common package pin-outs. An extensive Product Description covers these common aspects.

The much shorter individual Product Specifications then provide detailed parametric information for the XC3000A, XC3000L, XC3100A, and XC3100L product families. (The XC3000 and XC3100 families are not recommended for new designs, and their individual product specifications are not included in this book.)

Here is a simple overview of those XC3000 products currently emphasized:

- **XC3000A Family** — The XC3000A is an enhanced version of the basic XC3000 family, featuring additional interconnect resources and other user-friendly enhancements. The ease-of-use of the XC3000A family makes it the obvious choice for all new designs that do not require the speed of the XC3100A or the 3-V operation of the XC3000L.
- **XC3000L Family** — The XC3000L is identical in architecture and features to the XC3000A family, but operates at a nominal supply voltage of 3.3 V. The XC3000L is the right solution for battery-operated and low-power applications.
- **XC3100A Family** — The XC3100A is a performance-optimized relative of the XC3000A family. While both families are bitstream and footprint compatible, the XC3100A family extends toggle rates to 370 MHz and in-system performance to over 80 MHz. The XC3100A family also offers one additional array size, the XC3195A. The XC3100A is best suited for designs that require the highest clock speed or the shortest net delays.
- **XC3100L Family** — The XC3100L is identical in architectures and features to the XC3100A family, but operates at a nominal supply voltage of 3.3V.

Figure 1 illustrates the relationships between the families. Compared to the original XC3000 family, XC3000A offers additional functionality and, coming soon, increased speed. The XC3000L family offers the same additional functionality, but reduced speed due to its lower supply voltage of 3.3 V. The XC3100A family offers substantially higher speed and higher density with the XC3195A.

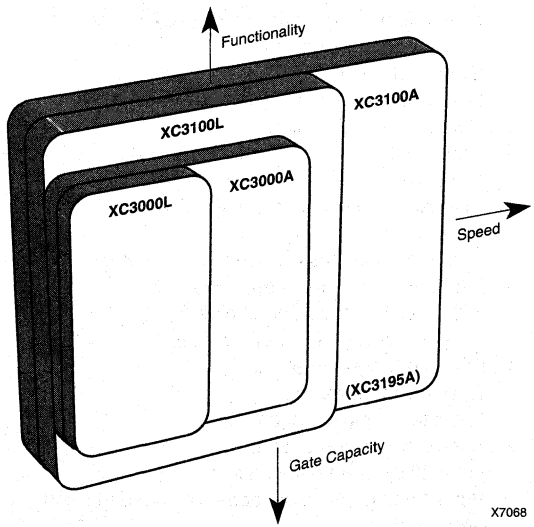


Figure 1: XC3000 FPGA Families

Detailed Functional Description

The perimeter of configurable Input/Output Blocks (IOBs) provides a programmable interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed circuit board traces connecting MSI/SSI packages.

The block logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass transistors.

These FPGA functions are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the device at power-up and may be reloaded on command. The FPGA includes logic and control signals to implement automatic or passive configuration. Program data may be either bit serial or byte parallel. The XACT*step* development system generates the configuration program bitstream used to configure the device. The memory loading process is independent of the user logic functions.

Configuration Memory

The static memory cell used for the configuration memory in the Field Programmable Gate Array has been designed specifically for high reliability and noise immunity. Integrity of the device configuration memory based on this design is assured even under adverse conditions. As shown in Figure 3, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the cell provides continuous control and the pass transistor is off and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and rewritten.

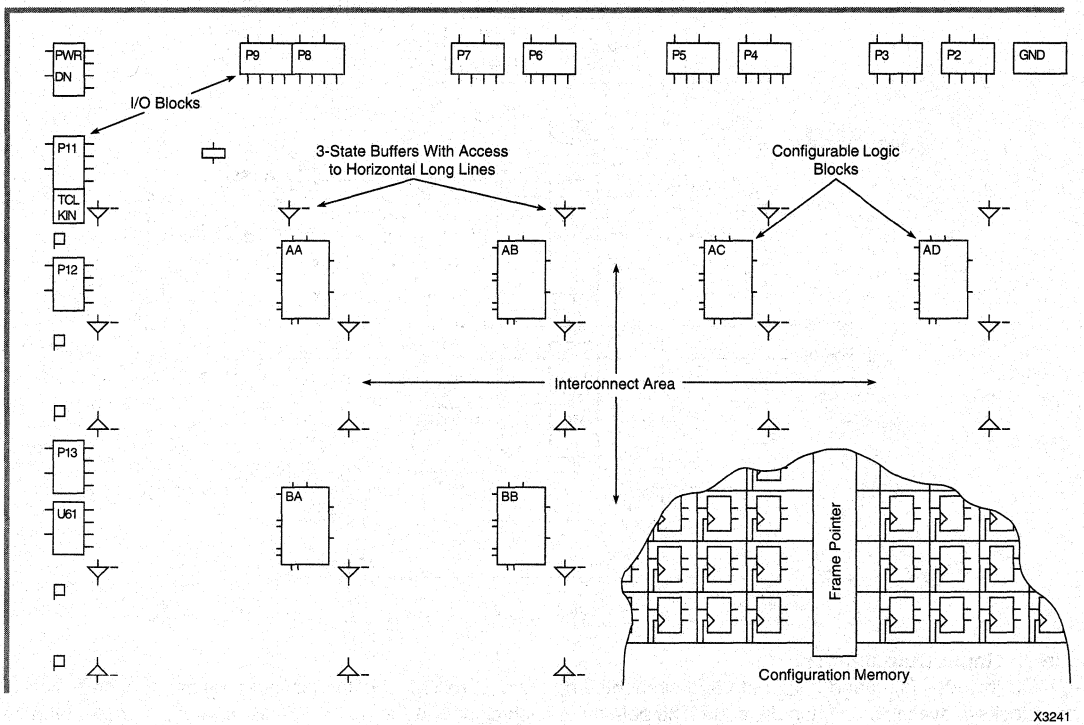


Figure 2: Field Programmable Gate Array Structure.
It consists of a perimeter of programmable I/O blocks, a core of configurable logic blocks and their interconnect resources. These are all controlled by the distributed array of configuration program memory cells.

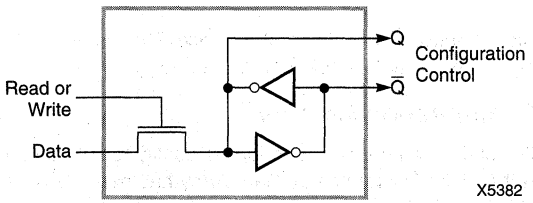


Figure 3: Static Configuration Memory Cell.
It is loaded with one bit of configuration program and controls one program selection in the Field Programmable Gate Array.

The memory cell outputs Q and $\overline{Q}$ use ground and V_{CC} levels and provide continuous, direct control. The additional capacitive load together with the absence of address decoding and sense amplifiers provide high stability to the cell. Due to the structure of the configuration memory cells, they are not affected by extreme power-supply excursions or very high levels of alpha particle radiation. In reliability testing, no soft errors have been observed even in the presence of very high doses of alpha radiation.

The method of loading the configuration data is selectable. Two methods use serial data, while three use byte-wide data. The internal configuration logic utilizes framing information, embedded in the program data by the XACT*step* development system, to direct memory-cell loading. The serial-data framing and length-count preamble provide programming compatibility for mixes of various FPGA device devices in a synchronous, serial, daisy-chain fashion.

I/O Block

Each user-configurable IOB shown in Figure 4, provides an interface between the external package pin of the device and the internal user logic. Each IOB includes both registered and direct input paths. Each IOB provides a programmable 3-state output buffer, which may be driven by a registered or direct output signal. Configuration options allow each IOB an inversion, a controlled slew rate and a high impedance pull-up. Each input circuit also provides input clamping diodes to provide electrostatic protection, and circuits to inhibit latch-up produced by input currents.

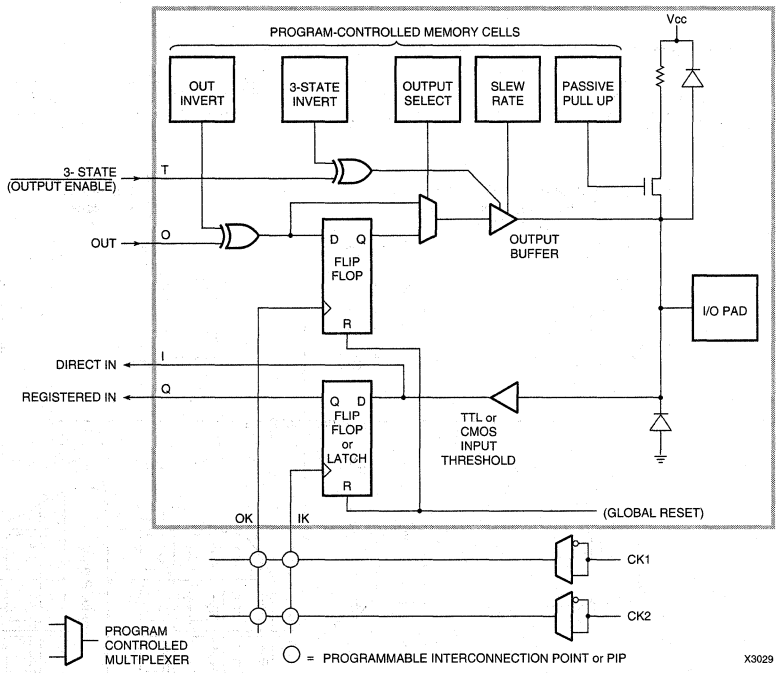


Figure 4: Input/Output Block.
Each IOB includes input and output storage elements and I/O options selected by configuration memory cells. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active Low Latch Enable (Latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are programmed for TTL or CMOS thresholds.

The input-buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOBs can be programmed to be compatible with either TTL or CMOS levels. The buffered input signal drives the data input of a storage element, which may be configured as either a flip-flop or a latch. The clocking polarity (rising/falling edge-triggered flip-flop, High/Low transparent latch) is programmable for each of the two clock lines on each of the four die edges. Note that a clock line driving a *rising* edge-triggered flip-flop makes any latch driven by the same line on the same edge Low-level transparent and vice versa (*falling* edge, *High* transparent). All Xilinx primitives in the supported schematic-entry packages, however, are positive edge-triggered flip-flops or High transparent latches. When one clock line must drive flip-flops as well as latches, it is necessary to compensate for the difference in clocking polarities with an additional inverter either in the flip-flop clock input or the latch-enable input. I/O storage elements are reset during configuration or by the active-Low chip $\overline{\text{RESET}}$ input. Both direct input (from IOB pin I) and registered input (from IOB pin Q) signals are available for interconnect.

For reliable operation, inputs should have transition times of less than 100 ns and should not be left floating. Floating CMOS input-pin circuits might be at threshold and produce oscillations. This can produce additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces sensitivity to input noise. Each user IOB includes a programmable high-impedance pull-up resistor, which may be selected by the program to provide a constant High for otherwise undriven package pins. Although the Field Programmable Gate Array provides circuitry to provide input protection for electrostatic discharge, normal CMOS handling precautions should be observed.

Flip-flop loop delays for the IOB and logic-block flip-flops are short, providing good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition that can result from assertion of the clock during data transitions. Because of the short-loop-delay characteristic in the Field Programmable Gate Array, the IOB flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the IOB, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing-path delays.

IOB output buffers provide CMOS-compatible 4-mA source-or-sink drive for high fan-out CMOS or TTL- compatible signal levels (8 mA in the XC3100A family). The network driving IOB pin O becomes the registered or direct data source for the output buffer. The 3-state control signal (IOB) pin T can control output activity. An open-drain output may be obtained by using the same signal for driving the output and 3-state signal nets so that the buffer output is enabled only for a Low.

Configuration program bits for each IOB control features such as optional output register, logic signal inversion, and 3-state and slew-rate control of the output.

The program-controlled memory cells of Figure 4 control the following options.

- Logic inversion of the output is controlled by one configuration program bit per IOB.
- Logic 3-state control of each IOB output buffer is determined by the states of configuration program bits that turn the buffer on, or off, or select the output buffer 3-state control interconnection (IOB pin T). When this IOB output control signal is High, a logic one, the buffer is disabled and the package pin is high impedance. When this IOB output control signal is Low, a logic zero, the buffer is enabled and the package pin is active. Inversion of the buffer 3-state control-logic sense (output enable) is controlled by an additional configuration program bit.
- Direct or registered output is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source may be supplied (IOB pin OK) by either of two metal lines available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased output transition speed can be selected to improve critical timing. Slower transitions reduce capacitive-load peak currents of non-critical outputs and minimize system noise.
- An internal high-impedance pull-up resistor (active by default) prevents unconnected inputs from floating.

Summary of I/O Options

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)

Configurable Logic Block

The array of CLBs provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. For example, the XC3020A has 64 such blocks arranged in 8 rows and 8 columns. The XACT*step* development system is used to compile the configuration data which is to be loaded into the internal configuration memory to define the operation and interconnection of each block. User definition of CLBs and their interconnecting networks may be done by automatic translation from a schematic-capture logic diagram or optionally by installing library or user macros.

Each CLB has a combinatorial logic section, two flip-flops, and an internal control section. See Figure 5. There are: five logic inputs (A, B, C, D and E); a common clock input (K); an asynchronous direct RESET input (RD); and an enable clock (EC). All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs (X and Y) which may drive interconnect networks.

Data input for either flip-flop within a CLB is supplied from the function F or G outputs of the combinatorial logic, or the block input, DI. Both flip-flops in each CLB share the asynchronous RD which, when enabled and High, is dominant over clocked inputs. All flip-flops are reset by the active-Low chip input, $\overline{\text{RESET}}$, or during the configuration process. The flip-flops share the enable clock (EC) which, when Low, recirculates the flip-flops' present states and inhibits response to the data-in or combinatorial function inputs on a CLB. The user may enable these control inputs and select their sources. The user may also select the clock net input (K), as well as its active sense within each CLB. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device. Flexible routing allows use of common or individual CLB clocking.

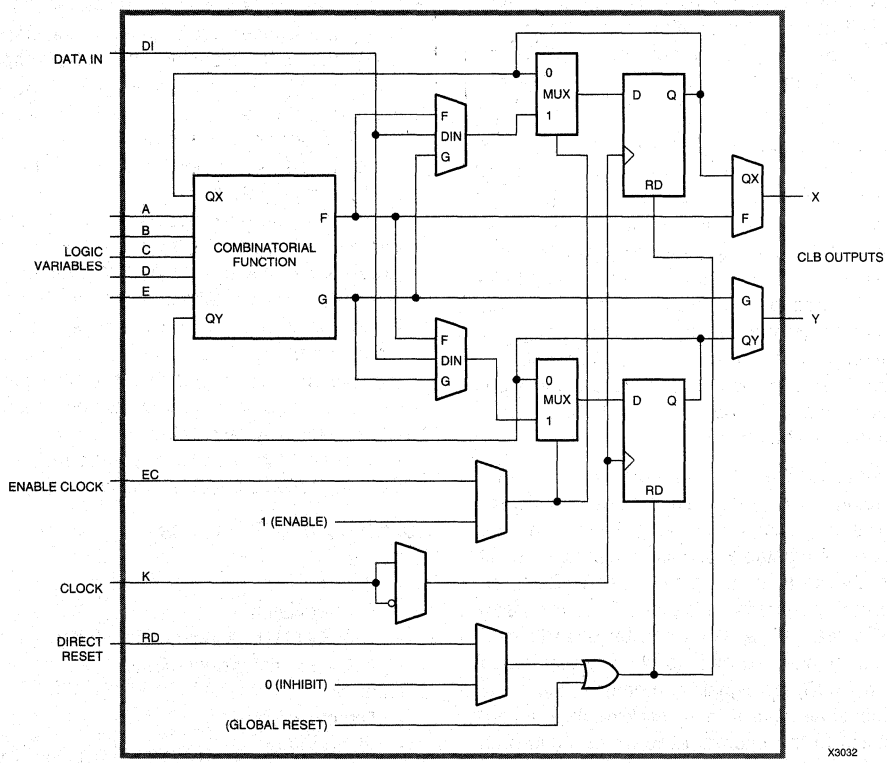


Figure 5: Configurable Logic Block.

Each CLB includes a combinatorial logic section, two flip-flops and a program memory controlled multiplexer selection of function. It has the following:

- five logic variable inputs A, B, C, D, and E
- a direct data in DI
- an enable clock EC
- a clock (invertible) K
- an asynchronous direct RESET RD
- two outputs X and Y

The combinatorial-logic portion of the CLB uses a 32 by 1 look-up table to implement Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinatorial propagation delay through the network is independent of the logic function generated and is spike free for single input variable changes. This technique can generate two independent logic functions of up to four variables each as shown in Figure 6a, or a single function of five variables as shown in Figure 6b, or some functions of seven variables as shown in Figure 6c. Figure 7 shows a modulo-8 binary counter with parallel enable. It uses one CLB of each type. The partial functions of six or seven variables are implemented using the input variable (E) to dynamically select between two functions of four different variables. For the two functions of four variables each, the independent results (F and G) may be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops allows the interchange of CLB outputs to optimize routing efficiencies of the networks interconnecting the CLBs and IOBs.

Programmable Interconnect

Programmable-interconnection resources in the Field Programmable Gate Array provide routing paths to connect inputs and outputs of the IOBs and CLBs into logic networks. Interconnections between blocks are composed of a two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. Figure 8 is an example of a routed net. The XACT*step* development system provides automatic routing of these interconnections. Interactive routing (Editnet) is also available for design optimization. The inputs of the CLBs or IOBs are multiplexers which can be programmed to select an input network from the adjacent interconnect segments. ***Since the switch connections to block inputs are unidirectional, as are block outputs, they are usable only for block input connection and not for routing.*** Figure 9 illustrates routing access to logic block input variables, control inputs and block outputs. Three types of metal resources are provided to accommodate various network interconnect requirements.

- General Purpose Interconnect
- Direct Connection
- Longlines (multiplexed busses and wide AND gates

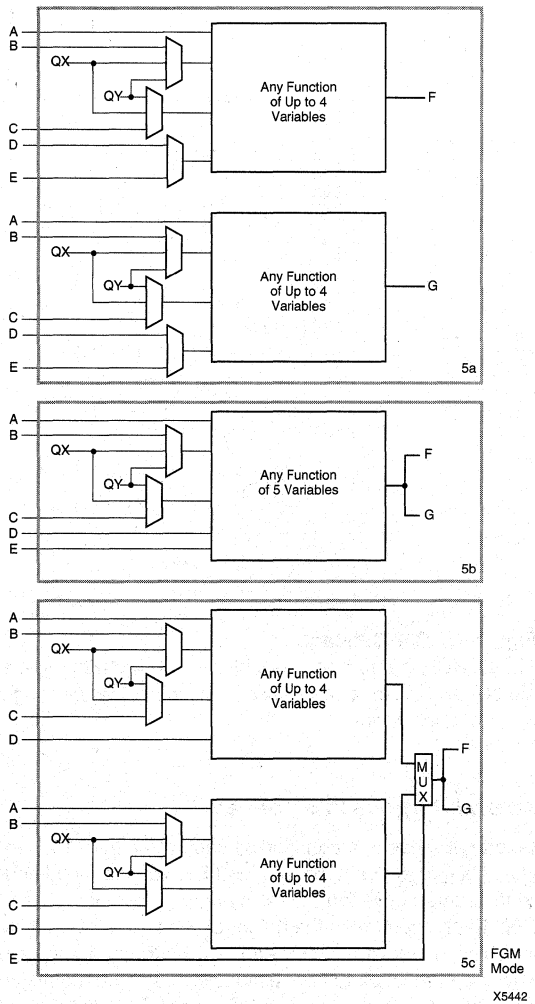


Figure 6: Combinational Logic Options

6a. Combinatorial Logic Option FG generates two functions of four variables each. One variable, A, must be common to both functions. The second and third variable can be any choice of B, C, QX and QY. The fourth variable can be any choice of D or E.

6b. Combinatorial Logic Option F generates any function of five variables: A, D, E and two choices out of B, C, QX, QY.

6c. Combinatorial Logic Option FGM allows variable E to select between two functions of four variables: Both have common inputs A and D and any choice out of B, C, QX and QY for the remaining two variables. Option 3 can then implement some functions of six or seven variables.

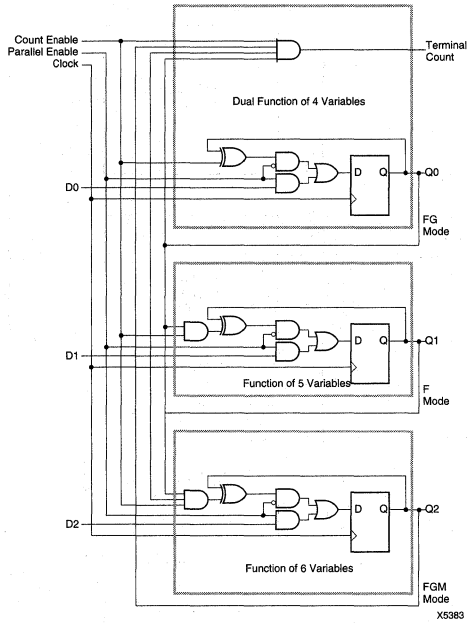


Figure 7: C8BCP Macro.
The C8BCP macro (modulo-8 binary counter with parallel enable and clock enable) uses one combinatorial logic block of each option.

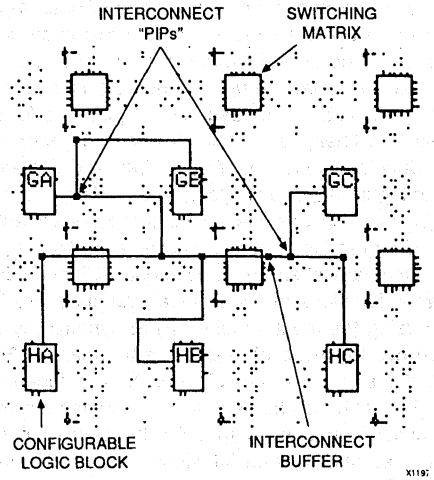


Figure 8: An XACT Design Editor view of routing resources used to form a typical interconnection network from CLB GA.

General Purpose Interconnect

General purpose interconnect, as shown in Figure 10, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and IOBs. Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix may be established by the automatic routing or by using Editnet to select the desired pairs of matrix pins to be connected or disconnected. The legitimate switching matrix combinations for each pin are indicated in Figure 11 and may be highlighted by the use of the Show-Matrix command in the XACT Design Editor.

Special buffers within the general interconnect areas provide periodic signal isolation and restoration for improved performance of lengthy nets. The interconnect buffers are available to propagate signals in either direction on a given general interconnect segment. These bidirectional (bidi) buffers are found adjacent to the switching matrices, above and to the right and may be highlighted by the use of the Show BIDI command in the XACT Design Editor. The other PIPs adjacent to the matrices are accessed to or from Longlines. The development system automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the XACT*step* development system automatically calculates and displays the block, interconnect and buffer delays for any paths selected. Generation of the simulation netlist with a worst-case delay model is provided by an XACT option.

Direct Interconnect

Direct interconnect, shown in Figure 12, provides the most efficient implementation of networks between adjacent CLBs or I/O Blocks. Signals routed from block to block using the direct interconnect exhibit minimum interconnect propagation and use no general interconnect resources. For each CLB, the X output may be connected directly to the B input of the CLB immediately to its right and to the C input of the CLB to its left. The Y output can use direct interconnect to drive the D input of the block immediately above and the A input of the block below. Direct interconnect should be used to maximize the speed of high-performance portions of logic. Where logic blocks are adjacent to IOBs, direct connect is provided alternately to the IOB inputs (I) and outputs (O) on all four edges of the die. The right edge provides additional direct connects from CLB outputs to adjacent IOBs. Direct interconnections of IOBs with CLBs are shown in Figure 13.

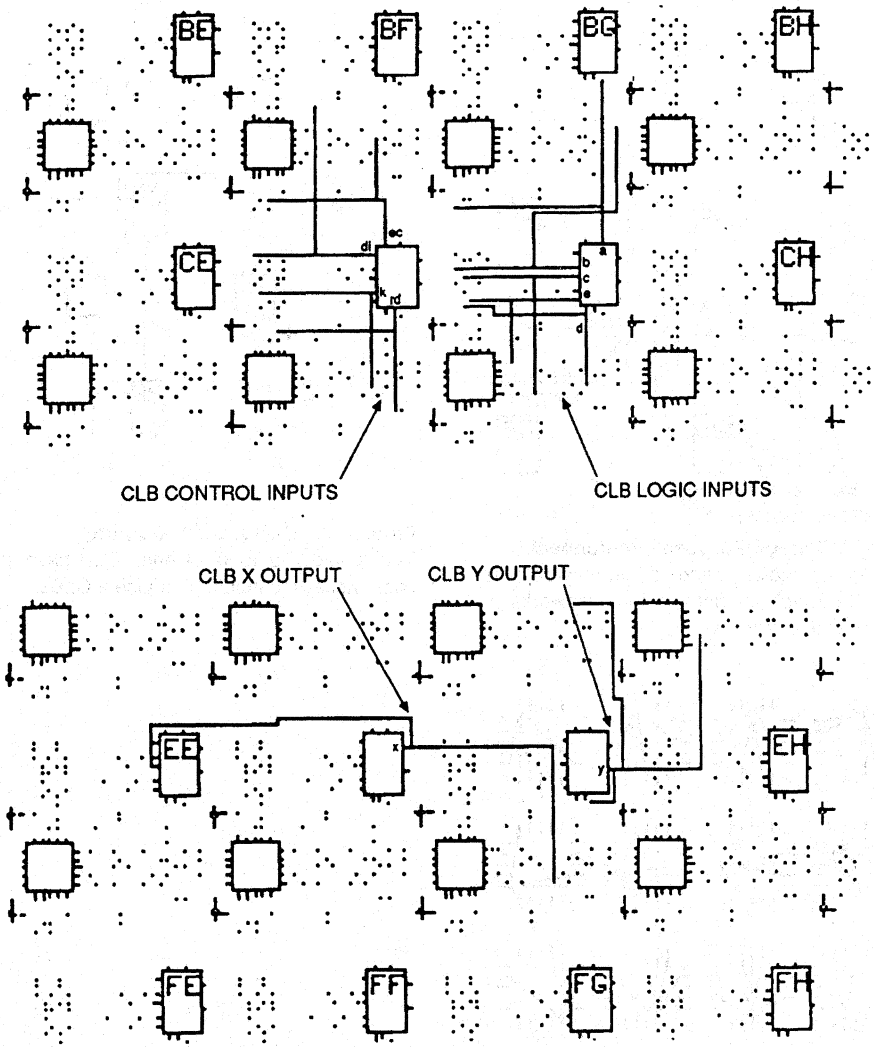


Figure 9: XACT Design Editor Locations of interconnect access, CLB control inputs, logic inputs and outputs. The dot pattern represents the available programmable interconnection points (PIPs).

Some of the interconnect PIPs are directional. This is indicated on the XACT Design Editor status line:

ND is a nondirectional interconnection.
D:H->V is a PIP that drives from a horizontal to a vertical line.
D:V->H is a PIP that drives from a vertical to a horizontal line.
D:C->T is a "T" PIP that drives from a cross of a T to the tail.
D:CW is a corner PIP that drives in the clockwise direction.
P0 indicates the PIP is non-conducting, P1 is on.

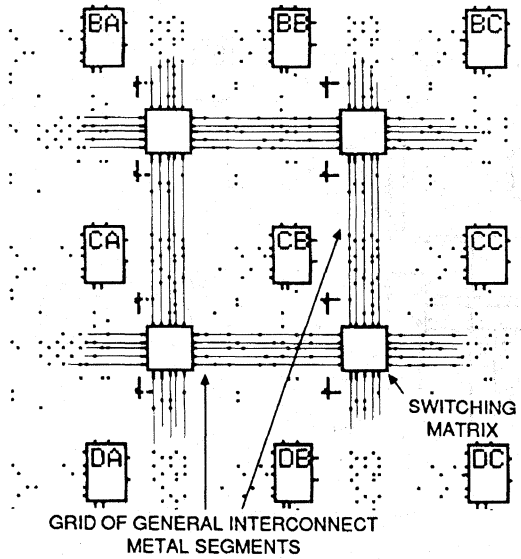


Figure 10: FPGA General-Purpose Interconnect.
Composed of a grid of metal segments that may be interconnected through switch matrices to form networks for CLB and IOB inputs and outputs.

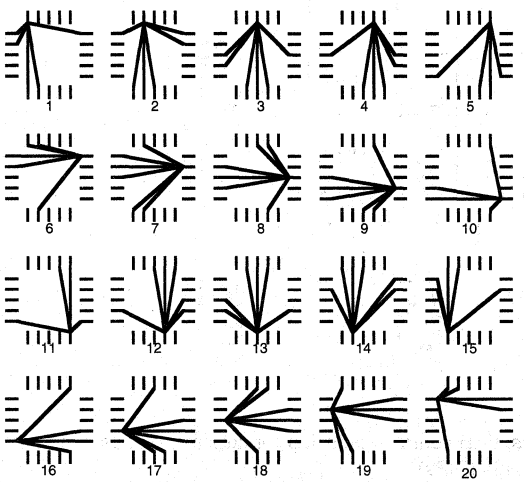


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Figure 11: Switch Matrix Interconnection Options for Each Pin.
Switch matrices on the edges are different. Use Show Matrix menu option in the XACT Design Editor.

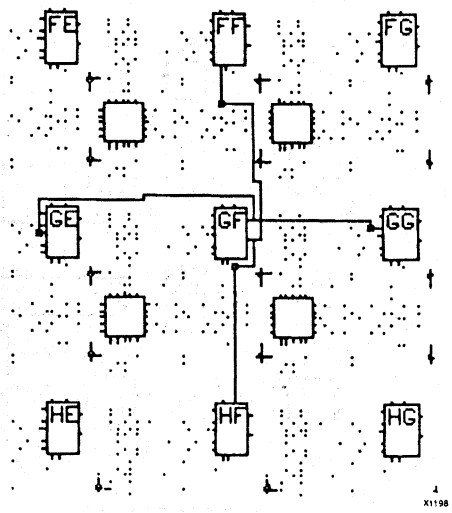


Figure 12: CLB X and Y Outputs.
The X and Y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs

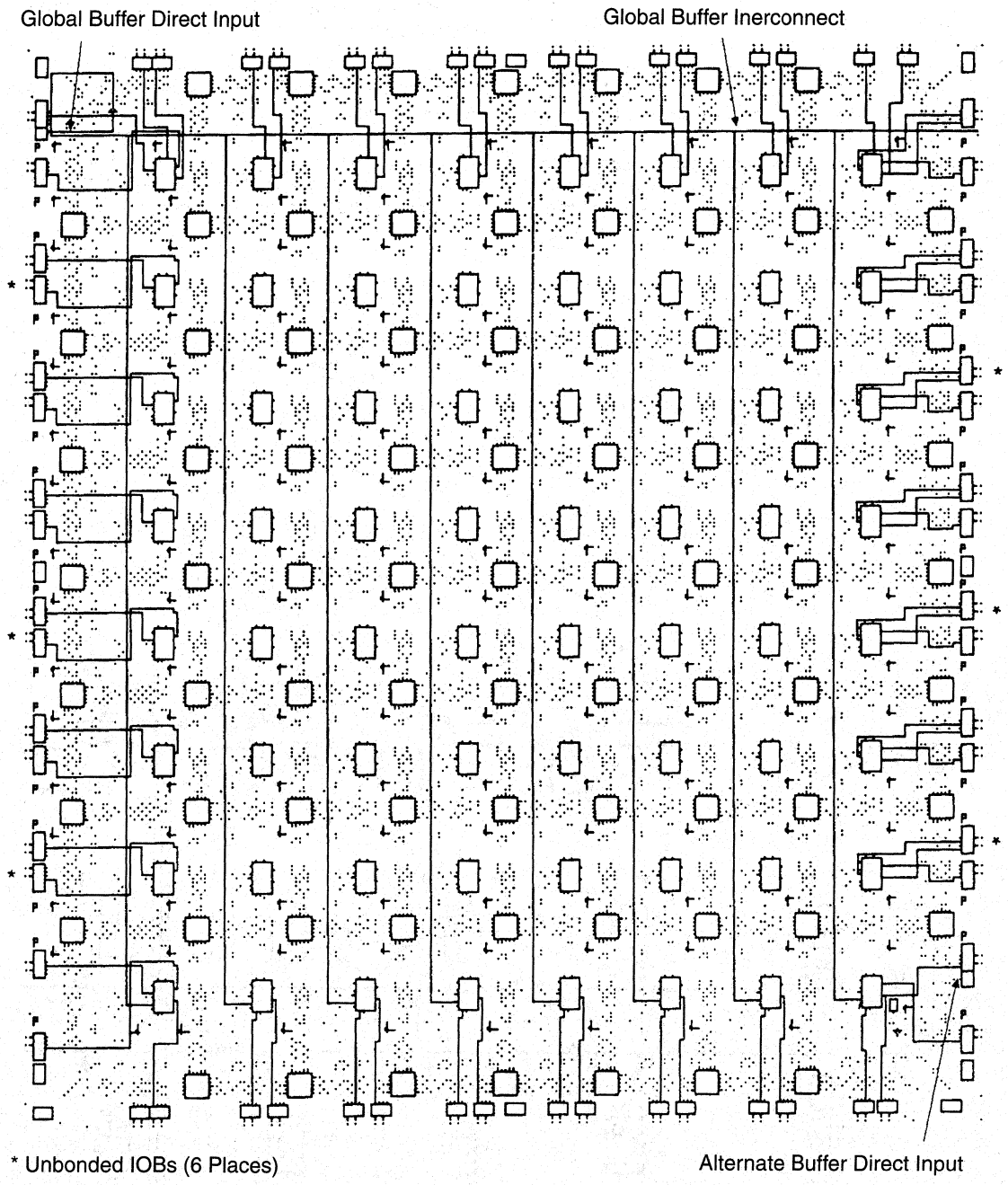


Figure 13: XC3020A Die-Edge IOBs. The XC3020A die-edge IOBs are provided with direct access to adjacent CLBs.

Longlines

The Longlines bypass the switch matrices and are intended primarily for signals that must travel a long distance, or must have minimum skew among multiple destinations. Longlines, shown in Figure 14, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical Longlines, and each interconnection row has two horizontal Longlines. Two additional Longlines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020A, two vertical Longlines in each column are connectable half-length lines. On the XC3020A, only the outer Longlines are connectable half-length lines.

Longlines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these Longlines are shown in Figure 15. Isolation buffers are provided at each input to a Longline and are enabled automatically by the development system when a connection is made.

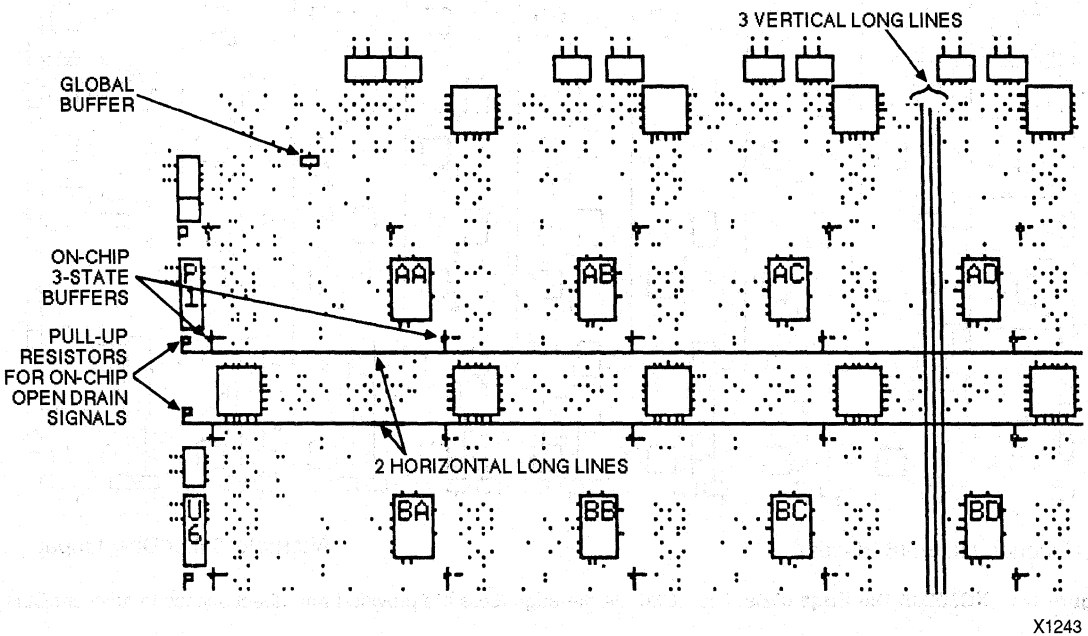


Figure 14: Horizontal and Vertical Longlines. These Longlines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the FPGA.

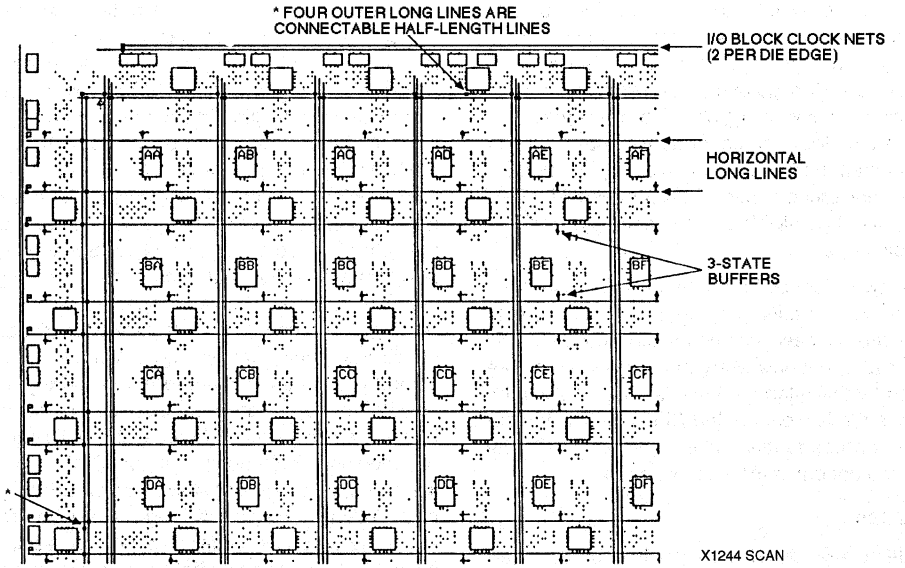


Figure 15: Programmable Interconnection of Longlines. This is provided at the edges of the routing area. Three-state buffers allow the use of horizontal Longlines to form on-chip wired AND and multiplexed buses. The left two non-clock vertical Longlines per column (except XC3020A) and the outer perimeter Longlines may be programmed as connectable half-length lines.

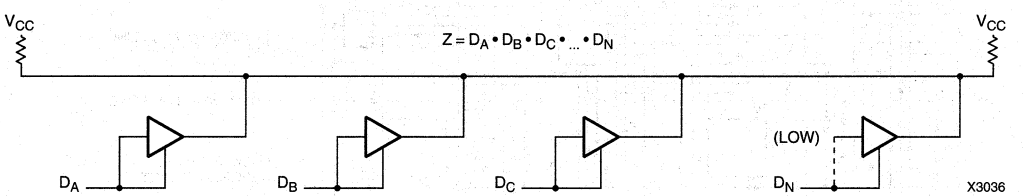


Figure 16: 3-State Buffers Implement a Wired-AND Function. When all the buffer 3-state lines are High, (high impedance), the pull-up resistor(s) provide the High output. The buffer inputs are driven by the control signals or a Low.

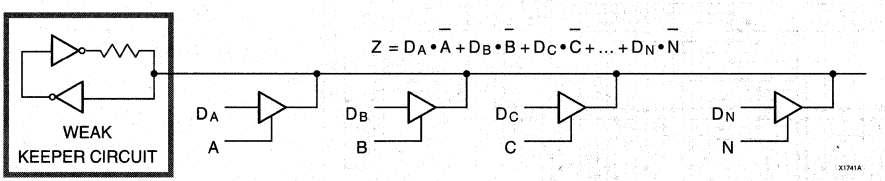


Figure 17: 3-State Buffers Implement a Multiplexer. The selection is accomplished by the buffer 3-state signal.

A buffer in the upper left corner of the FPGA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See Figure 16. The user is required to avoid contention which can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See Figure 17. Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state busses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. Figure 18 shows 3-state buffers, Longlines and pull-up resistors.

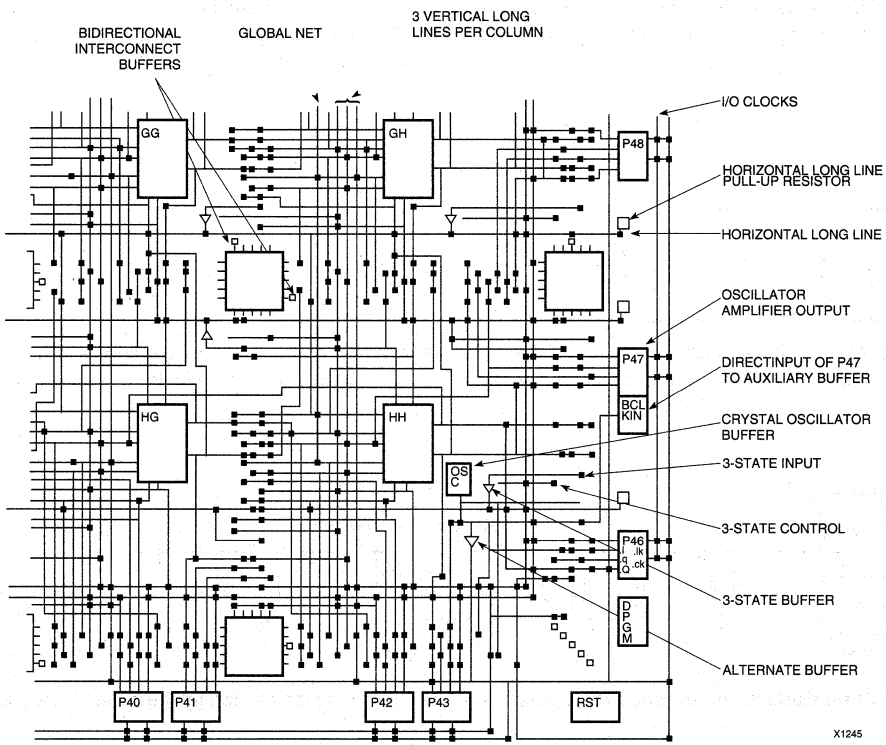
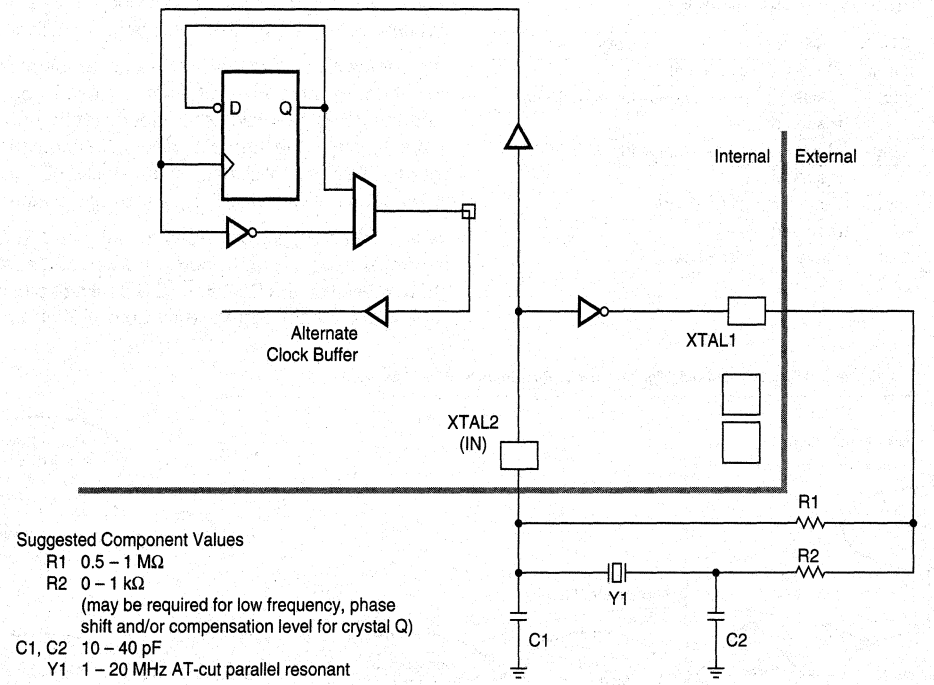


Figure 18: XACT Design Editor.
An extra large view of possible interconnections in the lower right corner of the XC3020A.

Crystal Oscillator

Figure 18 also shows the location of an internal high speed inverting amplifier that may be used to implement an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured by MakeBits and connected as a signal source, two special user IOBs are also configured to connect the oscillator amplifier with external crystal oscillator components as shown in Figure 19. A divide by two option is available to assure symmetry. The oscillator circuit becomes active early in the configuration process to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. In Figure 19 the feedback resistor R1, between the output and input, biases the amplifier at threshold. The inversion of the amplifier, together with the R-C networks and an AT-cut series resonant crystal, produce the 360-degree phase shift of the Pierce oscillator. A series resistor R2 may be included to add to the amplifier output impedance when needed for phase-shift control, crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be corrected by the ratio of C2/C1. The amplifier is designed to be used from 1 MHz to about one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series resistance. Crystal oscillators above 20 MHz generally require a crystal which operates in a third overtone mode, where the fundamental frequency must be suppressed by an inductor across C2, turning this parallel resonant circuit to double the fundamental crystal frequency, i.e., 2/3 of the desired third harmonic frequency network. When the oscillator inverter is not used, these IOBs and their package pins are available for general user I/O.



	44 PIN	68 PIN	84 PIN		100 PIN		132 PIN	160 PIN	164 PIN	175 PIN	176 PIN	208 PIN
	PLCC	PLCC	PLCC	PGA	CQFP	PQFP	PGA	PQFP	CQFP	PGA	TQFP	PQFP
XTAL 1 (OUT)	30	47	57	J11	67	82	P13	82	105	T14	91	110
XTAL 2 (IN)	26	43	53	L11	61	76	M13	76	99	P15	85	100

X7064

Figure 19: Crystal Oscillator Inverter. When activated in the MakeBits program and by selecting an output network for its buffer, the crystal oscillator inverter uses two unconfigured package pins and external components to implement an oscillator. An optional divide-by-two mode is available to assure symmetry.

Configuration

Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the FPGA device begin to operate (nominally 2.5 to 3 V), the programmable I/O output buffers are 3-stated and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time the power-down mode is inhibited. The Initialization state time-out (about 11 to 33 ms) is determined by a 14-bit counter driven by a self-generated internal timer. This nominal 1-MHz timer is subject to variations with process, temperature and power supply. As shown in Table 1, five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

Table 1: Configuration Mode Choices

M0	M1	M2	CCLK	Mode	Data
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	output	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	output	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	input	Slave	Bit Serial

In Master configuration modes, the device becomes the source of the Configuration Clock (CCLK). The beginning of configuration of devices using Peripheral or Slave modes must be delayed long enough for their initialization to be completed. An FPGA with mode lines selecting a Master configuration mode extends its initialization state using four times the delay (43 to 130 ms) to assure that all daisy-chained slave devices, which it may be driving, will be ready even if the master is very fast, and the slave(s) very slow. Figure 20 shows the state sequences. At the end of Initialization, the device enters the Clear state where it clears the configuration memory. The active Low, open-drain initialization signal $\overline{INIT}$ indicates when the Initialization and Clear states are complete. The FPGA tests for the absence of an external active Low $\overline{RESET}$ before it makes a final sample of the mode lines and enters the Configuration state. An external wired-AND of one or more $\overline{INIT}$ pins can be used to control configuration by the assertion of the active-Low $\overline{RESET}$ of a master mode device or to signal a processor that the FPGAs are not yet initialized.

If a configuration has begun, a re-assertion of $\overline{RESET}$ for a minimum of three internal timer cycles will be recognized and the FPGA will initiate an abort, returning to the Clear state to clear the partially loaded configuration memory words. The FPGA will then resample $\overline{RESET}$ and the mode lines before re-entering the Configuration state.

A re-program is initiated.when a configured XC3000 series device senses a High-to-Low transition and subsequent >6 µs Low level on the DONE/$\overline{PROG}$ package pin, or, if this pin is externally held permanently Low, a High-to-Low transi-

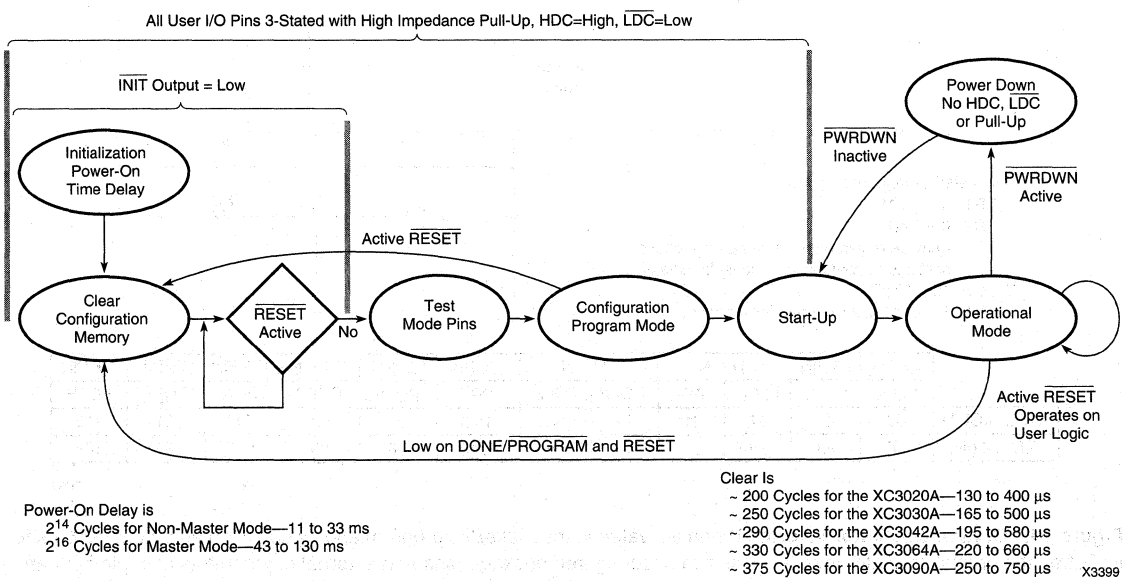
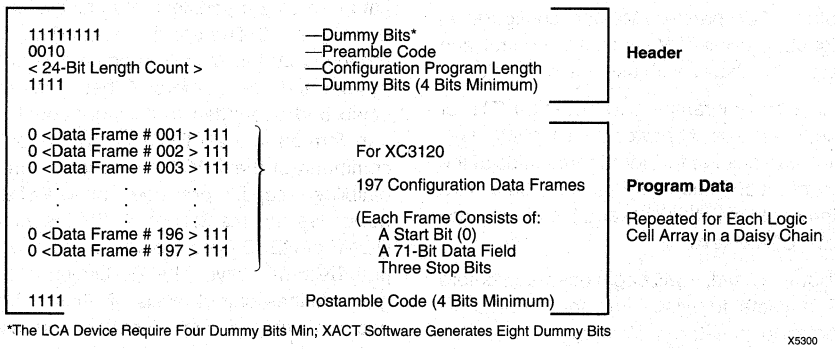


Figure 20: A State Diagram of the Configuration Process for Power-up and Reprogram.

tion and subsequent >6 µs Low time on the $\overline{\text{RESET}}$ package pin.

The device returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Length count control allows a system of multiple Field Programmable Gate Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program generated by the MakePROM program of the *XACTstep* development system begins with a preamble of 111111110010 followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 21. All FPGAs connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. A device which has received the preamble and length count then presents a High Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not yet compare, the device shifts any additional data through, as it did for preamble and length count. When the F{GA configuration memory is full and the length count



Device	XC3020A XC3020L XC3120 XC3120A	XC3030A XC3030L XC3130A	XC3042A XC3042L XC3142A XC3142L	XC3064A XC3064L XC3164A	XC3090A XC3090L XC3190A XC3190L	XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs	64	100	144	224	320	484
Row x Col	(8 x 8)	(10 x 10)	(12 x 12)	(16 x 14)	(20 x 16)	(22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

Figure 21: Internal Configuration Data Structure for an FPGA. This shows the preamble, length count and data frames generated by the XACT*step* Development System.

The Length Count produced by the MakeBits program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] – ($2 \le K \le 4$) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.

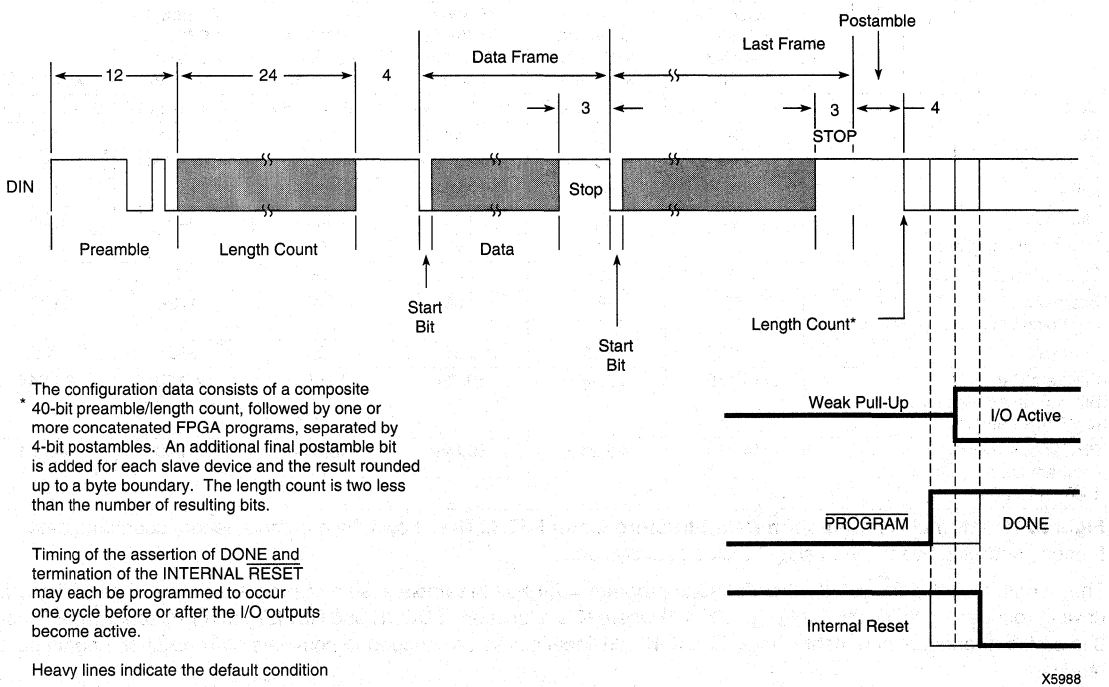
compares, the device will execute a synchronous start-up sequence and become operational. See Figure 22. Two CCLK cycles after the completion of loading configuration data, the user I/O pins are enabled as configured. As selected in MakeBits, the internal user-logic RESET is released either one clock cycle before or after the I/O pins become active. A similar timing selection is programmable for the DONE/$\overline{\text{PROG}}$ output signal. DONE/PROG may also be programmed to be an open drain or include a pull-up resistor to accommodate wired ANDing. The High During Configuration (HDC) and Low During Configuration ($\overline{\text{LDC}}$) are two user I/O pins which are driven active while an FPGA is in its Initialization, Clear or Configure states. They and DONE/$\overline{\text{PROG}}$ provide signals for control of external logic signals such as RESET, bus enable or PROM enable during configuration. For parallel Master configuration modes, these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

User I/O inputs can be programmed to be either TTL or CMOS compatible thresholds. At power-up, all inputs have TTL thresholds and can change to CMOS thresholds at the completion of configuration if the user has selected CMOS thresholds. The threshold of $\overline{\text{PWRDWN}}$ and the direct clock inputs are fixed at a CMOS level.

If the crystal oscillator is used, it will begin operation before configuration is complete to allow time for stabilization before it is connected to the internal circuitry.

Configuration Data

Configuration data to define the function and interconnection within a Field Programmable Gate Array is loaded from an external storage at power-up and after a re-program signal. Several methods of automatic and controlled loading of the required data are available. Logic levels applied to mode selection pins at the start of configuration time determine the method to be used. See Table 1. The data may be either bit-serial or byte-parallel, depending on the configuration mode. The different FPGAs have different sizes and numbers of data frames. To maintain compatibility between various device types, the Xilinx product families use compatible configuration formats. For the XC3020A, configuration requires 14779 bits for each device, arranged in 197 data frames. An additional 40 bits are used in the header. See Figure 22. The specific data format for each device is produced by the MakeBits command of the development system and one or more of these files can then be combined and appended to a length count preamble and be transformed into a PROM format file by the MakePROM command of the *XACTstep* development system. A compatibility exception precludes the use of an XC2000-series device as the master for XC3000-series devices if their DONE or RESET are programmed to occur after their outputs become active. The Tie Option of the MakeBits program defines output levels of unused blocks of a design and connects these to unused routing resources. This prevents indeterminate levels that might produce parasitic



* The configuration data consists of a composite 40-bit preamble/length count, followed by one or more concatenated FPGA programs, separated by 4-bit postambles. An additional final postamble bit is added for each slave device and the result rounded up to a byte boundary. The length count is two less than the number of resulting bits.

Timing of the assertion of DONE and termination of the INTERNAL $\overline{\text{RESET}}$ may each be programmed to occur one cycle before or after the I/O outputs become active.

Heavy lines indicate the default condition

Figure 22: Configuration and Start-up of One or More FPGAs.

supply currents. If unused blocks are not sufficient to complete the tie, the Flagnet command of EditLCA can be used to indicate nets which must not be used to drive the remaining unused routing, as that might affect timing of user nets. Norestore will retain the results of tie for timing analysis with Querynet before Restore returns the design to the untied condition. Tie can be omitted for quick breadboard iterations where a few additional milliamps of Icc are acceptable.

The configuration bitstream begins with eight High preamble bits, a 4-bit preamble code and a 24-bit length count. When configuration is initiated, a counter in the FPGA is set to zero and begins to count the total number of configuration clock cycles applied to the device. As each configuration data frame is supplied to the device, it is internally assembled into a data word, which is then loaded in parallel into one word of the internal configuration memory array. The configuration loading process is complete when the current length count equals the loaded length count and the required configuration program data frames have been written. Internal user flip-flops are held Reset during configuration.

Two user-programmable pins are defined in the unconfigured Field Programmable Gate Array. High During Configuration (HDC) and Low During Configuration ($\overline{\text{LDC}}$) as well as DONE/$\overline{\text{PROG}}$ may be used as external control signals during configuration. In Master mode configurations it is convenient to use $\overline{\text{LDC}}$ as an active-Low EPROM Chip Enable. After the last configuration data bit is loaded and the length count compares, the user I/O pins become active. Options in the MakeBits program allow timing choices of one clock earlier or later for the timing of the end of the internal logic RESET and the assertion of the DONE signal. The open-drain DONE/$\overline{\text{PROG}}$ output can be AND-tied with multiple devices and used as an active-High READY, an active-Low PROM enable or a RESET to other portions of the system. The state diagram of Figure 20 illustrates the configuration process.

Configuration Modes

Master Mode

In Master mode, the FPGA automatically loads configuration data from an external memory device. There are three Master modes that use the internal timing source to supply the configuration clock (CCLK) to time the incoming data. Master Serial mode uses serial configuration data supplied to Data-in (DIN) from a synchronous serial source such as the Xilinx Serial Configuration PROM shown in Figure 23. Master Parallel Low and High modes automatically use parallel data supplied to the D0–D7 pins in response to the 16-bit address generated by the FPGA. Figure 25 shows an example of the parallel Master mode connections required. The HEX starting address is 0000 and increments for Master Low mode and it is FFFF and decrements for Master High mode. These two modes provide address compatibility with microprocessors which begin execution from opposite ends of memory.

Peripheral Mode

Peripheral mode provides a simplified interface through which the device may be loaded byte-wide, as a processor peripheral. Figure 27 shows the peripheral mode connections. Processor write cycles are decoded from the common assertion of the active low Write Strobe ($\overline{\text{WS}}$), and two active low and one active high Chip Selects ($\overline{\text{CS0}}$, $\overline{\text{CS1}}$, CS2). The FPGA generates a configuration clock from the internal timing generator and serializes the parallel input data for internal framing or for succeeding slaves on Data Out (DOUT). A output High on READY/$\overline{\text{BUSY}}$ pin indicates the completion of loading for each byte when the input register is ready for a new byte. As with Master modes, Peripheral mode may also be used as a lead device for a daisy-chain of slave devices.

Slave Serial Mode

Slave Serial mode provides a simple interface for loading the Field Programmable Gate Array configuration as shown in Figure 29. Serial data is supplied in conjunction with a synchronizing input clock. Most Slave mode applications are in daisy-chain configurations in which the data input is driven from the previous FPGA's data out, while the clock is supplied by a lead device in Master or Peripheral mode. Data may also be supplied by a processor or other special circuits.

Daisy Chain

The *XACTstep* development system is used to create a composite configuration for selected FPGAs including: a preamble, a length count for the total bitstream, multiple concatenated data programs and a postamble plus an additional fill bit per device in the serial chain. After loading and passing-on the preamble and length count to a possible daisy-chain, a lead device will load its configuration data frames while providing a High DOUT to possible down-stream devices as shown in Figure 25. Loading continues while the lead device has received its configuration program and the current length count has not reached the full value. The additional data is passed through the lead device and appears on the Data Out (DOUT) pin in serial form. The lead device also generates the Configuration Clock (CCLK) to synchronize the serial output data and data in of down-stream FPGAs. Data is read in on DIN of slave devices by the positive edge of CCLK and shifted out the DOUT on the negative edge of CCLK. A parallel Master mode device uses its internal timing generator to produce an internal CCLK of 8 times its EPROM address rate, while a Peripheral mode device produces a burst of 8 CCLKs for each chip select and write-strobe cycle. The internal timing generator continues to operate for general timing and synchronization of inputs in all modes.

Special Configuration Functions

The configuration data includes control over several special functions in addition to the normal user logic functions and interconnect.

- Input thresholds
- Readback disable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal *XACTstep* development system bitstream generation process.

Input Thresholds

Prior to the completion of configuration all FPGA input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the $\overline{\text{PWRDWN}}$ input and direct clocks which always have a CMOS input. Prior to the completion of configuration the user I/O pins each have a high impedance pull-up. The configuration program can be used to enable the IOB pull-up resistors in the Operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

Readback

The contents of a Field Programmable Gate Array may be read back if it has been programmed with a bitstream in which the Readback option has been enabled. Readback may be used for verification of configuration and as a method of determining the state of internal logic nodes during debugging. There are three options in generating the configuration bitstream.

- "Never" inhibits the Readback capability.
- "One-time," inhibits Readback after one Readback has been executed to verify the configuration.
- "On-command" allows unrestricted use of Readback.

Readback is accomplished without the use of any of the user I/O pins; only M0, M1 and CCLK are used. The initiation of Readback is produced by a Low to High transition of the M0/RTRIG (Read Trigger) pin. The CCLK input must then be driven by external logic to read back the configuration data. The first three Low-to-High CCLK transitions clock out dummy data. The subsequent Low-to-High CCLK transitions shift the data frame information out on the M1/$\overline{\text{RDATA}}$ (Read Data) pin. Note that the logic polarity is always inverted, a zero in configuration becomes a one in Readback, and vice versa. Note also that each Readback frame has one Start bit (read back as a one) but, unlike in configuration, each Readback frame has only one Stop bit (read back as a zero). The third leading dummy bit mentioned above can be considered the Start bit of the first frame. All data frames must be read back to complete the process and return the Mode Select and CCLK pins to their normal functions.

Readback data includes the current state of each CLB flip-flop, each input flip-flop or latch, and each device pad. These data are imbedded into unused configuration bit positions during Readback. This state information is used by the *XACTstep* development system In-Circuit Verifier to provide visibility into the internal operation of the logic while the system is operating. To readback a uniform time-sample of all storage elements, it may be necessary to inhibit the system clock.

Reprogram

To initiate a re-programming cycle, the dual-function pin DONE/$\overline{\text{PROG}}$ must be given a High-to-Low transition. To reduce sensitivity to noise, the input signal is filtered for two cycles of the FPGA internal timing generator. When reprogram begins, the user-programmable I/O output buffers are disabled and high-impedance pull-ups are provided for the package pins. The device returns to the Clear state and clears the configuration memory before it indicates 'initialized'. Since this Clear operation uses chip-individual internal timing, the master might complete the Clear operation and then start configuration before the slave has completed the Clear operation. To avoid this problem, the slave $\overline{\text{INIT}}$ pins must be AND-wired and used to force a $\overline{\text{RESET}}$ on the master (see Figure 25). Reprogram control is often implemented using an external open-collector driver which pulls DONE/$\overline{\text{PROG}}$ Low. Once a stable request is recognized, the DONE/$\overline{\text{PROG}}$ pin is held Low until the new configuration has been completed. Even if the re-program request is externally held Low beyond the configuration period, the FPGA will begin operation upon completion of configuration.

DONE Pull-up

DONE/$\overline{\text{PROG}}$ is an open-drain I/O pin that indicates the FPGA is in the operational state. An optional internal pull-up resistor can be enabled by the user of the XACT development system when MakeBits is executed. The DONE/$\overline{\text{PROG}}$ pins of multiple FPGAs in a daisy-chain may be connected together to indicate all are DONE or to direct them all to reprogram.

DONE Timing

The timing of the DONE status signal can be controlled by a selection in the MakeBits program to occur either a CCLK cycle before, or after, the outputs going active. See Figure 22. This facilitates control of external functions such as a PROM enable or holding a system in a wait state.

RESET Timing

As with DONE timing, the timing of the release of the internal reset can be controlled by a selection in the MakeBits program to occur either a CCLK cycle before, or after, the outputs going active. See Figure 22. This reset keeps all user programmable flip-flops and latches in a zero state during configuration.

Crystal Oscillator Division

A selection in the MakeBits program allows the user to incorporate a dedicated divide-by-two flip-flop between the crystal oscillator and the alternate clock line. This guarantees a symmetrical clock signal. Although the frequency stability of a crystal oscillator is very good, the symmetry of its waveform can be affected by bias or feedback drive.

Bitstream Error Checking

Bitstream error checking protects against erroneous configuration.

Each Xilinx FPGA bitstream consists of a 40-bit preamble, followed by a device-specific number of data frames. The number of bits per frame is also device-specific; however, each frame ends with three stop bits (111) followed by a start bit for the next frame (0).

All devices in all XC3000 families start reading in a new frame when they find the first 0 after the end of the previous frame. XC3000 device does not check for the correct stop bits, but XC3000A/XC3100A/XC3000L and XC3100L devices check that the last three bits of any frame are actually 111.

Under normal circumstances, all these FPGAs behave the same way; however, if the bitstream is corrupted, an XC3000 device will always start a new frame as soon as it finds the first 0 after the end of the previous frame, even if the data is completely wrong or out-of-sync. Given sufficient zeros in the data stream, the device will also go Done, but with incorrect configuration and the possibility of internal contention.

An XC3000A/XC3100A/XC3000L/XC3100L device starts any new frame only if the three preceding bits are all ones. If this check fails, it pulls $\overline{\text{INIT}}$ Low and stops the internal configuration, although the Master CCLK keeps running. The user must then start a new configuration by applying a >6 µs Low level on $\overline{\text{RESET}}$.

This simple check does not protect against random bit errors, but it offers almost 100 percent protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, or PC-board level defects, such as broken lines or solder-bridges.

Reset Spike Protection

A separate modification slows down the $\overline{\text{RESET}}$ input before configuration by using a two-stage shift register driven from the internal clock. It tolerates submicrosecond High spikes on $\overline{\text{RESET}}$ before configuration. The XC3000 master can be connected like an XC4000 master, but with its $\overline{\text{RESET}}$ input used instead of $\overline{\text{INIT}}$. (On XC3000, $\overline{\text{INIT}}$ is output only).

Soft Start-up

After configuration, the outputs of all FPGAs in a daisy-chain become active simultaneously, as a result of the same CCLK edge. In the original XC3000/3100 devices, each output becomes active in either fast or slew-rate limited mode, depending on the way it is configured. This can lead to large ground-bounce signals. In XC3000A/XC3000L/XC31000A/XC3100L devices, all outputs become active first in slew-rate limited mode, reducing the ground bounce. After this soft start-up, each individual output slew rate is again controlled by the respective configuration bit.

Configuration Timing

This section describes the configuration modes in detail.

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. This puts the next data bit on the SPROM data output, connected to the DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

The SPROM CE input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output. Using DONE also avoids contention on DIN, provided the early DONE option is invoked.

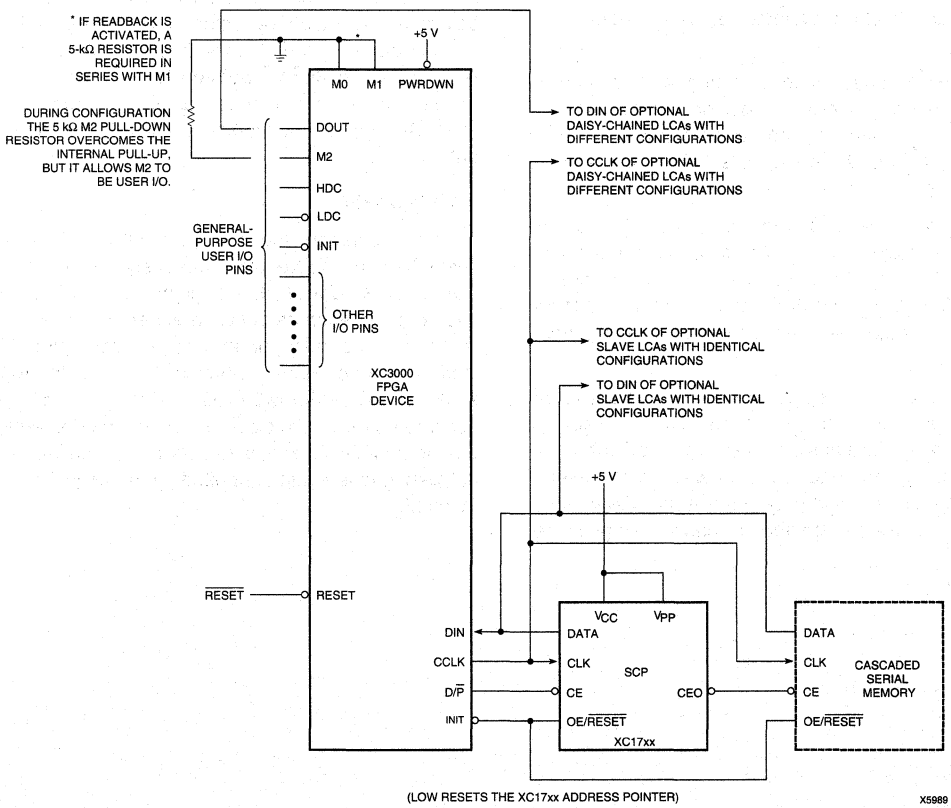
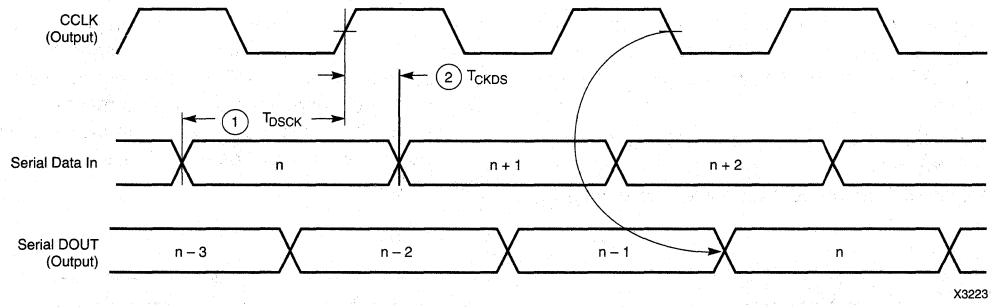


Figure 23: Master Serial Mode Circuit Diagram



	Description		Symbol	Min	Max	Units
CCLK	Data In setup	1	T_{DSCK}	60		ns
	Data In hold	2	C_{KDS}	0		ns

Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require >6-µs High level on RESET, followed by a >6-µs Low level on $\overline{\text{RESET}}$ and D/$\overline{\text{P}}$ after VCC has reached 4.0 V (2.5 V for the XC3000L).
2. Configuration can be controlled by holding $\overline{\text{RESET}}$ Low with or until after the $\overline{\text{INIT}}$ of all daisy-chain slave-mode devices is High.
3. Master-serial-mode timing is based on slave-mode testing.

Figure 24: Master Serial Mode Programming Switching Characteristics

Master Parallel Mode

In Master Parallel mode, the lead FPGA directly addresses an industry-standard byte-wide EPROM and accepts eight data bits right before incrementing (or decrementing) the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data (and all data that overflows the lead device) on the DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data, and also changes the EPROM address, until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next device in the daisy chain accepts data on the subsequent rising CCLK edge.

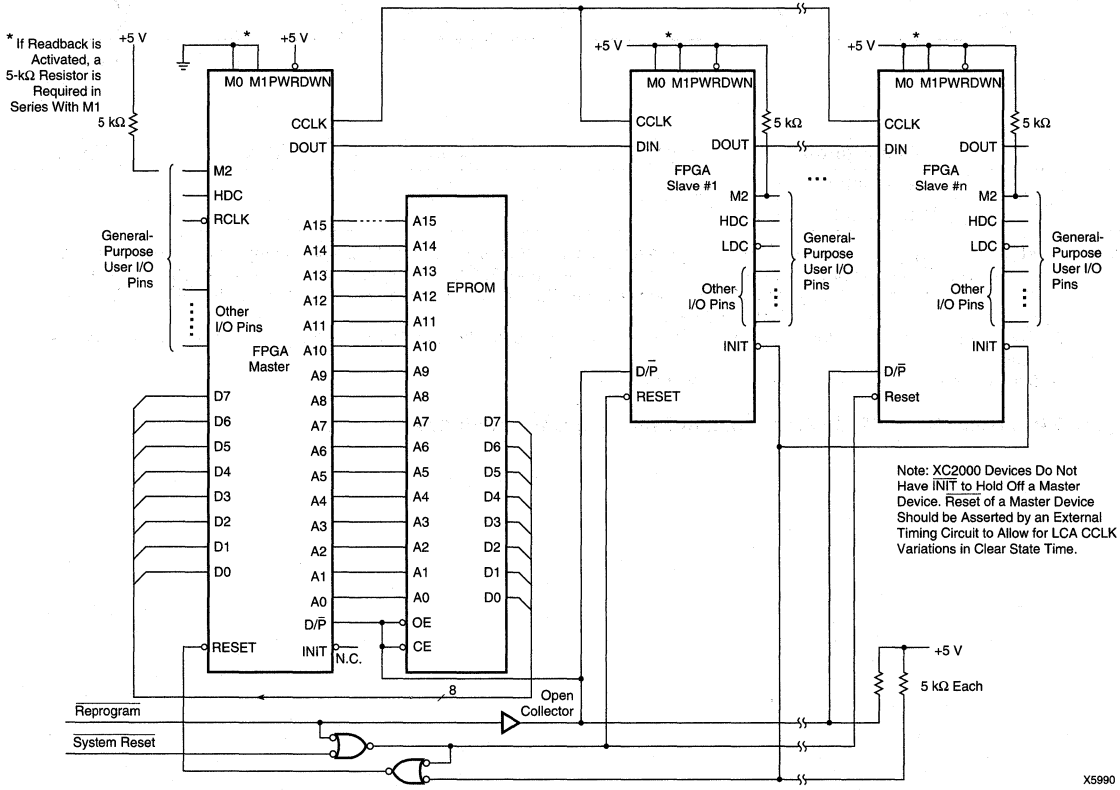
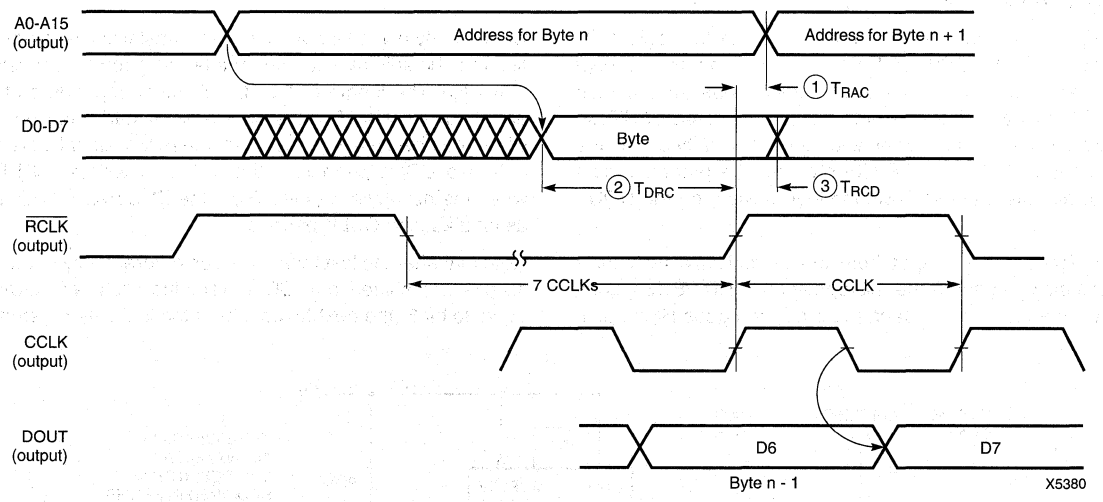


Figure 25: Master Parallel Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
RCLK	To address valid	1	T_{RAC}	0	200	ns
	To data setup	2	T_{DRC}	60		ns
	To data hold	3	T_{RCD}	0		ns
	RCLK High		T_{RCH}	600		ns
	RCLK Low		T_{RCL}	4.0		µs

Notes: 1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{\text{RESET}}$ Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on $\overline{\text{RESET}}$, followed by a >6-µs Low level on $\overline{\text{RESET}}$ and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

2. Configuration can be controlled by holding $\overline{\text{RESET}}$ Low with or until after the $\overline{\text{INIT}}$ of all daisy-chain slave-mode devices is High.

This timing diagram shows that the EPROM requirements are extremely relaxed:
EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

Figure 26: Master Parallel Mode Programming Switching Characteristics

Peripheral Mode

Peripheral mode uses the trailing edge of the logic AND condition of the $\overline{CS0}$, $\overline{CS1}$, CS2, and $\overline{WS}$ inputs to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic. The lead FPGA presents the preamble data (and all data that overflows the lead device) on the DOUT pin.

The Ready/Busy output from the lead device acts as a handshake signal to the microprocessor. RDY/$\overline{BUSY}$ goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. The length of the $\overline{BUSY}$ signal depends on the activity in the UART. If the shift register had been empty when the new byte was received, the $\overline{BUSY}$ signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the $\overline{BUSY}$ signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

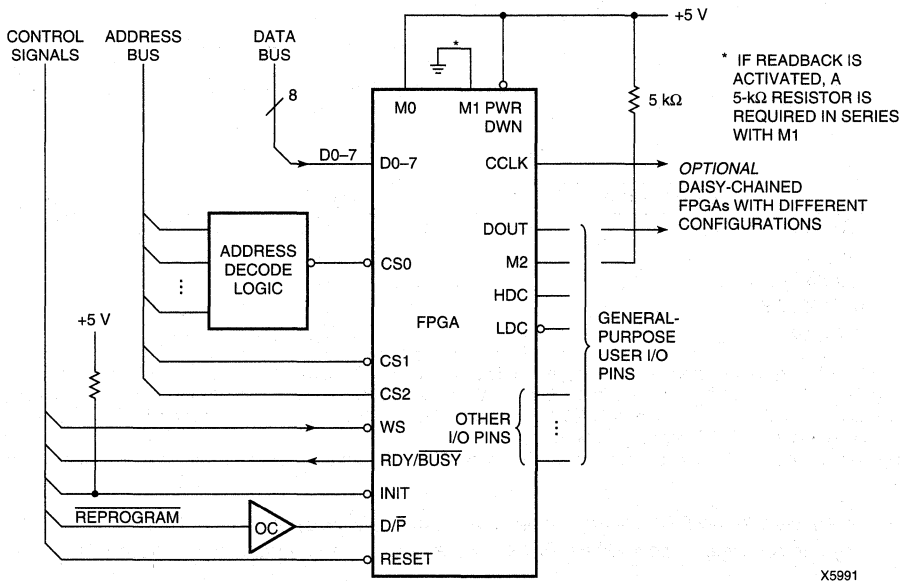
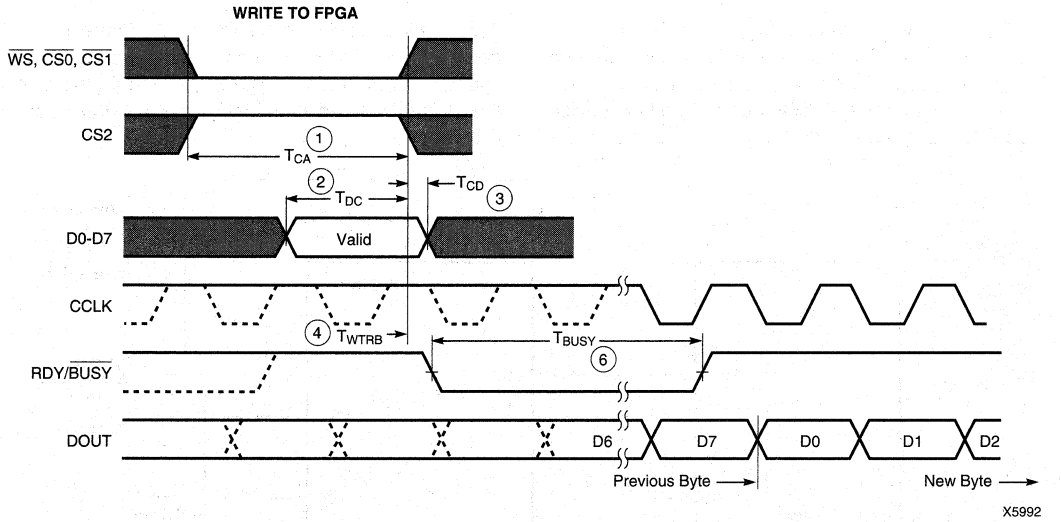


Figure 27: Peripheral Mode Circuit Diagram



	Description		Symbol	Min	Max	Units
WRITE	Effective Write time required (Assertion of $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{WS}$)	1	T_{CA}	100		ns
	DIN Setup time required	2	T_{DC}	60		ns
	DIN Hold time required	3	T_{CD}	0		ns
	RDY/$\overline{BUSY}$ delay after end of $\overline{WS}$	4	T_{WTRB}		60	ns
RDY	Earliest next $\overline{WS}$ after end of $\overline{BUSY}$	5	T_{RBWT}	0		ns
	$\overline{BUSY}$ Low time generated	6	T_{BUSY}	2.5	9	CCLK periods

Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{RESET}$ Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on $\overline{RESET}$, followed by a >6-µs Low level on $\overline{RESET}$ and D/$\overline{P}$ after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
2. Configuration must be delayed until the $\overline{INIT}$ of all FPGAs is High.
3. Time from end of $\overline{WS}$ to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
4. CCLK and DOUT timing is tested in slave mode.
5. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest TBUSY occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

Note: *This timing diagram shows very relaxed requirements: Data need not be held beyond the rising edge of $\overline{WS}$. $\overline{BUSY}$ will go active within 60 ns after the end of $\overline{WS}$. $\overline{BUSY}$ will stay active for several microseconds. $\overline{WS}$ may be asserted immediately after the end of $\overline{BUSY}$.*

Figure 28: Peripheral Mode Programming Switching Characteristics

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input(s) of the FPGA(s). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short set-up time before each rising CCLK edge. The lead device then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

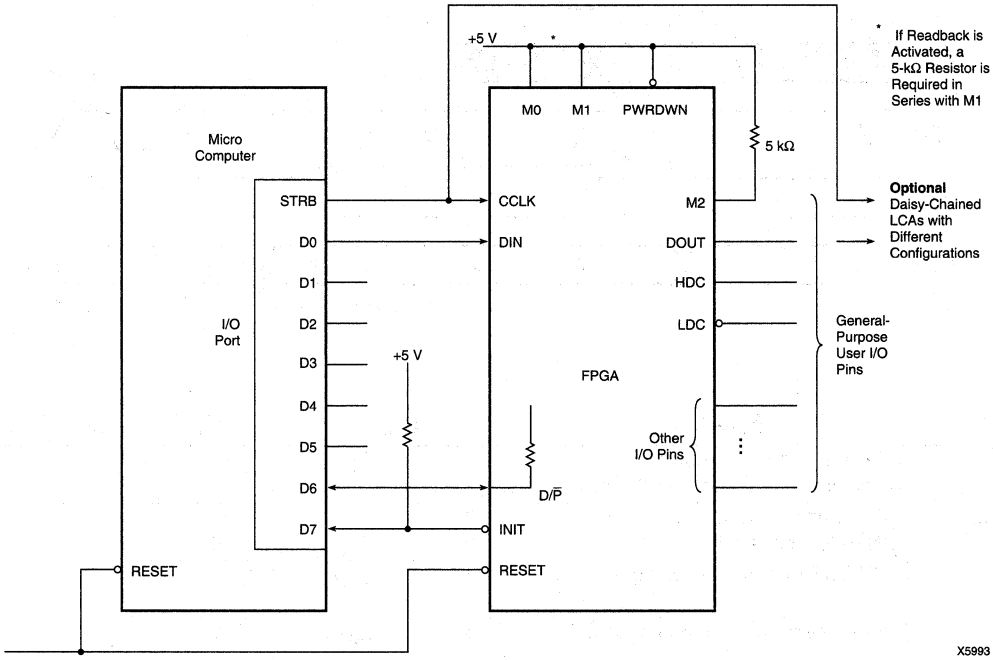
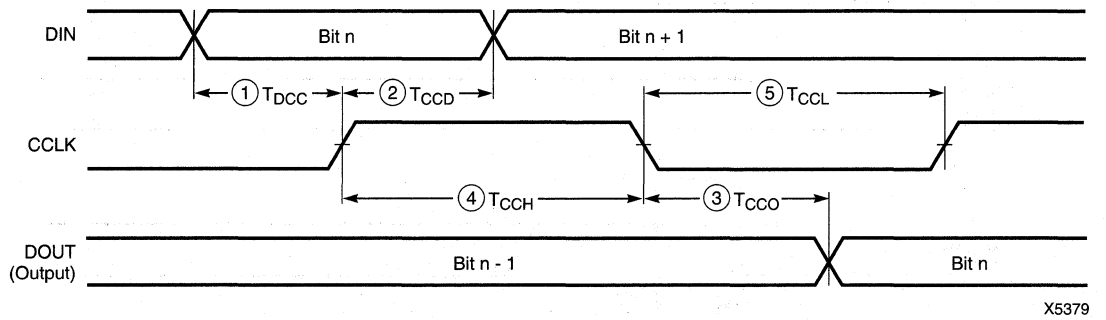


Figure 29: Slave Serial Mode Circuit Diagram

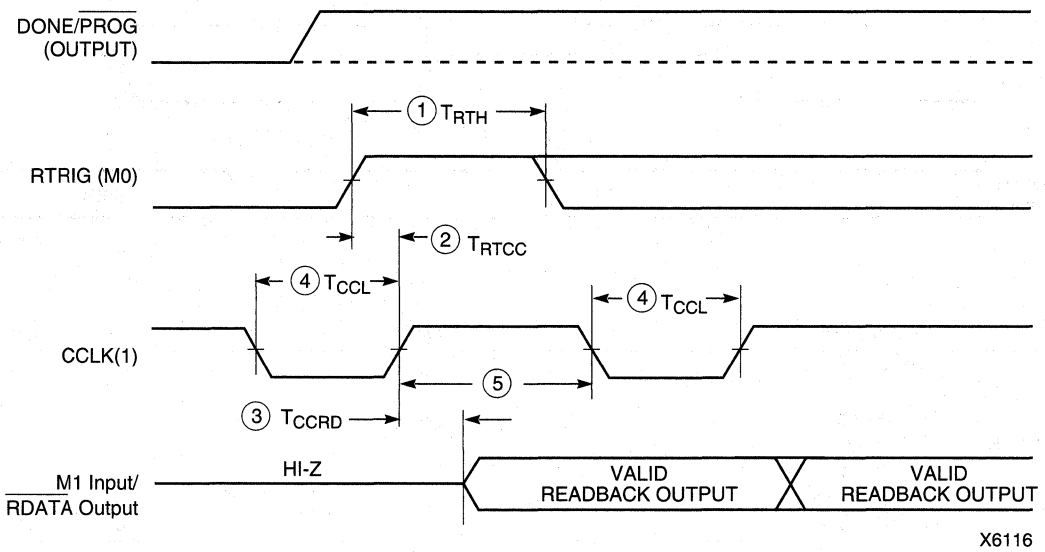


	Description		Symbol	Min	Max	Units
CCLK	To DOUT	3	T_{CCO}		100	ns
	DIN setup	1	T_{DCC}	60		ns
	DIN hold	2	T_{CCD}	0		ns
	High time	4	T_{CCH}	0.05		ns
	Low time (Note 1)	5	T_{CCL}	0.05	5.0	µs
	Frequency		F_{CC}		10	MHz

Notes:
1. The max limit of CCLK Low time is caused by dynamic circuitry inside the FPGA.
2. Configuration must be delayed until the $\overline{INIT}$ of all FPGAs is High.
3. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{RESET}$ Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on $\overline{RESET}$, followed by a >6-µs Low level on $\overline{RESET}$ and D/$\overline{P}$ after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

Figure 30: Slave Serial Mode Programming Switching Characteristics

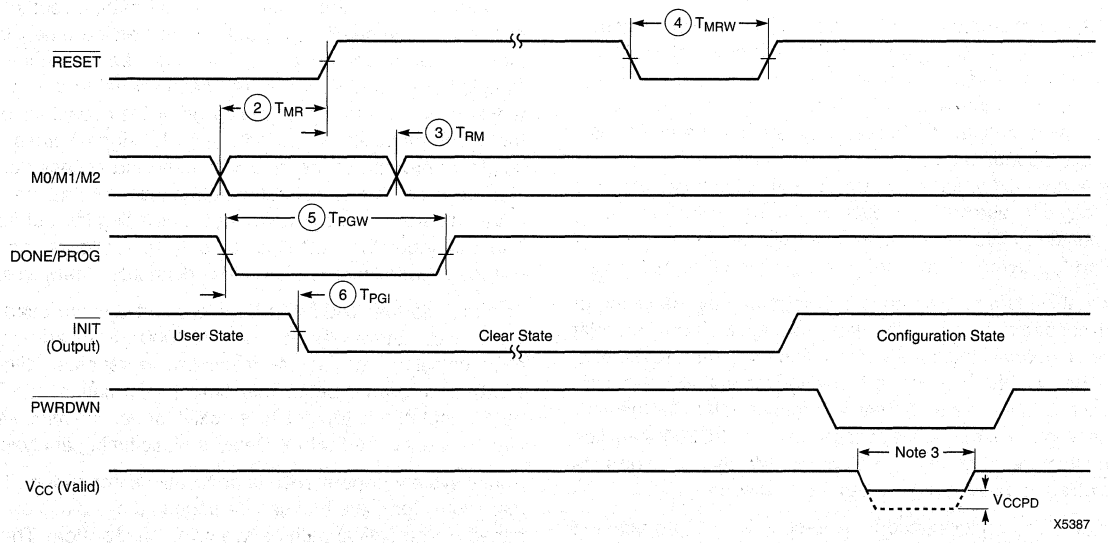
Program Readback Switching Characteristics



	Description		Symbol	Min	Max	Units
RTRIG	RTRIG High	1	T_{RTH}	250		ns
CCLK	RTRIG setup	2	T_{RTCC}	200		ns
	$\overline{RDATA}$ delay	3	T_{CCRD}		100	ns
	High time	4	T_{CCHR}	0.5		µs
	Low time	5	T_{CCLR}	0.5	5	µs

Notes:
1. During Readback, CCLK frequency may not exceed 1 MHz.
2. RETRIG (M0 positive transition) shall not be done until after one clock following active I/O pins.
3. Readback should not be initiated until configuration is complete.
4. T_{CCLR} is 5 µs min to 15 µs max for XC3000L.

General XC3000 Series Switching Characteristics



	Description		Symbol	Min	Max	Units
RESET (2)	M0, M1, M2 setup time required	2	T_{MR}	1		µs
	M0, M1, M2 hold time required	3	T_{RM}	4.5		µs
	RESET Width (Low) req. for Abort	4	T_{MRW}	6		µs
DONE/PROG	Width (Low) required for Re-config.	5	T_{PGW}	6		µs
	INIT response after D/P is pulled Low	6	T_{PGI}		7	µs
PWRDWN (3)	Power Down V_{CC}		V_{CCPD}	2.3		V

Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until Vcc has reached 4.0 V (2.5 V for XC3000L). A very long Vcc rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >1-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after Vcc has reached 4.0 V (2.5 V for XC3000L).
2. RESET timing relative to valid mode lines (M0, M1, M2) is relevant when RESET is used to delay configuration. The specified hold time is caused by a shift-register filter slowing down the response to RESET during configuration.
3. PWRDWN transitions must occur while V_{CC} >4.0 V(2.5 V for XC3000L).

Device Performance

The XC3000 families of FPGAs can achieve very high performance. This is the result of

- A sub-micron manufacturing process, developed and continuously being enhanced for the production of state-of-the-art CMOS SRAMs.
- Careful optimization of transistor geometries, circuit design, and lay-out, based on years of experience with the XC3000 family.
- A look-up table based, coarse-grained architecture that can collapse multiple-layer combinatorial logic into a single function generator. One CLB can implement up to four layers of conventional logic in as little as 1.5 ns.

Actual system performance is determined by the timing of critical paths, including the delay through the combinatorial and sequential logic elements within CLBs and IOBs, plus the delay in the interconnect routing. The AC-timing specifications state the worst-case timing parameters for the various logic resources available in the XC3000-families architecture. Figure 31 shows a variety of elements involved in determining system performance.

Logic block performance is expressed as the propagation time from the interconnect point at the input to the block to the output of the block in the interconnect area. Since combinatorial logic is implemented with a memory lookup table within a CLB, the combinatorial delay through the CLB, called T_{ILO}, is always the same, regardless of the function being implemented. For the combinatorial logic function driving the data input of the storage element, the critical timing is data set-up relative to the clock edge provided to the flip-flop element. The delay from the clock source to the output of the logic block is critical in the timing signals produced by storage elements. Loading of a logic-block output is limited only by the resulting propagation delay of the larger interconnect network. Speed performance of the logic block is a function of supply voltage and temperature. See Figure 32.

Interconnect performance depends on the routing resources used to implement the signal path. Direct interconnects to the neighboring CLB provide an extremely fast path. Local interconnects go through switch matrices (magic boxes) and suffer an RC delay, equal to the resistance of the pass transistor multiplied by the capacitance of the driven metal line. Longlines carry the signal across the length or breadth of the chip with only one access delay. Generous on-chip signal buffering makes performance relatively insensitive to signal fan-out; increasing fan-out from 1 to 8 changes the CLB delay by only 10%. Clocks can be distributed with two low-skew clock distribution networks.

The tools in the *XACTstep* Development System used to place and route a design in an XC3000 FPGA automatically calculate the actual maximum worst-case delays along each signal path. This timing information can be back-annotated to the design's netlist for use in timing simulation or examined with X-Delay, a static timing analyzer.

Actual system performance is applications dependent. The maximum clock rate that can be used in a system is determined by the critical path delays within that system. These delays are combinations of incremental logic and routing delays, and vary from design to design. In a synchronous system, the maximum clock rate depends on the number of combinatorial logic layers between re-synchronizing flip-flops. Figure 33 shows the achievable clock rate as a function of the number of CLB layers.

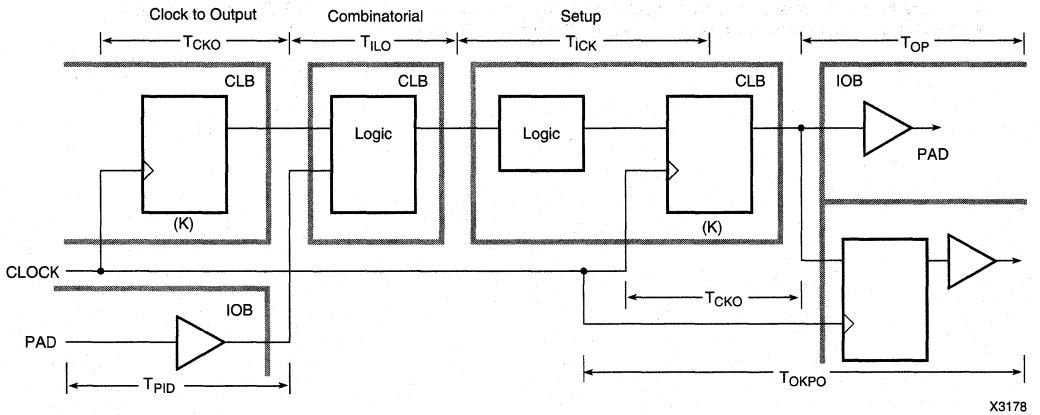


Figure 31: Primary Block Speed Factors. Actual timing is a function of various block factors combined with routing. factors. Overall performance can be evaluated with the XDelay timing calculator or by an optional simulation.

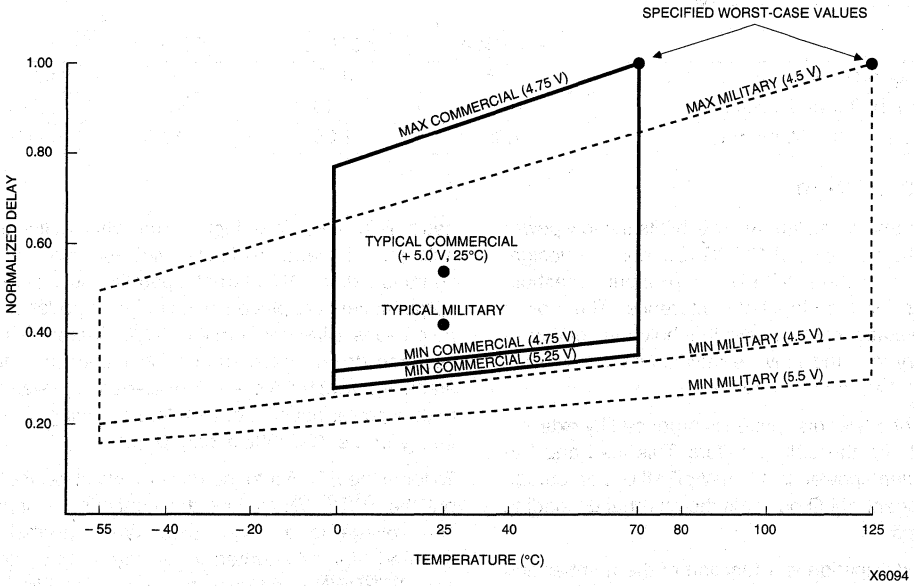


Figure 32: Relative Delay as a Function of Temperature, Supply Voltage and Processing Variations

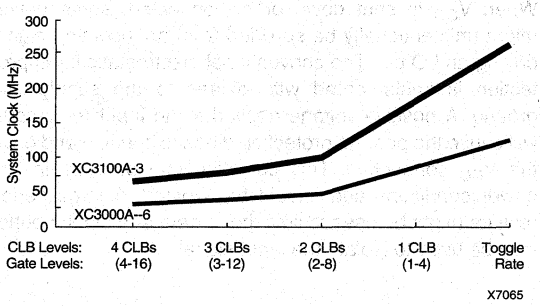


Figure 33: Clock Rate as a Function of Logic Complexity (Number of Combinational Levels between Flip-Flops)

Power

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated V_{CC} and ground ring surrounding the logic array provides power to the I/O drivers. An independent matrix of V_{CC} and groundlines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4- or 8-mA loads under worst-case conditions may be capable of driving as much as 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise.

Dynamic Power Consumption

	XC3042A	XC3042L	XC3142A	
One CLB driving three local interconnects	0.25	0.17	0.25	mW per MHz
One global clock buffer and clock line	2.25	1.40	1.70	mW per MHz
One device output with a 50 pF load	1.25	1.25	1.25	mW per MHz

Power Consumption

The Field Programmable Gate Array exhibits the low power consumption characteristic of CMOS ICs. For any design, the configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells that hold the configuration data is very low and may be maintained in a power-down mode.

Typically, most of power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25 μW/pF/MHz per output. Another component of I/O power is the external dc loading on all output pins.

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an FPGA, the fraction of nodes changing on a given clock is typically low (10-20%). For example, in a long binary counter, the total activity of all counter flip-flops is equivalent to that of only two CLB outputs toggling at the clock frequency. Typical global clock-buffer power is between 2.0 mW/MHz for the XC3020A and 3.5 mW/MHz for the XC3090A. The internal capacitive load is more a function of interconnect than fan-out. With a typical load of three general interconnect segments, each CLB output requires about 0.25 mW per MHz of its output frequency.

Because the control storage of the FPGA is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The FPGA has built in powerdown logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high-impedance state with no pull-ups. Different from the XC3000 family which can be powered down to a current consumption of a few microamps, the XC3100A draws 5 mA, even in power-down. This makes power-down operation less meaningful. In contrast, I_{CCPD} for the XC3000L is only 10 μA.

To force the FPGA into the Powerdown state, the user must pull the $\overline{\text{PWRDWN}}$ pin Low and continue to supply a retention voltage to the V_{CC} pins. When normal power is restored, V_{CC} is elevated to its normal operating voltage and $\overline{\text{PWRDWN}}$ is returned to a High. The FPGA resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal-I/O and logic-block storage elements will be reset, the outputs will become enabled and the DONE/$\overline{\text{PROG}}$ pin will be released.

When V_{CC} is shut down or disconnected, some power might unintentionally be supplied from an incoming signal driving an I/O pin. The conventional electrostatic input protection is implemented with diodes to the supply and ground. A positive voltage applied to an input (or output) will cause the positive protection diode to conduct and drive the V_{CC} connection. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bipolar buffer may be used to isolate the input signal.

Pin Descriptions

Permanently Dedicated Pins

V_{CC}

Two to eight (depending on package type) connections to the positive V supply voltage. All must be connected.

GND

Two to eight (depending on package type) connections to ground. All must be connected.

$\overline{\text{PWRDWN}}$

A Low on this CMOS-compatible input stops all internal activity, but retains configuration. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. When $\overline{\text{PWDWN}}$ returns High, the FPGA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. Before and during configuration, $\overline{\text{PWRDWN}}$ must be High. If not used, $\overline{\text{PWRDWN}}$ must be tied to V_{CC}.

$\overline{\text{RESET}}$

This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{\text{RESET}}$ are complete, the levels of the M lines are sampled and configuration begins.

If $\overline{\text{RESET}}$ is asserted during a configuration, the FPGA is re-initialized and restarts the configuration at the termination of $\overline{\text{RESET}}$.

If $\overline{\text{RESET}}$ is asserted after configuration is complete, it provides a global asynchronous $\overline{\text{RESET}}$ of all IOB and CLB storage elements of the FPGA.

CCLK

During configuration, Configuration Clock is an output of an FPGA in Master mode or Peripheral mode, but an input in Slave mode. During Readback, CCLK is a clock input for shifting configuration data out of the FPGA.

CCLK drives dynamic circuitry inside the FPGA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be "parked High". An internal pull-up resistor maintains High when the pin is not being driven.

DONE/$\overline{\text{PROG}}$ (D/$\overline{\text{P}}$)

DONE is an open-drain output, configurable with or without an internal pull-up resistor of 2 to 8 k Ω. At the completion of configuration, the FPGA circuitry becomes active in a synchronous order; DONE is programmed to go active High one cycle either before or after the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the FPGA and start a reconfiguration.

M0/RTRIG

As Mode 0, this input is sampled on power-on to determine the power-on delay (2^{14} cycles if M0 is High, 2^{16} cycles if M0 is Low). Before the start of configuration, this input is again sampled together with M1, M2 to determine the configuration mode to be used.

A Low-to-High input transition, after configuration is complete, acts as a Read Trigger and initiates a Readback of configuration and storage-element data clocked by CCLK. By selecting the appropriate Readback option when generating the bitstream, this operation may be limited to a single Readback, or be inhibited altogether.

M1/$\overline{\text{RDATA}}$

As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If Readback is never used, M1 can be tied directly to ground or V_{CC}. If Readback is ever used, M1 must use a 5-kΩ resistor to ground or V_{CC}, to accommodate the RDATA output.

As an active-Low Read Data, after configuration is complete, this pin is the output of the Readback data.

User I/O Pins That Can Have Special Functions

M2

During configuration, this input has a weak pull-up resistor. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin is a user-programmable I/O pin.

HDC

During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{\text{LDC}}$

During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. $\overline{\text{LDC}}$ is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

$\overline{\text{INIT}}$

This is an active Low open-drain output with a weak pull-up and is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired

AND of several slave mode devices, a hold-off signal for a master mode device. After configuration this pin becomes a user-programmable I/O pin.

BCLKIN

This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

XTL1

This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2

This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the MakeBits program.

$\overline{CS0}$, $\overline{CS1}$, CS2, $\overline{WS}$

These four inputs represent a set of signals, three active Low and one active High, that are used to control configuration-data entry in the Peripheral mode. Simultaneous assertion of all four inputs generates a Write to the internal data buffer. The removal of any assertion clocks in the D0-D7 data. In Master-Parallel mode, WS and CS2 are the A0 and A1 outputs. After configuration, these pins are user-programmable I/O pins.

RDY/$\overline{BUSY}$

During Peripheral Parallel mode configuration this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user-programmed I/O pin.

$\overline{RCLK}$

During Master Parallel mode configuration, each change on the A0-15 outputs is preceded by a rising edge on $\overline{RCLK}$, a redundant output signal. After configuration is complete, this pin becomes a user-programmed I/O pin.

D0-D7

This set of eight pins represents the parallel configuration byte for the parallel Master and Peripheral modes. After configuration is complete, they are user-programmed I/O pins.

A0-A15

During Master Parallel mode, these 16 pins present an address output for a configuration EPROM. After configuration, they are user-programmable I/O pins.

DIN

During Slave or Master Serial configuration, this pin is used as a serial-data input. In the Master or Peripheral configuration, this is the Data 0 input. After configuration is complete, this pin becomes a user-programmed I/O pin.

DOUT

During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave. After configuration is complete, this pin becomes a user-programmed I/O pin.

TCLKIN

This is a direct CMOS-level input to the global clock buffer. This pin can also be configured as a user programmable I/O pin. However, since TCLKIN is the preferred input to the global clock net, and the global clock net should be used as the primary clock source, this pin is usually the clock input to the chip.

Unrestricted User I/O Pins

I/O

An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned on the following page, have a weak pull-up resistor of 50 kΩ to 100 kΩ that becomes active as soon as the device powers up, and stays active until the end of configuration.

Note: *Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50 kΩ to 100 kΩ pull-up resistor.*

Pin Functions During Configuration

Configuration Mode <M2:M1:M0>					***												***		
SLAVE SERIAL <1:1:1>	**MASTER-SERIAL <0:0:0>**	**PERIPH <1:0:1>**	**MASTER-HIGH <1:1:0>**	**MASTER-LOW <1:0:0>**	**44 PLCC**	**64 VQFP**	**68 PLCC**	**84 PLCC**	**84 PGA**	**100 PQFP**	**100 VQFP TQFP**	**132 PGA**	**144 TQFP**	**160 PQFP**	**175 PGA**	**176 TQFP**	**208 PQFP**	**223 PGA**	**User Function**
$\overline{\text{POWER DWN}}$ (I)	$\overline{\text{POWER DWN}}$ (I)	$\overline{\text{POWER DWN}}$ (I)	$\overline{\text{POWER DWN}}$ (I)	$\overline{\text{POWER DWN}}$ (I)	7	17	10	12	B2	29	26	A1	1	159	B2	1	3	B2	$\overline{\text{POWER DWN}}$ (1)
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	16	31	25	31	J2	52	49	B13	36	40	B14	45	48	C16	RDATA
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	Mo (LOW) (I)	17	32	26	32	L1	54	51	A14	38	42	B15	47	50	B17	RTRIG (I)
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	18	33	27	33	K2	56	53	C13	40	44	C15	49	56	A17	I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	19	34	28	34	K3	57	54	B14	41	45	E14	50	57	A18	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	20	36	30	36	L3	59	56	D14	45	49	D16	54	61	E16	I/O
$\overline{\text{INIT}}$*	$\overline{\text{INIT}}$*	$\overline{\text{INIT}}$*	$\overline{\text{INIT}}$*	$\overline{\text{INIT}}$*	22	40	34	42	K6	65	62	G14	65	59	H15	65	77	J16	I/O
GND	GND	GND	GND	GND	23	41	35	43	J6	66	63	H12	55	19	J14	67	79	K15	GND
					26	47	43	53	L11	76	73	M13	69	76	P15	85	100	V18	XTL2 OR I/O
$\overline{\text{RESET}}$ (I)	$\overline{\text{RESET}}$ (I)	$\overline{\text{RESET}}$ (I)	$\overline{\text{RESET}}$ (I)	$\overline{\text{RESET}}$ (I)	27	48	44	54	K10	78	75	P14	71	78	R15	87	102	U17	$\overline{\text{RESET}}$ (I)
DONE	DONE	DONE	DONE	DONE	28	49	45	55	J10	80	77	N13	73	80	R14	89	107	V17	PROGRAM (I)
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)		50	46	56	K11	81	78	M12	74	81	N13	90	109	T16	I/O
					30	51	47	57	J11	82	79	P13	75	82	T14	91	110	U16	XTL1 OR I/O
		DATA 6 (I)	DATA 7 (I)	DATA 6 (I)		52	48	58	H10	83	80	N11	78	86	P12	96	115	U15	I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)		53	49	60	F10	87	84	M9	84	92	T11	102	122	U12	I/O
		$\overline{\text{CS0}}$ (I)				54	50	61	G10	88	85	N9	85	93	R10	103	123	V11	I/O
		DATA (4)	DATA (4)	DATA (4)		55	51	62	G11	89	86	N8	88	96	R9	108	128	U10	I/O
		DATA (3)	DATA (3)	DATA (3)		57	53	65	F11	92	89	N7	92	102	P8	112	132	T9	I/O
		$\overline{\text{CS1}}$ (I)				58	54	66	E11	93	90	P6	93	103	R8	113	133	U9	I/O
		DATA (2)	DATA (2)	DATA (2)		59	55	67	E10	94	91	M6	96	106	R7	118	138	V8	I/O
		DATA (1)	DATA (1)	DATA (1)		60	56	70	D10	98	95	M5	102	114	R5	124	145	U5	I/O
		RDY/$\overline{\text{BUSY}}$	$\overline{\text{RCLK}}$	$\overline{\text{RCLK}}$		61	57	71	C11	99	96	N4	103	115	P5	125	146	U4	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	38	62	58	72	B11	100	97	N2	106	119	R3	130	151	U3	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	39	63	59	73	C10	1	98	M3	107	120	N4	131	152	V2	I/O
CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (O)	40	64	60	74	A11	2	99	P1	108	121	R2	132	153	U2	CCLK (I)
		$\overline{\text{WS}}$ (I)	A0	A0		1	61	75	B10	5	2	M2	111	124	P2	135	161	T3	I/O
		CS2 (I)	A1	A1		2	62	76	B9	6	3	N1	112	125	M3	136	162	V1	I/O
			A2	A2		3	63	77	A10	8	5	L2	115	128	P1	140	165	R2	I/O
			A3	A3		4	64	78	A9	9	6	L1	116	129	N1	141	166	T1	I/O
			A15	A15			65	81	B6	12	9	K1	119	132	M1	146	172	N2	5
			A4	A4		5	66	82	B7	13	10	J2	120	133	L2	147	173	M4	I/O
			A14	A14		6	67	83	A7	14	11	H1	123	136	K2	150	178	L4	I/O
			A5	A5		7	68	84	C7	15	12	H2	124	137	K1	151	179	L2	I/O
			A13	A13		9	2	2	A6	17	14	G2	128	141	H2	156	184	K3	I/O
			A6	A6		10	3	3	A5	18	15	G1	129	142	H1	157	185	J1	I/O
			A12	A12		11	4	4	B5	19	16	F2	133	147	F2	164	192	G1	I/O
			A7	A7		12	5	5	C5	20	17	E1	134	148	E1	165	193	G4	I/O
			A11	A11		13	6	6	A3	23	20	D1	137	151	D1	169	199	F4	I/O
			A8	A8		14	7	9	A2	24	21	D2	138	152	C1	170	200	E2	I/O
			A10	A10		15	8	10	B3	25	22	B1	141	155	E3	173	203	E3	I/O
			A9	A9		16	9	11	A1	26	26	C2	142	156	C2	174	204	B1	I/O
																			All Others
							X	X	X	X									XC3x20A etc.
					X	X	X	X	X	X	X								XC3x30A etc.
								X	X	X	X	X	X						XC3x42A etc.
								X**				X	X						XC3x64A etc.
								X**					X	X	X	X	X		XC3x90A etc.
								X**						X	X		X		XC3195A

Notes:

Generic I/O pins are not shown.
For a detailed description of the configuration modes, see page 310 through page 319.
For pinout details, see page 327 through page 338.
▒▒ Represents a 50-kΩ to 100-kΩ pull-up before and during configuration.
* INIT is an open drain output during configuration.
(I) Represents an input.
** Pin assignment for the XC3064A/XC3090A and XC3195A differ from those shown.
*** Peripheral mode and master parallel mode are not supported in the PC44 package.
**** Pin assignments for the XC3195A PQ208 differ from those shown.
Pin assignments of PGA Footprint PLCC sockets and PGA packages are not indentical.
The information on this page is provided as a convenient summary. For detailed pin descriptions, see the preceding two pages.

Note: Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50-kW to 100-kW pull-up resistor.

XC3000 Series Pin Assignments

Xilinx offers the six different array sizes in the XC3000 families in a variety of surface-mount and through-hole package types, with pin counts from 44 to 223.

Each chip is offered in several package types to accommodate the available PC board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without the need for PC board changes.

Note that there is no perfect match between the number of bonding pads on the chip and the number of pins on a package. In some cases, the chip has more pads than there are pins on the package, as indicated by the information ("unused" pads) below the line in the following table. The IOBs of the unconnected pads can still be used as storage elements if the specified propagation delays and set-up times are acceptable.

In other cases, the chip has fewer pads than there are pins on the package; therefore, some package pins are not connected (n.c.), as shown above the line in the following table.

Number of Unbounded or Unconnected Pins

		Number of Package Pins											
Device	**Pads**	**44**	**64**	**68**	**84**	**100**	**132**	**144**	**160**	**175**	**176**	**208**	**223**
3020A	74	—	—	6 u	10 n.c.	26 n.c.	—	—	—	—	—	—	—
3030A	98	54 u	34 u	30 u	14 u	2 n.c.	—	—	—	—	—	—	—
3042A	118	—	—	—	34 u	18 u	14 n.c.	26 n.c.	—	—	—	—	—
3064A	142	—	—	—	50 u	—	10 u	2 u	18 n.c.	—	—	—	—
3090A	166	—	—	—	82 u	—	—	—	6 u	9 n.c	10 n.c.	42 n.c.	—
3195A	198	—	—	—	114 u	—	—	—	—	9 n.c. 32 u	—	10 n.c.	25 n.c.

n.c. = Unconnected package pin
u = Unbonded device pad

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Number of Available I/O Pins

		Number of Package Pins																
	Max I/O	**44**	**64**	**68**	**84**	**100**	**120**	**132**	**144**	**156**	**160**	**164**	**175**	**176**	**191**	**196**	**208**	**223**	**240**
XC3020A/XC3120A	64			58	64	64													
XC3030A/XC3130A	80	34	54	58	74	80													
XC3042A/XC3142A	96				74	82		96	96										
XC3064A/XC3164A	120				70			110	110		120								
XC3090A/XC3190A	144				70				120		138	144	144	144			144		
XC3195A	176				70						138		144				176	176	

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XC3000 Series 44-Pin PLCC Pinouts

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	GND
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	PWRDWN
8	TCLKIN-I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	M1-RDATA
17	M0-RTRIG
18	M2-I/O
19	HDC-I/O
20	LDC-I/O
21	I/O
22	$\overline{\text{INIT}}$-I/O

Pin No.	XC3030A
23	GND
24	I/O
25	I/O
26	XTL2(IN)-I/O
27	RESET
28	DONE-PGM
29	I/O
30	XTL1(OUT)-BCLK-I/O
31	I/O
32	I/O
33	I/O
34	VCC
35	I/O
36	I/O
37	I/O
38	DIN-I/O
39	DOUT-I/O
40	CCLK
41	I/O
42	I/O
43	I/O
44	I/O

Peripheral mode and Master Parallel mode are not supported in the PC44 package

XC3000 Series 64-Pin Plastic VQFP Pinouts

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	A0-$\overline{WS}$-I/O
2	A1-CS2-I/O
3	A2-I/O
4	A3-I/O
5	A4-I/O
6	A14-I/O
7	A5-I/O
8	**GND**
9	A13-I/O
10	A6-I/O
11	A12-I/O
12	A7-I/O
13	A11-I/O
14	A8-I/O
15	A10-I/O
16	A9-I/O
17	$\overline{PWRDN}$
18	TCLKIN-I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	**VCC**
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-$\overline{RDATA}$
32	M0-RTRIG

Pin No.	XC3030A
33	M2-I/O
34	HDC-I/O
35	I/O
36	$\overline{LDC}$-I/O
37	I/O
38	I/O
39	I/O
40	$\overline{INIT}$-I/O
41	**GND**
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	XTAL2(IN)-I/O
48	$\overline{RESET}$
49	DONE-$\overline{PG}$
50	D7-I/O
51	XTAL1(OUT)-BCLKIN-I/O
52	D6-I/O
53	D5-I/O
54	$\overline{CS0}$-I/O
55	D4-I/O
56	VCC
57	D3-I/O
58	$\overline{CS1}$-I/O
59	D2-I/O
60	D1-I/O
61	RDY/$\overline{BUSY}$-$\overline{RCLK}$-I/O
62	D0-DIN-I/O
63	DOUT-I/O
64	CCLK

XC3000 Series 68-Pin PLCC, 84-Pin PLCC and PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC	84 PGA
XC3030A	XC3020A			
10	10	$\overline{\text{PWRDN}}$	12	B2
11	11	TCLKIN-I/O	13	C2
12	—	I/O*	14	B1
13	12	I/O	15	C1
14	13	I/O	16	D2
—	—	I/O	17	D1
15	14	I/O	18	E3
16	15	I/O	19	E2
—	16	I/O	20	E1
17	17	I/O	21	F2
18	18	VCC	22	F3
19	19	I/O	23	G3
—	—	I/O	24	G1
20	20	I/O	25	G2
—	21	I/O	26	F1
21	22	I/O	27	H1
22	—	I/O	28	H2
23	23	I/O	29	J1
24	24	I/O	30	K1
25	25	M1-$\overline{\text{RDATA}}$	31	J2
26	26	M0-RTRIG	32	L1
27	27	M2-I/O	33	K2
28	28	HDC-I/O	34	K3
29	29	I/O	35	L2
30	30	$\overline{\text{LDC}}$-I/O	36	L3
—	31	I/O	37	K4
—		I/O*	38	L4
31	32	I/O	39	J5
32	33	I/O	40	K5
33	—	I/O*	41	L5
34	34	$\overline{\text{INIT}}$-I/O	42	K6
35	35	GND	43	J6
36	36	I/O	44	J7
37	37	I/O	45	L7
38	38	I/O	46	K7
39	39	I/O	47	L6
—	40	I/O	48	L8
—	41	I/O	49	K8
40		I/O*	50	L9
41		I/O*	51	L10
42	42	I/O	52	K9
43	43	XTL2(IN)-I/O	53	L11

68 PLCC XC3030A XC3020A	XC3020A, XC3030A, XC3042A	84 PLCC	84 PGA	XC3020A
44	$\overline{\text{RESET}}$	54	K10	44
45	DONE-$\overline{\text{PG}}$	55	J10	45
46	D7-I/O	56	K11	46
47	XTL1(OUT)-BCLKIN-I/O	57	J11	47
48	D6-I/O	58	H10	48
—	I/O	59	H11	—
49	D5-I/O	60	F10	49
50	$\overline{\text{CS0}}$-I/O	61	G10	50
51	D4-I/O	62	G11	51
—	I/O	63	G9	—
52	VCC	64	F9	52
53	D3-I/O	65	F11	53
54	$\overline{\text{CS1}}$-I/O	66	E11	54
55	D2-I/O	67	E10	55
—	I/O	68	E9	—
—	I/O*	69	D11	—
56	D1-I/O	70	D10	56
57	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O	71	C11	57
58	D0-DIN-I/O	72	B11	58
59	DOUT-I/O	73	C10	59
60	CCLK	74	A11	60
61	A0-$\overline{\text{WS}}$-I/O	75	B10	61
62	A1-CS2-I/O	76	B9	62
63	A2-I/O	77	A10	63
64	A3-I/O	78	A9	64
—	I/O*	79	B8	—
—	I/O*	80	A8	—
65	A15-I/O	81	B6	65
66	A4-I/O	82	B7	66
67	A14-I/O	83	A7	67
68	A5-I/O	84	C7	68
1	GND	1	C6	1
2	A13-I/O	2	A6	2
3	A6-I/O	3	A5	3
4	A12-I/O	4	B5	4
5	A7-I/O	5	C5	5
—	I/O*	6	A4	—
—	I/O*	7	B4	—
6	A11-I/O	8	A3	6
7	A8-I/O	9	A2	7
8	A10-I/O	10	B3	8
9	A9-I/O	11	A1	9

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of three different chips in three different packages. The pin-description column lists 84 of the 118 pads on the XC3042A (and 84 of the 98 pads on the XC3030A) that are connected to the 84 package pins. Ten pads, indicated by an asterisk, do not exist on the XC3020A, which has 74 pads; therefore the corresponding pins on the 84-pin packages have no connections to an XC3020A. Six pads on the XC3020A and 16 pads on the XC3030A, indicated by a dash (—) in the 68 PLCC column, have no connection to the 68 PLCC, but are connected to the 84-pin packages.

XC3064A/XC3090A/XC3195A 84-Pin PLCC Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PLCC Pin Number	XC3064A, XC3090A, XC3195A
12	$\overline{\text{PWRDN}}$
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND*
22	VCC
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-$\overline{\text{RDATA}}$
32	M0-RTRIG
33	M2-I/O
34	HDC-I/O
35	I/O
36	$\overline{\text{LDC}}$-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	VCC*
43	GND
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3064A, XC3090A, XC3195A
54	$\overline{\text{RESET}}$
55	DONE-$\overline{\text{PG}}$
56	D7-I/O
57	XTL1(OUT)-BCLKIN-I/O
58	D6-I/O
59	I/O
60	D5-I/O
61	$\overline{\text{CS0}}$-I/O
62	D4-I/O
63	I/O
64	VCC
65	GND*
66	D3-I/O*
67	$\overline{\text{CS1}}$-I/O*
68	D2-I/O*
69	I/O
70	D1-I/O
71	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
72	D0-DIN-I/O
73	DOUT-I/O
74	CCLK
75	A0-$\overline{\text{WS}}$-I/O
76	A1-CS2-I/O
77	A2-I/O
78	A3-I/O
79	I/O
80	I/O
81	A15-I/O
82	A4-I/O
83	A14-I/O
84	A5-I/O
1	GND
2	VCC*
3	A13-I/O*
4	A6-I/O*
5	A12-I/O*
6	A7-I/O*
7	I/O
8	A11-I/O
9	A8-I/O
10	A10-I/O
11	A9-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In the PC84 package, XC3064A, XC3090A and XC3195A have additional VCC and GND pins and thus a different pin definition than XC3020A/XC3030A/XC3042A.

XC3000 Series 100-Pin QFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin No.			XC3020A XC3030A XC3042A
CQFP	PQFP	TQFP VQFP	
1	16	13	GND
2	17	14	A13-I/O
3	18	15	A6-I/O
4	19	16	A12-I/O
5	20	17	A7-I/O
6	21	18	I/O*
7	22	19	I/O*
8	23	20	A11-I/O
9	24	21	A8-I/O
10	25	22	A10-I/O
11	26	23	A9-I/O
12	27	24	VCC*
13	28	25	GND*
14	29	26	$\overline{\text{PWRDN}}$
15	30	27	TCLKIN-I/O
16	31	28	I/O**
17	32	29	I/O*
18	33	30	I/O*
19	34	31	I/O
20	35	32	I/O
21	36	33	I/O
22	37	34	I/O
23	38	35	I/O
24	39	36	I/O
25	40	37	I/O
26	41	38	VCC
27	42	39	I/O
28	43	40	I/O
29	44	41	I/O
30	45	42	I/O
31	46	43	I/O
32	47	44	I/O
33	48	45	I/O
34	49	46	I/O
35	50	47	I/O*
36	51	48	I/O*
37	52	49	M1-$\overline{\text{RD}}$
38	53	50	GND*
39	54	51	MO-RT
40	55	52	VCC*
41	56	53	M2-I/O
42	57	54	HDC-I/O
43	58	55	I/O
44	59	56	$\overline{\text{LDC}}$-I/O
45	60	57	I/O*
46	61	58	I/O*
47	62	59	I/O
48	63	60	I/O
49	64	61	I/O
50	65	62	$\overline{\text{INIT}}$-I/O
51	66	63	GND
52	67	64	I/O
53	68	65	I/O
54	69	66	I/O
55	70	67	I/O
56	71	68	I/O
57	72	69	I/O
58	73	70	I/O
59	74	71	I/O*
60	75	72	I/O*
61	76	73	XTL2-I/O
62	77	74	GND*
63	78	75	$\overline{\text{RESET}}$
64	79	76	VCC*
65	80	77	DONE-$\overline{\text{PG}}$
66	81	78	D7-I/O
67	82	79	BCLKIN-XTL1-I/O
68	83	80	D6-I/O
69	84	81	I/O*
70	85	82	I/O*
71	86	83	I/O
72	87	84	D5-I/O
73	88	85	$\overline{\text{CS0}}$-I/O
74	89	86	D4-I/O
75	90	87	I/O
76	91	88	VCC
77	92	89	D3-I/O
78	93	90	$\overline{\text{CS1}}$-I/O
79	94	91	D2-I/O
80	95	92	I/O
81	96	93	I/O*
82	97	94	I/O*
83	98	95	D1-I/O
84	99	96	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
85	100	97	DO-DIN-I/O
86	1	98	DOUT-I/O
87	2	99	CCLK
88	3	100	VCC*
89	4	1	GND*
90	5	2	AO-$\overline{\text{WS}}$-I/O
91	6	3	A1-CS2-I/O
92	7	4	I/O**
93	8	5	A2-I/O
94	9	6	A3-I/O
95	10	7	I/O*
96	11	8	I/O*
97	12	9	A15-I/O
98	13	10	A4-I/O
99	14	11	A14-I/O
100	15	12	A5-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* This table describes the pinouts of three different chips in three different packages. The pin-description column lists 100 of the 118 pads on the XC3042A that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3030A, which has 98 pads; therefore the corresponding pins have no connections. Twenty-six pads, indicated by single or double asterisks, do not exist on the XC3020A, which has 74 pads; therefore, the corresponding pins have no connections. (See table on page 326.)

XC3000 Series 132-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA Pin Number	XC3042A XC3064A
C4	GND
A1	$\overline{\text{PWRDN}}$
C3	I/O-TCLKIN
B2	I/O
B3	I/O
A2	I/O*
B4	I/O
C5	I/O
A3	I/O*
A4	I/O
B5	I/O
C6	I/O
A5	I/O
B6	I/O
A6	I/O
B7	I/O
C7	GND
C8	VCC
A7	I/O
B8	I/O
A8	I/O
A9	I/O
B9	I/O
C9	I/O
A10	I/O
B10	I/O
A11	I/O*
C10	I/O
B11	I/O
A12	I/O*
B12	I/O
A13	I/O*
C12	I/O

PGA Pin Number	XC3042A XC3064A
B13	M1-$\overline{\text{RD}}$
C11	GND
A14	M0-RT
D12	VCC
C13	M2-I/O
B14	HDC-I/O
C14	I/O
E12	I/O
D13	I/O
D14	$\overline{\text{LDC}}$-I/O
E13	I/O*
F12	I/O
E14	I/O
F13	I/O
F14	I/O
G13	I/O
G14	$\overline{\text{INIT}}$-I/O
G12	VCC
H12	GND
H14	I/O
H13	I/O
J14	I/O
J13	I/O
K14	I/O
J12	I/O
K13	I/O
L14	I/O*
L13	I/O
K12	I/O
M14	I/O
N14	I/O
M13	XTL2(IN)-I/O
L12	GND

PGA Pin Number	XC3042A XC3064A
P14	$\overline{\text{RESET}}$
M11	VCC
N13	DONE-$\overline{\text{PG}}$
M12	D7-I/O
P13	XTL1-I/O-BCLKIN
N12	I/O
P12	I/O
N11	D6-I/O
M10	I/O
P11	I/O*
N10	I/O
P10	I/O
M9	D5-I/O
N9	$\overline{\text{CS0}}$-I/O
P9	I/O*
P8	I/O*
N8	D4-I/O
P7	I/O
M8	VCC
M7	GND
N7	D3-I/O
P6	$\overline{\text{CS1}}$-I/O
N6	I/O*
P5	I/O*
M6	D2-I/O
N5	I/O
P4	I/O
P3	I/O
M5	D1-I/O
N4	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
P2	I/O
N3	I/O
N2	D0-DIN-I/O

PGA Pin Number	XC3042A XC3064A
M3	DOUT-I/O
P1	CCLK
M4	VCC
L3	GND
M2	A0-$\overline{\text{WS}}$-I/O
N1	A1-CS2-I/O
M1	I/O
K3	I/O
L2	A2-I/O
L1	A3-I/O
K2	I/O
J3	I/O
K1	A15-I/O
J2	A4-I/O
J1	I/O*
H1	A14-I/O
H2	A5-I/O
H3	GND
G3	VCC
G2	A13-I/O
G1	A6-I/O
F1	I/O*
F2	A12-I/O
E1	A7-I/O
F3	I/O
E2	I/O
D1	A11-I/O
D2	A8-I/O
E3	I/O
C1	I/O
B1	A10-I/O
C2	A9-I/O
D3	VCC

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

*Indicates unconnected package pins (14) for the XC3042A.

XC3000 Series 144-Pin Plastic TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3042A XC3064A XC3090A
1	PWRDN
2	I/O-TCLKIN
3	I/O*
4	I/O
5	I/O
6	I/O*
7	I/O
8	I/O
9	I/O*
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O*
16	I/O
17	I/O
18	GND
19	VCC
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O*
29	I/O
30	I/O
31	I/O*
32	I/O*
33	I/O
34	I/O*
35	I/O
36	M1-RD
37	GND
38	MO-RT
39	VCC
40	M2-I/O
41	HDC-I/O
42	I/O
43	I/O
44	I/O
45	LDC-I/O
46	I/O*
47	I/O
48	I/O

Pin Number	XC3042A XC3064A XC3090A
49	I/O
50	I/O*
51	I/O
52	I/O
53	INIT-I/O
54	VCC
55	GND
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O*
64	I/O*
65	I/O
66	I/O
67	I/O
68	I/O
69	XTL2(IN)-I/O
70	GND
71	RESET
72	VCC
73	DONE-PG
74	D7-I/O
75	XTL1(OUT)-BCLKIN-I/O
76	I/O
77	I/O
78	D6-I/O
79	I/O
80	I/O*
81	I/O
82	I/O
83	I/O*
84	D5-I/O
85	CS0-I/O
86	I/O*
87	I/O*
88	D4-I/O
89	I/O
90	VCC
91	GND
92	D3-I/O
93	CS1-I/O
94	I/O*
95	I/O*
96	D2-I/O

Pin Number	XC3042A XC3064A XC3090A
97	I/O
98	I/O
99	I/O*
100	I/O
101	I/O*
102	D1-I/O
103	RDY/BUSY-RCLK-I/O
104	I/O
105	I/O
106	D0-DIN-I/O
107	DOUT-I/O
108	CCLK
109	VCC
110	GND
111	A0-WSI/O
112	A1-CS2-I/O
113	I/O
114	I/O
115	A2-I/O
116	A3-I/O
117	I/O
118	I/O
119	A15-I/O
120	A4-I/O
121	I/O*
122	I/O*
123	A14-I/O
124	A5-I/O
125	I/O (XC3090 only)
126	GND
127	VCC
128	A13-I/O
129	A6-I/O
130	I/O*
131	I/O (XC3090 only)
132	I/O*
133	A12-I/O
134	A7-I/O
135	I/O
136	I/O
137	A11-I/O
138	A8-I/O
139	I/O
140	I/O
141	A10-I/O
142	A9-I/O
143	VCC
144	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* Indicates unconnected package pins (24) for the XC3042A.

XC3000 Series 160-Pin PQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PQFP Pin Number	XC3064A, XC3090A, XC3195A
1	I/O*
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	GND
20	VCC
21	I/O*
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O*
39	I/O*
40	M1-$\overline{\text{RDATA}}$

PQFP Pin Number	XC3064A, XC3090A, XC3195A
41	GND
42	M0–RTRIG
43	VCC
44	M2-I/O
45	HDC-I/O
46	I/O
47	I/O
48	I/O
49	$\overline{\text{LDC}}$-I/O
50	I/O*
51	I/O*
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	$\overline{\text{INIT}}$-I/O
60	VCC
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O*
76	XTL2-I/O
77	GND
78	$\overline{\text{RESET}}$
79	VCC
80	DONE/$\overline{\text{PG}}$

PQFP Pin Number	XC3064A, XC3090A, XC3195A
81	D7-I/O
82	XTL1-I/O-BCLKIN
83	I/O*
84	I/O
85	I/O
86	D6-I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	D5-I/O
93	$\overline{\text{CS0}}$-I/O
94	I/O*
95	I/O*
96	I/O
97	I/O
98	D4-I/O
99	I/O
100	VCC
101	GND
102	D3-I/O
103	$\overline{\text{CS1}}$-I/O
104	I/O
105	I/O
106	I/O*
107	I/O*
108	D2-I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	D1-I/O
115	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
116	I/O
117	I/O
118	I/O*
119	D0-DIN-I/O
120	DOUT-I/O

PQFP Pin Number	XC3064A, XC3090A, XC3195A
121	CCLK
122	VCC
123	GND
124	A0-$\overline{\text{WS}}$-I/O
125	A1-CS2-I/O
126	I/O
127	I/O
128	A2-I/O
129	A3-I/O
130	I/O
131	I/O
132	A15-I/O
133	A4-I/O
134	I/O
135	I/O
136	A14-I/O
137	A5-I/O
138	I/O*
139	GND
140	VCC
141	A13-I/O
142	A6-I/O
143	I/O*
144	I/O*
145	I/O
146	I/O
147	A12-I/O
148	A7-I/O
149	I/O
150	I/O
151	A11-I/O
152	A8-I/O
153	I/O
154	I/O
155	A10-I/O
156	A9-I/O
157	VCC
158	GND
159	$\overline{\text{PWRDWN}}$
160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

*Indicates unconnected package pins (18) for the XC3064A.

XC3000 Series 175-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA Pin Number	XC3090A, XC3195A
B2	$\overline{\text{PWRDN}}$
D4	TCLKIN-I/O
B3	I/O
C4	I/O
B4	I/O
A4	I/O
D5	I/O
C5	I/O
B5	I/O
A5	I/O
C6	I/O
D6	I/O
B6	I/O
A6	I/O
B7	I/O
C7	I/O
D7	I/O
A7	I/O
A8	I/O
B8	I/O
C8	I/O
D8	GND
D9	VCC
C9	I/O
B9	I/O
A9	I/O
A10	I/O
D10	I/O
C10	I/O
B10	I/O
A11	I/O
B11	I/O
D11	I/O
C11	I/O
A12	I/O
B12	I/O
C12	I/O
D12	I/O
A13	I/O
B13	I/O
C13	I/O
A14	I/O

PGA Pin Number	XC3090A, XC3195A
D13	I/O
B14	M1-$\overline{\text{RDATA}}$
C14	GND
B15	M0-RTRIG
D14	VCC
C15	M2-I/O
E14	HDC-I/O
B16	I/O
D15	I/O
C16	I/O
D16	$\overline{\text{LDC}}$-I/O
F14	I/O
E15	I/O
E16	I/O
F15	I/O
F16	I/O
G14	I/O
G15	I/O
G16	I/O
H16	I/O
H15	$\overline{\text{INIT}}$-I/O
H14	VCC
J14	GND
J15	I/O
J16	I/O
K16	I/O
K15	I/O
K14	I/O
L16	I/O
L15	I/O
M16	I/O
M15	I/O
L14	I/O
N16	I/O
P16	I/O
N15	I/O
R16	I/O
M14	I/O
P15	XTL2(IN)-I/O
N14	GND
R15	$\overline{\text{RESET}}$
P14	VCC

PGA Pin Number	XC3090A, XC3195A
R14	DONE-$\overline{\text{PG}}$
N13	D7-I/O
T14	XTL1(OUT)-BCLKIN-I/O
P13	I/O
R13	I/O
T13	I/O
N12	I/O
P12	D6-I/O
R12	I/O
T12	I/O
P11	I/O
N11	I/O
R11	I/O
T11	D5-I/O
R10	$\overline{\text{CS0}}$-I/O
P10	I/O
N10	I/O
T10	I/O
T9	I/O
R9	D4-I/O
P9	I/O
N9	VCC
N8	GND
P8	D3-I/O
R8	$\overline{\text{CS1}}$-I/O
T8	I/O
T7	I/O
N7	I/O
P7	I/O
R7	D2-I/O
T6	I/O
R6	I/O
N6	I/O
P6	I/O
T5	I/O
R5	D1-I/O
P5	RDY/$\overline{\text{BUSY}}$-RCLK-I/O
N5	I/O
T4	I/O
R4	I/O
P4	I/O
R3	D0-DIN-I/O

PGA Pin Number	XC3090A, XC3195A
N4	DOUT-I/O
R2	CCLK
P3	VCC
N3	GND
P2	A0-$\overline{\text{WS}}$-I/O
M3	A1-CS2-I/O
R1	I/O
N2	I/O
P1	A2-I/O
N1	A3-I/O
L3	I/O
M2	I/O
M1	A15-I/O
L2	A4-I/O
L1	I/O
K3	I/O
K2	A14-I/O
K1	A5-I/O
J1	I/O
J2	I/O
J3	GND
H3	VCC
H2	A13-I/O
H1	A6-I/O
G1	I/O
G2	I/O
G3	I/O
F1	I/O
F2	A12-I/O
E1	A7-I/O
E2	I/O
F3	I/O
D1	A11-I/O
C1	A8-I/O
D2	I/O
B1	I/O
E3	A10-I/O
C2	A9-I/O
D3	VCC
C3	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected. Pin A1 does not exist.

XC3000 Series 176-Pin TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3090A
1	PWRDWN
2	TCLKIN-I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	VCC
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	–

Pin Number	XC3090A
45	M1-RDATA
46	GND
47	M0-RTRIG
48	VCC
49	M2-I/O
50	HDC-I/O
51	I/O
52	I/O
53	I/O
54	LDC-I/O
55	–
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	INIT-I/O
66	VCC
67	GND
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	–
83	–
84	I/O
85	XTAL2(IN)-I/O
86	GND
87	RESET
88	VCC

Pin Number	XC3090A
89	DONE-PG
90	D7-I/O
91	XTAL1(OUT)-BCLKIN-I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	D6-I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	D5-I/O
103	CS0-I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	D4-I/O
109	I/O
110	VCC
111	GND
112	D3-I/O
113	CS1-I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	D2-I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	D1-I/O
125	RDY/BUSY-RCLK-I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	D0-DIN-I/O
131	DOUT-I/O
132	CCLK

Pin Number	XC3090A
133	VCC
134	GND
135	A0-WS-I/O
136	A1-CS2-I/O
137	–
138	I/O
139	I/O
140	A2-I/O
141	A3-I/O
142	–
143	–
144	I/O
145	I/O
146	A15-I/O
147	A4-I/O
148	I/O
149	I/O
150	A14-I/O
151	A5-I/O
152	I/O
153	I/O
154	GND
155	VCC
156	A13-I/O
157	A6-I/O
158	I/O
159	I/O
160	–
161	–
162	I/O
163	I/O
164	A12-I/O
165	A7-I/O
166	I/O
167	I/O
168	–
169	A11-I/O
170	A8-I/O
171	I/O
172	I/O
173	A10-I/O
174	A9-I/O
175	VCC
176	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3000 Series 208-Pin PQFP Pinouts

XC3000A, and XC3000L families have identical pinouts

Pin Number	XC3090A
1	–
2	GND
3	$\overline{\text{PWRDWN}}$
4	TCLKIN-I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	–
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	GND
26	VCC
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	–
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	M1-$\overline{\text{RDATA}}$
49	GND
50	M0-RTRIG
51	–
52	–

Pin Number	XC3090A
53	–
54	–
55	VCC
56	M2-I/O
57	HDC-I/O
58	I/O
59	I/O
60	I/O
61	$\overline{\text{LDC}}$-I/O
62	I/O
63	I/O
64	–
65	–
66	–
67	–
68	I/O
69	I/O
70	I/O
71	I/O
72	–
73	–
74	I/O
75	I/O
76	I/O
77	$\overline{\text{INIT}}$-I/O
78	VCC
79	GND
80	I/O
81	I/O
82	I/O
83	–
84	–
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	–
91	–
92	–
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	XTL2-I/O
101	GND
102	$\overline{\text{RESET}}$
103	–
104	–

Pin Number	XC3090A
105	–
106	VCC
107	D/$\overline{\text{P}}$
108	–
109	D7-I/O
110	XTL1-BCLKIN-I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	D6-I/O
116	I/O
117	I/O
118	I/O
119	–
120	I/O
121	I/O
122	D5-I/O
123	$\overline{\text{CS0}}$-I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	D4-I/O
129	I/O
130	VCC
131	GND
132	D3-I/O
133	$\overline{\text{CS1}}$-I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	D2-I/O
139	I/O
140	I/O
141	I/O
142	–
143	I/O
144	I/O
145	D1-I/O
146	RDY/$\overline{\text{BUSY}}$-RCLK-I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	DIN-D0-I/O
152	DOUT-I/O
153	CCLK
154	VCC
155	–
156	–

Pin Number	XC3090A
157	–
158	–
159	–
160	GND
161	$\overline{\text{WS}}$-A0-I/O
162	CS2-A1-I/O
163	I/O
164	I/O
165	A2-I/O
166	A3-I/O
167	I/O
168	I/O
169	–
170	–
171	–
172	A15-I/O
173	A4-I/O
174	I/O
175	I/O
176	–
177	–
178	A14-I/O
179	A5-I/O
180	I/O
181	I/O
182	GND
183	VCC
184	A13-I/O
185	A6-I/O
186	I/O
187	I/O
188	–
189	–
190	I/O
191	I/O
192	A12-I/O
193	A7-I/O
194	–
195	–
196	–
197	I/O
198	I/O
199	A11-I/O
200	A8-I/O
201	I/O
202	I/O
203	A10-I/O
204	A9-I/O
205	VCC
206	–
207	–
208	–

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

*In PQ208, XC3090A and XC3195A have different pinouts.

XC3195A PQ208 and PG223 Pinouts

Pin Description	PG223	PQ208
A9-I/O	B1	206
A10-I/O	E3	205
I/O	E4	204
I/O	C2	203
I/O	C1	202
I/O	D2	201
A8-I/O	E2	200
A11-I/O	F4	199
I/O	F3	198
I/O	D1	197
I/O	F2	196
I/O	G2	194
A7-I/O	G4	193
A12-I/O	G1	192
I/O	H2	191
I/O	H3	190
I/O	H1	189
I/O	H4	188
I/O	J3	187
I/O	J2	186
A6-I/O	J1	185
A13-I/O	K3	184
VCC	J4	183
GND	K4	182
I/O	K2	181
I/O	K1	180
A5-I/O	L2	179
A14-I/O	L4	178
I/O	L3	177
I/O	L1	176
I/O	M1	175
I/O	M2	174
A4-I/O	M4	173
A15-I/O	N2	172
I/O	N3	171
I/O	P2	169
I/O	R1	168
I/O	N4	167
A3-I/O	T1	166
A2-I/O	R2	165
I/O	P3	164
I/O	T2	163
I/O	P4	162
I/O	U1	161
A1-CS2-I/O	V1	160
A0-$\overline{WS}$-I/O	T3	159
GND	R3	158
VCC	R4	157
CCLK	U2	156
DOUT-I/O	V2	155

Pin Description	PG223	PQ208
D0-DIN-I/O	U3	154
I/O	V3	153
I/O	R5	152
I/O	T4	151
I/O	V4	150
RDY/BUSY-RCLK-I/O	U4	149
D1-I/O	U5	148
I/O	R6	147
I/O	T5	146
I/O	U6	145
I/O	T6	144
I/O	V7	141
I/O	R7	140
I/O	U7	139
D2-I/O	V8	138
I/O	U8	137
I/O	T8	136
I/O	R8	135
I/O	V9	134
$\overline{CS1}$-I/O	U9	133
D3-I/O	T9	132
GND	R9	131
VCC	R10	130
I/O	T10	129
D4-I/O	U10	128
I/O	V10	127
I/O	R11	126
I/O	T11	125
I/O	U11	124
$\overline{CS0}$-I/O	V11	123
D5-I/O	U12	122
I/O	R12	121
I/O	V12	120
I/O	T13	119
I/O	U13	118
I/O	T14	117
I/O	R13	116
I/O	U14	115
D6-I/O	U15	114
I/O	V15	113
I/O	T15	112
I/O	R14	111
I/O	V16	110
XTLX1(OUT)BCLKN-I/O	U16	109
D7-I/O	T16	108
D/$\overline{P}$	V17	107
VCC	R15	106
$\overline{RESET}$	U17	105
GND	R16	104
XTL2(IN)-I/O	V18	103

Pin Description	PG223	PQ208
I/O	U18	102
I/O	P15	101
I/O	T17	100
I/O	T18	99
I/O	P16	98
I/O	R17	97
I/O	N15	96
I/O	R18	95
I/O	P17	94
I/O	N17	93
I/O	N16	92
I/O	M15	89
I/O	M18	88
I/O	M17	87
I/O	L18	86
I/O	L17	85
I/O	L15	84
I/O	L16	83
I/O	K18	82
I/O	K17	81
I/O	K16	80
GND	K15	79
VCC	J15	78
$\overline{INIT}$	J16	77
I/O	J17	76
I/O	J18	75
I/O	H16	74
I/O	H15	73
I/O	H17	72
I/O	H18	71
I/O	G17	70
I/O	G18	69
I/O	G15	68
I/O	F16	67
I/O	F17	66
I/O	E17	63
I/O	C18	62
I/O	F15	61
I/O	D17	60
$\overline{LDC}$-I/O	E16	59
I/O	C17	58
I/O	B18	57
I/O	E15	56
HDC-I/O	A18	55
M2-I/O	A17	54
VCC	D16	53
M0-RTIG	B17	52
GND	D15	51
M1/$\overline{RDATA}$	C16	50
I/O	B16	49

Pin Description	PG223	PQ208
I/O	A16	48
I/O	D14	47
I/O	C15	46
I/O	B15	45
I/O	A15	44
I/O	C14	43
I/O	D13	42
I/O	B14	41
I/O	C13	40
I/O	B13	39
I/O	B12	38
I/O	D12	37
I/O	A12	36
I/O	B11	35
I/O	C11	34
I/O	A11	33
I/O	D11	32
I/O	A10	31
I/O	B10	30
I/O	C10	29
I/O	C9	28
VCC	D10	27
GND	D9	26
I/O	B9	25
I/O	A9	24
I/O	C8	23
I/O	D8	22
I/O	B8	21
I/O	A8	20
I/O	B7	19
I/O	A7	18
I/O	D7	17
I/O	B6	14
I/O	C6	13
I/O	B5	12
I/O	A4	11
I/O	D6	10
I/O	C5	9
I/O	B4	8
I/O	B3	7
I/O	C4	6
I/O	D5	5
I/O	C3	4
I/O	A3	3
TCLKIN-I/O	A2	2
$\overline{PWRDN}$	B2	1
GND	D4	208
VCC	D3	207

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.
In the PQ208 package, pins 15, 16, 64, 65, 90, 91, 142, 143, 170 and 195 are not connected.
In the PG223 package, the following pins are not connected: A5, A6, A13, A14, D18, E1, E18, F1, F18, N1, N18, P1, P18, V5, V6, V13, and V14.
*In PQ208, XC3090A and XC3195A have different pinouts.

Product Availability

Pins		44	64	68	84		100				132		144	160	164	175		176	208	223
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast.P QFP	Plast. TQFP	Plast. VQFP	Top-Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Top-Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Cer. PGA
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3020A	-7			CI	CI	CI	CI													
	-6			C	C	C	C													
XC3030A	-7	CI	CI	CI	CI	CI	CI		CI											
	-6	C	C	C	C	C	C		C											
XC3042A	-7				CI	CI	CI		CI		CI	CI	CI							
	-6				C	C	C		C		C	C	C							
XC3064A	-7				CI						CI	CI	CI	CI						
	-6				C						C	C	C	C						
XC3090A	-7				CI								CI	CI		CI	CI	CI	CI	
	-6				C								C	C		C	C	C	C	
XC3020L	-8				C															
XC3030L	-8		C		C				C											
XC3042L	-8				C				C				C							
XC3064L	-8				C								C							
XC3090L	-8				C								C					C		
XC3120A	-5			CI	CI	CI	CI													
	-4			CI	CI	CI	CI													
	-3			CI	CI	CI	CI													
	-2			CI	CI	CI	CI													
	-1			C	C	C	C													
	-09			C	C	C	C													
XC3130A	-5	CI	CI	CI	CI	CI	CI		CI											
	-4	CI	CI	CI	CI	CI	CI		CI											
	-3	CI	CI	CI	CI	CI	CI		CI											
	-2	CI	CI	CI	CI	CI	CI		CI											
	-1	C	C	C	C	C	C		C											
	-09	C	C	C	C	C	C		C											
XC3142A	-5				CI	CIMB	CI		C	MB	C	CIMB	CI							
	-4				CI	CI	CI		C		C	CI	CI							
	-3				CI	CI	CI		CI		CI	CI	CI							
	-2				CI	CI	CI		CI		CI	CI	CI							
	-1				C	C	C		C		C	C	C							
	-09				C	C	C		C		C	C	C							
XC3164A	-5				CI						CI	CI	CI	CI						
	-4				CI						CI	CI	CI	CI						
	-3				CI						CI	CI	CI	CI						
	-2				CI						CI	CI	CI	CI						
	-1				C						C	C	C	C						
	-09				C						C	C	C	C						
XC3190A	-5				CI									CI	MB	CI	CIMB	CI	CI	
	-4				CI									CI		CI	CI	CI	CI	
	-3				CI									CI		CI	CI	CI	CI	
	-2				CI									CI		CI	CI	CI	CI	
	-1				C									C		C	C	C	C	
	-09				C									C		C	C	C	C	
XC3195A	-5				CI									CI	MB	CI	CIMB		CI	CIMB
	-4				CI									CI		CI	CI		CI	CI
	-3				CI									CI		CI	CI		CI	CI
	-2				CI									CI		CI	CI		CI	CI
	-1				C									C		C	C		C	C
	-09				C									C		C	C		C	C

Pins		44	64	68	84		100				132		144	160	164	175		176	208	223
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast.P QFP	Plast. TQFP	Plast. VQFP	Top-Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Top-Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Cer. PGA
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3142L	-3*				C				C				C							
	-2*				C				C				C							
XC3190L	-3*				C								C					C		
	-2*				C								C					C		

Notes: * Advance Information

C = Commercial, T_J= 0° to +85°C
M=Military Temp, T_C= -55° to +125°C
I = Industrial, T_J = -40° to +100°C
B = MIL-STD-883C Class B

Ordering Information

Example: **XC3030A-3 PC44C**

Device Type
Speed Grade
Temperature Range
Number of Pins
Package Type

XC3000A
Field Programmable Gate Arrays

June 1, 1996 (Version 1.0) — Product Specification

Features

- Enhanced, high performance FPGA family with five device types
  - Improved redesign of the basic XC3000 FPGA family
  - Logic densities from 1,000 to 6,000 gates
  - Up to 144 user-definable I/Os
- Superset of the industry-leading XC3000 family
  - Identical to the basic XC3000 in structure, pin out, design methodology, and software tools
  - 100% compatible with all XC3000, XC3000L, and XC3100A bitstreams
  - Improved routing and additional features
- Additional programmable interconnection points (PIPs)
  - Improved access to longlines and CLB clock enable inputs
  - Most efficient XC3000-class solution to bus-oriented designs
- Advanced 0.8 µ and 0.6 µ CMOS static memory technology
  - Low quiescent and active power consumption
- Performance specified by logic delays, faster than corresponding XC3000 versions
- XC3000A-specific features
  - 4 mA output sink and source current
  - Error checking of the configuration bitstream
  - Soft startup starts all outputs in slew-limited mode upon power-up
  - Easy migration to the XC3400 series of HardWire mask programmed devices for high-volume production.

Description

The XC3000A family offers the following enhancements over the popular XC3000 family:

The XC3000A family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3000A devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in the XC3000 family, determined by the individual configuration option.

The XC3000A family is a superset of the XC3000 family. Any bitstream used to configure an XC3000, XC3100 or XC3100A device configures an XC3000A device exactly the same way.

Device	Max Logic Gates	Typical Gate Range	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3020A	1,500	1,000 - 1,500	64	8 x 8	64	256	16	14,779
XC3030A	2,000	1,500 - 2,000	100	10 x 10	80	360	20	22,176
XC3042A	3,000	2,000 - 3,000	144	12 x 12	96	480	24	30,784
XC3064A	5,000	4,000 - 5,000	224	16 x 14	120	688	32	46,064
XC3090A	6,000	5,000 - 6,000	320	16 x 20	144	928	40	64,160

XC3000A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000A Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

XC3000A DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)			0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)			0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})	3020A		100	µA
		3030A		160	µA
		3042A		240	µA
		3064A		340	µA
		3090A		500	µA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD}				
	Chip thresholds programmed as CMOS levels			500	µA
	Chip thresholds programmed as TTL levels			10	µA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested)				
	All Pins except XTL1 and XTL2			10	pF
	XTL1 and XTL2			15	pF
	Input capacitance, PGA 175 (sample tested)				
	All Pins except XTL1 and XTL2			16	pF
	XTL1 and XTL2			20	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V (sample tested)		0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low			3.4	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a MakeBits tie option.

2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020A to the XC3090A.

XC3000A Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000A Global Buffer Switching Characteristics Guidelines

	Speed Grade	-7	-6	
Description	**Symbol**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution[1]				
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	7.5	7.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	6.0	5.7	ns
TBUF driving a Horizontal Longline (L.L.)[1]				
I to L.L. while T is Low (buffer active)	T_{IO}	4.5	4.0	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	9.0	8.0	ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	11.0	10.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	16.0	14.0	ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	10.0	8.0	ns
BIDI				
Bidirectional buffer delay	T_{BIDI}	1.7	1.5	ns

Note: 1. Timing is based on the XC3042A, for other devices see XACT timing calculator.

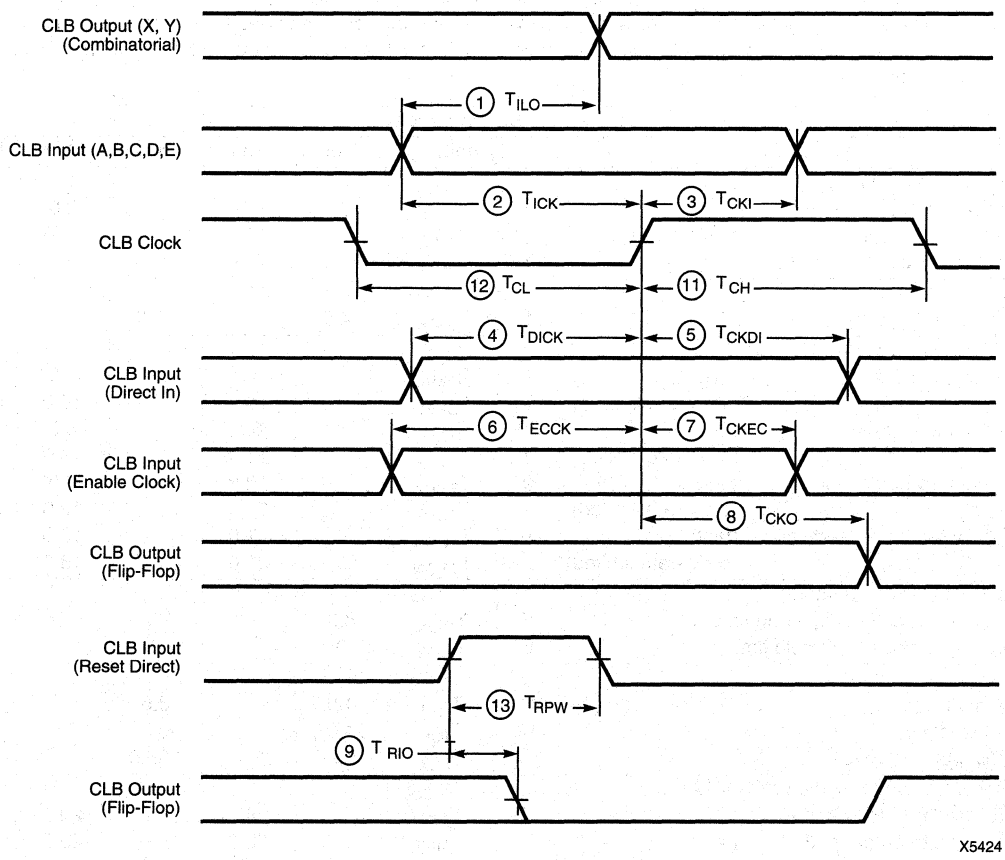
XC3000A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade		-7		-6		
Description		**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay								
Logic Variables	A, B, C, D, E, to outputs X or Y							
	FG Mode	1	T_{ILO}		5.1		4.1	ns
	F and FGM Mode				5.6		4.6	ns
Sequential delay								
Clock k to outputs X or Y		8	T_{CKO}		4.5		4.0	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y								
	FG Mode		T_{QLO}		9.5		8.0	ns
	F and FGM Mode				10.0		8.5	ns
Set-up time before clock K								
Logic Variables	A, B, C, D, E							
	FG Mode	2	T_{ICK}	4.5		3.5		ns
	F and FGM Mode			5.0		4.0		ns
Data In	DI	4	T_{DICK}	4.0		3.0		ns
Enable Clock	EC	6	T_{ECCK}	4.5		4.0		ns
Hold Time after clock K								
Logic Variables	A, B, C, D, E	3	T_{CKI}	0		0		ns
Data In	DI[2]	5	T_{CKDI}	1.0		1.0		ns
Enable Clock	EC	7	T_{CKEC}	2.0		2.0		ns
Clock								
Clock High time		11	T_{CH}	4.0		3.5		ns
Clock Low time		12	T_{CL}	4.0		3.5		ns
Max. flip-flop toggle rate			F_{CLK}	113.0		135.0		MHz
Reset Direct (RD)								
RD width		13	T_{RPW}	6.0		5.0		ns
delay from RD to outputs X or Y		9	T_{RIO}		6.0		5.0	ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]								
$\overline{\text{RESET}}$ width (Low)			T_{MRW}	16.0		14.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y			T_{MRQ}		19.0		17.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see XACT timing calculator.
2. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

XC3000A CLB Switching Characteristics Guidelines (continued)



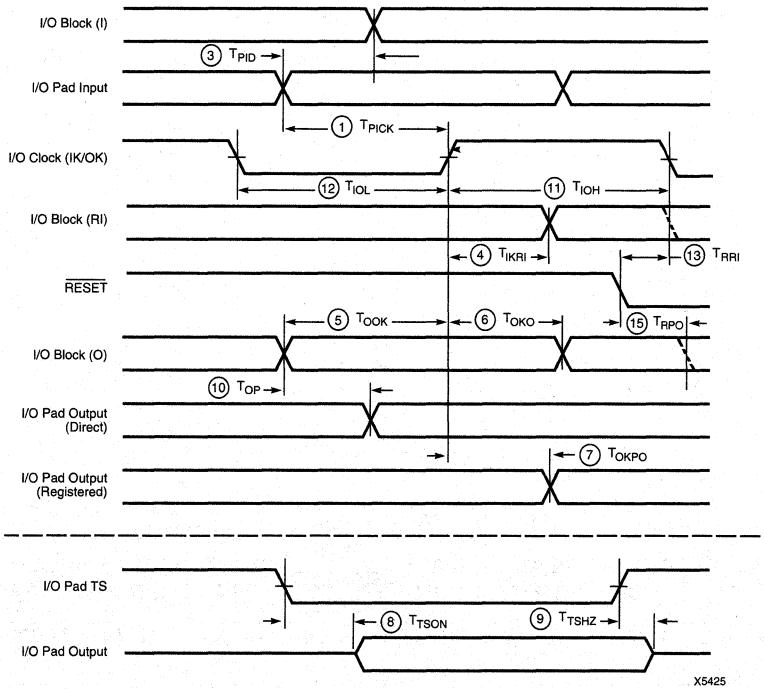
XC3000A IOB Switching Characteristics Guidelines

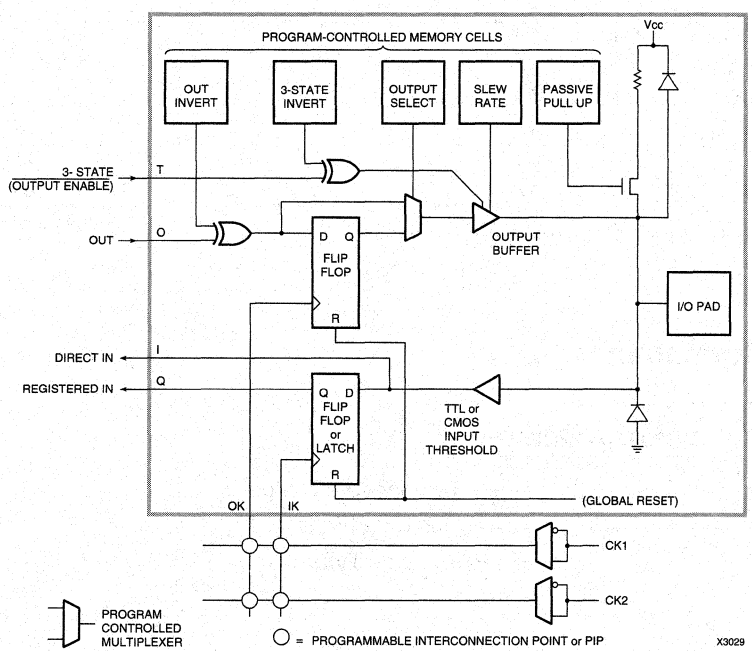
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade		-7		-6		
Description		**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)								
Pad to Direct In (I)		3	T_{PID}		4.0		3.0	ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		15.0		14.0	ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		3.0		2.5	ns
Set-up Time (Input)								
Pad to Clock (IK) set-up time		1	T_{PICK}	14.0		12.0		ns
Propagation Delays (Output)								
Clock (OK) to Pad	(fast)	7	T_{OKPO}		8.0		7.0	ns
same	(slew rate limited)	7	T_{OKPO}		18.0		15.0	ns
Output (O) to Pad	(fast)	10	T_{OPF}		6.0		5.0	ns
same	(slew-rate limited)	10	T_{OPS}		16.0		13.0	ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		10.0		9.0	ns
same	(slew-rate limited)	9	T_{TSHZ}		20.0		12.0	ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		11.0		10.0	ns
same	(slew -rate limited)	8	T_{TSON}		21.0		18.0	ns
Set-up and Hold Times (Output)								
Output (O) to clock (OK) set-up time		5	T_{OOK}	8.0		7.0		ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		0		ns
Clock								
Clock High time		11	T_{IOH}	4.0		3.5		ns
Clock Low time		12	T_{IOL}	4.0		3.5		ns
Max. flip-flop toggle rate			F_{CLK}	113.0		135.0		MHz
Global Reset Delays (based on XC3042A)								
$\overline{\text{RESET}}$ Pad to Registered In	(Q)	13	T_{RRI}		24.0		23.0	ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		33.0		29.0	ns
	(slew-rate limited)	15	T_{RPO}		43.0		37.0	ns

Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configures as a user input.

XC3000A IOB Switching Characteristics Guidelines (continued)





Product Availability

PINS		44	64	68	84		100			
TYPE		PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM PGA	PLAST. PQFP	PLAST. TQFP	PLAST. VQFP	TOP-BRAZED CQFP
CODE		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100
XC3020A	-7			C I	C I	C I	C I			
	-6			C	C	C	C			
XC3030A	-7	C I	C I	C I	C I	C I	C I		C I	
	-6	C	C	C	C	C	C		C	
XC3042A	-7				C I	C I	C I		C I	
	-6				C	C	C		C	
XC3064A	-7				C I					
	-6				C					
XC3090A	-7				C I					
	-6				C					

PINS		132		144	160	164	175		176	208	223
TYPE		PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE		PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3020A	-7										
	-6										
XC3030A	-7										
	-6										
XC3042A	-7	C I	C I	C I							
	-6	C	C	C							
XC3064A	-7	C I	C I	C I	C I						
	-6	C	C	C	C						
XC3090A	-7			C I	C I		C I	C I	C I	C I	
	-6			C	C		C	C	C	C	

Note: C = Commercial, T_J = 0° to +85°C I = Industrial, T_J = -40° to +100°C

Ordering Information

Example:

XC3020A-6PC84C

- Device Type
- Speed Grade
- Temperature Range
- Number of Pins
- Package Type

XC3000L
Field Programmable Gate Arrays

June 1, 1996 (Version 1.0) — Product Specification

Features

- Part of the Zero+ family of 3.3 V FPGAs
  - JEDEC-compliant 3.3 V version of theXC3000A FPGA family
  - Logic densities from 1,000 to 6,000 gates
  - Up to 144 user-definable I/Os
- Advanced, low power 0.8 µ and 0.6 µ CMOS static memory technology
  - Very low quiescent current consumption, ≤ 20µA
  - Operating power consumption 56% less than XC3000A, 66% less than previous generation 5 V FPGAs
- Superset of the industry-leading XC3000 family
  - Identical to the basic XC3000A in structure, pinout, design methodology, and software tools
  - 100% compatible with all XC3000, XC3000A, XC3100L and XC3100A bitstreams
  - Improved routing and additional features
- Additional programmable interconnection points (PIPs)
  - Improved access to Longlines and CLB clock enable inputs
  - Most efficient XC3000-class solution to bus-oriented designs
- XC3000L-specific features
  - Guaranteed over the 3.0 to 3.6 V Vcc range
  - 4 mA output sink and source current
  - Error checking of the configuration bitstream
  - Soft startup starts all outputs in slew-limited mode upon power-up
  - Easy migration to the XC3400 series of HardWire mask programmed devices for high-volume production

Description

The XC3000L family of FPGAs is optimized for operation from a nominally 3.3 V supply. Aside from the electrical and timing parameters listed in this data sheet, the XC3000L family is in all respects identical with the XC3000A family, and is a superset of the XC3000 family.

The operating power consumption of Xilinx FPGAs is almost exclusively dynamic, and it changes with the square of the supply voltage. For a given complexity and clock speed, the XC3000L consumes, therefore, only 44% of the power used by the equivalent XC3000A device. In accordance with its use in battery-powered equipment, the XC3000L family was designed for the lowest possible power-down and quiescent current consumption.

In mixed supply-voltage systems, the XC3000L, fed by a 3.3 V (nominal) supply, can directly drive any device with TTL-like input thresholds. When a 5 V device drives the XC3000L, a current-limiting resistor (1 kΩ) or a voltage divider is required to prevent excessive input current.

Like the XC3000A family, XC3000L offers the following functional improvements over the popular XC3000 family:

The XC3000L family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3000L devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in the XC3000 family, determined by the individual configuration option.

The XC3000L family is a superset of the XC3000 family. Any bitstream used to configure an XC3000 device configures an XC3000L device the same way.

Device	Max Logic Gates	Typical Gate Range	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3020L	1,500	1,000 - 1,500	64	8 x 8	64	256	16	14,779
XC3030L	2,000	1,500 - 2,000	100	10 x 10	80	360	20	22,176
XC3042L	3,000	2,000 - 3,000	144	12 x 12	96	480	24	30,784
XC3064L	5,000	4,000 - 5,000	224	16 x 14	120	688	32	46,064
XC3090L	6,000	5,000 - 6,000	320	16 x 20	144	928	40	64,160

XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage — TTL configuration	2.0	V_{CC}+0.3	V
V_{IL}	Low-level input voltage — TTL configuration	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 6.0 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	2.40		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		10	µA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD}[1] Chip thresholds programmed as CMOS levels		20	µA
I_{IL}	Input Leakage Current	–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V (sample tested)	0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a MakeBits tie option. I_{CCO} is in addition to I_{CCPD}.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.

XC3000L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-8	
Description	**Symbol**	**Max**	**Units**
Global and Alternate Clock Distribution[1]			
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	9.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	7.0	ns
TBUF driving a Horizontal Longline (L.L.)[1]			
I to L.L. while T is Low (buffer active)	T_{IO}	5.0	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	12.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	24.0	ns
BIDI			
Bidirectional buffer delay	T_{BIDI}	2.0	ns

1. Timing is based on the XC3042A, for other devices see XACT timing calculator.
2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

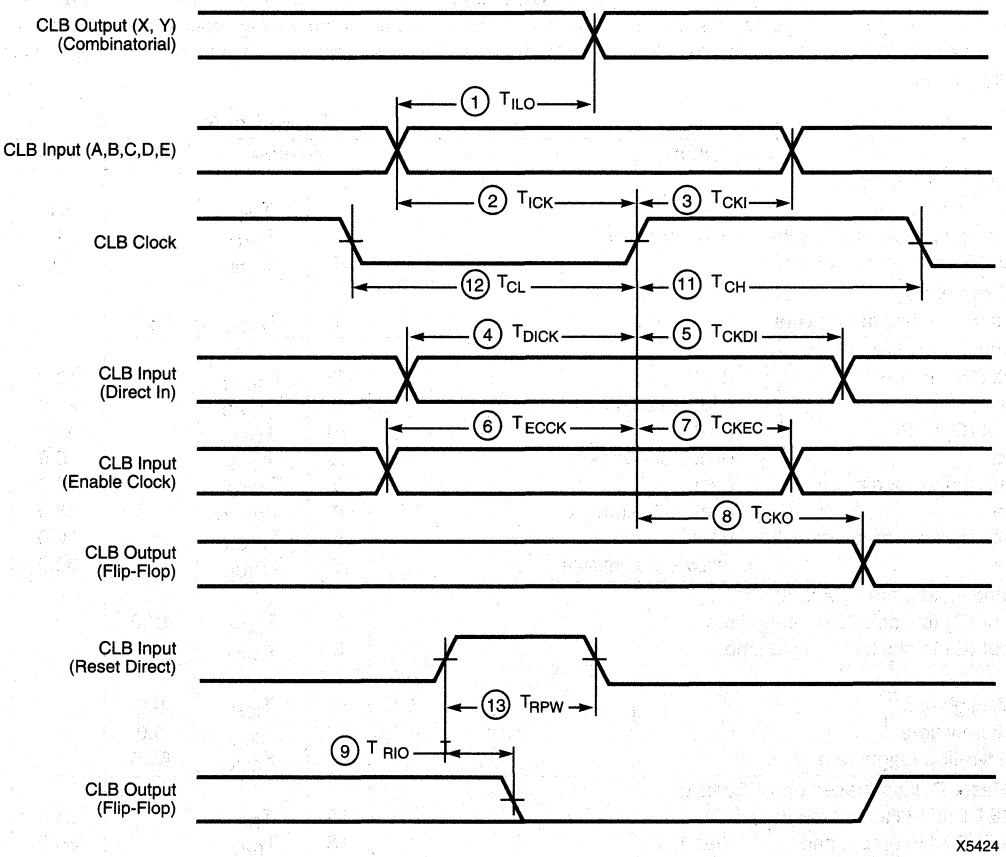
XC3000L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade		-8		
Description		**Symbol**		**Min**	**Max**	**Units**
Combinatorial Delay						
Logic Variables	A, B, C, D, E, to outputs X or Y					
	FG Mode	1	T_{ILO}		6.7	ns
	F and FGM Mode				7.5	ns
Sequential delay						
Clock k to outputs X or Y		8	T_{CKO}		7.5	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y						
	FG Mode		T_{QLO}		14.0	ns
	F and FGM Mode				14.8	ns
Set-up time before clock K						
Logic Variables	A, B, C, D, E					
	FG Mode	2	T_{ICK}	5.0		ns
	F and FGM Mode			5.8		ns
Data In	DI	4	T_{DICK}	5.0		ns
Enable Clock	EC	6	T_{ECCK}	6.0		ns
Hold Time after clock K						
Logic Variables	A, B, C, D, E	3	T_{CKI}	0		ns
Data In	DI[2]	5	T_{CKDI}	2.0		ns
Enable Clock	EC	7	T_{CKEC}	2.0		ns
Clock						
Clock High time		11	T_{CH}	5.0		ns
Clock Low time		12	T_{CL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Reset Direct (RD)						
RD width		13	T_{RPW}	7.0		ns
delay from RD to outputs X or Y		9	T_{RIO}	7.0		ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]						
$\overline{\text{RESET}}$ width (Low)			T_{MRW}	16.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y			T_{MRQ}		23.0	ns

Notes: 1. Timing is based on the XC3042L, for other devices see XACT timing calculator.
2. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

XC3000L CLB Switching Characteristics Guidelines (continued)



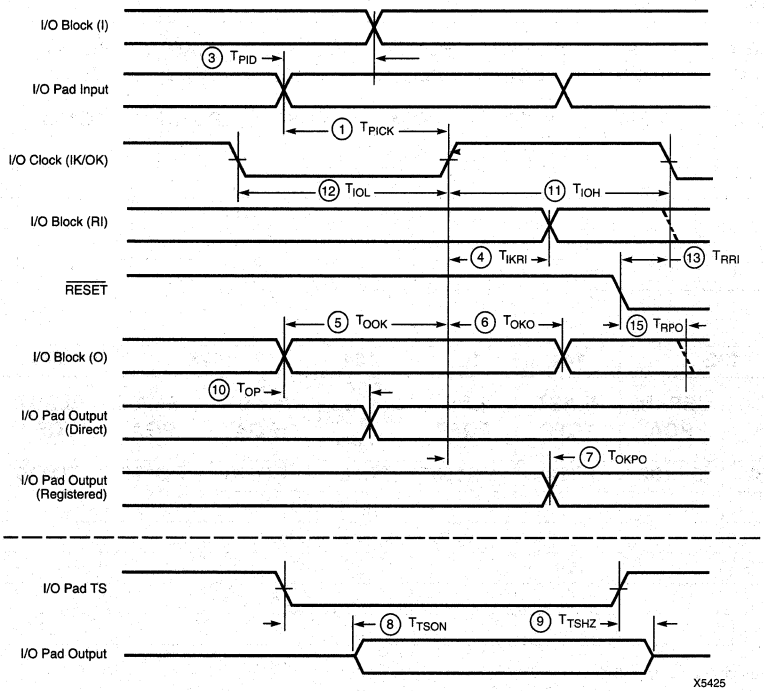
XC3000L IOB Switching Characteristics Guidelines

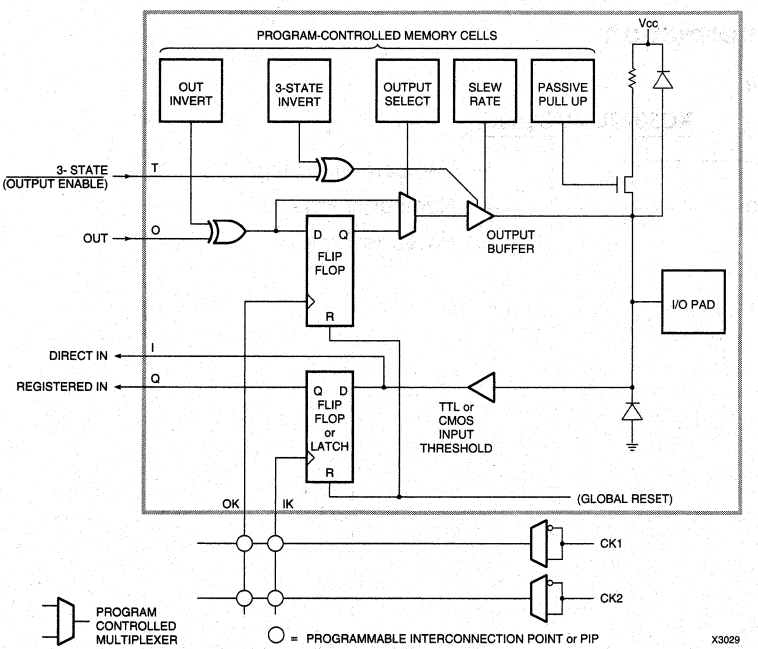
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade	-8		
Description		**Symbol**		**Min**	**Max**	**Units**
Propagation Delays (Input)						
Pad to Direct In (I)		3	T_{PID}		5.0	ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		24.0	ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		6.0	ns
Set-up Time (Input)						
Pad to Clock (IK) set-up time		1	T_{PICK}	22.0		ns
Propagation Delays (Output)						
Clock (OK) to Pad	(fast)	7	T_{OKPO}		12.0	ns
same	(slew rate limited)	7	T_{OKPO}		28.0	ns
Output (O) to Pad	(fast)	10	T_{OPF}		9.0	ns
same	(slew-rate limited)	10	T_{OPS}		25.0	ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		12.0	ns
same	(slew-rate limited)	9	T_{TSHZ}		28.0	ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		16.0	ns
same	(slew -rate limited)	8	T_{TSON}		32.0	ns
Set-up and Hold Times (Output)						
Output (O) to clock (OK) set-up time		5	T_{OOK}	12.0		ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		ns
Clock						
Clock High time		11	T_{IOH}	5.0		ns
Clock Low time		12	T_{IOL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Global Reset Delays (based on XC3042A)						
$\overline{\text{RESET}}$ Pad to Registered In	(Q)	13	T_{RRI}		25.0	ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		35.0	ns
	(slew-rate limited)	15	T_{RPO}		51.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configures as a user input.

XC3000L IOB Switching Characteristics Guidelines (continued)





Product Availability

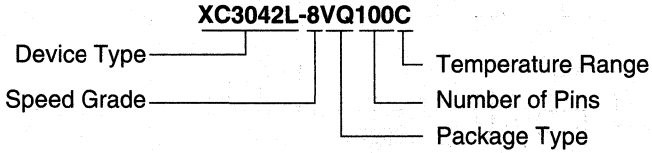
PINS	44	64	68	84		100			
TYPE	PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM PGA	PLAST. PQFP	PLAST. TQFP	PLAST. VQFP	TOP-BRAZED CQFP
CODE	PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100
XC3020L				C					
XC3030L		C		C				C	
XC3042L				C				C	
XC3064L				C					
XC3090L				C					

PINS	132		144	160	164	175		176	208	223
TYPE	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3020L										
XC3030L										
XC3042L			C							
XC3064L			C							
XC3090L			C					C		

Note: C = Commercial, T_J = 0° to +85°C

Ordering Information

Example:



XC3100A
Field Programmable Gate Arrays

June 1, 1996 (Version 4.1)

Product Specification

Features

- Ultra-high-speed FPGA family with six members
  - 50-95 MHz system clock rates
  - 190 to 370 MHz guaranteed flip-flop toggle rates
  - 1.55 to 4.1 ns logic delays
- High-end additional family member in the 22 X 22 CLB array-size XC3195A device
- 8 mA output sink current and 8 mA source current
- Maximum power-down and quiescent current is 5 mA
- 100% architecture and pin-out compatible with other XC3000 families
- Software and bitstream compatible with the XC3000, XC3000A, and XC3000L families
- 100% PCI complaint (A-2, A-1, A-09 speed grade in plastic quad flat pack (PQFP) packaging).

XC3100A combines the features of the XC3000A and XC3100 families.

- Additional interconnect resources for TBUFs and CE inputs
- Error checking of the configuration bitstream
- Soft startup holds all outputs slew-rate limited during initial power-up
- More advanced CMOS process

Description

The XC3100A is a performance-optimized relative of the XC3000A and XC3100A families. While all families are footprint compatible, XC3100A family extends the typical system performance beyond 85 MHz.

The XC3100A family follows the XC4000 speed-grade nomenclature, indicating device performance with a number that is based on the internal logic-block delay, in ns.

The XC3100A family offers the following enhancements over the popular XC3000 family.

The XC3100A family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3100A devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in all XC3000 families, determined by the individual configuration option.

The XC3100A family is a superset of the XC3000 families. Any bitstream used to configure an XC3000, XC3000A, XC3000L or XC3100 device, will configure the same-size XC3100A device exactly the same way.

Device	Max Logic Gates	Typical Gate Range	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3120A	1,500	1,000 - 1,500	64	8 x 8	64	256	16	14,779
XC3130A	2,000	1,500 - 2,000	100	10 x 10	80	360	20	22,176
XC3142A	3,000	2,000 - 3,000	144	12 x 12	96	480	24	30,784
XC3164A	4,500	3,500 - 4,500	224	16 x 14	120	688	32	46,064
XC3190A	6,000	5,000 - 6,000	320	16 x 20	144	928	40	64,160
XC3195A	7,500	6,500 - 7,500	484	22 x 22	176	1,320	44	94,944

XC3100A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100A Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.25	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

XC3100A DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} min)			0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} min)			0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I_{CCO}	Quiescent LCA supply current in addition to I_{CCPD}[1] Chip thresholds programmed as CMOS levels Chip thresholds programmed as TTL levels			 8 14	 mA mA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V (sample tested)		0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.20	2.80	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA device configured with a MakeBits tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. The number of ground pins varies from two for the XC3120A in the PC84 package, to eight for the XC3195A in the PQ208 or PG223 package.

XC3100A Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3100A Global Buffer Switching Characteristics Guidelines

Speed Grade		-5	-4	-3	-2	-1	-09	
Description	**Symbol**	**Max**	**Max**	**Max**	**Max**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution[1]								
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	6.8	6.5	5.6	4.7	4.3	3.9	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	5.4	5.1	4.3	3.7	3.5	3.1	ns
TBUF driving a Horizontal Longline (L.L.)[1]								
I to L.L. while T is Low (buffer active) (XC3100)	T_{IO}	4.1	3.7	3.1				ns
(XC3100A)	T_{IO}	3.6	3.6	3.1	3.1	2.9	2.1	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	5.6	5.0	4.2	4.2	4.0	3.1	ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	7.1	6.5	5.7	5.7	5.5	4.6	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	15.6	13.5	11.4	11.4	10.4	8.9	ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	12.0	10.5	8.8	8.1	7.1	5.9	ns
BIDI								
Bidirectional buffer delay	T_{BIDI}	1.4	1.2	1.0	0.9	0.85	0.75	ns
							Prelim	

Note: 1. Timing is based on the XC3142A, for other devices see XACT timing calculator.
The use of two pull-up resistors per longline, available on other XC3000 devices, is not a valid design option for XC3100A devices.

XC3100A CLB Switching Characteristics Guidelines

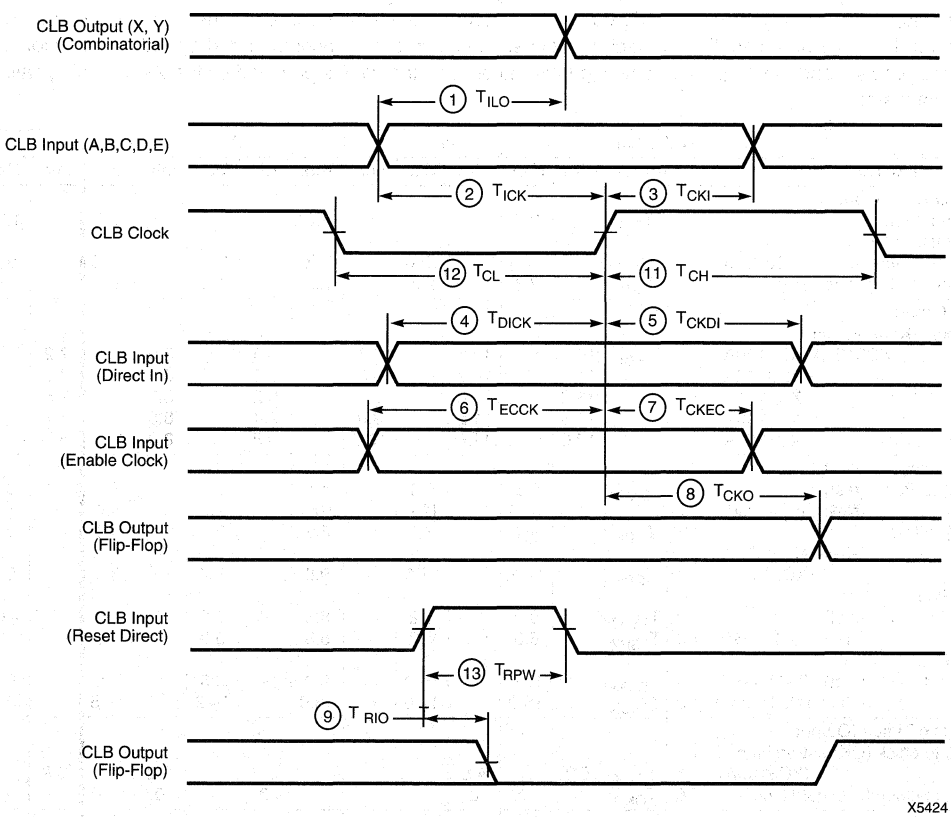
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade			-5		-4		-3		-2		-1		-09		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay															
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		4.1		3.3		2.7		2.2		1.75		1.5	ns
Sequential delay															
Clock k to outputs X or Y	8	T_{CKO}		3.1		2.5		2.1		1.7		1.4		1.25	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		6.3		5.2		4.3		3.5		3.1		2.7	ns
Set-up time before clock K															
Logic Variables A, B, C, D, E	2	T_{ICK}	3.1		2.5		2.1		1.8		1.7		1.5		ns
Data In DI	4	T_{DICK}	2.0		1.6		1.4		1.3		1.2		1.0		ns
Enable Clock EC	6	T_{ECCK}	3.8		3.2		2.7		2.5		2.3		2.05		ns
Reset Direct inactive RD			1.0		1.0		1.0		1.0		1.0		1.0		ns
Hold Time after clock K															
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		0		0		0		0		ns
Data In DI	5	T_{CKDI}	1.0		1.0		0.9		0.9		0.8		0.7		ns
Enable Clock EC	7	T_{CKEC}	1.0		0.8		0.7		0.7		0.6		0.55		ns
Clock															
Clock High time	11	T_{CH}	2.4		2.0		1.6		1.3		1.3		1.3		ns
Clock Low time	12	T_{CL}	2.4		2.0		1.6		1.3		1.3		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	188		227		270		323		323		370		MHz
Reset Direct (RD)															
RD width	13	T_{RPW}	3.8		3.2		2.7		2.3		2.3		2.05		ns
delay from RD to outputs X or Y	9	T_{RIO}		4.4		3.7		3.1		2.7		2.4		2.15	ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]															
$\overline{\text{RESET}}$ width (Low) (XC3142A)		T_{MRW}	14.0		14.0		12.0		12.0		12.0		12.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		17.0		14.0		12.0		12.0		12.0		12.0	ns
													Prelim		

Notes: 1. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100A family increases by 0.50 ns (-5), 0.42 ns (-4) and 0.35 ns (-3), 0.35 ns (-2), 0.30 ns (-1), and 0.30 ns (-09).

XC3100A CLB Switching Characteristics Guidelines (continued)



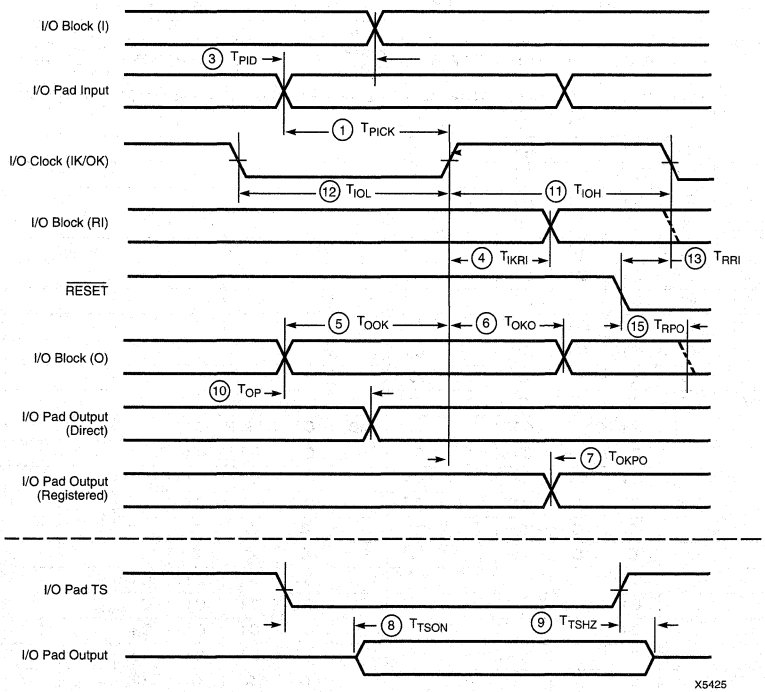
XC3100A IOB Switching Characteristics Guidelines

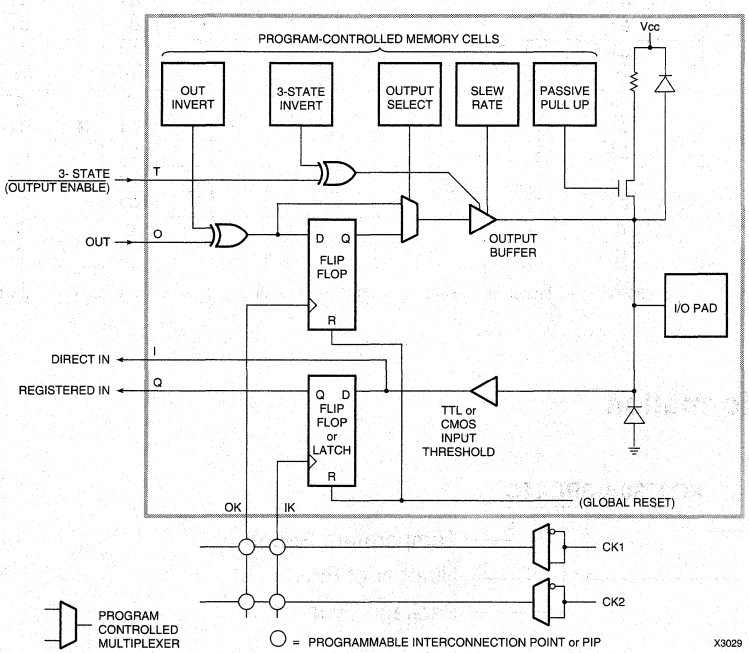
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-5		-4		-3		-2		-1		-09		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)															
Pad to Direct In (I)	3	T_{PID}		2.8		2.5		2.2		2.0		1.7		1.55	ns
Pad to Registered In (Q)															
with latch transparent (XC3100A)		T_{PTG}		14.0		12.0		11.0		11.0		10.0		9.2	ns
Clock (IK) to Registered In (Q)	4	T_{IKRI}		2.8		2.5		2.2		1.9		1.7		1.55	ns
Set-up Time (Input)															
Pad to Clock (IK) set-up time															
XC3120A, XC3130A	1	T_{PICK}	10.9		10.6		9.4		8.9		8.0		7.2		ns
XC3142A			11.0		10.7		9.5		9.0		8.1		7.3		ns
XC3164A			11.2		11.0		9.7		9.2		8.3		7.5		ns
XC3190A			11.5		11.2		9.9		9.4		8.5		7.7		ns
XC3195A			12.0		11.6		10.3		9.8		8.9		8.1		ns
Propagation Delays (Output)															
Clock (OK) to Pad (fast)	7	T_{OKPO}		5.5		5.0		4.4		3.7		3.4		3.3	ns
same (slew rate limited)	7	T_{OKPO}		14.0		12.0		10.0		9.7		8.4		6.9	ns
Output (O) to Pad (fast)	10	T_{OPF}		4.1		3.7		3.3		3.0		3.0		2.9	ns
same (slew-rate limited)															ns
(XC3100A)	10	T_{OPS}		12.1		11.0		9.0		8.7		8.0		6.5	ns
3-state to Pad															
begin hi-Z (fast)	9	T_{TSHZ}		6.9		6.2		5.5		5.0		4.5		4.05	ns
same (slew-rate limited)	9	T_{TSHZ}		6.9		6.2		5.5		5.0		4.5		4.05	ns
3-state to Pad															
active and valid (fast) (XC3100A)	8	T_{TSON}		10.0		10.0		9.0		8.5		6.5		5.0	ns
same (slew -rate limited)	8	T_{TSON}		18.0		17.0		15.0		14.2		11.5		8.6	ns
Set-up and Hold Times (Output)															
Output (O) to clock (OK) set-up time															
(XC3100A)	5	T_{OOK}	5.0		4.5				3.6		3.2		2.9		ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0		0				0		0				ns
Clock															
Clock High time	11	T_{IOH}	2.4		2.0		1.6		1.3		1.3		1.3		ns
Clock Low time	12	T_{IOL}	2.4		2.0		1.6		1.3		1.3		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	188		227		270		323		323		370		MHz
Global Reset Delays															
RESET Pad to Registered In (Q)															
(XC3142A)	13	T_{RRI}		18.0		15.0		13.0		13.0		13.0		14.4	ns
(XC3190A)				29.5		25.5		21.0		21.0		21.0		21.0	ns
RESET Pad to output pad (fast)	15	T_{RPO}		24.0		20.0		17.0		17.0		17.0		17.0	ns
(slew-rate limited)	15	T_{RPO}		32.0		27.0		23.0		23.0		22.0		21.0	ns
													Preliminary		

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). For larger capacitive loads, see page XAPP024. Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configures as a user input.

XC3100A IOB Switching Characteristics Guidelines (continued)





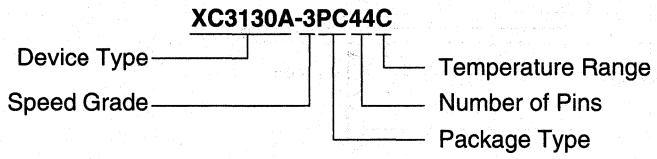
Product Availability

PINS		44	64	68	84		100				132		144	160	164	175		176	208	223
TYPE		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Ceram PGA	Plast. PQFP	Plast. TQFP	Plast. VQFP	Top-Brazed CQFP	Plast. PGA	Ceram PGA	Plast. TQFP	Plast. PQFP	Top-Brazed CQFP	Plast. PGA	Ceram PGA	Plast. TQFP	Plast. PQFP	Ceram PGA
CODE		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3120/A	-5			C I	C I	C I	C I													
	-4			C I	C I	C I	C I													
	-3			C I	C I	C I	C I													
	-2			C I	C I	C I	C I													
	-1			C	C	C	C													
	-09			C	C	C	C													
XC3130A	-5	C I	C I	C I	C I	C I	C I		C I											
	-4	C I	C I	C I	C I	C I	C I		C I											
	-3	C I	C I	C I	C I	C I	C I		C I											
	-2	C I	C I	C I	C I	C I	C I		C I											
	-1	C	C	C	C	C	C		C											
	-09	C	C	C	C	C	C		C											
XC3142A	-5				C I	C I M B	C I		C I	MB	C I	C I M B	C I							
	-4				C I	C I	C I		C I		C I	C I	C I							
	-3				C I	C I	C I		C I		C I	C I	C I							
	-2				C I	C I	C I		C I		C I	C I	C I							
	-1				C	C	C		C		C	C	C							
	-09				C	C	C		C		C	C	C							
XC3164A	-5				C I						C I	C I	C I	C I						
	-4				C I						C I	C I	C I	C I						
	-3				C I						C I	C I	C I	C I						
	-2				C I						C I	C I	C I	C I						
	-1				C						C	C	C	C						
	-09				C						C	C	C	C						
XC3190A	-5				C I									C I	M B	C I	C I M B	C I	C I	
	-4				C I									C I		C I	C I	C I	C I	
	-3				C I									C I		C I	C I	C I	C I	
	-2				C I									C I		C I	C I	C I	C I	
	-1				C									C		C	C	C	C	
	-09				C									C		C	C	C	C	
XC3195A	-5				C I									C I	M B	C I	C I M B		C I	C I M B
	-4				C I									C I		C I	C I		C I	C I
	-3				C I									C I		C I	C I		C I	C I
	-2				C I									C I		C I	C I		C I	C I
	-1				C									C		C	C		C	C
	-09				C									C		C	C		C	C

Note: C = Commercial, T_J = 0° to +85°C I = Industrial, T_J = -40° to +100°C M = Military, T_C = -55° to +125° C B = MIL-STD-883C Class B

Ordering Information

Example:



XC3100L
Field Programmable Gate Arrays

June 1, 1996 (Version 1.0)

Advance Product Specification

Features

- Ultra-high-speed FPGA family with two members
  - 50-85 MHz system clock rates
  - 270 to 325 MHz guaranteed flip-flop toggle rates
  - 2.2 to 2.7 ns logic delays
- 4 mA output sink current and 4 mA source current
- JEDEC compliant 3.3 V version of XC3100A FPGA family
- The XC3100L is 100% architecture, pin-out and bitstream compatible with the XC3000A, XC3000L and XC3100A families
- Advanced, 0.6 µ TLM CMOS technology
- XC3100L combines the features of the XC3000L and XC3100A families.
- Additional interconnect resources for TBUFs and CE inputs
- Error checking of the configuration bitstream
- Soft startup holds all outputs slew-rate limited during initial power-up
- More advanced CMOS process

Description

XC3100L is a performance-optimized relative of the XC3000L and XC3100A families. While all families are footprint compatible, the XC3100L family extends the typical system performance beyond 80 MHz.

The XC3100L family follows the XC4000 speed-grade nomenclature, indicating device performance with a number that is based on the internal logic-block delay, in ns.

The XC3100L family offers the following enhancements over the popular XC3000 family.

The XC3100L family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3100L devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in all XC3000 families, determined by the individual configuration option.

Any bitstream used to configure an XC3000, XC3000A, XC3000L or XC3100A device, will configure the same-size XC3100L device exactly the same way.

Device	Max Logic Gates	Typical Gate Range	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3142L	3,000	2,000 - 3,000	144	12 x 12	96	480	24	30,784
XC3190L	6,000	5,000 - 6,000	320	16 x 20	144	928	40	64,160

XC3100L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage	2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 V to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 and 3.6 V range later, when smaller device geometries might preclude operation @ 5 V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3100L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = -4.0 mA, V_{CC} min)	2.4		V
	High-level output voltage (@ I_{OH} = -100.0 µA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OH} = 4.0 mA, V_{CC} min)		0.40	V
	Low-level output voltage (@ I_{OH} = +100.0 µA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCO}	Quiescent FPGA supply current Chip thresholds programmed as CMOS levels[1]		1.5	mA
I_{IL}	Input Leakage Current	-10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
	Input capacitance, PGA175 (sample tested) All pins except XTL1 and XTL2 XTL1 and XTL2		 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V (sample tested)	0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic Low	0.20	2.80	mA

Notes: 1. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a MakeBits tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source current may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3142L to the XC3190L.

XC3100L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3100L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-3	-2	
Description	**Symbol**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution[1]				
Either:**Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	5.6	4.7	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	4.3	3.7	ns
TBUF driving a Horizontal Longline (L.L.)[1]				
I to L.L. while T is Low (buffer active)	T_{IO}	3.1	3.1	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	4.2	4.2	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	11.4	11.4	ns
BIDI				
Bidirectional buffer delay	T_{BIDI}	1.0	0.9	ns
		Advance		

Notes: 1. Timing is based on the XC3142L, for other devices see XACT timing calculator.
2. The use of two pull-up resistors per longline, available on other XC3000 devices, is not a valid option for XC3100L devices.

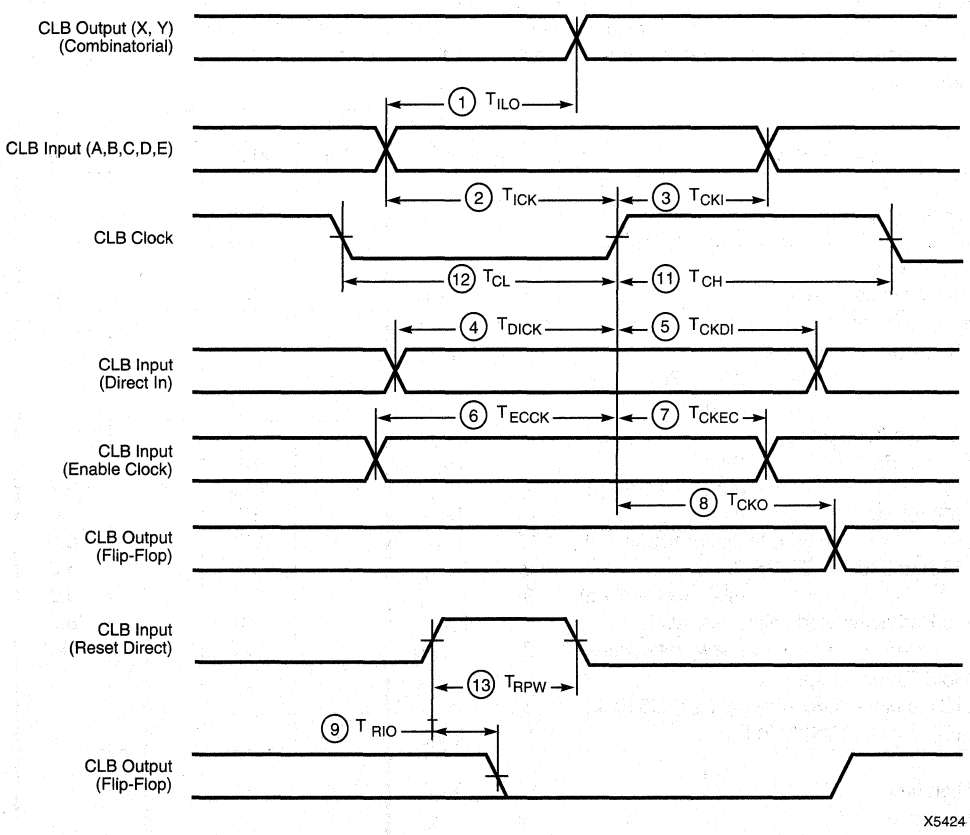
XC3100L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade		-3		-2		
Description		**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay								
Logic Variables A, B, C, D, E, to outputs X or Y		1	T_{ILO}		2.7		2.2	ns
Sequential delay								
Clock k to outputs X or Y		8	T_{CKO}		2.1		1.7	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y			T_{QLO}		4.3		3.5	ns
Set-up time before clock K								
Logic Variables	A, B, C, D, E	2	T_{ICK}	2.1		1.8		ns
Data In	DI	4	T_{DICK}	1.4		1.3		ns
Enable Clock	EC	6	T_{ECCK}	2.7		2.5		ns
Reset Direct Inactive	RD			1.0		1.0		ns
Hold Time after clock K								
Logic Variables	A, B, C, D, E	3	T_{CKI}	0		0		ns
Data In	DI	5	T_{CKDI}	0.9		0.9		ns
Enable Clock	EC	7	T_{CKEC}	0.7		0.7		ns
Clock								
Clock High time		11	T_{CH}	1.6		1.3		ns
Clock Low time		12	T_{CL}	1.6		1.3		ns
Max. flip-flop toggle rate			F_{CLK}	270		325		MHz
Reset Direct (RD)								
RD width		13	T_{RPW}	2.7		2.3		ns
delay from RD to outputs X or Y		9	T_{RIO}		3.1		2.7	ns
Global Reset ($\overline{\text{RESET}}$ Pad)								
$\overline{\text{RESET}}$ width (Low)								ns
	(XC3142L)		T_{MRW}	12.0		12.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y			T_{MRQ}		12.0		12.0	
					Advance			

Notes:
1. The CLB K to Q delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.
2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100L family increase by 0.35 ns (-3) and 0.29 ns (-2).

XC3100L CLB Switching Characteristics Guidelines (continued)



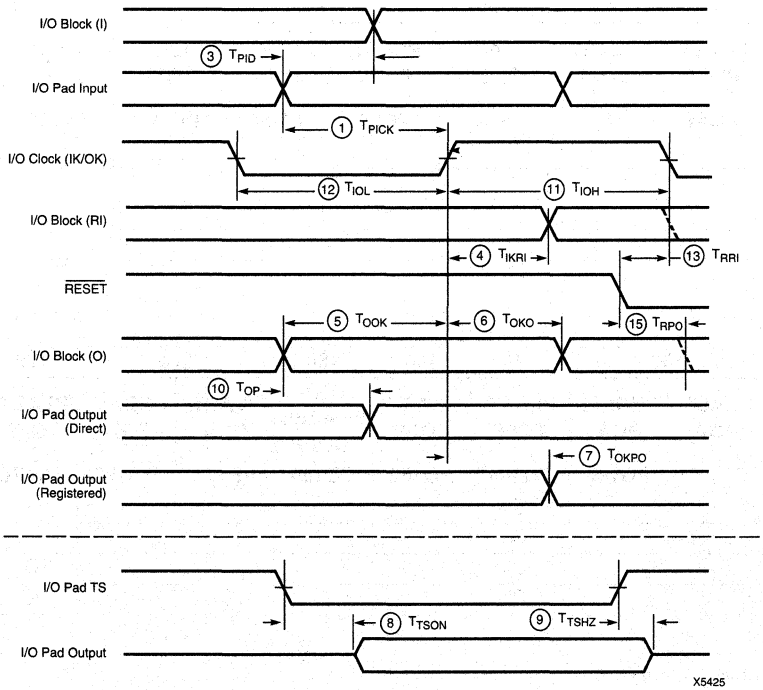
XC3100L IOB Switching Characteristics Guidelines

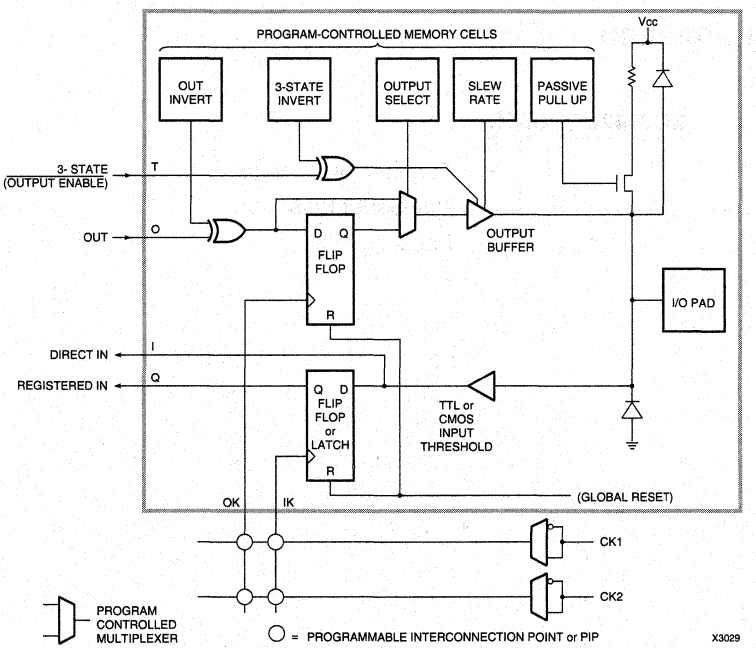
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-3		-2		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)							
Pad to Direct In (I)	3	T_{PID}		2.2		2.0	ns
Pad to Registered In (Q) with latch (XC3100L) transparent		T_{PTG}		11.0		11.0	ns
Clock (IK) to Registered In (Q)	4	T_{IKRI}		2.2		1.9	ns
Set-up Time (Input)							
Pad to Clock (IK) set-up time	1	T_{PICK}					
XC3142L			9.5		9.0		ns
XC3190L			9.9		9.4		ns
Propagation Delays (Output)							
Clock (OK) to Pad (fast)	7	$T_{OKPO}T_{OK}$		4.4		4.0	ns
same (slew rate limited)	7	PO		10.0		9.7	ns
Output (O) to Pad (fast)	10	T_{OPF}		3.3		3.0	ns
same (slew-rate limited)(XC3100L)	10	T_{OPF}		9.0		8.7	ns
3-state to Pad begin hi-Z (fast)	9	T_{TSHZ}		5.5		5.0	ns
same (slew-rate limited)	9	T_{TSHZ}		5.5		5.0	ns
3-state to Pad active and valid (fast)(XC3100L)	8	T_{TSON}		9.0		8.5	ns
same (slew -rate limited)	8	T_{TSON}		15.0		14.2	ns
Set-up and Hold Times (Output)							
Output (O) to clock (OK) set-up time (XC3100L)	5	T_{OOK}	4.0		3.6		ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0		0		ns
Clock							
Clock High time	11	T_{IOH}	1.6		1.3		ns
Clock Low time	12	T_{IOL}	1.6		1.3		ns
Export Control Maximum flip-flop toggle rate		F_{TOG}	270		325		MHz
Global Reset Delays							
$\overline{\text{RESET}}$ Pad to Registered In (Q)							
(XC3142L)	13	T_{RRI}		16.0		16.0	ns
(XC3190L)				21.0		21.0	ns
$\overline{\text{RESET}}$ Pad to output pad (fast)	15	T_{RPO}		17.0		17.0	ns
(slew-rate limited)	15	T_{RPO}		23.0		23.0	ns
			Advance				

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is negative. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.

XC3100L IOB Switching Characteristics Guidelines (continued)





Product Availability

PINS		44	64	68	84		100			
TYPE		PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM PGA	PLAST. PQFP	PLAST. TQFP	PLAST. VQFP	TOP-BRAZED CQFP
CODE		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100
XC3142L	-3				C				C	
	-2				C				C	
XC3190L	-3				C					
	-2				C					
	Adv.									

PINS		132		144	160	164	175		176	208	223
TYPE		PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE		PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3142L	-3			C							
	-2			C							
XC3190L	-3			C					C		
	-2			C					C		
	Adv.										

Note: C = Commercial, T_J = 0° to +85°C

Ordering Information

Example:

XC3142L-3PC84C

- Device Type
- Speed Grade
- Package Type
- Number of Pins
- Temperature Range

XC1700D Family of Serial Configuration PROMs

XC1700D Family of Serial Configuration PROMs

June 1, 1996 (Version 1.0)

Product Specification

Features

- Extended family of one-time programmable (OTP) bit-serial read-only memories used for storing the configuration bitstreams of Xilinx FPGAs
- On-chip address counter, incremented by each rising edge on the clock input
- Simple interface to the FPGA requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- XC17128D or XC17256D supports XC4000 fast configuration mode (12.5 MHz)
- Low-power CMOS EPROM process
- Available in 5 V and 3.3 V versions
- Available in plastic and ceramic packages, and commercial, industrial and military temperature ranges
- Space efficient 8-pin DIP, 8-pin SOIC, 8-pin VOIC, or 20-pin surface-mount packages.
- Programming support by leading programmer manufacturers.

Description

The XC1700 family of serial configuration PROMs (SCPs) provides an easy-to-use, cost-effective method for storing Xilinx FPGA configuration bitstreams.

When the FPGA is in master serial mode, it generates a configuration clock that drives the SCP. A short access time after the rising clock edge, data appears on the SCP DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SCP. When the FPGA is in slave mode, the SCP and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all SCPs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, the XACT development system compiles the FPGA design file into a standard Hex format, which is then transferred to the programmer.

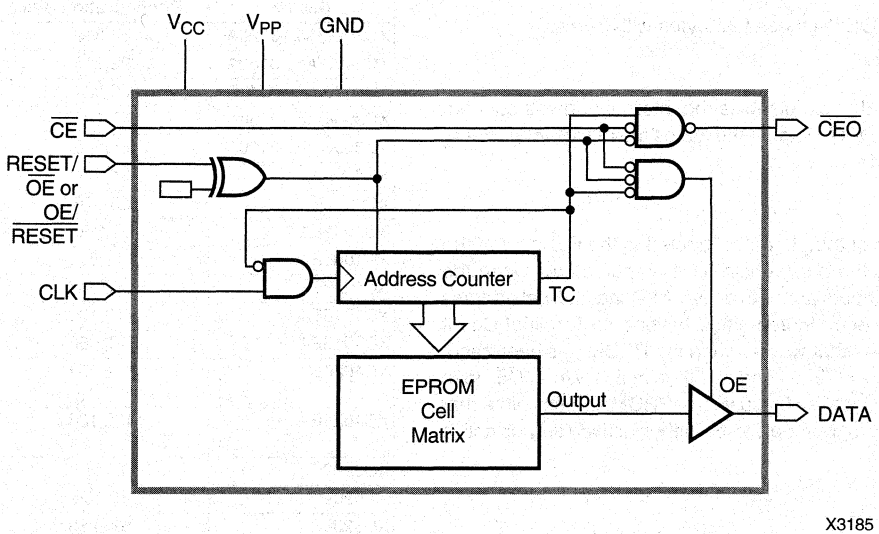


Figure 1: Simplified Block Diagram (does not show programming circuit)

Pin Description

DATA

Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK

Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.

RESET/$\overline{OE}$

When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is 3-stated. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGA's $\overline{INIT}$ pin.

The polarity of this pin is controlled in the programmer interface by writing data into four high-end byte locations. This input pin is easily inverted using the Xilinx PROM programmer software (XPP). Third-party programmers have different methods to invert this pin.

For RESET/$\overline{OE}$, fill the four polarity bytes with Ones or do nothing.

For $\overline{RESET}$/OE, fill these four bytes with Zeros.

$\overline{CE}$

When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$

Chip Enable output, to be connected to the $\overline{CE}$ input of the next SCP in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}

Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin *must* be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. *Do not leave VPP floating!*

V_{CC}

Positive supply pin.

GND

Ground pin.

Serial PROM Pinouts

Pin Name	8-Pin	20-Pin
DATA	1	2
CLK	2	4
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3	6
$\overline{CE}$	4	8
GND	5	10
$\overline{CEO}$	6	14
V_{PP}	7	17
V_{CC}	8	20

Capacity

Device	Configuration Bits
XC1718D or L	18,144
XC1736D	36,288
XC1765D or L	65,536
XC17128D or L	131,072
XC17256D or L	262,144

plus 32 bits for reset polarity control

Number of Configuration Bits, Including Header for all Xilinx FPGAs and Compatible SCP Type

Device	Configuration Bits	SCP
XC3020/A/L+3120A	14,819	XC1718D
XC3030/A/L+3130A	22,216	XC1736D
XC3042/A/L+3142A	30,824	XC1736D
XC3064/A/L+3164A	46,104	XC1765D
XC3090/A/L+3190A	64,200	XC1765D
XC3195A	94,984	XC17128D
XC4003E	53,976	XC1765D
XC4005E/L	95,000	XC17128D/L
XC4006E	119,832	XC17128D
XC4008E	147,544	XC17256D
XC4010E/L	178,136	XC17256D/L
XC4013E/L	247,960	XC17256D/L
XC4020E	329,304	XC17256D + XC17128D
XC4025E	422,168	XC17256D + XC17256D
XC5202	42,416	XC1765D
XC5204	70,704	XC17128D
XC5206	106,288	XC17128D
XC5210	165,488	XC17256D
XC5215	237,744	XC17256D

Controlling Serial PROMs

Most connections between the FPGA device and the Serial PROM are simple and self-explanatory.

- The DATA output(s) of the of the Serial PROM(s) drives the DIN input of the lead FPGA device.
- The master FPGA CCLK output drives the CLK input(s) of the Serial PROM(s).
- The $\overline{CEO}$ output of a Serial PROM drives the $\overline{CE}$ input of the next Serial PROM in a daisy chain (if any).
- The $\overline{RESET}$/OE input of all Serial PROMs is best driven by the $\overline{INIT}$ output of the XC3000 or XC4000 lead FPGA device. This connection assures that the Serial PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods – such as driving $\overline{RESET}$/OE from $\overline{LDC}$ or system reset – assume that the Serial PROM internal power-on-reset is always in step with the FPGA's internal power-on-reset, which may not be a safe assumption.
- The $\overline{CE}$ input of the lead (or only) Serial PROM is driven by the DONE/$\overline{PRGM}$ or DONE output of the lead FPGA device, provided that DONE/$\overline{PRGM}$ is not permanently grounded. Otherwise, $\overline{LDC}$ can be used to drive $\overline{CE}$, but must then be unconditionally High during user operation. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Logic Cell Array and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Mode, the FPGA automatically loads the configuration program from an external memory. The Serial Configuration PROM has been designed for compatibility with the Master Serial Mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial Mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the Serial Configuration PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the Serial Configuration PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The XC3000 and XC4000 families take care of this automatically with an on-chip default pull-up resistor. With XC2000-family devices, the user must either configure DIN as an active output, or provide a defined level, e.g., by using an external pull-up resistor, if DIN is configured as an input.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a Serial Configuration PROM, the $\overline{OE}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the D/$\overline{P}$ line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies $\overline{RESET}$ during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the Serial PROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (24) and D/$\overline{P}$ goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Cascading Serial Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded SCPs provide additional memory. After the last bit from the first SCP is read, the next clock signal to the SCP asserts its $\overline{CEO}$ output Low and disables its DATA line. The second SCP recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded SCPs are reset if the FPGA $\overline{RESET}$ pin goes Low, assuming the SCP reset polarity option has been inverted.

To reprogram the FPGA with another program, the D/$\overline{P}$ line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.

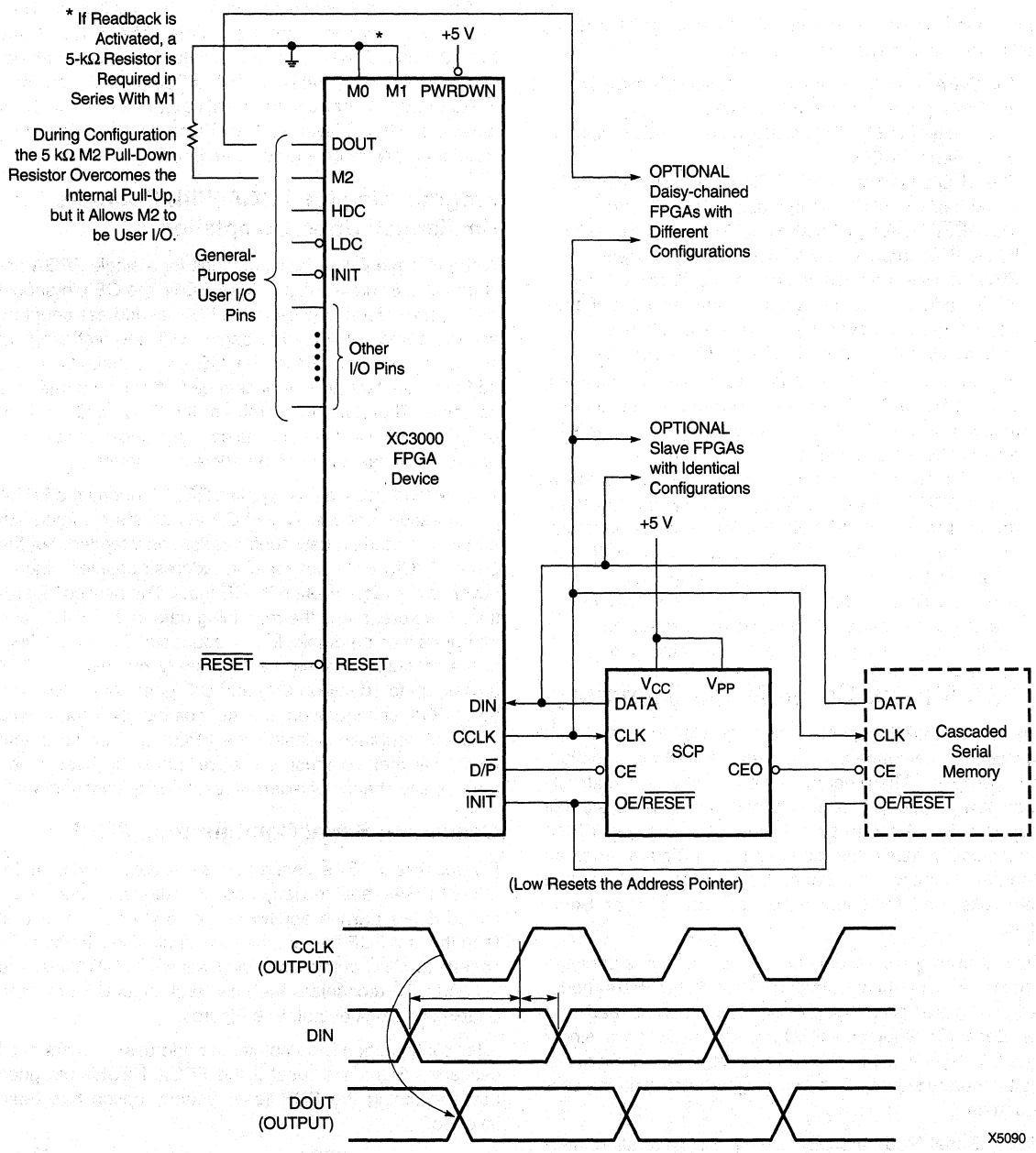


Figure 2: Master Serial Mode. The one-time-programmable Serial Configuration PROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGA. An early D/$\overline{P}$ inhibits the PROM data output one CCLK cycle before the FPGA I/Os become active.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

(A technique for further reducing the standby current of a Serial Configuration PROM is described in the XCELL journal, Issue 11, page 13.)

Programming the XC1700 Family Serial PROMs

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and voltages are used. Different product types use different algorithms and voltages, and the wrong choice can permanently damage the device.

Table 1: Truth Table for XC1700 Control Inputs

Control Inputs		Internal Address	Outputs		
RESET	CE		DATA	CEO	I_{CC}
Inactive	Low	if address ≤ TC: increment if address > TC: don't change	active 3-state	High Low	active reduced
Active	Low	Held reset	3-state	High	active
Inactive	High	Not changing	3-state	High	standby
Active	High	Held reset	3-state	High	standby

Notes: 1. The XC1700 RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC+1 = address 0.

Table 2: Data I/O Programmer Locations for Programming RESET Polarity

Device	Hex Address
XC1718D or L	8DC through 8DF
XC1736D	11B8 through 11BB
XC1765D or L	2000 through 2003
XC17128D or L	4000 through 4003
XC17256D or L	8000 through 8003

IMPORTANT: Always be sure to use the proper programming algorithm. "D" series PROMs will not program properly using "A" -series algorithms. Always tie the V_{PP} pin to V_{CC} in your application. Never leave V_{PP} floating.

XC1718D, XC1736D, XC1765D, XC17128D and XC17256D

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	-0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +125	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND 0°C to +70°C junction	4.75	5.25	V
	Industrial	Supply voltage relative to GND -40°C to +85°C junction	4.50	5.50	V
	Military	Supply voltage relative to GND -55°C to +125°C case	4.50	5.50	V

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode			10.0	mA
I_{CCS}	Supply current, standby mode, XC17128D, XC17256D			50.0	µA
	Supply current, standby mode, XC1718D, XC1736D, XC1765D			1.5	mA
I_L	Input or output leakage current		-10.0	10.0	µA

Note: During normal read operation V_{PP} ***must*** be connected to V_{CC}

XC1718L, XC1765L, XC17128L and XC17256L

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +6.0	V
V_{PP}	Supply voltage relative to GND	-0.5 to +12.5	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

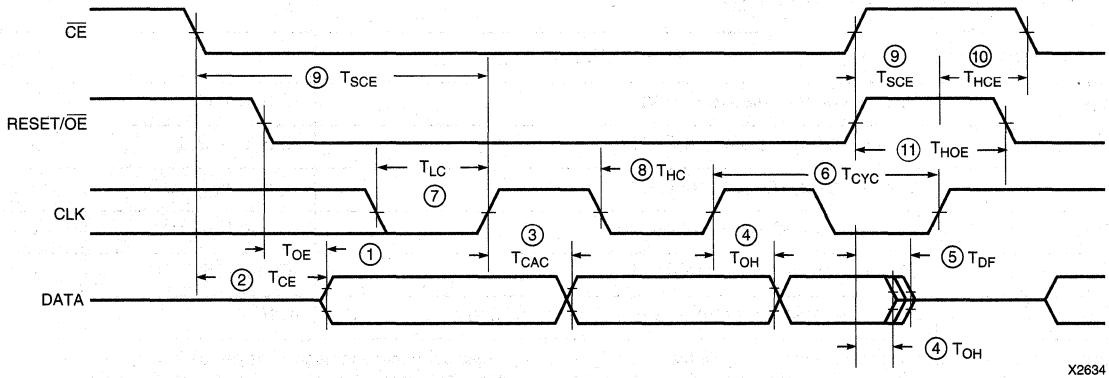
Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND 0°C to +70°C junction	3.0	3.6	V

DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)		0.4	V
I_{CCA}	Supply current, active mode		5.0	mA
I_{CCS}	Supply current, standby mode, XC1718L, XC1765L Supply current, standby mode, XC17128L, XC17265L		1.5 50.0	mA µA
I_L	Input or output leakage current	-10.0	10.0	µA

Note: During normal read operation V_{PP} ***must*** be connected to V_{CC}

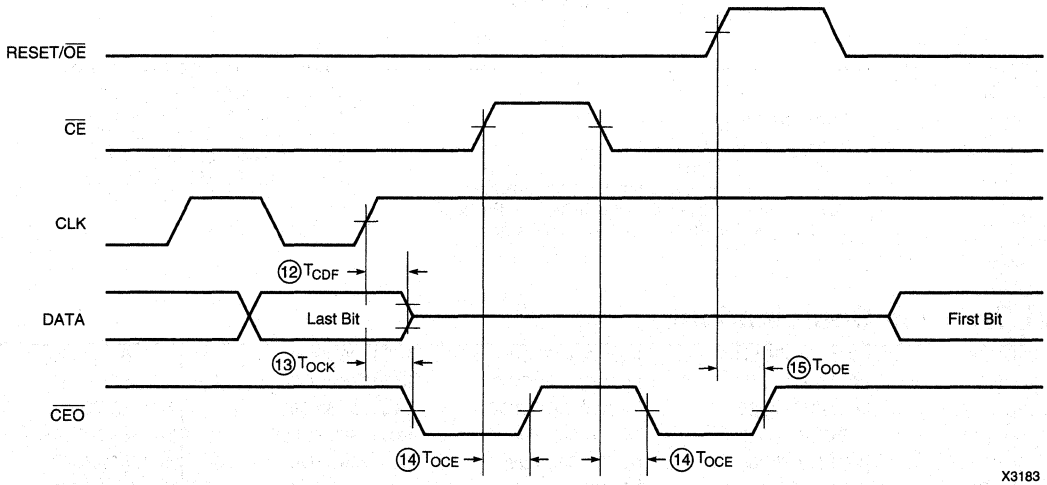
AC Characteristics Over Operating Condition



Symbol		Description	XC1718D XC1736D XC1765D		XC1718L XC1765L		XC17128D XC17256D		XC17128L XC17256L		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
1	T_{OE}	$\overline{OE}$ to Data Delay		45		45		25		30	ns
2	T_{CE}	$\overline{CE}$ to Data Delay		60		60		45		60	ns
3	T_{CAC}	CLK to Data Delay		150		200		50		60	ns
4	T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		0		0		ns
5	T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay[2]		50		50		50		50	ns
6	T_{CYC}	Clock Periods	200		400		80		100		ns
7	T_{LC}	CLK Low Time[3]	100		100		20		25		ns
8	THC	CLK High Time[3]	100		100		20		25		ns
9	TSCE	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25		40		20		25		ns
10	T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		0		0		0		ns
11	T_{HOE}	$\overline{OE}$ Hold Time (guarantees counters are reset)	100		100		20		25		ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with minimum tester ac load and maximum dc load.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

AC Characteristics Over Operating Condition (continued)



Symbol		Description	XC1718D XC1736D XC1765D		XC1718L XC1765L		XC17128D XC17256D		XC17128L XC17256L		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
12	T_{CDF}	CLK to Data Float Delay[2]		50		50		50		50	ns
13	T_{OCK}	CLK to $\overline{CEO}$ Delay		65		65		30		30	ns
14	T_{OCE}	CE to $\overline{CEO}$ Delay		45		45		35		35	ns
15	T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		40		40		30		30	ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with minimum tester ac load and maximum dc load.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

Ordering Information

XC1736D - PC20 C

Device Number
XC1718D
XC1718L
XC1736D
XC1765D
XC1765L
XC17128D
XC17128L
XC17256D
XC17256L

Package Type
PD8 = 8-Pin Plastic DIP
DD8 = 8-Pin CerDIP
SO8 = 8-Pin Plastic Small-Outline Package
VO8 = 8-Pin Plastic Small-Outline Thin Package
PC20 = 20-Pin Plastic Leaded Chip Carrier

Operating Range/Processing
C = Commercial (0° to +70°C)
I = Industrial (–40° to +85°C)
M = Military (–55° to +125°C)
B = Military (–55° to +125°C)
MIL-STD-883 Level B compliant

Valid Ordering Combinations

XC17128DPD8C	XC1718DPD8C	XC17256DPD8C	XC1736DPD8C	XC1765DPD8C
XC17128DVO8C	XC1718DSO8C	XC17256DVO8C	XC1736DSO8C	XC1765DSO8C
XC17128DPC20C	XC1718DVO8C	XC17256DPC20C	XC1736DVO8C	XC1765DVO8C
XC17128DPD8I	XC1718DPC20C	XC17256DPD8I	XC1736DPC20C	XC1765DPC20C
XC17128DVO8I	XC1718DPD8I	XC17256DVO8I	XC1736DPD8I	XC1765DPD8I
XC17128DPC20I	XC1718DSO8I	XC17256DPC20I	XC1736DSO8I	XC1765DSO8I
XC17128DDD8M	XC1718DVO8I	XC17256DDD8M	XC1736DVO8I	XC1765DVO8I
	XC1718DPC20I	XC17256DDD8B	XC1736DPC20I	XC1765DPC20I
			XC1736DDD8M	XC1765DDD8M
				XC1765DDD8B
XC17128LPD8C	XC1718LPD8C	XC17256LPD8C		XC1765LPD8C
XC17128LVO8C	XC1718LSO8C	XC17256LVO8C		XC1765LSO8C
XC17128LPC20C	XC1718LVO8C	XC17256LPC20C		XC1765LVO8C
XC17128LPD8I	XC1718LPC20C	XC17256LPD8I		XC1765LPC20C
XC17128LVO8I	XC1718LPD8I	XC17256LVO8I		XC1765LPD8I
XC17128LPC20I	XC1718LSO8I	XC17256LPC20I		XC1765LSO8I
	XC1718LVO8I			XC1765LVO8I
	XC1718LPC20I			XC1765LPC20I

Marking Information

Due to the small size of the serial PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.

1736D P C

Device Number
XC1718D
XC1718L
XC1736D
XC1765D
XC1765L
XC17128D
XC17128L
XC17256D
XC17256L

Package Type
P = 8-Pin Plastic DIP
D = 8-Pin CerDIP
S = 8-Pin Plastic Small-Outline Package
V = 8-Pin Plastic Small-Outline Thin Package
J = 20-Pin Plastic Leaded Chip Carrier

Operating Range/Processing
C = Commercial (0° to +70°C)
I = Industrial (–40° to +85°C)
M = Military (–55° to +125°C)
B = Military (–55° to +125°C)
MIL-STD-883 Level B compliant

3.3 V and Mixed Voltage Compatible Products

3.3 V and Mixed Voltage Compatible Products

August 6, 1996 (Version 1.1)

In anticipation of the market shift from 5 V to 3.3 V products, Xilinx introduced the Zero+ product line, the industry's first 3.3 V FPGAs, in 1993. The number of 3.3 V product offerings has since tripled and includes high-performance devices with system clock speeds of 85 MHz, high-density devices, and mixed-voltage devices.

Complete data sheets for the products mentioned below can be found in Chapters 3, 4, and 5 of this Data Book. 3.3 V versions of the Serial PROM devices also are available (see Chapter 6).

FPGAs

The Zero+ Family of Ultra Low Power Devices: XC3000L, XC4000L

The Zero+ Product Line includes two major families: the XC3000L and XC4000L FPGAs. These devices have quiescent supply currents below 1mA, with some below 50 µA. This is important in systems where prolonged battery life is critical.

3 V PCI-Compliant FPGA: XC3100L

The XC3100L is the highest performance 3.3 V FPGA, and is the only 3.3 V FPGA family that meets the stringent specifications of 3.3 V PCI applications.

High-Density FPGAs With On-Chip RAM: XC4000L and XC4000XL

Ranging from 5,000 to over 60,000 gates, the XC4000L and XC4000XL FPGA families represent the broadest 3.3 V product line in the industry.

High-Density FPGAs Without On-chip RAM: XC5200L

The XC5200L family features 5 V compatible inputs and densities from 2,000 to 23,000 gates.

5 V Compatible Inputs on 3.3 V Devices

Conventional 3.3 V device inputs cannot or should not be driven substantially higher than 3.6 V. The new XC5200L inputs can, however, be driven up to 5.5 V, provided that the 5 V supply voltage is connected to one dedicated bias supply pin, called V_{TT}, on the 3.3 V device.

All Xilinx device inputs maintain their excellent protection against Electro-Static Discharge (ESD), typically 10,000 V, even in mixed-voltage applications.

5 V SRAM FPGAs for Mixed-Voltage Systems: XC4000E and XC4000EX

While the market slowly shifts from 5V systems to 3.3V systems, a need exists for devices to function in dual environments. The 5 V XC4000E and XC4000EX FPGA families feature a unique output structure which makes them suitable for mixed-voltage system applications. When configured in TTL mode, the XC4000E and XC4000EX can be directly mixed with 3.3 V devices without the aid of external components such as current limiting resistors. This is described in more detail under, "Interfacing Between 5 V and 3.3 V Devices" on page 7-2.

CPLDs

5 V CPLDs for Mixed-Voltage Systems: XC7300 and XC9500

Xilinx CPLDs are an excellent fit for 5 V only and mixed-voltage systems. The Input/Output (I/O) ring can be powered by either a 5 V V_{CCIO} or a 3.3 V V_{CCIO}. Independent of the V_{CCIO} voltage level, the inputs can accept 5 V and 3.3 V inputs. The rail-to-rail output level is defined by V_{CCIO}. These single-chip solutions function extremely well in mixed-voltage systems without any performance penalty.

Supply Voltage Options

	Availability	Single 3.3 V Supply	Single 5 V Supply	Dual Supply	Mixed-Voltage Applications			Key Features
					Core VCC = 5 V I/O VCC = 3.3 V Inputs are 5 V Compatible	VCC = 5 V Inputs are 3.3 V Compatible	VCC = 3.3 V Inputs are 5 V Compatible[1]	
Reconfigurable FPGAs						**Yes**		
XC3000A	Now		Yes					Low quiescent current
XC3000L	Now	Yes						µA powerdown current and µA quiescent current
XC3100A	Now		Yes			**Yes**		Highest performance 5 V FPGA
XC3100L	Now	Yes						Highest performance 3.3 V FPGA
XC4000E	Now		Yes			**Yes**		Mixed voltage system capable
XC4000L	Now	Yes						High Density 3.3 V FPGAs
XC4000EX	2H96		Yes			**Yes**		Mixed voltage system capable
XC4000XL	2H96	Yes		Note 2			Note 2	Highest Density 3.3 V FPGA
XC5200	Now		Yes			**Yes**		Best value and broadest density FPGAs
XC5200L	4H96	Yes		Yes			**Yes**	Best 3.3 V FPGA value
CPLDs								
XC7300	Now		Yes	Yes	Yes	**Yes**		Mixed voltage system capable
XC9500	2H96		Yes	Yes	Yes	**Yes**		Mixed voltage system capable

Notes: 1. Provided VTT pin is connected to 5 V supply.
2. Initial XC4000XL devices do not have 5 V tolerant inputs. Future XC4000XL devices will have 5 V tolerant inputs. Contact the factory.

Interfacing Between 5 V and 3.3 V Devices

This section discusses the compatibility issues between devices with different supply voltages, and explains how 5 V XC4000E/EX devices are directly compatible with 3.3 V devices.

In the past, almost all digital logic devices used a 5 V supply voltage. To reduce chip size and meet the demand for higher integration and lower power consumption, the semiconductor industry has started the transition to 3.3 V logic. In the future, 3.3 V will become the dominant supply voltage. Today, many designs must accommodate both types of ICs on the same board. Since both types of supply share a common ground, there are no problems interfacing logic Low levels in either direction, but there are compatibility issues for the logic High levels.

3.3 V Devices Driving Inputs on 5 V Devices

The lowest output High voltage (VOH) of the 3.3 V device must exceed the VIH requirements of the 5 V device. This is not a problem if the 5 V device uses TTL-compatible input thresholds, available on all Xilinx devices. If, however, the 5 V device has CMOS input thresholds, an external pull-up resistor to 5 V on each such input will assure a sufficiently high input voltage. The resistor should be somewhere between 10 kΩ and 1 kΩ in value. The upper limit causes the rising input transition to be slow; the lower limit is set by the output current sinking capability of the 3.3 V device output. In the High state, the voltage will be clamped by the ESD protection diode of the 3.3 V device, as described later in this application note. With less than 1.5 V across this resistor, the current will be fairly small, but care should be taken that the sum of these pull-up currents does not exceed the 3.3 V supply current, thereby reverse-biasing the power supply and raising the 3.3 V supply voltage to an undefined level (but obviously lower than the 5 V V_{CC} minus a diode drop of ~0.7 V).

5 V Devices Driving Inputs on 3.3 V Devices

The highest 5 V device output voltage must not force excessive current into the input of the 3.3 V device. If the 5 V device has a truly complementary CMOS output (like all Xilinx FPGAs and CPLDS except the XC4000 family devices have), then the input current must be limited by a series resistor of no less than 150 Ω. This guarantees an input current below 10 mA, flowing through the ESD input protection diode backwards into the 3.3 V supply. That amount of input current is generally considered safe, causing neither metal migration nor latch-up problems. Care must be taken to avoid forcing the nominally 3.3 V supply voltage above its 3.6 V maximum whenever a large number of active High inputs drive the 3.3 V device, potentially causing the 3.3 V supply current to go negative.

If the 5 V device has "totem-pole" n-channel-only outputs, VOH is reduced by one threshold and the series resistor can be eliminated, provided the nominally 5 V supply does

not exceed 5.25 V. This is described in detail in the following section.

XC4000E/EX is Fully Compatible With 3.3 V Logic

As a default option, all XC4000E/EX have a TTL-like input threshold (compatible with 3.3 V output levels) and an n-channel-only "totem-pole" or TTL-like output structure with an n-channel transistor pulling the output to a VOH level that is one threshold below V_{CC}.

At a nominal 5.0 V V_{CC}, the unloaded output High voltage VOH is <3.7 V. When applied to the input of a device with a nominal 3.3 V V_{CC}, there is no additional input current, and the input level does not violate the conventional specification that prohibits input voltages more than 0.5 V above V_{CC}. See Figure 1.

If both 5 V and 3.3 V supply voltages track reasonably between their max and min values, there will never be any additional input current in excess of 1 µA at any commercial or industrial operating temperature.

A worst-case analysis of the interface might assume the (unrealistic) condition where the 5 V supply is at its max value (5.25 V for commercial applications), while the 3.3 V supply is at its min value of 3.0 V. Under these conditions, the interface violates the conventional specification, and drives current into the input of the 3.3 V device, as shown in figure 2. The following paragraphs explain that this interface is nevertheless reliable.

For protection against electro-static discharge (ESD), all CMOS inputs and I/O pins usually have a diode between the pin and the nearest V_{CC} connection. This diode prevents the input from going substantially more positive than V_{CC}, which might destroy the input transistor by rupturing its gate oxide. At room temperature, this ESD protection diode conducts negligible current at < 0.6 V forward bias, and conducts ~1 mA at ~0.7 V forward bias, typical for any silicon junction diode. These voltages have a predictable negative temperature coefficient of –2 mV per degree C. At 85 degrees C, these voltages are, therefore 120 mV lower.

Figure 1 superimposes the output characteristic of the XC4000E/EX and the input current characteristic of a typical 3.3 V device input. Both supply voltages are at their nominal value, but the die temperatures are at their worst-case value of 85 degrees C, and worst-case processing is assumed.

Figure 2 shows the same curves, but with 5.25 V and 3.0 V V_{CC} respectively. The intersection of the two curves defines the worst-case operating point of 3.8 V and 6 mA. That means that the XC4000E output drives 6 mA into the forward-biased ESD protection diode, raising the input voltage 0.8 V above 3.0 V, the assumed lowest value of the nominally 3.3 V supply voltage.

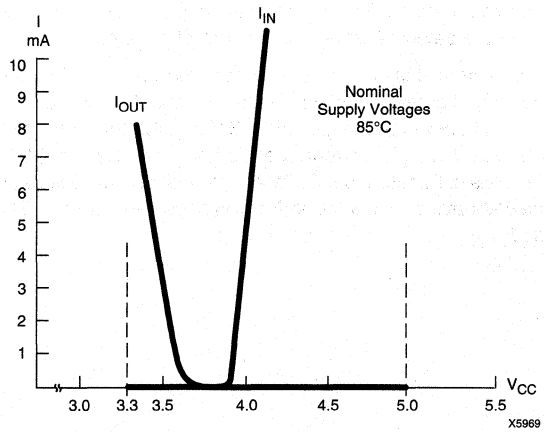


Figure 1: XC4000E Output in "TTL-Mode" driving 3.3 V Device Input with Both Supplies at Nominal Voltage (5.0 V and 3.3 V)

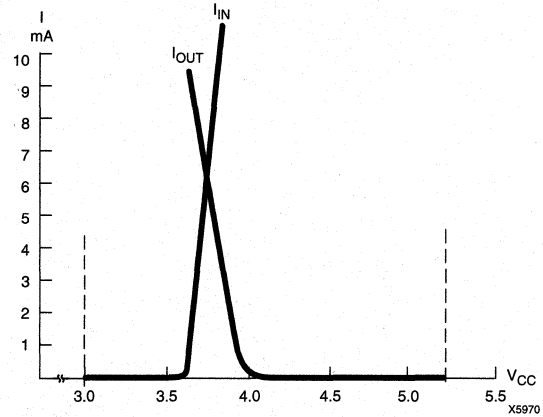


Figure 2: XC4000E Output in "TTL-Mode" driving 3.3 V Device Input with Both Supplies at Extreme Values (5.25 V and 3.0 V)

Although this input condition is not covered by the conventional specification, it does not cause any harm and does not affect reliability. ESD protection diodes are designed to conduct hundreds of mA, and the absolute value of the input voltage with respect to ground will never exceed 3.9 V. If the input pin is part of an I/O structure, there is theoretically possibility of causing latch-up, but all reputable IC manufacturers design their circuits such that latch-up does not occur below 100 mA of input current per pin.

The system designer must estimate the sum of all maximum input currents, and calculate the impact of this current flowing backwards towards the 3.3 V supply. But even if the total 3.3 V supply current goes to zero, V_{CC} for the 3.3 V device is still limited to < 3.6 V (the highest output voltage of the 5 V device minus the forward voltage drop of the ESD diode).

Conclusion

5 V XC4000E/EX devices can be freely mixed with 3.3 V devices, without any current or voltage limiting interface resistors, if the following conditions are met:

- The 5 V XC4000E/EX devices are in their default "TTL mode" with respect to input thresholds and output levels.
- The upper limit on the 5 V V_{CC} is 5.25 V and the lower limit on the 3.3 V supply is 3.0 V, as per standard commercial specifications.
- For industrial operating conditions with higher Vcc max, the user must make sure that the absolute difference between the two supply voltages does not exceed 2.20 V. Specifically, if the nominally 5 V V_{CC} is at its max value of 5.50 V, the nominally 3.3 V V_{CC} must not be lower than 3.30 V.

HardWire Products Table of Contents

Xilinx HardWire™ Array Overview

Xilinx HardWire™ Array Overview

August 6, 1996 (Version 1.1)

Features

- Mask-programmed versions of Xilinx programmable devices
  - Specifically designed for easy conversions
  - Significant cost reduction for high-volume applications
  - Same specifications and architecture as the programmable devices
  - On-chip scan path test registers
  - High-performance CMOS process
- Easy conversion with guaranteed results
  - "Design Once Methodology" requires no customer engineering resources for conversion
  - Fully pin-for-pin compatible with the programmable device
  - Support for most popular package types
  - PLD database file used to generate production-ready prototypes
  - Automatic test vector generation with >95% fault coverage
  - Prototypes built on production line

The following is an overview of the Xilinx HardWire device product line. Product specifications for the HardWire devices and additional information are available in a separate publication - The HardWire Data Book.

HardWire Arrays are mask-programmed versions of the popular XC2000, XC3000, XC4000, and XC5000 series FPGAs, as well as the XC9500 CPLDs. The HardWire devices provide a transparent migration path from a programmable logic device to a cost-reduced device without the engineering burden associated with conventional gate-array re-design.

In standard programmable logic, the functions and interconnections are determined by configuration data stored in memory cells. In the HardWire components, the memory cells and the logic they control are replaced by metal connections. All other circuitry in the HardWire devices is identical to the corresponding programmable logic's internal circuitry. Thus, a HardWire device is a semicustom device manufactured to provide a specific functionality, yet is completely compatible with the programmable device it replaces.

Advantages of Using Xilinx HardWire Arrays

Xilinx offers an easy, seamless process for achieving the shortest Time-to-Volume solution possible. Simply stated, our unique Design Once methodology allows engineers to develop their design in a programmable device, then switch to a lower cost mask-programmed product without utilizing additional internal resources.

Production is often started using the same programmable logic in which the application was designed. This flexibility allows the product to be introduced to the market quickly. Later in the production process, the PLD can be replaced with a HardWire Array without expending additional engineering time and effort to redesign either the FPGA's circuit or the printed circuit board. Other conversion methodologies introduce risk at each project milestone of the conversion process. Only the Xilinx Design Once Methodology can offer this no risk, 100% pin-for-pin compatible path to dramatic cost reductions.

Whenever a system incorporating Xilinx PLDs ramps to high production volumes, the HardWire mask-programmed solution should be the first consideration for cost reduction. Because the HardWire implementation dramatically reduces the die size by removing programmable elements, the resulting device is much smaller than the equivalent PLD. This smaller die provides a no-risk path to achieve dramatic cost reductions.

HardWire versus Full ASIC Gate Array Implementation

Converting a device from programmable logic to a HardWire Array has many advantages over generic gate array redesign. The most important is that the Xilinx HardWire methodology requires no additional customer engineering to convert the programmable logic design into a fully tested, completely verified mask-programmed design.

This ease of conversion is available only through Xilinx because the PLD database file is the actual physical data base previously created and verified in the process of developing the PLD design. Xilinx has the only methodology that preserves all attributes of the original physical data base file. If the design is mapped to a third party library for conversion at the schematic level to another technology, the design must be verified and prototyped. Third party implementation will change the placement and routing, thereby changing the design's performance characteristics.

Thus, the revised device needs to be re-verified and re-tested in the system to be certain both the functionality and the performance still meet the application's requirements.

A comparison of the activities required to convert a HardWire Array versus a standard array is shown in Figure 1.

Reverifying the Design

In conventional gate array conversion (redesign), the design must be re-verified after the schematic is translated or recaptured. The process of reverifying a design is rigorous and time-consuming. Functional simulation vectors need to be created, and the device must be exhaustively simulated before and after place and route. A suitable test methodology must be considered and implemented.

In contrast, no additional effort is required when converting to Xilinx HardWire Arrays. The HardWire design is self-verifying because the actual PLD database file is used for the conversion.

Fault Coverage and Test Vectors

All designs need to be testable. In a traditional mask-programmed gate array, the designer is required to build in testability and generate test vectors that verify chip performance by exercising as much of the device's circuitry as possible. Most designers strive for greater than 95% fault coverage. However, they often settle for significantly less because the iterative process is extremely time consuming and increases exponentially as fault coverage is increased.

Any third-party conversion from a Xilinx FPGA or CPLD to a gate array or other similar technology will require test vector generation. Typically, the original designers create the test vectors, since they are most familiar with the design implementation. This method ties up valuable design resources and reverses the value of the original decision to use programmable logic for their ease of design and time-to-market advantages. Another alternative is to contract with the conversion or gate array vendor to create the test vectors. This method can be both time-consuming and expensive, since vendors usually charge by the vector. In some cases, conversion or gate array vendors will accept a design without test vectors, but the customer accepts all the liability of determining whether the resulting device is production worthy. In today's competitive market, many projects can not afford the risk of possible respins if the design doesn't work.

Converting from a Xilinx programmable to a HardWire device requires no test vector generation. Xilinx guarantees greater than 95% fault coverage through a proprietary Automatic Test Vector Generation methodology. All HardWire Arrays are 100% fully guaranteed to work in the user's application exactly like the programmable logic.

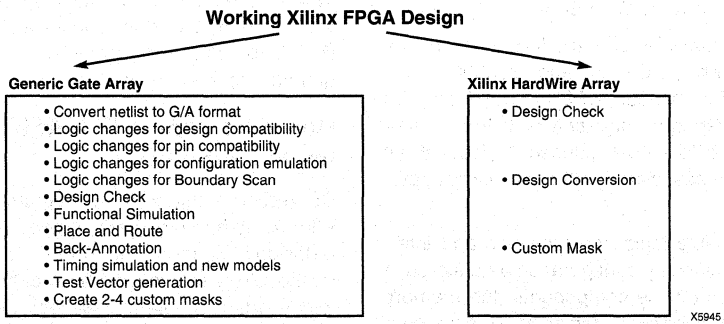


Figure 1: Steps Involved in Converting a PLD Design to a Gate Array as Compared to a Hard Wire Array

Packaging and Silicon Considerations

All of the physical attributes of the HardWire Arrays are virtually identical to the programmable logic devices. Xilinx uses the same qualified fabrication facilities for both the PLD and HardWire devices. The same IC process, as well as packaging, assembly, and test facilities, are used. This allows users to circumvent costly and time-consuming requalification efforts.

Converting from a Xilinx programmable logic device to anything but a Xilinx HardWire Array means a change to silicon, packaging, assembly and test. Each of these changes adds an element of risk into the qualification process.

Support for the Entire Product Life Cycle

Figure 2 shows the typical life cycle of a high-volume product, and illustrates the optimal way for using the programmable and HardWire devices.

During the development, prototype, and initial production stages, the programmable device is the best choice. Later in the life-cycle, when the design is stable and in high volume production, the HardWire Array can be used in place of the original programmable device.

Since the circuit board was designed initially for a programmable device, production can be switched back from the HardWire Array to the programmable device if the situation warrants. For example, if demand for the product increases dramatically, production can be increased in days or weeks by using programmable devices. In addition, a change can be quickly made to the product, since there is no manufacturing lead-time for an off-the-shelf programmable device. Production can be switched to programmable devices as the product nears the end of the life cycle, avoiding end-of-life buys and the risk of obsolescence.

Furthermore, designs implemented with multiple static RAM-based FPGAs can be cost reduced incrementally, converting one or more of the programmable devices while leaving the others for future conversion. As each PLD is converted to a Xilinx HardWire Array, the user enjoys a lower cost for that unit, while maintaining the ease-of-use of off-the-shelf programmable logic in the other sockets. When all of the devices are converted, the storage element can then be removed, giving even further cost reductions. This flexibility is unique to Xilinx, and allows OEMs to achieve cost reductions quickly with minimal effort.

The HardWire Product Series

As listed in Table 1, the HardWire product chart, there is a range of products available for Xilinx FPGAs and XC9500 CPLDs. For designs developed using the Xilinx XC4000 family, there are two HardWire options. The XC4400 family is based on Xilinx advanced technology. It is most beneficial for higher volume applications, as well as XC4000E designs utilizing Xilinx's Select-RAM™ features, and low power 3.3 volt designs. For an application with low annual volumes (as low as 1500 units) and where a low NRE is required, the XC4300 family provides the best fit. Xilinx also supports the low-power 3.3 volt XC2000L and XC3000L.

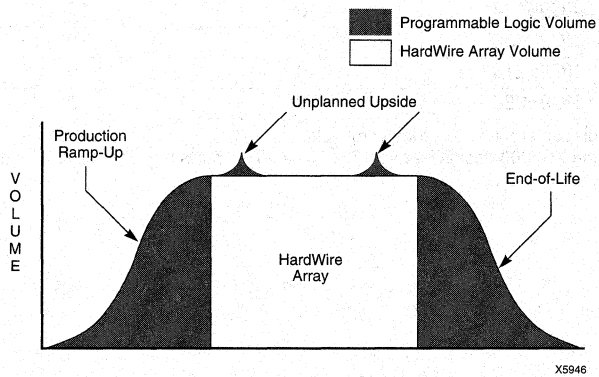


Figure 2: Typical High Volume Product Life Cycle

Table 1: HardWire Product Chart[1]

PLD Family	H/W Equivalent	Minimum Order Quantity (KU)	Minimum Shipment (KU)	Production Availability
XC2000	XC2300	7	2	Now
XC3000/A	XC3330	10	2	
XC3100A	XC3342	6	1	
	XC3390	4	0.5	
XC3195	XC4495T	10	2	
XC4000/E[2]	XC4303	6	2	
	XC4305	4	1	
	XC4310	1.5	0.4	
	XC4313	1.5	0.4	
	XC4403/H	10	2	
	XC4405/H	10	2	
	XC4406	5	1	
	XC4408	5	1	
	XC4410	5	1	
	XC4413	3.5	0.5	
	XC4425	2.5	0.5	
XC4000EX	XH4028EX	2.5	0.5	Q4/96
	XH4036EX	2.5	0.5	Q4/96
	XH4044EX	2.5	0.5	Q1/97
	XH4052EX	2.5	0.5	Q1/97
	XH4062EX	2.5	0.5	Q1/97
XC5200	XC5402	10	2	Now
	XC5404	10	2	
	XC5406	5	1	
	XC5410	5	1	
	XC5415	3.5	0.5	
XC9500	XC95144	10	10	Q2/97
	XC95180	10	10	
	XC95216	10	10	
	XC95288	10	10	

Notes: 1. Industrial temperature grades are available for all products.
2. The XC4300 supports the XC4000 design features. The XC4400 supports both the XC4000 and XC4000E design features.

High-Reliability and Military Products

High-Reliability and Military Products

June 1, 1996 (Version 1.0)

Xilinx is the world's leading supplier of High-Reliability Programmable Logic Devices (Hi-REL PLDs) to the aerospace, military, defense electronics, and related markets. These devices are being used in a wide variety of programs, including applications such as electronic warfare, missile guidance and targeting, RADAR/SONAR, communications, signal processing, aerospace and avionics.

Unmatched Hi-Rel Product Offering

Xilinx offers a wide variety of devices, delivering the fastest and biggest Hi-Rel devices available. Products with up to 25,000 gates are available today, with even higher densities to come. Xilinx offers multiple product families to allow you to select the right device to meet your design requirements.

This broad range of devices is available in a wide variety of speed and package options. Both military temperature range and full MIL-STD-883B/SMD versions are available as standard, off-the-shelf products, in through-hole and surface mount packages.

Committed to the Hi-Rel Market

Xilinx understands that you need to be able to count on your Hi-Rel supplier. Xilinx is committed to our customers, and we are expanding our Hi-Rel support and product portfolio. The unique capabilities of the Xilinx FPGA solution provide increased design flexibility, field-upgradability and system feature integration, while eliminating the NREs, lead-time and inventory problems of custom logic and gate arrays. Now more than ever, Xilinx is your Hi-Rel logic solution.

Xilinx Hi-Rel Products

Table 1 summarizes Xilinx high density and high performance product offerings. The following pages contain a complete listing of current Xilinx SMD (Standard Microcircuit Drawings) devices and "B" grade equivalents. Architectural descriptions for these FPGA products can be found in Chapter 4. For additional information, including Data Sheets on Hi-Rel devices, contact the nearest Xilinx Sales Office or Sales Representative.

Table 1: High Density and High Performance Products

Family	Devices	Features
XC4000/E	XC4003A XC4005/E XC4010/E XC4013/E XC4025E	Highest Density/Most Features Family • 3,000-25,000+ gates • Up to 256 user-definable I/Os • Extensive system features include on-chip user RAM, built-in 1149.1 test support and fast carry logic
XC3100A	XC3142A XC3190A XC3195A	Highest Performance Family • 2,500-7,500 gates • Up to 144 user-definable I/Os

Table 2: Xilinx SMD (Standard Microcircuit Drawing)

XC1700 Products

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9471701MPA	XC1765DDD8B		DD8	TOP
5962-9561701MPA	XC17256DDD8B		DD8	TOP

XC2000 Products

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-8863801XC	XC2018-33PG84B	-33	PG84	TOP
5962-8863802XC	XC2018-50PG84B	-50	PG84	TOP
5962-8863803XC	XC2018-70PG84B	-70	PG84	TOP
5962-8863804XC	XC2018-100PG84B	-100	PG84	TOP

XC3000 Products

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-8994801MXC	XC3020-50PG84B	-50	PG84	TOP
5962-8994802MXC	XC3020-70PG84B	-70	PG84	TOP
5962-8994803MXC	XC3020-100PG84B	-100	PG84	TOP
5962-8994801MNC	XC3020-50CB100B	-50	CB100	BASE
5962-8994802MNC	XC3020-70CB100B	-70	CB100	BASE
5962-8994803MNC	XC3020-100CB100B	-100	CB100	BASE
5962-8994801MMC		-50	CB100	LID
5962-8994802MMC		-70	CB100	LID
5962-8994803MMC		-100	CB100	LID
5962-8994801MYA*	XC3020-50CQ100B	-50	CQ100	BASE
5962-8994802MYA*	XC3020-70CQ100B	-70	CQ100	BASE
5962-8994803MYA*	XC3020-100CQ100B	-100	CQ100	BASE
5962-8994801MTA*		-50	CQ100	LID
5962-8994802MTA*		-70	CQ100	LID
5962-8994803MTA*		-100	CQ100	LID

* Do Not Use for New Designs (package to be obsoleted). Use "CB" Package Instead.

XC3000 Products (continued)

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-8971301MXC	XC3042-50PG84B	-50	PG84	TOP
5962-8971302MXC	XC3042-70PG84B	-70	PG84	TOP
5962-8971303MXC	XC3042-100PG84B	-100	PG84	TOP
5962-8971301MZC	XC3042-50PG132B	-50	PG132	TOP
5962-8971302MZC	XC3042-70PG132B	-70	PG132	TOP
5962-8971303MZC	XC3042-100PG132B	-100	PG132	TOP
5962-8971301M9C	XC3042-50CB100B	-50	CB100	BASE
5962-8971302M9C	XC3042-70CB100B	-70	CB100	BASE
5962-8971303M9C	XC3042-100CB100B	-100	CB100	BASE
5962-8971301MMC		-50	CB100	LID
5962-8971302MMC		-70	CB100	LID
5962-8971303MMC		-100	CB100	LID
5962-8971301MYA*	XC3042-50CQ100B	-50	CQ100	BASE
5962-8971302MYA*	XC3042-70CQ100B	-70	CQ100	BASE
5962-8971303MYA*	XC3042-100CQ100B	-100	CQ100	BASE
5962-8971301MNA*		-50	CQ100	LID
5962-8971302MNA*		-70	CQ100	LID
5962-8971303MNA*		-100	CQ100	LID

* Do Not Use for New Designs (package to be obsoleted). Use "CB" Package Instead.

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-8982301MXC	XC3090-50PG175B	-50	PG175	TOP
5962-8982302MXC	XC3090-70PG175B	-70	PG175	TOP
5962-8982303MXC	XC3090-100PG175B	-100	PG175	TOP
5962-8982301MZC	XC3090-50PG164B	-50	CB164	BASE
5962-8982302MZC	XC3090-70PG164B	-70	CB164	BASE
5962-8982303MZC	XC3090-100PG164B	-100	CB164	BASE
5962-8982301MTC		-50	CB164	LID
5962-8982302MTC		-70	CB164	LID
5962-8982303MTC		-100	CB164	LID
5962-8982301MYA*	XC3090-50CQ164B	-50	CQ164	BASE
5962-8982302MYA*	XC3090-70CQ164B	-70	CQ164	BASE
5962-8982303MYA*	XC3090-100CQ164B	-100	CQ164	BASE
5962-8982301MUA*		-50	CQ164	LID
5962-8982302MUA*		-70	CQ164	LID
5962-8982303MUA*		-100	CQ164	LID

* Package OBSOLETE. Use "CB" Package Instead.

XC3100A Products

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9561001MXC	XC3142A-5PG84B	-5	PG84	TOP
5962-9561002MXC	XC3142A-4PG84B	-4	PG84	TOP
5962-9561001MUC	XC3142A-5PG132B	-5	PG132	TOP
5962-9561002MUC	XC3142A-4PG132B	-4	PG132	TOP
5962-9561001MYC	XC3142A-5CB100B	-5	CB100	BASE
5962-9561002MYC	XC3142A-4CB100B	-4	CB100	BASE
5962-9561001MZC		-5	CB100	LID
5962-9561002MZC		-4	CB100	LID
5962-9561101MXC	XC3190A-5PG175B	-5	PG175	TOP
5962-9561102MXC	XC3190A-4PG175B	-4	PG175	TOP
5962-9561101MYC	XC3190A-5CB164B	-5	CB164	BASE
5962-9561102MYC	XC3190A-4CB164B	-4	CB164	BASE
5962-9561101MZC		-5	CB164	LID
5962-9561102MZC		-4	CB164	LID
5962-9561201MXC	XC3195A-5PG175B	-5	PG175	TOP
5962-9561202MXC	XC3195A-4PG175B	-4	PG175	TOP
5962-9561201MYC	XC3195A-5CB164B	-5	CB164	BASE
5962-9561202MYC	XC3195A-4CB164B	-4	CB164	BASE
5962-9561201MZC		-5	CB164	LID
5962-9561202MZC		-4	CB164	LID

XC4000 Products

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9471201MXC	XC4003A-10PG120B	-10	PG120	TOP
5962-9471202MXC	XC4003A-6PG120B	-6	PG120	TOP
5962-9471201MYC	XC4003A-10CB100B	-10	CB100	BASE
5962-9471202MYC	XC4003A-6CB100B	-6	CB100	BASE
5962-9471201MZC		-10	CB100	LID
5962-9471202MZC		-6	CB100	LID
5962-9225201MXC	XC4005-10PG156B	-10	PG156	TOP
5962-9225202MXC	XC4005-6PG156B	-6	PG156	TOP
5962-9225203MXC	XC4005-5PG156B	-5	PG156	TOP
5962-9225201MYC		-10	CB164	LID
5962-9225202MYC		-6	CB164	LID
5962-9225203MYC		-5	CB164	LID
5962-9225201MZC	XC4005-10CB164B	-10	CB164	BASE
5962-9225202MZC	XC4005-6CB164B	-6	CB164	BASE
5962-9225203MZC	XC4005-5CB164B	-5	CB164	BASE

XC4000 Products (continued)

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9230501MXC	XC4010-10PG191B	-10	PG191	TOP
5962-9230502MXC	XC4010-6PG191B	-6	PG191	TOP
5962-9230503MXC	XC4010-5PG191B	-5	PG191	TOP
5962-9230501MYC	XC4010-10CB196B	-10	CB196	BASE
5962-9230502MYC	XC4010-6CB196B	-6	CB196	BASE
5962-9230503MYC	XC4010-5CB196B	-5	CB196	BASE
5962-9230501MZC		-10	CB196	LID
5962-9230502MZC		-6	CB196	LID
5962-9230503MZC		-5	CB196	LID
5962-9473001MXC	XC4013-10PG223B	-10	PG223	TOP
5962-9473002MXC	XC4013-6PG223B	-6	PG223	TOP
5962-9473001MYC	XC4013-10CB228B	-10	CB228	BASE
5962-9473002MYC	XC4013-6CB228B	-6	CB228	BASE
5962-9473001MZC		-10	CB228	LID
5962-9473002MZC		-6	CB228	LID

Programming Support Table of Contents

HW-130 Programmer

HW-130 Programmer

August 6, 1996 (Version 1.1)

Programs All Xilinx Nonvolatile Devices

- XC1700 Serial PROMs
- XC7000 CPLDs
- XC9500 CPLDs
- Supports all Xilinx package types

Programmer Accessories

- Universal international power supply
- Power cord options for US/Asia, UK, EU and KK standards.
- Serial download cable and adapters
- Users manual

Interface Software and System Requirements

The programmer software operates on a variety of different platforms. Table 1 indicates the minimum system requirements for each of the supported platforms. In all cases, a 3.5" disk drive or a CD-ROM drive and an RS-232 serial port are required. A mouse is recommended.

Programmer Functional Specifications

- Device programming and verification
- CPLD security control
- PROM reset polarity control
- Checksum calculation and comparison
- Blank check and signature ID tests
- Master device program upload
- File transfer and comparison
- Self check and auto calibration

Programming Socket Adapters

- Supports all package styles: PLCC, PQFP, BGA, SOIC, VOIC, PGA and DIP
- CPLD adapters for the HW-120 may be used on the HW-130

Electrical Requirements and Physical Specifications

- Operating voltage: 100-250 VAC, 50-60 Mhz
- Power consumption: 1.0 Amps
- Dimensions: 6" x 7.75" x 2"
- Weight: 1 lb.
- Safety standards: approved by UL, CSA, TUV

New Programming Algorithm Support

- Available via the Xilinx BBS and e-mail.
- Send e-mail to xdocs@Xilinx. com with "search hw130" in the subject field.
- For the bulletin board, refer to page 6-2 in the data book. Type "F" and select directory #3. Select either Programming Support or type "Zhw130" to view all HW-130 related files.

Table 1: Interface Software and System Requirements

Requirements	DOS	Windows 3.1	Windows 95	Windows NT	Sun OS	Solaris	HP9000/700	IBM RS6000
Memory Needed	540KB	4MB	8MB	16MB	—	—	—	—
Hard Disk Space	2MB	2MB	2MB	2MB	1MB	1MB	1MB	1MB
System Software	3.3 or greater	3.1 or greater	4.00	3.1 or greater	SunOS 4.1.3 or greater, X11R5 with Motif 1.2 or greater	SunOS 5.4 or greater, X11R5 with Motif 1.2 or greater	HP-UX A09.05 or greater, X11R5 with Motif 1.2 or greater	AIX 3.2 or greater, X11R5 with Motif 1.2 or greater

Adapter Selector Table

Product Family	Package Types	Adapter P/N
XC7200A	PLCC/CLCC 44	HW-132-PC44
XC7200A	PLCC/CLCC 68	HW-132-PC68
XC7200A	PLCC/CLCC 84	HW-132-PC84
XC7200A	PGA 84	HW-132-PG84
XC7300	PLCC/CLCC 44	HW-133-PC44
XC7300	PQFP 44	HW-133-PQ44
XC7300	VQFP 44	HW-133-VQ44
XC7300	PLCC/CLCC 68	HW-133-PC68
XC7300	PLCC/CLCC 84	HW-133-PC84
XC7300	PQFP 100	HW-133-PQ100
XC7300	PGA 144	HW-133-PG144
XC7300	PQFP 160	HW-133-PQ160
XC7300	BGA 225	HW-133-BG225
XC1700	DIP 8	HW-137-DIP8
XC1700	PLCC20/SO8/VO8	HW-137-PC20/SO8
Calibration Adapter		HW-130-CAL

Packages and Thermal Characteristics Table of Contents

Packages and Thermal Characteristics

Number of Available I/O Pins

	Max I/O	44	64	68	84	100	120	132	144	156	160	164	175	176	191	196	208	223	225	228	240	299	304	352	411	432	499
XC7236A	36	36																									
XC7272A	72			56	72																						
XC7318	38	38																									
XC7336	38	38																									
XC7336Q	38	38																									
XC7354	58	38		58																							
XC7372	84			57	72	84																					
XC73108	120				72	84			120		120								120								
XC73144	156										136								156								
XC9536	34	34																									
XC9572	72				69	72																					
XC95108	108				69	81					108																
XC95144	133					81					133																
XC95180	168										133						168										
XC95216	168										133						168										
XC95288	192																168						192				
XC95432	240																						240				
XC95576	240																						240				
XC3020/A/L & XC3120A	64			58	64	64																					
XC3030/A/L & XC3130A	80	34	54	58	74	80																					
XC3042/A/L & XC3142A/L	96				74	82		96	96																		
XC3064/A/L & XC3164A	120				70			110	110		120																
XC3090/A/L & XC3190A/L	144				70				120		138	144	144	144			144										
XC3195A	176				70						138		144				176	176									
XC4003E	80				61	77	80																				
XC4005E	112				61	77			112	112	112	112					112										
XC4005L	112				61												112										
XC4006E	128				61				113	125	128						128										
XC4008E	144				61						129				144		144										
XC4010E	160				61						129				160	160	160		160								
XC4010L	160				61									153			160										
XC4013E	192										129						160	192	192	192	192						
XC4013L	192																160		192		192						
XC4020E	224																160	192			193						
XC4025E	256																	192		192	193	256	256				
XC4028EX	256																160				193	256	256	256			
XC4028XL	256																160				193	256	256	256			
XC4036EX	288																						256		288	288	
XC4036XL	288																						256		288	288	

Number of Available I/O Pins (Continued)

	Max I/O	44	64	68	84	100	120	132	144	156	160	164	175	176	191	196	208	223	225	228	240	299	304	352	411	432	499
XC4044EX	320																								320	320	
XC4044XL	320																								320	320	
XC4052XL	352																								352	352	
XC4062XL	384																										384
XC5202	84				65	81			84	84																	
XC5204	124				65	81			117	124	124																
XC5206	148				65	81			117		133			148	148		148										
XC5210	196				65				117		133			149			164	196	196		196						
XC5215	244										133						164		196		197	244	244	244			
XC6209	180																				180	180					
XC6216	242																				199	242					
XC6236	384																										
XC6264	512																										

Package Options

	Surface Mount							Through-hole
	PLCC	**PQFP**	**HQFP**	**TQFP**	**VQFP**	**CQFP**	**BGA**	**PGA**
Standard	JEDEC	EIAJ	EIAJ	EIAJ	EIAJ	JEDEC	JEDEC	JEDEC
Lead Pitch	50 mil	0.65/0.5 mm	0.65/0.5 mm	0.5 mm	0.5 mm	25 mil	1.5 mm	100 mil
Body	Plastic	Plastic	Plastic/Metal	Plastic	Plastic	Ceramic	FR4	Ceramic/ Plastic
Temperature Options	C, I	C, I	C, I	C, I	C, I	M, B	C	C, I, M, B
Ordering Code	PC	PQ	HQ	TQ/HT	VQ	CB	BG	PG, PP
XC7236A	44							
XC7272A	68, 84							84
XC7318	44	44						
XC7336	44	44						
XC7336Q	44	44			44			
XC7354	44, 68							
XC7372	68, 84	100						
XC73108	84	100,160					225	144
XC73144		160					225	184
XC9536	44				44			
XC9572	84	100		100				
XC95108	84	100, 160	100	100				
XC95144		100, 160						
XC95180		160	208					
XC95216		160	208					
XC95288			208, 304					
XC95432			304					
XC95576			304					
XC3020/A/L & XC3120A	68, 84	100				100		84
XC3030/A/L & XC3130A	44, 68, 84	100	100	100	64			84
XC3042/A/L & XC3142A/L	68, 84	100	100, 144	100, 144		100		84, 132
XC3064/A/L & XC3164A	84	160	144	144				132
XC3090/A/L & XC3190A/L	84	160, 208		144, 176		164		175
XC3195A	84	160, 208						175, 223
XC4003E	84	100			100			120
XC4005E	84	100, 160, 208		144		164		156
XC4005L	84	208						
XC4006E	84	160, 208		144				156
XC4008E	84	160, 208						191
XC4010E	84	160, 208				196	255	191
XC4010L	84	208		176				
XC4013E		160, 208, 240	208, 240			228	225	223
XC4013L		208, 240					225	
XC4020E			208, 240					223

Package Options (Continued)

	Surface Mount							Through-hole
	PLCC	**PQFP**	**HQFP**	**TQFP**	**VQFP**	**CQFP**	**BGA**	**PGA**
Standard	JEDEC	EIAJ	EIAJ	EIAJ	EIAJ	JEDEC	JEDEC	JEDEC
Lead Pitch	50 mil	0.65/0.5 mm	0.65/0.5 mm	0.5 mm	0.5 mm	25 mil	1.5 mm	100 mil
Body	Plastic	Plastic	Plastic/Metal	Plastic	Plastic	Ceramic	FR4	Ceramic/ Plastic
Temperature Options	C, I	C, I	C, I	C, I	C, I	M, B	C	C, I, M, B
Ordering Code	PC	PQ	HQ	TQ/HT	VQ	CB	BG	PG, PP
XC4025E			240, 304			228		223, 299
XC4028EX			208, 240, 304				352	299
XC4028XL			208, 240, 304				352	299
XC4036EX			304				432	411
XC4036XL			304				432	411
XC4044EX							432	411
XC4044XL							432	411
XC4052XL							432	411
XC4062XL								499
XC5202	84	100		144	100			156
XC5204	84	100, 160		144	100			156
XC5206	84	100, 160, 208		144, 176	100			191
XC5210	84	160, 208, 240		144, 176			225	223
XC5215		160	208, 240, 304				225, 352	299
XC6209	84		240					299
XC6216	84	240						299
XC6236								
XC6264								

Inches vs. Millimeters

The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25, 50, or 100 mils (0.025", 0.050" or 0.100").

The EIAJ standards for PQFP, HQFP, TQFP, and VQFP packages define package dimensions in millimeters. These packages have a lead spacing of 0.5 mm, except for the 100- and 160-pin PQFP packages, which have a lead spacing of 0.65 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters.

EIA Standard Board Layout of Soldered Pads for QFP Devices

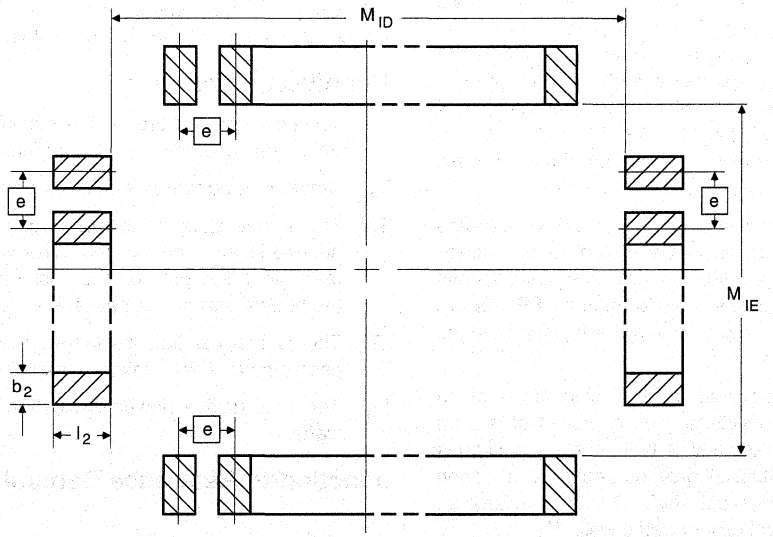


Table 1: Dimensions for Xilinx Quad Flat Packs[1]

Dim.	PQ44	VQ64	PQ100	PQ160	HQ/MQ/PQ208	VQ/TQ100	TQ144	TQ176	HQ/MQ/PQ240	HQ304
M_{ID}	10.40	9.80	20.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
M_{IE}	10.40	9.80	14.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
e	0.80	0.50	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50
b_2	0.4 - 0.6	0.3 - 0.4	0.3 - 0.5	0.3 - 0.5	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4
l_2	1.80	1.60	1.80[2]	1.80	1.60	1.60	1.60	1.60	1.60	1.60

Notes: 1. Dimensions in millimeters
2. For 3.2 mm footprint per MS022, JEDEC Publication 95.

Cavity Up or Cavity Down

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). This is called cavity-up, and has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins) and Ceramic Quad Flat Packs are assembled "Cavity Down", with the die attached to the inside top of the package, for optimal heat transfer to the ambient air.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP) packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

Clockwise or Counterclockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100- and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow to the surrounding air is impaired if the logo is mounted down.

Thermal Management

Modern high speed logic devices consume an appreciable amount of electrical energy. This energy invariably turns into heat. Higher device integration drives technologies to produce smaller device geometry and interconnections. With smaller chip sizes and higher circuit densities, heat generation on a fast switching CMOS circuit can be very significant. The heat removal needs for these modern devices must be addressed.

Managing heat generation in a modern CMOS logic device is an industry-wide pursuit. However, unlike the power needs of a typical Application Specific Integrated Circuit (ASIC) gate array, the power requirements for FPGAs are not determined as the device leaves the factory. Designs vary in power needs.

There is no way of anticipating the power needs of an FPGA device short of depending on compiled data from previous designs. For each device type, primary packages are chosen to handle 'typical' designs and gate utilization requirements. For the most part the choice of a package as the primary heat removal casing works well.

Occasionally designers exercise an FPGA device, particularly the high gate count variety, beyond "typical" designs. The use of the primary package without enhancement may not adequately address the device's heat removal needs. Heat removal management through external means or an alternative enhanced package should be considered.

Removing heat ensures the functional and maximum design temperature limits are maintained. The device may go outside the temperature limits if heat build up becomes excessive. As a consequence, the device may fail to meet electrical performance specifications. It is also necessary to satisfy reliability objectives by operating at a lower temperature. Failure mechanisms and the failure rate of devices depend on device operating temperature. Control of the package and the device temperature ensures product reliability.

Package Thermal Characterization Methods & Conditions

Method and Calibration

Xilinx uses the indirect electrical method for package thermal resistance characterization. The forward-voltage drop of an isolated diode residing on a special test die is calibrated at constant forcing current of 0.520mA with respect to temperature over a correlation temperature range of 22°C to 125°C (degree Celsius). The calibrated device is then mounted in an appropriate environment (still air, forced convection, circulating FC-40, etc.) Depending on the package, between 0.5 to 4 watts of power (Pd) is applied. Power (Pd) is applied to the device through diffused resistors on the same thermal die. The resulting rise in junction temperature is monitored with the forward-voltage drop of the precalibrated diode. Typically, three identical samples are tested at each data point. The reproducibility error in the set-up is within 6%.

Definition of Terms

T_J Junction Temperature — the maximum temperature on the die, expressed in °C (degree Celsius)

T_A Ambient Temperature — expressed in °C.

T_C The temperature of the package body taken at a defined location on the body. This is taken at the primary heat flow path on the package and represents the hottest part on the package — expressed in °C.

T_I The isothermal fluid temperature when junction to case temperature is taken — expressed in °C.

P_d The total device power dissipation — expressed in watts.

Junction-to-Reference General Setup

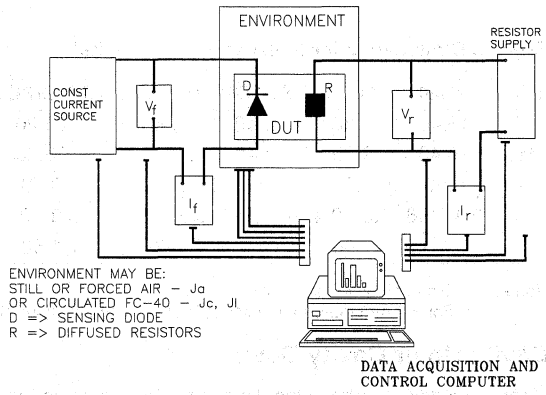


Figure 1: Thermal Measurement Set-Up (Schematic for Junction to Reference)

Junction-to-Case Measurement — Θ_{JC}

Θ_{JC} is measured in a 3M Flourinert (FC-40) isothermal circulating fluid stabilized at 25°C. The Device Under Test (DUT) is completely immersed in the fluid and initial stable conditions are recorded. **Pd** is then applied. Case temperature **(T_C)** is measured at the primary heat-flow path of the particular package. Junction temperature **(T_J)** is calculated from the diode forward-voltage drop from the initial stable condition before power was applied.

$$\Theta_{JC} = (T_J - T_C)/Pd$$

The junction-to-isothermal-fluid measurement **(Θ_{JI})** is also calculated from the same data.

$$\Theta_{JL} = (T_J - T_I)/Pd$$

The latter data is considered as the ideal Θ_{JA} data for the package that can be obtained with the most efficient heat removal scheme. Other schemes such as airflow, heatsinks, use of copper clad board, or some combination of all these will tend towards this ideal figure. Since this is not a widely used parameter in the industry, and it is not very realistic for normal application of Xilinx packages, the Θ_{JI} data is not published. The thermal lab keeps such data for package comparisons.

Junction-to-Ambient Measurement — Θ_{JA}

Θ_{JA} is measured on FR4 based PC boards measuring 4.5" x 6.0" x .0625" (114.3mm x 152.4mm x 1.6mm) with edge connectors. There are two main board types.

Type I, 2L/0P board, is single layer with 2 signal planes (one on each surface) and no internal Power/GND planes. The trace density on this board is less than 10% per side. Type II, the 4L/2P board, has 2 internal copper planes (one power, one ground) and 2 signal trace layers on both surfaces.

Data may be taken with the package mounted in a socket or with the package mounted directly on the board. Socket measurements typically use the 2L/0P boards. SMT devices may use either board. Published data always reflects the board and mount conditions used.

Data is taken at the prevailing temperature and pressure conditions (22°C to 25°C ambient). The board with the DUT is mounted in a cylindrical enclosure. The power application and signal monitoring are the same as Θ_{JC} measurements. The enclosure (ambient) thermocouple is substituted for the fluid thermocouple and two extra thermocouples brought in to monitor room and board temperatures. The junction to ambient thermal resistance is calculated as follows:

$$\Theta_{JA} = (T_J - T_A)/Pd$$

The setup described herein lends itself to the application of various airflow velocities from 0 - 800 Linear Feet per Minute (LFM), i.e., 0 - 4.06 m/s. Since the board selection (copper trace density, absence or presence of ground planes, etc.) affects the results of the thermal resistance, the data from these tests shall always be qualified with the board mounting information.

Data Acquisition and Package Thermal Database

Xilinx gathers data for a package type in die sizes, power levels and cooling modes (air flow and sometimes heatsink effects) with a Data Acquisition and Control system (DAS). The DAS controls the power supplies and other ancillary equipment for hands-free data taking. Different setups within the DAS software are used to run calibration, Θ_{JA}, Θ_{JC}, fan tests, as well as the power effect characteristics of a package.

A package is characterized with respect to the major variables that influence the thermal resistance. The results are stored in a database. Thermal resistance data is interpolated as typical values for the individual Xilinx devices that are assembled in the characterized package. Table 1 shows the typical values for different packages. Specific device data may not be the same as the typical data. However, the data will fall within the given minimum and maximum ranges. The more widely used packages will have a wider range. Customers may contact the Xilinx application group for specific device data.

Table 2: Summary of Thermal Resistance for Packages

PKG-CODE	Θ_{JA} at 0[7] (Max)	Θ_{JA} at 0[7] (Typ)	Θ_{JA} at 0[7] (Min)	Θ_{JA} at 250[6] (Typ)	Θ_{JA} at 500[6] (Typ)	Θ_{JA} at 750[6] (Typ)	Θ_{JC} (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
BG225	37	30	24	19	17	16	3.3	Various
CB100	44	41	38	25	19	17	5.1	Socketed
CB164	29	26	25	17	12	11	3.6	Socketed
CB196	25	24	24	15	11	10	1.8	Socketed
CB228	19	18	17	11	8	7	1.3	Socketed
CQ100	46	45	44	37	30	25	7.1	Socketed
DD8	114	109	97	90	73	60	8.2	Socketed
HQ208	15	14	14	10	8	7	1.7	4L/2P-SMT
HQ240	13	12	12	9	7	6	1.5	4L/2P-SMT
HQ304	11	11	10	7	5	5	0.9	4L/2P-SMT
MQ208	18	18	17	14	13	12	1.2	2L/0P-SMT
MQ240	17	17	16	12	11	10	1.2	2L/0P-SMT
PC20	86	84	76	63	56	53	25.8	2L/0P-SMT
PC44	51	46	42	35	31	29	13.7	2L/0P-SMT
PC68	46	42	38	31	28	26	9.3	2L/0P-SMT
PC84	41	33	28	25	21	17	5.3	2L/0P-SMT
PD48	43	43	43	33	29	27	11.6	Socketed
PD8	82	79	73	60	54	50	22.2	Socketed
PG120	32	27	25	19	15	13	3.6	Socketed
PG132	32	28	24	20	17	15	2.8	Socketed
PG144	26	25	23	17	14	13	3.7	Socketed
PG156	25	23	21	15	11	10	2.6	Socketed
PG175	25	23	20	14	11	10	2.6	Socketed
PG191	24	21	18	15	12	11	1.5	Socketed
PG223	24	20	18	15	12	11	1.5	Socketed
PG299	18	17	16	10	9	8	1.9	Socketed
PG411	16	15	14	9	8	7	1.2	Estimated
PG68	39	37	34	26	20	17	7.8	Socketed
PG84	37	34	31	24	18	16	5.8	Socketed
PP132	35	34	33	23	18	17	6.0	Socketed
PP175	29	29	28	19	15	13	2.5	Socketed
PQ100	35	33	32	29	28	27	5.5	4L/2P-SMT
PQ160	37	32	22	24	21	20	4.6	2L/0P-SMT
PQ208	35	32	26	23	21	19	4.3	2L/0P-SMT
PQ240	28	23	19	17	15	14	2.8	2L/0P-SMT
PQ44	52	51	51	40	36	35	12.4	4L/2P-SMT
SO8	147	147	147	112	105	98	48.3	IEEE-(Ref)
TQ100	37	31	31	26	24	23	7.5	4L/2P-SMT
TQ144	35	32	30	25	21	20	5.3	4L/2P-SMT
TQ176	29	28	27	21	18	17	5.3	4L/2P-SMT
VO8	162	162	162	123	116	108	48.3	Estimated
VQ100	47	38	32	32	30	29	9.0	4L/2P-SMT
VQ44	44	44	44	36	34	33	8.2	4L/2P-SMT
VQ64	44	41	39	34	32	31	8.2	4L/2P-SMT

Table 2: Summary of Thermal Resistance for Packages (Continued)

PKG-CODE	Θ_{JA} at 0[7] (Max)	Θ_{JA} at 0[7] (Typ)	Θ_{JA} at 0[7] (Min)	Θ_{JA} at 250[6] (Typ)	Θ_{JA} at 500[6] (Typ)	Θ_{JA} at 750[6] (Typ)	Θ_{JC} (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
WB144	28	28	28	—	—	—	6.0	2L/0P-SMT
WB225	28	28	28	—	—	—	6.0	2L/0P-SMT
WC44	47	46	45	38	31	25	9.1	Socketed
WC68	46	43	40	31	26	23	7.0	Socketed
WC84	43	41	38	29	24	21	3.9	Socketed

Notes:
1. Maximum, typical and minimum numbers are based on numbers for all the devices in the specific package at the time of compilation. The numbers do not necessarily reflect the absolute limits of that packages. Specific device data should lie within the limits. Packages used for a broader spectrum of devices have a wider range in the table. Specific device data in a package may be obtained from the factory.
2. Package configurations and drawings are in the package section of the data book.
3. 2L/0P - SMT: the data is from a surface mount type I board -- no internal planes on the board.
4. 4L/2P - SMT: the data is from a 4 layer SMT board incorporating 2 internal planes. Socketed data is taken in socket.
5. Thermal data is in degree Celsius/watt.
6. Airflow is reported in Linear Feet per minute (LFM).
7. Columns 1, 2 and 3 are for Θ_{JA} in still air.

Application of Thermal Resistance Data

Thermal resistance data gauges the IC package thermal performance. Θ_{JC} measures the internal package resistance to heat conduction from the die surface, through the die mount material to the package exterior. Θ_{JC} strongly depends on the package's heat conductivity, architecture and geometrical considerations.

Θ_{JA} measures the total package thermal resistance including Θ_{JC}. Θ_{JA} depends on the package material properties and such external conditions as convective efficiency and board mount conditions. For example, a package mounted on a socket may have a Θ_{JA} value 20% higher than the same package mounted on a 4 layer board with power and ground planes.

By specifying a few constraints, devices are ensured to operate within the intended temperature range. This also ensures device reliability and functionality. The system ambient temperature needs to be specified. A maximum T_J also needs to be established for the system. The following inequality will hold.

$$\mathbf{T_J(max) > \Theta_{JA}^{*} Pd + T_A}$$

The following two examples illustrates the use of this inequality.

Example 1:

The manufacturer's goal is T_J (max) < 100°C

A module is designed for a T_A = 45°C max.

A XC3042 in a PLCC 84 has a Θ_{JA} = 32°C/watt.

Given a XC3042 with a logic design with a rated power Pd of 0.75watt.

With this information, the maximum die temperature can be calculated as:

T_J = 45 + (32 x .75) ==> 69°C.

The system manufacturer's goal of T_J < 100°C is met.

Example 2:

A module has a T_A = 55°C max.

The Xilinx XC4013E is in a PQ240 package (HQ240 is also considered).

A XC4013E, in an example logic design, has a rated power of 2.50 watts. The module manufacturers goal is T_J(max.) < 100°C.

Table 3 shows the package and thermal enhancement combinations required to meet the goal of T_J < 100°C.

Table 3: Thermal Resistance for XC4013E in PQ240 and HQ240 Packages

Dev Name	Package	Θ_{JA} still air	Θ_{JA} (250 LFM)	Θ_{JA} (500 LFM)	Θ_{JA} (750 LFM)	Θ_{JC}	Comments
XC4013E	PQ240	23.7	17.5	15.4	14.3	2.7	Cu, SMT 2L/0P
XC4013E	HQ240	12.5	8.6	6.9	6.2	1.5	4 Layer Board data

Possible Solutions to meet the module requirements of 100°C:

1a. Using the standard PQ240; $T_J = 55 + (23.7 \times 2.50) ==> 114.25$ °C.

1b. Using standard PQ240 with 250LFM forced air $T_J = 55 + (17.5 \times 2.50) ==> 98.75$ °C

2a. Using standard HQ240 $T_J = 55 + (12.5 \times 2.50) ==> 86.25$ °C

2b. Using HQ240 with 250 LFM forced air $T_J = 55 + (8.6 \times 2.50) ==> 76.5$ °C

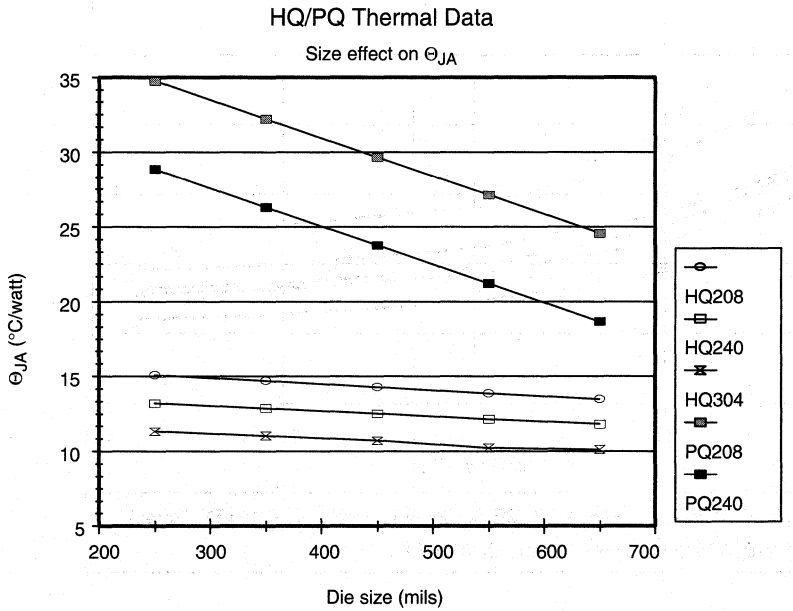
For all solutions, the junction temperature is calculated as:

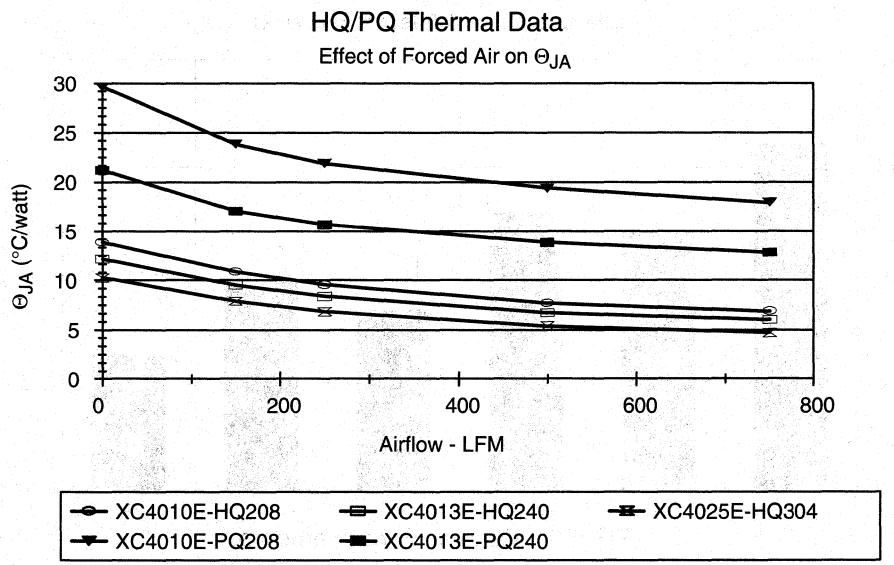
$$T_J = \text{Power} \times \Theta_{JA} + T_A$$

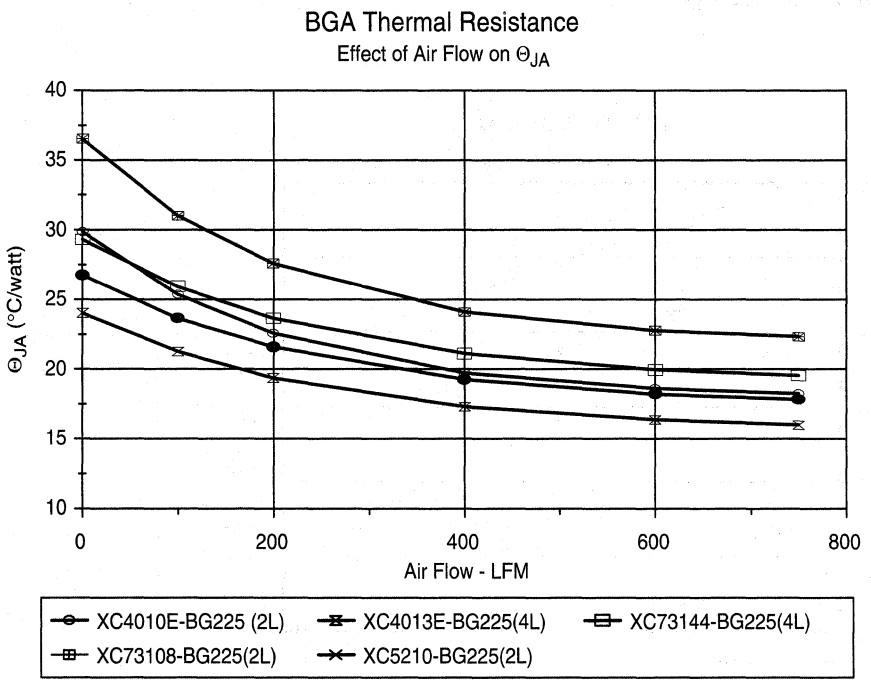
All solutions meet the module requirement of less than 100°C, with the exception of the PQ240 package in still air.

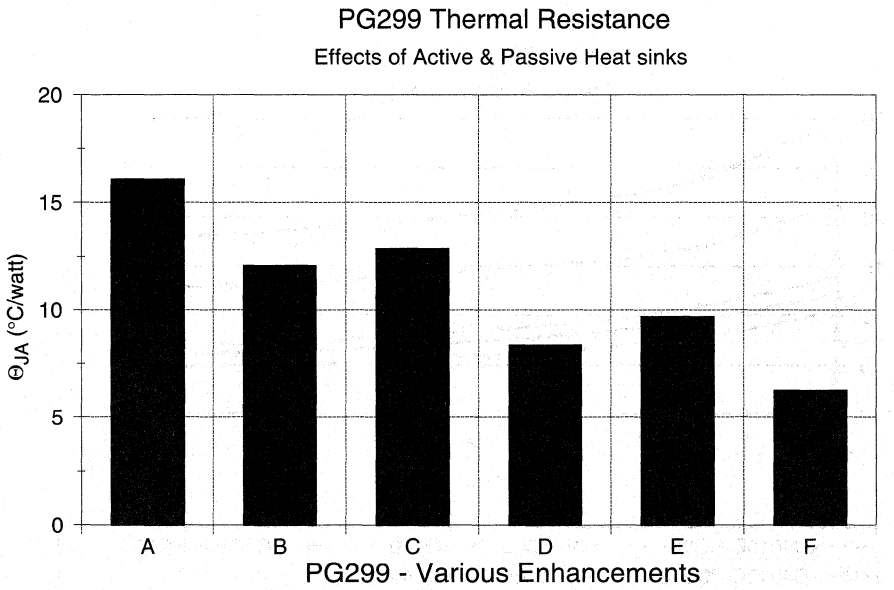
In general, depending on ambient and board temperatures conditions, and most importantly the total power dissipation, thermal enhancements -- such as forced air cooling, heat sinking, etc. may be necessary to meet the T_J(max) conditions set.

PQ/HQ Thermal Data Comparison

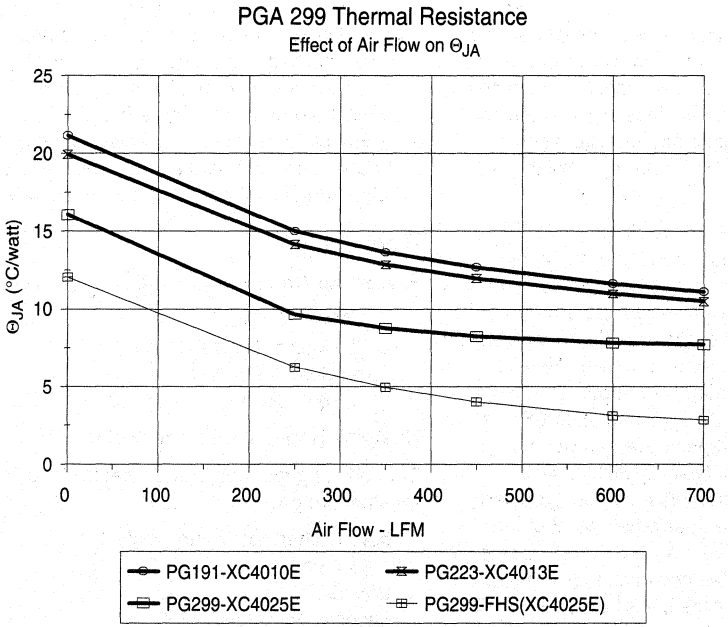








A Standard Pkg
B Pkg+Finned HS (Passive)
C Pkg+Active Fan (V=0)
D Pkg+Active Fan (V=12)
E Std Pkg +250LFM
F Pkg+Finned HS+ 250LFM


PGA 299 Thermal Resistance
Effect of Air Flow on ΘJA
25
20
15
10
5
0
ΘJA (°C/watt)
0
100
200
300
400
500
600
700
Air Flow - LFM
PG191-XC4010E
PG223-XC4013E
PG299-XC4025E
PG299-FHS(XC4025E)

Some Power Management Options

FPGA devices are usually not the dominating power consumers in a system, and do not have a big impact on power supply designs. There are obvious exceptions. When the actual or estimated power dissipation appears to be more than the specification of the chosen package, some options can be considered. Details on the engineering designs and analysis of some of these suggested considerations may be obtained from the references listed at the end of the section. The options include:

- A Xilinx low power (L) version of the circuit in the same package. With the product and speed grade of choice, up to a 40% power reduction can be anticipated. For more information, contact the Xilinx Hotline group.
- Explore thermally enhanced package options available for the same device. As illustrated above, the HQ240 package has a thermal impedance of about 50% of the equivalent PQ240. Besides, the 240 lead, the 208 lead and the 304 lead Quad packages have equivalent heatsink enhanced versions. Typically 25% to 40% improvement in thermal performance can be expected from these heatsink enhanced packages. Most of the high gate count devices above the XC4013 level come either exclusively in heat enhanced packages or have these packages as options. If the use of a standard PQ appears to be a handicap in this respect, a move to the equivalent HQ package if available may resolve the issue. The heat enhanced packages are pin to pin compatible and they use the same board layout.
- The use of forced air is an effective way to improve thermal performance. As seen on the graphs and the calculations above, forced air (200 -- 300 LFM) can reduce junction to ambient thermal resistance by 30%.
- If space will allow, the use of finned external heatsinks can be effective. If implemented with forced air as well, the benefit can be a 40% to 50% reduction. The HQ304, all cavity down PGAs, and the BG352 with exposed heatsink lend themselves to the application of external heatsinks for further heat removal efficiency.
- Outside the package itself, the board on which the package sits can have a significant impact. Board designs may be implemented to take advantage of this. Heat flows to the outside of a board mounted package and is sunk into the board to radiate. The effect of the board will be dependent on the size and how it conducts heat. Board size, the level of copper traces on it, the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package. Some of the heatsink packages with the exposed heatsink on the board side can be glued to the board with thermal compound to enhance heat removal.

References

Forced Air Cooling Application Engineering

COMAIR ROTRON
2675 Custom House Court
San Ysidro, CA 92173
1-619-661-6688

Heatsink Application Engineering

The following facilities provide heatsink solutions for industry standard packages.

AAVID Thermal Technologies
1 Kool Path
Box 400
Laconia, NH 03247-0400
1-603-528-3400

Thermalloy, Inc.
2021 W. Valley View Lane
Box 810839
Dallas, TX 75381-0839
1-214-243-4321

Wakefield Engineering, Inc.
60 Audubon Road
Wakefield MA 01880-1255
1-617-245-5900

Xilinx does not endorse these vendors nor their products. They are listed here for reference only. Any materials or services received from the vendors should be evaluated for compatibility with Xilinx components.

Component Mass (Weight) by Package Type

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
BG225	MOLDED BGA 27mm- ANAM	MO-151-CAL	OBG0001	2.2
BG352	SUPERBGA - 35X35MM AMKOR	MO-151-BAR	OBG0008	7.1
BG432	SUPERBGA - 40X40MM AMKOR	MO-151-BAU	OBG0009	9.1
CB100	NCTB TOP BRAZE 3K VER	MO-113	OCQ0008	10.8
CB100	NCTB TOP BRAZE 4K VER	MO-113	OCQ0006	10.8
CB164	NCTB TOP BRAZE 3K VER	MO-113-AA	OCQ0003	11.5
CB164	NCTB TOP BRAZE 4K VER	MO-113-AA	OCQ0007	11.5
CB196	NCTB TOP BRAZE 4K VER	MO-113-AB	OCQ0005	15.3
CB228	NCTB TOP BRAZE 4K VER	MO-113	OCQ0012	17.6
CC20	CERAMIC LEADED CHIP CARRIER	N/A	OCQ0011	8.4
DD8	.300 CERDIP PACKAGE	MO-036-AA	OPD0005	1.1
HQ208	METRIC 28 X 28 - H/S DIE UP	MO-143-FA1	OPQ0020	10.8
HQ240	METRIC QFP 32 32 - H/S DIE UP	MO-143-GA	OPQ0019	15.0
HQ304	METRIC QFP 40 40-H/S DIE DOWN	MO-143-JA	OPQ0014	26.2
MQ208	METAL QUAD EIAJ	N/A	OPQ0006	6.1
MQ240	METAL QUAD	N/A	OPQ0011	8.0
PC20	PLCC JEDEC MO-047	MO-047-AA	OPC0006	0.8
PC28	PLCC JEDEC MO-047	MO-047-AB	OPC0001	1.1
PC44	PLCC JEDEC MO-047	MO-047-AC	OPC0005	1.2
PC68	PLCC JEDEC MO-047	MO-047-AE	OPC0001	4.8
PC84	PLCC JEDEC MO-047	MO-047-AF	OPC0001	6.8
PD48	DIP .600	N/A	OPD0001	7.9
PD8	DIP .300 STANDARD	MO-001-AA	OPD0002	0.5
PG120	CERAMIC PGA 13 X 13 MATRIX	MO-067-AE	OPG0012	11.5
PG132	CERAMIC PGA 14 X 14 MATRIX	MO-067-AF	OPG0004	11.8
PG144	CERAMIC PGA 15 X15 CAVITY UP	MO-067-AG	OPG0017	16.9
PG156	CERAMIC PGA 16 X 16 MATRIX	MO-067-AH	OPG0007	17.1
PG175	CERAMIC PGA 16X16 STD VER.	MO-067-AH	OPG0009	17.7
PG184	CERAMIC PGA 15 X15 CAVITY UP	MO-067-AG	OPG0019	17.5
PG191	CERAMIC PGA 18 X 18 STD - ALL	MO-067-AK	OPG0008	21.8
PG223	CERAMIC PGA 18 X 18 TYPE	MO-067-AK	OPG0016	26.0
PG299	CERAMIC PGA 20 X 20 HEATSINK	MO-067-AK	OPG0022	37.5
PG299	CERAMIC PGA 20 X 20 TYPE	MO-067-AM	OPG0015	29.8
PG411	CERAMIC PGA 39 X 39 STAGGER	MO-128-AM	OPG0019	36.7
PG68	CERAMIC PGA CAV UP 11X11	MO-067-AC	OPG0002	7.0
PG84	CERAMIC PGA CAV UP 11X11	MO-067-AC	OPG0003	7.2
PP132	PLASTIC PGA 14 X 14 MATRIX	MO-83-AF	OPG0001	8.1
PP175	PLASTIC PGA 16X16 BURRIED	MO-83-AH	OPG0006	11.1
PQ100	EIAJ 14X20 QFP - 1.60	MO-108-CC1	OPQ0013	1.6
PQ160	EIAJ 28X28 .65MM 1.60	MO-108-DD1	OPQ0002	5.8
PQ208	EIAJ 28X28 .5MM 1.30	MO-143-FAI	OPQ0003	5.3
PQ240	EIAJ 32 X 32 .5MM	MO-143-GA	OPQ0010	7.1
PQ44	EIAJ 10 X 10 X 2.0	MO-108-AA2	OPQ0015	0.5
SO8	VERSION 1 - .150/55MIL	MO-150	OPD0006	0.1
TQ100	THIN QFP 1.4mm thick	MS-026-BDE	OPQ0004	0.7

Component Mass (Weight) by Package Type (Continued)

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
TQ144	THIN QFP 1.4mm thick	MS-026-BFB	OPQ0007	1.4
TQ176	THIN QFP 1.4mm thick	MS-026-BGA	OPQ0008	0.9
VO8	THIN SOIC-II	N/A	OPD0007	0.1
VQ100	THIN QFP 1.0 thick	MS-026-AED	OPQ0012	0.6
VQ44	EIAJ 10 X 10 X 1.0	MS-026-ACB	OPQ0017	0.4
VQ64	THIN QFP 1.0 thick	MS-026-ACD	OPQ0009	0.5
WC44	JEDEC WINDOWED CQUAD	MO-087	OCQ0004	2.9
WC68	WINDOWED CERQUAD	MO-087	OCQ0009	7.3
WC84	WINDOWED CERQUAD	MO-087	OCQ0010	11.0

Notes: 1. Data represents average values for typical packages with typical devices. The accuracy is between 7% to 10%.
2. More precise numbers (below 5% accuracy) for specific devices may be obtained from Xilinx through a factory representative or by calling the Xilinx Hotline.

Xilinx Thermally Enhanced Packaging

The Package Offering

Xilinx Code	Body (mm)	THK (mm)	Mass (gm)	Heatsink Location	JEDEC No.	Xilinx No.
HQ304	40x40	3.80	26.2	TOP	MO-143-JA	OPQ0014
HQ240	32x32	3.40	15.0	DOWN	MO-143-GA	OPQ0019
HQ208	28x28	3.37	10.0	DOWN	MO-143-FA	OPQ0020

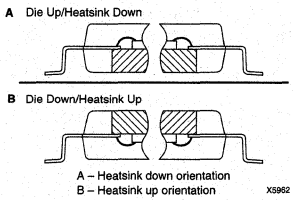
Overview

Xilinx offers thermally enhanced quad flat pack packages on certain devices. This section discusses the performance and usage of these packages (designated HQ). In summary:

- The HQ-series and the regular PQ packages conform to the same JEDEC drawings.
- The HQ and PQ packages use the same PCB land patterns.
- The HQ packages have more mass
- Thermal performance is better for the HQ packages

Where and When Offered

- HQ packages are offered as the thermally enhanced equivalents of PQ packages. They are used for high gate count or high I/O count devices in packages, where heat dissipation without the enhancement may be a handicap for device performance. Such devices include XC4013E, XC4020E, XC4025E, and XC5215.
- They are also being used in place of MQUAD (MQ) packages of the same lead count for new devices.
- The HQ series at the 240 pin count level or below are offered with the heatsink at the bottom of the package. This was done to ensure pin to pin compatibility with the existing PQ and MQ packages.
- At the 304 pin count level, the HQ is offered with the heatsink up. This arrangement offers a better potential for further thermal enhancement by the designer.



Mass Comparison

Because of the copper heatsink, the HQ series of packages are about twice as heavy as the equivalent PQ. Here is a quick comparison.

	PQ (gm)	MQ (gm)	HQ (gm)
208 Pin	5.3	6.1	10.0
240 Pin	7.1	8.0	15.0
304 Pin	N/A	N/A	26.2

Thermal Data for the HQ

The data for individual devices may be obtained from Xilinx.

Still Air Data Comparison			
	HQ Θ_{JA} (°C/Watt)	MQ Θ_{JA} (°C/watt)	PQ Θ_{JA} (°C/watt)
208 Pin	10-14	17-19	25-32
240 Pin	11-14	15-17	18-28
304 Pin	10-12	N/A	N/A

Note: Θ_{JC} is typically between 1 and 2 °C/Watt for HQ and MQ Packages. For PQ's, it is between 2 and 7 °C/Watt.

Data Comparison at Airflow - 250 LFM			
	HQ Θ_{JA} (°C/watt)	MQ Θ_{JA} (°C/watt)	PQ Θ_{JA} (°C/watt)
208 Pin	9-10	14-15	19-25
240 Pin	8-9	11-13	14-20
304 Pin	6.5-8	N/A	N/A

Other Information

- Leadframe: Copper EFTEC-64 or C7025
- Heat Slug: Copper - Nickel plated → Heatsink metal is Grounded
- Lead Finish 85/15 Sn/Pb 300 microinches minimum
- D/A material - Same as PQ; Epoxy 84-1LMISR4
- Mold Cpd. Same as PQ - EME7304LC
- Packed in the same JEDEC trays

Moisture Sensitivity of PSMCs

Moisture Induced Cracking During Solder Reflow

The surface mount reflow processing step subjects the Plastic Surface Mount Components (PSMC) to high thermal exposure and chemicals from solder fluxes and cleaning fluids during user's board mount assembly. The plastic mold compounds used for device encapsulation are, universally, hygroscopic and absorb moisture at a level determined by storage environment and other factors. Entrapped moisture can vaporize during rapid heating in the solder reflow process generating internal hydrostatic pressure. Additional stress is added due to thermal mismatch, and the Thermal Coefficient of Expansion (TCE) of plastic, metal lead frame, and silicon die. The resultant pressure may be sufficient to cause delamination within the package, or worse, an internal or external crack in the plastic package. Cracks in the plastic package can allow high moisture penetration, inducing transport of ionic contaminants to the die surface and increasing the potential for early device failure.

How the effects of moisture in plastic packages and the critical moisture content result in package damage or failure is a complex function of several variables. Among them are package construction details -- materials, design, geometry, die size, encapsulant thickness, encapsulant properties, TCE, and the amount of moisture absorbed. The PSMC moisture sensitivity has, in addition to package cracking, been identified as a contributor to delamination-related package failure artifacts. These package failure artifacts include bond lifting and breaking, wire neckdown, bond cratering, die passivation, and metal breakage.

Because of the importance of the PSMC moisture sensitivity, both device suppliers and device users have ownership and responsibility. The background for present conditions, moisture sensitivity standardized test and handling procedures have been published by two national organizations. Users and suppliers are urged to obtain copies of both documents (listed below) and use them rigorously. Xilinx adheres to both.

- JEDEC STANDARD JESD22-A112. Test Method A112 "Moisture-Induced Stress Sensitivity for Plastic Surface Mounted Devices".

  Available through Global Engineering Documents
  Phone: USA and Canada 800-854-7179, International 1-303-792-2181

- IPC Standard IPC-SM-786A "Procedures for Characterizing and Handling of Moisture/Reflow Sensitive ICs".

  Available through IPC
  Phone: 1-708-677-2850

None of the previously stated or following recommendations apply to parts in a socketed application. For board mounted parts careful handling by the supplier and the user is vital. Each of the above publications has addressed the sensitivity issue and has established 6 levels of sensitivity (based on the variables identified). A replication of those listings, including the preconditioning and test requirements, and the factory floor life conditions for each level are outlined in Table 4. Xilinx devices are characterized to their proper level as listed. This information is conveyed to the user via special labeling on the Moisture Barrier Bag (MBB).

In Table 4, the level number is entered on the MBB prior to shipment. This establishes the user's factory floor life conditions as listed in the time column. The soak requirement is the test limit used by Xilinx to determine the level number. This time includes manufacturer's exposure time or the time it will take for Xilinx to bag the product after baking.

Table 4: Package Moisture Sensitivity Levels per JEDEC A112

Level	Factory Floor Life		Soak Requirements (Preconditioning)			
	Conditions	Time	Time			Conditions
1	≤30°C / 90% RH	Unlimited	168 hours			85°C / 85% RH
2	≤30°C / 60% RH	1 year	168 hours			85°C / 60% RH
			Time (hours)			
			X +	Y =	Z	
3	≤30°C / 60% RH	168 hours	24	168	192	≤30°C / 60% RH
4	≤30°C / 60% RH	72 hours	12	72	84	≤30°C / 60% RH
5	≤30°C / 60% RH	24 hours	6	24	30	≤30°C / 60% RH
6	≤30°C / 60% RH	6 hours	0	6	6	≤30°C / 60% RH

Notes: X = Default value of semiconductor manufacturer's time between bake and bag. If the semiconductor manufacturer's actual time between bake and bag is different from the default value, use the actual time.
Y = Floor life of package after it is removed from dry pack bag.
Z = Total soak time for evaluation.

Factory Floor Life

Factory floor life conditions for Xilinx devices are clearly stated on MBB containing moisture sensitive PSMCs. These conditions have been ascertained by following Test Methods outlined in JEDEC JESD22-A112 and are replicated in Table 4. If factory floor conditions are outside the stated environmental conditions (85°C/85% RH for level 1, and 30°C/60% RH for Levels 2-6) or if time limits have been exceeded, then recovery can be achieved by baking the devices before the reflow step. Identified in the next section are two acceptable bake schedules. Either can be used for recovery to the required factory floor level.

Dry Bake Recommendation and Dry Bag Policy

Xilinx recommends, as do the mentioned publications and other industry studies, that all moisture sensitive PSMCs be baked prior to use in surface mount applications, or comply strictly with requirements as specified on the MBB. Tape and Reeled parts are universally dry packed. Level 1 parts are shipped without the need for, or use of, an MBB.

Two bake schedules have been identified as acceptable and equivalent. The first is 24 hours in air at 125°C., in shipping media capable of handling that temperature. The second bake schedule is for 192 hours in a controlled atmosphere of 40°C, equal to or less than 5% RH.

Dry Devices are sealed in special military specification Moisture Barrier Bags (MBB). Enough desiccant pouches are enclosed in the MBB to maintain contents at less than 20% RH for up to 12 months from the date of seal. A reversible Humidity Indicator Card (HIC) is enclosed to monitor the internal humidity level. The loaded bag is then sealed shut under a partial vacuum with an impulse heat sealer.

Artwork on the bags provides storage, handling and use information. There are areas to mark the seal date, quantity, and moisture sensitivity level and other information. The following paragraphs contain additional information on handling PSMCs.

Handling Parts in Sealed Bags

Inspection

Note the seal date and all other printed or hand entered notations. Review the content information against what was ordered. Thoroughly inspect for holes, tears, or punctures that may expose contents. Xilinx strongly recommends that the MBB remain closed until it reaches the actual work station where the parts will be removed from the factory shipping form.

Storage

The sealed MBB should be stored, unopened, in an environment of not more than 90% RH and 40°C. The enclosed HIC is the only verification to show if the parts have been exposed to moisture. Nothing in part appearance can verify moisture levels.

Expiration Date

The seal date is indicated on the MBB. The expiration date is 12 months from the seal date. If the expiration date has been exceeded or HIC shows exposure beyond 20% upon opening the bag bake the devices per the earlier stated bake schedules. The three following options apply after baking:

Use the devices within time limits stated on the MBB.

Reseal the parts completely under a partial vacuum with an impulse sealer (hot bar sealer) in an approved MBB within 12 hours, using fresh desiccant and HIC, and label accordingly. Partial closures using staples, plastic tape, or cloth tape are unacceptable.

Store the out-of-bag devices in a controlled atmosphere at less than 20% RH. A desiccator cabinet with controlled dry air or dry nitrogen is ideal.

Other Conditions

Open the MBB when parts are to be used. Open the bag by cutting across the top as close to the seal as possible. This provides room for possible resealing and adhering to the reseal conditions outlined above. After opening, strictly adhere to factory floor life conditions to ensure that devices are maintained below critical moisture levels.

Bags opened for less than one hour (strongly dependent on environment) may be resealed with the original desiccant. If the bag is not resealed immediately, new desiccant or the old one that has been dried out may be used to reseal, **if the factory floor life has not been exceeded**. Note that factory floor life is cumulative. Any period of time when MBB is opened must be added to all other opened periods.

Both the desiccant pouches and the HIC are reversible. Restoration to dry condition is accomplished by baking at 125°C for 10-16 hours, depending on oven loading conditions.

Tape and Reel

Xilinx offers a tape & reel packing for PLCC, BGA, QFP, and SO packages. The packing material is made of black conductive Polystyrene and protects the packages from mechanical and electrical damage. The reel material provides a suitable medium for pick and place equipment.

The tape & reel packaging consists of a pocketed carrier tape, sealed with a protective cover. The device sits on pedestals (for PLCC, QFP packages) to protect the leads from mechanical damage. All devices loaded into the tape carriers are baked, lead scanned before the cover tape is attached and sealed to the carrier. In-line mark inspection for mark quality and package orientation is used to ensure shipping quality.

Benefits

- Increased quantity of devices per reel versus tubes improves cycle time and reduces the amount of time to index spent tubes.
- Tape & reel packaging enables automated pick and place board assembly.
- Reels are uniform in size enabling equipment flexibility.
- Transparent cover tape allows device verification and orientation.
- Anti-static reel materials provides ESD protection.
- Carrier design include a pedestal to protect package leads during shipment.
- Bar code labels on each reel facilitate automated inventory control and component traceability.
- All tape & reel shipments include desiccant pouches and humidity indicators to insure products are safe from moisture.
- Compliant to Electronic Industries Association (EIA) 481.

Material and Construction

Carrier Tape

- The pocketed carrier Tape is made of conductive polystyrene material, or equivalent, with a surface resistivity level of less than 106 ohms per square inch.
- Devices are loaded 'live bug' or leads down, into a device pocket.
- Each carrier pocket has a hole in the center for automated sensing of whether a unit is in the pocket or not.
- Sprocket holes along the edge of the carrier tape enable direct feeding into an automated board assembly equipment.

Cover Tape

- An anti-static, transparent, polyester cover tape, with heat activated adhesive coating, sealed to the carrier edges to hold the devices in the carrier pockets.
- Surface resistivity on both sides is less than 1011 ohms per square inch.

Reel

- The reel is made of anti-static Polystyrene material. The loaded carrier tape is wound onto this conductive plastic reel.
- A protective strip made of conductive Polystyrene material is placed on the outer part of the reel to protect the devices from external pressure in shipment.
- Surface resistivity is less than 1011 ohms per square inch.
- Device loading orientation is in compliance with EIA Standard 481.

Bar Code Label

- The bar code label on each reel provides customer identification, device part number, date code of the product and quantity in the reel.
- Print quality are in accordance with ANSI X3.182-1990 Bar Code Print Quality Guidelines. Presentation of Data on labels are EIA-556-A compliant.
- The label is an alphanumeric, medium density Code 39 labels.
- This machine-readable label enhances inventory management and data input accuracy.

Shipping Box

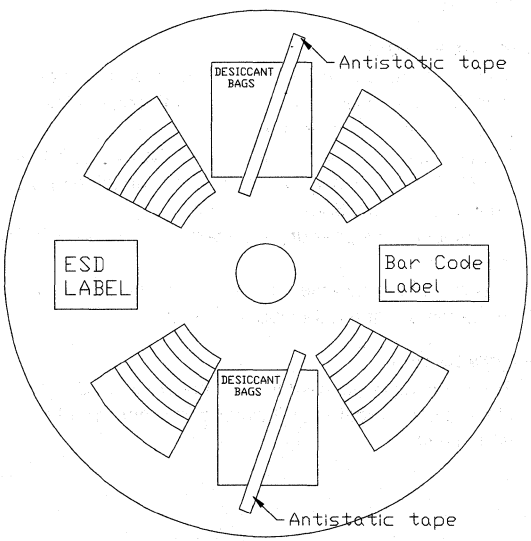
- The shipping container for the reels are in a 13" x 13" x 3" C-flute, corrugated, # 3 white 'pizza' box, rated to 200 lb test.

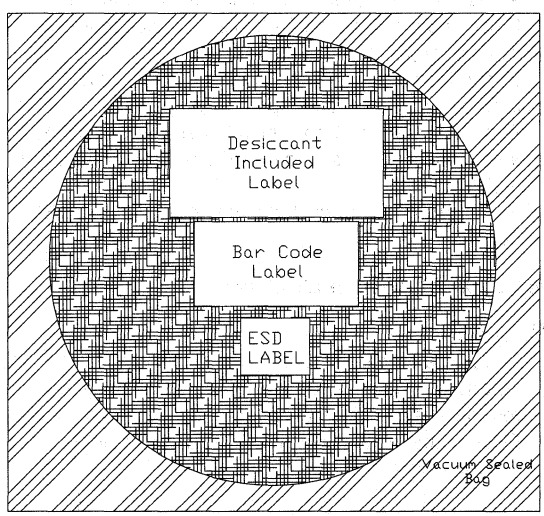
Table 5: Tape & Reel Packaging

Package Type	Pin Count	Carrier Width	Cover Width	Pitch	Reel Size	Qty per Reel
PLCC (Plastic Leaded Chip Carrier)	20	16 mm	13.3 mm	12 mm	7 inch	250
	20	16 mm	13.3 mm	12 mm	13 inch	750
	44	32 mm	25.5 mm	24 mm	13 inch	500
	68	44 mm	37.5 mm	32 mm	13 inch	250
	84	44 mm	37.5 mm	36 mm	13 inch	250
SO (Plastic Small Outline)	8	12 mm	9.2 mm	8 mm	7 inch	750
QFP (Plastic Quad Flat Pack)	100	44 mm	37.5 mm	32 mm	13 inch	250
	160	44 mm	37.5 mm	40 mm	13 inch	200
BGA (Plastic Ball Grid Array)	225	44 mm	37.5 mm	32 mm	13 inch	500

Notes:
1. A minimum of 230mm of empty pockets are provided at the beginning (leader) of each reel.
2. A minimum of 160mm of empty pockets are provided at the end (trailer) of each reel.
3. Tape Leader/Trailer requirements are in compliance to EIA Standards 481.
4. Peel Strength between 20 and 120 grams ensures consistency during de-reeling operations and is compliant to EIA Standard 481.
5. Each reel is subject to peel back strength tests.
6. For packages not listed above, please contact your Xilinx sales representative for updated information.

Standard Bar Code Label Locations





Reflow Soldering Process Guidelines

In order to implement and control the production of surface mount assemblies, the dynamics of the solder reflow process, and how each element of the process is related to the end result, must be thoroughly understood.

The primary phases of the reflow process are as follows:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

The sequence of five actions that occur during this process is shown in Figure 2.

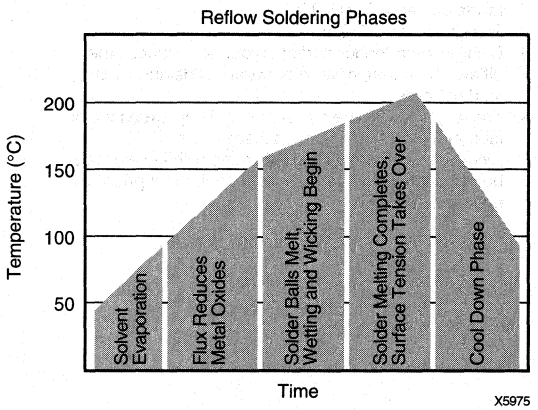


Figure 2:

Each phase of a surface mount reflow profile has min/max limits that should be viewed as a process window. The process requires a careful selection and control of the materials, geometries of the mating surfaces (package footprint vs. PCB land pattern geometries) and the time temperature of the profile. If all of the factors of the process are sufficiently optimized, there will be good solder wetting and fillet formation (between component leads and the land patterns on the substrate). If factors are not matched and optimized there can be potential problems as summarized in Figure 3.

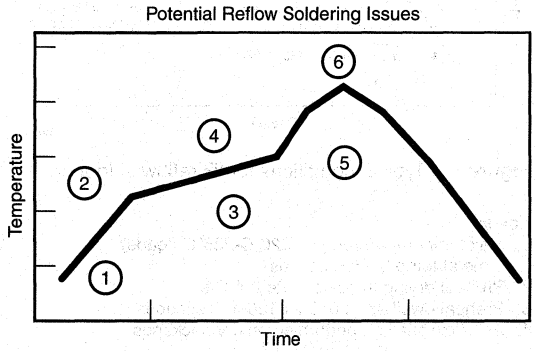


Figure 3:

Figure 4 and Figure 5 show typical conditions for solder reflow processing using Vapor Phase or IR Reflow. The moisture sensitivity of Plastic Surface Mount Components (PSMCs) must be verified prior to surface mount flow. See the preceding sections for a more complete discussion on PSMC moisture sensitivity.

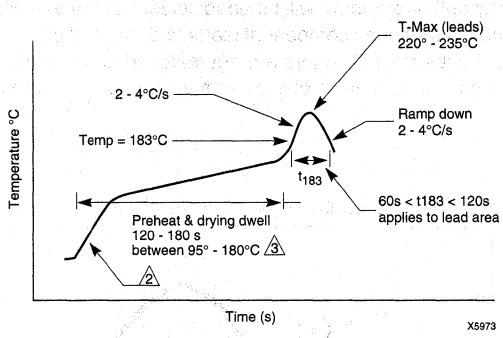


Figure 4: Typical conditions for IR reflow soldering

Notes:
1. Max temperature range = 220°C-235°C (leads) Time at temp 30-60 seconds
2. Preheat drying transition rate 2-4°C/s
3. Preheat dwell 95-180°C for 120-180 seconds
4. IR reflow shall be performed on dry packages

The IR process is strongly dependent on equipment and loading differences. Components may overheat due to lack of thermal constraints. Unbalanced loading may lead to significant temperature variation on the board. This guideline is intended to assist users in avoiding damage to the components; the actual profile should be determined by the users using these guidelines.

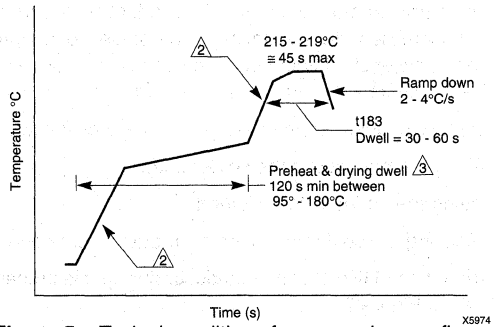


Figure 5: Typical conditions for vapor phase reflow soldering

Notes:
1. Solvent - FC5312 or equivalent - ensures temperature range of leads @ 215-219°C
2. Transition rate 4-5°C/s
3. Dwell is intended for partial dryout and reduces the difference in temperature between leads and PCB land patterns.
4. These guidelines are for reference. They are based on laboratory runs using dry packages. It is recommended that actual packages with known loads be checked with the commercial equipment prior to mass production.

Sockets

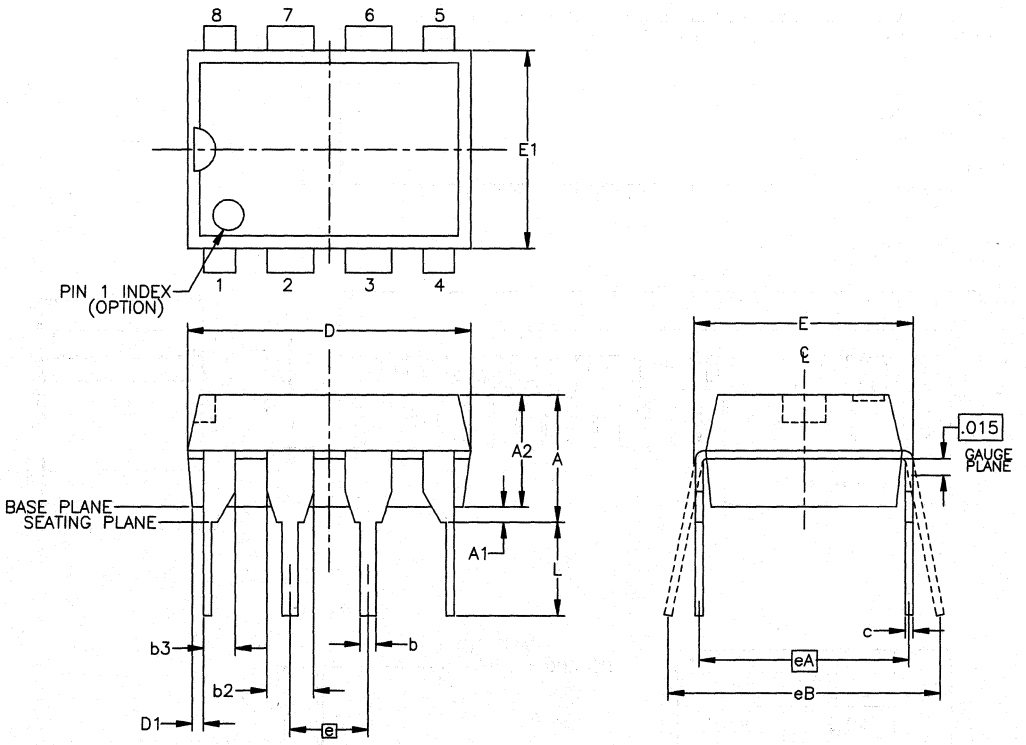
Table 6 lists manufacturers known to offer sockets for Xilinx Package types. This summary does not imply an endorsement by Xilinx. Each user has the responsibility to evaluate and approve a particular socket manufacturer.

Table 6: Socket Manufacturers

Manufacturer	Packages					
	DIP SO VO	PC WC	PQ HQ TQ VQ	PG PP	CB	BG CG
AMP Inc. 470 Friendship Road Harrisburg, PA 17105-3608 (800) 522-6752	X	X		X		
Augat Inc. 452 John Dietsch Blvd. P.O. Box 2510 Attleboro Falls, MA 02763-2510 (508) 699-7646	X	X		X		
McKenzie Socket Division 910 Page Avenue Fremont, CA 94538 (510) 651-2700	X	X		X		
3M Textool 6801 River Place Blvd. Austin, TX 78726-9000 (800) 328-0411 (612) 736-7167				X	X	X
Wells Electronics 1701 South Main Street South Bend, IN 46613-2299 (219) 287-5941				X		
Yamaichi Electronics Inc. 2235 Zanker Road San Jose, CA 95131 (408) 456-0797		X	X	X	X	

Physical Dimensions

Plastic DIP Packages — PD8, PD48

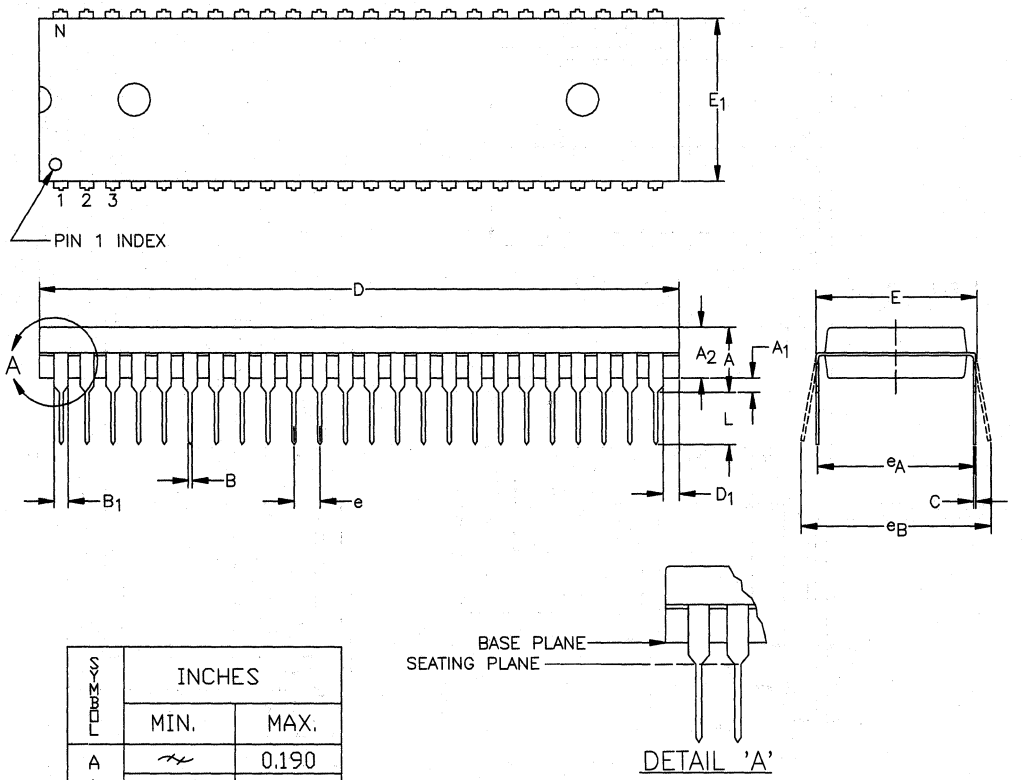


SYMBOL	INCHES		NOTE
	MIN.	MAX.	
A		0.181	
A_1	0.019		
A_2	0.122	0.161	
b	0.014	0.022	
b_2	0.045		
b_3		0.045	
c	0.009	0.012	
D	0.355	0.382	
D_1	0.005		
E	0.303	0.323	
E_1	0.240	0.272	
e	0.100 BSC		
e_A	0.300 BSC		
e_B		0.430	
L	0.115	0.150	
N	8		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .010" PER SIDE.
3. LEAD FINISH: (85±5%)Sn–Pb SOLDER PLATE
4. CONFORMS TO JEDEC MS–001–BA

8–PIN PLASTIC DIP (PD8)



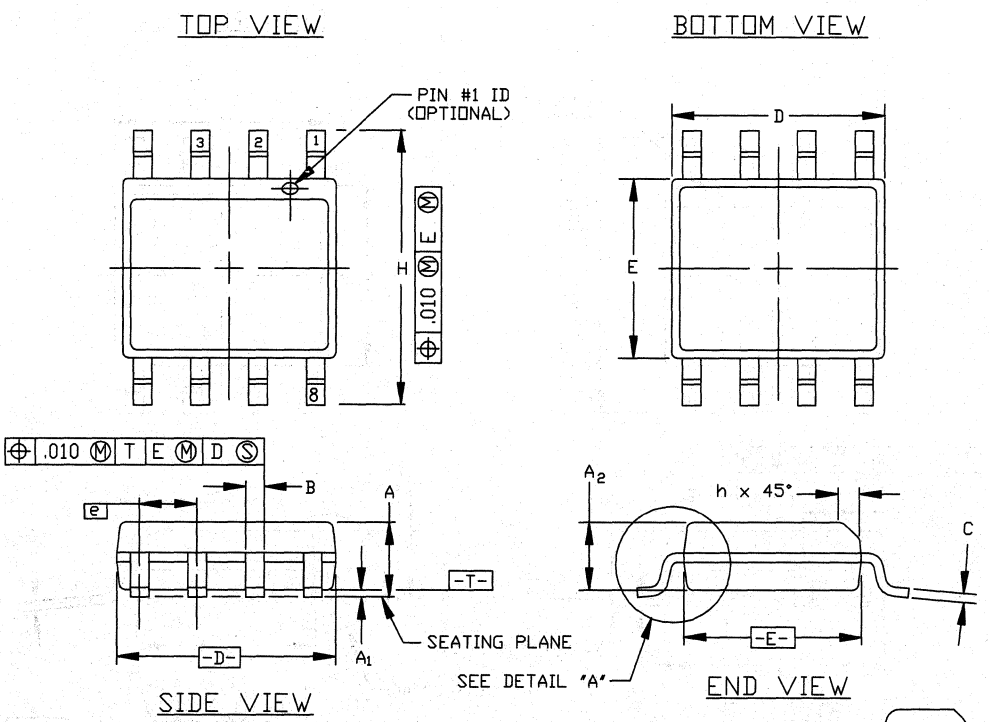
SYMBOL	INCHES	
	MIN.	MAX.
A	—	0.190
A_1	0.015	—
A_2	0.125	0.195
B	0.014	0.022
B_1	0.030	0.070
C	0.008	0.015
D	2.385	2.480
D_1	0.005	—
E	0.600	0.625
E_1	0.485	0.580
e	0.100 BSC	
e_A	0.600 BSC	
e_B	—	0.700
L	0.115	0.200
N	48	

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. "D" AND "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH or PROTRUSIONS SHALL NOT EXCEED .010".
3. LEAD FINISH: SOLDER PLATE
4. CONFORMS TO JEDEC MS–011–AD

48–PIN PLASTIC DIP (PD48)

SOIC Packages — SO8



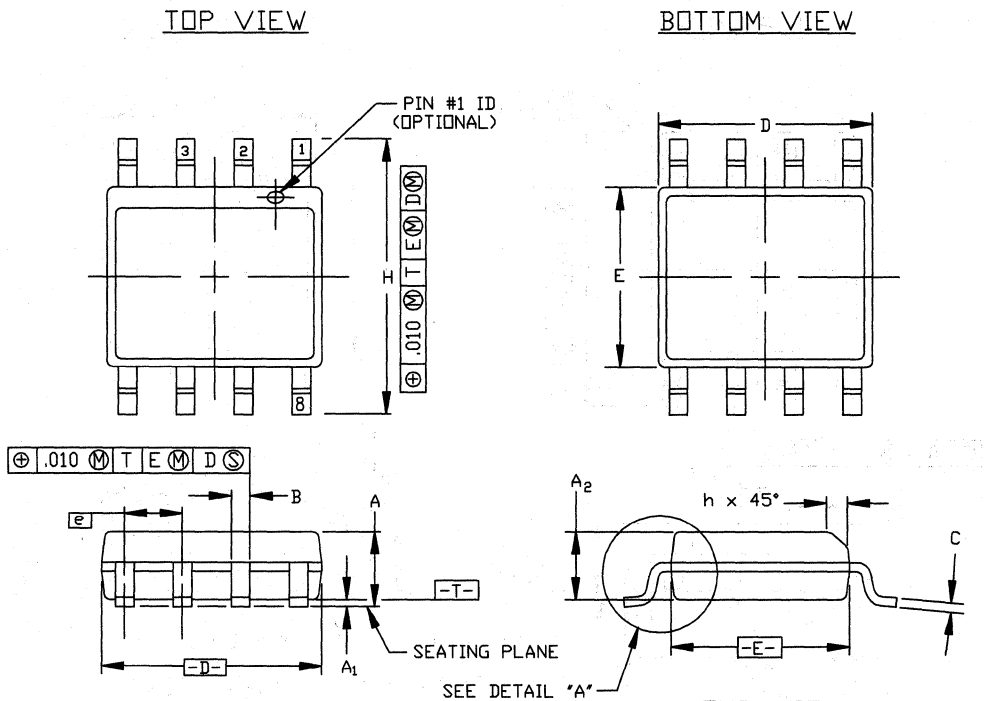
SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A	.059	.064	.068
A_1	.004	.006	.0098
A_2	.055	.058	.061
B	.013	.016	.020
C	.0075	.008	.0098
D	.189	.194	.196
E	.150	.155	.157
e		.050 BSC	
H	.229	.236	.244
h	.010	.013	.019
L	.016	.025	.035
α	0°	5°	8°

NOTES:

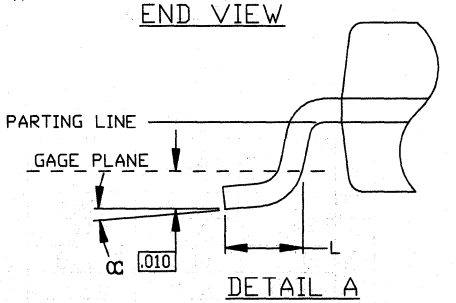
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .006" PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .010" PER SIDE.
4. LEAD FINISH: SOLDER PLATE
5. CONFORMS TO JEDEC MS–012

8 LEAD SOIC (SO8)

TSOP Packages — VO8



SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A			.047
A_1	.002	.004	.006
A_2	.037	.039	.044
B	.0138		.0192
C	.0075		.0089
D	.189	.194	.196
E	.150	.155	.157
e	.050 BSC		
H	.230	.236	.244
h	.010	.013	.019
L	.016	.025	.035
L_1	0.010 BSC		
α	0°		8°

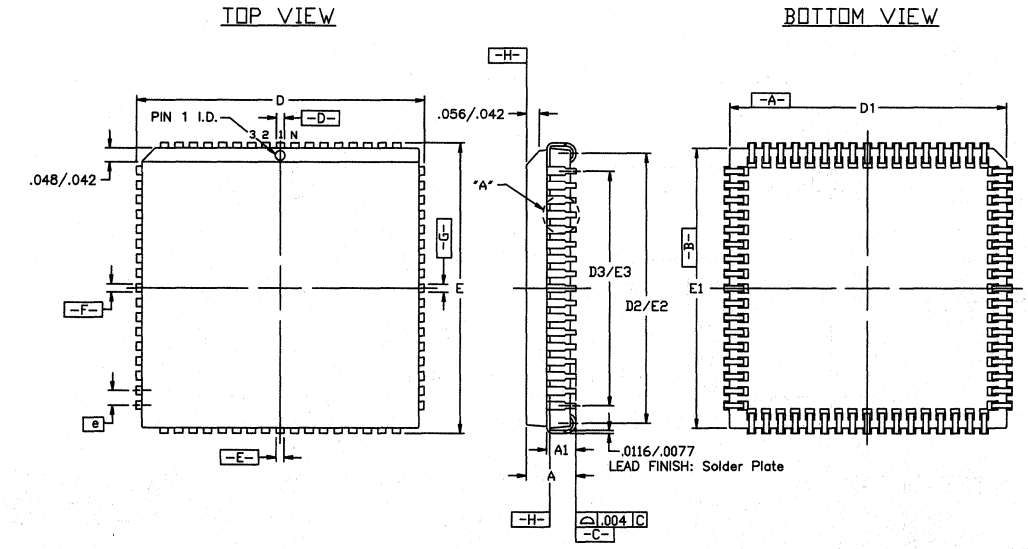


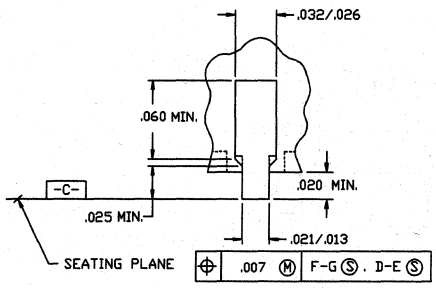
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. DIMENSION "D" DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .006" PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .010" PER SIDE.
4. LEAD FINISH: SOLDER PLATE

8 LEAD TSOP (VO8)

PLCC Packages — PC20, PC28, PC44, PC68, PC84





SYMBOL	INCHES									
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	.165	.180	.165	.180	.165	.180	.165	.200	.165	.200
A_1	.090	.120	.099	.110	.090	.120	.090	.130	.090	.130
D/E	.385	.395	.485	.495	.685	.695	.985	.995	1.185	1.195
D_1/E_1	.350	.356	.450	.456	.650	.656	.950	.958	1.150	1.158
D_2/E_2	.290	.330	.390	.430	.590	.630	.890	.930	1.090	1.130
D_3/E_3	.200 REF.		.300 REF.		.500 REF.		.800 REF.		1.000 REF.	
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
N	20		28		44		68		84	

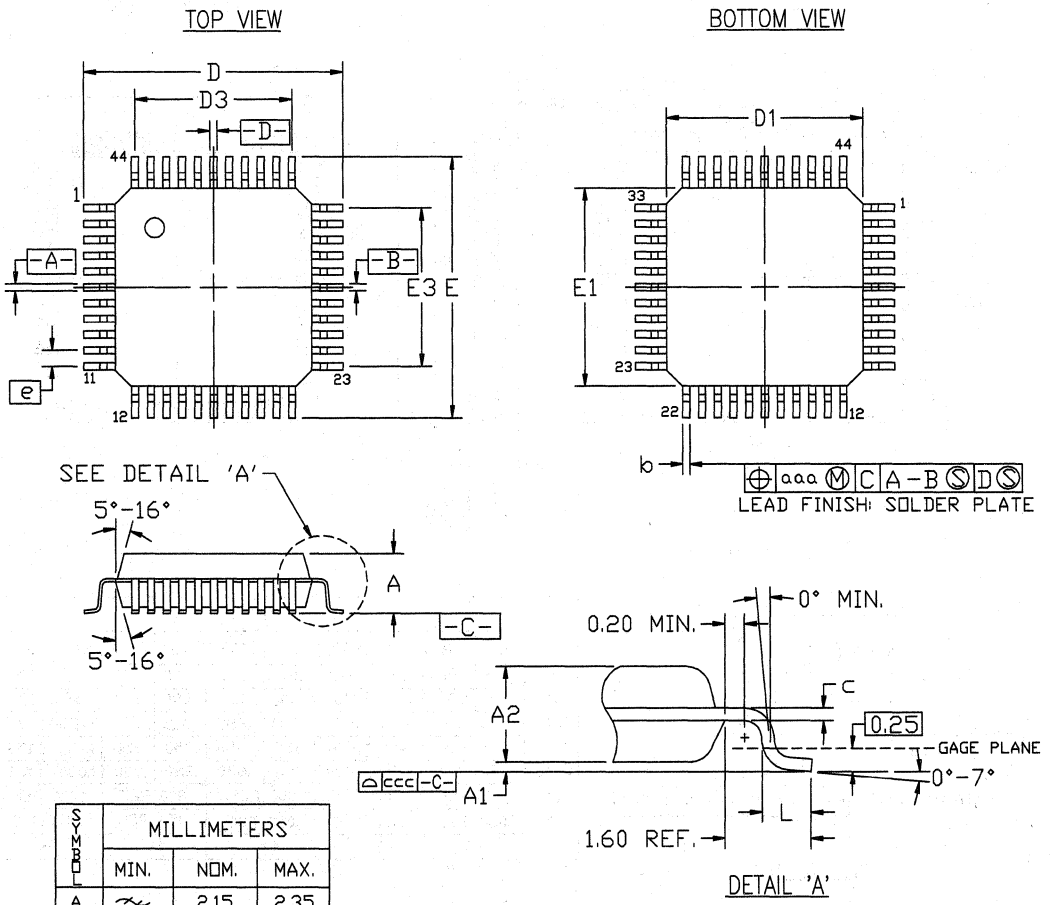
DETAIL "A"

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE.
3. "N" IS NUMBER OF TERMINALS.
4. CONFORM TO JEDEC MO-047
5. TOP OF PACKAGE MAY BE SMALLER THAN BOTTOM BY .010".

20, 28, 44, 68 and 84-PIN PLCC (PC20 THRU PC84)

PQFP Packages — PQ44, PQ100, PQ160, PQ208, PQ240, PQ304, HQ100, HQ160, HQ208, HQ240, HQ304



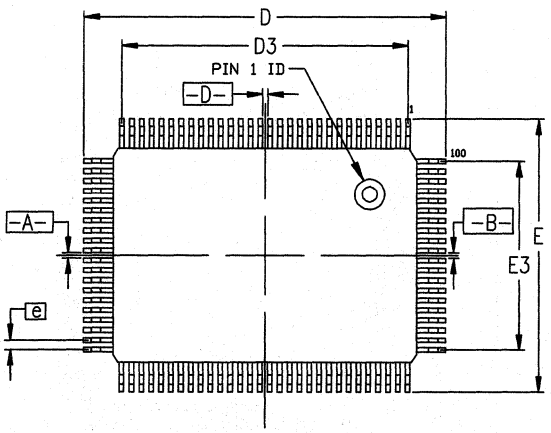
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.15	2.35
A_1	0.05		0.25
A_2	1.95	2.00	2.10
D/E	12.95	13.20	13.45
D_1/E_1	9.90	10.00	10.10
D_3/E_3		8.00 BSC	
L	0.73	0.88	1.03
e		0.80 BSC.	
b	0.30		0.45
c	0.13		0.23
aaa		0.20	
ccc			0.10

NOTES:

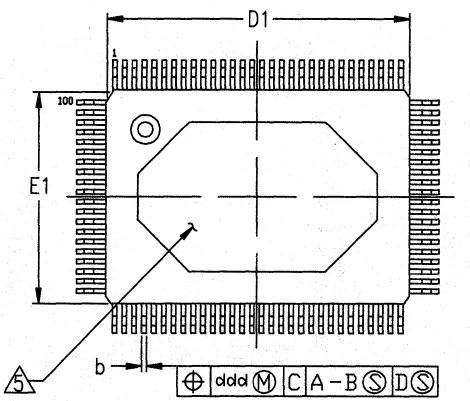
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
4. CONFORMS TO JEDEC MO–108–AA2

44–PIN PLASTIC PQFP (PQ44)

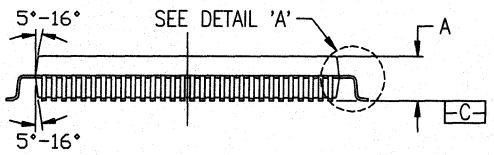
TOP VIEW

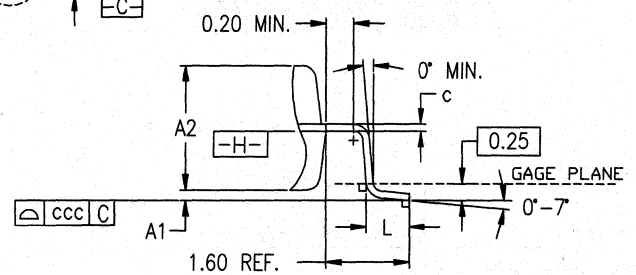


BOTTOM VIEW



LEAD FINISH: SOLDER PLATE





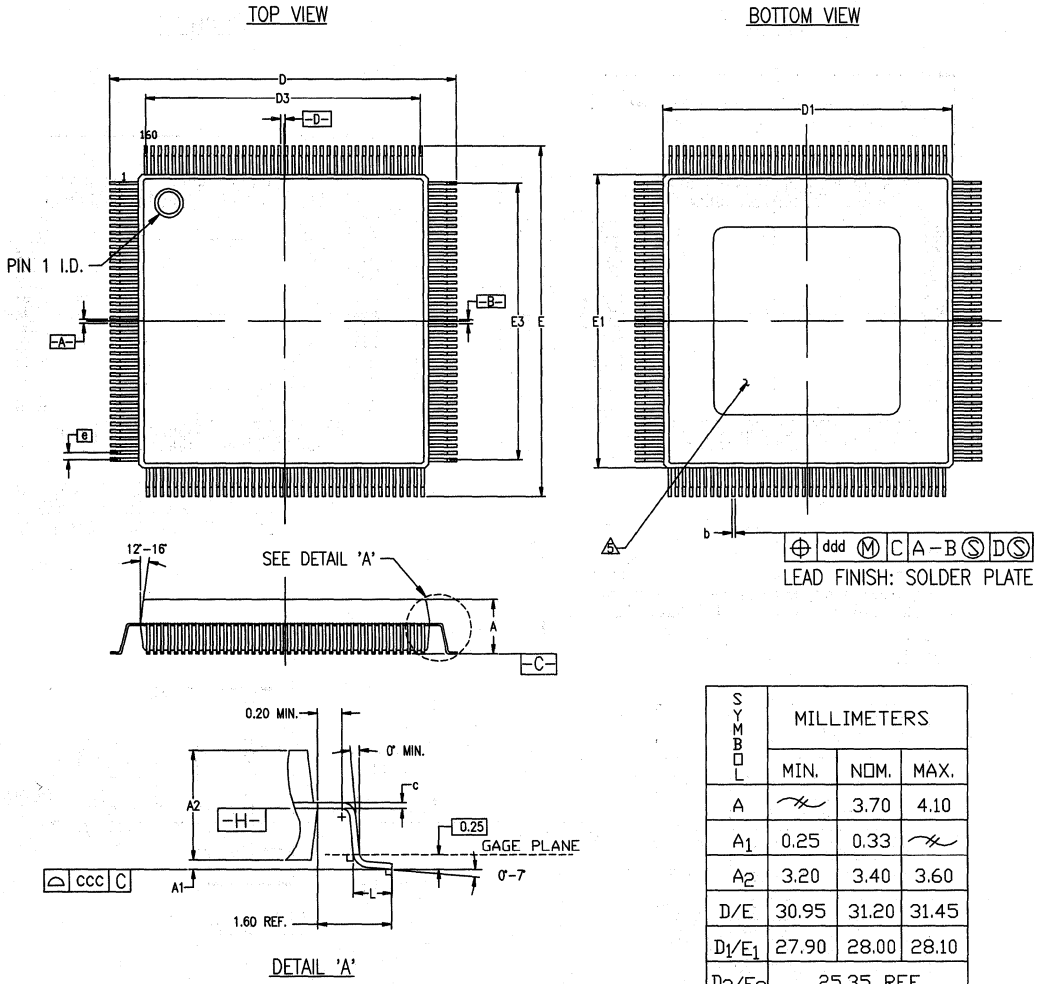
DETAIL 'A'

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			3.40
A_1	0.25		
A_2	2.55	2.80	3.05
D	22.95	23.20	23.45
D_1	19.90	20.00	20.10
D_3	18.85 REF.		
E	16.95	17.20	17.45
E_1	13.90	14.00	14.10
E_3	12.35 REF.		
L	0.73	0.88	1.03
e	0.65 BSC		
b	0.22		0.38
c	0.13		0.23
ccc			0.10
ddd			0.12

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25mm PER SIDE.
3. THE TOP OF PACKAGE MAY BE EQUAL TO OR SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
4. PACKAGE CONFORMS TO JEDEC OUTLINE MO-108-CC1
5. THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HQ".

100-PIN PQFP (PQ100)
100-PIN HEAT SINK PQFP (HQ100)

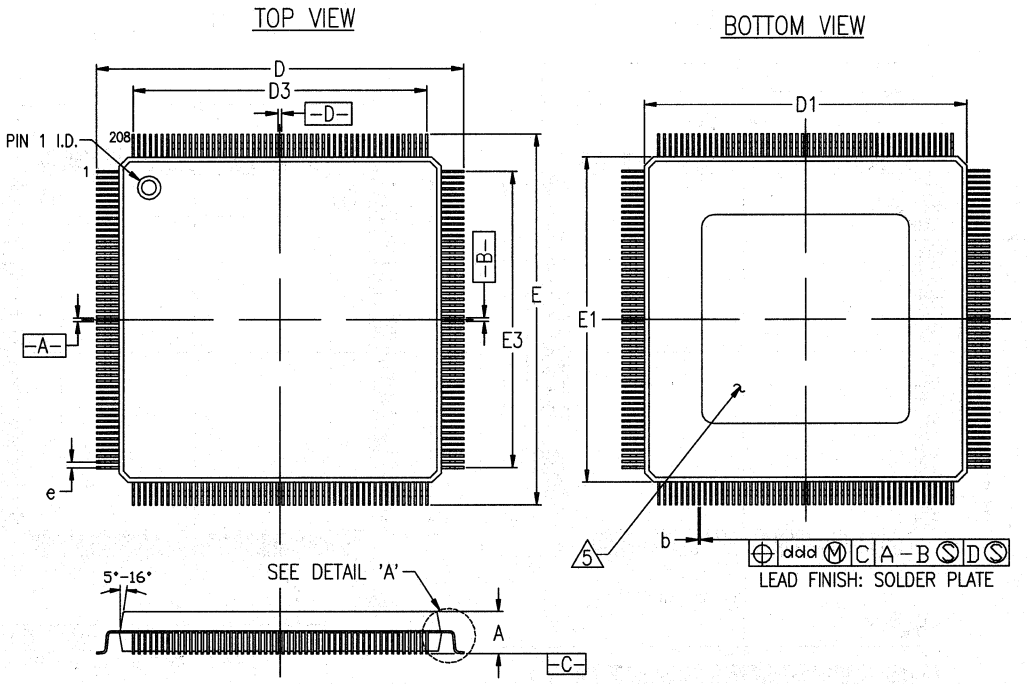


SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		3.70	4.10
A_1	0.25	0.33	
A_2	3.20	3.40	3.60
D/E	30.95	31.20	31.45
D_1/E_1	27.90	28.00	28.10
D_3/E_3	25.35 REF.		
L	0.73	0.88	1.03
e	0.65 BSC.		
b	0.22		0.38
c	0.13		0.23
ccc		0.10	
ddd		0.12	

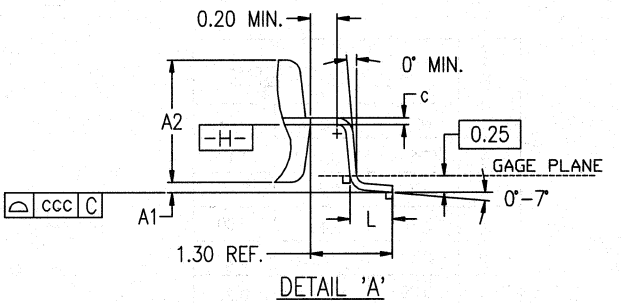
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. PACKAGE TOP DIMENSIONS MAY BE SMALLER THAN THE BOTTOM DIMENSIONS BY 0.20mm.
4. PACKAGE CONFORMS TO JEDEC MO-108-DD1
5. THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HQ".

160-PIN PQFP (PQ160)
160-PIN HEAT SINK PQFP (HQ160)



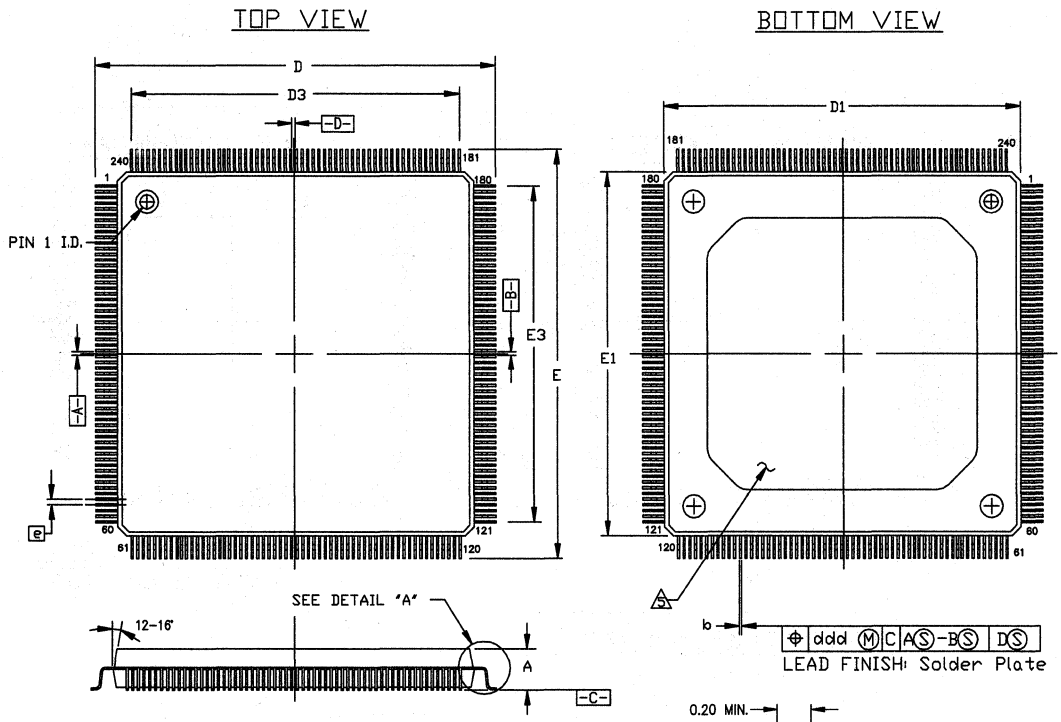
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	--	3.70	4.10
A_1	0.25	0.33	--
A_2	3.20	3.40	3.60
D/E	30.60 BSC		
D_1/E_1	28.00 BSC		
D_3/E_3	25.50 REF.		
L	0.50	0.60	0.75
e	0.50 BSC.		
b	0.17	0.22	0.27
c	0.09	--	0.20
ccc	--	--	0.08
ddd	--	--	0.08



NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. PACKAGE TOP DIMENSIONS MAY BE SMALLER THAN THE BOTTOM DIMENSIONS BY 0.20mm.
4. DRAWING CONFORMS TO JEDEC MO-143-FA-1
5. THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HQ".

208-PIN PQFP (PQ208)
208-PIN HEAT SINK PQFP (HQ208)



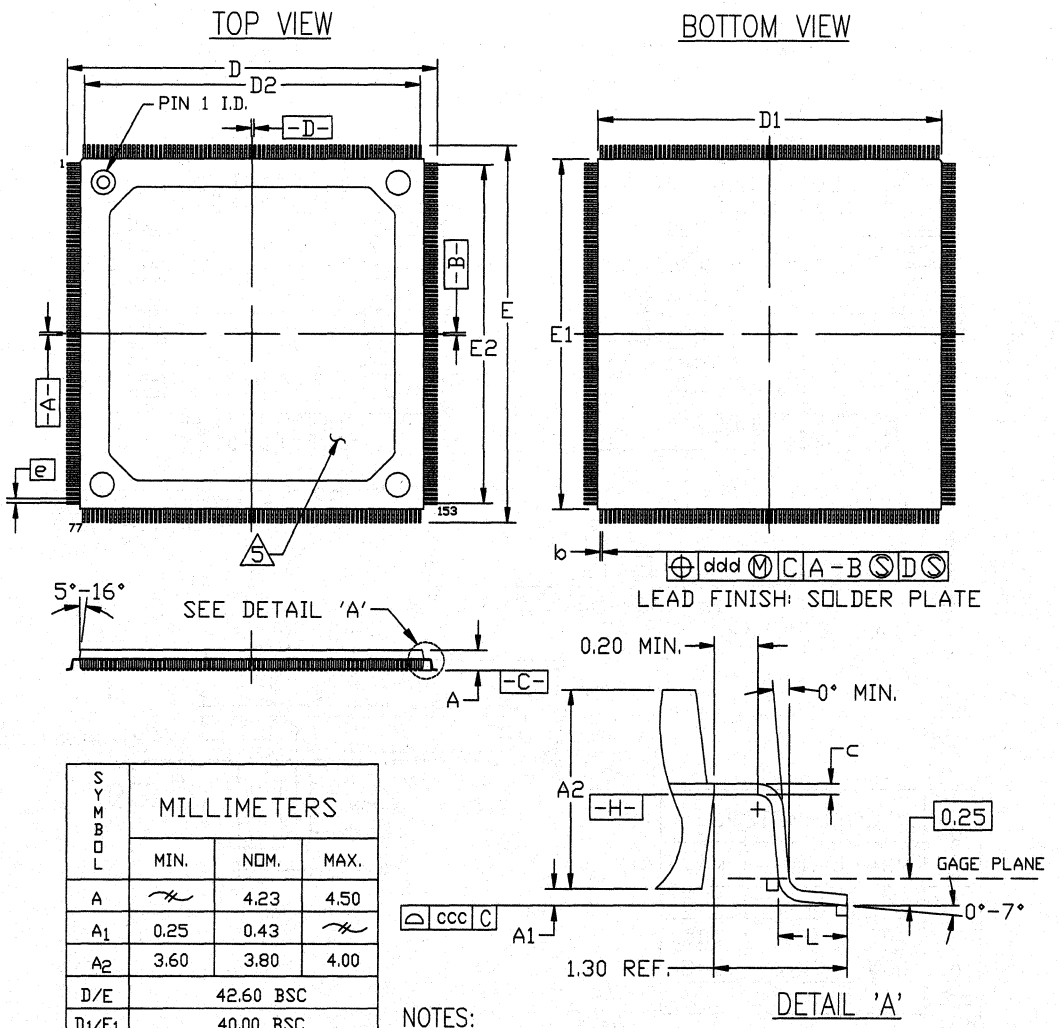
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		3.78	4.10
A_1	0.25	0.38	
A_2	3.20	3.40	3.60
b	0.17		0.27
c	0.09		0.20
D/E	34.60 BSC		
D_1/E_1	32.00 BSC		
D_3/E_3	29.50 REF.		
L	0.50	0.60	0.75
e	0.50 BSC.		
ddd	0.08		
ccc	0.08		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5–1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. PACKAGE TOP DIMENSIONS MAY BE SMALLER THAN BOTTOM DIMENSIONS BY 0.2mm.
4. CONFORMS TO JEDEC MO–143–GA

5. THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HQ".

240–PIN PQFP (PQ240)
240–PIN HEAT SINK PQFP (HQ240)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		4.23	4.50
A_1	0.25	0.43	
A_2	3.60	3.80	4.00
D/E	42.60 BSC		
D_1/E_1	40.00 BSC		
D_2/E_2	37.50 REF.		
L	0.45	0.60	0.75
e	0.50 BSC.		
b	0.17		0.27
b_1		0.20	
ccc	0.08		
ddd	0.07		

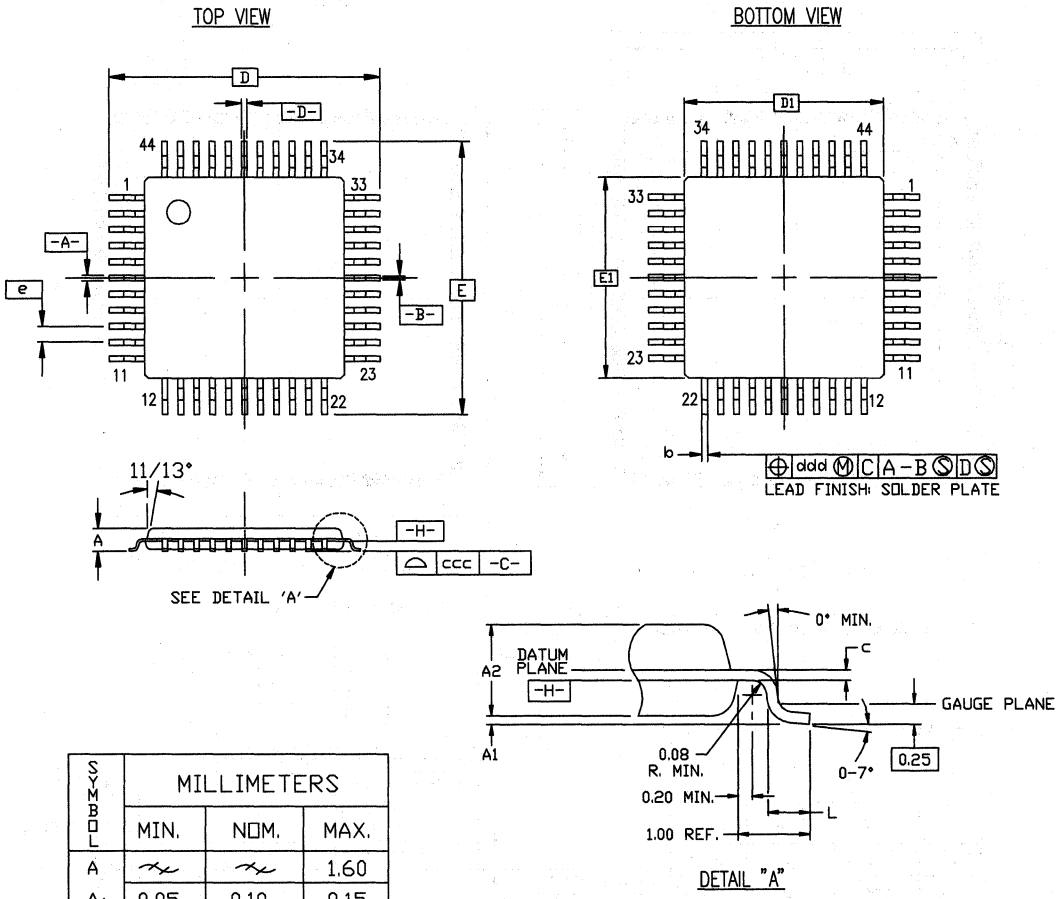
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. PACKAGE TOP DIMENSIONS MAY BE SMALLER THAN BOTTOM DIMENSIONS BY 0.15mm.
4. CONFORMS TO JEDEC OUTLINE MO-143-JA

5. THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HQ".

304-PIN PQFP (PQ304)
304-PIN HEAT SINK PQFP (HQ304)

TQFP Packages — TQ44, TQ100, TQ144, TQ176, HT100, HT144, HT176

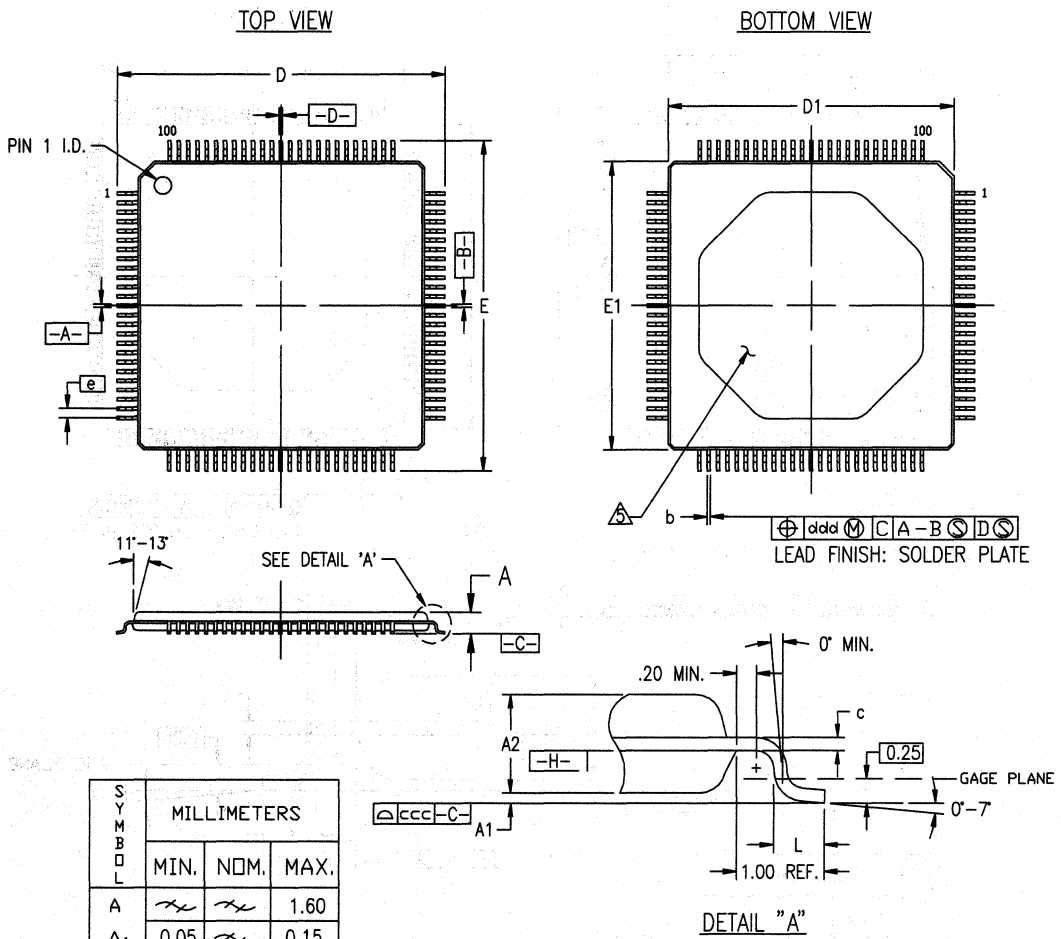


SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.60
A_1	0.05	0.10	0.15
A_2	1.35	1.40	1.45
D/E	12.00 BSC		
D_1/E_1	10.00 BSC		
b	0.30	0.37	0.45
c	0.09		0.20
e	0.80 BSC.		
L	0.45	0.60	0.75
ccc			0.10
ddd			0.20

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
4. CONFORMS TO JEDEC MS–026–BCB

44–PIN PLASTIC TQFP (TQ44)

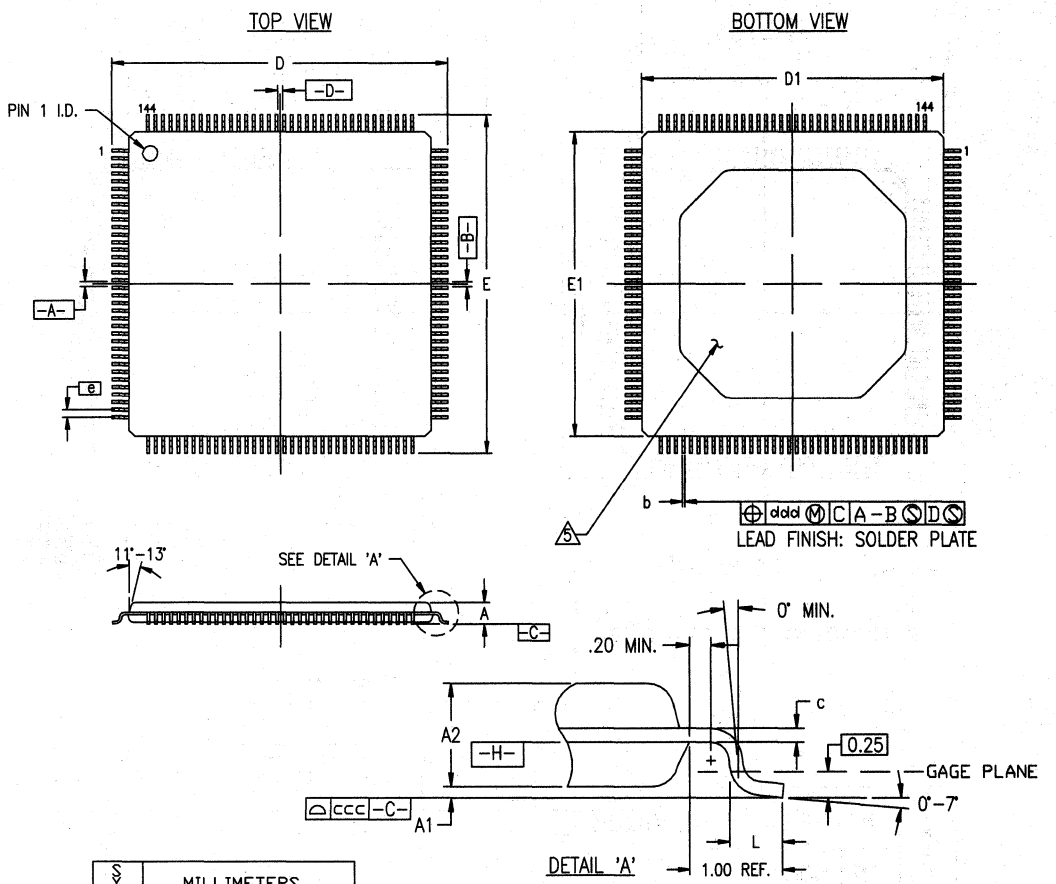


SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.60
A_1	0.05		0.15
A_2	1.35	1.40	1.45
D/E	16.00 BSC		
D_1/E_1	14.00 BSC		
L	0.45	0.60	0.75
e	0.50 BSC		
b	0.17	0.22	0.27
c	0.09		0.20
ccc			0.08
ddd			0.08

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. PACKAGE TOP DIMENSION MAY BE SMALLER THAN THE BOTTOM DIMENSION BY 0.15mm.
4. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026-BED
5. THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HT".

100-PIN TQFP (TQ100)
100-PIN HEAT SINK TQFP (HT100)



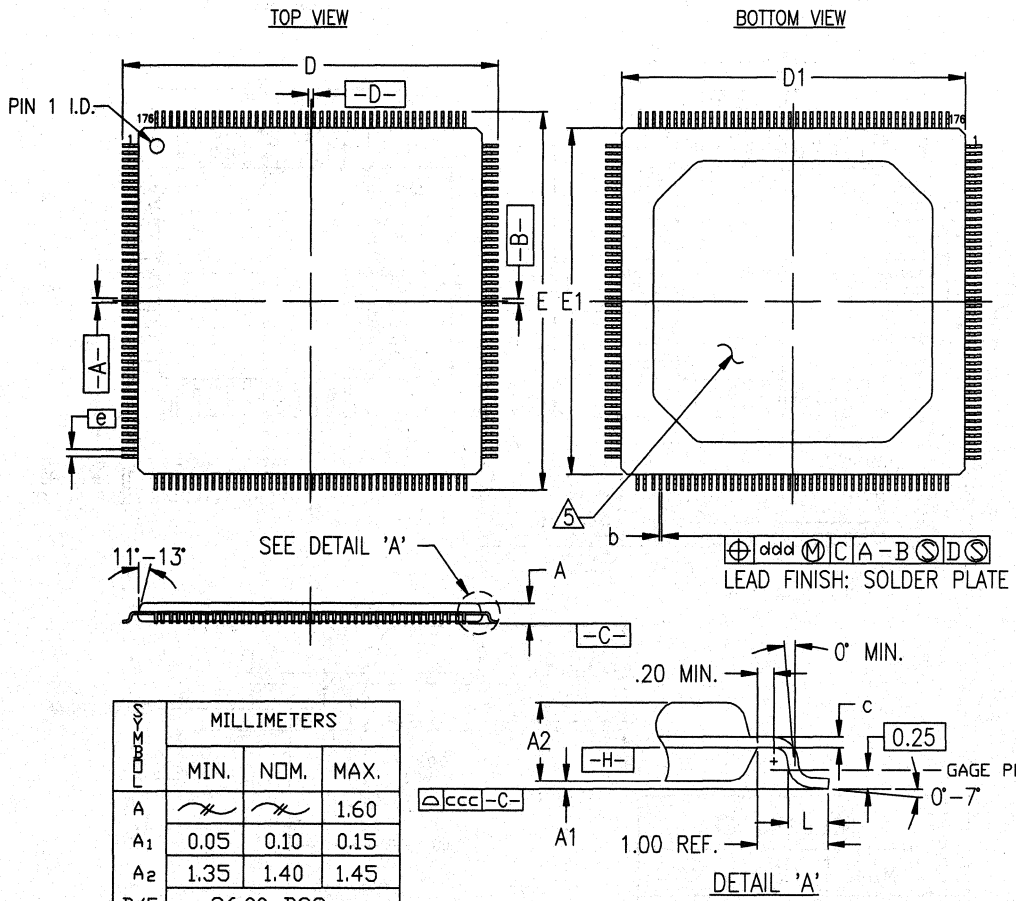
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.60
A_1	0.05	0.10	0.15
A_2	1.35	1.40	1.45
D/E	22.00 BSC		
D_1/E_1	20.00 BSC		
L	0.45	0.60	0.75
e	0.50 BSC		
b	0.17	0.22	0.27
c	0.09		0.20
ccc			0.08
ddd			0.08

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
4. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026-BFB

5. THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HT".

144-PIN TQFP (TQ144)
144-PIN HEAT SINK TQFP (HT144)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.60
A_1	0.05	0.10	0.15
A_2	1.35	1.40	1.45
D/E	26.00 BSC		
D_1/E_1	24.00 BSC		
L	0.45	0.60	0.75
e	0.50 BSC		
b	0.17	0.22	0.27
c	0.09		0.20
ccc			0.08
ddd			0.08

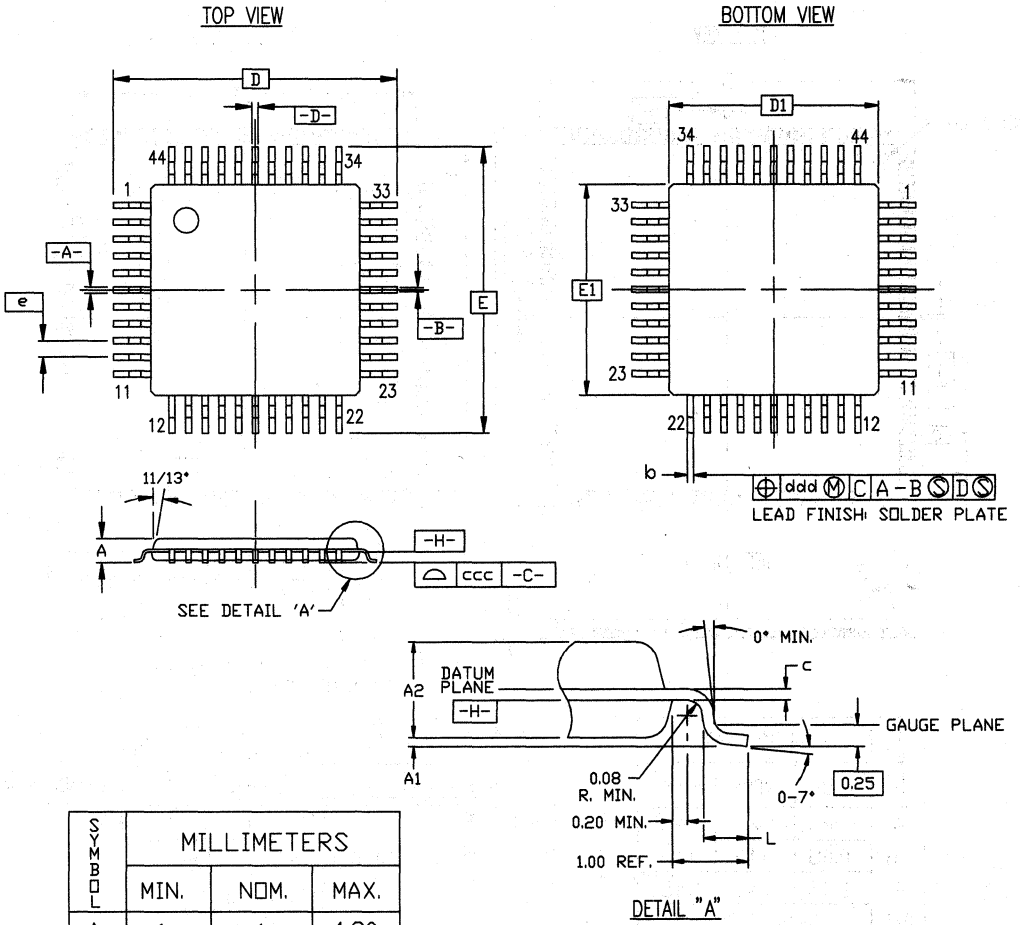
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
4. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026-BGA

5. THE SAME PACKAGE DIMESIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HT".

176-PIN TQFP (TQ176)
176-PIN HEAT SINK TQFP (HT176)

VQFP Packages — VQ44, VQ64, VQ100

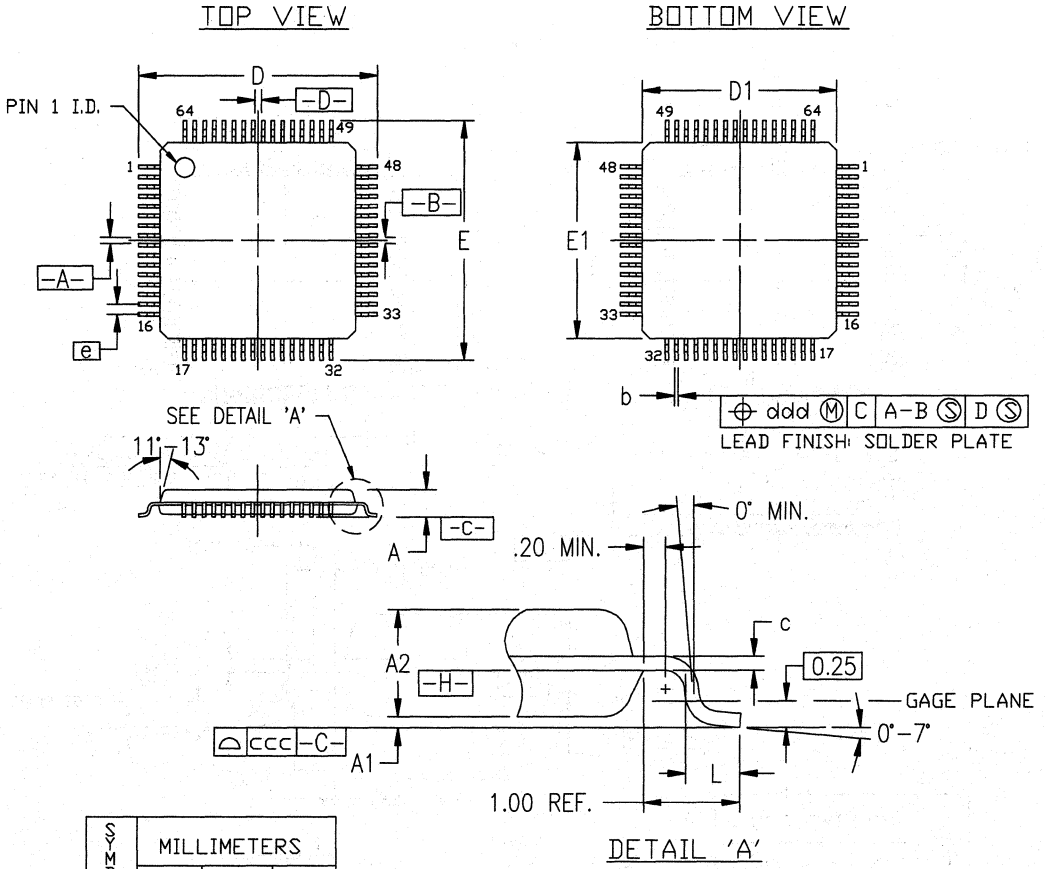


SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A_1	0.05	—	0.15
A_2	0.95	1.00	1.05
D/E	12.00 BSC		
D_1/E_1	10.00 BSC		
L	0.45	0.60	0.75
e	0.80 BSC.		
b	0.30	0.37	0.45
c	0.09	—	.020
ccc	—	—	0.10
ddd	—	—	0.20

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
4. CONFORMS TO JEDEC MS-026-ACB

44-PIN PLASTIC VQFP (VQ44)

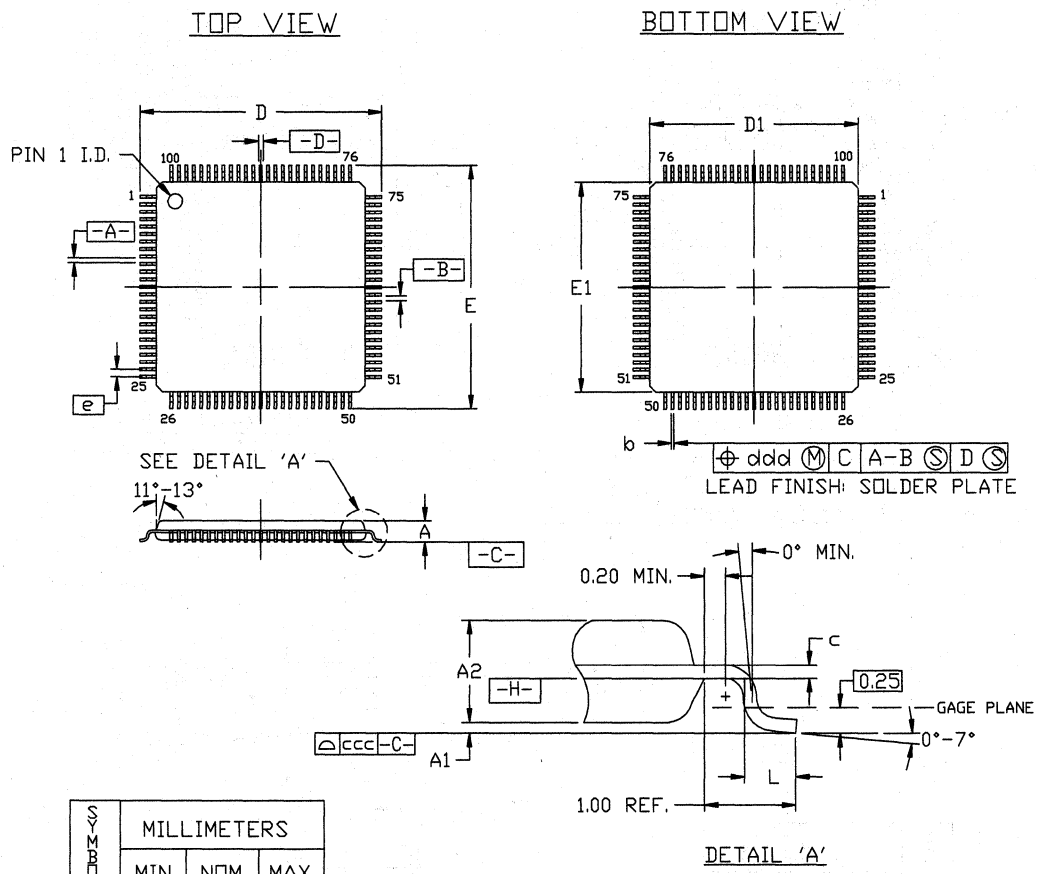


SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.20
A_1	0.05	0.10	0.15
A_2	0.95	1.00	1.05
D/E	12.00 BSC.		
D_1/E_1	10.00 BSC.		
b	0.17	0.22	0.27
c	0.09		0.20
e	0.50 BSC.		
L	0.45	0.60	0.75
ccc			0.08
ddd			0.08

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25mm PER SIDE.
3. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
4. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026-ACD

64-PIN PLASTIC VQFP (VQ64)



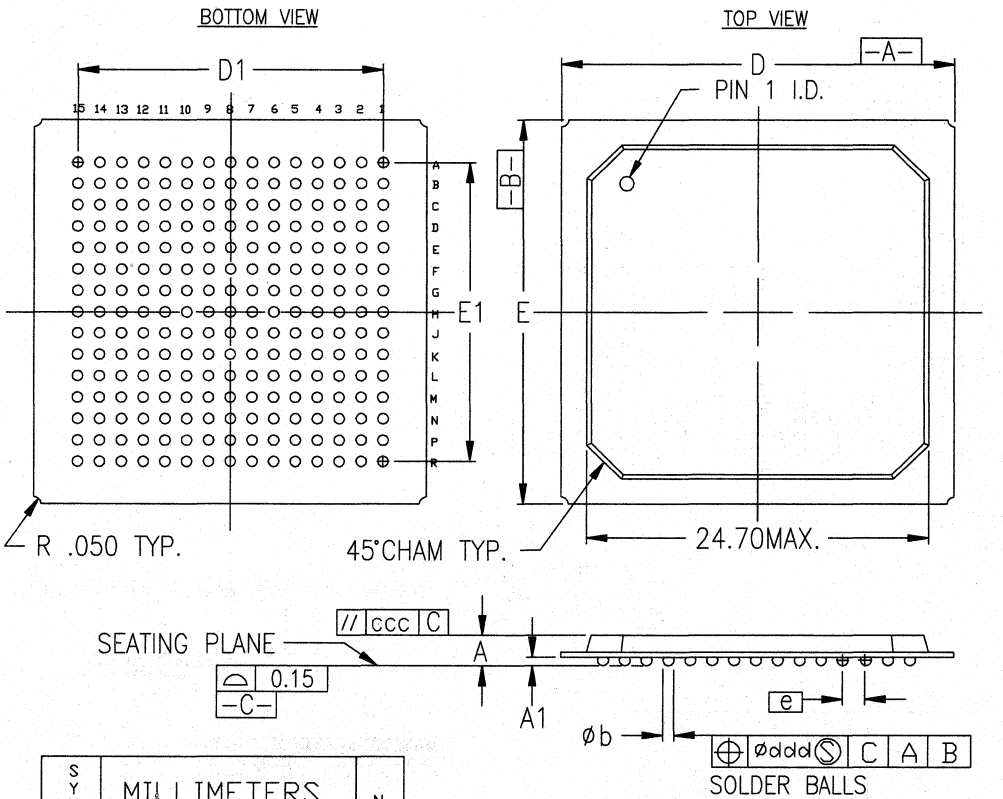
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.20
A_1	0.05	0.10	0.15
A_2	0.95	1.00	1.05
D/E	16.00 BSC.		
D_1/E_1	14.00 BSC.		
b	0.17	0.22	0.27
c	0.09		0.20
e	0.50 BSC.		
L	0.45	0.60	0.75
ccc			0.08
ddd			0.08

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
4. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026-AED.

100-PIN PLASTIC VQFP (VQ100)

BGA Packages — BG225, BG352, BG432

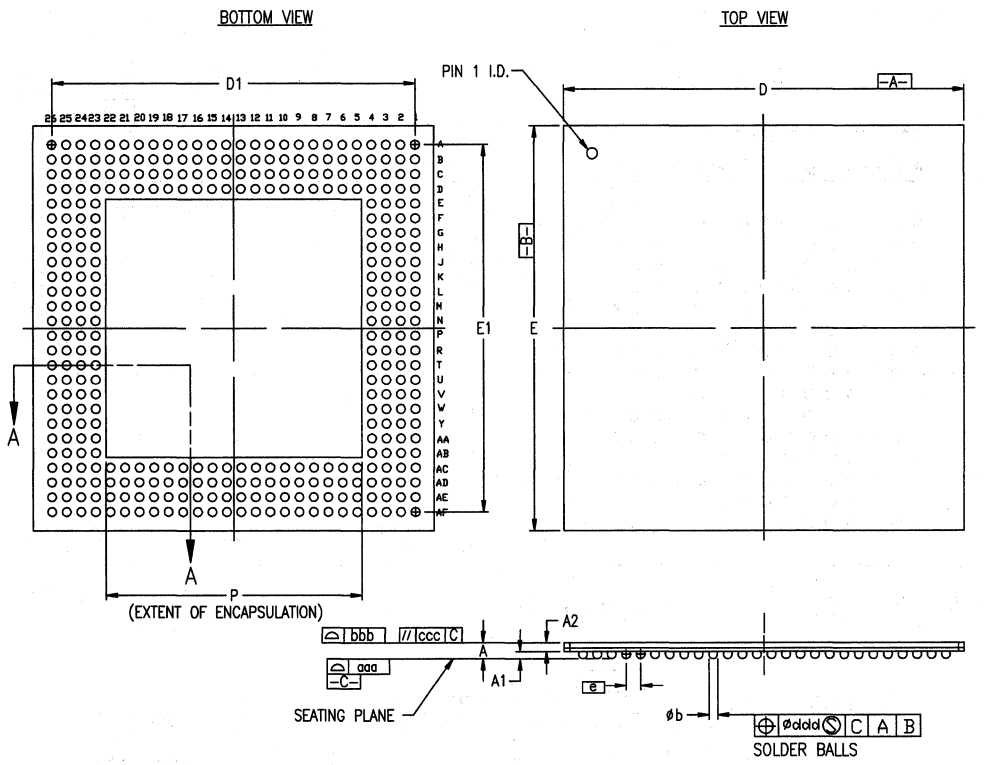


SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	---	2.15	3.50	
A_1	0.50	0.60	0.70	
D/E	26.80	27.00	27.20	
D_1/E_1	---	21.00	---	
e	1.50 BSC			
øb	0.60	0.75	0.90	
ccc	---	---	0.35	
ddd	---	---	0.30	
M	15			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–151–CAL (DEPOPULATED)

225–BALL PLASTIC BGA (BG225)

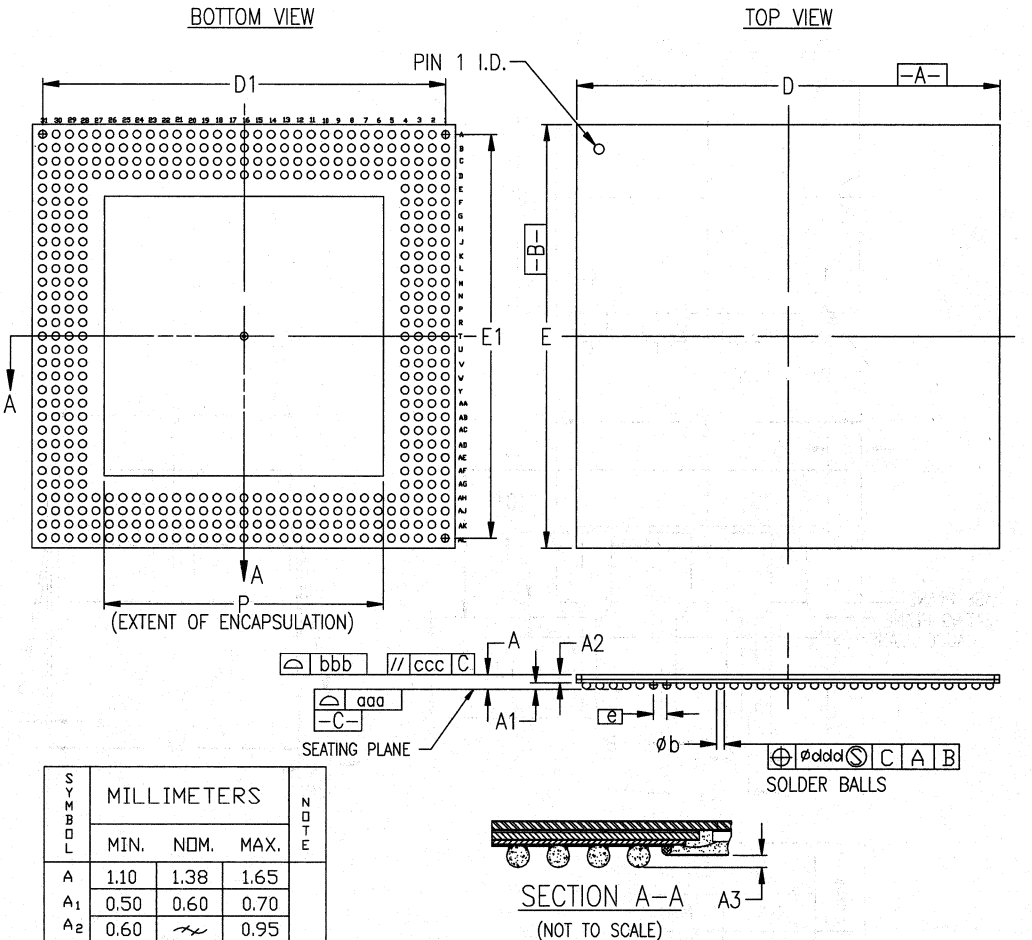


SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.10	1.38	1.65	
A_1	0.50	0.60	0.70	
A_2	0.60	~~~	0.95	
A_3	0.25	~~~	~~~	
D/E	34.80	35.00	35.20	
D_1/E_1	~~~	31.75	~~~	
e	1.27 BSC			
øb	0.60	0.75	0.90	
P	~~~	~~~	25.70	
aaa	~~~	~~~	0.15	
bbb	~~~	~~~	0.20	
ccc	~~~	~~~	0.25	
ddd	~~~	~~~	0.30	
M	26			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO-151-BAR (DEPOPULATED)

352-BALL PLASTIC BGA (BG352)
CAVITY DOWN



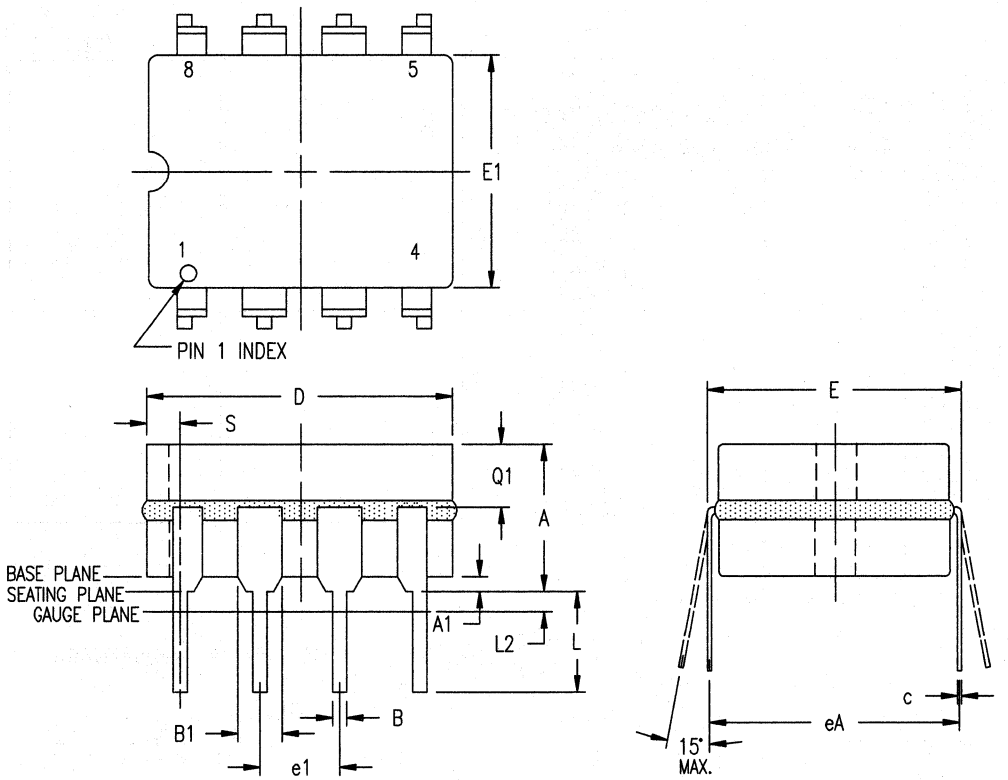
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.10	1.38	1.65	
A_1	0.50	0.60	0.70	
A_2	0.60	---	0.95	
A_3	0.25	---	---	
D/E	39.80	40.00	40.20	
D_1/E_1	38.00	38.10	38.20	
e	1.27 BSC			
øb	0.60	0.75	0.90	
P	---	---	26.40	
aaa	---	---	0.15	
bbb	---	---	0.20	
ccc	---	---	0.25	
ddd	---	---	0.30	
M	31			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO-151-BAU (DEPOPULATED)

432-BALL PLASTIC BGA (BG432)
CAVITY DOWN

Ceramic DIP Packages — DD8



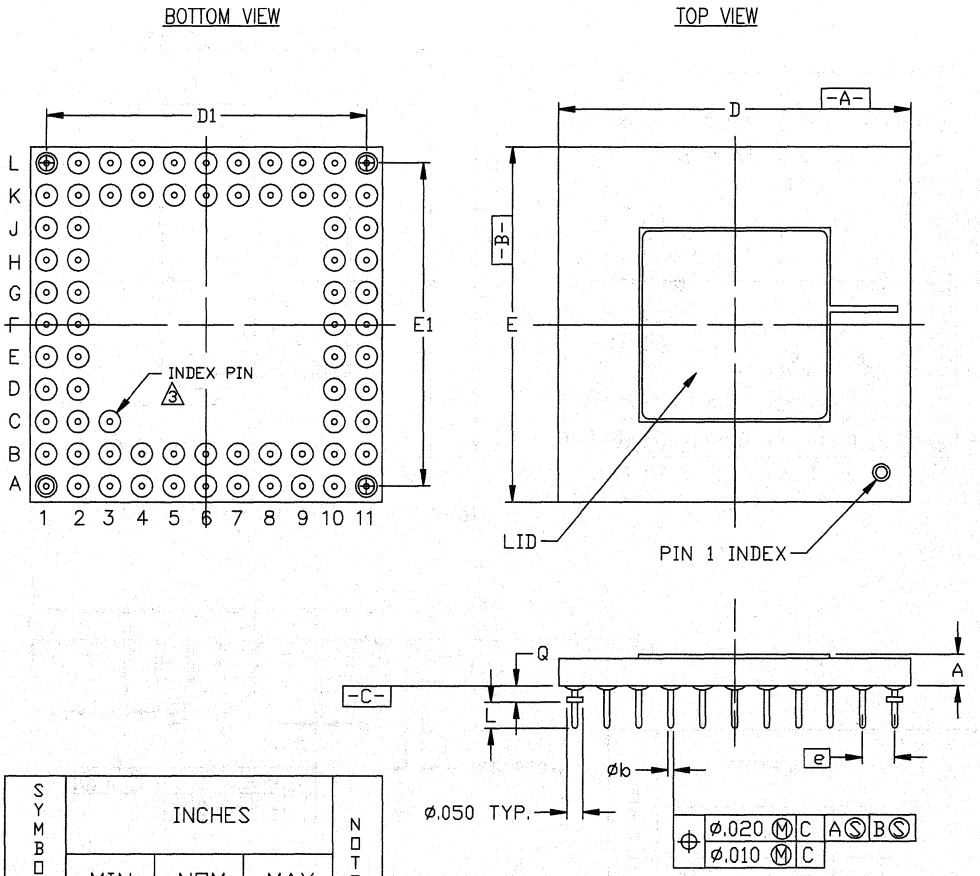
SYMBOL	INCHES	
	MIN.	MAX.
A	0.150	0.170
A_1	0.020	0.050
B	0.015	0.020
B_1	0.050	0.060
c	0.009	0.012
D	0.375	0.405
E	0.300	0.320
E_1	0.280	0.300
e_1	0.100 BSC	
e_A	0.300 BSC	
L	0.125	0.150
L_2	0	0.030
Q_1	0.040	0.075

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. LEAD FINISH: SOLDER DIPPED
3. CONFORMS TO JEDEC MO–001–AN EXCEPT BODY WIDTH.

8–PIN CERAMIC DIP (DD8)

Ceramic PGA Packages — PG68, PG84, WG84, PG120, PG132, PG144, PG156, PG175, PG191, PG223, PG299, PG411

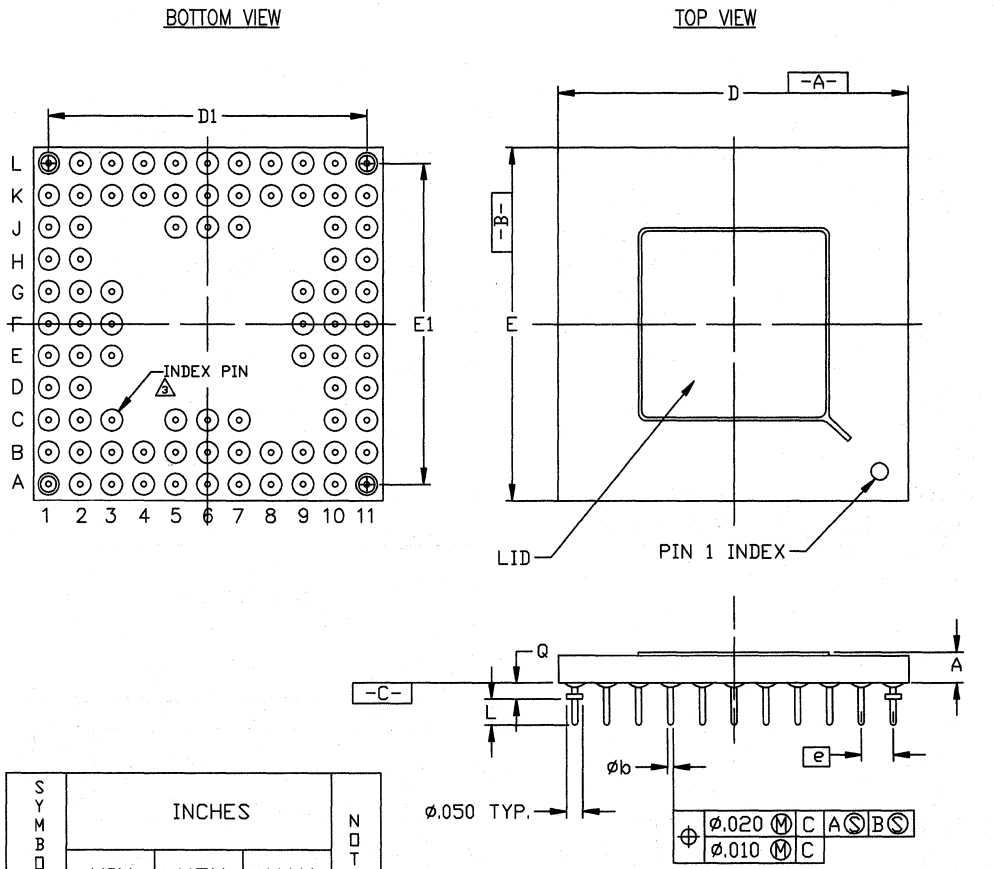


SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A			.145	
D/E	1.090	1.100	1.115	
D_1/E_1	1.000 BSC			
L	.120	.130	.140	
Q	.045		.060	
e	.100 BSC			
øb	.016	.018	.020	
M	11			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. PIN C3 MAY OR MAY NOT BE ELECTRICALLY CONNECTED.
4. LEAD FINISH: GOLD PLATED PINS
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)
5. PACKAGE CONFORMS TO JEDEC MO–66–AC

68–PIN CERAMIC PGA (PG68)

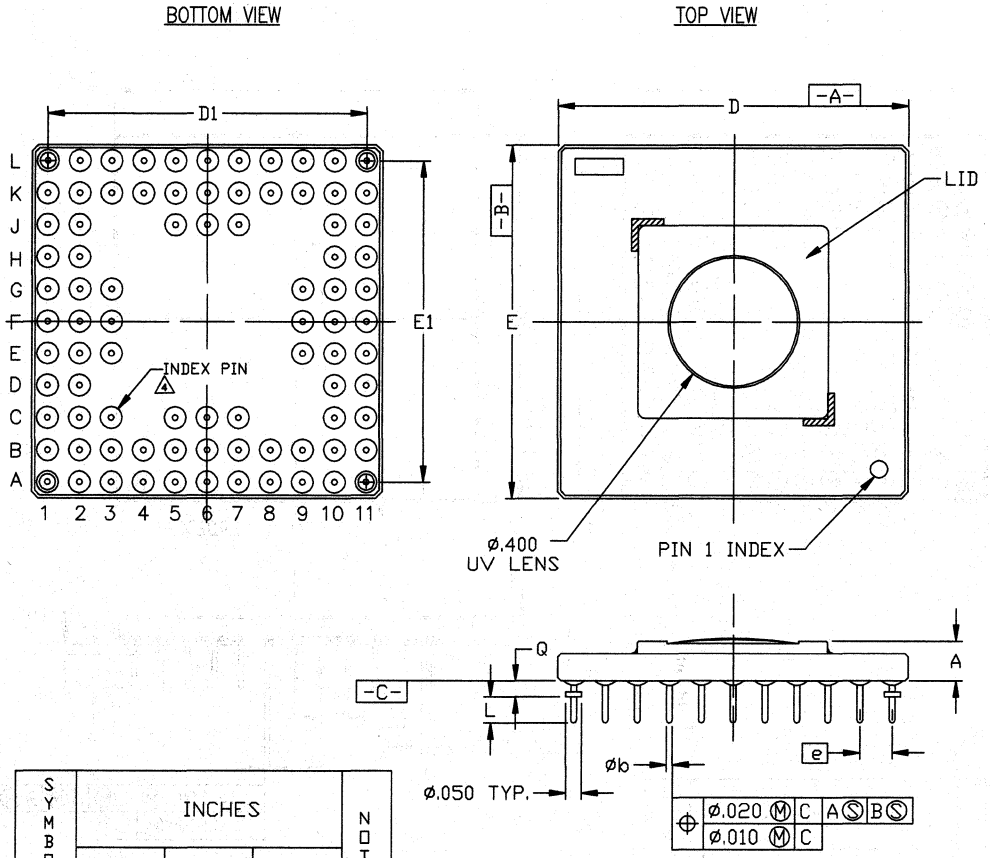


SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A			.145	
D/E	1.090	1.100	1.115	
D_1/E_1	1.000 BSC			
L	.120	.130	.140	
Q	.045		.060	
e	.100 BSC			
øb	.016	.018	.020	
M	11			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. PIN C3 MAY OR MAY NOT BE ELECTRICALLY CONNECTED.
4. CONFORMS TO JEDEC MO–066–AC
5. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

84–PIN CERAMIC PGA (PG84)

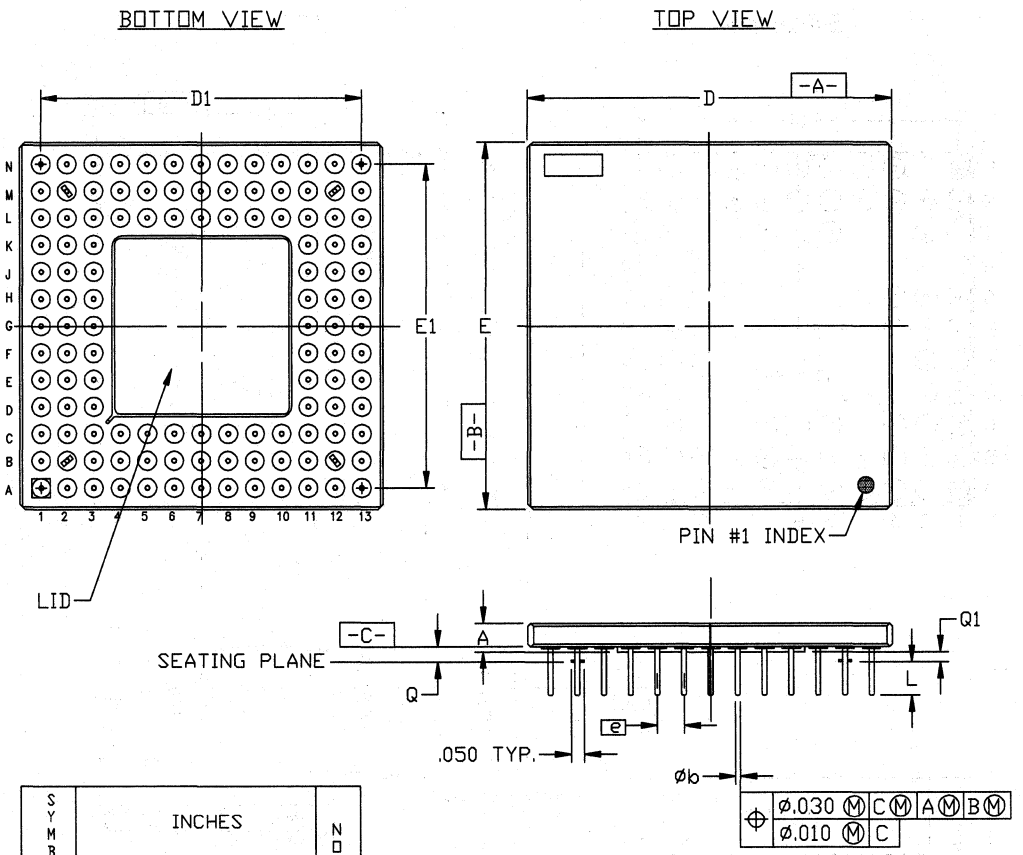


SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A			.145	
D/E	1.090	1.100	1.135	
D_1/E_1	1.000 BSC			
L	.120	.130	.140	
Q	.045		.060	
e	.100 BSC			
øb	.016	.018	.020	
M	11			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–066–AC
4. PIN C3 MAY OR MAY NOT BE ELECTRICALLY CONNECTED.
5. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

84–PIN WINDOWED PGA (WG84)

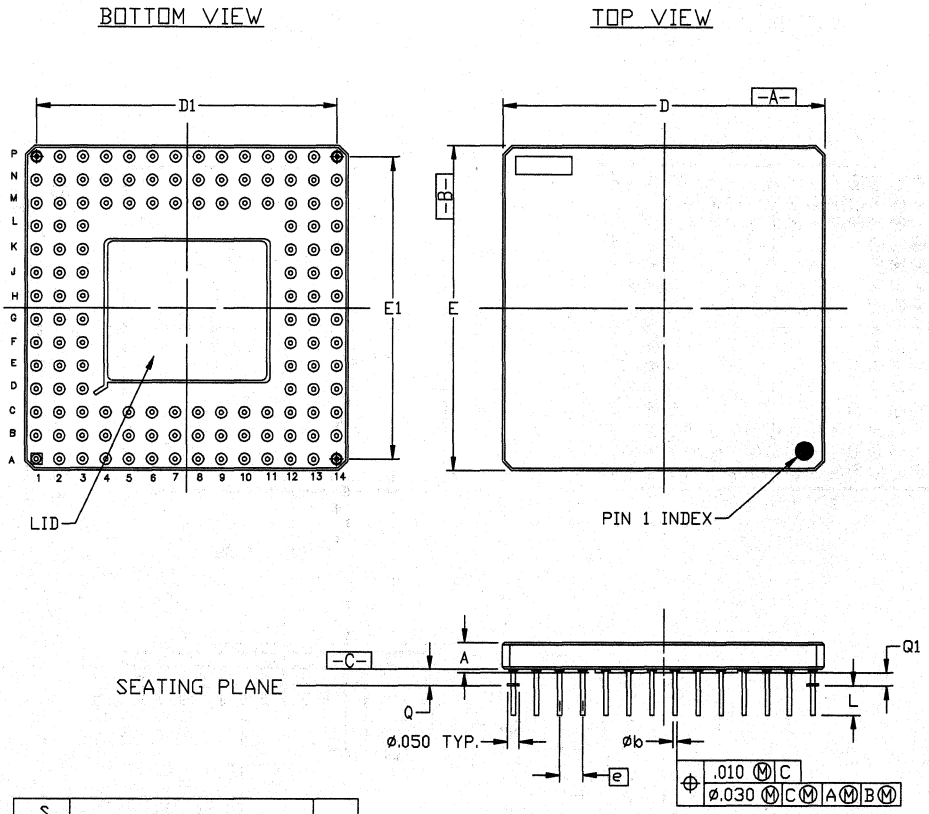


SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A			.145	
D/E	1.340	1.360	1.380	
D_1/E_1	1.200 BSC			
L	.120	.130	.140	
Q	.045		.060	
Q_1	.025			
e	.100 BSC			
øb	.016	.018	.020	
M	13			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–067–AE
4. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

120–LEAD CERAMIC PGA (PG120)

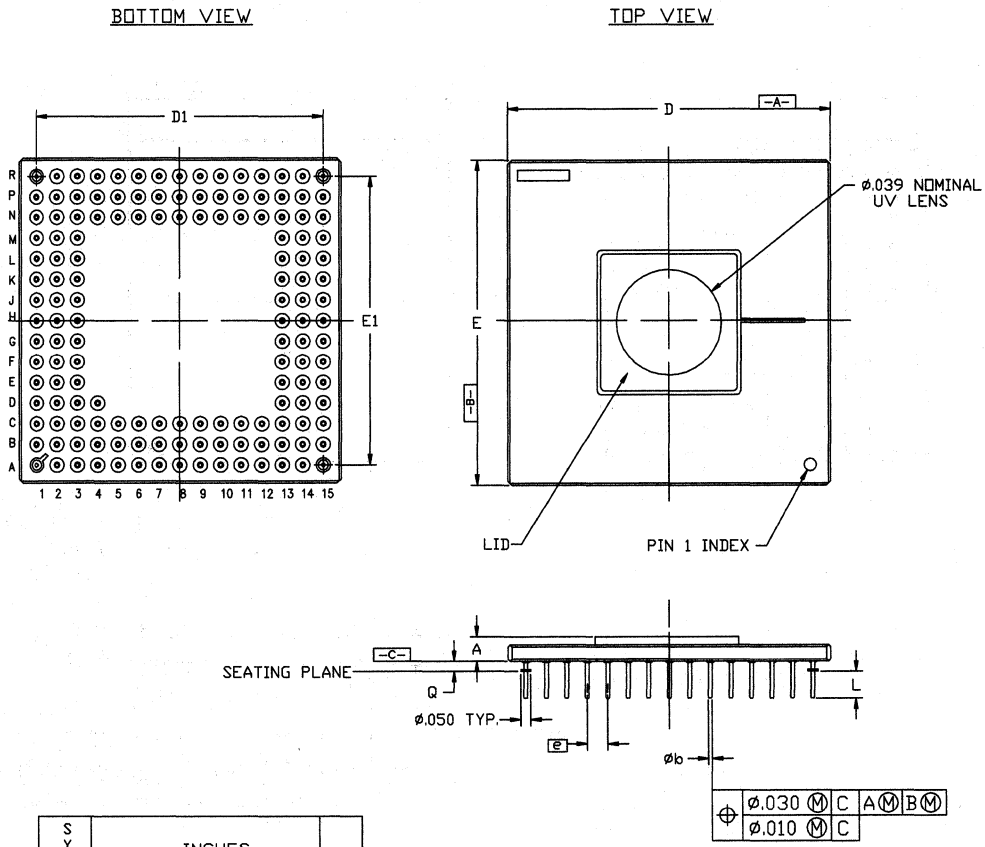


SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A			.145	
D/E	1.440	1.460	1.480	
D_1/E_1	1.300 BSC			
L	.120	.130	.140	
Q	.045		.060	
Q_1	.025			
e	.100 BSC			
øb	.016	.018	.020	
M	14			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–067–AF
4. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

132–PIN CERAMIC PGA (PG132)

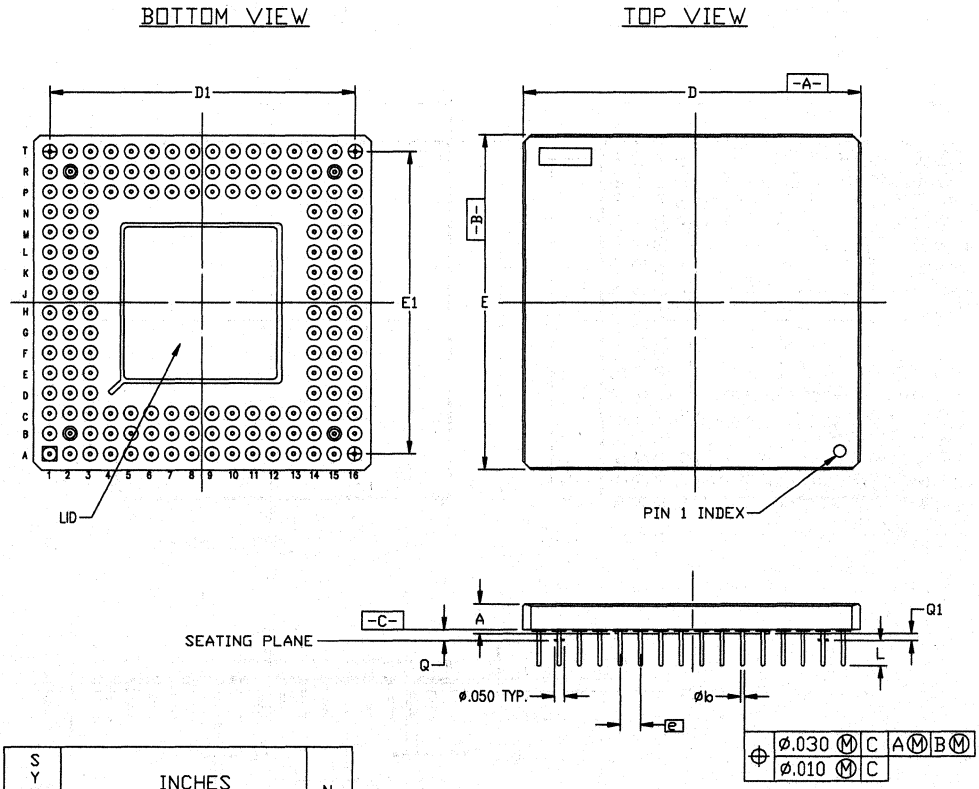


SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A	~	~	.145	
D/E	1.540	1.560	1.580	
D_1/E_1	1.400 BSC			
L	.120	.130	.140	
Q	.050	~	.060	
e	.100 BSC			
øb	.016	.018	.020	
M	15			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–067–AG
4. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

144–PIN WINDOWED PGA (PG144)

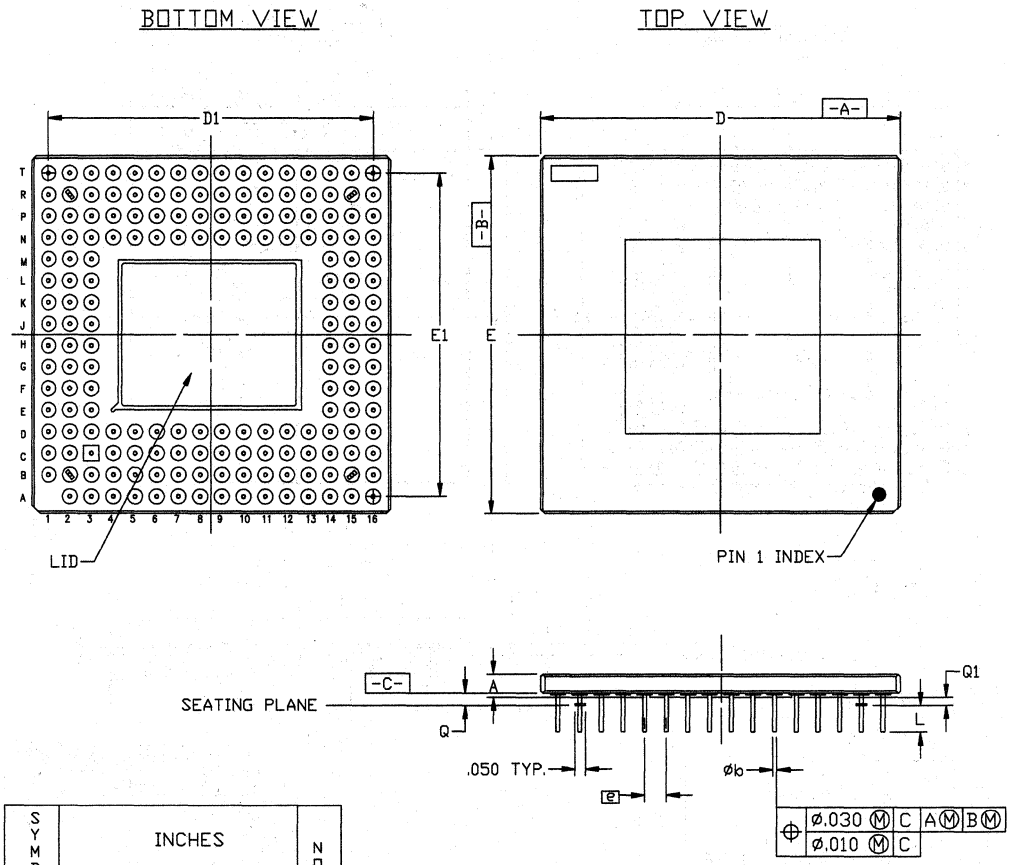


SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A			.145	
D/E	1.640	1.660	1.680	
D_1/E_1	1.500 BSC			
L	.120	.130	.140	
Q	.045		.060	
Q_1	.025			
e	.100 BSC			
øb	.016	.018	.020	
M	16			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–067–AH
4. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

156–PIN CERAMIC PGA (PG156)

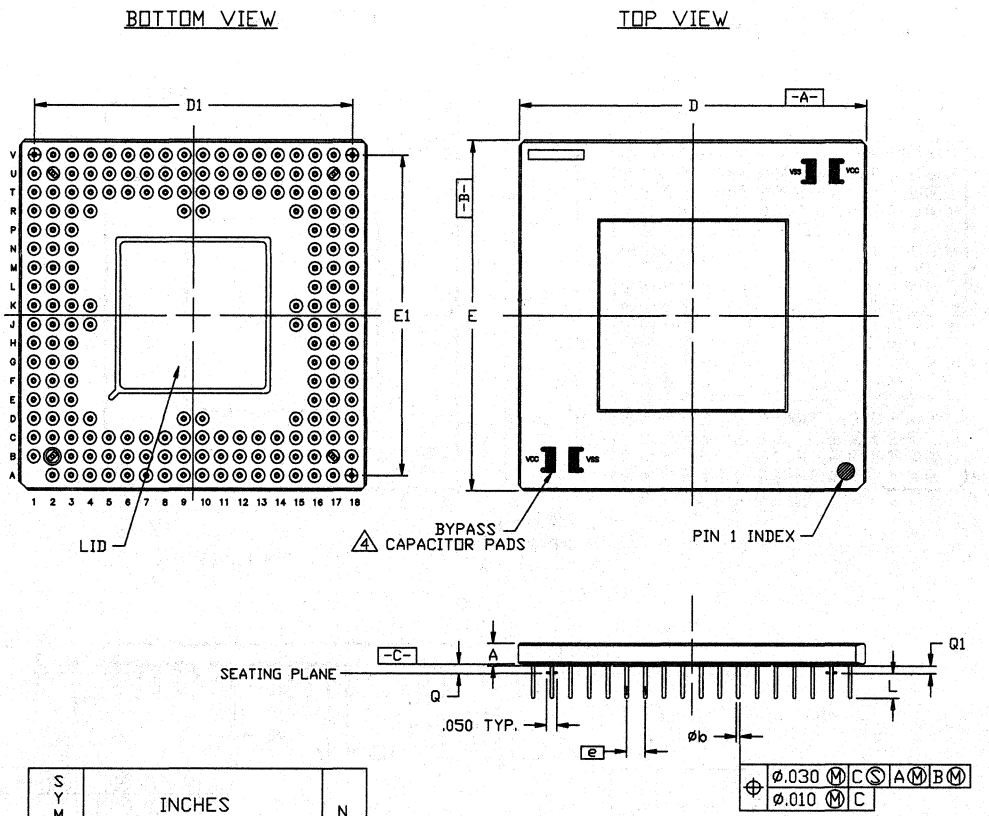


SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A			.145	
D/E	1.640	1.660	1.680	
D_1/E_1	1.500 BSC			
L	.120	.130	.140	
Q	.045		.060	
Q_1	.025			
e	.100 BSC			
øb	.016	.018	.020	
M	16			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–067–AH
4. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

175–PIN CERAMIC PGA (PG175)

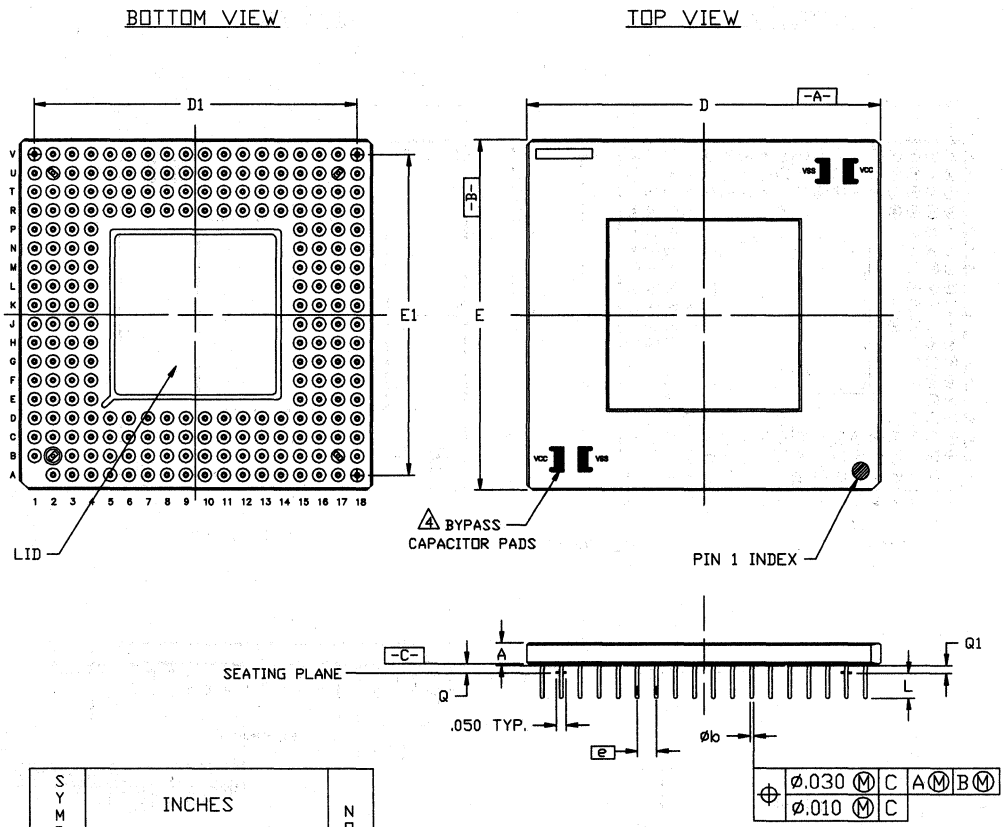


SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A	---	.115	.145	
D/E	1.840	1.860	1.880	
D_1/E_1	1.700 BSC			
L	.120	.130	.140	
Q	.045	---	.060	
Q_1	.025	---	---	
e	.100 BSC			
øb	.016	.018	.020	
M	18			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–067–AK
4. BYPASS CAPACITOR PADS – GOLD PLATED. MAY OR MAY NOT BE PRESENT ON ALL PACKAGES.
5. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

191–PIN CERAMIC PGA (PG191)

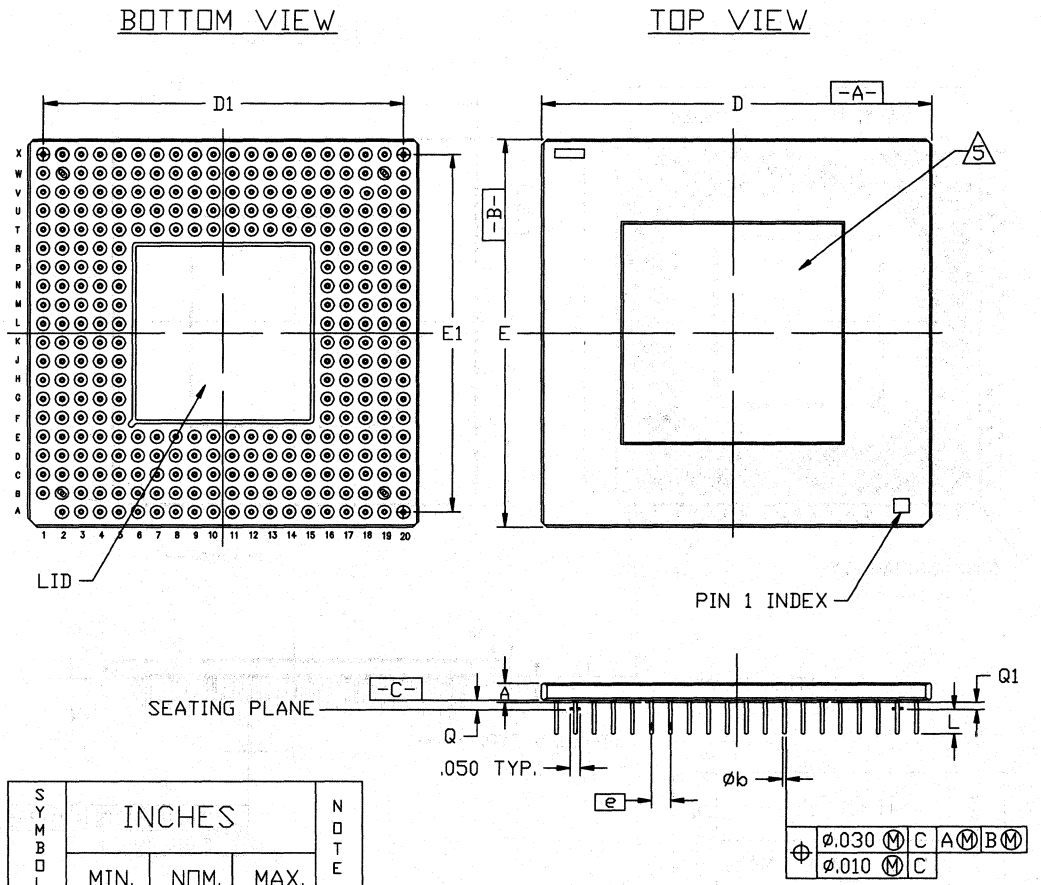


SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A		.115	.145	
D/E	1.840	1.860	1.880	
D_1/E_1	1.700 BSC			
L	.120	.130	.140	
Q	.045		.060	
Q_1	.025			
e	.100 BSC			
øb	.016	.018	.020	
M	18			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–067–AK
4. BYPASS CAPACITOR PADS – GOLD PLATED. MAY OR MAY NOT BE PRESENT ON ALL PACKAGES.
5. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

223–PIN CERAMIC PGA (PG223)



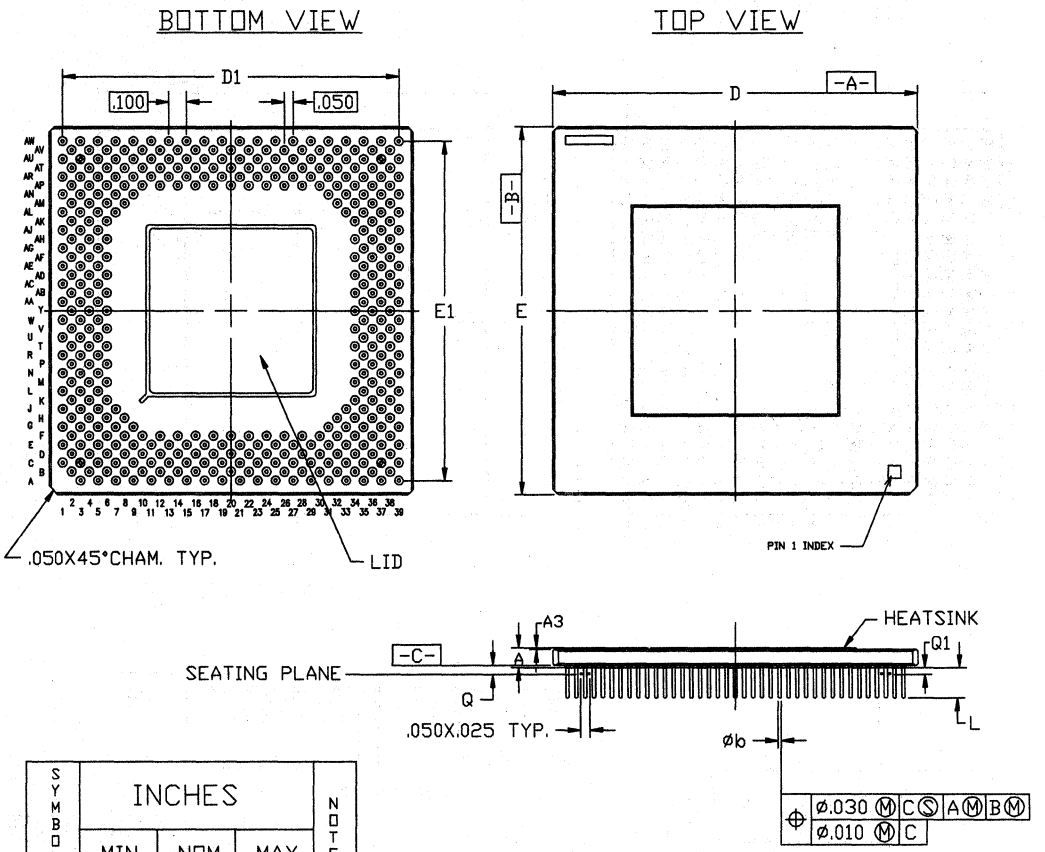
SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A	---	---	.145	5
D/E	2.040	2.060	2.080	
D_1/E_1	1.900 BSC			
L	.120	.130	.140	
Q	.045	---	.060	
Q_1	.025	---	---	
e	.100 BSC			
øb	.016	.018	.020	
M	20			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–067–AM
4. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

5. OPTION – HEAT SINK MAY BE ADDED FOR HIGH POWER DEVICES BUT DIMENSION 'A' REMAINS .145" MAX.

299–PIN CERAMIC PGA (PG299)



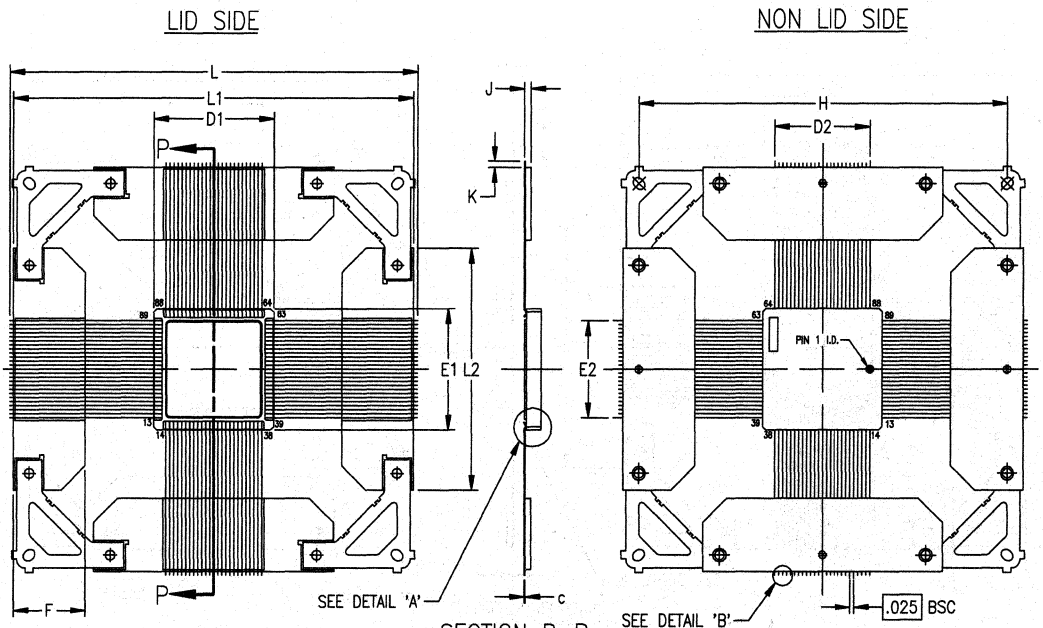
SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A			.145	
A3	.015	.020	.025	
D/E	2.040	2.060	2.080	
D_1/E_1	1.900 BSC			
L	.170	.180	.190	
Q	.045		.060	
Q_1	.025			
M	39			
øb	.016	.018	.020	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
3. SYMBOL "M" IS THE PIN MATRIX SIZE.
4. CONFORMS TO JEDEC MO–128.
5. LEAD FINISH: GOLD PLATED
   - COMMERCIAL (35 MICROINCHES MIN.)
   - MILITARY (50 MICROINCHES MIN.)

411–PIN CERAMIC PGA (PG411)

Ceramic Brazed QFP Packages — CB100, CB164, CB196, CB228

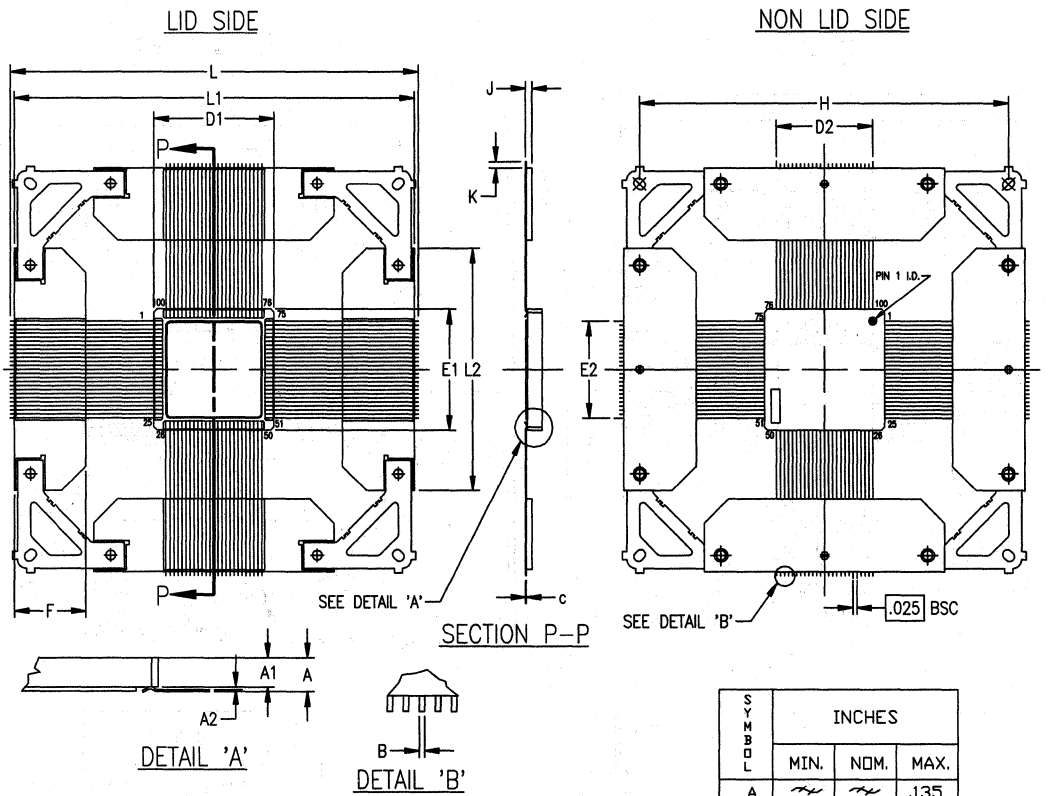


SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A	---	---	.135
A1	---	---	.115
A2	---	---	.020
B	.006	.008	.012
C	.005	.006	.009
D1/E1	.740	.750	.765
D2/E2	.600 BSC		
F	.425	.450	.475
H	2.300 BSC		
J	.030	.035	.040
K	---	---	.020
L	---	---	2.580
L1	2.490	2.500	2.510
L2	1.480	1.500	1.520
N	100		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "N" IS THE NUMBER OF TERMINALS.
3. PACKAGES ARE SHIPPED UNFORMED.
4. LEAD FINISH: GOLD (50 MICROINCHES MINIMUM) OVER NICKEL PER MIL–I–38535

100–PIN CERAMIC BRAZED CQFP (CB100)
(XC3000 VERSION)

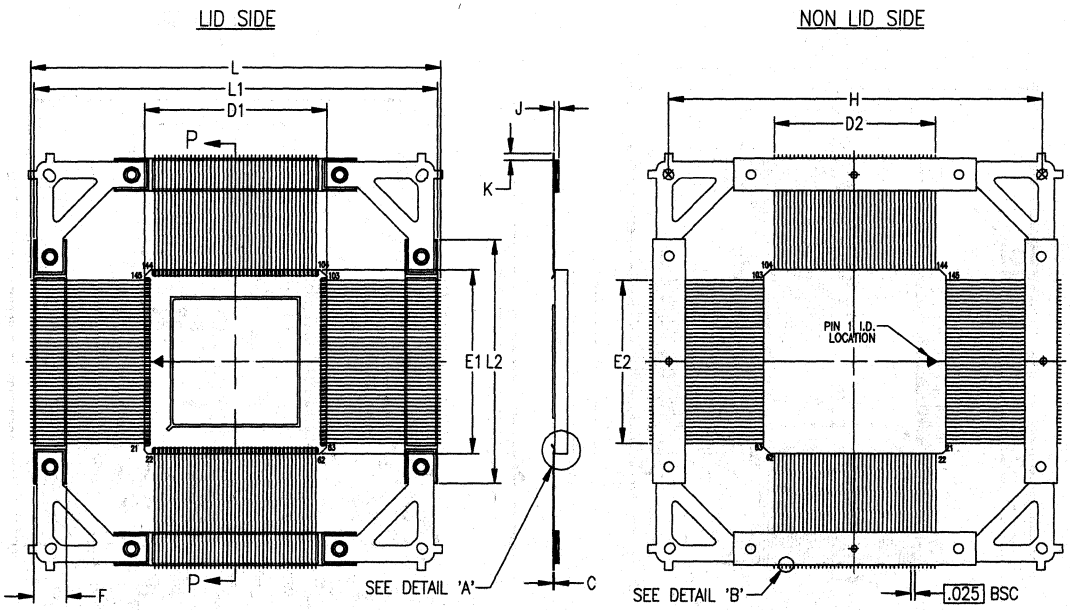


NOTES:

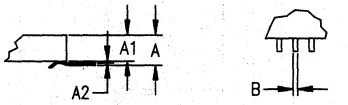
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "N" IS THE NUMBER OF TERMINALS.
3. PACKAGES ARE SHIPPED UNFORMED.
4. LEAD FINISH: GOLD (50 MICROINCHES MINIMUM) OVER NICKEL PER MIL–I–38535

SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A			.135
A1			.115
A2			.020
B	.006	.008	.012
C	.005	.006	.009
D1/E1	.740	.750	.765
D2/E2	.600 BSC		
F	.425	.450	.475
H	2.300 BSC		
J	.030	.035	.040
K			.020
L			2.580
L1	2.490	2.500	2.510
L2	1.480	1.500	1.520
N	100		

100–PIN CERAMIC BRAZED CQFP (CB100) (XC4000 VERSION)



SECTION P–P



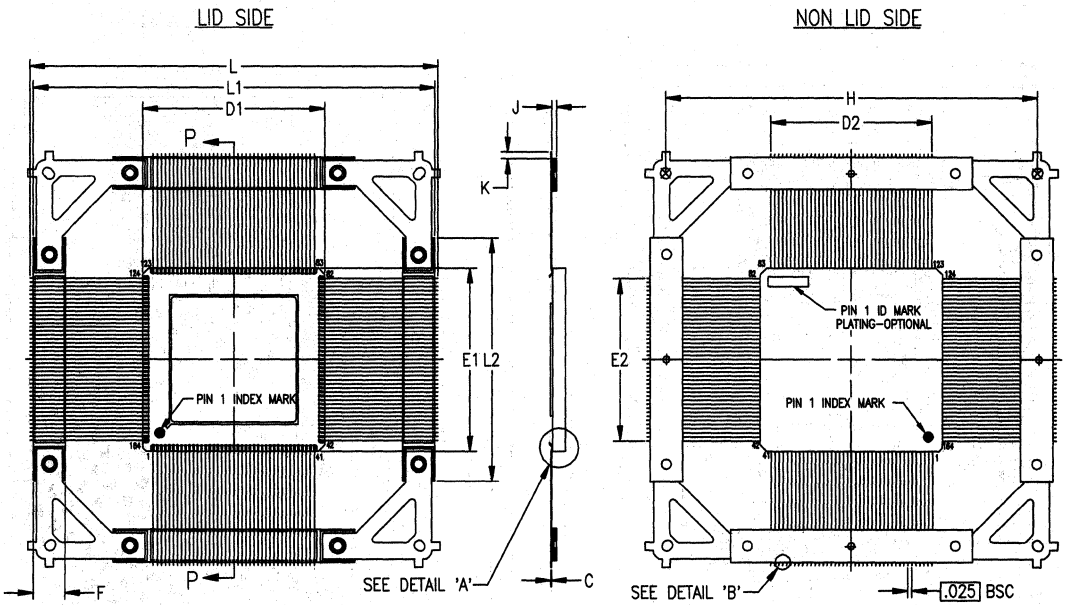
DETAIL 'A' DETAIL 'B'

SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A	---	---	.130
A1	---	---	.110
A2	---	---	.020
B	.007	---	.012
C	.005	.006	.009
D1/E1	1.120	1.130	1.145
D2/E2	1.000 BSC		
F	.175	.200	.225
H	2.300 BSC		
J	.030	.035	.040
K	---	---	.020
L	---	---	2.580
L1	2.485	2.500	2.505
L2	1.480	1.500	1.520
N	164		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "N" IS THE NUMBER OF TERMINALS.
3. PACKAGES ARE SHIPPED UNFORMED.
4. LEAD FINISH: GOLD (50 MICROINCHES MINIMUM) OVER NICKEL PER MIL–I–38535

164–PIN CERAMIC BRAZED CQFP (CB164) (XC3000 VERSION)

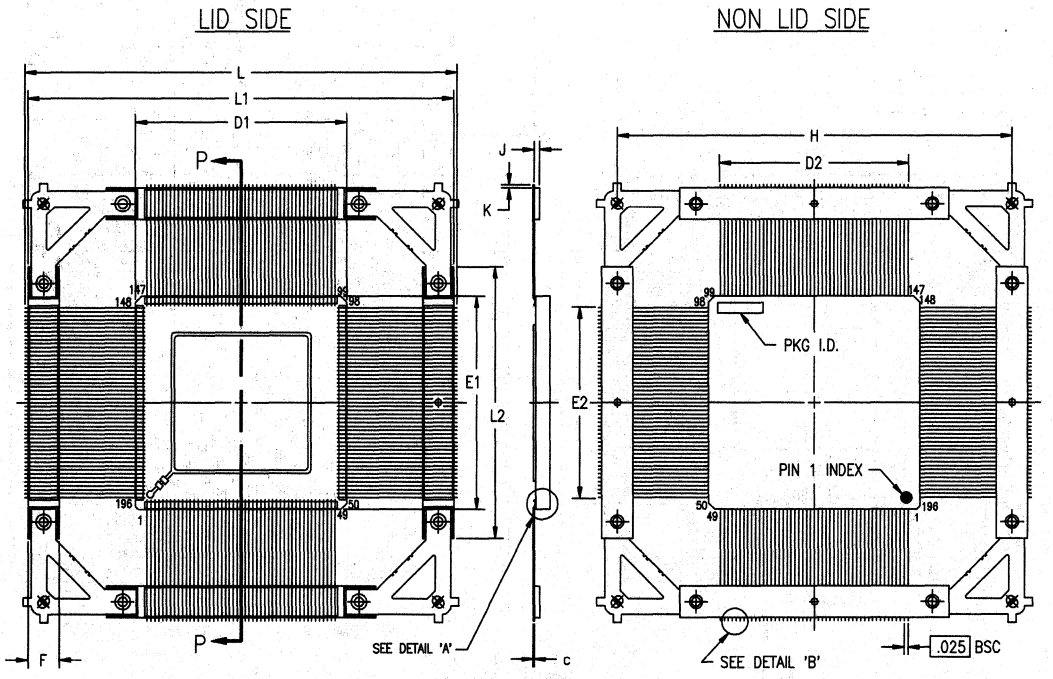


SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A			.130
A1			.110
A2			.020
B	.007		.012
C	.005	.006	.009
D1/E1	1.120	1.130	1.145
D2/E2	1.000 BSC		
F	.175	.200	.225
H	2.300 BSC		
J	.030	.035	.040
K			.020
L			2.580
L1	2.485	2.500	2.505
L2	1.480	1.500	1.520
N	164		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
2. SYMBOL "N" IS THE NUMBER OF TERMINALS.
3. PACKAGES ARE SHIPPED UNFORMED.
4. LEAD FINISH: GOLD (50 MICROINCHES MINIMUM) OVER NICKEL PER MIL-I-38535

164-PIN CERAMIC BRAZED CQFP (CB164)
(XC4000 VERSION)

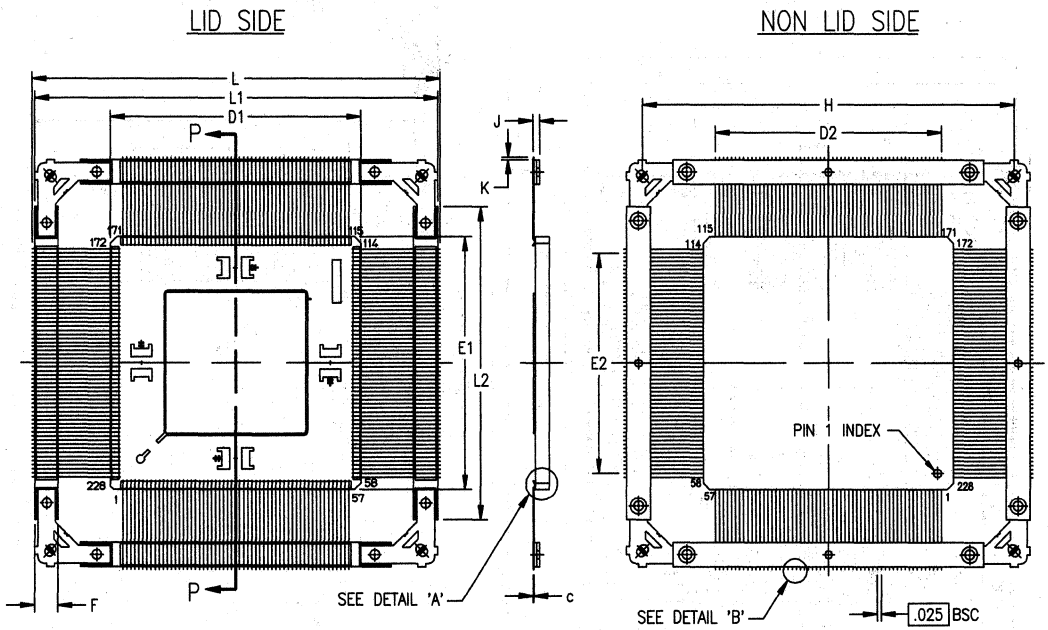


SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A			.130
A1	.081	.090	.105
A2			.020
B	.007		.012
C	.005	.006	.009
D1/E1	1.336	1.350	1.364
D2/E2	1.200 BSC		
F	.175	.200	.225
H	2.300 BSC		
J	.030	.035	.040
K			.020
L	2.500		2.580
L1	2.470	2.500	2.530
L2	1.700	1.720	1.740
N	196		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
2. SYMBOL "N" IS THE NUMBER OF TERMINALS.
3. PACKAGES ARE SHIPPED UNFORMED.
4. LEAD FINISH: GOLD (50 MICROINCHES MINIMUM) OVER NICKEL PER MIL-I-38535

196-PIN CERAMIC BRAZED CQFP (CB196)



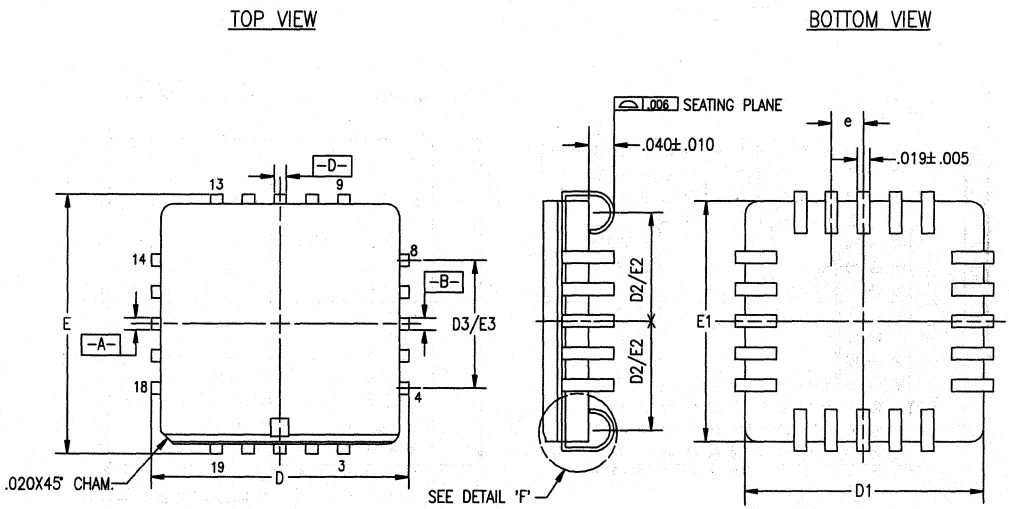
SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A	---	---	.130
A1	---	---	.110
A2	---	---	.020
B	.007	---	.012
C	.005	.006	.009
D1/E1	1.534	1.550	1.570
D2/E2	1.400 BSC		
F	.125	.150	.175
H	2.300 BSC		
J	.030	.035	.040
K	---	---	.020
L	---	---	2.580
L1	2.480	2.500	2.530
L2	1.900	1.920	1.940
N	228		

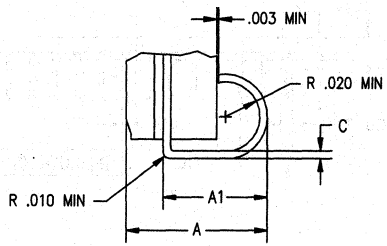
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "N" IS THE NUMBER OF TERMINALS.
3. PACKAGES ARE SHIPPED UNFORMED.
4. LEAD FINISH: GOLD (50 MICROINCHES MINIMUM) OVER NICKEL PER MIL–I–38535

228–PIN CERAMIC BRAZED CQFP (CB228)

CLCC Packages — CC20





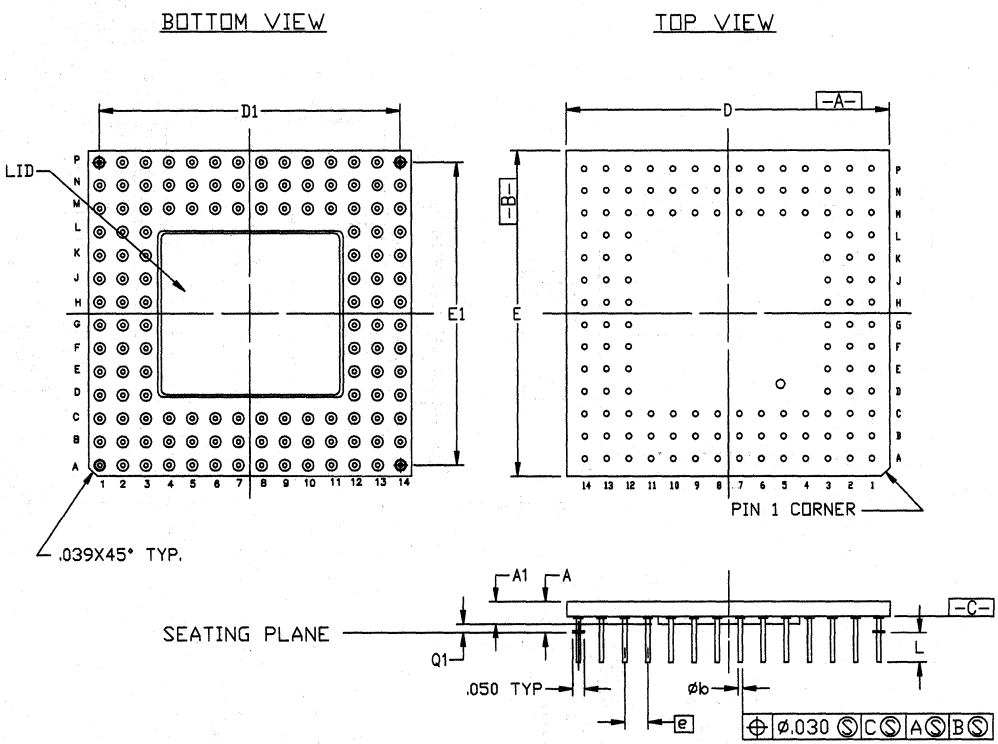
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. LEAD FINISH: SOLDER DIP
3. LEAD WIDTH DIMENSION INCLUDES LEAD TRIM OFFSET.
4. "N" IS THE NUMBER OF TERMINALS.

SYMBOL	INCHES		
	MIN	NOM	MAX
A	.140	.150	.155
A1	.080	.090	.100
C	.006	.007	.010
D/E	.395	.400	.405
D1/E1	.370	.375	.380
D2/E2	.145	.160	.175
D3/E3	.200 REF.		
e	.050 BSC		
N	20		

20–PIN CLCC (CC20)

Plastic PGA Packages — PP132, PP175



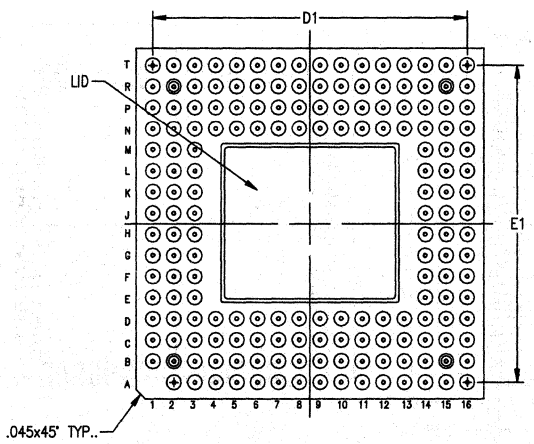
SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A			.165
A_1	.110	.120	.135
D/E	1.440	1.460	1.480
D_1/E_1	1.300 BSC		
L	.125		.150
Q_1	.025		.070
e	.100 BSC		
øb	.016	.018	.020
M	14		

NOTES:

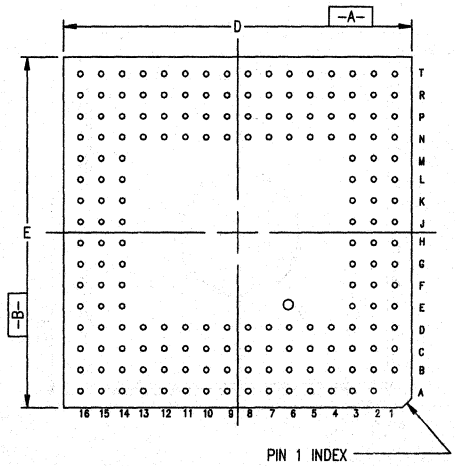
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–083–AF.
4. LEAD FINISH: SOLDER (90/10–Sn Pb) 50microinches MINIMUM COAT.

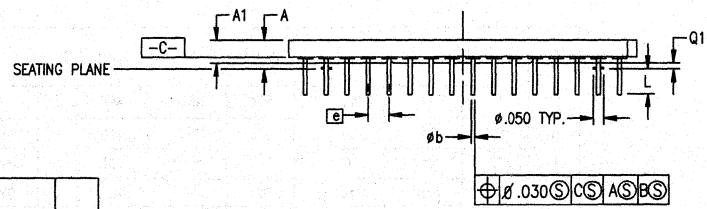
132–PIN PLASTIC PGA (PP132)

BOTTOM VIEW



TOP VIEW





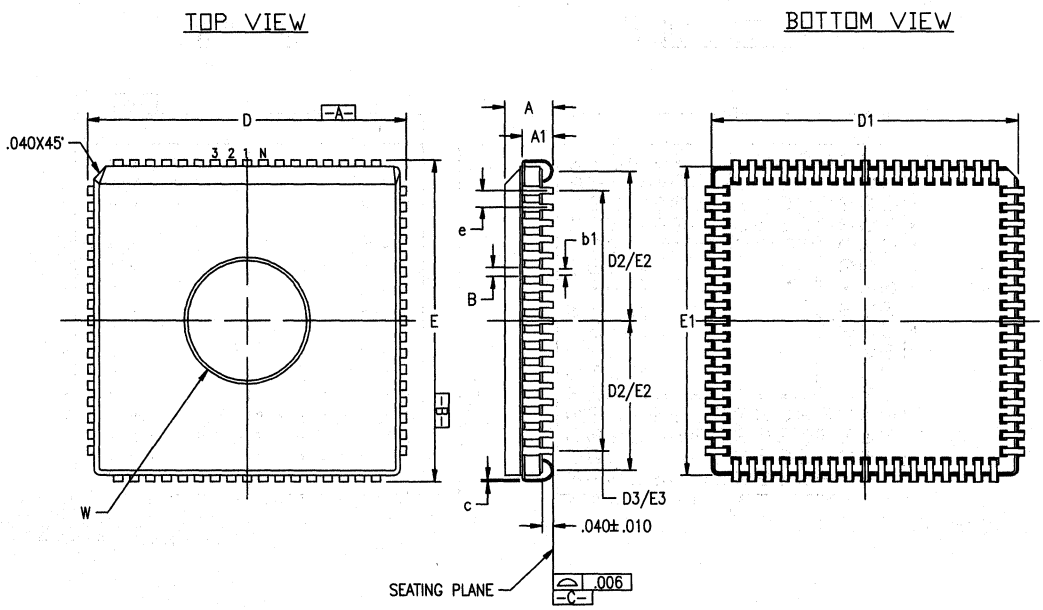
SYMBOL	INCHES			NOTE
	MIN.	NOM.	MAX.	
A			.165	
A_1	.110	.120	.135	
D/E	1.640	1.660	1.680	
D_1/E_1	1.500 BSC			
L	.125		.150	
Q_1	.025		.070	
e	.100 BSC			
øb	.016	.018	.020	
M	16			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–083–AH
4. LEAD FINISH: SOLDER (90/10–Sn Pb) 50microinches MINIMUM COAT.

175–PIN PLASTIC PGA (PP175)

Windowed CLCC Packages — WC44, WC68, WC84



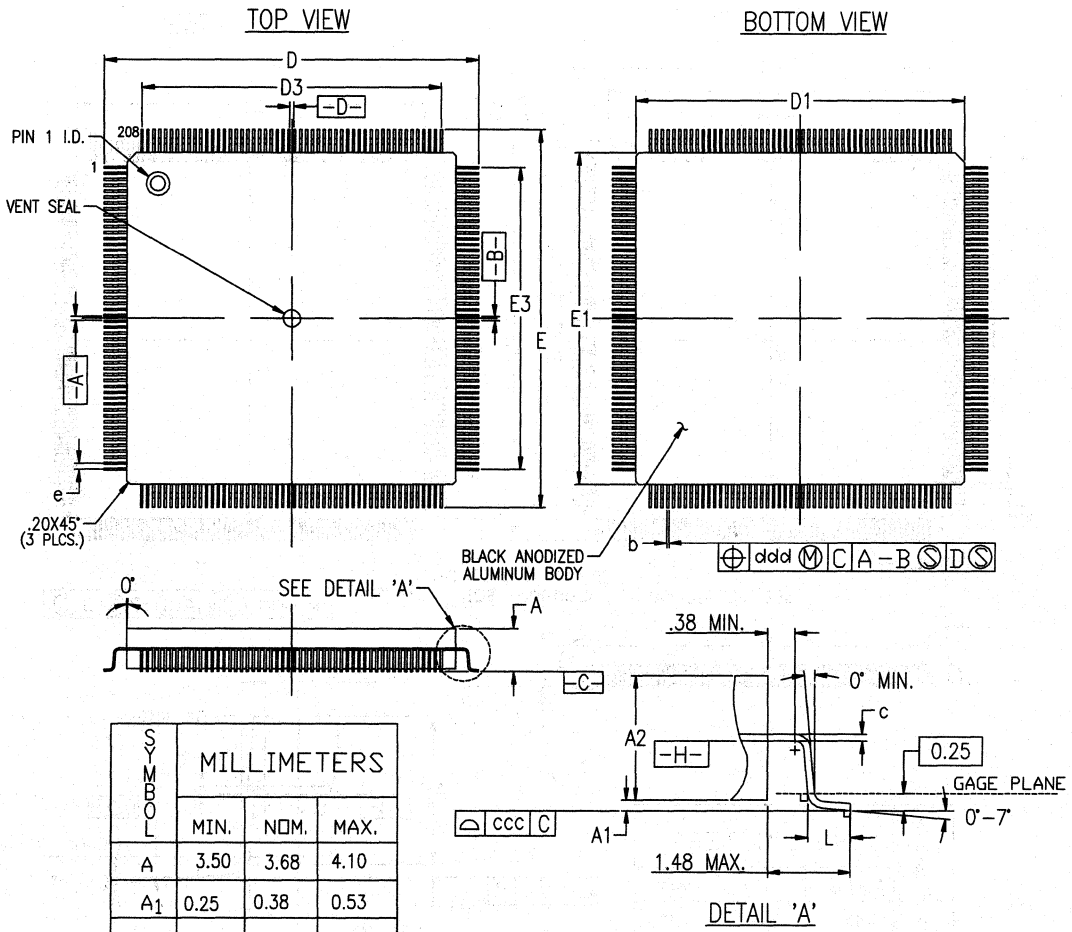
SYMBOL	DIMENSION IN INCHES								
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	.155	.172	.190	.155	.172	.190	.155	.172	.190
A1	.090	---	.120	.090	---	.120	.090	---	.120
B	.026	.028	.032	.026	.028	.032	.026	.028	.032
b1	.017	.019	.022	.017	.019	.022	.017	.019	.022
c	.006	.007	.012	.006	.007	.012	.006	.007	.012
D/E	.685	.690	.695	.985	.990	.995	1.185	1.190	1.195
D1/E1	.630	.650	.665	.930	.950	.965	1.130	1.150	1.165
D2/E2	.290	.305	.320	.440	.455	.470	.540	.555	.570
D3/E3	.500 REF.			.800 REF.			1.000 REF.		
e	.050 BSC			.050 BSC			.050 BSC		
N	44			68			84		
W	ø.350			ø.390 REF.			.450 SQ. REF		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. LEAD WIDTH DIMENSION INCLUDE LEAD TRIM OFFSET and LEAD FINISH, LEAD FINISH: (HOT SOLDER DIP)
3. SYMBOL 'N' IS THE NUMBER OF TERMINALS.
4. SYMBOL 'W' IS THE DIMENSION OF THE EPROM WINDOW.
5. THESE PACKAGES MEET DIMENSIONAL REQUIREMENTS OF JEDEC MO–087, VARIATIONS – AB(WC44); AD(WC68); AE(WC84).

44, 68, and 84–PIN WINDOWED CLCC (WC44, 68 and 84)

Metal Quad Packages — MQ208, MQ240

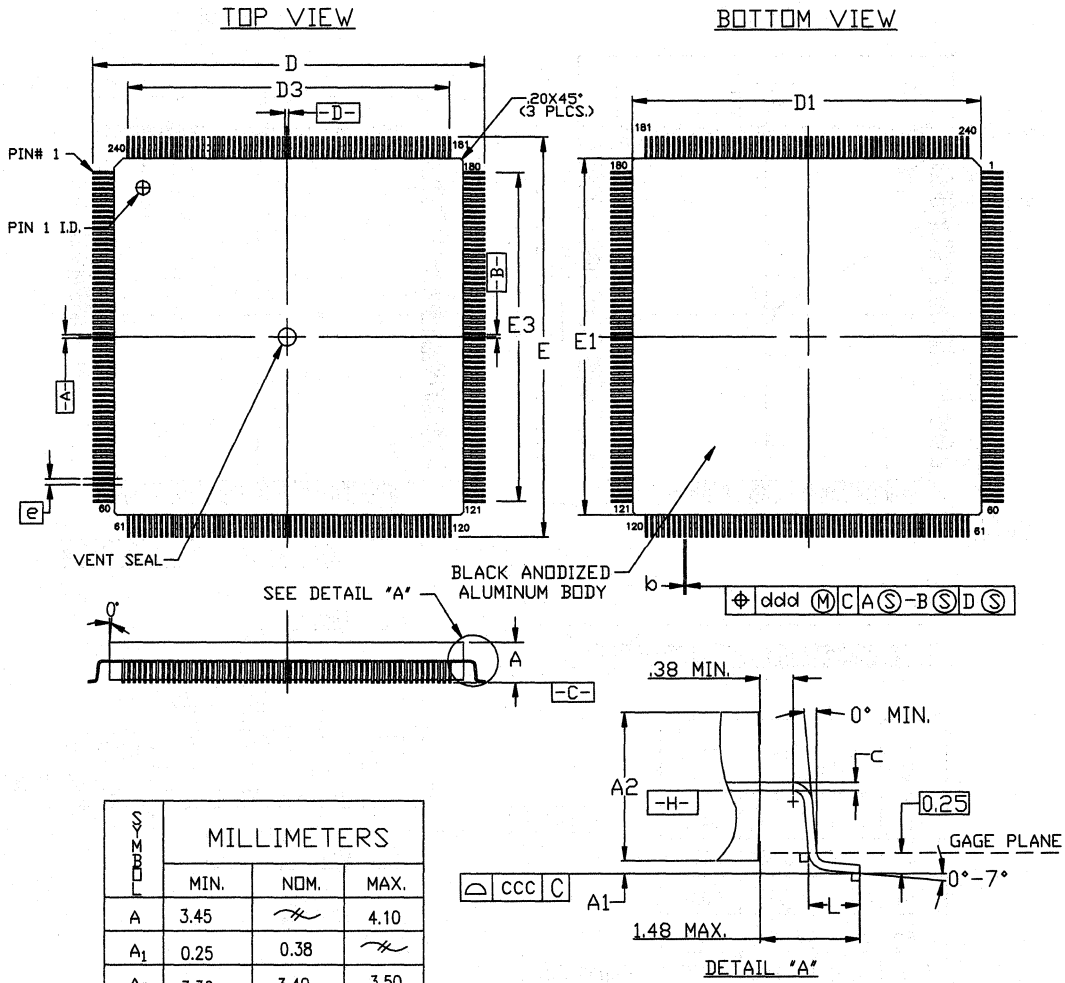


SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.50	3.68	4.10
A_1	0.25	0.38	0.53
A_2	3.20	3.40	3.60
D/E	30.35	30.60	30.85
D_1/E_1	27.58	27.64	27.79
D_3/E_3	25.50 REF.		
L	0.50	0.60	0.75
e	0.50 BSC.		
b	0.17	0.22	0.27
c	0.09	--	0.20
ccc	--	--	0.10
ddd	--	--	0.08

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE EPOXY PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT EXCEED 0.25mm ON EACH SIDE.
3. DRAWING CONFORMS TO JEDEC MO-143-FA1 EXCEPT BODY DIMENSIONS "D1/E1" and COPLANARITY.
4. LEAD FINISH: SOLDER PLATE

208-PIN METAL QUAD (MQ208)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.45		4.10
A_1	0.25	0.38	
A_2	3.30	3.40	3.50
b	0.17		0.27
c	0.09		0.20
D/E	34.35	34.60	34.85
D_1/E_1	31.59	31.64	31.79
D_3/E_3		29.50 REF.	
L	0.50	0.60	0.75
e		0.50 BSC.	
ddd		0.08	
ccc		0.10	

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE EPOXY PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT EXCEED 0.25mm ON EACH SIDE.
3. CONFORMS TO JEDEC MO-143-GA, EXCEPT IN BODY DIMENSIONS AND COPLANARITY.
4. LEAD FINISH: SOLDER PLATE

240-PIN METAL QUAD (MQ240)

XILINX®

Testing, Quality, and Reliability Table of Contents

Quality Assurance and Reliability

Quality Assurance Program

All aspects of the Quality Assurance Program at Xilinx have been designed to eliminate the root cause of defects, rather than to try to remove them by inspection. A quality system was put in place which is in full compliance with the requirements of ISO9002. Xilinx was found to be in full compliance of the requirements of ISO9002:1994 by an independent auditor in October, 1995. At that time Xilinx was registered for "the manufacturing and testing of programmable logic devices".

The aspects of ISO compliance in place at Xilinx include the following seventeen points:

- **Management Review:** a comprehensive system of management attention and direction for all aspects of company performance that directly affect our customers. These include (among others) Xilinx performance in the areas of Quality, Reliability and On-Time Delivery. Management assures that this quality policy is understood, implemented and maintained at all levels in the organization.
- **Quality Systems:** are in place to ensure that product conforms to customer specifications. These systems facilitate, measure and continuously improve Xilinx performance in those areas that affect customer satisfaction. Xilinx remains committed to achieving 100% customer satisfaction.
- **Contract Review:** is conducted to ensure each contract adequately defines and documents requirements, that differences between customer and Xilinx standard specifications are mutually satisfactorily resolved, and that Xilinx has the capability to meet contract requirements.
- **Document Control:** procedures are established and maintained to control all documents and data that relate to the performance of Xilinx business and processing requirements. All organizations who need access to such documentation during the performance of their functions are assured availability of the latest, controlled versions of that documentation.
- **Purchasing:** procedures are in place to ensure that all purchased products conform to the specified requirements. As Xilinx is a "fabless" manufacturing company, special attention is paid to our subcontract partners. They are required to demonstrate the type of control and capabilities that our customers require. All key Xilinx subcontract partners are ISO certified.
- **Product Identification & Traceability:** is maintained throughout the manufacturing process. Traceability back to the starting materials is available through unique product identification techniques and markings throughout the manufacturing process.
- **Process Control:** is assured by identifying and controlling those processes that directly affect the quality of our products, whether those processes are performed directly by Xilinx, or by our subcontract partners.
- **Inspection & Test**: is performed to ensure that incoming product is not used or processed until it has been verified as conforming to required specifications. This inspection is done jointly by Xilinx and by its subcontract partners.
- **Inspection, Measuring and Test Equipment:** is calibrated in conformance with the requirements of Mil Ref 45662 and/or other international standards. Equipment is maintained in such a manner to ensure that measurement uncertainty is known and is consistent with specification requirements.
- **Inspection & Test Status:** of product is uniquely identified throughout the manufacturing process both at Xilinx and at our subcontract partners. Records are kept to identify the authority responsible for the release of conforming production.
- **Control of Non-Conforming Product:** is assured through disposition procedures that are defined in such a manner as to prevent the shipping of non-conforming products. The responsibility and authority for the disposition of such products are well defined.
- **Corrective Action:** processes are documented and implemented to prevent the recurrence of nonconforming product. These processes are the key to implementing the Xilinx strategy of eliminating the root causes of nonconformity, rather that to apply inspection to try to remove nonconformity.
- **Handling, Storage, Packing & Delivery:** procedures are defined and implemented to prevent damage or deterioration of product once the manufacturing process is complete.
- **Quality Records:** procedures are established and maintained for the identification, collection, indexing, filing, storage, maintenance and disposition of quality records.
- **Internal Quality Audits:** are carried out to verify whether quality activities comply with planned arrangements and to determine the effectiveness of the quality system. These audits are regularly

supplemented by quality audits performed by our customers, and by our independent ISO auditors.

- **Training:** procedures have been established and are maintained to identify the training needs of all personnel affecting quality during the production of Xilinx products. Personnel performing such activities are qualified based upon appropriate education, training and/or experience.
- **Statistical Techniques:** are in place at Xilinx and at our subcontract partners for verifying the acceptability of process capabilities and product characteristics.

These key requirements are in place at Xilinx and at our subcontract partners to ensure our ability to achieve customer satisfaction through the **on-time delivery** of **quality products** that **meet customer requirements** and are **reliable**.

Device Reliability

Device reliability is often expressed in a measurement called *Failures in Time* (FITs). In this measure one FIT equals one failure per billion (10^9) device operating hours. A failure rate in FITS must include the operating temperature to be meaningful. Hence failure rates are often expressed in FITS at 70°C (or some other temperature in excess of the application).

Since one billion hours is well in excess of 100,000 years, the FIT rate of modern ICs can only be measured by accelerating the failure rate by testing at a higher junction temperature (usually 125°C or 145°C). Extensive testing of Xilinx devices (performed on actual production devices taken directly from finished goods) has been accomplished continuously since 1989 and reported quarterly. Quarterly reports on the reliability of Xilinx products are available through your Xilinx sales representative. During the last two years, over 20,000 devices have accumulated a total of over 36,000,000 hours of both static and dynamic operation at 125°C (equivalent) to yield the FIT rates shown in Figure 1.

Description of Tests

Die Qualification

1. **High Temperature Life**: This test is performed to evaluate the long-term reliability and life characteristics of the die. It is defined by the Military Standard from which it is derived as a "Die-Related Test" and is contained in the Group C Quality Conformance Tests. Because of the acceleration factor induced by higher temperatures, (typically 125°C and/or 145°C) data representing a large number of equivalent hours at a normal temperature of 25°C can be accumulated in a reasonable period of time.
2. **Biased Moisture Life**: This test is performed to evaluate the reliability of the die under conditions of long-term exposure to severe, high-moisture environments that could cause corrosion. Although it clearly stresses the package as well, this test is typically grouped under the die-related tests. The device is operated at maximum-rated voltage, 5.5 Vdc, and is exposed to a temperature of 85°C and a relative humidity of 85% throughout the test.

Package Integrity and Assembly Qualification

1. **Unbiased Pressure Pot**: This test is performed at a temperature of 121°C and a pressure of 2 atm of saturated steam to evaluate the ability of the plastic encapsulating material to resist water vapor. Moisture penetrating the package could induce corrosion of the bonding wires and nonglassivated metal areas of the die (bonding pads only for FPGA devices). Under extreme conditions, moisture could cause drive-in and corrosion under the glassivation. Although it is difficult to correlate this test to actual field conditions, it provides a well-established method for relative comparison of plastic packaging materials and assembly and molding techniques.

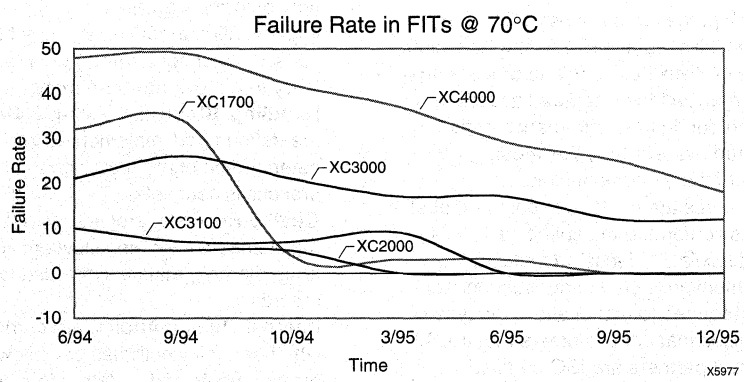


Figure 1: Failure Rates in FITs

2. **Thermal Shock**: This test is performed to evaluate the resistance of the package to cracking and resistance of the bonding wires and lead frame to separation or damage. It involves nearly instantaneous change in temperature from -65°C to +150°C (condition "C").
3. **Temperature Cycling**: This test is performed to evaluate the long-term resistance of the package to damage from alternating exposure to temperature extremes. The range of temperatures is -65°C to +150°C (condition "C"). The transition time is longer than that in the Thermal Shock test but the test is conducted for many more cycles.
4. **Salt Atmosphere**: This test was originally designed by the US Navy to evaluate resistance of military-grade ship-board electronics to corrosion from sea water. It is used more generally for non-hermetic industrial and commercial products as a test of corrosion resistance of the package marking and finish.
5. **Resistance to Solvents**: This test is performed to evaluate the integrity of the package marking during exposure to a variety of solvents. This is an especially important test, since an increasing number of board-level assemblies are subjected to severe conditions of automated cleaning before system assembly. This test is performed according to the methods specified by MIL-STD-883.
6. **Solderability**: This test is performed to evaluate the solderability of the leads under conditions of low soldering temperature following exposure to the aging effects of water vapor.
7. **Lead Fatigue**: This test is performed to evaluate the resistance of the completed assembly to vibrations during storage, shipping, and operation.

Testing Facilities

Xilinx has complete capability to perform High Temperature Life Testing, Thermal Shock, Temperature Cycling, Biased Moisture Life Test, Unbiased Pressure Pot, Solderability and Hermeticity, as well as complete Failure Analysis in house. Table 1 and Table 2 show typical qualification requirements for new and/or changed process flows. Table 3 is a list of current failure analysis capabilities. These laboratories are dedicated exclusively to increasing customer satisfaction through continuous improvements in our processes and technologies.

Table 1: Plastic Package/Product Qualification Requirements

							New Assy Techniques (Mat'l/Process/Method								
Test Seq	Test Description (note 1)	Acc# S.Size (note 2)	New Assy Plant	New Pkg Type I (note3)	New Pkg Type II (note4)	New Pkg Type III LF Design (note5)	Lead Frame	Die Attach	Die Coat	Wire Bond	Mold CLP	Lead Finish	New Device Mask (note6)	New Fab Proc	Full Qual
B1	* Phy. Dimension	0/5	X	X	X							X			X
B2	* Resist. to Solvents	0/3	X								X	X			X
B3	* Solderability Test (note 7)	0/5	X				X					X			X
B4	Solder Heat Test (Optn'l)	0/15				X	X				X				X
B5	Auto Clave (SPP)(Optn'l) 0/76	0/76	X	X	X	X	X		X		X		X		X
B6	* Ball Shear/Bond Pull (note 7)	0/5	X	X					X	X	X		X	X	X
B7	** X-Ray (note 7)	0/5	X	X	X	X			X	X	X		X		X
B8	* S.A.T/Dye Pen Test (note 7)	0/10	X	X	X	X	X				X	X			X
B9	* Adhesion of L/Finish (Optn'l)	0/3	X				X					X			X
B10	* External Visual (note 7)	0/25	X	X	X	X	X				X				X
B11	Internal Visual (note 7)	0/5	X	X	X		X	X	X	X			X	X	X
B12	* Die Shear (note 7)	0/5	X					X					X	X	X
B13	Flammability Test (note 7)	Per lot									X				X
C1-A	High Temp Life Test	0/76							X				X	X	X
C1-B	Low Temp Life Test (note 7)	0/22											X	X	X
C2	C2-A:HAST (0/22) or C2-B: 85/85	0/76	X	X		X	X	X	X		X			X	X
C3	ESD (HBM)	0/3											X	X	X
C4	High Temp Storage (Optn'l)	0/77									X		X	X	X
D1	* Lead Integrity	0/3	X	X	X							X			X
D2	Thermal Shock (Optn'l)	0/76													X
D3	Temp Cycle	0/76	X	X	X	X	X	X	X	X	X			X	X
E1	Electrical Test & Data Log	0/30											X	X	X
E2	Electrical Characterization	0/30											X	X	X
E3	T.D.D.B (note 7)	–											X	X	X
E4	Latch-up	0/9											X	X	X
E5	Electromigration (note 7)	–											X	X	X
E6	Photosensitivity (Optn'l)	0/11											X	X	X
E7	Data Retention Bake EPLD & EPR	0/22											X	X	X
E8	Input/Output Capacitance	0/5											X	X	X
E9	Power Cycling (Optn'l)	0/22											X	X	X
Qty required per lot		E.Good	239	238	162	248	248	157	314	86	325	0	393	464	636
		E.Reject	63	48	43	35	43	5	5	5	43	29	10	10	64
		Total	302	286	205	283	291	162	319	91	368	29	403	474	700

Notes:
1) Test method and stress conditions available upon request.
2) For any QUAL which does not meet the standard requirements, approval from Product Engineering and Product QA is required.
3) Any new package which has not been qualified in the qualified assembly facility.
4) Any new package where the same body size with different lead pitch has been qualified.
5) New leadframe design whereby the paddle size is larger than the existing leadframe paddle size used in the same qualified package.
6) For new mask from same device family, only high temp life test, ESD, Latch & Capacitance are required.
7) In-process monitor data may be used to satisfy this requirement.
*) Electrical rejects can be used as test sample.
**) This is a non-destructive test, sample can be re-used.

Table 2: Hermetic Package/Product Qualification Requirements (Commercial)

			New Assy Techniques (Mat'l/Process/Method												
Test Seq	Test Description (note 1)	Acc# S.Size (note 2)	New Assy Plant	New Pkg Family (note3)	New Pkg Qual Family (note4)	Lead Frame	Die Attach	Die Coat	Wire Bond	Type of Seal	Lead Finish	New Cavity Size (note6)	New Device (note6)	New Fab Proc	Full Qual
B1	Solder Heat Test (Optn'l)	0/15		X	X					X		X			X
B2	* Resist. to Solvents (note 7)	0/3	X	X							X				X
B3	* Solderability Test (note 7)	0/3	X	X		X					X				X
B4	* Die Shear/Stud Pull (note 7)	0/5	X	X	X		X						X	X	X
B5	* Bond Pull (note 7)	0/2	X	X	X	X		X	X				X	X	X
B6	* External Visual (note 7)	0/25	X	X	X	X			X		X				X
B7	Internal Visual (note 7)	0/5	X	X	X	X	X	X	X				X	X	X
C1-A	High Temp Life Test	0/76	X	X				X	X				X	X	X
C1-B	Low Temp Life Test (note 7)	0/22											X	X	X
C2	High Temp Storage (Optn'l)	0/77						X					X	X	X
C3	ESD (HBM)	0/3											X	X	X
D1	* Phy. Dimension	0/15	X	X	X						X	X		X	X
D2	* Lead Integrity	0/3	X	X	X	X					X			X	X
D3	Thermal Shock + Temp Cycl + Moisture Resistance	0/32	X	X	X	X	X	X	X	X	X	X	X	X	X
D4	Mech. Shock + Vibration + Constant Acceleration	0/32	X	X	X	X	X		X	X		X	X	X	X
D5	* Salt Atmosphere	0/15	X	X	X						X			X	X
D6	* Internal Vapor Content (note 7)	0/3	X	X	X		X	X		X		X		X	X
D7	* Adhesion of L/Finish (Optn'l)	0/2	X	X	X	X					X			X	X
D8	* Lid Torque	0/5	X	X	X					X		X		X	X
D9	Temp Cycle	0/45	X	X	X		X	X	X	X		X	X	X	X
E1	Electrical Test & Data Log	0/30											X	X	X
E2	Electrical Characterization	0/30											X	X	X
E3	T.D.D.B (note 7)	–											X	X	X
E4	Latch-up	0/9											X	X	X
E5	Electromigration (note 7)	–											X	X	X
E6	Photosensitivity (Optn'l)	0/11											X	X	X
E7	Data Retention Bake	0/22											X	X	X
E8	Input/Output Capacitance	0/5											X	X	X
Qty required per lot		E.Good	190	205	129	69	114	235	190	124	32	124	399	399	414
		E.Reject	81	81	75	50	8	5	2	33	41	48	7	50	81
		Total	271	286	204	119	122	240	192	157	73	172	406	449	495

Notes:
1) Test method and stress conditions available upon request.
2) For any QUAL which does not meet the standard requirements, approval from Product Engineering and Product QA is required.
3) Package Family - A set of package type with the same package, material, Package construction techniques, terminal pitch, lead shape, row spacing and with identical package assembly tech.
4) Package Type - A package with a unique case outline, configuration, material, piece parts and assembly process.
5) Application to new piece parts or leadframe where cavity size is larger than the largest cavity size for the same package.
6) For new mask from same device family, only high temp life test, ESP, Latch & Capacitance are required.
7) In-process monitor data may be used to satisfy this requirement, for Qual data, data from Assy. lot traveler maybe used.
*) Electrical rejects can be used as test samples

Table 3: Failure Analysis Equipment List

Item	Equipment	Vendor	Model Number
1	Scanning Electron Microscope	JEOL	JMS-6401F
2	Gold Sputter (SEM Sample Prep)	ANATECH	Hummer VIII
3	Energy Dispersive X-Ray	OXFORD INST.	LINK ISIS-L200C
4	F.I.B. - Focused Ion Beam Workstation	F.E.I.	FIB-600
5	Real-Time X-Ray Imaging System	FEIN FOCUS	FXS-100.10
6	Scanning Acoustic Microscopy	Sonix	Micro-Scan 4HF-200
7	Ball Shear Strength Tester	KELLER	MBS-200
8	XRF Lead Finish/Composition Measurement System	Twin City, Inc.	XRF-5500
9	Liquid Crystal Hot Spot Detection System/Kit, with 3 temp.	Technology Associates	P/N 4330
10	Emission Microscope for Multilayer Inspection (EMMI)	Hypervision	Visionary 2000
11	Curve Tracer	BID Services	
12	Metallurgical High Power Microscope	Scientific Instrument Company	see quote (various)
13	Stereozoom Low Power Microscope - video camera + monitor	Scientific Instrument Company	see quote (various)
14	Micro-Etcher System	TM Associates	
15	Viseco Camera Interface with High Power Microscope	Computer Modules	
16	Hermeticity Test System - Fine Leak - Gross Leak	BID Services	-Trio-tech 486 - Veeco MS-170
17	Die-Shear Tester	KELLER	see #7
18	Steam Aging System	Robotic Systems	ST2D
19	Solder Wave/Pot	Robotic Systems	RPS-202
20	Lead Fatigue Tester	B & G	004-012-00
21	Conventional Oven (C.D.A.)	BID Services	
22	Drill-bit to open MQUADS + Decapping vise		
23	Color Printer	Tektronic	Tektronic Phaser IISD
24	Stud Pull Tester	B & G	003-010-00
25	Work Benches		
26	Cabinets		
27	Facilities (Lab Area and Equipment Installation Costs)		
28	Tool Maker Microscope		
29	Flowhood & Rinse Station		
30	Precision X-Sectioning Equipment		
31	Plasma Etcher	March Instruments	CS-1701
32	E-Beam IDS-3000		

Data Integrity

Memory Cell Design in the FPGA Device

An important aspect of SRAM-based FPGA device reliability is the robustness of the static memory cells used to store the configuration program.

The basic cell is a single-ended 5-transistor memory element (Figure 2). By eliminating a sixth transistor, which would have been used as a pass transistor for the complementary bit line, a higher circuit density is achieved. During normal operation, the outputs of these cells are fixed, since they determine the user configuration. Write and readback times, which have no relation to the device performance during normal operation, will be slower without the extra transistor. In return, the user receives more functionality per unit area.

This explains the basic cell, but how is the FPGA user assured of high data integrity in a noisy environment? Consider three different situations: normal operation, a Write operation and a Read operation. In the normal operation, the data in the basic memory element is not changed. Since the two circularly linked inverters that hold the data are physically adjacent, supply transients result in only small relative differences in voltages. Each inverter is truly a complementary pair of transistors. Therefore, whether the output is High or Low, a low-impedance path exists to the supply rail, resulting in extremely high noise immunity. Power supply or ground transients of several volts have no effect on stored data.

The transistor driving the bit line has been carefully designed so that whenever the data to be written is opposite the data stored, it can easily override the output of the feedback inverter. The reliability of the Write operation is guaranteed within the tolerances of the manufacturing process.

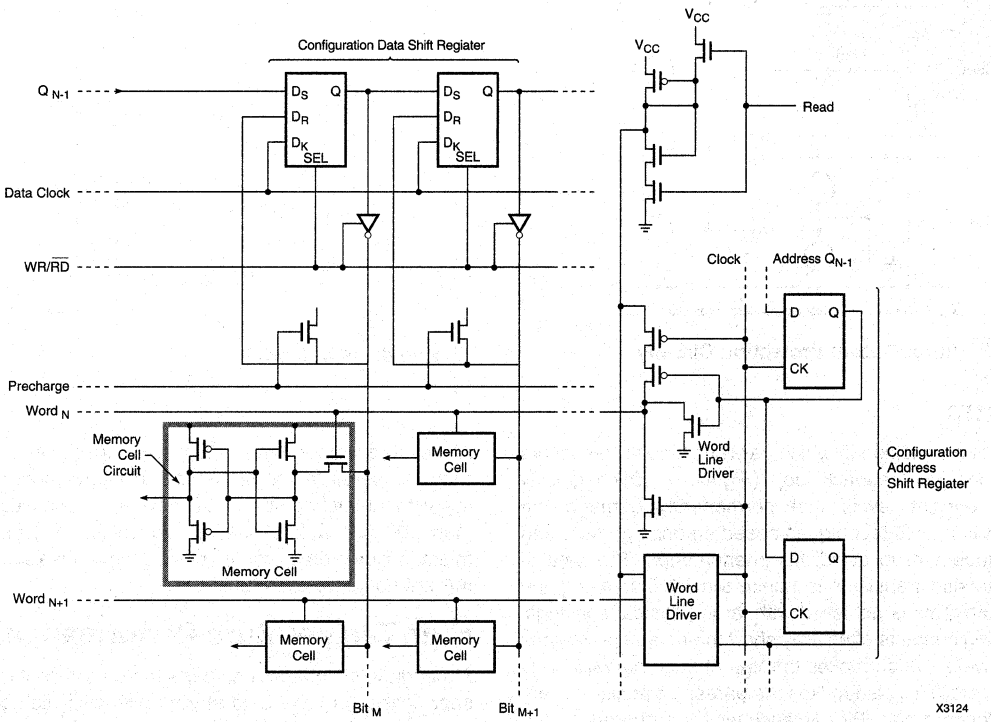


Figure 2: Configuration Memory Cell

In the Read mode, the bit line, which has a significant amount of parasitic capacitance, is precharged to a logic one. The pass transistor is then enabled by driving the word line High. If the stored value is a zero, the line is then discharged to ground. Reliable reading of the memory cell is achieved by reducing the word line High level during reading to a level that insures that the cell will not be disturbed.

Electrostatic Discharge

Electrostatic-discharge (ESD) protection for each pad is provided by circuitry that uses distributed transistors and/or diodes, represented by the circles in Figure 3. In older devices, these protection circuits are conventional diffused structures. In newer designs, Xilinx utilizes proprietary device structures which exhibit substantially enhanced ESD performance (see Table 4).

Whenever the voltage on a pad approaches a dangerous level, current flows through the protective structures to or from a power supply rail (V_{CC} or ground). In addition, the capacitances in these structures integrate the pulse to provide sufficient time for the protection networks to clamp the input, avoiding damage to the circuit being protected. Geometries and doping levels are chosen to provide ESD protection on all pads for both positive and negative voltages.

Table 4: ESD Performance of Xilinx Components

Circuit Family	Human Body Model 883D Method 3015	Machine Model EIAJ Method 20	Charged Device Model CDM
XC1700D	>6,000 V	800 V – 900 V	>2,000 V
XC2000	2,000 V – 2,500 V	250 V – 280 V	
XC3000A	3,000 V – 8,000 V	600 V – 700 V	>2,000 V
XC3100	2,500 V – 3,500 V	600 V – 700 V	
XC4000	4,000 V – 9,000 V	800 V – 900 V	>2,000 V
XC4000E	4,000 V– 5,000 V	600 V– 900 V	>2,000 V
XC5200	3,000 V– 5,000 V	tbd	
XC7000	2,000 V– 4,000 V	250 V– 300 V	>2,000 V

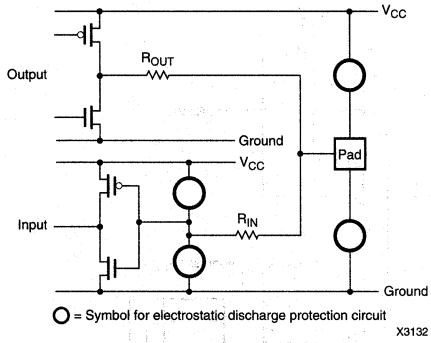


Figure 3: Input/Output Protection Circuity

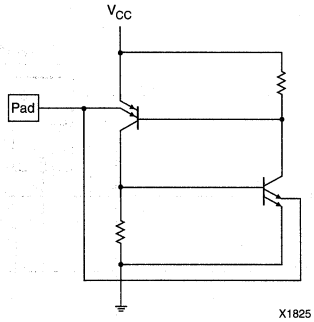


Figure 4: SCR Model

Latchup

Latchup is a condition in which parasitic bipolar transistors form a positive feedback loop (Figure 4), which quickly reaches current levels that permanently damage the device. Xilinx uses techniques based on doping levels and circuit placement to avoid this phenomenon. The beta of each parasitic transistor is minimized by increasing the base width. This is achieved with large physical spacings. The butting contacts effectively short the n+ and p+ regions for both wells, which makes the V_{BE} of each parasitic very close to zero. This also makes the parasitic transistors very hard to forward bias. Finally, each well is surrounded by a dummy collector, which forces the V_{CE} of each parasitic almost to zero and creates a structure in which the base width of each parasitic is large, thus making latchup extremely difficult to induce.

At elevated temperatures, 100 mA will not cause latchup. At room temperature, the FPGA can withstand more than 300 mA without latchup; the EPLD device can withstand more than 200 mA without latchup. However, to avoid metal-migration problems, continuous currents in excess of 10 mA are not recommended.

High Temperature Performance

Although Xilinx guarantees parts to perform only within the specifications of the data sheet, extensive high temperature life testing has been done at 145°C with excellent results.

Technical Support

Technical Support

June 1, 1996 (Version 1.0)

A complete and uniquely accessible offering of worldwide technical support services is available to Xilinx users.

Xilinx Field Application Engineers, located at sales offices and technical support centers worldwide, provide local engineering support, including design evaluation of new projects, close consultation throughout the design process, special training assignments, and new product presentations. Because their role as advisors and troubleshooters keeps them constantly on the go, they are best used, not for general questions, but for more targeted queries such as those related to architectural recommendations. The worldwide network of Xilinx sales representatives and distributors also provide local technical support for Xilinx users.

More general queries can be directed to the telephone "hotlines". Permanent teams of expert Technical Support Engineers located in the United States, United Kingdom, France, Germany, and Japan can handle problems and answer questions right on the spot, ensuring that the design process keeps moving forward.

In addition, Xilinx has several automated services, collectively referred to as X-TALX, to provide answers to user's queries 24 hours a day. These include a world wide web site, E-mail server, automated FAX system, bulletin board system, and special interest E-mail groups.

Many different publications assist users in completing designs quickly and efficiently, including technical manuals, data sheets, the AppLINX CD-ROM (a regularly-updated collection of the latest application notes and design hints), and the quarterly XCell newsletter.

For more in-depth support and instruction, a dedicated training organization conducts technical training classes worldwide. Courses geared for both novice and experienced users are available.

The following Technical Support Services are discussed in more detail in this chapter:

- Technical Support Hotline
- X-TALX: The Xilinx Network of Electronic Services
  - WebLINX World Wide Web Site
  - XDOCs E-mail document server
  - XFACTS document server
  - Xilinx Technical Bulletin Board Service
- Technical Literature
- AppLINX CD-ROM
- XCELL newsletter
- Training Courses

Technical Support Hotlines

The technical support hotlines give Xilinx users direct telephone access to Xilinx Technical Support Engineers worldwide, providing a quick resolution to any problem that occurs during the design process. Technical questions also may be submitted via FAX or E-mail.

Hotline Support, U.S.

Customer Support Hotline	800-255-7778 Hrs: 8:00 a.m. - 5:00 p.m. Pacific time
Customer Support Fax Number	408-879-4442 Avail: 24 hrs/day-7 days/week
E-mail Address	hotline@xilinx.com
Electronic Technical Bulletin Board	408-559-9327
Customer Service (Call for software updates, authorization codes, documentation updates, etc.)	408-559-7778, Ask for customer service

Hotline Support, Japan

telephone: (81) 3-3297-9163
fax: (81) 3-3297-0067
e-mail: jhotline@xilinx.com

Hotline Support, Europe

UK, London Office

telephone: (44) 1932 820821
fax: (44) 1932 828522
Bulletin Board Service: (44) 1932 333540
e-mail: ukhelp@xilinx.com

France, Paris Office

telephone: (33) 1 3463 0100
fax: (33) 1 3463 0959
e-mail: frhelp@xilinx.com

Germany, Munich Office

telephone: (49) 89 991 54930
fax: (49) 89 904 4748
e-mail: dlhelp@xilinx.com

X-TALX: The Xilinx Network of Electronic Services

WebLINX World Wide Web Site (www.xilinx.com)

Our World Wide Web site provides access to current information, including product data sheets, application notes, press releases, financial status, employment opportunities, and an on-line technical support database. *Smart*Search™, our industry-wide search engine, is the definitive resource for programmable logic information. *Smart*Search™ Agents will watch the Web for you and inform you, via e-mail, when new or updated information is found. An FTP site also is available to facilitate the quick and easy transfer of design and data files (ftp.xilinx.com).

XDOCs E-mail Document Server

The XDOCS E-mail system provides 24-hour a day, 7 days a week access to the same database that the Technical Support Engineers use. This database is updated regularly with information on bugs, workarounds, and helpful hints. Via E-mail, users can search for a specific record, or supply keywords to trigger a search of the database; XDOCS will send the requested information by return E-mail. Automated updates also can be sent on a periodic basis notifying users of new additions to the system. To subscribe to XDOCS, send an E-mail to xdocs@xilinx.com with "help" as the only word in the subject header.

XFACTS Document Server

The XFACTS automated FAX system provides the same information as XDOCS, but uses a phone/FAX interface instead of E-mail. Using a touch-tone telephone, users can request documents that are sent to their FAX machine. Located in San Jose, California, the XFACTS system can be reached at 408-879-4400.

Xilinx Technical Bulletin Board Service (408) 559-9327

To provide users with up-to-date information and software support, Xilinx provides a 24-hour electronic bulletin board system (BBS). The Xilinx Technical Support BBS is available to all registered Xilinx development system users. Users with full privileges can browse files on the bulletin board, download those of interest, or upload files to Technical Support Engineers.

All BBS files can be accessed through the Xilinx Web and FTP locations.

New bulletin board users must answer a questionnaire when they first access the BBS. After answering the questionnaire, callers can browse through the file areas or upload files. A caller with a valid XACT protection key or valid host ID will be given full user privileges within 24 hours.

The software and hardware requirements for accessing the BBS are as follows:

Baud Rate	28.8K or less bps
Character Format	8 data bits, no parity, 1 stop bit
Transfer Protocols	ASCII, Xmodem, Ymodem, Zmodem

The Xilinx Technical Support BBS is a menu-driven system. To choose a menu command, simply type the highlighted first letter of the command. Most commands are "hot keys" and do not require you to press the return key. Here is a quick description of the available menu commands:

Main

U)pload	Upload a file to the Technical Support group.
D)ownload	Download a file. This assumes you already know the filename, otherwise select the File Manager.
F)ile Manager	Takes you to the File Manager menu. This menu is for locating files.
S)ystem Folder	Takes you to the System menu. This menu is for changing your password, display options, etc.

File Manager

F)lag	Flag files for download.
L)ocate Files	Use wildcards to search for files.
N)ew Files	Lists recently added files.
Z)ippy DIR scan	Searches for text in file descriptions.
#'s	Chooses a file area to browse.

System

M)ode of display	Toggles between text and graphics display
P)age length	Changes the number of printed lines between "More?" prompts.
T)ransfer Protocol	Changes the default transfer protocol.
V)iew Settings	Shows current settings and user information.
W)rite User Info	Changes current user settings.

E-mail addresses for questions related to specific applications

Digital Signal Processing applications	dsp@xilinx.com
PCI-bus applications	pci@xilinx.com
Plug and Play ISA applications	PnP@xilinx.com
PCMCIA card applications	pcmcia@xilinx.com
Asynchronous Transfer Mode applications	atm@xilinx.com
Reconfigurable Computing applications	reconfig@xilinx.com

Technical Support E-mail addresses

hotline@xilinx.com	USA, Xilinx Headquarters
ukhelp@xilinx.com	United Kingdom
frhelp@xilinx.com	France
dlhelp@xilinx.com	Germany
jhotline@xilinx.com	Japan

Technical Literature

Xilinx offers many different publications to assist users in completing designs quickly and efficiently. These include technical manuals, Data Books, data sheets, application notes, AppLINX CD, and the XCELL newsletter. Many of these publications are available on-line at the Xilinx WebLINX World Wide Web site.

As part of the development system products, Xilinx provides manuals and supporting documents for the development system tools, libraries, CAE tool interfaces, and related software tools. Many of these manuals are available on the CD that holds the software as well as hardcopy format. On-line help facilities also are an integral part of the development system products.

AppLINX

AppLINX is a collection of current application notes and other new technical documentation provided on a CD-ROM for easy reference by the design engineer. All the material on the CD is provided in Adobe Acrobat format for easy viewing and printing. The AppLINX CD is updated regularly as new material becomes available.

XCELL Newsletter

XCELL, the quarterly journal for Xilinx programmable logic users, is dedicated to supplying up-to-date information for system designers. A typical issue includes descriptions of new products, updates on component and software availability and revision levels, application ideas, design hints and techniques, and answers to frequently-asked questions.

To add your name to the XCELL subscription list, please send your name, company affiliation, and mailing address to Brad Fawcett, XCELL editor, via FAX at 408-879-4676 or via e-mail sent to brad.fawcett@xilinx.com.

Programmable Logic Training Courses

All users of Xilinx products should attend one of our Training Courses. Attending a Xilinx Training Course is one of the fastest and most efficient ways to learn how to design with FPGA or CPLD devices from Xilinx. Hands-on expert instruction with the latest information and software will allow you to implement your own designs in less time with more effective use of the devices.

Xilinx offers a variety of classes to meet your specific needs. Training centers around the world schedule classes on a regular basis, and the classes can even be brought to your own facility.

What You Will Learn

Not only will you learn about our products, but we will recommend the best ways to use the software based on our years of experience with thousands of designs. You will learn how to efficiently enter, implement, and verify your design. The powerful yet easy-to-use Xilinx development system allows you to utilize the Xilinx automatic mode, or take a power-user approach and direct the automatic tools to the best implementation of your design.

Prerequisites

Students need only have a background in digital logic design. Basic familiarity with the PC or workstation is helpful but not required. It will benefit you to learn your design entry tool of choice before attending the Xilinx class, including an HDL language for the synthesis-based classes. Update or Advanced classes require previous experience with the Xilinx products.

Benefits

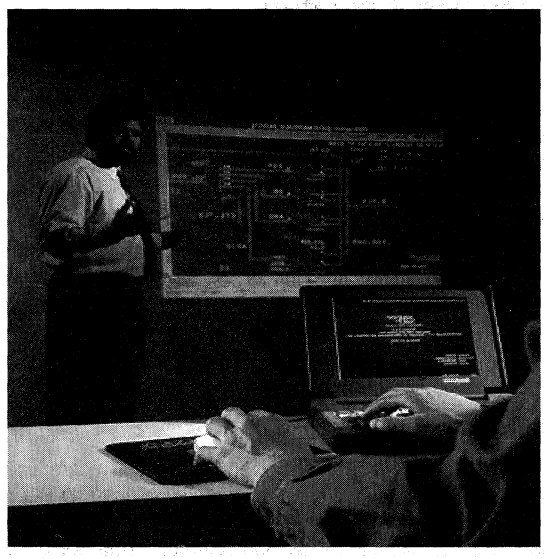
- Start or Complete Your Design During the Class
- Reduce Your Learning Time
- Make Fewer Design Iterations
- Get to Market Faster
- Lower Production Costs
- Increase Quality

The Training Classes

Xilinx offers classes for both schematic entry users and synthesis users, and both new and experienced users. All Xilinx classes focus on the Xilinx products, independent of the specific design entry tool.

Hands-On Experience

Each class includes over two hours each day for hands-on labs. There is at least one computer for every two people in the class.



Instructors

Xilinx Training Courses have been successfully held worldwide for over six years. The instructors are Xilinx experts who are skilled at passing that knowledge on to fellow engineers. A dedicated Training organization at Xilinx works closely with the Applications and Engineering groups to keep the classes up-to-date with the latest improvements and recommendations for Xilinx and third-party tools.

Course Materials

All course materials are supplied by Xilinx. Every student gets an excellent reference tool in the form of course notes, that include all the material presented during the class. The course notes are bound for easy use and include additional reference material beyond what is covered in the class.

Product Coverage

Xilinx classes will cover the latest released versions of our devices and development systems. While all available products are covered, emphasis is placed on the more popular and/or recommended solutions. New products are added to the class as they become available.

Schematic-Based Course Outline

The schematic-based Xilinx Training Class lasts three days. All North American training sites, and most international locations, teach the same class.

- Introduction
  - Development System Overview
  - Architecture Overview
- Xilinx Design Flow
  - Schematic Entry Guidelines
  - Design Manager
  - Flow Engine Automatic Translation
- Timing Specification
  - XACT-Performance Delay Specification
  - Static Timing Analyzer
- Designing for Xilinx FPGAs
  - Combinatorial Logic
  - Registered Logic
  - Memory Design
  - I/O Design
  - X-BLOX Module Generation
- Designing for Xilinx CPLDs
- Text Entry Guidelines
  - Xilinx-ABEL software
- Floorplanning
  - Incremental Design
  - XACT-Floorplanner
  - Relationally-Placed Macros
- Timing Analysis
  - Good Design Practices
  - Simulation Guidelines
- Configuration
  - Programming Modes
  - Bitstream Generator
  - PROM File Formatter
  - Hardware Debugger Download & Readback

Synthesis-Based Classes

Designing with high-level languages (VHDL and Verilog) and synthesis tools can be very different from using schematic entry. As a result, Xilinx offers classes that focus on VHDL and Verilog design entry for Xilinx products. Xilinx highly recommends the synthesis-based class for anyone using VHDL or Verilog for design entry. Synthesis-based classes include the following additional topics, using HDL code for design entry:

- Good coding styles
- Hierarchy within synthesis
- Synthesis design flow
- Controlling Xilinx implementation tools with synthesis

Synthesis-Based Course Outline

The following is a complete outline of the three-day synthesis-based class:

- Introduction
- FPGA Architecture
- Xilinx-Synopsys Design Flow
  - Good Coding Styles
  - Synopsys Scripts
  - Design Manager
  - Automatic Translation
- Timing Specification
  - XACT-Performance Delay Specification
  - Static Timing Analyzer
- Simulation Guidelines
- Good Design Practices
- Coding for Xilinx FPGAs
  - Combinatorial Logic
  - Carry Logic and X-BLOX Module Generation
  - Registered Logic
  - I/O Design
  - Memory Design
- Hierarchy
- Floorplanning
  - Incremental Design
  - XACT-Floorplanner
- Configuration
  - Programming Modes
  - Bitstream Generator
  - PROM File Formatter
  - XChecker Download & Readback

Update and Advanced Training Classes

If you have already attended a Xilinx class or have experience using Xilinx products, consider attending a one-day Update or Advanced Training session. These sessions will be most useful if you have the latest software.

Update Classes

One-day Update classes focus on the latest released products from Xilinx, describing them in relation to previous versions. For example, an Update class is available describing the new features in XACT*step* 6.0. The class will be offered for a limited time at regional sites, or can be brought to your facility. Browse the Xilinx web site (www.xilinx.com) for the latest information regarding special Update classes on new products from Xilinx.

Advanced Training Classes

If you have already attended a Xilinx class or have experience using Xilinx products, consider attending a one-day Advanced Training session. Advanced Training classes are offered at no charge to current in-warranty Xilinx customers; otherwise tuition is $200. Advanced Training sessions can vary according to the interests of the students. Popular topics include:

- Example Logic Design Techniques
- Timing Analysis and Avoiding Timing Hazards
- Design Methodology for Tough Designs
- Details of Advanced Optimization Capabilities
- XACT Design Editor
- Floorplanning

Advanced Training classes are held regularly at Xilinx headquarters, and sometimes at regional locations, but are replaced by Update Classes when appropriate. See the web site (www.xilinx.com) for scheduled classes, or contact Xilinx Training to hold an Advanced Training session at your site.

Training Locations

Xilinx Headquarters

Classes are held regularly at Xilinx headquarters in San Jose, California. During the class, you may elect to meet one-on-one with Xilinx Applications engineers to discuss specific issues not covered in the class. Topics may include using a specific third-party tool, optimizing your particular design, or more advanced issues beyond the coverage of the class.

North American Distributor Locations

Xilinx distributors sponsor training classes jointly with Xilinx, using the same material as the headquarters classes. Since the distributor sponsors the class, the tuition cost is often reduced to $495 for customers of the sponsoring distributor. Check with the distributor when registering. Locations include over fifty cities across North America.

International Locations

Xilinx classes are held throughout Europe, Asia, India, Israel, South Africa, Australia, South America, and other international locations. Classes vary in length and tuition, but are based on the same material used in North America. Contact your local Xilinx sales office or representative for classes in your area.

Customer-Site Classes

Xilinx can bring a Training Course to your own facility for the greatest convenience to your company.

On-Site Classes Provide Additional Benefits:

No Travel Costs

On-site Xilinx training classes eliminate travel time and expenses:

- No airfare
- No hotel bills
- No car rental

Classes Tailored To Your Needs

On-site classes can be tailored to meet the specific needs of your company:

- Convenient class time and location
- Projects of a proprietary nature can be discussed openly
- Students can use their own equipment and begin an actual design right in class

Costs: North America

Prices start at $4,500 for a minimum class size of six students.

Costs: International

- Prices vary; contact your local Xilinx sales representative.

Included in class fees:

- A Xilinx-certified instructor
- Training materials for each student
- PC for every two students (or if you prefer, the training labs can be done on your PCs or workstations)

Scheduling a Class

To schedule a training class at your facility and determine pricing, call the Xilinx sales office nearest you, or your local Xilinx sales representative. On-site training classes are popular, so the more advanced notice we have, the better our ability to schedule your class exactly when you want it.

Registration

Tuition

Class tuition in North America is $1,000 per student for the three-day classes, including the synthesis-based and workstation-based classes at Xilinx headquarters. The distributor-sponsored, schematic-based classes are offered at a reduced rate of $495 for customers of the sponsoring distributor. On-site classes start at $4500 per class, and vary according to the class and the number of students. For international locations, call the local registrar for pricing.

Most classes include a full lunch, with morning and afternoon snacks. Let the registrar know if you have any special dietary needs when registering for the class.

Money-back Guarantee

We are so confident you will be satisfied with the benefits of a Xilinx training class that we offer the following guarantee:

Full refund of the class cost if you are not completely satisfied.

Enrollment

To enroll, call the registrar for the location where you would like to attend a class. Or you may call the Training Registrar at Xilinx headquarters at (800) 231-3386 or contact your local sales office. You may also register on-line at www.xilinx.com.

Xilinx Training Registrar

Training Registrar
Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: (800) 231-3386 x1
Fax: (408) 879-4676, attn: Customer Training Registrar
E-mail: customer.training@xilinx.com
Register on-line: www.xilinx.com

Location		Tuition	Benefits
North America	Xilinx Headquarters	$1,000	• Can meet with applications engineers • Classes held frequently • All class types available
	Distributor Locations	$495	• Lower cost for distributor's customers • Local
	Customer Site	Starts at $4,500	• Convenience; can focus on specific issues
	Update	Typically $100	• One day, focus on new products
	Advanced	Free	• For experienced, in-warranty users
International	International Locations	Varies	• Offered in over 21 countries • Native language
	Customer Site	Varies	• Convenience • Can focus on specific issues

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XILINX®

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Choosing a Xilinx Product Family

August 6, 1996 (Version 1.1)

Application Note By PETER ALFKE

Summary

This Application Note describes the various Xilinx product families. Differences between the families are highlighted. The focus of the discussion is how to choose the appropriate family for a particular application.

Xilinx Families

XC2000, XC3000, XC4000, XC5000, XC6000, XC7000, XC9000

Demonstrates

Choosing an appropriate Xilinx family based on the intended application

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Introduction

Xilinx offers Field-Programmable Logic circuits, mass-produced standard integrated circuits that the user can customize for the specific application.

Xilinx products offer the following advantages:

- High integration (less space, lower power, higher reliability, lower cost) than solutions based on existing standard devices like MSI and PALs.
- No non-recurring engineering charges and associated risk, typically required for mask-programmed gate array solutions.
- Fast design time and easy design modification, important for early time-to-market.
- Designs can be upgraded in the field for added functionality.

Some potential users might be confused by the wide diversity of Xilinx product offerings. This application note provides a broad overview from the user's perspective.

Xilinx offers programmable logic circuits in two distinctly different technologies.

- SRAM-based FPGAs, the original Xilinx offering, now encompassing the XC2000, XC3000, XC4000, XC5200, and XC6200 series and their sub-families, like the XC3000A, XC3000L, XC3100, XC3100A, XC4000A, XC4000H, XC4000E, XC4000L, XC4000EX, and XC4000XL.
- Complex PLDs or EPLDs, XC7300, and XC9500 families.

SRAM-Based FPGAs

Xilinx SRAM-based FPGAs fall into two distinct categories. All are reconfigurable and can be programmed in-system; only the XC6200 family can be partially reconfigured and offers a built-in microprocessor interface. The two categories of devices are separately described below.

SRAM-Based FPGAs (XC2000, XC3000, XC3100, XC4000, XC5200)

These families represent an ongoing evolution of the original Xilinx FPGA architecture, characterized by structural flexibility and an abundance of flip-flops. Logic is implemented in look-up tables, and is interconnected by a hierarchy of metal lines controlled by pass transistors.

Attractive systems features include on-chip bidirectional busses and individual output 3-state and slew-rate control, common reset for all flip-flops, and multiple global low-skew clock networks.

The configuration can be loaded while the devices are connected into a system, and can be changed an unlimited number of times by reloading the "bitstream," the series of bits used to program the device. Configuration must be reloaded whenever Vcc is re-applied. Reconfiguration takes 20 to 200 ms, during which time all outputs are inactive.

Static power consumption is very low, down to microwatts for some of the families. Dynamic power consumption is proportional to the clock frequency, and depends on the logic activity inside the device and on the outputs.

The description "SRAM-based" refers primarily to the standard high-volume manufacturing process, and secondarily to the fact that configuration data is stored in latches. Different from typical SRAMs, these latches use low-impedance active pull-up and pull-down transistors. An on-chip voltage monitor 3-states the outputs and initiates reconfiguration when Vcc drops significantly (to 3.2 V in a 5-V system).

These FPGAs are available in different sizes and many different packages. Usually each device type is available in many package types. Any package can accommodate different sized devices with compatible pinouts, so the user can migrate to a larger or smaller device without changing the PC-board layout.

Overview of SRAM-Based FPGA Families

XC2000: Oldest, simplest, smallest, and lowest-cost FPGA family; not recommended for new designs

- Used for simple, very cost-sensitive applications.
- Accept limited logic flexibility, 3-input look-up tables, no clock enables, no output slew-rate control, only two device types covering the narrow complexity range of 600 to 1500 gates.

The XC5200 FPGA family or the XC7300 and XC9500 EPLD families, may often be a better alternative.

XC2000L: 3.3-V version of XC2000; not recommended for new designs

- Used for simple, battery-operated applications.
- Accept significantly slower speed at 3.3 V, compared to XC2000 at 5 V.

XC3000: Superseded

Don't use this venerable family for new designs, since it has been superseded by the improved, but fully backwards compatible, XC3000A family.

XC3000A: Newest version of the popular XC3000 family

Five device types cover a complexity range from 1,300 to 7,500 gates, with 256 to 928 flip-flops. Logic is implemented in 4-input look-up tables; two tables can be combined to implement any logic function of five variables with only one combinatorial delay of 4 or 5 ns. Flip-flop toggle rate is over 110 MHz.

Global choice of input thresholds (1.2 V or 2.5 V), output slew-rate control, and an on-chip crystal oscillator circuit are attractive system features.

- Use for medium-speed, medium-complexity applications.
- Accept lack of dedicated carry circuits, resulting in less efficient and slower arithmetic and counters than in XC4000E families. No on-chip RAM; data storage is thus limited to the available 256 to 928 flip flops.

XC3000L: 3.3-V version of XC3000A

- Use for battery-operated applications.
- Accept significantly slower speed at 3.3 V, compared to XC3000A at 5 V.

XC3100: Superseded

Don't use this family for new designs, since it has been superseded by the improved, but fully backwards compatible XC3100A family.

XC3100A: Newest version of the popular high-speed XC3100 family

XC3100A devices are functionally and bitstream identical with the XC3000A, and are available in the same packages with the same pinouts. The only difference is the higher speed of the XC3100A, with a look-up table delay of 1.5 to 4 ns, and the slightly higher standby current of 8 to 14 mA. One additional high-end family member, the XC3195A, can implement up to 9,000 gates and 1,320 flip-flops.

- Use for high performance design with system clock rates up to 100 MHz.
- Accept lack of dedicated carry circuits, resulting in less efficient and possibly slower arithmetic and counters than in XC4000E. No on-chip RAM; data storage is thus limited to the available 256 to 1,320 flip-flops.

XC3100L: 3.3-V version of XC3100A

- Use for 3.3-V applications.
- Accept significantly slower speed at 3.3 V, compared to XC3100A at 5 V, as well as higher quiescent power and much higher powerdown current than XC3000L at 3.3 V.

XC4000: Superseded

Don't use this family for new designs, since it has been superseded by the improved, but fully backwards compatible XC4000E family.

XC4000A: Superseded

Don't use this family for new designs, since it has been superseded by the improved, faster, less expensive, and pinout-compatible – but not bitstream-compatible – XC4000E family.

XC4000E: Enhanced superset of the XC4000 family

The XC4000E family is recommended for new designs.

The ten devices in this family stretch from 2,000 to 25,000 gate complexity. The emphasis is on systems features and speed. The function generators are more versatile than in the XC3000-Series parts, and there is a dedicated carry network to speed up arithmetic and counters and make them more efficient. Most importantly, the function generators can be used as user RAM with asynchronous or synchronous write addressing, even as dual-port RAMs. This capability makes register files, shift registers and especially FIFOs faster and much more efficient than in any other FPGA.

Logic speed is not as fast as XC3100, but dedicated carry logic can speed up wide arithmetic and long counters even above XC3100 speed.

- Use for general-purpose logic and data-path logic that can take advantage of internal busses and fast arithmetic carry logic. Use for on-chip distributed RAMs, e.g. 50-MHz FIFOs up to 64 deep, 32 bits wide.
- Accept lack of crystal oscillator circuitry and lack of Powerdown feature.

XC4000EX: Larger version of the XC4000E family, largest devices made by Xilinx

Extension of the XC4000E family from 28k to 125k gates, with greatly increased routing resources, faster clocking options and more versatile output logic.

- Use for designs beyond 20,000 gate complexity.

XC4000H: High I/O version of XC4000, not recommended for new designs

Variations of XC4003 and XC4005, with significantly increased number of I/Os. Internal functionality identical to XC4003 and XC4005, but number of I/Os increased from 80 to 160 for XC4003H, from 112 to 192 for XC4005H. No input or output flip-flops in the IOBs, but 24 mA sink current and sophisticated slew-rate control that can minimize ground bounce.

- Used for I/O-intensive applications, but also consider XC5200 as a lower-cost alternative when internal RAM is not required.
- Accept lack of I/O flip-flops, thus larger output delay, larger uncertainty in input set-up time.

XC5200: Low-cost FPGA

New architecture optimized for low cost, good routability, and the ability to lock pinout while internal logic is being modified. Dedicated carry structure similar to XC4000, but no RAM. Four-input function generators avoid the XC3000 input constraints. IOBs are less rigidly coupled to the internal matrix of CLBs and interconnects, which greatly improves the flexibility of pin-locked designs. IOBs have no flip-flops.

The XC5200 family offers the lowest cost per gate of all Xilinx FPGAs, whenever RAM is not required.

Performance is similar to XC3000A, but dedicated carry logic can speed up wide arithmetic and long counters.

- Use for medium-speed general-purpose logic, and for data-path logic that can take advantage of internal busses and fast arithmetic carry logic. Alternative to XC3000A at lower cost, and with additional benefits, such as dedicated carry for arithmetic and counters, improved routing, and ability to cope with locked pinout. High I/O count. Package pinout compatible with XC4000.
- Accept lack of internal RAM and lack of crystal oscillator circuitry.

Partially-Reconfigurable SRAM-Based FPGA with Bus Interface (XC6200)

This new fine-grained architecture is very different from the other Xilinx families. It offers partial and very fast reconfigurability, supported by an 8/16/32 bit wide microprocessor bus interface. This interface can directly write to and read from any internal cell, and can even treat part of the internal configuration as user RAM.

- Use for innovative reconfigurable-processor solutions, and for general purpose solutions where fast (re)configuration is an advantage, or for register-intensive, datapath-oriented, highly structured designs.
- Accept product availability starting later in 1996.

EPROM- and FLASH-Based CPLDs (XC7300, XC9500)

These device families are extensions of the popular PAL architecture, implementing logic as wide AND gates, ORed together, driving either a flip-flop or an output directly. The simple logic structure makes these devices easy to understand, and results in both fast design compilation and short pin-to-pin delays. Wide input gating and fast system clock rates up to 150 MHz are attractive features for state machines and complex synchronous counters.

The XC7300 CPLDs use EPROM technology.

The new XC9500 in-system programmable family, based on FLASH technology, eliminates the need for a separate programmer. These new devices also offer boundary scan (JTAG) to simplify board testing.

Overview of CPLD Families

XC7200A: Superseded

Not recommended for new designs. Use XC7300 instead.

XC7300: EPROM-Based CPLD

Six devices cover the range from 18 to 144 macrocells in 44- to 225-pin packages.

- Use for high-speed logic, short pin-to-pin delays, for state machines and flexible address decoding, and as PAL replacement. Dedicated carry logic offers fast and efficient adders, subtractors, comparators, and counters.
- Accept higher power consumption and fewer available flip-flops compared to SRAM-based or antifuse-based FPGAs.
- The XC7318, XC7336/Q, and XC7354 are very effective as PAL replacements. The XC7336Q boasts significantly reduced power consumption.

Delays are deterministic, and compile times are very short.

XC9500: FLASH-Based CPLD

Nine devices cover the range from 36 to 576 macrocells.

The new XC9500 family provides advanced in-system programming and test capabilities for high performance, general purpose logic integration.

- Use XC9500 for CPLD applications requiring fast pin-to-pin speeds.
- Accept higher power consumption and fewer available flip-flops compared to SRAM- or antifuse-based FPGA.

Selecting the Appropriate Xilinx Family

It is not always obvious which Xilinx family is the "right" choice for a particular application. To make a decision, start with the known data, the target application. Then address the following questions:

- What type of logic is used in the application?
- What special features are required?

Type of Logic

All Xilinx devices are general-purpose. Any family can implement any type of logic. There are, however, some features that make certain families more appropriate than others. The following items should be interpreted as "soft" suggestions, not as absolute, unequivocal choices.

1. For shortest pin-to-pin delays and fastest flip-flops:

Use XC9500, XC7300, or, if fan-in is sufficient, XC3100A, XC4000E/EX.

XC9500 and XC7300 CPLDs have a PAL-like AND/OR structure that is inherently very fast. XC3100 has extremely fast logic blocks, but the single-level fan-in is limited to five.

XC4000E/EX have slower logic blocks, but a wider fan-in of nine. XC4000EX FPGAs offer a very fast pin-to-pin path using a FastClk buffer and a 2-input function generator in the IOB.

2. For fastest state machines:

For encoded state machines, use XC9500, XC7300.

For "one-hot" state machines, use XC3100, XC4000E/EX, XC5200.

3. For fast counters/adders/subtractors/accumulators/ comparators:

Use XC4000E/EX, XC5200 or XC7300 for wide functions.

Use XC3100A for very fast, but short or simple counters.

XC4000E/EX and XC5200 have dedicated carry-logic that is most effective over the range of 8 to 32 bits.

XC7300 has dedicated carry within a function block, and can implement unlimited carry look-ahead in the Universal Interconnect Matrix.

XC3100A achieves high speed for short word-length and simple operations (such as non-loadable counters) through its extremely fast logic blocks.

4. For I/O-intensive applications with a high ratio of I/O to gates:

Use XC5200.

5. For shortest design compilation time:

Use XC9500, or XC6200.

XC9500 achieves fast compilation through the simplicity of its PAL-like architecture.

XC6200 achieves fast compilation through its ASIC-like small granularity, which requires no logic partitioning effort.

6. For lowest cost per gate, when on-chip RAM is not required:

Use XC5200, XC3000A (XC2000 for small devices in high volume).

7. For pinout compatibility within and between families:

Use XC4000E/EX, XC5200.

These three families are carefully designed to fit the same pinout in any given available package. This allows easy migration to different device sizes or families in the same package. The user can add logic or streamline the design or even use a less costly or faster family without any need to change the existing PC-board layout.

8. For Digital Signal Processing multiply-accumulate) applications:

Use XC4000E/EX.

The look-up-table architecture and the dedicated carry structure are very efficient for distributed arithmetic, a fast and effective way to implement fixed-point multiplication in digital filters.

Special Features Required

The sixteen items below describe specific features and characteristics available only in the listed families. These are, therefore, "hard" selection criteria.

9. For on-chip RAM:

Use XC4000E, XC4000EX, or XC6200.

XC4000E/EX has many 16x1 or 32x1 RAMs with synchronous or asynchronous write and dual-port capability.

XC6200 can implement an arbitrary portion of the configuration-memory space as user RAM.

10. For on-chip (bidirectional) bussing:

Use XC3000A, XC3100A, XC4000E, XC4000EX, XC5200, XC7300, XC9500 (i.e., use any Xilinx family except XC2000).

XC3000A, XC3100A, XC4000, and XC5200 families have horizontal Longlines that can be driven by internal 3-state drivers.

XC9500 and XC7300 devices implement busses indirectly using the wired-AND capability in the switch matrix.

11. For on-chip crystal oscillator circuitry:

Use XC2000/L, XC3000A/L, XC3100A/L.

The on-chip circuit is just a dedicated single-stage inverting amplifier that can be configured between two dedicated pins. It is not recommended for designs requiring very low power consumption or crystal frequencies below 1 MHz.

12. For very fast or partial reconfiguration, and for a dedicated microprocessor interface:

Use XC6200.

All other SRAM-based families must be completely reconfigured.

13. For non-volatile single-chip solutions:

Use XC9500, XC7300, or any HardWire device.

The SRAM-based devices require an external configuration source, which may be contained in the microprocessor's memory. XC3000A and XC3000L devices can be used with a battery-backed-up supply, thus eliminating the need for external configuration storage.

14. For lowest possible static power consumption at 5V:

Use XC2000, XC3000A and, to a lesser extent, XC5200, XC4000E, XC4000EX.

For Icc down to a few microamps, use XC2000/L or XC3000A/L in powerdown. The other families consume a few milliamps.

Configurations for CMOS input thresholds on all inputs reduce supply current significantly.

15. For avoiding pin-locking problems with routing-intensive designs:

Use XC9500, XC7300, XC4000EX, XC5200.

XC9500 and XC7300 have special architectural features to enable pin locking.

XC4000EX and XC5200 provide additional routing channels, called VersaRing, between the core logic and the I/O.

16. For Boundary-Scan support:

Use XC4000E, XC4000EX, XC5200, XC9500.

17. For rail-to-rail output voltage swing at 5 V Vcc:

Use XC2000, XC3000A, XC3100A, XC4000H, XC4000E, XC4000EX, XC5200, XC6200.

(In XC4000H/E/EX, rail-to-rail is a user-option.)

XC4000, XC7300, and XC9500 have a "totem-pole" output structure with lower Voh.

XC4000E/EX can be configured with a global choice of either totem-pole or rail-to-rail outputs.

XC4000H has this option per individual pin.

18. For 3.3-V operation:

Use XC2000L, XC3000L, XC4000L, XC4000XL.

19. For 5-V operation Interfacing with 3.3-V devices:

Use XC9500, XC7300 or XC4000E/EX.

Any XC4000E/EX "totem-pole" output drives 3.3-V inputs safely, and the TTL-like input threshold can be driven from 3.3-V logic.

20. For In-system programmability:

Use all Xilinx families except XC7300.

21. For PCI compatibility:

Use XC4000E/EX and XC9500.

Target and Initiator designs are available for the XC4000E.

XC3100 and XC7300 can implement target-only interfaces.

22. For Hi-Rel, military, or mil temperature-range applications:

Use XC2018, XC3000, XC3100A, XC4003A, XC4005, XC4010, XC4013.

23. For battery-operated applications requiring low stand-by current:

Use XC2000/L, XC3000A/L, XC4000E/EX, XC5200, XC6200.

XC2000L and XC3000L have inherently very low static power consumption.

XC2000 and XC3000A can use powerdown to ignore all input activity and tolerate Vcc down to 2.3 V, while maintaining configuration.

XC4000E/EX must be configured for CMOS input thresholds, and must shut down clock and logic activities externally.

24. For best protection against Illegal copying of a design (design security):

Use XC7300, XC9500 with security bit activated.

Use XC2000, XC2000L, XC3000A, XC3000L with powerdown battery-backed-up configuration.

Further Information

For further information on any of the Xilinx products discussed in this application note, see the Xilinx WEBLINX at http://www.xilinx.com, or call your local sales office.

Table 1: Selecting a Xilinx Family

Feature	XC3000A	XC3000L	XC3100A	XC3100L	XC4000E	XC4000L	XC4000EX	XC4000XL	XC5200	XC6200	XC7300	XC9500
1. Shortest pin-to-pin			X		X		X				X	X
2. Fastest state machines			X		X		X		X		X	X
3. Fastest arithmetic counters			X		X				X		X	
4. High I/O to gate ratio									X			
5. Fastest compilation										X	X	X
6. Lowest cost, no RAM	X								X			
7. Footprint compatible families					X	X	X	X	X			
8. DSP (multiply/accumulate)					X	X	X	X				
9. RAM					X	X	X	X		X		
10. Bidirectional busses	X	X	X	X	X	X	X	X	X		X	X
11. Crystal oscillator	X	X	X	X								
12. Fast/partial configuration										X		
13. Non-volatile/single chip											X	X
14. Low power @ 5 V	X				X		X		X			
15. Tolerates pin-locking							X	X	X		X	X
16. Boundary scan					X	X	X	X	X			X
17. Full-swing 5 V output	X		X		option		option		X	X		
18. 3.3 V operation		X		X		X		X				
19. 5 V out drives 3.3 V					option		option				X	X
20. In-system programmable	X	X	X	X	X	X	X	X	X	X		X
21. PCI-compatible			X		X		X				X	X
22. Hi-rel, mil, mil-temp	X		X		X							
23. Low standby current	X	X			X	X	X	X	X	X		
24. Design security	X	X									X	X

June 1, 1996 (Version 1.0)

Application Note

Summary

This Application Note contains additional information that may be of use when designing with XC4000 Series devices. This information supplements the product descriptions and specifications, and is provided for guidance only.

Xilinx Family

XC4000/XC4000A/XC4000H/XC4000E/XC4000L

Introduction

This application note describes the electrical characteristics of the output drivers, their static output characteristics or I/V curves, the additional delay caused by capacitive loading, and the ground bounce created when many outputs switch simultaneously.

Voltage/Current Characteristics of XC4000-Family Outputs

Figures 1 and 2 show the output source and sink currents, both drawn as absolute values. Note that the XC4000E/EX families offer a configuration choice between an n-channel only, totem-pole like output structure that pulls a High output to a voltage level that is one threshold drop lower than V_{CC}, and a conventional complementary output with a p-channel transistor pulling to the positive supply rail. When driving inputs that have a 1.4-V threshold, the lower V_{OH} of the totem-pole ("TTL") output offers faster speed and more symmetrical switching delays.

These curves represent typical devices. Measurements were taken at V_{CC}= 5 V, T = 25°C. These characteristics vary by manufacturing lot, and will be affected by future changes in minimum device geometries. These characteristics are not production-tested as part of the normal device test procedure; they can, therefore, not be guaranteed. Although these measurements show that the output sink and source capability far exceeds the guaranteed data sheet limits, continuous high-current operation beyond the data sheet limits can cause metal migration of the on-chip metal traces, permanently damaging the device. Output currents in excess of the data-sheet limits are, therefore, not recommended for continuous operation. These output characteristics can, however, be used to calculate or model output transient behavior, especially when driving transmission lines or large capacitive loads.

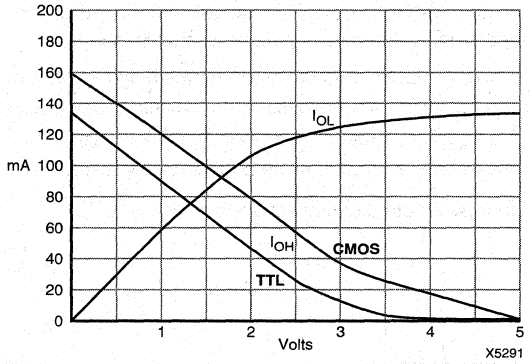


Figure 1: Output Voltage/Current Characteristics for XC4000E

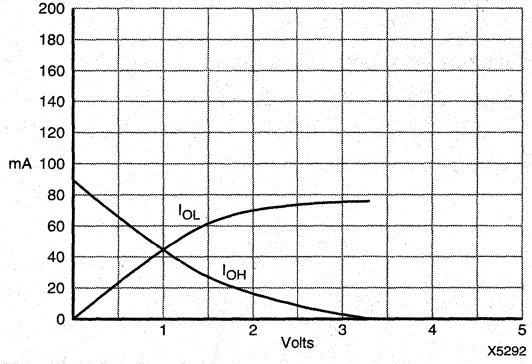


Figure 2: Output Voltage/Current Characteristics for XC4000L

Additional Output Delays When Driving Capacitive Load

Xilinx Product Specifications in chapter 4 give guaranteed worst-case output delays with a 50-pF load.

The values below are based on actual measurements on a small number of mid-93 production XC4005-5, all in PQ208 packages, measured at room temperature and V_{CC} = 5.5 V. Listed is the additional output delay, measured crossing 1.5 V, relative to the delays specified in this Data Book.

These parameters are not part of the normal production test flow, and can, therefore, not be guaranteed.

Table 1: Increase in Output Delay When Driving Light Capacitive Loads (<150 pF)

		High-to-Low			Low-to-High			
	Slew Mode	**10**	**50**	**100**	**10**	**50**	**100**	**pF**
XC4000	Slow	-1.6	0*	1.4	-1.4	0*	1.4	ns
	Fast	-1.6	0*	1.2	-1.2	0*	1.1	ns

Note: *Zero by definition

Table 2: Increase in Output Delay When Driving Heavy Capacitive Loads (>150 pF)

	Slew Mode	**High-to-Low**	**Low-to-High**	
XC4000	Slow	1.7	1.2	ns/100 pF
	Fast	1.5	1.2	ns/100 pF

Example:

ΔT High-to-Low for XC4005-5 with Fast-mode output driving 250 pF:

1.2 ns (from Table 1) plus (250-100) pF • 1.5 ns/100 pF = 1.2 ns + 2.25 ns = 3.45 ns

Total propagation delay, clock to pad:

T_{OKPOF} + 3.45 ns = 7.0 ns + 3.45 ns = 10.45 ns

Ground Bounce in XC4000 Devices

Ground-bounce is a problem with high-speed digital ICs, when multiple outputs change state simultaneously causing undesired transient behavior on an output, or in the internal logic. This is also referred to as the Simultaneous Switching Output (SSO) problem. Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC-internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously. Ground bounce affects outputs that are supposed to be stable Low, and it also affects all inputs since they interpret the incoming level by referencing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input will be interpreted as a short pulse with a polarity opposite to the ground bounce.

V_{CC} bounce is not as important as ground bounce, because it is of lower magnitude due to the weaker pull-up transistors. Also, the noise immunity in the High state is usually better than in the Low state, and input levels are referenced to ground, not V_{CC}. All this is the result of our industry's TTL heritage.

Test Method

Data was taken on XC4005-5, devices in the PQ208 package, soldered to the Xilinx Ground Bounce Test Board. Pin 82, two pins away from the nearest ground pin, was configured as a permanently Low output driver, effectively monitoring the internal ground level. The simultaneously switching outputs were on pins 80 and 83, for two outputs switching; additionally, pins 80 and 86 were used for four outputs switching. The closest ground pins are 79 and 90.

Four ground-bounce parameters were measured at room temperature, with Vcc set at 5.5 V as shown in Figure 3.

- V_{OLP-HL} Peak ground noise when switching High-to-Low
- V_{OLV-HL} Valley ground noise when switching High-to-Low
- V_{OLP-LH} Peak ground noise switching Low-to-High
- V_{OLV-LH} Valley ground noise switching Low-to-High

All four parameters can affect system reliability.

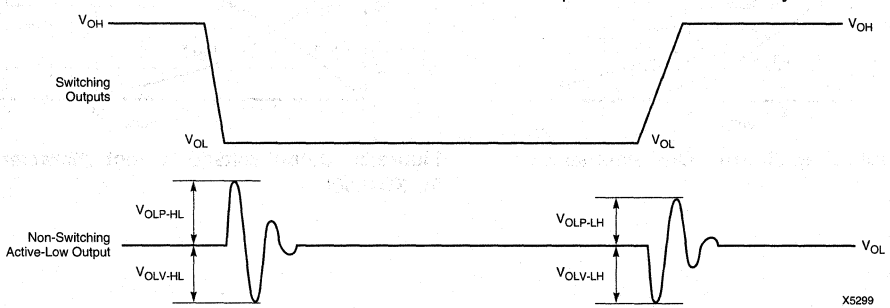


Figure 3: Ground Bounce

The two positive peak values can cause problems with a signal leaving the ground bounce chip, driving another chip. The positive ground bounce voltage is added to the V_{OL}, and may exceed the receiving input's noise margin. A continuously logic Low input may thus be interpreted as a short-duration High pulse.

The two negative valley parameters can cause problems with a signal arriving at the ground-bounce chip, reducing the Low-level noise immunity. The incoming voltage may not be Low enough, and may, therefore, be interpreted as a short-duration High input pulse.

Table 3: Ground Bounce, 16 Outputs Switching, Each With 50 or 150 pF Load, V_{CC} = 5.5 V

Load	Slew Rate	High-to-Low		Low-to-High		Unit
		V_{OLP}	V_{OLV}	V_{OLP}	V_{OLV}	
16 x 50 pF	Slow	670	480	240	240	mV
	Fast	1,170	710	480	660	mV
16 x 150 pF	Slow	740	330	210	280	mV
	Fast	1,180	420	350	710	mV

Interpretation of the Results

Ground bounce is a linear phenomenon. When multiple outputs switch, the total ground bounce is the sum of the ground-bounce values caused by individual outputs switching. Since the actual switching of multiple outputs is usually not quite simultaneous, small timing differences between the switching outputs, caused by routing delays, can indirectly affect the amplitude. With low capacitive loading, < 50 pF, the peaks and valleys might even partially cancel each other. With larger capacitive loads, the tendency is for valleys to combine with valleys and peaks to combine with peaks.

In most devices tested, the load capacitance does not directly affect the ground-bounce **amplitude**, but it does affect the **duration** of the ground-bounce signals.

On the fastest outputs, minimal load capacitance created a ground-bounce resonant frequency of 340 MHz, with a half-cycle time of 1.5 ns. Such a signal exceeds 90% of its peak amplitude for about 0.4 ns.

With a 50 pF load on the switching outputs, the ground bounce resonant frequency is 90 MHz, with a half-cycle time of 5 ns, staying 1.7 ns above 90% of peak amplitude.

With a 150 pF load on the switching outputs, the ground bounce resonant frequency is 40 to 60 MHz, with a half-cycle time of 8 to 12 ns, staying 3 ns above 90% of peak amplitude.

The main problem with large load capacitances is not an increase in amplitude, but rather an increase in duration of the ground-bounce signal. The amplitude is mainly affected by the number of outputs switching simultaneously, and by the slew-rate mode of these outputs. Switching outputs closer to the monitoring output also cause larger peaks and valleys than outputs further away.

Guidelines for Reducing Ground-Bounce Effects

- Minimize the impedance of the system ground distribution network and its connection to the IC pins. PQFPs are best suited, PGAs are worst, and PLCCs are in-between.
- Use PC-boards with ground- and V_{CC}-planes, connected directly to the ICs' supply pins. Place decoupling capacitors very close to these ground and V_{CC} pins.
- Keep the ground plane as undisturbed as possible. A row of vias can easily cause a dynamic ground-voltage drop.
- Keep the clock inputs physically away from the outputs that create ground bounce, and connect clocks to input pins that are close to a ground pin. Make sure that all clock and asynchronous inputs have ample noise margin, especially in the Low state.
- If possible, avoid simultaneous switching by staggering output delays, e.g. through additional local routing of signals or clocks.
- Spread simultaneously switching outputs around the IC periphery. For a 16-bit bus, use two outputs each on either side of four ground pins.

Ground-Bounce vs Delay Trade-Off

After the external sources of ground bounce have been reduced or eliminated. the designer can trade reduced ground bounce for additional delay by selecting between families and slew-rate options. Figure 4 shows the trade-off for 16 outputs switching simultaneously High-to-Low.

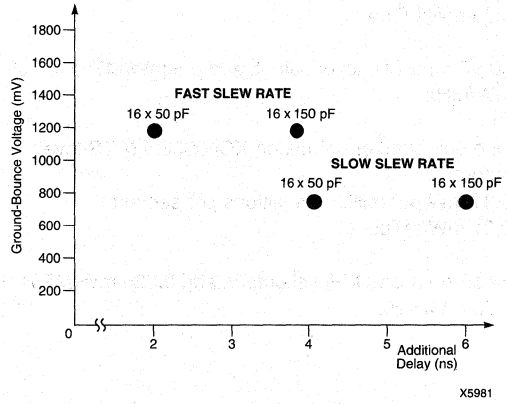


Figure 4: Ground-Bounce vs. Delay Trade-off for 16 Outputs Switching 50 and 150 pF Each

XC4000 and XC4000E Power Consumption

Below are the dynamic power consumption values for typical design elements in XC4000 and XC4000E.

The differences between XC4000 and XC4000E are too small to be statistically relevant:

Global clocks in XC4000E are 3% higher, and Longlines and unloaded outputs in XC4000E are 5 to 10% lower than in XC4000.

Power consumption is given at nominal 5.0-V supply and 25°C.

Power is proportional to the square of the supply voltage, but is almost constant over temperature changes. Power is given as "mW per million transitions per second", since the more commonly used "MHz" can be ambiguous. When a 10-MHz clock toggles a flip-flop, the clock line obviously makes 20 MTps, the flip-flop output only 10 MTps.

The first six elements are device-size independent, i.e. they are applicable to all XC4000 or XC4000E devices operating at 5-V Vcc.

- One CLB flip-flop driving nothing but a neighboring flip-flop in the same or adjacent CLB (a typical shift register design):
  0.1 mW per million transitions per second =
  0.1 mW/MTps

- One CLB flip-flop driving its neighbor plus 9 lines of interconnect:
  0.2 mW per million transitions per second =
  0.2 mW/MTps

- One unloaded or unbonded TTL-level output:
  0.25 mW per million transitions per second =
  0.25 mW/MTps

- 50 pF on a TTL-level output: add 0.5 mW/MTps = 1.0 mW/MHz

- One unloaded or unbonded XC4000E CMOS-level output:
  0.31 mW per million transitions per second =
  0.31 mW/MTps

- 50 pF on a CMOS-level output: add 0.625 mW/MTps = 1.25 mW/MHz

The following elements are obviously device-size dependent:

- One Global Clock driving all CLB flip-flops, but no flip-flop changing:
  in XC4005: 4 mW/MTps = 8 mW/MHz
  in XC4010: 8 mW/MTps = 16 mW/MHz
  in XC4013: 12 mW/MTps = 24 mW/MHz
  in XC4020: 16 mW/MTps = 32 mW/MHz
  in XC4025: 20 mW/MTps = 40 mW/MHz

- One full-length horizontal or vertical Longline with one driving CLB source and one driven CLB load:
  in XC4005: 0.10 mW/MHz = 0.20 mW/MHz
  in XC4010: 0.15 mW/MTps = 0.30 mW/MHz
  in XC4013: 0.18 mW/MTps = 0.36 mW/MHz
  in XC4020: 0.20 mW/MTps = 0.40 mW/MHz
  in XC4025: 0.24 mW/MTps = 0.48 mW/MHz

These numbers do not account for the 10 mA of static power consumption when all device inputs are configured in TTL mode, which is always the default mode, and in XC4000 is actually the only user-accessible mode.

These numbers assume short rise and fall times on all inputs, avoiding the cross-current when both the n-channel pull-down and the p-channel pull-up transistor in the input buffer might conduct simultaneously.

Tutorial Comments:

In its pure form, a CMOS output driving a capacitive load has a power consumption that is independent of drive impedance or rise and fall time. For a full-swing signal, the power consumed when charging the capacitor is $C \times V^2 \times f$ where f is the frequency of charge operations. In each charge operation, half the total energy consumed ends up on the capacitor, and the other half of the energy is dissipated in the current-limiting resistor or transistor, whatever its value may be.

The subsequent discharge cycle does not take any new energy from the power supply, but dissipates in the current-limiting resistor/transistor all the energy that was formerly stored in the capacitor.

It is assumed here that the frequency is low enough so that the capacitors are completely charged and discharged in each half-cycle.

XC3000 Series Technical Information

June 1, 1996 (Version 1.0)

Application Note By Peter Alfke and Bernie New

Summary

This Application Note contains additional information that may be of use when designing with the XC3000 series of FPGA devices. This information supplements the data sheets, and is provided for guidance only.

Xilinx Family

XC3000/XC3000A/XC3000L/XC3100/XC3100A/XC3100L

Contents

Introduction

The background information provided in this Application Note supplements the XC3000, XC3000A, XC3000L, XC3100A and XC3100L data sheets. It covers a wide range of topics, including a number of electrical parameters not specified in the data sheets, and unless otherwise noted, applies to all six families. These additional parameters are sufficiently accurate for most design purposes; unlike the parameters specified in the data sheets, however, they are not worst-case values over temperature and voltage, and are not 100% production tested. They can, therefore, not be guaranteed.

Configurable Logic Blocks

The XC3000/XC3100 CLB, shown in Figure 1, contains a combinatorial function generator and two D-type flip-flops. Two output pins may be driven by either the function generators or the flip-flops. The flip-flop outputs may be routed directly back to the function generator inputs without going outside of the CLB.

The function generator consists of two 4-input look-up tables that may be used separately or combined into a single function. Figure 2 shows the three available options. Since the CLB only has five inputs to the function generator, inputs must be shared between the two look-up tables.

In the FG mode, the function generator provides any two 4-input functions of A, B and C plus D or E; the choice between D and E is made separately for each function. In the F mode, all five inputs are combined into a single 5-input function of A, B, C, D and E. Any 5-input function may be emulated. The FGM mode is a superset of the F mode, where two 4-input functions of A, B, C and D are multiplexed together according to the fifth variable, E.

In all modes, either of the B and C inputs may be selectively replaced by QX and QY, the flip-flop outputs. In the FG mode, this selection is made separately for the two look-up tables, extending the functionality to any two functions of four variables chosen from seven, provided two of the variables are stored in the flip-flops. This is particularly useful in state-machine-like applications.

In the F mode, the function generators implement a single function of five variables that may be chosen from seven, as described above. The selection of QX and QY is constrained to be the same for both look-up tables. The FGM mode differs from the F mode in that QX and QY may be selected separately for the two look-up tables, as in the FG mode. This added flexibility permits the emulation of selected functions that can include all seven possible inputs.

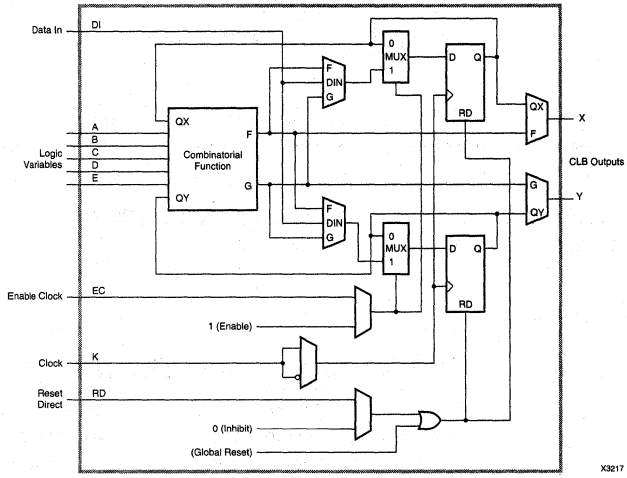


Figure 1: Configurable Logic Block (CLB)

Function Generator Avoids Glitches

The combinatorial logic in all CLBs is implemented as a function generator in the form of a multiplexer, built out of transfer gates. The logic inputs form the select inputs to this multiplexer, while the configuration bits drive the data inputs to the multiplexer.

The Xilinx circuit designers were very careful to achieve a balanced design with similar (almost equal) propagation delays from the various select inputs to the data output.

The delay from the data inputs to the output is, of course, immaterial, since the data inputs do not change dynamically. They are only affected by configuration.

This balanced design minimizes the duration of possible decoding glitches when more than one select input changes. Note that there can never be a decoding glitch when only one select input changes. Even a non-overlapping decoder cannot generate a glitch problem, since the node capacitance will retain the previous logic level until the new transfer gate is activated about a nanosecond later.

When more than one input changes "simultaneously," the user should analyze the logic output for any possible intermediate code. If any such code permutation produces a different result, the user must assume that such a glitch might occur and must make the system design immune to it. The glitch might be only a few nanoseconds long, but that is long enough to upset an asynchronous design.

If none of the possible address sequences produces a different result, the user can be sure that there will be no glitch.

The designer of synchronous systems generally doesn't worry about such glitches, since synchronous designs are fundamentally immune to glitches on all signals except clocks or direct SET/RESET inputs.

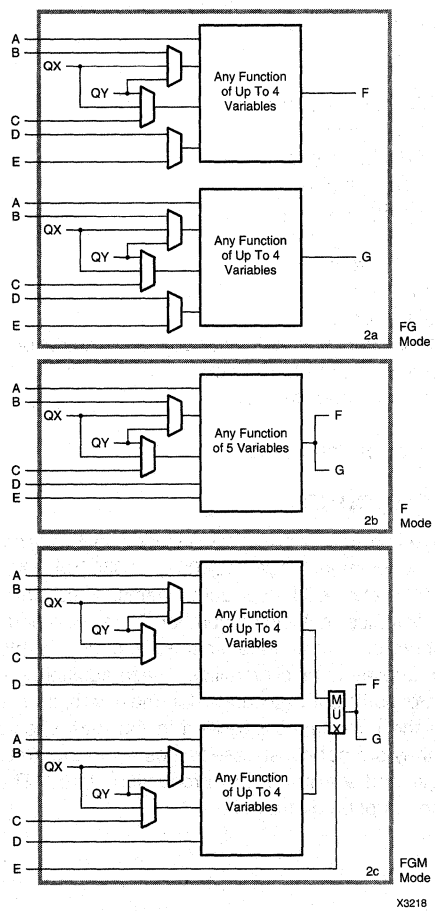


Figure 2: CLB Logic Options

The automatic logic-partitioning software in the XACT*step* development system only uses the FG and F modes. However, all three modes are available with manual partitioning, which may be performed in the schematic. If FG or F modes are required, it is simply a matter of including in the schematic CLBMAP symbols that define the inputs and outputs of the CLB.

The FGM mode is only slightly more complicated. Again, a CLBMAP must be used, with the signal that multiplexes between the two 4-input functions locked onto the E pin. The CLB will be configured in the FGM mode if the logic is drawn such that the gates forming the multiplexer are shown explicitly with no additional logic merged into them.

The two D-type flip-flops share a common clock, a common clock enable, and a common asynchronous reset signal. An asynchronous preset can be achieved using the asynchronous reset if data is stored in active-low form; the Low created by reset corresponds to the bit being asserted. The flip-flops cannot be used as latches.

If input data to a CLB flip-flop is derived directly from an input pad, without an intervening flip-flop, the data-pad-to-clock-pad hold time will typically be non-zero. This hold time is equal the delay from the clock pad to the CLB, but may be reduced according to the 70% rule, described later in the IOB Input section of this Application Note. Under this rule, the hold time is reduced by 70% of the delay from the data pad to the CLB, excluding the CLB set-up time. The minimum hold time is zero, even when applying the 70% rule results in a negative number.

The CLB pins to which Longlines have direct access are shown in Table 1. Note that the clock enable pin (EC) and the TBUF control pin are both driven from to the same vertical Long Line. Consequently, EC cannot easily be used to enable a register that must be 3-stated onto a bus. Similarly, EC cannot easily be used in a register that uses the Reset Direct pin (RD).

Table 1: Longline to CLB Direct Access

	CLB								TBUF
Longline	A	B	C	D	E	K	EC	RD	T
Left Most Vertical (GCLK)						X			
Left Middle Vertical		X					X	X	X
Right Middle Vertical			X		X				
Right Most Vertical (ACLK)						X			
Upper Horizontal				X					
Lower Horizontal	X							X	

Input/Output Blocks

The XC3000/XC3100 IOB, shown in Figure 3, includes a 3-state output driver that may be driven directly or registered. The polarities of both the output data and the 3-state control are determined by configuration bits. Each output buffer may be configured to have either a fast or a slow slew rate.

The IOB input may also be direct or registered. Additionally, the input flip-flop may be configured as a latch. When an IOB is used exclusively as an input, an optional pull-up resistor is available, the value of which is 40-150 kΩ. This resistor cannot be used when the IOB is configured as an output or as a bidirectional pin.

Unused IOBs should be left unconfigured. They default to inputs pulled High with the internal resistor.

Inputs

All inputs have limited hysteresis, typically in excess of 200 mV for TTL input thresholds and in excess of 100 mV for CMOS thresholds. Exceptions to this are the $\overline{\text{PWRDWN}}$ pin, and the XTL2 pin when it is configured as the crystal oscillator input.

Experiments show that the input rise and fall times should not exceed 250 ns. This value was established through a worst-case test using internal ring oscillators to drive all I/O pins except two, thus generating a maximum of on-chip noise. One of the remaining I/O pins was configured as an input, and tested for single-edge response; the other I/O was used as an output to monitor the response.

These test conditions are, perhaps, overly demanding, although it was assumed that the PC board had negligible ground noise and good power-supply decoupling. While conservative, the resulting specification is, in most instances, easily satisfied.

IOB input flip-flops are guaranteed to operate correctly without data hold times (with respect to the device clock-input pad) provided that the dedicated CMOS clock input pad and the GCLK buffer are used. The use of a TTL clock or a different clock pad will result in a data-hold-time requirement. The length of this hold time is equal to the delay from the actual clock pad to the GCLK buffer minus the delay from the dedicated CMOS clock pad to the GCLK buffer.

To ensure that the input flip-flop has a zero hold time, delay is incorporated in the D input of the flip-flop, causing it to have a relatively long set-up time. However, the set-up time specified in the data sheet is with respect to the clock reaching the IOB. Since there is an unavoidable delay between the clock pad and the IOB, the input-pad-to-clock-pad set-up time is actually less than the data sheet number.

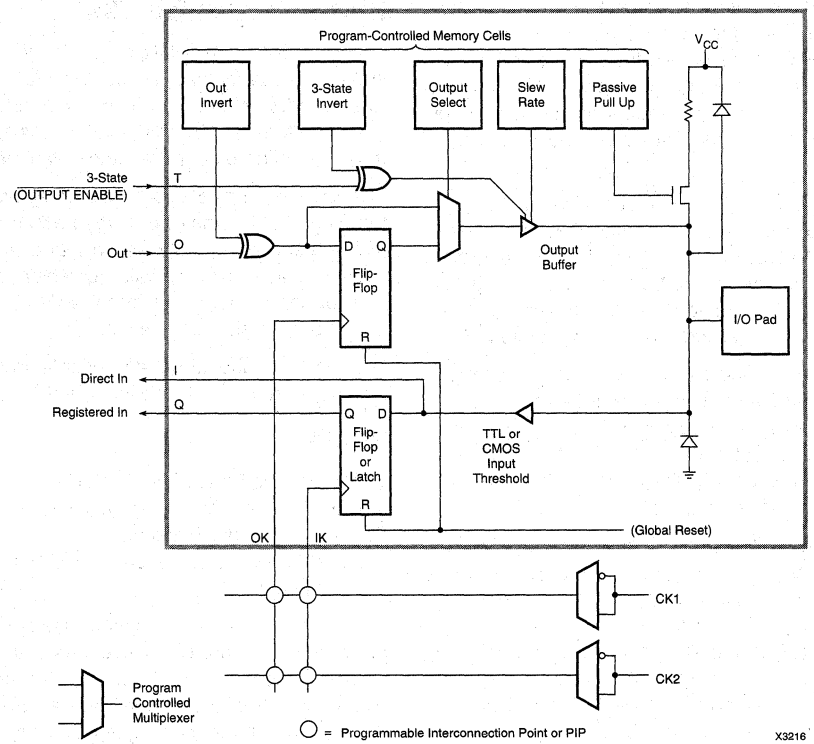


Figure 3: Input/Output Block (IOB)

Part of the clock delay can be subtracted from the internal set-up time. Ideally, all of the clock delay could be subtracted, but it is possible for the clock delay to be less than its maximum while the internal set-up time is at its maximum value. Consequently, it is recommended that, in a worst-case design, only 70% of the clock delay is subtracted.

The clock delay can only be less than 70% of its maximum if the internal set-up time requirement is also less than its maximum. In this case, the pad-to-pad set-up time actually required will be less than that calculated.

For example, in the XC3000-125, the input set-up time with respect to the clock reaching the IOB is 16 ns. If the delay from the clock pad to the IOB is 6 ns, then 70% of this delay, 4.2 ns, can be subtracted to arrive at a maximum pad-to-pad set-up time of ~12 ns.

The 70% rule must be applied whenever one delay is subtracted from another. However, it is recommended that delay compensation only be used routinely in connection with input hold times. *Delay compensation in asynchronous circuits is specifically not recommended.* In any case, the compensated delay must not become negative. If 70% of the compensating delay is greater than the delay from which it is deducted, the resulting delay is zero.

The 70% rule in no way defines the absolute minimum values delays that might be encountered from chip to chip, and with temperature and power-supply variations. It simply indicates the relative variations that might be found within a specific chip over the range of operating conditions.

Typically, all delays will be less than their maximum, with some delays being disproportionately faster than others. The 70% rule describes the spread in the scaling factors; the delay that decreases the most will be no less than 70% of what it would have been if it had scaled in proportion to the delay that decreased the least. In particular, in a worst-case design where it is assumed that any delay might not have scaled at all, and remains at its maximum value, other delays will be no less than 70% of their maximum.

Outputs

All XC3000/XC3100 FPGA outputs are true CMOS with n-channel transistors pulling down and p-channel transistors pulling up. Unloaded, these outputs pull rail-to-rail. Some additional ac characteristics of the output are listed in Table 2. Figure 4 and Figure 5 show output current/voltage curves for typical XC3000 and XC3100 devices.

Output-short-circuit-current values are given only to indicate the capability to charge and discharge capacitive

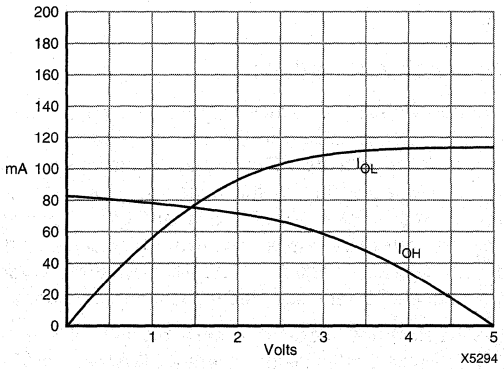


Figure 4: Output Current/Voltage Characteristics for XC3000, XC3000A, XC3100 and XC3100A Devices

loads. In accordance with common industry practice for other logic devices, only one output at a time may be short circuited, and the duration of this short circuit to V_{CC} or ground may not exceed one second. Xilinx does not recommend a continuous output or clamp current in excess of 20 mA on any one output pin. The data sheet guarantees the outputs for no more than 4 mA at 320 mV to avoid problems when many outputs are sinking current simultaneously.

The active-High 3-state control (T) is the same as an active-Low output enable ($\overline{OE}$). In other words, a High on the T-pin of an OBUFZ places the output in a high impedance state, and a Low enables the output. The same naming convention is used for TBUFs within the FPGA device.

I/O Clocks

Internally, up to eight distinct I/O clocks can be used, two on each of the four edges of the die. While the IOB does not provide programmable clock polarity, the two clock lines serving an IOB can be used for true and inverted clock, and the appropriate polarity connected to the IOB. This does, however, limit all IOBs on that edge of the die to using only the two edges of the one clock.

Table 2: Additional AC Output Characteristics

AC Parameters	Fast*	Slow*
Unloaded Output Slew Rate	2.8 V/ns	0.5 V/ns
Unloaded Transition Time	1.45 ns	7.9 ns
Additional rise time for 812 pF	100 ns	100 ns
normalized	0.12 ns/pF	0.12 ns/pF
Additional fall time for 812 pF	50 ns	64 ns
normalized	0.06 ns/pF	0.08 ns/pF

* Fast and Slow refer to the output programming option.

IOB latches have active-Low Latch Enables; they are transparent when the clock input is Low and are closed when it is High. The latch captures data on what would otherwise be the active clock edge, and is transparent in the half clock period before the active clock edge.

Routing

Horizontal Longlines

As shown in Table 3, there are two horizontal Longlines (HLLs) per row of CLBs. Each HLL is driven by one TBUF for each column of CLBs, plus an additional TBUF at the left end of the Longline. This additional TBUF is convenient for driving IOB data onto the Longline. In general, the routing resources to the T and I pins of TBUFs are somewhat limited.

Table 3: Number of Horizontal Longlines

Part Name	Rows x Columns	CLBs	Horizontal Longlines	TBUFs per HLL
XC3020	8 x 8	64	16	9
XC3030	10 x 10	100	20	11
XC3042	12 x 12	144	24	13
XC3064	16 x 14	224	32	15
XC3090	20 x 16	320	40	17
XC3195	22 x 22	484	44	23

Optionally, HLLs can be pulled up at either end, or at both ends. The value of each pull-up resistor is 3-10 kΩ.

In addition, HLLs are permanently driven by low-powered latches that are easily overridden by active outputs or pull-up resistors. These latches maintain the logic levels on HLLs that are not pulled up and temporarily are not driven. The logic level maintained is the last level actively driven onto the line.

When using 3-state HLLs for multiplexing, the use of fewer than four TBUFs can waste resources. Multiplexers with four or fewer inputs can be implemented more efficiently using CLBs.

Internal Bus Contention

XC3000 and XC4000 Series devices have internal 3-state bus drivers (TBUFs). As in any other bus design, such bus drivers must be enabled carefully in order to avoid, or at least minimize, bus contention. (Bus contention means that one driver tries to drive the bus High while a second driver tries to drive it Low).

Since the potential overlap of the enable signals is lay-out dependent, bus contention is the responsibility of the FPGA user. We can only supply the following information:

While two internal buffers drive conflicting data, they create a current path of typically 6 mA. This current is tolerable, but should not last indefinitely, since it exceeds our (conservative) current density rules. A continuous contention

could, after thousands of hours, lead to metal migration problems.

In a typical system, 10 ns of internal bus contention at 5 MHz would just result in a slight increase in Icc.

16 bits x 6 mA x 10 ns x 5 MHz x 50% probability = 2.5 mA.

There is a special use of the 3-state control input: When it is directly driven by the same signal that drives the data input of the buffer, i.e. when D and T are effectively tied together, the 3-state buffer becomes an "open collector" driver. Multiple drivers of this type can be used to implement the "wired-AND" function, using resistive pull-up.

In this situation there cannot be any contention, since the 3-state control input is designed to be slow in activating and fast in deactivating the driver. Connecting D to ground is an obvious alternative, but may be more difficult to route.

Vertical Longlines

There are four vertical Longlines per routing channel: two general purpose, one for the global clock net and one for the alternate clock net.

Clock Buffers

XC3000/XC3100 devices each contain two high-fan-out, low-skew clock-distribution networks. The global-clock net originates from the GCLK buffer in the upper left corner of the die, while the alternate clock net originates from the ACLK buffer in the lower right corner of the die.

The global and alternate clock networks each have optional fast CMOS inputs, called TCLKIN and BCLKIN, respectively. Using these inputs provides the fastest path from the PC board to the internal flip-flops and latches. Since the signal bypasses the input buffer, well-defined CMOS levels must be guaranteed on these clock pins.

To specify the use of TCLKIN or BCLKIN in a schematic, connect an IPAD symbol directly to the GCLK or ACLK symbol. Placing an IBUF between the IPAD and the clock buffer will prevent TCLKIN or BCLKIN from being used.

The clock buffer output nets only drive CLB and IOB clock pins. *They do not drive any other CLB inputs.* In rare cases where a clock needs to be connected to a logic input or a device output, a signal should be tapped off the clock buffer input, and routed to the logic input. This is not possible with clocks using TCLKIN or BCLKIN.

The clock skew created by routing clocks through local interconnect makes safe designs very difficult to achieve, and this practice is not recommended. In general, the fewer clocks that are used, the safer the design. High fan-out clocks should always use GCLK or ACLK. If more than two clocks are required, the ACLK net can be segmented into individual vertical lines that can be driven by PIPs at the top and bottom of each column. Clock signals routed through local interconnect should only be considered for individual flip-flops.

Power Dissipation

As in most CMOS ICs, almost all FPGA power dissipation is dynamic, and is caused by the charging and discharging of internal capacitances. Each node in the device dissipates power according to the capacitance in the node, which is fixed for each type of node, and the frequency at which the particular node is switching, which can be different from the clock frequency. The total dynamic power is the sum of the power dissipated in the individual nodes.

While the clock line frequency is easy to specify, it is usually more difficult to estimate the average frequency of other nodes. Two extreme cases are binary counters, where half the total power is dissipated in the first flip-flop, and shift registers with alternating zeros and ones, where the whole circuit is exercised at the clocking speed.

A popular assumption is that, on average, each node is exercised at 20% of the clock rate; a major EPLD vendor uses a 16-bit counter as a model, where the effective percentage is only 12%. Undoubtably, there are extreme cases, where the ratio is much lower or much higher, but 15 to 20% may be a valid approximation for most normal designs. Note that global clock lines must always be entered with their real, and obviously well-known, frequency.

Consequently, most power consumption estimates only serve as guidelines based on gross approximations. Table 4 shows the dynamic power dissipation, in mW per MHz, for different types of XC3000 nodes. While not precise, these numbers are sufficiently accurate for the calculations in which they are used, and may be used for any XC3000/XC3100 device. Table 5 shows a sample power calculation.

Table 4: Dynamic Power Dissipation

	XC3020	XC3090	
One CLB driving three local interconnects	0.25	0.25	mW/MHz
One device output with a 50 pF load	1.25	1.25	mW/MHz
One Global Clock Buffer and line	2.00	3.50	mW/MHz
One Longline without driver	0.10	0.15	mW/MHz

Table 5: Sample Power Calculation for XC3020

Quantity	Node	MHz	mW/MHz	mW
1	Clock Buffer	40	2.00	80
5	CLBs	40	0.25	50
10	CLBs	20	0.25	50
40	CLBs	10	0.25	100
8	Longlines	20	0.10	16
20	Outputs	20	1.25	500
		Total Power ~800		

Crystal Oscillator

XC3000 and XC3100 devices contain an on-chip crystal oscillator circuit that connects to the ACLK buffer. This circuit, Figure 5, comprises a high-speed, high-gain inverting amplifier with its input connected to the dedicated XTL2 pin, and its output connected to the XTL1 pin. An external biasing resistor, R1, with a value of 0.5 to 1 MΩ is required.

A crystal, Y1, and additional phase-shifting components, R2, C1 and C2, complete the circuit. The capacitors, C1 and C2, in series form the load on the crystal. This load is specified by the crystal manufacturer, and is typically 20 pF. The capacitors should be approximately equal: 40 pF each for a 20 pF crystal.

Either series- or parallel-resonant crystals may be used, since they differ only in their specification. Crystals constrain oscillation to a narrow band of frequencies, the width of which is <<1% of the oscillating frequency; the exact frequency of oscillation within this band depends on the components surrounding the crystal. Series-resonant crystals are specified by their manufacturers according to the lower edge of the frequency band, parallel-resonant crystals according to the upper edge.

The resistor R2 controls the loop gain and its value must be established by experimentation. If it is too small, the oscillation will be distorted; if it is too large, the oscillation will fail to start, or only start slowly. In most cases, the value of R2 is non-critical, and typically is 0 to 1 kΩ.

Once the component values have been chosen, it is good practice to test the oscillator with a resistor (~1 kΩ) in series with the crystal. If the oscillator still starts reliably, independent of whether the power supply turns on quickly or slowly, it will always work without the resistor.

For operation above 20 to 25 MHz, the crystal must be operated at its third harmonic. The capacitor C2 is replaced by a parallel-resonant LC tank circuit tuned to ~2/3 of the desired frequency, i.e., twice the fundamental frequency of the crystal. Table 6 shows typical component values for the tank circuit.

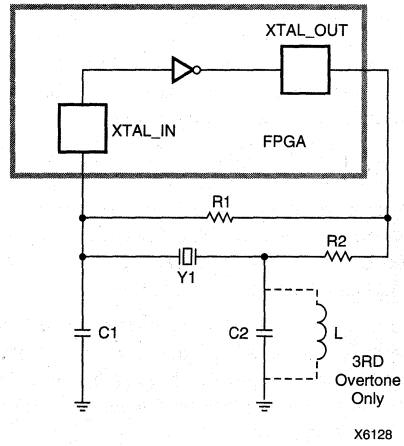


Figure 5: Crystal Oscillator

Table 6: Third-Harmonic Crystal Oscillator Tank-Circuit

Frequency	LC Tank				
(MHz)	L (μH)	C2 (pF)	Freq (MHz)	R2 (Ω)	C1 (pF)
32	1	60	20.6	430	23
35	1	44	24.0	310	23
49	1	31	28.6	190	23
72	1	18	37.5	150	12

Crystal-Oscillator Considerations

There is nothing Xilinx-specific about the oscillator circuit. It's a wide-band inverting amplifier, as used in all popular microcontrollers. When a crystal and some passive components close the feedback path, this circuit becomes a reliable and stable clock source.

The path from XTAL2 to XTAL1 inside the LCA device is a single-stage inverting amplifier, which means it has a low-frequency phase response of 180°, increasing by 45° at the 3-dB frequency.

Input impedance is 10-15 pF, input threshold is CMOS, but dc bias must be supplied externally through a megohm resistor from XTAL1 to XTAL2.

Low-frequency gain is about 10, rolling off 3dB at 125 MHz.

Output impedance is between 50 and 100 Ω and the capacitance on the output pin is 10 to 15 pF.

Pulse response is a delay of about 1.5 ns and a rise/fall time of about 1.5 ns.

For stable oscillation,

- the loop gain must be exactly one, i.e., the internal gain must be matched by external attenuation, and
- the phase shift around the loop must be 360° or an integer multiple thereof. The external network must, therefore, provide 180° of phase shift.

A crystal is a piezoelectric mechanical resonator that can be modeled by a very high-Q series LC circuit with a small resistor representing the energy loss. In parallel with this series-resonant circuit is unavoidable parasitic capacitance inside and outside the crystal package, and usually also discrete capacitors on the board.

The impedance as a function of frequency of this whole array starts as a small capacitor at low frequencies (Figure 6). As the frequency increases, this capacitive reactance decreases rapidly, until it reaches zero at the series resonant frequency.

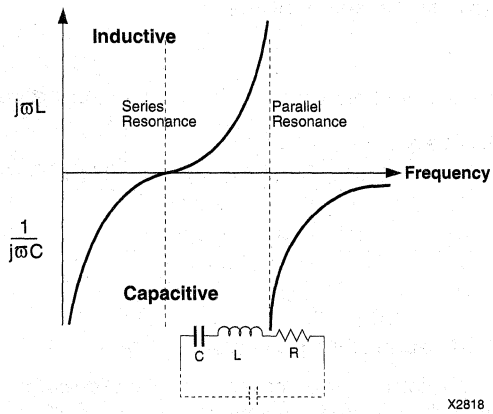


Figure 6: Reactance as a Function of Frequency

At slightly higher frequencies, the reactance is inductive, starting with a zero at series resonance, and increasing very rapidly with frequency. It reaches infinity when the effective inductive impedance of the series LC circuit equals the reactance of the parallel capacitor. The parallel resonance frequency is a fraction of a percent above the series-resonance frequency.

Over this very narrow frequency range between series and parallel resonance, the crystal impedance is inductive and changes all the way from zero to infinity. The energy loss represented by the series resistor prevents the impedance from actually reaching zero and infinity, but it comes very close.

Microprocessor- and FPGA-based crystal oscillators all operate in this narrow frequency band, where the crystal impedance can be any inductive value. The circuit oscillates at a frequency where the attenuation in the external circuit equals the gain in the FPGA device, and where the total phase shift, internal plus external, equals 360°.

Figure 7 explains the function. At the frequency of oscillation, the series-resonant circuit is effectively an inductor, and the two capacitors act as a capacitive voltage divider, with the center-point grounded. This puts a virtual ground somewhere along the inductor and causes the non-driven end of the crystal to be 180° out of phase with the driven end, which is the external phase shift required for oscillation. This circuit is commonly known as a Pierce oscillator.

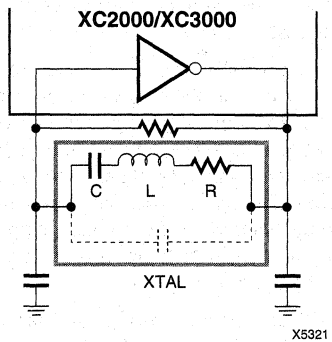


Figure 7: Pierce Oscillator

Practical Considerations

- The series resonance resistor is a critical parameter. To assure reliable operation with worst-case crystals, the user should experiment with a discrete series resistor roughly equal to the max internal resistance specified by the crystal vendor. If the circuit tolerates this additional loss, it should operate reliably with a worst-case crystal without the additional resistor.
- The two capacitors affect the frequency of oscillation and the start-up conditions. The series connection of the two capacitors is the effective capacitive load seen by the crystal, usually specified by the crystal vendor.
- The two capacitors also determine the minimum gain required for oscillation. If the capacitors are too small, more gain is needed, and the oscillator may be unstable. If the capacitors are too large, oscillation is stable but the required gain may again be higher. There is an optimum capacitor value, where oscillation is stable, and the required gain is at a minimum. For most crystals, this capacitive load is around 20 pF, i.e., each of the two capacitors should be around 40 pF.
- Crystal dissipation is usually around 1 mW, and thus of no concern. Beware of crystals with "drive-level dependence" of the series resistor. They may not start up. Proper drive level can be checked by varying Vcc. The frequency should increase slightly with an increase in Vcc. A decreasing frequency or unstable amplitude indicate an over-driven crystal. Excessive swing at the

XTAL2 input results in clipping near Vcc and ground. An additional 1 to 2 kΩ series resistor at the XTAL1 output usually cures that distortion problem. It increases the amplifier output impedance and assures additional phase margin, but results in slower start-up.

- Be especially careful when designing an oscillator that must operate near the specified max frequency. The circuit needs excess gain at small signal amplitudes to supply enough energy into the crystal for rapid start-up. High-frequency gain may be marginal, and start-up may be impaired.
- Keep the whole oscillator circuit physically as compact as possible, and provide a single ground connection. Grounding the crystal can is not mandatory but may improve stability.

Series Resonant or Parallel Resonant?

Crystal manufacturers label some crystals as series-resonant, others as parallel-resonant, but there really is no difference between these two types of crystals, they all operate in the same way. Every crystal has a series resonance, where the impedance of the crystal is extremely low, much lower than at any other frequency. At a slightly higher frequency, the crystal is inductive and in parallel resonance with the unavoidable stray capacitance or the deliberate capacitance between its pins.

The only difference between the two types of crystal is the manufacturer's choice of specifying either of the two frequencies. If series resonance is specified, the actual frequency of oscillation is a little higher than the specified value. If parallel resonance is specified, the frequency of oscillation is a little lower. In most cases, these small deviations are irrelevant.

CCLK Frequency Variation

The on-chip R-C oscillator that is brought out as CCLK also performs several other internal functions. It generates the power-on delay, 2^{16} = 65,536 periods for a master, 2^{14} = 16,384 periods for a slave or peripheral device. It generates the shift pulses for clearing the configuration array, using one clock period per frame, and it is the clock source for several small shift registers acting as low-pass filters for a variety of input signals.

The nominal frequency of this oscillator is 1 MHz with a max deviation of +25% to -10%. The clock frequency, therefore, is between 1.25 MHz and 0.5 MHz. In the XC4000 family, the 1-MHz clock is derived from an internal 8-MHz clock that also can be used as CCLK source.

Xilinx circuit designers make sure that the internal clock frequency does not get faster as devices are migrated to smaller geometries and faster processes. Even the newest and fastest Xilinx FPGA is compatible with the oldest and slowest device ever manufactured. The CCLK frequency is fairly insensitive to changes in V_{CC}, varying only 0.6% for a 10% change in V_{CC}. It is, however, very temperature dependent, increasing 40% as the temperature drops from 25°C to -30°C, (Table 7.)

Table 7: Typical CCLK Frequency Variation

V_{CC}	Temp	Frequency
4.5 V	25°C	687 kHz
5.0 V	25°C	691 kHz
5.5 V	25°C	695 kHz
4.5 V	-30°C	966 kHz
4.5 V	+130°C	457 kHz

CCLK Low-Time Restriction

When used as an input in Slave Serial and Readback modes, CCLK does not tolerate a Low time in excess of 5 µs. For very low speed operation, the CCLK High time can be stretched to any value, but the Low time must be kept short. XC4000 and XC5200 devices do not have this restriction.

Battery Back-up

Since SRAM-based FPGAs are manufactured using a high-performance low-power CMOS process, they can preserve the configuration data stored in the internal static memory cells even during a loss of primary power. This is accomplished by forcing the device into a low-power non-operational state, while supplying the minimal current requirement of V_{CC} from a battery.

Circuit techniques used in XC3100, XC4000 and XC5200 devices prevent I_{CC} from being reduced to the level need for battery back-up. Consequently, battery back-up should only be used for XC2000, XC2000L, XC3000, XC3000A and XC3000L devices.

There are two primary considerations for battery backup which must be accomplished by external circuits.

- Control of the Power-Down ($\overline{PWRDWN}$) pin
- Switching between the primary V_{CC} supply and the battery.

Important considerations include the following.

- Insure that $\overline{PWRDWN}$ is asserted logic Low prior to V_{CC} falling, is held Low while the primary V_{CC} is absent, and returned High after V_{CC} has returned to a normal level. $\overline{PWRDWN}$ edges must not rise or fall slowly.
- Insure "glitch-free" switching of the power connections to the FPGA device from the primary V_{CC} to the battery and back.
- Insure that, during normal operation, the FPGA V_{CC} is maintained at an acceptable level, 5.0 V ± 5% (±10% for Industrial and Military).

Figure 8 shows a power-down circuit developed by Shel Epstein of Epstein Associates, Wilmette, IL. Two Schottky diodes power the FPGA from either the 5.2 V primary supply or a 3 V Lithium battery. A Seiko S8054 3-terminal power

monitor circuit monitors V_{CC} and pulls $\overline{PWRDWN}$ Low whenever V_{CC} falls below 4 V.

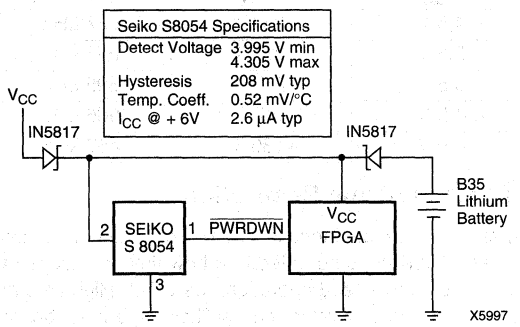


Figure 8: Battery Back-up Circuit

Powerdown Operation

A Low level on the PWRDWN input, while Vcc remains higher than 2.3 V, stops all internal activity, thus reducing Icc to a very low level:

- All internal pull-ups (on Long lines as well as on the I/O pads) are turned off.
- The crystal oscillator is turned off
- All package outputs are three-stated.
- All package inputs ignore the actual input level, and present a High to the internal logic.
- All internal flip-flops or latches are permanently reset.
- The internal configuration is retained.
- When PWRDWN is returned High, after V_{CC} is at its nominal value, the device returns to operation with the same sequence of buffer enable and D/$\overline{P}$ as at the completion of configuration.

Things to Remember

Powerdown retains the configuration, but loses all data stored in the device. Powerdown three-states all outputs and ignores all inputs. No clock signal will be recognized, and the crystal oscillator is stopped. All internal flip-flops and latches are permanently reset and all inputs are interpreted as High, but the internal combinatorial logic is fully functional.

Things to Watch Out For

Make sure that the combination of all inputs High and all internal flip-flop outputs Low in your design will not generate internal oscillations or create permanent bus contention by activating internal bus drivers with conflicting data onto the same Longline. These two situations are farfetched, but they are possible and will result in considerable power consumption. It is quite easy to simulate these conditions since all inputs are stable and the internal logic is entirely combinatorial, unless latches have been made out of function generators.

During powerdown, the Vcc monitoring circuit is disabled. It is then up to the user to prevent Vcc dips below 2.3 V, which would corrupt the stored configuration.

During configuration, the PWRDWN pin must be High, since configuration uses the internal oscillator. Whenever Vcc goes below 4 V, PWRDWN must already be Low in order to prevent automatic reconfiguration at low Vcc. For the same reason, Vcc must first be restored to 4 V or more, before PWRDWN can be made High.

PWRDWN has no pull-up resistor. A pull-up resistor would draw supply current when the pin is Low, which would defeat the idea of powerdown, where Icc is only microamperes.

Configuration and Start-up

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This means a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic "wakes up" gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset or Set at the right time.

Figure 10 describes Start-up timing for the XC3000 families in detail.

DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 11, but the designer can modify it to meet particular requirements.

Until the chip goes active after configuration, all I/O pins not involved in the configuration process remain in a high-impedance state with weak pull-up resistors; all internal flip-flops and latches are held reset. Multiple FPGA devices hooked up in a daisy chain will all go active simultaneously

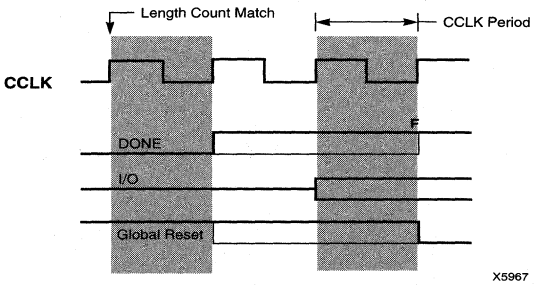


Figure 9: Start-up Timing

on the same CCLK edge. This is well documented in the data sheets.

Not documented, however, is how the internal combinatorial logic comes alive during configuration: As configuration data is shifted in and reaches its destination, it activates the logic and also "looks at" the IOB inputs. Even the crystal oscillator starts operating as soon as it receives its configuration data. Since all flip-flops and latches are being held reset, and all outputs are being held in their high-impedance state, there is no danger in this "staggered awakening" of the internal logic. The operation of the logic prior to the end of configuration is even useful; it ensures that clock enables and output enables are correctly defined before the elements they control become active.

Once configuration is complete, the FPGA device is activated. This occurs on a rising edge of CCLK, when all outputs and clocks that are enabled become active simultaneously. Since the activation is triggered by CCLK, it is an asynchronous event with respect to the system clock. To avoid start-up problems caused by this asynchronism, some designs might require a reset pulse that is synchronized to the system clock.

The circuit shown in Figure 10 generates a short Global Reset pulse in response to the first system clock after the end of configuration. It uses one CLB and one IOB, and also precludes the use of the $\overline{LDC}$ pin as I/O.

During Configuration, $\overline{LDC}$ is asserted Low and holds the D-input of the flip-flop High, while Q is held Low by the internal reset, and $\overline{RESET}$ is kept High by internal and external pull-up resistors. At the end of configuration, the $\overline{LDC}$ pin is unasserted, but D remains High since the function generator acts as an R-S latch; Q stays Low, and $\overline{RESET}$ is still pulled High by the external resistor. On the first system clock after configuration ends, Q is clocked High, resetting the latch and enabling the output driver. which forces $\overline{RESET}$ Low. This resets the whole chip until the Low on Q permits $\overline{RESET}$ to be pulled High again.

The whole chip has thus been reset by a short pulse instigated by the system clock. No further pulses are generated, since the High on $\overline{LDC}$ prevents the R-S latch from becoming set.

Beware of a Slow-Rising XC3000 Series RESET Input

It is a wide-spread habit to drive asynchronous $\overline{RESET}$ inputs with a resistor-capacitor network to lengthen the reset time after power-on. This can also be done with Xilinx FPGAs, but the user should question the need, and should beware of certain avoidable problems.

Xilinx FPGAs contain an internal voltage-monitoring circuit, and start their internal housekeeping operation only after V_{CC} has reached ~3.5 V. The internal housekeeping and configuration memory clearing operation then takes between about 10 and 100 ms, depending on configuration mode and processing variations. Any RC delay shorter than 40 ms for a device in master configuration mode, or shorter than 10 ms for a device in slave configuration mode, is clearly redundant.

A significantly longer RC delay can be used to hold off configuration. Without the use of an external Schmitt trigger circuit, the rise time on the $\overline{RESET}$ input will be very slow, and is likely to cross the threshold of ~1.4 V several times, due to external or internal noise. This can cause the FPGA to start configuration, then immediately abort it, then start it again, after having automatically cleared the configuration memory once more.

This is no problem for the FPGA, but it requires that the source of configuration data, especially an XC1700 serial PROM, be reset accordingly. This is another reason to use the $\overline{INIT}$ output of the lead FPGA, instead of $\overline{LDC}$, to drive the $\overline{RESET}$ input of the XC1700 serial PROMs.

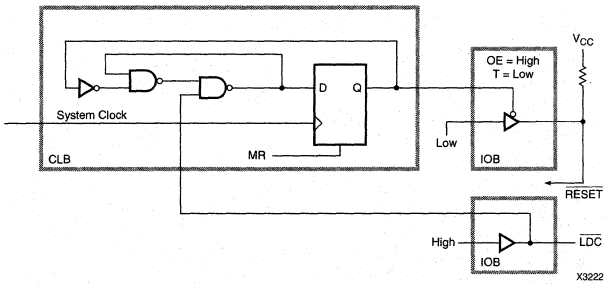


Figure 10: Synchronous Reset

FPGA Configuration Guidelines

June 1, 1996 (Version 1.0)

Application Note By PETER ALFKE

Summary

These guidelines describe the configuration process for XC2000, XC3000 and XC4000-Series FPGA devices. The average user need not understand all details, but should refer to the debugging hints when problems occur.

The XC2000, XC3000, and XC4000 series FPGAs share a basic configuration concept, and can be combined in a common configuration bitstream, but there are small differences among the three families as described below.

Following their initial power-on configuration-memory initialization, these Xilinx FPGAs are configured by a serial configuration bitstream. The byte-parallel configuration modes just activate an internal parallel-to-serial converter, and then use the serial bitstream internally. Express mode in XC4000EX operates on 8 bits in parallel. This mode is not covered in this application note. The software generates a bitstream that starts with a 40-bit header, see Figure 1.

Each device uses a few of the leading 1s to prepare for configuration, then detects the 0010 pattern and stores the following 24 bits as a length-count value in an internal register. The content of this register is continuously compared against a running counter that increments on every rising CCLK edge. CCLK is either an output (in Master and Asynchronous Peripheral modes) or an input (in Slave Serial and Synchronous Peripheral modes). In all modes, it is the externally observable Low-to-High transition on the CCLK pin that causes the internal action. Every CCLK rising edge that occurs while $\overline{\text{INIT}}$ and $\overline{\text{RESET}}$ are High is counted, even during the preamble. Note that XC2000 and XC3000 use quasi-static circuitry which imposes a 5 µs max limit on the CCLK Low time, while XC4000 is completely static and has no max CCLK time limit. This is, of course, only of interest in XC2000 and XC3000 Slave Serial mode, where CCLK is generated by the user.

While it is permissible, although not meaningful, to modify the number of leading ones by adding additional ones, or subtracting up to four ones, this would inevitably affect the number of CCLK pulses received by the counter, and thus change the moment when the internal counter is equal to the value stored in the length-count register. ***Don't add or delete preamble-leading ones!***

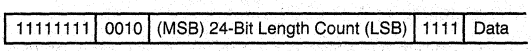


Figure 1: 40-Bit Header

Each device passes the incoming header, including the length-count value, on to the DOUT pin, delayed by half a CCLK period, i.e. the bits are clocked out on a falling CCLK edge. In this way, the header is passed on to all devices that might be connected in a daisy-chain. After the length-count data has been passed on, DOUT goes active High and stays High until the device has been filled with the appropriate number of configuration frames. After that, DOUT again passes all incoming configuration data on to other devices that might be part of the daisy chain.

DOUT is thus the best observation point to see whether the configuration process has started properly.

Immediately following the header, configuration data is received, formatted in a device-specific sequence of frames. Each frame starts with a single 0 as start bit, followed by a device-specific number of configuration bits per frame, followed by three 1s as stop bits (XC2000, XC3000) or, in XC4000, by four bits that are either 0110, or four bits of a running 16-bit CRC error-checking code. (The choice is made in Makebits, where the default is "CRC disabled"). The header is not included in the CRC calculation.

Each frame is physically shifted into a serial shift register that had been preset to all ones. When the zero start bit hits the far end of this shift register, the data frame is transferred in parallel into the configuration memory, as addressed by the position of an internal token or pointer. The three stop or four error-check bits provide ample time for this transfer, even at the 10 MHz CCLK rate allowed for XC3000 and XC4000 devices. After this transfer, the shift-in procedure continues with the following frame. Note that there is no counter for the number of bits in the frame or for the number of frames. The operation is self-synchronized by detecting the presence of a start bit at the far end of the shift register, and by moving the frame pointer.

Each Xilinx FPGA requires a number of configuration bits that is device-dependent, but independent of the configuration content, and independent of the configuration mode. The number of configuration bits per device varies from 12,038 for the XC2064 to 422,168 for the XC4025, roughly 20 bits per gate. The exact numbers of configuration bits are listed in the specific family data sheets.

Protection Against Data or Format Errors

The serial configuration scheme has proven reliable in thousands of designs and millions of devices, but there have been cases where an erroneous bitstream was loaded accidentally. The original XC2000 and XC3000 devices provide no effective protection against this type of error. If long enough, any random sequence of 0s and 1s will configure a device. This inevitably takes more CCLK pulses than specified in the length-count value. This means that the CCLK counter equals the length-count value before the FPGAs are filled. This comparison is, therefore, ignored, and an additional 16 million CCLK pulses are required to roll the 24-bit length counter and finish the configuration. Such a configuration will, of course, be wrong and might result in excessive power consumption due to internal or external contentions.

XC3000A, XC3100A, XC3000L and XC3100L devices use a simple and effective method to protect against erroneous configuration files or against loss (or gain) of CCLK pulses:

All Xilinx FPGA devices recognize a new frame when its leading zero reaches the end of the shift register. XC2000, XC3000, and XC3100 devices do not check for the presence of valid stop bits, but XC3000A/XC3100A/XC3000L/XC3100L devices always check whether the three bits at the end of the defined frame length are 111. If this check fails, $\overline{\text{INIT}}$ is pulled Low and the internal configuration is stopped, although a master CCLK keeps running. The user must recognize this state and start a new configuration by applying a >6 µs Low level on $\overline{\text{RESET}}$.

This simple check does not protect against single-bit random errors, but it offers almost 100% protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, as well as PC-board defects, such as broken lines or solder bridges.

The XC4000 series uses, optionally, four bits of a running 16-bit cyclic redundancy check code at the end of each frame, combined with additional CRC bits at the end of the bit stream. These error-detecting CRC codes provide excellent protection against errors, even those that do not change the frame structure. When an error is detected, $\overline{\text{INIT}}$ goes Low and stays Low until the user initiates a reconfiguration. (A master device does, however, continue generating CCLK pulses and incrementing or decrementing the parallel PROM address).

Daisy-Chain Operation

Multiple FPGAs can be configured by a single concatenated bitstream. The device daisy chain is formed by connecting DOUT to the next device's DIN, and connecting all CCLK pins in parallel. Since DOUT goes active on a falling clock edge, and DIN is used on the subsequent rising clock edge, each DOUT-to-DIN connection adds one extra bit of delay to the bitstream. Since the header is passed through all devices, they all receive this information almost simultaneously (staggered by one bit per device), but all devices maintain perfect synchronism between their CCLK counters.

Xilinx recognizes the need for all devices in a daisy chain to finish their configuration and begin user operation simultaneously, as a result of one common CCLK edge. Therefore, all devices in a daisy-chain need a common timing reference. They cannot rely on the start pattern received through the pipelined chain, but must all count the common CCLK pulses exactly the same way. This explains the importance of well-defined configuration clocking.

Start-Up Procedure

The transition from configuration to user operation faces several difficulties. During configuration, all outputs that are not involved in the configuration process are 3-stated, although the crystal oscillator circuit is activated as soon as possible. All internal flip-flops and latches are held reset (set or reset in XC4000), and the DONE output is held Low.

At the end of configuration, these three conditions must change: As shown in detail in Figure 2, the three families offer different options:

XC2000 has no options; the I/Os go active one CCLK period after length-count match. DONE goes active and the global reset is released one CCLK period later.

XC3000 makes the I/Os go active two CCLK periods after length-count match; but DONE and the release of the global reset can each occur either one CCLK period before or after the I/Os go active. The default is "early DONE and late release of the global reset". This makes the outputs go active while the internal logic is still held reset. The other Makebits option, "early release of global reset", lets the internal logic be clocked out of its reset state before the outputs go active.

Normally, there is no defined timing relationship between the last configuration events triggered by the rising edge of CCLK, and the subsequent events that are controlled by the system clock. The user must be aware of the potential problems of this asynchronous relationship. See the XC4000 solution described below.

XC4000 has more options for the relative timing of I/Os, DONE and GSR, the release of the global set or reset.

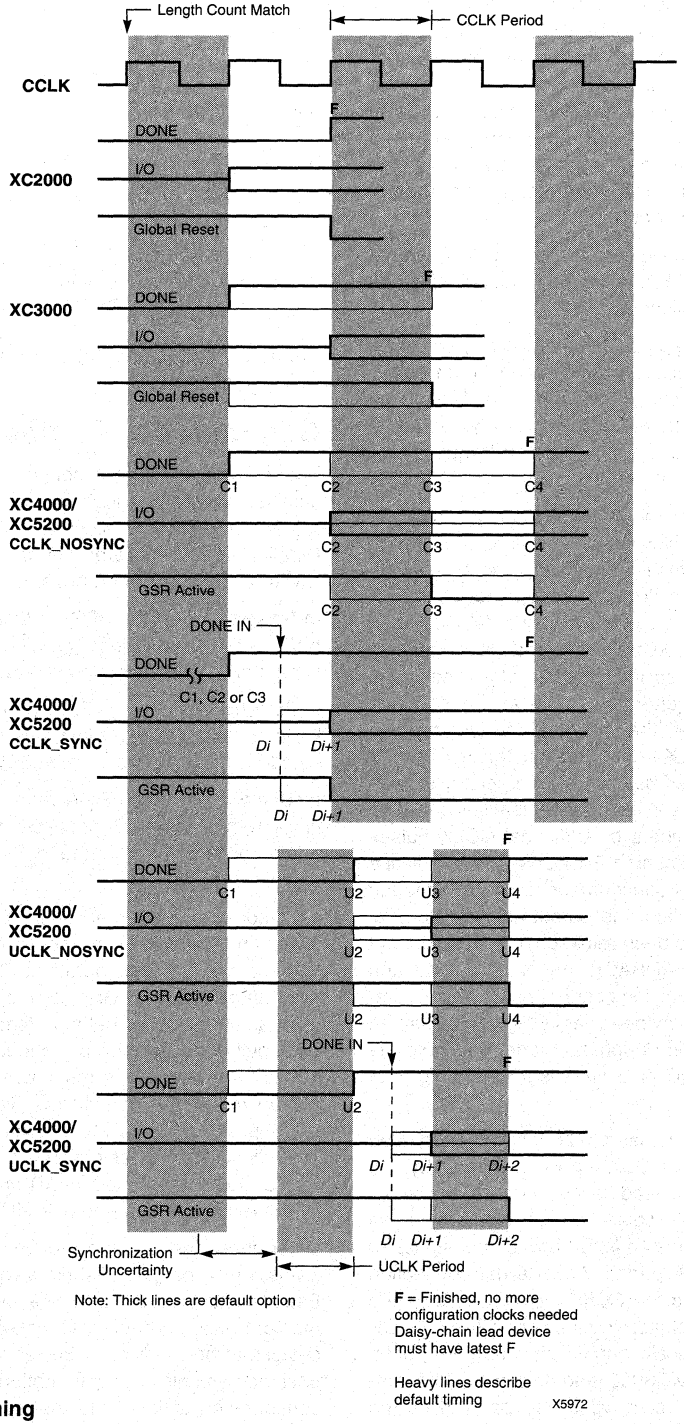


Figure 2: Start-up Timing

XC4000 can also use DONE as an input to hold off the activation of the I/Os and the release of GSR, until DONE is no longer pulled Low. The change then takes place either immediately upon the release of DONE, or as a result of the next CCLK rising edge. When all DONE pins in a daisy chain are interconnected, this start-up mode guarantees that all devices in the daisy chain will go active only when all of them have reached the DONE state, another protection against configuration errors.

XC4000 can also be configured to employ the system (user) clock instead of CCLK, again either using DONE as an output, or as a bidirectional pin.

The user clock provides a properly synchronized and race-free transition from the end of configuration to the beginning of user operation. The unspecified on-chip delay in the release of GSR (about 100 ns in XC4013) requires some caution, however, when using a high clock frequency for configuration.

While XC2000, XC3000, and XC4000 can be arbitrarily interspersed in a daisy-chain, there is one restriction: the lead device must belong to the highest family in the chain. If the chain contains XC4000 devices, the lead device cannot be XC2000 or XC3000; if the chain contains XC3000, then the lead device cannot be XC2000. The reason is shown in Figure 2. Since all devices in the chain store the same length-count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge. The master device then generates additional CCLK pulses until it reaches its finish point F. As shown in Figure 2, the different families generate and require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device has not really finished its configuration process, although DONE may have gone High, the outputs became active, and the internal reset has been released. For XC4000, not reaching F means that READBACK cannot be initiated, and most boundary scan instructions cannot be used. This limitation has been criticized by designers who want to use an inexpensive lead device in Peripheral Mode, and save the more precious XC4000 I/O pins. Here is a solution for that case (Figure 3):

One CLB and one IOB in the lead XC3000 device are used to generate the additional CCLK pulse required by the XC4000 devices. When the lead device releases its internal reset signal, the 2-bit shift register starts responding to its clock input, and it generates an active Low output signal for the duration of one clock period. An external connection between this IOB pin and the CCLK pin thus creates the extra CCLK pulse. This solution requires one CLB, one IOB and pin, and an internal clock source with a frequency of up to 5 MHz. Obviously, the XC3000 lead device must be configured with late internal reset, which happens to be the default option.

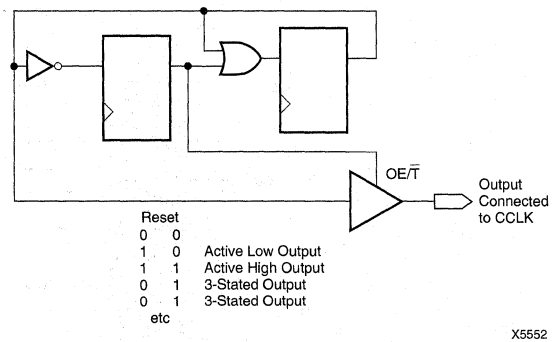


Figure 3: Additional CCLK-Pulse Generator

Configuration Modes

There are six different configuration modes, hardware-selected by applying logic levels to the three mode inputs, M0, M1, and M2. The six modes are: Master Serial, Master Parallel Up, Master Parallel Down, Synchronous Peripheral (XC4000 only), Asynchronous Peripheral, and Slave Serial.

In **Master** modes, the FPGA addresses an external PROM or EPROM storage device, and reads data from it. No additional timing or control signals are used.

In **Peripheral** mode, the FPGA accepts byte-wide data (bit-serial in XC2000), and interacts with the source of data, usually a microprocessor, with a Ready/Busy handshake.

In **Slave** mode, the FPGA receives bit-serial data and a clock from an external data and timing source, either from a microprocessor, or from the lead device in an FPGA-daisy chain.

The modes are selected by putting the appropriate logic levels on the three mode inputs, M0, M1, and M2 prior to the beginning of configuration. These three pins can be hardwired to V_{CC} or Ground, but they can then never be used as user I/O. It is better to force a mode pin Low with a 3 kΩ pull-down resistor to ground, acting against the 50 to 100 kΩ internal pull-up resistor, and to rely on the built-in pull-up resistor to establish a High level on the M1, M2 mode pins, and a 50 kΩ external pull-up resistor on M0. This eliminates the restrictions on using M2 as logic output on XC2000 and XC3000, or M1 on XC4000, and the use of M1 as readback data output in XC2000 and XC3000.

When mode pin levels are driven by external logic, these levels must be established very soon after power-up. Establishing a mode level later might eliminate the extra master power-on delay that makes a master wait for slave devices to be ready after power-on. Delaying mode levels until the beginning of configuration will obviously cause the configuration to fail. Note that some EPLD devices have surprisingly long power-up delays. Be very careful when controlling mode levels in creative ways.

Selecting the Best Configuration Mode

The selection of the most appropriate configuration mode is influenced by many factors, like

- the need for interface simplicity,
- the need for rapid configuration,
- the need for multiple configuration sources,
- the availability of a microprocessor-based configuration driver.

The simplest interface is Master Serial, using only two FPGA pins, CCLK and DIN, and no external timing or control signals.

The fastest configuration mode is Slave Serial or XC4000 Synchronous Peripheral. In these modes, the user can supply a well-defined CCLK frequency of up to 10 MHz for all XC3000 and XC4000 5-Volt devices. No other configuration mode is that fast. For prototyping and rapid configuration change, the PC can configure the FPGA directly in Slave Serial mode, using the Xilinx-provided Download Cable or XChecker.

Multiple configuration codes are most conveniently stored in a microprocessor memory, using Peripheral mode to configure the FPGA. For field upgrades, Peripheral mode offers the greatest flexibility. New files can be supplied via diskette or modem, and can be downloaded by the microprocessor.

When Configuration Fails

General Debugging Hints for all Families

If the DONE output does not go High, there are several things to check.

- Checking all supply and configuration-related pins with an oscilloscope or logic analyzer can reveal wiring errors, bad socket pins, noisy ground, noisy CCLK, a serial configuration PROM V_{PP} pin not connected to V_{CC}, $\overline{PWRDWN}$ not pulled High, poor or noisy $\overline{RESET}$, missing pull-up resistors on DONE (or $\overline{INIT}$ in the XC3000), etc.
- Monitor the DOUT pin of the lead device, i.e. the FPGA that is either configured alone, or forms the beginning of a daisy chain. At the start of configuration, you should see the 40-bit header shown in Figure 1. After this sequence, the DOUT pin remains High until the device has received all its data. Then, the device becomes transparent and passes additional data (provided there is a daisy chain) through the DOUT pin to the Slave devices. If you don't see this pattern, you have a gross error somewhere. Check the following items:
- $\overline{INIT}$ going Low again after configuration start indicates a configuration bitstream or framing error in XC3000A, XC3000L or XC4000 families.
- If $\overline{RESET}$ is used to delay configuration, make sure it has a rise time of <100 ns and that it is glitch-free.
- Ringing on the CCLK line can cause spurious clocking and loss of frame synchronization in the FPGA.
- Configuration functions can be disrupted by signal contention between configuration inputs and the FPGA user outputs which become active at the end of configuration. This change is indicated by I/O pins going active and HDC/$\overline{LDC}$ no longer at their configuration levels. Contention can be avoided by rearranging pin-outs, maintaining additional 3-state control of user-I/O outputs, or matching start-up output levels to the configuration input levels on inputs other than chip-select. It is also possible to use a series resistor (1-10 kΩ) to provide isolation between conflicting signal sources that could occur after configuration is complete.
- If an FPGA heats up significantly, this is usually the result of applying the wrong bitstream, e.g. the bitstream for a different device, causing contention.
- During reprogramming, user logic must generate a time-out that insures all devices have completed the Clear cycle before any configuration data is sent.
- Removing the FPGA supply voltage while externally powered signals continue to drive input pins, might keep the FPGA V_{CC} pins at a 0.5-to-2.0 V level, which can leave the FPGA in an invalid state. The FPGA input-protection diodes are there to clamp input-voltage excursions to the two supply connections. When the FPGA supply voltage falls more than 0.5 V below an active input signal, this input signal will supply degenerate V_{CC} levels. If the input signals are not current-limited, the FPGA inputs can even be damaged by the excessive input current.
- If extraneous CCLK pulses are applied after Clear but before the beginning of the header, the internal clock count will equal the stored length-count value before the configuration data is completely loaded. In this case, the DONE output does not become active until the clock counter equals length count a second time. This requires 2^{24} extra clocks, or about 20 s at the typical rate of 0.7 MHz.

Whenever configuration takes 15 to 25 seconds, this is due to a mismatch between length count and the number of CCLK pulses received.

- XChecker or the XACT Download Cable provide an alternate method of configuration to verify configuration data and to isolate wiring errors, such as interchanged or inverted configuration data or control signals.
- Try a different device. Although the chips are 100% factory-tested, an individual device might have been damaged later.

General Debugging Hints for the XC2000 and XC3000 Families

- An undefined (floating) or active Low $\overline{\text{PWRDWN}}$ during configuration can disturb the operation. A Low level on $\overline{\text{PWRDWN}}$ immediately before the start of configuration causes problems in XC2000, forces XC3000 into Slave mode, but is acceptable in XC3000A and L.
- In the XC2000 and XC3000 families, the configuration-clock input signal drives quasi-static circuitry that does not tolerate a Low time of more than 5 µs.
- At power-up, make sure V_{CC} rises in 25 ms or less. If this cannot be guaranteed, hold $\overline{\text{RESET}}$ active on the FPGAs and on the serial PROMs until V_{CC} has reached 4.5 V.
- A slowly rising or noisy $\overline{\text{RESET}}$ can cause multiple FPGAs to get out of synchronization. Always debounce reset switches.

General Debugging Hints for the XC4000 Family

- At power-up, make sure V_{CC} rises in 25 ms or less. If this cannot be guaranteed, hold $\overline{\text{PROGRAM}}$ or $\overline{\text{INIT}}$ active Low on the FPGAs and hold the serial PROMs reset until V_{CC} has reached 4.5 V.
- The boundary scan input pins are active during configuration, even if boundary scan is not used in the design. Toggling TCK, TMS and TDI during configuration might send the device into EXTEST mode, which interferes with configuration. Keeping at least one of these three inputs continuously High during configuration avoids this problem.

Additional Mode-Specific Debugging Hints for All Families

Master Parallel Up and Down Mode

- Review the general debugging hints.
- Check that the PROM data pins are connected to the FPGA input pins D0-D7. Check that the PROM address pins are connected to the FPGA output pins A0-A15. Verify that all these connections are in the right order. Monitor the FPGA pins, not the socket pins. Make sure the socket is good.
- If the PROM is dedicated to the FPGA, the $\overline{\text{CS}}$ and $\overline{\text{OE}}$ PROM inputs should be driven from the DONE or $\overline{\text{LDC}}$ FPGA output.
- Verify that the FPGA is sending addresses to the PROM. If it is not, check the FPGA mode pins.

  M0 = 0, M1 = 0, M2 = 1 for Master Parallel Up
  M0 = 0, M1 = 1, M2 = 1 for Master Parallel Down

  Make sure V_{CC}, $\overline{\text{RESET}}$ and $\overline{\text{PWRDWN}}$ are at 5 V and all ground pins are at 0 V.
- Check that the PROM is receiving addresses and is sending out data. If it is not, check that the PROM is enabled and has V_{CC} and ground connected, and verify that the PROM is programmed with the correct data.
- Check for contention between the PROM address or data pins and other signals on the board.
- Check that the FPGA is addressing the correct memory segment. In Master Parallel Up mode, the FPGA starts at address 0000 hex and counts up; in Master Parallel Down mode it starts at address FFFF hex (3FFFF hex in XC4000) and counts down. If the PROM requires different addressing, that must be taken care of by external hardware.
- Check for ringing and noise on address and data lines.
- Make sure the data in the PROM is correct. You can check it against the Rawbits file.

Master Serial Mode

- Review the general debugging hints.
- Verify that the FPGA is generating a clock signal on its CCLK pin and that this signal is reaching the CLK pin of the XC1700-series Serial-Configuration PROM. If it is not, check the mode pins.

  M0 = 0, M1 = 0, M2 = 0 for Master Serial mode

- Verify that the XC1700-series Serial Configuration PROM is sending data. If it is not, check that power and ground are applied to the Serial PROM, and V_{PP} is connected to V_{CC}.

Do Not Let the V_{PP} Pin Float

A floating VPP pin results in temperature-dependent operation, the most notorious cause of unreliable configuration.

- Check that the DATA pin of the Serial PROM is connected to the DIN pin of the FPGA, and that the PROM is enabled with $\overline{\text{CE}}$ Low and OE active. Note that the OE/RESET pin is programmable for either polarity.
- Verify that the PROM is programmed with the correct data.
- At power-up, make sure V_{CC} rises from 2.0 V to 4.5 V in less than 25 ms. If it does not, hold the FPGA RESET and the PROM RESET active until V_{CC} reaches 4.5 V. A typical result of a slow V_{CC} rise time is that the FPGA sends out CCLK continuously, the $\overline{\text{CEO}}$ pin on the PROM(s) goes Low, but the DONE pin never goes High.
- If you abort configuration by asserting XC3000 $\overline{\text{RESET}}$ or by pulling XC4000 PROGRAM Low, you must also reset the serial PROM by asserting its RESET. Note that this pin can be programmed for either polarity.

Asynchronous Peripheral Mode

- Review the general debugging hints.
- Check the mode pin levels.

  M0 = 1, M1 = 0, M2 = 1 for Peripheral mode

- See schematics on pages 2-40 and 2-128.
- Verify that the FPGA is receiving data at its input pin(s) and that it is receiving valid Write-Strobe and Chip-Select signals. If not, check the device driving the FPGA. Make sure that these signals meet the timing requirements listed in the product family documentation.
  XC3000 Family: Check that the minimum Write-Strobe active time (T_{CA} min = 100 ns) is met and observe the RDY/$\overline{BUSY}$ signal.
  XC2000 Family: Be sure maximum and minimum Write-Strobe active times (T_{CA} max = 5.0 µs, min = 0.25 µs) are met.
- Make sure that the FPGA is ready to receive data.
  XC3000 Family: On power up, make sure that the $\overline{INIT}$ pin has gone High, or wait at least 34 ms before you begin sending data to the FPGA. Make sure that the RDY/$\overline{BUSY}$ signal is High before sending each data byte.
  XC2000 Family: On power up, make sure that the FPGA has had time to "wake up," at least 34 ms, before sending it data.
- Check for contention between the Chip Select and Write Strobe signals and monitor the levels on those pins after configuration. It is best to use the Chip Select pins only as inputs after configuration. Avoid contention if they are used as outputs. With XC2000 family devices, the I/Os become active before the FPGA receives its final data bits and clocks, and also before the DONE pin goes High. If the user function for any of the Chip Selects or the Write Strobe become outputs after configuration, they could contend and, in effect, de-select the FPGA so that it never receives its final data bits. See also next page, left column. ***Beware of contention!***
- Check for contention between the FPGA pins and other signals on the board.
  XC4000 and XC3000 Families: Data is received as eight bits in parallel. Make sure bit 0 is connected to the D0 pin, bit 1 to D1 pin, etc.
  XC2000 Family: Data is received serially. If a PROM file is used as a data source, check that data is properly serialized LSB first. Data must be LSB first, although length count is MSB first.

Slave Serial Mode

- Review the general debugging hints.
- Check the mode pin levels.

  M0 =1, M1 = 1, M2 = 1 for Slave Serial mode

- See schematics on pages 2-35 and 2-130.
- Make sure Vcc, $\overline{RESET}$, and $\overline{PWRDWN}$ are at 5 V, and ground pins are at 0 V.
- Verify that the FPGA is receiving data on DIN and that it is receiving a valid clock signal on CCLK.
  Check the device sending the data.
  Check the device sending the clock signal, and make sure the clock meets the timing requirements specified in the product family documentation. A CCLK generated by a Master FPGA always meets the timing requirements.
  Don't violate the XC3000 and XC2000 CCLK Low time specification of 5.0 µs.
- Make sure the FPGA is ready to receive data.
  XC3000 Family: On power up, make sure the $\overline{INIT}$ pin is High or wait at least 34 ms before you begin sending data to the FPGA.
  XC2000 Family: On power up, make sure that the FPGA has had time to "wake up" at least 34 ms, before sending it data.
- At power up, make sure V_{CC} rises from 2.0 V to 4.5 V in less than 25 ms. If it does not, hold $\overline{RESET}$ Low until the V_{CC} pins reach 4.5 V.

Daisy Chain Debugging Hints

- The key to debugging daisy-chain configurations is to isolate the problem and attempt to configure a single FPGA. Remove all but the first device from the board and configure it. Then insert the second device and configure both. Repeat as you add one device at a time until they all configure.
- The first device in the chain can be in any of the configuration modes. Debug it first, using the hints provided for the appropriate mode.
- All devices after the first one are in Slave Serial mode, so refer to the Slave Serial mode debugging hints above to solve any problems with Slave device.
- Monitor the DOUT pin of each device in the chain and verify that the 40-bit header appears at the beginning of configuration, staggered by one CCLK period per device.
- If the Master device in the chain is an XC2000-family device and the Slaves are XC3000-family, make sure the XC3000-family devices are configured with early DONE.

Potential Length-Count Problem in Parallel or Peripheral Modes

It is highly desirable that the complete change from configuration to user operation occur as the result of one single byte-wide input. The activation of outputs and DONE, the de-activation of the global reset (set/reset in XC4000), and the progression to the "finished" state F (see Figure 2) should all occur as a result of one common byte input. Under normal circumstances, the software achieves this by manipulating the length-count value appropriately, taking into account the additional bits between devices, and adjusting for the fact that byte-wide interfaces always leave the last bit sitting in the P-S converter, shifting it out at the beginning of the next byte. These complexities, combined with the many possible daisy-chain arrangements have occasionally led to problems, where the device outputs go active before the last required byte had been received. This can lead to contention on the address outputs or data inputs and might prevent the device from going DONE, or reaching the real end of its configuration sequence. Not reaching this "finished" state limits the use of readback and boundary scan. A new Makebits option solves this problem:

Since XACT 5.0, the default option is "Length-Count aligned" which adjusts the length-count value such that length-count match occurs during the first bit in the last configuration byte. This assures sufficient CCLK pulses to complete any selected type of start-up sequence. The other option is "DONE-aligned", which adjusts length count value to make DONE go active at the end of a configuration data byte, which can cause problems in Peripheral mode.

Only Peripheral modes seem to be sensitive to the difference between these two options.

Miscellaneous Notes

CCLK is the most important configuration signal. Once the $\overline{\text{INIT}}$ output is High, each device counts every Low-to-High transition of this configuration clock. In all modes except Slave Serial and XC4000 Synchronous Peripheral, CCLK is a very fast output that cannot be made slew-rate limited. When distributing this clock, the user should pay special attention to glitches, overshoots, and undershoots. In severe cases, a 33 Ω resistor in series with the CCLK output might improve the signal integrity. In other cases, it might be better to provide a pull-up resistor at the far end of the CCLK net. Since the clock net has a transmission-line characteristic impedance of always less than 100 Ω, the limited output drive capability of the CCLK output precludes proper parallel termination.

DOUT is an excellent observation point, since every device must output the preamble on this pin, irrespective of the selected configuration mode, and irrespective of the position in, or the existence of, a daisy chain.

$\overline{\text{INIT}}$ of all XC4000 and XC3000 devices in a daisy chain should be interconnected to prevent the configuration from starting before all devices are ready. A 10 kΩ pull-up resistor is recommended. The parallel $\overline{\text{INIT}}$ of the daisy-chained devices must be connected to the $\overline{\text{INIT}}$ of the lead XC4000 device, or to the $\overline{\text{RESET}}$ input of the lead XC3000 device. This is especially important for re-configuration, where the master does not have a four-times longer wait period.

The **DONE** output indicates the end of the configuration process. In XC2000 and XC3000 systems, it makes sense to ground DONE permanently. The $\overline{\text{RESET}}$ input then becomes the reconfiguration input, and cannot be used as the dedicated asynchronous user $\overline{\text{RESET}}$ input. $\overline{\text{LDC}}$ can be used to indicate end of configuration.

$\overline{\text{PWRDWN}}$ (on XC2000 and XC3000 devices) must be High before and during the configuration process.

Don't let $\overline{\text{PWRDWN}}$ float!

Configuring Mixed FPGA Daisy Chains

June 1, 1996 (Version 1.0)

Application Note by PETER ALFKE

Xilinx FPGAs can be configured in a common daisy-chain structure, where the lead device generates CCLK pulses and feeds serial configuration information into the next downstream device, which in turn feeds data into the next downstream device, etc. There is no limit to the number of devices in a daisy chain, and XC2000, XC3000, XC4000, and XC5200 series devices can be mixed freely with only one constraint: the lead device must be a member of the highest-order family used in the chain. (For the purposes of this discussion, there is no difference between the XC4000 series and the XC5200 family, when XC5200 is used in any configuration mode except Express Mode). The lead device must generate a sufficient number of CCLK pulses after length-count-match was achieved, but XC3000-series devices generate fewer CCLK pulses than XC4000-series or XC5200-family devices require, and XC2000 devices generate even fewer CCLK pulses after length-count match. See Figure 1.

In a daisy-chain, all CCLK pins are interconnected, and DOUT of any upstream device feeds the DIN input of its downstream neighbor. Those are the basic connections. For control purposes, it is advisable to interconnect all the slave $\overline{\text{INIT}}$ pins (the XC2000 does not have this pin) and connect them to the $\overline{\text{INIT}}$ pin of the lead XC4000/XC5200 device or the $\overline{\text{RESET}}$ input of the lead XC3000 device.

Interconnected $\overline{\text{INIT}}$ pins prevent the master from starting the configuration process until all slaves are ready. For power-up this is assured automatically, since the master uses four times as many internal clocks for the power-up as any slave does, but, when re-configuring, master and slave devices consume the same number of clocks to clear a frame, and a fast master might be ready before a slow slave is. Interconnecting $\overline{\text{INIT}}$s solves this problem.

The DONE/$\overline{\text{PROG}}$ (D/$\overline{\text{P}}$) and $\overline{\text{RESET}}$ pins (XC2000, XC3000) and the XC4000/XC5200 $\overline{\text{PROGRAM}}$ pins can be used in different ways, depending on the designer's preferences regarding reconfiguration, pin utilization, and need for a global RESET input.

If there is no need for a global logic RESET input, then it is best to permanently ground the XC2000/3000 D/$\overline{\text{P}}$ pin, which means that the $\overline{\text{RESET}}$ input functions as the Reconfigure input, and should be connected to all XC4000/XC5200 *PROGRAM* inputs.

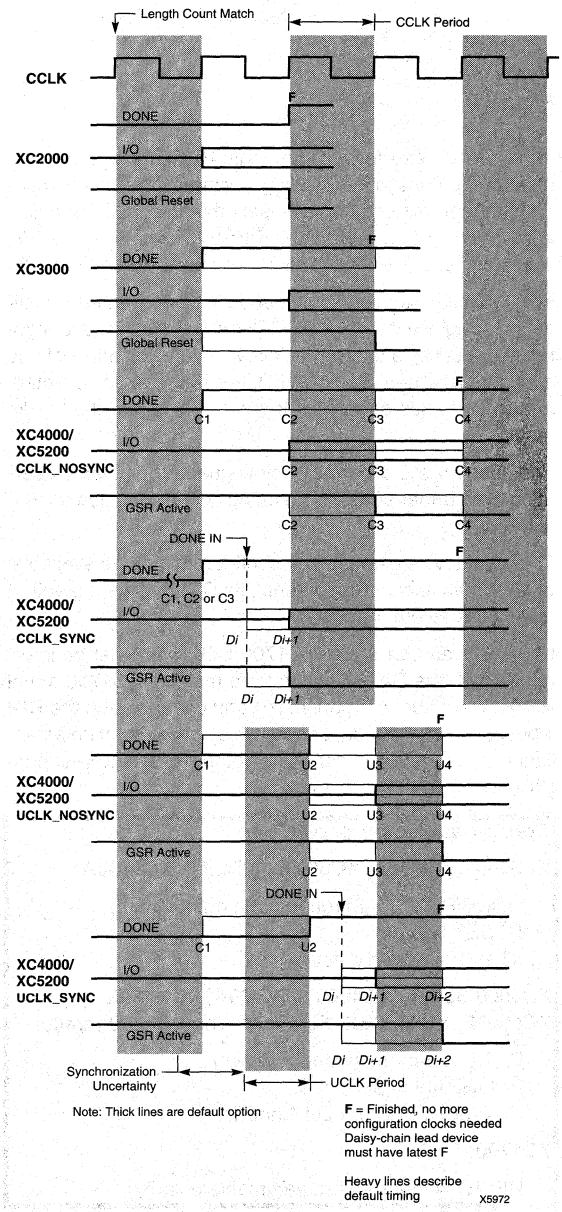


Figure 1: Start-up Timing

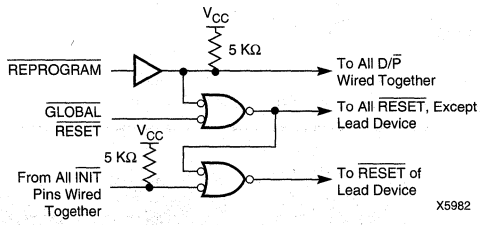


Figure 2:

If there is a need for a global logic RESET input that can reset all flip-flops in the user logic without causing reconfiguration, then external logic must combine $\overline{\text{RESET}}$ and D/$\overline{\text{P}}$ in such a way, that pulling Low $\overline{\text{RESET}}$ does not affect D/$\overline{\text{P}}$, but pulling Low D/$\overline{\text{P}}$ also pulls down $\overline{\text{RESET}}$. See Figure 2.

The following simple recommendations guarantee a well-defined beginning for any FPGA configuration or reconfiguration process, after the initialization and clearing of the configuration memory in all FPGAs has been completed, and the address counter in the serial PROM(s) has been reset.

The connections described below guarantee reliable operation even under adverse operating conditions such as V_{CC} glitches.

The lead device can use any configuration mode available. In all modes except Slave Serial, its CCLK pin is the output that clocks all other devices.

Obviously, all CCLK and XC1700 CLK pins must be interconnected, the DATA outputs from multiple XC1700 serial PROMs must be interconnected and connected to the DIN input of the lead device, and the daisy-chain must be established by connecting each DOUT output to the downstream DIN input.

Configuration control pins are:

XC3000, XC3000A, XC3000L, XC3100, XC3100A:

DONE/$\overline{\text{PROGRAM}}$ (open-drain output/input)
$\overline{\text{RESET}}$ (input)
$\overline{\text{INIT}}$ (open-drain output)

XC4000 Series (XC4000, XC4000A, XC4000D, XC4000E, XC4000EX, XC4000H) and XC5200-family:

DONE (open-drain output / input)
$\overline{\text{PROGRAM}}$ (input)
INIT (open-drain output / input)

XC1700:

RESET (input with programmable polarity)

The following recommendations assume that there are no XC2000 devices in the daisy chain (they lack the INIT output) and that, if Serial mode is chosen for the lead device, the XC1700 device(s) store only one configuration for the whole daisy chain. The serial PROM(s) must, therefore, be reset before the daisy chain is to be (re)programmed.

There are three possible types of daisy chains using XC3000 and XC4000/XC5200 devices. Here are the recommended connections for the configuration control pins.

Case 1:
Daisy chain consists of nothing but XC3000-series devices:

Use lead device's $\overline{\text{LDC}}$ to drive XC1700 CE.

Use lead device's $\overline{\text{INIT}}$ to drive XC1700 RESET.

Interconnect all slave $\overline{\text{INIT}}$s and connect them to the lead *RESET* input.

Interconnect all DONE pins.

Interconnect all slave $\overline{\text{RESET}}$ inputs

Instigate Reprogram by pulling the slave RESET net Low for at least 6 µs while all DONE pins are Low.

(DONE can be permanently wired Low, but that sacrifices the use of $\overline{\text{RESET}}$ as a global reset of the user logic. If DONE is not wired Low, reprogram must pull DONE Low with an open-collector or open-drain driver).

Case 2:
Lead device is XC4000-series or XC5200 family, driving any mixture of XC3000, XC4000 and XC5200 devices:

Use lead device's $\overline{\text{LDC}}$ to drive XC1700 $\overline{\text{CE}}$.

Use lead device's $\overline{\text{INIT}}$ to drive XC1700 RESET.

Interconnect all $\overline{\text{INIT}}$ pins.

Interconnect all DONE pins.

Interconnect all XC4000/XC5200 $\overline{\text{PROGRAM}}$ inputs.

Interconnect all XC3000 $\overline{\text{RESET}}$ inputs.

Combine these two nets into one $\overline{\text{PROGRAM}}$/$\overline{\text{RESET}}$ net

Instigate Reprogram by pulling the combined $\overline{\text{PROGRAM}}$/$\overline{\text{RESET}}$ Low.

Case 3:
Daisy chain consists of nothing but XC4000/ and XC5200-type devices:

Use lead device's $\overline{\text{LDC}}$ to drive XC1700 CE.

Use lead device's $\overline{\text{INIT}}$ to drive XC1700 RESET.

Interconnect all INIT pins.

Interconnect all DONE pins (only required for UCLK-SYNC option).

Interconnect all XC4000/XC5200 $\overline{\text{PROGRAM}}$ inputs.

Instigate Reprogram by pulling $\overline{\text{PROGRAM}}$ Low.

Configuration Issues: Power-up, Volatility, Security, Battery Back-up

June 1, 1996 (Version 1.0)

Application Note by PETER ALFKE

Summary

This application note covers several related subjects: How does a Xilinx FPGA power up, and how does it react to power-supply glitches? Is there any danger of picking up erroneous data and configuration? What can be done to maintain configuration during loss of primary power? What can be done to secure a design against illegal reverse-engineering?

Xilinx Families

XC2000, XC3000, XC4000, XC5200

Power-Up

Here is a detailed description of XC3000 Series, XC4000 Series and XC5200 device behavior during supply ramp-up and ramp-down.

When V_{cc} is first applied and is still below about 3 V, the device wakes up in the pre-initialization mode. HDC is High; $\overline{INIT}$, $\overline{LDC}$ and DONE or DONE/$\overline{PROG}$ (D/$\overline{P}$) are Low, and all other outputs are 3-stated with a weak pull-up resistor.

When V_{CC} has risen to a value above ~3 V, and a 1 and a 0 have been successfully written into two special cells in the configuration memory, the initialization power-on time delay is started. This delay compensates for differences in V_{CC} detect threshold and internal CCLK oscillator frequency between different devices in a daisy chain. The initialization delay counts clock periods of an on-chip oscillator (CCLK) which has a 3:1 frequency uncertainty depending on processing, voltage and temperature. Time-out, therefore, takes between 11 and 33 ms for a slave device, four times longer for a master device.

This factor of four makes sure that even the fastest master will always take longer than any slave. We assume that the worst- case difference between 33 ms and 4 x 11 ms is enough to compensate for the V_{CC} rise time spent between threshold differences (max 2 V) of devices in a daisy chain. Only in cases of very slow V_{CC} rise time (>25 ms), must the user hold RESET Low until V_{CC} has reached a proper level. Interconnecting the $\overline{INIT}$ pins of all devices in a daisy-chain is a better method of synchronizing start-up, but cannot be used with XC2000 devices, since they lack an $\overline{INIT}$ pin.

After the end of the initialization time-out, each device clears its configuration memory in a fraction of a millisecond, then tests for inactive $\overline{RESET}$ or $\overline{PROGRAM}$, stores the MODE value and starts the configuration process, as described in the Data Sheet. After the device is configured, the 5-V V_{CC} may dip to about 3.5 V without any significant consequences beyond an increase in delays (circuit speed is proportional to V_{cc}), and a reduction in output drive. If V_{cc} drops into the 3-V range, it triggers a sensor that forces the device back to the pre-initialization mode described above. All flip-flops are reset, HDC goes High; $\overline{INIT}$, $\overline{LDC}$ and D/$\overline{P}$ or DONE go Low, and all other outputs are 3-stated with a weak resistive pull-up. If V_{CC} dips substantially lower, the active outputs become weaker, but the device stays in this preinitialization mode. When V_{CC} rises again, a normal configuration process is initiated, as described above.

Sensitivity to V_{CC} Glitches

The user need not be concerned about power supply dips: The XC3000/XC4000/XC5200 devices stay configured for small dips and they are "smart enough" to reconfigure themselves (if a master) or to ask for reconfiguration by pulling $\overline{INIT}$ and D/$\overline{P}$ or DONE Low (if a slave). The devices will not lock up; the user can initiate re-configuration at any time just by pulling D/$\overline{P}$ or $\overline{PROGRAM}$ Low or, if D/$\overline{P}$ is Low, by forcing a High-to-Low transition on RESET.

Any digital logic device with internal data storage in latches or flip-flops is sensitive to power glitches. This includes every RAM, microprocessor, microcontroller, and peripheral circuit. Only purely combinatorial circuits can be guaranteed to survive a severe power glitch without any problem.

Xilinx SRAM-based FPGAs store their configuration in latches that lose their data when the supply voltage drops below a critical value (which is substantially below 3 V for the 5-V devices), but configuration data is extremely robust and reliable while V_{CC} stays above 3 V. All Xilinx configuration latches are implemented as cross-coupled complementary inverters with active pull-down n-channel transistors and active pull-up p-channel transistors. Both High and Low logic levels have an impedance of less than 5kΩ with respect to their respective supply rail.

Typical SRAM memory devices use passive poly-silicon pull-up resistors with an impedance of about 5,000 MΩ. A current of one nanoamp (!) is sufficient to upset the typical SRAM cell, whereas it takes a million times more current to upset the Xilinx configuration latch.

This does not mean that SRAMs are unreliable, it just shows that the levels in Xilinx configuration latches are six orders of magnitude more resistant to upsets caused by external events, like cosmic rays or alpha particles. Xilinx has never heard about any occurrence of a spontaneous change in the configuration store in any of its ~50 million FPGA devices sold over the past twelve years.

Whereas most digital circuits rely on V_{cc} staying within specification, Xilinx FPGAs have an internal voltage monitoring circuit. For example, in the 5-Volt devices, whenever the supply voltage dips below 3 V, the internal monitoring circuit causes the Xilinx FPGA to stop normal operation. All outputs go 3-state, and the device waits for the supply voltage to rise closer to 4 V, when it either demands (slave or peripheral mode) or initiates (master mode) a reconfiguration. In the range between 5.5 and 3 V, all typical CMOS devices maintain their functionality and their data storage, they just get slower as the voltage goes down.

Xilinx has made sure that the FPGA cannot be corrupted by a power glitch. The most sensitive circuit is the low-voltage detector. It kicks in while all other configuration storage and user logic is still guaranteed to be functional. The voltage-monitoring feature in the Xilinx device can even be used to protect other circuitry, or it can be coordinated with external monitoring circuits.

There is no possibility of a V_{CC} dip causing the device to malfunction, i.e., to operate with erroneous configuration information.

- If V_{CC} stays above the trip point, the device functions normally, albeit at reduced speed, like any other CMOS device.
- If V_{CC} dips below the trip point, the device 3-states all outputs and waits for reconfiguration.

Xilinx production-tests the V_{CC}-dip tolerance of all XC3000 devices in the following way.

After the device is configured, V_{CC} is reduced to 3.5 V, and then raised back to 5.0 V. Configuration data is then read back and compared against the original configuration bit stream. Any discrepancy results in rejection of the device.

Subsequently, V_{CC} is reduced to 1.5 V and then raised to 5.0 V. The device must first go 3-state, then respond with a request for reconfiguration.

Both these tests are performed at high temperature (>85°C for commercial parts, >100°C for military). Any part failing any of these tests is rejected as a functional failure.

As a result of these careful precautions, we contend that Xilinx FPGAs are safer than all other types of circuitry (except purely combinatorial circuits). A microprocessor can loose the content of its address register, its accumulator or other control register due to an undetected power glitch, with disastrous consequences to the subsequent operation. A Xilinx FPGA detects the power glitch and always plays it safe by flagging the problem.

No complex system of any kind can function reliably when V_{cc} is unreliable. Xilinx FPGAs do the safest thing possible, whenever such problems occur.

Design Security

Some Xilinx customers are concerned about the security of their designs. How can they protect their designs against unauthorized copying or reverse-engineering?

We must distinguish between two very different situations:

- Configuration data in accessible from a serial or parallel EPROM or in a microprocessor's memory. This is the normal case.
- Configuration data is hidden from the user, since the design does not permanently store a source of configuration data. After the FPGA was configured, the EPROM or other source was removed from the system, and configuration is kept alive in the FPGA through battery-back-up.

Design Security when Configuration Data is Accessible

In the first case, it is obviously very easy to make an identical replica of the design by copying the configuration data and the pc-board interconnect pattern of the standard devices, but it is virtually impossible to interpret the bitstream in order to understand the design or make intelligent modifications to it. Xilinx keeps the interpretation of the bitstream a closely guarded secret. Reverse-engineering an FPGA would require an enormously tedious analysis of each individual configuration bit, which would still only generate an XACT view of the FPGA, not a usable schematic.

The best protection against a mindless copy is legal. The bitstream is easily protected by copyright laws that have proven to be more successfully enforced than the intellectual property rights of circuit designs.

The combination of copyright protection, and the almost insurmountable difficulty of creating any design variation for the intended function, provides good design security. The recent successes of small companies in reverse-engineering microprocessors and microprocessor support circuits show that a non-programmable device can actually be more vulnerable than an FPGA. For advice on legal protection of the configuration bitstream, see the following paragraphs.

Legal Protection of Configuration Bit-Stream Programs

The bit-stream program loaded into the FPGA may qualify as a "computer program" as defined in Section 101, Title 17 of the United States Code, and as such may be protectable under the copyright law. It may also be protectable as a trade secret if it is identified as such. We suggest that a user wishing to claim copyright and/or trade secret protection in the bit stream program consider taking the following steps.

Place an appropriate copyright notice on the FPGA device or adjacent to it on the PC board to give notice to third parties of the copyright. For example, because of space limitations, this notice on the FPGA device could read "©1996 XYZ Company" or, if on the PC board, could read "Bit Stream ©)1996 XYZ Company".

File an application to register the copyright claim for the bit-stream program with the U.S. Copyright Office.

If practicable, given the size of the PC board, notice should also be given that the user is claiming that the bit- stream program is the user's trade secret. A statement could be added to the PC board such as: "Bit-stream proprietary to XYZ Company. Copying or other use of the bitstream program except as expressly authorized by XYZ Company is prohibited."

To the extent that documentation, data books, or other literature accompanies the FPGA-based design, appropriate wording should be added to this literature providing third parties with notice of the user's claim of copyright and trade secret in the bit-stream program. For example, this notice could read: "Bit-Stream©)1996 XYZ Company. All rights reserved. The bit-stream program is proprietary to XYZ Company and copying or other use of the bit- stream program except as expressly authorized by XYZ Company is expressly prohibited."

To help prove unauthorized copying by a third party, additional nonfunctional code should be included at the end of the bit-stream program. Therefore, should a third party copy the bit-stream program without proper authorization, if the non-functional code is present in the copy, the copier cannot claim that the bit-stream program was independently developed.

These are only suggestions, and Xilinx makes no representations or warranties with respect to the legal effect or consequences of the above suggestions. Each user is advised to consult legal counsel with respect to seeking protection of a bit-stream program and to determine the applicability of these suggestions to the specific circumstances.

If the user has any questions, contact the Xilinx legal department at 408-879-4984.

Design Security by Hiding the Configuration Data

If the design does not contain the source of configuration data, but relies on battery-back-up of the FPGA configuration, then there is no conceivable way of copying this design. Opening up the package and probing thousands of latches in undocumented positions to read out their data without ever disturbing the configuration is impossible.

This mode of operation offers the ultimate design security. It is being used by several Xilinx customers who have reason to be concerned about illegal pirating of their designs.

Battery Back-up and Powerdown

Since SRAM-based FPGAs are manufactured using a high-performance low-power CMOS process, they can preserve the configuration data stored in the internal static memory cells even during a loss of primary power. This is accomplished by forcing the device into a low-power non-operational state, while supplying the minimal current requirement of V_{CC} from a battery.

Circuit techniques used in XC3100, XC4000 and XC5200 devices prevent I_{CC} from being reduced to the level needed for battery back-up. Consequently, battery back-up should only be used for XC2000, XC2000L, XC3000, XC3000A and XC3000L devices.

There are two primary considerations for battery backup which must be accomplished by external circuits.

- Control of the Power-Down ($\overline{PWRDWN}$) pin
- Switching between the primary V_{CC} supply and the battery.

Important considerations include the following.

- Insure that $\overline{PWRDWN}$ is asserted logic Low prior to V_{CC} falling, is held Low while the primary V_{CC} is absent, and returned High after V_{CC} has returned to a normal level. $\overline{PWRDWN}$ edges must not rise or fall slowly.
- Insure "glitch-free" switching of the power connections to the FPGA device from the primary V_{CC} to the battery and back.
- Insure that, during normal operation, the FPGA V_{CC} is maintained at an acceptable level, 5.0 V ± 5% (±10% for Industrial and Military).

Figure 1 shows a power-down circuit developed by Shel Epstein of Epstein Associates, Wilmette, IL. Two Schottky diodes power the FPGA from either the 5.2 V primary supply or a 3 V Lithium battery. A Seiko S8054 3-terminal power monitor circuit monitors V_{CC} and pulls $\overline{PWRDWN}$ Low whenever V_{CC} falls below 4 V.

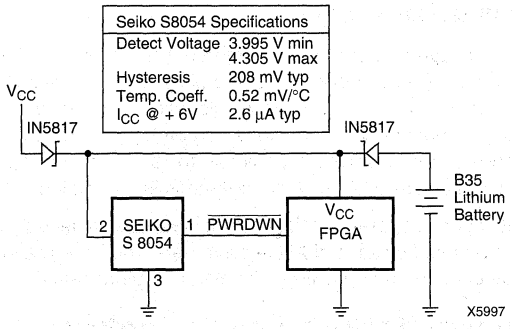


Figure 1: Battery Back-up Circuit

Powerdown Operation

A Low level on the $\overline{\text{PWRDWN}}$ input, while V_{CC} remains higher than 2.3 V, stops all internal activity, thus reducing I_{CC} to a very low level:

- All internal pull-ups (on Long lines as well as on the I/O pads) are turned off.
- The crystal oscillator is turned off
- All package outputs are three-stated.
- All package inputs ignore the actual input level, and present a High to the internal logic.
- All internal flip-flops or latches are permanently reset.
- The internal configuration is retained.
- When $\overline{\text{PWRDWN}}$ is returned High, after V_{CC} is at its nominal value, the device returns to operation with the same sequence of buffer enable and D/$\overline{\text{P}}$ as at the completion of configuration.

Things to Remember:

Powerdown retains the configuration, but loses all data stored in the device. Powerdown three-states all outputs and ignores all inputs. No clock signal will be recognized, and the crystal oscillator is stopped. All internal flip- flops and latches are permanently reset and all inputs are interpreted as High, but the internal combinatorial logic is fully functional.

Things to Watch Out for:

Make sure that the combination of all inputs High and all internal flip-flop outputs Low in your design will not generate internal oscillations or create permanent bus contention by activating internal bus drivers with conflicting data onto the same long line. These two situations are farfetched, but they are possible and will result in considerable power consumption. It is quite easy to simulate these conditions since all inputs are stable and the internal logic is entirely combinatorial, unless latches have been made out of function generators.

During powerdown, the V_{CC} monitoring circuit is disabled. It is then up to the user to prevent V_{CC} dips below 2.3 V, which would corrupt the stored configuration.

During configuration, the $\overline{\text{PWRDWN}}$ pin must be High, since configuration uses the internal oscillator. Whenever V_{CC} goes below 4 V, $\overline{\text{PWRDWN}}$ must already be Low in order to prevent automatic reconfiguration at low V_{CC}. For the same reason, V_{CC} must first be restored to 4 V or more, before $\overline{\text{PWRDWN}}$ can be made High.

$\overline{\text{PWRDWN}}$ has no pull-up resistor. A pull-up resistor would draw supply current when the pin is Low, which would defeat the idea of powerdown, where I_{CC} is only microamperes.

Dynamic Reconfiguration

June 1, 1996 (Version 1.0)

Application Note By PETER ALFKE

All Xilinx SRAM-based FPGAs can be in-system configured and re-configured an unlimited number of times. The XC6200 family has additional features that allow partial and very fast (re-)configuration from a microprocessor bus. See the XC62000 product documentation for details.

This application note describes the procedures for reconfiguring the more traditional Xilinx FPGAs of the XC2000, XC3000, XC3100, XC4000, and XC5200 families.

All configuration information is stored in latches that are loaded serially, conceptually like a shift register. There are several different bit-serial or byte-parallel configuration data interfaces, selected by logic levels on three mode inputs, but – with the exception of the XC5200 Express mode – they all result in the bit-serial loading of the configuration latches. The byte-parallel interfaces in Master Parallel and Peripheral modes act just as an 8-bit parallel-to-serial converter. Between devices in a daisy-chain, the configuration information is transmitted bit-serially with a common Configuration Clock (CCLK). In Master and Peripheral modes, CCLK is generated by the lead FPGA device, in Slave Serial mode, CCLK comes from an external source.

Reconfiguration of an operational device, or a daisy-chain of devices, goes through the following sequence of events:

- Reconfiguration is initiated by pulling a specific device pin Low.
- First, all outputs are 3-stated, except HDC = High, $\overline{\text{LDC}}$ and DONE = Low
- Then, all internal registers, flip-flops and latches, as well as the configuration storage latches are cleared. During this time, the $\overline{\text{INIT}}$ output is being pulled Low.
- Then, the Mode inputs and $\overline{\text{RESET}}$ or $\overline{\text{PROGRAM}}$ inputs are sampled to determine the selected configuration mode and whether to start the new configuration process, or to wait.
- Then configuration data is accepted and loaded into the internal latches and distributed through the daisy-chain.
- When all configuration information has been entered, the user outputs are activated, DONE goes High and the internal reset is released, all in the order specified in the configuration bitstream. All devices in a daisy-chain perform each of these operations in synchronism.

Important Considerations

- Reconfiguration is "all or nothing". There is no way to restrict reconfiguration to a part of the chip (Note that XC6200 devices do not have this limitation).
- Reconfiguration takes a specific time, determined only by device type, size and clock speed, independent of the particular configuration pattern. Configuration takes from tens to hundreds of milliseconds. During that time, all user-outputs of the device, or the whole daisy-chain of devices, are 3-stated with weak internal pull-ups, except for HDC and $\overline{\text{LDC}}$, which are active High or Low respectively.
- All user-data stored in registers, flip-flops or latches is erased. There is no way to retain data inside the device from one configuration to the next.

These limitations are absolute. If they are not acceptable, the user must resort to creative solutions, like piggy-backing multiple devices.

The designer of reconfigurable applications should be familiar with the normal configuration process of each device, as described in the individual product descriptions. There is also pertinent information about daisy-chain operation, especially about mixed daisy chains, on previous pages.

Interconnecting the $\overline{\text{INIT}}$ pins of all devices in a daisy-chain is mandatory for reconfiguration, since this is the only way to guarantee that the master device does wait for the rest of the daisy-chain to be cleared, before starting the reconfiguration. Only the first configuration after power-up makes the master device spend four times as many clock periods as any slave during the initial clear operation, so that the master cannot possibly get ahead of the slaves. Reconfiguration, however, does not slow down the master this way, so the interconnection of all $\overline{\text{INIT}}$ pins must serve that same purpose.

Note that the XC2000-family devices do not have an $\overline{\text{INIT}}$ pin.

In Master Serial mode, it is highly recommended that the active Low level of $\overline{\text{INIT}}$ be used to reset the XC1700-family Serial PROM.

Reconfiguration Time

Reconfiguration time is usually more critical than the original power-on configuration time, which is often masked by the general power-on delays.

Here are some suggestions to reduce reconfiguration time.

- A daisy-chain is obviously not conducive to fast configuration, it should be broken up into shorter blocks, perhaps single devices. Multiple devices can be configured in parallel, but can still use a common CCLK, and can also be made to start up together. If the devices differ in size or family, they should all be given the same length count as the largest device in the group.
- Configuration Mode
  Parallel and Peripheral modes are not any faster than Master Serial mode, since all modes (with the exception of XC4000EX and XC5200 Express mode) internally operate on serial data. The internally generated CCLK frequency is guard-banded to never approach the upper limit of what the device can tolerate. Therefore, the fastest possible configuration mode for XC3000 and XC4000-series devices is Slave Serial, with an external well-controlled source for CCLK. Its frequency can be up to 10 MHz for all 5-V devices, and there are ways to increase the average clock rate well beyond that, but they require dynamic clock frequency changes and an intimate understanding of the configuration frame structure.
  At 10 MHz, configuration time per device ranges from 1.5 ms for the XC3020A to 42 ms for the XC4025E and 143 ms for the XC4062EX.
- Possible Contention Problems:
  Certain user outputs become active during the configuration process:
  Address outputs during Master Parallel mode, Chip Select and Ready/Busy during Peripheral modes.
  The designer must make sure that these active outputs do not cause contention with other logic that might use the same pins as device inputs.

Initiating Reconfiguration in Different Xilinx Device Families

XC2000 and XC3000 Series

There are three alternatives:

1. Pull $\overline{\text{RESET}}$ Low while DONE is permanently grounded externally.

This is the simplest scheme, but it precludes the use of $\overline{\text{RESET}}$ to clear the flip-flops and latches in the operating user-design. $\overline{\text{RESET}}$ must be pulled Low for more than six microseconds to overcome its internal low-pass filtering. Configuration starts when $\overline{\text{RESET}}$ has gone High again.

2. Pull DONE Low with an open-drain ("open-collector") output. This assumes that DONE was High, i.e. that the previous configuration was successful. Reconfiguration starts as soon as the internal memory has been cleared. DONE can be released anytime.

3. Pull DONE Low with an open-drain ("open-collector") output and pull $\overline{\text{RESET}}$ Low. Keep $\overline{\text{RESET}}$ Low for at least six microseconds while DONE is Low. DONE can be released anytime after that, or not released at all. See alternative 1.

XC4000 Series and XC5200 Family

Pull the $\overline{\text{PROGRAM}}$ input Low for at least 0.3 microseconds to initiate clearing the configuration memory, then pull $\overline{\text{PROGRAM}}$ up to start the new configuration process.

While PROGRAM is held Low, a Low level on $\overline{\text{INIT}}$ indicates that the device is continuously clearing the configuration memory. When $\overline{\text{PROGRAM}}$ has been pulled up, $\overline{\text{INIT}}$ stays Low during one more clear operation, then goes High.

All device families, except the original XC4000, have a continuously active pull-up resistor on the $\overline{\text{PROGRAM}}$ pin.

Metastable Recovery

August 10, 1996 (Version 2.1)

Application Note By PETER ALFKE and BRIAN PHILOFSKY

Whenever a clocked flip-flop synchronizes an asynchronous input, there is a small probability that the flip-flop output will exhibit an unpredictable delay. This happens when the input transition not only violates the setup and hold-time specifications, but actually occurs within the tiny timing window where the flip-flop accepts the new input. Under these circumstances, the flip-flop can enter a symmetrically balanced transitory state, called metastable (meta = between).

While the slightest deviation from perfect balance will cause the output to revert to one of its two stable states, the delay in doing so depends not only on the gain-bandwidth product of the circuit, but also on how perfect the balance is, and on the noise level within the circuit; the delay can, therefore, only be described in statistical terms.

The problem for the system designer is not the illegal logic level in the balanced state (it's easy enough to translate that to either a 0 or a 1), but the unpredictable timing of the final change to a valid logic state. If the metastable flip-flop drives two destinations with differing path delays, one destination might clock in the final data state while the other does not.

With the help of a self-contained circuit, Xilinx evaluated the XC4000 and XC3000-series flip-flops. The result of this evaluation shows the Xilinx flip-flop to be superior in metastable performance to many popular MSI and PLD devices.

Since metastability can only be measured statistically, this data was obtained by configuring several different Xilinx FPGAs with a detector circuit shown in Figure 1. The flip-flop under test receives the asynchronous ~1-MHz signal on its D input, and is clocked by a much higher manually adjustable frequency. The output QA feeds two flip-flops in parallel, one (QB) being clocked by the same clock edge, the other (QC) being clocked by the opposite clock edge. When clocked at a low frequency, each input change gets captured by the rising clock edge and appears first on QA, then, after the falling clock edge, on QC, and finally, after the subsequent rising clock edge, on QB.

If a metastable event in the first flip-flop increases the settling time on QA so much that QC misses the change, but QB still captures it on the next rising clock edge, this error can be detected by feeding the XOR of QB and QC into a falling-edge triggered flip-flop. Its output (QD) is normally

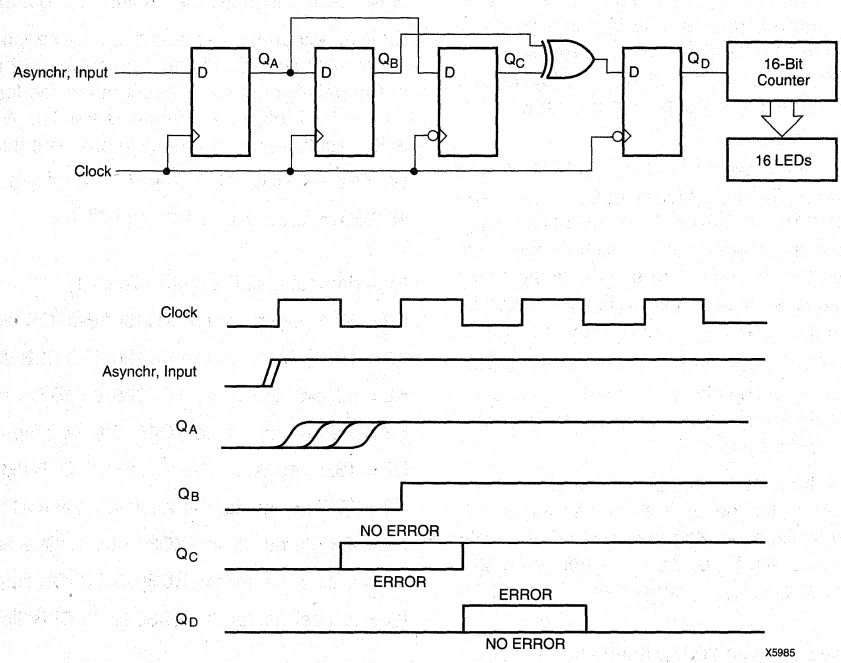


Figure 1: Test Circuit and Timing Diagram

Low, but goes High for one clock period each time the asynchronous input transition caused such a metastable delay in QA. The frequency of metastable events can be observed with a 16-bit counter driven by QD.

By changing the clock frequency, and thus the clock half-period, the amount of acceptable metastable delay on the QA output can be varied, and the resulting frequency of metastable events can be observed on the counter outputs.

As expected, no metastable events were observed at clock rates below 70 MHz for the XC4005-6, or below 100 MHz for the XC4005E-3, since a half clock period at those frequencies is adequate for almost any metastability-resolution delay. Increasing the clock rate slightly brought a sudden burst of metastable events. Careful adjustment of the clock frequency gave repeatable, reliable measurements.

Metastability Measurements

The circuit of Figure 1 was implemented in five different Xilinx devices: two cutting-edge devices using 0.5 micron, 3-layer-metal technology, the XC4005E-3 and the XC3142A-09, one device, the XC5206 using 0.6 micron, 3-layer-metal, and, for comparison purposes, also in two older-technology devices, the XC4005-6 and the XC3042-70.

In each device two different implementations put QA, the flip-flop under test, into an IOB and a CLB (Except for the XC5200 family which has no flip-flops in the IOB). The XC4000-series devices showed little difference between IOB and CLB behavior, but in the XC3000-series devices, the IOB flip-flops showed dramatically better metastable performance than the CLB flip-flops. This difference can be traced to subtle differences in circuit design and layout, and will guide us to further improvements in metastable performance in future designs.

Metastable measurement results are listed in Table 1, and are plotted in Figure 2. The results for XC4000E-3 (IOB and CLB) and for XC3100A-09 IOB flip-flops are outstanding, far superior to most metastable data published anywhere else. When granted 2 or 3 ns of extra settling delay, these devices come close to eliminating the problems caused by metastability, since their MTBF exceeds millions of years.

The older-technology devices are obviously less impressive, but they still show acceptable performance, especially in the IOB input flip-flops that are normally used to synchronize asynchronous input signals.

Table 1 lists the experimental results from which the exponential factor K2 was derived. The clock frequency was adjusted manually, while observing the LSB and the MSB of the 16-bit error counter. F_L is the clock frequency that generated a ~1 Hz error rate, F_H generated a ~64,000 Hz error rate.

K2 is derived by dividing ln 64,000 by the half-period difference.

Table 1: Metastable Measurement Results

Device	F_L (MHz)	F_H (MHz)	Half-period Difference (ns)	K2 (1/ ns)
XC4005E-3 IOB	111.5	131.6	0.685	16.1
XC4005E-3 CLB	109.0	124.4	0.568	19.4
XC4005-6 IOB	73.0	90.0	1.294	8.5
XC4005-6 CLB	71.2	88.8	1.392	7.9
XC5206-5 CLB	70.8	79.8	0.80	13.7
XC3142A-09 IOB	152.2	206.6	0.87	12.7
XC3142A-09 CLB	107.4	211.3	2.29	4.8
XC3042-70 IOB	46.6	61.5	2.60	4.2
XC3042-70 CLB	41.9	64.8	4.22	2.6

Metastability Calculations

The Mean Time Between Failures (MTBF) can only be defined statistically. It is inversely proportional to the product of the two frequencies involves, the clock frequency and the average frequency of the asynchronous data changes, provided that these two frequencies are independent and have no correlation.

The generally accepted equation for MTBF is

$$MTBF = \frac{e^{K2 * t}}{F1 * F2 * K1}$$

K1 represents the metastability-catching set-up time window, which describes the likelihood of going metastable.

K2 is an exponent that describes the speed with which the metastable condition is being resolved. K2 is an indication of the gain-bandwidth product in the feedback path of the master latch of the master-slave flip-flop. A small increase in K2 results in an enormous improvement in MTBF.

With F1 = 1 MHz, F2 = 10 MHz and K1 = 0.1 ns = 10^{-10} s:

MTBF (in seconds) = $10^{-3} * e^{K2*t}$

Experimentally derived (see Table 1):

K2 = 16.1 per ns, for the XC4005E-3 IOB flip-flops

K2 = 19.4 per ns, for the XC4005E-3 CLB flip-flops

K2 = 8.5 per ns, for the XC4005-6 IOB flip-flops

K2 = 7.9 per ns, for the XC4005-6 CLB flip-flops

K2 = 13.7 per ns, for the XC5206-5 CLB flip-flops

K2 = 12.7 per ns, for the XC3142A-09 IOB flip-flops

K2 = 4.8 per ns, for the XC3142A-09 CLB flip-flops

K2 = 4.2 per ns, for the XC3042-70 IOB flip-flops

K2 = 2.6 per ns, for the XC3042-70 CLB flip-flops

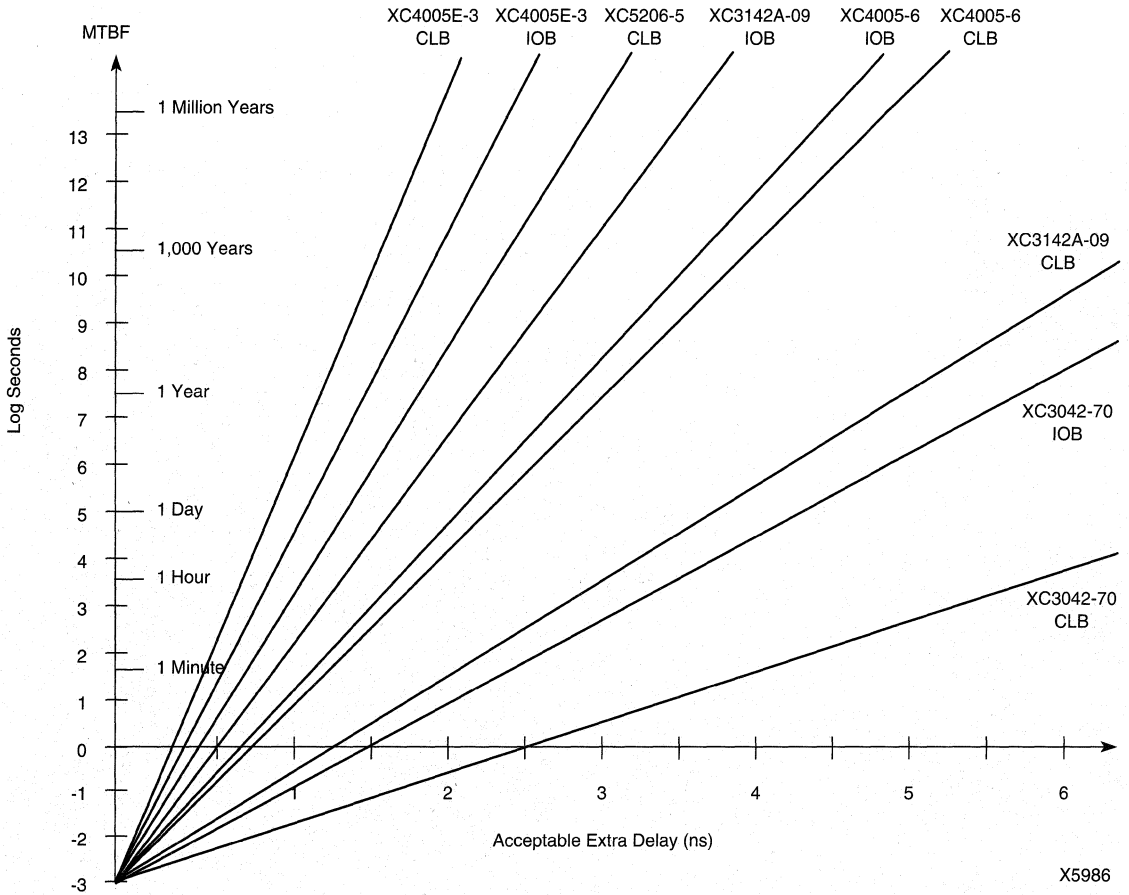


Figure 2: Mean Time Between Failure for various IOB and CLB flip-flop outputs when synchronizing a ~1 MHz asynchronous input with a 10 MHz clock.

For other operating conditions, divide MTBF by the product of the two frequencies. For a ~10 MHz asynchronous input synchronized by a 40 MHz clock, the MTBF is 40 times shorter than plotted; for a ~50 kHz signal synchronized by a 1 MHz clock, the MTBF is 200 times longer than plotted here.

Set-up and Hold Times

June 1, 1996 (Version 1.0)

Application Brief By PETER ALFKE

Beware of hold-time problems, because they can lead to unreliable, temperature-sensitive designs that can fail even at low clock rates.

"Set-up time" and "hold time" describe the timing requirements on the data input of a flip-flop or register with respect to the clock input. The set-up and hold times describe a window of time during which data must be stable in order to guarantee predictable performance over the full range of operating conditions and manufacturing tolerances.

A positive set-up time describes the length of time that the data must be available and stable before the active clock edge. A positive hold time, on the other hand, describes the length of time that the data to be clocked into the flip-flop must remain available and stable after the active clock edge. A positive set-up time limits the maximum clock rate of a system, but a positive hold time can cause malfunction at any clock rate. Thus, chip designers and system designers strive to eliminate hold-time requirements.

The IC design usually guarantees that any individual flip-flop does not require a positive hold time with respect to the clock signal at this flip-flop.

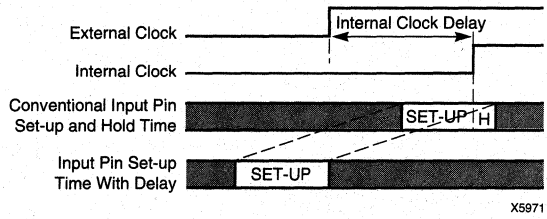
Hold-time requirements between flip-flops or registers on the same chip can be avoided by careful design of the on-chip clock distribution network. If the worst-case clock-skew value is shorter than the sum of minimum clock-to-Q plus minimum interconnect delays, there is never any on-chip hold-time problem.

It is, however, far more difficult to avoid a hold time problem in the device input flip-flops, with respect to the device clock input pin. When specifying the data pin-to-clock pin set-up and hold times, the chip-internal clock distribution delay must be taken into consideration. It effectively moves the timing window to the right (see figure), thus subtracting from the specified internal set-up time (which is good), but adding to the hold time (which is very bad). If the clock distribution delay is any longer than the data input delay – and it easily might be – the device data input has a hold-time requirement with respect to the clock input.

This means that the data source, usually another IC driven by the same clock, must guarantee to maintain data beyond the clock edge. In other words, the data source is not allowed to be very fast. If it is, the receiver might erroneously input the new data instead of the data created by the previous clock, as it should. This is called a race condition, and can be a fatal system failure.

If the receiving device has a hold time requirement, the source of data must guarantee an equivalent minimum value for its clock-to-output delay. Almost no IC manufacturer is willing to do this, and in the few cases where it is done, the minimum value is usually a token 1 ns. Any input hold time requirement is, therefore, an invitation to system failure. Any clock distribution skew on the PC-board can compound this issue and wipe out even the specified short minimum delay.

Xilinx has addressed this problem by adding a deliberate delay to every FPGA data input. In XC3000, and XC3100 FPGAs, this delay is fixed and always present; in XC4000 and XC5200 FPGAs, this delay is optional, and its value is tailored to the clock distribution delay (i.e. it is larger for bigger devices). As a result we can claim that no Xilinx FPGA Data input has a hold-time problem (i.e., none has a positive hold time with respect to the externally applied clock), when the design uses the internal global clock distribution network (and, in XC4000 and XC5200, uses the delayed input option). Most competitive devices do not offer this feature.



Overshoot and Undershoot

June 1, 1996 (Version 1.0)

Application Brief By PETER ALFKE

The "Absolute Maximum Ratings" table in the Xilinx Data Book restricts the signal-pin voltage to a maximum 500 mV excursion above V_{CC} and below ground. The reason for this tight specification is to prevent uncontrolled current in the input-clamping ESD-protection diodes. Such tight specifications are common in the industry; some manufacturers limit the excursion to 300 mV.

This specification seems to be clean and simple, but it is violated in almost every practical design. When users put modern CMOS devices on PC boards, and interconnect them with unterminated traces, there are reflections, commonly called "ringing", that cause overshoots and undershoots of substantial amplitude (2 V and more). The recent migration to smaller device geometries has made the IC outputs even faster and increased the slew-rate, causing more reflections even on short PC-board traces.

Fortunately, this problem has an easy solution:

The concern is not the input voltage, but rather the current through the input protection diode and other input structures. Excessive current can cause latch-up if it exceeds hundreds of milliamps AND if it lasts for microseconds (shorter duration current spikes do not activate the SCR-like latch-up mechanism).

PC-board reflections, on the other hand, usually have a short duration of just a few nanoseconds, and have an impedance of 40 to 100 Ω, which makes them incapable of causing latch-up. They don't drive enough current and they don't last long enough to cause any harm.

Here is the new Xilinx specification:

"Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns".

Boundary Scan in XC4000 and XC5000 Series Devices

June 1, 1996 (Version 2.0)

Summary

XC4000 and XC5000 Series FPGA devices contain boundary-scan facilities that are compatible with IEEE Standard 1149.1. This Application Note describes those facilities in detail, and explains how boundary scan is incorporated into an FPGA design.

Xilinx Family

XC4000 Series, XC5200

Demonstrates

Boundary Scan

Introduction

In production, boards must be tested to assure the integrity of the components and the interconnections. However, as integrated circuits have become more complex and multi-layer PC-boards have become more dense, it has become increasingly difficult to test assembled boards.

Originally, manufacturers used functional tests, applying input stimuli to the input connectors of the board, and observing the results at the output. Later, "bed-of-nails" testing became popular, where a customized fixture presses sharp, nail-like stimulus- and test-probes into the exposed traces on the board. These probes were used to force signals onto the traces and observe the response.

However, increasingly dense multi-layer PC boards with ICs surface-mounted on both sides have stretched the capability of bed-of-nail testing to its limit, and the industry is forced to look for a better solution. Boundary-scan techniques provide that solution.

The inclusion of boundary-scan registers in ICs greatly improves the testability of boards. Boundary scan provides a mechanism for testing component I/Os and inter-connections, while requiring as few as four additional pins and a minimum of additional logic in each IC. Component testing may also be supported in ICs with self-test capability.

Devices containing boundary scan have the capability of driving or observing the logic levels on I/O pins. To test the external interconnect, devices drive values onto their outputs and observe input values received from other devices. A central test controller compares the received data with expected results. Data to be driven onto outputs is distributed through a chain of shift registers, and observed input data is returned through the same shift-register path.

Data is passed serially from one device to the next, thus forming a boundary-scan path or loop that originates at the test controller and returns there. Any device can be temporarily removed from the boundary-scan path by bypassing its internal shift registers, and passing the serial data directly to the next device.

XC4000/XC5000 FPGA devices contain boundary-scan registers that are compatible with the IEEE Standard 1149.1, that was derived from a proposal by the Joint Test Action Group (JTAG). External (I/O and interconnect) testing is supported; there is also limited support for internal self-test.

Overview of XC4000/XC5000 Boundary-Scan Features

XC4000/XC5000 devices support all the mandatory boundary-scan instructions specified in the IEEE Standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD and BYPASS instructions. The TAP can also support two USERCODE instructions.

Note: If boundary scan is not used after the device is configured, the user can use the special boundary scan pads as input or output pins. And like the regular IOBs, these input and output pins have pullups and pulldowns available. The TDI, TMS, and TCK pads can be used as input pads. The TDO pad can be used as an output pad.

Boundary-scan operation is independent of individual IOB configuration and package type. All IOBs are treated as independently controlled bidirectional pins, including any unbonded IOBs. Retaining the bidirectional test capability even after configuration affords tremendous flexibility for interconnect testing.

Additionally, internal signals can be captured during EXTEST by connecting them to unbonded IOBs, or to the unused outputs in IOBs used as unidirectional input pins. This partially compensates for the lack of INTEST support.

The public boundary-scan instructions are always available prior to configuration. After configuration, the public instructions and any USERCODE instructions are only available if specified in the design. While SAMPLE and BYPASS are available during configuration, it is recommended that boundary-scan operations not be performed during this transitory period.

In addition to the test instructions outlined above, the boundary-scan circuitry can also be used to configure the FPGA device, and readback the configuration data.

The following description assumes that the reader is familiar with boundary-scan testing and the IEEE Standard. Only issues specific to the XC4000/XC5000 implementation are discussed in detail. For general information on boundary scan, please refer to the bibliography.

Deviations from the IEEE Standard

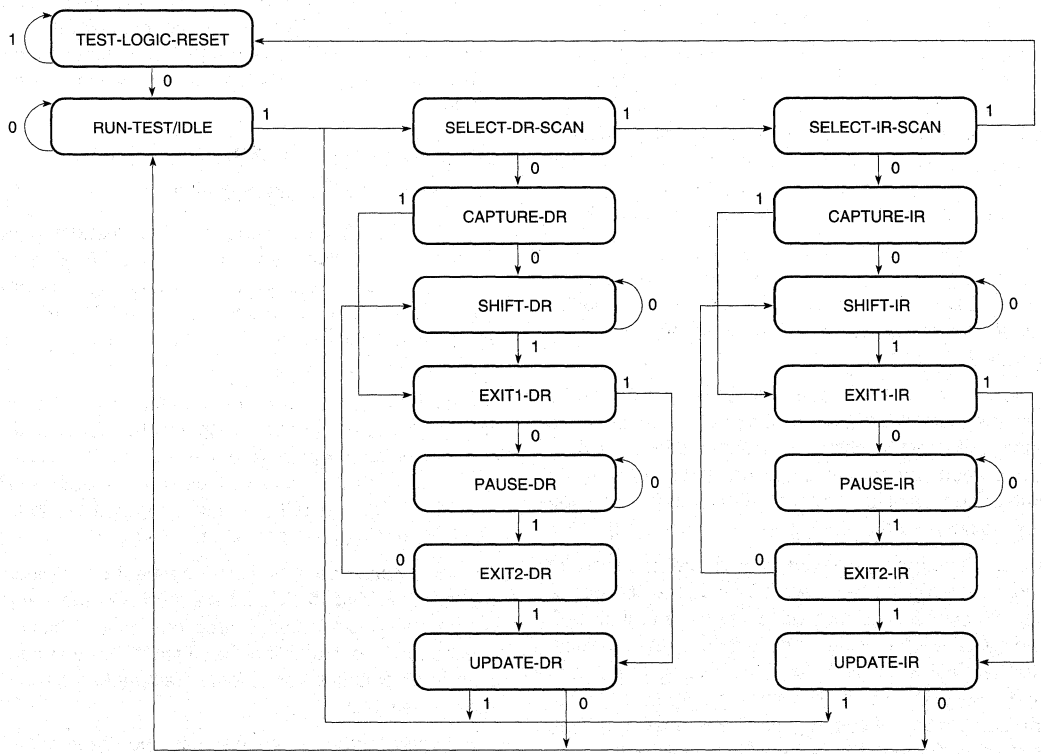
The XC4000/XC5000 boundary scan implementation deviates from the IEEE standard in that three dedicated pins (CCLK, $\overline{\text{PROGRAM}}$ and DONE) are not scanned.

It should also be noted that the Test Data Register contains three Xilinx test bits (BSCANT.UPD, TDO.O and TDO.T) and that bits of the register may correspond to unbonded or unused pins.

Additionally, the EXTEST instruction incorporates INTEST-like functionality that is not specified in the standard, and system clock inputs are not disabled during EXTEST, as recommended in the standard.

The TAP pins (TMS, TCK, TDI and TDO) are scanned, but connections to the TAP controller are made before the boundary-scan logic. Consequently, the operation of the TAP controller cannot be affected by boundary-scan test data.

When the TAP is in the shift-DR state the contents of all data registers are shifted; if you are in the middle of shifting out data from the data register in a XC4000, complete shifting out of all data first, before switching to the instruction or bypass register.



NOTE: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

X2680

Figure 1: State Diagram for the TAP Controller

Boundary-Scan Hardware Description

Test Access Port

The boundary-scan logic is accessed through the Test Access Port (TAP), which comprises four semi-dedicated pins: Test Mode Select (TMS), Test Clock (TCK), Test Data Input (TDI) and Test Data Output (TDO), as defined in the IEEE specification.

The TAP pins are permanently connected to the boundary-scan circuitry. However, once the device is configured, the connections may be ignored unless the use of boundary scan is specified in the design (See "Using Boundary Scan").

If the use of boundary scan is specified, the TAP input pins (TMS, TCK and TDI) may still be shared with other logic, subject to limitations imposed by external connections and the operation of the TAP Controller. In designs that do not use boundary scan after configuration, the TAP pins can be used as inputs or outputs from the user logic in the FPGA device. TMS, TCK and TDI are available as unrestricted I/Os, while TDO only provides a 3-state output.

TAP Controller

The TAP Controller is a 16-state state machine that controls the operation of the boundary-scan circuitry in response to TMS. This state machine implements the state diagram specified by the IEEE standard (Figure 1) and is clocked by TCK.

Upon power-on, or if the boundary scan logic is not used in the application, the TAP controller is forced into the Test-Logic-Reset state. After configuration, the controller remains disabled, unless its use is explicitly specified in the user design. $\overline{\text{PROGRAM}}$ resets the latched decodes for EXTEST, CONFIGURE, and READBACK instructions.

Loading a 3-bit instruction into the Instruction Register (IR) determines the subsequent operation of the boundary-scan logic, Table 1. The instruction selects the source of the TDO pin, and selects the source of device input and output data (boundary-scan register or input pin/user logic)

Note: In the XC4000, whenever the TAP Controller is in the Shift-DR state, all data registers are shifted, regardless of the instruction. DR data is modified even if a BYPASS instruction is executed.

The instruction register is not used only to hold the current instruction. If the TAP is in the capture-IR state and TCK goes high, the instruction register captures the current boundary-scan state of the device. I_0 is 1 by default. I_1 is 0 by default. I_2 is 0 if the devices is in configure by boundary scan mode. Before and after configure by boundary scan mode, I_2 will capture 1. Note that I_0 is shifted out of TDO first, then I_1, and then I_2.

Table 1: Boundary Scan Instructions.

Instruction I_2	I_1	I_0	Test Selected	TDO Source	I/O Data Source
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	TDO1	Pin/Logic
0	1	1	USER 2	TDO2	Pin/Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	RESERVED	—	—
1	1	1	BYPASS	Bypass Reg	Pin/Logic

I_0 is closest to DTO

The Boundary-Scan Data Register

The Data Register (DR) is a serial shift register implemented in the IOBs of the FPGA device, (Figure 2). Potentially, each IOB can be configured as an independently controlled bidirectional pin. Therefore, three data register bits are provided per IOB: for input data, output data and 3-state control. In practice, many of these bits are redundant, but they are not removed from the scan chain.

An update latch accompanies each bit of the DR, and is used to hold injected test data stable during shifting. The update latch is opened during the Update-DR state of the TAP Controller when TCK is Low.

In a typical DR instruction, the DR captures data during the Capture-DR state (on the rising edge of TCK). This data is then shifted out and replaced with new test data. Subsequently, the update latch opens, and the new test data becomes available for injection into the logic or the interconnect. The injection of data occurs only if an EXTEST instruction is in progress.

Note: The update latch is opened whenever the TAP Controller is in the Update-DR state, regardless of the instruction. Care must be exercised to ensure that appropriate data is contained in the update latch prior to initiating an EXTEST. Any DR instruction, including BYPASS, that is executed after the test data is loaded, but before the EXTEST commences, changes the test data.

The IEEE Standard does not require the ability to inject data into the on-chip system logic and observe the results during EXTEST. However, this capability helps compensate for the lack of INTEST. Logic inputs may be set to specific levels by a SAMPLE/PRELOAD or EXTEST instruction and the resulting logic outputs captured during a subsequent EXTEST. It must be recognized, however, that all DR bits are captured during an EXTEST and, therefore, may change.

Pull-up and pull-down resistors remain active during boundary scan. Before and during configuration, all pins

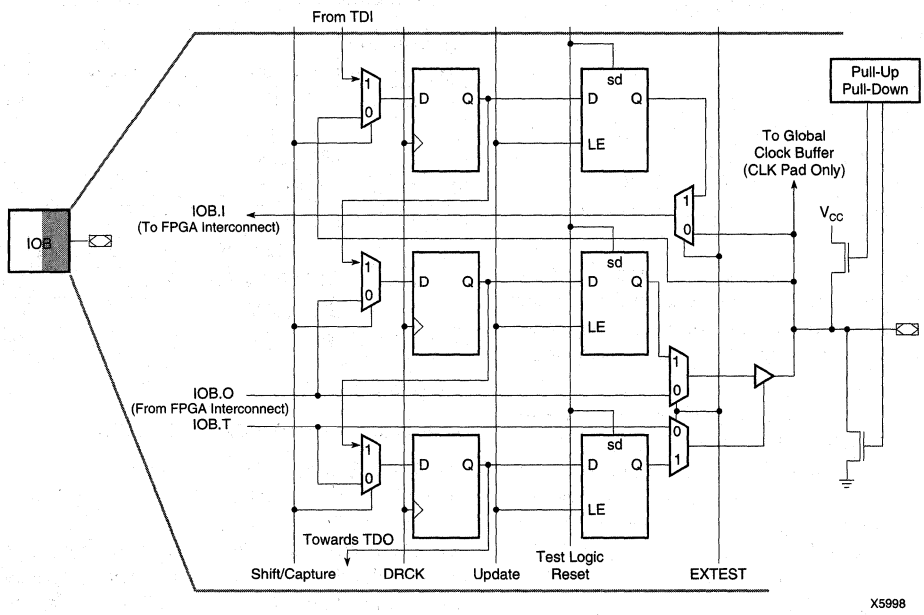


Figure 2: Boundary Scan Logic in a Typical IOB

are pulled up. After configuration, the IOB can be configured with a pull-up resistor, a pull-down resistor or neither.

Note: Internal pull-up/pull-down resistors must be taken into account when designing test vectors to detect open circuit PC traces.

The primary and secondary global clock inputs (PGCK1-4 and SGCK1-4) are taken directly from the pins, and cannot be overwritten with boundary-scan data. However, if necessary, it is possible to drive the clock input from boundary scan. The external clock source is 3-stated, and the clock net is driven with boundary scan data through the output driver in the clock-pad IOB. If the clock-pad IOBs are used for non-clock signals, the data may be overwritten normally.

Figure 3 shows the data-register cell for a TAP pin. An OR-gate permanently disables the output buffer if boundary-scan operation is selected. Consequently, it is impossible for the outputs in IOBs used by TAP inputs to conflict with TAP operation. TAP data is taken directly from the pin, and cannot be overwritten by injected boundary-scan data.

Table 2 lists, in data-stream order, the boundary-scan cells that make up the DR. The cell closest to TDO corresponds to the first bit of the data-stream, and is at the top of the table. This order is consistent with the BSDL description.

Each IOB corresponds to three bits in the DR. The 3-state control is first (closest to TDO), the output is next, and the input is last. Other signals correspond to individual register bits. IOB locations assume that the die is viewed from the top, as in XDE.

Note: All IOBs remain in the DR, independent of whether they are actually used, or even bonded. Three bits, BSCANT.UPD, TDO.O and TDO.T, are included for Xilinx test purposes, and may be ignored by other users. CCLK, $\overline{\text{PROGRAM}}$ and DONE are not included in the boundary scan.

Table 2: Boundary Scan Order

Bit 0 (TDO end)	TDO.T
Bit 1	TDO.O
Bit 2	Top-edge IOBs (Right to Left)
	Left-edge IOBs (Top to Bottom)
	MD1.T
	MD1.O
	MD1.I
	MD0.I
	MD2.I
	Bottom-edge IOBs (Left to Right)
	Right-edge IOBs (Bottom to Top)
(TDI end)	B SCANT.UPD

X2674

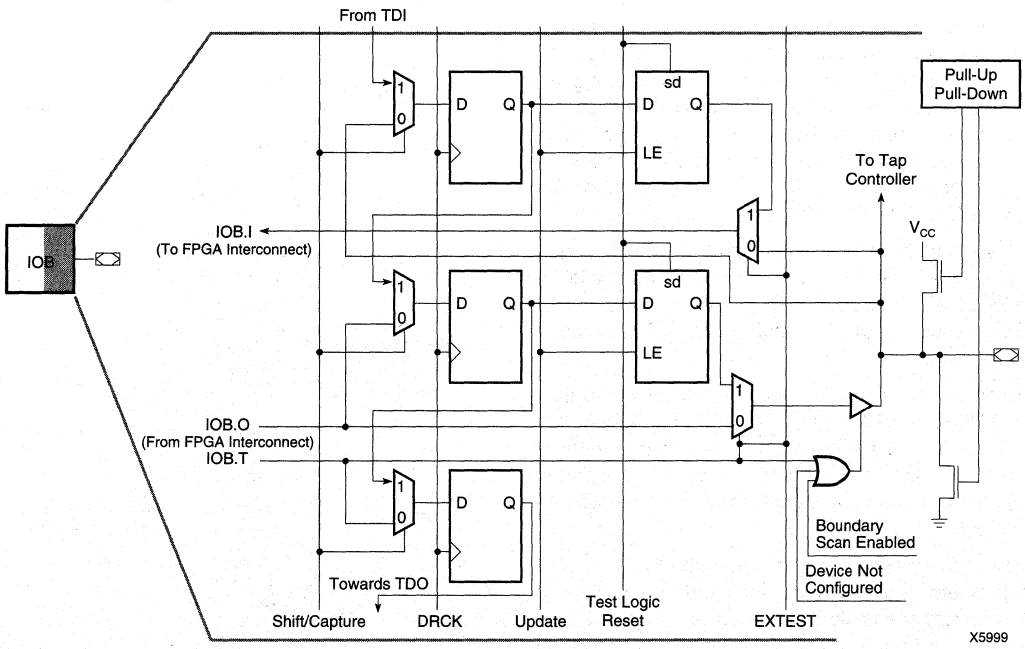


Figure 3: Boundary Scan Logic in a TAP Input (TMS, TCK, and TDI Only)

Tables in the data sheet show the DR order for all XC4000 family devices. The DR also includes the following non-pin bits: TDO.T and TDO.I, which are always bits 0 and 1 of the DR, respectively, and BSCANT.UPD which is always the last bit of the DR.

The Bypass Register

This is a 1-bit shift register that passes the serial data directly to TDO when a bypass instruction is executed.

User Registers

The XC4000 boundary-scan instruction set includes two USERCODE instructions, USER1 and USER2. Connections are provided to the TAP and TAP controller that, together with direct connections to the TAP pins, permit the user to include boundary-scan self-test features in the design.

The boundary scan block has six connections for user registers: SEL1, SEL2, TDO1, TDO2, DRCK and IDLE. TDI is available directly from the IOB that provides the TDI pin.

Note: The TDI signal supplied to user test logic is overwritten by boundary-scan test data during EXTEST. During user tests, it is not altered.

SEL1, SEL2 – SEL1 and SEL2 enable user logic. They are asserted (High) when the instruction register contains instructions USER1 and USER2, respectively.

TDO1, TDO2 – TDO1 and TDO2 are inputs to the TDO output multiplexer, permitting user access to the serial boundary-scan output. They are selected when executing the instructions USER1 and USER2, respectively. Input to user data registers can be derived directly from the TDI pin, thus completing the boundary-scan chain.

There is a one flip-flop delay between TDO1/TDO2 and the TDO output. This flip-flop is clocked on the falling edge of TCK.

DRCK – Data register clock (DRCK) is a gated and inverted version of TCK. It is provided to clock user test-data registers. TDI data should be sampled with the falling edge of DRCK (rising edge of TCK). The TDO output flip-flop accepts data on the rising edge of DRCK (falling edge of TCK). DRCK is active only during the Capture-DR and Shift-DR states of the TAP controller.

IDLE – IDLE is a second gated and inverted version of TCK. It is active during the Run-Test/Idle state of the TAP controller, and may be used to clock user test logic a set number of times, determined through TMS by the central test controller.

Using Boundary Scan

Full access to the built-in boundary-scan logic is always available between power-up and the start of configuration. Optionally, the built-in logic is fully available after configuration if boundary scan is specified in the design. At this time, user test logic is also available, and may be accessed through the boundary-scan port. During configuration, a reduced boundary-scan capability remains available: the SAMPLE/PRELOAD and BYPASS instructions only.

Figure 4 is a flow chart of the FPGA start-up sequence that shows when the boundary-scan instructions are available. Since $\overline{\text{PROGRAM}}$ resets the TAP controller, boundary-scan operations cannot commence until $\overline{\text{PROGRAM}}$ has been taken High.

Full boundary-scan capabilities are then available until $\overline{\text{INIT}}$ is High. Without external intervention, $\overline{\text{INIT}}$ automatically goes High after ~1 ms. If more time is required for boundary-scan testing, $\overline{\text{INIT}}$ may be held Low beyond this period by applying an external Low signal to the $\overline{\text{INIT}}$ pin until testing is complete.

Boundary scan can be accessed before the FPGA is configured and after the FPGA is configured. If you want to access boundary scan before the device is configured, then when you power-up the device, hold the $\overline{\text{INIT}}$ pin low until VCC has risen to Vcc(min). If you have already started configuring the device, data frames are already being sent to the FPGA, then you have two choices. You can either access full-boundary scan mode, or limited boundary scan mode. If you want to access full-boundary scan mode, then both $\overline{\text{INIT}}$ and $\overline{\text{PROGRAM}}$ must be brought low (Hold $\overline{\text{INIT}}$ and $\overline{\text{PROG}}$ low for over 300 ns and then release $\overline{\text{PROGRAM}}$. After releasing $\overline{\text{PROGRAM}}$, continue to hold $\overline{\text{INIT}}$ low while sending signals to the TAP. If you can use the limited boundary scan mode (which means you only can use the SAMPLE/PRELOAD and BYPASS instructions), then just bring $\overline{\text{INIT}}$ low.

Accessing boundary scan after the device is configured has one requirement. The BSCAN symbol must be instantiated/inserted into your design with the correct syntax (see Figure 5). In this case, activating boundary scan after configuration amounts to toggling the TAP pins.

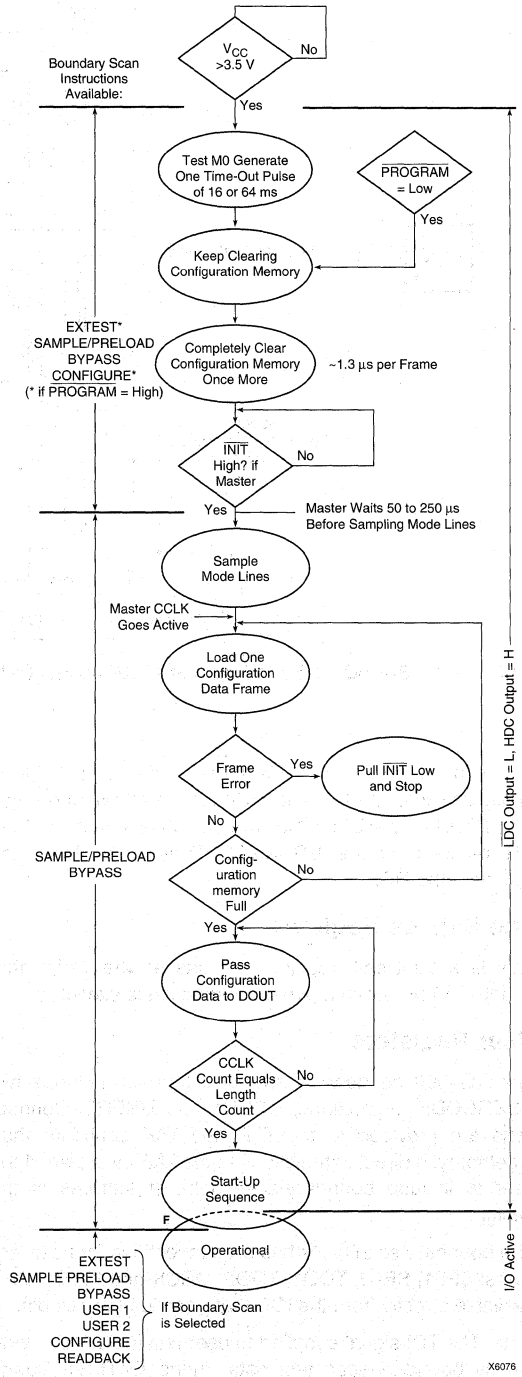
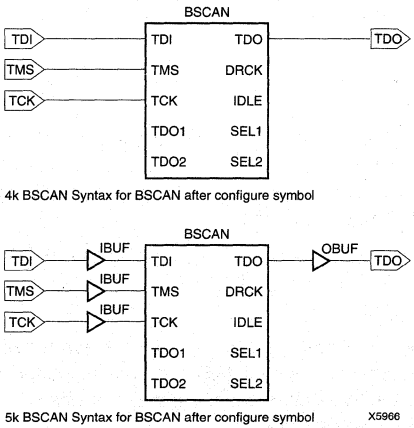


Figure 4: Start-up Sequence



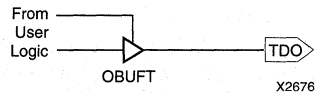


Figure 6: Typical Non-Boundary-Scan TDO Connection

Figure 5: Boundary-Scan Schematic

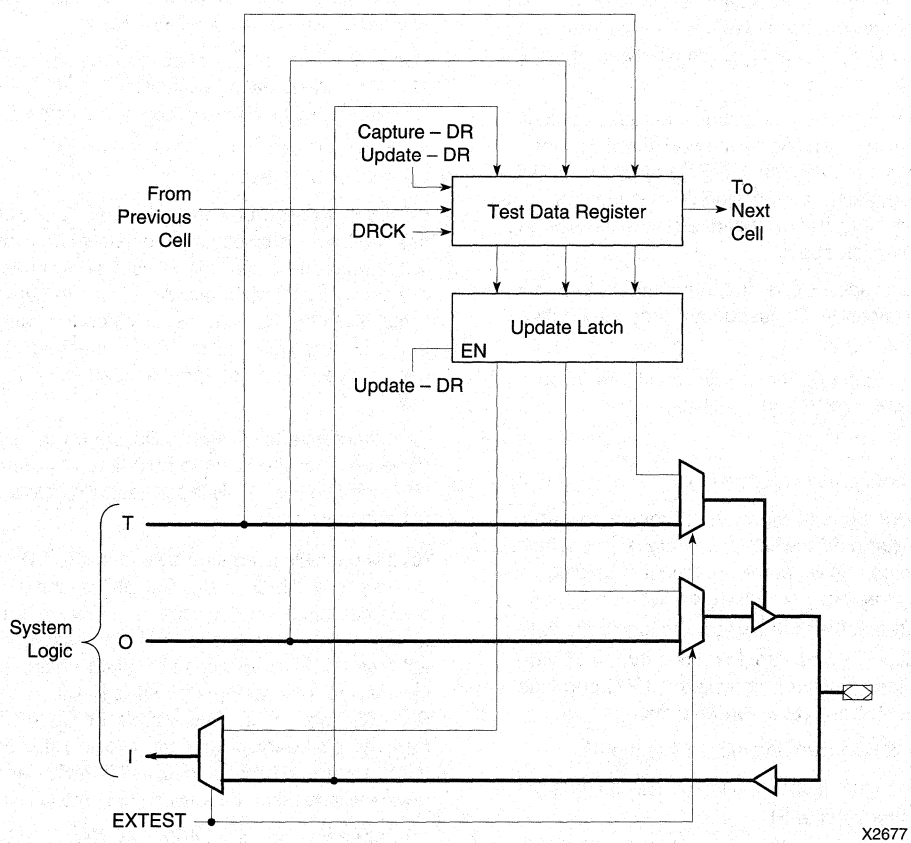


Figure 7: EXTEST Data Flow

The IEEE definition of EXTEST only requires that test data be driven onto outputs, that 3-state output controls be overridden, and that input data be captured. The capture of output data and 3-state controls and the forcing of test data into the system logic is normally performed during INTEST.

The XC4000 effectively performs EXTEST and INTEST simultaneously. This added functionality permits the testing of internal logic, and compensates for the absence of a separate INTEST instruction. However, when performing an EXTEST, care must be taken over what signals are driven into the system logic; data captured from internal system logic must be masked out of the test-data stream before performing check-sum analysis.

SAMPLE/PRELOAD – The SAMPLE/PRELOAD instruction permits visibility into system operation by capturing the state of the I/O. It also permits valid data to be loaded into the update register before commencing an EXTEST.

The DR and update latch operate exactly as in EXTEST (see above). However, data flows through the I/O unmodified.

BYPASS – The BYPASS instruction permits data to be passed synchronously to the next device in the boundary-scan path. There is a 1-bit shift register between the TDI and TDO flip-flop.

USER1, USER2 – These instructions permit test logic, designed by the user and implemented in CLBs, to be accessed through the TAP. Test clocks and paths to TDO are provided, together with two signals that indicate that user instructions have been loaded. For details, see the User Registers section above.

User tests depend upon CLBs and interconnect that must be configured to operate. Consequently, they may only be performed after configuration.

CONFIGURE – Steps to Follow to configure a Xilinx XC4000, XC4000E, or XC5200 via JTAG:

1. Turn 'on' the boundary scan circuitry.

   This can be done one of two ways, either via powerup or via a configured device with boundary scan enabled. If you want to do this via powerup, then just hold the $\overline{\text{INIT}}$ pin low when power is turned on. When V_{CC} has reached V_{CC}(min), then the TAP can be toggled to enter JTAG instructions. If you want to do this from a configured device, then just start toggling the JTAG port pins to go from test-logic-reset to run-test-idle.

2. Load the Xilinx Configure instruction into the IR.

   The Xilinx Configure instruction is 101(I_2 I_1 I_0). I_0 is the bit shifted in first into the IR.

3. After shifting in the Xilinx Configure instruction, make the Configure instruction the current JTAG instruction by going to the update-IR state. When TCK goes low in the update-IR state, the FPGA is now in the JTAG configuration mode and will start clearing the configuration memory.

   At this point, the user should be in the update-IR state in the TAP.

4. Once the Xilinx Configure instruction has been made current, the user must go from the update-IR state to the shift-DR state before the FPGA has finished clearing it's configuration memory.

   The approximate time it takes to clear an FPGA's configuration memory is: 2 * 1 us * (# of frames per device bitstream).

   If the user doesn't get to the shift-dr state before $\overline{\text{INIT}}$ goes high, then the bitstream will not be shifted into the FPGA in the right sequence and the device will not configure as expected.

5. Once $\overline{\text{INIT}}$ has gone high, the TAP should already be in the shift-DR state.

   In the shift-DR state, start shifting in the bitstream. Continue shifting in the bitstream until DONE has gone high and the startup sequence has finished.

   During the time you are shifting in the bitstream via the TAP, the configuration pins $\overline{\text{LDC}}$. HDC, $\overline{\text{INIT}}$, $\overline{\text{PROGRAM}}$, etc. all function as they normally do during non-JTAG configuration.

Some Additional Notes:

(a) If you want to power-up the FPGA in JTAG mode, this can be done by placing a pulldown of approximately 4.7 Kohms on the $\overline{\text{INIT}}$ pin. This pulldown has the merit of holding $\overline{\text{INIT}}$ low to allow the user to get into JTAG, *and* allow the user during JTAG configuration to 'see' the $\overline{\text{INIT}}$ pin; With the pulldown attached to $\overline{\text{INIT}}$, the user will see a drop of approximately 0.5V if $\overline{\text{INIT}}$ drops low.

The alternative to using a pulldown on the $\overline{\text{INIT}}$ pin on powerup is for the 'user' to hold $\overline{\text{INIT}}$ low during powerup, and once the TAP is in run-test-idle, release the $\overline{\text{INIT}}$ pin and pull it up to V_{CC}.

(b) It is possible to configure several 4K, 4KE, and/or 5K devices in a JTAG chain. But unlike non-JTAG daisy-chain configuration, this doesn't mean merging all the bitstreams into one bitstream. In the case of JTAG configuration of Xilinx devices in a JTAG chain, all devices, except the one being configured, will be placed in BYPASS mode. The one device in CONFIGURE will have its bitstream downloaded to it. After configuring this device it will be placed in BYPASS, and another device will be taken out of BYPASS into CONFIGURE.

(c) In general for the XC4000, XC4000E, and XC5200, if you are configuring these devices via JTAG, finish configuring the device first before executing any other

JTAG instructions. If the bitstream has not finished loading, then if you decide to execute some other JTAG instructions, then the configuration process via JTAG must be re-started from test-logic-reset.

(d) If boundary scan is not available after the FPGA is configured, then make sure that the release of I/Os is the last event in the startup sequence.

If boundary scan is not available, the FPGA is configured, and the I/Os are released before the startup sequence is finished, the FPGA will not respond to input signals and outputs won't respond at all.

READBACK – Readback through the TAP allows the user to access the readback features of the device, which would normally need to be accessed through user-specified pins. All limits of 'normal' readback are the same with readback through the TAP. Like regular readback, readback through the TAP is at a minimum of 10 KHz and at a maximum of 1 MHz. Like regular readback, the readback bistream through boundary scan has the same format.

Unlike regular readback, which can be done over and over again, readback through the TAP requires the following circuit:

1. In your schematic, or top-level synthesis design, instantiate the BSCAN and READBACK symbols.
2. Connect the BSCAN symbol pins TDI, TMS, TCK, and TDO to the boundary scan pads TDI, TMS, TCK, and TDO, respectively.
3. Next, connect the net between the TCK pad and TCK pin on the BSCAN symbol to an IBUF. Take the output of the IBUF and connect it to the CLK pin of the READBACK symbol. See Figure 8.
4. After entering the above circuit, compile the design to an .lca file.
5. Make the .bit file for the .lca file by using the following option with makebits:

   -f readclk:rdbk

   For example, at a unix prompt:

   % makebits -f readclk:rdbk designame

6. Now the FPGA is ready to perform consecutive readbacks.

   READBACK is performed by loading the IR with the READBACK instruction and then shifting out the captured data from the shift-dr state in the TAP.

   Perform the first readback by loading the IR with the READBACK instruction. This first readback must be finished, which means shifting out the *entire* readback bitstream. To be safe, shift out the entire bitstream and then send three additional TCK's.

7. After performing the first readback, another readback can be performed by going to the test-logic-reset state, and re-loading the READBACK instruction and performing the READBACK as described in the previous paragraph.

   In summary, consecutive readbacks are performed by starting from test-logic-reset, loading the IR with the READBACK instruction, shifting out the readback bitstream plus three additional TCK's, and then going back to the test-logic-reset state.

   Alternatively, if you do not want to go back to the test-logic-reset state, realize that after shifting out readback bitstream, a minimum of 3 additional clocks are needed on the readback register. So, after doing a readback, instead of going back to test-logic-reset, a user can opt to execute some other JTAG instruction, and then perform another readback.

   Also, this above procedure is only needed if you intend to do more than 1 readback. If you intend only to do a readback once, then connection between the BSCAN symbol and the READBACK symbol is not needed. In that case, all that is needed is the BSCAN symbol instantiated with the boundary scan pads (TDI, TMS, TCK, & TDO) on the top-level of the design.

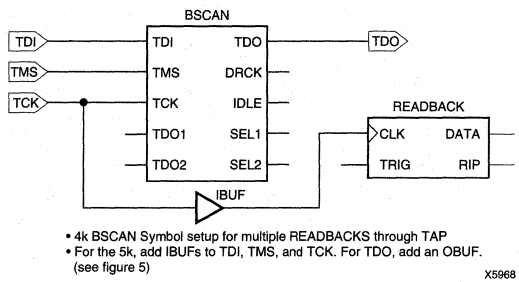


Figure 8: Symbol Setup for Multiple Readbacks

Boundary Scan Description Language Files

Boundary Scan Description Language (BSDL) files describe boundary-scan-capable parts in a standard format used by automated test-generation software. The order and function of bits in the boundary-scan data register are included in this description.

BSDL files are available via the Xilinx BBS (408-559-9327)

Bibliography

The following publications contains information about the IEEE Standard 1149.1, and should be consulted for gen-

eral boundary-scan information beyond the scope of this application note.

Colin M. Maunder & Rodham E. Tulloss. *The Test Access Port and Boundary Scan Architecture.* IEEE Computer Society Press, 10662 Los Vaqueros Circle, P.O. BOX 3014, Los Alamitos, CA 90720-1264.

John Fluke Mfg. Co. Inc. *The ABC of Boundary Scan Test.* John Fluke Mfg. Co. Inc., P.O. BOX 9090, Everett, WA 98206.

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