XC95144 In-System Programmable CPLD

April, 1997 (Version 1.0)

Advanced Product Specification

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 144 macrocells with 3,200 usable gates
- Up to 133 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 100-pin PQFP, and 160-pin PQFP packages

Description

The XC95144 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of eight 36V18 Function Blocks, providing 3,200 usable gates with propagation delays of 7.5 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95144 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

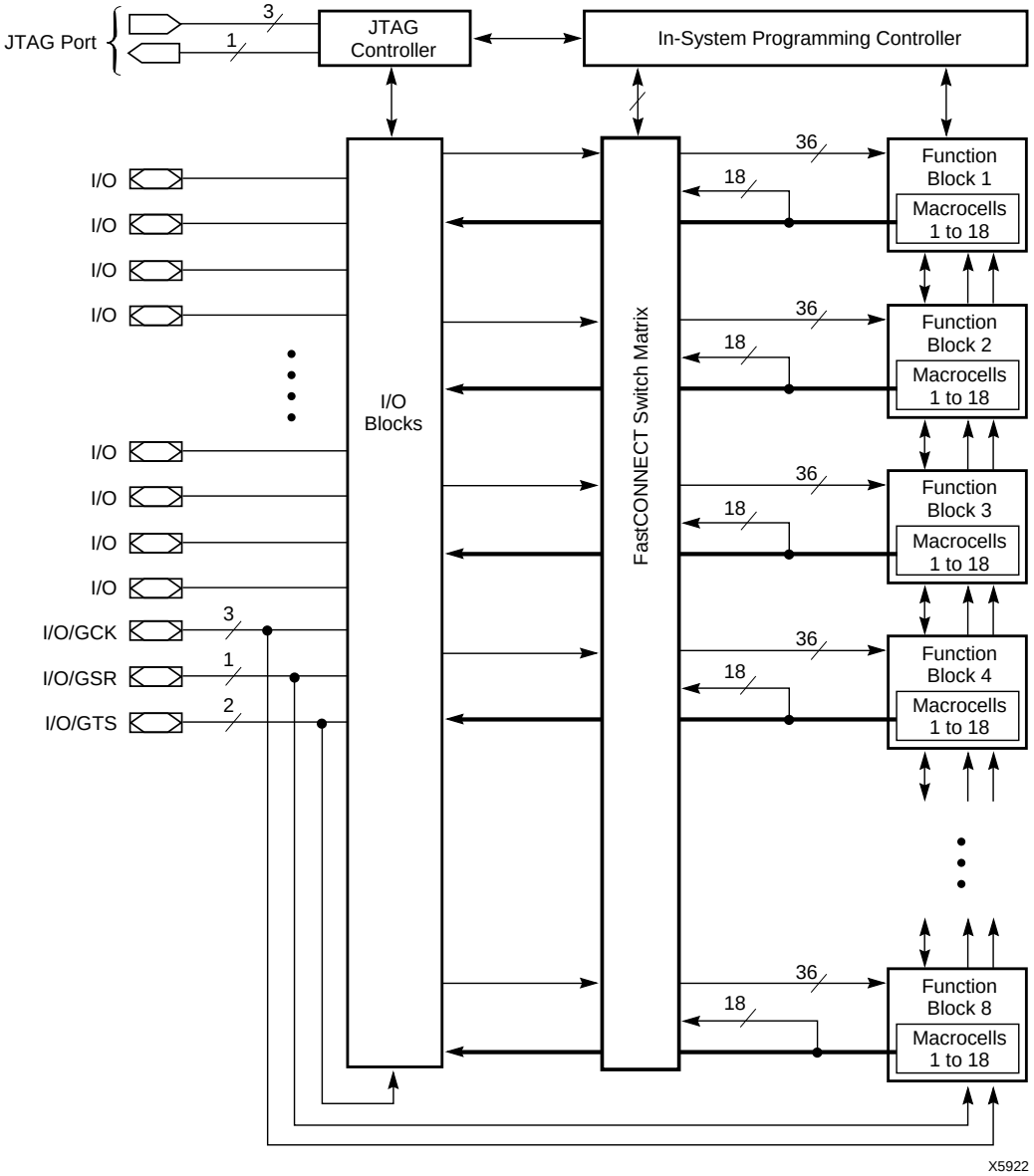

Figure 1: XC95144 Architecture

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

XC95144 I/O Pins

Function Block	Macrocell	PQ100	PQ160	BScan Order	Notes
1	1	–	38	429	
1	2	15	21	426	
1	3	16	22	423	
1	4	–	25	420	
1	5	17	23	417	
1	6	18	24	414	
1	7	–	32	411	
1	8	19	26	408	
1	9	20	28	405	
1	10	–	27	402	
1	11	21	29	399	
1	12	22	30	396	
1	13	–	39	393	
1	14	24	33	390	[1]
1	15	25	36	387	[1]
1	16	–	34	384	
1	17	26	35	381	
1	18	–	–	378	
2	1	–	3	375	
2	2	4	4	372	[1]
2	3	–	14	369	
2	4	–	158	366	
2	5	5	6	363	[1]
2	6	6	11	360	[1]
2	7	–	7	357	
2	8	8	8	354	
2	9	9	12	351	
2	10	–	9	348	
2	11	10	13	345	
2	12	11	15	342	
2	13	–	5	339	
2	14	12	17	336	
2	15	13	18	333	
2	16	–	16	330	
2	17	14	19	327	
2	18	–	–	324	

Function Block	Macrocell	PQ100	PQ160	BScan Order	Notes
3	1	–	53	321	
3	2	27	37	318	
3	3	–	43	315	
3	4	–	45	312	
3	5	29	42	309	[1]
3	6	30	44	306	
3	7	–	48	303	
3	8	31	47	300	
3	9	32	49	297	
3	10	–	50	294	
3	11	34	54	291	
3	12	35	56	288	
3	13	–	55	285	
3	14	36	57	282	
3	15	37	58	279	
3	16	–	52	276	
3	17	38	59	273	
3	18	–	–	270	
4	1	–	149	267	
4	2	92	143	264	
4	3	–	130	261	
4	4	–	153	258	
4	5	93	144	255	
4	6	94	145	252	
4	7	–	151	249	
4	8	95	146	246	
4	9	96	148	243	
4	10	–	147	240	
4	11	97	152	237	
4	12	98	154	234	
4	13	–	150	231	
4	14	99	156	228	
4	15	1	159	225	[1]
4	16	–	155	222	
4	17	3	2	219	[1]
4	18	–	–	216	

Notes: [1] Global control pin
Macrocell outputs to package pins subject to change, contact factory for latest information. Power, GND, JTAG and Global Signals are fixed.

XC95144 I/O Pins (continued)

Function Block	Macrocell	PQ100	PQ160	BScan Order	Notes
5	1	–	65	213	
5	2	39	60	210	
5	3	–	74	207	
5	4	–	76	204	
5	5	41	62	201	
5	6	42	63	198	
5	7	–	67	195	
5	8	43	64	192	
5	9	44	68	189	
5	10	–	84	186	
5	11	45	69	183	
5	12	48	72	180	
5	13	–	66	177	
5	14	51	77	174	
5	15	52	79	171	
5	16	–	78	168	
5	17	54	82	165	
5	18	–	–	162	
6	1	–	–	159	
6	2	79	124	156	
6	3	–	125	153	
6	4	–	122	150	
6	5	80	126	147	
6	6	81	129	144	
6	7	–	131	141	
6	8	82	133	138	
6	9	83	134	135	
6	10	–	128	132	
6	11	84	135	129	
6	12	87	138	126	
6	13	–	132	123	
6	14	88	139	120	
6	15	89	140	117	
6	16	–	123	114	
6	17	91	142	111	
6	18	–	–	108	

Function Block	Macrocell	PQ100	PQ160	BScan Order	Notes
7	1	–	–	105	
7	2	55	86	102	
7	3	–	93	99	
7	4	–	89	96	
7	5	56	88	93	
7	6	57	90	90	
7	7	–	83	87	
7	8	58	92	84	
7	9	60	95	81	
7	10	–	91	78	
7	11	61	96	75	
7	12	62	97	72	
7	13	–	85	69	
7	14	63	98	66	
7	15	65	101	63	
7	16	–	87	60	
7	17	66	102	57	
7	18	–	–	54	
8	1	–	–	51	
8	2	67	103	48	
8	3	–	107	45	
8	4	–	105	42	
8	5	68	104	39	
8	6	69	106	36	
8	7	–	118	33	
8	8	70	108	30	
8	9	72	111	27	
8	10	–	114	24	
8	11	73	113	21	
8	12	74	115	18	
8	13	–	119	15	
8	14	75	116	12	
8	15	76	117	9	
8	16	–	112	6	
8	17	78	109	3	
8	18	–	–	0	

XC95144 Global, JTAG and Power Pins

Pin Type	PQ100	PQ160
I/O/GCK1	24	33
I/O/GCK2	25	35
I/O/GCK3	29	42
I/O/GTS1	5	6
I/O/GTS2	6	8
I/O/GTS3	3	2
I/O/GTS4	4	4
I/O/GSR	1	159
TCK	50	75
TDI	47	71
TDO	85	136
TMS	49	73
V_{CCINT} 5 V	7,59,100	10,46,94,157
V_{CCIO} 3.3 V/5 V	28,40,53,90	1,41,61,81,121,141
GND	2,23,33,46,64,71, 77,86	20,31,40,51,70,80, 99,100,110,120,127, 137,160
No Connects	–	–