1997 Master Selection Guide

Master Selection Guide

A Complete Guide to Zilog's ICs and Support Product Solutions

MS96COR3200

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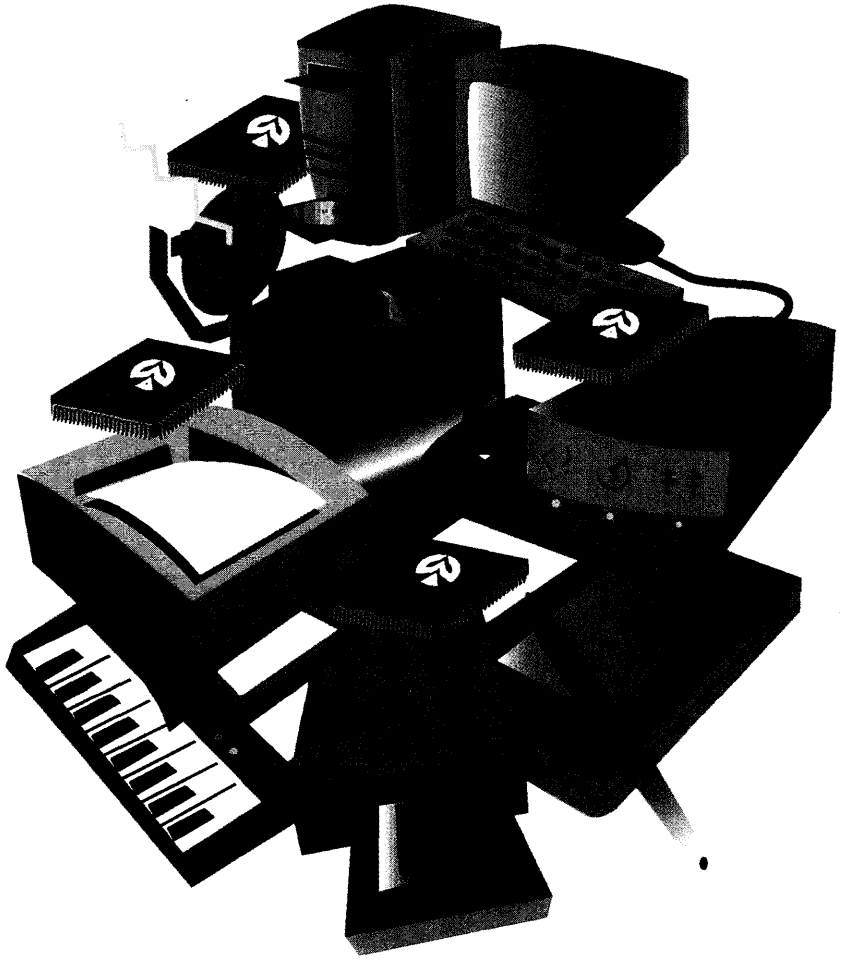


Breaking New Barriers

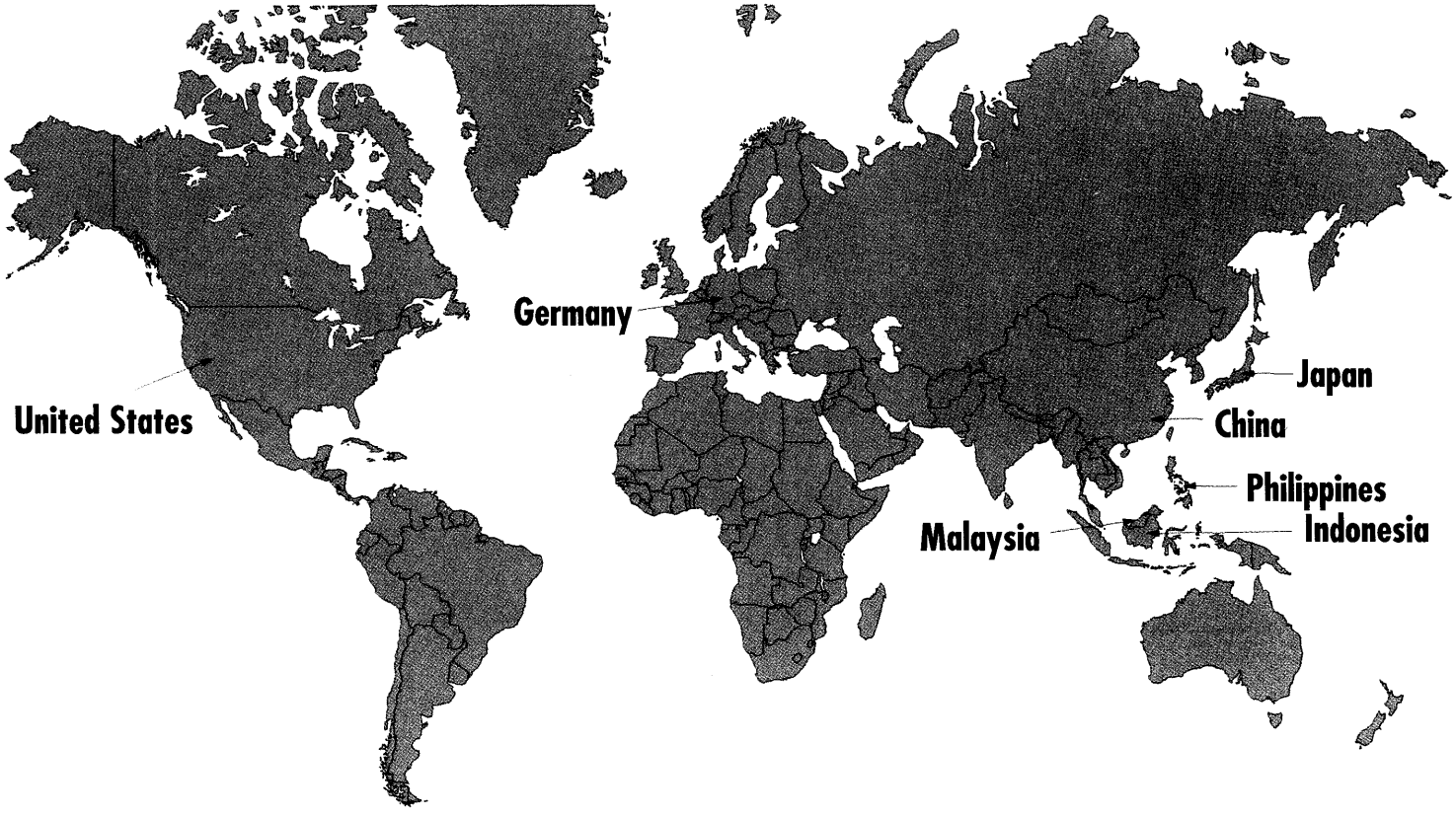
Worldwide Sales Presence

Worldwide Sales Network

– 26 Zilog sales offices

– More than 120 distributor and representative locations

Zilog Manufacturing Facilities



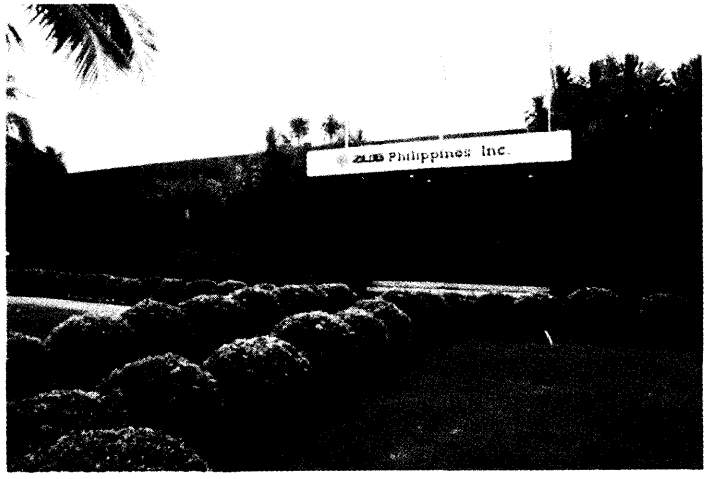
Headquarters — Campbell, CA

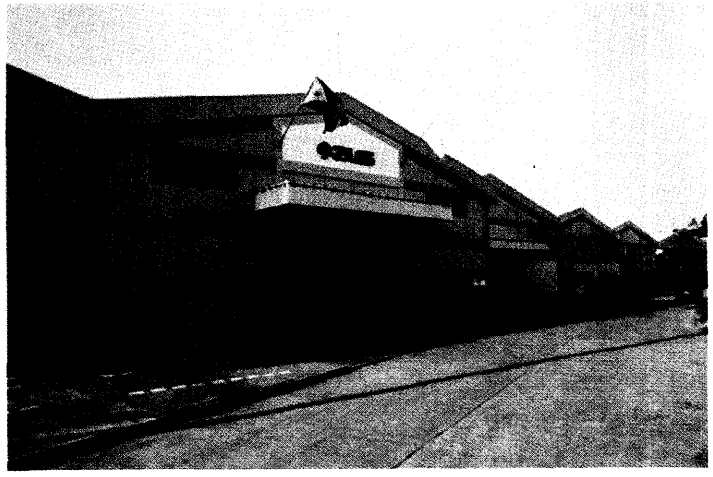
- Zilog Formed: 1974
- Management-Led Buyout from Exxon: June 1989
- Successful Public Offering: February 1991
- Follow-On Offerings: February 1992 February 1993
- NYSE:ZLG
- 1,500 Zilog Employees Worldwide

The company is an innovator in the development, design and manufacture of integrated circuits for the consumer electronics, computer peripheral and communications markets.

ZILOG

Test and Assembly





- Two Sites in Manila, the Philippines
- 82,576 Sq. Ft. Facility
- Subcontractors: Indonesia and Malaysia

Wafer Fabrication

Locations: Nampa, Idaho

Building I

- Five-inch wafers
- 109,000 sq. ft. facility

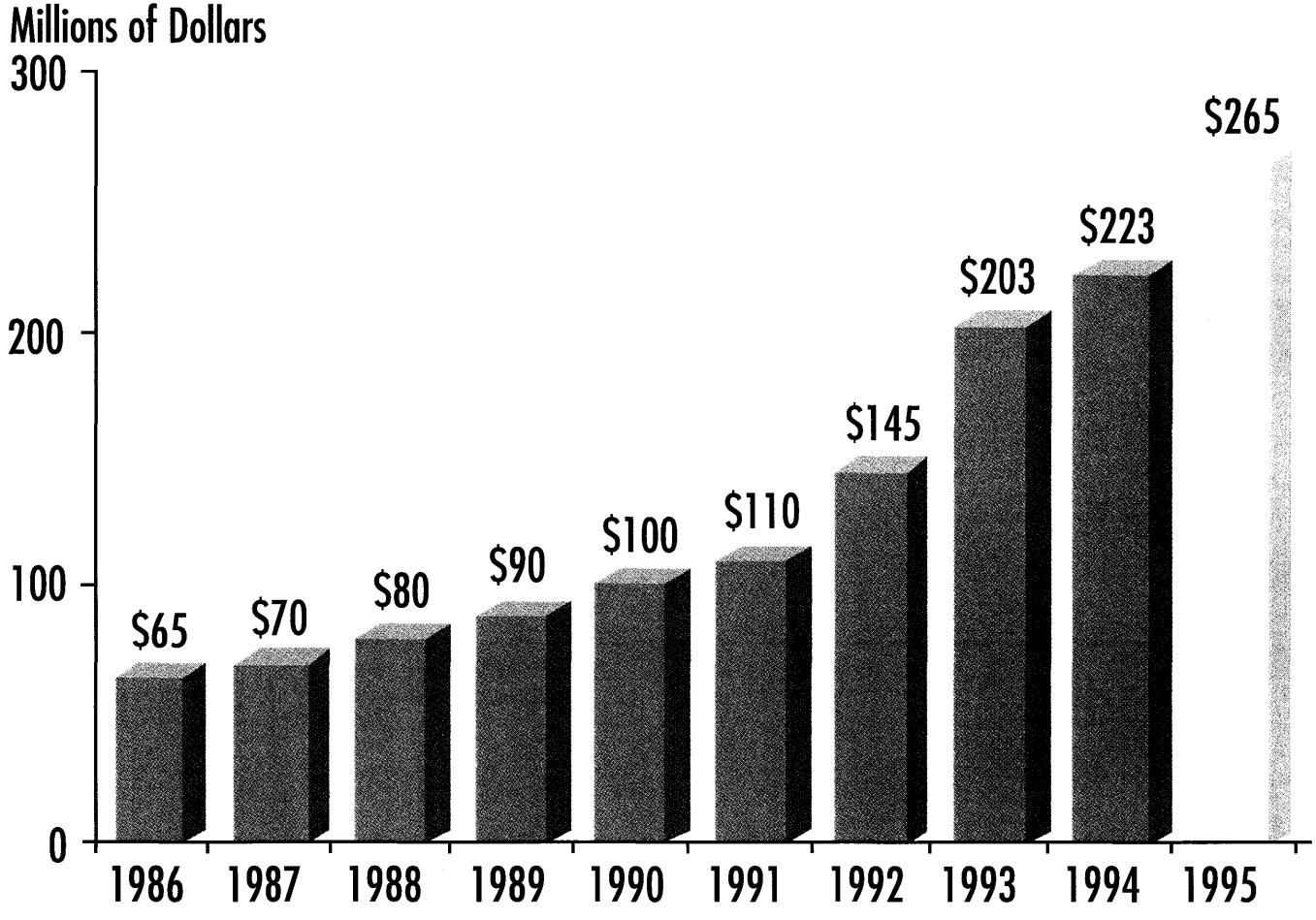
Building II

- Eight-inch wafers in submicron sizes
- 144,000 sq. ft. facility
- Mini-environments with robotic handling

Subcontractors: Japan and Germany

ZiLOG

Sales Growth



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ZiLOG

8-Bit Microcontrollers

Z86C02/E02/L02

LOW-COST, 512-BYTE ROM MICROCONTROLLERS

1

FEATURES

Device	ROM (KB)	RAM* (Bytes)	Speed (MHz)	Auto Latch	Permanent WDT
Z86C02	512	61	8	Optional	Optional
Z86E02	512	61	8	Optional	Optional
Z86L02	512	61	8	Optional	Optional

Note: *General-Purpose

- 18-Pin DIP and SOIC Packages
- 0°C to 70°C Standard Temperature
  –40°C to 105°C Extended Temperature
  (Z86C02/E02 only)
- 3.0V to 5.5V Operating Range (Z86C02)
  4.5V to 5.5V Operating Range (Z86E02)
  2.0V to 3.9V Operating Range (Z86L02)
- 14 Input / Output Lines
- Five Vectored, Prioritized Interrupts from Five Different Sources
- Two On-Board Comparators
- Software Enabled Watch-Dog Timer (WDT)
- Programmable Interrupt Polarity
- Two Standby Modes: STOP and HALT
- Low-Voltage Protection
- ROM Mask/OTP Options:
  - Low-Noise (Z86C02/E02 only)
  - ROM Protect
  - Auto Latch
  - Permanent Watch-Dog Timer (WDT)
  - RC Oscillator (Z86C02/L02 Only)
  - 32 KHz Operation (Z86C02/L02 Only)
- One Programmable 8-Bit Counter/Timer with a 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer
- On-Chip Oscillator that Accepts RC, Crystal, Ceramic Resonator, LC, or External Clock Drive (C02/L02 only)
- On-Chip Oscillator that Accepts RC or External Clock Drive (Z86E02 SL1903 only)
- On-Chip Oscillator that Accepts Crystal, Ceramic Resonator, LC, or External Clock Drive (Z86E02 only)
- Clock-Free WDT Reset
- Low-Power Consumption (50mw)
- Fast Instruction Pointer (1.5µs @ 8 MHz)
- Fourteen Digital Inputs at CMOS Levels; Schmitt-Triggered

GENERAL DESCRIPTION

Zilog's Z86C02/E02/L02 microcoontrollers (MCUs) are members of the Z8® single-chip microcontroller family which offer easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the MCU's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

One on-chip counter/timer, with a large number of user selectable modes, off-load the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

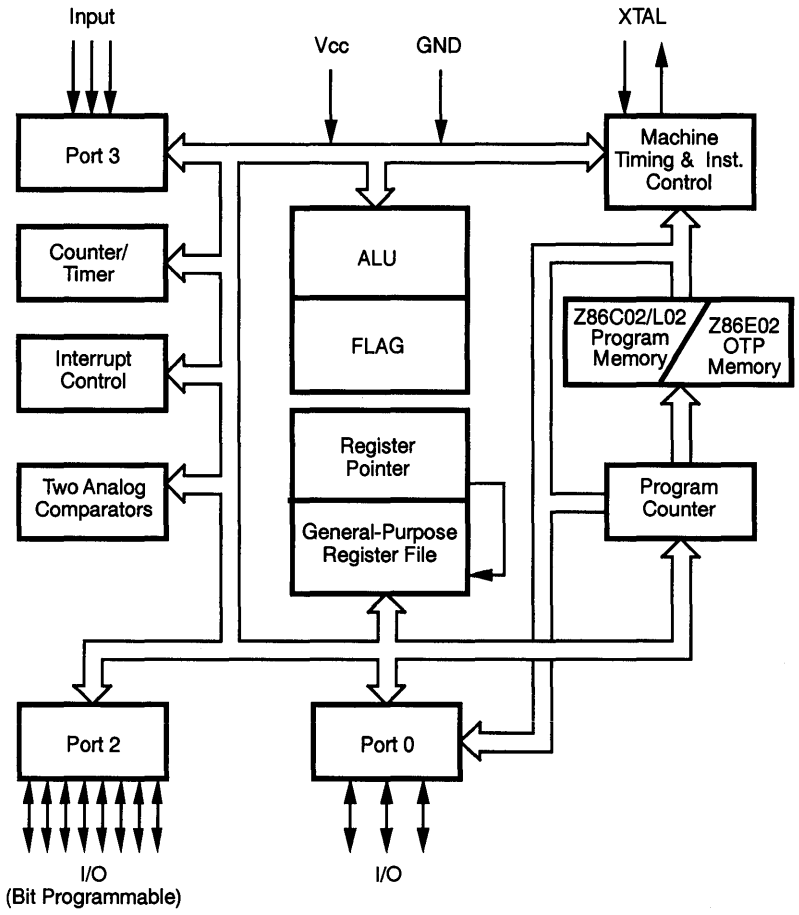


Figure 1. Z86C02/E02/L02 Functional Block Diagram

Z86C04/C08

CMOS Z8® 8-BIT LOW-COST 1K/2K-ROM MICROCONTROLLERS

FEATURES

Part Number	ROM (Kbytes)	RAM* (Bytes)	Speed (MHz)	Auto Latch	Permanent WDT
Z86C04	1	125	8	Optional	Optional
Z86C08	2	125	12	Optional	Optional

Note: * General-Purpose

- 18-Pin DIP and SOIC Packages
- 3.0V to 5.5V Operating Range
- 14 Input / Output Lines
- Six Vectored, Prioritized Interrupts from Six Different Sources
- ROM Mask Options:
  - Low Noise
  - ROM Protect
  - Auto Latch (C04/C08)
  - Permanent Watch-Dog Timer (WDT) (C04/C08)
  - RC Oscillator
  - 32 KHz Operation
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer
- On-Chip Oscillator that Accepts RC, Crystal, Ceramic Resonance, LC, or External Clock Drive
- Clock-Free WDT Reset
- Two On-Board Comparators
- Low-Power Consumption (50mw)
- Fast Instruction Pointer (1.5µs @ 8 MHz, 1.0 µs @ 12 MHz)
- Fourteen Digital Inputs at CMOS Levels; Schmitt-Triggered
- Software Enabled Watch-Dog Timer
- Programmable Interrupt Polarity
- Two Standby Modes: STOP and HALT
- Low-Voltage Protection

GENERAL DESCRIPTION

Zilog's Z86C04/C08 Microcontrollers (MCU) are members of the Z8® single-chip microcontroller family which offer easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the Z86C04/C08 dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, off-load the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions.

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

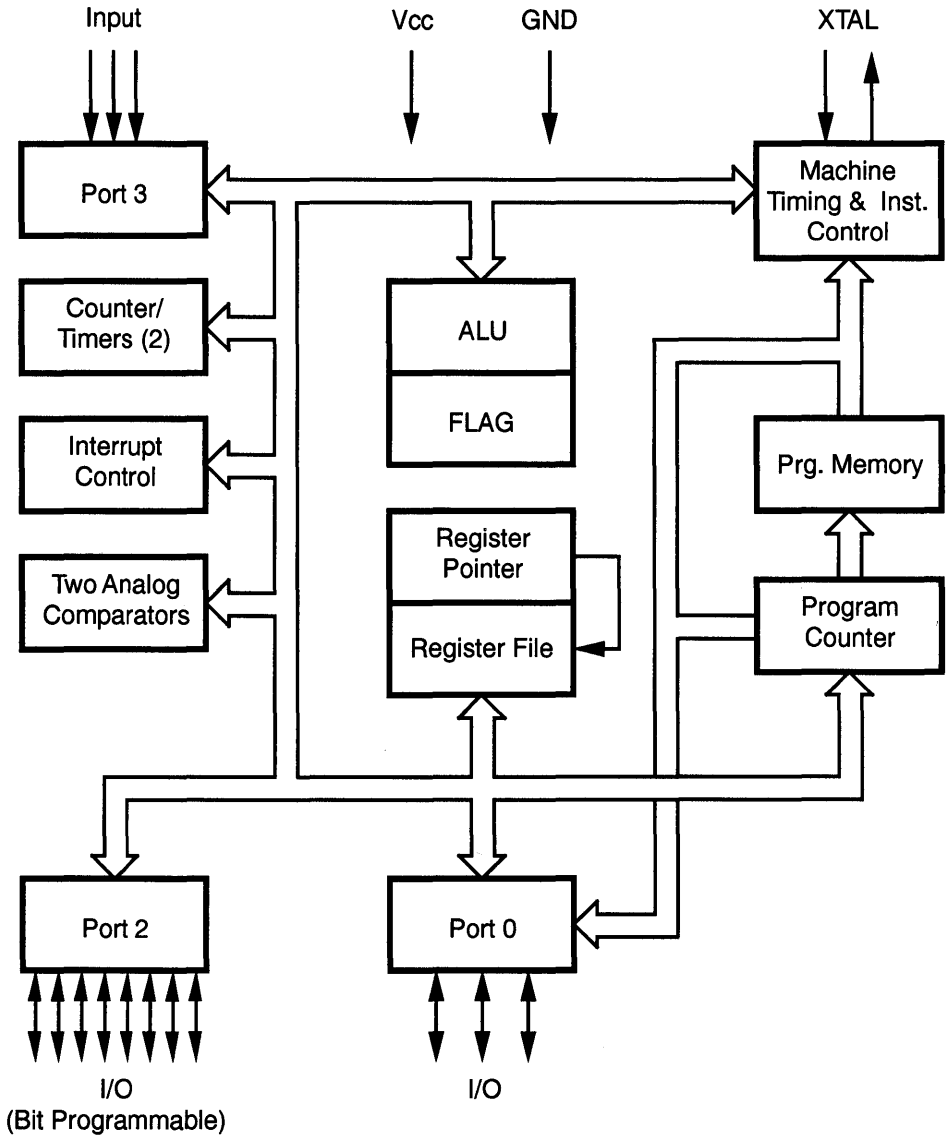


Figure 1. Z86C04/C08 Functional Block Diagram

Z86C30/C31/C32/C40

CMOS Z8® CONSUMER CONTROLLER PROCESSOR

FEATURES

Part	ROM (Kbyte)	RAM* (Byte)	Speed (MHz)
Z86C30	4	237	16
Z86C31	2	125	12
Z86C32	2	237	12
Z86C40	4	236	16

* General-Purpose

- 28-Pin DIP, 28-Pin SOIC, 28-Pin PLCC Packages (Z86C3X)
  40-Pin DIP, 44-Pin PLCC/QFP Packages (Z86C40)
- 3.0- to 5.5-Volt Operating Range
- Low-Power Consumption
- –40°C to +105°C Operating Range
- Expanded Register File (ERF)
- 32 Input/Output Lines (C40)
  24 Input/Output Lines (C3X)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer/Power-On Reset
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86C3X/C40 Consumer Controller Processors are members of the Z8® single-chip microcontroller family offering a unique register-to-register architecture that avoids accumulator bottlenecks and offers fast execution of code.

Three address spaces, the Program Memory, Register File, and Expanded Register File (ERF), support a wide range of memory configurations. Through the ERF, the designer has access to three additional control registers that provide extra peripheral devices, I/O ports, and register addresses. The rest of the ERF is not physically implemented and is open for future expansion.

For applications demanding powerful I/O capabilities, the Z86C3X/C40's dedicated input and output lines are grouped into three and four ports, respectively, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O datacommunications.

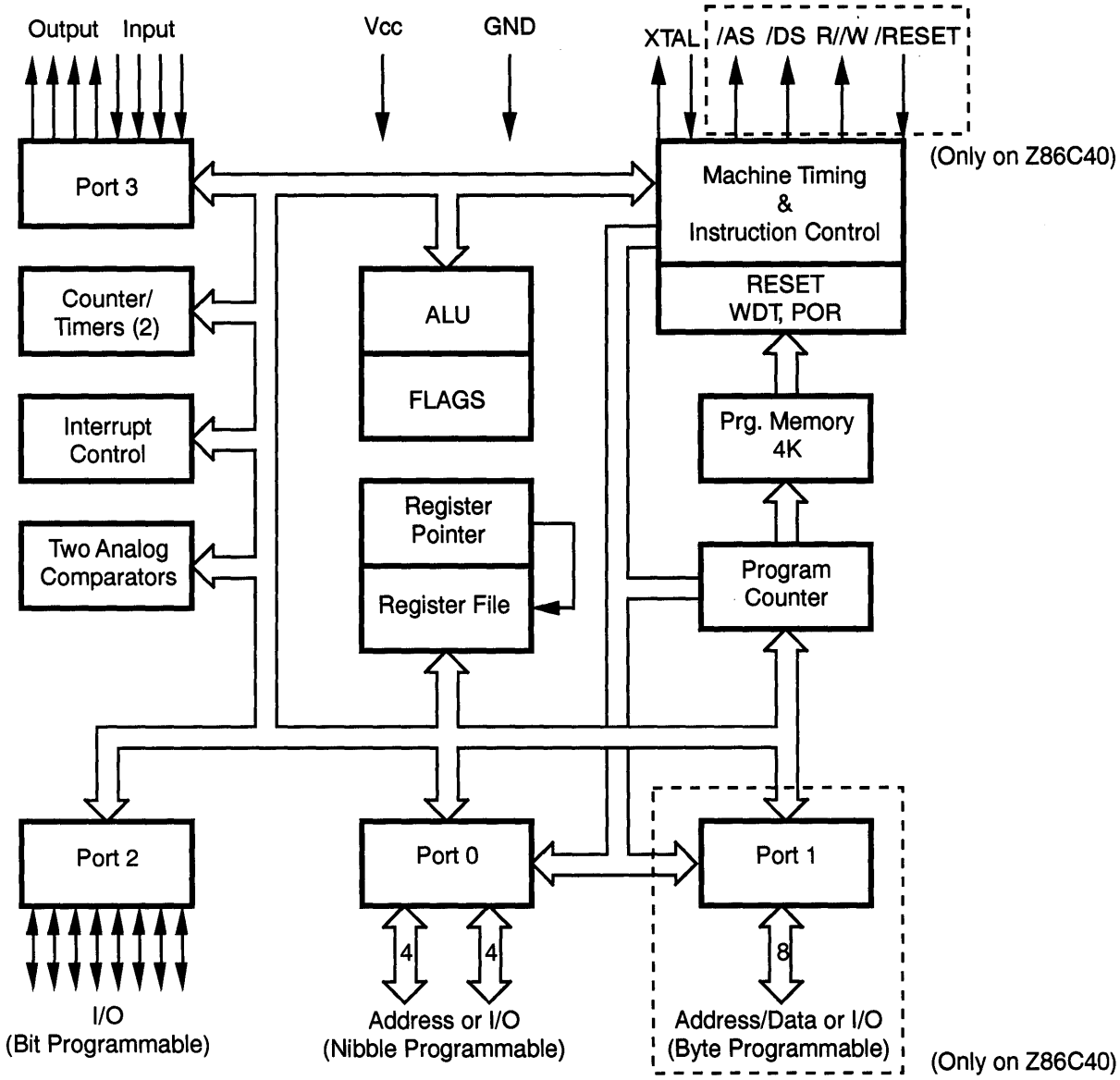
With ROM/ROMless selectivity, the Z86C40 provides both external memory and pre-programmed ROM, which enables these Z8 microcontrollers to be used in high-volume applications, or where code flexibility is required.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z86C33/C43

CMOS Z8®
CONSUMER CONTROLLER PROCESSOR

FEATURES

Part	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z86C33	4	237	12, 16
Z86C43	4	236	12, 16

* General-Purpose

- 40-Pin DIP, 44-Pin PLCC and QFP Packages (C43)
  28-Pin DIP, 28-Pin SOIC, 28-Pin PLCC (C33)
- 3.0- to 5.5-Volt Operating Range
- Clock Free Watych-Dog Timer (WDT) Reset
- –40°C to +105°C Operating Range
- Expanded Register File (ERF)
- 32 Input/Output Lines (C43)
  24 Input/Output Lines (C33)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86C33/C43 Consumer Controller Processor (CCP™) is a member of Zilog's Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. This low-power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C33/C43 features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, Data Memory, and ERF. The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The ERF consists of three control registers

For applications demanding powerful I/O capabilities, the Z86C33 provides 24 pins, and the Z86C43 provides 32 pins dedicated to input and output. These lines are configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z86C33/C43 offers two on-chip counter/timers with a large number of user-selectable modes.

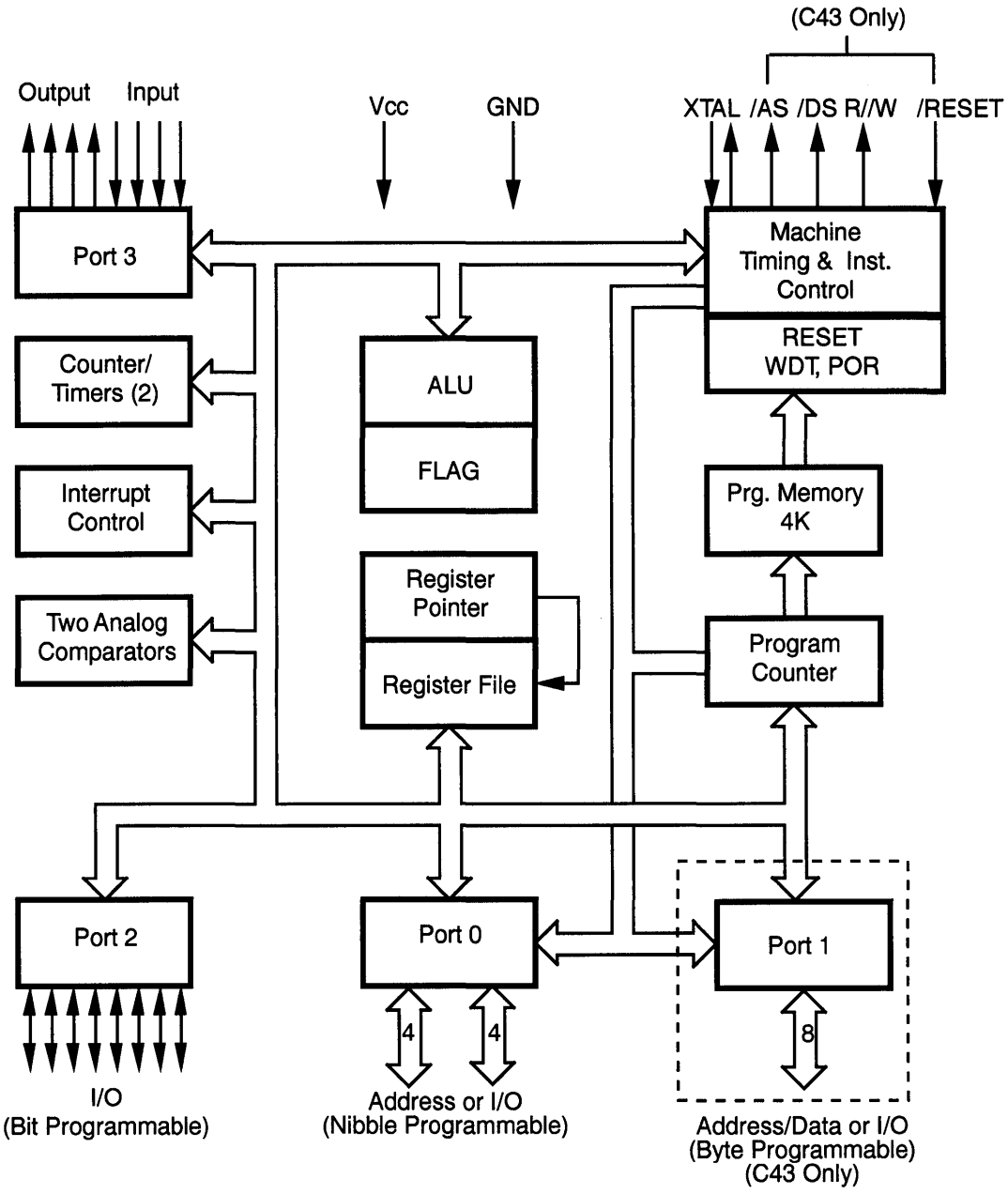
With ROM/ROMless selectivity, the Z86C43 provides both external memory and pre-programmed ROM, which enables this Z8 microcontroller to be used in high-volume applications, or where code flexibility is required.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z86C60/65

CMOS Z8®
32K ROM MICROCONTROLLER

FEATURES

Part	ROM (KB)	RAM* (Bytes)	I/O	Speed (MHz)	28-pin DIP
Z86C60	16	256	22	16	X
Z86C65	32	256	22	16	X

*General-Purpose

- 28-Pin DIP Package
- 3.0V to 5.5V Operating Range
- Low-Power Consumption: 200 mW
- Fast Instruction Pointer: 0.75 µs @ 16 MHz
- Two Standby Modes: STOP and HALT
- Low EMI Mode Option
- Auto Latches
- Two Programmable 8-Bit Counter/Timers Each with 6-Bit Programmable Prescaler
- Three Vectored, Priority Interrupts from Three Different Sources
- On-Chip Oscillator that Accepts a Crystal Ceramic Resonator, LC, or External Clock Source
- ROM Mask Options:
  - ROM Protect
  - RAM Protect

GENERAL DESCRIPTION

The Z86C60/65 microcontrollers introduce a new level of sophistication to single-chip architecture. The Z86C65 is a member of the Z8 single-chip microcontroller family with 32 Kbytes of ROM and 256 bytes of RAM. The Z86C60 is identical, except that it only has 16 Kbytes of ROM.

The Z86C60/65 are housed in a 28-pin DIP package, and manufactured in CMOS technology. The Z86C96 ROMless Z8 will support the Z86C60/65.

Zilog's CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C60/65 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C60/65 fulfills this with 22 pins dedicated to input and output. These lines are grouped into four ports. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Data Memory, and 236 General-Purpose Registers.

To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C60/65 offers two on-chip counter/timers with a large number of user selectable modes.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION

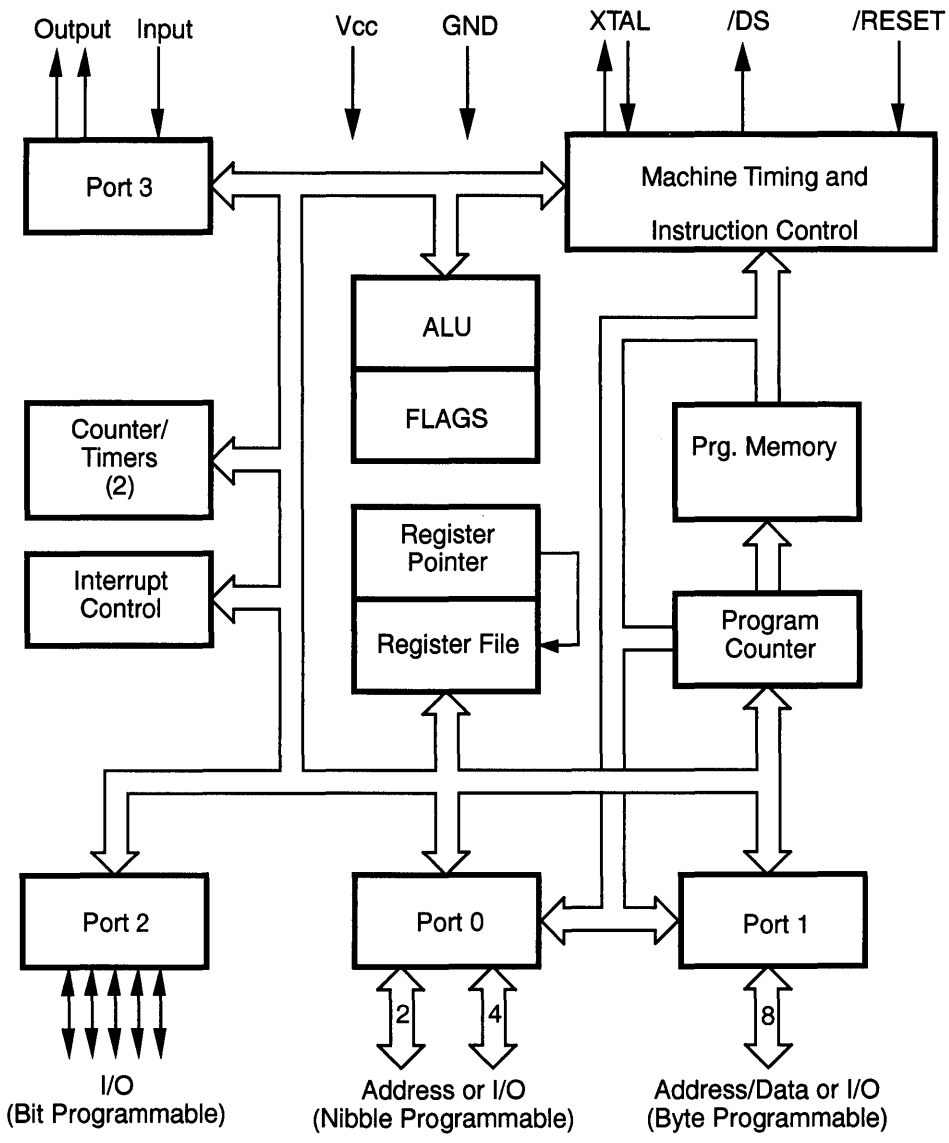


Figure 1. Z86C60/65 Functional Block Diagram

Z86C61/62

CMOS Z8® MICROCONTROLLER

FEATURES

ROM (Kbytes)	RAM* (Bytes)	I/O Lines	Speed (MHz)	Pin Count/ Package
16	236	32	5	40-DIP 44-PLCC 44-QFP

* General-Purpose

- 4.5- to 5.5-Volt Operating Range
- 0°C to 70°C Operating Temperature Range
- Expanded Register File
- Low-Power Consumption
- On-Chip Asynchronous Receiver/Transmitter (UART)
- Two On-Chip Counter/Timers
- On-Chip RC Oscillator

GENERAL DESCRIPTION

The Z86C61/62 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C61/62 is a member of the Z8 single-chip microcontroller family with 16 Kbytes of ROM and 236 bytes of general-purpose RAM.

The MCU is housed in 40-pin DIP, 44-pin Leaded Chip Carrier and 44-pin Quad Flat Pack packages and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin versions only. Having the ROM/ROMless selectively, the MCU offers both external memory and preprogrammed ROM which enables this Z8 microcontroller to be used in high volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C61/62 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced consumer applications.

The device is well suited to applications demanding powerful I/O capabilities. The Z86C61/62 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

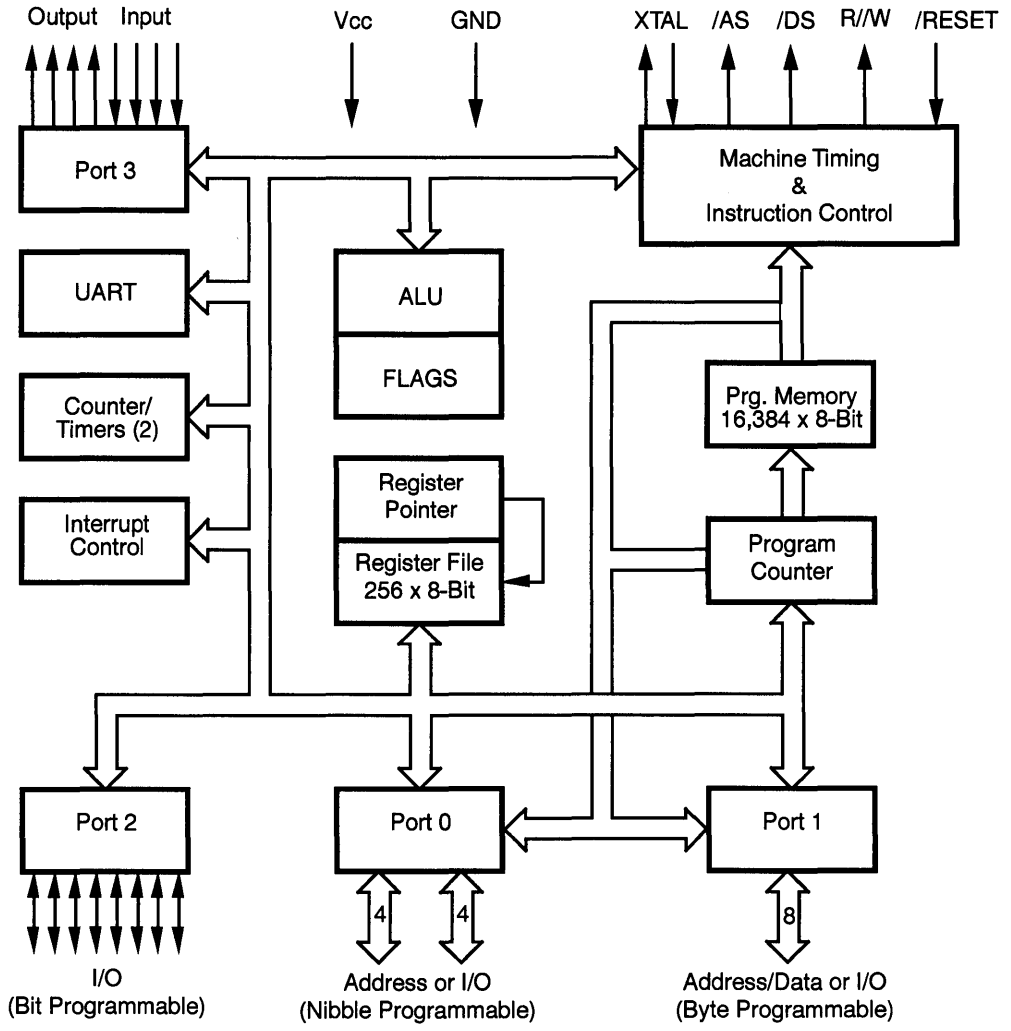
There are three basic address spaces available to support this wide range of configuration: program memory, data memory and 236 general-purpose registers.

To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C61/62 offers two on-chip Counter/Timers with a large number of user selectable modes, and a Asynchronous Receiver/Transmitter (UART - see block diagram).

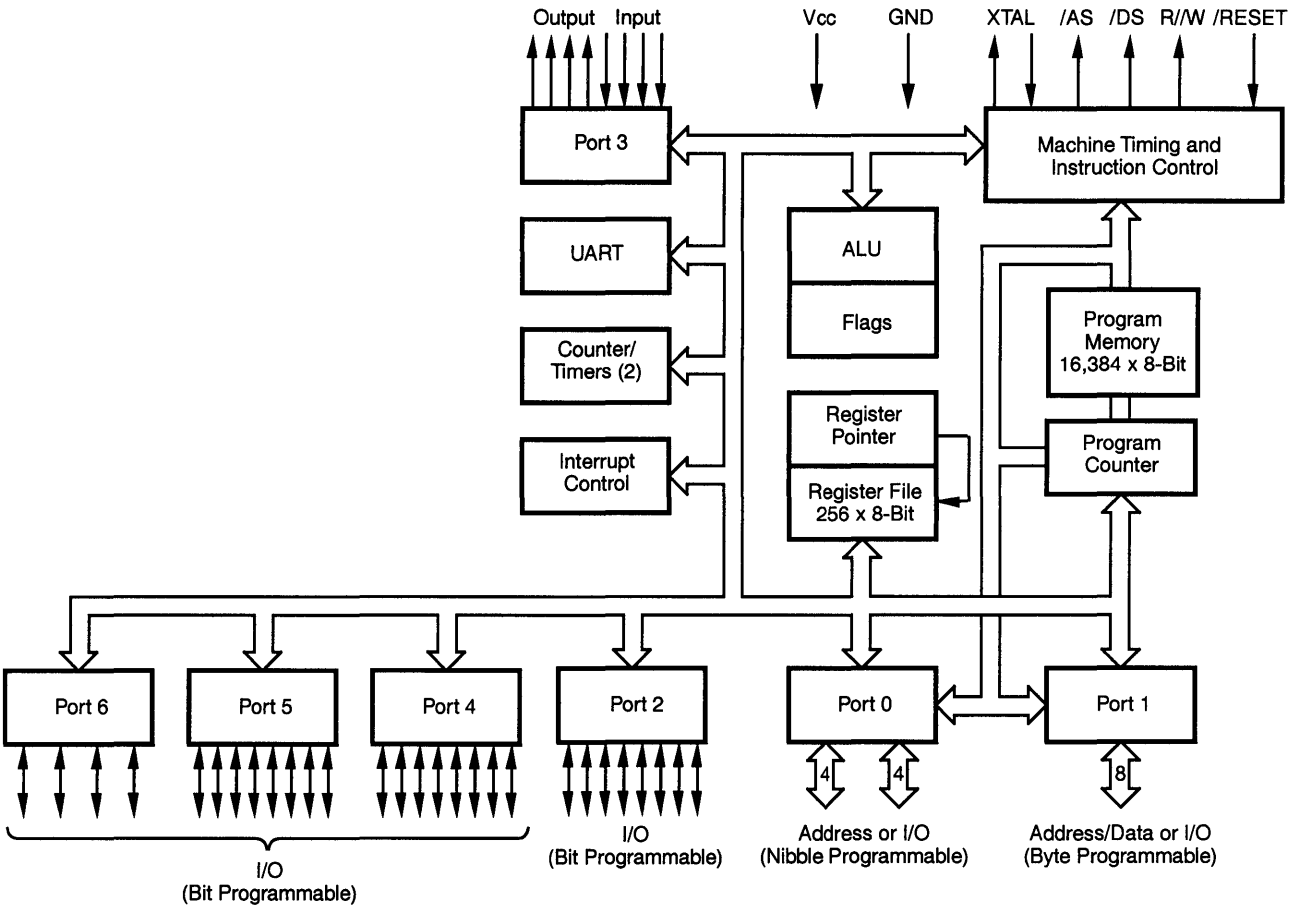
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}



Functional Block Diagram



Z86C62 Functional Block Diagram

Z86C63/64

CMOS Z8®
32K ROM MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C63/64 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C63/64 is a member of the Z8 single-chip microcontroller family with 32 Kbytes of ROM and 256 bytes of RAM.

The Z86C63 is housed in a 40-pin DIP, and a 44-pin PLCC package, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin version only. The Z86C64 is housed in a 64-pin DIP, and a 68-pin PLCC. Both versions of the Z86C64 have the ROMless pin option, which allows both external memory and preprogrammed ROM, enabling this Z8 microcontroller to be used in high-volume applications or where code flexibility is required. The Z86C96 ROMless Z8 will support the Z86C63/64.

Zilog's CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C63/64 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C63 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports with eight lines each. The Z86C64 has 52 pins for input and output, and these lines are grouped into six, 8-bit ports and one 4-bit port. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Data Memory, and 236 General-Purpose Registers.

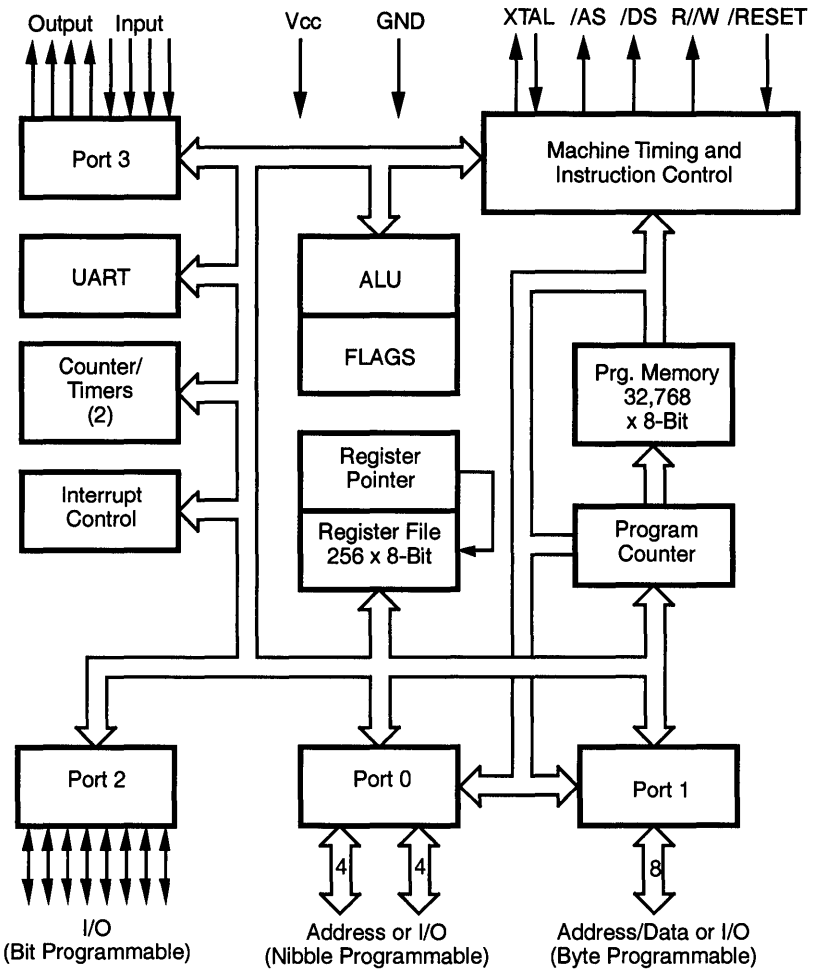
To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C63/64 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Block Diagrams).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

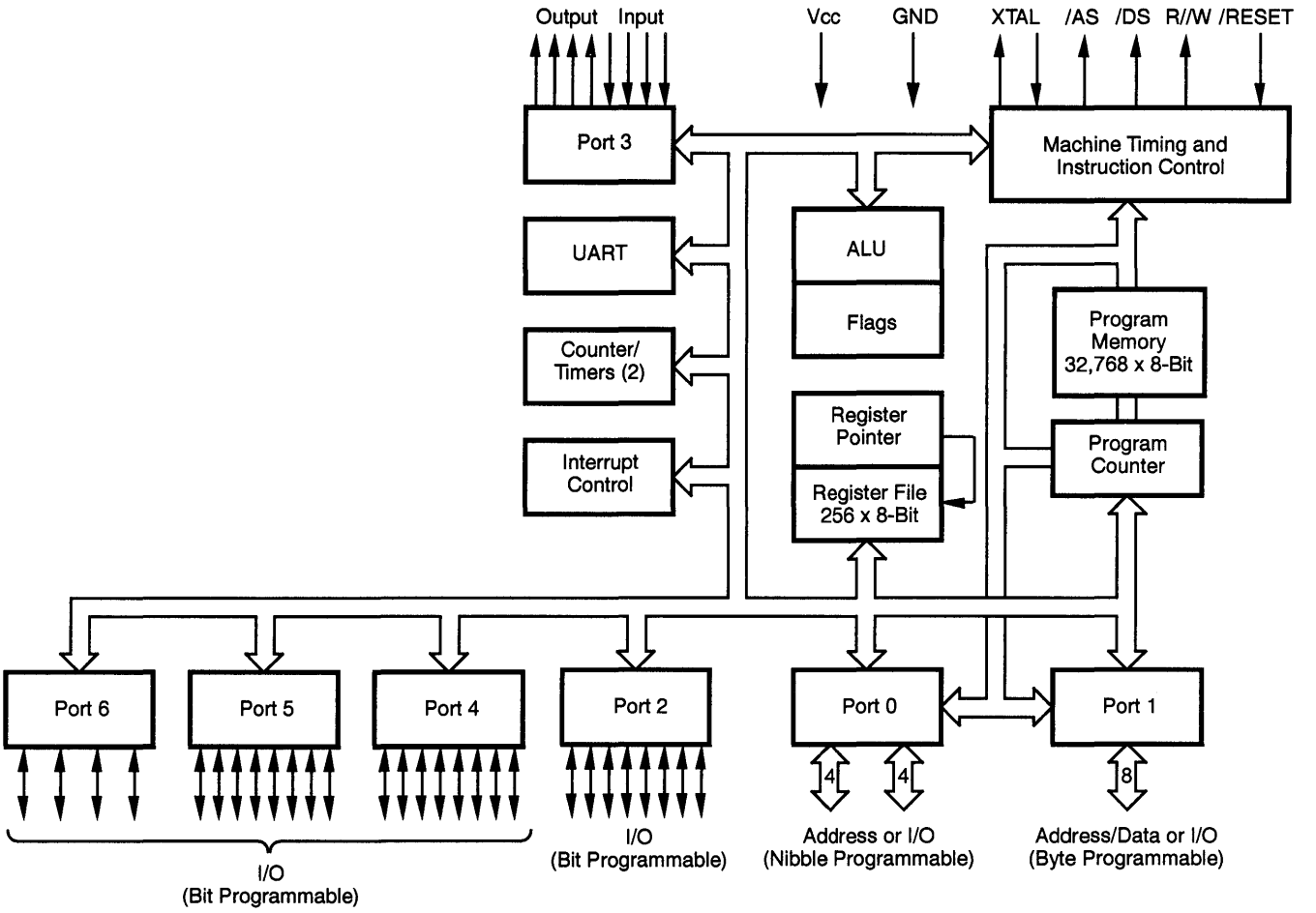
Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION



Z86C63 Functional Block Diagram



Z86C64 Functional Block Diagram

Z86C83/C84

Z8® MCU MICROCONTROLLERS

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86C83	4	237	21	3.0V to 5.5V
Z86C84	4	237	17	3.0V to 5.5V

Note: * General-Purpose

- 28-Pin DIP, SOIC, and PLCC Packages
- Clock Speed: 16 MHz
- Three Expanded Register Groups
- 8-Channel, 8-Bit A/D Converter with Track and Hold, and Unique R-Ladder A_{GND} Offset Control
- Z86C84 has two 8-Bit D/A Converters with Programmable Gain Stages, 3 µs Settling Time
- Six Vectored, Prioritized Interrupts from Six Different Sources
- Two Analog Comparator Inputs with Programmable Interrupt Polarity
- Two Programmable 8-Bit Timers, each with a 6-Bit Programmable Prescaler
- Auto Latch Mask Option for P00, P01, and P02
- Power-On Reset (POR) Timer
- Permanent Watch-Dog Timer (WDT) Mask Option
- Software-Programmable Pull-Up Resistors
- On-Chip Oscillator for Crystal, Resonator or LC

GENERAL DESCRIPTION

The Z86C83/C84 Consumer Controller Processors (CCP™) are full-featured members of the CMOS Z8 microcontroller family offering a unique register-to-register architecture that avoids accumulator bottlenecks for higher code efficiency than RISC processors.

The Z86C83/C84 are designed to be used in a wide variety of embedded control applications, such as appliances, process controls, keyboards, security systems, battery chargers, and automotive modules.

For applications requiring powerful I/O capabilities, the Z86C83/C84 devices can have up to 21/17 (C83/C84 respectively) pins dedicated to input and output. These lines are grouped into three ports, and are configured by software to provide digital/analog I/O timing and status signals.

An on-chip, half-flash 8-bit ±1/2 Least Significant Bit (LSB) A/D converter can multiplex up to eight analog inputs. Unused analog inputs revert to standard digital I/O use. Unique, programmable A_{GND} offset control of the A/D resistor ladder compresses the converter's dynamic range for maximum effective 9-bit A/D resolution.

The Z86C84 has two 8-bit ±1/2 LSB D/A converters. High and low reference voltages provide precise control of the output voltage range. Programmable gain for each D/A converter provides a maximum effective 10-bit resolution for many tasks.

On-chip 8-bit counter/timers with many user-selectable modes simplify real-time tasks, such as counting, timing, and generation of PWM signals.

The designer can prioritize six different maskable, vectored, internal or external interrupts for efficient interrupt handling and multitasking functions.

GENERAL DESCRIPTION (Continued)

By means of an expanded register file, the designer has access to additional control registers for configuring peripheral functions including the A/D and D/A converters, counter/timers, and I/O port functions (Figure 1).

Notes: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{CC}
Ground	GND	V_{SS}

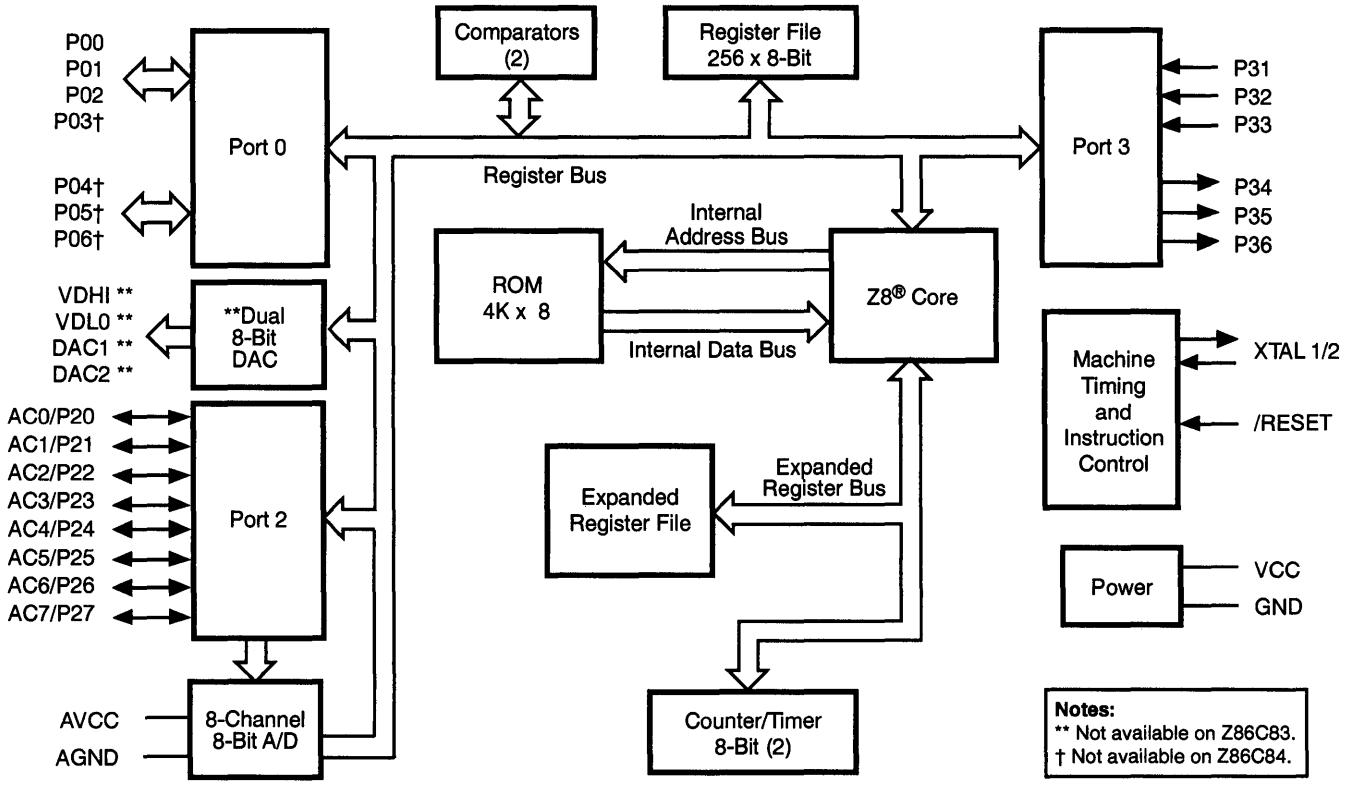


Figure 1. Z86C83/C84 Functional Block Diagram

Z86233/243

CMOS Z8® 8K ROM
CONSUMER CONTROLLER PROCESSOR

FEATURES

Part	ROM Kbytes	RAM bytes	I/O	Package Information
Z86233	8	237	24	28-pinDIP,SOIC,PLCC
Z86243	8	236	32	40-pin DIP, 44-pin PLCC, 44-pin QFP

- 3.0-to 5.5-Volt Operating Range
- Low-Power Consumption: 40 mW (Typical @5.0V)
- 0°C to +70°C Temperature Range (–40°C to +105°C Temperature Range Available)
- Three Expanded Register File Control Registers
- Z86C33/C43 Pin and Package Compatible Version (With Addition of 4K ROM)
- 32 Input/Output Lines (Three with Comparator Inputs) (Z86243 Only)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Comparators
- Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- RAM and ROM Protect
- Clock Free Watch-Dog Timer (WDT) Reset

GENERAL DESCRIPTION

The Z86233/243 Consumer Controller Processor is a member of Zilog's Z8® single-chip microcontroller family featuring enhanced wake-up circuitry, programmable Watch-Dog timers and low-EMI options. The parts provide flexible and efficient growth paths for designers currently using the 4K ROM versions of the consumer controller devices (Z86C30/C40/C33/C43).

Four address spaces, the Program Memory, Register File, Data Memory and Expanded Register File (ERF), support a wide range of memory configurations. Through the ERF, the designer has access to two additional control registers which provide extra peripheral devices, I/O ports, and register addresses.

For applications demanding powerful I/O capabilities, the Z86243 provides 32 pins dedicated to input and output. The Z86233 provides 24 pins dedicated to input and output. These lines are grouped into four ports with eight lines each, and are configurable under software control to provide timing, status signals, or parallel I/O.

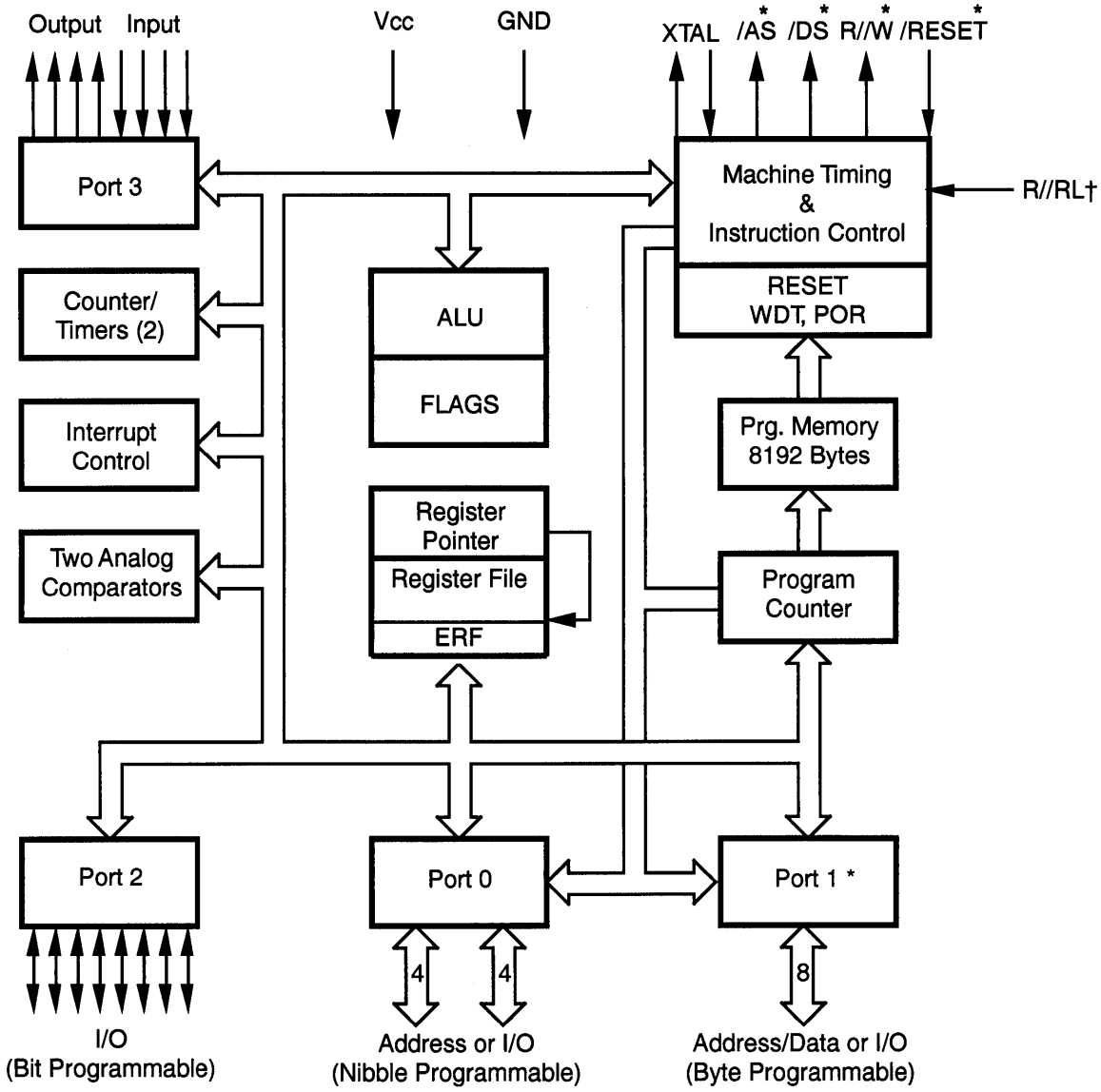
With ROM/ROMless selectivity, the Z86243 provides both external memory and pre-programmed ROM, which enables this Z8 microcontroller to be used in high-volume applications, or where code flexibility is required.

Note: All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



*** Not available on Z86233.**
† Available on Z86243 44-Pin QFP and PLCC versions only.

Functional Block Diagram

Z86E03/E06

CMOS Z8® OTP MICROCONTROLLERS

FEATURES

Part	ROM (Kbytes)	RAM* (Kbytes)	SPI	Speed (MHz)
Z86E03	512	61	No	8
Z86E06	1	125	Yes	12

*General-Purpose

- 18-Pin DIP, WIN, and SOIC Packages
- 4.5- to 5.5-Volt Operating Range
- 0°C to +70°C Temperature Range
- Low-Power Consumption
- Expanded Register File (ERF)
- 14 Input/Output Lines
- Serial Peripheral Interface (SPI) (Z86E06 Only)
- Software Watch-Dog Timer (WDT)
- Power-On Reset (POR)

GENERAL DESCRIPTION

The Z86E03/E06 are One-Time Programmable (OTP) members of the Z8® microcontroller family allowing easy software development, debug, and prototyping for small production runs that are not economically desirable with a masked ROM version.

Three address spaces, the Program Memory, Register File, and Expanded Register File (ERF), support a wide range of memory configurations. Through the ERF, the designer has access to four additional control registers that provide extra peripheral devices, I/O ports, register addresses, an SPI receive buffer and SPI compare register.

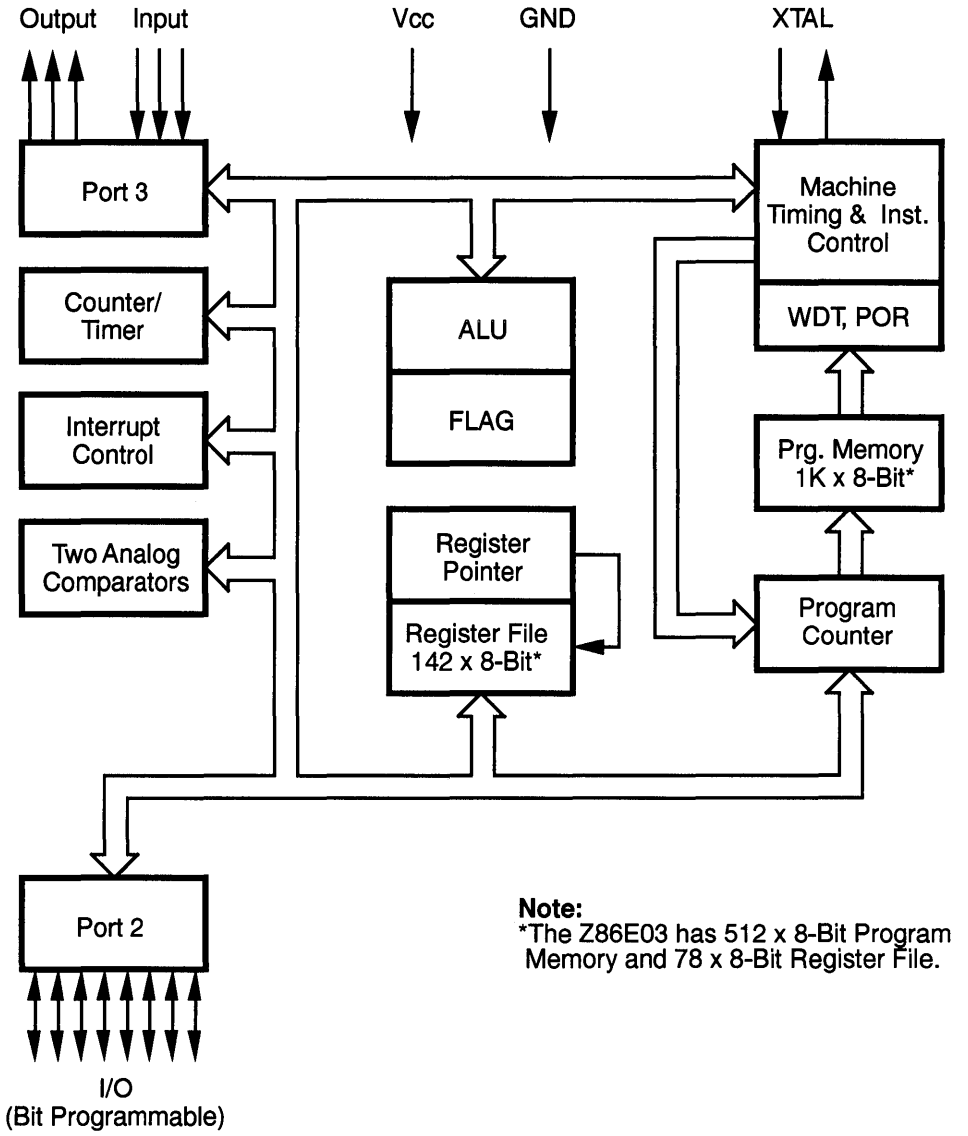
For applications demanding powerful I/O capabilities, the Z86E03/E06's dedicated input and output lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z86E04/E08

CMOS Z8® OTP MICROCONTROLLERS

1

FEATURES

Part Number	ROM (Kilobytes)	RAM* (Bytes)	Speed (MHz)
Z86E04	1	125	12
Z86E08	2	125	12

* General-Purpose

- 18-Pin DIP and SOIC Packages
- 3.0V to 5.5V Operating Range @ 0°C to 70°C
  4.5V to 5.5V Operating Range @ -40°C to 105°C
- 14 Input / Output Lines
- Six Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- WDT/ Power-On Reset (POR)
- On-Chip Oscillator that Accepts XTAL, Ceramic Resonance, LC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50mw)
- Fast Instruction Pointer (1µs @ 12 MHz)

GENERAL DESCRIPTION

Zilog's Z86E04/E08 Microcontrollers (MCU) are One-Time Programmable (OTP) members of the Z8 single-chip microcontroller family which allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E04/E08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

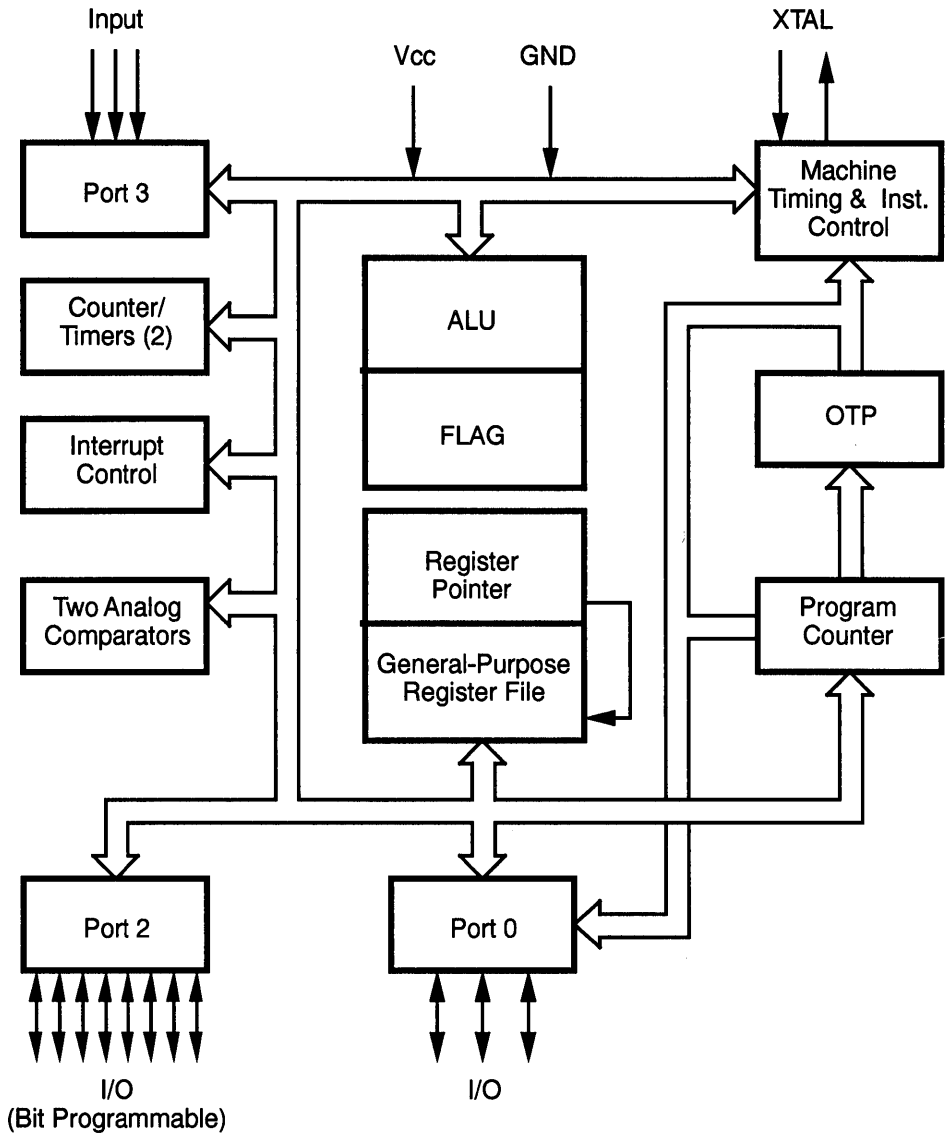


Figure 1. Functional Block Diagram

Z86E21
CMOS Z8® OTP MICROCONTROLLER

GENERAL DESCRIPTION

The Z86E21 microcontroller (MCU) introduces the next level of sophistication to single-chip architecture. The Z86E21 is a member of the Z8 single-chip microcontroller family with 8 Kbytes of EPROM and 236 bytes of general purpose RAM.

The Z86E21 is a pin compatible, One-Time-Programmable (OTP) version of the Z86C21. The Z86E21 contains 8 Kbytes of EPROM memory in place of the 8 Kbyte of ROM on the Z86C21.

The MCU is housed in a 40-pin DIP, 44-pin Leaded Chip-Carrier, or a 44-pin Quad Flat Pack, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin versions only. The MCU can address both external memory and preprogrammed ROM which enables this Z8 microcomputer to be used in high volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E21 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The Z86E21 fulfills this with 32-pin dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory and 236 General-Purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and serial data communication, the Z86E21 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Functional Block Description).

In ROM Protect Mode, the instructions LDC, LDCI, LDE and LDEI are disabled when reading address locations %0000 to %1FFF.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

PRODUCT RECOMMENDATIONS

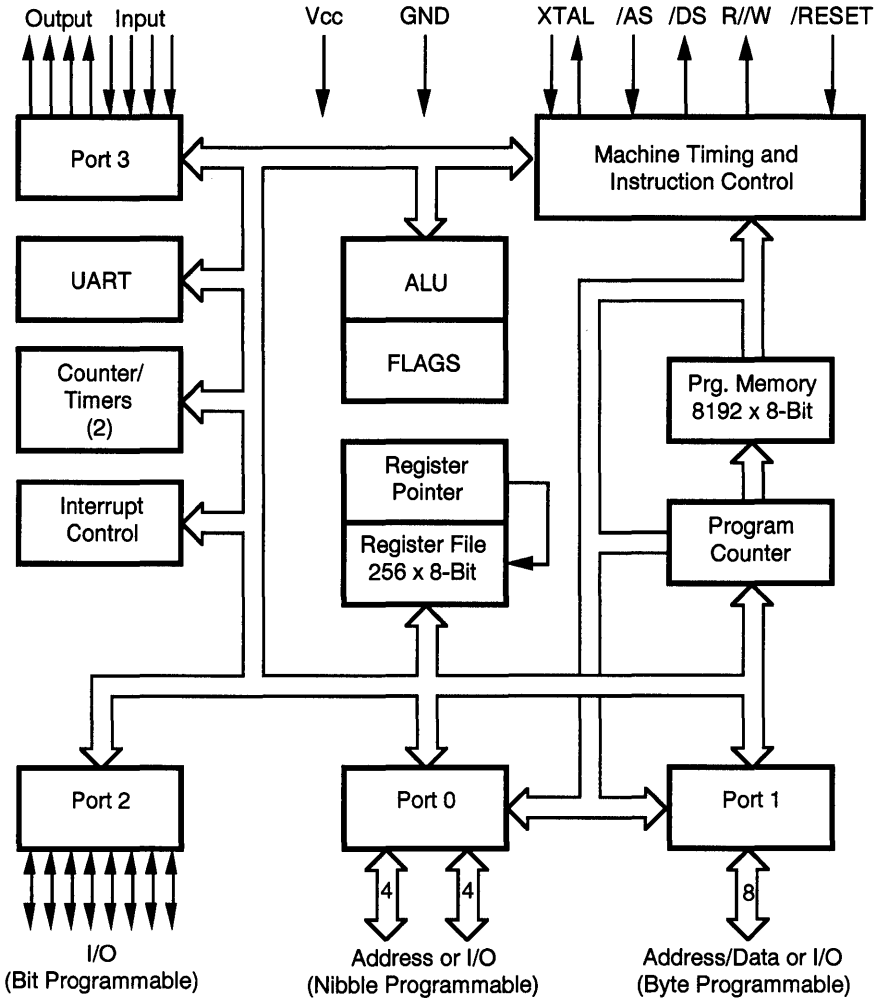
Zilog recommends the following programming equipment for use with this One-Time-Programmable product:

Device	Zilog Support Tool	Recommended Revision Level Hardware	Software
Z86E21	Z86C1200ZEM ICEBOX™ Emulator* (*Does not support 4K/8K option.)	B	1.5
Z86E21	Data I/O 3900 Programmer* (*Does not support option bits.)		1.1
Z86E21	Data I/O Unisite Programmer* (*Does not support option bits.)		3.7

Some non-Zilog programmers may have different programming waveforms, voltages and timings and not all programmers may meet the programming requirements of Zilog's One-Time-Programmable products.

If difficulty is encountered in programming a Zilog OTP product, please contact your local Zilog sales office.

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z86E30/E31/E40 SL1873

PROGRAMMABLE CONSUMER CONTROLLER PROCESSOR

FEATURES

Part Number	ROM (KB)	RAM* (Bytes)	I/O Lines	Speed (Mhz)
Z86E30	4	237	24	16
Z86E31	2	125	24	12
Z86E40	4	236	32	16

*General-Purpose

- 8-Bit CMOS, One-Time Programmable (OTP) Microcontroller
- Standard Temperature (V_{CC} = 3.5V to 5.5V) Extended Temperature (V_{CC} = 4.5V to 5.5V)
- 28-Pin DIP/SOIC/PLCC OTP, 28-Pin DIP Window, 40-Pin DIP OTP/Window, 44-Pin PLCC/QFP OTP, and 44-Pin PLCC Window Packages
- Software Enabled Watch-Dog Timer (WDT)
- Pull-Up Active/Open-Drain Programmable on Port 0, Port 1 and Port 2
- Programmable RC Oscillator, EPROM Protect, and RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: 0.6 µs
- Two Standby Modes: STOP and HALT
- 24/32 Input/Output Lines
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Auto Latches
- Auto Power-On Reset (POR)
- Two Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

GENERAL DESCRIPTION

The Z86E30/E31/E40 One-Time Programmable (OTP) Consumer Controller Processors are members of Zilog's Z8® single-chip microcontroller family featuring enhanced wake-up circuitry, programmable Watch-Dog Timers, Low Noise EMI options, and easy hardware/software system expansion capability.

Four basic address spaces with three Expanded Register Files (ERF) support a wide range of memory configurations. Through the ERF, the deisgner has access to three additional control registers that allow easy access to register mapped peripheral and I/O circuits.

For applications demanding powerful I/O capabilities, the Z86E30/E31 have 24 pins, and the Z86E40 has 32 pins of dedicated input and output. These lines are grouped into four ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake, and address/data bus for interfacing external memory.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

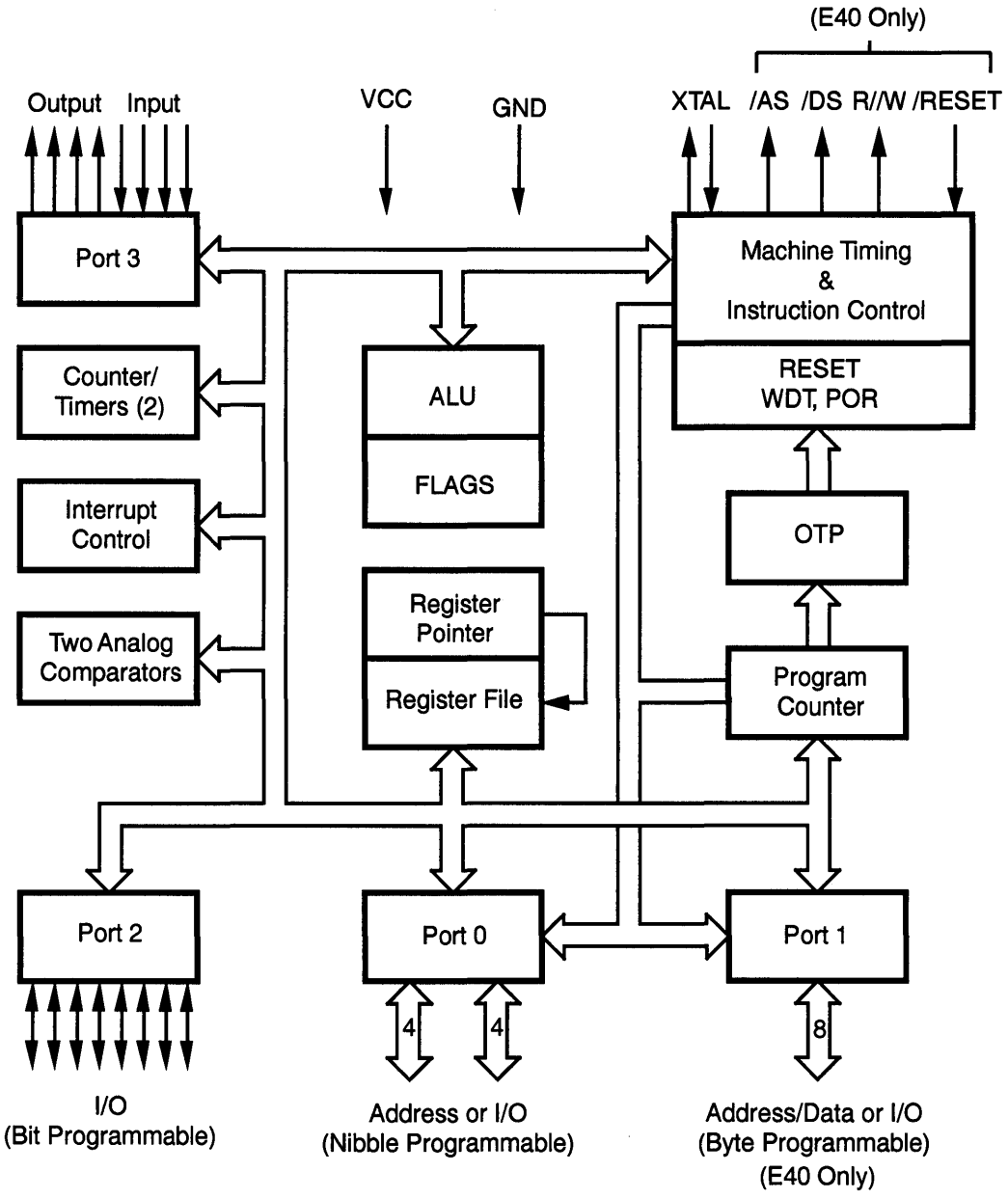


Figure 1. Z86E30/E31/E40 Functional Block Diagram

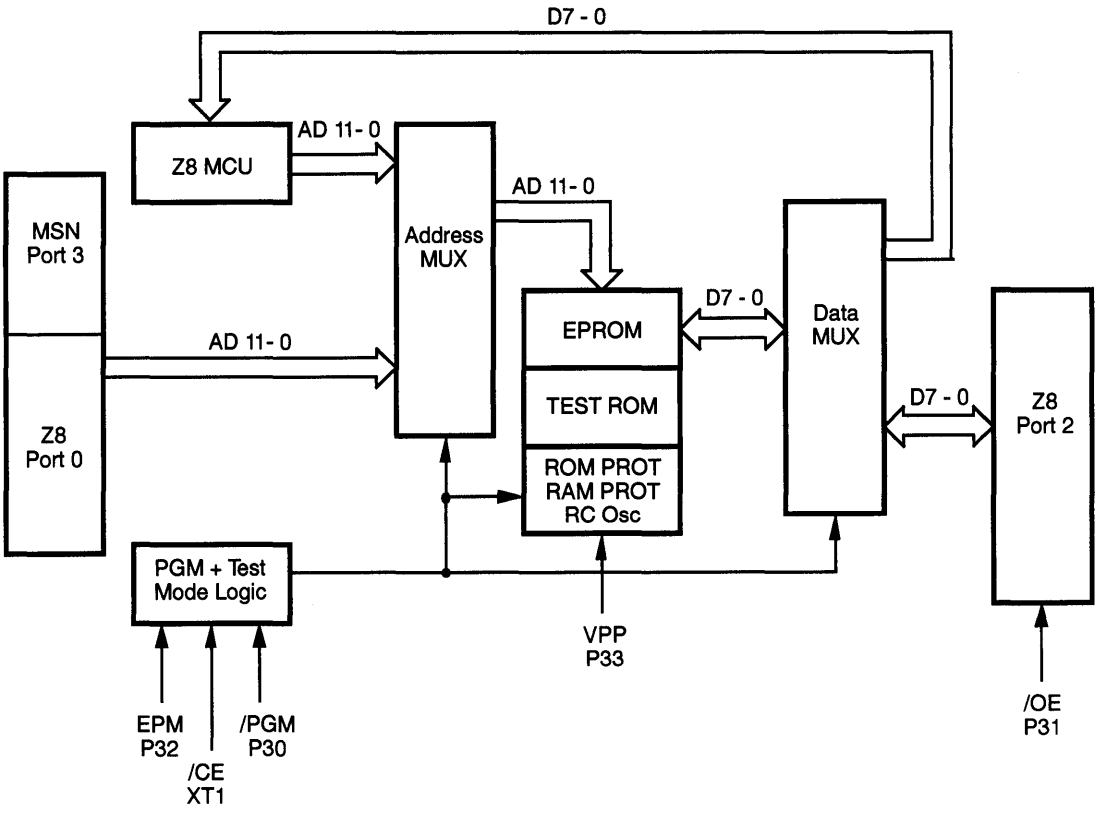


Figure 2. Z86E30/E31/E40 EPROM Programming Block Diagram

Z86E61 AND Z86E63
CMOS Z8® OTP MICROCONTROLLER

GENERAL DESCRIPTION

The Z86E61 is a member of the Z8® single-chip microcontroller family with 16 Kbytes of EPROM and 236 bytes of general-purpose RAM and the Z86E63 has 32K bytes of EPROM.

The Z86E61/63 are pin compatible, One-Time-Programmable (OTP) versions of the Z86C61/63. The Z86E61/63 contain 16/32 Kbytes of EPROM memory in place of the 16/32 Kbytes of ROM on the Z86C61/63.

The MCU is housed in a 40-pin DIP, 44-pin Leaded Chip-Carrier, or a 44-pin Quad Flat Pack, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin versions only. The MCU can address both external memory and preprogrammed ROM which enables this Z8 microcomputer to be used in high volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E61/63 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The Z86E61/63 fulfills this with 32-pin dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory and 236 general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and serial data communication, the Z86E61/63 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Functional Block description).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

PRODUCT RECOMMENDATIONS

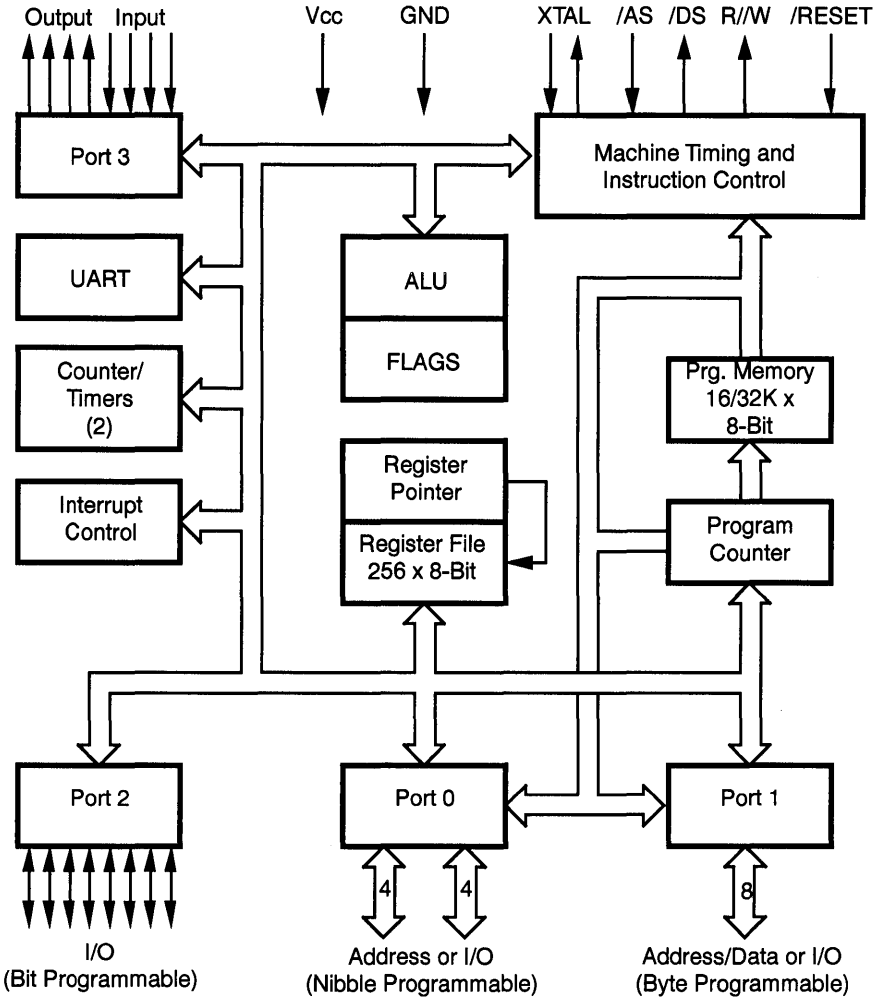
Zilog recommends the following programming equipment for use with this One-Time-Programmable product:

Device	Zilog Support Tool	Recommended Revision Level Hardware	Software
Z86E61/63	Z86C1200ZEM ICEBOX™ Emulator* (*Does not support 4K/8K option.)	B	2.1

Some non-Zilog programmers may have different programming waveforms, voltages and timings and not all programmers may meet the programming requirements of Zilog's One-Time-Programmable products.

If difficulty is encountered in programming a Zilog OTP product, please contact your local Zilog sales office.

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z86E64

CMOS Z8 OTP MICROCONTROLLER

1

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86E64	32	236	52	4.5-5V

Note: *General-Purpose

- Low-Power Consumption: 200 mW (max)
- Fast Instruction Pointer: 0.75 µs @ 16 MHz
- Two Standby Modes: STOP and HALT
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- RAM and ROM Protect
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- Low EMI Mode Option
- 68-Pin Leaded Chip-Carrier

GENERAL DESCRIPTION

The Z86E64 is a member of the Z8 single-chip microcontroller family. The Z86E64 can address both external memory and pre-programmed ROM, which enables this Z8 MCU™ to be used in high-volume applications where code flexibility is required.

The Z86E64 is a pin compatible, One-Time-Programmable (OTP) version of the Z86C64. The Z86E64 contains 32 KB of EPROM memory in place of the 32 KB of ROM on the Z86C64.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory, and 236 general-purpose registers.

The Z86E64 offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications demanding powerful I/O capabilities, the Z86E64's dedicated input and output lines are grouped into six ports. Each port consists of eight lines, except port 6, which has four lines. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

The Z86E64 offers two on-chip counter/timers with a large number of user-selectable modes, and an Universal Asynchronous Receiver/Transmitter (UART). See figure 1 for-Functional Block description.

Note: All Signals with a preceding front slash, "/", are active Low, for example: B//W (WORD is active Low); /B/W (BYTE is active Low, only). Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

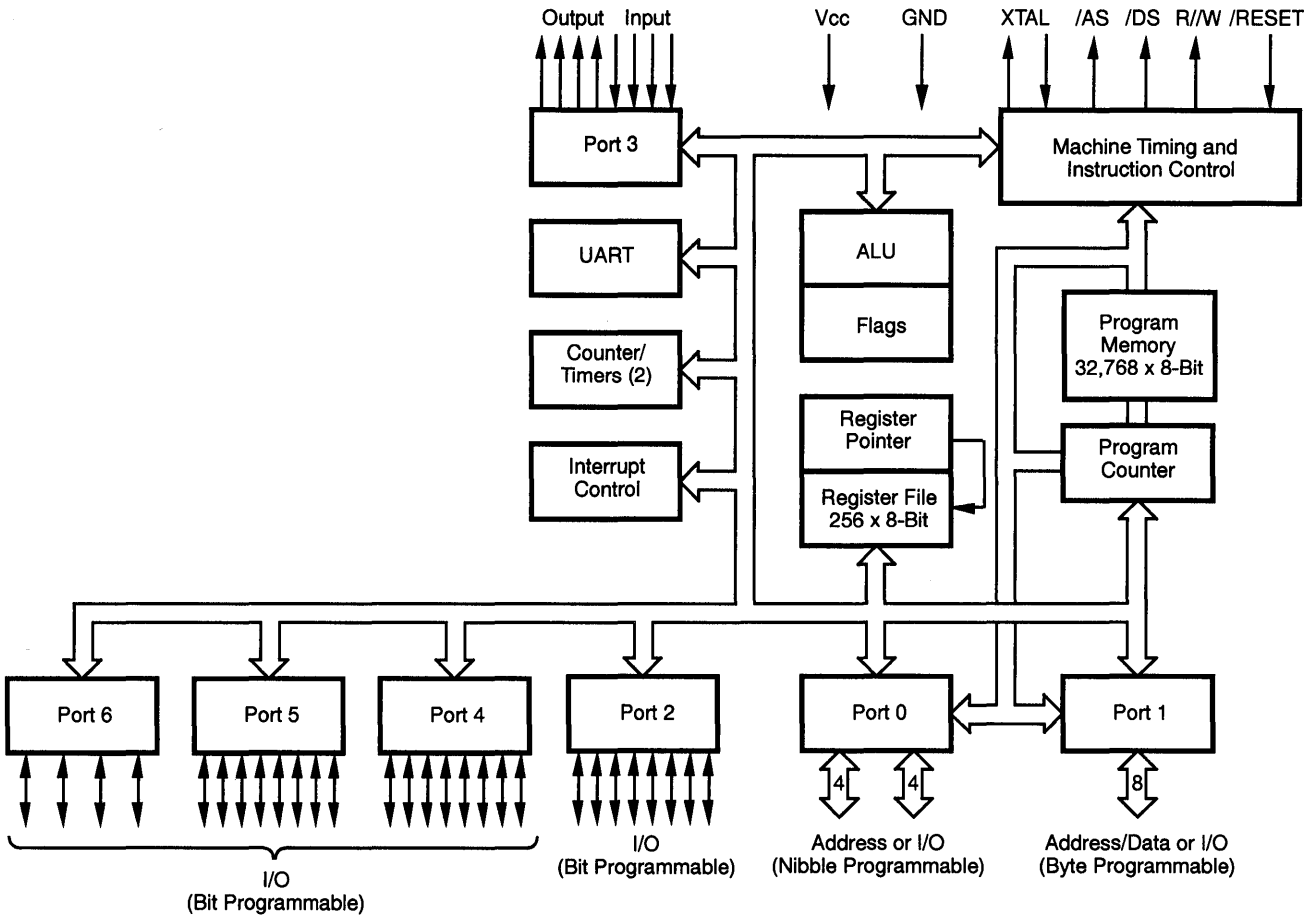


Figure 1. Z86E64 Functional Block Diagram

Z86E66

CMOS Z8® OTP MICROCONTROLLER

FEATURES

Part	ROM Kbytes	RAM Kbytes	I/O	Package Information
Z86E66	16	236	32	44-Pin QFP

- 4.5-to 5.5-Volt Operating Range
- Low-Power Consumption
- 0°C to +70°C Temperature Range
- Three Expanded Register File Control Registers
- 32 Input/Output Lines
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Comparators
- Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86E66 is a member of the Z8® single-chip microcontroller family with 16 Kbytes of EPROM and 236 bytes of general-purpose RAM.

The Z86E66 is pin compatible, One-Time-Programmable (OTP) versions of the Z86C66. The Z86E66 contains 16 Kbytes of EPROM memory in place of the 16 Kbytes of ROM on the Z86C66.

The MCU is housed in a 44-pin Quad Flat Pack, and is manufactured in CMOS technology.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E66 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The Z86E66 fulfills this with 32-pin dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory and 236 general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and serial data communication, the Z86E66 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Functional Block description).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

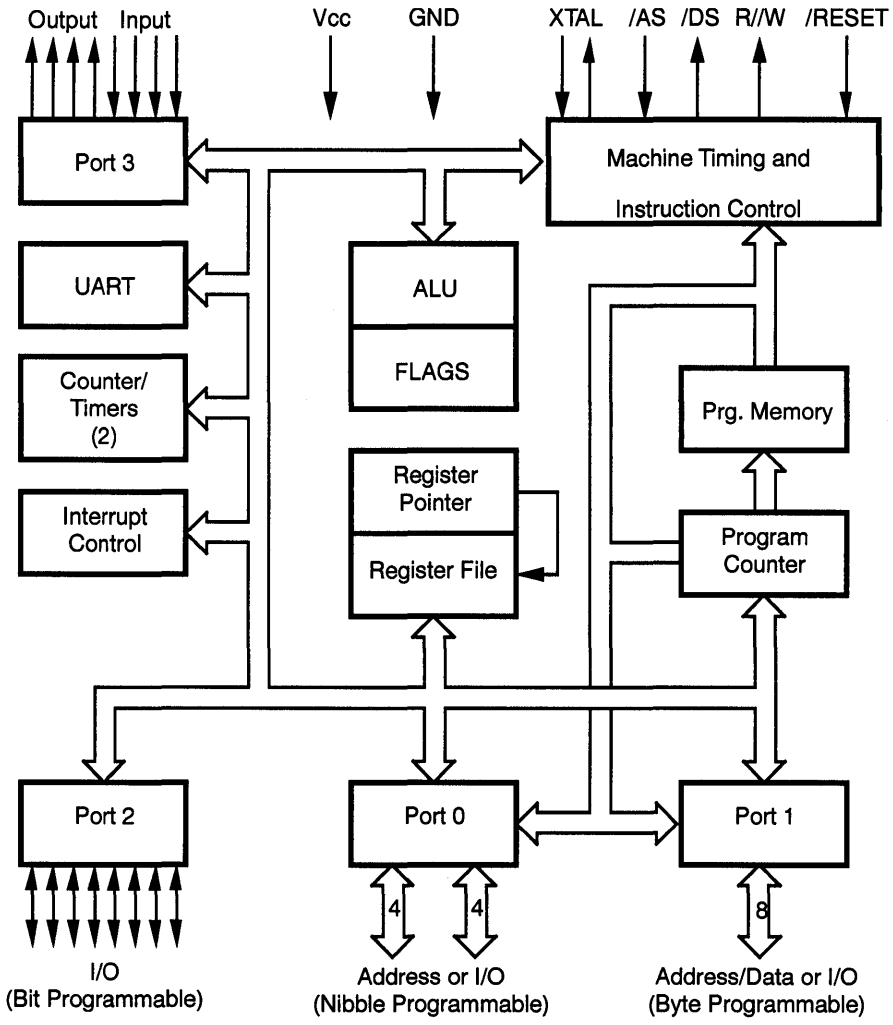
PRODUCT RECOMMENDATIONS

Zilog recommends the following programming equipment for use with this One-Time-Programmable product:

Device	Zilog Support Tool	Recommended Revision Level Hardware	Software
Z86E66	Z86C1200ZEM ICEBOX™ Emulator* (*Does not support 4K/8K option.)	B	2.1

Some non-Zilog programmers may have different programming waveforms, voltages and timings and not all programmers may meet the programming requirements of Zilog's One-Time-Programmable products.

If difficulty is encountered in programming a Zilog OTP product, please contact your local Zilog sales office.



Functional Block Diagram

Z86L03/L06/L16

CONSUMER CONTROLLER PROCESSOR

1

FEATURES

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86L03	0.5	60	14	2.0V to 3.6V
Z86L06	1.0	124	14	2.0V to 3.6V
Z86L16	1.0	124	14	2.0V to 3.6V

Note: *General-Purpose

- Fast Instruction Pointer: 1.5 µs @ 8 MHz
- Expanded Register File Control Registers
- One/Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Watch-Dog/Power-On Reset Timers
- Two Standby Modes: STOP and HALT
- Two Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.
- Software Programmable Low EMI Mode (4 MHz only)
- ROM Protect Option

GENERAL DESCRIPTION

Zilog's Z86L03/L06/L16 CCP™ (Consumer Controller Processors) are members of Zilog's two volt Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 0.5 and 1K bytes of ROM and 60 and 124 bytes of general-purpose RAM, respectively, these 18-pin CMOS CCPs offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with cost-effective and low power consumption.

The Z86L03/L06/L16 architecture is characterized by Zilog's 8-bit microcontroller core with the addition of an Expanded Register File to allow easy access to register mapped peripheral and I/O circuits. The Z86L03/L06/L16 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, and industrial applications.

For applications demanding powerful I/O capabilities, the Z86L03/L06/L16 provides 14 pins dedicated to input and output. These lines are grouped into two ports and are configurable under software control to provide timing, status signals, or parallel I/O (Figure 1).

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File. The register file is composed of 60/124 bytes of general-purpose registers, two I/O port registers, and 13/15 control and status registers. The Expanded Register File consists of three control registers in the Z86L03, and four control registers in the Z86L06/L16.

With powerful peripheral features, such as on-board comparators, counter/timer(s), Watch-Dog Timer (WDT), and software programmable Low EMI Mode, the Z86L03/L06/L16 meets the needs of a variety of sophisticated controller applications.

GENERAL DESCRIPTION (Continued)

Notes: All Signals with a preceding front slash, "/", are active Low, e.g.:B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

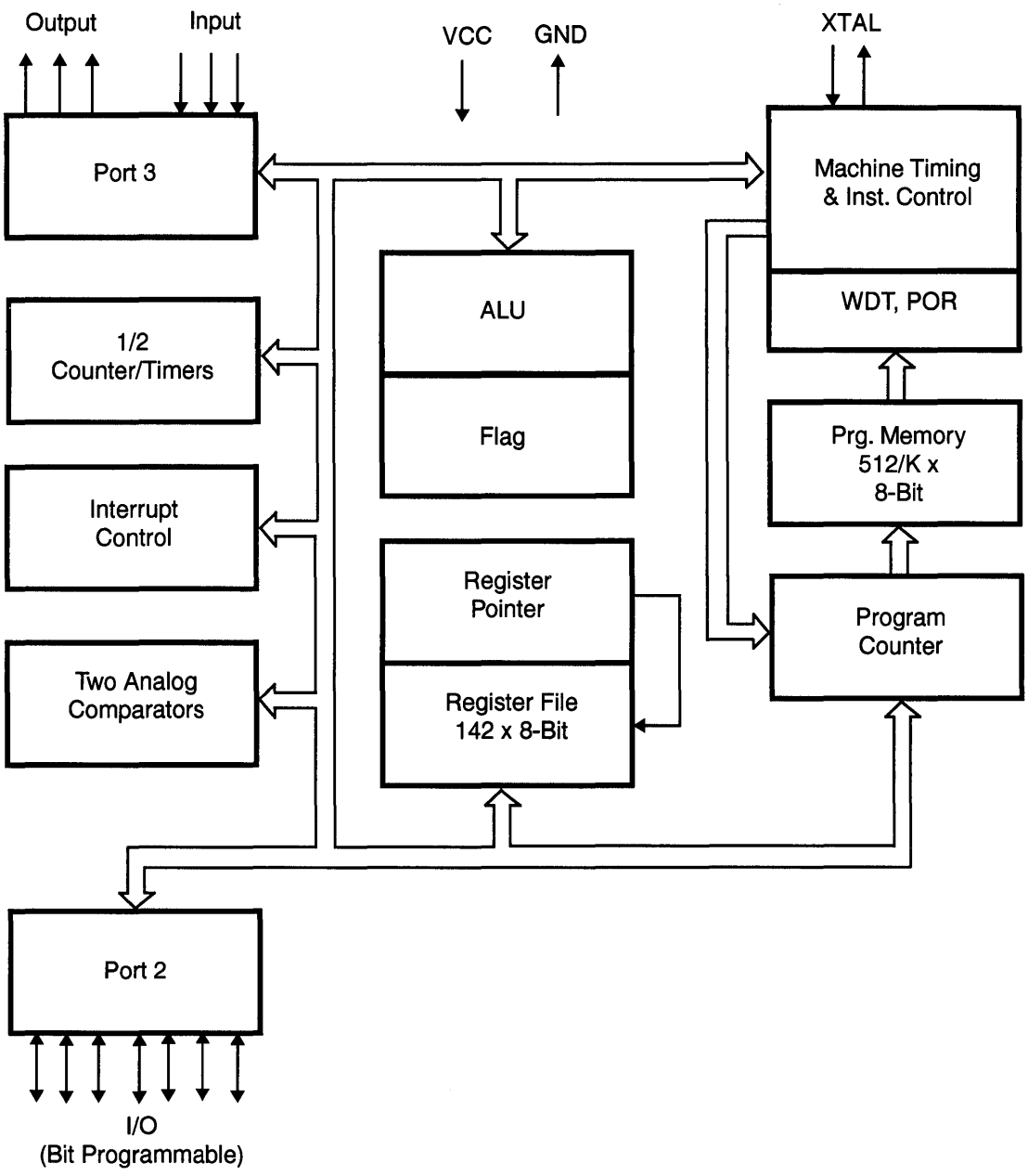


Figure 1. Functional Block Diagram

Z86L04/L08

CMOS Z8® 8-BIT LOW-COST 1K/2K-ROM MICROCONTROLLERS

FEATURES

Part Number	ROM (Kbytes)	RAM* (Bytes)	Speed (MHz)	Auto Latch	Permanent WDT
Z86L04	1	125	8	Optional	Optional
Z86L08	2	125	8	Optional	Optional

* General-Purpose

- 18-Pin DIP and SOIC Packages
- 2.0V to 3.9V Operating Range (0°C–70°C)
- 14 Input / Output Lines
- Six Vectored, Prioritized Interupts from Six Different Sources
- Two On-Board Comparators
- ROM Mask Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Permanent Watch-Dog Timer (WDT)
  - RC Oscillator
  - 32 KHz Operation
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer
- On-Chip Oscillator that Accepts RC, Crystal, Ceramic Resonance, LC, or External Clock Drive
- Clock-Free WDT Reset
- Low-Power Consumption (40mw typical)
- Fast Instruction Pointer (1.5µs @ 8 MHz)
- Fourteen Digital Inputs at CMOS Levels; Schmitt-Triggered
- Software Enabled Watch-Dog Timer
- Programmable Interrupt Polarity
- Two Standby Modes: STOP and HALT
- Low-Voltage Protection

GENERAL DESCRIPTION

Zilog's Z86L04/L08 Microcontrollers (MCU) are members of the Z8® single-chip microcontroller family which offer easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the Z86L04/L08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/ /W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

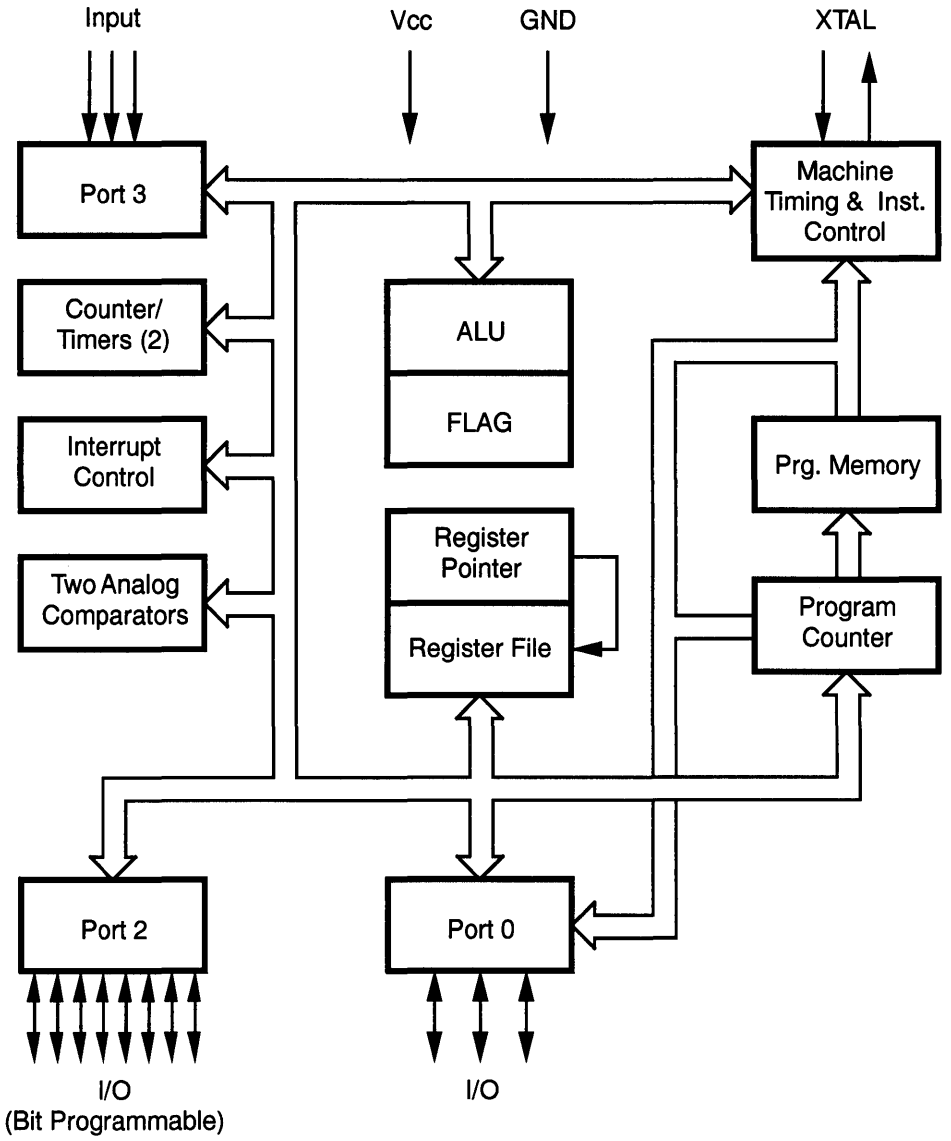


Figure 1. Z86L04/L08
Functional Block Diagram

Z86L33/L43

CMOS Z8®
CONSUMER CONTROLLER PROCESSOR

FEATURES

Part	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z86L33	4	237	8
Z86L43	4	236	8

* General-Purpose

- 40-Pin DIP, 44-Pin PLCC and QFP Packages (L43)
  28-Pin DIP, 28-Pin SOIC (L33)
- 2.0- to 3.9-Volt Operating Range
- Low-Power Consumption
- 0°C to +70°C Operating Range
- Expanded Register File (ERF)
- 32 Input/Output Lines (L43)
  24 Input/Output Lines (L33)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86L33/L43 Consumer Controller Processor (CCP™) is a member of Zilog's Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. This low-power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86L33/L43 features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, External Data Memory (L43), and ERF. The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The ERF consists of three control registers (Banks 0,D, and F)

For applications demanding powerful I/O capabilities, the Z86L33 provides 24 pins, and the Z86L43 provides 32 pins dedicated to input and output. These lines are configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z86L33/L43 offers two on-chip counter/timers with a large number of user-selectable modes.

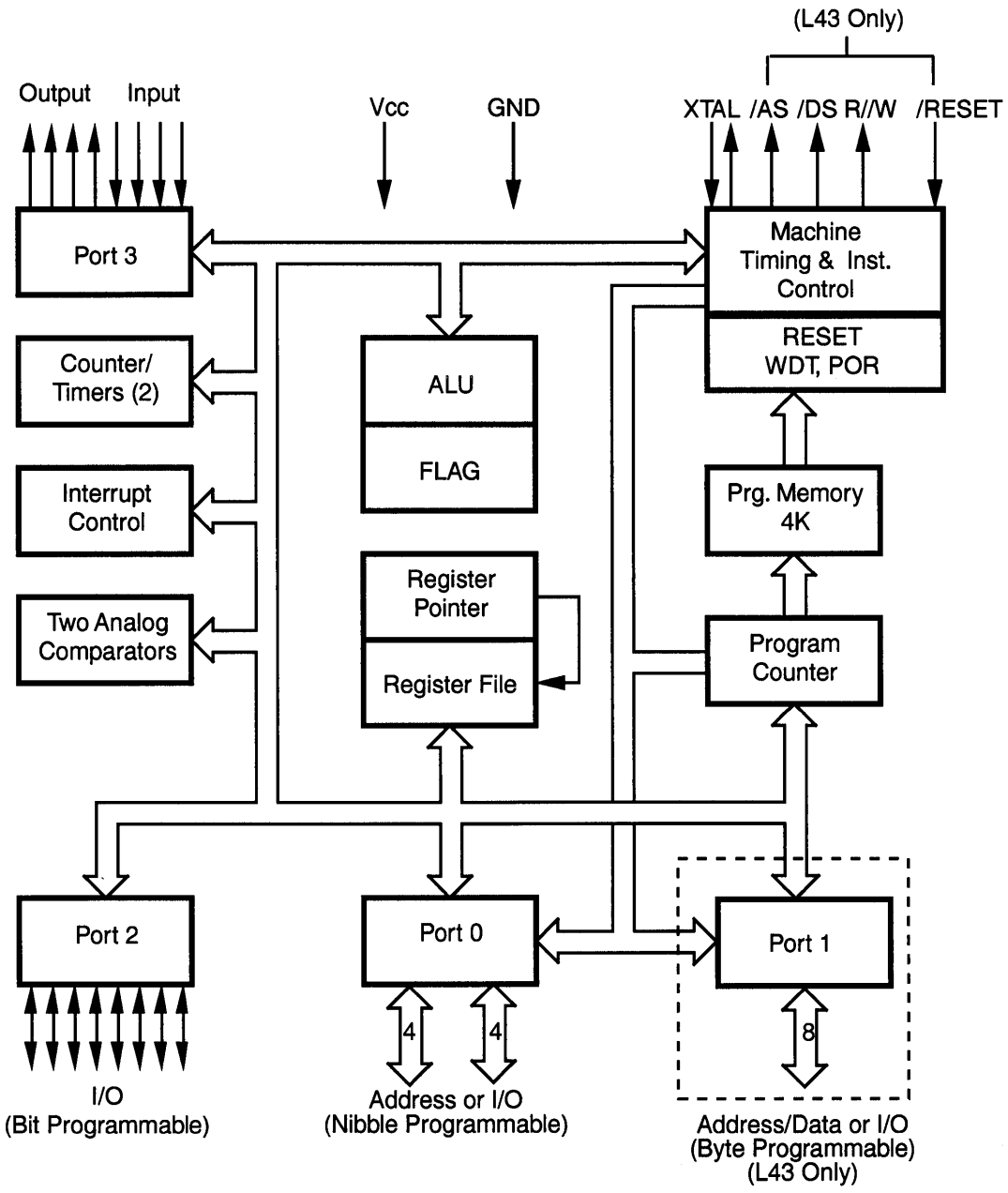
With ROM/ROMless selectivity, the Z86L43 provides both external memory and pre-programmed ROM, which enables this Z8 microcontroller to be used in high-volume applications, or where code flexibility is required.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

ZiLOG

SUPPORT PRODUCT

Z8® MICROCONTROLLER

REAL-TIME S SERIES IN-CIRCUIT EMULATOR

MAIN FEATURES

- Interchangeable µP Pods to Emulate Various Z8 Family Members
- Source Level Debug for C
- Real-Time Transparent Emulation up to 25 MHz
- 33 MHz Available for Z86C93 and Z86C95
- 32K Frames (80 Bits Wide) of Execution Trace Buffer with Time Stamp
- 4K Frames (24 Bits Wide) of DSP Execution Trace Buffer (Z86C95)
- In-Line Symbolic Assembler and Disassembler
- Choose from 64K, 128K, or 256K of Emulation Progam RAM
- 64K of Emulation Data RAM
- Real-Time Hardware Breakpoints
- Complex Events to Trigger Breakpoints or Trace Logic
- Two 16-bit Pass Counters
- Eight Level Hardware Break Sequencer
- Eight Channel User Logic State Analyzer
- External Trigger Inputs and Outputs
- Trace Display During Execution
- Program and Data Memory Display/Edit During Execution
- Windowing or Command-Driven User Interface
- RS-232 Serial Interface to IBM® PC/XT/AT/386/486 and PS-2
- Made in U.S.A.

IBM PC SUPPORT

This unit was designed to work with the IBM® PC/XT/AT/ 386/486 and compatible computers. A special window/ menu user interface provides these unique features:

- Pop-up windows for stack, source, trace buffer, registers, set-up, program and data memory.
- Source window for assembler and HLL debugging
- Full screen edit with mouse support
- User defined windows
- Full Macro Support
- Sixteen user defined set-ups to hold Breakpoint, Trace and Event information for easy recall from disk.
- 115 KBaud serial download
- Monochrome, CGA, EGA, VGA and custom display formats support

COMPLEX EVENTS

An Event is a set of conditions that control the operation of complex program breakpoints and trace start/stop logic in realtime.

There are three Events available, each consisting of the combination of the following:

- Up to 256K address breakpoints or ranges
- 8-bit data pattern with less than, greater than, equal, not equal and don't care combinations.
- RD, WR, INT, instruction fetch, operand read as qualifiers.
- External input with programmable trigger polarity

In addition, Events can be counted/delayed by the use of two 16-bit Pass Counters. An eight level hardware sequencer is available to sequentially trigger to/from any Event or Pass Counter.

BREAKPOINTS

Breakpoints are set to stop program status. Breakpoints can be triggered from a combination of:

- Address or range of address
- Complex Events
- External input
- Pass Counters
- Sequencer
- Trace full condition

TRACE BUFFER

The Trace Buffer is a high speed RAM used to capture, in real time, all activity on the microprocessor's internal bus and pins. A dedicated start/stop logic allows filtering of unwanted information. The Trace Buffer remembers the selected 32K samples (frames) comprised of the following:

- Address Bus
- Data Bus
- Control signals
- I/O pins
- Real-time Clock Stamp
- User logic inputs (8 bits)

The Trace can be started/stopped by the combination of:

- GO command
- Any Event
- Any Pass Counter
- Sequencer
- Trace Full condition

Additionally, the Trace Buffer is equipped with a special internal counter that allows tracing to stop after a specified number of instructions or cycles. This feature allows a trace to catch as much as 32K of small fragments (snapshots) of executed program at full running speed.

The Trace Buffer contents can also be examined during program execution without slowing down the microcontroller.

SUPPORT PRODUCT

Z86C1200ZEM

ICEBOX™ FAMILY Z8® IN-CIRCUIT EMULATOR –C12

HARDWARE FEATURES

- Supported Devices

Package	Emulation	Programming	Notes
18-Pin DIP	Z86C04/07/08/ Z86E04/07/08	Z86E03/06* Z86E04/07/08	[1]*
18-Pin SOIC	N/A	Z86E03/06*	[1]*
		Z86E04/07/08*	[2]*
20-Pin DIP	Z86117/717*	Z86717*	[9, 6]*
20-Pin SOIC	N/A	Z86717*	[8]*
20-Pin SSOP	N/A	Z86717*	[7]*
28-Pin DIP	Z86C20	N/A	
40-Pin DIP	Z86C21/61/63/91	Z86E21/61/63	
	Z86E21/23/61/63	Z86E23*	[3]*
44-Pin PLCC	N/A	Z86E21*	[4]*
44-Pin QFP	N/A	Z86E21*	[5]*

- Real-Time Emulation
- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Z8 GUI Emulator Software
- Windows-Based User Interface
- One-Time Programmable (OTP) Option
- RS-232 Connector
- ICE Pod Connector for Emulation

***Notes:**
[1] With optional, separately purchased adapter, Z86E0601ZDP.
[2] With optional, separately purchased adapter, Z86E0700ZDP.
[3] With optional, separately purchased adapter, Z86E2301ZDP.
[4] With optional, separately purchased adapter, Z86E2101ZDV.
[5] With optional, separately purchased adapter, Z86E2101ZDF.
[6] With optional, separately purchased adapter, Z8671701ZDP.
[7] With optional, separately purchased adapter, Z8671701ZDH.
[8] With optional, separately purchased adapter, Z8671701ZDS.
[9] With optional, separately purchased adapter, Z8671700ZDP.

GENERAL DESCRIPTION

The Z86C1200ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the above listed Z8 microcontroller devices.

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering, program debugging, and OTP programming are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z86C1200ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5.0 VDC, ± 5%
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 16 MHz*
* Shipped with 12 MHz Crystal

Power Requirements

+5.0 VDC @ 0.5A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z86C12 Emulator

- Emulation Base Board includes:
  - CMOS Z86C9320PSC
  - 8K x 8 EPROM (Programmed with Debug Monitor)
  - 32K x 8 Static RAM
  - Three 64K x 4 Static RAM
  - RS-232C Interface
  - Reset Switch

- Z86C12 Emulation Daughterboard
  - 16 MHz CMOS Z86C1216GSE ICE Chip
  - 2K x 8 Static RAM
  - 18/40-Pin DIP Zero Insertion Force (ZIF) Programming Sockets
  - 40/60/80-Pin Target Connectors

Cables/Pods

Power Cable with Banana Plugs
Power Cable with 1A Slow-Blow Fuse
DB25 RS-232C Cable
18-Pin DIP Emulation Pod Cable
28-Pin DIP Emulation Pod Cable
40-Pin DIP Emulation Pod Cable

Devices

One Z86E0812PSC (18-Pin DIP OTP)
One Z86E2112PSC (40-Pin DIP OTP)

Host Software

Z8® GUI Emulator Software
ZASM Cross-Assembler/ MOBJ Object File Utilities

Miscellaneous

20-Pin DIP Jumper Block
Two, Two-Position Shunt Jumpers

Documentation

Emulator User Manual
Z8 Cross-Assembler User's Guide
Universal Object File Utilities (MOBJ)
Registration Card
Product Information

LIMITATIONS

1. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

3. Switching ICEBOXes without quitting the GUI is not supported.

4. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

5. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

```
000C    SRP    #%0
000E    LD     R4, #%0016
0010    LD     R5, @R4
0012    NOP
0013    JP     %000C
0016    NOP
```

   Setting the breakpoint at %0016 and click GO.

   Result: The code will break and stop at %0012.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

6. If the emulator is running a user code at full speed and the port window is opened: Switching to another application or minimizing the GUI (then restoring) will result in the following ICEBOX Communications Error message: "Emulator rejected command: target program is executing." This message may need to be cleared several times (as many as seven) before the GUI returns to normal operation.

   Workaround: Always close the port window before leaving the GUI.

7. Do not put breakpoint at address after Stop instruction. This will cause program counter to continue at that location after a Stop-Mode Recovery.

8. The ICEBOX cannot stop timers during single-step operation, or upon reaching of breakpoint.

PRECAUTION LIST

All Devices

1. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

2. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization must be disabled prior to invoking the VERIFY operation.

3. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

4. For 386 PCs, set the baud rate to 19.2K or less because Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.

5. Do not press hardware reset when the ICEBOX is in OTP programming. If reset is pressed while the GUI is doing OTP programming, close the OTP dialog window and reopen it to reload the information back to the hardware.

   Note: Although the Command Status shows "Processing" after the GUI reestablishes the communication link when Retry was selected, the ICEBOX is actually sitting idle.)

6. All Z8 control registers are write only unless stated otherwise.

7. Programming the ROM protect bit on all Z8s and Z8 OTPs will disable all use of the LDC, LDCI, LDE, and LDEI instructions. Thus, ROM protect does not support the use of a ROM look-up table. The value must be loaded as "immediate values."

8. The special OTP programming options such as ROM protect, RAM protect, Low Noise, and RC will be programmed if the option has been selected and the VERIFY command was then executed.

9. Power Supply ramp-up/rise time must be such that when minimum power-on reset time (T_{POR}) expires, then the V_{CC} must be in the supported specified operating range of the device.

10. The ICEBOX cannot stop Timers and Interrupts at a breakpoint or during ICEBOX Halt operation or a single-step operation. The stack will overflow if an interrupt is enabled and the ICEBOX is in HALT, single-step, or breakpoint. (This is a limitation of the ICE chip.)

PRECAUTION LIST (Continued)

11. Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the ICE chip specifications.

12. The general-purpose registers after Power-On Reset or at initial emulator use will be different than the actual device. The emulator self test will always leave the same values in the general-purpose registers, while the real device will have a random/undefined value in the general-purpose registers.

13. RC oscillator emulation is not supported.

Z86C04/C08/C07

1. To emulate these devices correctly, the user must select either Digital P3 or Analog P3 Emulation Mode in the Configuration Window of the ICEBOX GUI.

2. The register %F8 (PO1M register) bits D4 and D3 must be set to state 0 and bit D2 must be set to state 1.

3. Watch-Dog Timer (WDT) running in Stop Mode is not supported.

4. For Z86C07 emulation, the permanent WDT is not emulated. We recommend that you make the first instruction an enable WDT (5F hex).

5. For Z86C07 emulation, the "No Auto Latch" feature is not implemented.

6. The Z86E07 does not have permanently enabled WDT.

Z86C06

1. When using the C12 Emulator to emulate the C06, the comparator outputs are at P34 and P37, unlike the C06, which are at P34 and P35.

Z86E03/E06

1. The ICEBOX does not support the programming of RC option bits.

Z86E04/E08/E07

1. To emulate these devices correctly, the user must select either Digital P3 or Analog P3 Emulation Mode in the Configuration Window of the ICEBOX GUI.

2. Z86E04 and Z86E08 have special features such that programming the ROM protect mode will also put the device in Low EMI mode, where XTAL frequency = internal SCLK and all output drive capabilities are reduced by 75%.

3. The register %F8 (PO1M register) bits D4 and D3 must be set to state 0 and bit D2 must be set to state 1.

4. Watch-Dog Timer (WDT) running in Stop Mode is not supported.

5. For Z86C07 emulation, the "No Auto Latch" feature is not implemented.

Z86E21

1. The ICEBOX does not support the programming of 8K/4K option bits.

Z86E61/E63

1. The ICEBOX does not support the programming of 32K/16K or 8K/4K option bits.

Z86E08DB 1840

1. The C12 emulator does not support the programming of WDT enable or "kill" EPM option bits.

Z86C1500ZEM

ICEBOX™ FAMILY
Z8® IN-CIRCUIT EMULATOR –C15

HARDWARE FEATURES

- Supported Products

Package	Emulation	Programming
40-Pin DIP	Z86C15	N/A
	Z86K15	N/A

- Real-Time Emulation
- Z8 GUI Emulator Software
- Windows-Based User Interface
- Bit-Programmable I/O Ports for Digital Input/Output Functions
- RS-232 Connector
- ICE Pod Connector for Emulator
- HP-16500 Logic Analysis System Interface Connector

GENERAL DESCRIPTION

The Z86C1500ZEM is a member of Zilog's family of ICEBOX in-circuit emulators providing support for the above listed keyboard microcontrollers.

Zilog's in-circuit emulators are interactive, Windows-based development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering and program debugging are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z86C1500ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5 VDC, ± 5%
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 20 MHz

Power Requirements

+5 VDC @ .75 A Minimum

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z86C15 Emulator

Emulation Base Board

CMOS Z86C9320PSC
8K x 8 EPROM (Programmed with Debug Monitor)
32K x 8 Static RAM
Three 64K x 4 Static RAM
RS-232C Interface
Reset Switch

Z86C15 Emulation Daughterboard

20 MHz CMOS Z86C5020GSE ICE Chip
100-Pin HP-16500A Logic Analysis System Interface Connector
80-Pin Target Connector

Cables/Pods

Power Cable with Banana Plugs
DB25 RS-232C Cable
40-Pin DIP Emulation Cable

Host Software (IBM PC Platform)

Z8 GUI Emulator Software
ZASM Cross-Assembler/MOBJ Object File Utilities

Documentation

C15 Icebox User's Manual
Z8® Cross-Assembler User's Guide
Universal Object File Utilities (MOBJ) User Guide
Registration Card
Product Information

LIMITATIONS

1. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

3. Switching ICEBOXes without quitting the GUI is not supported.

4. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

5. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

```
000C    SRP    #%0
000E    LD     R4, #%0016
0010    LD     R5, @R4
0012    NOP
0013    JP     %000C
0016    NOP
```

   Setting the breakpoint at %0016 and click GO.

   Result: The code will break and stop at %0012.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

6. If the emulator is running a user code at full speed and the port window is opened: Switching to another application or minimizing the GUI (then restoring) will result in the following ICEBOX Communications Error message: "Emulator rejected command: target program is executing." This message may need to be cleared several times (as many as seven) before the GUI returns to normal operation.

   Workaround: Always close the port window before leaving the GUI.

7. Do not put breakpoint at address after Stop instruction. This will cause program counter to continue at that location after a Stop-Mode Recovery.

8. Since the emulator uses the C50 ICE Chip, Port 1 cannot be configured to Low EMI mode. (Bit 4 in PCON register must be set to "1")

   Note: The actual emulated device is unaffected.

PRECAUTION LIST

1. All Z8 control registers are write only unless stated otherwise.

2. Power Supply ramp-up/rise time must be such that when minimum power-on reset time (T_{POR}) expires, then the V_{CC} must be in the supported specified operating range of the device.

3. The bits of non-implemented features (of devices having a PCON register) must be set to "1" state on the emulator.

4. Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the ICE chip specifications.

5. The general-purpose registers after Power-On Reset or at initial emulator use will be different than the actual device. The emulator self test will always leave the same values in the general-purpose registers, while the real device will have a random/undefined value in the general-purpose registers.

6. WDT Register (F) %0F can only be written in the first 64 internal system clocks from the start of program execution.

7. Since the emulator uses the Z86C50 ICE chip and the ICE chip has built-in WDT, the WDT time-out period must be based on the Z86C50. The following table compares the WDT time-out period of the Z86C15 and the Z86C50.

Z86C15 and Z86C50
WDT Time-Out Period Comparison

Internal RC (ms) Time-Out			
D1	D0	Z86C15	Z86C50
0	0	5	4
0	1	15	9
1	0	25	18
1	1	100	75

8. There is no RC oscillator emulation. Use either the XTAL on the emulator or from the target. the internal frequency (SCLK) of the emulator defaults to XTAL2. The emulator has the option of configuring the internal frequency to XTAL1 by writing a "0" to bit 7 of the PCON register, which is located in Bank F Register 0 of the Z86C50. (note: The Z86C15 does not have a PCON register.)

9. There is no WDT hot-bit emulation.

10. Since the Z86C50 ICE chip is used to emulate the Z86C15, the Stop-Mode Recovery source for NAND (P00-03,P31,P33,P24,P25,P26) in the SMR register must be programmed to "100" instead of "111" on the Z86C15 in order to get proper emulation. However, the Stop-Mode Recovery source must be changed back to "111" before submission to ROM code.

    The following is an example of utilizing the conditional assembly to switch the SMR source between emulation or ROM code.

```
nandsmr: .macro flag            ;set up a macro called "nandsmr." Using
                                ;flag to select either emulation mode or
                                ;submission for ROM code.
         .if     flag=1         ;if flag=1, program the SMR source for
                                ;emulation mode.
         ld    r11,#01010000b
         .else
         ld    r11,#01011100b ;if flag=0, program the SMR source for
                                ;Z86C15 ROM code.
         .endif
         .endm

         ld          rp,#0f     ;change register pointer to Bank F
         nandsmr  1             ;program SMR source for emulation mode.
```

11. The GUI comes up as "CCP" in the window caption and uses Z8EM_CCP.BSC as the firmware.

12. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

13. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization must be disabled prior to invoking the VERIFY operation.

PRECAUTION LIST (Continued)

14. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

15. For 386 PCs, set the baud rate to 19.2K or less because Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.

16. Do not press hardware reset when the ICEBOX is in OTP programming. If reset is pressed while the GUI is doing OTP programming, close the OTP dialog window and reopen it to reload the information back to the hardware.

    Note: Although the Command Status shows "Processing" after the GUI reestablishes the communication link when Retry was selected, the ICEBOX is actually sitting idle.)

Z86C2100ZDV

Z86C21 PLCC EMULATION POD

FEATURES

- Supported Devices

Part	Packages	Speed (MHz)
Z86C21/C61/E21	44-Pin PLCC	16

- Cost-Effective Emulator Solution
- Allows Use of Existing Emulator
- Emulation Converter

GENERAL DESCRIPTION

The Z86C21 PLCC Emulation Pod is specifically designed to enable Zilog's C12 ICEBOX™ to emulate the 44-Pin PLCC Z86C21/C61/E21 Z8 Microcontroller.

The kit is a cost-effective cable assembly allowing the use of an existing emulator.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Operating Humidity: 10-90% RH (Non-condensing)

Power Requirements

Not Applicable

Dimensions

Width: 1.30 in.
Length: 2.35 in.

KIT CONTENTS

Hardware

Z86C21 PLCC Emulation Pod Kit Includes:
- Z86C21 PLCC Emulation Pod
- 80-Pin Circuit Header
- 44-Pin PLCC Socket Interface

Documentation

Z86C2100ZDV PLCC Emulation Pod User's Guide

Z86C4000ZDV

Z86C40 PLCC EMULATION POD

FEATURES

- Supported Devices

Part	Packages	Speed (MHz)
Z86C40/C43/E40	44-Pin PLCC	20

- Cost-Effective Emulator Solution
- Allows Use of Existing Emulator
- Emulation Converter

GENERAL DESCRIPTION

The Z86C40 PLCC Emulation Pod is specifically designed to enable Zilog's C50 ICEBOX™ to emulate the 44-Pin PLCC Z86C40/C43/E40 Z8® Microcontroller. The kit is a cost-effective cable assembly allowing the use of an existing emulator.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Operating Humidity: 10-90% RH (Non-condensing)

Power Requirements

Not Applicable

Dimensions

Width: 1.40 in.
Length: 2.35 in.

KIT CONTENTS

Hardware

Z86C40 PLCC Emulation Pod Kit Includes:
- Z86C40 PLCC Emulation Pod
- 80-Pin Circuit Header
- 44-Pin PLCC Socket Interface

Documentation

Z86C4000ZDV PLCC Emulation Pod User's Guide

Z86C5000ZEM

ICEBOX™ Z8® FAMILY IN-CIRCUIT EMULATOR –C50

HARDWARE FEATURES

- Supported Products

Packages	Emulation	Programming	Notes
18-Pin DIP	Z86C03/06/09/ 16/19, Z86E03/06	Z86E04/07/08 Z86E03/06	[1]
20-Pin DIP	N/A	Z86717	[3]
18-Pin SOIC	N/A	Z86E04/07/08 Z86E03/06	[2] [1]
20-Pin SOIC	N/A	Z86717	[4]
20-Pin SSOP	N/A	Z86717	[5]
28-Pin DIP	Z86C30/31/233	Z86E30/31	[6]
40-Pin DIP	Z86C40/90/243	Z86E40	[7]
44-Pin PLCC	N/A	Z86E40	[8]
44-Pin QFP	N/A	Z86E40	[9]

Notes:
[1] E03/06: With optional, separately purchased adapter, Z86E0601ZDP.
[2] With optional, separately purchased adapter, Z86E0700ZDP.
[3] With optional, separately purchased adapter, Z8671701ZDP.
[4] With optional, separately purchased adapter, Z8671701ZDS.
[5] With optional, separately purchased adapter, Z8671701ZDH.
[6] To emulate Z86233, select Z86C30 with 8 KB of ROM.
[7] To emulate Z86243, select Z86C40 with 8 KB of ROM.
[8] With optional, separately purchased adapter, Z86E4001ZDV.
[9] With optional, separately purchased adapter, Z86E4001ZDF.

- Real-Time Emulation
- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Windows-Based User Interface
- Z8 GUI Emulator Software
- Bit-Programmable I/O Ports for Digital Input/Output Functions
- RS-232 Connector
- One-Time Programmable (OTP) Option
- HP-16500 Logic Analysis System Interface Connector

GENERAL DESCRIPTION

The Z86C5000ZEM is a member of Zilog's family of ICEBOX in-circuit emulators providing support for the Consumer Controller Processor (CCP™) microcontrollers.

Zilog's in-circuit emulators are interactive, Windows-based development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering, program debugging, and OTP programming are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z86C5000ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5 VDC, ± 5%
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 20 MHz

Power Requirements

+5 VDC @ 1.0 A Minimum

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z86C50 Emulator

Emulation Base Board:
CMOS Z86C9320PSC
8K x 8 EPROM (Programmed with Debug Monitor)
32K x 8 Static RAM
Three 64K x 4 Static RAM
RS-232C Interface
Reset Switch

Z86C50 Emulation Daughterboard:
20 MHz CMOS Z86C5020GSE ICE Chip
2K x 8 Static RAM
18/28/40-Pin ZIF OTP Sockets
Six HP-16500A Logic Analysis System Interface Connectors
40/60/80-Pin Target Connectors

Cables

Power Cable with Banana Plugs
DB25 RS-232C Cable
40-Pin DIP Emulation Cable
28-Pin DIP Emulation Cable
18-Pin DIP Emulation Cable
Power Cable with 1A Slow-Blow Fuse

Devices

One Z86E3012PSC (28-Pin DIP OTP)
One Z86E4012PSC (40-Pin DIP OTP)

Host Software (IBM PC Platform)

Z8® GUI Emulator Software
ZASM Cross-Assembler / MOBJ Object File Utilities

Miscellaneous

20-Pin Jumper Block
Two, Two Position Shunt Jumpers

Documentation

Emulator User's Manual
Z8 Cross-Assembler User's Guide
Universal Object File Utilities (MOBJ) User's Guide
Registration Card
Product Information

LIMITATIONS

1. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

3. Switching ICEBOXes without quitting the GUI is not supported.

LIMITATIONS (Continued)

4. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

5. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

   ```
   000C    SRP    #%0
   000E    LD     R4, #%0016
   0010    LD     R5, @R4
   0012    NOP
   0013    JP     %000C
   0016    NOP
   ```

   Setting the breakpoint at %0016 and click GO.

   Result: The code will break and stop at %0012.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

6. If the emulator is running a user code at full speed and the port window is opened: Switching to another application or minimizing the GUI (then restoring) will result in the following ICEBOX Communications Error message: "Emulator rejected command: target program is executing." This message may need to be cleared several times (as many as seven) before the GUI returns to normal operation.

   Workaround: Always close the port window before leaving the GUI.

7. Do not put breakpoint at address after Stop instruction. This will cause program counter to continue at that location after a Stop-Mode Recovery.

8. Since the emulator uses the C50 ICE Chip, port 1 cannot be configured to Low EMI mode. (Bit 4 in PCON registers must be set to logic "1").
   Note: This is not a problem with the actual emulated device.

PRECAUTIONS

All Devices

1. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

2. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization must be disabled prior to invoking the VERIFY operation.

3. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

4. For 386 PCs, set the baud rate to 19.2K or less because Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.

5. Do not press hardware reset when the ICEBOX is in OTP programming. If reset is pressed while the GUI is doing OTP programming, close the OTP dialog window and reopen it to reload the information back to the hardware.

   Note: Although the Command Status shows "Processing" after the GUI reestablishes the communication link when Retry was selected, the ICEBOX is actually sitting idle.)

6. All Z8 control registers are write-only unless stated otherwise.

7. Programming the ROM protect bit on all Z8s and Z8 OTPs will disable all use of the LDC, LDCI, LDE, and LDEI instructions. Thus, ROM protect does not support the use of a ROM look-up table. The value must be loaded as "immediate values."

8. The special OTP programming options such as ROM protect, RAM protect, Low Noise, and RC will be programmed if the option has been selected and the VERIFY command was then executed.

PRECAUTIONS (Continued)

9. Power Supply ramp-up/rise time must be such that when minimum power-on reset time (T_{POR}) expires, then the V_{CC} must be in the supported specified operating range of the device.

10. The bits of non-implemented features (of devices having a PCON register) must be set to "1" state on the emulator.

11. Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the ICE chip specifications.

12. The general-purpose registers after Power-On Reset or at initial emulator use will be different than the actual device. The emulator self test will always leave the same values in the general-purpose registers, while the real device will have a random/undefined value in the general-purpose registers.

Z86C03/06/09/16

1. Devices with the comparator output feature have the P32 comparator output coming out of P35.

2. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08/30/31, the register %F8 (PO1M register) bits D4 and D3 must be set to state "0" and bit D2 must be set to state "1."

3. WDT Register (F) %0F should only be written in the first 64 internal system clocks from the start of program execution.

4. The PCON register on Z86C16 is not reset after Stop-Mode Recovery.

5. When using the C50 ICEBOX to emulate the C06, the comparator outputs are at P34 and P37, which is different than the C06, which is at P34 and P35.

Z86E04/E08/E07

1. Z86E04 and Z86E08 have special features such that programming the ROM protect mode will also put the device in Low EMI mode, where XTAL frequency = internal SCLK and all output drive capabilities are reduced by 75 percent.

Z86E04/E08/E07

1. The Z86C30/31/40/50/89/90 and Z86E30/31/40 have the P32 comparator output coming out of P37.

2. Reg (F) %00 PCON has D2 controlling the open-drain for Port 0 and D1 controlling the open-drain for Port 1. This is for the following:
   Z86C30/31/40/50/89/90
   Z86E30/31/40

3. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08/30/31, the register %F8 (PO1M register) bits D4 and D3 must be set to state "0" and bit D2 must be set to state "1."

4. WDT Register (F) %0F should only be written in the first 64 internal system clocks from the start of program execution.

5. For Z86C30/31, the "No Auto Latch" feature is not implemented.

Z86C40/50/89/90 and Z86E40

1. WDT Register (F) %0F should only be written in the first 64 internal system clocks from the start of program execution.

2. The Z86C30/31/40/50/9/90 and Z86E30/31/40 have the P32 comparator output coming out of P37.

3. Reg (F) %00 PCON has D2 controlling the open-drain for Port 0 and D1 controlling the open-drain for Port 1. This is for the following:
   Z86C30/31/40/50/89/90
   Z86E30/31/40

4. For Z86C40, the "No Auto Latch" feature is not implemented.

Z86C6100TSC

Z86C61/63 MCU OTP EMULATION BOARD

DESCRIPTION

The Z86C6100TSC Emulation Board allows the user to plug a programmed EPROM into the board to verify operation of code before submitting for mask ROM.

The Z86C61 Emulation Board provides emulation for Zilog's 40-pin Z86C61/63 16K/32K MCUs.

Supported Devices

Z86C61, Z86C63

Specifications

Emulation Specification
Maximum Emulation Speed: 16.0 MHz

Power Requirements
+5 Vdc @ 100 mA from Target Board

Dimensions

Width:	0.9 in. (2.28 cm)
Length:	2.7 in. (6.86 cm)

Target Clock or Crystal Frequency
1 to 16 MHz

Operating Voltage Range
4.5 V to 5.5 V

Operating Temperature
0 to 70°C

Operating Humidity
10-90% RH (non-condensing)

KIT CONTENTS

Z86C6100TSC Emulation Board
CMOS Z86C12 ICE
28-Pin 16K x 8 or 32K x 8 EPROM Socket
40-Pin Z86C61/63 Socket Plug

Documentation
Z86C6100TSC Emulation Board User Guide

Ordering Information

Part Number: Z86C6100TSC

SUPPORT PRODUCT

Z86C6200ZEM

ICEBOX™ FAMILY Z8® IN-CIRCUIT EMULATOR –C62

HARDWARE FEATURES

- Supported Devices

Package	Emulation	Programming
64-Pin DIP	Z86C62/C64	N/A
68-Pin PLCC	Z86C62/C64	N/A

- Real-Time Emulation
- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Z8 GUI Emulator Software
- Windows-Based User Interface
- RS-232 Connector
- ICE Pod Connector for Emulation
- HP-16510 Logic Analysis System Interface Connector

GENERAL DESCRIPTION

The Z86C6200ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the above listed Z8 microcontroller devices.

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering,and program debugging, are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z86C6200ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5.0 VDC, ± 5%
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 16 MHz*
*Shipped with 12 MHz Crystal

Power Requirements

+5.0 VDC @ 0.5A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z86C62 Emulator

- Emulation Base Board includes:
  - CMOS Z86C9320PSC
  - 8K x 8 EPROM (Programmed with Debug Monitor)
  - 32K x 8 Static RAM
  - Three 64K x 4 Static RAM
  - RS-232C Interface
  - Reset Switch
- Z86C62 Emulation Daughterboard Includes:
  - 20 MHz CMOS Z86C9620VSC Chip
  - 60/80-Pin Target Connectors
  - Five HP-16510 Logic Analysis System Interface Connector

Cables/Pods

Power Cable with Banana Plugs
Power Cable with 1A Slow-Blow Fuse
DB25 RS-232C Cable
64-Pin DIP Emulation Pod Cable
68-Pin PLCC Emulation Pod Cable

Host Software

Z8® GUI Emulator Software
ZASM Cross-Assembler / MOBJ Object File Utilities

Documentation

Emulator User Manual
Z8 Cross-Assembler User's Guide
Universal Object File Utilities (MOBJ)
Registration Card
Product Information

LIMITATIONS

1. Breakpointing in interrupt service routine and single-stepping pass the IRET statement will cause global interrupts to be disabled.

2. Do not put breakpoint at address after Stop instruction. This will cause program counter to continue at that location after a Stop-Mode Recovery.

4. The ICEBOX cannot stop timers during single-step operation, or upon reaching of breakpoint.

5. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

6. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

7. Switching ICEBOXes without quitting the GUI is not supported.

8. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

9. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

   ```
   000C    SRP    #%0
   000E    LD     R4, #%0016
   0010    LD     R5, @R4
   0012    NOP
   0013    JP     %000C
   0016    NOP
   ```

   Setting the breakpoint at %0016 and click GO.

   Result: The code will break and stop at %0012.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

10. If the emulator is running a user code at full speed and the port window is opened: Switching to another application or minimizing the GUI (then restoring) will result in the following ICEBOX Communications Error message: "Emulator rejected command: target program is executing." This message may need to be cleared several times (as many as seven) before the GUI returns to normal operation.

    Workaround: Always close the port window before leaving the GUI.

PRECAUTION LIST

All Devices

1. All Z8 control registers are write only unless stated otherwise.

2. Power Supply ramp-up/rise time must be such that when minimum power-on reset time (T_{POR}) expires, then the V_{CC} must be in the supported specified operating range of the device.

3. The ICEBOX cannot stop Timers and Interrupts at a breakpoint or during ICEBOX Halt operation or a single-step operation. The stack will overflow if an interrupt is enabled and the ICEBOX is in HALT, single-step, or breakpoint. (This is a limitation of the ICE chip.)

4. Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the ICE chip specifications.

5. The general-purpose registers after Power-On Reset or at initial emulator use will be different than the actual device. The emulator self test will always leave the same values in the general-purpose registers, while the real device will have a random/undefined value in the general-purpose registers.

6. RC oscillator emulation is not supported.

7. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

8. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization must be disabled prior to invoking the VERIFY operation.

9. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

10. For 386 PCs, set the baud rate to 19.2K or less because Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.

11. Do not press hardware reset when the ICEBOX is in OTP programming. If reset is pressed while the GUI is doing OTP programming, close the OTP dialog window and reopen it to reload the information back to the hardware.

    Note: Although the Command Status shows "Processing" after the GUI reestablishes the communication link when Retry was selected, the ICEBOX is actually sitting idle.)

SUPPORT PRODUCT

Z86C8400ZEM

ICEBOX™ FAMILY Z8® IN-CIRCUIT EMULATOR –C84

HARDWARE FEATURES

- Supported Devices

Package	Emulation	Programming	Notes
28-Pin DIP	Z86C83/84	N/A	
28-Pin PLCC	Z86C83/84	N/A	
28-Pin SOIC	Z86C83/84*	N/A	[1]*

- Real-Time Emulation
- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Z8 GUI Emulator Software
- Windows-Based User Interface
- RS-232C Connector
- ICE Pod Connector for Emulation
- Selectable Baud Rate: 9600 – 57600

***Notes:**
[1] With optional, separately purchased adapter available from:

Emulation Technology, Inc.
Telephone (408) 982-0660
FAX (408) 982-0664
Part # AS-DIP.6-028-S003-1

GENERAL DESCRIPTION

The Z86C8400ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the above listed Z8 microcontroller devices.

Zilog's in-circuit emulators are interactive, Windows-based development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering and program debugging are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z86C8400ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5.0 VDC, ± 5%
Minimum Emulation Speed: 200 KHz
Maximum Emulation Speed: 16 MHz

Power Requirements

+5.0 VDC @ 1.0A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z86C84 Emulator

- Emulation Base Board includes:
  - CMOS Z86C9320PSC
  - 8K x 8 EPROM (Programmed with Debug Monitor)
  - 32K x 8 Static RAM
  - Three 64K x 4 Static RAM
  - RS-232C Interface
  - Reset Switch

- Z86C84 Emulation Daughterboard
  - 20 MHz CMOS Z86C5020GSE ICE Chip
  - Two 32 MHz CMOS Z86C9520VSC
  - 28-Pin DIP Zero Insertion Force (ZIF) Programming Socket
  - 60-Pin Target Connector
  - Two 8-Channel A/D
  - Two 8K x 8 EPROM
  - 100-Pin HP-16500 Logic Analyzer Interface Connector

Cables/Pods

Power Cable with Banana Plugs
DB25 RS-232C Cable
28-Pin DIP Emulation Pod Cable
28-Pin PLCC Emulation Pod Cable

Host Software

Z8® GUI Emulator Software
ZASM Cross-Assembler /MOBJ Object File Utilities

Documentation

Z86C84 ICEBOX User's Manual
Z8 Cross-Assembler User's Guide
Universal Object File Utilities (MOBJ)
Registration Card
Product Information

PRECAUTIONS

1. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point.

2. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization should be disabled prior to invoking the VERIFY operation.

3. The status color bar in the OTP dialog box will be cleared in the area where a new window opens on top of it.

4. For some 386 PCs, the user is cautioned to set the baud rate to 19.2K or less because the Windows' communication driver does not guarantee "reliable" operation above 9600 baud. It is possible that on some slower 386 machines, selecting a high baud rate would crash the Windows' environment or result in excessive communication errors.

5. Do not press hardware reset when the ICEBOX is in the OTP dialog for programming. If reset is pressed while the GUI is doing OTP programming, the user would need to close the OTP dialog box and reopen it to reload the information back to the hardware. (**Note:** Although the Command Status indicates "Processing" after the GUI reestablishes the communication link when Retry was selected, the ICEBOX is really sitting idle.)

6. The emulator cannot be operated while performing ESD/EMI testing on the target board.

7. The PCON Register reserved bits for the C84 Emulator must be set to 1.

8. All Z8 control registers are write-only unless stated otherwise.

9. Power Supply ramp-up/rise time must be such that when minimum power-on reset time (T_{POR}) expires, then the V_{CC} must be in the supported specified operating range of the device.

10. Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the ICE chip specifications.

11. The general-purpose registers after Power-On Reset or at initial emulator use will be different than the actual device. The emulator self test will always leave the same values in the general-purpose registers, while the real device will have a random/undefined value in the general-purpose registers.

12. When using the Analog-to-Digital (A/D) Converter, the conversion data is dependent upon the V_{CC} voltage input to the A/D chip of the emulator. For improved accuracy, measure the actual V_{CC} voltage to the A/D chip of the emulator before performing any A/D operation. (Refer to the C84 ICEBOX User's Manual, Chapter 2 "A/D Measurement" section for more information.)

LIMITATIONS

1. Typing into the File Name box in order to change the drive in the file download and load symbol dialog boxes is not anticipated by the GUI. Instead, use the mouse in the Directories box as the workaround.

2. Switching ICEBOXes without quitting the GUI is not supported and may cause unexpected results.

3. The maximum loadable symbols is 32,768 provided there is enough system resource (memory).

4. The keyboard and mouse will lock up if the screen saver supplied by Windows 3.1 times out while the GUI software is waiting for the user to complete entering a line of assembly code in the Debug window. To recover, the user must reset the computer. The "Totally Twisted After Dark Screen Saver" version 3.2 and the Windows 95 screen saver both work fine. The workaround is to either turn off the screen saver, set the screen saver to much longer time out value, finish the line of code before the time-out occurs (press ENTER), or use a different screen saver such as "After Dark". This problem may also exist at other points in the GUI that request input from the user.

5. Although GUI 3.00 and later support baud rates up to 57.6K, the actual maximum usable rate may be less due to limitations of the user is hardware and or system software setup. The maximum usable rate is determined by the user is tolerance of the frequency of communication errors.

6. Although the ICEBOX has auto latches, Auto Latch Mask Option for P00, P01, and P02 is not supported.

7. The ICEBOX does not support software-programmable pull-up resistors. The pull-up resistors are emulated by jumper switches. (Refer to the C84 ICEBOX User's Manual, Chapter 2, Table 2-2.)

8. The initial blue Zilog screen can be distorted by other active windows. This only affects the appearance, not the functionality, of the GUI.

9. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

```
000C    SRP    #%0
000E    LD     R4, #%0016
0010    LD     R5, @R4
0012    NOP
0013    JP     %000C
0016    NOP
```

   Setting the breakpoint at %0016 and click GO.

   Result: The code will break and stop at %0012.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

10. If the emulator is running a user code at full speed and the port window is opened: Switching to another application or minimizing the GUI (then restoring) will result in the following ICEBOX Communications Error message: "Emulator rejected command: target program is executing." This message may need to be cleared several times (as many as seven) before the GUI returns to normal operation.

    Workaround: Always close the port window before leaving the GUI.

LIMITATIONS (Continued)

11. Do not put breakpoint at address after Stop instruction. This will cause program counter to continue at that location after a Stop-Mode Recovery.

12. Since the emulator uses the C50 ICE Chip, port 1 cannot be configured to Low EMI mode. (Bit 4 in PCON registers must be set to logic "1").

    Note: This is not a problem with the actual emulated device.

13. Clicking on the HALT button does not always halt the ICEBOX execution. If the application goes into Stop Mode or Halt Mode, the only way to halt the emulator execution is by doing a Stop-Mode or Halt-Mode Recovery (as defined by the user program). You may also reset the application using the RESET button; however, this will reset the whole ICEBOX.

14. Single-stepping into the Halt instruction will cause an ICEBOX "Fatal Error" message to be displayed on the screen. The Ice Chip must be reset, either by /Reset Pin on the target board or by resetting the whole ICEBOX by pressing the RESET button at back of the emulator.

15. Breakpointing in interrupt service routing and single-stepping pass the IRET statement will cause global interrupts to be disabled.

16. The ICEBOX does not support any OTP programming.

17. RC oscillator emulation is not supported.

Z86CCP00ZAC

Z8® CCP™ EMULATOR ACCESSORY KIT

DESCRIPTION

The Z86CCP00ZAC is the accessory kit for the Z86CCP00ZEM. The kit contains all accessories to fully populate and operate all functions of the Z86CCP00ZEM.

KIT CONTENTS

Z8 CCP Emulator Accessory Kit

- 28-Pin ZIF Socket
- 28-Pin Target Connector Cable
- 40-Pin ZIF Socket
- 40-Pin Target Connector Cable
- RS-232 Cable
- Power Cable

Z86CCP00ZEM
IN-CIRCUIT EMULATOR

HARDWARE FEATURES

- Supported Products

Packages	Emulation	Programming	Notes
18-pin DIP	Z86C03/04/06/07 /08/09/16/19 Z86E03/04/06/07/08	Z86E04/07/08 Z86E03/06	1
20-pin DIP	N/A	Z86717	2
18-pin SOIC	N/A	Z86E04/07/08 Z86E03/06	3
20-pin SOIC	N/A	Z86717	4
20-pin SSOP	N/A	Z86717	5
28-pin DIP	Z86C03/31/32/233	Z86E30/31	6,7
28-pin SOIC	N/A	N/A	
40-pin DIP	Z86C40/243	Z86E40	7,8
44-pin PLCC	N/A	N/A	
44-pin QFP	N/A	N/A	

Notes:

1. E03/06; With optional, separately purchased adapter, Z86E0601ZDP.
2. With optional, separately purchased adapter, Z86E0700ZDP.
3. With optional, separately purchased adapter, Z8671701ZDp.
4. With optional, separately purchased adapter, Z8671701ZDS.
5. With optional, separately purchased adapter, Z8671701ZDH.
6. To emulate Z86233, select Z86C30 with 8 KB or ROM.
7. E30/31/140: With opt., separately purchased acc. kit Z86CCP00ZAC
8. To emulate Z86243, select Z86C40 with 8 KB or ROM.

- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Z8 GUI Emulator Software
- Bit-Programmable I/O Ports for Digital Input/Output Functions
- RS-232 Connector
- One-Time Programmable

GENERAL DESCRIPTION

The Z86CCP00ZEM is a member of Zilog's family of in-circuit emulators providing support for the Consumer Controller Processor (CCP™) microcontrollers.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering, program debugging, and OTP programming are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z86CCP00ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C ±10°C
Supply Voltage +7.5 VDC to +9.0 VDC
(+8.0 VDC Typical)
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 8 MHz

Power Requirements

+8.0 VDC @ 0.5A Minimum

Dimensions

Width: 7.0 in. (17.7 cm)
Length: 9.0 in (22.9 cm)
Height: 0.9 in. (2.3 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB or RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z8® CCP™ Emulator

CMOS Z86C9320VSC
20 MHz CMOS Z86C5020FSE ICE Chip
8K x 8 Static RAM (For Code Memory)
18-pin DIP Zero Insertion Force (ZIF)
Programming Socket
Sockets Available for 18/28/40-Pin Target Cables
Holes Available for 28/40-Pin ZIF Sockets
RS-232C Interface
Reset Switch

Cables

18-Pin DIP Target Cable

Devices

One Z86E0812PSC (18-Pin DIP)

Software (IBM PC Platform)

Z8 GUI Emulator Software
ZASM Cross-Assembler/MOBJ Object File Utilities
Production Languages Corporation COMPASS/Z8
(Evaluation Version)

Documentation

Emulator User Manual
Discrete Z8 Databook
Z8 Microcontroller Technical Manual
Registration Card
Product Information

Z8 CCP Emulator Accessory Kit (Z86CCP00ZAC)

(Not included with Z86CCP00ZEM)

28-Pin ZIF Socket

28-Pin DIP Target Cable

40-Pin ZIF Socket

40-Pin DIP Target Cable

DB25 RS-232C Cable

Power Cable with Banana Plugs

LIMITATIONS

1. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionary, of the GUI.

3. Switching ICEBOXes without quitting the GUI is not supported.

4. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

5. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

Example:

```
000C    SRP     #%0
00OE    LD      R4, #%0016
0010    LD      R5, @R4
0012    NOP
0013    JP      %000C
0016    NOP
```

Setting the breakpoint at %0016 and click GO.

Result: The code will break and stop at %0012.

Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

6. If the emulator is running a user code at full speed and the port window is opened: Switching to another application or minimizing the GUI (then restoring) will result in the following ICEBOX Communications Error message: "Emulator rejected command: target program is executing.: This message may need to be cleared several times (as many as seven) before the GUI returns to normal operation.

Workaround: Always close the port window before leaving the GUI.

7. Do not put breakpoint at address after Stop instruction. This will cause program counter to continue at that location after a Stop-Mode Recovery.

8. Since the emulator uses the C50 ICE Chip, port 1 cannot be configured to Low EMI mode. (Bit 4 in PCON registers must be set to logo "1").

Note: This is not a problem with the actual emulated device.

PRECAUTIONS

All Devices

1. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

2. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization must be disabled prior to invoking the VERIFY operation.

3. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

4. For 386 PCs, set the baud rate to 19.2K or less because Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.

5. Do not press hardware reset when ICEBOX is in OTP programming. If reset is pressed while the GUI is doing OTP programming, close the OTP dialog window and reopen it to reload the information back to the hardware.

Note: Although the Command Status shows "Processing" after the GUI reestablishes the communication link when Retry was selected, the ICEBOX is actually sitting idle.)

6. All Z8® control registers are Write-Only unless stated otherwise.

7. Programming the ROM protect bit on all Z8s and Z8 OTPs will disable all use of the LDC, LDCI, LDE, and LDEI instructions. Thus, ROM protect does not support the use of a ROM look-up table. The value must be loaded as "immediate values."

8. The special OTP programming options such as ROM protect, RAM protect, Low Noise, and RC will be programmed if the option has been selected and the VERIFY command was then executed.

9. Power Supply ramp-up/rise time must be such that when minimum power-on reset time (T_{POR}) expires, then the V_{CC} must be in the supported specified operating range of the device.

10. The bits of non-implementing features (of devices having a PCON register) must be set to '1' state on the emulator.

11. The jumpers for implementing IRQ3 rising edge interrupt on P32 for Z86C04/C07/C08/Eo4/E08 must be removed when emulating other devices.

12 Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the ICE chip specifications.

13 The general-purpose registers after Power-On Reset or at initial emulator use will be different than the actual device. The emulator self test will always leave the same values in the general-purpose registers, while the real device will have a random/undefined value in the general-purpose registers.

14. RC oscillator emulation is not supported.

Z86C03/06/09/16

1. Devices with the comparator output feature have the P32 comparator output coming out of P335.

2. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08/30/31, the register %F8 (P01M register) bits D4 and D3 must be set to state 0 and bit D2 must be set to state 1.

3. WDT Register (F) %0F can only be written in the first 64 internal system clocks from the start of program execution.

4. The PCON register on Z86C16 is not reset after Stop-Mode Recovery.

5. SPI functions are not supported.

6. When using the CCP Emulator to emulate the C06, the comparator outputs are at P34 and P37, which is different than the C06, which is at P34 and P35.

Z86C04/C08/C07

1. WDT Register (F) %0F can only be written in the first 64 internal system clocks from the start of program execution (need for emulation of device only).

2. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08/30/31, the register %F8 (PO1M register) bits D4 and D3 must be set to state 0 and bit D2 must be set to state 1.

3. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08 emulation, the IRQ3 rising edge interrupt of P32 is not supported. To implement the rising edge of P32, a jumper from P32 must be connected to Pin 1 of U27 74HCT04. Another jumper must connect the output of the 74HCT04 Pin 2 to P30 on emulation socket P3, Pin 25 or emulation socket P2, Pin 18.

4. Stop Mode. For Z86C04/08 or Z86E04/08, P27 is used to release Stop Mode. However, since the CCP™ emulator (C50 Ice Chip) is used, you must write to SMR(F)0B 101 in D2, D3, and D4. Use the following code:

```
LD RP, #%0F              ;select Bank F
LD %0B, #00010100B       ;selects P27 as the Stop-Mode
                          Recovery pin.
```

This code must be removed before final ROM code submission or OTP programming. Note that P27 must be in Input Mode, which is accomplished with the following code:

```
LD P2M, #1xxxxxxB
NOP                      ;clears pipeline
Stop                     ;halts processor
```

5. Z86C04/07/08 and Z86E04/07/08 do not support the Watch-Dog Timer (WDT) running in Stop Mode.

6. Z86C04/07/08 and Z86E04/07/08 do not support WDT register. Use the command "4F" to run WDT in HALT Mode.

7. For Z86C07 emulation, the permanent WDT is not emulated. We recommend that you make the first instruction an enable WDT (5F hex).

8. For Z86C07 emulation, the "No Auto Latch" feature is not implemented.

9. The Z86E07 does not have permanently enabled WDT.

10. For Z86C04/07/08 and Z86E04/07/08, the register %FA (IRQ register) bits D7 and D6 must be set to state "0."

Z86E04/E08/E07

1. WDT Register (F1 %0F can only be written in the first 64 internal system clocks from the start of program execution (need for emulation of device only).

2. Z86E04 and Z86E08 have special features such that programming the ROM Protect mode will also put the device in Low EMI mode, where XTAL frequency = internal SCLK and all output drive capabilities are reduced by 75%.

3. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08/30/31, the register %F8 (PO1M register) bits D4 and D3 must be set to state 0 and bit D2 must be set to state 1.

4. Z86C04/07/08 Emulation Rising Edge of P32. For Z86C04/07/08 emulation, the IRQ3 rising edge interrupt on P32 is not supported. To implement the rising edge of P32, a jumper from P32 must be connected to Pin 1 of U27 74HCT04. Another jumper must connect the output of the 74HCT04 Pin 2 to P30 on emulation socket P3, Pin 25 or emulation socket P2, Pin 18.

5. Stop Mode. For Z86C04/08 or Z86E04/08, P27 is used to release Stop Mode. However, since the CCP™ emulator (C50 Ice Chip) is used, you must write to SMR(F) 0B 101 in D2, D3, and D4. Use the following code:

```
LD RP, #%0F              ;selects Bank F
LD %0B, #00010100B       ;selects P27 as the Stop-Mode
                          Recovery pin.
```

This code must be removed before final ROM code submission or OTP programming. Note that P27 must be in Input Mode, which is accomplished with the following code:

```
LD P2M, #1xxxxxxB
NOP                      ;clears pipeline
Stop                     ;halts processor
```

6. Z86C04/07/08 and Z86E04/07/08 do not support the Watch-Dog Timer (WDT) running in Stop Mode.

7. Z86C04/07/08 and Z86E04/07/08 do not support WDT register. Use the command "4F" to run WDT in HALT Mode.

8. For Z86E07, the "No Auto Latch" feature is not implemented.

9. For Z86C04/07/08 and Z86E04/07/08, the register %FA (IRQ register) bits D7 and D6 must be set to state "0."

Z86C30/31 and Z86E30/31

1. The Z86C30/31/40/50 and Z86E30/31/40 have the P32 comparator output coming out of P37.

2. Reg (F) %00 PCON has D2 controlling the open-drain for Port 0 and D1 controlling the open-drain for Port 1. This is for the following:
   Z86C30/31/40/50
   Z86E30/31/40

3. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08/30/31, the register %F8 (PO1M register) bits D4 and D3 must be set to state 0 and bit D2 must be set to state 1.

4. WDT Register (F) %0F can only written in the first 64 internal system clocks from the start of program execution.

5. For Z86C30/31, the "No Auto Latch" feature is not implemented.

6. To emulate the Z86C89/90, select the "Z86C40/E40' option from the "Microcontroller" pull-down window of the Configuration dialog box, which appears when the Z8® CCP™ GUI starts up and when the Configuration Menu item is selected from the ICEBOX™ Menu.

Z86C40/50 and Z86E40

1. WDT Register (F) %0F can only be written in the first 64 internal system clocks from the start of program execution.

2. The Z86C30/31/40/50 and Z86E30/31/40 have the P32 comparator output coming out of P37.

3. Reg (F) %00 PCON has D2 controlling the open-drain for Port 0 and D1 controlling the open-drain for Port 1. This is for the following:
   Z86C30/31/40/50
   Z86E30/31/40

4. For Z86C40, the "No Auto Latch" feature is not implemented.

Z86CCP00ZTK

Z8® MICROCONTROLLER TRAINING KIT

HARDWARE FEATURES

- Supported Products

Packages	Emulation	Programming	Notes
18-Pin DIP	Z86C03/04/06/07/ 08/09/16/19 Z86E03/04/06/07/08	Z86E04/07/08 Z86E03/06	[1]
20-Pin DIP	N/A	Z86717	[2]
18-Pin SOIC	N/A	Z86E04/07/08	[3]
		Z86E03/06	[1]
20-Pin SOIC	N/A	Z86717	[4]
20-Pin SSOP	N/A	Z86717	[5]
28-Pin DIP	Z86C30/31/32/233	Z86E30/31	[6],[7]
28-Pin SOIC	N/A	N/A	
40-Pin DIP	Z86C40/243	Z86E40	[7],[8]
44-Pin PLCC	N/A	N/A	
44-Pin QFP	N/A	N/A	

Notes:
[1] E03/06: With optional, separately purchased adapter, Z86E0601ZDP.
[2] With optional, separately purchased adapter, Z86E0700ZDP.
[3] With optional, separately purchased adapter, Z8671701ZDP.
[4] With optional, separately purchased adapter, Z8671701ZDS.
[5] With optional, separately purchased adapter, Z8671701ZDH.
[6] To emulate Z86233, select Z86C30 with 8 KB of ROM.
[7] E30/31/40: With opt., separately purchased acc. kit, Z86CCP00ZAC
[8] To emulate Z86243, select Z86C40 with 8 KB of ROM.

- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Z8 GUI Emulator Software
- Bit-Programmable I/O Ports for Digital Input/Output Functions
- RS-232 Connector
- One-Time Programmable (OTP) Option
- Windows-Based Training Course and Test on 3.5-Inch Floppy Disk

GENERAL DESCRIPTION

The Z86CCP00ZTK is a member of Zilog's family of in-circuit emulators providing support for the Consumer Controller Processor (CCP™) microcontrollers, with the addition of a Windows-based training and test program.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering, program debugging, and OTP programming are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z86CCP00ZTK's technical manual includes documentation to help train new users with Z8 designs. The computer-based training course incorporates interactive questions and answers to reinforce learning.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +7.5 VDC to +9.0 VDC
(+8.0 VDC Typical)
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 8 MHz

Power Requirements

+8.0 VDC @ 0.5A Minimum

Dimensions

Width: 7.0 in. (17.7 cm)
Length: 9.0 in. (22.9 cm)
Height: 0.9 in. (2.3 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z8® CCP™ Emulator

CMOS Z86C9320VSC
20 MHz CMOS Z86C5020FSE ICE Chip
8K x 8 Static RAM (For Code Memory)
18-Pin DIP Zero Insertion Force (ZIF) Programming Socket
Sockets Available for 18/28/40-Pin Target Cables
Holes Available for 28/40-Pin ZIF Sockets
RS-232C Interface
Reset Switch

Cables

18-Pin DIP Target Cable

Devices

One Z86E0812PSC (18-Pin DIP)

Software (IBM PC Platform)

Z8 GUI Emulator Software
ZASM Cross-Assembler / MOBJ Object File Utilities
Production Languages Corporation COMPASS/Z8 (Evaluation Version)
Z8 Training Course and Test

Documentation

Emulator User Manual
Discrete Z8 Databook
Z8 Microcontroller Technical Manual
Registration Card
Product Information

Z8 CCP Emulator Accessory Kit (Z86CCP00ZAC)

(Not Included with Z86CCP00ZTK)
28-Pin ZIF Socket
28-Pin DIP Target Cable
40-Pin ZIF Socket
40-Pin DIP Target Cable
DB25 RS-232C Cable
Power Cable with Banana Plugs

LIMITATIONS

1. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

3. Switching ICEBOXes without quitting the GUI is not supported.

4. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

5. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

   ```
   000C    SRP    #%0
   000E    LD     R4, #%0016
   0010    LD     R5, @R4
   0012    NOP
   0013    JP     %000C
   0016    NOP
   ```

   Setting the breakpoint at %0016 and click GO.

   Result: The code will break and stop at %0012.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

6. If the emulator is running a user code at full speed and the port window is opened: Switching to another application or minimizing the GUI (then restoring) will result in the following ICEBOX Communications Error message: "Emulator rejected command: target program is executing." This message may need to be cleared several times (as many as seven) before the GUI returns to normal operation.

   Workaround: Always close the port window before leaving the GUI.

7. Do not put breakpoint at address after Stop instruction. This will cause program counter to continue at that location after a Stop-Mode Recovery.

8. Since the emulator uses the C50 ICE Chip, port 1 cannot be configured to Low EMI mode. (Bit 4 in PCON registers must be set to logic "1").
   Note: This is not a problem with the actual emulated device.

PRECAUTIONS

All Devices

1. All Z8 control registers are Write-Only unless stated otherwise.

2. Programming the ROM protect bit on all Z8s and Z8 OTPs will disable all use of the LDC, LDCI, LDE, and LDEI instructions. Thus, ROM protect does not support the use of a ROM look-up table. The value must be loaded as "immediate values."

3. The special OTP programming options such as ROM protect, RAM protect, Low Noise, and RC will be programmed if the option has been selected and the VERIFY command was then executed.

4. Power Supply ramp-up/rise time must be such that when minimum power-on reset time (T_{POR}) expires, then the V_{CC} must be in the supported specified operating range of the device.

5. The bits of non-implemented features (of devices having a PCON register) must be set to "1" state on the emulator.

6. The jumpers for implementing IRQ3 rising edge interrupt on P32 for Z86C04/C07/C08/E04/E08 must be removed when emulating other devices.

7. Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the ICE chip specifications.

8. The general-purpose registers after Power-On Reset or at initial emulator use will be different than the actual device. The emulator self test will always leave the same values in the general-purpose registers, while the real device will have a random/undefined value in the general-purpose registers.

9. RC oscillator emulation is not supported.

10. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

PRECAUTION LIST (Continued)

11. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization must be disabled prior to invoking the VERIFY operation.

12. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

13. For 386 PCs, set the baud rate to 19.2K or less because Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.

14. Do not press hardware reset when the ICEBOX is in OTP programming. If reset is pressed while the GUI is doing OTP programming, close the OTP dialog window and reopen it to reload the information back to the hardware.

    Note: Although the Command Status shows "Processing" after the GUI reestablishes the communication link when Retry was selected, the ICEBOX is actually sitting idle.)

Z86C03/06/09/16

1. Devices with the comparator output feature have the P32 comparator output coming out of P335.

2. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08/30/31, the register %F8 (PO1M register) bits D4 and D3 must be set to state 0 and bit D2 must be set to state 1.

3. WDT Register (F) %0F can only be written in the first 64 internal system clocks from the start of program execution.

4. The PCON register on Z86C16 is not reset after Stop-Mode Recovery.

5. SPI functions are not supported.

6. When using the CCP Emulator to emulate the C06, the comparator outputs are at P34 and P37, which is different than the C06, which is at P34 and P35.

Z86C04/C08/C07

1. WDT Register (F) %0F can only be written in the first 64 internal system clocks from the start of program execution (need for emulation of device only).

2. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08/30/31, the register %F8 (PO1M register) bits D4 and D3 must be set to state 0 and bit D2 must be set to state 1.

3. Z86C04/07/08 Emulation Rising Edge of P32. For Z86C04/07/08 emulation, the IRQ3 rising edge interrupt on P32 is not supported. To implement the rising edge of P32, a jumper from P32 must be connected to Pin 1 of U27 74HCT04. Another jumper must connect the output of the 74HCT04 Pin 2 to P30 on emulation socket P3, Pin 25 or emulation socket P2, Pin 18.

4. Stop Mode. For Z86C04/08 or Z86E04/08, P27 is used to release Stop Mode. However, since the CCP™ emulator (C50 Ice Chip) is used, you must write to SMR(F)0B 101 in D2, D3, and D4. Use the following code:

```
LD RP, #%0F              ;select Bank F
LD %0B, #00010100B       ;selects P27 as the
                          Stop-Mode Recovery pin.
```

   This code must be removed before final ROM code submission or OTP programming. Note that P27 must be in Input Mode, which is accomplished with the following code:

```
LD P2M, #1xxxxxxxB
NOP                      ;clears pipeline
Stop                     ;halts processor
```

5. Z86C04/07/08 and Z86E04/07/08 do not support the Watch-Dog Timer (WDT) running in Stop Mode.

6. Z86C04/07/08 and Z86E04/07/08 do not support WDT register. Use the command "4F" to run WDT in HALT Mode.

7. For Z86C07 emulation, the permanent WDT is not emulated. We recommend that you make the first instruction an enable WDT (5F hex).

8. For Z86C07 emulation, the "No Auto Latch" feature is not implemented.

9. The Z86E07 does not have permanently enabled WDT.

10. For Z86C04/07/08 and Z86E04/07/08, the register %FA (IRQ register) bits D7 and D6 must be set to state "0."

Z86E04/E08/E07

1. WDT Register (F) %0F can only be written in the first 64 internal system clocks from the start of program execution (need for emulation of device only).

2. Z86E04 and Z86E08 have special features such that programming the ROM Protect mode will also put the device in Low EMI mode, where XTAL frequency = internal SCLK and all output drive capabilities are reduced by 75%.

3. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08/30/31, the register %F8 (PO1M register) bits D4 and D3 must be set to state 0 and bit D2 must be set to state 1.

4. Z86C04/07/08 Emulation Rising Edge of P32. For Z86C04/07/08 emulation, the IRQ3 rising edge interrupt on P32 is not supported. To implement the rising edge of P32, a jumper from P32 must be connected to Pin 1 of U27 74HCT04. Another jumper must connect the output of the 74HCT04 Pin 2 to P30 on emulation socket P3, Pin 25 or emulation socket P2, Pin 18.

5. Stop Mode. For Z86C04/08 or Z86E04/08, P27 is used to release Stop Mode. However, since the CCP™ emulator (C50 Ice Chip) is used, you must write to SMR(F)0B 101 in D2, D3, and D4. Use the following code:

```
LD RP, #%0F              ;select Bank F
LD %0B, #00010100B       ;selects P27 as the
                          Stop-Mode Recovery pin.
```

   This code must be removed before final ROM code submission or OTP programming. Note that P27 must be in Input Mode, which is accomplished with the following code:

```
LD P2M, #1xxxxxxxB
NOP                      ;clears pipeline
Stop                     ;halts processor
```

6. Z86C04/07/08 and Z86E04/07/08 do not support the Watch-Dog Timer (WDT) running in Stop Mode.

7. Z86C04/07/08 and Z86E04/07/08 do not support WDT register. Use the command "4F" to run WDT in HALT Mode.

8. For Z86E07, the "No Auto Latch" feature is not implemented.

9. For Z86C04/07/08 and Z86E04/07/08, the register %FA (IRQ register) bits D7 and D6 must be set to state "0."

PRECAUTION LIST (Continued)

Z86C30/31 and Z86E30/31

1. The Z86C30/31/40/50 and Z86E30/31/40 have the P32 comparator output coming out of P37.

2. Reg (F) %00 PCON has D2 controlling the open-drain for Port 0 and D1 controlling the open-drain for Port 1. This is for the following:
   Z886C30/31/40/50
   Z86E30/31/40

3. For Z86C03/04/06/07/08/09/16/19/30/31 and Z86E03/04/07/08/30/31, the register %F8 (PO1M register) bits D4 and D3 must be set to state 0 and bit D2 must be set to state 1.

4. WDT Register (F) %0F can only be written in the first 64 internal system clocks from the start of program execution.

5. For Z86C30/31, the "No Auto Latch" feature is not implemented.

6. To emulate the Z86C89/90, select the "Z86C40/E40" option from the "Microcontroller" pull-down window of the Configuration dialog box, which appears when the Z8® CCP™ GUI starts up and when the Configuration Menu item is selected from the ICEBOX™ Menu.

Z86C40/50 and Z86E40

1. WDT Register (F) %0F can only be written in the first 64 internal system clocks from the start of program execution.

2. The Z86C30/31/40/50 and Z86E30/31/40 have the P32 comparator output coming out of P37.

3. Reg (F) %00 PCON has D2 controlling the open-drain for Port 0 and D1 controlling the open-drain for Port 1. This is for the following:
   Z886C30/31/40/50
   Z86E30/31/40

4. For Z86C40, the "No Auto Latch" feature is not implemented.

Z86E0600ZDP

Z86E19/09/06
CONVERTER KIT

GENERAL DESCRIPTION

The Z86E06 converter board is a simple adapter which converts the 28-pin footprint of the Zilog Z86E30 OTP chip to the 18-pin DIP configuration of the Z86E06/09/19 OTP chip. The converter supports all the functions of the Z86E06/09/19 except for SPI function.

SUPPORTED DEVICES

Z86E06/09/19

SPECIFICATIONS

Power Requirements
Not applicable

Dimensions
Width: 0.8 in. (2.0 cm)
Length: 1.5 in. (3.8 cm)

KIT CONTENTS

Z86E06 Converter Board
28-Pin Z86E30 MCU Socket
18-Pin Z86E06/09/19 Connector

Cables
25-Pin RS-232 Cable
18-Pin Z86C19 Emulation Cable

Documentation
Z86E06 OTP Converter Kit User Guide

Document No.	Description
99C0214-001	Z86E19/09/06 Converter Kit

ORDERING INFORMATION

Part No: Z86E0600ZDP

Z86E0601ZDP

Z86E06/Z86E03 OTP ADAPTER KIT

FEATURES

- Supported Devices

Part	Packages	Speed (MHz)
Z86E03/E06	18-Pin DIP	8, 12
Z86E03/E06	18-Pin SOIC	8, 12

- Allows Z86E06/E03 Development System Programming

GENERAL DESCRIPTION

The Z86E0601ZDP is an adapter kit specifically designed to enable Zilog's Z86E06 and Z86E03 One-Time Programmable (OTP) microcontrollers to be programmed by selected Zilog emulators (the C12 ICEBOX™, C50 ICEBOX, and the Z8® CCP™ Emulator).

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C ± 10°C

Power Requirements

Not Applicable

Dimensions

Width: 1.55 inches
Length: 1.65 inches

KIT CONTENTS

Z86E06 OTP Program Adapter Board
- 18-Pin DIP ZIF Socket
- 18-Pin SOIC ZIF Socket
- 18-Pin Connector

Documentation

Z86E06 OTP Programming Adapter Kit User's Guide

Z86E0700ZDP

OTP PROGRAM CONVERTER KIT

GENERAL DESCRIPTION

The Z86E07 OTP (One Time Programmable) Converter Kit adapts an 18-pin SOIC package to an 18-pin DIP package. This allows Z86E07 DIP OTP programmers to program the 18-pin SOIC Z86E07 OTP microcontroller.

Supported Device

Z86E07 SOIC and SOIC (18-pin) to DIP (18-pin) Devices

Specifications

Power Requirements
Not Applicable

Dimensions
Width: 0.95 in.
Length: 1.10 in.

Operating Voltage Range
Not Applicable

Operating Temperature
0 to 50°C

Operating Humidity
10-90% RH (Non-Condensing)

KIT CONTENTS

Z86E07 OTP Program Converter Board

18-Pin SOIC ZIF Socket
18-Pin DIP Connector

Documentation
Z86E07 OTP Program Converter User Guide

Ordering Information
Part No: Z86E0700ZDP

Z86E2100ZDP/ZDV/ZDF

Z86E21 OTP ADAPTER KIT

GENERAL DESCRIPTION

The 86E21 OTP Adapter Kit allows a standard EPROM programmer to program the Z86E21 One-Time-Programmable microcontroller, and the Z86E21 Erasable-Programmable microcontroller.

KIT CONTENTS

Z86E21 Adapter Board Kit includes:

Document No.	Description	Hardware Revision
99C0147-001	Z86E2100ZDP DIP Programming Adapter	B
99C0147-002	Z86E2100ZDV PLCC Programming Adapter	B
99C0147-003	Z86E2100ZDF QFP Programming Adapter	B

Z86E2101ZDV/ZDF

Z86E21 CONVERSION KIT

GENERAL DESCRIPTION

The Z86E2101ZDV Kit converts the pin-outs of the 44-pin PLCC package to that of the 40-pin DIP package.

The Z86E2101ZDF Kit converts the pin-outs of the 44-pin QFP package to that of the 40-pin DIP package.

KIT CONTENTS

Z86E21 Conversion Kit includes:

Document No.	Description	Hardware Revision
99C0229-001	Z86E2101ZDV PLCC Converter	A
99C0230-001	Z86E2101ZDF QFP Converter	A

Z86E4000ZDP/ZDV/ZDF

Z86E40 OTP ADAPTER KIT

GENERAL DESCRIPTION

The 86E40 OTP Adapter Kit allows a standard EPROM programmer to program the Z86E40 One-Time-Programmable microcontroller, and the Z86E40 Erasable-Programmable microcontroller.

KIT CONTENTS

Z86E40 Adapter Board Kit includes:

Document No.	Description	Hardware Revision
99C0201-001	Z86E4000ZDP DIP Programming Adapter	B
99C0201-002	Z86E4000ZDV PLCC Programming Adapter	B
99C0201-003	Z86E4000ZDF QFP Programming Adapter	B

Z86E4001ZDV/ZDF

Z86E40 CONVERSION KIT

GENERAL DESCRIPTION

The 86E4001ZDV Kit converts the pin-outs of the 44-pin PLCC package to that of the 40-pin DIP package.

The Z86E4001ZDF Kit converts the pin-outs of the 44-pin package to that of the 40-pin DIP package.

KIT CONTENTS

Z86E40 Converter Board Kit includes:

Document No.	Description	Hardware Revision
99C0232-001	Z86E4001ZDV PLCC Converter	B
99C0231-001	Z86E4001ZDF QFP Converter	A

ZiLOG

8-Bit Microcontrollers

Z86C02/E02/L02

LOW-COST, 512-BYTE ROM MICROCONTROLLERS

FEATURES

Device	ROM (KB)	RAM* (Bytes)	Speed (MHz)	Auto Latch	Permanent WDT
Z86C02	512	61	8	Optional	Optional
Z86E02	512	61	8	Optional	Optional
Z86L02	512	61	8	Optional	Optional

Note: *General-Purpose

- 18-Pin DIP and SOIC Packages
- 0°C to 70°C Standard Temperature
  –40°C to 105°C Extended Temperature
  (Z86C02/E02 only)
- 3.0V to 5.5V Operating Range (Z86C02)
  4.5V to 5.5V Operating Range (Z86E02)
  2.0V to 3.9V Operating Range (Z86L02)
- 14 Input / Output Lines
- Five Vectored, Prioritized Interrupts from Five Different Sources
- Two On-Board Comparators
- Software Enabled Watch-Dog Timer (WDT)
- Programmable Interrupt Polarity
- Two Standby Modes: STOP and HALT
- Low-Voltage Protection
- ROM Mask/OTP Options:
  - Low-Noise (Z86C02/E02 only)
  - ROM Protect
  - Auto Latch
  - Permanent Watch-Dog Timer (WDT)
  - RC Oscillator (Z86C02/L02 Only)
  - 32 KHz Operation (Z86C02/L02 Only)
- One Programmable 8-Bit Counter/Timer with a 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer
- On-Chip Oscillator that Accepts RC, Crystal, Ceramic Resonator, LC, or External Clock Drive (C02/L02 only)
- On-Chip Oscillator that Accepts RC or External Clock Drive (Z86E02 SL1903 only)
- On-Chip Oscillator that Accepts Crystal, Ceramic Resonator, LC, or External Clock Drive (Z86E02 only)
- Clock-Free WDT Reset
- Low-Power Consumption (50mw)
- Fast Instruction Pointer (1.5µs @ 8 MHz)
- Fourteen Digital Inputs at CMOS Levels; Schmitt-Triggered

GENERAL DESCRIPTION

Zilog's Z86C02/E02/L02 microcoontrollers (MCUs) are members of the Z8® single-chip microcontroller family which offer easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the MCU's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

One on-chip counter/timer, with a large number of user selectable modes, off-load the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

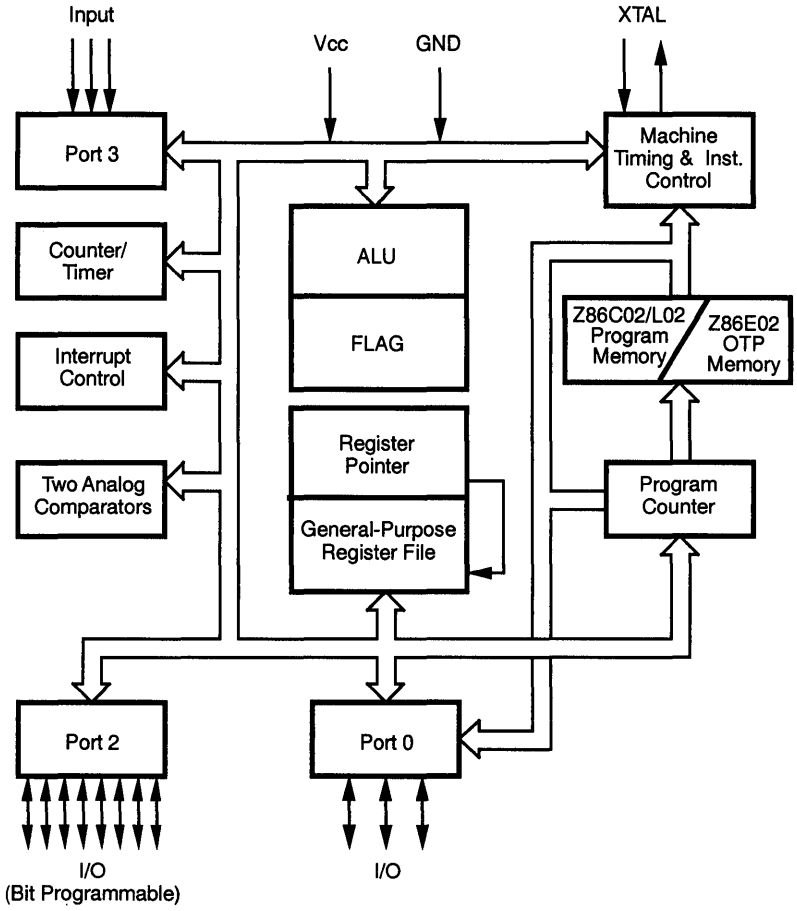


Figure 1. Z86C02/E02/L02 Functional Block Diagram

Z86C72/C92/L72/L92

IR/LOW-VOLTAGE MICROCONTROLLER

FEATURES

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86C72	16	748	31	4.5V to 5.5V
Z86C92	0	748	31	4.5V to 5.5V
Z86L72	16	748	31	2.0V to 3.9V
Z86L92	0	748	31	2.0V to 3.9V

Note: *General-Purpose

- Two Standby Modes (Typical)
  - STOP - 2 μA
  - HALT - 0.8 mA
- Expanded Register File Control Registers
- Automatic External ROM Access Beyond 16K (Z86L72 Version)
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Register
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
- Low Voltage Detection and Protection
- Programmable Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC (mask option), or External Clock Drive
- Mask Selectable 200 kOhms Pull-Ups on Ports 0, 2, 3
- All Eight Port 2 Bits at One Time or Not Pull-Ups Automatically Disabled Upon Selecting Individual Pins as Outputs.
- Maskable Mouse/Trackball Interface on P00 Through P03 is available on the L72 version.

GENERAL DESCRIPTION

The Z86C7X/L7X family of IR (Infrared) are ROM/ROM-less-based members of the Z8® single-chip microcontroller family with 768 bytes of internal RAM. The differentiating factor between these devices is the availability of RAM, ROM and package options. The use of external memory enables these Z8 microcontrollers to be used where code flexibility is required. Offering the 3V versions (Z86CXX) and gives optimum performance in both the low and high voltage ranges. Zilog's CMOS Low-Voltage Microcontroller offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up resistors. The Z86C/L7X product line offers easy hardware/software system expansion with low cost and low power consumption.

The Z86C7X/L7X architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

CCP™ applications demand powerful I/O capabilities. The Z86L/C7X family fulfills this with three package options in which the L72 version provides 31 pins of dedicated input and output. These lines are grouped into four ports. Each port consists of eight lines (Port 3 has seven lines) and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory. The lower pin count version reduces the I/O count as shown in the pin descriptions while maintaining hardware and software compatibility, thereby providing the user a wide spectrum of I/O options without major rework/changes when migrating to different family versions.

There are five basic address spaces available to support a wide range of configurations: Program Memory, Register File, Expanded Register File. Extended Data RAM and External Memory. The register file is composed of 256/128 bytes of RAM. It includes four I/O port registers, 16 control and status registers and the rest are General-Purpose registers. The Extended Data RAM (L72 only) adds 512 bytes of usable general-purpose registers. The Expanded Register FIle consists of two additional register groups (F and D). External Memory is not available on 18 and 20-pin versions.

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86C/L7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

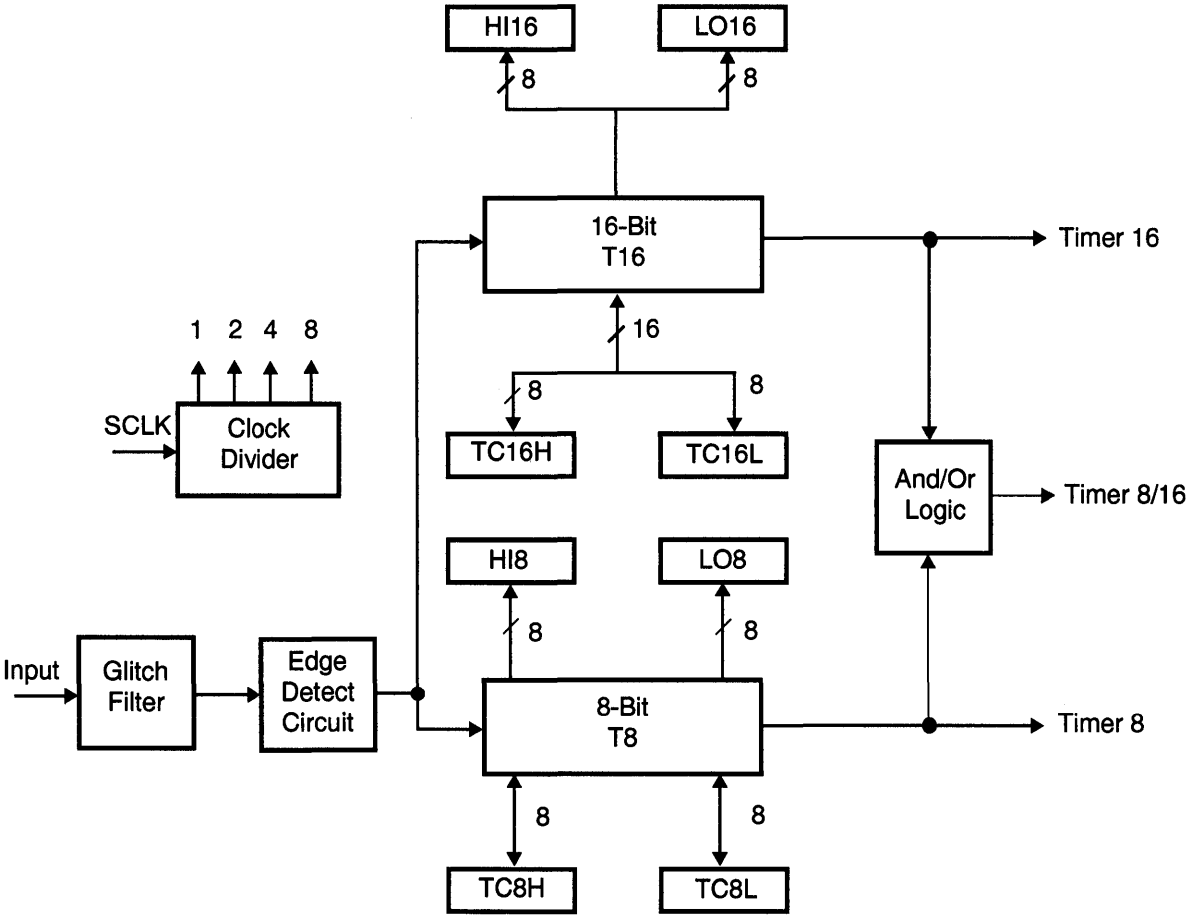


Figure 1. Counter/Timer Block Diagram

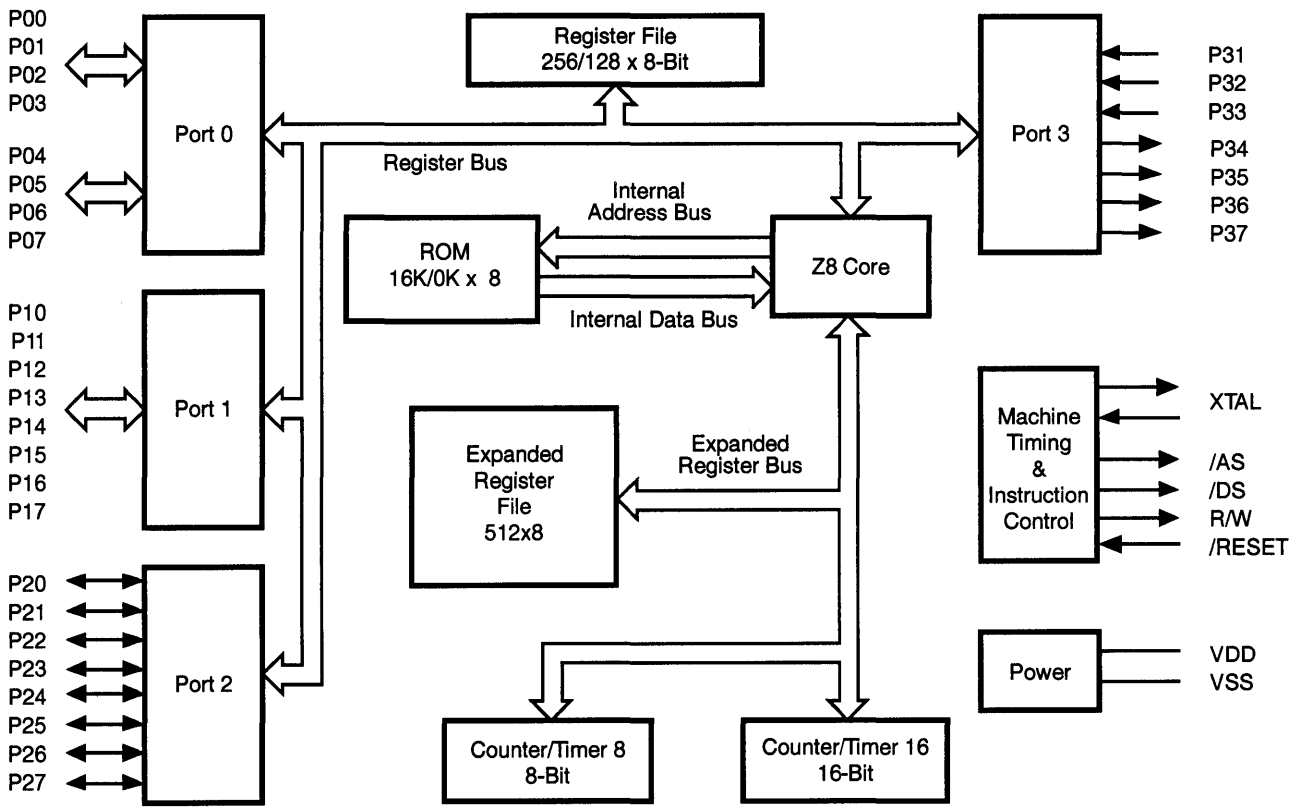


Figure 2. Functional Block Diagram

Note: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Z86E72/73
IR/OTP MICROCONTROLLER

FEATURES

Part	ROM (Kbytes)	RAM* (Bytes)	I/O	Voltage Range
Z86E72	16	748	31	3.0V to 5.5V
Z86E73	32	236	31	3.0V to 5.5V

Note: *General-Purpose

- Low Power Consumption - 60 mW (Typical)
- Two Standby Modes (Typical)
  - STOP - 2 µA
  - HALT - 0.8 mA
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
  - Three External
  - Two Assigned to Counter/Timers
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC (mask option), or External Clock Drive
- Software Selectable 200 kOhms Pull-Ups on Ports 0 and Port 2
  - All Eight Port 2 Bits at One Time or Not Pull-Ups Automatically Disabled Upon Selecting Individual Pins as Outputs.
- Software Mouse/Trackball Interface on P00 Through P03

GENERAL DESCRIPTION

The Z86E7X family of IR (Infrared) CCP™ (Consumer Controller Processor) Controllers are OTP-based members of the Z8® single-chip microcontroller family with 236 or 748/1004 bytes of general-purpose RAM. The only differentiating factor between the versions is the availability of RAM and ROM. The Z86E72/73 provide the high-end of the ROM/RAM and I/O options. The Low-Voltage Microcontrollers family of ROM devices (E72/73) offers the use of external memory which enables this Z8 microcontroller to be used where code flexibility is required. Zilog's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E7X architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

CCP™ applications demand powerful I/O capabilities. The Z86L7X family fulfills this with five package options in which the E72/73/L74 versions provide 31 and 51 pins respectively of dedicated input and output. These lines are grouped into four ports for the E72/E73. Each port consists of eight lines (Port 3 has seven lines and Port 6 has four lines) and is configurable under software control to provide

GENERAL DESCRIPTION (Continued)

timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are five basic address spaces available to support a wide range of configurations: Program Memory, Register FIle, Expanded Register File, Extended Data RAM and External Memory. The register file is composed of 256 bytes of RAM. It includes four I/O port registers, 16 control and status registers and the rest are General Purpose registers. The Extended Data RAM adds 512 (E72) bytes of usable general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86L7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

Notes: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

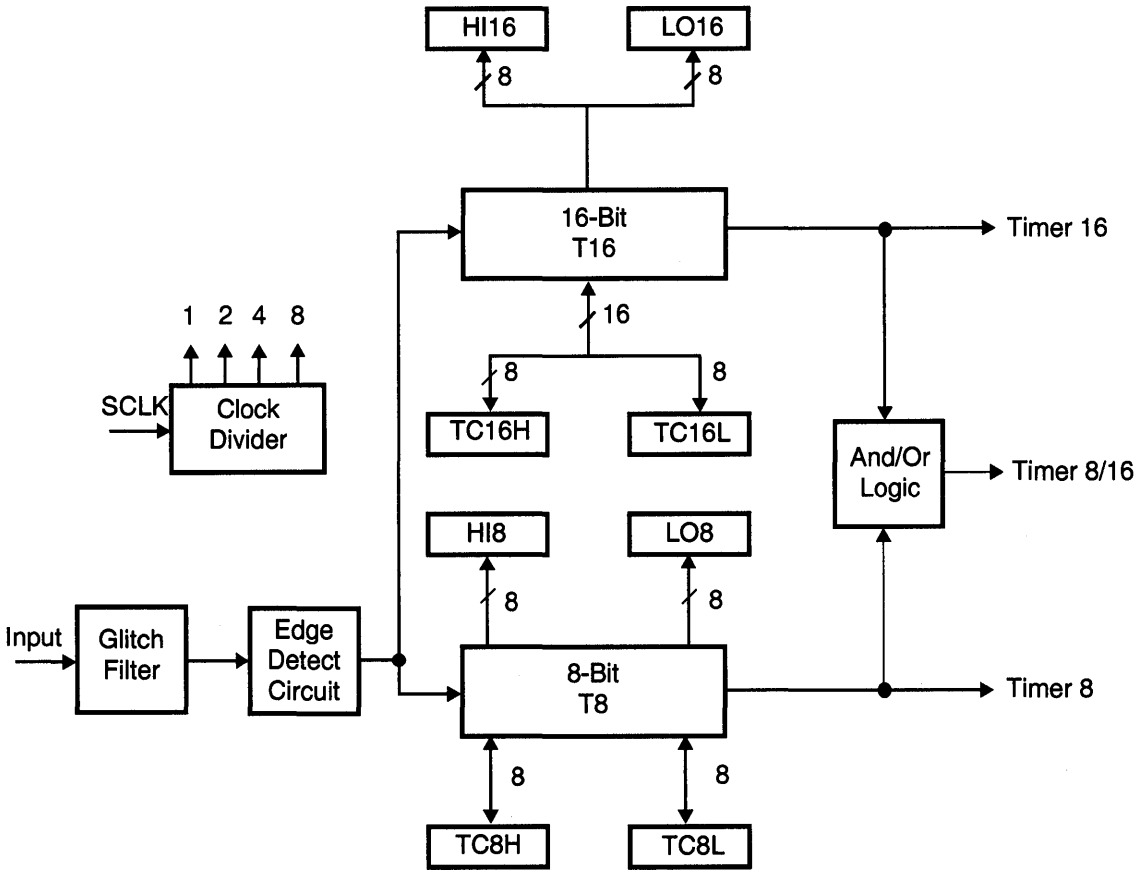


Figure 1. Counter/Timer Block Diagram

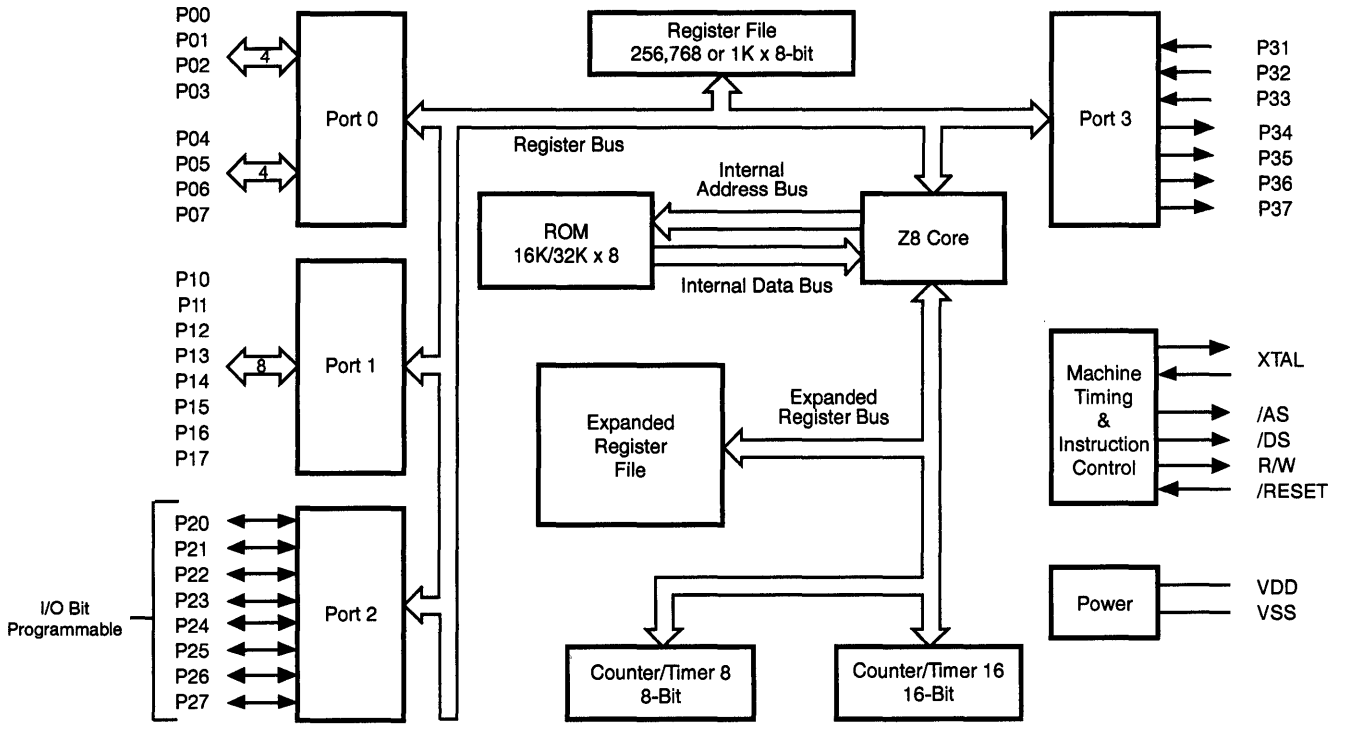


Figure 2. Functional Block Diagram

Z86L04/L08

CMOS Z8® 8-BIT LOW-COST 1K/2K-ROM MICROCONTROLLERS

FEATURES

Part Number	ROM (Kbytes)	RAM* (Bytes)	Speed (MHz)	Auto Latch	Permanent WDT
Z86L04	1	125	8	Optional	Optional
Z86L08	2	125	8	Optional	Optional

* General-Purpose

- 18-Pin DIP and SOIC Packages
- 2.0V to 3.9V Operating Range (0°C–70°C)
- 14 Input / Output Lines
- Six Vectored, Prioritized Interupts from Six Different Sources
- Two On-Board Comparators
- ROM Mask Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Permanent Watch-Dog Timer (WDT)
  - RC Oscillator
  - 32 KHz Operation
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer
- On-Chip Oscillator that Accepts RC, Crystal, Ceramic Resonance, LC, or External Clock Drive
- Clock-Free WDT Reset
- Low-Power Consumption (40mw typical)
- Fast Instruction Pointer (1.5µs @ 8 MHz)
- Fourteen Digital Inputs at CMOS Levels; Schmitt-Triggered
- Software Enabled Watch-Dog Timer
- Programmable Interrupt Polarity
- Two Standby Modes: STOP and HALT
- Low-Voltage Protection

2

GENERAL DESCRIPTION

Zilog's Z86L04/L08 Microcontrollers (MCU) are members of the Z8® single-chip microcontroller family which offer easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the Z86L04/L08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/ /W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

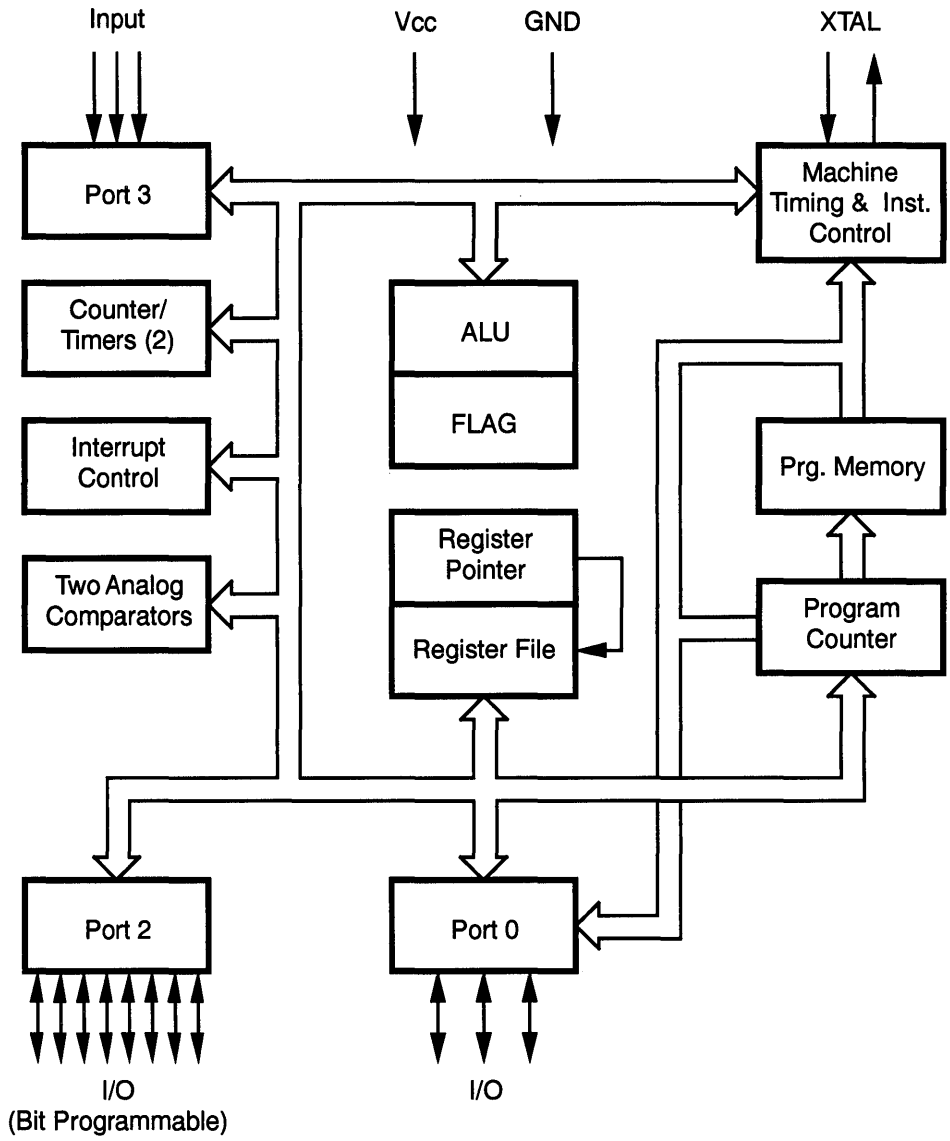


Figure 1. Z86L04/L08
Functional Block Diagram

Z86L29

IR/LOW-VOLTAGE MICROCONTROLLER

FEATURES

Part	ROM (KB)	RAM (Bytes)*	Speed	Voltage Range
Z86L29	6	125	8	2.0V to 3.6V

Note: *General-Purpose

- Low Power Consumption - 18 mW (Typical)
- Four High-Current Outputs at 2V
- 7 mA Source (1)
- 10 mA Sink (3)
- Two Standby Modes - STOP and HALT
- 14 Input/Output Lines (Two with Comparator Inputs)
- All Digital Inputs are CMOS Level
- Three Expanded Register File Control Registers
- Two Programmable 8-Bit Counter/Timers
- 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Five Different Sources
- Low Voltage Protection
- Watch-Dog/Power-On Reset Timer
- Two Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

GENERAL DESCRIPTION

The Z86L29 IR Controller is a low voltage Consumer Controller Processor (CCP™) is a member of Zilog's Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 6 Kbytes of ROM and 125 bytes of general-purpose RAM, this low cost, low power consumption CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86L29 architecture is characterized by Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, and a number of ancillary features that are useful in many industrial, automotive, hand held, battery operated, and advanced scientific applications.

For device applications that demand powerful I/O capabilities, the CCP fulfills this with 14 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

GENERAL DESCRIPTION (Continued)

Three basic address spaces are available to support this wide range of configurations; Program Memory, Register File, and Expanded Register File. The Register File is composed of 125 bytes of general-purpose registers, two I/O Port registers, and 14 Control and Status registers. The Expanded Register File consists of three control registers.

To unburden the program from coping with real-time problems such as counting/timing and input/output data communication, the Z86L29 offers two on-chip counter/timers with a large number of user selectable modes, and two on-board comparators that can process analog signals with a common reference voltage (Figure 1).

Notes: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

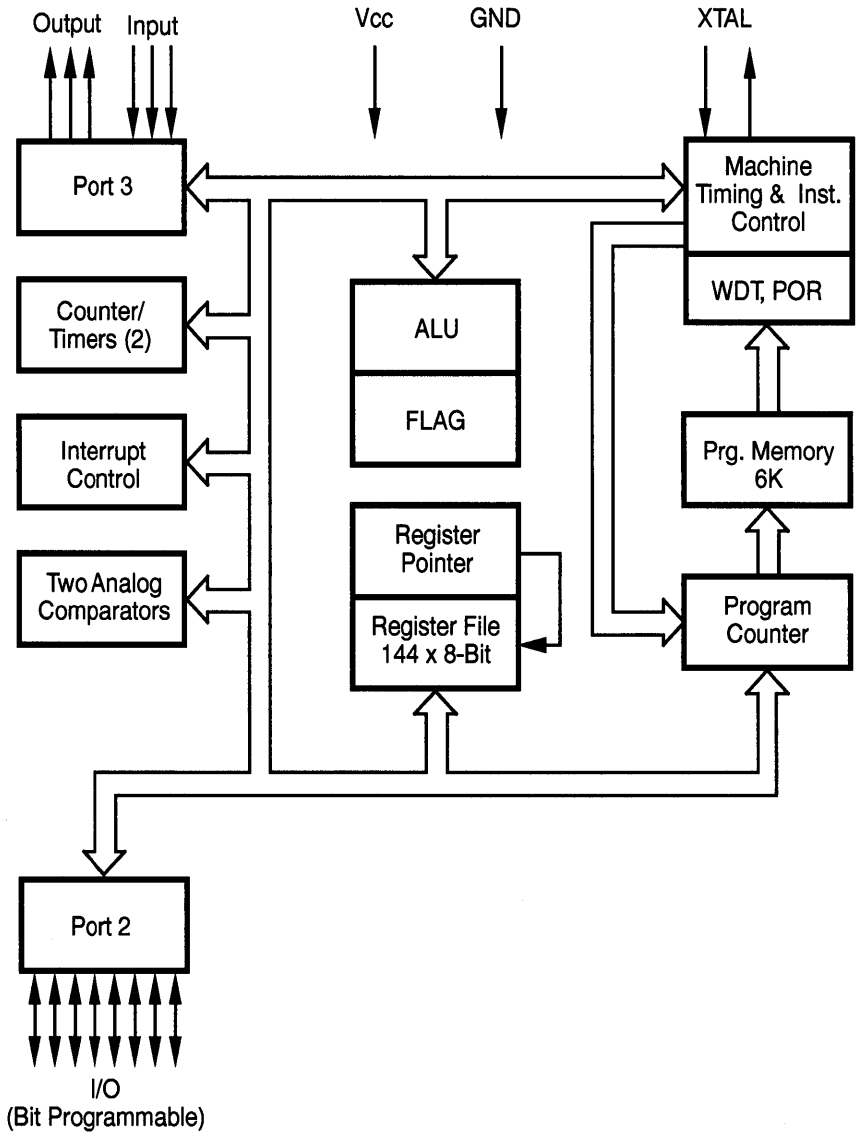


Figure 1. Functional Block Diagram

Z86L70/71/75/C71

IR/LOW-VOLTAGE MICROCONTROLLER

FEATURES

Part	ROM (Kbytes)	RAM* (Bytes)	I/O	Voltage Ranges
Z86L70	2	108	14	2.0V to 3.9V
Z86L71	8	236	16	2.0V to 3.9V
Z86L75	4	236	14	2.0V to 3.9V
Z86C71	8	236	16	4.5V to 5.5V

Note: *General-Purpose

- Two Standby Modes (Typical)
  - STOP - 2 µA
  - HALT - 0.8 mA
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Register
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
- Low Voltage Detection and Protection
- Programmable Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC (mask option), or External Clock Drive
- Mask Selectable 200 kOhms Pull-Ups on Ports 0, 2, 3
- All Eight Port 2 Bits at One Time or Not Pull-Ups Automatically Disabled Upon Selecting Individual Pins as Outputs.

GENERAL DESCRIPTION

The Z86L7X family of IR (Infrared) are ROM/ROMless-based members of the Z8® single-chip microcontroller family with 236/108 bytes of internal RAM. The differentiating factor between these devices is the availability of RAM, ROM and package options. The use of external memory enables these Z8 microcontrollers to be used where code flexibility is required. Offering the 3V versions (Z86LXX) and gives optimum performance in both the low and high voltage ranges. Zilog's CMOS Low-Voltage Mircocontroller microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up resistors. The Z86L7X product line offers easy hardware/software system expansion with low cost and low power consumption.

The Z86L7X architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

There are five basic address spaces available to support a wide range of configurations: Program Memory, Register File, Expanded Register File. Extended Data RAM and External Memory. The register file is composed of 256/128 bytes of RAM. It includes four I/O port registers, 16 control and status registers and the rest are General-Purpose registers. The Extended Data RAM (L7X only) adds 512 bytes of usable general-purpose registers. The Expanded Regis-

GENERAL DESCRIPTION (Continued)

ter FIle consists of two additional register groups (F and D). External Memory is not available on 18 and 20-pin versions.

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86L7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

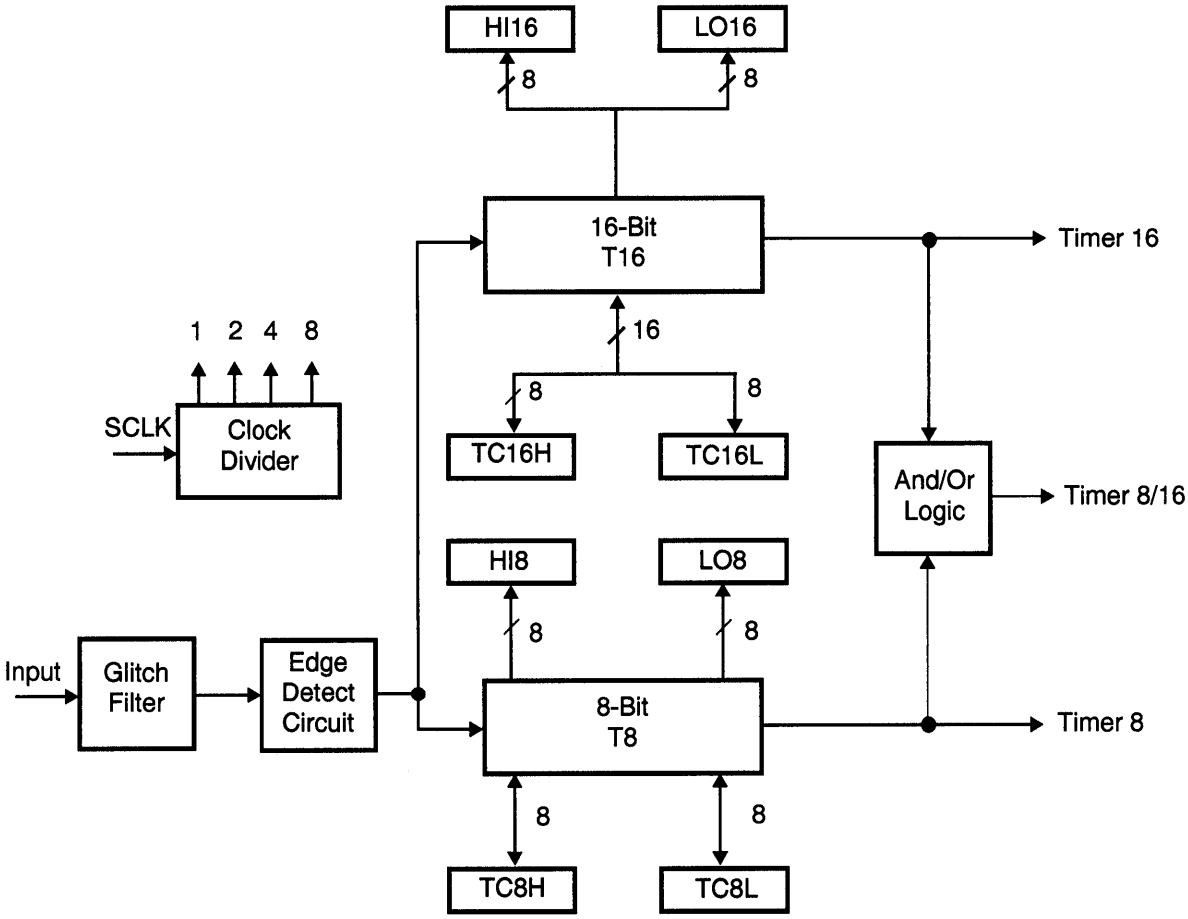


Figure 1. Counter/Timer Block Diagram

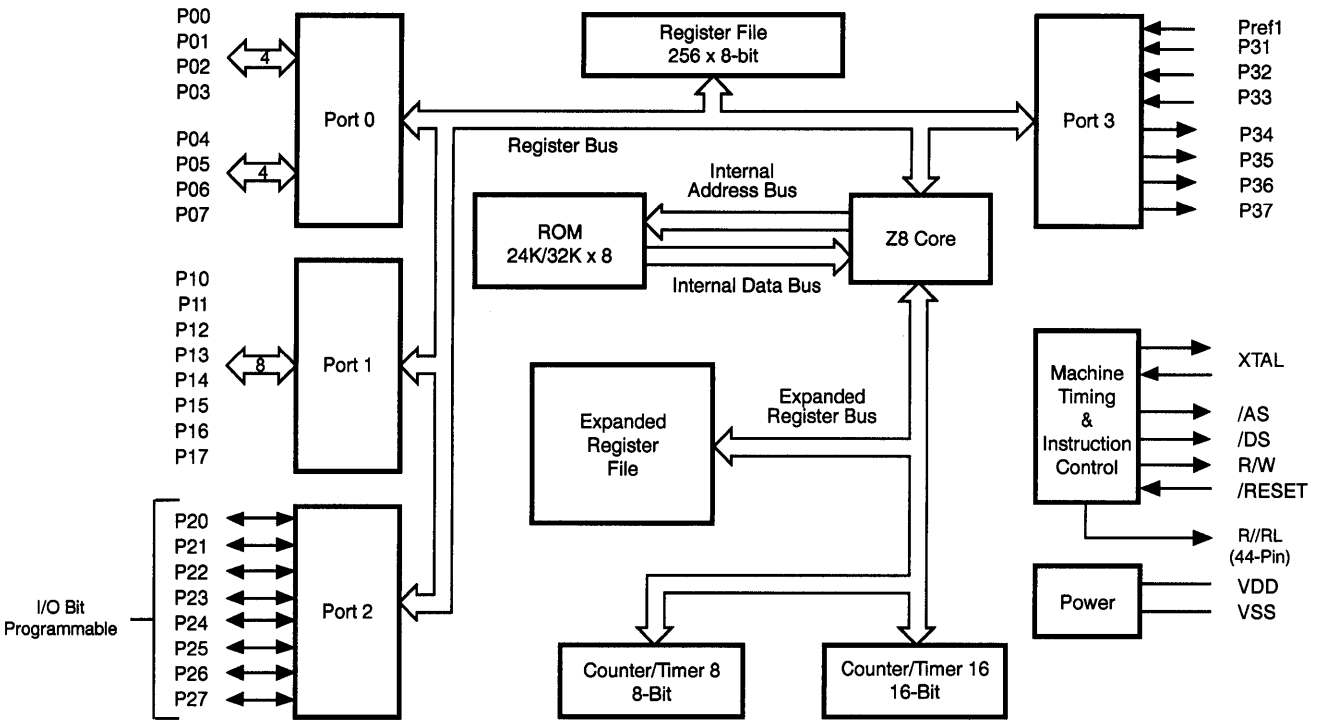


Figure 2. Functional Block Diagram

Note: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Z86L78

IR/LOW VOLTAGE MICROCONTROLLER

FEATURES

Part	ROM (Kbytes)	RAM* (Bytes)	I/O	Voltage Range
Z86L78	16	493	16	2.0V to 3.9V

Note: *General-Purpose

- Low Power Consumption: 40 mW (Typical)
- Three Standby Modes (Typical)
  - STOP - 2 μA
  - HALT - 0.8 mA
  - Low Voltage ($<V_{Lv}$)
- Programmable Watch-Dog/Power-On Reset Circuits
- All Digital Inputs are CMOS Levels
- Five Priority Interrupts
  - Three External
  - Two Assigned to Counter/Timers
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC (Mask Selectable), or External Clock Drive
- Mask Selectable Option to Enable 32 kHz Crystal Operation
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Mask-Selectable 200 kOhm Pull-Ups on Ports 0, 2, 3:
  - All Eight Port 2 Bits Individually Selected
  - Pull-Ups Automatically Disabled Upon Selecting an Output.

GENERAL DESCRIPTION

Zilog's Z86L78 is a low-voltage microcontroller a member of the IR (Infrared) Family with 16 Kbytes of ROM and 493 bytes of general-purpose RAM. Manufactured in CMOS technology and offered in 20-pin DIP or SOIC styles packages, this low cost, low power consumption ROM-based device offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion.

The Z86L78 architecture is based on Zilog's 8-bit microcontroller core, with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z86L78 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

For applications demanding powerful I/O capabilities, the Z86L78 provides 16 pins dedicated to input and output. These lines are grouped into three ports, which are configurable under software control to provide timing, status signals and parallel I/O.

There are fouμr basic address spaces are available to support a wide range of configurations: Program Memory, Register File, Expanded Register File, and Extended Data

GENERAL DESCRIPTION (Continued)

RAM. The Register File is composed of 256 bytes of RAM, and it includes four I/O port registers, 16 control and status registers and the rest are General-Purpose registers. The Extended Data RAM adds 256 bytes of usable general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the system from coping with real-time tasks, such as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86L78 offers an innovative intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Additionally, the Z86L78 features a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

Notes: Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	VCC	VDD
Ground	GND	VSS

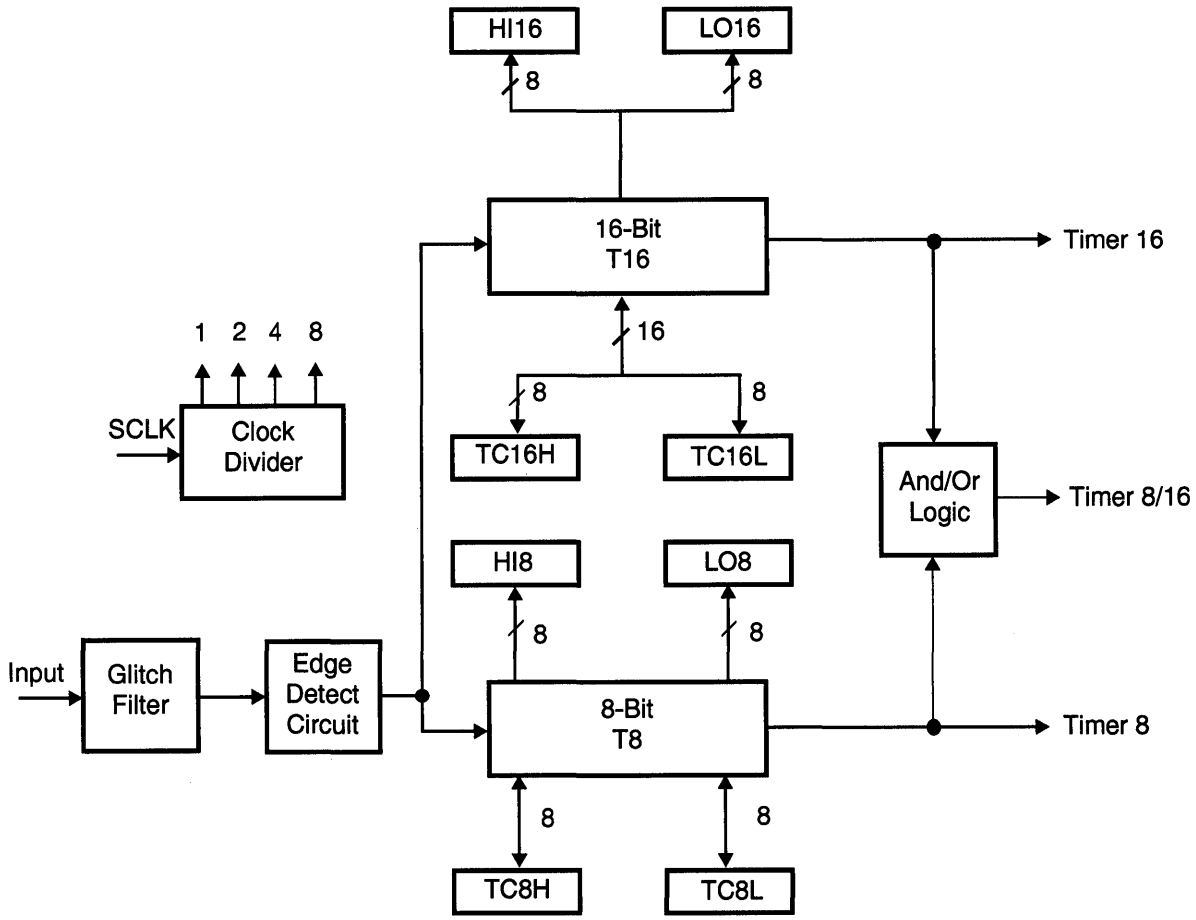


Figure 1. Counter/Timer Block Diagram

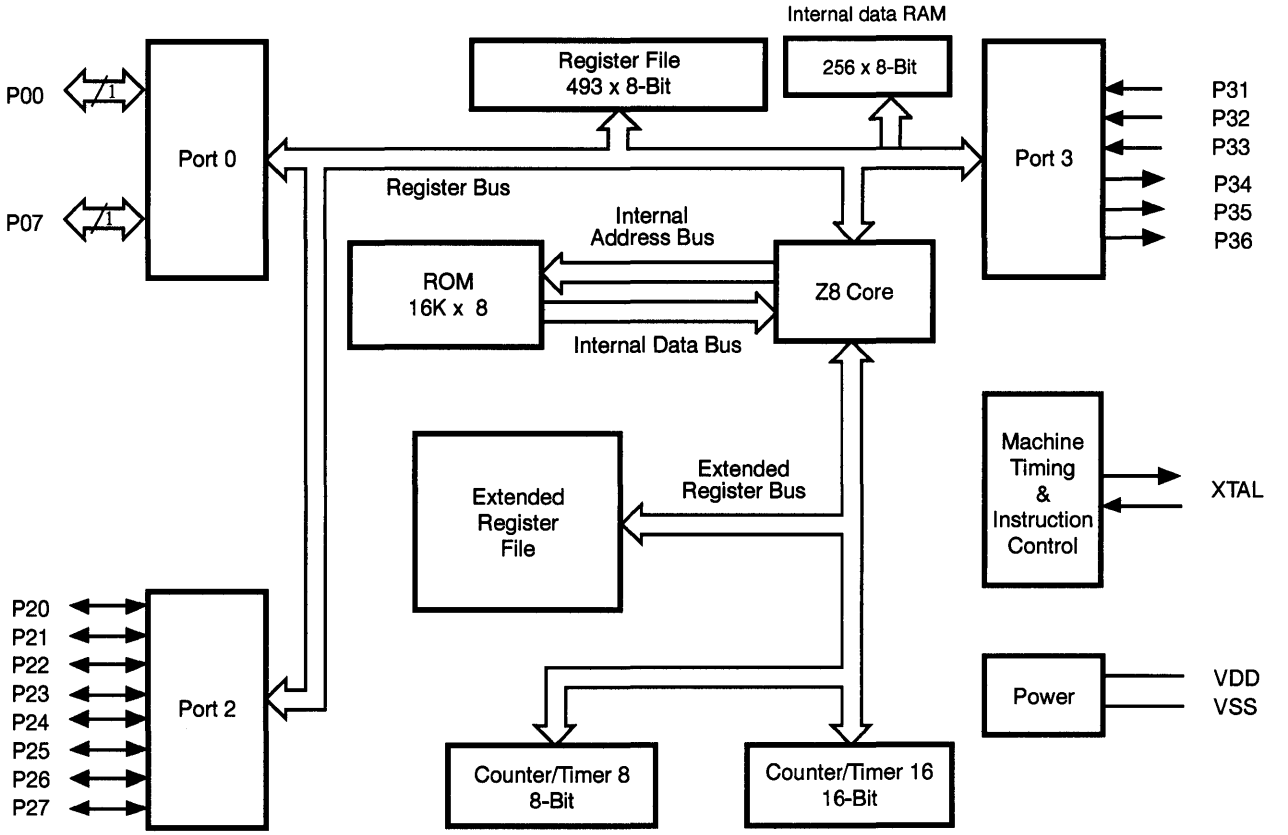


Figure 2. Functional Block Diagram

Z86L79/80

IR/LOW-VOLTAGE MICROCONTROLLER

FEATURES

Part	ROM (Kbytes)	RAM* (Bytes)	I/O	Voltage Range
Z86L79	4	237	24	2.0V to 3.9V
Z86L80	8	237	24	2.0V to 3.9V

Note: *General-Purpose

- Three Standby Modes (Typical)
  - STOP - 2 µA
  - HALT - 0.8 mA
  - Low Voltage Standby ($<V_{LV}$)
- Expanded Register File Control Registers
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
- One Programmable 8-Bit Counter/Timer with Two Capture Registers
- One Programmable 16-Bit Counter/Timer with One Capture Register
- Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
- Low Voltage Detection and Standby Mode
- Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- Mask Selectable 200 kOhms Pull-Ups on Ports 0, 2, 3
- Pull-Ups Automatically Disabled Upon Selecting Individual Pins as Outputs.
- Maskable SingleTrip Point Inputs on P00 Through P03.
- Permanently Enabled WDT Option (Maskable)

GENERAL DESCRIPTION

The Z86L79/L80 family of IR (Infrared) Controllers are ROM-based members of the Z8® single-chip microcontroller family with 256 bytes of general-purpose RAM. The only differentiating factor between these two versions is the availability of ROM. Zilog's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86L7X architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

GENERAL DESCRIPTION (Continued)

CCP™ applications demand powerful I/O capabilities. The Z86L79/80 fulfills this with two package options in which 24 pins of dedicated input and output. These lines are grouped into three ports. Each port consists of eight lines and is configurable under software control to provide timing, status signals, and parallel I/O.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File, and Expanded Register File. The Register File is composed of 256 bytes of RAM. It includes four I/O port registers, ten control and status registers, and the rest are general purpose registers. The Expanded Register File consists of three register groups.

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86L7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

Notes: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

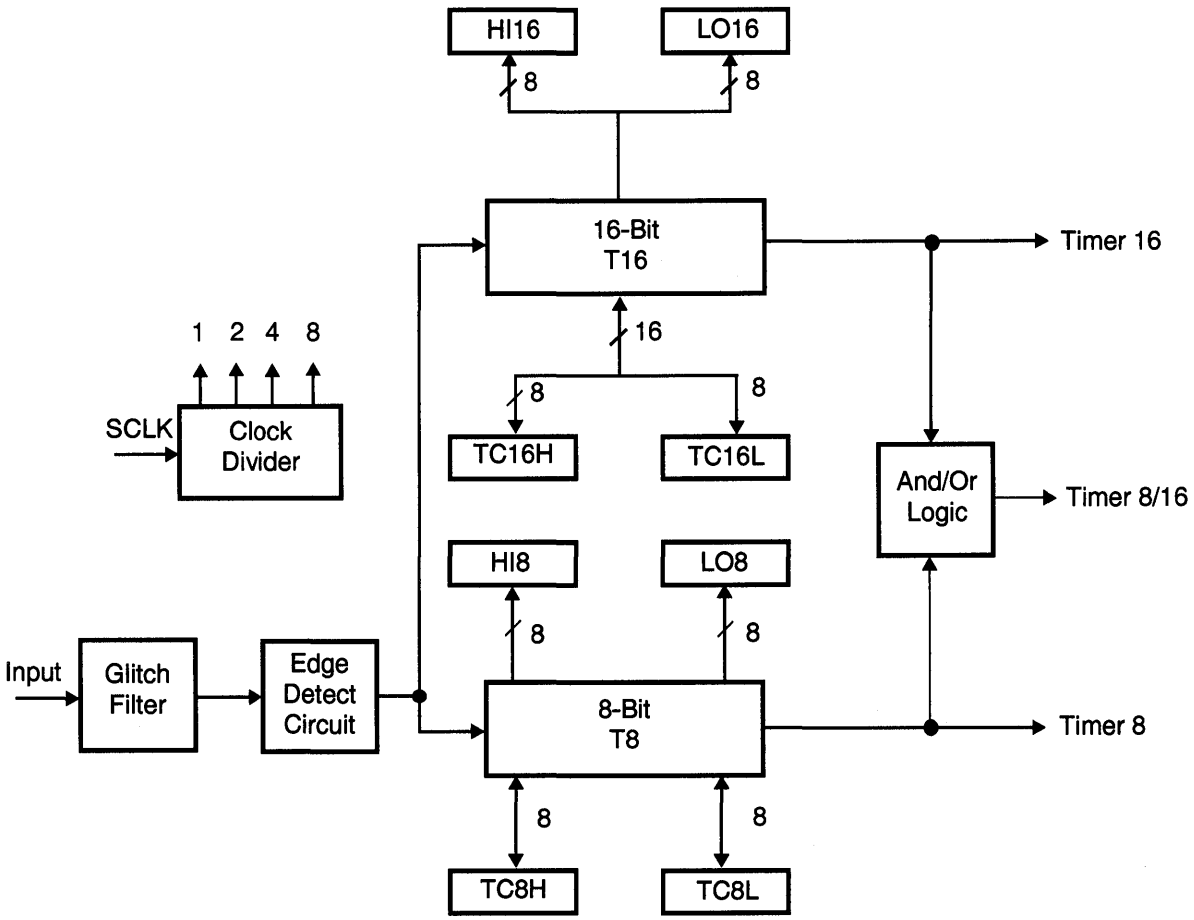


Figure 1. Counter/Timer Block Diagram

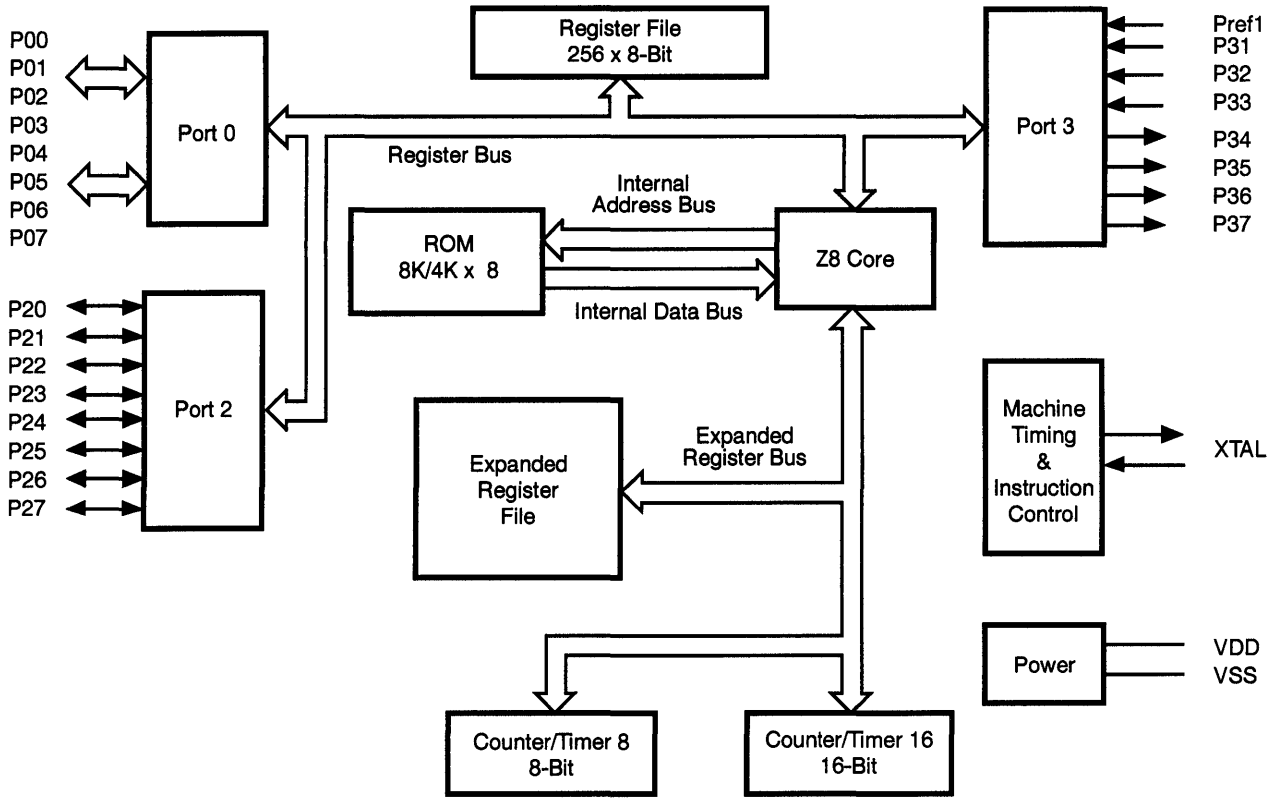


Figure 2. Functional Block Diagram

Z86L88/81/86/87/89/73

IR/LOW-VOLTAGE MICROCONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86L88	16	237	23	2.0V to 3.9V
Z86L81	24	237	23	2.0V to 3.9V
Z86L86	32	237	23	2.0V to 3.9V
Z86L87	16	236	32	2.0V to 3.9V
Z86L89	24	236	32	2.0V to 3.9V
Z86L73	32	236	32	2.0V to 3.9V

Note: *General-Purpose

- Low Power Consumption - 40 mW (Typical)
- Three Standby Modes
  - STOP
  - HALT
  - Low Voltage
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One 16-Bit Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
  - Three External
  - Two Assigned to Counter/Timers
- Low Voltage Detection and Standby Mode
- Programmable Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC (Mask Option), or External Clock Drive
- Mask Selectable 200 kOhms Pull-Ups on Ports 0, 2, 3
  - All Eight Port 2 Bits at One Time or Not
  - Pull-Ups Automatically Disabled Upon Selecting Individual Pins as Outputs.
- Maskable Mouse/Trackball Interface on P00 Through P03.
- 32 kHz Oscillator Mask Option

GENERAL DESCRIPTION

The Z86LXX family of IR (Infrared) CCP™ (Consumer Controller Processor) Controllers are ROM/ROMless-based members of the Z8® single-chip microcontroller family with 256 bytes of internal RAM. The differentiating factor between these devices is the availability of ROM, and package options. For the 40 and 44-pin devices the use of external memory enables these Z8 microcontrollers to be used where code flexibility is required. Zilog's CMOS microcontrollers offers fast executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up resistors. The Z86LXX product line offers easy hardware/software system expansion cost-effective and low power consumption.

The Z86LXX architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many

GENERAL DESCRIPTION (Continued)

consumer, automotive, computer peripheral, and battery operated hand-held applications.

There are four basic address spaces available to support a wide range of configurations: Program Memory, Register File, Expanded Register File, and External Memory. The register file is composed of 256 bytes of RAM. It includes four I/O port registers, 16 control and status registers and the rest are General Purpose registers. The Expanded Register File consists of two additional register groups (F and D). External Memory is not available on 28-pin versions.

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86LXX family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

Notes: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

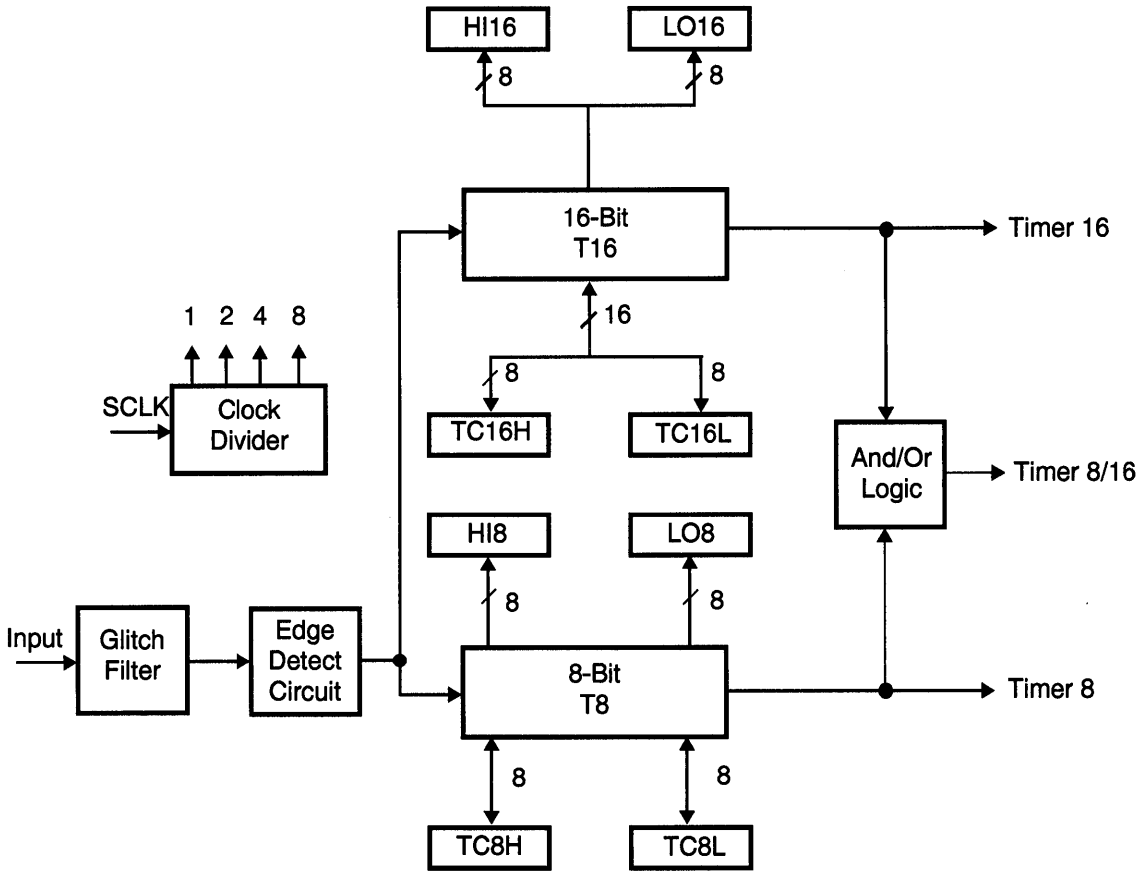


Figure 1. Counter/Timers Diagram

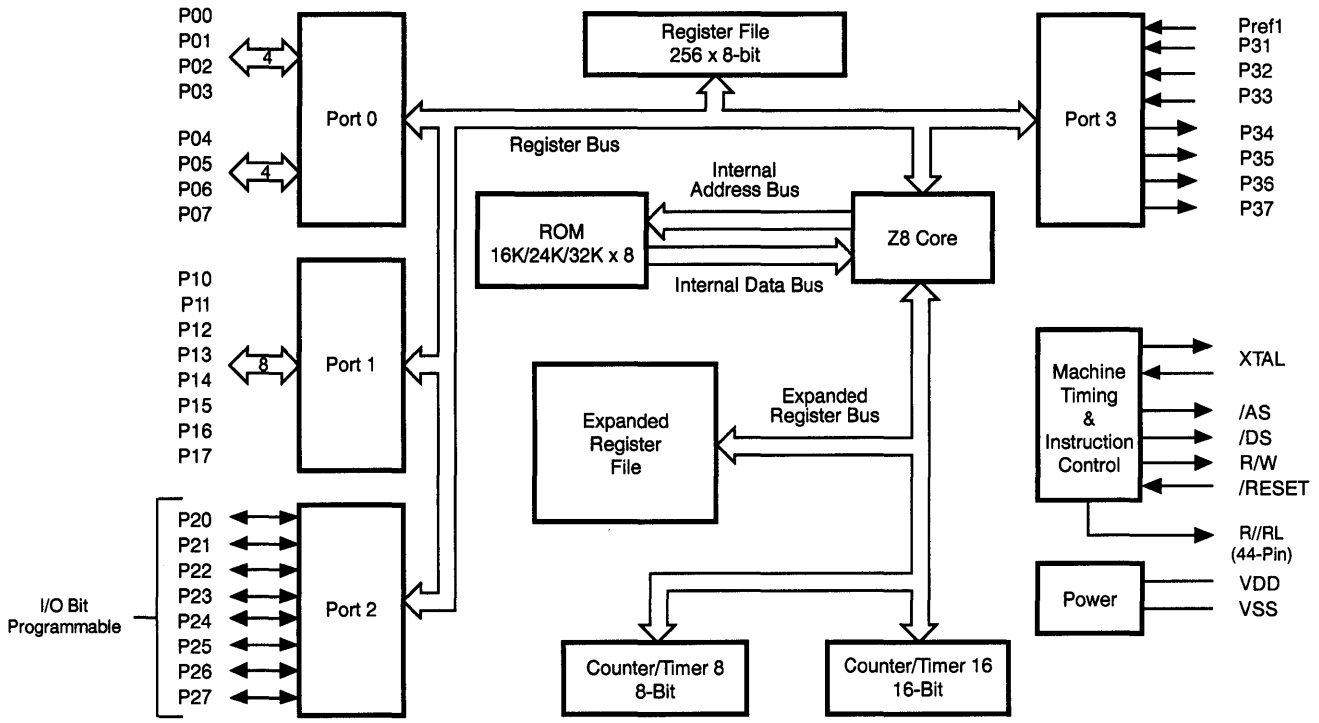


Figure 2. Functional Block Diagram

Z86L7100ZDB

ICEBOX™ EMULATOR BOARD

DESCRIPTION

The Z86L7100ZDB is a member of Zilog's ICEBOX™ Emulator product family of daughter boards. The board provides emulation for Zilog's ZIRC microcontroller family. This includes all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware and/or software product.

Utilizing the daughter board stand-alone operation with a plug-in EPROM may be done.

Supported Devices

Z86L70, Z86L71, Z86L72, Z86E72

Specifications

Emulation Specification

Maximum Emulation Speed: 16 MHz

Power Requirements

+5 Vdc @ 1.5 A

Dimensions

Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

KIT CONTENTS

Z86L71 Emulation Daughter Board

Z86C5020GSE Z8® ICE Chip
Three EPM5128 EPLD
2K x 8 STATIC RAM
40-PIN ZIF OTP Socket
80/40-Pin Target Connector
100-Pin HP-16500 Interface Board Connector

Cables

12", 20-Pin DIP Emulation Cable

Documentation

Z8 ICEBOX User Manual
Z86L7X User Manual Supplement
Z8 Cross Assembler User's Guide
MOBJ Link/Loader User's Guide
Registration Card

Ordering Information

Part Number: Z86L7100ZDB

SUPPORT PRODUCT

Z86L7102ZEM

Z8® ICEBOX™ INFRARED REMOTE CONTROLLER FAMILY EMULATOR

FEATURES

- Supported Devices

Packages	Emulation	Programming
18-Pin DIP/SOIC	N/A	N/A
20-Pin DIP	Z86L71/L78	N/A
20-Pin SOIC	N/A	N/A
40-Pin DIP	Z86L72/E72 Z86L73/E73 Z86L76/L77	Z86E72/E73*
44-Pin PLCC	Z86L72/E72 Z86L73/E73 Z86L76/L77	Z86E72/E73*
44-Pin QFP	N/A	Z86E72/E73*
64-Pin DIP	N/A	Z86E74**
68-Pin PLCC	N/A	Z86E74**
28-Pin DIP	Z86L79/L80*	

- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Window-Based User Interface
- RS-232 Connector
- Z8 GUI Emulator Software
- ICE Pod Connector for Emulation
- HP-16500 Logic Analysis System Interface Connector

Notes:
*Adapter included.
** With optional separately purchased adapter, Z86E7401ZDP.

GENERAL DESCRIPTION

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The Z86L7102ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the Z86L7X family of infrared remote controllers.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering and program debugging are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z86L7102ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5 VDC, ± 5%
Minimum Emulation Speed: 200 KHz
Maximum Emulation Speed: 16 MHz *

Notes:* 1) A software workaround is required for emulation above 12 MHz. 2) Emulator is shipped with 8 MHz crystal.

Power Requirements

+5 VDC @ 1.5A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z86L7X Emulator

- Emulation Base Board Includes:
  - CMOS Z86C9320PSC
  - 8K x 8 EPROM (Programmed with Debug Monitor)
  - 32K x 8 Static RAM
  - Three 64 x 4 Static RAM
  - RS-232C Interface
  - Reset Switch

- Z86L7X Emulation Daughterboard Includes:
  - Z86C5020GSE ICE Chip
  - 32K x 8 Static RAM
  - 40-Pin DIP Zero Insertion Force (ZIF) Programming Socket
  - 40/80-Pin Target Connectors
  - 100-Pin HP-16500A Logic Analysis System Interface Connector
  - Reset Switch

Z86E73 Program Adapter Board Z86L79/80 Emulation Pod

Cables/Pods

Power Cable with Banana Plugs
DB25 RS-232C Cable
20-Pin DIP Emulation Cable
40-Pin DIP Emulation Cable
44-Pin PLCC Pod

Host Software

Z8® GUI Emulator Software
ZASM Cross-Assembler/ MOBJ Object File Utilities

LIMITATIONS

1. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

3. Switching ICEBOXes without quitting the GUI is not supported.

4. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

5. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

   ```
   000C    SRP    #%0
   000E    LD     R4, #%0016
   0010    LD     R5, @R4
   0012    NOP
   0013    JP     %000C
   0016    NOP
   ```

   Setting the breakpoint at %0016 and click GO.

   Result: The code will break and stop at %0012.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

6. If the emulator is running a user code at full speed and the port window is opened: Switching to another application or minimizing the GUI (then restoring) will result in the following ICEBOX Communications Error message: "Emulator rejected command: target program is executing." This message may need to be cleared several times (as many as seven) before the GUI returns to normal operation.

   Workaround: Always close the port window before leaving the GUI.

7. Do not put breakpoint at address after Stop instruction. This will cause program counter to continue at that location after a Stop-Mode Recovery.

8. RC Oscillator Emulation is not supported.

9. Port 1 can only be written. The data in Port 1 cannot be read from Port 1 directly, but it can be read from Register %03 in Expanded Register Group D.

10. The L71 ICEBOX uses the Z86C50 ICE Chip; therefore, emulation at more than 12 MHz requires that the Expanded Register file timing of the ICE Chip be slowed to SCLK x 2. This is accomplished by loading value %01 to ICECON Register (Bank F, Register A) of the ICE Chip.
Example:
PUSH RP
LD RP, #%0F
LD %A, #%01
POP RP

11. The emulator uses the C50 ICE Chip; therefore, port 1 cannot be configured to Low EMI mode. (Bit 4 in PCON registers must be set to logic "1".)
Note: This condition is not present with the actual emulated device.

PRECAUTIONS

All Devices

1. All Z8® control registers are Write-Only unless stated otherwise.

2. Programming the ROM protect bit on all Z8s and Z8 OTPs will disable all use of the LDC, LDCI, LDE, and LDEI instructions. Thus ROM protect does not support the use of a ROM look-up table. The value must be loaded as "immediate values."

3. The special OTP programming options such as ROM protect, RAM protect, Low Noise, and RC will be programmed if the option has been selected and the VERIFY command was then executed.

4. Power Supply ramp-up/rise time must be such that when minimum power on reset time (T_{POR}) expires then the V_{cc} must be in the supported specified operating range of the device.

5. Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the Z86C50 ICE chip specifications.

6. The general-purpose registers (GPRs) after Power-On Reset or at initial emulator use will be different than the actual device. The emulator self test will always leave the same values in the GPRs, while the real device will have a random/undefined value in the GPRs.

7. The Port 3 Mode Register (R247 P3M) bit D1 must be set as follows:
0 = Digital Mode
1 = Analog Mode

8. The emulator cannot be operated while performing ESD/EMI testing on the target board.

9. Program Counter jumps to strange address.
a. stack not set to internal. Register %F8 (P01M Register) bit D2 not set to 1 state.
b. Stack Pointer Register %FB (SPH) and Register %FF (SPL) are not initialized. For internal stack, SPH does not have to be initialized since it is not used.
c. any instruction other than a "DI" instruction was used to disable interrupts.
d. the stack over flowed into the general register locations.
e. extra "POP", "PUSH", "IRET", or "RET" was encountered.

10. Program keeps resetting.
a. Program Counter rolled over from value "FFFF" to "0000" and proceeded back to beginning of program.
b. Watch-Dog Timer (WDT) was not refreshed.
c. single-steps more than 256 times.
d. refer to item "Precaution List—All Devices" No. 1.

11. For SMR2 Recovery Source to work correctly, Port 2 must be configured to input. (P2M Register must be written.)

12. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

13. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization must be disabled prior to invoking the VERIFY operation.

PRECAUTIONS (Continued)

14. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

15. For 386 PCs, set the baud rate to 19.2K or less because Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.

16. Do not press hardware reset when the ICEBOX is in OTP programming. If reset is pressed while the GUI is doing OTP programming, close the OTP dialog window and reopen it to reload the information back to the hardware.

    Note: Although the Command Status shows "Processing" after the GUI reestablishes the communication link when Retry was selected, the ICEBOX is actually sitting idle.)

17. There is no software option for port 3 pull-up resistor for all OTP devices when using the L71 ICEBOX.

Z86L70/71/75/78

1. The register %F8 (P01M register) bit D2 must be set to state "1".

2. WDT Register (F)%0F can only be written in the first 64 internal system clocks from the start of program execution.

3. The PCON register reserved bits for the L71 emulator must be set to "1".

4. The L71 emulator does not correctly emulate L71 ports P34 and P35 when open-drain. The C50 ICE Chip does not exhibit the same behavior when the P3M Control Register is programmed.

Z86L72/73/76/77 and Z86E72/73

1. WDT Register (F) %0F can only be written in the first 64 internal system clocks from the start of program execution.

2. Reg (F) %00 PCON has D2 controlling the open-drain for Port 0 and D1 controlling the open-drain for Port 1.

Z86L73/77 and Z86E73

1. The device has 256 bytes of internal register and 768 bytes of internal data memory (%FD00 to %FFFF). The emulator has 256 bytes of internal register and 1 Kbytes of internal data memory (%FC00 to %FFFF).

Z86L72/76 and E72

1. The device has 256 bytes of internal register and 512 bytes of internal data memory (%FE00 to %FFFF). The emulator has 256 bytes of internal register and 512 bytes of internal data memory (%FE00 to %FFFF).

Z86L79/L80

1. The Register %F8 (P01M) Bit D2 must be set to State 1.

2. WDT Register (F)%0F can only be written in the first 64 internal system clocks from the start of program execution.

Z86L71

1. When the emulator is set up to allow the analog comparators to output their value on P34, and one writes to port 0, P34 stops following the comparator input.

2. The L71 emulator does not correctly emulate L71 ports P34 and P35 when open-drain. The C50 ICE Chip does exhibit the same behavior when the P3M Control Register is programmed.

Z86L7200TSC

Z86L72 EMULATION MODULE

DESCRIPTION

The Z86L72 Emulation Module can be used like an OTP for plug-in emulation of the Z86L71/70 chip family in users' target applications. It uses external EPROM for Z8® codes to provide immediate software verification, with nearly identical electrical characteristics.

Users can develop and debug Z8 applications code using the Z86L72 toolbox software, and a Z86L7100ZEM emulator, then transfer the code to EPROMs for final testing with the Z86L7200TSC Emulation Module. The module can also be used in conjunction with one or more ROM emulators.

Supported Devices

Z86L71, Z86L70
(P00 and P07 not fully supported on L71)

Specifications

Power Requirements
+5Vdc @ 300 mA (from target board)

Dimensions
Width: 1.9 inches
Length: 1.8 inches

KIT CONTENTS

Z86L72 Emulation Module

20-Pin DIP Plug Block (use first 18 for L70)
(to insert in users target board)
One 28-Pin Socket
(for 85 nsec EPROM for Z8 code)

Documentation
Z86L7100ZEM User Instructions
Z86L7200TSC Schematics

Z86L7900ZDP

Z86L79/L80 EMULATOR ADAPTER KIT

FEATURES

- Supported Devices

Part	Packages	Speed (MHz)
Z86L79	28-Pin DIP	8
Z86L80	28-Pin DIP	8

- Cost-Effective Emulator Solution
- Allows Use of Existing Emulator
- Emulation Converter

GENERAL DESCRIPTION

The Z86L79/L80 emulation adapter kit is specifically designed to enable Zilog's L71ICEBOX™ to emulate the 28-Pin DIP Z86L79/L80 devices.

The kit is a cost-effective cable assembly allowing the use of an existing emulator.

SPECIFICATIONS

Operating Conditions

Not Applicable

Power Requirements

Not Applicable

Dimensions

Width: 0.800 in.
Length: 2.75 in.

KIT CONTENTS

Z86L79 Adapter Kit Includes:
Z86L7900ZDP Cable Assembly for Z86L71 ICEBOX

Documentation

Z86L79/L80 User's Guide

ZiLOG

8-Bit Microcontrollers

Z8® Microcontrollers 1

IR Remote Controllers 2

Computer Peripheral Controllers

Keyboard /Input Devices 3

Mass Storage 4

PCMCIA 5

DSP (Digital Signal Processors)

Television/Cable/Satellite/Set-Top Boxes 6

Voice Processors 7

DSP Cores 8

Z08602

KEYBOARD CONTROLLER (KBC™) NMOS Z8® 8-BIT MCU

GENERAL DESCRIPTION

The Z8602 Keyboard Controller (KBC™) introduces a new level of sophistication to single-chip architecture. The Z8602 is a member of the Z8 single-chip microcontroller family with 2 Kbytes of ROM.

The Z8602 KBC is housed in a 40-lead DIP, and is manufactured in NMOS technology. Zilog's microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupt, input/output bit-manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The KBC architecture is characterized by a flexible I/O scheme, an efficient register, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The KBC fulfills this with 32-pins dedicated to input and output. These lines are grouped into four ports, each port consists of 8 lines, and are configurable under software control to provide timing, status signals, and serial or parallel I/O ports.

The Z8602 offers low EMI emission achieved by means of several modifications in the output drivers and clock circuitry of the device.

There are two basic address spaces available to support this wide range of configurations: Program Memory and 124 General-Purpose Registers.

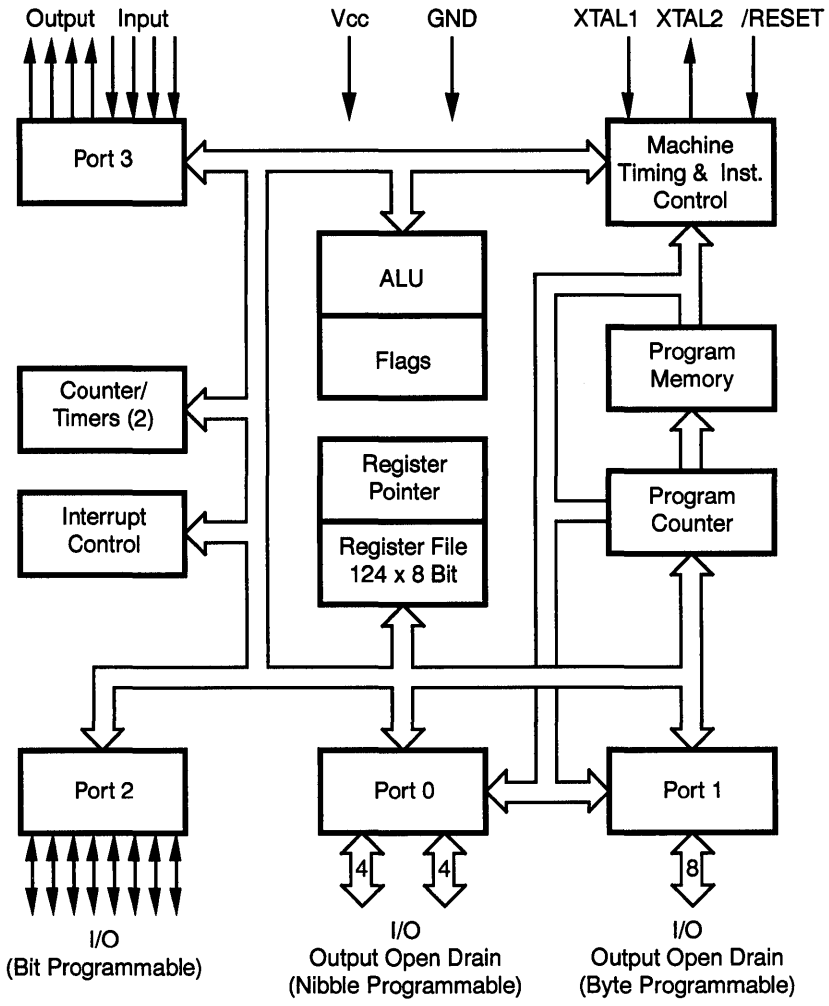
The KBC offers two on-chip counter/timers with a large number of user selectable modes. This unburdens the program from coping with real-time problems such as counting/timing.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z08614

KEYBOARD CONTROLLER (KBC™)
NMOS Z8® 8-BIT MCU

DESCRIPTION

The Z8614 Keyboard Controller (KBC™) introduces a new level of sophistication to single-chip architecture. The Z8614 is a member of the Z8 single-chip microcontroller family with 4 Kbytes of ROM.

The Z8614 KBC is housed in 40-lead DIP and 44-lead PLCC packages, and is manufactured in NMOS technology. Zilog's microcontroller offers fast execution, efficient use of memory, sophisticated interrupt, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The KBC architecture is characterized by a flexible I/O scheme, an efficient register, I/O, and a number of ancillary features that are useful in keyboard applications.

The device applications demand powerful I/O capabilities. The KBC fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports, each port consists of eight lines, and are configurable under software control to provide timing, status signals, and serial or parallel I/O ports.

The Z8614 offers low EMI emission achieved by means of several modifications in the output drivers and clock circuitry of the device.

There are two basic address spaces available to support this wide range of configurations: Program Memory and 124 General-Purpose Registers.

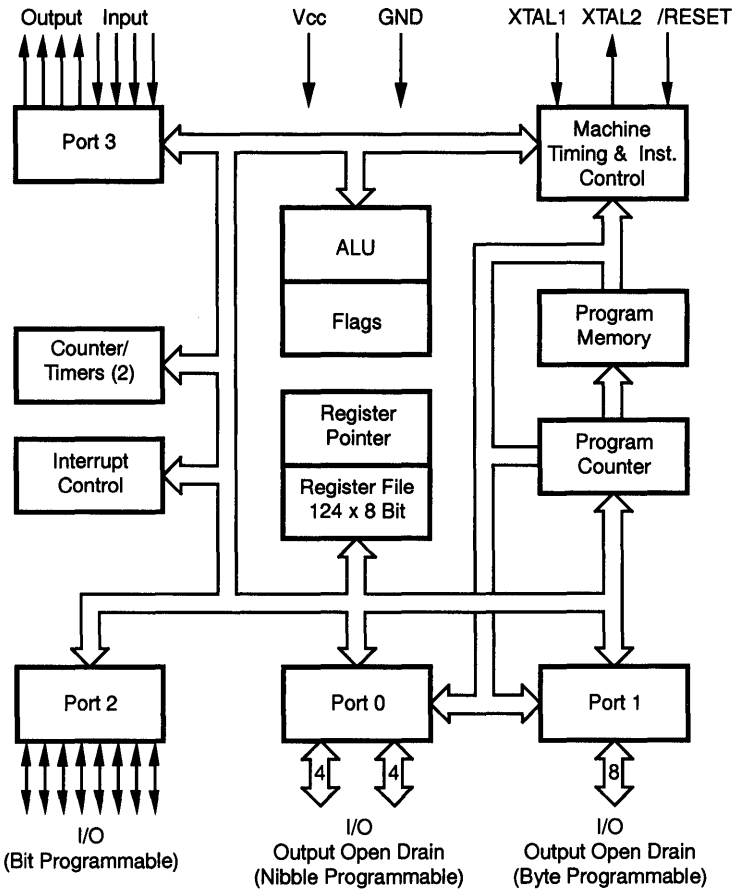
The KBC offers two on-chip counter/timers with a large number of user selectable modes. This unburdens the program from coping with real-time problems such as counting/timing.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

ZILOG

SUPPORT PRODUCT

Z08615

NMOS Z8® 8-BIT MCU KEYBOARD CONTROLLER

DESCRIPTION

The Z8615 Keyboard Controller (KBC) is a member of the Z8® single-chip microcontroller family with 4 Kbytes of ROM. The device is housed in a 40-pin DIP and 44-pin PLCC package, and is manufactured in NMOS technology. The Z8615 KBC microcontroller offers fast execution, efficient use of memory, sophisticated interrupt, input/output bit-manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z8615 KBC architecture is characterized by a flexible I/O scheme, an efficient register, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the KBC provides 32 pins dedicated to input and output. These lines are grouped into four ports, each port consists of 8 lines, and are configurable under software control to provide timing, status signals, and serial or parallel I/O ports.

The Z8615 KBC offers low EMI emission which is achieved by means of several modifications in the output drivers and clock circuitry of the device.

There are two basic address spaces which are available to support this wide range of configurations: Program Memory and 124 General-Purpose Registers.

The Z8615 KBC offers two on-chip counter/timers with a large number of user-selectable modes. This unburdens the program from coping with real-time problems such as counting/timing (Block Diagram).

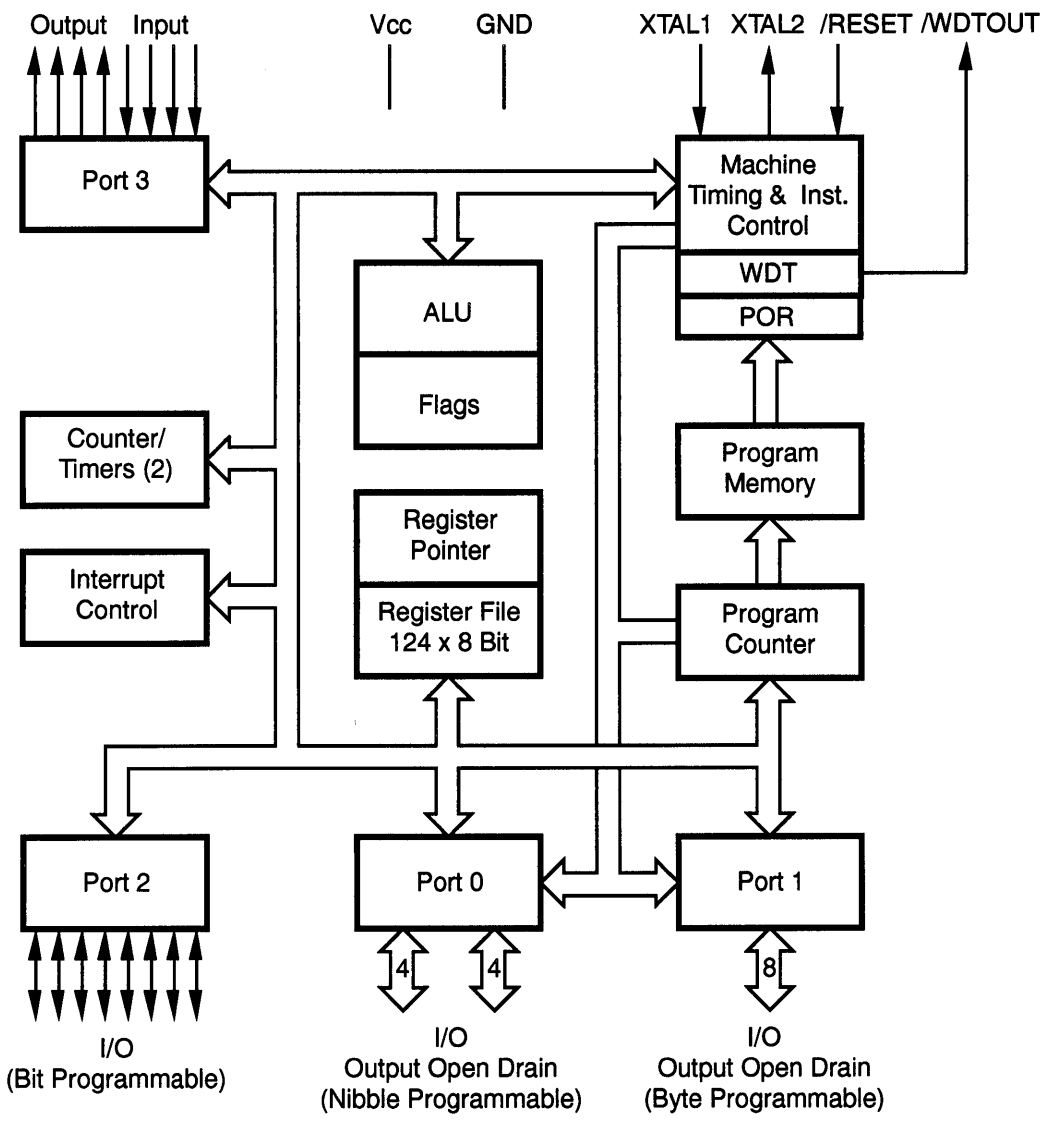
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

3

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

ZILOG

SUPPORT PRODUCT

Z08617

NMOS Z8® 8-BIT MCU KEYBOARD CONTROLLER

FEATURES

- Low Power Consumption - 750 mW
- 32 Input/Output Lines
- Digital Inputs NMOS Levels with Internal Pull-Up Resistors
- 4 Kbytes ROM
- Four Direct Connect LED Drive Pins
- 124 Bytes of RAM
- Hardware Watch-Dog Timer (WDT)
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- On-Chip RC Oscillator
- Clock Frequency: Up to 5MHz
- Low EMI Emission

3

GENERAL DESCRIPTION

The Z08617 Keyboard Controller is a member of the Z8® single-chip microcontroller family with 4 Kbytes of ROM. The device is housed in a 40-pin DIP package, and is manufactured in NMOS technology. The Z08617 microcontroller offers fast execution, efficient use of memory, sophisticated interrupt, input/output bit-manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z08617 architecture is characterized by a flexible I/O scheme, an efficient register, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z08617 provides 32 pins dedicated to input and output. These lines are grouped into four ports, each port consists of 8 lines, and are configurable under software control to provide timing, status signals, and serial or parallel I/O ports.

The Z08617 offers low EMI emission which is achieved by means of several modifications in the output drivers and clock circuitry of the device.

There are two basic address spaces which are available to support this wide range of configurations: Program Memory and 124 General-Purpose Registers.

The Z08617 offers two on-chip counter/timers with a large number of user-selectable modes. This unburdens the program from coping with real-time problems such as counting/timing (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

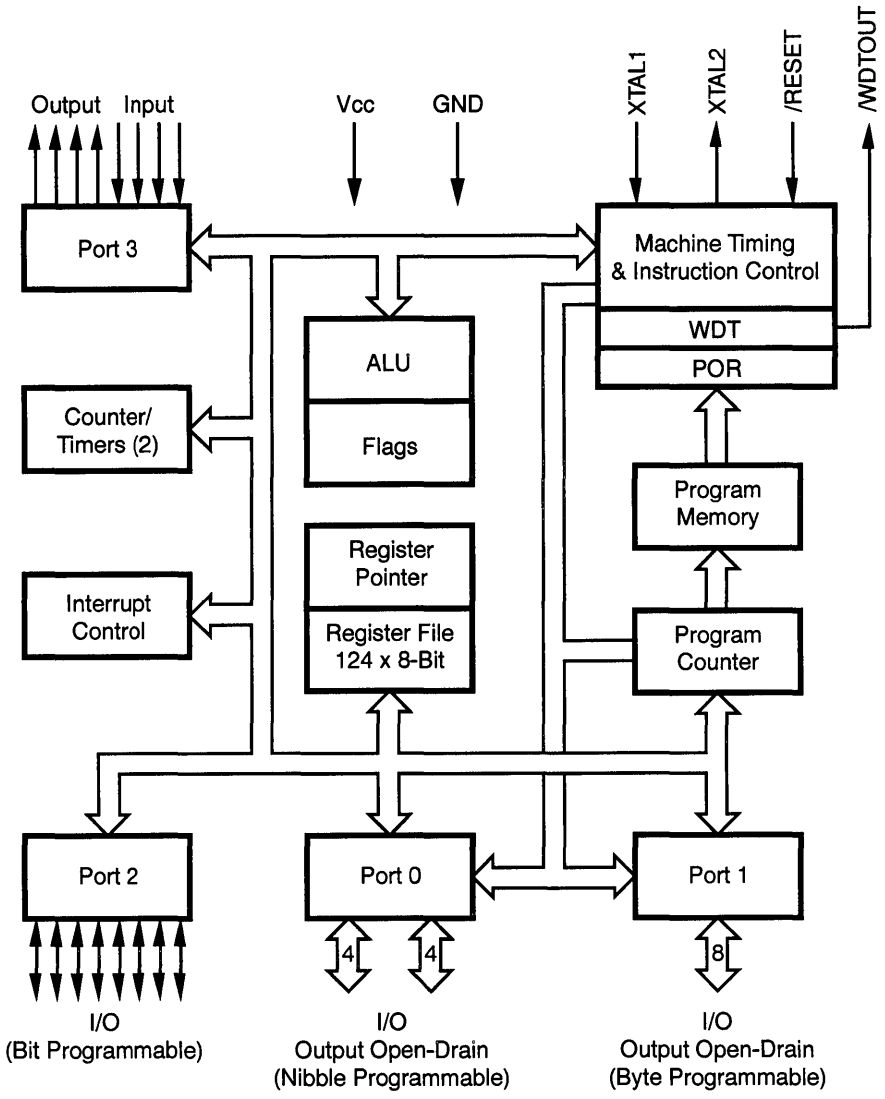


Figure 1. Z08617 Functional Block Diagram

Z86217/C17

CMOS Z8® 8-BIT MICROCONTROLLERS (POINTING DEVICE/TRACKBALL)

FEATURES

Part Number	ROM (Kbytes)	RAM* (Bytes)	I/O Lines	Speed (MHz)
Z86217	2	124	14	4
Z86C17	2	124	14	4

* General-Purpose

- 18-Pin DIP and SOIC Packages
- 3.0- to 5.5-Volt Operating Range
- 0°C to 70°C Operating Temperature Range
- Permanent Watch-Dog Timer (WDT)
- Oscillator Filter
- Two Programmable 8-Bit Counter/Timers
- Low-EMI Operation
- Scalable Trip-Point Buffer
- On-Board Pull-Up Resistors
- High Drive Ports Can Sink 20 mA Per Pin, with Three Pins Maximum

3

GENERAL DESCRIPTION

The Z86217/C17 are members of Zilog's Z8® family of microcontrollers designed to reduce external system components and offer easy software/hardware development tools for pointing device and trackball applications.

The devices feature on-board pull-up resistors, and a scalable trip-point buffer to accommodate opto-transistor outputs. The high drive ports are capable of up to 20 mA (at V_{OL} = 0.8-volt) current sinking per pin, with three pins maximum, providing extra sinking current capability.

The Z86217/C17's permanently enabled Watch-Dog Timer (WDT) operates upon power-up of the MCU, and provides added operational reliability for pointing device and trackball environments.

An oscillator filter assists in separating out high-frequency noise from the oscillator input pin.

Two on-chip counter/timers with a large number of selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Notes:
Refer to the DC electrical characteristics for detailed specification of the sinking current.

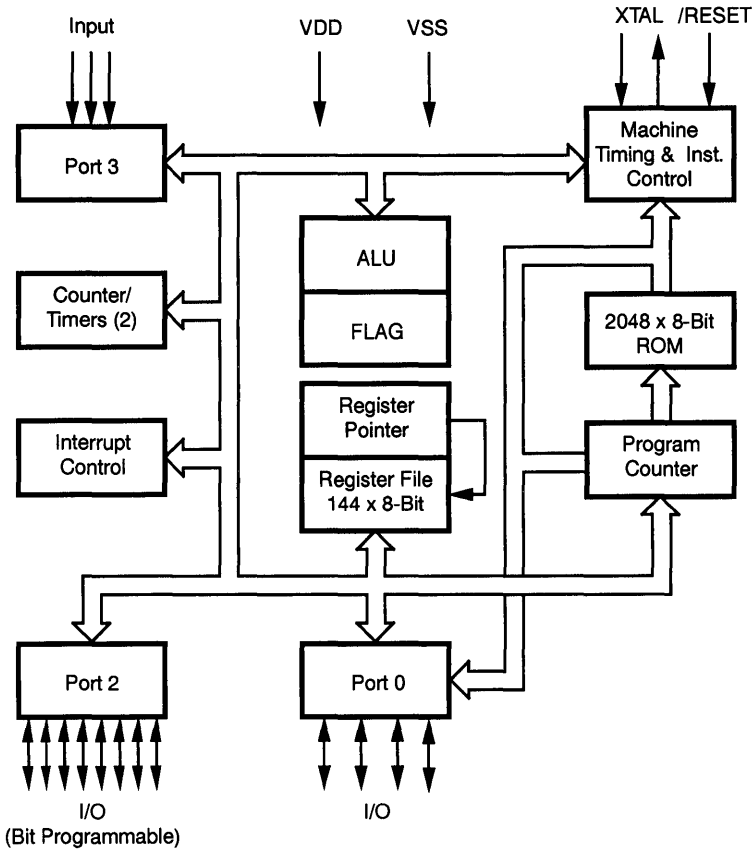
On the Z86C17, P24-P27 has a 20K pull-up, and P32 has a 47K pull-down. The Z86217 does not have these functions.

All Signals with a preceding front slash, "/", are active Low, e.g.; B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

BLOCK DIAGRAM



Functional Block Diagram

Z86317
CMOS Z8® 8-BIT MCU

FEATURES

Part Number	ROM (KB)	RAM* (Bytes)	Speed (MHz)	I/O	Package (18-Pin)
Z86317	2	124	4	13	DIP, SOIC

*General Purpose

- 4.5- to 5.5-Volt Operating Range
- 0°C to + 40°C Operating Temperature Range
- Low-Power Consumption: 33 mW (Typical)
- P24-P27 Can be Configured as a Voltage Divider During Input Mode
- On-Chip Precision RC Oscillator (Tolerance = ± 10%)
- Fast Instruction Pointer: 1.5 µs @ 4 MHz
- ESD Protection Circuitry
- Hardwired Watch-Dog Timer (WDT)

GENERAL DESCRIPTION

The Z86317 is a member of the Z8® family of CMOS microcontrollers architected to be used in mouse applications. These devices offer on-board pull-up and pull-down resistors, a scalable trip-point buffer to accommodate opto-transistor outputs, and high drive ports capable of up to 10 mA current sinking per pin (six pins maximum).

A permanently enabled Watch-Dog Timer ensures operational reliability across a broad range of mouse application environments. The precision RC oscillator filters out high-frequency noise from the oscillator input pin. When configured as inputs, P24-P27 are configured as voltage divider (25K pull-up / 7.5K pull-down). The input levels are adjusted for connection to the emitters of the opto-transistors and switch at a voltage level of 0.4 V_{DD}.

For applications requiring powerful I/O capabilities, the Z86317 provides dedicated input and output lines that are grouped into three ports. There are two basic address spaces available to support this configuration: Program Memory, and 124 bytes of general-purpose registers.

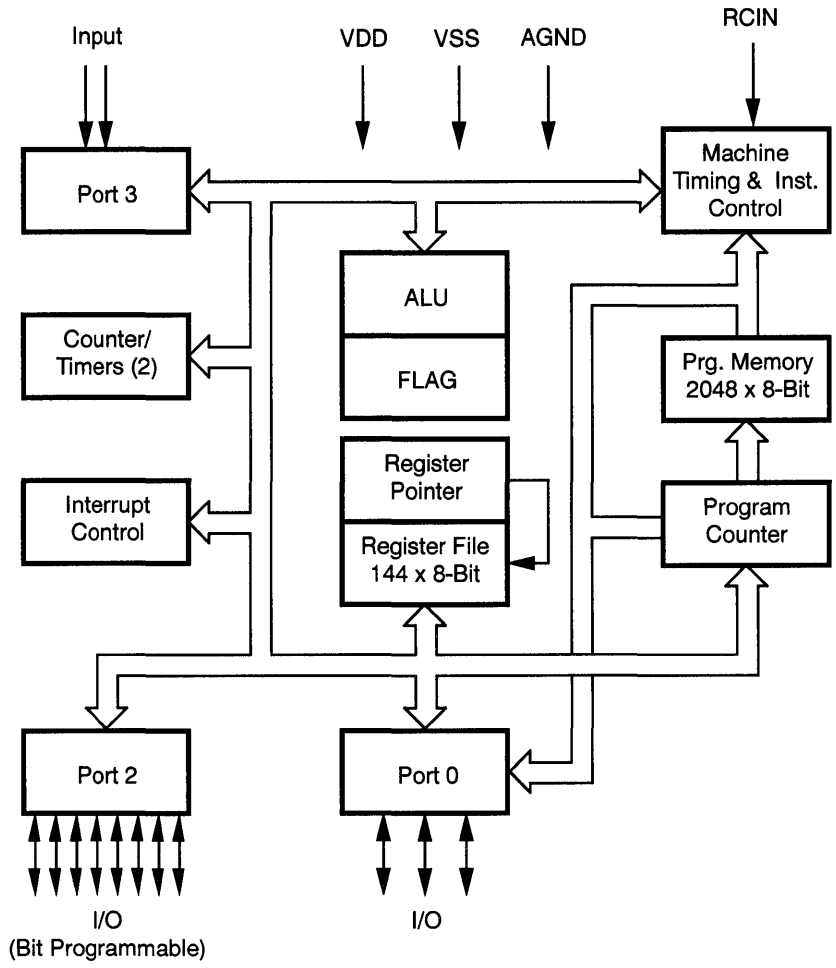
The Z86317 device provides two on-chip 8-bit programmable counter/timers with a large number of user-selectable modes. Each counter/timer is driven by its own 6-bit programmable prescaler. The Z86317 counter/timers offload system real-time tasks such as counting/timing and input/output data communications for increased system efficiency.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.; B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

BLOCK DIAGRAM



Functional Block Diagram

Z86318

Z8® MCU 8-BIT MICROCONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86318	124	14	21	0V to 6.0V

Note: *General-Purpose

- –40°C to +105°C Operating Temperature Range
- Low-Power Consumption: 33 mW (Typical)
- ROM Mask Options:
  - Permanent Watch-Dog Timer
  - ROM Protect
  - Low-Voltage Protection
  - Pull-Up/Pull-Down I/O Pins (Nibble Programmable)
  - Feedback Resistor on the On-Chip Oscillator
- On-Chip Oscillator (Crystal, Ceramic Resonator, LC, or External Clock Drive)
- Fast Instruction Pointer: 1.5 µs @ 4 MHz
- ESD Protection Circuitry

3

GENERAL DESCRIPTION

The Z86318 is a member of the Z8® MCU family of CMOS microcontrollers. This device offers on-board pull-up and pull-down resistors (ROM mask-option programmable on a nibble basis), a scalable trip-point buffer to accommodate opto-transistor outputs, and high drive ports capable of up to 20 mA current sinking per pin (3 pins maximum).

The Z86318 features I/O Ports (IOL = 20 mA at VOL = 0.8V, 3 pins max.) to provide increased current sinking capabilities. These devices also offer users a selection of ROM mask options, which include a permanently enabled Watch-Dog Timer that ensures operational reliability across a broad range of application environments.

For applications requiring powerful I/O capabilities, the Z86318 provides dedicated input and output lines that are grouped into three ports. These ports can be configured by means of ROM mask options (nibble-programmable) as pull ups, pull downs, or neither. There are two basic address spaces available. Program Memory, and 124 bytes of general-purpose registers.

The Z86318 devices provide two on-chip 8-bit programmable counter/timers with a large number of user-selectable modes. Each counter/timer is driven by its own 6-bit programmable prescaler. The Z86318 counter/timers off-load system real-time tasks such as counting/timing and input/output data communications for increased system efficiency.

Notes: All Signals with a preceding front slash, "/", are active Low, e.g.; B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	VCC	VDD
Ground	GND	VSS

GENERAL DESCRIPTION (Continued)

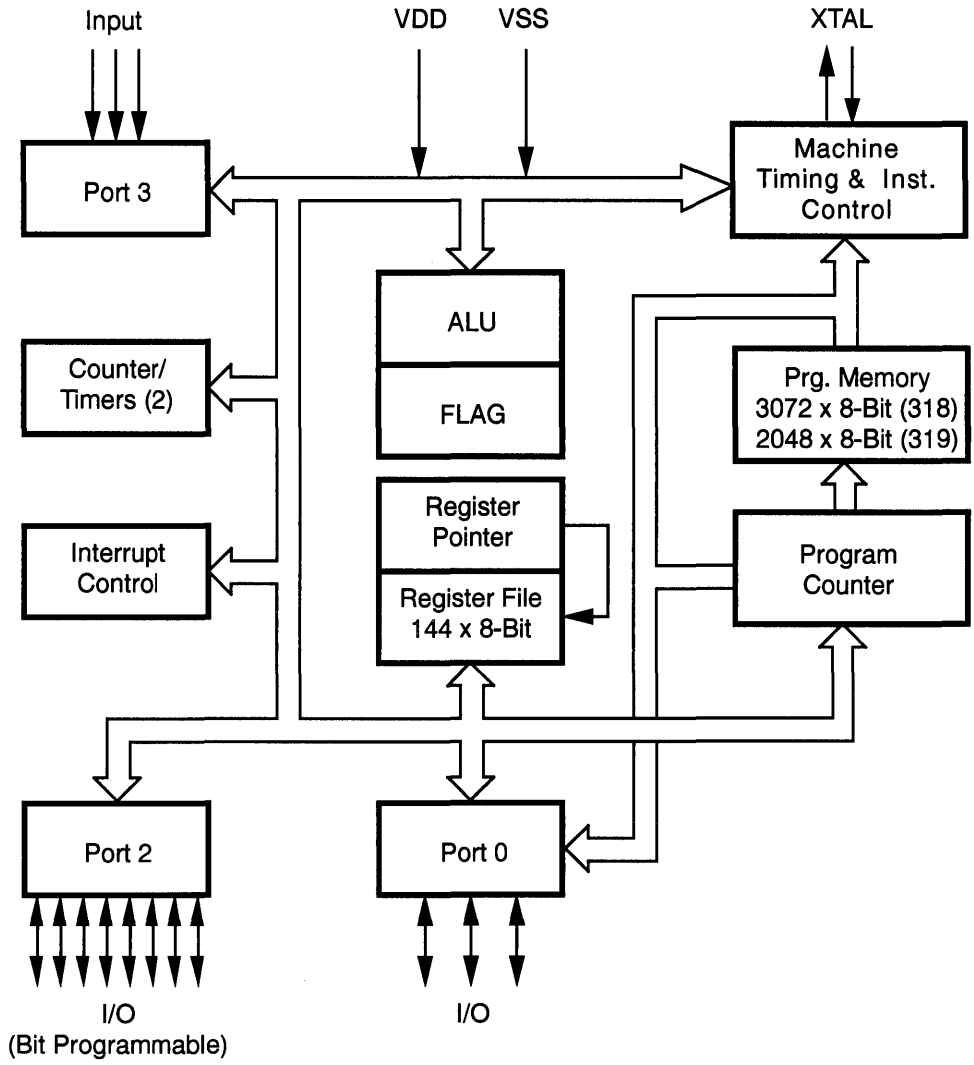


Figure 1. Z86318 Functional Block Diagram

ZiLOG

SUPPORT PRODUCT

Z86417

CMOS Z8®
TOUCH-PAD CONTROLLER

FEATURES

Part	ROM (Kbyte)	RAM* (Kbyte)	Speed (MHz)
Z86417	4	236	12

* General-Purpose

- 64-Pin QFP Package
- 4.0- to 5.5-Volt Operating Range
- Low-Power Consumption
- 0°C to +70°C Operating Range
- 45 Capacitance Change Sensing Inputs
- Dual Measurement Modes: Differential or Single Ended
- Watch-Dog Timer (WDT) and Stop Mode Recovery
- Two On-Chip Oscillators: Ceramic Resonator or External 1% Resistor
- RAM and ROM Protect
- Low-Voltage Protection and Asynchronous Reset

3

GENERAL DESCRIPTION

The Z86417 is an integrated Z8® microcontroller with capacitance sensors that allow users to develop touch-pad controls for PC peripherals. The Z86417 operates in ROMless (code development) and processorless (test and emulation) modes.

In response to the user placing and moving a finger on the sensor area, the Z86417 senses capacitance and then maps the profile from which it calculates the current finger location. By comparing this data to previous information, the programmer can infer movement. Information is reformulated into standard mouse-click data and then serially transmitted to the PC.

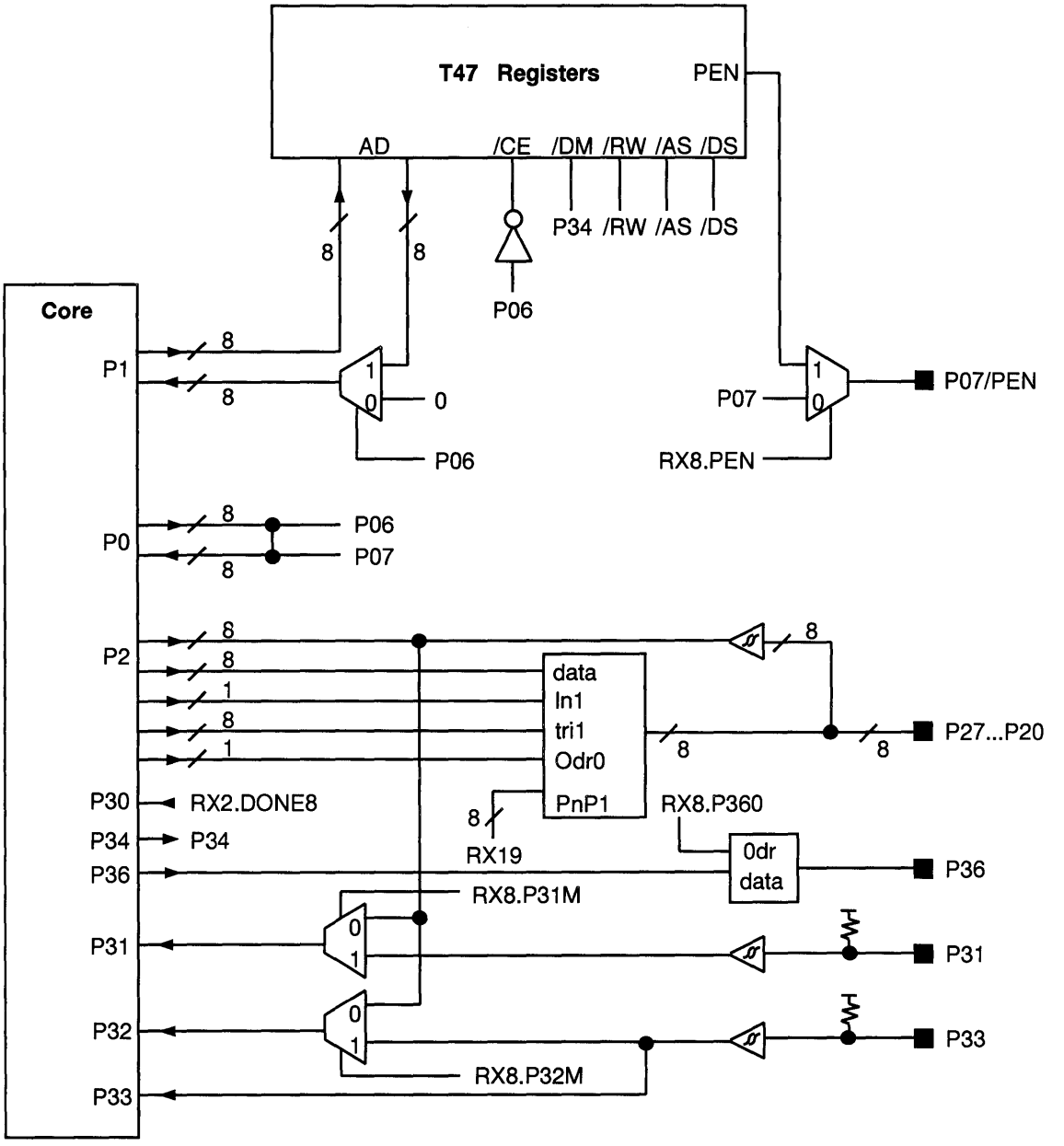
In mouse/trackball mode, the PC cannot distinguish between touch-pad movement and click data from standard mouse and trackball devices.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

ZiLOG

SUPPORT PRODUCT

Z86C15

CMOS Z8® 8-BIT MCU KEYBOARD CONTROLLER

FEATURES

ROM (Kbytes)	RAM* (Bytes)	I/O Lines	Speed (MHz)	Pin Count / Package
4	236	32	5	40 DIP 44 PLCC 44 QFP

* General-Purpose

- 4.5- to 5.5-Volt Operating Range
- 0°C to 70°C Operating Temperature Range
- Expanded Register File
- Low-Power Consumption: 30 mW @ 5 MHz Typical
- Six Vectored, Priority Interrupts from Six Different Sources
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer, Hardware Watch-Dog Timer (WDT)
- Digital Inputs CMOS Levels with Internal Pull-Up Resistors
- Four Direct Connect LED Drive Ports
- On-Chip RC Oscillator, 4 MHz to 5 MHz

3

GENERAL DESCRIPTION

The Z86C15 Keyboard Controller is a full-featured member of the Z8® microcontroller family offering a unique register-to-register architecture that avoids accumulator bottlenecks and is more code efficient than RISC processors.

For applications demanding powerful I/O capabilities, the Z86C15 provides 32 pins dedicated to input and output. These lines are grouped into four ports, each port consisting of eight lines, and are configurable under software control to provide timing, status signals, and serial or parallel I/O ports.

Two on-chip counter/timers, with a large number of user-selectable modes, are available to relieve the system of administering real-time tasks, such as counting/timing and I/O datacommunications.

Six different internal or external interrupt sources are maskable and prioritized so a vectored address is provided for efficient interrupt subroutine handling and multitasking functions.

The Z86C15 achieves low-EMI by means of several modifications in the output drivers and clock circuitry of the device.

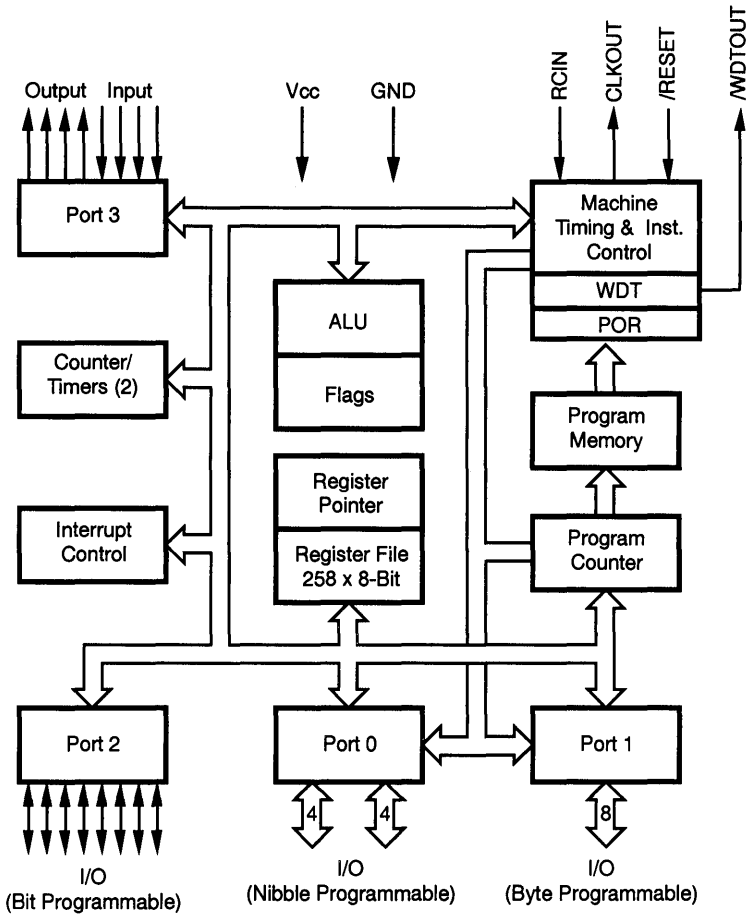
By means of an expanded register file, the designer has access to three additional system control registers that provide extra peripheral devices, I/O ports, and register addresses (see Functional Block Diagram).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Z86C15 Functional Block Diagram

Z86K13/K14/K15/ K16/K17/K18

CMOS Z8® 8-BIT MCU KEYBOARD CONTROLLERS

FEATURES

Device	ROM (KB)	I/O Lines	Speed (MHz)	Pin Count/ Package
Z86K13	2	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB
Z86K14	3	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB
Z86K15	4	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB
Z86K16	2	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB
Z86K17	3	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB
Z86K18	4	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB

- 4.5- to 5.5-Volt Operating Range
- 0°C to 70°C Operating Temperature Range
- Low-Power Consumption: 60 mW @ 5 MHz
- Five Vectored, Priority Interrupts from FIve Different Sources
- A Programmable 8-Bit Counter/Timer, with 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer, Hardware Watch-Dog Timer (WDT)
- Digital Inputs CMOS Levels with Internal Pull-Up Resistors
- Four Direct Connect LED Drive Ports
- On-Chip RC Oscillator (Z86K13/14/15)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive (Z86K16/17/18)
- Low System EMI Emission

3

GENERAL DESCRIPTION

The Z86KXX Keyboard Controllers are full-featured members of the Z8® MCU family offering a unique register-to-register architecture that avoids accumulator bottlenecks and is more code efficient than RISC processors.

For keyboard applications demanding powerful I/O capabilities, the Z86KXX provides 32 pins dedicated to input and output for row, column, clock, data, and LEDs.

The on-chip counter/timer is available to relieve the system of administering real-time tasks.

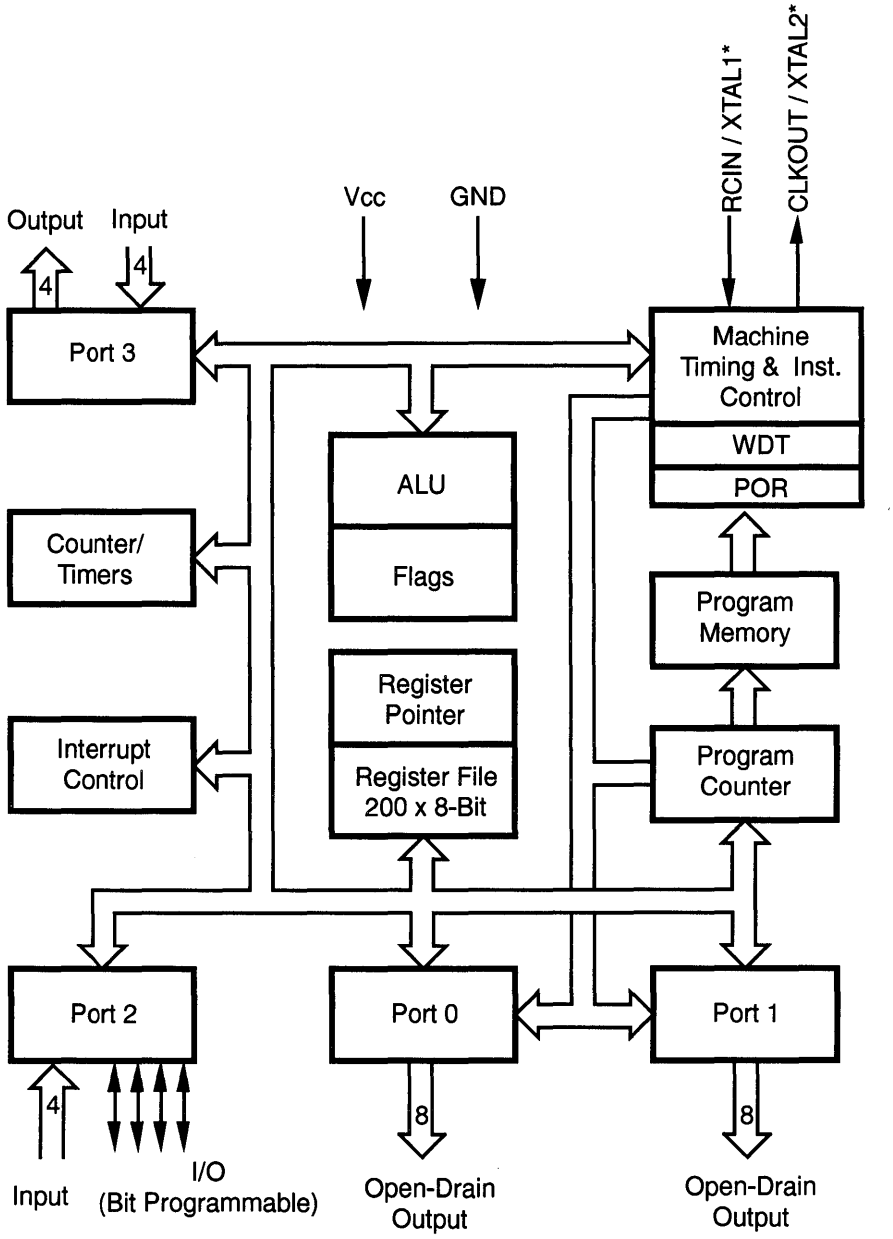
Five different internal or external interrupt sources are maskable and prioritized in which a vectored address is provided for efficient interrupt subroutine handling and multitasking functions.

The Z86K15 achieves low EMI by means of several modifications in the output drivers and clock circuitry of the device.

GENERAL DESCRIPTION (Continued)

Note: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}



Note: *Z86K16/17/18

Figure 1. Z86KXX Functional Block Diagram

Z0860200ZCO

KEYBOARD KIT

DESCRIPTION

The kit contains an assembled circuit board, Z08602 with keyboard, ROM-code, and documentation to help the user become familiar with the features of the Z08602 keyboard controller.

The Z08602 microcontroller is designed into a 101/102 PC keyboard circuit to control all scan codes, line status modes, scan timing and communication between the keyboard and PC.

SUPPORTED DEVICES

Z08602

SPECIFICATIONS

Power Requirements

+5 Vdc @ .2 A (Supplied By PC)

Dimensions

Width: 4.6 in. (11.7 cm)
Length: 9.3 in. (23.6 cm)

KIT CONTENTS

Z08602 101/102 Keyboard

NMOS Z08602 MPU
2 MHz Crystal
101/102 Keyboard Option
3 LEDs
Two 8-Position Dip Switches
6-Pin Communication Header

Software (IBM-PC Platform)

Z8/Z80/Z8000 Cross Assembler
MOBJ Link/Loader
Application Source Code available with factory approval.

Documentation

Z08602 Application Kit User Guide
Z8 Family Data Book
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ZILOG

SUPPORT PRODUCT

Z0861500ZCO

IBM PC-COMPATIBLE DEVELOPMENT KEYBOARD KIT

FEATURES

- Supported Devices

Part	Packages	Speed (MHz)
Z08615	40-Pin DIP	5
Z86C15	40-Pin DIP	5
Z86K15/K17	40-Pin DIP	5

- Platform to Develop/Evaluate Existing Keyboard Scan Code
- Standalone or Emulation Modes
- Flexible Jumper Settings
- Short Circuit Protection Circuitry
- Supports PC and PS/2 Compatible Systems

GENERAL DESCRIPTION

The Z0861500ZCO is a keyboard kit specifically designed to support Zilog's Z8® keyboard controller family by providing an assembled circuit board and documentation to help the user become familiar with the features of the Z86C15/K15.

The Z08615, Z86C15 and Z86K15 microcontrollers are designed into a 101/102 PC keyboard circuit to administer control of all scan codes, line status modes, scan timing, and communications between the keyboard and the PC.

3

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C

Power Requirements

+5 V_{DC} @ .2 A (Supplied by PC)

Dimensions

Width: 4.6 in. (11.7 cm)
Length: 9.3 in. (23.6 cm)

KIT CONTENTS

101/102 Keyboard with 6-Pin DIN Cable and PS2 Adapter

Documentation

IBM PC-Compatible Keyboard Development Kit
User's Manual
Registration Card

LIMITATIONS

1. Keys 127, 128, and 129 are not intended for standard applications and should not be used to evaluate Zilog standard code.

PRECAUTIONS

1. Turn off the host PC before connecting the keyboard development kit to the PC.

Z0861500ZDP

EMULATION ADAPTER BOARD

DESCRIPTION

The Z0861500ZDP is an adapter board tool that is used with the Z86C12 ICEBOX™. The adapter board will provide emulation for the Z8615 Keyboard MCU. The adapter board connects between the emulator and target application board through a pair of 40-pin connectors.

Supported Device

Z8615

Specifications

Power Requirements

Not Applicable

Dimensions

Width: 2.2 in. (5.6 cm)
Length: 2.4 in. (6.2 cm)

KIT CONTENTS

Z08615 Emulation Adapter Board

40-Pin Z86C12 Connector
40-Pin Z08615 Connector

Documentation

Z0861500ZDP Emulation Adapter User Guide

Z86E2300ZDP/ZDV

Z86E23 OTP ADAPTER KIT

DESCRIPTION

The Z86E23 OTP Adapter Kit allows a standard EPROM programmer to program the Z86E23 One-Time-Programmable microcontroller, and the Z86E23 Erasable-Programmable microcontroller.

KIT CONTENTS

Z86E23 Adapter Board Kit includes:

Description	Hardware Revision
Z86E2300ZDP DIP Programming Adapter	B
Z86E2300ZDV PLCC Programming Adapter	B

Z86E2301ZDP/ZDV

Z86E23 CONVERSION KIT

GENERAL DESCRIPTION

The Z86E23101ZDV Kit* converts the pin-outs of the 44-pin PLCC package to that of the 40-pin DIP package.

The Z86E2301ZDP provides the additional hardware to program the 40-pin DIP Z86E2304PSC*.

Note:
* Conversion kit is dedicated to program on Zilog's C12 ICEBOX™.

KIT CONTENTS

Z86E23 Conversion Kit includes:

Description	Hardware Revision
Z86E2301ZDV PLCC Converter	B
Z86E2301ZDP DIP Converter	B

3

ZiLOG

8-Bit Microcontrollers

Z8® Microcontrollers 1

IR Remote Controllers 2

Computer Peripheral Controllers

Keyboard /Input Devices 3

Mass Storage 4

PCMCIA 5

DSP (Digital Signal Processors)

Television/Cable/Satellite/Set-Top Boxes 6

Voice Processors 7

DSP Cores 8

Z86018
DATA PATH CONTROLLER

FEATURES

Part	ROM (Kbyte)	RAM* (Bytes)	Speed (MHz)
Z86018		124	40

*General-Purpose

- Low Profile 100-Pin Plastic VQFP
- 4.5- to 5.5-Volt Operating Range
- Low-Power Consumption
- 0°C to +70°C Temperature Range
- Programmable Power-Down Mode
- Point and Go Automatic Disk and Host Control and Transfers

GENERAL DESCRIPTION

The Z86018 single-chip data path controller is a high performance integrated device that combines the functions necessary to implement a variety of low-cost, high-performance Winchester® products. The five functions performed by this chip are: disk control and sequencing, host interface logic, local microcontroller interface, Reed-Solomon® ECC Correction, and sector buffer interface. Programmable power down modes are provided for battery operated applications.

The disk controller interface features a low overhead programmable sequencer that can be programmed to transfer a full track of data from disk to buffer with no firmware intervention. The sequencer can support all types of Winchester drives, but is especially well suited to low-power sampled, or embedded servo types of drives.

The 31x32 bit sequencer has the ability to be interrupted, save its state, execute a servo interrupt routine, and return to the interrupted instruction. The sequencer can fetch up to 1024 bytes of format specific data per track operation, to be used as format data, to load the servo interrupt counter, or as section numbers, allowing for full track reads with no firmware intervention.

Data rates of up to 34 Mbits/sec are supported through the use of high-speed, low cost CMOS technology. Data integrity through a hardware implementation of a widely used 88-bit Reed-Solomon ECC code is provided. 16-bit CRC is also supported in hardware for error detection on ID fields.

The microcontroller port provides for Intel, Motorola, National, NEC and Zilog microcontroller interfaces with no need for external chip select logic. Interrupt and status registers facilitate interrupt or polling operations. Direct microcontroller access to the buffer RAM is possible even during disk and Host data transfer.

The Z86018 provides automatic host interface control which allows for full track reads from disk to host with no microcontroller intervention. The ATA signals DRQ, BSY and IRQ14 are generated by the Z86018 in hardware allowing for the fastest possible transfers over the AT bus.

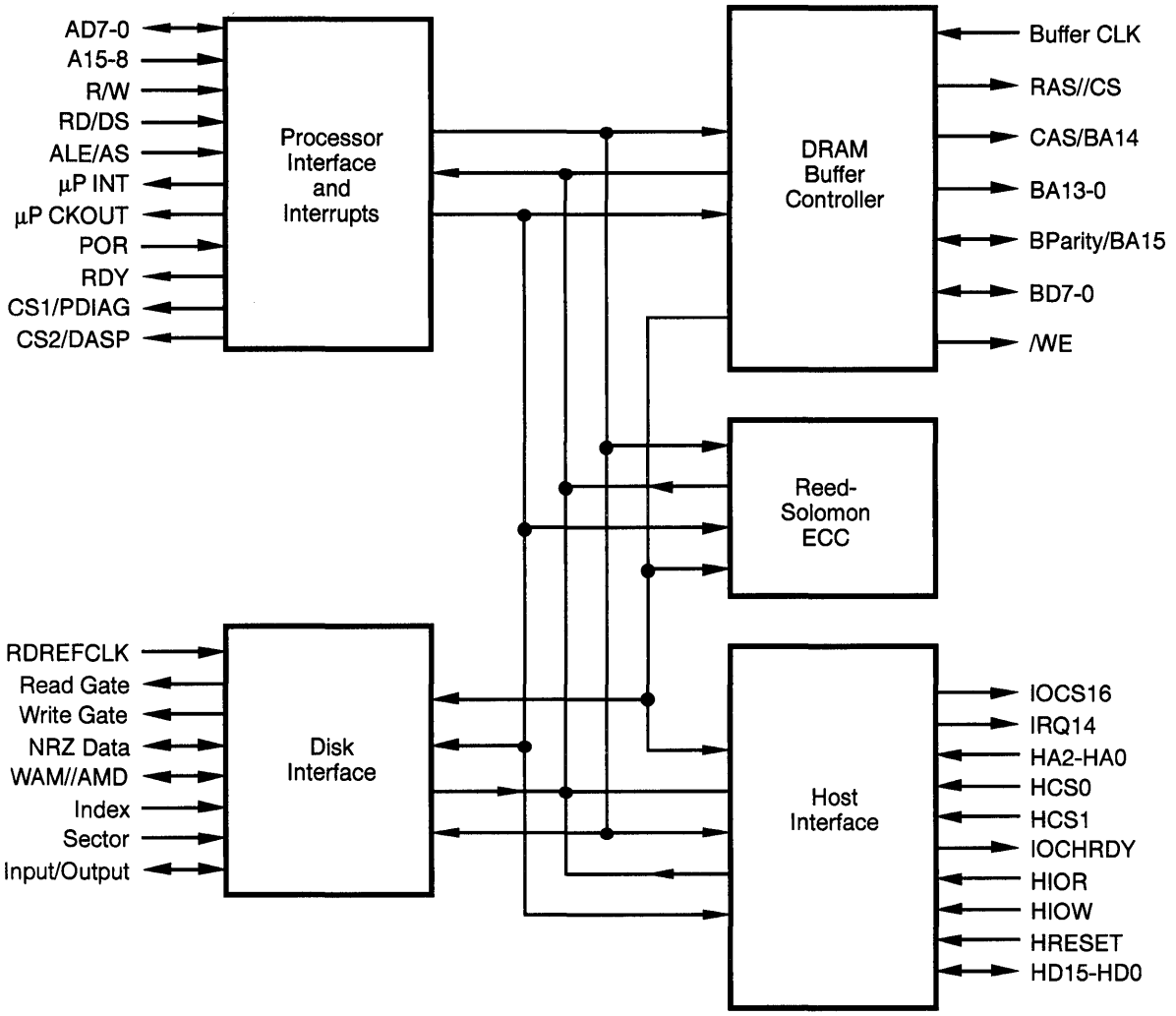
The buffer controller interface arbitrates between disk, host, Reed-Solomon ECC, microcontroller, and formatter data requests. The buffer interface directly drives up to 64K of SRAM, or 1 Mbyte of DRAM. To maximize buffer bandwidth page mode is used when accessing DRAMs. Parity generation and checking is also supported for data integrity. The buffer controller operates with an independent clock source to maximize its bandwidth.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Z86018 Functional Block Diagram

Z86193

CMOS Z8® MICROCONTROLLER MULTIPLIER/DIVIDER/SEARCH/MERGE

GENERAL DESCRIPTION

The Z86193 is a CMOS ROMless Z8® microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier, 32-bit/16-bit divider, three 16-bit counter/timers, search and merge instructions, Evaluation mode and a Bus Request mode. The device is code compatible with other Z8 family devices, yet it offers more powerful mathematical capabilities, data searching capabilities, and bit manipulation. The Z86193 is offered in a 64-pin VQFP package.

The Z86193 provides up to 16 output address lines permitting an address space of up to 64 Kbytes each of Program or Data memory. Eight address outputs are provided by a de-multiplexed 8-bit Address Bus (A7-A0) or by a multiplexed 8-bit Address/Data Bus (AD7-AD0). The remaining eight address lines (A15-A8) can be provided by the software configuration of Port0 to output address.

The Z86193 includes a bus which differs from other Z8 devices. The Z86193 provides bus control signals /RD (Read Strobe), /WR (Write Strobe), and ALE (Address Latch Enable).

There are 464 8-bit registers located on-chip and organized as 444 general-purpose registers, 16 control and status registers, one reserved register, and up to three I/O port registers. The Register File is partitioned into two Register Pages. Page0 contains 208 registers and Page1 contains 208 registers. The 48 other registers are common to both Register Pages. The Register file is also divided into 29 working register groups of 16 registers each. Configuration of the registers in this format allows the use of short format instructions. There are 17 additional registers implemented in the Expanded Register file in Banks D and E. Two of the registers may be used as general-purpose, while the other 15 are used to supply data and control for the multiplier/divider unit and the additional counter/timers.

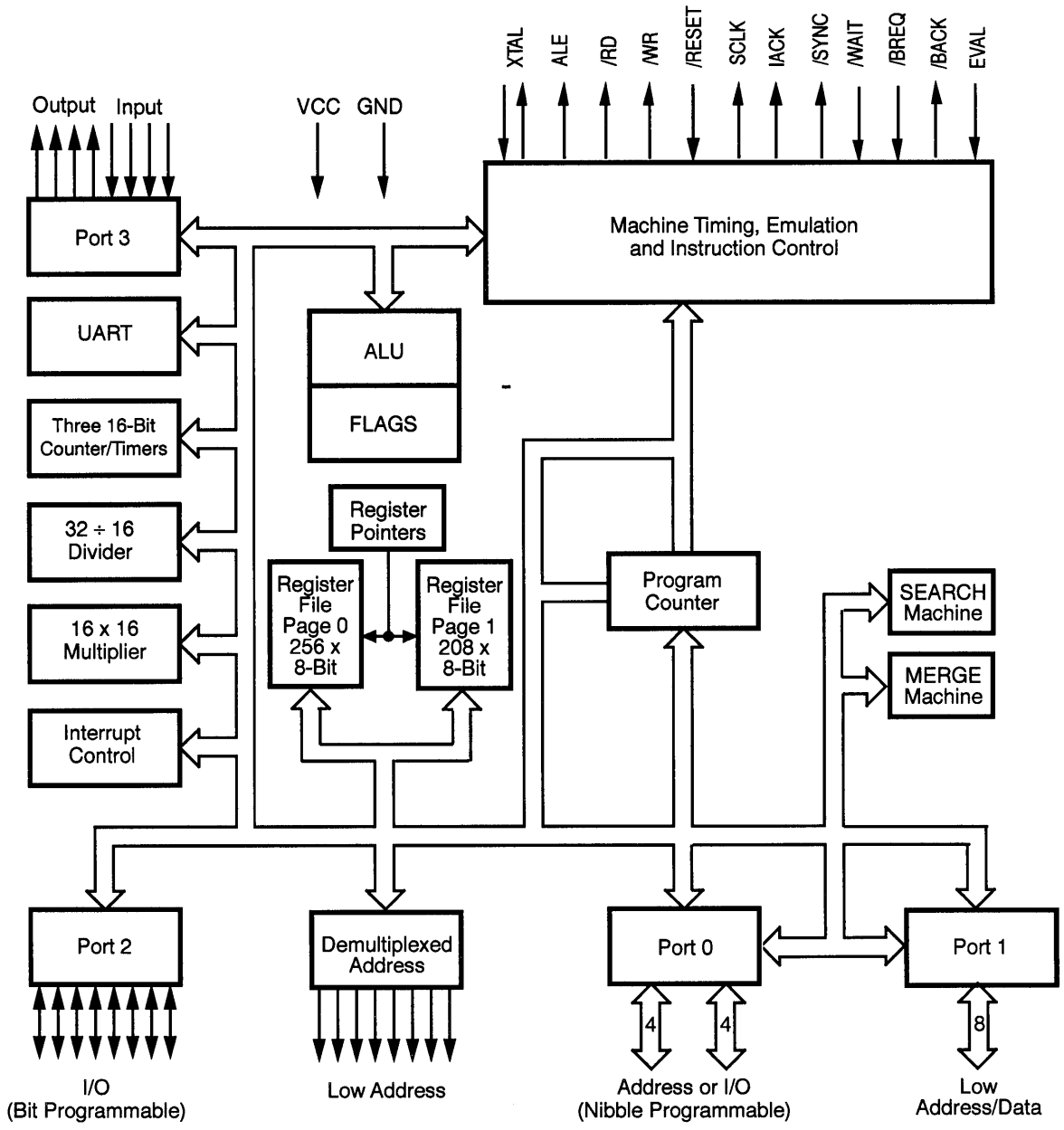
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

4

GENERAL DESCRIPTION (Continued)



Z86193 Functional Block Diagram

Z86295

HDD MICROCONTROLLER WITH ENHANCED DSP SERVO CONTROL

FEATURES

Part	ROM (Kbyte)	RAM* (Kbyte)	Speed (MHz)
Z86295	0	256	40

*General-Purpose

- 100-Pin VQFP
- 0°C to +70°C Temperature Range
- 4.5- to 5.5- Volt Operation Range
- 10-Bit Digital-to-Analog Converter (DAC)
- Programmable Servo Timer
- Z8® Microcontroller
- 16-Bit Digital Signal Processor (DSP)
- Six-Channel, 10-Bit Analog-to-Digital Converter (ADC)

GENERAL DESCRIPTION

The Z86295 microcontroller and servo controller provides increased system level integration. In addition to the industry-standard Z8 MCU, the Z86295 features an enhanced 16-bit DSP, a servo control timing generator, a six-channel 10-bit Analog-to-Digital Converter (ADC), and a 10-bit Digital-to-Analog Converter (DAC).

The DSP provides calculations for servo control. It allows arithmetic operations such as multiplication, addition, subtraction, and multiply accumulate of two 16-bit operands. Instruction executions are one-cycle pipeline and are usually performed in one clock cycle.

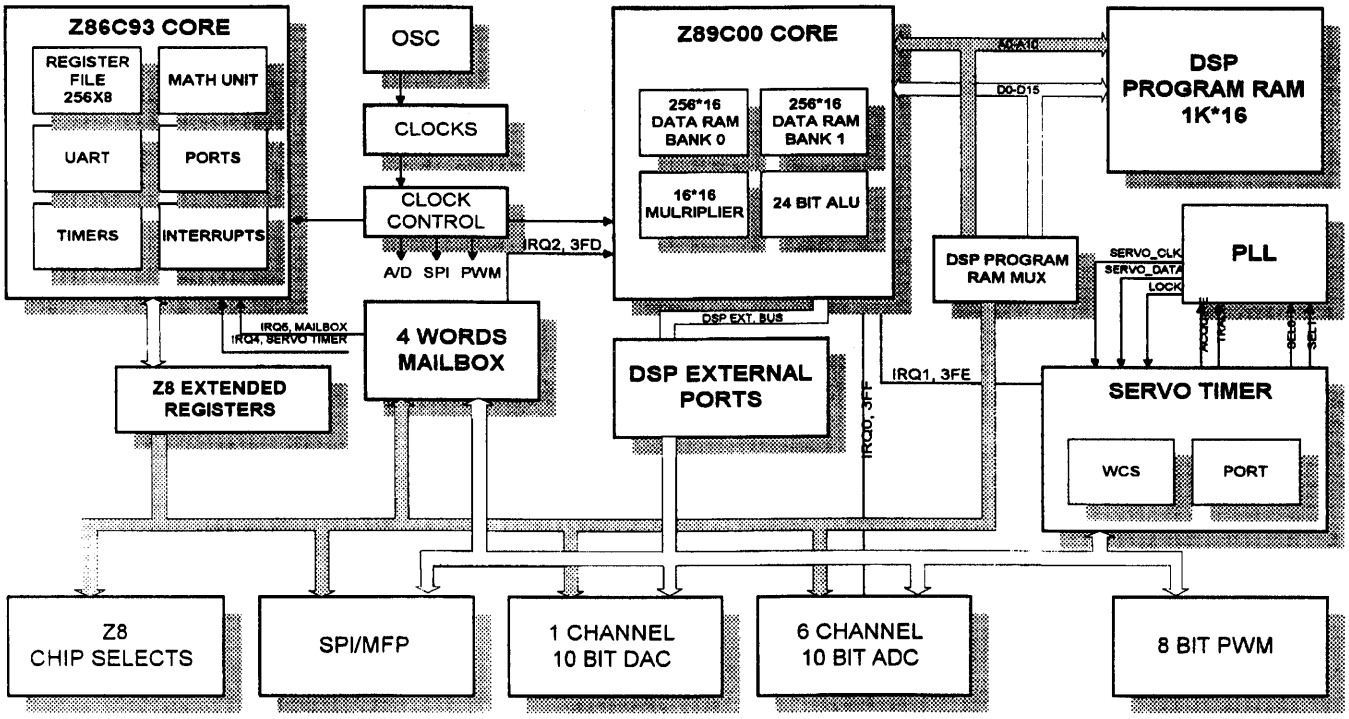
A mailbox feature provides an efficient communication link between the Z8 and the DSP. When the mailbox register is written to, an interrupt signal is sent to the other processor.

The servo timing processor handles the generation of burst and sector timing, spindle speed control, and detection of servo timing marks. It is fully programmable from the Z8 and can interrupt the Z8 or the DSP. Additionally, selected registers are available to the DSP for servo control.

The built-in 10-bit half-flash ADC and 10-bit DAC eliminates the need for additional system level components.

The Z86295 supports numerous power management modes including STOP, HALT, or low power-down of selected blocks. The Z86295 can be used to power-down external components such as the Read channel.

GENERAL DESCRIPTION (Continued)



Z86295 Functional Block Diagram

Z86C91 25 & 33 MHz

CMOS Z8® ROMLESS MICROCONTROLLER

FEATURES

Part	ROM (Kbyte)	RAM* (Kbyte)	Speed (MHz)
Z86C91	0	236	25, 33

*General-Purpose

- 44-Pin PLCC Package
- +4.5 to +5.5-Volt Operating Range
- Low-Power Consumption
- 0°C to +70°C Temperature Range
- 236 Byte Register Files
- 24 Input/Output Lines
- Vectored, Prioritized Interrupts with Programmable Polarity
- Full-Duplex UART
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescalers
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- Two Standby Modes: HALT and STOP

GENERAL DESCRIPTION

The Z86C91 is a ROMless member of the Z8® single-chip microcontroller family offering external memory use for applications where code flexibility is required.

Three address spaces, the Program Memory, Data Memory, and Register File, support a wide range of memory configurations with an efficient register/address space structure and multiplexed capabilities between address/data and I/O features.

For applications demanding powerful I/O capabilities, the Z86C91's 24 dedicated input and output lines are grouped into four ports, and are configurable under software control to provide timing, status signals, or parallel I/O, and an address/data bus for interfacing external memory.

Two on-chip counter/timers, with a large number of selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O datacommunications.

The Z86C91 is a cost-effective solution designed to use in mass storage applications requiring easy hardware/software system expansion and low-power consumption.

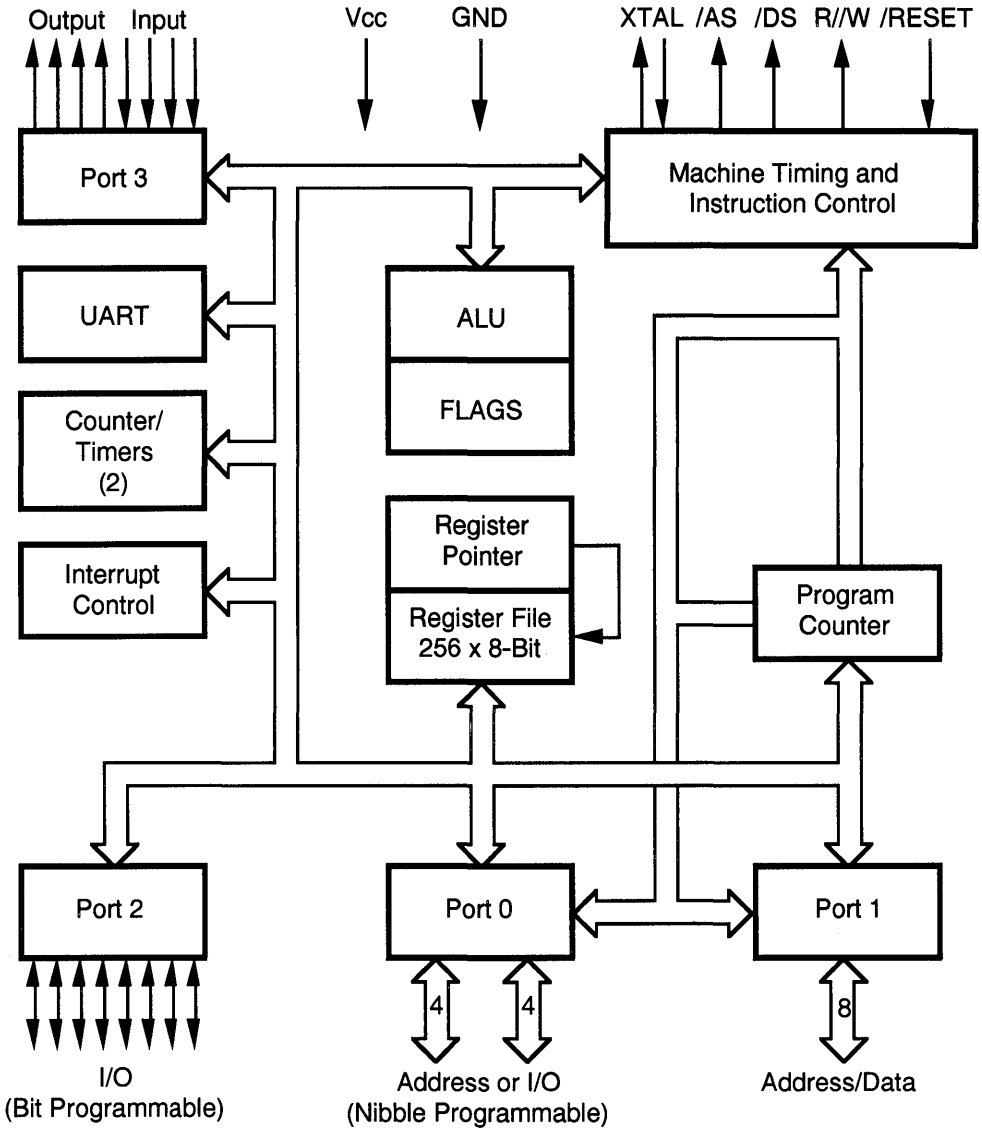
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

4

BLOCK DIAGRAM



Functional Block Diagram

Z86C93

CMOS Z8® MULT/DIV MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C93 is a CMOS ROMless Z8 microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier, 32-bit/16-bit divider, and three 16-bit counter timers (see Functional Block Diagram). A capture register and a fast decrement mode are also provided. It is offered in 40-pin PDIP, 44-pin PLCC, 44-pin QFP, and 48-pin VQFP packages. The Z86C93 is functionally compatible with the Z86C91, yet it offers a more powerful mathematical capability. In the PDIP package, the Z86C93 is fully pin compatible with the Z86C91. In the PLCC package, the Z86C93 is also pin compatible to the Z86C91, with the addition of four signals (SCLK, /IACK, /SYNC, and /WAIT). The /WAIT signal is only available on the 25 MHz and 33 MHz devices.

The Z86C93 provides up to 16 output address lines permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

There are 256 registers located on chip and organized as 236 general-purpose registers, 16 control and status registers, one reserved register, and up to three I/O port registers. The register file can be divided into 16 groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. There are an additional 17 registers implemented in the Expanded Register File in Banks D and E. Two of the registers may be used as general-purpose registers, while 15 registers supply the data and control functions for the Multiply/Divide Unit and additional Counter/Timer blocks.

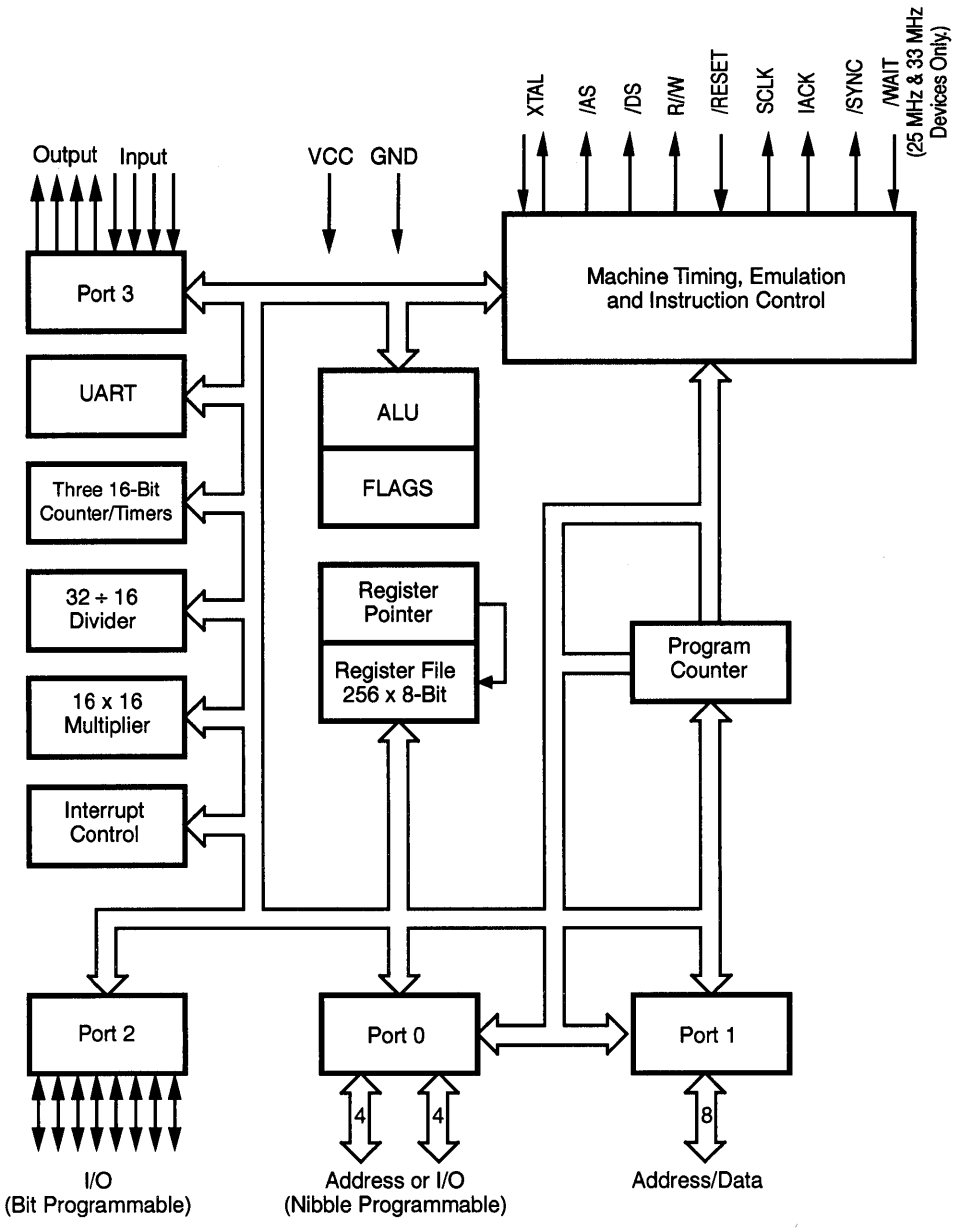
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

4

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z86C95
CMOS Z8® DIGITAL SIGNAL PROCESSOR (DSP)

GENERAL DESCRIPTION

The Z86C95 MCU (Microcontroller Unit) introduces a new level of sophistication to Superintegration™ ICs. The Z86C95 is a member of the Z8® single-chip microcontroller family incorporating a CMOS ROMless Z8 microcontroller with an embedded DSP processor for digital servo control. The DSP slave processor can perform 16-bit x 16-bit multiplicates and accumulates in one clock cycle. Additionally, the Z86C95 is further enhanced with a hardwired 16-bitx16-bit multiplier and a 32-bit/16-bit divider, three 16-bit counter timers with capture and compare registers, a half flash 8-channel 8-bit A/D converter with a 2 µsec conversion time, an 8-bit DAC with 1/4 programmable gain stage, UART, serial peripheral interface, and a PWM output channel (Functional Block Diagram). It is fabricated using CMOS technology and offered in an 80-pin QFP, 84-pin PLCC, or 100-pin VQFP package.

The Z86C95 provides up to 16 output address lines thus permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits are provided via output address bits A15-A8.

There are 256 registers located on chip and organized as 236 general-purpose registers, 16 control and status registers, and four I/O port registers. The register file can be divided into sixteen groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. Also, the Z86C95 contains 512 bytes of DSP Program RAM and 128 words of DSP data RAM.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

4

OPERATING ERRATA

This notice only applies to devices top marked "Z86C9524 ASC/FSC/VSC" with a date code of 9237 or later.

1. A DSP load to the DAC Register fails below approximately V_{CC} = 4.7V.
2. Clipping occurs in the linearity of the DAC with a 100K load at about 3.3V output (VDHI = 3.5V).
3. $I_{CC}1$ at HALT Mode will show a current of 17-18 mA, then will jump to 40-70 mA, and will settle between 17-24 mA. Settling time is about 10-15 seconds.
4. $I_{CC}2$ at STOP Mode and DSP Pause will show a current of 1-2 mA, then will jump to 5-7 mA, and will settle at 3-4 mA. Settling time is about 10-15 seconds.

The following operating errata only applies to devices topmarked with "Z86C95 ASC/FSC/VSC."

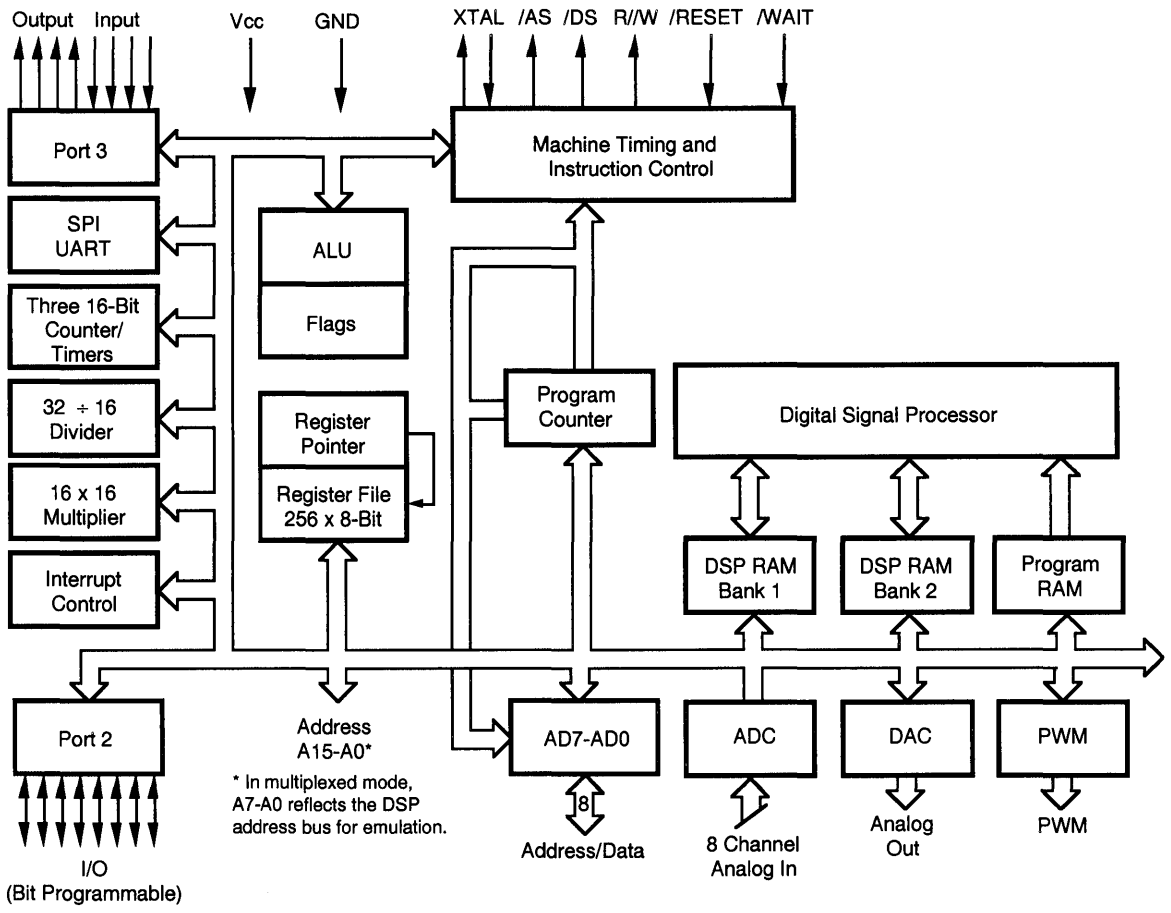
1. ICC1 at HALT Mode will show a current of 17-18 mA, then will jump to 40-70 mA, and will settle between 17-24 mA. Settling time is about 10-15 seconds.
2. ICC2 at STOP Mode and DSP Pause will show a current of 1-2 mA, then will jump to 5-7 mA, and will settle at 3-4 mA. Settling time is about 10-15 seconds.

The following operating errata only applies to devices topmarked with "Z86C9540 ASC/FSC/VSC or SL 1636."

1. ICC1 at HALT Mode will show a current of 17-18 mA, then will jump to 40-70 mA, and will settle between 17-24 mA. Settling time is about 10-15 seconds.

GENERAL DESCRIPTION (Continued)

2. ICC2 at STOP Mode and DSP Pause will show a current of 1-2 mA, then will jump to 5-7 mA, and will settle at 3-4 mA. Settling time is about 10-15 seconds.
3. The zero error for the ADC at 25°C is about 180 mV.



Functional Block Diagram

SUPPORT PRODUCT

Z86C9300ZEM

ICEBOX™ FAMILY Z8® IN-CIRCUIT EMULATOR –C93

HARDWARE FEATURES

- Supported Devices

Package	Emulation	Programming
40-Pin DIP	**Z86C93**	**N/A**
44-Pin PLCC	Z86C93	N/A

- Real-Time Emulation
- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Z8 GUI Emulator Software
- Windows-Based User Interface
- RS-232 Connector
- ICE Pod Connector for Emulation
- HP-16510 Logic Analysis System Interface Connector

GENERAL DESCRIPTION

The Z86C9300ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the above listed Z8 microcontroller devices.

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering, and program debugging, are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z86C9300ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5.0 VDC, ± 5%
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 16 MHz
Shipped with 12 MHz Crystal

Power Requirements

+5.0 VDC @ 0.5A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

BM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z86C93 Emulator

•Emulation Base Board includes:
CMOS Z86C9320PSC
8K x 8 EPROM (Programmed with Debug Monitor)
32K x 8 Static RAM
Three 64K x 4 Static RAM
RS-232C Interface
Reset Switch

•Z86C93 Emulation Daughterboard
20 MHz CMOS Z86C9320VSC Chip
80-Pin Target Connectors
Three HP-16510 Logic Analysis System Interface Connectors

Cables/Pods

Power Cable with Banana Plugs
Power Cable with 1A Slow-Blow Fuse
DB25 RS-232C Cable
44Pin PLCC Emulation Pod Cable
40-Pin DIP Emulation Pod Cable

Host Software

Z8® GUI Emulator Software
ZASM Cross-Assembler/MOBJ Object File Utilities

Documentation

Emulator User Manual
Z8 Cross-Assembler User's Guide
Universal Object File Utilities (MOBJ)
Registration Card
Product Information

LIMITATIONS

1. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

3. Switching ICEBOXes without quitting the GUI is not supported.

4. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

5. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

   ```
   000C    SRP    #%0
   000E    LD     R4, #%0016
   0010    LD     R5, @R4
   0012    NOP
   0013    JP     %000C
   0016    NOP
   ```

   Setting the breakpoint at %0016 and click GO.

   Result: The code will break and stop at %0012.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

6. If the emulator is running a user code at full speed and the port window is opened: Switching to another application or minimizing the GUI (then restoring) will result in the following ICEBOX Communications Error message: "Emulator rejected command: target program is executing." This message may need to be cleared several times (as many as seven) before the GUI returns to normal operation.

   Workaround: Always close the port window before leaving the GUI.

LIMITATIONS (Continued)

7. Do not put breakpoint at address after Stop instruction. This will cause program counter to continue at that location after a Stop-Mode Recovery.

8. The ICEBOX cannot stop timers during single-step operation, or upon reaching of breakpoint.

PRECAUTION LIST

1. All Z8 control registers are write only unless stated otherwise.

2. Power Supply ramp-up/rise time must be such that when minimum power-on reset time (T_{POR}) expires, then the V_{CC} must be in the supported specified operating range of the device.

3. The ICEBOX cannot stop Timers and Interrupts at a breakpoint or during ICEBOX Halt operation or a single-step operation. The stack will overflow if an interrupt is enabled and the ICEBOX is in HALT, single-step, or breakpoint. (This is a limitation of the ICE chip.)

4. Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the ICE chip specifications.

5. The general-purpose registers after Power-On Reset or at initial emulator use will be different than the actual device. The emulator self test will always leave the same values in the general-purpose registers, while the real device will have a random/undefined value in the general-purpose registers.

6. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

7. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

8. For 386 PCs, set the baud rate to 19.2K or less because Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.

ZiLOG

SUPPORT PRODUCT

Z86C9500ZCO

Z8®/DSP EVALUATION BOARD

DESCRIPTION

The Z86C9500ZCO Evaluation Board contains an assembled circuit board, software and documentation for use in evaluating the Z86C95 Z8®/DSP microcontroller. The board comes equipped with a monitor program which provides access to all the Z86C95 registers and on-board memory and assists in using the Z86C95.

SUPPORTED DEVICES

Z86C95

SPECIFICATIONS

Power Requirements

+3 < Vcc < +5 Vdc

Dimensions

Width: 5.2 in. (13.2 cm)
Length: 5.0 in. (12.7 cm)

KIT CONTENTS

Z86C95 Evaluation Board

Z86C95 CMOS Microcontroller Z8®/DSP unit
8Kx8 EPROM with Monitor Program
32Kx8 SRAM
RS232-C Port
Sockets for external DAC80 and ADC0820
12 LEDs
Headers for access to all signals
Pin-out Header
RS232-C Connector
Power Connector

Software (IBM-PC Platform)

Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader

Documentation

Z8 Family Data Book
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide
Z86C95 Product Specification
Z86C95 Evaluation Kit User's Guide

ZiLOG

SUPPORT PRODUCT

Z8619300ZCO

Z8® MULTIPLY/DIVIDE/SEARCH/MERGE EVALUATION KIT

DESCRIPTION

The Z86193 Evaluation Board contains an assembled circuit board, software and documentation for use in evaluating the Z86193 microcontroller. It is equipped with a monitor program to assist in the use of the Z86193 and to provide access to all the registers within the Z86193 and the on-board memory.

Headers are included for access to all signals and for connection to an emulation system. The board also supports the use of FLASH memory.

Supported Device

Z86193

Specifications

Power Requirements

4.5VDC to 5.5VDC

Dimensions

Width: 4.1 in. (10.4 cm)
Length: 6.1 in. (15.5 cm)

KIT CONTENTS

Board

Z86193 CMOS Microcontroller Z8® with Multiply/Divide/Search/Merge
32K x 8 EPROM with Monitor Program
32K x 8 SRAM
40 MHz Oscillator
13 LEDs
Pin-Out Header
RS-232C Connector
Power Connector
Reset Switch

Cables

Power Cable
RS-232 Cable

Software (IBM-PC Platform)

Z8®/Z80®/Z8000® Cross Assembler
MOBJ Linker/Loader
Serial Communications Program

Documentation

Z86193 User's Manual
Z86193 Evaluation Kit User's Manual
Z8® Cross Assembler User's Guide
MOBJ Linker/Loader User's Guide
Product Registration Card

ZILOG

SUPPORT PRODUCT

Z8629501ZCO

Z8® DSP/SERVO TIMER DEVELOPMENT KIT

DESCRIPTION

The Z86295 Development Board contains an assembled circuit board, software and documentation for use in developing with the Z86295 microcontroller. It is equipped with a monitor program to assist in the use of the Z86295, and to provide access to all the registers within the Z86295 and the on-board memory.

Separate headers are included for access to all signals and for connection to an emulation system. The board can be used stand-alone or in conjunction with the ZIA™ development board.

Supported Device

Z86295

Specifications

Power Requirements

4.5VDC to 5.5VDC

Dimensions

Width: 8.0 in. (20.3 cm)
Length: 10.0 in. (25.4 cm)

KIT CONTENTS

Board

Z86295 CMOS Microcontroller Z8® with DSP and Servo Timer
32K x 8 EPROM with Monitor Program
8K x 8 SRAM
20 MHz Oscillator
16 LEDs
Pin-Out Header
H-P Logic Analyzer Connectors
ZIA Development Board Connector
RS-232C Connector
Power Connector
Reset Switch

Cables

Power Cable
RS-232 Cable

Software (IBM-PC Platform)

Z8®/Z80®/Z8000® Cross Assembler
MOBJ Linker/Loader

Documentation

Z86295 User's Manual
Z86295 Evaluation Kit User's Manual
Z8® Cross Assembler User's Guide
MOBJ Linker/Loader User's Guide
Product Registration Card

ZiLOG

8-Bit Microcontrollers

Z8® Microcontrollers 1

IR Remote Controllers 2

Computer Peripheral Controllers

Keyboard /Input Devices 3

Mass Storage 4

PCMCIA 5

DSP (Digital Signal Processors)

Television/Cable/Satellite/Set-Top Boxes 6

Voice Processors 7

DSP Cores 8

Z16M27

PCMCIA-16 INTERFACE

FEATURES

Part	RAM* (Bytes)	Speed (MHz)
Z16M27	256	20

*Attribute

Translation Capabilities

- PCMCIA to IDE Translation
- IDE to IDE Mapping, Pass Through Mode
- Direct Memory Access (DMA) Support

Supports Multiple Applications

- 256 Bytes of Attribute Memory
- Five Configuration Registers
- Three Additional Registers to Support EEPROM Programming
- Three Programmable Memory or I/O Map Ranges
- Conforms to PCMCIA Standards
- EXCA Register Compatible

DESCRIPTION

The Z16M27 is a general-purpose PCMCIA adapter chip used on the side of the interface. The Z16M27 contains special circuitry for PCMCIA-to-ATA/IDE applications, but easily configures to all types of memory and I/O mapped peripheral hardware, supporting a wide variety of PC card applications.

The Z16M27 can be used in a stand-alone configuration without the use of a local processor by providing all of the attribute memory, CCRs, range, and interrupt types through a serial EEPROM. The serial EEPROM is read automatically using an internal EEPROM sequencer. The Z16M27 can also be configured through a local processor for use on intelligent controller systems.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

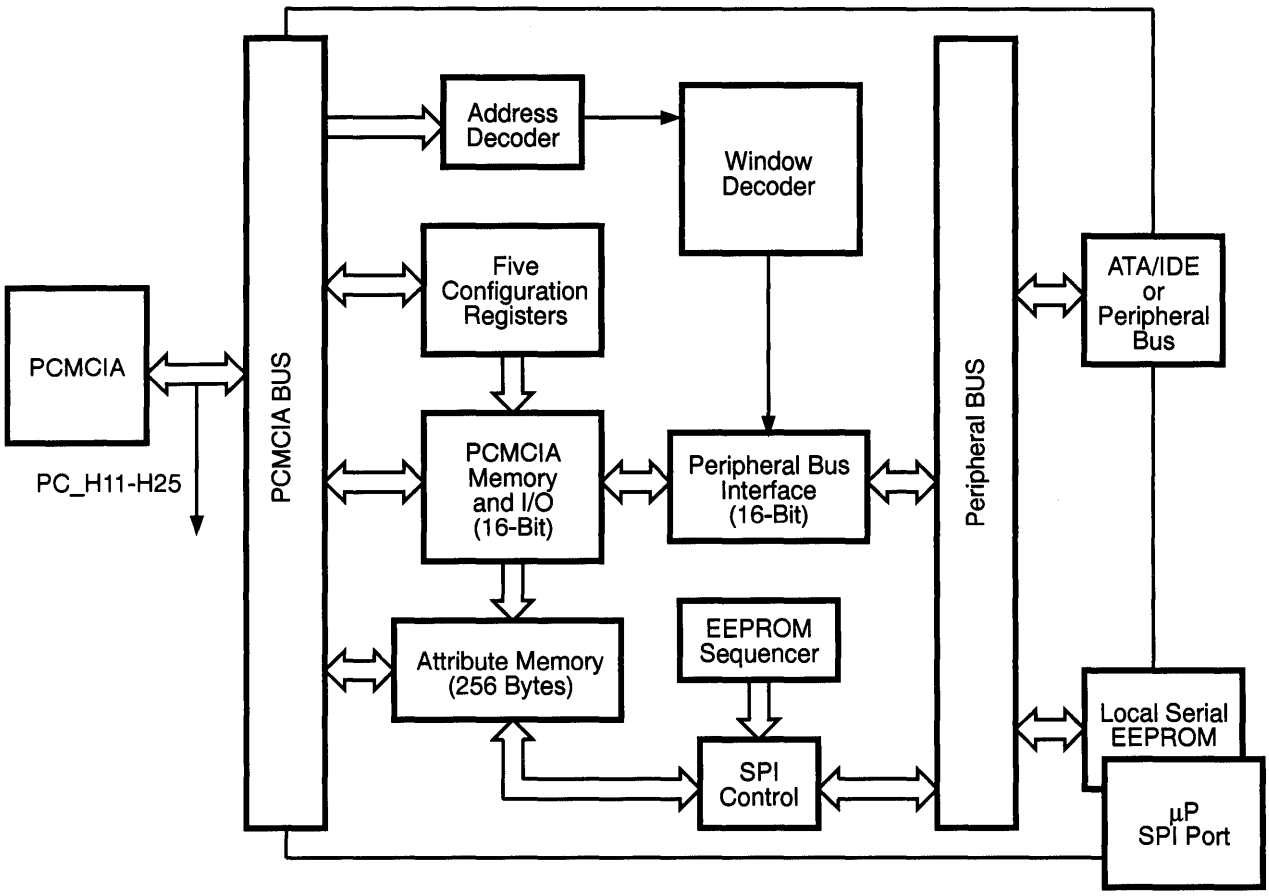
Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

5

GENERAL DESCRIPTION (Continued)

The local processor connects to the Z16M27 through the serial interface or can be programmed through an external EEPROM. The Z16M27 provides for the PCMCIA to ATA/IDE translation, ATA/IDE to ATA/IDE mapping, or PCMCIA to three general-purpose maps.



Z16M27 Functional Block Diagram

Z16017/Z16M17
SL1868
PCMCIA-16 INTERFACE

FEATURES

Device	RAM* (KB)	Speed MHz
Z16017 - 1868	256	20
Z16M17 - 1868	256	20

Note: *General-Purpose

Translation Capabilities

- PCMCIA to IDE Translation
- IDE to IDE Mapping, Pass Through Mode
- Direct Memory Access (DMA) Support

Supports Multiple Applications

- 256 Bytes of Attribute Memory
- Five Configuration Registers
- Three Additional Registers to Support EEPROM Programming
- Three Programmable Memory or I/O Map Ranges
- Conforms to PCMCIA Standards
- EXCA Register Compatible

GENERAL DESCRIPTION

The Z16017/Z16M17 is a general-purpose PCMCIA adaptor chip used on the card side of the interface. The Z16017/Z16M17 contains special circuitry for PCMCIA-to-ATA/IDE applications, but easily configures to all types of memory and I/O mapped peripheral hardware, supporting a wide variety of PC card applications.

The Z16017/Z16M17 can be used in a stand-alone configuration without the use of a local processor by providing all of the attribute memory, CCRs, range, and interrupt types through a serial EEPROM. The serial EEPROM is read automatically using an internal EEPROM sequencer. The Z16017 can also be configured by a local processor if used in intelligent controller systems.

The Z16017/Z16M17 provides for the PCMCIA to ATA/IDE translation, ATA/IDE to ATA/IDE mapping, or PCMCIA to three general-purpose maps.

The Z16017/Z16M17 supports three general-purpose maps and one special map for PCMCIA to ATA/IDE translations.

5

GENERAL DESCRIPTION (Continued)

Notes: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

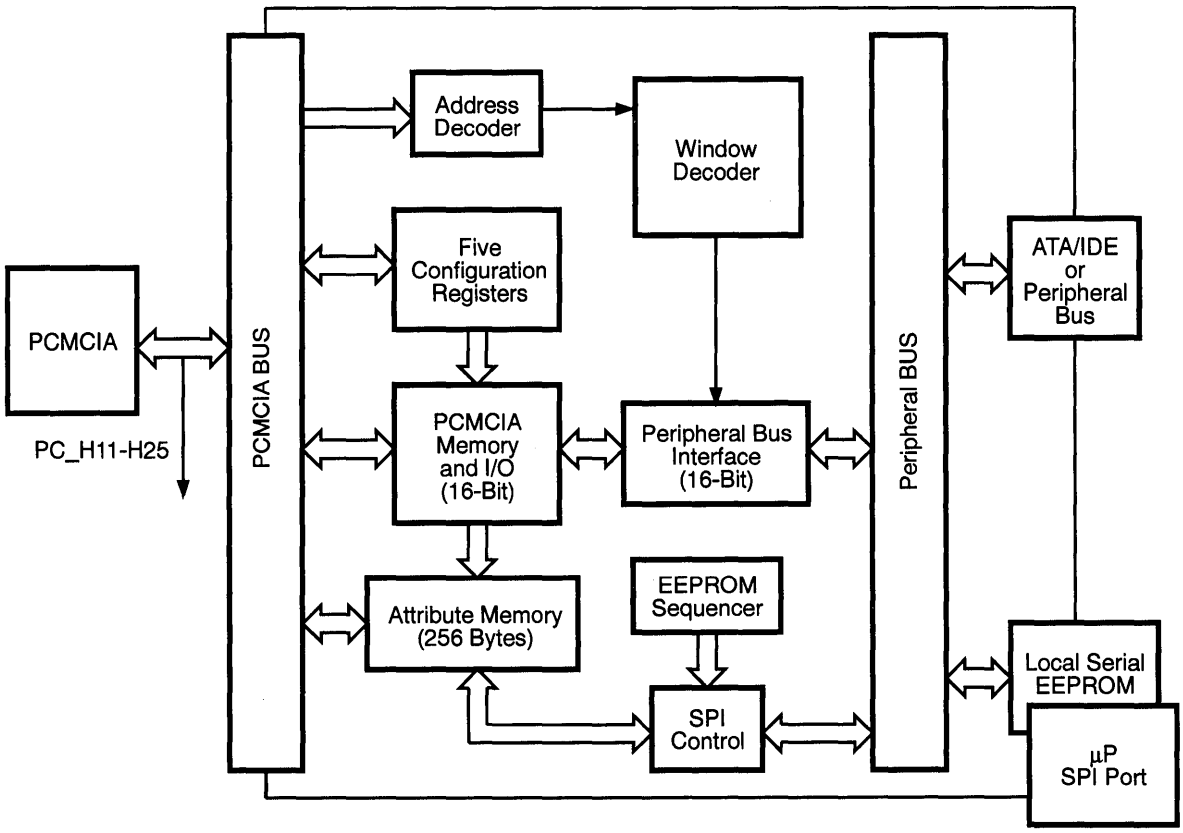


Figure 1. Z16017/Z16M17 Functional Block Diagram

ZiLOG

SUPPORT PRODUCT

Z8601700ZCO

PCMCIA INTERFACE DEVELOPMENT KIT

GENERAL DESCRIPTION

The Z8601700ZCO Development Kit allows easy evaluation of the functions and capabilities of the Z86017 PCMCIA Interface Adapter. The board provides a ZIF socket for easy insertion and removal of the Z86017, as well as a full pin-out header for access to all signals. The board also provides breadboard space to assist in development.

The power to the Z86017 can either be supplied through a common point for current measurements, applied through the interface, or supplied through a separate power connector. Programming the Z86017 is accomplished through the SPI port of a microcontroller or through the on-board EEPROM. The main clock source is supplied through the interface or through the on-board clock.

Supported Devices

Z86017

Specifications

Power Requirements

+3.0V < VCC < +5.5V

Dimensions

Length: 7.6 in. (19.3 cm)
Width: 4.5 in. (11.4 cm)

Kit Contents

Evaluation Board

Z86017 PCMCIA Interface Adapter Device
100-Pin VQFP ZIF Socket
256 X 8-Byte EEPROM
20 MHz Oscillator
Headers for full Z86017 pin-out
Headers for access for PCMCIA signals
Headers for connection to AT-Bus (on both Host and ATA side)
Headers for connection to PCMCIA Extender Card
Header for intelligent peripheral programming of EEPROM
Power Connector

ZPCMCIA0ZDP PCMCIA Extender Card

Cables

Two 6-inch, 34-pin IDC to 34-pin IDC Cables
Power Cable with 1.0A Fuse
Power Cable with Bana Plugs

Software

Example Initialization Code

Documentation

Z8601700ZCO Evaluation Kit User's Manual
Z86017 Product Specification
Z86017 User's Manual
Product Registration Card

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ZPCMCIA0ZDP

PCMCIA EXTENDER CARD

GENERAL DESCRIPTION

The ZPCMCIA0ZDP PCMCIA Extender Card extends PCMCIA Type II based PC cards by extending the card out of the slot. The card provides labeled headers for access to all signals. The flat-keyed connector allows easy insertion and removal of the card from the PCMCIA slot.

Kit Contents

ZPCMCIA0ZDP PCMCIA Extender Card

- 68-Pin PCMCIA Connector
- Two 34-Pin Headers
- Two 0.1 µF Capacitors
- Two 10 Position DIP Switches
- 68-Pin PCMCIA Socket
- 4-Pin Ground Header
- 100 µF Capacitor

Documentation

- ZPCMCIA0ZDP User's Guide
- Product Registration Card

ZPCSCSI0ZDP

PCMCIA SCSI ADAPTER EVALUATION KIT

GENERAL DESCRIPTION

The ZPCSCSI0ZDP is an evaluation kit for Zilog's PCMCIA SCSI adapter solution, available for OEM license and manufacture.

Housed in a Type II PCMCIA card, the kit is provided with a SCSI Software Driver that interfaces the Zilog Z53C8003FSC1746 and Z8601720ASC to certain SCSI CD-ROM, hard disk, removable hard disk, magneto-optical and floptical drives, as well as other SCSI peripherals.

Supported Devices

Z53C8003FSC1746, Z8601720ASC

Specifications

Power Requirements

4.75 to 5.25 VDC

Dimensions

Type II PC Card
Width: 54.0 mm
Length: 85.6 mm

Contents

PC Card
33-Pin PCMCIA to High Density 50-Pin SCSI Cable
Floppy Disk Containing Device Driver and Utilities
Z86017 User Manual
Z53C8003FSC1746 Product Specification
ZPCSCSI0ZDP User Manual

SCSI DRIVER SPECIFICATIONS

Capacity

Up to seven daisy-chained SCSI devices.

Driver and Installation Files

File Name	Description
INSTALL.EXE	DOS installation program.
INSTALL.DAT	Installation Script for INSTALL.EXE.
DELAY.EXE	Used by INSTALL.EXE to prevent SMARTDRV from forgetting to update AUTOEXEC.BAT and CONFIG.SYS during warm boot. The program creates a small delay then instructs SMARTDRV to flush cache & send all cache data to hard disk.
XL720.LST	Up to date device support list.
SETUP.EXE	Windows setup program.
DISK.ID	Floppy disk identification.
\DOS\MBOX.EXE	DOS version audio CD player utility.
\DOS\XFDISK.COM	A setup and format utility for hard disk, MO and floptical drives.
\DOS\ASPI720.SYS	Card enabler and ASPI manager for all SCSI devices.
\DOS\CD720.SYS	CD-ROM device driver.
\DOS\RHD720.SYS	Hard disk/removable hard disk/MO/floptical device driver.
\WINDOWS\MBOX.EXE	Windows version audio CD player utility.
\WINDOWS\SCSCSI.EXE	Windows SCSI device inquiry utility.
\WINDOWS\WINASPI.DLL	Windows card enabler and ASPI manager for all SCSI devices.
\WINDOWS\VBRUN300.DLL	Visual Basic Interpreter.
\WINDOWS\THREED.VBX	Used by Visual Basic Interpreter.
\WINDOWS\OMNI.GRP	Group File for Omni SCSI.
\WINDOWS\README.TXT	Read Me File.

Wait State

Supports zero and one wait state.

Data Transfer

500 Kbyte+ per second.

Data Format

8-Bit with automatic parity generation.

Compatibility

MS-DOS Versions 5.X, 6.X, PC-DOS 6.2, Windows 3.1
IBM PC XT/AT Compatible Systems with PCMCIA Card Reader
IBM PC Compatible Notebook Computers with PCMCIA Support
PCMCIA 2.1 and Future Releases

Transfer Mode

Blind Mode

* IBM is a registered trademark of International Business Machines Corp.

Card and Socket Services Software:

AMI	Socket Service Version 1.00 and above
	Card Service Version 1.04 and above
Award	Socket Service Version 2.0 and above
(Cardware)	Card Service Version 2.0 and above
DataBook	Socket Service Version 3.00 and above
(CardTalk)	Card Service Version 3.00 and above
IBM	Socket Service Version 1.04 and above
	Card Service Version 1.12 and above
Phoenix	Socket Service Version 3.00 and above
	Card Service Version 3.00 and above
SystemSoft	Socket Service Version 1.02 and above
(CardSoft)	Card Service Version 2.06 and above

Hard Disk:

All 1.8", 2.5", 3.5" and 5.25" SCSI hard disk, block size must be equal to 512 bytes.

Floptical:

Insite	1325VM
Iomega	Io20S

Removable Hard Disk:

Bernoulli	B290X-UNI, MultiDisk 150
SyQuest	SQ555, SQ3270S, SQ5110

Magneto Optical:

Canon	MO-50015
Fujitsu	Dynamo MO 128
HP	C1701A, C1711, C1716
IBM	3510
Magstore	M/O, Mini 128, Mini 256
Maxoptics	Tahiti 1, Tahiti 2
Mitsubishi	ME-3U1-M21, ME-5U1-M21
MOST	RMS-128E
Panasonic	LF3000, LF3004, LF900
Reflection Sys.	RF3010
Ricoh	RO-3010E, RO-5030E, RO-5031E, RO-5031EII, RS-3010E, RS-9200E, RS-9200EII
Sony	SMO S350, SMO S510
Teac	OD-3000

CD-ROM:

Apple	Power CD, CD-SC, CD-SC Plus, CD-150, CD-300, CD-300i
APS Tech.	T3401
CD Tech.	Porta-Drive
Chinon	CDS-535, CDX-535
DC Tech.	DC Hornet
FWB Inc.	Hammer CD
Insight	Talon TA-200
Intoll Corp.	600CD
JPN	CDR-93
Mac Product	Majik CD-ROM
Mass Micro.	Datapak CD
MediaVision	CDR-93, Reno
Micronet	Micro/CR-ROM
Micro Design	SCSI Express 600
Mirror Tech.	Mirror CD-ROM
Legacy	CD-ROM 2x
Liberty Sys.	Liberty 115 Series
NEC Corp.	CDR-25, CDR-35, CDR-36,CDR-36M, CDR-37, CDR-38, CDR-55, CDR-72, CDR-73, CDR-73M, CDR-74, CDR-74-1, CDR-80, CDR-82, CDR-83, CDR-83M, CDR-84, CDR-84-1, CDR-210,CDR-510
Optical Access	CD/Allegro II, CD/Performer II
Peripheral Land	PL CD-ROM MS200
Plextor	DM-3028, DM-5028, 4PLEX
Procom Tech.	CD/MX, ICD/MX, MCD-DS
Relax Tech.	Vista Toshiba
Sanyo	CRD-400I
Sony	CDU-55S, CDU-541, CDU-561, CDU-6110, CDU-6111, CDU-6211, CDU-6811, CDU-7211, CDU-8003, CDU-8012
Teac	CD-50
Texel	DM-3010, DM-3020, DM-3021, DM-3022, DM-3024, DM-3028, DM-3110, DM-3120, DM-5021, DM-5022, DM-5024, DM-5110, DM-5120, DM-7120A, DM-7120B,
Toshiba	XM-3100, XM-3101, XM-3201A, XM-3201B, XM-3301, XM-3301TA, XM-3401, XM-3401B, XM-4101, XM-5100A

Note: Some special functions in certain devices may not be supported.

ZiLOG

8-Bit Microcontrollers

Computer Peripheral Controllers

DSP (Digital Signal Processors)

Z86C27-ROM
Z86C97-ROMLESS
CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller for Consumer Television Applications, 64-Pin DIP Package
- Low Cost
- Low Power Consumption
- Fast Instruction Pointer - 1.5 µs @ 4 MHz
- Two Standby Modes-STOP and HALT
- Low Voltage Detection/Voltage Sensitive Reset
- 35 Input/Output Lines
- On-Screen Display Controller
- All Digital CMOS Levels Schmitt-Triggered
- 8 Kbytes of ROM (Z86C27)
- 236 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speed up to 4 MHz
- Permanently Enabled Watch-Dog/Power-On Reset Timer
- 4K x 6-Bit Character Generator ROM
- 160 x 7-Bit Video RAM
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.
- Mask Programmable 128 Character Set Displayed in an 8-Row x 20-Column Format, 12 x 5 Pixel Character Cell, Capable of Supporting English, Korean, Chinese, and Japanese High Resolution Characters.
- Fully Programmable Color Attributes Including Row Character, Row Background/Fringes, Frame Back-Ground/Position, Bar Graph Color Change, and Character Size.
- Programmable Display Position and Character Size Control.
- One Pulse Width Modulator (14-Bit Resolution) for Voltage Synthesis Tuner Control
- Five Pulse Width Modulators (8-Bit Resolution) for Picture Control
- Seven Pulse Width Modulators (6-Bit Resolution) for Audio Control
- Port 2 (8-Bit Programmable I/O) and Port 3 (2-Bit Input, 3-Bit Output) Register Mapped Ports
- Port 4 (8-Bit Output), Port 5 (8-Bit LED Drive Output) and Port 6 (6-Bit Input and Tri-State Comparator AFC Input) Memory Mapped I/O Ports.

6

GENERAL DESCRIPTION

The Z86C27 and Z86C97 Digital Television Controllers (DTC) introduce a new level of sophistication to single-chip architecture. The Z86C27/C97 are members of the Z8® single-chip microcontroller family with 8 Kbytes of ROM (Z86C27), ROMless (Z86C97) and 236 bytes of RAM. Both devices are housed in a 64-pin DIP package, and are CMOS compatible. Having the ROM/ROMless selectivity, the DTC offers both external memory and pre-programmed ROM which enables the Z8 microcontroller to be used in a high-volume production application device embedded with a custom program (customer supplied program).

GENERAL DESCRIPTION (Continued)

The Z86C97 ROMless offers the use of external memory rather than a preprogrammed ROM. This enables the Z8 microcontroller to be used in prototyping, low volume applications, or where code flexibility is required. Zilog's DTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications. The Z86C97 is supplied with Zilog's own character ROM.

The Z86C27/C97 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The devices have an 8-bit internal data path controlled by a Z8 microcontroller, and On Screen Display (OSD) logic circuits/Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Port 2 and Port 3), Interrupt control logic (1 software, 2 external and 3 internal interrupts), and a standby mode recovery input port (Port 3, P30).

The OSD control circuits support 8 rows x 20 columns for 128 kinds of characters. The character color is specified by row. One of the 8 rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying 11 x 15 dot characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Seven 6-bit PWM ports are used for controlling audio signal level. Five 8-bit PWM ports are used to vary picture levels.

The Z86C27/97 have 35 I/O pins dedicated to input and output for DTC applications demanding powerful I/O capabilities. These lines are grouped into five ports, and are configurable under software control to provide timing, status signals, parallel I/O, and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Register File, and Data Memory. The Register File is composed of 236 bytes of general-purpose register, two I/O Port registers and 15 control and status registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the Z86C27/97 offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

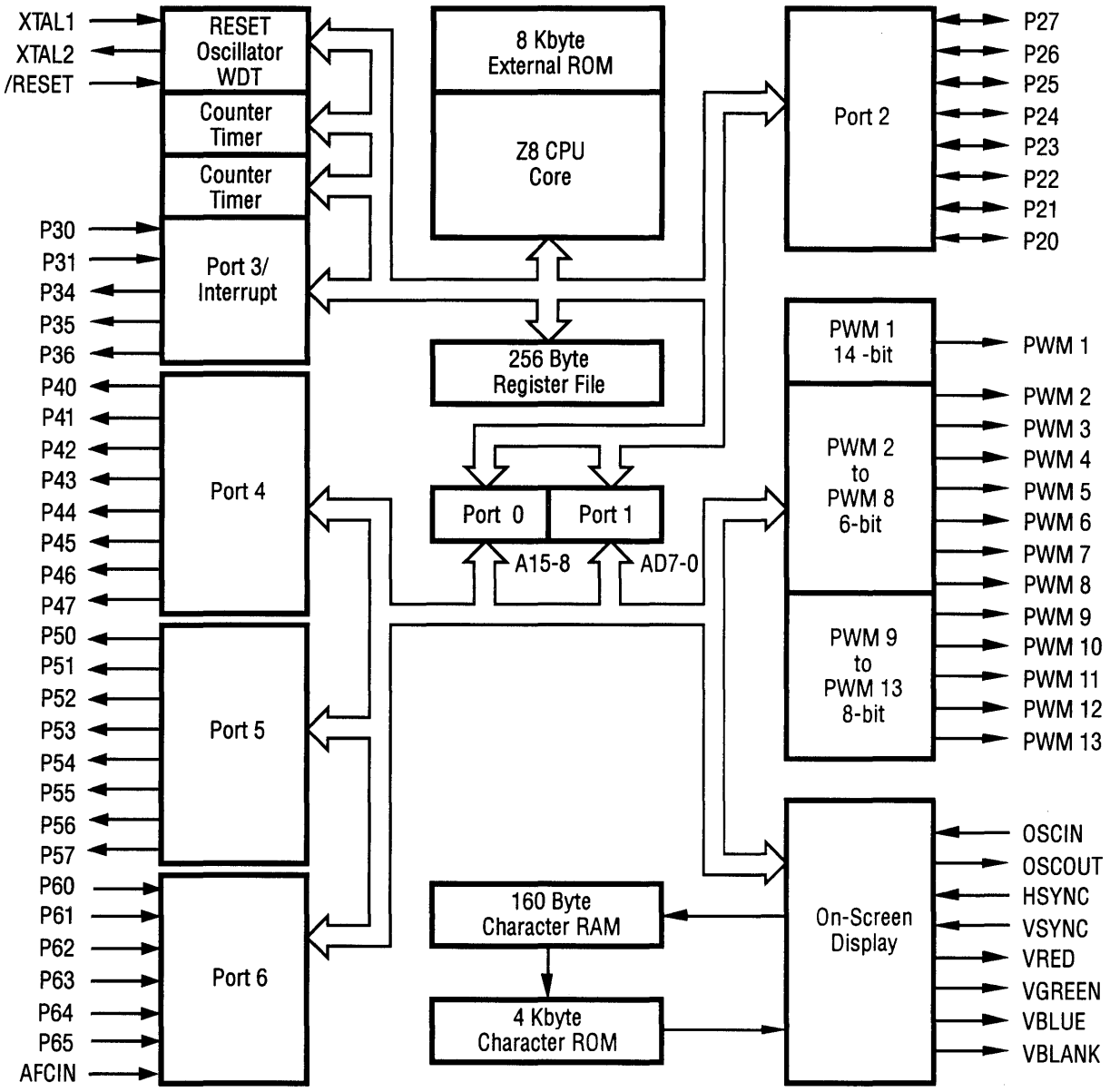


Figure 1a. Z86C27 Functional Block Diagram

6

FUNCTIONAL DESCRIPTION (Continued)

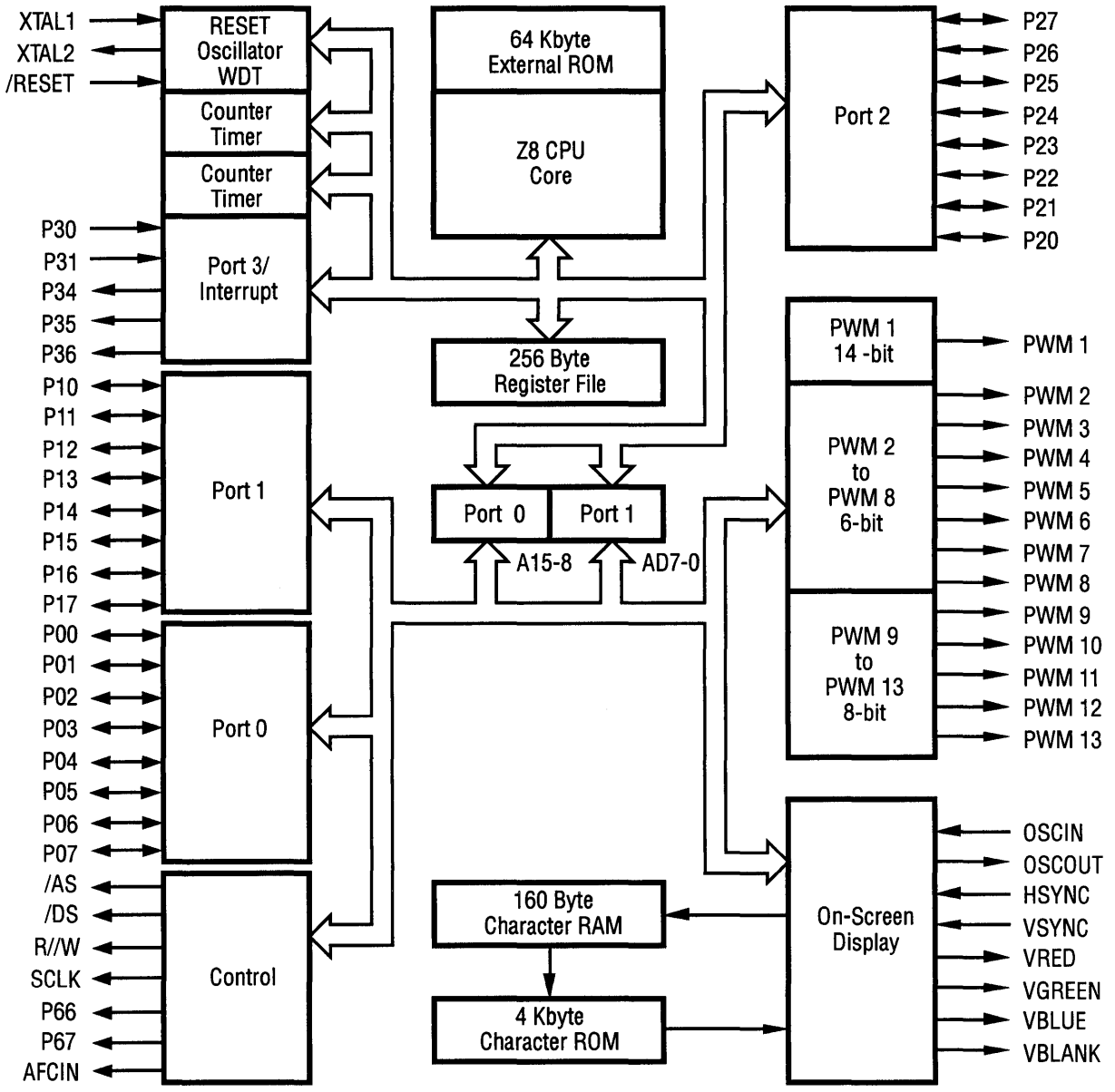


Figure 1b. Z86C97 Functional Block Diagram

Z86C47 ROM

CMOS Z8® 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C47 Digital Television Controller (DTC) introduces a new level of sophistication to single-chip architecture. The Z86C47 is a member of the Z8® single-chip microcontroller family with 16 Kbytes of ROM and 236 bytes of RAM. The device is housed in a 64-pin DIP package, and is CMOS compatible. The part features ROMs for program storage and character generation. The Z86C47 microcontroller may be used in prototyping, low volume applications or where code development is required. Zilog's DTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86C47 architecture utilizes Zilog's advanced Superintegration™ design methodology. The device has an 8-bit internal data path controlled by a Z8 microcontroller, On-Screen Display (OSD) logic circuits/Pulse Width Modulators (PWM). On-chip peripherals include five register/memory mapped I/O ports (Ports 2, 3, 4, 5, and 6), Interrupt control logic (1 software, 2 external and 3 internal interrupts) and a standby mode recovery input port (Port 3, pin P30).

The OSD control circuits support eight rows by 20 columns for 128 kinds of characters. The character color is specified by row. One of the eight rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying high resolution (11 x 15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Seven 6-bit PWM ports are used for controlling audio signal level. Five 8-bit PWM ports are used to vary picture levels.

DTC applications demand powerful I/O capabilities. The Z86C47 fulfills this with 35 I/O pins dedicated to input and output. These lines are grouped into five ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Register File and Data Memory. The Data Memory address space contains a number of control registers for the PWMs, OSD, and I/O Ports 4, 5, and 6. Specifically, there are 13 PWM and eight OSD control registers mapped into the external memory address space. Three I/O registers for Ports 4, 5, and 6 reside in data memory space as well. The Register File is composed of 236 bytes of general purpose register, two I/O Port registers and 15 control and status registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the DTC's offer two on-chip counter/timers with a large number of user selectable modes (see block diagram).

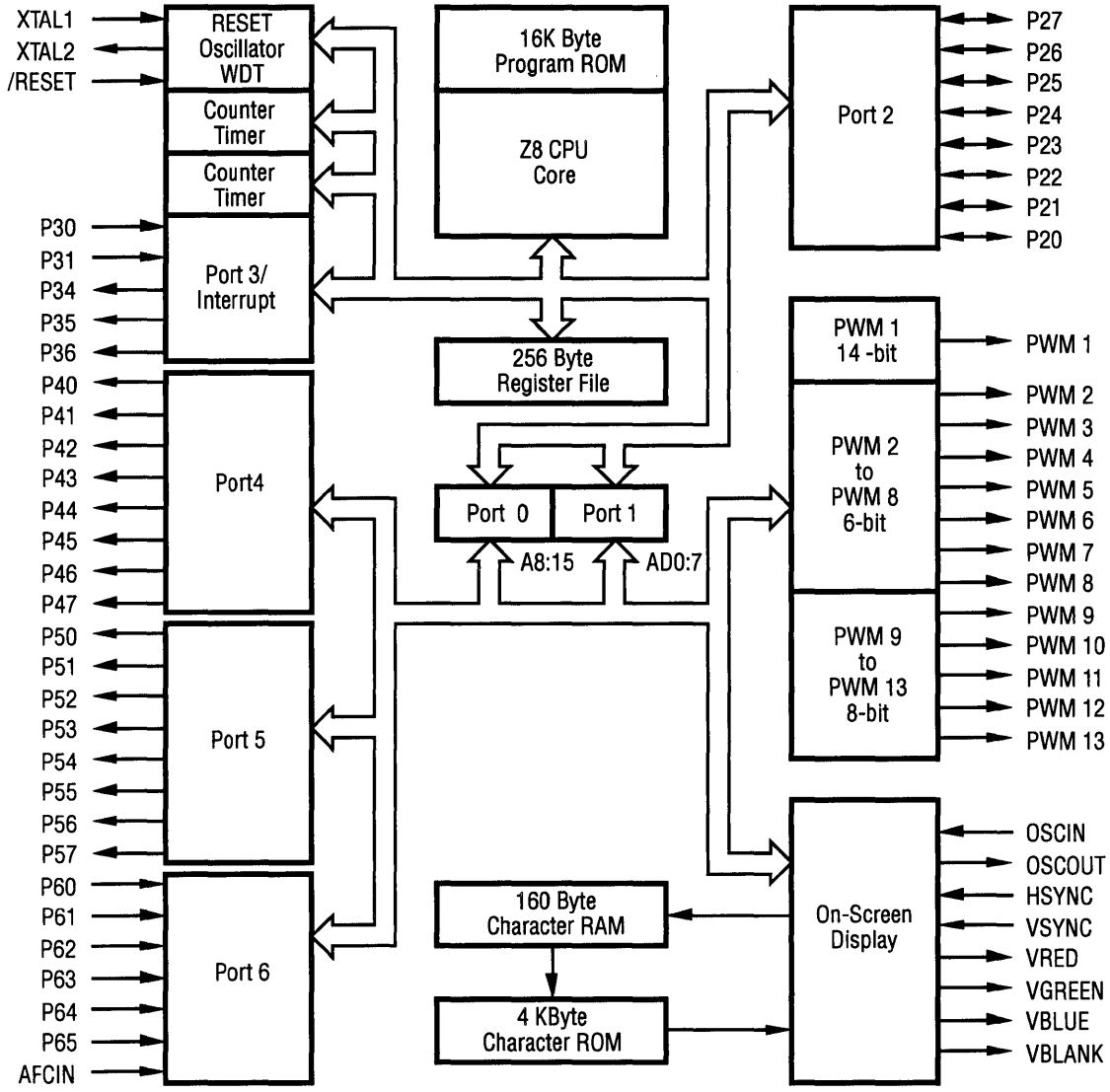
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

6

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z86E47 OTP ROM

CMOS Z8® 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The Z86E47 Digital Television Controller (DTC) introduce a new level of sophistication to single-chip architecture. The Z86E47 is a member of the Z8 single-chip microcontroller family with 16 Kbytes of OTP (One-Time-Programmable) ROM and 236 bytes of RAM. The device is housed in a 64-pin DIP package, and is CMOS compatible. The part features ROMs for program storage and character generation. The Z86E47 microcontroller may be used in prototyping, low volume applications or where code development is required. Zilog's DTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86E47 architecture utilizes Zilog's advanced Superintegration™ design methodology. The device has an 8-bit internal data path controlled by a Z8 microcontroller, On-Screen Display (OSD) logic circuits/Pulse Width Modulators (PWM). On-chip peripherals include five register/memory mapped I/O ports (Ports 2, 3, 4, 5, and 6), Interrupt control logic (1 software, 2 external and 3 internal interrupts) and a standby mode recovery input port (Port 3, pin P30).

The OSD control circuits support eight rows by 20 columns for 128 kinds of characters. The character color is specified by row. One of the eight rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying high resolution (11x15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Seven 6-bit PWM ports are used for controlling audio signal level. Five 8-bit PWM ports are used to vary picture levels.

DTC applications demand powerful I/O capabilities. The Z86E47 fulfills this with 35 I/O pins dedicated to input and output. These lines are grouped into five ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Register File and Data Memory. The Data Memory address space contains a number of control registers for the PWMs, OSD, and I/O Ports 4, 5, and 6. Specifically, there are 13 PWM and eight OSD control registers mapped into the external memory address space. Three I/O registers for Ports 4, 5, and 6 reside in data memory space as well. The Register File is composed of 236 bytes of general purpose register, two I/O Port registers and 15 control and status registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the DTC's offer two on-chip counter/timers with a large number of user selectable modes (see block diagram).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

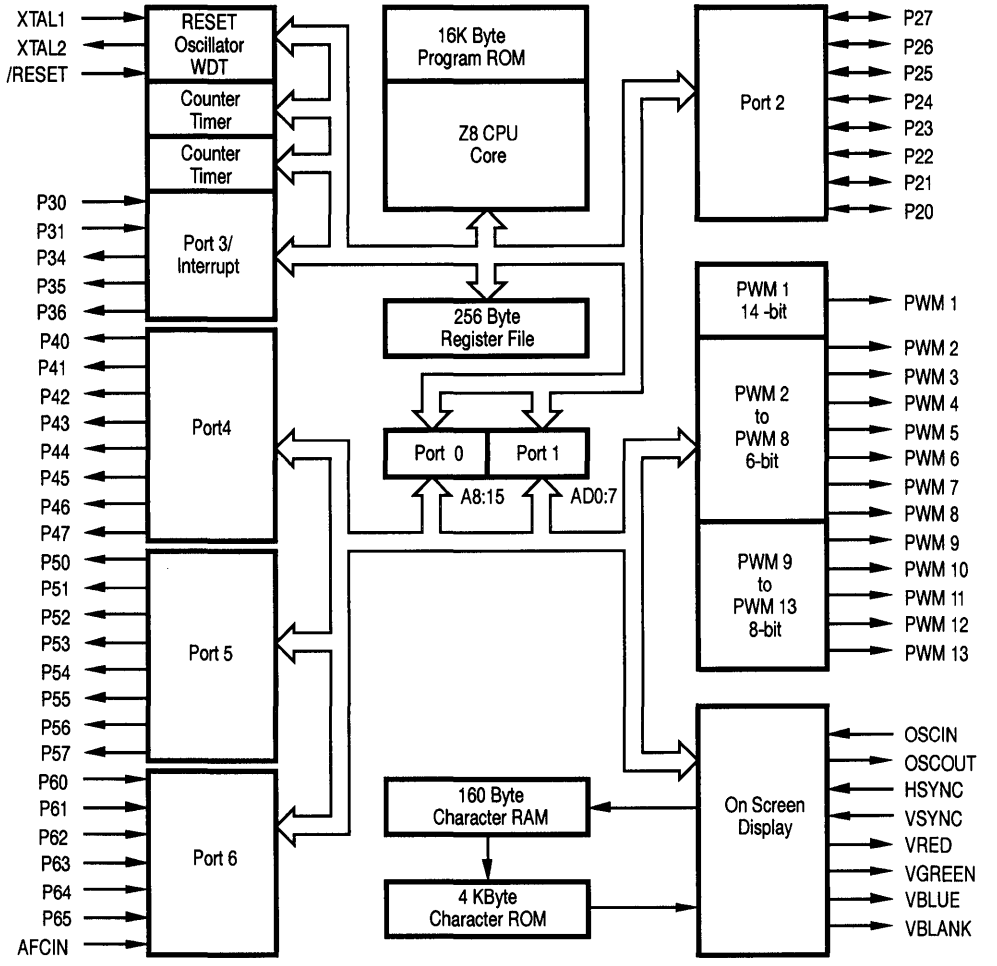
PRODUCT RECOMMENDATIONS

Zilog recommends the following programming equipment for use with this one-time-programmable product.

Device	Zilog Support Tool	Recommended Hardware
Z86E4700ZDP	Z86E47 Programming Adapter	A

Some non-Zilog programmers may have different programming waveforms, voltages and timings and not all programmers may meet the programming requirements of Zilog's one-time-programmable products.

If difficulty is encountered in programming a Zilog OTP product, please contact your local Zilog sales office.



Functional Block Diagram

Z86127

LOW-COST DIGITAL TELEVISION CONTROLLER (LDTC)

FEATURES

8-Bit CMOS Microcontroller for Consumer Television Applications.

- 64-Pin DIP Package
- Low-Cost
- Low Power Consumption
- Fast Instruction Pointer - 1.5 µs @ 4 MHz
- Two Standby Modes - STOP and HALT
- Low Voltage Detection/Voltage Sensitive Reset
- 35 Input/Output Lines
- Port 2 (8-Bit Programmable I/O) and Port 3 (2-Bit Input, 3-Bit Output) Register Mapped Ports.
- Port 5 (8-Bit LED Drive Output) and Port 6 (6-Bit Input and Tri-State Comparator AFC Input) Memory Mapped I/O Ports.
- All Digital CMOS Levels Schmitt-Triggered
- 8 Kbytes of ROM
- 236 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers Each With 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speed up to 4 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.
- Permanently Enabled Watch-Dog/Power-On Reset Timer

On-Screen Display Controller

- 4K x 6-Bit Character Generator ROM
- 160 x 7-Bit Video RAM
- Mask Programmable 128-Character Set Displayed in an 8-Row x 20-Column Format, 12 x 15 Pixel Character Cell, Capable of Supporting English, Korean, Chinese, and Japanese High Resolution Characters.
- Fully Programmable Color Attributes Including Row Character, Row Background/Fringes, Frame Background/Position, Bar Graph Color Change, and Character Size.
- Programmable Display Position and Character Size Control.
- One Pulse Width Modulator (14-Bit Resolution) for Voltage Synthesis Tuner Control.
- Five Pulse Width Modulators (8-Bit Resolution) for Picture Control.
- Three Pulse Width Modulators (6-Bit Resolution) for Audio Control.

GENERAL DESCRIPTION

The Z86127 Low-Cost Digital Television Controller (LDTC) introduces a new level of sophistication to single-chip architecture. The Z86127 is a member of the Z8® single-chip microcontroller family with 8 Kbytes of ROM and 236 bytes of RAM. The device is housed in a 64-Pin DIP package, in which only 52 are active, and are CMOS compatible. The LDTC offers mask programmed ROM which enables the Z8 microcontroller to be used in a high-volume production application device embedded with a custom program (customer supplied program).

GENERAL DESCRIPTION (Continued)

Zilog's LDTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86127 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The device has an 8-bit internal data path controlled by a Z8 microcontroller and On-Screen Display (OSD) logic circuits/ Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Port 2 and 3), interrupt control logic (one software, two external and three internal interrupts), and a standby mode recovery input port (Port 3, P30).

The OSD control circuits support 8 rows by 20 columns of characters. The character color is specified by row. One of the eight rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying high resolution (11 x 15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Three 6-bit PWM ports are used for controlling audio signal levels. Five 8-bit PWM ports are used to vary picture levels.

The Z86127 have 27 I/O pins dedicated to input and output for LDTC applications demanding powerful I/O capabilities. These lines are grouped into four ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Video RAM, and Register File. The Register File is composed of 236 bytes of general-purpose registers, two I/O Port registers, 15 control and status registers and three reserved registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the Z86127 offers two on-chip counter/timers with a large number of user selectable modes.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

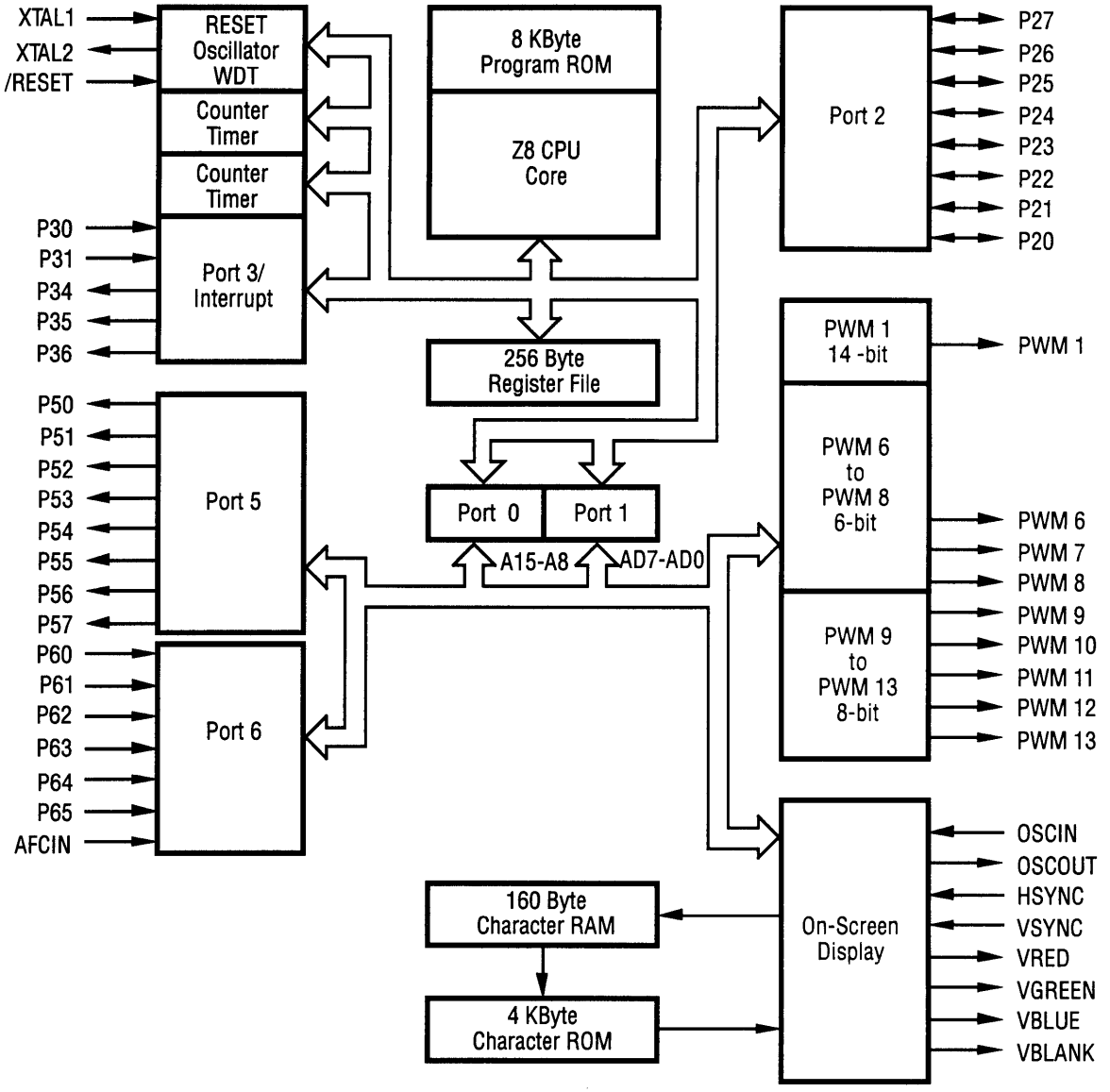


Figure 1. Functional Block Diagram

6

Z86128/Z86228

L21C™ LINE 21 CLOSED-CAPTION CONTROLLER

FEATURES

- Complete Stand-Alone Line 21 Closed-Caption Controller which Conforms to FCC Line 21 Closed-Caption Specifications of April 12, 1991
- Compatible with Electronics Industry Association's Recommended Practice 608 (RP-608) for Extended Data Services (EDS) Captions, and Text in Field 2*. (*Z86228 only)
- Displays Data in Ten Different Modes; CC1-CC4; T1-T4, and Extended Data Services* (*Z86228 only)
- Optional Serial/Parallel Interface
- On-board Analog Sync and Data Slicer
  - No External Analog Required
- CMOS VLSI Design for Low Power and Low Cost
- On-Board Display RAM
- Odd or Even Field Selectable in Serial Control Mode
- On-Board Character Font ROM - 12 x 18 Character in 16 x 26 Cell
- Visual Attributes
  - Color
  - Underline
  - Italic
  - Blink
- Smooth Scrolling
- Valid Line 21 Input Detection
- Automatic Screen Blanking after 1.5 Seconds with no Valid Input (Auto Blanking)
- Automatic Caption Display RAM Erase after 16 seconds with no Valid Input
- 18-Pin DIP Package
- Automatic Erase on Channel Change
- Requires only Two Inputs to Operate
  - Composite Video
  - Any Horizontal Timing Pulse

GENERAL DESCRIPTION

Z86128

The Z86128 (Line 21 Closed-Caption Controllers) is a single I.C. designed to provide the functional performance of a L21C Decoder module (Figure 1). This Superintegration™ VLSI device is completely self contained and only requires a composite video signal and a horizontal SYNC signal as inputs. An "external keyer", i.e., video signal switch between TV RGB and Closed-Caption RGB (Figure 5) is used to produce captioned video. It is fabricated using standard CMOS technology and designed to achieve the lowest possible cost.

The Z86128 is intended for use in a set-top decoder or in any television receiver conforming to the NTSC standard. It is capable of processing and displaying all standard L21C format transmissions including the codes specified by the FCC "Report and Order" on GEN Docket No. 91-1, dated April 12, 1991. If and when PAL and SECAM TV standards define a protocol using the Line 21 format, this design will be readily convertible to that standard.

GENERAL DESCRIPTION (Continued)

Z86228

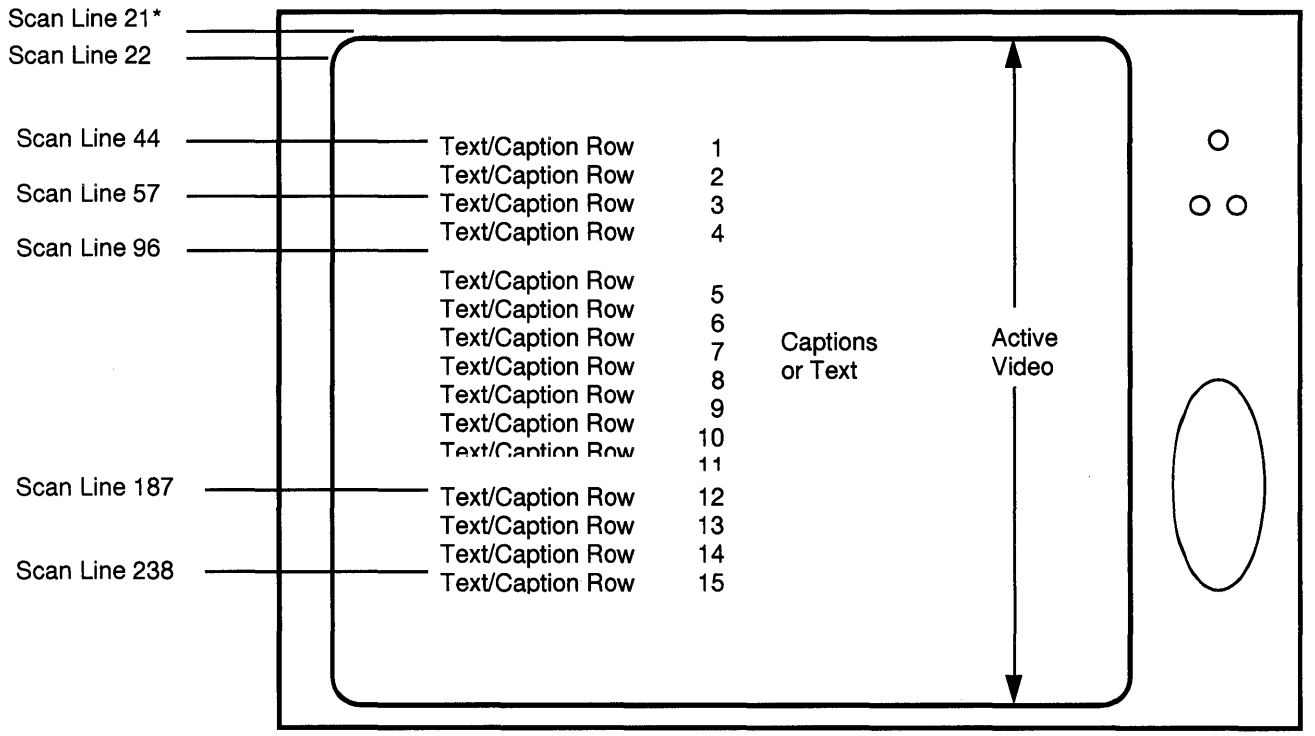
The Z86228 is Zilog's second generation Line 21 decoder suitable for use in television receivers, VCRs, and set-top decoders designed to operate according to NTSC standards. Information encoded on line 21 of both video fields is processed simultaneously to provide ten different display modes. Caption channels 1 through 4 (CC1-CC4), TEXT modes 1 through 4 (T1-T4), and two Extended Data Services (EDS) display modes are supported by the device. The 86228 offers full compliance the FCC's requirements for closed caption display as specified in FCC Report and Order on Gen Docket No. 91-1 dated April 12, 1991 and EIA-608 recommended practices for CAPTIONS, TEXT, and EDS in field 2.

In addition, the device conforms to the Electronic Industry Association's Recommended Practice 608 (RP-608) which provides supplemental guidelines for the transmission and display of captions, text, and extended data services on NTSC field 2.

The Z86228 is pin compatible with Zilog's Z86128 Closed Caption Controller. In addition, the Z86228 operates as a Line 21, field 2 decoder when the data transmission conforms to EIA-608. Extended Data Services (EDS) packets encoded on field 2 may be displayed in either of two screen formats. It should be noted that the display of EDS packets can only be enabled through the Serial Control Port.

The Line 21 Closed Captioning System

The L21C system provides for the transmission of CAPTION information and other TEXT material as an encoded composite data signal. This is during the unblanked portion of Line 21, Field 1, of the standard NTSC video signal. In addition, a framing code is transmitted during the first half of Line 21, Field 2. The encoded composite video signal for Line 21, Field 1 and 2, is shown in Figure 2. The video signal conforms to the Standard Synchronizing Waveform for Color Transmission given in Sub-part E, Part 73 of the FCC Rules and Regulations.



*Scan Line 21 is the last scan line of the vertical retrace blank interval

Figure 1. Closed-Caption TV Display Format

Z86129/130/131

NTSC LINE 21 DECODER

FEATURES

Devices	Speed (MHz)	Pin Count/ Package Types	Standard Temp. Range	On-Screen Display & Closed Captioning	Automatic Data Extraction V-Chip	Time of Day
Z86129	12	18-Pin DIP, SOIC	0° to +70°C	Yes	Yes	Yes
Z86130	12	18-Pin DIP, SOIC	0° to +70°C	No	Yes	Yes
Z86131	12	18-Pin DIP, SOIC	0° to +70°C	No	No	Yes

- Complete Stand-Alone Line 21 Decoder for Closed-Captions and Extended Data Services (XDS).
- Preprogrammed to Provide Full Compliance with EIA-608 Specifications for Extended Data Services.
- Automatic Extraction and Serial Output of Special XDS Packets such as Time of Day, Local Time Zone, and Program Rating (**V-Chip**).
- Cost-Effective Solution for NTSC Violence Blocking inside Picture-in-Picture (PiP) Windows.
- Minimal Communications and Control Overhead Provides Simple Implementation of Violence Block, Closed Caption, and Auto Clock Set Features.
- Programmable, Full Screen On-Screen Display (OSD) for Creating OSD or Captions inside a Picture-in-Picture (PiP) Window (Z86129 only).
- I^2C Serial Data and Control Communication
- User-Programmable Horizontal Display Position for easy OSD Centering and Adjustment (Z86129 only).

GENERAL DESCRIPTION

The Z86129/130/131 is a stand-alone integrated circuit, capable of processing Vertical Blanking Interval (VBI) data from both fields of the video frame in data conforming to the transmission format defined in the Television Decoder Circuits Act of 1990 and in accordance with the Electronics Industry Association specification 608 (EIA-608).

The Line 21 data stream can consist of data from several data channels multiplexed together. Field 1 has four data channels, two Captions and two Text. Field 2 has five additional data channels, two Captions, two Text and Extended Data Services (XDS). XDS data structure is defined in EIA-608. The Z86129 can recover and display data transmitted on any of these nine data channels. The Z86130 and Z86131 are derivatives of the Z86129 which can recover XDS data and output the recovered data via the serial port. The Z86130 and Z86131 do not have OSD capability, but are ideally suited for Line 21 data slicer applications.

The Z86129/130/131 can recover and output to a host processor via the I^2C serial bus any XDS data packet defined in EIA-608. On-chip XDS filters are fully programmable, enabling recovery of only those XDS data packets selected by the user, making the Z86129/130 an ideal choice for implementing NTSC Violence Block. The Z86131 is designed especially for extracting XDS time information for Automatic Clock-Set features in TVs, VCRs, and Set-Top boxes.

In addition, the Z86129/130 is ideally suited to monitor Line 21 of video displayed in a PiP window for violence blocking purposes. A block diagram of the Z86129/130/131 is shown in Figure 1.

GENERAL DESCRIPTION (Continued)

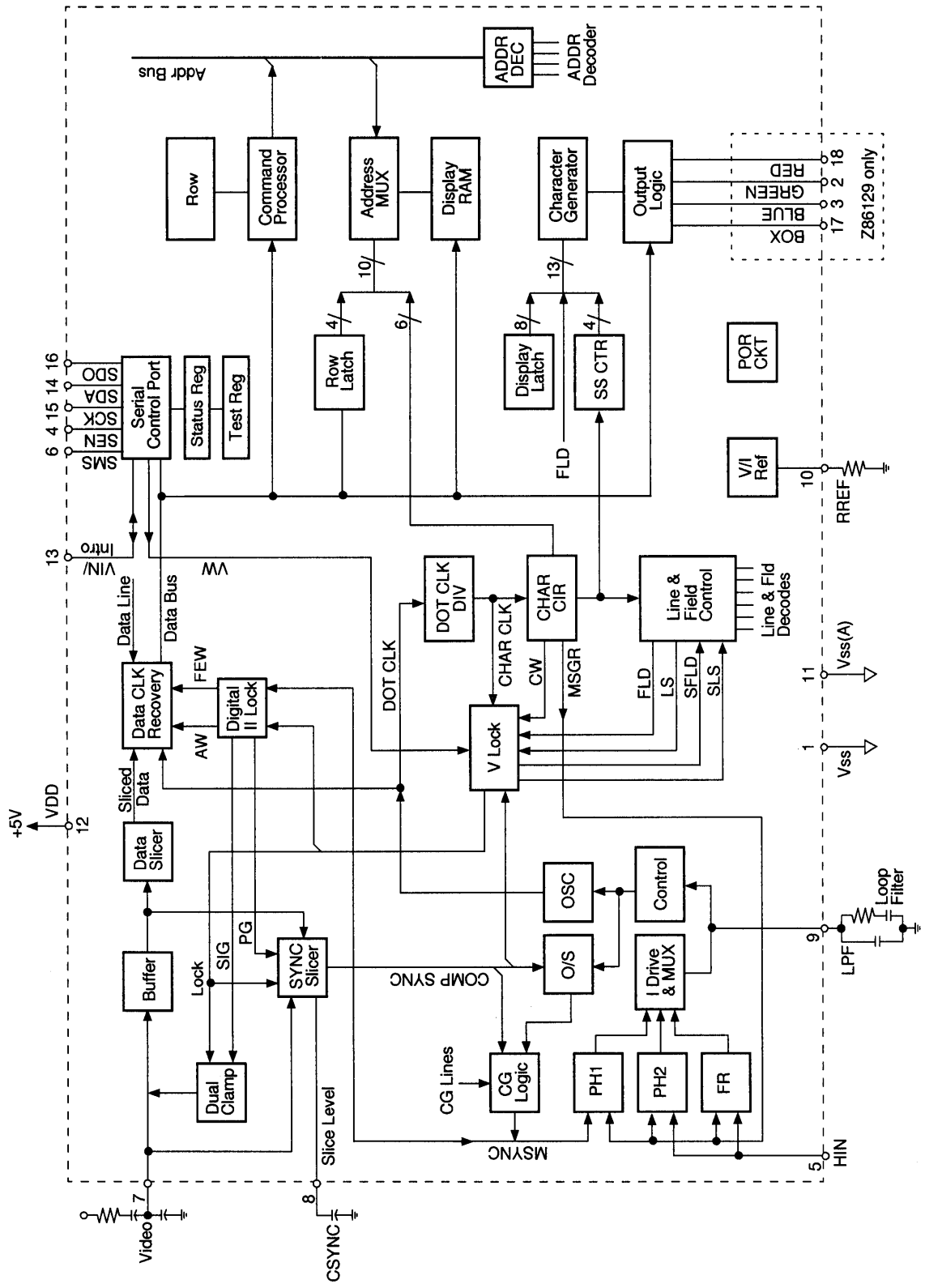


Figure 1. Z86129 Block Diagram

Z86160
SET-TOP CONTROLLER

FEATURES

Part	ROM Kbytes	RAM* Bytes	Speed	Package Information
Z86160	32	768	16	100-Pin QFP

*General-Purpose

- 3.0- to 5.5-Volt Operating Range
- Low-Power Consumption
- Custom Input/Output Lines
- 0°C to +70°C Temperature Range
- 512 Bytes Battery Backed-Up (BBU) Secure RAM
- Keypad Buffer
- LED Controller
- Two Comparators
- Two On-Chip Counter/Timers

GENERAL DESCRIPTION

The Z86160 is a member of the Z8® single-chip microcontroller family offering a unique architecture that is characterized by Zilog's 8-bit microcontroller core.

This CMOS microcontroller features fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low-cost and low-power consumption.

For applications demanding powerful I/O capabilities, the Z86160 fulfills this with custom I/O, specifically tailored to meet the needs of set-top requirements.

Four basic address spaces, the Program Memory, Data Memory, 236 General-Purpose Registers, and 512 bytes of protected RAM, support a wide range of memory configurations. The protected RAM is mapped into data memory.

To unburden the program from coping with real-time problems such as counting/timing, and serial data communications, the Z86160 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Block Diagram).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION

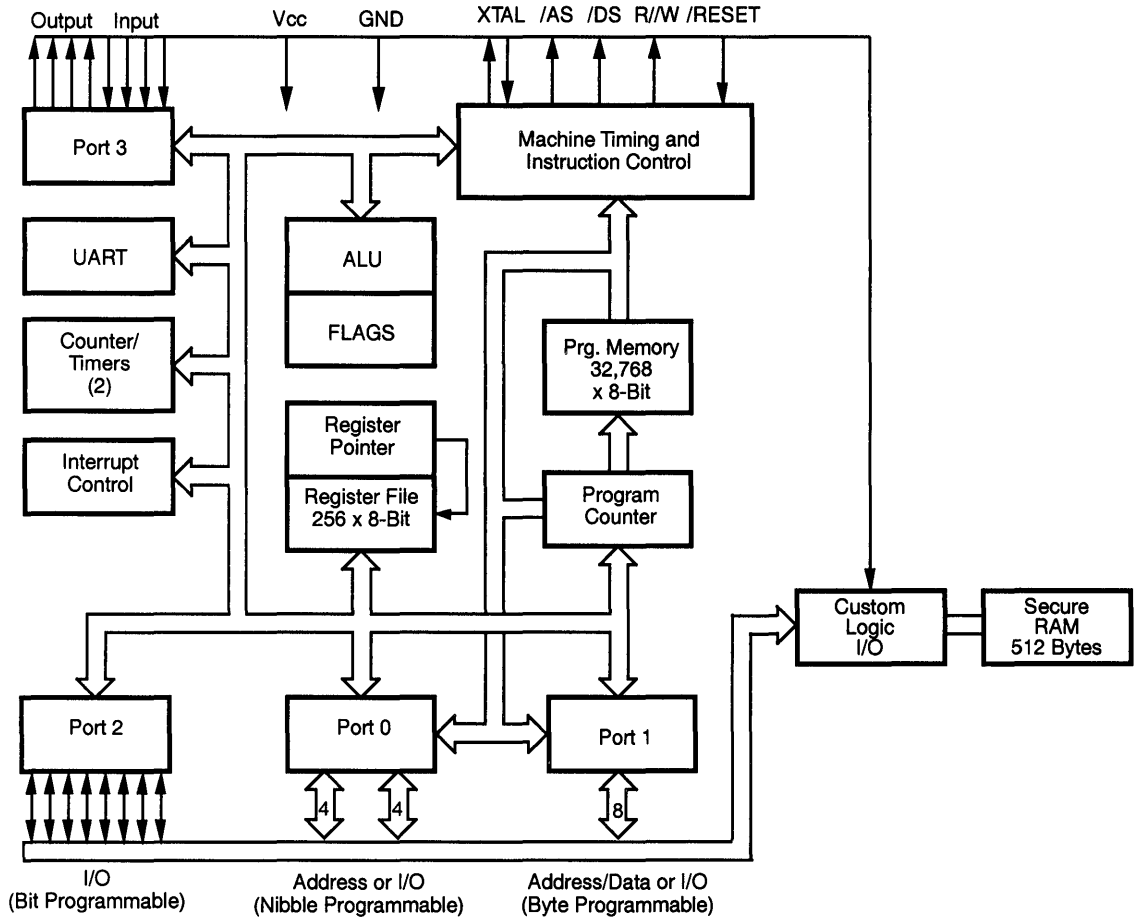


Figure 1. Z86160 Functional Block Diagram

Z86227

40-PIN LOW-COST DIGITAL TELEVISION CONTROLLER (4LDTC™)

FEATURES

8-Bit CMOS Microcontroller for Consumer Television, Cable and Satellite Receiver Applications.

- 40-Pin DIP Package
- Low Power Consumption
- Fast Instruction Pointer - 1.5 µs @ 4 MHz
- Two Standby Modes - STOP and HALT
- Low Voltage Detection/Voltage Sensitive Reset
- 24 Input/Output Lines
- Port 2 (8-Bit Programmable I/O) and Port 3 (2-Bit Input, 3-Bit Output) Register Mapped Ports
- Port 6 (6-Bit Input and Tri-State Comparator AFC Input) Memory Mapped I/O Ports
- All Digital CMOS Levels Schmitt-Triggered
- 6 Kbytes of ROM
- 236 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speed up to 4 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive
- Permanently Enabled Watch-Dog/Power-On Reset Timer

On-Screen Display Controller

- 3K x 6-Bit Character Generator ROM
- 120 x 7-Bit Video RAM
- Mask Programmable 96-Character Set Displayed in an 6-Row x 20-Column Format, 12 x 15 Pixel Character Cell, Capable of Supporting English, Korean, Chinese and Japanese High Resolution Characters.
- Fully Programmable Color Attributes Including Row Character, Row Background/Fringes, Frame Background/Position, Bar Graph Color Change, and Character Size.
- Programmable Display Position and Character Size Control
- One Pulse Width Modulator (14-Bit Resolution) for Voltage Synthesis Tuner Control.
- Three Pulse Width Modulator (8-Bit Resolution) for Picture Control
- Three Pulse Width Modulators (6-Bit Resolution) for Audio Control

6

GENERAL DESCRIPTION

The Z86227 40-pin Low-Cost Digital Television Controller (4LDTC™) introduces a new level of sophistication to single-chip architecture. The Z86227 is a member of the Z8® single-chip microcontroller family with 6 Kbytes of ROM and 236 bytes of RAM. The device is offered in a 40-pin package and is CMOS compatible. The 4LDTC offers mask programmed ROM which enables the Z8® microcontroller to be used in a high volume production application device embedded with a custom program (customer supplied program) and combines together with the Z86C27 (DTC) and Z86127 (LDTC) to provide support for high end, mid range and low end TV applications.

GENERAL DESCRIPTION (Continued)

Zilog's 4LDTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86227 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The device has an 8-bit internal data path controlled by a Z8 microcontroller and On Screen Display (OSD) logic circuits and Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and 3), interrupt control logic (one software, two external and three internal interrupts) and a standby mode recovery input port (Port 3, P30).

The OSD control circuits support 6 rows x 20 columns of characters. The character color is specified by row. One of the six rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying either low resolution (5 x 7 dot pattern) or high resolution (11 x 15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Three 6-bit PWM ports are used for controlling audio signal levels. Three 8-bit PWM ports used to vary picture levels.

For 4LDTC applications demanding powerful I/O capabilities, the Z86227 fulfills this with 24 I/O pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Video RAM, and Register File. The Register File is composed of 236 bytes of general-purpose registers, two I/O Port registers, 15 control and status registers and three reserved registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the 4LDTC offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

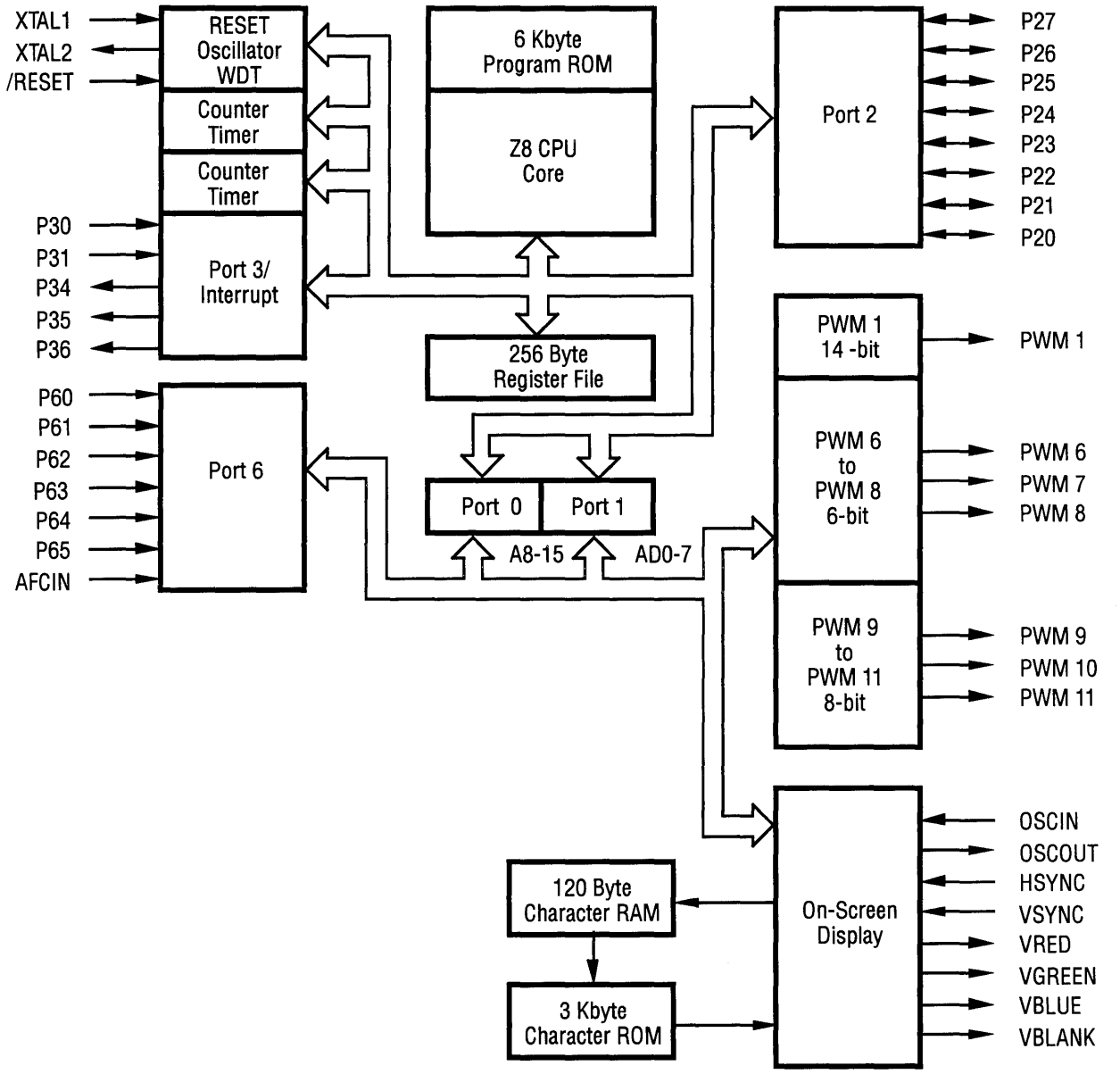


Figure 1. Functional Block Diagram

6

Z86247

40-PIN LOW-COST DIGITAL TELEVISION CONTROLLER (4LDTC)

GENERAL DESCRIPTION

The Z86247 40-pin Low-Cost Digital Television Controller (4LDTC) introduces a new level of sophistication to single-chip architecture. The Z86247 is a member of the Z8® single-chip microcontroller family with 8 Kbytes of ROM and 236 bytes of RAM. The device is offered in a 40-pin package and is CMOS compatible. The 4LDTC offers mask programmed ROM which enables the Z8 microcontroller to be used in a high volume production application device embedded with a custom program (customer supplied program) and combines together with the Z86C27 (DTC) and Z86127 (LDTC) to provide support for high end, mid range and low end TV applications.

Zilog's 4LDTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86247 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The device has an 8-bit internal data path controlled by a Z8 microcontroller and On Screen Display (OSD) logic circuits and Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and Port 3), interrupt control logic (one software, two external and three internal interrupts) and a standby mode recovery input port (Port 3, pin P30).

The OSD control circuits support 8 rows by 20 columns of characters. The character color is specified by row. One of the eight rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying high resolution (11x15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Three 6-bit PWM ports are used for controlling audio signal levels. Three 8-bit PWM ports used to vary picture levels.

The 4LDTC applications demand powerful I/O capabilities. The Z86247 fulfills this with 24 pins dedicated to input or output. These lines are grouped into three ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Video RAM, and Register File. The Register File is composed of 236 bytes of general purpose registers, two I/O Port registers, 15 control and status registers and three reserved registers.

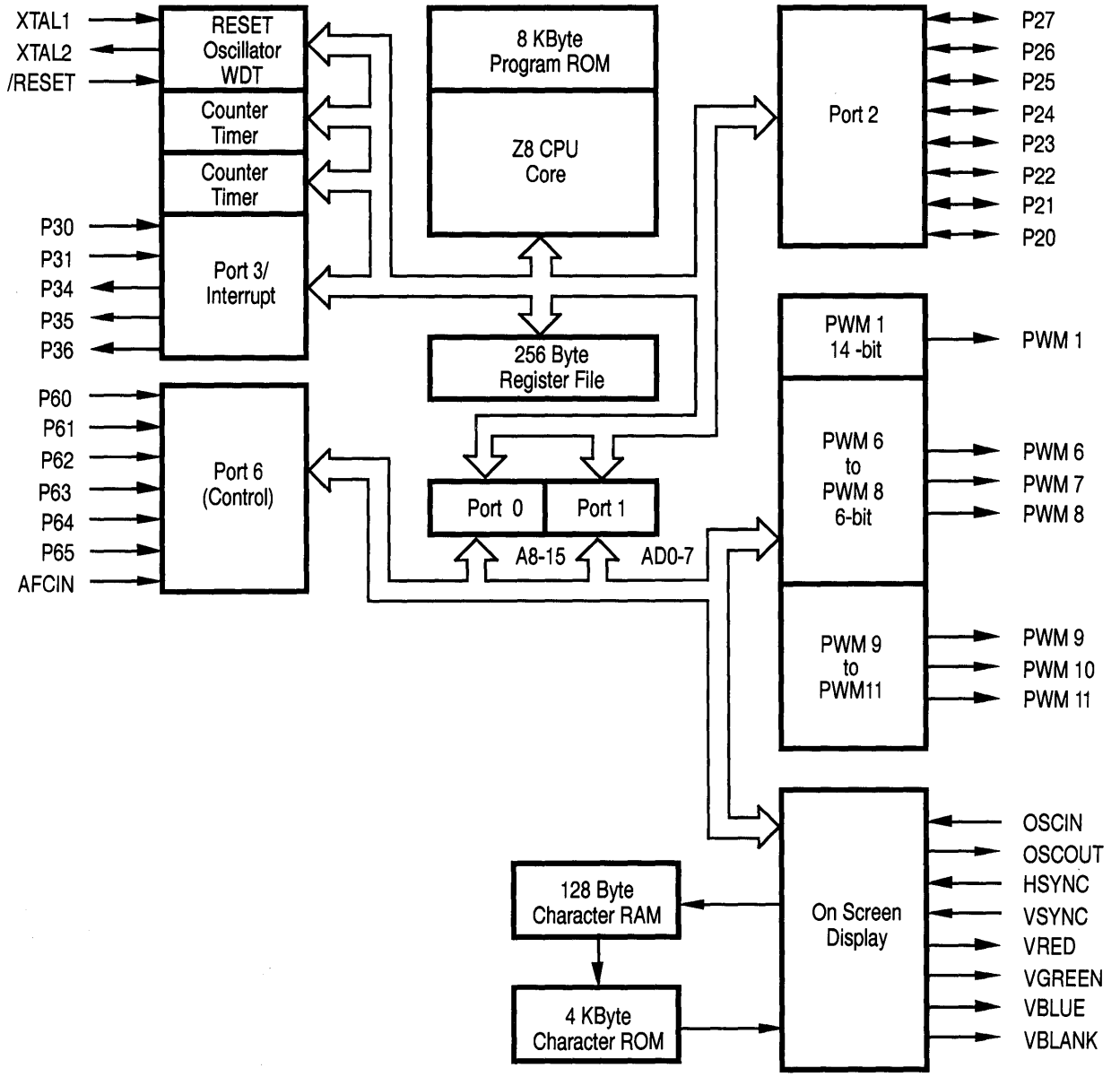
To unburden the program from coping with the real-time problems such as counting/timing and data communication, the 4LDTC offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z86250
STARSIGHT DATABASE ENGINE

FEATURES

- **Part** Z86250 — **Package** 84-Pin PLCC — **Speed (MHz)** 24
- 4.3- to 5.5-Volt Operating Range
- 0°C to +70°C Temperature Range
- Low-Power Consumption
- Segmented Base Registers
- Infrared Receiver Logic
- CRC-32 Encoding and Decoding Logic
- Watch-Dog Timer (WDT) for Error Recovery
- Serial I.M. and I²C Compatible Bus for External Communication
- Test Multiplexer for Chip Debug

GENERAL DESCRIPTION

Zilog's Z86250 StarSight Data Base Engine (DBE) is designed to process extracted data for the StarSight on-screen programming guide. The device is logically equivalent to the DBE1200 for StarSight applications.

The Z86250 provides a number of important peripheral functions, such as the IR Blaster to send command signals to the VCR, and low-power management to avoid loss of data.

For fast memory data manipulation, the Z86250 offers segmented base registers. The device also features PSRAM memory control and refresh logic.

The DBE is optimized to work with Zilog's Z89300 series of TV controller devices to provide a cost-effective solution for StarSight programming-guide data extraction and display.

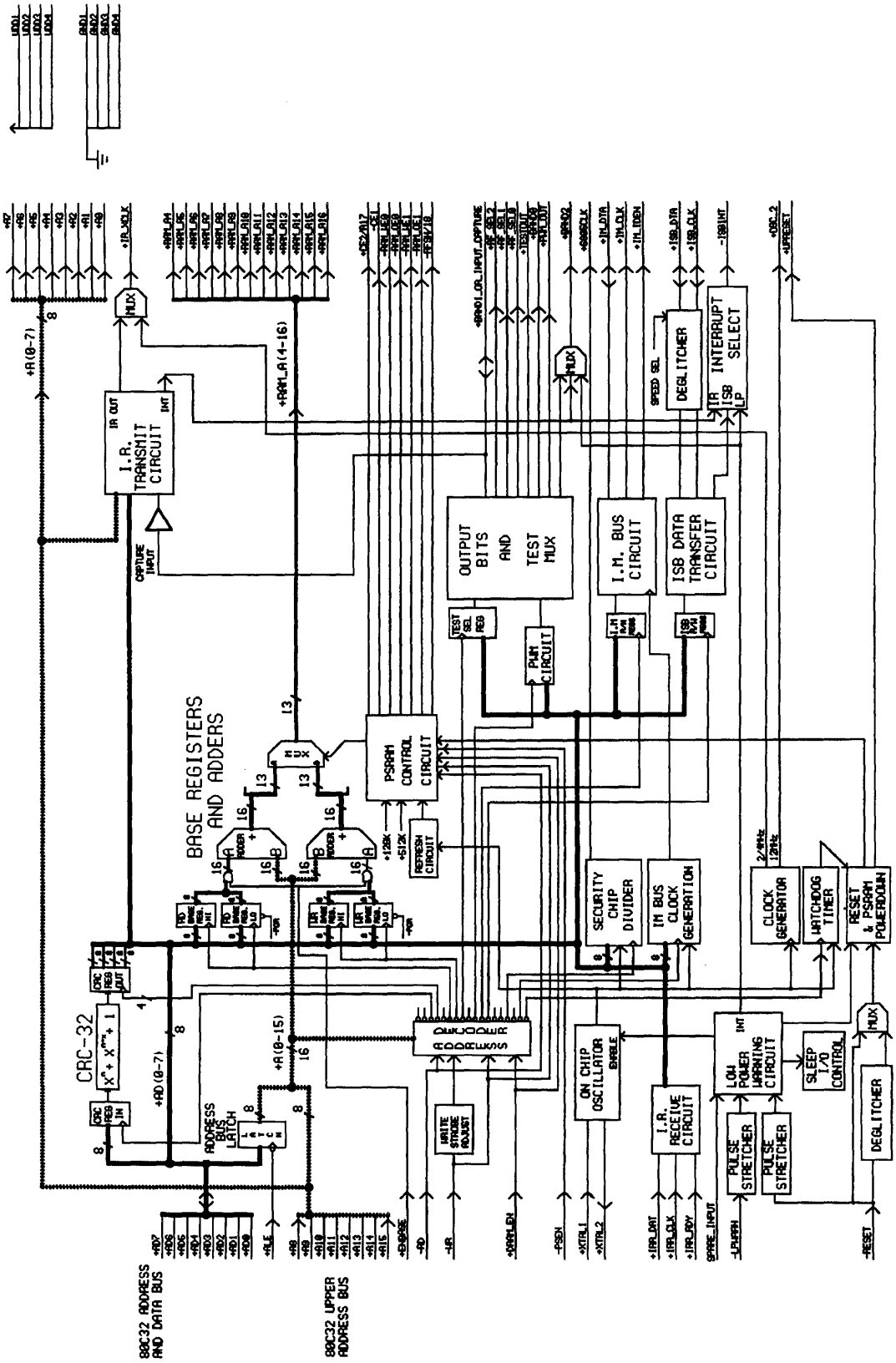
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

6

GENERAL DESCRIPTION (Continued)



Database Engine Block Diagram

Z86251
STARSIGHT DATABASE ENGINE

FEATURES

- **Part** Z86251 — **Package** 68-Pin PLCC — **Speed (MHz)** 24
- 4.5- to 5.5-Volt Operating Range
- 0°C to +70°C Temperature Range
- Low-Power Consumption
- Segmented Base Registers
- DRAM Memory Control and Refresh Logic
- Power-Down DRAM Data Retention
- Infrared Transmitter Circuits for TV and VCR Control
- CRC-32 Encoding and Decoding Logic
- Watch-Dog Timer (WDT) for Error Recovery
- I^2C Compatible Bus for External Communication
- Test Multiplexer for Chip Debug
- On-Chip Crystal Oscillator

GENERAL DESCRIPTION

Zilog's Z86251 StarSight Data Base Engine (DBE) is designed to process extracted data for the StarSight on-screen programming guide.

The Z86251 provides a number of important peripheral functions, such as the IR Blaster to send command signals to the VCR, and low-power management to avoid loss of data.

For fast memory data manipulation, the Z86251 offers segmented base registers. The device also features DRAM memory control and refresh logic.

The DBE is optimized to work with Zilog's Z89300 series of TV controller devices to provide a cost-effective solution for StarSight programming-guide data extraction and display.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

6

Z89309
DIGITAL TELEVISION CONTROLLER

GENERAL DESCRIPTION

The Z89309 Digital Television Controller is an application-specific controller designed to provide complete audio and video control of television receivers, video recorders, with advanced on-screen display facilities. The Z89309 is the ROMless ICE chip version of the Z89300 Digital Television Controller family used in emulators and development boards. The powerful 12 MHz Z89C00 RISC processor core allows the user to control the on-board peripheral functions and registers using the standard processor instruction set.

The extensive character attributes can be controlled in two modes: by the on-screen display controller character control mode for maximum display control flexibility, and closed caption mode for optimum display of closed caption text.

Closed caption text can be decoded directly from the composite video signal with the assistance of the processor's digital signal processing capabilities and displayed on the screen. The character representation in this mode allows for a simple attribute control through the insertion of control characters, and each word of RAM specifies two displayed characters.

The character control mode provides access to the full set of attribute controls. Each word of RAM specifies a single displayed character and basic character attributes, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that incude underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency. The 16-bit display character representation allows the modification of some key attributes on a character-by-character basis. The external ROM contents are referenced by a 16-bit word stored in video RAM (VRAM) defining the character type and its key attributes.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tunning adjustments, may be accessed through the industry standard I^2C port.

Additional hardware provides the capability to display two times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Fringing circuitry can be activated to improve the visibiity of text by surrounding the character lines with a one-pixel border.

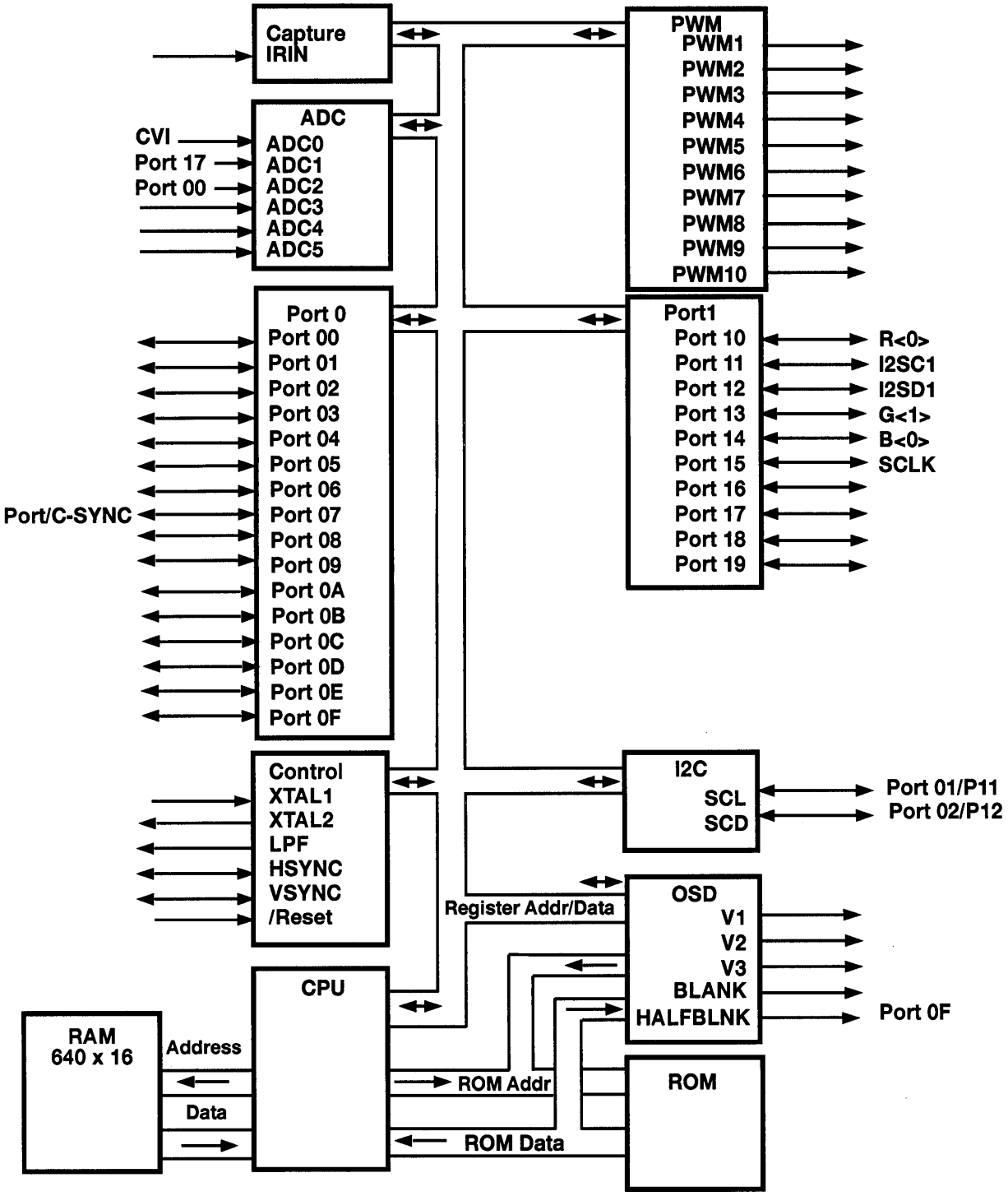
RGB outputs provide the direct video signals, and a blanking output is provided to control the video multiplexor. Dot clock and verticle line synchronization are normally obtained from H_FLYBACK and V_FLYBACK, but can be generated by the Z89309, and driven to the external deflection unit through the bidirectional SYNC ports when external video synchronization signals are not present.

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

Ten PWM ports are available in the 124 PGA package.

The Z89309 has two internal 12 MHz VCOs that are referenced to a 32 KHz internal oscillator to provide the system clock. In Sleep mode, the controller uses the 32 KHz clock for the system clock to reduce power consumption. The processor can be suspended by placing it into STOP mode when main power is not available for minimal power consumption.

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z89313
DIGITAL TELEVISION CONTROLLER

FEATURES

Part Number	ROM (Word)	RAM (Word)	Speed (MHz)
Z89313	32K x 16	1K x 16	12
- 52-Pin Shrink DIP Package
- 4.5- to 5.5-Volt Operating Range
- Z89C00 RISC Processor Core
- 0°C to +70°C Temperature Range
- Direct Closed Caption Decoding
- TV Tuner Serial Interface
- Customized Character Set
- Character Control Mode
- Directly Controlled Receiver Functions

GENERAL DESCRIPTION

The Z89313 is a member of Zilog's family of Digital Television Controllers designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities.

The Z89313 features a powerful Z89C00 RISC processor core that controls on-board peripheral functions and registers using the standard processor instruction set.

In closed caption mode, text can be decoded directly from the composite video signal and displayed on the screen with assistance from the processor's digital signal processing capabilities. The character representation in this mode allows for a simple attribute control through the insertion of control characters.

The character control mode provides access to the full set of attribute controls. The modification of attributes is allowed on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

Display attributes, including underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency, are made possible through a fully customized 512 character set, formatted in two 256 character banks.

Serial interfacing with the television tuner is provided through the tuner serial port. Digital channel tuning adjustments may be accessed through the industry-standard I^2C port.

Additional hardware provides the capability to display two to three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Special circuitry can be activated to improve the visibiity of text by adding a right-sided shadow effect to the characters.

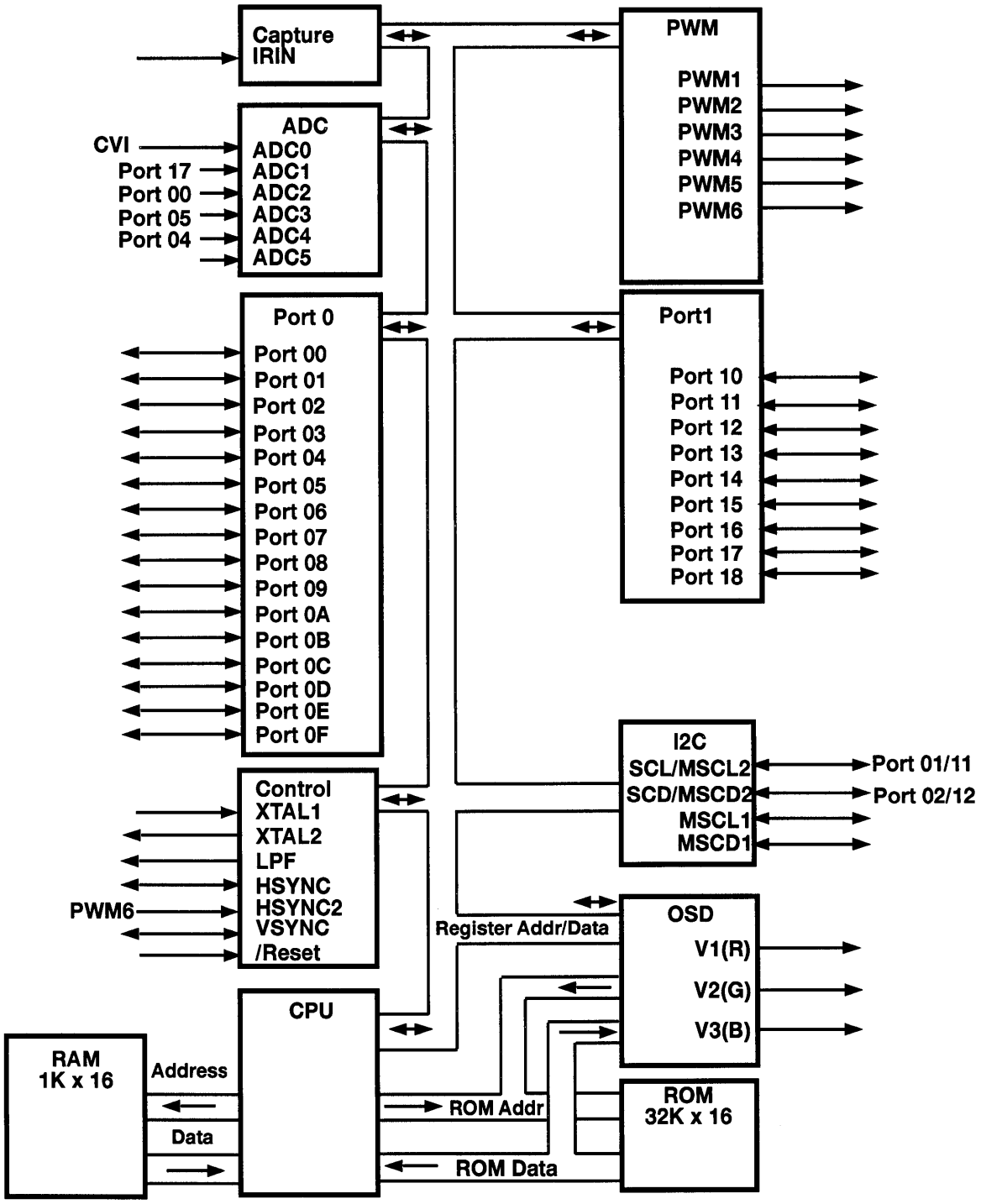
Receiver functions such as color and volume can be directly controlled by six 8-bit pulse width modulated ports.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z89319/328

DIGITAL TELEVISION CONTROLLER IN-CIRCUIT EMULATOR (ICE) DEVICE

FEATURES

Part Number	ROM (Word)	RAM (Word)	Speed (MHz)
Z89319	0	0	12
Z89328	0	0	12

- 124-Pin Grid Array (PGA) Package (Z89319)
  100-Pin Quad Flat Pack (QFP) Package (Z89328)
- 4.5- to 5.5-Volt Operating Range
- Z89C00 RISC Processor Core
- 0°C to +70°C Temperature Range
- Direct Closed Caption Decoding
- TV Tuner Serial Interface
- Customized Character Set
- Character Control Mode
- Directly Controlled Receiver Functions

GENERAL DESCRIPTION

The Z89319 and Z89328 are ROMless versions of the Z89300 family of Zilog's Digital Television Controllers designed for use in emulators and development boards to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities.

The powerful Z89C00 RISC processor core allows users to control on-board peripheral functions and registers using the standard processor instruction set.

In closed caption mode, text can be decoded directly from the composite video signal and displayed on the screen with assistance from the processor's digital signal processing capabilities. The character representation in this mode allows for a simple attribute control through the insertion of control characters.

The character control mode provides access to the full set of attribute controls. The modification of attributes is allowed on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

Display attributes, including underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency, are made possible through a fully customized 512 character set, formatted in two 256 character banks.

Serial interfacing with the television tuner is provided through the tuner serial port. Digital channel tuning adjustments may be accessed through the industry-standard I^2C port.

Additional hardware provides the capability to display two to three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Special circuitry can be activated to improve the visibiity of text by adding a right-sided shadow effect to the characters.

Receiver functions such as color and volume can be directly controlled by six 8-bit pulse width modulated ports.

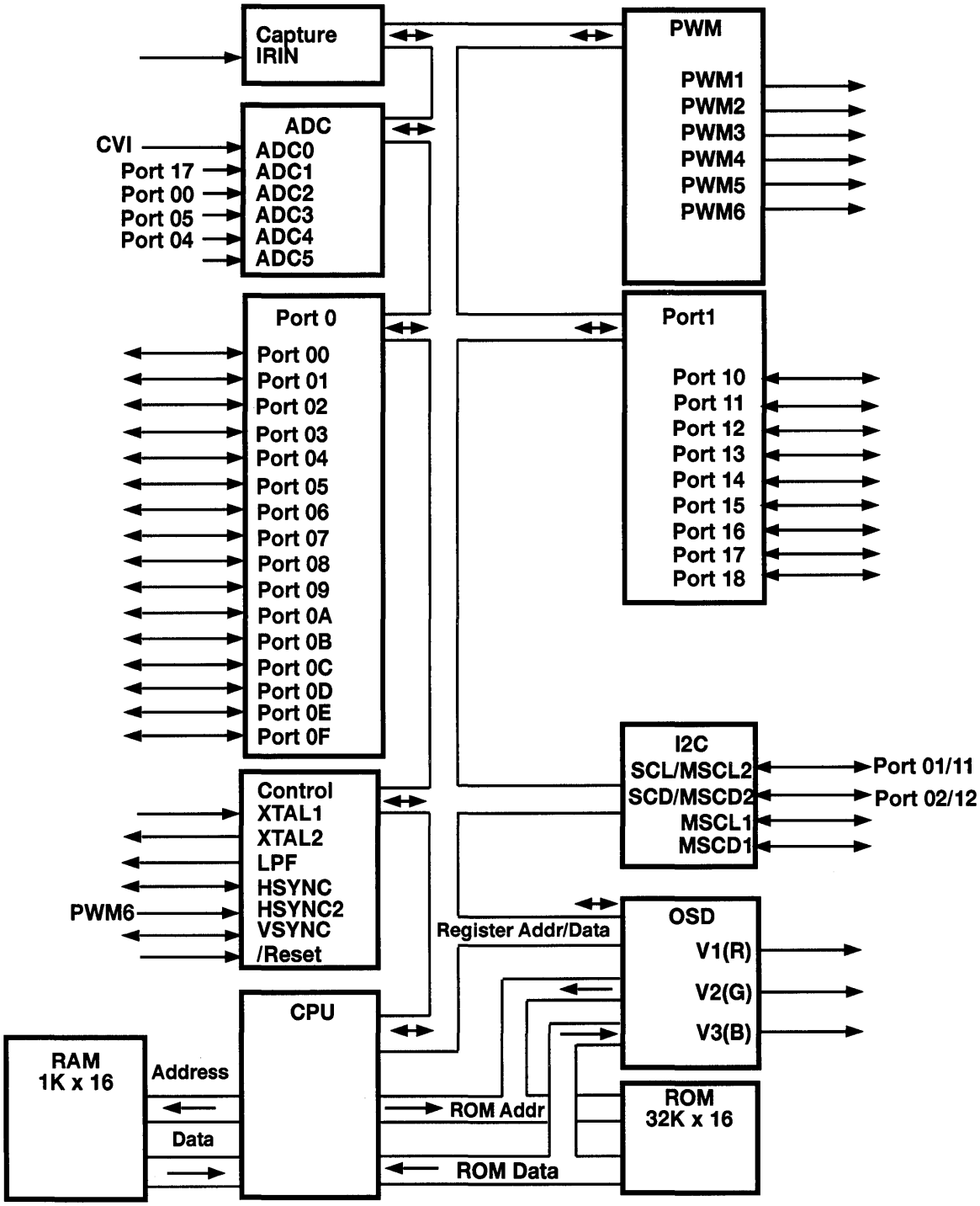
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

6

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z89331
OTP DIGITAL TELEVISION CONTROLLER

FEATURES

Part Number	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z89331	24	640	12

  *General-Purpose
- 42-Pin SDIP Package
- 4.75- to 5.25-Volt Operating Range
- 0°C to +70°C Temperature Range
- One-Time Programmable
- Serial Interfacing I²C Port
- Fully Customized Character Set
- Character-Control and Closed-Caption Modes
- Keypad User Control
- TV Tuner Serial Interface
- Direct Video Signals
- Low-EMI Option

GENERAL DESCRIPTION

The Z89331 One-Time Programmable (OTP) Digital Television Controller is designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities. The Z89331 features a Z89C00 RISC processor core that controls on-board peripheral functions and registers using the standard processor instruction set.

Character attributes can be controlled through two modes: the on-screen display Character-Control Mode and the Closed-Caption Mode. The Character-Control Mode provides access to the full set of attribute controls, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes. Closed-caption text can be decoded directly from the composite video signal and displayed on-screen with the assistance of the processor's digital signal processing (DSP) capabilities.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that include underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tunning adjustments, may be accessed through the industry-standard I²C port.

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

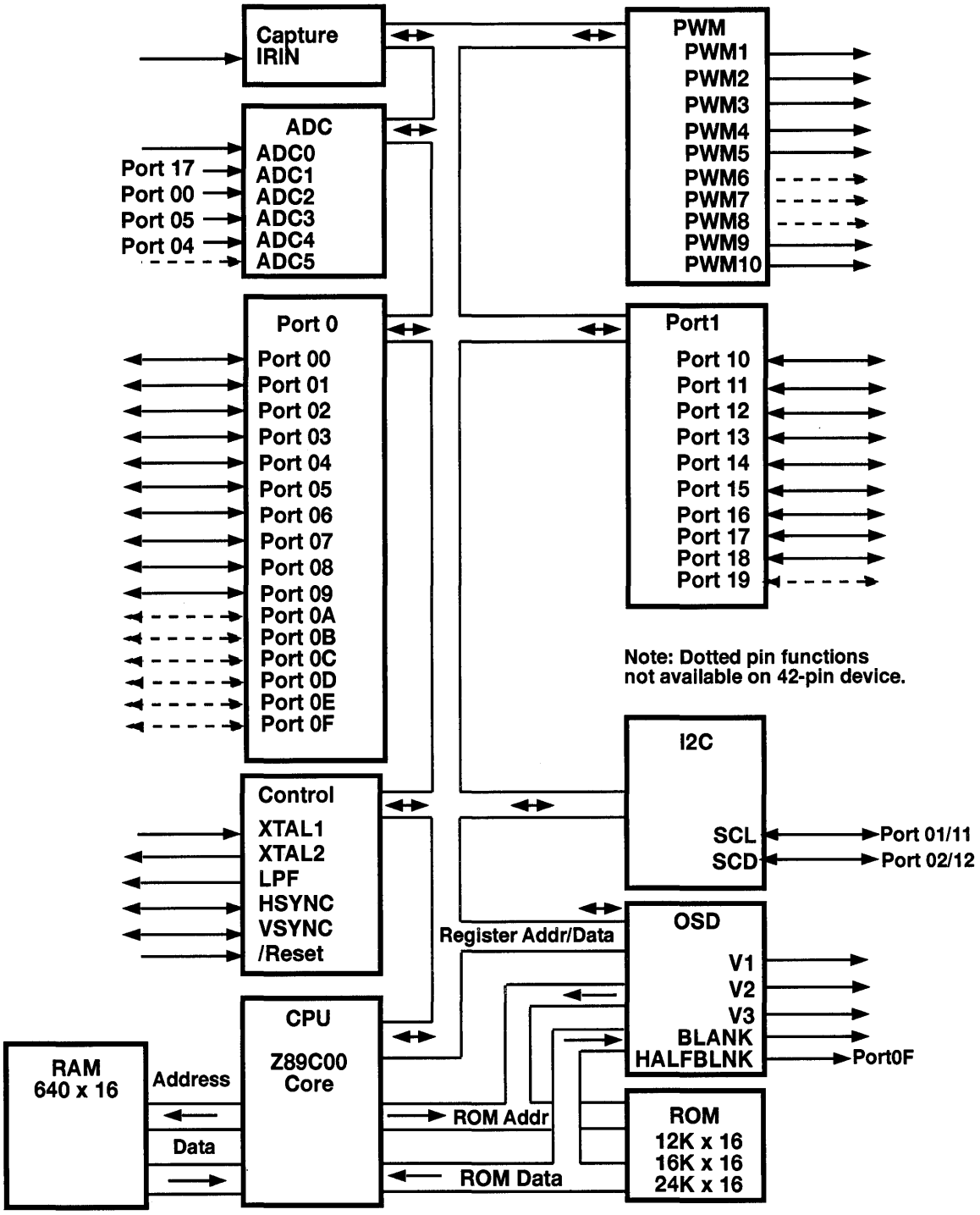
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

6

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z89332

DIGITAL TELEVISION CONTROLLER

FEATURES

Device	ROM (KW)	RAM* (Words)	PWM (8-Bit)	Voltage Range
Z89332	24	640	8	4.5 to 5.5V

Note: *General-Purpose

- 42-Pin SDIP and 48-Pin Ceramic Packages with 42- to 48-Pin Adapter Socket
- 0°C to +70°C Temperature Range
- Fully Customized Character Set
- Character-Control and Closed-Caption Modes
- Keypad User Control
- TV Tuner Serial Interface
- Direct Video Signals
- Speed: 12 MHz

GENERAL DESCRIPTION

The Z89332 Digital Television Controller is designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities. The television controller features a Z89C00 RISC processor core that controls the on-board peripheral functions and registers using the standard processor instruction set.

Character attributes can be controlled through two modes: the on-screen display Character-Control Mode and the Closed-Caption Mode. The Character-Control Mode provides access to the full set of attribute controls, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes. Closed-caption text can be decoded directly from the composite video signal and displayed on-screen with the assistance of the processor's digital signal processing (DSP) capabilities.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that include underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tunning adjustments, may be accessed through the industry-standard I^2C port.

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

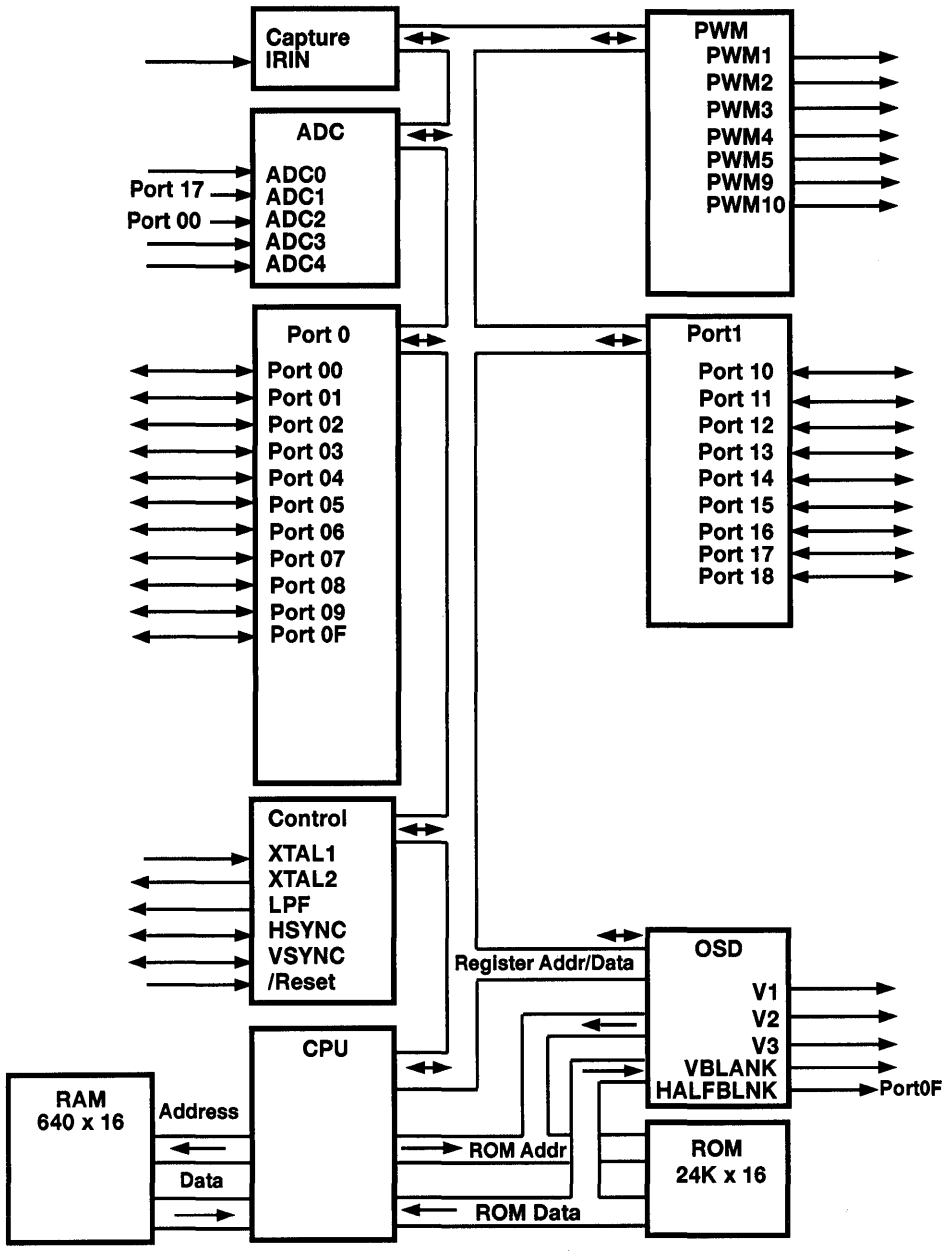


Figure 1. Functional Block Diagram

Z90102/90103/90104

40-PIN LOW-COST DIGITAL TELEVISION CONTROLLER (4LDTC™)

FEATURES

8-Bit CMOS Microcontroller for Consumer Television, Cable and Satellite Receiver Applications.

Part	ROM (KB)	RAM* (Bytes)	I/O	40-pin DIP
Z90102	4	236	24	X
Z90103	6	236	24	X
Z90104	8	236	24	X

*General-Purpose

- Low Power Consumption
- Fast Instruction Pointer - 1.5 µs @ 4 MHz
- Two Standby Modes - STOP and HALT
- Low Voltage Detection/Voltage Sensitive Reset
- Port 2 (8-Bit Programmable I/O) and Port 3 (2-Bit Input, 3-Bit Output) Register Mapped Ports
- Port 6 (6-Bit Input and Tri-State Comparator AFC Input) Memory Mapped I/O Ports
- All Digital CMOS Levels Schmitt-Triggered
- Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speed up to 4 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive
- Permanently Enabled Watch-Dog/Power-On Reset Timer

On-Screen Display Controller

- 3K x 6-Bit Character Generator ROM
- 120 x 7-Bit Video RAM
- Mask Programmable 96-Character Set Displayed in an 6-Row x 20-Column Format, 12 x 15 Pixel Character Cell, Capable of Supporting English, Korean, Chinese and Japanese High Resolution Characters.
- Fully Programmable Color Attributes Including Row Character, Row Background/Fringes, Frame Background/Position, Bar Graph Color Change, and Character Size.
- Programmable Display Position and Character Size Control
- One Pulse Width Modulator (14-Bit Resolution) for Voltage Synthesis Tuner Control.
- Three Pulse Width Modulator (8-Bit Resolution) for Picture Control
- Three Pulse Width Modulators (6-Bit Resolution) for Audio Control

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GENERAL DESCRIPTION

The Z90102/3/4 40-pin Low-Cost Digital Television Controller (4LDTC™) introduces a new level of sophistication to single-chip architecture. The Z90102/3/4 is a member of the Z8® single-chip microcontroller family with 6 Kbytes of ROM and 236 bytes of RAM. The device is offered in a 40-pin package and is CMOS compatible. The 4LDTC offers mask programmed ROM which enables the Z8® microcontroller to be used in a high volume production application device embedded with a custom program (customer supplied program) and combines together with the Z86C27 (DTC) and Z86127 (LDTC) to provide support for high end, mid range and low end TV applications.

GENERAL DESCRIPTION (Continued)

Zilog's 4LDTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z90102/3/4 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The device has an 8-bit internal data path controlled by a Z8 microcontroller and On Screen Display (OSD) logic circuits and Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and 3), interrupt control logic (one software, two external and three internal interrupts) and a standby mode recovery input port (Port 3, P30).

The OSD control circuits support 6 rows x 20 columns of characters. The character color is specified by row. One of the six rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying either low resolution (5 x 7 dot pattern) or high resolution (11 x 15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Three 6-bit PWM ports are used for controlling audio signal levels. Three 8-bit PWM ports used to vary picture levels.

For 4LDTC applications demanding powerful I/O capabilities, the Z90102/3/4 fulfills this with 24 I/O pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Video RAM, and Register File. The Register File is composed of 236 bytes of general-purpose registers, two I/O Port registers, 15 control and status registers and three reserved registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the 4LDTC offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

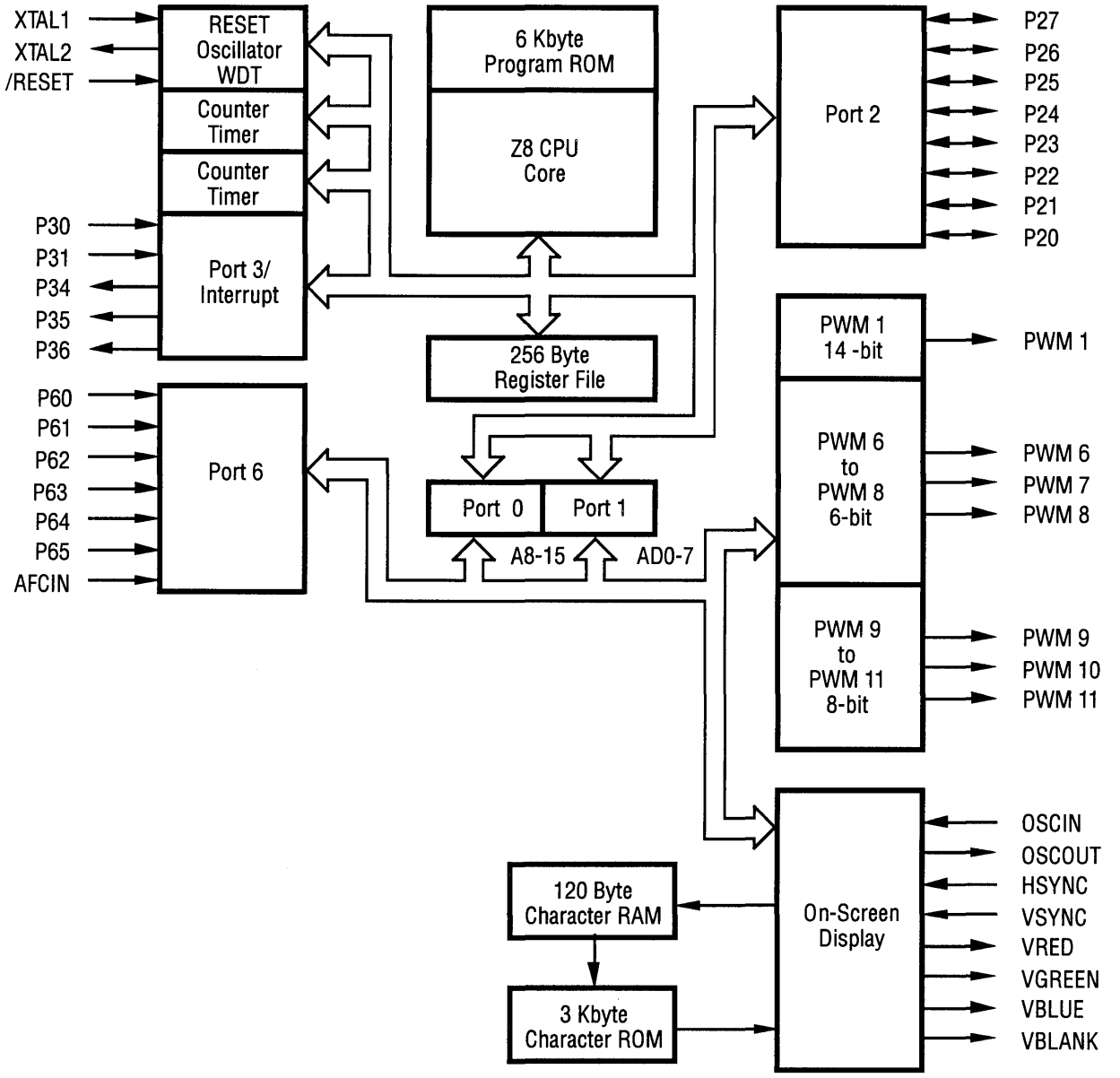

Figure 1. Functional Block Diagram

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Z90209/203/202

TELEVISION CONTROLLERS

FEATURES

■ Part	ROM (KB)	RAM* (Kbyte)	Speed (MHz)	Package Type
Z90209	16	236	6	124-Pin PGA
Z90203	16	236	6	42-Pin SDIP
Z90202	8	236	6	42-Pin SDIP

*General-Purpose

- 4.5V to 5.5V Operating Range
- 0°C to +70°C Temperature Range
- Low-Power Consumption
- On-Screen Display (OSD) Logic Circuits
- One 14-Bit and One 108-Bit Pulse Width Modulator (PWM) Circuits
- 20 Input/Output Lines
- Program Memory, Video RAM, and Register File Address Spaces
- Two On-Chip Counter/Timers

GENERAL DESCRIPTION

The Z9020X Family of Digital Television Controllers are cost-effective members of the Z8® single-chip microcontroller family. The devices provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z90209 is the ROMless In-Circuit Emulation (ICE)Chip version of the Z90200 Digital Television Controller Family used in emulators and development boards.

The device features an 8-bit internal data path controlled by a Z8 microcontroller, On-Screen Display (OSD) logic circuits, and Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and Port 3), interrupt control logic (one software, two external and three internal interrupts) and a standby mode recovery input port (Port 3, pin P30).

The OSD control circuits support ten rows by 24 columns of characters. The character color is specified by character. The OSD inter-row spacing is variable and can be programmed from 0 to 15 horizontal scan lines. The OSD is capable of displaying high resolution (14 x 18 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Ten 8-bit PWM ports are used for controlling audio signal levels to vary picture levels.

Three basic address spaces, The Program Memory, Video RAM, and Register File, support a wide range of memory configurations.

For applications demanding powerful I/O capabilities, the Z9020X's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the Z9020X offers two on-chip counter/timers with a large number of user selectable modes.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

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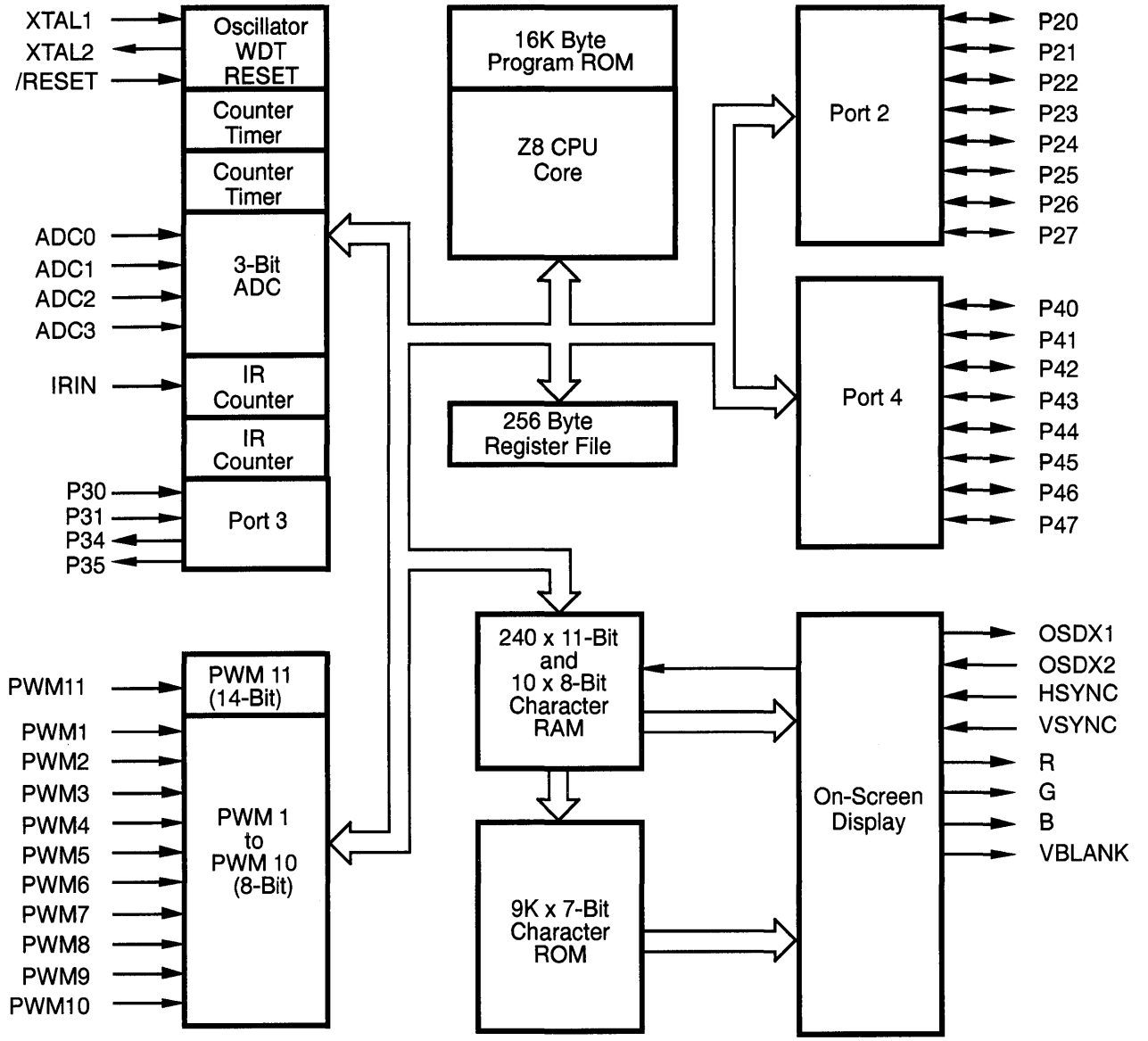
GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z86C2700ZDB

DTC FAMILY EMULATOR DAUGHTER BOARD

DESCRIPTION

The Z86C2700ZDB daughter board can be used in a standalone mode. An EPROM socket is provided for applying the application Software. In Addition, it can be used in conjunction with an ORION™ Unilab 8620 Emulator to generate program code and provide a simple connector interconnection for this purpose.

SUPPORTED DEVICES

Z86C27, Z86127, Z86227

SPECIFICATIONS

Emulation Specification

Maximum Emulation Speed 16 MHz

Power Requirements

+5 Vdc @ 1.5 A

Dimensions

Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

KIT CONTENTS

Z86C27 Emulation Daughter Board
- EPM5192 EPLD
- EPM5128 EPLD (2)
- EPM5032 EPLD
- 16 MHz CMOS Z86C1216GSE ICE Chip
- 8k x 8 Static RAM
- 28-Pin ZIF Socket
- 6 HP-16500A Logic Analysis System Interface Connectors
- 2 60-Pin Target Connectors
- 64-Pin ESD Protection Adapter
- Reset Switch

Cables

- 15" Power Cable with Banana Plugs
- 12" 64-Pin DIP Emulation Cable Pod
- 12" 40-Pin DIP Emulation Cable Pod

Software (IBM-PC Platform)

- Z8®/Z80®/Z8000® Cross Assembler
- MOBJ Link/Loader

Documentation

- Daughter Board User Guide
- Z8 Cross Assembler User Guide
- MOBJ Link/Loader User Guide
- Registration Card

SUPPORT PRODUCT

Z86C2700ZEM

EMULATION ADAPTER BOARD

DESCRIPTION

The Z86C2700ZEM Emulation Adapter Board is specifically designed to assist in the development of software for Zilog's Z86C27, 127, 227 mask-ROM Digital Television Controllers.

The Z86C2700ZEM Emulation Board allows the user to plug a programmed EPROM into the board to test out code. The board utilizes a Z86C97 ROM-less device that provides an address and data path (for access to external memory and I/O) and additional emulation signals. As the Z86C97 uses Port 4, Port 5 and Port 6 for the external interface, the emulation board simulates true Z86C27, 127, 227 port functions with additional on-board logic.

An EPROM socket is provided to allow validation of the customer ROM-code before submitting to Zilog for generation of the Z86C27, 127, 227 ROM mask.

Supported Devices

Z86C27, Z86127, Z86227

Specifications

Power Requirements

+5 Vdc @ 0.3A

KIT CONTENTS

Z86C27 Emulation Board

CMOS Z86C97 MPU
EP1800LC-2 EPLD
(32K)/8K x 8 ZIF Socket
4 MHz Crystal
Z86C97 Adapter Board
Z86C97 Expansion Header
Unilab 8620 or 8420 Analyzer-Emulator Headers

Software (IBM PC platform)

Z8/Z80/Z8000 Cross Assembler
MOBJ Link/Loader

Documentation

Z8 Family Data Book
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide

Document Number Description

99C0152-001 Z86C27 Emulation Board
99C0153-001 Z86C27, 127, 227 Target Adapter

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* IBM is a registered trademark of International Business Machines Corp.

SUPPORT PRODUCT

Z86C2702ZEM

ICEBOX™ DTC FAMILY IN-CIRCUIT EMULATOR –C27

HARDWARE FEATURES

- Supported Devices

Package	Emulation	Programming
40-Pin DIP	Z86227/Z86247	N/A
64-Pin DIP	Z86C27/C47/E47	N/A
64-Pin DIP	Z86127	N/A

- Real-Time Emulation
- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Z8 GUI Emulator Software
- Windows-Based User Interface
- RS-232 Connector
- ICE Pod Connector for Emulation
- HP-16500A Logic Analysis System Interface Connectors
- Orion™ Unilab 8620 Emulator Connectors

GENERAL DESCRIPTION

The Z86C2702ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the above listed Digital Television Controllers.

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering, and program debugging are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z86C2702ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

The Z86C2702ZEM daughter board can also be used in a standalone mode. An EPROM socket is provided for applying the application software. In addition,it can be used in conjunction with an Orion Unilab 8620 Emulator to generate program code and provide a simple connector interconnection for this purpose

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5.0 VDC, ± 5%
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 8 MHz

Power Requirements

+5.0 VDC @ 1.5A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

Z86E4700ZDP

Z86E47 OTP PROGRAMMING ADAPTER KIT

GENERAL DESCRIPTION

The Z86E47 OTP Adapter Kit enables a standard EPROM programmer to program the Z86E47 OTP device.

The adapter board accepts a blank Z86E47 in a 64-pin ZIF socket and routes the necessary signals to a 28-pin connector targeted for a standard programmer.

Not all commercially available EPROM programmers support the Z86E4700ZDP. Zilog recommends using the System General TURPRO series in conjunction with the Z86E4700ZDP. Contact a Zilog sales office for details.

KIT CONTENTS

Z86E47 Adapter Board Kit includes:

Document No.	Description	Revision
99C0333-001	Z86E4700ZDP DIP Programming Adapter	B
	User's Guide Documentation	

Z86E4701ZDP

Z86E47 OTP PROGRAMMING ADAPTER KIT FOR C12 ICEBOX™

GENERAL DESCRIPTION

The Z86E47 OTP Adapter Kit enables the Z86C1200ZEM ICEBOX™ to program the Z86E47 OTP device.

The adapter board accepts a blank Z86E47 in a 64-pin ZIF socket and routes the necessary signals to a 40-pin connector targeted for the C12 ICEBOX.

In addition, special software for the C12 ICEBOX is included to support programming of the Z86E47. This software should only be used for programming the Z86E47.

KIT CONTENTS

Z86E47 Adapter Board Kit includes:

Document No.	Description
99C0359-001	Z86E4701ZDP DIP Programming Adapter
25C0164-001	Programming Software
88C0032-001	User's Guide Documentation

SUPPORT PRODUCT

Z89301/33101ZDP

ONE-TIME PROGRAMMABLE (OTP) PROGRAMMING ADAPTER KIT FOR Z89309001ZEM ICEBOX™

FEATURES

- Supported Devices

Part	Packages	Speed (MHz)
Z89301	52-Pin DIP	N/A
Z89331	42-Pin DIP	N/A

- Cost-Effective Programming Adapter
- Allows Use of Existing Emulator
- One-Time Programmable Converter

GENERAL DESCRIPTION

The Z8930101ZDP and Z8933101ZDP are adapter kits specifically designed to enable Zilog's Z89301 and Z89331 One-Time Programmable (OTP) microcontrollers to be programmed by the Zilog Z8930901ZEM emulator.

The adapter boards will accept either a Z89301 in a 52-pin or a Z89331 in a 42-pin Zero Insertion Force (ZIF) socket, convert it to a 40-Pin DIP pinout, and route the necessary signals to the targeted ICEBOX. Software included with the ICEBOX supports programming of the Z89301 and Z89331.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Operating Humidity: 10-90% RH (Non-Condensing)

Power Requirements

Not Applicable

Dimensions

Width: 1.0 in.
Length: 2.5 in.

KIT CONTENTS

Z89301 OTP Adapter Kit Includes:
Z8930101ZDP Programmer Adapter

Z89331 OTP Adapter Kit Includes:
Z8933101ZDP Programmer Adapter

Documentation

Z893XX OTP Programming Adapter User's Guide (DC# UG95DSP0100)

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Z8930200TSC

EMULATION MODULE (PROTOPACK)

DESCRIPTION

The Z8930200TSC Emulation Module allows the user to plug programmed EPROMs into the board to verify operation of code before submitting for mask ROM.

The emulation module board is connected through a cable to a plug, which is inserted into a socket on the pod. This pod converts to the 40-pin footprint, which plugs into a socket on the target board.

The Z89302 Emulation Module provides emulation for 12 MHz operation of the Z89302/4/6/14.

Supported Devices

Z89302/4/6/14

Specifications

Emulation Specification

Maximum Emulation Speed: 12 MHz

Power Requirements

+5 Vdc @ 150 mA from Target Board

Operating Voltage Range

4.5V to 5.5V

Operating Temperature

0 to 70°C

Operating Humidity

10-90% RH (Non-Condensing)

KIT CONTENTS

Z89300 Emulation Module

CMOS Z89309 DSP Processor
2 x 28-Pin 16K x 8 EPROM Socket
Z89302 Emulation Pod

Documentation

Z89300 Series Module User Guide

Ordering Information

Part Number: Z8930200TSC

Z8930201TSC

EMULATION MODULE (PROTOPACK)

DESCRIPTION

The Z8930201TSC Emulation Module allows the user to plug programmed EPROMs into the board to verify operation of code before submitting for mask ROM.

The emulation module board is connected through a cable to a plug, which is inserted into a socket on the pod. This pod converts to the 40-pin footprint, which plugs into a socket on the target board.

The Z89302 Emulation Module provides emulation for 12 MHz operation of the Z89302/4/6/14.

Supported Devices

Z89302/4/6/14

Specifications

Emulation Specification
Maximum Emulation Speed: 12 MHz

Power Requirements
+5 Vdc @ 150 mA from Target Board

Operating Voltage Range
4.5V to 5.5V

Operating Temperature
0 to 70°C

Operating Humidity
10-90% RH (Non-Condensing)

KIT CONTENTS

Z89300 Emulation Module
CMOS Z89309 DSP Processor
2 x 28-Pin 16K x 8 EPROM Socket
Z89302 Emulation Pod

Documentation
Z89300 Series Module User Guide

Ordering Information
Part Number: Z8930201TSC

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Z8930300TSC

EMULATION MODULE (PROTOPACK)

DESCRIPTION

The Z8930300TSC Emulation Module allows the user to plug programmed EPROMs into the board to verify operation of code before submitting for mask ROM.

A plug soldered directly onto the emulation module board connects to the pod. This pod converts to a 52-pin footprint which plugs directly into a socket on the target board.

The Z89303 Emulation Module provides emulation for 12 MHz operation of the Z89303/05/07.

Supported Devices

Z89303/05/07

Specifications

Emulation Specification
Maximum Emulation Speed: 12 MHz

Power Requirements
+5 Vdc @ 150 mA from Target Board

Operating Voltage Range
4.5V to 5.5V

Operating Temperature
0 to 70°C

Operating Humidity
10-90% RH (Non-Condensing)

KIT CONTENTS

Z89300 Emulation Module
CMOS Z89309 DSP Processor
2 x 28-Pin 16K x 8 EPROM Socket
Z89303 Emulation Pod

Documentation
Z89300 Series Module User Guide

Ordering Information
Part Number: Z8930300TSC

Z8930301TSC

EMULATION MODULE (PROTOPACK)

DESCRIPTION

The Z8930301TSC Emulation Module allows the user to plug programmed EPROMs into the board to verify operation of code before submitting for mask ROM.

The emulation module board is connected through a cable to a plug, which is inserted into a socket on the pod. This pod converts to the 52-pin footprint, which plugs into a socket on the target board.

The Z89303 Emulation Module provides emulation for 12 MHz operation of the Z89303/5/7.

Supported Devices

Z89303/5/7

Specifications

Emulation Specification
Maximum Emulation Speed: 12 MHz

Power Requirements
+5 Vdc @ 150 mA from Target Board

Operating Voltage Range
4.5V to 5.5V

Operating Temperature
0 to 70°C

Operating Humidity
10-90% RH (Non-Condensing)

KIT CONTENTS

Z89300 Emulation Module
CMOS Z89309 DSP Processor
2 x 28-Pin 16K x 8 EPROM Socket
Z89303 Emulation Pod

Documentation
Z89300 Series Module User Guide

Ordering Information
Part Number: Z8930301TSC

SUPPORT PRODUCT

Z8930901ZEM

ICEBOX™
Z89300 FAMILY EMULATOR

FEATURES

- Supported Devices

Packages	Emulation	Programming
40-Pin DIP	Z89300/2/4/ 6/14/18	Z89300
52-Pin SDIP	Z89301/3/5/7	Z89301*
42-Pin SDIP	Z89331/2/4/6	Z89331**

Notes:
*With optional separately purchased adapter, Z8930101ZDP.
**With optional separately purchased adapter, Z8933101ZDP.

- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Window-Based User Interface
- RS-232 Connector
- DSP GUI Emulator Software
- ICE Pod Connector for Emulation
- HP-16500 Logic Analyzer System Interface Connector

GENERAL DESCRIPTION

The Z8930901ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the Z89300 family of digital television controllers.

Zilog's in-circuit emulators are interactive, Window-oriented development tools, featuring a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering and program debugging are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z8930901ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

Z8931302TSC

EMULATION MODULE (PROTOPACK)

FEATURES

- Supported Devices

Packages	Emulation	Programming
52-Pin SDIP	Z89313	NONE

- ROM Code Verification
- Emulation Module

GENERAL DESCRIPTION

The Z8931302TSC Emulation Module allows the user to plug programmed EPROMs into the board to verify operation of code before submitting for mask ROM.

The Z89313 Emulation Module provides emulation for 12 MHz operation of the Z89313.

SPECIFICATIONS

Emulation Specification

Maximum Emulation Speed: 12 MHz

Power Requirements

+5 Vdc @ 150 mA from Target Board

Operating Voltage Range

4.5V to 5.5V

Dimensions

2.4-inch x 3..5-inch

Operating Temperature

20°C ± 10°C

Operating Humidity

10-90% RH (Non-Condensing)

KIT CONTENTS

Z89313 Emulation Module

CMOS Z89319 DSP Processor
2 x 28-Pin 16K x 8 EPROM Socket
Z89313 Emulation Pod

Documentation

Z89313 Series Module User Guide

SUPPORT PRODUCT

Z8931900ZEM

ICEBOX™
Z89313 FAMILY EMULATOR

FEATURES

- Supported Devices

Packages	Emulation	Programming
52-Pin SDIP	Z89313	NONE

- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Window-Based User Interface
- RS-232 Connector
- DSP GUI Emulator Software
- ICE Pod Connector for Emulation
- HP-16500 Logic Analyzer System Interface Connector

GENERAL DESCRIPTION

The Z8931900ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the Z89313 family of digital television controllers.

Zilog's in-circuit emulators are interactive, Window-based development tools, featuring a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering and program debugging are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z8931900ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5 VDC, ± 5%
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 12 MHz

Power Requirements

+5 VDC @ 2.0A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

Z8933200TSC

EMULATION MODULE (PROTOPACK)

DESCRIPTION

The Z8933200TSC Emulation Module allows the user to plug programmed EPROMs into the board to verify operation of code before submitting for mask ROM.

A plug soldered directly onto the emulation module board connects into a pod. This pod converts to the 42-pin footprint which plugs directly into a socket on the target board.

The Z89313 Emulation Module provides emulation for 12 MHz operation of the Z89332/6.

Supported Devices

Z89332/6

Specifications

Emulation Specification
Maximum Emulation Speed: 12 MHz

Power Requirements
+5 Vdc @ 150 mA from Target Board

Operating Voltage Range
4.5V to 5.5V

Operating Temperature
0 to 70°C

Operating Humidity
10-90% RH (Non-Condensing)

KIT CONTENTS

Z89300 Emulation Module
CMOS Z89309 DSP Processor
2 x 28-Pin 16K x 8 EPROM Socket
Z89332 Emulation Pod

Documentation
Z89300 Series Module User Guide

Ordering Information
Part Number: Z8933200TSC

Z8933201TSC

EMULATION MODULE (PROTOPACK)

DESCRIPTION

The Z8933201TSC Emulation Module allows the user to plug programmed EPROMs into the board to verify operation of code before submitting for mask ROM.

The emulation module board is connected through a cable to a plug, which is inserted into a socket on the pod. This pod converts to the 42-pin footprint, which plugs into a socket on the target board.

The Z89332 Emulation Module provides emulation for 12 MHz operation of the Z89332/4/6.

Supported Devices

Z89332/4/6

Specifications

Emulation Specification
Maximum Emulation Speed: 12 MHz

Power Requirements
+5 Vdc @ 150 mA from Target Board

Operating Voltage Range
4.5V to 5.5V

Operating Temperature
0 to 70°C

Operating Humidity
10-90% RH (Non-Condensing)

KIT CONTENTS

Z89300 Emulation Module
CMOS Z89309 DSP Processor
2 x 28-Pin 16K x 8 EPROM Socket
Z89332 Emulation Pod

Documentation
Z89300 Series Module User Guide

Ordering Information
Part Number: Z8933201TSC

Z9020900TSC

Z90209 EMULATION MODULE

FEATURES

- Supported Devices

Packages	Emulation
42-Pin SDIP	Z90202/03/04

- In-Circuit Emulation
- EPROM for Easy Code Change

GENERAL DESCRIPTION

The Z90209 Emulation Module can be used like a One-Time Programmable (OTP) for plug-in emulation of the Z9020X chip in user target applications. It provides external EPROMs to simulate an OTP and can be used repeatedly. Its electrical characteristics are nearly identical with the OTP.

Users can develop and debug their application software using a Z90209 Emulator (Z9020900ZEM) and transfer it to the EPROMs on the Emulation Module for final test.

SPECIFICATIONS

Dimensions

Width: 2.60 in. (6.60 cm)
Length: 3.00 in. (7.62 cm)
Height: 1.30 in. (3.30 cm)

Power Requirements

–4.75 VDC to + 5.25 VDC (+5.0 VDC typical)
@ 300 mA

Operating Temperature

20°C, ±10°C

Operating Humidity

40-90% RH (non-condensing)

PACKAGE CONTENTS

Hardware

Qty. Description

1 Z90209 Emulation Module (Z9020900TSC) includes:
- (1) Z90209 ICE Chip
- (1) Character Generator ROM (CGROM)
- (2) 28-Pin Sockets

2 27C256-35 EPROMs

Documentation

User's Guide

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SUPPORT PRODUCT

Z9020900ZEM

ICEBOX™ Family
IN-CIRCUIT EMULATOR – 209

FEATURES

- Supported Devices

Packages	Emulation	Programming
42-Pin SDIP	Z90202/03/04	N/A

- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Window-Based User Interface
- RS-232 Connector
- Z8 GUI Emulator Software
- ICE Pod Connector for Emulation
- Selectable Baud Rates (9600 to 57.6K)
- HP-16500 Logic Analysis System Interface Connector

GENERAL DESCRIPTION

The Z90209 Emulator (Z9020900ZEM) is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the Z90200 family of digital television controllers.

Zilog's in-circuit emulators are interactive, Window-oriented development tools, featuring a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering and program debugging are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z90209 emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5 VDC, ± 5%
Maximum Emulation Speed: 6 MHz

Power Requirements

+5 VDC @ 2.0A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

Serial Interface
RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

ZiLOG

8-Bit Microcontrollers

Z8® Microcontrollers 1

IR Remote Controllers 2

Computer Peripheral Controllers

Keyboard /Input Devices 3

Mass Storage 4

PCMCIA 5

DSP (Digital Signal Processors)

Television/Cable/Satellite/Set-Top Boxes 6

Voice Processors 7

DSP Cores 8

Z89135

LOW-COST DUAL-PROCESSOR DTAD CONTROLLERS

FEATURES

Part Number	Z8 ROM (KBytes)	Z8 RAM* (KBytes)	Speed (MHz)
Z89135	24	236	20

  *General-Purpose

Part Number	DSP ROM (Words)	DSP RAM (Words)	Speed (MHz)
Z89135	6K	512	20

- 68-Pin PLCC Package
- 4.75- to 5.25-Volt Operating Range
- Low-Power Consumption (200 mW Typical)
- 0°C to +55°C Temperature Range
- 25 Expanded Register Files
- 47 Input/Output Lines
- Six Vectored, Prioritized Z8 Interrupts with Programmable Polarity
- Three Vectored, Prioritized DSP Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable Z8 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer /Power-On Reset
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- RAM and ROM Protect, Low-EMI Option

GENERAL DESCRIPTION

Zilog's Digital Voice Processor Controller family combines a Z8® microcontroller and a DSP processor on-chip for a cost-effective turnkey system in digital telephone answering devices and other voice processing applications.

The dual-processor architecture is loosely coupled by mailbox registers and an interrupt system, enabling DSP or Z8 programs to be directed by events in each other's domain.

The Z8 microcontroller uses an expanded register file to allow access to register-mapped peripheral and I/O circuits for programming versatility.

The 16-bit DSP processor features a 24-bit ALU and accumulator with single-cycle instructions, providing the algorithm processing power necessary for telephone voice quality.

The Z89135 device offers a half-flash 8-bit A/D converter with up to 128 kHz sample rate and a 10-bit Pulse-Width modulator (PWM) D/A converter, eliminating the need for an external CODEC.

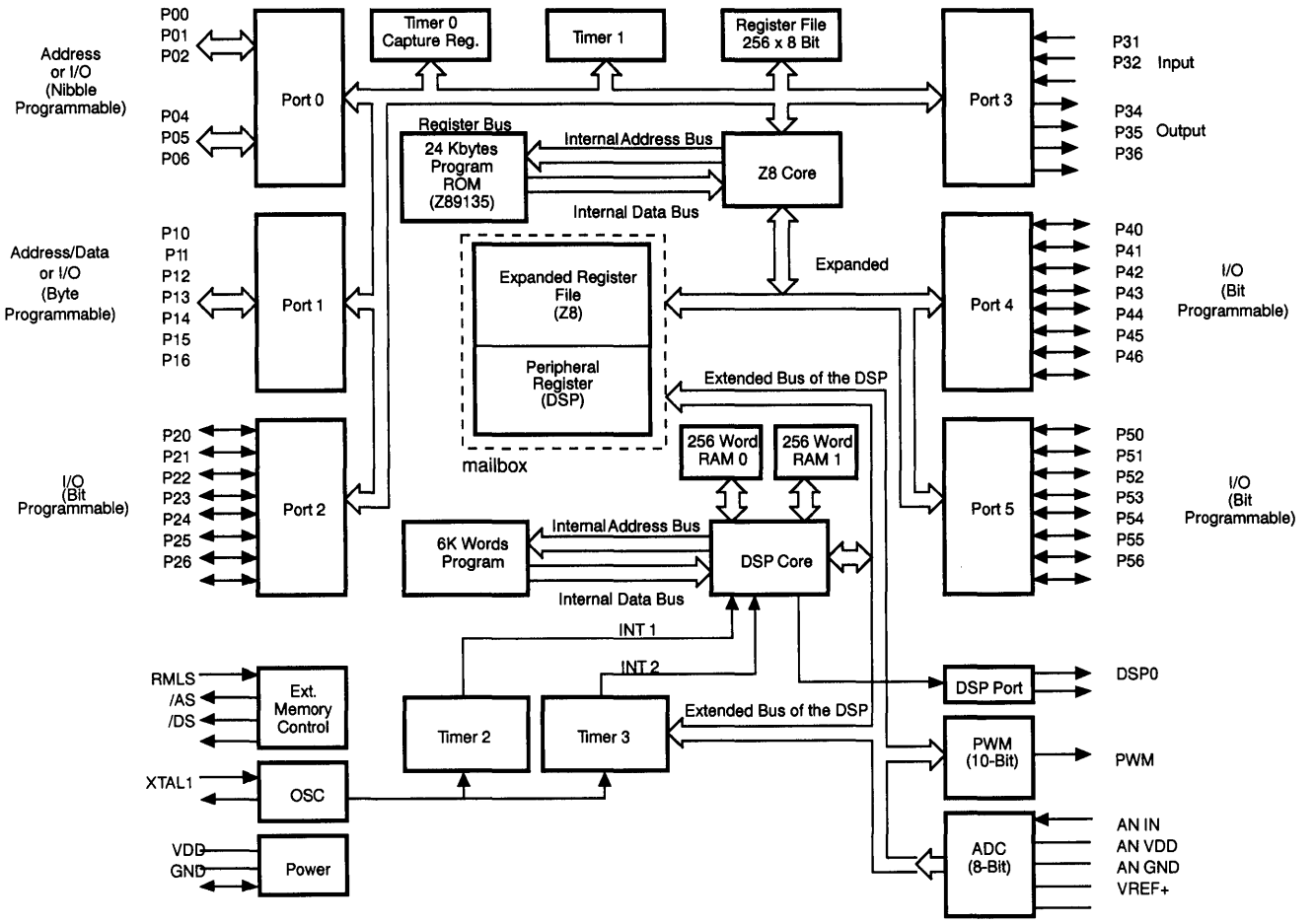
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

7

GENERAL DESCRIPTION (Continued)



Z89135 Functional Block Diagram

Z89165/167/169 AND Z89166/168 (ROMLESS)

ENHANCED DUAL-PROCESSOR DTAD CONTROLLERS

FEATURES

Part Number	Z8 ROM (KBytes)	Z8 RAM* (KBytes)	Speed (MHz)
Z89165	24	236	20
Z89166	ROMless	236	20
Z89167	24	236	24
Z89168	ROMless	236	24
Z89169	32	236	24

  *General-Purpose

Part Number	DSP ROM (Words)	DSP RAM (Words)	Speed (MHz)
Z89165	6K	512	20
Z89166	6K	512	20
Z89167	8K	512	24
Z89168	8K	512	24
Z89169	8K	512	24

- 68- and 84-Pin PLCC Packages
- 4.5- to 5.5-Volt Operating Range
- Low-Power Consumption (200 mW Typical)
- 0°C to +70°C Temperature Range
- 25 Expanded Register Files
- 47 Input/Output Lines (Z89165)
  31 Input/Output Lines (Z89166)
  43 Input/Output Lines (Core Processor)
- Six Vectored, Prioritized Z8 Interrupts with Programmable Polarity
- Three Vectored, Prioritized DSP Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable Z8 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer /Power-On Reset
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- RAM and ROM Protect, Low-EMI Option

GENERAL DESCRIPTION

Zilog's Digital Voice Processor Controller family combines a Z8® microcontroller and a DSP processor on-chip for a cost-effective turnkey system in digital telephone answering devices and other voice processing applications.

The dual-processor architecture is loosely coupled by mailbox registers and an interrupt system, enabling DSP or Z8 programs to be directed by events in each other's domain.

The Z8 microcontroller uses an expanded register file to allow access to register-mapped peripheral and I/O circuits for programming versatility.

The 16-bit DSP processor features a 24-bit ALU and accumulator with single-cycle instructions, providing the algorithm processing power necessary for telephone voice quality.

The Z89165/166 devices offer a half-flash 8-bit A/D converter with up to 128 kHz sample rate and a 10-bit Pulse-Width modulator (PWM) D/A converter, eliminating the need for an external CODEC.

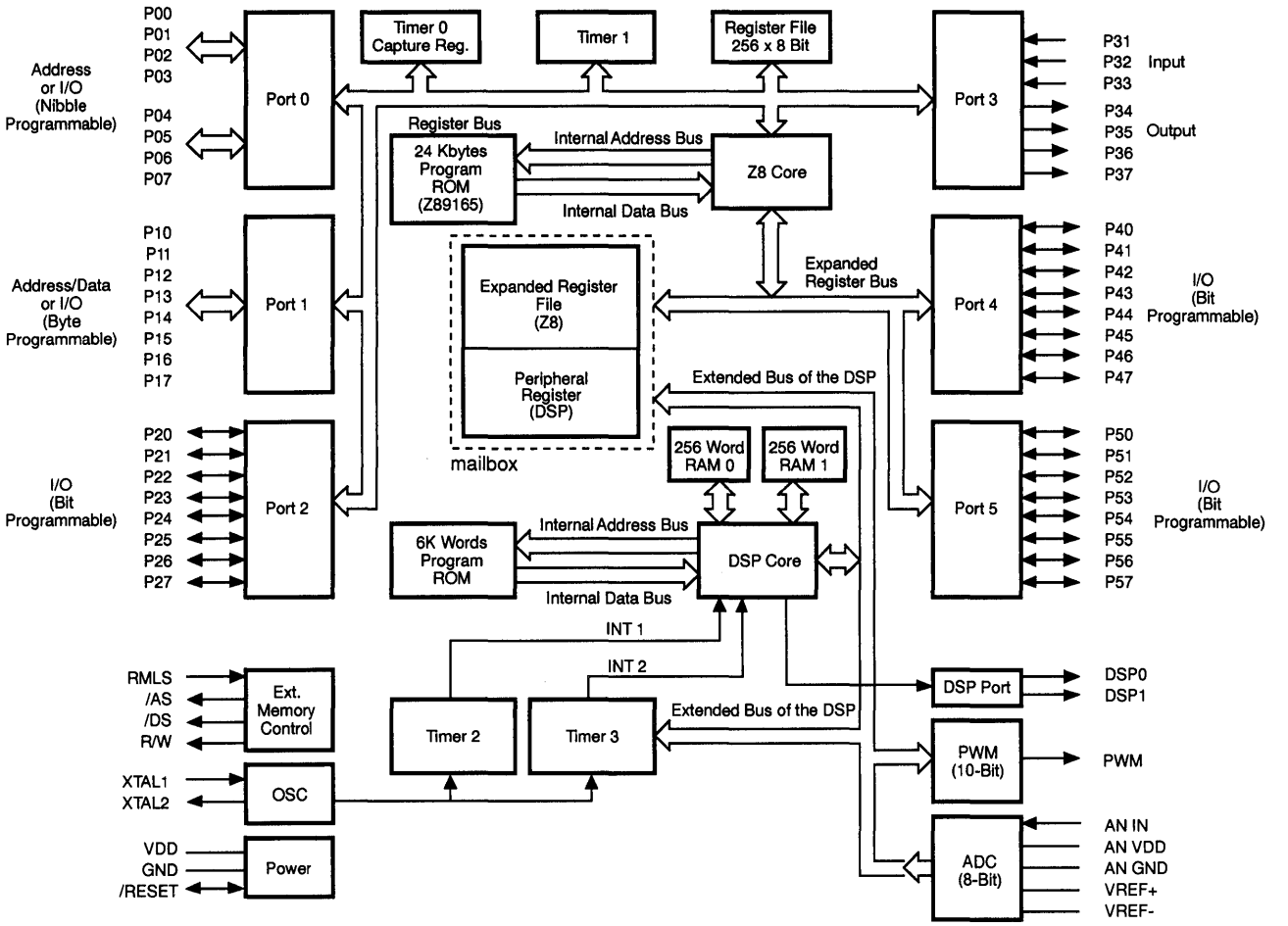
The Z89167/168/169 devices feature a hardware ARAM interface, as well as a dual-CODEC interface. A 10-bit PWM D/A converter is also on-chip.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

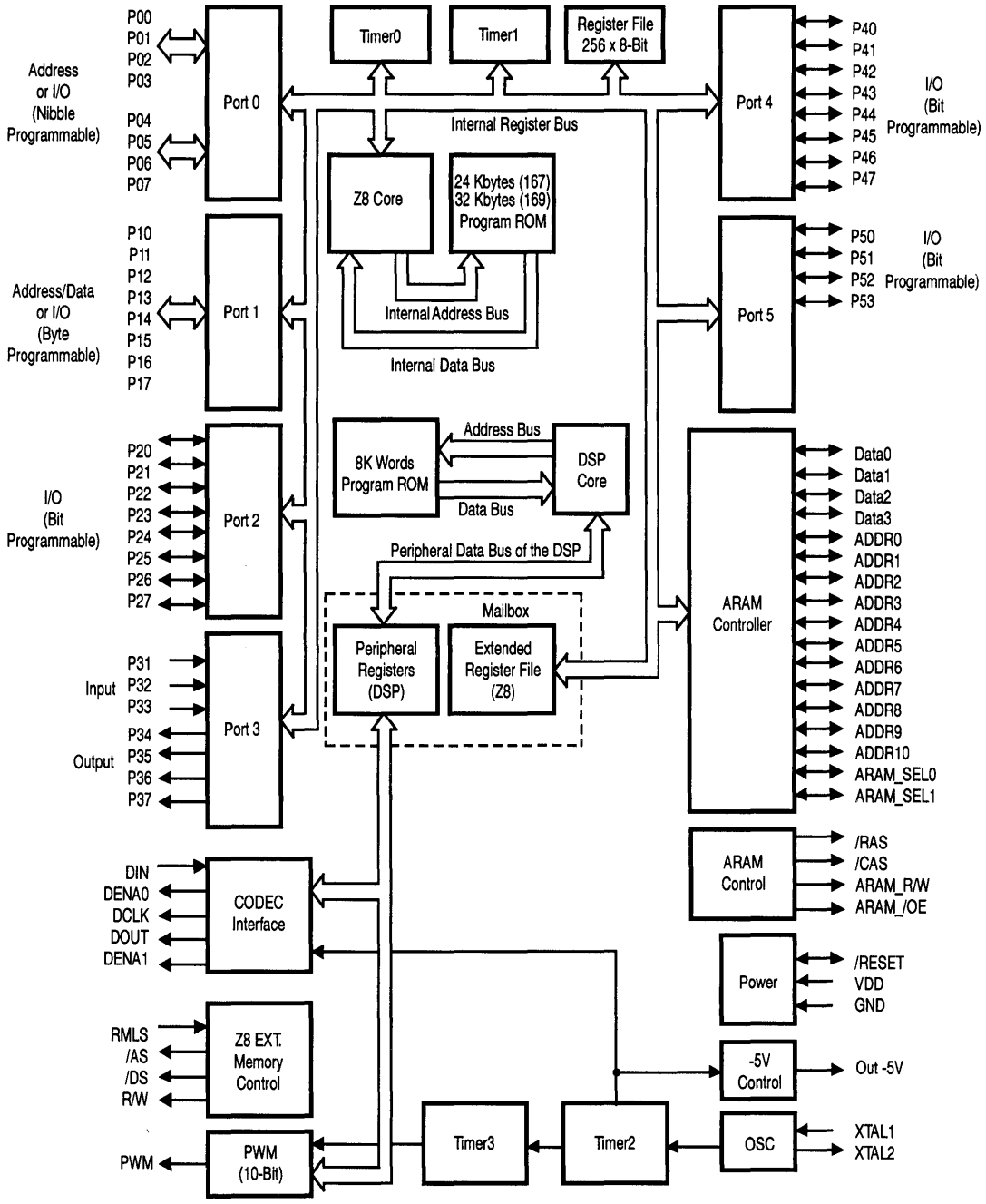
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Z89165/166 Functional Block Diagram

GENERAL DESCRIPTION (Continued)



Z89167/168/169 Functional Block Diagram

Z89175
Z89176 (ROMLESS)
VOICE PROCESSING CONTROLLERS

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z89175	24	256	47	4.5V to 5.5V
Z89176	-	256	31	4.5V to 5.5V

Note: *General-Purpose

- Watch-Dog Timer and Power-On Reset
- Improved Low Power Stop Mode
- On-Chip Oscillator which Accepts a Crystal or External Clock Drive
- Improved Global Power-Down Mode
- Low Power Consumption - 200 mW (typical)
- Two Comparators
- RAM and ROM Protect
- On-Board Oscillator for 32.768 kHz Real-Time Clock
- Clock Speeds of 20.48 or 29.49 MHz
- 16-Bit Digital Signal Processor (DSP)
- 8K Word DSP Program ROM
- 512 Words On-Chip DSP RAM
- 8-Bit A/D Converter with up to 16 kHz Sample Rate
- 10-Bit PWM D/A Converter
- Six Vectored, Prioritized Z8 Interrupts
- Three Vectored, Prioritized DSP Interrupts
- Two DSP Timers to Support Different A/D and D/A Sampling Rates
- IBM® PC-Based Development Tools
- Developer's Toolbox for T.A.M. Applications

GENERAL DESCRIPTION

The Z89175/176 is a fully integrated, dual processor controller designed for voice processing applications. The I/O control processor is a Z8® with 24 KB of program memory, two 8-bit counter/timers, and up to 47 I/O pins. The DSP is a 16-bit processor with a 24-bit ALU and accumulator, 512x16 bits of RAM, single cycle instructions, and 8K words of program ROM. The chip also contains a half-flash 8-bit A/D converter with up to a 16 kHz sample rate and a 10-bit PWM D/A converter. The sampling rates for the converters are programmable. The precision of the 8-bit A/D can be extended by resampling the data at a lower rate in software. The Z8 and DSP processors are coupled by mailbox registers and an interrupt system. DSP or Z8 programs can be directed by events in each other's domain.

The Z89176 is the ROMless version of the Z89175. However, the on-chip DSP is not ROMless.

Notes: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

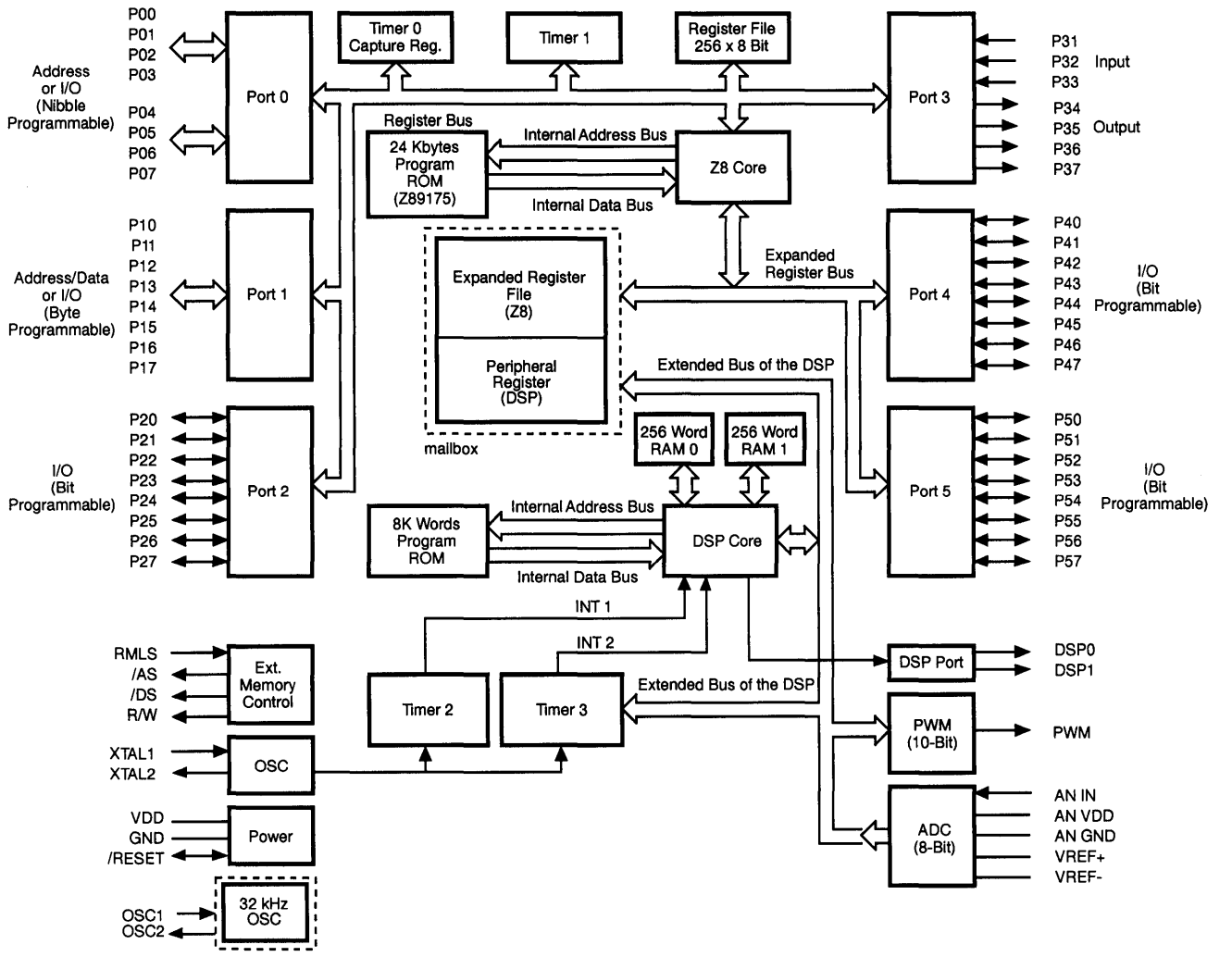


Figure 1. Z89175/176 Functional Block Diagram

ZILOG

SUPPORT PRODUCT

Z89165000ZCO

LOW COST TAPELESS ANSWERING DEVICE EVALUATION BOARD

DESCRIPTION

The Low Cost Tapeless Answering Device Evaluation Board can be used to demonstrate the full-digital answering machine capabilities of the Z89165/166 devices, including LPC speech generation, voice compression/expansion and DTMF detection. The on-board A/D and D/A converter allows demonstration of the memo and ICM functions. One DRAM allows for speech storage.

The user can develop and debug Z8® application code using the Z89165 Toolbox software and a Z89C6501ZEM emulator. No DSP code writing is necessary.

Supported Devices

Z89165, Z89166

Specifications

Power Requirements

9 VAC @ 500 mA

Dimensions

Electrical Board
5" x 4"

KIT CONTENTS

Low Cost Tapeless Answering Device Evaluation Board

One 68-Pin PLCC Socket for Z89165/166 or Z89C6501ZEM Emulator or Z89C6500ZDB Daughter Board
One 20.48 MHz Crystal
One 1-Meg x 4 DRAM
One 64K x 8 EPROM (with Z8 Application Code)
One RJ-11 Phone Jack
One Reset Button
Keypad Matrix
One LED Indicator
One Microphone

One 2" Speaker

One 9 VAC Power Supply

Documentation

User's Manual which includes:
Block Diagram
Schematics

7

Z8916902ZCO

LOW COST TAPELESS ANSWERING DEVICE EVALUATION BOARD

DESCRIPTION

The Low Cost Tapeless Answering Device Evaluation Board can be used to demonstrate the full-digital answering machine capabilities of the Z89C67/68/69 and Z89167/168/169 chips, including LPC speech generation, voice compression and expansion, and DTMF detection. One Codec allows demonstration of the memo and speakerphone functions and two DRAMs allow for speech storage.

The User can develop and debug Z8® applications code using the Z86C67 Toolbox software and a Z89C6700ZEM emulator or a Z89C5900ZEM emulator. No DSP code writing is necessary.

Supported Device

Z89C67, Z89C68, Z89C69, Z89167, Z89168, Z89169

Specifications

Power Requirements

9 VAC @ 0.5A

Dimensions

Electrical Board
7.75" x 3.5"

KIT CONTENTS

Low Cost Tapeless Answering Device Evaluation Board

84-Pin PLCC Socket for Z89C67/68/69, or Z89167/168/169, or Z89C6700ZEM /ZDB or Z89C5900ZEM Emulator
24.57 MHz Crystal
2 1Megx4 DRAMs
32K x 8 EPROM (with Z8® Application Code)
1 Codec
1 RJ-11 Telephone Connector Jack
Reset Switch
Keypad Matrix
4 LED Indicators
2 7-Seg LED Indicators
1 Microphone

2 1/2" Speaker

9 VAC Power Supply

Documentation

User's Manual which includes:
Block Diagram
Schematics

Z8917500ZCO

Z89175/176 VOICE PROCESSING EVALUATION KIT

FEATURES

- Supported Devices:

Packages	Emulation
100-Pin QFP	Z89175
100-Pin QFP	Z89176

- Fully Digital Answering Machine Capability
- Caller ID Support
- Date and Time Stamping
- High-Quality Voice
- Z89175 Evaluation Kit Software
- DTMF Detection/Generation

GENERAL DESCRIPTION

Zilog's Z89175 Voice Processing Evaluation Kit (Z8917500ZC0) demonstrates the fully digital answering machine capabilities of the Z89175 and Z89176 voice processing devices, including LPC speech generation, voice compression/expansion, and DTMF encoding/decoding.

The Z89175/176 Evaluation Board features:

- On-chip CODEC that provides demonstration for the Memo and Incoming Message functions.
- Caller ID On-Hook function with LCD display.
- One Samsung KM29N040, 512 x 8-bit FLASH memory with expandability for a second KM29N040.

The Z89175 Evaluation Kit can be used to develop and debug Z8® application code with the Z89175 Toolbox Software (included in this kit) and the C65 ICEBOX™ Emulator (Z89C6501ZEM, not included in this kit). No DSP code writing is necessary. The Z89175 Voice Processing Evaluation Kit provides a complete suite of software aids: application code, DSP code, and toolbox code to assist in evaluation and development of 175/176-supported applications.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 25°C, ±10°C

Power Requirements

+12 VDC @ 500 mA

Dimensions

Width: 4.25 in. (10.8 cm)

Length: 5.75 in. (14.61 cm)

Height: 4.5 in. (11.43 cm)

KIT CONTENTS

Z89175 Evaluation Board

Circuit Board

On-Board Operation Instructions

4 x 16 Character Liquid Crystal Display (LCD)

Two-Inch Speaker

Support Hardware

12 VDC Power Supply

68-PLCC Adapter

100-QFP Adapter

Z8 I/0 Expander

Telephone Cord

Evaluation Kit Software Diskette

Application Code

DSP Code

Toolbox Code

Documentation

Z89175 Evaluation Kit User's Manual

(Includes Kit Schematic and Bill of Material)

SOFTWARE DEVELOPMENT REQUIREMENTS (OPTIONAL)

Host Computer

IBM PC (or 100-percent compatible) 386-based machine running Microsoft Windows 3.1. For increased performance, the following is recommended: 486- or Pentium-based machine, 66 MHz (or faster), 8 MB of RAM (or more), SVGA video adapter, color monitor, and printer.

Note: Exact host computer requirements are dependent on which particular support tools are used.

Support Tools

Z89175 Evaluation Kit Software

Z8 Assembler

C65 ICEBOX Emulator (Z89C6501ZEM)

ZiLOG

8-Bit Microcontrollers

Computer Peripheral Controllers

DSP (Digital Signal Processors)

Z89C00
16-BIT DIGITAL SIGNAL PROCESSOR

FEATURES

- 16-Bit Single Cycle Instructions
- Zero Overhead Hardware Looping
- 16-Bit Data
- Ready Control for Slow Peripherals
- Single Cycle Multiply/Accumulate (100 ns)
- Six-Level Stack
- 512 Words of On-Chip RAM
- Static Single-Cycle Operation
- 16-Bit I/O Port
- 4K Words of On-Chip Masked ROM
- Three Vectored Interrupts
- 64K Words of External Program Address Space
- Two Conditional Branch Inputs/Two User Outputs
- 24-Bit ALU, Accumulator and Shifter
- IBM® PC Development Tools

GENERAL DESCRIPTION

The Z89C00 is a second generation, 16-bit, fractional, two's complement CMOS Digital Signal Processor (DSP). Most instructions, including multiply and accumulate, are accomplished in a single clock cycle. The processor contains 1 Kbyte of on-chip data RAM (two blocks of 256 16-bit words), 4K words of program ROM and 64K words of program memory addressing capability. Also, the processor features a 24-bit ALU, a 16 x 16 multiplier, a 24-bit Accumulator and a shifter. Additionally, the processor contains a six-level stack, three vectored interrupts and two inputs for conditional program jumps. Each RAM block contains a set of three pointers which may be incremented or decremented automatically to affect hardware looping without software overhead. The data RAMs can be simultaneously addressed and loaded to the multiplier for a true single cycle multiply.

There is a 16-bit address and a 16-bit data bus for external program memory and data, and a 16-bit I/O bus for transferring data. Additionally, there are two general purpose user inputs and two user outputs. Operation with slow peripherals is accomplished with a ready input pin. The clock may be stopped to conserve power.

Development tools for the IBM PC include a relocatable assembler, a linker loader, and an ANSI-C compiler. Also, the development tools include a simulator/debugger, a cross assembler for the TMS320 family assembly code and a hardware emulator.

To assist the user in understanding the Z89C00 DSP Q15 two's complement fractional multiplication, an application note has been included in this product specification as an appendix.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

8

GENERAL DESCRIPTION (Continued)

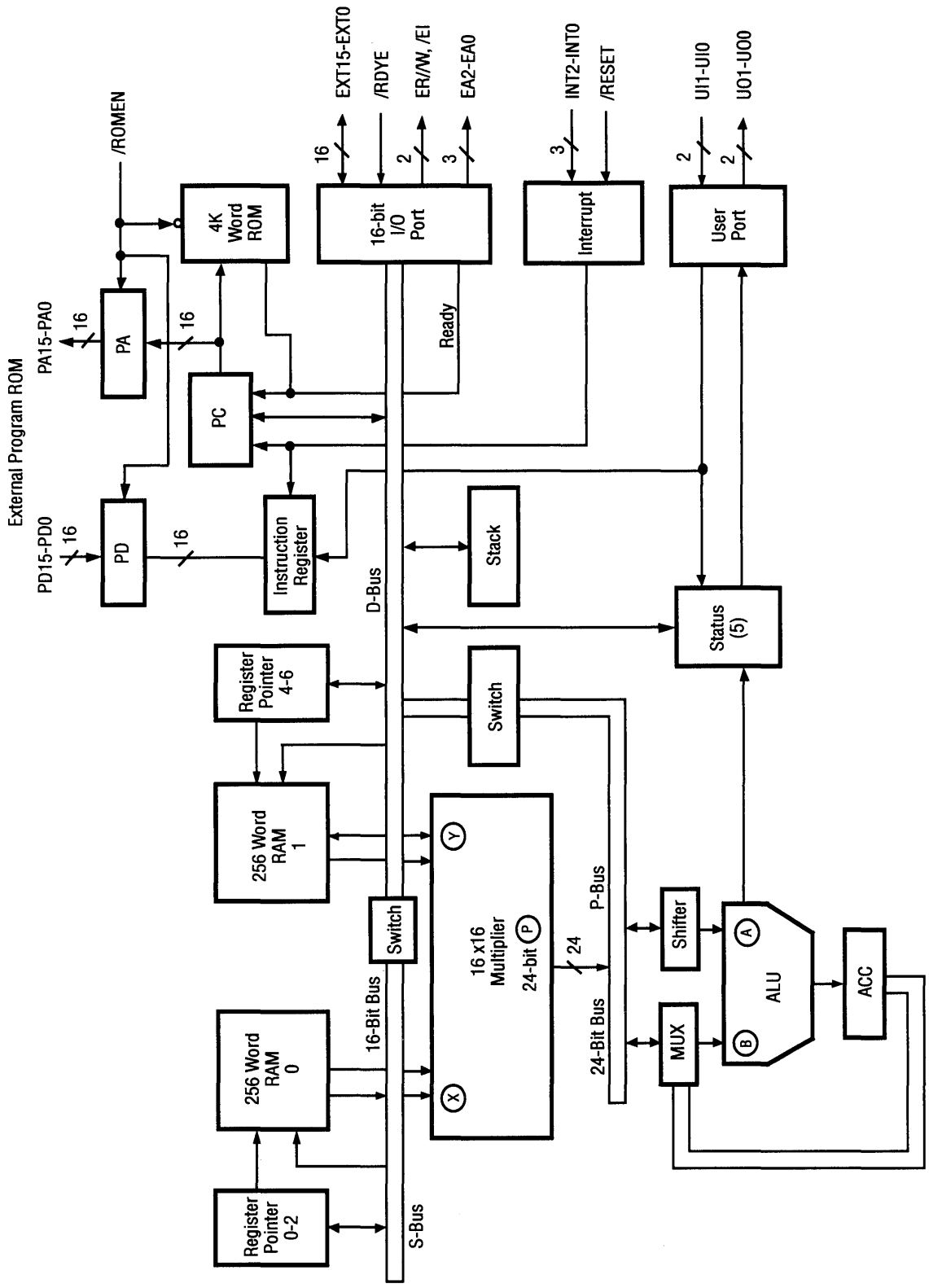


Figure 1. Functional Block Diagram

Z89320
16-BIT DIGITAL SIGNAL PROCESSOR

FEATURES

- 16-Bit Single Cycle Instructions
- Zero Overhead Hardware Looping
- 16-Bit Data
- Ready Control for Slow Peripherals
- Single Cycle Multiply/Accumulate (100 ns)
- Six-Level Stack
- 512 Words of On-Chip RAM
- 16-Bit I/O Port
- 4K Words of On-Chip Masked ROM
- Three Vectored Interrupts
- Two Conditional Branch Inputs/Two User Outputs
- 24-bit ALU, Accumulator and Shifter
- IBM® PC Development Tools
- Cost Effective 40-pin DIP Package

GENERAL DESCRIPTION

The Z89320 is a second generation, 16-bit, fractional, two's complement CMOS Digital Signal Processor (DSP). Most instructions, including multiply and accumulate, are accomplished in a single clock cycle. The processor contains 1 Kbyte of on-chip data RAM (two blocks of 256 16-bit words), 4K words of program ROM. Also, the processor features a 24-bit ALU, a 16 x 16 multiplier, a 24-bit Accumulator and a shifter. Additionally, the processor contains a six-level stack, three vectored interrupts and two inputs for conditional program jumps. Each RAM block contains a set of three pointers which may be incremented or decremented automatically to affect hardware looping without software overhead. The data RAMs can be simultaneously addressed and loaded to the multiplier for a true single cycle multiply.

The device includes a 16-bit I/O bus for transferring data or for mapping peripherals into the processor address space. Additionally, there are two general purpose user inputs and two user outputs. Operation with slow peripherals is accomplished with a ready input pin.

Development tools for the IBM PC include a relocatable assembler, a linker loader, and an ANSI-C compiler. Also, the development tools include a simulator/debugger, a cross assembler for the TMS320 family assembly code and a hardware emulator.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

8

GENERAL DESCRIPTION (Continued)

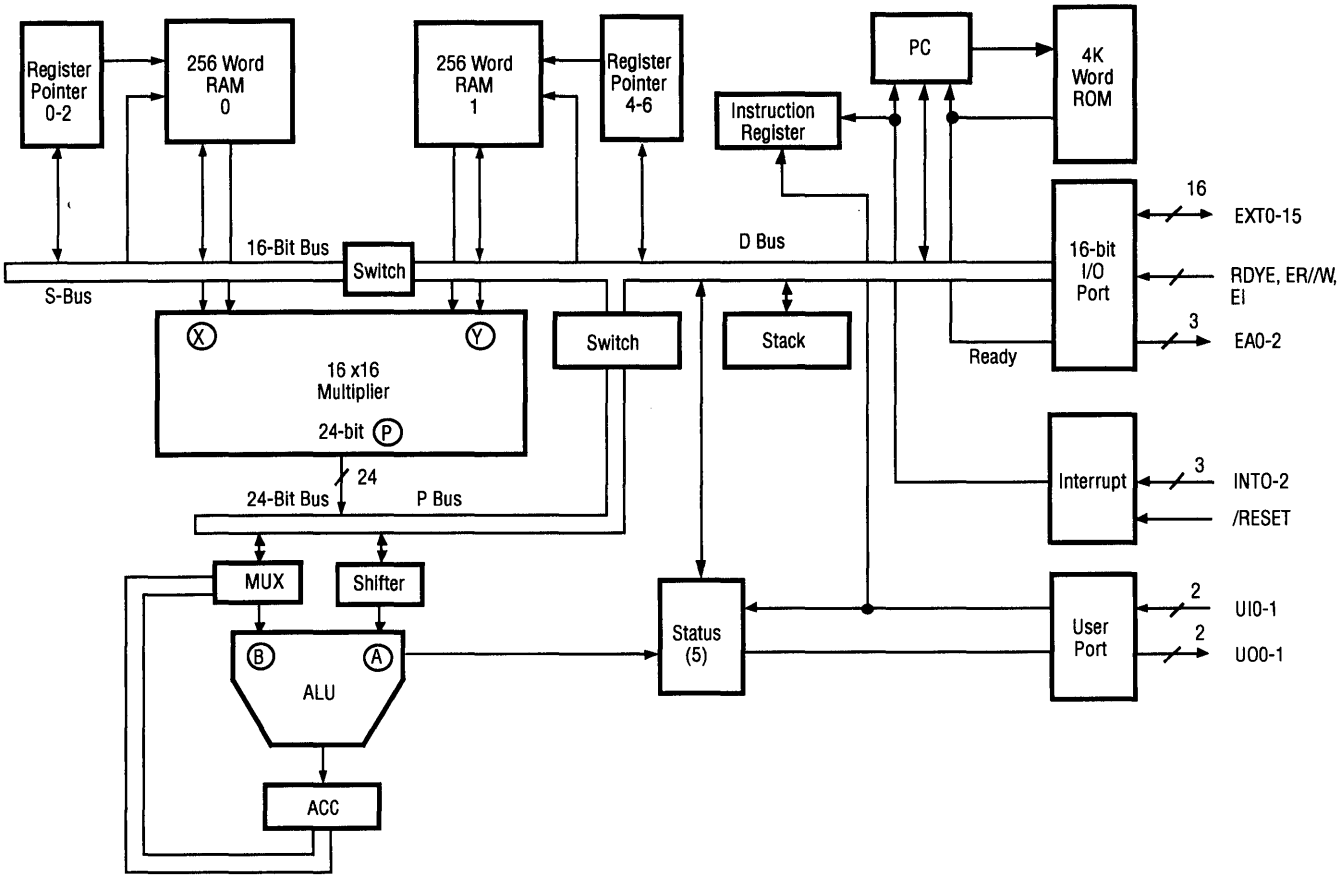


Figure 1. Functional Block Diagram

Z89321/371/391

16-BIT DIGITAL SIGNAL PROCESSORS

FEATURES

Part	DSP ROM (K Words)	OTP (K Words)	DSP RAM (Words)	MIPS (Max)
Z89321	4		512	10, 20
Z89371		4	512	10, 16
Z89391	64*		512	10, 20

Package Part	40-Pin DIP	44-Pin PLCC	44-Pin QFP	84-Pin PLCC
Z89321	X	X	X	
Z89371	X	X	X	
Z89391				X

* External

- 0°C to +70°C Operating Temperature Range
- 4.5- to 5.5-Volt Operating Range (4.75- to 5.25 for Z89371)

DSP Core

- 20 MIPS @ 20 MHz Maximum, 16-Bit Fixed Point DSP
- 50 ns Minimum Instruction Cycle Time
- Six-Level Hardware Stack
- Six Register Address Pointers
- Optimized Instruction Set (30 Instructions)

On-Board Peripherals

- Dual 8/16-Bit CODEC Interface Capable of up to 10 Mbps
- μ-Law Compression Option (Decompression Is Performed in Software)
- 16-Bit I/O Bus (Tri-Stated)
- Three I/O Address Pins (Latched Outputs)
- Wait-State Generator
- Three Vectored Interrupts
- 13-Bit General-Purpose Timer

GENERAL DESCRIPTION

The Z893XX products are high-performance Digital Signal Processors (DSPs) with a modified Harvard-type architecture featuring separate program and data memory. The design has been optimized for processing power and minimizing silicon space.

The single-cycle instruction execution and bus structure promotes efficient algorithm execution, while the six register pointers provide circular buffering capabilities and dual operand fetching.

Three vectored interrupts are complemented by a six-level stack, and the CODEC interface allows high-speed transfer rates to accommodate digital audio and voice data.

A dedicated Counter/Timer provides the necessary timing signals for the CODEC interface, and an additional 13-bit timer is available for general-purpose use.

The Z893XX DSPs are optimized to accommodate advanced signal processing algorithms. The 20 MIPS (maximum) operating performance and efficient architecture provides real-time instruction execution. Compression, filtering, frequency detection, audio, voice detection/synthesis, and other vital algorithms can all be accommodated.

GENERAL DESCRIPTION (Continued)

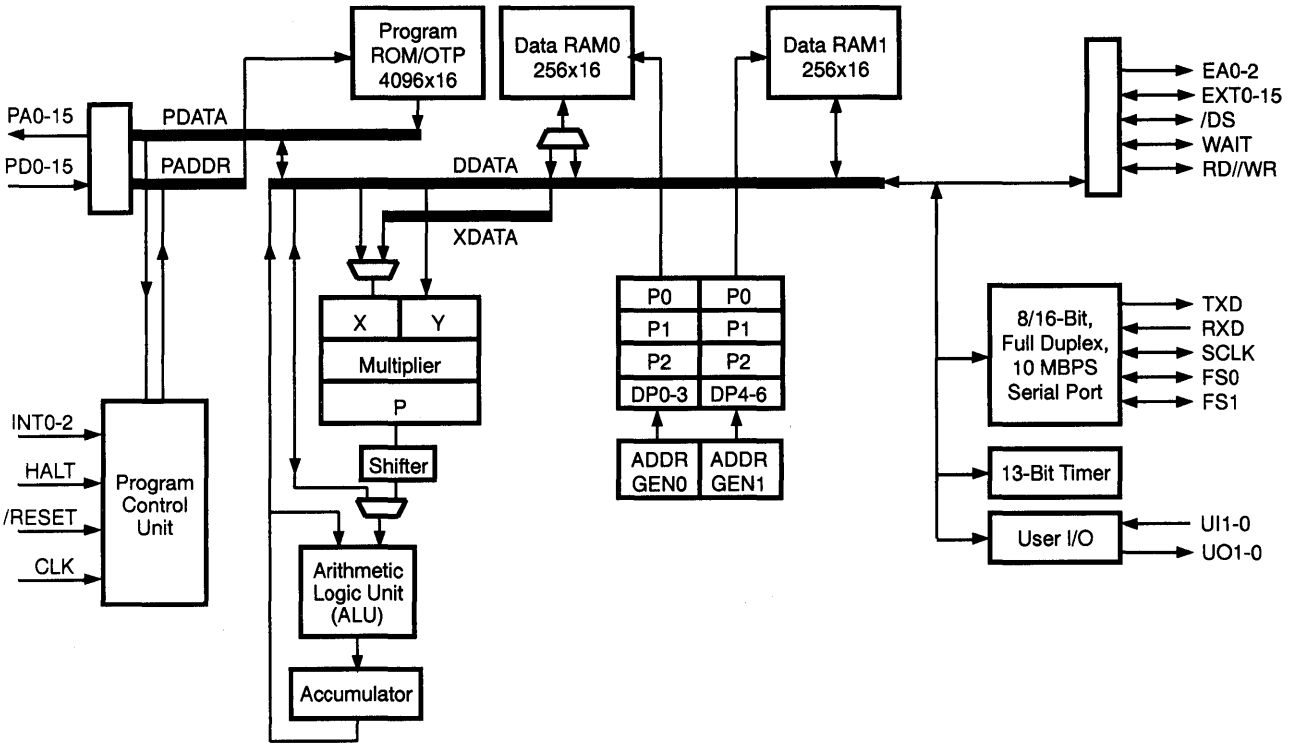
The Z89321/371/391 devices feature an on-board CODEC interface, compatible with 8-bit PCM and 16-bit CODECs for digital audio applications. Additionally, an on-board wait-state generator is provided to accommodate slow external peripherals.

For prototypes, as well as production purposes, the Z89371 member of the DSP product family is a one-time programmable (OTP) device with a 16 MHz maximum operating frequency.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}



Z89321/371/391 Functional Block Diagram

Z89390
16-BIT DIGITAL SIGNAL PROCESSOR

GENERAL DESCRIPTION

The Z89390 is a CMOS Digital Signal Processor (DSP). Single-cycle instruction execution and a Harvard bus structure promotes efficient algorithm execution. The processor contains 512 word data RAM and 64K word of external program address space is accessible. Six register pointers provide circular buffering capabilities and dual operand fetching. Three vectored interrupts are complemented by a six level stack. The CODEC interface enables high-speed transfer rates to accommodate digital audio and voice data. A dedicated Counter/Timer provides the necessary timing signals for the CODEC interface. An additional 13-bit timer is available for general-purpose use.

The Z89390 is optimized to accommodate intricate signal processing algorithms. The 20-MIP operating performance and efficient architecture provides real-time execution. Compression, filtering, frequency detection, audio, voice detection/synthesis and other available algorithms can all be accommodated. The on-board peripherals provide additional cost advantages.

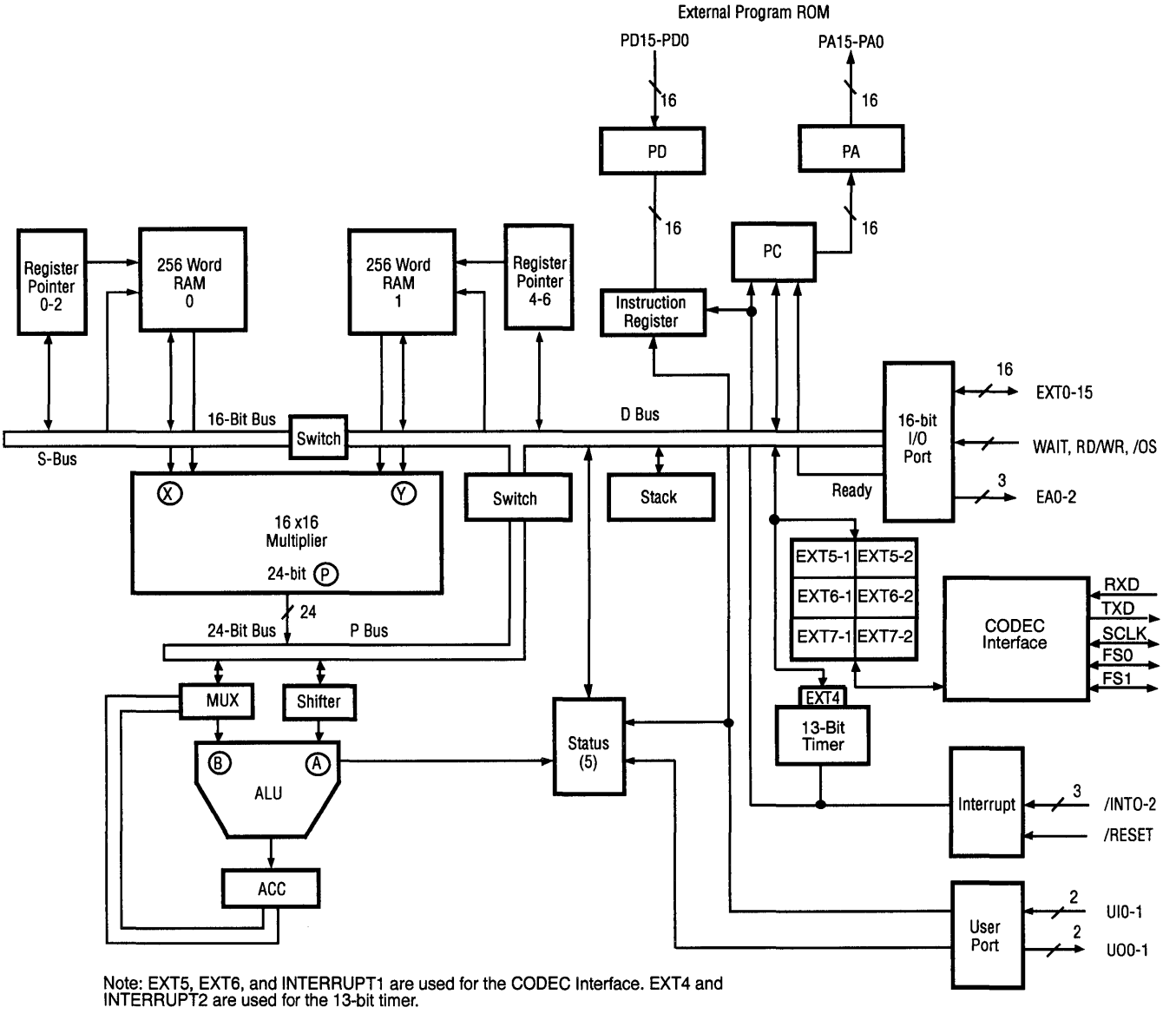
Development tools for the IBM PC include a relocatable assembler, a linker loader debugger.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Note: EXT5, EXT6, and INTERRUPT1 are used for the CODEC Interface. EXT4 and INTERRUPT2 are used for the 13-bit timer.

Z89391 Functional Block Diagram

Z89462

16-BIT, FIXED-POINT DIGITAL SIGNAL PROCESSOR

FEATURES

Part	Prog. RAM (K Words)	Prog./Data (K Words)	Data RAM (Words)	Speed (MHz)
Z89462	1	64	512	20, 40

- 100-Pin QFP and 124-Pin PGA Packages
- 0°C to +70°C Temperature Range
- 3.3- to 5.0-Volt Operating Range
  40 MHz Operation @ 5.0V
  20 MHz Operation @ 3.3V
- Six RAM Pointers for 4K-Word RAM Banks
- Three Maskable Vectored Interrupts, Edge or Level Trigger Selectable
- Enhanced Instruction Set
- Single-Cycle Instruction Execution
- Four-Stage Pipeline

On-Board Peripherals

- Dual 8/16-Bit CODEC Interface
- Wait-State Generator
- Two 16-Bit Timer/Counters
- Dynamic Program Bus Sizing

GENERAL DESCRIPTION

The Z89462 is a high-performance Digital Signal Processor (DSP) optimized for processing and transferring data. This enhanced processor provides an upward migration path for its Z89C00/Z89321 predecessors.

The DSP provides three 12-bit Register Pointers for each RAM bank. These pointers may be incremented or decremented automatically to implement circular buffers without software overhead.

Three prioritized and individually maskable interrupts are provided for use by external peripherals requiring service from the DSP. The interrupt inputs can be individually conditioned for edge or level trigger. Acknowledgement of an activated interrupt occurs at the end of an instruction execution.

Two banks of 512 x 16-bit data RAM are available. Expansion of the on-chip data RAM is provided through future upgrades.

External interfaces include Address Bus and Data Bus for external Program Memory, Address Bus and Data Bus for external Data Memory, three vectored interrupt ports, and two input/two output user ports.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

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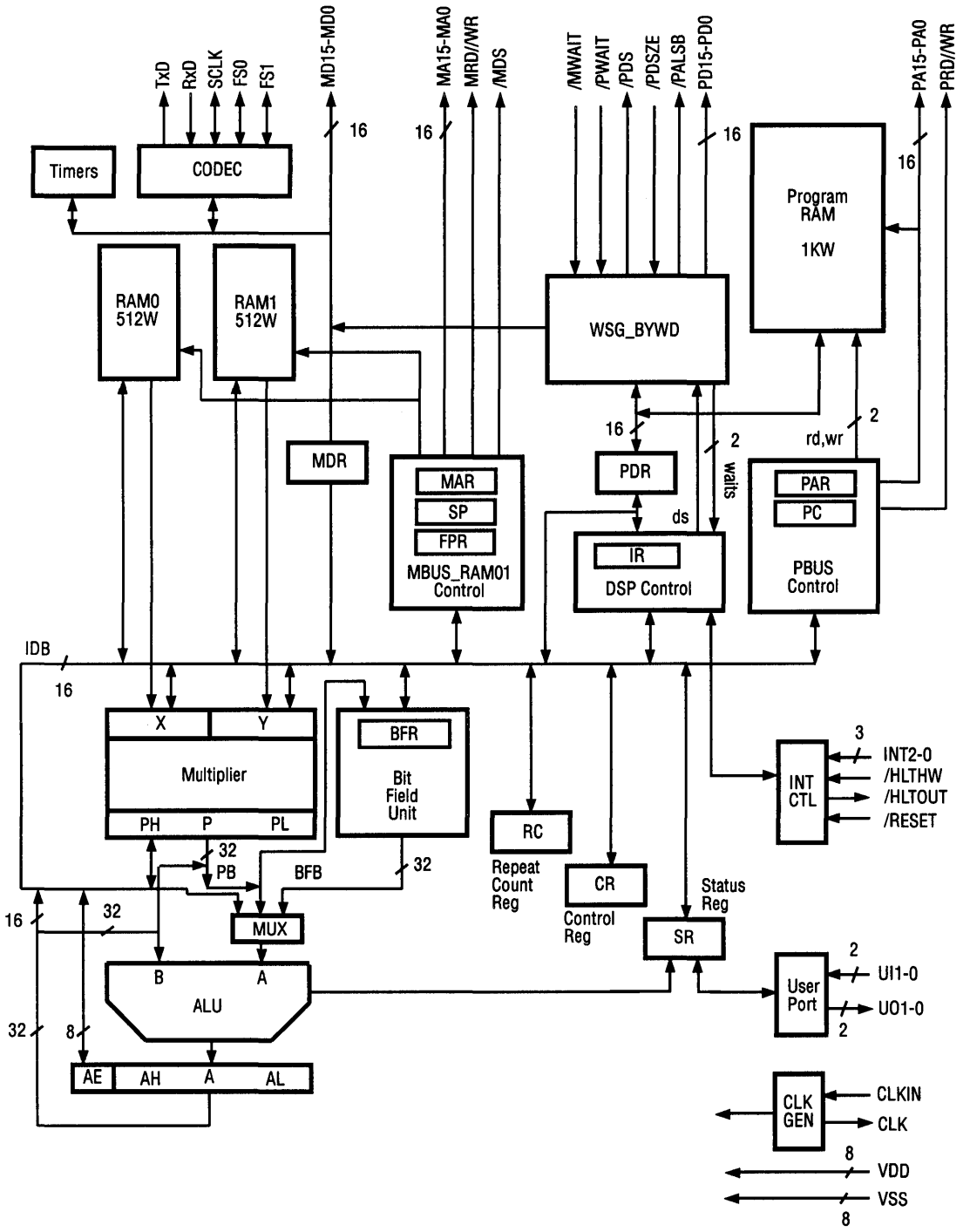
GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z8922300TSC
EMULATION MODULE

FEATURES

- Supported Devices

Packages	Emulation	OTP Programming
44-Pin PLCC	Z89223/273	N/A

- In-Circuit Emulation
- EPROM for Easy Code Change

GENERAL DESCRIPTION

The Z89223 Emulation Module can be used like a One-Time Programmable (OTP) for plug-in emulation of the Z89223 chip in user target applications. It provides external EPROMs to emulate an OTP and can be used repeatedly. Its electrical characteristics are nearly identical with the OTP.

Users can develop and debug their application software using a Z89323 ICEBOX™ Emulator (Z8932300ZEM) and transfer it to the EPROMs on the Emulation Module for final test.

SPECIFICATIONS

Dimensions

Width: 2.5 in. (6.35 cm)
Length: 3.4 in. (8.64 cm)
Height: 1.2 in. (3.05 cm)

Power Requirements

4.75 to 5.25 VDC (5.0 VDC typical)
300 mA maximum current

Operating Frequency

Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 10 MHz

Operating Conditions

Operating Temperature: 20°C ±10°C
Operating Humidity: 10-90% RH (non-condensing)

PACKAGE CONTENTS

Z8922300TSC Emulation Module

Z89393 ICE chip
Two (2) 32K x 8 EPROMs
44-Pin PLCC Socket Plug

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Z8922300ZAC
ACCESSORY KIT

FEATURES

- Supported Devices

Packages	Emulation	OTP Programming
44-Pin PLCC	Z89223/273	Z89273
44-Pin QFP	Z89223/273*	N/A

*Requires optional, separately purchased emulation pod, EPP-044-QF16-W, from Emulation Technology. 044-QF16-W, from Emulation Technology.

Emulation Technology, Inc.
2344 Walsh Ave., Bldg. F
Santa Clara, CA 95051-1301
FAX: 408-982-0664
TEL: 408-982-0660

- Cost-Effective Emulation Solution
- In-Circuit Emulation
- Cost-Effective Emulation Solution
- Programs OTPs
- Allows Use of Existing Emulator

GENERAL DESCRIPTION

The Z89223 Accessory Kit is specifically designed to enable the Z89323 ICEBOX™ Emulator to emulate Z89223/273 devices and program Z89273 OTPs.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C ± 10°C
Operating Humidity: 10-90% RH (non-condensing)

KIT CONTENTS

Hardware

44-Pin PLCC Programming Adapter
44-Pin PLCC Emulation Pod
44-Pin QFP Emulation Converter*
Two (2) 80-Pin Emulation Cables

Note: * Requires optional, separately purchased emulation pod, EPP-044-QF16-W, from Emulation Technology.

Documentation

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Z8922301TSC
EMULATION MODULE

FEATURES

- Supported Devices

Packages	Emulation	OTP Programming
44-Pin QFP	Z89223[1]	N/A

[1] Requires optional, separately purchased emulation pod, EPP-044-QF16-W, from Emulation Technology.

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Santa Clara, CA 95051-1301
FAX: 408-982-0664
TEL: 408-982-0660

- In-Circuit Emulation
- EPROM for Easy Code Change

GENERAL DESCRIPTION

The Z89223 Emulation Module is designed to be used like a One-Time Programmable (OTP) device for plug-in emulation of the Z89223 chip in user target applications. This module, with electrical characteristics that are nearly identical with the OTP, provides external EPROMs to emulate an OTP and can be used repeatedly.

Users can develop and debug their application software using a Z89323 ICEBOX™ Emulator (Z8932300ZEM) and transfer it to the EPROMs on the Emulation Module for final test.

SPECIFICATIONS

Dimensions

Width: 2.5 in. (6.35 cm)
Length: 3.4 in. (8.64 cm)

Power Requirements

4.75 to 5.25 VDC (5.0 VDC typical)
300 mA maximum current

Operating Frequency

Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 10 MHz

Operating Conditions

Operating Temperature: 20°C ±10°C
Operating Humidity: 10-90% RH (non-condensing)

PACKAGE CONTENTS

Z8922301TSC Emulation Module

- Z89393 ICE Chip
- Two (2) 32K x 8 EPROMs
- A 4-section connector for 44-Pin QFP emulation pod, PN: EPP-044-QF16-W, from Emulation Technology.

Documentation

User's Guide

SUPPORT PRODUCT

Z8932300ZEM

ICEBOX™ FAMILY
IN-CIRCUIT EMULATOR – 323

FEATURES

- Supported Devices

Packages	Emulation	OTP Programming
44-Pin PLCC	Z89223/273[1]	Z89273[1]
44-Pin QFP	Z89223[1] & [2]	N/A
68-Pin PLCC	Z89323/373	Z89373
80-Pin QFP	Z89323/373[3]	Z89373
84-Pin PLCC	Z89423/473[4]	Z89473[4]

1. Requires optional, separately purchased emulation pod, Z8922300ZAC, from Zilog.
2. Requires optional, separately purchased emulation pod, EPP-044-QF16-W, from Emulation Technology.
3. Requires optional, separately purchased emulation adapter, Z080QFP0ZET, from Zilog and emulation pod, EPP-080-QF08-W, from Emulation Technology.
4. Requires optional, separately purchased accessory kit, Z8942300ZAC, from Zilog. (Emulation Technology address is as follows.

   2344 Walsh Ave., Bldg. F
   Santa Clara, CA 95051-1301
   FAX: 408-982-0664
   TEL: 408-982-0660

- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Selectable Baud Rates – 9600 to 57.6 Kbps
- Window-Based User Interface
- RS-232 Connector
- DSP GUI Emulator Software
- ICE Pod Connector for Emulation
- HP-16500 Logic Analysis System Interface Connector

GENERAL DESCRIPTION

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The Z89323 Emulator is a member of Zilog's ICEBOX Z89223/323 product family of in-circuit emulators providing support for the Z89323 DSP family. The emulator provides essential DSP timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

The Z89323 Emulator provides users with a hardware platform to develop and debug software in a real-time environment as opposed to software simulators which provide significantly slower operation, making them less practical for DSP code development.

The Z89323 Emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature:	20°C, ±10°C
Supply Voltage:	+5 VDC, ± 5%
Minimum Emulation Speed:	1 MHz
Maximum Emulation Speed:	10 MHz

Power Requirements

+5 VDC @ 1.3A

Dimensions

Width:	6.25 in. (15.8 cm)
Length:	9.5 in. (24.1 cm)
Height:	2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine

33 MHz

4 MB RAM

VGA Video Adapter

Hard Disk Drive (1 MB free space)

3.5-inch, High-Density (HD) Floppy Disk Drive

RS-232C COM port

Mouse or Pointing Device

Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine

66 MHz (or faster)

8 MB of RAM (or more)

SVGA Video Adapter

Color Monitor

Printer

Kit Contents

Z89323 Emulator

- Emulation Base Board Includes:
  - CMOS Z86C9320GSC
  - 8K x 8 EPROM (Programmed with Debug Monitor)
  - 32K x 8 Static RAM
  - RS-232C Interface
  - Reset Switch
- Z89323 Emulation Daughterboard Includes:
  - Z8939320GSE DSP ICE Chip
  - 80-Pin Target Connector
  - 100-Pin HP-16500A Logic Analysis
  - System Interface Connector
  - 40-Pin DIP Zero Insertion Force (ZIF)
  - Reset Switch

Cables/Pods

- Power Cable with Banana Plugs
- DB25 RS-232C Cable
- 68-Pin PLCC Emulation Cable win/Pod

Programming adapter for both 68-Pin PLCC and 80-Pin QFP OTPs.

Host Software

- DSP GUI Emulator Software

Note: Cross-Assembler and C Compiler must be purchased separately from Zilog or Production Languages Corp. (817) 599-8363.

Documentation

Emulator User's Manual

Registration Card

Product Information

LIMITATIONS

1. Typing into the File Name box in order to change the drive in the file download and load symbol dialog boxes is not anticipated by the GUI. Instead, use the mouse in the Directories box as the workaround.

2. Switching ICEBOXes without quitting the GUI is not supported and may cause unexpected results.

3. The maximum loadable symbols is 32,768 provided there is enough system resource (memory).

4. The keyboard and mouse will lock up if the screen saver supplied by Windows 3.1 times out while the GUI software is waiting for the user to complete entering a line of assembly code in the Debug window. To recover, the user must reset the computer. The "Totally Twisted After Dark Screen Saver" version 3.2 and the Windows 95 screen saver both work fine. The workaround is to either turn off the screen saver, set the screen saver to much longer time out value, finish the line of code before the time-out occurs (press ENTER), or use a different screen saver such as "After Dark". This problem may also exist at other points in the GUI that request input from the user.

5. Although GUI 3.00 and later support baud rates up to 57.6K baud, the actual maximum usable rate may be less due to limitations of the user's hardware and or system software setup. The maximum usable rate is determined by the user's tolerance of the frequency of communication errors.

6. The initial blue Zilog screen can be distorted by other active windows. This only affects the appearance, not the functionality, of the GUI.

7. The GUI does not recognize the PUSH and POP instructions when entered in the In-Line Assembler (Debug window). As a workaround, use "LD STACK,xxx" for PUSH and "LD xxx,STACK" for POP.

8. The ICEBOX breakpoint hardware cannot distinguish between instruction and data fetches. Consequently, the breakpoint hardware triggers when the address specified matches either an instruction or data fetch.

   Example:

   ```
   0000   LD   A,#%0006
   0002   ADD  A,#%0002
   0003   LD   Y,@A
   0004   NOP
   0005   NOP
   0006   JP   %0000
   0008   NOP
   ```

   Setting a breakpoint at %0008 and clicking "GO" causes the code to break at %0004 due to the data fetch address match during the prior instruction. This anomaly does not occur during Animate mode because Animate mode does not use hardware breakpoints.

9. Interrupt will not work when accessing EXT registers while Wait State is enabled.

10. "ROM PROTECT" Option programming is temporarily disabled.

PRECAUTIONS

1. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point.

2. For some 386 PCs, the user is cautioned to set the baud rate to 19.2K or less because the Windows' communication driver does not guarantee "reliable" operation above 9600 baud. It is possible that on some slower 386 machines, selecting a high baud rate would crash the Windows' environment or result in excessive communication errors.

3. Pod Hazard. The user must exercise care to ensure the emulation pod is correctly aligned (pin-1 to pin-1) before inserting into the target system. An incorrectly aligned pod inserted into a target system may damage the emulator and/or the target system. The colored edge of the target cable denotes pin 1 and the connectors are keyed to only plug-in one way. Each emulation pod is marked with a "1" and/or a "triangle" to denote pin 1.

4. Breakpoint Overshoot. The Disassembly window shows the processor halting at one or two instructions past the instruction where the breakpoint was set.

5. Download File Name is not shown except at Time of Download. The emulator only shows the name of the file during the download process. To check the name of the file currently downloaded, select "File" and then "Download DSP Memory." The File Name box in the "Down to DSP Code Memory" window will reflect the file that is selected for download. Unlike our other emulators, the Debug window or Memory window does not show the name of the currently downloaded file.

6. Executing GUI. The GUI will occasionally continue to indicate Executing after it has been told to halt. Pushing the GO button will then result in Executing. (Executing showing at the top of the screen.)

7. The emulator cannot be operated while performing ESD/EMI testing on the target board.

8. When simultaneously running two different GUI versions on two different communication ports, the former executed version is used for both emulators. This is a problem related to the Windows operating system.

9. Port 0 is emulated by EXT3 of bank 1, 2, or 4. The ICEBOX emulates Port 0, bit 15 to bit 4 as input bits and bit 3 to bit 0 as output bits.

10. When emulating Port 0, the Wait State needs to be enabled to guarantee a reliable read and write.

11. Instruction SIEF should be added inside Interrupt Service Routine to re-enable interrupt.

12. When GUI 3.02 is used and the ICEBOX is executing a code in full speed, the interrupt will not work until the daughterboard RESET button (not the ICEBOX RESET button at back of emulator) is pressed.

13. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization should be disabled prior to invoking the VERIFY operation.

14. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

15. Do not press Hardware Reset when the ICEBOX is in the OTP dialog for programming. Close the OTP dialog box first, then reopen to reload the information back to the hardware.

    Note: The ICEBOX is really sitting idle, although Command Status shows "Processing" after the GUI re-establishes the communication link when "Retry" was selected in the "Out of Synchronization with the Emulator" dialog box.

16. Do not start the ICEBOX with OTP in socket.

17. A shorted PLCC or DIP OTP can crash the ICEBOX when inserted into the OTP programming socket. If a PLCC part is inserted in such a way as to cause a temporary short, then functionality is lost. An attempt to perform BLANK CHECK on such a part will cause the Windows hourglass to appear continuously. Windows must then be restarted.

Z8932301TSC
EMULATION MODULE

FEATURES

- Supported Devices

Packages	Emulation	OTP Programming
80-Pin QFP	Z89323/373[1]	Z89373

[1] Requires optional, separately purchased emulation pod, EPP-080-QF08-W, from Emulation Technology.

Emulation Technology, Inc.
2344 Walsh Ave., Bldg. F
Santa Clara, CA 95051-1301
FAX: 408-982-0664
TEL: 408-982-0660

- In-Circuit Emulation
- EPROM for Easy Code Change

GENERAL DESCRIPTION

The Z89323 Emulation Module is designed to be used like a One-Time Programmable (OTP) device for plug-in emulation of the Z89323/373 chips in user target applications. This module, with electrical characteristics that are nearly identical with the OTP, provides external EPROMs to emulate an OTP and can be used repeatedly. Users can develop and debug their application software using a Z89323 ICEBOX™ Emulator (Z8932300ZEM) and transfer it to the EPROMs on the Emulation Module for final test.

SPECIFICATIONS

Dimensions

Width: 3.3 in. (8.38 cm)
Length: 3.8 in. (9.65 cm)

Power Requirements

4.75 to 5.25 VDC (5.0 VDC typical)
300 mA maximum current

Operating Frequency

Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 10 MHz

Operating Conditions

Operating Temperature: 20°C ±10°C
Operating Humidity: 10-90% RH (non-condensing)

PACKAGE CONTENTS

Z8932301TSC Emulation Module

- Z89393 ICE Chip
- Two (2) 32K x 8 EPROMs
- A 4-section connector for 80-Pin QFP emulation pod, PN: EPP-080-QF08-W, Emulation Technology.

Documentation

User's Guide

Z8937100TSC

EMULATION MODULE

DESCRIPTION

The Z8937100TSC Emulation Module allows the user to plug programmed EPROMs into the board to verify operation of code before submitting for mask ROM.

The Z89371Emulation Module provides emulation for 20 MHz operation of the Z89321.

Supported Devices

Z89321/371

Specifications

Emulation Specification

Maximum Emulation Speed: 20 MHz

Power Requirements

+5 Vdc @ 100 mA from Target Board

Target Clock or Crystal Frequency

Up to 20 MHz

Operating Voltage Range

4.5V to 5.5V

Operating Temperature

0 to 70°C

Operating Humidity

10-90% RH (Non-Condensing)

KIT CONTENTS

Z8937100TSC Emulation Module

CMOS Z89391 DSP Processor
28-Pin 16K x 8 or 32K x 8 EPROM Socket
44-Pin PLCC Socket Plug

Documentation

Z8937100TSC Emulation Board User Guide

Ordering Information

Part Number: Z8937100TSC

Z8937100ZDF

QFP TO DIP PROGRAMMING ADAPTER

DESCRIPTION

The Z8937100ZDF Programming Adapter is used in conjunction with the Z8937100ZEM Icebox™. The adapter connects directly to the DIP programming socket to provide QFP programming capability.

Supported Devices

Z89371

Specifications

Power Requirements
+5 Vdc @ 100 mA from Emulator

Target Clock or Crystal Frequency
Provided by Emulator

Operating Voltage Range
4.5V to 5.5V

Operating Temperature
0 to 70°C

Operating Humidity
10-90% RH (Non-Condensing)

KIT CONTENTS

Z8937100ZDF Programming Adapter
40-Pin DIP Socket Plug
44-Pin QFP Socket

Documentation
Z8937100ZDF Specification Sheet

Ordering Information
Part Number: Z8937100ZDF

SUPPORT PRODUCT

Z8937100ZEM

ICEBOX™ FAMILY IN-CIRCUIT EMULATOR –371

FEATURES

- Supported Devices

Packages	Emulation	Programming
40-Pin DIP	Z89321/371	Z89371
44-Pin PLCC	Z89321/371	Z89371
44-Pin QFP	N/A	Z89371*
84-Pin PLCC	N/A	N/A

Notes:
*With optional separately purchased adapter, Z8937100ZDF.

- Dual CODEC Interface
- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Window-Based User Interface
- RS-232 Connector
- DSP GUI Emulator Software
- ICE Pod Connector for Emulation
- HP-16500 Logic Analysis System Interface Connector

GENERAL DESCRIPTION

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The Z8937100ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the Z89321/371/391 Digital Signal Processor (DSP) family.

The emulator provides essential DSP timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

The Z8937100ZEM provides users with a hardware platform to develop and debug software in a real-time environment as opposed to software simulators which provide significantly slower simulation, making them less practical for DSP code development.

The CODEC interface enables high-speed transfer rates to accommodate digital audio and voice data.

The Z8937100ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5 VDC, ± 5%
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 18 MHz

Power Requirements

+5 VDC @ 1.5A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

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HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z89371 Emulator

- Emulation Base Board Includes:
  CMOS Z86C9320PSC
  8K x 8 EPROM (Programmed with Debug Monitor)
  32K x 8 Static RAM
  RS-232C Interface
  Reset Switch

- Z89371 Emulation Daughterboard Includes:
  Z8939020VSC DSP ICE Chip
  80-Pin Target Connector
  100-Pin HP-16500A Logic Analysis System Interface Connector
  44-Pin PLCC Programming Socket
  40-Pin DIP Zero Insertion Force (ZIF) Programming Socket
  Reset Switch

Cables/Pods

Power Cable with Banana Plugs
DB25 RS-232C Cable
44-Pin PLCC Emulation Cable
40-Pin DIP Pod

Host Software

DSP GUI Emulator Software

Note: Cross-Assembler and C Compiler must be purchased separately from Zilog or Production Languages Corp. (817) 599-8363.

Documentation

Emulator User's Manual
Registration Card
Product Information

LIMITATIONS

1. Changing the drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The GUI does not recognize the PUSH and POP instructions when entered from In-Line Assembler. Use "LD STACK, xxx" for PUSH and "LD xxx, STACK" for POP instead.

3. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

4. Switching ICEBOXes without quitting the GUI is not supported.

5. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

6. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. Thus when a breakpoint is set in the GUI, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

```
0000    LD    A, #%0006
0002    ADD   A, #%0002
0003    LD    Y, @A
0004    NOP
0005    NOP
0006    JP    %0000
0008    NOP
```

   Setting the breakpoint at %0008 and click GO.

   Result: The code will break and stop at %0004.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

PRECAUTION LIST

1. HALT/Interrupt. There is a danger that Code memory will be modified if the GUI is stopped (either by halting or by setting a breakpoint) when interrupts are active. As a result: a. The user cannot restart the code without re-downloading it; b. Although the code breaks at the correctly set breakpoint, the GUI sometimes shows code breaking at the Interrupt Service Routine (ISR) entry point; c. All other windows are updated correctly except for Debug and Code windows.

   Workaround: Set Breakpoints only within the ISRs.

2. In 8-bit Mode, CODEC interface 0 and 1 must both be enabled for CODEC interface 1 to work properly.

3. UO0, UO1 are both Open-Drain.

4. Pod Hazard. The user must exercise care to ensure the emulation pod is correctly aligned (pin-1 to pin-1) before inserting into the target system. An incorrectly aligned pod inserted into a target system may damage the emulator and/or the target system. The colored edge of the target cable denotes pin 1 and the connectors are keyed to only plug-in one way. Each emulation pod is marked with a "1" and/or a "triangle" to denote pin 1.

5. Breakpoint Overshoot. The Disassembly window shows the processor halting at one or two instructions past the instruction where the breakpoint was set.

6. Should Not Start Emulator with OTP in Socket. The emulator may not start correctly if an attempt is made to start the emulator with a part in the programming socket.

7. A Shorted PLCC or DIP OTP Can Crash the Emulator. If a PLCC part is inserted in such a way as to cause a temporary short, then functionality is lost. An attempt to perform BLANK CHECK on such a part will cause the "Sand Glass" to appear continuously; it is necessary to reset windows and restart.

8. Download File Name is not shown except at Time of Download. The emulator only shows the name of the file during the download process. To check the name of the file currently downloaded, select "File" and then "Download DSP Memory." The File Name box in the "Down to DSP Code Memory" window will reflect the file that is selected for download. Unlike our other emulators, the Debug window or Memory window does not show the name of the currently downloaded file.

9. Disabling Peripherals Allows Use of EXT0-6. There is no internal register access for EXT4, 5, 6 except as used for their intended purposes, such as counter, and CODEC interface. EXT7 is essentially off limits as it is the CODEC interface control register.

10. Executing GUI. The GUI will occasionally continue to indicate Executing after it has been told to halt. Pushing the GO button will then result in Executing. (Executing showing at the top of the screen.)

11. Programming 44-pin PLCC Parts. When programming 44-pin PLCC parts, ensure Pin 1 orientation.

12. The ICEBOX™ is designed to program the Z89371 OTP devices with date code 9445 or later.

13. To reliably program the Z89371 OTP devices with date code 9445 or later, ensure the ICEBOX has the latest hardware revision (any ICEBOX purchased or repaired after March, 1995 or ICEBOX serial number with the last three digits that are 088 or higher).

14. The emulator cannot be operated while performing ESD/EMI testing on the target board.

15. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

16. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

17. The PLC Z89C00 Assembler RESET symbol in symbol table is fixed at 1000 when the assembly code contains "VECTOR RESET =" statement.

18. For 386 PCs, set the baud rate to 19.2K or less because the Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.

ZiLOG

SUPPORT PRODUCT

Z8939100ZCO

Z89391 DSP APPLICATION DEVELOPMENT KIT

HARDWARE FEATURES

Part	DSP ROM (K Words)	DSP RAM (Words)	Speed (MHz)	MIPS Core
Z89321	4	512	20	20
Z89371	4	512	16	16
Z89391	64*	512	20	20

* External

- Single-Cycle Multiply/ALU Operations
- External CODEC Interface
- Two Timers, CODEC, and General-Purpose
- 32K x 16 Zero Wait State External Program SRAM
  32K x 16 Zero Wait State External Data SRAM
  512 x 16 Zero Wait State Internal Data SRAM
- Prototype Area
- ICE Pod Connector for Emulation
- Seven LEDs and Buttons

GENERAL DESCRIPTION

The Z8939100ZCO Digital Signal Processor (DSP) Application Development Kit is a full-featured, flexible development tool for the Z893XX DSP family, including the Z89321 (ROM), Z89371 (EPROM), and the Z89391 (External ROM/RAM).

The Z89391 kit provides users with a hardware platform to develop and debug Z893XX software in a real-time environment as opposed to software simulators which provide significantly slower simulation, making them less practical for DSP code development.

The Z89391 kit provides basic digital and analog I/O to interface to other components of the user system, the Z89391 kit also provides a prototype area for users to customize the application hardware if necessary.

The Z89391 Development Board can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses the same Graphical User Interface (GUI) software as the Z89391 In-Circuit Emulator (ICEBOX™).

SUPPORTED DEVICES

Z89321 (ROM)
Z89371 (EPROM)
Z89391 (External ROM/RAM)

SPECIFICATIONS

Operating Conditions

Maximum DSP Speed: 20 MHz
Operating Temperature: 20°C, ±10°C
Supply Voltage: +5 VDC, ± 5%
-5 VDC, ± 5%
Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 20 MHz

Power Requirements

+5 VDC @ 1.5A
-5 VDC @ 100ma
(CODEC Supply Not Necessary if CODEC Not Used)

Dimensions

Width: 8.25 in. (21.0 cm)
Length: 10.5 in. (26.7 cm)
Height: 1.5 in. (3.8 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z89391 Development Board

Z8939120VSC
64Kx16 SRAM (Program Data)
8-Bit PCM CODEC
RS-232C Interface
Control Buttons and LEDs
Minijacks for CODEC Input/Output
Connectors for All DSP Signals
100-Pin HP-16500 Interface Board Connector

Cables

Power Cable with Banana Plugs
DB25 RS-232C Cable

Software

DSP GUI Emulator Software

Note:
Cross-Assembler and C Compiler are sold separately from Zilog or Production Languages Corp. Tel.: (817) 599-8363.

Documentation

Application Development Kit User's Manual
Registration Card
Product Information

LIMITATIONS

1. One-Time Programmable (OTP) programming is not supported.

2. Changing the drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

3. The GUI does not recognize the PUSH and POP instructions when entered from In-Line Assembler. Use "LD STACK, xxx" for PUSH and "LD xxx, STACK" for POP instead.

4. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

5. Switching ICEBOXes without quitting the GUI is not supported.

6. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

7. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. Thus when a breakpoint is set in the GUI, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

```
0000    LD    A, #%0006
0002    ADD   A, #%0002
0003    LD    Y, @A
0004    NOP
0005    NOP
0006    JP    %0000
0008    NOP
```

   Setting the breakpoint at %0008 and click GO.

   Result: The code will break and stop at %0004.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

8. Download File Name is not shown except at Time of Download. The emulator only shows the name of the file during the download process. To check the name of the file currently downloaded, select "File" and then "Download DSP Memory." The File Name box in the "Down to DSP Code Memory" window will reflect the file that is selected for download. Unlike other emulators, the Debug window or Memory window does not show the name of the currently downloaded file.

PRECAUTION LIST

1. Download Progress. The GUI code download status is not reflected correctly by the color bar download process indicator.

2. Pod Hazard. At the emulator connection, the red-line on the 40-PDIP pod ribbon correctly indicates pin 1; however, the red-line on the 40-PDIP pod ribbon does not indicate target pin 1. The pod should be connected to the target reference (shown on the pod that is actually opposite the red-line mark. A pod connected backwards may indicate a Z89C00 emulator instead of the Z89371 emulator.

3. Breakpoint Overshoot. The Disassembly window shows the processor halting at one or two instructions past the instruction where the breakpoint was set.

4. EXT4, 5, and 6 can be used as external registers only when disabled for their intended purposes, such as counter and CODEC interface. EXT7 is essentially off limits as it is the CODEC interface control register.

6. Executing GUI. The GUI will occasionally continue to indicate Executing after it has been told to halt. Pushing the GO button will then result in Executing. (Executing showing at the top of the screen.)

6. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

7. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

8. The PLC Z89C00 Assembler RESET symbol in symbol table is fixed at 1000 when the assembly code contains "VECTOR RESET =" statement.

9. For 386 PCs, set the baud rate to 19.2K or less because the Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.

Z8942300TSC

EMULATION MODULE – PROTO-PAK

FEATURES

- Supported Devices

Packages	Emulation	OTP Programming
84-Pin PLCC	Z89423/473	N/A

- In-Circuit Emulation
- EPROM for Easy Code Change

GENERAL DESCRIPTION

The Z89423 Emulation Module is designed to be used like a One-Time Programmable (OTP) device for plug-in emulation of the Z89423/473 chips in user target applications. This module, with electrical characteristics that are nearly identical with the OTP, provides external EPROMs to emulate an OTP and can be used repeatedly.

Users can develop and debug their application software using a Z89323 ICEBOX™ Emulator (Z8932300ZEM) and transfer it to the EPROMs on the Emulation Module for final test.

SPECIFICATIONS

Dimensions

Width: 2.5 in. (6.35 cm)
Length: 5.3 in. (13.46 cm)

Power Requirements

4.75 to 5.25 VDC (5.0 VDC typical)
300 mA maximum current

Operating Frequency

Minimum Emulation Speed: 1 MHz
Maximum Emulation Speed: 10 MHz

Operating Conditions

Operating Temperature: 20°C ±10°C
Operating Humidity: 10-90% RH (non-condensing)

PACKAGE CONTENTS

Z8942300TSC Emulation Module

- Z89323 QFP Proto-Pak
- Two (2) 32K x 8 EPROMs
- 84-Pin PLCC Adapter

Documentation

User's Guide

Z8942300ZAC
ACCESSORY KIT

FEATURES

- Supported Devices

Packages	Emulation	OTP Programming
84-Pin PLCC	Z89423/473	Z89473

- Cost-Effective Emulation Solution
- In-Circuit Emulation
- Programs OTPs
- Allows Use of Existing Emulator

GENERAL DESCRIPTION

The Z89423 (Z8942300ZAC) Accessory Kit is specifically designed as an enhancement to the Z89323 ICEBOX™ Emulator. This accessory kit enables the Z89323 Emulator to emulate the Z89423/473 devices and program Z89473 One-Time Programmable (OTP) devices.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C ± 10°C

Operating Humidity: 10-90% RH (non-condensing)

KIT CONTENTS

Hardware

- 84-Pin PLCC Programming Adapter
- 84-Pin PLCC Emulation Pod
- Two (2) 80-Pin Emulation Cables

Documentation

User's Guide

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SUPPORT PRODUCT

Z89C0000ZEM

ICEBOX™ FAMILY
IN-CIRCUIT EMULATOR –C00

HARDWARE FEATURES

- Supported Devices

Package	Emulation	Programming
68-Pin PLCC	Z89C00	N/A
40-Pin DIP	Z89320	N/A

- Real-Time Emulation
- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- DSP GUI Emulator Software
- Windows-Based User Interface
- RS-232 Connector
- ICE Pod Connector for Emulation

GENERAL DESCRIPTION

The Z89C0000ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the above listed DSP microcontroller devices.

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering, and program debugging, are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z89C0000ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5.0 VDC, ± 5%
Maximum Emulation Speed: 15 MHz

Power Requirements

+5.0 VDC @ 1.5A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z89C00 Emulator

- Emulation Base Board includes:
  - CMOS Z86C9320PSC
  - 8K x 8 EPROM (Programmed with Debug Monitor)
  - 32K x 8 Static RAM
  - RS-232C Interface
  - Reset Switch

- Z89C00 Emulation Daughterboard
  - 10 MHz Z89C00 ICE Chip
  - Four 64K x 4 Static RAM for Program RAM
  - 64K x 4 Static RAM for Breakpoints
  - 100-Pin HP Connectors
  - 60/80-Pin Target Connectors

Cables/Pods

Power Cable with Banana Plugs
DB25 RS-232C Cable
68-Pin PLCC Emulation Cable

Host Software

DSP GUI Emulator Software

Documentation

Emulator User Manual
Registration Card

LIMITATIONS

1. Changing the drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The GUI does not recognize the PUSH and POP instructions when entered from In-Line Assembler. Use "LD STACK, xxx" for PUSH and "LD xxx, STACK" for POP instead.

3. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

4. Switching ICEBOXes without quitting the GUI is not supported.

5. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

6. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. Thus when a breakpoint is set in the GUI, the breakpoint hardware triggers when the addresses match for either code or data fetches.

   Example:

```
0000    LD    A, #%0006
0002    ADD   A, #%0002
0003    LD    Y, @A
0004    NOP
0005    NOP
0006    JP    %0000
0008    NOP
```

   Setting the breakpoint at %0008 and click GO.

   Result: The code will break and stop at %0004.

   Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

PRECAUTION LIST

1. Breakpoint Overshoot. The Disassembly window shows the processor halting at one or two instructions past the instruction where the breakpoint was set.

2. Downloaded File Name Not Shown except at Time of Download. The emulator only shows the name of the file during the download process. To check the name of the file currently downloded, select "File" and then "Download DSP Memory." The File Name box in the "Download To DSP Code Memory" window will reflect the file that is selected for download. Unlike our other emulators, the Debug window or Memory window does not show the name of the currently downloaded file.

3. Executing GUI. The GUI will occasionally continue to indicate executing after it has been told to halt. Pushing the GO button will then result in executing. (Executing showing at the top of the screen).

4. The emulator cannot be operated while performing ESD testing on the target board.

5. Power Supply ramp-up/rise time must be such that when minimum power-on reset time (T_{POR}) expires, then the V_{CC} must be in the supported specified operating range of the device.

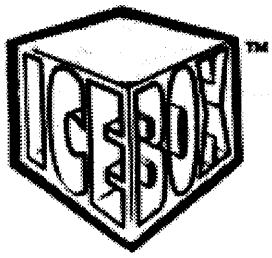
6. The ICEBOX cannot stop Timers and Interrupts at a breakpoint or during ICEBOX Halt operation or a single-step operation. The stack will overflow if an interrupt is enabled and the ICEBOX is in HALT, single-step, or breakpoint. (This is a limitation of the ICE chip.)

7. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

8. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

9. The PLC Z89C00 Assembler RESET symbol in symbol table is fixed at 1000 when the assembly code contains "VECTOR RESET =" statement.

10. For 386 PCs, set the baud rate to 19.2K or less because the Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selecting a high baud rate on some slower 386 machines may crash the Windows environment.



SUPPORT PRODUCT

Z89C0000ZHP

ICEBOX™ /H-P
LOGIC ANALYZER ADAPTER BOARD

DESCRIPTION

The ICEBOX/H-P Logic Analyzer Adapter Board provides the owner of a Hewlett-Packard Logic Analyzer (model #16500A) with real-time trace capabilities for the Zilog ICEBOX Emulator. The adapter board interfaces to the H-P Logic Analyzer probes and ICEBOX interface connector. At the touch of a button, the captured code can be disassembled, providing a complete listing of program flow in native assembly language on the analyzer screen. This simple and low-cost setup transforms the logic analyzer into a powerful tool for software debugging.

SUPPORTED DEVICES

L7X, C67/121, C65/120, C00

SPECIFICATIONS

Power Requirements

Not Applicable

Dimensions

Width: 4.9 in. (12.4 cm)
Length: 5.4 in. (13.7 cm)

KIT CONTENTS

ICEBOX/H-P Logic Analyzer Adapter Board
- 10 18-Pin DIP RC Network ICs
- 100-Pin ICEBOX Interface Connector
- 5 H-P 165XX Logic Analyzer Connectors

Cables

- 2", 100-Pin Cable

Software (IBM-PC Platform)

- Z89C00 Disassembler Software
- Z8® Disassembler Software**

Documentation

- H-P Adapter Board User Guide

** Future support.

* IBM is a registered trademark of International Business Machines Corp.

8

Z89C0000ZSM

Z89C00 SIMULATOR

GENERAL DESCRIPTION

The Z89C00 Simulator is designed to work with the PLC Z89C00 development tools to simulate code written with those tools.

The simulator interacts with the user through a user-defined, windowed interface. The user has complete control over what each window looks like, where it is located on the screen, when it is displayed, and what information the window contains. Thus, the simulator display may be tailored to a specific application.

Features include:

- Source code window
- All registers are displayed, and can be modified.
- Single step or operate at full speed.
- Break points can be set.
- Disassembler with line assembler.
- RAM and ROM windows.
- Clock/time count
- Mouse option for user interface

The Z89C00 (Z89SIM) requires an IBM® PC or true compatible with:

- DOS 3.2 or higher,
- a hard drive, and
- a floppy drive.

The real-mode version requires at least 640K of RAM.

The protected-mode version requires:

- an 80386 or 80486 CPU and
- 2 Mbytes of RAM with at least 1 Mbyte of extended memory free.

Device Supported
Z89C00

Kit Contents

Software (IBM PC platform)
Simulator

Documentation
Z89C00 Simulator User's Guide.
Registration Card

* IBM is a registered trademark of International Business Machines Corp.

Z89C2500ZCO

Z89C25 DEVELOPMENT BOARD

FEATURES

- Z182 Controller Code with AT Command Set
- DSP RAM Download Capability
- Headers for Logic Analyzer/Oscilloscope Probes
- Wire-Wrap Bread-Board Area
- RS-232 DB25 Port Interface
- V.24-Compatible Serial Port Interface
- Telephone/DAA Interface with RJ-11 Jack
- Piezo Speaker
- Power Supply for +/-12V, +5V with 12V AC Power Supply
- Operates from Single 12V AC Wall Adapter Power Supply
- Development Kit Software Included

GENERAL DESCRIPTION

The Z89C2500ZCO Development Board is an evaluation platform for the development and debugging of application code for the Z89C25 DSP. This board has been designed to support AT commands to the Z89C25 board and to download sample hex code to demonstrate the Z89C25.

Included on the evaluation board is a wire-wrap area that allows implementation of customer-specific circuitry. Additionally, the board provides header pins for logic analyzer/oscilloscope probes for monitoring DSP signals and two serial port interfaces (RS-232 and V.24-Compatible Serial Port with DB25 connectors). Typically, the RS-232 interface is used for connecting to the host, while the V.24-Compatible Serial Port Interface is used for direct communication with the DSP data pump.

SPECIFICATIONS

Dimensions

Length: 9.50 inches (23.75 cm)

Width: 6.80 inches (17 cm)

Operating Conditions

Temperature: 20°C +/-10°C,

Operating Humidity: 10-90% RH (non-condensing)

Power Requirements

Evaluation Board: 12V AC @ 1A (600 mA typical)

12V AC Wall Adapter: 120V AC, 60 Hz, 2-prong, USA-style plug

Interfaces

RS-232 DB25 Serial Interface for connection to the host

V.24-DB25-Compatible Serial Port Interface for direct communication with the DSP data pump

PACKAGE CONTENTS

Hardware

- Z89C25 Evaluation Board with Surface-Mounted C25 Chip
  - CMOS Z80182 Zilog Intelligent Peripheral
  - 24.576 MHz Crystal (for Z89C25 DSP)
  - 14.576 MHz Crystal (for Z80182)
- 12V AC Wall Adapter Power Supply
- RS-232 DB25 Male-to-Female Cable

Software

- Z89C25 Development Kit Diskette (3.5-inch HD)

Documentation

- Z89C2500ZCO Development Board User's Manual
- Z89C25 Preliminary Product Specification
- Registration Card

Additional Required Items Not Supplied with the Support Package

- Fax/Modem communications software (AT command set compatible), such as Procomm Plus, Delrina CommSuite, or others.
- IBM-PC (or 100-percent compatible) to run fax/modem software
- Telephone RJ-11 line cord

Communication Controllers

Z87000

SPREAD-SPECTRUM CONTROLLER

9

FEATURES

Device	ROM (KWords)	RAM* (Words)	I/O Lines	Package Information
Z87000	12	512	32	84-Pin PLCC 100-Pin QFP

Note: *General-Purpose

- Transceiver/Controller Chip Optimized for Implementation of 900 MHz Spread Spectrum Cordless Phone
  - Adaptive Frequency Hopping
  - Transmit Power Control
  - Error Control Signaling
  - Handset Power Management
  - Support of 32 kbps ADPCM Speech Coding for High Voice Quality
- DSP Core Acts as Phone Controller
  - Zilog-Provided Embedded Transceiver Software to Control Transceiver Operation and Base Station-Handset Communications Protocol
  - User-Modifiable Software Governs Phone Features
- Transceiver Circuitry Provides Primary Cordless Phone Communications Functions
  - Digital Downconversion with Automatic Frequency Control (AFC) Loop
  - FSK Demodulator
  - FSK Modulator
  - Symbol Synchronizer
  - Time Division Duplex (TDD) Transmit and Receive Buffers
- On-Chip A/D and D/A to Support 10.7 MHz IF Interface
- Bus Interface to Z87010 ADPCM Processor
- Static CMOS for Low Power Consumption
- 3.0V to 5.5V; -20°C to +70°C
- 16.384 MHz Base Clock

GENERAL DESCRIPTION

The Z87000 Cordless Phone Transceiver/Controller is expressly designed to implement a 900 MHz spread spectrum cordless phone compliant with US FCC regulations for unlicensed operation. The Z87000 supports a specific cordless phone system design that uses frequency hopping and digital modulation to provide extended range, high voice quality, and low system costs.

The Z87000 uses a Zilog 16-bit fixed-point two's complement static CMOS Digital Signal Processor core as the phone and RF section controller. The Z87000's DSP core processor further supports control of the RF section's frequency synthesizer for frequency hopping and the generation of the control messages needed to coordinate incorporation of the phone's handset and base station.

GENERAL DESCRIPTION (Continued)

Additional on-chip transceiver circuitry supports Frequency Shift Keying modulation/demodulation and multiplexing/demultiplexing of the 32 kbps voice data and 4 kbps command data between handset and base station. The Z87000 provides thirty-two I/O pins, including four wake-up inputs and two CPU interrupt inputs. These programmable I/O pins allow a variety of user-determined phone features and board layout configurations. Additionally, the pins may be used so that phone features and interfaces are supported by an optional microcontroller rather than by the Z87000's DSP core.

In combination with an RF section designed according to the system specifications, Zilog's Z87010 ADPCM Processor, a standard 8-bit PCM telephone codec and minimal additional phone circuity, the Z87000 and its embedded software provide a total system solution.

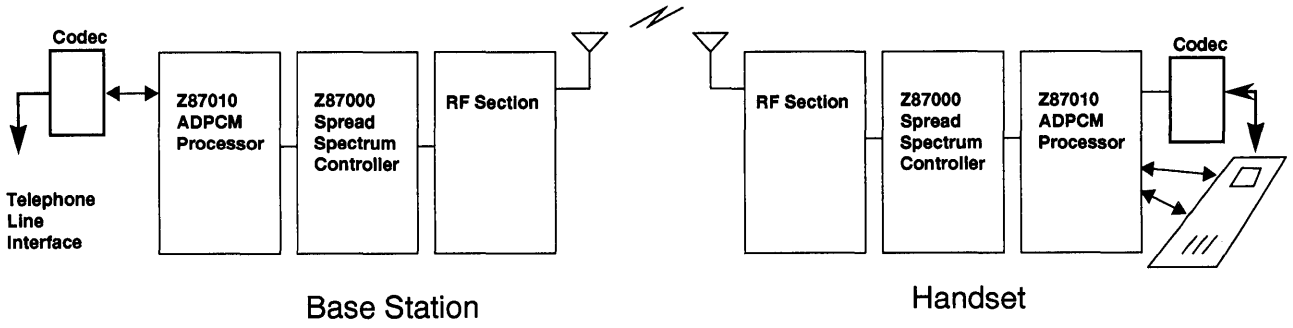


Figure 1. System Block Diagram of a Z87000/Z87010 Based Phone

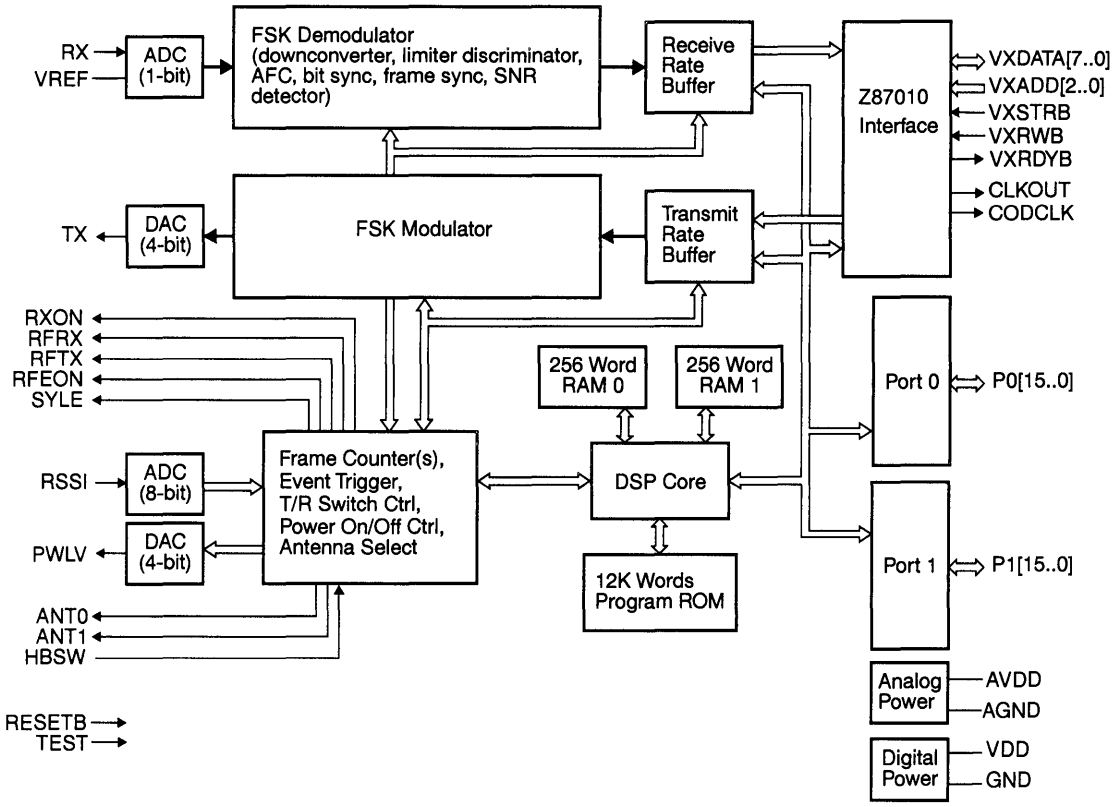


Figure 2. Z87000 Functional Block Diagram

Z87010
AUDIO ENCODER/DECODER

9

FEATURES

Device	ROM (Kbyte)	I/O Lines	Package Information
Z87010	4	16	44-Pin PLCC 44-Pin QFP

Hardware

- 16-Bit DSP Processor
- 3.0V to 5.5V; -20° to +70°C
- Static Architecture
- 512 Word On-Chip RAM
- Modified Harvard Architecture
- Direct Interface to Z87000 Frequency Hopping Spreader/Despreader
- Direct Interface to 8-Bit μ-law Telephone Codec
- I/O Bus (16-Bit Tristable Data, 3-Bit Address)
- Wait State Generator
- Two External Interrupts
- Four Separate I/O Pins (2 Input, 2 Output)

Software

- Full Duplex 32 Kbps ADPCM Encoding/Decoding
- Single Tone and DTMF Signal Generation
- Sidetone, Volume Control, Mute Functions
- Large Phone Number Memory (21 numbers of 23 digits each)
- Master-Slave Protocol Interface to Z87000 Spreader/Despreader

GENERAL DESCRIPTION

The Z87010 is a second generation CMOS Digital Signal Processor (DSP), that has been ROM-coded by Zilog to provide full-duplex 32 Kbps, Adaptive Delta Pulse Code Modulation (ADPCM) speech coding/decoding, and interface to the Z87000 Frequency Hopping Spreader and Despreader. Together the Z87000 and Z87010 support the implementation of a 900 MHz spread spectrum phone in conformance with United States FCC regulations for unlicensed operation.

The Z87010's single cycle instruction execution and Harvard bus structure promote efficient algorithm execution. The processor contains a 4K word program ROM and 512 word data RAM. Six dual operand fetching. Three vectored interrupts are complemented by a six level stack. The codec interface enables high-speed transfer rate to accommodate digital audio and voice data. A dedicated Counter/Timer provides the necessary timing signals for the codec interface. An additional 13-bit timer is dedicated for general-purpose use.

The Z87010's circuitry is optimized to accommodate intricate signal processing algorithms and is used here for speech compression/decompression, generation of DTMF tones and other cordless phone functions. Dedicated hardware allows direct interface to a variety of codec. As configured by the Zilog provided embedded software for digital cordless phones, a low cost 8-bit μ-law telephone codec is supported. The Z87010 is to be used with the Z87000 and operate at 16.384 MHz, where that provides 16 MIPS of processing power as needed for the cordless phone application.

GENERAL DESCRIPTION (Continued)

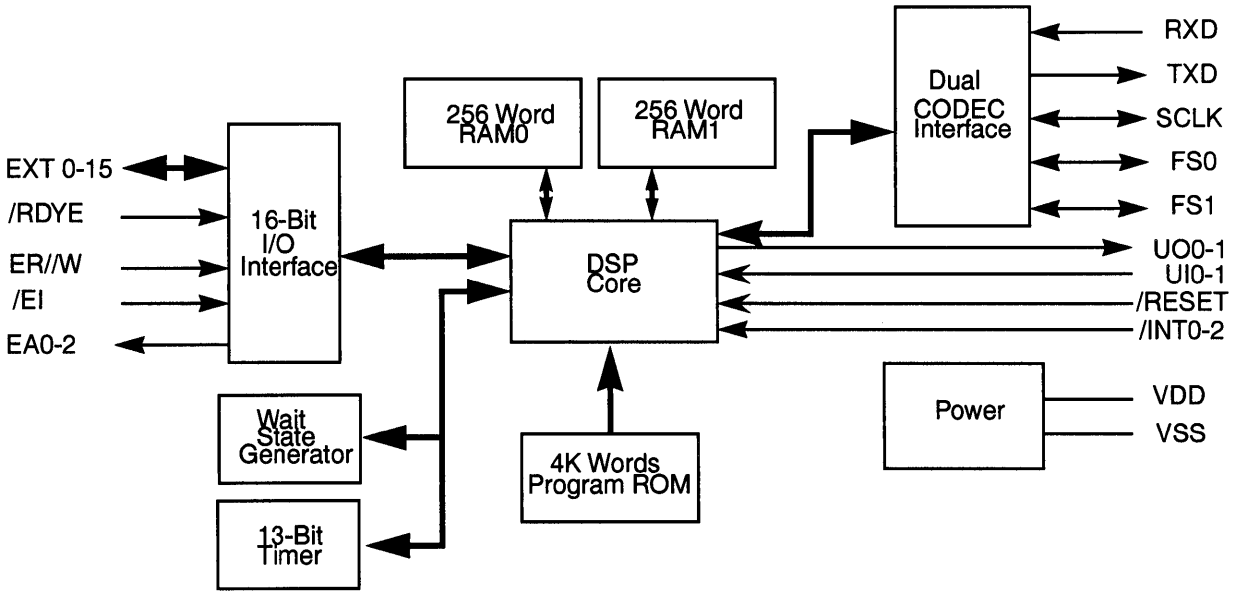


Figure 1. Z87010 Functional Block Diagram

Notes: All signals with a preceding front slash, '/', are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Z87021

TRANSMIT ONLY METER MODULE (TOMM)

FEATURES

Part	ROM (Kbytes)	RAM* (bytes)	SPEED (MHz)
Z87021	6	236	14

* General-Purpose

- 28-Pin SOIC and 44-Pin PLCC Packages
- 3.0- to 5.5-Volt Operating Range
- Low-Power Consumption
- –40° to +85°C Temperature Range
- 8-Bit Microcontroller (Z86C43) With Watch-Dog Timer (WDT) and Two 8-Bit Programmable Timer/Counters Plus Additional Custom Logic
- Digital ASIC Based on Zilog's Z8 Microcontroller Specificly designed for use in Electric TOMM and Gas TOMM
- 8-Bit Idle Timer for Microcontroller STOP Mode
- Alarm and Sensor Control/Detection
- Programmable 63-Chip Code Sequencer
- Two Analog Comparators
- DC Voltage Doubler Control Circuit
- Normal and Stop Mode Oscillator
- Interface support of External ROM and RAM for Small-Volume or New TOMM
- Low-Voltage Protection / Low-EMI Option

GENERAL DESCRIPTION

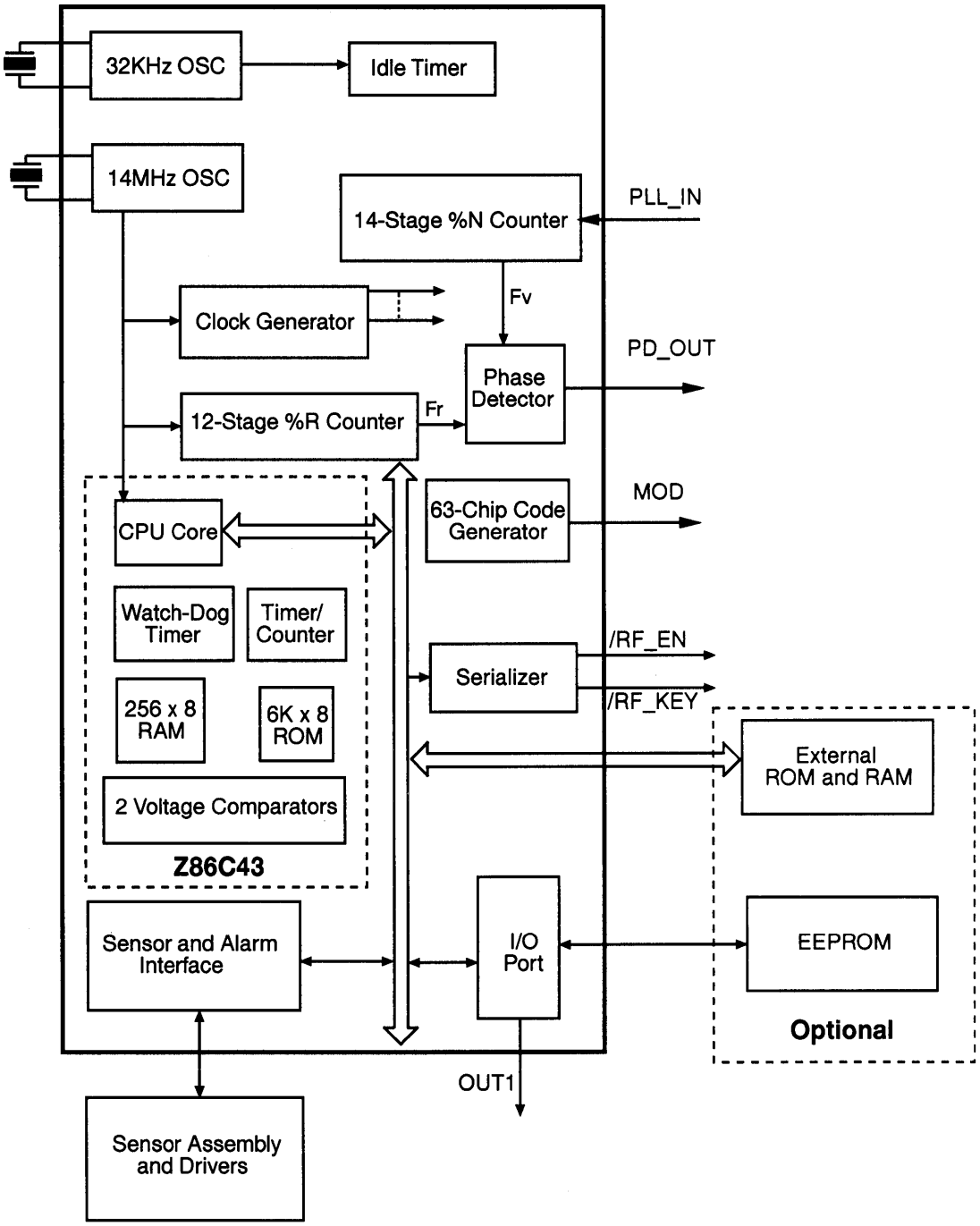
The Z87021 TOMM (Transmit Only Meter Module) is a member of the Z8® single-chip microcontroller family based on Zilog's 8-bit microcontroller core. The Z87021 is a digital ASIC device which supports and integrates all the digital control functions of the existing Electric TOMM and Gas TOMMs. It combines with RF ASIC to constitute the next generation ASIC TOMM.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

FUNCTIONAL DESCRIPTION



Functional Block Diagram

Z87100

PN MODULATOR WIRELESS TRANSMITTER

9

FEATURES

Part	ROM (Kbytes)	RAM* (Bytes)	Package Information
Z87100	1	124	18-pin DIP & SOIC

Note: *General-Purpose

- 3.0V to 5.5V Operating Range
- On-Chip PN Modulator for Spread Spectrum Communications
- ROM-Programmable PN Codes, up to 256 Bits ("Chips")
- Fast Instruction Pointer - 1.0 µs @ 12 MHz
- Two Standby Modes - STOP and HALT
- 12 Input/Output Lines (One with Comparator Input)
- Two Programmable 8-Bit Counter/Timers
- 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts (Two External, One Software Generated)
- Maximum Clock Speed of 12 MHz
- Watch-Dog/Power-On Reset Timer
- Analog Comparator with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a RC, or External Clock Drive
- Low EMI Noise Mode
- 0° to +70°C Ultra-Low Power Operation at 10 kHz

GENERAL DESCRIPTION

The Z87100 Wireless Controller is a member of the Z8® single-chip microcontroller family and is manufactured in CMOS technology. Zilog's CMOS Z87100 microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z87100 architecture is based on Zilog's 8-bit microcontroller core with the addition of an Expanded Register File which allows access to register mapped peripheral and I/O circuits. The Z87100 offers a flexible I/O scheme and a number of ancillary features that are useful in many consumer, industrial, automotive, and advanced scientific applications.

The Z87100 is designed with specific features for wireless spread spectrum applications using direct sequence pseudo-noise (PN) modulation. With up to 256 bits ("chips") of specially designated "PN ROM", one or more PN code sequences may be stored and used to PN-modulate data generated by the Z87100. PN modulation is synchronous with the data, using an integer number of PN chips per data bit.

The Z87100 features an Internal Time Base Counter which provides a real time clock for Stop-Mode Recovery or interrupt at programmable intervals of 0.25 seconds, one second, one minute and one hour. This requires an external clock oscillator signal at 32.768 kHz.

Special PN modulator control registers allow the user to select the desired PN modulator outputs, to choose the PN clock source and PN sequence start address in PN ROM, to stop/start and enable/disable the PN modulator, and to determine whether a complete PN code sequence is modulated against a single bit or an integer fraction or multiple of a single bit. The PN-modulated data may then be used

GENERAL DESCRIPTION (Continued)

with an external modulator and RF section to form a complete wireless spread spectrum transmitter.

The device's many applications demand powerful I/O capabilities. The Wireless Controller fulfills this with 12 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Three basic address spaces are available to support this wide range of configurations; Program Memory, Register File, and Expanded Register File. The Register File is composed of 124 bytes of General-Purpose Registers, two I/O Port registers and fifteen Control and Status registers. The Expanded Register File consists of two port registers, four control registers and six PN modulator registers.

With powerful peripheral features such as on-board comparators, counter/timers, Watch-Dog Timer, and PN modulator, the Z87100 meets the needs for most sophisticated wireless and low-power controller applications (Figure 1).

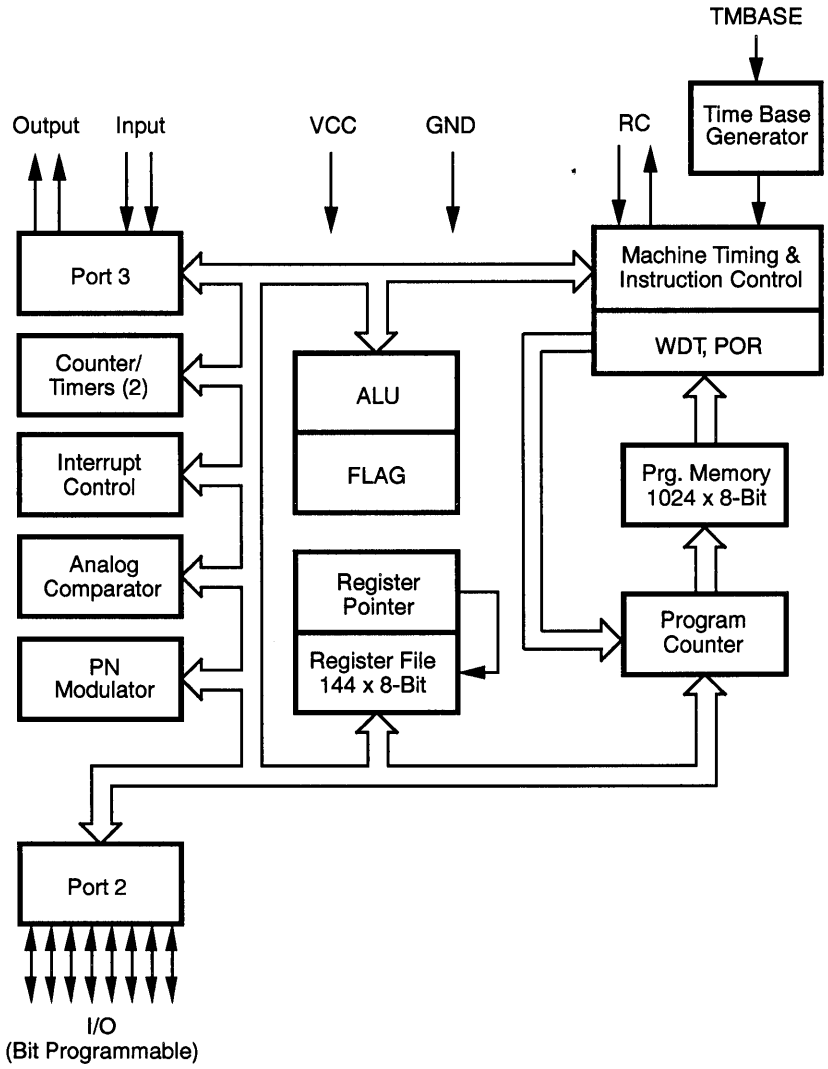


Figure 1. Functional Block Diagram

Z87200

SPREAD-SPECTRUM TRANSCEIVER

9

FEATURES

Device	Min PN Rate* (Mchips)	Max Data Rate* (Mbps)	Speed (MHz)	Package
Z87200	11	2.048	20/45	100-Pin PQFP

Note: *45 MHz only

- Complete Direct Sequence Spread-Spectrum Transceiver in a Single CMOS IC
- Programmable Functionality Supports Many Different Operational Modes
- Acquires Within One Symbol Duration Using Digital PN Matched Filter
- Two Independent PN Sequences, Each up to 64 Chips Long for Distinct Processing of the Acquisition/Preamble Symbol and Subsequent Data Symbols
- Power Management Features
- Optional Spectral Whitening Code Generation
- Full- or Half-Duplex Operation

Benefits

- High Performance and High Reliability for Reduced Manufacturing Costs
- Ideal for a Wide Range of Wireless Applications Including Data Acquisition Systems, Transaction Systems, and Wireless Local Area Networks (WLANs)
- Fast Response and Very Low Overhead when Operating in Burst Modes
- Allows High Processing Gain to Maximize the Acquisition Probability, then Reduced Code Length for Increased Data Rate
- Reduced Power Consumption
- Randomizes Data to Meet Regulatory Requirements
- Permits Dual Frequency (Frequency Division Duplex) or Single Frequency (Time Division Duplex) Operation
- Small Footprint, Surface Mount

GENERAL DESCRIPTION

The Z87200 is a programmable single-chip, spread-spectrum, direct-sequence transceiver. The Z87200 incorporates Stanford Telecom spread-spectrum and wireless technology and is identical to Stanford Telecom's STEL-2000A. By virtue of its fast acquisition capabilities and its ability to support a wide range of data rates and spread-spectrum parameters, the Z87200 spread-spectrum transceiver supports the implementation of a wide range of burst data communications applications.

Available in both 45- and 20-MHz versions, the Z87200 performs all the digital processing required to implement a fast-acquisition direct sequence (such as pseudonoise- or PN-modulated), spread-spectrum full- or half-duplex system. Differentially encoded BPSK and QPSK are fully supported. The receiver section can also handle differentially encoded pi/4 QPSK. A block diagram of the Z87200 is shown in Figure 1; its pin configuration is shown in Z87200 receive functions integrate the capabilities of a digital downconverter, PN matched filter, and DPSK demodulator, where the input signal is an analog-to-digital converted I.F. signal. Z87200 transmit functions include a differential BPSK/QPSK encoder, PN modulator (spreader), and BPSK/QPSK modulator, where the transmitter output is a sampled digitally modulated signal ready for external digi-

GENERAL DESCRIPTION (Continued)

tal-to-analog conversion (or, if preferred, the spread baseband signal may be output to an external modulator).

These transceiver functions have been designed and integrated for the transmission and reception of bursts of spread data. In particular, the PN Matched Filter has two distinct PN coefficient registers (rather than a single one) in order to speed and improve signal acquisition performance by automatically switching from one to the other upon signal acquisition. The Z87200 is thus optimized to provide reliable, high-speed wireless data communications.

Symbol-Synchronous PN Modulation

The Z87200 operates with symbol-synchronous PN modulation in both transmit and receive modes. Symbol-synchronous PN modulation refers to operation where the PN code is aligned with the symbol transitions and repeats once per symbol. By synchronizing a full PN code cycle over a symbol duration, acquisition of the PN code at the receiver simultaneously provides symbol synchronization, thereby significantly improving overall acquisition time.

As a result of the Z87200's symbol-synchronous PN modulation, the data rate is defined by the PN chip rate and length of the PN code; that is, by the number of chips per symbol, where a "chip" is a single "bit" of the PN code. The PN chip rate, R_c chips/second, is programmable to as much as 1/4 the rate of RXIFCLK, and the PN code length, N, can be programmed up to a value of 64. When operating with BPSK modulation, the data rate for a PN code of length N and PN chip rate R_C chips/sec is R_C/N bps. When operating with QPSK modulation (or $\pi/4$ QPSK with an external modulator), two bits of data are transmitted per symbol, and the data rate for a PN code of length N and PN chip rate R_c chips/sec is $2R_c/N$ bps. Conversely, for a given data rate R_b bps, the length N of the PN code defines the PN chip rate R_c as $N \times R_b$ chips/sec for BPSK or as $(N \times R_b)/2$ chips/sec for QPSK.

The data rate R_b and the PN code length N, however, cannot generally be arbitrarily chosen. United States FCC Part 15.247 regulations require a minimum processing gain of 10 dB for unlicensed operation in the Industrial, Scientific, and Medical (ISM) bands, implying that the value of N must be at least 10. To implement such a short code, a Barker code of length 11 would typically be used in order to obtain desirable auto- and cross-correlation properties, although compliance with FCC regulations depends upon the overall system implementation. The Z87200 further includes transmit and receive code overlay generators to insure that signals spread with such a short PN code length possess the spectral properties required by FCC regulations.

The receiver clock rate established by RXIFCLK must be at least four times the receive PN spreading rate and is limited to a maximum speed of 45.056 MHz in the 45 MHz Z87200 and 20.0 MHz in the 20 MHz Z87200. The ensuing discussion is in terms of the 45 MHz Z87200, but the numerical values may be scaled proportionately for the 20 MHz version. As a result of the maximum 45.056 MHz RXIFCLK, the maximum supported PN chip rate is 11.264 Mchips/second. When operating with BPSK modulation, the maximum data rate for a PN code of length N is 11.264/N Mbps. When operating with QPSK modulation (or $\pi/4$ QPSK with an external modulator), two bits of data are transmitted per symbol, and the data rate for a PN code of length N is 22.528/N Mbps. Conversely, for a given data rate R_b, the length N of the PN code employed must be such that the product of $N \times R_b$ is less than 11.264 Mchips/sec (for BPSK) or 22.528 Mchips/sec (for QPSK). For the 45 MHz Z87200, then, a PN code length of 11 implies that the maximum data rate that can be supported in compliance with the processing gain requirements of FCC regulations is 2.048 Mbps using differential QPSK. Note again, however, that FCC compliance using the Z87200 with a PN code of length 11 depends upon the overall system implementation.

Z87200 I.F. Interface

The Z87200 receiver circuitry employs an NCO and complex multiplier referenced to RXIFCLK to perform frequency downconversion, where the input I.F. sampling rate and the clock rate of RXIFCLK must be identical. In "complex input" or Quadrature Sampling Mode, external dual analog-to-digital converters (ADCs) sample quadrature I.F. signals so that the Z87200 can perform true full single sideband downconversion directly from I.F. to baseband. At PN chip rates less than one-eighth the value of RXIFCLK, downconversion may also be effected using a single ADC in "real input" or Direct I.F. Sampling Mode.

The input I.F. frequency is not limited by the capabilities of the Z87200. The highest frequency to which the NCO can be programmed is 50% of the I.F. sampling rate (the frequency of RXIFCLK); moreover, the signal bandwidth, NCO frequency, and I.F. sampling rate are all interrelated, as discussed in Higher I.F. frequencies, however, can be supported by using one of the aliases of the NCO frequency generated by the sampling process. For example, a spread signal presented to the Z87200's receiver ADCs at an I.F. frequency of $f_{I.F.}$, where $f_{RXIFCLK} < f_{I.F.} < 2 \times f_{RXIFCLK}$, can generally, as allowed by the signal's bandwidth, be supported by programming the Z87200's NCO to a frequency of $(f_{I.F.} - f_{RXIFCLK})$, as discussed in Appendix A of this product specification. The maximum I.F. frequency is then limited by the track-and-hold capabilities of the ADC(s) selected. Signals at I.F. frequencies up to about 100 MHz can be processed by currently available 8-bit ADCs, but the implementation cost as well as the performance can typically be improved by using an I.F. frequency of 30 MHz or lower. Downconversion to baseband is then accomplished digitally by the Z87200, with a programmable loop filter provided to establish a frequency tracking loop.

Burst and Continuous Data Modes

The Z87200 is designed to operate in either burst or continuous mode: in burst mode, built-in symbol counters allow bursts of up to 65,533 symbols to be automatically transmitted or received; in continuous mode, the data is simply treated as a burst of infinite length. The Z87200's use of a digital PN Matched Filter for code detection and despreading permits signal and symbol timing acquisition in just one symbol. The fast acquisition properties of this design are exploited by preceding each data burst with a single Acquisition/Preamble symbol, allowing different PN codes (at the same PN chip rate) to independently spread the Acquisition/Preamble and data symbols. In this way, a long PN code with high processing gain can be used for the Acquisition/Preamble symbol to maximize the probability of burst detection, and a shorter PN code can be used thereafter to permit a higher data rate.

To improve performance in the presence of high noise and interference levels, the Z87200 receiver's symbol timing recovery circuit incorporates a "flywheel circuit" to maximize the probability of correct symbol timing. This circuit will insert a symbol clock pulse if the correlation peak obtained by the PN Matched Filter fails to exceed the programmed detect threshold at the expected time during a given symbol. During each burst, a missed detect counter tallies each such event to monitor performance and allow a burst to be aborted in the presence of abnormally high interference. A timing gate circuit further minimizes the probability of false correlation peak detection and consequent false symbol clock generation due to noise or interference.

To minimize power consumption, individual sections of the device can be turned off when not in use. For example, the receiver circuitry can be turned off during transmission and, conversely, the transmitter circuitry can be turned off during reception when the Z87200 is operating in a half-duplex/time division duplex (TDD) system. If the NCO is not being used as the BPSK/QPSK modulator (that is, if an external modulator is being used), the NCO can also be turned off during transmission to conserve still more power.

Conclusion

The fast acquisition characteristics of the Z87200 make it ideal for use in applications where bursts are transmitted relatively infrequently. In such cases, the device can be controlled so that it is in full "sleep" mode with all receiver, transmitter, and NCO functions turned off over the majority of the burst cycle, thereby significantly reducing the aggregate power consumption. Since the multiply operations of the PN Matched Filter consume a major part of the overall power required during receiver operation, two independent power-saving techniques are also built into the PN Matched Filter to reduce consumption during operation by a significant factor for both short and long PN spreading codes.

The above features make the Z87200 an extremely versatile and useful device for spread-spectrum data communications. Operating at its highest rates, the Z87200 is suitable for use in wireless Local Area Network implementations, while its programmability allows it to be used in a variety of data acquisition, telemetry, and transaction system applications.

GENERAL DESCRIPTION (Continued)

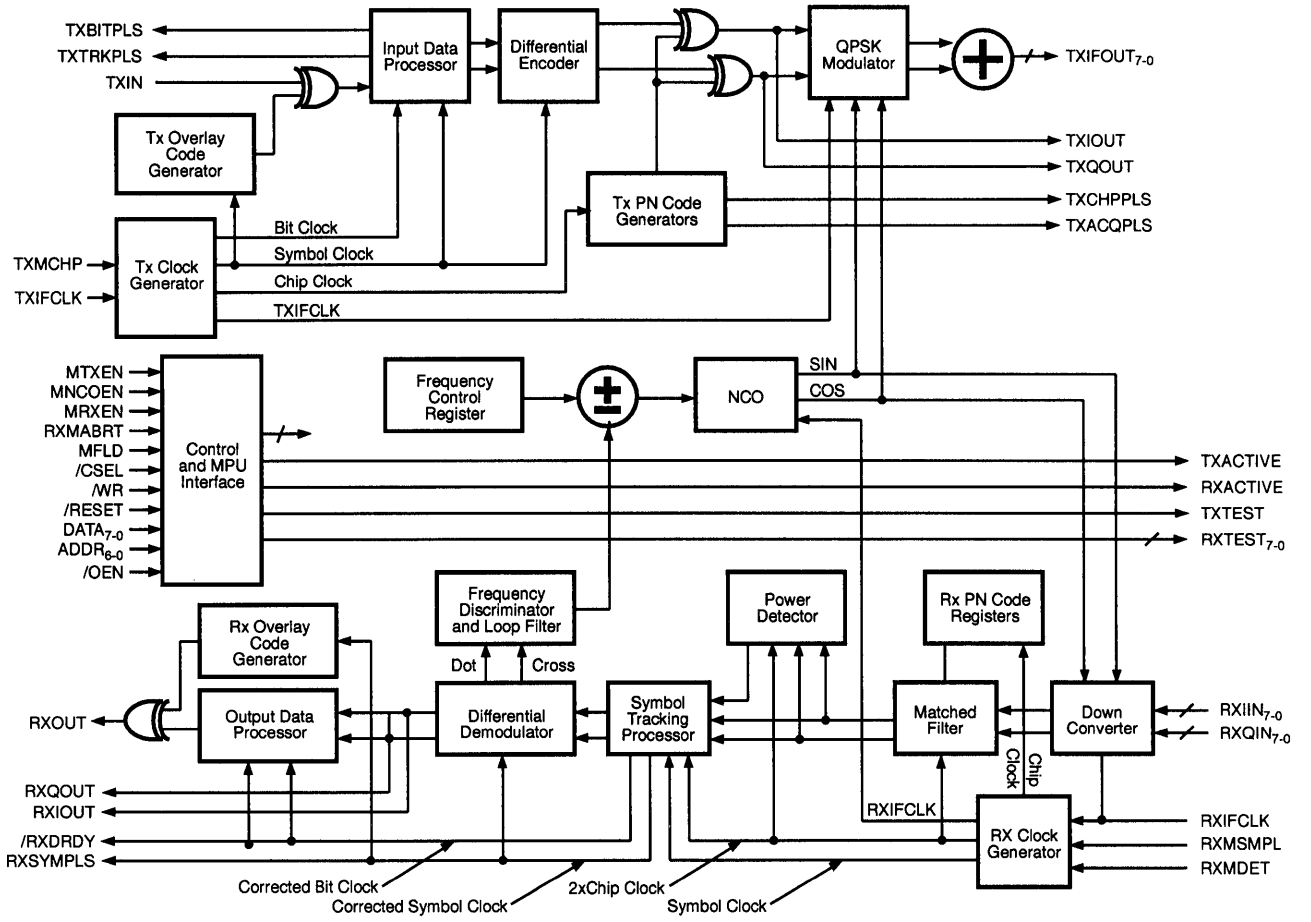


Figure 1. Z87200 Block Diagram

Z8700000TSC
EMULATION MODULE

FEATURES

The Z870000TSC Emulation Module allows the user to plug programmed EPROMs into the board to verify operation of code before submitting for mask ROM.

The Z870000TSC Emulation Module provides emulation for 16.384 MHz operation for the Z87000.

Supported Devices

Z8700016VSC

Specifications

Emulation Specification
Maximum Emulation Speed: 16.384 MHz

Power Requirements
+5 Vdc @ 100 mA from Target Board

Target Clock or Crystal Frequency
16.384 MHz

Operating Voltage Range
4.0V to 5.5V

Operating Temperature
-40°C to +85°C

Operating Humidity
10-90% RH (Non-Condensing)

KIT CONTENTS

Z8700000TSC Emulation Module

CMOS Z87001 Cordless Phone Transceiver/Controller ICE Chip
Two 28-Pin 16K x 8 EPROM Socket
84-Pin PLCC Socket Plug

Documentation

Z8700000TSC Emulation Board User Guide

Ordering Information

Part Number: Z8700000TSC

Z8700000ZEM
IN-CIRCUIT EMULATOR

HARDWARE FEATURES

- Supported Products

Packages	Emulation	Programming
84-pin PLCC 100-pin QFP	Z87000	N/A

- Real-Time Emulation
- DSP GUI Emulator Software
- Windows-Based User Interface
- RS-232 Connector
- ICE Pod Connector for Emulation

GENERAL DESCRIPTION

The Z8700000EM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the above listed DSP microcontroller devices.

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering and program debugging are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z8700000ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C ±10°C
Supply Voltage +5.0 VDC , ±5%
Maximum Emulation Speed: 16.384 MHz

Power Requirements

+5.0 VDC @ 0.5A Minimum

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB or RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z87000 Emulator

- Emulation Base Board includes:
  CMOS Z86C9320VSC
  8K x 8 EPROM (Programmed with Debug Monitor)
  32K x 8 Static RAM
  RS-232C Interface
  Reset Switch
- Z87000 Emulation Daughterboard
  16 MHz CMOS Z86C1216GSE ICE Chip
  64K x 4 Static RAM
  Two 32K x 4 Static RAM for Breakpoints
  Two 80-pin Target Connectors
  Mini-Coax with SMA Connectors

Cables/Pods

Power Cable with Banana Plugs
DB25 RS-232C Cable
84-Pin PLCC Emulation Pod Cable
Mini-Coax with SMA Connectors

Host Software

DSP GUI Emulator Software

Note: Cross-Assembler and C Compiler are sold separately from Zilog or Production Languages, Tel: (817) 599-8363

Documentation

Emulator User's Manual
Registration Card
Product Information

LIMITATIONS

1. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The GUI does not recognize the PUSH and POP instructions when entered from In-Line Assembler. Use "LD STACK, xxx' for PUSH and "LD xxx, STACK" for POP instead.

3. The initial blue Zilog screen will be distored by other active windows. This only affects the appearance, not functionality, of the GUI.

4. Switching ICEBOXes without quitting the GUI is not supported.

5. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

6. Download File Name is not shown except at Time of Download. The emulator only shows the name of the file during the download process. To check the name of the file currently downloaded, select "File" and then "Download DSP Memory." The File Name box in the "Down to DSP Code Memory" window will reflect the file that is selected for download. Unlike other emulators, the Debug window or Memory window does not show the name of the currently downloaded file.

7. The ICEBOX breakpoint hardware does not distinguish between instruciton and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

Z8700001ZCO
DEVELOPMENT KIT

FEATURES

- Supported Devices

Packages	Evaluation	Programming/ Emulation
100-Pin QFP	Z8700016FSC	N/A
84-Pin PLCC	Z8700016VSC	N/A
44-Pin QFP	Z8701016FSC	N/S
44-Pin PLCC	Z870106VSC	N/A

- Two Jumper Configurable Circuit Boards
- Supports Real-Time Code Trace
- Direct Connect Logic Analyzer Probe Points
- Hosts Z87000 Emulation Tools
- Voice Processing Capability
- Z87010 ADPCM Encoder/Decoder

GENERAL DESCRIPTION

Zilog's Z87000 Development Kit is a member of the support tool family providing demonstrations and evaluation of spread-spectrum cordless phone transceiver/controllers.

Z8700001ZCO kit includes two identical circuit boards and the hardware required to operate as a cordless telephone handset or base. Each circuit board contains a Z87000 spread-spectrum transceiver/controller and a Z87010 ADPCM encoder/decoder.

The kit enables jumper connection of the cordless phone handset and base at intermediate frequency (IF). This configuration demonstrates the voice processing quality of the Z87000 system.

The kit circuit boards are socketed for easy replacement of the Z87000 spread-spectrum transceiver/controller with either the Zilog Z8700000ZEM ICEBOX™ in-circuit emulator or Z870000TSC emulation module as a platform for software development.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5 VDC
Evaluation Speed: 16.384 MHz

Power Requirements

+5 VDC @ 1.5A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Telephone Interface

RJ11 Plug

KIT CONTENTS

Two Z87000 Evaluation Boards

Evaluation Base Board:
CMOS Z8700016VSC

CMOS Z870106VSC or Z89371116VSC
(Programmable OTP for the Z87010)

Telephone Hybrid

Telephone Keypad

RJ14 Telephone Handset Interface

RJ11 Telephone Line Interface

Two (32K X 8) Static RAM

(32K x 4) Static RAM for Breakpoints

2 x 80-pin Target Connectors

Two 100-Pin HP-16500A Logic Analyzer
Interface Connector

Cables

Two IF Interface Cables
Two Telephone Handsets with Cords
One Telephone Line with RJ11 Plugs

Documentation

Zilog Z87000 Z-Phone Development User's Manual
Registration Card
Product Information Sheet

PRECAUTIONS

1. The Z87000 R2017, when configured as the handset unit, will sometimes reset itself due to stack overflow. A possible workaround is to reset the base.

2. Pulse dialing does not work due to incorrect software polarity control.

Note: The problems listed in Precautions Number 1 and Number 2 do not occur when using the Z87000 Emulation Module (Proto-Pack, Zilog part number: Z870000TSC), or the Z87000 ICEBOX Emulator (Zilog part number: Z870000ZEM), instead of the Z87000 R2017 device. Contact The Wireless Group at Zilog for the latest software updates to use with the Proto-Pack and emulator. (Zilog address information follows.)

DOCUMENTATION ERRATA

Refer to the Z87000 ZPhone™ Development Kit User's Manual, Chapter 1, "Introduction." The Z8937116VSC is shipped instead of the Z87010. The Z8937116VSC is the one-time programmable device versions of the Z87010 that is programmed with the latest Z87010 ROM code.

Z8720000ZCO
EVALUATION KIT

HARDWARE FEATURES

- Supported Devices

Packages	Emulation	Programming
100-pin QFP	Z8720045FSC	N/A
100-pin QFP	Z8018216FSC	N/A

- Fully Programmable Transmitter and Receiver
- Programmable Intermediate Frequency
- Intermediate Frequency and Baseband Inputs/Outputs
- 16550 MIMIC Interface
- IBM PC Plug-In I/O
- Configurable as a Stand-Alone System
- ESCC™ Ports and S180 Microprocessor Core

GENERAL DESCRIPTION

Zilog's Z87200 Evaluation Board is a member of the support tool family providing a development platform to implement data communication applications based onthe Z87200 Spread-Spectrum Burst Processor and the Z80182 Intelligent Modem Controller.

The Z8720000ZCO kit includes an evaluation board operating at baseband, a Z87200 spread-spectrum processor with programmable intermediate frequency, firmware, and host PC software.

Baseband control and interface functions are supported by the Z80182 Enhanced Serial Communications Controller (ESCC™) ports and S180 microprocessor core. The Z87200 spread-spectrum transmitter and receiver are fully programmable and may be monitored through a variety of test points. The board also provides inputs and outputs at both Intermediate Frequency and baseband to allow connection to a user provided RF section or the Zilog loopback board.

SPECIFICATIONS

Power Requirements

+5V, 12V DC

Dimensions (PC AT Board)

Width: 4.3 in
Length: 9.7 in

Serial Interface

26-Pin Header for RS-232-C
(Data Rates up to 115.2 Kbps)
DB25 RS-422 (EIA-530)
(Data Rates up to 4 Mbps)

KIT CONTENTS

Z87200 Evaluation Board
CMOS Z87200 Spread-Spectrum Transceiver
CMOS Z80182 Modem Controller
45.056 MHz Crystal (Z87200)

16.384 MHz Crystal (Z80182)
Comprehensive Test Points
128 KB RAM
64 KB ROM
Reset and NMI Buttons

Documentation

Z87200 Preliminary Product Specification
Z87200 Technical Manual
Z80182 Product Specification
Z80180 Technical Manual
ESCC Technical Manual
Evaluation Board User's Manual
Including Schematics

Z16C30

CMOS USC™ UNIVERSAL SERIAL CONTROLLER

GENERAL DESCRIPTION

The USC Universal Serial Controller is a dual-channel multi-protocol data communications peripheral designed for use with any conventional multiplexed or non-multiplexed bus. The USC functions as a serial-to-parallel, parallel-to-serial converter/controller and may be software configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including two baud rate generators per channel, a digital phase-locked loop per channel, character counters for both receive and transmit in each channel and 32-byte data FIFO's for each receiver and transmitter.

Zilog now offers a single version of the USC, Z16C3010VSC. Bus bandwidth is fast enough to allow CPU accesses of 110 ns. The USC handles transmit and receive clocks to 10 MHz and data transfer rates up to 10 MBits/sec. When using the DPLL, Baud Rate Generator (BRG), and Counter Timer Register (CTR) the clock can run as fast as 20 MHz.

The USC handles asynchronous formats, synchronous byte-oriented formats such as BISYNC and synchronous bit-oriented formats such as HDLC. This device supports virtually any serial data transfer application.

The device can generate and check CRC in any synchronous mode and can be programmed to check data integrity in various modes. The USC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O. The same is true for most of the other pins in each channel.

Interrupts are supported with a daisy-chain hierarchy, with the two channels having completely separate interrupt structures.

High-speed data transfers via DMA are supported by a Request/Acknowledge signal pair for each receiver and transmitter. The device supports automatic status transfer via DMA and also allows device initialization under DMA control.

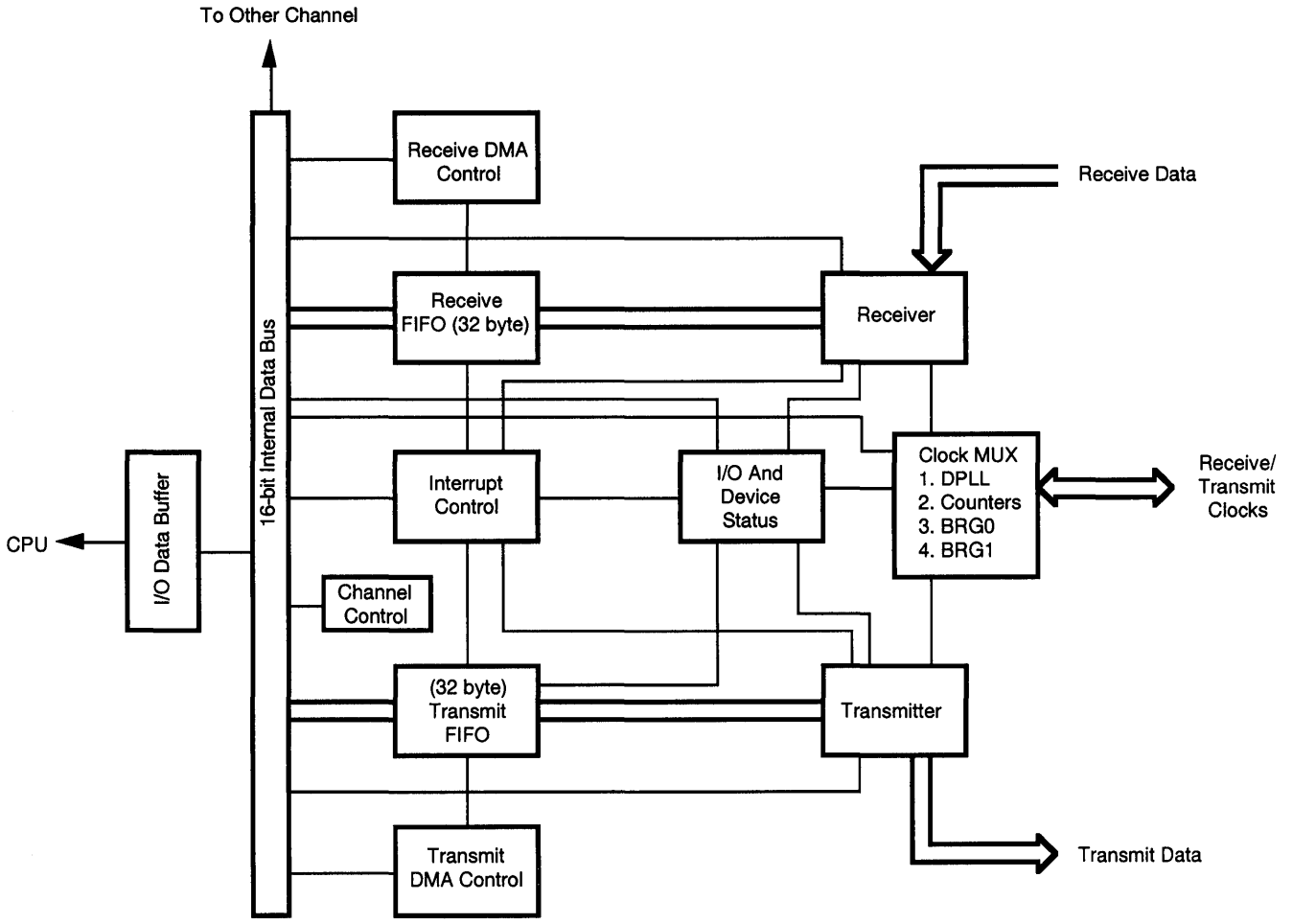
To aid the designer in efficiently programming the USC, support tools are available. The Technical Manual describes in detail all features presented in this Product Specification and gives programming sequence hints. The Programmer's Assistant is a MS-DOS disk-based programming initialization tool to be used in conjunction with the Technical Manual. There are also available assorted application notes and development boards to assist the designer in the hardware/software development.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



USC Block Diagram

Z16C32

IUSC™ INTEGRATED UNIVERSAL SERIAL CONTROLLER

GENERAL DESCRIPTION

The IUSC (Integrated Universal Serial Controller) is a single-channel multple protocol data communications device with on-chip dual-channel DMA. The integration of a high speed serial communications channel with a high performance DMA facilitates higher data throughput than is possible with discrete serial/DMA chip combinations. The buffer chaining capabilities combined with features like character counters, frame status block and buffer termination at the end of the frame facilitate sophisticated buffer management that can significantly reduce CPU overhead.

The IUSC is software configurable to satisfy a wide variety of serial communications applications. Offered at 20 Mbit/sec, its fast data transfer rate and multiple protocol support make it ideal for applications in todays dynamic environment of changing specifications and ever increasing speed. The many programmable features allow the user to tune the device response to meet system requirements and adapt to future changes with software instead of redesigning hardware.

The on-chip DMA channels allow high-speed data transfers for both the receiver and the transmitter. The device supports automatic status transfer via DMA and allows device initialization under DMA control. Each DMA channel can transfer data words in as little as three 50 ns clock cycles and can generate addresses compatible with 32-, 24- or 16-bit memory ranges. The DMA channels may operate in any of four modes: single buffer, pipelined, array-chained, or linked-list. The array-chained and linked-list modes reduce the problems with segmentation and reassembly of messages in systems. To prevent the DMA from holding bus mastership too long, mastership time may be limited by counting the absolute number of clock cycles, the number of bus transactions, or both.

The CPU bus interface is designed for use with any conventional multiplexed or non-multiplexed bus. The device contains a variety of sophisticated internal functions including two baud rate generators, a digital phase-locked loop, character counters, and 32-byte FIFOs for both the receiver and transmitter.

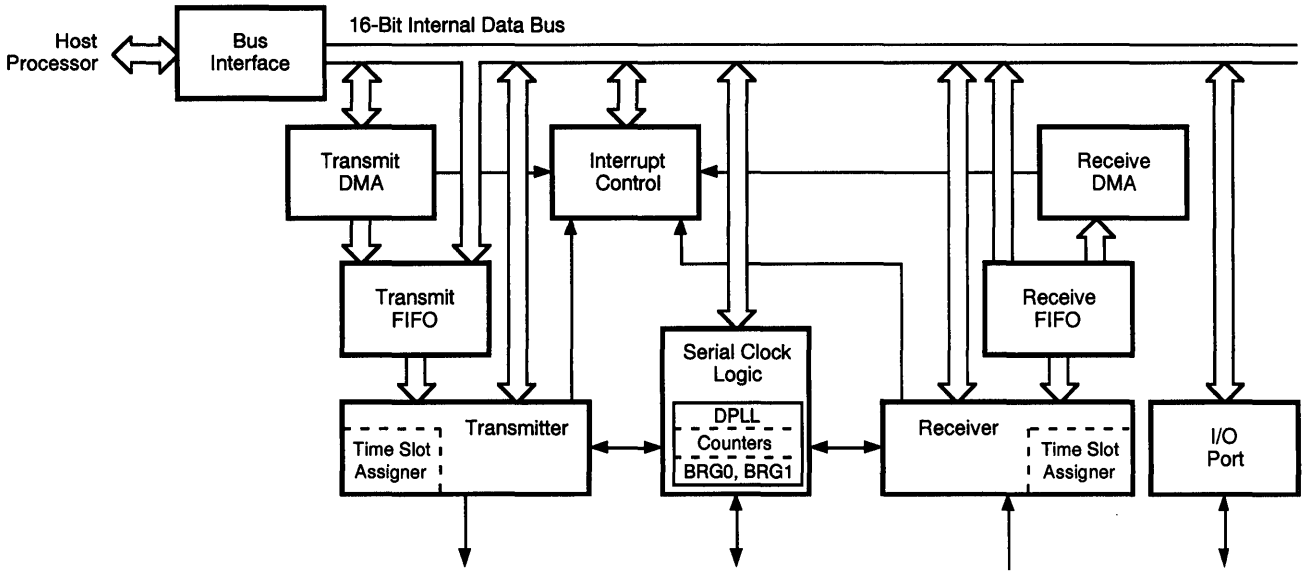
The IUSC handles asynchronous formats, synchronous byte-oriented formats (e.g., BISYNC), and synchronous bit-oriented formats such as HDLC. This device supports virtually any serial data transfer application.

The IUSC can generate, and check CRC in any synchronous mode and is programmed to check data integrity in various modes. Access to the CRC value allows system software to resend or manipulate it as needed in various applications. The IUSC also has facilities for modem controls. In applications where these controls are not needed, the modem controls can be used for general purpose I/O.

Interrupts are supported by a daisy-chain hierarchy within the serial channel and between the serial channel and the DMA.

Support tools are available to aid the designer in efficiently programming the IUSC. The Technical Manual describes in detail all features presented in this Product Specification and gives programming sequence hints. The EPM™ manual (Electronic Programmers Manual) is an MS-DOS, disk-based programming initialization tool, used in conjunction with the Technical Manual. Also, there are assorted application notes and development boards to assist the designer in hardware/software development.

GENERAL DESCRIPTION (Continued)



IUSC Block Diagram

ZILOG

SUPPORT PRODUCT

Z16C3001ZCO

EVALUATION KIT

DESCRIPTION

The kit contains an assembled PC/XT/AT circuit board with two high-speed serial connections, DB9 and DB25 connectors selectively driven by RS-232 or RS-422 line drivers. The kit also contains software and documentation to support software and hardware development for Zilog's USC and MUSC™ devices.

The board illustrates the use of Zilog's USC and MUSC devices in a variety of communication applications such as high speed ASYNC and SDLC/HDLC.

SUPPORTED DEVICES

Z16C30, Z16C33

SPECIFICATIONS

Power Requirements

+5 Vdc @ .5 A

Dimensions

Width: 4.5 in. (11.43 cm)
Length: 6.5 in. (16.51 cm)

Serial Interface

DB9 and DB25 connectors selectively driven by RS-232C or RS-422 at selectable baud rates.

KIT CONTENTS

Z16C30/Z16C33 Evaluation Board

CMOS Z16C30 USC and Z16C33 MUSC
RS-232C and RS-422 line drivers
DB9 and DB25 Interfaces

Software (IBM™ PC Platform)

Source and executable codes to run the USC or MUSC in SDLC/HDLC or ASYNC mode. All codes are written and compiled using Microsoft Quick C 2.5.

Documentation

Z16C30 and Z16C33 Product Specifications
Z16C30/Z16C33 Technical Manual
Z16C3001ZCO Kit User Guide

*IBM is a registered trademark of International Business Machines Corp.
*Microsoft is a registered trademark of Microsoft Corp.

SUPPORT PRODUCT

Z16C3200ZC0

ZNW2000 PC WAN ADAPTER BOARD DEVELOPER'S KIT

DESCRIPTION

The ZNW2000 WAN Developer's Kit comprises an add-in board for AT/ISA systems that allow Wide Area Network (WAN) communication speeds up to and above T1/E1 (1.544/2.048 Mbps) rates.

The kit contains software, hardware, and documentation to aid in developing a wide variety of IUSC™-based serial communications applications, including WAN access for PC-based LAN server/routers.

SUPPORTED DEVICES

Z16C32 IUSC

SPECIFICATIONS

Power Requirements

+5 Vdc @ 500 mA

Dimensions

Width: 6.7 in.
Length: 4.8 in.

Serial Interface

The two connectors on the board end-panel, and the near end of their mating cables are 26-pin, D-subminiatures with 25 mil contact pitch. There is a different mating cable for each of the interfaces. The two serial ports may use different cables/interfaces.

Cables (Included):

Type	Ordering Information
Inter-Channel Loopback	Z93C0042Z01

Optional (Ordered Separately):

Type	Ordering Information
V.35	Z93C0043Z01
RS232	Z93C0044Z01
RS449 (RS422 & RS423)	Z93C0045Z01
X.21	Z93C0046Z01

KIT CONTENTS

ZNW2000 PC WAN Adapter Board

Two Z16C32 IUSCs
256 Kbytes of RAM
High-Speed Bus Interface
V.35, RS232, RS449/422, RS449/423 and X.21 Serial Interfaces

Disks Containing

Test Software - Source and Object Code
PAL Equations

Documentation

ZNW2000 User's Manual
- Board Hardware Description
- Board Test Software Description
- PAL Equations
- Timing Characteristics
- Bill of Materials
- Schematics

IUSC User's Manual
High-Serial Communications Controllers Product Specification Databook

Z16C35

CMOS ISCC™ INTEGRATED SERIAL COMMUNICATIONS CONTROLLER

GENERAL DESCRIPTION

The Z16C35 ISCC™ is a CMOS Superintegrated device with a flexible Bus Interface Unit (BIU) connecting a built-in Direct Memory Access (DMA) cell to the CMOS Serial Communications Control (SCC) cell.

The ISCC is a dual-channel, multi-protocol data communications peripheral which easily interfaces to CPUs with either multiplexed or non-multiplexed address and data buses. The advanced CMOS process offers lower power consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allow the ISCC to be configured for a wide variety of serial communications applications. The many on-chip features such as, streamlined bus interface, four channel DMA, baud rate generators, digital phase-locked loops, and crystal oscillators dramatically reduce the need for external logic.

The ISCC can address up to 4 gigabytes per DMA channel by using the /UAS and /AS signals to strobe out 32-bit multiplexed addresses.

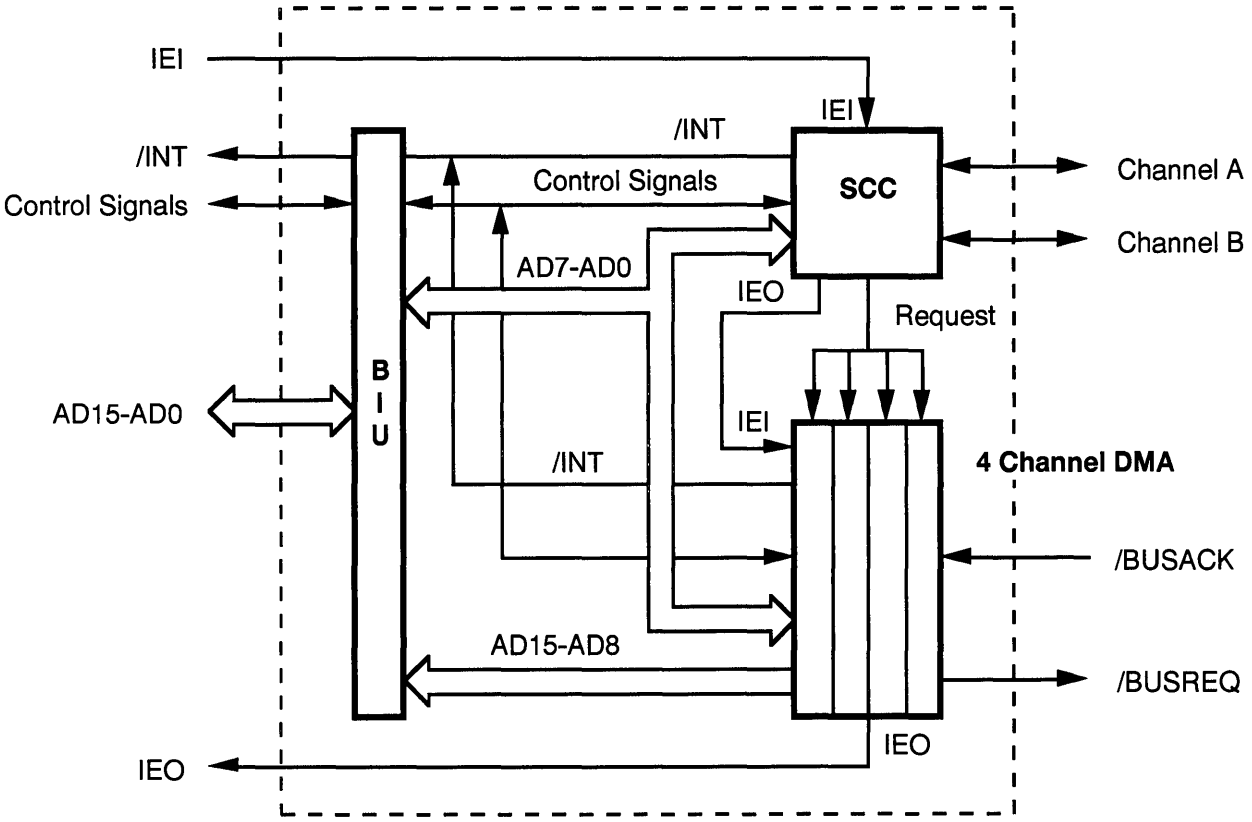
The ISCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC.

FEATURES

- Low Power CMOS Technology
- Two General-Purpose SCC Channels, Four DMA Channels; and Universal Bus Interface Unit.
- Software Compatible to the Zilog CMOS SCC
- Four DMA Channels; Two Transmit and Two Receive Channels to and from the SCC
- Four Gigabyte Address Range per DMA Channel
- Fly-by DMA Transfer Mode
- Programmable DMA Channel Priorities
- Independent DMA Register Set
- A Universal Bus Interface Unit Providing Simple Interface to Most CPUs Multiplexed or Non-Multiplexed Bus; Compatible with 680x0 and 8x86 CPUs.
- 32-Bit Addresses Multiplexed to 16-Pin Address/Data Lines
- 68-Pin PLCC
- Supports all Zilog CMOS SCC Features.
- Two Independent, 0 to 4.0 Mbit/sec, Full-Duplex Channels, each with a Separate Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop Circuit for Clock Recovery.
- Multi-Protocol Operation Under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.
- Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits Per Character; Programmable Clock Factor; Break Detection and Generation; Parity, Overrun, and Framing Error Detection.
- Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT Preset to Either 1's or 0's.

FEATURES (Continued)

- SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRC Generation and Checking, and SDLC Loop Mode Operation.
- Full CMOS SCC Register Set
- 10 and 16 MHz Speeds Suitable for T1 Full Duplex Operation



FunctionalBlock Diagram

Z53C80/C85

SMALL COMPUTER SYSTEM INTERFACE (SCSI)

GENERAL DESCRIPTION

The Z53C80/C85 SCSI (Small Computer System Interface) controller is a 44-pin PLCC, 44-pin QFP or 48-pin DIP CMOS device. It is designed to implement the SCSI protocol as defined by the ANSI X3.131-1986 standard, and is fully compatible with the industry standard 5380. It is capable of operating both as a Target and as an Initiator. Special high-current open-drain outputs enable it to directly interface to the SCSI bus. The Z53C80/C85 has the necessary interface hook-ups so the system CPU can communicate with it like with any other peripheral device. The CPU can read from, or write to, the SCSI registers which are addressed as standard or memory-mapped I/Os.

Differing only on pinouts and package offering, the Z53C80 and Z53C85 are identical. The Z53C85 is only available in the 44-pin QFP package. The pin signals are offset by one pin to make the pinout NCR compatible.

The Z53C80/C85 increases the system performance by minimizing the CPU intervention in DMA operations which the SCSI controls. The CPU is interrupted by the SCSI when it detects a bus condition that requires attention. It also supports arbitration and reselection.
The Z53C80/C85 has the proper hand-shake signals to support normal and block mode DMA operations with most DMA controllers available.

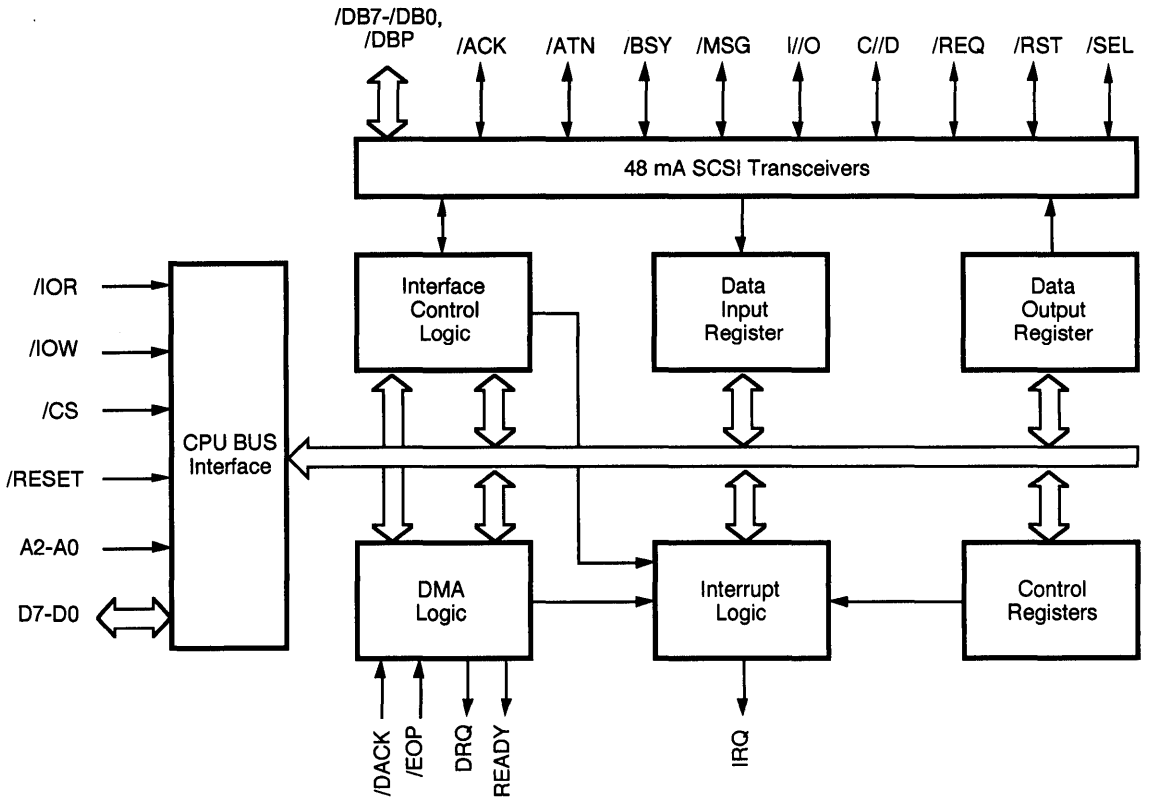
The following pages show a sample of the AC Timing Diagrams. Please refer to the Product Specification for a complete list.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



SCSI Block Diagram

Z80230

ESCC™ ENHANCED SERIAL COMMUNICATION CONTROLLER

GENERAL DESCRIPTION

The Zilog Enhanced Serial Communications Controller, Z80230 ESCC, is a pin and software compatible CMOS member of the SCC family introduced by Zilog in 1981. The ESCC is a dual-channel, full-duplex data communications controller capable of supporting a wide range of popular protocols. The ESCC is built from Zilog's industry standard SCC core and is compatible with designs using Zilog's SCC to receive and transmit data. It has many improvements that significantly reduce CPU overhead. The addition of a 4-byte transmit FIFO and an 8-byte receive FIFO significantly reduces the overhead required to provide data to, and get data from, the transmitters and receivers.

The ESCC also has many features that improve packet handling in SDLC mode. The ESCC will automatically: transmit a flag before the data, reset the Tx Underrun/EOM latch, force the TxD pin high at the appropriate time when using NRZI encoding, deassert the /RTS pin after the closing flag, and better handle ABORTed frames when using the 10x19 status FIFO. The combination of these features along with the deeper data FIFOs significantly simplifies SDLC driver software.

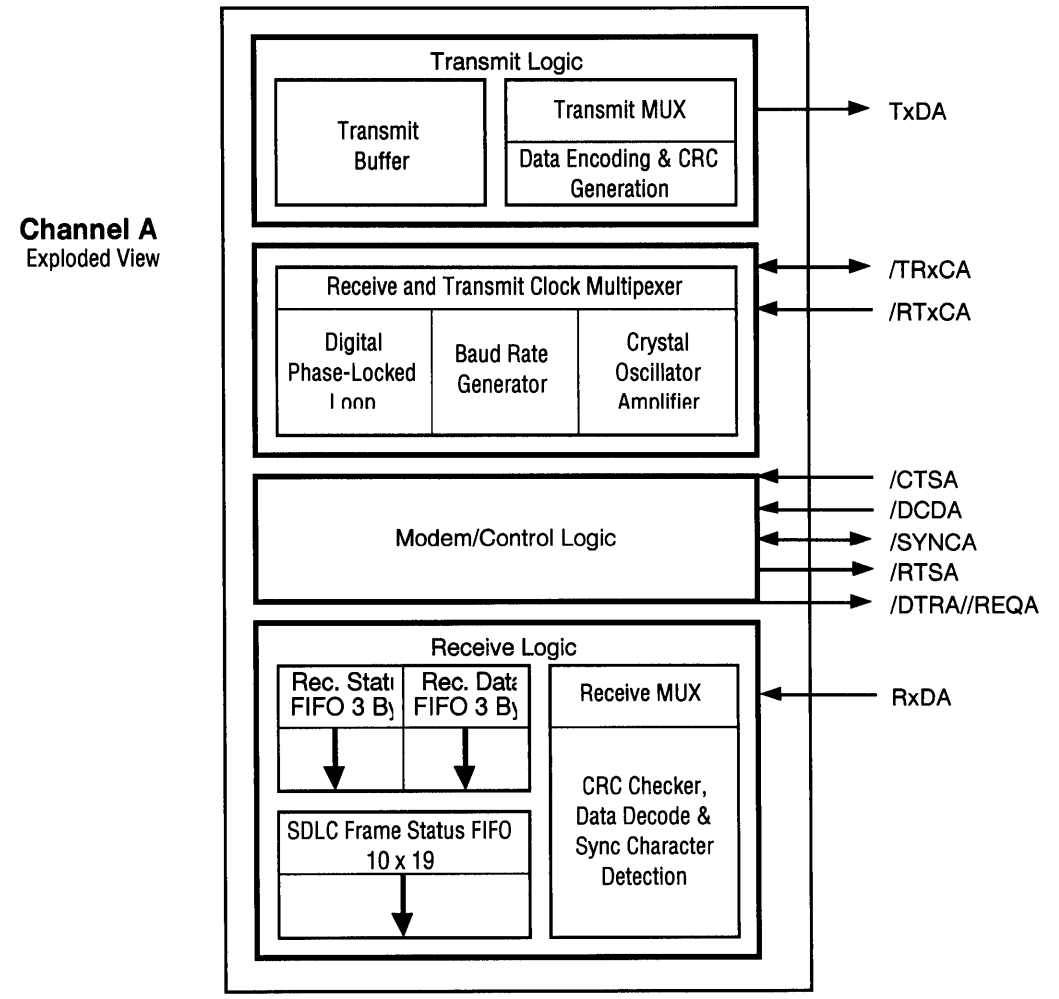
The CPU hardware interface has been simplified by relieving the databus setup time requirement and supporting the software generation of the interrupt acknowledge signal (INTACK). These changes allow an interface with less external logic to many microprocessor families while maintaining compatibility with existing designs. I/O handling of the ESCC is improved over the SCC with faster response of the /INT and /DTR//REQ pins.

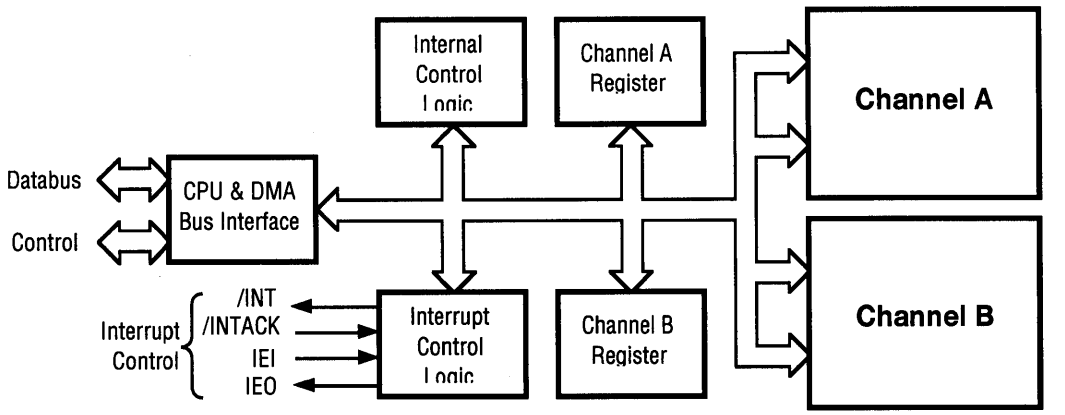
The many enhancements added to the ESCC permits a system design that increases overall system performance with better data handling and less interface logic.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}





Functional Block Diagram

Z8030/Z8530

Z-BUS® SCC/SCC SERIAL COMMUNICATIONS CONTROLLER

GENERAL DESCRIPTION

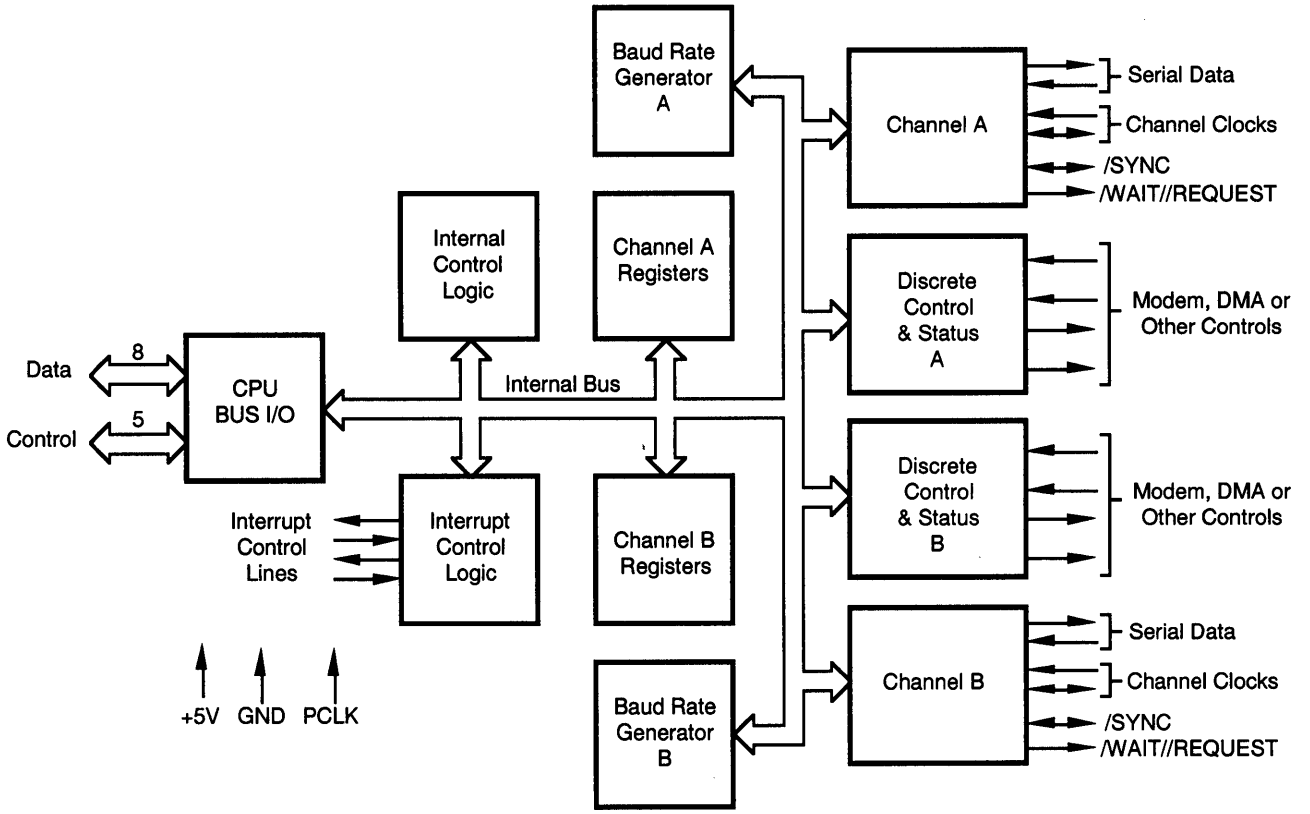
The SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with conventional non-multiplexed buses and the Zilog Z-Bus®. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators that dramatically reduce the need for external logic.

10

FEATURES

- Two Independent, 0 to 2M Bit/Second, Full Duplex Channels, each with a Separate Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop for Clock Recovery.
- Multi-Protocol Operation under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.
- Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits per Character; Programmable Clock Factor; Break Detection and Generation; Parity, Overrun, and Framing Error Detection.
- Supports T1 Digital Trunk.
- Clock Speeds: 4, 6 and 8 MHz.
- Local Loopback and Auto Echo Modes.
- Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT Preset to Either 1s or 0s.
- SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRC Generation and Checking, and SDLC Loop Mode Operation.
- Available in 40-Pin DIP and 44-Pin PLCC Package Types.

FEATURES (Continued)



Functional Block Diagram

Z80C30

CMOS Z-BUS® SCC
SERIAL COMMUNICATION CONTROLLER

GENERAL DESCRIPTION

The Zilog Serial Communications Controller, Z80C30 SCC, is a pin and software compatible CMOS member of the SCC family introduced by Zilog in 1981. It is a dual channel, multi-protocol data communications peripheral that easily interfaces to CPU's with multiplexed address/data buses. The advanced CMOS process offers lower power consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allows the SCC to be configured to satisfy a wide variety of serial communications applications. The many on-chip features such as baud rate generators, digital phase locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features including a 10x19-bit status FIFO and 14-bit byte counter were added to support high speed SDLC transfers using DMA controllers.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.) The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

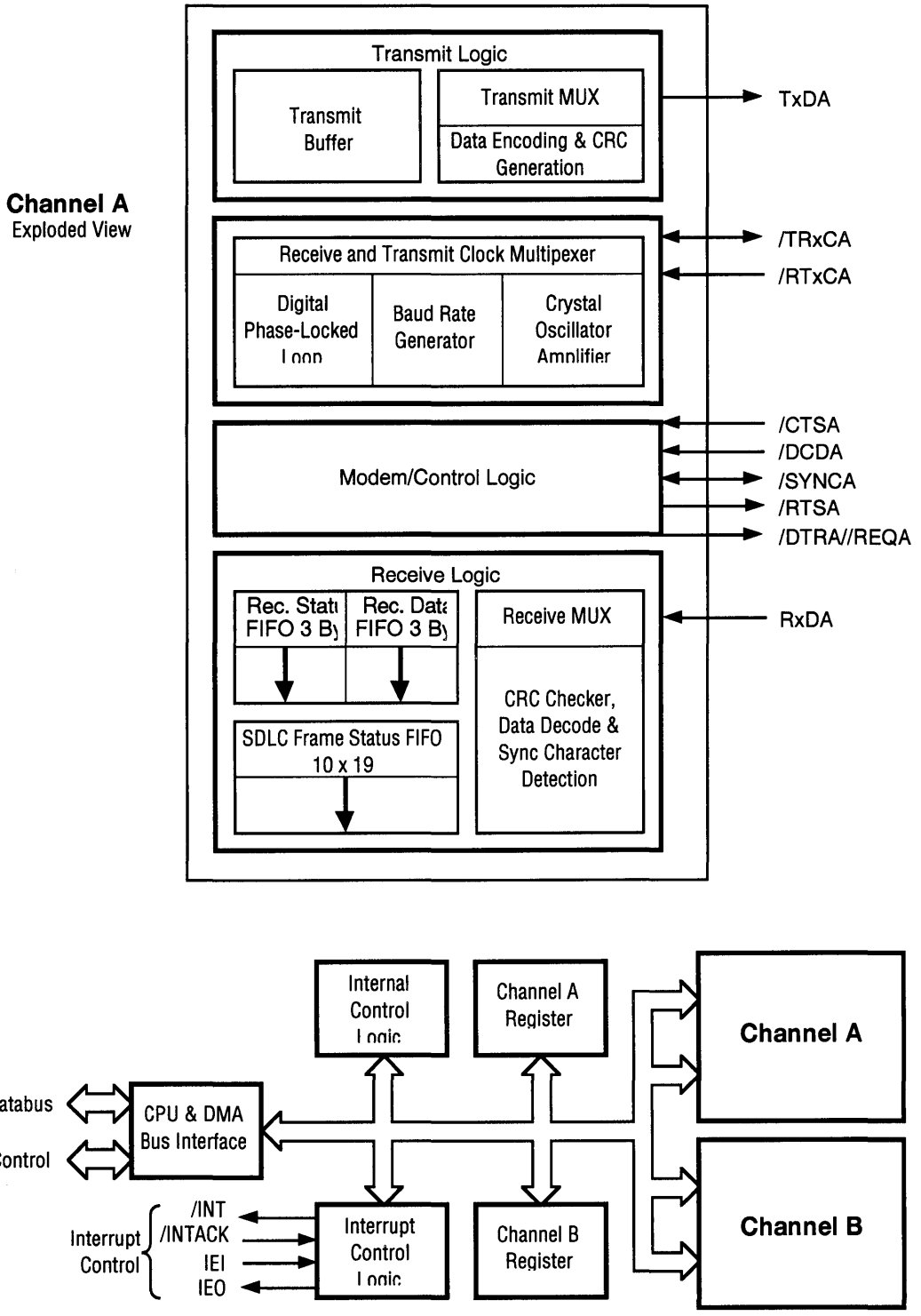
The daisy-chain interrupt hierarchy is also supported as is standard for Zilog peripheral components.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



SCC Block Diagram

Z84013/Z84015

Z80 CMOS IPC INTELLIGENT PERIPHERAL CONTROLLER

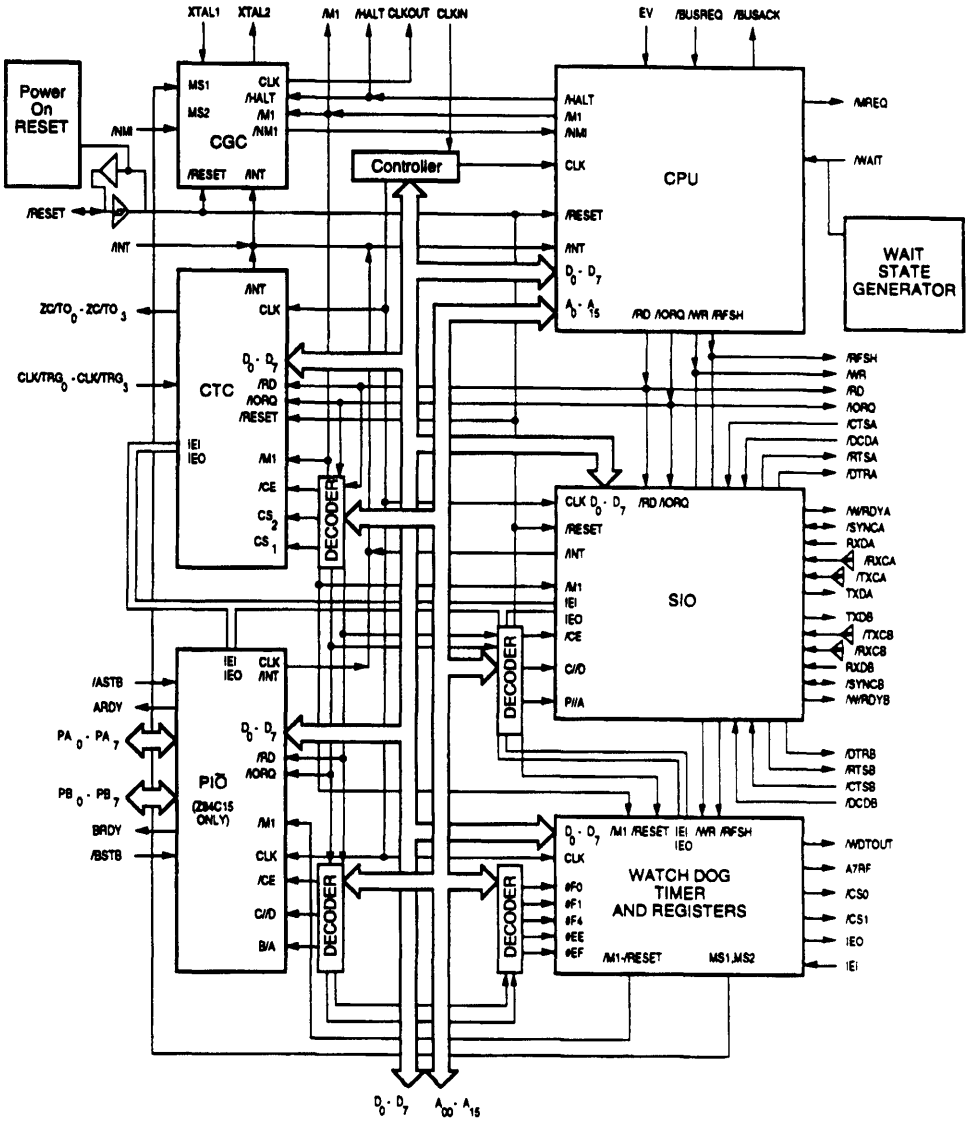
GENERAL DESCRIPTION

The Intelligent Peripheral Controller (IPC) is a series of highly superintegrated devices. The Z84015 is a CMOS 8-bit microprocessor integrated with the CTC, SIO, CGC, WDT and the PIO into a single 100-pin Quad Flat Pack (QFP) package. The Z84013 is the Z84015 without PIO, and is housed in a 84-pin PLCC package. These high-end superintegrated intelligent peripheral controllers are targeted for a broad range of applications ranging from error correcting modems to enhancement/cost reductions of existing hardware using Z80-based discrete peripherals.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}



Functional Block Diagram

Z85233

EMSCC™ ENHANCED MONO SERIAL COMMUNICATION CONTROLLER

GENERAL DESCRIPTION

The Zilog Enhanced Mono Serial Communication Controller, Z85233 EMSCC, is a software compatible CMOS member of the SCC family introduced by Zilog in 1981. The EMSCC is a full-duplex data communications controller capable of supporting a wide range of popular protocols. The Z85233 EMSCC is a single channel version (Channel A) of Zilog's Z85230 ESCC. Based on Zilog's unique Superintegration™ Technology, the EMSCC is compatible with designs using Zilog's SCC and ESCC to receive and transmit data. It has many improvements that significantly reduce CPU overhead. The addition of a 4-byte transmit FIFO and an 8-byte receive FIFO significantly reduces the overhead required to provide data to, and get data from, the transmitter and receiver.

The EMSCC also has many features that improve packet handling in SDLC mode. The EMSCC will automatically: transmit a flag before the data, reset the Tx Underrun/EOM latch, force the TxD pin high at the appropriate time when using NRZI encoding, deassert the /RTS pin after the closing flag, and better handle ABORTed frames when using the 10x19 status FIFO. The combination of these features along with the deeper data FIFOs significantly simplifies SDLC driver software.

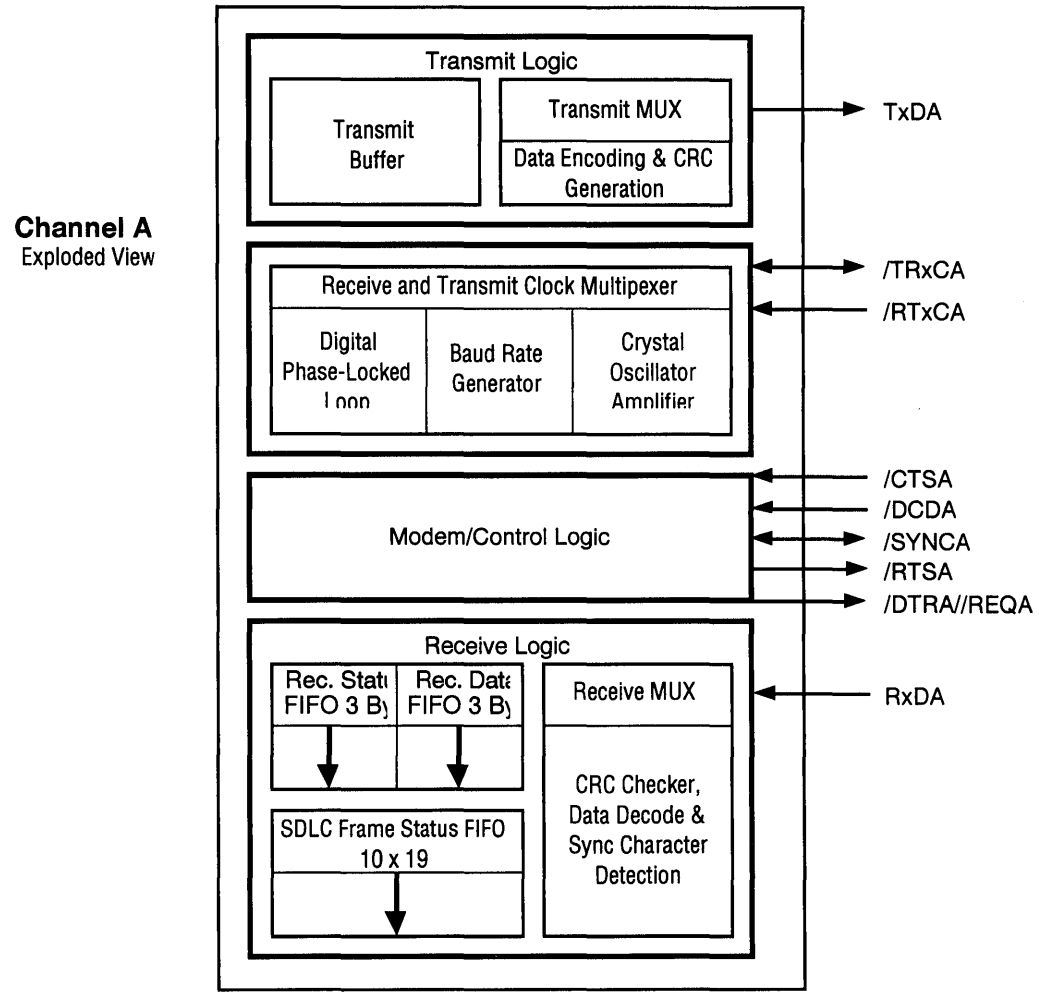
The CPU hardware interface has been simplified by relieving the databus setup time requirement and supporting the software generation of the interrupt acknowledge signal (/INTACK). These changes allow an interface with less external logic to many microprocessor families while maintaining compatibility with existing designs. I/O handling of the EMSCC is improved over the SCC with faster response of the /INT and /DTR//REQ pins.

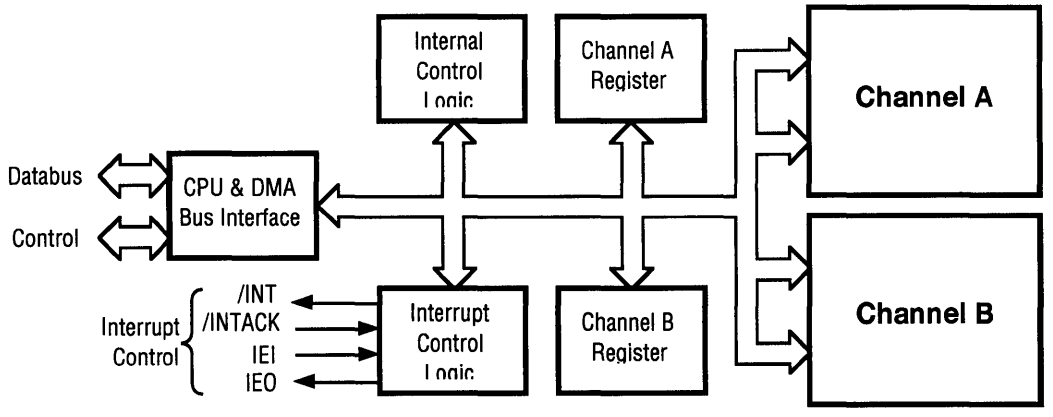
The many enhancements added to the EMSCC permits a system design that increases overall system performance with better data handling and less interface logic.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}





Functional Block Diagram

Z85C30

CMOS SCC SERIAL COMMUNICATION CONTROLLER

GENERAL DESCRIPTION

The Zilog Serial Communications Controller, Z85C30 SCC, is a pin and software compatible CMOS member of the SCC family introduced by Zilog in 1981. It is a dual channel, multi-protocol data communications peripheral that easily interfaces to CPU's non-multiplexed address/data buses. The advanced CMOS process offers lower power consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allows the SCC to be configured to satisfy a wide variety of serial communications applications. The many on-chip features such as baud rate generators, digital phase locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features including a 10x19-bit status FIFO and 14-bit byte counter were added to support high speed SDLC transfers using DMA controllers.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The daisy-chain interrupt hierarchy is also supported as is standard for Zilog peripheral components.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

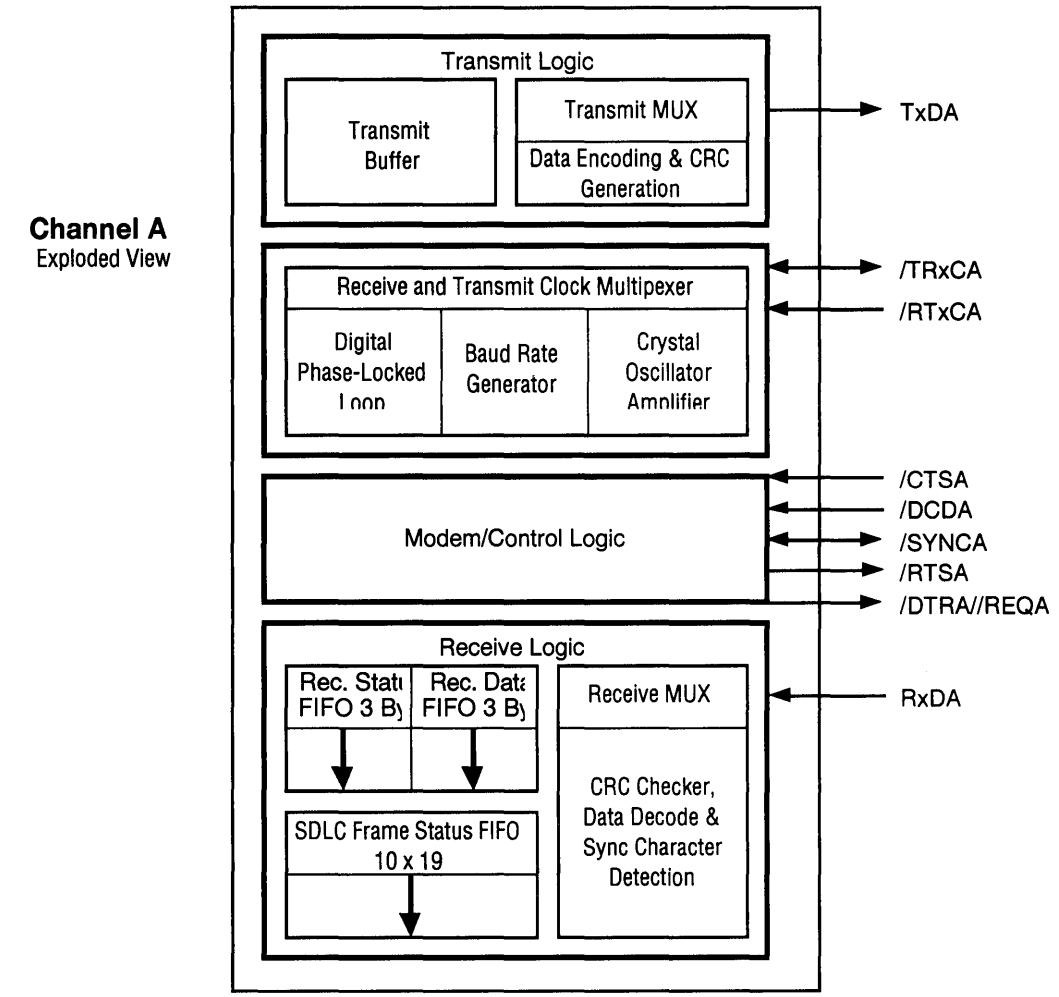
Power connections follow conventional descriptions below:

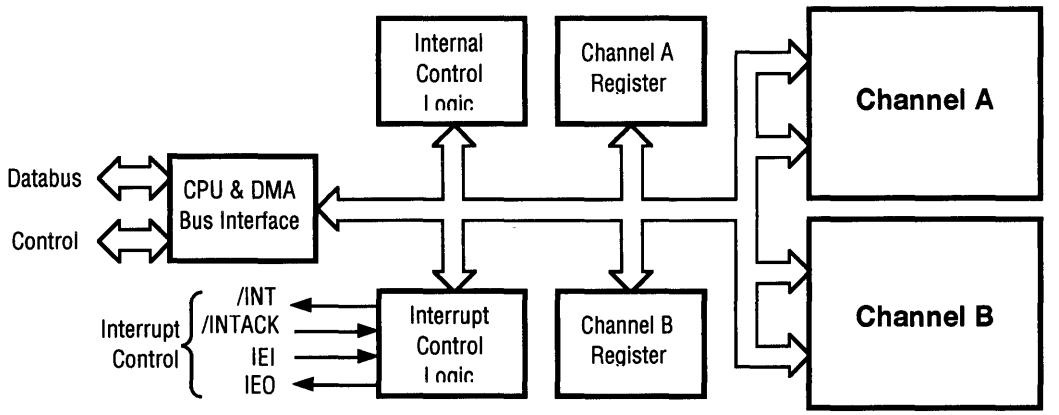
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

The description on Z85C30 is applicable to the following parts:

Z85C3008PSC
Z85C3010PSC
Z85C3016PSC
Z85C3008VSC
Z85C3010VSC
Z85C3016VSC

GENERAL DESCRIPTION (Continued)





SCC Block Diagram

Z85C80

SCSCI SERIAL COMMUNICATIONS AND SMALL COMPUTER INTERFACE

GENERAL DESCRIPTION

The Z85C80 CMOS SCSCI is an industry standard 85C30 dual channel Serial Communication Controller (SCC) and an industry standard 53C80 Small Computer System Interface (SCSI) integrated into one monolithic Integrated Circuit. The internal SCC and SCSI share the 8-bit data bus (D7 through D0) and read and write inputs (/RD and /WR).

The Z85C80 is offered in a 68-pin PLCC package in both 10 MHz and 16 MHz speed grades for the SCC interface, and in 100-pin VQFP in the 16 MHz speed grade. The SCSI interface data transfer rate is 3.0 MBytes/sec. With a few exceptions, all of the internal SCC and SCSI signals are connected to the outside pins.

The exceptions are:

- IEI input to SCC is internally connected to VDD.
- IEO output from SCC is not internally connected (N/C).
- READY output from SCSI is not internally connected (N/C).
- /SYNCB output from the SCC is not internally connected (N/C).
- /TRXCA and /CTSA inputs to the SCC are internally connected.
- /TRXCB and /CTSB inputs to the SCC are internally connected.

The internal SCC is a dual channel, multi-protocol data communications peripheral that easily interfaces to CPUs with non-multiplexed address/data buses. The programming flexibility of the internal registers allows the SCC to be configured to satisfy a wide variety of serial communications applications. The many on-chip features such as baud rate generators, digital phase locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features, including a 10x19-bit status FIFO and 14-bit byte counter, were added to support high speed SDLC transfers using DMA controllers.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. The internal SCC can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. It also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls are used for general-purpose I/O. The daisy-chain interrupt hierarchy is also supported and is standard for Zilog peripheral components.

The internal SCSI is designed to implement the SCSI protocol as defined by the ANSI X3.131-1986 standard, and is fully compatible with the industry standard 53C80. It is capable of operating both as a target and as an initiator. Special high current open-drain outputs enable it to directly interface to, and drive, the SCSI bus. The internal SCSI has the necessary interface hook-ups so the system CPU can communicate with it like with any other peripheral device. The CPU can read from, or write to, the SCSI registers which are addressed as standard or memory-mapped I/Os.

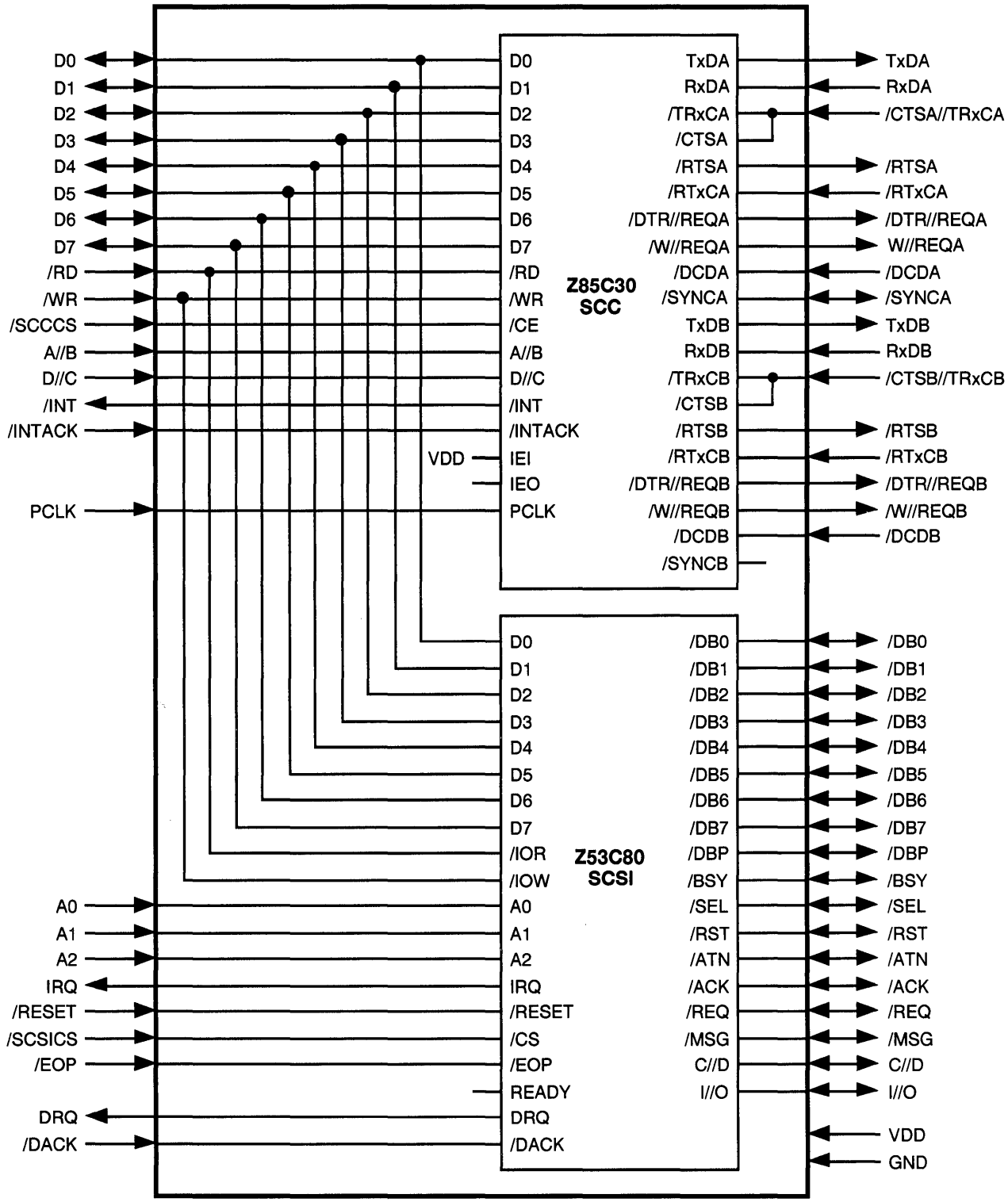
The Internal SCSI increases the system performance by minimizing the CPU intervention in DMA operations which the SCSI controls. The CPU is interrupted by the SCSI when it detects a bus condition that requires attention. It also supports arbitration and reselection. The internal SCSI has the proper hand-shake signals to support normal DMA operations with most DMA controllers available.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Z85C80 SCSCI Block Diagram

Note: [1]: Pins /CTSB and /TRxCB are bonded out separately in the 100-pin VQFP package and should be externally tied together by the user to meet the pinout specification.

SUPPORT PRODUCT

Z8523000ZCO

ESCC PC XT/AT APPLICATIONS BOARD

DESCRIPTION

The kit contains an assembled PC/XT/AT circuit board with one high speed serial port, selectively driven by RS-232C or RS-422 line drivers. The kit also contains software and documentation to support software and hardware development for Zilog's ESCC™ device.

The board illustrates the use of Zilog's ESCC in a variety of communication applications such as SDLC/HDLC, and high speed ASYNC.

SUPPORTED DEVICES

Z85230, Z85233

SPECIFICATIONS

Power Requirements
+5 Vdc @ .5 A

Dimensions
Width: 4 in. (10.16 cm)
Length: 5 in. (12.70 cm)

Serial Interface
A DB25 port selectively driven by RS-232C or RS-422 at selectable baud rates.

KIT CONTENTS

Z85230 Evaluation Board
CMOS Z85230 ESCC
RS-232C and RS-422 line drivers
DB25 connector

Software (IBM-PC Platform)
Source and executable codes to run the ESCC in SDLC/HDLC and ASYNC modes using DMA, Interrupt and polling methods. All codes are written in C and compiled using the Microsoft™ Quick C compiler.

Documentation
Z85230 Product Specifications
Z85230 Technical Manuals
Z85C3000ZCO User's Guide
Sealevel™ User's Manual

Communication Controllers

Z80/Z180 Microprocessors

Z8400/84C00

NMOS/CMOS Z80 CPU CENTRAL PROCESSING UNIT

FEATURES

- The Extensive Instruction Set.Contains 158 Instructions, Including the 8080A Instructions Set as a Subset.
- Single 5 Volt Power Supply
- NMOS Version for Low Cost, High Performance Solutions; CMOS Version for High Performance, Low Power Designs.
- NMOS Z084004 - 4 MHz
  Z0840006 - 6.17 MHz
  Z084008 - 8 MHz
- CMOS Z0840006 - DC to 6.17 MHz
  Z84C0008 - DC to 8 MHz
  Z84C0010 - DC to 10 MHz
  Z84C0020 - DC to 20 MHz
- 6 MHz Version can be Operated at 6.144 MHz Clock Speed
- The Z80 Microprocessors and Associated Family of Peripherals can be Linked by a Vectored Interrupt System. This System can be Daisy-Chained to Allow Implementation of a Priority Interrupt Scheme.
- Duplicate Set of Both General-Purpose and Flag Registers
- Two 16-Bit Index Registers
- Three Modes of Maskable Interrupts:
  - Mode 0 - 8080A Similar
  - Mode 1 - Non-Z80 Environment, Location 38H
  - Mode 2 - Z80 Family Peripherals, Vectored Interrupts
- On-Chip Dynamic Memory Refresh Counter

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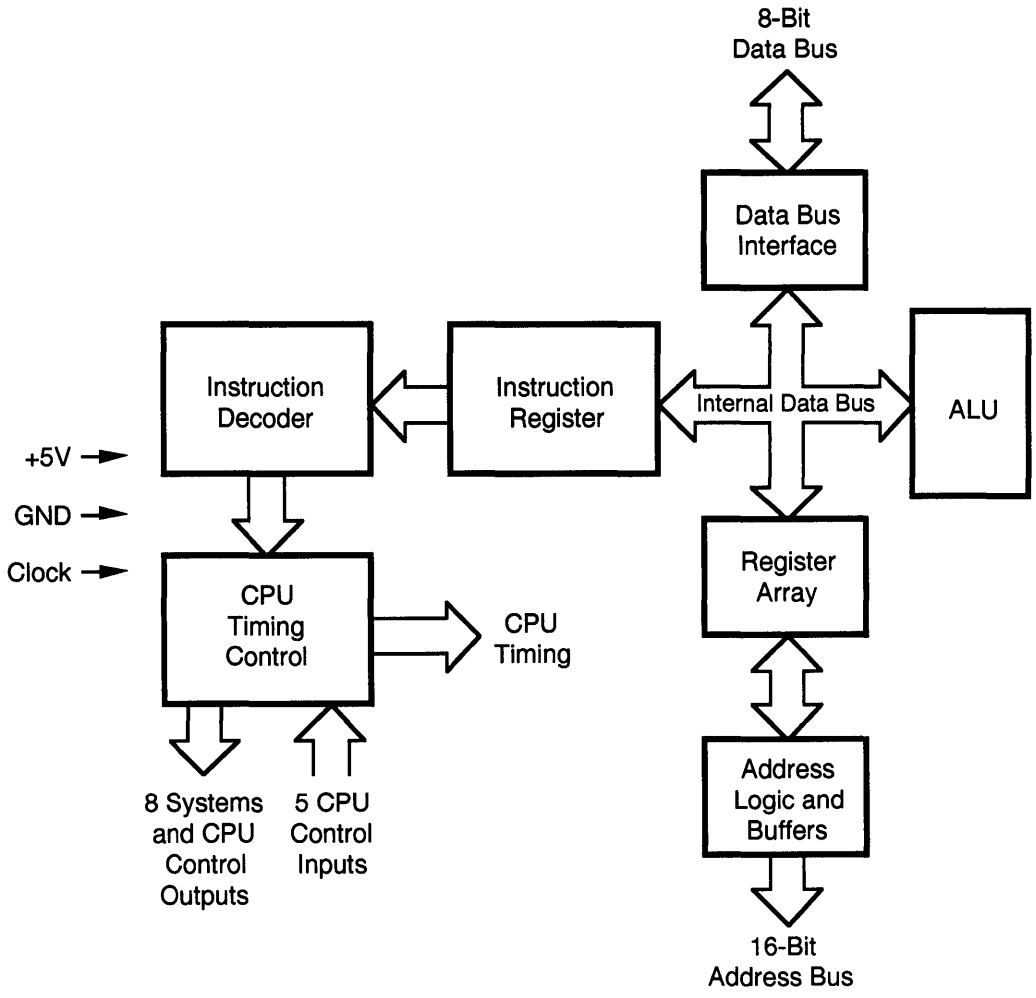
GENERAL DESCRIPTION

The Z8400/Z84C00 CPUs are fourth-generation enhanced microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The speed offerings from 6 - 20 MHz suit a wide range of applications which migrate software. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The CPU also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5V power source. All output signals are fully decoded and timed to control standard memory or peripheral circuits; the CPU is supported by an extensive family of peripheral controllers.

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

Z84C10

CMOS Z80® DMA Direct Memory Access Controlller

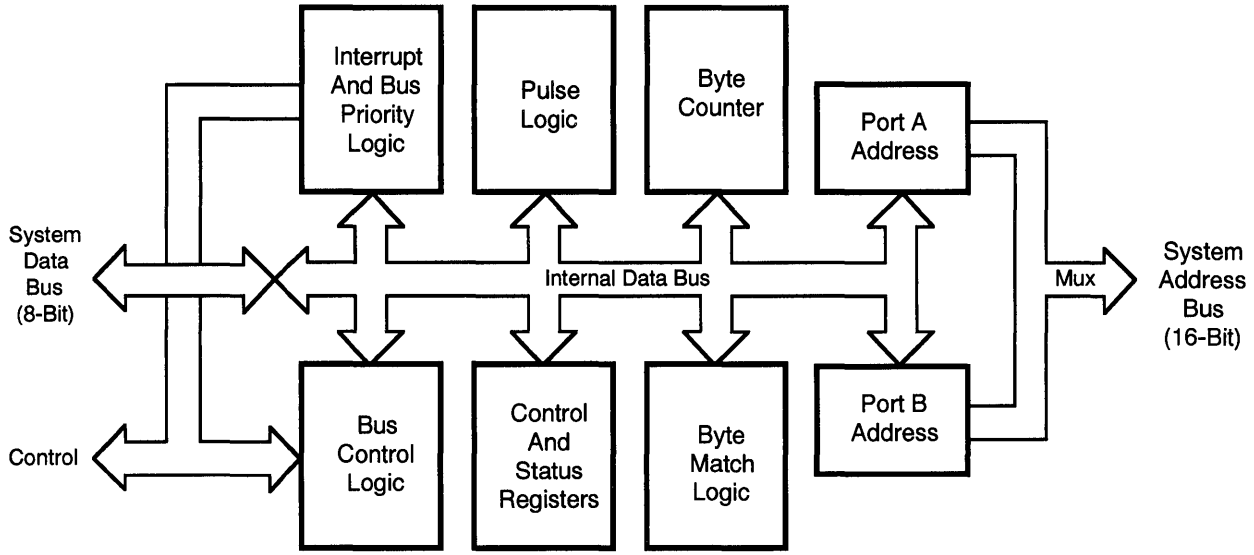
GENERAL DESCRIPTION

The Z80® DMA (Direct Memory Access), hereafter referred to as Z80 DMA or DMA, is a powerful and versatile device for controlling and processing transfers of data. Its basic function of managing CPU-independent transfers between two ports is augmented by an array of features that optimize transfer speed and control with little or no external logic in systems using an 8- or 16-bit data bus and a 16-bit address bus.

Transfers can be done between any two ports (source and destination), including memory-to-I/O, memory-to-memory, and I/O-to-I/O. Dual port addresses are automatically generated for each transaction and may be either fixed or incrementing/decrementing. In addition, bit-maskable byte searches can be performed either concurrently with transfers or as an operation itself.

The Z80 DMA contains direct interfacing to and independent control of, system buses, as well as sophisticated bus and interrupt controls. Many programmable features, including variable cycle timing and auto-restart, minimize CPU software overhead. They are especially useful in adapting this special-purpose transfer processor to a broad variety of memory, I/O and CPU environments.

The Z80 DMA is packaged in a 40-pin plastic or Cerdip DIP, or 44-pin PLCC. It uses a single +5V power supply and the standard Z80 Family single-phase clock.



Z84C10 Functional Block Diagram

Z84C15

IPC/EIPC ENHANCED INTELLIGENT PERIPHERAL CONTROLLER

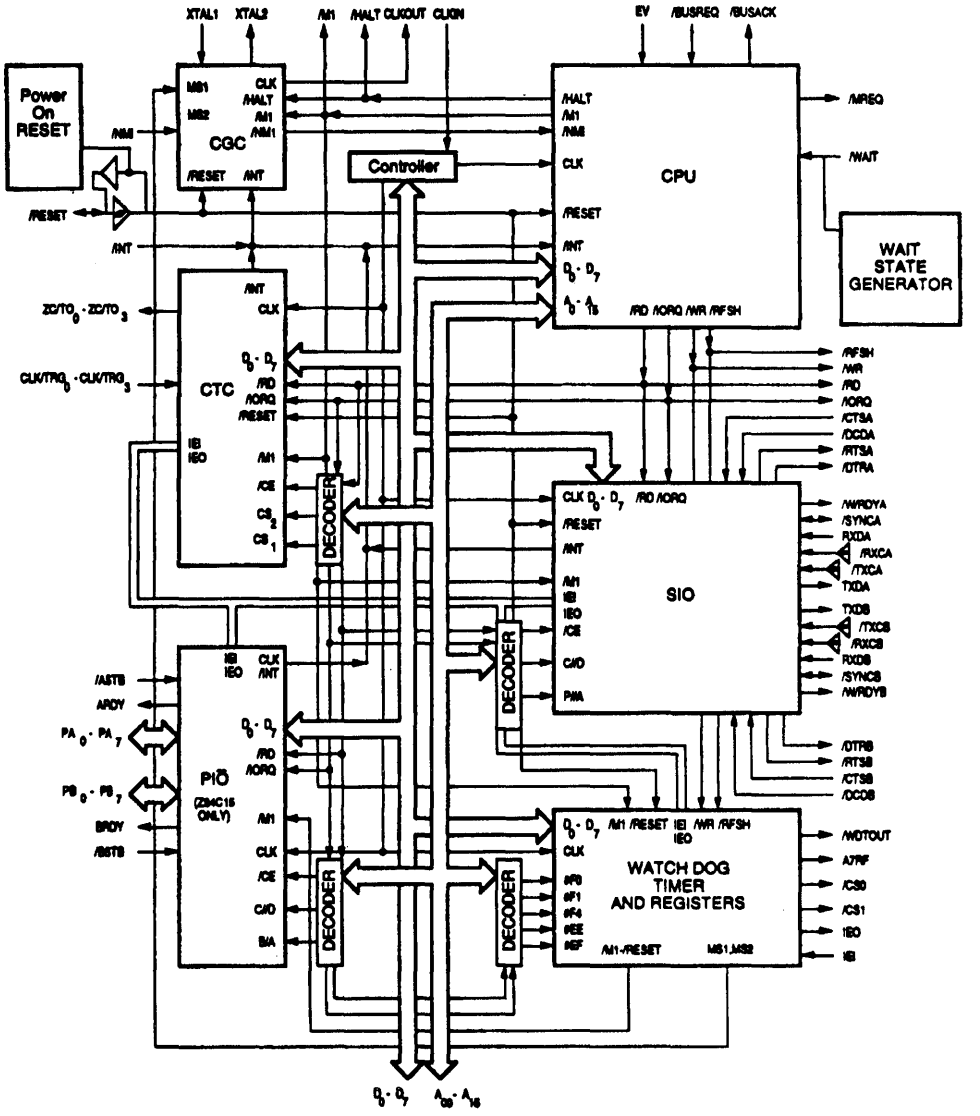
GENERAL DESCRIPTION

The Z84C15 are a series of Intelligent Peripheral Controllers (IPC) targeted for a broad range of applications from error correction modems/faxes, to enhancement/cost reduction of existing Z80 hardware using Z80 based discrete devices. The products are software and hardware compatible with the discrete devices Z84C00, Z84C20, Z84C30 and Z84C40.

The enhanced version, Z84C15, is pin compatible with the Z84015 and both are housed in a 100-pin QFP package. Zilog also offers Z84C15 in a 100-pin VQFP package.

FEATURES

- Z84C15 Enhancements:
  - Power-On Reset
  - Two Additional Chip Select Pins
  - 32-Bit CRC for Channel A of SIO
  - WAIT State Generator
  - Simplified EV Mode
  - Schmitt Trigger I/O, No Tx/Rx Clock
  - Crystal Divide-by-One Mode
- Z84C15 Features the Z84015 and Above Enhancements
- Z84015 Features:
  - Z84C00 - CPU
  - Z84C40 - SIO - Two Serial Channels
  - Z84C30 - CTC - 4x8 bit C/T
  - Z84C20 - PIO
  - Watch-Dog Timer (WDT)
  - Clock Generator Controller (CGC)
- Low Power Consumption
  Three Operating Modes
- 16 MHz Operation for Z84C15 Only.
- Voltage Range 5V ±10%
- 100-Pin VQFP Package for Z84C15



Functional Block Diagram

Z84C90

CMOS Z80 KIO SERIAL/ PARALLEL/COUNTER/TIMER

GENERAL DESCRIPTION

Zilog's Z84C90 Serial/Parallel I/O Counter/Timer (KIO) is a multi-channel, multi-purpose I/O device designed to provide the end-user with a cost effective and powerful solution to meet the designer's peripheral needs. The Z84C90 combines the features of one Z84C30 CTC, one Z84C4xSIO, one Z84C20 PIO, a byte-wide bit programmable I/O and a crystal oscillator in a single 84-pin package.

Utilizing fifteen internal registers for data and programming information, the KIO can easily be configured to any given system environment. Although the optimum performance is obtained with a Z84C00 CPU, the KIO can also be used with any other CPU.

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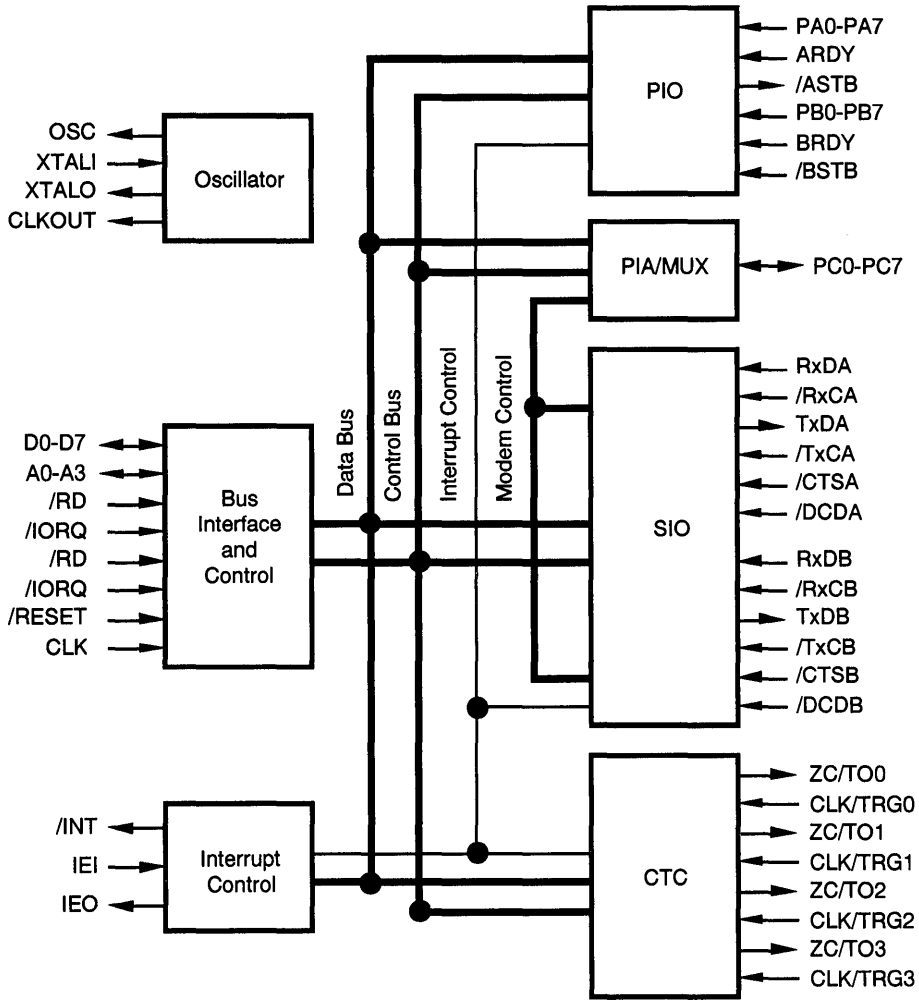
FEATURES

- Two Independent Synchronous/Asynchronous Serial Channels
- Three 8-Bit Parallel Ports
- Four Independent Counter/Timer Channels
- On-Chip Clock Oscillator/Driver
- Software/Hardware Resets
- Designed in CMOS for Low Power Operation
- Supports Z80 Family Interrupt Daisy-Chain
- Programmable Interrupt Priorities
- 8, 10 and 12.5 MHz Bus Clock Frequency
- Single +5V ±10% Power Supply
- Available in 84-Pin PLCC and 80-Pin QFP Packages

FEATURES (Continued)



Functional Block Diagram

Communication Controllers

Z80180

ENHANCED Z180™ MICROPROCESSOR

FEATURES

- Code Compatible with Zilog Z80® CPU
- Extended Instructions
- Two Chain-Linked DMA Channels
- Low Power-Down Modes
- On-Chip Interrupt Controllers
- Three On-Chip Wait-State Generators
- On-Chip Oscillator/Generator
- Expanded MMU Addressing (up to 1 MB)
- Clocked Serial I/O Port
- Two 16-Bit Counter/Timers
- Two Enhanced UARTs (up to 512 Kbps)
- Clock Speeds: 6, 8, 10, 20, 33 MHz
- Operating Range: 5V (3.3V@ 20MHz)
- Operating Temperature Range: 0^0C to +70^0C
- Three Packaging Styles
  - 68-Pin PLCC
  - 64-Pin DIP
  - 80-Pin QFP

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GENERAL DESCRIPTION

The enhanced Z80180 significantly improves on the previous Z80180 models while still providing full backward compatibility with existing Zilog Z80 devices. The Z80180 now offers faster execution speeds, power saving modes, and EMI noise reduction.

This enhanced Z180 design also incorporates additional feature enhancements to the ASCIs, DMAs, and I_{CC} STANDBY Mode power consumption. With the addition of "ESCC-like" Baud Rate Generators (BRGs), the two ASCIs now have the flexibility and capability to transfer data asynchronously at rates of up to 512 Kbps. In addition, the ASCI receiver has added a 4-byte First In First Out (FIFO) which can be used to buffer incoming data to reduce the incidence of overrun errors. The DMAs have been modified to allow for a "chain-linking" of the two DMA channels when set to take their DMA requests from the same peripherals device. This feature allows for non-stop DMA operation between the two DMA channels, reducing the amount of CPU intervention (Figure1).

Not only does the Z80180 consume less power during normal operations than the previous model, it has also been designed with three modes intended to further reduce the power consumption. Zilog reduced I_{cc} power consumption during STANDBY Mode to a minimum of 10 µA by stopping the external oscillators and internal clock. The SLEEP mode reduces power by placing the CPU into a "stopped" state, thereby consuming less current while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a "stopped" mode, thereby reducing power consumption even further.

A new clock doubler feature has been implemented in the Z80180 device that allows the programmer to double the internal clock from that of the external clock. This provides a systems cost savings by allowing the use of lower cost, lower frequency crystals instead of the higher cost, and higher speed oscillators.

GENERAL DESCRIPTION (Continued)

Notes:

All Signals with a preceding front slash, "/" are active Low, for example, B//W (WORD is active Low); /B/W (BYTE is active Low, only). Alternatively, an overslash may be used to signify active Low, for example $\overline{WR}$

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

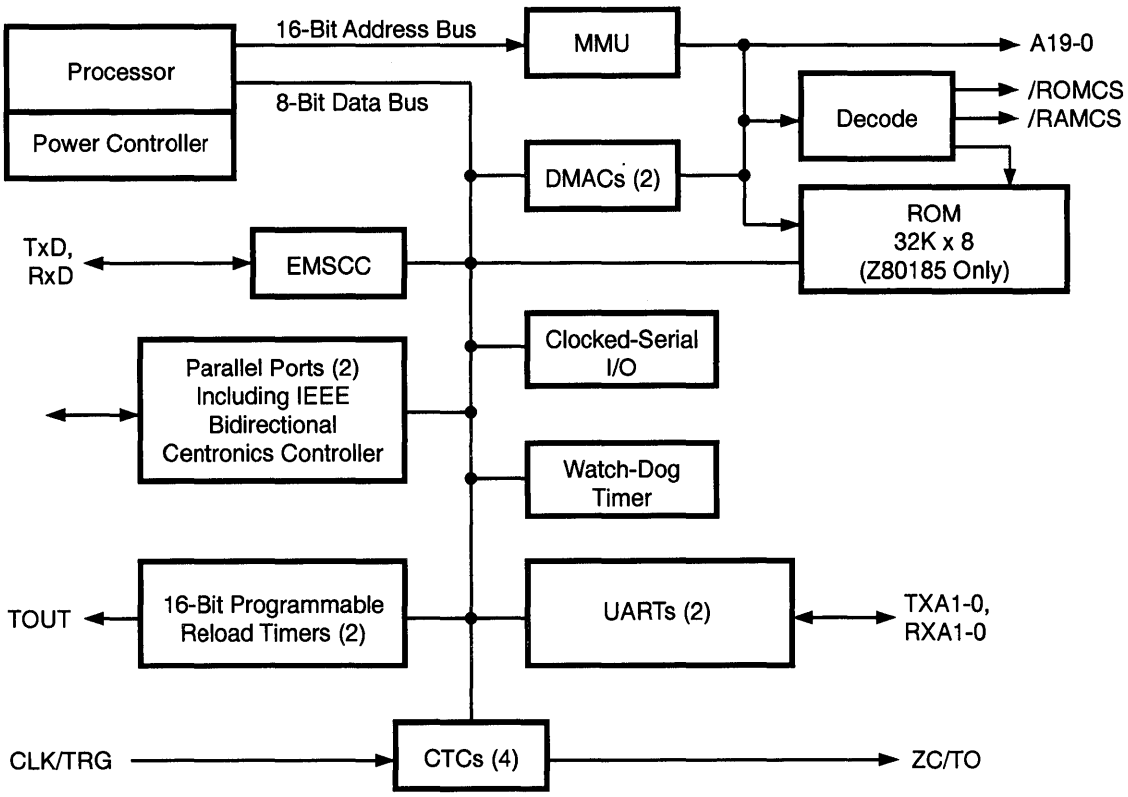


Figure 1. Z80180 Functional Block Diagram

Z80181

Z181™ SAC™ MPU
SMART ACCESS CONTROLLER

GENERAL DESCRIPTION

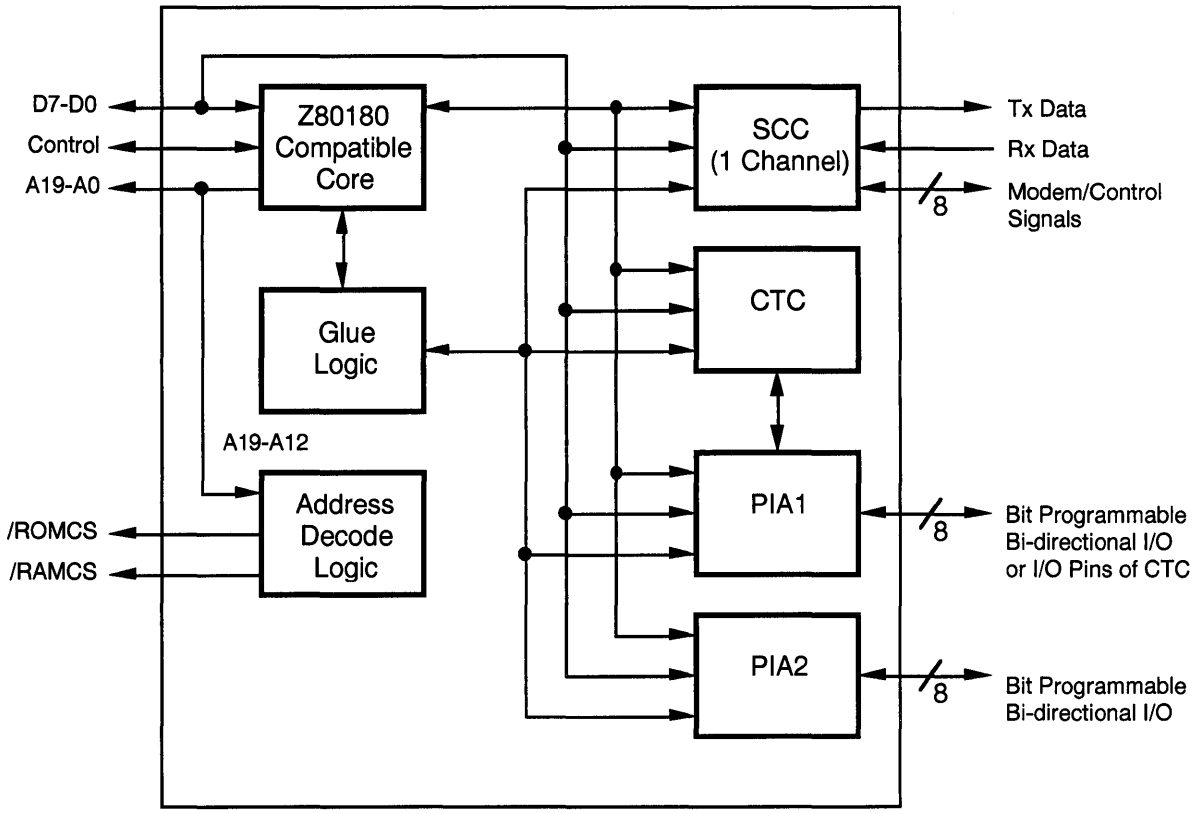
The Z80181 (hereinafter, referred to as Z181) is a CMOS 8-bit microprocessor. It is integrated with the Z180 compatible MPU (Z181 MPU), one channel of Z85C30 Serial Communication Controller (SCC™), Z80® CTC, two 8-bit general-purpose parallel ports, and two chip select signals, all into a single 100-pin QFP package. This high-end superintegrated intelligent peripheral controller is targeted for a broad range of intelligent communication control applications, i.e., terminals, printers, modems, and slave communication processors for 8-, 16- and 32-bit MPU based systems. Also included are enhancement/cost reductions of existing hardware using Z80/Z180 with Z8530/Z85C30 applications. The Functional Block Diagram shows the Z80181.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

11



Z80181 = Z180 + SCC/2 + CTC + PIA

Functional Block Diagram

Z80182

ZILOG INTELLIGENT PERIPHERAL CONTROLLER (ZIP™)

FEATURES

- Z8S180 MPU
  - Code Compatible with Zilog Z80®/Z180™ CPU
  - Extended Instructions
  - Operating Frequency: 33 MHz/5V or 20 MHz/3.3V
  - Two DMA Channels
  - On-Chip Wait State Generators
  - Two UART Channels
  - Two 16-Bit Timer Counters
  - On-Chip Interrupt Controller
  - On-Chip Clock Oscillator/Generator
  - Clocked Serial I/O Port
  - Fully Static
  - Low EMI Option
- Two ESCC™ Channels with 32-Bit CRC
- Three 8-Bit Parallel I/O Ports
- 16550 Compatible MIMIC Interface for Direct Connection to PC, XT, AT Bus
- 100-Pin Package Styles (QFP, VQFP) (0.8 Micron CMOS 5120 Technology)
- Individual WSG for RAMCS and ROMCS

GENERAL DESCRIPTION

The Z80182 is a smart peripheral controller IC for modem (in particular V. Fast applications), fax, voice messaging and other communications applications. It uses the Z80180 microprocessor (Z8S180 MPU core) linked with two channels of the industry standard Z85230 ESCC (Enhanced Serial Communications Controller), 24 bits of parallel I/O, and a 16550 MIMIC for direct connection to the IBM PC, XT, AT bus.

The Z80182 allows complete flexibility for both internal PC and external applications. Also current PC modem software compatibility can be maintained with the Z80182 ability to mimic the 16550 UART chip. The Z80180 acts as an interface between the ESCC™ and 16550 MIMIC interface when used in internal applications, and between the two ESCC channels in the external applications. This interface allows data compression and error correction on outgoing and incoming data. In external applications, three 8-bit parallel ports are available for driving LEDs or other devices. Figure 1 shows the Z80182 block diagram, while the pin assignments for the QFP and the VQFP packages are shown in Figures 2 and 3, respectively.

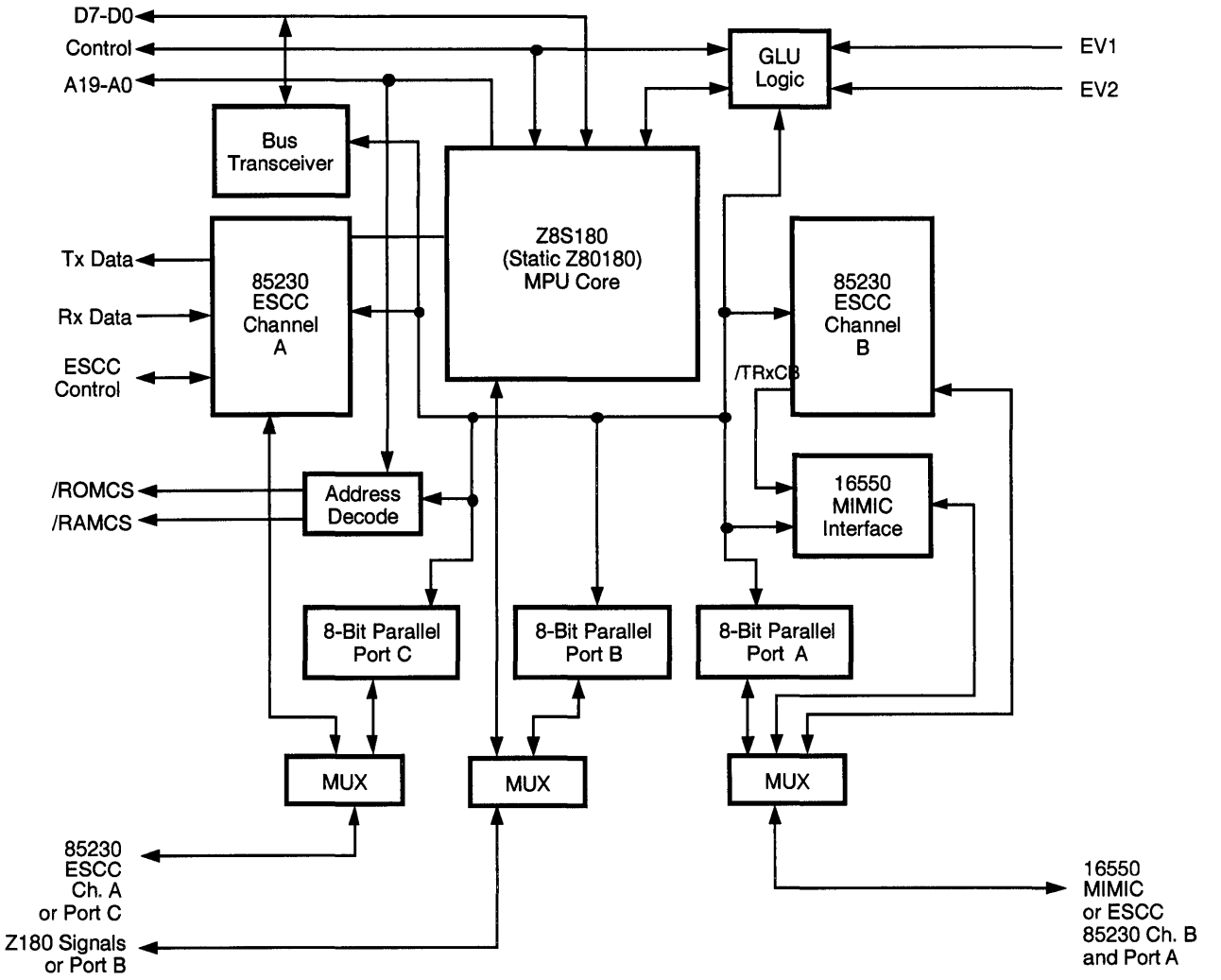
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

11

GENERAL DESCRIPTION (Continued)



Note: Conventional use of the term "MPU side" refers to all interface through the Z180 MPU core and "PC side" refers to all interface through the16550 MIMIC interface.

Figure 1. Z80182 Functional Block Diagram

Z80185/Z80195

SMART PERIPHERAL CONTROLLERS

FEATURES

Device	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z80185	32 x 8	512 Kbps	20, 33
Z80195	0	512 Kbps	20, 33

Note: *General-Purpose

- 100-Pin QFP Package
- 5.0-Volt Operating Range
- Low-Power Consumption
- 0°C to +70°C Temperature Range
- Enhanced Z8S180™ MPU
- Four Z80® CTC Channels
- One Channel ESCC™ Controller
- Two 8-Bit Parallel I/O Ports
- Bidirectional Centronics Interface (IEEE 1284)
- Low-EMI Option

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GENERAL DESCRIPTION

The Z80185 and Z80195 are smart peripheral controller devices designed for general data communications applications, and architected specifically to accommodate all input and output (I/O) requirements for serial and parallel connectivity. Combining a high-performance CPU core with a variety of system and I/O resources, the Z80185/195 are useful in a broad range of applications. The Z80195 is the ROMless version of the device.

The Z80185 and Z80195 feature an enhanced Z8S180 microprocessor linked with one enhanced channel of the Z85230 ESCC™ serial communications controller, and 25 bits of parallel I/O, allowing software code compatibility with existing software code.

Seventeen lines can be configured as bidirectional Centronics (IEEE 1284) controllers. When configured as a 1284 controller, an I/O line can operate in either the host or peripheral role in compatible, nibble, byte or ECP mode. In addition, the Z80185 includes 32 Kbytes of on-chip ROM.

These devices are well-suited for external modems using a parallel interface, protocol translators, and cost-effective WAN adapters. The Z80185/195 is ideal for handling all laser printer I/O, as well as the main processor in cost-effective printer applications.

Notes: All Signals with a preceding front slash, "/", are active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

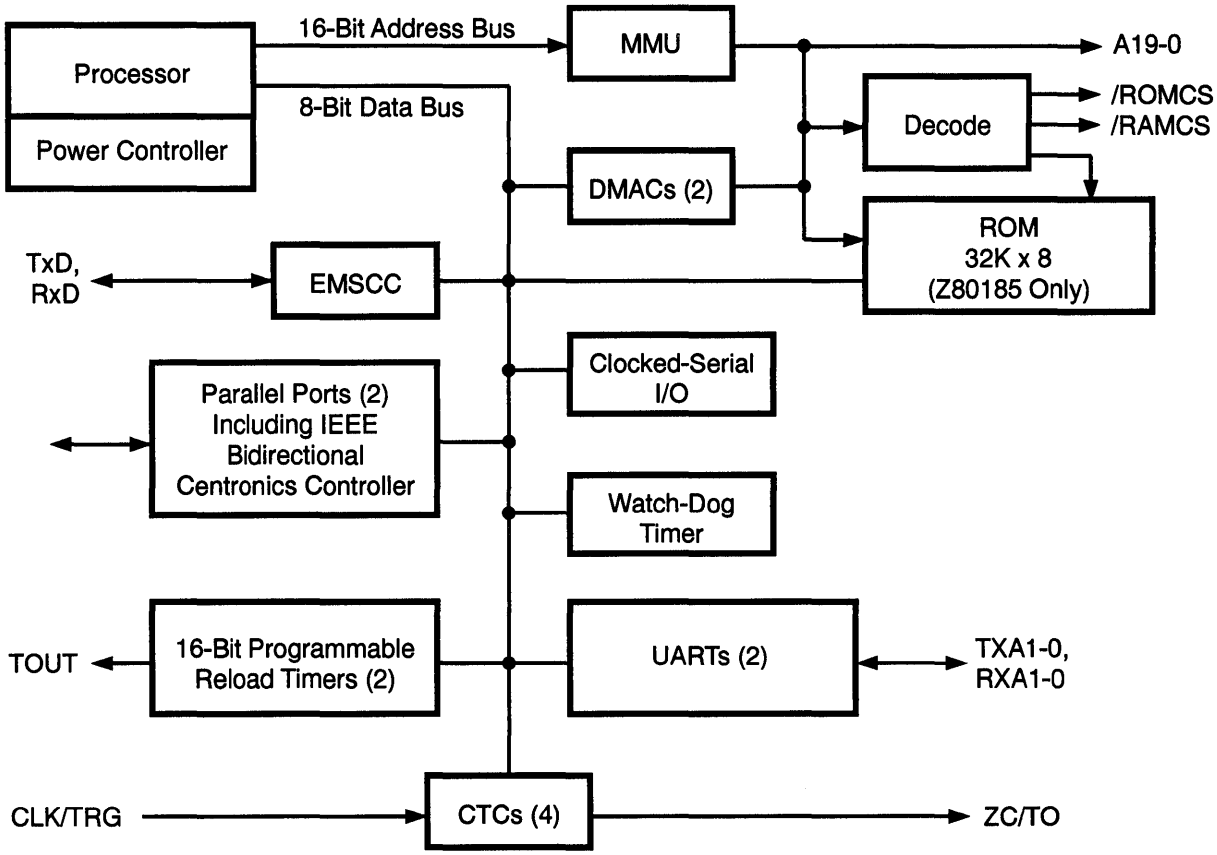


Figure 1. Functional Block Diagram

Z80189/Z8L189

GENERAL-PURPOSE EMBEDDED CONTROLLERS

FEATURES

Part	CPU	UART	I/O	Speed (MHz)
Z80189	S180*	16550	24	33
Z8L189	S180*	16550	24	20

- Fully Static Z180™ MPU Core*
  - On-Chip 1 MByte MMU
  - Two Enhanced UART Channels (up to 512 Kbps)†
  - Two Chain-Linked DMA Channels†
  - x 2 Clock Multiplier
  - Low-Power Consumption Modes
  - Two 16-Bit Timer/Counters
  - Clocked Serial I/O
  - On-Chip Wait State Generator (WSG)
  - On-Chip Interrupt Controller
  - On-Chip Clock Oscillator/Generator
- 16550 Compatible MIMIC Interface
  - 16 mA MIMIC Output Drive Capability
- Com Port Decode
- PC DMA Mailbox Registers
- Host I/O Mailbox
- Programmable Fixed /ROMCS and /RAMCS Boundaries
- 100-Pin QFP and VQFP Packages
- 3.3 and 5.0-Volt Operating Ranges
- 0°C to +70°C Temperature Range

Notes:
† Enhancements from the Discrete S180 device.

11

GENERAL DESCRIPTION

The Z80189/Z8L189 are cost-effective modem controllers that address a new generation of data pumps having the HDLC formatting feature. Data pumps of these types do not require an HDLC interface; therefore, the Z80189 does not need the ESCC™. The addition of the PC DMA Mailbox Registers allow DMA data transfer between the PC memory and the modem speaker/microphone CODEC. The Z80189 is a smart peripheral controller chip for modem (in particular V.34 applications), fax, voice messaging, and other communications applications.

The Z80189/Z8L189 consists of an enhanced Z8S180 microprocessor, a 16550 MIMIC with increased MIMIC drive capability for direct connection to the IBM PC, XT, AT bus, and 24 bits of parallel I/O. Current PC modem software compatibility can be maintained with the Z80189's ability to mimic the 16550 UART chip. The Z80180 core is the intelligent controller between the data pump and 16550 MIMIC interface when used in internal applications. This intelligent controller performs the data compression and error correction on outgoing and incoming data.

The integration of COM Port Decode circuitry to the Z80189 allows the MIMIC to be selected for a specific COM Port Address (PC COM Port Address 1-4). COM Port Decode circuitry is simplified by allowing the user to select the MIMIC COM Port addresses through software, in addition to eliminating the need for external circuitry required for COM Port Decode logic.

The PC DMA and I/O Mailbox Interface can be used to provide communication paths between the PC Host and the Z80189. These new communication paths can be used for voice, DTAD, or jumperless COM Port selection.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

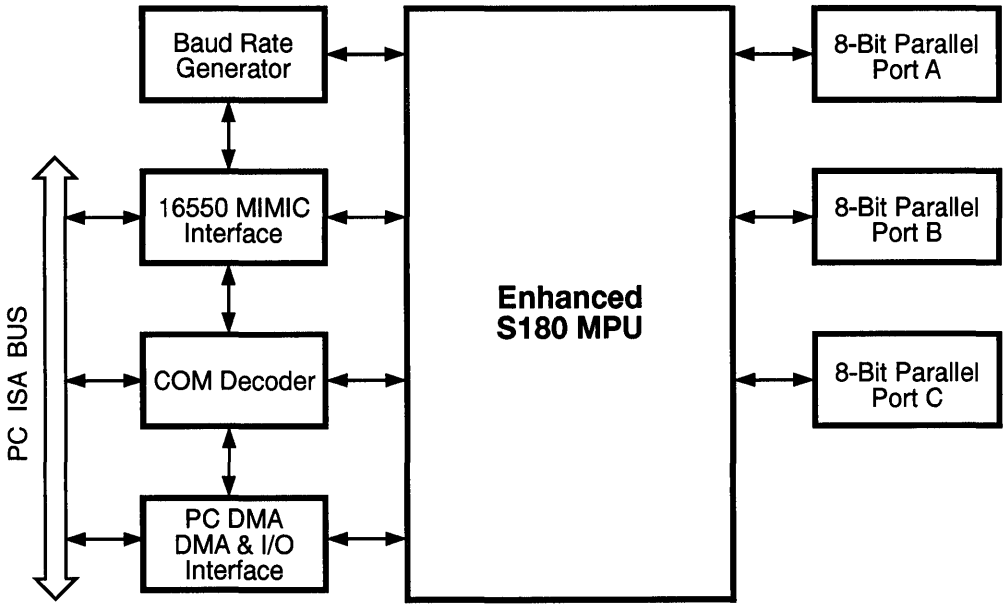


Figure 1. Z80189 Block Diagram

Communication Controllers

Z80/Z180 Microprocessors

Z380™ MPU

MICROPROCESSOR UNIT

GENERAL DESCRIPTION

Zilog's new Z380 Microprocessor Unit (MPU) is an integrated high-performance microprocessor designed to give the end-user a powerful and cost-effective solution to application requirements. The Z380 MPU incorporates advanced architectural features that allow fast and efficient throughput and increased memory addressing capabilities while maintaining Z80 CPU and Z180 MPU object code compatibility. The Z380 offers a continuing growth path for present Z80 or Z180-based designs and serves as a high-performance microprocessor for new designs.

Central to the Z380 MPU is an enhanced version of the Z80 CPU. The Z80 CPU instruction set has been retained, meaning that the Z380 microprocessor is completely binary code compatible with present Z80 and Z180 code. The basic addressing modes of the Z80 microprocessor have been augmented with Stack Pointer relative loads and stores, 16-bit and 24-bit Indexed offsets, and more flexible Indirect Register addressing, with all of the addressing modes allowing access to the entire 32-bit address space. Significant additions have been made to the instruction set, with a full complement of 16-bit arithmetic and logical operations, 16-bit I/O operations, multiply and divide, plus a complete set of register-to-register loads and exchanges.

The basic register file of the Z80 microprocessor is expanded to include alternate register versions of the IX and IY registers. There are four sets of this basic Z80 microprocessor register file present in the Z380 MPU, along with the necessary resources to manage switching between the different register sets. All of the register pairs and index registers in the basic Z80 microprocessor register file are expanded to 32 bits.

The Z380 MPU expands the basic 64 Kbyte Z80 and Z180 address space to a full 4 Gbyte (32-bit) address space. This address space is linear and completely accessible to the user program. The I/O address space is similarly expanded to a full 4 Gbyte (32-bit) range and 16-bit I/O, both simple and block move are added.

Some features that have traditionally been handled by external peripheral devices have been incorporated in the design of the Z380 microprocessor. The on-chip peripherals reduce system chip count and reduce interconnection on the external bus. The Z380 MPU contains a refresh controller for DRAMs that employs a /CAS-before-/RAS refresh cycle at a programmable rate and burst size.

Six programmable memory chip selects are available, along with programmable wait-state generators for each chip select address range.

The Z380 MPU provides very flexible bus interface timing, with separate control signals and timing for memory and I/O. The memory bus control signals provide timing references suitable for direct interface to DRAM, static RAM, EPROM or ROM. Full control of the memory bus timing is possible because the /WAIT signal is sampled three times during a memory transaction, allowing complete user control of edge-to-edge timing between the reference signals provided by the Z380 MPU. The I/O bus control signals allow direct interface to members of the Z80 family of peripherals, or the Z8500 series of peripherals.

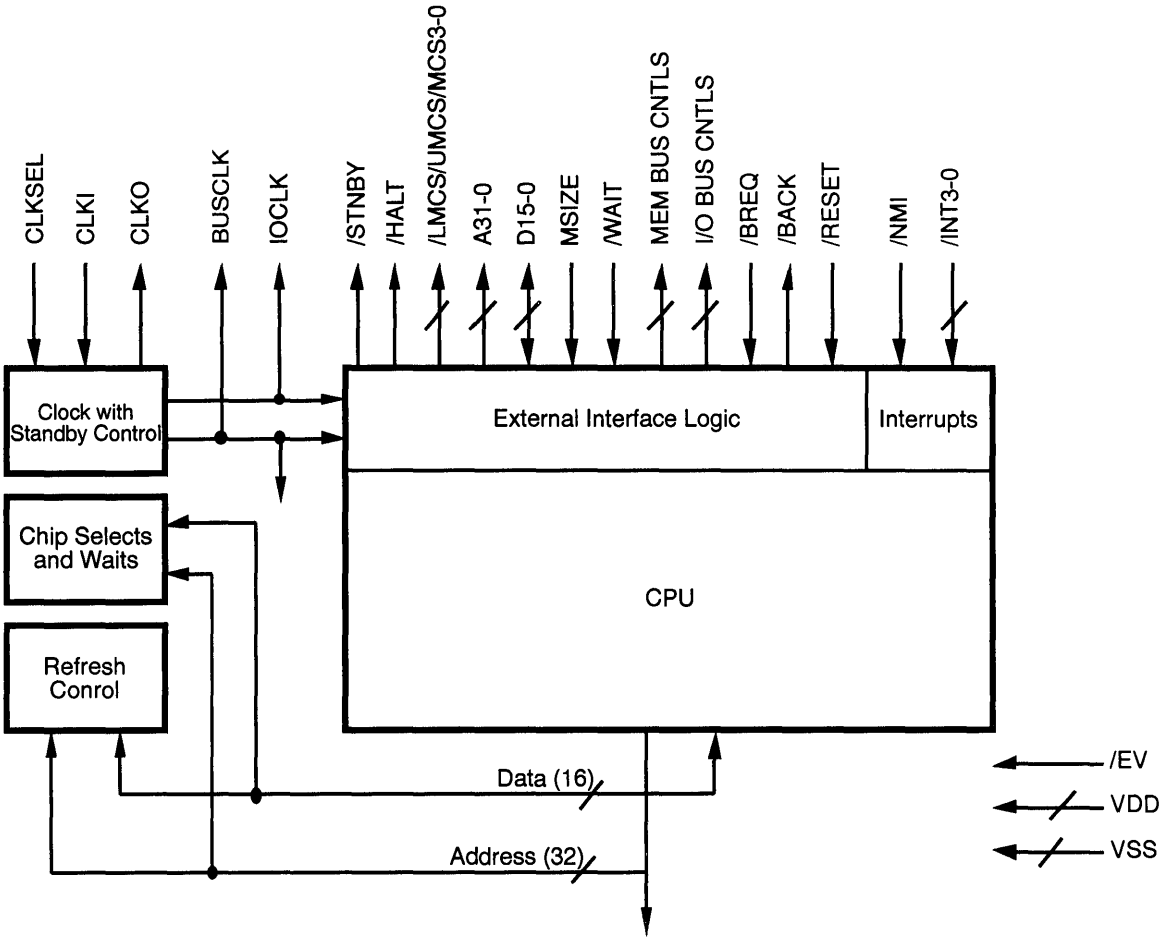
The Z380 functional block diagram and pin assignments are shown on the next page.

Notes:
All Signals with a preceding front slash, "/", are active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Z380 Functional Block Diagram

LOW VOLTAGE Z380™ MPU

MICROPROCESSOR UNIT

GENERAL DESCRIPTION

Zilog's Z380 Microprocessor Unit (MPU) is an integrated high-performance microprocessor designed to give the end-user a powerful and cost-effective solution to application requirements. The Z380 MPU incorporates advanced architectural features that allow fast and efficient throughput and increased memory addressing capabilities while maintaining Z80 CPU and Z180 MPU object code compatibility. The Z380 offers a continuing growth path for present Z80 or Z180-based designs and serves as a high-performance microprocessor for new designs.

Central to the Z380 MPU is an enhanced version of the Z80 CPU. The Z80 CPU instruction set has been retained, meaning that the Z380 microprocessor is completely binary code compatible with present Z80 and Z180 code. The basic addressing modes of the Z80 microprocessor have been augmented with Stack Pointer relative loads and stores, 16-bit and 24-bit Indexed offsets, and more flexible Indirect Register addressing, with all of the addressing modes allowing access to the entire 32-bit address space. Significant additions have been made to the instruction set, with a full complement of 16-bit arithmetic and logical operations, 16-bit I/O operations, multiply and divide, plus a complete set of register-to-register loads and exchanges.

The basic register file of the Z80 microprocessor is expanded to include alternate register versions of the IX and IY registers. There are four sets of this basic Z80 microprocessor register file present in the Z380 MPU, along with the necessary resources to manage switching between the different register sets. All of the register pairs and index registers in the basic Z80 microprocessor register file are expanded to 32 bits.

The Z380 MPU expands the basic 64 Kbyte Z80 and Z180 address space to a full 4 Gbyte (32-bit) address space. This address space is linear and completely accessible to the user program. The I/O address space is similarly expanded to a full 4 Gbyte (32-bit) range and 16-bit I/O, both simple and block move are added.

Some features that have traditionally been handled by external peripheral devices have been incorporated in the design of the Z380 microprocessor. The on-chip peripherals reduce system chip count and reduce interconnection on the external bus. The Z380 MPU contains a refresh controller for DRAMs that employs a /CAS-before-/RAS refresh cycle at a programmable rate and burst size.

Six programmable memory chip selects are available, along with programmable wait-state generators for each chip select address range.

The Z380 MPU provides very flexible bus interface timing, with separate control signals and timing for memory and I/O. The memory bus control signals provide timing references suitable for direct interface to DRAM, static RAM, EPROM or ROM. Full control of the memory bus timing is possible because the /WAIT signal is sampled three times during a memory transaction, allowing complete user control of edge-to-edge timing between the reference signals provided by the Z380 MPU. The I/O bus control signals allow direct interface to members of the Z80 family of peripherals, or the Z8500 series of peripherals.

The Z380 functional block diagram and pin assignments are shown on the next page.

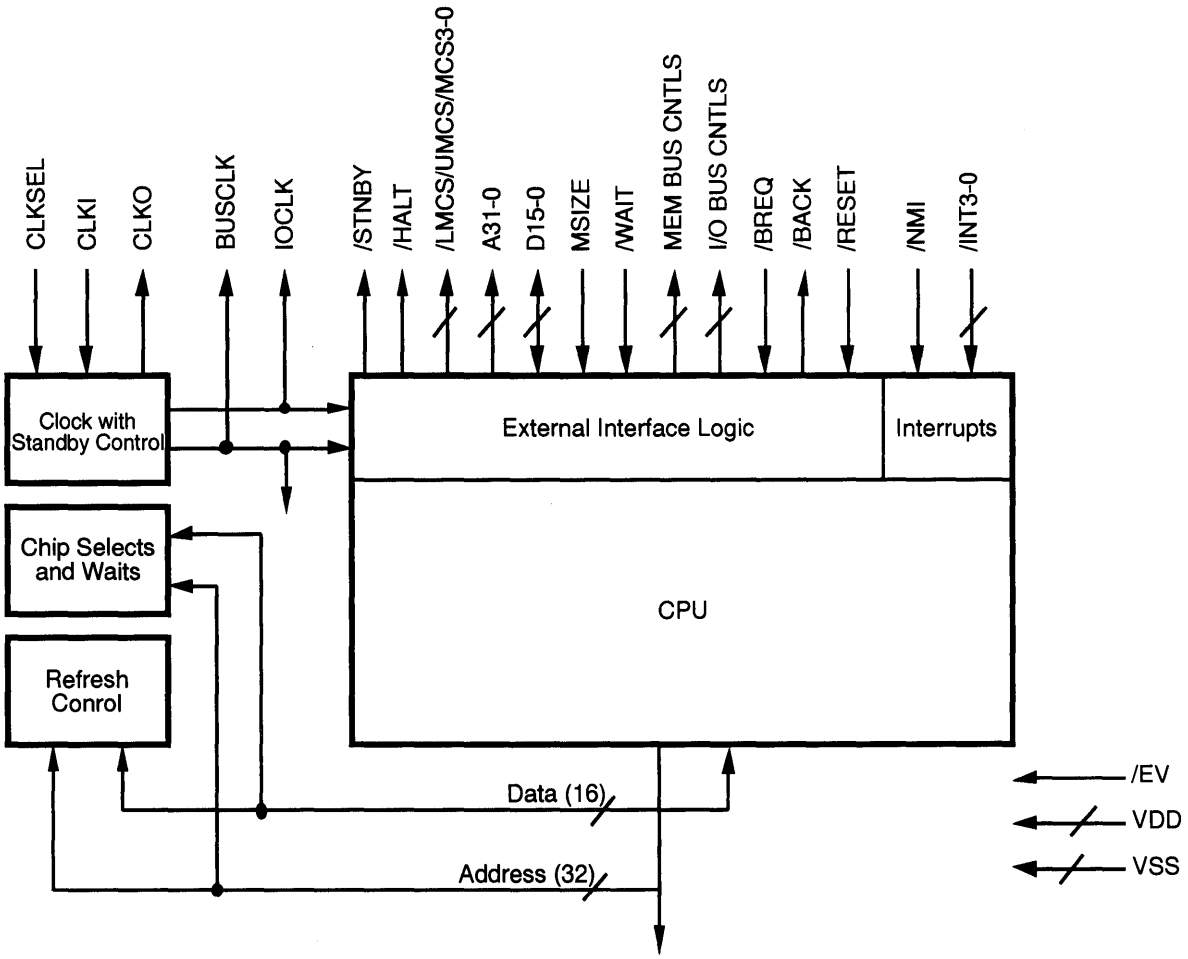
The Zilog Low Voltage Z380 is specified to operate at 3.3 volts ± 10%. The maximum speed grading for the above voltage is 10 MHz.

Notes:
All Signals with a preceding front slash, "/", are active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Z380 Functional Block Diagram

ZiLOG

SUPPORT PRODUCT

Z8038000ZAS

Z80380 ASSEMBLER, LINKER AND LIBRARIAN

GENERAL DESCRIPTION

The Z80380 Macro Assembler

The Z80380 Macro Assembler (ZASM) generates relocatable object code modules in IEEE 695 OMF format. The assembler also handles macros and conditional assembly, eliminating the need for a macro preprocessor.

The Z80380 Linker

The Z80380 Linker (ZLINK) links object modules produced by the assembler. The linker produces two files:

- an absolute object file in Motorola S-record format, and
- an optional comprehensive linkmap file.

Linking offers the benefits of:

- smaller, faster-assembling modules,
- use of local and global variables, and
- ease of relocating to a specified address.

Linking lets the user develop commonly-used routines separately, test them, and link them to programs under development.

The Z80380 Librarian

The Z80380 Librarian (ZLIB) is the librarian facility. The librarian can be used to place the relocatable object files in a library. In this way, the user can collect user-defined modules which allows commonly used routines to be easily included in programs.

Requirements

The PLC Z80380 Macro Assembler/Linker/Librarian requires an IBM® PC or true compatible with:

- DOS 5.0 or higher
- 5 Mbytes of hard disk space
- floppy drive
- mouse
- 80386 or 80486 CPU
- 4 Mbytes of RAM

Device Supported

Z80380/Z80180/Z84C00

Kit Contents

Software (IBM PC platform)

Assembler, linker, librarian

Documentation

Macro Assembler/linker/librarian User's Guide.
Registration Card.

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* IBM is a registered trademark of International Business Machines Corp.

Z8038000ZCO

Z80380 EVALUATION BOARD

DESCRIPTION

This kit contains an assembled circuit board, software and documentation to aid evaluators and potential users in designing with the Z80380.

The supplied Z80™ cross assembler and link/loader package allows full assembly language programming support. A board resident debug monitor program allows executable code to be down-loaded and subsequently debugged.

Supported Devices
Z80380

Specifications
Power Requirements
+5 V_{DC} @ 140 mA

Dimensions
Width: 5.6 in.
Length: 7.6 in.

Serial Interface
RS-232C @ 9600 Baud

KIT CONTENTS

Z80380 Evaluation Board
CMOS 80380 MPU
CMOS 85230 ESCC™
18.432 MHz Oscillator
1 Socketed 32K x 8 EPROM
2 Socketed 8K x 8 EPROMs
1 Socketed 32K/128K x 8 Static RAM
2 Unsocketed 1 Mb Dynamic RAM Slots
RS-232C PC Interface
Reset Switch
NMI Switch

Cables
RS-232 Ribbon Cable
Pigtail Power Cable

Software (IBM® Platform)
Z80380 EPM™
Resident Debug Monitor Source Code
Resident ESCC Device Driver
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader

Documentation
Z80380 Kit User Manual
Z380 Technical Manual
Z380 Product Specification
SCC User's Manual
EPM User Manual
Z80 Cross Assembler User Guide
MOBJ Link/Loader User Guide

References
Third Party Hardware and Software Support
(Not Supplied with Kit)

Z380 Assembler:	PLC (817) 599-8365
Z380 ICE:	Signum (805) 371-4608

* IBM is a registered trademark of International Business Machines Corp.

Additional Information

Zilog's Quality and Reliability Program

Introduction

Zilog Inc. has an excellent reputation for the quality and reliability of its products.

Zilog's Quality and Reliability Program is based on careful study of the principles laid down by such pioneers as W.E. Deming and J.M. Juran, but even more importantly, the observation and practical implementation of those principles as practiced in Japanese, European and American manufacturing facilities.

The Zilog program begins with employee involvement. Whether the judgement of our performance is based on perfection with incoming inspection, trouble-free service in the field, or timely and accurate customer service, we recognize that our employees ultimately control these factors. Hence, our Quality Program is broadly shared throughout the organization.

1. Harmony Between Design and Process

High product quality and reliability in VLSI products are possible only if there is structural harmony between product design and manufacturing. Great care is taken to ensure that the statistical process control limits observed within the manufacturing plants properly guardband the design technology used to configure the circuit and layout in Zilog's automated design methodology.

Through use of a technique which we call Process Templating, the technology file in the automated design system is periodically updated to ensure that product design parameters fall within the statistical control limits with which the process is actually operated. In simple terms, the Process Template is the profile displayed by the process evaluation parameters which are automatically recorded from the test patterns on wafers as they proceed through the production line. These parameters are translated into the design technology file attributes so every product design technology file attributes bears a key and lock relationship to the process.

2. Training

The integrity of our product design and manufacturing process depends on the skills of our employees. Zilog training emphasizes the fundamentals involved in product design and processing for quality and reliability.

Customer Service, an important aspect of Zilog's quality performance as a vendor, also depends upon our people clearly understanding their jobs, and our obligations to our customers. This too is part of the training curriculum administered by Zilog.

3. Order Acknowledgment Policy

One definition of vendor quality performance is that the vendor "does what he promises or acknowledges." Reliability and quality warranties are met only if Zilog and the customer are in agreement on product and delivery specifications. Zilog makes an extra effort to ensure that the customer is fully informed by providing documents with its purchase order acknowledgments that clearly state what Zilog understands the specifications to be.

4. Test Guardbanding

No physical attribute is absolute. Customers' test methods may differ from Zilog's due to variations in test equipment, temperature or specification interpretation. To ensure that every Zilog product performs to full customer expectations, Zilog uses a "waterfall" methodology in its testing. The first electrical tests made on the circuit, at the wafer probe operation, are guardbanded to the final test specifications. The final test specifications, in turn, are guardbanded to the quality control outgoing sample. The quality control outgoing sample is guardbanded to the customer procurement or data sheet specifications. This technique of "waterfall" guard-banding ensures that circuits which may be marginal to the customer's expectations are eliminated in the manufacturing process long before they get to the shipping container.

5. Probe at Temperature

Semiconductor devices tend to exhibit their most limited performance at the highest operating temperature. Therefore, it is Zilog's policy that all chips are tested at high temperature the very first time they are electrically screened, at the wafer probe station. The circuits are tested again at their upper operating temperature limit in the 100% final test operation.

6. Process Characterization

Before release to production, every process is thoroughly characterized by an exhaustive series of pilot production runs and tests which identify the statistical, electrical, and mechanical limits of which that particular process regime is capable. This documentation, which fills a large loose-leaf binder for each process, is maintained as the historical record or "footprint" for that particular regime.

Process recharacterization is done any time there is a major process or manufacturing site change, and the resulting documentation is then added to the characterization history. Once the process is fully characterized, the frequent test site evaluation and process template data demonstrate that the process remains in specification.

7. Product Characterization
Every Zilog product design is evaluated over extremes of operating temperature, supply voltage and clock frequencies, prior to production release. This information permits the proper guardbanding of the test program waterfall and identification of any marginal "corners" in design tolerances.

A product characterization report, which summarizes the more important tolerances identified in the process of this exhaustive product design evaluation, is available to Zilog's customers.

8. Process Qualification
Zilog also qualifies every process prior to production by an exhaustive stress sequence performed on test chips and on representative products. Once a process regime is qualified, a process requalification is performed any time there is a major process change, or whenever the process template statistical quality limits are significantly exceeded or adjusted.

9. Product Qualification
In addition to characterization, every new Zilog product design is fully qualified by a comprehensive series of life, electrical, and environmental tests before release to production. Again, a qualification report is available to our customers which summarizes certain key life and environmental data taken in the course of these evaluations. Whenever possible, industry standard environmental and life tests are employed.

10. PPM Measurement, Direct and Indirect
It is frequently said that if you want to improve something, you need to put a measure on it. Therefore, Zilog measures its outgoing quality "parts per million" by the maintenance of careful records on the statistical sampling of production lots prepared for shipment. This information is then translated by our statisticians to a statement of our parts per million (or parts per billion) outgoing quality performance.

Of course, it is one thing for Zilog to think it is doing a good job in outgoing product quality and it is another for a customer to agree. Therefore, we ask certain key customers to provide us with their incoming inspection data which helps us calibrate our outgoing performance in terms of the actual results in the field. The fact that Zilog has been awarded "ship to stock" status by many customers testifies to our success in this area.

11. FIT Measurement Direct and Indirect
Just as Zilog records its outgoing quality in terms of parts per million, it also measures its outgoing product reliability in terms of "FITS" or failures per billion device hours, using the results of weekly operating life test measurements on the circuits, performed in accordance with standard specifications.

12. Field Quality Engineers
It is frequently said that the customer is always right. If the customer has an application quality or reliability problem while using a Zilog product, whether it is Zilog's responsibility or not, we believe that we have a responsibility to resolve it. Therefore, Zilog maintains a force of skilled Applications Engineers who are also trained as field quality engineers and are available on immediate call to consult at the customer's locations on any problems they may be experiencing with Zilog product performance.

13. Product Analysis
As noted earlier, we feel that a customer problem is a Zilog problem. Accordingly, Product Analysis facilities, staffed by experienced professionals, exist at each Zilog site to provide rapid evaluation of in-process and in-field rejects to determine the cause and provide corrective action through a feedback loop into the production, design, and applications process. Zilog is pleased to share product analysis reports on specific products with the customer upon request.

14. Test Site Step-Stress
The process evaluation test sites on the wafer are packaged and subjected to step-stress testing. Any drift in parameters under severe conditions of stress outside the norm is taken as an indication of possible process contamination or variation.

15. Statistical Process Control
Zilog employs Statistical Process Control at all critical process steps. Deviations from norms must be evaluated by a Q/R review board.

16. Perfection Plus Program
Zilog employees actively participate in meetings where methods are proposed, reviewed, and adopted and which enable a department to do its job in more of a precise and accurate manner. Employees who have made suggestions proudly wear the Zilog Perfection Plus pin.

17. Zilog Vendor of the Year Award
Zilog is proud of the many quality and performance awards it has received from its customers. In turn, Zilog makes an annual award to the vendor who has done the best overall job for Zilog.

Additional Information

Z8® MICROCONTROLLERS
IR REMOTE CONTROLLERS
KEYBOARD CONTROLLERS

Hardware Support

Company	Phone	Devices
Creative Technology	(404) 455-8255	IR
Data I/O (OTP Programmer)	(800) 332-8246	Z8/IR
Emulation Technologies (OTP Socket Adapters)	(408) 982-0660	Z8
iSystems (Germany)	(49) 8131-25085	Z8/IR/KEY
JK Systems (Singapore)	011-65-744-8418	IR/KEY
Logical Devices, Inc. (OTP Programmer)	(303) 279-6868	Z8/IR
Microtime (Taiwan)	011-886-2-881-1791	IR
Needham Electronics (OTP Programmer)	(916) 924-8037	Z8
Orion Instruments	(408) 747-0440	Z8/IR/KEY
Signum Systems	(805) 523-9774	Z8/KEY
System General (OTP Programmer)	(408) 263-6667	Z8
Wytec	(708) 894-1440	IR

Software Support

Company	Phone	Devices
Allen Ashley	(818) 793-5748	Z8
Avocet Systems	(800) 448-8500	Z8/IR
Byte Craft	(519) 888-6911	Z8/IR/KEY
Cybernetic Micro	(415) 726-3000	Z8
Eris Systems	(612) 374-2967	Z8/KEY
Laboratory Microsystems	(213) 306-7412	Z8
Micro Computer Control	(609) 466-1751	Z8/IR/KEY
Micro Dialects	(513) 271-9100	Z8
MPE	(716) 461-9187	Z8
Pseudo Corp.	(514) 683-9173	Z8/IR/KEY
PLC	(817) 599-8363	Z8/IR
Software Development	(800) 448-7733	Z8
Western Wares	(303) 327-4888	Z8/IR/Key
2500 A.D. Software	(800) 843-8144	Z8/IR/KEY

MASS STORAGE

Hardware Support

Company	Phone
MacroChip Research, Inc. Emulator	(214) 242-0450

Software Support

Company	Phone
PLC	(817) 599-8363

WIRELESS DEVICES

Software Support

Company	Phone
PLC	(817) 599-8365

SERIAL COMMUNICATION CONTROLLERS

Hardware Support

Company	Phone
Computer Modules 2350A Walsh Avenue Santa Clara, CA 95051 Two Channel, High Speed Async/Sync Serial Interface for the IBM PC/AT bus	(408) 496-1881
Metacomp 10989 Via Frontera San Diego, CA 92127 Multi-Protocol Serial Communications Board that can be configured for RS-232C, RS-449, RS-485, RS-423, V.35, X.21 and MILSTD-188/114A interface standards	(619) 674-5000
Comtrol	(800) 926-6876

Software Support

Company	Phone
Forward Technology 125 Michael Drive Syosset, NY 11791 Software drivers for SCCs/ESCCs, Z16C22	(516) 496-9033
GCOM 1776 East Washington Street Urbana, IL 61801 Drivers for SCCs/ESCCs/ISCC for many common protocols including Frame Relay, X.25, LAPD, SDLC/HDLC	(217) 337-4471
Novell NetWare Multi-Protocol router (MPR 2.1) driver for the NW2000 Frame Relay available Dec. '93 with X.25 and PPP coming in Q194 **(Z16C32 Only)**	
Probitas Corporation 2570 El Camino Real, Suite 310 Mountain View, CA 94040 LLAP driver, Appletalk protocol stack, custom projects	(415) 941-2090
Telnetworks 625 Second Street Petaluma, CA 94952 Software for data and telecommunications Specialists in ISDN protocols **(Z16C32 Only)**	(707) 778-8737
Trillium Digital Systems 2001 S. Barrington Avenue #2 Los Angeles, CA 90025 Protocol stacks for SCCs	(310) 479-0500

Z80, Z180, Z181, Z182 AND Z185 MICROPROCESSORS

Hardware Support

Company	Product	Phone
American Automation	Emulator	(714) 731-1661
Applied Microsystems	Emulator	(206) 882-2000
Cactus Logic	IDS/LC	(818) 337-4547
Emulation Technology	80180 Emulator	(408) 982-0660
Hewlett-Packard	Emulator pods for HP 64000/UX/PC	(800) 4HP-DATA
Huntsville Microsystems	Emulator	(205) 881-6005
iSystems (Germany)	Emulator	49-8131-25085
Lauterbach (Germany)	Emulator	49-8104-8943-0
Lauterbach	Emulator	(508) 620-4521
Micromint	SB180, SB180FX, BCC180, RTC180	(800) 635-3355
MicroWorks	Prototyping Board	(408) 997-1644
Orion Instruments	80180 Emulator	(408) 747-0440
Pentica Systems, Inc.	Emulator	(617) 577-1101
Softaid	Emulator, ICEBOX, ICE Analyzer	(800) 433-8812
Softart	Modem Development Kit	(519) 746-6750
Sophia Systems	Emulator, SA 2000	(415) 493-6700
Versalogic	Z80 STD Bus Circuit Brd	(800) 824-3163
Z-World	IBM PC Development Board	(916) 753-3722
Zaxtek	Emulator	(714) 474-1170

Software Support

Company	Phone
2500 AD	(800) 843-8144
Allen Ashley	(818) 793-5748
American Automation	(714) 731-1661
Avocet Systems	(800) 448-8500
Enertec	(215) 362-0966
Huntsville	(205) 881-6005
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Micro Computer Tools	(415) 825-4200
MicroDialects	(513) 271-9100
Micromint	(800) 635-3355
Microtek Research	(408) 980-1300
MPE	(716) 461-9187
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Softtools	(410) 750-3733
Software Development Systems	(708) 990-4640
The AG Group	(510) 937-7900
Z-World	(916) 753-3722

Z380 MICROPROCESSORS

Hardware Support

Company	Phone
Signum	(805) 523-9774

Software Support

Company	Phone
2500 AD Assembler	(800) 843-8144
PLC C-Compiler/Assembler	(817) 599-8365

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Promate Electronics Co. Ltd. 886-2-659-0303

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Eltee Electronics Ltd. 66-2-933-7565

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Ceske Mezirizi
ECOM spol 42-443-92202

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Thesys/AE 49-6434-5041

Berlin
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EBV Elektronik GMBH 49-30-3421041

Burgwedel
EBV Elektronik GMBH 49-5139-80870

Dortmund
Future GMBH 49-231-9750480

Duesseldorf
Thesys/AE 49-211-5360214

Eppstein/Taunus
EBV Elektronik GMBH 49-6198-59200

Erfurt
Future GMBH 49-361-420870
Thesys 49-361-4278101

Erkrath
Avnet/Electronic 2000 49-211-920030

Frankfurt
Avnet/Electronic 2000 49-69-9738040

Gerlingen
Avnet/Electronic 2000 49-7156-3560

Hamburg
Avnet/Electronic 2000 49-40-6969520

Idstein
Future GMBH 49-6126-93210

Kaarst
EBV Elektronik GMBH 49-2131-96770

Langenhagen
Future GMBH 49-511-725620

Leonberg
EBV Elektronik GMBH 49-7152-30090

Muenchen
Avnet/Electronic 2000 49-89-4511001
EBV Elektronik GMBH 49-89-991140
Future GMBH 49-89-957270
Thesys A/E 49-89-99355866

Nuernberg
Avnet/Electronic 2000 49-911-931490

Quickborn
Future GMBH 49-4106-71021

Stuttgart
Future GMBH 49-711-830380
Thesys/AE 49-711-9889100

Weissbach
EBV Elektronik GMBH 49-36426-22486

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Cinisello
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