ZILOG

PRELIMINARY PRODUCT SPECIFICATION

Z80182

ZILOG INTELLIGENT PERIPHERAL (ZIP™)

Q2/92

ZILOG

PRELIMINARY PRODUCT SPECIFICIATION

Z80182

ZILOG INTELLIGENT PERIPHERAL (ZIP™)

FEATURES

- Z80180 MPU Core
  - Code Compatible with Zilog Z80® CPU
  - Extended Instructions
  - Operating Frequency DC to 16 MHz and 20 MHz
  - Two DMA Channels
  - On-Chip Wait State Generators
  - Two UART Channels
  - Two 16-Bit Timer Counters
  - On-Chip Interrupt Controller
  - On-Chip Clock Oscillator/Generator with Idle and Standby Modes of Operation
  - Clocked Serial I/O Port
  - Fully Static
- Two ESCC™ Channels
- Three 8-Bit Parallel I/O Ports
- 16550 Compatible MIMIC Interface for Direct Connection to PC, PS/2, XT, AT Bus
- Package 100-Pin QFP (Quad Flat Package) or 100-Pin VQFP (Very Small Quad Flat Package)

GENERAL DESCRIPTION

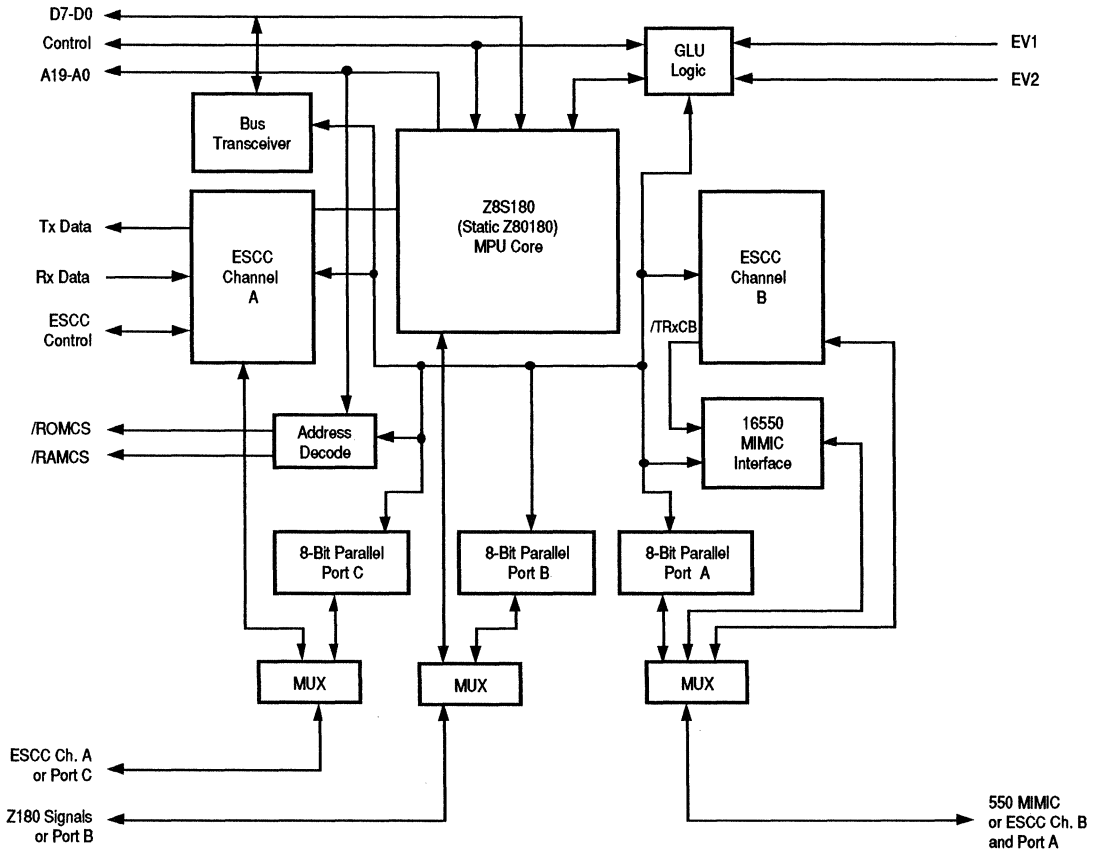
The Z80182 is the Zilog Intelligent Peripheral controller chip that can be used for modems, faxes, voice messaging and other communications applications. It uses the static Z80180 microprocessor (Z8S180 MPU core) linked with two channels of the industry standard Z85230 ESCC™ (Enhanced Serial Communications Controller), 24 bits of Parallel I/O, and a 16550 MIMIC for direct connection to the IBM PC, XT, AT, bus. Two different modes of operation allow complete flexibility for both internal PC and external applications. Also current PC modem software compatibility can be maintained with the Z80182's ability to MIMIC the 16550 UART chip. The Z80180 acts as an interface between the ESCC and 16550 MIMIC interface when used in internal applications and between the two ESCC channels in the external applications. This interface allows for data compression and error correction on outgoing and incoming data. Figure 1 shows the Z80182 block diagram. The pin assignments for the QFP and the VQFP packages are shown in Figures 2 and 3.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Note: The convention uses the term "MPU side" which refers to interface to the Z180 MPU core and "PC side" which refers to all interface via the 16550 MIMIC interface.

Figure 1. Z80182 Block Diagram

PIN DESCRIPTION

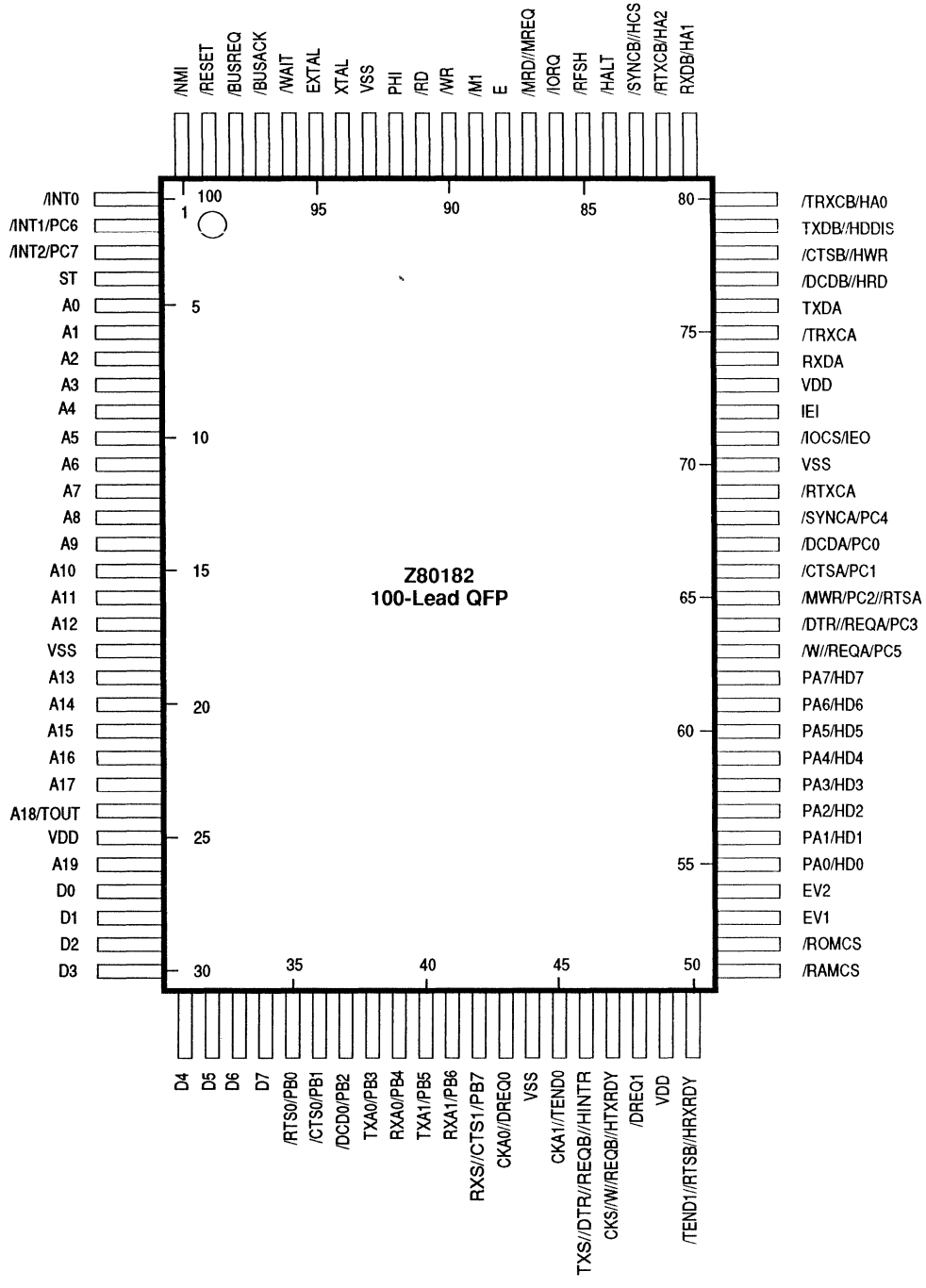


Figure 2. Z80182 100-Lead QFP Pin Identification

PIN DESCRIPTION (Continued)

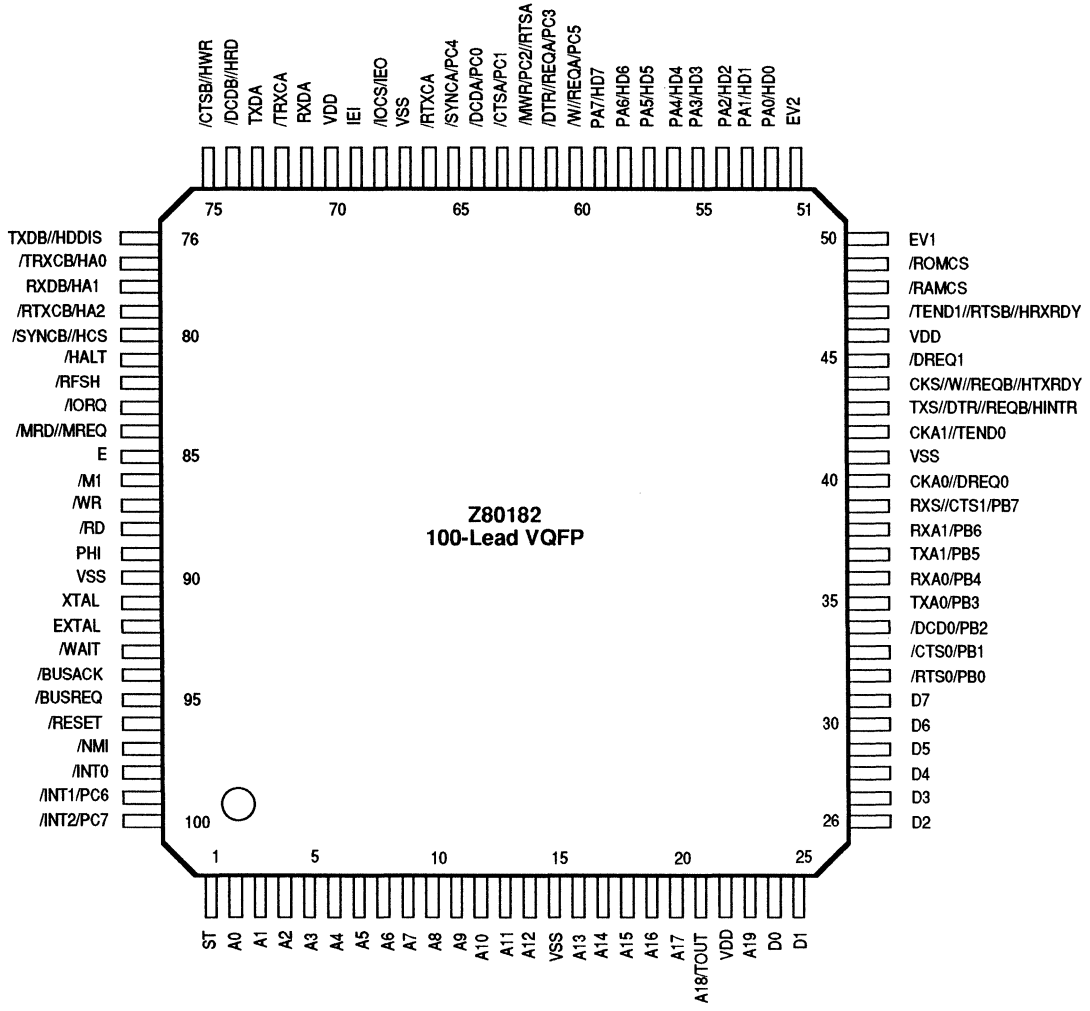


Figure 3. Z80182 100-Lead VQFP Pin Identification

Z180 CPU SIGNALS

A19-A0. *Address Bus (input/output, active High, tri-state).* A19-A0 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges, up to 1 Mbyte, and I/O data bus exchanges, up to 64K. The address bus enters a high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states. This bus is an input when the external bus master is accessing the on-chip peripherals. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset).

D7-D0. *Data Bus (bidirectional, active High, tri-state).* D7-D0 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states.

/RD. *Read (input/output, active Low, tri-state).* /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

/WR. *Write (input/output, active Low, tri-state).* /WR indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

/IORQ. *I/O Request (input/output, active Low, tri-state).* /IORQ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. /IORQ is also generated, along with /M1, during the acknowledgment of the /INT0 input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the IOE signal of the Z64180.

/M1. *Machine Cycle 1 (input/output, active Low).* Together with /MREQ, /M1 indicates that the current cycle is the opcode fetch cycle of an instruction execution; unless /M1E bit in the OMCR is cleared to 0. Together with /IORQ, /M1 indicates that the current cycle is for an interrupt acknowledge. It is also used with the /HALT and ST signals to decode status of the CPU machine cycle. This signal is analogous to the /LIR signal of the Z64180.

/MREQ. *Memory Request (input/output, active Low, tri-state).* /MREQ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the /ME signal of the Z64180. /MREQ is multiplexed with /MRD on the /MRD//MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if the /MREQ function is selected; and is inactive High if /MRD function is selected.

/MRD. *Memory Read (input/output, active Low, tri-state).* /MRD is active when both the internal /MREQ and /RD are active. /MRD is multiplexed with /MREQ on the /MRD //MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if /MREQ function is selected; and is inactive High if /MRD function is selected. The default function on power up is /MRD and may be changed by programming bit 3 of the Interrupt Edge/Pin MUX Register (xxDFH).

/MWR. *Memory Write (input/output, active Low, tri-state).* /MWR is active when both the internal /MREQ and /WR are active. This /RTSA or PC2 combination is pin multiplexed with /MWR on the /MWR/PC2//RTSA pin. The default function of this pin on power up is /MWR, which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

/WAIT. *(input/output active Low).* /WAIT indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The /WAIT input is sampled on the falling edge of T2 (and subsequent wait states). If the input is sampled Low, then additional wait states are inserted until the /WAIT input is sampled High, at which time execution will continue.

/HALT. *Halt/Sleep Status (input/output, active Low).* This output is asserted after the CPU has executed either the HALT or SLEEP instruction, and is waiting for either non-maskable or maskable interrupts before operation can resume. It is also used with the /M1 and ST signals to decode status of the CPU machine cycle. On exit of HALT/SLEEP, the first instruction fetch is delayed 16 clock cycles after the /HALT pin goes High.

/BUSACK. *Bus Acknowledge (input/output, active Low).* /BUSACK indicates to the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

/BUSREQ. *Bus Request (input, active Low).* This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than /NMI and is always recognized at the end of the current machine cycle. This signal will stop the CPU from executing further instructions and places the address/data buses and other control signals, into the high impedance state.

Z180 CPU SIGNALS (Continued)

/NMI. *Non-maskable interrupt (input, negative edge triggered).* /NMI has a higher priority than /INT and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location 0066H.

/INT0. *Maskable Interrupt Request 0 (input/output active Low).* This signal is generated by external I/O devices. The CPU will honor this request at the end of the current instruction cycle as long as the /NMI and /BUSREQ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the /M1 and /IORQ signals become active. The internal Z180 MPU's /INT0 source is: /INT0 or ESCC or the MIMIC.

/INT1, /INT2. *Maskable Interrupt Requests 1 and 2 (inputs, active Low).* This signal is generated by external I/O devices. The CPU will honor these requests at the end of the current instruction cycle as long as the /NMI, /BUSREQ, and /INT0 signals are inactive. The CPU acknowledges these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgment for /INT0, during this cycle neither the /M1 or /IORQ signals become active. These pins may be programmed to provide an active Low level on rising or falling edge interrupts. The level of the external /INT1 and /INT2 pins may be read through bits PC6 and PC7 of parallel Port C. Pin /INT1/PC6 multiplexes /INT1 and PC6. Pin /INT2/PC7 multiplexes /INT2 and PC7.

/RFSH. *Refresh (input/output, active Low, tri-state).* Together with /MREQ, /RFSH indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low order 8 bits of the address bus (A7-A0) contain the refresh address. This signal is analogous to the /REF signal of the Z64180.

Z180 MPU UART AND SIO SIGNALS

CKA0, CKA1. *Asynchronous Clocks 0 and 1 (bidirectional, active High).* These pins are the transmit and receive clocks for the synchronous channels. CKA0 is multiplexed with /DREQ0 on the CKA0//DREQ0 pin. CKA1 is multiplexed with /TEND0 on the CKA1//TEND0 pin.

CKS. *Serial Clock (bidirectional, active High).* This line is clock for the CSIO channel and is multiplexed with the ESCC signal (/W//REQB) and the 16550 MIMIC interface signal /HTxRDY on the CKS//W//REQB//HTxRDY pin.

/DCD0. *Data Carrier Detect 0 (input, active Low).* This is a programmable modem control signal for ASCI channel 0. /DCD0 is multiplexed with the PB2 (parallel Port B, bit 2) on the /DCD0/PB2 pin.

/RTS0. *Request to Send 0 (output, active Low).* This is a programmable modem control signal for ASCI channel 0. This pin is multiplexed with PB0 (parallel Port B, bit 0) on the /RTS0/PB0 pin.

/CTS0. *Clear to Send 0 (input, active Low).* This line is a modem control signal for the ASCI channel 0. This pin is multiplexed with PB1 (parallel Port B, bit 1) on the /CTS0 /PB1 pin.

TxA0. *Transmit Data 0 (output, active High).* This signal is the transmitted data from the ASCI channel 0. This pin is multiplexed with PB3 (parallel Port B, bit 3) on the TxA0/PB3 pin.

TxS. *Clocked Serial Transmit Data (output, active High).* This line is the transmitted data from the CSIO channel. TxS is multiplexed with the ESCC signal (/DTR//REQB) and the 16550 MIMIC interface signal HINTR on the TxS//DTR //REQB//HINTR pin.

RxA0. *Receive Data 0 (input, active High).* This signal is the receive data to ASCI channel 0. This pin is multiplexed with PB4 (parallel Port B, bit 4) on the RxA0/PB4.

RxS. *Clocked Serial Receive Data (input, active High).* This line is the receive data for the CSIO channel. RxS is multiplexed with the /CTS1 signal for ASCI channel 1 and with PB7 (parallel Port B, bit 7) on the RxS//CTS1/PB7 pin.

RxA1. *Received Data ASCI channel 1 (input, active High).* This pin is multiplexed with PB6 (parallel Port B, bit 6) on the RxA1/PB6 pin.

TxA1. *Transmitted Data ASCI Channel 1 (output, active High).* This pin is multiplexed with PB5 (parallel Port B, bit 5) on the TxA1/PB5 pin.

Z180 MPU DMA SIGNALS

/TEND0. *Transfer End 0 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND0 is multiplexed with CKA1 on the CKA1//TEND0 pin.

/TEND1. *Transfer End 1 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND1 is multiplexed with the ESCC signal /RTSB and the 16550 MIMIC interface signal /HRxRDY on the /TEND1//RTSB//HRxRDY pin.

/DREQ0. *DMA request 0 (input, active Low).* /DREQ0 is used to request a DMA transfer from DMA channel 0. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed. /DREQ0 is multiplexed with CKA0 on the CKA0//DREQ0 pin.

/DREQ1. *DMA request 1 (input, active Low).* /DREQ1 is used to request a DMA transfer from DMA channel 1. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed.

Z180 MPU TIMER SIGNALS

T_{OUT}. *Timer Out (output, active High).* T_{OUT} is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus on the A18/T_{OUT} pin.

Z85230 ESCC SIGNALS

TxDA. *Transmit Data (output, active High).* This output signal transmits channel A's serial data at standard TTL levels.

TxDB. *Transmit Data (output, active High).* This output signal transmits channel B's serial data at standard TTL levels. In Z80182 mode 1, TxDB is multiplexed with the 16550 MIMIC interface /HDDIS signal on the TxDB//HDDIS pin.

RxDA. *Receive Data (inputs, active High).* These inputs receive channel A's serial data at standard TTL levels.

RxDB. *Receive Data (input, active High).* These inputs receive channel B's serial data at standard TTL levels. In Z80182 mode 1 RxDB is multiplexed with the 16550 MIMIC HA1 input on the RxDB/HA1 pin.

/TRxCA. *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel A program control. /TRxCA may supply the receive clock or the transmit clock in the Input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

/TRxCB. *Transmit/Receive Clock (input or output, active Low).* The functions of this pin is under channel B program control. /TRxCB may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop (DPLL), the crystal oscillator, the baud rate generator, or the transmit clock in the output mode. In Z80182 mode 1 /TRxCB is multiplexed with the 16550 MIMIC interface HA0 input on the /TRxCB/HA0 pin.

/RTxCA. *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel A program control. In channel A, /RTxCA may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCA pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode.

/RTxCB. *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel B program control. In channel B, /RTxCB may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCB pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode. In Z80182 mode 1 the /RTxCB signal is multiplexed with 16550 MIMIC interface HA2 input on the /RTxCB/HA2 pin.

Z85230 ESCC SIGNALS (Continued)

/SYNCA, /SYNCB. *Synchronization (inputs/outputs, active Low).* These pins can act as either inputs, outputs, or as part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to /CTS and /DCD. In this mode, transitions on these lines affect the state of the Sync /Hunt status bits in Read Register 0, but have no other function. /SYNCA is also multiplexed with PC4 (parallel Port C, bit 4) on the /SYNCA/PC4 pin.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode /SYNC must be driven Low two receive clock cycles after the last bit in the sync character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of /SYNC.

In the Internal Synchronization mode, (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync character is recognized (regardless of the character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag. In Z80182 mode 1 the /SYNCB signal is multiplexed with the 16550 MIMIC interface /HCS input on the /SYNCB //HCS pin.

/CTSA. *Clear To Send (input, active Low).* If this pin is programmed as auto enables, a Low on this input enables the channel A transmitter. If not programmed as auto enables, it may be used as a general-purpose input. The input is Schmitt-trigger buffered to accommodate slow rise-time input. The ESCC™ detects transitions on this input and can interrupt the Z180™ MPU on either logic level transitions. /CTSA is multiplexed with PC1 (parallel Port C, bit 1) on the /CTSA/PC1 pin.

/CTSB. *Clear To Send (input, active Low).* This pin is similar to /CTSA's functionality but is applicable to the channel B transmitter. In Z80182 mode, the /CTSB signal is multiplexed with the 16550 MIMIC interface /HWR input on the /CTSB //HWR pin.

/DCDA. *Data Carrier Detect (input, active Low).* This pin functions as receiver enables if it is programmed as an auto enable bit; otherwise, it may be used as general-purpose input pin. The pin is Schmitt-trigger buffered to accommodate slow rise-time signals. The ESCC detects transitions on this pin and can interrupt the Z180 MPU on either logic level transitions. /DCDA is also multiplexed with PC0 (parallel Port C, bit 0) on the /DCDA/PC0 pin.

/DCDB. *Data Carrier Detect (input, active Low).* This pin's functionality is similar to /DCDA but applicable to the channel B receiver. In Z80182 mode 1, /DCDB is multiplexed with the 16550 MIMIC interface /HRD input on the /DCDB/ /HRD pin.

/RTSA. *Request to Send (output, active Low).* When the Request to Send (RTS) bit in Write Register 5 channel A is set, the /RTSA signal goes Low. When the RTS bit is reset in the Asynchronous mode and auto enables is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with auto enables off, the /RTSA pin strictly follows the state of the RTS bit. The pin can be used as general-purpose output. /RTSA is multiplexed with PC2 (parallel Port C bit 2). This /RTSA or PC2 combination is pin multiplexed with /MWR (active when both the internal /MREQ and /WR are active) on the /MWR/PC2//RTSA pin. The default function of this pin on power-up is /MWR which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

/RTSB. *Request to Send (output, active Low).* This pin is similar in functionality as /RTSA but is applicable on channel B. The /RTSB signal is multiplexed with the Z180 MPU /TEND1 signal and the 16550 MIMIC interface /HRxRDY signal on the /TEND1//RTSB//HRxRDY pin.

/DTR//REQA. *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. /DTR//REQA is also multiplexed with PC3 (parallel Port C, bit 3) on the /DTR//REQA /PC3 pin.

/DTR//REQB. *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. The /DTR//REQB signal is multiplexed with the Z180 MPU TxS signal and the 16550 MIMIC interface HINTR signal on the /TxS//DTR//REQB //HINTR pin.

/W//REQA. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This dual-purpose output can be programmed as Request (receive) lines for a DMA controller or as Wait lines to synchronize the Z180 MPU to the ESCC data rate. The reset state is Wait. The ESCC allows full duplex DMA transfers. /W//REQA is also multiplexed with PC5 (parallel Port C, bit 5) on the /W//REQA/PC5 pin.

/W//REQB. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This pin is similar in functionality as /W//REQA but is applicable on channel B. The /W//REQB signal is multiplexed with the Z180 MPU CKS signal and the 16550 MIMIC interface /HTxRDY signal on the CKS//W//REQB//HTxRDY pin.

16550 MIMIC INTERFACE SIGNALS

HD7-HD0. *Host Data Bus (input/output, tri-state).* In Z80182 mode 1, the host data bus is used to communicate between the 16550 MIMIC interface and the PC/XT/AT. It is multiplexed with the PA7-PA0 of parallel Port A when the Z80182 is in mode 0.

/HDDIS. *Host Driver Disable (output, active Low).* In Z80182 mode 1, this signal goes Low when ever the PC/XT/AT is reading data from the 16550 MIMIC interface. In Z80182 mode 0, this pin is multiplexed with the ESCC™ TxDB signal on the TxDB//HDDIS pin.

HA2-HA0. *Host Address (input).* In Z80182 mode 1, these pins are the address inputs to the 16550 MIMIC interface. This address determines which register the PC/XT/AT accesses. HA0 is multiplexed with /TRxCB on the /TRxCB/HA0 pin; HA1 is multiplexed with RxDB on the RxDB/HA1 pin; HA2 is multiplexed with /RTxCB on the /RTxCB/HA2 pin.

/HCS. *Host Chip Select (input, active Low).* In Z80182 mode 1, this input is used by the PC/XT/AT to select the 16550 MIMIC interface for an access. In Z80182 mode 0, it is multiplexed with the ESCC /SYNCB signal on the SYNCB//HCS pin.

/HWR. *Host Write (Input, active Low).* In Z80182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a write operation is taking place. In Z80182 mode 0, this input is multiplexed with the ESCC /CTSB signal on the /CTSB//HWR pin.

/HRD. *Host Read (input, active Low).* In Z80182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a read operation is taking place. In Z80182 mode 0, this pin is multiplexed with the ESCC /DCDB signal on the /DCDB//HRD pin.

HINTR. *Host Interrupt (output, active High).* In Z80182 mode 1, this output is used by the 16550 MIMIC interface to signal the PC/XT/AT that an interrupt is pending. In Z80182 mode 0, this pin is multiplexed with the ESCC (/DTR//REQB) signal and the Z180 MPU TxS signal on the TxS//DTR//REQB//HINTR pin.

/HTxRDY. *Host Transmit Ready (output, active Low).* In Z80182 mode 1, this output is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that a data byte is ready in the Receive Buffer. In Z80182 mode 0, this pin is multiplexed with the ESCC (/W//REQB) signal and the Z180 MPU CKS signal on the CKS//W//REQB//HTxRDY pin.

/HRxRDY. *Host Receive Ready (output, active Low).* In Z80182 mode 1 this output is used by the 16550 MIMIC interface in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. In Z80182 mode 0, this pin is multiplexed with the ESCC /RTSB signal and the Z180 MPU /TEND1 signal on the /TEND1/RTSB /HRxRDY pin.

PARALLEL PORTS

PA7-PA0. *Parallel Port A (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Z80182 is operated in mode 0. These pins are multiplexed with the HD7-HD0 when the Z80182 is in mode 1.

PB7-PB0. *Parallel Port B (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Port function is selected in the System Configuration register. The pins are multiplexed with the following Z180 peripheral functions:/RTS0,/CTS0,/DCD0, TxA0, RxA0, TxA1, RxA1,(RxS//CTS1).

PC7-PC0. *Parallel Port C (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis for bits PC5-PC0. Bits PC7 and PC6 are input only and read the level of the external /INT2 and /INT1 pins. When /INT2 and/or /INT1 are in edge capture mode writing a '1' to the respective PC7, PC6 bit clears the interrupt capture latch. Writing a '0' has no effect. Bits PC5-PC0 are multiplexed with the following pins from ESCC channel A: (/W//REQA), /SYNCA, (/DTR//REQA), /RTSA,/MWR, /CTSA, /DCDA. The Port function is selected through a bit in the System Configuration Register.

EMULATION SIGNALS

EV1, EV2. *Emulation Select (input).* These two pins determine the emulation mode that the Z180 MPU is in (see Table 1, Evaluation Modes).

Table 1. Evaluation Modes.

	EV1	EV2	
Mode 0	0	0	Normal mode, on chip Z180 bus master
Mode 1	0	1	Emulation Adapter Mode
Mode 2	1	0	Emulator Probe Mode
Mode 3	1	1	Reserved for Test

SYSTEM CONTROL SIGNALS

ST. *Status (output, active High).* This signal is used with the /M1 and /HALT output to decode the status of the CPU machine cycle.

/RESET. *Reset Signal (input, active Low).* /RESET signal is used for initializing the MPU and other devices in the system. It must be kept in the active state for a period of at least three system clock cycles.

IEI. *Interrupt Enable Signal (input, active High).* IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.

IEO. *Interrupt Enable Output Signal (output, active High).* In the daisy-chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is 1 and the CPU is not servicing an interrupt from the on-chip peripherals. This pin is multiplexed with /IOCS on the /IOCS/IEO pin. The /IOCS function is the default on Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

/IOCS. *Auxiliary Chip Select Output Signal (output, active Low).* This pin is multiplexed with /IEO on the /IOCS/IEO pin. /IOCS is an auxiliary chip select that decodes A7,A6, /IORQ, /M1 and effectively decodes the address space xx80H to xxBFH for I/O transactions. A15 through A8 are not decoded so that the chip select is active in all pages of I/O address space. The /IOCS function is the default on the /IOCS/IEO pin after Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

/RAMCS. *RAM Chip Select (output, active Low).* Signal used to access RAM based upon the Address and the RAMLBR and RAMUBR registers.

/ROMCS. *ROM Chip Select (output, active Low).* Signal used to access ROM based upon the address and the ROMBR register.

E. *Enable Clock (output, active High).* Synchronous machine cycle clock output during bus transactions.

XTAL. *Crystal (input, active High).* Crystal oscillator connection. This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics).

EXTAL. *External Clock/Crystal (input, active High).* Crystal oscillator connections to an external clock can be input to the Z80180 on this pin when a crystal is not used. This input is Schmitt triggered.

PHI. *System Clock (output, active High).* The output is used as a reference clock for the MPU and the external system. The frequency of this output is equal to one-half that of the crystal or input clock frequency (in X2 mode).

V_{CC} Power Supply, +5 Volts

V_{SS} Power Supply, 0 Volts

MULTIPLEXED PIN DESCRIPTIONS

A18/T_{OUT}. During Reset, this pin is initialized as an A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, The T_{OUT} function is selected. If TOC1 and TOC0 bits are cleared to 0, the A18 function is selected.

In normal user mode (on-chip bus master), the A18 signal for the chip select logic is obtained from the CPU before the external pin is muxed as A18/T_{OUT}. Therefore, the selection of T_{OUT} will not affect the operation of the 182 chip select logic. However, in adapter mode (off-chip bus master), the A18 signal MUST be provided by the external bus master.

CKA0//DREQ0. During Reset, this pin is initialized as CKA0 pin. If either DM1 or SM1 in the DMA Mode Register (DMODE) is set to 1, /DREQ0 function is always selected.

CKA1//TEND0. During Reset, this pin is initialized as CKA1 pin. If CKA1D bit in the ASCI control register Ch1 (CNTLA1) is set to 1, /TEND0 function is selected. If CKA1D bit is set to 0, CKA1 function is selected.

RxS//CTS1. During Reset, this pin is initialized as the RxS pin. If CST1E bit in the ASCI status register Ch1 (STAT1) is set to 1, /CTS1 function is selected. If CTS1E bit is set to 0, RxS function is selected. This pin is also multiplexed with PB7 based on bit 6 in the System Configuration Register.

The pins below are triple-multiplexed based upon the values of bit 1 and bit 2 of the System Configuration Register. The pins are configured as Table 2 specifies. On Reset, both bits 1 and 2 are zero, so /TEND1,TxS,CKS are selected.

Table 2. Triple Multiplexed Pins

Bit 1	Bit 2	Master Configuration Register
0	0	/TEND1,TxS,CKS
0	1	/RTSB,/DTR//REQB,/W//REQB
1	0	/TEND1,TxS,CKS
1	1	/HRxRDY,//HTxRDY,HINTR

The pins below are multiplexed based upon the value of bit 1 of the System Configuration register. If bit 1 is a zero, then the Z80182 Mode 0 (non-16550 MIMIC mode) signals are selected; if bit 1 is a 1, then Z80182 Mode 1 (16550 MIMIC mode) signals are selected. On Reset, Z80182 Mode 0 is always selected as shown in Table 3.

Table 3. Mode 0 and Mode 1 Multiplexed Pins

Z80182 Mode 0	Z80182 Mode 1
TxDB	/HDDIS
RxDB	HA1
/TRxCB	HA0
/RTxCB	HA2
/SYNCB	/HCS
/CTSB	/HWR
/DCDB	/HRD
PA7-PA0	HD7-HD0

Ports B and C Multiplexed Pin Descriptions

Ports B and C are pin multiplexed with the Z180 ASCI functions and part of ESCC channel A. The MUX function is controlled by bits 7-5 in the System Configuration Register. The MUX scheme works as shown by the Table 4.

Table 4. Multiplexed Port Pins

Port Mode Function		ASCI/ESCC Mode Function
PB7		RxS,/CTS1
PB6	Select with bit 6=1	RxA1
PB5	System Config Reg.	TxA1
PB4		RxA0
PB3		TxA0
PB2	Select with bit 5=1	/DCD0
PB1	System Config Reg.	/CTS0 (see note 1)
PB0		/RTS0
PC7		Always Reads /INT2 Ext. Status
PC6		Always Reads /INT1 Ext. Status
PC5		/W//REQA
PC4		/SYNCA
PC3	Select with bit 7=1	/DTR//REQA
PC2	System Config Reg.	/RTSA (see note 2)
PC1		/CTSA
PC0		/DCDA

Note 1:
When the Port function (PB1) is selected the internal Z180/CTS0 is always driven Low. This ensures that the ASCI channel 0 of the Z180™ MPU is enabled to transmit data.

Note 2:
Interrupt Edge /Pin MUX register, bit 3 chooses between the /MWR or PC2//RTSA combination; the System Configuration Register bit 7 chooses between PC2 and /RTSA.

Refer to Table 5 for the 1st, 2nd and 3rd pin functionalities.

Table 5. Primary, Secondary and Tertiary Pin Functions

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
1	4	ST			
2	5	A0			
3	6	A1			
4	7	A2			
5	8	A3			
6	9	A4			
7	10	A5			
8	11	A6			
9	12	A7			
10	13	A8			
11	14	A9			
12	15	A10			
13	16	A11			
14	17	A12			
15	18	V_{SS}			
16	19	A13			
17	20	A14			
18	21	A15			
19	22	A16			
20	23	A17			
21	24	A18/T_{OUT}			
22	25	V_{DD}			
23	26	A19			
24	27	D0			
25	28	D1			
26	29	D2			
27	30	D3			
28	31	D4			
29	32	D5			
30	33	D6			
31	34	D7			
32	35	/RTS0	PB0		SYS CONF REG Bit 5
33	36	/CTS0	PB1		SYS CONF REG Bit 5
34	37	/DCD0	PB2		SYS CONF REG Bit 5
35	38	TxA0	PB3		SYS CONF REG Bit 5
36	39	RxA0	PB4		SYS CONF REG Bit 5
37	40	TxA1	PB5		SYS CONF REG Bit 6
38	41	RxA1	PB6		SYS CONF REG Bit 6
39	42	RxS//CTS1	PB7		SYS CONF REG Bit 6
40	43	CKA0//DREQ0			

MULTIPLEXED PIN DESCRIPTIONS (Continued)

Table 5. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
41	44	V_{SS}			
42	45	CKA1//TEND0			
43	46	TxS	/DTR//REQB	HINTR	SYS CONF REG Bit 1,2
44	47	CKS	/W//REQB	/HTxRDY	SYS CONF REG Bit 1,2
45	48	/DREQ1			
46	49	V_{DD}			
47	50	/TEND1	/RTSB	/HRxRDY	SYS CONF REG Bit 1,2
48	51	/RAMCS			
49	52	/ROMCS			
50	53	EV1			
51	54	EV2			
52	55	PA0	HD0		SYS CONF REG Bit 1
53	56	PA1	HD1		SYS CONF REG Bit 1
54	57	PA2	HD2		SYS CONF REG Bit 1
55	58	PA3	HD3		SYS CONF REG Bit 1
56	59	PA4	HD4		SYS CONF REG Bit 1
57	60	PA5	HD5		SYS CONF REG Bit 1
58	61	PA6	HD6		SYS CONF REG Bit 1
59	62	PA7	HD7		SYS CONF REG Bit 1
60	63	/W//REQA	PC5		SYS CONF REG Bit 7
61	64	/DTR//REQA	PC3		SYS CONF REG Bit 7
62	65	/MWR	PC2	RTSA	SYS CONF REG Bit 7 *
63	66	/CTSA	PC1		SYS CONF REG Bit 7
64	67	/DCDA	PC0		SYS CONF REG Bit 7
65	68	/SYNCA	PC4		SYS CONF REG Bit 7
66	69	/RTxCA			
67	70	V_{SS}			
68	71	/IOCS	IEO		INT EDG/PIN REG Bit 2
69	72	IEI			
70	73	V_{DD}			
71	74	RxDA			
72	75	/TRxCA			
73	76	TxDA			
74	77	/DCDB	/HRD		SYS CONF REG Bit 1
75	78	/CTSB	/HWR		SYS CONF REG Bit 1
76	79	TxDB	/HDDIS		SYS CONF REG Bit 1
77	80	/TRxCB	HA0		SYS CONF REG Bit 1
78	81	RxDB	HA1		SYS CONF REG Bit 1
79	82	/RTxCB	HA2		SYS CONF REG Bit 1
80	83	/SYNCB	/HCS		SYS CONF REG Bit 1

Table 5. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
81	84	/HALT			
82	85	/RFSH			
83	86	/IORQ			
84	87	/MRD	/MREQ		INT EDG/PIN REG Bit 3
85	88	E			
86	89	/M1			
87	90	/WR			
88	91	/RD			
89	92	PHI			
90	93	V_{SS}			
91	94	XTAL			
92	95	EXTAL			
93	96	/WAIT			
94	97	/BUSACK			
95	98	/BUSREQ			
96	99	/RESET			
97	100	/NMI			
98	1	/INT0			
99	2	/INT1	PC6**		
100	3	/INT2	PC7**		

* Also controlled by Interrupt Edge/Pin MUX Register
** PC7 and PC6 are inputs only and can read values of /INT1 and /INT2.

Z80182 FUNCTIONAL DESCRIPTION

Functionally, the on-chip Z182 MPU and ESCC™ are the same as the discrete devices (Figure 1). Therefore, for a detailed description of each individual unit, refer to the Product Specification/Technical Manuals of each discrete product. The following subsections describe each of the individual units of the Z182.

Z182 MPU FUNCTIONAL DESCRIPTION

This unit provides all the capabilities and pins of the Zilog Z8S180 MPU (Static Z80180 MPU). Figure 4 shows the Z182 MPU Block Diagram. This allows 100% software compatibility with existing Z180™ (and Z80®) software. The following is an overview of the major functional units of the Z182.

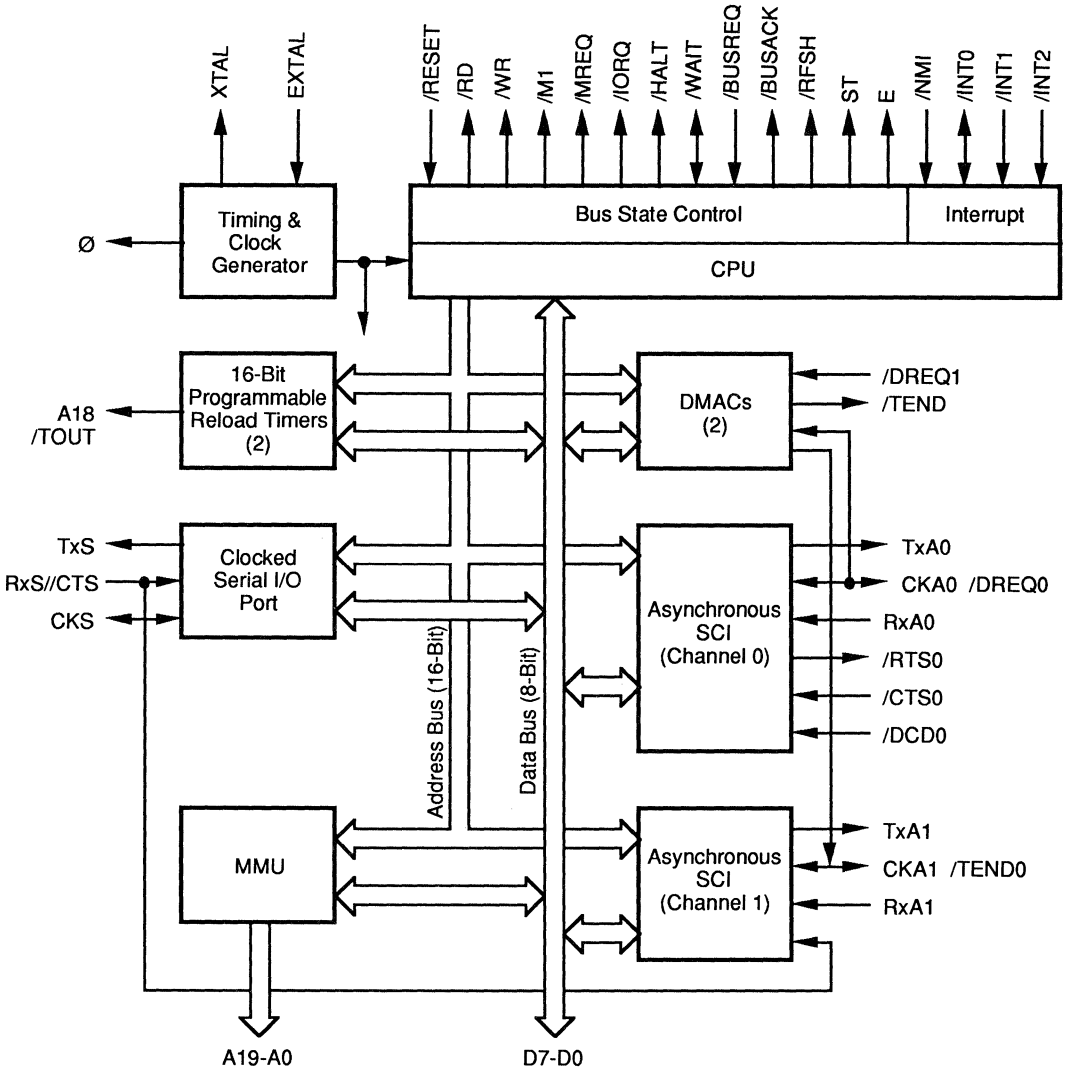


Figure 4. Z182 MPU Block Diagram

Z182 CPU

The Z182 CPU has 100% software compatibility with the Z80® CPU. In addition, the Z182 CPU has the following features:

Faster execution speed. The Z182 CPU is "fine tuned," making execution speed, on average, 10% to 20% faster than the Z80 CPU.

Enhanced DRAM Refresh Circuit. Z182 CPU's DRAM refresh circuit does periodic refresh and generates an 8-bit refresh address. It can be disabled or the refresh period adjusted, via software control.

Enhanced Instruction Set. The Z182 CPU has seven additional instructions to those of the Z80 CPU, which include the MLT (Multiply) instruction.

HALT and Low Power Modes of Operation. The Z182 CPU has HALT and Low Power modes of operation, which are ideal for the applications requiring low power consumption like battery operated portable terminals.

System Stop Mode. When the Z182 is in System Stop mode, it is only the Z182 MPU that is in STOP mode.

Standby and Idle Mode. Please refer to the Z8S180 Datasheet for additional information on these two additional Low Power modes.

Instruction Set. The instruction set of the Z182 CPU is identical to the Z180. For more details about each transaction, please refer to the Data Sheet/Technical Manual for the Z180/Z80 CPU.

Z182 CPU Basic Operation

Z182 CPU's basic operation consists of the following events. These are identical to the Z180 MPU. For more details about each operation, please refer to the Data Sheet/Technical manual for the Z180.

- Operation Code Fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus Request/Acknowledge operation
- Maskable Interrupt Request operation
- Trap and Non-Maskable Interrupt Request operation
- HALT and Low Power modes of operation
- Reset operation

Memory Management Unit (MMU)

The Memory Management Unit (MMU) allows the user to map the memory used by the CPU (64 Kbytes of logical addressing space) into 1 Mbyte of physical addressing space. The organization of the MMU allows object code compatibility with the Z80 CPU while offering access to an extended memory space. This is accomplished by using an effective common area-banked area scheme.

DMA Controller

The Z182 MPU has two DMA controllers. Each DMA controller provides high-speed data transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory-to/from-I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. The DMA can access the full 1 Mbytes addressing range with a block length up to 64 Kbytes and can cross over 64K boundaries.

Asynchronous Serial Communication Interface (ASCI)

This unit provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels also support a multiprocessor communication format.

Programmable Reload Timer (PRT)

The Z182 MPU has two separate Programmable Reload Timers, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is system clock divided by 20. PRT channel 1 provides an optional output to allow for waveform generation.

Clocked Serial I/O (CSI/O)

The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another CPU or MPU.

Programmable Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z182 MPU unit has a programmable wait state generator. By programming the DMA/WAIT Control Register (DCNTL), up to three wait states are automatically inserted in memory and I/O cycles. This unit also inserts wait states during on-chip DMA transactions.

Z85230 ESCC™ FUNCTIONAL DESCRIPTION

The Zilog Enhanced Serial Communication Controller ESCC™ is a dual channel, multiprotocol data communication peripheral. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem control in both channels in applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (number of the registers varies depending on the version), the user can configure the ESCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements. The ESCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the ESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The ESCC (Enhanced SCC) is pin and software compatible to the CMOS SCC version. The following enhancements were made to the CMOS SCC:

- Deeper Transmit FIFO (4 bytes)
- Deeper Receive FIFO (8 bytes)
- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced High with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers, 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced /DTR, /RTS deactivation timing

The following features are common to both the ESCC and the CMOS SCC:

- Two independent full-duplex channels
- Synchronous/Isochronous data rates:
  - Up to 1/4 of the PCLK using external clock source. Up to 5 Mbits/sec at 20 MHz PCLK (ESCC)

- Asynchronous capabilities
  - 5, 6, 7 or 8 bits/character (capable of handling 4 bits/character or less)
  - 1, 1.5, or 2 stop bits
  - Odd or even parity
  - Times 1, 16, 32 or 64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection

- Byte oriented synchronous capabilities:
  - Internal or external character synchronization
  - One or two sync characters (6 or 8 bits/sync character) in separate registers
  - Automatic Cyclic Redundancy Check (CRC) generation/detection

- SDLC/HDLC capabilities:
  - Abort sequence generation and checking
  - Automatic zero insertion and detection
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - CRC generation/detection
  - SDLC loop mode with EOP recognition/loop entry and exit

- NRZ, NRZI or FM encoding/decoding. Manchester code decoding (encoding with external logic).

- Baud Rate Generator in each channel

- Digital Phase-Locked Loop (DPLL) for clock recovery

- Crystal oscillator

BLOCK DIAGRAM

Figure 5 has the block diagram of the ESCC™. Please refer to the ESCC Technical Manual for further details.

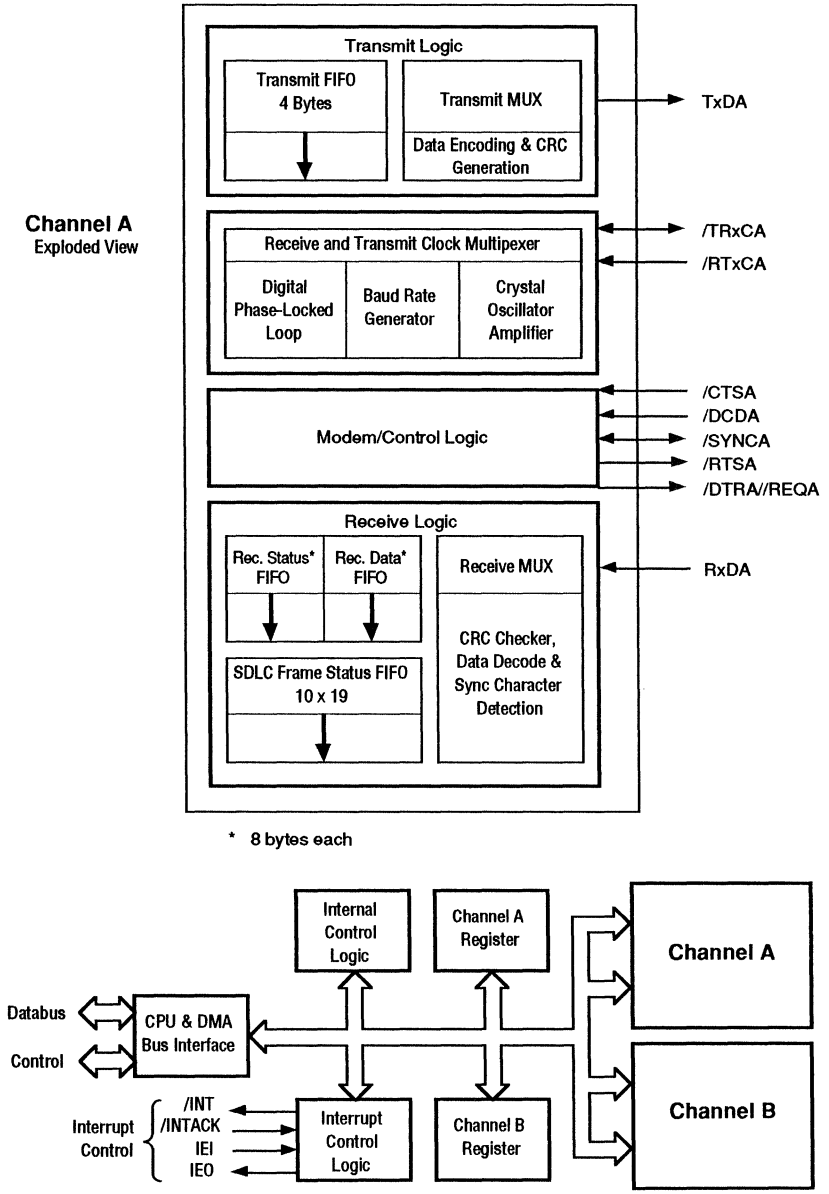


Figure 5. ESCC Block Diagram

16550 MIMIC INTERFACE FUNCTIONAL DESCRIPTION

The Z80182 has a 16550 MIMIC interface that allows it to MIMIC the 16550 device. It has all the interface pins necessary to connect to the PC/XT/AT bus without any extra circuitry. It contains the complete register set of the part with the same interrupt structure. The data path allows parallel transfer of data to and from the register set by the internal Z80180 of the Z80182. There is no shift register associated with the MIMIC of the 16550 UART. This interface saves the application from doing a serial transfer before performing data compression or error correction on the data.

Control of the register set is maintained by six priority encoded interrupts to the Z80182. When the PC/XT/AT writes to THR, MCR, LCR, DLL, DLM, FCR or reads the RBR, an interrupt to the Z80182 is generated. Each interrupt can be individually masked off or all interrupts can be disabled by writing a single bit. Both mode 0 and mode 2 interrupts are supported by the 16550 MIMIC interface.

Two eight-bit timers are also available to control the data transfer rate of the 16550 MIMIC interface. Their input is tied to the ESCC channel B divide clock, so a down count of 24 bits is possible. An additional two eight bit timers are available for programming the FIFO timeout feature (Four Character Time Emulation) for both Receiver and Transmit FIFO's.

The 16550 MIMIC interface supports the PC/XT/AT interrupt structure as well as an addition mode that allows for a wired Logic AND interrupt structure.

The 16550 MIMIC interface is also capable of high speed parallel DMA transfers by using two control lines and the transmit and receive registers of the 16550 MIMIC interface.

All registers of the 16550 MIMIC interface are accessible in any page of I/O space since only the lowest eight address lines are decoded. See Figure 6 for a block diagram of the 16550 MIMIC interface.

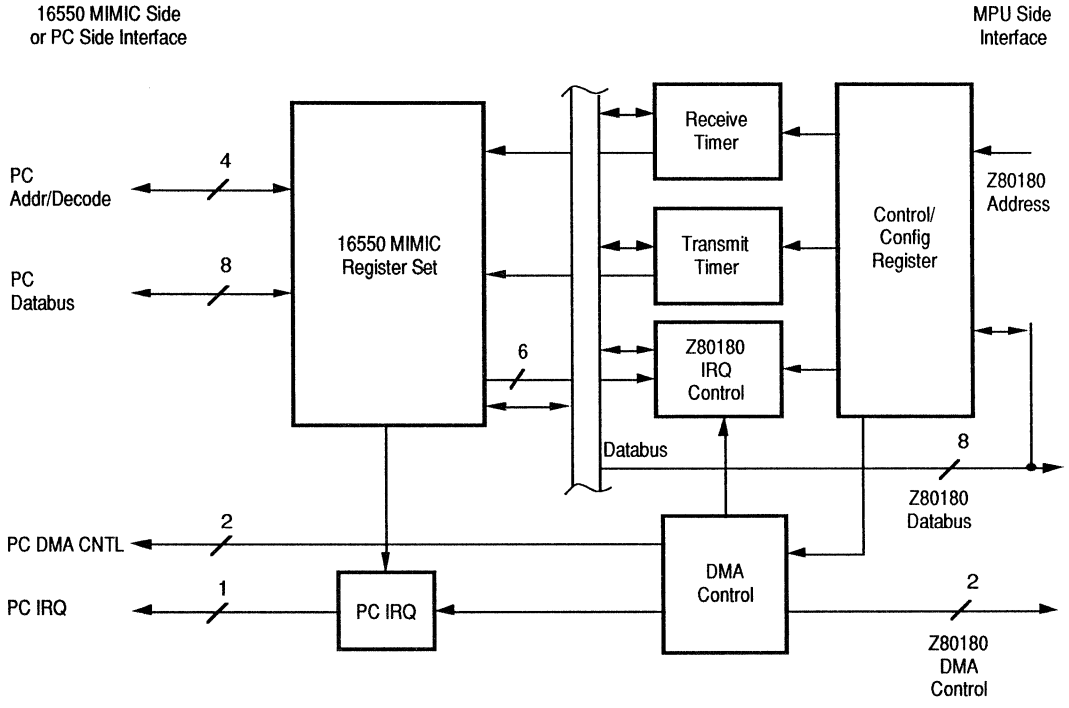


Figure 6. 16550 MIMIC Block Diagram

16550 MIMIC FIFO DESCRIPTION

The receiver FIFO consists of a 16-word FIFO capable of storing eight data bits and three error bits for each character stored (Figure 7). Parity error, Framing error and Break detect bits are stored along with the data bits by copying their value from three shadow bits that are write only bits for the Z80180 MPU LSR address. The three shadow bits are cleared after they are copied to the FIFO memory. In FIFO mode, to write error bits into the receive FIFO, the MPU must first write the Parity, Framing and Break detect status to the Line Status Register (shadow bits) and then write the character associated into the receiver buffer. The data and error bits will then move into the same address in the FIFO.

The error bits become available to the PC side of the interface when that particular location becomes the next address to read (top of FIFO). At that time, they may either be read by the PC by accessing them in the LSR, or they may cause an interrupt to the PC interface if so enabled. The error bits are set by the error status of the byte at the top of the FIFO, but may only be cleared by reading the LSR. If successive reads of the receiver FIFO are performed without reading the LSR, the status bits will be set if any of the bytes read have the respective error bit set. See Table 6 for the setting and clearing of the Line Status Register bits.

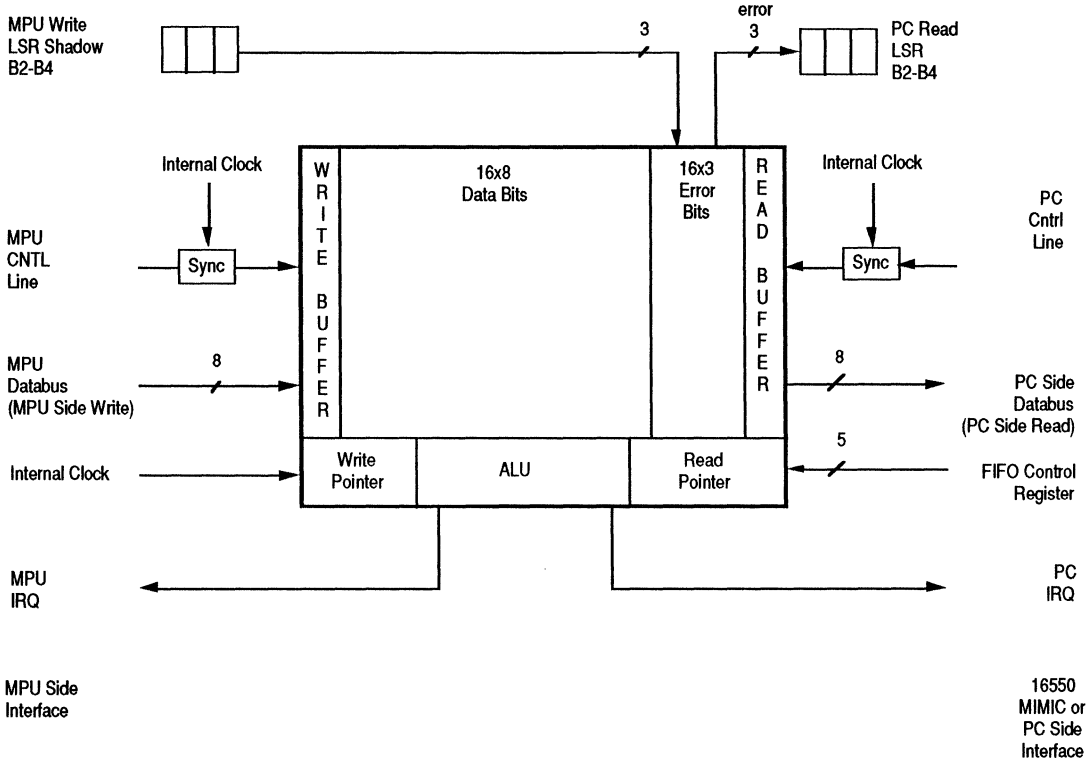


Figure 7. 16550 MIMIC Receiver FIFO Block Diagram

Table 6. 16550 Line Status Register

Error	Description	How to Set	How to Clear
Error in RCVR FIFO	At least one data byte available in FIFO with one error	At least one error in receiver FIFO	When there are no more errors
TEMT	Transmitter empty	MPU writes a "1"	MPU writes a "0"
THRE	Transmitter holding register is empty	When MPU has read or emptied the holding register	When holding register is not empty
Break Detect	Break occurs when received data input is held in logic-0 for longer than a full word transmission	MPU writes "1"	There is a PC-side read of the LSR
Framing Error	Received character did not have a valid stop bit	MPU writes "1"	There is a PC-side read of the LSR
Parity Error	Received character did not have correct even or odd parity	MPU writes "1"	There is a PC-side read of the LSR
Overrun Error	Overlapping received characters, thereby destroying the previous character	MPU makes two writes to receiver buffer register	There is a PC-side read of the LSR
Data Ready	Indicates complete incoming data has been received	MPU writes to RCVR FIFO or receiver buffer register	There is a PC-side read of data

16550 MIMIC FIFO DESCRIPTION (Continued)

The PC interface may be interrupted when 1, 4, 8 or 14 bytes are available in the receive FIFO by setting bits 6 and 7 in the FCR (FIFO Control Register, PC address 02H) to the appropriate trigger value. If the FIFO is not empty, but below the above trigger value, a timeout interrupt is available if the receiver FIFO is not written by the MPU or read by the PC from an interval determined by the Character Timeout Timer. This is an additional Timer with MPU access only that is used to emulate the 16550 4 character timeout delay. The timer receives the ESCC /TRxCB as its input clock. Software must determine the correct values to program into the Receiver Timeout register and the SCC TRxCB to achieve the correct delay interval for timeout. These interrupts are cleared by the FIFO reaching the trigger point or by resetting the Timeout Interval Timer by FIFO MPU write or PC read access.

With FIFO mode enabled, the MPU is interrupted when the receive FIFO is empty, corresponding to bit 5 being set in the IUS/IP register (MPU access only). This bit corresponds to a PC read of the receive buffer in non-FIFO (16450) mode. The interrupt source is cleared when the FIFO becomes non-empty or the MPU reads the IUS/IP register.

The transmitter FIFO is a 16-byte FIFO with PC write and MPU read access (Figure 8). In FIFO mode, the PC receives an interrupt when the transmitter becomes empty corresponding to bit 5 being set in the LSR. This bit and the interrupt source are cleared when the transmit FIFO becomes non-empty or the Interrupt Indentification Register (IIR) register is read by the PC.

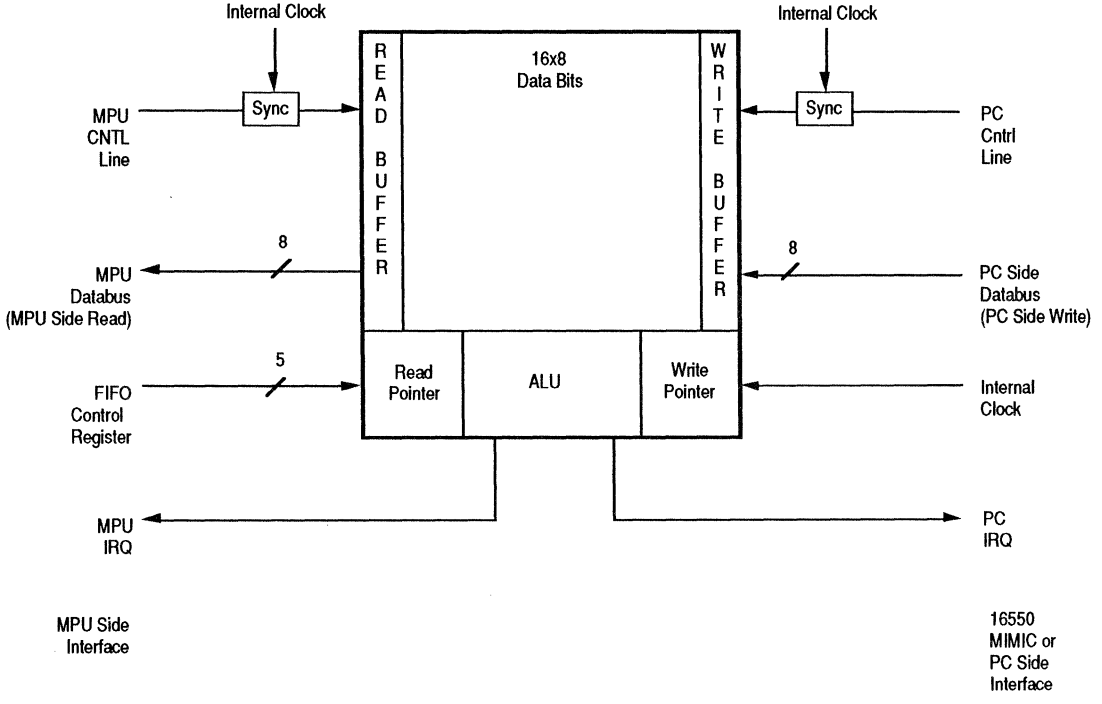


Figure 8. 16550 MIMIC Transmitter FIFO Block Diagram

On the MPU interface, the transmitted data available can be programmed to interrupt the MPU on 1, 4, 8 or 14 bytes of available data by seeing the appropriate value in the MPU FSCR control register (MPU write only xxECH) bits 6 and 7. A timeout feature exists, Transmit Timeout Timer, which is an additional 8-bit timer with SCC TxRCB as the input source. If the transmitter FIFO is non-empty and no PC write or MPU read of the FIFO has taken place within the timer interval, a timeout occurs causing a corresponding interrupt to the MPU.

Z80182 MIMIC SYNCHRONIZATION CONSIDERATIONS

Because of the asynchronous nature of the FIFO's on the MIMIC, some scheme of synchronization must be provided to prevent conflict from the dual port accesses of the MPU and the PC.

To solve this problem, I/O to the FIFO is buffered and the buffers allow both PC and MPU to access the FIFO asynchronously. Read and Write requests are then synchronized by means of the MPU clock. Incoming signals are buffered in such a way that meta-stable input levels are stabilized to valid 1 or 0 levels. Actual transfers to and from the buffers, from and to the FIFO memory, are timed by the MPU clock. ALU evaluation is performed on a different phase than the transfer to ensure stable pointer values.

Another potential problem is that of simultaneous access of the MPU and PC to any of the various 'mailbox' type registers. This is solved by dual buffering of the various read/write registers. During a read access by either the MPU or PC to a mailbox register, the data in the output or slave portion of the buffered register is not permitted to change. Any write that might take place during this time will be stored in the input of master part of the register. The corresponding status/interrupt is reset appropriately based on the write having followed the read to the register. For example, the IUS/IP bit for the LCR write will not be cleared by the MPU read of the LCR if a simultaneous write to the LCR by the PC takes place. Instead the LSR data will change after the read access and IUS/IP bit 3 remains at logic 1.

PARALLEL PORTS FUNCTIONAL DESCRIPTION

The Z80182 has three eight bit bi-directional Ports. Each bit is individually programmable for input or output (with the exception of PC6 and PC7 which are inputs only). The Ports are controlled via two registers: the Port Direction Control Register and the Port Data Register. (Please see register description for Ports A, B and C).

PROGRAMMING

The following subsections explain and define the parameters for I/O Address assignments. The three tables in this section describe the mapping of the common registers shared by the MPU and the 16550 MIMIC. The MPU address refers to the I/O address as accessed from the MPU side (the Z180™ MPU interface side of the 16550 MIMIC). Note that only the lowest eight address lines are decoded for access. The PC address (coined because the UART is common in PCs) is the address needed to access the MIMIC registers via the MIMIC interface signals. The MIMIC interface signals are multiplexed with the ESCC channel B and the Port A signals, and must be activated via the System Configuration Register and the Interrupt Edge/ Pin MUX Register.

Table 7. Z80182 MPU Registers

Register Name	MPU Addr	PC Addr
Z80182 MPU Control Registers	xx00H to xx3FH (Relocatable to xx40H to xx7FH or xx80H to xxBFH)	None

Note: "xx" indicates don't care condition

Table 8. Z80182 MIMIC Register MAP

Register Name	MPU Addr/Access		PC Addr/Access	
MMC MIMIC Master Control Register	xxFFH	R/W	None	
IUS/IP Interrupt Pending	xxFEH	R/Wb7	None	
IE Interrupt Enable	xxFDH	R/W	None	
IVEC Interrupt Vector	xxFCH	R/W	None	
TTCR Transmit Time Constant	xxFAH	R/W	None	
RTCR Receive Time Constant	xxFBH	R/W	None	
FSCR FIFO Status and Control	xxECH	R/W7-4	None	
RTTC Receive Timeout Time Constant	xxEAH	R/W	None	
TTTC Transmit Timeout Time Constant	xxEBH	R/W	None	
RBR Receive Buffer Register	xxF0H	W only	00H	DLAB=0 R only
THR Transmit Holding Register	xxF0H	R only	00H	DLAB=0 W only
IER Interrupt Enable Register	xxF1H	R only	01H	DLAB=0 R/W
IIR Interrupt Identification	None		02H	R only
FCR FIFO Control Register	xxE9H	R only	02H	W only
LCR Line Control Register	xxF3H	R only	03H	R/W
MCR Modem Control Register	xxF4H	R only	04H	R/W
LSR Line Status Register	xxF5H	R/Wb6432	05H	R only
MSR Modem Status Register	xxF6H	R/Wb7-4	06H	R only
SCR Scratch Register	xxF7H	R only	07H	R/W
DLL Divisor Latch (LSByte)	xxF8H	R only	00H	DLAB=1 R/W
DLM Divisor Latch (MSByte)	xxF9H	R only	01H	DLAB=1 R/W

Table 9. Z80182 ESCC, PIA and MISC Registers

Register Name	MPU Addr/Access		PC Addr/Access
PC Data Direction Register	xxDDH	R/W	None
PC Data Register	xxDEH	R/W	None
Interrupt Edge/Pin MUX Control	xxDFH	R/W	None
ESCC Chan A Control Register	xxE0H	R/W	None
ESCC Chan A Data Register	xxE1H	R/W	None
ESCC Chan B Control Register	xxE2H	R/W	None
ESCC Chan B Data Register	xxE3H	R/W	None
PB Data Direction Register	xxE4H	R/W	None
PB Data Register	xxE5H	R/W	None
RAMUBR RAM Upper Boundary Register	xxE6H	R/W	None
RAMLBR RAM Lower Boundary Register	xxE7H	R/W	None
ROM Address Boundary Register	xxE8H	R/W	None
PA Data Direction Register	xxEDH	R/W	None
PA Data Register	xxEEH	R/W	None
System Configuration Register	xxEFH	R/W	None

Z182 MPU CONTROL REGISTERS

Figures 9 through 49 refer to the Z80182 MPU Control registers. Refer to the Z8S180 Product/Technical Books for details.

ASCI CHANNELS CONTROL REGISTERS

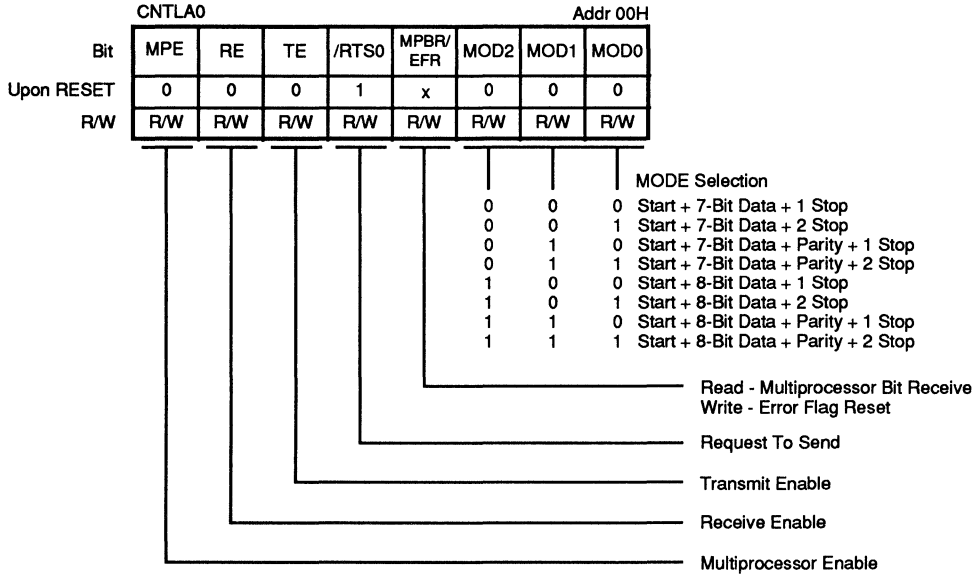


Figure 9. ASCI Control Register A (Ch. 0)

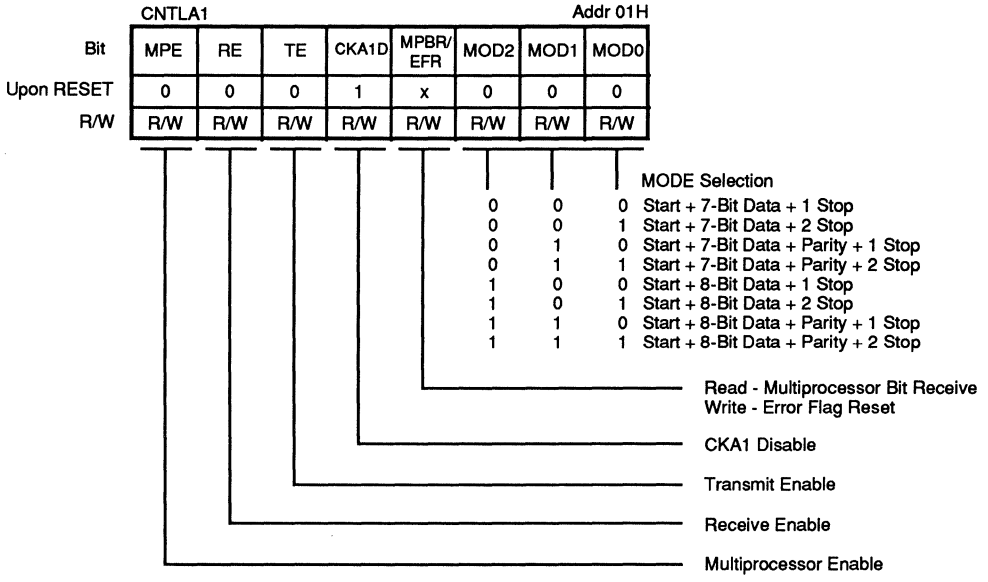
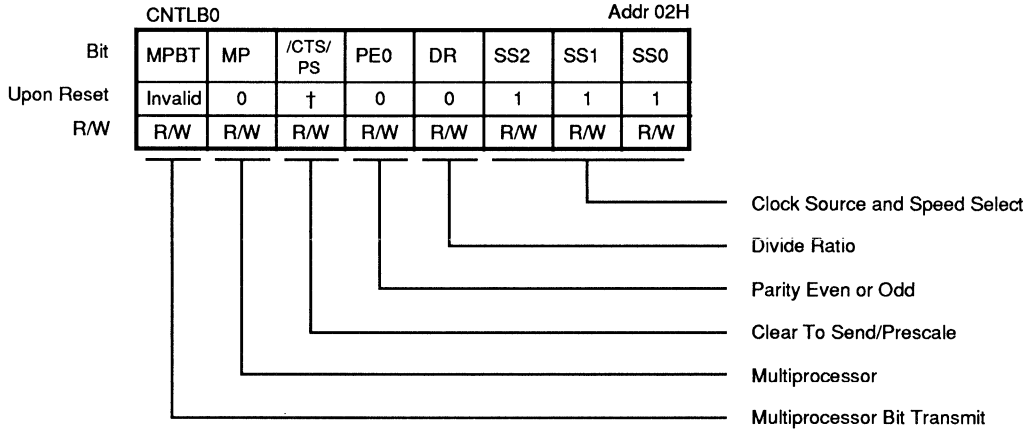


Figure 10. ASCI Control Register A (Ch. 1)

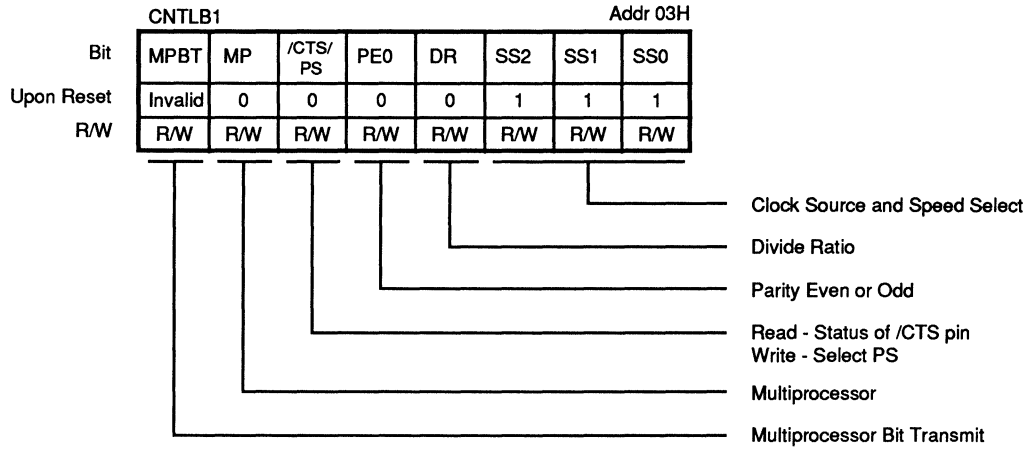


† /CTS - Depending on the condition of /CTS pin.
PS - Cleared to 0.

General Divide Ratio	PS = 0 (Divide Ratio = 10)		PS = 1 (Divide Ratio = 30)	
SS, 2, 1, 0	DR = 0 (x16)	DR = 1 (x64)	DR = 0 (x16)	DR = 1 (x64)
000	Ø ÷ 160	Ø ÷ 640	Ø ÷ 480	Ø ÷ 1920
001	Ø ÷ 320	Ø ÷ 1280	Ø ÷ 960	Ø ÷ 3840
010	Ø ÷ 640	Ø ÷ 2580	Ø ÷ 1920	Ø ÷ 7680
011	Ø ÷ 1280	Ø ÷ 5120	Ø ÷ 3840	Ø ÷ 15360
100	Ø ÷ 2560	Ø ÷ 10240	Ø ÷ 7680	Ø ÷ 30720
101	Ø ÷ 5120	Ø ÷ 20480	Ø ÷ 15360	Ø ÷ 61440
110	Ø ÷ 10240	Ø ÷ 40960	Ø ÷ 30720	Ø ÷ 122880
111	External Clock (Frequency < Ø ÷ 40)			

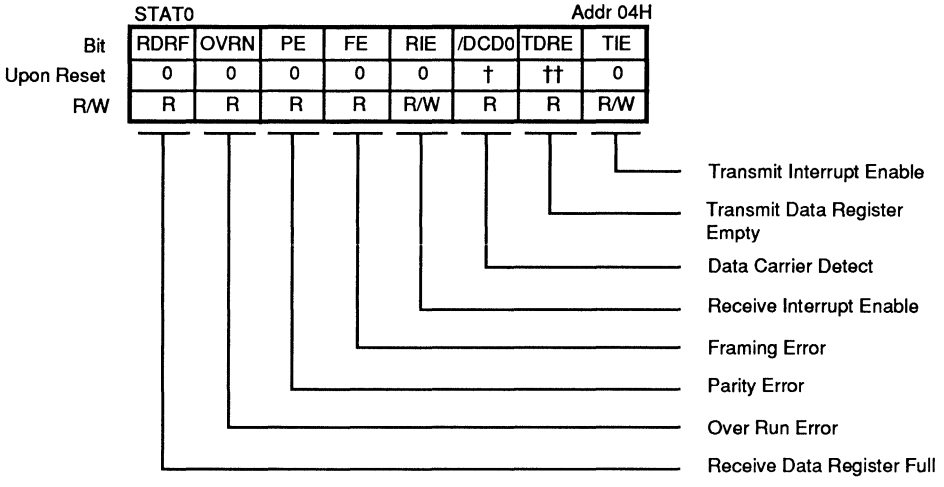
Figure 11. ASCI Control Register B (Ch. 0)

ASCI CHANNELS CONTROL REGISTERS (Continued)



General Divide Ratio SS, 2, 1, 0	PS = 0 (Divide Ratio = 10) DR = 0 (x16)	DR = 1 (x64)	PS = 1 (Divide Ratio = 30) DR = 0 (x16)	DR = 1 (x64)
000	Ø ÷ 160	Ø ÷ 640	Ø ÷ 480	Ø ÷ 1920
001	Ø ÷ 320	Ø ÷ 1280	Ø ÷ 960	Ø ÷ 3840
010	Ø ÷ 640	Ø ÷ 2580	Ø ÷ 1920	Ø ÷ 7680
011	Ø ÷ 1280	Ø ÷ 5120	Ø ÷ 3840	Ø ÷ 15360
100	Ø ÷ 2560	Ø ÷ 10240	Ø ÷ 7680	Ø ÷ 30720
101	Ø ÷ 5120	Ø ÷ 20480	Ø ÷ 15360	Ø ÷ 61440
110	Ø ÷ 10240	Ø ÷ 40960	Ø ÷ 30720	Ø ÷ 122880
111	External Clock (Frequency < Ø ÷ 40)			

Figure 12. ASCI Control Register B (Ch. 1)



† /DCD0 - Depending on the condition of /DCD0 Pin.

†† /CTS0 Pin	TDRE
L	1
H	0

Figure 13. ASCI Status Register

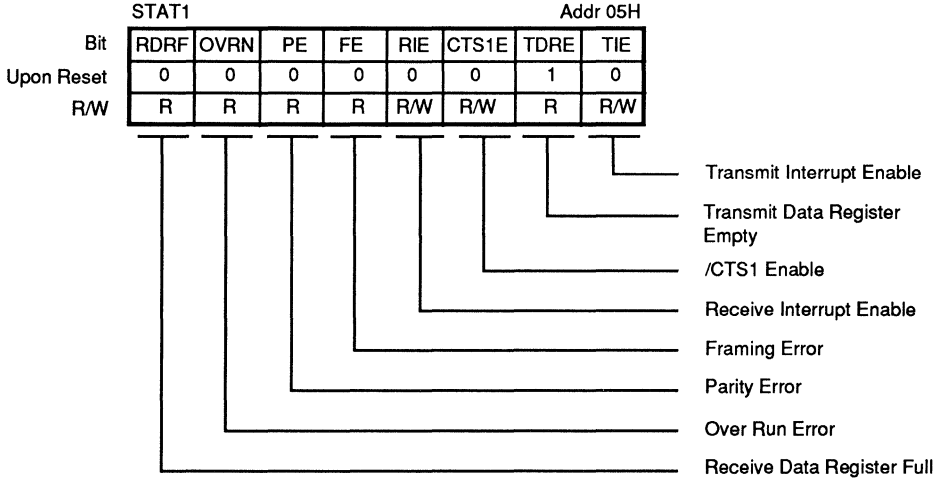


Figure 14. ASCI Status Register (Ch. 1)

ASCI CHANNELS CONTROL REGISTERS (Continued)

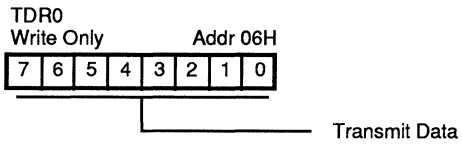


Figure 15. ASCI Transmit Data Register (Ch. 0)

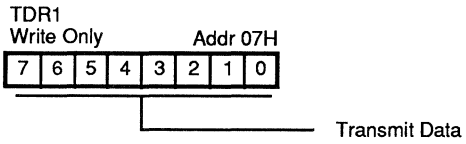


Figure 16. ASCI Transmit Data Register (Ch. 1)

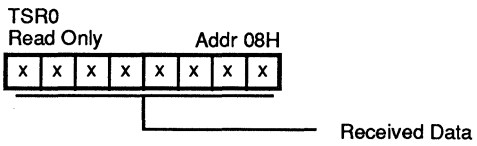


Figure 17. ASCI Receive Data Register (Ch. 0)

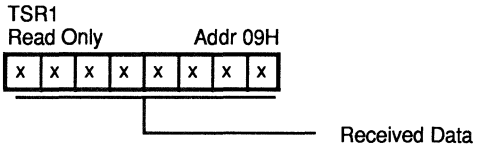
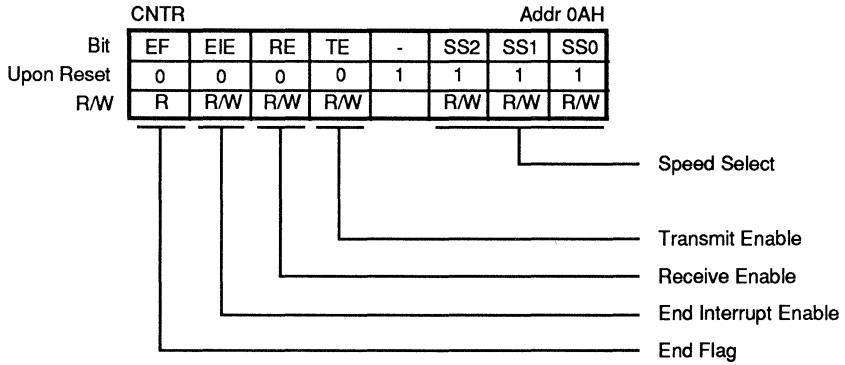


Figure 18. ASCI Receive Data Register (Ch. 1)

CSI/O REGISTERS



SS2, 1, 0	Baud Rate
000	Ø ÷ 20
001	Ø ÷ 40
010	Ø ÷ 80
011	Ø ÷ 100

SS2, 1, 0	Baud Rate
100	Ø ÷ 320
101	Ø ÷ 640
110	Ø ÷ 1280
111	External Clock (Frequency < Ø ÷ 20)

Figure 19. CSI/O Control Register

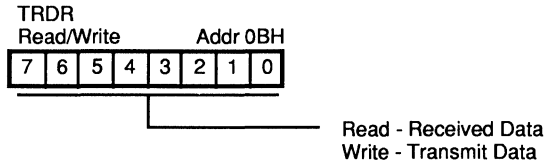


Figure 20. CSI/O Transmit/Receive Data Register

TIMER DATA REGISTERS

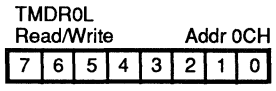
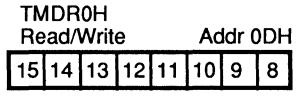


Figure 21. Timer 0 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 23. Timer 0 Data Register H

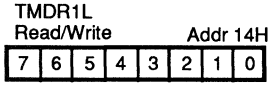
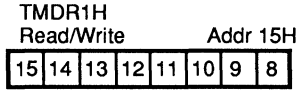


Figure 22. Timer 1 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 24. Timer 1 Data Register H

TIMER RELOAD REGISTERS

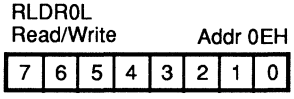


Figure 25. Timer 0 Reload Register L

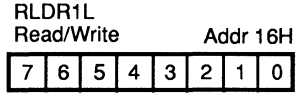


Figure 26. Timer 1 Reload Register L

TIMER RELOAD REGISTERS (Continued)

RLDR0H
Read/Write — Addr 0FH

15	14	13	12	11	10	9	8

Figure 27. Timer 0 Reload Register H

RLDR1H
Read/Write — Addr 17H

15	14	13	12	11	10	9	8

Figure 28. Timer 1 Reload Register H

TIMER CONTROL REGISTER

TCR — Addr 10H

Bit	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0
Upon Reset	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Timer Down Count Enable 1,0
Timer Output Control 1,0
Timer Interrupt Enable 1,0
Timer Interrupt Flag 1,0

TOC1,0	A15/TOUT
00	Inhibited
01	Toggle
10	0
11	1

Figure 29. Timer Control Register

FREE RUNNING COUNTER

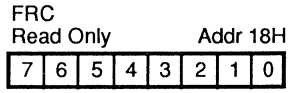


Figure 30. Free Running Counter

CPU CONTROL REGISTER

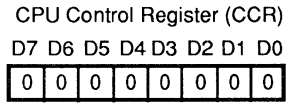
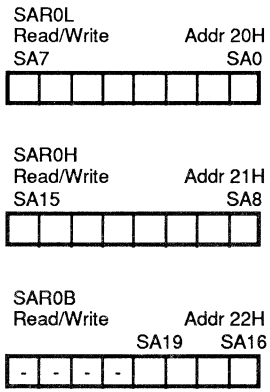


Figure 31. CPU

DMA REGISTERS

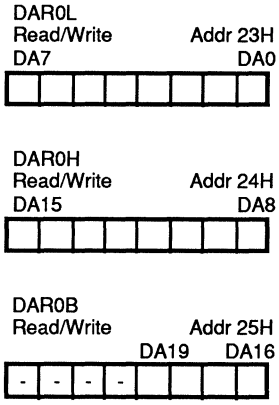


Bits 0-2 (3) are used for SAR0B

A19,	A18,	A17,	A16	DMA Transfer Request
x	x	0	0	/DREQ0 (external)
x	x	0	1	RDR0 (ASCI0)
x	x	1	0	TDR0 (ASCI1)
x	x	1	1	Not Used

Figure 32. DMA 0 Source Address Registers

DMA REGISTERS



Bits 0-2 (3) are used for DAR0B

A19,	A18,	A17,	A16	DMA Transfer Request
x	x	0	0	/DREQ0 (external)
x	x	0	1	RDR0 (ASCI0)
x	x	1	0	TDR0 (ASCI1)
x	x	1	1	Not Used

Figure 33. DMA 0 Destination Address Registers

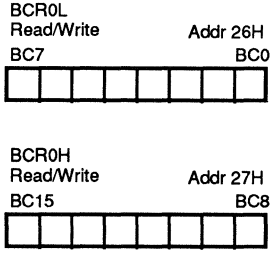


Figure 34. DMA 0 Byte Counter Registers

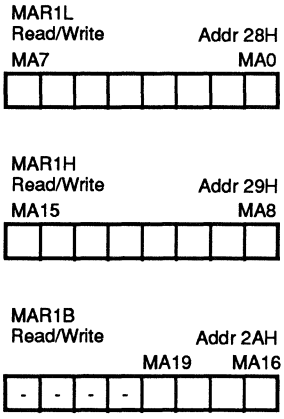


Figure 35. DMA 1 Memory Address Registers

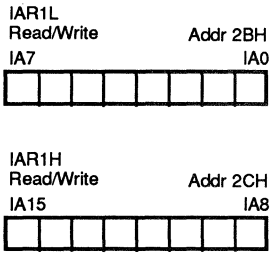


Figure 36. DMA I/O Address Registers

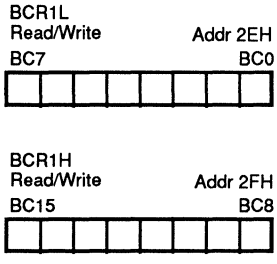


Figure 37. DMA 1 Byte Count Registers

DSTAT — Addr 30H

Bit	DE1	DE0	/DWE1	/DWE0	DIE1	DIE0	-	DIME
Upon Reset	0	0	1	1	0	0	1	0
R/W	R/W	R/W	W	W	R/W	R/W		R

DIME — DMA Master Enable
DIE1, DIE0 — DMA Interrupt Enable 1, 0
/DWE1, /DWE0 — DMA Enable Bit Write Enable 1, 0
DE1, DE0 — DMA Enable Ch 1, 0

Figure 38. DMA Status Register

DMODE — Addr 31H

Bit	-	-	DM1	DM0	SM1	SM0	MMOD	-
Upon Reset	1	1	0	0	0	0	0	1
R/W			R/W	R/W	R/W	R/W	R/W	

MMOD — Memory MODE Select
SM1, SM0 — Ch 0 Source Mode 1, 0
DM1, DM0 — Ch 0 Destination Mode 1, 0

DM1, 0	Destination	Address
00	M	DAR0+1
01	M	DAR0-1
10	M	DAR0 Fixed
11	I/O	DAR0 Fixed

SM1, 0	Source	Address
00	M	SAR0+1
01	M	SAR0-1
10	M	SAR0 Fixed
11	I/O	SAR0 Fixed

MMOD	Mode
0	Cycle Steal Mode
1	Burst Mode

Figure 39. DMA Mode Registers

DCNTL — Addr 32H

Bit	MWI1	MWI0	IWI1	IWI0	DMS1	DMS0	DIM1	DIM0
Upon Reset	1	1	1	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DIM1 — DMA Ch 1 I/O Memory Mode Select

DMS0 — /DREQi Select, i = 1, 0

IWI0 — I/0 Wait Insertion

MWI0 — Memory Wait Insertion

MWI1, 0	No. of Wait States
00	0
01	1
10	2
11	3

IWI1, 0	No. of Wait States
00	0
01	2
10	3
11	4

DMSi	Sense
1	Edge Sense
0	Level Sense

DM1, 0	Transfer Mode	Address Increment/Decrement	
00	M - I/O	MAR1+1	IAR1 Fixed
01	M - I/O	MAR1-1	IAR1 Fixed
10	I/O - M	IAR1 Fixed	MAR1+1
11	I/O - M	IAR1 Fixed	MAR1-1

Figure 40. DMA/WAIT Control Register

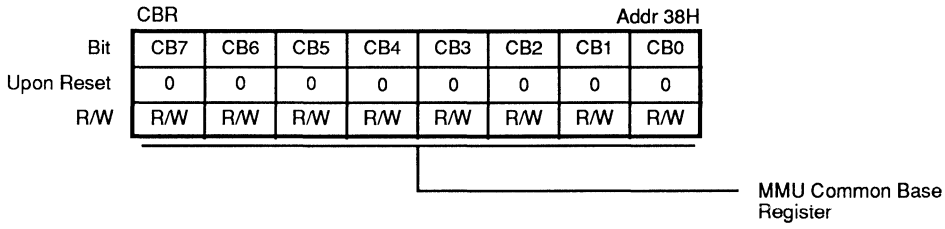


Figure 41. MMU Common Base Register

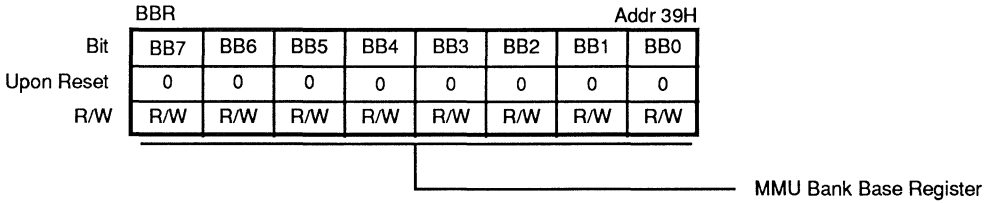


Figure 42. MMU Bank Base Register

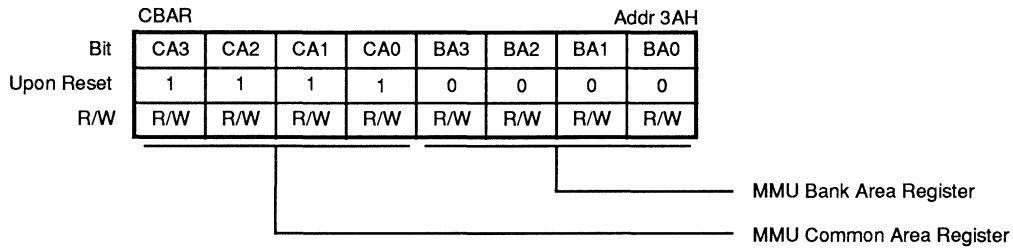


Figure 43. MMU Common/Bank Area Register

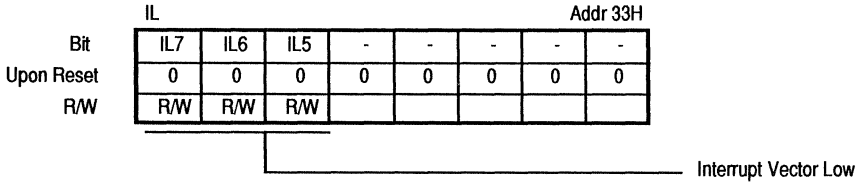


Figure 44. Interrupt Vector Low Register

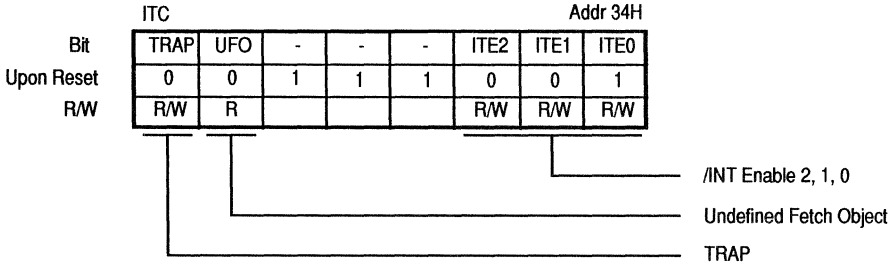
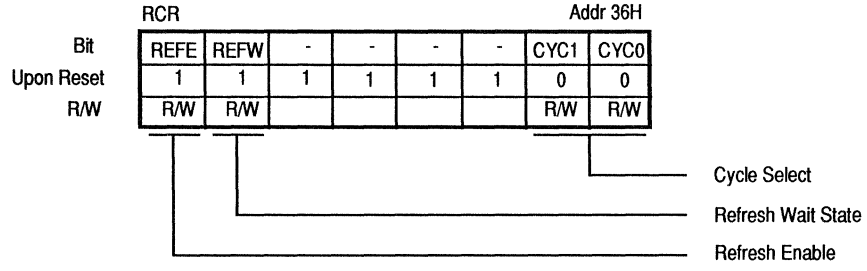
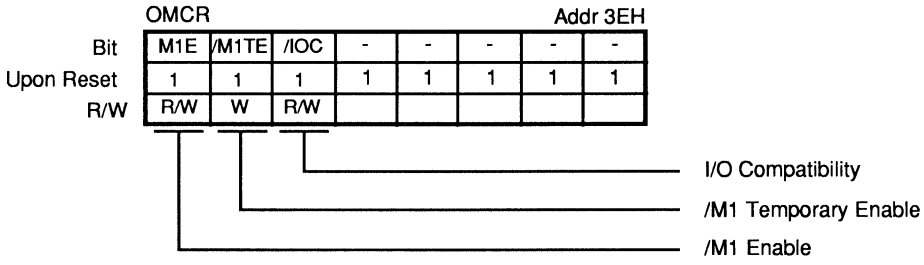


Figure 45. INT/TRAP Control Register



CYC1, 0	Interval of Refresh Cycle
00	10 states
01	20 states
10	40 states
11	80 states

Figure 46. Refresh Control Register



Note: This register has to be programmed to 0x0xxxxxb(x:don't care) as a part of Initialization.

Figure 47. Operation Mode Control Register

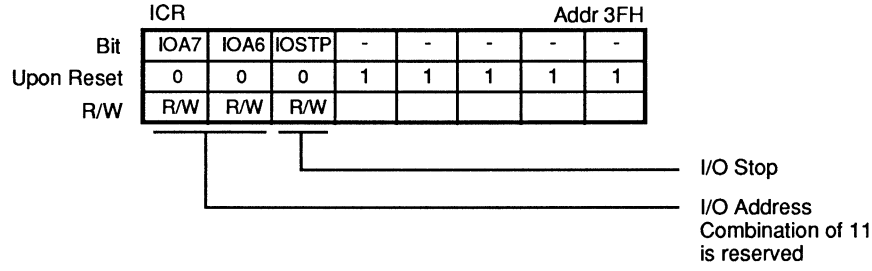


Figure 48. I/O Control Register

ADDITIONAL FEATURES ON THE Z182 MPU

The following is a detailed description of the enhancements to the Z8S180 from the standard Z80180 in the areas of STANDBY, IDLE, and STANDBY-QUICK RECOVERY modes.

Add-On Features

There are five different power-down modes. SLEEP and SYSTEM STOP are inherited from the Z80180. In SLEEP mode, the CPU is in a stopped state while the on-chip I/Os are still operating. In I/O STOP mode, the on-chip I/Os are in a stopped state while leaving the CPU running. In SYSTEM STOP mode, both the CPU and the on-chip I/Os are in the stopped state to reduce the current consumption. The Z8S180 has added two additional power-down modes, STANDBY and IDLE, to reduce the current consumption even further. The differences among these power-down modes are summarized in Table 10.

Table 10. Power Down Modes

Power-Down Modes	CPU Core	On-Chip I/O	OSC.	CLKOUT	Recovery Source	Recovery Time (Minimum)
SLEEP	Stop	Running	Running	Running	RESET, Interrupts	1.5 Clock
I/O STOP	Running	Stop	Running	Running	By Programming	-
SYSTEM STOP	Stop	Stop	Running	Running	RESET, Interrupts	1.5 Clock
IDLE†	Stop	Stop	Running	Stop	RESET, Interrupts, BUSREQ	8 +1.5 Clock
STANDBY†	Stop	Stop	Stop	Stop	RESET, Interrupts, BUSREQ	2^{17} +1.5 Clock (Normal Recovery) 2^{6} +1.5 Clock (Quick Recovery)

Notes:
† IDLE and STANDBY modes are only offered in Z8S180. Note that the minimum recovery time can be achieved if INTERRUPT is used as the Recovery Source.

STANDBY Mode

The Z8S180 has been designed to save power. Two low-power programmable power-down modes have been added; STANDBY mode and IDLE mode. The STANDBY/IDLE mode is selected by multiplexing D6 and D3 of the CPU Control Register (CCR, I/O Address = 1FH). To enter STANDBY mode:

1. Set D6 and D3 to 1 and 0, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY mode, it behaves similar to the SYSTEM STOP mode which currently exists on the Z80180, except that the STANDBY mode stops the external oscillator, internal clocks and reduces power consumption to less than 10 µA.

Since the clock oscillator has been stopped, a restart of the oscillator requires a period of time for stabilization. An 18-bit counter has been added in the Z8S180 to allow for oscillator stabilization. When the part receives an external IRQ or BUSREQ during STANDBY mode, the oscillator is restarted and the timer counts down 2^{17} counts before acknowledgment is sent to the interrupt source.

The following is a description of how the part exits STANDBY for different interrupts and modes of operation.

STANDBY Mode Exit with /RESET

The /RESET input is to be asserted for a duration long enough for the crystal oscillator to stabilize and then exit from the STANDBY mode. When /RESET is de-asserted, it goes through the normal reset timing to start instruction execution at address (logical and physical) 0000H.

The clocking is resumed within the Z8S180 and at the system clock output after /RESET is asserted when the crystal oscillator is restarted, but not yet stabilized.

STANDBY Mode Exit with BUS REQUEST

Optionally, if the BREXT bit (D5 of CPU Control Register) is set to 1, the Z8S180 exits STANDBY mode when the /BUSREQ input is asserted; the crystal oscillator is then restarted. An internal counter automatically provides time for the oscillator to stabilize, before the internal clocking and the system clock output of the Z8S180 are resumed.

The Z8S180 relinquishes the system bus after the clocking is resumed by:

- Tri-State the address outputs A19 through A0.
- Tri-State the bus control outputs /MREQ, /IORQ, /RD and /WR.
- Asserting /BUSACK

The Z8S180 regains the system bus when /BUSREQ is deactivated. The address outputs and the bus control outputs are then driven High; the STANDBY mode is exited.

If the BREXT bit of the CPU Control Register (CCR) is cleared, asserting the /BUSREQ would not cause the Z8S180 to exit STANDBY mode.

If STANDBY mode is exited due to a reset or an external interrupt, the Z8S180 remains relinquished from the system bus as long as /BUSREQ is active.

STANDBY Mode Exit with External Interrupts

STANDBY mode can be exited by asserting input /NMI. The STANDBY mode may also exit by asserting /INT0, /INT1 or /INT2, depending on the conditions specified in the following paragraphs.

If exit conditions are met, the internal counter provides time for the crystal oscillator to stabilize, before the internal clocking and the system clock output within the Z8S180 are resumed.

1. Exit with Non-Maskable Interrupts

If /NMI is asserted, the CPU begins a normal NMI interrupt acknowledge sequence after clocking resumes.

2. Exit with External Maskable Interrupts

If an External Maskable Interrupt input is asserted, the CPU responds according to the status of the Global Interrupt Enable Flag IEF1 (determined by the ITE1 bit) and the settings of the corresponding interrupt enable bit in the Interrupt/Trap Control Register (ITC: I/O Address = 34H):

a. If an interrupt source is disabled in the ITC, asserting the corresponding interrupt input would not cause the Z8S180 to exit STANDBY mode. This is true regardless of the state of the Global Interrupt Enable Flag IEF1.

b. If the Global Interrupt Flag IEF1 is set to 1, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input causes the Z8S180 to exit STANDBY mode. The CPU performs an interrupt acknowledge sequence appropriate to the input being asserted when clocking is resumed if:
   - The interrupt input follows the normal interrupt daisy chain protocol.
   - The interrupt source is active until the acknowledge cycle is completed.

c. If the Global Interrupt Flag IEF1 is disabled, i.e., reset to 0, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input will still cause the Z8S180 to exit STANDBY mode. The CPU will proceed to fetch and execute instructions that follow the SLEEP instruction when clocking is resumed.

If the External Maskable Interrupt input is not active until clocking resumes, the Z8S180 will not exit STANDBY mode. If the Non-Maskable Interrupt (/NMI) is not active until clocking resumes, the Z8S180 still exits the STANDBY mode even if the interrupt sources go away before the timer times out, because /NMI is edge-triggered. The condition is latched internally once /NMI is asserted Low.

IDLE Mode

IDLE mode is another power-down mode offered by the Z8S180. To enter IDLE mode:

1. Set D6 and D3 to 0 and 1, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in IDLE mode, the clock oscillator is kept oscillating, but the clock to the rest of the internal circuit, including the CLKOUT, is stopped completely. IDLE mode is exited in a similar way as STANDBY mode, i.e., RESET, BUS REQUEST or EXTERNAL INTERRUPTS, except that the 2^{17} bit wakeup timer is bypassed; all control signals are asserted eight clock cycles after the exit conditions are gathered.

STANDBY-QUICK RECOVERY Mode

STANDBY-QUICK RECOVERY mode is an option offered in STANDBY mode to reduce the clock recovery time in STANDBY mode from 2^{17} clock cycles (6.5 ms at 20 MHz) to 2^{6} clock cycles (3.2 µs at 20 MHz).

To enter STANDBY-QUICK RECOVERY mode:

1. Set D6 and D3 to 1 and 1, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY-QUICK RECOVERY mode, the operation is identical to STANDBY mode except when exit conditions are gathered, i.e., RESET, BUS REQUEST or EXTERNAL INTERRUPTS; the clock and other control signals are recovered sooner than the STANDBY mode.

Note: If STANDBY-QUICK RECOVERY is enabled, the user must make sure stable oscillation is obtained within 64 clock cycles.

CPU Control Register

The Z8S180 has an additional register which allows the programmer to select options that directly affect the CPU performance as well as controlling the STANDBY operating mode of the chip. The CPU Control Register (CCR) allows the programmer to change the divide-by-two internal clock to divide-by-one. In addition, applications where EMI noise is a problem, the Z8S180 can reduce the output drivers on selected groups of pins to 25% of normal pad driver capability which minimizes the EMI noise generated by the part.

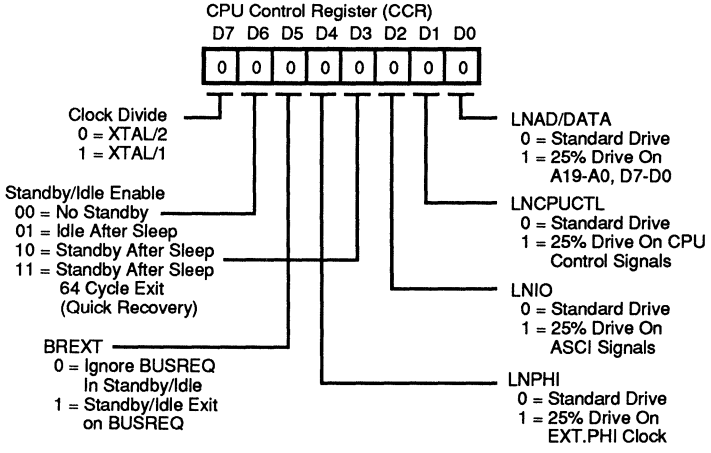


Figure 49. CPU Control Register

Bit 7. *Clock Divide Select.* Bit 7 of the CCR allows the programmer to set the internal clock to divide the external clock by 2 if the bit is 0 and divide-by-one if the bit is 1. Upon reset, this bit is set to 0 and the part is in divide-by-two mode. Since the on-board oscillator is not guaranteed to operate above 20 MHz, an external source must be used to achieve the maximum 20 MHz operation of the part, i.e., an external clock at 40 MHz with 50% duty cycle.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement must be satisfied.

Bits 6 and 3. *STANDBY/IDLE Enable.* These two bits are used for enabling/disabling the IDLE and STANDBY mode.

Setting D6, D3 to 0 and 1, respectively, enables the IDLE mode. In the IDLE mode, the clock oscillator is kept oscillating but the clock to the rest of the internal circuit, including the CLKOUT, is stopped. The Z8S180 enters IDLE mode after fetching the second opcode of a SLEEP instruction, if the I/O STOP bit is set.

Setting D6, D3 to 1 and 0, respectively, enables the STANDBY mode. In the STANDBY mode, the clock oscillator is stopped completely. The Z8S180 enters STANDBY after fetching the second opcode of a SLEEP instruction, if the I/O STOP bit is set.

Setting D6, D3 to 1 and 1, respectively, enables the STANDBY-QUICK RECOVERY mode. In this mode, its operations are identical to STANDBY except that the clock recovery is reduced to 64 clock cycles after the exit conditions are gathered. Similarly, in STANDBY mode, the Z8S180 enters STANDBY after fetching the second opcode of a SLEEP instruction, if the I/O STOP bit is set.

Bit 5. *BREXT.* This bit controls the ability of the Z8S180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

Bit 4. *LNPHI.* This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output is reduced to 25% of its drive capability.

Bit 2. *LNIO.* This bit controls the drive capability of the external I/O pins of the Z8S180. When this bit is set to 1, the output drive capability of the following pins is reduced to 25% of the original drive capability:

- CKS
- RxS/CTS1
- TxS
- CKA1/TEND0
- TxA1
- CKA0/DREQ0
- TxA0

Bit 1. *LNCPUCTL.* This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 25% of the original drive capability:

- /BUSACK
- /RD
- /WR
- /M1
- E
- /MREQ
- /IORQ
- /RFSH
- /HALT
- /TEND1

Bit 0. *LNAD/DATA.* This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus output is reduced to 25% of its original drive capability.

Z85230 ESCC™ CONTROL REGISTERS

See Figures 50 and 51 for the ESCC Control registers. Refer to the ESCC Product/Technical Books for detail.

The Z80182 has two ESCC channels. They can be accessed in any page of I/O space since only the lowest eight address lines are decoded for access. Their Z180™ MPU Address locations are shown in Table 11.

When the 16550 MIMIC interface is enabled ESCC channel B is disconnected from the output pins. The channel B /TRxCB clock is connected to the Transmit and Receive timers of the 16550 MIMIC interface. It is suggested that /TRxCB be programmed as an output with proper baud rate values to time out the transmitter and receiver of the 16550 MIMIC interface.

Table 11. ESCC Control and Data Map

ESCC Channel A	Control	Z180 MPU Address xxE0H
	Data	Z180 MPU Address xxE1H
ESCC Channel B	Control	Z180 MPU Address xxE2H
	Data	Z180 MPU Address xxE3H

PROGRAMMING THE ESCC

The ESCC contains write registers in each channel that are programmed by the system separately to configure the functional uniqueness of the channels.

In the ESCC, the data registers are directly addressed by selecting a High on the D//C pin. With all other registers (with the exception of WR0 and RR0), programming the write registers requires two write operations and reading the read registers, both a write and a read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected read register accessed. All of the ESCC registers, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

Initialization. The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, in the Asynchronous mode, character length, clock rate, number of stop bits, and even or odd parity should be set first. Then the interrupt mode is set, and finally, the receiver and transmitter are enabled.

Write Registers. The ESCC contains 16 write registers (17 counting the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. There are two registers (WR2 and WR9) shared by the two channels that are accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits and reset commands. A new register, WR7', was added to the ESCC and may be written to if WR15, D0 is set. Figure 50 shows the format of each write register.

Read Registers. The ESCC contains ten read registers (eleven, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) are read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (channel A) or the vector modified by status information (channel B). RR3 contains the Interrupt Pending (IP) bits (channel A only). RR6 and RR7 contain the information in the SDLC Frame Status FIFO, but is only read when WR15, D2 is set. If WR7' D6 is set, Write Registers WR3, WR4, WR5, WR7, and WR10 can be read as RR9, RR4, RR5, and RR14, respectively. Figure 51 shows the format of each Read register.

CONTROL REGISTERS

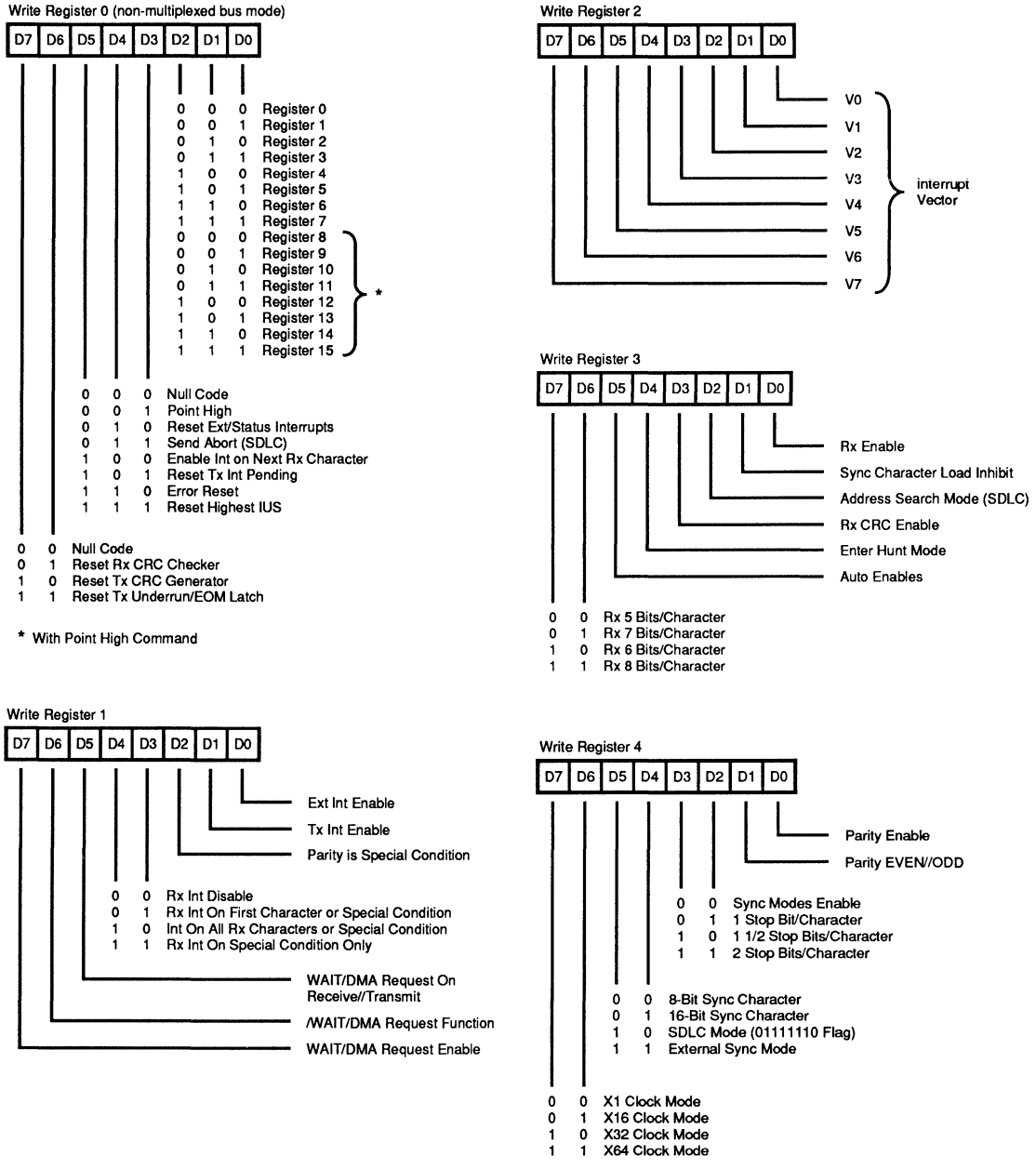
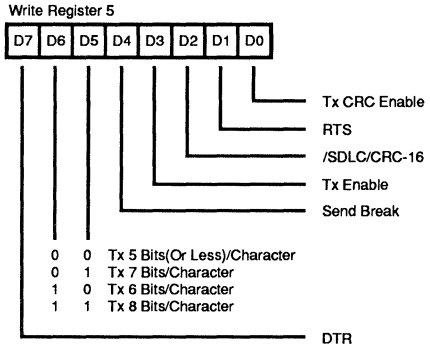
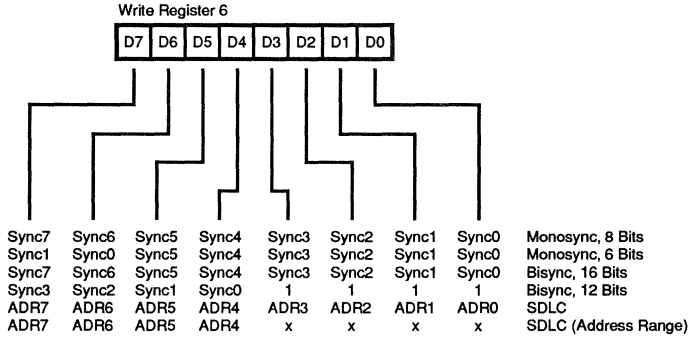


Figure 50. Write Register Bit Functions





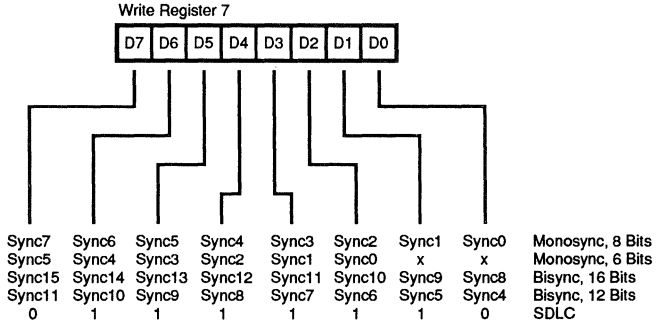


Figure 50. Write Register Bit Functions (Continued)

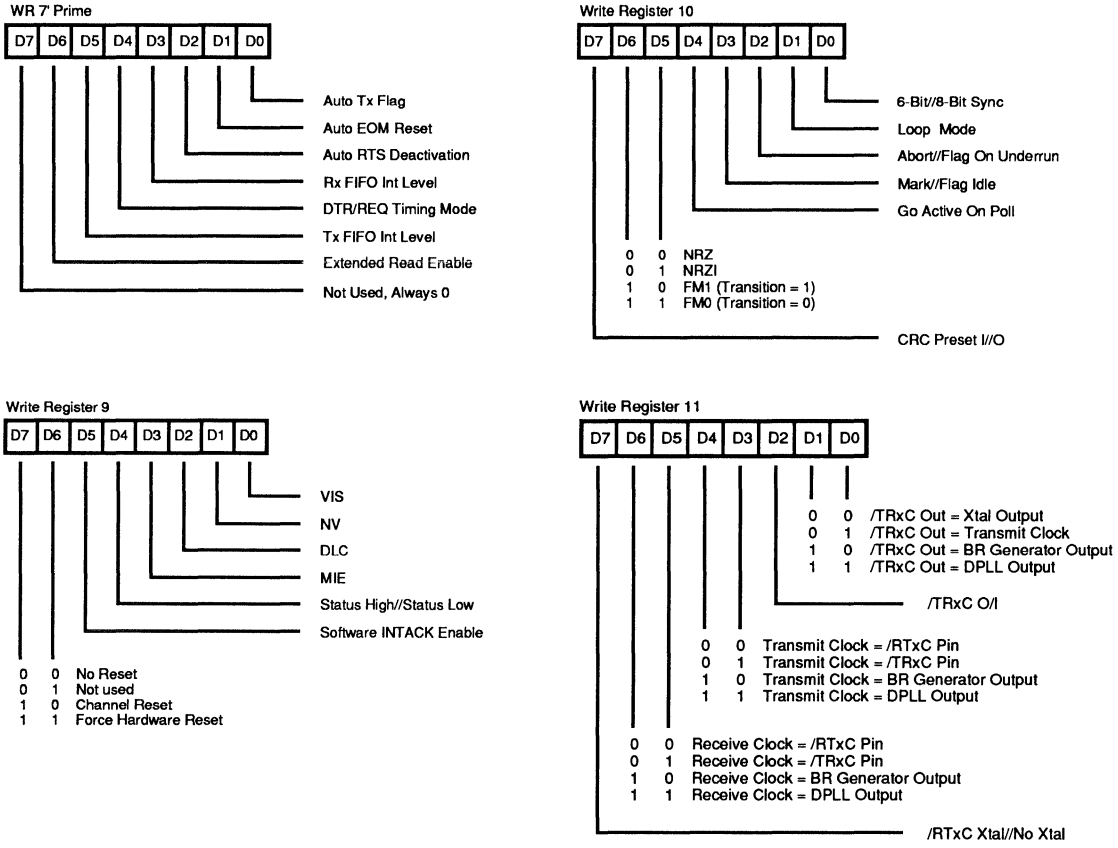


Figure 50. Write Register Bit Functions (Continued)

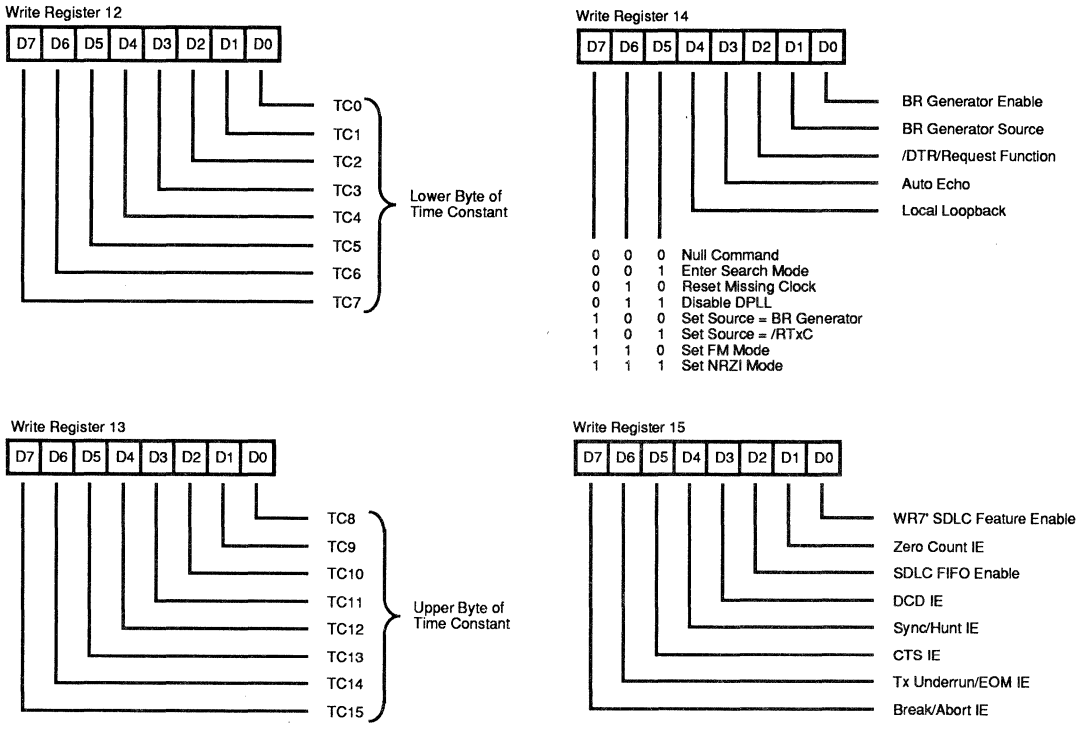


Figure 50. Write Register Bit Functions (Continued)

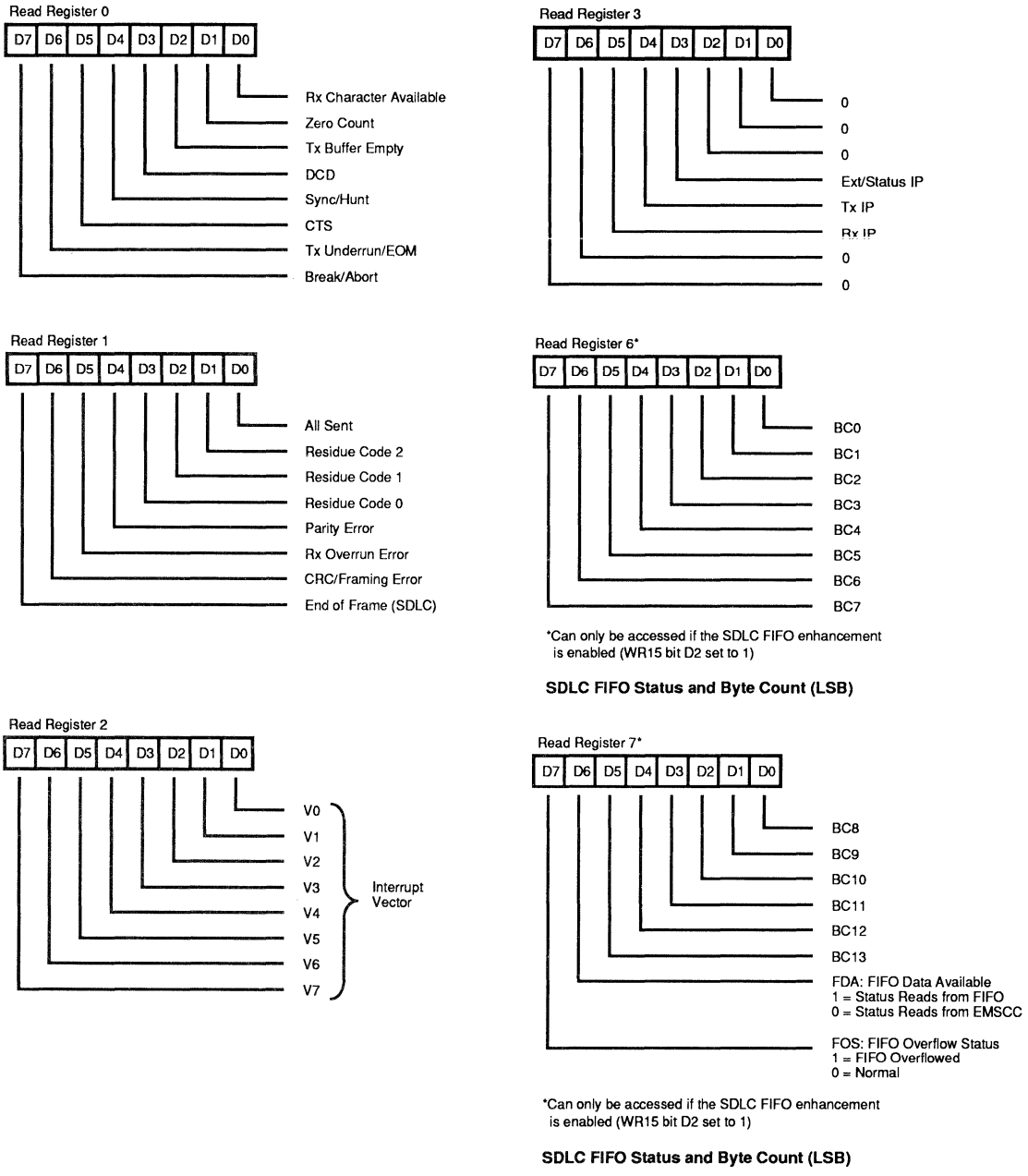


Figure 50. Write Register Bit Functions (Continued)

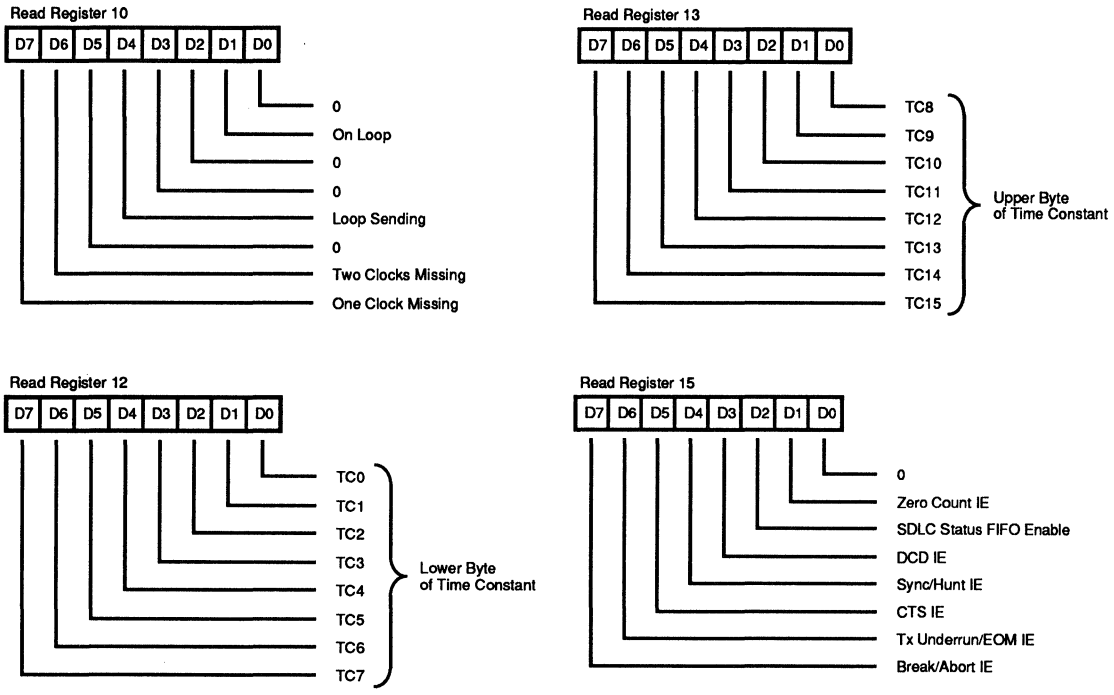


Figure 51. Read Register Bit Functions

Z182 MISCELLANEOUS CONTROL AND INTERFACE REGISTERS

Figures 52 through 65 describe miscellaneous registers that control the Z182 configuration, RAM/ROM chip select, interrupt and various status and timers.

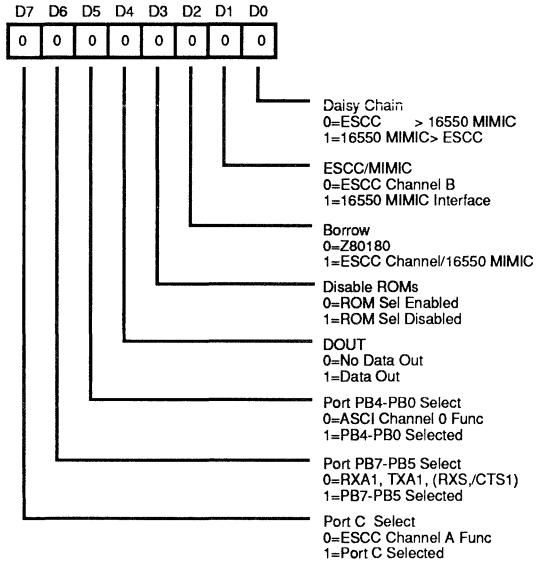


Figure 52. System Configuration Register
(Z180 MPU Read/Write, Address xxEFH)

Bit 7 Port C Select
When this bit is set to a 1 then eight-bit parallel Port C is selected on the multiplexed pins. When this bit is reset to a 0 then these multiplexed pins take ESCC™ Channel A functions.

Bit 6 PB7-PB5 Select
When this bit is set to a 1 then parallel Port B bit 7-bit 5 are selected on the multiplexed pins. When this bit is reset to a 0, then these multiplexed pins become RxA1, TxA1 and RxS/CTS1.

Bit 5 PB4-PB0 Select
When this bit is set to a 1 then parallel Port B bit 4-bit 0 are selected on the multiplexed pins. When this bit is reset to a 0 then these multiplexed pins take ASCI channel 0 functions.

Bit 4 DD_{OUT} ROM Emulator Mode Enable
When this bit is set to a 1, the Z182 is in "ROM emulator mode". In this mode, bus direction for certain transaction periods are set to the opposite direction to export internal bus transactions outside the Z80182. This allows the use of ROM emulators/logic analyzers for application development. See Tables 12a and 12b.

Table 12a. Data Bus Direction (Z182 Bus Master)

I/O And Memory Transactions

	I/O Write to On-Chip Peripherals	I/O Read From On-Chip Peripherals	I/O Write to Off-Chip Peripherals	I/O Read From Off-Chip Peripherals	Write To Memory	Read From Mode	Refresh	Z80182 Idle Mode
Z80182 Data Bus (DD_{OUT} =0)	Out	Z	Out	In	Out	In	Z	Z
Z80182 Data Bus (DD_{OUT} =1)	Out	Out	Out	In	Out	In	Z	Z

Table 12b. Data Bus Direction (Z182 Bus Master)

Interrupt Acknowledge Transaction

	Intack For On-Chip Peripheral	Intack For Off-Chip Peripheral
Z80182 Data Bus (DD_{OUT}=0)	Z	In
Z80182 Data Bus (DD_{OUT}=1)	Out	In

Table 13a. Data Bus Direction (Z80182 is Not Bus Master)

I/O And Memory Transactions

	I/O Write to On-Chip Peripherals	I/O Read From On-Chip Peripherals	I/O Write to Off-Chip Peripherals	I/O Read From Off-Chip Peripherals	Write To Memory	Read From Mode	Refresh	Z80182 Idle Mode
Z80182 Data Bus DD_{OUT}=0)	In	Out	Z	Z	Z	In	Z	Z
Z80182 Data Bus (DD_{OUT}=1)	In	Out	Z	Z	Z	In	Z	Z

Table 13b. Data Bus Direction (Z80182 is Not Bus Master)

Interrupt Acknowledge Transaction

	Intack For On-Chip Peripheral	Intack For Off-Chip Peripheral
Z80182 Data Bus (DD_{OUT}=0)	Out	In
Z80182 Data Bus (DD_{OUT}=1)	Out	In

The word "Out" means that the Z182 data bus direction is in output mode, "In" means input mode, and "Z" means high impedance. DD_{OUT} stands for Data Direction out and is the status of the D4 bit in the System Configuration Register (SCR).

Bit 3 Disable ROMs
If this bit is a one, it disables the ROMSEL pin. If it is a zero, addresses below the ROM boundary set by the ROMBR register will cause the ROMSEL pin to go Low.

Bit 2 Borrow
The Z80182 has three pins that are triple multiplexed and controlled by bit 2 and bit 1. Table 14 shows the different modes.

Table 14. SCR Control for Triple Multiplexed Pins

Bit 2	Bit 1	System Configuration Register
0	0	/TEND1,TxS,CKS
0	1	/TEND1,TxS,CKS
1	0	/RTSB,(/DTR//REQB),(/W//REQB)
1	1	/HRxRDY,//HTxRDY,HINTR

Bit 1 ESCC™ Channel B/MIMIC
If this bit is a zero, Mode 0 is selected.
If this bit is one, Mode 1 is selected.

Mode 0:
Channel A ESCC Enabled
Channel B ESCC Enabled
PIA Port Enabled
16550 MIMIC Interface Disabled

Mode 1:
Channel A ESCC enabled
Channel B outputs disabled
PIA disabled
16550 MIMIC Interface Enabled

Bit 0 Daisy Chain
This bit is used to set interrupt priority of the ESCC and 16550 MIMIC interface. If it is a zero, the ESCC is higher up in the daisy chain than the 16550 MIMIC interface. If it is a one then the 16550 interface is higher up than the ESCC.

/RAMCS AND /ROMCS REGISTERS

To assist decoding of ROM and RAM blocks of memory, three more registers and two pins have been added to the Z80182. The two pins are /ROMCS and /RAMCS. The three registers are the RAMUBR, RAMLBR, and ROMBR.

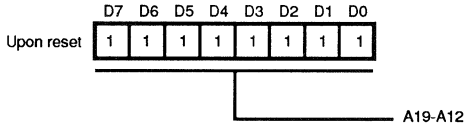


Figure 53. RAMUBR
(Z180 MPU Read/Write, Address xxE6H)

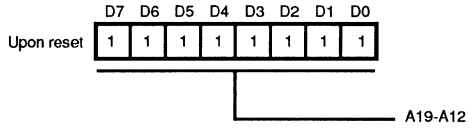


Figure 54. RAMLBR
(Z180 MPU Read/Write, Address xxE7H)

/RAMCS AND /ROMCS REGISTERS (Continued)

RAMUBR, RAMLBR RAM Upper Boundary Range, RAM Lower Boundary Range
These two registers specify the address range for the /RAMCS signal. When accessed memory addresses are less than or equal to the value programmed in the RAMUBR and greater than or equal to the value programmed in the RAMLBR, /RAMCS is asserted. The A18 signal from the CPU is taken before it is multiplexed with T_{OUT}. In the case that these registers are programmed to overlap, /ROMCS takes priority over /RAMCS (/ROMCS is asserted and /RAMCS is inactive).

Chip Select signals are going active for the address range:

/ROMCS: (ROMBR) >= A19-A12 >= 0
/RAMCS: (RAMUBR) >= A19-A12 >= (RAMLBR)

These registers are set to FFH at POR, and the boundary addresses of ROM and RAM are as follows:

ROM lower boundary address
(fixed) = 00000H

ROM upper boundary address
(ROMBR register) = 0FFFFFH

RAM lower boundary address
(RAMLBR register) = 0FFFFFH

RAM upper boundary address
(RAMUBR register) = 0FFFFFH

Since /ROMCS takes priority over /RAMCS, the latter will never be asserted until the value in the ROMBR and RAMLBR registers are re-initialized to lower values.

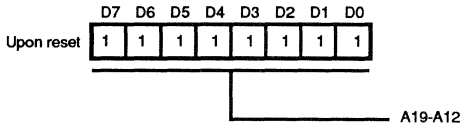


Figure 55. ROMBR
(Z180 MPU Read/Write, Address xxE8H)

ROMBR ROM Address Boundary Register
This register specifies the address range for the /ROMCS signal. When accessed, memory addresses are less than or equal to the value programmed in this register, the /ROMCS signal is asserted.

The A18 signal from the CPU is obtained before it is multiplexed with T_{OUT}. This signal can be forced to a "1" (inactive state) by setting bit 3 in the System Configuration Register, to allow the user to overlay the RAM area over the ROM area.

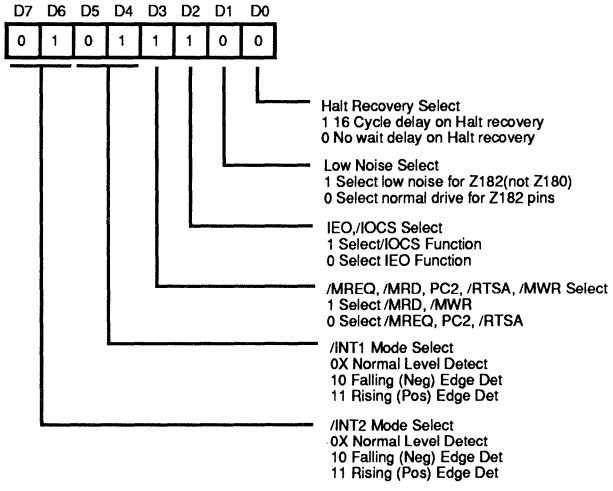


Figure 56. Interrupt Edge/Pin MUX Register
(Z180 MPU Read/Write, Address xxDFH)

Bits 7-6 control the interrupt capture logic for the external /INT2 PIN. When programmed as '0X', the /INT2 pin performs as the normal level detecting interrupt pin. When programmed as 10 the negative edge detection is enabled. Any falling edge latches an active Low on the internal /INT2 of the Z180. This interrupt must be cleared by writing a 1 to bit 7 of the Port C Data Register. Programming these control bits to 11 enables rising edge interrupts to be latched. The latch is cleared in the same fashion as the falling edge.

Bits 5-4 control the interrupt capture logic for the external /INT1 PIN. When programmed as '0X', the /INT1 pin performs as the normal level detecting interrupt pin. When programmed as 10, the negative edge detection is enabled. Any falling edge latches an active Low on the internal /INT1 of the Z180. This interrupt must be cleared by writing a 1 to bit 6 of the Port C Data Register. Programming these control bits to 11 enables rising edge interrupts to be latched. The latch is cleared in the same fashion as the falling edge.

Bit 3, a 1 selects the /MRD and the /MWR functions. The default for power up and /RESET conditions is 1, i.e. the /MRD and /MWR. By programming this bit to 0 the /MREQ Z180 function is enabled, as well as the PC2//RTSA function on the PC2//RTSA//MWR pin.

Bit 2 selects the /IOCS function which is the default for power up and /RESET conditions. By programming this bit to 0 the IEO function is enabled for this multiplexed pin.

Bit 1 selects the low noise or normal drive feature for the Z182 pins (non-Z180 pins). The default at power up is normal drive for Z182 pins. By programming this bit to 1, low noise for the Z182 pins is chosen. Programming this bit to 0 selects normal drive for the Z182 pins. Refer to the Z8S180 Product Specification for Low noise control of Z180 pins.

Bit 0, a 1 selects 16 cycle wait delay on recovery from HALT. A 0 selects no wait delay on HALT recovery.

16550 MIMIC INTERFACE REGISTERS

MIMIC Master Control Register (MMC)

The 16550 MIMIC interface is controlled by the MMC register. Setting it allows for different modes of operation such as using the eight-bit counters, DMA accesses, and which IRQ structure is used with the PC/XT/AT.

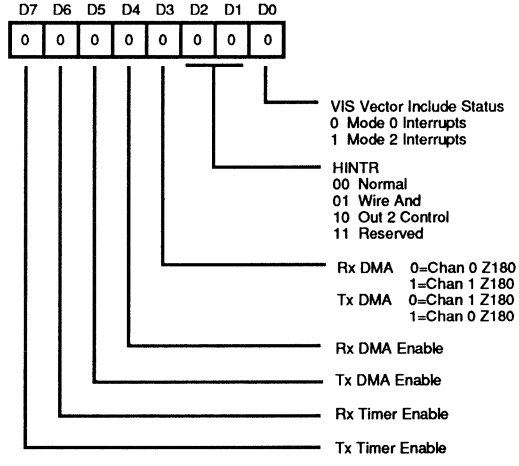


Figure 57. MIMIC Master Control Register
(Z180 MPU Read/Write, Address xxFFH)

Bit 7 Transmit Timer Delay Counter Enable (Read/Write)
If bit 7 is set to a one, it enables the transmit delay timer. When the Z180 reads the Transmit Register, it loads the transmit delay timer from the Transmit Time Constant Register and enables the timer to count down to zero. This timer delays setting the Transmit Holding Register Empty (THRE) bit until the timer times out. If this bit is zero, then THRE is set immediately on a Z180 read of the Transmit Register.

Bit 6 Receive Timer Delay Counter Enable (Read/Write)
If bit 6 is set to a one, it enables the receive delay timer. When the Z180 writes to the Receive Buffer, it loads the receive delay timer from the Receive Time Constant Register and enables the timer to count down to zero. This timer delays setting the Data Ready (DR) bit in the LSR until the timer times out. If this bit is a zero then DR is set immediately on a Z180 write to the Receive Buffer.

Both counters are single pass and stop on a count of Zero. Their purpose is to delay data transfer just as if the 16550 UART had to shift the data in and out. This is provided to alleviate any software problems a high speed continuous data transfer might cause to existing software. If this is not a problem, then data can be read and written as fast as the two machines can access the devices. In FIFO mode of operation, the timers are used to delay the status to the PC interface by the time required to actually shift the characters out, or in, if an actual UART were present.

Bit 5 Transmit DMA Enable (Read/Write)
If this bit is set to a one, it enables the Transmit DMA function.

Bit 4 Receive DMA Enable (Read/Write)
If this bit is set to one, it enables the Receive DMA function.

Bit 3 Receive DMA Channel Select (Read/Write)
If bit 3 is set to a zero, then Receive DMA transfer is done via Z180 DMA channel 0 and the Transmit DMA is done via DMA channel 1. If bit 3 is set to a one, then Receive DMA transfer is done via Z180 DMA channel 1 and the Transmit DMA is done via DMA channel 0.

Bits 2,1 Interrupt Select (Read/Write).
See Table 15.

Bit 0 Vector Include Status (Read/Write)
This bit is used to select the interrupt response mode of the Z180. A 0 in this bit enables mode 0 interrupts; a 1 enables mode 2 response.

Table 15. MIMIC Master Control Register Interrupt Select

bit 2	bit 1	HINTR Function
0	0	HINTR is set to normal 16550 MIMIC mode. A fully driven output is required when external priority arbiters are used.
0	1	A wired AND condition on the HINTR pin is possible to the PC/XT/AT. The interrupt is active High with only the pullup of the HINTR pin driving; otherwise this pin is tri-state. Wired AND is needed when an external arbiter is not available.
1	0	HINTR is driven when out 2 of the Modem Control Register is a 1. HINTR is tri-state when MCR out 2 is a 0.
1	1	RESERVED

IUS/IP Register

The IUS/IP Register is used by the Z180™ MPU to determine the source of the interrupt. This register will have the appropriate bit set when an interrupt occurs.

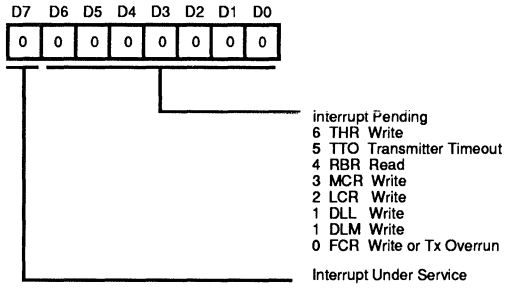


Figure 58. IUS/IP Register
(Z180 MPU, Address xxFEH)

Bit 7 Interrupt Under Service (Read/Write)
This bit represents a logical OR of each individual IUS bit for the internal MIMIC interrupt daisy chain. An IUS bit is set when an interrupt is registered (IP set) and enabled (IE set), the incoming IEI daisy chain is active (chain enabled) and an interrupt acknowledge cycle is entered. By writing a 1 to this bit the highest priority IUS bit that is set will be reset. Writing a 0 to this bit has no effect.

Bit 6 Transmit Holding Register Written (Read Only)
This bit is set when the PC/XT/AT writes to the Transmit Holding Register. It is reset when the Z180 MPU reads the Transmit Holding Register. In FIFO mode, this bit is set when the trigger level is reached (4,8,14 bytes available). Note: The THR bit is set (interrupts) when the transmitter FIFO reaches the data available trigger level set in the MPU FCR control register. The bit and interrupt source is cleared when the number of data bytes falls below the set trigger level.

Bit 5 Transmitter Timeout with Data in FIFO (Read Only)
This bit is set when the transmitter FIFO has been idle (no read or write and timer decrements to zero) with data bytes below the trigger level. It is cleared when the FIFO is read or written.

Bit 4 Receive Buffer Read (Read Only)
This bit is set when the PC/XT/AT reads the Receive Buffer Register. It is reset when the Z180 MPU writes to the Receive Buffer Register. In FIFO mode, this bit is set upon the PC reading all the data in the receive FIFO. Note: RBR is set and interrupts when the receive FIFO has been emptied by the PC. This bit and interrupt are cleared when one or more bytes are written into the receive FIFO by the MPU.

Bit 3 Modem Control Register Write (Read Only)
This bit is set when the PC/XT/AT writes to the Modem Control Register. It is reset when the Z180™ MPU reads the Modem Control Register.

Bit 2 Line Control Register Write (Read Only)
This bit is set when the PC/XT/AT writes to the Line Control Register. It is reset when the Z180 MPU reads the Line Control Register.

Bit 1 Divisor Latch LS/MS Write (Read Only)
This bit is set when the PC/XT/AT writes to the Divisor Latch Least Significant or Most Significant bytes. It is reset when the PC reads the LS/MS register(s). To determine which byte(s) have been written, the Z180 must read either LS or MS locations and then repoll this bit. If only one location is interrupting, the interrupt is cleared when that location is read by the Z180.

Bit 0 FIFO Control Register Write (Read Only)
This bit is set when the PC/XT/AT writes to the FCR. It is reset when the Z180 MPU reads this register.

Interrupt Enable Register

The IE Register allows each of the 16550/8250 interrupts to the Z180™ MPU to be masked off individually or globally.

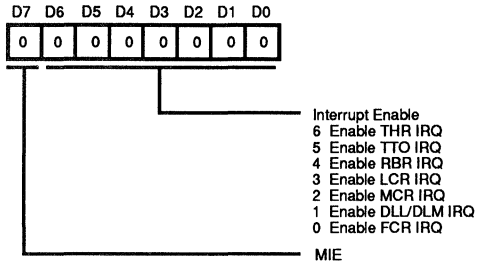


Figure 59. IE Register
(Z180 MPU, Address xxFDH)

Bit 7 Master Interrupt Enable (Read/Write)
If bit 7 is a zero, all interrupts from the 16550 MIMIC are masked off. If this bit is a one, then interrupts are enabled individually by setting the appropriate bit.

Bit 6 Enable THR Interrupt (Read/Write)
If this bit is a one, it enables the Transmit Holding Register Interrupt.

Bit 5 Enable TTO Interrupt (Read/Write)
If this bit is a one, it enables the Transmitter Timeout Interrupt. This interrupts the CPU when characters remain in the FIFO below the trigger level and the FIFO is not read or written for the length of time in the transmitter timeout register.

Bit 4 Enable RBR Interrupt (Read/Write)
If this bit is a one, it enables the Receive Buffer Register Interrupt.

Bit 3 Enable LCR Interrupt (Read/Write)
If this bit is a one, it enables the Line Control Register interrupt.

Bit 2 Enable MCR Interrupt (Read/Write)
If this bit is a one, it enables the Modem Control Register Interrupt.

Bit 1 Enable DLL/DLM Interrupt (Read/Write)
If this bit is a one, it enables the Divisor Latch Least and Most Significant Byte interrupts.

Bit 0 Enable FCR Interrupt (Read/Write)
If this bit is a one, then interrupts are enabled for a PC write to the FIFO control register (FCR).

Priority of interrupts are in this order:
Highest 6. THR IRQ
5. TTO IRQ
4. RBR IRQ
3. MCR IRQ
2. LCR IRQ
1. DLL IRQ
1. DLM IRQ
Lowest 0. FCR IRQ

Interrupt Vector Register

The Interrupt Vector Register contains either the opcode (Z180 Interrupt Mode 0) or the modified vector used as the lower address for a Z180 interrupt service routine (Z180 Interrupt Mode 2), depending upon the VIS bit in the MMC Register (MIMIC Master Control Register). If the VIS bit is a zero, then Z180 Mode 0 interrupt is selected; if VIS is a one, then Z180 Mode 2 is selected. Note that in Z180 Interrupt Mode 0, the data input to the MPU during the interrupt acknowledge cycle is an instruction opcode; in Z180 Interrupt Mode 2, this data (modified depending on the source of the interrupt) becomes part of an address from which to get the starting address of the interrupt service routine.

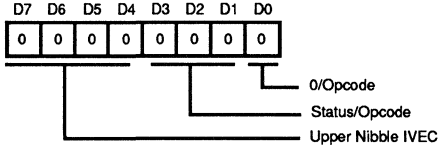


Figure 60. IVEC Register
(Z180 MPU, Address xxFCH)

Bits 7-4 Upper Nibble IVEC (Read/Write)
These four bits generate either an opcode for Z180 Interrupt Mode 0, or the upper four bits of the interrupt modified vector used as eight bit address to support the Z180 Interrupt Mode 2. These bits are read/write and always read back what was last written to them.

Bits 3-1 Interrupt Modified Vector/Opcode (Read/Write Table 16)
These three bits are the Interrupt Status bits when VIS in the MMC register is a one (Z180 Interrupt Mode 2). If VIS bit is a zero, then this field contains bit 3-bit 1 of the opcode. If the VIS bit is a zero, then these bits contain what was last written to them.

Table 16. Interrupt Status Bits

Bits 321	Interrupt Request
000	NO IRQ
001	FCR IRQ
010	DLL/DLM IRQ
011	LCR IRQ
100	MCR IRQ
101	RBR IRQ
110	TTO IRQ
111	THR IRQ

Bit 0 0/Opcode (Read/Write)
This bit is always a zero when the VIS bit is a one. If the VIS bit is a zero then this bit reads back what was last written to it.

This register serves both interrupt modes. When the VIS bit is a zero the last value written to the register can be read back. If the VIS bit is a one and an interrupt is pending the value read is the last value written to the upper nibble plus the status for the interrupt that is pending. If no interrupt is pending, then the last value written to the upper nibble plus the lower nibble is read from the register.

If the vector includes the status, then the lower four bits of the vector change asynchronously depending on the interrupting source. Since this vector changes asynchronously, then the interrupt service routine to read the IVEC register might read the source of the most recent IRQ/INTACK cycle if that IRQ does not have its IUS set.

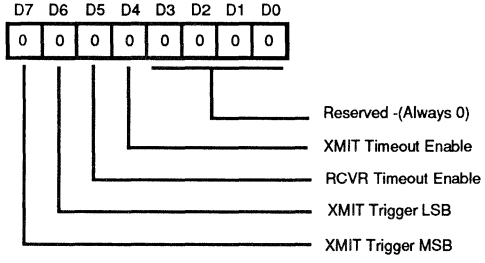


Figure 61. FIFO Status and Control Register
(Z180 MPU Read/Write, Address xxECH)

Bit 7 and Bit 6 XMIT Trigger MSB,LSB
This field determines the number of bytes available to read in the transmitter FIFO before an interrupt occurs to the MPU (Table 17).

Table 17. Transmitter Trigger Level

b7	b6	Level (# bytes)
0	0	1
0	1	4
1	0	8
1	1	14

Bit 5 Receive Timeout Enable
This bit enables the Z80182 Receive Timeout Timer that is used to emulate the four character timeout delay that is specified by the 16550. If no read or write to the RCVR FIFO has taken place and data bytes are available, but are below the PC trigger level. If this timer reaches zero, an interrupt is sent to the PC.

Bit 4 Transmitter Timeout Enable
This bit enables the Z80182 timer that is used to interrupt the Z180 MPU if characters are available, but are below the trigger level. The timer is enabled to count down if this bit is one and the number of bytes is below the set transmitter trigger level. The timer will timeout and interrupt the MPU if no read or write to the XMIT FIFO takes place within the timer interval.

Bit 3 Reserved for future use. Always write and read as 0 by users. Writing 1 enables a test mode for emulation of timers.

Bits 2-0 Reserved for Future Use. Always write and read as 0.

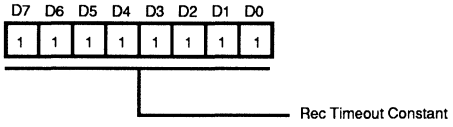


Figure 62. Receive Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEAH)

This register contains an 8-bit constant for emulation of the 16550 four character timeout feature. Software must determine the value to load into this register based on the bit rate and word length specified by the MIMIC interface with the PC. This timer receives its input from the /TRxCB Clock of the SCC. This timer is enabled to down count when the enable bit in the FSR register is set and the trigger level has not been reached on the RCVR FIFO. The counter reloads each time there is a read or write to the RCVR FIFO.

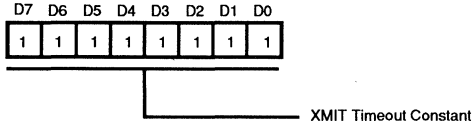


Figure 63. Transmit Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEBH)

This register contains an 8-bit constant for determining the interval for the Transmit Timeout Timer. If allowed to decrement to zero, this timer interrupts the MPU by setting the THR bit in the IUS/IP register. This timer receives its input from the /TRxCB Clock of the SCC. The timer is enabled to down count when the enable bit in the FSR register is set and the trigger level has not been reached on the XMIT FIFO. The counter reloads each time there is a read or write to the XMIT FIFO.

Transmit And Receive Timers

Because of the speed at which data transfers can take place between the Z180™ MPU and the PC/XT/AT, two timers have been added to alleviate any software problems that a high speed data transfer might cause. These timers allow the programmer to slow down the data transfer just as if the 16550 MIMIC interface had to shift the data in and out. The Timers receive their input from the /TRxCB Clock since, in 16550 MIMIC mode, the ESCC channel B is disabled. For example, the clock source for the 8-bit registers: RTTC (Receive Timeout Time Constant, xxEAH), TTTC (Transmit Timeout Time Constant, xxEBH), TTCR (Transmit Time Constant Register, xxFAH) and RTCR (Receive Time Constant Register, xxFBH) uses the /TRxCB Clock. The /TRxCB Clock can use the ESCC's 16-bit BRG as its clock source thus allowing the programmer to access a total of 24 bits as a timer to slow down the data transfer.

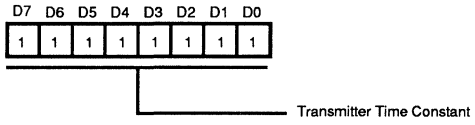


Figure 64. Transmitter Time Constant Register
(Z180 MPU Read/Write, Address xxFAH)

When a write from the PC/XT/AT is made to the Transmit Holding Register, an interrupt to the Z180 MPU is generated. The Z180 MPU then reads the data in the Transmit Holding Register. Upon this read, if the Transmitter timer is enabled, the time constant from the Transmitter Time Constant Register is loaded into the Transmitter timer and enables the count. After the timer reaches a count of zero the Transmit Holding Register Empty bit is set. However, the above is only true when the PC/XT/AT is reading the Transmit Holding Register Empty bit. To allow the Z180 MPU to know that it has already read the byte of data, immediately following a read from the Transmit Holding Register, a mirrored Transmit Holding Register, Empty bit is set. This mirrored bit is always read back to the Z180 MPU when it reads the Line Status Register.

If the transmitter timer is not enabled when the Z180 MPU reads the Transmit Holding Register, both Transmit Holding Register Empty bits are set immediately. In FIFO mode of operation, the effect is similar as the status to PC is always delayed such that a PC interrupt for empty FIFO will not occur before the time required for each character read from the FIFO by the Z180 has elapsed. The effect is that the PC will not see data requests from an empty FIFO any faster than would occur with a true UART when the delay feature is enabled.

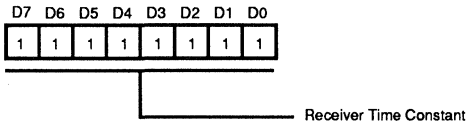


Figure 65. Receive Time Constant Register
(Z180 MPU Read/Write, Address xxFBH)

When the Z180™ MPU writes to the Receive Buffer register and the Receive Timer is enabled, the Receive Timer is loaded with the Receive Time Constant, the timer is enabled and counts down to zero. When the timer reaches zero, the Data Ready bit in the Line Status Register is set. As with the Transmit Timer, the Data Ready bit is also mirrored. Immediately upon a write to the Receive Buffer, the mirrored bit is set to let the Z180 MPU know that the byte has already been written. If the timer is not enabled, then both Data Ready bits are set immediately upon a write to the Receive Buffer. The FIFO mode of operation is similar in that the status to the PC is always delayed by the time required for each character written to the FIFO by the Z180. The effect is that the PC will not see a FIFO trigger level or DMA request faster than would occur with a true UART when the delay feature is enabled.

16550 MIMIC REGISTERS

The Z80182 contains a register set for interfacing with the PC/XT/AT. The registers are shown in Figures 66 to Figure 78.

Receive Buffer Register
Transmit Holding Register
Interrupt Enable Register
Interrupt Identification Register
Line Control Register
Modem Control Register
Line Status Register
Modem Status Register
Scratch Register
Divisor Latch Least Significant/Most Significant Bytes
FIFO Control Register

These registers are used to emulate the 16550 UART. The PC/XT/AT can access these registers just as if it was interfacing with the 16550 UART. This allows the Z80182 to be software compatible with existing modem software.

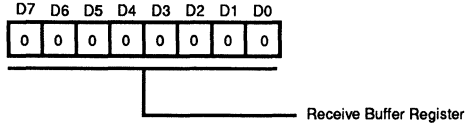


Figure 66. Receive Buffer Register
(PC Read Only, Address 00H, DLAB=0, R/W=Read)
(Z180 MPU Write Only, Address XXF0H)

When the Z180 has assembled a byte of data to pass to the PC/XT/AT, it places it in the Receive Buffer Register. If the Received Data Available interrupt is enabled then an interrupt is generated for the PC/XT/AT and the Data Ready bit is set (if the Receive Timer is enabled, the interrupt and setting of the Data Ready bit is delayed until after the timer times out). Also the shadowed bits of the Line Status Register are transferred to their respective bits when the Z180 MPU writes to the Receive Buffer Register (See Line Status Register Bits 1, 2, 3 and 4). This allows a simultaneous setting of error bits when the data is written to the Receive Buffer Register. In FIFO, mode this address is used to read (PC) and write (Z180) the Receive FIFO.

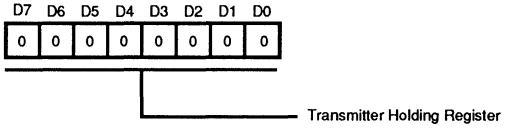


Figure 67. Transmit Holding Register
(PC Write Only, Address 00H, DLAB=0, R/W=Write)
(Z180 MPU Read Only, Address xxF0H)

When the PC/XT/AT writes to the Transmit Holding Register, the Z80182 responds by setting the appropriate bit in the IP register and by generating an interrupt to the Z180 MPU if it is enabled. When the Z180 MPU reads this register the Transmit Holding Register empty flag is set (if the transmitter timer is enabled , this bit is set after the timer times out). In FIFO mode of operation, this address is used to read (Z180) and write (PC) the Transmitter FIFO.

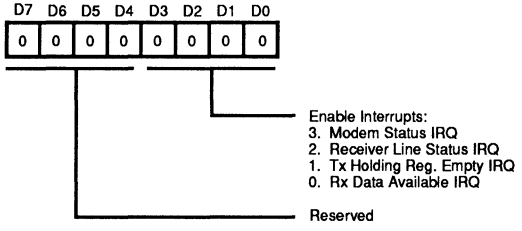


Figure 68. Interrupt Enable Register
(PC Read/Write, Address 01H)
(Z180 MPU Read Only, Address xxF1H)

Bits 7-4 Reserved (Always 0)
These bits reserved for future use.

Bit 3 Modem Status IRQ
If bits 0, 1, 2 or 3 of the Modem Status Register are set and this bit is a one, an interrupt to the PC/XT/AT is generated.

Bit 2 Receive Line Status IRQ
If bits 1, 2, 3 and 4 of the Line status register are set and this bit is a one, an interrupt to the PC/XT/AT is generated.

Bit 1 Transmit Holding Register Empty IRQ
If bit 5 of the Line Status Register is a one and this bit is a one, an interrupt to the PC/XT/AT is generated.

Bit 0 Received Data Available IRQ
If bit 0 of the Line Status Register is a one and this bit is a one, an interrupt to the PC/XT/AT is generated.

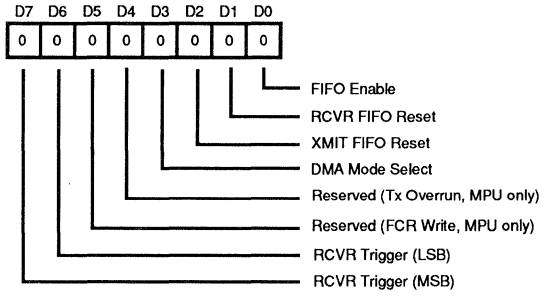


Figure 69. FIFO Control Register
(PC Write Only, Address 02H)
(Z180 MPU Read Only, Address xxE9H)

Bit 6 and Bit 7 RCVR trigger LSB and MSB bits
This 2 bit field determines the number of available bytes in the receiver FIFO before an interrupt to the PC occurs. See Table 18.

Bit 4 and Bit 5
Reserved for future use (PC side). Note: From the MCU side, bit 4 and bit 5 flags two sources of interrupts. Bit 5 is a FIFO interrupt indicating that the FCR had changed; bit 4 is a Tx overrun interrupt, indicating transmit overrun. A read of the FCR from the MCU side will clear a previously set bit 4 or bit 5.

Bit 3 DMA mode select
Setting this bit to 1 will cause the MIMIC DMA mode to change from mode 0 to mode 1 (if bit 0 is 1, FIFO mode is enabled). This affects the DMA mode of the FIFO. A '1' in this bit enables multi-byte DMA).

Bit 2 XMIT FIFO Reset
Setting this bit to a 1 will cause the transmitter FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing; however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 1 RCVR FIFO Reset
Setting this bit to a 1 will cause the receiver FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing, however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 0 FIFO Enable
The PC writes this bit to logic 1 to put the 16550 MIMIC into FIFO mode. This bit must be a 1 when writing to the other bits in this register or they will not be programmed. When this bit changes state, any data in the FIFO's or transmitter holding and Receive Buffer Registers is lost and any pending interrupts are cleared.

Table 18. Receive Trigger Level

b7	b6	Trigger Level, Number of Bytes
0	0	1
0	1	4
1	0	8
1	1	14

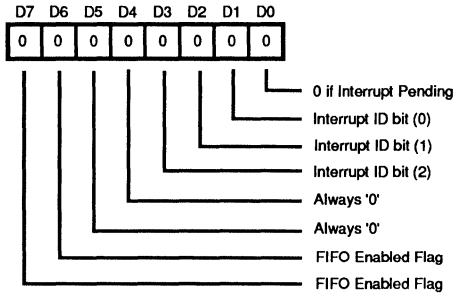


Figure 70. Interrupt Identification Register
(PC Read Only, Address 02H)
(Z180 MPU no access)

Bit 7 and Bit 6 FIFO's enabled
These bits will read 1 if FIFO mode is enabled on the MIMIC.

Bit 5 and Bit 4 Always read 0
Reserved bits.

Bits 3-1 Interrupt ID bits
This 3 bit field is used to determine the highest priority interrupt pending. See Table 19.

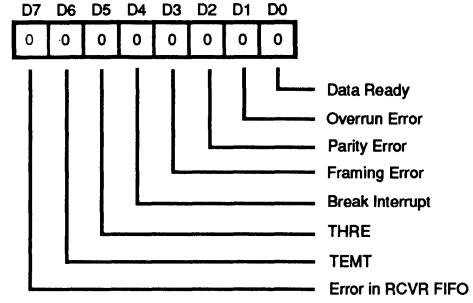


Figure 71. Line Status Register
(PC Read Only, Address 05H)
(Z180 MPU Read/Write bits 6, 4, 3, 2, Address xxF5H)

Table 19. Interrupt Identification Field

b3	b2	b1	Priority	Interrupt Source	INT Reset Control
0	1	1	Highest	Overrun, Parity, Framing error or Break detect bits set by MPU	Read Line Status Register
0	1	0	2nd	Received Data trigger level	RCVR FIFO drops below trigger level
1	1	0	2nd	Receiver Timeout with data in RCVR FIFO	Read RCVR FIFO
0	0	1	3rd	Transmitter Holding Register Empty.	Writing to the Transmitter Holding Register or reading the Interrupt Identification Register when the THRE is the source of the interrupt.
0	0	0	4th	MODEM status: CTS,DSR,RI or DCD	Reading the MODEM

Bit 0 Interrupt Pending
This bit is logic 0 and interrupt is pending.

When the PC accesses the IIR, the contents of the register and all pending interrupts are frozen. Any new interrupts will be recorded, but not acknowledged, during the IIR access.

Bit 7 Error in RCVR FIFO
In 16450 mode, this bit will read logic 0. In 16550 mode this bit is set if at least one data byte is available in the FIFO with one of its associated error bits set. This bit will clear when there are no more errors (or break detects) in the FIFO.

Bit 6 Transmitter Empty
This bit must be set or reset by the MPU by a write to this register bit.

Bit 5 Transmit Holding Register Empty, THRE
This bit is set to one when either the THR has been read (emptied) by the MPU (16450 mode) or the XMIT FIFO is empty (16550 mode). This bit is set to 0 when either the THR or XMIT FIFO become non-empty. A shadow bit exists so that the register bit setting to 1 is delayed by the Transmitter Timer if enabled. The MPU when reading this bit will not see the delay. Both shadow and register bits are cleared when the PC writes to the THR of XMIT FIFO.

Bit 2, 3, 4 Parity Error, Framing Error, Break Detect
These bits are written, indirectly, by the MPU as follows: The bits are first written to shadow bit locations when the MPU write accesses the LSR. When the next character is written to the Receive Buffer or RCVR FIFO, the data in the shadow bits is then copied to the LSR (16450 mode) or FIFO RAM (16550 mode). In FIFO mode bits become available to the PC when the data byte associated with the bits is next to be read (top of FIFO). In FIFO mode, with successive reads of the receiver, the status bits will be set if an error occurs on any byte. Once the MPU writes to the Receive Buffer or RCVR FIFO, the shadow bits are auto cleared. The register bits are cleared upon the PC reading the LSR. In FIFO mode these bits will be set if any byte has the respective error bit set while the PC reads multiple characters from the FIFO.

Bit 1 Overrun Error
This bit is set if the Z180 MPU makes a second write to the Receive Buffer before the PC reads the data in the Buffer (16450 mode) or with a full RCVR FIFO (16550 mode.) No data will be transferred to the RCVR FIFO under these circumstances. This bit is reset when the PC reads the Line Status Register.

Bit 0 Data Ready
This bit is set to 1 when received data is available, either in the RCVR FIFO (16550 mode) or Receive Buffer Register (16450 mode). This bit is set immediately upon the MPU writing data to the Receive Buffer or FIFO if the Receive Timer is not enabled but is delayed by the timer interval if the Receive Timer is enabled. For MPU read access a shadow bit exists so that the MPU does not see the delay the PC does. Both bits are cleared to logic zero immediately upon reading all the data in either the Receive Buffer or FIFO.

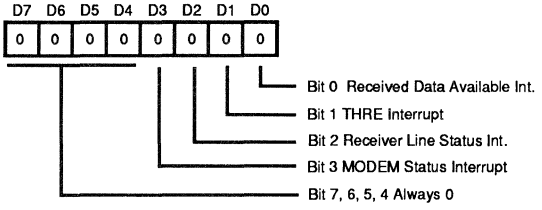


Figure 72. Interrupt Enable Register
(PC Read/Write, Address 01H)
(Z180 MPU Read Only, Address xxF1H)

Bits 7, 6, 5, 4 Reserved
These bits will always read 0 (PC and MPU).

Bit 3 Modem Status IRQ
If bits 0, 1, 2 or 3 of the Modem Status Register are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 2 Receive Line Status IRQ
If bits 1, 2, 3 or 4 of the LSR are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 1 Transmit Holding Register Empty IRQ
If bit 5 of the LSR is set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 0 Received Data Available IRQ
If bit 0 of the LSR is set or a Receive Timeout occurs and this enable bit is a logic 1, then an interrupt to the PC is generated.

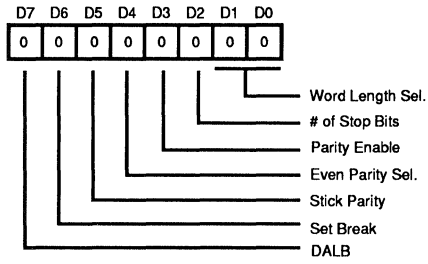


Figure 73. Line Control Register
(PC Read/Write, Address 03H)
(Z180 MPU Read Only, Address xxF3H)

Bit 7 Divisor Latch Access Bit (DALB)
This bit allow access to the divisor latch by the PC/XT/AT. If this bit is set to a one, access to the Transmitter, Receiver and Interrupt Enable Registers is disabled. When an access is made to address 0 the Divisor Latch Least Significant byte is accessed. If an access is made to address 1, the Divisor Latch Most Significant byte is accessed.

Bit 6 - Bit 0
These bits do not affect the Z80182 directly, however they can be read by the Z180 MPU and the 16550 MIMIC modes can be emulated by the Z180 MPU.

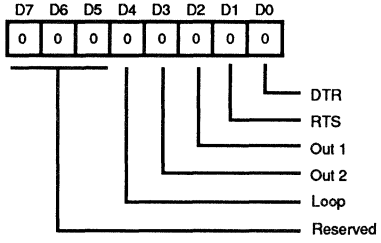


Figure 74. Modem Control Register
(PC Read/Write, Address 04H)
(Z180 MPU Read Only, Address xxF4H)

Bit 7-5 Reserved
Reserved for future use, always 0.

Bit 4 Loop
When this bit is set to a one then D3-D0 field reflects the status of Modem Status Register, as follows:
RI = Out 1
DCD = Out 2
DSR = DTR
CTS = RTS
Emulation of the loop back feature of the 16550 UART must be done by the Z180 MPU except for the above conditions.

Bit 3 Out 2
This bit controls the tri-state on the HINTR pin if bits 2 and 1 are a 10. Otherwise it can be read by the Z180 MPU.

Bit 2 -Bit 0
These bits have no direct control of the 16550 MIMIC interface and the Z180 MPU must emulate the function if it is to be implemented.

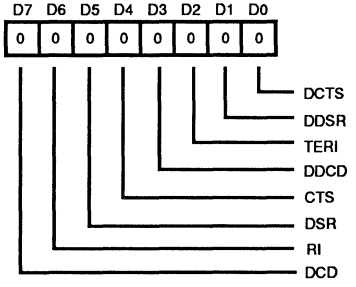


Figure 75. Modem Status Register
(PC Read Only, Address 06H)
(Z180 MPU Read/Write bits 7-4, Address xxF6H)

Bit 7 Data Carrier Detect
This bit must be written by the Z180 MPU.

Bit 6 Ring Indicator
This bit must be written by the Z180 MPU.

Bit 5 Data Set Ready
This bit must be written by the Z180 MPU.

Bit 4 Clear to Send
This bit must be written by the Z180™ MPU.

Bit 3 Delta Data Carrier Detect
This bit is set to a one whenever the Data Carrier Detect bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

Bit 2 Trailing Edge Ring Indicator
This bit is set to a one on the falling edge of the Ring Indicator bit. This bit is reset when the PC/XT/AT reads the Modem Status Register.

Bit 1 Delta Data Set Ready
This bit is set to a one whenever the Data Set Ready bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

Bit 0 Delta Clear To Send
This bit is set to a one whenever the Clear To Send bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

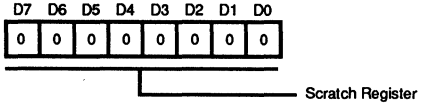


Figure 76. Scratch Register
(PC Read/Write, Address 07H)
(Z180 MPU Read Only, Address xxF7H)

Bits 7-0 Scratch Register
This register is used by the PC/XT/AT programmer for temporary data storage. The Z180 MPU is able to read this register. If the PC/XT/AT writes to this register, no interrupt to the Z180 MPU is generated.

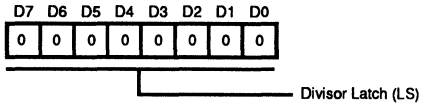


Figure 77. Divisor Latch (LS)
(PC Read/Write, Address 00H and DLAB=1)
(Z180 MPU Read Only, Address xxF8H)

Bit 7-0 Divisor Latch Most Significant Byte (MS)
This register contains the Low order byte of the Baud rate divisor. Writing to this register with the PC/XT/AT will generate an interrupt to the Z180 MPU. It can then read the Baud rate divisor and set up the application.

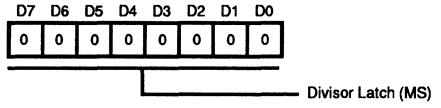


Figure 78. Divisor Latch (MS)
(PC Read/Write, Address 01H and DLAB=1)
(Z180 MPU Read Only, Address xxF9H)

Bit 7-0 Divisor Latch Most Significant Byte (MS)
This register contains the High order byte of the Baud rate divisor. Writing to this register with the PC/XT/AT will generate an interrupt to the Z180 MPU. It can then read the Baud rate divisor and set up the application.

PARALLEL PORTS REGISTERS

The Z80182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output. The Ports consist of two registers the Port Direction Control Register and the Port Data Register. The Port and direction register can be accessed in any page of I/O space since only the lowest eight address lines are decoded. Bits PC7 and PC6 are input only bits and have the special function of reading the external value of the /INT2 and /INT1 pins. Writing '1' to these bits will clear the edge detect interrupt logic when operating /INT2 and/or /INT1 in edge detect mode.

When Port B and Port C bits 5-0 are deselected in the System Configuration Register, the Data and Data Direction Registers are still available as read/write scratch registers. If a Port is deselected and if the DDR bit is a '0', then the written value to that bit will be latched and this value can be read back. If a Port is deselected and if the DDR bit is a '1', then you could read only the external pin value; any write to that bit is latched but can be read back only with DDR=0.

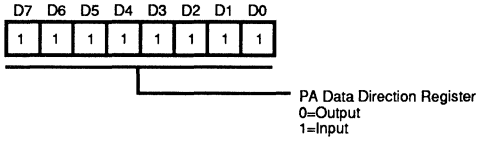


Figure 79. PA, Port A, Data Direction Register
(Z180 MPU Read/Write, Address xxEDH)

The data direction register determines which are inputs and outputs in the PA Data Register. When a bit is set to a one the corresponding bit in the PA Data Register is an input. If the bit is zero, then the corresponding bit is an output.

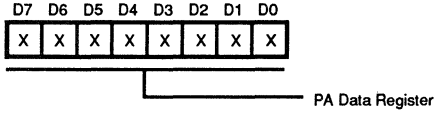


Figure 80. PA, Port A, Data Register
(Z180 MPU Read/Write, Address xxEEH)

When the Z180 MPU writes to the PA Data Register the data is stored in the internal buffer. The values of the PA Data Register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PA Data Register the data on the external pins is returned.

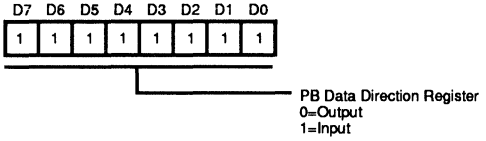


Figure 81. PB, Port B, Data Direction Register
(Z180 MPU Read/Write, Address xxE4H)

The data direction register determines which are inputs and outputs in the PB Data Register. When a bit is set to a one the corresponding bit in the PB Data Register is an input. If the bit is zero then the corresponding bit is an output.

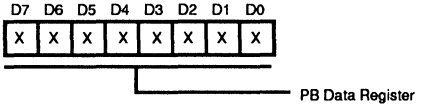


Figure 82. PB, Port B, Data Register
(Z180 MPU, Address xxE5H)

When the Z180 MPU writes to the PB Data Register the data is stored in the internal buffer. The values of Port B data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PB Data Register, the data on the external pins is returned.

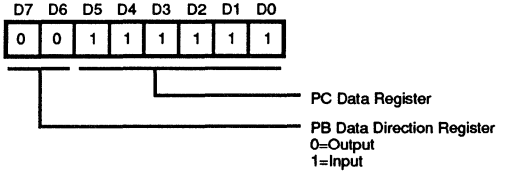


Figure 83. PC, Port C, Data Direction Register
(Z180 MPU Read/Write, Address xxDDH)

PARALLEL PORTS REGISTERS (Continued)

The data direction register determines which are inputs and outputs in the PB Data Register. When a bit is set to a one the corresponding bit in the PB Data Register is an input. If the bit is zero, then the corresponding bit is an output.

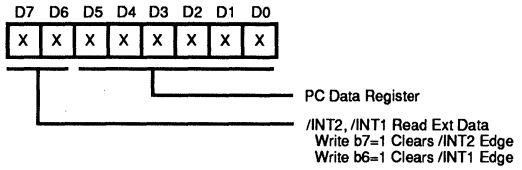


Figure 84. PC, Port C, Data Register
(Z180 MPU Read/Write, Address xxDEH)

When the Z180 MPU writes to the PC Data Register, the data is stored in the internal buffer. The values of Port C data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PC Data Register, the data on the external pins is returned.

Bits 6 and 7 serve the special function of reading the value of the external /INT2 and /INT1 lines. When operating either /INT2 or /INT1 in edge detection mode, the edge detect latch is reset by writing a '1' to bit 6 or 7 respectively. Writing a '0' has no effect.

16550 MIMIC INTERFACE DMA

The 16550 MIMIC is also able to do direct DMA with the PC/XT/AT. DMA is enabled by setting bits 3, 4 and 5 of the Master Control Register. DMA is accomplished by using the two DMA pins and the Transmitter Holding and Receive Data Registers.

If bit 5 is a one, the /HTxRDY pin is equal to the complement of the Transmit Holding Register Empty bit. If bit 5 is a one and bit 3 is a zero the external /DREQ1 pin of the Z180 MPU is disabled and the internal /DREQ1 is equal to the complement of the Transmit Holding Register Empty Shadow bit. If bit 5 is a one and bit 3 is a one the external /DREQ0 pin of the Z180 MPU is disabled and the internal /DREQ0 is equal to the complement of the Transmit Holding Register Empty Shadow bit.

If bit 4 is a one, then the /HRxRDY pin is equal to the complement of the Data Ready bit. If bit 4 is a one and bit 3 is a zero the external /DREQ0 pin of the Z180 MPU is disabled and the internal /DREQ0 is equal to the complement of the Data Ready Shadow bit. If bit 4 is a one and bit 3 is a one the external /DREQ1 pin of the Z180 MPU is disabled and the internal /DREQ1 is equal to the complement or the Data Ready Shadow bit.

Z80182 MIMIC DMA CONSIDERATIONS

For the PC Interface, the 16550 device has two modes of operation that need to be supported by the MIMIC. In single transfer mode, the DMA request line for the receiver goes active whenever there is at least one character in the RCVR FIFO. For the transmitter, the DMA request line is active on an empty XMIT FIFO and inactive on non-empty.

In multi-transfer mode, the RCVR DMA goes active at the trigger level and inactive on RCVR FIFO empty. The XMIT DMA is active on non-full XMIT FIFO and inactive on a full XMIT FIFO.

Bit 3 in the FCR controls the DMA mode for the PC interface. If a '1' is programmed into this bit, multi-byte DMA is enabled. A '0' in this bit (default) enables single byte DMA.

As specified, the 16550 does not have any means of handling the error status bits in the FIFO in this multi-transfer mode. Such DMA transfers would require blocks with some checksum or other error checking scheme.

For the MPU interface, the DMA is controlled by a non-empty transmit FIFO and by a non-full receive FIFO conditions (THRE and the DR bits in the LSR). If the delay timers are enabled, the respective shadow bits are used for DMA control. The effect of the DMA logic is to request DMA service when at least one byte of data is available to be read or written to the FIFO's by the Z180. The Z180's DMA channel can be programmed to trigger on edge or on level.

EMULATION MODES

The Z80182 provides four modes of operation. The modes are selected by the EV1 and EV2 pins. These four modes allow the system development and commercial production to be done with the same device. The four emulation modes are shown in Table 20.

Table 20. EV2 and EV1, Emulation Mode Control

	EV2	EV1	EV Description
Mode 0	0	0	Normal Mode, on-chip Z180 bus master
Mode 1	0	1	Emulation Adapter Mode
Mode 2	1	0	Emulator Probe Mode
Mode 3	1	1	RESERVED, for Test Use Only

Mode 0 Normal Mode
This is the normal operating mode for the Z80182.

Mode 1 Emulation Adapter Mode
The Emulation Adaptor Mode enables system development for the Z182 with a readily available Z180 emulator. The Emulator provides the Z180™ MPU and Z180 peripheral functions to the target system, with their signals passing through the emulation adapter. In Emulation Adaptor Mode the Z182s, Z180 MPU and Z180 peripheral signals are tri-state or physically disconnected. The Z182 continues to provide its ESCC, MIMIC and Port functions and signals to the target system. The Mode 1 effects on the Z182 are shown in Table 21.

EMULATION MODES (Continued)

Table 21. Emulation Mode 1

	Mode 0	Mode 1
Signal	Normal	Emulation Adaptor
CLK	Output	Input
/M1	Output	Input
/MREQ,/MRD	Output	Input
/IORQ	Output	Input
/RD	Output	Input
/WR	Output	Input
/RFSH	Output	Input
/HALT	Output	Input
ST	Output	Input
E	Output	tri-state
/BUSACK	Output	Input
/WAIT	Input	Output
A19,A18/T_{OUT}	Output	Input
A17-A0	Output	Input
D7-D0	Input/Output	Input/Output
TxA0.	Output	Tri-state
/RTS0	Output	Tri-state
TxA1	Output	Tri-state
/INT0	Input	Output, Open Drain

Mode 2 Emulation Probe Mode
In the Emulator Probe Mode all of the Z182 output signals are tri-state. This scheme allows a Z182 emulator probe to grab on to the Z182 package leads on the target system.

Mode 3 RESERVED, for Test Purposes Only
This mode is reserved for test purpose only, do not use.

Note: Z182 has 2 branches of reset. /RESET controls the Z182 overall configuration, RAM and ROM boundaries, plus the ESCC, Port and the 16550 MIMIC interface. Reset to the Z180 is a logical OR of the /RESET input in Mode 1 and Mode 2. Note also that the Z180's crystal oscillator feedback resistor is disabled in Mode 1 and Mode 2.

Note that in Mode 1 the emulator must provide /MREQ on the (/MREQ,/MRD) Z80182 pin (not /MRD); and A18 (not T_{OUT}) on the A18/T_{OUT} pin.

SLEEP, HALT EFFECT ON MIMIC AND 182 SIGNALS

The Following Z80182 signals are driven High when Z180™ MPU enters a SLEEP or HALT State:

/MRD when selected in the Interrupt Edge/Pin MUX Register.

/MWR when selected in the Interrupt Edge/Pin MUX Register.

/ROMCS,/RAMCS always High in SLEEP or HALT.

The following signals are High-Z during SLEEP and HALT:

/IOCS when so selected in the Interrupt Edge/Pin MUX Register.

/RD and /WR.

A0-A19 (A18 if selected) always High-Z in power down.

D0-D7 always High-Z in power down modes.

The MIMIC logic of the 182 is disabled during power down modes of the Z180.

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} with respect to V_{SS} .....-0.3V to +7.0V
Voltages on all inputs
with respect to V_{SS} .....-0.3V to V_{CC} +0.3V
Operating Ambient Temperature .....0 to 70°C
Storage Temperature .....-55°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

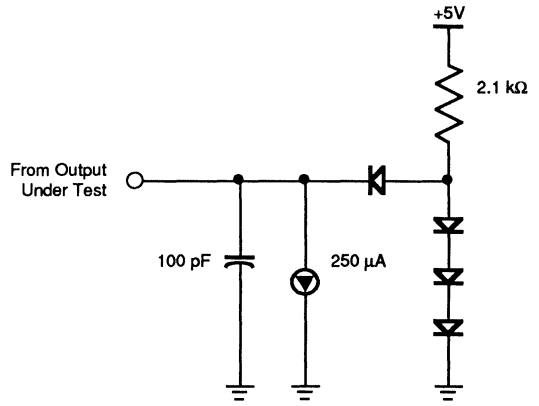
STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Test Load Diagram).

Available operating temperature range is:
S = 0°C to +70°C

Voltage Supply Range:
+4.50V ≤ V_{CC} ≤ + 5.50V

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pF.



Test Load Diagram

DC CHARACTERISTICS

Z80182

(V_{CC} = 5V ±10%, V_{SS} = 0V, over specified temperature range unless otherwise notes.)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH1}	Input H Voltage /RESET, EXTAL	V_{CC} -1.0		V_{CC} +0.3	V	
V_{IH2}	Input H Voltage Except /RESET, EXTAL	2.0		V_{CC} +0.3	V	
V_{IL1}	Input L Voltage /RESET, EXTAL	-0.3		0.6	V	
V_{IL2}	Input L Voltage Except /RESET, EXTAL	-0.3		0.8	V	
V_{OH1}	Output H Voltage All outputs	2.4 V_{CC} - 1.2			V	I_{OH} = -250 µA I_{OH} = -25 µA
V_{OH2}	Output H PHI	V_{CC} -1.0			V	I_{OH}=-250 µA
V_{OL1}	Output L Voltage All outputs			0.40	V	I_{OL} = 2.0 mA
V_{OL2}	Output L PHI			0.40	V	I_{OL}= 2.0 mA
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL			10	µA	V_{IN} = 0.5 - V_{CC} -0.5
I_{TL}	Tri-state Leakage Current			10	µA	V_{IN} = 0.5 - V_{CC} -0.5
I_{CC}*	Power Dissipation*		60	125	mA	f = 20 MHz
	(Normal Operation)		50	100	mA	f = 16 MHz
	Power Dissipation*		12	25	mA	f = 20 MHz
	(SYSTEM STOP mode)		9	20	mA	f = 16 MHz
	IDLE Mode		6	12	mA	f = 20 MHz
			5	10	mA	f = 16 MHz
	STANDBY Mode		10	10	µA	f = 20 MHz
			10	10	µA	f = 16 MHz
Cp	Pin Capacitance			12	pF	V_{IN} = 0V, f = 1 MHz T_A = 25°C

Notes:

* V_{IH} Min = V_{CC} -1.0V, V_{IL} Max = 0.8V (all output terminals are at no load)
  V_{CC} = 5.0V

These ICC values are preliminary and subject to change without notice.

TIMING DIAGRAMS
Z180 MPU Timing

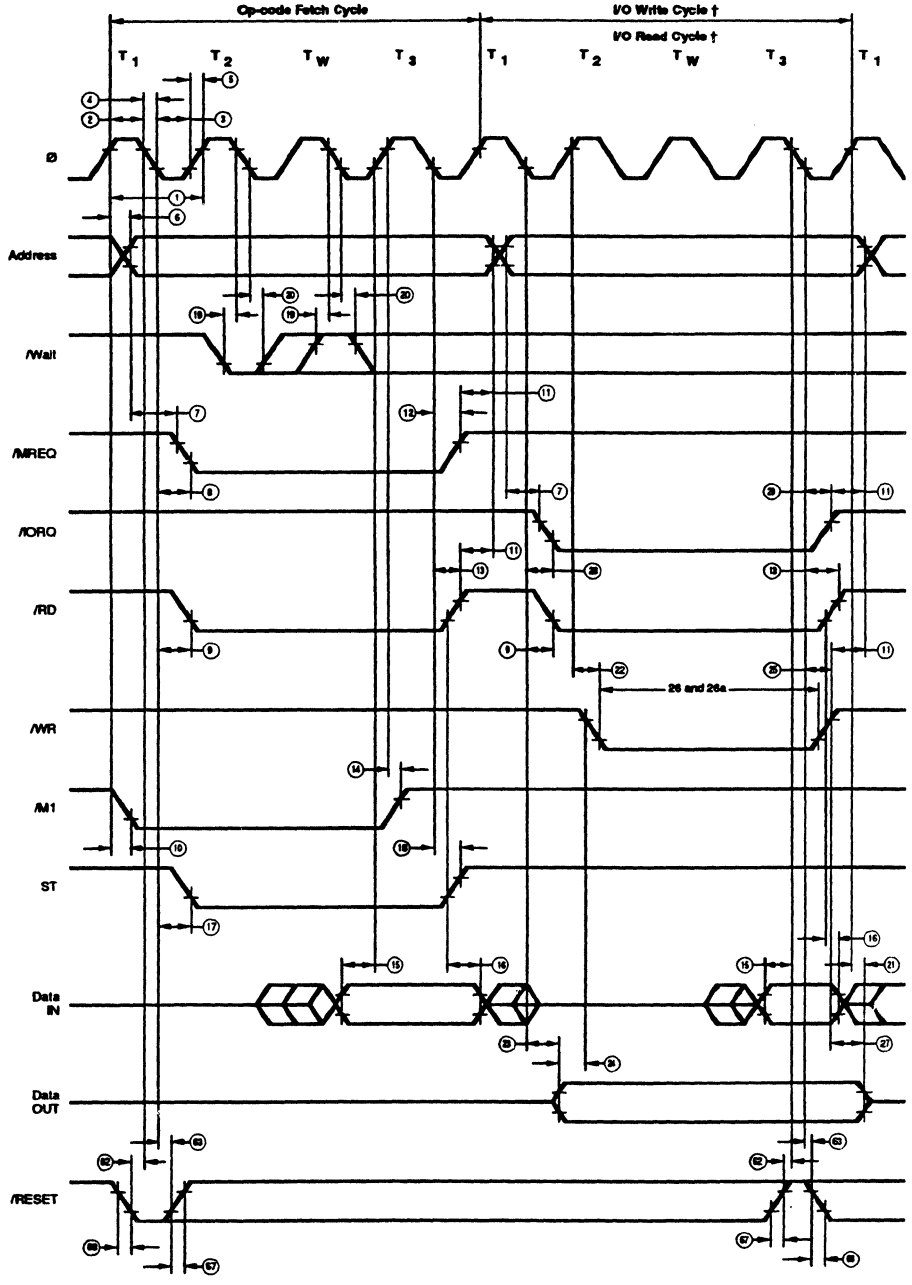


Figure 85. CPU Timing
(Opcode Fetch Cycle, Memory Read/Write Cycle
I/O Read/Write Cycle)

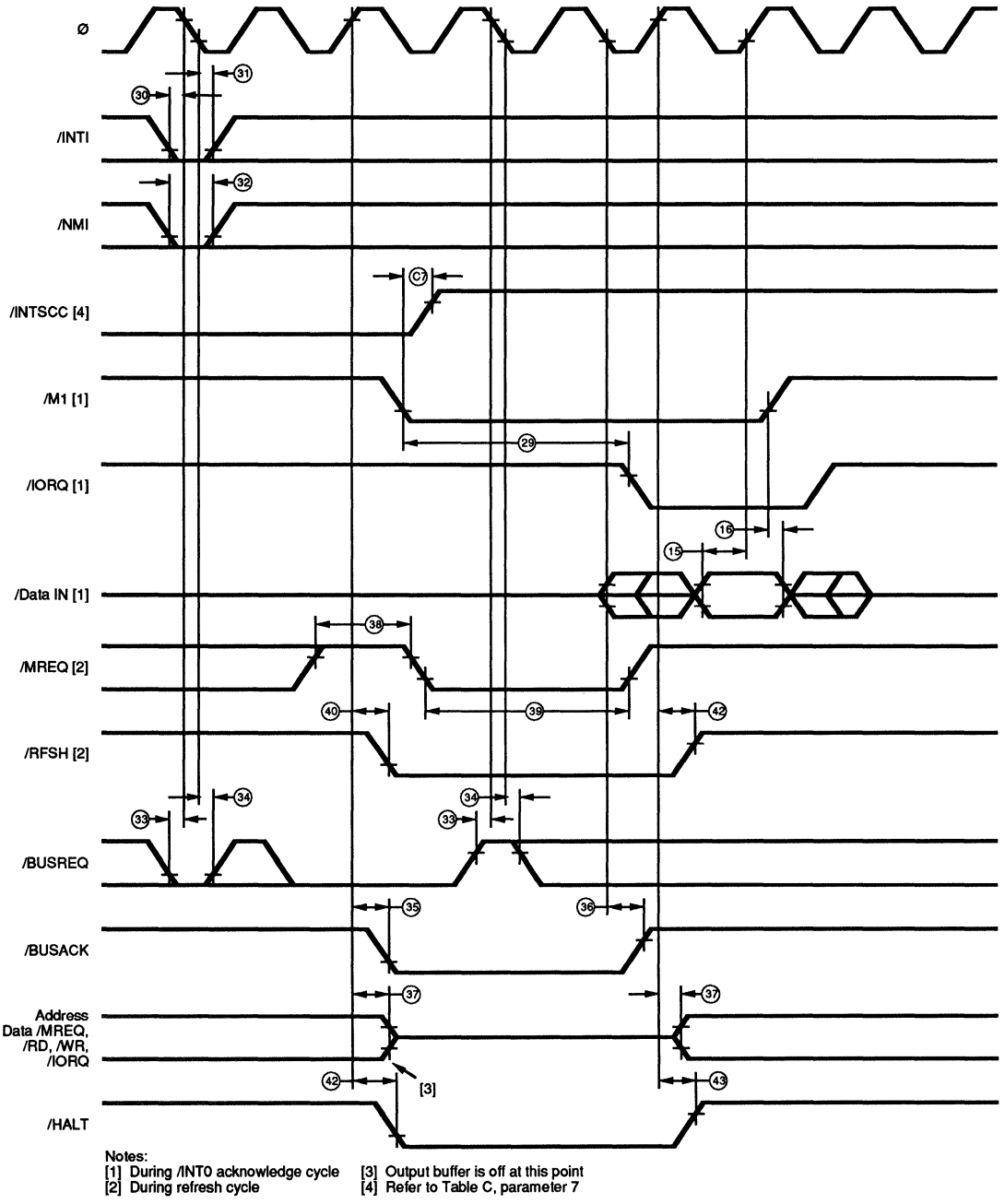


Figure 86. CPU Timing
(/INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode
HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

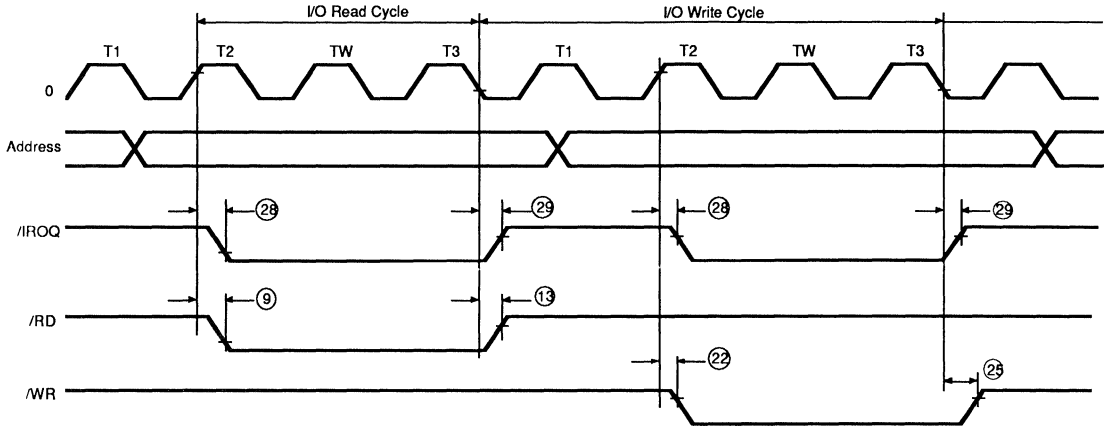
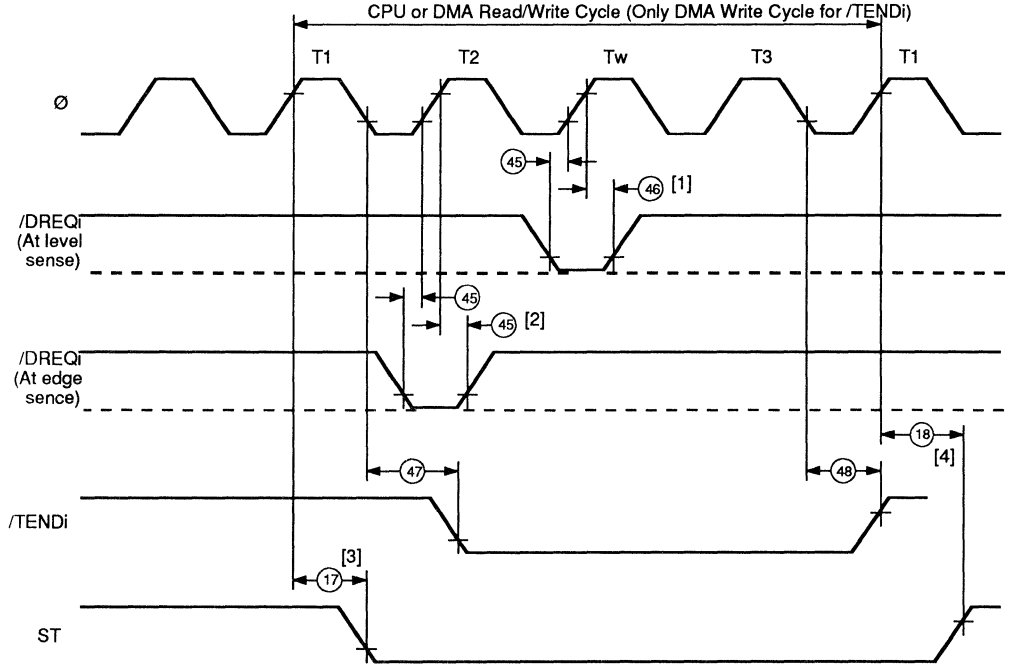


Figure 87. CPU Timing



DMA Control Signals
[1] tDRQS and tDRQH are specified for the rising edge of clock followed by T3.
[2] tDRQS and tDRQH are specified for the rising edge of clock.
[3] DMA cycle starts.
[4] CPU cycle starts.

Figure 88. DMA Control Signals

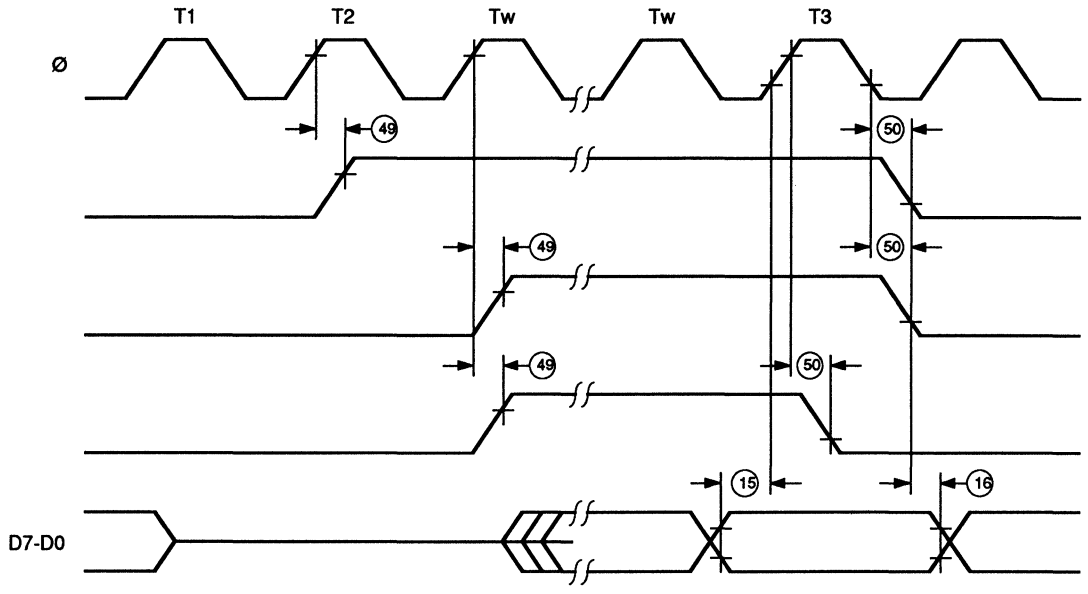


Figure 89. E Clock Timing
(Memory Read/Write Cycle
I/O Read/Write Cycle)

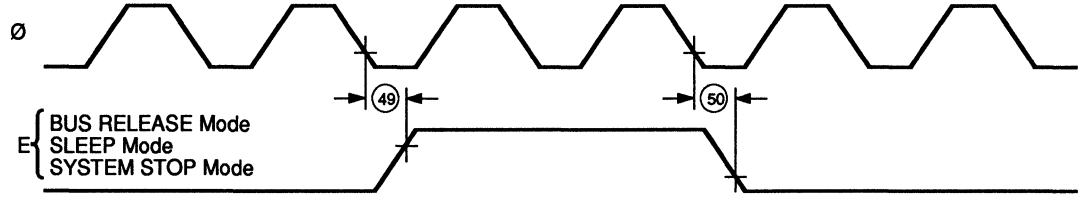


Figure 90. E Clock Timing

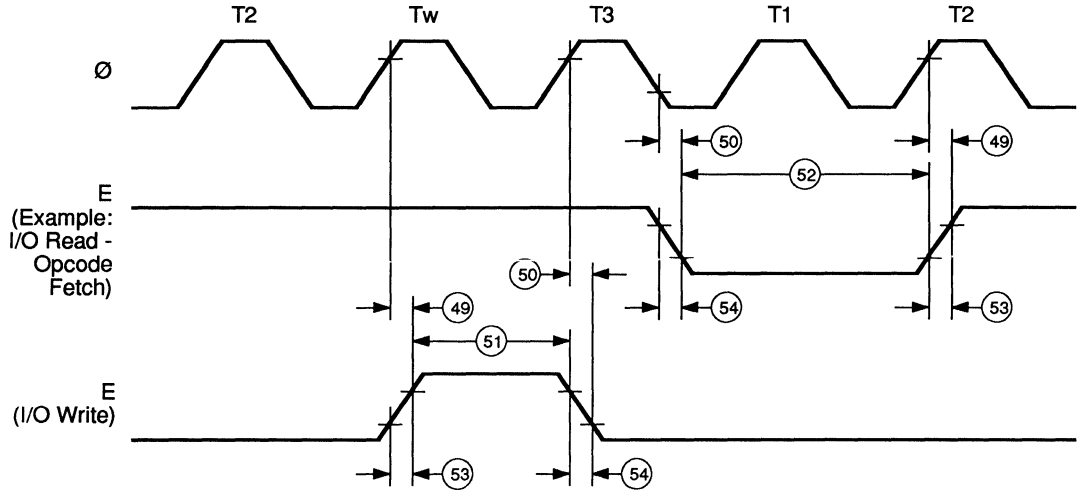


Figure 91. E Clock Timing
(Minimum timing example
of PWEL and PWEH)

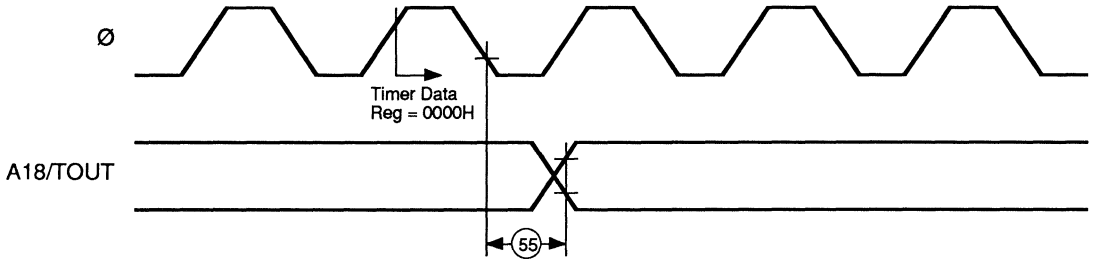


Figure 92. Timer Output Timing

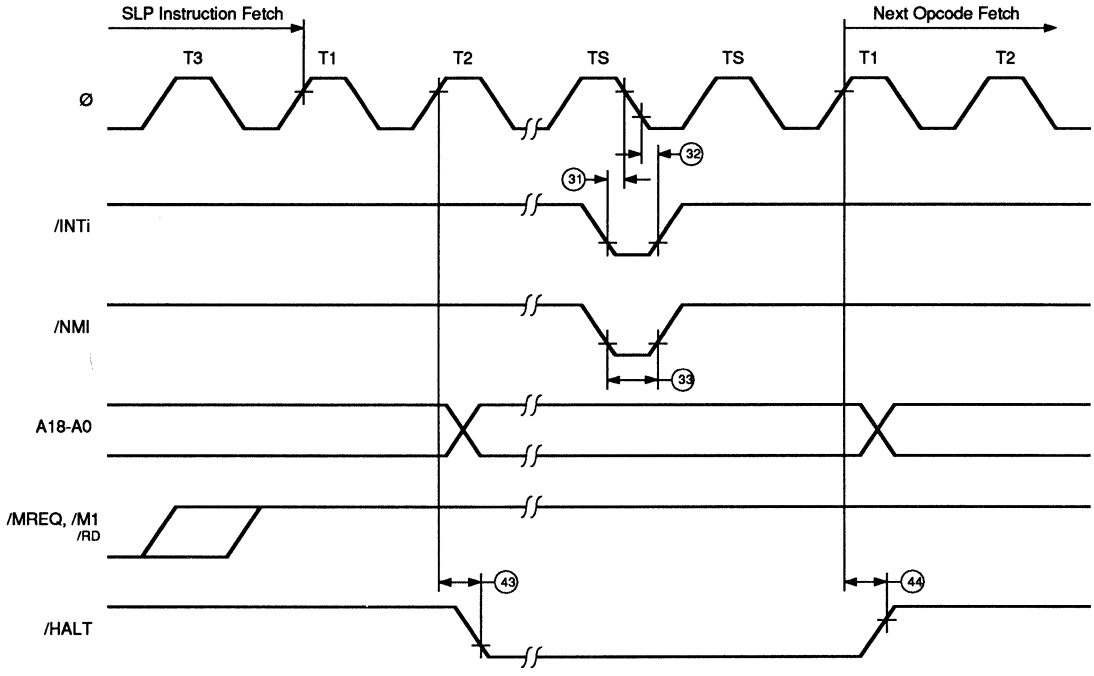


Figure 93. SLEEP Execution Cycle

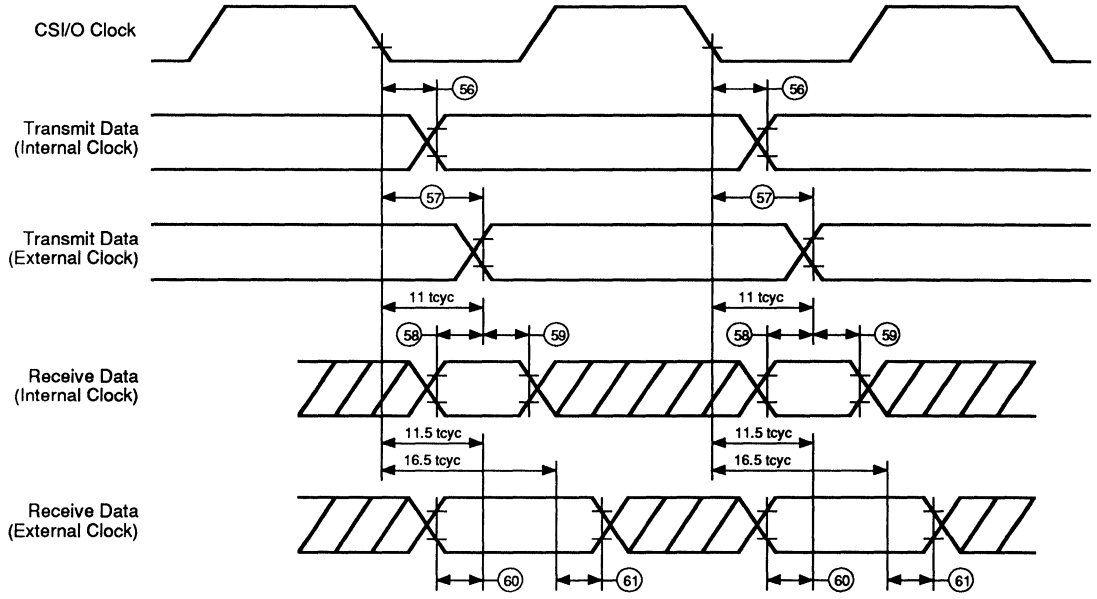


Figure 94. CSI/O Receive/Transmit Timing

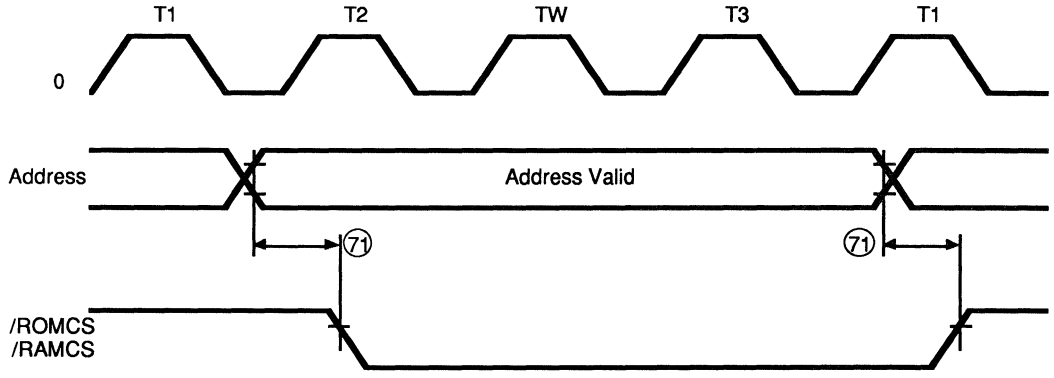


Figure 95. /ROMCS and /RAMCS Timing

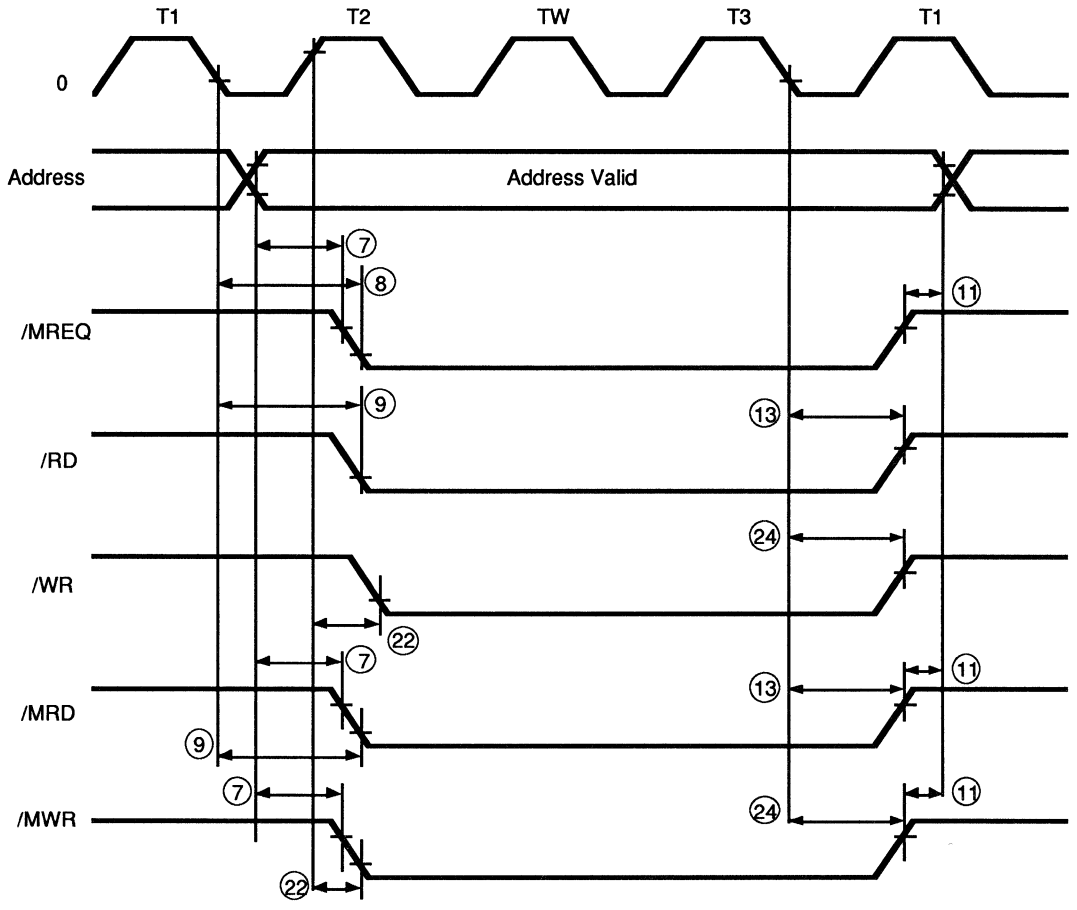


Figure 96. /MWR and /MRD Timing

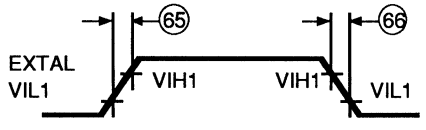


Figure 97. External Clock Rise Time and Fall Time

Figure 98. Input Rise and Fall Time
(Except EXTAL, /RESET)

Z8S180 AC CHARACTERISTICS

Table A. Z8S180 CPU & Z8S180 Peripherals Timing

No	Sym	Parameter	Z8S18016 Min	Z8S18016 Max	Z8S18020 Min	Z8S18020 Max	Unit	Note
1	tcyc	Clock Cycle Time	62	DC	50	DC	ns	[1]
2	tCHW	Clock Pulse Width (High)	25	DC	20	DC	ns	[1]
3	tCLW	Clock Pulse Width (Low)	25	DC	20	DC	ns	[1]
4	tcf	Clock Fall Time		6		5	ns	[1]
5	tcr	Clock Rise Time		6		5	ns	[1]
6	tAD	Address Valid from Clock Rise		35		30	ns	
7	tAS	Address Valid to /MREQ, /IORQ, /MRD Fall	5		5		ns	
8	tMED1	Clock Fall to /MREQ Fall Delay		25		25	ns	
9	tRDD1	Clock Fall to /RD, /MRD (/IOC=1)		25		25	ns	
		Clock Rise to /RD, /MRD Fall (/IOC=0)		25		25	ns	
10	tM1D1	Clock Rise to /M1 Fall delay		45		35	ns	
11	tAH	Address Hold time (/MREQ, /IORQ, /RD, /WR/MRD)	5		5		ns	
12	tMED2	Clock Fall to /MREQ Rise Delay		30		25	ns	
13	tRDD2	Clock Fall to /RD, /MRD Rise Delay		30		25	ns	
14	tM1D2	Clock Rise to /M1 Rise Delay		45		40	ns	
15	tDRS	Data Read Setup Time	15		10		ns	
16	tDRH	Data Read Hold Time	0		0		ns	
17	tSTD1	Clock Edge to ST Fall		35		30	ns	
18	tSTD2	Clock Edge to ST Rise		35		30	ns	
19	tWS	/WAIT Setup Time to Clock Fall	15		15		ns	[2]
20	tWH	/WAIT Hold Time from Clock Fall	10		10		ns	
21	tWDZ	Clock Rise to Data Float Delay		40		35	ns	
22	tWRD1	Clock Rise to /WR,/MWR Fall Delay		25		25	ns	
23	tWDD	Clock Fall to Write Data Delay		30		25	ns	
24	tWDS	Write Data Setup Time to /WR,/MWR Fall	10		10		ns	
25	tWRD2	Clock Fall to /WR Rise		30		25	ns	
26	tWRP	/WR Pulse Width (Memory Write Cycles)	80		80		ns	
26a		/WR Pulse Width (I/O Write Cycles)	150		150		ns	
27	tWDH	Write Data Hold Time from /WR Rise	10		10		ns	
28	tIOD1	Clock Fall to /IORQ Fall Delay (/IOC=1)		30		25	ns	
		Clock Rise to /IORQ Fall Delay (/IOC=0)		30		25	ns	
29	tIOD2	Clock Fall /IOQR Rise Delay		30		25	ns	
30	tIOD3	/M1 Fall to /IORQ Fall Delay	120		100		ns	
31	tINTS	/INT Setup Time to Clock Fall	20		20		ns	
32	tINTH	/INT Hold Time from Clock Fall	10		10		ns	
33	tNMIW	/NMI Pulse Width	40		35		ns	
34	tBRS	/BUSREQ Setup Time to Clock Fall	10		10		ns	
35	tBRH	/BUSREQ Hold Time from Clock Fall	10		10		ns	
36	tBAD1	Clock Rise to /BUSACK Fall Delay		30		25	ns	
37	tBAD2	Clock Fall to /BUSACK Rise Delay		30		25	ns	
38	tBZD	Clock Rise to Bus Floating Delay Time		45		40	ns	
39	tMEWH	/MREQ Pulse Width (High)	45		35		ns	
40	tMEWL	/MREQ Pulse Width (Low)	45		35		ns	

Table A. Z8S180 CPU & Z8S180 Peripherals Timing (Continued)

No	Sym	Parameter	Z8S18016 Min	Z8S18016 Max	Z8S18020 Min	Z8S18020 Max	Unit	Note
41	tRFD1	Clock Rise to /RFSH Fall Delay		25		20	ns	
42	tRFD2	Clock Rise to /RFSH Rise Delay		25		20	ns	
43	tHAD1	Clock Rise to /HALT Fall Delay		20		15	ns	
44	tHAD2	Clock Rise to /HALT Rise Delay		20		15	ns	
45	tDRQS	/DREQi Setup Time to Clock Rise	20		20		ns	
46	tDRQH	/DREQi Hold Time from Clock Rise	20		20		ns	
47	tTED1	Clock Fall to /TENDi Fall Delay		30		25	ns	
48	tTED2	Clock Fall to /TENDi Rise Delay		30		25	ns	
49	tED1	Clock Rise to E Rise Delay		35		30	ns	
50	tED2	Clock Edge to E Fall Delay		35		30	ns	
51	PWEH	E Pulse Width (High)	30		25		ns	
52	PWEL	E Pulse Width (Low)	60		50		ns	
53	tEr	Enable Rise Time		10		10	ns	
54	tEf	Enable Fall Time		10		10	ns	
55	tTOD	Clock Fall to Timer Output Delay		100		75	ns	
56	tSTDI	CSI/O Tx Data Delay Time (Internal Clock Operation)		100		75	ns	
57	tSTDE	CSI/O Tx Data Delay Time (External Clock Operation)		7.5 tcyc +100		7.5 tcyc+75	ns	
58	tSRSI	CSI/O Rx Data Setup Time (Internal Clock Operation)	1		1		tcyc	
59	tSRHI	CSI/O Rx Data Hold Time (Internal Clock Operation)	1		1		tcyc	
60	tSRSE	CSI/O Rx Data Setup Time (External Clock Operation)	1		1		tcyc	
61	tSRHE	CSI/O Rx Data Hold Time (External Clock Operation)	1		1		tcyc	
62	tRES	/RESET Setup time to Clock Fall	45		40		ns	
63	tREH	/RESET Hold time from Clock Fall	30		25		ns	
64	tOSC	Oscillator Stabilization Time		20		20	ms	
65	tEXr	External Clock Rise Time (EXTAL)		6		5	ns	
66	tEXf	External Clock Fall Time (EXTAL)		6		5	ns	
67	tRr	/RESET Rise Time		50		50	ms	[2]
68	tRf	/RESET Fall Time		50		50	ms	[2]
69	tIr	Input Rise Time (Except EXTAL, /RESET)		50		50	ns	[2]
70	tIf	Input Fall Time (Except EXTAL, /RESET)		50		50	ns	[2]
71	TdCS	Address Valid to /ROMCS, /RAMCS Valid Delay		20		20		

Notes:
[1] tcyc=tCHW+tCLW+tcf+tcr
[2] This parameter has to be modified if other specification(s) can not be met.
These AC parameters values are preliminary and subject to change without notice.

ESCC Timing

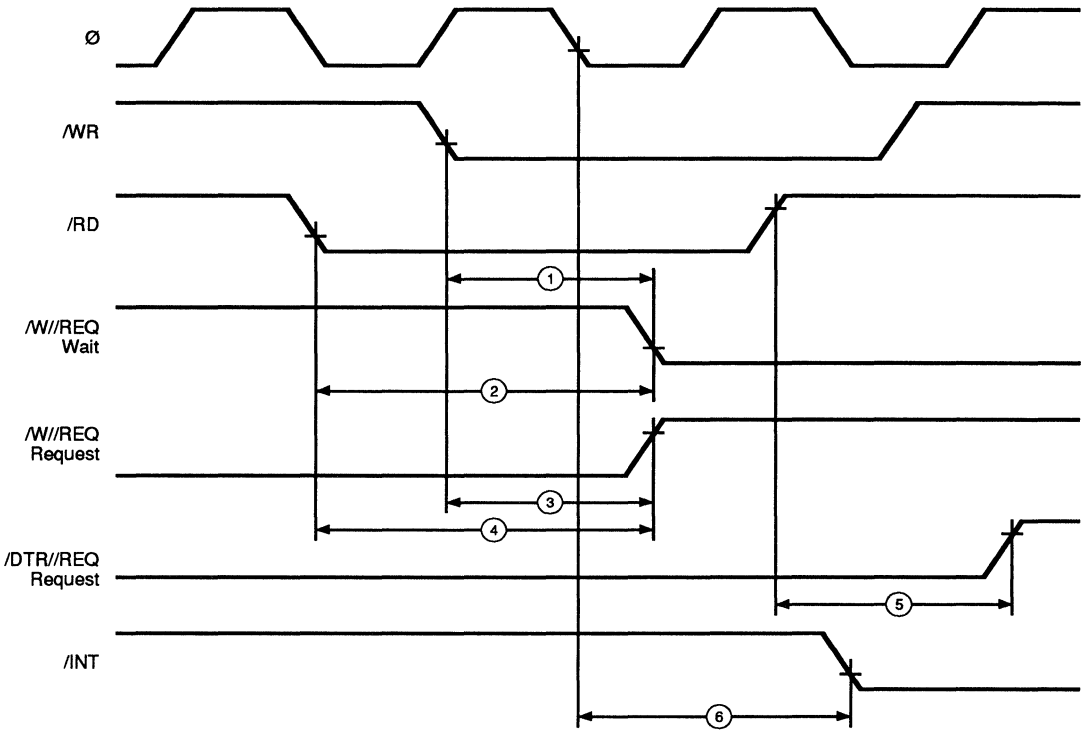


Figure 99. ESCC AC Parameter

Table B. ESCC Timing Parameters

No	Symbol	Parameter	Z8018216 Min	Z8018216 Max	Z8018220 Min	Z8018220 Max	Unit
1.	TdWR(W)	/WR Fall to Wait Valid Delay		50		50	ns
2	TdRD(W)	/RD Fall to Wait Valid Delay		50		50	
3	TdWRf(REQ)	/WR Fall to /W//REQ Not Valid Delay		70		65	
4	TdRDf(REQ)	/RD Fall to /W//REQ Not Valid Delay		70		65	
5	TdRdr(REQ)	/RD Rise to /DTR//REQ Not Valid Delay		TBD		TBD	
6	TdPC(INT)	Clock to /INT Valid Delay		175		160	

Z85230 General Timing Diagram

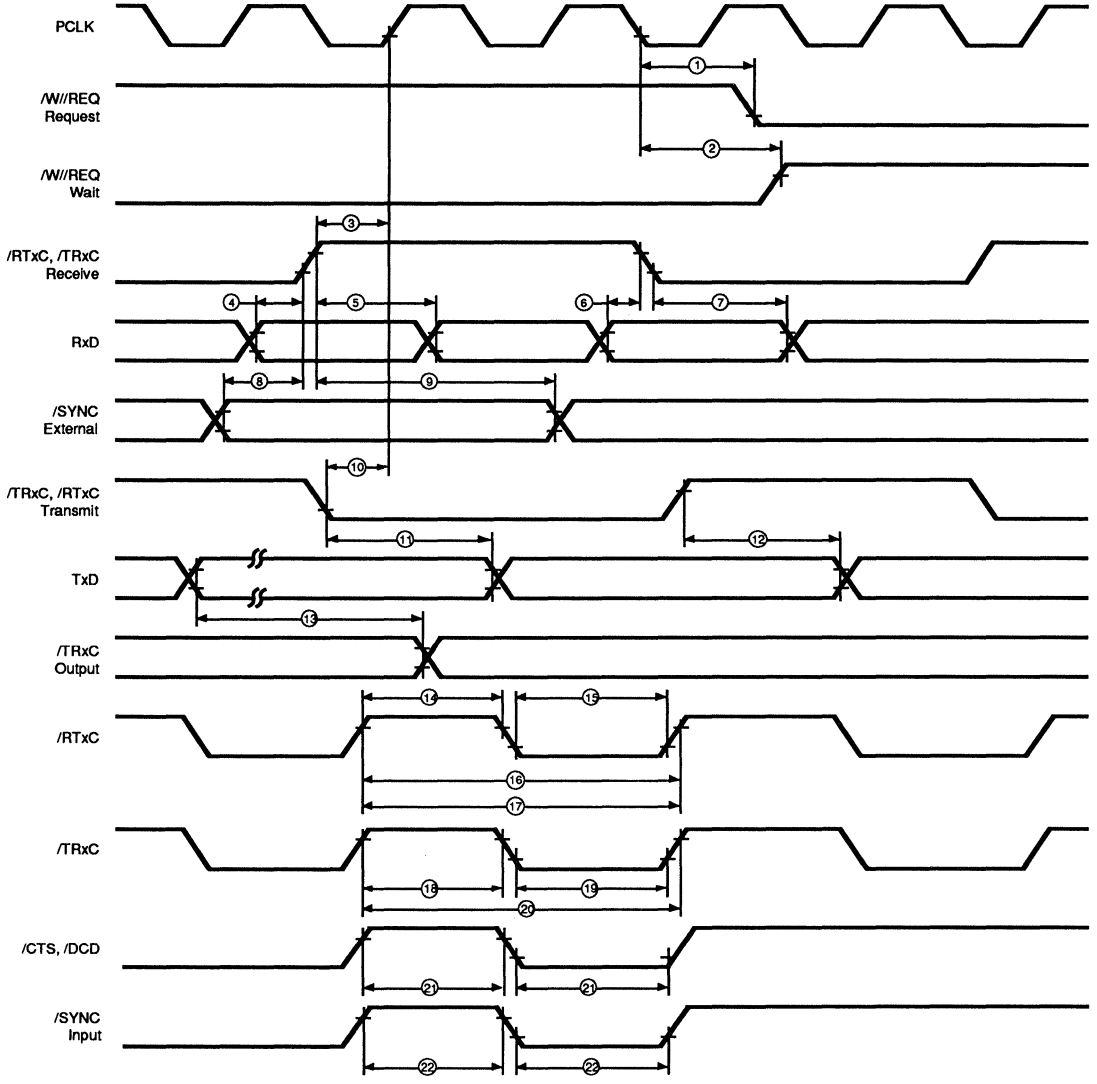


Figure 100. General Timing Diagram

Table C. Z85230 General Timing Table

No	Symbol	Parameter	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max	Notes
1	TdPC(REQ)	/PCLK to W/REQ Valid		80		70	
2	TdPC(W)	/PCLK to Wait Inactive		180		170	
3	TsRxC(PC)	/RxC to /PCLK Setup Time	NA		NA		[1,4]
4	TsRxD(RxCr)	RxD to /RxC Setup Time		0		0	[1]
5	ThRxD(RxCr)	RxD to /RxC Hold Time	50		45		[1]
6	TsRxD(RxCf)	RxD to /RxC Setup Time	0		0		[1,5]
7	ThRxD(RxCf)	RxD to /RxC Hold Time	50		45		[1,5]
8	TsSY(RxC)	/SYNC to /RxC Setup Time	-100		-90		[1]
9	ThSY(RXC)	/SYNC to/RxC Hold Time	5TcPc		5TcPc		[1]
10	TsTxC(PC)	/TxC to /PCLK Setup Time	NA		NA		[2,4]
11	TdTxCf(TXD)	/TxC to TxD Delay		80		70	[2]
12	TdTxCr(TXD)	/TxC to TxD Delay		80		70	[2,5]
13	TdTxD(TRX)	TxD to TRxC Delay		80		70	
14	TwRTxh	RTxC High Width	80		70		[6]
15	TwRTxl	TRxC Low Width	80		70		[6]
16a	TcRTx	RTxC Cycle Time	244		200		[6,7]
16b	TxRx(DPLL)	DPLL Cycle Time Min	31		31		[7,8]
17	TcRTxx	Crystal OSC. Period	61	1000	61	1000	[3]
18	TwTRxh	TRxC High Width	80		70		[6]
19	TwTRxl	TRxC Low Width	80		70		[6]
20	TcTRx	TRxC Cycle Time	244		200		[6,7]
21	TwExT	DCD or CTS Pulse Width	70		60		
22	TwSY	SYNC Pulse Width	70		60		

Notes:

[1] RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
[2] TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
[3] Both /RTxC and /SYNC have 30 pF capacitors to ground connected to them.
[4] Synchronization of RxC to PCLK is eliminated in divide by four operation.
[5] Parameter applies only to FM encoding/decoding.
[6] Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
[7] The maximum receive or transmit data rate is 1/4 PCLK.
[8] Applies to DPLL clock source only. Maximum data rate of 1/4 PCLK still applies. DPLL clock should have a 50% duty cycle.

These AC parameter values are preliminary and subject to change without notice.

Z85230 System Timing Diagram

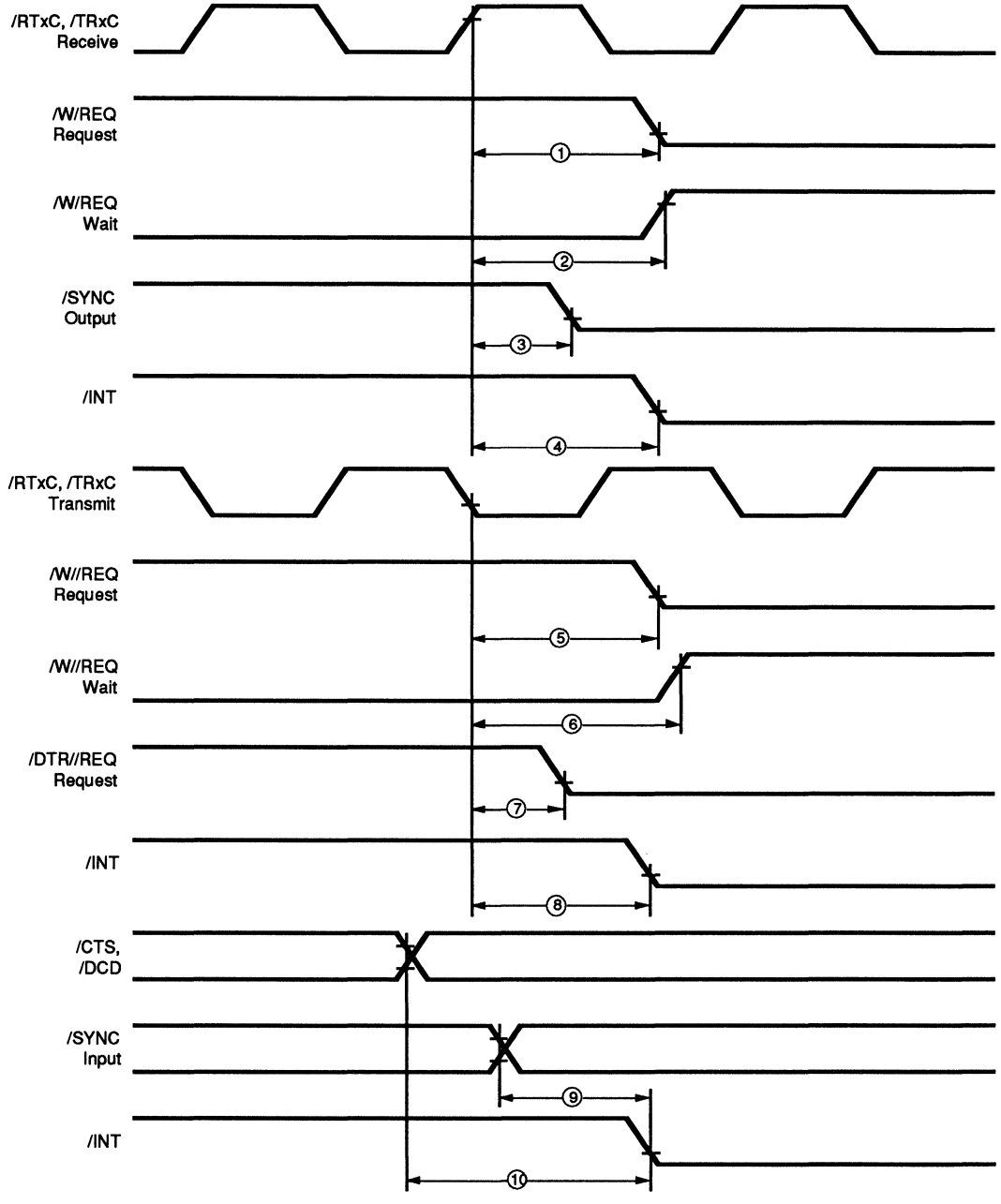


Figure 101. Z85230 System Timing

Table D. Z85230 System Timing Table

No	Symbol	Parameter	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max	Notes [4]
1	TdRxC(REQ)	/RxC to /W//REQ Valid	13	17	13	18	[2]
2	TdRxC(W)	/RxC to /Wait Inactive	13	17	13	18	[1,2]
3	TdRxC(SY)	/RxC to /SYNC Valid	9	12	9	13	[2]
4	TdRxC(INT)	/RxC to /INT Valid	15	21	15	22	[1,2]
5	TdTxC(REQ)	/TxC to /W//REQ Valid	8	11	8	12	[3]
6	TdTxC(W)	/TxC to /Wait Inactive	8	14	8	15	[1,3]
7	TdTxC(DRQ)	/TxC to /DTR//REQ Valid	7	10	7	11	[3]
8	TdTxC(INT)	/TxC to /INT Valid	9	13	9	14	[1,3]
9	TdSY(INT)	/SYNC to /INT Valid	2	6	2	6	[1]
10	TdExT(INT)	/DCD or /CTS to /INT Valid	3	8	3	9	[1]

Notes:

[1] Open drain-output, measured with open-drain test load.
[2] /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
[3] /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
[4] Units equal to TcPc
These AC parameters are preliminary and are subject to change without notice.

General Purpose I/O Port Timing

Figure 102 shows the timing for the Ports A, B and C. Parameters referred to in this figure appear in Table E.

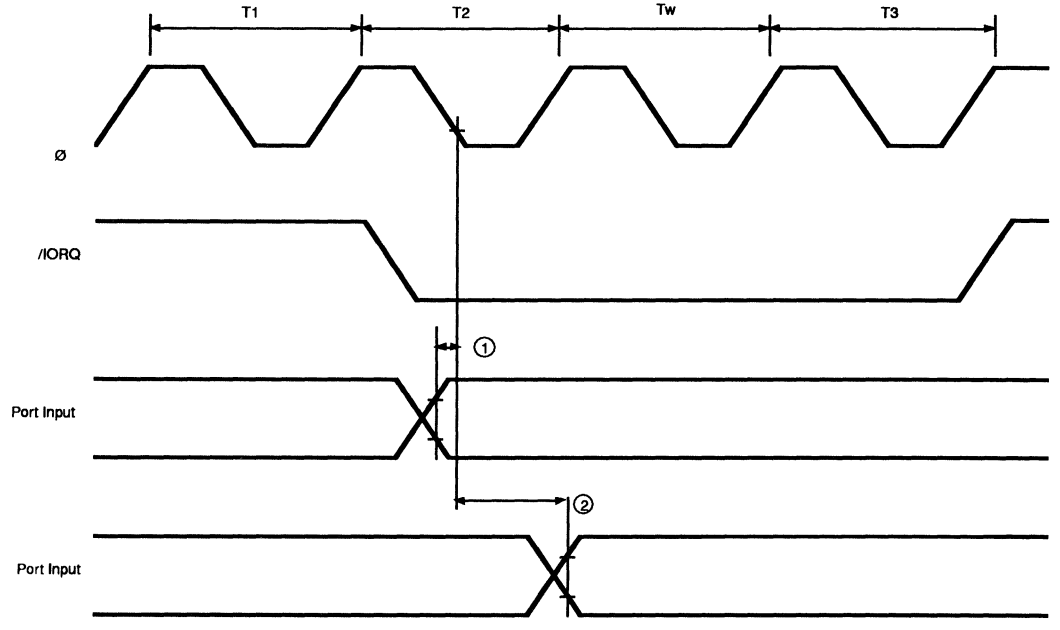


Figure 102. PORT Timing

AC CHARACTERISTICS (Continued)

Table E. PORT General Purpose I/O Timing Parameters

No	Symbol	Parameter	Z8018216 Min	Z8018216 Max	Z8018220 Min	Z8018220 Max	Unit
1	TsPIA(C)	PORT Data Setup time to Clock Fall	20		20		ns
2	TdCr(PIA)	Clock Fall to PORT Data Valid Delay		60		60	ns

These AC parameter values are preliminary and are subject to change without notice.

Read Write External Bus Master Timing

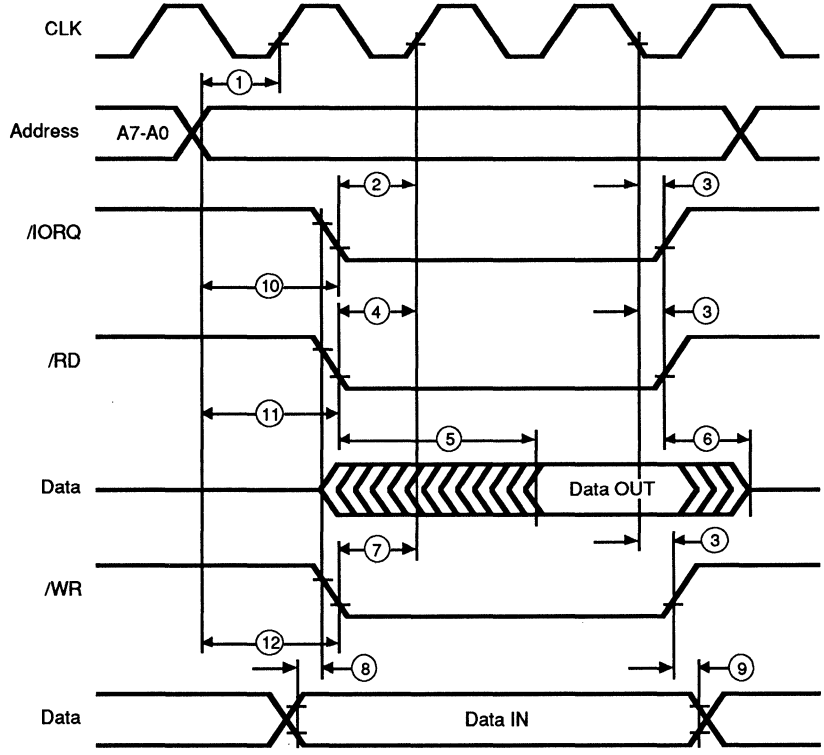


Figure 103. Read/Write External Bus Master Timing

Table F. External Bus Master Interface Timing (Read/Write Cycles)

No	Symbol	Parameter	Z8018216		Z8018220	
			Min	Max	Min	Max
1	TsA(Cr)	Address to CLK Rise Setup Time	20		20	
2	TsIO(Cr)	/IORQ Fall to CLK Rise Setup Time	20		20	
3	Th	Hold Time	0		0	
4	TsRD(Cr)	/RD Fall to CLK Rise Setup Time	20		20	
5	TdRD(DO)	/RD Fall to Data Out Delay		50		45
6	TdRIr(DOz)	/RD, /IORQ Rise to Read Data Float	0		0	
7	TsWR(Cr)	/WR Fall to CLK Rise Setup Time	20		20	
8	TsDi(WRf)	Data in to /WR Fall Setup Time	0		0	
9	ThWIr(Di)	/IORQ, /WR Rise to Data In Hold Time	0		0	
10	TsA(IORQf)	Address to /IORQ Fall Setup Time	40		35	
11	TsA(RDf)	Address to /RD Fall Setup Time	40		35	
12	TsA(WRf)	Address to /WR Fall Setup Time	40		35	

These AC parameter values are in preliminary and are subject to change without notice.

ESCC External Bus Master Timing

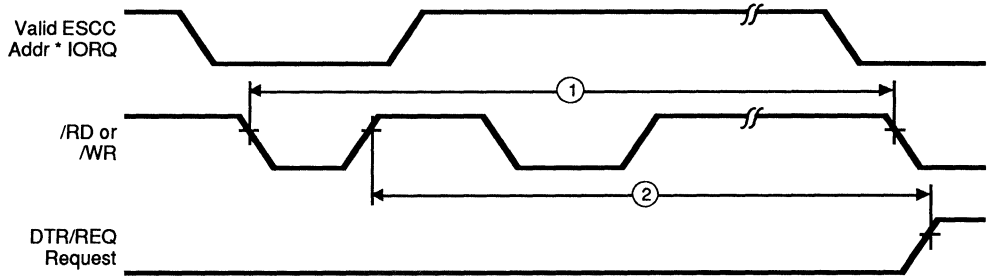


Figure 104. ESCC External Bus Master Timing

Table G. External Bus Master Interface Timing (SCC Related Timing)

No	Symbol	Parameter	Z8018216		Z8018220		Unit	Notes
			Min	Max	Min	Max		
1	TrC	Valid Access Recovery Time	4TcC		4TcC		ns	[1]
2	TdRDr(REQ)	/RD Rise to /DTR//REQ Not Valid Delay	4TcC		4TcC		ns	

Note:
[1] Applies only between transactions involving the ESCC.
These AC parameter values are preliminary and are subject to change without notice.

16550 MIMIC TIMING

Refer to Figures 105 thru 111 for MIMIC AC Timing.

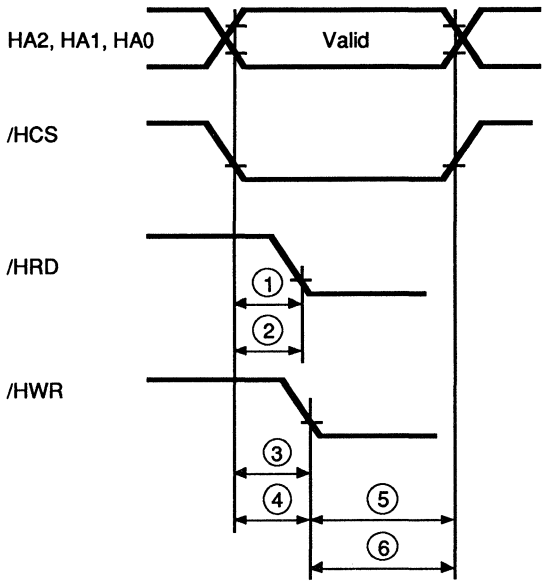


Figure 105. PC Host /RD /WR Timing

Table H. PC Host /RD /WR Timing

No	Symbol	Parameter	16 MHz		20 MHz		Units
			Min	Max	Min	Max	
1	tAR	/HRD Delay from Address	30		30		ns
2	tCSR	/HRD Delay from /HCS	30		30		ns
3	tAW	/HWR Delay from Address	30		30		ns
4	tCSW	/HWR Delay from /HCS	30		30		ns
5	tAh	Address Hold Time	20		20		ns
6	tCSh	/HCS Hold Time	20		20		ns

These AC parameter values are preliminary and are subject to change without notice.

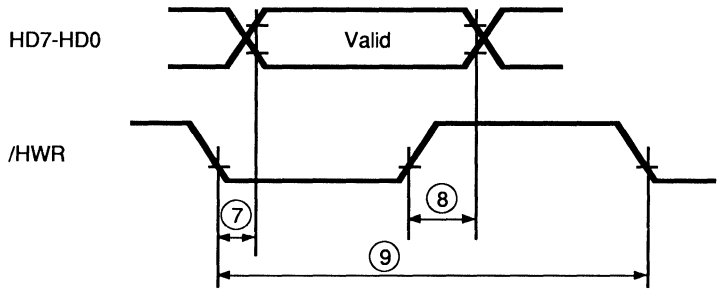


Figure 106. Data Setup and Hold, Output Delay, Write Cycle

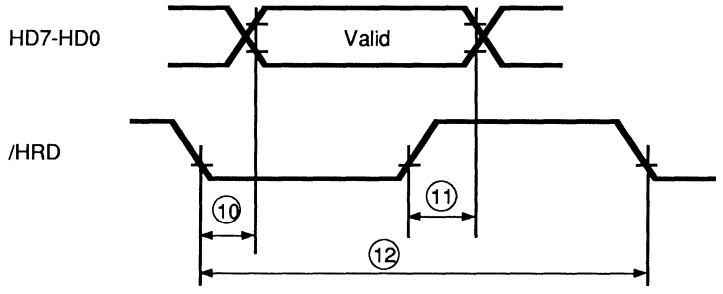


Figure 107. Data Setup and Hold, Output Delay, Read Cycle

Table I. Data Setup and Hold, Output Delay, Read Cycle

No	Sym	Parameter	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max	Units
7	tDs	Data Setup Time	30		30		ns
8	tDh	Data Hold Time	30		30		ns
9	tWc	Write Cycle Delay	2.5 MPU Clock Cycles		2.5 MPU Clock Cycles		ns
10	tRvD	Delay from /HRD to Data		125		125	ns
11	tHz	/HRD to Floating Delay	0	100	0	100	ns
12	tRc	Read Cycle Delay	125		125		ns

These AC parameter values are preliminary and are subject to change without notice.

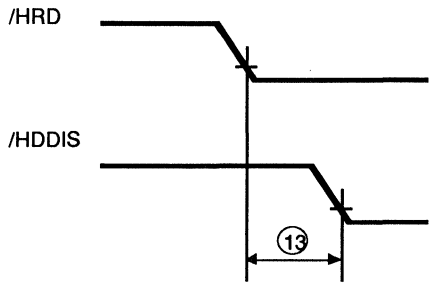


Figure 108. Driver Enable Timing

Table J. Driver Enable Timing

No	Sym	Parameter	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max	Units
13	tRDD	/HRD to Driver Enable/Disable		60		60	ns

The AC parameter values are preliminary and are subject to change without notice.

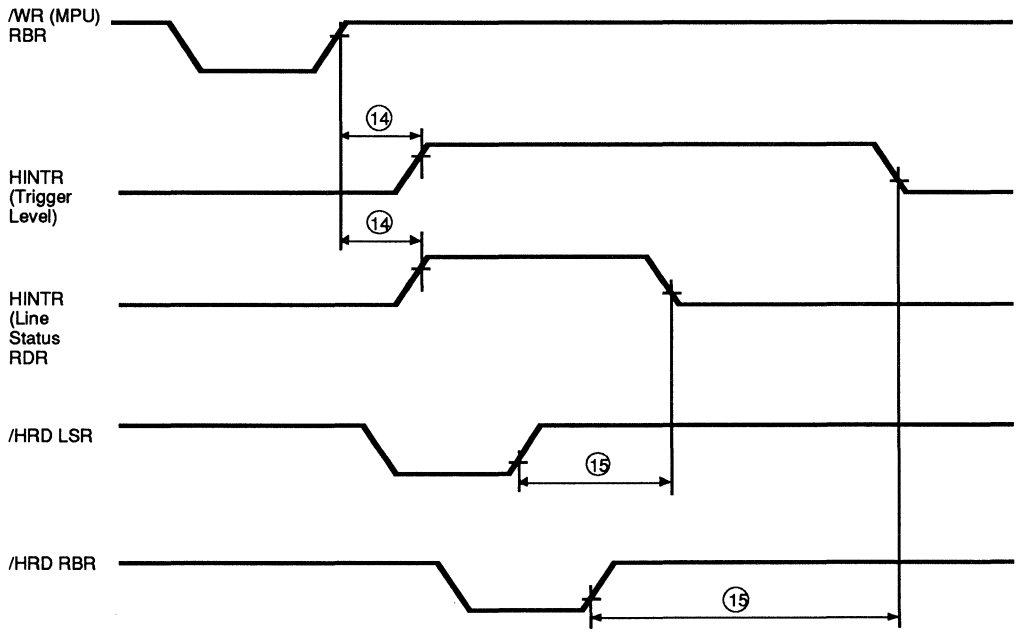


Figure 109. Interrupt Timing RCVR FIFO

Table K. Interrupt Timing RCVR FIFO

No	Sym	Parameter	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max
14	tSINT	Delay from Stop to Set Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles
15	tRINT	Delay from /HRD (RD RBR or RD LSR) to Reset Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles

These AC parameter values are preliminary and are subject to change without notice.

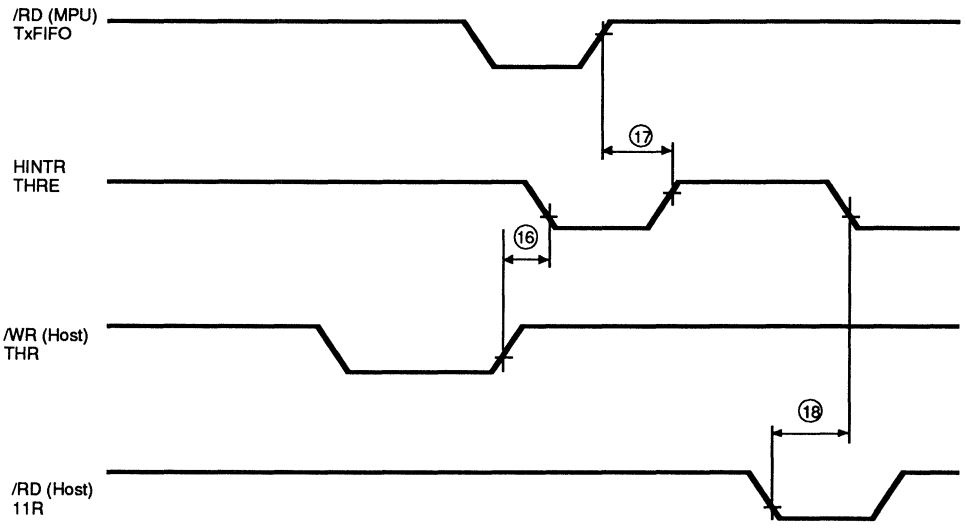


Figure 110. Interrupt Timing Transmitter FIFO

Table L. Interrupt Timing Transmitter FIFO

No	Sym	Parameter	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max
16	tHR	Delay from /WR (WR THR) to Reset Interrupt		2.5 MPU Clock Cycles		2.5 MPU Clock Cycles
17	TSTI	Delay from Stop to Interrupt (THRE)	2 MPU Clock Cycles		2 MPU Clock Cycles	
18	TIR	Delay from /RD (RD IIR) to Reset Interrupt (THRIE)		75		75

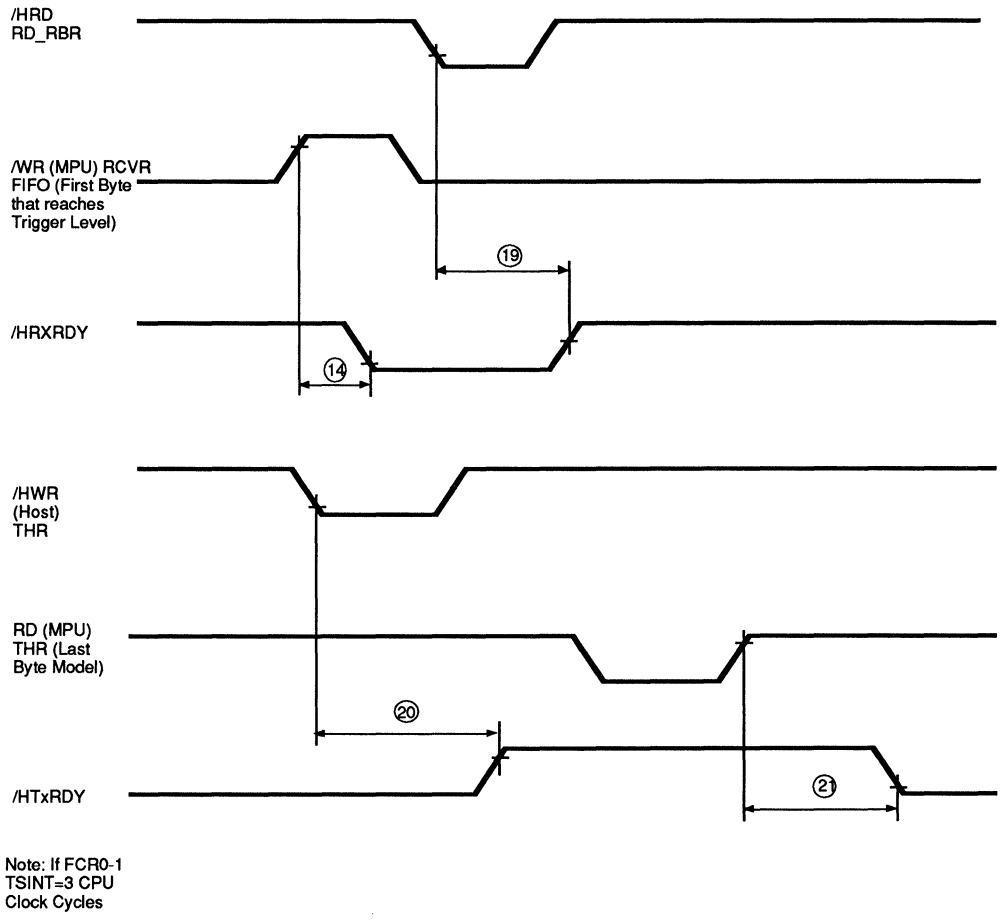


Figure 111. RCVR FIFO Bytes Other Than First

Table M. RCVR FIFO Bytes Other Than First

No	Sym	Parameter	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max	Units
19	tRXi	Delay from /HRD RBR to /HRxRDY Inactive		290		290	ns
20	TWxi	Delay from Write to /HTxRDY Inactive		125		125	
21	tSXa	Delay From Start to /HTxRDY Active		3 MPU Clock Cycles		3 MPU Clock Cycles	

These AC parameter values are preliminary and are subject to change without notice.

Clock Generator

The ZIP™ uses the Z182 MPUs on-chip clock generator to supply system clock. The required clock is easily generated by connection a crystal to the external terminals (XTAL,EXTAL). The clock output runs at half the crystal frequency for X2 mode.

Recommended characterstics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).

Type of crystal: Fundamental, parallel type crystal (AT cut is recommended).

Frequency tolerance: Application dependent.
CL, Load capacitance: Approximately 22 pF (acceptable range is 20-30 pF).

Rs, equivalent-series resistance: ≤ 30 Ohms

$C_{IN}=C_{OUT}=15\sim22$ pF.

For PHI > 15 MHz (X2 Mode), it is recommended that an oscillator be used as input to EXTAL.

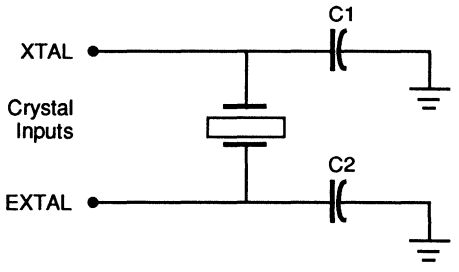
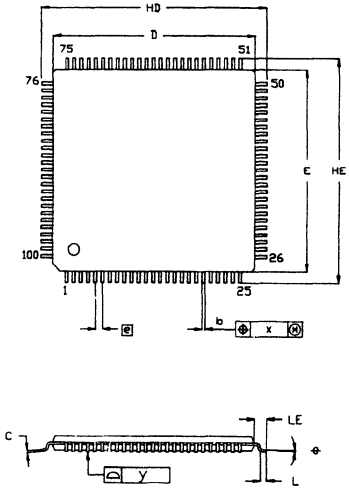


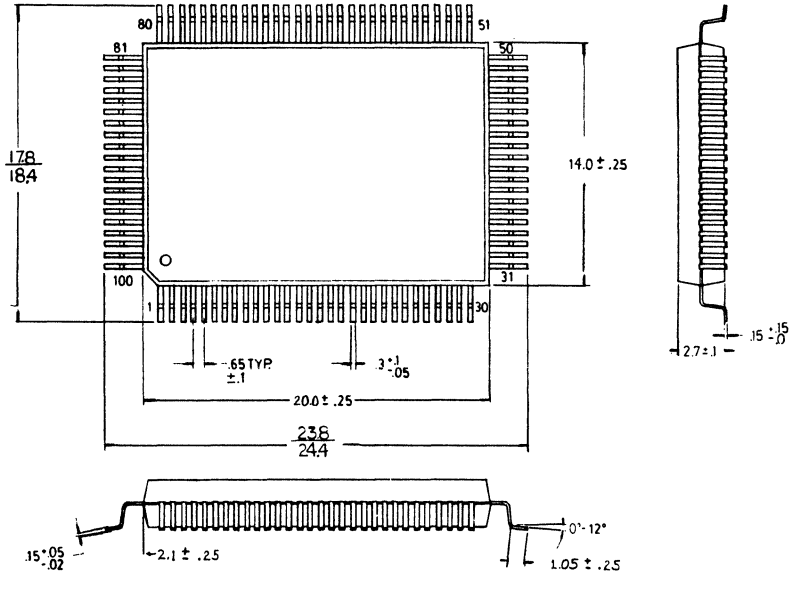
Figure 112. Circuit Configuration For Crystal

PACKAGE INFORMATION



SYMBOL	DIMENSIONS IN MM.		
	MIN.	NOM.	MAX.
A	–	–	1.60
A1	–	–	0.20
A2	1.30	1.40	1.50
b	0.15	0.18	0.26
c	0.10	0.15	0.20
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.50	–
L	0.35	0.50	0.65
LE	0.90	1.00	1.10
HD	15.85	16.00	16.15
HE	15.85	16.00	16.15
x	–	–	0.15
y	–	–	0.10
θ	0°	–	5°

100-Lead VQFP Package Diagram



100-Lead QFP Package Diagram

ORDERING INFORMATION

Z80182

16 MHz	20 MHz
Z8018216ASC	Z8018220DASC
Z8018216FSC	Z8018220FSC

Please check availability before placing order.

Package
A=VQFP (Very Small QFP)
F=Plastic Quad Flatpack

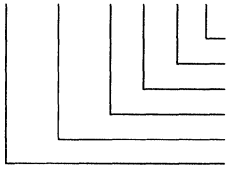
Temperature
E=-40°C to +100°C
S=0°C to +70°C

Speeds
16=16.384 MHz
20=20.0 MHz

Environmental
C=Plastic Standard
D=Plastic Stressed
E=Hemetric Standard

Example:

Z 80182 16 A S C is a Z80182, 16 MHz, VQFP, 0°C to +70°C, Plastic Standard Flow



ZILOG DOMESTIC SALES OFFICES AND TECHNICAL CENTERS

CALIFORNIA
Agoura 818-707-2160
Campbell 408-370-8120
Irvine 714-453-9701

COLORADO
Boulder 303-494-2905

FLORIDA
Largo 813-585-2533

GEORGIA
Norcross 404-448-9370

ILLINOIS
Schaumburg 708-517-8080

MINNESOTA
Minneapolis 612-944-0737

NEW HAMPSHIRE
Nashua 603-888-8590

NORTH CAROLINA
Raleigh 919-790-7706

OHIO
Independence 216-447-1480

PENNSYLVANIA
Ambler 215-653-0230

TEXAS
Dallas 214-987-9987

WASHINGTON
Seattle 206-523-3591

INTERNATIONAL SALES OFFICES

CANADA
Toronto 416-673-0634

GERMANY
Munich 49-89-672-045
Sömmerda 37-626-23906

JAPAN
Tokyo 81-3-3587-0528

HONG KONG
Kowloon 852-7238979

KOREA
Seoul 82-2-552-5401

SINGAPORE
Singapore 65-2357155

TAIWAN
Taipei 886-2-741-3125

UNITED KINGDOM
Maidenhead 44-628-392-00

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
Telex 910-338-7621
FAX 408 370-8056