ZiLOG

Discrete Z8®
Microcontrollers

For Computer Peripheral and Consumer Electronics Applications

Includes Specifications for the following parts:

Z86C03	Z86C08
Z86E03	Z86E08
Z86C04	Z86C30
Z86E04	Z86E30
Z86C06	Z86C31
Z86E06	Z86E31
Z86C07	Z86C40
Z86E07	Z86E40

Product Specifications Databook

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- Z86C03
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- Z86C07
- Z86E07
- Z86C08
- Z86E08
- Z86C30
- Z86E30
- Z86C31
- Z86E31
- Z86C40
- Z86E40

Databook

Q3/94 DC 8318-02

DISCRETE Z8® MICROCONTROLLERS

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ZiLOG Discrete Z8® Microcontrollers

Quick Take — A Summary of Parts and Features

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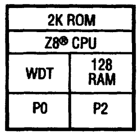
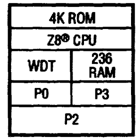
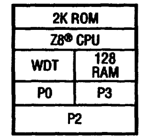
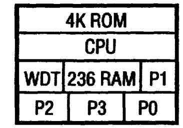
Part Number	**Z86C03**	**Z86C04/Z86E04**	**Z86C06**	**Z86C07/Z86E07**
Description	Consumer Controller Processor (CCP™) with 512 Byte ROM	Z86C04 = 8-Bit Low Cost 1 Kbyte ROM MCU Z86E04 = OTP Version	Consumer Controller Processor (CCP™) with 1 Kbyte ROM	Z86C07 = 8-Bit 2 Kbyte ROM MCU Z86E07 = OTP Version
Process/Speed	CMOS: 8 MHz	CMOS: 8 MHz	CMOS: 12 MHz	CMOS: 8 and 12 MHz
Features	■ 512 Byte ROM ■ 64-Byte RAM ■ Two Standby Modes ■ One Counter/Timer ■ ROM Protect ■ Two Analog Comparator ■ Auto Power-On Reset ■ Low-Voltage Protection ■ 14 I/O ■ RC Oscillator Option ■ Low-Noise Option	■ 1 Kbyte ROM ■ 128-Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparator ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 14 I/O ■ Low-Noise Option	■ 1 Kbyte ROM ■ 128-Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparator ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 14 I/O ■ RC Oscillator Option ■ Serial Peripheral Interface (SPI)	■ 2 Kbytes ROM ■ 124-Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparator ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 14 I/O ■ Low Noise Option ■ Programmable Interrupt Polarity
Package	18-Pin DIP 18-Pin SOIC	18-Pin DIP 18-Pin SOIC	18-Pin DIP 18-Pin SOIC	18-Pin DIP 18-Pin SOIC
Support Products	Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator	Z86C0800ZCO - Evaluation Board Z86C0800ZDP - Adaptor Kit Z86C1200ZEM - Emulator Z86C1200ZPD - Adaptor Kit Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator	Z86E0600ZDP - Adaptor Kit Z86C5000ZEM - Emulator Z86C5000ZDP - Adaptor Kit Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator	Contact Your Local Zilog Sales Office

ZiLOG Discrete Z8® Microcontrollers — Quick Take — A Summary of Parts and Features

Block Diagram				
Part Number	**Z86C08/Z86E08**	**Z86C30/Z86E30**	**Z86C31/Z86E31**	**Z86C40/Z86E40**
Description	Z86C08 = Z8® MCU with 2 Kbyte ROM Z86E08 = OTP Version	Z86C30 = Z8® (CCP™) with 4 Kbyte ROM Z86E30 = OTP Version	Z86C31 = 8-Bit MCU with 2 Kbyte ROM Z86E31 = OTP Version	Z8® Consumer Controller Processor (CCP™) Z86E40 = OTP Version
Process/Speed	CMOS: 12 MHz	CMOS: 12 MHz	CMOS: 8 MHz	CMOS: 12 MHz
Features	■ 2 Kbyte ROM ■ 128 Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparators ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 14 I/O ■ Low-Noise Option	■ 4 Kbyte ROM ■ 236 Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparators ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 24 I/O ■ RC Oscillator Option ■ Low-Noise Option	■ 2 Kbyte ROM ■ 128 Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparators ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 24 I/O ■ RC Oscillator Option ■ Low-Noise Option	■ 4K ROM, 236 RAM ■ Two Standby Modes ■ Two Counter/Timers ■ ROM Protect ■ RAM Protect ■ Four Ports ■ Low-Voltage Protection ■ Two Analog Comparators ■ Low-EMI Mode ■ Watch-Dog Timer (WDT) ■ Auto Power-On Reset ■ Low-Power Option
Package	18-Pin DIP 18-Pin SOIC	28-Pin DIP 28-Pin PCB Chip Carrier	28-Pin DIP 28-Pin PCB Chip Carrier	40-Pin DIP 44-Pin PLCC
Support Products	Z86C0800ZCO - Evaluation Board Z86C0800ZDP - Adaptor Kit Z86C1200ZEM - Emulator Z86C1200ZDP - Adaptor Kit Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator	Z86E3000ZDP - Adaptor Kit Z86C5000ZEM - Emulator Z86C5000ZPD - Emulator Pod Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator	Z86E3000ZDP - Adaptor Kit Z86C5000ZEM - Emulator Z86C5000ZPD - Emulator Pod Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator	Z86C5000ZEM - Emulator Z86CCP00ZEM - Emulator Z86E4000ZDP - Adaptor Kit Z86E4000ZDV - Adaptor Kit

Z86C03/C06

CMOS Z8® 8-BIT CCP™ CONSUMER CONTROLLER PROCESSORS

FEATURES

- The Z86C03/C06 Devices Have the Following General Characteristics:

Part	ROM	RAM	Speed
Z86C03	512 bytes	60	8 MHz
Z86C06	1 Kbyte	124	12 MHz

- 18-Pin Package (DIP, SOIC)
- 3.0 to 5.5 Volt Operating Range
- Operating Temperature: –40°C to +105°C
- Fast Instruction Pointer: 1.5 µs @ 8 MHz (C03); 1.0 µs @ 12 MHz (C06)
- Multiple Expanded Register File Control Registers and Two SPI Registers (Z86C06 only)
- One/Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speeds up to 8 MHz (C03) and 12 MHz (C06)
- Software-Enabled Watch-Dog Timer
- Power-On Reset Timer
- Two Standby Modes: STOP and HALT
- Two Comparators with Programmable Interrupt Polarity
- 14 Input/Output Lines (Two with Comparator Inputs)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.
- Serial Peripheral Interface (SPI) (Z86C06 Only)
- Software Programmable Low EMI Mode
- ROM Protect Option
- Auto Latches

GENERAL DESCRIPTION

The Z86C03/C06 CCP™ (Consumer Controller Processors) are members of Zilog's the Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 512 and 1K bytes of ROM and 60 and 124 bytes of general-purpose RAM, respectively, these low cost, low power consumption CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C03/C06 CCP architecture is characterized by Zilog's 8-bit microcontroller core with the addition of an Expanded Register File to allow easy access to register mapped peripheral and I/O circuits. The Z86C03/C06 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, and industrial applications.

For applications demanding powerful I/O capabilities, the Z86C03/C06 provides 14 pins dedicated to input and output. These lines are grouped into two ports and are configurable under software control to provide timing, status signals, or parallel I/O.

GENERAL DESCRIPTION (Continued)

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File. The Register File is composed of 60/124 bytes of General-Purpose Registers, two I/O Port registers, and 13/15 Control and Status registers. The Expanded Register File consists of three control registers in the Z86C03, and four control registers, a SPI Receive Buffer, and a SPI compare register in the Z86C06.

With powerful peripheral features such, as on-board comparators, counter/timer(s), Watch-Dog Timer (WDT), and Serial Peripheral Interface (SPI) (C06 only), the Z86C03/C06 meets the needs of a variety of sophisticated controller applications (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

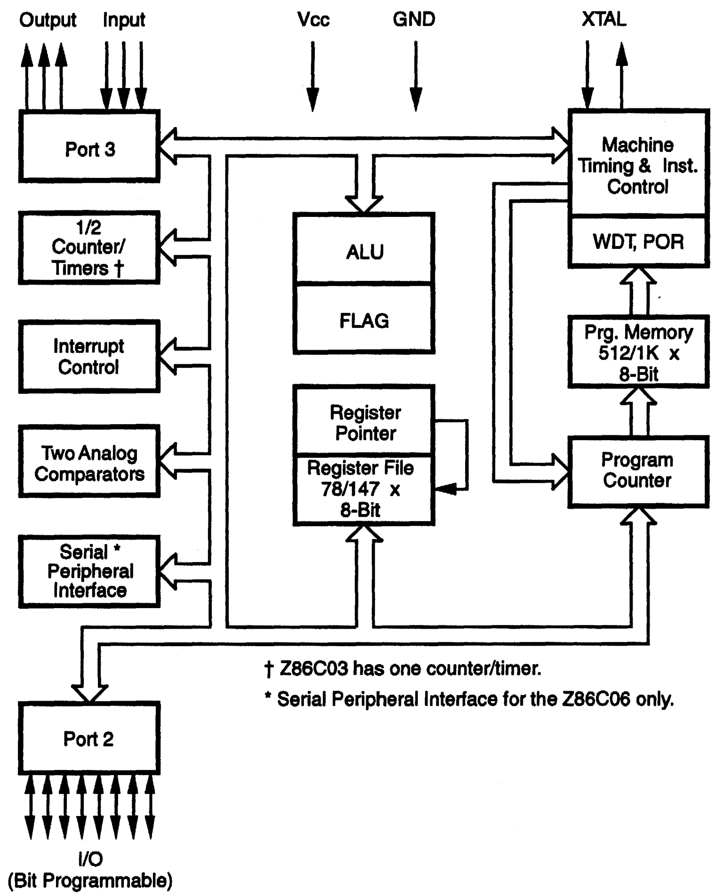


Figure 1. Z86C03/C06 Functional Block Diagram

PIN DESCRIPTION

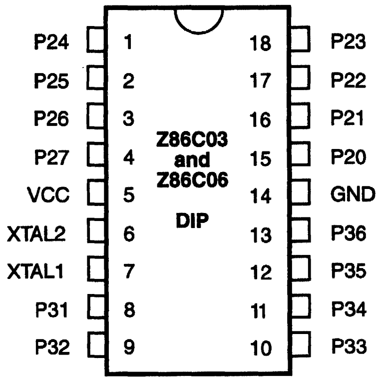


Figure 2. 18-Pin DIP Pin Configuration

Table 1. 18-Pin DIP and SOIC Pin Identification

No	Symbol	Function	Direction
1-4	P24-27	Port 2, pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-33	Port 3, pins 1, 2, 3	Fixed Input
11-13	P34-36	Port 3, pins 4, 5, 6	Fixed Output
14	GND	Ground	
15-18	P20-23	Port 2, pins 0, 1, 2, 3	In/Output

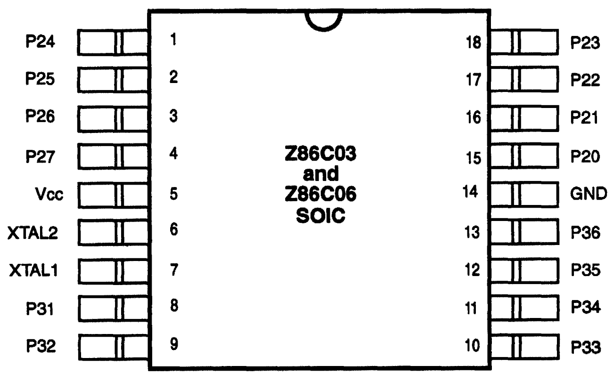


Figure 3. 18-Pin SOIC Pin Configuration

PIN FUNCTIONS

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2 (P27-P20). Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered and contain Auto Latches. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figures 4a, 4b, and 4c). Low EMI output buffers can be globally programmed by the software. In addition, when the SPI is enabled, P20 functions as data-in (DI), and P27 functions as data-out (DO) for the SPI (SPI on the Z86C06 only).

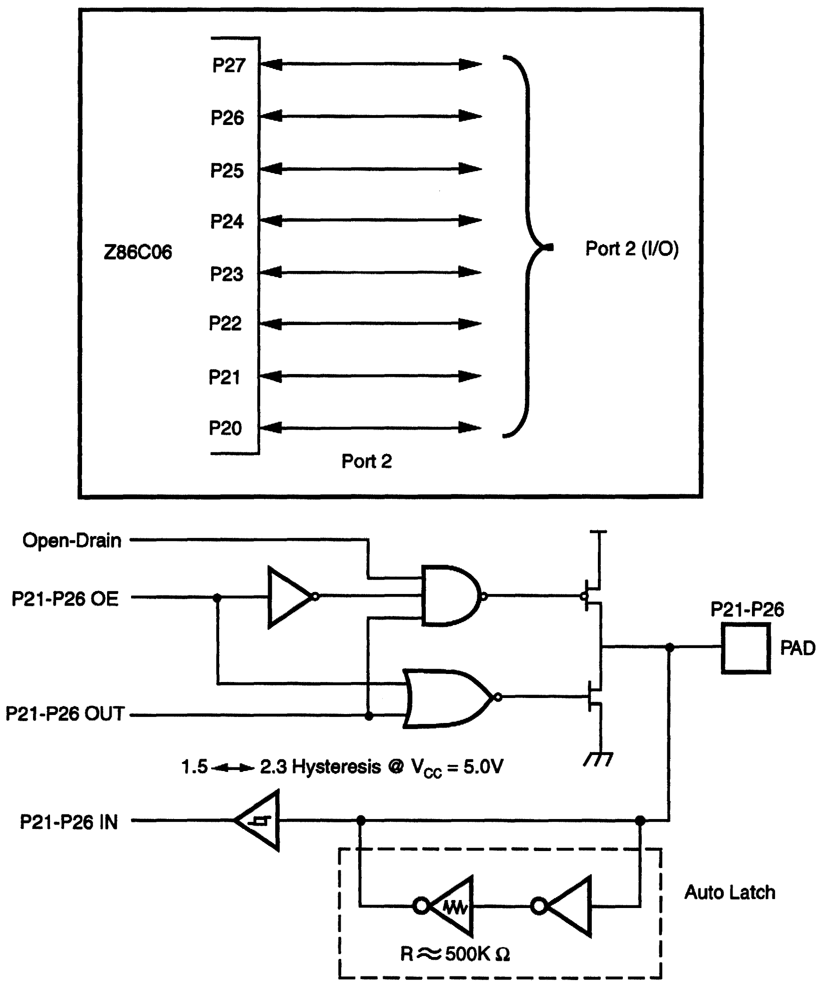


Figure 4a. Port 2 Configuration (Z86C06)

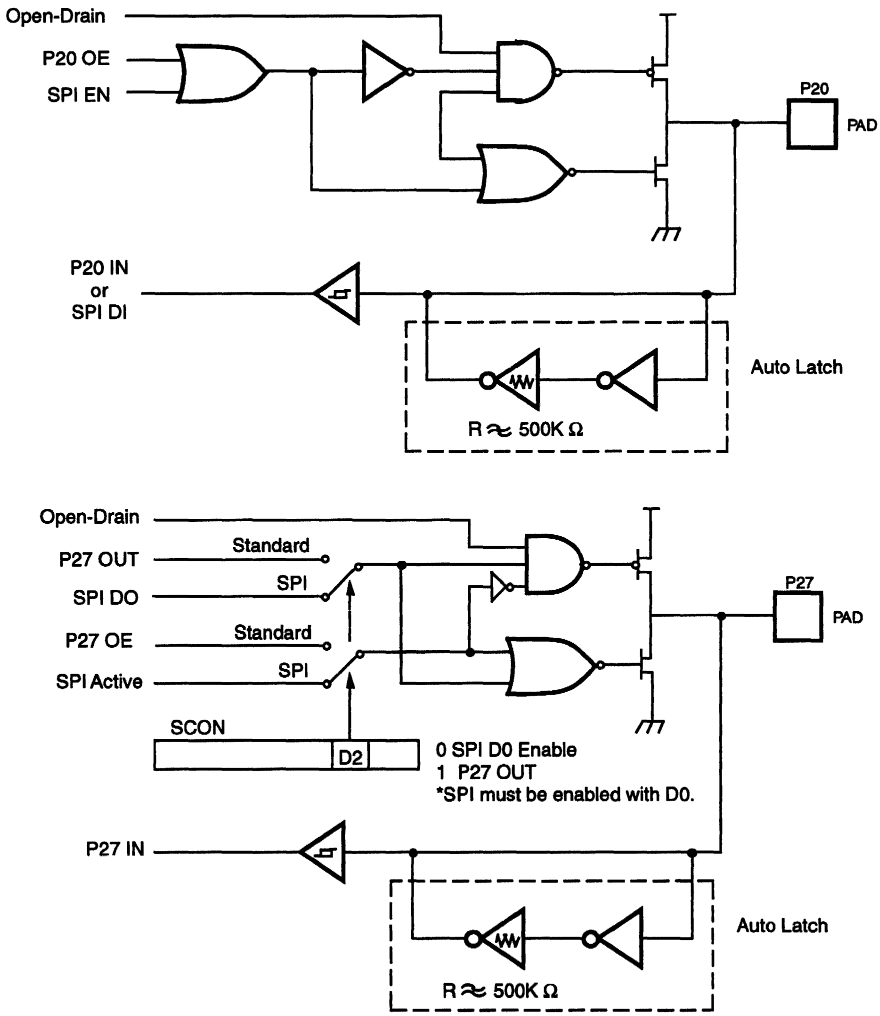


Figure 4b. Port 2 Configuration (Z86C06)

PIN FUNCTIONS (Continued)

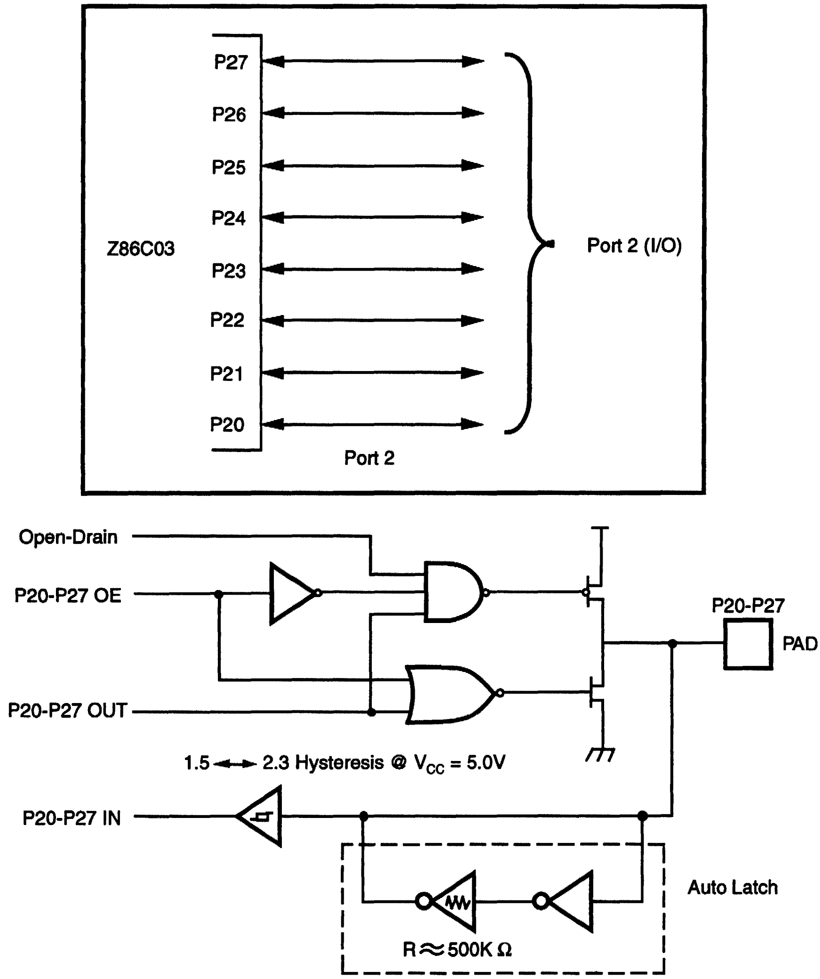


Figure 4c. Port 2 Configuration (Z86C03)

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

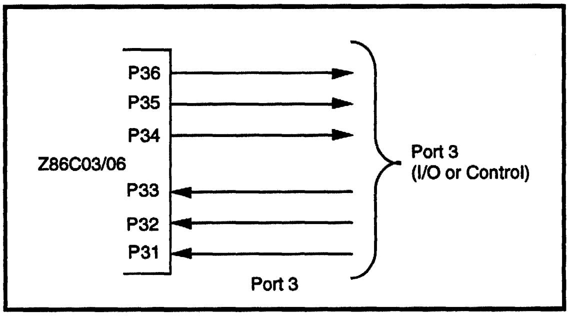
Port 3 (P36-P31). Port 3 is a 6-bit, CMOS compatible port. These six lines consist of three fixed inputs (P31-P33) and three fixed outputs (P34-P36). Pins P31, P32, and P33 are standard CMOS inputs (no auto latches) and pins P34, P35, and P36 are push-pull outputs. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M-bit D1). Pins P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input when the analog mode is selected. P33 is a falling edge interrupt input only.

Note: P33 is available as an interrupt input only in the digital mode. P31 and P32 are valid interrupt inputs and P31 is the T_{IN} input when the analog or digital input mode is selected.

The outputs from the analog comparator can be globally programmed to output from P34 and P35 by setting PCON (F) 00 bit D0 = 1.

Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}).

In the Z86C06, pin P34 can also be configured as SPI clock (SK), input and output, and pin P35 can be configured as Slave Select (SS) in slave mode only, when the SPI is enabled (Figures 5a and 5b).



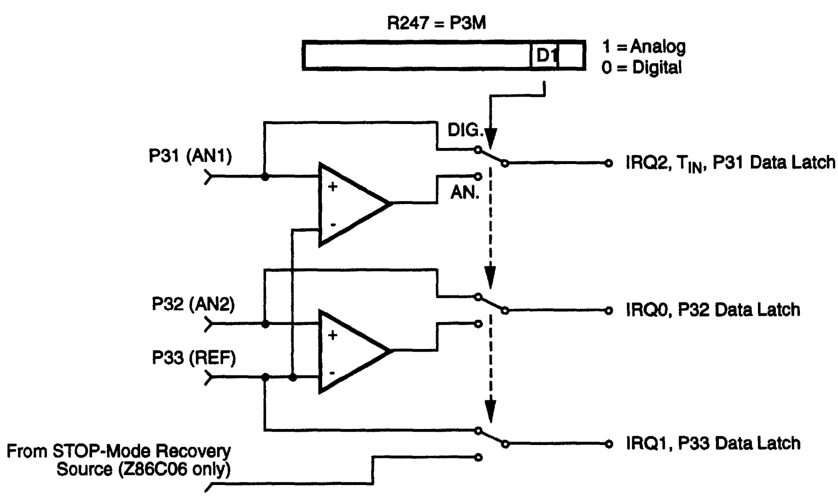


Figure 5a. Port 3 Configuration

PIN FUNCTIONS (Continued)

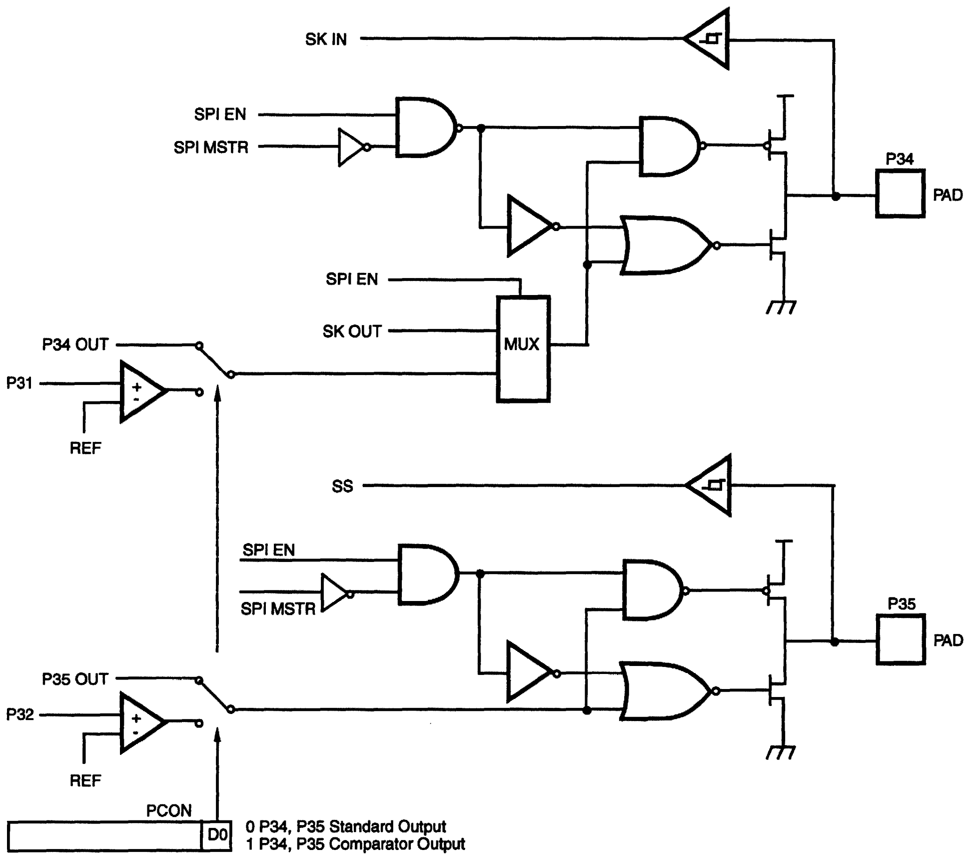


Figure 5b. Port 3 Configuration (Z86C06)

Low EMI Emission. The Z86C03/C06 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns (typical).
- Low EMI output drivers resistance of 200 ohms (typical).
- Low EMI oscillator.
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz (250 ns cycle time) when the low EMI oscillator is selected and SCLK = External (SMR Register Bit D1=1).

Comparator Inputs. Port 3 Pin P31 and P32 each have a comparator front end. The comparator reference voltage pin P33 is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In digital mode, Pin P33 can be used as a P33 register input or IRQ1 source.

FUNCTIONAL DESCRIPTION

The following special functions have been added to the Z86C03/C06 CCPs to enhance the standard Z8® architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of four ways:

1. Power-On Reset
2. Watch-Dog Timer
3. STOP-Mode Recovery Source
4. Low Voltage Protection

Having the Auto Power-On Reset circuitry built-in, the Z86C03/C06 does not require an external reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles.

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a STOP-Mode Recovery operation.

Program Memory. Z86C03/C06 can address up to 512/1K bytes of internal program memory (Figure 6). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 511/1023 consists of on-chip, user program mask ROM.

ROM Protect. The 512/1K bytes of Program Memory is mask programmable. A ROM protect feature will prevent "dumping" of the ROM contents by inhibiting execution of the LDC and LDCI instructions to program memory in all modes.

ROM protect is mask-programmable. It is selected by the customer when the ROM code is submitted. **Selecting ROM protect disables the LDC and LDCI instructions in all modes. ROM look-up tables are not supported in this mode.**

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 7). These register groups are known as the Expanded Register File (ERF).

Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of register RP select the working register group (Figure 7). For the Z86C03, three system configuration registers reside in the ERF address space Bank F. For the Z86C06, three system configuration registers reside in the ERF address space Bank F, while three SPI registers reside in Bank C. The rest of the ERF address space is not physically implemented and is open for future expansion.

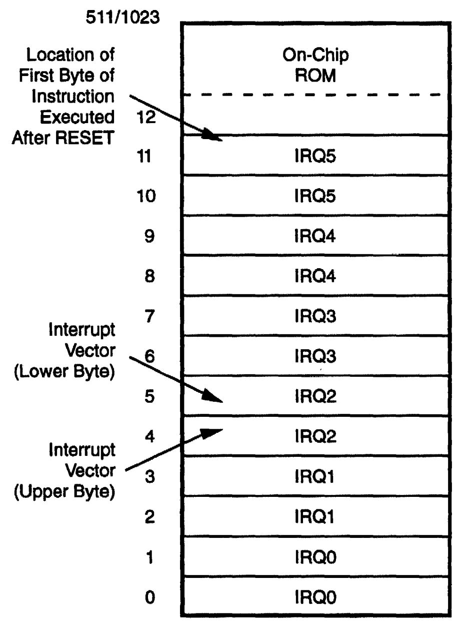
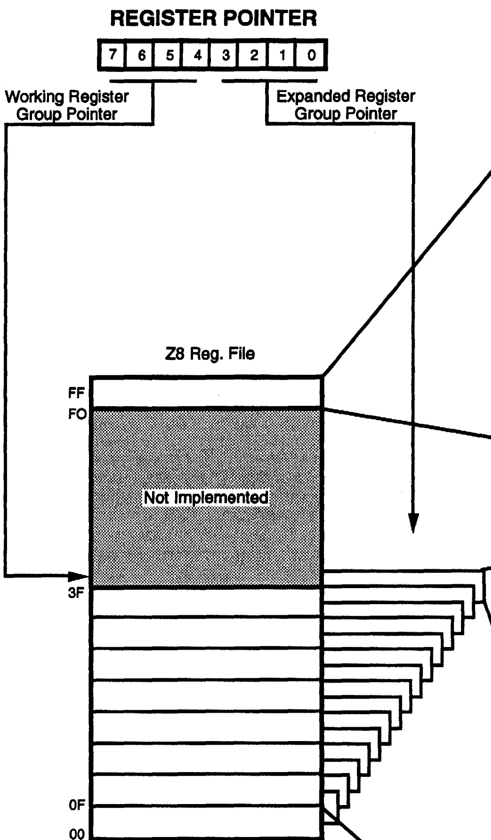


Figure 6. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)



Z8 STANDARD CONTROL REGISTERS

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
	FF	SPL	U	U	U	U	U	U	U	U
	FE	GPR	U	U	U	U	U	U	U	U
	FD	RP	0	0	0	0	0	0	0	0
	FC	FLAGS	U	U	U	U	U	U	U	U
	FB	IMR	0	U	U	U	U	U	U	U
	FA	IRQ	0	0	0	0	0	0	0	0
	F9	IPR	U	U	U	U	U	U	U	U
	F8	P01M	U	U	U	0	U	U	U	U
*	F7	P3M	U	U	U	U	U	U	0	0
*	F6	P2M	1	1	1	1	1	1	1	1
	F5	Reserved								
	F4	Reserved								
	F3	PRE1	U	U	U	U	U	U	0	0
	F2	T1	U	U	U	U	U	U	U	U
	F1	TMR	0	0	0	0	0	0	0	0
	F0	Reserved								

RESET CONDITION

EXPANDED REG. GROUP (F)

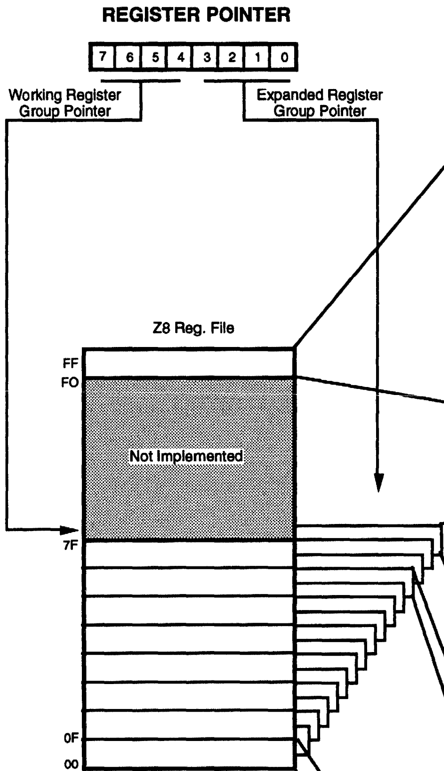
	REGISTER		RESET CONDITION							
*	(F) 0F	WDTMR	U	U	U	0	1	1	0	1
	(F) 0E	Reserved								
	(F) 0D	Reserved								
	(F) 0C	Reserved								
*	(F) 0B	SMR	0	0	1	0	0	0	0	†
	(F) 0A	Reserved								
	(F) 09	Reserved								
	(F) 08	Reserved								
	(F) 07	Reserved								
	(F) 06	Reserved								
	(F) 05	Reserved								
	(F) 04	Reserved								
	(F) 03	Reserved								
	(F) 02	Reserved								
	(F) 01	Reserved								
	(F) 00	PCON	1	1	1	U	U	U	U	0

EXPANDED REG. GROUP (0)

REGISTER		RESET CONDITION							
(0) 03	P3	†	1	1	1	U	U	U	†
(0) 02	P2	U	U	U	U	U	U	U	U
(0) 01	Reserved	U	U	U	U	U	U	U	U
(0) 00	Reserved	U	U	U	U	U	U	U	U

Notes:
General-purpose registers are undefined after power-up, and they are not changed after reset.
* Will not be reset with a STOP-Mode Recovery
U = Unknown
† = Reserved

Figure 7a. Expanded Register File Architecture (Z86C03)



Z8 STANDARD CONTROL REGISTERS

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
	FF	SPL	U	U	U	U	U	U	U	U
	FE	GPR	U	U	U	U	U	U	U	U
	FD	RP	0	0	0	0	0	0	0	0
	FC	FLAGS	U	U	U	U	U	U	U	U
	FB	IMR	0	U	U	U	U	U	U	U
	FA	IRQ	0	0	0	0	0	0	0	0
	F9	IPR	U	U	U	U	U	U	U	U
	F8	P01M	U	U	U	0	U	U	U	U
*	F7	P3M	U	U	U	U	U	U	0	0
*	F6	P2M	1	1	1	1	1	1	1	1
	F5	PRE0	U	U	U	U	U	U	U	0
	F4	T0	U	U	U	U	U	U	U	U
	F3	PRE1	U	U	U	U	U	U	0	0
	F2	T1	U	U	U	U	U	U	U	U
	F1	TMR	0	0	0	0	0	0	0	0
	F0	Reserved								

EXPANDED REG. GROUP (F)

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
*	(F) 0F	WDTMR	U	U	U	0	1	1	0	1
	(F) 0E	Reserved								
	(F) 0D	Reserved								
	(F) 0C	Reserved								
**	(F) 0B	SMR	0	0	1	0	0	0	0	0
	(F) 0A	Reserved								
	(F) 09	Reserved								
	(F) 08	Reserved								
	(F) 07	Reserved								
	(F) 06	Reserved								
	(F) 05	Reserved								
	(F) 04	Reserved								
	(F) 03	Reserved								
	(F) 02	Reserved								
	(F) 01	Reserved								
	(F) 00	PCON	1	1	1	U	U	U	U	0

EXPANDED REG. GROUP (C)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
(C) 02	SCON	U	U	U	U	0	0	0	0
(C) 01	RxBUF	U	U	U	U	U	U	U	U
(C) 00	SCOMP	0	0	0	0	0	0	0	0

EXPANDED REG. GROUP (0)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
(0) 03	P3	†	1	1	1	U	U	U	†
(0) 02	P2	U	U	U	U	U	U	U	U
(0) 01	Reserved	U	U	U	U	U	U	U	U
(0) 00	Reserved	U	U	U	U	U	U	U	U

Notes:
General-purpose registers are undefined after power-up, and they are not changed after reset.
* Will not be reset with a STOP-Mode Recovery.
** Will not be reset with a STOP-Mode Recovery, except D0.
U = Unknown
† = Reserved

Figure 7b. Expanded Register File Architecture (Z86C06)

FUNCTIONAL DESCRIPTION (Continued)

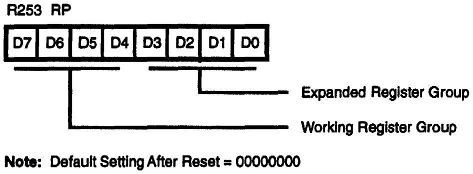


Figure 8. Register Pointer Register

Register File. The Register File consists of two I/O port registers, 60/124 general-purpose registers, and 13/15 control and status registers. The Z86C03 General-Purpose Register file ranges from address 00 to 3F while the Z86C06 General-Purpose Register file ranges from address 00 to 7F (see Figure 9). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 9). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

Stack. An 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60/124 general-purpose registers.

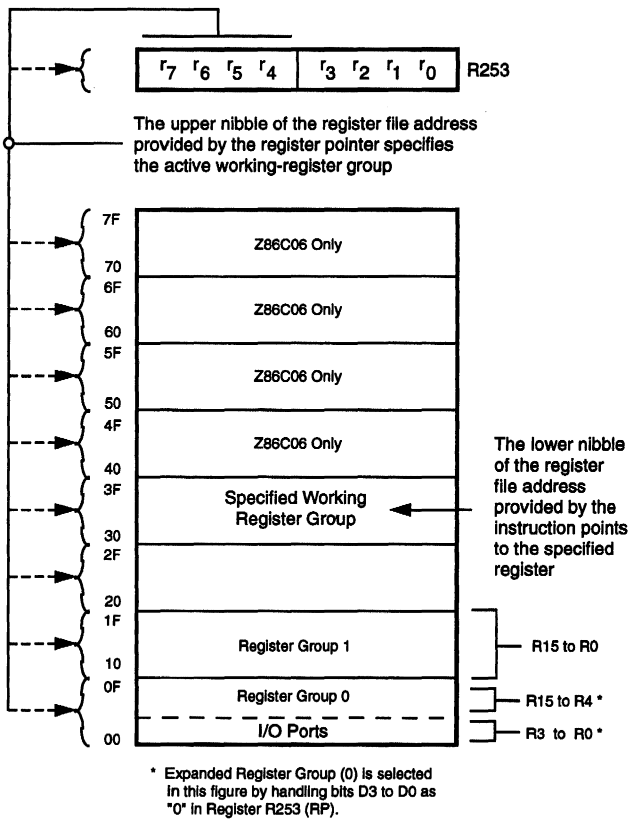
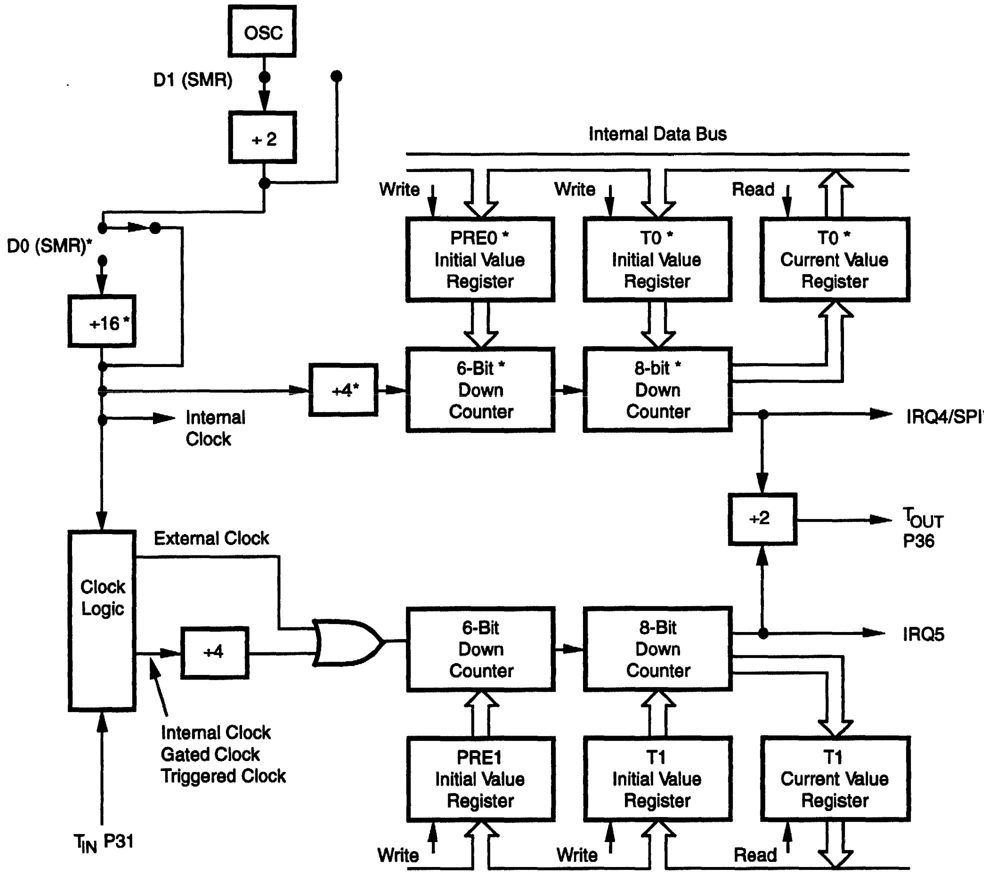


Figure 9. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler (Z86C03 only has T1). The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 10).



* Available only in the Z86C06

Figure 10. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated. Note that IRQ4 is software-generated in the Z86C03.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 serves as a timer output (T_{OUT}) through which T0 (C06 only), T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1 (C06 only). The T_{IN} mode is enabled by setting PRE1 bit D1 (R243) to 0.

Interrupts. The Z86C03/C06 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 11). The six sources are divided as follows; three sources are claimed by Port 3 lines P31-P33, two sources in the counter/timers, and one source for the SPI. The Interrupt Mask Register globally or singularly enables or disables the six interrupt requests (Table 2).

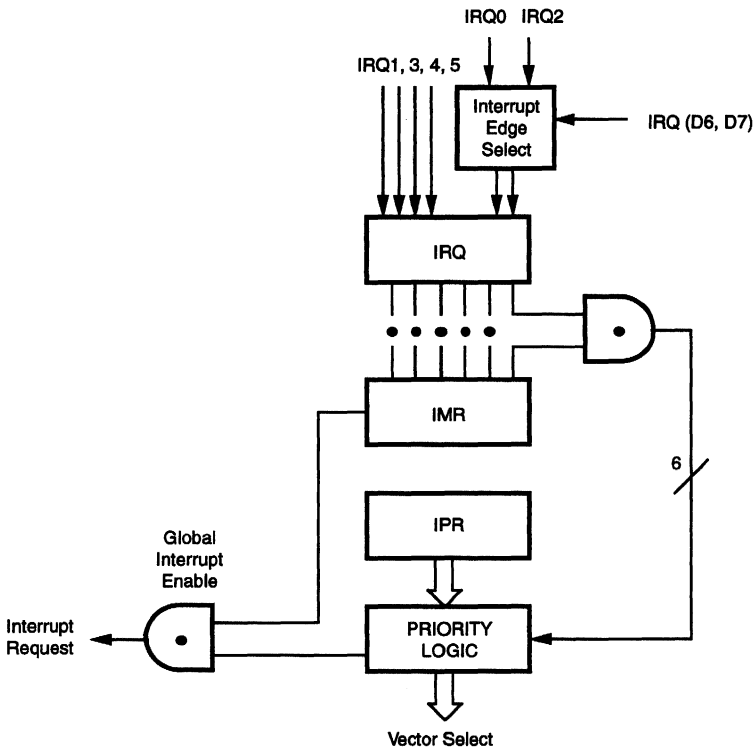


Figure 11. Interrupt Block Diagram

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	IRQ 0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ 1	IRQ 1	2, 3	External (P33), Falling Edge Triggered
IRQ 2	IRQ 2, T_{IN}	4,5	External (P31), Rising/Falling Edge Triggered
IRQ 3*	IRQ 3	6, 7	Software Generated, SPI Receive
IRQ 4	T0/IRQ 4	8, 9	Internal for C06 and Software Generated for C03
IRQ 5	TI	10, 11	Internal

Note:
* In the Z86C06, the SPI receive interrupt is mapped to IRQ3 when enabled.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86C03/C06 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service. In the Z86C06, when the SPI is disabled, IRQ3 has no hardware source but can be invoked by software (write to IRQ3 Register). When the SPI is enabled, an interrupt will be mapped to IRQ3 after a byte of data has been received by the SPI Shift Register.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

The programming bits for the INTERRUPT EDGE SELECT are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

Table 3. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

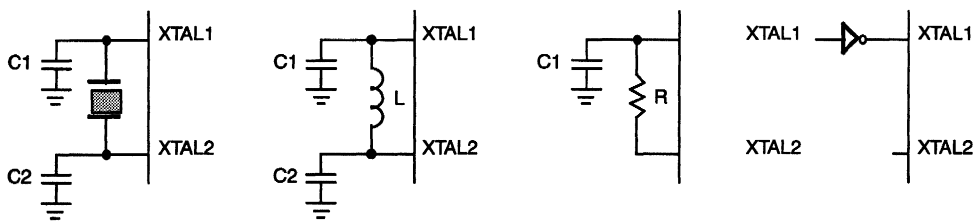
FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86C03/C06 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 8 MHz/12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values (capacitance between 10 pF to 300 pF) from each pin directly to the device ground (pin 14). The layout is important to reduce ground noise injection.

The RC oscillator option is mask-programmable, to be selected by the customer at the time ROM code is submitted. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 12). The RC value vs. Frequency curves are shown in Figures 57 and 58.

In addition, a special feature has been incorporated into the Z86C03/C06; in low EMI noise mode (bit 7 of PCON register=0) with the RC option selected, the oscillator is targeted to consume considerately less I_{CC} current at frequencies of 10 kHz or less.



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC
C1, C2 = 22 pF
L = 130 µH *
F = 3 MHz

RC
@ 5V Vcc (TYP)
C1 = 33pF*
R = 1kΩ*
F = 9.5 MHz

External Clock

* Preliminary Value Including Pin Parasitics

Figure 12. Oscillator Configuration

Power-On Reset. A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the three conditions:

- Power-Fail to Power-OK Status
- STOP-Mode Recovery (If D5 of SMR=1)
- WDT Timeout

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. A Halt instructions will turn off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device may be recovered by interrupts either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP mode is terminated by a RESET only, either by WDT timeout, POR, SPI compare; or SMR recovery. This causes the processor to restart the application program at address 000C (HEX). Note, the crystal remains active in STOP mode if bits 3 and 4 of the WDTMR are enabled. In this mode, only the Watch-Dog Timer runs in STOP mode.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF   NOP   ; clear the pipeline
6F   STOP  ; enter STOP mode
or
FF   NOP   ; clear the pipeline
7F   HALT  ; enter HALT mode
```

Serial Peripheral Interface (SPI)—Z86C06 Only. The Z86C06 incorporates a serial peripheral interface for communication with other microcontrollers and peripherals. **The SPI does not exist on the Z86C03**. The SPI includes features such as STOP-Mode Recovery, Master/Slave selection, and Compare mode. Table 4 contains the pin configuration for the SPI feature when it is enabled. The SPI consists of four registers: SPI Control Register (SCON), SPI Compare Register (SCOMP), SPI Receive/Buffer Register (RxBUF), and SPI Shift Register. SCON is located in bank (C) of the Expanded Register Group at address 02.

Table 4. Z86C06 SPI Pin Configuration

Name	Function	Pin Location
DI	Data-In	P20
DO	Data-Out	P27
SS	Slave Select	P35
SK	SPI Clock	P34

The SPI Control Register (SCON) (Figure 13) is a read/write register that controls; Master/Slave selection, interrupts, clock source and phase selection, and error flag. Bit 0 enables/disables the SPI with the default being SPI disabled. A 1 in this location will enable the SPI, and a 0 will disable the SPI. Bits 1 and 2 of the SCON register in Master mode select the clock rate. The user may choose whether internal clock is divide-by-2, -4, -8, or -16. In slave mode, Bit 1 of this register flags the user if an overrun of the RxBUF Register has occurred. The RxCharOverrun flag is only reset by writing a 0 to this bit. In slave mode, bit 2 of the Control Register disables the data-out I/O function. If a 1 is written to this bit, the data-out pin is released to its original port configuration. If a 0 is written to this bit, the SPI shifts out one bit for each bit received. Bit 3 of the SCON Register enables the compare feature of the SPI, with the default being disabled. When the compare feature is enabled, a comparison of the value in the SCOMP Register is made with the value in the RxBUF Register. Bit 4 signals that a receive character is available in the RxBUF Register.

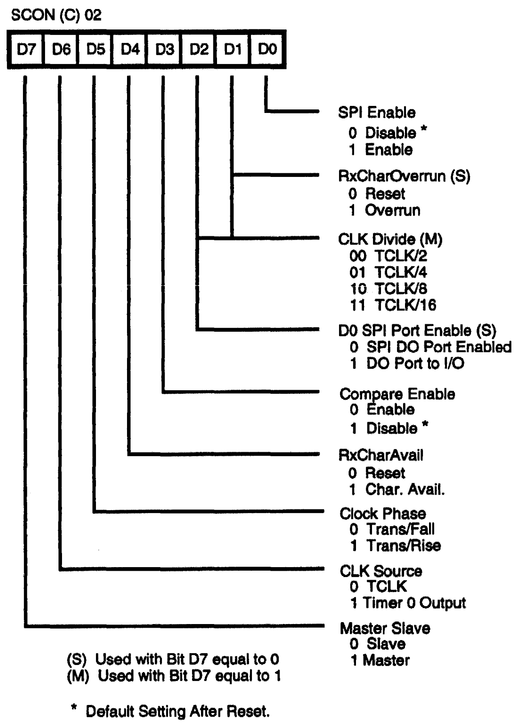


Figure 13. SPI Control Register (SCON) (Z86C06 Only)

If the associated IRQ3 is enabled, an interrupt is generated. Bit 5 controls the clock phase of the SPI. A 1 in Bit 5 allows for receiving data on the clock's falling edge and transmitting data on the clock's rising edge. A 0 allows receiving data on the clock's rising edge and transmitting on the clock's falling edge. The SPI clock source is defined in bit 6. A 1 uses Timer0 output for the SPI clock, and a 0 uses TCLK for clocking the SPI. Finally, bit 7 determines whether the SPI is used as a Master or a Slave. A 1 puts the SPI into Master mode and a 0 puts the SPI into Slave mode.

FUNCTIONAL DESCRIPTION (Continued)

SPI Operation (Z86C06 only). The SPI is used in one of two modes: either as system slave, or as system master. Several of the possible system configurations are shown in Figure 14. In the slave mode, data transfer starts when the slave select (SS) pin goes active. Data is transferred into the slave's SPI Shift Register through the DI pin, which has the same address as the RxBUF Register. After a byte of data has been received by the SPI Shift Register, a Receive Character Available (RCA/IRQ3) flag and interrupt is generated. The next byte of data will be received at this time. The RxBUF Register must be cleared, or a Receive Character Overrun (RxCharOverrun) flag will be set in the SCON Register, and the data in the RxBUF Register will be overwritten. When the communication between the master and slave is complete, the SS goes inactive.

Unless disconnected, for every bit that is transferred into the slave through the DI pin, a bit is transferred out through the DO pin on the opposite clock edge. During slave operation, the SPI clock pin (SK) is an input. In master mode, the CPU must first activate a SS through one of it's I/O ports. Next, data is transferred through the master's DO pin one bit per master clock cycle. Loading data into the shift register initiates the transfer. In master mode, the master's clock will drive the slave's clock. At the conclusion of a transfer, a Receive Character Available (RCA/IRQ3) flag and interrupt is generated. Before data is transferred via the DO pin, the SPI Enable bit in the SCON Register must be enabled.

SPI Compare (Z86C06 only). When the SPI Compare Enable bit, D3 of the SCON Register is set to 1, the SPI Compare feature is enabled. The compare feature is only valid for slave mode. A compare transaction begins when the (SS) line goes active. Data is received as if it were a normal transaction, but there is no data transmitted to avoid bus contention with other slave devices. When the compare byte is received, IRQ3 is not generated. Instead, the data is compared with the contents of the SCOMP Register. If the data does not match, DO remains inactive and the slave ignores all data until the (SS) signal is reset. If the data received matches the data in the SCOMP register, then a SMR signal is generated. DO is activated if it is not tri-stated by D2 in the SCON Register, and data is received the same as any other SPI slave transaction.

When the SPI is activated as a slave, it operates in all system modes; STOP, HALT, and RUN. Slaves' not comparing remain in their current mode, whereas slaves' comparing wake from a STOP or HALT mode by means of an SMR.

SPI Clock (Z86C06 only). The SPI clock maybe driven by three sources: Timer0, a division of the internal system clock, or the external master when in slave mode. Bit D6 of the SCON Register controls what source drives the SPI clock. A 0 in bit D6 of the SCON Register determines the division of the internal system clock if this is used as the SPI clock source. Divide by 2, 4, 8, or 16 is chosen as the scaler.

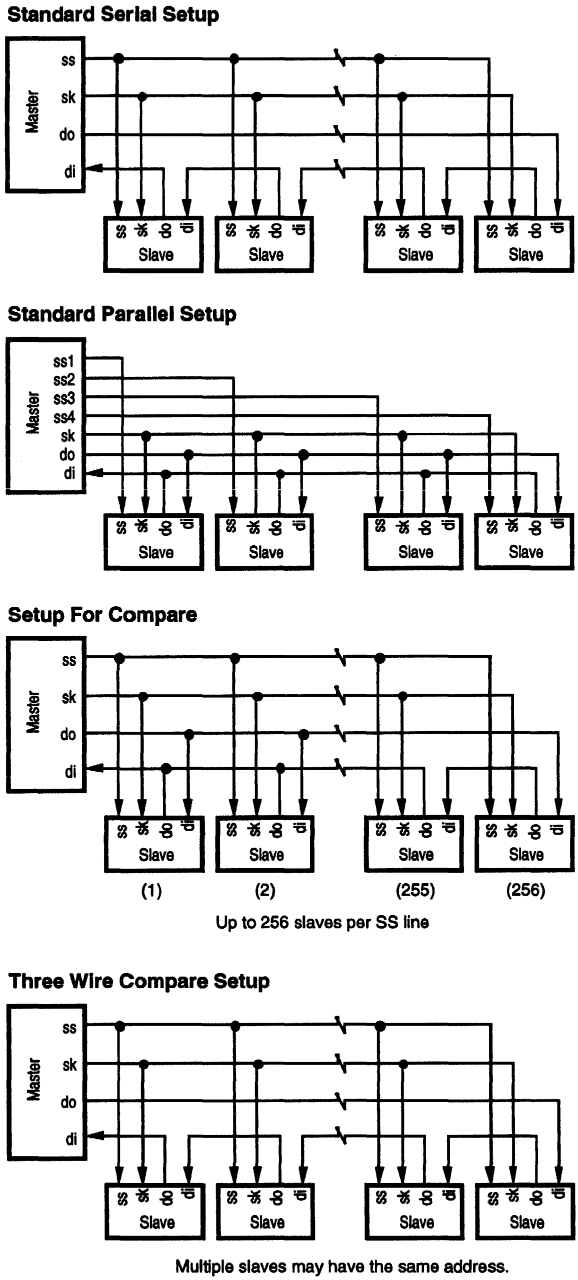


Figure 14. SPI System Configuration (Z86C06 Only)

FUNCTIONAL DESCRIPTION (Continued)

Receive Character Available and Overrun (Z86C06 Only). When a complete data stream is received, an interrupt is generated and the RxCharAvail bit in the SCON Register is set. Bit 4 in the SCON Register is for enabling or disabling the RxCharAvail interrupt. The RxCharAvail bit is available for interrupt polling purposes and is reset when the RxBUF Register is read. RxCharAvail is generated in both master and slave modes. While in slave mode, if the RxBUF is not read before the next data stream is received and loaded into the RxBUF Register, Receive Character Overrun (RxCharOverrun) occurs. Since there is no need for clock control in slave mode, bit D1 in the SPI Control Register is used to log any RxCharOverrun (Figure 15 and Figure 16).

No	Parameter	Min	Units
1	DI to SK Setup	10	ns
2	SK to D0 Valid	15	ns
3	SS to SK Setup	.5 Tsk	ns
4	SS to D0 Valid	15	ns
5	SK to DI Hold Time	10	ns

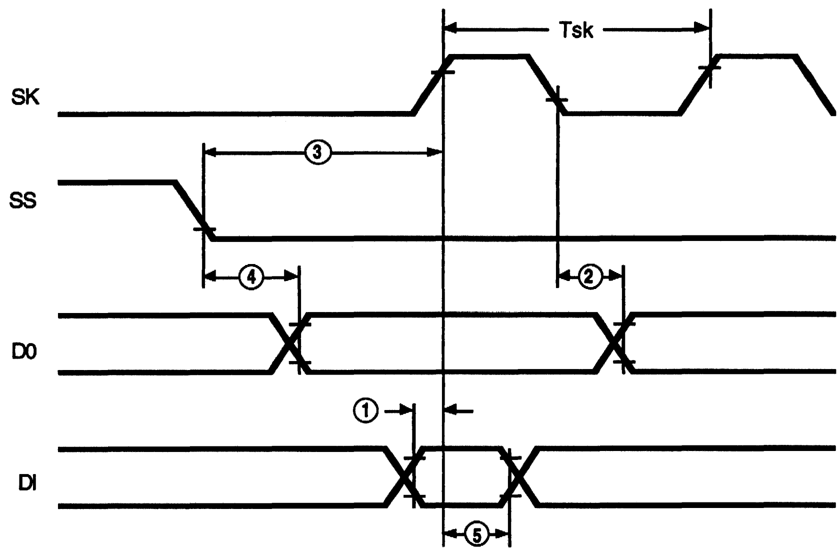


Figure 15. SPI Timing (Z86C06 Only)

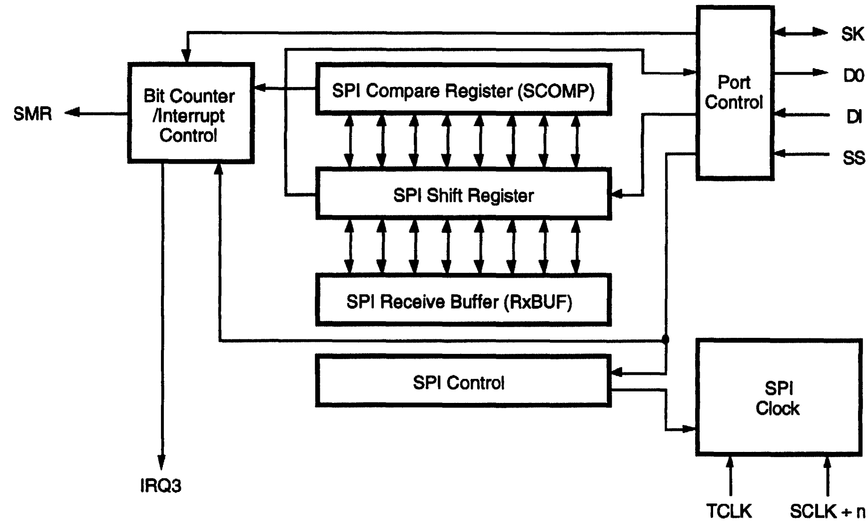


Figure 16. SPI Logic (Z86C06 Only)

PORT Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 17).

Comparator Output Port 3 (D0). Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34, and P35 and a 0 releases the Port to its standard I/O configuration.

Bits D4-D1. These bits are reserved and must be 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting D5=1. The default value is 1.

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting D6=1. The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive, it does not affect the relationship of SCLK and XTAL.

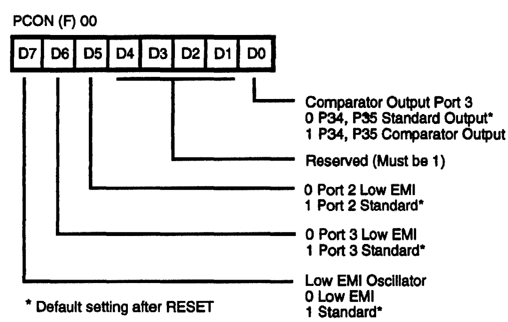


Figure 17. Port Configuration Register (PCON) (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP-Mode Recovery (Figure 18). All bits are Write Only except bit 7, which is Read Only. Bit 7 is a flag bit that is hardware set on the condition of a STOP recovery and reset on a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. The recovery level must be active Low to work with SPI. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR specify the source of the STOP-Mode Recovery signal. Bit 1 determines whether the XTAL is divided by 1 or 2. A 0 in this location uses XTAL divide-by-two, and a 1 uses XTAL. The default for this bit is XTAL divide-by-two. Bit 0 controls the divide-by-16 prescaler of SCLK/TCLK. The SMR is located in bank F of the Expanded Register Group at address 0BH.

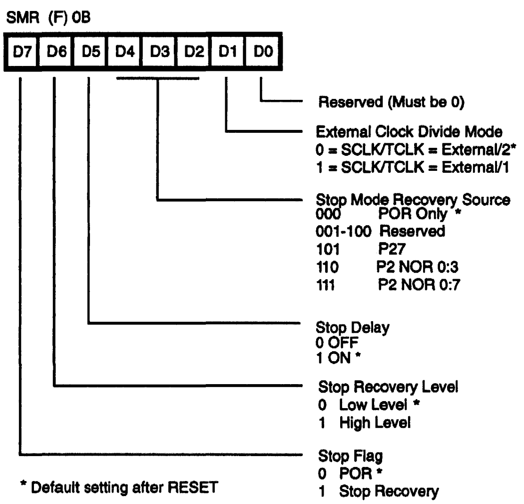


Figure 18a. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only.) (Z86C03)

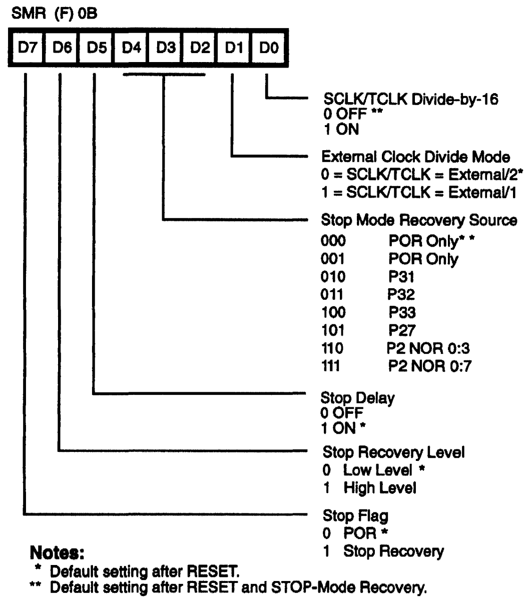


Figure 18b. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only.) (Z86C06)

SCLK/TCLK Divide-by-16 Select (D0)—Z86C06 Only. D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources the counter/timers and interrupt logic).

External Clock Divide Mode (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit, together with D7 of PCON, helps further lower EMI [i.e., D7 (PCON)=0, D1 (SMR=1]. The default setting is 0.

STOP-Mode Recovery Source (D2,D3,D4). These three bits of the SMR specify the wake-up source of the STOP-Mode Recovery (Figure 19 and Table 5).

Table 5. STOP-Mode Recovery Source

SMR D4	D3	D2	Operation Description of Action
0	0	0	POR recovery only
0	0	1	POR recovery only (C03 = Reserved)
0	1	0	P31 transition (C03 = Reserved)
0	1	1	P32 transition (C03 = Reserved)
1	0	0	P33 transition (C03 = Reserved)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0:3
1	1	1	Logical NOR of Port 2 bits 0:7

P31-P33 cannot wake up from STOP Mode if the input lines are configured as analog inputs. In the Z86C06, when the SPI is enabled and the Compare feature is active, a SMR is generated upon a comparison in the SPI Shift Register and SCOMP Register, regardless of the above SMR Register settings. If SPI Compare is used to wake up the part from STOP Mode, it is still possible to have one of the other STOP-Mode Recovery sources active. **Note:** These other STOP- Mode Recovery sources have to be active level Low (bit D6 in SMR set to 0 if P31, P32, P33, and P27 selected, or bit D6 in SMR set to 1 if logical NOR of Port 2 is selected).

STOP-Mode Recovery Delay Select (D5). This bit disables the 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the "fast" wake up is selected, the STOP-Mode Recovery source needs to be kept active for at least 5 TpC.

STOP-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 19).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. It is active High, and is 0 (cold) on POR/WDT RESET. This bit is Read Only. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

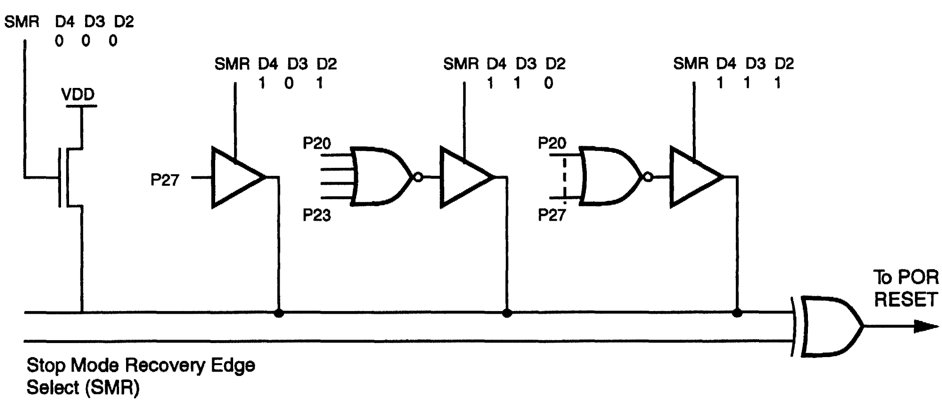
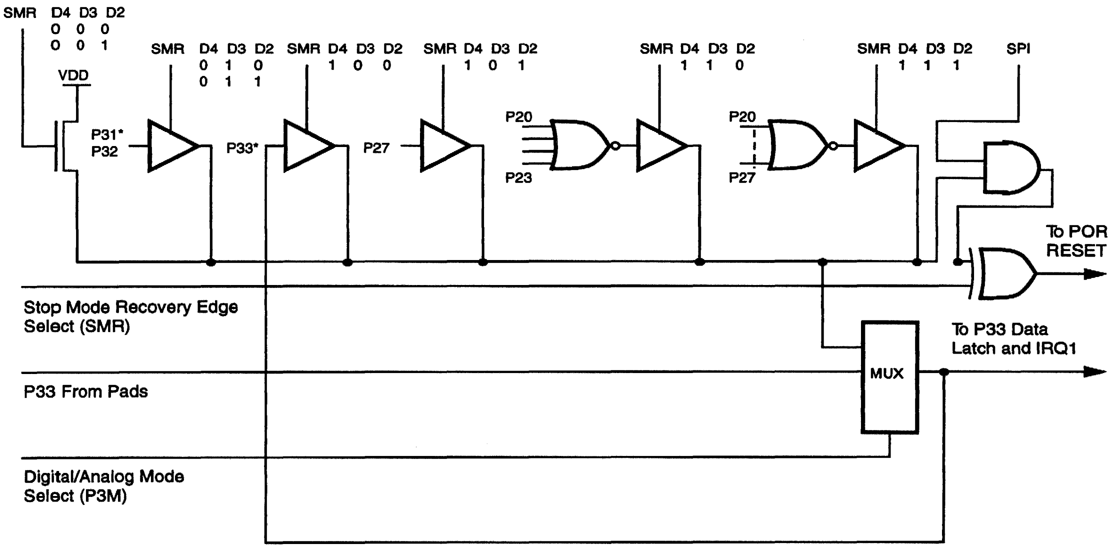


Figure 19a. STOP-Mode Recovery Source (Z86C03)

FUNCTIONAL DESCRIPTION (Continued)



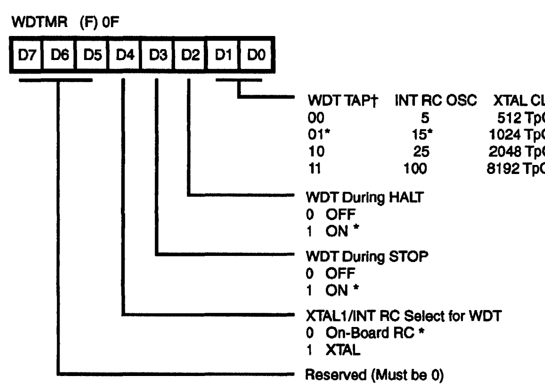
*Note: P31, P32 and P33 are not in Analog Mode.

Figure 19b. STOP-Mode Recovery Source (Z86C06)

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled after it has been initially enabled. The WDT circuit is driven by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDTMR register.

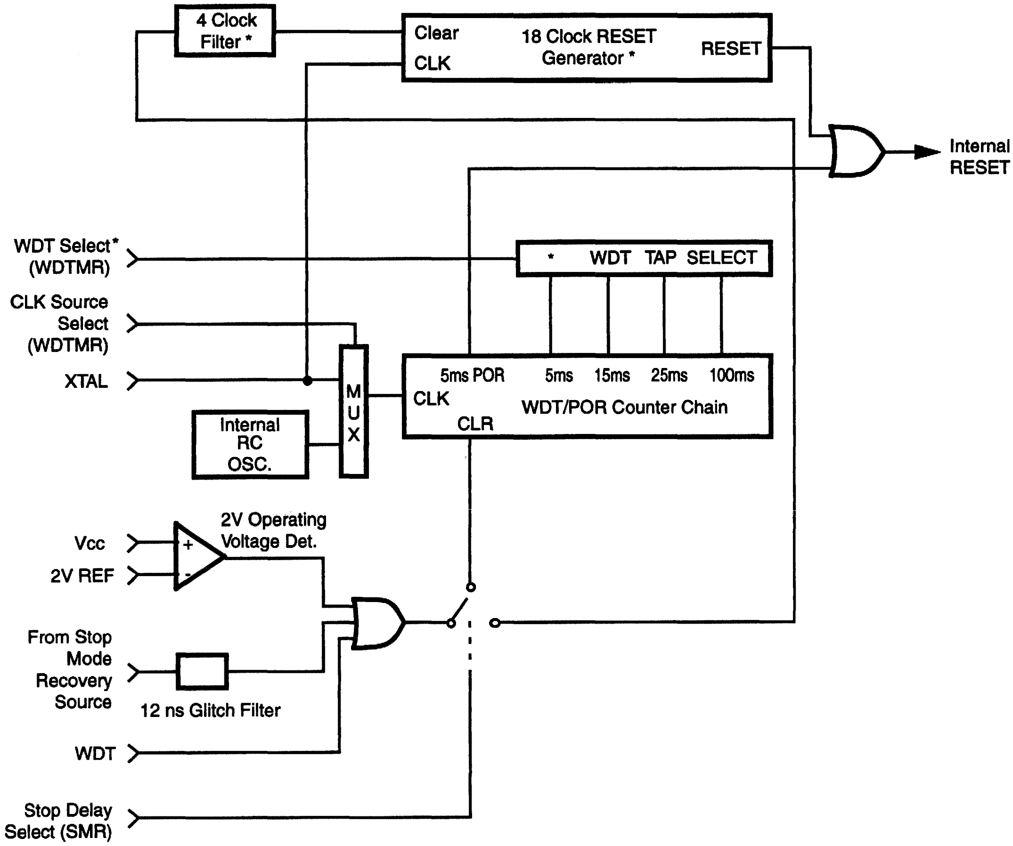
Note: Execution of the WDT instruction affects the Z (zero), S (sign), and V (overflow) flags.

Bits 0 and 1 control a tap circuit that determines the timeout period (on Z86C06 only). Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to 1, the WDT is only driven by the external clock during STOP mode. This feature makes it possible to wake up from STOP mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 20). ***Note: This register is accessible only during the first 64 processor cycles (128 XTAL clocks) from the execution of the first instruction after Power-On Reset, Watch-Dog Reset or a STOP Mode Recovery (Figure 21). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH.***



* Default setting after RESET
† Must be 01 for Z86C03

Figure 20. Watch-Dog Timer Mode Register (Write Only)



* Not available on the Z86C03, WDT fixed at 15 ms/1024TpC in the Z86C03.

Figure 21. Resets and WDT

FUNCTIONAL DESCRIPTION (Continued)

WDT Time Select (D1, D0). Bits 0 and 1 control a tap circuit that determines the time-out period. Table 6 shows the different values that can be obtained. The default value of D0 and D1 are 1 and 0, respectively. These select bits are present in the Z86C06 only.

Table 6. Time-Out Period of the WDT (Z86C06 Only)

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256TpC
0	1	15 ms min	512TpC
1	0	25 ms min	1024TpC
1	1	100 ms min	4096TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 15 ms, D0 = 1 and D1 = 0.
See Figures 53 to 56 for details.
The values given are for V_{CC} = 5.0V.
For the Z86C03, the WDT time-out value is fixed at 1024 TpC (depending on WDTMR bit D4) period. When writing to the WDTMR in the Z86C03, bit D0 must be 1 and D1 must be 0.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1. If bits D3 and D4 are both set to 1, the WDT only, is driven by the external clock during STOP mode.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the internal RC oscillator.

Bits 5, 6 and 7. These bits are reserved.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the specified voltage (typically 2.1V).

Low Voltage Protection (V_{LV}). The Low Voltage Protection trip point (V_{LV}) will be less than 3 volts and above 1.4 volts under the following conditions.

Maximum (V_{LV}) Conditions:

Case 1: T_A = –40° to +105°C, Internal Clock (SCLK) Frequency equal or less than 1 MHz

Case 2: T_A = –40° to +85°C, Internal Clock (SCLK) Frequency equal or less than 2 MHz

Note: The internal clock frequency (SCLK) is determined by SMR (F) 0BH bit D1.

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device is guaranteed to function normally until the Low Voltage Protection trip point (V_{LV}) is reached, for the temperatures and operating frequencies in cases 1 and 2 above. The actual low voltage trip point is a function of temperature and process parameters (Figure 22).

1

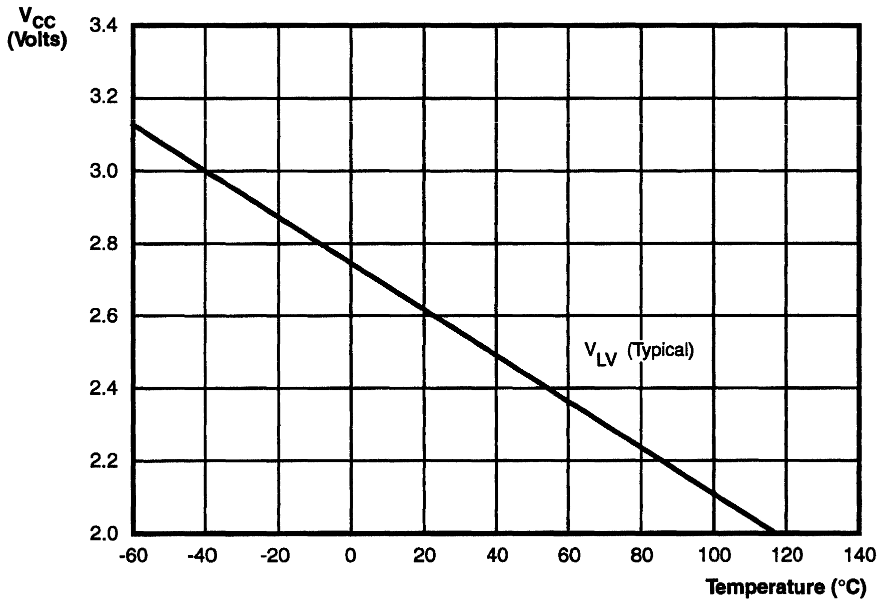


Figure 22. Typical Z86C03/C06 V_{LV} Voltage vs Temperature

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
V_{IHM}	Max Input Voltage**		12	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp	†		°C

Notes:
* Voltage on all pins with respect to GND.
** Applies to Port pins only and must limit current going into or out of Port pins to 250 μA maximum.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 23).

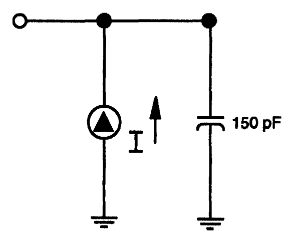


Figure 23. Test Load Configuration

CAPACITANCE

T_A = 25° C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input Capacitance	0	12 pF
Output Capacitance	0	20 pF
I/O Capacitance	0	25 pF

V_{CC} SPECIFICATION

V_{CC} = 3.0V to 5.5V

DC ELECTRICAL CHARACTERISTICS
Z86C03/C06

1

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	T_A = 0°C to +70°C Max	T_A = −40°C to +105°C Min	T_A = −40°C to +105°C Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.9 V_{CC}	V_{CC}+0.3	0.9 V_{CC}	V_{CC}+0.3	2.4	V	Driven by External Clock Generator	
		5.5V	0.9 V_{CC}	V_{CC}+0.3	0.9 V_{CC}	V_{CC}+0.3	3.9	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}−0.3	0.2 V_{CC}	V_{SS}−0.3	0.2 V_{CC}	1.6	V	Driven by External Clock Generator	
		5.5V	V_{SS}−0.3	0.2 V_{CC}	V_{SS}−0.3	0.2 V_{CC}	2.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	3.0V	V_{SS}−0.3	0.2 V_{CC}	V_{SS}−0.3	0.2 V_{CC}	1.0	V		
		5.5V	V_{SS}−0.3	0.2 V_{CC}	V_{SS}−0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.0V	V_{CC}−0.4		V_{CC}−0.4		3.1	V	I_{OH} = -2.0 mA	[10]
		5.5V	V_{CC}−0.4		V_{CC}−0.4		4.8	V	I_{OH} = -2.0 mA	[10]
V_{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.2	V	I_{OL} = +4.0 mA	[10]
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	[10]
V_{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.4	V	I_{OL} = + 6 mA, 3 Pin Max	[10]
		5.5V		1.0		1.0	0.5	V	I_{OL} = +12 mA, 3 Pin Max	[10]
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		
		5.5V		25		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	3.0V	0V	V_{CC}−1.0v	0V	V_{CC}−1.5v				[7]
		5.5V	0V	V_{CC}−1.0v	0V	V_{CC}−1.5v				[7]
I_{IL}	Input Leakage (Input bias current of comparator)	3.0V	−1.0	1.0	−1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	−1.0	1.0	−1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	−1.0	1.0	−1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	−1.0	1.0	−1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	3.2V					8.0	µA	@32 kHz	[13]
		3.0V		6		6	3.0	mA	@ 8 MHz	[4,5,10]
		5.5V		11.0		11.0	6.0	mA	@ 8 MHz	[4,5,10]
		3.0V		8.0		8.0	4.5	mA	@ 12 MHz	[4,5,10,11]
		5.5V		15		15	9.0	mA	@ 12 MHz	[4,5,10,11]

DC ELECTRICAL CHARACTERISTICS
Z86C03/C06

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	3.0V		3.0		3.0	1.3	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 8 MHz	[4, 5,10]
		5.5V		5		5	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 8 MHz	[4, 5,10]
		3.0V		4.5		4.5	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 12 MHz	[4, 5,10,11]
		5.5V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4, 5,10,11]
		3.0V		1.4		1.4	0.7	mA	Clock Divide-by-16 @ 8 MHz	[4, 5,10]
		5.5V		3.5		3.5	2.0	mA	Clock Divide-by-16 @ 8 MHz	[4, 5,10]
		3.0V		2.0		2.0	1.0	mA	Clock Divide-by-16 @ 12 MHz	[4, 5,10,11]
		5.5V		4.5		4.5	2.5	mA	Clock Divide-by-16 @ 12 MHz	[4, 5,10,11]
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6, 9]
		5.5V		10		20	3.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6, 9]
		3.0V		600		600	400	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6, 9,12]
		5.5V		1000		1000	800	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6, 9,12]
I_{ALL}	Auto Latch Low Current	3.0V		7.0		14.0	4.0	µA	0V < V_{IN} < V_{CC}	
		5.5V		20.0		30.0	10	µA	0V < V_{IN} < V_{CC}	
I_{ALH}	Auto Latch High Current	3.0V		−4.0		−8.0	−2.0	µA	0V < V_{IN} < V_{CC}	
		5.5V		−9.0		−16.0	−5.0	µA	0V < V_{IN} < V_{CC}	
V_{LV}	V_{CC} Low Voltage Protection Voltage		1.50	2.95	1.2	2.95	2.1	V	2 MHz max Ext. CLK Freq.	[3]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven on XTAL	0.3	5.0	mA	8 MHz
Crystal or Ceramic Resonator	3.0	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND
[3] V_{CC} = 3.0V to 5.5V. The V_{LV} increases as the temperature decreases. Typical values measured at 3.3V and 5.0V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] C_{L1} = C_{L2} = 100 pF
[6] Same as note [4] except inputs at V_{CC}.
[7] For analog comparator inputs when analog comparators are enabled.
[8] Excludes clock pins.
[9] Clock must be forced Low when XTAL1 is clock-driven and XTAL2 is floating.
[10] STD mode (not low EMI mode).
[11] Z86C06 only
[12] Internal RC is WDT clock source.
[13] C_{L1} = 100 pF, C_{L2} = 220 pF

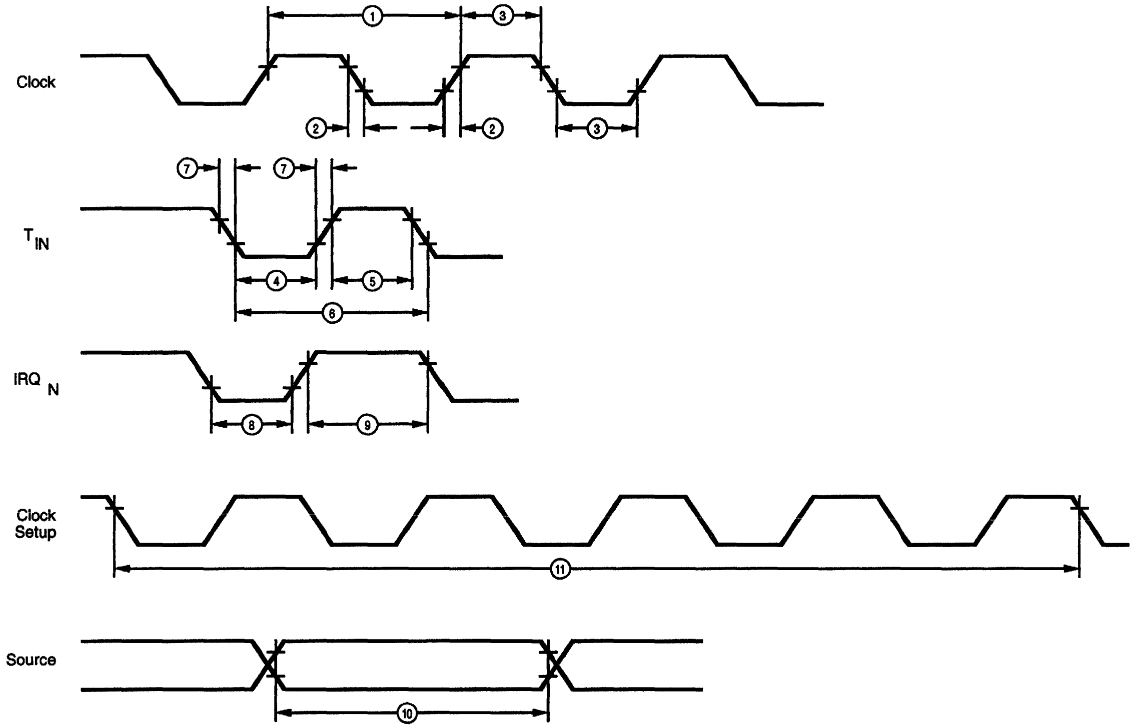


Figure 24. Additional Timing

AC ELECTRICAL CHARACTERISTICS

(SCLK/TCLK = EXTERNAL/2)

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C 8 MHz [11] Min	Max	12 MHz [11] Min	Max	T_A = –40°C to +105°C 8 MHz [11] Min	Max	12 MHz [11] Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	125	DC	83	DC	ns	[1,7]
			5.5V	125	DC	83	DC	125	DC	83	DC	ns	[1,7]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15		25		15	ns	[1,7]
			5.5V		25		15		25		15	ns	[1,7]
3	TwC	Input Clock Width	3.0V	62		41		62		41		ns	[1,7]
			5.5V	62		41		62		41		ns	[1,7]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1,7]
			5.5V	70		70		70		70		ns	[1,7]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			[1,7]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,7]

AC ELECTRICAL CHARACTERISTICS (Continued)
(SCLK/TCLK = EXTERNAL/2)

				T_A = 0°C to +70°C				T_A = –40°C to +105°C					
			V_{CC}	8 MHz[11]		12 MHz[11]		8 MHz[11]		12 MHz[11]			
No	Symbol	Parameter	Note [3]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			[1,7]
			5.5V	8TpC		8TpC		8TpC		8TpC			[1,7]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100		100		100	ns	[1,7]
			5.5V		100		100		100		100	ns	[1,7]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	[1,2]
			5.5V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1,2]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,2]
10	Twsm	STOP-Mode Recovery Width Spec	3.0V	5TpC		5TpC		5TpC		5TpC			[8,10]
			5.5V	5TpC		5TpC		5TpC		5TpC			[8,10]
11	Tost	Oscillator Startup Time	3.0V	12		12		12		12		ns	[4,9]
			5.5V	12		12		12		12		ns	[4,9]
12	Twdt	Watch-Dog Timer Refresh Time	3.0V	15		15		12		12		ms	D0 = 0 [5,6,12]
			5.5V	5		5		3		3		ms	D1 = 0 [5,6,12]
			3.0V	30		30		25		25		ms	D0 = 1 [5,6]
			5.5V	16		16		12		12		ms	D1 = 0 [5,6]
			3.0V	60		60		50		50		ms	D0 = 0 [5,6,12]
			5.5V	25		25		30		30		ms	D1 = 1 [5,6,12]
			3.0V	250		250		200		200		ms	D0 = 1 [5,6,12]
			5.5V	120		120		100		100		ms	D1 = 1 [5,6,12]
13	T_{POR}	Power-On Reset	3.0V	7		24		6		25	13	ms	
			5.5V	3		13		2		14	7	ms	

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] V_{CC} = 3.0V to 5.5V.
[4] SMR-D5 = 0.
[5] WDTMR Register
[6] Internal RC Oscillator only.
[7] SMR D1 = 0.
[8] Maximum frequency for internal system clock is 4 MHz when using SCLK = EXTERNAL clock mode.
[9] For RC and LC oscillator and for clock-driven oscillator.
[10] SMR-D5 = 1, STOP-Mode Recovery delay is on.
[11] Z86C03 = 8 MHz; Z86C06 = 12 MHz.
[12] Z86C06 only.

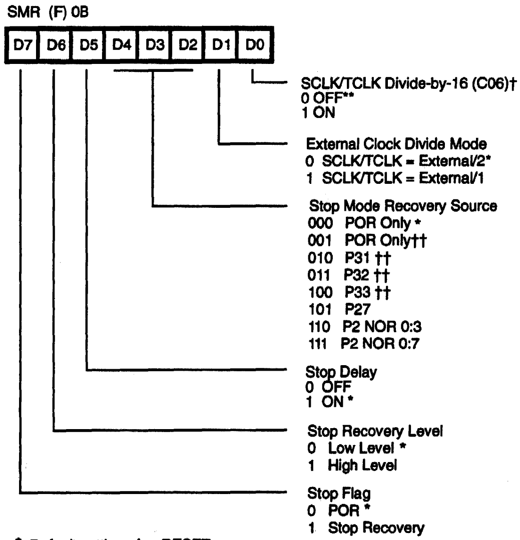
1

AC ELECTRICAL CHARACTERISTICS
Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = EXTERNAL)

No	Symbol	Parameter	V_{CC} Note [6]	T_A = 0°C to +70°C 4 MHz Min	Max	T_A = −40°C to +105°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	[1,7,8]
			5.5V	250	DC	250	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25	ns	[1,7,8]
			5.5V		25		25	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	125		125		ns	[1,7,8]
			5.5V	125		125		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			[1,7,8]
			5.5V	3TpC		3TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1,7,8]
			5.5V	4TpC		4TpC			[1,7,8]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	[1,7,8]
			5.5V		100		100	ns	[1,7,8]
8	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,7,8]
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			[1,2,7,8]
			5.5V	3TpC		2TpC			[1,2,7,8]
10	Twsm	STOP-Mode Recovery Width Spec	3.0V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		[3,8,9]
			5.5V		5TpC		5TpC		[3,8,9]

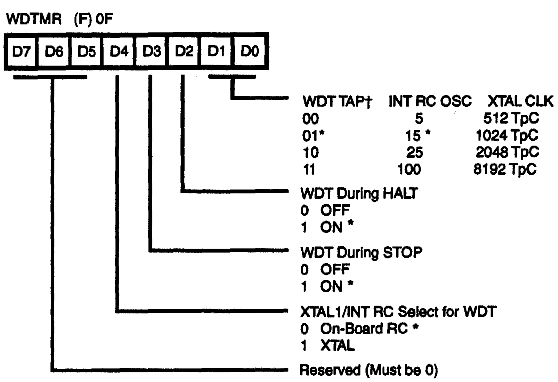
Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P33-P31).
[3] SMR-D5 = 0.
[4] SMR-D5 = 1, POR STOP mode delay is on.
[5] Reg. WDTMR.
[6] V_{CC} = 3.0V to 5.5V.
[7] SMR D1 = 1.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.

EXPANDED REGISTER FILE CONTROL REGISTERS



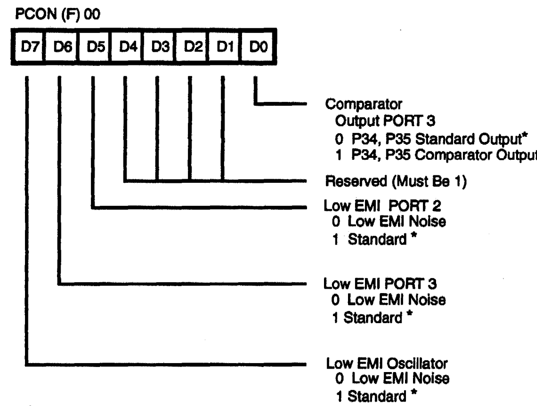
* Default setting after RESET.
** Default setting after STOP-Mode Recovery and RESET.
† C03 Reserved; must be 0.
†† C06 Only

Figure 25. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only)



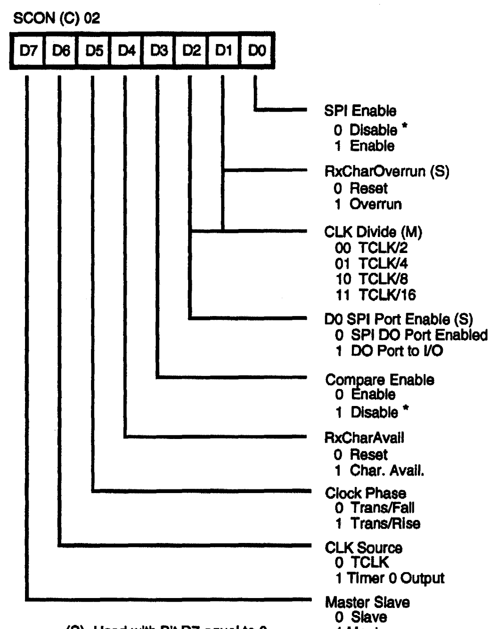
* Default setting after RESET
† For C06; C03 Must Be D0 = 1, D1 = 0

Figure 26. Watch-Dog Timer Mode Register (Write Only)



* Default Setting After Reset.

Figure 27. PORT Control Register (Write Only)



(S) Used with Bit D7 equal to 0
(M) Used with Bit D7 equal to 1

* Default Setting After Reset.

Figure 28. SPI Control Register (Z86C06 Only)

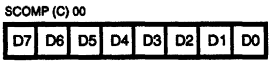


Figure 29. SPI Compare Register (Z86C06 Only)

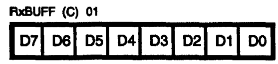


Figure 30. SPI Receive Buffer (Z86C06 Only)

Z8 CONTROL REGISTER DIAGRAMS

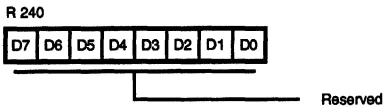


Figure 31. Reserved

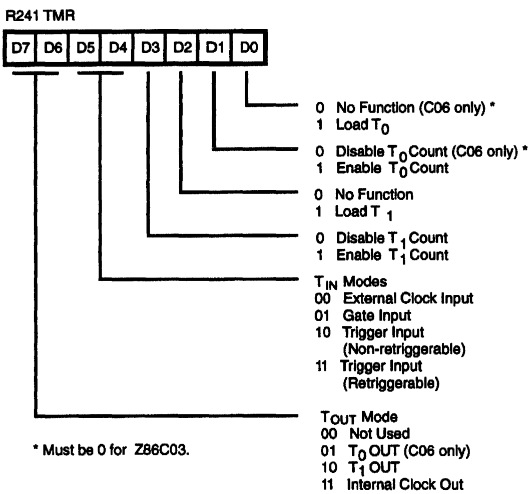


Figure 32. Timer Mode Register ($F1_H$: Read/Write)

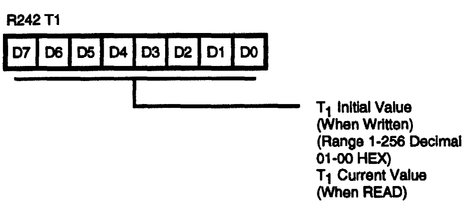


Figure 33. Counter Timer 1 Register ($F2_H$: Read/Write)

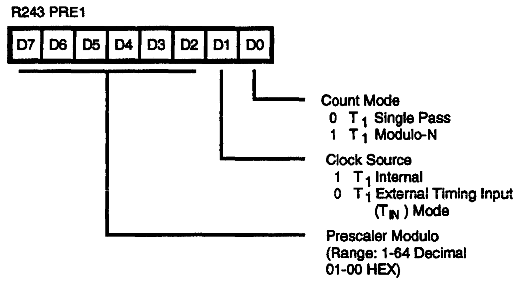


Figure 34. Prescaler 1 Register ($F3_H$: Write Only)

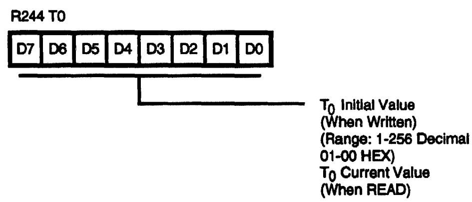


Figure 35. Counter/Timer 0 Register ($F4_H$: Read/Write; Z86C06 Only)

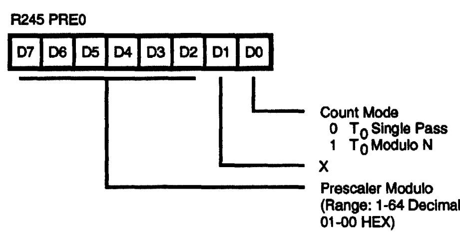


Figure 36. Prescaler 0 Register ($F5_H$: Write Only; Z86C06 Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

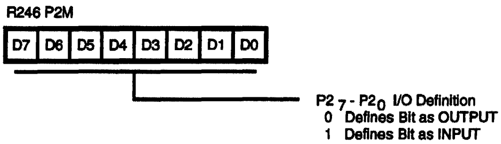


Figure 37. Port 2 Mode Register ($F6_H$: Write Only)

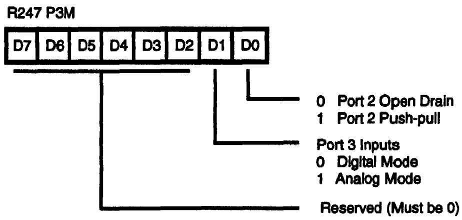


Figure 38. Port 3 Mode Register ($F7_H$: Write Only)

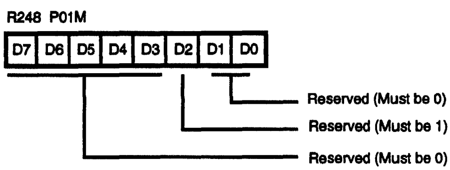


Figure 39. Port 0 and 1 Mode Register ($F8_H$: Write Only)

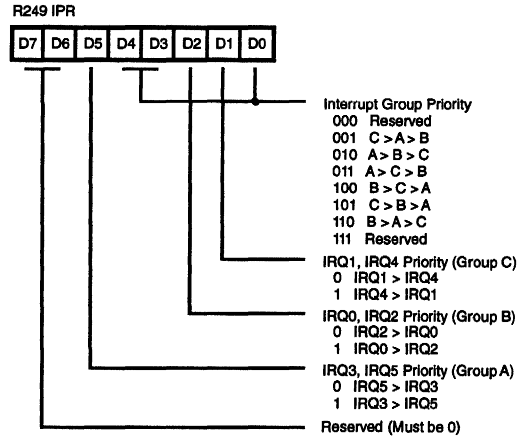


Figure 40. Interrupt Priority Register ($F9_H$: Write Only)

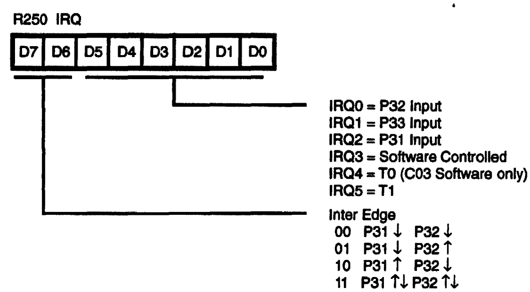


Figure 41. Interrupt Request Register (FA_H: Read/Write)

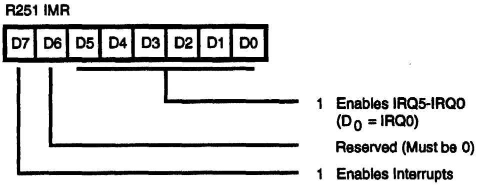


Figure 42. Interrupt Mask Register (FB$_H$: Read/Write)

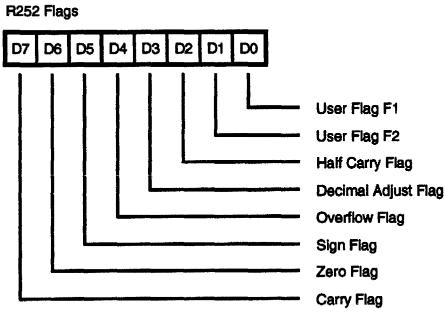


Figure 43. Flag Register (FC$_H$: Read/Write)

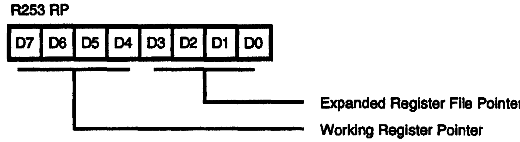


Figure 44. Register Pointer (FD$_H$: Read/Write)

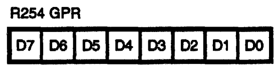


Figure 45. General Purpose Register (FE$_H$: Read/Write)

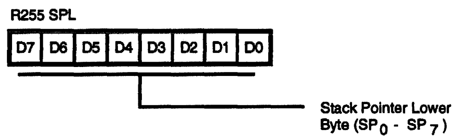


Figure 46. Stack Pointer (FF$_H$: Read/Write)

DEVICE CHARACTERISTICS

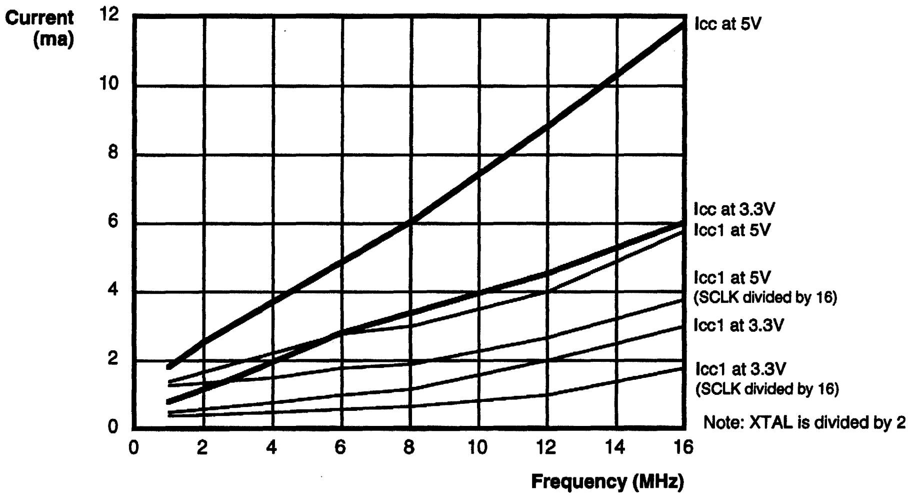


Figure 47. Typical I_{CC} vs Frequency

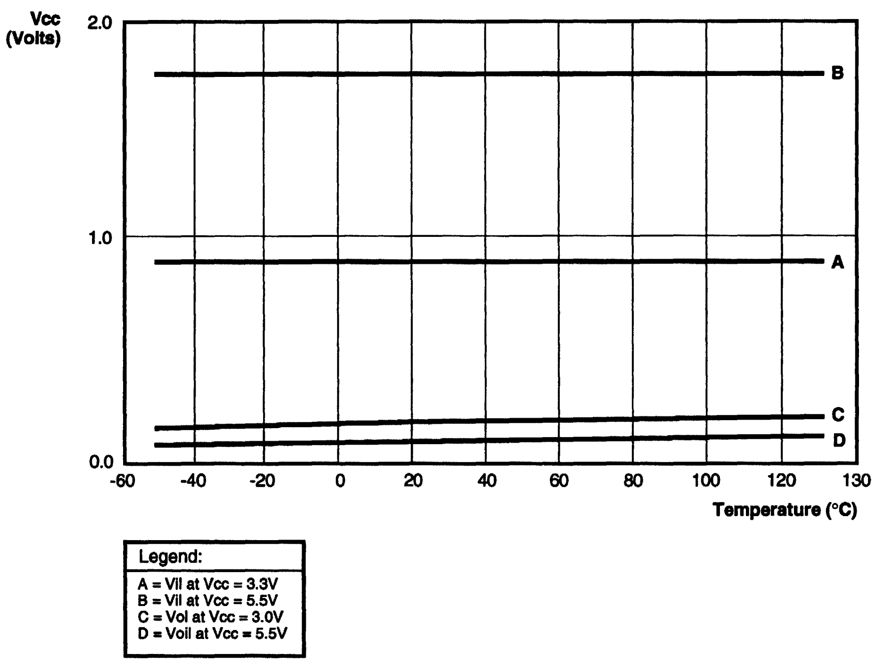


Figure 48. Typical V_{OL}, V_{IL} vs Temperature

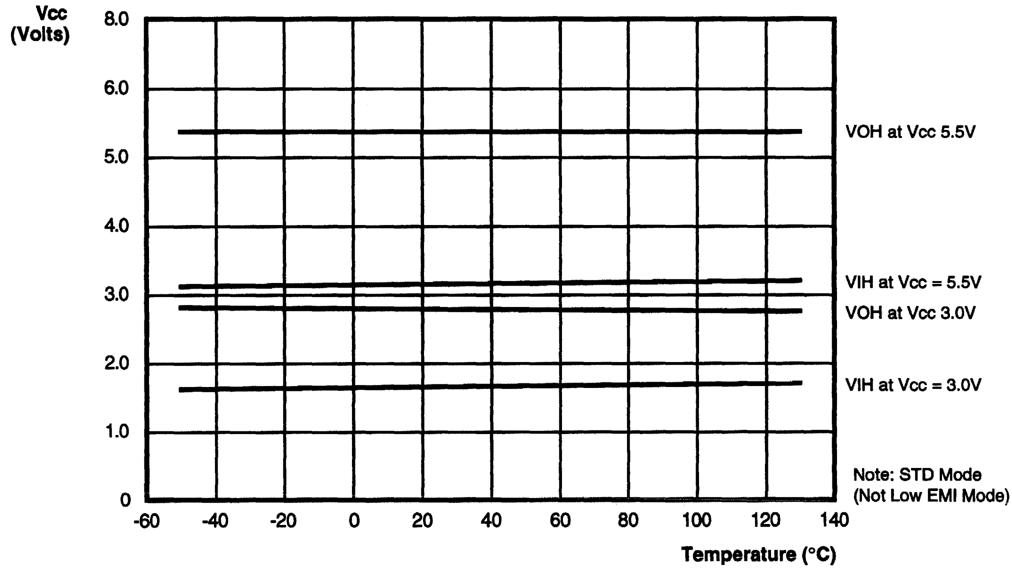


Figure 49. Typical V_{OH}, V_{IH} vs Temperature

DEVICE CHARACTERISTICS (Continued)

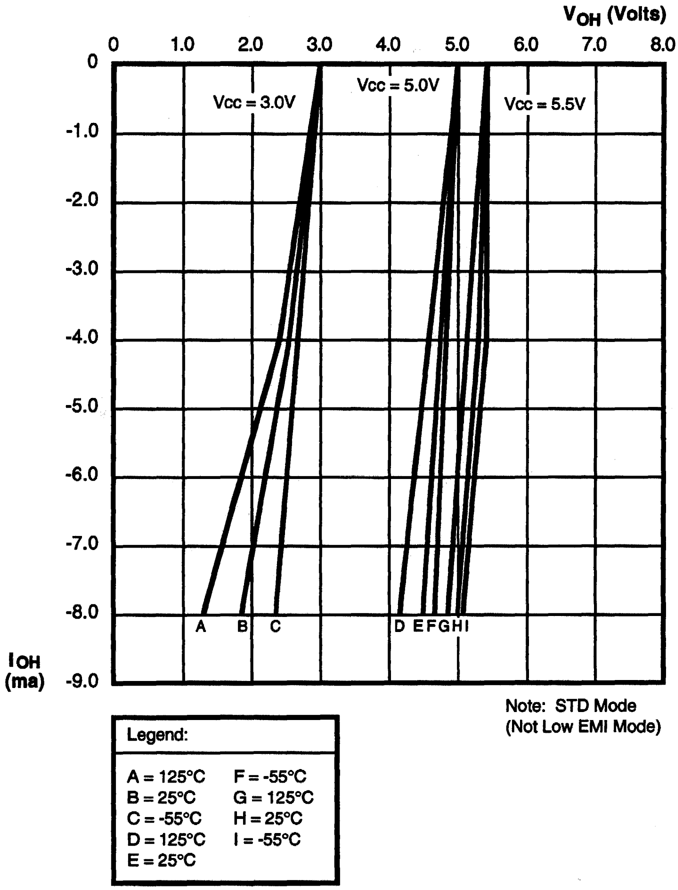


Figure 50. Typical V_{OH} vs I_{OH} Over Temperature

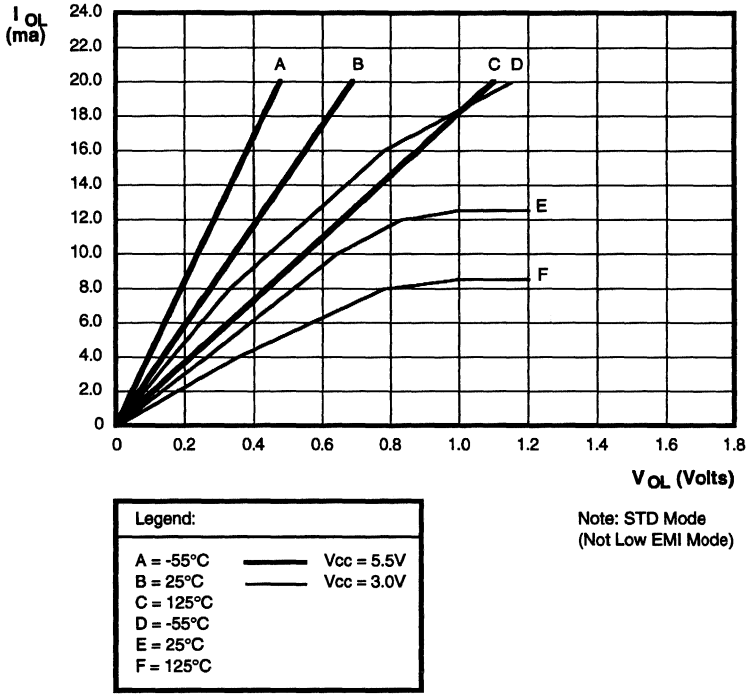
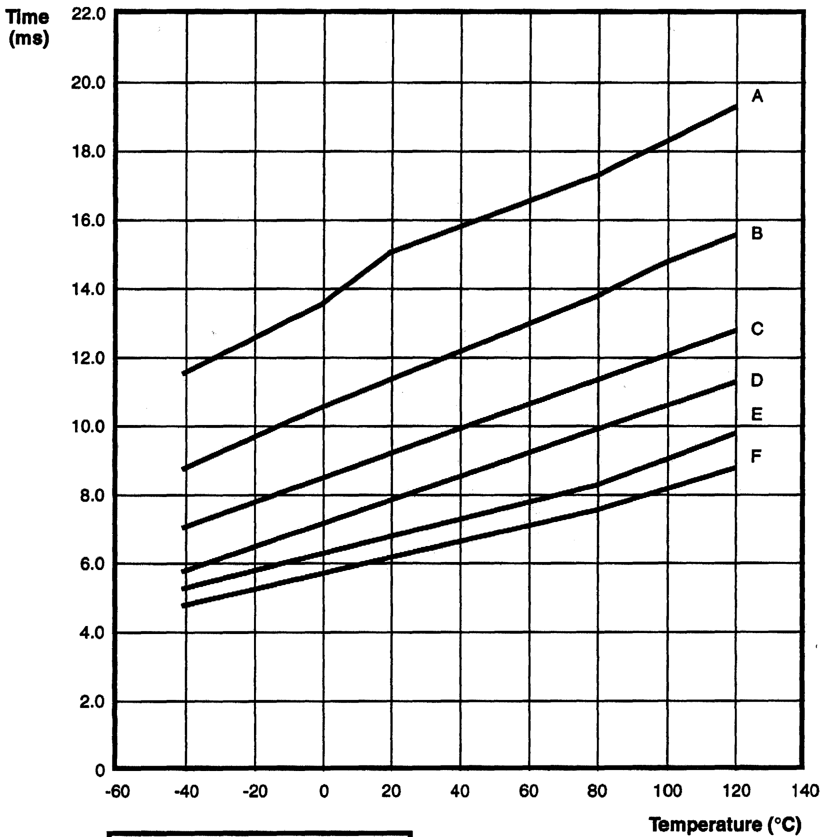


Figure 51. Typical I_{OL} vs V_{OL} Over Temperature

DEVICE CHARACTERISTICS (Continued)



Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Note: Using internal RC.

Figure 52. Typical Power-On Reset Time vs Temperature

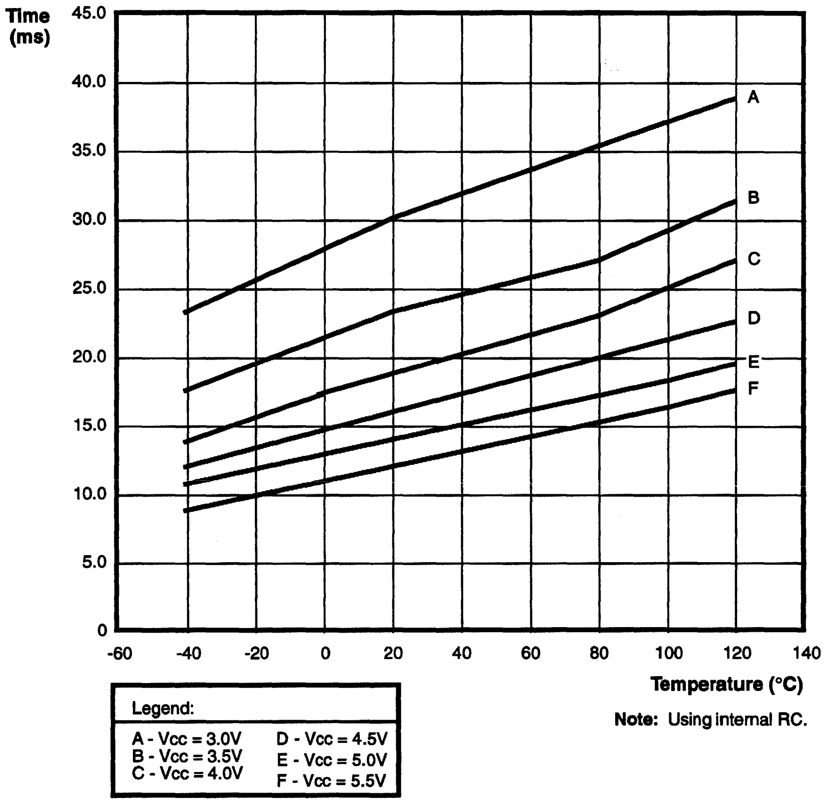
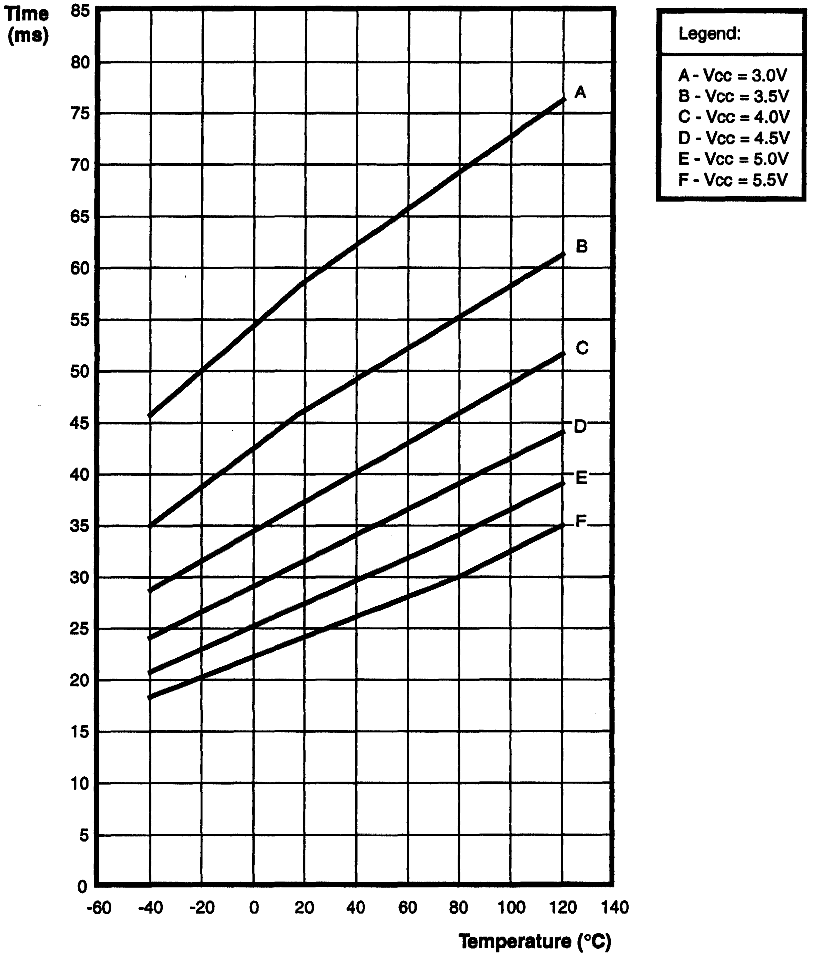


Figure 53. Typical 5 ms WDT Setting vs Temperature (Z86C06 Only)

DEVICE CHARACTERISTICS (Continued)



Note: Using internal RC.

Figure 54. Typical 15 ms WDT Setting vs Temperature

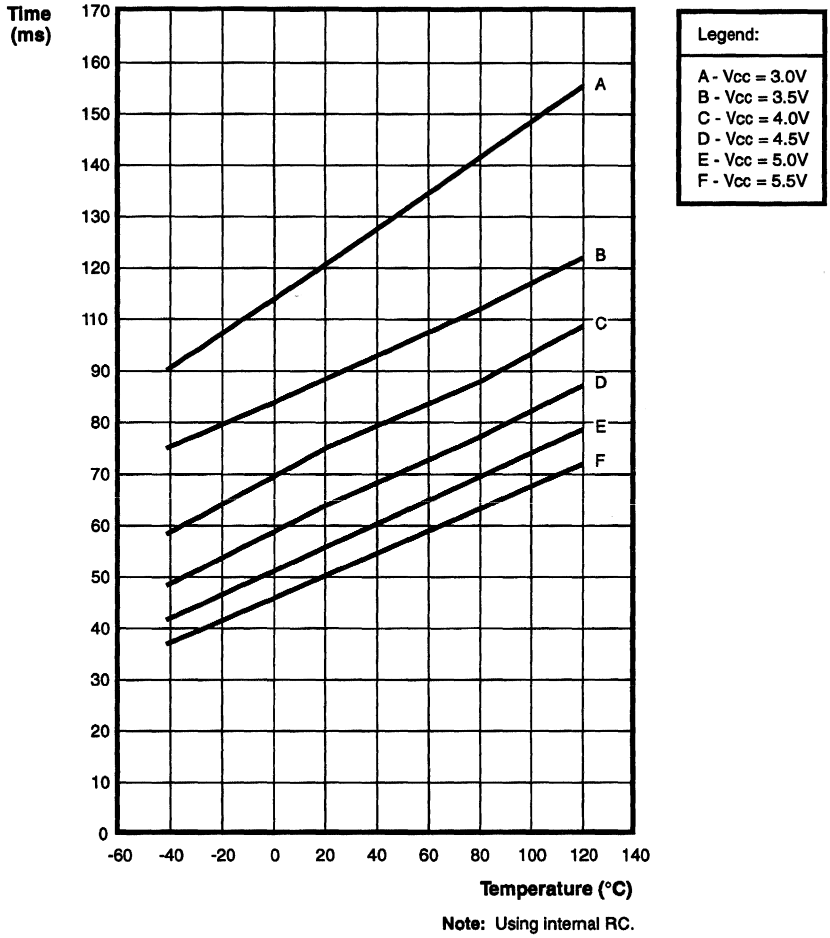
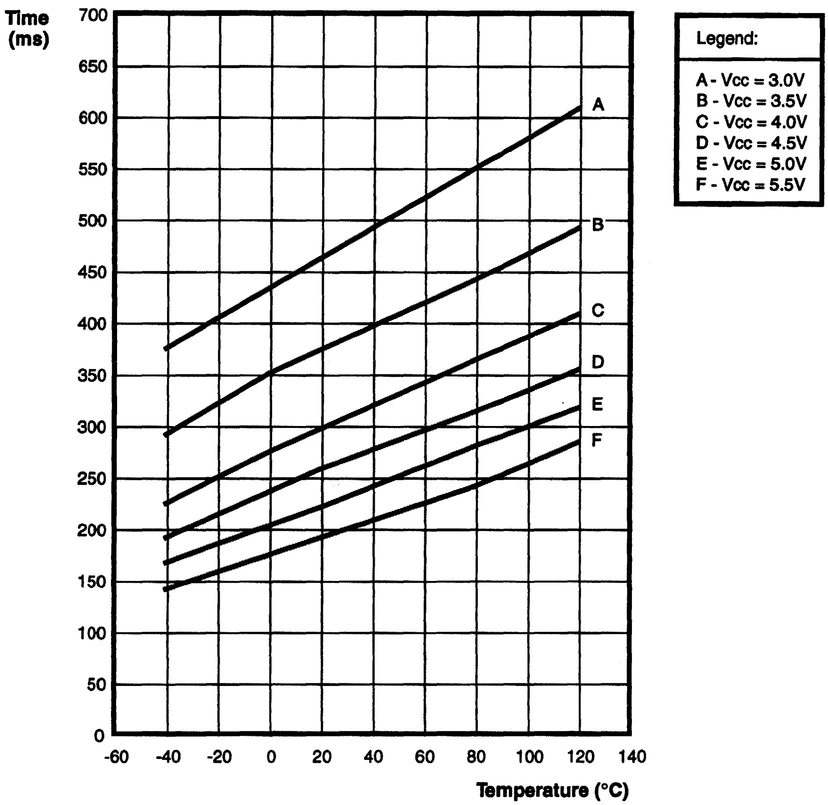


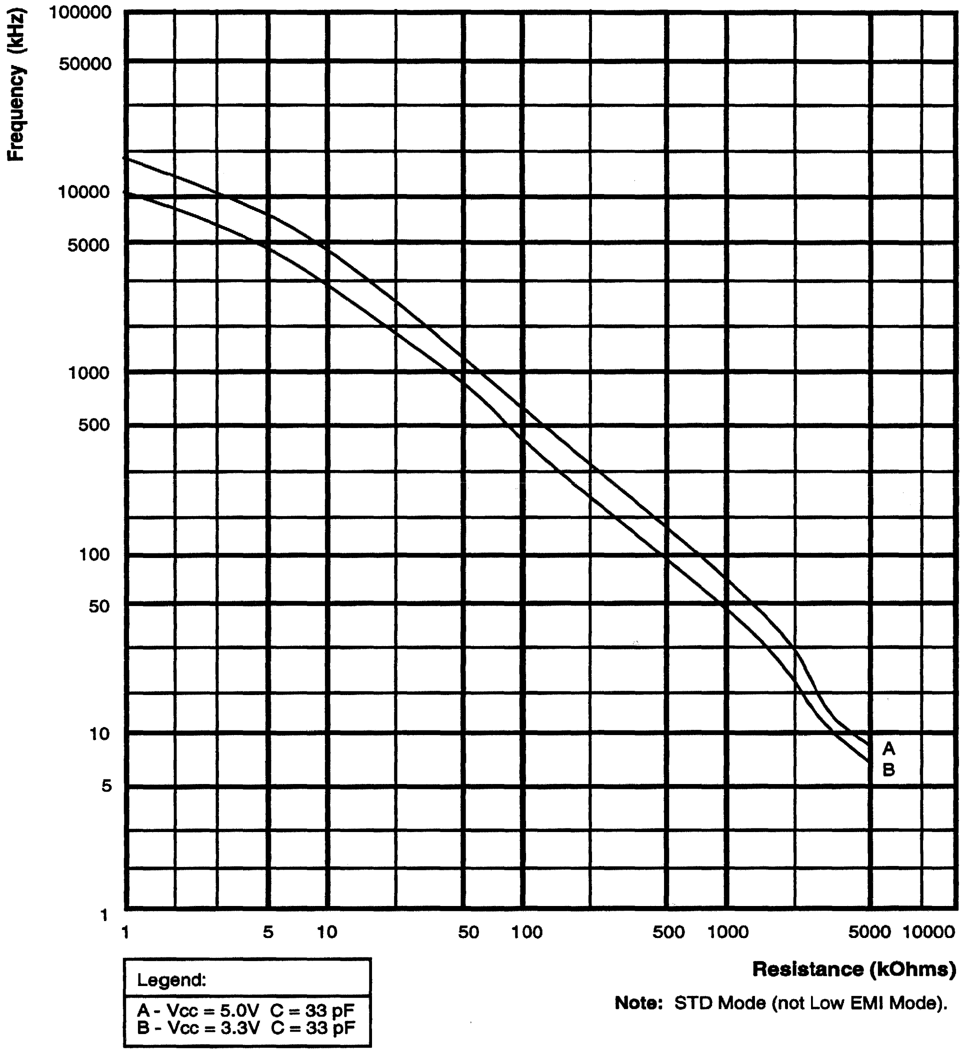
Figure 55. Typical 25 ms WDT Setting vs Temperature (Z86C06 Only)

DEVICE CHARACTERISTICS (Continued)



Note: Using internal RC.

Figure 56. Typical 100 ms WDT Setting vs Temperature (Z86C06 Only)



Note: STD Mode (not Low EMI Mode).

Note: This chart for reference only. Each process will have a different characteristic curve.

Figure 57. Typical Frequency vs RC Resistance

DEVICE CHARACTERISTICS (Continued)

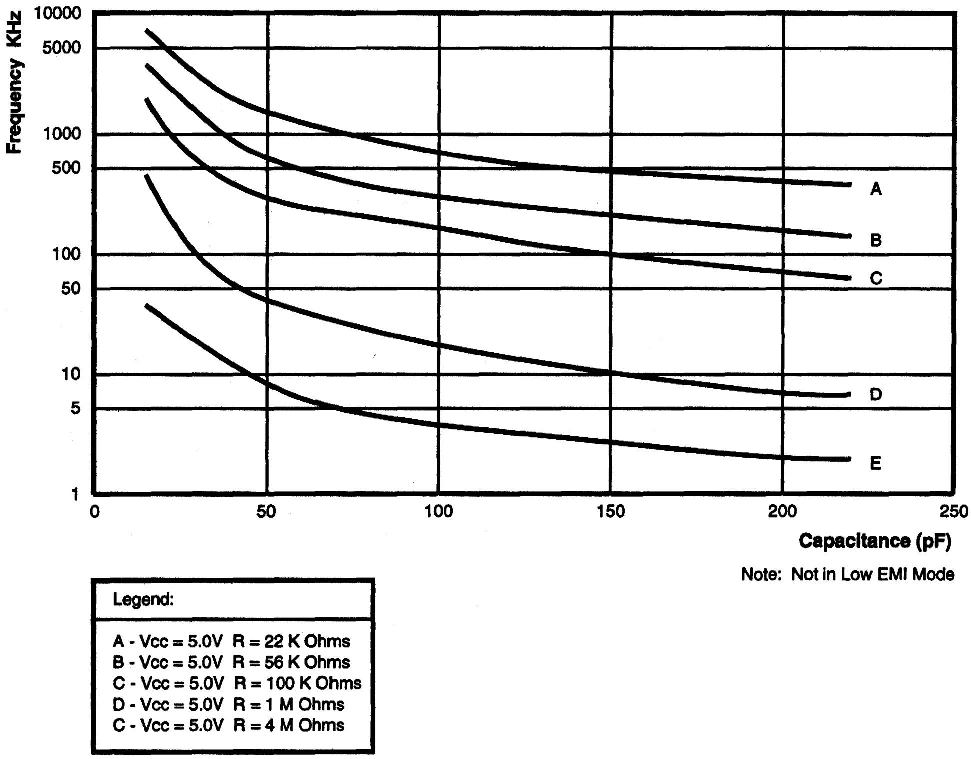


Figure 58. Typical RC Resistance/Capacitance vs Frequency

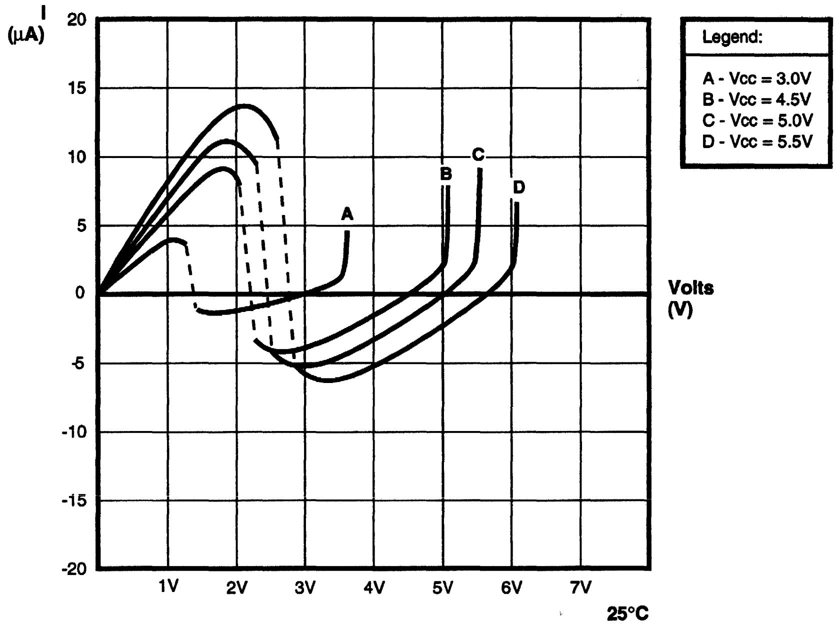


Figure 59. Auto Latch Characteristics

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR address	Register pair or working register pair

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

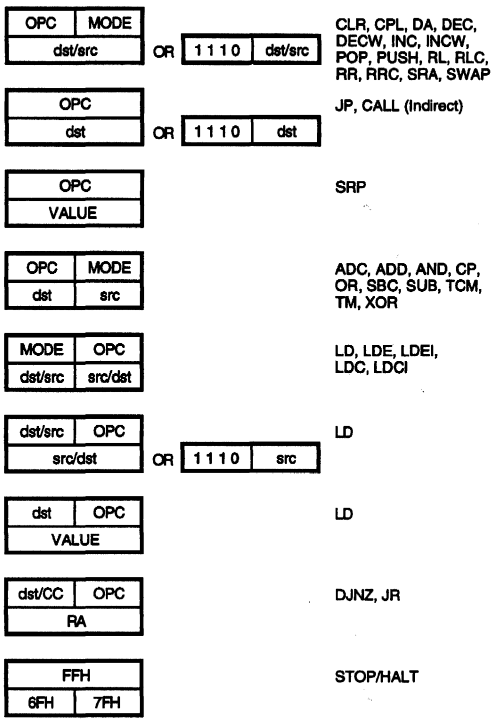
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

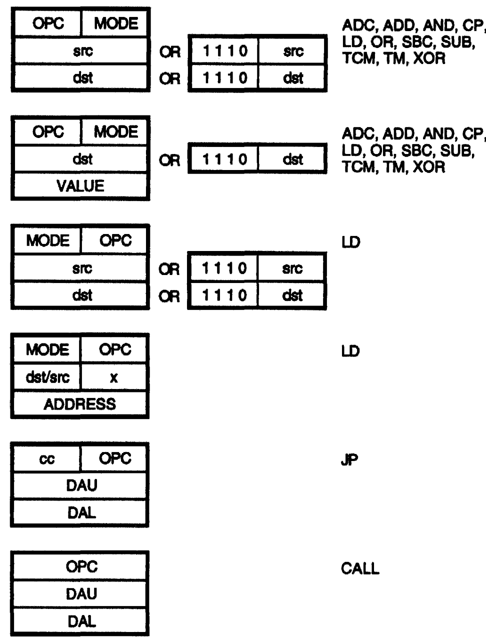
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

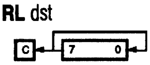
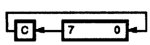
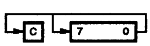
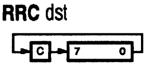
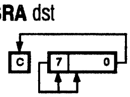
refers to bit 7 of the destination operand.

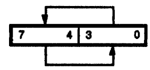
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src	†		1[ ]	*	*	*	*	0	*
dst←dst + src +C									
ADD dst, src	†		0[ ]	*	*	*	*	0	*
dst←dst + src									
AND dst, src	†		5[ ]	-	*	*	0	-	-
dst←dst AND src									
CALL dst	DA		D6	-	-	-	-	-	-
SP←SP - 2	IRR		D4						
@SP←PC,									
PC←dst									
CCF			EF	*	-	-	-	-	-
C←NOT C									
CLR dst	R		B0	-	-	-	-	-	-
dst←0	IR		B1						
COM dst	R		60	-	*	*	0	-	-
dst←NOT dst	IR		61						
CP dst, src	†		A[ ]	*	*	*	*	-	-
dst - src									
DA dst	R		40	*	*	*	X	-	-
dst←DA dst	IR		41						
DEC dst	R		00	-	*	*	*	-	-
dst←dst - 1	IR		01						
DECW dst	RR		80	-	*	*	*	-	-
dst←dst - 1	IR		81						
DI			8F	-	-	-	-	-	-
IMR(7)←0									
DJNZr, dst	RA		rA	-	-	-	-	-	-
r←r - 1			r = 0 - F						
if r ≠ 0									
PC←PC + dst									
Range: +127, 128									
EI			9F	-	-	-	-	-	-
IMR(7)←1									
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	C	Z	S	V	D	H
INC dst	r		rE	-	*	*	*	-	-
dst←dst + 1			r = 0 - F						
	R		20						
	IR		21						
INCW dst	RR		A0	-	*	*	*	-	-
dst←dst + 1	IR		A1						
IRET			BF	*	*	*	*	*	*
FLAGS←@SP;									
SP←SP + 1									
PC←@SP;									
SP←SP + 2;									
IMR(7)←1									
JP cc, dst	DA		cD	-	-	-	-	-	-
if cc is true,			c = 0 - F						
PC←dst	IRR		30						
JR cc, dst	RA		cB	-	-	-	-	-	-
if cc is true,			c = 0 - F						
PC←PC + dst									
Range: +127, -128									
LD dst, src	r	Im	rC	-	-	-	-	-	-
dst←src	r	R	r8						
	R	r	r9						
			r = 0 - F						
	r	X	C7						
	X	r	D7						
	r	Ir	E3						
	Ir	r	F3						
	R	R	E4						
	R	IR	E5						
	R	IM	E6						
	IR	IM	E7						
	IR	R	F5						
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
dst←src									
LDCI dst, src	Ir	Irr	C3	-	-	-	-	-	-
dst←src									
r←r + 1;rr←rr + 1									
NOP			FF	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -
POP dst dst←@SP; SP←SP+1	R IR	50 51	- - - - - -
PUSH src SP←SP-1; @SP←src	R IR	70 71	- - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP+2		AF	- - - - - -
RL dst 	R IR	90 91	* * * * - -
RLC dst 	R IR	10 11	* * * * - -
RR dst 	R IR	E0 E1	* * * * - -
RRC dst 	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst–src–C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst 	R IR	D0 D1	* * * 0 - -
SRP dst RP←src	Im	31	- - - - - -
STOP		6F	1 - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
SUB dst, src dst←dst - src	†	2[ ]	* * * * 1 *
SWAP dst 	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
WDT		5F	- X X X - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

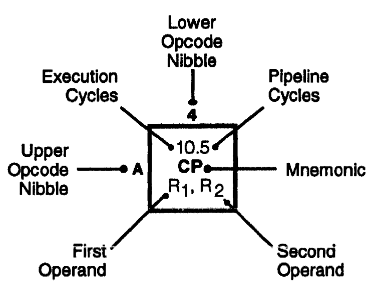
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) across; Upper Nibble (Hex) down

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



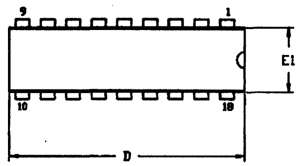
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_1 = Dst address
R_2 or r_2 = Src address

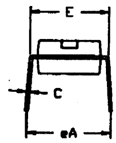
Sequence:
Opcode, First Operand, Second Operand

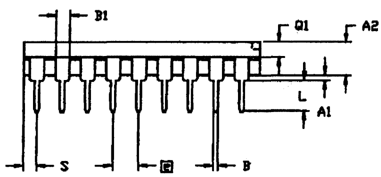
Note: The blank areas are reserved.

* 2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION



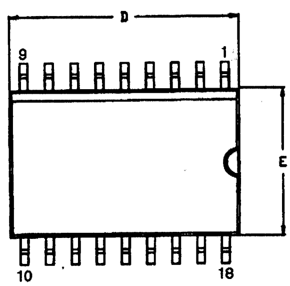


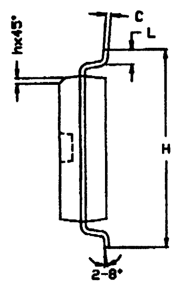


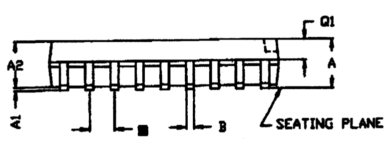
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
■	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram







CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
■	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C03 (8 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	**18-Pin SOIC**	**18-Pin DIP**	**18-Pin SOIC**
Z86C0308PSC	Z86C0308SSC	Z86C0308PEC	Z86C0308SEC

Z86C06 (12 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	**18-Pin SOIC**	**18-Pin DIP**	**18-Pin SOIC**
Z86C0612PSC	Z86C0612SSC	Z86C0612PEC	Z86C0612SEC

For fast results, contact your local Zilog sale offices for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
S = Plastic SOIC

Preferred Temperature
S = 0°C to +70°C

Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86C03 08 P S C is a Z86C03, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 08 — Speed
- 86C03 — Product Number
- Z — Zilog Prefix

Z86C03/C06 CMOS Z8® 8-Bit CCP™
Consumer Controller Processors 1

**Z86E03/E06 CMOS Z8® 8-Bit OTP CCP™
Consumer Controller Processors** 2

Z86C04/C08 CMOS Z8® Low Cost
1K /2K ROM Microcontrollers 3

Z86E04/E08 CMOS Z8®
8-Bit OTP Microcontrollers 4

Z86C07 CMOS Z8®
8-Bit Microcontroller 5

Z86E07 CMOS Z8®
8-Bit OTP Microcontroller 6

Z86C30/C31 CMOS Z8® 8-Bit CCP™
Consumer Controller Processors 7

Z86E03/E06

CMOS Z8® 8-BIT OTP CCP™ CONSUMER CONTROLLER PROCESSORS

FEATURES

- The Z86E03/E06 Devices Have the Following General Characteristics:

Part	ROM	RAM	Speed
Z86E03	512 bytes	60	8 MHz
Z86E06	1 Kbyte	124	12 MHz

- 18-Pin Package (DIP, SOIC)
- 3.0 to 5.5 Volt Operating Range
- Operating Temperature: –40°C to +105°C
- Clock Speeds up to 8 MHz (E03) and 12 MHz (E06)
- Fast Instruction Pointer: 1.5 µs @ 8 MHz (E03); 1.0 µs @ 12 MHz (E06)
- Multiple Expanded Register File Control Registers and Two SPI Registers (Z86E06 only)
- One/Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Permanent Watch-Dog Timer Option
- Power-On Reset Timer
- Programmable Auto Latches
- Two Standby Modes: STOP and HALT
- Two Comparators with Programmable Interrupt Polarity
- 14 Input/Output Lines (Two with Comparator Inputs)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.
- Serial Peripheral Interface (SPI) (Z86E06 Only)
- Software Programmable Low EMI Mode
- EPROM Protect Option

GENERAL DESCRIPTION

Zilog's Z86E03/E06 OTP (One-Time Programmable) CCP™ (Consumer Controller Processors) are members of the Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/ EMI options. These enhancements result in a more efficient, cost effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 512 and 1K bytes of EPROM and 60 and 124 bytes of general-purpose RAM, respectively. These low cost, low power consumption 18-pin CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86E03/E06 architecture is characterized by Zilog's 8-bit microcontroller core with the addition of an Expanded Register File to allow easy access to register mapped peripheral and I/O circuits. The Z86E03/E06 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, and industrial applications.

For applications demanding powerful I/O capabilities, the Z86E03/E06 provides 14 pins dedicated to input and output. These lines are grouped into two ports and are configurable under software control to provide timing, status signals, or parallel I/O.

GENERAL DESCRIPTION (Continued)

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File (Figure 1). The Register File is composed of 60/124 bytes of General-Purpose Registers, two I/O Port registers, and thirteen/fifteen Control and Status registers. The Expanded Register File consists of three control registers in the Z86E03, and four control registers, a SPI Receive Buffer, and a SPI compare register in the Z86E06.

With powerful peripheral features such as on-board comparators, counter/timer(s), Watch-Dog Timer (WDT), and serial peripheral interface (E06 only), the Z86E03/E06 meets the needs of a variety of sophisticated controller applications.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

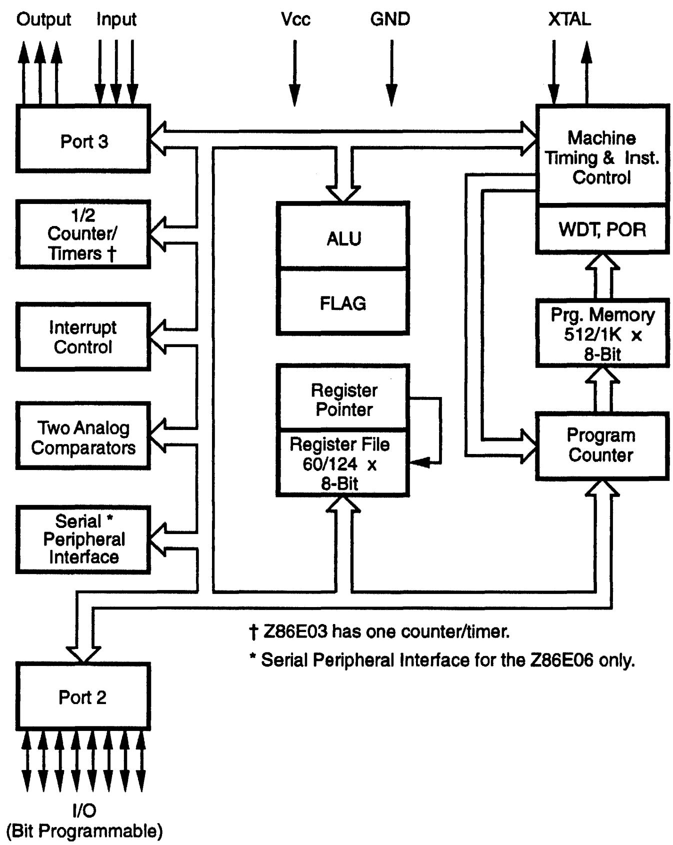


Figure 1. Z86E03/E06 Functional Block Diagram

PIN DESCRIPTION

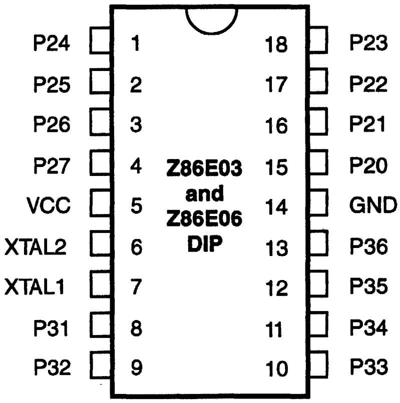


Figure 2. 18-Pin DIP Pin Configuration

Table 1. 18-Pin DIP and SOIC Pin Identification

No	Symbol	Function	Direction
1-4	P24-27	Port 2, pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-33	Port 3, pins 1, 2, 3	Fixed Input
11-13	P34-36	Port 3, pins 4, 5, 6	Fixed Output
14	GND	Ground	
15-18	P20-23	Port 2, pins 0, 1, 2, 3	In/Output

2

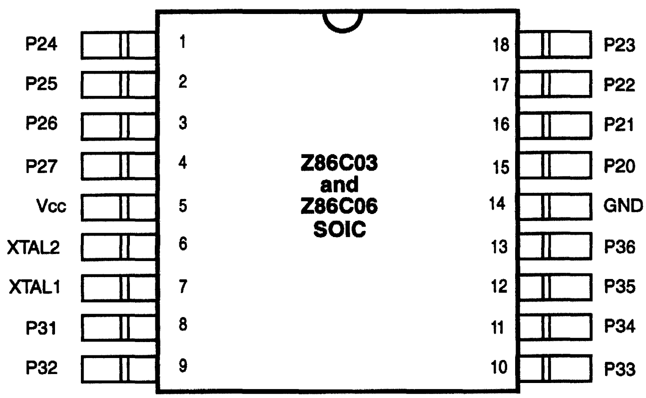


Figure 3. 18-Pin SOIC Pin Configuration

PIN FUNCTIONS

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered and contain Auto Latches. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 4a., 4b., and 4c.). Low EMI output buffers can be globally programmed by the software. In addition, when the SPI is enabled, P20 functions as data-in (DI), and P27 functions as data-out (DO) for the SPI (SPI on the Z86E06 only).

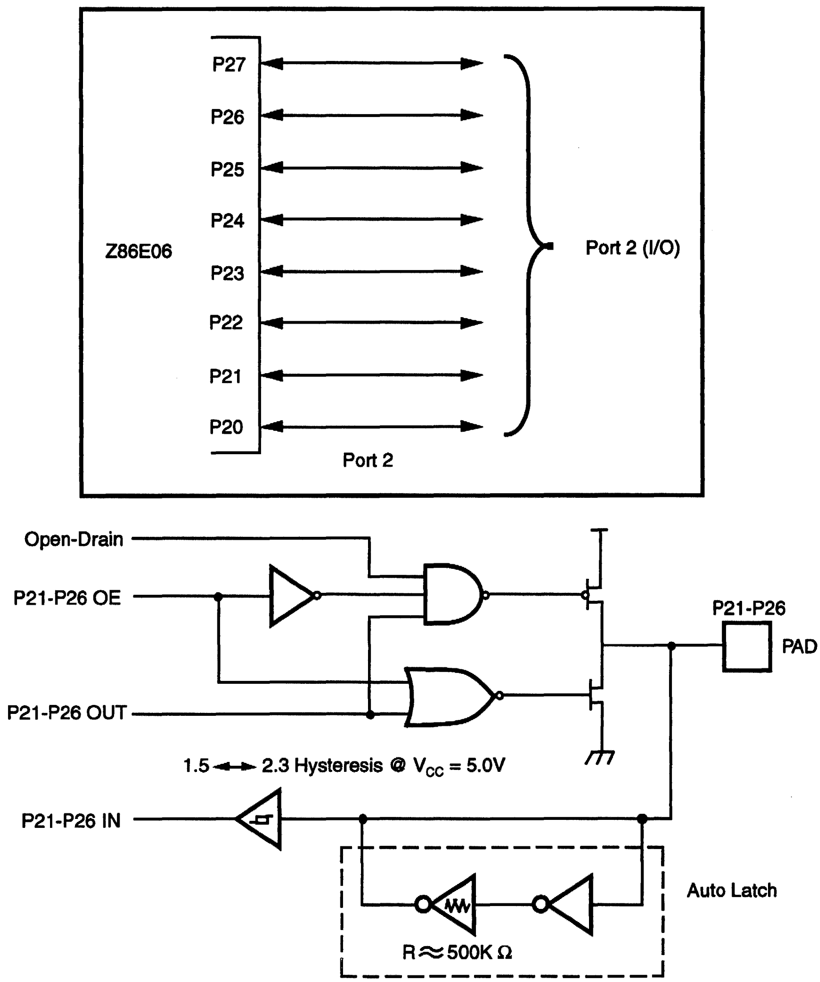


Figure 4a. Port 2 Configuration (Z86E06)

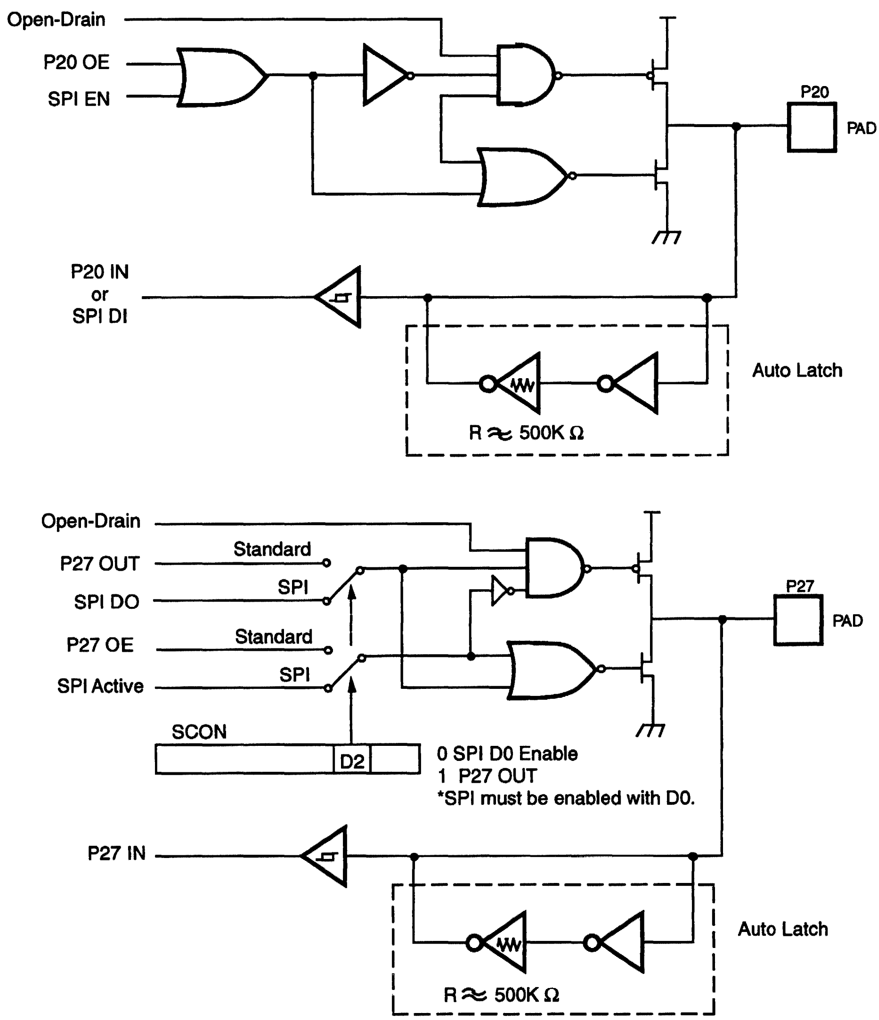


Figure 4b. Port 2 Configuration (Z86E06)

PIN FUNCTIONS (Continued)

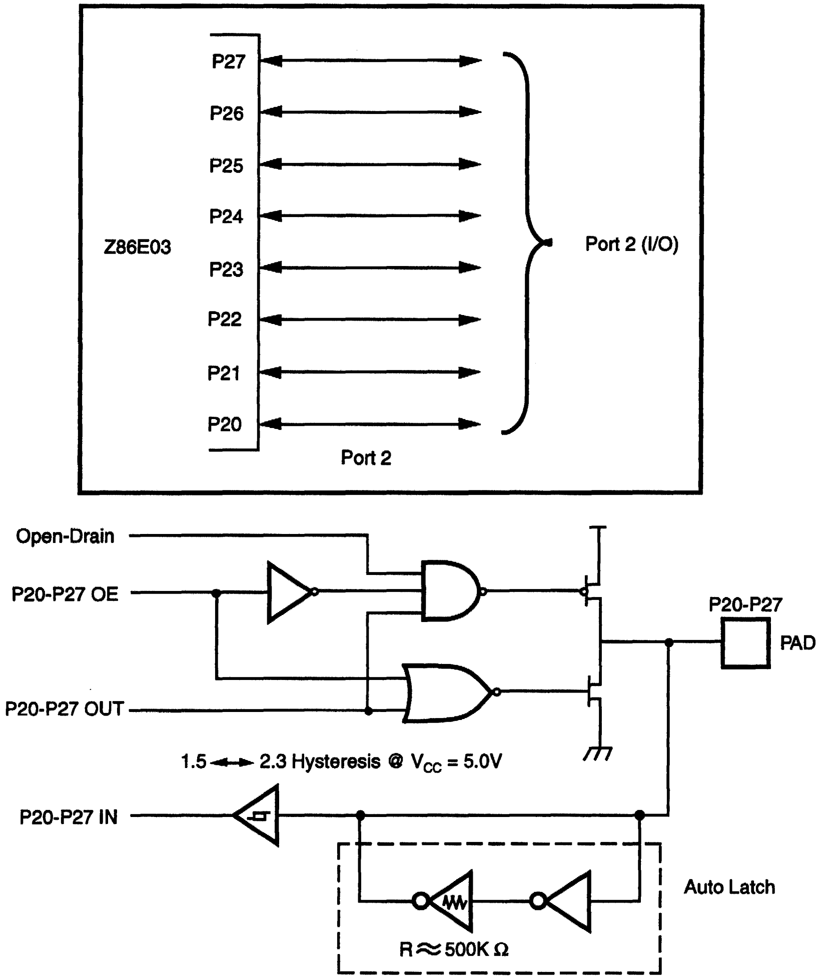


Figure 4c. Port 2 Configuration (Z86E03)

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Port 3 (P36-P31). Port 3 is a 6-bit, CMOS compatible port. These six lines consist of three fixed inputs (P31-P33) and three fixed outputs (P34-P36). Pins P31, P32, and P33 are standard CMOS inputs (no auto latches) and pins P34, P35, and P36 are push-pull outputs. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M-bit D1). Pins P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input when the analog mode is selected. P33 is a falling edge interrupt input only.

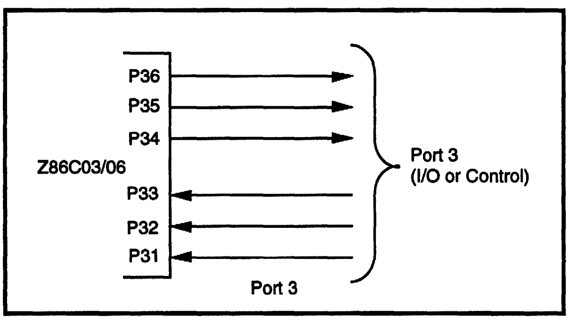
Note: P33 is available as an interrupt input only in the digital mode. P31 and P32 are valid interrupt inputs and P31 is the T_{IN} input when the analog or digital input mode is selected.

The outputs from the analog comparator can be globally programmed to output from P34 and P35 by setting PCON (F) 00 bit D0 = 1.

Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}).

In the Z86E06, pin P34 can also be configured as SPI clock (SK), input and output, and pin P35 can be configured as Slave Select (SS) in slave mode only, when the SPI is enabled (Figures 5a and 5b).

2



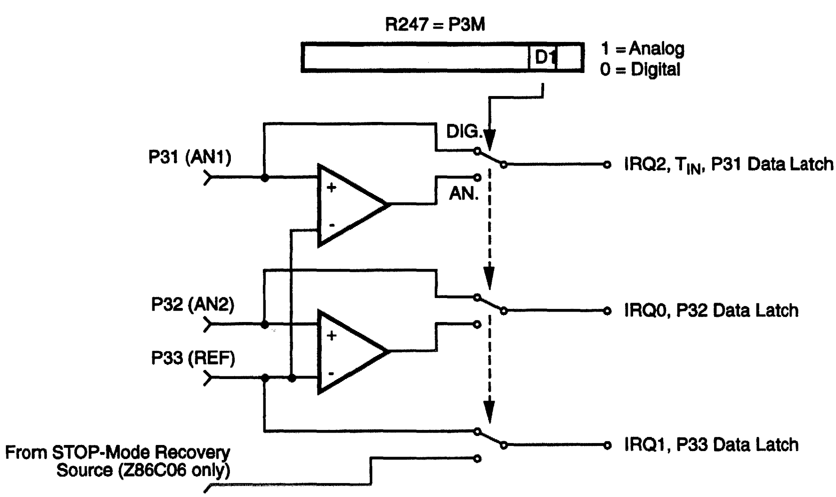


Figure 5a. Port 3 Configuration

PIN FUNCTIONS (Continued)

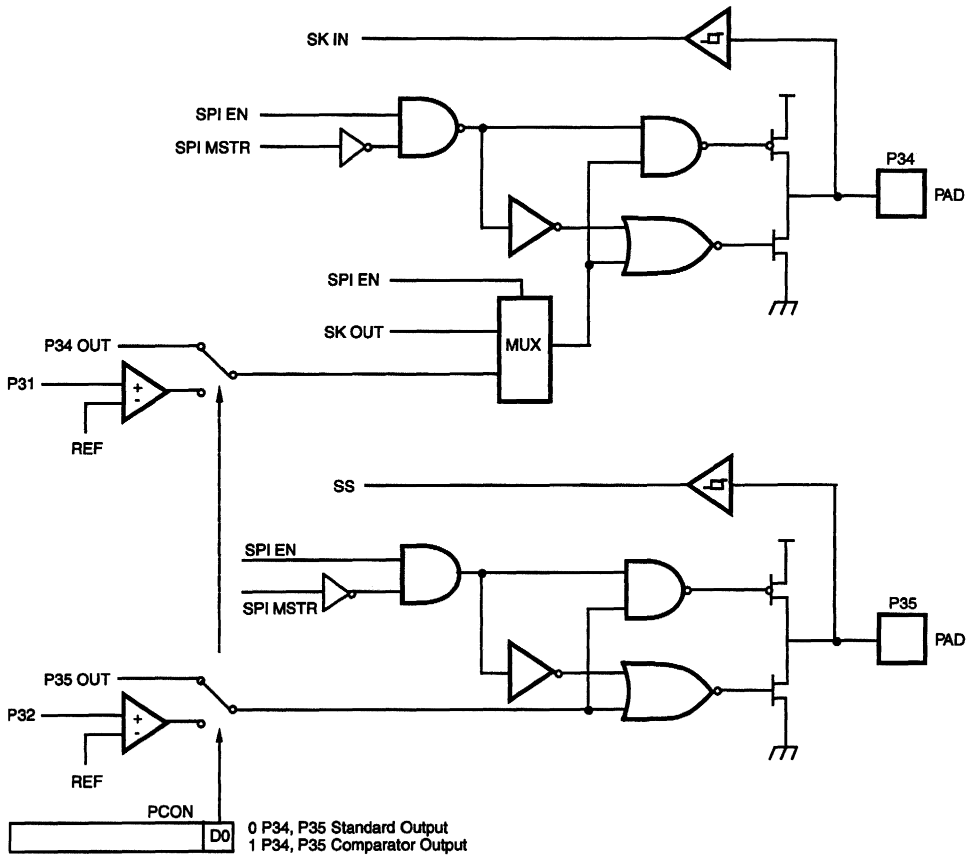


Figure 5b. Port 3 Configuration (Z86E06)

Low EMI Emission. The Z86E03/E06 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns (typical).
- Low EMI output drivers resistance of 200 ohms (typical).
- Low EMI oscillator.
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz (250 ns cycle time) when the low EMI oscillator is selected and SCLK = External (SMR Register Bit D1=1).

Comparator Inputs. Port 3 Pin P31 and P32 each have a comparator front end. The comparator reference voltage pin P33 is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In digital mode, Pin P33 can be used as a P33 register input or IRQ1 source.

FUNCTIONAL DESCRIPTION

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- STOP-Mode Recovery Source
- Low Voltage Protection

Having the Auto Power-On Reset circuitry built-in, the Z86E03/E06 does not require an external reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles.

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a STOP-Mode Recovery operation.

Program Memory. Z86E03/E06 can address up to 512/1K bytes of internal program memory (Figure 6). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 511/1023 consists of on-chip, user program mask ROM.

EPROM Protect. The 512/1K bytes of Program Memory is mask programmable. A EPROM protect feature will prevent "dumping" of the EPROM contents by inhibiting execution of the LDC and LDCI instructions to program memory in all modes.

EPROM protect is EPROM-programmable. It is selected by the customer when the ROM code is submitted. **Selecting ROM protect disables the LDC and LDCI instructions in all modes. ROM lookup tables are not supported in this mode.**

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 7). These register groups are known as the Expanded Register File (ERF).

Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of the RP register select the working register group (Figure 7). For the Z86E03, three system configuration registers reside in the ERF address space Bank F. For the Z86E06, three system configuration registers reside in the ERF address space Bank F, while three SPI registers reside in Bank C. The rest of the ERF address space is not physically implemented and is open for future expansion.

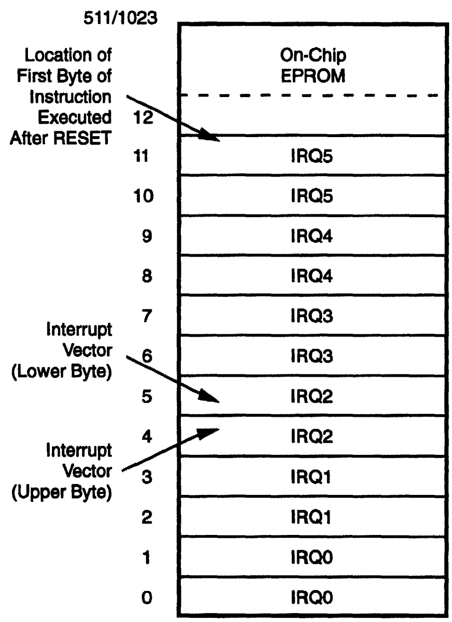
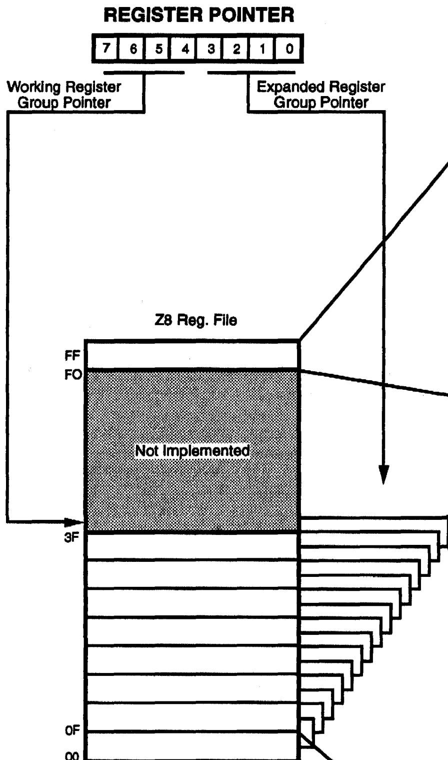


Figure 6. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)



Z8 STANDARD CONTROL REGISTERS

	REGISTER		RESET CONDITION D7	D6	D5	D4	D3	D2	D1	D0
	FF	SPL	U	U	U	U	U	U	U	U
	FE	GPR	U	U	U	U	U	U	U	U
	FD	RP	0	0	0	0	0	0	0	0
	FC	FLAGS	U	U	U	U	U	U	U	U
	FB	IMR	0	U	U	U	U	U	U	U
	FA	IRQ	0	0	0	0	0	0	0	0
	F9	IPR	U	U	U	U	U	U	U	U
	F8	P01M	U	U	U	0	U	U	U	U
*	F7	P3M	U	U	U	U	U	U	0	0
*	F6	P2M	1	1	1	1	1	1	1	1
	F5	Reserved								
	F4	Reserved								
	F3	PRE1	U	U	U	U	U	U	0	0
	F2	T1	U	U	U	U	U	U	U	U
	F1	TMR	0	0	0	0	0	0	0	0
	F0	Reserved								

EXPANDED REG. GROUP (F)

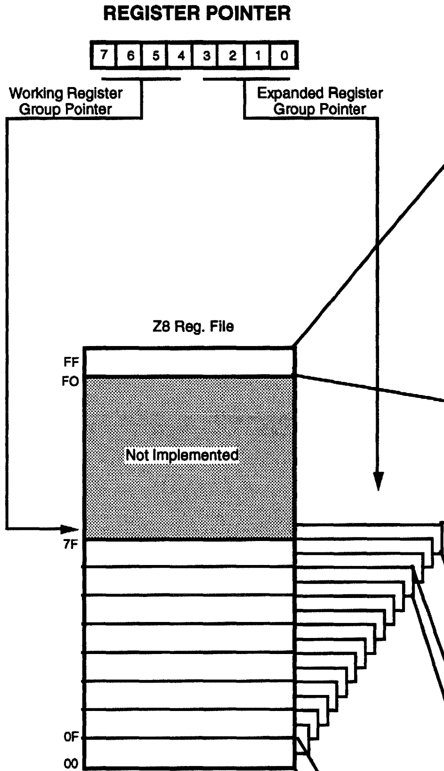
	REGISTER		RESET CONDITION D7	D6	D5	D4	D3	D2	D1	D0
*	(F) 0F	WDTMR	U	U	U	0	1	1	0	1
	(F) 0E	Reserved								
	(F) 0D	Reserved								
	(F) 0C	Reserved								
*	(F) 0B	SMR	0	0	1	0	0	0	0	†
	(F) 0A	Reserved								
	(F) 09	Reserved								
	(F) 08	Reserved								
	(F) 07	Reserved								
	(F) 06	Reserved								
	(F) 05	Reserved								
	(F) 04	Reserved								
	(F) 03	Reserved								
	(F) 02	Reserved								
	(F) 01	Reserved								
	(F) 00	PCON	1	1	1	U	U	U	U	0

EXPANDED REG. GROUP (0)

REGISTER		RESET CONDITION D7	D6	D5	D4	D3	D2	D1	D0
(0) 03	P3	†	1	1	1	U	U	U	†
(0) 02	P2	U	U	U	U	U	U	U	U
(0) 01	Reserved	U	U	U	U	U	U	U	U
(0) 00	Reserved	U	U	U	U	U	U	U	U

Notes:
General-purpose registers are undefined after power-up, and they are not changed after reset.
* Will not be reset with a STOP-Mode Recovery.
U = Unknown
† = Reserved

Figure 7a. Expanded Register File Architecture (Z86E03)



Z8 STANDARD CONTROL REGISTERS

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
	FF	SPL	U	U	U	U	U	U	U	U
	FE	GPR	U	U	U	U	U	U	U	U
	FD	RP	0	0	0	0	0	0	0	0
	FC	FLAGS	U	U	U	U	U	U	U	U
	FB	IMR	0	U	U	U	U	U	U	U
	FA	IRQ	0	0	0	0	0	0	0	0
	F9	IPR	U	U	U	U	U	U	U	U
	F8	P01M	U	U	U	0	U	U	U	U
*	F7	P3M	U	U	U	U	U	U	0	0
*	F6	P2M	1	1	1	1	1	1	1	1
	F5	PRE0	U	U	U	U	U	U	U	0
	F4	T0	U	U	U	U	U	U	U	U
	F3	PRE1	U	U	U	U	U	U	0	0
	F2	T1	U	U	U	U	U	U	U	U
	F1	TMR	0	0	0	0	0	0	0	0
	F0	Reserved								

EXPANDED REG. GROUP (F)

	REGISTER		RESET CONDITION							
*	(F) 0F	WDTMR	U	U	U	0	1	1	0	1
	(F) 0E	Reserved								
	(F) 0D	Reserved								
	(F) 0C	Reserved								
**	(F) 0B	SMR	0	0	1	0	0	0	0	0
	(F) 0A	Reserved								
	(F) 09	Reserved								
	(F) 08	Reserved								
	(F) 07	Reserved								
	(F) 06	Reserved								
	(F) 05	Reserved								
	(F) 04	Reserved								
	(F) 03	Reserved								
	(F) 02	Reserved								
	(F) 01	Reserved								
	(F) 00	PCON	1	1	1	U	U	U	U	0

EXPANDED REG. GROUP (C)

REGISTER		RESET CONDITION							
(C) 02	SCON	U	U	U	U	0	0	0	0
(C) 01	RxBUF	U	U	U	U	U	U	U	U
(C) 00	SCOMP	0	0	0	0	0	0	0	0

EXPANDED REG. GROUP (0)

REGISTER		RESET CONDITION							
(0) 03	P3	†	1	1	1	U	U	U	†
(0) 02	P2	U	U	U	U	U	U	U	U
(0) 01	Reserved	U	U	U	U	U	U	U	U
(0) 00	Reserved	U	U	U	U	U	U	U	U

Notes:
General-purpose registers are undefined after power-up, and they are not changed after reset.
* Will not be reset with a STOP-Mode Recovery
** Will not be reset with a STOP-Mode Recovery, except Bit D0.
U = Unknown
† = Reserved

Figure 7b. Expanded Register File Architecture (Z86E06)

FUNCTIONAL DESCRIPTION (Continued)

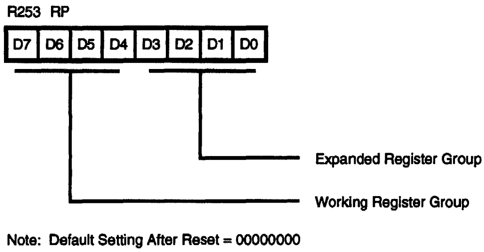


Figure 8. Register Pointer Register

Register File. The Register File consists of two I/O port registers, 60/124 general-purpose registers, and 13/15 control and status registers. The Z86E03 General-Purpose Register file ranges from address 00 to 3F while the Z86E06 General-Purpose Register file ranges from address 00 to 7F (see Figure 9). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 9). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

Stack. An 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60/124 general-purpose registers.

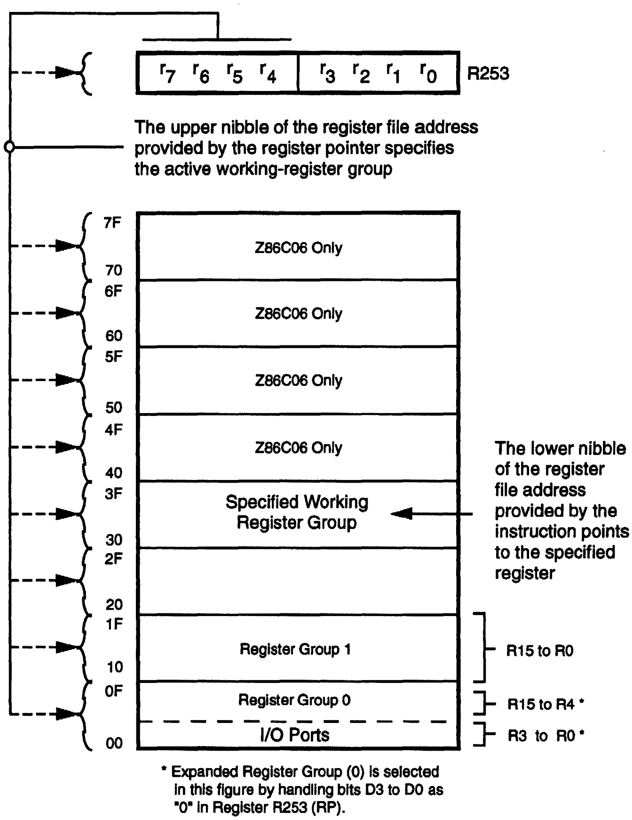


Figure 9. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler (Z86E03 only has T1). The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 10).

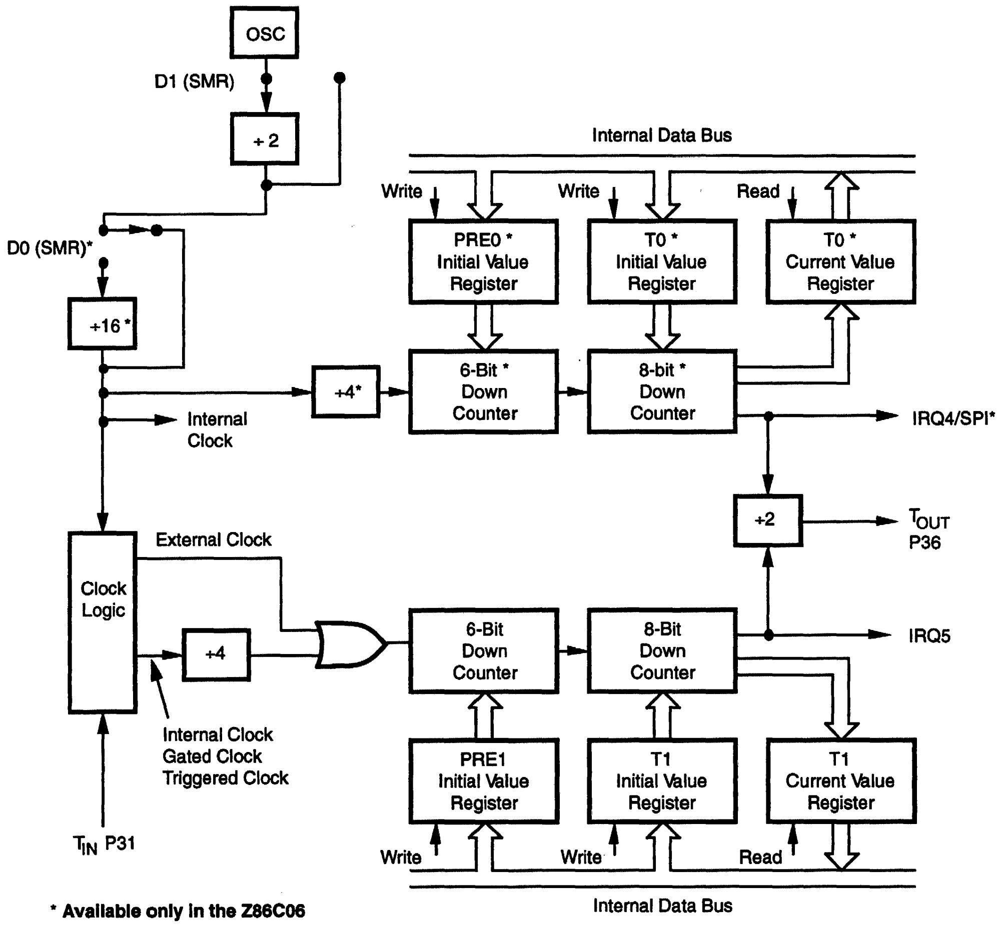


Figure 10. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, RQ4 (T0) or IRQ5 (T1), is generated. Note that IRQ4 is software-generated in the Z86E03.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 serves as a timer output (T_{OUT}) through which T0 (E06 only), T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1 (E06 only). The T_{IN} mode is enabled by setting PRE1 bit D1 (R243) to 0.

Interrupts. The Z86E03/E06 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 11). The six sources are divided as follows; three sources are claimed by Port 3 lines P31-P33, two sources in the counter/timers, and one source for the SPI. The Interrupt Mask Register globally or singularly enables or disables the six interrupt requests (Table 2).

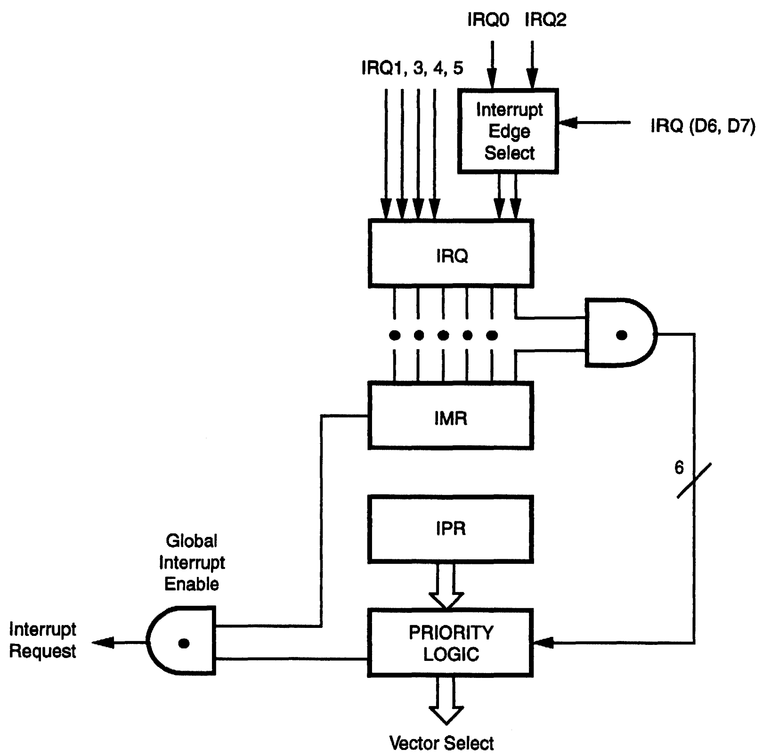


Figure 11. Interrupt Block Diagram

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	IRQ 0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ 1	IRQ 1	2, 3	External (P33), Falling Edge Triggered
IRQ 2	IRQ 2, T_{IN}	4,5	External (P31), Rising/Falling Edge Triggered
IRQ 3	IRQ 3	6, 7	Software Generated, SPI Receive
IRQ 4	T0/IRQ 4	8, 9	Internal for E06 and Software Generated for E03
IRQ 5	TI	10, 11	Internal

Note:
When enabled, the SPI receive interrupt is mapped to IRQ3 in the Z86E06.

2

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E03/E06 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service. In the Z86E06, when the SPI is disabled, IRQ3 has no hardware source but can be invoked by software (write to IRQ3 Register). When the SPI is enabled, an interrupt will be mapped to IRQ3 after a byte of data has been received by the SPI Shift Register.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

The programming bits for the INTERRUPT EDGE SELECT are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

Table 3. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

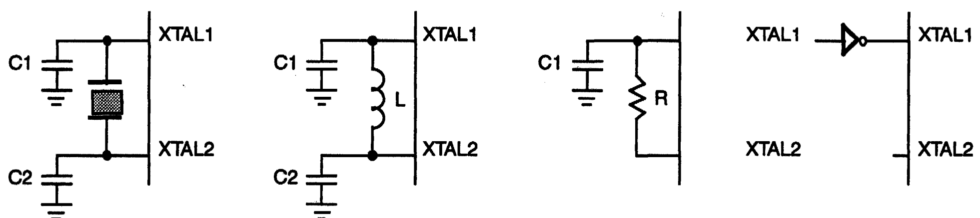
FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86E03/E06 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 8 MHz/12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values (capacitance between 10 pF to 300 pF) from each pin directly to the device ground (pin 14). The layout is important to reduce ground noise injection.

The RC oscillator option is EPROM-programmable, to be selected by the customer at the time the Z8 is EPROM programmed. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 12).

In addition, a special feature has been incorporated into the Z86E03/E06; in low EMI noise mode (bit 7 of PCON register=0) with the RC option selected, the oscillator is targeted to consume considerately less I_{CC} current at frequencies of 10 kHz or less.



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC
C1, C2 = 22 pF
L = 130 µH *
F = 3 MHz

RC
@ 5V Vcc (TYP)
C1 = 33pF*
R = 1kΩ*
F = 9.5 MHz

External Clock

* Preliminary Value Including Pin Parasitics

Figure 12. Oscillator Configuration

Power-On Reset. A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the three conditions:

- Power-Fail to Power-OK Status
- STOP-Mode Recovery (If D5 of SMR=1)
- WDT Time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after STOP mode recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. Will turn off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device may be recovered by interrupts either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP mode is terminated by a RESET only, either by WDT time-out, POR, SPI compare; or SMR recovery. This causes the processor to restart the application program at address 000C (HEX). Note, the crystal remains active in STOP mode if bits 3 and 4 of the WDTMR are enabled. In this mode, only the Watch-Dog Timer runs in STOP mode.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, i.e.:

```
FF   NOP   ; clear the pipeline
6F   STOP  ; enter STOP mode
or
FF   NOP   ; clear the pipeline
7F   HALT  ; enter HALT mode
```

Serial Peripheral Interface (SPI)—Z86E06 Only. The Z86E06 incorporates a serial peripheral interface for communication with other microcontrollers and peripherals. **The SPI does not exist on the Z86E03**. The SPI includes features such as STOP-Mode Recovery, Master/Slave selection, and Compare mode. Table 4 contains the pin configuration for the SPI feature when it is enabled. The SPI consists of four registers: SPI Control Register (SCON), SPI Compare Register (SCOMP), SPI Receive/Buffer Register (RxBUF), and SPI Shift Register. SCON is located in bank (C) of the Expanded Register Group at address 02.

Table 4. SPI Pin Configuration

Name	Function	Pin Location
DI	Data-In	P20
DO	Data-Out	P27
SS	Slave Select	P35
SK	SPI Clock	P34

The SPI Control Register (SCON) (Figure 13) is a read/write register that controls; Master/Slave selection, interrupts, clock source and phase selection, and error flag. Bit 0 enables/disables the SPI with the default being SPI disabled. A 1 in this location will enable the SPI, and a 0 will disable the SPI. Bits 1 and 2 of the SCON register in Master mode select the clock rate. The user may choose whether internal clock is divide-by-2, -4, -8, or -16. In slave mode, Bit 1 of this register flags the user if an overrun of the RxBUF Register has occurred. The RxCharOverrun flag is only reset by writing a 0 to this bit. In slave mode, bit 2 of the Control Register disables the data-out I/O function. If a 1 is written to this bit, the data-out pin is released to its original port configuration. If a 0 is written to this bit, the SPI shifts out one bit for each bit received. Bit 3 of the SCON Register enables the compare feature of the SPI, with the default being disabled. When the compare feature is enabled, a comparison of the value in the SCOMP Register is made with the value in the RxBUF Register. Bit 4 signals that a receive character is available in the RxBUF Register.

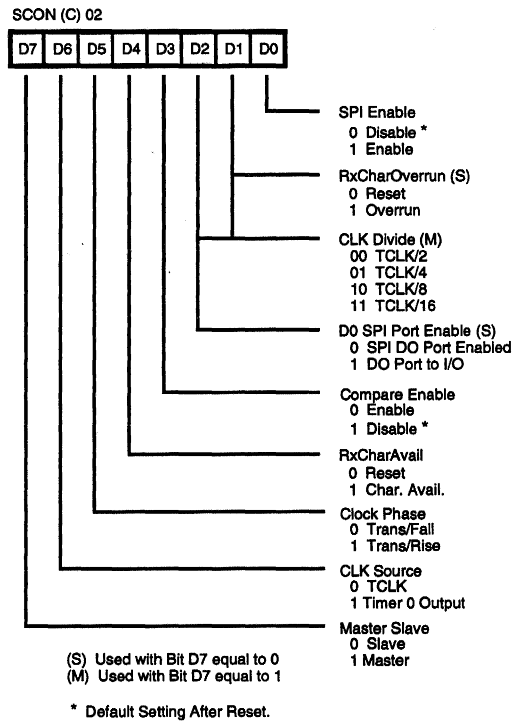


Figure 13. SPI Control Register (SCON) (Z86E06 Only)

If the associated IRQ3 is enabled, an interrupt is generated. Bit 5 controls the clock phase of the SPI. A 1 in Bit 5 allows for receiving data on the clock's falling edge and transmitting data on the clock's rising edge. A 0 allows receiving data on the clock's rising edge and transmitting on the clock's falling edge. The SPI clock source is defined in bit 6. A 1 uses Timer0 output for the SPI clock, and a 0 uses TCLK for clocking the SPI. Finally, bit 7 determines whether the SPI is used as a Master or a Slave. A 1 puts the SPI into Master mode and a 0 puts the SPI into Slave mode.

FUNCTIONAL DESCRIPTION (Continued)

SPI Operation (Z86E06 only). The SPI is used in one of two modes: either as system slave, or as system master. Several of the possible system configurations are shown in Figure 14. In the slave mode, data transfer starts when the slave select (SS) pin goes active. Data is transferred into the slave's SPI Shift Register through the DI pin, which has the same address as the RxBUF Register. After a byte of data has been received by the SPI Shift Register, a Receive Character Available (RCA/IRQ3) flag and interrupt is generated. The next byte of data will be received at this time. The RxBUF Register must be cleared, or a Receive Character Overrun (RxCharOverrun) flag will be set in the SCON Register, and the data in the RxBUF Register will be overwritten. When the communication between the master and slave is complete, the SS goes inactive.

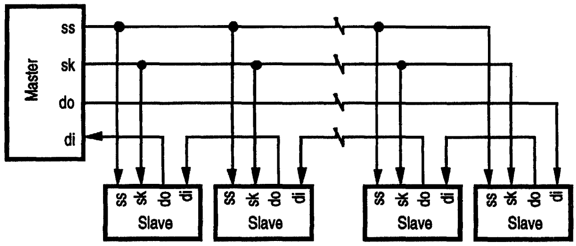
Unless disconnected, for every bit that is transferred into the slave through the DI pin, a bit is transferred out through the DO pin on the opposite clock edge. During slave operation, the SPI clock pin (SK) is an input. In master mode, the CPU must first activate a SS through one of it's I/O ports. Next, data is transferred through the master's DO pin one bit per master clock cycle. Loading data into the shift register initiates the transfer. In master mode, the master's clock will drive the slave's clock. At the conclusion of a transfer, a Receive Character Available (RCA/IRQ3) flag and interrupt is generated. Before data is transferred via the DO pin, the SPI Enable bit in the SCON Register must be enabled.

SPI Compare (Z86E06 only). When the SPI Compare Enable bit, D3 of the SCON Register is set to 1, the SPI Compare feature is enabled. The compare feature is only valid for slave mode. A compare transaction begins when the (SS) line goes active. Data is received as if it were a normal transaction, but there is no data transmitted to avoid bus contention with other slave devices. When the compare byte is received, IRQ3 is not generated. Instead, the data is compared with the contents of the SCOMP Register. If the data does not match, DO remains inactive and the slave ignores all data until the (SS) signal is reset. If the data received matches the data in the SCOMP register, then a SMR signal is generated. DO is activated if it is not tri-stated by D2 in the SCON Register, and data is received the same as any other SPI slave transaction.

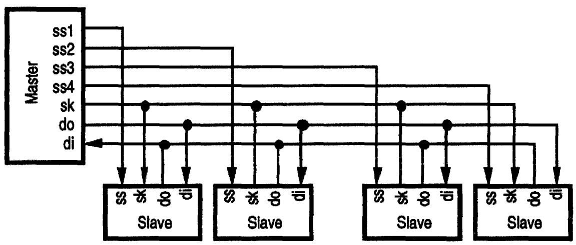
When the SPI is activated as a slave, it operates in all system modes; STOP, HALT, and RUN. Slaves' not comparing remain in their current mode, whereas slaves' comparing wake from a STOP or HALT mode by means of an SMR.

SPI Clock (Z86E06 only). The SPI clock maybe driven by three sources: Timer0, a division of the internal system clock, or the external master when in slave mode. Bit D6 of the SCON Register controls what source drives the SPI clock. A 0 in bit D6 of the SCON Register determines the division of the internal system clock if this is used as the SPI clock source. Divide by 2, 4, 8, or 16 is chosen as the scaler.

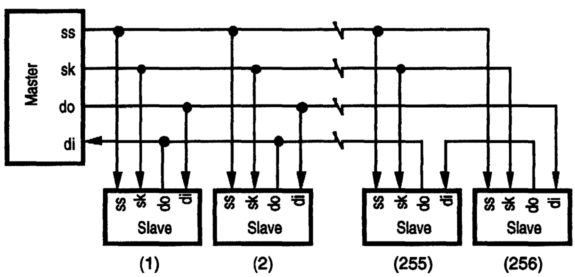
Standard Serial Setup



Standard Parallel Setup

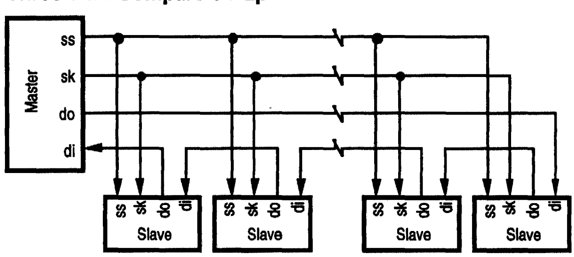


Setup For Compare



Up to 256 slaves per SS line

Three Wire Compare Setup



Multiple slaves may have the same address.

Figure 14. SPI System Configuration (Z86E06 Only)

FUNCTIONAL DESCRIPTION (Continued)

Receive Character Available and Overrun (Z86E06 Only). When a complete data stream is received, an interrupt is generated and the RxCharAvail bit in the SCON Register is set. Bit 4 in the SCON Register is for enabling or disabling the RxCharAvail interrupt. The RxCharAvail bit is available for interrupt polling purposes and is reset when the RxBUF Register is read. RxCharAvail is generated in both master and slave modes. While in slave mode, if the RxBUF is not read before the next data stream is received and loaded into the RxBUF Register, Receive Character Overrun (RxCharOverrun) occurs. Since there is no need for clock control in slave mode, bit D1 in the SPI Control Register is used to log any RxCharOverrun (Figure 15 and Figure 16).

No	Parameter	Min	Units
1	DI to SK Setup	10	ns
2	SK to D0 Valid	15	ns
3	SS to SK Setup	.5 Tsk	ns
4	SS to D0 Valid	15	ns
5	SK to DI Hold Time	10	ns

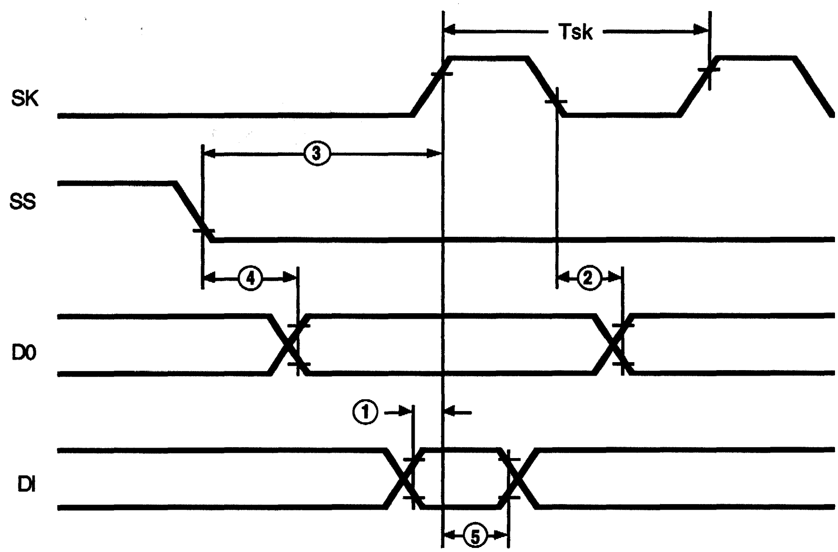


Figure 15. SPI Timing (Z86E06 Only)

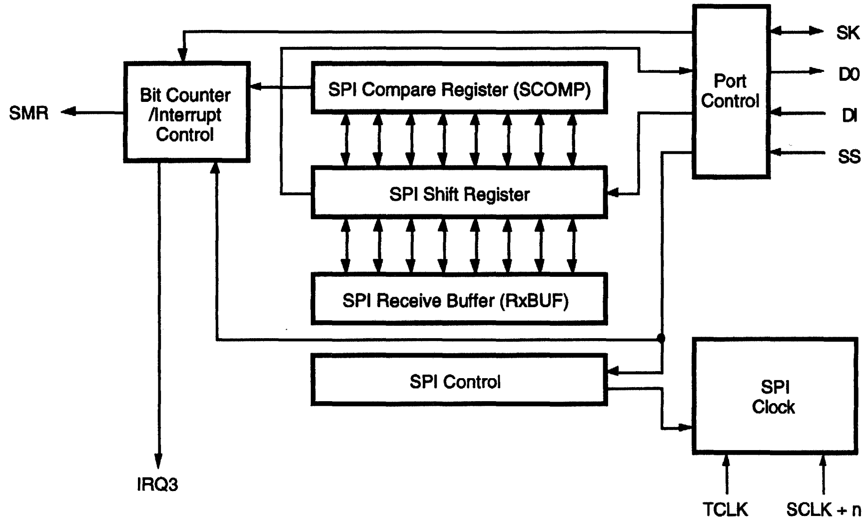


Figure 16. SPI Logic (Z86E06 Only)

PORT Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 17).

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34, and P35 and a 0 releases the Port to its standard I/O configuration.

Bits D4-D1. These bits are reserved and must be 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting D5=1. The default value is 1.

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting D6=1. The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive, it does not affect the relationship of SCLK and XTAL.

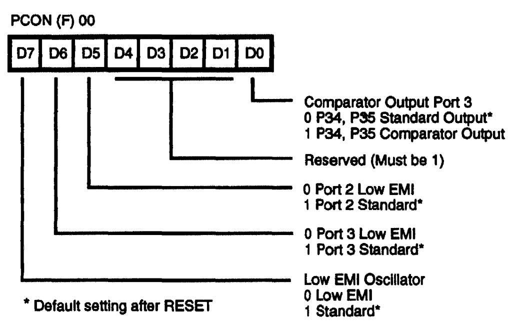


Figure 17. Port Configuration Register (PCON) (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP-Mode Recovery (Figure 18). All bits are Write Only except bit 7, which is Read Only. Bit 7 is a flag bit that is hardware set on the condition of a STOP recovery and reset on a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. The recovery level must be active Low to work with SPI. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR specify the source of the STOP-Mode Recovery signal. Bit 1 determines whether the XTAL is divided by 1 or 2. A 0 in this location uses XTAL divide-by-two, and a 1 uses XTAL. The default for this bit is XTAL divide-by-two. Bit 0 controls the divide-by-16 prescaler of SCLK/TCLK. The SMR is located in bank F of the Expanded Register Group at address 0BH.

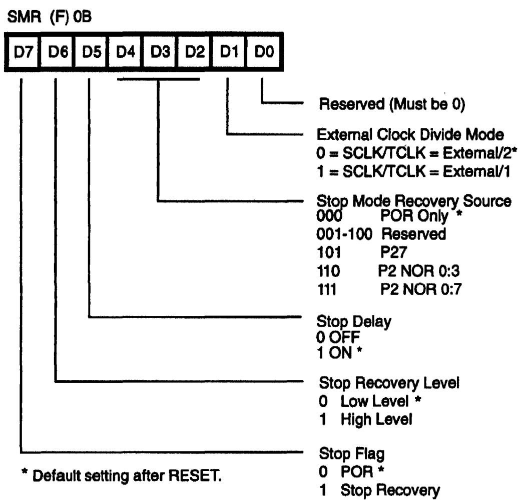


Figure 18a. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only.) (Z86E03)

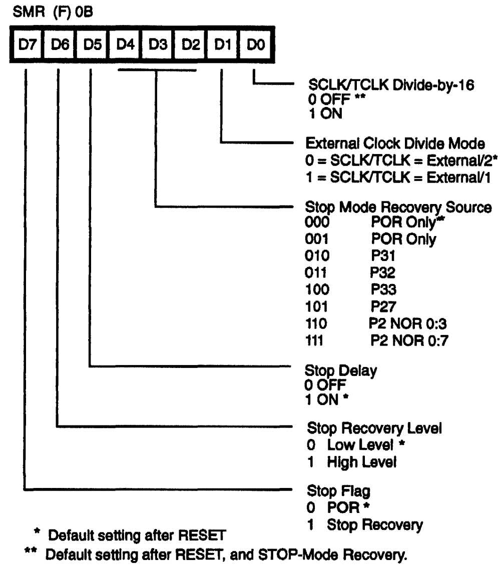


Figure 18b. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only.) (Z86E06)

SCLK/TCLK Divide-by-16 Select (D0)—Z86E06 Only. D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources the counter/timers and interrupt logic).

External Clock Divide Mode (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit, together with D7 of PCON, helps further lower EMI [i.e., D7 (PCON)=0, D1 (SMR=1]. The default setting is 0.

STOP-Mode Recovery Source (D2,D3,D4). These three bits of the SMR specify the wake-up source of the STOP-Mode Recovery (Figure 19 and Table 5).

Table 5. STOP-Mode Recovery Source

SMR D4	D3	D2	Operation Description of Action
0	0	0	POR recovery only
0	0	1	POR recovery only (E03 = Reserved)
0	1	0	P31 transition (E03 = Reserved)
0	1	1	P32 transition (E03 = Reserved)
1	0	0	P33 transition (E03 = Reserved)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0:3
1	1	1	Logical NOR of Port 2 bits 0:7

P31-P33 cannot wake up from STOP Mode if the input lines are configured as analog inputs. In the Z86E06, when the SPI is enabled and the Compare feature is active, a SMR is generated upon a comparison in the SPI Shift Register and SCOMP Register, regardless of the above SMR Register settings. If SPI Compare is used to wake up the part from STOP Mode, it is still possible to have one of the other STOP-Mode Recovery sources active. **Note:** These other STOP- Mode Recovery sources must be active level Low (bit D6 in SMR set to 0 if P31, P32, P33, and P27 selected, or bit D6 in SMR set to 1 if logical NOR of Port 2 is selected).

STOP-Mode Recovery Delay Select (D5). This bit disables the 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the "fast" wake up is selected, the STOP-Mode Recovery source needs to be kept active for at least 5 TpC.

STOP-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 19).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. It is active High, and is 0 (cold) on POR/WDT RESET. This bit is Read Only. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

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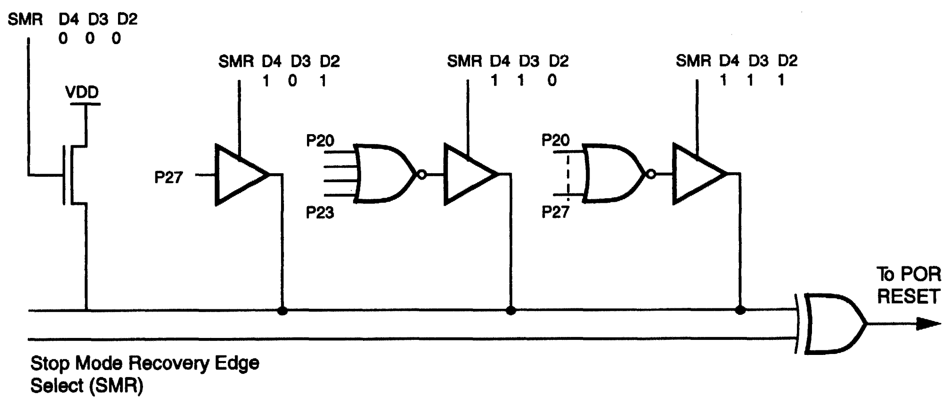
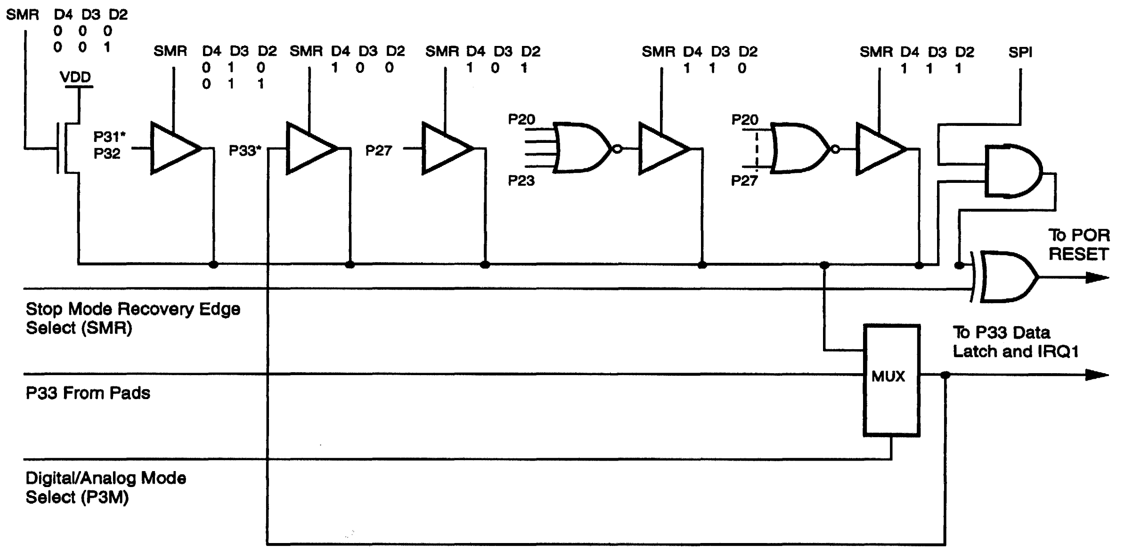


Figure 19a. STOP Mode Recovery Source (Z86E03)

FUNCTIONAL DESCRIPTION (Continued)



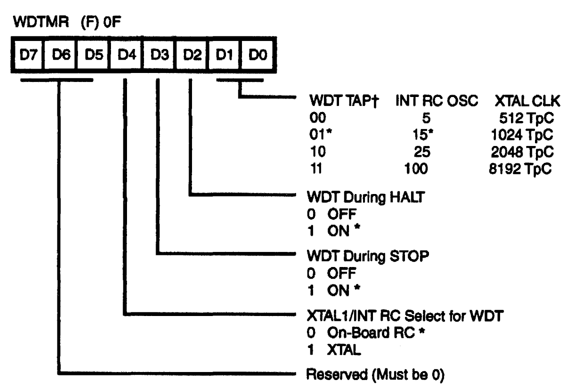
*Note: P31, P32 and P33 are not in Analog Mode.

Figure 19b. STOP-Mode Recovery Source (Z86E06)

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled after it has been initially enabled. The WDT circuit is driven by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDTMR register.

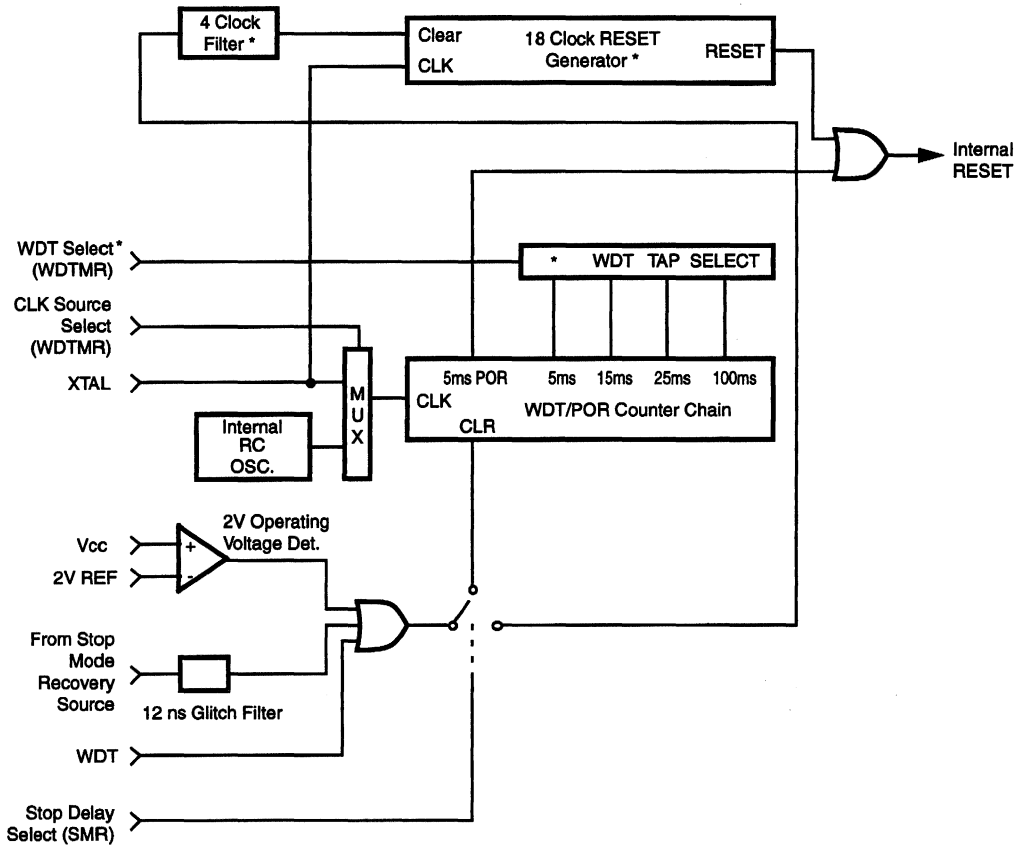
Note: Execution of the WDT instruction affects the Z (zero), S (sign), and V (overflow) flags.

Bits 0 and 1 control a tap circuit that determines the timeout period (on Z86E06 only). Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to 1, the WDT is only driven by the external clock during STOP mode. This feature makes it possible to wake up from STOP mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 20). ***This register is accessible only during the first 64 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Reset or a STOP Mode Recovery (Figure 21). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH.***



* Default setting after RESET
† Must be 01 for Z86E03

Figure 20. Watch-Dog Timer Mode Register (Write Only)



* Not available on the Z86E03, WDT fixed at 15 ms/1024TpC in the Z86E03.

Figure 21. Resets and WDT

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FUNCTIONAL DESCRIPTION (Continued)

WDT Time Select (D1,D0). Bits 0 and 1 control a tap circuit that determines the time-out period. Table 6 shows the different values that can be obtained. The default value of D0 and D1 are 1 and 0, respectively. These select bits are present in the Z86E06 only.

Table 6. Time-Out Period of the WDT (Z86E06 Only)

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256TpC
0	1	15 ms min	512TpC
1	0	25 ms min	1024TpC
1	1	100 ms min	4096TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 15 ms, D0 = 1 and D1 = 0.
The values given are for V_{CC} = 5.0V

For the Z86E03, the WDT time-out value is fixed at 1024 TpC (depending on WDTMR bit D4) period. When writing to the WDTMR in the Z86E03, bit D0 must be 1 and D1 must be 0.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1. If bits D3 and D4 are both set to 1, the WDT only, is driven by the external clock during STOP mode.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the internal RC oscillator.

Bits 5, 6 and 7. These bits are reserved.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the specified voltage (typically 2.6V).

Low Voltage Protection (V_{LV}). The Low Voltage Protection trip point (V_{LV}) will be less than 3 volts and above 1.8 volts under the following conditions.

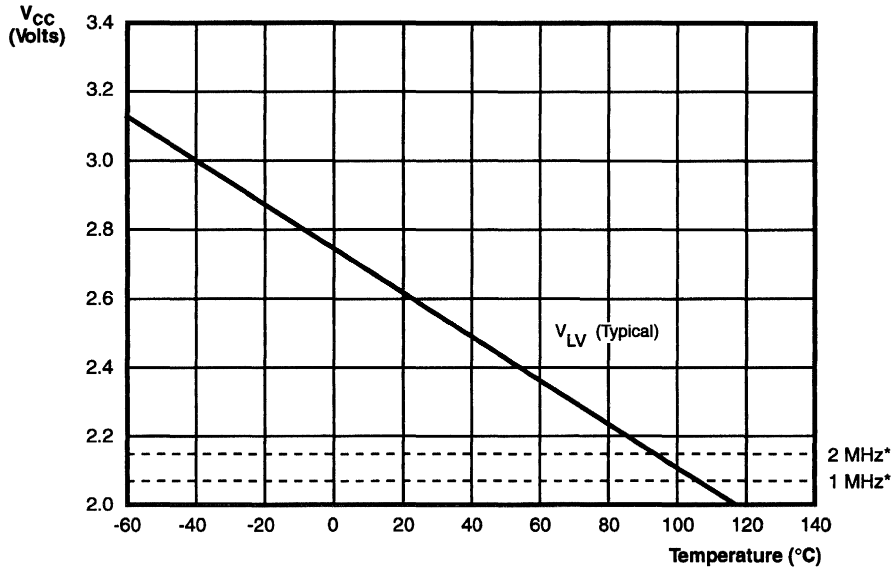
Maximum (V_{LV}) Conditions:

Case 1: T_A = –40° to +105°C, Internal Clock (SCLK) Frequency equal or less than 1 MHz

Case 2: T_A = –40° to +85°C, Internal Clock (SCLK) Frequency equal or less than 2 MHz

Note: The internal clock frequency (SCLK) is determined by SMR (F) 0BH bit D1.

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device is guaranteed to function normally until the Low Voltage Protection trip point (V_{LV}) is reached, for the temperatures and operating frequencies in cases 1 and 2 above. The actual low voltage trip point is a function of temperature and process parameters (Figure 22).



Note: * The typical minimum operating Vcc voltage at that frequency.

Figure 22. Typical Z86E03/E06 V_{LV} Voltage vs Temperature

SPECIAL FUNCTIONS
EPROM Mode

Besides V_{DD} and GND (V_{SS}), the Z86E03/E06 changes all its pin functions in the EPROM mode. XTAL2 has no function, XTAL1 functions as /CE, P31 functions as /OE, P32 functions as EPM, P33 functions as V_{PP}, and P02 functions as /PGM.

EPROM Protect. ROM protect is EPROM-programmable. It is selected by the customer at the time the ROM code is EPROM programmed. The selection of ROM Protect disables the LDC and LDCI instructions in all modes. A ROM look-up table cannot be used in this mode.

Application Caution

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM, /CE, /OE pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP mode. The V_{PP} requires both a diode and a 100 pF capacitor.

User Modes. Table 7 shows the programming voltage of each mode of Z86E06.

Table 7. OTP Programming Table

Programming Modes	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ1	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V
EPROM READ2	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V
PROGRAM	V_H	X	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.0V
PROGRAM VERIFY	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
EPROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
PERMANENT WDT ENABLED	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
GLOBAL AUTO LATCH DISABLED	V_H	V_{IH}	V_H	V_{IL}	V_{IL}	NU	NU	6.0V
RC OSCILLATOR	V_H	V_{IL}	V_H	V_{IH}	V_{IL}	NU	NU	6.0V

Notes:
In EPROM Mode, all Z8 inputs are TTL inputs.
V_H = 12.5V ±0.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.

Internal Address Counter. The address of Z86E03/E06 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the high level of pin P00 (Clear) will reset the address to zero. Figure 16 shows the setup time of the serial address input.

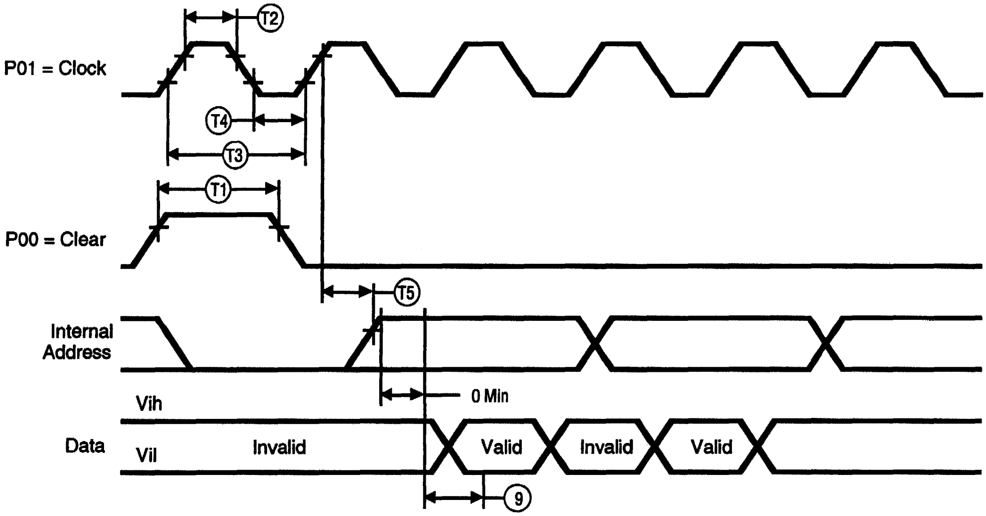
Programming Waveform. Figures 24, 25 and 26 show the programming waveforms of each mode. Table 7 shows the timing of programming waveforms.

Programming Algorithm. Figure 27 shows the flow chart of the Z86E03/E06 programming algorithm.

Table 8. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

SPECIAL FUNCTIONS (Continued)
EPROM Mode



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	30 ns Min
T3 Input Clock Period	70 ns Min
T4 Input Clock Low	30 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max

Figure 23. Z86E03/E06 Address Counter Waveform

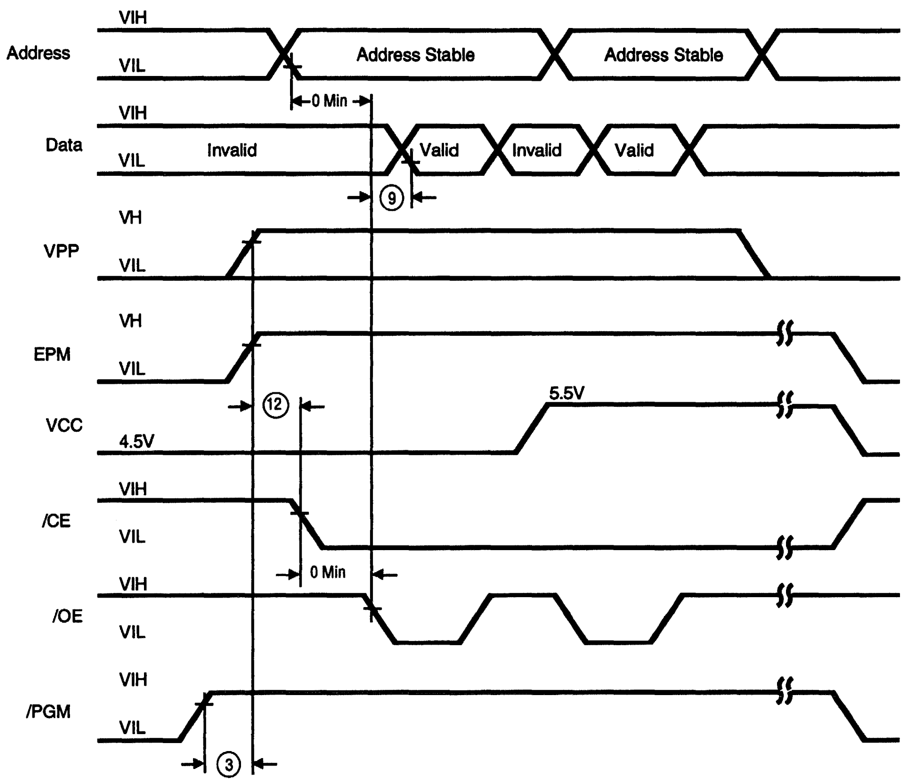


Figure 24. Z86E03/E07 Programming Waveform (EPROM Read)

SPECIAL FUNCTIONS (Continued)
EPROM Mode

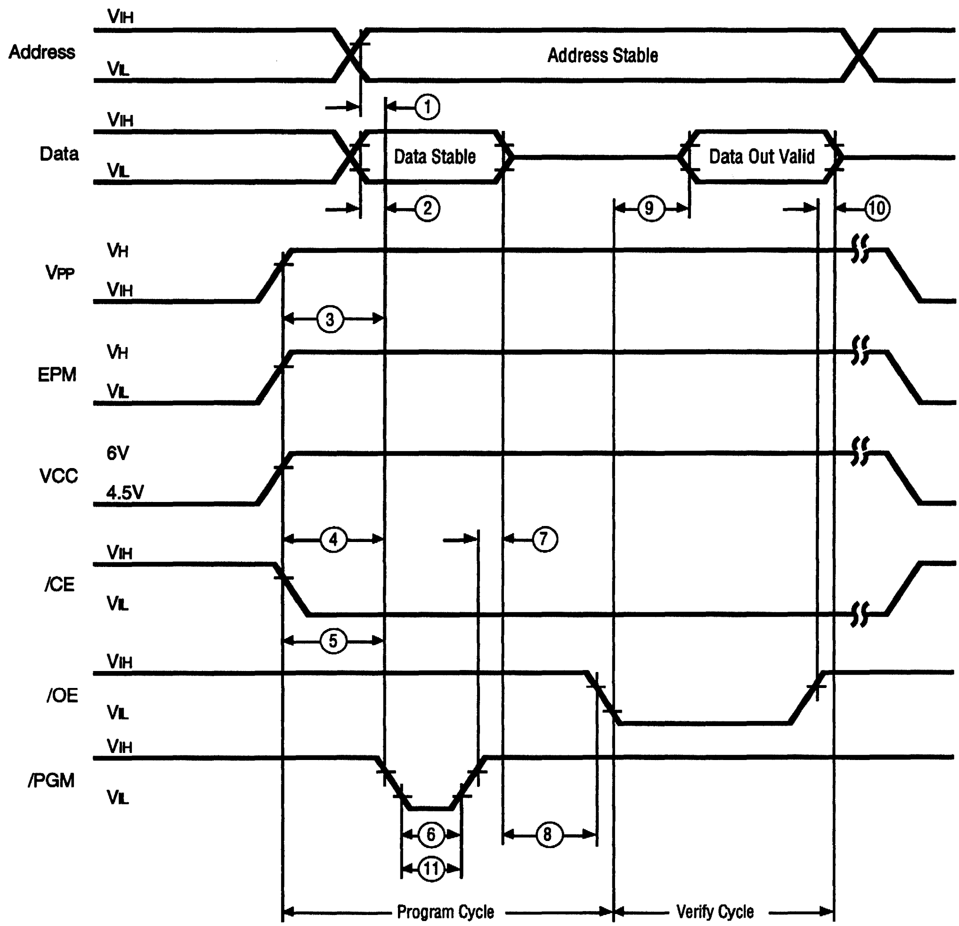


Figure 25. Z86E03/E06 Programming Waveform (Program and Verify)

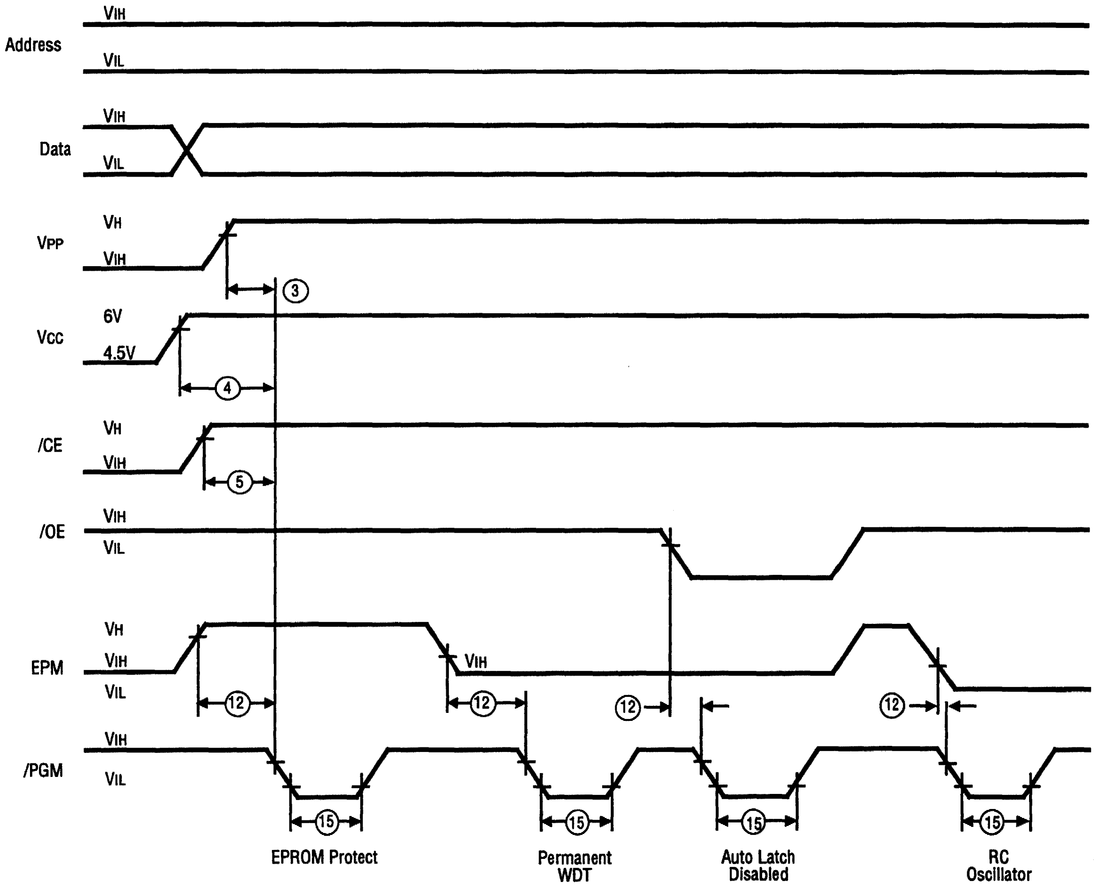
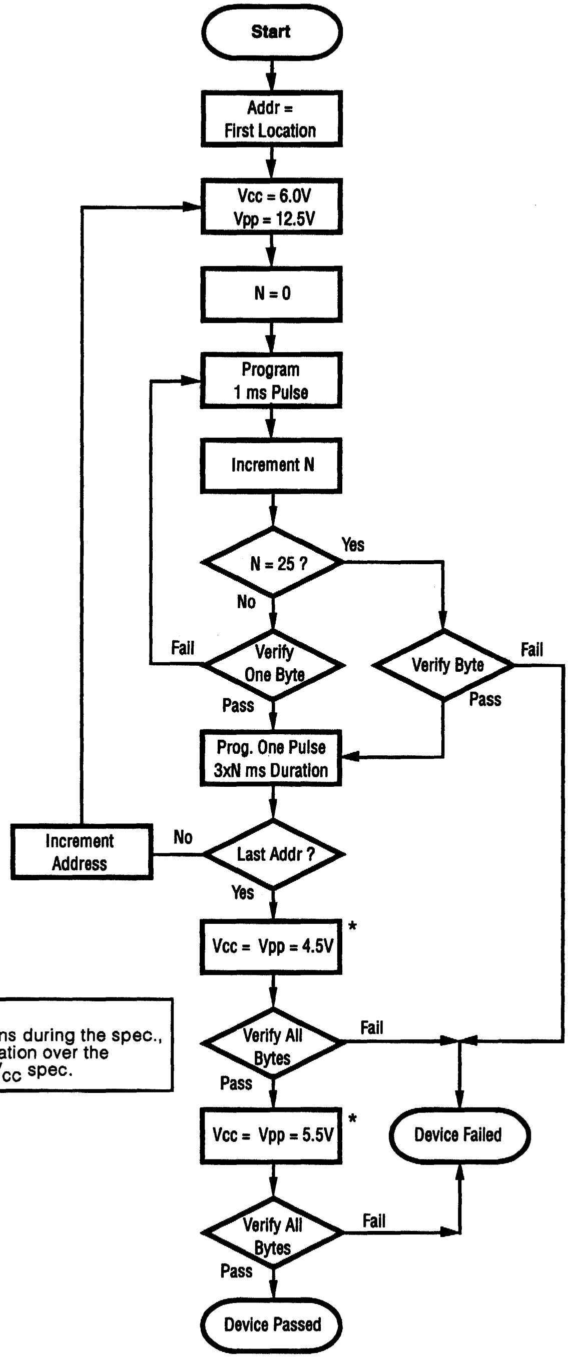


Figure 26. Z86E03/E06 Programming Waveform (EPROM Protect and Low EMI Program)

SPECIAL FUNCTIONS (Continued)
EPROM Mode



Note:
* To ensure proper operations during the spec., Zilog recommends verification over the V_{CC} range of the device V_{CC} spec.

Figure 27. Z86E03/E06 Programming Algorithm

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
V_{IHM}	Max Input Voltage**		12	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp	†		°C

Notes:
* Voltage on all pins with respect to GND.
** Applies to Port pins only and must limit current going into or out of Port pins to 250 µA maximum.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 28).

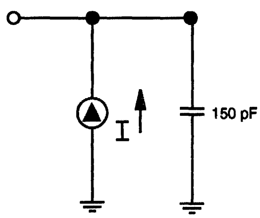


Figure 28. Test Load Configuration

CAPACITANCE

T_A = 25° C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input Capacitance	0	12 pF
Output Capacitance	0	20 pF
I/O Capacitance	0	25 pF

V_{CC} SPECIFICATION

V_{CC} = 3.0V to 5.5V

DC ELECTRICAL CHARACTERISTICS

Z86E03/E06

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.3V	0.9 V_{CC}	V_{CC}+0.3	0.9 V_{CC}	V_{CC}+0.3	2.4	V	Driven by External Clock Generator	
		5.0V	0.9 V_{CC}	V_{CC}+0.3	0.9 V_{CC}	V_{CC}+0.3	3.9	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.3V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.6	V	Driven by External Clock Generator	
		5.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	2.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	3.3V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.0	V		
		5.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.3V	V_{CC}–0.4		V_{CC}–0.4		3.1	V	I_{OH} = -2.0 mA	[10]
		5.0V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	I_{OH} = -2.0 mA	[10]
V_{OL1}	Output Low Voltage	3.3V		0.8		0.8	0.2	V	I_{OL} = +4.0 mA	[10]
		5.0V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	[10]
V_{OL2}	Output Low Voltage	3.3V		1.0		1.0	0.4	V	I_{OL} = + 6 mA, 3 Pin Max	[10]
		5.0V		1.0		1.0	0.5	V	I_{OL} = +12 mA, 3 Pin Max	[10]
V_{OFFSET}	Comparator Input Offset Voltage	3.3V		±10		±10	±5	mV		
		5.0V		±10		±10	±5	mV		
V_{ICR}	Input Common Mode Voltage Range	3.3V	0V	V_{CC}–1.0v	0V	V_{CC}–1.5v				[7]
		5.0V	0V	V_{CC}–1.0v	0V	V_{CC}–1.5v				[7]
I_{IL}	Input Leakage	3.3V	–1.0	1.0	–1.0	1.0		μA	V_{IN} = 0V, V_{CC}	
		5.0V	–1.0	1.0	–1.0	1.0		μA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.3V	–1.0	1.0	–1.0	1.0		μA	V_{IN} = 0V, V_{CC}	
		5.0V	–1.0	1.0	–1.0	1.0		μA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	3.3V		6		6	3.0	mA	@ 8 MHz	[4,5,12]
		5.0V		11.0		11.0	6.0	mA	@ 8 MHz	[4,5,12]
		3.3V		8.0		8.0	4.5	mA	@ 12 MHz	[4,5,10,13]
		5.0V		15		15	9.0	mA	@ 12 MHz	[4,5,10,13]
I_{OB}	Input Bias Current	3.3V		300		300		nA		[7]
		5.0V		300		300		nA		[7]
I_{IO}	Input Offset Current	3.3V		+150		+150		nA		[7]
		5.0V		+150		+150		nA		[7]

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OL3}	P36	5.0V		1.0		1.0		V	I_{OL} = 24 mA	
I_{CC1}	Standby Current	3.3V		3.0		3.0	1.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4, 5,12]
		5.0V		5		5	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4, 5,12]
		3.3V		4.5		4.5	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5,13]
		5.0V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5,13]
		3.3V		1.4		1.4	0.7	mA	Clock Divide-by-16 @ 8 MHz	[4, 5,12]
		5.0V		3.5		3.5	2.0	mA	Clock Divide-by-16 @ 8 MHz	[4, 5,12]
		3.3V		2.0		2.0	1.0	mA	Clock Divide-by-16 @ 12 MHz	[4, 5,13]
		5.0V		4.5		4.5	2.5	mA	Clock Divide-by-16 @ 12 MHz	[4, 5,13]
		5.0V		1.0		1.0		mA	HALT Mode @ 12 kHz	[4,5,11,13]
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6, 9]
		5.0V		10		20	3.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6, 9]
		3.3V		600		600	400	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6, 9,12]
		5.0V		1000		1000	800	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6, 9,12]
I_{ALL}	Auto Latch Low Current	3.3V		7.0		14.0	4.0	µA	0V < V_{IN} < V_{CC}	
		5.0V		20.0		30.0	10	µA	0V < V_{IN} < V_{CC}	
I_{ALH}	Auto Latch High Current	3.3V		–4.0		–8.0	–2.0	µA	0V < V_{IN} < V_{CC}	
		5.0V		–9.0		–16.0	–5.0	µA	0V < V_{IN} < V_{CC}	
T_{POR}	Power-On Reset	3.3V	7	24	6	25	13	ms		
		5.0V	3	13	2	14	7	ms		
V_{LV}	V_{CC} Low Voltage Protection Voltage		2.2	2.8	1.7	3.0	2.6	V	6 MHz max Int. CLK Freq.	[3]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven on XTAL	0.3	5.0	mA	8 MHz
Crystal or Ceramic Resonator	3.0	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND
[3] V_{CC} = 3.0V to 5.5V. The V_{LV} increases as the temperature decreases. Typical values measured at 3.3V and 5.0V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] C_{L1} = C_{L2} = 100 pF
[6] Same as note [4] except inputs at V_{CC}.
[7] For analog comparator inputs when analog comparators are enabled.
[8] Excludes clock pins.
[9] Clock must be forced Low when XTAL1 is clock-driven and XTAL2 is floating.
[10] STD mode (not low EMI mode).
[11] Low EMI Oscillator enabled.
[12] Z86E03 only.
[13] Z86E06 only.

2

AC ELECTRICAL CHARACTERISTICS
Z86E03/E06

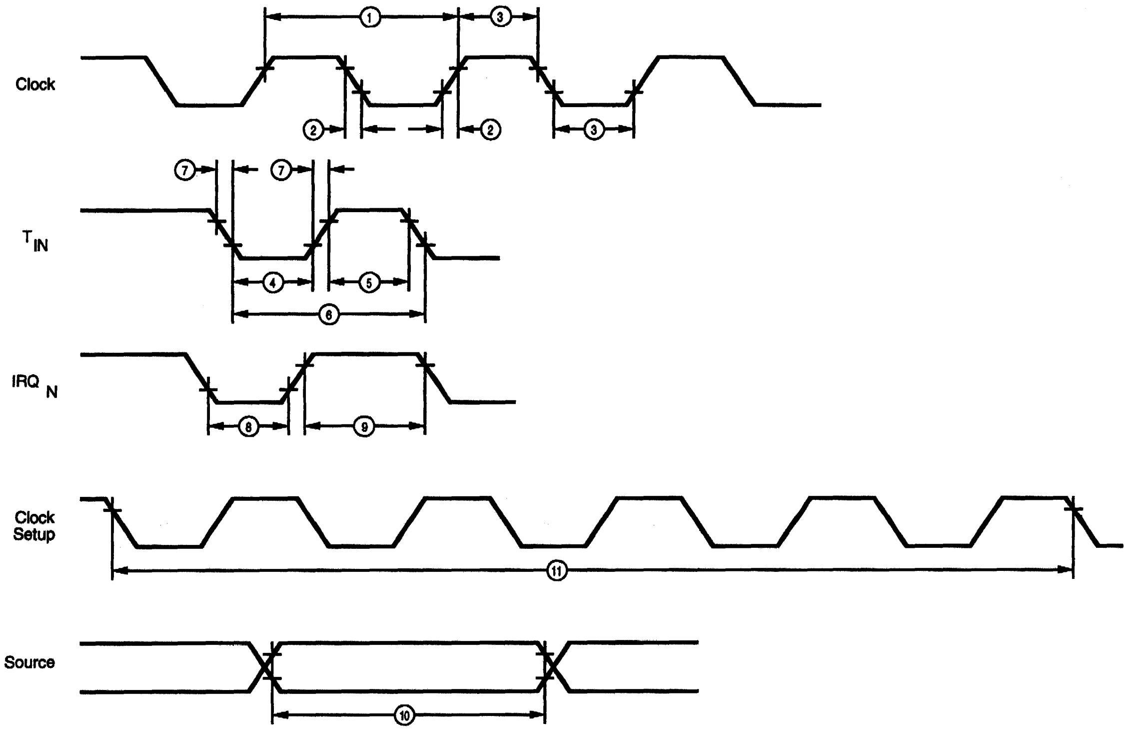


Figure 29. Additional Timing

AC ELECTRICAL CHARACTERISTICS
(SCLK/TCLK = EXTERNAL/2)

				T_A = 0°C To +70°C				T_A = –40°C To +105°C					
			V_{CC}	8 MHz [11]		12 MHz [11]		8 MHz [11]		12 MHz [11]			
No	Symbol	Parameter	Note[3]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	125	DC	83	DC	ns	[1,7,8]
			5.5V	125	DC	83	DC	125	DC	83	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15		25		15	ns	[1,7,8]
			5.5V		25		15		25		15	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	62		41		62		41		ns	[1,7,8]
			5.5V	62		41		62		41		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1,7,8]
			5.5V	70		70		70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			[1,7,8]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,7,8]

AC ELECTRICAL CHARACTERISTICS (Continued) (SCLK/TCLK = EXTERNAL/2)

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C TO +70°C 8 MHz[11] Min	Max	12 MHz[11] Min	Max	T_A = –40°C TO +105°C 8 MHz[11] Min	Max	12 MHz[11] Min	Max	Units	Notes
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			[1,7,8]
			5.5V	8TpC		8TpC		8TpC		8TpC			[1,7,8]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100		100		100	ns	[1,7,8]
			5.5V		100		100		100		100	ns	[1,7,8]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	[1,2,7,8]
			5.5V	70		70		70		70		ns	[1,2,7,8]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1,2,7,8]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,2,7,8]
10	Twsm	STOP Mode Recovery Width Spec	3.0V	12		12		12		12			[1,8,10]
			5.5V	12		12		12		12			[1,8,10]
11	Tost	Oscillator Startup Time	3.0V	5TpC		5TpC		5TpC		5TpC		ns	[1,3,4,9]
			5.5V	5TpC		5TpC		5TpC		5TpC		ns	[1,3,4,9]
12	Twdt	Watch-Dog Timer Refresh Time	3.0V	15		15		12		12		ms	D0 = 0 [5,6]
			5.5V	5		5		3		3		ms	D1 = 0 [5,6]
			3.0V	30		30		25		25		ms	D0 = 1 [5,6]
			5.5V	16		16		12		12		ms	D1 = 0 [5,6]
			3.0V	60		60		50		50		ms	D0 = 0 [5,6]
			5.5V	25		25		30		30		ms	D1 = 1 [5,6]
			3.0V	250		250		200		200		ms	D0 = 1 [5,6]
			5.5V	120		120		100		100		ms	D1 = 1 [5,6]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] V_{CC} = 3.0V to 5.5V.
[4] SMR-D5 = 0, POR delay is off.
[5] WDTMR Register
[6] Internal RC Oscillator only.
[7] SMR D1 = 0, SCLK = External/2
[8] Maximum frequency for internal system clock is 4 MHz when using SCLK = EXTERNAL clock mode.
[9] For RC and LC oscillator and for clock-driven oscillator.
[10] SMR-D5 = 1, STOP-Mode Recovery delay is on.
[11] Z86E03 = 8 MHz; Z86E06 = 12 MHz.

AC ELECTRICAL CHARACTERISTICS

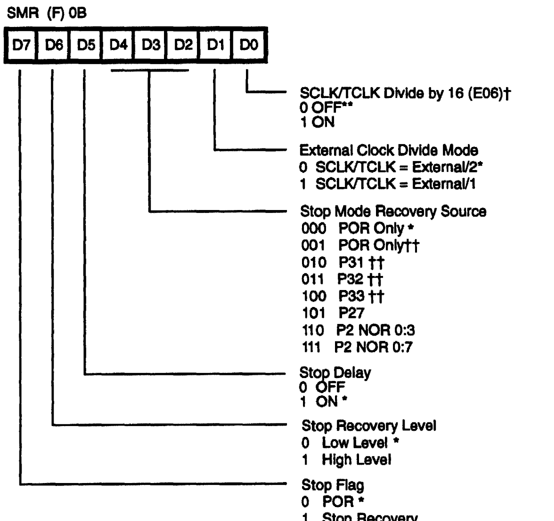
Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = EXTERNAL)

No	Symbol	Parameter	V_{CC} Note [6]	T_A = 0°C to +70°C 4 MHz Min	Max	T_A = –40°C to +105°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	[1,7,8]
			5.5V	250	DC	250	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	[1,7,8]
			5.5V		25		25	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	125		125		ns	[1,7,8]
			5.5V	125		125		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			[1,7,8]
			5.5V	3TpC		3TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1,7,8]
			5.5V	4TpC		4TpC			[1,7,8]
7	TrTin,	Timer Input Rise & Fall Timer	3.0V		100		100	ns	[1,7,8]
	TfTin		5.5V		100		100	ns	[1,7,8]
8	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,7,8]
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			[1,2,7,8]
			5.5V	3TpC		3TpC			[1,2,7,8]
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	[1,4,]
			5.5V	12		12		ns	[1,4]
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		[1,3,8,9]
			5.5V		5TpC		5TpC		[1,3,8,9]

Notes:

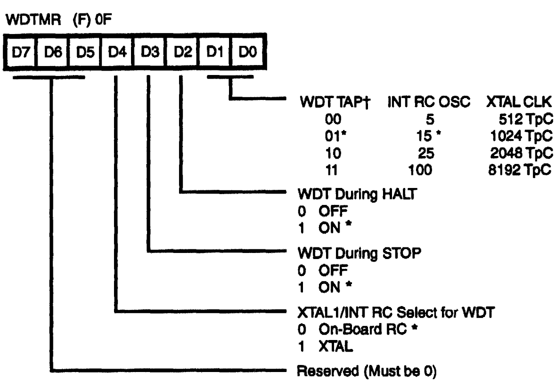
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P33-P31).
[3] SMR-D5 = 0.
[4] SMR-D5 = 1, POR STOP mode delay is on.
[5] Reg. WDTMR.
[6] V_{CC} = 3.0V to 5.5V.
[7] SMR D1 = 1.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.

EXPANDED REGISTER FILE CONTROL REGISTERS



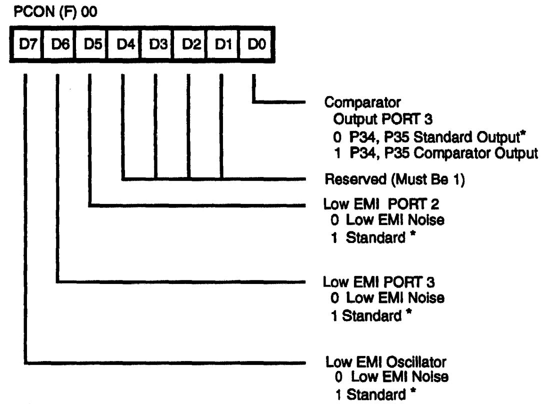
* Default setting after RESET.
** Default setting after RESET and STOP-Mode Recovery.
† E03 reserved; must be 0.
†† E06 only

Figure 30. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only)



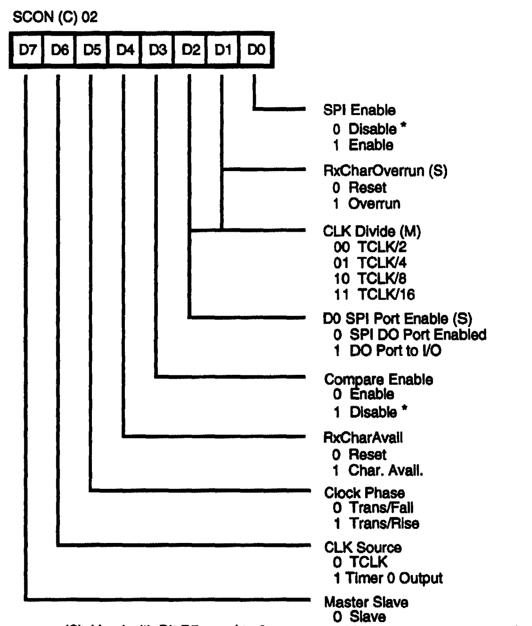
* Default setting after RESET.
† For E06; E03 must be D0 = 1, D1 = 0.

Figure 31. Watch-Dog Timer Mode Register (Write Only)



* Default Setting After Reset.

Figure 32. PORT Control Register (Write Only)



(S) Used with Bit D7 equal to 0
(M) Used with Bit D7 equal to 1

* Default Setting After Reset.

Figure 33. SPI Control Register (Z86E06 Only)

2

EXPANDED REGISTER FILE CONTROL REGISTERS (Continued)

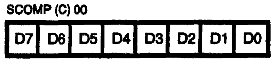


Figure 34. SPI Compare Register (Z86E06 Only)

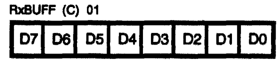


Figure 35. SPI Receive Buffer (Z86E06 Only)

Z8 CONTROL REGISTER DIAGRAMS

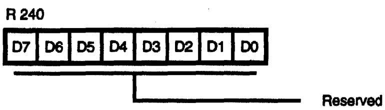


Figure 36. Reserved

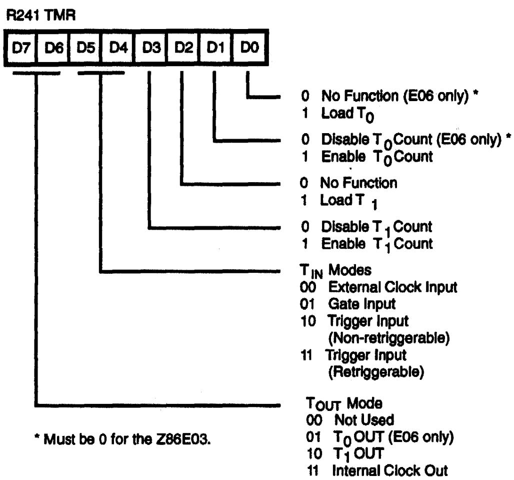


Figure 37. Timer Mode Register ($F1_H$: Read/Write)

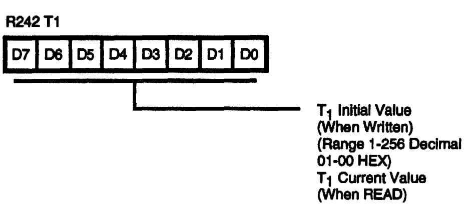


Figure 38. Counter Timer 1 Register ($F2_H$: Read/Write)

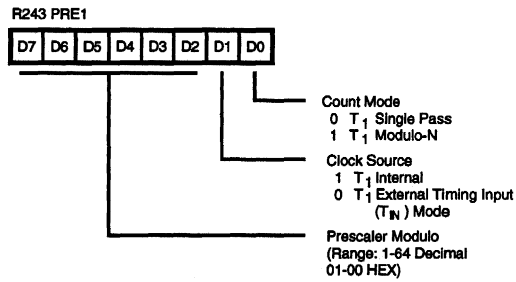


Figure 39. Prescaler 1 Register ($F3_H$: Write Only)

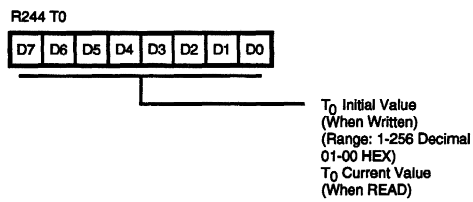


Figure 40. Counter/Timer 0 Register ($F4_H$: Read/Write; Z86E06 Only)

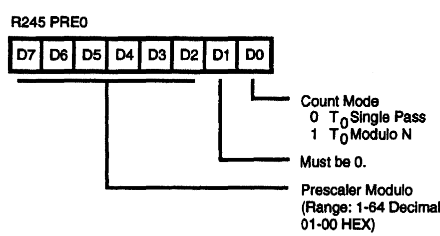


Figure 41. Prescaler 0 Register ($F5_H$: Write Only; Z86E06 Only)

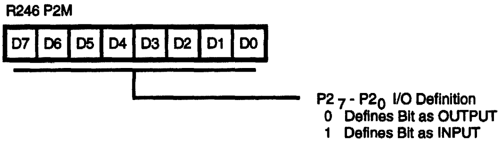


Figure 42. Port 2 Mode Register ($F6_H$: Write Only)

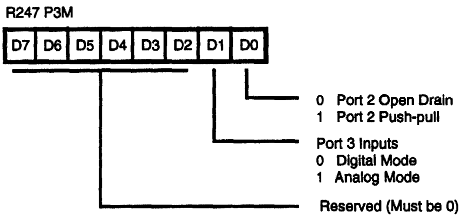


Figure 43. Port 3 Mode Register ($F7_H$: Write Only)

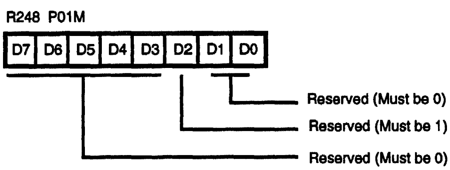


Figure 44. Port 0 and 1 Mode Register ($F8_H$: Write Only)

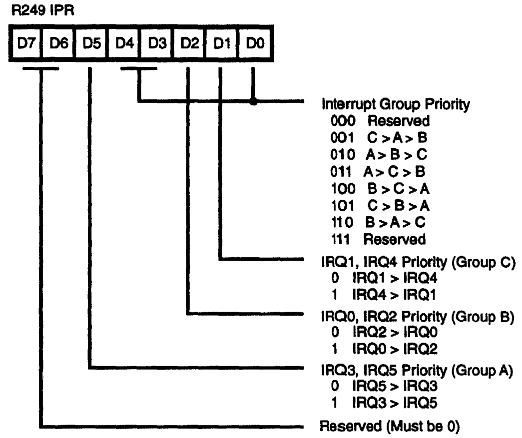


Figure 45. Interrupt Priority Register ($F9_H$: Write Only)

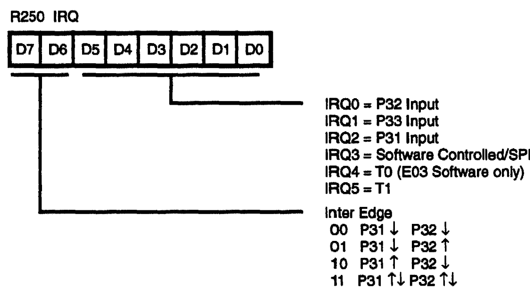


Figure 46. Interrupt Request Register (FA_H: Read/Write)

2

Z8 CONTROL REGISTER DIAGRAMS (Continued)

R251 IMR

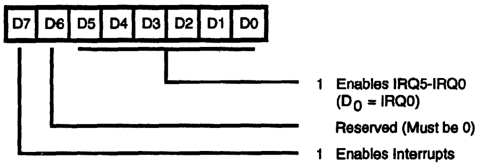


Figure 47. Interrupt Mask Register (FB_H: Read/Write)

R252 Flags

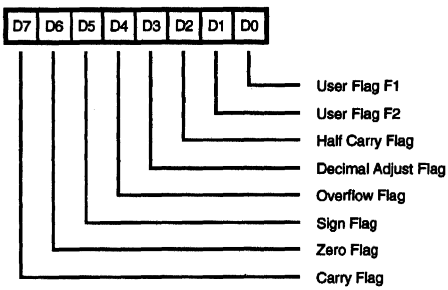


Figure 48. Flag Register (FC_H: Read/Write)

R253 RP

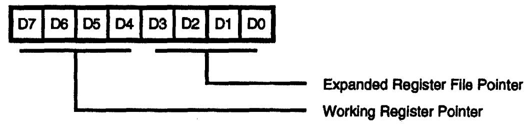


Figure 49. Register Pointer (FD_H: Read/Write)

R254 GPR

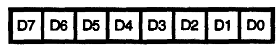


Figure 50. General Purpose Register (FE_H: Read/Write)

R255 SPL

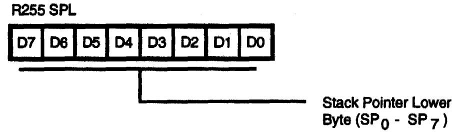


Figure 51. Stack Pointer (FF_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR address	Register pair or working register pair

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag
Affected flags are indicated by:	
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

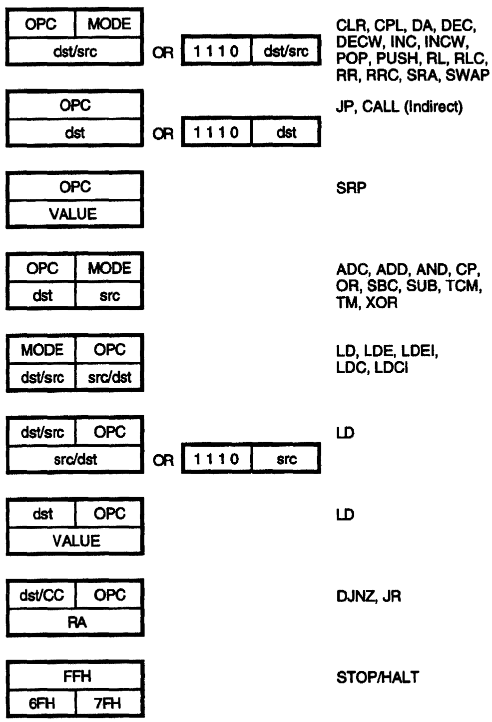
2

CONDITION CODES

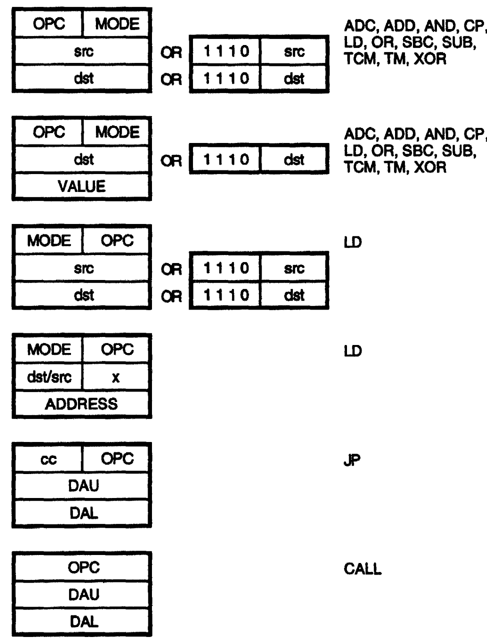
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

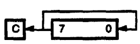
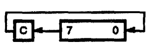
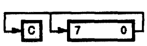
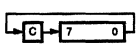
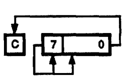
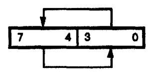
dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst + src +C	†		1[ ]	* * * * 0 *
ADD dst, src dst←dst + src	†		0[ ]	* * * * 0 *
AND dst, src dst←dst AND src	†		5[ ]	- * * 0 - -
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	- - - - - - -
CCF C←NOT C			EF	* - - - - - -
CLR dst dst←0	R IR		B0 B1	- - - - - - -
COM dst dst←NOT dst	R IR		60 61	- * * 0 - -
CP dst, src dst - src	†		A[ ]	* * * * - -
DA dst dst←DA dst	R IR		40 41	* * * X - -
DEC dst dst←dst - 1	R IR		00 01	- * * * - -
DECW dst dst←dst - 1	RR IR		80 81	- * * * - -
DI IMR(7)←0			8F	- - - - - - -
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, 128	RA		rA r = 0 - F	- - - - - - -
EI IMR(7)←1			9F	- - - - - - -
HALT			7F	- - - - - - -

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	- * * * - -
INCW dst dst←dst + 1	RR IR		A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	* * * * * *
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 - F 30	- - - - - - -
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	- - - - - - -
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - - -
LDC dst, src dst←src	r	Irr	C2	- - - - - - -
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir	Irr	C3	- - - - - - -
NOP			FF	- - - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	C	Z	S	V	D	H
OR dst, src dst←dst OR src	†	4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP+1	R IR	50 51	-	-	-	-	-	-
PUSH src SP←SP-1; @SP←src	R IR	70 71	-	-	-	-	-	-
RCF C←0		CF	0	-	-	-	-	-
RET PC←@SP; SP←SP+2		AF	-	-	-	-	-	-
RL dst 	R IR	90 91	*	*	*	*	-	-
RLC dst 	R IR	10 11	*	*	*	*	-	-
RR dst 	R IR	E0 E1	*	*	*	*	-	-
RRC dst 	R IR	C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst–src–C	†	3[ ]	*	*	*	*	1	*
SCF C←1		DF	1	-	-	-	-	-
SRA dst 	R IR	D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im	31	-	-	-	-	-	-
STOP		6F	1	-	-	-	-	-
SUB dst, src dst←dst - src	†	2[ ]	*	*	*	*	1	*
SWAP dst 	R IR	F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†	6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†	7[ ]	-	*	*	0	-	-
WDT		5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†	B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

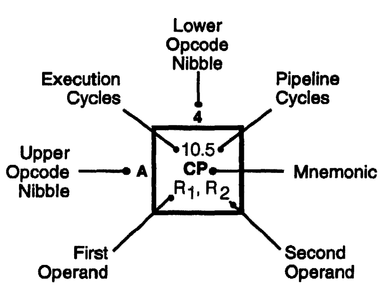
Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

2

OPCODE MAP

Lower Nibble (Hex) across; Upper Nibble (Hex) down.

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



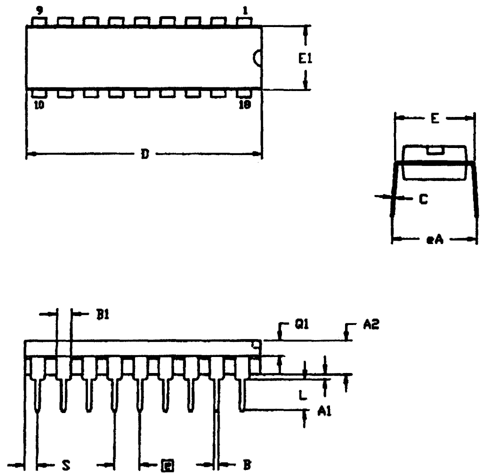
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_1 = Dst address
R_2 or r_2 = Src address

Sequence:
Opcode, First Operand, Second Operand

Note: The blank areas are reserved.

* 2-byte instruction appears as a 3-byte instruction

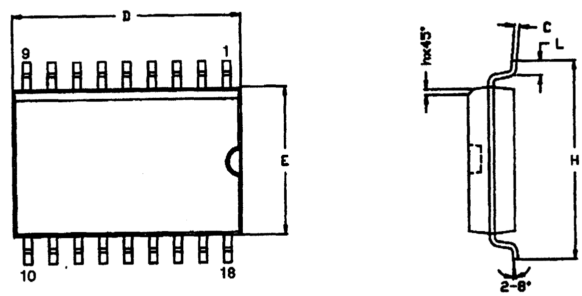
PACKAGE INFORMATION

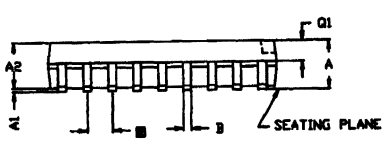


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
■	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
■	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86E03 (8 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86E0308PSC	Z86E0308SSC	Z86E0308PEC	Z86E0308SEC

Z86E06 (12 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86E0612PSC	Z86E0612SSC	Z86E0612PEC	Z86E0612SEC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
S = Plastic SOIC

Preferred Temperature
S = 0°C to +70°C

Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:
Z 86E03 08 P S C is a Z86E03, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 08 — Speed
- 86E03 — Product Number
- Z — Zilog Prefix

Z86C04/Z86C08

CMOS Z8® 8-BIT LOW-COST 1K/2K-ROM MICROCONTROLLERS

FEATURES

- The Z86C04/C08 Devices Have the Following General Characteristics:

Part	ROM	RAM	Speed
Z86C04	1 Kbytes	124	8 MHz
Z86C08	2 Kbyte	124	12 MHz

- 18-Pin Package (DIP and SOIC)
- 3.0V to 5.5V Operating Range
- Operating Temperature: –40°C to +105°C
- Clock Speed up to 8 MHz (C04), 12 MHz (C08)
- Low Power Consumption: 50 mW (Typical)
- Low Voltage Protection
- Fast Instruction Pointer: 1.5 µs @ 8 MHz (C04), 1.00 µs @ 12 MHz (C08)
- Two Standby Modes: STOP and HALT
- 14 Input/Output Lines
- Three Digital Inputs at CMOS Levels
- Eleven Digital Inputs at CMOS Levels; Schmitt-Triggered
- Two Programmable 8-Bit Counter/Timers, each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Software-Enabled Watch-Dog Timer
- Power-On Reset Timer
- Two On-Board Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive
- Programmable Interrupt Polarity
- Auto Latches
- ROM Protect, Low EMI Options

GENERAL DESCRIPTION

The Z86C04/C08 Microcontroller Units (MCUs) are members of the Z8® single-chip microcontroller family with 124 bytes of general-purpose RAM and 1/2 Kbytes of ROM, respectively. The devices are offered in 18-pin DIP and SOIC style packages and are manufactured in CMOS technology. Zilog's low-cost, low-power consumption Z86C04/C08 offers all the outstanding features of the Z8 family architecture, plus easy software/hardware system expansion .

For applications demanding powerful I/O capabilities, the Z86C04/C08 provides 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals. There are two basic address spaces available to support this configuration: Program Memory, and 124 bytes of general-purpose RAM.

To unburden the system from coping with real-time tasks, such as counting/timing and I/O data communications, the Z86C04/C08 offers two on-chip counter/timers with a large number of user-selectable modes. Additionally, two onboard comparators process analog signals with a common reference voltage (Figure 1).

GENERAL DESCRIPTION (Continued)

Characterized by a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features, the Z86C04/C08 is well-suited for a variety of consumer, industrial and commercial applications.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

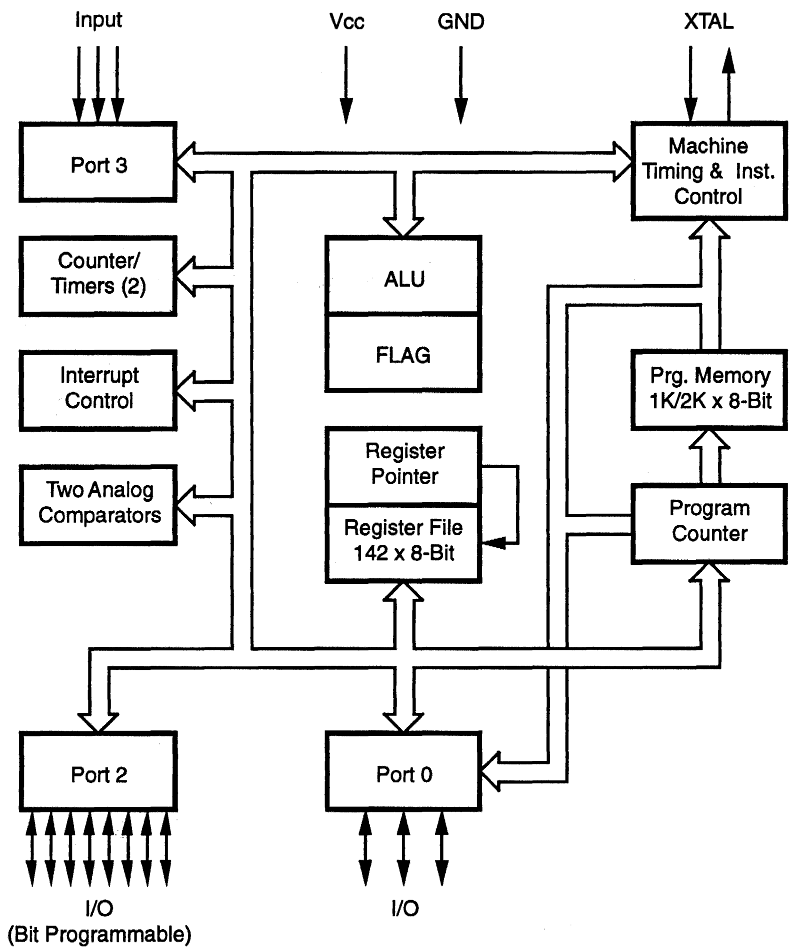


Figure 1. Z86C04/C08 Functional Block Diagram

PIN DESCRIPTIONS

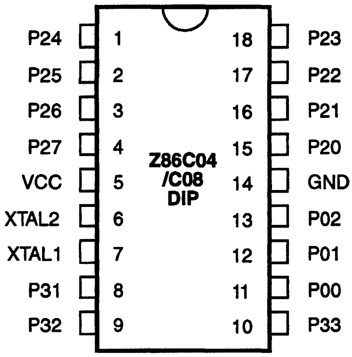


Figure 2. 18-Pin DIP Configuration

Table 1. 18-Pin DIP and SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1, 2, 3	In/Output

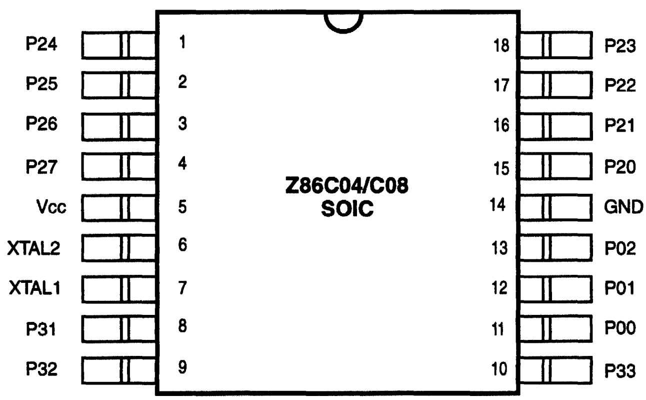


Figure 3. 18-Pin SOIC Pin Configuration

3

PIN DESCRIPTION (Continued)

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock to the on-chip clock oscillator and buffer.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Port 0 (P02-P00). Port 0 is a 3-bit I/O, bi-directional, Schmitt-triggered CMOS compatible I/O port. These three I/O lines can be configured under software control to be all inputs or all outputs (Figure 4).

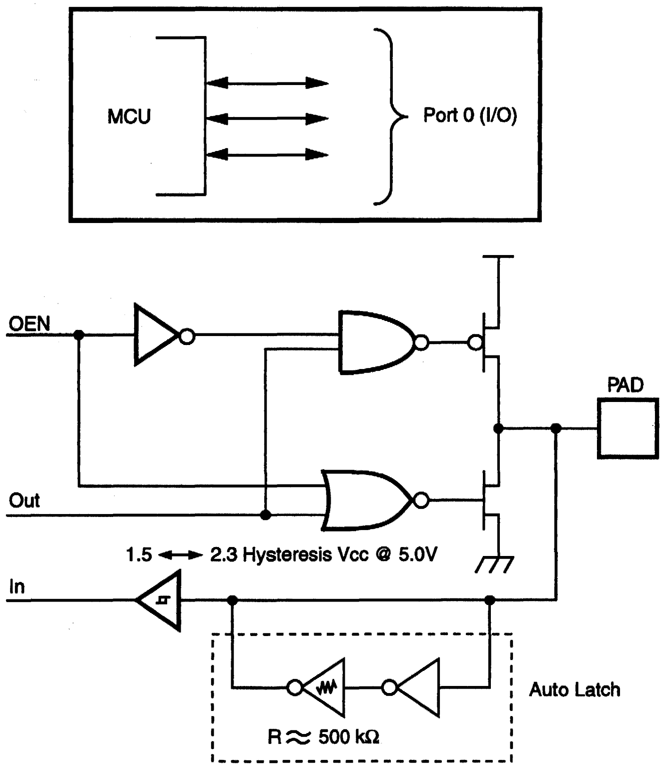


Figure 4. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit I/O, bit programmable, bi-directional, Schmitt-triggered CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 5).

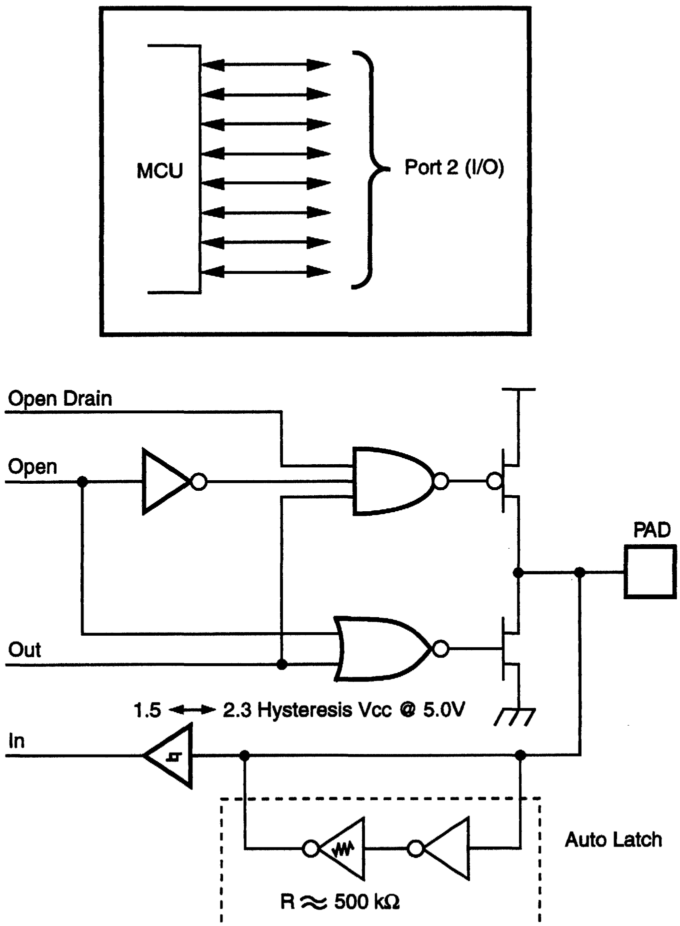
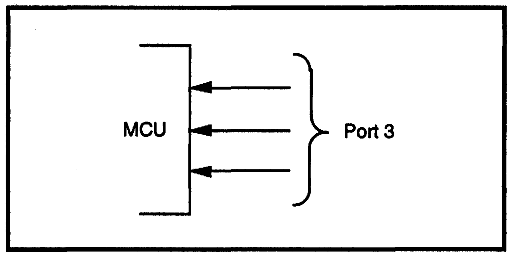


Figure 5. Port 2 Configuration

PIN DESCRIPTION (Continued)

Port 3 (P33-P31). Port 3 is a 3-bit, CMOS compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines can also be used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN}) (Figure 6).



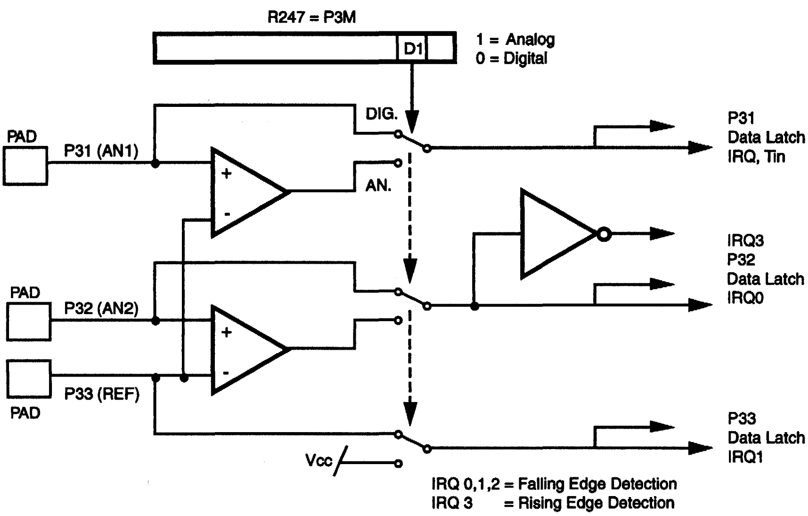


Figure 6. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to Port 3 inputs for interface flexibility. Typical applications for these on-board comparators are: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP mode. The common voltage range is 0-4V when the V_{CC} is 5.0V.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output may be used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternately, the comparators may be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

RESET. Upon power-up the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, and then starts program execution at address %000C (Hex) (Figure 7). The Z86C04/C08 control registers' reset value is shown in Table 2.

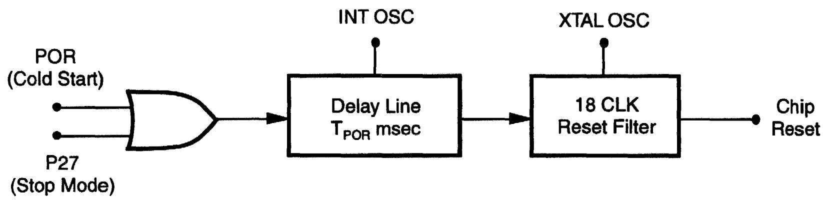


Figure 7. Internal Reset Configuration

Table 2. Z86C04/C08 Control Registers

Addr.	Reg.	Reset Condition D7	D6	D5	D4	D3	D2	D1	D0	Comments
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
FB	IMR	0	U	U	U	U	U	U	U	
FC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0	0	
FF	SPL	U	U	U	U	U	U	U	U	
*00	Port 0	U	U	U	U	U	U	U	U	
*02	Port 2	U	U	U	U	U	U	U	U	
03	Port 3	U	U	U	U	U	U	U	U	

Note:
* Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be re-configured as shown in Table 2 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86C04/C08 can address up to 1K/2K bytes of internal program memory (Figure 8). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-1023/2047 are on-chip mask-programmed ROM.

3

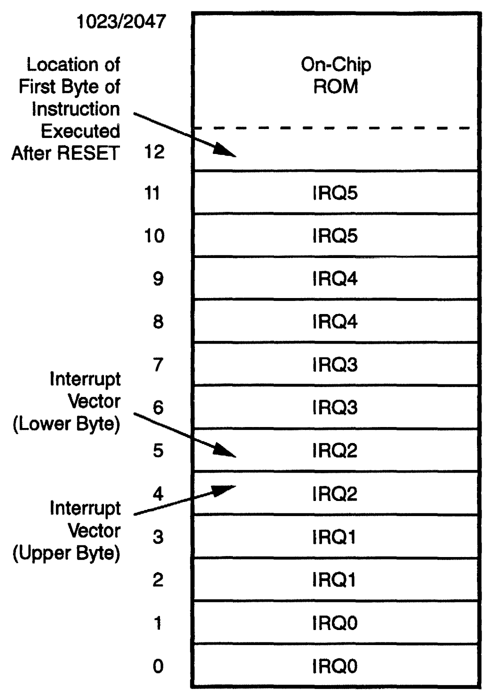


Figure 8. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 15 control and status registers (R0, R2-R3, R4-R127, and R241-R255, respectively; see Figure 9). Note that R254 is available for general purpose use. The Z86C04/C08 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 10) addresses the starting location of the active working-register group. Upon power-up, the general purpose registers are undefined.

Location		Indentifiers
255	Stack Pointer (Bits 7-0)	SPL
254	General Purpose Register	
253	Register Pointer	RP
252	Program Control Flags	Flags
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240 128	Not Implemented	
127 4	General Purpose Registers	
3	Port 3	P3
2	Port 2	P2
1	Reserved	P1
0	Port 0	P0

Figure 9. Register File

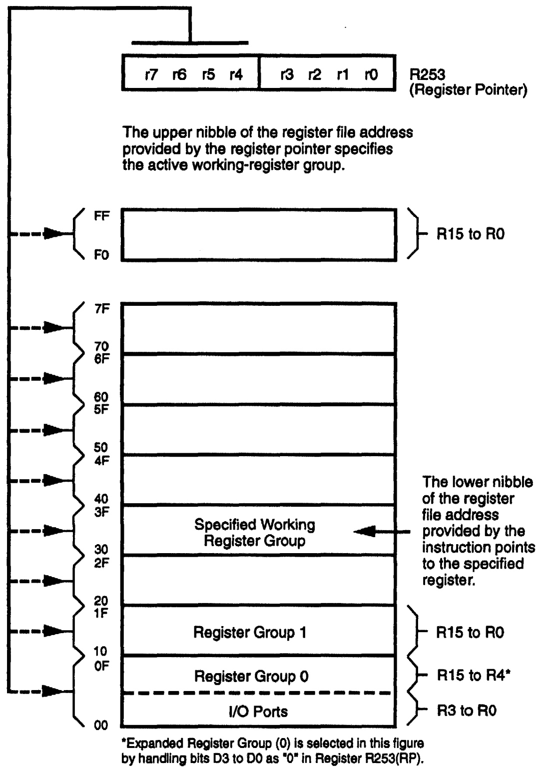


Figure 10. Register Pointer

Stack Pointer. The Z86C04/C08 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

General-Purpose Register (GPR). The general-purpose register upon device power-up is undefined. The general-purpose register upon a STOP-Mode Recovery and reset stays in its last state. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V. **Note:** Register R254 has been designated as a general-purpose register.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 11).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock.

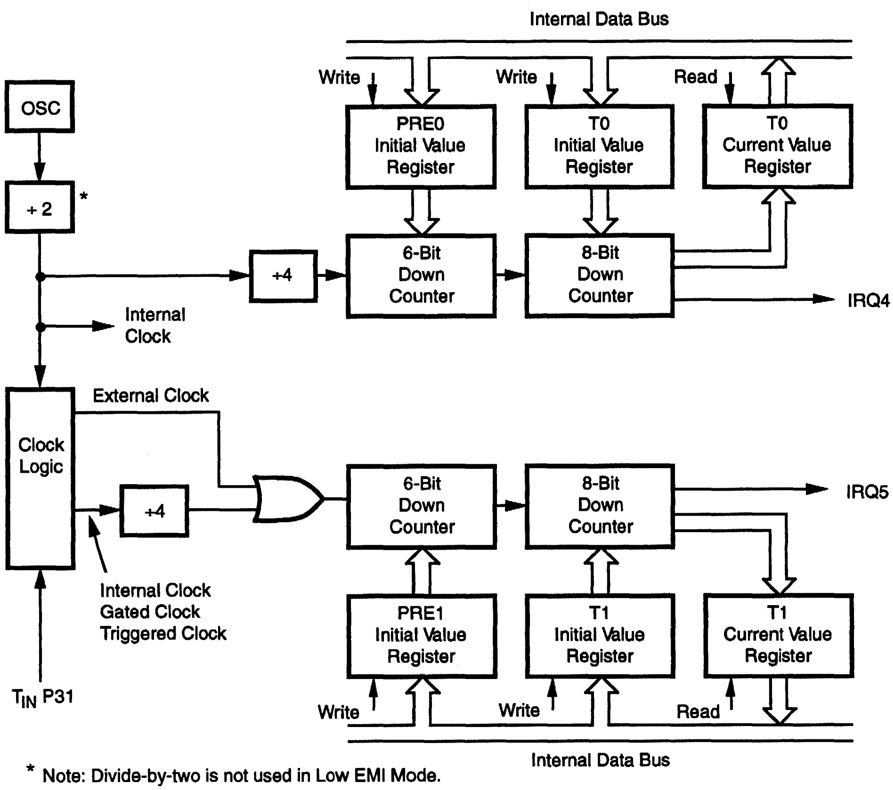


Figure 11. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86C04/C08 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 12). The six sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 3).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C04/C08 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86C08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the Z86CCP00ZEM emulator.

Table 3. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

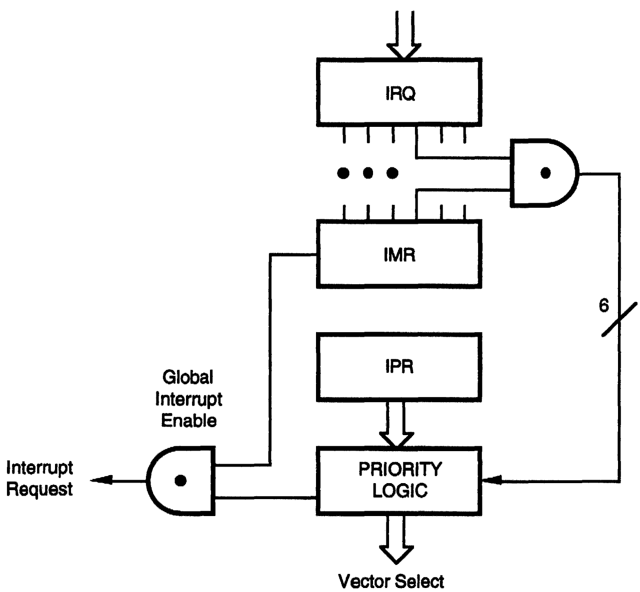


Figure 12. Interrupt Block Diagram

Clock. The Z86C04/C08 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms. **Note:** C04 is 8 MHz max.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's crystal recommended capacitors (capacitance is between 10 pF to 250 pF, which depends on the crystal manufacturer, ceramic resonator and PCB layout) from each pin directly to device Ground pin 14 (Figure 13).

Note that the crystal capacitor loads should be connected to V_{SS} pin 14 to reduce ground noise injection.

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device can be recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP mode can be released by two methods. The first method is a RESET of the device by removing V_{CC}. The second method is if P27 is configured as an input line when the device executes the STOP instruction. A low input condition on P27 releases the STOP mode.

Program execution under both conditions begins at location 000C (Hex). However, when P27 is used to release the STOP mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

(X = dependent upon user's application.)

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, that is, as follows:

```
FF   NOP     ; clear the pipeline
6F   STOP    ; enter STOP mode
             or
FF   NOP     ; clear the pipeline
7F   HALT    ; enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT should be refreshed once the WDT is enabled within every Twdt period; otherwise, the Z86C04/C08 resets itself. The WDT instruction affects the Flags accordingly: Z = 1, S = 0, V = 0.

WDT = 5F (Hex)

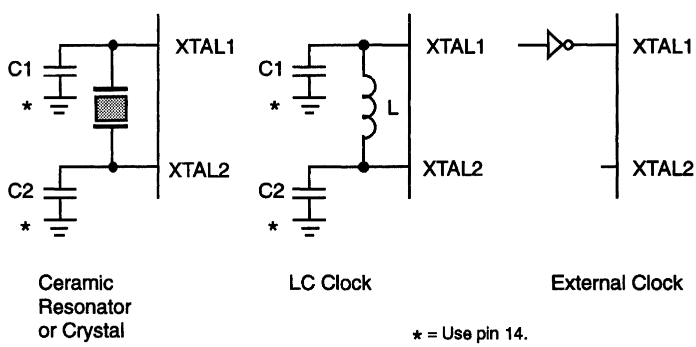


Figure 13. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Opcode WDT (5FH). The first time opcode 5FH is executed, the WDT is enabled, and subsequent execution clears the WDT counter. This has to be done within the maximum T_{WDT} period; otherwise, the WDT times out and generates a Reset. The generated Reset is the same as a Power-On Reset of T_{POR} plus 18 XTAL clock cycles. The WDT does not work in STOP mode. The WDT is disabled during and after a Reset, until the WDT is enabled again.

Opcode WDH (4FH). When this instruction is executed it will enable the WDT during HALT. If not, the WDT will stop when entering HALT. This instruction does not clear the counters, it facilitates running the WDT function during HALT mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Low Voltage Protection (V_{LV}). Maximum (V_{LV}) Conditions:

Case 1: T_A= –40°C, +85°C, Internal Clock Frequency equal or less than 2 MHz

Case 2: T_A= –40°C, +105°C, Internal Clock Frequency equal or less than 1 MHz

Note: The internal clock frequency is one-half the external clock frequency in standard mode.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low Voltage Protection trip point (V_{LV}) is reached. The device is guaranteed to function normally at supply voltages above the low voltage trip point for the temperatures and operating frequencies in Cases 1 and 2. The actual low voltage trip point is a function of temperature and process parameters (Figure 14).

2 MHz (Typical)

Temp	–40°	0°C	+25°C	+70°C	+105°C
V_{LV}	2.55	2.4	2.1	1.7	1.6

ROM Protect. ROM Protect fully protects the Z86C04/C08 ROM code from being read internally. **When ROM Protect is selected, the Z86C04/C08 will disable the instructions LDC and LDCI (Z86C04/C08 and Z86E04/E08 do not support the instructions of LDE and LDEI) in all modes. ROM look-up tables cannot be used in this mode.**

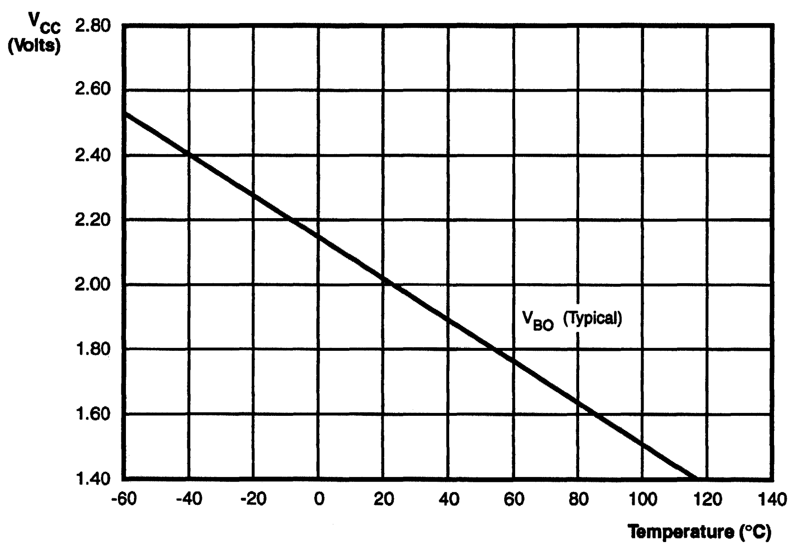


Figure 14. Typical Z86C04/C08 V_{LV} vs. Temperature

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+12	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on Pin 7 with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		462	mW
Maximum Current out of V_{SS}		84	mA
Maximum Current into V_{DD}		84	mA
Maximum Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Output Current Sinked by Any I/O Pin		12	mA
Maximum Output Current Sourced by Any I/O Pin		12	mA
Total Maximum Output Current Sinked by Port 2		70	mA
Total Maximum Output Current Sourced by Port 2		70	mA

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

Notes:
[1] This applies to all pins except where otherwise noted. Maximum current into pin must be ±600µA.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes Pin 6 and Pin 7.
[4] Device pin is not at an output Low state.

Total Power dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})] + sum of [(V_{DD} – V_{OH}) x I_{OH}] + sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 15).

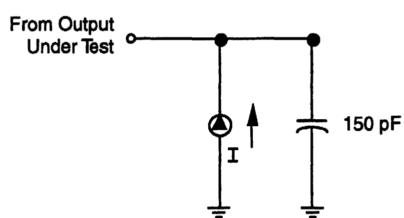


Figure 15. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		V_{CC}–0.4		3.0	V	I_{OH} = –2.0 mA	[5]
		5.5V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	[5]
		3.0V	V_{CC}–0.4		V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4		V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	
V_{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.2	V	I_{OL} = +4.0 mA	[5]
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	[5]
		3.0V		0.4		0.4		V	Low Noise @ I_{OL} = 1.0 mA	
		5.5V		0.4		0.4		V	Low Noise @ I_{OL} = 1.0 mA	
V_{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.8	V	I_{OL} = +12 mA, 3 Pin Max	[5]
		5.5V		0.8		0.8	0.3	V	I_{OL} = +12 mA, 3 Pin Max	[5]
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		
		5.5V		25		25	10	mV		
V_{LV}	V_{CC} Low Voltage			2.7		2.95	2.1	V	@ 1 MHz Max, Int. CLK Freq	
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
V_{VICR}	Comparator Input Common Mode Voltage Range		0	V_{CC} –1.0	0	V_{CC} –1.5		V		

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	3.2V					80	µA	All output and I/O Pins Floating @ 32 kHz	[7]
		3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 2 MHz	[5]
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @ 2 MHz	[5]
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 8 MHz	[5]
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @ 8 MHz	[5]
		3.0V		10		10	3.6	mA	All Output and I/O Pins Floating @ 12 MHz	[5,6]
		5.5V		15		15	9.0	mA	All Output and I/O Pins Floating @ 12 MHz	[5,6]
I_{CC1}	Standby Current	3.0V		2.5		2.5	0.7	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	[5]
		5.5V		4.0		5.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	[5]
		3.0V		4.0		4.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	[5]
		5.5V		5.0		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	[5]
		3.0V		4.5		4.5	1.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	[5,6]
		5.5V		7.0		7.0	4.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	[5,6]
I_{CC}	Supply Current (Low Noise Mode)	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 1 MHz	
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @ 1 MHz	
		3.0V		5.8		5.8	2.5	mA	All Output and I/O Pins Floating @ 2 MHz	
		5.5V		9.0		9.0	4.0	mA	All Output and I/O Pins Floating @ 2 MHz	
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 4 MHz	
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @ 4 MHz	

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC1}	Standby Current (Low Noise Mode)	3.0V		1.2		1.2	0.4	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz
		5.5V		1.6		1.6	0.9	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz
		3.0V		1.5		1.5	0.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		1.9		1.9	1	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		2.0		2.0	0.8	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz
		5.5V		2.4		2.4	0.3	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running
		5.5V		10		20	1.0	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running
I_{ALL}	Auto Latch Low Current	3.0V		6.0		8.0	3.0	µA	$0V < V_{IN} < V_{CC}$
		5.5V		22		30	16	µA	$0V < V_{IN} < V_{CC}$
I_{ALH}	Auto Latch High Current	3.0V		−4.0		-5.0	-1.5	µA	$0V < V_{IN} < V_{CC}$
		5.5V		−12.0		-20	-8.0	µA	$0V < V_{IN} < V_{CC}$

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3	5.0	mA	8 MHz
Crystal/Resonator	3.0	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND

[3] For 2.75V operating, the device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.

[4] V_{CC} = 3.0V to 5.5V, typical values measured at V_{CC} = 3.3V and V_{CC} = 5.0V.

[5] Standard Mode (not Low EMI mode)

[6] Z86C08 only.

[7] CL1 = 100 pF, CL2 = 220 pF, RF = 30 kOhm

AC ELECTRICAL CHARACTERISTICS

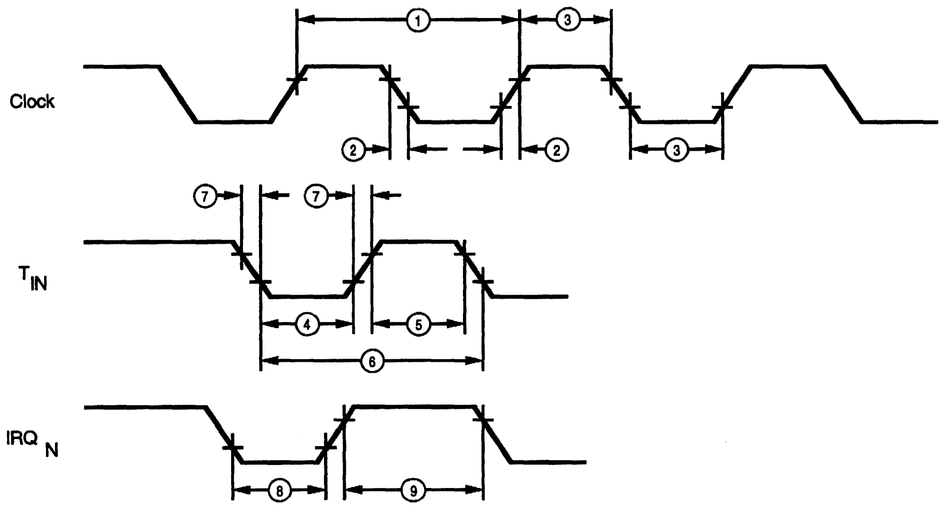


Figure 16. AC Electrical Timing Diagram

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AC ELECTRICAL CHARACTERISTICS
Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

				T_A = 0°C to +70°C				T_A = –40°C to +105°C					
				8 MHz (C04)		12 MHz (C08)		8 MHz (C04)		12 MHz (C08)			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	125	DC	83	DC	ns	[1]
			5.5V	125	DC	83	DC	125	DC	83	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15		25		15	ns	[1]
			5.5V		25		15		25		15	ns	
3	TwC	Input Clock Width	3.0V	62		41			62		41		[1]
			5.5V	62		41			62		41	ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1]
			5.5V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			[1]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			[1]
			5.5V	8TpC		8TpC		8TpC		8TpC			[1]
7	TrTin, TfTin	Timer Input Rise and Fall Timer	3.0V		100		100		100		100	ns	[1]
			5.5V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	[1,2]
			5.5V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	3.0V		25		25		25		25	ms	[1]
			5.5V		12		12		10		10	ms	[1]
11	Tpor		3.0V	24		24		24		24		ms	[1]
			5.5V	12		12		12		12		ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).

AC ELECTRICAL CHARACTERISTICS
Low Noise Mode

				T_A= 0°C to +70°C				T_A= –40°C to +105°C					
				1 MHz		4 MHz		1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TPC	Input Clock Period	3.0V	1000	DC	250	DC	1000	DC	250	DC	ns	[1]
			5.5V	1000	DC	250	DC	1000	DC	250	DC	ns	[1]
2	TrC	Clock Input Rise	3.0V		25		25		25		25	ns	[1]
	TfC	and Fall Times	5.5V		25		25		25		25	ns	[1]
3	TwC	Input Clock Width	3.0V	500		125		500		125		ns	[1]
			5.5V	500		125		500		125		ns	[1]
4.	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1]
			5.5V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC		4TpC		4TpC			[1]
			5.5V	4TpC		4TpC		4TpC		4TpC			[1]
7	TrTin,	Timer Input Rise	3.0V		100		100		100		100	ns	[1]
	TtTin	and Fall Timer	5.5V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input	3.0V	100		100		100		100		ns	[1,2]
		Low Time	5.5V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
		High Time	5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer	3.0V		25		25		25		25	ms	[1]
		Delay Time	5.5V		12		12		10		10	ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).

3

LOW NOISE VERSION

Low EMI Emission

The Z86C04/C08 can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

EMI Characteristics

The Z86C04/C08 operating in the Low EMI mode generates EMI as measured in the following chart:

The measurements, shown in Figure 17, were made while operating the Z86C04/C08 in three states: (1) idle condition; (2) static output; (3) switched output.

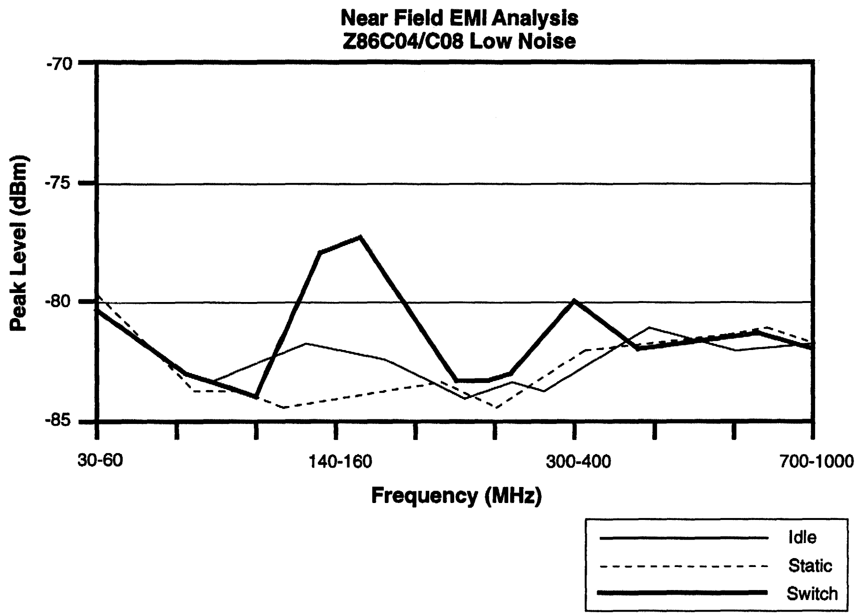

Figure 17. Low Noise Analysis

Z8® CONTROL REGISTER DIAGRAMS

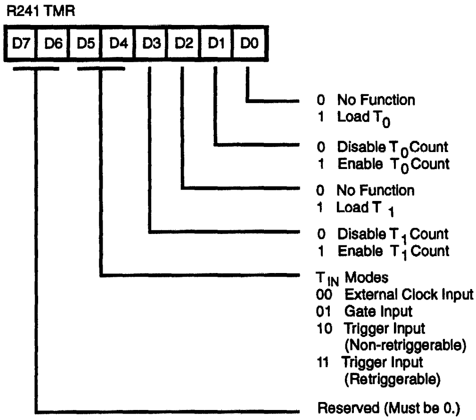

Figure 18. Timer Mode Register ($F1_H$: Read/Write)

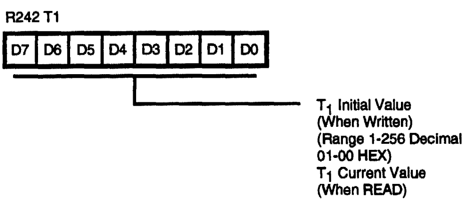

Figure 19. Counter Time 1 Register ($F2_H$: Read/Write)

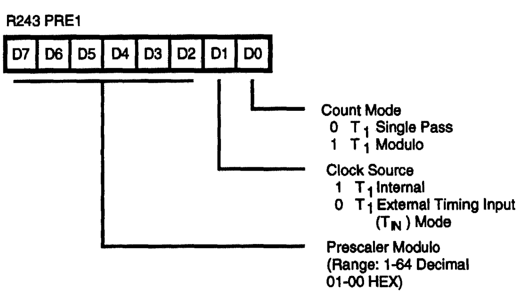

Figure 20. Prescaler 1 Register ($F3_H$: Write Only)

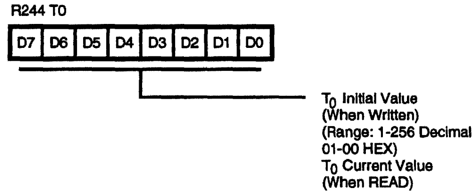

Figure 21. Counter/Timer 0 Register ($F4_H$: Read/Write)

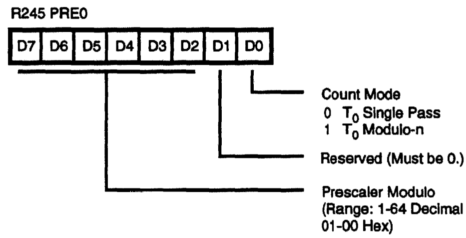

Figure 22. Prescaler 0 Register ($F5_H$: Write Only)

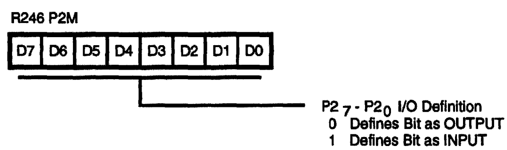

Figure 23. Port 2 Mode Register ($F6_H$: Write Only)

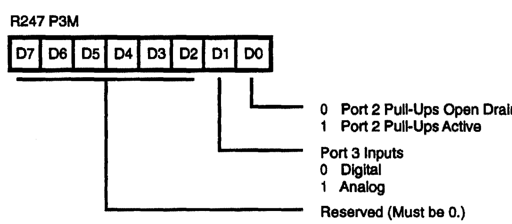

Figure 24. Port 3 Mode Register ($F7_H$: Write Only)

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Z8 CONTROL REGISTER DIAGRAMS (Continued)

R248 P01M

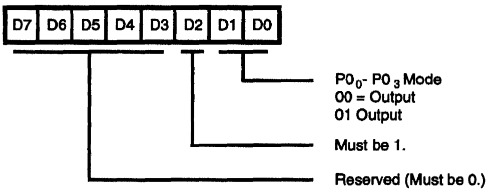

Figure 25. Port 0 and 1 Mode Register ($F8_H$: Write Only)

R249 IPR

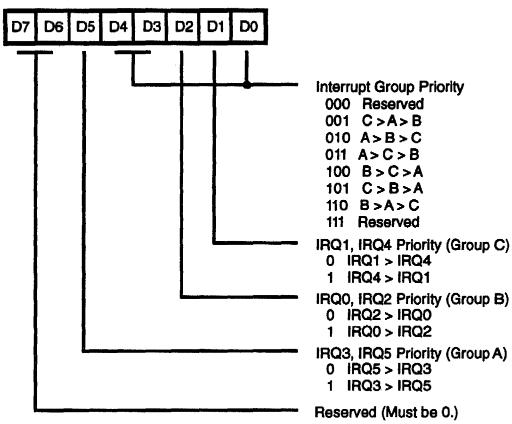

Figure 26. Interrupt Priority Register ($F9_H$: Write Only)

R250 IRQ

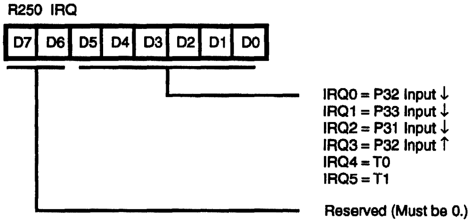

Figure 27. Interrupt Request Register (FA_H: Read/Write)

R251 IMR

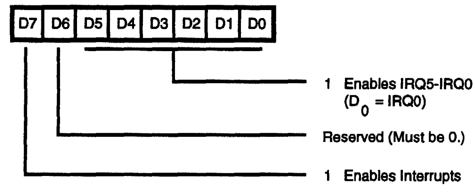

Figure 28. Interrupt Mask Register (FB_H: Read/Write)

R252 Flags

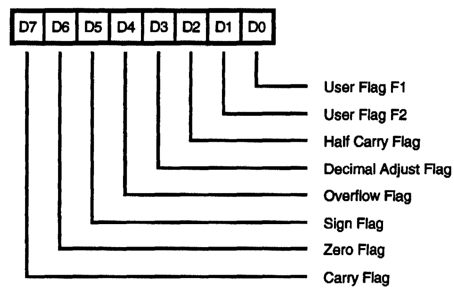

Figure 29. Flag Register (FC_H: Read/Write)

R253 RP

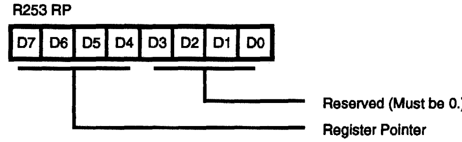

Figure 39. Register Pointer (FD_H: Read/Write)

R255 SPL

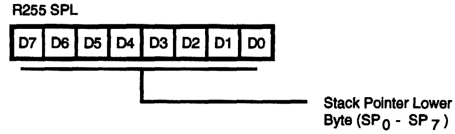

Figure 31. Stack Pointer (FF_H: Read/Write)

DEVICE CHARACTERISTICS

Standard Mode

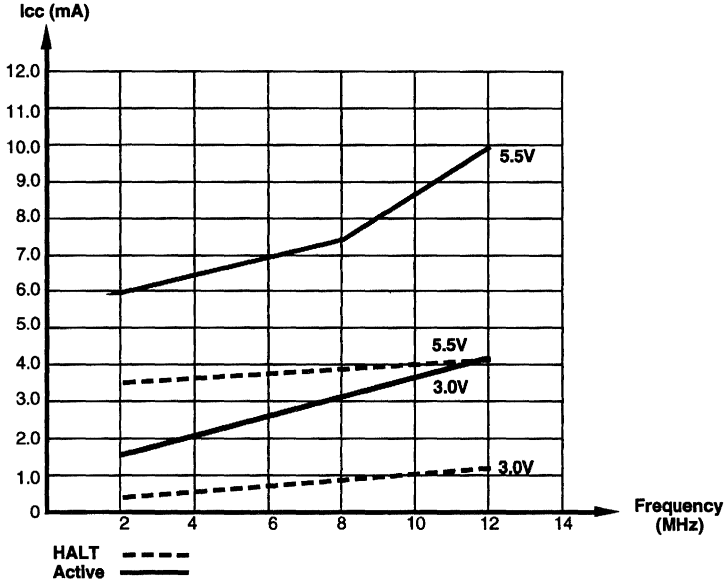

Figure 32. Typical I_{CC} vs Frequency

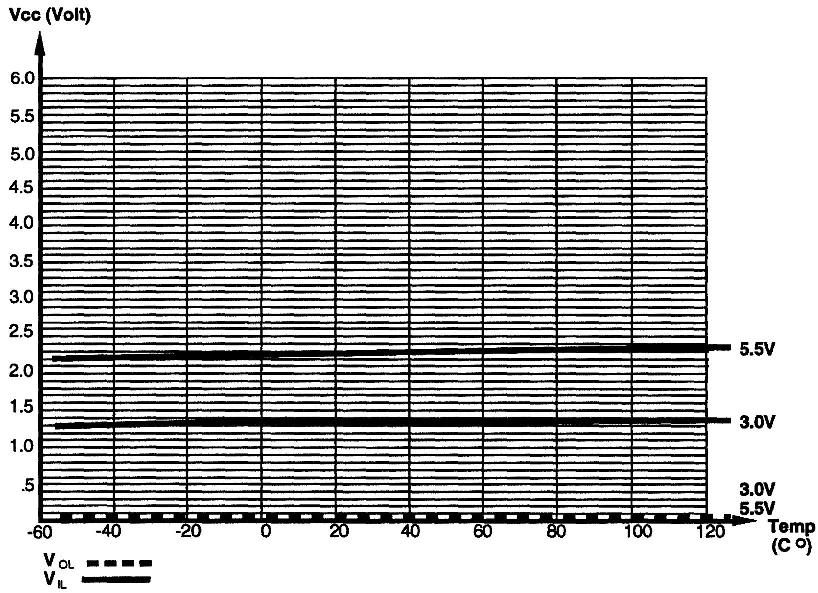

Figure 33. V_{IL}, V_{OL} vs. Temperature

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DEVICE CHARACTERISTICS (Continued)

Standard Mode

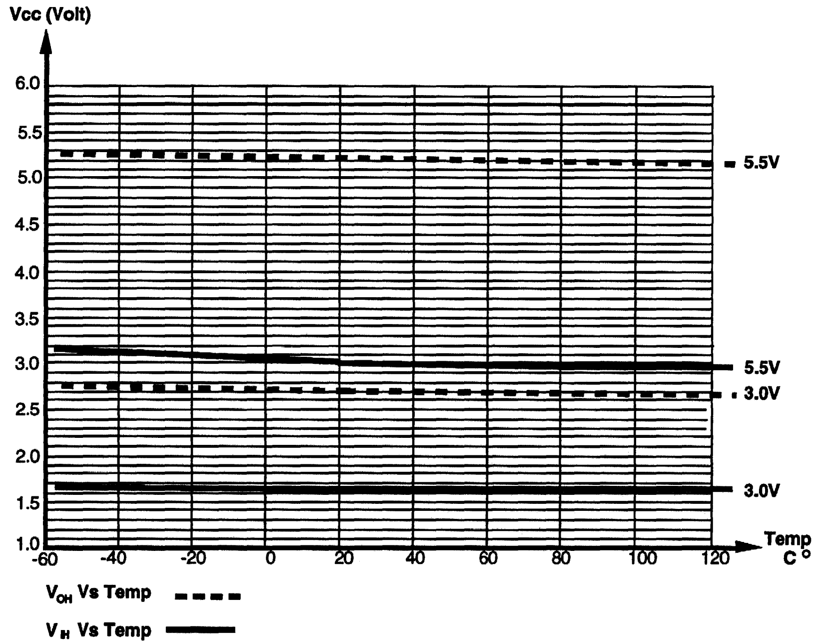


Figure 34. V_{IH}, V_{OH} vs. Temperature

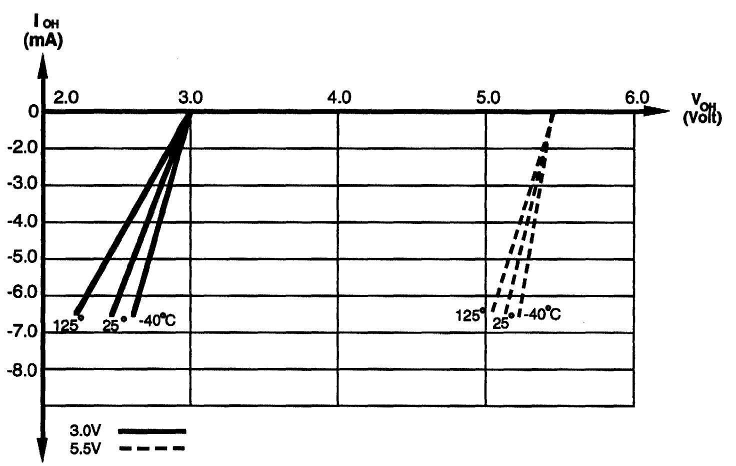


Figure 35. Typical I_{OH} vs. V_{OH}

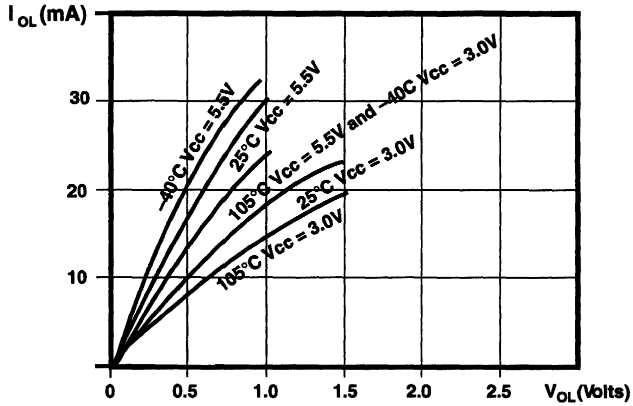


Figure 36. Typical I_{OL} vs. V_{OL}

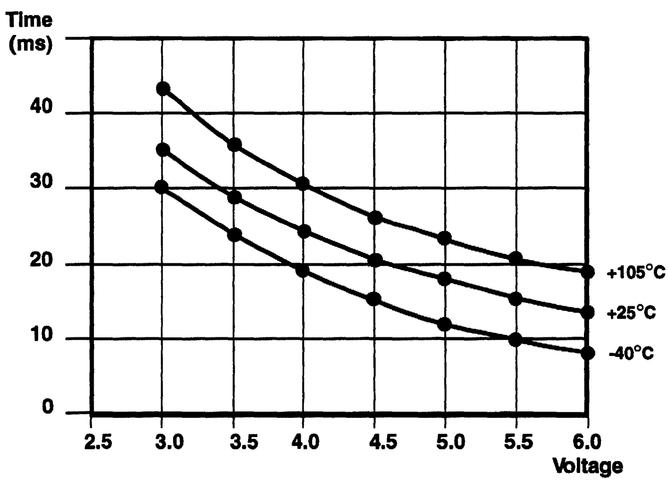


Figure 37. Typical WDT Time Out Period vs V_{CC} Over Temperature

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	—	Always true	—
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000	F	Never true (always false)	—

INSTRUCTION FORMATS

Format	Instructions
OPC	CCF, DI, EI, IRET, NOP, RCF, RET, SCF
dst | OPC	INC r

One-Byte Instructions

Format	Alternate	Instructions
OPC | MODE; dst/src	OR 1110 | dst/src	CLR, CPL, DA, DEC, DECW, INC, INCW, POP, PUSH, RL, RLC, RR, RRC, SRA, SWAP
OPC; dst	OR 1110 | dst	JP, CALL (Indirect)
OPC; VALUE		SRP
OPC | MODE; dst | src		ADC, ADD, AND, CP, OR, SBC, SUB, TCM, TM, XOR
MODE | OPC; dst/src | src/dst		LD, LDE, LDEI, LDC, LDCI
dst/src | OPC; src/dst	OR 1110 | src	LD
dst | OPC; VALUE		LD
dst/CC | OPC; RA		DJNZ, JR
FFH; 6FH | 7FH		STOP/HALT

Two-Byte Instructions

Format	Alternate	Instructions
OPC | MODE; src; dst	OR 1110 | src; OR 1110 | dst	ADC, ADD, AND, CP, LD, OR, SBC, SUB, TCM, TM, XOR
OPC | MODE; dst; VALUE	OR 1110 | dst	ADC, ADD, AND, CP, LD, OR, SBC, SUB, TCM, TM, XOR
MODE | OPC; src; dst	OR 1110 | src; OR 1110 | dst	LD
MODE | OPC; dst/src | x; ADDRESS		LD
cc | OPC; DAU; DAL		JP
OPC; DAU; DAL		CALL

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

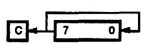
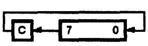
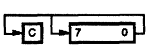
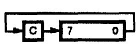
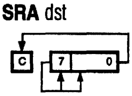
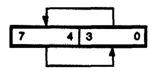
dst(7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src dst ← dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst ← dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst ← dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP ← SP − 2 @SP ← PC, PC ← dst	DA IRR		D6 D4	–	–	–	–	–	–
CCF C ← NOT C			EF	*	–	–	–	–	–
CLR dst dst ← 0	R IR		B0 B1	–	–	–	–	–	–
COM dst dst ← NOT dst	R IR		60 61	–	*	*	0	–	–
CP dst, src dst ← src	†		A[ ]	*	*	*	*	–	–
DA dst dst ← DA dst	R IR		40 41	*	*	*	X	–	–
DEC dst dst ← dst − 1	R IR		00 01	–	*	*	*	–	–
DECW dst dst ← dst − 1	RR IR		80 81	–	*	*	*	–	–
DI IMR(7) ← 0			8F	–	–	–	–	–	–
DJNZr, dst r ← r − 1 if r ≠ 0 PC ← PC + dst Range: +127, −128	RA		rA r = 0 − F	–	–	–	–	–	–
EI IMR(7) ← 1			9F	–	–	–	–	–	–
HALT			7F	–	–	–	–	–	–
INC dst dst ← dst + 1	r R IR		rE r = 0 − F 20 21	–	*	*	*	–	–
INCW dst dst ← dst + 1	RR IR		A0 A1	–	*	*	*	–	–
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) − 1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC ← dst	DA IRR		cD c = 0 − F 30	–	–	–	–	–	–
JR cc, dst if cc is true, PC ← PC + dst Range: +127, −128	RA		cB c = 0 − F	–	–	–	–	–	–
LD dst, src dst ← src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 − F C7 D7 E3 F3 E4 E5 E6 E7 F5	–	–	–	–	–	–
LDC dst, src dst ← src	r	Irr	C2	–	–	–	–	–	–
LDCI dst, src dst ← src r ← r + 1; rr ← rr + 1	Ir	Irr	C3	–	–	–	–	–	–
NOP			FF	–	–	–	–	–	–

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
OR dst, src dst ← dst OR src	†		4[ ]	–	*	*	0	–	–
POP dst dst ← @SP; SP ← SP + 1	R IR		50 51	–	–	–	–	–	–
PUSH src SP ← SP – 1; @SP ← src	R IR		70 71	–	–	–	–	–	–
RCF C ← 0			CF	0	–	–	–	–	–
RET PC ← @SP; SP ← SP + 2			AF	–	–	–	–	–	–
RL dst 	R IR		90 91	*	*	*	*	–	–
RLC dst 	R IR		10 11	*	*	*	*	–	–
RR dst 	R IR		E0 E1	*	*	*	*	–	–
RRC dst 	R IR		C0 C1	*	*	*	*	–	–
SBC dst, src dst ← dst – src – C	†		3[ ]	*	*	*	*	1	*
SCF C ← 1			DF	1	–	–	–	–	–
SRA dst 	R IR		D0 D1	*	*	*	0	–	–
SRP dst RP ← src	Im		31	–	–	–	–	–	–
STOP			6F	1	–	–	–	–	–
SUB dst, src dst ← dst – src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	–	–
TCM dst, src (NOT dst) AND src	†		6[ ]	–	*	*	0	–	–
TM dst, src dst AND src	†		7[ ]	–	*	*	0	–	–
WDH			4F	–	–	–	–	–	–
WDT			5F	–	X	X	X	–	–
XOR dst, src dst ← dst XOR src	†		B[ ]	–	*	*	0	–	–

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

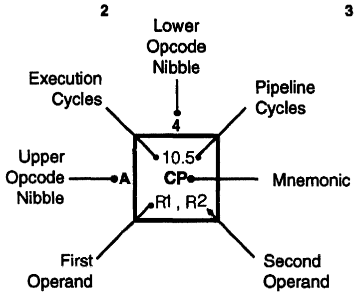
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								4.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2	2	2	2	3	3	3	3	2	2	2	2	2	3	1	1



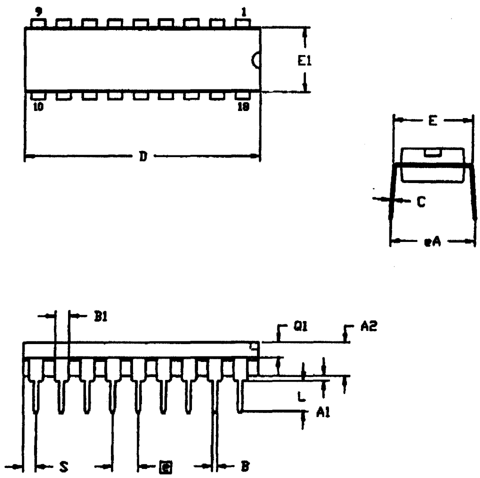
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas are reserved.

*2-byte instruction appears as a 3-byte instruction

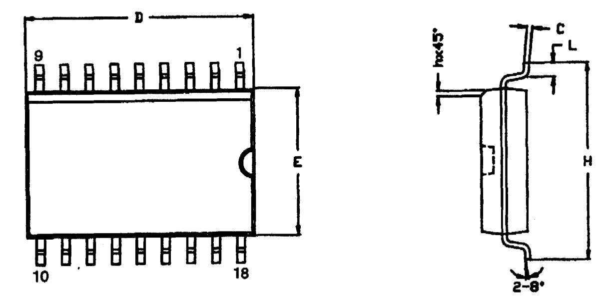
PACKAGE INFORMATION

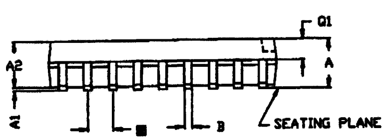


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
■	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
■	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C04 (8 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	**18-Pin SOIC**	**18-Pin DIP**	**18-Pin SOIC**
Z86C0408PSC	Z86C0408SSC	Z86C0408PEC	Z86C0408SEC

Z86C08 (12 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	**18-Pin SOIC**	**18-Pin DIP**	**18-Pin SOIC**
Z86C0812PSC	Z86C0812SSC	Z86C0812PEC	Z86C0812SEC

For fast results, contact your local Zilog sale offices for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = DIP

Longer Lead Time
S = SOIC

Preferred Temperature
S = 0°C to +70°C

Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:
Z 86C04 08 P S C is a Z86C04, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 08 — Speed
- 86C04 — Product Number
- Z — Zilog Prefix

3

ZiLOG

PRODUCT SPECIFICATION

Z86E04/E08

CMOS Z8® 8-BIT OTP MICROCONTROLLERS

FEATURES

- The Z86E04/E08 Devices Have the Following General Characteristics:

Part	ROM	RAM	Speed
Z86E04	1 Kbyte	124	8 MHz
Z86E08	2 Kbyte	124	12 MHz

- 18-Pin Package (DIP, SOIC)
- Clock Speeds up to 8 MHz (E04), 12 MHz (E08)
- Low Noise Programmable
- ROM Protect Programmable
- 4.5V to 5.5V Operating Range
- Low Power Consumption: 50 mW (Typical)
- Fast Instruction Pointer: 1 µs @ 12 MHz (E08), 1.25 µs @ 8 MHz (E04)
- Two Standby Modes: STOP and HALT
- 14 Input/Output Lines
- All Digital Inputs, CMOS Levels, Schmitt-Triggered.
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Six Different Sources.
- Programmable Watch-Dog Timer
- Power-On Reset Timer
- Two On-Board Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.
- Programmable Interrupt Polarity
- Auto Latches

GENERAL DESCRIPTION

The Z86E04/E08 8-bit One-Time-Programmable (OTP) Microcontrollers (MCUs) are members of Zilog's single-chip Z8® microcontroller family with 1K/2K bytes of one-time PROM, respectively. Offered in 18-pin DIP or SOIC style packages, and manufactured in CMOS technology, the Z86E04/E08 allow easy software development, debug and prototyping, and are ideal for small production runs not economically desirable with a masked ROM version.

The Z86E04/E08 are characterized by a flexible I/O scheme, an efficient register, and address space structure, in addition to a number of ancillary features useful in many consumer, industrial, and commercial applications.

For applications demanding powerful I/O capabilities, the Z86E04/E08 provides 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals. There are two basic address spaces available to support this configuration: program memory and 124 bytes of general-purpose registers.

The Z86E04/E08 each offer programmable EPROM Protect and programmable Low Noise. When the part is programmed for EPROM Protect, the Low Noise feature will automatically be enabled. When programmed for Low Noise, the EPROM Protect feature is optional.

GENERAL DESCRIPTION (Continued)

To unburden the system from coping with real-time tasks, such as counting/timing and I/O data communications, the Z86E04/E08 offers two on-chip counter/timers with a large number of user selectable modes. Included, are two on-board comparators that can process analog signals with a common reference voltage (Figures 1 and 2).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

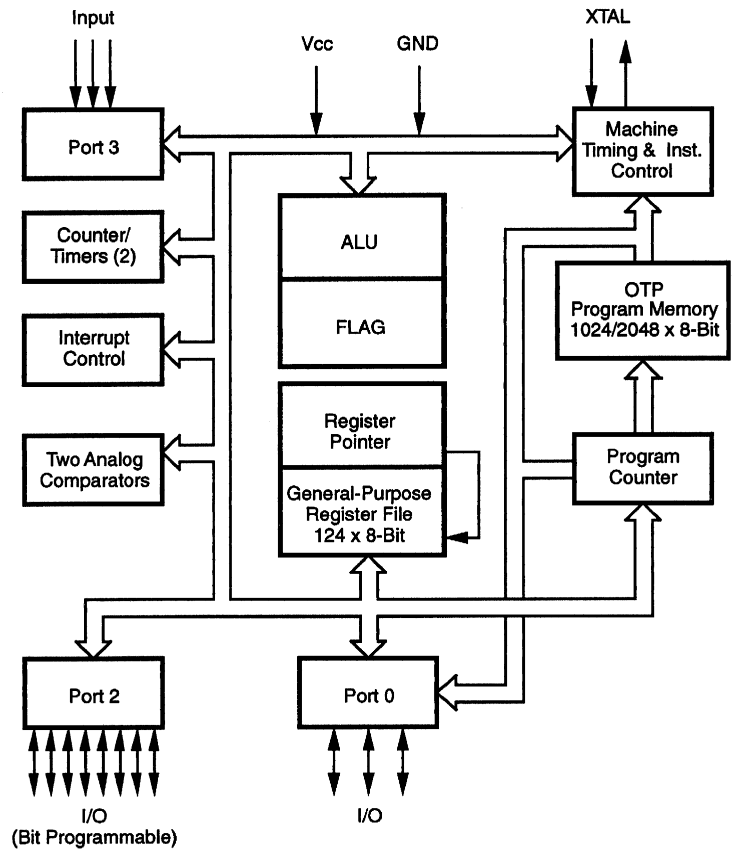


Figure 1. Z86E04/E08 Functional Block Diagram

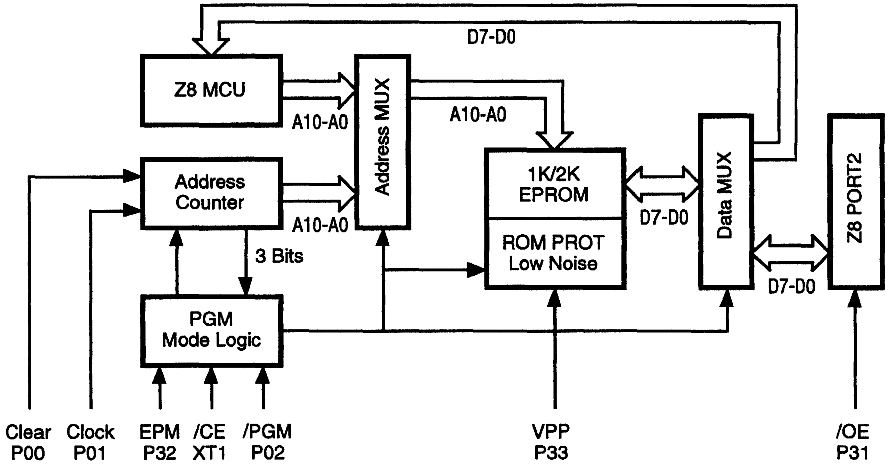


Figure 2. Z86E04/E08 EPROM Programming Mode Block Diagram

PIN DESCRIPTION

Table 1. 18-Pin DIP/SOIC Pin Identification

EPROM Programming Mode Pin #	Symbol	Function	Direction
1-4	D7-D4	Data 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	N/C	No Connection	
7	/CE	Chip Enable	Input
8	/OE	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	V_{PP}	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	/PGM	Prog Mode	Input
14	GND	Ground	
15-18	D3-D0	Data 0,1, 2, 3	In/Output

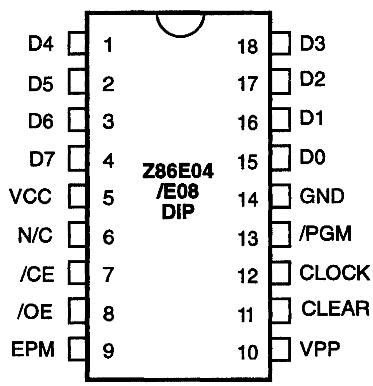


Figure 3. 18-Pin DIP/SOIC Pin Configuration EPROM Programming Mode

PIN DESCRIPTION

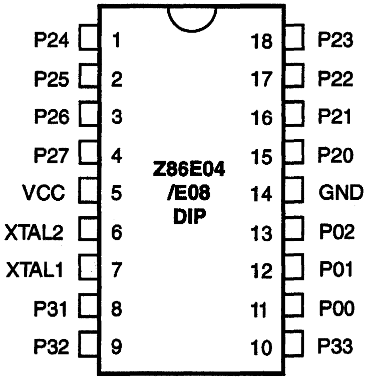


Figure 4. 18-Pin DIP Pin Configuration Standard Mode

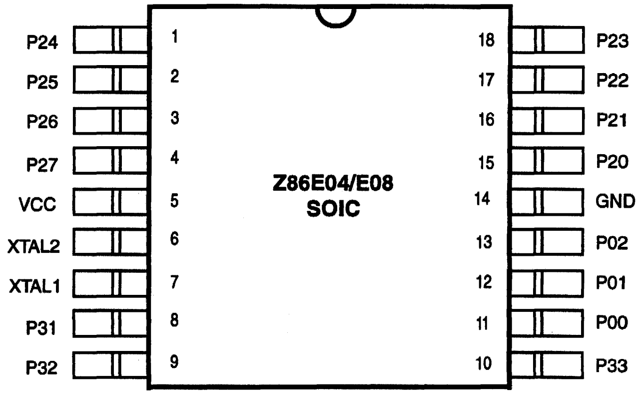


Figure 5. 18-Pin SOIC Pin Configuration Standard Mode

Table 2. 18-Pin DIP/SOIC Pin Identification

Standard Mode Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4,5,6,7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0,1,2,3	In/Output

PIN FUNCTIONS

OTP Programming Mode

D7-D0 *Data Bus.* Data can be read from, or written to the EPROM through this data bus.

V_{CC} *Power Supply.* It is 5V during EPROM Read Mode and 6V during the other modes (Program, Program Verify, etc.).

/CE *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

/OE *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} *Program Voltage.* This pin supplies the program voltage.

Clear *Clear* (active High). This pin resets the internal address counter at the High Level.

Clock *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock cycle.

/PGM *Program Mode* (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise*** surges above V_{cc} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by ***excessive noise*** surges on the V_{pp}, /CE, /EPM, /OE pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin.

4

Z86E04/E08 STANDARD MODE

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (8 MHz or 12 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02-P00. Port 0 is a 3-bit bi-directional, Schmitt-triggered CMOS compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 6).

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

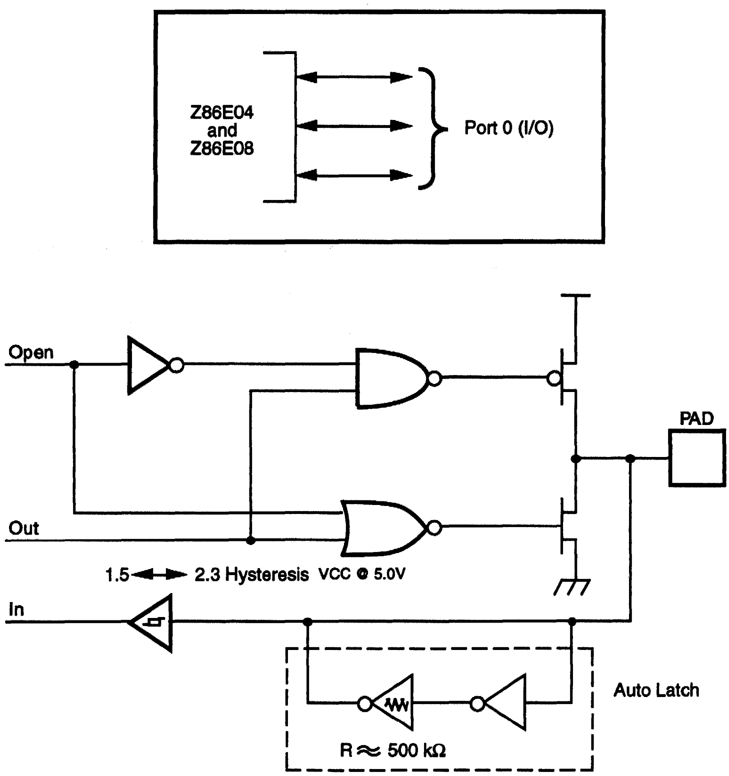


Figure 6. Port 0 Configuration

Port 2, P27-P20. Port 2 is an 8-bit, bit programmable, bi-directional, Schmitt-triggered CMOS compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 7).

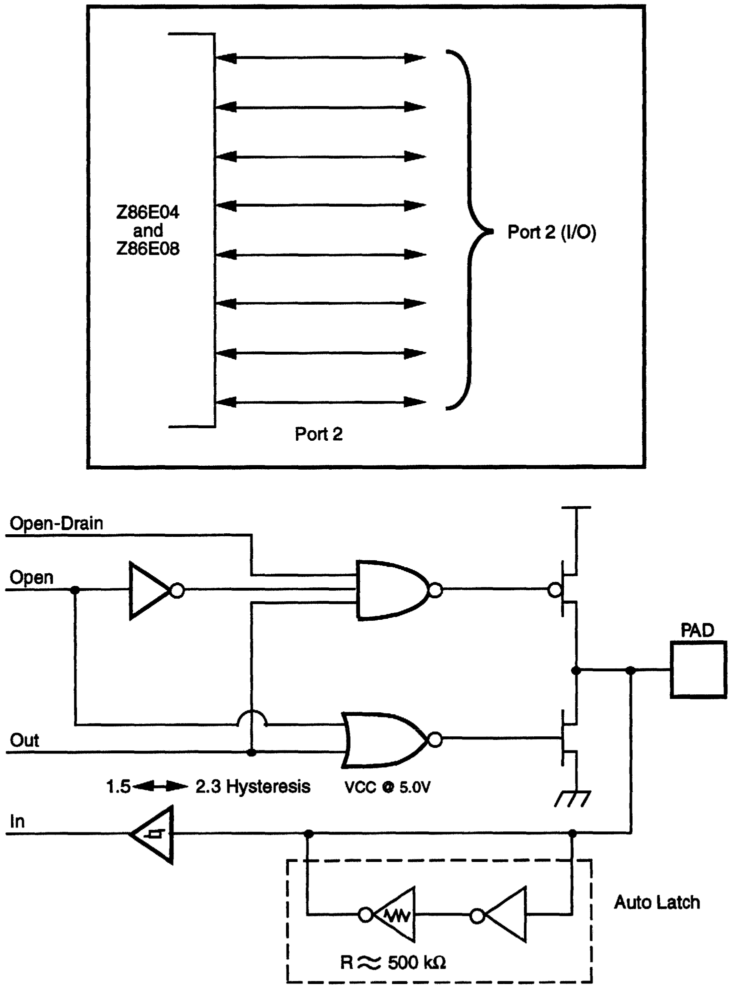
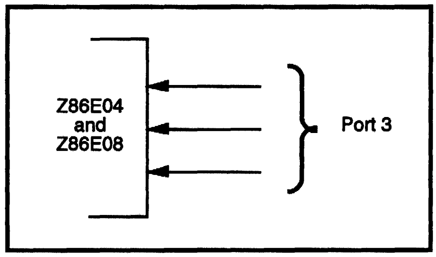


Figure 7. Port 2 Configuration

Z86E04/E08 Standard Mode (Continued)

Port 3, P33-P31. Port 3 is a 3-bit, CMOS compatible port with three fixed input (P32-P30) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN} - Figure 8).



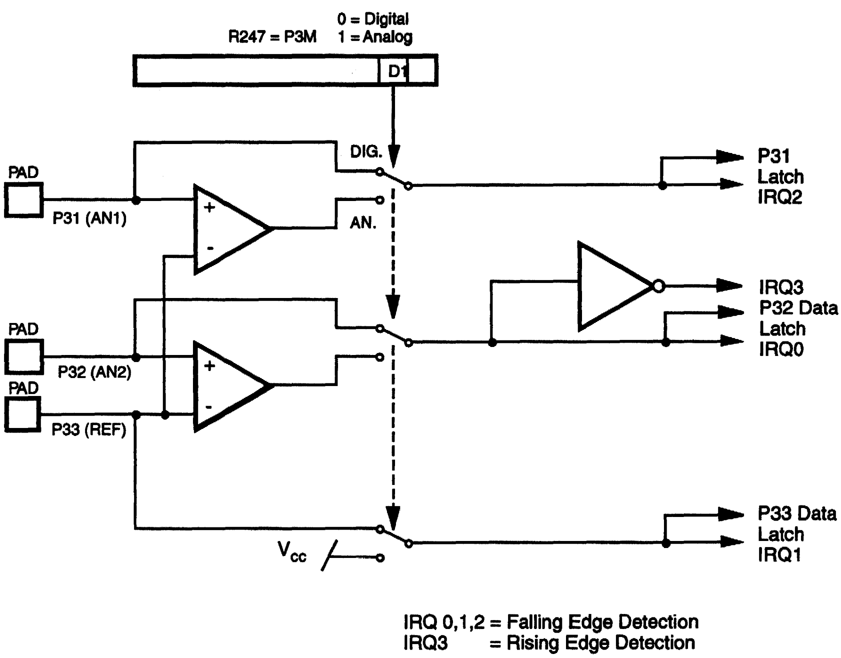


Figure 8. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31 and P32, for interface flexibility. The comparators reference voltage P3 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In analog mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP mode. The common voltage range is 0-4 V when the V_{CC} is 5.0 V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z86E04/E08 devices to enhance the standard Z8® core architecture to provide the user with increased design flexibility.

RESET. This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 9). The Z86E04/E08 control registers' reset value is shown in Table 3.

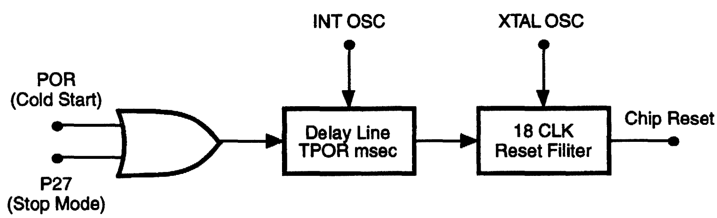


Figure 9. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power bad to power good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

FUNCTIONAL DESCRIPTION (Continued)

Table 3. Z86E04/E08 Control Registers

Addr.	Reg.	D7	D6	D5	D4	D3	D2	D1	D0	Comments
		Reset Condition								
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
FB	IMR	0	U	U	U	U	U	U	U	
FC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0	0	
FF	SPL	U	U	U	U	U	U	U	U	

Note:
* Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86E04/E08 addresses up to 1K/2K bytes of internal program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-1024/2048 are on-chip one-time programmable ROM.

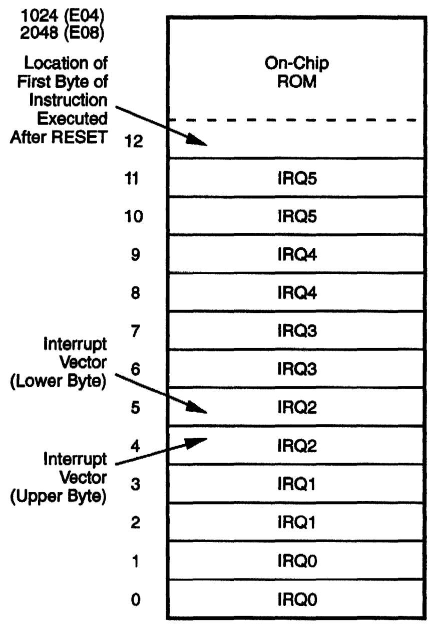


Figure 10. Program Memory Map

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0-R3, R4-R127 and R241-R255, respectively (Figure 11). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8. The Z86E04/E08 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 12) addresses the starting location of the active working-register group.

Location		Identifiers
255	Stack Pointer (Bits 7-0)	SPL
254	General-Purpose Register	GPR
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	HMH
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter1	T1
241	Timer Mode	TMR
128	Not Implemented	
127 4	General-Purpose Registers	
3	Port 3	P3
2	Port 2	P2
1	Reserved	P1
0	Port 0	P0

Figure 11. Register File

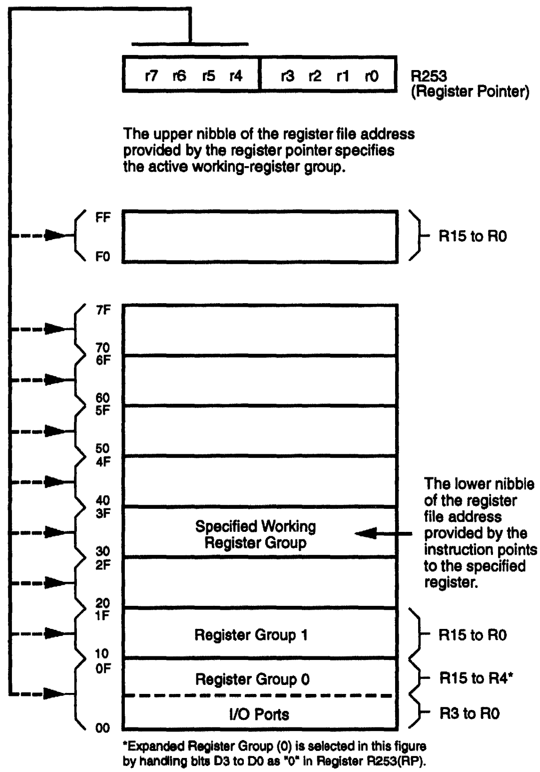


Figure 12. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)

Stack Pointer. The Z86E04/E08 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 13).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

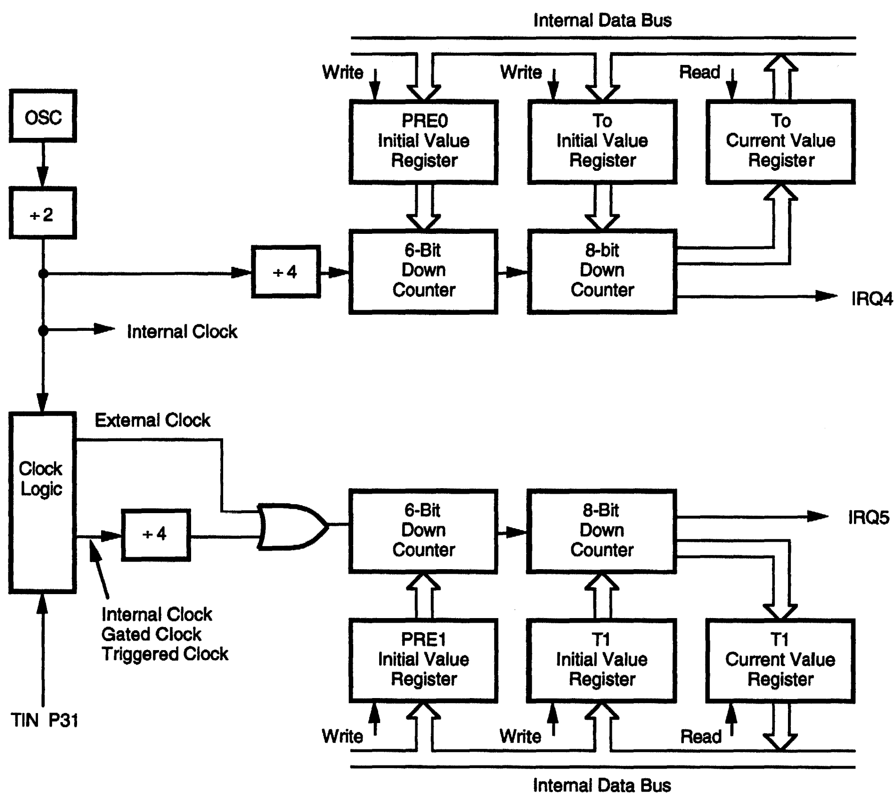


Figure 13. Counter/Timers Block Diagram

Interrupts. The Z86E04/E08 has six interrupts from five different sources. These interrupts are maskable and prioritized (Figure 14). The sources are divided as follows: the rising edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86E04/E08 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the Z86CCP00ZEM emulator.

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

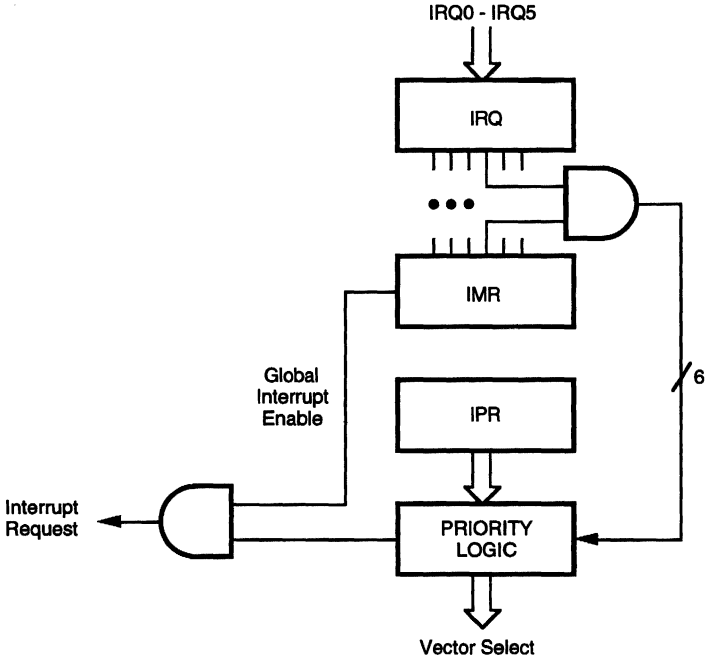


Figure 14. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86E04/E08 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, 8 MHz or 12 MHz max, with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 15). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.

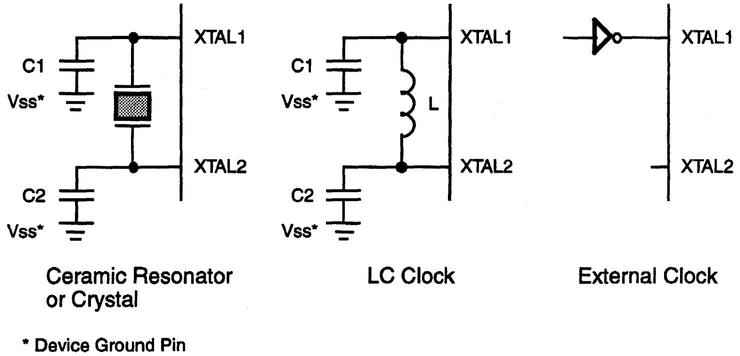


Figure 15. Oscillator Configuration

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

X = Dependent on user's application.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, i.e.:

```
FF   NOP    ; clear the pipeline
6F   STOP   ; enter STOP mode
or
FF   NOP    ; clear the pipeline
7F   HALT   ; enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the Z86E04 resets itself, The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

WDT = 5F (Hex)

Opcode WDT (5FH). The first time opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 XTAL clock cycles.

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Auto Reset Voltage (V_{RST}). The Z86E04/E08 has an auto-reset built-in. The auto-reset circuit resets the Z86E04/E08 when it detects the V_{CC} below V_{RST}. Figure 16 shows the Auto Reset Voltage vs temperature. The Z86E04/E08 does not function from V_{RST} to below 4.5V. Upon power-up of the device, the V_{CC} rise time must reach 4.5V before the T_{POR} expires so that program execution begins with the V_{CC} in the range 4.5V to 5.5V.

If the V_{CC} drops below 4.5V while the device is in operation, the device must be powered down and then re-powered up again.

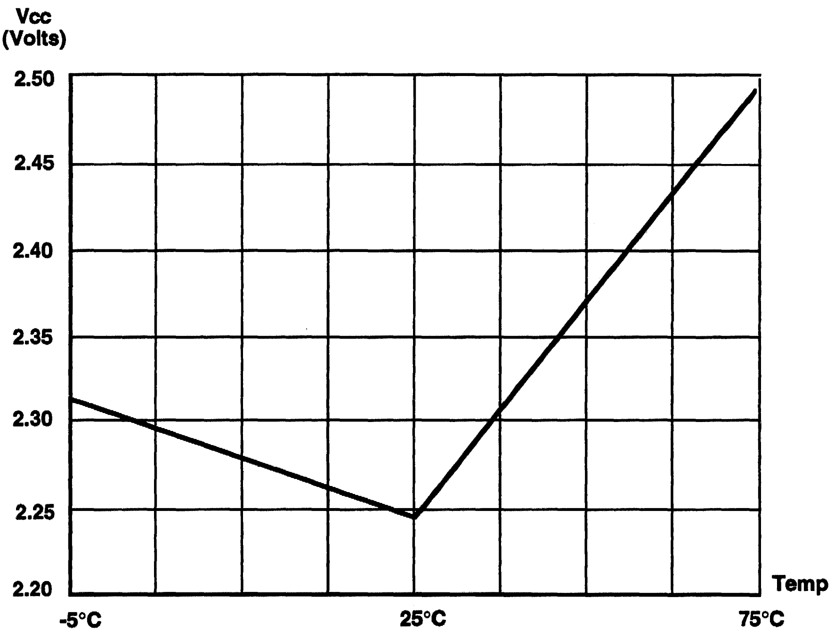


Figure 16. Typical Auto Reset Voltage (V_{RST}) vs Temperature

FUNCTIONAL DESCRIPTION (Continued)

Low EMI Emission

The Z86E04/E08 can be programmed to operate in a low EMI emission mode by means of an EPROM programmable bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT mode.
- All drivers slew rates reduced to 10 ns (typical).
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Z86E04/E08 offers programmable ROM Protect and programmable Low Noise features. When programmed for Low Noise, the ROM Protect feature is optional.

In addition to V_{DD} and GND (V_{SS}), the Z86E04/E08 changes all its pin functions in the EPROM mode. XTAL2 has no function, XTAL1 functions as /CE, P31 functions as /OE, P32 functions as EPM, P33 functions as V_{PP}, and P02 functions as /PGM.

ROM Protect. ROM Protect fully protects the Z86E04/E08 ROM code from being read externally. When ROM Protect is selected, the Z86E04/E08 will disable the instructions LDC and LDCI (Z86E04/E08 and Z86C04/C08 do not support the instructions of LDE and LDEI). When the device is programmed for ROM Protect, the Low Noise feature will automatically be enabled.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM and CE pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP mode. The V_{PP} requires both a diode and a 100 pF capacitor.

User Modes. Table 5 shows the programming voltage of each mode of Z86E04/E08.

Table 5. OTP Programming Table

Programming Modes	Device	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ1	All	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V
EPROM READ2	All	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V
PROGRAM	All	V_H	X	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.0V
PROGRAM VERIFY	All	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
EPROM PROTECT	All	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
LOW NOISE SELECT	E04/E08	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	6.0V

Notes:
V_H = 12.5V ±0.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.

Internal Address Counter. The address of Z86E04/E08 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 17 shows the setup time of the serial address input.

Programming Waveform. Figures 18, 19 and 20 show the programming waveforms of each mode. Table 6 shows the timing of programming waveforms.

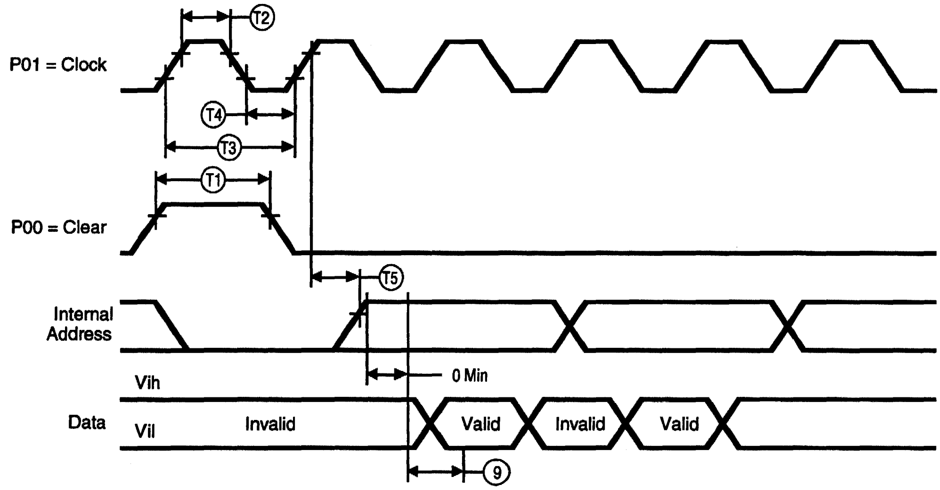
Programming Algorithm. Figure 21 shows the flow chart of the Z86E04/E08 programming algorithm.

Table 6. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

4

FUNCTIONAL DESCRIPTION (Continued)



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	30 ns Min
T3 Input Clock Period	70 ns Min
T4 Input Clock Low	30 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max

Figure 17. Z86E04/E08 Address Counter Waveform

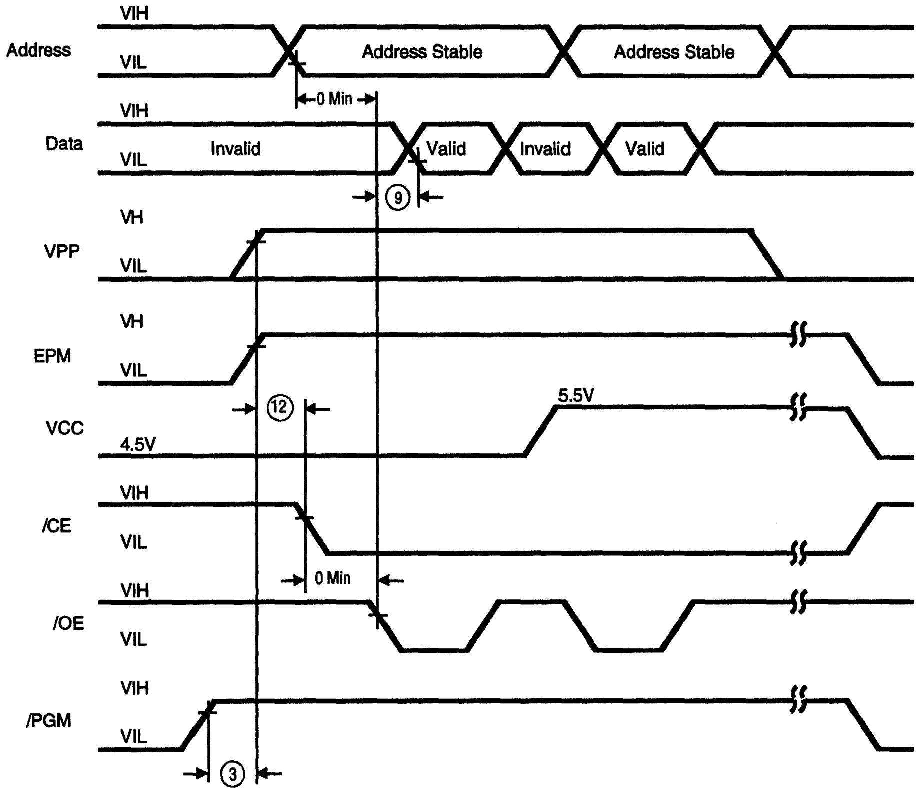


Figure 18. Z86E04/E08 Programming Waveform (EPROM Read)

FUNCTIONAL DESCRIPTION (Continued)

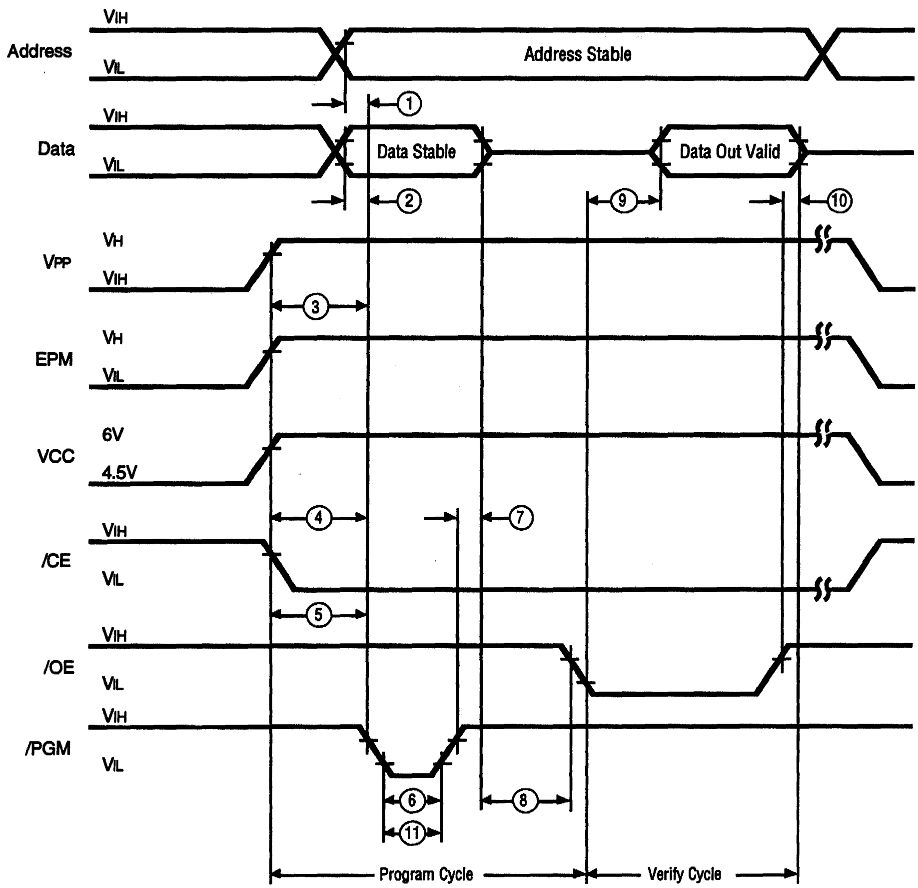


Figure 19. Z86E04/E08 Programming Waveform (Program and Verify)

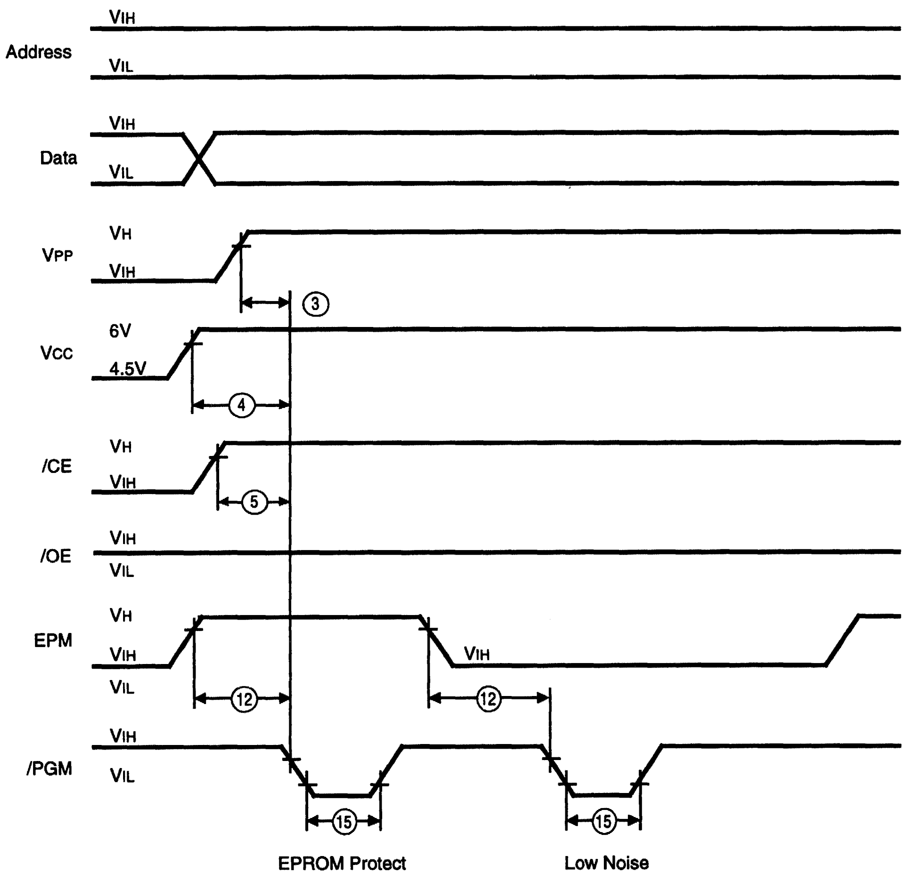


Figure 20. Z86E04/E08 Programming Waveform (EPROM Protect and Low EMI Program)

4

FUNCTIONAL DESCRIPTION (Continued)

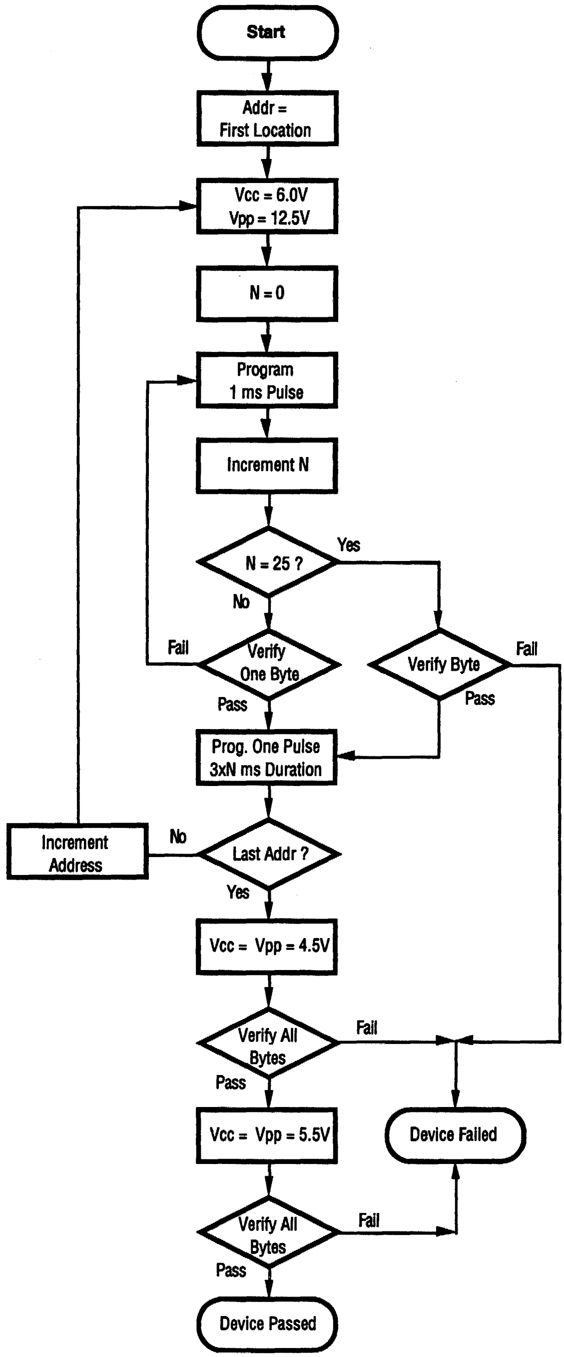


Figure 21. Z86E04/E08 Programming Algorithm

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [\, I_{DD} - (\text{sum of } I_{OH})\,] + \text{sum of } [\,(V_{DD} - V_{OH}) \times I_{OH}\,] + \text{sum of } (V_{OL} \times I_{OL})$$

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+12	V	[1]
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on Pins 7, 8, 9, 10 with Respect to V_{SS}	–0.6	V_{DD}+1	V	[2]
Total Power Dissipation		462	mW	
Maximum Current out of V_{SS}		84	mA	
Maximum Current into V_{DD}		84	mA	
Maximum Current into an Input Pin	–600	+600	µA	[3]
Maximum Current into an Open-Drain Pin	–600	+600	µA	[4]
Maximum Output Current Sinked by Any I/O Pin		12	mA	
Maximum Output Current Sourced by Any I/O Pin		12	mA	
Total Maximum Output Current Sinked by Port 2		70	mA	
Total Maximum Output Current Sourced by Port 2		70	mA	

Notes:
[1] This applies to all pins except where otherwise noted. Maximum current into pin must be ±600 µA.
[2] There is no input protection diode from pin to V_{DD} (not applicable to EPROM Mode).
[3] This excludes Pin 6 and Pin 7.
[4] Device pin is not at an output Low state.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 22).

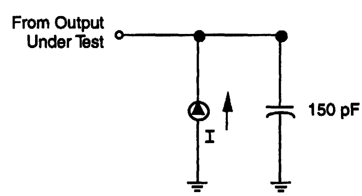


Figure 22. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.8 V_{CC}	V_{CC}+0.3	2.4	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.6		Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	2.3	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.1	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.7	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.2	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		3.9	V	I_{OH} = –2.0 mA	[3]
		5.5V	V_{CC}–0.4		5.4	V	I_{OH} = –2.0 mA	[3]
V_{OH}	Output Low Voltage	4.5V	V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	
V_{OL}	Output Low Voltage	4.5V		0.4		V	Low Noise @ I_{OL} = +1 mA	
		5.5V		0.4		V	Low Noise @ I_{OL} = +1 mA	
V_{OL1}	Output Low Voltage	4.5V		0.8	0.2	V	I_{OL} = +4.0 mA	[3]
		5.5V		0.4	0.2	V	I_{OL} = +4.0 mA	[3]
V_{OL2}	Output Low Voltage	4.5V		TBD	0.7	V	I_{OL} = +12 mA, 3 Pin Max	[3]
		5.5V		0.8	0.5	V	I_{OL} = +12 mA, 3 Pin Max	[3]
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		10	6	mV		
		5.5V		25	7	mV		
V_{RST}	Auto Reset Voltage		1.55	2.7	2.4	V		
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Input Common Mode Voltage Range		0	V_{CC}–1.0		V		

Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC}	Supply Current (Standard Mode)	4.5V		4.0	2.2	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		7.0	5.0	mA	All Output and I/O Pins Floating @ 2 MHz
		4.5V		9.0	4.5	mA	All Output and I/O Pins Floating @ 8 MHz
		5.5V		11.0	8.3	mA	All Output and I/O Pins Floating @ 8 MHz
		4.5V		10	6.1	mA	All Output and I/O Pins Floating @ 12 MHz (E08)
		5.5V		15	10.8	mA	All Output and I/O Pins Floating @ 12 MHz (E08)
I_{CC1}	Standby Current (Standard Mode)	4.5V		2.5	0.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		4.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz
		4.5V		4.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz
		5.5V		5.0	2.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz
		4.5V		5.0	1.3	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz (E08)
		5.5V		7.0	2.3	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz (E08)
I_{CC}	Supply Current (Low Noise Mode)	4.5V		4.0	2.2	mA	All Output and I/O Pins Floating @ 1 MHz
		5.5V		7.0	4.2	mA	All Output and I/O Pins Floating @ 1 MHz
		4.5V		6.0	2.9	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		9.0	5.5	mA	All Output and I/O Pins Floating @ 2 MHz
		4.5V		8.0	4.4	mA	All Output and I/O Pins Floating @ 4 MHz
		5.5V		11.0	7.9	mA	All Output and I/O Pins Floating @ 4 MHz

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		1.2	0.4	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz
		5.5V		1.6	0.9	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz
		4.5V		1.5	0.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		1.9	1	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz
		4.5V		2.0	0.8	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz
		5.5V		2.4	1.3	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz
I_{CC2}	Standby Current	4.5V		10	1.0	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running
		5.5V		10	1.0	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running
I_{ALL}	Auto Latch Low Current	4.5V		10	6.0	µA	0V < V_{IN} < V_{CC}
		5.5V		15	11.5	µA	0V < V_{IN} < V_{CC}
I_{ALH}	Auto Latch High Current	4.5V		-7.0	–3.3	µA	0V < V_{IN} < V_{CC}
		5.5V		-7.0	-6.5	µA	0V < V_{IN} < V_{CC}

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3	5.0	mA	8 MHz
Crystal or Resonator	3.5	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND

AC ELECTRICAL CHARACTERISTICS

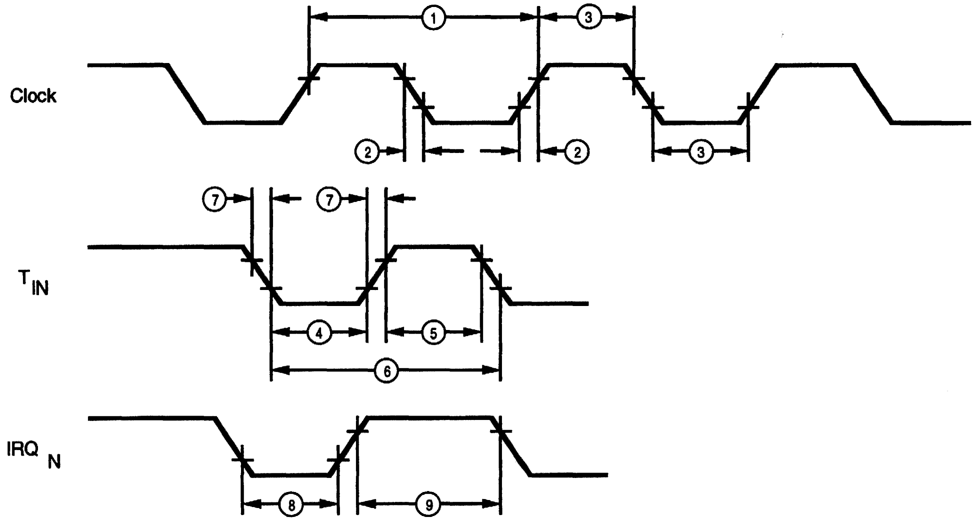


Figure 23. Electrical Timing Diagram

4

AC ELECTRICAL CHARACTERISTICS
Low Noise Mode

				T_A = 0°C to +70°C					
				1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	1000	DC	250	DC	ns	[1]
			5.5V	1000	DC	250	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	[1]
			5.5V		25		25	ns	
3	TwC	Input Clock Width	4.5V	500		125		ns	[1]
			5.5V	500		125		ns	[1]
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			[1]
			5.5V	4TpC		4TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	4.5V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	4.5V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	4.5V		15		15	ms	[1]
			5.5V		10		10	ms	[1]
11	TPOR	Power-On Reset Time	4.5V	15		10		ms	[1]
			5.5V	15		10		ms	[1]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31)

AC ELECTRICAL CHARACTERISTICS
Standard Mode, Standard Temperature

				T_A = 0°C to +70°C					
				8 MHz (E04)		12 MHz (E08)			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	[1]
			5.5V	125	DC	83	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	[1]
			5.5V		25		15	ns	
3	TwC	Input Clock Width	4.5V	62		41		ns	[1]
			5.5V	62		41		ns	[1]
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1]
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			[1]
			5.5V	8TpC		8TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	4.5V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	4.5V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	4.5V		15		15	ms	[1]
			5.5V		10		10	ms	[1]
11	TPOR	Power-On Reset Timer	4.5V		60		60	ms	[1]
			5.5V		45		45	ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31)

Z8 CONTROL REGISTERS

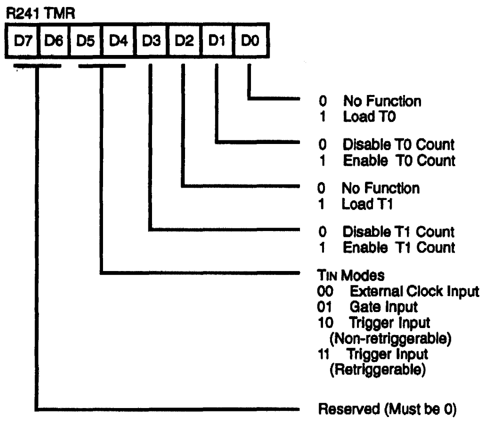


Figure 24. Timer Mode Register ($F1_H$: Read/Write)

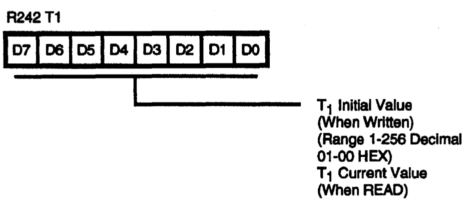


Figure 25. Counter Timer 1 Register ($F2_H$: Read/Write)

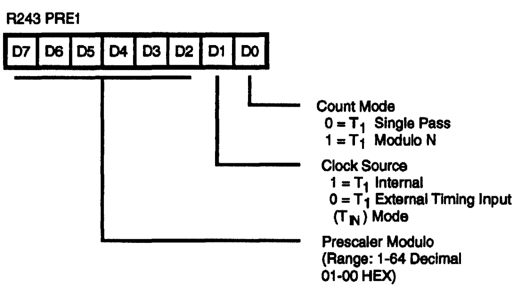


Figure 26. Prescaler 1 Register ($F3_H$: Write Only)

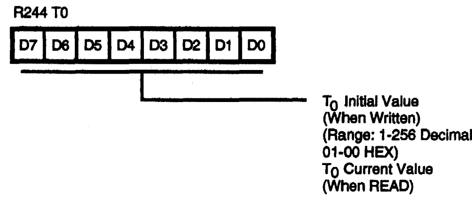


Figure 27. Counter/Timer 0 Register ($F4_H$: Read/Write)

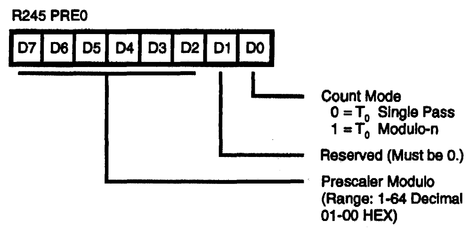


Figure 28. Prescaler 0 Register ($F5_H$: Write Only)

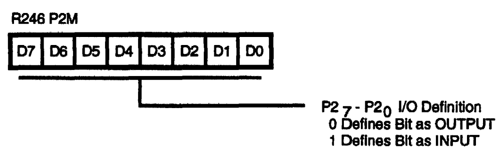


Figure 29. Port 2 Mode Register ($F6_H$: Write Only)

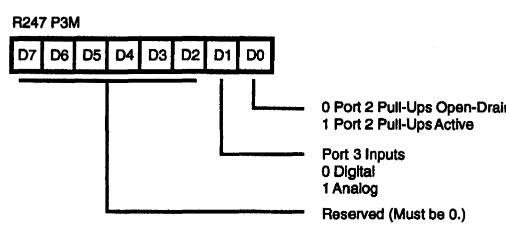


Figure 30. Port 3 Mode Register ($F7_H$: Write Only)

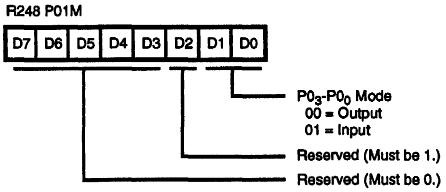


Figure 31. Port 0 and 1 Mode Register (F8$_H$: Write Only)

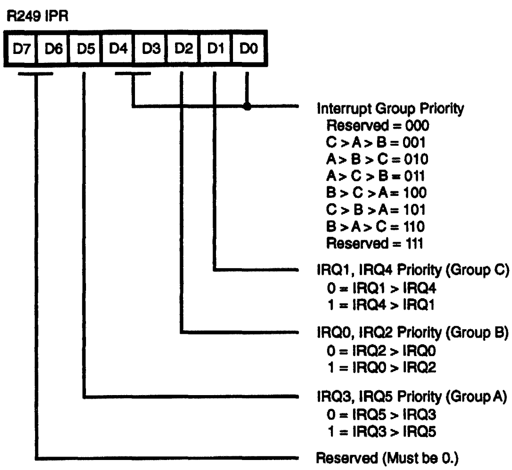


Figure 32. Interrupt Priority Register (F9$_H$: Write Only)

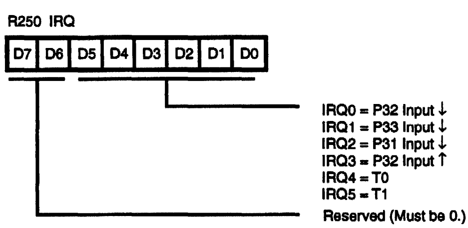


Figure 33. Interrupt Request Register (FA$_H$: Read/Write)

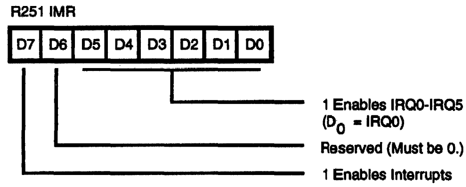


Figure 34. Interrupt Mask Register (FB$_H$: Read/Write)

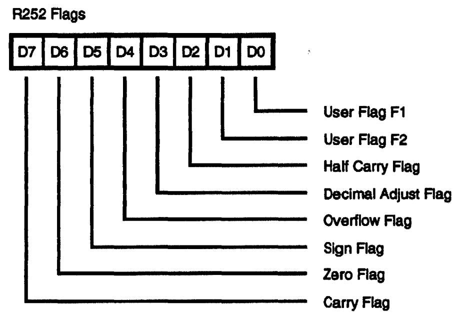


Figure 35. Flag Register (FC$_H$: Read/Write)

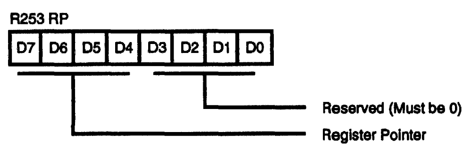


Figure 36. Register Pointer (FD$_H$: Read/Write)

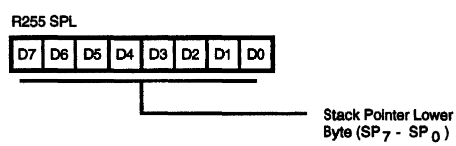


Figure 37. Stack Pointer (FF$_H$: Read/Write)

4

OPERATING MODES

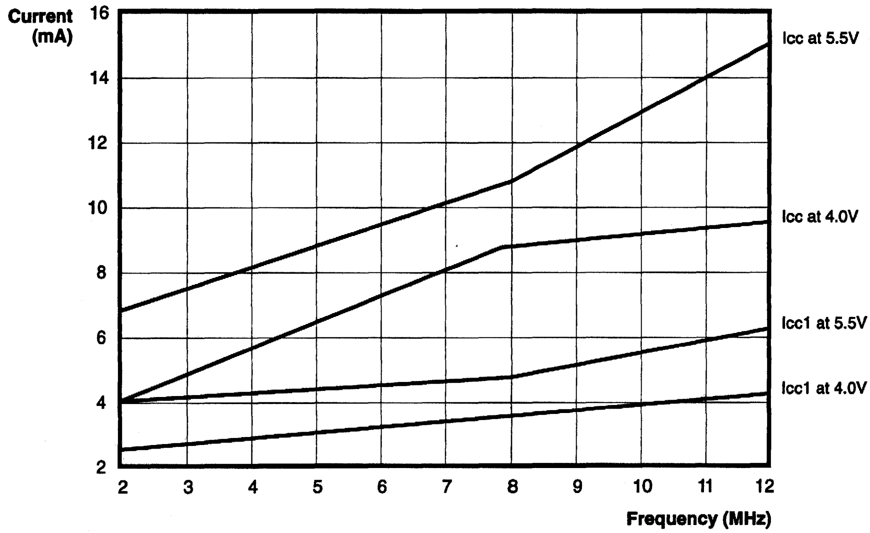


Figure 38. Maximum I_{CC} and I_{CC1} vs Frequency in Standard Mode

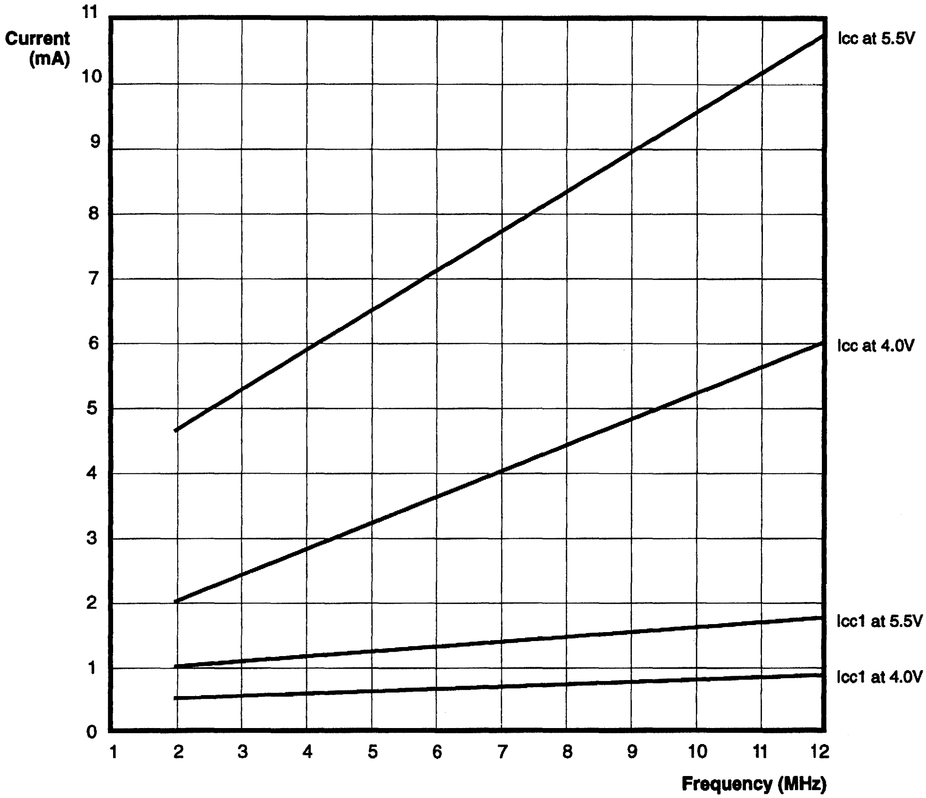


Figure 39. Typical I_{CC} and I_{CC1} vs Frequency in Standard Mode

4

OPERATING MODES (Continued)

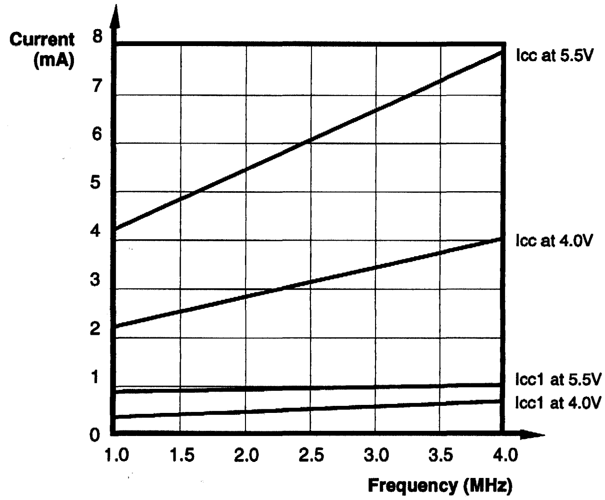


Figure 40. Typical I_{CC} and I_{CC1} vs Frequency in Low EMI Mode

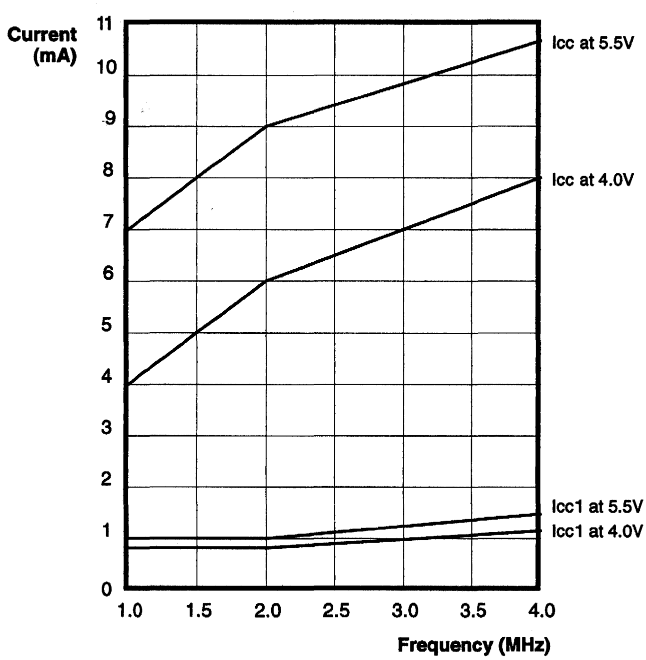


Figure 41. Maximum I_{CC} and I_{CC1} vs Frequency in Low EMI Mode

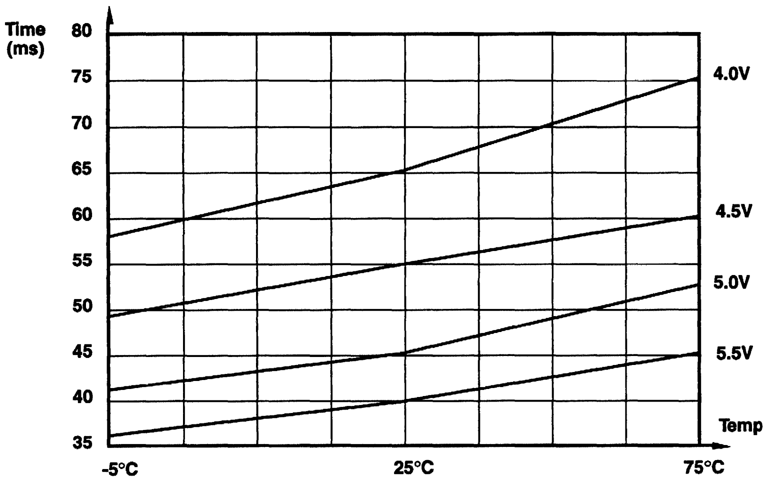


Figure 42. Typical POR Time Out Period vs Temperature

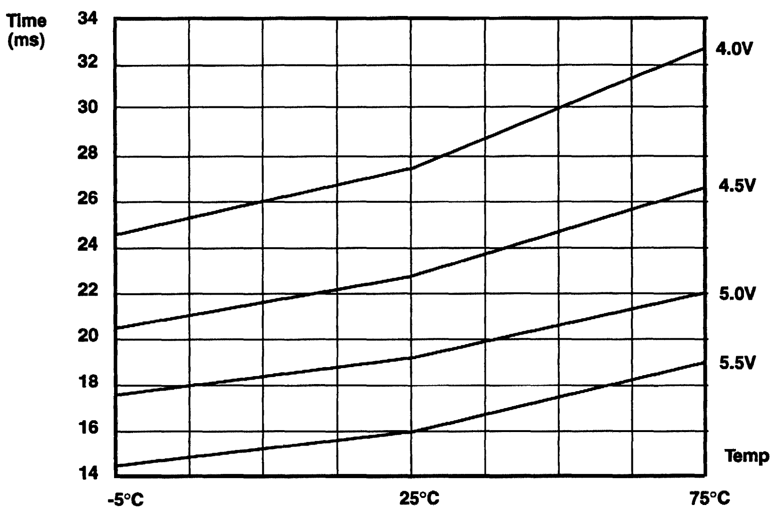


Figure 43. Typical WDT Time Out Period vs Temperature

4

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag
Affected flags are indicated by:	
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

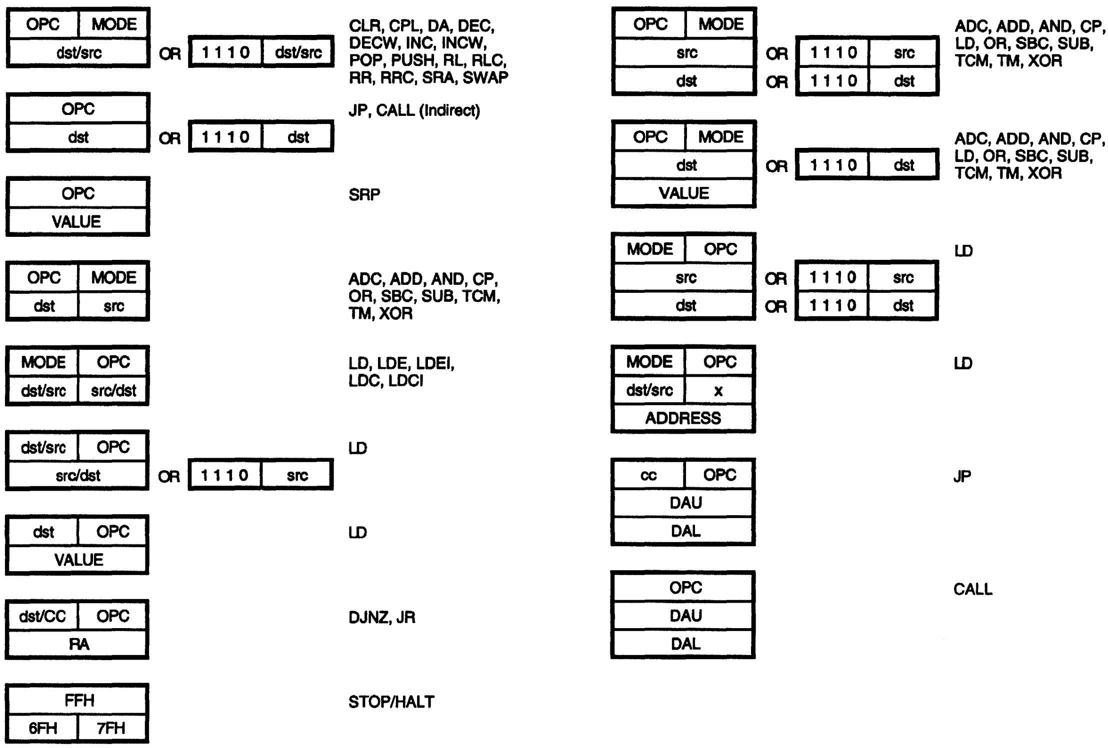
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	—	Always true	—
0111	C	Carry	C=1
1111	NC	No Carry	C=0
0110	Z	Zero	Z=1
1110	NZ	Not zero	Z=0
1101	PL	Plus	S=0
0101	MI	Minus	S=1
0100	OV	Overflow	V=1
1100	NOV	No overflow	V=0
0110	EQ	Equal	Z=1
1110	NE	Not equal	Z=0
1001	GE	Greater than or equal	(S XOR V)=0
0001	LT	Less than	(S XOR V)=1
1010	GT	Greater than	[Z OR (S XOR V)]=0
0010	LE	Less than or equal	[Z OR (S XOR V)]=1
1111	UGE	Unsigned greater than or equal	C=0
0111	ULT	Unsigned less than	C=1
1011	UGT	Unsigned greater than	(C = 0 AND Z=0)=1
0011	ULE	Unsigned less than or equal	(C OR Z)=1
0000	F	Never true (Always False)	—

4

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst(7)

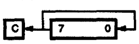
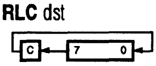
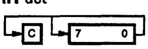
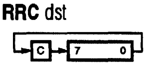
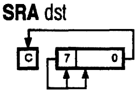
refers to bit 7 of the destination operand.

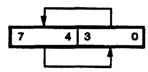
INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst + src +C	†	1[ ]	* * * * 0 *
ADD dst, src dst←dst + src	†	0[ ]	* * * * 0 *
AND dst, src dst←dst AND src	†	5[ ]	- * * 0 - -
CALL dst SP←SP − 2 @SP←PC, PC←dst	DA IRR	D6 D4	- - - - - -
CCF C←NOT C		EF	* - - - - -
CLR dst dst←0	R IR	B0 B1	- - - - - -
COM dst dst←NOT dst	R IR	60 61	- * * 0 - -
CP dst, src dst − src	†	A[ ]	* * * * - -
DA dst dst←DA dst	R IR	40 41	* * * X - -
DEC dst dst←dst − 1	R IR	00 01	- * * * - -
DECW dst dst←dst − 1	RR IR	80 81	- * * * - -
DI IMR(7)←0		8F	- - - - - -
DJNZr, dst r←r − 1 if r ≠ 0 PC←PC + dst Range: +127, −128	RA	rA r = 0 - F	- - - - - -
EI IMR(7)←1		9F	- - - - - -
HALT		7F	- - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
INC dst dst←dst + 1	r R IR	rE r = 0 − F 20 21	- * * * - -
INCW dst dst←dst + 1	RR IR	A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1		BF	* * * * * *
JP cc, dst if cc is true, PC←dst	DA IRR	cD c = 0 − F 30	- - - - - -
JR cc, dst if cc is true, PC←PC + dst Range: +127, −128	RA	cB c = 0 − F	- - - - - -
LD dst, src dst←src	r Im r R R r r X X r r Ir Ir r R R R IR R IM IR IM IR R	rC r8 r9 r = 0 − F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst, src dst←src	r Irr	C2	- - - - - -
LDCI dst, src dst←src r←r + 1; rr←rr + 1	Ir Irr	C3	- - - - - -

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
NOP		FF	- - - - - - -
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -
POP dst dst←@SP; SP←SP + 1	R IR	50 51	- - - - - - -
PUSH src SP←SP – 1; @SP←src	R IR	70 71	- - - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP + 2		AF	- - - - - - -
RL dst 	R IR	90 91	* * * * - -
RLC dst 	R IR	10 11	* * * * - -
RR dst 	R IR	E0 E1	* * * * - -
RRC dst 	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst__src__C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst 	R IR	D0 D1	* * * 0 - -
SRP dst RP←src	Im	31	- - - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
STOP		6F	1 - - - - -
SUB dst, src dst←dst—src	†	2[ ]	* * * * 1 *
SWAP dst 	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
WDH		4F	- - - - - - -
WDT		5F	- X X X - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

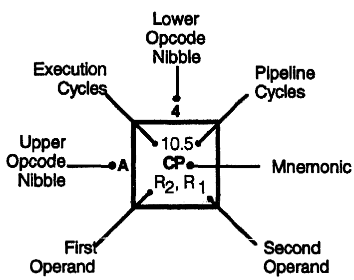
Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) (columns) / **Upper Nibble (Hex)** (rows)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	4.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	5.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1							↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1							↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**

Bytes per Instruction: columns 0–1: 2; columns 2–7: 3; columns 8–C: 2; column D: 3; columns E–F: 1



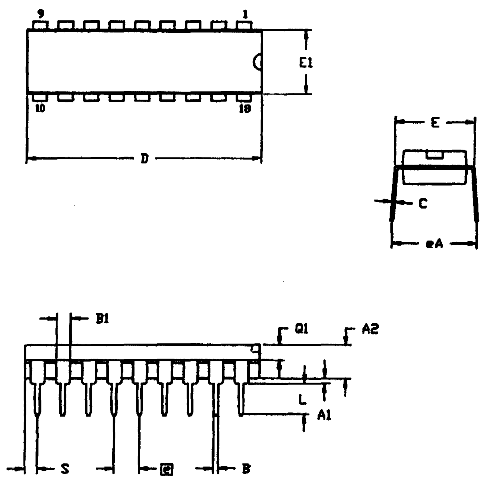
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_1 = Dst address
R_2 or r_2 = Src address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

* 2-byte instruction appears as a 3-byte instruction

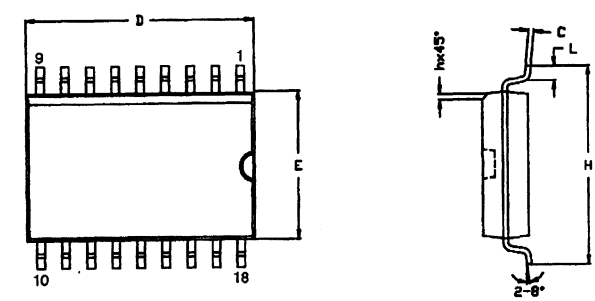
PACKAGE INFORMATION

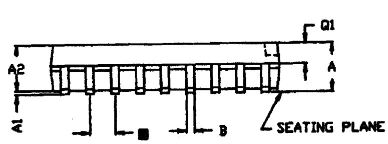


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86E04 (8 MHz)

Standard Temperature	
18-Pin DIP	18-Pin SOIC
Z86E0408PSC	Z86E0408SSC

Z86E08 (12 MHz)

Standard Temperature	
18-Pin DIP	18-Pin SOIC
Z86E0812PSC	Z86E0812SSC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
S = SOIC

Preferred Temperature
S = 0°C to +70°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86E04 08 P S C is a Z86E04, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 08 — Speed
- 86E04 — Product Number
- Z — Zilog Prefix

Z86C07

CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- Low Cost, 8-Bit CMOS MCU
- 2 Kbytes of ROM
- 124 Bytes of RAM
- 18-Pin Package (DIP, SOIC)
- 3.0 to 5.5 Volt Operating Range
- Low Power Consumption: 50 mW (typical)
- Low Voltage Protection
- ROM Protection
- Fast Instruction Pointer: 1 µs @ 12 MHz
- Two Standby Modes: STOP and HALT
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler.
- 14 Input/Output Lines
- Three Digital Inputs at CMOS Levels
- Eleven Digital Inputs at CMOS Levels; Schmitt-Triggered
- Extended Operating Range: –40°C to +105°C
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speeds: 8 and 12 MHz
- On-Board Power-On Reset Circuit
- Permanently Enabled Watch-Dog Timer
- Two Comparators with Programmable Interrupt Polarity.
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.

GENERAL DESCRIPTION

The Z86C07 Microcontroller Unit (MCU) is a member of the Z8® single-chip microcontroller family with 2 Kbytes of ROM and 124 bytes of general- purpose RAM. Offered in an 18-pin (DIP, SOIC) package style and manufactured in CMOS technology, Zilog's low cost, low power consumption Z86C07 offers all the outstanding features of the Z8 family architecture, including easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the Z86C07 provides 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals. The Z86C07 also features two on-board comparators that can process analog signals with a common reference voltage. There are two basic address spaces available to support this configuration: Program Memory, and 124 bytes of general-purpose registers.

The Z86C07 is characterized by a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer and industrial applications.

GENERAL DESCRIPTION (Continued)

To unburden the system from coping with real-time tasks, such as counting/timing and I/O data communications, the Z86C07 offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

With powerful peripheral features, such as on-board comparators, counter/timer(s) and permanently enabled Watch-Dog Timer (WDT), the Z86C07 meets the needs of a variety of sophisticated controller applications.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

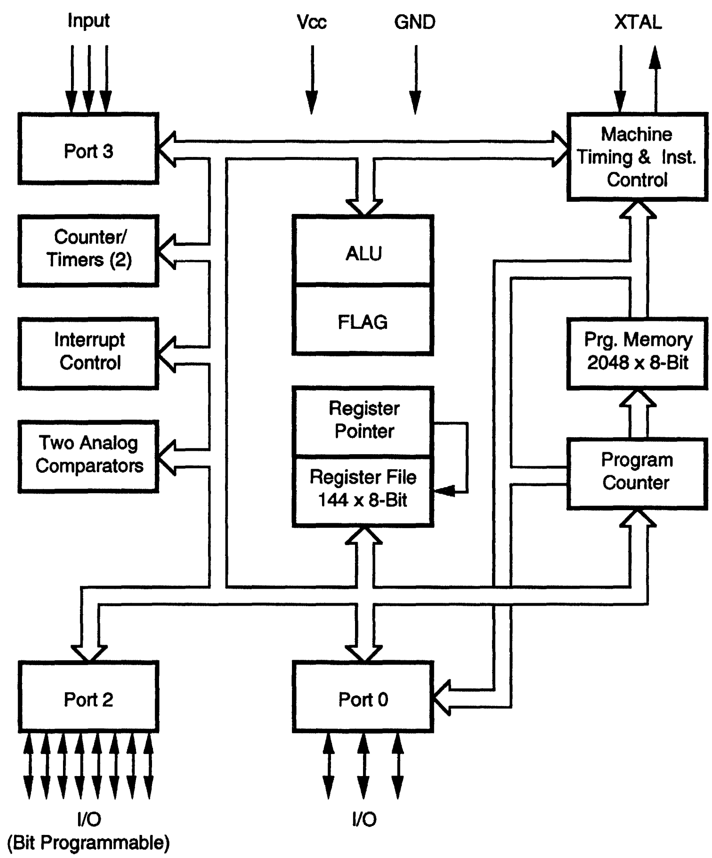


Figure 1. Z86C07 Functional Block Diagram

PIN DESCRIPTION

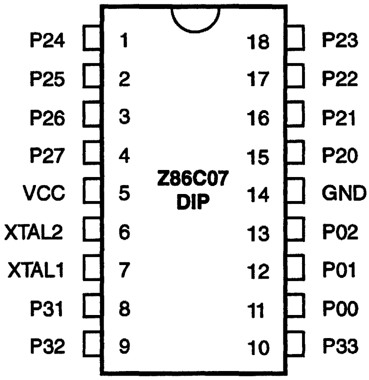


Figure 2. 18-Pin DIP Pin Configuration

Table 1. 18-Pin DIP and SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Input
7	XTAL1	Crystal Oscillator Clock	Output
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1 ,2, 3	In/Output

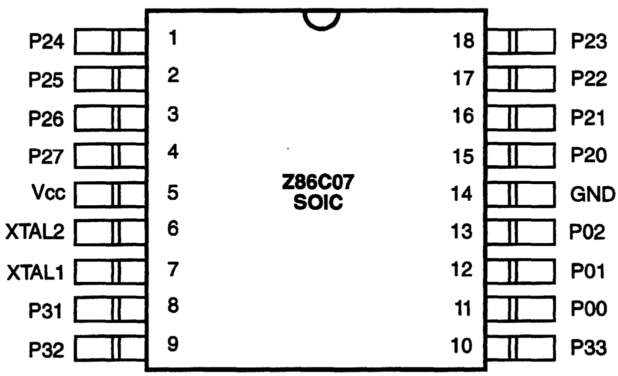
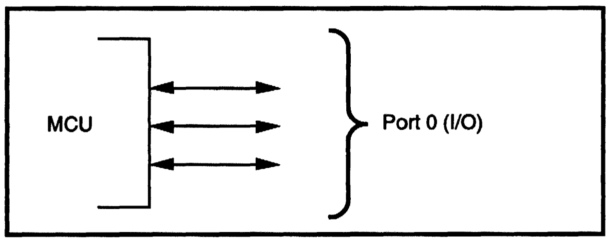


Figure 3. 18-Pin SOIC Pin Configuration

PIN FUNCTIONS

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (12 MHz max) to the on-chip clock oscillator and buffer.

Port 0 (P02-P00). Port 0 is a 3-bit I/O, nibble programmable, bidirectional, CMOS compatible I/O port. These three I/O lines can be configured under software control to be inputs or outputs (Figure 4). Inputs are Schmitt-triggered.



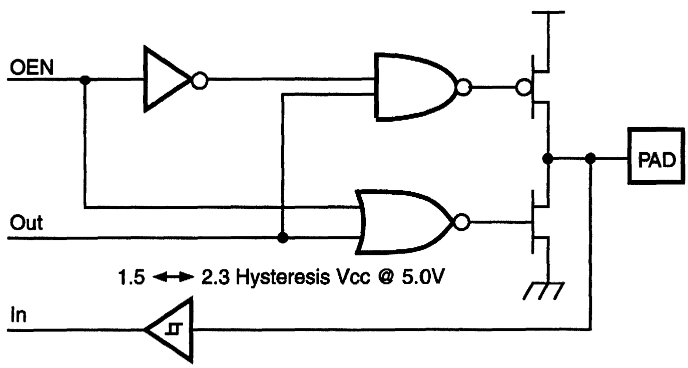
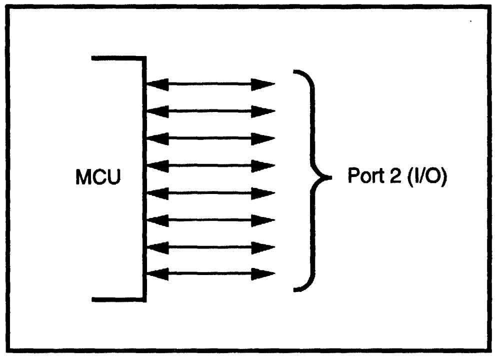


Figure 4. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit I/O, bit programmable, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 5). Inputs are Schmitt-triggered.



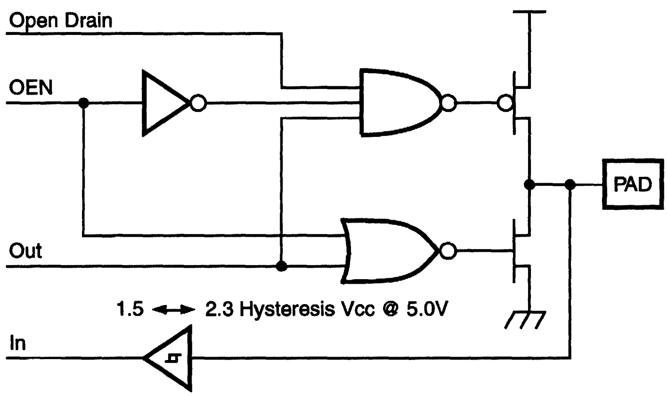


Figure 5. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P33-P31). Port 3 is a 3-bit, CMOS compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines can also be used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN}) (Figure 6).

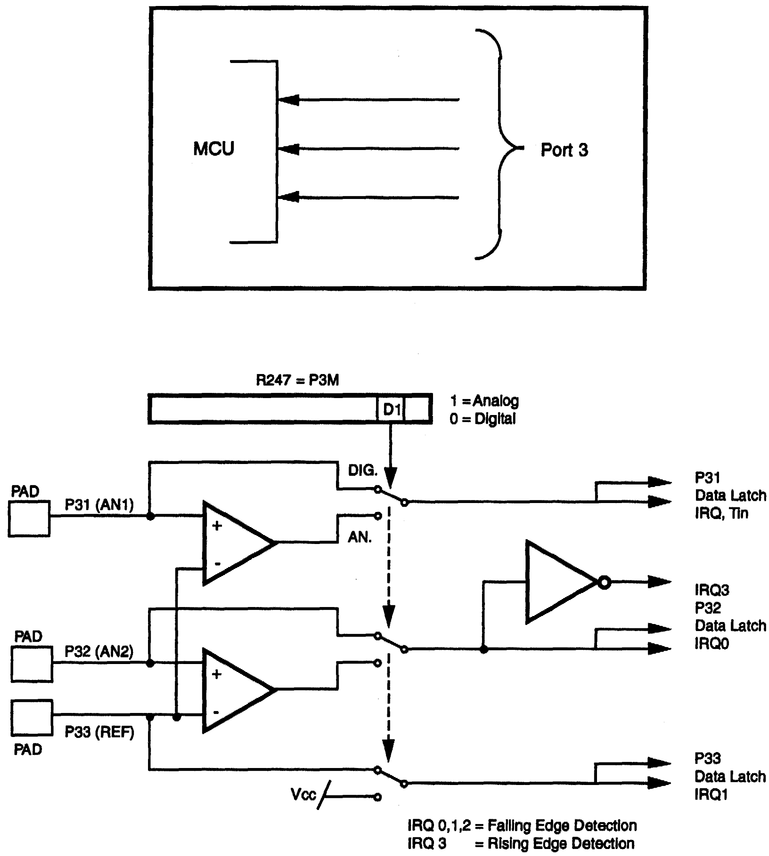


Figure 6. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to Port 3 inputs for interface flexibility.

Typical applications for the on-board comparators are: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output may be used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators may be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

Reset. Upon power-up the Power-On Reset circuit waits for T_{POR}, plus 18 clock cycles, and then starts program execution at address %000C (HEX) (Figure 7). Reference the Z86C07 control registers' Reset value (Table 2).

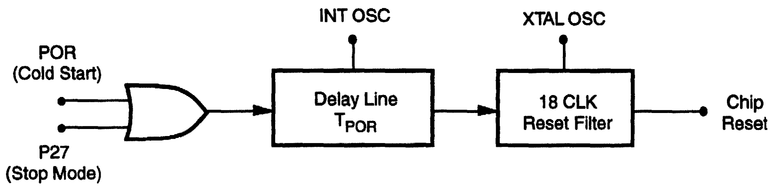


Figure 7. Internal Reset Configuration

Table 2. Z86C07 Control Registers

Addr.	Reg.	Reset Condition D7	D6	D5	D4	D3	D2	D1	D0	Comments
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
PB	IMR	0	U	U	U	U	U	U	U	
PC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0	0	
FE	SPH	U	U	U	U	U	U	U	U	Not used, stack always internal
FF	SPL	U	U	U	U	U	U	U	U	

Note:
* Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 3 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86C07 can address up to 2 Kbytes of internal program memory (Figure 8). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-2048 are on-chip mask-programmed ROM.

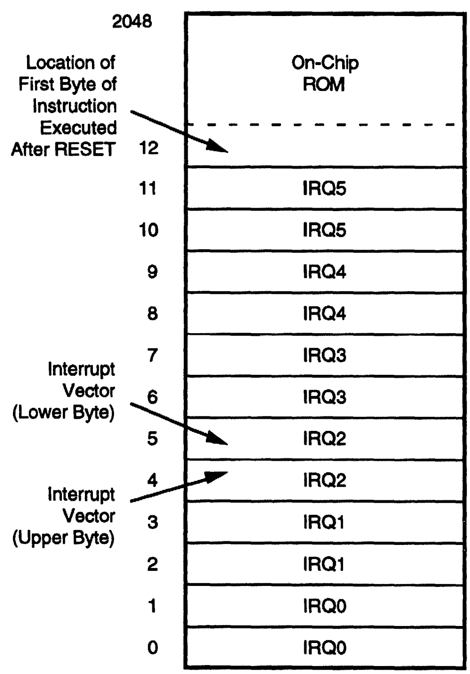


Figure 8. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 15 control and status registers (R3-R0, R127-R4 and R255-R241, respectively - Figure 9). The Z86C07 instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 10) addresses the starting location of the active working-register group.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

Location		Indentifiers
255	Stack Pointer (Bits 7-0)	SPL
254	General Purpose Register	
253	Register Pointer	RP
252	Program Control Flags	Flags
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240 / 128	Not Implemented	
127 / 4	General Purpose Registers	
3	Port 3	P3
2	Port 2	P2
1	Reserved	P1
0	Port 0	P0

Figure 9. Register File

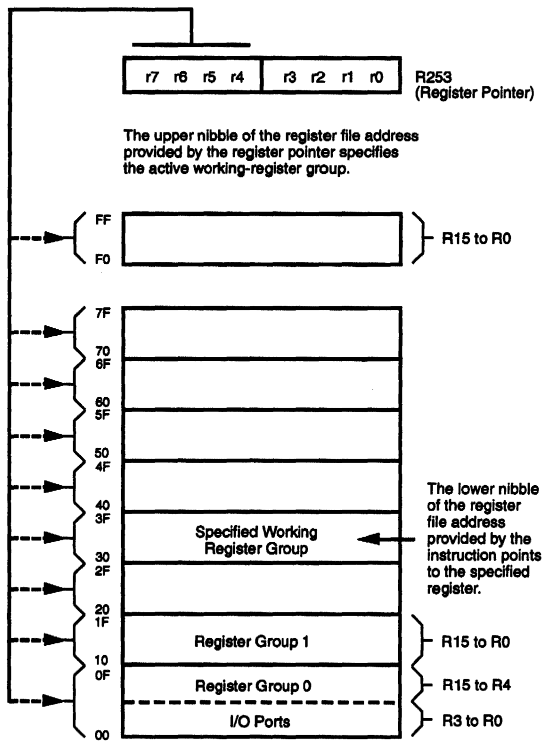


Figure 10. Register Pointer

Stack Pointer. The Z86C07 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 11).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that is retriggerable or not retriggerable, or as a gate input for the internal clock.

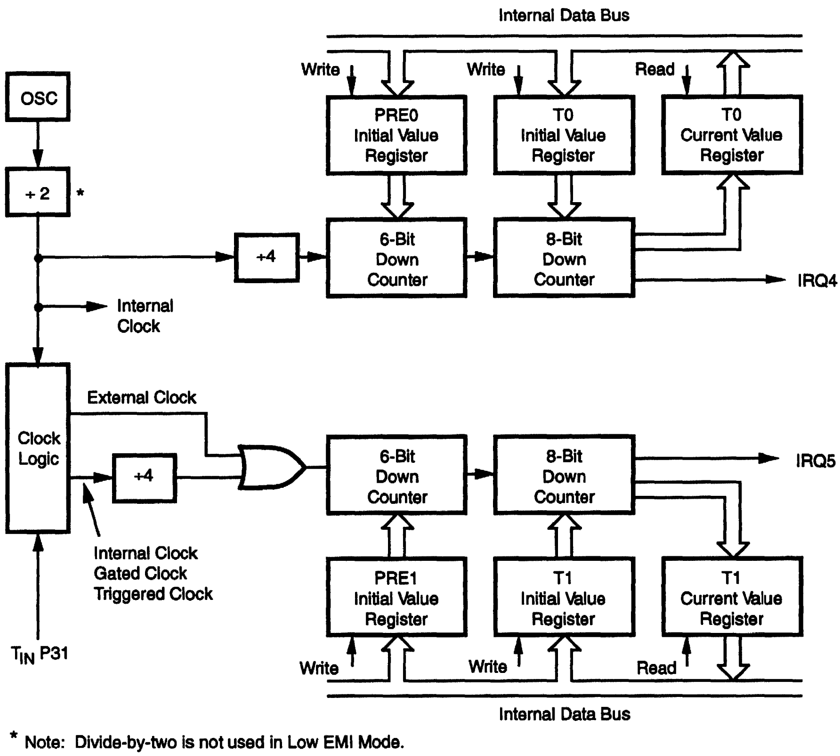


Figure 11. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86C07 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 12). The six sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 3).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C07 interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86C08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the Z86CCP00ZEM emulator.

Table 3. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

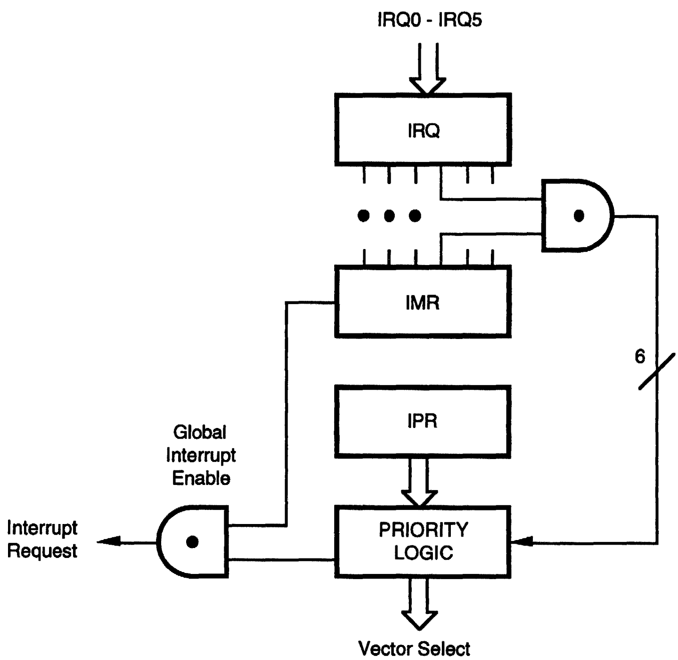


Figure 12. Interrupt Block Diagram

Clock. The Z86C07 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 13).

Note that the crystal capacitor loads should be connected to V_{SS}, pin 14 to reduce Ground noise injection.

HALT Mode. This instruction turns off the internal CPU clock, but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device can be recovered by interrupts, either externally or internally generated. The program execution begins at location 000C (HEX). An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to less than 10 µA. The STOP Mode can be released by two methods. The first method is a RESET of the device by removing V_{CC}. The second method is if P27 is configured as an input line when the device executes the STOP instruction. A low input level on P27 releases the STOP Mode.

Program execution under both conditions begins at location 000C (HEX). However, when P27 is used to release the STOP Mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state.

To use the P27 release approach with STOP Mode, use the following instruction:

```
LD P2M, #1XXXXXXXB
NOP
STOP
X = depends on user's application
```

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate SLEEP instruction. i.e.:

```
FF   NOP    ; clear the pipeline
6F   STOP   ; enter STOP mode
            or
FF   NOP    ; clear the pipeline
7F   HALT   ; enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is permanently enabled. The WDT should be refreshed at least every Twdt; otherwise, the Z86C07 resets itself.

WDT = 5F (HEX).

Opcode WDT (5FH). Execution of this command clears the WDT counter. This has to be done at least every Twdt. Otherwise, the WDT times out and generates a Reset. The generated Reset is the same as a Power-On Reset of T_{POR}, plus 18 XTAL clock cycles. The WDT instruction affects the Flags accordingly: Z = 1, S = 0, V = 0.

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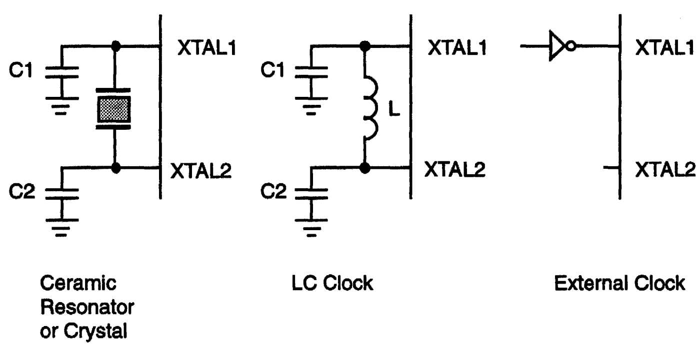


Figure 13. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

ROM Protect. ROM Protect fully protects the Z86C07 ROM code from being read internally. **When ROM Protect is selected, the Z86C07 will disable the instructions LDC and LDCI (Z86C04/C08 and Z86E04/E08 do not support the instructions of LDE and LDEI) in all modes. ROM look-up tables cannot be used in this mode.**

Low Voltage Protection (VLV). The Low Voltage trip voltage (V_{LV}) is less than 3 volts and above 1.4 volts under the following conditions:

Maximum (V_{LV}) Conditions:

Case 1: T_A = –40°C, +105°C, Internal Clock Frequency equal or less than 1 MHz

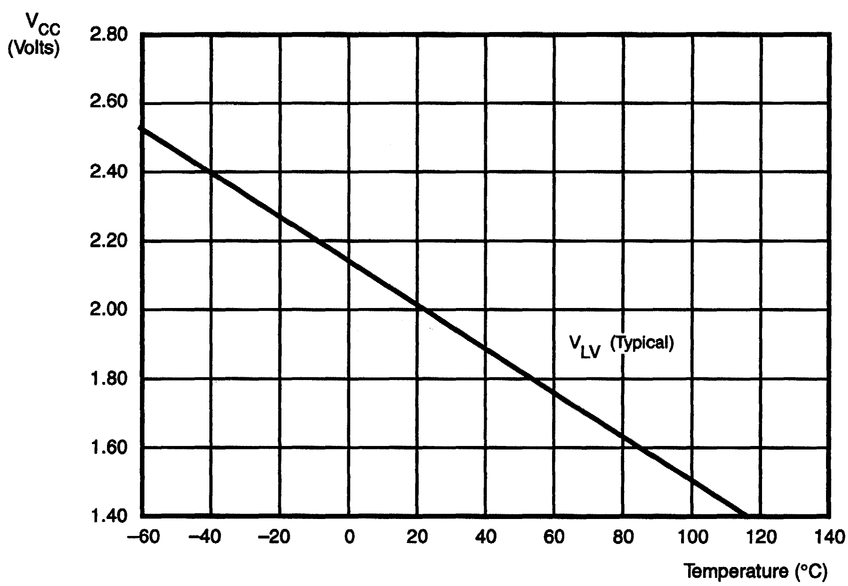
Case 2: T_A = –40°C, +85°C, Internal Clock Frequency equal or less than 2 MHz

Note: The internal clock frequency is one-half the external clock frequency.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low Voltage Protection trip point (V_{LV}) is reached. The device is guaranteed to function normally at supply voltages above the low voltage trip point for the temperatures and operating frequencies in Case 1 and Case 2 above. The actual low voltage trip point is a function of temperature and process parameters (Figure 14).

2 MHz (Typical)

Temp	–40°C	0°C	+25°C	+70°C	+105°C
V_{LV}	2.55	2.4	2.1	1.7	1.6



Power-On Reset threshold for V_{CC} and 4 MHz V_{LV} overlap

Figure 14. Typical Z86C07 V_{LV} vs Temperature

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	°C
Storage Temperature	–65	+150	°C
Voltage on any Pin with Respect to V_{SS} (Note 1)	–0.6	+12	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on Pin 7 with Respect to V_{SS} (Note 2)	–0.6	V_{DD}+1	V
Total Power Dissipation		462	mW
Maximum Current out of V_{SS}		85	mA
Maximum Current into V_{DD}		85	mA
Maximum Current into an Input Pin (Note 3)		±600	µA
Maximum Current into an Open-Drain Pin (Note 4)		±600	µA
Maximum Output Current Sinked by any I/O Pin		12	mA
Maximum Output Current Sourced by any I/O Pin		12	mA
Total Maximum Output Current Sinked by Port 2		70	mA
Total Maximum Output Current Sourced by Port 2		70	mA

Notice:
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Total power dissipation should not exceed 616 mW for the package. Power dissipation is calculated as follows:

Notes:
[1] This applies to all pins except where noted. Maximum current into pin must be ±600 µA.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes Pin 7 and Pin 8.
[4] Device pin is not at an output Low state.

Total Power Dissipation = $V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$

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STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 15).

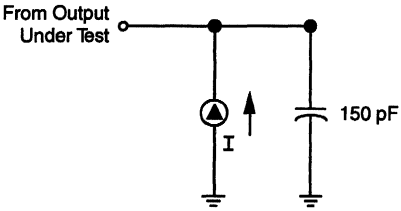

Figure 15. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

V_{CC} SPECIFICATION

V_{CC} = 3.0V to 5.0V
Typicals are at 3.3V and 5.0V.

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC}[4]	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
V_{CH}	Clock Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator
		5.5V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	2.75	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V	
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V	
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		V_{CC}–0.4		2.7	V	I_{OH} = –2.0 mA [5]
		5.5V	V_{CC}–0.4		V_{CC}–0.4		5.5	V	I_{OH} = –2.0 mA [5]
		3.0V	V_{CC}–0.4		V_{CC}–0.4			V	Low Noise @ 0.5 mA
		5.5V	V_{CC}–0.4		V_{CC}–0.4			V	Low Noise @ 0.5 mA
V_{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.3	V	I_{OL} = +4.0 mA [5]
		5.5V		0.4		0.4	0.2	V	I_{OL} = +4.0 mA [5]
		3.0V		0.4		0.4		V	Low Noise @ 0.5 mA
		5.5V		0.4		0.4		V	Low Noise @ 0.5 mA
V_{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.8	V	I_{OL} = +12 mA, 3 Pin Max [5]
		5.5V		0.8		0.8	0.3	V	I_{OL} = +12 mA, 3 Pin Max [5]
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV	
		5.5V		25		25	10	mV	
V_{LV}	V_{CC} Low Voltage			2.7		2.95	2.1	V	@ 1 MHz Max, Int. CLK Freq
I_{IL}	Input Leakage	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}
$_{OL}$	Output Leakage	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}
V_{ICMR}	Input Common Mode Range		0	V_{CC} –1.0	0	V_{CC} –1.5		V	

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DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC}[4]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC}	Supply Current	3.2V					80	µA	All output and I/O Pins Floating @ 32 kHz [7]
		5.5V		7.0		7.0	3.5	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		5.0		8.0	2.5	mA	All Output and I/O Pins Floating @ 8 MHz
		5.5V		11.0		11.0	5.3	mA	All Output and I/O Pins Floating @ 8 MHz
		3.0V		7.5		10	3.0	mA	All Output and I/O Pins Floating @ 12 MHz
		5.5V		15		15	7.5	mA	All Output and I/O Pins Floating @ 12 MHz
I_{CC1}	Standby Current	3.0V		2.5		2.5	0.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		4.0		5.0	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		3.0		4.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz
		5.5V		5.0		5.0	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz
		3.0V		4.5		4.5	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
		5.5V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
I_{CC}	Supply Current (Low Noise Mode)	3.0V		3.5		3.5	1.0	mA	All Output and I/O Pins Floating @ 1 MHz
		5.5V		7.0		7.0	2.8	mA	All Output and I/O Pins Floating @ 1 MHz
		3.0V		5.8		5.8	1.5	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		9.0		9.0	3.5	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		8.0		8.0	2.0	mA	All Output and I/O Pins Floating @ 4 MHz
		5.5V		11.0		11.0	5.4	mA	All Output and I/O Pins Floating @ 4 MHz

Sym	Parameter	V_{CC}[4]	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC1}	Standby Current (Low Noise Mode)	3.0V		1.2		1.2	0.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		5.5V		1.6		1.6	0.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		3.0V		1.5		1.5	0.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		1.9		1.9	1	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		2.0		2.0	0.9	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
		5.5V		2.4		2.4	1.6	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
I_{CC2}	Standby Current	3.0V		10		20	1.2	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running
		5.5V		10		20	2.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3	5.0	mA	8 MHz
Crystal/Resonator	3.5	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND

[3] For 2.75V operating, the device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.

[4] The V_{CC} Voltage specification of 3.0V guarantees 3.3V ±0.3V and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.

[5] Standard Mode (not Low EMI Mode)

[6] Excludes clock pins.

[7] CL1 = 100 pF, CL2 = 220 pF, RF = 30 kOhms.

DC ELECTRICAL CHARACTERISTICS

Timing Diagrams

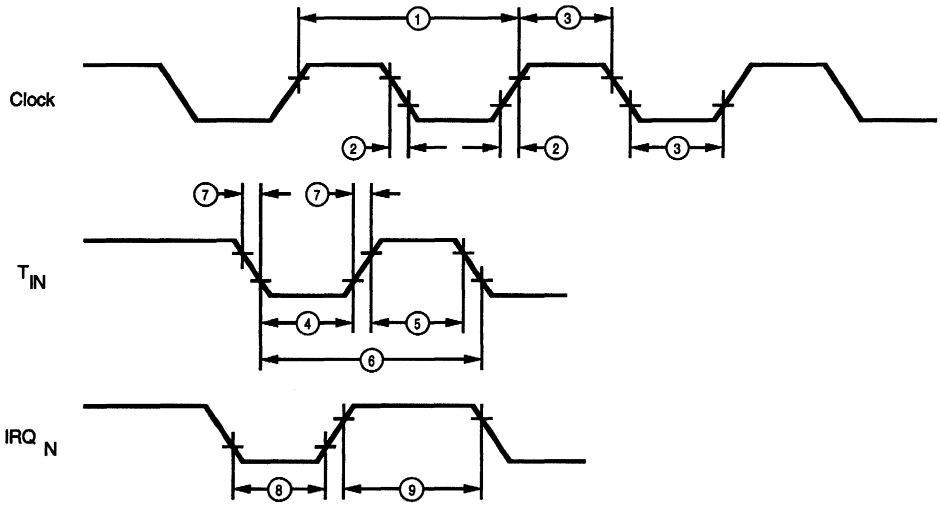

Figure 16. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS
Timing Table (Standard Mode)

				T_A = –40°C to +105°C					
				8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}[3]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	ns	[1]
			5.5V	125	DC	83	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15	ns	[1]
			5.5V		25		15	ns	
3	TwC	Input Clock Width	3.0V	62		41			[1]
			5.5V	62		41		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			[1]
			5.5V	8TpC		8TpC			[1]
7	TrTin, TfTin	Timer Input Rise and Fall Timer	3.0V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	3.0V	25		25		ms	[1,4]
			5.5V	5		5		ms	[1,4]
11	Tpor		3.0V		24		24	ms	[1]
			5.5V		12		12	ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] The V_{CC} Voltage specification of 3.0V guarantees 3.3V ±0.3V and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
[4] Length of time before WDT times out.

Low Noise Version

Low EMI Emission

The Z86C07 can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT mode, –0°C to +70°C.
- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

EMI Characteristics

The Z86C07 operating in the Low EMI mode generates EMI as measured in the following chart:

The measurements shown in Figure 17 were made while operating the Z86C07 in three states: (1) Idle condition; (2) static output; (3) switched output.

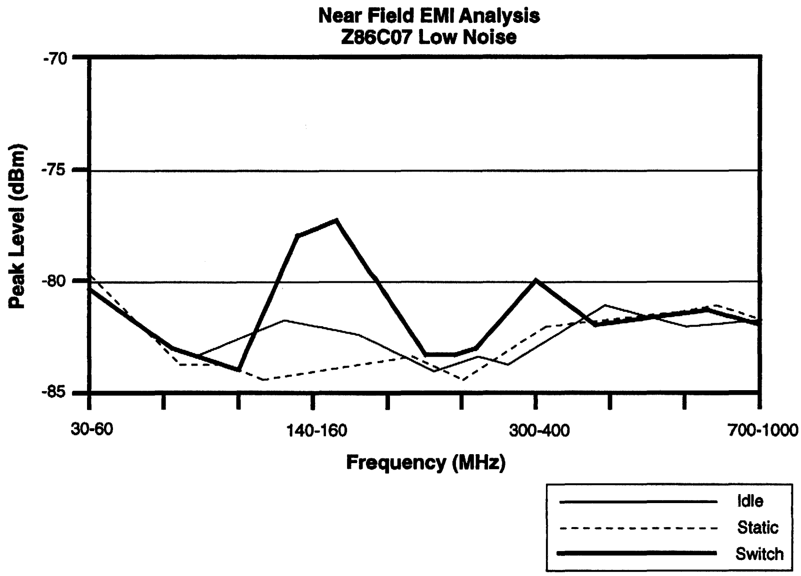

Figure 17. Low Noise Analysis

AC ELECTRICAL CHARACTERISTICS
Low Noise Mode

				T_A = 0°C to +70°C				T_A = –40°C to +105°C					
				1 MHz		4 MHz		1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}[3]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC		4TpC		4TpC			[1]
			5.5V	4TpC		4TpC		4TpC		4TpC			[1]
7	TrTin,	Timer Input Rise	3.0V		100		100		100		100	ns	[1]
	TtTin	and Fall Timer	5.5V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input	3.0V	100		100		100		100		ns	[1,2]
		Low Time	5.5V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
		High Time	5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer	3.0V	25		25		25		25		ms	[1,4]
		Delay Time	5.5V	5		5		5		5		ms	[1,4]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] The V_{CC} Voltage specification of 3.0V guarantees 3.3V ±0.3V and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
[4] Length of time before WDT times out.

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Z8 CONTROL REGISTER DIAGRAMS

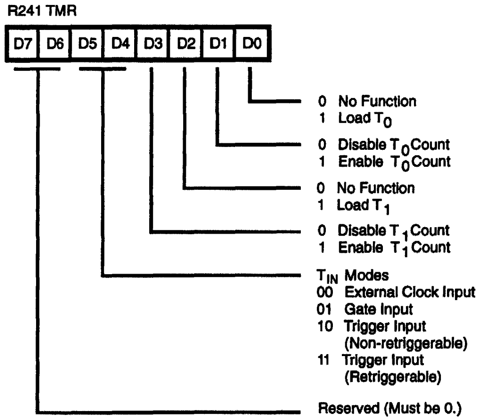

Figure 18. Timer Mode Register ($F1_H$: Read/Write)

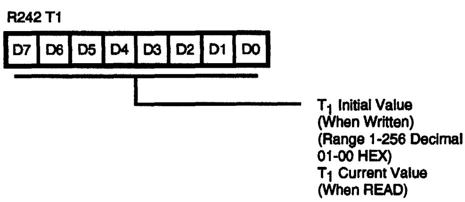

Figure 19. Counter Time 1 Register ($F2_H$: Read/Write)

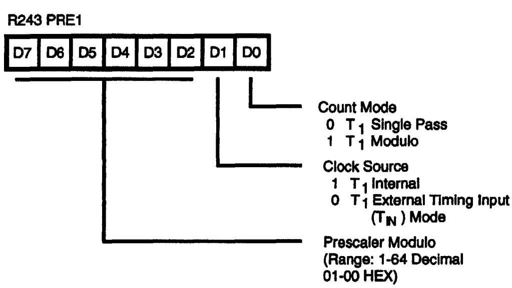

Figure 20. Prescaler 1 Register ($F3_H$: Write Only)

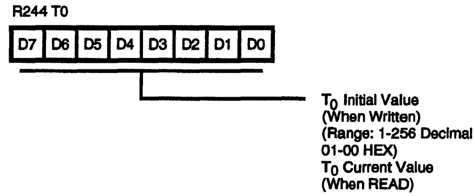

Figure 21. Counter/Timer 0 Register ($F4_H$: Read/Write)

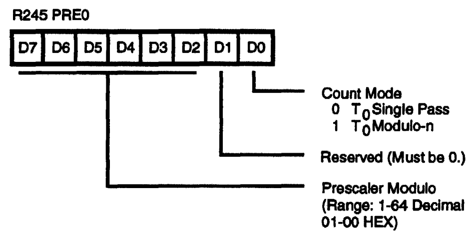

Figure 22. Prescaler 0 Register ($F5_H$: Write Only)

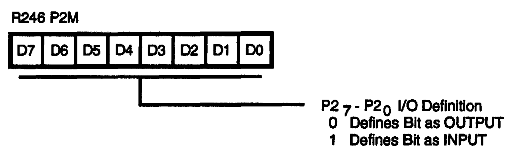

Figure 23. Port 2 Mode Register ($F6_H$: Write Only)

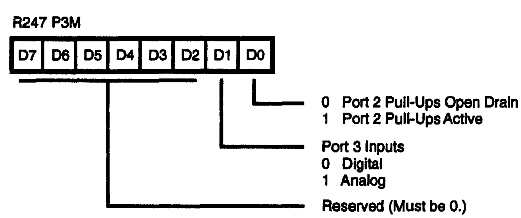

Figure 24. Port 3 Mode Register ($F7_H$: Write Only)

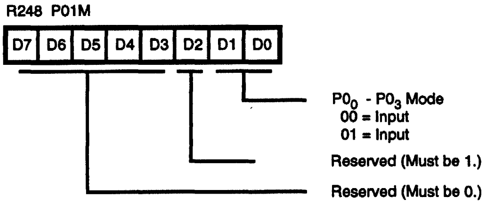

Figure 25. Port 0 and 1 Mode Register (F8$_H$: Write Only)

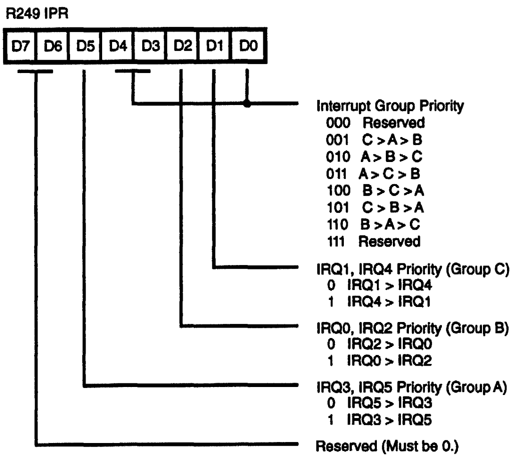

Figure 26. Interrupt Priority Register (F9$_H$: Write Only)

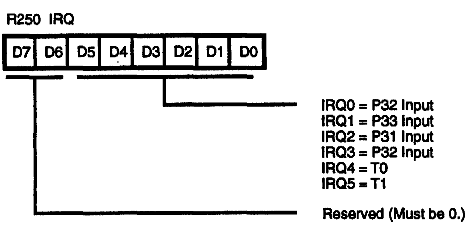

Figure 27. Interrupt Request Register (FA$_H$: Read/Write)

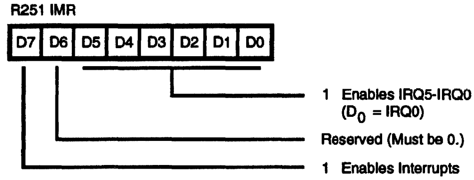

Figure 28. Interrupt Mask Register (FB$_H$: Read/Write)

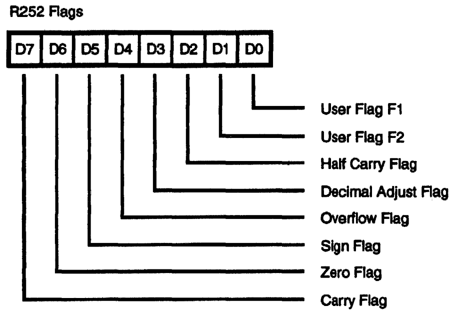

Figure 29. Flag Register (FC$_H$: Read/Write)

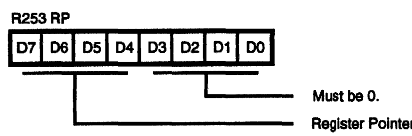

Figure 30. Register Pointer (FD$_H$: Read/Write)

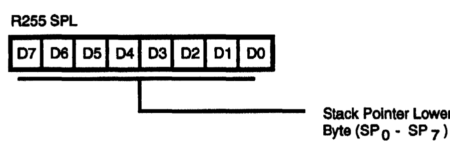

Figure 31. Stack Pointer (FF$_H$: Read/Write)

DEVICE CHARACTERISTICS

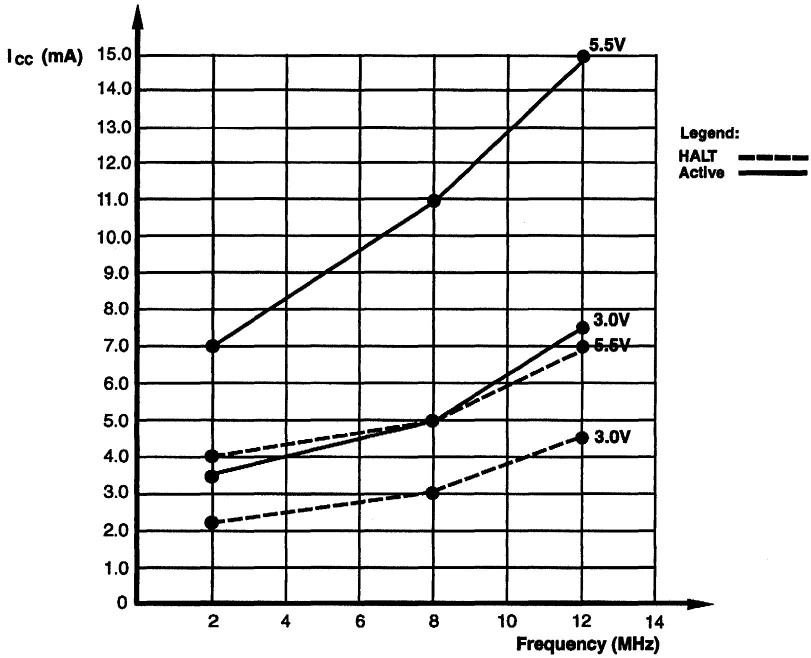

Figure 32. Maximum I_{CC} vs Frequency

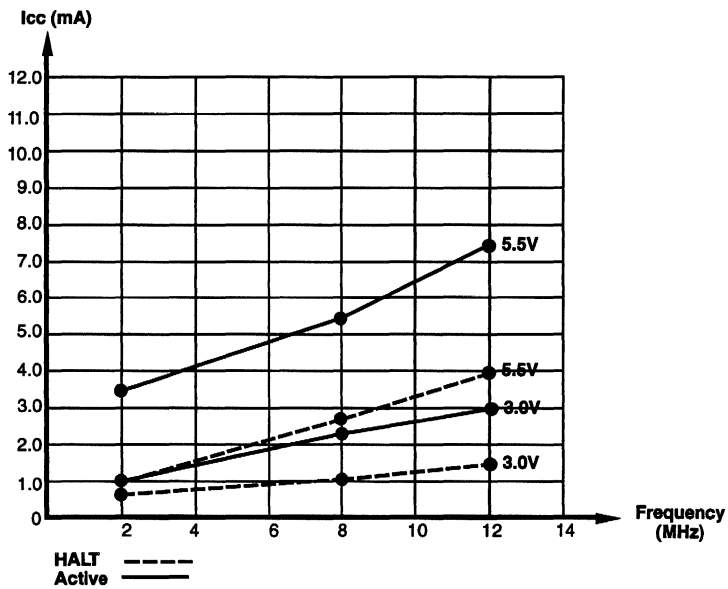

Figure 33. Typical I_{CC} vs Frequency

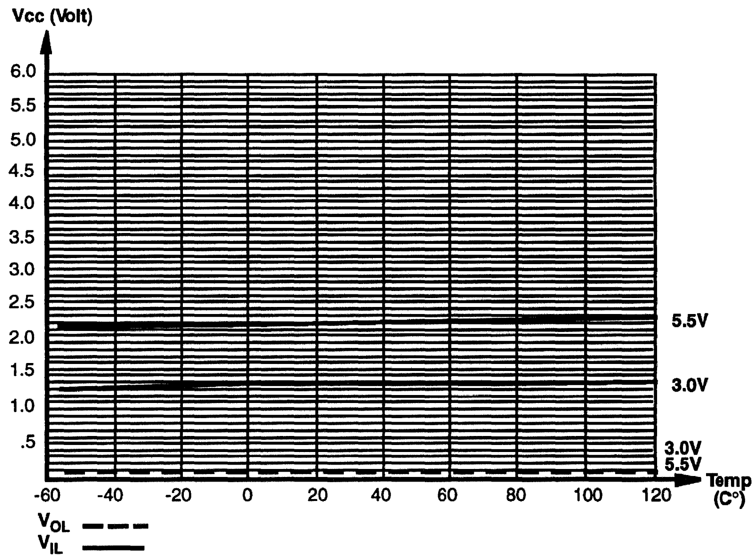

Figure 34. V_{IL}, V_{OL} vs Temperature

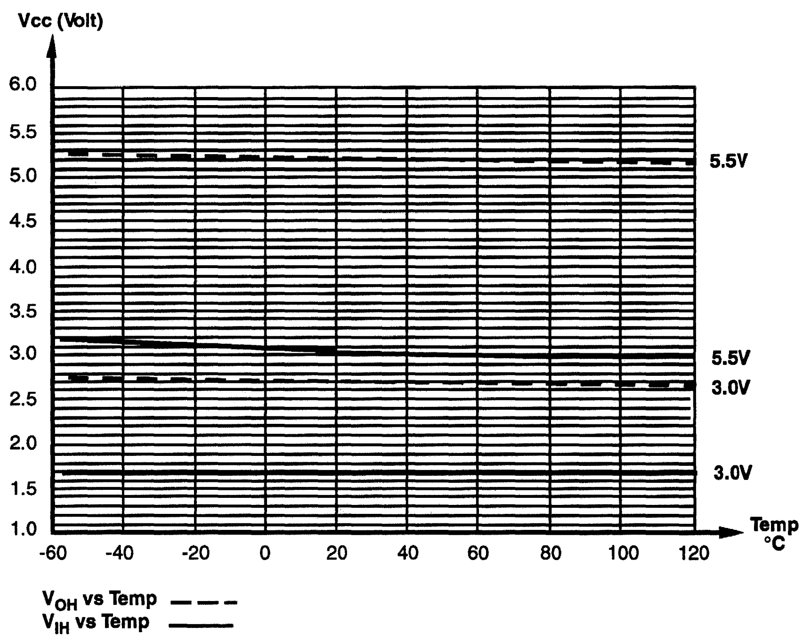

Figure 35. V_{IH}, V_{OH} vs Temperature

DEVICE CHARACTERISTICS (Continued)

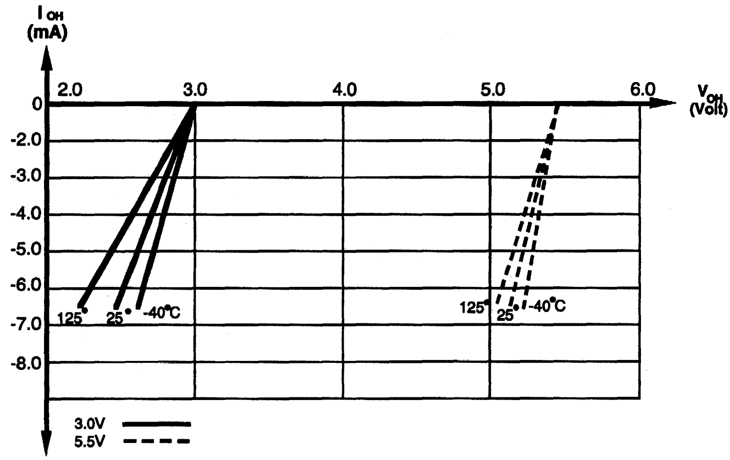

Figure 36. Typical I_{OH} vs V_{OH}

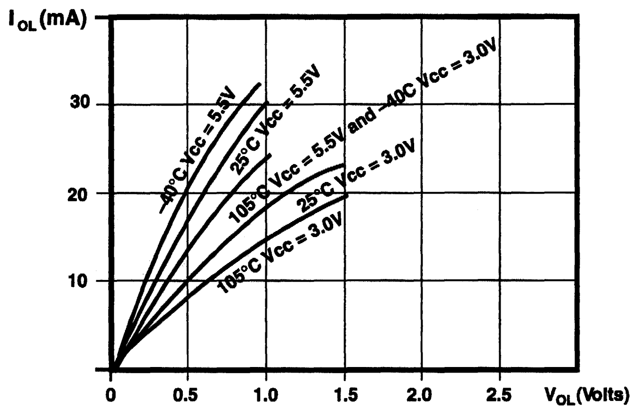

Figure 37. Typical I_{OL} vs V_{OL}

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

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CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	---	Always true	---
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000	F	Never True (Always False)	---

INSTRUCTION FORMATS

One-Byte Instructions

Format	Instructions
[OPC]	CCF, DI, EI, IRET, NOP, RCF, RET, SCF
[dst | OPC]	INC r

Two-Byte Instructions

Format	Instructions
[OPC | MODE] [dst/src] OR [1 1 1 0 | dst/src]	CLR, CPL, DA, DEC, DECW, INC, INCW, POP, PUSH, RL, RLC, RR, RRC, SRA, SWAP
[OPC] [dst] OR [1 1 1 0 | dst]	JP, CALL (Indirect)
[OPC] [VALUE]	SRP
[OPC | MODE] [dst | src]	ADC, ADD, AND, CP, OR, SBC, SUB, TCM, TM, XOR
[MODE | OPC] [dst/src | src/dst]	LD, LDE, LDEI, LDC, LDCI
[dst/src | OPC] [src/dst] OR [1 1 1 0 | src]	LD
[dst | OPC] [VALUE]	LD
[dst/CC | OPC] [RA]	DJNZ, JR
[FFH] [6FH | 7FH]	STOP/HALT

Three-Byte Instructions

Format	Instructions
[OPC | MODE] [src] OR [1 1 1 0 | src] [dst] OR [1 1 1 0 | dst]	ADC, ADD, AND, CP, LD, OR, SBC, SUB, TCM, TM, XOR
[OPC | MODE] [dst] OR [1 1 1 0 | dst] [VALUE]	ADC, ADD, AND, CP, LD, OR, SBC, SUB, TCM, TM, XOR
[MODE | OPC] [src] OR [1 1 1 0 | src] [dst] OR [1 1 1 0 | dst]	LD
[MODE | OPC] [dst/src | x] [ADDRESS]	LD
[cc | OPC] [DAU] [DAL]	JP
[OPC] [DAU] [DAL]	CALL

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

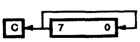
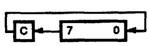
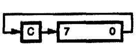
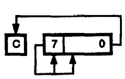
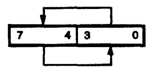
dst(7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	C	Z	S	V	D	H
OR dst, src dst←dst OR src	†	4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP+1	R IR	50 51	-	-	-	-	-	-
PUSH src SP←SP−1; @SP←src	R IR	70 71	-	-	-	-	-	-
RCF C←0		CF	0	-	-	-	-	-
RET PC←@SP; SP←SP+2		AF	-	-	-	-	-	-
RL dst 	R IR	90 91	*	*	*	*	-	-
RLC dst 	R IR	10 11	*	*	*	*	-	-
RR dst 	R IR	E0 E1	*	*	*	*	-	-
RRC dst 	R IR	C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst−src−C	†	3[ ]	*	*	*	*	1	*
SCF C←1		DF	1	-	-	-	-	-
SRA dst 	R IR	D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im	31	-	-	-	-	-	-
STOP		6F	1	-	-	-	-	-
SUB dst, src dst←dst−src	†	2[ ]	*	*	*	*	1	*
SWAP dst 	R IR	F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†	6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†	7[ ]	-	*	*	0	-	-
WDH		4F	-	-	-	-	-	-
WDT		5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†	B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

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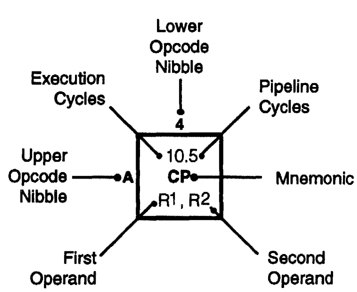
OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1							↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1							↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** Irr1, r2	18.0 **LDCI** Irr1, Ir2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



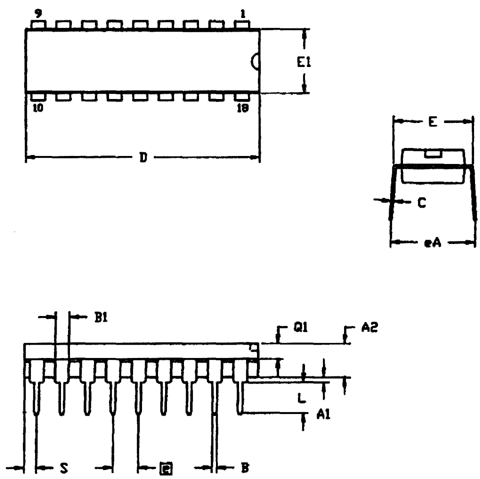
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas reserved.

*2-byte instruction appears as a 3-byte instruction

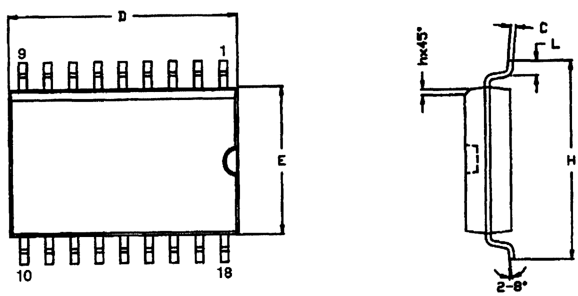
PACKAGE INFORMATION

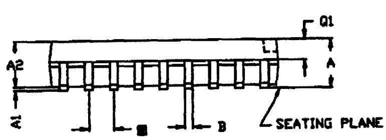


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

5

ORDERING INFORMATION

Z86C07 (8 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	**18-Pin SOIC**	**18-Pin DIP**	**18-Pin SOIC**
Z86C0708PSC	Z86C0708SSC	Z86C0708PEC	Z86C0708SEC

Z86C07 (12 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	**18-Pin SOIC**	**18-Pin DIP**	**18-Pin SOIC**
Z86C0712PSC	Z86C0712SSC	Z86C0712PEC	Z86C0712SEC

For fast results, contact your local Zilog sale offices for assistance in ordering the part desired.

CODES

Preferred Package
P = DIP

Longer Lead Time
S = SOIC

Preferred Temperature
S = 0°C to +70°C

Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:
Z 86C07 08 P S C is a Z86C07, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 08 — Speed
- 86C07 — Product Number
- Z — Zilog Prefix

ZILOG

Z86E07

CMOS Z8® 8-BIT OTP MICROCONTROLLER

FEATURES

- Low Cost, 8-Bit CMOS MCU (OTP Support for Z86C07)
- 18-Pin Package (DIP, SOIC)
- 2 Kbytes of One-Time-PROM
- 124 Bytes of General-Purpose RAM
- 4.0V to 5.5V Operating Range
- Clock Speed: 12 MHz
- Low Power Consumption: 50 mW (Typical)
- Low Noise Programmable
- Programmable ROM Protect
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler.
- Fast Instruction Pointer: 1 µs @ 12 MHz
- Two Standby Modes: STOP and HALT
- 14 Input/Output Lines
- 11 Digital Inputs, CMOS Levels, Schmitt-Triggered.
- Six Vectored, Priority Interrupts from Six Different Sources.
- Programmable Interrupt Polarity
- Software-Programmable Watch-Dog Timer
- Power-On Reset Timer
- Two On-Board Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.

GENERAL DESCRIPTION

The Z86E07 8-bit One-Time-Programmable (OTP) Microcontroller (MCU) is a member of the Z8® single-chip microcontroller family with 2 Kbytes of one-time PROM and 124 Bytes of General-Purpose RAM. The device is housed in an 18-pin DIP or SOIC style package and is manufactured in CMOS technology. The Z86E07 allows easy software development and debug, prototyping, and is ideal for small production runs not economically desirable with a masked ROM version.

For applications demanding powerful I/O capabilities, the Z86E07 provides 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals. There are two basic address spaces available to support this configuration: program memory and 124 bytes of general-purpose registers.

The Z86E07 offers programmable EPROM Protect and programmable Low Noise. When the part is programmed for EPROM Protect, the Low Noise feature will automatically be enabled. When programmed for Low Noise, the EPROM Protect feature is optional.

With a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features, the Z86E07 is well-suited for a variety of consumer, industrial and commercial applications.

GENERAL DESCRIPTION (Continued)

To unburden the system from coping with real-time tasks, such as counting/timing and I/O data communications, the Z86E07 offers two on-chip counter/timers with a large number of user selectable modes. The device also features two on-board comparators that process analog signals with a common reference voltage (Figures 1 and 2).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

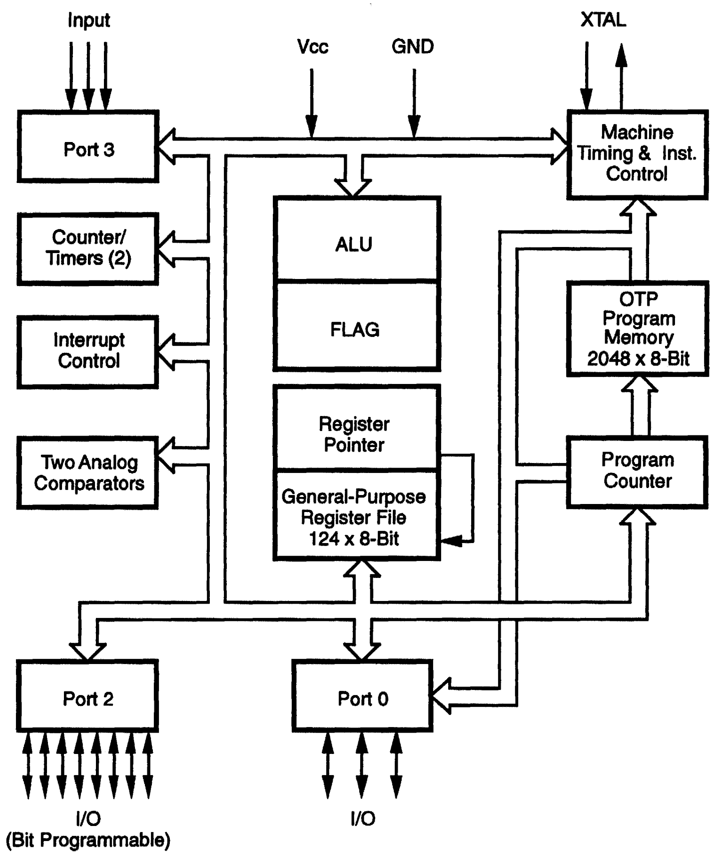


Figure 1. Z86E07 Functional Block Diagram

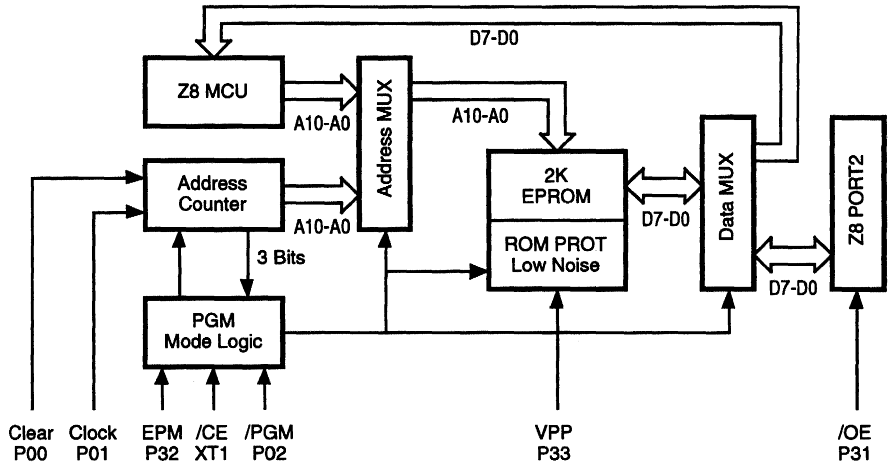


Figure 2. Z86E07 EPROM Mode Block Diagram

PIN DESCRIPTION

Table 1. Z86E07 18-Pin DIP Pin Identification

EPROM Mode Pin #	Symbol	Function	Direction
1-4	D7-D4	Data 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	N/C	No Connection	
7	/CE	Chip Enable	Input
8	/OE	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	V_{PP}	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	/PGM	Prog Mode	Input
14	GND	Ground	
15-18	D3-D0	Data 0,1, 2, 3	In/Output

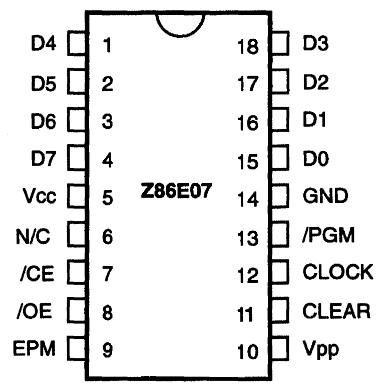


Figure 3. Z86E07 18-Pin DIP Pin Configuration EPROM Mode

PIN DESCRIPTION

Table 2. Z86E07 18-Pin DIP Pin Identification*

Standard Mode Pin #	**Symbol**	**Function**	**Direction**
1-4	P27-P24	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1	Input
9	P32	Port 3, Pin 2	Input
10	P33	Port 3, Pin 3	Input
11-13	P02-P00	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P23-P20	Port 2, Pins 0, 1, 2, 3	In/Output

Note:
* Pin Identification and Configuration identical on DIP and SOIC style packages.

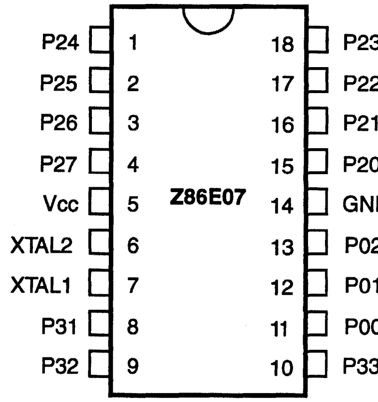


Figure 4. Z86E07 18-Pin DIP Pin Configuration* Standard Mode

PIN FUNCTIONS

OTP Programming Mode

D7-D0 *Data Bus.* The data can be read from, or written to the EPROM through this data bus.

V_{CC} *Power Supply.* It is 5V during the EPROM Read mode and 6V during the other mode.

/CE *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode (V_{IL}, V_{IH}, V_H = 12V ±0.5V).

/OE *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages (V_{IL}, V_{IH}, V_H = 12V ±0.5V).

V_{PP} *Program Voltage.* This pin supplies the program voltage (V_H = 12V ±0.5V).

Clear *Clear* (active High). This pin resets the internal address counter at the High Level.

Clock *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock signal.

/PGM *Program Mode* (active Low). Low Level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise surges*** above V_{cc} occur on the XTAL1 pin.

In addition, processor operation of Z8 One-Time Programmable devices may be affected by ***excessive noise surges*** on the V_{pp}, /CE, /EPM, /OE pins while the microcontroller is in standard mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}.
- Adding a capacitor to the affected pin.

Z86E07 Standard Mode

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (12 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02-P00. Port 0 is a 3-bit bi-directional, Schmitt-triggered CMOS compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 5).

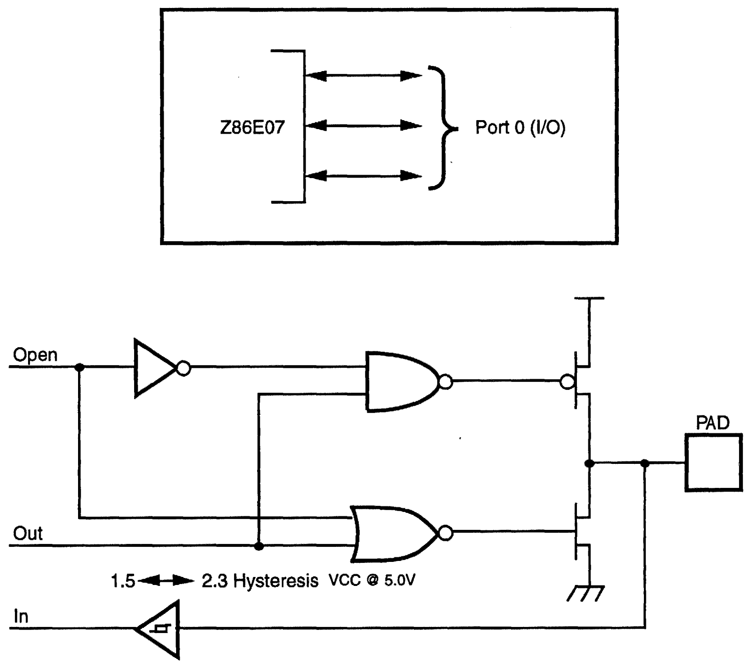


Figure 5. Port 0 Configuration

Z86E07 Standard Mode (Continued)

Port 2, P27-P20. Port 2 is an 8-bit, bit programmable, bi-directional, Schmitt-triggered CMOS compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 6).

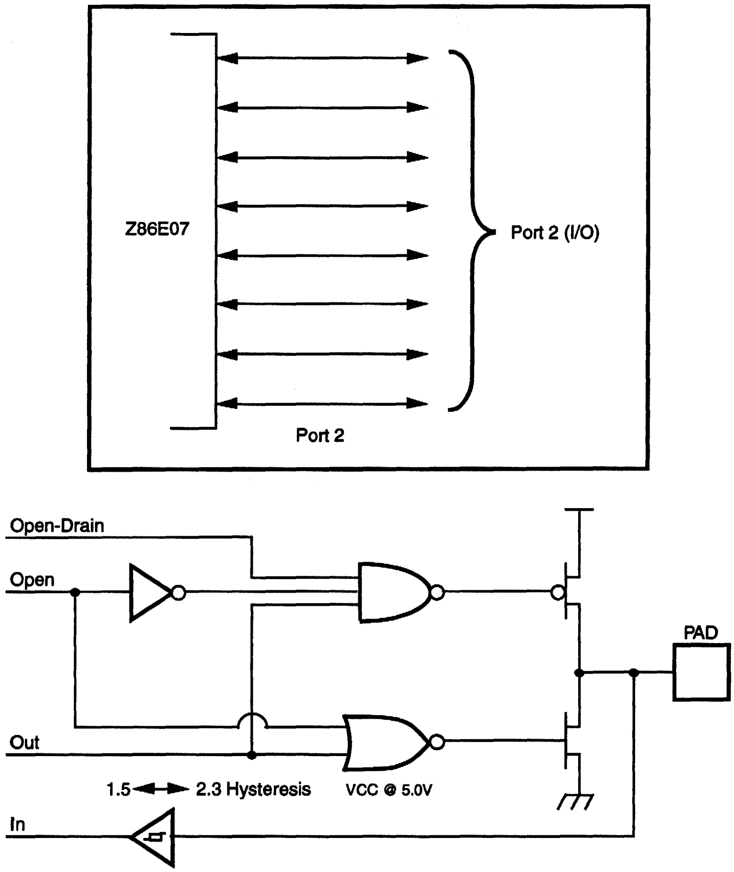
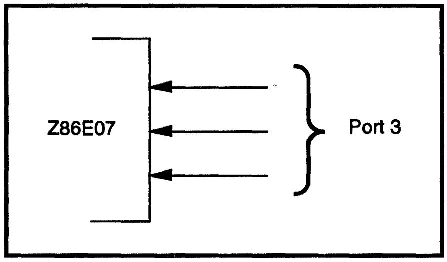


Figure 6. Port 2 Configuration

Port 3, P33-P31. Port 3 is a 3-bit, CMOS compatible port with three fixed input (P32-P30) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0-IRQ3 and as the timer input signal T_{IN} (Figure 7).



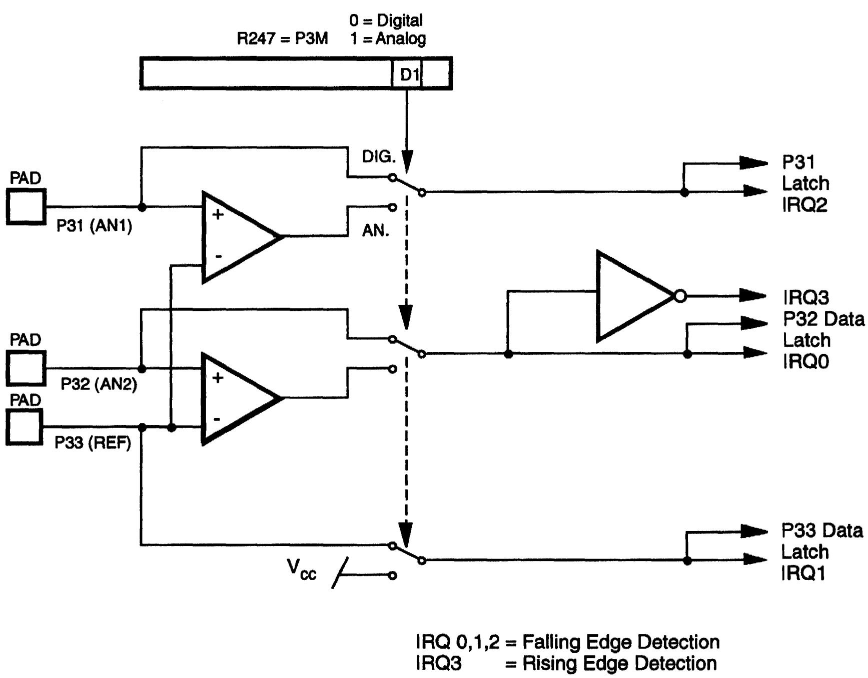


Figure 7. Port 3 Configuration

6

Z86E07 Standard Mode (Continued)

Comparator Inputs. Two analog comparators are added to input of Port 3, P31 and P32, for interface flexibility. The comparators reference voltage P3 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In analog mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP mode. The common voltage range is 0-4 V when the V_{CC} is 5.0 V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

RESET is accomplished through Power-On or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for T_{POR}, plus 18 clock cycles, then starts program execution at address 000C (Hex). Reference Table 3 for the Z86E07 control registers' reset values (Figure 8).

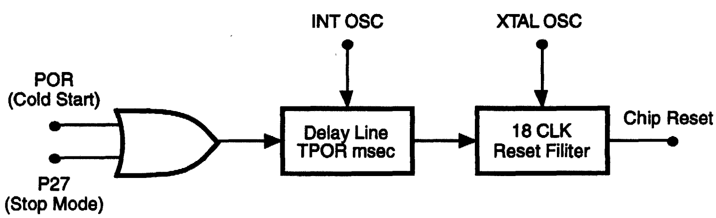


Figure 8. Internal Reset Configuration

Power-On Reset (POR). A timer circuit, clocked by a dedicated on-board RC oscillator, is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power bad to power good status
- STOP-Mode Recovery
- WDT time-out
- WDH time-out

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

Table 2. Z86C07 Control Registers

Addr.	Reg.	Reset Condition D7	D6	D5	D4	D3	D2	D1	D0	Comments
F1	TMR	0	0	0	0	0	0	0	0	Timers Off
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset.
F7*	P3M	U	U	U	U	U	U	0	0	Standard Port 3 inputs.
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection.
PB	IMR	0	U	U	U	U	U	U	U	
PC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0	0	
FF	SPL	U	U	U	U	U	U	U	U	

Note:
* Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 3 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86E07 addresses up to 2 Kbytes of internal program memory (Figure 9). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-2047 are on-chip one-time programmable ROM.

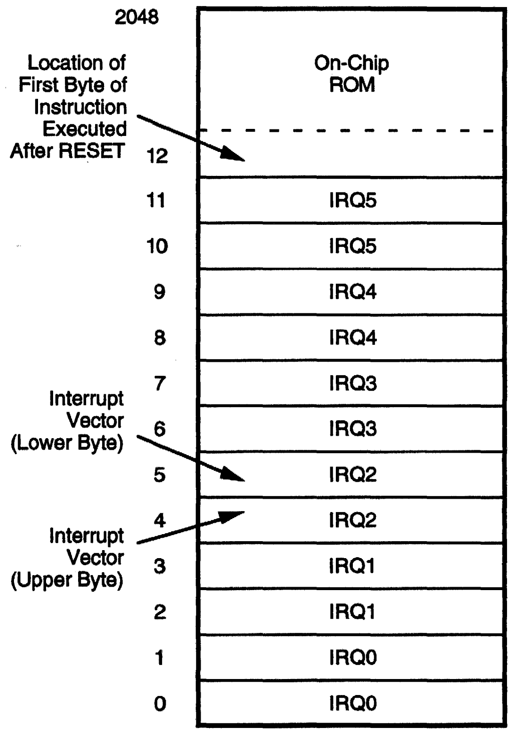


Figure 9. Program Memory Map

6

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers, R0-R3, R4-R127 and R241-R255, respectively (Figure 10). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8. The Mode and Configuration Registers are the same as the Z86C07. The Z86E07 instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 11) addresses the starting location of the active working-register group.

Stack Pointer. The Z86E07 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

Location		Indentifiers
255	Stack Pointer (Bits 7-0)	SPL
254	General-Purpose Register	GPR
253	Register Pointer	RP
252	Program Control Flags	Flags
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter1	T1
241	Timer Mode	TMR
128	Not Implemented	
127–4	General-Purpose * Registers	
3	Port 3	P3
2	Port 2	P2
1	Reserved	P1
0	Port 0	P0

* The general-purpose registers are undefined after device power-up. These register contents are not affected by reset from STOP-Mode Recovery or by WDT timeout.

Figure 10. Register File

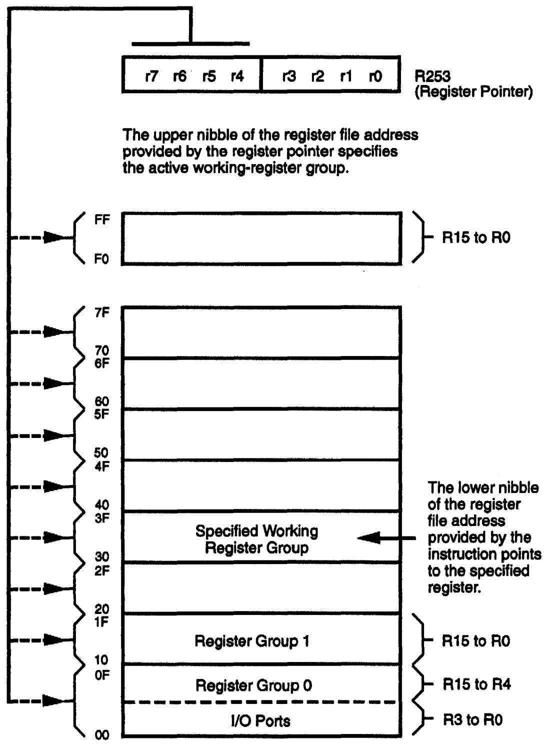


Figure 11. Register Pointer

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 12).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that is retriggerable or not retriggerable, or used as a gate input for the internal clock.

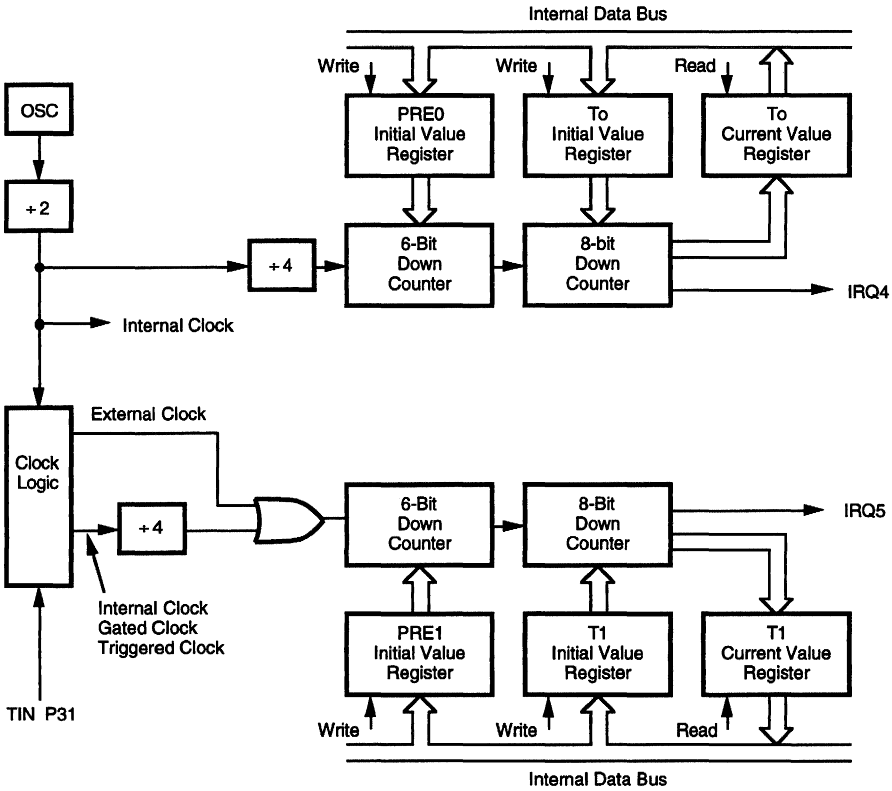


Figure 12. Counter/Timers Block Diagram

6

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86E07 has six interrupts from five different sources. These interrupts are maskable and prioritized (Figure 13). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86E07 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86C08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the Z86CCP00ZEM emulator.

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

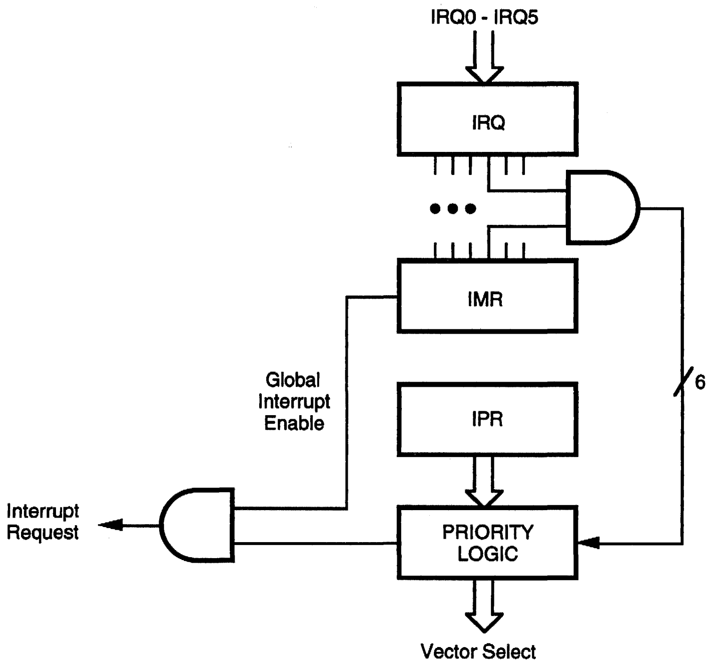


Figure 13. Interrupt Block Diagram

Clock. The Z86E07 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, 12 MHz max, with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors (capacitance values depend upon the crystal manufacturer, ceramic resonator and PCB layout) from each pin directly to device ground pin 14 (Figure 14). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.

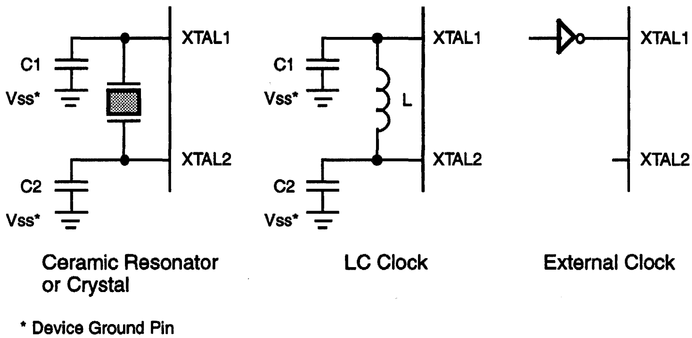


Figure 14. Oscillator Configuration

HALT Mode. This instruction turns off the internal CPU clock, but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP mode is released by a RESET through a STOP-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD     P2M, #1XXX XXXXB
NOP
STOP
```

X = Dependent on user's application.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF   NOP    ; clear the pipeline
6F   STOP   ; enter STOP mode
or
FF   NOP    ; clear the pipeline
7F   HALT   ; enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every Twdt period; otherwise, the Z86E07 resets itself, The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

WDT = 5F (Hex)

Opcode WDT (5FH). The first time opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every Twdt period; otherwise, the WDT times out and generates a reset. The generated reset is the same as a Power-On Reset of T_{POR}, plus 18 XTAL clock cycles. The WDT does not work in STOP Mode.

6

FUNCTIONAL DESCRIPTION (Continued)

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Auto Reset Voltage (V_{RST}). The Z86E07 has an auto-reset built-in. The auto-reset circuit resets the Z86E07 when it detects the V_{CC} below V_{RST}. Figure 15 shows the Auto Reset Voltage vs temperature. The Z86E07 does not function from V_{RST} to below 4.5V. Upon power-up of the device, the V_{CC} rise time must reach 4.5V before the T_{POR} expires so that program execution begins with the V_{CC} in the range 4.5V to 5.5V.

If the V_{CC} drops below 4.5V while the device is in operation, the device must be powered down and then re-powered up again.

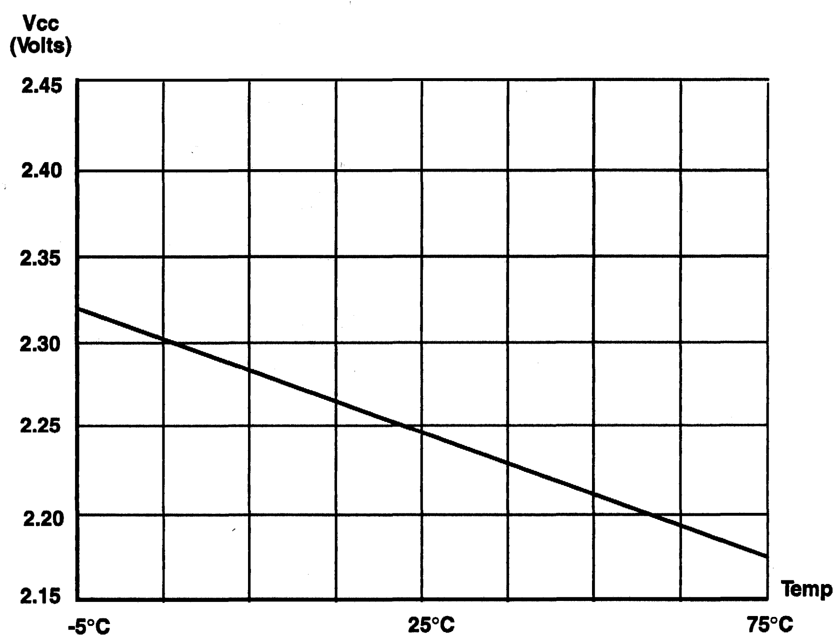


Figure 15. Typical Auto Reset Voltage (V_{RST}) vs Temperature

Low EMI Emission

The Z86E07 can be programmed to operate in a low EMI emission mode by means of an EPROM programmable bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT mode.
- All drivers slew rates reduced to 10 ns (typical).
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Z86E07 offers programmable ROM Protect and programmable Low Noise features. When programmed for Low Noise, the ROM Protect feature is optional.

Besides V_{DD} and GND (V_{SS}), the Z86E07 changes all its pin functions in the EPROM mode. XTAL2 has no function, XTAL1 functions as /CE, P31 functions as /OE, P32 functions as EPM, P33 functions as V_{PP}, and P02 functions as /PGM.

EPROM Protect. ROM Protect fully protects the Z86E07 ROM code from being read externally. When ROM Protect is selected, the Z86E07 will disable the instructions LDC and LDCI (Z86E07 and Z86C08 do not support the instructions of LDE and LDEI). When the device is programmed for ROM Protect, the Low Noise feature will automatically be enabled. A ROM look-up table cannot be used when EPROM Protect is selected.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM, /CE, /OE pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP mode. The V_{PP} requires both a diode and a 100 pF capacitor.

User Modes. Table 5 shows the programming voltage of each mode of Z86E07.

Table 5. OTP Programming Table

Programming Modes	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ1	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V
EPROM READ2	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V
PROGRAM	V_H	X	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.0V
PROGRAM VERIFY	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
EPROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
LOW NOISE SELECT	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	6.0V

Notes:
V_H = 12.5V ±0.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.

6

SPECIAL FUNCTIONS

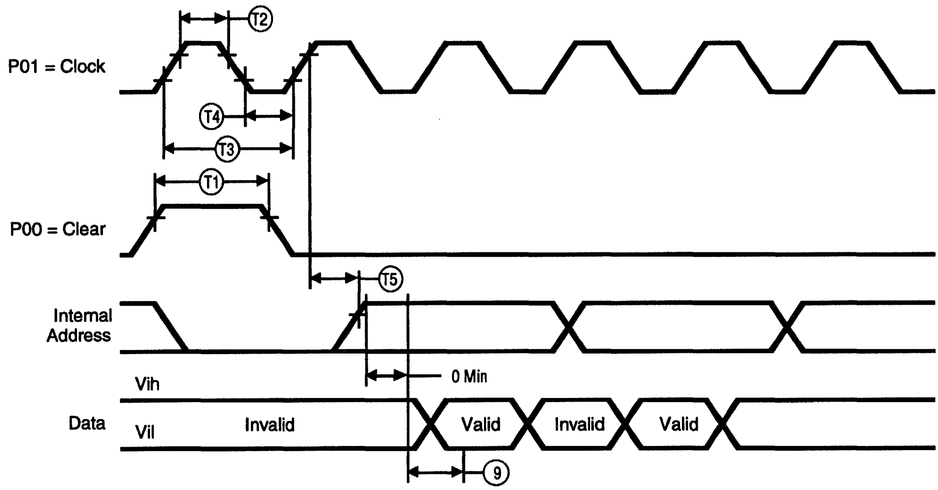
Internal Address Counter. The address of Z86E07 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 16 shows the set-up time of the serial address input.

Programming Waveform. Figures 17, 18 and 19 show the programming waveforms of each mode. Table 6 shows the timing of programming waveforms.

Programming Algorithm. Figure 20 shows the flow chart of the Z86E07 programming algorithm.

Table 6. Timing of Programming Waveforms

Parameter	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	30 ns Min
T3 Input Clock Period	70 ns Min
T4 Input Clock Low	30 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max

Figure 16. Z86E07 Address Counter Waveform

6

SPECIAL FUNCTIONS (Continued)

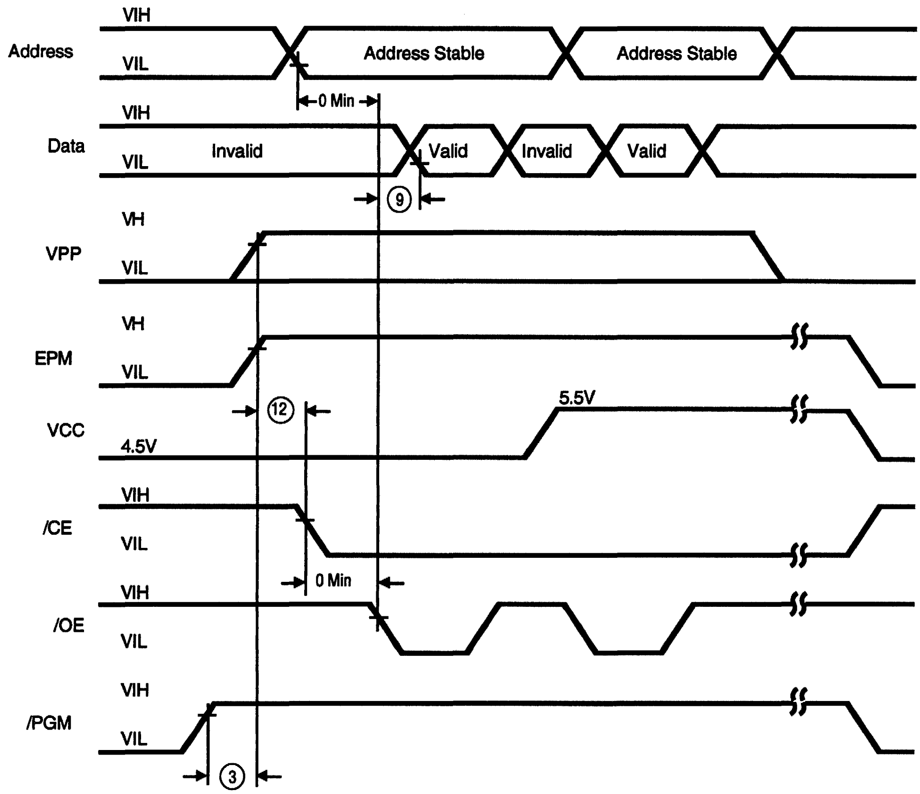


Figure 17. Z86E07 Programming Waveform (EPROM Read)

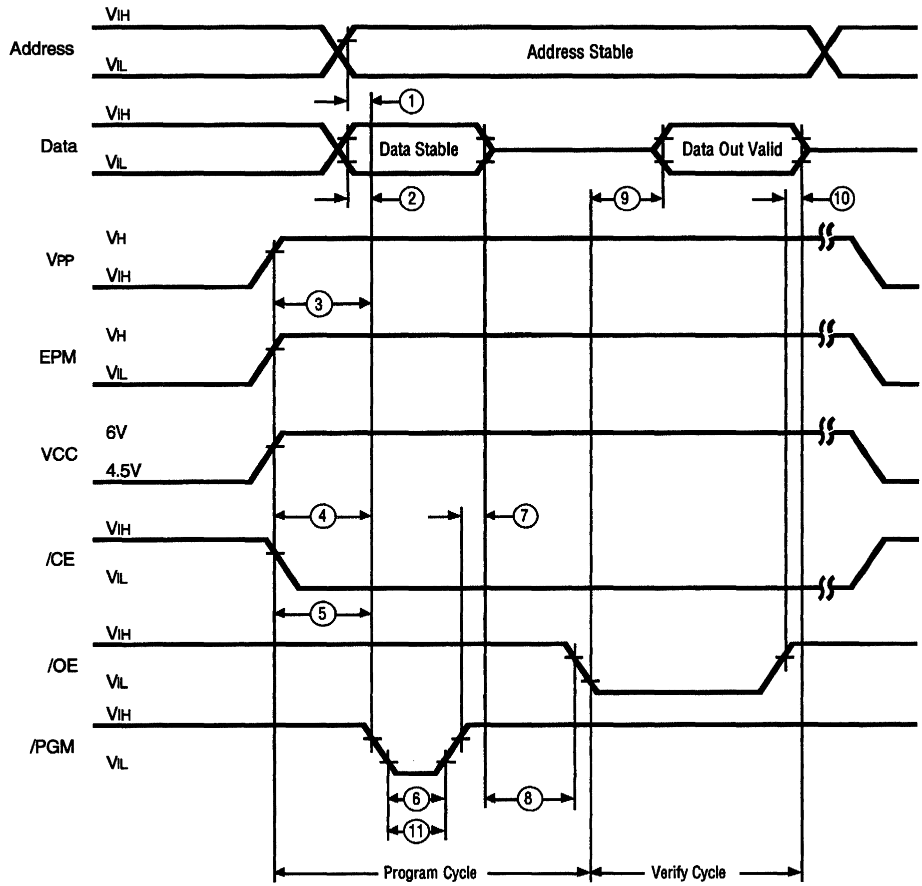


Figure 18. Z86E07 Programming Waveform (Program and Verify)

6

SPECIAL FUNCTIONS (Continued)

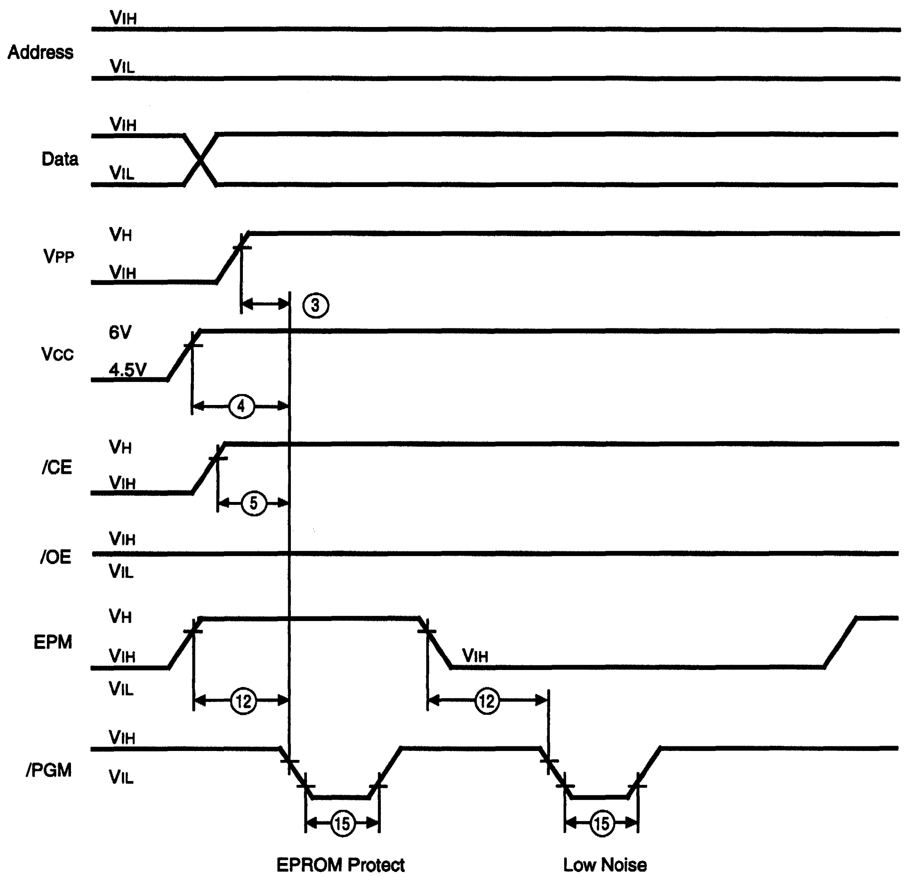
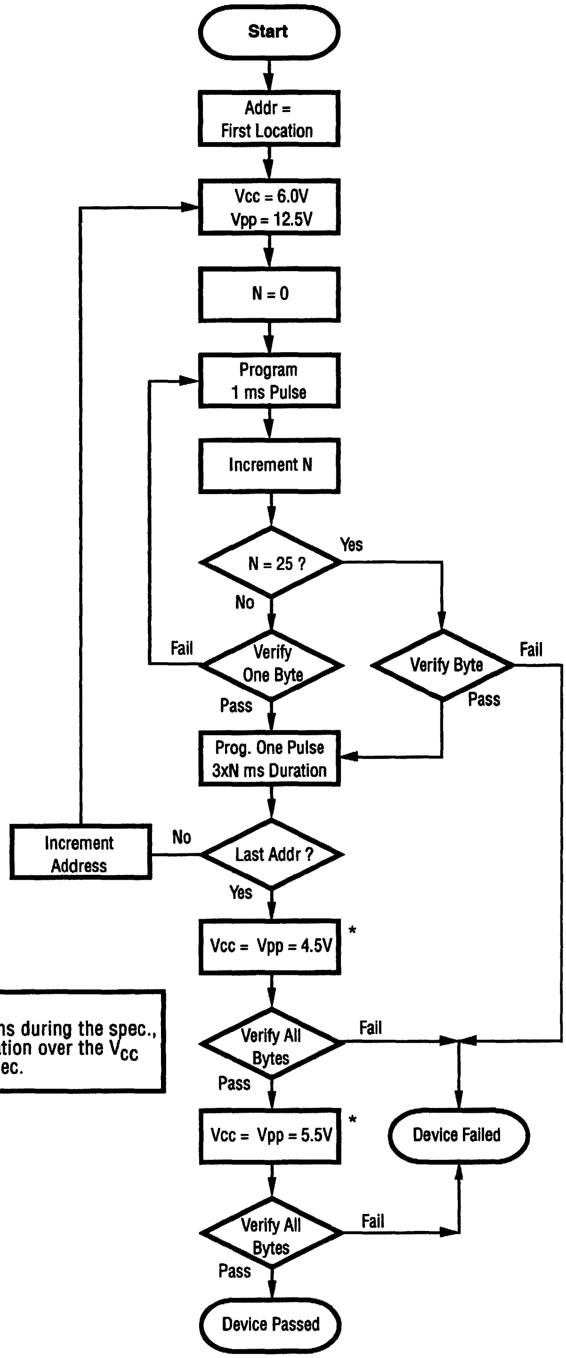


Figure 19. Z86E07 Programming Waveform (EPROM Protect and Low EMI Program)



Note:
* To ensure proper operations during the spec., Zilog recommends verification over the V_{CC} range of the device V_{CC} spec.

Figure 20. Z86E07 Programming Algorithm

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+12	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on Pin 7, 8, 9, 10 with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		462	mW
Maximum Current out of V_{SS}		84	mA
Maximum Current into V_{DD}		84	mA
Maximum Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Output Current Sinked by Any I/O Pin		12	mA
Maximum Output Current Sourced by Any I/O Pin		12	mA
Total Maximum Output Current Sinked by Port 2		70	mA
Total Maximum Output Current Sourced by Port 2		70	mA

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

Notes:
[1] This applies to all pins except where otherwise noted. Maximum current into pin must be ±600µA.
[2] There is no input protection diode from pin to V_{DD} (not applicable to EPROM Mode).
[3] This excludes Pin 6 and Pin 7.
[4] Device pin is not at an output Low state.

Total Power dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})] + sum of [(V_{DD} – V_{OH}) x I_{OH}] + sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 21).

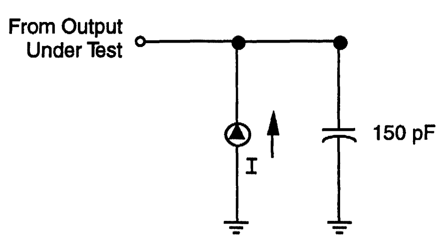


Figure 21. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}[3]	T_A = 0°C to +70°C Min	Max	Typical [11] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.8 V_{CC}	V_{CC}+0.3	2.4	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.6		Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	2.3	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.1	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.7	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.2	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		3.9	V	I_{OH} = –2.0 mA	[9]
		5.5V	V_{CC}–0.4		5.4	V	I_{OH} = –2.0 mA	[9]
V_{OH}	Output Low Voltage	4.5V	V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	[10]
		5.5V	V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	[10]
V_{OL}	Output Low Voltage	4.5V		0.4		V	Low Noise @ I_{OL} = +1 mA	[10]
		5.5V		0.4		V	Low Noise @ I_{OL} = +1 mA	[10]
V_{OL1}	Output Low Voltage	4.5V		0.4	0.2	V	I_{OL} = +4.0 mA	[9]
		5.5V		0.4	0.2	V	I_{OL} = +4.0 mA	[9]
V_{OL2}	Output Low Voltage	4.5V		1.0	0.7	V	I_{OL} = +12 mA, 3 Pin Max	[9]
		5.5V		0.8	0.5	V	I_{OL} = +12 mA, 3 Pin Max	[9]
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	6	mV		
		5.5V		25	7	mV		
V_{RST}	Auto Reset Voltage		1.55	2.7	2.4	V		
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V	–1.0	1.0	1.0	µA	0V<V_{IN}<V_{CC}	
		5.5V	–1.0	1.0	1.0	µA	0V<V_{IN}<V_{CC}	
I_{OL}	Output Leakage	4.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Input Common Mode Voltage Range		0	V_{CC}–1.0		V		

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}[3]	T_A = 0°C to +70°C Min	Max	Typical[11] @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current (Standard Mode)	4.5V		4.0	2.2	mA	All Output and I/O Pins Floating @ 2 MHz	[4,5,8,9]
		5.5V		7.0	5.0	mA	All Output and I/O Pins Floating @ 2 MHz	[4,5,8,9]
		4.5V		9.0	4.5	mA	All Output and I/O Pins Floating @ 8 MHz	[8,9]
		5.5V		11.0	8.3	mA	All Output and I/O Pins Floating @ 8 MHz	[8,9]
		4.5V		10	6.1	mA	All Output and I/O Pins Floating @ 12 MHz	[8,9]
		5.5V		15	10.8	mA	All Output and I/O Pins Floating @ 12 MHz	[8,9]
I_{CC1}	Standby Current (Standard Mode)	4.5V		2.5	0.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	[4,5,8,9]
		5.5V		4.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	[4,5,8,9]
		4.5V		4.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	[8,9]
		5.5V		5.0	2.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	[8,9]
		4.5V		5.0	1.3	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	[8,9]
		5.5V		7.0	2.3	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	[8,9]
I_{CC}	Supply Current (Low Noise Mode)	4.5V		4.0	2.2	mA	All Output and I/O Pins Floating @ 1 MHz	[4,5,8,10]
		5.5V		7.0	4.2	mA	All Output and I/O Pins Floating @ 1 MHz	[4,5,8,10]
		4.5V		6.0	2.9	mA	All Output and I/O Pins Floating @ 2 MHz	[4,5,8,10]
		5.5V		9.0	5.5	mA	All Output and I/O Pins Floating @ 2 MHz	[4,5,8,10]
		4.5V		8.0	4.4	mA	All Output and I/O Pins Floating @ 4 MHz	[4,5,8,10]
		5.5V		11.0	7.9	mA	All Output and I/O Pins Floating @ 4 MHz	[4,5,8,10]

Symbol	Parameter	V_{CC}[3]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		1.2	0.4	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	[4,5,8,10
		5.5V		1.6	0.9	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	[4,5,8,10
		4.5V		1.5	0.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	[4,5,8,10
		5.5V		1.9	1	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	[4,5,8,10
		4.5V		2.0	0.8	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz	[4,5,8,10
		5.5V		2.4	1.3	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz	[4,5,8,10
I_{CC2}	Standby Current	4.5V		10	1.0	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running	[4,5,8,10
		5.5V		10	1.0	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running	[4,5,8,10
I_{ALL}	Auto Latch Low Current	4.5V		10	6.0	µA	0V < V_{IN} < V_{CC}	
		5.5V		15	11.5	µA	0V < V_{IN} < V_{CC}	
I_{ALH}	Auto Latch High Current	4.5V		-7.0	–3.3	µA	0V < V_{IN} < V_{CC}	
		5.5V		-7.0	-6.5	µA	0V < V_{IN} < V_{CC}	

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3	5.0	mA	8 MHz
Crystal or XTAL Resonator	3.0	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND
[3] V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum T_{POR} time-out. V_{CC} is specified at 4.5V to 5.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF.
[6] Same as Note [4] except inputs at V_{CC}.
[7] Except clock pins and Port 3 input pins unless in EPROM Mode.
[8] Using resonator/or crystal (not by Clock Driver).
[9] Standard Mode (Low EMI not selected).
[10] Low EMI selected.
[11] Typical is V_{CC} = 5.0V; Temperature = 25°C.
[12] For comparator inputs, the inputs must be in the common-mode range.
[13] A 10 Megohm pull-down resistor may be required on the XTAL1 clock input pin.

AC ELECTRICAL CHARACTERISTICS

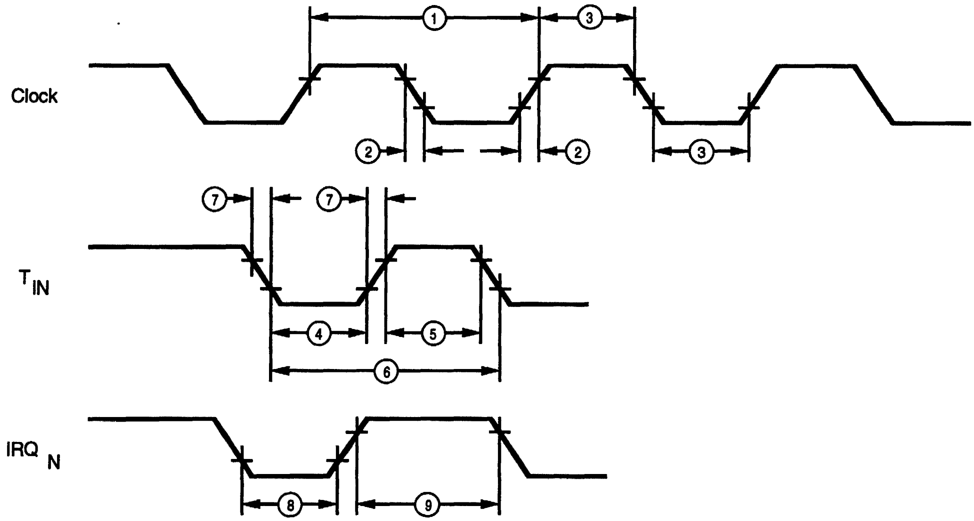


Figure 22. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS
Low Noise Mode

				T_A = 0°C to +70°C					
				1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}[3]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	1000	DC	250	DC	ns	[1]
			5.5V	1000	DC	250	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	[1]
			5.5V		25		25	ns	
3	TwC	Input Clock Width	4.5V	500		125		ns	[1]
			5.5V	500		125		ns	[1]
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			[1]
			5.5V	4TpC		4TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	4.5V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	4.5V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	4.5V	15		15		ms	[1,3]
			5.5V	10		10		ms	[1,3]
11	TPOR	Power-On Reset Time	4.5V	15		10		ms	[1]
			5.5V	15		10		ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] Delay time between WDT refresh.

6

AC ELECTRICAL CHARACTERISTICS
Standard Mode, Standard Temperature

				T_A = 0°C to +70°C					
				8 MHz		12 MHz			
No	Symbol	Parameter	V_{cc}[3]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	[1]
			5.5V	125	DC	83	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	[1]
			5.5V		25		15	ns	
3	TwC	Input Clock Width	4.5V	62		41		ns	[1]
			5.5V	62		41		ns	[1]
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1]
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			[1]
			5.5V	8TpC		8TpC			[1]
7	TrTin, TfTin	Timer Input Rise and Fall Timer	4.5V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	4.5V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	4.5V	15		15		ms	[1,3]
			5.5V	10		10		ms	[1,3]
11	TPOR	Power-On Reset Timer	4.5V	15		10		ms	[1]
			5.5V	15		10		ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31)
[3] Delay time between WDT refresh.

Z8® CONTROL REGISTERS

R241 TMR

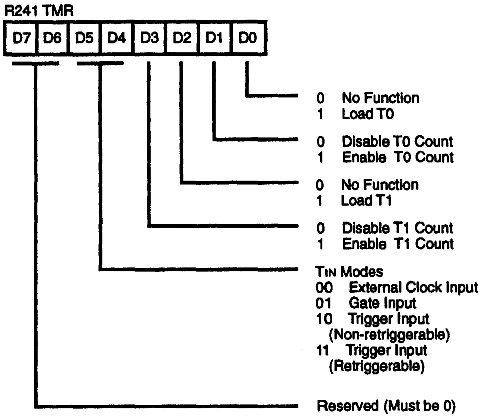


Figure 23. Timer Mode Register ($F1_H$: Read/Write)

R242 T1

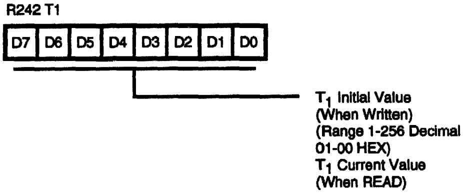


Figure 24. Counter Timer 1 Register ($F2_H$: Read/Write)

R243 PRE1

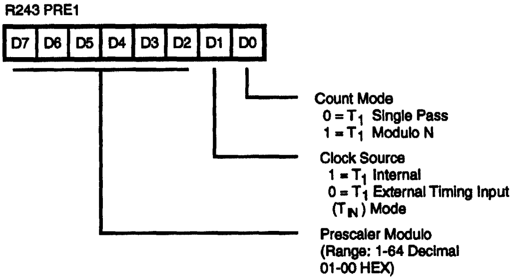


Figure 25. Prescaler 1 Register ($F3_H$: Write Only)

R244 T0

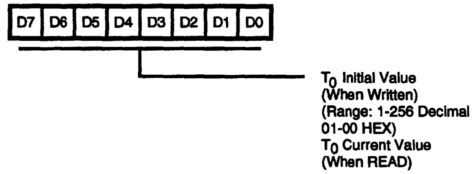


Figure 26. Counter/Timer 0 Register ($F4_H$: Read/Write)

R245 PRE0

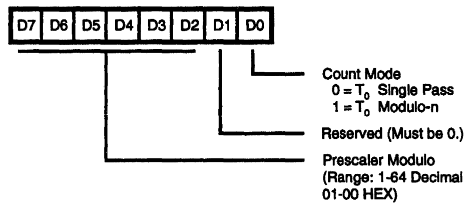


Figure 27. Prescaler 0 Register ($F5_H$: Write Only)

R246 P2M

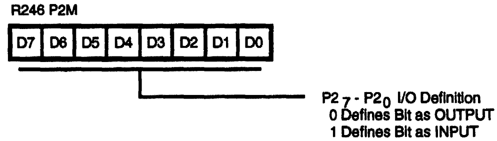


Figure 28. Port 2 Mode Register ($F6_H$: Write Only)

R247 P3M

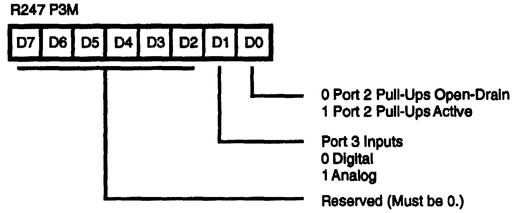


Figure 29. Port 3 Mode Register ($F7_H$: Write Only)

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Z8 CONTROL REGISTERS (Continued)

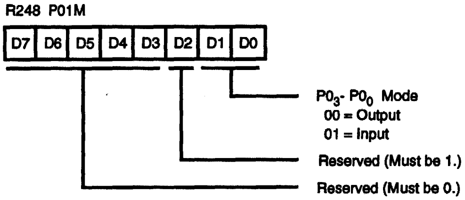


Figure 30. Port 0 and 1 Mode Register ($F8_H$: Write Only)

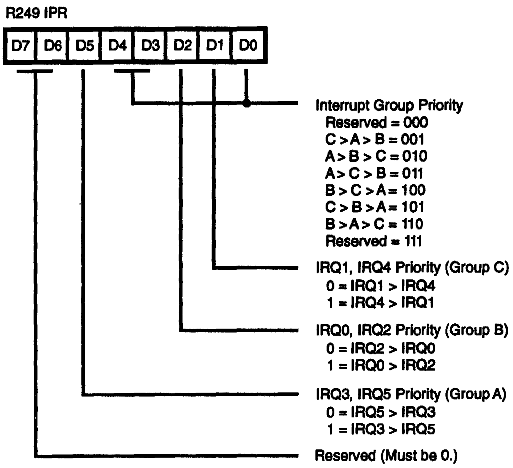


Figure 31. Interrupt Priority Register ($F9_H$: Write Only)

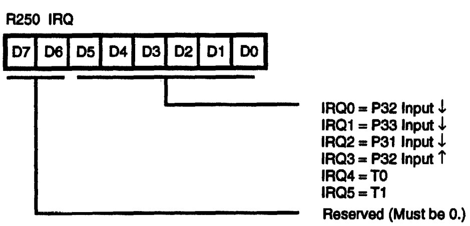


Figure 32. Interrupt Request Register (FA_H: Read/Write)

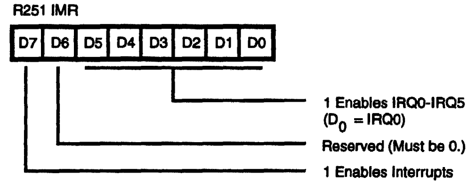


Figure 33. Interrupt Mask Register (FB_H: Read/Write)

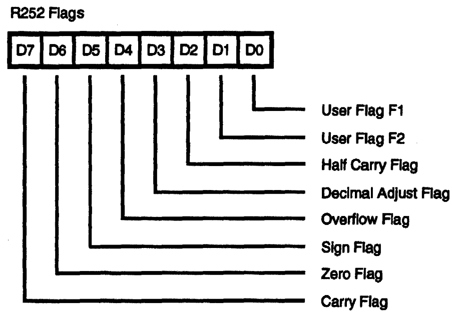


Figure 34. Flag Register (FC_H: Read/Write)

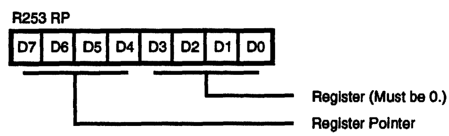


Figure 35. Register Pointer (FD_H: Read/Write)

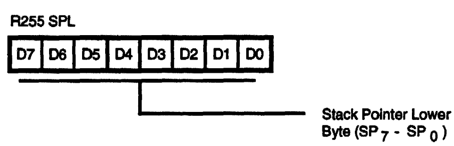


Figure 36. Stack Pointer (FF_H: Read/Write)

OPERATING MODES

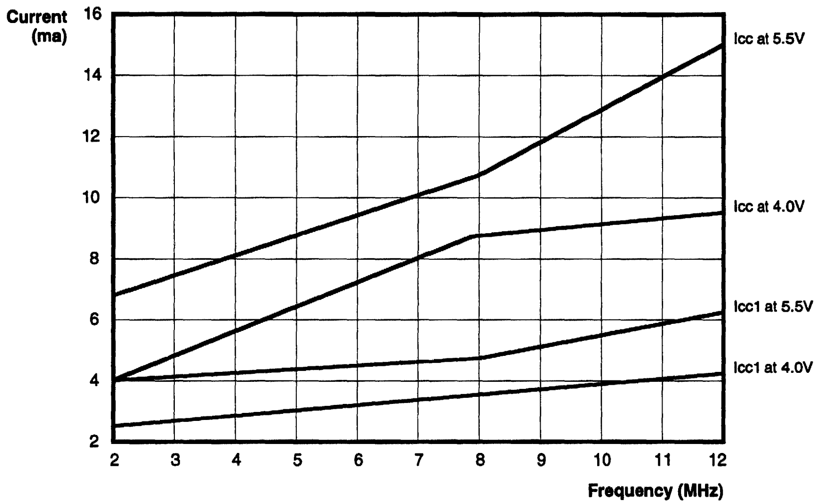


Figure 37. Maximum I_{CC} and I_{CC1} vs Frequency in Standard Mode

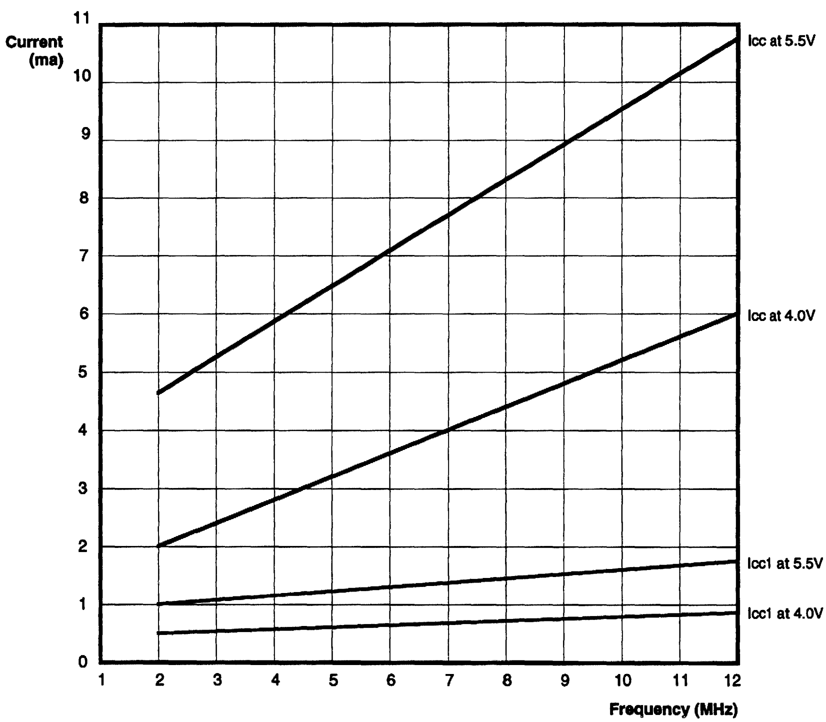


Figure 38. Typical I_{CC} and I_{CC1} vs Frequency in Standard Mode

OPERATING MODES (Continued)

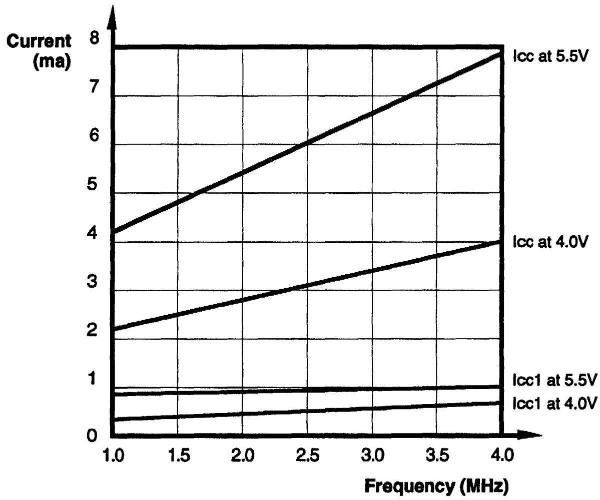


Figure 39. Typical I_{CC} and I_{CC1} vs Frequency in Low EMI Mode

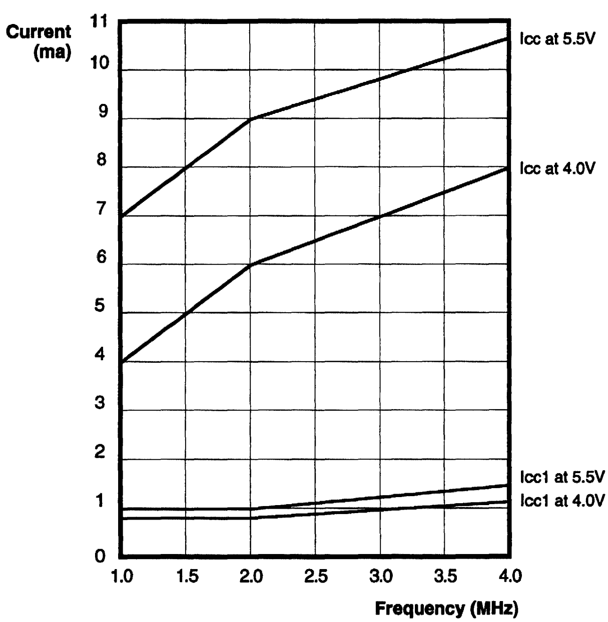


Figure 40. Maximum I_{CC} and I_{CC1} vs Frequency in Low EMI Mode

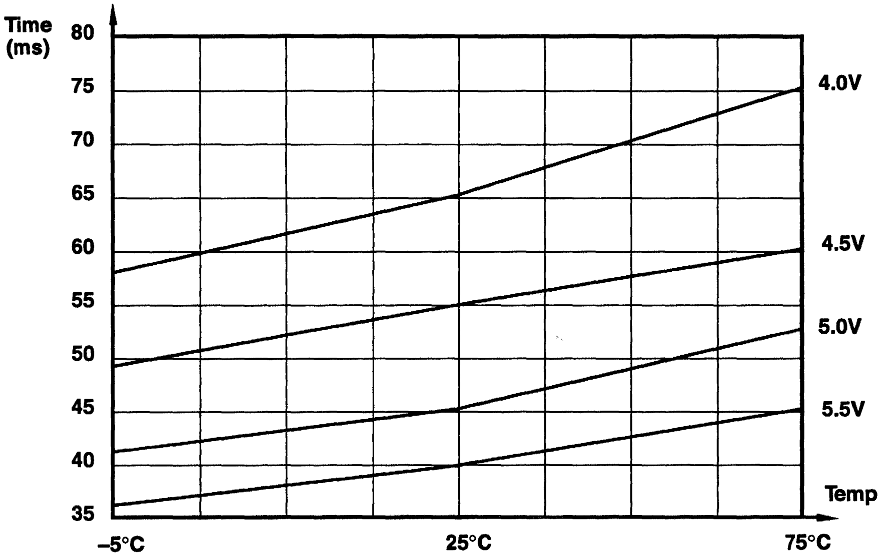


Figure 41. Typical POR Time Out Period vs Temperature

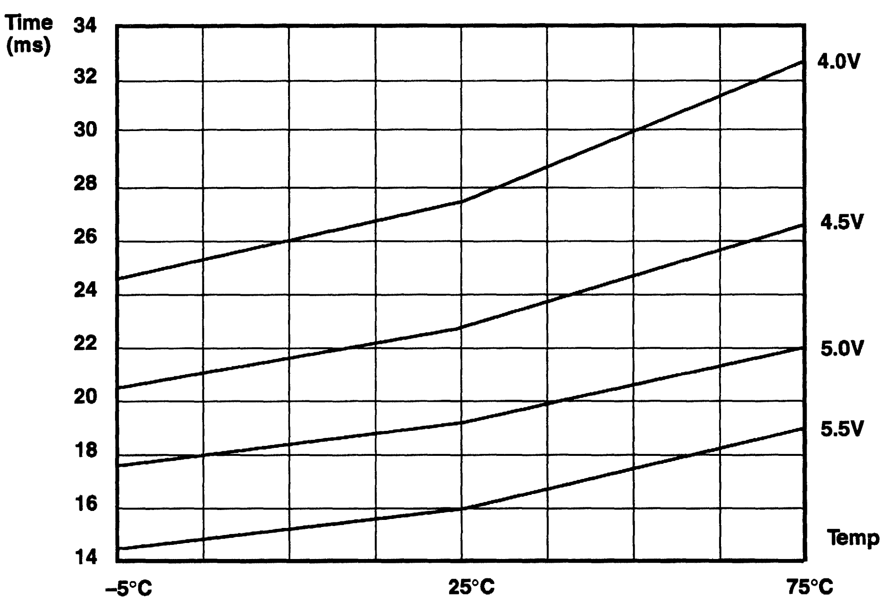


Figure 42. Typical WDT Time Out Period vs Temperature

6

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

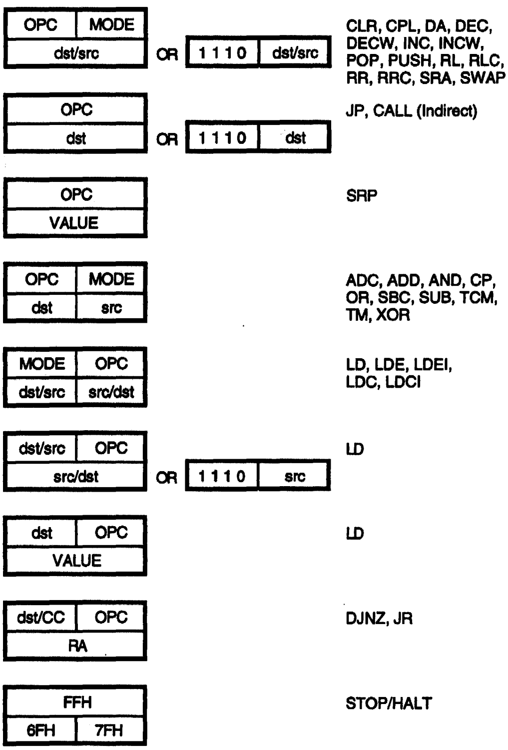
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

CONDITION CODES

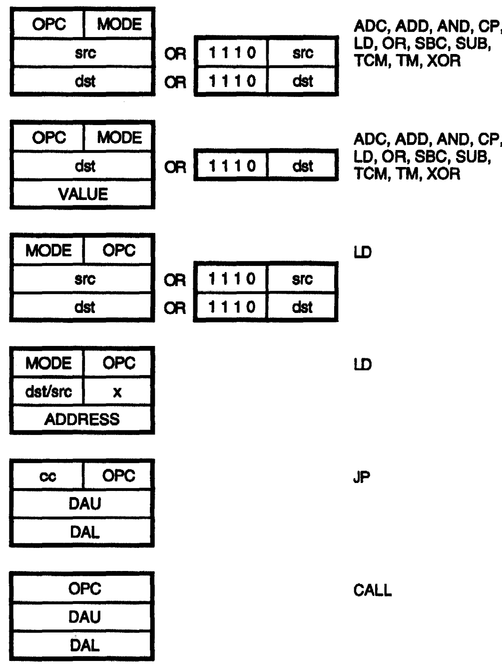
Value	Mnemonic	Meaning	Flags Set
1000	---	Always true	---
0111	C	Carry	C=1
1111	NC	No Carry	C=0
0110	Z	Zero	Z=1
1110	NZ	Not zero	Z=0
1101	PL	Plus	S=0
0101	MI	Minus	S=1
0100	OV	Overflow	V=1
1100	NOV	No overflow	V=0
0110	EQ	Equal	Z=1
1110	NE	Not equal	Z=0
1001	GE	Greater than or equal	(S XOR V)=0
0001	LT	Less than	(S XOR V)=1
1010	GT	Greater than	[Z OR (S XOR V)]=0
0010	LE	Less than or equal	[Z OR (S XOR V)]=1
1111	UGE	Unsigned greater than or equal	C=0
0111	ULT	Unsigned less than	C=1
1011	UGT	Unsigned greater than	(C = 0 AND Z=0)=1
0011	ULE	Unsigned less than or equal	(C OR Z)=1
0000	F	Never true (Always False)	---

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst(7)

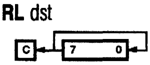
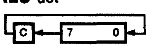
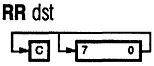
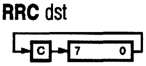
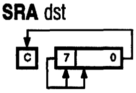
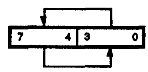
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst + src +C	†		1[ ]	* * * * 0 *
ADD dst, src dst←dst + src	†		0[ ]	* * * * 0 *
AND dst, src dst←dst AND src	†		5[ ]	- * * 0 - -
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	- - - - - - -
CCF C←NOT C			EF	* - - - - -
CLR dst dst←0	R IR		B0 B1	- - - - - - -
COM dst dst←NOT dst	R IR		60 61	- * * 0 - -
CP dst, src dst – src	†		A[ ]	* * * * - -
DA dst dst←DA dst	R IR		40 41	* * * X - -
DEC dst dst←dst – 1	R IR		00 01	- * * * - -
DECW dst dst←dst – 1	RR IR		80 81	- * * * - -
DI IMR(7)←0			8F	- - - - - - -
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 - F	- - - - - - -
EI IMR(7)←1			9F	- - - - - - -
HALT			7F	- - - - - - -
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	- * * * - -
INCW dst dst←dst + 1	RR IR		A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	* * * * * *
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	- - - - - - -
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	- - - - - - -
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - - -
LDC dst, src dst←src	r	Irr	C2	- - - - - - -
LDCI dst, src dst←src r←r + 1; rr←rr + 1	Ir	Irr	C3	- - - - - - -

6

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
NOP		FF	- - - - - -
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -
POP dst dst←@SP; SP←SP + 1	R IR	50 51	- - - - - -
PUSH src SP←SP – 1; @SP←src	R IR	70 71	- - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP + 2		AF	- - - - - -
RL dst 	R IR	90 91	* * * * - -
RLC dst 	R IR	10 11	* * * * - -
RR dst 	R IR	E0 E1	* * * * - -
RRC dst 	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst–src–C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst 	R IR	D0 D1	* * * 0 - -
SRP dst RP←src	Im	31	- - - - - -
STOP		6F	1 - - - - -
SUB dst, src dst←dst—src	†	2[ ]	* * * * 1 *
SWAP dst 	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
WDH		4F	- - - - - -
WDT		5F	- X X X - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

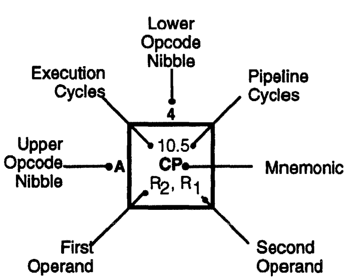
Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) (columns) / **Upper Nibble (Hex)** (rows)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								4.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								5.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1	6.5 **LD** Ir1, r2			10.5 **LD** R2, IR1										6.0 **NOP**

Bytes per Instruction: columns 0–3: 2; columns 4–7: 3; columns 8–C: 2; column D: 3; columns E–F: 1



Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_1 = Dst address
R_2 or r_2 = Src address

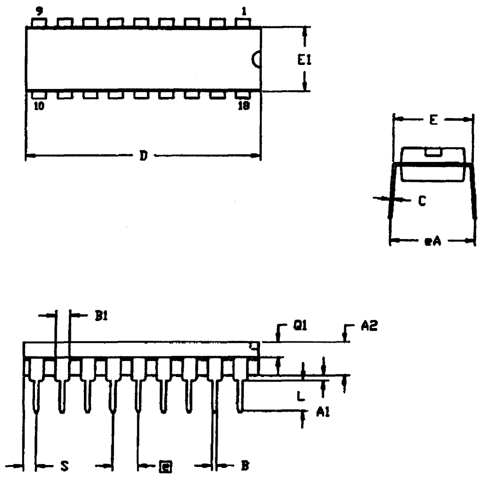
Sequence:
Opcode, First Operand,
Second Operand

Note: Blank areas are reserved.

* 2-byte instruction appears as a 3-byte instruction

6

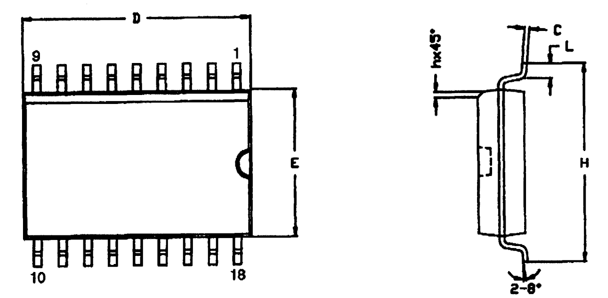
PACKAGE INFORMATION

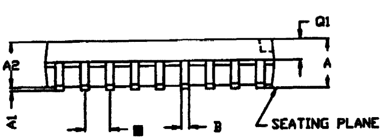


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86E07 (12 MHz)

Standard Temperature	
DIP	**SOIC**
Z86E0712PSC	Z86E0712SSC

For fast results, contact your local Zilog sales office or technical center for assistance in ordering the part desired.

CODES

Preferred Package
P = DIP

Longer Lead Time
S = SOIC

Preferred Temperature
S = 0°C to +70°C

Speed
12 = 12 MHz

Environmental
C= Plastic Standard

Example:
Z 86E07 12 P S C is a Z86E07, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 12 — Speed
- 86E07 — Product Number
- Z — Zilog Prefix

Z86C03/C06 CMOS Z8® 8-Bit CCP™
Consumer Controller Processors

1

Z86E03/E06 CMOS Z8® 8-Bit OTP CCP™
Consumer Controller Processors

2

Z86C04/C08 CMOS Z8® Low Cost
1K /2K ROM Microcontrollers

3

Z86E04/E08 CMOS Z8®
8-Bit OTP Microcontrollers

4

Z86C07 CMOS Z8®
8-Bit Microcontroller

5

Z86E07 CMOS Z8®
8-Bit OTP Microcontroller

6

Z86C30/C31 CMOS Z8® 8-Bit CCP™
Consumer Controller Processors

7

Z86C30/C31

CMOS Z8® 8-BIT CCP™ CONSUMER CONTROLLER PROCESSORS

FEATURES

- The Z86C30/C31 Devices Have the Following General Characteristics:

Part	ROM	RAM	Speed
Z86C30	4 Kbyte	236 Bytes	12 MHz
Z86C31	2 Kbyte	124 Bytes	8 MHz

- 28-Pin Package Styles (DIP, SOIC, PCB Chip Carrier)
- 3.0 to 5.5 Volt Operating Range
- Operating Temperature: –40° to +105°C
- Low Power Consumption: 50 mW (Typical)
- Fast Instruction Pointer: 1.5 µs @ 8 MHz (Z86C31), 1.0 µs @ 12 MHz (Z86C30)
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Two Standby Modes: STOP and HALT
- ROM Protect Option
- RAM Protect Option (Z86C30 Only)
- 24 Input/Output Lines (Two with Comparator Inputs)
- Seven Digital Inputs CMOS Levels, Schmitt-Triggered
- Three Digital Inputs CMOS Levels
- Three Expanded Register File Control Registers
- Low Voltage Protection
- Watch-Dog/Power-On Reset Timers
- Two Comparators with Programmable Interrupt Polarity
- Six Vectored, Priority Interrupts from Six Different Sources
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.
- Software Programmable Low EMI Mode
- Open-Drain Mode on Three Ports
- Auto Latches

GENERAL DESCRIPTION

The Z86C30/C31 CCP™ (Consumer Controller Processors) are members of Zilog's the Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 4K/2K bytes of ROM and 236/124 bytes of RAM for the Z86C30 and Z86C31, respectively, these low cost, low power consumption CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C30/C31 architecture is characterized by Zilog's 8-bit microcontroller core with an Expanded Register File to allow easy access to register mapped peripheral and I/O circuits. These devices offer a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many industrial, automotive, and industrial applications.

For applications demanding powerful I/O capabilities, the Z86C30/C31 provides 24 pins dedicated to input and output. These lines are grouped into three ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake.

GENERAL DESCRIPTION (Continued)

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File. The Register File is composed of 236/124 bytes of general-purpose registers, three I/O port registers and 15 control and status registers. The Expanded Register File consists of three Control registers.

To unburden the system from coping with real-time tasks, such as counting/timing and input/output data communication, the Z86C30/C31 offers two on-chip counter/timers with a large number of user-selectable modes, and on-board comparators to process analog signals with a common reference voltage (Figure 1).

With powerful peripheral features such as on-board comparators, counter/timer(s), Watch-Dog Timer (WDT), the Z86C30/C31 meets the needs of a variety of sophisticated controller applications.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

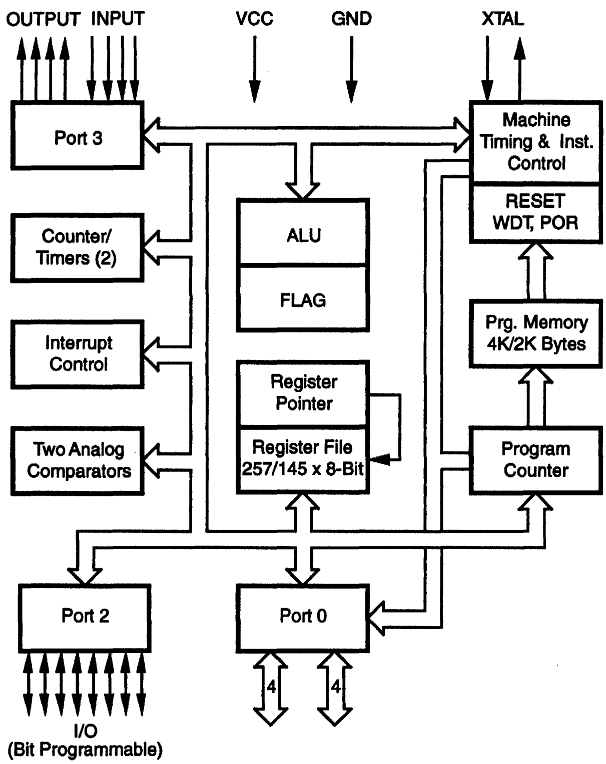


Figure 1. Z86C30/C31 Functional Block Diagram

PIN DESCRIPTION

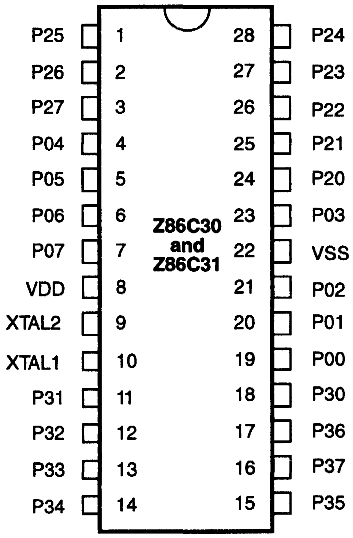


Figure 2. 28-Pin DIP* Pin Configuration

Table 1. 28-Pin DIP* Pin Identification

Pin #	Symbol	Function	Direction
1-3	P25-27	Port 2, Pins 5,6,7	In/Output
4-7	P04-07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P04-07	Port 3, Pins 1,2,3	Fixed Input
14-15	P34-35	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P00-02	Port 0, Pins 0,1,2	In/Output
22	GND	Ground	
23	P03	Port 0, Pins 3	In/Output
24-28	P20-24	Port 2, Pins 0,1,2,3,4	In/Output

Note:
* SOIC style package is identical in pin identification and configuration.

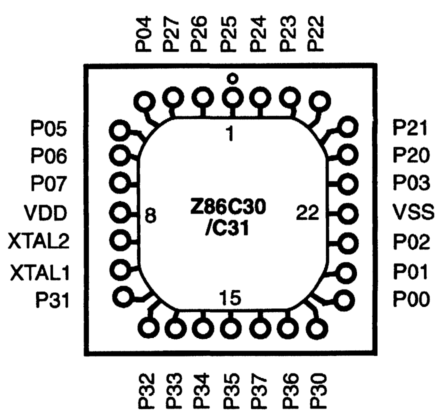


Figure 3. 28-Pin PCB Chip Carrier Pin Configuration

Table 2. 28-Pin PCB Chip Carrier Pin Identification

Pin #	Symbol	Function	Direction
1-3	P25-27	Port 2, Pins 5,6,7	In/Output
4-7	P04-07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P04-07	Port 3, Pins 1,2,3	Fixed Input
14-15	P34-35	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P00-02	Port 0, Pins 0,1,2	In/Output
22	GND	Ground	
23	P03	Port 0, Pins 3	In/Output
24-28	P20-24	Port 2, Pins 0,1,2,3,4	In/Output

PIN FUNCTIONS

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 0 (P07-P00). Port 0 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be nibble programmed as P03-P00 input/output and P07-P04 input/output, separately. The input buffers are Schmitt-Triggered and nibbles programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can also be used as a handshake I/O port.

In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble (Figure 4).

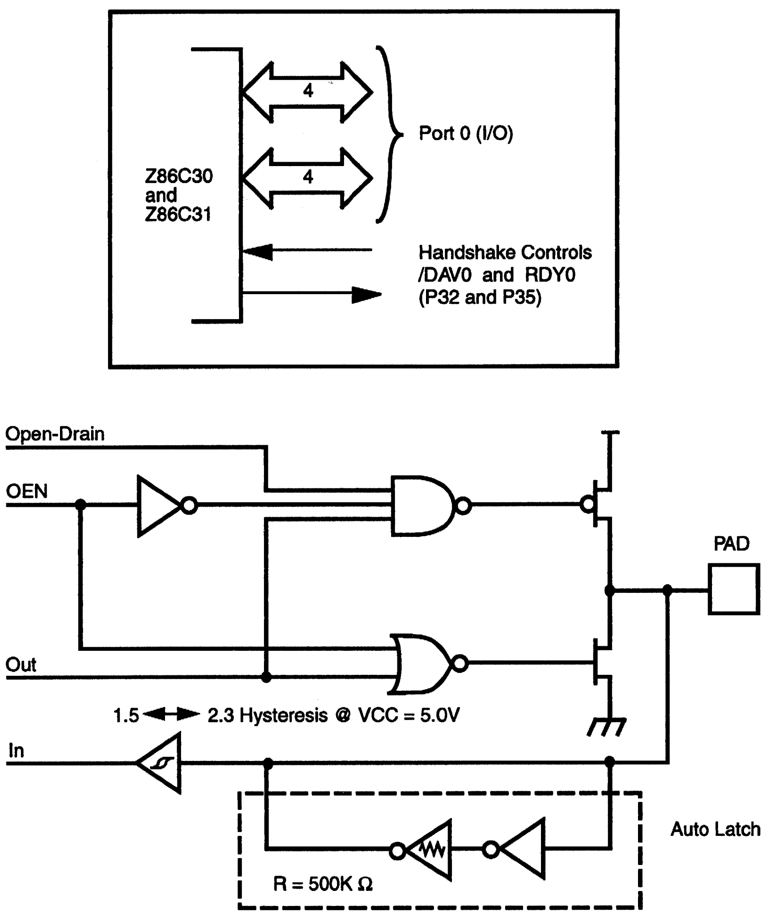


Figure 4. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as inputs or outputs, independently. All input buffers are Schmitt-Triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control. In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 5)

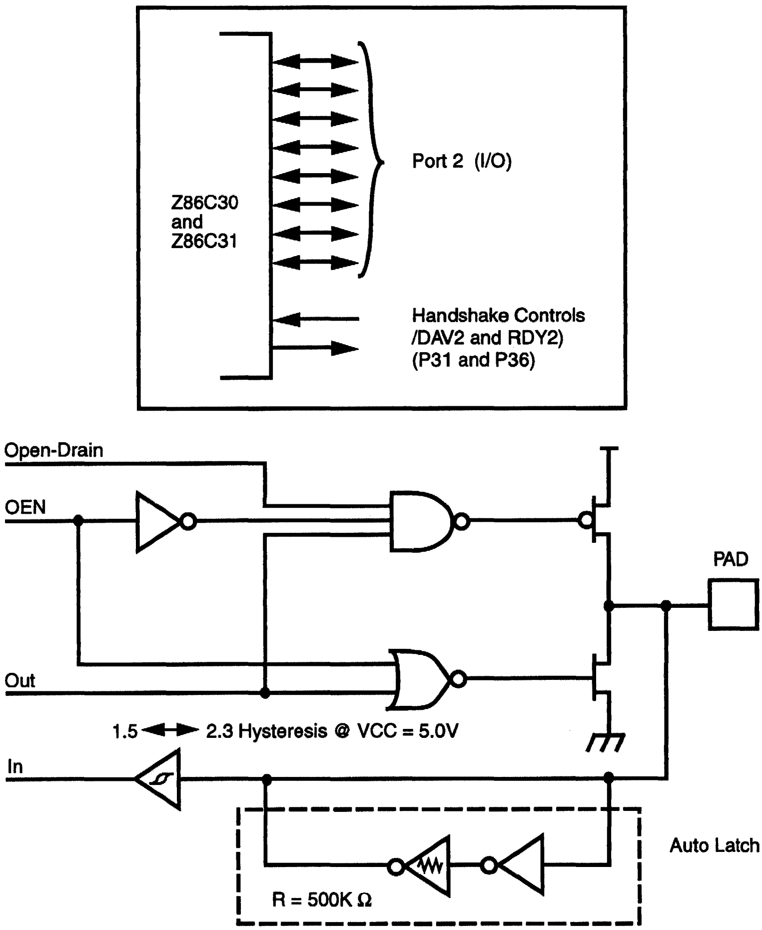


Figure 5. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible port. These eight lines consist of four fixed inputs (P33-P30) and four fixed outputs (P37-P34), and can be configured under software for interrupt and port handshake functions. Port 3 pin 0 input is Schmitt-triggered. Pins P31, P32 and P33 are standard CMOS inputs (no auto latches) and pins P34, P35, P36, P37 are push-pull output lines. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The comparator output can be outputted from P34 and P37, respectively, by setting PCON register (PCON) bit D0 to 1. The analog function is enabled by programming the Port 3 Mode Register (P3M) (bit D1) for interrupt function. P30 and P33 are falling edge interrupt inputs. P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). In Analog Mode, P33 is the comparator reference voltage input.

Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are available on P3 pin 1 through 6 (Figure 6).

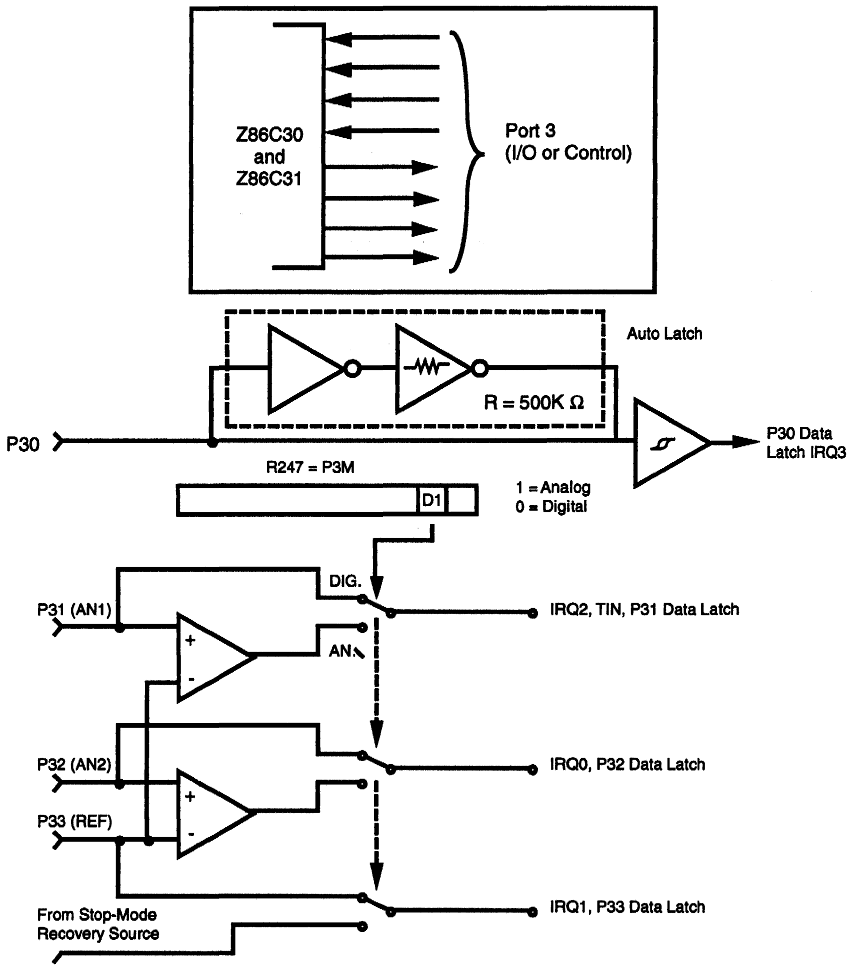


Figure 6. Port 3 Configuration

Table 3. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P2 HS
P30	IN			IRQ3		
P31	IN	T_{IN}	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT		AN1-OUT			
P35	OUT				R/D	
P36	OUT	T_{OUT}				R/D
P37	OUT		AN2-OUT			

Notes:
HS = Handshake Signals
D = DAV
R = RDY

Comparator Inputs. Port 3 Pin P31 and P32 each have a comparator front end. The comparator reference voltage, Pin P33, is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source. The comparator outputs can be programmed out on P34 and P37 by setting the PCON register bit D0 to a 1 state.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. Whether this is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating mode, reduces excessive supply current flow is the input buffer.

Note: Deletion of all port pin auto latches is available as a ROM mask option. The auto latch delete option is selected by the customer when the ROM code is submitted. P01M reg. bit D4 and D3 must be "0" with the Auto Latch Delete option.

Low EMI Emission. The Z86C30/C31 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z86C30/C31 CCPs to enhance the standard Z8® core architecture to provide the user with increased design flexibility.

Reset. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Recovery

Having the auto Power-on Reset circuitry built-in, the Z86C30/C31 does not require an external reset circuit. The reset time is 5 ms (typical), plus 18 clock cycles.

The Z86C30/C31 does not re-initialize WDTMR, SMR, P2M, PCON and P3M registers to their reset values on a Stop-Mode Recovery operation.

Program Memory. The Z86C30/C31 can address up to 4K/2K bytes of internal program memory (Figure 7). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six, 16-bit vectors that correspond to the six available interrupts. Address 12 to 4095/2047 are reserved for the user ROM Program. After reset, the program counter points to the program start address at 000CH.

ROM Protect. The 4K/2K bytes of program memory is mask programmable. **A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC and LDCI instructions to program memory in ALL modes. A ROM look up table cannot be used with this feature selected.**

The ROM protect option is mask-programmable and is selected by the customer when the ROM code is submitted.

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 8). These register groups are known as the Expanded Register File (ERF).

Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of register RP select the working register group (Figure 9). Three system configuration registers reside in the Expanded Register File at bank F (PCON, SMR, WDTMR). The rest of the Expanded Register is not physically implemented and is open for future expansion.

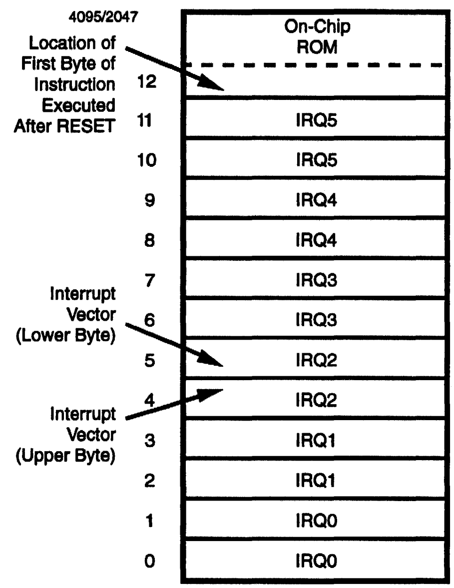
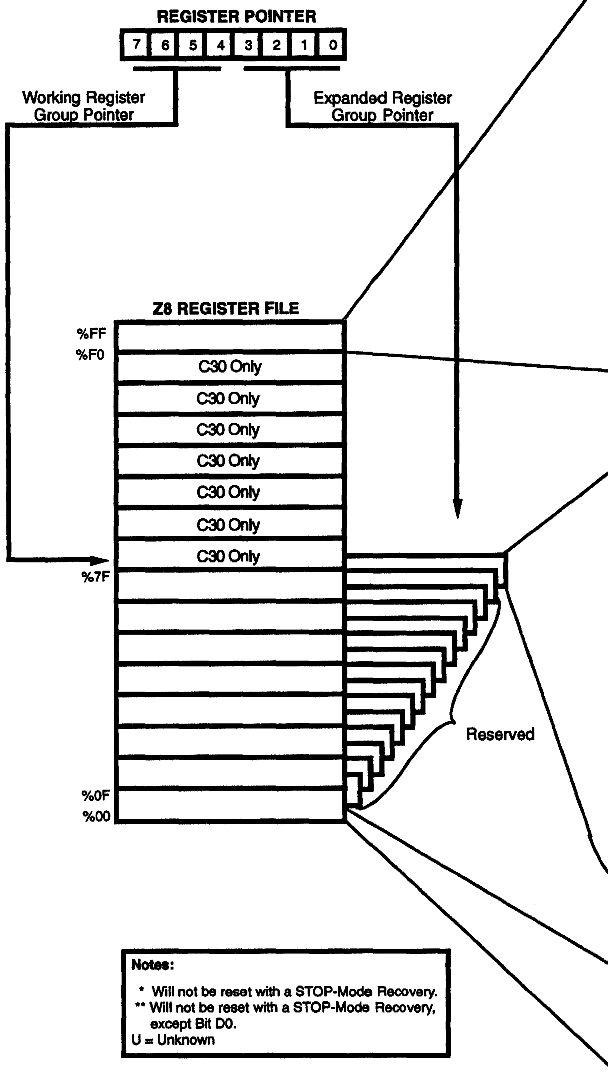


Figure 7. Program Memory Map



Z8® STANDARD CONTROL REGISTERS

	REGISTER		RESET CONDITION D7	D6	D5	D4	D3	D2	D1	D0
	% FF	SPL	U	U	U	U	U	U	U	U
	% FE	GPR	U	U	U	U	U	U	U	U
	% FD	RP	0	0	0	0	0	0	0	0
	% FC	FLAGS	U	U	U	U	U	U	U	U
	% FB	IMR	0	U	U	U	U	U	U	U
	% FA	IRQ	0	0	0	0	0	0	0	0
	% F9	IPR	U	U	U	U	U	U	U	U
	% F8	P01M	0	1	0	0	1	1	0	1
*	% F7	P3M	0	0	0	0	0	0	0	0
*	% F6	P2M	1	1	1	1	1	1	1	1
	% F5	PRE0	U	U	U	U	U	U	U	0
	% F4	T0	U	U	U	U	U	U	U	U
	% F3	PRE1	U	U	U	U	U	U	0	0
	% F2	T1	U	U	U	U	U	U	U	U
	% F1	TMR	0	0	0	0	0	0	0	0
	% F0	Reserved								

EXPANDED REG. GROUP (F)

	REGISTER		RESET CONDITION D7	D6	D5	D4	D3	D2	D1	D0
	% (F) 0F	WDTMR	U	U	U	0	1	1	0	1
	% (F) 0E	Reserved								
	% (F) 0D	Reserved								
	% (F) 0C	Reserved								
**	% (F) 0B	SMR	0	0	1	0	0	0	U	0
	% (F) 0A	Reserved								
	% (F) 09	Reserved								
	% (F) 08	Reserved								
	% (F) 07	Reserved								
	% (F) 06	Reserved								
	% (F) 05	Reserved								
	% (F) 04	Reserved								
	% (F) 03	Reserved								
	% (F) 02	Reserved								
	% (F) 01	Reserved								
*	% (F) 00	PCON	1	1	1	1	1	1	1	0

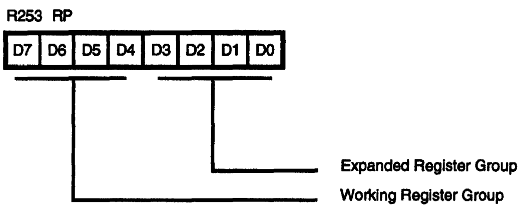
EXPANDED REG. GROUP (0)

	REGISTER		RESET CONDITION D7	D6	D5	D4	D3	D2	D1	D0
*	% (0) 03	P3	1	1	1	1	U	U	U	U
*	% (0) 02	P2	U	U	U	U	U	U	U	U
	% (0) 01	Reserved	U	U	U	U	U	U	U	U
	% (0) 00	P0	U	U	U	U	U	U	U	U

Notes:
* Will not be reset with a STOP-Mode Recovery.
** Will not be reset with a STOP-Mode Recovery, except Bit D0.
U = Unknown

Figure 8. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)



Default setting after RESET = 00000000

Figure 9. Register Pointer Register

Register File. The register file consists of three I/O port registers, 236/124 general-purpose registers and 15 control and status registers and three system configuration registers in the expanded register group (See Figure 8). The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 9 and 10). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group. The general-purpose registers on device power-up are undefined.

Note: Register Bank E0-EF can only be accessed through working register and indirect addressing modes. (This bank is available in Z86C30 only.)

General Purpose Register (GPR). The general purpose registers are undefined after the device is powered-up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general purpose register.

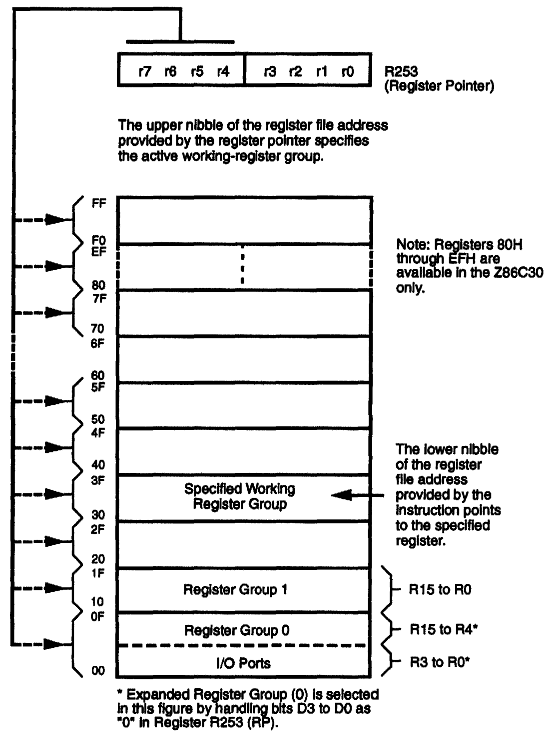


Figure 10. Register Pointer

RAM Protect (Z86C30 Only). The upper portion of the RAM's address spaces %80 to %EF (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

Stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236/124 general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 11).

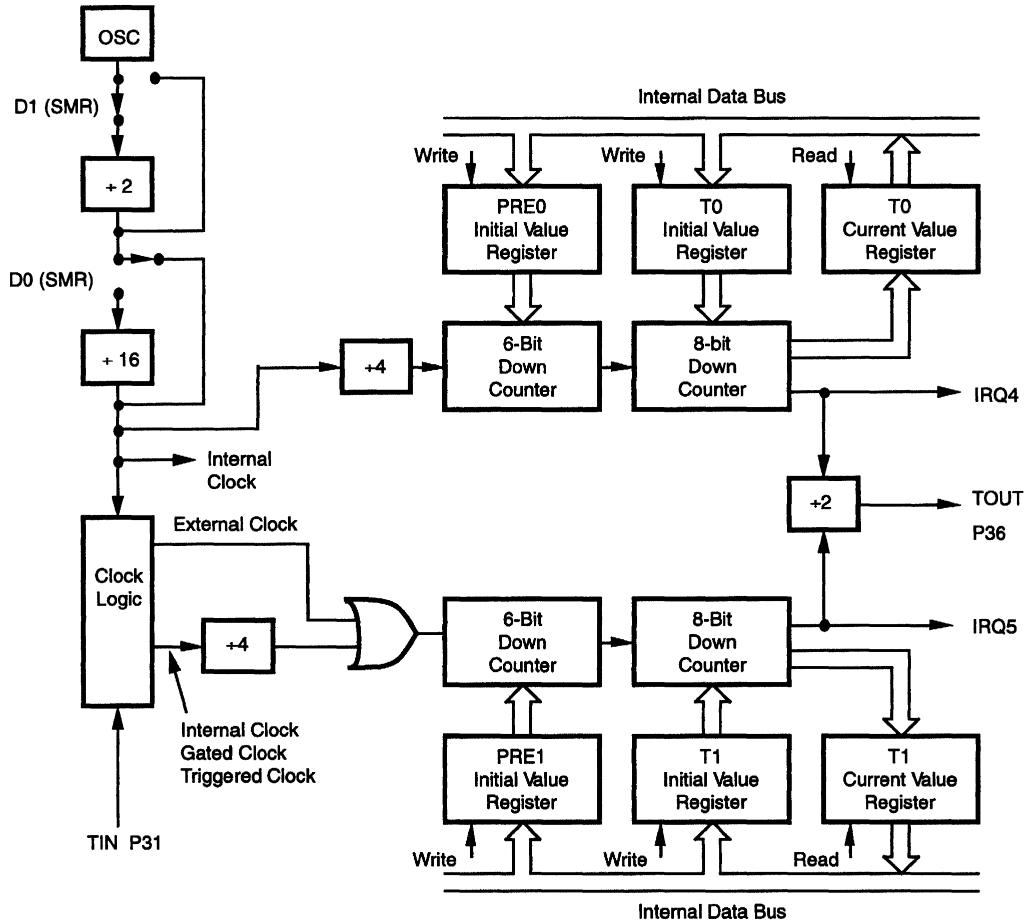


Figure 11. Counter/Timer Block Diagram

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FUNCTIONAL DESCRIPTION (Continued)

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock; a trigger input that can be retriggerable or not-retriggerable; or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock are output. The counter/timers can be cascaded by connecting the T0 output to the input of T1. T_{IN} Mode is enabled by setting R243 PRE1 Bit D1 to 0.

Interrupts. The Z86C30/C31 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 12). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30 and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

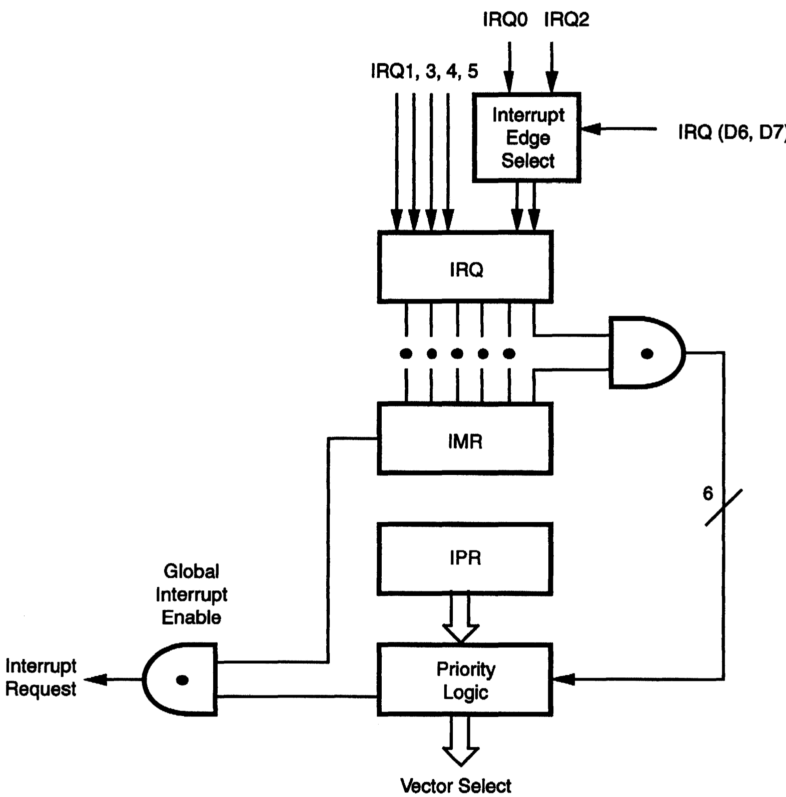


Figure 12. Interrupt Block Diagram

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted; it disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86C30/C31 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 5.

Table 5. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86C30/C31 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 12 MHz max., with a series resistance (RS) less than, or equal to, 100 Ohms. (**Note:** The Z86C31 is 8 MHz max.)

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitors values from each pin directly to Ground, pin 22. This is to reduce ground noise injection. The RC oscillator option is mask-programmable, to be selected by the customer at the time ROM code is submitted. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 13).

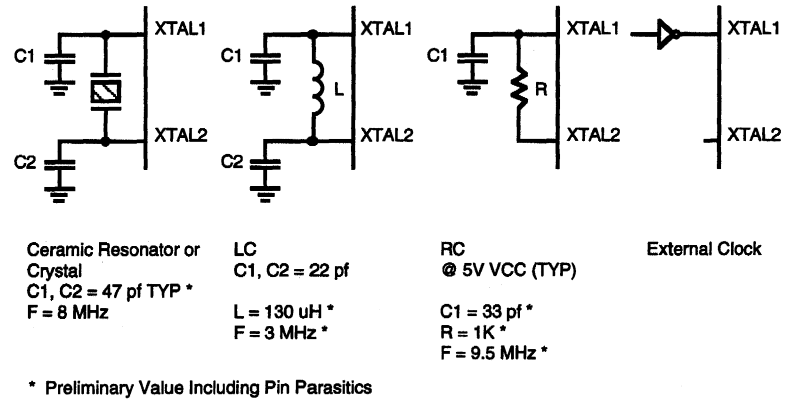


Figure 13. Oscillator Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power-fail to Power-OK status
2. Stop-Mode Recovery (if D5 of SMR=1)
3. WDT time-out

The POR time is T_{POR}. Bit 5 of the STOP mode register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, IRQ2 and IRQ3, remain active. The device may be recovered by interrupts, either external or internal generated.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF  NOP   ; clear the pipeline
6F  STOP  ; enter STOP mode
            or
FF  NOP   ; clear the pipeline
7F  HALT  ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP mode is terminated by a RESET only, either by WDT time-out, POR; or SMR recovery. This causes the processor to restart the application program at address 000C (HEX).

Port Configuration Register (PCON). The Port Configuration Register (PCON) configures the ports individually: Comparator Output on Port 3, Open-Drain on Port 0, Low EMI Noise on Ports 0, 2, and 3, and Low EMI Noise Oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 14).

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P37 and a 0 releases the Port to its standard I/O configuration.

Port 0 Open-Drain (D2). Port 0 is configured as an open-drain by resetting this bit (D2=0) and configured as Pull-up Active by setting D2 = 1. The default value is 1.

Low EMI Port 0 (D3). Port 0 is configured as a Low EMI Port by resetting this bit (D3=0) and configured as a Standard Port by setting D3=1. The default value is 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5=0) and configured as a Standard Port by setting D5=1. The default values is 1.

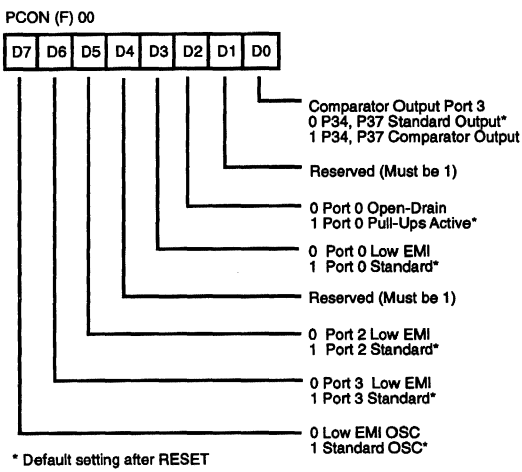


Figure 14. Port Configuration Register (Write Only)

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6=0) and configured as a Standard Port by setting D6=1. The default values is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low-noise drive, it does not affect the relationship of SCLK and XTAL.

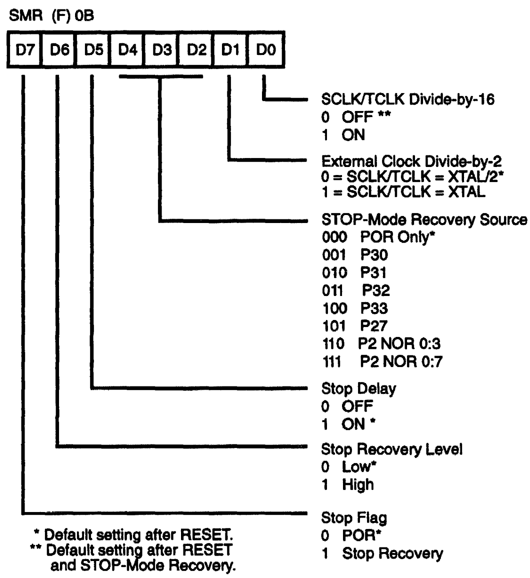


Figure 15. Stop-Mode Recovery Register (Write Only Except Bit D7 Which is Read Only)

7

FUNCTIONAL DESCRIPTION (Continued)

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 15). All bits are Write Only, except Bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power- on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the source of the STOP-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT (Table 7). The SMR is located in bank F of the Expanded Register Group at address OBH.

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (TCLK sources, counter/timers, and interrupt logic). The default setting after either a Reset or a Stop-Mode Recovery is 0.

External Clock Divide-by-2 (D1). This bit can eliminate the oscillator divide-by-2 circuitry. When this bit is 0. SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1 = 1). Using this bit, together with D7 of PCON, further helps lower EMI [i.e., D7 (PCON) = 0, D1 (SMR) = 1]. The default setting is 0.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the STOP-Mode Recovery (Figure 16).

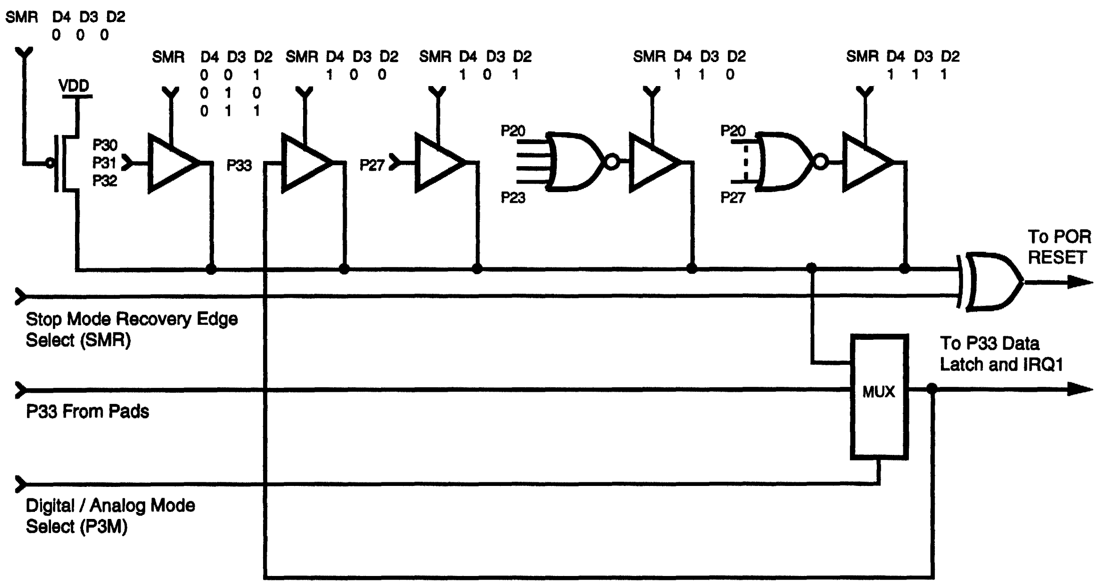


Figure 16. STOP-Mode Recovery Source

Table 6. STOP-Mode Recovery Source

SMR D4	D3	D2	Operation Description of action
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in Analog Mode.)
0	1	1	P32 transition (Not in Analog Mode.)
1	0	0	P33 transition (Not in Analog Mode.)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2, bits 0-3
1	1	1	Logical NOR of Port 2, bits 0-7

STOP-Mode Recovery Delay Select (D5). This bit disables the 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the "fast" wake up is selected, the STOP-Mode Recovery source needs to be kept active for at least 5 TpC.

STOP-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z86C30/C31 from STOP mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 16).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device was reset by POR RESET. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that will reset the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled after it has been initially enabled. The WDT circuit is driven by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (zero), S (sign), V (overflow) flags.

WDT Time Select (D0, D1). Bits 0 and 1 control a tap circuit that determines the time-out period. Table 6 shows the different values that can be obtained. The default value of D0 and D1 are 1 and 0, respectively.

Table 7. Time-out Period of the WDT

D1	D0	Time-out of Internal RC OSC	Time-out of XTAL clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 15 ms.
The values given are for V_{CC} = 5.0V

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during STOP. A 0 will disable the WDT during STOP mode. Since the on-board OSC is stopped during STOP mode, the WDT clock source has to select the on-board RC OSC for the WDT to recover from STOP mode. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

FUNCTIONAL DESCRIPTION (Continued)

WDTMR Register Accessibility. The WDTMR register (Figure 17) is accessible only during the first 64 system clock cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Timer reset or a STOP-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH (Figure 18).

Note: The WDT can be permanently enabled through a mask programming option on the Z86C30/C31. This option is selected by the customer at the time of ROM code submittal. In this mode, WDT is always activated when the device comes out of reset. Execution of the WDT instruction serves to refresh the WDT time-out period. WDT operation in the HALT and STOP modes is controlled by WDTMR programming. If this mask option is not selected at the time of ROM code submission, the WDT must be activated by the user through the WDT instruction and is always disabled by any reset to the device.

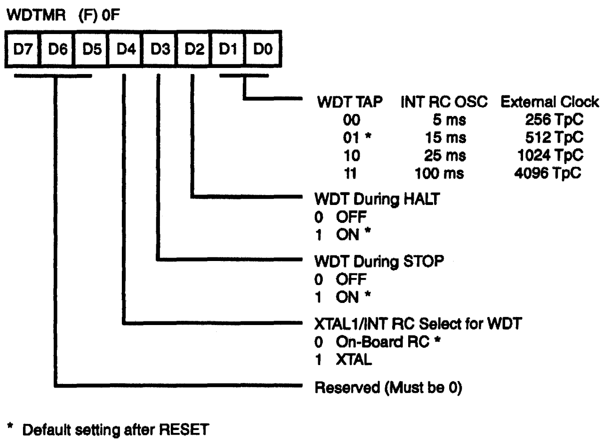


Figure 17. Watch-Dog Timer Mode Register (Write Only)

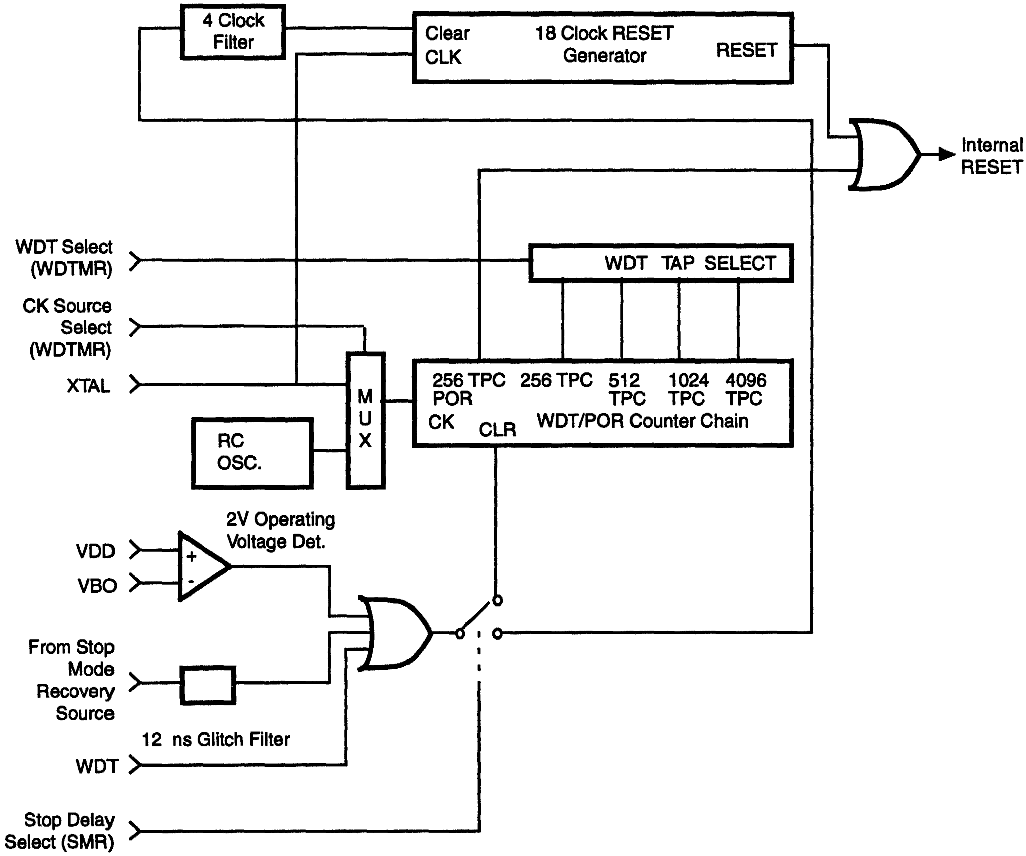


Figure 18. Resets and WDT

FUNCTIONAL DESCRIPTION (Continued)

Low Voltage Protection. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the referenced Low Voltage Protection trip point voltage. The minimum operating voltage for functionality varies with temperature and operating frequency, while the Low Voltage Protection trip point voltage (V_{LV}) varies with temperature only.

The Low Voltage Protection trip voltage (V_{LV}) is less than 3 volts and above 1.4 volts under the following conditions.

Maximum (V_{VL}) Conditions:

Case 1: T_A = –40°C to +105°C, Internal Clock (SCLK) Frequency equal or less than 1 MHz

Case 2: T_A = –40°C to +85°C, Internal Clock (SCLK) Frequency equal to or less than 2 MHz

Note: The internal clock frequency (SCLK) is determined by SMR (F) 0B bit D1.

The Z86C30/C31 functions normally at or above 3.0V under all conditions. Below 3.0V, the devices are guaranteed to function normally until the Low Voltage Protection trip point (V_{LV}) is reached for the temperatures and operating frequencies in Case 1 and Case 2 above. The actual Low Voltage Protection trip point is a function of temperature and process parameters (Figure 19).

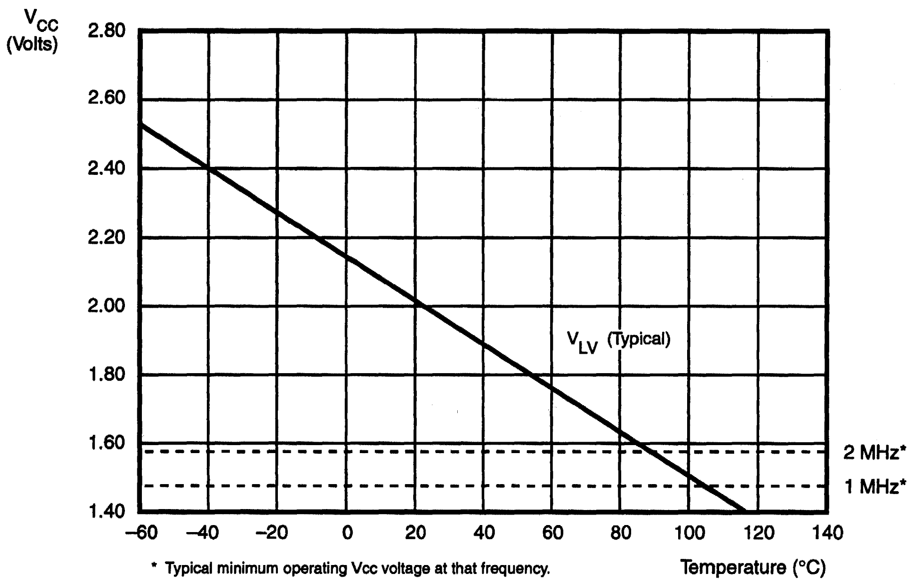


Figure 19. Typical Z86C30/C31 V_{LV} Voltage vs Temperature

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on XTAL1 and /RESET Pins with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		770	mW
Maximum Current out of V_{SS}		140	mA
Maximum Current into V_{DD}		125	mA
Maximum Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Output Current Sinked by Any I/O Pin		25	mA
Maximum Output Current Sourced by Any I/O Pin		25	mA

Notes:
[1] This applies to all pins except XTAL pins and where otherwise noted.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes XTAL pins.
[4] Device pin is not at an output Low state.

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [\, I_{DD} - (\text{sum of } I_{OH})\,] + \text{sum of } [\, (V_{DD} - V_{OH}) \times I_{OH}\,] + \text{sum of } (V_{OL} \times I_{OL})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 20).

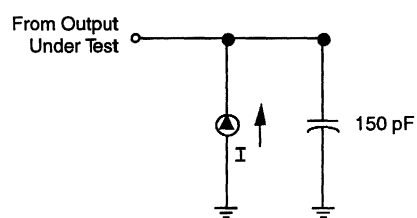


Figure 20. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS
Z86C30/C31

Sym	Parameter	V_{CC} Note[3]	T_A = 0°C to +70°C / T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND –0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND –0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	1.3	V		
		5.0V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	GND–0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND –0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage (Low EMI Mode)	3.0V	V_{CC}–0.4		3.1	V	I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –0.5 mA	
V_{OH1}	Output High Voltage	3.0V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	[8]
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	[8]
V_{OL}	Output Low Voltage (Low EMI Mode)	3.0V		0.6	1.3	V	I_{OL} = 1.0 mA	
		5.5V		0.4	2.5	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I_{OH} = +4.0 mA	[8]
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	[8]
V_{OL2}	Output Low Voltage	3.0V		1.2	0.3	V	I_{OL} = +6 mA, 3 Pin Max	[8]
		5.5V		1.2	0.3	V	I_{OL} = +12 mA, 3 Pin Max	[8]
V_{RH}	Reset Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}	1.5	V		
		5.5V	0.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input Low Voltage	3.3V	GND–0.3	0.2 V_{CC}	1.1			
		5.0V	GND –0.3	0.2 V_{CC}	1.7			
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	3.0V	0	V_{CC}–1.5V		V		[10]
		5.5V	0	V_{CC}–1.5V		V		[10]
		3.0	0	V_{CC}–1.0V		V		[13]
		5.5	0	V_{CC}–1.0V		V		[13]
I_{IL}	Input Leakage	3.0V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.0V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V		–130	–60	µA		
		5.5V		–180	–80	µA		
I_{CC}	Supply Current	3.0V		10	4	mA	@ 8 MHz	[4,5]
		5.5V		15	10	mA	@ 8 MHz	[4,5,15]
		3.0V		15	5	mA	@ 12 MHz	[4,5,15]
		5.5V		20	15	mA	@ 12 MHz	[4,5]

Sym	Parameter	V_{CC} Note[3]	T_A =0°C to +70°C Min	T_A =0°C to +70°C Max	T_A = −40°C to +105°C Min	T_A = −40°C to +105°C Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	3.0V		3		3	1	mA	HALT mode V_{IN} = 0V,V_{CC} @ 8 MHz	[4,5]
		5.5V		5		5	2.4	mA	HALT mode V_{IN} = 0V,V_{CC} @ 8 MHz	[4,5]
		3.0V		4		4	1.5	mA	HALT mode V_{IN} = 0V,V_{CC} @ 12 MHz	[4,5,15]
		5.5V		6		6	3.2	mA	HALT mode V_{IN} = 0V,V_{CC} @ 12 MHz	[4,5,15]
		3.0V		2		2	0.8	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		5.5V		4		4	1.8	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		3.0V		3		3	1.2	mA	Clock Divide by 16 @ 12 MHz	[4,5,15]
		5.5V		5		5	2.5	mA	Clock Divide by 16 @ 12 MHz	[4,5,15]
I_{CC2}	Standby Current	3.0V		8		15	1	µA	STOP mode VIN = 0V, V_{CC} WDT is not Running	[6,11]
		5.5V		10		20	2	µA	STOP mode VIN = 0V, V_{CC} WDT is not Running	[6,11]
		3.0V		500		600	310	µA	STOP mode VIN = 0V, V_{CC} WDT is Running	[6,11]
		5.5V		800		1000	600	µA	STOP mode VIN = 0V, V_{CC} WDT is Running	[6,11]
I_{ALL}	Auto Latch Low Current	3.0V		8		25	16	µA	0V < V_{IN} < V_{CC}	[9]
		5.5V		15		42	23	µA	0V < V_{IN} < V_{CC}	[9]
I_{ALH}	Auto Latch High Current	3.0V		−5		−18	−13	µA	0V < V_{IN} < V_{CC}	[9]
		5.5V		−8		−26	−17	µA	0V < V_{IN} < V_{CC}	[9]
T_{POR}	Power-On Reset	3.0V	7	24	7	25	8.5	ms		
		5.5V	3	13	3	14	5	ms		
V_{LV}	V_{CC} Low Voltage Protection Voltage		1.5	2.8	1.5	3.0	2.1	V	2 MHz max Int. CLK Freq.	[7]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3 mA	5	mA	8 MHz
Crystal or Resonator	24 mA	5	mA	8 MHz

[2] GND=0V.
[3] The V_{CC} voltage specification of 3.0 guarantees 3.3V ±0.3 V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V ±0.5 V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF
[6] Same as note [4] except inputs at V_{CC}.
[7] The V_{LV} increases as the temperature decreases.
[8] Standard Mode (not Low EMI Mode)
[9] Auto Latch (mask option) selected
[10] For analog comparator inputs when analog comparators are enabled.
[11] Clock must be forced Low, when XTAL1 is clock-driven and XTAL2 is floating.
[12] Excludes clock pins.
[13] Temperature is 0° to +70°C.
[14] Auto Latch Delete option is not selected.
[15] Z86C30 only.

AC ELECTRICAL CHARACTERISTICS
Additional Timing Diagram

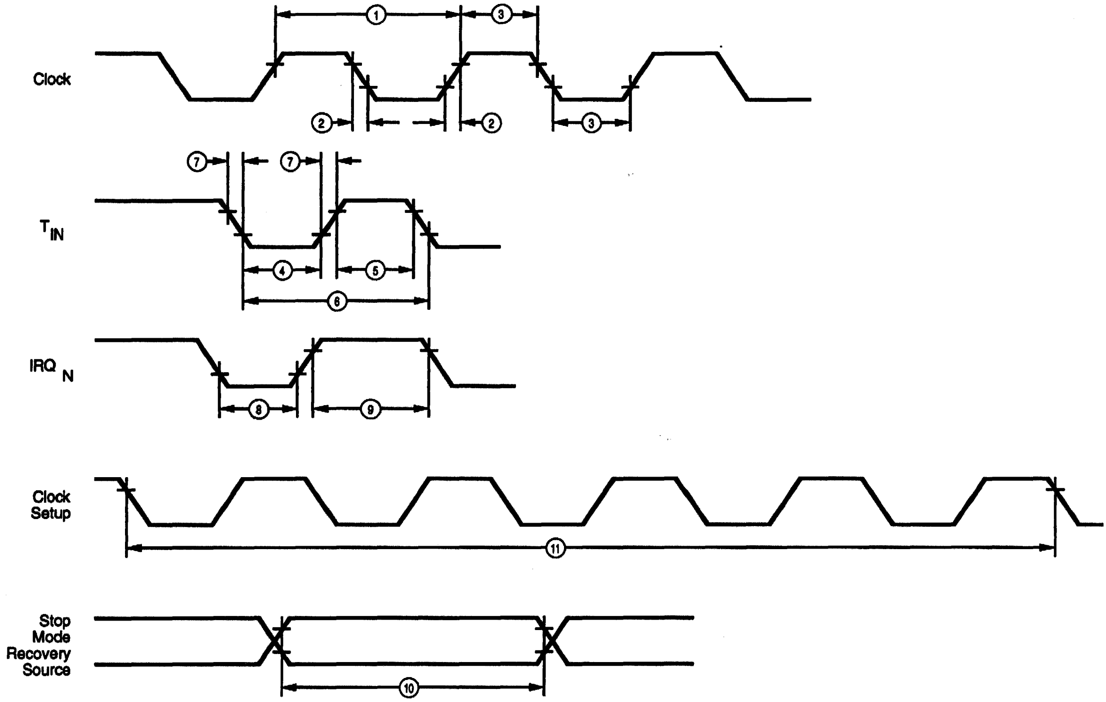


Figure 21. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (For SCLK/TCLK = XTAL/2)

No	Sym	Parameter	V_{CC} Note[6]	T_A = 0°C to +70°C 8 MHz (C31) Min	Max	T_A = –40°C to +105°C 12 MHz (C30) Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	ns	[1,7,8]
			5.5V	125	DC	83	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V	25		15		ns	[1,7,8]
			5.5V	25		15		ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	62.5		62.5		ns	[1,7,8]
			5.5V	62.5		62.5		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			[1,7,8]
			5.5V	5TpC		5TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			[1,7,8]
			5.5V	8TpC		8TpC			[1,7,8]
7	TrTin,	Timer Input Rise and Fall Timer	3.0V		100		100	ns	[1,7,8]
	TfTin		5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC			[1,3,7,8]
			5.5V	5TpC		5TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC			[1,2,7,8]
			5.5V	5TpC		5TpC			[1,2,7,8]
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		[4,9]
			5.5V		5TpC		5TpC		[4,9]
12	Twdt	Watch-Dog Timer Delay Time	3.0V	6.0		6.0		ms	D0=0[5,11]
			5.5V	3.0		3.0		ms	D1=0 [5,11]
			3.0V	20		20		ms	D0=1 [5,11]
			5.5V	10		10		ms	D1=0 [5,11]
			3.0V	33		33		ms	D0=0 [5,11]
			5.5V	16		16		ms	D1=1 [5,11]
			3.0V	132		132		ms	D0=1 [5,11]
			5.5V	66		66		ms	D1=1[5,11]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P30)
[3] Interrupt request through Port 3 (P30).
[4] SMR-D5 = 1, POR STOP mode delay is on.
[5] Reg. WDTMR.
[6] The V_{CC} voltage specification of 3.0 guarantees 3.3V ±0.3V and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
[7] SMR D1=0.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-1 mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.
[10] Standard mode (not Low EMI output ports).
[11] Using internal RC
[12] Z86C31 max. freq. = 8 MHz; Z86C30 max. freq. = 12 MHz.

AC ELECTRICAL CHARACTERISTICS
Additional Timing Table (Divide-By-One Mode)

No	Symbol	Parameter	V_{CC} Note [6]	T_A = 0°C to +70°C 4 MHz Min	Max	T_A = –40°C to +105°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	[1,7,8]
			5.5V	250	DC	250	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25	ns	[1,7,8]
			5.5V		25		25	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	100		100		ns	[1,7,8]
			5.5V	100		100		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			[1,7,8]
			5.5V	3TpC		3TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1,7,8]
			5.5V	4TpC		4TpC			[1,7,8]
7	TrTin,	Timer Input Rise and Fall Timer	3.0V		100		100	ns	[1,7,8]
	TfTin		5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC			[1,3,7,8]
			5.5V	3TpC		3TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			[1,2,7,8]
			5.5V	3TpC		2TpC			[1,2,7,8]
10	Twsm	STOP-Mode Recovery Width Spec	3.0V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		[4,8,9]
			5.5V		5TpC		5TpC		[4,8,9]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P33-P31).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 1, POR STOP mode delay is on.
[5] Reg. WDTMR.
[6] The V_{CC} voltage specification of 3.0 guarantees 3.3V ±0.3V and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
[7] SMR D1 = 0.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-1 mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Table

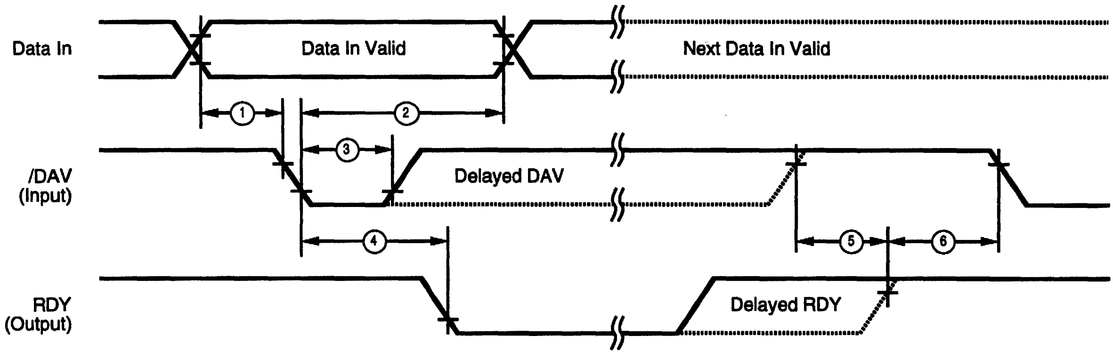


Figure 22. Input Handshake Timing

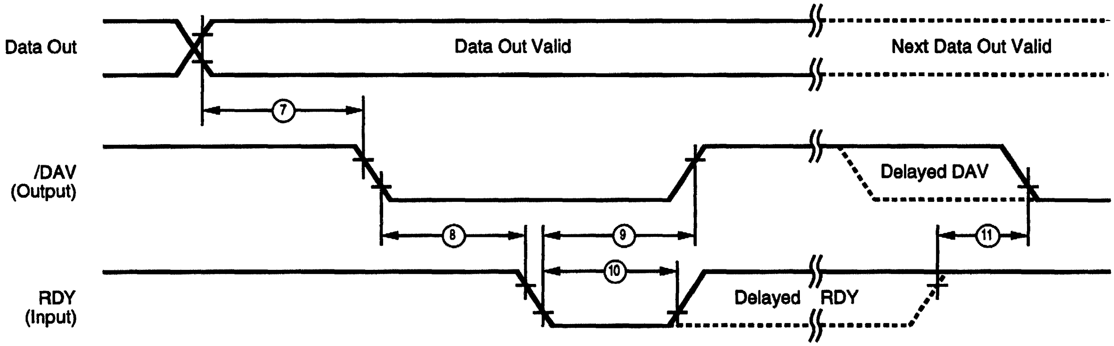


Figure 23. Output Handshake Timing

7

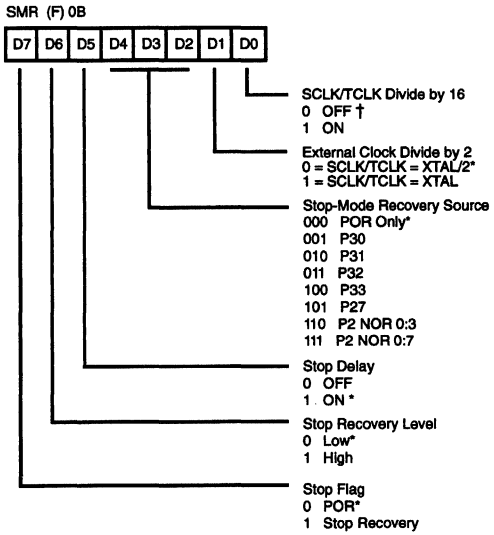
AC ELECTRICAL CHARACTERISTICS (Continued)

Handshake Timing Table

No	Sym	Parameter	V_{CC} Note[1]	T_A =0°C to +70°C 8 MHz (C31) Min	Max	T_A = –40°C to +105°C 12 MHz (C30) Min	Max	Data Direction	Notes
1	TsDI(DAV)	Data In Setup Time	3.0V	0		0		IN	[2]
			5.5V	0		0		IN	[2]
2	ThDI(DAV)	Data In Hold Time	3.0V	160		160		IN	[2]
			5.5V	115		115		IN	[2]
3	TwDAV	Data Available Width	3.0V	155		155		IN	[2]
			5.5V	110		110		IN	[2]
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	3.0V		160		160	IN	[2]
			5.5V		115		115	IN	[2]
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	3.0V		120		120	IN	[2]
			5.5V		80		80	IN	[2]
6	RDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V	0		0		IN	[2]
			5.5V	0		0		IN	[2]
7	TdD0(DAV)	Data Out to DAV Fall Delay	3.0V	63		42		OUT	[2]
			5.5V	63		42		OUT	[2]
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	3.0V	0		0		OUT	[2]
			5.5V	0		0		OUT	[2]
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	3.0V		160		160	OUT	[2]
			5.5V		115		115	OUT	[2]
10	TwRDY	RDY Width	3.0V	110		110		OUT	[2]
			5.5V	80			80	OUT	[2]
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V		110		110	OUT	[2]
			5.5V		80		80	OUT	[2]

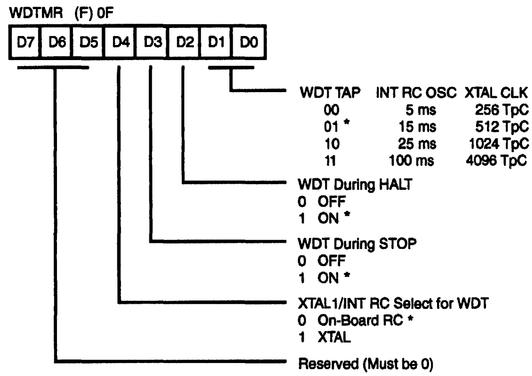
Notes:
[1] The V_{CC} voltage specification of 3.0 guarantees 3.3V ±0.3V and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
[2] Standard Mode (not Low EMI mode on output ports).
[3] Z86C31 max. freq. = 8 MHz; Z86C30 max. freq. = 12 MHz.

EXPANDED REGISTER FILE CONTROL REGISTERS



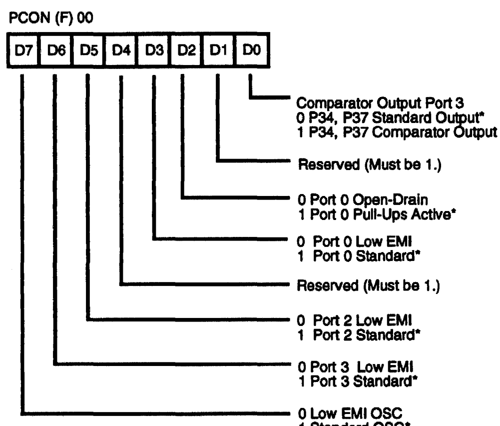
* Default setting after RESET
† Default setting after reset and Stop-Mode Recovery.

Figure 24. Stop-Mode Recovery Register (Write only Except Bit D7 Which is Read Only)



* Default setting after RESET

Figure 25. Watch-Dog Timer Mode Register (Write Only)



* Default setting after RESET

Figure 26. Port Configuration Register (Write Only)

Z8® CONTROL REGISTER DIAGRAMS

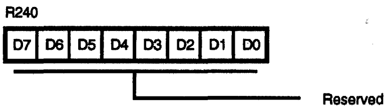


Figure 27. Reserved

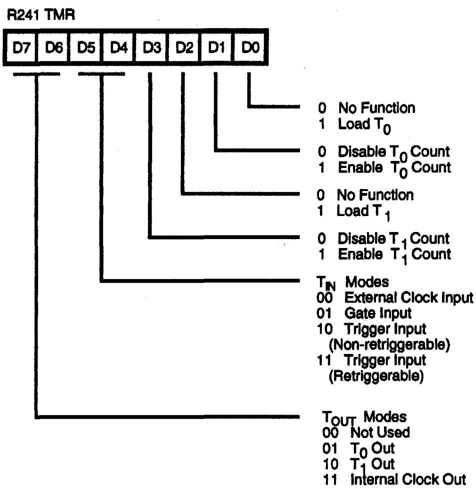


Figure 28. Timer Mode Register ($F1_H$: Read/Write)

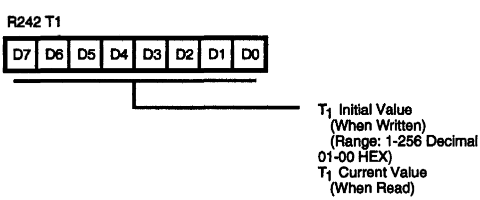


Figure 29. Counter Timer 1 Register ($F2_H$: Read/Write)

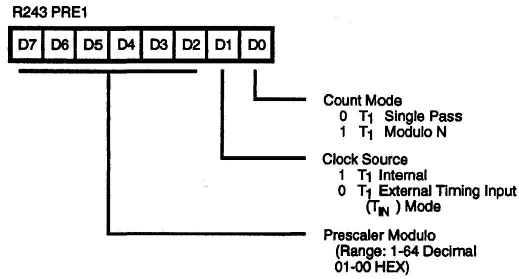


Figure 30. Prescaler 1 Register ($F3_H$: Write Only)

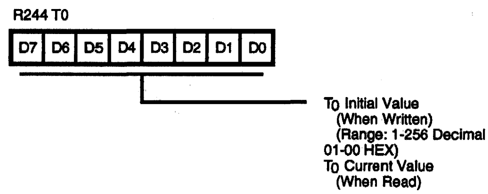


Figure 31. Counter/Timer 0 Register ($F4_H$: Read/Write)

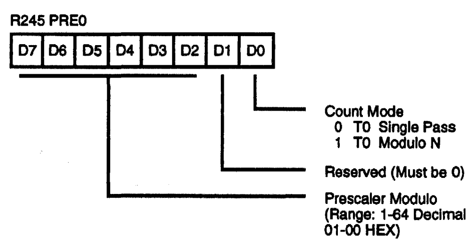


Figure 32. Prescaler 0 Register ($F5_H$: Write Only)

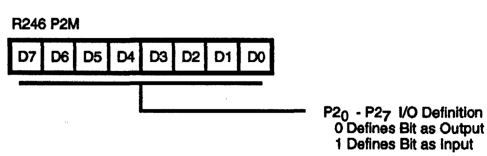


Figure 33. Port 2 Mode Register ($F6_H$: Write Only)

Z8® CONTROL REGISTER DIAGRAMS (Continued)

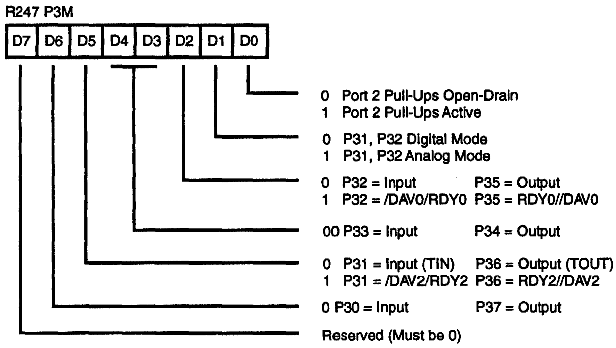


Figure 34. Port 3 Mode Register ($F7_H$: Write Only)

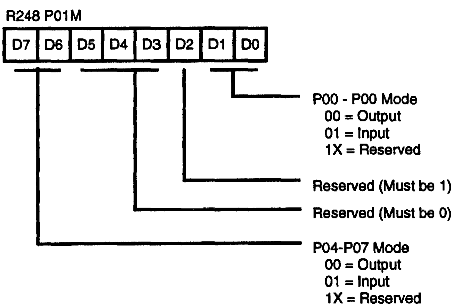


Figure 35. Port 0 and 1 Mode Register ($F8_H$: Write Only)

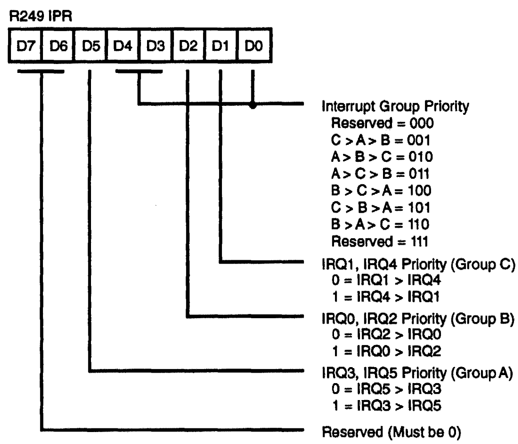


Figure 36. Interrupt Priority Register ($F9_H$: Write Only)

Z8® CONTROL REGISTER DIAGRAMS (Continued)

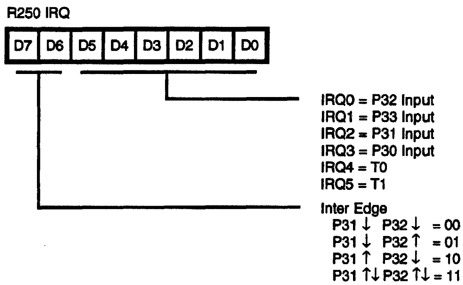


Figure 37. Interrupt Request Register (FA_H: Read/Write)

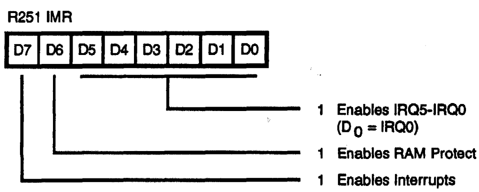


Figure 38. Interrupt Mask Register (FB_H: Read/Write)

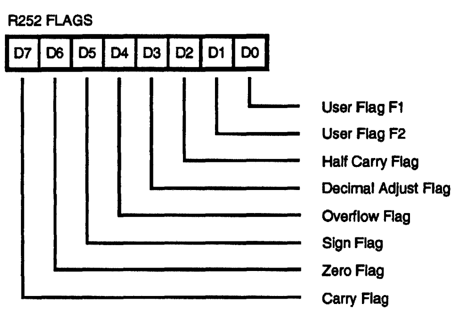


Figure 39. Flag Register (FC_H: Read/Write)

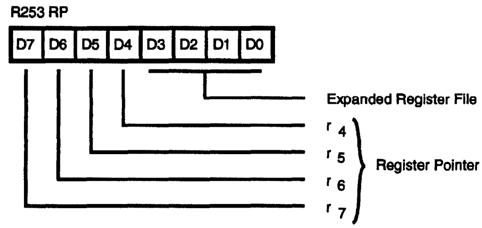


Figure 40. Register Pointer (FD_H: Read/Write)

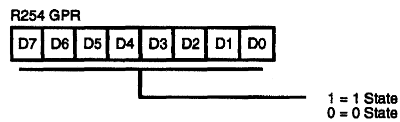


Figure 41. General-Purpose Register

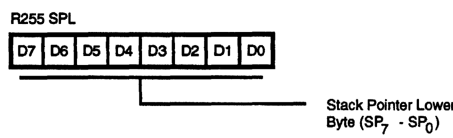


Figure 42. Stack Pointer (FF_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag
Affected flags are indicated by:	
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS

One-Byte Instructions

Format	Instructions
OPC	CCF, DI, EI, IRET, NOP, RCF, RET, SCF
dst | OPC	

Two-Byte Instructions

Format	Alternate	Instructions
OPC | MODE / dst/src	OR 1 1 1 0 | dst/src	CLR, CPL, DA, DEC, DECW, INC, INCW, POP, PUSH, RL, RLC, RR, RRC, SRA, SWAP
OPC / dst	OR 1 1 1 0 | dst	JP, CALL (Indirect)
OPC / VALUE		SRP
OPC | MODE / dst | src		ADC, ADD, AND, CP, OR, SBC, SUB, TCM, TM, XOR
MODE | OPC / dst/src | src/dst		LD, LDE, LDEI, LDC, LDCI
dst/src | OPC / src/dst	OR 1 1 1 0 | src	LD
dst | OPC / VALUE		LD
dst/CC | OPC / RA		DJNZ, JR
FFH / 6FH | 7FH		STOP/HALT

Three-Byte Instructions

Format	Alternate	Instructions
OPC | MODE / src / dst	OR 1 1 1 0 | src; OR 1 1 1 0 | dst	ADC, ADD, AND, CP, LD, OR, SBC, SUB, TCM, TM, XOR
OPC | MODE / dst / VALUE	OR 1 1 1 0 | dst	ADC, ADD, AND, CP, LD, OR, SBC, SUB, TCM, TM, XOR
MODE | OPC / src / dst	OR 1 1 1 0 | src; OR 1 1 1 0 | dst	LD
MODE | OPC / dst/src | x / ADDRESS		LD
cc | OPC / DAU / DAL		JP
OPC / DAU / DAL		CALL

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " $\leftarrow$ ". For example:

dst $\leftarrow$ dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location.

The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

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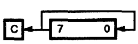
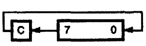
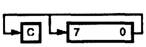
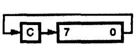
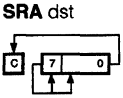
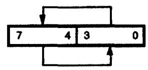
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src	†		1[ ]	*	*	*	*	0	*
dst←dst + src +C									
ADD dst, src	†		0[ ]	*	*	*	*	0	*
dst←dst + src									
AND dst, src	†		5[ ]	-	*	*	0	-	-
dst←dst AND src									
CALL dst	DA		D6	-	-	-	-	-	-
SP←SP - 2	IRR		D4						
@SP←PC,									
PC←dst									
CCF			EF	*	-	-	-	-	-
C←NOT C									
CLR dst	R		B0	-	-	-	-	-	-
dst←0	IR		B1						
COM dst	R		60	-	*	*	0	-	-
dst←NOT dst	IR		61						
CP dst, src	†		A[ ]	*	*	*	*	-	-
dst - src									
DA dst	R		40	*	*	*	X	-	-
dst←DA dst	IR		41						
DEC dst	R		00	-	*	*	*	-	-
dst←dst - 1	IR		01						
DECW dst	RR		80	-	*	*	*	-	-
dst←dst - 1	IR		81						
DI			8F	-	-	-	-	-	-
IMR(7)←0									
DJNZr, dst	RA		rA	-	-	-	-	-	-
r←r - 1			r = 0 - F						
if r ≠ 0									
PC←PC + dst									
Range: +127, -128									
EI			9F	-	-	-	-	-	-
IMR(7)←1									
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
INC dst	r		rE	-	*	*	*	-	-
dst←dst + 1			r = 0 - F						
	R		20						
	IR		21						
INCW dst	RR		A0	-	*	*	*	-	-
dst←dst + 1	IR		A1						
IRET			BF	*	*	*	*	*	*
FLAGS←@SP;									
SP←SP + 1									
PC←@SP;									
SP←SP + 2;									
IMR(7)←1									
JP cc, dst	DA		cD	-	-	-	-	-	-
if cc is true			c = 0 - F						
PC←dst	IRR		30						
JR cc, dst	RA		cB	-	-	-	-	-	-
if cc is true,			c = 0 - F						
PC←PC + dst									
Range: +127, -128									
LD dst, src	r	Im	rC	-	-	-	-	-	-
dst←src	r	R	r8						
	R	r	r9						
			r = 0 - F						
	r	X	C7						
	X	r	D7						
	r	Ir	E3						
	Ir	r	F3						
	R	R	E4						
	R	IR	E5						
	R	IM	E6						
	IR	IM	E7						
	IR	R	F5						
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src	Ir	Irr	C3	-	-	-	-	-	-
dst←src									
r←r +1;									
rr←rr + 1									

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dstf←dst – src – C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst–src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

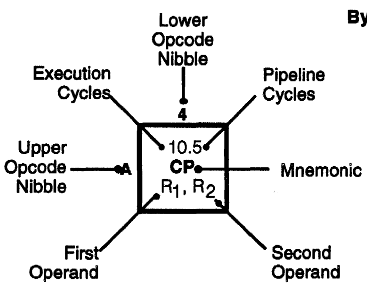
Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) across; **Upper Nibble (Hex)** down

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1							↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1							↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2		3						2					3	1	

Bytes per Instruction



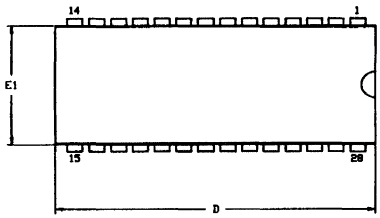
Legend:
R = 8-bit address
r = 4-bit address
R1 or r1 = Dst address
R2 or r2 = Src address

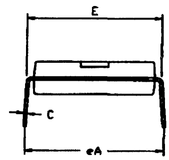
Sequence:
Opcode, First Operand,
Second Operand

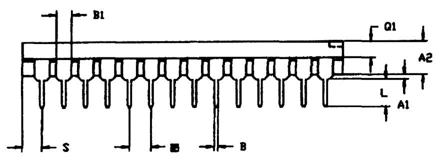
Note: The blanks are reserved.

* 2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION





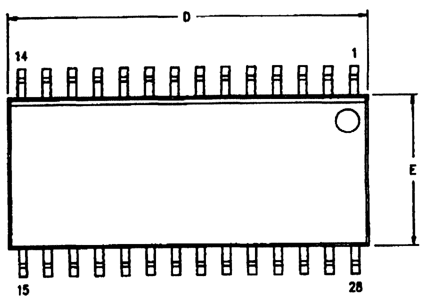


OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

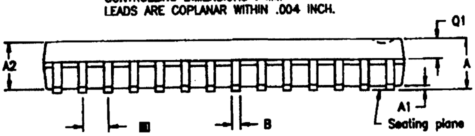
SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	0.81	.020	.032
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.52	1.78	.060	.070
	02	1.27	1.52	.050	.060
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
■		2.54 TYP		.100 TYP	
eA		15.49	16.51	.610	.650
L	•	3.18	3.81	.125	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

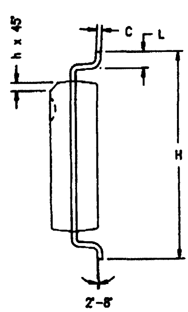
CONTROLLING DIMENSIONS : INCH

28-Pin DIP Package Diagram



CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.





SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
■	1.27 typ		.050 typ	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.07	.038	.042

28-Pin SOIC Package Diagram

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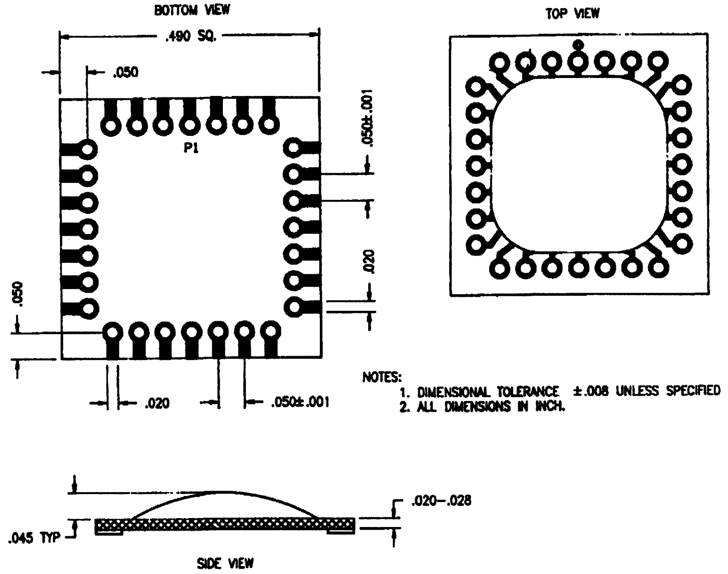
PACKAGE INFORMATION (Continued)



28-Pin PCB Chip Carrier Package Diagram

ORDERING INFORMATION

Z86C30 (12 MHz)

Standard Temperature 28-Pin DIP	Extended Temperature 28-Pin DIP	Standard Temperature 28-Pin SOIC	Extended Temperature 28-Pin SOIC
Z86C3012PSC	Z86C3012PEC	Z86C3012SSC	Z86C3012SEC

Standard Temperature 28-Pin PCB Chip Carrier	Extended Temperature 28-Pin PCB Chip Carrier
Z86C3012TSC	Z86C3012TEC

Z86C31 (8 MHz)

Standard Temperature 28-Pin DIP	Extended Temperature 28-Pin DIP	Standard Temperature 28-Pin SOIC	Extended Temperature 28-Pin SOIC
Z86C3108PSC	Z86C3108PEC	Z86C3108SSC	Z86C3108SEC

Standard Temperature 28-Pin PCB Chip Carrier	Extended Temperature 28-Pin PCB Chip Carrier
Z86C3108TSC	Z86C3108TEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
S = SOIC
T = PCB Chip Carrier

Preferred Temperature
S = 0° C to +70° C

Longer Lead Time
E = –40° C to +105° C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86C30 12 P S C is a Z86C30, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 12 — Speed
- 86C30 — Product Number
- Z — Zilog Prefix

Zilog

Z86E30/E31 CMOS Z8® OTP CCP™ Consumer Controller Processor

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Z86E30/E31

CMOS 8-BIT Z8® OTP CCP™ CONSUMER CONTROLLER PROCESSORS

FEATURES

- The Z86E30 and Z86E31 Have the Following General Characteristics:

Part	EPROM	RAM	Speeds
Z86E30	4K	236	12 MHz
Z86E31	2K	124	8 MHz

- 28-Pin Packages (DIP, Cerdip Window Lid)
- 4.5V to 5.5V Operating Range
- Clock Speeds up to 8 MHz (E31) and 12 MHz (E30)
- Software Programmable Low EMI Mode
- Pull-Up Active/Open-Drain Programmable on Ports 0 and 2
- EPROM Protect Option
- RAM Protect Programmable
- RC Oscillator Programmable
- Low Power Consumption: 60 mW
- Two Standby Modes: STOP and HALT
- 24 Input/Output Lines (Three with Comparator Inputs)
- 17 Digital Inputs with CMOS Levels, Schmitt-Triggered
- Three Digital Inputs with CMOS Levels Only
- Three Expanded Register File Control Registers
- Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Software Enabled Watch-Dog Timer
- Auto Power-On Reset
- Auto Latches
- Two Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

GENERAL DESCRIPTION

The Z86E30/E31 CCP™ (Consumer Controller Processors) are members of Zilog's the Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 4K/2K bytes of EPROM and 236/124 bytes of general-purpose RAM, respectively, these low cost, low power consumption CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

Manufactured in CMOS technology and offered in 28-pin DIP and Cerdip Window Lid package styles, these devices allow easy software development and debug, prototyping, and small production runs not economically desirable with a masked ROM version.

For applications demanding powerful I/O capabilities, the Z86E30/E31 provides 24 pins dedicated to input and output. These lines are grouped into three ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake.

GENERAL DESCRIPTION (Continued)

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File (ERF). The Register File is composed of 236/124 bytes of general-purpose registers, three I/O port registers and 15 control and status registers. The Expanded Register File consists of three control resisters.

To unburden the system from coping with the real-time tasks such as counting/timing and input/output data communication, the Z86E30/31 offers two on-chip counter/timers with a large number of user-selectable modes, and two on-board comparators to process analog signals with a common reference voltage (Figures 1 and 2).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

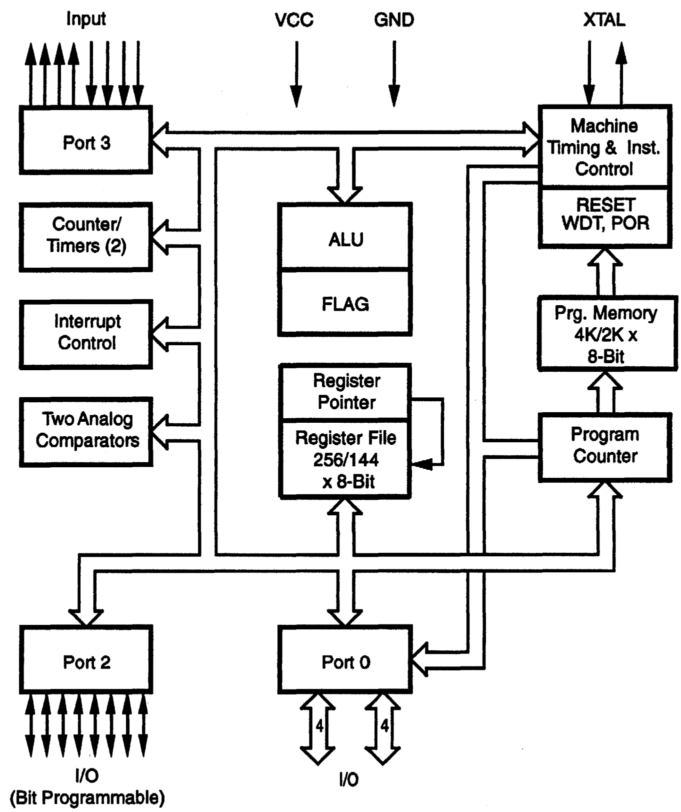


Figure 1. Z86E30/E31 Functional Block Diagram

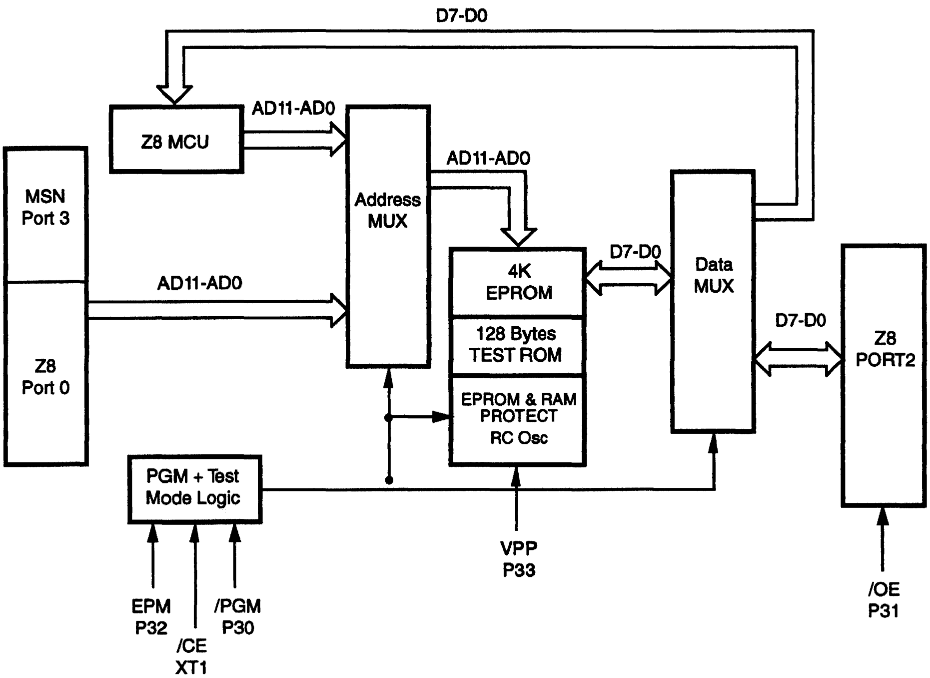


Figure 2. Z86E30/E31 EPROM Programming Block Diagram

PIN DESCRIPTION

Table 1. Z86E30/E31 28-Pin DIP Pin Identification*

Standard Mode

Pin #	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,	In/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output

Note:
* Pin Identification and Configuration identical on DIP and Cerdip Window Lid style packages.

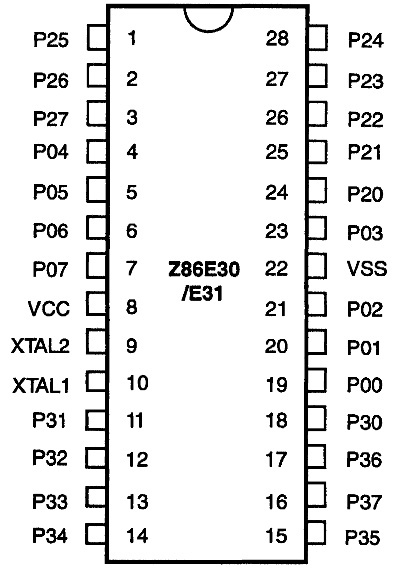


Figure 3. Z86E30/31 Standard Mode 28-Pin DIP Pin Configuration*

Table 2. Z86E30/E31 28-Pin DIP Pin Identification*

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1-3	D5-D7	Data 5,6,7	In/Output
4-7	A4-A7	Address 4,5,6,7	Input
8	V_{CC}	Power Supply	
9	NC	No connection	
10	/CE	Chip Select	Input
11	/OE	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14-15	A8-A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	/PGM	Prog. Mode	Input
19-21	A0-A2	Address 0,1,2	Input
22	V_{SS}	Ground	
23	A3	Address 3	Input
24-28	D0-D4	Data 0,1,2,3,4	In/Output

Note:
* Pin Identification and Configuration identical on DIP and Cerdip Window Lid style packages.

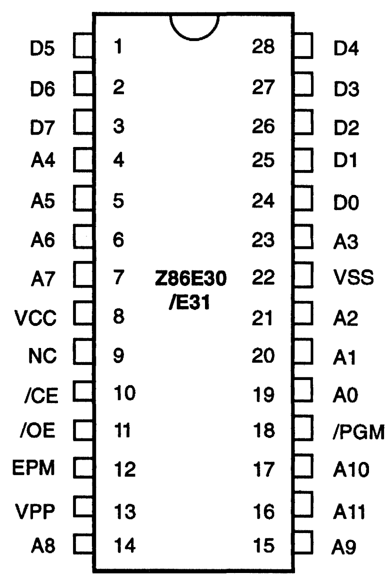


Figure 4. Z86E30/31 EPROM Programming Mode 28-Pin DIP Pin Configuration*

8

PIN FUNCTIONS

Z86E30/31 Standard Mode

XTAL1 *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network or external single-phase clock to the on-chip oscillator input.

XTAL2 *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 0 (P07-P00). Port 0 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be nibble programmed as P03-P00 input/output and P07-P04 input/output, separately. The input buffers are Schmitt-triggered and nibbles programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can also be used as a handshake I/O port.

In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble (Figure 5).

EPROM Programming Mode

D7-D0 *Data Bus*. The data can be read from or written to the EPROM through the data bus.

A11-A0 *Address Bus*. During programming, the EPROM address is written to the address bus.

V_{CC} *Power Supply*. This pin must be supply 5V during the EPROM Read Mode and 6V during other modes.

/CE *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode and Program Verify Mode.

/OE *Output Enable* (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM *EPROM Program Mode*. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} *Program Voltage*. This pin supplies the program voltage.

/PGM *Program Mode* (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise surges above V_{cc}*** occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{pp}, /CE, /EPM, /OE pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin.

PIN FUNCTIONS (Continued)

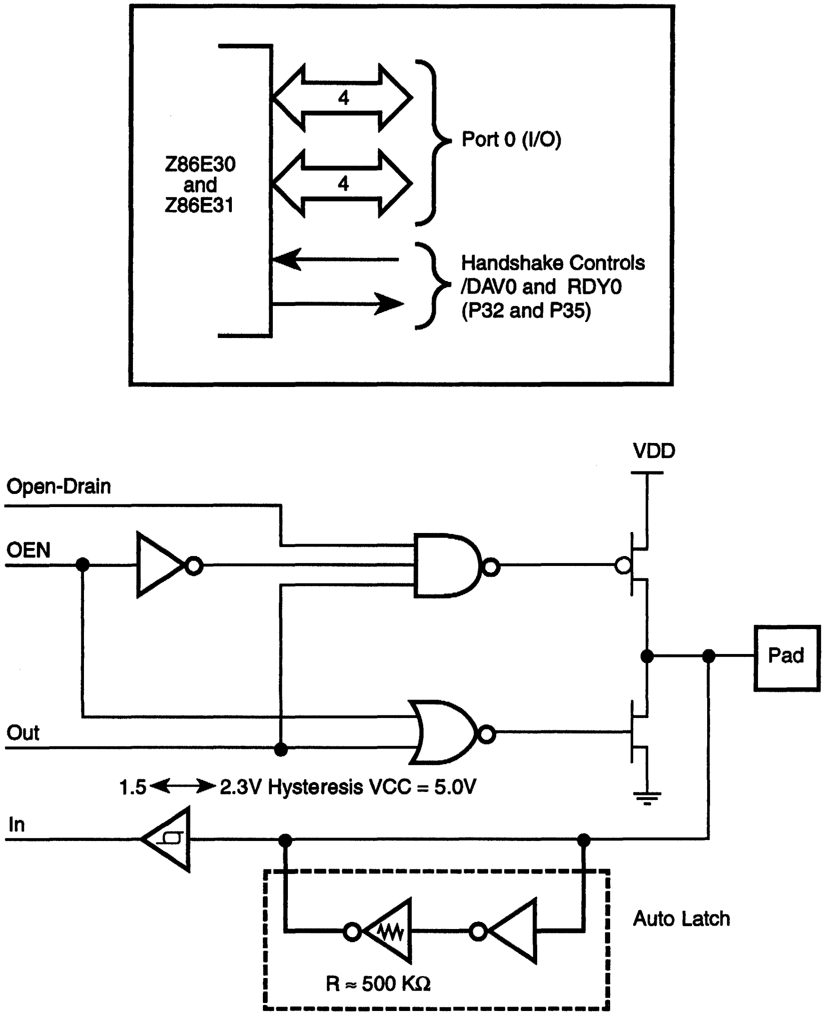


Figure 5. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control. In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 6).

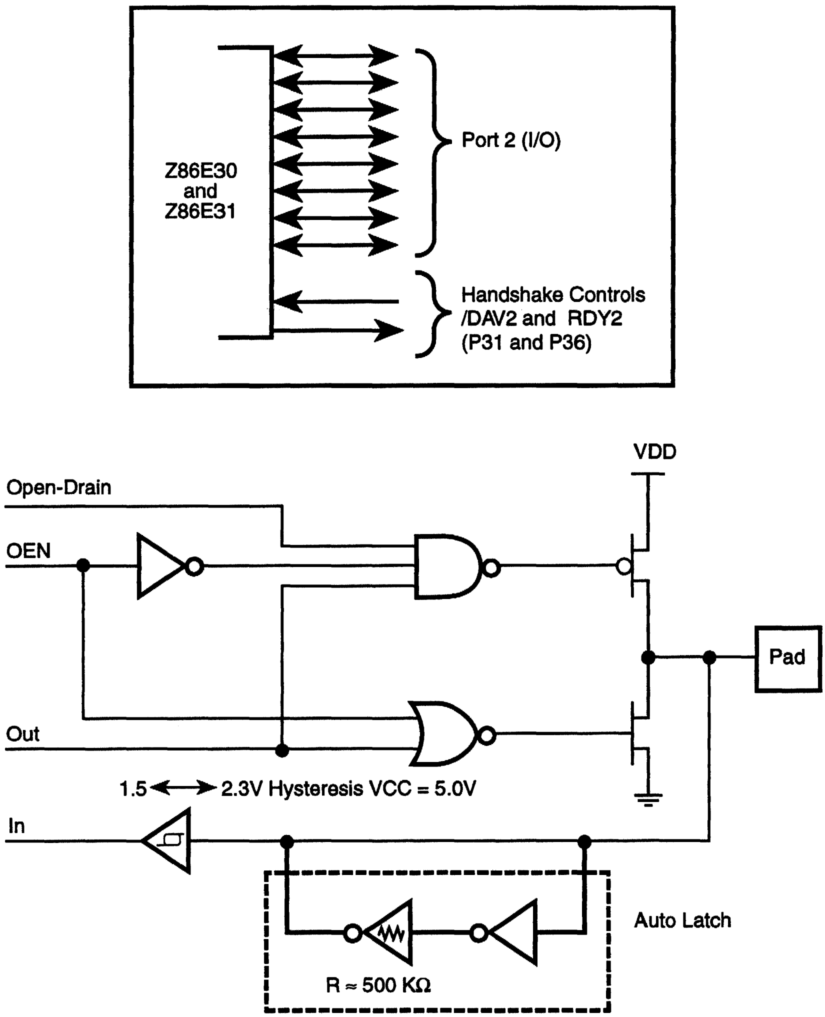


Figure 6. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible port with four fixed inputs (P33-P30) and four fixed outputs (P37-P34), and can be configured under software for interrupt and handshake control functions. Port 3, pin 0 is Schmitt-triggered. Pins P31, P32, and P33 are standard CMOS inputs (no Auto Latches) and pins P34, P35, P36, and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The comparator output can be outputted from P34 and P37, respectively, by setting PCON register (PCON) bit D0 to 1.

The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edge triggered interrupt inputs (Figure 7). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are also available on Port 3 (Table 3). T_{IN} Modes are enabled by setting R243 PRE1 Bit D1 to 0.

Table 3. Port 3 Pin Assignments

Pin	I/O	CTC1	AN IN	Int.	P0 HS	P2 HS
P30	IN			IRQ3		
P31	IN	T_{IN}	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT					
P35	OUT				R/D	
P36	OUT	T_{OUT}				R/D
P37	OUT					

Note: P33-P30 inputs differ from the Z86C30/31 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

Comparator Inputs. Port 3, pins P31 and P32 each have a comparator front end. The comparator reference voltage (pin P33) is common to both comparators. In analog mode, P31 and P32 are the positive inputs, and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this is 0 or 1, cannot be determined.

A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Low EMI Emission. The Z86E30/31 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).

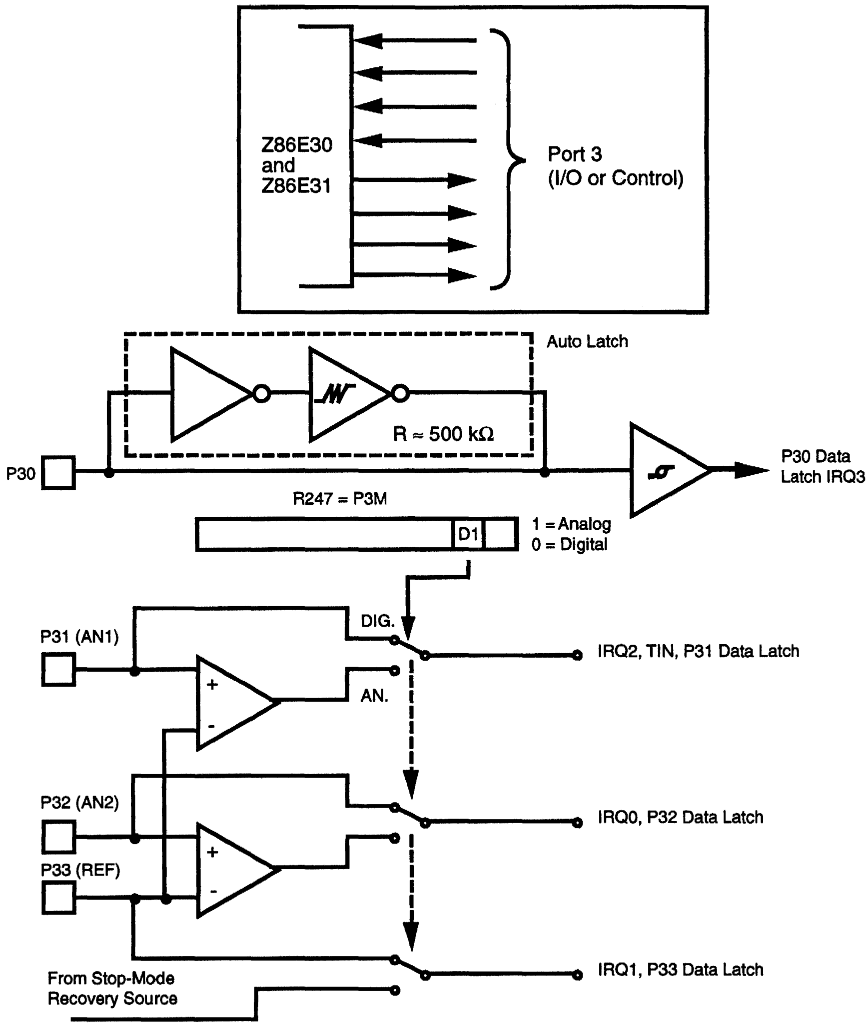


Figure 7. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The Z86E30/E31 CCP™'s incorporate the following special functions to enhance the standard Z8® architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- STOP-Mode Recovery Source

Having the Auto Power-on Reset circuitry built in, the Z86E30/E31 does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles. The Z86E30/31 does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP-Mode Recovery operation.

Program Memory. The Z86E30/E31 can address up to 4K/2K bytes of internal program memory (Figure 8). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Address 12 (000CH) to address 4095 (0FFFH)/2047(07FFH) are reserved for the user program. After reset, the program counter points at the address 000CH which is the starting address of the user program.

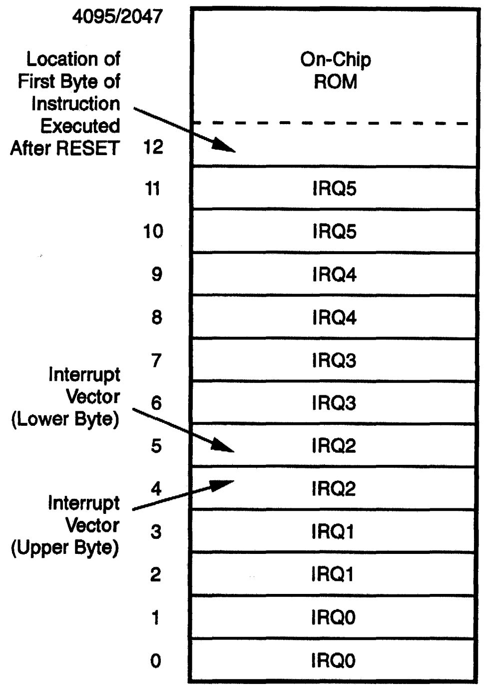


Figure 8. Program Memory Map

EPROM Protect. The 4K/2K bytes program memory is a One-Time-PROM. An EPROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC and LDCI instructions (LDE and LDEI instructions are not available in Z86E30/E31) to program memory in all modes. In EPROM protect mode, the instructions of LDC and LDCI are disabled globally. ROM look-up tables cannot be used with this option.

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices, and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 11). These register groups are known as the Expanded Register File (ERF).

The low nibble (D3-D0) of the Register Pointer (RP) selects the active ERF group, and the high nibble (D7-D4) of register RP selects the working register group (Figure 9).

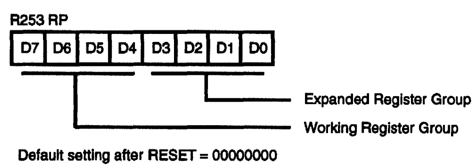


Figure 9. Register Pointer Register

Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

Register File. The register file consists of three I/O port registers, 236/124 general-purpose registers, 15 control and status registers, and three system configuration registers in the expanded register group. The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 10). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0-EF can only be accessed through working register and indirect addressing modes. (This bank is available in Z86C30 only.)

General Purpose Register (GPR). The general purpose registers are undefined after the device is powered-up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general purpose register.

8

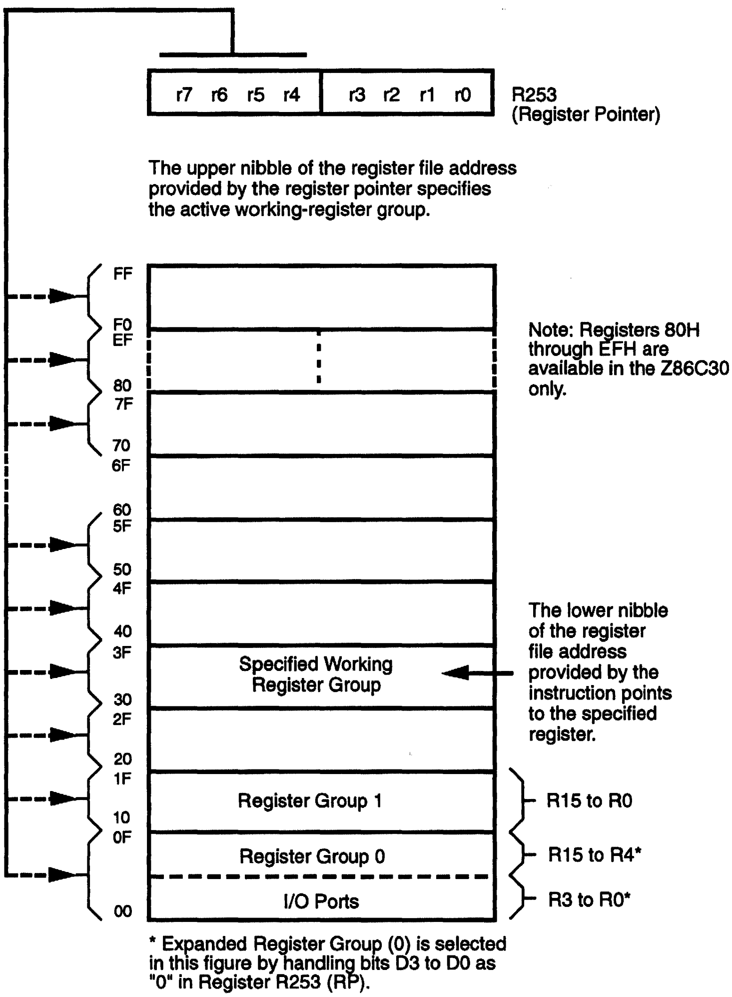
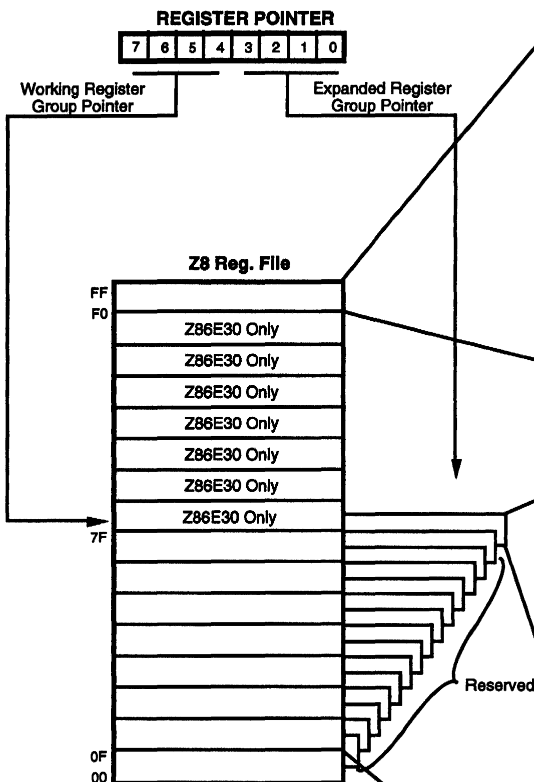


Figure 10. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)



Z8® STANDARD CONTROL REGISTERS

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
	FF	SPL	U	U	U	U	U	U	U	U
	FE	GPR	U	U	U	U	U	U	U	U
	FD	RP	0	0	0	0	0	0	0	0
	FC	FLAGS	U	U	U	U	U	U	U	U
	FB	IMR	0	U	U	U	U	U	U	U
	FA	IRQ	0	0	0	0	0	0	0	0
	F9	IPR	U	U	U	U	U	U	U	U
	F8	P01M	0	1	0	0	1	1	0	1
*	F7	P3M	0	0	0	0	0	0	0	0
*	F6	P2M	1	1	1	1	1	1	1	1
	F5	PRE0	U	U	U	U	U	U	U	0
	F4	T0	U	U	U	U	U	U	U	U
	F3	PRE1	U	U	U	U	U	U	0	0
	F2	T1	U	U	U	U	U	U	U	U
	F1	TMR	0	0	0	0	0	0	0	0
	F0	Reserved								

EXPANDED REG. GROUP (F)

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
*	(F) 0F	WDTMR	U	U	U	0	1	1	0	1
	(F) 0E	Reserved								
	(F) 0D	Reserved								
	(F) 0C	Reserved								
**	(F) 0B	SMR	0	0	1	0	0	0	0	0
	(F) 0A	Reserved								
	(F) 09	Reserved								
	(F) 08	Reserved								
	(F) 07	Reserved								
	(F) 06	Reserved								
	(F) 05	Reserved								
	(F) 04	Reserved								
	(F) 03	Reserved								
	(F) 02	Reserved								
	(F) 01	Reserved								
	(F) 00	PCON	1	1	1	1	1	1	1	0

EXPANDED REG. GROUP (0)

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
	(0) 03	P3	*U	*U	U	U	U	U	U	U
*	(0) 02	P2	U	U	U	U	U	U	U	U
	(0) 01	Reserved	U	U	U	U	U	U	U	U
	(0) 00	P0	U	U	U	U	U	U	U	U

Notes:
U = Unknown
* Will not be reset with a STOP-Mode Recovery.
** Will not be reset with a STOP-Mode Recovery, except D0.

Figure 11. Expanded Register File Architecture

RAM Protect (Z86E30 Only). The upper portion of the RAM's address spaces %7F to %EF (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is EPROM-programmable. After the EPROM option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or 1, respectively. A 1 in D6 indicates RAM Protect enabled. This option is only available in the Z86E30.

Stack. The Z86E30/E31 has 236/124 general-purpose registers. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 12).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that can be retriggerable or not-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

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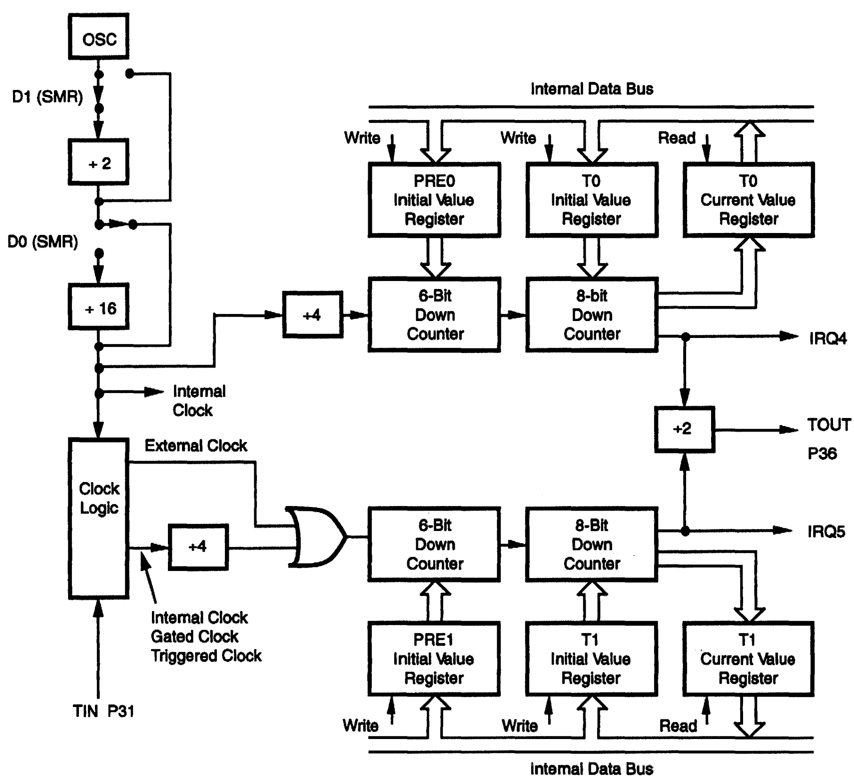


Figure 12. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86E30/E31 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 13). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

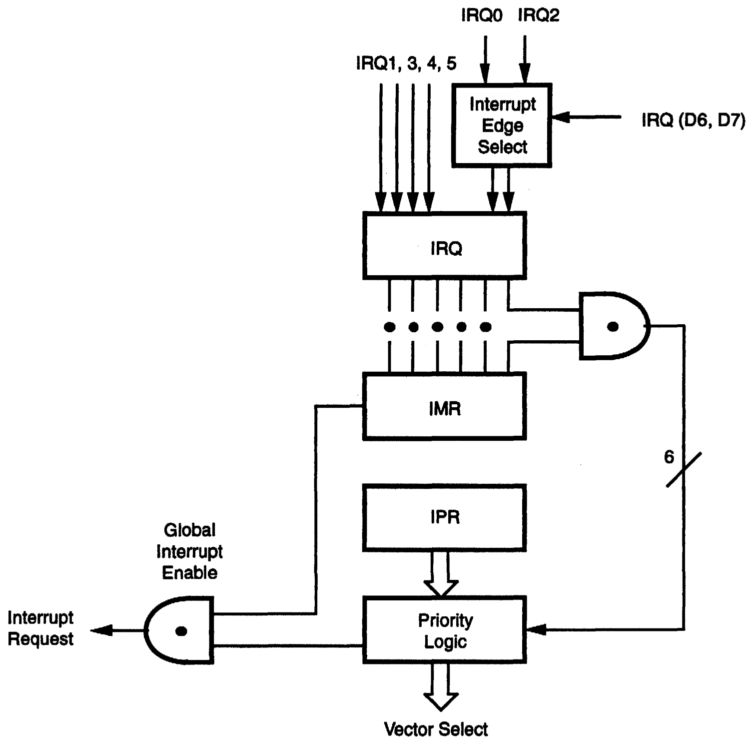


Figure 13. Interrupt Block Diagram

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E30/E31 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 5.

Table 5. IRQ Register Configuration

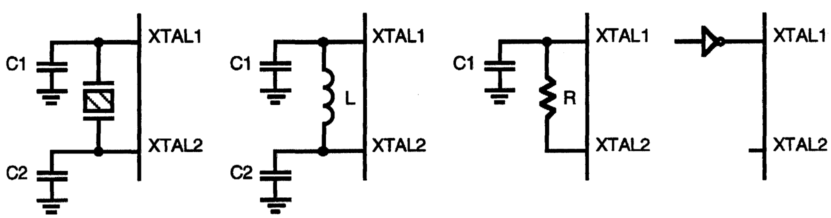
IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86E30/E31 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitors from each pin directly to device pin 22 to reduce injection of system ground noise. The RC oscillator option is selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 14).

Note: RC OSC does not support 12 MHz.



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz

LC
C1, C2 = 22 pF

L = 130 uH *
f = 3 MHz *

RC
@ 5V VCC (TYP)

C1 = 33 pF *
R = 1k *
f = 6.6 MHz *

External Clock

* Typical value including pin parasitics

Figure 14. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power bad to Power OK status
2. STOP-Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode Register (SMR) determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP instruction (opcode=FFH) immediately before the appropriate SLEEP instruction, i.e.:

```
FF  NOP   ; clear the pipeline
6F  STOP  ; enter STOP mode
or
FF  NOP   ; clear the pipeline
7F  HALT  ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA or less. STOP mode is terminated by one of the following resets: WDT time-out, POR, or STOP-Mode Recovery Source which is defined by SMR register . This causes the processor to restart the application program at address 000C (HEX).

Port Configuration Register (PCON). The PORT Configuration Register (PCON) configures the ports ndividually: Comparator Output on Port 3, Open-Drain on Port 0, Low EMI Noise on Ports 0, 2, and 3, and Low EMI Noise Oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 15).

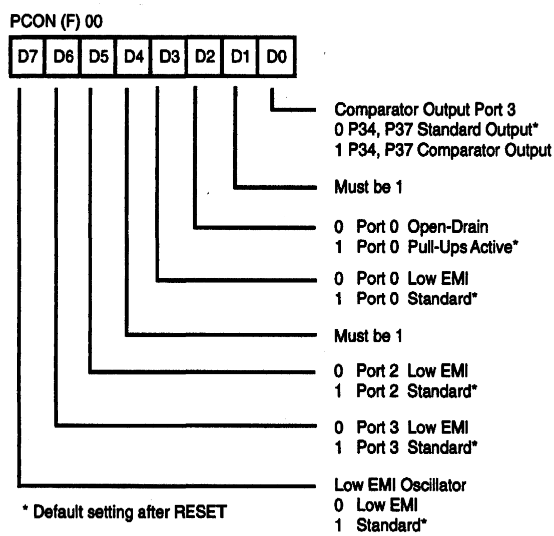


Figure 15. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P35 and a 0 releases the Port to its standard I/O configuration.

Port 0 Open-Drain (D1). Port 0 is configured as an open-drain by resetting this bit (D1 = 0) and configured as pull-up active by setting D1 = 1. The default value is 1.

Low EMI Port 0 (D3). Port 0 is configured as a Low EMI Port by resetting this bit (D3 =0) and configured as a Standard Port by setting D3 =1. The default value is 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5 = 0) and configured as a Standard Port by setting D5 = 1. The default value is 1.

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6 = 0) and configured as a Standard Port by setting D6 = 1. The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive; however, it does not affect the relationship of SCLK and XTAL.

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP mode recovery (Figure 16). All bits are Write Only except Bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the STOP-Mode Recovery Source (Table 7). The SMR is located in Bank F of the Expanded Register Group at address 0BH.

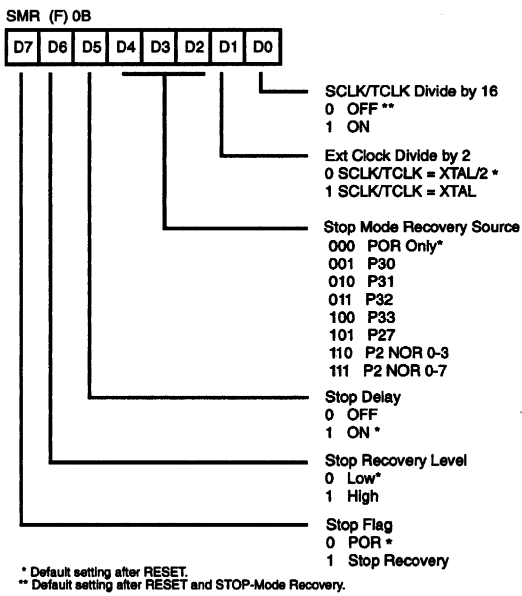


Figure 16. STOP-Mode Recovery Register (Write Only Except D7 Which Is Read Only)

FUNCTIONAL DESCRIPTION (Continued)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-By-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1 = 1). Using this bit, together with D7 of PCON, further helps lower EMI [i.e., D7 (PCON) = 0, D1 (SMR) = 1]. The default setting is 0. Maximum frequency is 4 MHz with D1 = 1

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake-up source of the STOP-Mode Recovery (Figure 17). Table 6 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up from STOP mode when programmed as analog inputs.

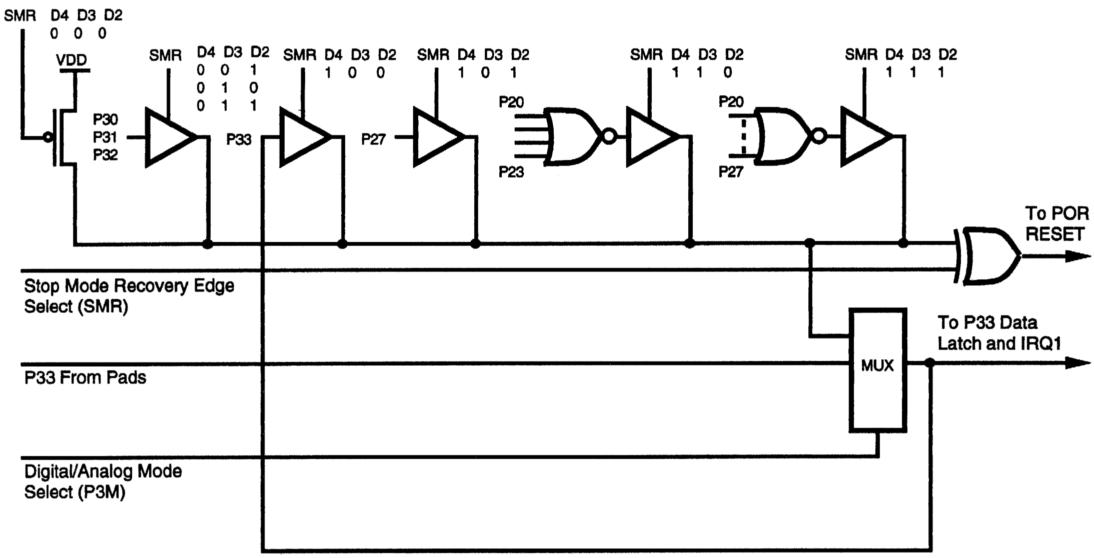


Figure 17. STOP-Mode Recovery Source

Table 6. STOP-Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

STOP-Mode Recovery Delay Select (D5). The 5 ms RESET delay after STOP-Mode Recovery is disabled by programming this bit to a zero. A1 in this bit causes a 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the STOP-Mode Recovery source must be kept active for at least 5 TpC.

STOP-Mode Recovery Level Select (D6). A 1 in this bit defines that a high level on any one of the recovery sources wakes the Z86E30/E31 from STOP Mode. A 0 defines the low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A 0 in this bit indicates that the device has been reset by POR (cold). A 1 in this bit indicates the device was awakened by a SMR source (warm). This bit is read only.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches terminal count (Figure 18). The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction. It is refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled when it has been enabled. The WDT is driven either by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 19).

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 64 processor cycles (128 XTAL clock cycles) from the execution of the first instruction after Power-On Reset, Watch-Dog Reset, or a STOP-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH.

WDT Time-out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained. Table 7 shows the time-out period. The default value of D0 and D1 are 1 and 0, respectively.

Table 7. Time-out Period of the WDT

D1	D0	Time-Out of Internal RC OSC	Time-Out of the Crystal Clock
0	0	5 ms	256TpC
0	1	15 ms	512TpC
1	0	25 ms	1024TpC
1	1	100 ms	4096TpC

Notes:
TpC = crystal clock cycle
The default setting is 15 ms.
Values shown are for V_{CC} = 5.0V.

WDT During the HALT Mode (D2). This bit determines whether or not the WDT is active during HALT mode. A1 indicates that the WDT is active during HALT. A 0 disables the WDT in HALT mode. The default value is 1.

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A1 indicates active during STOP Mode. A 0 disables the WDT during STOP mode. Since the on-board OSC is stopped during STOP mode, the WDT clock source has to select the on-board RC OSC for the WDT to recover from STOP mode. The default is 1.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of the bit is 0, which selects the RC oscillator.

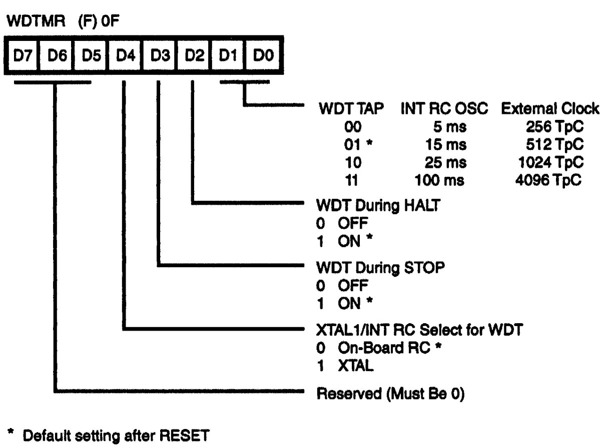


Figure 18. Watch-Dog Timer Mode Register (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

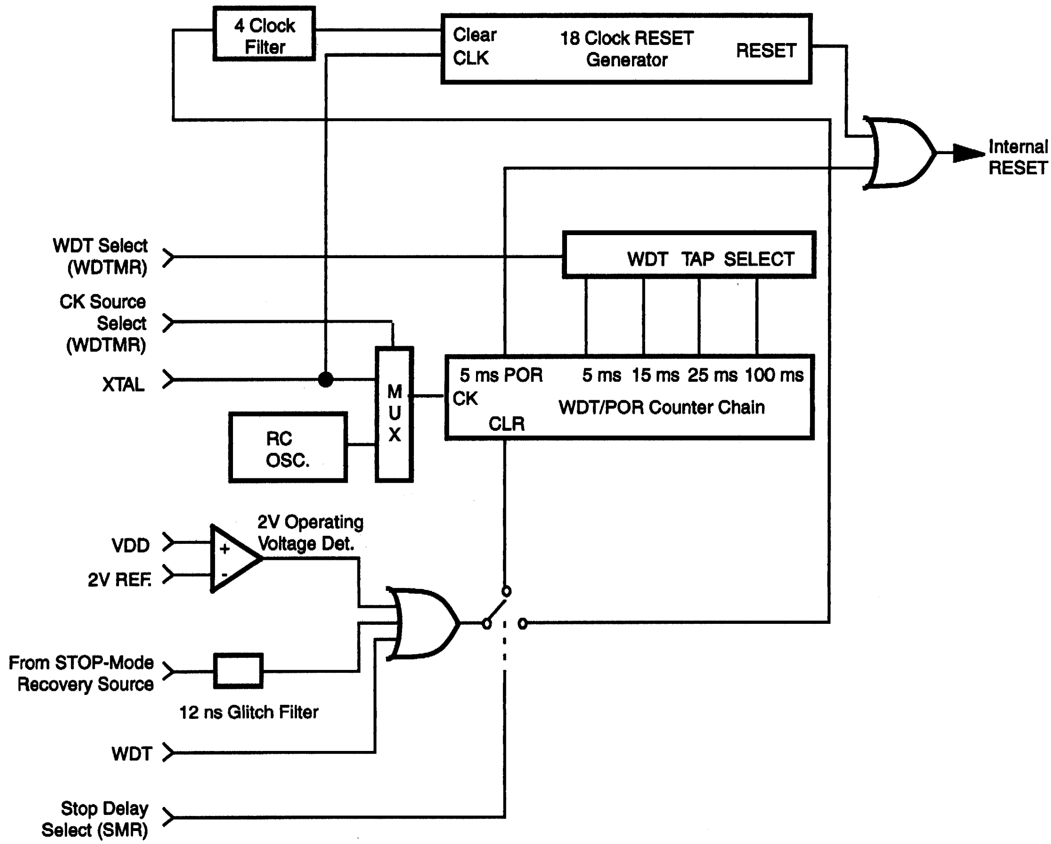


Figure 19. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{RST} (Figure 20).

If the V_{CC} drops below 4.5V while the device is in operation, the device must be powered down and then re-powered up again. **Note:** V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum Power-On Reset time-out (T_{POR}).

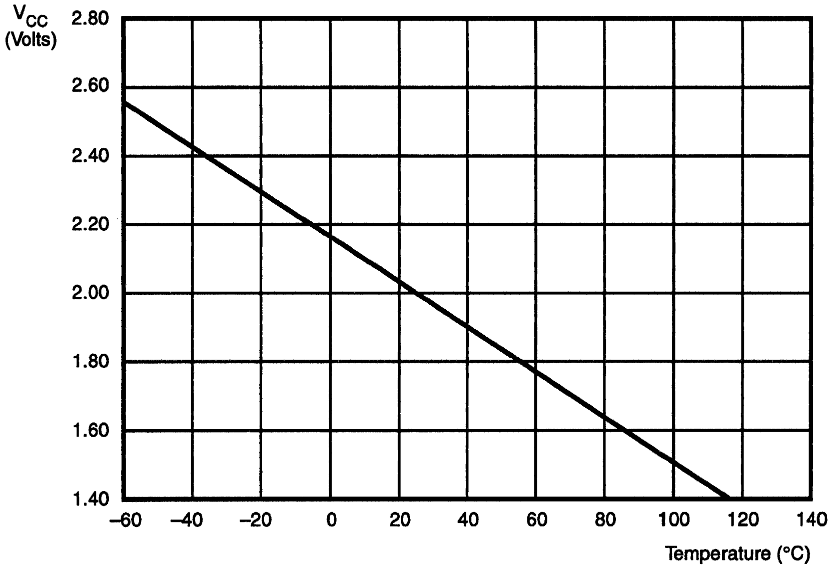


Figure 20. Typical Z86E30/E31 V_{RST} Voltage vs Temperature

FUNCTIONAL DESCRIPTION (Continued)

EPROM Programming Mode

Table 8 shows the programming voltages of each programming mode. Table 9, Figures 21, 22, and 23 show the programming timing of each programming mode. Figure 24 shows the flow-chart of an Intelligent Programming Algorithm, which is compatible with a 2764A EPROM (Z86E30/E31 is 4K/2K EPROM, 2764A is 8K EPROM).

Figure 25 shows the circuit diagram of the Z86E30/E31 programming adaptor which adapts from 2764A to Z86E30/E31. Since the EPROM size of Z86E30/E31 differs from 2764A, the programming address range should be set from 0000H to 0FFFH.

Table 8. EPROM Programming Table

Programming Modes	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ1	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V†
EPROM READ2	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V†
PROGRAM	V_H	X	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.0V
PROGRAM VERIFY	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
EPROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
RC OSCILLATOR SELECT	V_H	V_{IL}	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
RAM PROTECT	V_H	V_{IH}	V_H	V_{IL}	V_{IL}	NU	NU	6.0V

Notes:
V_H = .12.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.
† Although most progammers do an EPROM read at V_{cc} = 5.0V, Zilog recommends an EPROM read at V_{cc} = 4.5V and 5.0V to ensure proper device operations during the V_{cc} after programming.

Table 9. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

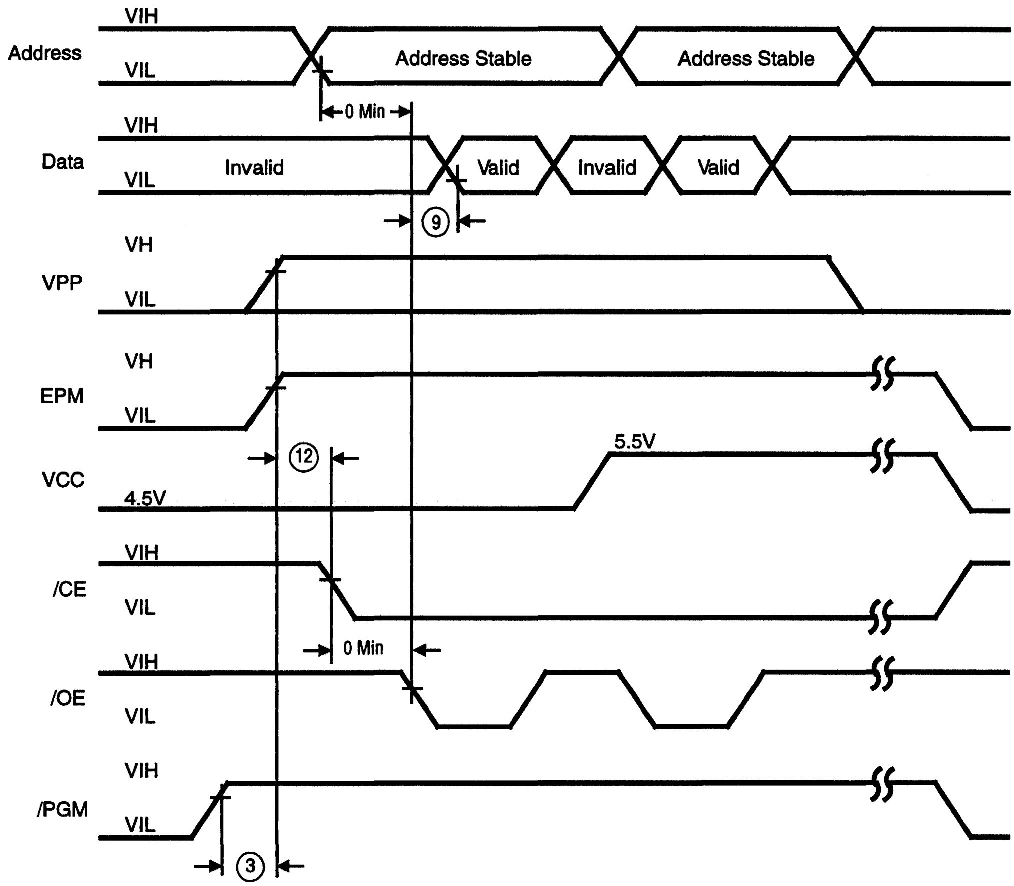


Figure 21. EPROM READ Mode Timing Diagram

FUNCTIONAL DESCRIPTION (Continued)

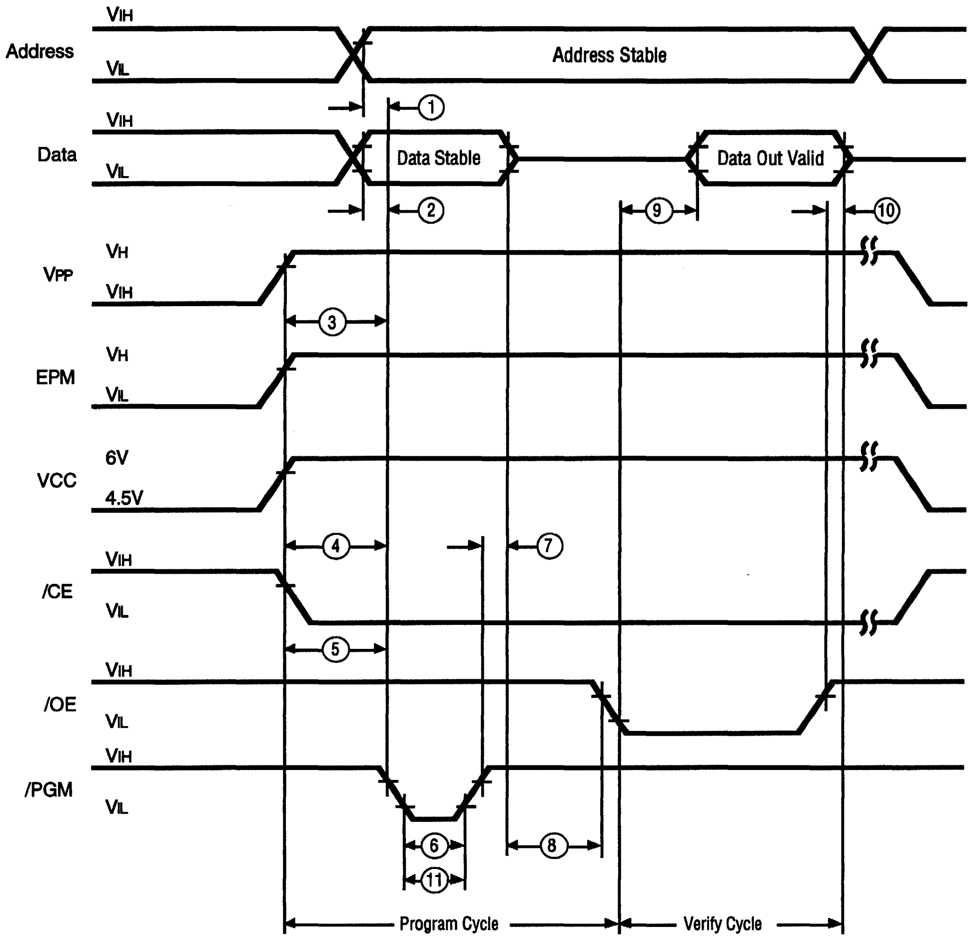


Figure 22. Timing Diagram of EPROM Program and Verify Modes

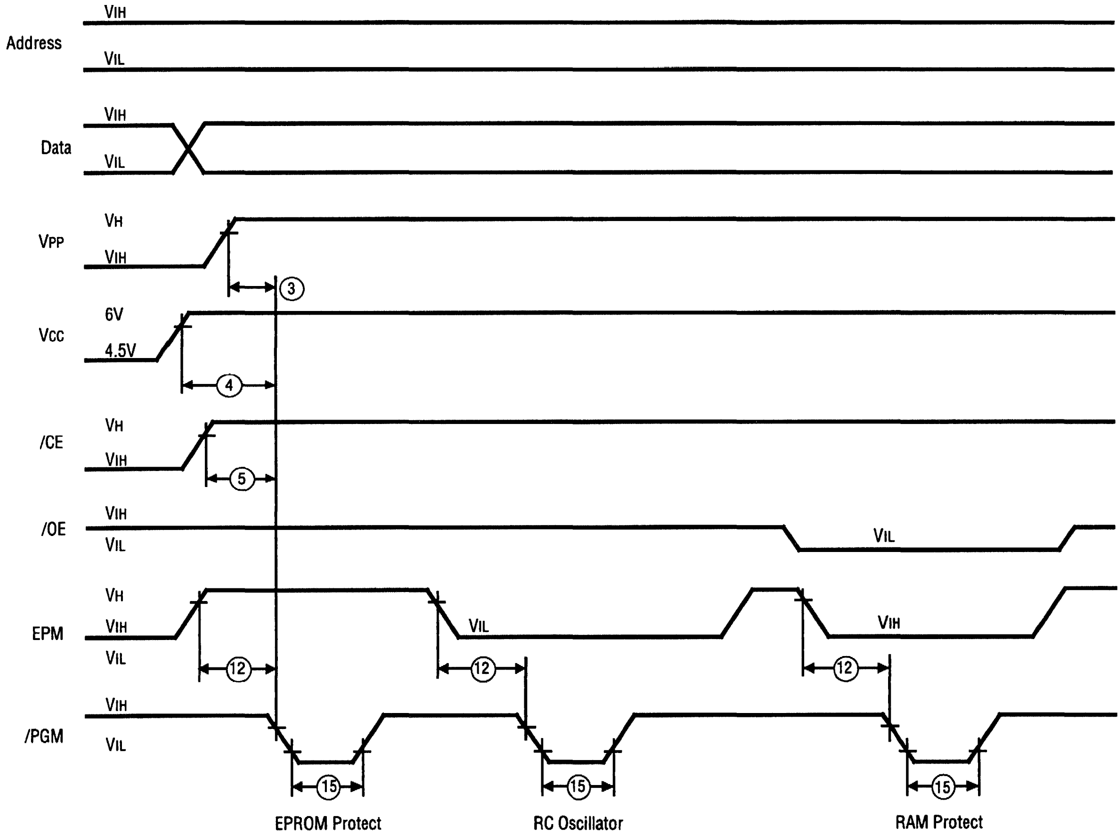
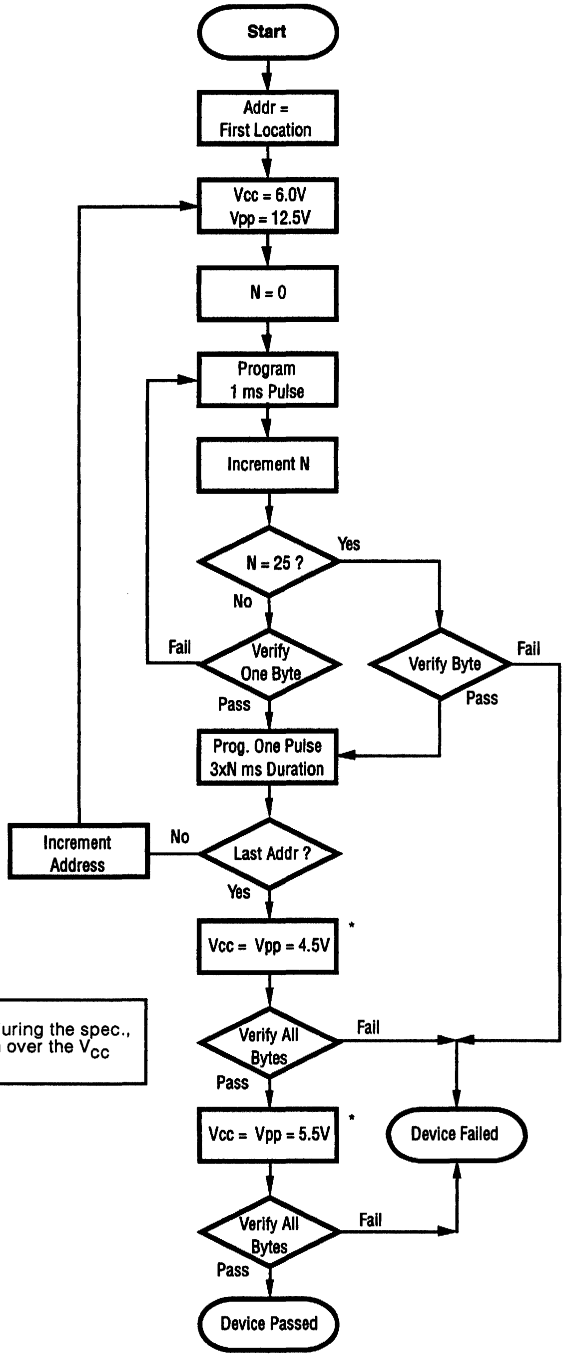


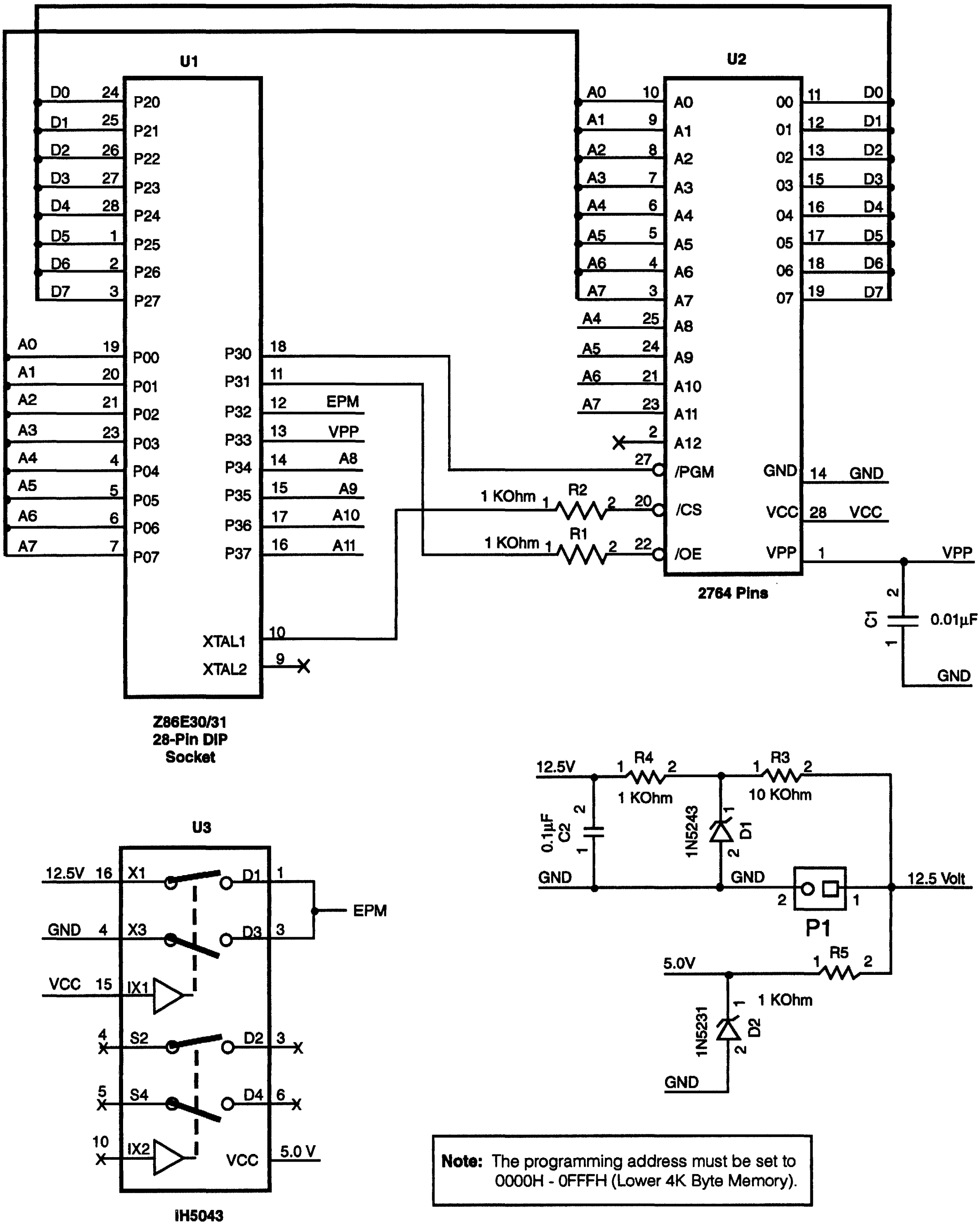
Figure 23. Timing Diagram of EPROM Protect, RAM Protect, and RC OSC Modes

FUNCTIONAL DESCRIPTION (Continued)



Note: * To ensure proper operations during the spec., Zilog recommends verification over the V_{CC} range of the device V_{CC} spec.

Figure 24. Z86E30/E31 Programming Algorithm



Note: The programming address must be set to 0000H - 0FFFH (Lower 4K Byte Memory).

Figure 25. Z86E30/E31 Programming Adaptor Circuitry

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
V_{IHM}**	Max Input Voltage		7	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp		†	C
	Power Dissipation		2.2	W

Notes:
* Voltage on all pins with respect to Ground.
** Applies to all Port pins, except Port 31, 32, 33 and must limit current going into and out of Port pin to 250 µA maximum.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 26).

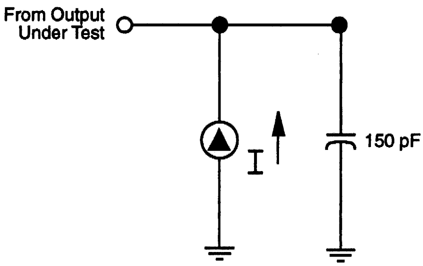


Figure 26. Test Load Configuration

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V; f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

V_{CC} SPECIFICATION

V_{CC} = 5.0V ±0.5V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} Note[3]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	5.0V		V_{CC} + 0.5V		V	I_{IN} <250 µA	[7]
V_{CH}	Clock Input High Voltage	5.0V	0.7 V_{CC}	V_{CC} + 0.3V	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	5.0V	V_{SS} –0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	5.0V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		[7]
V_{IL}	Input Low Voltage	5.0V	V_{SS} –0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage (Low EMI Mode)	5.0V 5.0V	V_{CC} –0.4 V_{CC} –0.4		4.8 4.8	V V	I_{OH} = –2.0 mA I_{OH} = –0.5 mA	[9] [8]
V_{OL1}	Output Low Voltage (Low EMI Mode)	5.0V 5.0V		0.4 0.4	0.1 0.1	V V	I_{OL} = +4.0 mA I_{OL} = +1.0 mA	[9] [8]
V_{OL2}	Output Low Voltage	5.0V		1.5	0.3	V	I_{OL} = +12 mA, 3 Pin Max	[9]
V_{OFFSET}	Comparator Input Offset Voltage	5.0V		50	10	mV		
I_{IL}	Input Leakage	5.0V	–10	+10	< 1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	5.0V	–10	+10	< 1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current (Standard Mode)	5.0V		16 20	15 18	mA mA	@ 8 MHz @ 12 MHz	[4,5,11] [4,5,11]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock-driven XTAL	0.3 mA	6.0	mA	8 MHz
Crystal or resonator	3.5 mA	6.0	mA	8 MHz

[2] V_{SS}=0V=GND.
[3] V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum T_{POR} timeout. V_{CC} specified at 4.5V to 5.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] Except clock pins and Port 3 input pins in EPROM mode.
[8] Port Low EMI mode.
[9] Port STD mode.
[10] SMR Reg Bit D1=1.
[11] Z86E30 only.

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC} Note[3]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Standard Mode)	5.0V		6.0	3.5	mA	HALT mode V_{IN} = 0V, V_{CC} V_{CC} @ 8 MHz	[4,5]
		5.0V		3.0	1.50	mA	Clock Divide-by-16 @ 8 MHz	[4,5]
I_{CC}	Supply Current (SCLK/TCLK = XTAL)	5.0V		7.5	5.0	mA	@ 2 MHz	[4,5,10]
		5.0V		12.0	8.0	mA	@ 4 MHz	[4,5,10]
I_{CC1}	Standby Current (SCLK/TCLK = XTAL)	5.0V		2.0	1.0	mA	@ 2 MHz	[4,5,10]
		5.0V		3.0	1.5	mA	@ 4 MHz	[4,5,10]
I_{CC1}	(Standard Mode)	5.0V		2.0	0.75	mA	Clock Divide-by-16 @ 2 MHz	[4,5]
		5.0V		2.0	1.0	mA	Clock Divide-by-16 @ 4 MHz	[4,5]
I_{CC2}	Standby Current	5.0V		10	2	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running	[6]
		5.0V		800	450	µA	STOP mode V_{IN} =0V, V_{CC} WDT is Running	[6]
I_{ALL}	Auto Latch Low Current	5.0V		–10	–5	µA	0V < V_{IN} < V_{CC}	
I_{ALH}	Auto Latch High Current	5.0V		20	10	µA	0V < V_{IN} < V_{CC}	
T_{POR}	Power-On Reset	5.0V	2.5		4.5	ms		[3]
V_{RST}	Auto Reset Voltage			3.0	2.6	V		

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock-driven XTAL	0.3 mA	6.0	mA	8 MHz
Crystal or resonator	3.5 mA	6.0	mA	8 MHz

[2] V_{SS}=0V=GND.
[3] V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum T_{POR} timeout. V_{CC} specified at 4.5V to 5.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1=CL2=100 pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] Except clock pins and Port 3 input pins in EPROM mode.
[8] Port Low EMI mode.
[9] Port STD mode.
[10] SMR Reg Bit D1=1.
[11] Z86E30 only.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram (Standard Mode for SCLK/TCLK + XTAL/2)

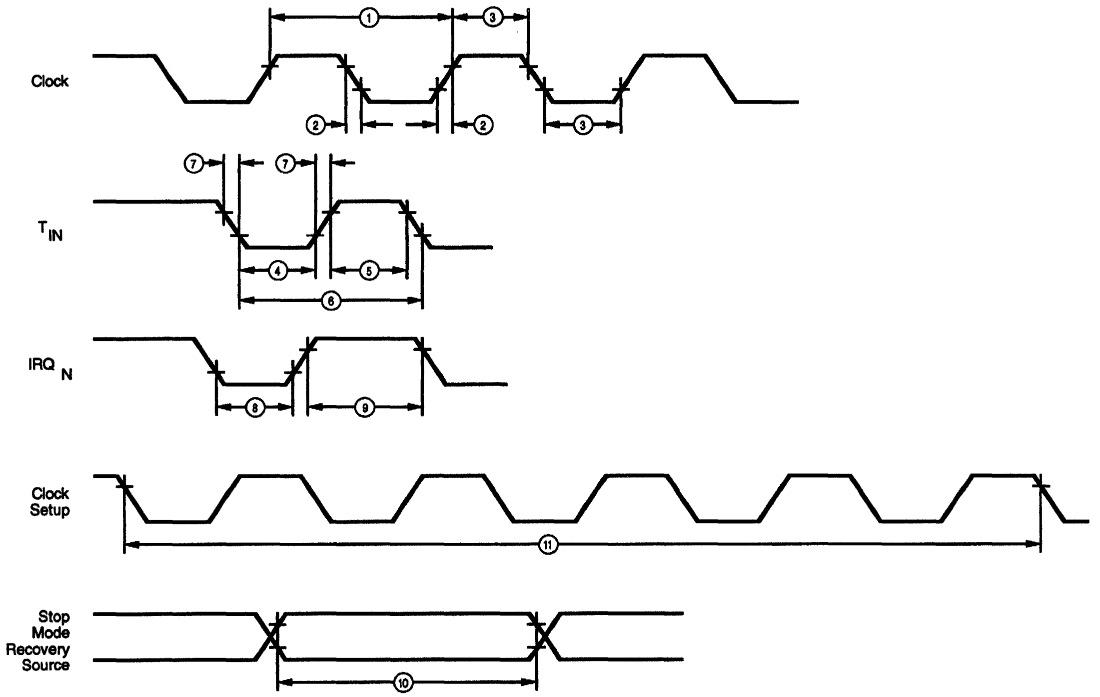

Figure 27. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Standard Mode)

				T_A = 0°C to +70°C					
			V_{CC}	8 MHz [11]		12 MHz [11]			
No	Symbol	Parameter	Note[6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	5.0V	125	DC	83.3	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	5.0V		25		15	ns	[1]
3	TwC	Input Clock Width	5.0V	62.5		41.6		ns	[1]
4	TwTinL	Timer Input Low Width	5.0V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	5.0V	5TpC		5TpC			[1]
6	TpTin	Timer Input Period	5.0V	8TpC		8TpC			[1]
7	TpTin TfTin	Timer Input Rise and Fall Timers	5.0V		100		100	ns	[1]
8A	TwIL	Int. Request Low Time	5.0V	70		70		ns	[1,2]
8B	TwIL	Int. Request Low Time	5.0V	5TpC		5TpC			[1,3]
9	TwIH	Int. Request Input High Time	5.0V	5TpC		5TpC			[1,2]
10	Twsm	STOP-Mode Recovery Width Spec	5.0V	12		12		ns	
11	Tost	Oscillator Start-up Time	5.0V	5TpC		5TpC			[4]
12	Twdt	Watch-Dog Timer Delay Time	5.0V	5		5		ms	D1 = 0 [5] [7]
			5.0V	15		15		ms	D1 = 0 [5] [8]
			5.0V	25		25		ms	D1 = 1 [5] [9]
			5.0V	100		100		ms	D1 = 1 [5] [10]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] Interrupt request through Port 3 (P30).
[4] SMR – D5 = 0.
[5] Reg. WDTMR.
[6] 5.0V .±0.5V
[7] Reg. WDTMR D1 = 0, D0 = 0.
[8] Reg. WDTMR D1 = 0, D0 = 1.
[9] Reg. WDTMR D1 = 1, D0 = 0.
[10] Reg.WDTMR D1 = 1, D0 = 1.
[11] Z86E30 max frequency = 12 MHz; Z86E31 max frequency = 8 MHz.

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AC ELECTRICAL CHARACTERISTICS

Handshake Timing Diagrams

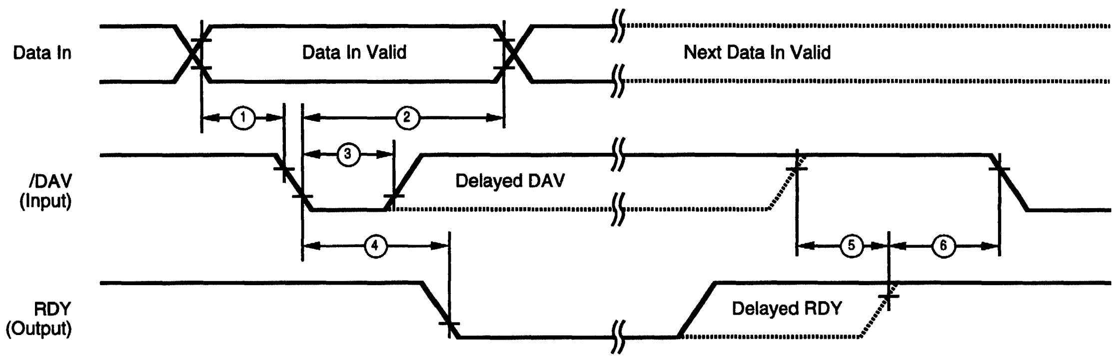


Figure 28. Input Handshake Timing

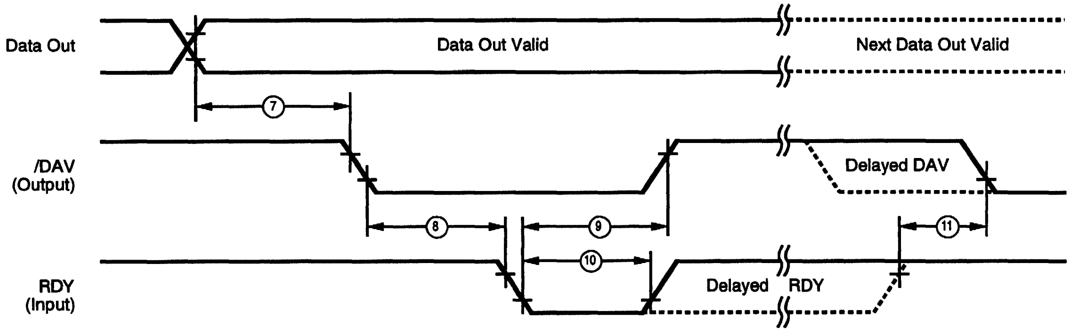


Figure 29. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Table - Standard Mode

No	Symbol	Parameter	V_{CC} Note[1]	T_A = 0°C to +70°C 8 MHz, 12 MHz [2] Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	5.0V	0		IN
2	ThDI(DAV)	Data In Hold Time	5.0V	115		IN
3	TwDAV	Data Available Width	5.0V	110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	5.0V		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	5.0V		80	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	5.0V	0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay	5.0V	63		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	5.0V	0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	5.0V		115	OUT
10	TwRDY	RDY Width	5.0V	80		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0V	80	80	OUT

Note:
[1] 5.0V ±0.5V Standard operating temperature range 0°C to +70°C.
[2] Z86E30 max frequency = 12 MHz; Z86E31 max frequency = 8 MHz.

EXPANDED REGISTER FILE CONTROL REGISTERS

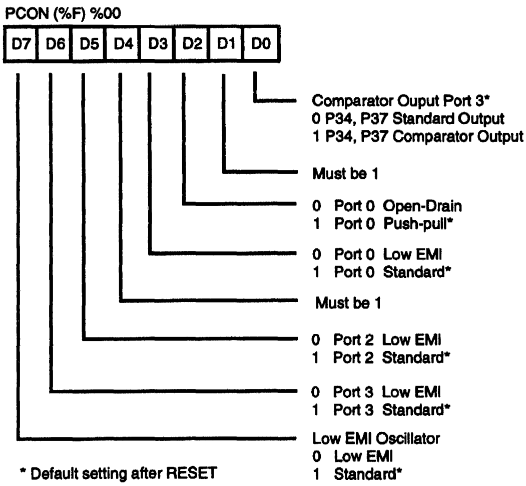


Figure 30. Port Configuration Register (Write Only)

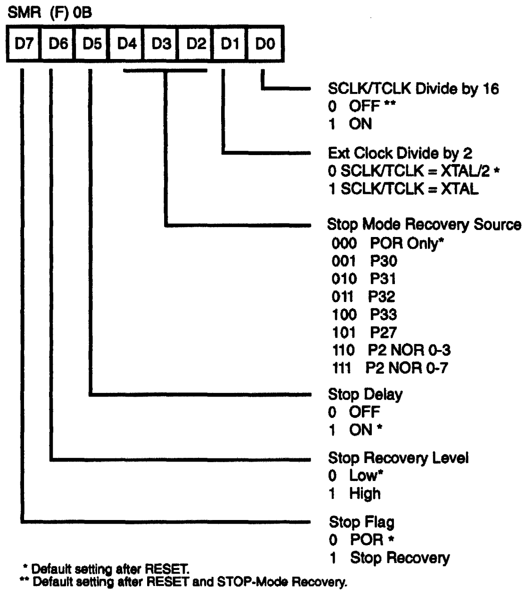


Figure 31. STOP-Mode Recovery Register (Write Only Except Bit D7, Which is Read Only)

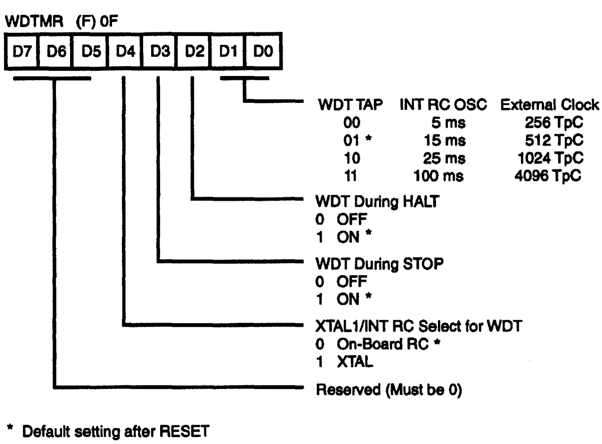


Figure 32. Watch-Dog Timer Mode Register (Write Only)

Z8® CONTROL REGISTER DIAGRAMS

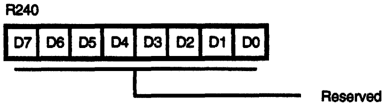


Figure 33. Reserved

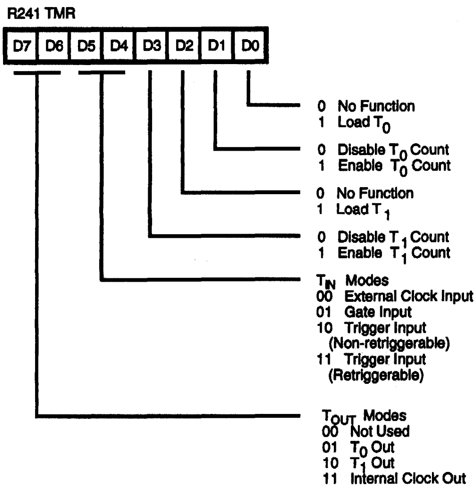


Figure 34. Timer Mode Register
($F1_H$: Read/Write)

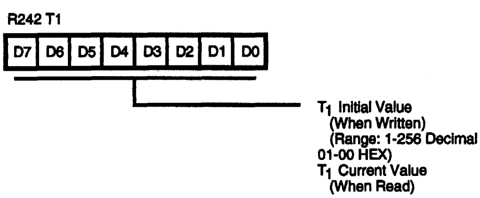


Figure 35. Counter Timer 1 Register
($F2_H$: Read/Write)

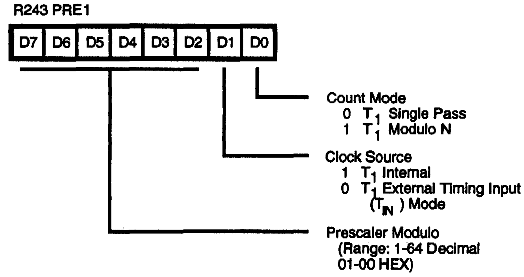


Figure 36. Prescaler 1 Register
($F3_H$: Write Only)

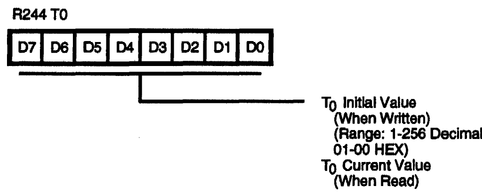


Figure 37. Counter/Timer 0 Register
($F4_H$: Read/Write)

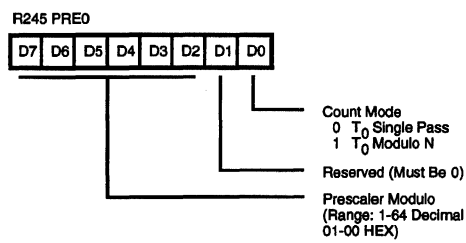


Figure 38. Prescaler 0 Register
($F5_H$: Write Only)

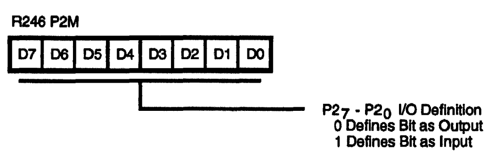


Figure 39. Port 2 Mode Register
($F6_H$: Write Only)

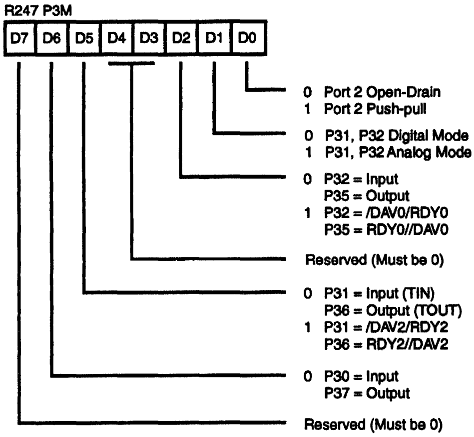


Figure 40. Port 3 Mode Register ($F7_H$: Write Only)

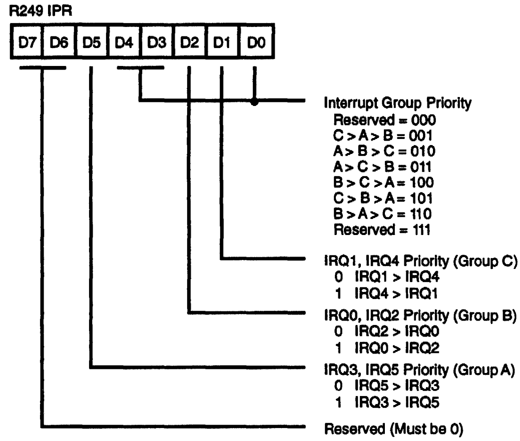


Figure 42. Interrupt Priority Register ($F9_H$: Write Only)

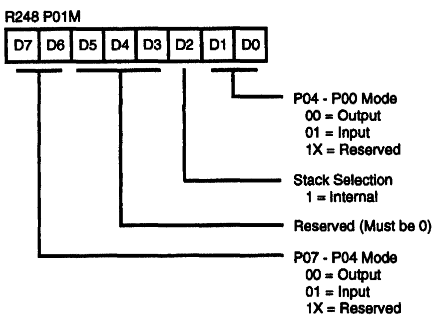


Figure 41. Port 0 and 1 Mode Register ($F8_H$: Write Only)

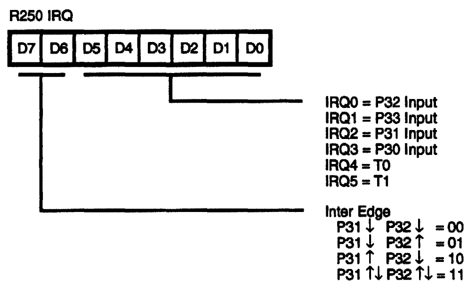
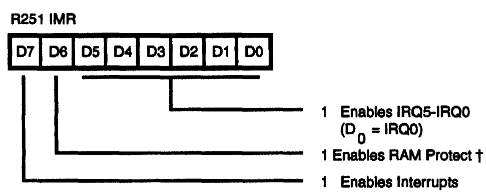


Figure 43. Interrupt Request Register (FA_H: Read/Write)



† RAM Protect option must be previously selected.

Figure 44. Interrupt Mask Register (FB_H: Read/Write)

Z8® CONTROL REGISTER DIAGRAMS (Continued)

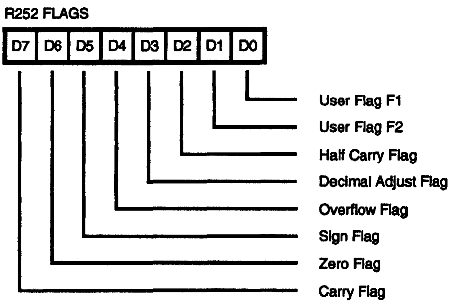


Figure 45. Flag Register (FC_H: Read/Write)

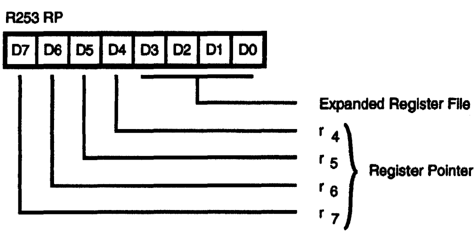


Figure 46. Register Pointer (FD_H: Read/Write)

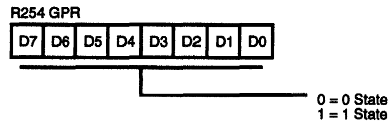


Figure 47. General-Purpose Register

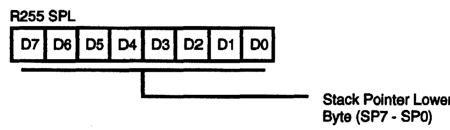


Figure 48. Stack Pointer (FF_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

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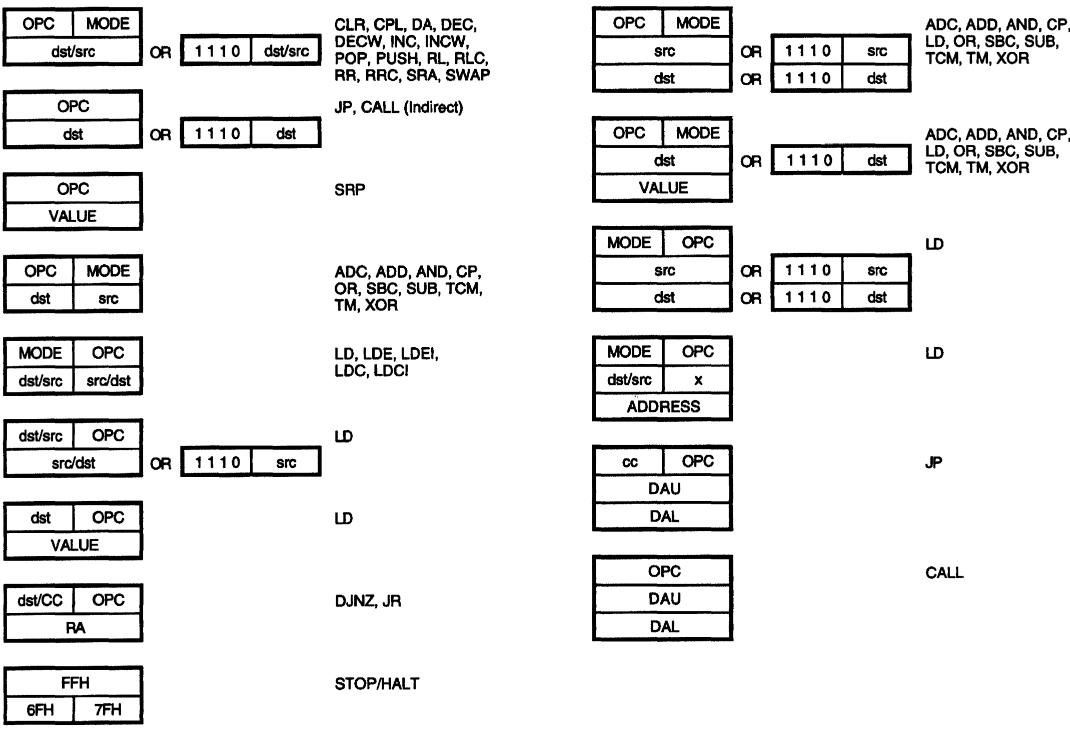
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions **Three-Byte Instructions**

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

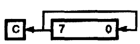
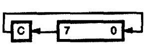
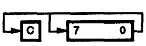
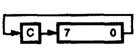
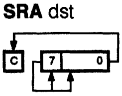
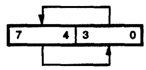
dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst –src – C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst – src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

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† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

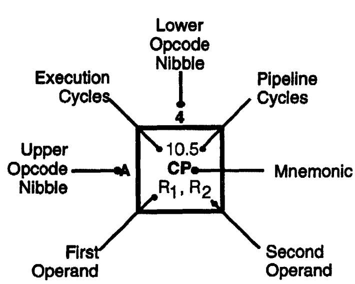
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) / Upper Nibble (Hex)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1							↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1							↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** Irr1, r2	18.0 **LDCI** Irr1, Ir2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2	2	2	2	3	3	3	3	2	2	2	2	2	3	3	1



Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_1 = Dst address
R_2 or r_2 = Src address

Sequence:
Opcode, First Operand,
Second Operand

Note: The blanks are reserved.

* 2-byte instruction appears as a 3-byte instruction.

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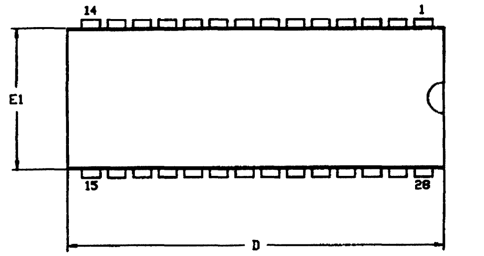
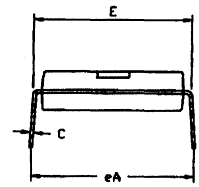
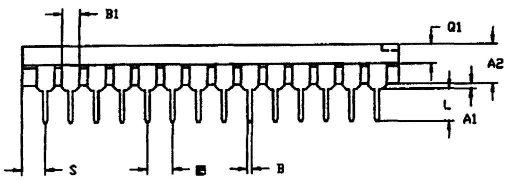
PACKAGE INFORMATION







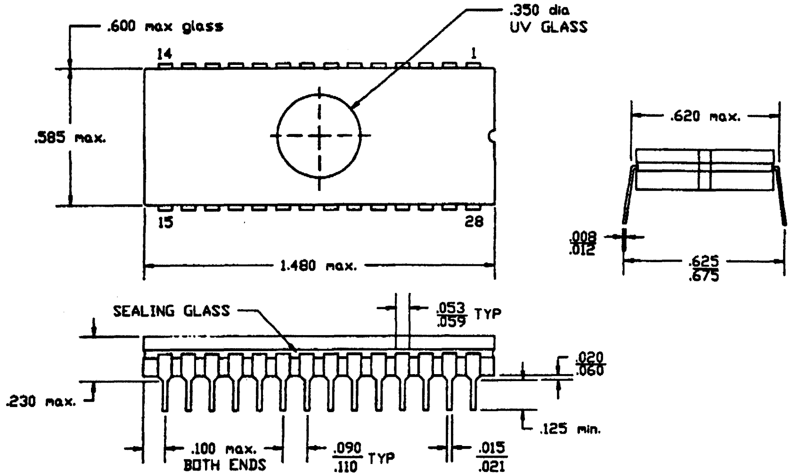
OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	0.81	.020	.032
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.52	1.78	.060	.070
	02	1.27	1.52	.050	.060
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.51	.610	.650
L		3.18	3.81	.125	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

28-Pin DIP Package Diagram

PACKAGE INFORMATION (Continued)



28-Pin Window Cerdip Package Diagram

ORDERING INFORMATION

Z86E30 (12 MHz)

28-Pin DIP	28-Pin Cerdip Window Lid
Z86E3012PSC	Z86E3012KSE

Z86E31 (8 MHz)

28-Pin DIP	28-Pin Cerdip Window Lid
Z86E3108PSC	Z86E3108KSE

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
K= Cerdip Window Lid

Temperature
S = 0°C to +70°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard
E = Hermetic Standard

Example:

Z 86E30 12 P S C is a Z86E30, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 12 — Speed
- 86E30 — Product Number
- Z — Zilog Prefix

Z86E30/E31 CMOS Z8® OTP CCP™
Consumer Controller Processor
8

Z86C40 CMOS Z8® 4K ROM CCP™
Consumer Controller Processor
9

Z86E40 CMOS Z8® 8-Bit OTP CCP™
Consumer Controller Processor
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Z86C40

CMOS Z8® 4K ROM CCP™ CONSUMER CONTROLLER PROCESSOR

FEATURES

- 8-Bit, CMOS MCU with 4 Kbytes of ROM and 256 Bytes of RAM (236 Bytes for General Purpose)
- Package Styles: 40-Pin DIP, 44-Pin PLCC, 44-Pin QFP
- Software Programmable Low EMI Modes
- Programmable Open-Drain Mode on Port 0, Port1, and Port 2
- Low-Power Consumption: 40 mW (Typical @ 5.0V)
- Fast Instruction Pointer: 750 ns @ 16 MHz
- Two Standby Modes: STOP and HALT
- 32 Input/Output Lines (Three with Comparator Inputs)
- 25 Digital CMOS Level, Schmitt-Triggered Inputs
- Three Digital CMOS Level Inputs
- Three Expanded Register File Control Registers
- Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speeds up to 12 MHz and 16 MHz
- Low Voltage Protection
- Watch-Dog/Power-On Reset Timers
- Permanently Enabled WDT Option
- Two Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- RAM and ROM Protect
- Programmable Interrupt Polarity
- Auto Latches

GENERAL DESCRIPTION

The Z86C40 CCP™ (Consumer Controller Processor) is a member of Zilog's Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 4 Kbytes of ROM and 236 bytes of general-purpose RAM, this low cost, low power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C40 architecture is characterized by Zilog's 8-bit microcontroller core with an Expanded Register File (ERF) to allow access to register mapped peripheral and I/O circuits. The Z86C40 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many industrial, automotive, computer peripherals, and consumer applications.

With ROM/ROMless selectivity, the Z86C40 provides both external memory and pre-programmed ROM, which enables this Z8 microcontroller to be used in high-volume applications, or where code flexibility is required.

GENERAL DESCRIPTION (Continued)

For applications demanding powerful I/O capabilities, the Z86C40 provides 32 pins dedicated to input and output. These lines are grouped into four ports with eight lines each, and are configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory (Figure 1).

Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, Data Memory, and Expanded Register File (ERF). The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The Expanded Register File consists of two control registers.

To unburden the system from coping with the real-time tasks, such as counting/timing and data communication, the Z86C40 offers two on-chip counter/timers with a large number of user-selectable modes. Additionally, two on-board comparators allow analog signals to be processed using a common reference voltage.

Note: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

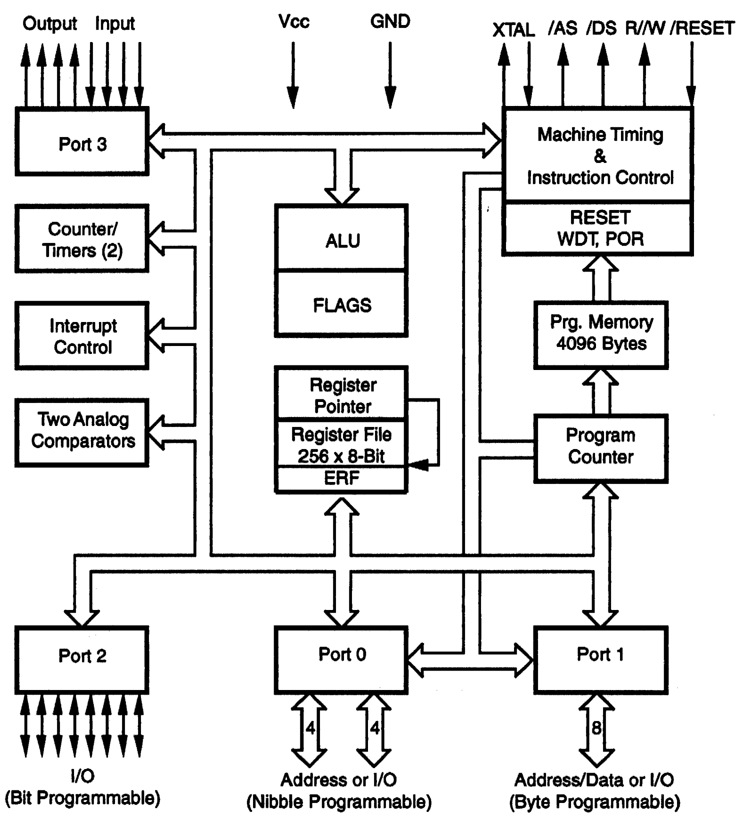

Figure 1. Functional Block Diagram

PIN DESCRIPTION

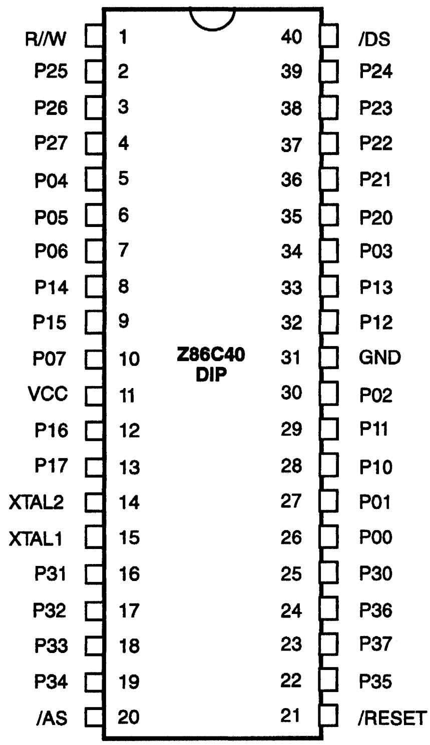

Figure 2. 40-Pin DIP Pin Configuration

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	R/W	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	In/Output
5-7	P04-P06	Port 0, Pins 4,5,6	In/Output
8-9	P14-P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	In/Output
28-29	P10-P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

PIN DESCRIPTION (Continued)

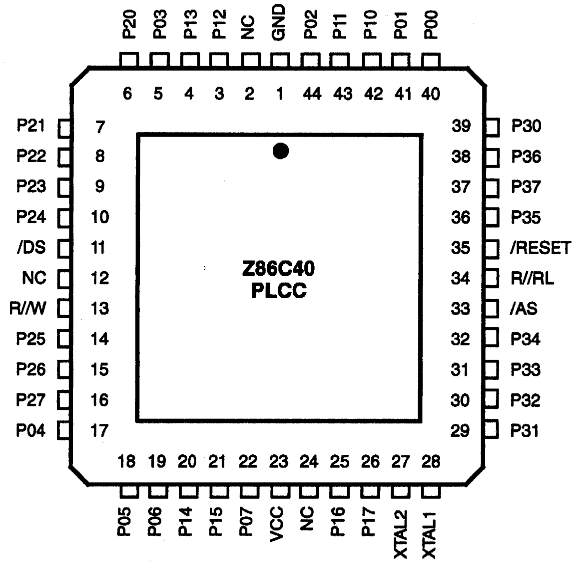

Figure 3. 44-Pin PLCC Pin Configuration

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	GND	Ground	
2	NC	Not Connected	
3-4	P12-P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	NC	Not Connected	
13	R/W	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	In/Output
17-19	P04-P06	Port 0, Pins 4,5,6	In/Output
20-21	P14-P05	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23	V_{CC}	Power Supply	
24	NC	Not Connected	
25-26	P16-P17	Port 1, Pins 6,7	In/Output

Pin #	Symbol	Function	Direction
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29-31	P31-P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless select	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-P01	Port 0, Pins 0,1	In/Output
42-43	P10-P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

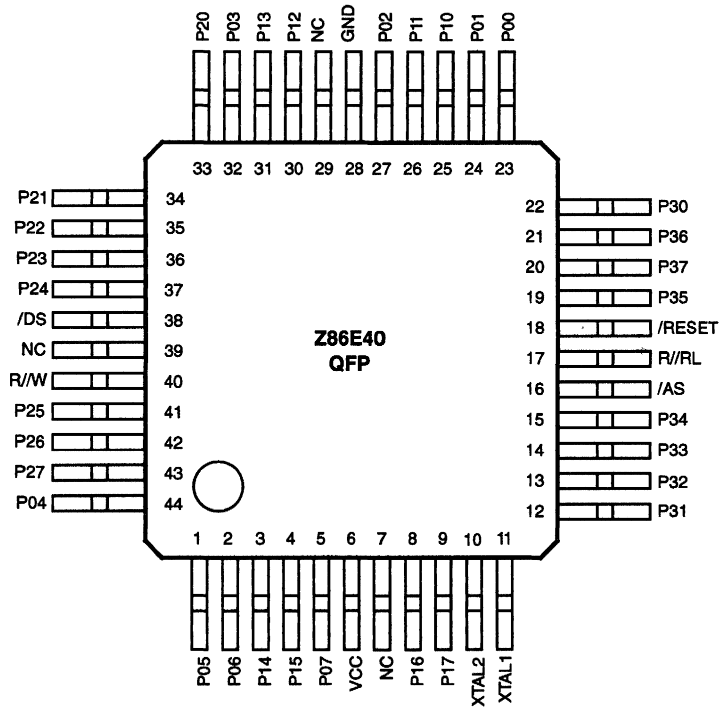

Figure 4. 44-Pin QFP Pin Configuration

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	In/Output	21	P36	Port 3, Pin 6	Output
3-4	P14-P05	Port 1, Pins 4,5	In/Output	22	P30	Port 3, Pin 0	Input
5	P07	Port 0, Pin 7	In/Output	23-24	P00-P01	Port 0, Pin 0,1	In/Output
6	V_{CC}	Power Supply		25-26	P10-P11	Port 1, Pins 0,1	In/Output
7	NC	Not Connected		27	P02	Port 0, Pin 2	In/Output
8-9	P16-P17	Port 1, Pins 6,7	In/Output	28	GND	Ground	
10	XTAL2	Crystal Oscillator	Output	29	NC	Not Connected	
11	XTAL1	Crystal Oscillator	Input	30-31	P12-P13	Port 1, Pins 2,3	In/Output
12-14	P31-P33	Port 3, Pins 1,2,3	Input	32	P03	Port 0, Pin 3	In/Output
15	P34	Port 3, Pin 4	Output	33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
16	/AS	Address Strobe	Output	38	/DS	Data Strobe	Output
17	R//RL	ROM/ROMless select	Input	39	NC	Not Connected	
18	/RESET	Reset	Input	40	R/W	Read/Write	Output
19	P35	Port 3, Pin 5	Output	41-43	P25-P27	Port 2, Pins 5,6,7	In/Output
20	P37	Port 3, Pin 7	Output	44	P04	Port 0, Pin 4	In/Output

PIN FUNCTIONS

/ROMless (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to $V_{CC,}$ the device functions normally as a Z8 ROM version).

Note: When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to $V_{CC.}$

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1 *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network, or an external single-phase clock to the on-chip oscillator input.

XTAL2 *Crystal 2* (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R//W (output, write Low). Read/Write, the R//W signal is Low when the Z86C40 is writing to the external program or data memory.

Port 0 (P00-P07). Port 0 is an 8-bit, bidirectional, CMOS compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03-P00 input/output and P07-P04 input/output), or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04-P07. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after reset.)

Port 0 is set in the high-impedance mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R//W (Figure 5).

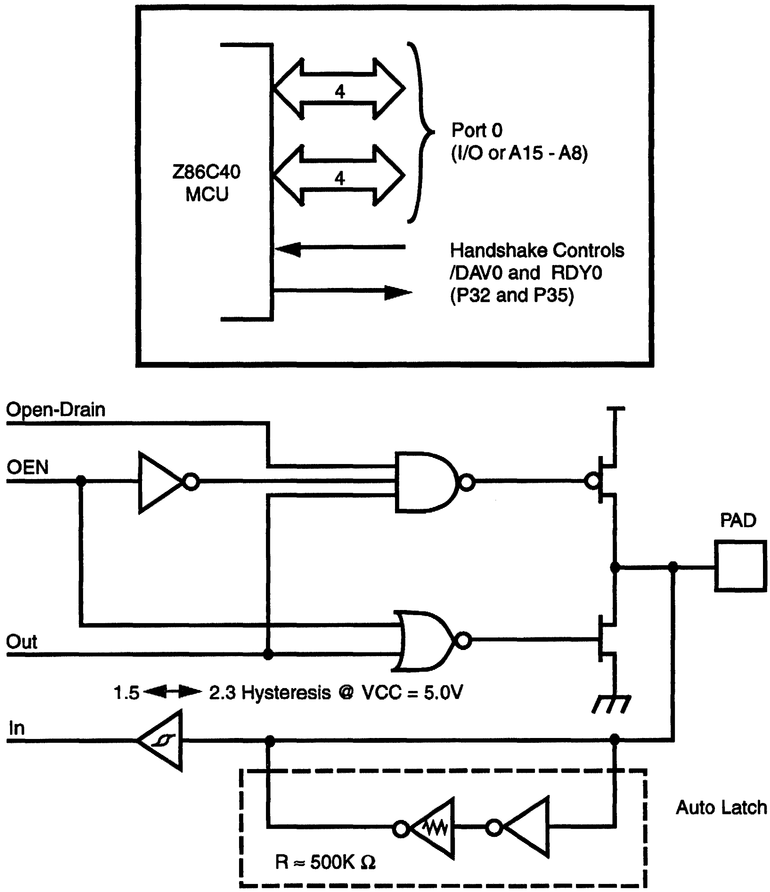

Figure 5. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P10-P17). Port 1 is an 8-bit, bidirectional, CMOS compatible port (Figure 6), with multiplexed Address (A7-A0) and Data (D7-D0) ports. For the Z86C40 ROM device, these eight I/O lines are programmed as inputs or outputs, or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and byte-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software.

Port 1 may be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). Memory locations greater than 4095 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the Z86C40 to share common resources in multiprocessor and DMA applications.

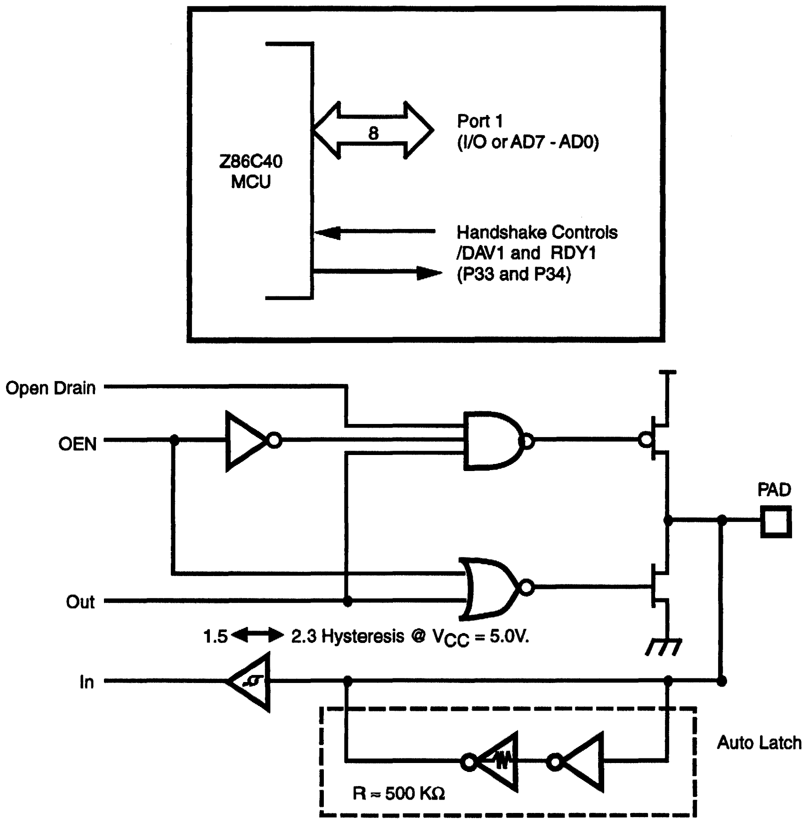

Figure 6. Port 1 Configuration

Port 2 (P20-P27). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software.

Port 2 may be placed under handshake control. In this Handshake Mode, Port 3 lines P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 7).

9

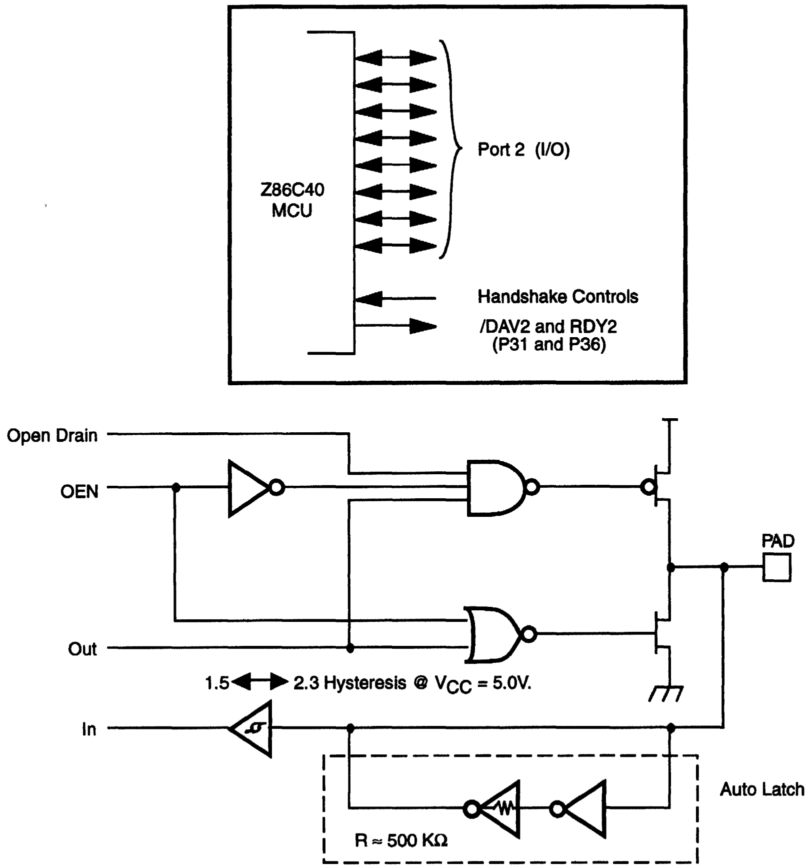

Figure 7. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P30-P37). Port 3 is an 8-bit, CMOS compatible, four fixed inputs (P30-P33) and four fixed outputs (P34-P37), and is configured under software control for Input/Output, Counter/Timers, interrupt, port handshake, and Data Memory functions. Port 3, pin 0 input is Schmitt-triggered, and pins P31, P32, and P33 are standard CMOS inputs (no Auto Latches). Pins P34, P35, P36, P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit 1). For Interrupt functions, Port 3, pin 0 and pin 3 are falling edge interrupt inputs. P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and bit 7). P33 is the comparator reference voltage input when in Analog Mode. Access to Counter/Timers 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}); Data Memory Select (/DM, see Table 4, Figure 37).

P34 output can be software-programmed to function as a Data Memory Select (DM). The Port 3 mode register (P3M) bit D3, D4 selects this function. When accessing external Data Memory, the P34 goes active Low; when accessing external program memory, the P34 goes High.

Table 4. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T_{IN}	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT		AN1-OUT			R/D		/DM
P35	OUT				R/D			
P36	OUT	T_{OUT}					R/D	
P37	OUT		AN2-OUT					

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Auto Latch. The Auto-Latch instruction puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Note: Deletion of all Port Auto Latches is available as a ROM Mask option. The Auto Latch Delete option is selected by the customer when the ROM code is submitted.

Comparator Inputs. Port 3, Pins P31 and P32 each have a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source. P34 and P37 outputs the comparator outputs by software-programming the PCON Reg. bit D0 to 1.

/RESET (input, active Low). Initializes the MCU. Reset is accomplished either through Power-On Reset, Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Reset, the internally generated reset is driving the reset pin Low for the POR time. ***Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions.*** Pull-up is provided internally.

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86C40 is equipped with a reset filter of four external clocks (4 TpC). If the external reset signal is less than 4 TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000C (HEX), 5-10 TpC cycles after the RST is released. For Power-On Reset, the reset output time is T_{POR} ms.

Once program execution begins, /AS and /DS toggles only for external memory accesses. The Z86C40 does not reset WDTMR, SMR, P2M, PCON, and P3M registers on a STOP-Mode Recovery operation.

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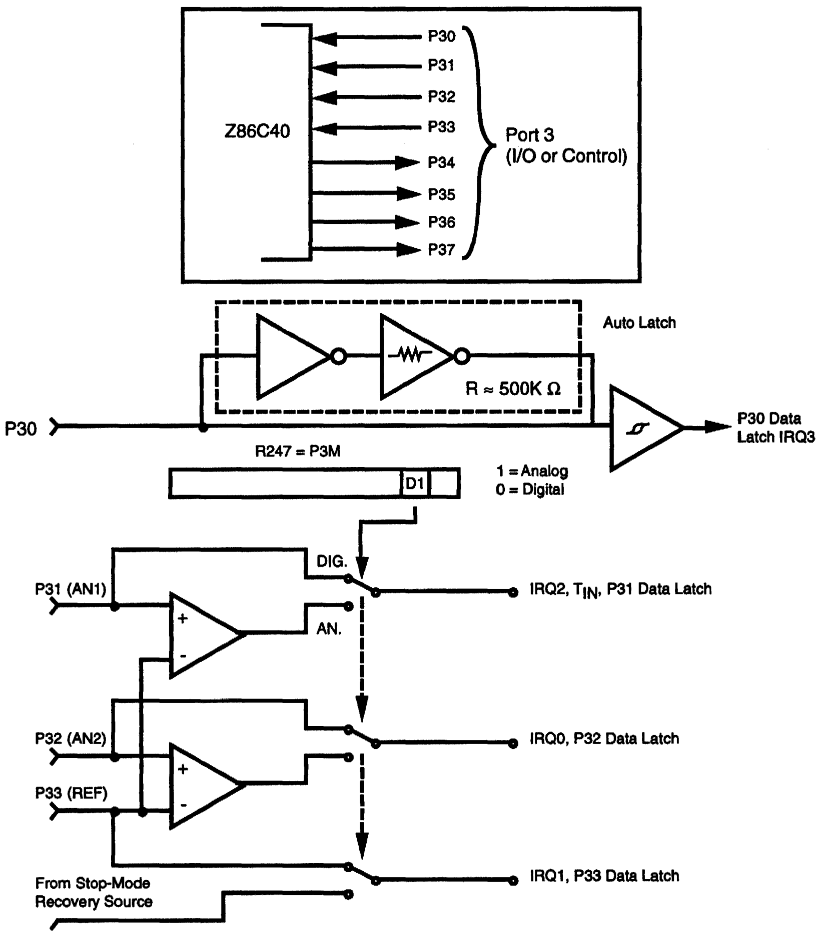

Figure 8a. Port 3 Configuration

PIN FUNCTIONS (Continued)

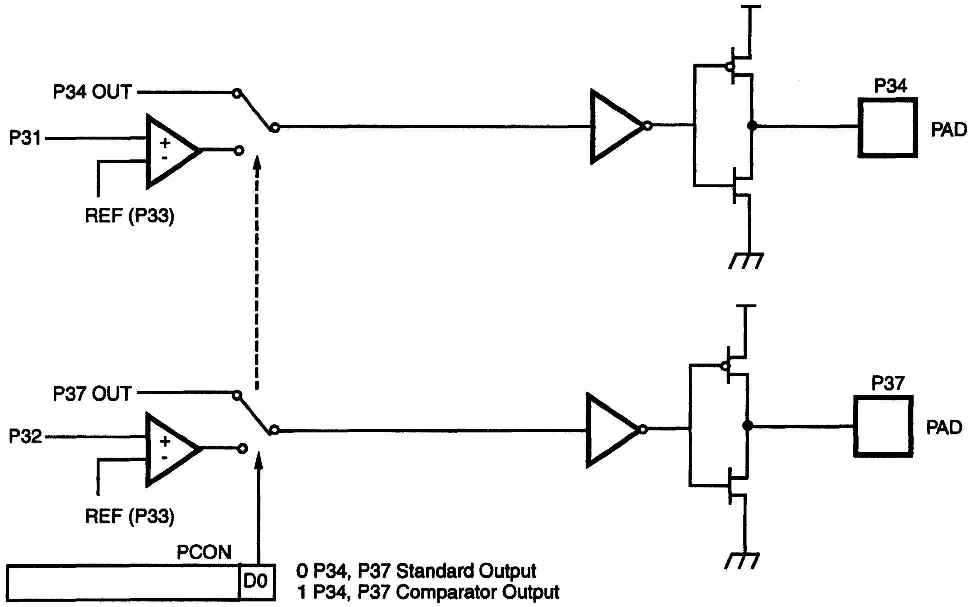

Figure 8b. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The Z86C40 MCU incorporates the following special functions to enhance the standard Z8® architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- External Reset
- Low Voltage Recovery

Auto Power-On Reset circuitry is built into the Z86C40, eliminating the need for an external reset circuit to reset upon power-up. The internal pull-up resistor is on the Reset pin, so a pull-up resistor is not required; however, in high EMI (noisy) environment, it is recommended that a small value pull-up resistor be used.

Program Memory. The Z86C40 addresses up to 4 Kbytes of internal program memory and 60 Kbytes of external memory (Figure 9). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, address 12 to address 4095 consists of on-chip mask-programmed ROM. At addresses 4096 and greater, the Z86C40 executes external program memory fetches through Port 0 and Port 1 in Address/Data mode.

The 4 Kbyte program memory is mask programmable. ***A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to Program Memory in all modes. ROM look-up tables cannot be used with this feature.***

The ROM Protect option is mask-programmable, to be selected by the customer when the ROM code is submitted.

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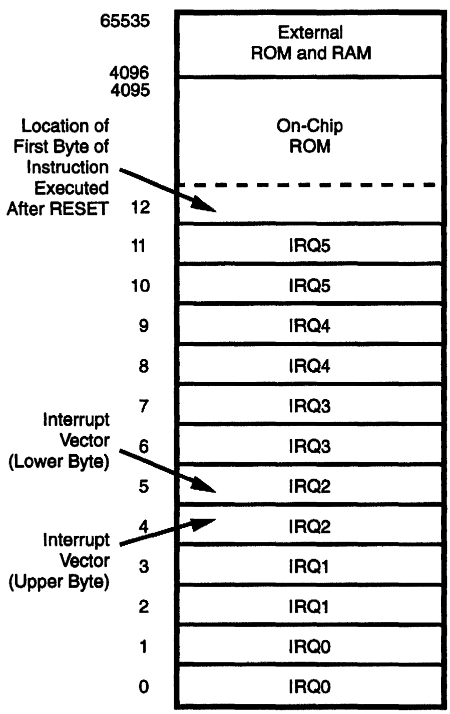


Figure 9. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Data Memory (/DM). The Z86C40 ROM version can address up to 60 Kbytes of external data memory beginning at location 4096. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 10). The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode.

Expanded Register File (ERF). The Z86C40 register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group (Figure 11). These register groups are known as the Expanded Register File (ERF). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 12). Three system configuration registers reside in the Expanded Register File at Bank F (PCON, SMR, WDTMR). The rest of the Expanded Register is not physically implemented, and is open for future expansion.

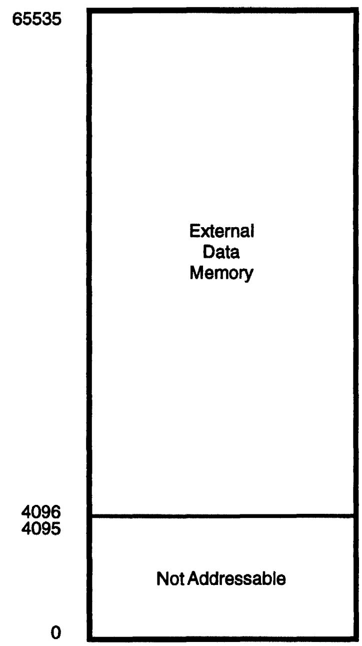
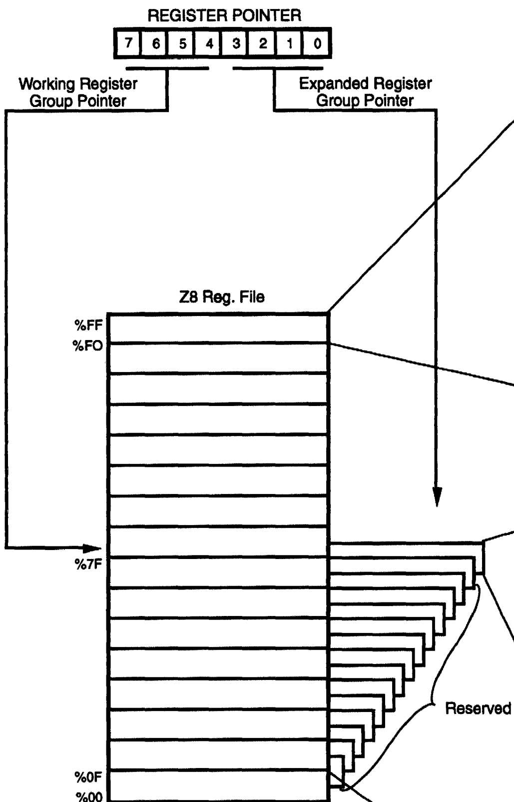


Figure 10. Data Memory Map



Z8® STANDARD CONTROL REGISTERS

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
	% FF	SPL	U	U	U	U	U	U	U	U
	% FE	SPH	U	U	U	U	U	U	U	U
	% FD	RP	0	0	0	0	0	0	0	0
	% FC	FLAGS	U	U	U	U	U	U	U	U
	% FB	IMR	0	U	U	U	U	U	U	U
	% FA	IRQ	0	0	0	0	0	0	0	0
	% F9	IPR	U	U	U	U	U	U	U	U
†	% F8	P01M	0	1	0	0	1	1	0	1
*	% F7	P3M	0	0	0	0	0	0	0	0
*	% F6	P2M	1	1	1	1	1	1	1	1
	% F5	PRE0	U	U	U	U	U	U	U	0
	% F4	T0	U	U	U	U	U	U	U	U
	% F3	PRE1	U	U	U	U	U	U	0	0
	% F2	T1	U	U	U	U	U	U	U	U
	% F1	TMR	0	0	0	0	0	0	0	0
	% F0	Reserved								

EXPANDED REG. GROUP (F)

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
*	% (F) 0F	WDTMR	U	U	U	0	1	1	0	1
	% (F) 0E	Reserved								
	% (F) 0D	Reserved								
	% (F) 0C	Reserved								
**	% (F) 0B	SMR	0	0	1	0	0	0	0	0
	% (F) 0A	Reserved								
	% (F) 09	Reserved								
	% (F) 08	Reserved								
	% (F) 07	Reserved								
	% (F) 06	Reserved								
	% (F) 05	Reserved								
	% (F) 04	Reserved								
	% (F) 03	Reserved								
	% (F) 02	Reserved								
	% (F) 01	Reserved								
*	% (F) 00	PCON	1	1	1	1	1	1	1	0

EXPANDED REG. GROUP (0)

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
*	% (0) 03	P3	1	1	1	1	U	U	U	U
*	% (0) 02	P2	U	U	U	U	U	U	U	U
	% (0) 01	P1	U	U	U	U	U	U	U	U
	% (0) 00	P0	U	U	U	U	U	U	U	U

(Bit columns D7–D0 give the RESET CONDITION.)

Notes:
U = Unknown
† For Z86C90/C89 (ROMless) Reset condition: "10110110"
* Will not be reset with a STOP-Mode Recovery.
** Will not be reset with a STOP-Mode Recovery, except bit D0.

Figure 11. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

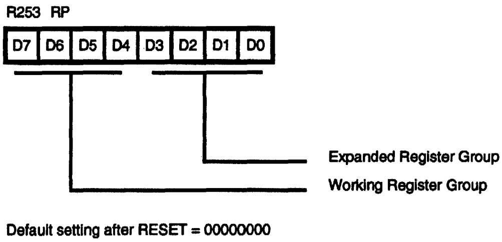


Figure 12. Register Pointer Register

Register File. The register file consists of four I/O port registers, 236 general-purpose registers and 15 control and status registers (R0-R3, R4-239 and R240-R255, respectively), plus three system configuration registers in the expanded register group. The instructions access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 13). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

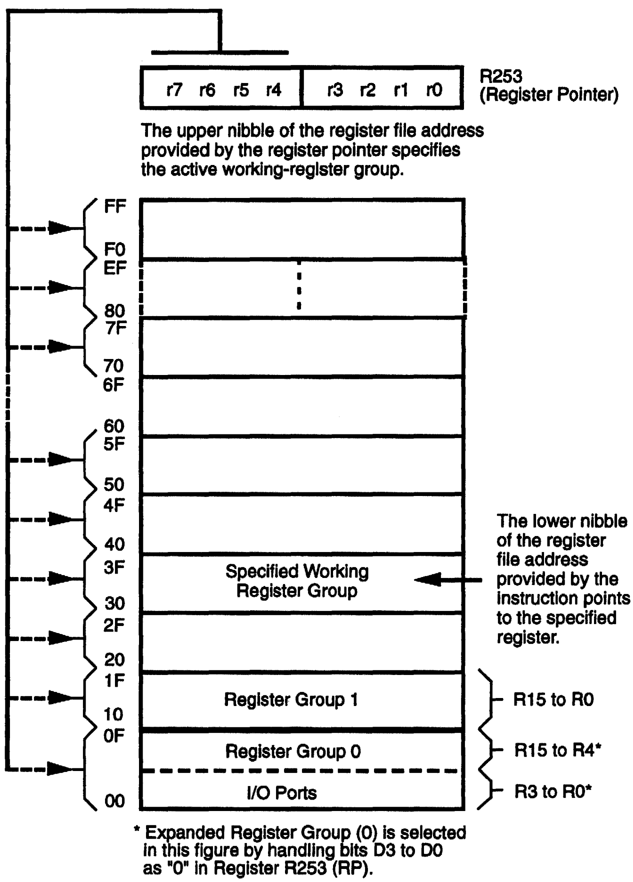


Figure 13. Register Pointer

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V.

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the IMR register, bit D6. A 1 in D6 enables RAM Protect.

Stack. The Z86C40 external data memory or the internal register file is used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack which can reside anywhere in the data memory for ROMless mode, but only from 4096 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). SPH is used as a general-purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 14).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, ***but not the prescalers***, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1. T_{IN} Mode is enabled by setting R243 PRE1 Bit D1 to 0.

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FUNCTIONAL DESCRIPTION (Continued)

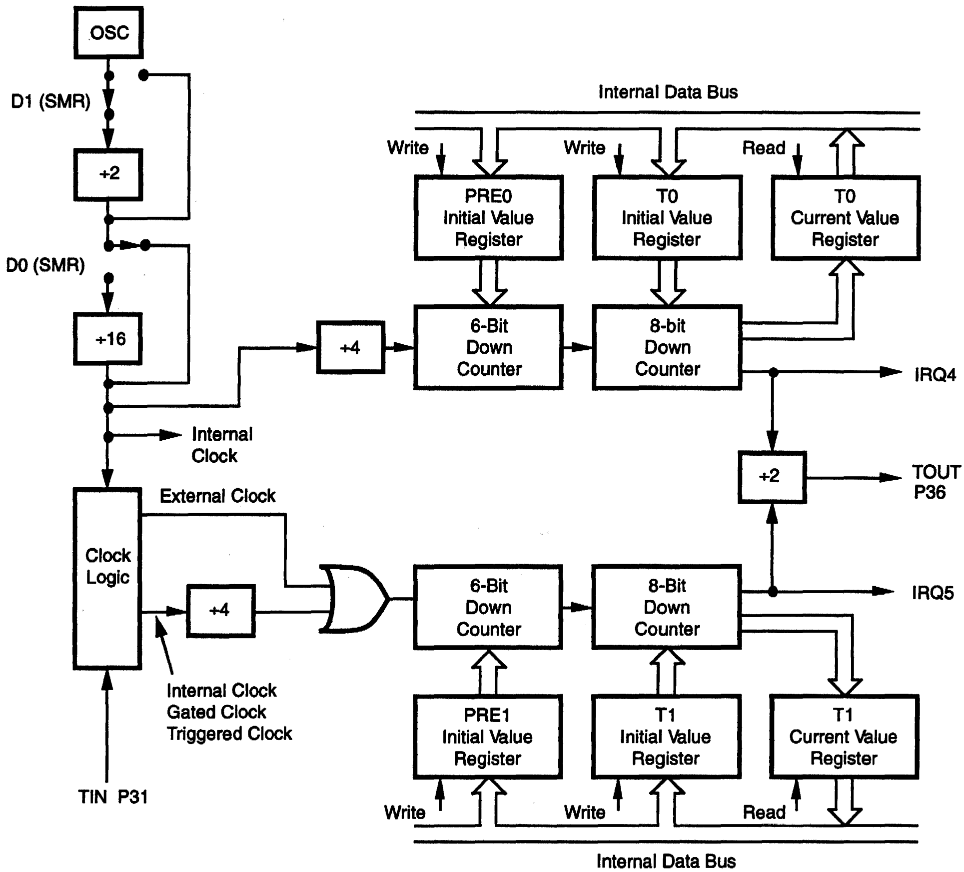


Figure 14. Counter/Timer Block Diagram

Interrupts. The Z86C40 has six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 15) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers (Table 5). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

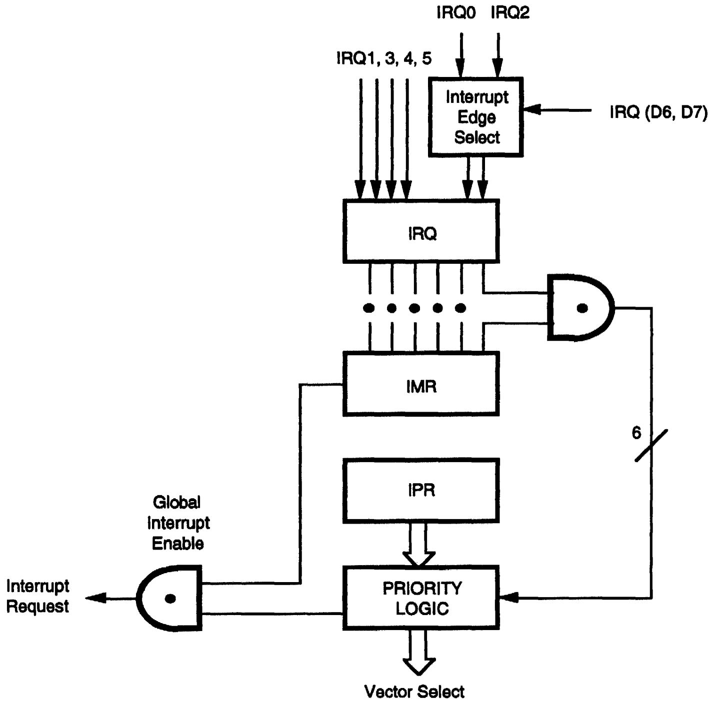


Figure 15. Interrupt Block Diagram

Table 5. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Fall Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

FUNCTIONAL DESCRIPTION (Continued)

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

All Z86C40 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6 . The configuration is shown in Table 6.

Table 6. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86C40 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 16 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce Ground noise injection into the oscillator. The RC oscillator option is mask-programmable on the Z86C40 and is selected by the customer at the time when the ROM code is submitted. (Note that the RC option is available up to 8 MHz.) The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 16).

Note: For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).

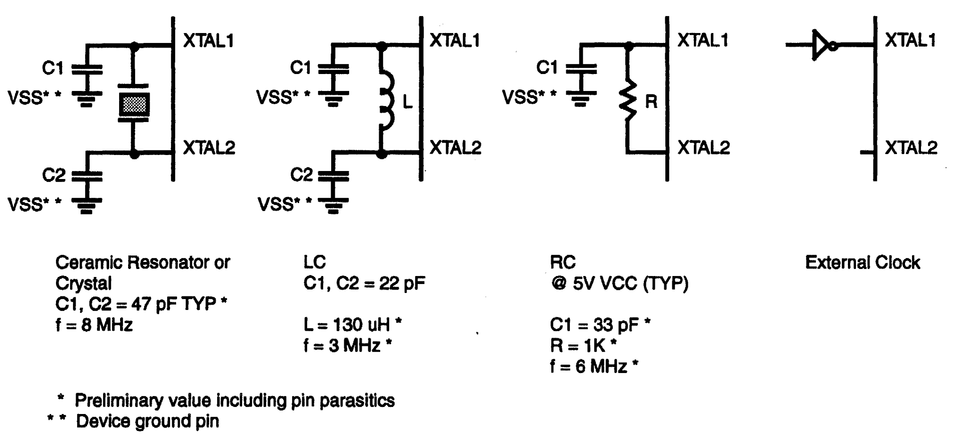


Figure 16. Oscillator Configuration

Power-On-Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status.
2. STOP-Mode Recovery (if D5 of SMR=1).
3. WDT timeout.

The POR time is a specified as T_{POR}. Bit 5 of the STOP-Mode Register determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be enabled and executed to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
           or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation. It also reduces the standby current to 10 µA or less. The STOP mode is terminated by a reset only, either by WDT timeout, POR, SMR recovery, or external reset. This causes the processor to restart the application program at address 000C (HEX).

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2, and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 17).

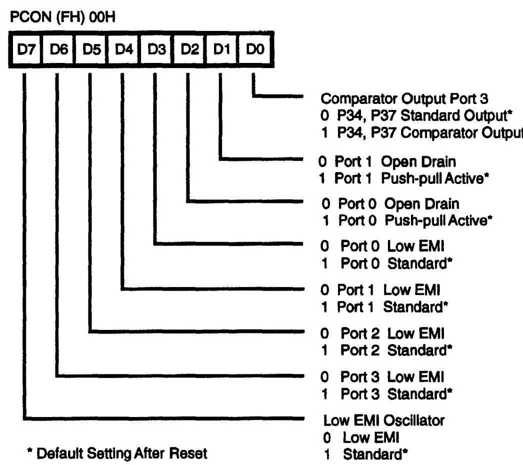


Figure 17. Port Configuration Register (PCON) (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1.

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low noise drive. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1. **Note:** Maximum external clock frequency of 4 MHz when running in the low EMI oscillator mode.

Low EMI Emission. The Z86C40 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP-Mode Recovery (Figure 18). All bits are Write Only, except bit 7 which is Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the STOP-Mode Recovery signal. Bits 0 and 1 determine the timeout period of the WDT. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

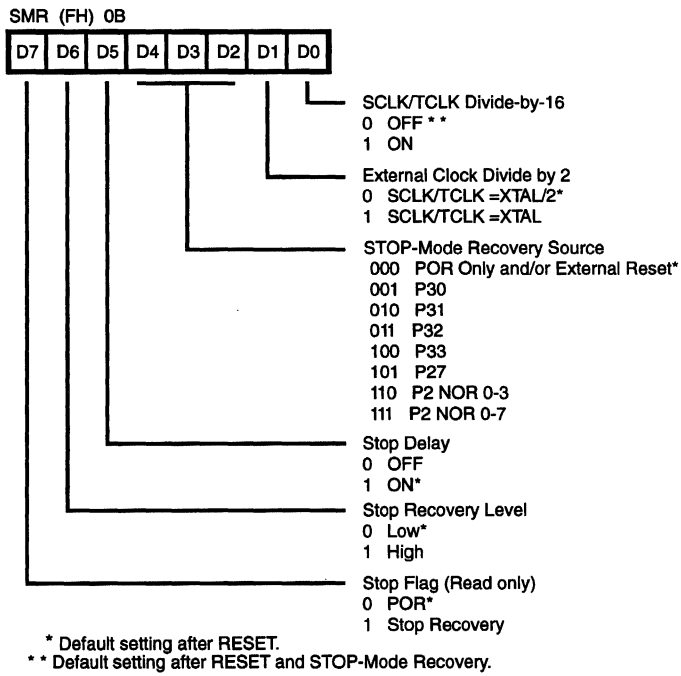


Figure 18. STOP-Mode Recovery Register (Write Only Except Bit D7, Which Is Read Only)

FUNCTIONAL DESCRIPTION (Continued)

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery.

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero. Maximum external clock frequency is 4 MHz when SMR Bit D1 = 1 where SCLK/TCLK = XTAL.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 19 and Table 7).

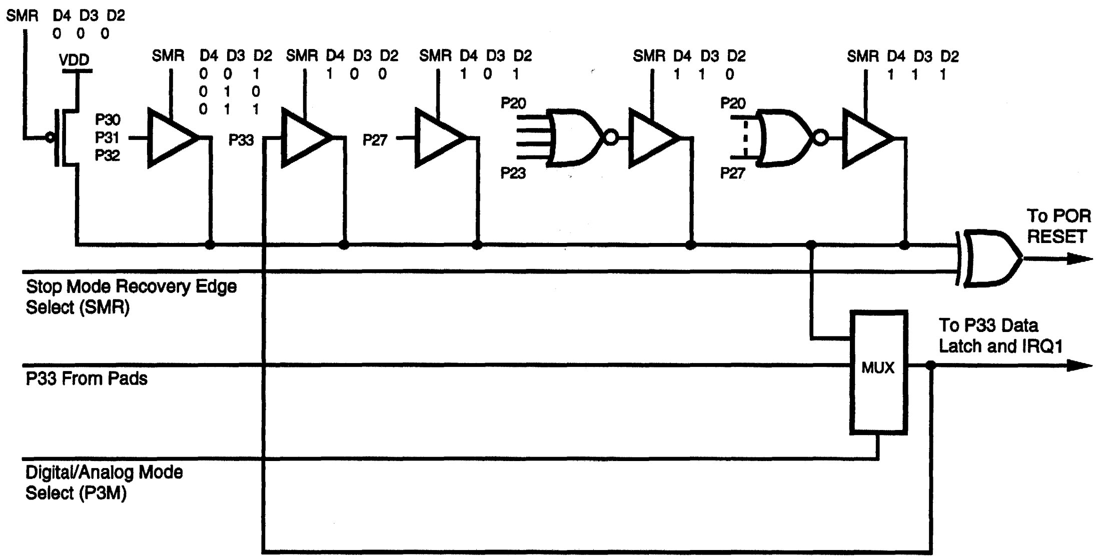


Figure 19. STOP-Mode Recovery Source

Table 7. STOP-Mode Recovery Source

SMR:432 D4	D3	D2	Operation Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition (not in Analog Mode)
0	1	1	P32 transition (not in Analog Mode)
1	0	0	P33 transition (not in Analog Mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

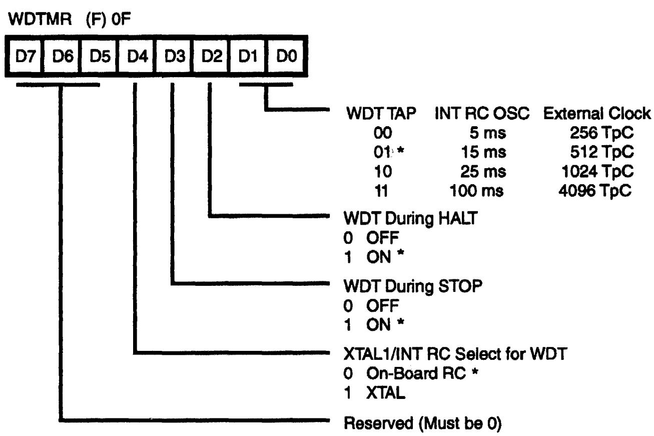
STOP-Mode Recovery Delay Select (D5). This bit, if High, enables the T_{POR} /RESET delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop-Mode Recovery source is kept active for at least 5 TpC.

STOP-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z86C40 from STOP mode. A 0 indicates low-level recovery. The default is 0 on POR (Figure 19).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device resets by POR/WDT RESET. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 20).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.



* Default setting after RESET

Figure 20. Watch-Dog Timer Mode Register (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

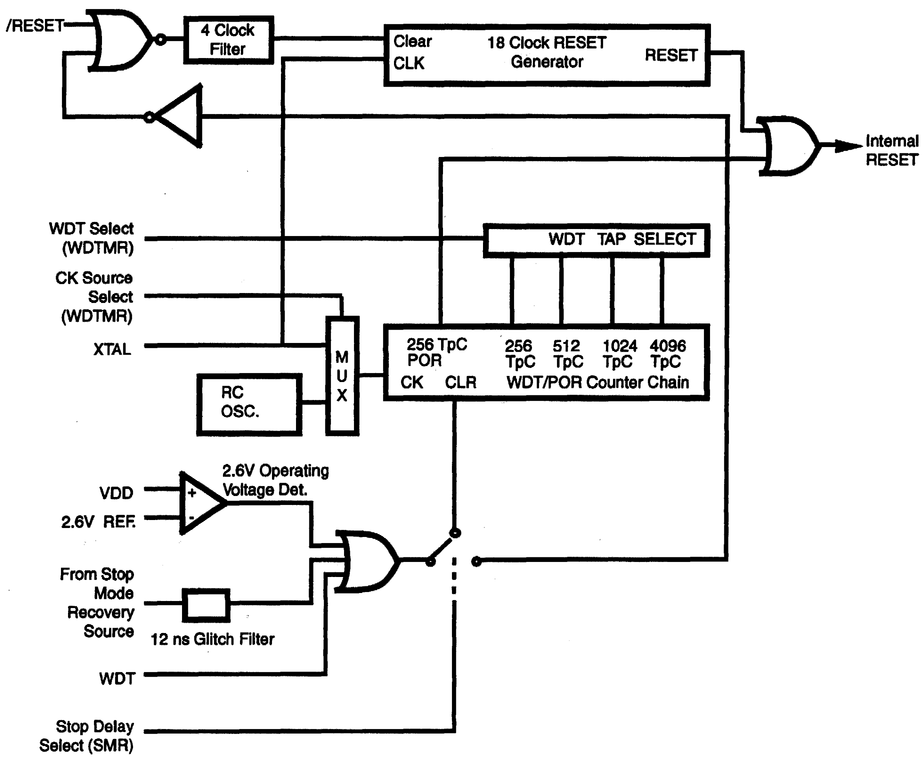


Figure 21. Resets and WDT

WDT Time Select. (D0,D1). Selects the WDT time period and is configured as shown in Table 8.

Table 8. WDT Time Select

D1	D0	Timeout of Internal RC OSC	Timeout of XTAL Clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 15 ms.
Values given are for V_{CC} = 5.0V.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP mode, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0 which selects the Internal RC oscillator.

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 64 internal system clock cycles from the execution of the first instruction after Power-On Reset, watch dog reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH (Figure 20).

Note: The WDT can be permanently enabled through a mask programming option. The option is selected by the customer at the time of ROM code submittal. In this mode, WDT is always activated when the device comes out of reset. Execution of the WDT instruction serves to refresh the WDT time-out period. WDT operation in the HALT and STOP modes is controlled by WDTMR programming. If this mask option is not selected at the time of ROM code submission, the WDT must be activated by the user through the WDT instruction and is always disabled by any reset to the device.

FUNCTIONAL DESCRIPTION (Continued)

Low Voltage Protection. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the specified voltage (Low Voltage Protection voltage). The minimum operating voltage is varying with the temperature and operating frequency, while the Low Voltage Protection voltage (V_{LV}) varies with temperature only.

The Low Voltage Protection trip voltage (V_{LV}) is less than 3V and above 1.4V under the following conditions.

Maximum (V_{LV}) Conditions:

Case 1: T_A = –40°C, +105°C, Internal Clock Frequency equal or less than 1 MHz

Case 2: T_A = –40°C, +85°C, Internal Clock Frequency equal or less than 2 MHz

Note: The internal clock frequency is one-half the external clock frequency (SMR D1 = 0).

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low Voltage Protection trip point (V_{LV}) is reached, for the temperatures and operating frequencies in Case 1 and Case 2, above. The device is guaranteed to function normally at supply voltages above the Low Voltage Protection trip point. The actual Low Voltage Protection trip point is a function of temperature and process parameters (Figure 22).

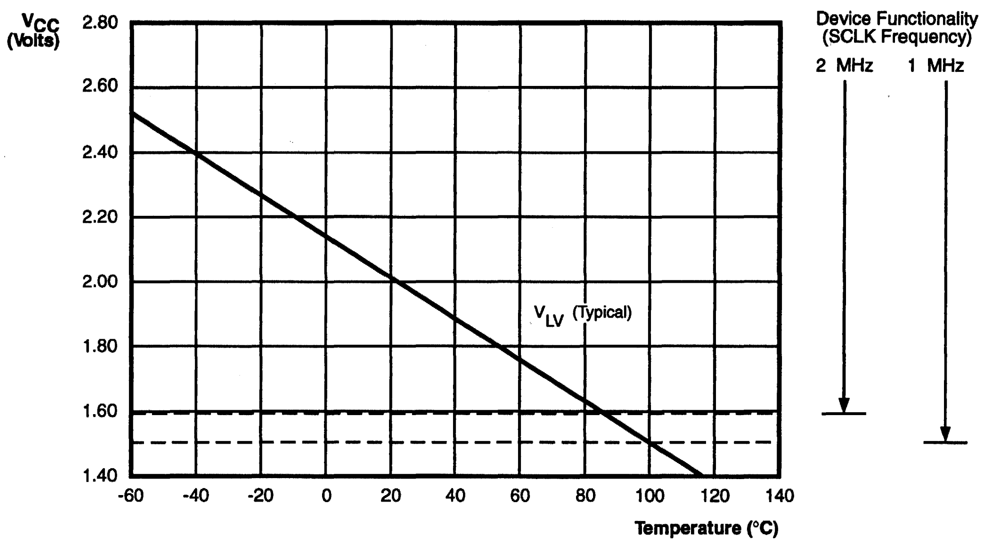


Figure 22. Typical Z86C40 Low Voltage Protection Voltage vs Temperature

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on XTAL1 and /RESET Pins with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		770	mW
Maximum Current out of V_{SS}		140	mA
Maximum Current into V_{DD}		125	mA
Maximum Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Output Current Sinked by Any I/O Pin		25	mA
Maximum Output Current Sourced by Any I/O Pin		25	mA

Notes:
[1] This applies to all pins except XTAL pins and where otherwise noted.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes XTAL pins.
[4] Device pin is not at an output Low state.

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 770 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [\, I_{DD} - (\text{sum of } I_{OH})\,] + \text{sum of } [\, (V_{DD} - V_{OH}) \times I_{OH}\,] + \text{sum of } (V_{OL} \times I_{OL})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 23).

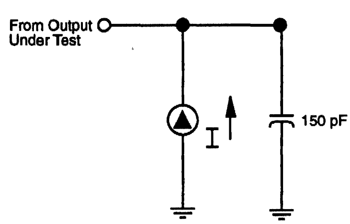


Figure 23. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	T_A = 0° C to +70°C Max	T_A = -40°C to +105°C Min	T_A = -40°C to +105°C Max	Typical [13] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Output High Voltage	3.0V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA	[8]
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	[8]
V_{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	[8]
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	[8]
V_{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I_{OL} = +6 mA	[8]
		5.5V		1.2		1.2	0.3	V	I_{OL} = +12 mA	[8]
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.5	V		
		5.5V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		[10]
		5.5V		25		25	10	mV		[10]
I_{IL}	Input Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V		-130		-130	-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	[4,5]
		5.5V		25		25	12	mA	@ 16 MHz	[4,5]
		3.0V		15		15	5	mA	@ 12 MHz	[4,5]
		5.5V		20		20	15	mA	@ 12 MHz	[4,5]
I_{CC1}	Standby Current	3.0V		4.5		4.5	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 16 MHz	[4,5]
		5.5V		8		8	3.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 16 MHz	[4,5]
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	[4,5]
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	[4,5]
I_{CC2}	Standby Current	3.0V		8		15	1	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6,11]
		5.5V		10		20	2	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6,11]
		3.0V		500		600	310	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6,11,14]
		5.5V		800		1000	600	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6,11,14]

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	T_A = 0° C to +70°C Max	T_A = -40°C to +105°C Min	T_A = -40°C to +105°C Max	Typical [13] @ 25°C	Units	Conditions	Notes
V_{ICR}	Input Common Mode Voltage Range	3.0	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		[10]
		5.5	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		[10]
I_{ALL}	Auto Latch Low Current	3.0V		8		10	5	µA	$0V < V_{IN} < V_{CC}$	[9]
		5.5V		15		20	11	µA	$0V < V_{IN} < V_{CC}$	[9]
I_{ALH}	Auto Latch High Current	3.0V		-5		-7	-3	µA	$0V < V_{IN} < V_{CC}$	[9]
		5.5V		-8		-10	-6	µA	$0V < V_{IN} < V_{CC}$	[9]
T_{POR}	Power On Reset	3.0V	7	24	7	25	8.5	mS		
		5.5V	3	13	3	14	5.0	mS		
V_{LV}	V_{CC} Low Voltage Protection Voltage		1.7	2.95	1.7	3.3	2.6	V	2 MHz max Int. CLK Freq.	[7]
V_{OH}	Output High Voltage (Low EMI Mode)	3.3V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -0.5mA	
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -0.5mA	
V_{OL}	Output Low Voltage (Low EMI Mode)	3.3V		0.6		0.6	0.2	V	I_{OL} = 1.0mA	
		5.0V		0.4		0.4	0.1	V	I_{OL} = 1.0mA	

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock-Driven	0.3 mA	5	mA	8 MHz
Resonator or Crystal	3.0 mA	5	mA	8 MHz

[2] GND = 0V.
[3] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] The V_{LV} increases as the temperature decreases.
[8] Standard Mode (not Low EMI).
[9] Auto Latch (Mask Option) selected.
[10] For analog comparator, inputs when analog comparators are enabled.
[11] Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
[12] Excludes clock pins.
[13] Typicals are at V_{CC} = 5.0V and 3.3V.
[14] Internal RC selected.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

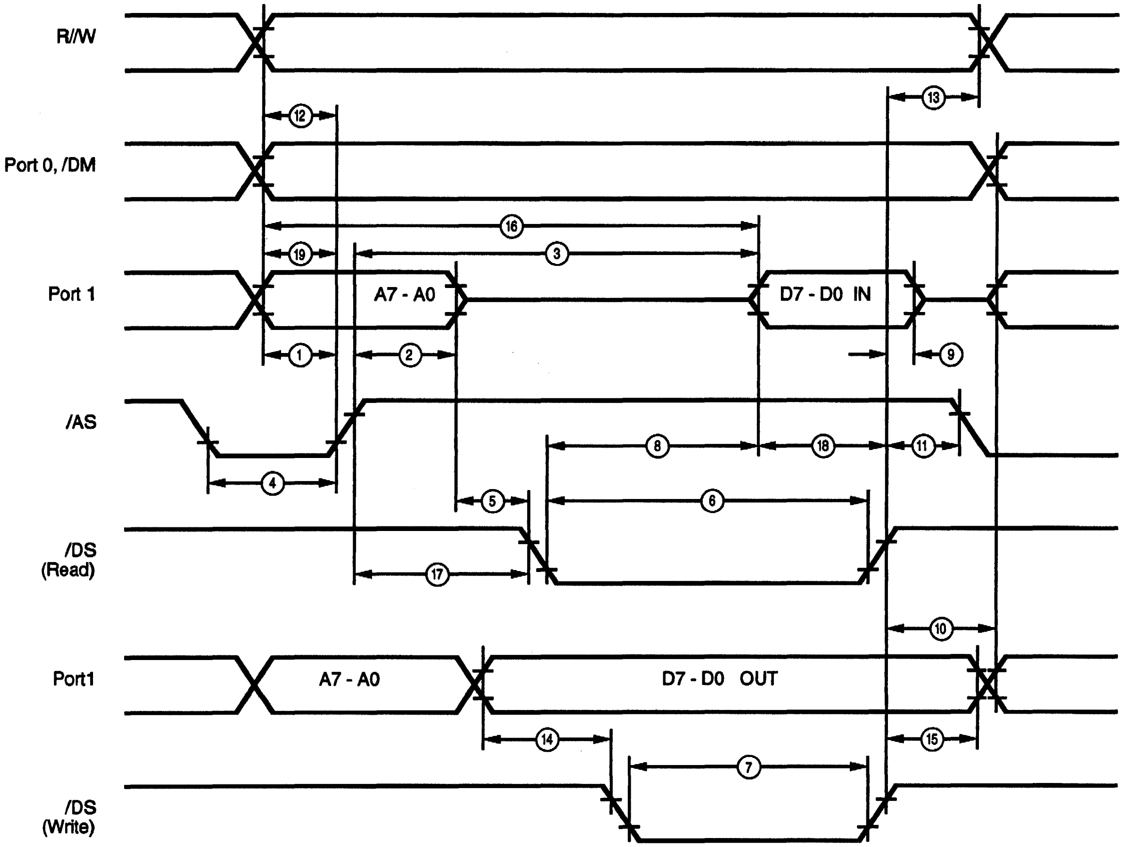


Figure 24. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table
(SCLK/TCLK = XTAL/2)

			Note [3]	T_A = 0°C to +70°C 12 MHz		16 MHz		T_A = –40°C to +105°C 12 MHz		16 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	3.0	35		25		35		25		ns	[2]
			5.5	35		25		35		25			
2	TdAS(A)	/AS Rise to Address Float Delay	3.0	45		35		45		35		ns	[2]
			5.5	45		35		45		35		ns	
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	3.0		250		180		250		180	ns	[1,2]
			5.5		250		180		250		180	ns	
4	TwAS	/AS Low Width	3.0	55		40		55		40		ns	[2]
			5.5	55		40		55		40		ns	
5	Td	Address Float to /DS Fall	3.0	0		0		0		0		ns	
			5.5	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	3.0	200		135		200		135		ns	[1,2]
			5.5	200		135		200		135		ns	
7	TwDSW	/DS (Write) Low Width	3.0	110		80		110		80		ns	[1,2]
			5.5	110		80		110		80		ns	
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	3.0		150		75		150		75	ns	[1,2]
			5.5		150		75		150		75	ns	
9	ThDR(DS)	Read Data to /DS Rise Hold Time	3.0	0		0		0		0		ns	[2]
			5.5	0		0		0		0		ns	
10	TdDS(A)	/DS Rise to Address Active Delay	3.0	45		50		45		50		ns	[2]
			5.5	55		50		55		50		ns	
11	TdDS(AS)	/DS Rise to /AS Fall Delay	3.0	30		35		30		35		ns	[2]
			5.5	45		35		45		55		ns	
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	3.0	45		25		45		25		ns	[2]
			5.5	45		25		45		25		ns	
13	TdDS(R/W)	/DS Rise to R//W Not Valid	3.0	45		35		45		35		ns	[2]
			5.5	45		35		45		35		ns	
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	3.0	55		25		55		25		ns	[2]
			5.5	55		25		55		25		ns	
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	3.0	45		35		45		35		ns	[2]
			5.5	55		35		55		35		ns	
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.0		310		230		310		230	ns	[1,2]
			5.5		310		230		310		230	ns	
17	TdAS(DS)	/AS Rise to /DS Fall Delay	3.0	65		45		65		45		ns	[2]
			5.5	65		45		65		45		ns	
18	TdDI(DS)	Data Input Setup to /DS Rise	0.0	115		60		115		60		ns	[1,2]
			5.5	75		60		75		60		ns	
19	TdDM(AS)	/DM Valid to /AS Fall Delay	3.0	35		30		35		30		ns	[2]
			5.5	35		30		35		30		ns	

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.

Standard Test Load
All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

AC ELECTRICAL CHARACTERISTICS
Additional Timing Diagram

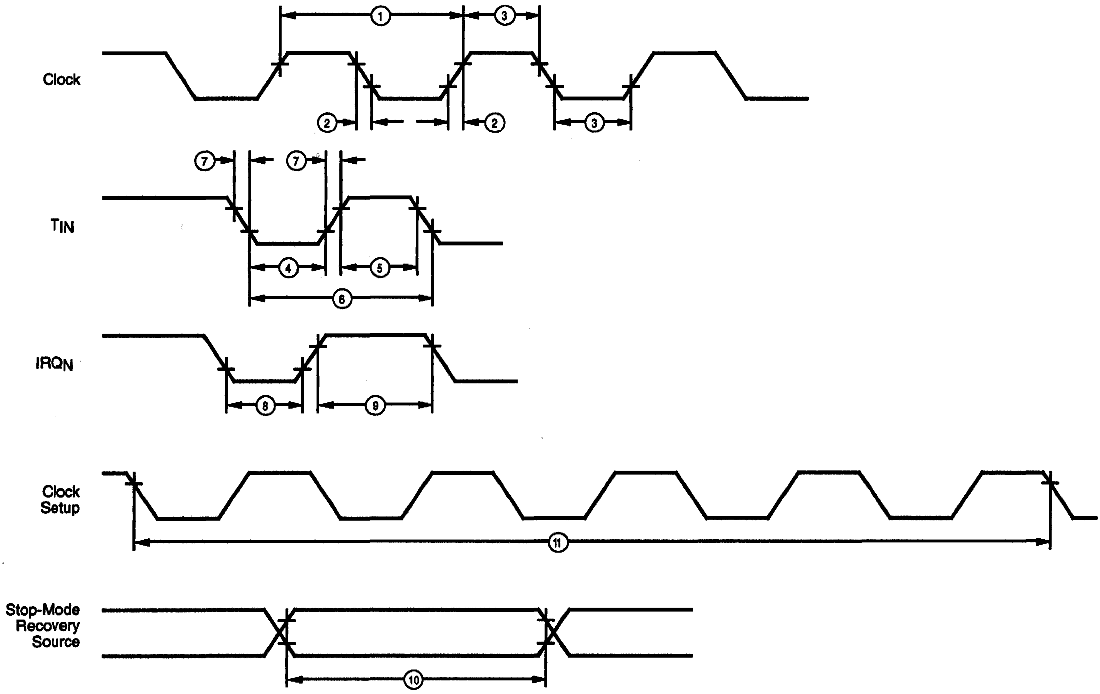


Figure 25. Additional Timing

AC ELECTRICAL CHARACTERISTICS
Additional Timing Table (SCLK/TCLK = XTAL/2)

				T_A = 0°C to +70°C				T_A = –40°C to +105°C					
			V_{CC}	12 MHz		16 MHz		12 MHz		16 MHz			
No	Symbol	Parameter	Note[6]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	[1]
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	[1]
			5.5V		15		15		15		15	ns	[1]
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	[1]
			5.5V	41		31		41		31		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1]
			5.5V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			[1]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			[1]
			5.5V	8TpC		8TpC		8TpC		8TpC			[1]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	[1]
			5.5V		100		100		100		100	ns	[1]
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	[1,2]
			5.5V	70		70		70		70		ns	[1,2]
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1,3]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,3]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1,2]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,2]
10	Twsm	STOP-Mode Recovery Width Spec	3.0V	12		12		12		12		ns	
			5.5V	12		12		12		12		ns	
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		5TpC		5TpC		[4]
			5.5V		5TpC		5TpC		5TpC		5TpC		[4]
12	Twdt	Watch-Dog Timer Delay Time	3.0V	10		10		10		10		ms	D0 = 0 [5]
			5.5V	5		5		5		5		ms	D1 = 0 [5]
			3.0V	30		30		30		30		ms	D0 = 1 [5]
			5.5V	15		15		15		15		ms	D1 = 0 [5]
			3.0V	50		50		50		50		ms	D0 = 0 [5]
			5.5V	25		25		25		25		ms	D1 = 1 [5]
			3.0V	200		200		200		200		ms	D0 = 1 [5]
			5.5V	100		100		100		100		ms	D1 = 1 [5]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 0.
[5] Reg. WDTMR.
[6] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.

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AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = XTAL)

No	Symbol	Parameter	V_{cc} Note [6]	T_A = 0°C to +70°C 4 MHz Min	Max	T_A = –40°C to +105°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	[1,7,8]
			5.5V	250	DC	250	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	[1,7,8]
			5.5V		25		25	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	125		125		ns	[1,7,8]
			5.5V	125		125		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			[1,7,8]
			5.5V	3TpC		3TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1,7,8]
			5.5V	4TpC		4TpC			[1,7,8]
7	TrTin,	Timer Input Rise & Fall Timer	3.0V		100		100	ns	[1,7,8]
	TfTin		5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC			[1,3,7,8]
			5.5V	3TpC		3TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			[1,2,7,8]
			5.5V	3TpC		2TpC			[1,2,7,8]
10	Twsm	STOP-Mode Recovery Width Spec	3.0V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		[4,8,9]
			5.5V		5TpC		5TpC		[4,8,9]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P33-P31).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 1, POR STOP mode delay is on.
[5] Reg. WDTMR.
[6] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.5V ±0.5V.
[7] SMR D1 = 0.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Diagrams

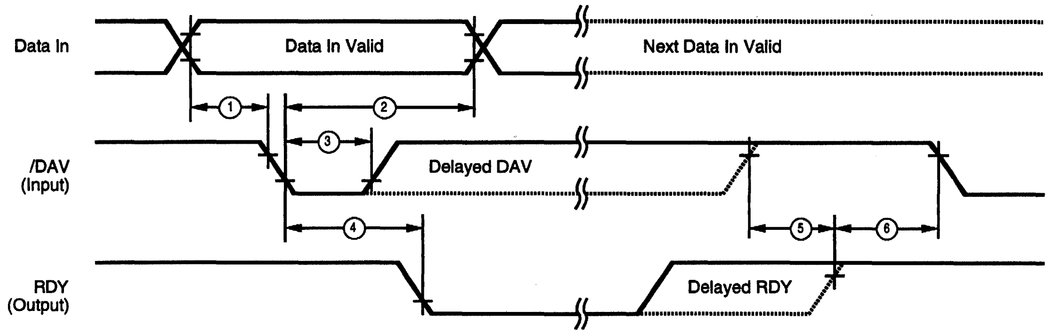

Figure 26. Input Handshake Timing

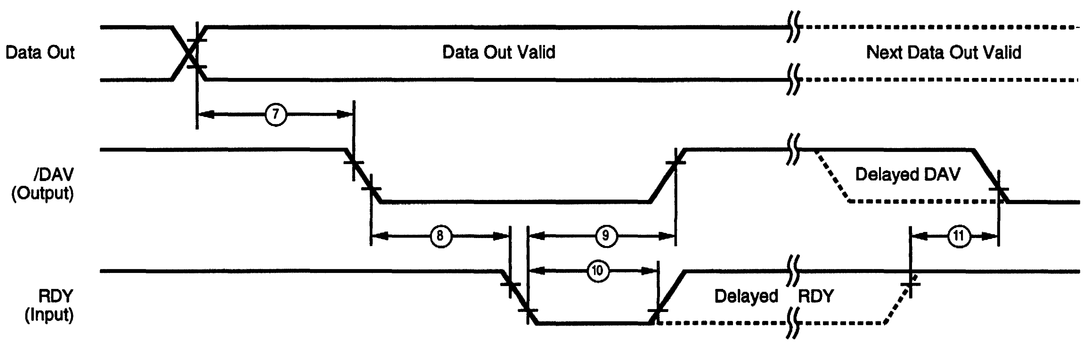

Figure 27. Output Handshake Timing

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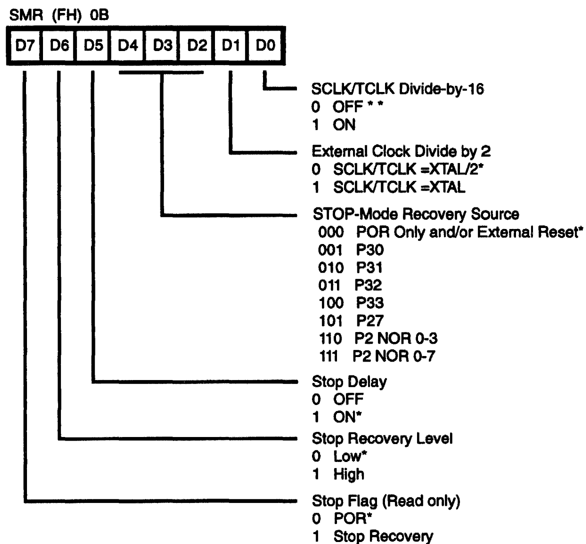
AC ELECTRICAL CHARACTERISTICS
Handshake Timing Table

				T_A = 0°C to +70°C				T_A = –40°C to +105°C				
			V_{CC}	12 MHz		16 MHz		12 MHz		16 MHz		Data
No	Symbol	Parameter	Note[1,2]	Min	Max	Min	Max	Min	Max	Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
2	ThDI(DAV)	Data In Hold Time	3.0V	160		160		160		160		IN
			5.5V	115		115		115		115		IN
3	TwDAV	Data Available Width	3.0V	155		155		155		155		IN
			5.5V	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	3.0V		160		160		160		160	IN
			5.5V		115		115		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	3.0V		120		120		120		120	IN
			5.5V		80		80		80		80	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay	3.0V	42		31		42		31		OUT
			5.5V	42		31		42		31		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	3.0V	0		0		0		0		OUT
			5.5V	0		0		0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	3.0V		160		160		160		160	OUT
			5.5V		115		115		115		115	OUT
10	TwRDY	RDY Width	3.0V	110		110		110		110		OUT
			5.5V	80		80		80		80		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V		110		110		110		110	OUT
			5.5V		80		80		80		80	OUT

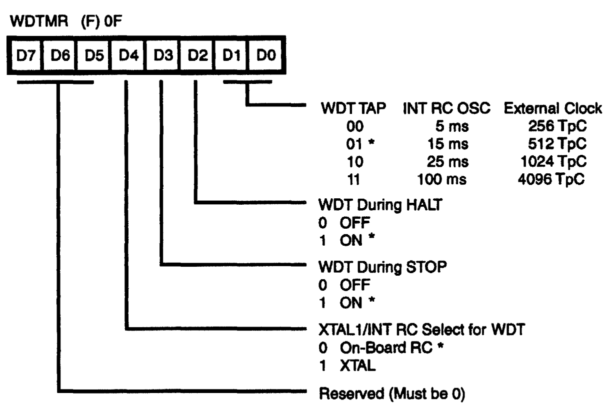
Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.

EXPANDED REGISTER FILE CONTROL REGISTERS



* Default setting after RESET.
* * Default setting after RESET and STOP-Mode Recovery.

Figure 28. Stop-Mode Recovery Register (Write Only Except Bit D7, Which Is Read Only)



* Default setting after RESET

Figure 29. Watch-Dog Timer Mode Register (Write Only)

Z8® CONTROL REGISTERS

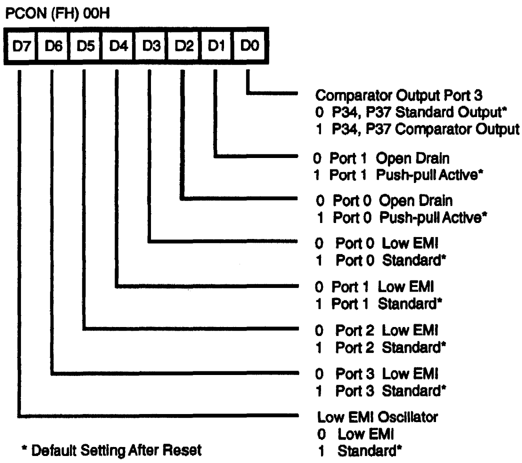


Figure 30. Port Configuration Register (PCON) (Write Only)

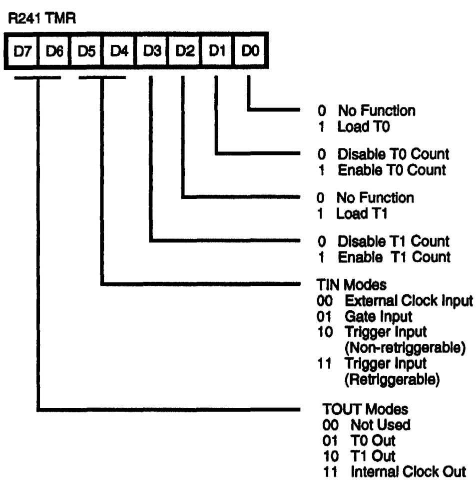


Figure 31. Timer Mode Register ($F1_H$: Read/Write)

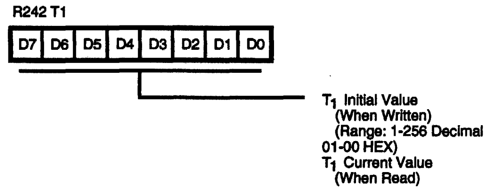


Figure 32. Counter/Timer 1 Register ($F2_H$: Read/Write)

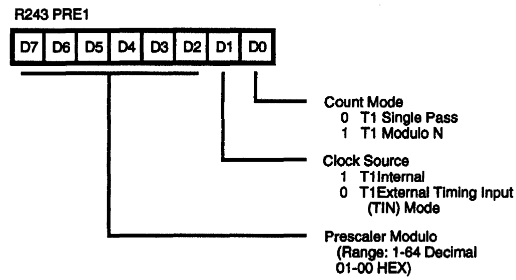


Figure 33. Prescaler 1 Register ($F3_H$: Write Only)

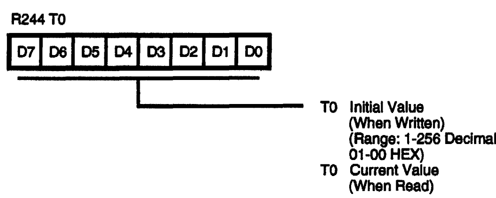


Figure 34. Counter/Timer 0 Register ($F4_H$: Read/Write)

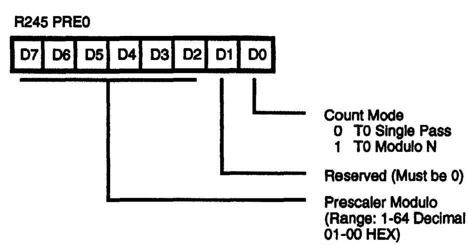


Figure 35. Prescaler 0 Register ($F5_H$: Write Only)

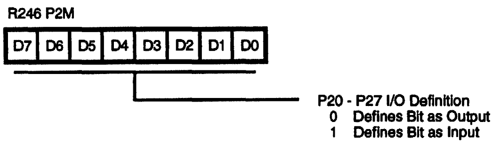


Figure 36. Port 2 Mode Register ($F6_H$: Write Only)

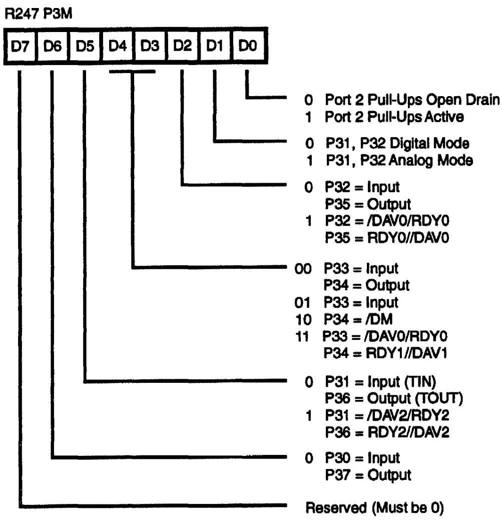


Figure 37. Port 3 Mode Register ($F7_H$: Write Only)

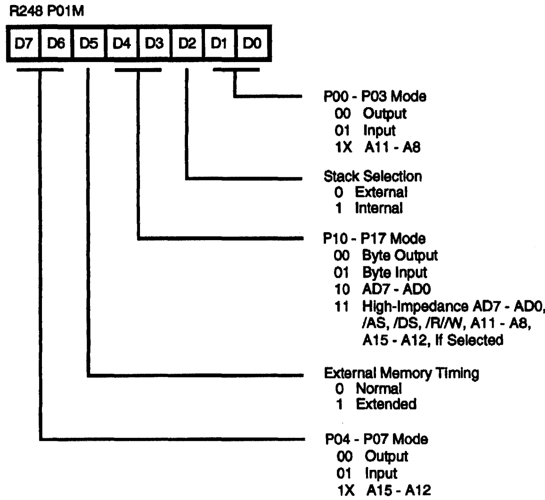


Figure 38. Port 0 and 1 Mode Register ($F8_H$: Write Only)

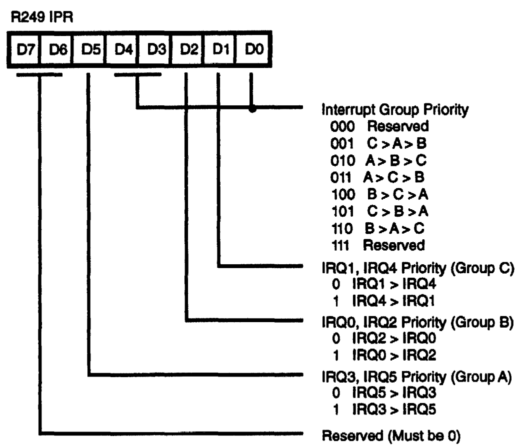


Figure 39. Interrupt Priority Register ($F9_H$: Write Only)

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Z8 CONTROL REGISTERS (Continued)

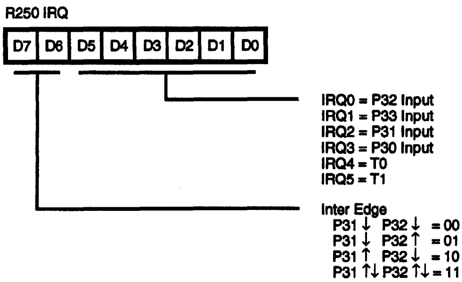
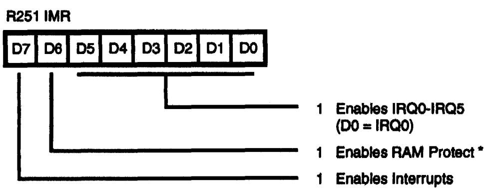


Figure 40. Interrupt Request Register (FA_H: Read/Write)



* This option must be selected when ROM code is submitted for ROM Masking, otherwise this control bit is disabled permanently.

Figure 41. Interrupt Mask Register (FB_H: Read/Write)

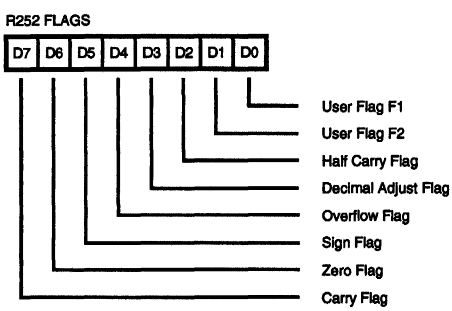


Figure 42. Flag Register (FC_H: Read/Write)

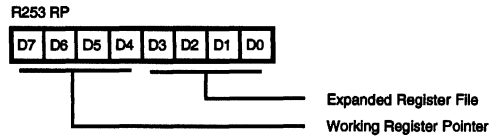


Figure 43. Register Pointer (FD_H: Read/Write)

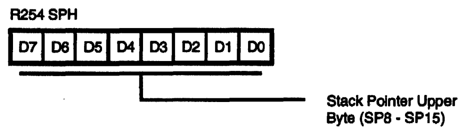


Figure 44. Stack Pointer High (FE_H: Read/Write)

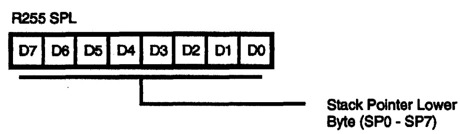


Figure 45. Stack Pointer Low (FF_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

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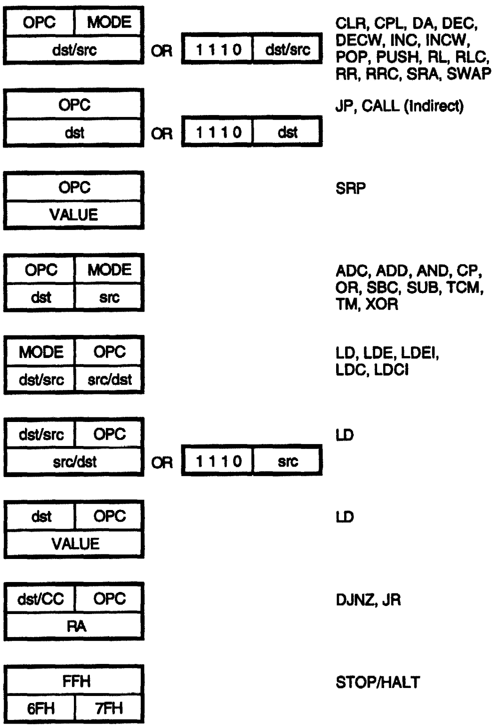
CONDITION CODES

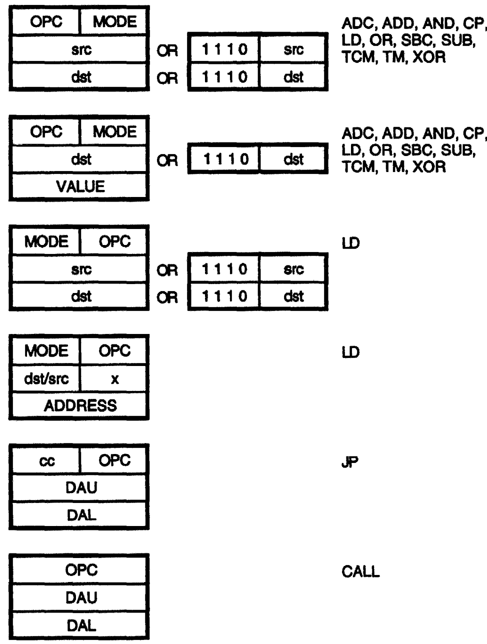
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

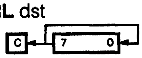
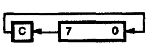
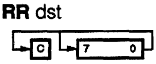
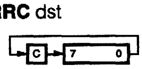
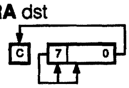
dst (7)

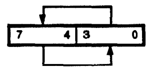
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src	†		1[ ]	* * * * 0 *
dst←dst + src + C				
ADD dst, src	†		0[ ]	* * * * 0 *
dst←dst + src				
AND dst, src	†		5[ ]	- * * 0 - -
dst←dst AND src				
CALL dst	DA		D6	- - - - - - -
SP←SP - 2	IRR		D4	
@SP←PC,				
PC←dst				
CCF			EF	* - - - - -
C←NOT C				
CLR dst	R		B0	- - - - - - -
dst←0	IR		B1	
COM dst	R		60	- * * 0 - -
dst←NOT dst	IR		61	
CP dst, src	†		A[ ]	* * * * - -
dst - src				
DA dst	R		40	* * * X - -
dst←DA dst	IR		41	
DEC dst	R		00	- * * * - -
dst←dst - 1	IR		01	
DECW dst	RR		80	- * * * - -
dst←dst - 1	IR		81	
DI			8F	- - - - - - -
IMR(7)←0				
DJNZr, dst	RA		rA	- - - - - - -
r←r - 1			r = 0 - F	
if r ≠ 0				
PC←PC + dst				
Range: +127, -128				
EI			9F	- - - - - - -
IMR(7)←1				
HALT			7F	- - - - - - -

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
INC dst	r		rE	- * * * - -
dst←dst + 1			r = 0 - F	
	R		20	
	IR		21	
INCW dst	RR		A0	- * * * - -
dst←dst + 1	IR		A1	
IRET			BF	* * * * * *
FLAGS←@SP;				
SP←SP + 1				
PC←@SP;				
SP←SP + 2;				
IMR(7)←1				
JP cc, dst	DA		cD	- - - - - -
if cc is true			c = 0 - F	
PC←dst	IRR		30	
JR cc, dst	RA		cB	- - - - - -
if cc is true,			c = 0 - F	
PC←PC + dst				
Range: +127, -128				
LD dst, src	r	Im	rC	- - - - - -
dst←src	r	R	r8	
	R	r	r9	
			r = 0 - F	
	r	X	C7	
	X	r	D7	
	r	Ir	E3	
	Ir	r	F3	
	R	R	E4	
	R	IR	E5	
	R	IM	E6	
	IR	IM	E7	
	IR	R	F5	
LDC dst, src	r	Irr	C2	- - - - - -
LDCI dst, src	Ir	Irr	C3	- - - - - -
dst←src				
r←r +1;				
rr←rr + 1				

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst–src–C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst–src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

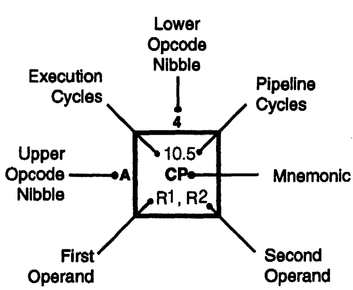
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) / Upper Nibble (Hex)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2					↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1					↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** Irr1, r2	18.0 **LDCI** Irr1, Ir2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 o **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



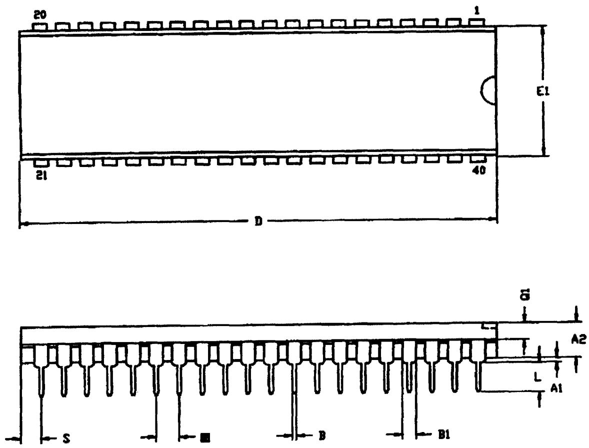
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

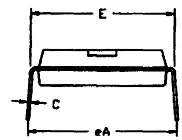
Sequence:
Opcode, First Operand,
Second Operand

Note: Blanks are reserved.

*2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION

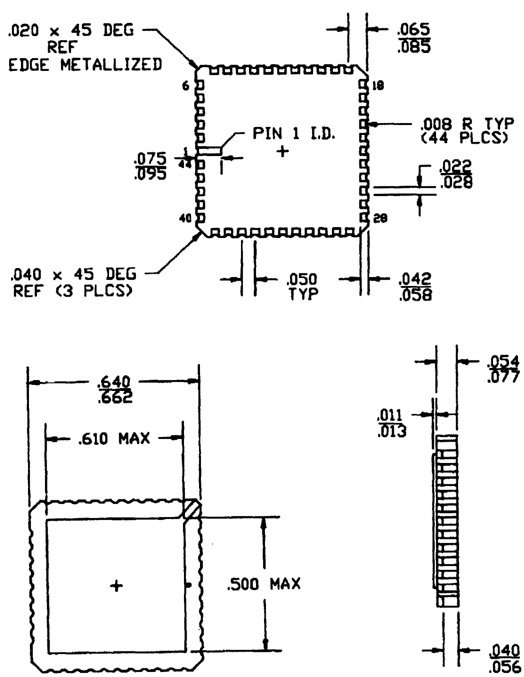




SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
■	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

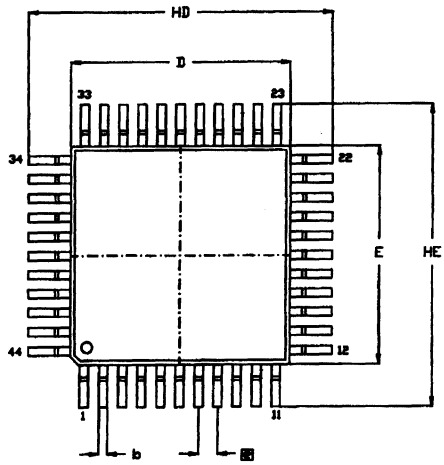
CONTROLLING DIMENSIONS : INCH

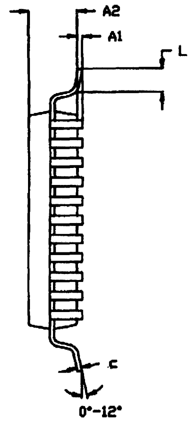
40-Pin DIP Package Diagram



44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)





NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm / .004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
▩	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86C40 (12 MHz)

Standard Temperature			Extended Temperature		
40-Pin DIP	**40-Pin PLCC**	**44-Pin QFP**	**40-Pin DIP**	**40-Pin PLCC**	**44-Pin QFP**
Z86C4012PSC	Z86C4012VSC	Z86C4012FSC	Z86C4012PEC	Z86C4012VEC	Z86C4012FEC

Z86C40 (16 MHz)

Standard Temperature			Extended Temperature		
40-Pin DIP	**40-Pin PLCC**	**44-Pin QFP**	**40-Pin DIP**	**40-Pin PLCC**	**44-Pin QFP**
Z86C4016PSC	Z86C4016VSC	Z86C4016FSC	Z86C4016PEC	Z86C4016VEC	Z86C4016FEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Preferred Package
P = Plastic DIP
V = Plastic Chip Carrier

Longer Lead Time
F = Plastic Quad Flat Pack

Preferred Temperature
S = 0°C to +70°C

Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
16 = 16 MHz

Environmental
C = Plastic Standard

Example:

Z 86C40 16 P S C is a Z86C40, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 16 — Speed
- 86C40 — Product Number
- Z — Zilog Prefix

Z86E30/E31 CMOS Z8® OTP CCP™
Consumer Controller Processor
8

Z86C40 CMOS Z8® 4K ROM CCP™
Consumer Controller Processor
9

Z86E40 CMOS Z8® 8-Bit OTP CCP™
Consumer Controller Processor
10

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and Third Party Vendors
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Z86E40

CMOS Z8® 8-BIT OTP CCP™ CONSUMER CONTROLLER PROCESSOR

FEATURES

- Low Cost, 8-Bit CMOS OTP Microcontroller, with 4 Kbytes of One-Time PROM and 236 Bytes of RAM
- Package Styles: 40-Pin DIP, 44-Pin PLCC, 44-Pin QFP, 40-Pin Cerdip Window Lid
- 4.5V to 5.5V Operating Range
- Clock Speeds up to 12 MHz
- Software Programmable Low EMI Mode.
- Software Enabled Watch-Dog Timer
- Pull-Up Active/Open-Drain Programmable on Port 0, Port 1 and Port 2
- Programmable RC Oscillator, EPROM Protect, and RAM Protect
- Low Power Consumption: 60 mW
- Fast Instruction Pointer: 0.6 µs
- Two Standby Modes: STOP and HALT
- 32 Input/Output Lines
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Three Expanded Register File Control Registers
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Auto Latches
- Auto Power-On Reset
- Two Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.

GENERAL DESCRIPTION

The Z86E40 OTP (One-Time-Programmable) CCP™ (Consumer Controller Processors) is a member of Zilog's Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/ EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 4 Kbytes of One-Time-PROM and 236 bytes of general-purpose RAM, this low cost, low power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/ output bit manipulation capabilities, and easy hardware/ software system expansion.

The Z86E40 architecture is characterized by Zilog's 8-bit microcontroller core with an expanded register file to allow easy access to register mapped peripheral and I/O circuits.

The Z86E40 has 32 pins dedicated to input and output for applications demanding powerful I/O capabilities. These lines are grouped into four ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake, and address/data bus for interfacing external memory.

GENERAL DESCRIPTION (Continued)

Four basic address spaces are available to support this wide range of configurations: Program Memory, Data Memory, Register File, and Expanded Register File (ERF). The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The Expanded Register File consists of three control resisters.

To unburden the system from coping with the real-time tasks such as counting/timing and input/output data communication, the Z86E40 offers two on-chip counter/timers with a large number of user selectable modes, and two on-board comparators to process analog signals with a common reference voltage (Figures 1 and 2).

Offered in a variety of package styles, such as 40-pin DIP, 44-pin PLCC, 44-pin QFP and 40-pin Cerdip Window Lid, the Z86E40 is well-suited for a wide range of applications.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

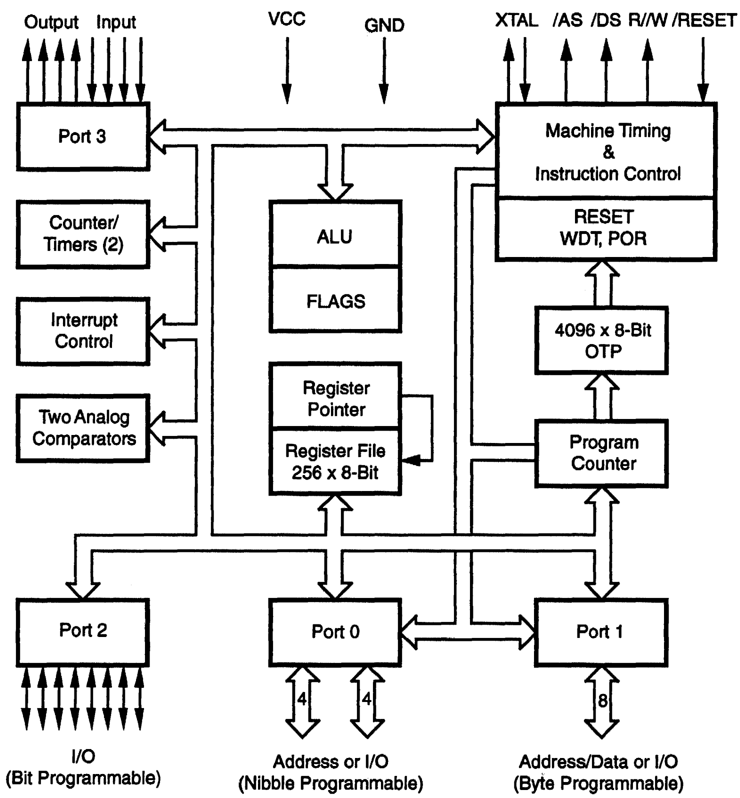

Figure 1. Z86E40 Functional Block Diagram

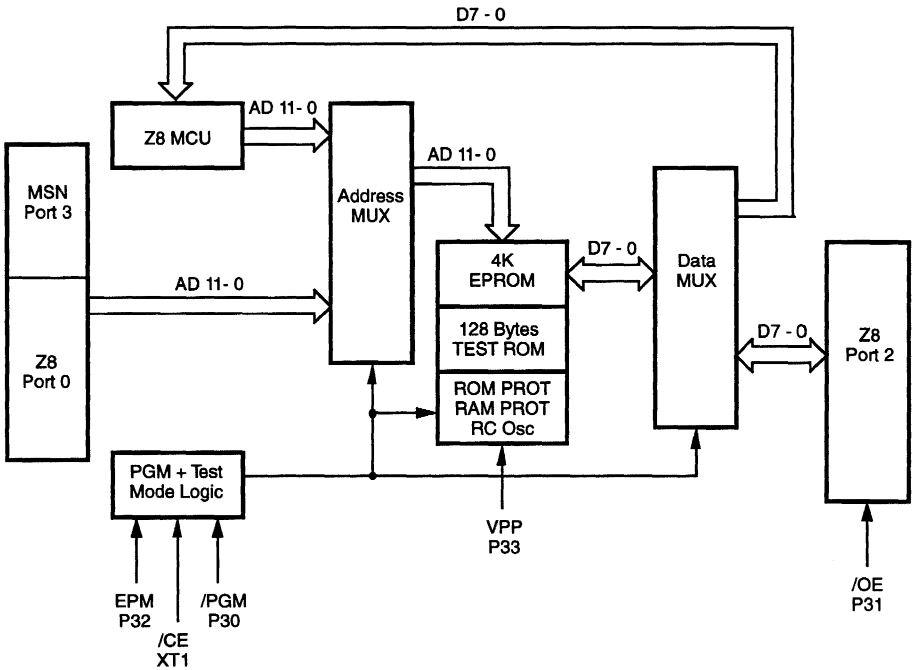

Figure 2. Z86E40 EPROM Programming Block Diagram

PIN IDENTIFICATION

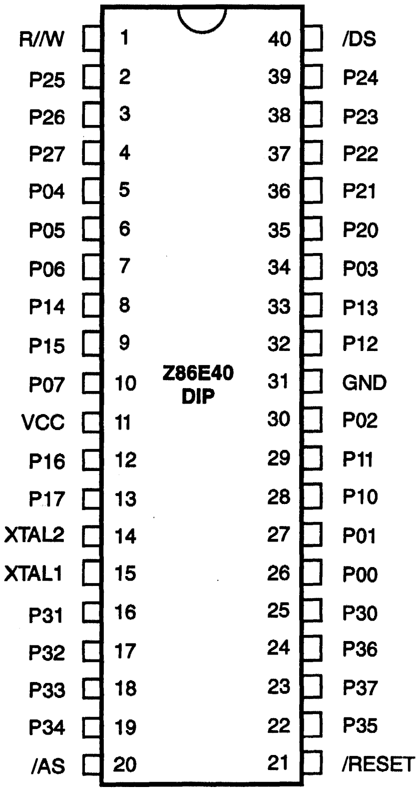

Figure 3. 40-Pin DIP Pin Configuration* (Standard Mode)

Table 1. 40-Pin DIP Pin Identification*

Standard Mode Pin #	Symbol	Function	Direction
1	R//W	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	In/Output
5-7	P04-P06	Port 0, Pins 4,5,6	In/Output
8-9	P14-P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	In/Output
28-29	P10-P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

Note:
* Pin Configuration and Identification identical on DIP and Cerdip Window Lid style packages.

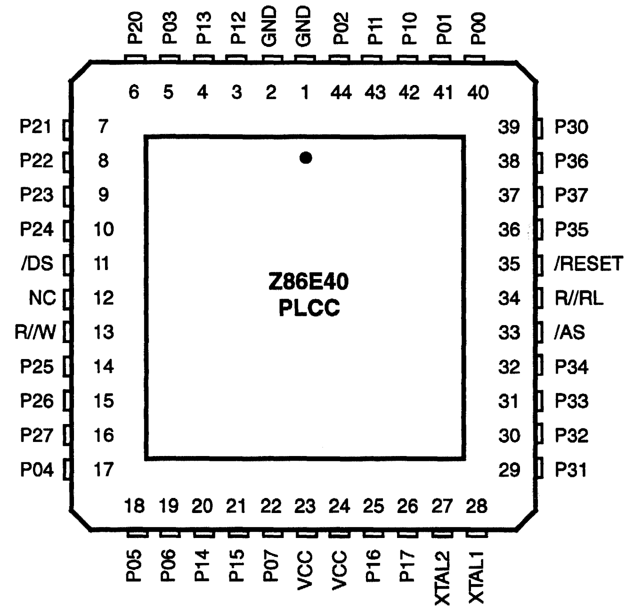

Figure 4. 44-Pin PLCC Pin Configuration (Standard Mode)

Table 2. 44-Pin PLCC Pin Identification

Standard Mode Pin #	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	NC	No Connection	
13	R/W	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	In/Output
17-19	P04-P06	Port 0, Pins 4,5,6	In/Output
20-21	P14-P05	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23-24	V_{CC}	Power Supply	
25-26	P16-P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29-31	P31-P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless select	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-P01	Port 0, Pins 0,1	In/Output
42-43	P10-P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN IDENTIFICATION (Continued)

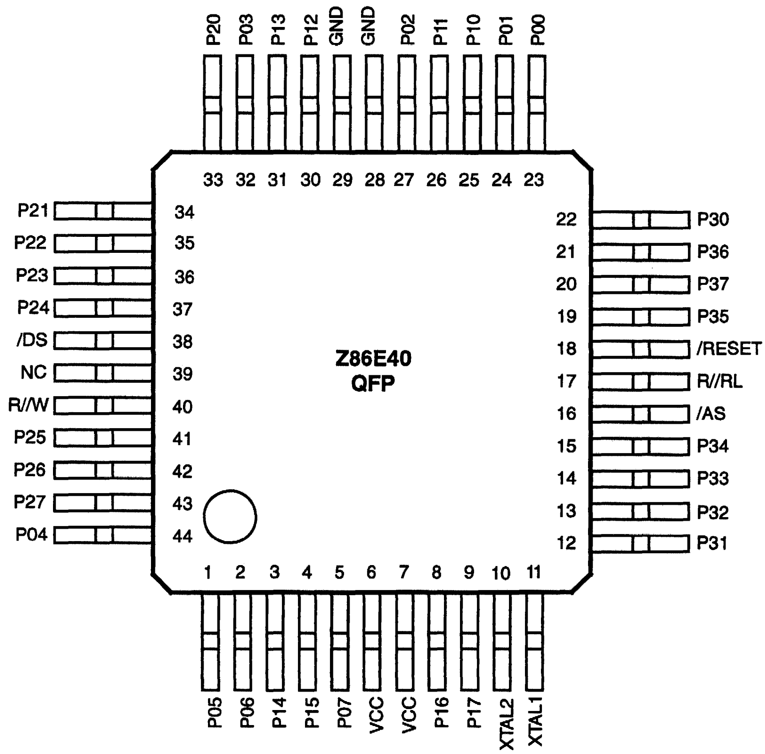

Figure 5. 44-Pin QFP Pin Configuration (Standard Mode)

Table 3. 44-Pin QFP Pin Identification

Standard Mode Pin #	Symbol	Function	Direction	Standard Mode Pin #	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	In/Output	21	P36	Port 3, Pin 6	Output
3-4	P14-P05	Port 1, Pins 4,5	In/Output	22	P30	Port 3, Pin 0	Input
5	P07	Port 0, Pin 7	In/Output	23-24	P00-P01	Port 0, Pin 0,1	In/Output
6-7	V_{CC}	Power Supply		25-26	P10-P11	Port 1, Pins 0,1	In/Output
8-9	P16-P17	Port 1, Pins 6,7	In/Output	27	P02	Port 0, Pin 2	In/Output
10	XTAL2	Crystal Oscillator	Output	28-29	GND	Ground	
11	XTAL1	Crystal Oscillator	Input	30-31	P12-P13	Port 1, Pins 2,3	In/Output
12-14	P31-P13	Port 3, Pins 1,2,3	Input	32	P03	Port 0, Pin 3	In/Output
15	P34	Port 3, Pin 4	Output	33-37	P20-4	Port 2, Pins 0,1,2,3,4	In/Output
16	/AS	Address Strobe	Output	38	/DS	Data Strobe	Output
17	R//RL	ROM/ROMless select	Input	39	NC	No Connection	
18	/RESET	Reset	Input	40	R/W	Read/Write	Output
19	P35	Port 3, Pin 5	Output	41-43	P25-P27	Port 2, Pins 5,6,7	In/Output
20	P37	Port 3, Pin 7	Output	44	P04	Port 0, Pin 4	In/Output

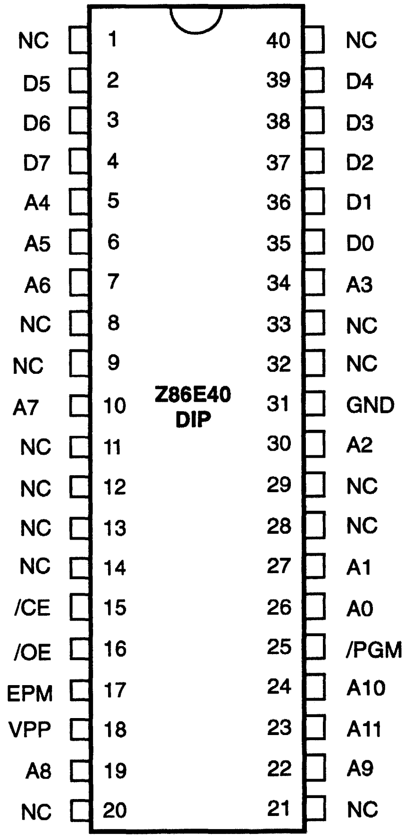

Figure 6. 40-Pin DIP Pin Configuration* (EPROM Mode)

Table 4. 40-Pin DIP Package Pin Identification*

EPROM Mode Pin #	Symbol	Function	Direction
1	NC	No Connection	
2-4	D5-D7	Data 5,6,7	In/Output
5-7	A4-A6	Address 4,5,6	Input
8-9	NC	No Connection	
10	A7	Address 7	Input
11	V_{CC}	Power Supply	
12-14	NC	No Connection	
15	/CE	Chip Select	Input
16	/OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19	A8	Address 8	Input
20-21	NC	No Connection	
22	A9	Address 9	Input
23	A11	Address 11	Input
24	A10	Address 10	Input
25	/PGM	Prog. Mode	Input
26-27	A0-A1	Address 0,1	Input
28-29	NC	No Connection	
30	A2	Address 2	Input
31	GND	Ground	
32-33	NC	No Connection	
34	A3	Address 3	Input
35-39	D0-D4	Data 0,1,2,3,4	In/Output
40	NC	No Connection	

Note:
* Pin Configuration and Description identical on DIP and Cerdin Window Lid style packages.

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PIN IDENTIFICATION (Continued)

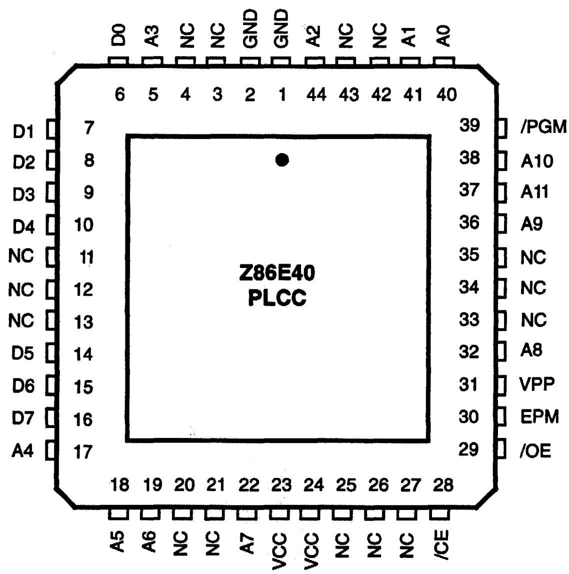


Figure 7. 44-Pin PLCC Pin Configuration (EPROM Programming Mode)

Table 5. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
EPROM Programming Mode				**EPROM Programming Mode**			
1-2	GND	Ground		29	/OE	Output Enable	Input
3-4	NC	No Connection		30	EPM	EPROM Prog. Mode	Input
5	A3	Address 3	Input	31	V_{PP}	Prog. Voltage	Input
6-10	D0-D4	Data 0,1,2,3,4	In/Output	32	A8	Address 8	Input
11-13	NC	No Connection		33-35	NC	No Connection	
14-16	D5-D7	Data 5,6,7	In/Output	36	A9	Address 9	Input
17-19	A4-A6	Address 4,5,6	Input	37	A11	Address 11	Input
20-21	NC	No Connection		38	A10	Address 10	Input
22	A7	Address 7	Input	39	/PGM	Prog. Mode	Input
23-24	V_{CC}	Power Supply		40-41	A0,A1	Address 0,1	Input
25-27	NC	No Connection		42-43	NC	No Connection	
28	/CE	Chip Select	Input	44	A2	Address 2	Input

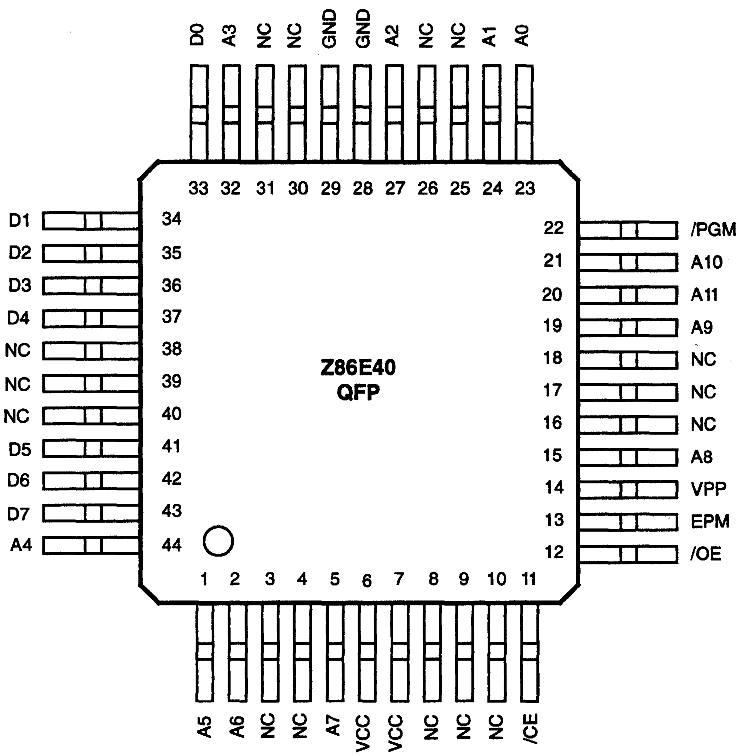


Figure 8. 44-Pin QFP Pin Configuration (EPROM Programming Mode)

Table 6. 44-pin QFP Pin Identification

EPROM Programming Mode				EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**	**Pin #**	**Symbol**	**Function**	**Direction**
1-2	A5-A6	Address 5,6	Input	21	A10	Address 10	Input
3-4	NC	No Connection		22	/PGM	Prog. Mode	Input
5	A7	Address 7	Input	23-24	A0,A1	Address 0,1	Input
6-7	V_{CC}	Power Supply		25-26	NC	No Connection	
8-10	NC	No Connection		27	A2	Address 2	Input
11	/CE	Chip Select	Input	28-29	GND	Ground	
12	/OE	Output Enable	Input	30-31	NC	No Connection	
13	EPM	EPROM Prog. Mode	Input	32	A3	Address 3	Input
14	V_{PP}	Prog. Voltage	Input	33-37	D0-D4	Data 0,1,2,3,4	In/Output
15	A8	Address 8	Input	38-40	NC	No Connection	
16-18	NC	No Connection		41-43	D5-D7	Data 5,6,7	In/Output
19	A9	Address 9	Input	44	A4	Address 4	Input
20	A11	Address 11	Input				

PIN FUNCTIONS

EPROM Programming Mode

D7-D0 *Data Bus.* The data can be read from or written to external memory through the data bus.

A11-A0 *Address Bus.* During programming, the EPROM address is written to the address bus.

V_{CC} *Power Supply.* This pin must supply 5V during the EPROM read mode and 6V during other modes.

/CE *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode and Program Verify Mode.

/OE *Output Enable* (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} *Program Voltage.* This pin supplies the program voltage.

/PGM *Program Mode* (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise surges*** above V_{CC} occur on pins XTAL1 and /RESET.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{PP}, /CE, /EPM, /OE pins while the microcontroller is in standard mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC};
- Adding a capacitor to the affected pin.

Z86E40 Standard Mode

XTAL *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

R/W *Read/Write* (output, write Low). The R/W signal is Low when the CCP is writing to the external program or data memory.

/RESET *Reset* (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. After the POR time, /RESET is a Schmitt-triggered input.

To avoid asynchronous and noisy reset problems, the Z86E40 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5-10 TpC cycles after /RESET is released. For Power-On Reset, the reset output time is 5 ms. The Z86E40 does not reset WDTMR, SMR, P2M, and P3M registers on a STOP-Mode Recovery operation.

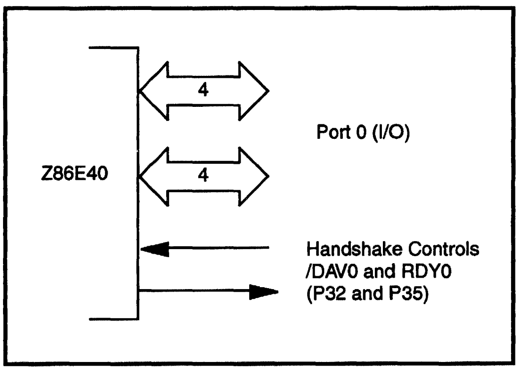
/ROMless (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions normally as a Z8 ROM version).

Note: When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.

Port 0 (P07-P00). Port 0 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the high-impedance mode if selected as an address output state, along with Port 1 and the control signals /AS, /DS, and R//W (Figure 9).



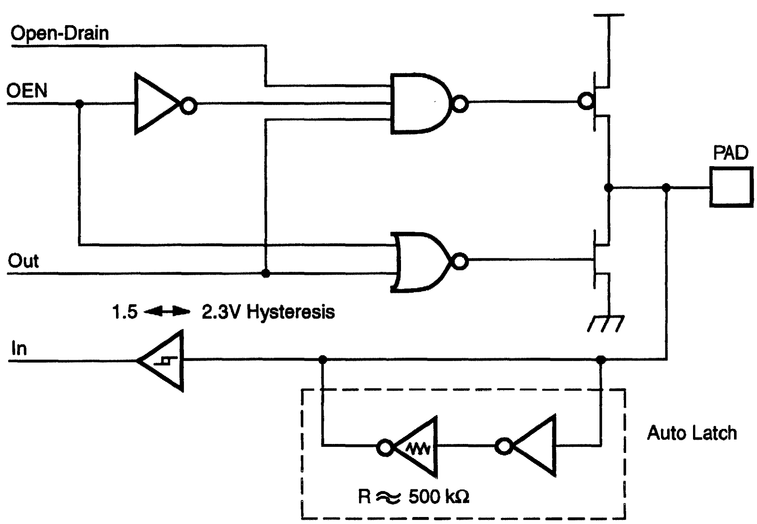


Figure 9. Port 0 Configuration

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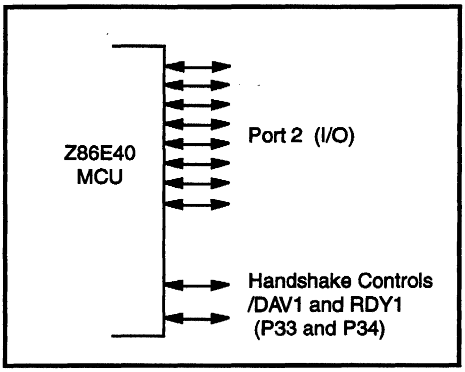
PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, bi-directional, CMOS compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 10).

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the Z86E40 to share common resources in multiprocessor and DMA applications.



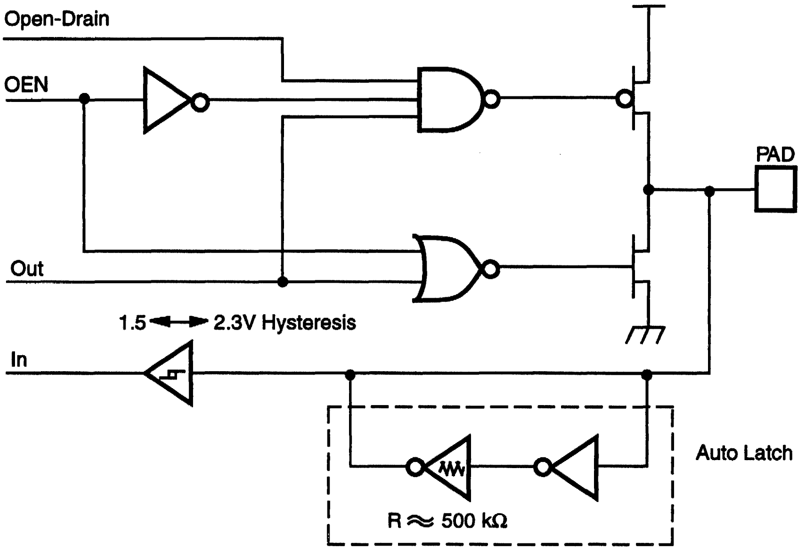


Figure 10. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 11).

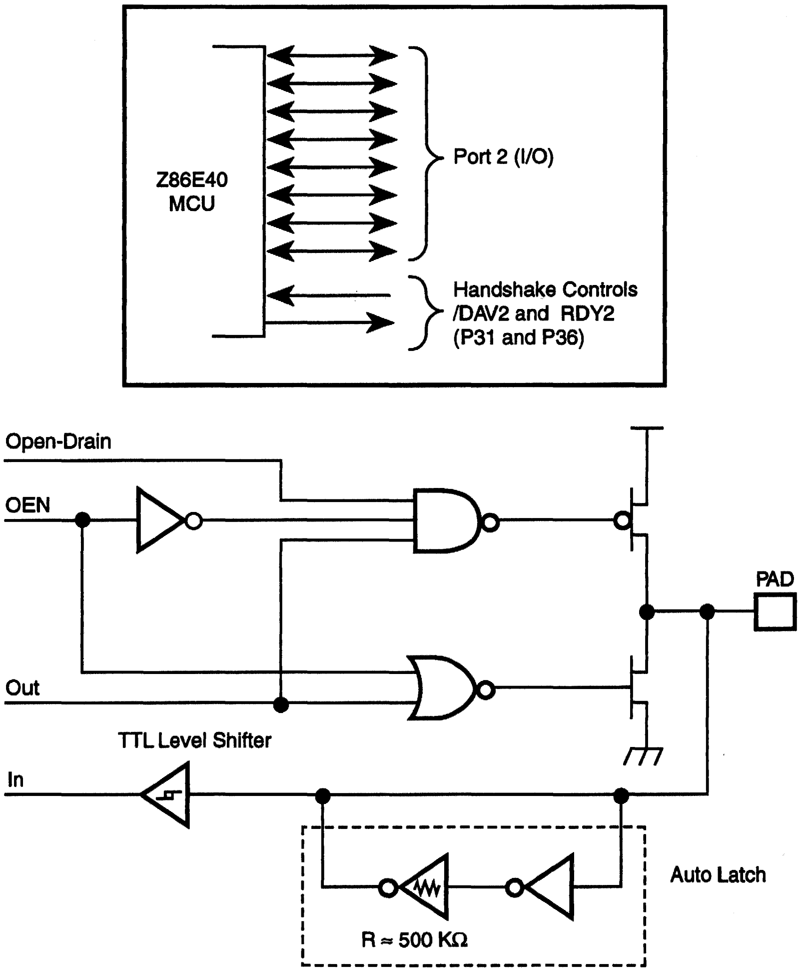


Figure 11. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible port with our fixed inputs (P33-P30) and four fixed outputs (P37-P34). These eight lines can be configured by software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt- triggered. P31, P32 and P33 are standard CMOS inputs (no Auto Latches) and P34, P35, P36 and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respectively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (Figure 12). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Port 0, Port 1, and Port 2 are also available on Port 3 (Table 7).

Note: P33-P30 differs from the Z86C40 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

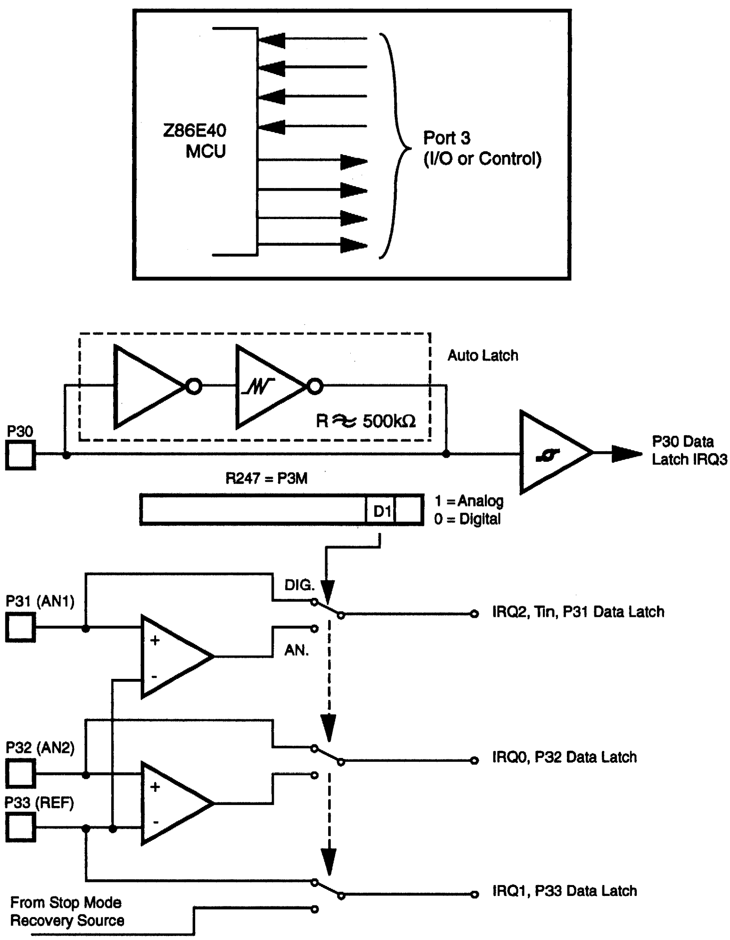


Figure 12. Port 3 Configuration

Table 7. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Interrupt	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T_{IN}	AN1	IRQ2		D/R		
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT		AN1-Out			R/D		/DM
P35	OUT				R/D			
P36	OUT	T_{OUT}				R/D		
P37	OUT		An2-Out					

Comparator Inputs. Port 3, P31 and P32, each have a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 2 and P30. There are no Auto Latches on P31, P32, and P33.

Low EMI Emission. The Z86E40 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1)

FUNCTIONAL DESCRIPTION

The Z86E40 MCU incorporates the following special functions to enhance the standard Z8® architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watch-Dog Timer
3. STOP-Mode Recovery Source

Having the Auto Power-on Reset circuitry built-in, the Z86E40 does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles. The Z86E40 does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP-Mode Recovery operation. Note: The device V_{CC} must rise up to the operating V_{CC} specification before the T_{POR} expires.

Program Memory. The Z86E40 can address up to 4 Kbytes of internal program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000CH) to address 4095 (0FFFH) consists of programmable EPROM. After reset, the program counter points at the address 000CH which is the starting address of the user program. In ROMless mode, the Z86E40 can address up to 64 Kbytes of external program memory. The ROM/ROMless option is only available on the 44-pin devices.

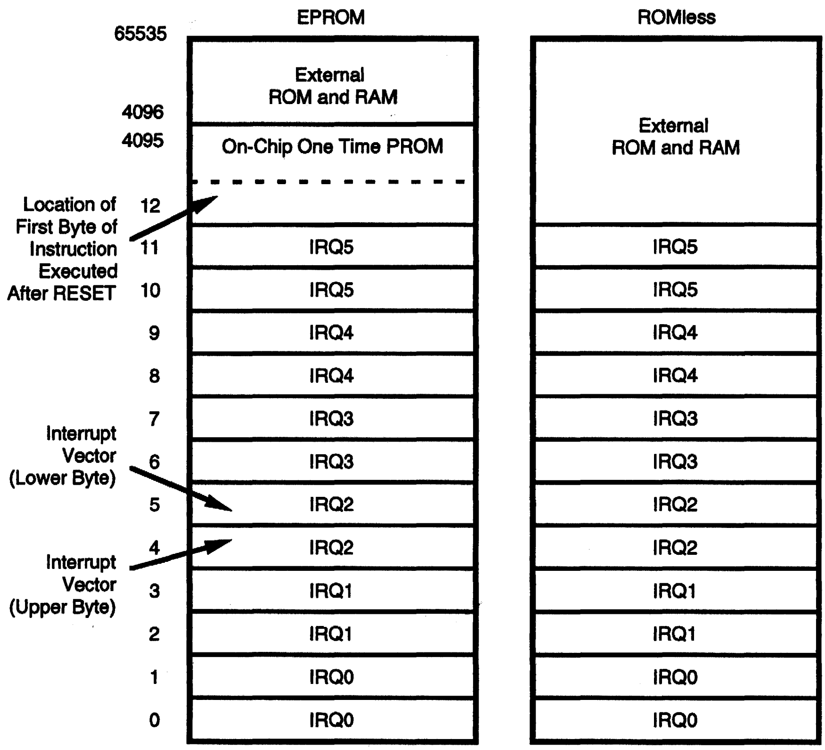


Figure 13. Program Memory Map

EPROM Protect. The 4 Kbytes of program memory is a one-time PROM. ***An EPROM protect feature prevents dumping of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to program memory in all modes.*** ROM look-up tables cannot be used with this feature.

Data Memory (/DM). In EPROM mode, the Z86E40 can address up to 60 Kbytes of external data memory beginning at location 4096. In ROMless mode, the Z86E40 can address up to 64 Kbytes of data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory.

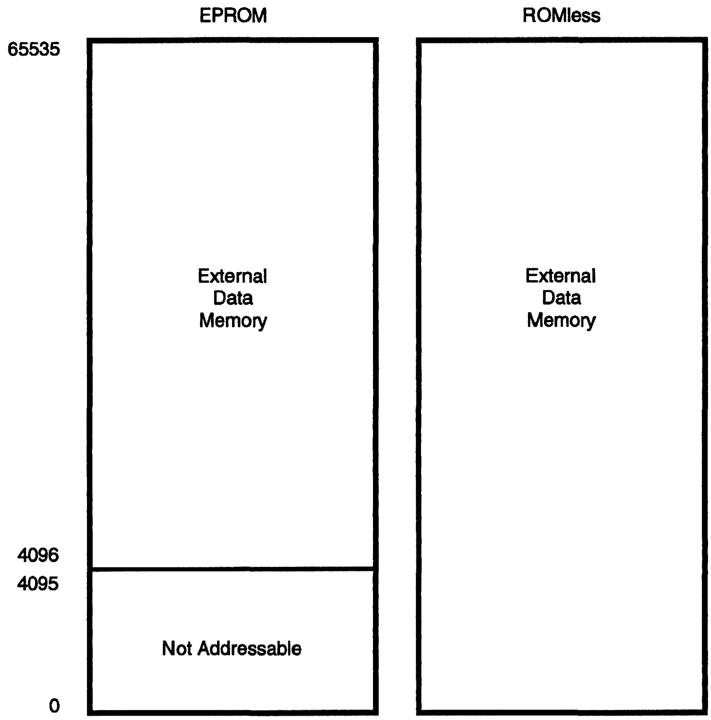
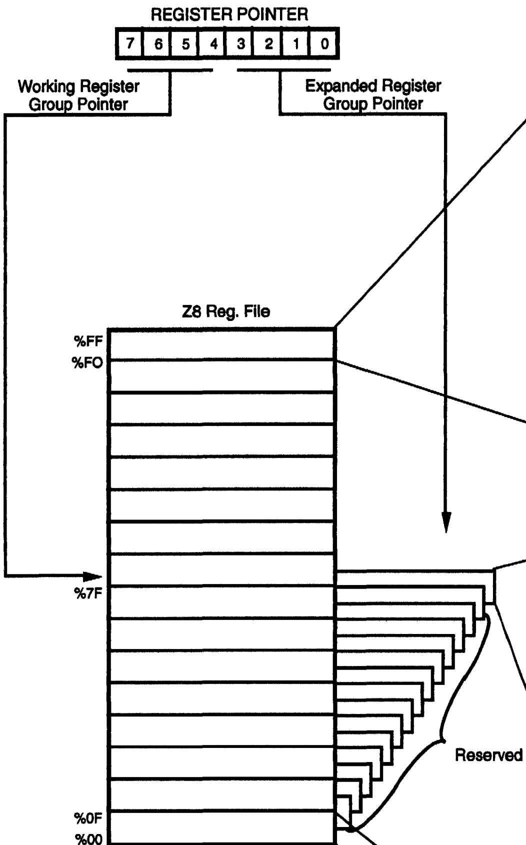


Figure 14. Data Memory Map

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 15). These register groups are known as the Expanded Register File (ERF). The low nibble (D3-D0) of the Register Pointer (RP) select the active ERF group, and the high nibble (D7-D4) of register RP select the working register group (Figure 16). Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

FUNCTIONAL DESCRIPTION (Continued)



Z8® STANDARD CONTROL REGISTERS

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
	% FF	SPL	U	U	U	U	U	U	U	U
	% FE	Reserved	U	U	U	U	U	U	U	U
	% FD	RP	0	0	0	0	0	0	0	0
	% FC	FLAGS	U	U	U	U	U	U	U	U
	% FB	IMR	0	U	U	U	U	U	U	U
	% FA	IRQ	0	0	0	0	0	0	0	0
	% F9	IPR	U	U	U	U	U	U	U	U
†	% F8	P01M	0	1	0	0	1	1	0	1
*	% F7	P3M	0	0	0	0	0	0	0	0
*	% F6	P2M	1	1	1	1	1	1	1	1
	% F5	PRE0	U	U	U	U	U	U	U	0
	% F4	T0	U	U	U	U	U	U	U	U
	% F3	PRE1	U	U	U	U	U	U	0	0
	% F2	T1	U	U	U	U	U	U	U	U
	% F1	TMR	0	0	0	0	0	0	0	0
	% F0	Reserved								

EXPANDED REG. GROUP (F)

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
*	% (F) 0F	WDTMR	U	U	U	0	1	1	0	1
	% (F) 0E	Reserved								
	% (F) 0D	Reserved								
	% (F) 0C	Reserved								
**	% (F) 0B	SMR	0	0	1	0	0	0	0	0
	% (F) 0A	Reserved								
	% (F) 09	Reserved								
	% (F) 08	Reserved								
	% (F) 07	Reserved								
	% (F) 06	Reserved								
	% (F) 05	Reserved								
	% (F) 04	Reserved								
	% (F) 03	Reserved								
	% (F) 02	Reserved								
	% (F) 01	Reserved								
	% (F) 00	PCON	1	1	1	1	1	1	1	0

EXPANDED REG. GROUP (0)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
% (0) 03	P3	*1	*1	1	1	U	U	U	U
% (0) 02	P2	U	U	U	U	U	U	U	U
% (0) 01	P1	U	U	U	U	U	U	U	U
% (0) 00	P0	U	U	U	U	U	U	U	U

Notes:
U = Unknown
† For Z86E40 (ROMless) reset condition: "10110110"
* Will not be reset with a STOP Mode Recovery
** Will not be reset with a STOP Mode Recovery, except Bit D0.

Figure 15. Expanded Register File Architecture

Register File. The 256 byte register file consists of four I/O port registers, 236 general-purpose registers and 15 control and status registers (R240 is reserved). The instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addresses using the Register Pointer (Figures 16 and 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0H-EFH can only be accessed through working registers and indirect addressing modes.

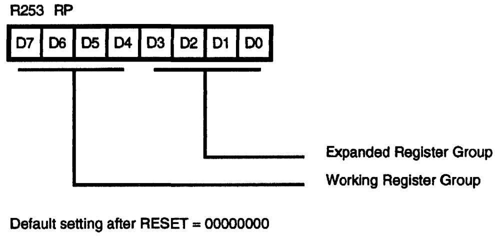
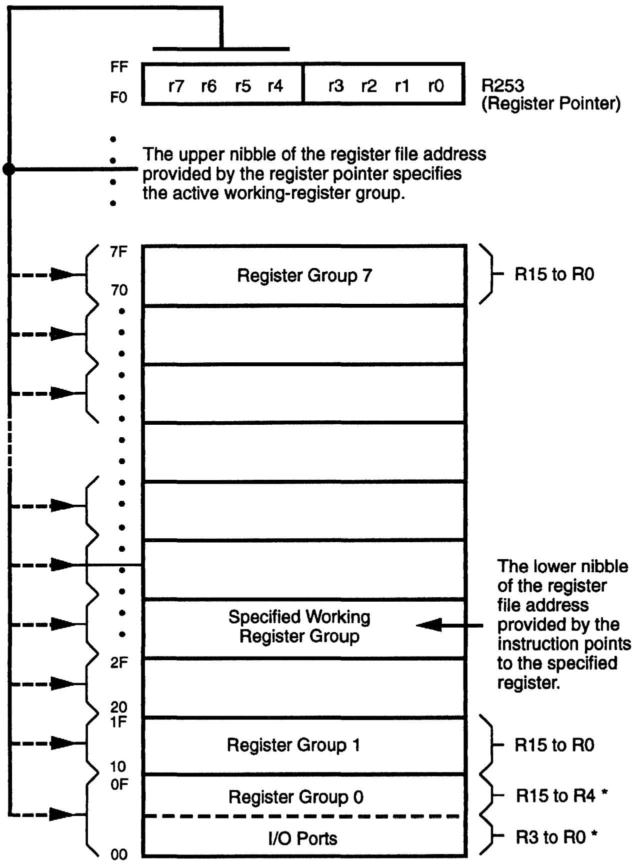


Figure 16. Register Pointer Register



* Expanded Register Group (0) is selected in this figure by handling bits D3 to D0 as "0" in Register R253 (RP).

Figure 17. Register Pointer

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FUNCTIONAL DESCRIPTION (Continued)

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range.

RAM Protect. The upper portion of the RAM's address spaces 80H to EFH (excluding the control registers) can be protected from reading and writing. This option can be selected during the EPROM Programming Mode. After this option is selected, the user can activate this feature from the internal EPROM. D6 of the IMR control register (R251) is used to turn off/on the RAM protect by loading a 0 or 1, respectively. A 1 in D6 indicates RAM Protect enabled.

Stack. The Z86E40 external data memory or the internal register file can be used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack which can reside anywhere in the data memory for ROMless mode, but only from 4096 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). SPH can be used as a general-purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 18).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

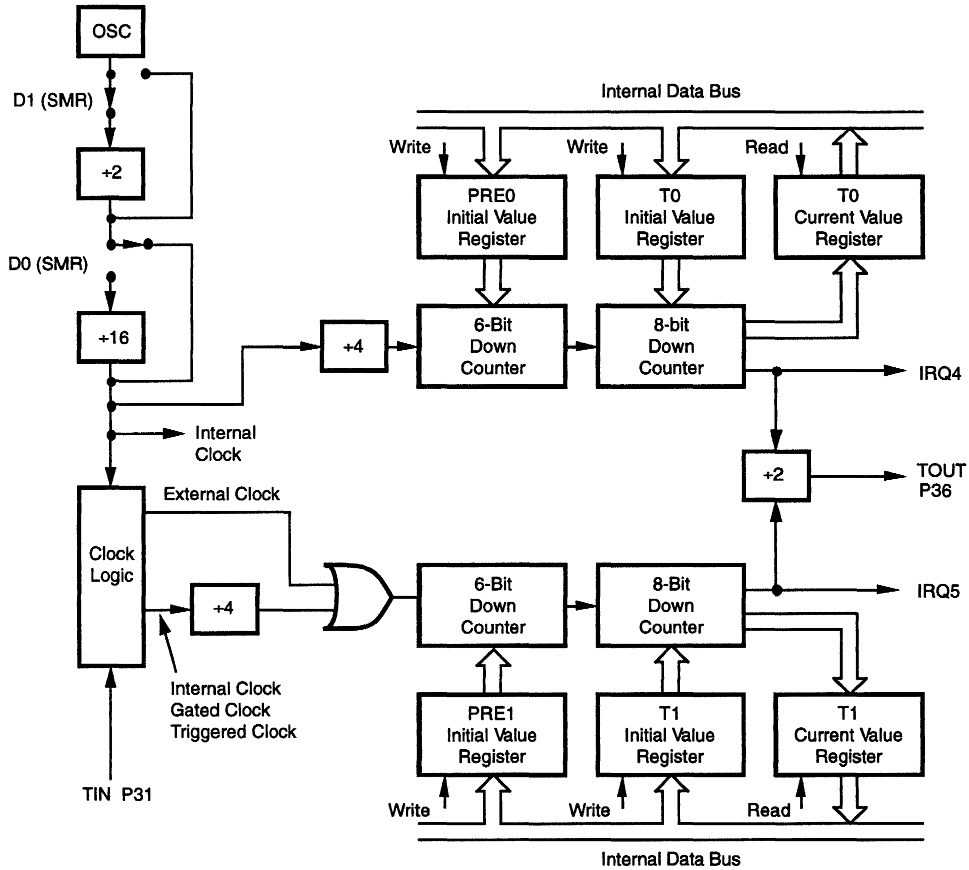

Figure 18. Counter/Timer Block Diagram

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FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86E40 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 19). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30) and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 8).

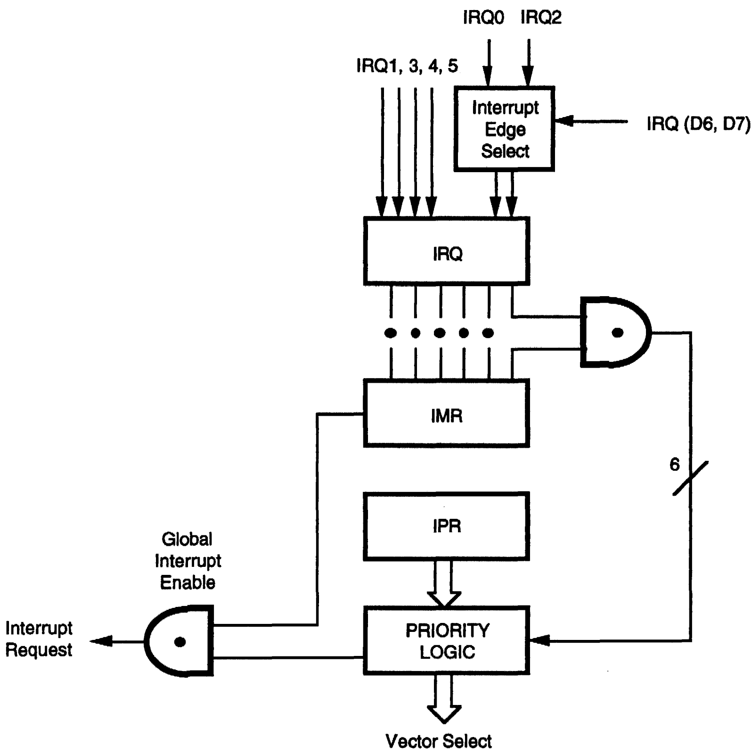


Figure 19. Interrupt Block Diagram

Table 8. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	TI	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E40 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 9.

Table 9. IRQ Register Configuration

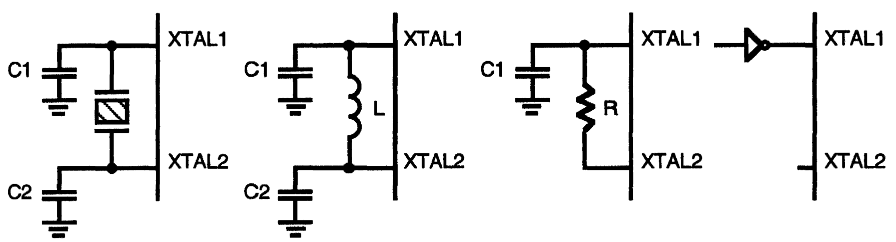
IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86E40 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 20).

Note: RC OSC does not support 12 MHz.



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC
C1, C2 = 22 pF
L = 130 µH *
F = 3 MHz *

RC
@ 5V Vcc (TYP)
C1 = 33 pF *
R = 1K *
F = 6.6 MHz *

External Clock

* Typical value including pin parasitics

Figure 20. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. STOP-Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF  NOP   ; clear the pipeline
6F  STOP  ; enter STOP mode
            or
FF  NOP   ; clear the pipeline
7F  HALT  ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. STOP mode is terminated by one of the following resets: either by WDT time-out, POR, a STOP-Mode Recovery Source which is defined by the SMR register or external reset. This causes the processor to restart the application program at address 000CH.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2 and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 21).

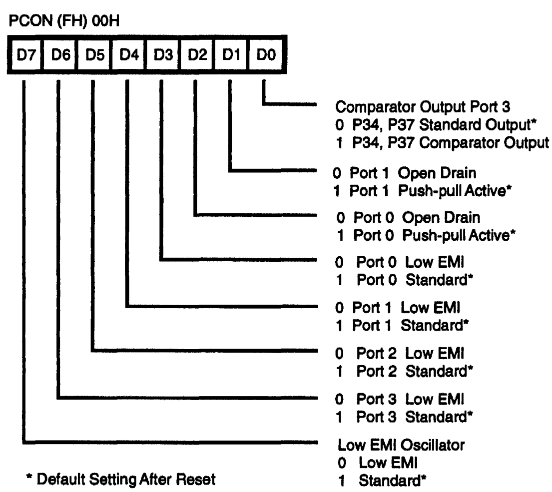


Figure 21. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1.

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive, however, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1. **Note:** 4 MHz is the maximum external clock frequency when running in the low EMI oscillator mode.

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP-Mode Recovery (Figure 22). All bits are Write Only except bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the STOP-Mode Recovery Source. The SMR is located in Bank F of the Expanded Register Group at address OBH.

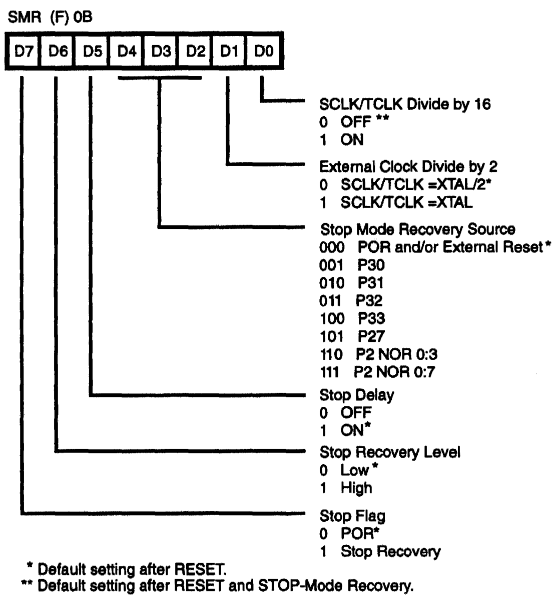


Figure 22. STOP-Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

FUNCTIONAL DESCRIPTION (Continued)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the STOP-Mode Recovery (Figure 23). Table 10 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up from STOP mode when programmed as analog inputs.

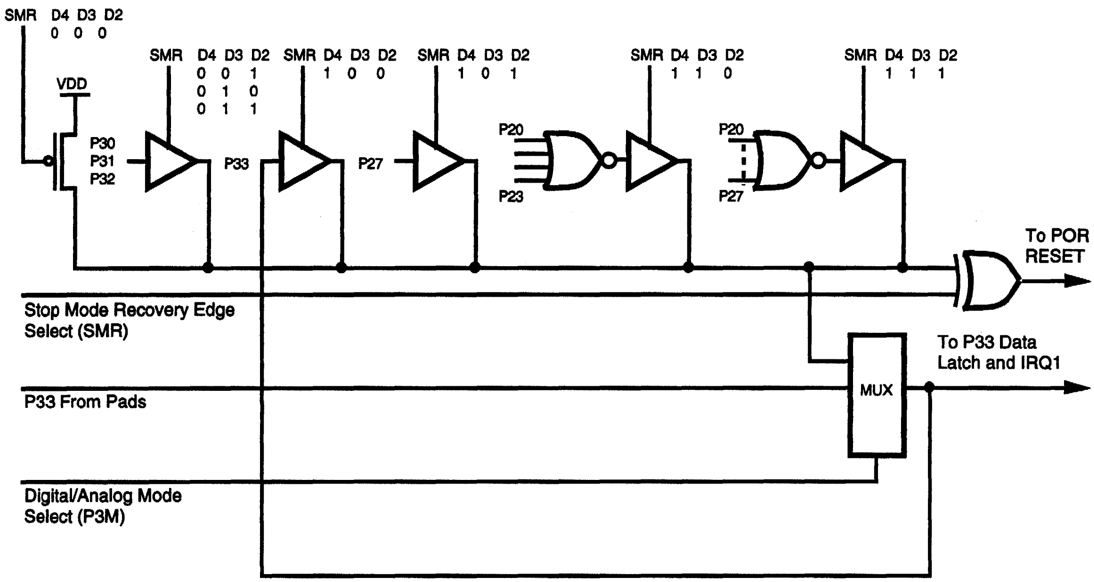


Figure 23. STOP-Mode Recovery Source

Table 10. STOP-Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

STOP-Mode Recovery Delay Select (D5). The 5 ms RESET delay after STOP-Mode Recovery is disabled by programming this bit to a zero. A 1 in this bit will cause a 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the STOP-Mode Recovery source needs to be kept active for at least 5TpC.

STOP-Mode Recovery Level Select (D6). A 1 in this bit defines that a high level on any one of the recovery sources wakes the Z86E40 from STOP mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. A 0 in this bit indicates that the device has been reset by POR (cold). A 1 in this bit indicates the device was awakened by a SMR source (warm).

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled when it has been enabled. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Time-out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 11). The default value of D0 and D1 are 1 and 0, respectively.

Table 11. Time-out Period of the WDT

D1	D0	Time-out of the Internal RC OSC	Time-out of the External Clock
0	0	5 ms	256TpC
0	1	15 ms*	512TpC*
1	0	25 ms	1024TpC
1	1	100 ms	4096TpC

Notes:
TpC = External clock cycle.
* The default setting is 15 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates that the WDT is active during HALT. A 0 disables the WDT in HALT mode. The default value is 1.

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during STOP. A 0 disables the WDT during STOP mode.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

WDTMR Register Accessibility. The WDTMR register is accessible only during the ***first 64*** internal system clock cycles from the execution of the first instruction after Power-On Reset, Watch-Dog reset or a STOP-Mode Recovery (Figures 24 and 25). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location OFH.

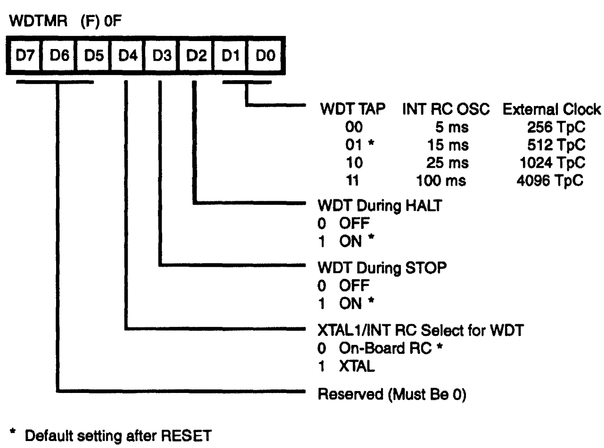


Figure 24. Watch-Dog Timer Mode Register (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

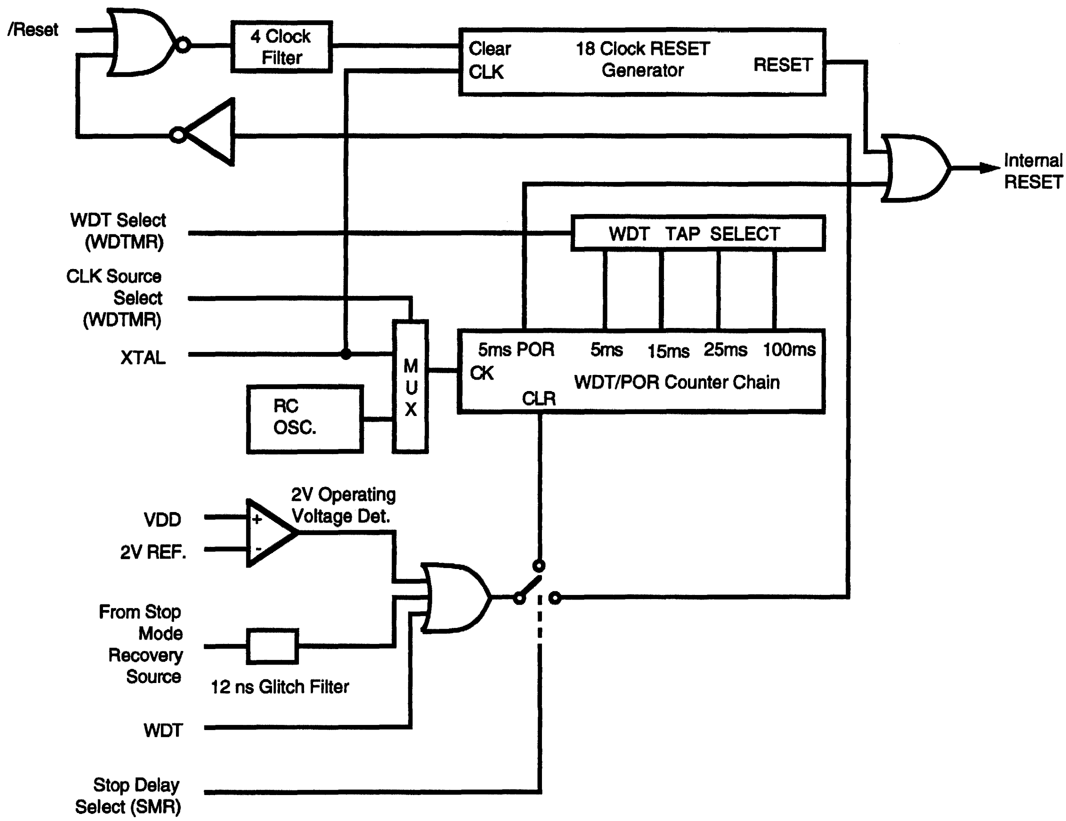


Figure 25. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{RST} (Figure 26). If the V_{CC} drops below 4.5V while the device is operating, the device must be powered down, then powered up again.

Note: V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum Power-On Reset time-out (T_{POR}).

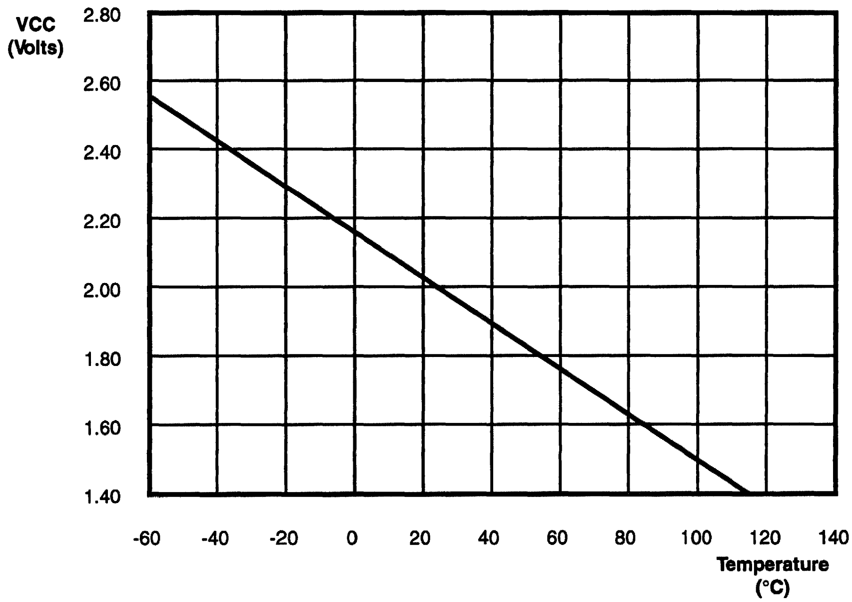


Figure 26. Typical Z86E40 V_{RST} Voltage vs Temperature

FUNCTIONAL DESCRIPTION (Continued)

EPROM Programming Mode

Table 12 shows the programming voltages of each programming mode. Table 13, Figures 27, 28, and 29 show the programming timing of each programming mode. Figure 30 shows the circuit diagram of a Z86E40 programming adaptor, which adapts from 2764A to Z86E40. Figure 31 shows the flow-chart of an Intelligent Programming Algorithm, which is compatible with 2764A EPROM (Z86E40 is 4K EPROM, 2764A is 8K EPROM). Since the EPROM size of Z86E40 differs from 2764A, the programming address range has to be set from 0000H to 0FFFH. Otherwise, the upper 4K of data (1000H-1FFFH) will overwrite the lower 4K of data.

Note: EPROM Protect feature disables the LDC, LDCI, LDE, and LDEI instructions, and a ROM look-up table cannot be used with this feature.

Table 12. EPROM Programming Table

Programming Modes	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ1	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V†
EPROM READ2	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V†
PROGRAM	V_H	X	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.0V
PROGRAM VERIFY	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
EPROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
RC OSCILLATOR SELECT	V_H	V_{IL}	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
RAM PROTECT	V_H	V_{IH}	V_H	V_{IL}	V_{IL}	NU	NU	6.0V

Notes:
V_H = 12.5V ± 12.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.

Notes (Continued):
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.
† Although most programmers do an EPROM read at V_{CC} = 5.0, Zilog recommends an EPROM read at V_{CC} = 4.5 and 5.0 to ensure proper device operations during the V_{CC} after programming.

Table 13. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95	1.05	ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

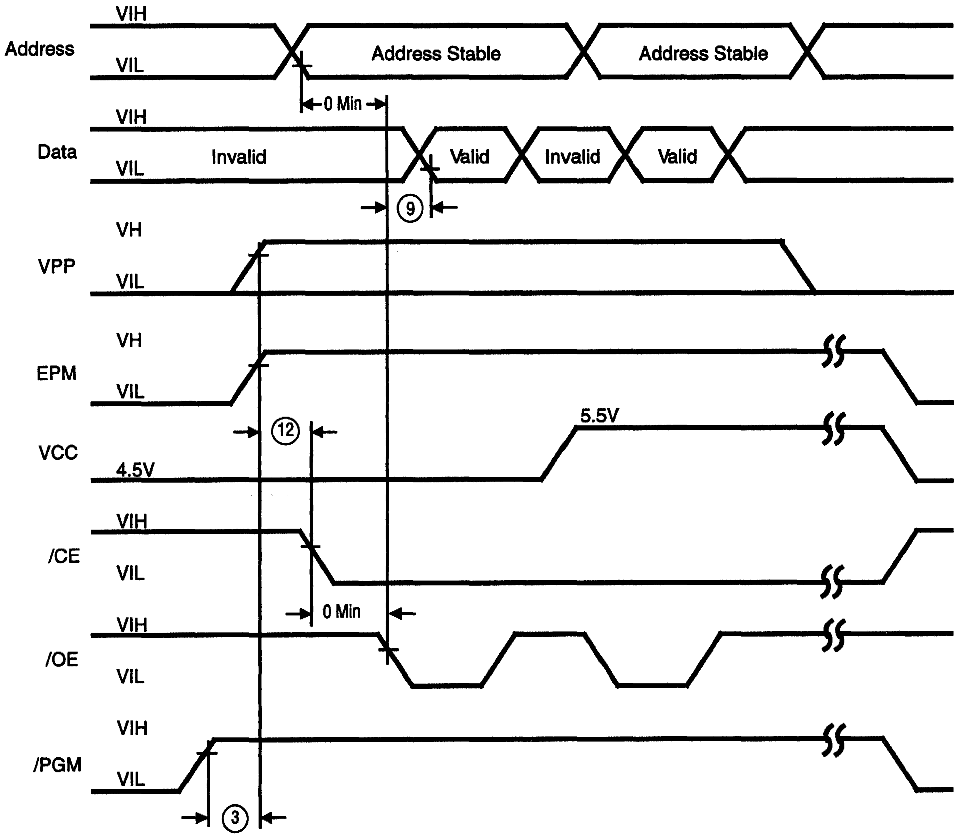


Figure 27. EPROM READ Mode Timing Diagram

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Z86E40 TIMING DIAGRAMS

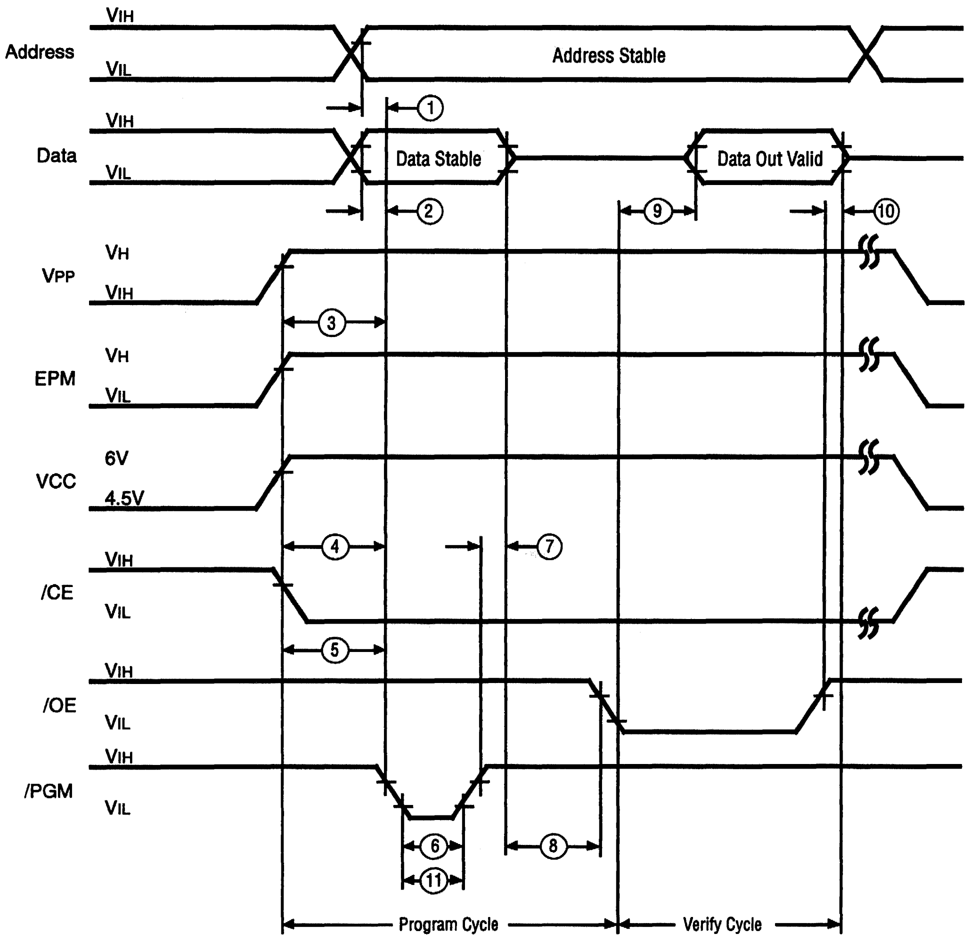


Figure 28. Timing Diagram of EPROM Program and Verify Modes

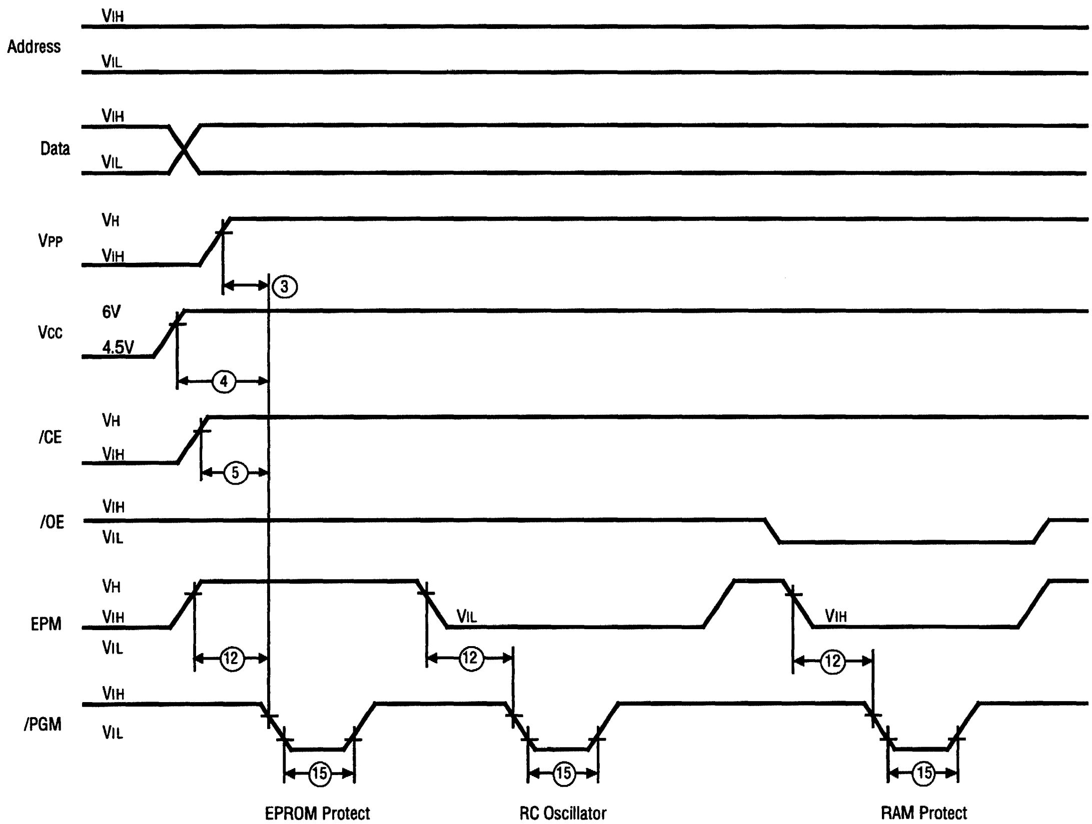


Figure 29. Timing Diagram of EPROM Protect, RAM Protect and RC OSC Modes

FUNCTIONAL DESCRIPTION (Continued)

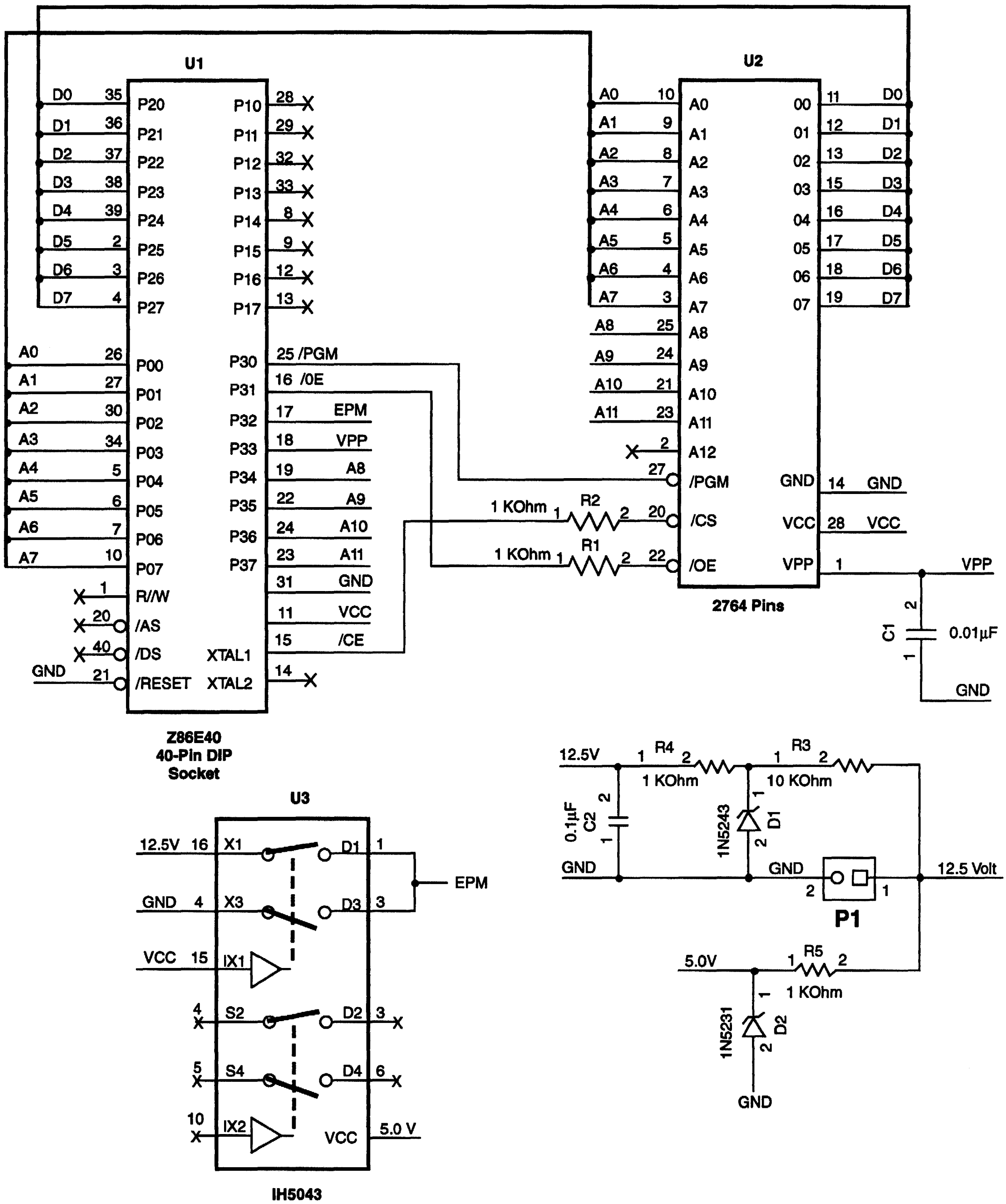
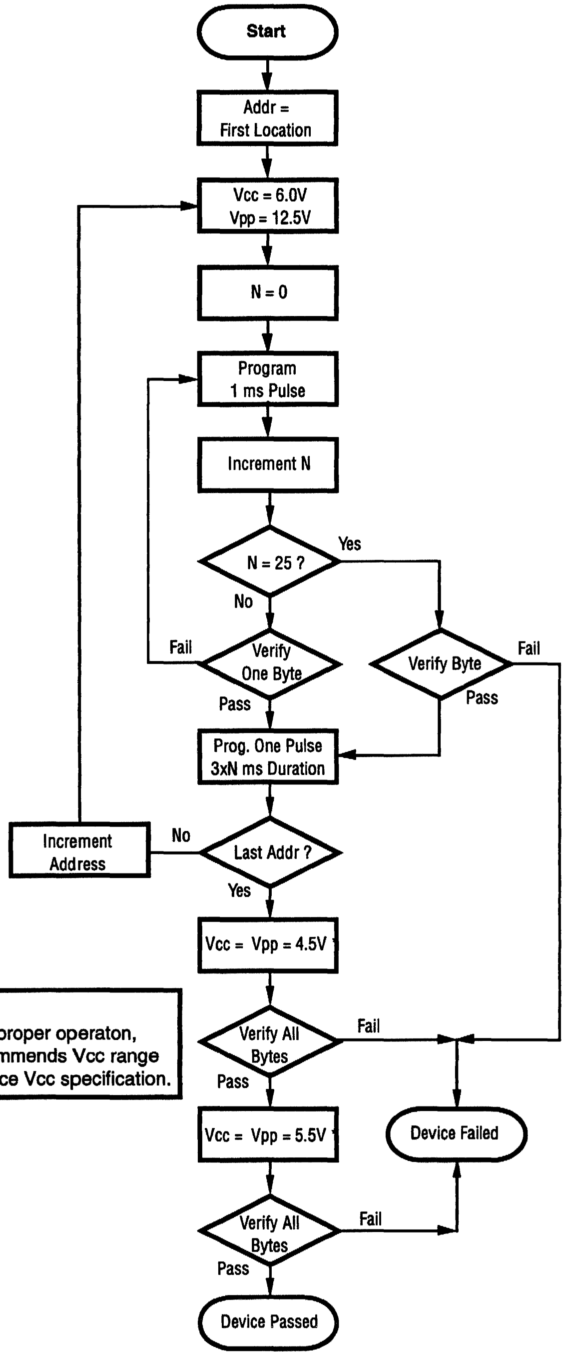


Figure 30. Z86E40 Z8 OTP Programming Adapter



Note:
* To ensure proper operaton, Zilog recommends Vcc range of the device Vcc specification.

Figure 31. Z86E40 Programming Algorithm

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
V_{IHM}	Max. Input Voltage (**)		7	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp	†	†	C
	Power Dissipation		2.2	W

Notes:
* Voltage on all pins with respect to GND.
** Applies to all Port pins only, except Port 31, 32, 33 and must limit current going into or out of port pin to 250 µA max.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 32).

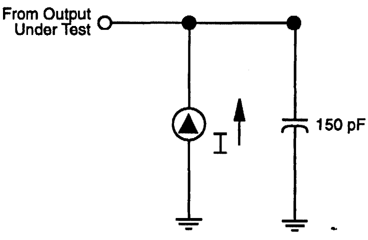


Figure 32. Test Load Diagram

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V; f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

V_{CC} SPECIFICATION

V_{CC} 5.0V ±0.5V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} Note[3]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	5.0V		V_{CC} + 0.5V		V	I_{IN} <250 µA	[7]
V_{CH}	Clock Input High Voltage	5.0V	0.7 V_{CC}	V_{CC} + 0.3V	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	5.0V	V_{SS} –0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	5.0V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		[7]
V_{IL}	Input Low Voltage	5.0V	V_{SS} –0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage (Low EMI Mode)	5.0V 5.0V	V_{CC} –0.4 V_{CC} –0.4		4.8	V V	I_{OH} = –2.0 mA I_{OH} = –0.5 mA	[9] [8]
V_{OL1}	Output Low Voltage (Low EMI Mode)	5.0V 5.0V		0.4 0.4	0.1 0.1	V V	I_{OL} = +4.0 mA I_{OL} = +1.0 mA	[9] [8]
V_{OL2}	Output Low Voltage	5.0V		1.5	0.3	V	I_{OL} = +12 mA, 3 Pin Max	[9]
V_{RH}	Reset Input High Voltage	5.0V	0.7 V_{CC}	V_{CC}+0.3	2.1	V		
V_{RI}	Reset Input Low Voltage	5.0V	V_{SS} –0.3	0.2 V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	5.0V		50	10	mV		
I_{IL}	Input Leakage	5.0V	–10	+10	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	5.0V	–10	+10	<1	µA	V_{IN} = 0V, V_{RL} = 0	
I_{IR}	Reset Input Current	5.0V	60	45		µA	V_{CC} = 5.0V,	
I_{CC}	Supply Current (Standard Mode)	5.0V	16 20	15.0 18		mA mA	@ 8 MHz @ 12 MHz	[4,5] [4,5]

10

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC} Note[3]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Standard Mode)	5.0V		6.0	3.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4,5]
		5.0V		7.5	4.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5]
		5.0V		3.0	1.5	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		5.0V		3.0	1.7	mA	Clock Divide by 16 @ 12 MHz	[4,5]
I_{CC}	Supply Current (Low EMI Mode)	5.0V		7.5	5.0	mA	@ 2 MHz	[4,5]
		5.0V		12.0	8.0	mA	@ 4 MHz	[4,5]
I_{CC1}	Standby Current (Low EMI Mode)	5.0V		2.0	1.0	mA	@ 2 MHz	[4,5]
		5.0V		3.0	1.5	mA	@ 4 MHz	[4,5]
		5.0V		2.0	0.75	mA	Clock Divide-by-16 @ 2 MHz	[4,5]
		5.0V		2.0	1.0	mA	Clock Divide-by-16 @ 4 MHz	[4,5]
I_{CC2}	Standby Current	5.0V		10	2	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running	[6]
		5.0V		800	450	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is Running	[6,10]
I_{ALL}	Auto Latch Low Current	5.0V		–10	–5	µA	0V < V_{IN} < V_{CC}	
I_{ALH}	Auto Latch High Current	5.0V		20	10	µA	0V < V_{IN} < V_{CC}	
T_{POR}	Power-On Reset	5.0V	2.5		4.5	ms		
V_{RST}	Auto Reset Voltage				2.6	V		

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock-driven crystal	0.3 mA	6.0	mA	8 MHz
or resonator	3.5 mA	6.0	mA	8 MHz

[2] V_{SS}=0V=GND.
[3] V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum T_{POR} timeout. V_{CC} specified at 4.5V to 5.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] Except clock pins and Port 3 input pins in EPROM mode.
[8] Port Low EMI mode.
[9] Port STD mode.
[10] Internal RC

AC ELECTRICAL CHARACTERISTICS

External I/O or Memory Read/Write Timing Diagrams (Standard Mode)

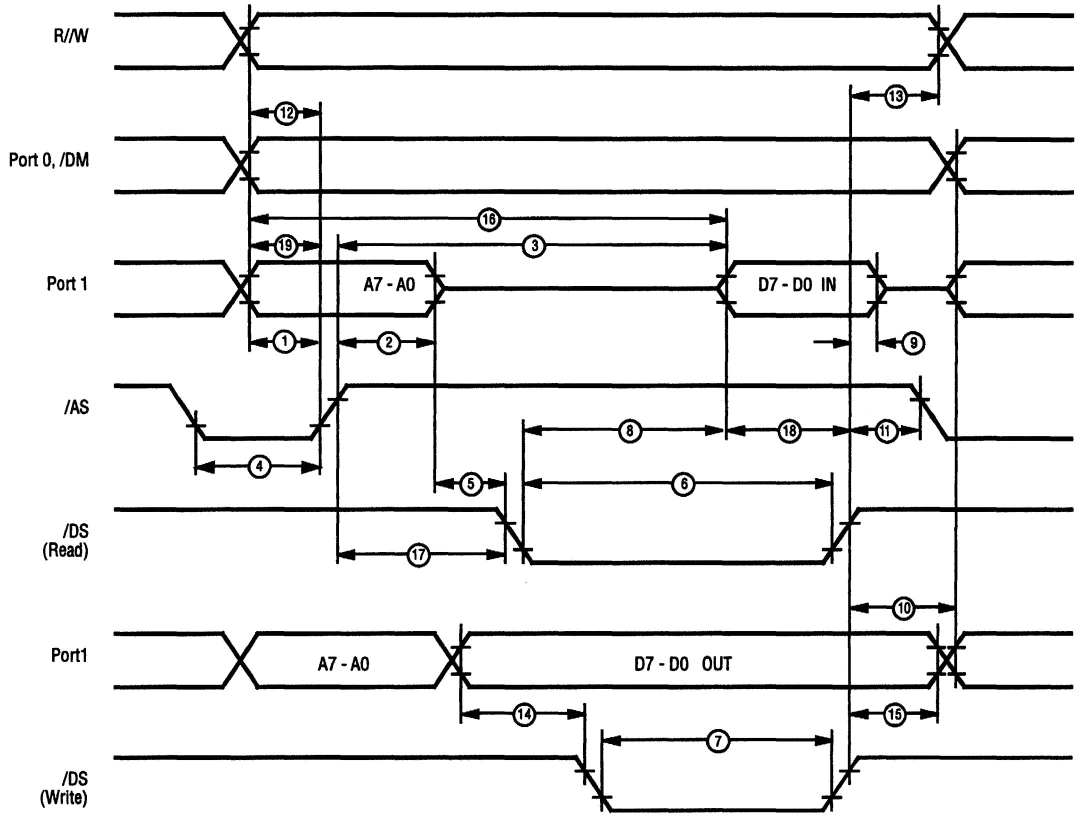


Figure 33. External I/O or Memory Read/Write Timing

AC ELECTRICAL CHARACTERISTICS
External I/O or Memory Read/Write Timing (Standard Mode)

				Standard Mode					
			V_{CC}	8 MHz		12 MHz			
No	Symbol	Parameter	Note [1]	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	5.0V	35		35		ns	[2]
2	TdAS(A)	/AS Rise to Address Float Delay	5.0V	70		45		ns	[2]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	5.0V		400		250	ns	[1,2]
4	TwAS	/AS Low Width	5.0V	80		55		ns	[2]
5	TdAS(DS)	Address Float to /DS Fall	5.0V					ns	
6	TwDSR	/DS (Read) Low Width	5.0V	300		200		ns	[1,2]
7	TwDSW	/DS (Write) Low Width	5.0V	165		110		ns	[1,2]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	5.0V		260		160	ns	[1,2]
9	ThDR(DS)	Read Data /DS Rise Hold Time	5.0V					ns	[2]
10	TdDS(A)	/DS Rise to Address Active Delay	5.0V	95		55		ns	[2]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	5.0V	70		45		ns	[2]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	5.0V	70		45		ns	[2]
13	TdDS(R/W)	/DS Rise to R//W Not Valid	5.0V	70		45		ns	[2]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	5.0V	80		55		ns	[2]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	5.0V	80		55		ns	[2]
16	TdA(DR)	Address Valid to Read Data Req'd Valid	5.0V		475		310	ns	[1,2]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	5.0V	100		65		ns	[2]
18	TdDI(DS)	Data Output Setup to /DS Rise	5.0V	75		75		ns	[1,2]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	5.0V	55		35		ns	[2]

Notes:
[1] When using extended memory timing add 2TpC.
[2] Timing numbers given are for minimum TpC.
[3] 5.0V ±0.5V Standard Test Load. All timing references use 0.7V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0. Standard operating temperature range 0°C to +70°C.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagrams (Standard Mode)

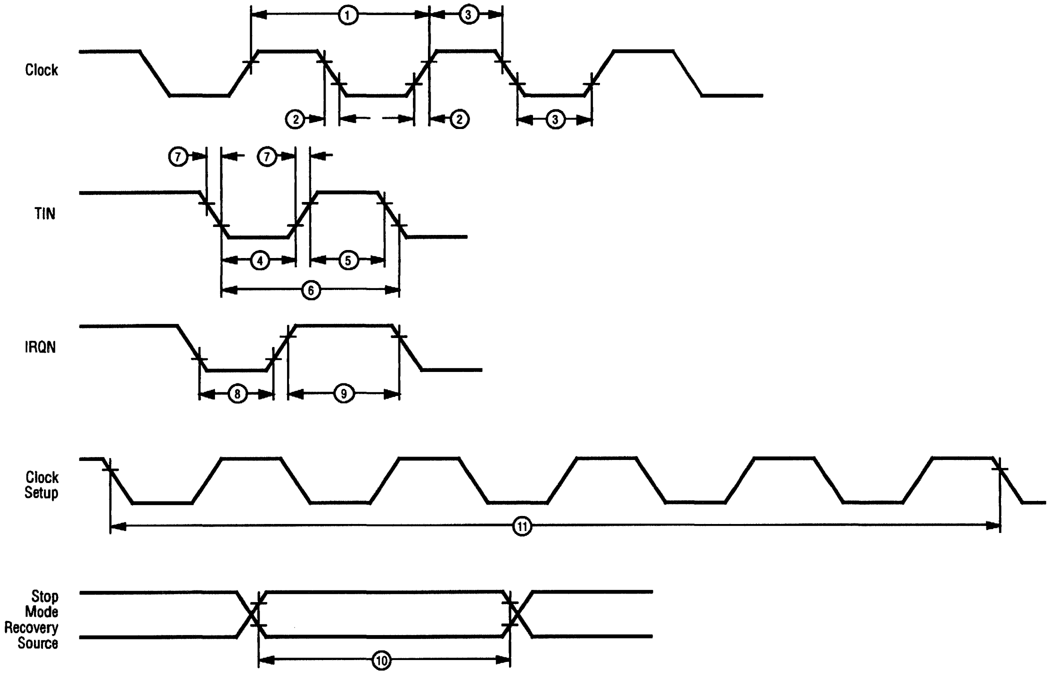


Figure 34. Additional Timing

AC ELECTRICAL CHARACTERISTICS
Additional Timing Table (Standard Mode)

No	Symbol	Parameter	V_{CC} Note [1]	Standard Mode 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
1	TpC	Input Clock Period	5.0V	125	DC	83	DC	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		25		15	ns	[1]
3	TwC	Input Clock Width	5.0V	62.5		41.5		ns	[1]
4	TwTinL	Timer Input Low Width	5.0V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	5.0V	5TpC		5TpC			[1]
6	TpTin	Timer Input Period	5.0V	8TpC		8TpC			[1]
7	TrTin,TfTin	Timer Input Rise & Fall Timers	5.0V		100		100	ns	[1]
8A	TwIL	Int. Request Low Time	5.0V	70		70		ns	[1,2]
8B	TwIL	Int. Request Low Time	5.0V	5TpC		5TpC			[1,3]
9	TwIH	Int. Request Input High Time	5.0V	5TpC		5TpC			[1,2]
10	Twsm	STOP-Mode Recovery Width Spec	5.0V	12		12		ns	[11]
			5.0V	5TpC		5TpC			[10]
11	Tost	Oscillator Startup Time	5.0V		5TpC		5TpC		[4]
12	Twdt	Watch-Dog Timer Delay Time	5.0V	5		5		ms	[6]
			5.0V	15		15		ms	[7]
			5.0V	25		25		ms	[8]
			5.0V	100		100		ms	[9]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] Interrupt request through Port 3 (P30).
[4] SMR-D5 = 0
[5] 5.0V ±0.5V
[6] Reg. WDTMR D1=0, D0=0
[7] Reg. WDTMR D1=0, D0=1
[8] Reg. WDTMR D1=1, D0=0
[9] Reg. WDTMR D1=1, D0=1
[10] Reg. SMR-D5=0. No Delay.
[11] Reg. SMR-D5=1. With Delay.

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Diagrams

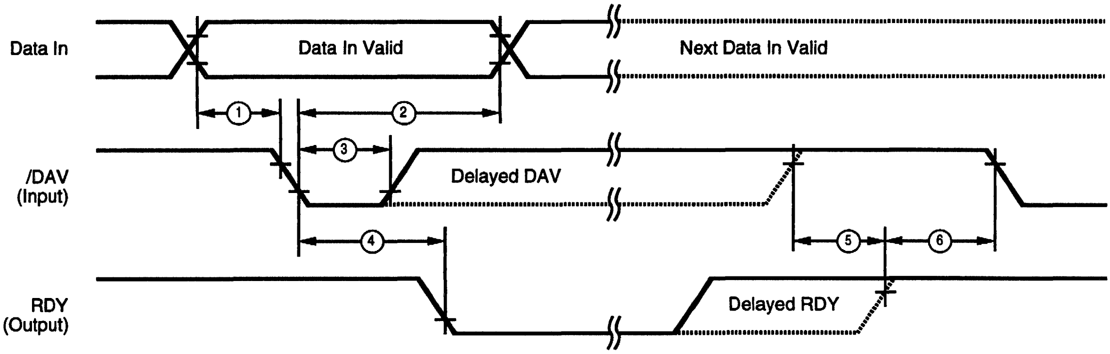


Figure 34. Input Handshake Timing

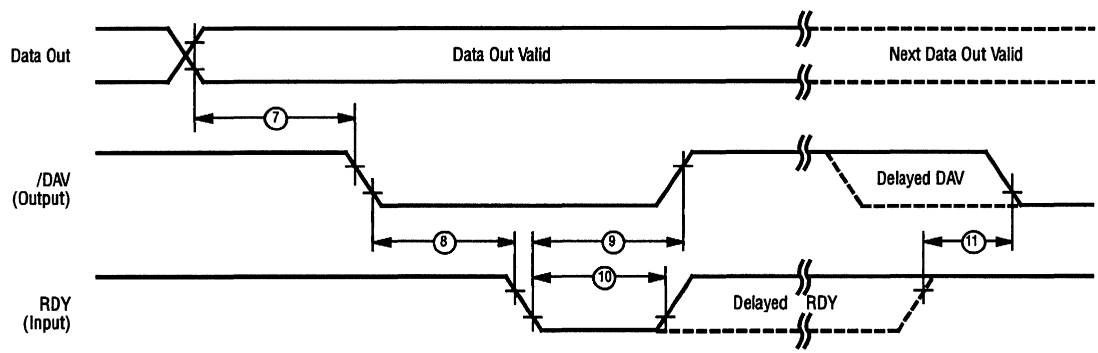


Figure 35. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Table - (Standard Modes)

				Standard Mode				
			V_{CC}	8 MHz		12 MHz		Data
No	Symbol	Parameter	Note[1]	Min	Max	Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	5.0V	0		0		IN
2	ThDI(DAV)	Data In Hold Time	5.0V	115		115		IN
3	TwDAV	Data Available Width	5.0V	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	5.0V		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	5.0V		80		80	IN
6	TdRDYO(DAV)	RDY Rise to DAV Fall Delay	5.0V	0		0		IN
7	TdDO(DAV)	Data Out to DAV Fall Delay	5.0V	63		42		OUT
8	TdDAVO(RDY)	DAV Fall to RDY Fall Delay	5.0V	0		0		OUT
9	TdRDYO(DAV)	RDY Fall to DAV Rise Delay	5.0V		115		115	OUT
10	TwRDY	RDY Width	5.0V	80		80		OUT
11	TdRDYOd(DAV)	RDY Rise to DAV Fall Delay	5.0V		80		80	OUT

Notes:
[1] 5.0 V ±0.5V
Standard operating temperature range 0°C to +70°C

EXPANDED REGISTER FILE CONTROL REGISTERS

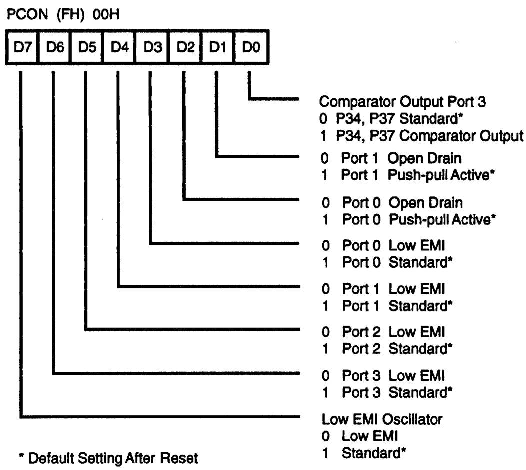


Figure 36. Port Configuration Register (Write Only)

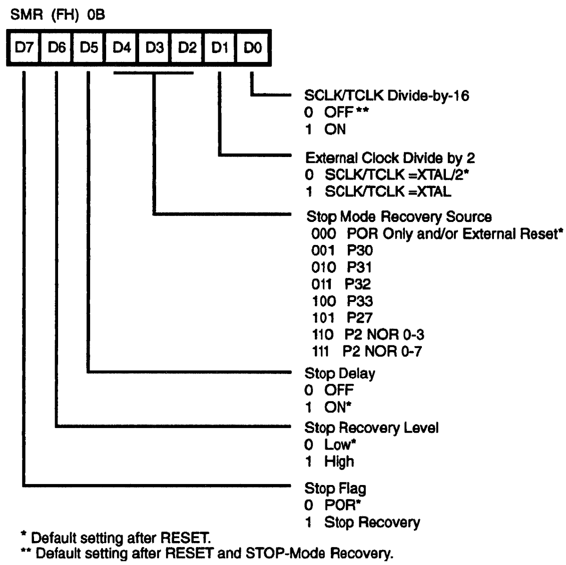


Figure 37. STOP-Mode Recovery Register (Write Only Except Bit D7, Which Is Read Only))

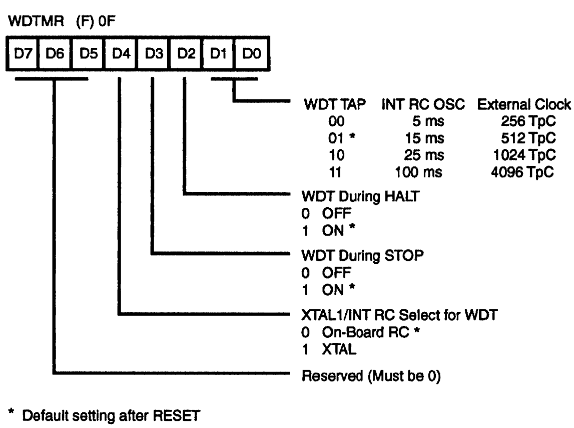


Figure 38. Watch-Dog Timer Mode Register (Write Only)

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Z8 CONTROL REGISTER DIAGRAMS

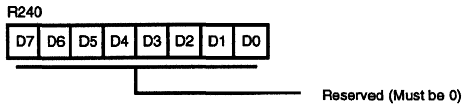
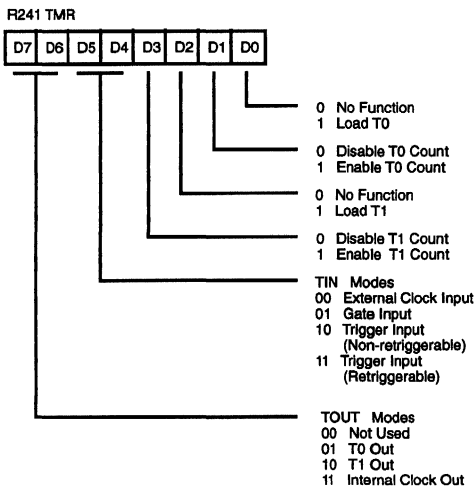


Figure 39. Reserved



Default After Reset = 00H

Figure 40. Timer Mode Register ($F1_H$: Read/Write)

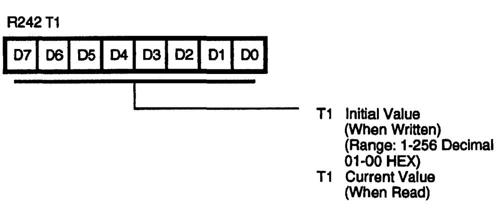
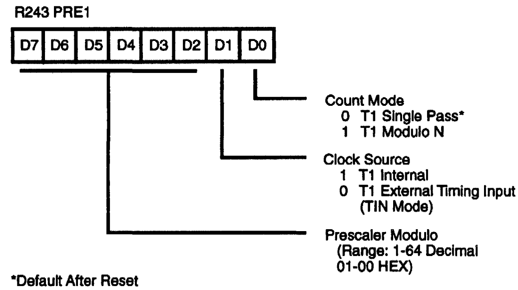


Figure 41. Counter/Timer 1 Register ($F2_H$: Read/Write)



*Default After Reset

Figure 42. Prescaler 1 Register ($F3_H$:Write Only)

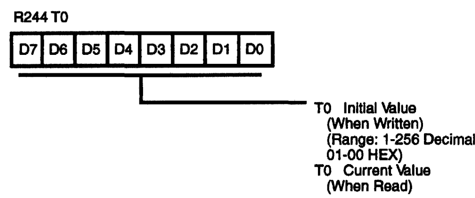


Figure 43. Counter/Timer 0 Register ($F4_H$: Read/Write)

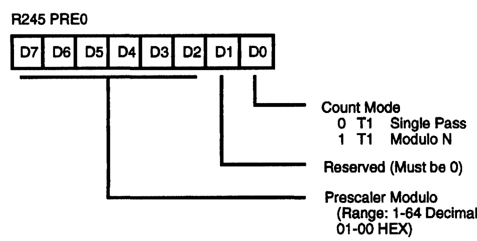


Figure 44. Prescaler 0 Register ($F5_H$: Write Only)

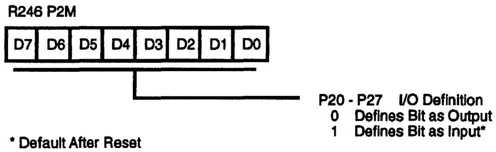


Figure 45. Port 2 Mode Register (F6$_H$: Write Only)

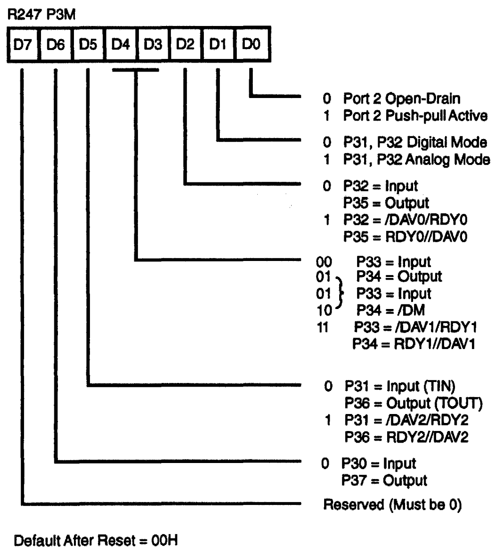


Figure 46. Port 3 Mode Register (F7$_H$: Write Only)

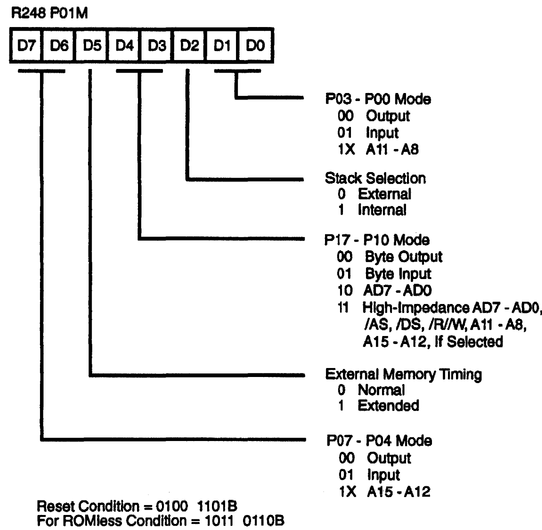


Figure 47. Port 0 and 1 Mode Register (F8$_H$: Write Only)

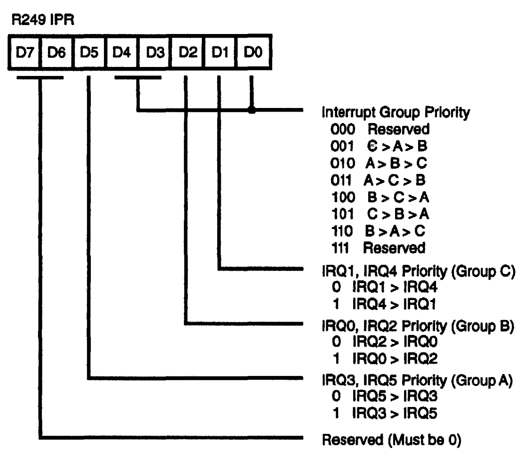


Figure 48. Interrupt Priority Register (F9$_H$: Write Only)

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Z8 CONTROL REGISTER DIAGRAMS (Continued)

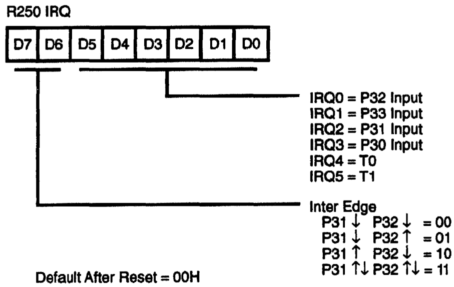

Figure 49. Interrupt Request Register (FA_H: Read/Write)

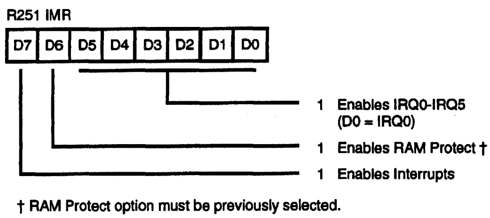

Figure 50. Interrupt Mask Register (FB_H: Read/Write)

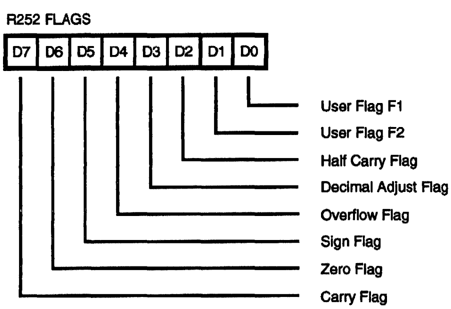

Figure 51. Flag Register (FC_H: Read/Write)

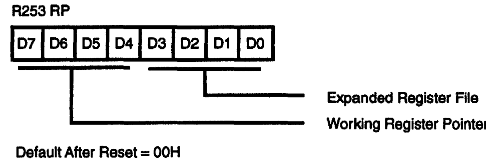

Figure 52. Register Pointer (FD_H: Read/Write)

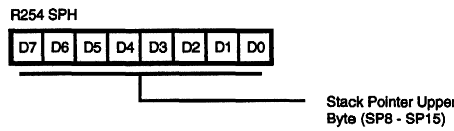

Figure 53. Stack Pointer High (FE_H: Read/Write)

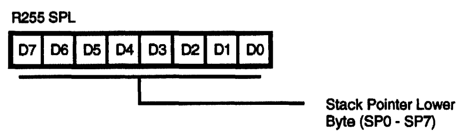

Figure 54. Stack Pointer Low (FF_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
–	Unaffected
x	Undefined

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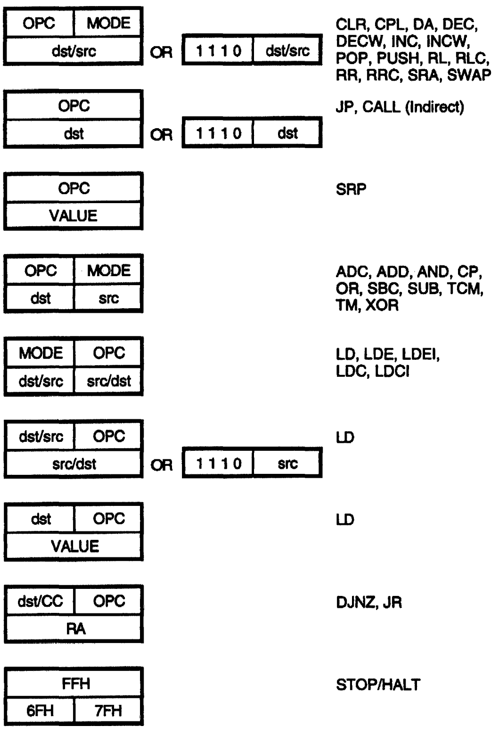
CONDITION CODES

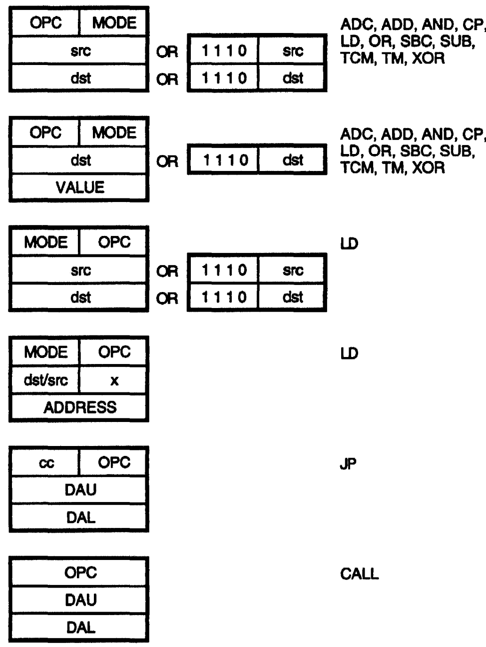
Value	Mnemonic	Meaning	Flags Set
1000		Always True	—
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

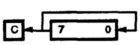
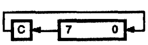
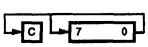
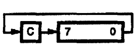
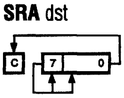
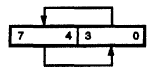
dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	–	*	*	0	–	–
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	–	–	–	–	–	–
CCF C←NOT C			EF	*	–	–	–	–	–
CLR dst dst←0	R IR		B0 B1	–	–	–	–	–	–
COM dst dst←NOT dst	R IR		60 61	–	*	*	0	–	–
CP dst, src dst – src	†		A[ ]	*	*	*	*	–	–
DA dst dst←DA dst	R IR		40 41	*	*	*	X	–	–
DEC dst dst←dst – 1	R IR		00 01	–	*	*	*	–	–
DECW dst dst←dst – 1	RR IR		80 81	–	*	*	*	–	–
DI IMR(7)←0			8F	–	–	–	–	–	–
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	–	–	–	–	–	–
EI IMR(7)←1			9F	–	–	–	–	–	–
HALT			7F	–	–	–	–	–	–

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	–	*	*	*	–	–
INCW dst dst←dst + 1	RR IR		A0 A1	–	*	*	*	–	–
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	–	–	–	–	–	–
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	–	–	–	–	–	–
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	–	–	–	–	–	–
LDC dst, src dst←src	r	Irr	C2	–	–	–	–	–	–
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir	Irr	C3	–	–	–	–	–	–
NOP			FF	–	–	–	–	–	–

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	C	Z	S	V	D	H
OR dst, src dst←dst OR src	†	4[ ]	–	*	*	0	–	–
POP dst dst←@SP; SP←SP + 1	R IR	50 51	–	–	–	–	–	–
PUSH src SP←SP – 1; @SP←src	R IR	70 71	–	–	–	–	–	–
RCF C←0		CF	0	–	–	–	–	–
RET PC←@SP; SP←SP + 2		AF	–	–	–	–	–	–
RL dst 	R IR	90 91	*	*	*	*	–	–
RLC dst 	R IR	10 11	*	*	*	*	–	–
RR dst 	R IR	E0 E1	*	*	*	*	–	–
RRC dst 	R IR	C0 C1	*	*	*	*	–	–
SBC dst, src dst←dst–src–C	†	3[ ]	*	*	*	*	1	*
SCF C←1		DF	1	–	–	–	–	–
SRA dst 	R IR	D0 D1	*	*	*	0	–	–
SRP dst RP←src	Im	31	–	–	–	–	–	–
STOP		6F	1	–	–	–	–	–
SUB dst, src dst←dst–src	†	2[ ]	*	*	*	*	1	*
SWAP dst 	R IR	F0 F1	X	*	*	X	–	–
TCM dst, src (NOT dst) AND src	†	6[ ]	–	*	*	0	–	–
TM dst, src dst AND src	†	7[ ]	–	*	*	0	–	–
XOR dst, src ds←dst XOR src	†	B[ ]	–	*	*	0	–	–
WDT		5F	–	X	X	X	–	–

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

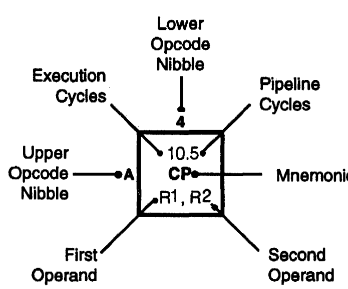
Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

10

OPCODE MAP

Lower Nibble (Hex) across; Upper Nibble (Hex) down.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2					↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1					↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



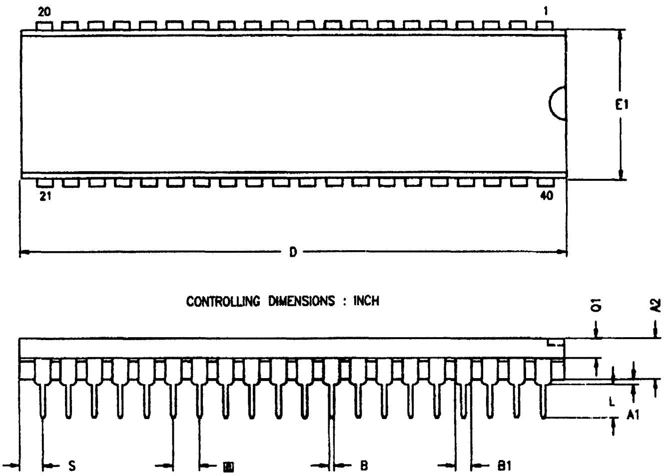
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

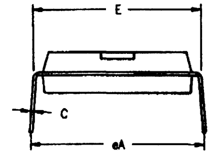
Sequence:
Opcode, First Operand, Second Operand

Note: Blanks are reserved.

*2-byte instruction appears as a 3-byte instruction

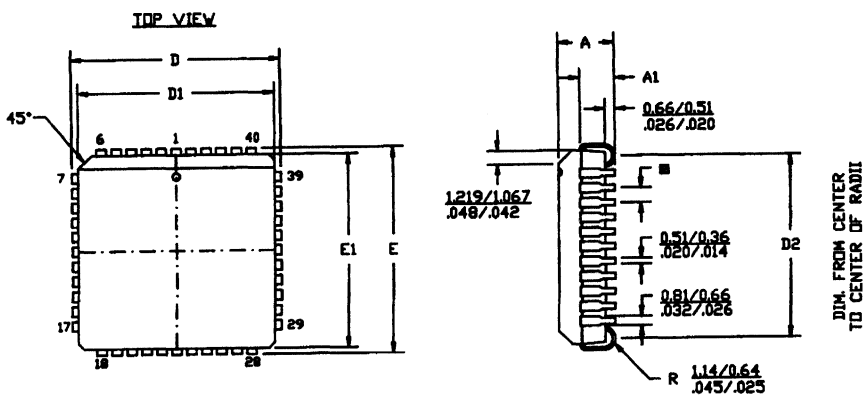
PACKAGE INFORMATION





SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
▣	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

40-Pin DIP Package Diagram



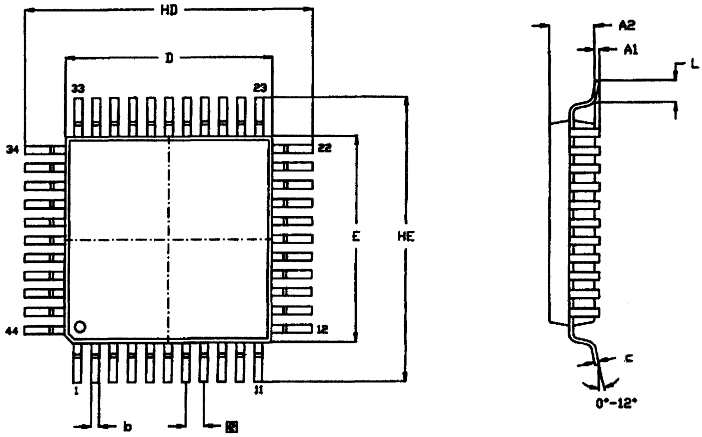
NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
▣	1.27 TYP		.050 TYP	

44-Pin PLCC Package Diagram

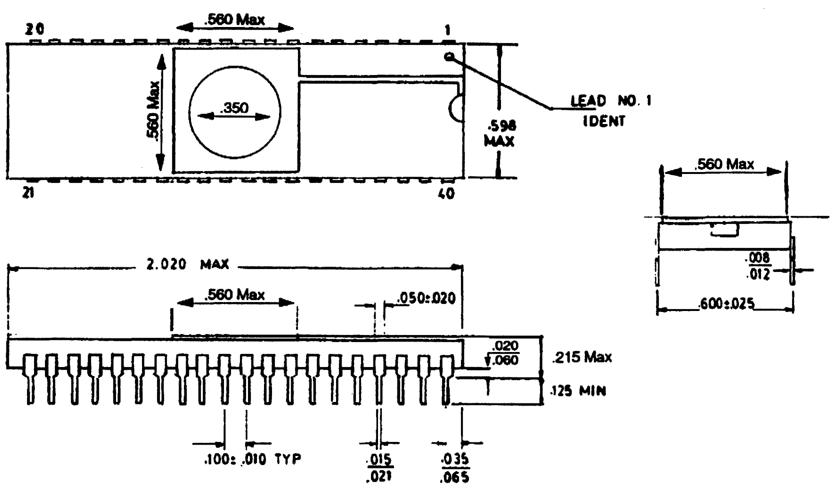
PACKAGE INFORMATION (Continued)



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm / .004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram



40-Pin Cerdip Window Lid Package Diagram

ORDERING INFORMATION

Z86E40 (12 MHz)

40-Pin DIP	40-Pin PLCC	44-Pin QFP	40-Pin Cerdip Window Lid
Z86E4012PSC	Z86E4012VSC	Z86E4012FSC	Z86E4012KSE

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Preferred Package
P = Plastic DIP
V = Plastic Chip Carrier

Longer Lead Time
F = Plastic Quad Flat Pack
K = Cerdip Window Lid

Temperature
S = 0°C to +70°C

Speed
12 = 12 MHz

Environmental
C= Plastic Standard
E = Hermetic Standard

Example:

Z 86E40 12 P S C is a Z86E40, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 12 — Speed
- 86E40 — Product Number
- Z — Zilog Prefix

Z86E30/E31 CMOS Z8® OTP CCP™
Consumer Controller Processor

8

Z86C40 CMOS Z8® 4K ROM CCP™
Consumer Controller Processor

9

Z86E40 CMOS Z8® 8-Bit OTP CCP™
Consumer Controller Processor

10

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Representatives & Distributors

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TIMEKEEPING WITH THE Z8®

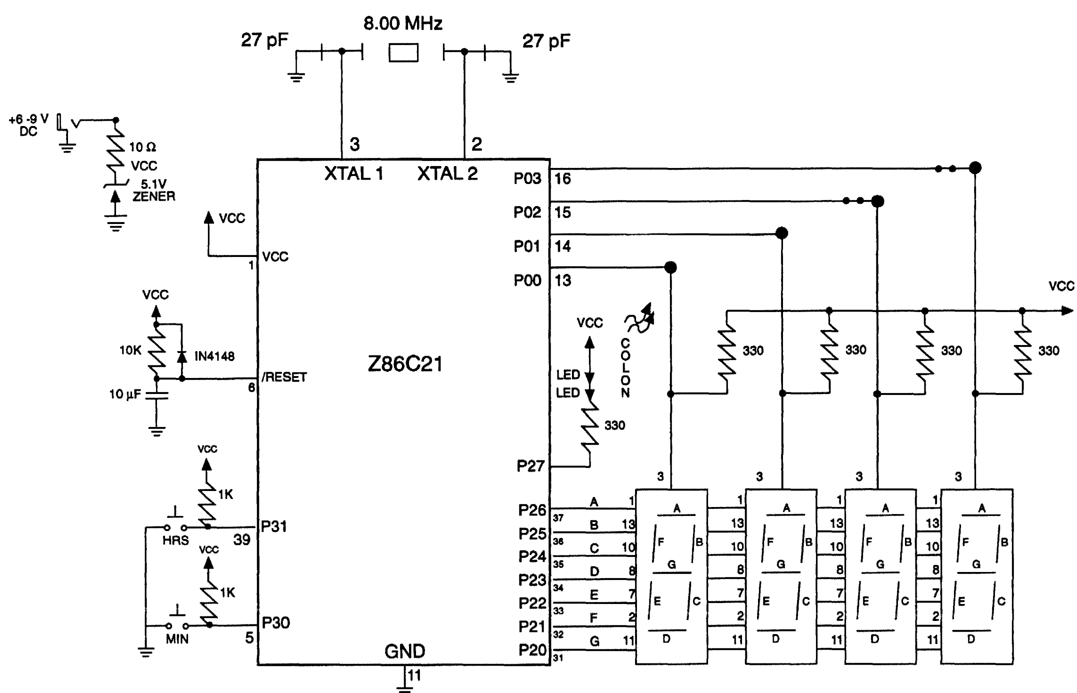
Keep track of the current time with the Z8®, using minimal hardware. This Application Note describes several software-based methods of timekeeping, with complete code listings.

INTRODUCTION

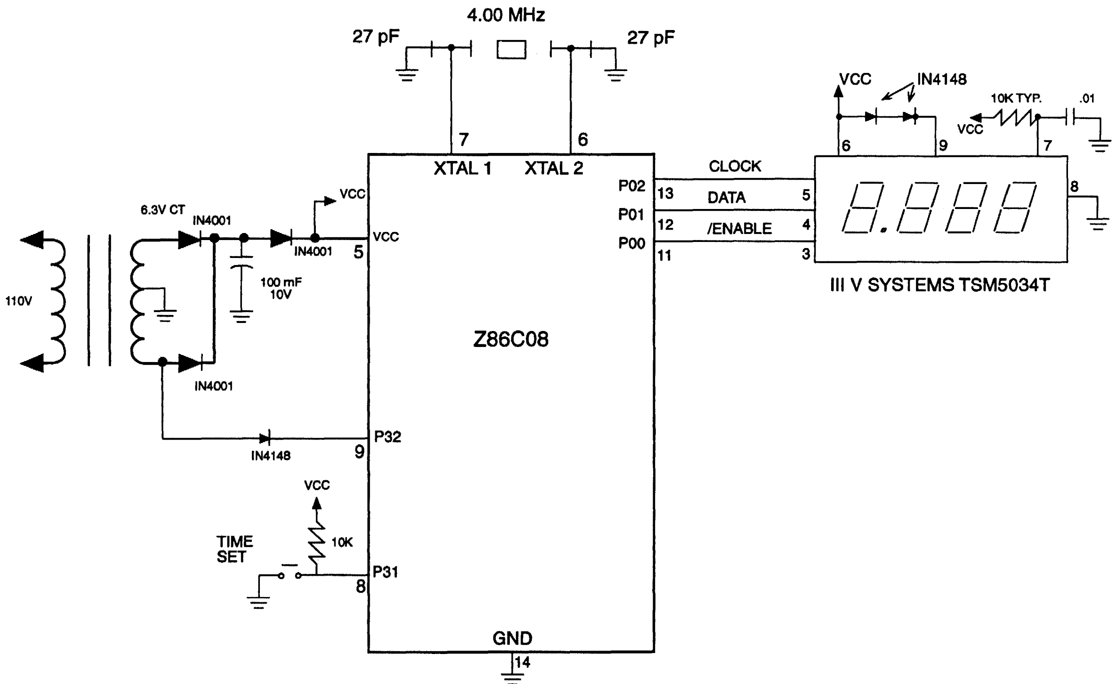
Many controller applications require ongoing tracking of the current time — at a specific time, for instance, the controller may have to take a specific action, like turning on a solenoid. This is accomplished by using a Real Time Clock, or RTC, the sole purpose of which is to keep track of time. A microprocessor-based system may use a RTC integrated circuit for timekeeping, or accomplish the same results through software, using the microprocessor's internal clock as a timebase. There are trade-offs associated with each approach, but the software method is by far the most economical, provided the micro can handle the added software overhead.

This Application Note covers two methods of timekeeping in software, with display of the current time on seven-segment LEDS. Time set switches are provided to advance the time. One method uses the microprocessor crystal as a timebase, while the other uses the highly-accurate 60 Hz line frequency as the timebase.

TIMEKEEPING BASED ON THE 8 MHZ CRYSTAL



TIMEKEEPING BASED ON THE 60 HZ LINE FREQUENCY



TIMEKEEPING BASED ON THE 8 MHZ CRYSTAL

```
;------------------------------------------------------------------------------
;       This program configures the Zilog Z8 to keep time using the 12.00 MHz
; crystal frequency as a timebase. The time is displayed on four (4) seven-
; segment, common-anode LEDs. The cathodes of the displays are driven by P2.
; The anodes of the displays are connected to P0, and a pull-up resistor. The
; colon, made up of two discrete LEDs, flashes at a 1 Hz rate, and is driven by
; P2-7. The set switches are connected to P3. This program may be adapted to
; any 28-pin or 40-pin Z8. Written by Don Owen Newquist, Zilog, on 5-1-91.
;------------------------------------------------------------------------------
WORK_REG        .equ    10h
address_hi      .equ    r0
address_lo      .equ    r1
address         .equ    rr0
pointer         .equ    r2
data            .equ    r3
col_count       .equ    r4
ring_counter    .equ    r5
HALF_SECOND     .equ    16h

TIME_REG        .equ    00h
millisec        .equ    r5
seconds         .equ    r6
minutes         .equ    r7
hours           .equ    r8
seconds_lo      .equ    r9
seconds_hi      .equ    r10
minutes_lo      .equ    r11
minutes_hi      .equ    r12
hours_lo        .equ    r13
hours_hi        .equ    r14
sw_count        .equ    r15
STATUS          .equ    %04
MILLISEC        .equ    %05
SECONDS         .equ    %06
MINUTES         .equ    %07
HOURS           .equ    %08
SECONDS_LO      .equ    %09
SECONDS_HI      .equ    %0a
MINUTES_LO      .equ    %0b
MINUTES_HI      .equ    %0c
HOURS_LO        .equ    %0d
HOURS_HI        .equ    %0e

                .org    00
                .word   00
                .word   00
                .word   00
                .word   00
                .word   time
                .word   load_time
                .org    000ch
```

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```
;****************************************************************************;
;                  Initialization                                            ;
;****************************************************************************;
init:           srp     #WORK_REG
                di                              ; disable int
                ld      t0,#250                 ; 250 decimal
                ld      pre0,#01010001b         ; set t0 for 5 mS period
                ld      pre1,#%13               ;
                ld      t1,#00                  ; set for .250 mS refresh
                ld      p2m,#0                  ; outputs on p2
                ld      p3m,#0                  ; open drain on p2
                ld      p01m,#04                ; outputs on p0, int stack
                clr     p0                      ; p0 low
                clr     p3                      ; p3 low
                clr     sw_count                ; sw count = 0
                clr     STATUS                  ; clear status reg
                clr     HALF_SECOND             ;
                ld      ipr,#00001000b          ; make irq5 > irq3
                ld      imr,#%30                ; enable irq4,irq5
                ld      spl,#%80                ; set stack pointer
                clr     sph                     ;
                ld      tmr,#%0f                ; load and enable counters
                ld      pointer,#04             ; point to time regs
                ld      r15,#12                 ; six locations
clear_reg:      clr     @pointer                ; clear ram
                inc     pointer                 ;
                djnz    r15,clear_reg           ; continue until all zero
                ld      HOURS,#%12              ; start time at 12:00
                ld      pointer,#HOURS_HI       ; start at hours reg
                ld      ring_counter,#%88       ; enable first digit
main_loop:      ei                              ; enable interrupts
                jr      main_loop               ;
;****************************************************************************;
;               This routine converts the seconds, minutes, and hours bcd    ;
;               data into units and tens-of-units for displaying             ;
;****************************************************************************;
time_convert:   ld      SECONDS_LO,SECONDS      ; transfer contents
                ld      SECONDS_HI,SECONDS      ;
                and     SECONDS_LO,#%0f         ; keep only lower bits
                swap    SECONDS_HI              ; swap nibbles
                and     SECONDS_HI,#%0f         ; keep only lower bits
                ld      MINUTES_LO,MINUTES      ; transfer contents
                ld      MINUTES_HI,MINUTES      ;
                and     MINUTES_LO,#%0f         ; keep only lower bits
                swap    MINUTES_HI              ; swap nibbles
                and     MINUTES_HI,#%0f         ; keep only lower bits
                ld      HOURS_LO,HOURS          ; transfer contents
                ld      HOURS_HI,HOURS          ;
                and     HOURS_LO,#%0f           ; keep only lower bits
                swap    HOURS_HI                ;
                and     HOURS_HI,#%0f           ; keep only lower bits
                ret                             ; return
```

```
;*****************************************************************************;
;               This interrupt routine updates the time                       ;
;*****************************************************************************;
time:           push    rp                      ; save current reg pointer
                srp     #TIME_REG               ; point to time reg group
                call    test_sw                 ; look at time-set switches
                inc     millisec                ; increment millisec reg
                cp      millisec,#100           ; half second?
                jr      ult,exit_time           ; don't toggle colon
                tm      STATUS,#00000001b       ; sw 1 pressed?
                jr      z,test_sw2              ; no
                add     MINUTES,#1              ;
                da      MINUTES                 ; convert to bcd
                cp      MINUTES,#%60            ; sixty minutes?
                jr      ult,inc_half_sec        ;
                clr     MINUTES                 ;
                jr      inc_half_sec            ;
test_sw2:       tm      STATUS,#00000010b       ; sw 2 pressed?
                jr      z,inc_half_sec          ; no
                add     HOURS,#1                ;
                da      HOURS                   ;
                cp      HOURS,#%13              ; 1:00?
                jr      ult,inc_half_sec        ;
                ld      HOURS,#1                ;
inc_half_sec:   inc     HALF_SECOND             ;
                clr     millisec                ;
                xor     p2,#%80                 ; toggle colon bit now
one_second:     cp      HALF_SECOND,#2          ; one second?
                jp      ult,exit_time           ; exit if not
                clr     HALF_SECOND             ; set to zero
inc_seconds:    add     seconds,#1              ; increment sec
                da      seconds                 ; convert to bcd
                cp      seconds,#%60            ; sixty seconds?
                jr      ult,exit_time           ; no
                clr     seconds                 ; set to zero
                add     minutes,#1              ; inc minutes
                da      minutes                 ; convert to bcd
                cp      minutes,#%60            ; sixty minutes?
                jr      ult,exit_time           ; not yet
                clr     minutes                 ; set to zero
set_hrs:        add     hours,#1                ; inc hours
                da      hours                   ; convert to bcd
                cp      hours,#%13              ; 1:00?
                jr      ult,exit_time           ; exit
                ld      hours,#1                ; set to 1:00
exit_time:      call    time_convert            ; convert to individual bcd
                pop     rp                      ; return to orig reg pointer
                iret                            ; return from int
```

```
;*****************************************************************************;
;      This subroutine checks to see if the time-set switches are pressed.    ;
;*****************************************************************************;
test_sw:        push    rp                  ;
                srp     #WORK_REG           ;
                ld      data,p3             ; get switch data
                com     data                ; invert data
                and     data,#%03           ; only first two bits
                cp      data,#0             ;
                jr      eq,clear_sw         ;
                tm      data,#1             ; min pressed?
                jr      z,test_hrs          ; no
                inc     sw_count            ; inc counter
                cp      sw_count,#2         ; debouncd?
                jr      ult,exit_sw         ; not yet
                or      STATUS,#00000001b   ; set bit
                jr      exit_sw             ; exit
test_hrs:       tm      data,#2             ; hrs pressed?
                jr      z,clear_sw          ; no
                inc     sw_count            ; inc debounce counter
                cp      sw_count,#2         ; debounced?
                jr      ult,exit_sw         ; not yet
                or      STATUS,#00000010b   ; set bit
exit_sw:        pop     rp                  ;
                ret                         ; return to caller
clear_sw:       clr     STATUS              ; reset sw status bits
                clr     sw_count            ; reset debounce counter
                pop     rp                  ;
                ret                         ; return
;*****************************************************************************;
;          This subroutine loads the time data into the RAM buffer            ;
;*****************************************************************************;
load_time:      push    rp                  ; save current reg pointer
                srp     #WORK_REG           ; point to working reg
load_table:     ld      r12,@pointer        ; load contents
                ld      address_hi,#^hb led_table; load hi address of table
                ld      address_lo,#^lb led_table; load lo address of table
                cp      r12,#0              ; is it zero?
                jr      eq,no_index         ; if yes, don't step thru table
index_num:      incw    address             ; step thru table
                djnz    r12,index_num       ; index if not zero
no_index:       lde     data,@address       ; load segments
                and     p2,#%80             ;
                or      p2,data             ; load port 2 with segments
                ld      p3,ring_counter     ; turn on digit
                dec     pointer             ; inc reg location
                cp      pointer,#SECONDS_HI ; at ending reg?
                jr      ugt,load_time_ret   ; exit
                ld      pointer,#HOURS_HI   ; start at beginning
                cp      @pointer,#0         ;
                jr      ne,load_time_ret    ;
                dec     pointer             ; don't display leading zero
                rr      ring_counter        ;
load_time_ret:  rr      ring_counter        ; rotate counter
                pop     rp                  ; return to time regs
                iret                        ; return from interrupt
```

```
led_table:
                .byte   00111111B       ; ZERO
                .byte   00000110B       ; ONE
                .byte   01011011B       ; TWO
                .byte   01001111B       ; THREE
                .byte   01100110B       ; FOUR
                .byte   01101101B       ; FIVE
                .byte   01111101B       ; SIX
                .byte   00000111B       ; SEVEN
                .byte   01111111B       ; EIGHT
                .byte   01100111B       ; NINE

                .end
```

TIMEKEEPING BASED ON THE 60 HZ LINE FREQUENCY

```
;---------------------------------------------------------------------------
;   This clock routine uses the Zilog Z86E08 to keep time. The 60 Hz line
; frequency causes an interrupt to the CPU every half cycle using one of the
; on-board comparators. The time registers are then incremented, and the dis-
; play refreshed at 1/ 60 second intervals. The time is displayed on a Three-
; Five Systems TSM6X34 Four Digit Display. The display has serial data and
; clock inputs, along with on-board display drivers. Port P0 provides the
; clock, data, and reset lines for the display. Port P2 is available for
; user options. The time set switch is connected to the second comparator
; input, and when pressed, advances the time at a 60 Hz rate.
;   This program was written by Don Owen Newquist on May 16, 1992.
;---------------------------------------------------------------------------
TIME_REG        .equ    10h
counter         .equ    r0
bit_count       .equ    r1
address_hi      .equ    r4
address_lo      .equ    r5
address         .equ    rr4
pointer         .equ    r6
data            .equ    r7
milliseconds    .equ    r8
seconds         .equ    r9
minutes         .equ    r10
hours           .equ    r11
minutes_lo      .equ    r12
minutes_hi      .equ    r13
hours_lo        .equ    r14
hours_hi        .equ    r15

BUFFER          .equ    04h
START           .EQU    02
ENABLE_HI       .EQU    01
ONE             .EQU    02
ZERO            .EQU    %FD
CLOCK_HI        .EQU    04
CLOCK_LO        .EQU    %FB

                .org    00
                .word   00
                .word   00
                .word   00
                .word   time
                .word   00
                .word   00
                .org    000ch
```

```
;***************************************************************************
;               Initialization                                             *
;***************************************************************************
init:           srp     #TIME_REG
                di                                  ; disable int
                ld      p2m,#0                      ; outputs on p2
                ld      p3m,#0                      ; open drain on p2
                ld      p01m,#04                    ; outputs on p0, int stack
                clr     p0                          ; p0 low
                clr     p3                          ; p3 low
                clr     irq                         ;
                ld      imr,#%08                    ; enable irq3
                ld      spl,#%80                    ; set stack pointer
                clr     sph                         ;
                ld      pointer,#18h                ; point to time regs
                ld      counter,#6                  ; six locations
clear_reg:      clr     @pointer                    ; clear ram
                inc     pointer                     ;
                djnz    counter,clear_reg           ; continue until all zero
                ld      hours,#%12                  ; start time at 12:00
                ld      pointer,#minutes_lo         ; start at minutes reg
                call    time_convert                ;
                call    load_time                   ;
main_loop:      ei                                  ; enable interrupts
                jr      main_loop                   ;
;***************************************************************************
;          This interrupt routine updates the time                         *
;***************************************************************************
time:           tm      p3,#2                       ; sw pressed?
                jr      nz,inc_minutes              ; no
                inc     milliseconds                ;
                cp      milliseconds,#60            ; one second yet?
                jr      ult,exit_time               ;
                clr     milliseconds                ;
                inc     seconds                     ;
                cp      seconds,#60                 ;
                jr      ult,exit_time               ;
                clr     seconds                     ;
inc_minutes:    add     minutes,#1                  ; inc minutes
                da      minutes                     ; convert to bcd
                cp      minutes,#%60                ; sixty minutes?
                jr      ult,exit_time               ; not yet
                clr     minutes                     ; set to zero
set_hrs:        add     hours,#1                    ; inc hours
                da      hours                       ; convert to bcd
                cp      hours,#%13                  ; 1:00?
                jr      ult,exit_time               ; exit
                ld      hours,#1                    ; set to 1:00
exit_time:      call    time_convert                ; convert to individual bcd
                call    load_time                   ;
                iret                                ; return from int
```

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```
;*************************************************************************;
;              This routine converts the seconds, minutes, and hours bcd    ;
;              data into units and tens-of-units for displaying             ;
;*************************************************************************;
time_convert:  ld      minutes_lo,minutes       ; transfer contents
               ld      minutes_hi,minutes       ;
               and     minutes_lo,#%0f          ; keep only lower bits
               swap    minutes_hi               ; swap nibbles
               and     minutes_hi,#%0f          ; keep only lower bits
               ld      hours_lo,hours           ; transfer contents
               ld      hours_hi,hours           ;
               and     hours_lo,#%0f            ; keep only lower bits
               swap    hours_hi                 ;
               and     hours_hi,#%0f            ; keep only lower bits
               ret                              ; return

;**************************************************************************;
; This subroutine loads the time data into the RAM buffer,then to the display ;
;**************************************************************************;

load_time:     ld      pointer,#minutes_lo      ; load contents
               ld      BUFFER,#04               ; load buffer add
               ld      counter,#4               ;
               ld      address_hi,#^hb led_table; load hi address of table
load_table:    ld      address_lo,#^lb led_table; load lo address of table
               ld      data,@pointer            ;
               add     address_lo,data          ;
no_index:      ldc     data,@address            ; load segments
               ld      @BUFFER,data             ;
               inc     pointer                  ;
               inc     BUFFER                   ;
               djnz    counter,load_table       ;
               ld      BUFFER,#4                ;
               ld      counter,#3               ;
               ld      p0,#START                ; clock & enable low, data hi
send_start:    call    clock_out                ; clock the data
               djnz    counter,send_start       ;
               ld      counter,#4               ;
next_digit:    ld      bit_count,#8             ;
               ld      data,@BUFFER             ;
rotate:        rcf                              ;
               rrc     data                     ;
               jr      nc,zero                  ;
               or      p0,#ONE                  ;
               jr      clock_it                 ;
zero:          and     p0,#ZERO                 ;
clock_it:      call    clock_out                ;
               djnz    bit_count,rotate         ;
               inc     BUFFER                   ;
               djnz    counter,next_digit       ;
               call    clock_out                ; one more to load data
               ld      p0,#ENABLE_HI            ; take enable line high
               ret
```

```
;------------------------------------------------------------------------------
;                Clock Out LED Data
;------------------------------------------------------------------------------
clock_out:       or       p0,#CLOCK_HI            ; set hi
                 nop                              ; delay
                 nop                              ; delay
                 nop                              ; delay
                 and      p0,#CLOCK_LO            ; take clock lo
                 nop                              ;
                 nop                              ;
                 nop                              ;
                 ret                              ; return from interrupt

                 .org     %00f0
led_table:
                 .byte    00111111B               ; ZERO
                 .byte    00000110B               ; ONE
                 .byte    01011011B               ; TWO
                 .byte    01001111B               ; THREE
                 .byte    01100110B               ; FOUR
                 .byte    01101101B               ; FIVE
                 .byte    01111101B               ; SIX
                 .byte    00000111B               ; SEVEN
                 .byte    01111111B               ; EIGHT
                 .byte    01100111B               ; NINE

                 .end
```

SINE TABLE

```
05 ' Listing 1
10 '------------------------------------------------------------
20 '              *** SIN-TAB.BAS ***
30 '
40 '  Purpose= to generate a complete sine table
50 '  of hex numbers in format... [TAB].byte[TAB]01h,02h,...,0Ch
60 '------------------------------------------------------------
70 '
80 ON ERROR GOTO 590
90 DIM B$(256)
100 DIM C$(22)
110 DEFINT A,B
120 PI = 3.141593
130 C=360/256
140 GOTO 390
150 FOR I=0 TO 255
160 H=B+A*SIN((C*I*PI)/180)
170 A$=HEX$(H)                  'HEX$ function rounds off H autom'ly
180 IF LEN(A$)>2 THEN PRINT "--Bad data: some bytes bigger than FFh":GOTO 430
190 IF LEN(A$)=1 THEN A$="0"+A$         'ADD LEADING ZERO, IF NECESS.
200 B$(I+1)=A$+"h"
210 NEXT I
220 I=1
230 FOR J=1 TO 22
240 C$(J)=CHR$(9)+".byte"+CHR$(9)       'START W/[TAB].byte[TAB]
250 FOR K=1 TO 12
260 C$(J)=C$(J)+B$(I)+","
270 I=I+1:IF I>256 GOTO 290
280 NEXT K
290 L=LEN(C$(J))-1
300 C$(J)=LEFT$(C$(J),L)                'KILL LAST COMMA
310 NEXT J
320 OPEN "TABLE.ASC" FOR OUTPUT AS #1
330 FOR J=1 TO 22:PRINT #1,C$(J):NEXT J
340 CLOSE #1
350 BEEP:PRINT:PRINT "SINE DATA STORED IN CURRENT DRIVE & DIRECTORY"
360 PRINT "IN ASCII FILE CALLED    TABLE.ASC  ":PRINT
370 PRINT "   ( Press any key )"
380 T$=INKEY$:IF T$="" THEN 380 ELSE SYSTEM
390 CLS:LOCATE 10,35:PRINT "* SIN-TAB *":PRINT
400 PRINT TAB(10);"Generates a 256-byte sine table in the current"
410 PRINT TAB(10);"directory by creating an ASCII file called: TABLE.ASC"
420 PRINT TAB(10);"(If the file already exists, it will be overwritten !!!)"
430 PRINT TAB(10);"Sine wave is of the form:  A sin(xt) where A= amplitude."
440 PRINT TAB(10);"What is amplitude ? (range= 1 - 127)  A= ";
450 LINE INPUT T$
460 A=VAL(T$):IF A<1 OR A>127 THEN GOTO 430
470 PRINT TAB(10);"An offset is needed to keep all values positive."
480 PRINT TAB(15);"Suggest:";A+1
490 PRINT TAB(20);"Is this okay ? (Y/N)"
```

```
500 T$=INKEY$:IF T$="" GOTO 500
510 IF T$=CHR$(27) THEN SYSTEM
520 IF T$="Y" OR T$="y" THEN B=A+1:PRINT "WAIT...":GOTO 150
530 IF T$="N" OR T$="n" THEN 540 ELSE 500
540 PRINT TAB(10);"Enter new value (0-255): ";
550 LINE INPUT T$
560 B=VAL(T$):IF B<0 OR B>255 THEN PRINT "--Illegal value--":GOTO 470
570 PRINT "WAIT...":GOTO 150
580 '         *** ERROR TRAP ***
590 IF ERL<>320 GOTO 630
600 BEEP:PRINT:PRINT "Unable to create (or write to) file: TABLE.ASC"
610 PRINT "    ( Press any key )"
620 RESUME 380
630 IF ERL=460 THEN PRINT "--Illegal value--":PRINT:RESUME 440
640 IF ERL=560 THEN PRINT "--Illegal value--":PRINT:RESUME 470
650 BEEP:PRINT:PRINT "*** ERROR ";ERR;" OCCURRED AT LINE";ERL:PRINT
660 PRINT "    ( Press any key )"
670 RESUME 380
```

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Notes:

USING THE ZILOG Z86C06 SPI BUS

The SPI stuffs a lot of power into a small package. Utilized in either Master or Slave mode with the ability to talk to many different processors and work with a wide range of peripherals, it fits readily into the low cost/high performance bracket.

INTRODUCTION

The Zilog Z86C06 SPI (Serial Peripheral Interface) is a compact, powerful and cost effective microcontroller. Its small form factor (18 pins) does not limit the full power of the Z8 core. The Z86C06 provides 1K (on-board) of program memory, 124 general purpose registers and an SPI bus that can be used in master or slave mode. This combines to overcome any pin I/O limitations and unleash the full Z8 capabilities.

Zilog's Superintegration™ also reduces system cost because two analog comparators are provided. No external interrupt reset circuitry is required because an interrupt Power-On-Reset along with Low Voltage (brownout) protection has been incorporated internally. A crystal may be optionally bypassed because the part is capable of using an RC or LC clocking source. It is also ideal for battery applications because the part can be placed in SLEEP mode and draw less than 10 microamps (2 microamps typical) of supply current. The user has a number of options available both internal and external, to recover from SLEEP mode by using the Stop Mode Recovery Register.

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SPI BUS OPERATION

The SPI bus is useful because many peripherals exist to directly support it. Among these are E^2 Serial PROMS, Real Time Clock chips, A/D converters, Frequency Generators, and display drivers for LED, LCD and VF displays. The other facet of the SPI bus that makes it useful is its ability to communicate with other processors. This is a requirement for distributed processing systems. SPI communications between processors is done in a Master/Slave type of arrangement.

In order to understand how the SPI bus is utilized to communicate with some of the peripherals mentioned, the architecture of the SPI bus itself must first be understood. In the simplest application, the SPI bus consists of three lines: a serial clock line, a serial in line, and a serial out line. Most peripherals also require a /CS line so that multiple peripherals can be utilized on the bus. A simplified diagram is shown in Figure 1.

SPI BUS OPERATION (Continued)

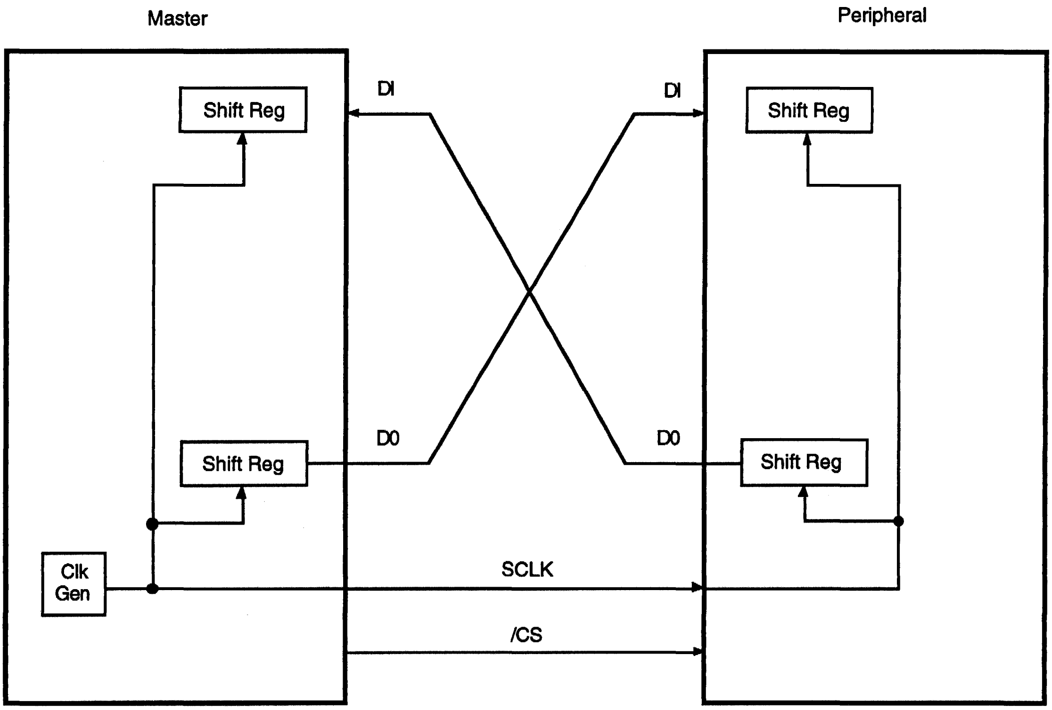

Figure 1. Simplified SPI Bus Configuration

The serial clock (SCLK) line synchronizes the transfer of data between the master and the peripheral or slave device. SCLK is generated and controlled by the master device. Typically, the serial data output is transmitted on the falling edge of SCLK and the receive data is captured on the rising edge of SCLK. The Z8 has the capability of altering this relationship by manipulating bit D5 of the SCON register. When the data is transmitted, the most significant bit is transmitted first.

Control of the SPI bus in the Z8 is done in the SCON register (location (C) 02 in the expanded register file). There are also two other SPI bus registers in the Z8 which are necessary; the TX/RCV buffer and the SPI compare register. A diagram of the bit manipulation of the SPI Control Register is given in Figure 2. The Master/Slave mode is controlled by bit D7 in the SCON register. In the master mode, the definition of the bits is defined as follows:

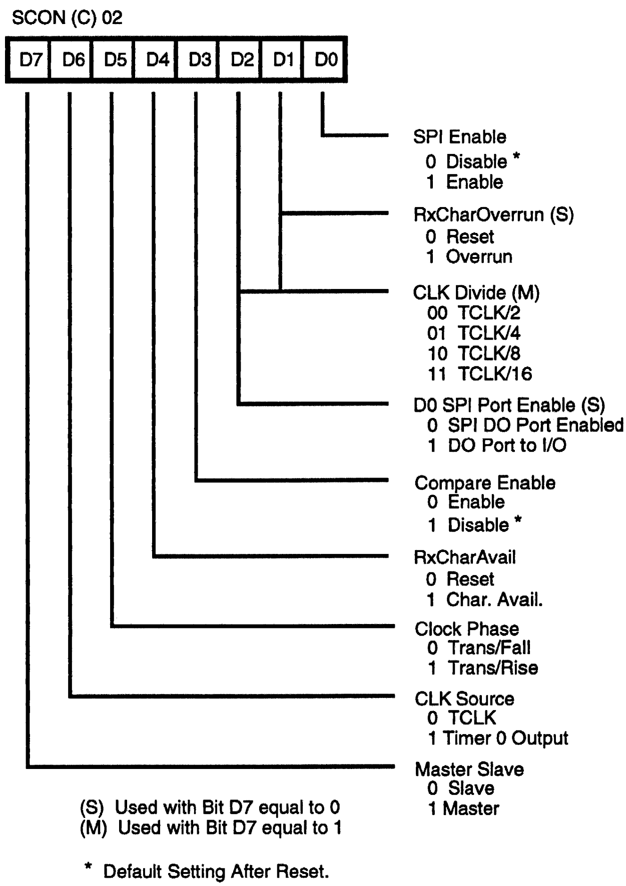

Figure 2. SPI Control Register (SCON)

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Master Mode

D7 - Master/Slave Select: Programmed as a 1 to select master mode.

D6 - CLK Source Select: This is used to select the SCLK source for SPI bus. A 1 selects the T0 output as the control clocking source; a 0 selects the internal clock (XTAL/2). If the internal clock is selected, the actual clocking source is modified according to bits D2 and D1.

D5 - Clock Phase: This bit controls the phase relationship of the latching of the receive data and the transmitted data. A 1 transmits data on the rising edge of SCLK and latches the receive data on the falling edge. A 0 performs the opposite.

D4 - Rx Character Available: This bit can be used to determine if the receive data buffer is full. If activated, this also activates IRQ3.

D3 - Compare Enable: This bit has no effect in Master Mode.

D2,D1 - Clock Divide: If the SCLK source in bit D6 was programmed as a 0, then these bits control how the internal clock is manipulated to generate the SCLK. In the non-low noise mode, the SCLK can be programmed to be 1/4, 1/8, 1/16, or 1/32 of the external XTAL1 frequency. Note that PCLK is 1/2 of the XTAL1 frequency when the part is not operating in low noise mode. TCLK is equal to the XTAL1 frequency if low noise mode is selected (bit D7 of the PCON register).

D0 - SPI Enable: This bit controls the activation of the SPI bus. When the SPI bus is enabled, the SPI signals get mapped according to Table 1.

Table 1. SPI Pin Configuration

Name	Function	Port Location
DI	Data In	P20
DO	Data Out	P27
SS	Slave Select	P35
SLCKS	PI Clock	P34

Slave Mode

In slave mode these same bits change their function and are defined as follows:

D7 - Master/Slave Select: Programmed as a 0 to select slave mode. No slave mode transactions are initiated unless the Slave Select input is active low.

D6 - CLK Source Select: This has no effect in slave mode since the SCLK is controlled by the SPI Master.

D5 - Clock Phase: This bit controls the phase relationship of the latching of the receive data and the transmitted data described above.

D4 - Rx Character Available: Same as above.

D3 - Compare Enable: This bit can be used to enable a stop mode recovery source. When the processor is in SLEEP mode, and a character has been transferred into the receive buffer, and if it matches the SPI compare register, then the controller recovers from stop mode.

D2 - DO SPI Port Enable: When the slave mode is active, this bit controls the activation of the Data-out signal. If a 1 is written in this location, then P27 is controlled by the P2M register and P2. A 0 enables data to be shifted out with the SCLK.

D1 - Rx Character Overrun: When a 1 is read in this location, then the receive buffer has been overrun. This condition must be reset by writing a 1 to this bit.

D0 - SPI Enable: Same as Master Mode.

Compare Mode

Another special mode, commonly used in high end communication devices, is the SPI's internal Compare/Wakeup mode (Figure 3). This mode, commonly known in communications terminology as "wake up," is a compare register and logic which monitors the received data when in the low power SLEEP modes. If a "match" occurs between the compare register and the received data, the Z86C06 "wakes up" and processes according to the programmed, "waking up" state or condition.

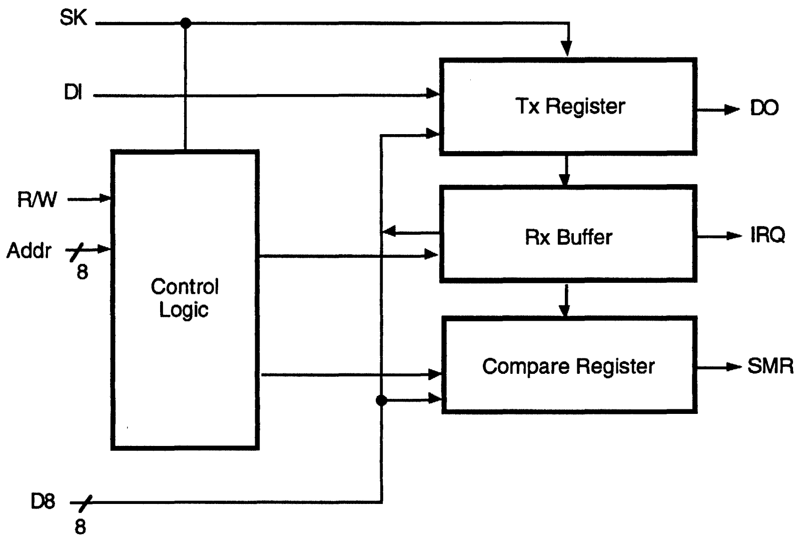


Figure 3. SPI Internal Compare/Wakeup Mode

CONNECTING THE Z8 SPI BUS TO THE XICOR X25C02 SPI E2PROM

One of the most popular peripherals for microcontrollers is the serial E²PROM. Economics is the obvious reason for this. It costs significantly less to add a serial E²PROM to a microcontroller than to purchase a microcontroller with embedded E² capability.

Connecting SPI peripherals to the Z8 is an easy task. An example of this is demonstrated by connecting the Z86C06 to the XICOR X25C02 (Figure 4). Note that the X25C02 is in the standby mode, the standby current is specified to be less than 150 microamps. The sleep mode current of the Z8 is less than 10 microamps (2 microamps typical). Since the active current of the X25C02 is less than 2 milliamps, it may be advantageous to use a port pin to supply power to the serial E² part in order to minimize application sleep mode current.

An example of the source code required to interface the X25C02 to the Z86C06 is given in Appendix A (Listing 1). This example, given in the listing, exercises the X25C02 by writing to it and reading from it. The listing also has three general-purpose routines for SPI utilization; SPI_MASTER_INIT, SPI_ENABLE and SPI. They are used to initialize the bus as a master, enable the SPI bus, and write/read data from the SPI peripheral, respectively.

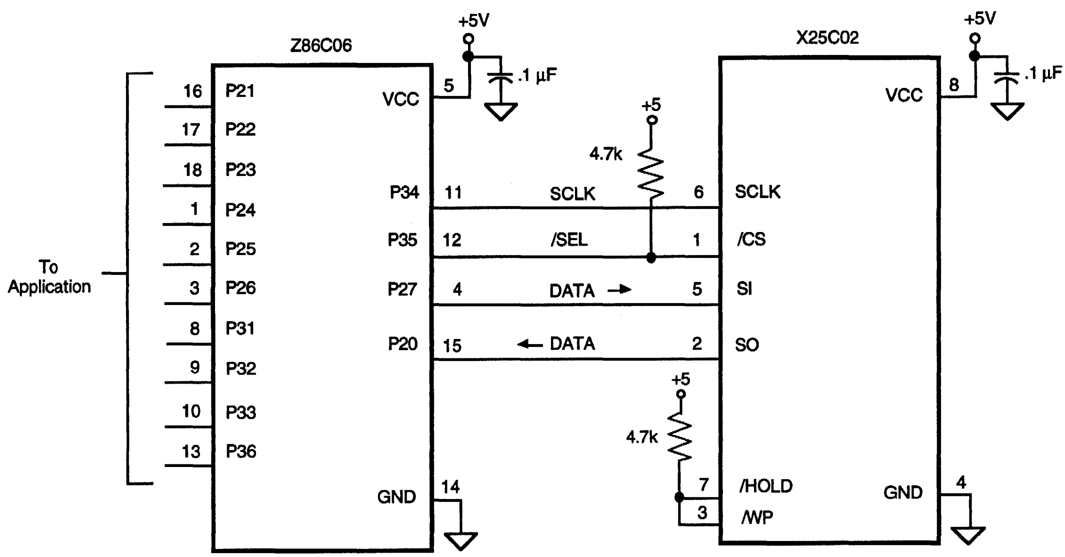


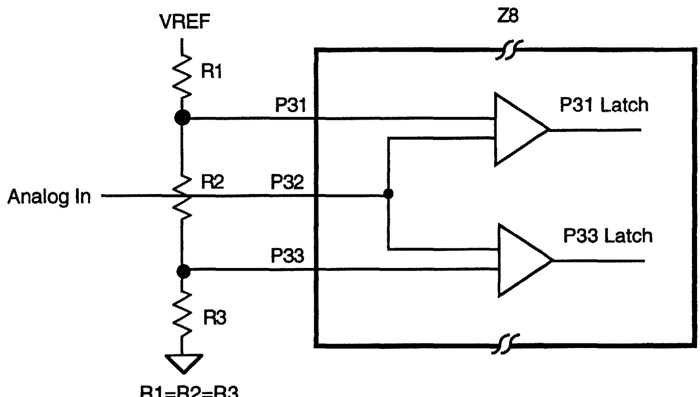
Figure 4. Z86C06 and XICOR X25C02 Application Interconnection

CONNECTING THE Z8 SPI BUS TO AN A/D CONVERTER

Port 3 of the Z86C06 includes two analog comparators (when the port is programmed to operate in the analog mode in the P3M register). In addition to using the internal comparators as general purpose comparators, they can also be configured and used as a 3-bit A/D (Figure 5).

If more resolution than three bits is required, there are two alternatives. First, use an output port pin to charge a capacitor, start a timer, discharge the capacitor, then use the timer and an analog comparator to calculate the input voltage. This method is shown in Figure 5. The required amount of resolution is achieved by adjusting R1 and C1 to provide a maximum time constant for the Z8 timers. The most common way to utilize this technique is to provide a precalculated lookup table based on the timer results.

While the method shown in Figure 6 is cost effective, it may not be accurate enough for some applications. When additional accuracy is required, it is possible to find A/D converters with SPI interfaces. One such part is a Motorola MC145053 that provides 10 bits of conversion resolution. The hardware interface for the Z86C06 and the MC145053 is shown in Figure 7. An example of the source code required to interface the MC145053 to the Z86C06 is given in Appendix B (Listing 2). The general purpose SPI routines used in the E² application are also used to interface to the MC145053.



P31	P33	Meaning
0	0	Analog In < 1/3 VREF
0	1	1/3 VREF< Analog In < 2/3 VREF
1	C	No Meaning (Invalid)
1	1	Analog In > 2/3 VREF

Figure 5. Three-Bit Analog/Digital Converter

CONNECTING THE Z8 SPI BUS TO AN A/D CONVERTER (Continued)

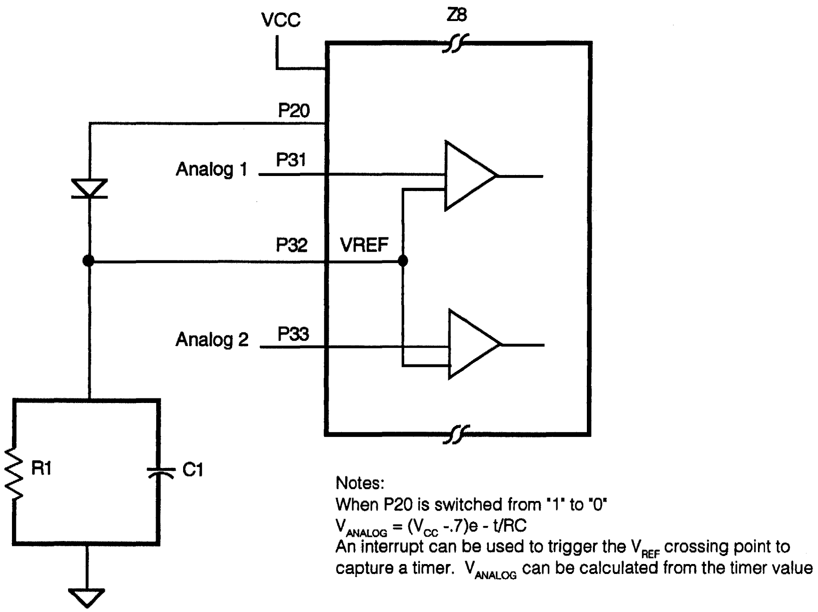


Figure 6. Low Cost Analog/Digital Converter

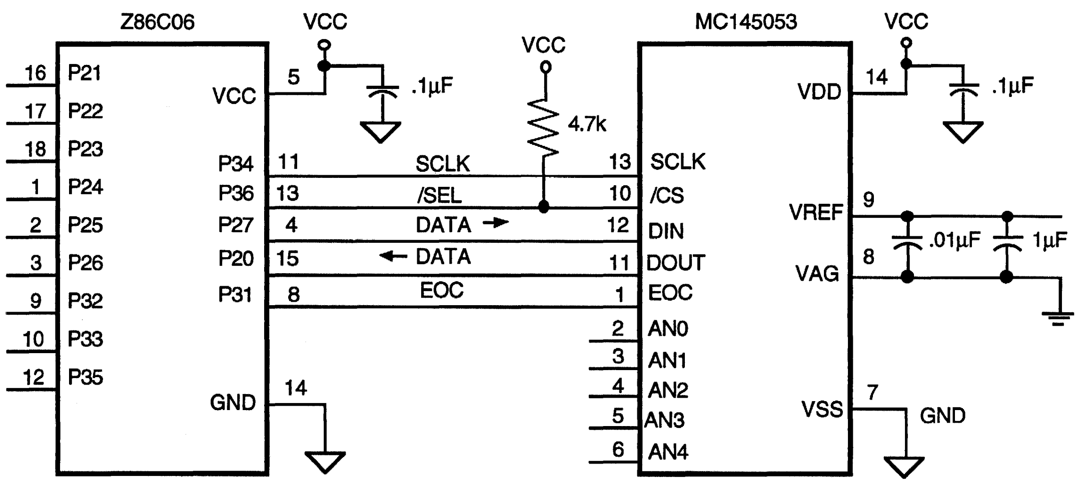


Figure 7. Z86C06/MC145053 Hardware Interface

CONCLUSION

The SPI bus is a simple, three-wire serial interface that can be used to communicate with a number of different specialized peripherals. While not discussed in detail in this App Note, it also lends itself as an excellent communications protocol controller in a distributed processing architecture. The Z86C06 is a very powerful and highly integrated processor that supports the SPI bus.

Control of the SPI bus is simple as demonstrated with each of the examples. Because control of the SPI bus is easy with the Z8, there is little hardware and software overhead required to use it. This also makes it an excellent cost-effective choice as a processor in a distributed processing environment even where an analog interface is involved.

APPENDIX A

Listing 1

```
LOC      OBJ             LINE# — SOURCE —
                          ;*****************************************************************************
                          ;                                                                            *
                          ;     ZILOG / SPI INTERFACE                                                  *
                          ;     Z86C06 AND X25C02                                                      *
                          ;                                                                            *
                          ;     BY: LYN ZASTROW                                                        *
                          ;     COPYWRITE 1991                                                         *
                          ;                                                                            *
                          ;     ASSEMBLER: ZILOG ASMS8 ASSEMBLER                                       *
                          ;                                                                            *
                          ;     Z86C06 I/O UTILIZATION                                                 *
                          ;     PORT DEFINITIONS:                                                      *
                          ;     P20:   SPI PROCESSOR INPUT DATA                                        *
                          ;     P21:   NOT USED                                                        *
                          ;     P22:   NOT USED                                                        *
                          ;     P23:   NOT USED                                                        *
                          ;     P24:   NOT USED                                                        *
                          ;     P25:   NOT USED                                                        *
                          ;     P26:   X25C02 POWER CONTROL                                            *
                          ;     P27:   SPI PROCESSOR OUTPUT DATA                                       *
                          ;     P31:   NOT USED                                                        *
                          ;     P32:   NOT USED                                                        *
                          ;     P33:   NOT USED                                                        *
                          ;     P34:   SCLK OUTPUT FROM PROCESSOR                                      *
                          ;     P35:   /CS OUTPUT FROM PROCESSOR                                       *
                          ;     P36:   NOT USED                                                        *
                          ;                                                                            *
                          ;    TIME CONSTANTS ARE BASED ON 8MHz OPERATIONAL FREQUENCY                  *
                          ;                                                                            *
                          ;*****************************************************************************
                          ;
                          ;
                          ;    ------------- REGISTER POINTER DECLARATIONS ----------------
                          ;
                          ;
                          ;    ------------------ REGISTER DECLARATIONS ------------------
   abs 00000000           TDATA    .EQU   R0      ;SAME AS XDATA, BUT WORKING REGISTER   (%10)
   abs 00000001           RXBUF    .EQU   R1      ;SPI RX & XMIT BUFFER                  (%11)
   abs 00000002           SCON     .EQU   R2      ;SPI CONTROL REGISTER (EXTENDED REG)   (%12)
   abs 00000004           MCHR     .EQU   R4      ;MULTIPLE WRITE CHARACTER COUNTER      (%14)
   abs 00000005           TREAD    .EQU   R5      ;READ CHARACTER FOR TEST               (%15)
   abs 0000000e           MADDR    .EQU   RR14    ;MESSAGE ADDRESS POINTER               (%1E)
   abs 0000000f           MDR      .EQU   R15     ;MESSAGE ADDRESS POINTER (LSB)         (%1F)
   abs 0000000b           SMR      .EQU   R11     ;STOP MODE RECOVERY REGISTER        (OF %0B)

0000000000000000010       XDATA    .EQU   %10     ;SPI XMIT DATA
0000000000000000011       RDATA    .EQU   %11     ;SPI RECEIVED DATA
0000000000000000012       CS       .EQU   %12     ;REGISTER CONTAINING /CS
0000000000000000013       DCS      .EQU   %13     ;REGISTER DE-ACTIVATING CS
000000000000000001c       XADDR    .EQU   %1C     ;LOCATION FOR X25C02 BYTE ADDRESS
                          ;
                          ;
```

```
                         ;  ---------------------- PROGRAM CONSTANTS ----------------------
00000000000000000000df   XCS          .EQU     11011111B        ;P35 = /CS FOR THE X25C02
0000000000000000000020   XCSNOT       .EQU     00100000B        ;P35 = DEACTIVE X25C02 /CS
00000000000000000000ef   RCARESET     .EQU     11101111B        ;RECIEVED CHAR AVAIL RESET
0000000000000000000010   RCAMASK      .EQU     00010000B        ;RECIEVED CHAR AVAIL MASK
                                                                ;SPI INSTRUCTIONS:
0000000000000000000006   WREN         .EQU     00000110B        ;SET WRITE ENABLE LATCH
0000000000000000000004   WRDI         .EQU     00000100B        ;DISABLE WRITE ENABLE LATCH
0000000000000000000005   RDSR         .EQU     00000101B        ;READ STATUS REGISTER
0000000000000000000001   WRSR         .EQU     00000001B        ;WRITE STATUS REGISTER
0000000000000000000003   READ         .EQU     00000011B        ;READ MEMORY LOCATION
0000000000000000000002   WRITE        .EQU     00000010B        ;WRITE MEMORY LOCATION

0000000000000000000002   WELMASK      .EQU     00000010B        ;WRITE ENABLE LATCH MASK OF STATUS REG
0000000000000000000002   NOBP         .EQU     00000010B        ;WRSR MASK FOR NO BLOCK PROTECT
000000000000000000000c   BPMASK       .EQU     00001100B        ;BLOCK PROTECT MASK FOR RDSR
                         ;
                         ;
                         ;  ---------------------- INTERRUPT VECTORS ----------------------
                         ;
                         ;     LOAD INTERRUPT VECTOR JUMP TABLE:
00000000                       .ORG     0000H
                         ;
                         ;
00000000 Wwww                  .WORD    INTRET                  ;IRQ0 - PORT P32 - PROGRAMMABLE EDGE
00000002 Wwww                  .WORD    INTRET                  ;IRQ1 - PORT P33 - NEGATIVE EDGE ONLY
00000004 Wwww                  .WORD    INTRET                  ;IRQ2 - PORT P31 - PROGRAMMABLE EDGE
00000006 Wwww                  .WORD    INTRET                  ;IRQ3 - SPI
00000008 Wwww                  .WORD    INTRET                  ;IRQ4 - T0 - INTERNAL
0000000a Wwww                  .WORD    INTRET                  ;IRQ5 - T1 - INTERNAL
                         ;
                         ;*****************************************************************************
                         ;
                         ;     INITIALIZE THE OPERATION OF THE CONTROLLER
                         ;
                         ;*****************************************************************************
                         ;
0000000c 8dWwww                JP       START

0000000f                 MESSAGE:
0000000f 5448495320415343      .ASCIC   'THIS ASCII DATA WILL BE STORED IN THE X25C02.
00000017 4949204441544120
0000001f 57494c4c20424520
00000027 53544f5245442049
0000002f 4e20544845205832
00000037 35434f322ea0
```

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APPENDIX A
Listing 1
(Continued)

```
0000003d 494e205245414c20      .ASCII  'IN REAL APPLICATIONS, IT COULD BE USED TO STORE SERIAL NUMBERS,
00000045 4150504c49434154
0000004d 494f4e532c204954
00000055 20434f554c442042
0000005d 4520555345442054
00000065 4f2053544f524520
0000006d 53455249414c204e
00000075 554d424552532c20
0000007d 50524f4752414d4d      .ASCIC  'PROGRAMMABLE PRESETS, OR CONFIGURATION INFORMATION.
00000085 41424c4520505245
0000008d 534554532c204f52
00000095 20434f4e46494755
0000009d 524154494f4e2049
000000a5 4e464f524d415449
000000ad 4f4e2ea0

000000b1                   START:
000000b1 9f                     EI                              ;RESET THE INTERRUPT FLIP-FLOP
000000b2 8f                     DI                              ;
                                                                ;UPON POWER-UP, THE STOP MODE RECOVERY
                                                                ;REGISTER IS SET FOR A POR SOURCE ONLY.
                                                                ;THE WDT IS NOT ACTIVE UNTIL A WDT
                                                                ;INSTRUCTION IS EXECUTED.
000000b3 b002                   CLR     P2                      ;CLEAR THE P2 OUTPUT BUFFER,  NOTE THAT IF
                                                                ; P26 IS USED TO POWER THE X25C02, THEN
                                                                ; THIS WILL TURN OFF THE POWER
000000b5 e6f601                 LD      P2M,#00000001B          ;SET ALL P2 BITS TO OUTPUT EXCEPT SPI
                                                                ; DATA INPUT LINE
000000b8 e603e0                 LD      P3,#%E0                 ;SET THE P3 OUTPUTS (P34-P36)
                                                                ; DEFAULT SCLK LOW, REST ARE HIGH
000000bb e6f701                 LD      P3M,#%01                ;SET THE P3 INPUTS TO BE IN ANALOG MODE
                                                                ; SET THE P2 OUTPUTS TO BE PUSH-PULL
000000be e6f92f                 LD      IPR,#00101111B          ;PRIORITIZE THE INTERRUPTS AS FOLLOWS:
                                                                ; IRQ3>IRQ5>IRQ4>IRQ1>IRQ0>IRQ2
000000c1 e6f804                 LD      P01M,#%04               ;SET INTERNAL STACK
000000c4 3110                   SRP     #%10                    ;SET A DEFAULT WORKING REGISTER SET
000000c6 e6ff7f                 LD      SPL,#%7F                ;
000000c9 d6Wwww                 CALL    SPI_MASTER_INIT         ;INITIALIZE THE SPI REGISTERS
000000cc d6Wwww                 CALL    SPI_ENABLE              ;ENABLE THE SPI BUSS

000000cf e612df                 LD      CS,#XCS                 ;LOAD THE CHIP SELECT VARIABLE
000000d2 e61320                 LD      DCS,#XCSNOT             ;LOAD THE CHIP DE-SELECT VARIABLE

                           ;
                           ;***************************************************************************;
                           ;                                                                          ;
                           ;    SEND WRITE ENABLE AND VERIFY STATUS BEFORE PROCEDING - ALSO CODE TO   ;
                           ;    CHECK STATUS OF THE BLOCK PROTECT BITS AND UNPROTECT THE CHIP.  BEFORE ;
                           ;    DOING ANYTHING, TURN ON THE X25C02 POWER                              ;
                           ;                                                                          ;
                           ;***************************************************************************;
```

```
                             ;
000000d5                     POWER_ON:
000000d5 460240                  OR      P2,#01000000B        ;TURN ON THE POWER TO THE X25C02.  THERE
000000d8 ff                      NOP                          ; MAY NEED TO BE SOME NOPs INSERTED TO
000000d9 ff                      NOP                          ; ACCOUNT FOR CAPACITANCE CHARGING.
                             ;
000000da                     WRITE_ENABLE:
000000da e61006                  LD      XDATA,#WREN          ;PROVIDE WRITE ENABLE CAPABILITY
000000dd d6Wwww                  CALL    SPI .                ;
000000e0 441303                  OR      P3,DCS               ;DE-ACTIVATE THE CHIP SELECT OUTPUT

000000e3                     READ_STATUS:
000000e3 e61005                  LD      XDATA,#RDSR          ;READ THE STATUS REGISTER
000000e6 d6Wwww                  CALL    SPI                  ;
000000e9 e61000                  LD      XDATA,#00            ;TRANSMIT DUMMY ADDRESS AND
000000ec d6Wwww                  CALL    SPI                  ;GET DATA FROM PERIPHERIAL
000000ef 441303                  OR      P3,DCS               ;DE-ACTIVATE THE CHIP SELECT OUTPUT

000000f2                     VERIFY_WE:
000000f2 761102                  TM      RDATA,#WELMASK       ;CHECK THE WRITE ENABLE BIT IN STATUS
000000f5 6be3                    JR      EQ,WRITE_ENABLE      ;WRITE ENABLE MASK WAS NOT SET

000000f7                     BLOCK_PROTECT:
000000f7 76110c                  TM      RDATA,#BPMASK        ;CHECK BLOCK PROTECT BITS IN STATUS
000000fa 6b**                    JR      EQ,WR_1BYTE_MESS     ;NO PROTECTION ACTIVATED
000000fc e61002                  LD      XDATA,#NOBP          ;SELECT NO BLOCK PROTECT
000000ff d6Wwww                  CALL SPI                     ;
00000102 441303                  OR      P3,DCS               ;DE-ACTIVIATE THE CHIP SELECT

                             ;
                             ;*****************************************************************************
                             ;                                                                           *
                             ;    CODE TO DEMONSTRATE TWO DIFFERENT METHODS OF WRITING DATA TO THE X25C02. *
                             ;    THE FIRST METHOD WRITES ONE BYTE AT A TIME, AND THE SECOND METHOD WILL   *
                             ;    WRITE FOUR BYTES AT A TIME.                                              *
                             ;                                                                           *
                             ;*****************************************************************************
                             ;
00000105                     WR_1BYTE_MESS:                   ;WRITE THE FIRST LINE OF THE MESSAGE ONE
                                                              ; BYTE AT A TIME
00000105 fcR000+0f,              LD      MDR,#MESSAGE         ;STORE THE MESSAGE ADDRESS POINTER
00000107 e61c00                  LD      XADDR,#%00           ;STORE THE MESSAGE STARTING AT LOCATION 00H
0000010a                     NEXT_BYTE:
0000010a e61002                  LD      XDATA,#WRITE         ;SEND THE WRITE COMMAND TO THE X25C02
0000010d d6Wwww                  CALL    SPI                  ;
00000110 e41c10                  LD      XDATA,XADDR          ;SEND THE ADDRESS TO STORE THE WRITE DATA
00000113 d6Wwww                  CALL    SPI                  ;
00000116 c20e                    LDC     TDATA,@MADDR         ;SEND THE MESSAGE DATA TO THE WRITE BUFFER
00000118 d6Wwww                  CALL    SPI                  ;
0000011b 441303                  OR      P3,DCS               ;DE-ACTIVATE THE CHIP SELECT OUTPUT
0000011e a0ee                    INCW    MADDR                ;INCREMENT THE MESSAGE ADDRESS POINTER
00000120 201c                    INC     XADDR                ;INCREMENT X25C02 ADDRESS
00000122 76e080                  TM      TDATA,#%80           ;CHECK IF END OF CHARACTER STRING
```

APPENDIX A
Listing 1
(Continued)

```
00000125 eb**                       JR     NE,WR_4BYTE      ;DONE WITH FIRST STRING
00000127 8be1                       JR     NEXT_BYTE            ;REPEAT LOOP UNTIL MESSAGE IS LOADED

00000129                  WR_4BYTE:                         ;WRITE THE NEXT LINE OF THE MESSAGE 4 BYTES
                                                            ; AT A TIME
00000129 4c04                       LD     MCHR,#4          ;X25C02 CAN PROCESS UP TO 4 BYTES IN A ROW
0000012b e61002                     LD     XDATA,#WRITE     ;SEND THE WRITE COMMAND TO THE X25C02
0000012e d6Wwww                     CALL   SPI              ;
00000131 e41c10                     LD     XDATA,XADDR      ;SEND THE ADDRESS TO STORE THE WRITE DATA
00000134 d6Wwww                     CALL   SPI              ;
00000137                  NEXT_CHAR:
00000137 c20e                       LDC    TDATA,@MADDR     ;SEND THE MESSAGE DATA TO THE WRITE BUFFER
00000139 d6Wwww                     CALL   SPI              ;
0000013c a0ee                       INCW   MADDR            ;INCREMENT THE MESSAGE ADDRESS POINTER
0000013e 201c                       INC    XADDR            ;INCREMENT X25C02 ADDRESS
00000140 76e080                     TM     TDATA,#%80       ;CHECK IF END OF CHARACTER STRING
00000143 eb**                       JR     NE,RD_MESSAGE    ;DONE WITH WRITING SECOND STRING
00000145 4af0                       DJNZ   MCHR,NEXT_CHAR   ;GET THE NEXT BYTE OF THE MESSAGE
00000147 441303                     OR     P3,DCS           ;DE-ACTIVATE THE CHIP SELECT OUTPUT
0000014a 8dR000+0129,               JP     WR_4BYTE             ;REPEAT UNTIL MESSAGE STORED
                          ;
                          ;***************************************************************************
                          ;                                                                          *
                          ;    CODE TO DEMONSTRATE HOW TO READ DATA FROM THE X25C02.  BEFORE READING,  *
                          ;    THE WRITE DISABLE INSTRUCTION IS SENT TO PROTECT THE INFORMATION       *
                          ;                                                                          *
                          ;***************************************************************************
                          ;
0000014d                  RD_MESSAGE:                       ;READ A LINE OF MESSAGE FROM THE EEPROM
                                                            ; - THIS ONLY CHECKS FIRST STRING (THERE
                                                            ;   ARE WO STRINGS TOTAL)
0000014d 441303                     OR     P3,DCS           ;DE-ACTIVATE THE CHIP SELECT OUTPUT
00000150 e61004                     LD     XDATA,#WRDI      ;DISABLE FUTURE WRITES
00000153 d6Wwww                     CALL   SPI              ;
00000156 441303                     OR     P3,DCS           ;DE-ACTIVATE THE CHIP SELECT OUTPUT

00000159 fcR000+0f,                 LD     MDR,#MESSAGE     ;STORE THE MESSAGE ADDRESS POINTER
0000015b e61003                     LD     XDATA,#READ      ;SEND THE READ OPCODE
0000015e d6Wwww                     CALL   SPI              ;
00000161 e61000                     LD     XDATA,#%00       ;SEND THE STARTING ADDRESS TO READ FROM
00000164 d6Wwww                     CALL   SPI              ;
00000167                  RD_NEXT:
00000167 c25e                       LDC    TREAD,@MADDR     ;GET A CHARACTER FROM THE MESSAGE
00000169 d6Wwww                     CALL   SPI              ;READ CHARACTER
0000016c a4e511                     CP     RDATA,TREAD      ;COMPARE THE CHARACTERS
                                                            ;*** IF THEY DID NOT COMPARE, SOMETHING
                                                            ;*** WOULD BE DONE HERE ***************
0000016f a0ee                       INCW   MADDR            ;MOVE THE MESSAGE POINTER
00000171 761180                     TM     RDATA,#%80       ;CHECK IF LAST CHARACTER IN THE STRING
00000174 6bf1                       JR     EQ,RD_NEXT       ;NOT THE LAST CHARACTER
00000176 441303                     OR     P3,DCS           ;DE-ACTIVATE THE CHIP SELECT OUPTUT

                          ;
```

```
                      ;*****************************************************************************
                      ;                                                                           *
                      ;     TURN OFF POWER TO THE X25C02, AND PLACE THE Z86C06 TO SLEEP           *
                      ;                                                                           *
                      ;*****************************************************************************
                      ;
00000179 b002               CLR     P2                      ;TURN OFF POWER TO X25C02

0000017b 70fd               PUSH    RP                      ;SAVE THE CURRENT REGISTER POINTER
0000017d e6fd0f             LD      RP,#%0F                 ;ACCESS THE STOP MODE RECOVERY REGISTER
00000180 bc28               LD      SMR,#00101000B          ;CONFIGURE STOP MODE FOR A HIGH LEVEL
                                                            ; TRANSITION OF P31.
00000182 50fd               POP     RP                      ;RESET THE REGISTER POINTER

00000184 ff                 NOP                             ;CLEAR THE PIPELINE
00000185 6f                 STOP                            ;STOP THE PROCESSOR
                                                            ; NOTE THAT WHEN THE PROCESSOR WAKES UP, IT
                                                            ; WILL RUN EVERYTHING ALL OVER AGAIN AND
                                                            ; THEN GOES BACK TO SLEEP.  A DECISION LOOP
                                                            ; COULD BE PUT AT THE BEGINNING OF THE CODE
                                                            ; TO CHECK THE PROCESSOR WAS ACTIVATED AS
                                                            ; THE RESULT OF A POR, OR AS THE RESULT OF
                                                            ; A STOP MODE RECOVERY
                      ;
                      ;*****************************************************************************
                      ;                                                                           *
                      ;     SPI_MASTER_INIT                                                       *
                      ;                                                                           *
                      ;     INITIALIZE THE SPI BUSS FOR MASTER MODE OF OPERATION                  *
                      ;     SPECIAL NOTE: THIS ROUTINE DOES NOT ENABLE THE SPI BUSS               *
                      ;                                                                           *
                      ;*****************************************************************************
                      ;
00000186              SPI_MASTER_INIT:
00000186 70fd               PUSH    RP                      ;SAVE THE CURRENT REGISTER POINTER
00000188 e6fd0c             LD      RP,#%0C                 ;ACCESS THE SPI EXPANDED REGISTER FILE
0000018b 2c8a               LD      SCON,#10001010B         ;ENABLE MASTER MODE
                                                            ;SET CLOCK SOURCE TO TCLK
                                                            ;XMIT ON FALLING EDGE, RECEIVE ON RISING
                                                            ;RESET THE RCV CHAR AVAILABLE
                                                            ;DISABLE THE COMPARE WAKE-UP FEATURE
                                                            ;SET CLOCK RATE (1 MHZ WITH 8 MHZ CRYSTAL)
0000018d 50fd               POP     RP                      ;RETRIEVE WORKING REGISTER POINTER
0000018f af                 RET
                      ;
                      ;*****************************************************************************
                      ;                                                                           *
                      ;     SPI_ENABLE                                                            *
                      ;                                                                           *
                      ;     ENABLE THE SPI BUSS - THIS STARTS THE SCLK                            *
                      ;                                                                           *
                      ;*****************************************************************************
```

APPENDIX B
Listing 2

```
                   ;
00000190           SPI_ENABLE:
00000190 70fd           PUSH    RP                  ;SAVE THE CURRENT REGISTER POINTER
00000192 e6fd0c         LD      RP,#%0C             ;ACCESS THE SPI EXPANDED REGISTER FILE
00000195 46e201         OR      SCON,#00000001B     ;ENABLE THE SPI BUSS
00000198 50fd           POP     RP                  ;RETURN TO NORMAL REGISTERS
0000019a af             RET
                   ;
                   ;*****************************************************************************
                   ;                                                                            *
                   ;    SPI                                                                     *
                   ;                                                                            *
                   ;    XMIT A BYTE OF DATA ON THE SPI BUSS FOUND IN REGISTER XDATA.  ALSO, PLACE *
                   ;    A RECEIVED CHARACTER IN REGISTER RDATA.  THIS ROUTINE WILL ACTIVATE THE  *
                   ;    /CS LINE, BUT WILL NOT DE-ACTIVATE THE LINE IN CASE MULTIPLE WRITES OR   *
                   ;    READS ARE GOING TO TAKE PLACE.                                          *
                   ;                                                                            *
                   ;    XDATA - REGISTER LOCATION 10h                                           *
                   ;    RDATA - REGISTER LOCATION 11h                                           *
                   ;                                                                            *
                   ;*****************************************************************************
                   ;
0000019b           SPI:
0000019b 70fd           PUSH    RP                  ;SAVE THE CURRENT REGISTER POINTER
0000019d 541203         AND     P3,CS               ;ACTIVATE /CS LINE FOR THE PERIPHERIAL
000001a0 e6fd0c         LD      RP,#%0C             ;ACCESS THE SPI EXPANDED REGISTER FILE
000001a3 56e2ef         AND     SCON,#RCARESET      ;RESET THE RECIEVED CHAR AVAIL
000001a6 1810           LD      RXBUF,XDATA         ;LOAD BUFFER WITH DATA TO BE XMITTED
000001a8           RCV_CHECK:
000001a8 76e210         TM      SCON,#RCAMASK       ;CHECK IF CHARACTER AVIALABLE IN RCVR
000001ab 6bfb           JR      EQ,RCV_CHECK        ;CHARACTER NOT IN RECEIVER
000001ad 1911           LD      RDATA,RXBUF         ;STORE THE RECIEVED CHARACTER
000001af 50fd           POP     RP                  ;RETURN TO NORMAL REGISTERS
000001b1 af             RET

                   ;
                   ;*****************************************************************************
                   ;                                                                            *
                   ;     INTERRUPTS                                                             *
                   ;                                                                            *
                   ;     THERE WERE NO INTERRUPTS USED BY THIS PROGRAM.  AN INTERRUPT COULD HAVE *
                   ;     BEEN USED TO READ THE SPI DATA (IRQ3).                                 *
                   ;                                                                            *
                   ;*****************************************************************************
                   ;
000001b2           INTRET:


                        .END
```

```
LOC      OBJ            LINE# --- SOURCE ---
                         ;*****************************************************************************
                         ;                                                                            *
                         ;     ZILOG / SPI INTERFACE                                                  *
                         ;     Z86C06 AND MC145053                                                    *
                         ;                                                                            *
                         ;     BY: LYN ZASTROW                                                        *
                         ;     COPYWRITE 1991                                                         *
                         ;                                                                            *
                         ;     ASSEMBLER: ZILOG ASMS8 ASSEMBLER                                       *
                         ;                                                                            *
                         ;     Z86C06 I/O UTILIZATION                                                 *
                         ;     PORT DEFINITIONS:                                                      *
                         ;     P20:   SPI PROCESSOR INPUT DATA                                        *
                         ;     P21:   NOT USED                                                        *
                         ;     P22:   NOT USED                                                        *
                         ;     P23:   NOT USED                                                        *
                         ;     P24:   NOT USED                                                        *
                         ;     P25:   NOT USED                                                        *
                         ;     P26:   NOT USED                                                        *
                         ;     P27:   SPI PROCESSOR OUTPUT DATA                                       *
                         ;     P31:   END OF CONVERSION SIGNAL                                        *
                         ;     P32:   NOT USED                                                        *
                         ;     P33:   NOT USED                                                        *
                         ;     P34:   SCLK OUTPUT FROM PROCESSOR                                      *
                         ;     P35:   NOT USED                                                        *
                         ;     P36:   /CS OUTPUT FROM PROCESSOR                                       *
                         ;                                                                            *
                         ;    TIME CONSTANTS ARE BASED ON 8MHz OPERATIONAL FREQUENCY                  *
                         ;                                                                            *
                         ;*****************************************************************************
                         ;
                         ;
                         ;    --------------- REGISTER POINTER DECLARATIONS ---------------
                         ;
                         ;
                         ;    ------------------- REGISTER DECLARATIONS -------------------
   abs 00000000          TDATA     .EQU    R0        ;SAME AS XDATA, BUT WORKING REGISTER   (%10)
   abs 00000001          RXBUF     .EQU    R1        ;SPI RX & XMIT BUFFER                  (%11)
   abs 00000002          SCON      .EQU    R2        ;SPI CONTROL REGISTER (EXTENDED REG)   (%12)
   abs 00000004          HIAD      .EQU    R4        ;HIGH BYTE OF CONVERSION               (%14)
   abs 00000005          LOAD      .EQU    R5        ;LOW BYTE OF A/D CONVERSION            (%15)
   abs 00000006          SLOOP     .EQU    R6        ;SHIFT LOOP COUNTER FOR CONVERSION     (%16)

 0000000000000000010     XDATA     .EQU    %10       ;SPI XMIT DATA
 0000000000000000011     RDATA     .EQU    %11       ;SPI RECEIVED DATA
 0000000000000000012     CS        .EQU    %12       ;REGISTER CONTAINING /CS
 0000000000000000013     DCS       .EQU    %13       ;REGISTER DE-ACTIVATING CS
                         ;
                         ;
```

APPENDIX B
Listing 2
(Continued)

```
                          ; ──────────────────── PROGRAM CONSTANTS ────────────────────
000000000000000000bf       XCS        .EQU    10111111B       ;P36 = /CS FOR THE MC145053
0000000000000000040        XCSNOT     .EQU    01000000B       ;P36 = DEACTIVE MC145053 /CS
000000000000000000ef       RCARESET   .EQU    11101111B       ;RECIEVED CHAR AVAIL RESET
0000000000000000010        RCAMASK    .EQU    00010000B       ;RECIEVED CHAR AVAIL MASK
0000000000000000002        EOCMASK    .EQU    00000010B       ;MASK FOR P31 - END OF CONVERSION

                                                              ;ANALOG MULTIPLEXOR ADDRESSES
0000000000000000000        AN0        .EQU    %00             ;ANALOG CHANNEL 0
0000000000000000010        AN1        .EQU    %10             ;ANALOG CHANNEL 1
0000000000000000020        AN2        .EQU    %20             ;ANALOG CHANNEL 2
0000000000000000030        AN3        .EQU    %30             ;ANALOG CHANNEL 3
0000000000000000040        AN4        .EQU    %40             ;ANALOG CHANNEL 4
000000000000000000b0       HSCALE     .EQU    %B0             ;HALF SCALE CHANNEL
000000000000000000c0       ZSCALE     .EQU    %C0             ;ZERO SCALE CHANNEL
000000000000000000d0       FSCALE     .EQU    %D0             ;FULL SCALE CHANNEL

                          ;
                          ; ──────────────────── INTERRUPT VECTORS ────────────────────
                          ;
                          ;  LOAD INTERRUPT VECTOR JUMP TABLE:
00000000                         .ORG    0000H
                          ;
                          ;
00000000 Wwww                    .WORD   INTRET               ;IRQ0 - PORT P32 - PROGRAMMABLE EDGE
00000002 Wwww                    .WORD   INTRET               ;IRQ1 - PORT P33 - NEGATIVE EDGE ONLY
00000004 Wwww                    .WORD   INTRET               ;IRQ2 - PORT P31 - PROGRAMMABLE EDGE
00000006 Wwww                    .WORD   INTRET               ;IRQ3 - SPI
00000008 Wwww                    .WORD   INTRET               ;IRQ4 - T0 - INTERNAL
0000000a Wwww                    .WORD   INTRET               ;IRQ5 - T1 - INTERNAL
                          ;
                          ;****************************************************************************
                          ;                                                                          *
                          ;  INITIALIZE THE OPERATION OF THE CONTROLLER                              *
                          ;                                                                          *
                          ;****************************************************************************
                          ;
0000000c                  START:
0000000c 9f                      EI                           ;RESET THE INTERRUPT FLIP-FLOP
0000000d 8f                      DI                           ;
                                                              ;UPON POWER-UP, THE STOP MODE RECOVERY
                                                              ;REGISTER IS SET FOR A POR SOURCE ONLY.
                                                              ;THE WDT IS NOT ACTIVE UNTIL A WDT
                                                              ;INSTRUCTION IS EXECUTED.
0000000e b002                    CLR     P2                   ;CLEAR THE P2 OUTPUT BUFFER
00000010 e6f601                  LD      P2M,#00000001B       ;SET ALL P2 BITS TO OUTPUT EXCEPT SPI
                                                              ; DATA INPUT LINE
00000013 e603e0                  LD      P3,#%E0              ;SET THE P3 OUTPUTS (P34-P36)
                                                              ; DEFAULT SCLK LOW, REST ARE HIGH
00000016 e6f701                  LD      P3M,#%01             ;SET THE P3 INPUTS TO BE IN ANALOG MODE
                                                              ; SET THE P2 OUTPUTS TO BE PUSH-PULL
00000019 e6f92f                  LD      IPR,#00101111B       ;PRIORITIZE THE INTERRUPTS AS FOLLOWS:
                                                              ; IRQ3>IRQ5>IRQ4>IRQ1>IRQ0>IRQ2
```

```
0000001c e6f804            LD      P01M,#%04          ;SET INTERNAL STACK
0000001f 3110              SRP     #%10               ;SET A DEFAULT WORKING REGISTER SET
00000021 e6ff7f            LD      SPL,#%7F           ;

00000024 d6Wwww            CALL    SPI_MASTER_INIT    ;INITIALIZE THE SPI REGISTERS
00000027 d6Wwww            CALL    SPI_ENABLE         ;ENABLE THE SPI BUSS

0000002a e612bf            LD      CS,#XCS            ;LOAD THE CHIP SELECT VARIABLE
0000002d e61340            LD      DCS,#XCSNOT        ;LOAD THE CHIP DE-SELECT VARIABLE

                         ;
                         ;*****************************************************************************
                         ;                                                                           *
                         ;    PERFORM A SELF TEST ON THE A/D CONVERTER.                              *
                         ;                                                                           *
                         ;*****************************************************************************
                         ;
00000030                 TEST_HALF:
00000030 e610b0            LD      XDATA,#HSCALE      ;PROVIDE ADDRESS FOR THE HALF SCALE TEST
00000033 d6Wwww            CALL    CONVERT            ;PERFORM THE A/D CONVERSION
00000036 a6e402            CP      HIAD,#%02          ;CHECK THE HI BYTE
00000039 ff                NOP                        ;THIS WOULD NORMALLY BE A CONDITIONAL JUMP
0000003a a6e500            CP      LOAD,#%00          ;CHECK THE LO BYTE
0000003d ff                NOP                        ;THIS WOULD NORMALLY BE A CONDITIONAL JUMP

0000003e                 TEST_ZERO:
0000003e e610c0            LD      XDATA,#ZSCALE      ;PROVIDE ADDRESS FOR THE ZERO SCALE TEST
00000041 d6Wwww            CALL    CONVERT            ;PERFORM THE A/D CONVERSION
00000044 a6e400            CP      HIAD,#%00          ;CHECK THE HI BYTE
00000047 ff                NOP                        ;THIS WOULD NORMALLY BE A CONDITIONAL JUMP
00000048 a6e500            CP      LOAD,#%00          ;CHECK THE LO BYTE
0000004b ff                NOP                        ;THIS WOULD NORMALLY BE A CONDITIONAL JUMP

0000004c                 TEST_FULL:
0000004c e610d0            LD      XDATA,#FSCALE      ;PROVIDE ADDRESS FOR THE FULL SCALE TEST
0000004f d6Wwww            CALL    CONVERT            ;PERFORM THE A/D CONVERSION
00000052 a6e403            CP      HIAD,#%03          ;CHECK THE HI BYTE
00000055 ff                NOP                        ;THIS WOULD NORMALLY BE A CONDITIONAL JUMP
00000056 a6e5ff            CP      LOAD,#%FF          ;CHECK THE LO BYTE
00000059 ff                NOP                        ;THIS WOULD NORMALLY BE A CONDITIONAL JUMP

                         ;
                         ;*****************************************************************************
                         ;                                                                           *
                         ;    PERFORM CONVERSION ON ALL OF THE CHANNELS                              *
                         ;                                                                           *
                         ;*****************************************************************************
                         ;
0000005a                 MUX_LOOP:
0000005a e61000            LD      XDATA,#0           ;START AT ANALOG CHANNEL 0
0000005d d6Wwww            CALL    CONVERT            ;PERFORM THE A/D CONVERSION
```

APPENDIX B
Listing 2
(Continued)

```
00000060                LOOP:
00000060 e61000                 LD      XDATA,#0            ;START THE LOOP AGAIN BECAUSE OF CONVERSION
                                                            ; DELAY IN MULTIPLEXOR
00000063 d6Wwww                 CALL    CONVERT             ;PERFORM THE A/D CONVERSION
00000066 ff                     NOP                         ;THIS WOULD NORMALLY BE CODE TO UTILIZE
                                                            ; HIAD AND LOAD FOR THE CHANNEL BEING
                                                            ; CONVERTED
00000067 061010                 ADD     XDATA,#%10          ;DO THE NEXT CHANNEL
0000006a a61050                 CP      XDATA,#%50          ;CHECK IF ALL CHANNELS CONVERTED
0000006d 1bf1                   JR      LT,LOOP             ;CONTINUE UNTIL ALL CHANNELS CONVERTED


                        ;
                        ;
                        ;
                        ;
0000006f 8dR000+0030,           JP      TEST_HALF           ;DO IT ALL OVER AGAIN!

                        ;
                        ;**************************************************************************
                        ;                                                                         *
                        ;       CONVERT                                                           *
                        ;                                                                         *
                        ;       SEND THE CHANNEL TO CONVERT, WAIT FOR THE EOC SIGNAL, AND READ THE *
                        ;       DATA.  THE ANALOG CHANNEL MUST BE STORED IN XDATA.  THE 10 BIT DATA IS *
                        ;       IS RETURNED HIAD AND LOAD.                                        *
                        ;                                                                         *
                        ;**************************************************************************
                        ;
00000072                CONVERT:
00000072 d6Wwww                 CALL    SPI                 ;TRANSMIT DATA IN 16 BIT FORMAT
00000075 d6Wwww                 CALL    SPI                 ;
00000078 441303                 OR      P3,DCS              ;DE-ACTIVATE THE CHIP SELECT OUTPUT
0000007b d6Wwww                 CALL    CONVERT_END         ;WAIT FOR END OF CONVERSION
0000007e d6Wwww                 CALL    SPI                 ;READ THE DATA - HI BYTE
00000081 4811                   LD      HIAD,RDATA          ;STORE THE HIGH BYTE
00000083 d6Wwww                 CALL    SPI                 ;READ THE LAST TWO BITS
00000086 5811                   LD      LOAD,RDATA          ;STORE THE LOW BYTE
00000088 441303                 OR      P3,DCS              ;DEACTIVATE THE CHIP SELECT OUTPUT
0000008b 6c06                   LD      SLOOP,#6            ;SHIFT THE DATA TO MAKE IT LOOK LIKE TRUE
                                                            ; 16 BIT DATA WITH THE 6 MSBs SET TO 0.  IF
                                                            ; IF 8 BIT DATA IS DESIRED, THEN THIS DOES
                                                            ; NOT NEED TO BE DONE AND THE HIAD RESULT
0000008d                SHIFT:                              ; COULD BE USED AS IS.
0000008d d0e4                   SRA     HIAD                ;SHIFT THE HI BYTE, PUT LSB IN CARRY FLAG
0000008f c0e5                   RRC     LOAD                ;SHIFT THE LO BYTE PUTTING THE CARRY FLAG
                                                            ; IN THE MSB
00000091 6afa                   DJNZ    SLOOP,SHIFT         ;CONTINUE THE SHIFTING UNTIL COMPLETE
00000093 56e403                 AND     HIAD,#00000011B     ;MASK OFF THE UPPER 6 BITS AFTER THE SHIFT

00000096 af                     RET
                        ;
```

```
                  ;***************************************************************************
                  ;                                                                          *
                  ;     CONVERT_END                                                          *
                  ;                                                                          *
                  ;     POLL THE END OF CONVERT LINE UNTIL A/D CONVERSION IS DONE            *
                  ;                                                                          *
                  ;***************************************************************************
                  ;
00000097          CONVERT_END:
00000097 760302         TM      P3,#EOCMASK          ;CHECK THE EOC BIT
0000009a 6bfb           JR      EQ,CONVERT_END          ;WAIT UNTIL THE EOC BIT IS HIGH
0000009c af             RET
                  ;
                  ;***************************************************************************
                  ;                                                                          *
                  ;     SPI_MASTER_INIT                                                      *
                  ;                                                                          *
                  ;     INITIALIZE THE SPI BUSS FOR MASTER MODE OF OPERATION                 *
                  ;     SPECIAL NOTE: THIS ROUTINE DOES NOT ENABLE THE SPI BUSS              *
                  ;                                                                          *
                  ;***************************************************************************
                  ;
0000009d          SPI_MASTER_INIT:
0000009d 70fd           PUSH    RP                      ;SAVE THE CURRENT REGISTER POINTER
0000009f e6fd0c         LD      RP,#%0C                 ;ACCESS THE SPI EXPANDED REGISTER FILE
000000a2 2c8a           LD      SCON,#10001010B         ;ENABLE MASTER MODE
                                                        ;SET CLOCK SOURCE TO TCLK
                                                        ;XMIT ON FALLING EDGE, RECEIVE ON RISING
                                                        ;RESET THE RCV CHAR AVAILABLE
                                                        ;DISABLE THE COMPARE WAKE-UP FEATURE
                                                        ;SET CLOCK RATE (1 MHZ WITH 8 MHZ CRYSTAL)
000000a4 50fd           POP     RP                      ;RETRIEVE WORKING REGISTER POINTER
000000a6 af             RET
                  ;
                  ;***************************************************************************
                  ;                                                                          *
                  ;     SPI_ENABLE                                                           *
                  ;                                                                          *
                  ;     ENABLE THE SPI BUSS - THIS STARTS THE SCLK                           *
                  ;                                                                          *
                  ;***************************************************************************
                  ;
000000a7          SPI_ENABLE:
000000a7 70fd           PUSH    RP                      ;SAVE THE CURRENT REGISTER POINTER
000000a9 e6fd0c         LD      RP,#%0C                 ;ACCESS THE SPI EXPANDED REGISTER FILE
000000ac 46e201         OR      SCON,#00000001B         ;ENABLE THE SPI BUSS
000000af 50fd           POP     RP                      ;RETURN TO NORMAL REGISTERS
000000b1 af             RET
                  ;
```

11

DTMF Tone Generation Using the Z8® CCP

In many applications a microprocessor must access phone lines for communications or data exchange. This has traditionally been accomplished by adding a DTMF tone encoder and a 3.58 MHz crystal; however, the Z8's pulse width modulation capabilities allow DTMF tone generation in software.

INTRODUCTION AND THEORY OF OPERATION

The program outlined below generates DTMF tones using a pulse width modulation (PWM) algorithm. PWM is used to vary the DC level of the output by varying the duty cycle (the "on" time divided by the cycle period) of the square wave. Varying the "on" time by a sine function and then feeding the output through a lowpass filter yields a sine wave.

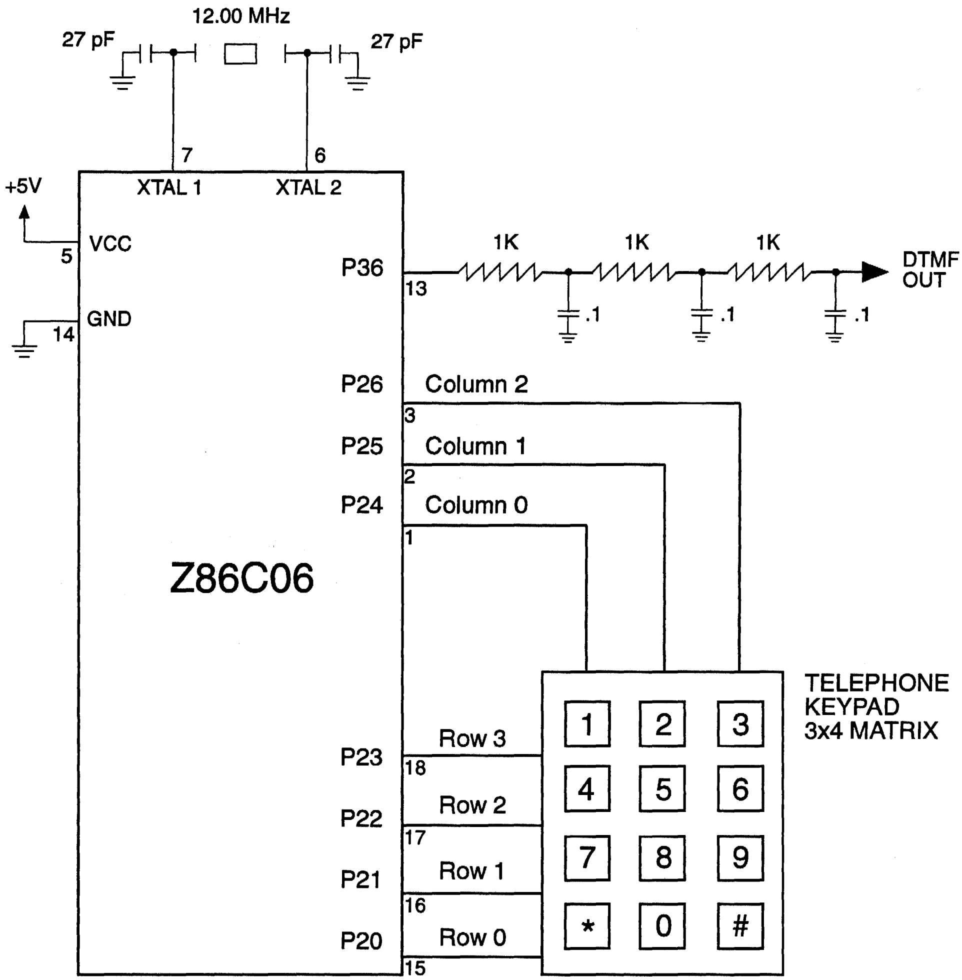
Sine values are determined by the Basic program in Listing 1. The sine table contains 256 entries, which in turn contain hexadecimal values representing a sine function for 360 degrees. These values are indexed and loaded into T1 at a sampling rate that, according to Nyquist, must be at least twice the highest frequency tone that we want to reproduce. Since the highest frequency for this application is 1477 Hz, the sampling rate must be at least twice this, or 2954 samples per second. The higher the sampling rate, the greater the accuracy. In the example illustrated here a sample rate of 12000 samples per second is used both for higher accuracy and ease in filtering.

SInce we are, in effect, producing two tones, two pointers are used to fetch the next value in the look-up table: one for row frequencies, and one for column frequencies. The frequency of the resulting sine wave can be calculated by multiplying the number of steps in the sine look-up table (256) by the desired frequency, divided by the sampling rate. This offset value is added to the current pointer, which then fetches the next hex number from the look-up table. This is done for both the row and column frequencies. The two are added, then loaded into the timer register (T1).

The lowpass filter was chosen to have a corner frequency of the lowest column frequency, or 1209 Hz. At this point, the column frequencies will be at least 3 dB below the row frequencies. However, telephone lines themselves act as a large-scale lowpass filter, and by the time the tones reach the telephone switching equipment, the amplitude should be the same. The spec therefore calls for the column frequencies to be 3 dB higher than the row frequencies. In the telephone industry this is known as "twist."

This adjustment can be made in software by taking the hex value from the look-up table for the column frequency and doing a "rotate left." This results in twice the amplitude for the column frequency — 6 dB gain, or 3 dB up from the row frequency, just where we want to be. Overall dB level from the output of the lowpass filter can be adjusted with a potentiometer.

DTMF TONE GENERATION



LISTING 1

```
;---------------------------------------------------------------------------------
;  This program, using the Zilog Z8, is designed to produce DTMF tones without
; an external DAC. The tones are produced using PWM, using one of the timers
; to vary the duty cycle of the output pulses. A sine look-up table is indexed
; at a sample rate well above the highest tone (1447 Hz). Both column and row
; values from the look-up table are added in software to produce the PWM output
; at the sample frequency. These hex values are loaded into a timer, which det-
; ermines the pulse width. At Terminal Count (TC), the port pin is taken low,
; and the difference between this period and the sample period is loaded into
; the timer. When run through a low-pass filter, the result is an accurate DTMF
; tone. Crystal frequency is 12.0000 MHz. The keypad columns are output from
; P24-6, while the row inputs are connected to P20-3.
;  This program was written on 6-2-92 by Don Owen Newquist, Zilog, Inc.
;---------------------------------------------------------------------------------
WORK_REG1       .equ    10h
offset_hi       .equ    r0
offset_lo       .equ    r1
offset          .equ    rr0
row_inc_hi      .equ    r4
row_inc_lo      .equ    r5
row_inc         .equ    rr4
pointer_hi      .equ    r6
pointer_lo      .equ    r7
pointer         .equ    rr6
col_inc_hi      .equ    r8
col_inc_lo      .equ    r9
col_inc         .equ    rr8
r_freq_hi       .equ    r10
r_freq_lo       .equ    r11
r_freq          .equ    rr10
c_freq_hi       .equ    r12
c_freq_lo       .equ    r13
c_freq          .equ    rr12
row_val         .equ    r14
col_val         .equ    r15
xtal            .equ    12000
sample          .equ    12000
ctval           .equ    xtal/8/sample
tabstp          .equ    256

WORK_REG0       .equ    00h
bounce          .equ    r4
counter_1       .equ    r5
key_cnt         .equ    r6
key_temp        .equ    r7
temp_1          .equ    r8
scan            .equ    r9
```

```
BOUNCE          .EQU    %04
COUNTER_1       .EQU    %05
KEY_CNT         .EQU    %06
KEY_TEMP        .EQU    %07
TEMP_1          .EQU    %08
SCAN            .EQU    %09

                .org    0000h
                .word   0
                .word   0
                .word   0
                .word   0
                .word   key_scan
                .word   timer_1
;--------------------------------------------------------------------------;
;                           INITIALIZATION                                 ;
;--------------------------------------------------------------------------;
                .org    000ch
                di                      ; disable int
                ld      rp,#0f0h        ; point to
                ld      r0,#0feh        ; pcon reg
                ld      r11,#0          ; crystal div by 2
                srp     #WORK_REG1      ; lowest bank
                ld      p3m,#0          ; default
                ld      p01m,#04h       ; int stack
                ld      spl,#80h        ; stack at highest ram
                ld      irq,#00h        ;
                clr     imr             ; clear int mask
                ld      pre0,#05h       ; cont mode
                ld      t0,#00          ; sampling time = 125 microsec
                ld      pre1,#6h        ; one shot mode
                clr     p3              ; clear port 3
                ld      imr,#10h        ; enable irq4
                ld      ipr,#0bh        ; irq5 > irq4
                ld      tmr,#03h        ; load & en t0
                ld      pointer_hi,#^hb sine    ; get lookup table
                ld      pointer_lo,#^lb sine    ; address
                ld      r_freq_hi,#1fh          ; 697
                ld      r_freq_lo,#0efh
                ld      c_freq_hi,#17h  ; 1209
                ld      c_freq_lo,#26h
                ld      row_inc_hi,#00  ; 697
                ld      row_inc_lo,#01
                ld      col_inc_hi,#00  ; 1209
                ld      col_inc_lo,#01  ;
                ld      row_val,#10h    ;
                ld      col_val,#10h    ;
                clr     BOUNCE          ; debounce counter
                clr     KEY_CNT         ;
                clr     KEY_TEMP        ;
                clr     TEMP_1          ;
                clr     SCAN            ;
                ei                      ; enable interrupts
check_bounce:   jr      check_bounce    ;
```

```
;------------------------------------------------------------------------;
;                    KEYBOARD SCAN ROUTINE                               ;
;------------------------------------------------------------------------;
key_scan:       push    rp              ;
                srp     #WORK_REG0      ;
                ld      p2m,#00001111b  ; out for p27-p24, in p23-p20
                ld      scan,#11101111b ; load scan byte
load_scan:      ld      p2,scan         ; output to port 2
                nop                     ;
                nop                     ;
                ld      temp_1,p2       ; load contents of p2
                ld      counter_1,#0    ; load counter
row_loop:       inc     key_cnt         ;
                scf                     ;
                rrc     temp_1          ; rotate right
                jr      c,no_keys       ;
                cp      key_temp,key_cnt; same key?
                jr      ne,load_keys    ; not the same
                inc     bounce          ; increment bounce counter
                cp      bounce,#2       ; bounce = 2 ?
                jr      ult,load_keys   ;
                call    dtmf_out        ; call transmit routine
                jr      exit            ;
load_keys:      ld      key_temp,key_cnt; transfer key data
                clr     key_cnt         ;
                pop     rp              ;
                iret                    ;
no_keys:        inc     counter_1       ; looking for a one
                cp      counter_1,#4    ; keep looking if not all rows
                jr      ult,row_loop    ; look again at next row
                scf                     ; set carry flag
                rlc     scan            ; rotate to scan next column
                jr      c,load_scan     ; scan next column if no carry
exit:           clr     bounce          ;
                clr     key_cnt         ;
                clr     key_temp        ;
                clr     counter_1       ;
                pop     rp              ;
no_irq:         iret                    ;
```

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```
;----------------------------------------------------------------------------
;                 Get Keyswitch Offset Values
;----------------------------------------------------------------------------
dtmf_out:         push    rp
                  srp     #WORK_REG1
                  ld      tmr,#00h         ; reset t0 bits
                  ld      imr,#20h         ; reset t0 vector
                  ld      pre0,#4          ; one-shot mode
                  ld      offset_hi,#^hb offset_tbl
                  ld      offset_lo,#^lb offset_tbl
                  sub     KEY_CNT,#1
                  cp      KEY_CNT,#0
                  jr      eq,no_index
index_loop:       incw    offset
                  incw    offset
                  incw    offset
                  incw    offset
                  dec     KEY_CNT
                  cp      KEY_CNT,#0
                  jr      ne,index_loop
no_index:         ldc     r_freq_hi,@offset
                  incw    offset           ;
                  ldc     r_freq_lo,@offset
                  incw    offset           ;
                  ldc     c_freq_hi,@offset
                  incw    offset
                  ldc     c_freq_lo,@offset
                  ld      t0,#ctval
enable:           ei
;----------------------------------------------------------------------------
;                 DTMF Generation Routine
;----------------------------------------------------------------------------
start:            or      p3,#40h          ;
                  or      tmr,#0fh         ;
                  tcm     p2,#0fh          ;
                  jr      z,exit_dtmf      ;
dtmf_loop:        tm      irq,#10h         ;
                  jr      z,dtmf_loop      ;
                  and     irq,#0efh        ;
                  jr      start            ;
exit_dtmf:        ld      imr,#10h         ; timer 0 int
                  ld      pre0,#01h        ; cont mode, full count
                  ld      imr,#10h         ; t0 only
                  ld      tmr,#03h         ;
                  ld      t0,#00           ;
                  pop     rp               ;
                  ret                      ;
```

```
;-----------------------------------------------------------------------
;               Timer 1 Interrupt Routine
;-----------------------------------------------------------------------
timer_1:        xor     p3,#40h         ; toggle port pin
                rcf
                add     row_inc_lo,r_freq_lo
                adc     row_inc_hi,r_freq_hi
                ld      pointer_lo,row_inc_hi
                ldc     row_val,@pointer
                add     col_inc_lo,c_freq_lo
                adc     col_inc_hi,c_freq_hi
                ld      pointer_lo,col_inc_hi
                ldc     col_val,@pointer
                rl      col_val
                add     row_val,col_val
load_t1:        ld      t1,row_val
                iret

                .org    180h
offset_tbl:
                .byte   1fh,0bfh,37h,70h
                .byte   23h,00h,37h,70h
                .byte   26h,0cfh,37h,70h
                .byte   2ah,0d7h,37h,70h
                .byte   1fh,0bfh,3dh,30h
                .byte   23h,00h,3dh,30h
                .byte   26h,0cfh,3dh,30h
                .byte   2ah,0d7h,3dh,30h
                .byte   1fh,0bfh,43h,0afh
                .byte   23h,00h,43h,0afh
                .byte   26h,0cfh,43h,0afh
                .byte   2ah,0d7h,43h,0afh

                .org    200h
sine:
        .byte   18h,18h,18h,18h,18h,19h,19h,19h,19h,19h,1ah,1ah
        .byte   1ah,1ah,1ah,1ah,1bh,1bh,1bh,1bh,1bh,1bh,1ch,1ch
        .byte   1ch,1ch,1ch,1ch,1dh,1dh,1dh,1dh,1dh,1dh,1dh,1dh
        .byte   1eh,1eh,1eh,1eh,1eh,1eh,1eh,1eh,1eh,1eh,1fh,1fh
        .byte   1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh
        .byte   1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh
        .byte   1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1fh,1eh
        .byte   1eh,1eh,1eh,1eh,1eh,1eh,1eh,1eh,1eh,1dh,1dh,1dh
        .byte   1dh,1dh,1dh,1dh,1dh,1ch,1ch,1ch,1ch,1ch,1ch,1bh
        .byte   1bh,1bh,1bh,1bh,1bh,1ah,1ah,1ah,1ah,1ah,1ah,19h
        .byte   19h,19h,19h,19h,18h,18h,18h,18h,18h,18h,17h,17h
        .byte   17h,17h,17h,16h,16h,16h,16h,16h,16h,15h,15h,15h
        .byte   15h,15h,15h,14h,14h,14h,14h,14h,14h,13h,13h,13h
        .byte   13h,13h,13h,13h,12h,12h,12h,12h,12h,12h,12h,12h
        .byte   12h,11h,11h,11h,11h,11h,11h,11h,11h,11h,11h,11h
        .byte   11h,11h,11h,11h,11h,11h,11h,11h,11h,11h,11h,11h
        .byte   11h,11h,11h,11h,11h,11h,11h,11h,11h,11h,11h,11h
        .byte   11h,11h,11h,11h,11h,11h,11h,11h,11h,11h,11h,11h
        .byte   12h,12h,12h,12h,12h,12h,12h,12h,12h,13h,13h,13h
        .byte   13h,13h,13h,13h,14h,14h,14h,14h,14h,14h,15h,15h
        .byte   15h,15h,15h,15h,16h,16h,16h,16h,16h,16h,17h,17h
        .byte   17h,17h,17h,18h

                .end
```

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Notes:

SERIAL COMMUNICATIONS USING THE Z8® CCP SOFTWARE UART

Many applications require asynchronous communications with the outside world. This Application Note presents one method for accomplishing serial communications through software rather than hardware by taking advantage of the flexibility of the Z8® CCP™.

INTRODUCTION

Straightforward serial communications between Zilog Z8® CCP™ processors and the outside world are possible using the 9600 baud software UART described in this Application Note. This technique is particularly well suited to projects which require asynchronous communications, but where a hardware UART is cost- or space-prohibitive. Designed to be used with the Zilog CCP family, running at an 8 MHz clock frequency, this approach requires the use of only one counter/timer and two port pins.

THEORY OF OPERATION

Essentially, the UART remains in an idle loop until it either (a) senses an interrupt request on port P3-1 (Receive), or (b) it senses a character in the BUFFER register to be transmitted. Eleven bits in total are counted: one start bit, eight data bits, one parity bit, and one stop bit. A typical schematic is provided in Figure 1.

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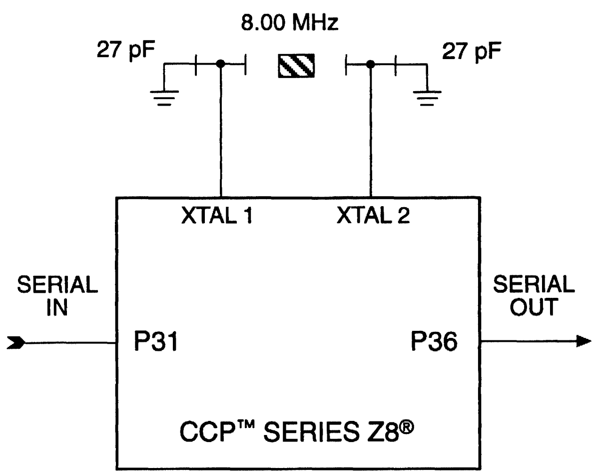

Figure 1. Serial CCP UART

RECEIVE MODE

The UART goes into operation upon sensing a receive character via an interrupt (Low-going edge) request on P3-3. It then prepares to receive one start bit (R10), eight data bits (R10), one parity bit, and one stop bit (R10). Subsequently, it programs the T0 timer as a down-counter which reaches a terminal count in 0.104 ms. This is the sampling rate. The interrupt vector is loaded with the receive subroutine address, which is jumped to when an IRQ 4 interrupt is generated. This routine decrements the bit counters, and rotates the data in register R10. When a byte is assembled, it waits for the parity and stop bit, which then completes the transfer.

TRANSMIT MODE

The UART is ready to transmit at any time, and senses a transmit character when BUFFER is not zero. When BUFFER is loaded with data to be transmitted, the jump vector is loaded with the transmit subroutine address. The counter/timer T0 is then loaded for a terminal count at 0.104 ms. This is the sampling rate for the transmission. When T0 times out, an IRQ 4 interrupt is generated. The program jumps to the IRQ 4 interrupt routine, and then immediately jumps to the transmit routine. The transmit routine decrements the bit counter and rotates out the transmit data.

```
;*********************************************************************
;*                                                                   *
;*      SERIAL DATATRANSFER APPLICATION FOR CCP-SERIES               *
;*      WITHOUT HARDWARE UART.                                       *
;*                                                                   *
;*      WRITTEN BY W. MANSFELD, ZILOG GERMANY / feb. 1991/ dec.91    *
;*                                                                   *
;*********************************************************************
TO_VECTOR_H:    .EQU    %20
TO_VECTOR_L:    .EQU    %21
BYTE_BUFF:      .EQU    %22     ;CONTAINS Rx RETURN BYTE ( RP=20 )

                .ORG    %00

                .WORD   DUMMY
                .WORD   DUMMY
                .WORD   DUMMY
                .WORD   SER_IN          ;RX BYTE INTERRUPT
                .WORD   TO_INT          ;TO JUMP VECTOR INTERRUPT
                .WORD   DUMMY

                .ORG    %0C

                DI
                LD      SPL,#%7E
                CLR     SPH
                LD      IPR,#1          ;INT. PRIORITY
                SRP     #%20            ;SET REG. POINTER
                                        ;refer to upper EQU's

                LD      P3M,#00000001B  ;PORT 3 NORMAL MODE
                LD      P01M,#00000100B ;SELECT INTERNAL STACK

;               PORTS 0,1,2 NOT USED IN THIS APP.

                LD      IMR,#00011000B  ;ENABLE TO,RX INT
                EI

;       SEND A ENDLESS BYTE STREAM VIA Tx LINE

TEST_LOOP:
                LD      R4,#'5'         ;ASCII 5  TEST BYTE
                CALL    SER_OUT         ;SEND BYTE
                JR      TEST_LOOP
```

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```
;*********************************************************************
;       SERIAL RECEIVE ON INTERRUPT P3,0                             *
;       INTERRUPT WHEN A CHARACTER COMES FROM HOST                   *
;       input: none                                                  *
;*********************************************************************
SER_IN:

;       SAVE USED REGISTERS

        PUSH    R15             ; TRANSPARENT /DATA BUFFER
        PUSH    R6              ; SERIAL BIT COUNT ++

        PUSH    IMR             ;SAVE INT. MODE REGISTER
        LD      IMR,#00010000B  ;SELECTE T0 INT. ONLY


;       PUT A DELAY LOOP TO THAT POINT IF BAUDRATE IS BELOW OR
;       9600 BAUD, TO REACH MIDDLE OF START BIT BEFORE STARTING
;       RX BIT WINDOW



;       SERIAL BAUDRATE
;       USE T0 FOR BIT-CENTRE INTERRUPT

        LD      PRE0,#00000111B ;MODIFY PRESCALER PRE0
        LD      T0,#104         ;BAUD RATE = 9600 / ON 8MHz CRYSTAL
        LD      TMR,#00000011B  ;START/PRESET T0

;       MODIFY T0 INT. JUMP VECTOR

        LD      R7,#^HB SERIN_T0_INT
        LD      T0_VECTOR_H,R7
        LD      R7,#^LB SERIN_T0_INT
        LD      T0_VECTOR_L,R7
        EI
        LD      R6,#8           ;READ 8 DATABYTES
        CLR     R15             ;CLEAR RECEIVESHIFT REGISTER(BUFFER)
SER_IN1:
        CP      R6,#0           ;8 BITS RECEIVED ?
        JR      NE,SER_IN1      ;WAIT FOR BITS RECEIVED
        LD      BYTE_BUFF,R15   ;SAVE RX BYTE IN BUFFER

        LD      R6,#1           ;READ 1 STOPBIT
        CLR     R15
SER_IN2:
        CP      R6,#0           ;READ  DATA DONE?
        JR      NE,SER_IN2      ;WAIT FOR BIT RECEIVED
        DI
        AND     TMR,#11111100B  ;T0 OFF
        POP     IMR             ;INTERRUPT MASK BACK
        CLR     IRQ
        POP     R6
        POP     R15
        IRET                    ;RX DONE
```

```
;*****************************************************
;*      OUTPUT A BYTE THROUGH THE SERIAL            *
;*      INPUT : R4 CONTAINS TX-DAT                  *
;*      OUTPUT: R4 HOLDS INPUT DATA                 *
;*****************************************************
SER_OUT:
;       SAVE USED REGISTERS
        PUSH    R5              ;TO INT. VECTOR POINTER LB
        PUSH    R7              ;TX DATA
        PUSH    R10             ;BIT COUNTER
        PUSH    IMR             ;FOR TO int. ONLY ACTIVE HEREIN
        PUSH    R4              ;SAVE DATA
        LD      IMR,#00010000B  ;TO int. ON

;       SERIAL BAUDRATE, USE TO FOR TIMING

        LD      TO,#104         ; BAUD RATE = 9600
        LD      PREO,#00000101B ; PRESCALER VALUE 1
        LD      TMR,#%03        ; LOAD + ENABLE TO

;       MODIFY TO INT. JUMP VECTOR FOR Tx

        LD      R7,#^HB SER_OUT_TO_INT
        LD      TO_VECTOR_H,R7
        LD      R7,#^LB SER_OUT_TO_INT
        LD      TO_VECTOR_L,R7
        EI

;       NOW SEND DUMMY 0-bit and one START BIT

        LD      R10,#2          ;SEND 2 BIT: 0 + START-BIT
        LD      R7,#11111101B   ;VALUE for the 2 bits
SER_OUT1:
        CP      R10,#0          ;DONE?
        JR      NZ,SER_OUT1
        LD      R10,#8          ;SEND 8 BITS OF DATA
        POP     R7              ;TAKE DATABYTE FROM STACK
        PUSH    R7              ;CORRECT THE STACK ( PUT BACK THAT BYTE )
;       CHECK IF ALL DATABITS SENT
SER_OUT2:
        CP      R10,#0          ;DONE?
        JR      NZ,SER_OUT2

;       NOW SEND STOP-BIT

        LD      R10,#1          ;SEND  ONE BIT ( STOP BIT )
        LD      R7,#%FF         ;VALUE
SER_OUT3:
        CP      R10,#0          ;DONE?
        JR      NZ,SER_OUT3
        DI
        AND     TMR,#11111100B  ;STOP TO
        POP     R4
        POP     IMR             ;OLD IMR BACK
        POP     R10
        POP     R7
        POP     R5
        EI
        RET                     ;RET ONLY, WAS NOT AN INT. SERVICE
```

```
;*************************************************
;*      TRANSMIT TO INTERRUPT HANDLER            *
;*      FOR  BIT GENERATION TO P3,7              *
;*************************************************
SER_OUT_TO_INT:
                DEC     R10             ;BIT CNT DOWN
                RR      R7              ;SHIFT BIT
                JR      C,SER_O_TO_INT1 ;BIT = 1
                AND     P3,#%7F         ;BIT = 0
                IRET
SER_O_TO_INT1:  OR      P3,#%80         ;BIT = 1
                IRET

;       PROGRAMMABLE USE OF TO ( RX or TX )

TO_INT:
                JP      @TO_VECTOR_H    ;INDIRECT TO int JUMP
                                        ;FOR Tx,RX bit read
DUMMY:          IRET

;*************************************************
;*      RECEIVE  TO INTERRUPT HANDLER            *
;*      FOR  BIT READ FROM P3,0                  *
;*************************************************
SERIN_TO_INT:
                DEC     R6      ;BIT COUNT
                PUSH    R15     ;SAVE FOR TEMPORARY USE
                LD      R15,P3  ;READ THE PORT / BIT  Rx
                RR      R15     ;CHECK if 0 or 1
                POP     R15     ;NOW USE AS RECEIVE SHIFT BUFFER
                RRC     R15     ;SHIFT THE CARRY =0 OR 1 INTO BUFFER
                IRET


                .END
```

THE VERSATILE Z86C08: THREE KEY FEATURES OF THIS Z8® MICROCONTROLLER

If you need D/A conversion, or a zero crossing detector, or a current sensing device ... Use the Z86C08's dual comparator.

DUAL ANALOG COMPARATOR

Using the dual analog comparators on the Z86C08 in conjunction with several on-chip features, provides a cost effective way to monitor power failures and frequency excursions (comparator used as a zero crossing detector), as a blood pressure tester and digital readout (comparator used as a A/D converter), or as a current sensing device in automotive design to detect and subsequently shut off any short circuiting of relays, lights, monitors, etc.

In many microcontroller applications, the digital designer is often concerned with sampling and controlling non-digital elements within the system. However, when the designer is forced to deviate from the precise world of TTL logic and regulated 5 volt supplies, frequently, microcontroller architectures and specifications fall short in the areas of cost sensitivity and consumer orientation. Therefore, using the analog comparators in these specific areas are a few of the reliable, inexpensive design applications for the Z86C08.

Comparator Basics

The dual comparators share a common inverting terminal with non-inverting terminals bonded directly to external I/O ports (Figure 1). The comparators are enabled by a bit in the I/O port mode/control register. If bit D1 of R247 is zero, then the comparators are in digital mode. If D1 is one, then they are in analog mode. With the comparators disabled, the I/O ports are available for normal activities. These particular I/O ports can be used to generate external interrupt requests to the Z8®. With the comparators enabled, interrupts can also be generated.

The ideal comparator is a three terminal device (Figure 2). V1 is a non-inverting terminal. Signals entering at V2, the inverting terminal, exit V_{OUT} 180° out of phase. Since a comparator is essentially an operational amplifier, it has an associated gain. The open look gain (no feedback) of a comparator is defined as the Voltage Out (V_{OUT}) over the Differential Input Voltage. The Differential Input Voltage is the voltage at the non-inverting input with respect to the inverting input. Thus gain is:

GAIN = V_{OUT}/V1 – (V2) = Voltage Out/Differential Input Volt

The Inset Offset Voltage, the difference between V1 and V2, forces V_{OUT} to a specified level. The Input Offset Voltage is typically below 50 mV.

Zero Crossing Detect Applications

The dual comparator can be used as a zero crossing detector to monitor 110 VAC (or other power line parameters) and its frequency (Figure 3). Each time the voltage passes through zero an interrupt is generated. The outputs of the comparators on the Z86C08 connect directly to the on-chip CPU. When using the comparators to detect zero crossing of the signal, interrupts are generated at every crossing of a signal, interrupts are generated at every crossing. Interrupt subroutines can then calculate period and phase angle relationships between any two analog signals. The phase angle being critical when calculating power factor in power line circuits.

In the case of 110 VAC, 60 Hz power line, an interrupt is generated every 1/120 of a second. This means that whenever the monitor stops (no interrupts), there is a power fail or other problem which can be translated by a control device recovery action (Figure 4).

Frequency checks can also be made by zero crossing detection. Whenever frequency drifts from the normal monitoring zero points, interrupts are either increased (higher frequency) or decreased (lower frequency) from the norm. If necessary, appropriate action is then taken.

Zero Crossing Detect Applications (Cont'd.)

Another application is threshold detection for low voltage battery operated devices. Whenever the VBB drops below the Zener reference voltage level, an interrupt is generated to alert a control device or alarm.

The addition of two on-chip counter/timers further complement the above mentioned applications. Crystal precision timing is done on the period of zero crossings. The sum or difference of two separate analog signals can then be calculated. For example, negative or positive feedback is returned from the Z86C08 in closed loop calculations. In power circuits, a time-of-day clock could be implemented with a timer. Then, date and time of power failures and frequency excursions can be recorded. CMOS technology allows for battery backup.

Analog to Digital (A/D) Conversion

Accurate low speed A/D conversion is implemented with the Z86C08 using the dual slope or ratiometric method. With this method, a dv/dt is applied to the inverting terminal of a comparator. The analog input (V_{INPUT}) signal is applied to the non-inverting terminal. The charge rate of the RC circuit is a dv/dt (Figure 5). As V_{REF} ramps upward from zero volts during time T1, V_{REF} will exceed V_{INPUT}. This causes the comparator to change state and produce an interrupt. By using the on-chip timer, time T1 can be quickly determined.

The RC circuit is immediately discharged over fixed time T2 (Figure 6), where T2 is determined by the time constant Tc = RCn. Since the product of RC is only an approximate indicator of discharge time, a value of n should be multiplied to improve accuracy. A general guideline should equate n to 1.4. Then, T2 = 1.4 RC. The dual slope A/D converter measures voltage by converting voltage into time intervals. Or,

$T2/T1 = V_{INPUT}/V_{REF}$, then, $V_{INPUT} = V_{REF} = T2/T1$

By using an I/O port on the Z86C08 as the V_{REF} input, interrupts generated by the comparators can alternately switch V_{REF} ON or OFF to perform the conversions.

Example: Blood Pressure Tester

A pressure transducer in a blood pressure tester is a good example of the dual slope A/D conversion method. A minimum system consists of display logic, Z86C08 circuitry and a transducer signal input (Figure 7). P00 outputs the appropriate signal to the RC ramp circuit of the V_{REF} input. The output from the pressure transducer (Figure 8) is a linear voltage response to the applied pressure. This signal is input to An2, the non-inverting terminal of the comparator.

In this configuration, the sampling cycle for the A/D conversion begins when a logical 1 is output on P00 and a timer is enabled. When the comparator transitions, an interrupt is generated, the timer is stopped and P00 is toggled to discharge the RC circuit. By storing the count T1 and resetting the timer, the converter is now ready to take another sample. The value of V_{IN} is mathematically determined later and software algorithms are used to determine corresponding pressure.

The display is driven from a simple multiplexer circuit. The Z86C08 can sink large I_{OC} currents which reduces or eliminates buffering.

Current Sensing

The dual comparator is used as a current sensing device in many application areas, e.g., in automotive relays, lights, monitors, etc. In the automotive arena, current sensing is used in a typical case as shown in Figure 9a. If the functional block shorts, then current (I) surges causing voltage (V) to fall. When V reaches 2.5V, the comparator triggers an interrupt which allows software to enable an emergency shut off.

Comparator Basics

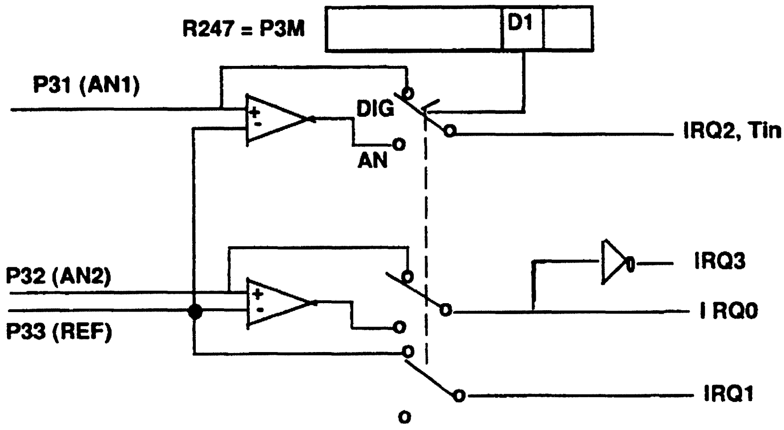


Figure 1. Dual Analog Comparator

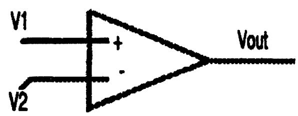


Figure 2. Ideal Comparator

Zero Crossing Detect Applications

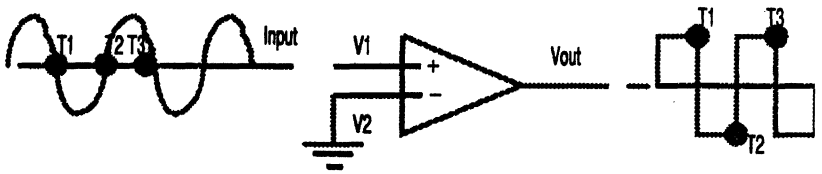


Figure 3. Zero Crossing Detector

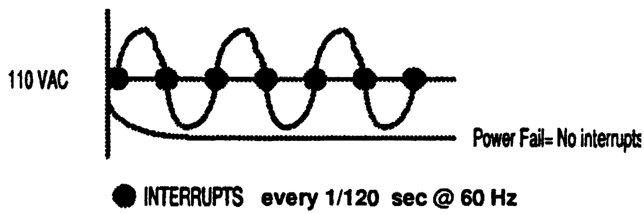


Figure 4. Interrupt After Power Failure

Analog to Digital (A/D) Conversion

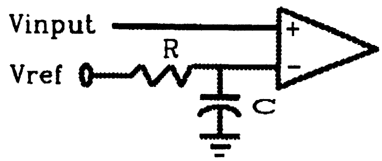


Figure 5. A/D Converter

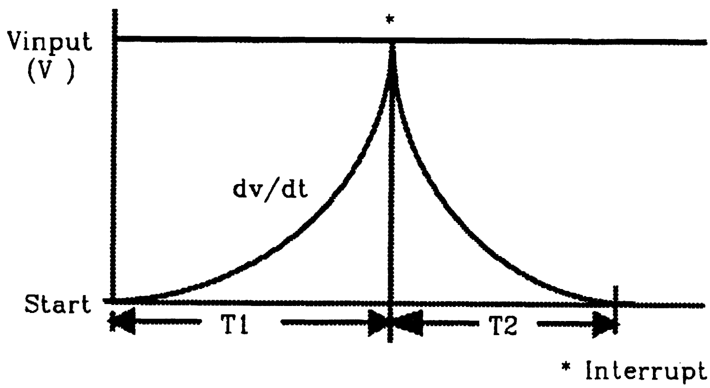


Figure 6. Voltage vs. Time

Blood Pressure Tester

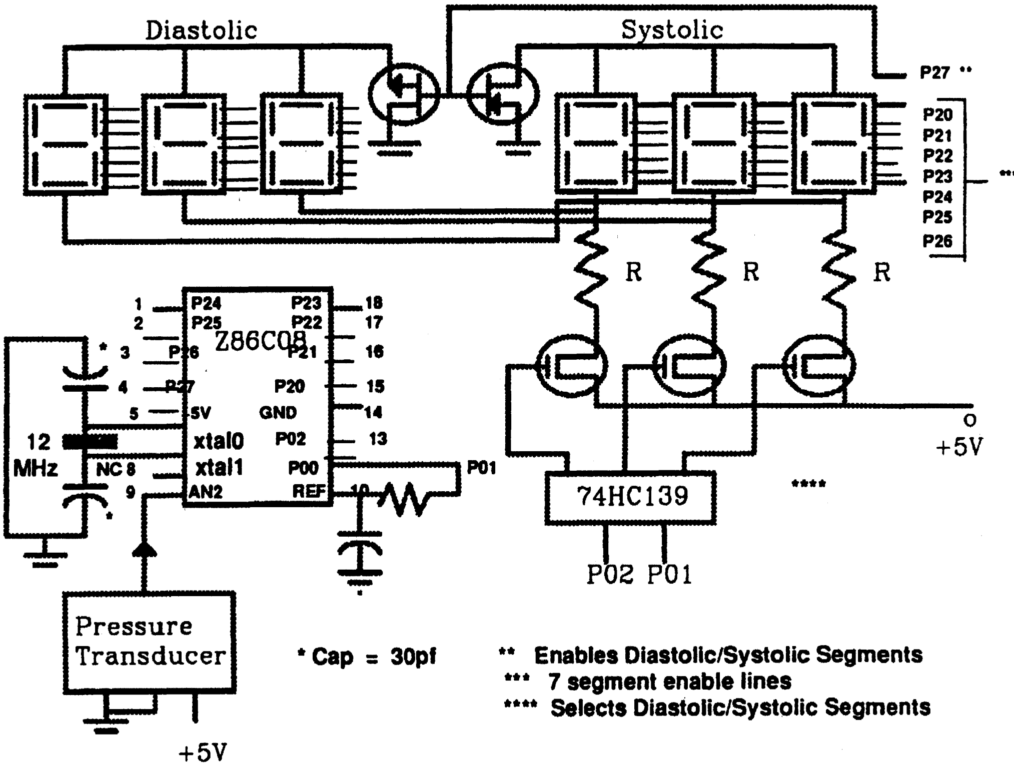


Figure 7. A/D Blood Pressure Test and Readout

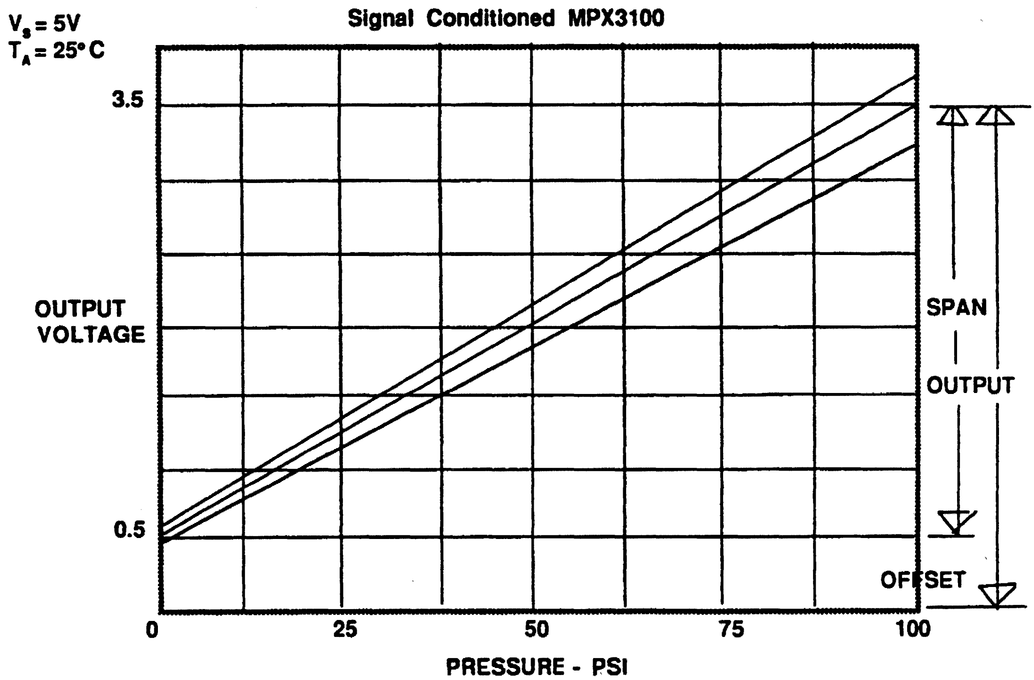


Figure 8. Silicon Pressure Transducer

Current Sensing

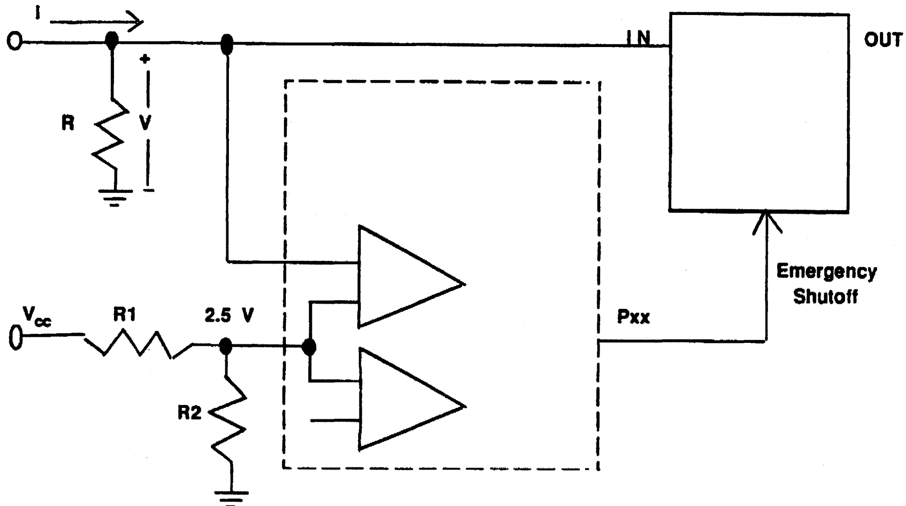
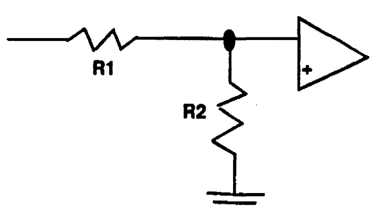


Figure 9a. Current Sensing

Note:
R is large compared to the equivalent impedance of the Functional Block input. R1 and R2 are user-selectable and are generally in a 10K to 100K range of power dissipation considerations. R1 and R2 are determined from the following formula (Figure 9b.).



$$\frac{R2}{R1 + R2}$$

Figure 9b. Power Dissipation Formula

THE Z86C08 CONTROLS A SCROLLING LED MESSAGE DISPLAY

Display text and graphics while scrolling the LED message with a minimum of hardware The characters are displayed using a time-division multiplex technique with more than six characters easily added by software.

INTRODUCTION

Designed around the Zilog Z86C08, 18-pin microcontroller, this LED display is capable of displaying text as well as graphics, with hardware being kept to a minimum. The present design is configured to display u to six characters, but additional characters are easily added with minimal software changes.

The display uses a TDM (Time-Division Multiplexed) technique to display the characters. That is, each character segment is turned on for a few hundred microseconds at a time, then is "refreshed" every 18 ms.

For demonstration purposes, the software routine displays the time in hours, minutes, and seconds. Once every sixty seconds, a "secret message" scrolls across the display. Then, after the message is displayed, the program reverts back to displaying the time.

11

THE HARDWARE

The Z86C08 (Figure 1) uses Port 2 for the row data and clocks the column data out of Port 0. PNP transistors are used to drive the rows, since the Z86C08 cannot source the required current directly. The characters are displayed in a 5x7 format, so only seven lines are needed out of Port 2. A logic Low turns on the transistors, while a logic High turns them off.

THE HARDWARE (Continued)

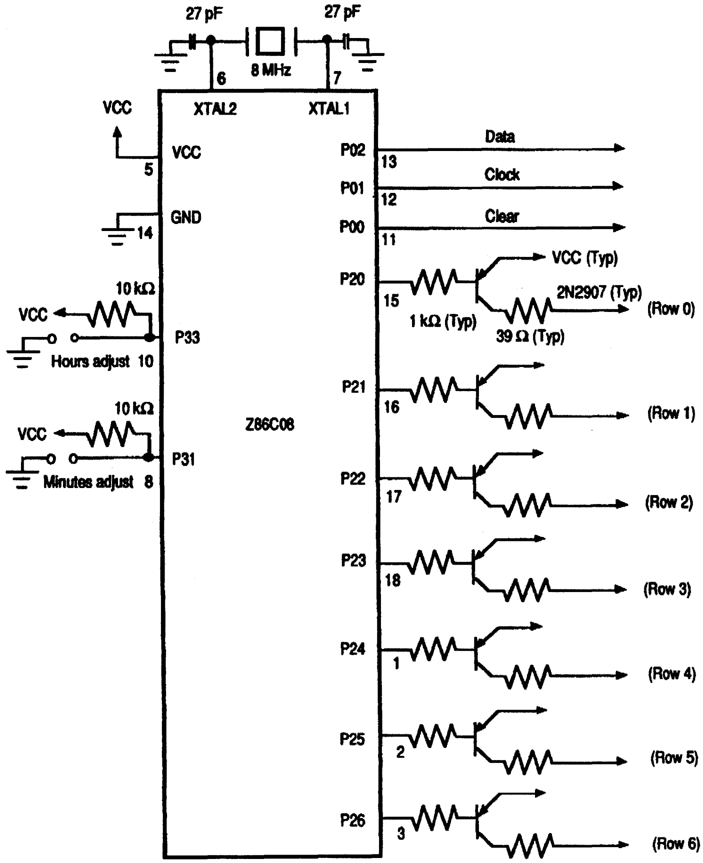


Figure 1. Z86C08 Circuit Functions

The columns are driven by six 74HCT164 shift registers (Figure 2). The 74HCT164s do not have the necessary sink capability to drive the LEDs, so the outputs of the shift registers drive six 75492 high-current buffers. These are capable of sinking 250 mA per pin continuously, with instantaneous current per column approaching 1.5 A.

Each 74HCT164 drives six columns; five character segments, plus one space. The last Q output from the shift register is then fed to the DATA input of the next shift register, while all CLEAR and CLOCK lines are wired in parallel.

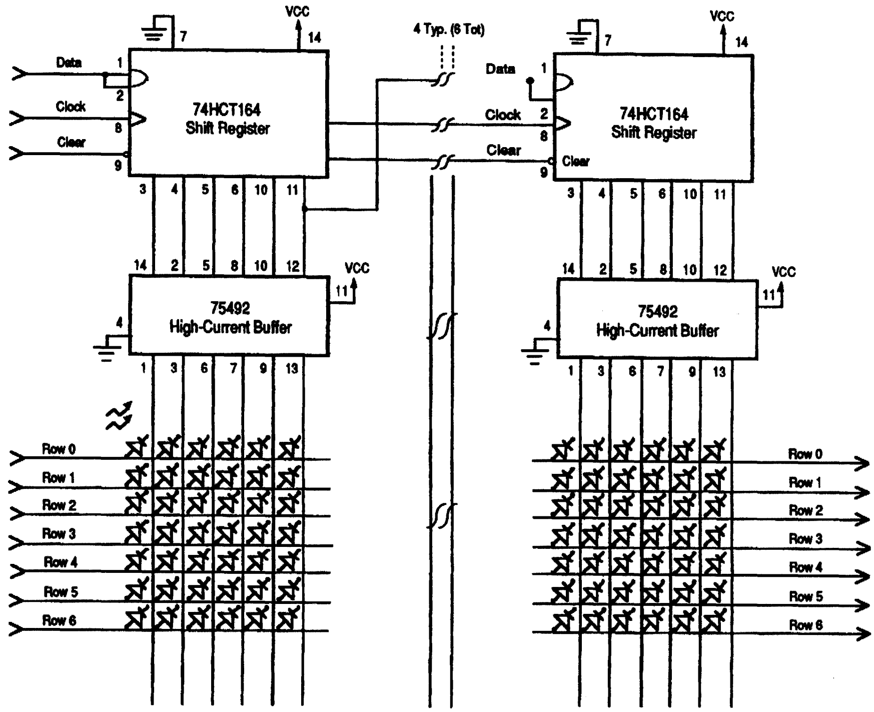


Figure 2. LED Circuitry

THE HARDWARE (Continued)

To scan the display, a logic 1 is output at P0-2. Next, P0-1 is taken High, then immediately taken Low, along with P0-2. This clocks a logic 1 into the first shift register (column 1). Next a character segment is output at P2. The transistors that are turned on will source current for the LEDs with the column providing a sink path. The columns are left on for about 500 µs and then turned off. Now, the column data is shifted one and a new character segment is output. After the last column has been scanned, the display is "refreshed" starting at the first column again.

To set the time, two push-button switches are connected to Port 3 to adjust the hours and minutes.

THE SOFTWARE

The initialization part of the program configures the ports, timers, interrupts, etc. The size of the display buffer (FIFO) is determined by the number of columns in the display. The bottom of the display buffer starts at 20H. The upper limit of the display buffer can extend to 70H. This translates into a sixteen-character display. There is no need to have a display buffer larger than the display itself, since only that many characters can be viewed at a time. A power-up, the display is configured for showing the time.

The flowchart for the display appears in Figures 3a and 3b. To keep time, the internal clock was divided down by T0 to provide an interrupt every 5 ms. The interrupt routine increments a counter, and when 200 counts is reached, the seconds register is incremented by one. Also, when ten seconds is reached, tens-of-seconds is incremented. This counter continues to increment minutes, tens-of-minutes, hours, and tens-of-hours. Upon power-up, the display shows 12:00. When it is around 9:00, the leading hours digit is blanked. Time is adjusted by two push-button switches. When pressed, one increments the minutes register every second, while the other increments the hours register every second. The time data is stored in locations 09H-0EH.

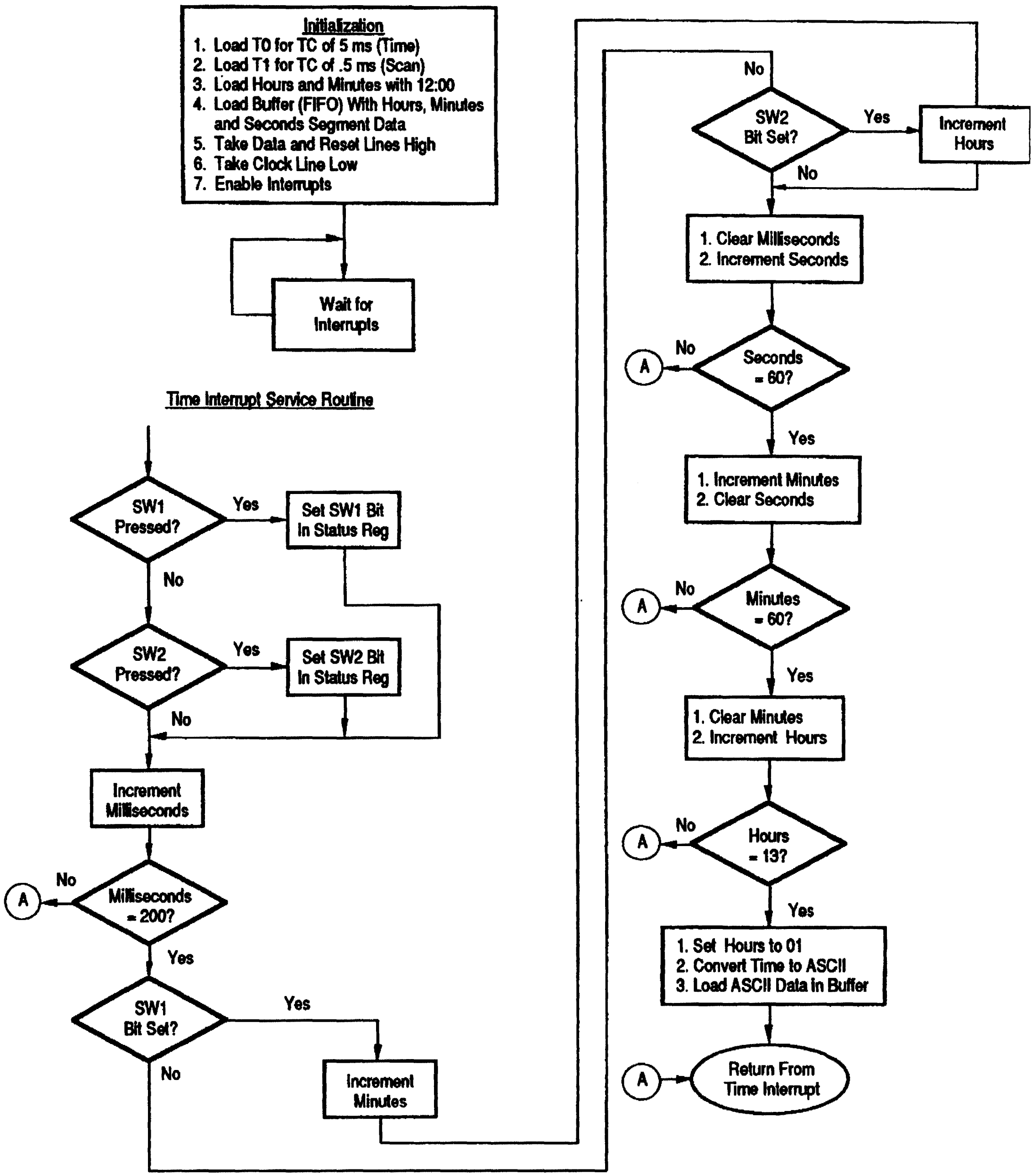


Figure 3a. Display Flowchart

THE SOFTWARE (Continued)

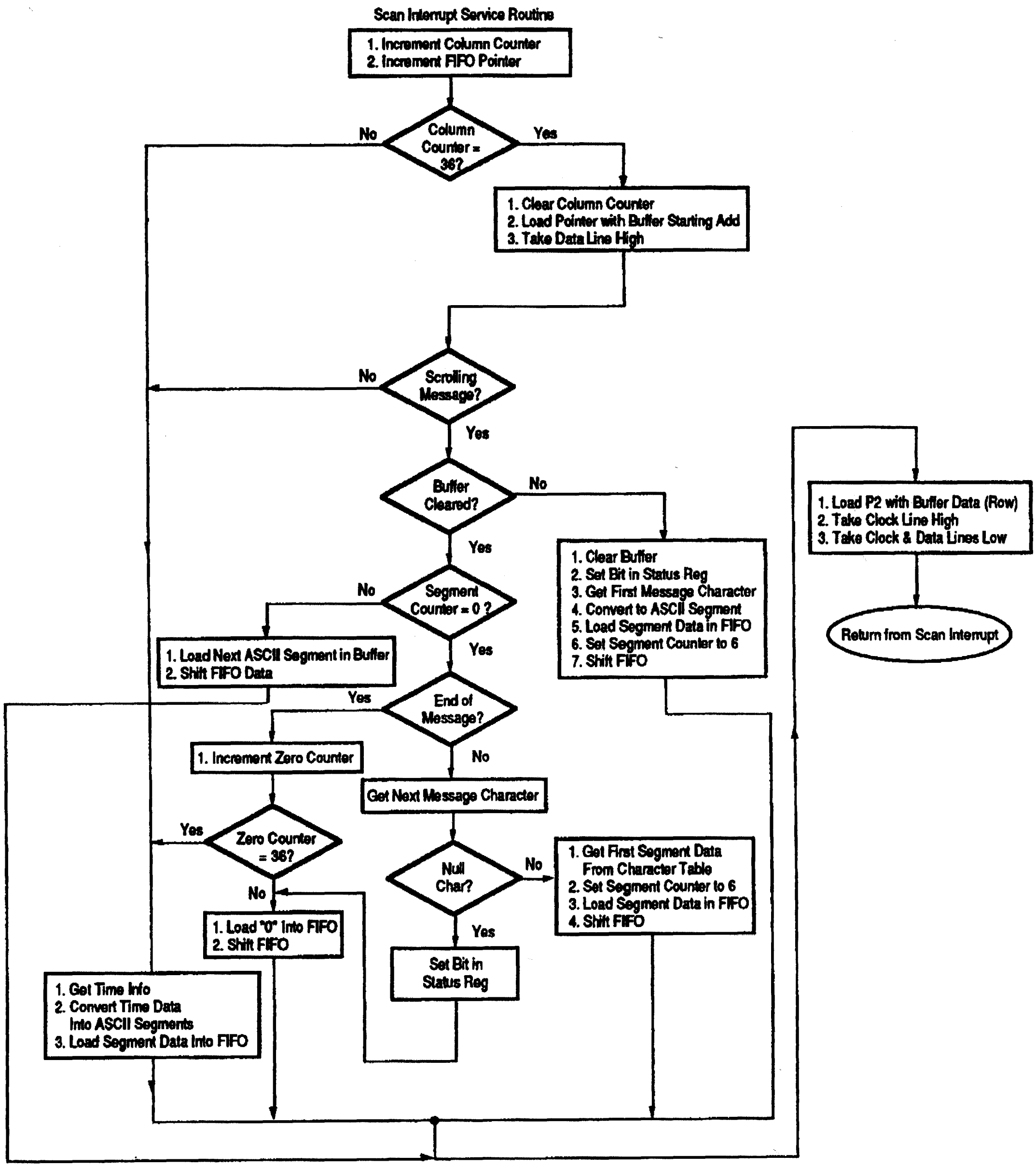


Figure 3b. Display Flowchart

At sixty-second intervals, the time display is blanked, and the internal message is scrolled across the display. The message is stored in an ASCII format. The individual ASCII characters index a look-up table, which converts the characters to a 6x7 format (first segment is a space). The software checks to see if all of the segments have been indexed at the beginning of the scan. If so, it then indexes the next character (Figures 4a and 4b).

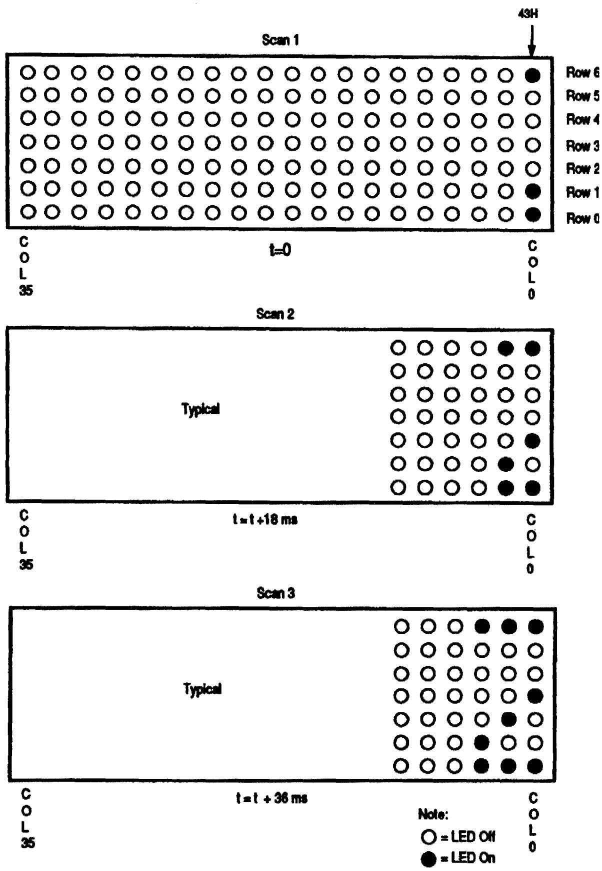


Figure 4a. Scrolling the Letter Z.

THE SOFTWARE (Continued)

For scrolling messages, the display buffer acts like a FIFO (First In - First Out). The FIFO is cleared at power-up. When the internal message is being indexed, the character segments are queued up in the FIFO. The FIFO size is determined by the size of the display. At the end of each scan, the next character segment is indexed, and is stored at the bottom of the FIFO. The character segments are then shifted up the FIFO one location. This process continues until the entire message is displayed. At this time, a 0 is loaded into the FIFO at the beginning of each scan allowing the columns trailing the message to blank out. As the display is being scanned, the byte at each FIFO location is output at P2 as each column is turned on. The scrolling effect is created by shifting the FIFO data at the start of each scan (Figure 5).

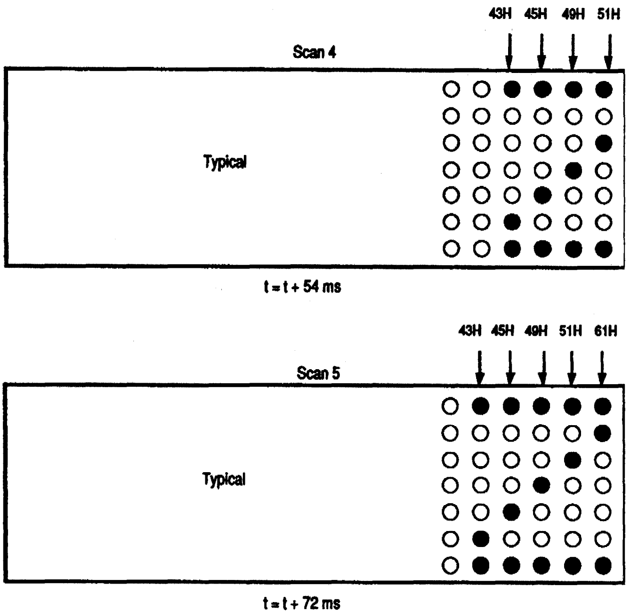


Figure 4b. Scrolling the Letter Z.

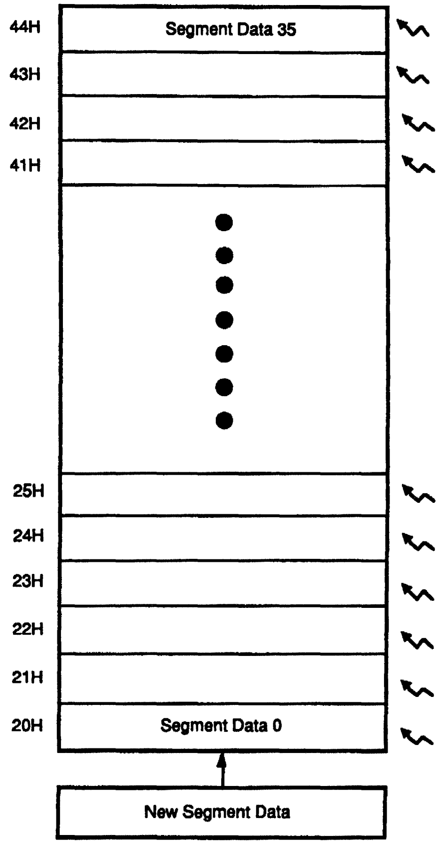


Figure 5. Shifting FIFO Data

APPENDIX

```
                              SCROLL1
                       LINE#  --- SOURCE ---
                              ;*************************************************************************;
                              ;                                                                         ;
                              ;   This is a scrolling LED display routine using the Zilog Z86C08, 'C17  ;
                              ;  18-pin CMOS processor. The processor's P2 port outputs the row data, and ;
                              ;  the column data is clocked out of P0 into cascaded shift registers. It ;
                              ;  has a real-time clock in software, and displays the time in hours, min- ;
                              ;  utes, and seconds. At every 60-second interval, it blanks the screen and ;
                              ;  displays an internal message. The message is stored in ROM, and can be up ;
                              ;  to 127 characters in length. After scrolling the message, the program re- ;
                              ;  sumes the time display, until the next 60 seconds.                     ;
                              ;   The size of the display is 36-columns long, enough to display six char- ;
                              ;  acters. The display can be made longer, but the refresh time may need ad- ;
                              ;  justing to eliminate flicker. Current refresh time is 500 microseconds, ;
                              ;  using a crystal frequency of 8.00 MHz.                                 ;
                              ;   There are two pushbutton switches that are read to adjust the hours and ;
                              ;  minutes. On power-up, the display will show 12:00.                     ;
                              ;   This program was written by Don Owen Newquist on 12-1-91.             ;
                              ;*************************************************************************;
00000000000000000010          WORK_REG        .equ    10h
  abs 00000000                address_hi      .equ    r0
  abs 00000001                address_lo      .equ    r1
  abs 00000000                address         .equ    rr0
  abs 00000002                pointer         .equ    r2
  abs 00000004                zero_count      .equ    r4
  abs 00000005                temp_1          .equ    r5
  abs 00000006                temp_2          .equ    r6
  abs 00000007                temp_3          .equ    r7
  abs 00000008                col_count       .equ    r8
  abs 00000009                seq_count       .equ    r9
00000000000000000000          TIME_REG        .equ    00h
  abs 00000005                millisec        .equ    r5
  abs 00000006                seconds         .equ    r6
  abs 00000007                minutes         .equ    r7
  abs 00000008                hours           .equ    r8
  abs 00000009                seconds_lo      .equ    r9
  abs 0000000a                seconds_hi      .equ    r10
  abs 0000000b                minutes_lo      .equ    r11
  abs 0000000c                minutes_hi      .equ    r12
  abs 0000000d                hours_lo        .equ    r13
  abs 0000000e                hours_hi        .equ    r14
  abs 0000000f                sw_count        .equ    r15
00000000000000000004          STATUS          .equ    %04
00000000000000000005          MILLISEC        .equ    %05
00000000000000000006          SECONDS         .equ    %06
00000000000000000007          MINUTES         .equ    %07
00000000000000000008          HOURS           .equ    %08
00000000000000000009          SECONDS_LO      .equ    %09
0000000000000000000a          SECONDS_HI      .equ    %0a
0000000000000000000b          MINUTES_LO      .equ    %0b
0000000000000000000c          MINUTES_HI      .equ    %0c
0000000000000000000d          HOURS_LO        .equ    %0d
0000000000000000000e          HOURS_HI        .equ    %0e
00000000000000000020          BUFFER          .equ    %20
                              ;
                              ;               STATUS  REG:    d4 d3 d2 d1 d0
                              ;                               |  |  |  |  |_ displaying message
                              ;                               |  |  |  |____ buffer cleared
```

```
                          ;                              |  |  |______ end of message
                          ;                              |  |_________ min sw pressed
                          ;                              |____________ hrs sw pressed
                          ;
00000000                                  .org   00
00000000 0000                             .word  00
00000002 0000                             .word  00
00000004 0000                             .word  00
00000006 0000                             .word  00
00000008 vvvv                             .word  time
0000000a vvvv                             .word  shift
0000000c                                  .org   000ch
                          ;****************************************************************************;
                          ;                   Initialization                                           ;
                          ;****************************************************************************;
0000000c 3110             init:           srp    #WORK_REG
0000000e 8f                               di                           ; disable int
0000000f e6f464                           ld     t0,#%64               ; 100 decimal
00000012 e6f5c9                           ld     pre0,#11001001b       ; set t0 for 5 mS period
00000015 e6f27d                           ld     t1,#125               ;
00000018 e6f313                           ld     pre1,#00010011b       ; set t1 for .5 mS period
0000001b e6f600                           ld     p2m,#0                ; outputs on p2
0000001e e6f701                           ld     p3m,#1                ; active on p2
00000021 e6f800                           ld     p01m,#0               ; outputs on p0
00000024 b000                             clr    p0                    ; p0 low
00000026 b0ef                             clr    sw_count              ; sw count = 0
00000028 e6f908                           ld     ipr,#00001000b        ; make irq5 > irq3
0000002b e6fb30                           ld     imr,#%30              ; enable irq4,irq5
0000002e e6ff80                           ld     spl,#%80              ; set stack pointer
00000031 e6f10f                           ld     tmr,#%0f              ; load and enable counters
00000034 2c04                             ld     pointer,#%04          ; point to time regs
00000036 fc0c                             ld     r15,#12               ; six locations
00000038 b1e2             clear_reg:      clr    @pointer              ; clear ram
0000003a 2e                               inc    pointer               ;
0000003b fafb                             djnz   r15,clear_reg         ; continue until all zero
0000003d d6vvvv                           call   clear_buffer          ; clear buffer
00000040 e60812                           ld     HOURS,#%12            ; start time at 12:00
00000043 d6vvvv                           call   load_time             ; load starting time
00000046 2c20                             ld     pointer,#BUFFER       ; start at top of buffer
00000048 e60003                           ld     p0,#00000011b         ; take data and clear hi
0000004b 9f               main_loop:      ei                           ; enable interrupts
0000004c 8bfd                             jr     main_loop             ;

                          ;****************************************************************************;
                          ;              This interrupt routine updates the time                       ;
                          ;****************************************************************************;
0000004e 70fd             time:           push   rp                    ; save current reg pointer
00000050 3100                             srp    #TIME_REG             ; point to time reg group
00000052 d6vvvv                           call   test_sw               ; look at time-set switches
00000055 5e                               inc    millisec              ; increment millisec reg
00000056 a6e5c8                           cp     millisec,#200         ; one second?
00000059 7dvvvv                           jp     ult,exit_time         ; exit if not
0000005c b0e5                             clr    millisec              ; set to zero
0000005e 760408                           tm     STATUS,#00001000b     ; sw 1 pressed?
00000061 6b**                             jr     z,test_sw2            ; no
00000063 060701                           add    MINUTES,#1            ;
00000066 4007                             da     MINUTES               ; convert to bcd
00000068 a60760                           cp     MINUTES,#%60          ; sixty minutes?
0000006b 7b**                             jr     ult,inc_seconds       ;
0000006d b007                             clr    MINUTES               ;
```

APPENDIX (Continued)

```
0000006f 8b**                       jr      inc_seconds         ;
00000071 760410     test_sw2:       tm      STATUS,#00010000b   ; sw 2 pressed?
00000074 6b**                       jr      z,inc_seconds       ; no
00000076 060801                     add     HOURS,#1            ;
00000079 4008                       da      HOURS               ;
0000007b a60813                     cp      HOURS,#%13          ; 1:00?
0000007e 7b**                       jr      ult,inc_seconds     ;
00000080 e60801                     ld      HOURS,#1            ;
00000083 06e601     inc_seconds:    add     seconds,#1          ; increment sec
00000086 40e6                       da      seconds             ; convert to bcd
00000088 a6e660                     cp      seconds,#%60        ; sixty seconds?
0000008b 7b**                       jr      ult,exit_time       ; no
0000008d 460401                     or      STATUS,#00000001b   ; set message flag
00000090 b0e6                       clr     seconds             ; set to zero
00000092 06e701                     add     minutes,#1          ; inc minutes
00000095 40e7                       da      minutes             ; convert to bcd
00000097 a6e760                     cp      minutes,#%60        ; sixty minutes?
0000009a 7b**                       jr      ult,exit_time       ; not yet
0000009c b0e7                       clr     minutes             ; set to zero
0000009e 06e801     set_hrs:        add     hours,#1            ; inc hours
000000a1 40e8                       da      hours               ; convert to bcd
000000a3 a6e813                     cp      hours,#%13          ; 1:00?
000000a6 7b**                       jr      ult,exit_time       ; exit
000000a8 8c01                       ld      hours,#1            ; set to 1:00
000000aa d6Wwww     exit_time:      call    time_convert        ; convert to individual chars
000000ad d6Wwww                     call    load_time           ; load new values into buffer
000000b0 50fd                       pop     rp                  ; return to orig reg pointer
000000b2 bf                         iret                        ; return from int

                    ;*****************************************************************************;
                    ;               This routine converts the seconds, minutes, and hours bcd     ;
                    ;               data into units and tens-of-units for displaying              ;
                    ;*****************************************************************************;
000000b3 e40609     time_convert:   ld      SECONDS_LO,SECONDS  ; transfer contents
000000b6 e4060a                     ld      SECONDS_HI,SECONDS  ;
000000b9 56090f                     and     SECONDS_LO,#%0f     ; keep only lower bits
000000bc f00a                       swap    SECONDS_HI          ; swap nibbles
000000be 560a0f                     and     SECONDS_HI,#%0f     ; keep only lower bits
000000c1 e4070b                     ld      MINUTES_LO,MINUTES  ; transfer contents
000000c4 e4070c                     ld      MINUTES_HI,MINUTES  ;
000000c7 560b0f                     and     MINUTES_LO,#%0f     ; keep only lower bits
000000ca f00c                       swap    MINUTES_HI          ; swap nibbles
000000cc 560c0f                     and     MINUTES_HI,#%0f     ; keep only lower bits
000000cf e4080d                     ld      HOURS_LO,HOURS      ; transfer contents
000000d2 e4080e                     ld      HOURS_HI,HOURS      ;
000000d5 560d0f                     and     HOURS_LO,#%0f       ; keep only lower bits
000000d8 f00e                       swap    HOURS_HI            ;
000000da 560e0f                     and     HOURS_HI,#%0f       ; keep only lower bits
000000dd af                         ret                         ; return

                    ;*****************************************************************************;
                    ;           This subroutine loads the time data into the RAM buffer          ;
                    ;*****************************************************************************;

000000de 70fd       load_time:      push    rp                  ; save current reg pointer
000000e0 3110                       srp     #WORK_REG           ; point to working reg
000000e2 ac09                       ld      r10,#%09            ; load starting time reg
000000e4 bc20                       ld      r11,#BUFFER         ; load starting buffer reg
000000e6 e3ca       load_table:     ld      r12,@r10            ; load contents
000000e8 0c**                       ld      address_hi,#^hb number_table; load hi address of table
```

```
000000ea 1c**                           ld      address_lo,#^lb number_table; load lo address of table
000000ec a6ec00                         cp      r12,#0                  ; is it zero?
000000ef 6b**                           jr      eq,no_index             ; if yes, don't step thru table
000000f1 a0e0           index_num:      incw    address                 ; step thru table
000000f3 a0e0                           incw    address                 ;
000000f5 a0e0                           incw    address                 ;
000000f7 a0e0                           incw    address                 ;
000000f9 a0e0                           incw    address                 ;
000000fb a0e0                           incw    address                 ;
000000fd caf2                           djnz    r12,index_num           ; index if not zero
000000ff cc06           no_index:       ld      r12,#6                  ; load no of segments
00000101 c3b0           load_time_reg:  ldci    @r11,@address           ; load into reg
00000103 cafc                           djnz    r12,load_time_reg       ; keep going if not zero
00000105 ae                             inc     r10                     ; inc reg location
00000106 a6ea0f                         cp      r10,#%0f                ; at ending reg?
00000109 7bdb                           jr      ult,load_table          ; go again
0000010b e62b3a                         ld      %2b,#%3a                ; put colon here
0000010e e6373a                         ld      %37,#%3a                ; and here too
00000111 a60e00                         cp      HOURS_HI,#0             ; zero?
00000114 eb**                           jr      ne,load_time_ret        ;
00000116 ac00                           ld      r10,#0                  ; load zeros on last 5 columns
00000118 bc3e                           ld      r11,#%3e                ; starting here
0000011a cc05                           ld      r12,#5                  ; blank out leading zero
0000011c f3ba           leading_loop:   ld      @r11,r10                ;
0000011e be                             inc     r11                     ; blank last five columns (hrs)
0000011f cafb                           djnz    r12,leading_loop        ; step thru ram
00000121 50fd           load_time_ret:  pop     rp                      ; return to time regs
00000123 af                             ret                             ; return to caller


                        ;**************************************************************************;
                        ;       This subroutine checks to see if the time-set switches are pressed.   ;
                        ;**************************************************************************;
00000124 a803           test_sw:        ld      r10,p3                  ; load sw data
00000126 60ea                           com     r10                     ; 1's complement
00000128 56ea03                         and     r10,#03                 ; mask off upper bits
0000012b 760301                         tm      p3,#1                   ; min pressed?
0000012e 6b**                           jr      z,test_hrs              ; no
00000130 fe                             inc     sw_count                ; inc counter
00000131 a6ef02                         cp      sw_count,#2             ; debouncd?
00000134 7b**                           jr      ult,exit_sw             ; not yet
00000136 460408                         or      STATUS,#00001000b       ; set bit
00000139 8b**                           jr      exit_sw                 ; exit
0000013b 760304         test_hrs:       tm      p3,#4                   ; hrs pressed?
0000013e 6b**                           jr      z,clear_sw              ; no
00000140 fe                             inc     sw_count                ; inc debounce counter
00000141 a6ef02                         cp      sw_count,#2             ; debounced?
00000144 7b**                           jr      ult,exit_sw             ; not yet
00000146 460410                         or      STATUS,#00010000b       ; set bit
00000149 af             exit_sw:        ret                             ; return to caller
0000014a 5604e7         clear_sw:       and     STATUS,#11100111b       ; reset sw status bits
0000014d b0ef                           clr     sw_count                ; reset debounce counter
0000014f af                             ret                             ; return

                        ;**************************************************************************;
                        ;       This is the timer interrupt routine.  When T1 hits TC, column data is ;
                        ;       shifted one.                                                       ;
                        ;**************************************************************************;
00000150 70fd           shift:          push    rp                      ; save reg pointer
00000152 3110                           srp     #WORK_REG               ; point to working reg
```

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APPENDIX (Continued)

```
00000154 2e                         inc     pointer             ; point to next location in ram
00000155 8e                         inc     col_count           ;
00000156 a6e824                     cp      col_count,#36       ; thirty-six columns?
00000159 7b**                       jr      ult,test_flag       ; end of screen?
0000015b b0e8                       clr     col_count           ; reset col number
0000015d 2c20                       ld      pointer,#BUFFER     ; start at beginning of buffer
0000015f 460002                     or      p0,#00000010b       ; take data line high
00000162 760401      test_flag:     tm      STATUS,#00000001b   ; time to scroll message?
00000165 6b**                       jr      z,continue          ; no, display time
00000167 d6Wwww                     call    load_message        ; load message data
0000016a 8b**                       jr      load_row            ; load row data
0000016c d6R000+00de, continue:     call    load_time           ; get time data
0000016f e352        load_row:      ld      temp_1,@pointer     ; load contents
00000171 60e5                       com     temp_1              ;
00000173 5902                       ld      p2,temp_1           ; out to port
00000175 460004      clock_it:      or      p0,#00000100b       ; take clock hi
00000178 560001                     and     p0,#00000001b       ; take clock and data low
0000017b 50fd                       pop     rp                  ; restore reg pointer
0000017d bf                         iret                        ;
                     ;*****************************************************************************;
                     ;              This routine loads the message into the buffer                 ;
                     ;*****************************************************************************;
0000017e 760402      load_message:  tm      STATUS,#00000010b   ; clear buffer?
00000181 eb**                       jr      nz,reg_scroll       ;
00000183 d6Wwww                     call    clear_buffer        ; clear contents of buffer
00000186 460402                     or      STATUS,#00000010b   ; set bit
00000189 0c**                       ld      address_hi,#^hb mess_beg   ;
0000018b 1c**                       ld      address_lo,#^lb mess_beg   ;
0000018d d6Wwww                     call    get_ascii           ; get first character
00000190 9c06                       ld      seg_count,#6        ; start out with six segs
00000192 8b**                       jr      load_next_seg       ;
00000194 a6e900      reg_scroll:    cp      seg_count,#0        ; six segments loaded?
00000197 eb**                       jr      ne,load_next_seg    ; no
00000199 760404                     tm      STATUS,#00000100b   ; end of message?
0000019c 6b**                       jr      z,load_next_char    ; load next ascii char
0000019e 6c00                       ld      temp_2,#0           ;
000001a0 d6Wwww                     call    load_fifo           ; load data
000001a3 4e                         inc     zero_count          ; inc no of locations cleared
000001a4 a6e424                     cp      zero_count,#36      ; 36 locations yet?
000001a7 7b**                       jr      ult,scroll_return   ; load segment data
000001a9 b004                       clr     STATUS              ; display time now
000001ab b0e4                       clr     zero_count          ; clear counter
000001ad 8b**                       jr      scroll_return       ; return
000001af 9c06        load_next_char: ld     seg_count,#6        ; load 6 segments/character
000001b1 a0e0                       incw    address             ; point to next ascii char
000001b3 d6Wwww                     call    get_ascii           ; get next character
000001b6 c26c        load_next_seg: ldc     temp_2,@rr12        ; load seg from ascii table
000001b8 d6Wwww                     call    load_fifo           ; shift the data
000001bb a0ec                       incw    rr12                ; point to next seg in table
000001bd 00e9                       dec     seg_count           ; decrement segment count
000001bf af          scroll_return: ret                         ;

                     ;*****************************************************************************;
                     ;       This subroutine loads and shifts the RAM buffer                       ;
                     ;*****************************************************************************;
000001c0 fc24        load_fifo:     ld      r15,#36             ; load number of columns
000001c2 2c20                       ld      pointer,#BUFFER     ; load starting buffer reg
000001c4 e372        shift_fifo:    ld      temp_3,@pointer     ; get data
000001c6 f326                       ld      @pointer,temp_2     ; load new data
000001c8 68e7                       ld      temp_2,temp_3       ; transfer bytes
```

```
000001ca 2e                                inc     pointer             ; next buffer address
000001cb faf7                              djnz    r15,shift_fifo      ; load all columns
000001cd af                                ret                         ; return to caller
                     ;*************************************************************************;
                     ;  This subroutine indexes the character table and fetches the segment data. ;
                     ;*************************************************************************;
000001ce cc**        get_ascii:            ld      r12,#^hb char_table ; load starting add of table
000001d0 dc**                              ld      r13,#^lb char_table ;
000001d2 c2ea                              ldc     r14,@rr10           ; load ascii data
000001d4 a6ee00                            cp      r14,#0              ; end of message?
000001d7 eb**                              jr      ne,load_next        ; no
000001d9 460404                            or      STATUS,#00000100b   ; set bit to mark mess end
000001dc 8b**                              jr      mess_return         ; return
000001de 26ee20      load_next:            sub     r14,#%20            ; subtract 20h
000001e1 a6ee00                            cp      r14,#0              ; is it a space?
000001e4 6b**                              jr      eq,mess_return      ; if yes, don't index table
000001e6 a0ec        index_table:          incw    rr12                ; index table
000001e8 a0ec                              incw    rr12                ;
000001ea a0ec                              incw    rr12                ;
000001ec a0ec                              incw    rr12                ;
000001ee a0ec                              incw    rr12                ;
000001f0 a0ec                              incw    rr12                ;
000001f2 eaf2                              djnz    r14,index_table     ; keep going if not zero
000001f4 af          mess_return:          ret                         ;

                     ;*************************************************************************;
                     ;             This subroutine clears the RAM buffer.                      ;
                     ;*************************************************************************;
000001f5 fc24        clear_buffer:         ld      r15,#36             ; get no of columns
000001f7 2c20                              ld      pointer,#BUFFER     ; starting point of buffer
000001f9 b1e2        clear_loop:           clr     @pointer            ; clear contents
000001fb 2e                                inc     pointer             ; next location
000001fc fafb                              djnz    r15,clear_loop      ;  till out of columns
000001fe af                                ret                         ; return to caller

                     ;*************************************************************************;
                     ;          Message data area. Message can be up to 80 ASCII characters    ;
                     ;*************************************************************************;
00000200                                   .org    200h
00000200             mess_beg:
00000200 5448495320444953                  .asciz  'THIS DISPLAY IS POWERED BY ZILOG!'
00000208 504c415920495320
00000210 504f574552454420
00000218 4259205a494c4f47
00000220 2100

                     ;*************************************************************************;
                     ;        This is the ASCII character look-up table.                       ;
                     ;*************************************************************************;
00000280                                   .org    280h
00000280             char_table:
00000280 000000000000                      .byte   0,0,0,0,0,0                 ; space
00000286 0000007d00                        .byte   0,0,0,7DH,0                 ; !
0000028b 000070007000                      .byte   0,0,70H,0,70H,0             ; "
00000291 00147f147f14                      .byte   0,14H,7FH,14H,7FH,14H       ; #
00000297 00122a7f2a24                      .byte   0,12H,2AH,7FH,2AH,24H       ; $
0000029d 006264081323                      .byte   0,62H,64H,08H,13H,23H       ; %
000002a3 003649350205                      .byte   0,36H,49H,35H,02H,05H       ; &
000002a9 000000700000                      .byte   0,00,00,70H,00,00           ; '
000002af 001c22410000                      .byte   0,1CH,22H,41H,0,0           ; (
```

APPENDIX (Continued)

```
000002b5 00000041221c                   .byte   0,0,0,41H,22H,1CH       ; )
000002bb 0022147f1422                   .byte   0,22H,14H,7FH,14H,22H   ; *
000002c1 0008083e0808                   .byte   0,08H,08H,3EH,08H,08H   ; +
000002c7 000001060000                   .byte   0,0,1,6,0,0             ; ,
000002cd 000808080808                   .byte   0,8,8,8,8,8             ; -
000002d3 000000010000                   .byte   0,0,0,1,0,0             ; .
000002d9 000204081020                   .byte   0,2,4,8,10H,20H         ; /
                      ;numbers
000002df 003e4549513e number_table:     .byte   0,3EH,45H,49H,51H,3EH   ; 0
000002e5 0000217f0100                   .byte   0,0,21H,7FH,01,0        ; 1
000002eb 002345494931                   .byte   0,23H,45H,49H,49H,31H   ; 2
000002f1 004241495966                   .byte   0,42H,41H,49H,59H,66H   ; 3
000002f7 000c14247f04                   .byte   0,0CH,14H,24H,7FH,04H   ; 4
000002fd 00725151514e                   .byte   0,72H,51H,51H,51H,4EH   ; 5
00000303 001e29494946                   .byte   0,1EH,29H,49H,49H,46H   ; 6
00000309 004047485060                   .byte   0,40H,47H,48H,50H,60H   ; 7
0000030f 003649494936                   .byte   0,36H,49H,49H,49H,36H   ; 8
00000315 003149494a3c                   .byte   0,31H,49H,49H,4AH,3CH   ; 9
                      ;      MORE SPECIAL CHARACTERS
0000031b 000000140000                   .byte   0,0,0,14H,0,0           ; :
00000321 000001160000                   .byte   0,0,1,16H,0,0           ; ;
00000327 000814224100                   .byte   0,8,14H,22H,41H,0       ; <
0000032d 001414141414                   .byte   0,14H,14H,14H,14H,14H   ; =
00000333 000041221408                   .byte   0,0,41H,22H,14H,08H     ; >
00000339 0020404d5020                   .byte   0,20H,40H,4DH,50H,20H   ; ?
                      ;      AT SIGN AND UPPERCASE LETTERS              ;
0000033f 003e415d4d39                   .byte   0,3EH,41H,5DH,4DH,39H   ; @
00000345 001f2444241f                   .byte   0,1FH,24H,44H,24H,1FH   ; A
0000034b 007f49494936                   .byte   0,7FH,49H,49H,49H,36H   ; B
00000351 003e41414122                   .byte   0,3EH,41H,41H,41H,22H   ; C
00000357 007f4141413e                   .byte   0,7FH,41H,41H,41H,3EH   ; D
0000035d 007f49494941                   .byte   0,7FH,49H,49H,49H,41H   ; E
00000363 007f48484840                   .byte   0,7FH,48H,48H,48H,40H   ; F
00000369 003e41414547                   .byte   0,3EH,41H,41H,45H,47H   ; G
0000036f 007f0808087f                   .byte   0,7FH,08H,08H,08H,7FH   ; H
00000375 0000417f4100                   .byte   0,00H,41H,7FH,41H,00H   ; I
0000037b 00020101017e                   .byte   0,02H,01H,01H,01H,7EH   ; J
00000381 007f08142241                   .byte   0,7FH,08H,14H,22H,41H   ; K
00000387 007f01010101                   .byte   0,7FH,01H,01H,01H,01H   ; L
0000038d 007f2018207f                   .byte   0,7FH,20H,18H,20H,7FH   ; M
00000393 007f1008047f                   .byte   0,7FH,10H,08H,04H,7FH   ; N
00000399 003e4141413e                   .byte   0,3EH,41H,41H,41H,3EH   ; O
0000039f 007f48484830                   .byte   0,7FH,48H,48H,48H,30H   ; P
000003a5 003e4145423d                   .byte   0,3EH,41H,45H,42H,3DH   ; Q
000003ab 007f484c4a31                   .byte   0,7FH,48H,4CH,4AH,31H   ; R
000003b1 003249494926                   .byte   0,32H,49H,49H,49H,26H   ; S
000003b7 0040407f4040                   .byte   0,40H,40H,7FH,40H,40H   ; T
000003bd 007e0101017e                   .byte   0,7EH,01H,01H,01H,7EH   ; U
000003c3 007c0201027c                   .byte   0,7CH,02H,01H,02H,7CH   ; V
000003c9 007f020c027f                   .byte   0,7FH,02H,0CH,02H,7FH   ; W
000003cf 006314081463                   .byte   0,63H,14H,08H,14H,63H   ; X
000003d5 0060100f1060                   .byte   0,60H,10H,0FH,10H,60H   ; Y
000003db 004345495161                   .byte   0,43H,45H,49H,51H,61H   ; Z
000003e1 007f7f414141                   .byte   0,7FH,7FH,41H,41H,41H   ; [
000003e7 002010080402                   .byte   0,20H,10H,08H,04H,02H   ; \
000003ed 004141417f7f                   .byte   0,41H,41H,41H,7FH,7FH   ; ]
000003f3 000408100804                   .byte   0,04H,08H,10H,08H,04H   ; ^
000003f9 000101010101                   .byte   0,01H,01H,01H,01H,01H   ; -

                                        .end
```

INTERFACING LCDs TO THE Z8®

By trading hardware approaches for software solutions, interfacing a Z8 Microcontroller to a M1641 LCD module becomes a practical and simplified design methodology.

INTRODUCTION

There has been an increasing demand for interfacing Liquid Crystal Displays (LCDs) to low-end microcontrollers in recent years. Unfortunately, little has been offered to address real-world applications and to help the design engineer understand how to make LCDs work. This App Note (Application Note) explains and shows a software method of interfacing a Z8 to an LCD module. The challenge to the programmer is the fixed amount of ROM space. Although almost any Z8 device is usable, the CCP™ (Consumer Controller Processor) Family is referenced; For example, the Z86C40, Z86C96/61, etc.

OVERVIEW

Since the Z8 architecture is so flexible, it would be very difficult to include all possible applications in the spec sheet example Figures and Tables. Since the purpose of this App Note is to reduce the complexity of interfacing Z8s with LCDs, the software routines are intended to be "cut and paste," so choose the ones that meet your needs (caution, do not forget the initialization routines). Also, remember that not all possible functions inside the LCD were utilized. In many applications, it is only necessary to transfer ASCII for display in 16-character chunks. For messages containing more than 16 characters, the message may be broken down into two 16-character fields, each alternately being displayed. The details on special functions are in the manufacturers data sheets.

M1641 LCD MODULE

The M1641 LCD Module is a 1-line by 16-character display with an on-board controller; the HD44780. The HD44780 divides the 16 characters into two lines of eight characters each. Even though this is a two-line device, physically, all characters appear on the same line. The controller has an on-board character generator in ROM capable of displaying 192 ASCII characters, along with eight user programmable characters. All characters are displayed in a 5x7 font.

INTERFACE

The LCD module can be connected to either an 8-bit or 4-bit data bus. There are three control lines: RS, R/W, and E (Enable). The RS line selects either an instruction (Low), or data (High). The R/W line (write active Low), allows data to be written to the LCD (Low) or read from the LCD (High).

The Enable line (E) is used to latch data to and from the LCD (Figure 1a and 1b and Table 1a and 1b). The V1c line is used for adjusting the contrast, but for most applications may be tied to ground.

Table 1a. Read Characteristics

Item		Symbol	Standard Min.	Standard Max.	Unit
Enable cycle time		$t_{CYC}E$	1000	-	ns
Enable pulse width	High level	PW_{EH}	450	-	ns
Enable rise and fall time		t_{Er}, t_{Ef}	-	25	ns
Setup time	RS, R/W—E	t_{AS}	140	-	ns
Address hold time		t_{AH}	10	-	ns
Data delay time		t_{DDR}	-	320	ns
Data hold time		t_H	20	-	ns

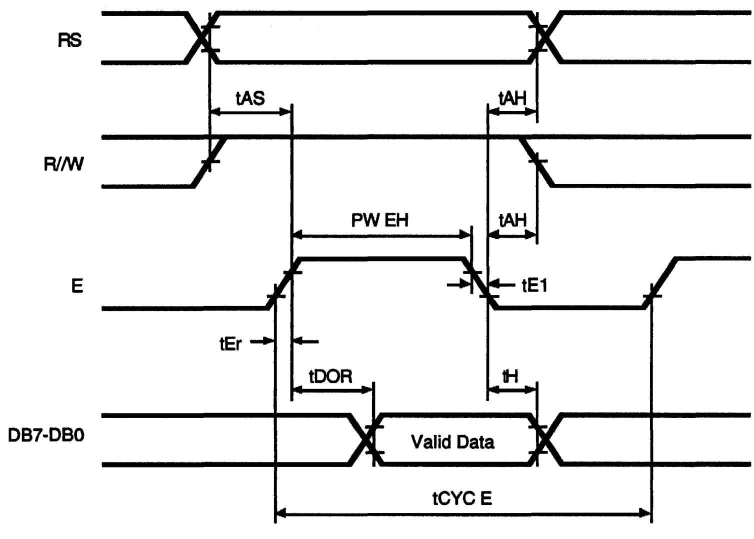

Figure 1a. LCD Read* Timing

Note:
*V_{DD}=5.0V ±5%, V_{SS}=0V, T_A=0°C to 50°C

Table 1b. Write Characteristics

Item		Symbol	Standard Min.	Standard Max.	Unit
Enable cycle time		$t_{CYC}E$	1000	-	ns
Enable pulse width	High level	PW_{EH}	450	-	ns
Enable rise and fall time		t_{Er}, t_{Ef}	-	25	ns
Setup time	RS, R/W—E	t_{AS}	140	-	ns
Address hold time		t_{AH}	10	-	ns
Data delay time		t_{DDR}	195	-	ns
Data hold time		t_H	10	-	ns

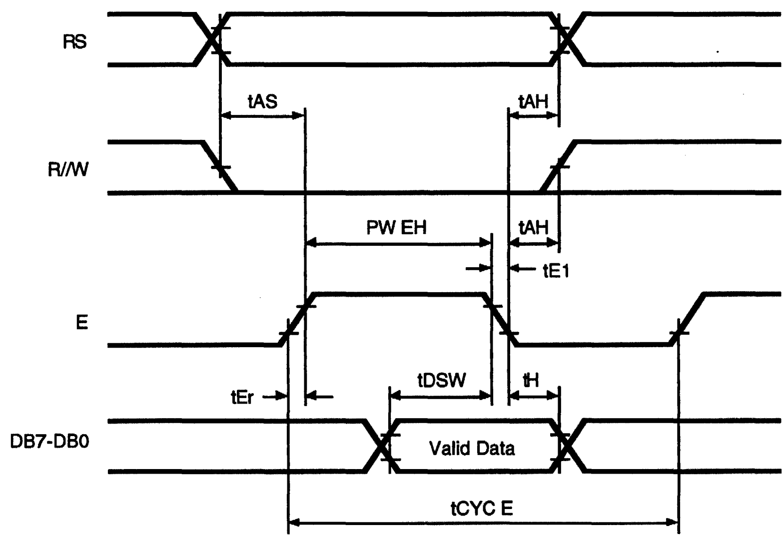

Figure 1b. LCD Write* Timing

Note:
*V_{DD}=5.0V ±5%, V_{SS}=0V, T_A=0°C to 50°C

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INTERFACE (Continued)

V_{SS} is tied to ground while V_{CC} is tied to the +5 Volt supply. Unless your application is heavily "I/O bound," it is easiest to use one of the Z8's 8-bit ports for data, and use two lines from Port 3 for control. Figure 2 shows a typical Z8 interface.

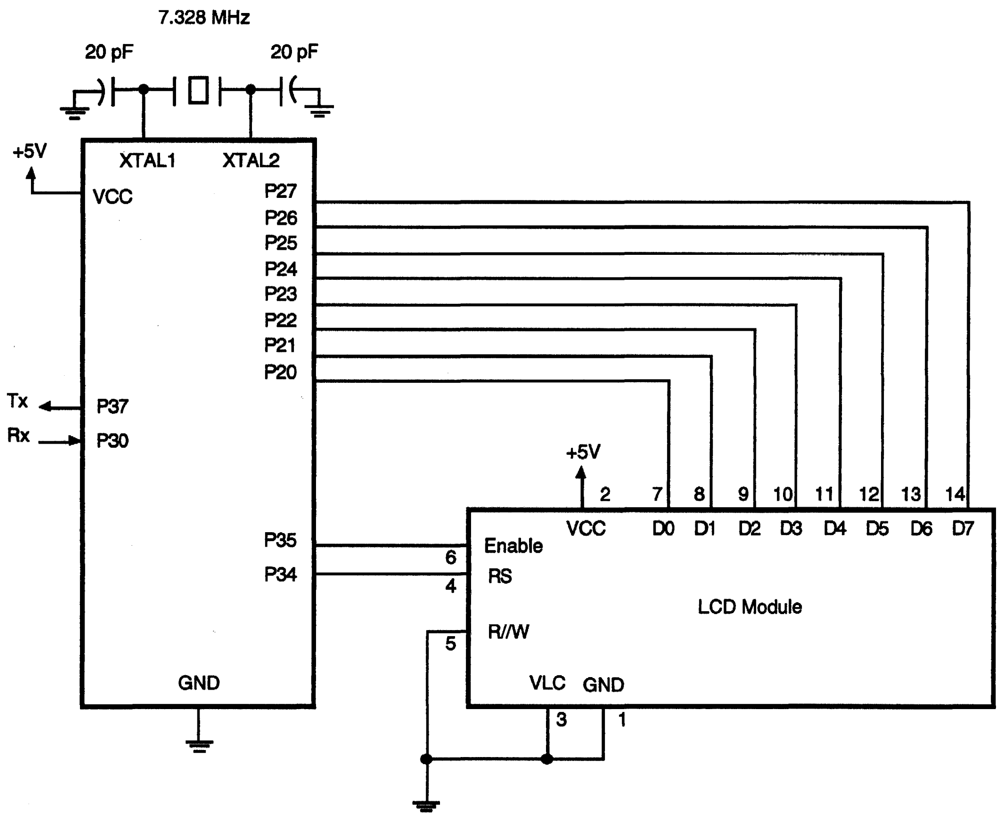

Figure 2. Typical Z8/LCD Interface

INITIALIZATION

After power up, initialize the LCD before sending data. Note that the LCD module is very slow. Therefore, it is necessary to write a delay loop program in between instructions. Again, the LCD can be configured for either 8-bit or 4-bit data transfer. When operating in 4-bit mode, the upper nibble gets transferred first, followed by the lower nibble.

Table 2 shows complete instruction codes. In order to write the instruction codes to the LCD module, the RS line must be Low. Figure 3 shows an initialization sequence for an 8-bit transfer operation. The starting address for the DD RAM is 8OH for the first eight characters. For the next eight characters, the starting address is COH. If the DD RAM is programmed for auto increment, then the DD RAM address is automatically incremented after each character write.

Table 2. LCD Instructions Codes

Instruction	Set		Instruction Code								Description	Execution Time (when fCP or fOSC is 250 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display memory and returns the cursor to the home position (Address 0).	82 µs ~ 1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	40 µs ~ 1.6 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40 µs ~ 1.64 ms
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	(D) is display ON/OFF control, memory remains unchanged in OFF condition. (C) cursor ON/OFF (B) blinking cursor.	40 µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40 µs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N), and character font (F).	40 µs
Set CG RAM Address	0	0	0	1	ACG						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 µs
Set DD RAM Address	0	0	1	ADD							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 µs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents.	1 µs
Write Data to CG or DD RAM	1	0	Write Data								Writes into DD RAM or CG RAM.	40 µs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 µs

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INITIALIZATION (Continued)

Notes to the previous table:

1. *Doesn't Matter

2. DD RAM :	Display data RAM	I/D=1:	Increment	C=1:	Cursor On	R/L=1:	Right shift
CG RAM:	Character generator RAM	I/D=0:	Decrement	C=0:	Cursor Off	R/L=0:	Left shift
A_{CG}:	CG RAM address	S=1:	Display shift	B=1:	Blink ON	DL=1:	8 bits
A_{DD}:	DD RAM address Corresponds to cursor address	S=0:	No display shift	B=0:	Blink OFF	DL=0:	4 bits
		D=1:	Display ON	S/C=1:	Display shift	N=1:	2 lines (M1641)
AC:	Address counter used for both of DD and CG RAM address	D=0:	Display OFF	S/C=0:	Cursor movement	N=0:	1 line (M24111 & L4041)
				BF=1:	Internal operation in progress	F=1:	5x10 dot-matrix (M24111 & L4041)
				BF=0:	Instruction can be accepted	F=0:	5x7 dot-matrix

3. Execution times in Table 2 indicate the maximum values when operating frequency is 250 kHz.
4. When f_{OSC} is 270 kHz: 40 µ s x 250/270 = 37 µ s

Display Initialization

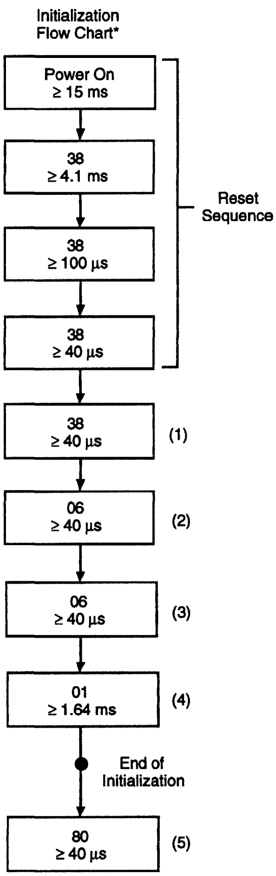
Each time the module is turned on or reset, an initialization procedure must be executed. The procedure consists of sending a sequence of hex codes from the microprocessor or parallel I/O port. The initialization sequence turns on the cursor, clears the display, and sets the module onto an auto-increment mode.

The initial hex code 30, 34, or 38 is sent two or more times to ensure the module enters the 8-bit or 4-bit data mode. All the initialization sequences are performed under the condition of Register Select (RS) = 0 (Low) and Read/Write (R/W) = 0 (Low).

4-bit data bus microcontroller may operate the display module by sending the initialization sequence in 4-bit format. Since 4-bit operation requires the data to be sent twice over the higher 4-bit bus lines (D4-D7), memory requirements are doubled.

Example for the module with 5x7 character format under 8-bit data transfer.

Applicable modules: M1641, L1651, M1632, L1642, L1652, L2012, L2432, L4042, L1614, L2014, M4024



	Hex Code*	D7	D6	D5	D4	D3	D2	D1	D0	Instructions
(1)	38	0	0	1	1	1	0	0	0	Function Set (D7–D5); 8-bit Data Length (D4); 2 Line (D3); 5x7 Dot Format (D2)
(2)	06	0	0	0	0	0	1	1	0	Entry Mode Set (D7–D2); Increment one (D1); No Shift (D0)
(3)	0E	0	0	0	0	1	1	1	0	Display ON/OFF Control (D7–D3); Display ON (D0); Cursor ON (D1); Blink OFF (D2)
(4)	01	0	0	0	0	0	0	0	1	Display Clear
(5)	80	1	0	0	0	0	0	0	0	DD RAM Address Set (D7); 1st Digit (D6–D0)

*All addresses in Hexidecimal

Figure 3. Initialization Sequence

Notes:
1. Both RS and R/W terminals shall be "0" in this sequence.
2. RS, R/W and Data are latched at the falling edge of the Enable signal, (falling edge is typically 10 ns; MAX: 25 ns).
3. M4024 has to be initialized on E1 and E2, respectively. Refer to (2) in Sample Programs.

LCD/Z8 PROGRAM

Appendix A (Listing 1) has all the routines for communicating to an LCD module. For this App Note exercise, there is no cursor, auto-increment for the DD RAM address, and no display shift. Since there is no read instruction from the LCD, the R/W is tied Low.

Transferring ASCII to the Z8 via the UART requires buffering before writing to the LCD, since the LCD is not able to keep up with the Z8 at high baud rates. Therefore, the 16 ASCII are first stored within one of the working register groups, then transferred to the LCD. Actually, the Z8 has the ability to store several messages within the register file. This is useful for applications that require a handful of commonly used messages that are downloaded from a master MPU after initialization.

Of course, messages can be stored in the internal Z8 ROM space. Since the program occupies less than 750 bytes, there is plenty of room to display other custom messages.

This program allows the Z8 user to interface to a 1-line by 16-character Liquid Crystal Display (LCD). It includes a routine to load serial data from the UART to the register file, then out to the display. For displaying "canned" messages send a control character followed by the message number. Another control character is used for accepting ASCII from the outside world followed by sixteen ASCII characters.

This program is intended to be used with the industry-standard 1-line by sixteen-character LCD module (Seiko M1641, etc.). Certain modifications are necessary for 2-line modules (see manufacturers data sheets).

APPENDIX A
LCD Program
(Listing 1)

```
;           M1641 Pinout                                                      ;
;           ------------                                                      ;
;            1 - Vss                                                          ;
;            2 - Vdd                                                          ;
;            3 - Vlc                                                          ;
;            4 - RS                                                           ;
;            5 - R//W                                                         ;
;            6 - E                                                            ;
;            7 - DB0                                                          ;
;            8 - DB1                                                          ;
;            9 - DB2                                                          ;
;           10 - DB3                                                          ;
;           11 - DB4                                                          ;
;           12 - DB5                                                          ;
;           13 - DB6                                                          ;
;           14 - DB7                                                          ;
;-----------------------------------------------------------------------------;
CUR_HOME  .EQU    02H
DIS_CLEAR  .EQU   01H
CG_RAM    .EQU    40H
DD_RAM_1  .EQU    80H
DD_RAM_2  .EQU    0C0H
PORT_2    .EQU    02H
PORT_0    .EQU    00H
CONST_1   .EQU    1FH
CONST_2   .EQU    0FFH
POLL_SIO  .EQU    08H
IRQ3_RES  .EQU    0F7H
STACK     .EQU    80H
CLOCK_LO  .EQU    0FEH
CLOCK_HI  .EQU    01H
RS_LOW    .EQU    0FDH
RS_HIGH   .EQU    02H
E_LOW     .EQU    0F8H
E_HIGH    .EQU    04H
MYREG_0   .EQU    00H
8_BITS    .EQU    38H
AI_NS     .EQU    06H
DO_NC     .EQU    0CH
BUFF_BEG  .EQU    10H
BUFF_END  .EQU    20H
MASK      .EQU    01H

MYREG2    .EQU    20H
;
          .ORG       0000H
          .WORD      0,0,0
          .word      RXD
          .word      0
          .word      0
          .org       000ch
```

APPENDIX A (Continued)

```
;-----------------------------------------------------------------------;
;                    INITIALIZATION                                     ;
;-----------------------------------------------------------------------;
BEGIN:
         DI                            ; DISABLE INTERRUPTS
         SRP    #MYREG_0               ; POINT TO REGS 10 - 1F HEX
         LD     SPL,#STACK             ; INITIALIZE STACK POINTER
         LD     P01M,#00               ; CONFIGURE P0 FOR OUTPUT
         LD     P2M,#0                 ; CONFIGURE P2 FOR OUTPUT
         LD     P3M,#%41               ; ACTIVE PULL-UPS FOR P2
         LD     IPR,#%28               ; IRQ3 IS HIGHEST
         LD     IMR,#%88               ; ENABLE IRQ3
         LD     IRQ,#0                 ; CLEAR IRQ
         CALL   LCD_INIT               ; INITIALIZE THE LCD
         EI                            ; ENABLE INTERRUPTS
ENABLE:
         JR     ENABLE                 ; WAIT FOR INTERRUPTS
;
;-----------------------------------------------------------------------;
;         INITIALIZE THE LIQUID CRYSTAL DISPLAY                         ;
;-----------------------------------------------------------------------;
LCD_INIT:
         AND    PORT_0,#RS_LOW         ; MAKE SURE P3-4 IS 0
         LD     PORT_2,#00             ; MAKE P2 ZERO
         OR     PORT_0,#E_HIGH         ; TAKE ENABLE HIGH
         AND    PORT_0,#E_LOW          ; BRING ENABLE BACK LOW
         CALL   WAIT_1                 ; WAIT AWHILE
         LD     PORT_2,#8_BITS         ; SET DATA LENGTH FOR 8 BITS
         OR     PORT_0,#E_HIGH         ; TAKE ENABLE HIGH
         AND    PORT_0,#E_LOW          ; BRING ENABLE BACK LOW
         CALL   WAIT_1                 ; WAIT AWHILE
         OR     PORT_0,#E_HIGH         ; TAKE ENABLE HIGH
         AND    PORT_0,#E_LOW          ; BRING ENABLE BACK LOW
         CALL   WAIT_1                 ; WAIT AWHILE
         OR     PORT_0,#E_HIGH         ; TAKE ENABLE HIGH
         AND    PORT_0,#E_LOW          ; BRING ENABLE BACK LOW
         CALL   WAIT_1                 ; WAIT AWHILE
         LD     PORT_2,#DO_NC          ; TURN ON DISPLAY, NO CURSOR!
         OR     PORT_0,#E_HIGH         ; TAKE ENABLE HIGH
         AND    PORT_0,#E_LOW          ; BRING ENABLE BACK LOW
         CALL   WAIT_1                 ; WAIT AWHILE
         LD     PORT_2,#AI_NS          ; ENTRY MODE: INC ADDRESS,NO SHIFT
         OR     PORT_0,#E_HIGH         ; TAKE ENABLE HIGH
         AND    PORT_0,#E_LOW          ; BRING ENABLE BACK LOW
         CALL   WAIT_1                 ; WAIT AWHILE
```

```
LCD_RES:
        LD      PORT_2,#DIS_CLEAR ; CLEAR DISPLAY
        OR      PORT_0,#E_HIGH    ; TAKE ENABLE HIGH
        AND     PORT_0,#E_LOW     ; BRING ENABLE BACK LOW
        CALL    WAIT_1            ; WAIT AWHILE
        LD      PORT_2,#CUR_HOME  ; CURSOR HOME
        OR      PORT_0,#E_HIGH    ; TAKE ENABLE HIGH
        AND     PORT_0,#E_LOW     ; BRING ENABLE BACK LOW
        CALL    WAIT_1            ; WAIT AWHILE
        LD      PORT_2,#CG_RAM    ; SET CG RAM
        OR      PORT_0,#E_HIGH    ; TAKE ENABLE HIGH
        AND     PORT_0,#E_LOW     ; BRING ENABLE BACK LOW
        CALL    WAIT_2            ; WAIT AWHILE
        LD      PORT_2,#DD_RAM_1  ; SET DD RAM
        OR      PORT_0,#E_HIGH    ; TAKE E HIGH
        AND     PORT_0,#E_LOW     ; TAKE E LOW
        CALL    WAIT_2            ; WAIT AWHILE
        RET
;---------------------------------------------------------------------------;
;         RECEIVE INTERRUPT ROUTINE - RECEPTION OF 1B HEX IS FOLLOWED       ;
;         BY SIXTEEN ASCII CHARACTERS TO BE DISPLAYED ON LCD MODULE.        ;
;         RECEPTION OF 1C HEX, FOLLOWED BY A MESSAGE NUMBER (e.g. 0-9),     ;
;         DISPLAYS ONE OF THE INTERNAL MESSAGES.                            ;
;---------------------------------------------------------------------------;
RXD:
        DI                        ; DISABLE INTERRUPTS
        PUSH    RP                ; SAVE REG POINTER
        SRP     #MYREG2           ; POINT TO WORKING REGS
        LD      R7,SIO            ; GET BYTE FROM SIO
        CP      R7,#%1B           ; ESCAPE CHARACTER?
        JR      NE,FS             ; NO, TRY FS CHARACTER
        CALL    ASCII             ; GET READY FOR TEXT
        JR      RXDOUT            ; EXIT
FS:
        CP      R7,#%1C           ; IF FS, THEN CANNED MESSAGE
        JR      NE,RXDOUT         ; IF NOT, EXIT
        CALL    INT_MSG           ; CALL CANNED MESSAGE ROUTINE
RXDOUT:
        POP     RP                ; RESTORE POINTER
        IRET                      ; RETURN FROM INTERRUPT
;
;---------------------------------------------------------------------------;
;       ACCESS ONE OF THE INTERNAL LCD MESSAGES                             ;
;---------------------------------------------------------------------------;
INT_MSG:
        PUSH    RP                ; SAVE CURRENT REG POINTER
        SRP     #MYREG_0          ; POINT TO REG 0 - FH
        PUSH    IMR               ; SAVE CURRENT IMR
        DI                        ; DISABLE INTERRUPTS
        LD      IMR,#%20          ; ENABLE IRQ5 ONLY
        CLR     IRQ               ; CLEAR ANY PENDING
        EI                        ; ENABLE INTERRUPTS
```

APPENDIX A (Continued)

```
MSG_NUM:
          TM      IRQ,#POLL_SIO        ; POLL SIO FOR NEXT BYTE
          JR      Z,MSG_NUM            ; KEEP POLLING
          AND     IRQ,#IRQ3_RES        ; CLEAR IRQ3
          LD      R4,SIO               ; LOAD BYTE FROM SIO
          LD      R8,^HB LCD_MSG       ; LOAD LOOKUP TABLE ADD
          LD      R9,^LB LCD_MSG       ;
          LD      R7,#BUFF_BEG         ; GET BUFFER START ADD
LOOKUP_1:
          LD      R6,#16               ; SET BYTE COUNTER FOR 16
LOOKUP_2:
          INCW    RR8                  ; STEP TO DESIRED MESSAGE
          DJNZ    R6,LOOKUP_2          ; IF NOT 0, KEEP DECREMENTING
          DJNZ    R4,LOOKUP_1          ; INDEX MESSAGES
LOAD_MSG:
          LDEI    @R7,@RR8             ; LOAD INT BUFFER, INCREMENT
          CP      R7,#BUFF_END         ; END OF BUFFER?
          JR      LT,LOAD_MSG          ; NO, KEEP LOADING
          CALL    LCD_RES              ; SETUP FOR LCD TRANSFER
          CALL    LCD_LOAD             ; GO TO LOAD ROUTINE
          POP     IMR                  ; RESTORE INTERRUPT STRUCTURE
          POP     RP                   ; RESTORE REG POINTER
          RET                          ; RETURN TO CALLER

;------------------------------------------------------------------------;
;         LOAD ASCII CHARACTERS FOR DISPLAY ON LCD MODULE                ;
;------------------------------------------------------------------------;
ASCII:
          PUSH    IMR                  ; SAVE CONTENTS OF IMR
          DI                           ; DISABLE INTERRUPTS
          LD      IMR,#%20             ; ENABLE IRQ 5 ONLY
          CLR     IRQ                  ; CLEAR IRQ
          EI                           ; ENABLE INTERRUPTS
          CALL    TXT_LOAD             ; LOAD TEXT INTO BUFFER
          CALL    LCD_RES              ; CLEAR THE LCD
          POP     IMR                  ; RESTORE IMR
          RET                          ; RETURN FROM INTERRUPT
;
;------------------------------------------------------------------------;
;         TAKE THE ASCII TEXT AND LOAD IT INTO THE BUFFER                ;
;------------------------------------------------------------------------;
TXT_LOAD:
          CLR     R6                   ; RESET BYTE COUNTER
          LD      R7,#BUFF_BEG         ; POINT TO ASCII BUFFER
LOAD:
          TM      IRQ,#POLL_SIO        ; BYTE IN SIO?
          JR      Z,LOAD               ; LOAD SOME MORE
          LD      @R7,SIO              ; STORE AT THIS BUFFER LOCATION
          AND     IRQ,#IRQ3_RES        ; RESET IRQ3
          INC     R7                   ; INC BUFFER ADDRESS
          INC     R6                   ; INC BYTE COUNTER
          CP      R6,#16               ; SIXTEEN BYTES YET?
          JR      LT,LOAD              ;  NO, KEEP GOING
          RET                          ; RETURN TO CALLER
```

```
;------------------------------------------------------------------------;
;         TAKE THE ASCII FROM THE BUFFER AND LOAD THE LCD                 ;
;------------------------------------------------------------------------;
LCD_LOAD:
         CALL    LCD_OUT              ; OUTPUT CONTENTS OF BUFFER TO LCD
         AND     PORT_0,#RS_LOW       ; TAKE RS LOW
         LD      PORT_2,#DD_RAM_2     ; LOAD STARTING ADDRESS FOR LINE 2
         OR      PORT_0,#E_HIGH       ; TAKE ENABLE HIGH
         AND     PORT_0,#E_LOW        ; TAKE ENABLE LOW
         CALL    LCD_OUT              ; OUTPUT TO LCD
         RET
LCD_OUT:
         OR      PORT_0,#RS_HIGH      ; TAKE RS HIGH
         CLR     R6                   ; RESET BYTE COUNTER
LCD_LOOP:
         LD      PORT_2,@R7           ; FETCH ASCII FROM BUFFER
         OR      PORT_0,#E_HIGH       ; TAKE ENABLE HIGH
         AND     PORT_0,#E_LOW        ; TAKE ENABLE LOW
         CALL    WAIT_2               ; WAIT AWHILE
         INC     R6                   ; INC BYTE COUNTER
         INC     R7                   ; INC BUFFER ADDRESS
         CP      R6,#8                ; EIGHT BYTES YET?
         JR      LT,LCD_LOOP          ;  NO, GO AGAIN
         RET                          ; RETURN
;------------------------------------------------------------------------;
;         DELAY LOOP FOR LCD WRITES                                       ;
;------------------------------------------------------------------------;
WAIT_2:
         LD      R4,#CONST_1          ; THIS DELAY NOT
BUSY:
         DJNZ    R5,BUSY              ; QUITE AS LONG
         RET                          ; RETURN TO CALLER
;
;
;
;
;
;------------------------------------------------------------------------;
;         DELAY LOOP FOR LCD INITIALIZATION                               ;
;------------------------------------------------------------------------;
WAIT_1:
         PUSH    RP                   ; SAVE RP
         SRP     #MYREG_0             ; POINT TO 00H
         LD      R4,#CONST_1          ; LOAD FOR DELAY
LCDELY_1:
         LD      R5,#CONST_2          ; LCD'S ARE SLOW!
LCDELY_2:
         DJNZ    R5,LCDELY_2          ; DONE YET?
         DJNZ    R4,LCDELY_1          ;
         POP     RP                   ; RESTORE RP
         RET                          ; RETURN TO CALLER
;
;------------------------------------------------------------------------;
;         INTERNAL LCD MESSAGES                                           ;
;------------------------------------------------------------------------;
LCD_MSG:
         .BLOCK 16
         .ASCII 'ZILOG Z8s ARE OK'
         .END
```

11

ON-CHIP OSCILLATOR DESIGN

Design and Build Reliable, Cost-Effective, On-Chip Oscillator Circuits That are Trouble Free. Putting Oscillator Theory Into A Practical Design Makes for a More Dependable Chip.

INTRODUCTION

This Application Note (App Note) is written for designers using Zilog Integrated Circuits with on-chip oscillators; circuits in which the amplifier portion of a feedback oscillator is contained on the IC. This App Note covers common theory of oscillators, and requirements of the circuitry (both internal and external to the IC) which comes from the theory for crystal and ceramic resonator based circuits.

Purpose and Benefits

The purposes and benefits of this App Note include:

1. Providing designers with greater understanding of how oscillators work and how to design them to avoid problems.

2. To eliminate field failures and other complications resulting from an unawareness of critical on-chip oscillator design constraints and requirements.

Problem Background

Inadequate understanding of the theory and practice of oscillator circuit design, especially concerning oscillator start-up, has resulted in an unreliable design and subsequent field problems (See on page 10 for reference materials and acknowledgments).

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OSCILLATOR THEORY OF OPERATION

The circuit under discussion is called the Pierce Oscillator (Figures 1, 2). The configuration used is in all Zilog on-chip oscillators. Advantages of this circuit are low power consumption, low cost, large output signal, low power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects). One drawback is the need for high gain in the amplifier to compensate for feedback path losses.

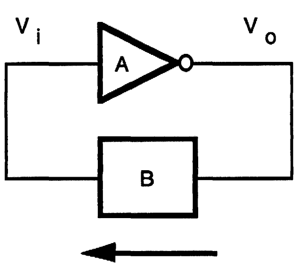


Figure 1. Basic Circuit and Loop Gain

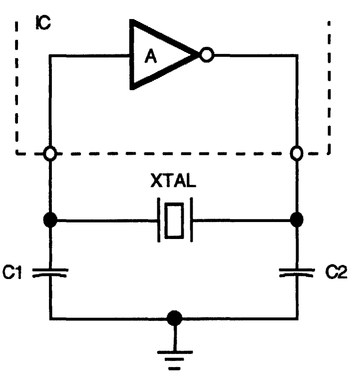


Figure 2. Zilog Pierce Oscillator

OSCILLATOR THEORY OF OPERATION (Continued)

Pierce Oscillator (Feedback Type)

The basic circuit and loop gain is shown in Figure 1. The concept is straightforward; gain of the amplifier is A = Vo/Vi. The gain of the passive feedback element is B = Vi/Vo. Combining these equations gives the equality AB = 1. Therefore, the total gain around the loop is unity. Also, since the gain factors A and B are complex numbers, they have phase characteristics. It is clear that the total phase shift around the loop is forced to zero (i.e., 360 degrees), since V_{IN} must be in phase with itself. In this circuit, the amplifier ideally provides 180 degrees of phase shift (since it is an inverter). Hence, the feedback element is forced to provide the other 180 degrees of phase shift.

Additionally, these gain and phase characteristics of both the amplifier and the feedback element vary with frequency. Thus, the above relationships must apply at the frequency of interest. Also, in this circuit the amplifier is an active element and the feedback element is passive. Thus, by definition, the gain of the amplifier at frequency must be greater than unity, if the loop gain is to be unity.

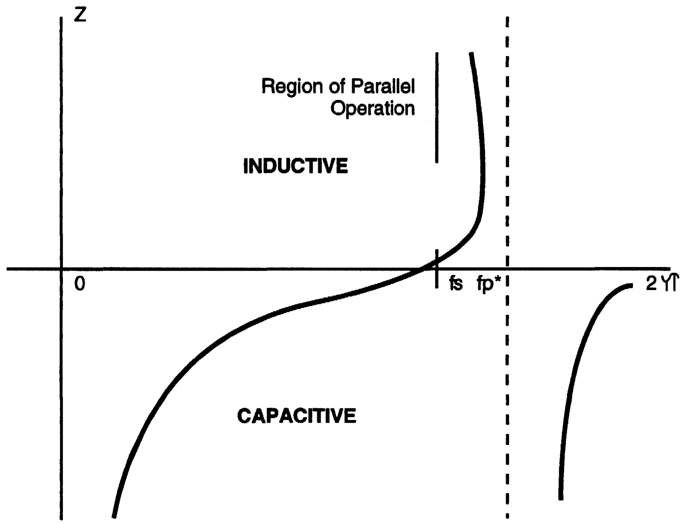
The described oscillator amplifies its own noise at start-up until it settles at the frequency which satisfies the gain/phase requirement AB = 1. This means loop gain equals one, and loop phase equals zero (360 degrees). To do this, the loop gain at points around the frequency of oscillation must be greater than one. This achieves an average loop gain of one at the operating frequency.

The amplifier portion of the oscillator provides gain > 1 plus 180 degrees of phase shift. The feedback element provides the additional 180 degrees of phase shift without attenuating the loop gain to < 1. To do this the feedback element is inductive, i.e., it must have a positive reactance at the frequency of operation. The feedback elements discussed are quartz crystals and ceramic resonators.

Quartz Crystals

A quartz crystal is a piezoelectric device; one which transforms electrical energy to mechanical energy and vice versa. The transformation occurs at the resonant frequency of the crystal. This happens when the applied AC electric field is sympathetic in frequency with the mechanical resonance of the slice of quartz. Since this characteristic can be made very accurate, quartz crystals are normally used where frequency stability is critical. Typical frequency tolerance is .005 to 0.3%.

The advantage of a quartz crystal in this application is its wide range of positive reactance values (i.e., it looks inductive) over a narrow range of frequencies (Figure 3).



* fs - fp is very small (approximately 300 parts per million)

Figure 3. Series vs. Parallel Resonance

However, there are several ranges of frequencies where the reactance is positive; these are the fundamental (desired frequency of operation), and the third and fifth mechanical overtones (approximately 3 and 5 times the fundamental frequency). Since the desired frequency range in this application is always the fundamental, the overtones must be suppressed. This is done by reducing the loop gain at these frequencies. Usually, the amplifier's gain roll off, in combination with the crystal parasitics and load capacitors, is sufficient to reduce gain and prevent oscillation at the overtone frequencies.

The following parameters are for an equivalent circuit of a quartz crystal (Figure 4):

L - motional inductance (typ 120 mH @ 4 MHz)

C - motional capacitance (typ .01 pf @ 4 MHz)

R - motional resistance (typ 36 ohm @ 4 MHz)

Cs - shunt capacitance resulting from the sum of the capacitor formed by the electrodes (with the quartz as a dielectric) and the parasitics of the contact wires and holder (typ 3 pf @ 4 MHz).

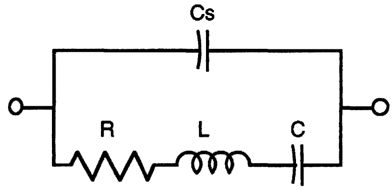
The series resonant frequency is given by:

Fs = 1/(2π x sqrt of LC),
where Xc and Xl are equal.

Thus, they cancel each other and the crystal is then R shunted by Cs with zero phase shift.

The parallel resonant frequency is given by:

Fp = 1/[2π x sqrt of L (C Ct/C+Ct)],
where: $Ct = C_L + C_S$



Quartz Equivalent Circuit

Symbolic Representation

Figure 4. Quartz Oscillator

Series vs. Parallel Resonance. There is very little difference between series and parallel resonance frequencies (Figure 3). A series resonant crystal (operating at zero phase shift) is desired for non-inverting amplifiers. A parallel resonant crystal (operating at or near 180 degrees of phase shift) is desired for inverting amps. Figure 3 shows that the difference between these two operating modes is small. Actually, all crystals have operating points in both serial and parallel modes. A series resonant circuit will NOT have load caps C1 and C2. A data sheet for a crystal designed for series operation does not have a load cap spec. A parallel resonant crystal data sheet specifies a load cap value which is the series combination of C1 and C2. For this App Note discussion, since all the circuits of interest are inverting amplifier based, only the parallel mode of operation is considered.

OSCILLATOR THEORY OF OPERATION

Ceramic Resonators

Ceramic resonators are similar to quartz crystals, but are used where frequency stability is less critical and low cost is desired. They operate on the same basic principle as quartz crystals as they are piezoelectric devices and have a similar equivalent circuit. The frequency tolerance is wider (0.3 to 3%), but the ceramic costs less than quartz.

Figure 5 shows reactance vs. frequency and Figure 6 shows the equivalent circuit.

Typical values of parameters are L = .092 mH, C = 4.6 pf, R = 7 ohms and Cs = 40 pf, all at 8 MHz. Generally, ceramic resonators tend to start up faster but have looser frequency tolerance than quartz. This means that external circuit parameters are more critical with resonators.

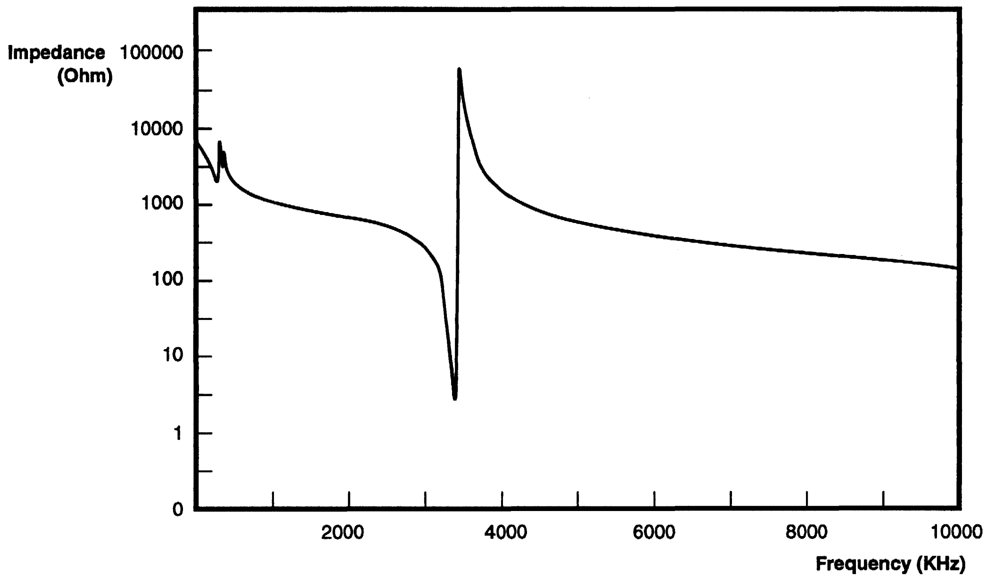


Figure 5. Ceramic Resonator Reactance

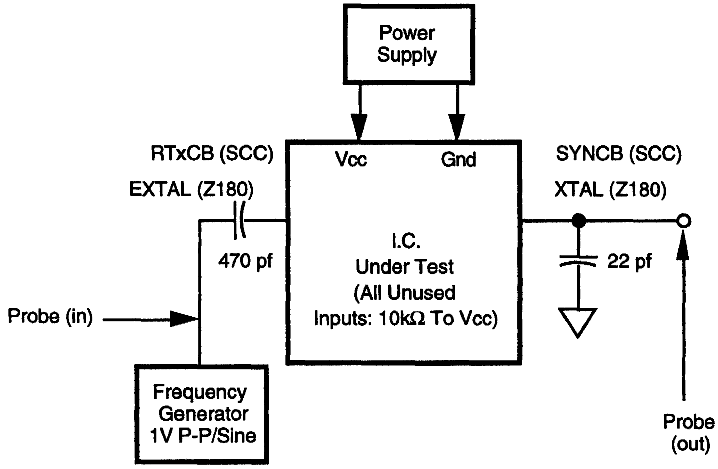


Figure 6. Gain Measurement

Load Capacitors

The effects/purposes of the load caps are:

Cap C2 combined with the amp output resistance provides a small phase shift. It also provides some attenuation of overtones.

Cap C1 combined with the crystal resistance provides additional phase shift.

These two phase shifts place the crystal in the parallel resonant region of Figure 3.

Crystal manufacturers specify a load capacitance number. This number is the load seen by the crystal which is the series combination of C1 and C2, including all parasitics (PCB and holder). This load is specified for crystals meant to be used in a parallel resonant configuration. The effect on start-up time; if C1 and C2 increase, start-up time increases to the point at which the oscillator will not start. Hence, for fast and reliable start-up, over manufacture of large quantities, the load caps should be sized as low as possible without resulting in overtone operation.

Amplifier Characteristics

The following text discusses open loop gain vs. frequency, open loop phase vs. frequency, and internal bias.

Open Loop Gain vs. Frequency over lot, VCC, Process Split, and Temp. Closed loop gain must be adequate to start the oscillator and keep it running at the desired frequency. This means that the amplifier open loop gain must be equal to one plus the gain required to overcome the losses in the feedback path, across the frequency band and up to the frequency of operation. This is over full process, lot, V_{CC}, and temperature ranges. Therefore, measuring the open loop gain is not sufficient; the losses in the feedback path (crystal and load caps) must be factored in.

Open Loop Phase vs. Frequency. Amplifier phase shift at and near the frequency of interest must be 180 degrees plus some, minus zero. The parallel configuration allows for some phase delay in the amplifier. The crystal adjusts to this by moving slightly down the reactance curve (Figure 3).

Internal Bias. Internal to the IC, there is a resistor placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and to provide the start-up transition. Typical values are 1M to 20M ohms.

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PRACTICE: CIRCUIT ELEMENT AND LAY OUT CONSIDERATIONS

The discussion now applies prior theory to the practical application.

Amplifier and Feedback Resistor

The elements of the circuit, internal to the IC, include the amplifier, feedback resistor, and output resistance. The amplifier is modeled as a transconductance amplifier with a gain specified as I_{OUT}/V_{IN} (amps per volt).

Transconductance/Gain. The loop gain AB = gm x Z1, where gm is amplifier transconductance (gain) in amps/volt and Z1 is the load seen by the output. AB must be greater than unity at and about the frequency of operation to sustain oscillation.

Gain Measurement Circuit. The gain of the amplifier can be measured using the circuits of Figures 6 & 7. This may be necessary to verify adequate gain at the frequency of interest and in determining design margin.

Gain Requirement vs. Temperature, Frequency and Supply Voltage. The gain to start and sustain oscillation (Figure 8) must comply with:

$gm > 4\pi^2 f^2 Rq \; C_{IN} \; C_{OUT}t \times M$
where: M is a quartz form factor $= (1 + C_{OUT}/C_{IN} + C_{OUT}/C_{OUT})^2$

Output Impedance. The output impedance limits power to the XTAL and provides small phase shift with load cap C2.

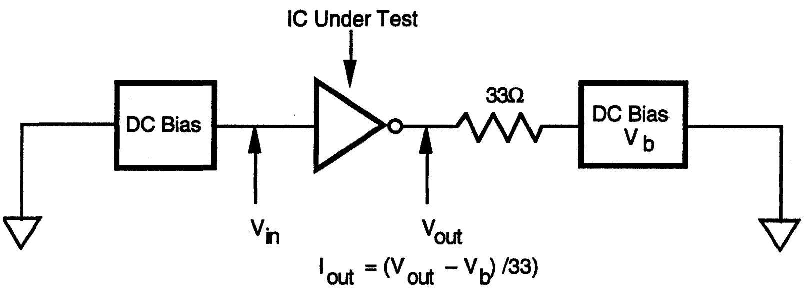
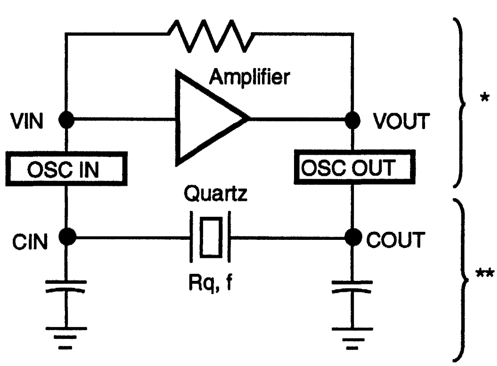


Figure 7. Transconductance (gm) Measurement



* Inside chip, feedback resistor biases the amplifier in the high gm region.

** External components typically: CIN = COUT = 30 to 50 pf (add 10 pf pin cap).

Figure 8. Quartz Oscillator Configuration

Load Capacitors

In the selection of load caps it is understood that parasitics are always included.

Upper Limits. If the load caps are too large, the oscillator will not start because the loop gain is too low at the operating frequency. This is due to the impedance of the load capacitors. Larger load caps produce a longer start-up.

Lower Limits. If the load caps are too small, either the oscillator will not start (due to inadequate phase shift around the loop), or it will run at a 3rd, 5th, or 7th overtone frequency (due to inadequate suppression of higher overtones).

Capacitor Type and Tolerance. Ceramic caps of ±10% tolerance should be adequate for most applications.

Ceramic vs. Quartz. Manufacturers of ceramic resonators generally specify larger load cap values than quartz crystals. Quartz C is typically 15 to 30 pf and ceramic typically 100 pf.

Summary. For reliable and fast start-up, capacitors should be as small as possible without resulting in overtone operation. The selection of these capacitors is critical and all of the factors covered in this note should be considered.

Feedback Element

The following text describes the specific parameters of a typical crystal:

Drive Level. There is no problem at frequencies greater than 1 MHz and V_{CC} = 5V since high frequency AT cut crystals are designed for relatively high drive levels (5-10 mw max).

A typical calculation for the approximate power dissipated in a crystal is:

$$P = 2R (\pi \times f \times C \times V_{CC})^2$$

Where. R = crystal resistance of 40 ohms, C = C1 + Co = 20 pf. The calculation gives a power dissipation of 2 mW at 16 MHz.

Series Resistance. Lower series resistance gives better performance but costs more. Higher R results in more power dissipation and longer start-up, but can be compensated by reduced C1 and C2. This value ranges from 200 ohms at 1 MHz down to 15 ohms at 20 MHz.

Frequency. The frequency of oscillation in parallel resonant circuits is mostly determined by the crystal (99.5%). The external components have a negligible effect (0.5%) on frequency. The external components (C1,C2) and layout are chosen primarily for good start-up and reliability reasons.

Frequency Tolerance (initial temperature and aging). Initial tolerance is typically ±.01%. Temperature tolerance is typically ±.005% over the temp range (-30 to +100 degrees C). Aging tolerance is also given, typically ±.005%.

Holder. Typical holder part numbers are HC6, 18, 25, 33, 44.

Shunt Capacitance. (Cs) typically <7 pf.

Mode. Typically the mode (fundamental, 3rd or 5th overtone) is specified as well as the loading configuration (series vs. parallel).

The ceramic resonator equivalent circuit is the same as shown in Figure 4. The values differ from those specified in the theory section. Note that the ratio of L/C is much lower than with quartz crystals. This gives a lower Q which allows a faster start-up and looser frequency tolerance (typically ±0.9% over time and temperature) than quartz.

Layout

The following text explains trace layout as it affects the various stray capacitance parameters (Figure 9).

Traces and Placement. Traces connecting crystal, caps, and the IC oscillator pins should be as short and wide as possible (this helps reduce parasitic inductance and resistance). Therefore, the components (caps and crystal) should be placed as close to the oscillator pins of the IC as possible.

Grounding/Guarding. The traces from the oscillator pins of the IC should be guarded from all other traces (clock, V_{CC}, address/data lines) to reduce crosstalk. This is usually accomplished by keeping other traces away from the oscillator circuit and by placing a ground ring around the traces/components (Figure 9).

Measurement and Observation

Connection of a scope to either of the circuit nodes is likely to affect operation because the scope adds 3-30 pf of capacitance and 1M-10M ohms of resistance to the circuit.

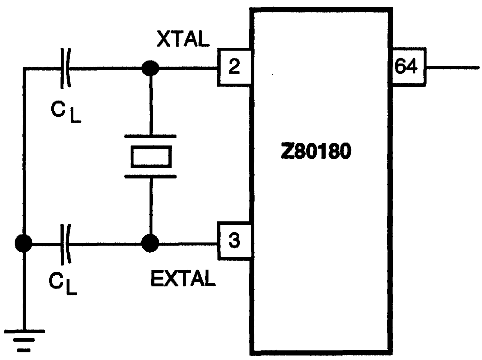
PRACTICE: CIRCUIT ELEMENT AND LAY OUT CONSIDERATIONS (continued)

Indications of an Unreliable Design

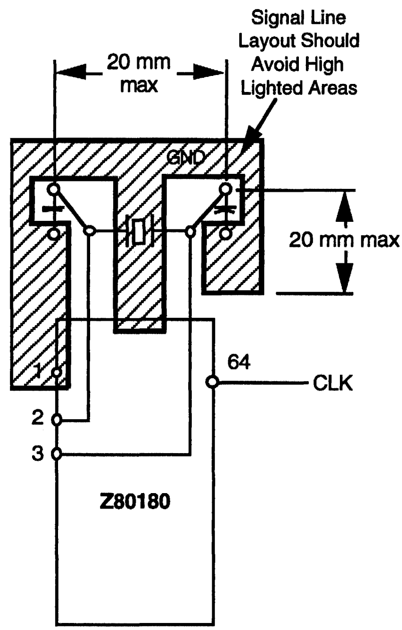
There are two major indicators which are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start Up Time. If start up time is excessive, or varies widely from unit to unit, there is probably a gain problem. C1/C2 needs to be reduced; the amplifier gain is not adequate at frequency, or crystal Rs is too large.

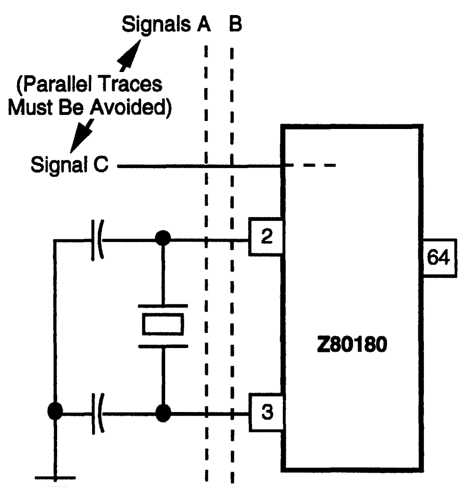
Output Level. The signal at the amplifier output should swing from ground to V_{CC}. This indicates there is adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs, at which point, the loop gain is effectively reduced to unity and constant oscillation is achieved. A signal of less than 2.5 Vp-p is an indication that low gain may be a problem. Either C1/C2 should be made smaller or a low R crystal should be used.



Clock Generator Circuit



Board Design Example
(Top View)



- To prevent induced noice, the crystal and load capacitors should be physically located as close to the LSI as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particullar, the clock input circuitry and the system clock output (pin 64) should be separated as much as possible.
- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistivity between XTAL or EXTAL and the other pin should be greater than 10 MΩ

Figure 9. Circuit Board Design Rules

SUMMARY

Understanding the Theory of Operation of oscillators, combined with practical applications, should give designers enough information to design reliable oscillator circuits. Proper selection of crystals and load capacitors, along with good layout practices, results in a cost effective, trouble free design. Reference the following text for Zilog products with on-chip oscillators and their general/specific requirements.

ZILOG PRODUCT USING ON-CHIP OSCILLATORS

Zilog products that have on-chip oscillators:

Z8® Family: All
Z80®: C01, C11, C13, C15, C50, C90, 180, 181, 280
Z8000®: 8581
Communications Products: SCC™, ISCC™, ESCC™

ZILOG CHIP PARAMETERS

The following are some recommendations on values/parameters of components for use with Zilog on-chip oscillators. These are only recommendations; no guarantees are made by performance of components outside of Zilog ICs. Finally, the values/parameters chosen depend on the application. This App Note is meant as a guideline to making these decisions. Selection of optimal components is always a function of desired cost/performance trade-offs.

Note: All load capacitance specs include stray capacitance.

Z8® Family

General Requirements:

Crystal Cut: AT cut, parallel resonant, fundamental mode.
Crystal Co: < 7 pf for all frequencies.
Crystal Rs: < 100 ohms for all frequencies.
Load Capacitance: 10 to 22 pf, 15 pf typical.

Specific Requirements:

8604: xtal or ceramic, f = 1 - 8 MHz.
8600/10: f = 8 MHz.
8601/03/11/13: f = 12.5 MHz.
8602: xtal or ceramic, f = 4 MHz.
8680/81/82/84/91: f = 8, 12, 16, MHz.
8671: f = 8 MHz.
8612: f = 12, 16 MHz.
86C08/E08: f = 8, 12 MHz.
86C09/19: xtal/resonator, f = 8 MHz, C = 47 pf max.
86C00/10/20/30: f = 8, 12, 16 MHz.
86C11/21/91/40/90: f = 12, 16, 20 MHz.
86C27/97: f = 4, 8 MHz.
86C12: f = 12, 16 MHz.
Super8 (all): f = 1 - 20 MHz.

Z8000® Family (8581 only)

General Requirements:

Crystal cut: AT cut, parallel resonant, fundamental mode.
Crystal Co: < 7 pf for all frequencies.
Crystal Rs: < 150 ohms for all frequencies.
Load capacitance: 10 to 33 pf.

Z80® Family

General Requirements:

Crystal cut: AT cut, parallel resonant, fundamental mode.
Crystal Co: < 7 pf for all frequencies.
Crystal Rs: < 60 ohms for all frequencies.
Load capacitance: 10 to 22 pf.

Specific Requirements:

84C01: C1 = 22 pf, C2 = 33 pf (typ); f = DC to 10 MHz.
84C90: DC to 8 MHz.
84C50: same as 84C01.
84C11/13/15: C1 = C2 = 20 -33 pf; f = 6 -10 MHz
80180: f = 12, 16, 20 MHz (Fxtal = 2 x sys. clock).
80280: f = 20 MHz (Fxtal = 2 x Fsysclk).
80181: TBD.

ZILOG CHIP PARAMETERS (Continued)

Communications Family

General Requirements:

Crystal cut: AT cut, parallel resonant, fundamental mode.
Crystal Co: < 7 pf for all frequencies.
Crystal Rs: < 150 ohms for all frequencies.
Load capacitance: 20 to 33 pf.
Frequency: cannot exceed PCLK.

Specific Requirements:

8530/85C30/SCC: f = 1 - 6 MHz (10 MHz SCC), 1 - 8.5 MHz (8 MHz SCC).
85130/ESCC (16/20 MHz), f = 1 - 16.384 MHz.
16C35/ISCC: f = 1 -10 MHz.

REFERENCES MATERIALS AND ACKNOWLEDGMENTS

Intel Corp., Application Note AP-155, "Oscillators for Micro Controllers", order #230659-001, by Tom Williamson, Dec. 1986.

Motorola 68HC11 Reference Manual.

National Semiconductor Corp., App Notes 326 and 400.

Zilog, Inc., Steve German; Figures 4 and 8.

Zilog, Inc., Application Note, "Design Considerations Using Quartz Crystals with Zilog Components" - Oct. 1988.

Data Sheets; CTS Corp. Knights Div., Crystal Oscillators.

Z86C0800ZCO Evaluation Board
Product Specification

DEVICES SUPPORTED: Z86C08, Z86C04

DESCRIPTION

The Z86C0800ZCO Evaluation Board kit contains an assembled circuit board, software and documentation to help the user become familiar with the features of the Z86C08 microcontroller.

The Z86C0800ZCO Evaluation Board is used to demonstrate the advantages and versatility of the 18-pin Z8 device. The kit contains hardware and software that demonstrates the implementation of WDT, HALT, and STOP mode, low cost D to A, and A to D conversion techniques.

SPECIFICATIONS

Power Requirements

+5 Vdc @ 50 mA

Dimensions

Width: 4.4 in. (11.2 cm)
Length: 4.8 in. (12.2 cm)

KIT CONTENTS

Z86C08 Evaluation Board

CMOS Z86C08 MPU
4 MHz Crystal
Four 7-Segment LED Displays
17-Key Keypad

Software (IBM® PC Platform)

Application Source Code
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader

Documentation

Discrete Z8® Databook
Z8 Cross Assembler User's Guide
MOBJ Link/Loader User's Guide
Z86C08 Evaluation Board User's Guide

ORDERING INFORMATION

Part No: Z86C0800ZCO

Z86C0800ZDP ADAPTOR KIT
PRODUCT SPECIFICATION

DEVICE SUPPORTED: Z86C08

DESCRIPTION
The Z86C08 Adaptor Kit is used to convert a Z8® MCU 40-pin package to an 18-pin package. This adaptor board allows a standard Z8 emulation device to emulate the Z86C08. The Z86C08 Adaptor Board is placed between the Z8 emulator and the user's target socket. The board does not emulate the watch-dog timer function.

SPECIFICATIONS
Dimensions
Width: 2.5 in. (6.4 cm)
Length: 2.9 in. (7.4 cm)

KIT CONTENTS
Z86C08 Adaptor Board
40-Pin Z8 MPU Socket
18-Pin Z86C08 Socket
12 MHz Crystal

Cables
18-Pin Z86C08 Emulation Cable

Documentation
Z86C08 Adaptor Kit User's Guide

ORDERING INFORMATION
Part No: Z86C0800ZDP

Z86C1200ZEM EMULATOR
PRODUCT SPECIFICATION

DEVICES SUPPORTED: Z86C04/E04, Z86C07, Z86C08/E08, Z86C11, Z86C20, Z86C21/E21[1], Z86E22[1], Z86E23[2], Z86C61, Z86C63, Z86C65, Z86C91

DESCRIPTION

The Z86C1200ZEM Z8® Emulator is a member of Zilog's ICEBOX™ product family of in-circuit emulators. The Z86C1200ZEM provides emulation and OTP programming support for Zilog's Z8 microcontrollers. The Emulator provides all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware/software product. The data entering, program debugging, and OTP programming are performed by the monitor ROM and the Host Package which communicates through a RS-232C serial interface with a fixed 19200 baud rate. The user program can be downloaded directly from the host computer through the RS-232C connector. The user code may then be executed using various debugging commands in the monitor. The Emulator can be connected to a serial port COM 1 or COM 2 of the host computer (IBM® XT, AT 386, 486 Compatible).

SPECIFICATIONS

Emulation Specification

Maximum Emulation Speed 16 MHz

Power Requirements

+5 Vdc @ 1.0 A

Dimensions

Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

Serial Interface

RS-232C @ 19200 baud

Notes:
[1] Does not support 4K/8K option bit.
[2] With Z86E2300ZDP Programming Adaptor, Rev. 1.0

KIT CONTENTS

Z86C12 Emulator

- Z8 Emulation Base Board (Revision B)
  - CMOS Z86C9120PSC
  - 8K X 8 EPROM (Programmed with Debug Monitor)
    - EPM5128 EPLD
    - 32K X 8 STATIC RAM
    - 3 64K X 4 STATIC RAM
    - RS-232C Interface
    - Reset Switch
  - Z86C12 Emulation Daughter Board
    - EPM5032 EPLD
    - 16 MHz CMOS Z86C1216GSE ICE Chip
    - 40/18 Pin ZIF OTP Sockets
    - 80/60/40 Pin Target Connectors

Cables

- 12", 40-Pin DIP Emulation Cable
- 12", 28-Pin DIP Emulation Cable
- 12", 18-Pin DIP Emulation Cable
- 15", Power Cable with Banana Plugs
- 48", Power Cable
- 60", DB 25 RS-232C Cable

Software (IBM®-PC Platform)

- Z8/Z80/Z8000 Cross Assembler
- MOBJ Link/Loader
- Host Package (Revision 1.5)
- Includes Windows and non-Windows

Documentation

- Emulator User's Guide
- Support Products Catalog
- Z8 Cross Assembler User's Guide
- MOBJ Link/Loader User's Guide
- Registration Card

ORDERING INFORMATION

Part No: Z86C1200ZEM

Z86E0600ZDP ADAPTOR KIT
PRODUCT SPECIFICATION

DEVICES SUPPORTED: Z86C06/09/19

DESCRIPTION
The Z86E06 Adaptor Kit converts the 28-pin footprint of Zilog's Z86E30 OTP chip to the 18-pin DIP configuration of the Z86E06/09/19 OTP chip. The board supports all the functions of the Z86C06/09/19 except for Serial Peripheral Interface.

SPECIFICATIONS
Dimensions
Width: 0.8 in. (2.0 cm)
Length: 1.5 in. (3.8 cm)

KIT CONTENTS
Z86E06 Adaptor Kit
28-Pin Z86E30 MCU Socket
18-Pin Z86C06/09/19 Connector

Documentation
Z86E06 OTP Conversion Kit User's Guide

ORDERING INFORMATION
Part No: Z86E0600ZDP

Z86E0700ZDP Adaptor Kit
Product Specification

DEVICE SUPPORTED: Z86E07 SOIC

DESCRIPTION
The Z86E07 Adaptor Kit converts an 18-pin SOIC package to an 18-pin DIP package, allowing a Z86E07 DIP OTP programmer to program the 18-pin SOIC Z86E07 OTP microcontroller

SPECIFICATIONS
Dimensions
Width: 0.95 in.
Length: 1.10 in.

Operating Temperature
0 to 50°C

Operating Humidity
10-90% RH (non-condensing)

KIT CONTENTS
Z86E07 Adaptor Board
18-Pin SOIC ZIF Package
18-Pin DIP Connector

Documentation
Z86E07 OTP Adaptor Kit User's Guide

ORDERING INFORMATION
Part No: Z86E0700ZDP

Z86E3000ZDP ADAPTOR KIT
PRODUCT SPECIFICATION

DEVICES SUPPORTED: Z86E30, Z86E31

DESCRIPTION
The Z86E30 DIP OTP Adaptor Kit allows a standard EPROM programmer to program the Z86E30 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5A

Dimensions
Width: 1.45 in. (3.68 cm)
Length: 2.0 in. (5.08 cm)

KIT CONTENTS
Z86E30 OTP Program Adaptor Board
28-Pin DIP ZIF Socket
28-Pin Connector

Documentation
OTP Program Adaptor User's Guide

ORDERING INFORMATION
Part No: Z86E3000ZDP

Z86E4000ZDF ADAPTOR KIT
PRODUCT SPECIFICATION

DEVICE SUPPORTED: Z86E40

DESCRIPTION
The Z86E40 QFP OTP Adaptor Kit allows a standard EPROM programmer to program the Z86E40 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

Dimensions
Width: 1.75 in. (4.4 cm)
Length: 2.20 in. (5.6 cm)

KIT CONTENTS
Z86E40 QFP OTP Adaptor Board
44-Pin QFP ZIF Socket
28-Pin Connector

Documentation
OTP Program Adaptor User's Guide

ORDERING INFORMATION
Part No: Z86E4000ZDF

Z86E4000ZDP ADAPTOR KIT
PRODUCT SPECIFICATION

DEVICE SUPPORTED: Z86E40

DESCRIPTION
The Z86E40 DIP OTP Adaptor Kit allows a standard EPROM programmer to program the Z86E40 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

Dimensions
Width: 1.4 in. (3.6 cm)
Length: 2.6 in. (6.6 cm)

KIT CONTENTS
Z86E40 DIP OTP Adaptor Board
40-Pin DIP ZIF Socket
28-Pin Connector

Documentation
OTP Program Adaptor User's Guide

ORDERING INFORMATION
Part No: Z86E4000ZDP

Z86E4000ZDV ADAPTOR KIT
PRODUCT SPECIFICATION

DEVICE SUPPORTED: Z86E40

DESCRIPTION

The Z86E40 PLCC OTP Adaptor Kit allows a standard EPROM programmer to program the Z86E40 OTP microcontroller.

SPECIFICATIONS

Power Requirements

+12.5 Vdc @ .5 A

Dimensions

Width: 1.6 in. (4.1 cm)
Length: 2.0 in. (5.1 cm)

KIT CONTENTS

Z86E40 PLCC OTP Adaptor Board

40-Pin ZIF Socket
28-Pin Connector

Documentation

OTP Program Adaptor User's Guide

ORDERING INFORMATION

Part No: Z86E4000ZDV

Z86E4001ZDF ADAPTOR KIT
PRODUCT SPECIFICATION

DEVICE SUPPORTED: Z86E40

DESCRIPTION

The Z86E40 OTP Adaptor Kit converts a 44-pin QFP package to a 40-pin DIP package, allowing the C50 ICEBOX™ to program the 44-pin QFP Z86E40 OTP microcontroller.

SPECIFICATIONS

Power Requirements

+12.5 Vdc @ .5 A

Dimensions

Width: 2.05 in. (5.2 cm)
Length: 2.10 in. (5.3 cm)

KIT CONTENTS

Z86E40 OTP Adaptor Board

44-Pin QFP ZIF Socket
40-Pin Connector

Documentation

OTP Program Adaptor User's Guide

ORDERING INFORMATION

Part No: Z86E4001ZDF

Z86E4001ZDV Adaptor Kit
Product Specification

DEVICE SUPPORTED: Z86E40

DESCRIPTION
The Z86E40 OTP Adaptor Kit converts a 44-pin PLCC package to a 40-pin DIP package, allowing the C50 ICEBOX™ to program the 44-pin PLCC Z86E40 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

Dimensions
Width: 1.8 in. (4.6 cm)
Length: 2.1 in. (5.3 cm)

KIT CONTENTS
Z86E40 OTP Adaptor Board
40-Pin PLCC ZIF Socket
40-Pin Connector

Documentation
OTP Program Adaptor User's Guide

ORDERING INFORMATION
Part No: Z86E4001ZDV

Z86CCP00ZEM Emulator
Product Specification

DEVICES SUPPORTED: Z86C03, Z86C04/E04, Z86C06, Z86C08/E08, Z86C09/19

DESCRIPTION

The Z86CCP00ZEM is a member of Zilog's family of in-circuit emulators. The Z8 CCP emulator provides emulation and OTP programming support for Zilog's Consumer Controller Processor (CCP™) microcontroller. The Emulator provides all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware/software product.

The data entering, program debugging, and OTP programming are performed by the monitor ROM and the Host Package which communicates through RS-232C serial interface with a fixed 19200 baud rate. The user program can be downloaded directly from the host computer via an RS-232C connector. The user code may then be executed using various debugging commands in the monitor. The Emulator can be connected to any serial port (COM 1, 2, 3 or 4) of the host computer.

The Z86CCP00ZEM supports stand-alone mode (without host mode) through special jumper options. In stand-alone mode, the C50 ICE chip is used in conjunction with a PROM and can support speeds of DC to 12 MHz at V_{CC} of 3V to 5.5V.

SPECIFICATIONS

Emulation Specification

Maximum Emulation Speed 8 MHz
Minimum Emulation Speed 1 MHz
Maximum Emulation Speed
Stand-Alone Mode 16 MHz
Minimum Emulation Speed
Stand-Alone Mode DC

Power Requirements

+8V Vdc @ 0.5 A

Dimensions

Width: 7.0 in. (17.7 cm)
Length: 9.0 in. (22.9 cm)

Serial Interface

RS-232C @ 19200 baud

System Requirements

IBM-Compatible 286 @ 12 MHz or Newer
CPU Running DOS 5.0 or Higher
Windows Version 3.0 or Higher
720 Kbytes of Disk Space
512 Kbytes of RAM

KIT CONTENTS

Z8 CCP Emulator

Z8 CCP Emulation Board (Revision A)
- CMOS Z86C9320VSC
- RS-232C Interface
- Reset Switch
- 20 MHz CMOS Z86C5020FSE ICE Chip
- 8K x 8 STATIC RAM for Code Memory
- 18-Pin ZIF OTP Socket
- Socket Available for 18-Pin Target Connector
- 18-Pin Target Connector Cable
- Holes Available for 40-Pin ZIF Socket
- Socket Available for 40-Pin Target Connector
- Holes Available for 28-Pin ZIF Socket
- Socket Available for 28-Pin Target Connector

Software (IBM PC platform)

Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Emulator GUI Host Package

Documentation

Emulator User's Guide
Z8 Cross Assembler User's Guide
MOBJ Link/Loader User's Guide
Registration Card
Z8 CCP Emulator GUI User's Guide
Discrete Z8 Data Book
Z8 Microcontroller Technical Manual

ORDERING INFORMATION

Part No: Z86CCP00ZEM

Z86CCP00ZAC Emulator Kit
Product Specification

DEVICES SUPPORTED: Z86C31/E31, Z86C30/E30, Z86C40/E40

DESCRIPTION

The Z86CCP00ZAC is the accessory kit for the Z86CCP00ZEM. The kit contains all accessories to fully populate and operate all functions of the Z86CCP00ZEM.

SPECIFICATIONS

Emulation Specification

Maximum Emulation Speed 8 MHz
Minimum Emulation Speed 1 MHz
Maximum Emulation Speed
Stand-Alone Mode 16 MHz
Minimum Emulation Speed
Stand-Alone Mode DC

Power Requirements

+8V Vdc @ 0.5 A

Dimensions

Width: 7.0 in. (17.7 cm)
Length: 9.0 in. (22.9 cm)

Serial Interface

RS-232C @ 19200 baud

System Requirements

IBM-Compatible 286 @ 12 MHz or Newer
CPU Running DOS 5.0 or Higher
Windows Version 3.0 or Higher
720 Kbytes of Disk Space
512 Kbytes of RAM

KIT CONTENTS

Z8 CCP Emulator Kit

28-Pin ZIF Socket
28-Pin Target Connector Cable
40-Pin ZIF Socket
40-Pin Target Connector Cable
RS-232 Cable
Power Cable

Software (IBM PC platform)

Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Emulator GUI Host Package

Documentation

Emulator User's Guide
Z8 Cross Assembler User's Guide
MOBJ Link/Loader User's Guide
Registration Card
Z8 CCP Emulator GUI User's Guide
Discrete Z8 Data Book
Z8 Microcontroller Technical Manual

ORDERING INFORMATION

Part No: Z86CCP00ZAC

Z8® S SERIES EMULATORS BASE UNITS AND PODS

DESCRIPTION

The system comprises 24 MHz or 33 MHz base unit options, and pod options which allow the emulation of various Z8 microcontrollers. Features include real-time transparent emulation up to 33 MHz, in-line symbolic assembler and disassembler, real-time hardware breakpoints, eight channel user logic analyzer, external trigger input and outputs, trace display and memory display/edit during execution, and window or command driven user interface.

SPECIFICATIONS

Microcontrollers Emulated:

Z86C1200ZPD
Z86C00, Z86C10, Z86C11, Z86C20, Z86C21, Z86E21, Z86C91, Z86C61, Z86C63

Z86C5000ZPD
Z86C03, Z86C06, Z86C09, Z86C19, Z86C30, Z86C31, Z86C40, Z86C90

Z86C9300ZPD
Z86C93 (24 MHz)

Z86C9301ZPD
Z86C93 (33 MHz)

Z86C9500ZPD
Z86C95 (24 MHz)

Z86C9501ZPD
Z86C95 (33 MHz)

Maximum Emulation Speed:

Up to 24 MHz (microcontroller dependent)
Up to 33 MHz (Z86C93 and Z86C95)

Size:

260 mm wide, 260 mm deep, 64 mm high

Operating Temperature:

0°C to +40°C

Storage Temperature:

–10°C to +65°C

Operating Humidity:

0 to 90%

Maximum Emulation Program and Data Memory:

64 Kbytes

Program Memory Mapping:

1K blocks

Pass Counters:

Two, 16-bit each

Trace Buffer:

32K - 80 bits

Sequencer:

Hardware, 8 levels

User Probe:

Eight channel logic input
One trigger input
Seven trigger outputs (Events, Pass Counters, Sequencer)

Host Interface:

Asynchronous RS-232C
9600/115 KBaud
XON/XOFF support

File Upward/Downward Format:

Zilog MUFOM (EEE 695-1985)
Intel® HEX
Intel AOMF
2500AD® Software

MINIMUM HOST REQUIREMENTS

- IBM® compatible PC/XT/AT/386/486 or PS-2
- 640 Kbyte memory
- 20 Mbyte hard disk
- RS-232 serial port (COM 1 or COM 2)
- Mouse (serial or bus)
- MDA, CGA, EGA, or VGA video adaptor

MINIMUM EMULATION SUPPORT

- One base unit
- One emulation pod

ORDERING INFORMATION:

Base Unit	Emulation Pod
Z86C0000ZUSP064	
Z86C0001ZUSP064 (33 MHz)	Z86C1200ZPD
Z86C9500ZUSP064	Z86C5000ZPD
Z86C9501ZUSP064 (33 MHz)	Z86C9500ZPD (24 MHz)
	Z86C9301ZPD (33 MHz)
	Z86C9500ZPD (24 MHz)
	Z86C9501ZPD (33 MHz)

Z8 Support

Company	Assembler	C Compiler	Simulator	Operating System	Phone Number
Allen Ashley	X		X	DOS, CP/M	(818) 793-5748
Avocet Systems	X			DOS	(800) 448-8500
Byte Craft		X		DOS	(519) 888-6911
Cybernetic Micro	X			DOS	(415) 726-3000
Micro Computer Control	X	X	X	DOS	(609) 466-1751
Micro Dialects	X			Macintosh	(513) 271-9100
Production Language Corp.	X	X	X	DOS (386+)	(817) 599-8363
Pseudo Corp.	X		X	DOS	(804) 873-1947
Software Development Systems	X			DOS UNIX	(800) 448-7733
Western Wares	X			DOS CP/M-80 ISIS-II	(303) 327-4888
2500AD Software	X	X	X	DOS UNIX CP/M VAX VMS	(719) 395-8683

Super8® Support

Company	Assembler	C Compiler	Simulator	Operating System	Phone Number
Allen Ashley	X		X	Macintosh	(818) 793-5748
Micro Computer Control		X		DOS	(609) 466-1751
Pseudo Corp.	X		X	DOS	(804) 873-1947
2500AD Software	X		X	DOS	(719) 395-8683

Emulators

Part Number

Development System	Z8600	Z8601	Z8611	Z8681	Z8691	Z86C08	Z86C00	Z86C10	Z86C20	Z86C11	Z86C21	Z86C27	Z86C91	Z86C09	Z86C19	Z86C30	Z86C40	Z86C90	Z86C93	Z86C94	Z86E21	Z86C61
Creative Technology	●	●	●	●	●	●		●	●	●	●		●								●	
iSystems						A	●	●	●	●	●		●	●	●	●	●	●	●		●	●
JK Board V.3.8	●	●	●	●	●	●	●	●	●	●	●		●									
MicroTime	●	●	●	●	●	A	●	●	●	●	●		●									
Orion Instruments	B	B	B	●	●	C	D	D	D	D	D	●	●	E	E			●				
Signum Systems							●	●	●	●	●		●	●	●	●	●	●	●	●	●	●
Wytec						A	●	●	●	●	●											

A = Emulate with Z86C0800ZDP Adaptor
B = Emulate with Z8612 Board
C = Emulate with Z86C0800ZDP and Z8612 Board or Z86C0800ZEM
D = Emulate with Z8612 Board
E = Emulate with Z86C90 Board

OTP Programmers

Part Number

Development System	Z86E08	Z86E21	Z86E22	Z86E30	Z86E40
Data I/O, Inc.		●			
Logical Devices, Inc.*	●	●	●	●	●
Needham, Inc.	●	●		●	
Smart Access, Inc.		●	●		

* Single and Gang Programming Available

Hardware Support

Company	Product	Phone
American Automation	Emulator	(714) 731-1661
Applied Microsystems	Emulator	(206) 882-2000
Hewlett-Packard	Emulator pods for HP 64000/UX/PC	(800) 4HP-DATA
Huntsville Microsystems	Emulator	(205) 881-6005
iSystems (Germany)	Emulator	08131-25083
Micromint	SB180,SB180FX, BCC180,RTC180	(800) 635-3355
MicroWorks	Prototyping board	(408) 997-1644
Orion Instruments†	Emulator	(415) 327-8800
Pentica Systems, Inc.	Emulator	(617) 577-1101
Softaid††	Emulator, ICEBOX, ICE Analyzer (symbolic debug)	(800) 433-8812
Sophia Systems	Emulator, SA2000	(415) 493-6700
Versalogic	Z80 STD Bus circuit board	(503) 485-8575
Z-World	IBM PC Development Bd.	(916) 753-3722
Zaxtek	Emulator	(714) 474-1170
Zilog	S180+ESCC (Z8S18000ZCO) Application Board	*Call Zilog*
Zilog	Z80181 Eval. Kit (Z8018100ZCO)	*Call Zilog*
Zilog	Z84C15 Eval. Kit (Z84C1500ZCO)	*Call Zilog*
Zilog	Z84C50+KIO Application Bd. (Z84C5000ZCO)	*Call Zilog*
Zilog	Z84C01+KIO Development Bd. (Z84C9000ZCO)	*Call Zilog*
Emulation Technology††	Emulator	(408) 982-0660

Note:
Z80180 Emulators can be utilized for Z80182 in Eval Mode 1.
† Supports Z182 in Mode 0 also.
†† Supports Z182 in Mode 2 also.

68 PLCC Socket Manufacturers:
Methode, TNB, ITT, Cannon, Precicontact

64 Shrink DIP Socket Manufacturers:
TI, Bevar, Yamaichi

44/80/100 Pin QFP:
ZIF (Zero Insertion Force) sockets for prototyping may be obtained from Yamaichi Electronics, (408) 450-0797.

100-Pin QFP Clip:
Emulation Technology, 408-982-0660

Assemblers and Cross Assemblers

Company	Host/Comments	Phone
2500AD	C; IBM PC, CP/M, VAX, Sun	(800) 843-8144
American Automation	C; IBM PC	(714) 731-1661
Archimedes	C; IBM PC, Sun, VAX, HP	(415) 567-4010
Avocet Systems	C; IBM PC	(800) 448-8500
Laboratory	Forth; IBM PC MicroSystems	(213) 306-7412
MicroDialects	Z80/Z180 for Apple Macintosh only	(513) 271-9100
Microtek Research	C Compilers; PC DOS, Sun Sparc	(408) 980-1300
MPE	Forth; IBM PC	(716) 461-9187
Softaid	MT-Basic; IBM PC	(800) 433-8812
Softools	C Compilers; ANSI C compatibility with ET emulator	(410) 750-3733
Software Development Systems	C; Uniware, IBM PC, VAX, UNIX/VMX, Apollo	(708) 990-4640
Z-World	Dynamic C; IBM PC	(916) 753-3722

Simulators/Applications Software

Company	Host/Comments	Phone
Avocet Systems	Simulator/IBM PC	(800) 448-8500
Lear Com Company	Simulator/IBM PC	(303) 232-2226
Logisoft	8080 to Z80 Translator	(408) 773-8465
Micromint	Z-System OS	(800) 635-3355
Softaid	Z80180 Guide, IBM PC diskette	(800) 433-8812
The AG Group	LLAP Dvmnt/Apple	(510) 937-7900

Z80 & Z80180 High Level Language Compilers

Company	Language Host	Phone
2500AD	C, IBM PC, CP/M, VAX	(800) 843-8144
American Automation	C, IBM PC	(714) 731-1661
Archimedes	C, IBM PC, Sun, VAX, HP	(415) 567-4010
Avocet Systems	C, IBM PC	(800) 448-8500
Laboratory	Forth IBM PC Microsystems	(213) 306-7412
Microtek Lab, Inc.	C, Pascal IBM PC,	(213) 321-2121
Microtek Research	Sun Micro, VAX	(408) 980-1300
MPE	Forth IBM PC	(716) 461-9187
Softaid	MT-Basic IBM PC	(800) 433-8812
Software Development Systems	C, IBM PC, VAX, Sun, Apollo	(708) 971-8170
Z-World	Dynamic C, IBM PC	(916) 753-3722

Note: Z80/64180 software is also compatible with the Z80180.

Simulators

Company	Host/Comments	Phone
Micro Methods, Inc.	IBM PC (ZRPM)	(503) 861-1765

High Level Language Compilers

Company	Language Host	Phone
2500AD	C, IBM PC, CP/M, VAX	(800) 843-8144
Computer Design Solutions	C, IBM PC	(704) 876-2346

Note: Z80 software is object code compatible with the Z280.

This is NOT a complete list of hardware and software vendors who support Zilog products. Please contact the Zilog sales office nearest you if what you are looking for is not on this list. This list is for reference only and is not an endorsement for any company.

Communications Software Support
SCC Physical Layer Drivers and Upper Layer Software

Company	Software	Phone
AT Barret Assoc.		(713) 728-8688
Forward Technology	Software drivers for SCCs/ESCCs	(516)496-9033
GCOM	Drivers for SCCs/ ESCCs/ISCC for many common protocols including Frame Relay, X.25, LAPD, SDLC/HDLC	(217) 337-4471
Probitas	LLAP Driver, AppleTalk® protocol stack, custom projects	(415) 941-2090
Real Time Kernel		(800) 525-4303
Trillium Digital Systems SCC Physical Layer, X.25, ISDN, Frame Relay Networking Layers		(310) 479-0500

Z80280 Hardware Support

Company	System Name	Phone
Computer Design Solutions	STD Buscard & Z280 Dvmnt. Board	(704) 876-2346
Softaid	Z280 ICE Analyzer	(800) 433-8812

68 PLCC Socket Manufacturers:
Methods, TNB, ITT, Cannon, Precicontact

Z80280 Assemblers and Cross Assemblers:

Company	Host/Comments	Phone
2500AD	IBM PC, CP/M, VAX	(800) 843-8144
Computer Design Solutions	IBM PC	(704) 876-2346

Z80380 Hardware Support

Company	System Name	Phone
Signum	In-Circuit Emulator	(805) 371-4608
Zilog	Z80380 Evaluation Kit	

Z380 Assemblers and Cross Assemblers:

Company	Host/Comments	Phone
PLC	IBM PC, Unix	(817) 599-8365
2500AD	IBM PC, CP/M, VAX	(800) 843-8144

Company	Product
Allen Ashley 395 Sierra Madre Villa Pasadena, CA 91107-2902 (818) 793-5748	Assembler Disassembler Simulator
Avocet Systems 120 Union Street Rockport, ME 04856 (800) 448-8500	Assembler
Byte Craft Limited 421 King Street North Waterloo, Ontario Canada N2J4E4 (519) 888-6911	C Compiler
Creative Technology 5144 Peachtree Road Suite 301 Atlanta, GA 30341 (404) 455-8255	Emulator
Cybernetic Micro Systems P.O. Box 3000 San Gregorio, CA 94074 (415) 726-3000	Assembler
Dantrol 1910 Rena Ln. Dalton, GA 30720 (404) 226-3714	Emulator
Data I/O, Inc. 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (206) 867-6829	OTP Programmer (Z86E21)
iSystems GmbH Einsteinstr. 5 W8050 Dachau, Germany (49) 8131-25085	Emulator
J K Engineering 37 Kallang Pudding Rd. Blk. B Tong Lee Bldg. #08-03 Singapore 1334 011-65-7448418	Emulator
Laboratory Microsystems 12555 West Jefferson Blvd. Los Angeles, CA 90060 (213) 306-7412	Forth Compiler

Company	Product
Logical Devices, Inc. 1201 NW 65th Place Fort Lauderdale, FL 33309 (800) 331-7766	OTP Programmer (Z86E21, Z86E22)
Micro Computer Control P.O. Box 275 / 17 Model Ave. Hopewell, NJ 08525 (609) 466-1751	Assembler C Compiler Simulator
Micro Dialects P.O. Box 30014 Cincinnati, OH 45230 (513) 271-9100	Assembler
MicroTime 10F No. 1180 Chen-De Rd. 11148 Taipei, Taiwan, R.O.C. 11-886-2-881-1791	Emulator
MPE 2604 Elmwood Ave. Rochester, NY 14618 (716) 461-9187	Forth Complier
Needham Electronics 4539 Orange Grove Ave. Sacramento, CA 95841 (916) 924-8037	OTP Programming
Orion Instruments 180 Independence Dr. Menlo Park, CA 94025 (415) 327-8800	Emulator
Production Languages Corp. P.O. Box 109 Weatherford, TX 76086-0109 (817) 599-8363	Assembler Simulator C Compiler
Pseudo Corp. 716 Thimble Shoals Blvd. Ste. E Newport News, VA 23606 (804) 873-1947	Assembler Disassembler Simulator
Signum Systems 171 E. Thousand Oaks Blvd. Thousand Oaks, CA 91360 (805) 371-4608	Emulator

Company	Product
Smart Access, Inc. 124 Robin Road Altamonte Springs, FL 32701 (407) 331-4724	OTP Programmer (Z86E21, Z86E22)
Software Development Systems 4248 Belle Aire Lane Downers Grove, IL 60515 (800) 448-7733	Assembler
Software Science 3750 Round Bottom Road Cincinnati, OH 45244 (513) 561-2060	Z8® Prototyping System

Company	Product
Western Wares P.O. Box C Norwood, CO 81423 (303) 327-4898	Assembler
Wytec 185C East Lake Street Ste. 140 Bloomingdale, IL 60108 (708) 894-1440	Emulator
2500AD Software, Inc. 109 Brookdale Ave. P.O. Box 480 Buena Vista, CO 81211 (719) 395-8683, or 800-843-8144	Assembler C Compiler Simulator

ZiLOG Telephone Answering Devices — Superintegration™ Products Guide

Block Diagram	ROM UART 8611 ⋮ CPU COUNTER/TIMERS | RAM P0 | P1 | P2 | P3	ROM CPU WDT | 236 RAM | P1 P2 | P3 | P0	Z8 | DSP 24K ROM | 4K ROM A/D | D/A 31 or 47 DIGITAL I/O	Z8 | DSP 24K ROM | 6K ROM A/D | D/A 31 or 47 DIGITAL I/O
Part Number	**Z8600/Z8611**	**Z86C30/E30/C31/E31**	**Z89C65/Z89C66**	**Z89165/Z89166**
Description	Z8® NMOS (CCP™) Z8600 = 2K ROM Z8611 = 4K ROM	Z8® Consumer Controller Processor (CCP™) Z86C30 = 28-Pin, 4K ROM Z86C31 = 28-Pin, 2K ROM Z86C40 = 40-Pin, 4K ROM Z86E30, Z86E31, Z86E40 = OTP Version	Telephone Answering Controller Z89C66 = ROMLess with 31 I/O Pins	Low-Cost DTAD Controller Z89166 = ROMLess with 31 I/O Pins
Process/Speed	NMOS: 8,12 MHz	CMOS: 12 MHz	CMOS: 20 MHz	CMOS: 20 MHz
Features	■ 2K/4K ROM ■ 128 Bytes RAM ■ 22/32 I/O Lines ■ On-Chip Oscillator ■ Two Counter/Timers ■ Six Vectored, Priority Interrupts ■ UART (Z8611 Only)	■ 4K ROM/236 RAM ■ Two Standby Modes ■ Two Counter/Timers ■ ROM/RAM Protect ■ Four Ports (Z86C40/E40) ■ Three Ports (Z86C30/E30/C31/E31) ■ Low-Voltage Protection ■ Two Analog Comparators ■ Low-EMI Option ■ Watch-Dog Timer (WDT) ■ Auto Power-On Reset ■ Low-Power Option	■ 24K ROM (Z89C65 Only) ■ 16-Bit DSP ■ 4K Word ROM ■ 8-Bit A/D with Automatic Gain Control (AGC) ■ DTMF Macro Available ■ LPC Macro Available ■ 10-Bit PWM D/A ■ Other DSP Software Options Available ■ 47 I/O Pins (Z89C65 Only)	■ 24K ROM (Z89165 Only) ■ 16-Bit DSP ■ 6K Word DSP ROM ■ 8-Bit A/D with Automatic Gain Control (AGC) ■ DTMF Macro Available ■ LPC Macro Available ■ 10-Bit PWM D/A ■ Other DSP Software Options Available ■ 47 I/O Pins (Z89165 Only)
Package	28-Pin DIP 40-Pin DIP 44-Pin PLCC	28-Pin DIP 40-Pin DIP 44-Pin PLCC, QFP	68-Pin PLCC	68-Pin PLCC 80-Pin QFP
Support Products	Z86C1200ZEM - Emulator Z0860000ZCO - Evaluation Board Z0860000ZDP - Adaptor Kit	Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator Z86C5000ZEM - Emulator Z86E3000ZDP - Adaptor Kit Z86E4000ZDP - Program Adaptor Kit	Z89C6501ZEM - Emulator Z89C6500ZDB - Emulator	Z89C6501ZEM - Emulator Z89C6500ZDB - Emulator Z8916500ZCO - Evaluation Board

ZiLOG Telephone Answering Devices — Superintegration™ Products Guide

Block Diagram	Z8 | DSP 24K/32K ROM | 6K ROM RAM PORT | CODEC INTF. RAM REFRESH | PWM 27 or 43 DIGITAL I/O	Z8 | DSP 24K ROM | 8K ROM RAM PORT | CODEC INTF. RAM REFRESH | CODEC INTF. 27 or 43 DIGITAL I/O	Z8 | DSP 32K ROM | 8K ROM RAM PORT | CODEC INTF. RAM REFRESH | CODEC INTF. 27 or 43 DIGITAL I/O
Part Number	**Z89C67/Z89C68/Z89C69**	**Z89167/Z89168**	**Z89169**
Description	Telephone Answering Controller Z89C67 = 24 Kbytes of Program ROM Z89C68 = ROMLess with 27 I/O Pins Z89C69 = 32 Kbytes of Program ROM	Enhanced Telephone Answering Controller Z89168 = ROMLess with 27 I/O Pins	Enhanced Telephone Answering Controller
Process/Speed	CMOS: 20 MHz	CMOS: 24 MHz	CMOS: 24 MHz
Features	■ 16-Bit DSP ■ 6K Word ROM ■ DTMF Macro Available ■ LPC Macro Available ■ 10-Bit PWM D/A ■ Other DSP Software Options Available ■ ARAM/DRAM/ROM Controller and Interface ■ Dual CODEC Interface ■ 43 I/O (Z89C67 Only)	■ 24K ROM (Z89167 Only) ■ 16-Bit DSP ■ 8K Word ROM ■ DTMF Macro Available ■ LPC Macro Available ■ 10-Bit PWM D/A ■ Other DSP Software Options Available ■ ARAM/DRAM/ROM ■ Dual CODEC Interface ■ 43 I/O (Z89167 Only)	■ 32K ROM ■ 16-Bit DSP ■ 8K Word ROM ■ DTMF Macro Available ■ LPC Macro Available ■ 10-Bit PWM D/A ■ Other DSP Software Options Available ■ ARAM/DRAM/ROM ■ Dual CODEC Interface ■ 43 I/O
Package	84-Pin PLCC	84-Pin PLCC 100-Pin QFP	84-Pin PLCC 100-Pin QFP
Support Products	Z89C5900ZEM - Emulator Z89C6700ZEM - Emulator Z89C6700ZDB - Emulator Z8916902ZCO - Evaluation Board	Z89C5900ZEM - Emulator Z89C6700ZEM - Emulator Z89C6700ZDB - Emulator Z8916902ZCO - Evaluation Board	Z89C5900ZEM - Emulator Z89C6700ZEM -Emulator Z89C6700ZDB - Emulator Z8916902ZCO - Evaluation Board

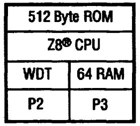
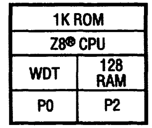
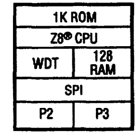
ZiLOG TV/Video Products — Superintegration™ Products Guide

Block Diagram	16/8K ROM 4K CHAR ROM Z8 CPU | RAM OSD 13 PWM | TIMER WDT | 5 PORTS	6K ROM 3K CHAR ROM Z8 CPU | RAM OSD 7 PWM | TIMER WDT | 3 PORTS	CHAR ROM COMMAND INTERPRETER ANALOG SYNC/DATA SLICER | OSD CTRL	1K/6K ROM Z8 CPU WDT | 124 RAM P2 | P3	2K/8K/16K ROM Z8 CPU WDT | 128,256, 768 RAM P0 | P1 | P2 | P3
Part Number	**Z86C27/127/97/47/E47**	**Z86227**	**Z86128/Z86228/Z86129**	**Z86L06/Z86L29**	**Z86L70/71/72/73/74 75/76/77/78**
Description	Digital Television Controller (DTC™) Television, VCRs, and Cable Z86E47 = OTP Version	Standard DTC™ Features with Reduced ROM, RAM, PWM Outputs for Greater Economy	Z86128/228 = Line 21 Closed Caption Controller (L21C™) Z86129/228 = Line 21 Closed Caption and EDS Controller	Z86L06 = Low-Voltage CMOS Consumer Controller Processor Z86L29 = 6K Infrared Remote Controller	Zilog Infrared Remote Controllers (ZIRC™) for IR Remote/Battery Operated Applications Ranging in ROM: L70=2K, L71=8K, L72&78=16K, L73&74=32K, L75=4K, L76=12K, L77=24K
Process/Speed	CMOS: 4 MHz	CMOS: 4 MHz	CMOS: 12 MHz	Low-Voltage CMOS: 8 MHz	Low-Voltage CMOS: 8 MHz
Features	■ 8K/16K/OTP ROM ■ 256 Byte RAM ■ 160x7-Bit Video RAM ■ On-Screen Display (OSD) Video Controller ■ Programmable – Color – Size – Position Attributes ■ 13 PWMs for D/A Conversion ■ 128-Character Set ■ 4Kx6-Bit Char. Gen. ROM ■ Watch-Dog Timer (WDT) ■ Low-Voltage Protection ■ Five Ports/36 Pins ■ Two Standby Modes ■ Low-EMI Mode	■ 6K ROM, 256 Byte RAM ■ 120x7-Bit Video RAM ■ OSD On-Board Programmable – Color – Size – Position Attributes ■ 7 PWMs ■ 96 Character Set ■ 3Kx6-Bit Char. Gen. ROM ■ Watch-Dog Timer (WDT) ■ Low-Voltage Protection ■ Three Ports/20 Pins ■ Two Standby Modes ■ Low-EMI Mode	■ Conforms to FCC Line 21 Format ■ Parallel or Serial Modes ■ Stand-Alone Operation ■ On-Board Data Sync and Slicer ■ On-Board Character Generator – Color – Blinking – Italic – Underline – Extended Data Services	■ 1K ROM and 6K ROM ■ Watch-Dog Timer (WDT) ■ Two Analog Comparators with Output Option ■ Two Standby Modes ■ Two Counter/Timers ■ Auto Power-On Reset ■ 2V Operation ■ RC Oscillator Option ■ Low-Noise Option ■ Low-Voltage Protection ■ High-Current Drivers (2, 4)	■ Watch-Dog Timer (WDT) ■ Two Analog Comparators with Output Option ■ Two Standby Modes ■ Two Enhanced Counter/Timers – Auto Pulse – Reception/Generation ■ Auto Power-On Reset ■ 2V Operation ■ RC Oscillator Option ■ Low-Voltage Protection ■ High-Current Drivers – Three OTP Versions Available – Z86E72/73/74
Package	64-Pin DIP	40-Pin DIP	18-Pin DIP	18-Pin DIP 18-Pin SOIC	Z86L71=20-Pin DIP/SOIC Z86L70/L75=18-Pin DIP, SOIC Z86L72/L76/L77=40,44-Pin DIP, PLCC, QFP Z86L74=64/68-Pin
Support Products	Z86C2700ZCO - Evaluation Board Z86C2700ZDB - Emulator Z86C2700ZEM - Emulator	Z86C2700ZDB - Emulator Z86C2702ZEM - Emulator Z86C2700ZCO - Evaluation Board	Support Documentation Provided with the device	Z86C5000ZEM - Emulator	Z86L7200TSC - Emulator Z86L7100ZEM - Emulator Z86L7100ZDB - Emulator

ZiLOG TV/Video Products — Superintegration™ Products Guide

Block Diagram	4K ROM CPU WDT | 236 RAM | P1 P2 | P3 | P0	16K ROM | UART CPU | 236 RAM P0 | P1 | P2 P3 | P4 | P5 | P6	12K/16K/24K ROM DSP CORE RAM I^2C OSD CCD PWM | WDT | 2 PORTS	12K/16K/24K ROM DSP CORE RAM I^2C OSD CCD PWM | WDT | 2 PORTS	32K OTP | 16K ROM DSP CORE RAM I^2C OSD CCD PWM | WDT | 2 PORTS
Part Number	**Z86C40/Z86E40**	**Z86C61/Z86C62**	**Z89300/02/04/06/14**	**Z89301/03/05/07/13**	**Z89331/Z89336**
Description	Z8® Consumer Controller Processor (CCP™) Z86E40 = OTP Version	Z8® MCU with Expanded I/Os	Advanced TV Controller with Closed Caption Decoder (CCD), StarSight*, OSD for TV, VCR, Cable, Satellite Z89301 = OTP Version	Advanced TV Controller with CCD StarSight, for TV, VCR, Cable, Satellite Z89301 = OTP Version	Advanced TV Controller with CCD StarSight, OSD for TV, VCR, Cable, Satellite Z89301 = OTP Version
Process/Speed	CMOS: 12 MHz	CMOS: 16, 20 MHz	CMOS: 12 MHz	CMOS: 12 MHz	CMOS: 12 MHz
Features	■ 4K ROM, 236 RAM ■ Two Standby Modes ■ Two Counter/Timers ■ ROM Protect ■ RAM Protect ■ Four Ports ■ Low-Voltage Protection ■ Two Analog Comparators ■ Low-EMI Mode ■ Watch-Dog Timer (WDT) ■ Auto Power-On Reset ■ Low-Power Option	■ 16K ROM ■ Full-Duplex UART ■ Two Standby Modes (STOP and HALT) ■ Two Counter/Timers ■ ROM Protect Option ■ RAM Protect Option ■ Pin Compatible to Z86C21 ■ Z86C61 = Four Ports ■ Z86C62 = Seven Ports	■ StarSight Capability ■ Closed-Captioning ■ DSP 12 MHz ■ 16-Bit, 512 Byte (Z89314) ■ 640 Byte RAM ■ 12K/16K/24K ROM ■ Programmable OSD ■ I^2C*, 7 PWM ■ 3-Channel ADC ■ Watch-Dog Timer (WDT) ■ Two Ports ■ 32 kHz, XTAL ■ Low-Power Mode *Not Available on Z89314	■ StarSight Capability ■ Closed-Captioning ■ DSP 12 MHz ■ 16-Bit, 640 Byte RAM ■ 12K/16K/24K ROM ■ Programmable OSD ■ I^2C, 9 PWM ■ 4-Channel ADC ■ Watch-Dog Timer (WDT) ■ Two Ports ■ 32 kHz, XTAL ■ Low-Power Mode	■ StarSight Capability ■ Closed-Captioning ■ DSP 12 MHz ■ 16-Bit, 640 Byte RAM ■ 12K/16K/24K ROM ■ Programmable OSD ■ I^2C, 7 PWM ■ 5-Channel ADC ■ Watch-Dog Timer (WDT) ■ Two Ports ■ 32 kHz, XTAL ■ Low-Power Mode
Package	40-Pin DIP 44-Pin PLCC	Z86C61 = 40-Pin DIP Z86C61 = 44-Pin PLCC,QFP Z86C62 = 68-Pin PLCC	40-Pin SDIP	52-Pin SDIP	42-Pin SDIP
Support Products	Z86C5000ZEM - Emulator Z86CCP00ZEM - Emulator Z86E4000ZDP - Adaptor Kit Z86E4000ZDV - Adaptor Kit	Z86C5000ZEM - Emulator Z86CCP00ZEM - Emulator	Z8930900ZEM - Emulator Z8930900TSC - Emulator Z8930901TSC - Emulator	Z8930900ZEM - Emulator Z8930900TSC - Emulator Z8930901TSC - Emulator	Z8930900ZEM - Emulator Z8930900TSC - Emulator Z8930901TSC - Emulator

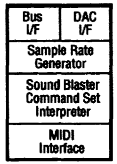
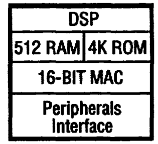
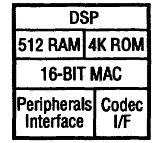
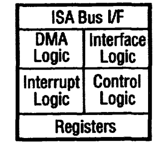
Zilog Discrete Z8® Microcontroller — Superintegration™ Products Guide

Block Diagram			
Part Number	**Z86C03**	**Z86C04/Z86E04**	**Z86C06**
Description	Consumer Controller Processor (CCP™) with 512 Byte ROM	Z86C04 = 8-Bit Low Cost 1 Kbyte ROM MCU Z86E04 = OTP Version	Consumer Controller Processor (CCP™) with 1 Kbyte ROM
Process/Speed	CMOS: 8 MHz	CMOS: 8 MHz	CMOS: 12 MHz
Features	■ 512 Byte ROM ■ 64 Byte RAM ■ Two Standby Modes ■ One Counter/Timer ■ ROM Protect ■ Two Analog Comparator ■ Auto Power-On Reset ■ Low-Voltage Protection ■ 14 I/O ■ RC Oscillator Option ■ Low-Noise Option	■ 1 Kbyte ROM ■ 128 Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparator ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 14 I/O ■ Low-Noise Option	■ 1 Kbyte ROM ■ 128-Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparator ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 14 I/O ■ RC Oscillator Option ■ Serial Peripheral Interface (SPI)
Package	18-Pin DIP 18-Pin SOIC	18-Pin DIP 18-Pin SOIC	18-Pin DIP 18-Pin SOIC
Support Products	Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator	Z86C0800ZCO - Evaluation Board Z86C0800ZDP - Adaptor Kit Z86C1200ZEM - Emulator Z86C1200ZPD - Adaptor Kit Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator	Z86E0600ZDP - Adaptor Kit Z86C5000ZEM - Emulator Z86C5000ZDP - Adaptor Kit Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator

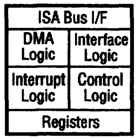
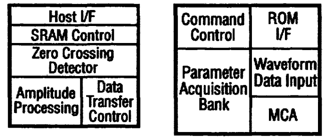
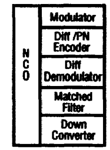
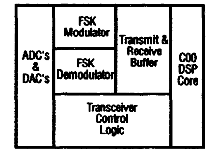
ZiLOG Discrete Z8® Microcontroller — Superintegration™ Products Guide

Block Diagram	2K ROM Z8® CPU WDT | 128 RAM P0 | P2	4K ROM Z8® CPU WDT | 236 RAM P0 | P3 P2	2K ROM Z8® CPU WDT | 128 RAM P0 | P3 P2
Part Number	**Z86C08/Z86E08**	**Z86C30/Z86E30**	**Z86C31/Z86E31**
Description	Z86C08 = Z8® MCU with 2 Kbyte ROM Z86E08 = OTP Version	Z86C30 = Z8® (CCP™) with 4 Kbyte ROM Z86E30 = OTP Version	Z86C31 = 8-Bit MCU with 2 Kbyte ROM Z86E31 = OTP Version
Process/Speed	CMOS: 12 MHz	CMOS: 12 MHz	CMOS: 8 MHz
Features	■ 2 Kbyte ROM ■ 128 Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparators ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 14 I/O ■ Low-Noise Option	■ 4 Kbyte ROM ■ 236 Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparators ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 24 I/O ■ RC Oscillator Option ■ Low-Noise Option	■ 2 Kbyte ROM ■ 128 Byte RAM ■ Two Standby Modes ■ Two Counter/Timer ■ ROM Protect ■ Two Analog Comparators ■ Auto Power-On Reset ■ Low-Voltage Protection (ROM Only) ■ 24 I/O ■ RC Oscillator Option ■ Low-Noise Option
Package	18-Pin DIP 18-Pin SOIC	28-Pin DIP	28-Pin DIP 28-Pin PLCC
Support Products	Z86C0800ZCO - Evaluation Board Z86C0800ZDP - Adaptor Kit Z86C1200ZEM - Emulator Z86C1200ZDP - Adaptor Kit Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator	Z86E3000ZDP - Adaptor Kit Z86C5000ZEM - Emulator Z86C5000ZPD - Emulator Pod Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator	Z86E3000ZDP - Adaptor Kit Z86C5000ZEM - Emulator Z86C5000ZPD - Emulator Pod Z86CCP00ZEM - Emulator Z86CCP00ZAC - Emulator

ZiLOG Multimedia/PC Audio — Superintegration™ Products Guide

Block Diagram				
Part Number	**Z86321**	**Z89320**	**Z89321/Z89371**	**Z5380**
Description	8-Bit Digital Audio Processor	16-Bit Digital Signal Processor	16-Bit Digital Signal Processor Z89371= OTP Version	Small Computer System Interface (SCSI)
Process/Speed	CMOS: 12 MHz	CMOS: 10 MHz	CMOS: 20 MHz	Clock: 1.5 Mb/s
Features	■ Sound Blaster™ Compatible ■ ADPCM Decompression ■ 8-Bit DAC Interface ■ Successive Approximation ADC Algoritant ■ MIDI Interface	■ 16-Bit Multiply/Accumulate ■ 100 ns ■ 512 Word RAM ■ 4K Word RAM ■ Peripherals Interface Bus ■ 74 Instruction Set	■ 16-Bit Multiply/Accumulate ■ 50 µs ■ 512 Word RAM ■ 4K Word ROM ■ Peripherals Interface Bus ■ CODEC Interface	■ Compatible 5380 Pin-out ■ CMOS ■ Asynchronous I/F Supports 1.5 Mb/s ■ 48 mA Drivers ■ Arbitration Support ■ Support Normal or Block Mode DMA
Package	40-Pin DIP 44-Pin PLCC	40-Pin DIP 44-Pin PLCC	40-Pin DIP 44-Pin PLCC	40-Pin DIP 44-Pin PLCC
Support Products	Support Documentation Provided with Device	Z89C0000ZEM - Emulator	Z8937100ZEM - Emulator	Support Documentation Provided with Device

SoundBlaster™ is a Trademark of Creative Labs, Inc.

ZiLOG	Multimedia/PC Audio		Wireless Devices	
Block Diagram				
Part Number	**Z53C80**	**Z89341/Z89342**	**Z2000***	**Z87000**
Description	SCSI Adaptor	Wave Synthesis Chip Set	Spread Spectrum Burst Processor	Cordless Phone Transceiver/Controller
Speed MHz	Clock: 3 Mb/s	CMOS: 36 MHz	CMOS: 45 MHz Clock: 2.048 Mb/s	CMOS: 16.384 MHz
Features	■ ANSI X3, 131-1986 Standard ■ DMA or Programmed I/O Data Transfers ■ Asynchronous Interface Support ■ 3 Mb/s ■ ISA Bus I/F ■ Glitch Eater	■ 4-Channel ■ 16-Bit Linear ■ PCM Sound Generator ■ Sampling Rates 20 kHz to 44.1 kHz ■ Support 16-, 18-, and 20-Bit DAC ■ Audio Bandwidth 0 Hz to 20,000 Hz ■ Direct Interface with PC ISA Bus ■ Direct Support 4Mx16 ROM	■ Operates up to 11.1264 Mchips Second in Transmit and Receive Modes ■ Maximum Data Rate of 2.048 Mbps in Conformance with FCC Regulations ■ Supports Differentially Encoded BPSK or QPSK Modulation ■ Full-or Half-Duplex Operation for FDD or TDD Implementations ■ Two Independent PN Sequences ■ Power Management Features	■ Supports 900 MHz Spread Spectrum Cordless Phone Design ■ Adaptive Frequency Hopping ■ Transmit Power Control ■ Bus Interface to ADPCM Processor ■ 12K Words of RAM for Transceiver and Phone Control Software ■ 32 Pins of Program I/O ■ ROM Code, OTP and ICEBOX™ Version to be Available Q3/94
Package	40-Pin DIP 44-Pin PLCC	84-Pin PLCC	100-Pin VQFP	84-Pin PLCC
Support Products	Support Documentation Provided with Device	Support Documentation Provided with Device	Z0200000ZC0 - Evaluation Board	Z870000ZEM - Emulator

*Z2000 is sold under license from Stanford Telecommunications, Inc. ASIC and Custom Products Division

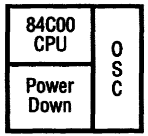
Block Diagram	4K ROM Z8® CPU | RAM Counter/Timers WDT P0 | P1 | P2 | P3	2/4K ROM Z8® CPU | RAM Counter/Timers P0 | P1 | P2 | P3	8K OTP/ROM Z8® CPU | RAM Counter/Timer P0 | P1 | P2 | P3	2K ROM Z8® CPU | RAM Counter/Timer WDT P0 | P2 | P3
Part Number	**Z8615**	**Z8614/Z8602**	**Z86E23**	**Z86C17**
Description	Keyboard MCU	Z8602 = 2K ROM Keyboard MCU Z8614 = 4K ROM Keyboard MCU	Keyboard OTP MCU	Mouse MCU
Process/Speed	NMOS: 4, 5 MHz	NMOS: 4 MHz	CMOS: 4 MHz	CMOS: 4 MHz
Features	■ 4K ROM ■ 124-Byte RAM ■ 32 I/O Lines ■ Two Counter/Timers ■ Watch-Dog Timer (WDT) ■ RC Oscillator ■ Dedicated Row Column Pins ■ Data/Clock Pins ■ Direct Connect LED Pins	■ 4K ROM ■ 124 Byte RAM ■ 32 I/O Lines ■ Two Counter/Timers ■ Dedicated Row Column Pins	■ 8K ROM ■ 256 Byte RAM ■ 32 I/O Lines ■ Two Counter/Timers ■ Dedicated Row Column Pins	■ 2K ROM ■ 124 Byte RAM ■ 14 I/O Lines ■ Two Counter/Timers ■ Dedicated Opto-Transistor Pins ■ Integrated Pull-up Resistors ■ Power-Down Modes ■ Power-On Reset (POR) ■ Watch-Dog Timer (WDT)
Package	40-Pin DIP 44-Pin PLCC	40-Pin DIP 44-Pin PLCC	40-Pin DIP 44-Pin PLCC	18-Pin DIP 18-Pin SOIC
Support Products	Z0861500ZCO - Evaluation Board Z86C1200ZEM -Emulator Z0861500ZDP - Adaptor Kit	Z0860200ZCO - Evaluation Board Z86C1200ZEM - Emulator Z0860200ZDP - Adaptor Kit Z86C1200ZPD - Emulator Pod	Z0860200ZCO - Evaluation Board Z86C1200ZEM - Emulator Z0860200ZDP - Adaptor Kit	Z86C1200ZEM - Emulator

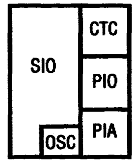
ZiLOG Keyboard/Input Devices — Superintegration™ Products Guide

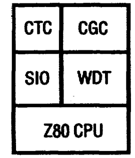
Block Diagram	2K ROM Z8® CPU | RAM Counter/Timer WDT Comparators P0 | P2 | P3	1K ROM Z8® CPU | RAM Counter/Timer WDT Comparators P0 | P2 | P3	4K ROM DSP | RAM Counter/Timer Codec Interface 16-Bit MAC | DATA I/O	4K ROM Z8® MCU | RAM Counter/Timer WDT Comparators P0 | P2 | P3
Part Number	**Z86C08/Z86C07/Z86E08**	**Z86C04/Z86E04**	**Z89321/Z89371**	**Z86C30/Z86E30**
Description	Pointing Device Z8® MCU Z86E08 = OTP Version	Discrete MCU Z86E04 = OTP Version	16-Bit Digital Signal Processor Z89371 = OTP Version	Z8® MCU Z86E30 = OTP Version
Process/Speed	CMOS: 4,8,12 MHz	CMOS: 4 MHz	CMOS: 15, 20 MHz	CMOS: 8, 12 MHz
Features	■ 2K ROM ■ 124 Byte RAM ■ 14 I/O Lines ■ Two Counter/Timers ■ Power-Down Modes ■ Two Comparators ■ Power-On Reset (POR) ■ Watch-Dog Timer (WDT) ■ Auto Latch (Z86C07 Only)	■ 1K ROM ■ 124 Byte RAM ■ 14 I/O Lines ■ Two Counter/Timers ■ Power-Down Modes ■ Two Comparators ■ Power-On Reset (POR) ■ Watch-Dog Timer (WDT)	■ 4K Word ROM ■ 512 Word RAM ■ 16 Bit I/O Bus ■ Two Counter/Timers ■ CODEC Interface ■ 50/75 ns Cycle Timer ■ 4K OTP ROM (Z89371 Only)	■ 4K Word ROM ■ 256 Byte RAM ■ 24 I/O Lines ■ 2 Counter/Timers ■ Power-Down Mode ■ Two Comparators ■ Power-On Reset (POR) ■ Watch-Dog Timer (WDT)
Package	18-Pin DIP 18-Pin SOIC	18-Pin DIP 18-Pin SOIC	40-Pin DIP 44-Pin PLCC	28-Pin DIP 28-Pin SOIC
Support Products	Z86C1200ZEM - Emulator	Z86C1200ZEM - Emulator Z86CCP00ZEM - Emulator	Z8937100ZEM - Emulator Z8937100TSC - Emulator	Z86C5000ZEM - Emulator

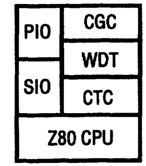
ZILOG Z80® EMBEDDED CONTROLLERS — SUPERINTEGRATION™ PRODUCTS GUIDE

BLOCK DIAGRAM



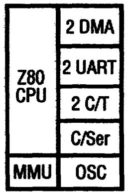
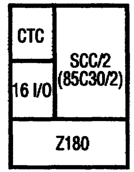
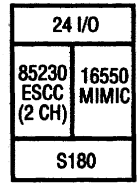
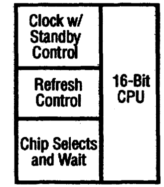






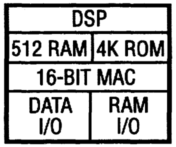
PART NUMBER	**Z84C01**	**Z84C90**	**Z84013/Z84C13**	**Z84015/Z84C15**
DESCRIPTION	Z80® CPU with Clock Generator/Clock	Killer I/O (Three Z80® Peripherals)	Intelligent Peripheral Controller	Enhanced Intelligent Peripheral
PROCESS/SPEED	CMOS: 10 MHz	CMOS: 8, 10, 12 MHz	Z84013 = CMOS: 6, 10 MHz Z84C13 = CMOS: 6, 10 MHz	Z84015 = CMOS: 6, 10 MHz Z84C15 = CMOS: 16 MHz
FEATURES	■ Clock Generator/Controller ■ Four Power Down Modes	■ Serial Input/Output (SIO) ■ Counter/Timer Circuit (CTC) ■ Plus Eight I/O Lines ■ Three 8-Bit Ports	■ Serial Input/Output (SIO) ■ Counter/Timer Circuit (CTC) ■ Watch-Dog Timer (WDT) ■ Clock Generator Circuit (CGC) ■ Wait State Generator (WSG) ■ Power-On Reset (POR) ■ Two Chip Selects ■ Evaluation Mode	■ Serial Input/Output (SIO) ■ Counter/Timer Circuit (CTC) ■ Watch-Dog Timer (WDT) ■ Clock Generator Circuit (CGC) ■ Four Power-Down Modes ■ Power-On Reset ■ Two Chip Selects ■ 32-Bit CRC ■ Wait State Generator (WSG) ■ Evaluation Mode
PACKAGE	44-Pin QFP 44-Pin PLCC	84-Pin PLCC 80-Pin QFP	84-Pin PLCC	100-Pin QFP 100-Pin VQFP
SUPPORT PRODUCTS	Z84C9000ZCO - Evaluation Board	Z84C9000ZCO - Evaluation Board	Z84C1500ZCO - Evaluation Board	Z84C1500ZCO - Evaluation Board

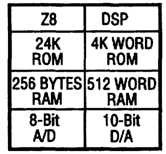
ZILOG Z80® EMBEDDED CONTROLLERS — SUPERINTEGRATION™ PRODUCTS GUIDE

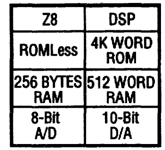
Block Diagram				
Part Number	**Z80180/Z8S180/Z8L180**	**Z80181**	**Z80182/Z8L182**	**Z80380/Z8L380**
Description	High-Performance Z80® CPU with Peripherals Z8S180 = Static Version Z8L180 = Low-Voltage Version	Smart Access Controller	Zilog Intelligent Peripheral (ZIP™) Z8L182 = Low-Voltage Version	Z380™ Microprocessor Z8L380 = Low-Voltage Z380
Process/Speed	Z80180 = CMOS: 6, 8, 10, MHz Z8S180 = CMOS: 16 MHz Z8L180 = CMOS: 20, 33 MHz	CMOS: 10, 12 MHz	Z80182 = CMOS: 16, 33 MHz Z8L182 = CMOS: 20 MHz	Z8L380 = CMOS: 10 MHz Z80380 = CMOS: 16, 18 MHz
Features	■ Enhanced Z80® CPU ■ 1 Mbyte MMU ■ 2 DMAs ■ 2 UARTs with Baud Rate Generators ■ C/Serial I/O Port Oscillator ■ Z8S180 Includes; – Power-Down – Programmable EMI – Divide-By-One – Clock Option – 3.3V and 5V Version	■ Complete Z180™ plus SCC/2 Counter/Timer Circuit ■ 16 I/O Lines ■ Emulation Mode	■ Static Version of Z180™ plus ESCC (2 Channels of Z85230 with 32-Bit CRC Not Available for 16 MHz) ■ 16550 MIMIC ■ 24 Parallel I/O ■ Emulation Mode ■ 3.3V and 5V Version	■ 16/32-Bit MPU ■ Internal 32-Bit Datapaths and ALU ■ 2 Clocks/Cycle Instruction Execution up to 4 Gbytes of Linear Addressing ■ Enhanced Instruction Set ■ 4 Banks of On-Chip Register Files ■ Object-Code Compatible with Z80/Z180 Microprocessors up to 6 Programmable Memory Chip Selects ■ 3.3V and 5V Version
Package	64-Pin DIP 68-Pin PLCC 80-Pin QFP	100-Pin QFP	100-Pin QFP 100-Pin VQFP	100-Pin QFP
Support Products	Z8S18000ZCO - Evaluation Board ZEPMIP00001 - EPM™ Manual	Z8018100ZCO - Evaluation Board Z8018100ZDP - Adaptor Kit Z8018101ZCO* - Evaluation Board * Includes LLAP software that can be licensed (Z80181ZA6). ZEPMIP00001- EPM™ Manual	Z8018200ZCO - Evaluation Board ZEPMIP00002 - EPM™ Manual	Z8038000ZCO - Evaluation Board ZEPMIP00003 - EPM™ Manual

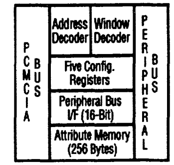
ZiLOG Modem/Fax — Superintegration™ Products Guide

Block Diagram



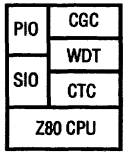
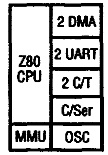
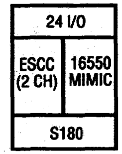
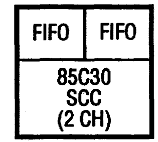




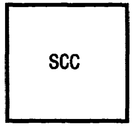
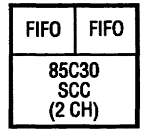
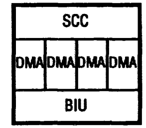
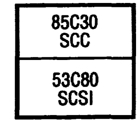


Part Number	**Z89C00**	**Z89120**	**Z89920**	**Z86017**
Description	16-Bit Digital Signal Processor	Zilog Modem/Fax Controller	Zilog Modem/Fax Controller	PCMCIA Interface Adaptor
Process/Speed	CMOS: 10, 15 MHz	CMOS: 20 MHz	CMOS: 20 MHz	CMOS: 20 MHz
Features	■ 16-Bit Multiply/Accumulate ■ 75 ns ■ Two Data RAMs (256 Words each) ■ 4K Word ROM ■ 64Kx16 Ext. ROM ■ 16-Bit I/O Port ■ 74 Instructions ■ Most Single Cycle ■ Two Conditional Branch Inputs, Two User Outputs ■ Library of Macros ■ Zero Overhead Pointers	■ Z8® with 24 Kbyte ROM ■ 16-Bit DSP with 4K Word ROM ■ 8-Bit A/D ■ 10-Bit D/A (PWM) ■ Library of Macros ■ 47 I/O Pins ■ Two Comparators Independent Z8® and DSP Operations Power-Down Mode	■ Z8 with 64K External Memory ■ DSP with 4K Word ROM ■ 8-Bit A/D ■ 10-Bit D/A ■ Library of Macros ■ 47 I/O Pins ■ Two Comparators Independent Z8® and DSP Operations Power-Down Mode	■ 256 Bytes of Attribute Memory ■ Five Configuration Registers ■ EEPROM Sequencer or SPI Interface ■ PCMCIA to I/O, Memory or Both ■ PCMCIA to ATA/IDE ■ ATA/IDE to ATA/IDE ■ 3.0V to 5.5V Operation ■ 8- or 16-Bit Peripheral Support
Package	68-Pin PLCC 60-Pin VQFP	68-Pin PLCC	68-Pin PLCC	100-Pin VQFP
Support Products	Z89C0000ZEM - Emulator Z89C0000ZCC - Emulator	Z89C6501ZEM - Emulator Z89C6500ZDP - Emulator	Z89C6501ZEM - Emulator Z89C6500ZDB - Emulator	Z8601700ZCO - Evaluation Board

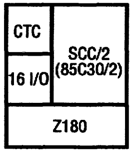
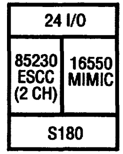
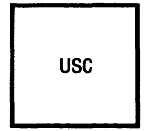
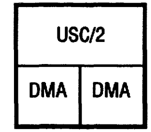
ZILOG MODEM/FAX — SUPERINTEGRATION™ PRODUCTS GUIDE

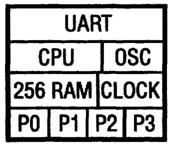
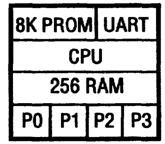
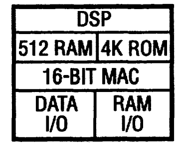
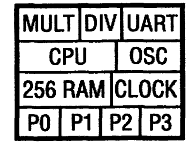
Block Diagram				
Part Number	**Z84C15/Z84015**	**Z80180/Z8S180/Z8L180**	**Z80182/Z8L182**	**Z85230**
Description	Enhanced Intelligent Peripheral Controller	High-Performance Z80® CPU with Peripherals Z8S180 = Static Version Z8L180 = Low-Voltage Version	Zilog Intelligent Peripheral (ZIP™) Z8L182 = Low-Voltage Version	Enhanced Serial Communication Controller
Process/Speed	Z84015 = CMOS: 6, 10 MHz Z84C15 = CMOS: 16 MHz	Z80180 = CMOS: 6, 8, 10, MHz Z8S180 = CMOS: 16 MHz Z8L180 = CMOS: 20, 33 MHz	Z80182 = CMOS: 16, 18, 33 MHz Z8L182 = CMOS: 20 MHz	CMOS: 8, 10,16, 20 MHz
Features	■ Z80® CPU, Serial Input/Output (SIO) ■ Counter/Timer Circuit (CTC) ■ Watch-Dog Timer (WDT) ■ Clock Generator Circuit (CGC) ■ Four Power-Down Modes Z84C15 Enhancements Include: ■ Power-On Reset ■ Two Chip Selects ■ 32-Bit CRC ■ Wait State Generator (WSG) ■ Evaluation Mode	■ Enhanced Z80® CPU ■ 1 Mbyte MMU ■ 2 DMAs ■ 2 UARTs with Baud Rate Generators ■ C/Serial I/O Port Oscillator ■ Z8S180 Includes; – Power Down – Programmable EMI – Divide-By-One – Clock Option – 3.3V and 5V Version	■ Static Version of Z180™ plus ESCC (Two Channels of Z85230 with 32-Bit CRC Not Available for 16 MHz) ■ 16550 MIMIC ■ 24 Parallel I/O ■ Emulation Mode ■ 3.3V and 5V Version	■ Full Dual-Channel ■ SCC Plus Deeper FIFOs: – 4 Bytes on Transceivers – 8 Bytes on Receivers ■ DPLL Counter Per Channel ■ Software Compatible to SCC
Package	100-Pin QFP 100-Pin VQFP	64-Pin DIP 68-Pin PLCC 80-Pin QFP	100-Pin QFP 100-Pin VQFP	40-Pin DIP 44-Pin PLCC
Support Products	Z84C1500ZCO - Evaluation Board	Z8S18000ZCO - Evaluation Board ZEPMIP00001- EPM™ Manual	Z8018200ZCO - Evaluation Board ZEPMIP00002 - EPM™ Manual	Z8S18000ZCO - Evaluation Board Z8038000ZCO - Evaluation Board Z8523000ZCO - Evaluation Board Z8018600ZCO - Evaluation Board ZEPMDC00002 - EPM™ Manual

ZiLOG Serial Communications — Superintegration™ Products Guide

Block Diagram				
Part Number	**Z8030/Z80C30 Z8530/Z85C30**	**Z85230/Z80230 Z85233**	**Z16C35**	**Z85C80**
Description	Serial Communication Controller Z8030/Z80C30 = Multiplexed Bus Z8530/Z85C30 = Non-Multiplexed Bus	Enhanced Serial Communication Controller Z8230/Z80230 = Dual Channel Z85233 = Single Channel	Integrated Serial Communication Controller	SCSCI Serial Communication and Small Computer Interface
Process/Speed	Z8030/Z8530 = NMOS: 4, 6, 8 MHz Z80C30/Z85C30 = CMOS: 8,10 16 MHz Clock: 2, 2.5, 4 Mb/s	CMOS: 10, 16 20 MHz Clock: 2.5, 4.0, 5.0 Mb/s	CMOS: 10, 16 MHz Clock: 2.5, 4.0 Mb/s	CMOS: 10, 16 MHz Clock: 2.5 Mb/s
Features	■ Two Independent Full-Duplex Channels ■ Enhanced DMA Support: ■ 10x19 Status FIFO ■ 14-Bit Byte Counter ■ NRZ/NRZI/FM Encoding Modes	■ Full Dual-Channel SCC Plus Deeper FIFOs: – 4 Bytes on Transmitters – 8 Bytes on Receivers ■ DPLL Counter Per Channel ■ Software Compatible to SCC	■ Full Dual-Channel SCC ■ Four DMA Controllers ■ Bus Interface Unit	■ Two Independent Full-Duplex Channels ■ Direct SCSI Bus Interface ■ Supports SCSI ANSI-X3.131-1986 Standard
Package	40-Pin DIP 44-Pin CERDIP 44-Pin PLCC	40-Pin DIP 44-Pin PLCC 44-Pin QFP (Z85233 Only)	68-Pin PLCC	68-Pin PLCC 100-Pin VQFP
Support Products	Z8018600ZCO - Evaluation Board Z8523000ZCO - Evaluation Board Z8018100ZCO - Evaluation Board ZEPMD000002 - EPM™ Manual	Z8018600ZCO - Evaluation Board Z8S18000ZCO - Evaluation Board Z8038000ZCO - Evaluation Board Z8523000ZCO - Evaluation Board ZEPMDC00002 - EPM™ Manual	Z8018600ZCO - Evaluation Board	ZEPMD00002 - EPM™ Manual

ZiLOG Serial Communications — Superintegration™ Products Guide

Block Diagram				
Part Number	**Z80181**	**Z80182/Z8L182**	**Z16C30**	**Z16C32**
Description	Smart Access Controller	Zilog Intelligent Peripheral (ZIP™) Z80L182 = Low-Voltage Version	Universal Serial Controller (USC®)	Integrated Universal Serial Controller
Process/Speed	CMOS: 10, 12 MHz	Z80182 = CMOS: 16,18, 33 MHz Z8L182 = CMOS: 20 MHz	CMOS: 10 MHz CPU Bus 10 Mb/s	CMOS: 20 MHz DMA Clock 20 Mb/s
Features	■ Complete Z180™ plus SCC/2CTC ■ 16 I/O Lines ■ Emulation Mode	■ Complete Static Version of Z180™ plus ESCC (2 Channels of Z85230 with 32-Bit CRC not Available for 16 MHz) ■ 16550 MIMIC ■ 24 Parallel I/O ■ Emulation Mode ■ 3.3V and 5V Version	■ Two Dual-Channel 32-Byte Receive and Transmit FIFOs ■ 16-Bit Bus B/W:18.2 Mb/s ■ Two BRGs Per Channel ■ Flexible 8/16-Bit Bus Interface ■ 12 Serial Protocols ■ Eight Data Encoding Bits	■ Single-Channel (Half of USC) plus two DMA Controllers ■ Array Chained and Linked-List Modes with Ring Buffer Support
Package	100-Pin QFP	100-Pin QFP 100-Pin VQFP	68-Pin PLCC	68-Pin PLCC
Support Products	Z8018100ZCO - Evaluation Board Z8018100ZDP - Adaptor Kit Z8018101ZCO* - Evaluation Board ZEPMIP00001 - EPM™ Manual * Includes LLAP software that can be licensed (Z80181ZA6)	Z8018200ZCO - Evaluation Board ZEPMIP00002 - EPM™ Manual	Z16C3001ZCO - Evaluation Board Z8018600ZCO - Evaluation Board ZEPMDC00001 - EPM™ Manual	Z16C3200ZCO - Evaluation Board Z8018600ZCO - Evaluation Board ZEPMDC00001 - USC® EPM™ Manual

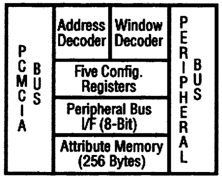
BLOCK DIAGRAM				
PART NUMBER	**Z86C91/Z8691**	**Z86E21/Z86C21**	**Z89C00**	**Z86C93**
DESCRIPTION	ROMLess Z8®	Z86E21 = 8K OTP Z86C21 = 8K ROM	16-Bit Digital Signal Processor	ROMLess Enhanced Z8® Mult/Div
PROCESS/SPEED	Z86C91 = CMOS: 16 MHz Z8691 = NMOS: 12 MHz	CMOS: 12, 16 MHz	CMOS: 10, 15 MHz	CMOS: 20, 25, 33 MHz
FEATURES	■ Full-Duplex UART ■ Two Standby Modes (STOP and HALT) ■ 2x8 Bit ■ Counter/Timer	■ 256 Byte RAM ■ Full-Duplex UART ■ Two Standby Modes (STOP and HALT) ■ Two Counter/Timers ■ ROM Protect Option ■ RAM Protect Option ■ Low-EMI Option	■ 16-Bit Multiply/Accumulate ■ 75 ns ■ Two Data RAMs (256 Words Each) ■ 4K Word ROM ■ 64Kx16 Ext. ROM ■ 16-Bit I/O Port ■ 74 Instructions ■ Most Single Cycle ■ Two Conditional Branch Inputs, Two User Outputs ■ Library of Macros ■ Zero Overhead Pointers	■ 16x16 Multiply 17 Clocks ■ 32x16 Divide 20 Clocks ■ Full-Duplex UART ■ Two Standby Modes (STOP and HALT) ■ Three 16-Bit Counter/Timers
PACKAGE	40-Pin DIP 44-Pin PLCC 44-Pin QFP	40-Pin DIP 44-Pin PLCC 44-Pin QFP	68-Pin PLCC	40-Pin DIP 44-Pin PLCC 44-Pin QFP
SUPPORT PRODUCTS	Z0860000ZCO - Evaluation Board Z86C0000ZUSP064 - Signum Emulator Z86C1200ZPD - Signum Emulator Pod	Z0860000ZCO - Evaluation Board Z86C0000ZUSP064 - Signum Emulator Z86C1200ZPD - Signum Emulator Pod	Z89C00ZEM - Emulator	Z0860000ZCO - Evaluation Board Z86C0000ZUSP064 - Signum Emulator Z86C0001ZUSP064 - Signum Emulator Z86C9300ZPD - Signum Emulator Pod Z86C9301ZPD - Signum Emulator Pod

Block Diagram	MULT | DIV | UART CPU | DSP DAC | PWM ADC | SPI P2 | P3 | A15-0	88-BIT R-S ECC | SRAM/ DRAM CTRL DISK INTER-FACE | MCU INTER-FACE | AT/DE HOST INTER-FACE	MULT | DIV | UART CPU | OSC 464 RAM | CLOCK Search | Merge P2 | P3 | A15-A0	SERVO | MAILBOX MULT | DIV | UART CPU | DSP DAC | PWM ADC | SPI P2 | P3 | A15-A0
Part Number	**Z86C95**	**Z86018**	**Z86193**	**Z86295**
Description	ROMLess Enhanced Z8® with DSP	Zilog Datapath Controller	ROMLess Enhanced Z8® Multiply/Divide	ROMLess Enhanced Z8® DSP Servo Timer
Process/Speed	CMOS: 24, 33 MHz	CMOS: 40 MHz	CMOS: 40 MHz	CMOS: 40 MHz
Features	■ Eight Channel ■ 8-Bit ADC ■ 8-Bit DAC ■ 16-Bit Multiply/Divide ■ Full-Duplex UART ■ Serial Peripheral Interface (SPI) ■ Three Standby Modes (STOP/HALT/PAUSE) ■ Pulse Width Modulator (PWM) ■ 3x16-Bit Timer ■ 16-Bit DSP Slave Processor ■ 83 ns Multiply/Accumulate	■ Full-Track Read ■ Automatic Data Transfer (Point & Go®) ■ 88-Bit Reed Solomon ECC "On The Fly" ■ Full AT/IDE Bus Interface ■ 64 Kbytes SRAM Buffer ■ 1 Mbytes DRAM Buffer ■ Split Data Field Support ■ Joint Test Action Group (JTAG) Boundary Scan Option ■ 8 Kbytes Buffer RAM Reserved for MCU	■ 16x16 Multiply 17 Clocks ■ 32x16 Divide 38 Clocks ■ Full-Duplex UART ■ Two Standby Modes (STOP & HALT) ■ Three 16-Bit Counter/Timers ■ SEARCH Machine ■ MERGE Machine ■ Bus Request Mode ■ Evaluation Mode	■ Eight Channel ■ 8-Bit ADC ■ 8-Bit DAC ■ Serial Peripheral Interface (SPI) ■ Pulse Width Modulator (PWM) ■ Three 16-Bit Counter/Timer ■ Full-Duplex UART ■ 16-Bit Z8® Multiply/Divide ■ Full 16-Bit DSP ■ Programmable Servo Timer ■ Z8® - DSP Mail Box
Package	80-Pin QFP 84-Pin PLCC 100-Pin VQFP	100-Pin VQFP	64-Pin VQFP	100-Pin VQFP 144-Pin QFP
Support Products	Z86C9500ZCO - Evaluation Board Z86C9500ZUSP064 - Signum Emulator Z86C9501ZUSP064 - Signum Emulator Z86C9500ZPD - Signum Emulator POD Z86C9501ZPD - Signum Emulator POD Z86ZIA00ZCO - Evaluation Board	Z86C9900ZCO - Evaluation Board	Z8619200ZME - Emulator Z8619300ZCO - Evaluation Board	Z86ZIA01ZCO - Evaluation Board

Bus Interface — Superintegration™ Products Guide

Block Diagram

Z86016:



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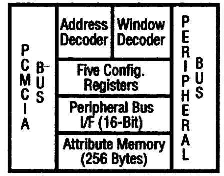

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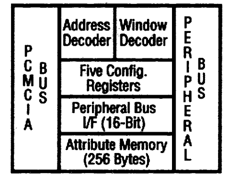

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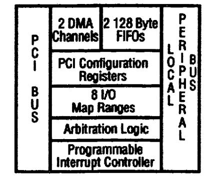

Part Number	**Z86016**	**Z86017**	**Z86M17**	**Z86020**
Description	8-Bit PCMCIA Interface Adaptor	PCMCIA Interface Adaptor	PCMCIA Interface Adaptor	PCI/Multifunction Bridge
Process/Speed	CMOS: 20 MHz	CMOS: 20 MHz	CMOS: 20 MHz	CMOS: 33 MHz
Features	■ Z86017 with 8-Bit Peripheral Bus Only	■ 256 Bytes of Attribute Memory ■ Five Configuration Registers ■ EEPROM Sequencer or SPI Interface ■ PCMCIA to I/O, Memory or Both ■ PCMCIA to ATA/IDE ■ ATA/IDE to ATA/IDE ■ 3.0V to 5.5V Operation ■ 8- or 16-Bit Peripheral Support	■ Mirror Image Pin-Out of Z86017 for Opposite PCB - Surface Layout	■ 256 Bytes of Configuration Memory ■ 64 PCI Configuration Registers ■ Eight Programmable Memory or I/O Map Ranges with Independent Timing Control ■ 128 Byte FIFO's ■ Two Full Featured DMA Channels ■ PCI Initiator/Target Operations ■ On-Chip Peripheral Bus Arbitration
Package	48-Pin VQFP 64-Pin VQFP	100-Pin VQFP	100-Pin VQFP	160-Pin QFP
Support Products	Z8601600ZCO - Evaluation Board (Available Q494)	Z8601700ZCO -Evaluation Board	Z8601700ZCO - Evaluation Board	Available Q494

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EBV Elektronik 0039-2-66017111
Firenze
EBV Elektronik 0039-55-350792
Roma
EBV Elektronik 0039-6-2253367
Modena
EBV Elektronik 0039-59-344752
Napoli
EBV Elektronik 0039-81-2395540
Torino
EBV Elektronik 0039-11-2161531
Vicenza
EBV Elektronik 0039-444-572366

NETHERLANDS
EBV Elektronik 313-46562353

NORWAY
Bexab Norge 47-63833800

POLAND
Warsaw
Gamma Ltd. 004822-330853

PORTUGAL
Amadora
Amitron-Arrow. 0035-1-4714806

RUSSIA
Woronesh
Thesys/Intertechna 0732593697
Vyborg
Gamma Ltd. 081278-31509
St. Petersburg
Gamma Ltd. 0812-5131402

SPAIN
Barcelona
Amitron-Arrow S.A. 0034-3-4907494
Madrid
Amitron-Arrow S.A. 0034-1-3043040

SWEDEN
Bexab Sweden AB 46-8-630-8800

SWITZERLAND
Dietikon
EBV Elektronik GMBH 0041-1-7401090
Lausanne
EBV Elektronik AG 0041-21-3112804
Regensdorf
Eurodis AG 0041-1-8433111

UKRAINE
Kiev
Thesys/Mikropribor 04434-9533

LITERATURE GUIDE

Z8® MICROCONTROLLERS - CONSUMER FAMILY OF PRODUCTS

Databooks By Market Niche	Part No	Unit Cost
Z8® Microcontrollers Databook	**DC-8305-02**	**$ 5.00**

Product Specifications

Z86C07 CMOS Z8 8-Bit Microcontroller
Z86C08 CMOS Z8 8-Bit Microcontroller
Z86E08 CMOS Z8 8-Bit OTP Microcontroller
Z86C11 CMOS Z8 Microcontroller
Z86C12 CMOS Z8 In-Circuit Microcontroller Emulator
Z86C21 8K ROM Z8 CMOS Microcontroller
Z86E21 CMOS Z8 8K OTP Microcontroller
Z86C61/62/96 CMOS Z8 Microcontroller
Z86C63/64 32K ROM Z8 CMOS Microcontroller
Z86C91 CMOS Z8 ROMless Microcontroller
Z86C93 CMOS Z8 Multiply/Divide Microcontroller

Support Product Specifications

Z0860000ZCO Development Kit
Z86C0800ZCO Applications Board
Z86C0800ZDP Adaptor Board
Z86E2100ZDF Adaptor Kit
Z86E2100ZDP Adaptor Kit
Z86E2100ZDV Adaptor Kit
Z86E2100ZDV Adaptor Kit
Z86E2101ZDF Conversion Kit
Z86E2101ZDV Conversion Kit
Z86C6100TSC Z86C61/63 MCU OTP Emulation Board
Z86C6200ZEM In-Circuit Emulator
Z86C1200ZEM Z8® In-Circuit Emulator -C12
Z8® S Series Emulators, Base Units and Pods

Additional Information

Zilog's Superintegration™ Products Guide
Literature Guide
Third Party Support Vendors
Zilog's Sales Offices, Representatives and Distributors

Infrared Remote (IR) Controllers Databook	**DC-8301-04**	**$ 5.00**

Product Specifications

Z86L06 Low Voltage CMOS Consumer Controller Processor (Preliminary)
Z86L29 6K Infrared (IR) Remote (ZIRC™) Controller (Advance Information)
Z86L70/L71/L72/L75/L76 Zilog IR (ZIRC™) CCP™ Controller Family (Preliminary)
Z86E72/E73/E74 Zilog IR (ZIRC™) CCP™ Controller Family (Preliminary)

Application Note

Beyond the 3 Volt Limit

Support Product Specifications

Z86L7100ZDB Emulator Board
Z86L7100ZEM ICEBOX™ In-Circuit Emulator Board

Additional Information

Zilog's Superintegration™ Products Guide
Literature Ordering Guide
Zilog's Sales Offices, Representatives and Distributors

Z8® MICROCONTROLLERS - CONSUMER FAMILY OF PRODUCTS

Databooks By Market Niche	Part No	Unit Cost
Discrete Z8® Microcontrollers	DC 8318-02	$ 5.00

Product Specifications

Z86C03/C06 CMOS Z8® 8-Bit Consumer Controller Processors
Z86E03/E06 CMOS Z8® 8-Bit OTP Consumer Controller Processors
Z86C04/C08 CMOS Z8® 8-Bit Low Cost 1K/2K ROM Microcontrollers
Z86E04/E08 CMOS Z8® 8-Bit OTP Microcontrollers
Z86C07 CMOS Z8® 8-Bit Microcontroller
Z86E07 CMOS Z8® 8-Bit OTP Microcontroller
Z86C30/C31 CMOS Z8® 8-Bit Consumer Controller Processors
Z86E30/E31 CMOS Z8® 8-Bit OTP Consumer Controller Processors
Z86C40 CMOS Z8® 4K ROM Consumer Controller Processor
Z86E40 CMOS Z8® 8-Bit OTP Consumer Controller Processor

Z8® Microcontrollers Application Notes

Timekeeping with the Z8®
Using The Zilog Z86C06 SPI Bus
DTMF Tone Generation Using the Z8® CCP™
Serial Communications Using the Z8® CCP™ Software UART
The Versatile Z86C08: Three Key Features of this Z8® MCU
The Z86C08 Controls a Scrolling LED Message Display
Interfacing LCDs to the Z8® Microcontroller

Support Product Specifications and Third Party Vendors

Z86C0800ZCO Evaluation Board
Z86C0800ZDP Adaptor Kit
Z86C1200ZEM Emulator
Z86E0600ZDP Adaptor Kit
Z86E0700ZDP Adaptor Kit
Z86E3000ZDP Adaptor Kit
Z86E4000ZDF Adaptor Kit
Z86E4000ZDP Adaptor Kit
Z86E4000ZDV Adaptor Kit
Z86E4001ZDF Adaptor Kit
Z86E4001ZDV Adaptor Kit
Z86CCP00ZEM Emualtor
Z86CCP00ZAC Emulator Kit
Z8® S Series Emulators, Base Units and Pods

Additional Information

Zilog's Superintegration™ Products Guide
Literature Guide and Ordering Information
Zilog's Sales Offices, Representatives and Distributors

Z8® MICROCONTROLLERS - CONSUMER FAMILY OF PRODUCTS

Databooks By Market Niche	Part No	Unit Cost
Digital Television Controllers	DC-8308-01	$ 5.00

Product Specifications

Z89300 Series Digital Television Controller
Z86C27/97 CMOS Z8® Digital Signal Processor
Z86C47/E47 CMOS Z8® Digital Signal Processor
Z86127 Low Cost Digital Television Controller
Z86128/228 Line 21 Closed-Caption Controller (L21C™)
Z86227 40-Pin Low Cost (4LDTC™) Digital Television Controller

Support Product Specifications

Z86C2700ZCO Application Kit
Z86C2700ZDB Emulation Board
Z86C2702ZEM In-Circuit Emulator

Additional Information

Zilog's Superintegration™ Products Guide
Literature Guide and Ordering Information
Zilog's Sales Offices, Representatives and Distributors

Telephone Answering Device Databook	DC-8300-02	$ 5.00

Product Specifications

Z89C65, Z89C66 (ROMless) Dual Processor T.A.M. Controller (Preliminary)
Z89C67, Z89C68/C69 (ROMless) Dual Processor Tapeless T.A.M. Controller (Preliminary)

Development Guides

Z89C65 Software Development Guide
Z89C67/C69 Software Development Guide

Technical Notes

Using Samsung KT8554 Codec on the ZTAD Development Board
Z89C67/C69 Design Guidelines
Z89C67/C69 ARAM Bit-Rate Measurements
Z89C67 Codec Interfacing (Preliminary)
Controlling the Out –5V and Codec Clock Signals for Low-Power Halt Mode

Support Product Specifications

Z89C5900ZEM Emulation Module
Z89C6500ZDB Emulation Board
Z89C6501ZEM ICEBOX™ In-Circuit Emulator
Z89C6700ZDB Emulator Board
Z89C6700ZEM ICEBOX™ Emulator Board

Additional Information

Zilog's Superintegration™ Products Guide
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Z8® MICROCONTROLLERS - PERIPHERALS MULTIMEDIA FAMILY OF PRODUCTS

Databooks By Market Niche	Part No	Unit Cost
Digital Signal Processor Databook	**DC-8299-04**	**$ 5.00**

Product Specifications

Z89321/371 16-Bit Digital Signal Processor (Preliminary)
Z89C00 16-Bit Digital Signal Processor (Preliminary)
Z89320 16-Bit Digital Signal Processor (Preliminary)
Z86C95 Z8® Digital Signal Processor (Preliminary)
Z89120, Z89920 (ROMless) 16-Bit Mixed Signal Processor (Preliminary)
Z89121, Z89921 (ROMless) 16-Bit Mixed Signal Processor (Preliminary)

Application Note

Using the Z89371/321 CODEC Interface
Z89371 Inter Processor Communication
Understanding Q15 Two's Complement Fractional Multiplication (Z89C00 DSP)

Support Product Specifications

Z8937100ZEM In-Circuit Emulator -C00
Z8937100TSC Emulation Module
Z89C0000ZAS Z89C00 Assembler, Linker and Librarian
Z89C0000ZCC Z89C00 C Cross Compiler
Z89C0000ZEM In-Circuit Emulator -C00
Z89C0000ZHP Logic Analyzer Adaptor Board
Z89C0000ZSD Z89C00 Simulator/Debugger
Z89C0000ZTR Z89C00 Translator

Additional Information

Zilog's Superintegration™ Products Guide
Literature Guide and Third Party Support
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Databooks By Market Niche	Part No	Unit Cost
Keyboard/Mouse/Pointing Devices Databook	DC-8304-01	$ 5.00

Product Specifications
- Z8602/14 NMOS Z8® 8-Bit Keyboard Controller
- Z8615 NMOS Z8® 8-Bit Keyboard Controller
- Z86C15 CMOS Z8® 8-Bit MCU Keyboard Controller
- Z86E23 Z8® 8-Bit Keyboard Controller with 8K OTP
- Z86C04/C08 CMOS Z8® 8-Bit Microcontroller
- Z86E08 CMOS Z8® 8-Bit Microcontroller
- Z88C17 CMOS Z8® 8-Bit Microcontroller
- Z86C117/717 Z8® 8-Bit Microcontroller
- Z86217 Z8® 8-Bit Microcontroller

Application Notes
- Z8602 Keyboard
- Z86C17 In-Mouse Applications

Support Product Specifications and Third Party Support
- Z0860200ZCO Evaluation Board
- Z0860200ZDP Adaptor Kit
- Z86C0800ZCO Evaluation Board
- Z86C0800ZDP Adaptor Kit
- Z86C1200ZEM Emulator
- Z86E2300ZDP Adaptor Kit
- Z86E2301ZDP Adaptor Kit
- Z86E2300ZDV Adaptor Kit
- Z86E2301ZDV Adaptor Kit

Additional Information
- Zilog's Superintegration™ Products Guide
- Literature Guide and Ordering Information
- Zilog's Sales Offices, Representatives and Distributors

PC Audio Databook	DC-8317-00	$ 5.00

Product Specifications
- Z86321 Digital Audio Processor (Preliminary)
- Z89320 16-Bit Digital Signal Processor (Preliminary)
- Z89321/371 16-Bit Digital Signal Processor (Preliminary)
- Z89331 16-Bit PC ISA Bus Interface (Advance Information)
- Z89341/42/43 Wave Synthesis Chip Set (Advance Information)
- Z5380 Small Computer System Interface

Additional Information
- Zilog's Superintegration™ Products Guide
- Literature Guide

Z8® MICROCONTROLLERS - PERIPHERALS MEMORY FAMILY OF PRODUCTS

Databooks By Market Niche	Part No	Unit Cost
Mass Storage Solutions	DC-8303-01	$ 5.00

Product Specifications

Z86C21 8K ROM Z8 CMOS Microcontroller
Z86E21 CMOS Z8 8K OTP Microcontroller
Z86C91 CMOS Z8 ROMless Microcontroller
Z86C93 CMOS Z8 Multiply/Divide Microcontroller
Z86C95 Z8 Digital Signal Processor
Z86018 Data Path Controller
Z89C00 16-Bit Digital Signal Processor

Application Note

Understanding Q15 Two's Complement Fractional Multiplication (Z89C00 DSP)

Support Product Specifications

Z8060000ZCO Development Kit
Z86C1200ZEM In-Circuit Emulator
Z86E2100ZDF Adaptor Kit
Z86E2100ZDP Adaptor Kit
Z86E2100ZDV Adaptor Kit
Z86E2101ZDF Conversion Kit
Z86E2101ZDV Conversion Kit
Z86C9300ZEM ICEBOX™ Emulator
Z86C9500ZCO Evaluation Board
Z8® S Series Emulators, Base Units and Pods
Z89C0000ZAS Z89C00 Assembler, Linker and Librarian
Z89C0000ZCC Z89C00 C Cross Compiler
Z89C0000ZEM In-Circuit Emulator -C00
Z89C0000ZSD Z89C00 Simulator/Debugger
ZPCMCIA0ZDP PCMCIA Extender Card

Additional Information

Zilog's Superintegration™ Products Guide
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Z8® MICROCONTROLLERS LITERATURE (Continued)

Technical Manuals and Users Guides	Part No.	Unit Cost
Z8® Microcontrollers Technical Manual	DC-8291-02	5.00
Z86018 Preliminary User's Manual	DC-8296-00	N/C
Digital TV Controller User's Manual	DC-8284-01	5.00
Z89C00 16-Bit Digital Signal Processor User's Manual/DSP Software Manual	DC-8294-02	5.00
Z86C95 16-Bit Digital Signal Processor User Manual	DC-8595-00	5.00
Z86017 PCMCIA Adaptor Chip User's Manual and Databook	DC-8298-03	5.00
PLC Z89C00 Cross Development Tools Brochure	DC-5538-01	N/C

Z8® Application Notes	Part No	Unit Cost
The Z8 MCU Dual Analog Comparator	DC-2516-01	N/C
Z8 Applications for I/O Port Expansions	DC-2539-01	N/C
Z86E21 Z8 Low Cost Thermal Printer	DC-2541-01	N/C
Zilog Family On-Chip Oscillator Design	DC-2496-01	N/C
Using the Zilog Z86C06 SPI Bus	DC-2584-01	N/C
Interfacing LCDs to the Z8	DC-2592-01	N/C
X-10 Compatible Infrared (IR) Remote Control	DC-2591-01	N/C
Z86C17 In-Mouse Applications	DC-3001-01	N/C
Z86C40/E40 MCU Applications Evaluation Board	DC-2604-01	N/C
Z86C08/C17 Controls A Scrolling LED Message Display	DC-2605-01	N/C
Z86C95 Hard Disk Controller Flash EPROM Interface	DC-2639-01	N/C
Three Z8® Applications Notes: Timekeeping with Z8; DTMF Tone Generation; Serial Communication Using the CCP Software UART	DC-2645-01	N/C

Z80®/Z8000® DATACOMMUNICATIONS FAMILY OF PRODUCTS

Databooks By Market Niche	Part No	Unit Cost
High-Speed Serial Communication Controllers	DC-8314-00	5.00
Product Specifications		
Z16C30 CMOS Universal Serial Controller (USC™) (Preliminary)		
Z16C32 Integrated Universal Serial Controller (IUSC™) (Preliminary)		
Application Notes		
Using the Z16C30 Universal Serial Controller with MIL-STD-1553B		
Design a Serial Board to Handle Multiple Protocols		
Datacommunications IUSC™/MUSC™ Time Slot Assigner		
Support Products		
Z16C3001ZCO Evaluation Board Product Specification		
Z8018600ZCO Evaluation Board Product Specification		
Additional Information		
Zilog's Superintegration™ Products Guide		
Literature Guide		
Third Party Support Vendors		
Serial Communication Controllers	DC-8316-00	5.00
Product Specifications		
Z8030/Z8530 Z-Bus® SCC Serial Communication Controller		
Z80C30/Z85C30 CMOS Z-Bus® SCC Serial Communication Controller		
Z80230 Z-Bus® ESCC™ Enhanced Serial Communication Controller (Preliminary)		
Z85230 ESCC™ Enhanced Serial Communication Controller		
Z85233 EMSCC™ Enhanced Mono Serial Communication Controller		
Z85C80 SCSCI™ Serial Communications and Small Computer Interface		
Z16C35/Z85C35 CMOS ISCC™ Integrated Serial Communications Controller		
Application Notes		
Interfacing Z8500 Peripherals to the 68000		
SCC in Binary Synchronous Communications		
Zilog SCC Z8030/Z8530 Questions and Answers		
Integrating Serial Data and SCSI Peripheral Control on One Chip		
Zilog ISCC™ Controller Questions and Answers		
Boost Your System Performance Using the Zilog ESCC™		
Zilog ESCC™ Controller Questions and Answers		
The Zilog Datacom Family with the 80186 CPU		
On-Chip Oscillator Design		
Support Products		
Z8S18000ZCO Evaluation Board Product Specification		
Z8523000ZCO Evaluation Board Product Specification		
Z8018600ZCO Evaluation Board Product Specification		
ZEPMDC00002 Electronic Programmer's Manual Software		
Additional Information		
Zilog's Superintegration™ Products Guide		
Literature Guide		

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Z80®/Z8000® DATACOMMUNICATIONS FAMILY OF PRODUCTS

Databooks	Part No	Unit Cost
Z80 Family Databook	**DC-8321-00**	**5.00**

Discrete Z80® Family
- Z8400/C00 NMOS/CMOS Z80® CPU Product Specification
- Z8410/C10 NMOS/CMOS Z80 DMA Product Specification
- Z8420/C20 NMOS/CMOS Z80 PIO Product Specification
- Z8430/C30 NMOS/CMOS Z80 CTC Product Specification
- Z8440/C40 NMOS/CMOS Z80 SIO Product Specification

Embedded Controllers
- Z84C01 Z80 CPU with CGC Product Specification
- Z8470 Z80 DART Product Specification
- Z84C90 CMOS Z80 KIO™ Product Specification
- Z84013/015 Z84C13/C15 IPC/EIPC Product Specification

Application Notes and Technical Articles
- Z80® Family Interrupt Structure
- Using the Z80® SIO with SDLC
- Using the Z80® SIO in Asynchronous Communications
- Binary Synchronous Communication Using the Z80® SIO
- Serial Communication with the Z80A DART
- Interfacing Z80® CPUs to the Z8500 Peripheral Family
- Timing in an Interrupt-Based System with the Z80® CTC
- A Z80-Based System Using the DMA with the SIO
- Using the Z84C11/C13/C15 in Place of the Z84011/013/015
- On-Chip Oscillator Design
- A Fast Z80® Embedded Controller
- Z80® Questions and Answers

Additional Information
- Zilog's Superintegration™ Products Guide
- Literature Guide
- Third Party Support Vendors
- Zilog's Sales Offices, Representatives and Distributors

Z80®/Z8000® DATACOMMUNICATIONS FAMILY OF PRODUCTS

Databooks	Part No	Unit Cost
Z180™ Microprocessors and Peripherals Databook	**DC-8322-00**	**5.00**

Product Specifications
- Z80180/Z8S180/Z8L180 Z180™ Microprocessor
- Z80181 Z181™ Smart Access Controller (SAC™)
- Z80182/Z8L182 Zilog Intelligent Peripheral Controller (ZIP™)

Application Notes and Technical Articles
- Z180™ Questions and Answers
- Z180™/SCC Serial Communication Controller Interface at 10 MHz
- Interfacing Memory and I/O to the 20 MHz Z8S180 System
- Break Detection on the Z80180 and Z181™
- Z182 Programming the MIMIC Autoecho ECHOZ182 Sample Code
- Local Talk Link Access Protocol Using the Z80181

Support Products
- Z8S18000ZCO Evaluation Board
- Z8018100ZCO Evaluation Board
- Z8018101ZCO Evaluation Board
- Z8018101ZA6 Driver Software
- Z8018100ZDP Adaptor Board
- Z8018200ZCO Evaluation Board
- Z80® and Z80180 Hardware and Software Support
- Third Party Support Vendors

Additional Information
- Zilog's Superintegration™ Products Guide
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Z80®/Z8000® DATACOMMUNICATIONS FAMILY OF PRODUCTS

Databooks and User's Manuals	Part No	Unit Cost
Z8000 Family of Products	**DC-8319-00**	**5.00**
Z8000 Family Databook		
Zilog's Z8000 Family Architecture		
Z8001/Z8002 Z8000 CPU Product Specification		
Z8016 Z8000 Z-DTC Product Specification		
Z8036 Z8000 Z-CIO Product Specification		
Z8536 CIO Counter/Timer and Parallel I/O Unit Product Specification		
Z8038/Z8538 FIO FIFO Input/Output Interface Unit Product Specification		
Z8060/Z8560 FIFO Buffer Unit		
Z8581 Clock Generator and Controller Product Specification		
User's Manuals		
Z8000 CPU Central Processing Unit User's Manual		
Z8010 Memory Management Unit (MMU) User's Manual		
Z8036 Z-CIO/Z8536 CIO Counter/Timer and Parallel Input/Output User's Manual		
Z8038 Z8000 Z-FIO FIFO Input/Output Interface User's Manual		
Z8000 Application Notes and Military Products		
Application Notes		
Using SCC with Z8000 in SDLC Protocol		
SCC in Binary Synchronous Communication		
Zilog's Military Products Overview		
Additional Information		
Zilog's Superintegration™ Products Guide		
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Zilog's Sales Offices, Representatives and Distributors		
Z80 Family Technical Manual	DC-8309-00	5.00
Z80180 Z180 MPU Microprocessor Unit Technical Manual	DC-8276-04	5.00
Z280 MPU Microprocessor Unit Technical Manual	DC-8224-03	5.00
Z380™ Preliminary Product Specification	DC-6003-03	N/C
Z380™ User's Manual	DC-8297-03	5.00
Z2000 Spread-Spectrum Transceiver Advance Information Product Specification	DC-6021-00	N/C
ZNW2000 User's Manual for PC WAN Adaptor Board Development Kit	DC-8315-00	N/C
SCC Serial Communication Controller User's Manual	DC-8293-02	5.00
High-Speed SCC, Z16C30 USC User's Manual	DC-8280-04	5.00
High-Speed SCC, Z16C32 IUSC User's Manual	DC-8292-02	5.00
Z16C35 ISCC Integrated Serial Communication Controller Technical Manual	DC-8286-01	5.00
Z16C35 ISCC Integrated Serial Communication Controller Addendum	DC-8286-01A	N/C

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MILITARY COMPONENTS FAMILY

Military Product Specifications	Part No	Unit Cost
Z8681 ROMless Microcomputer	DC-2392-02	N/C
Z8001/8002 Military Z8000 CPU Central Processing Unit	DC-2342-03	N/C
Z8581 Military CGC Clock Generator and Controller	DC-2346-01	N/C
Z8030 Military Z8000 Z-SCC Serial Communications Controller	DC-2388-02	N/C
Z8530 Military SCC Serial Communications Controller	DC-2397-02	N/C
Z8036 Military Z8000 Z-CIO Counter/Timer Controller and Parallel I/O	DC-2389-01	N/C
Z8038/8538 Military FIO FIFO Input/Output Interface Unit	DC-2463-02	N/C
Z8536 Military CIO Counter/Timer Controller and Parallel I/O	DC-2396-01	N/C
Z8400 Military Z80 CPU Central Processing Unit	DC-2351-02	N/C
Z8420 Military PIO Parallel Input/Output Controller	DC-2384-02	N/C
Z8430 Military CTC Counter/Timer Circuit	DC-2385-01	N/C
Z8440/1/2/4 Z80 SIO Serial Input/Output Controller	DC-2386-02	N/C
Z80C30/85C30 Military CMOS SCC Serial Communications Controller	DC-2478-02	N/C
Z84C00 CMOS Z80 CPU Central Processing Unit	DC-2441-02	N/C
Z84C20 CMOS Z80 PIO Parallel Input/Output	DC-2384-02	N/C
Z84C30 CMOS Z80 CTC Counter/Timer Circuit	DC-2481-01	N/C
Z84C40/1/2/4 CMOS Z80 SIO Serial Input/Output	DC-2482-01	N/C
Z16C30 CMOS USC Universal Serial Controller (Preliminary)	DC-2531-01	N/C
Z80180 Z180 MPU Microprocessor Unit	DC-2538-01	N/C
Z84C90 CMOS KIO Serial/Parallel/Counter Timer (Preliminary)	DC-2502-00	N/C
Z85230 ESCC Enhanced Serial Communication Controller	DC-2595-00	N/C

LITERATURE GUIDE

GENERAL LITERATURE

Catalogs, Handbooks, Product Flyers and Users Guides	Part No	Unit Cost
Superintegration Master Selection Guide 1994-1995	DC-5634-00	N/C
Superintegration Products Guide	DC-5676-00	N/C
Quality and Reliability Report	DC-8329-00	N/C
ZIA™ 3.3-5.5V Matched Chip Set for AT Hard Disk Drives Datasheet	DC-5556-01	N/C
ZIA ZIA00ZCO Disk Drive Development Kit Datasheet	DC-5593-01	N/C
Zilog Hard Disk Controllers - Z86C93/C95 Datasheet	DC-5560-01	N/C
Zilog Infrared (IR) Controllers - ZIRC™ Datasheet	DC-5558-01	N/C
Zilog V. Fast Modem Controller Solutions	DC-5525-02	N/C
Zilog Digital Signal Processing - Z89320 Datasheet	DC-5547-01	N/C
Zilog Keyboard Controllers Datasheet	DC-5600-01	N/C
Z380™ - Next Generation Z80®/Z180™ Datasheet	DC-5580-02	N/C
Fault Tolerant Z8® Microcontroller Datasheet	DC-5603-01	N/C
32K ROM Z8® Microcontrollers Datasheet	DC-5601-01	N/C
Zilog Datacommunications Brochure	DC-5519-00	N/C
Z89300 DTC Controller Family Brochure	DC-5608-01	N/C
Zilog Digital Signal Processing Brochure	DC-5536-02	N/C
Zilog ASSPs - Partnering With You Product Brochure	DC-5553-01	N/C
Zilog Wireless Products Datasheet	DC-5630-00	N/C
Zilog Z8604 Cost Efficient Datasheet	DC-5662-00	N/C
Zilog Chip Carrier Device Packaging Datasheet	DC-5672-00	N/C
Zilog Database of IR Codes Datasheet	DC-5631-00	N/C
Zilog PCMCIA Adaptor Chip Z86017 Datasheet	DC-5585-01	N/C
Zilog Television/Video Controllers Datasheet	DC-5567-01	N/C
Zilog TAD Controllers - Z89C65/C67/C69 Datasheet	DC-5561-02	N/C
Zilog Z87000 Z-Phone Datasheet	DC-5632-00	D/C
Zilog 1993 Annual Report	DC-1993-AR	N/C
Zilog 1994 First Quarter Financial Report	DC-1994-Q1	N/C

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- ❑ General-Purpose
- ❑ Mass Storage
- ❑ Low Voltage Controllers
- ❑ Wireless Communications
- ❑ Multimedia
- ❑ Fax/Modem Control
- ❑ Datacommunications
- ❑ Speech Processing/Synthesis

he primary product/industry in which my company is involved is: ______________________________.

y specific application is: ______________________________.

y need is: ❑ Immediate ❑ Within 6-12 months ❑ Long-term ❑ For information only

Name ______________________ **Title** ______________________
Company ______________________________
Address ______________________________
City ______________________ **ST** _____ **ZIP** __________
Telephone (____)________________, **Ext.** __________
Fax (____)________________

lease tell us where you heard about Zilog:

- ❑ Colleague's recommendation
- ❑ Direct sales call
- ❑ Advertisement (where?______________________)
- ❑ Prior experience with company
- ❑ Distributor or rep
- ❑ Conference Presentation (where?______________)

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