THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

COMPUTER DESIGN

JUNE 1967

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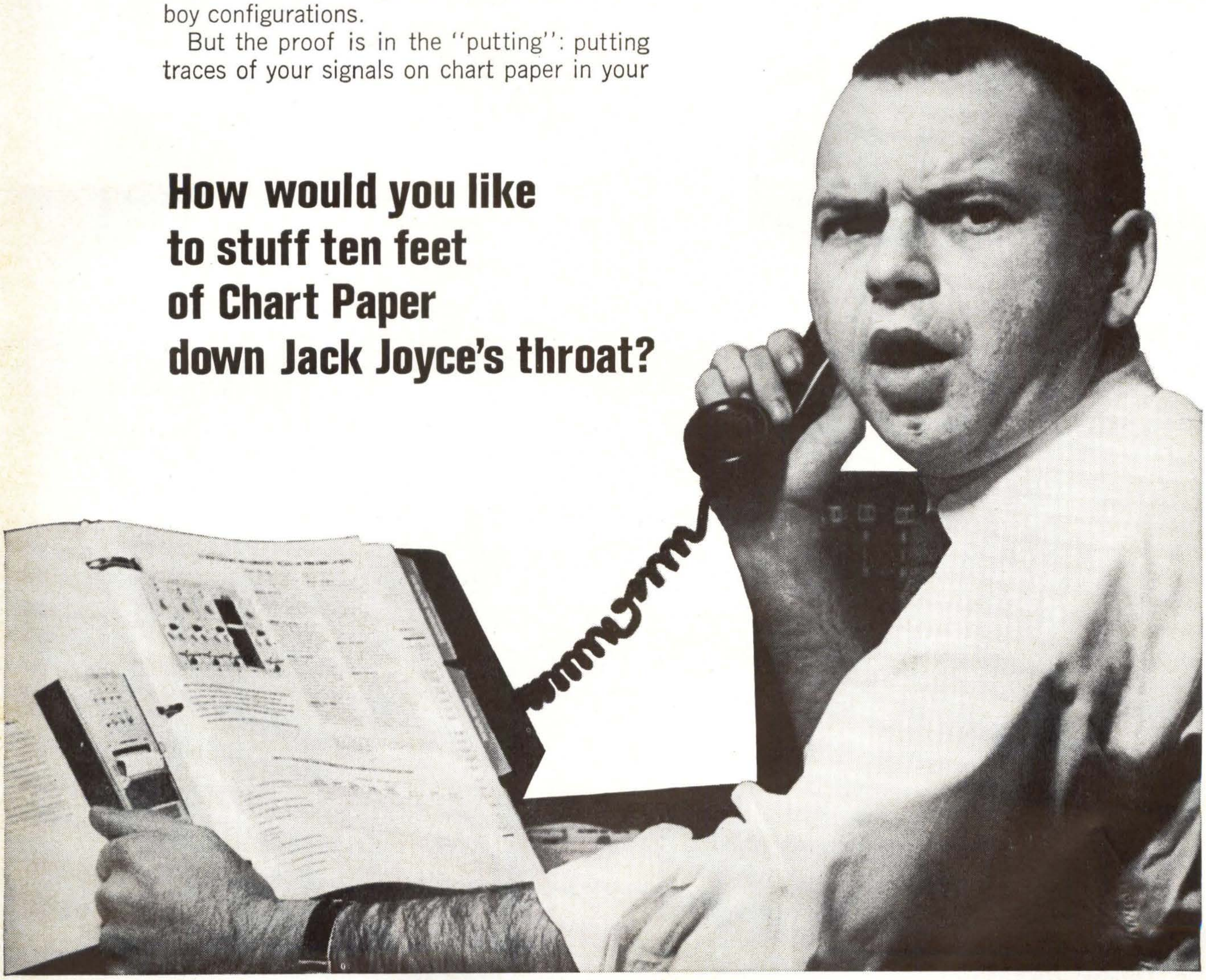

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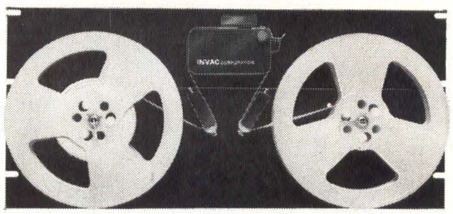

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Write for the Model R-360 Technical Bulletin

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JUNE 1967 • VOLUME 6 • NUMBER 6

COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

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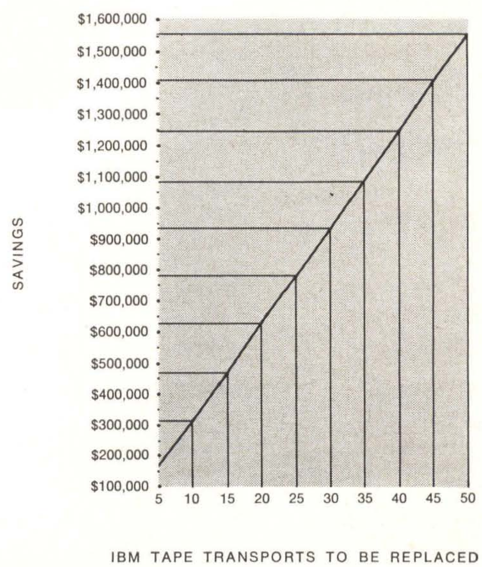
FEATURES

DEPARTMENTS

A COMPUTER IS ONLY AS RELIABLE AS ITS WEAKEST LINK



A six per cent increase in tape transport-to-computer availability ratio can mean the difference between completing a computer's assigned workload or running a second shift. Couple this increased availability with improved data reliability, and you have an excellent case for the replacement of those IBM 729 leased transports with their "identical twins", the Midwestern Instruments 4700 series.

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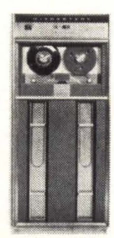
4700



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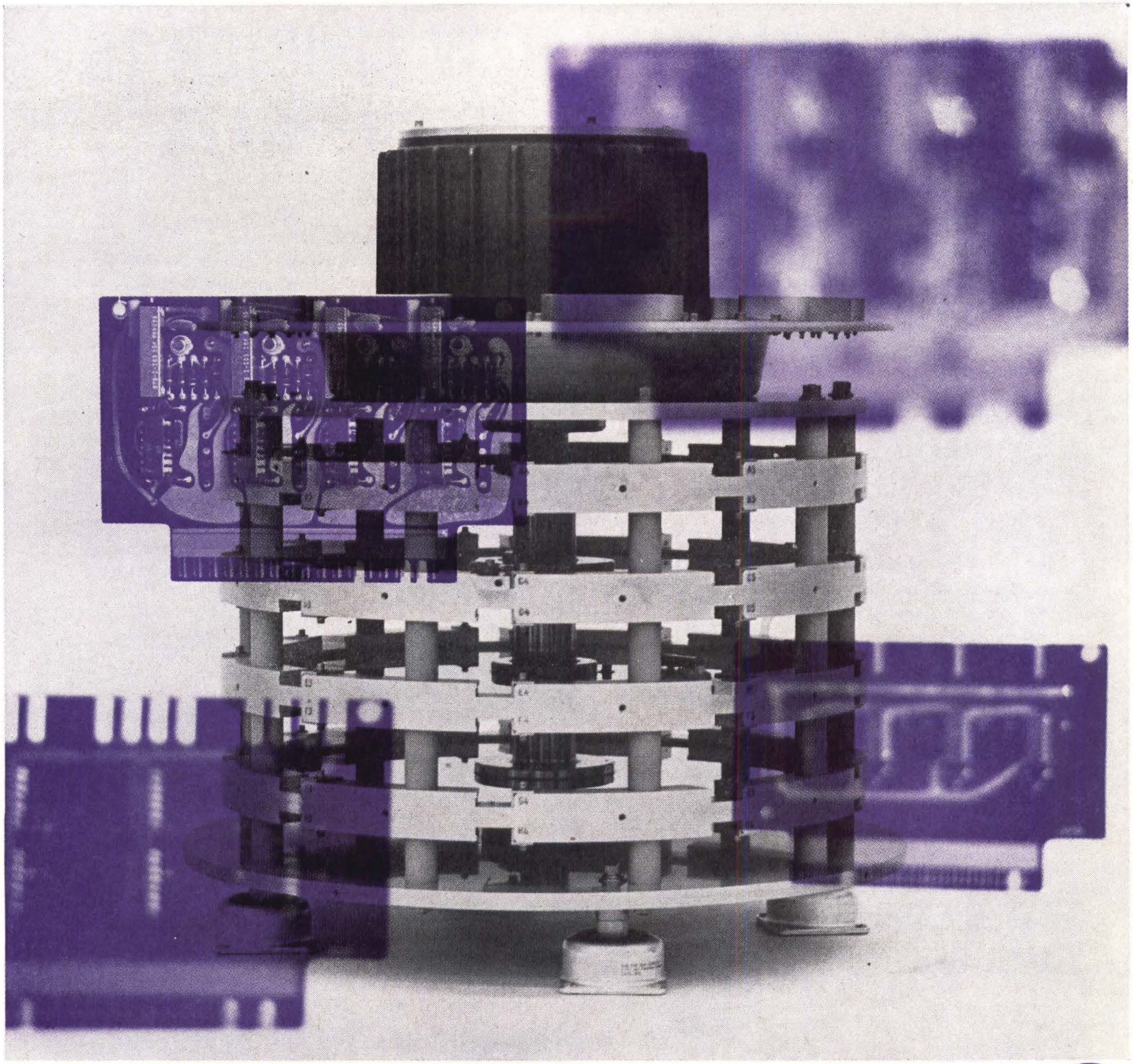

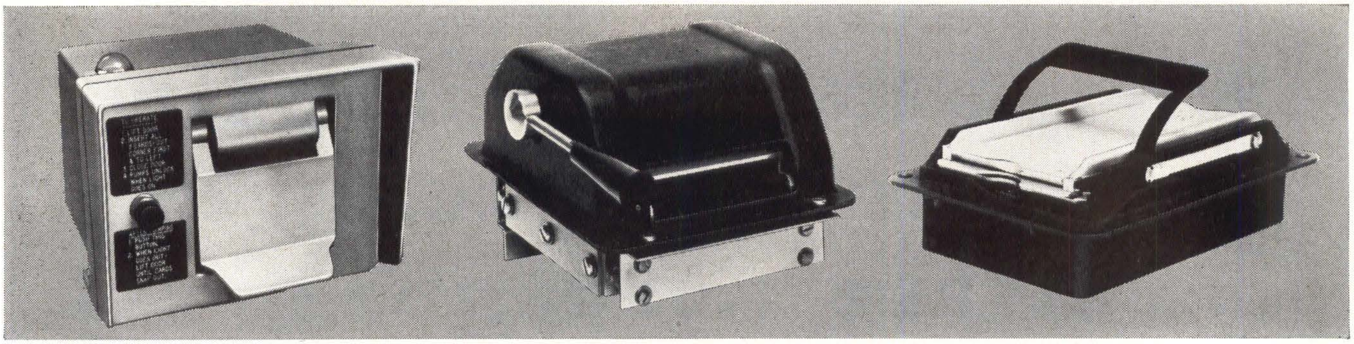

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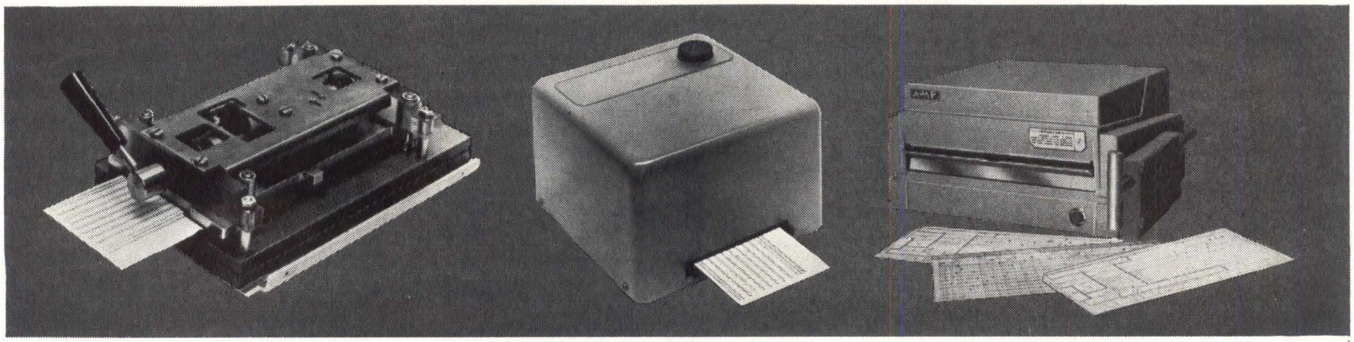

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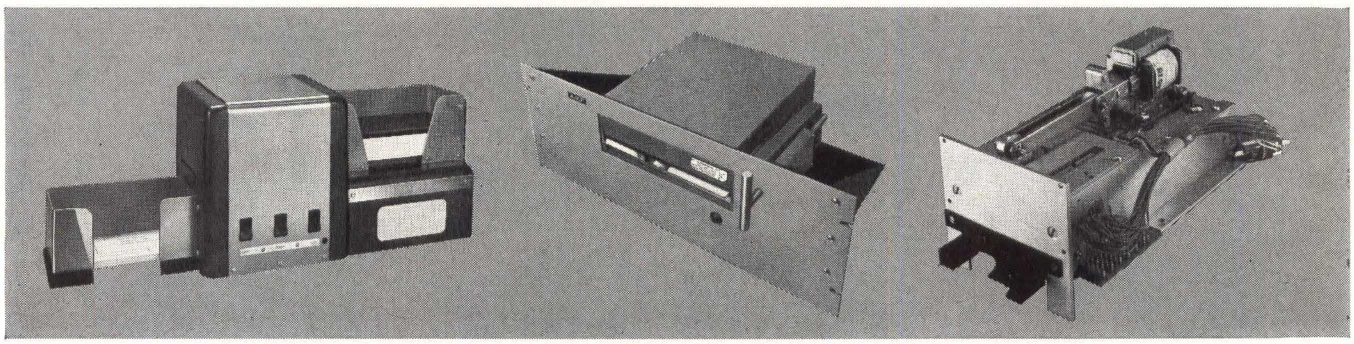

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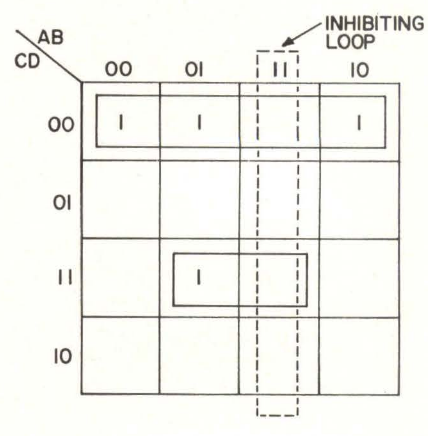
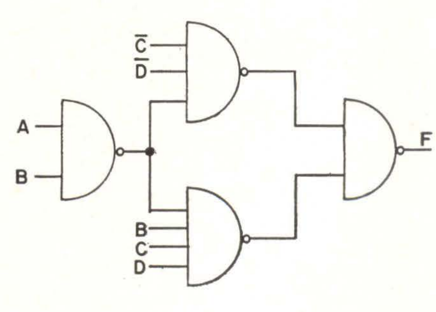
Letters to Editor

LOGIC MINIMIZATION

To the Editor:

Concerning Mr. Levine's article in the March issue of Computer Design, I feel obligated to point out that in spite of a multitude of "methods," minimization is still at least as much an art as a science. The NAND circuit realization below has the same





number of inputs, the same number of logic levels, and one less gate than Mr. Levine's "minimum."

Very truly yours,

Robert B. Lackey,
Assoc. Prof. E.E.,
Ohio State University,
Columbus, Ohio 43210

commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

THE CASE AGAINST STATISTICAL LOGIC DESIGN TECHNIQUES

David S. St. Lawrence

The usual rallying cry for the proponents of statistical logic design techniques goes something like this: "statistical design techniques permit a more realistic evaluation of system operation than do worst-case design techniques." This is usually accompanied by a dissertation on the desirability of avoiding worst-case design methods in calculating signal delays through a logic network because of the extremely low probability that all of the elements in a logic chain would exhibit worst-case delays. The argument then skips nimbly over the abyss of component specification, barely mentions relative design effort, and concentrates on the appeal of applying a formalized statistical method to logic design.

The statistical design technique treats the delay through an n stage logic chain as the sum of n random variables. The probability distribution of the sum of n random variables becomes more peaked as n increases, indicating clearly the decreasing probability of this sum approaching the sum of the worst-case delays. In addition, the probability distribution of the sum of n random varibles will be normal for larger values of n regardless of the individual probability distributions, thereby simplifying the task of computation.

However, let us examine what is involved in the application of statistical techniques to the design of a digital system logic network. The logic network under consideration might be a data transfer path for a 30-bit word and consist of at least 30 independent logic chains of nine gates in length. A consistent performance specification would require that all 30 outputs of this logic network be stable within some interval, following a change to the input of the logic network.

Even if not explicitly stated, the confidence level of such a minor network specification must be 99.5% or better if the total system is to be mass-produced economically and reliably. This requirement springs from the fact that it becomes prohibitively expensive if more than a small percentage of completed systems suffer from what is essentially a basic design defect. Considering that the total system might have ten or more such logic networks contributing to the system confidence level, it is not at all unreasonable that each network specification be required to have a 0.995 probability of successful operation. For the example under consideration, there are thirty independent logic chains of nine gates each, and the individual logic chain delay must be computed for a 0.9998 probability of satisfactory operation ($0.9998^{30} = 0.995$). Even with this requirement, the logic delay so computed can be 30% less than the worst-case delay through nine gates. Thus, the statistical approach to logic design can show a possibility of significant improvement in the system performance, and it requires only the specification of the logic element delay distributions.

The case against the application of statistical techniques to logic design is based almost entirely upon economic considerations. Logic element performance can indeed be specified adequately for statistical design purposes and sampling procedures can be set up to insure the continuing delivery of satisfactory devices. Design techniques can be elaborated to make use of this increased information but all of this acts to increase the cost of the basic logic element. Since a statistical design technique merely reduces the number of logic elements required for a given level of performance, the increased cost of suitably specified devices acts to negate any advantage for the statistical design approach. The vendor, planning for a long production run with

The author of this month's CD Commentary, David S. St. Lawrence, is a senior design engineer at Honeywell's Computer Control Division. He is responsible for central processor logic design and development.

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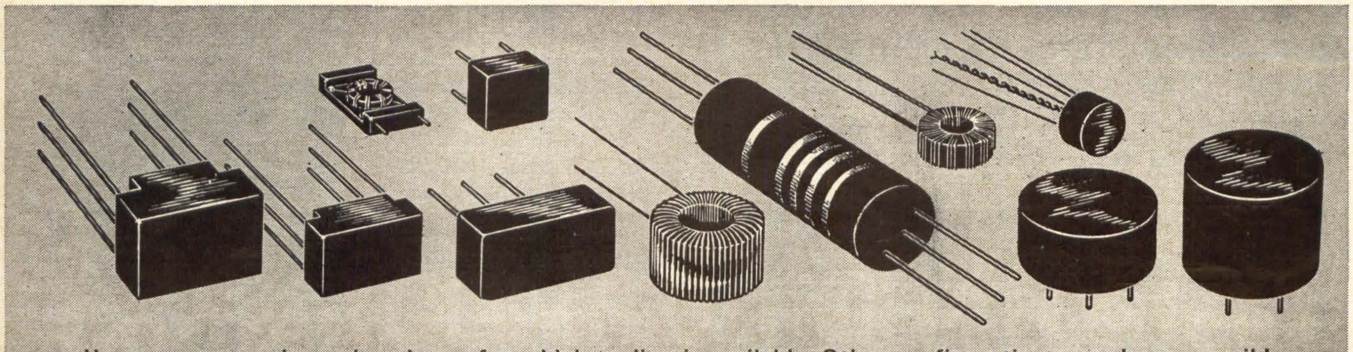

Here are commonly used packages for which tooling is available. Other configurations are always possible.

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normal process evolution, will charge more because of his reduced yield. The inspection of purchased material will be more elaborate and expensive than the far simpler one-sided tests used for checking conformance to existing specifications. Management will have a difficult time accepting the element cost-differential due to the increased specifications.

There is little possibility of circumventing this specification problem by in-house testing of devices purchased to a general specification because those attributes of the device that are being relied upon are not under control. For example, a shift in the mean delay can occur without a significant change in the reject rate if the manufacturer has negotiated sufficiently wide guard bands in the purchase specification.

Thus, the designer contemplating statistical design techniques must balance the desirability of using fewer elements for equivalent system performance against the increased cost of adequately specified devices. The alternate choice of using worst-case design techniques with the identical devices that are less expensive because of reduced specification requirements may be a more attractive solution. ■

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SOVIET COMPUTER TECHNOLOGY

Articles of Soviet developments in computer technology have been compiled and abstracted by the Aerospace Technology Division of the Library of Congress. The seventh in a continuing series, the compilation includes 69 abstracts in the categories of components, design, applications, and associated systems. Specific items describe a semiconductor-controlled memory unit with increased speed of operation, tape cores, a magnetic parametron-type null circuit, scanning device utilizing a fiber-optical converter, and various devices and converters. A bibliography is included. . . . ORDER AD-643 854 — COMPUTER TECHNOLOGY, price $3.00 (microfiche 65 cents). . . . B. Doncov, Aerospace Technology Division, Library of Congress (ATD Report 66-120), Sept. 1966, 84 pages.

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What do you think?

This department is devoted to a continuous interchange of ideas, comments, and opinions on significant problems facing the industry. What do you think about the impact of a computer-automated world and the engineer/scientist's role in it? What do you think about engineering unions — professional societies — industry conferences? Or any significant facet of your professional life. COMPUTER DESIGN will print your views here. Write to: CD Readers' Forum, Computer Design, Baker Ave., West Concord, Mass. 01781.

CD READERS' FORUM

LOGIC SYMBOLS STANDARDS

Editor's Note: *In the CD Readers' Forum (January issue), we pointed out that "the basic and apparently irreconcilable matter of the right triangle versus the circle appears to prevent a compromise between the Y32.14 and 806B standards."*

This month's correspondents represent Sandia Corporation, a military contractor who has chosen Y32.14, and they offer a suggestion for resolving the "basic and apparently irreconcilable matter."

TO CD READERS' FORUM:

At Sandia Corporation, we deplored the same situation you portrayed so vividly in your Readers' Forum and tried to pick the eventual winner. We based our final selection mostly on two opinions, one historical — the other technical. The historically-based opinion relates to the fact that many military standards have been dropped in favor of commercial or ASA standards. Historically, MIL-806-B was an offshoot of an ASA task force on logic, to meet an immediate need. The technical opinion is that fixed potential logic is less powerful and less widely acceptable than mixed logic will be. As a result, we selected the one set of the options available in the ASA which would be as close as possible to MIL-806-B in case we had selected a loser. The result was Sandia Logic Diagram Standard, D10252.

We chose to omit the optional use of the filled right triangle in order to minimize the reproduction processing difficulties and to permit a simple "rule of thumb" substitution if translation from or to positive potential logic MIL-806-B is required. The rule is to substitute an open circle for the right triangle wherever it appears or vice versa. The portions of the standard pertinent to this rule are presented below. This restriction to one of the many options of ASA Y32.14 will also allow direct reading of Bell Labs Standard SD-Schematic Dwg. Stds.-Appendix A (essentially Positive Logic ASA) and the NASA Standard MFSFC-STD.-353 by anyone familiar with this single rule of equivalence. Thus, anyone could use either 806B or ASA Y32.14 (the above described option only) and be able to read and interpret electrical logic, mathematical logic, circuit functions, and troubleshooting voltage levels by equating the open triangle and circle to the same place on a logic diagram.

We consider there is a real advantage to the use of the ASA over MIL-806-B in the realm of precise definitions. Careful scrutiny of the ASA definition of the electrical inverter indicates a distinction must be made between electric potential and (logic) truth. Such a distinction is contrary to fixed potential logic and was difficult to accept at first. After using the ASA, however, we find that it makes much more sense to permit the above distinction than to perform a logic inversion at the input or the output of every gate. The result of the distinction is called mixed logic. With such a system every symbol on the diagram conveys meaningful information to both the logic designer and the field maintenance, service, and troubleshooting staff. By keeping electrical condition information separate from the logic equations until they must be reconciled, the interpretation of logic diagrams is simplified. The troubleshooter can interpret each symbol separately to find out which item is failing to act electrically the way the symbol says it should. The logic designer can document exactly what he had in mind by showing the OR shapes for gates where his logic

Continued on page 25

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Continued from page 22

equations contained + symbols and AND shapes for gates where the equations contained • symbols and selecting the inverter symbol or the amplifier symbol depending on whether polarity correction or gain was primarily intended.

Your final paragraph states that a compromise between the standards is apparently irreconcilable because of the matter of right triangle vs. circle. As we have presented above, there is a compromise for one set of options of ASA and a restriction to positive potential logic in MIL-806-B. These marks are not equivalent to the symbol and associated level, but they are translatable.

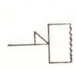
Please count us among those who recognize the need for a universally accepted standard. Also count us among those who strongly advocate thoughtful consideration of the set of options we have selected from those available in the ASA as a technically and economically attractive candidate for such a standard.

Robert W. Roberts, Div. Supervisor,
and
L. J. O'Connell, Staff Member,
Sandia Corp.,
Albuquerque, New Mexico.

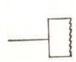
SANDIA LOGIC DIAGRAM STANDARD D10252 EXTRACTS

1. INTRODUCTION

This standard provides mixed logic and assignment of open right triangle for less positive voltage as logical 1 and absence of filled right triangle for more positive voltage as logical 1.

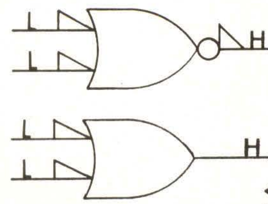


= less positive (L)
= logical 1



= more positive (H)
= logical 1

We observe that the combination of the logic negation symbol ○ and the level indicator (L), is equal to (H). Therefore, the following two logic diagrams are equivalent:



← **Note the absence of Filled right triangle per convention above.**

2. LOGIC NEGATION

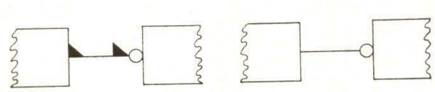
The output of a logic negation operation takes on the 1 state if and only if the input does not take on the 1 state.

a. Symbol — a small circle, ○, drawn at the point where a signal line joins a logic symbol indicates a logic negation.

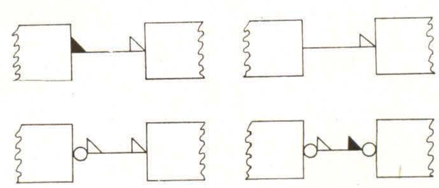
b. Detailed Logic Diagram — it should be noted that logic negation, in a detailed logic diagram, may be indicated by the relationship between types of level indicators on opposite ends of a line.

c. Deletion of Symbol — note that whenever a small circle appears adjacent to a level indicator, the circle may be deleted provided the level indicator is replaced by its opposite kind. Conversely, whenever a level indicator appears without adjacent small circle, it may be replaced by its opposite kind and adjacent small circle. Since they are equivalent representations, interchanging such symbols and indicators does not disturb the relationship between logic function symbols. For example, the following logic diagrams are equivalent.

SANDIA BASIC POSITIVE LOGIC



SANDIA DETAILED MIXED LOGIC



CD Readers' Forum welcomes comments from our readers on the above technique developed by Sandia.

DC OUTPUT

from our man in Washington

"It is well-known that the electronic computer industry at the present time is, and for many years, has been, out of balance in competitive structure," Representative Emanuel Celler, Chairman of the House Judiciary Committee recently told a Washington meeting of the Antitrust Law Section of the American Bar Association. Rep. Celler was discussing an investigation the House Antitrust Subcommittee, which he also heads, was conducting of the computer industry. Moreover, he said, "the significance of computers to innovation in our modern interrelated society can not be overstated. Antitrust enforcement officials must keep abreast of these emerging technologies if future markets are to remain accessible to all operators that have the means and are eligible to participate."

Rep. Cornelius E. Gallagher (D. N.J.) has asked the Defense Department and the General Accounting Office to reconsider the decision to assign social security numbers to incoming and present military personnel until a considerable amount of re-thinking had gone into the possibility that this information would be used to violate the privacy of the individual. Gallagher, who is Chairman of the House Invasion of Privacy Subcommittee, pointed out that "the computerization of this information would be a step in the wrongireciton — the direction of the establishment of a dossier bank within the government. The information accumulated under an individual's social security number is immense, and at least partially beyond the review of and the challenging by the individual. Such things as induction tests and their result would be indelibly attached to the personal history of every American inducted into the Armed Services."

Public Law 89-306, the Brooks Bill, assigned to the National Bureau of Standards a comprehensive responsibility for establishing standards to govern the widespread use of data processing systems by the Federal Government. A Research Associate Program directed towards the development of standards proposal has been undertaken by Stanley F. Buckland under the sponsorship of Control Data Corp. In this program, a natural adjunct to the work of the NBS Center for Computer Sciences and Technology, Buckland is developing both qualitative and quantitative information on the value of standards to EDP users, and is surveying user, manufacturer, and data transmission requirements for compatibility in data interchange. The possible impact of standards on capital operating costs of Federal EDP installations is also being studied.

IBM has been selected by the Air Force to provide EDP equipment (System 360 30/40) for a Base Level Automation Standardization Program which will provide a modern computer capability at base level throughout the Air Force. The IBM system will permit standardization and centralization of computer programming, processing techniques, and systems design. Installation of what has been estimated to be between 100 to 150 computers will be completed by 1970. No cost figures were given for the job, but it is estimated by trade sources to cost about $100 million.

Recent Government Contracts

URS CORP., Burlingame, Cal., has been issued a $1,154,-741 modification to a previously awarded contract for development of an automatic data processing system dealing with software for the Seventh Army. Work will be done in Germany. The Engineeer R&D Labs, Fort Belvoir, Va., is awarding the contract.

RCA, Burlington, Mass., has received $1,000,000 for work on an airborne data automation system. The Electronic Systems Division (Air Force Systems Command), L. G. Hanscom Field, Mass., is the contracting agency.

DATA PRODUCTS CORP., Culver City, Cal., has received a $1,342,948 fixed-price incentive contract for high-speed line printers for ship computer systems. The Naval Ship Systems Command is the contracting agency.

IBM, Gaithersburg, Md., has been awarded a $17,216,536 contract for four additional computer systems to automate and modernize the nation's air traffic control system by the Federal Aviation Administration. The systems will be installed in four of FAA's air route traffic control centers.

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The DATA/620-I integrated circuit computer is the newest member of the DATA/620 family of system computers. DATA/620-I fills the gap between general purpose and special purpose computers. It belongs in a system, and solves problems previously considered too difficult or expensive for computer solution.

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Extremely compact, the DATA/620-I requires only 10" of 19" rack space. It's available with memory modules from 1024 to 32,768 words of 16 or 18 bits, and with a selection of control, arithmetic and I/O facilities, including D.M.I.'s unique Micro-Exec.

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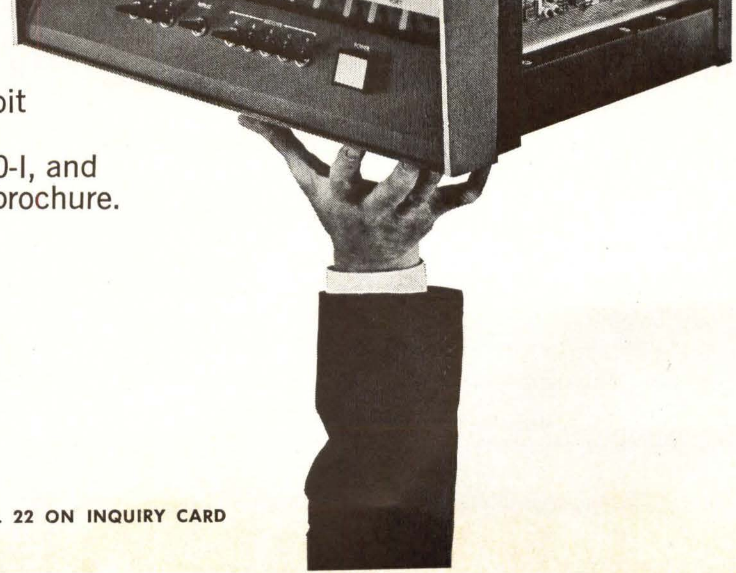

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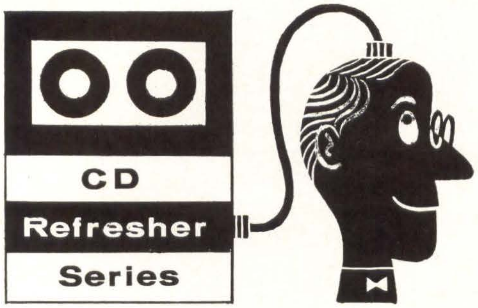


MATHEMATICS REVISITED:

Selected Topics In Probability And Statistics

Dan M. Bowers, Contributing Editor

Part 11 - TESTS of HYPOTHESES and RANDOMNESS

Last month we investigated sampling, a useful application of statistics which allows us, by examining only a relatively few bits of the data, to obtain information about a large population of data. This month we shall discuss another useful application: testing of hypotheses — which is a method by which we can minimize the chance of error by evaluating the risks inherent in a prospective decision.

The hypothesis which we desire to test may be one of the following kind:

- Selling through sales representatives is more effective than selling with direct salesmen.
- Transistors purchased from manufacturer X have a longer life than those purchased from manufacturer Y.
- Most UFO sightings have not been satisfactorily explained.
- Trout in the Yellow Breeches Creek are larger than those in Kettle Creek.

Based on the results of testing the hypothesis under consideration, we plan to take some action or make a decision, and we desire to know the risks involved. If the above hypotheses were true, we might plan to take the following actions:

- Change from direct salesmen to reps.
- Specify manufacturer X as the primary source for transistors.
- Initiate a research effort to determine whether UFO's are of extra-terrestial origin.
- Fish only in the Yellow Breeches Creek.

Any time a decision is made, there is the possibility that it is wrong. For example, if we are presently selling with direct salesmen, we are continually making either the decision to stay direct, or change to reps. If we stay direct, but it would have been better to change to reps, we have made an error; and if we change to reps but it would have been better to stay direct, we have again erred. These two kinds of errors are known in statistics as alpha-type and beta-type errors:

- Alpha-type error: we reject a hypothesis which should be accepted.
- Beta-type error: we accept a hypothesis which should be rejected. Obviously, we define what is an alpha-error and what is a beta-error by the way in which we state the hypothesis.

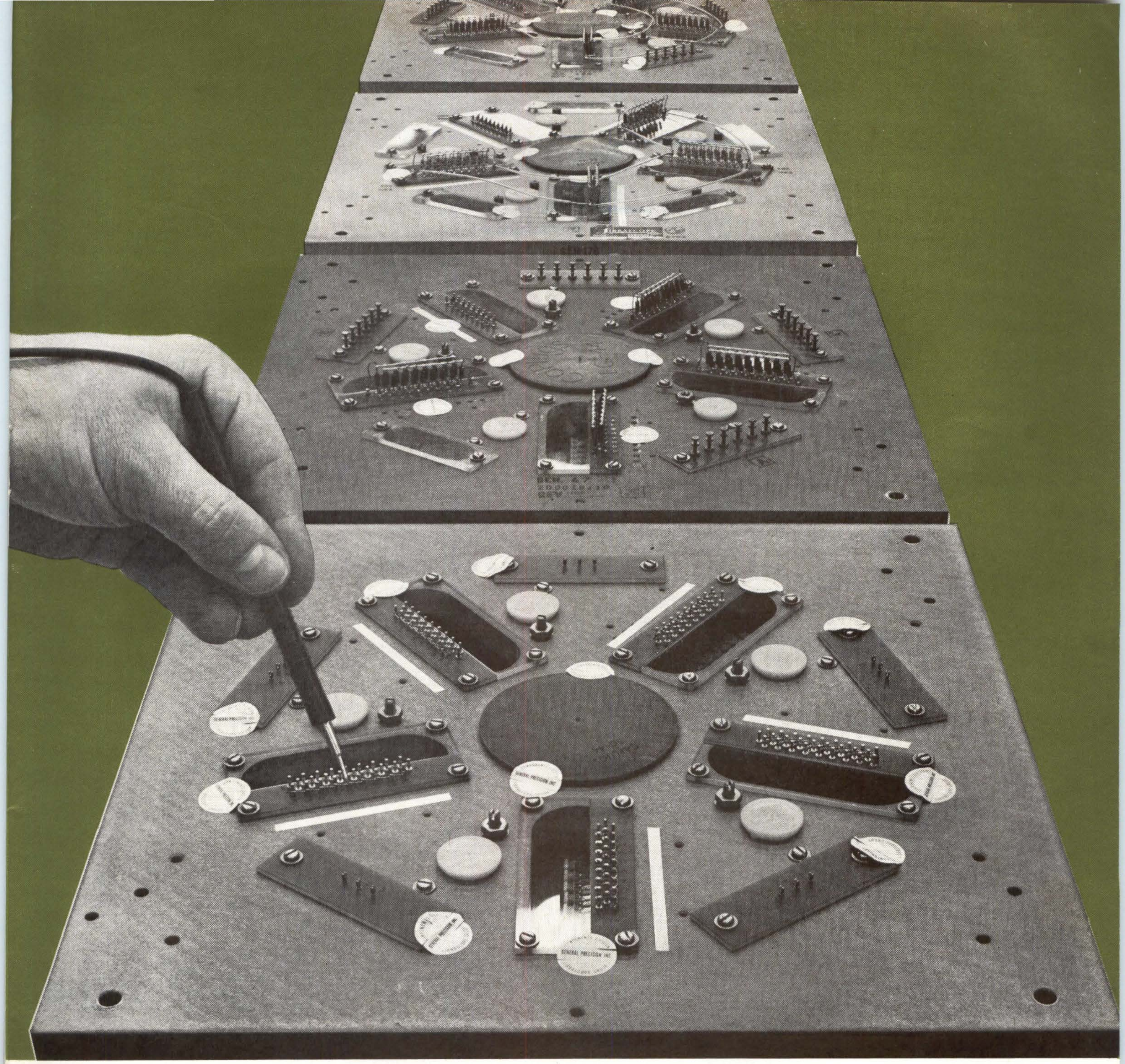
As an example of this decision-making process, let us consider the transistor life problem. Assume that we are presently purchasing transistors from manufacturer Y, and that our long-run experience (1000 samples) is that the mean life of these transistors is 10,000 hours, with a standard deviation of 1000 hours. Our QC department has tested 100 transistors from manufacturer X, and has established that these devices have a mean life of 10,250 hours with a standard deviation of 1200 hours. Engineering management desires to know whether, on the basis of these facts, manufacturer X should become our supplier, replacing manufacturer Y. Statistically speaking, we want to know whether the apparent longer life of X is **statistically significant,** or whether it can **reasonably be attributed to chance.** We may state our hypothesis as: "There is no statistically significant difference between the two means." Therefore if the hypothesis is true, we shall continue to purchase transistors from Y, and if it is false, we shall change to X as a supplier; our alpha and beta errors have thus been defined.

The sampling theorems which we presented last month are modified to fit this situation, and we have:

- Theorem: **standard error of the difference of two means** — if two large random samples of size n_1 and n_2 have means m_{s1} and m_{s2}, and are taken from populations with means m_1 and m_2 and standard deviations σ_1 and σ_2, then the theoretical sampling distribution of $m_{s1} - m_{s2}$ can be approximated closely with a Gaussian curve with mean $m_1 - m_2$ and standard deviation:

$$\sqrt{\frac{\sigma_1^2}{n_1} + \frac{\sigma_2^2}{n_2}}$$

which is known as the standard error of the difference of two means.



As we did last month, we shall substitute the standard deviations of the samples for the unknown, σ_1 and σ_2, and therefore we have for the theoretical sampling distribution of $m_{s1} - m_{s2}$:

$$m = m_1 - m_2$$

$$\sigma = \sqrt{\frac{\sigma_{s1}^2}{n_1} + \frac{\sigma_{s2}^2}{n_2}}$$

From our statement of the transistor problem:

$$m_{sy} = 10{,}000 \qquad m_{sx} = 10{,}250$$
$$\sigma_{sy} = 1{,}000 \qquad \sigma_{sx} = 1{,}200$$
$$n_y = 1{,}000 \qquad n_x = 100$$

and the hypothesis is: $m_x = m_y$.

In accordance with the theorem, then, we construct the normal curve shown in Fig. 1 for the theoretical sampling distribution of $m_{sy} - m_{sx}$, with $m = 0$ in accordance with our hypothesis, that $m_1 = m_2$ and:

$$\sigma = \sqrt{\frac{\sigma_{sy}^2}{n_y} + \frac{\sigma_{sx}^2}{n_x}} = \sqrt{\frac{(1000)^2}{1000} + \frac{(1200)^2}{100}} = 120.$$

The actual observed value of $m_{sy} - m_{sx}$ is 250 hours, or 2.08 σ from the mean. From the chart in Part 6 (November 1966), we find that the area under the Gaussian curve between this and the mean is 0.481, and therefore the probability of occurrence of this deviation is $2(0.500 - 0.481) = 0.038$ (the shaded area in Fig. 1), i.e., the probability that the hypothesis $m_x = m_y$ is true is about 0.04.

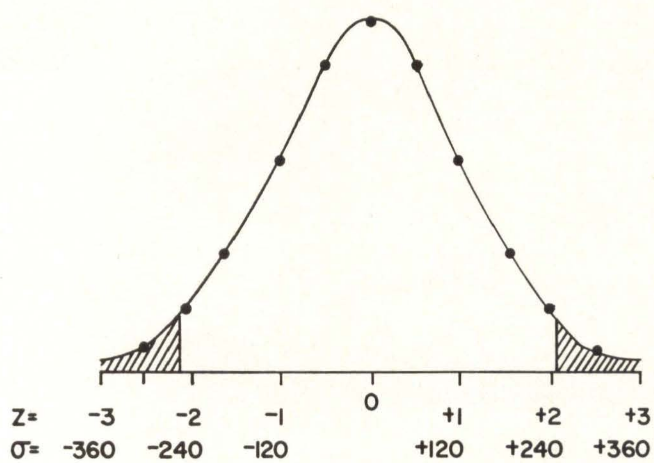


Fig. 1: Theoretical Sampling Distribution of $m_{sy} - m_{sx}$.

We conclude therefore, that the probability that brand X transistors have a longer life than brand Y transistors is 0.96, and that we would be well advised to change to brand X (providing, of course, that life-time is the ruling criterion).

Tests For Randomness

In the opening sentence of this series of articles, we specified the three cornerstones of probability and statistics: "randomness," "independent trials," and "in the long run." Although we have discussed these frequently during the series, the reader may still be left with the nagging doubt that, despite careful procedures, he may somehow end up with a non-random sample or a non-random experiment. There are several methods of determining, from sampled data alone, whether or not the sample is random, and we shall discuss three of these as the last topic in this series of articles.

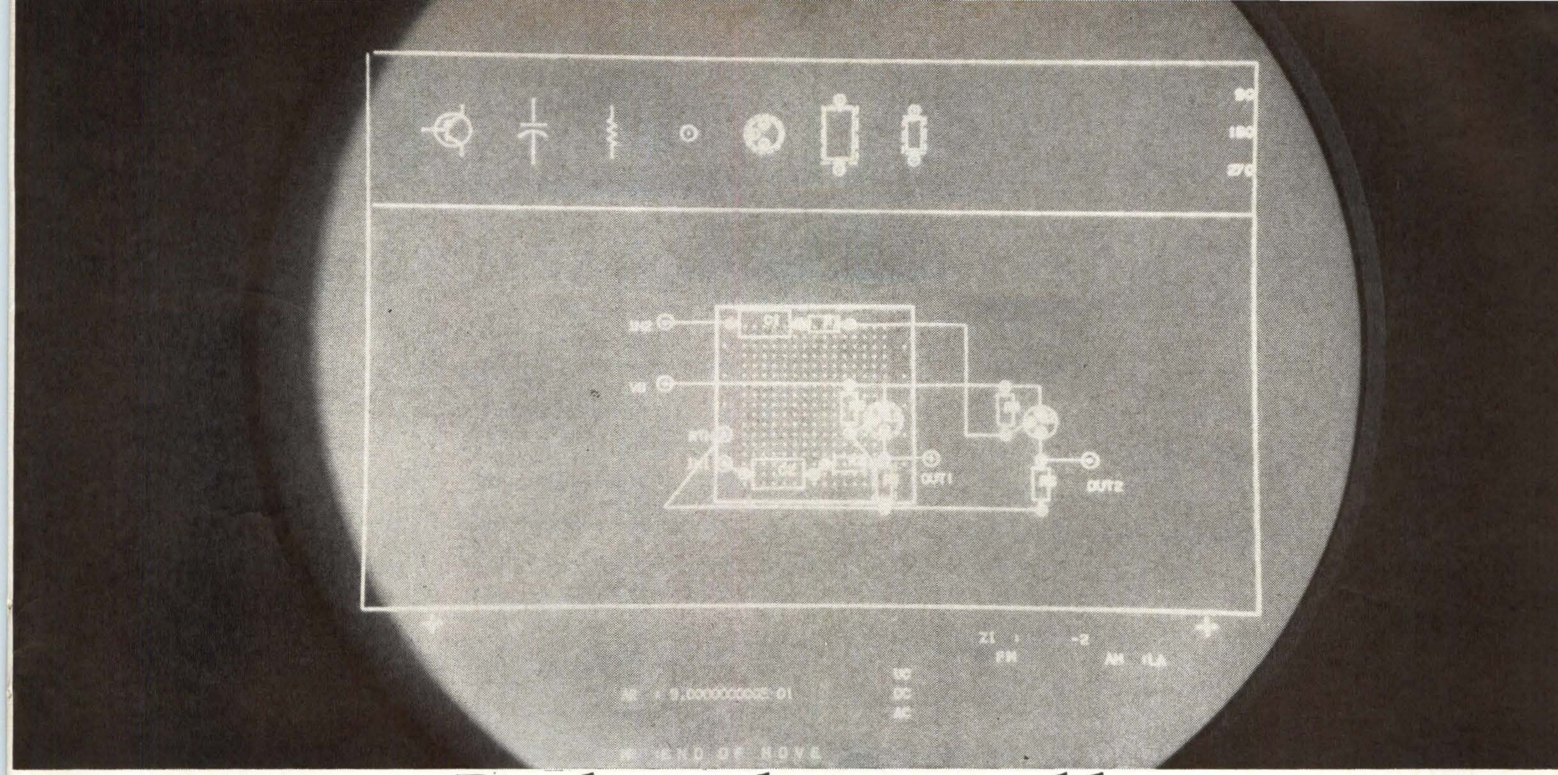
The first of the three relates to the method of testing of hypotheses described above. Although several variations are possible, for illustrative purposes we might consider the method of taking two (or, by extension, more) samples from the same population. We can then test by the above method to see if the difference between the means of these two (or more) samples is statistically significant: if so, then at least one of the samples is probably not a random sample.

A second method which has been used is to determine whether the data in question is a good fit to an expected (e.g., Gaussian or binomial) curve. This requires a large quantity of data; for example, if a binary digit stream were being tested for randomness, we would calculate the following probabilities of occurrence for various bit patterns:

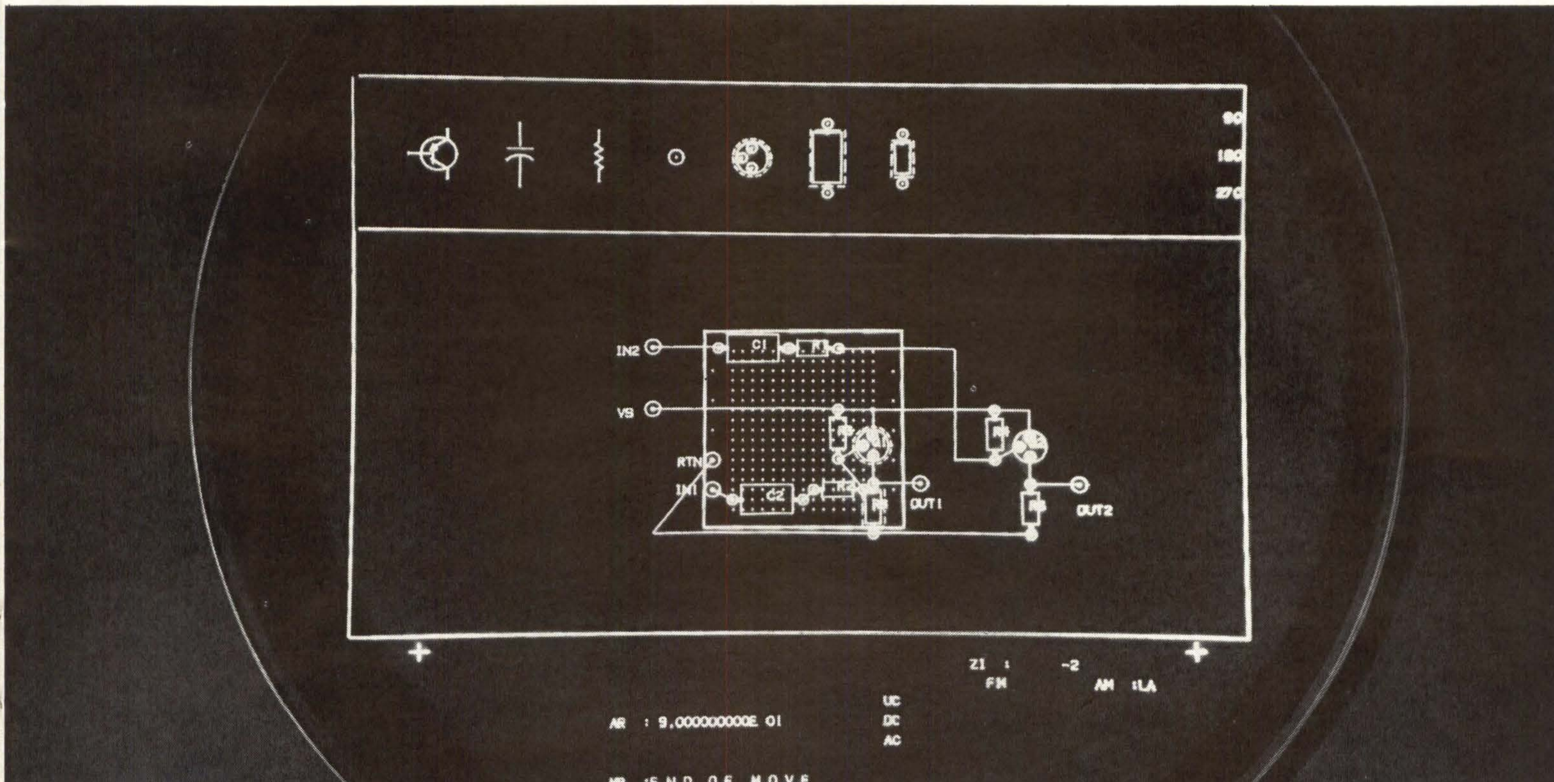
bit pattern	P	Occurrences per 10^3 bits
0	0.500	500
1	0.500	500
00	0.250	250
01	0.250	250
10	0.250	250
11	0.250	250
000	0.125	125
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
111	0.125	125
0000	0.063	63
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
1111	0.063	63
•	•	•
•	•	•
•	•	•

The entire bit stream would then be analyzed, the number of occurrences of each bit pattern counted, and the results compared with the calculated occurrences to determine "goodness of fit."

The third — and most interesting — test for randomness is known as the theory of **runs.** It is particularly well adapted to binary problems such as that discussed above under the curve-fitting test; however, to illustrate both its binary and general utility, we shall use it to test the randomness of



Readouts clear up problems.



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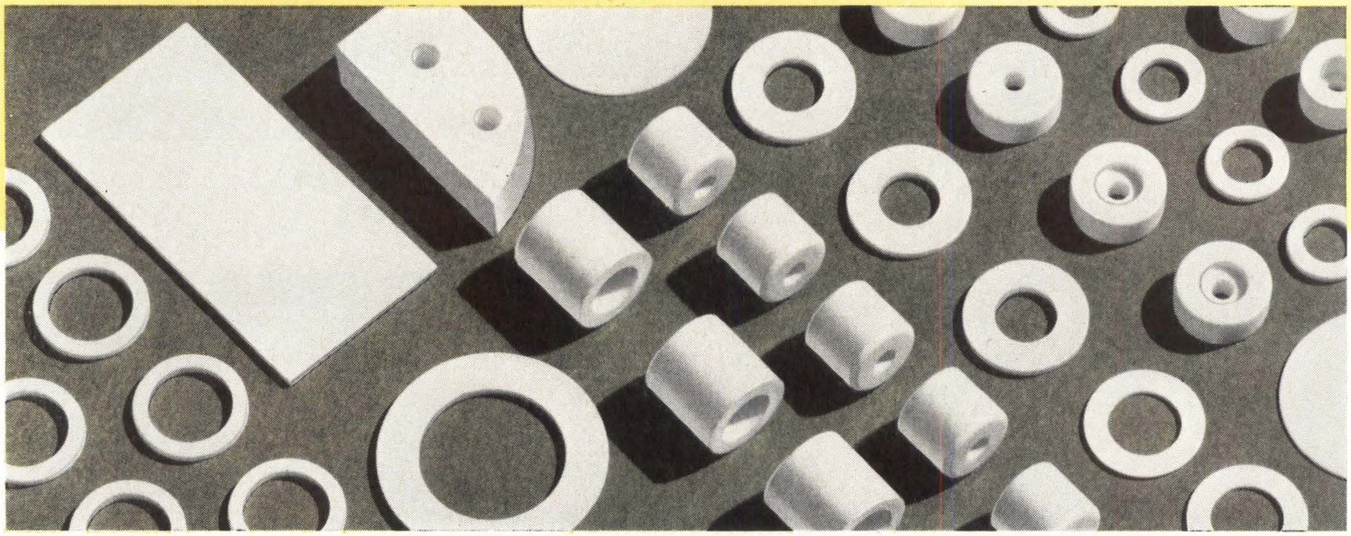

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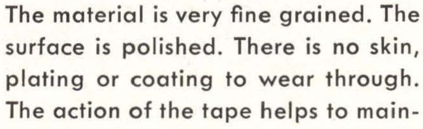

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the 36 mutual fund prices used last month to illustrate sampling theory:

32.69	6.27	8.77	6.85
14.67	32.69	16.74	8.14
7.52	18.85	30.49	18.33
7.25	10.24	14.67	7.25
6.58	9.80	11.61	14.09
21.62	8.88	10.29	7.54
23.79	4.78	1.72	4.46
8.79	13.84	18.14	11.30
6.91	11.54	18.98	13.67

We begin by finding the median of the sample, which is \$10.29½. We then replace each item in the sample by either the letter H or the letter L, depending upon whether the item had a value higher or lower than the median:

HHLLLHHLLLHHLLLLHHLHHHHLLHHLLHLHLLHH

Note that we have created a binary sequence of digits out of the sample of dollar values, and that therefore the procedure from this point applies equally well to determining the randomness of, for example, a coin (heads or tails), a roulette wheel (odd or even, red or black), or consumer preference between two brands (A or B).

The theory of runs is a method of testing the randomness of a binary sample, based on the order in which the items occur in the sample. Taking the string of H's and L's above, we define a "run" as a contiguous sequence of identical letters, and count the total number of runs:

HH	LL	HH	LLL	HH	LLLL	HH	L	
1	2	3	4	5	6	7	8	
HHHH	LL	HH	LL	H	L	H	LL	HH
9	10	11	12	13	14	15	16	17

The theory of runs postulates that too many runs in a sample indicates a cyclic pattern (e.g., HLHLHLHL), and that too few runs indicates a trend (e.g., HHHHLHHLLHLLLL); the tests of hypothesis can be used to establish the presence of cycles or trends once the theory of runs has indicated that they may exist.

The basis of the theory is to judge whether the observed number of runs differs significantly from the number to be expected in a random selection, and we shall accept on faith the statement that the theoretical sampling distribution of the total number of runs in a binary sequence can be closely approximated by a Gaussian curve with the following parameters:

$$m = \frac{2n_1 n_2}{n_1 + n_2} + 1$$

$$\sigma = \sqrt{\frac{2n_1 n_2 (2n_1 n_2 - n_1 - n_2)}{(n_1 + n_2)^2 (n_1 + n_2 - 1)}}$$

where n_1 and n_2 are the number of items of each of the two binary values. In our sample, we had $n_1 = 18 = n_2$; therefore:

$$m = \frac{2 \times 18^2}{36} + 1 = 19$$

$$\sigma = \sqrt{\frac{2 \times 18^2 (2 \times 18^2 - 36)}{36^2 \times 35}} = 2.96$$

← Circle No. 24 on Inquiry Card

The total number of runs in our sample was 17, or 0.675σ from the mean of 19, giving a probability of occurrence of slightly over 0.500, and indicating that we do have a truly random sample.

Tables of Random Numbers

There exist tables of random numbers, for which random digits have been generated by digital computers or other machines, which can be used in the selection of random samples and in other random operations. The sampling of 36 mutual fund prices from the list of 188, which we have just shown to be random, was selected from such a table using the following procedure. The book of random numbers was opened to an arbitrary ("random") page, and the first three random digits thereon were used to select a page number, the next two digits to designate a column on the selected page, and the following two digits to designate a row on the selected page. The designated row and column on the selected page was then used as the starting point, from which the succeeding 108 random digits were extracted in thirty-six groups of three digits each; each of these 36 three-digit numbers was then reduced modulo-188 to obtain a number between 1 and 188.

EPILOGUE

In introducing the **CD Refresher Series** in April 1966, we stated that our purpose was to present basic analytical techniques, of use to the design engineers and management personnel whom we serve in a form useful both as a review and as a primer We have devoted the first eleven articles in this series to communicating a basic understanding of the usefulness of probability and statistics, which is not a difficult subject when reduced to a relatively simple form and stripped of its mystique, jargon, and mathematical rigor. To avoid becoming bogged down in rigorous mathematical developments and pages of integrals, we have frequently used borrowed results and intuitive arguments, and we hope that this applications-oriented approach will stimulate the reader to utilize probability and statistics as tools in the pursuit of his profession — or in the pursuit of riches through gambling, to which we have also devoted considerable space because games of chance are excellent illustrations of the subject.

The CD Refresher Series will observe a summer vacation from cerebral endeavors (to the inexpressable relief of our production staff, who are tasked with keeping each integral sign, greek letter, and sub-subscript in its rightful place), and will begin discussion of a new technical subject, with the same concern for usefulness over rigor, in the fall. We shall soon make the "Selected Topics in Probability and Statistics" series available in booklet form.

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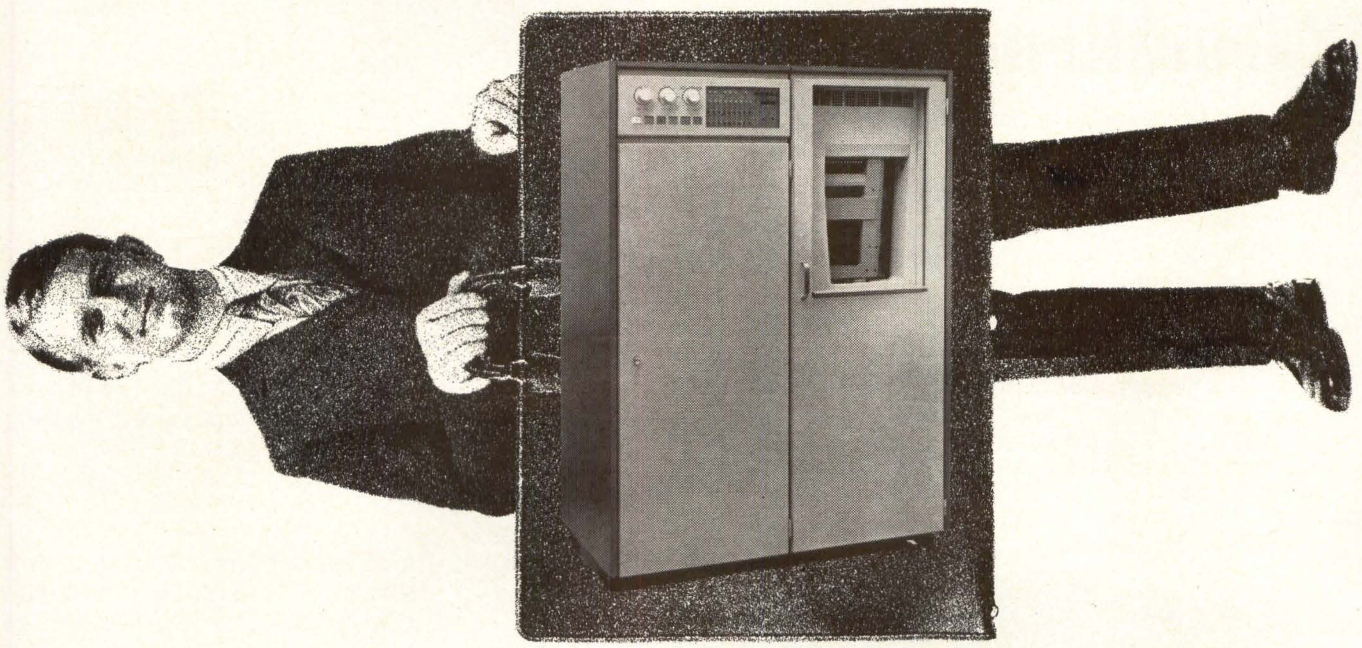

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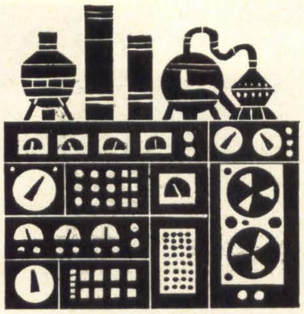

INDUSTRY NEWS

THE FIRST PRACTICAL PROCESS FOR BUILDING SUPERCONDUCTIVE COMPUTER MEMORIES THAT MAY STORE UP TO A BILLION BITS OF DATA AND OPERATE SEVERAL TIMES FASTER THAN PRESENT WIDELY USED MASS-INFORMATION STORAGE UNITS was announced recently by the Radio Corporation of America. Dr. James Hillier, Vice President, RCA Laboratories, called the achievement a major advance in information storage technology. He said that it represents the culmination of 11 years of intensive research to harness superconductivity for use in practical high-capacity memory systems. Dr. Hillier said RCA scientists already have constructed a unit that stores 14,120 bits of information in arrays of microscopic "loop cells" made of superconductive materials deposited in thin films on glass slides. The experimental unit can recall the stored information at a rate of nearly half a million bits per second, he said. Both the new technology and the experimental memory resulted from a program partially sponsored by the Air Force Systems Command, Wright-Patterson Air Force Base, Dayton, Ohio, and led by John Carrona, head of Cryoelectric Devices Laboratory at RCA's David Sarnoff Research Center, Princeton, N. J. The technical effort was directed by Robert Gange, of the RCA Laboratories technical staff.

According to Mr. Carrona, the problem in applying superconductivity to computer memories was to devise a loop structure that could be fabricated uniformly by the thousands and could be made to carry a tiny current whose energy could be sensed or removed at will. "This has been accomplished through development of a cell consisting of thin layers of lead, tin, and insulating material deposited in large arrays on a glass slide," he said. "Our experimental memory is made up of four such slides stacked one atop the other and interconnected along their edges."

A DEVELOPMENT PROGRAM FOR A NEW TYPE OF MAGNETIC RECORDING TAPE is being conducted by the Du Pont Company. The tape employs a unique magnetic material, chromium dioxide, rather than conventional iron oxide. The patented compound was developed in the course of a Du Pont research program in the general field of magnetism. Among the advantages of the new tape are its greater magnetic strength and fidelity in high frequency instrumentation and video recording, and its increased reliability and information storage capacity in computer use. Du Pont is planning to produce development quantities of the tape in a manufacturing facility recently completed at the company's Newport, Del., site.

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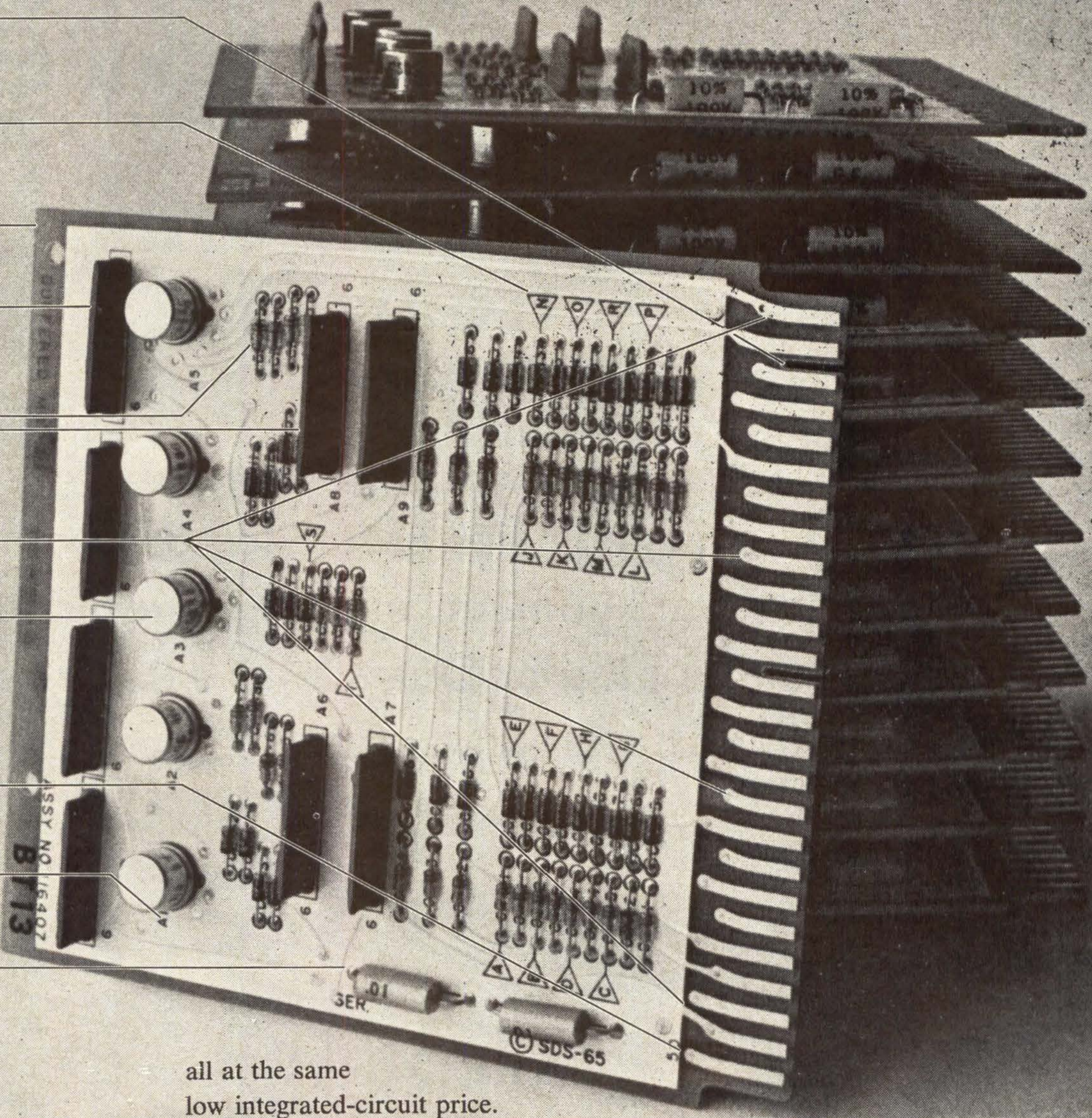

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INDUSTRY NEWS

A PATENT FOR AN INVENTION WHICH HELPED PAVE THE WAY TO FASTER, MORE EFFICIENT DATA PROCESSING SYSTEMS AND WHICH HAS BEEN WIDELY USED THROUGHOUT THE COMPUTER INDUSTRY was issued to IBM Corp. The invention provided an automatic interruption to the processor to signal that a data transfer originally requested by the processor was ready to occur. The execution of the program is delayed or interrupted for a minimum length of time, permitting maximum use of the computer components. The unique interrupt feature of this data processing machine is used in most present-day computers. Incorporated in U.S. Patent number 3,319,230 for which a patent application was originally filed in 1956, the invention is entitled "Data Processing Machine Including Program Interrupt." The invention has a simultaneous overlapping feature which permits a computer program to continue operating after requesting input/output (I/O) information. These I/O data are retrieved independently of the program after the request is initiated. Prior systems either required the computer program to issue instructions at appropriately-timed intervals to transfer data from or to memory, or to wait after selecting an I/O device until data transmission was complete. Principles of the invention are used in IBM System/360 and in almost all other data processing systems. It resulted from the work of Dr. Morton M. Astrhan, Bennett Housman, Hrand L. Kurkjian, and Bernard L. Sarahan while they were working on an early computer system for IBM.

A FOUR-WAY EXPANSION OF THE LOW-COST IBM 1130 COMPUTING SYSTEM WAS ANNOUNCED BY IBM. Users whose data processing needs grow, but who do not require the computing power of an IBM System/360, can now use the 1130 to meet those needs in both technical and commercial areas. C.B. Rogers, Jr., vice president—marketing of IBM's Data Processing Division, said, "The 1130, originally developed as a small scientific computer, has now been improved in four major areas to help users tailor it to their individual needs." Expansions of the 1130 include:

- Five times the disc storage; four time the magnetic core memory size;
- An additional processing speed almost 40 per cent faster than previously available;
- More and faster peripheral equipment, including an optical mark reader;
- An improved commercial programming package.

Other peripheral include high-speed printers, card and paper tape readers and punches, and a plotter that represents data in graphic form. Printing speeds of 600 lines per minute and card reading speeds of 1,000 cards per minute are now available. The minimum IBM 1130 computing system rents for $716 a month and sells for $30,975. Ranges for disc-oriented systems are monthly rentals of about $950 to $5,800 and purchase prices of about $45,000 to $270,000, depending on core storage size and types of peripherals. Deliveries of 1130's with newly-announced features are scheduled to start in January 1968. The system will continue to be manufactured at IBM facilities in San Jose, Cal.

INDUSTRY NEWS

TWENTY COUNTRY BANKS NESTLED THROUGHOUT NORTHWESTERN OHIO AND SOUTHWESTERN MICHIGAN ARE PROVING THAT THE COOPERATIVE USE OF MODERN DATA COMMUNICATIONS AND DATA PROCESSING IS GIVING THEM THE EDGE NEEDED TO COMPETE WITH THE BIGGER INSTITUTIONS. Tied to a computer center in Fremont, Ohio, by a teletypewriter network, the banks have been able to broaden their services to customers while simultaneously cutting their costs of doing business. The center is identified as Financial Computer Services, Inc., which was established originally by six of the present banks. It is one of the first of its type in the nation, and is designed to permit on-line, real-time operation in the future. Today, data transmitted to the center is digested by two computers in the processing of over 70,000 checking, 55,000 savings, and 7,000 installment loan accounts of member banks. And, according to James E. Stoner, executive vice president, the center is also processing bank general ledgers, safe deposit box rental billings, Christmas clubs, shareholder records and dividend checks, certificates of deposit, and bank payrolls. Modern teletypewriters provide the communications link to transmit a variety of bank "file maintenance" information from new accounts to name and address changes. The network also finds application in providing ready, fast communications not only between member banks but also with others throughout the country. This is particularly important within the Federal Reserve System, Stoner states. Over half of the twenty banks on the teletypewriter network transmit via Bell System Teletypewriter Exchange Service (TWX), with the remaining firms transmitting over private leased lines. The basic communications device is the Teletype Model 33 ASR (automatic send-receive) set. This machine features a send-receive page printer, a paper tape punch, and a paper tape reader which can be used in various combinations. It operates at 100 words per minute (10 characters per second) and utilizes a code compatible with the United States of America Standard Code for Information Interchange (USASCII). Financial Computer Services pays all teletypewriter costs, including charges for the machine on bank premises.

AN ELECTRONIC BALLPOINT PEN WHICH TRANSLATES GRAPHIC MATERIAL TO COMPUTER LANGUAGE AS IT WRITES AND TRANSMITS DATA SIMULTANEOUSLY TO COMPUTERS FOR STORAGE OR ANALYSIS was introduced recently by Sylvania Electric Products Inc. Known as the Sylvania Data Tablet, the system converts written symbols to digital and analog signals for transmittal to computers or over telephone lines for display at remote locations. The writing area is a conductive surface on which electric waves travel in "x" (horizontal) and "y" (vertical) directions. As the pen passes over the writing surface it records its position by measuring the phase of these "x" and "y" signals at a rate of 200 per second. In addition to "x" and "y" measurements, the Sylvania Data Tablet has a third axis capability. Varying the height of the pen above the tablet can assign electronically an increased number of characteristics to graphic elements.

FORMATION OF THE INTERNATIONAL SOCIETY OF HYBRID MICROELECTRONICS, a professional society devoted to the furtherance of the state of the art in hybrid film microelectronics, was announced recently in Mountain View, California by the Ad Hoc Committee for Thick Films. Acting as spokesmen for the committee, George Anderson of Fairchild Semiconductor and George Doyle of Union Carbide explained that the First Technical Thick Film Symposium, held by the committee in Palo Alto, California in February, was a great success and has stimulated interest in formation of a permanent organization to provide an open forum on Hybrid Film Microelectronics. Mr. Doyle stated that interest has not been limited to so-called thick films alone, but that substantial interest in vacuum deposited thin film has also been evident. Since both techniques are used for microelectronics and perform similar functions, it is necessary for engineers and scientists to know something of both disciplines in making a technical and economic selection for their application. The Society will concentrate on, and encourage, a free interchange of ideas, problems and technology covering film microelectronics. It will include those areas related to materials, processes, control, adjustment, attachment to, and protection of the film microcircuit from the point of view of design and manufacture. In addition, it will encourage interest in developing new circuit and systems philosophies which optimize designs for the characteristics inherent in film and hybrid microelectronics. For further information, contact Mr. George Doyle, Union Carbide Electronics, 365 Middlefield Road, Mountain View, Cal.

BROADBAND LIGHT MODULATORS FOR FUTURE OPTICAL COMMUNICATIONS SYSTEMS

Light modulators developed at Bell Telephone Laboratories now makes it possible to impress broadband communications signals onto laser beams using modulating powers of less than one watt. Most earlier modulators required too much power or had insufficient bandwidth to be practical.

In one device, pulses of visible light passing through a lithium tantalate crystal are modulated for digital transmission when an electric field is pulsed rapidly through the crystal. In another, near-infrared light waves traveling through a gallium-doped crystal of yttrium iron garnet (YIG) are continuously modulated when the direction of the crystal's internal magnetic field is varied. In a third device, varying a reverse bias to a gallium phosphide diode modulates visible or near-infrared light traveling along the plane of the diode p-n junction.

The three devices are the most efficient modulators of infrared and visible light to be demonstrated thus far. All three can modulate both pulsed and continuous laser light.

The lithium tantalate electro-optic modulator — developed by R. T. Denton, T. S. Kinsel, F. S. Chen, and A. A. Ballman — has been used in an experimental system for high-speed transmission of pulse code modulation (PCM) signals. In PCM systems, information (television, voice, and data signals) is translated into a coded sequence of electrical pulses (bits), which are then transmitted at very high rates (in this case, 224 million bits per second).

The electro-optic modulator uses this coded sequence of high-speed electrical pulses to modulate an equally fast, uncoded train of light pulses from a helium-neon laser. A thin rod of lithium tantalate crystal, measuring only 0.4 x 0.01 x 0.01 inch, acts as a high-speed optical gate. In effect, the crystal either blocks or passes each pulse, producing a coded sequence of optical pulses.

Because the optical pulses are of considerably shorter duration than the PCM pulse repetition period, several high-speed PCM signals converted to optical pulses can be multiplexed or combined on a single laser beam. The width of the pulses from the helium-neon laser allows four pulses to be inserted during each PCM pulse repetition period, so the maximum potential speed of this optical PCM system is 896 megabits (million bits) per second. This bit-rate, corresponding to a bandwidth of about 1600 megahertz, can be achieved by using four modulators to time-multiplex signals from four PCM terminals. Future experimental systems using a solid state laser with narrower pulse widths will have a potential speed of 5000 megabits per second.

The lithium tantalate modulator requires only 10 milliwatts input power to a transistor pulse amplifier, which supplies the drive voltage for the crystal (30 volts across 5.5 picofarad capacitance to produce 100 per cent modulation). Lithium tantalate requires only 1/20 the power required by KDP (potassium dihydrogen phosphate), the most common electro-optic material used in the past.

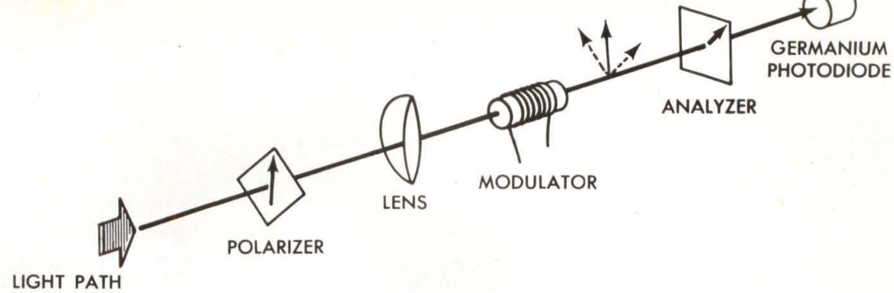
The infrared modulator, invented by R. C. LeCraw, consists of a thin rod of gallium-doped YIG crystal with a small coil wound around it. It operates on the principle of Faraday rotation. Light passing through the crystal is continuously modulated by varying a current or signal in the coil. The strength of this signal determines the amount of modulation at any time.

When operated at room temperature with a modulating power of less than 1/10 of a watt, this modulator exhibits a bandwidth of 200 megahertz and 40 per cent modulation. (A bandwidth of 200 megahertz is sufficient to transmit about 50,000 telephone calls or 30 television programs.) LeCraw's modulator has a bandwidth of 400 megahertz when operated at ⅓ of a watt; its maximum potential bandwidth has not yet been determined.

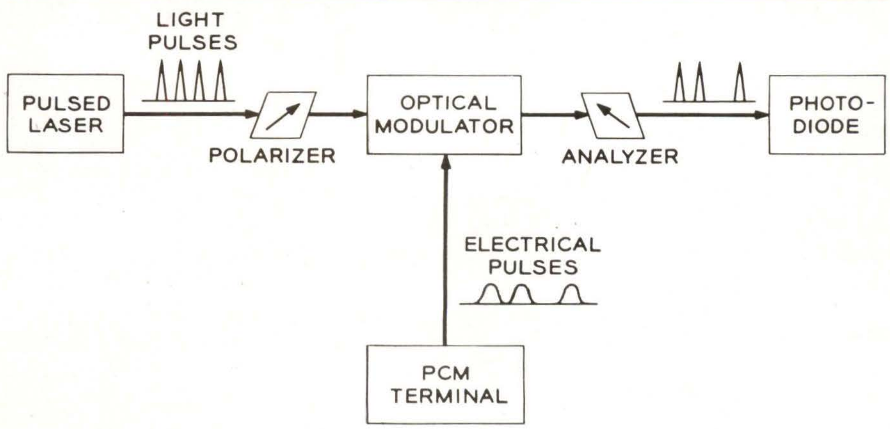
The gallium phosphide modulator — developed by A. Ashkin, M. Gershenzon, D. F. Nelson, and F. K. Reinhart — consists of a semiconductor p-n junction, together with a suitable mounting and input and output lenses. The p-n junction is made in the form of a narrow strip. The laser light is confined within the plane of the p-n junction by discontinuities in the index of refraction along both sides of the junction. This light is modulated by varying a reverse bias voltage to the junction. Light of wavelengths ranging from 0.55 micron to several microns can be modulated with gallium phosphide diodes.

This type of modulator has exhibited phase modulation corresponding to over 80 per cent intensity modulation of visible light (0.63 micron wavelength) when excited with 1.5 milliwatts of power per megahertz of modulation bandwidth. The diode used to demonstrate this capability was 0.06 inch long, and the modulation required 24 volts (peak-to-peak) across the capacitive (6.7 picofarad) junction. This test of modulation efficiency was made at 51.1 megahertz, but modulation can be achieved in this diode at all frequencies up to 7000 megahertz. Optical losses were less than 3 db.

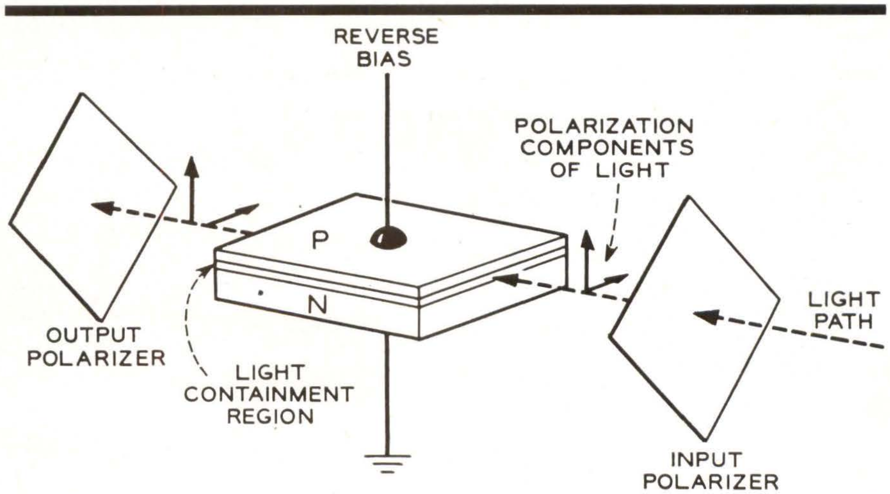
Many other light modulating materials are being studied at Bell Laboratories. For example, work done by I. P. Kaminow, E. G. Spencer, R. T. Denton, and E. H. Turner has shown that barium titanate and lithium niobate exhibit modulating efficiencies that are comparable to those of the materials mentioned above. Many modulating materials are being investigated because each material modulates most efficiently at its own characteristic frequency. The ability to modulate efficiently several laser frequencies is an obvious advantage for the designers of optical communications systems of the future. The operating frequency or frequencies of these future systems will be established when the system designers choose — from the lasers, modulators, transmission paths, demodulators, and detectors then available — those elements that are the most economical and technically sound. END



The modulator of near-infrared laser light is a thin, rod-shaped crystal of gallium-doped yttrium iron garnet. Polarized infrared light is focused by the lens and enters the modulating crystal. The magnetic field within the modulator changes as the signal in the surrounding coil varies. The plane of polarization of the light fluctuates in response to the changing magnetic field. An analyzer, which is simply another polarizer rotated clockwise 45 degrees, translates the fluctuating plane of polarization into an amplitude modulated light wave. This light wave is detected by a high-speed germanium photodiode, which demodulates the signal impressed on the light beam.



This diagram illustrates how light waves are modulated with gallium phosphide diodes. With a reverse bias applied to the diode, an incoming light wave is polarized and focused on the diode p-n junction region. The two polarization components of the light wave then travel at different velocities along the plane of the p-n junction and emerge from the junction out of phase with each other. The change in velocity imparts a phase modulation to each polarization component of light. To achieve amplitude modulation, the phase-modulated components of light are passed through an output polarizer.



A lithium tantalate modulator uses high-speed electrical pulses from a pulse code modulation (PCM) terminal to modulate an equally fast stream of visible light pulses. After passing through a polarizer, the light pulses enter the lithium tantalate crystal, which acts as a high-speed gate. Two electrodes are plated on opposite rectanglar faces of the crystal. When the PCM terminal sends an electrical pulse (a ONE) to these electrodes, it causes the plane of polarization of the light pulse, then passing through the crystal, to shift 90 degrees. This change allows the light pulse to pass through the analyzer and to be detected by the photodiode. If no electrical pulse (a ZERO) is sent from the PCM terminal, the light pulse passing through the crystal is blocked when it reaches the analyzer and does not register at the photodiode.

DESIGNING COMBINATORIAL AND SEQUENTIAL ADAPTIVE LOGIC NETWORKS

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Synthesis of combinatorial and sequential adaptive logic networks described in this article, uses a technique which partitions the logic into two sub-networks. The first sub-network contains the logic necessary to perform the functions to which the network adapts; the second sub-network is a sequential logic network which controls the adaptive process, and employs binary encoding to minimize the number of memory cells needed. A specific implementation of a memory cell is given to illustrate the application of the technique to network examples.

In the past decade, much theory has been added to the analysis and synthesis of both combinatorial and sequential logic circuitry. The problems of analyzing and synthesizing sequential circuits can be greatly simplified by stating them in terms of combinatorial circuitry and then applying known theoretical approaches. Recently, extensive interest has been shown in adaptive logic circuitry; circuits that possess the ability to "learn" a logical function. Since an adaptive network eventually learns to produce a given logical function or a given sequence of logical functions, it eventually results in either a combinatorial or a sequential circuit; the "learning" process is analogous to the design of the circuit. During the learning process, the network takes the form of a set of sequentially-changing combinatorial circuits, with the performed logical functions varying as the output function is learned.

It would seem reasonable that an adaptive logic network could be synthesized by breaking the network into combinatorial and sequential sub-networks. This done, each sub-network might be designed independently and then the two be put together to form the overall adaptive network. Using this approach, the separation of the network must be made with intent to achieve circuit minimality and simplicity of design of each sub-network. This article presents a method for organizing the sub-networks efficiently. The method allows existing theoretical approaches to be used in the design of both segments of the problem. A sequential memory cell is illustrated which makes the design of either a combinatorial or a sequential adaptive logic network only slightly more difficult than the design of the equivalent non-adaptive circuit.

The Adaptive Technique

An adaptive logic network must consist of both memory elements and combinatorial logic elements; the memory elements are essential to the learning process which the network must perform, and the logic elements are nec-

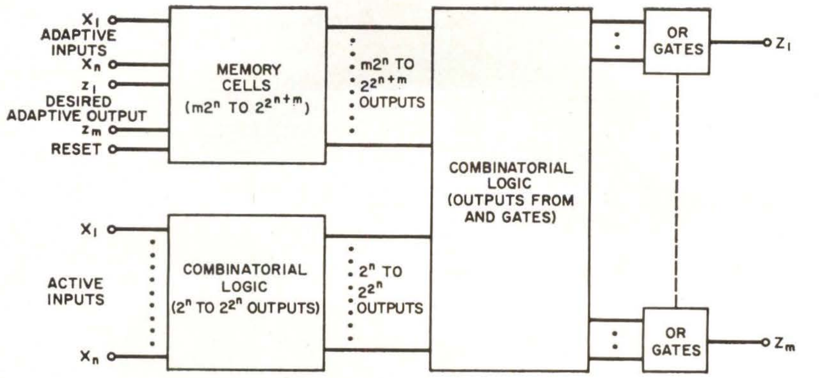

Fig. 1. Generalized multi-output combinatorial adaptive logic network.

essary in analyzing the inputs on the network in relation to the response desired from the network during the learning process. Once this process is complete the logic elements are necessary to produce the learned output from a given input. Since the adaptive network consists of both memory and combinatorial logic elements, it is a network which is in part sequential and in part combinatorial.

The organization of the sequential and combinatorial sub-networks within the adaptive network plays an important part in minimality and simplicity of design which may be achieved. Minimality problems in relatively few input variables become unwieldy even for solution by computer programs if the adaptive network is poorly organized. This is especially true of networks which require every input combination to be considered and/or will produce all possible output functions, and therefore provide no logical redundancy.

Since 2^{2^n} different functions can be created from n input variables, the amount of memory necessary to remember each of these functions becomes prohibitive in any economical design. By coding the 2^{2^n} functions, 2^n memory elements can be used to remember them, thus minimizing the sequential portion of the network. This is equivalent to remembering (or learning) the 2^{2^n} functions represented by the 2^n elements of the n-variable Karnaugh map. If 2^n memory elements are used in the network, the primary inputs (which shall be referred to as $x_1, x_2, \ldots x_n$) must be decoded into the 2^n minterms which can be formed from n variables. Once these functions are formed, the ANDing of the minterms with the associated memory element output (which represents the presence of the minterm in the function the network is trying to learn) will provide an output equivalent to one element of the Karnaugh map, and when all the AND outputs are ORed together, the entire function is formed. The general form of such a network is shown in Fig. 1. The combinatorial logic necessary to generate each of the minterms of interest may be designed using existing minimization techniques.

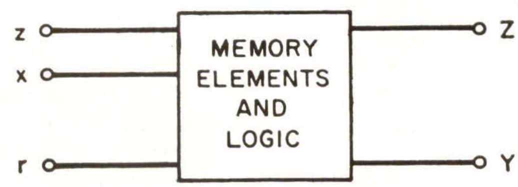

Fig. 2. A typical memory cell.

The Memory Cell

Since each memory cell represents an element of a Karnaugh map, both the input variables which define that element of the map and the desired output from the circuit which is being synthesized must be present on the input to the memory cell. The output from the cell represents the presence of the minterm in the function the network is trying to learn. Therefore, a sequential network must be synthesized which gives an output when a given function of $x_1 \ldots\ldots x_n$ and a given desired output z are both present; once "set," the network must continue to give this output for the same given input function of $x_1 \ldots x_n$.

Fig. 2 shows a typical memory cell with x as the input representing a function of $x_1 \ldots\ldots x_n$, z representing the input which signals a desired output, and r representing clearing or resetting the memory cell. The cell will be "set" when x and z occur simultaneously. It will be "reset" when r occurs. An output Z will be produced from the cell whenever x occurs following the "setting" of the cell (and also upon initial setting of the cell). Straightforward application of sequential circuit theory[1] to the cell description above, and proper choice of the "don't cares" in the matrices result in the "set dominant" circuit implementation shown in Fig. 3. This circuit, if studied carefully, clearly portrays the action of a typical adaptive memory cell.

Initially, the latch portion of the cell is "reset." The cell will be "set" only if x and z are present at the same time, and the combinatorial circuitry on the "set" of the

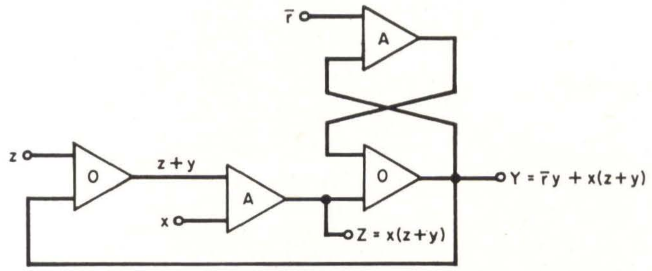

Fig. 3. A set-dominant circuit implementation.

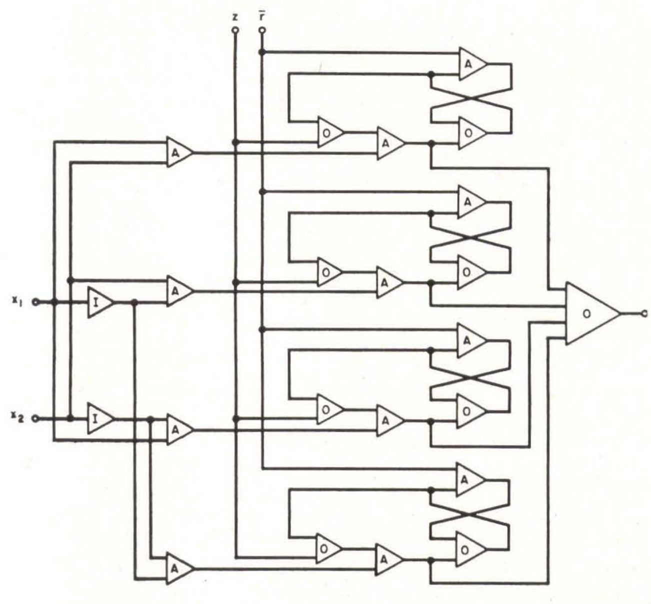

Fig. 4. Two-input adaptive combinatorial network.

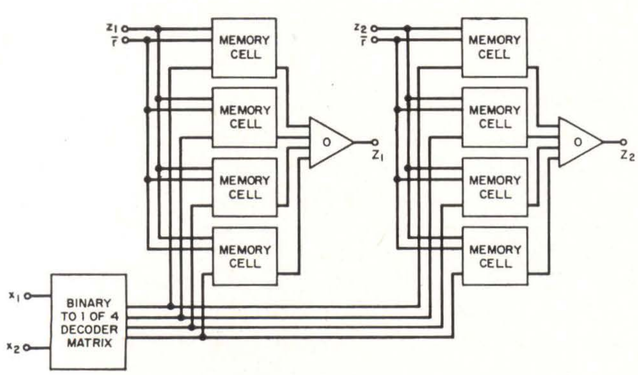

Fig. 5. Two-input, two-output adaptive combinatorial network.

latch serves the dual purpose of initially allowing the latch to be "set" and subsequently providing the desired output of the cell.

Combinatorial Adaptive Network

The input x to the typical memory cell is in no way restricted and may be any decoded Boolean minterm. Therefore, if a memory cell is provided for each of the 2^n input minterms of $x_1 \ldots x_n$, the network is capable of learning any of the possible 2^{2^n} functions of n variables. To implement a functionally-complete combinatorial adaptive network, it is both necessary and sufficient to have available all the minterms of the functions of n variables. A combinatorial circuit, to produce these minterms, would consist of at least 2^n AND gates, since a unique output for each minterm must be available.

Using the 2^n outputs of the combinatorial AND gates as inputs to the 2^n memory cells and ORing the outputs of all the memory cells together completes the network design. The output appears at the output of the final OR circuit. The logic for a two-input network is shown in Fig. 4.

Combinatorial networks with multiple outputs are designed using an extension of the method described in the previous section. For a network with n inputs and m outputs, any one of the 2^{2^n} functions of the input variables may produce any of the m output functions. (For each output function to be unique m must be less than or equal to 2^{2^n}.) Since each minterm must have a cell for every possible desired output, the total number of memory cells needed for a coded implementation of the input functions is:

$$N_T = (2^n)\ (m)$$

To produce the adaptive output, all cells having a particular z_k $(1 \leq k \leq m)$ as an input have their outputs ORed together. The multiple output problem is, in essence, the solution of m single output combinatorial problems. Fig. 5 shows a two-output adaptive network.

Sequential Adaptive Networks

The design of sequential networks is analogous to that of combinatorial networks, once they are separated into combinatorial and sequential portions. For simplicity, it is assumed that the inputs x_1 to x_n are independent with only one input ever present at a time, and that each stable state of the resulting sequential network is represented by one memory cell, and that only one cell at a time is ever set. (This is the form of networks designed using flow table logic.[2,3]) Although these restrictions are not necessary for the application of the following technique, they greatly simplify the organization of the network and the illustration of the approach, just as a minterm implementation did in the combinatorial case. The inputs to the adaptive memory cells of a sequential network are functions of the primary input variables (as they were in the combinatorial case) and also of the present and next desired secondary state of the network. The sequential network must learn a particular sequence of minterms; there are n primary input variables and s secondary states, and from any state s_k the network may

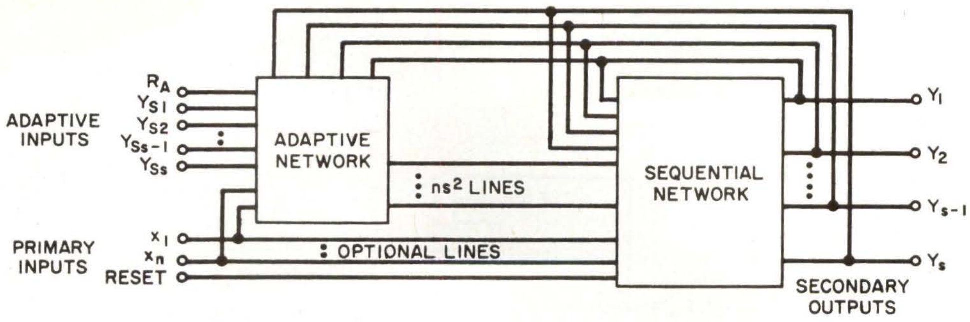

Fig. 6. Generalized n input adaptive sequential circuit.

go to s-1 secondary states. Therefore, the number of adaptive memory cells needed to provide the "sets" for the sequential network is:

$$N_s = ns\,(s - k) = ns^2 - ns$$

Since a unique memory cell is set for each stable state, the previous stable state must be reset; for n inputs and s stable states, the number of possible "resets" is:

$$N_R = ns$$

Therefore, the total number of adaptive memory cells needed to implement the sets and resets for the sequential network is:

$$N_T = N_S + N_R = (ns^2 - ns) + ns = ns^2$$

Fig. 6 shows a general block diagram of an adaptive sequential network. The sequential network block is a set of s memory cells, each of which is set by any one of s-1 lines from the adaptive network and reset by any one of n lines from the adaptive network. A typical memory cell, as shown in Fig. 7, has a reset line and is set by the primary input x_n and the present stable state y_s and the next desired stable state Y_k. The resets for the sequential block are obtained by setting an adaptive cell, which represents a primary input occurring simultaneously with a desired next stable state. Therefore, once the network has adapted itself, the resets are functions of only the primary inputs.

The set lines, however, are functions of both the primary inputs and the present stable states. Using ns AND gates to produce all possible combinations of the n x's and s y's produces one input to the adaptive cells, which produce the sets for the sequential network. The second input needed is the next desired stable state (represented by Y). The outputs of these cells go to the sets of the sequential network.

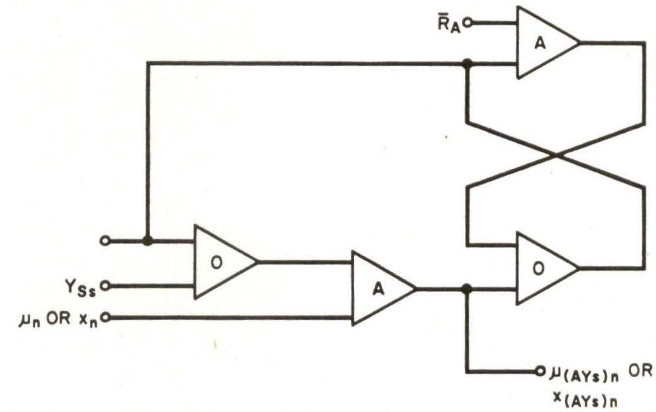

Fig. 7. Adaptive memory cell for sequential network.

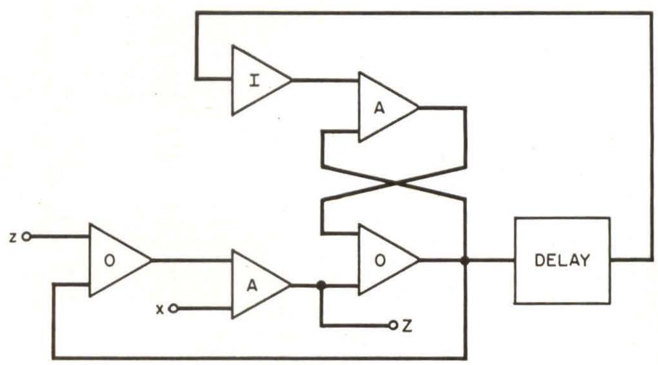

Fig. 8. Single shot type memory cell.

Restrictions And Alternatives

The design approach described in this article was not meant to be restrictive, and may be modified and expanded to handle most adaptive synthesis problems. However, we have imposed several restrictions, and they and the alternatives to them should be discussed.

- The learning process for the networks described in this article was a sequential minterm by minterm process. Up to 2^n inputs are necessary to complete this learning process, depending on the particular function being synthesized. This learning process is serial rather than parallel, and in some applications this would seriously limit the usefulness of the network. However, a parallel decoding network may be employed to generate all minterms of a given function simultaneously, thus allowing the learning process to take place with parallel minterm inputs.
- The design procedure assumes that a minimum of memory cells (2^n cells) are used in the design. In some applications it may be desirable to use more cells (up

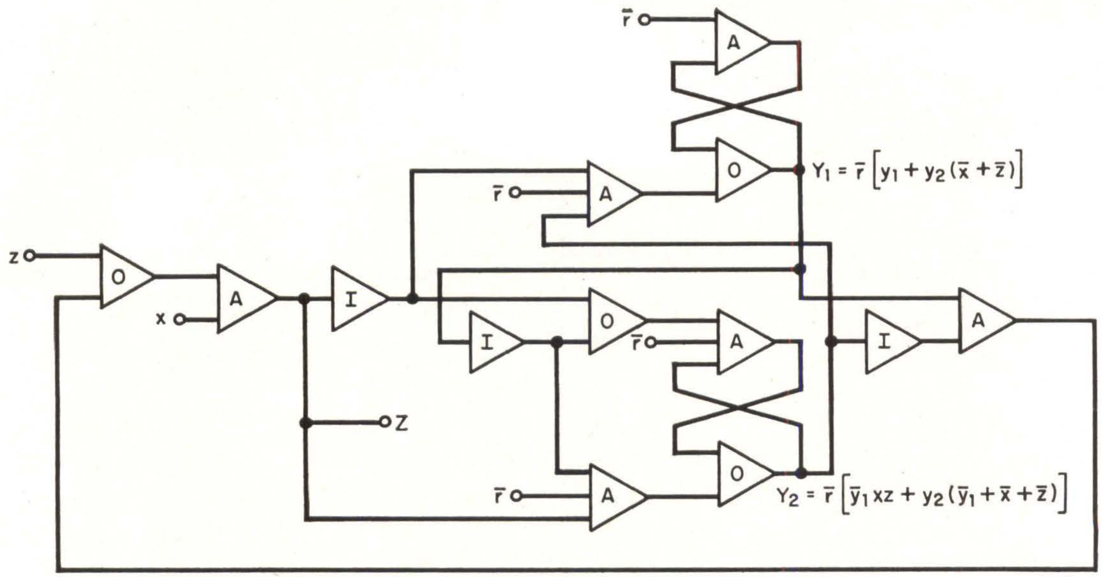

Fig. 9. Counter type memory cell.

to 2^{2^n}). However, the use of only 2^n memory cells is not a true restriction since the input to a memory cell may be any Boolean function. If all 2^{2^n} functions of n variables are available and if 2^{2^n} memory cells are used, the design is reduced to the trivial process of attaching one memory cell to each of the function lines and using the cell outputs as the appropriate learned function output.

• A specific memory cell was designed and used for the applications described in this article. The limitation of the design to a memory cell with fixed properties may be undesirable in certain applications. However, any memory cell with equivalent input-output characteristics may be used. For example, the "single-shot" type cell shown in Fig. 8 learns a function for a fixed period of time and then forgets it. A counter type cell (shown in Fig. 9) has a greater memory capacity than either cell so far described, since it learns a function only after it has been shown the function a given number of times (in Fig. 9, two). Since the design of the memory cell is independent of the adaptive network synthesis, various memory cells may be employed within one adaptive network, to allow certain minterms or functions to be learned more quickly than others.

Comments And Observations

It should be observed that the memory cells presented in this article provide a valid partial output while the network is learning its output function, provide a valid partial output for repeated settings of the same minterm function, and can accumulate additional minterm settings even after the circuit has been producing a useful output.

Knowledge of the characteristics of a particular problem may allow simplifications and reductions in the circuitry provided. If it is known that certain minterms will never appear in any of the output functions of the adaptive network, then the memory cells associated with these minterms may be omitted. If it is known that certain minterms will never appear in the input to the adaptive network, then standard minimization techniques may be employed in implementing the input combinatorial logic. It should, however, be noted that the most generally-useful adaptive network will have no redundancy (that is, it will allow all possible inputs and provide all possible outputs), and, therefore, many designs will be straightforward application of the approach presented.

Because of the learning properties of the networks described in this paper, several interesting applications may be cited:

• A digital synchronization circuit, which under control of the incoming data, allows the synchronization pattern to be varied;

• A correlation circuit for seeking a relation between two logical functions in a network;

• A dynamic logic gate which changes its output function on the basis of incoming signals to the point of resetting all previously-set memory cells and/or inhibiting further setting of memory cells;

• An adaptive pattern recognizer (which has been implemented by Clapper[4]). END

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4. G. L. Clapper, *"An Adaptive Pattern Recognizer,"* IBM Technical Report TR 01.808, General Products Division, Endicott, New York, June 19, 1964.

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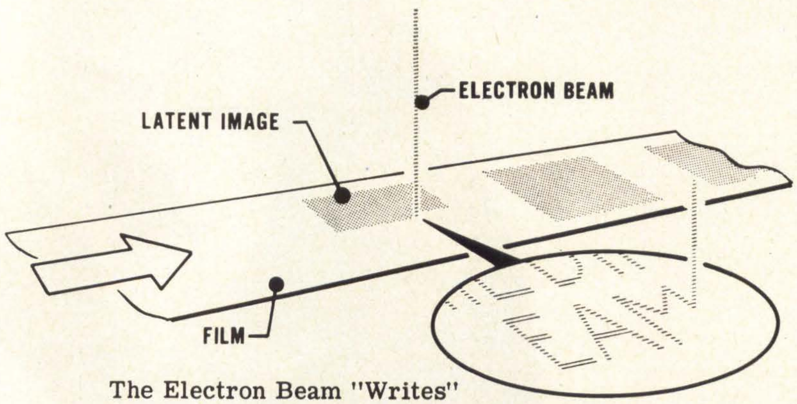
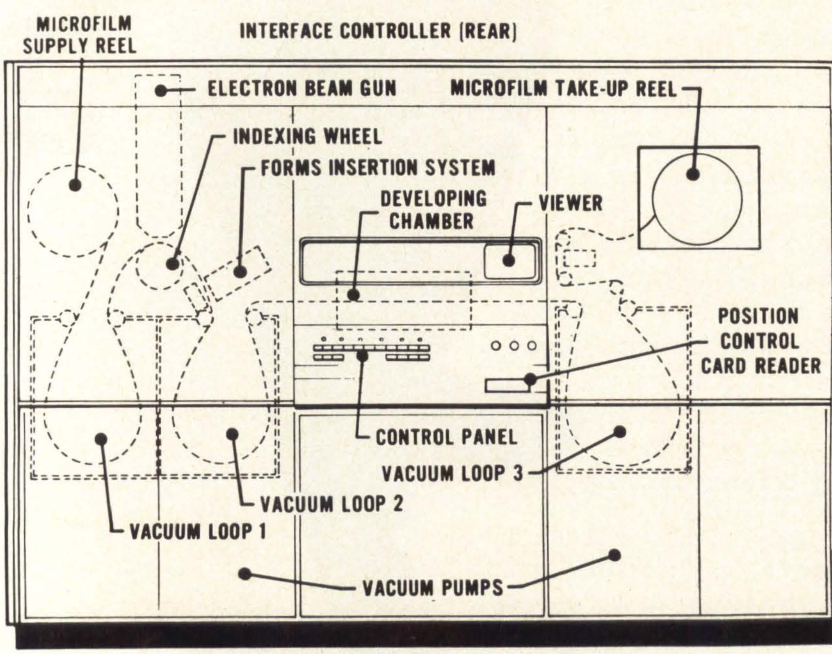
ELECTRON BEAM RECORDING

New Technique Converts Computer Data 25 Times Faster Than Conventional Printers



The Electron Beam "Writes" a Latent Image on Dry-silver Microfilm.

Electron beam "writes" a latent image on dry-silver microfilm in new unit developed by 3M Co. which converts computer generated information into human readable language at speeds of 60,000 characters per second or 30,000 lines per minute. Since the film is developed by heat, it is ready for instant viewing on microfilm reader-printers without the need for a darkroom, chemicals, or other conventional photographic processing equipment.



ELECTRON BEAM RECORDER (EBR)

Details of 3M's new electron beam recorder showing path of dry-silver film from left, proceeding under electron gun where latent images are "written" on the film. Footage is then passed through chamber where film is developed by heat. Viewer permits visual check of film while processing occurs.

By firing electron beams onto a new type of microfilm, an electron beam recorder, developed by 3M Co., will convert computer-generated information into human readable language. Signals from a computer are fired through an electron gun and are written in standard or enlarged symbols at speeds of 60,000 characters per second or 30,000 lines per minute on a dry-silver microfilm. Since the film is developed by heat, it is ready for instant viewing without the need for a darkroom, chemicals, or other conventional photographic processing equipment.

"With this recorder, we are converting machine language into human readable language electronically at fantastic speeds," said Dr. Marshall R. Hatfield, technical director of the 3M Co., Microfilm Products Division. "This system is the result of five years research effort in our laboratories with electron beams, how they can be controlled, and how to image directly with them. The results of our searches indicate the beams have few limitations. We have found they can be squeezed to the size of a micron or 25,000 dots or lines per inch.

"Electronic advances in the computer industry during the past 15 years have been significant," Dr. Hatfield said. "In fact, the speed with which computers handle calculations is so fast that they have outpaced the speed and flexibility of electronics with the latest graphics technology. By combining our research in electron beams with our dry-silver technology, we believe we have developed a system to overcome this problem and will enable computer users to realize the full potential of their equipment.

"In addition," Dr. Hatfield added, "we have designed the system to be compatible with future computers as well as hardware which is available today. The use of microfilm also will enable users to realize considerable cost savings."

A typical electron beam recording system consists of a computer magnetic tape unit, the electron beam recorder itself, a microfilm duplicator, and microfilm viewers or printers at point-of-use locations. Digital information is transferred from the tape unit to the electron beam recorder. In one operation, the electron beam recorder converts the digital language on computer-generated tape into microfilm images.

The electron beam recorder is a self-contained unit which includes control interfacing electronics, a film transport system, an electron beam gun, an automatic random optical forms insertion system, a film developing unit, and a viewer for inspecting the microfilm images. Film is processed within the recorder which keeps pace with the magnetic tape unit supplying the digital information. No buffer is required.

The output of the electron beam recorder is positive-appearing frames of 16mm microfilm in roll form. Output rate is eight frames per second. The film is ready for instant viewing, copying, or duplicating into any of the standard formats.

Dry-silver is a new photographic type emulsion which can be processed and fixed almost instantly with heat and offers resolutions ranging up to 1500 line pairs per millimeter. It is supplied for the system in 12½ inch reels containing 2,400 feet of film with a capacity of 45,000 images.

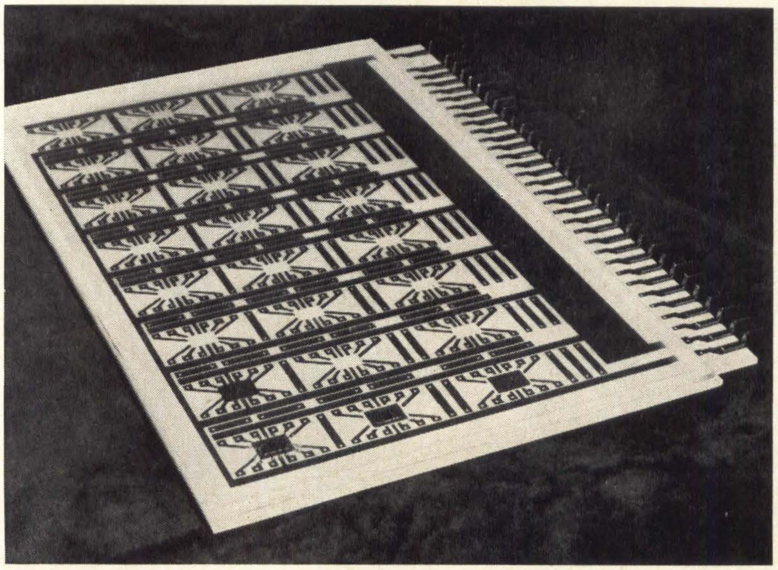
The film is developed in a chamber in which hot air is passed over the microfilm. Electronic-optical controls insure development with consistent quality. A viewer allows the operator to inspect the microfilm frames at random while they are being processed for proper forms insertion, image format, and similar qualities.

The forms insertion feature of the recorder permits the printing of catalogs, maintenance manuals, and similar publications which include a combination of alphanumeric and graphic information. Sales price for the basic unit is $80,000. The unit may be rented for $3,000 per month, which includes a maintenance agreement. A number of optional features will be available and range in purchase price from $1,200 to $15,000. For more information:

Circle No. 106 on Inquiry Card

SMALL-SCALE, LARGE-SCALE INTEGRATION

Twenty-Four IC Chips In a Single Ceramic Package



The Westinghouse interim approach to LSI is like a miniature printed circuit board that neatly carries 24 tiny encased circuit chips (only four in place in this photo, two right-side up and two flipped over). But unlike a printed circuit board, this package is made of ceramic and acts as a protective container for it hermetically seals the chips against the environment by means of a ceramic lid (that isn't shown but would cover top making contact with ridge that is barely visible around the edge).

Terming it an interim approach to large-scale integration (LSI), the Molecular Electronics Division of Westinghouse has put 24 individual integrated-circuit chips into a single ceramic package, about the size of a businessman's calling card. This package not only seals the chips against the environment but carries all the complex wiring needed to connect the chips into a working subsystem.

There are 64 electrical connections coming out of the new package and they are all purposely brought out along one of the long edges. This makes it possible to plug the packages on-edge into larger printed-circuit "motherboards." For the user, this is said to represent a large saving in assembly labor. Only 50 of these LSI packages might be needed for a fair-sized computer and they could all fit onto a roughly one-foot square motherboard. Then one dip of the motherboard into a solder bath would form all the LSI package-to-motherboard electrical circuit connections and the lion's share of the assembly task would be over.

Plugging in the complete LSI packages would be child's play compared to the present tedious soldering or welding of the individual leads of the integrated circuits. For the 50 LSI package example, there would be 50 x 24 = 1,200 individual integrated circuit packages. Each of these integrated circuits would probably have 14 leads so the total number of joints that the user would have to make without LSI would be 1,200 x 14 = 16,800. A mistake in any one of these joints might ruin the whole circuit. The user can obtain the LSI packages complete and tested from Westinghouse.

The multi-chip package uses an alumina ceramic substrate as its main structural member. The 24 integrated circuit chips are fastened to one side and as many layers of metal circuit patterns built up on the other side as are necessary to interconnect the 24 chips into a complete, self-contained working subsystem. Westinghouse is able to use several methods to attach the circuit leads to the chips. It can put the chips face up on the substrate and use conventional wire bonding connection methods, or it can flip the chips face down on the substrate and use either solder dot or beam lead connections. Westinghouse says it will start with the familiar wire bonding attachments and then progressively phase into the new solder dot and beam lead methods as it is proved that these newer methods can be reliably accomplished in regular production.

The metal interconnection patterns on the opposite side from the chips are applied either by evaporative deposition techniques (thin-film processes) or silk-screened and fired on thick metallic films. The metal films would be separated by fired-on ceramic layers. Naturally, says Westinghouse, the interconnection patterns would be varied for different applications and could be customized to suit the system needs of particular customers.

Connections from the chip side to the wiring side are made by plated-through holes going through the ceramic substrate. These plated-through holes are also the means for achieving wiring crossovers and there are a number of short circuit runs on the chip side of the substrate for just this purpose.

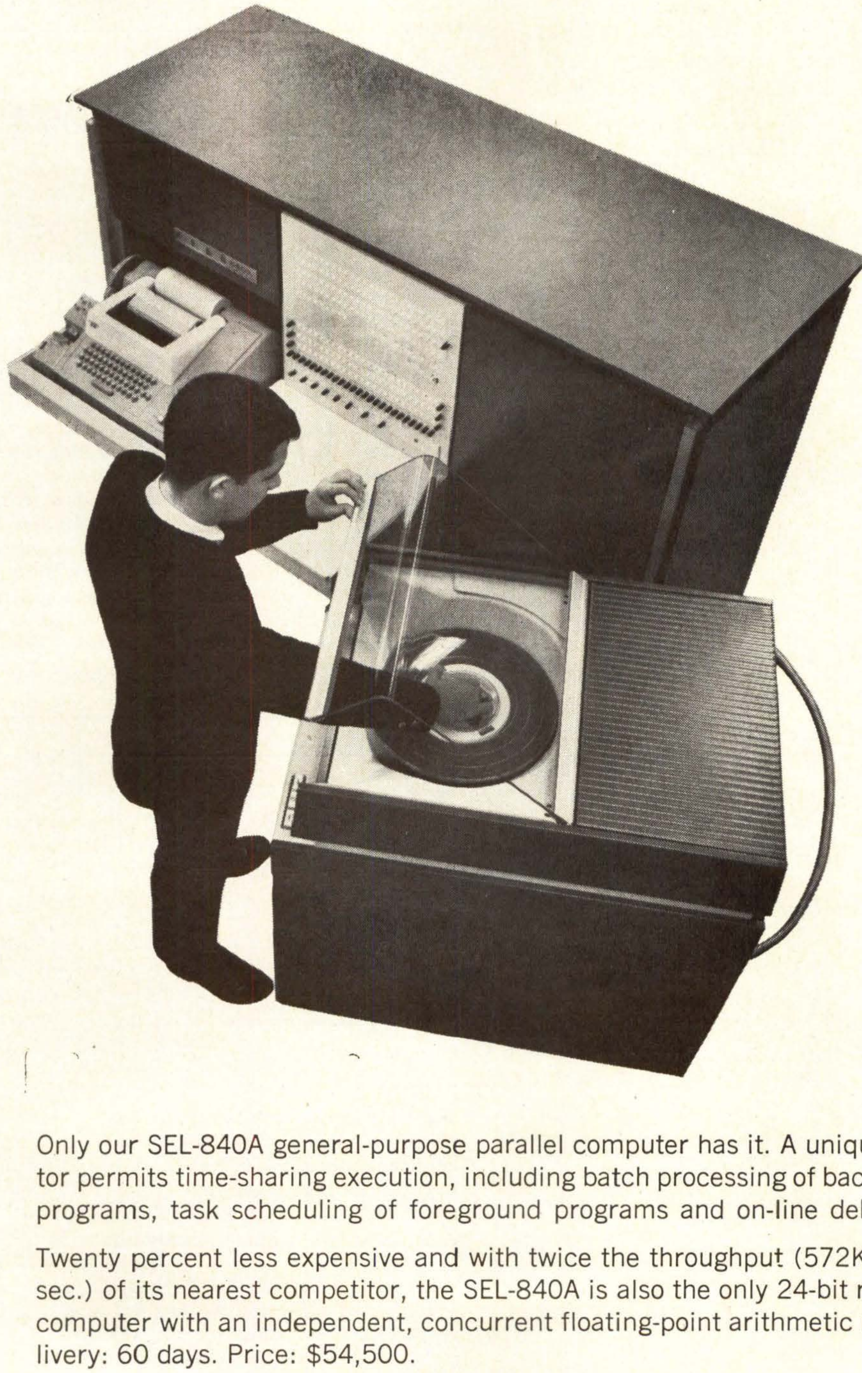
The chips are protected by either one large ceramic lid that hermetically seals them all or by smaller lids that cover the chips individually. The advantage of the individual lid for each chip approach is that the individual chips can be replaced after the package is finished — a feature that should appeal to industrial users who like inexpensively repairable systems.

All-in-all, the package might be considered a ceramic version of a multiple-layer printed circuit board, such as the types that are now being used to carry complex assemblies of integrated circuits. However, the ceramic LSI package is said to be more rugged and compact than an equivalent circuit board.

For more information:

Circle No. 102 on Inquiry Card

The first real real-time monitor for a 24-bit computer.



Only our SEL-840A general-purpose parallel computer has it. A unique monitor permits time-sharing execution, including batch processing of background programs, task scheduling of foreground programs and on-line debugging.

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For further information, write for BULLETIN 9056A, or contact Systems Engineering Laboratories, Inc., 6901 West Sunrise Blvd., Fort Lauderdale, Fla. 33310. Area Code 305-587-2900. Offices also in Washington, D.C.; Los Angeles, California; Boston, Massachusetts; San Francisco, California; Cleveland, Ohio; Houston, Texas; Huntsville, Alabama; and Orlando, Florida.

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CIRCLE NO. 35 ON INQUIRY CARD

EXPERIMENTAL SUPERCONDUCTING LOGIC ELEMENT SWITCHES FASTER THAN A CRYOTRON

R & D Report

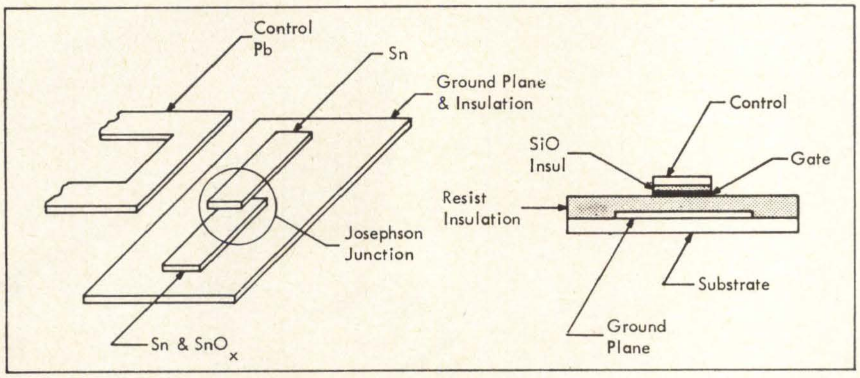
Described in the current Proceedings of the IEEE by Juri Matisoo, of IBM's Research Division, a new superconducting device differs from a cryotron in that it is never in the normal state. It switches in less than 800 picoseconds (the limit of resolution of Matisoo's measurements). Switching is probably much faster than this. More important, calculations indicate that, after switching, it can transfer current from one path to another in 80 to 200 picoseconds, depending on the materials used. Processes inherent in switching a cryotron between the normal and superconducting states had limited its switching speed to 20 or 30 nanoseconds under reasonable operating conditions. The new device avoids this limitation since it remains superconducting at all times.

The new superconducting element takes advantage of the fact that two different types of electron tunneling can occur through a thin insulating barrier separating two superconducting metals. In one form of tunneling, single electrons pass through the barrier with a voltage drop corresponding to the energy required to break up the electron pairs characteristic of superconductivity. This type of tunneling has been known for some time.

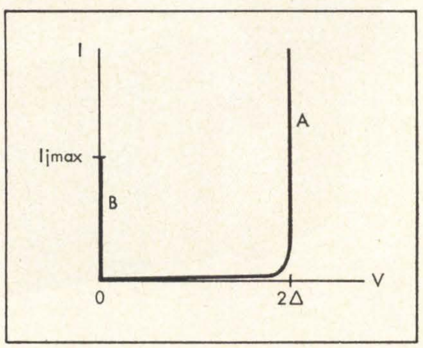
A second type of tunneling was predicted theoretically by B. D. Josephson, of Cambridge University, in 1962, and was observed shortly thereafter. In Josephson tunneling, paired electrons flow through an ultra-thin insulating barrier with no voltage drop, just as if the insulator itself were a superconductor. Josephson tunneling is extremely sensitive to a magnetic field in the plane of the insulator.

The switching device described by Matisoo consists of two metal films separated by an oxide layer 10 to 30 Angstroms thick. Above the metal films, and insulated from them, is a control film through which a current can be passed to generate a magnetic field in the plane of the device. The device works as follows. A current of up to about 30 milliamps will flow across the insulator by Josephson tunneling with no voltage drop. If a magnetic field of about one-half gauss is then generated by a current in the control line, the Josephson tunneling is quenched. But a single-electron tunneling process is available at a voltage corresponding to the energy required to break apart the electron pairs (about 1 mv for Sn-Sn junctions, 2.5 mv for Pb-Pb). If the current is held constant, the device switches to this mode.

If a second path is available to the current, such as another device in parallel with the first, the voltage across the first device will drive the current into the alternate path. This is a unique characteristic of the device; after switching, the current does not decay by an L/R time constant, but rather is driven into a new path by a voltage which is very nearly constant during the entire current transfer period. The effect is exactly the same as if a battery had been inserted in place of the first device. The time required for current transfer is calculated to be 200 picoseconds for Sn-Sn junctions which have a single electron tunneling voltage of 1 mv, and 80 picoseconds for Pb-Pb with 2.5 mv. END



The new superconducting logic element, reported by IBM, takes advantage of the two types of electron tunneling that can occur through an ultra-thin insulating layer separating two superconductors. The junction is fabricated by depositing a film of metal allowing a thin oxide layer to form on it, then depositing a second film of metal on top of the oxide. Above the junction is another metal film through which a current can be passed to generate a magnetic field in the plane of the junction. When this control film is pulsed, its magnetic field quenches the paired-electron (Josephson) tunneling through the junction. The junction then switches to single-electron tunneling in which a voltage appears across the junction. This voltage tends to drive the current into another path if one is available.



The current-voltage characteristics of the two types of tunneling that can occur through a thin-insulating barrier between two superconductors is shown here. Curve A is for single-electron tunneling. No current flows until the voltage provides enough energy to raise electrons to an excited state corresponding to breaking up the pairs of electrons characteristic of the superconducting state. In contrast, curve B shows Josephson tunneling in which paired electrons tunnel through the insulator with no voltage drop. The insulator thus behaves as a superconductor itself.

The new, small DECdisk provides 32K words extra memory for the PDP-8 for $6,000. Additional 32K DECdisk units cost $3,000 each. Since a basic $18,000 PDP-8 computer has 4096 words in core, with four DECdisk units, that could give you a high speed computer with 135,168 12 bit words for $33,000!

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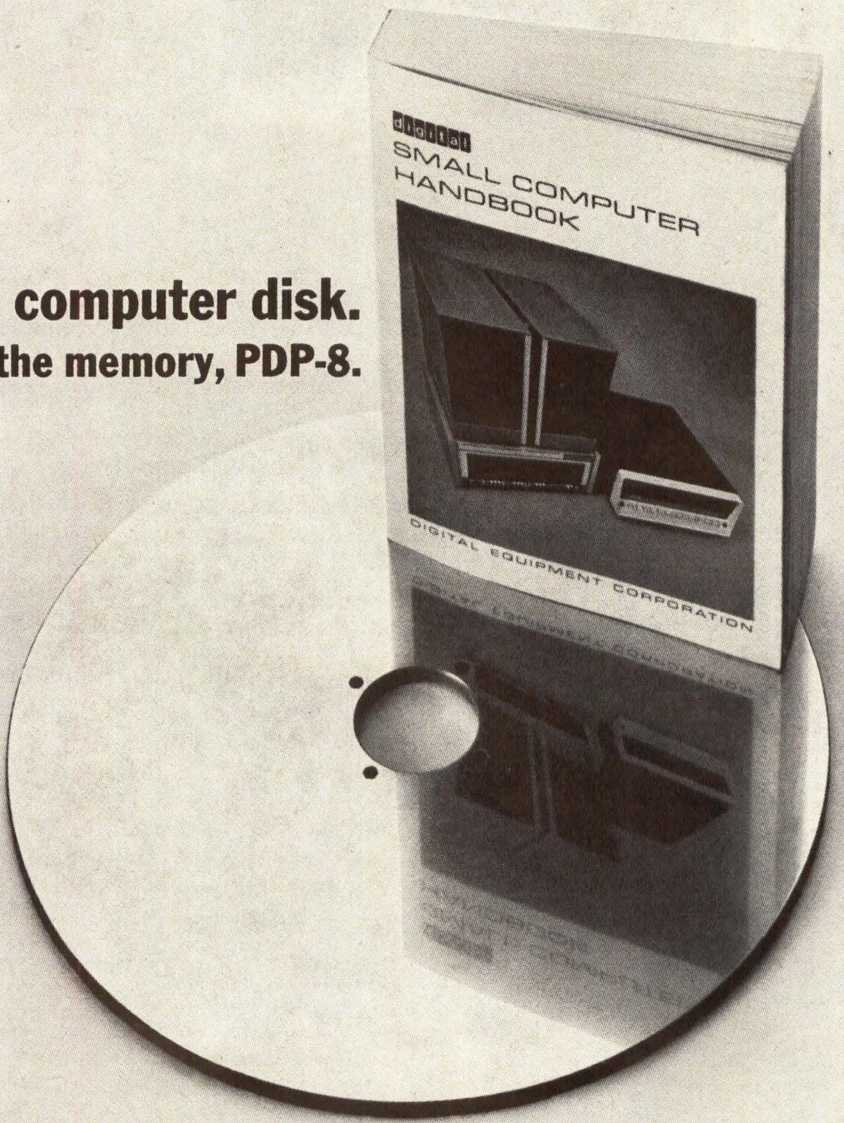

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negative radix arithmetic

M. P. deRegt

In last month's issue, Part 1 introduced the notion of using a negative number as a radix, and illustrated the representation of numbers and the arithmetic using a base of -10. The rules of arithmetic in this system were explained by means of a special decimal system in which the negative numerals -1, -2, -3, . . . , -9, were used for odd positions (positions in which the radix exponent is odd), and the normal numerals were used in even positions. We also speculated on how the properties of negative-radix scales of notation might be exploited in computer systems.

Here in Part 2, we shall concentrate on the number representation aspects of negative radix notation. It was mentioned in the first article that the operational aspects were of much greater importance than the representational, however, the representational aspects are the first which strike the individual when considering the possible advantages of negative radix notation. (In fact, a common reaction is that one bit per word will be saved, since the sign bit is eliminated. This is not true, of course, since N positions of **any** two-symbol number system will permit 2^N different combinations of the two symbols. If $N = 12$, 4096 different combinations exist, and these combinations may be defined to be the integers from 0 to 4095; they may be defined to be the negative and positive integers from -2047 to $+2047$, with two representations for zero; they may be defined to represent fractions.) We will examine certain conventions as they apply specifically to negative radix notation, present descriptions and properties of systems for representing integers and fractions, and examine various number systems in which the numerals are represented by negative binary codes.

Terminology & Conventions

Any negative radix could be used to illustrate a discussion on the representation of numbers using negative radix notation. However, following the example set in the first article, negative decimal will be the system upon which most of the emphasis will be placed. This emphasis results from our objective of achieving familiarity with the notation and the arithmetic, which is best done through development of manual, rather than machine, algorithms. In negative decimal, all of the normal decimal symbols, rules, tables, and conventions apply except that the sign of a carry is changed; negative binary is a sort of special case, and generalities may be more easily illustrated in a system having more than two numerals.

We will be speaking extensively of negative and positive numbers with negative and positive radices. This could lead to awkward terminology, such as speaking of a negative number in negative decimal as a "negative negative decimal" number, and it is essential to coin some names for these negative radix systems. We shall use the following:

-2 Negabinary
-3 Negaternary
-4 Negaquarternary
-8 Negoctonary (Negoctal)
-10 Negadenary (Negadecimal)
-16 Negahexadenary (Negahexadecimal).

The names binary, octal, decimal, etc., will continue to refer to $+2$, $+8$, $+10$ base systems. The words **negaradix** and **posiradix** will be used to refer to numbers of either polarity expressed in negative radix systems and positive radix systems, respectively.

PART 2

Negative Radix Representation

Editor's Note: Last month's issue introduced the concept of negative radix number systems and put forth the advantages of designing digital systems based on a negative radix system. Here, in part 2, the terminology, conventions, and properties of negative radix systems are described and illustrated.

The words "digit," "numeral," "number," and "quantity" have overlaps of common and technical meaning. In order to make meanings immediately clear, **digit** will be used to indicate one of a set of n symbols comprising a **number** whose radix is r. **Numeral** will be used to indicate one of a set of $|r|$ symbols used in a scale of notation whose radix is r. The words **quantity** or **amount** will frequently be used in the place of "number" to reduce the confusion which arises when "number" is used for two different meanings in the same paragraph.

REPRESENTATION OF INTEGERS

Referring to the polynomial which defines positional notation (see Part 1, last month), the most significant nonzero digit in an n digit integer was defined as a_{n-1}, the coefficient of the term $a_{n-1}r^{n-1}$. Assuming all $a > 0$ and $r < -1$, this term will be negative for even n and positive for odd n. Since the magnitude of this term must be greater than the sum of the magnitudes of all the lower order terms, it can be said that **a negative radix number having an even number of digits is negative, and one having an odd number of digits is positive.**

The counting exercise of the first article suggested that the distribution of negative and positive numbers for a given quantity of digit positions might not be symmetrical, and this is indeed the case. Let us consider negadecimal integers. For one digit position, we have ten possible representations: zero, and the numerals 1 through 9, that is, zero and nine positive numbers. The lower limit in this set is zero; the upper limit nine. For two positions, we have one hundred representations; the ten formed by one digit, and ninety more, which are the negative numbers 19 (-1) through 90 (-90). The upper limit is still nine; the lower limit is now -90. Table 1 shows the upper and lower limits in decimal for each of the given quantities of positions. Negadecimal representations are identical, with the signs dropped. The pattern of alternating zeroes and nines for the upper and lower limits is easily explained by reference to the polynomial. Because even positions (even powers 0, 2, 4, etc.) have positive values and odd positions (odd powers 1, 3, 5, etc.) have negative values, a number having 9's in even positions and zeroes in odd positions has the maximum value for the word size. Similarly, when the 9's are in the odd positions and zeroes in the even, the number has the minimum value for the word size.

Analogous numbers may be formed for any negative radix system having the numerals $0, 1, \ldots, |r|-1$. If

negative radix arithmetic

continued

$|r|$ is represented by R, then the upper and lower limits for a number having n positions are as follows:

n is even

$$A_{UL} = (R-1)r^{n-2} + (R-1)r^{n-4} + \ldots + (R-1) = \frac{R^n - 1}{R+1}$$

$$A_{LL} = (R-1)\,r^{n-1} + (R-1)r^{n-3} + \ldots + (R-1)r = -\frac{R(R^n-1)}{R+1}$$

n is odd

$$A_{UL} = (R-1)r^{n-1} + (R-1)r^{n-3} + \ldots + (R-1) = \frac{R^{n+1}-1}{R+1}$$

$$A_{LL} = (R-1)r^{n-2} + (R-1)r^{n-4} + \ldots + (R-1)r = -\frac{R(R^{n-1}-1)}{R+1}$$

A decrease in a coefficient from $(R-1)$ will decrease the magnitude of A, and an increase from zero in the coefficient of a missing term will also decrease the magnitude. If these expressions for the limits are applied to negabinary, we will have limit values as shown in Table 2. The numbers in Tables 1 and 2 that start with zero correspond to the series that start with $(R-1)r^{n-2}$, in which the r^{n-1} term has a zero coefficient. The distribution of the four-digit negabinary integers is illustrated in Table 3.

REPRESENTATION OF FRACTIONS

Fractional values may also be represented to any desired degree of precision by a descending power series. To find the limiting values of the limits of the range of values which may be represented, the infinite series comprising the non-zero terms are summed, as follows:

$$A_{UL} = (R-1)r^{-2} + (R-1)r^{-4} + (R-1)r^{-6} + \ldots = \frac{1}{R+1}$$

$$A_{LL} = (R-1)r^{-1} + (R-1)r^{-3} + (R-1)r^{-5} + \ldots = -\frac{R}{R+1}$$

As in normal notation, the range of numbers which can be represented is independent of the number of digits, and depends only on the radix. The number of digits affects only the precision with which numbers within the range can be represented. For negadecimal, the resulting range (expressed in normal decimal) is:

$$+\frac{1}{11} > A > -\frac{10}{11}$$

and for negabinary it is:

$$+\frac{1}{3} > A > -\frac{2}{3}$$

The proper fractions which lie outside of these ranges are represented by numbers with digits to the left of the radix point. If unity is added to the positive limit, and subtracted from the negative limit, the corresponding number ranges clearly include all proper fractions of both polarities:

$$\text{negadecimal: } +\frac{12}{11} > A > -\frac{21}{11}$$

$$\text{negabinary: } +\frac{4}{3} > A > -\frac{5}{3}$$

The two strings of alternating zeroes and nines (or zeroes and ones for negabinary) may be regarded as special number forms. For radix r and numerals zero to $R-1$, the alternating digits are zero and $R-1$. If we add to these two special number forms, a third one comprising a string of digits $R-1$ to the right of the radix point, and a fourth comprising a string of zeroes, and then add and subtract unity to each of these four special forms, we will have a total of twelve repeating proper and improper radix fractions. Table 4 is a table of the resulting representations for negabinary, in which the representations have been arranged in decreasing order of value.

The limiting values for these radix fractions, presented in Column 1 of Table 4, cannot be represented by a finite number of terms; they represent the sums of infinite geometric progressions. The difference between each of these limiting values and the sum of the first m fractional terms of the geometric progression are given in Columns 3 and 4. These increments are given as fractions of Δ a, which is $1/(R+1)$ of the weight of the least significant digit, r^{-m}. For negabinary, therefore, $\Delta\ a = 1/3(-2)^m$. The first fractional terms of each geometric progression are represented by the repeating radix fractions given in Column 2. If we truncate the repeating radix fractions to four positions to the right

TABLE 1

Limits for n Nega decimal Digit Positions

n	Lower Limit	Upper Limit
1	0	+9
2	−90	+09
3	−090	+909
4	−9,090	+0,909
5	−09,090	+90,909
6	−909,090	+090,909

TABLE 2

Upper and Lower Limits for n Negabinary Digit Positions

	NEGABINARY NUMBERS		DECIMAL VALUES	
n	Lower	Upper	Lower	Upper
1	0	1	0	+1
2	10	01	−2	+1
3	010	101	−2	+5
4	1 010	0 101	−10	+5
5	01 010	10 101	−10	+21
6	101 010	010 101	−42	+21
7	0 101 010	1 010 101	−42	+85
8	10 101 010	01 010 101	−170	+85

of the radix point, then the increments $-\Delta a$, 0, Δa, and $2\Delta a$ (in Column 3, for even m) will have values, respectively, of $-1/48$, 0, $+1/48$, and $+1/24$. These increments may be added to the decimal-limiting values to obtain the true decimal value of the repeating negabinary fraction truncated to four places. Examples are:

$$0.0101 = +1/3 - \Delta a = +1/3 - 1/48 = +5/16$$
$$0.1111 = -1/3 + \Delta a = -1/3 + 1/48 = -5/16$$
$$00.1010 = -2/3 + \Delta a = -2/3 + 1/24 = -5/8$$
$$11.0101 = -2/3 - \Delta a = -2/3 - 1/48 = -11/16$$

An interesting and important property revealed by Table 4 and the last two examples is the fact that the upper and lower limits in each box have limiting values identical to those in the adjoining boxes, are complements on $R-1$ in radix fraction form, and have a difference of r^{-m} in truncated form. An attempt to generate a number whose less significant portion has a value in the neighborhood of a limiting value could result in either one of two correct negative radix representations. This fact is of extreme importance in negative radix division operations, as will be seen in a later article. For example, the result of dividing 0.0010 $(-1/8)$ by 0.0111 $(+3/16)$ is the representation for $-2/3$, which lies between $-5/8$ and $-11/16$. If this division in negabinary is carried to only four places, then either of two quotients could correctly be obtained: 0.1010 or 11.0101.

Table 4 also illustrates the form of combined integral and fractional parts required to represent the full range of fractions. The analogous table for negadecimal is readily worked out.

OTHER NEGARADIX SYSTEMS

If the digits of a number expressed in negabinary are grouped in pairs, triplets, or higher quantity groups, the result can be considered to be the same number expressed in a higher radix, with the numerals represented by the possible bit configurations. In positive octal notation, for example, the 3-bit binary groups ranging from 000 to 111 represent the digits 0 through 7. If this same procedure is followed for 2-bit, 3-bit, and 4-bit negabinary groups, we have the sets of coded numerals as shown in Table 5.

The radices of the systems shown in Table 5 would be $(-2)^2$, $(-2)^3$, and $(-2)^4$ respectively, or quarternary, negoctal, and hexadecimal. However, as we have learned to expect in negaradix systems, these systems do not have the normal range of numerals progressing up from zero, but include numerals with negative values. The basis for this is quickly demonstrated for negoctal by reference to the polynomial, with its terms grouped into triplets. Each triplet will have the form:

$$\ldots + [a_{3i+2}\,(-2)^{3i+2} + a_{3i+1}\,(-2)^{3i+1} + a_{3i}\,(-2)^{3i}] + \ldots$$

This group may be rearranged to:

$$\ldots + [a_{3i+2}\,(-2)^2 + a_{3i+1}\,(-2) + a_{3i}]\,(-2)^{3i} + \ldots$$

or:

$$\ldots + (4a_{3i+2} - 2a_{3i+1} + a_{3i})\,(-8)^i + \ldots$$

In this form, the terms in the parentheses comprise the general expression for the values of the eight numerals of a negoctal system. By assigning all of the possible combinations of values (of 0 and 1) to the a's, we have the lower set of eight codes and decimal values of Table 5.

When the grouping comprises an even number of terms, the power of (-2) taken outside of the brackets is even, hence the radix is positive. We then have a positive-radix system whose numerals are symbolized by negabinary codes and have appropriate values, both negative and positive.

Although such codes for radices which are integral powers of (-2) are quite natural, other sets of numerals can be used and the radices need not be confined to integral powers of -2. Some of these, including decimal, are discussed below.

The Cobinary System

This introduction of the concept of numerals of negative value (called "signed digits") leads to the possibility of a system whose radix is -2 and whose numerals have

TABLE 3

Decimal Distribution of the Four-Digit Negabinary Integers

Negabinary Number	DECIMAL EQUIVALENT															
	Negative											Positive				
	10	9	8	7	6	5	4	3	2	1	0	1	2	3	4	5
0	–	–	–	–	–	–	–	–	–	–	X	–	–	–	–	–
1	–	–	–	–	–	–	–	–	–	–	–	X	–	–	–	–
10	–	–	–	–	–	–	–	–	X	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–	–	X	–	–	–	–	–	–
100	–	–	–	–	–	–	–	–	–	–	–	–	–	–	X	–
101	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	X
110	–	–	–	–	–	–	–	–	–	–	–	–	X	–	–	–
111	–	–	–	–	–	–	–	–	–	–	–	–	–	X	–	–
1000	–	–	X	–	–	–	–	–	–	–	–	–	–	–	–	–
1001	–	–	–	X	–	–	–	–	–	–	–	–	–	–	–	–
1010	X	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
1011	–	X	–	–	–	–	–	–	–	–	–	–	–	–	–	–
1100	–	–	–	–	–	–	X	–	–	–	–	–	–	–	–	–
1101	–	–	–	–	–	–	–	X	–	–	–	–	–	–	–	–
1110	–	–	–	–	X	–	–	–	–	–	–	–	–	–	–	–
1111	–	–	–	–	–	X	–	–	–	–	–	–	–	–	–	–

TABLE 4

Negabinary Repeating Radix Fraction

	Special Number Forms		Increments to obtain true limits for m digits $\Delta a = 1/3\,(-2)^m$	
	Limiting Decimal Value	Repeating Radix Fraction	Even m	Odd m
	+4/3	1.0101. . .	$-\Delta a$	$2\Delta a$
←Full proper fraction range→	+1	1.0000. . .	0	0
	+2/3	1.1111. . .	Δa	Δa
	+1/3	1.1010. . .	$2\Delta a$	$-\Delta a$
	+1/3	0.0101. . .	$-\Delta a$	$2\Delta a$
	0	0.0000. . .	0	0
	−1/3	00.1111. . .	Δa	Δa
	−2/3	00.1010. . .	$2\Delta a$	$-\Delta a$
	−2/3	11.0101. . .	$-\Delta a$	$2\Delta a$
	−1	11.0000. . .	0	0
	−4/3	11.1111. . .	Δa	Δa
	−5/3	11.1010. . .	$2\Delta a$	$-\Delta a$

the values 0 and -1. (Since the numeral -1 will be frequently used, it will be convenient to establish a separate symbol for it, and the letter N will be used.) The system of radix -2 using symbols $(0, N)$ could be called a second negabinary system, simply because of its radix, but will be more convenient to give it a separate name, since the two sets of digits (0,1) and $(0, N)$ are the only practicable non-redundant numeral sets. It will be called cobinary — which is short for complementary binary — since both the radix and the non-zero digit are complemented relative to binary. Table 6 is an expansion of Table 5 to include cobinary.

Although negabinary and cobinary appear to be merely complementary ways of representing numbers, a fundamental difference appears in the multiplication operation. The range for proper radix fractions in negabinary is:

$$+\frac{1}{3} > A_{neg} > -\frac{2}{3}.$$

Because identical number configurations in negabinary and cobinary have opposite polarities, the limits of the range for proper fractions have opposite signs, and for cobinary the range is:

$$+\frac{2}{3} > A_{cob} > -\frac{1}{3}.$$

If we multiply two proper fractions, then the lower and upper limits of the product for negabinary are:

$$\left\{AB\right\}_{LL} = \left(\frac{1}{3}\right)\left(-\frac{2}{3}\right) = -\frac{2}{9}$$

$$\left\{AB\right\}_{UL} = \left(-\frac{2}{3}\right)\left(-\frac{2}{3}\right) = +\frac{4}{9}$$

and for cobinary they are:

$$\left\{AB\right\}_{LL} = \left(+\frac{2}{3}\right)\left(-\frac{1}{3}\right) = -\frac{2}{9}$$

$$\left\{AB\right\}_{UL} = \left(+\frac{2}{3}\right)\left(+\frac{2}{3}\right) = +\frac{4}{9}$$

Thus, the limiting values for a product of two proper radix fractions are the same for negabinary and for cobinary.

The fundamental difference comes in when these product limits are compared with those for a proper radix fraction. For both negabinary and cobinary it is seen that lower product limit, $-\frac{2}{9}$, lies within the lower proper fraction limit, which is $-\frac{2}{3}$ for negabinary and $-\frac{1}{3}$ for cobinary. However, only for cobinary does the upper product limit of $+\frac{4}{9}$ lie within the upper proper fraction limit, which is $+\frac{1}{3}$ for negabinary and $+\frac{2}{3}$ for cobinary. This implies that **overflow in multiplication is possible in negabinary, but not in cobinary.**

Conversion between negabinary and cobinary is readily accomplished. One method is to write down the representation for the number of opposite polarity and exchange 1's and N's, which is equivalent to subtracting the number from zero, and then changing the polarity (or vice versa). (Note that in negative radix arithmetic, subtraction from zero is not a trivial operation.) For example:

$$\begin{array}{r} 0\,0\,0\,0\,0\,0\,0 \\ -1\,1\,0\,1\,0\,1\,1 \\ \hline 0\,1\,1\,1\,0\,0\,1 \\ N N N 0\,0 N \end{array} \qquad \begin{array}{r} 0\,0 \\ -\,(+\,2\,3) \\ \hline -\,2\,3 \\ +\,2\,3 \end{array}$$

TABLE 5

Bit Groupings to Form Higher-Radix Systems

Negabinary Code		Decimal Value
1 0 1 0		−10
1 0 1 1		−9
1 0 0 0		−8
1 0 0 1		−7
1 1 1 0		−6
1 1 1 1	Hexadecimal	−5
1 1 0 0		−4
1 1 0 1		−3
0 0 1 0		−2
0 0 1 1	Quarternary	−1
0 0 0 0		0
0 0 0 1		+1
0 1 1 0		+2
0 1 1 1	Negoctal	+3
0 1 0 0		+4
0 1 0 1		+5

TABLE 6

Decimal Equivalents of Negabinary and Cobinary

Negabinary	Decimal	Cobinary
1010	−10	NNNNO
1011	−9	NNOON
1000	−8	NNOOO
1001	−7	NNONN
1110	−6	NNONO
1111	−5	NON
1100	−4	NOO
1101	−3	NNN
10	−2	NNO
11	−1	N
0	0	O
1	+1	NN
110	+2	NO
111	+3	NNON
100	+4	NNOO
101	+5	NNNN
11010	+6	NNNO
11011	+7	NOON
11000	+8	NONO
11001	+9	NONN
11110	+10	NOOO

negative radix arithmetic

continued

A Symmetrical Ternary System

A symmetrical ternary (base $+3$) system using numerals *N*, 0, and 1 has certain advantages. These include an average truncation error of zero, simple arithmetic, elimination of polarity symbols, and the theoretical high storage efficiency of base 3 data. These three symbols could also be used for base -3 (although the utility of this is questionable), base $+2$ (which has been discussed) and base -2 (where it has advantages in division, because the quotient may be generated in any scale of notation).

Although representation in a system using redundant digits is not unique, there is a special case of representing base ± 2 numbers uniquely with the symmetrical ternary numerals. In base -2 systems, this unique representation is obtained by proceeding from the radix point, and replacing digit pairs 11 with 0*N* or *NN* with 01. The result is a representation which contains a minimum number of 1's and *N*'s, and which may be useful for minimizing time for such operations as multiplication and division.

Comparison of the procedures for obtaining such a representation for normal base $+2$ and -2 systems will show the latter to be much simpler, because no carry or borrow is propagated. In the $+2$ system, the digit pair 11 is equivalent to the triplet 10*N*, so that it is replaced by 0*N*, with the "1" carried into the next higher position. For example, converting $+10111$ $(+23)$ to the symmetrical (base $+2$) notation,

$$\begin{array}{rcr}
+00011 & = & +0010N \\
+00100 & = & +00100 \\ \hline
+00111 & = & +0100N \\
+10000 & = & +10000 \\ \hline
+10111 & = & +1100N \\
 & = & +10N00N
\end{array}$$

For negabinary and cobinary 1101011 $(+23)$ and *NNN*00*N* $(+23)$, respectively, the conversions are made easily: *N*0100*N* and *N*0100*N*. Naturally, they are identical. There are clear implications of advantages over binary for high speed multiplication and division.

Use of this notation offers a method of conversion between binary and negabinary (or cobinary). For conversion to base -2, convert the normal binary form to the symmetrical form. Then change all non-zero digits in **odd** positions to the opposite polarity — that is, 1's to *N*'s and *N*'s to 1's. The result is the base -2 symmetrical form for the number. Then change 0*N* to 11 for negabinary, or 01 to *NN* for cobinary. Reverse the process for conversion the other way.

Examples:

1) Convert $+1011101$ from binary to symmetrical binary

$$\begin{array}{rcr}
+0001101 & = & 10N01 \\
+1010000 & = & +101 \\ \hline
+1011101 & = & +1100N01 \\
 & = & +10N00N01 \text{ Sym. Binary}
\end{array}$$

2) Convert 10*N*00*N*01 from symmetrical binary to negabinary and cobinary

10*N*00*N*01	Symmetrical Binary
*N*0100*N*01	Symmetrical Negative Binary
110101101	Negabinary
*NNN*00*NNN*	Cobinary

Negabinary-Coded Decimal

A symmetrical set of eleven numerals ranging from -5 to $+5$ was first suggested by Shannon in 1950 (see Bibliography) as having possible application to simplification of computer arithmetic. As can be seen from Tables 5 and 6, these values can be neatly bracketed by four-bit codes in either negabinary or cobinary. The easy complementation of digits is lost; however the need is eliminated because the primary object of such complementation is to perform subtraction by adding the complement, and this practice is not necessary in negative radix arithmetic. Hence, even though the primary radix is positive $(+10)$, the secondary radix can be negative (-2) and the resulting system (negabinary-coded-decimal) has many of the advantages of negative radix notation.

Many other decimal codes, both ten-numeral sets and redundant sets are, of course, possible. An almost symmetrical set of sixteen decimal numerals having values corresponding to four bits may be obtained by biasing the zero by -2 (cobinary $+2$), so that the zero is represented by 0010 (cobinary 00*N*0). A biased code confuses the addition algorithm somewhat, because 0100 (cobinary 0*N*00) has to be added to each digit of the sum to compensate. In subtraction, the bias is automatically wiped out.

It is interesting that the normal, 0-9, set of ten-decimal numerals can be represented by an unbiased cobinary code of four bits. A more useful set might be one which includes at least one negative digit, say *N*, followed by the normal 0, 1, . . . , 7, and 8, which would also permit decimal representation and arithmetic without separate polarity symbols.

Codes for Residue Number Systems

A more interesting set of possible codes is presented by residue notation, also called modular or mixed radix notation. In this type of number system, each digit position has its own radix, rather than a different power of one radix, and the numerals for each such radix comprise the set of residues for that radix. Radices must be relatively prime, and a set of numbers may be uniquely represented ranging from 0 to the product of all radices, less one. For example, in a two-digit number system using radices 3 and 2, a total of six different representations is possible, e.g., the numbers 0, $+1$, $+2$, $+3$, $+4$, and $+5$. To find the representation for each of these, we divide it by the radices, 3 and 2, and obtain the residues, or remainders. Thus, 4 is represented by the digit pair (1,0) since the residue of 4 modulo 3 is 1, and the residue of 4 modulo 2 is 0. Table 7 gives the entire set of digit pairs, or "numbers," for the decimal numbers 0-5 in a radix (3,2) residue number system. If radices 5, 3, and 2 were used, then there would be a total of $5 \times 3 \times 2 = 30$ representations; larger sets of representations

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3005 PP	X		DC	1.0MHz	5	X		X		2	2
3008 PS	X		DC	1.0MHz	8	X			X	2	2
3012 SP	X		DC	100kHz	12		X	X		1	1
3016-2	X		DC	1.0MHz	32 (16, 16)		X		X	2	2
3016-2D		X	10kHz	3.0MHz	32 (16, 16)		X		X	2	1*
3020	X		DC	1.0MHz	20		X		X	2	2
3021	X		DC	500kHz	21 (1, 4, 16)		X		X	1	1
3021 B	X		DC	250kHz	21 (1, 4, 16)		X		X	1	1
3050		X	10kHz	500kHz	50 (25, 25)		X		X	2	1*
3064		X	10kHz	5.0MHz	64		X		X	4	NONE

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can be obtained by using more and larger radices.

The advantage of such a system is primarily that carry propagation is eliminated. Thus, in the radix (3,2) residue system of Table 7, the sum of two numbers is formed by adding residues (digits) **without** carries, as illustrated in the following example:

Residue	Binary	Decimal
2,0	+10	+2
0,1	+11	+3
2,1	+101	+5

No carry was involved in the above example. In adding +2 to +2 however, we have:

Residue	Binary	Decimal
2,0	+10	+2
2,0	+10	+2
1,0	+100	+4

The arithmetic is explained by recalling that summing each column involves **residue** arithmetic; that is, 2 mod 3 + 2 mod 3 is 4 mod 3, which is congruent to 1 mod 3. No carry is involved.

In past attempts to adapt residue number systems to computers, the numerals sets for each radix were generally expressed in a binary code, including normal binary representation for the positive integers. Thus, the arithmetic for each digit (radix) position still involved normal binary arithmetic, with provision for carry. However, the carry chain was limited to the length of the binary equivalent of the largest radix. At present, the utility of residue notation for computer design is rather limited. Major problems exist in sign detection, detection of overflow, division, and scaling, and while algorithms for these operations have been developed, they are not generally practicable. It is possible that some of these problems are traceable to the difficulties of the coding of numerals, rather than to residue notation. This may be particularly true of sign detection, which is in turn an operation critical to division. If so, the use of a negative binary code may provide better solutions. Some possibilities are therefore discussed here.

Since the radices must be relatively prime (or else unique representation would be lost), only one radix can be even. The use of all odd radices introduces the fascinating possibility of using a set of residues for each (odd) radix comprising a symmetrical set of negative and positive numerals ranging from $-(R-1)/2$ to $+(R-1)/2$, where R is the absolute value of the radix. These could be encoded in negabinary or cobinary. A total of P representations is thus possible, which could represent the set of numbers from $-(P-1)/2$ to $+(P-1)/2$, where P is the product of all the radices.

An example of such a system, using radices 7 and 3, is given in Table 8. The complement of a number is obtained by complementing each digit, and addition, subtraction, and multiplication of either negative or positive numbers can thus be accomplished without need for special provision for negative representation or polarity manipulation.

TABLE 7

Radix (3,2) Residue Number System

Decimal Number	Binary Number	Residues Mod 3	Residues Mod 2	Radix (3,2) Residue Number
+0	+0	0	0	0,0
+1	+1	1	1	1,1
+2	+10	2	0	2,0
+3	+11	0	1	0,1
+4	+100	1	0	1,0
+5	+101	2	1	2,1

TABLE 8

Symmetrical Negabinary Residue Number System of Radix (7,3)

Decimal Number	Residues 7	Modulo 3	Negabinary Coded Residue Number
−10	−3	−1	1101,11
−9	−2	−0	0010,00
−8	−1	+1	0011,01
−7	0	−1	0000,11
−6	+1	0	0001,00
−5	+2	+1	0110,01
−4	+3	−1	0111,11
−3	−3	0	1101,00
−2	−2	+1	0010,01
−1	−1	−1	0011,11
0	0	0	0000,00
+1	+1	+1	0001,01
+2	+2	−1	0110,11
+3	+3	0	0111,00
+4	−3	+1	1101,01
+5	−2	−1	0010,11
+6	−1	0	0011,00
+7	0	+1	0000,01
+8	+1	−1	0001,11
+9	+2	0	0110,00
+10	+3	+1	0111,01

TABLE 9

Negabinary Residue System With Unused Codes

Decimal Number	Residues 7	Modulo 3	Negabinary Coded Residue Number
−10	+4	−1	100,11
−9	−2	0	010,00
−8	−1	+1	011,01
−7	0	−1	000,11
−6	+1	0	001,00
−5	+2	+1	110,01
−4	+3	−1	111,11
−3	+4	0	100,00
−2	−2	+1	010,01
−1	−1	−1	011,11
0	0	0	000,00
+1	+1	+1	001,01
+2	+2	−1	110,11
+3	+3	0	111,00
+4	+4	+1	100,01
+5	−2	−1	010,11
+6	−1	0	011,00
+7	0	+1	000,01
+8	+1	−1	001,11
+9	+2	0	010,00
+10	+3	+1	111,01

A second possibility is illustrated by Table 9, in which radices are selected equal to $2^k - 1$ for various values of k such that the radices are relatively prime. This system is highly efficient in storage requirements. For each radix, a negative binary code is used comprising k bits, and all but one of the possible bit combinations are used to represent the numerals. In Table 9, for example, radices 7 and 3 were used, corresponding to values of k of 3 and 2. The unused codes are 101 and 10, each being the maximum magnitude combination for 3 and 2 bit numbers, and having decimal values of $+5$ and -2. This system also has the advantage that overflow can be used to indicate that an addition or subtraction has resulted in an out-of-range residue, so that the radix can be added or subtracted to yield a residue of not more than k bits. The single illegitimate k-bit code is easily detected, and its one's complement substituted to provide the correct residue. For example, the sum of -5 and $+10$ requires addition of the residue pairs (110, 01) and (111, 01), the sum of which is (101, 110). The code 101 is not legitimate and its complement 010 is substituted; the code 110 has a positive overflow, and the radix is subtracted. The final answer (010, 11), is the residue pair for $+5$.

Summary And Look-Ahead

Many other codes could doubtless be invented for particular kinds of representation and arithmetic. Since negative numbers are a practical necessity in any number system to be used for performing arithmetic, negabinary or cobinary coding offers a simple solution in those cases where use of negative numerals is acceptable or advantageous.

Next month we shall develop the normal arithmetic operations of addition and subtraction, in negative radix systems. Future articles will discuss multiplication, division, and the conversion between positive and negative radix systems. The above reference to "normal" arithmetic operations implies the existence of new arithmetic operations; this is indeed the case, and a later article will introduce the new concept of "complementary arithmetic operations."

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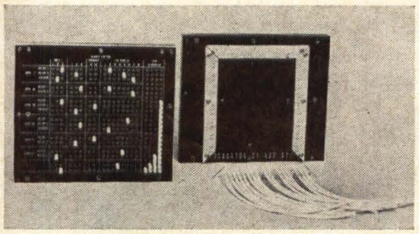


MATRIX PROGRAM BOARDS

Newly-developed X-Y matrix program boards are capable of handling high frequency signals. Typical capacitance through the unit is 4 uuf; crosstalk pickup is 40-60 db down. A cordless video patching panel contains 16 inputs and 17 outputs. Input-output connections are made by inserting pins at the appropriate crosspoints. These units may be supplied with mating coaxial connectors for terminating shielded cables. Co-Ord Switch, Div. of LVC Inds., Corona, N. Y.

Circle No. 221 on Inquiry Card

CRYSTAL OSCILLATOR

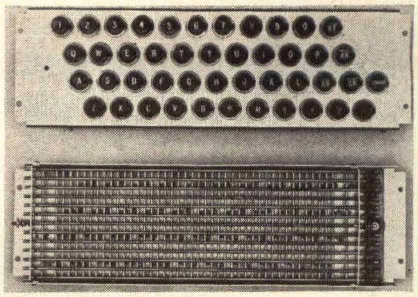
A crystal oscillator was designed for DTL and TTL logic circuitry. Rise and fall time is less than 15 nanoseconds. Fan-out is 5 and input voltage is 5 $\pm 10\%$. Frequency ranges from KHz to 1 MHz. Stability over the range of $-55°C$ to $125°C$ is $\pm 0.025\%$. Size is 1″ x 1″ x 0.375″ Hill Electronics, Inc., Mechanicsburg, Pa.

Circle No. 238 on Inquiry Card

ELECTROLUMINESCENT DIODE

Claimed to be the first reproducible silicon carbide electroluminescent diode, the new device has applications for recording data on film, computer components, and in high temperature electronic components. The diode emits a needle-thin beam of cold yellow light with an efficiency of about 10^{-5} or one photon of light emitted for every 100,000 electrons passing through the diode. It measures 0.030 x 0.030 x 0.015″. Norton Co., Worcester, Mass.

Circle No. 272 on Inquiry Card

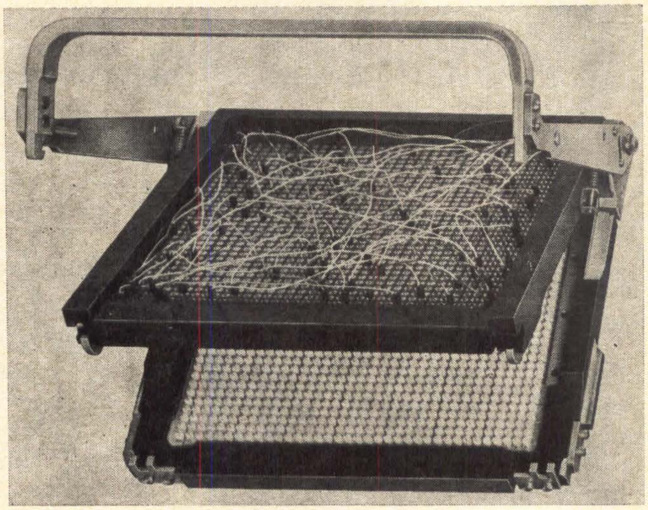


SUB-ASSEMBLY KEYBOARD

An unusual word length of 12 bits is provided by means of a unique mechanical x-y matrix. This sub-assembly keyboard provides high reliability and long life by reducing switch contacts by as much as 15 to 1. Interface problems are eliminated by bounce-free action of the switch contact output. Keys have snap action, light touch feel, and short stroke. The module can generate either Morse, 3 BCD's, ASCII, IBM, EBCDIC, CCIT, or any cipher required on order. It is 7/8″ deep, 3¼″ wide, 11″ long including mounting. Price is $150, Computronics Engineering, Los Angeles, Cal.

Circle No. 253 on Inquiry Card

NEW PRODUCTS



PATCH PANEL ASSEMBLY

Designed for use in programming computers and digital systems, a new patch panel assembly permits 1064 simultaneous connections. It can be interconnected into a system with patchcords or can be wired permanently. The patch panel features a levered-activated anodized aluminum frame with a positive locking feature. The top patchboard is made of epoxy glass with 0.040″ cage type high reliability jacks for positive contact. One or more top boards can be supplied for a variety of programs. The bottom board is made from anodized aluminum with Teflon pressmount type 0.040″ plug connectors with clamp or soldered tails. The Teflon plugs can be replaced without removing the board from its frame or mounting. Patchboards are marked into grids of 25 contacts and are numbered and lettered for ease of wiring identification. Cambridge Thermionic Corp., Cambridge, Mass.

Circle No. 242 on Inquiry Card

DUAL IN-LINE RECEPTACLE

New receptacle is a universal mounting device for all dual-in-line packages with 14 round or blade leads. Compact insulator design permits high packaging density (side-by-side mounting on 0.500″ centers, in-line mounting on 0.800″ centers). Wire-wrap contacts are of the double-leaf type and are made of spring-temper phosphor bronze with a gold flash over a nickel underplate. Insulator is a wood-flour filled phenolic (per MIL-M-14F, Type CFG) molding. Mounting is by interference fit between contacts and PC holes (no soldering needed with plated-through holes), or riveting. Closed-entry contact holes with chamfered edges prevent contact damage and facilitate DIP insertion. Elco Corp., Willow Grove, Pa.

Circle No. 232 on Inquiry Card

SQUARE WAVE GENERATOR

Solid-state square wave generator is said to produce square waves of exceptionally clean shape over a wide frequency range, from 1Hz to 10 MHz. Square-wave rise and fall times are less than 5 nanoseconds, overshoot, preshoot, and ringing are less than 5%, there is no sag, and jitter is less than 0.2% of waveform period at any repetition rate. The generator supplies 5-volt pulses into a 50-ohm load (10 V open-circuited). A second output, matched for 600 ohms, supplies 30 V peak into 600 ohms or 60 V open-circuited (risetime at this output is 70 ns across 600 ohms). Both output waveforms are dc-coupled negative-going but differ in time phase by 180°. A third output supplies 2-volt trigger pulses into 50 ohms, either positive or negative as selected by a switch, coincident with the leading edge of the 50-ohm square wave. These pulses are useful for synchronizing an oscilloscope and they also make generator useful as a controllable-rate trigger source. Hewlett-Packard, Palo Alto, Cal.

Circle No. 216 on Inquiry Card

DIGITAL OSCILLOSCOPE SYSTEM

An oscilloscope and a digital unit comprise a new high-speed digital oscilloscope system that provides digital readout of measurements that are displayed in analog form on the CRT. The system has flexible measurement capabilities and features up to 50 measurements per second, easy external programming, BCD data outputs, and solid-state circuitry with extensive use of integrated circuits. The digital unit can make a wide variety of repetitive pulse measurements on the signals displayed on the oscilloscope. The digital presentation can designate voltage measurements, time-difference measurements between similar pulses, and time-difference measurements between percentages or voltages of pulse amplitudes. All of its measurement functions can be programmed by means of ground closures or logic levels. The programming is achieved with 104 program lines using negative logic with true being ground or less than 2 V and false being open or greater than 6 V. Suitable programming devices include card readers, block readers, computers, etc. Tektronix, Inc., Beaverton, Oregon.

Circle No. 211 on Inquiry Card

TRIM POTENTIOMETER

A new ½ watt trimmer potentiometer costs less than $1.00 each in quantities of 1,000. Designated as the 2300 Series, this new commercial grade trimmer is directly interchangeable with other 1-inch commercial models. New construction method is said to create excellent setting stability, allowing reliable use for balancing printed circuits. Other design features include ultrasonically-welded lid for protection against dust and dirt, shockproof insulated nylon-head lead screw, an exclusive wiper arm that provides positive settings (idles at either end to prevent over-travel damage), gold-plated collector bar and printed circuit pins, and precision-molded case made for use with production soldering processes. Resistance range is 10 ohms to 50K ohms with a standard tolerance of ±10%. Power rating is 0.5 watt at room temperature to 0 watt at 85C with an operating temperature dange of −55C to 85C. Dimensions are 1 inch long by 0.36 inch high by 0.28 inch wide. Dale Electronics, Columbus, Nebraska.

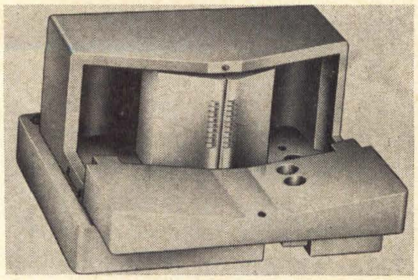
Circle No. 203 on Inquiry Card

NEW PRODUCTS

SYSTEMS POWER SUPPLIES

New systems power supplies offer a packaging technique that allows them to be mounted on any of three mounting surfaces. The new series is available in 88 different voltage-current combinations. Up to 485 watts of power from the modules will fit into a standard 19" rack. There are four package sizes, providing 6 watts in the smallest size. The others are 18 watts, 48 watts, and 120 watts. A wide variety of rack mount adapters is also available to allow the systems designer to use the smallest possible rack for his power requirements. The modules, designated the SC series, are self-cooled. No external heat sinking is required. Remote sensing and remote voltage adjustment capabilities are standard. Line and load regulation combined is ±0.05% or 2mv, whichever is greater. Response time is 20 usec. and ripple is 1 mv, rms. Consolidated Avionics, Westbury, L.I., N.Y.

Circle No. 246 on Inquiry Card



TAPE HEADS

Seven and nine channel read/write digital tape heads are said to be distinguished by extremely high temperature stability, encapsulated above 250 degrees Fahrenheit. These digital heads have glass deposited read and write gaps. Combination ferrite and hi-nickel shields included on covered models. Tape cleaner is included or provision is made for installation holes on tape drive equipment. Magnetic Heads, Inc., Minneapolis, Minn.

Circle No. 257 on Inquiry Card

FET OPERATIONAL AMPLIFIER

New FET input amplifier offers a common mode rejection ratio in exces ofs 10,:1000, over a temperature range of −55 to 85C. The amplifier, Model D-15, has an input impedance, in both differential and common mode, greater than 10^{11} ohms. Its typical frequency for full output is 35KHz (either input). Frequency for unity gain is 2.5MHz and voltage gain (into a 10K load) is 25,000. Salient stability specifications include offset current of 10pA and voltage drift of 5uV/°C. Data Device Corp., Hicksville, N.Y.

Circle No. 258 on Inquiry Card

PC CARD TESTER

An automatic card tester for printed circuit cards is adaptable to operate with a wide range of central control and evaluating subsystems. The use of plugboards provides a combination of readily-changed connections to accommodate many types of cards, including discrete and integrated circuits. The tester operates with two types of control; digital computer or programmer/comparator. For computer control, a perforated tape reader and typewriter are included as peripheral equipment. For programmer/comparator control, a manual programming panel is provided instead of the typewriter. A symbolic language has been devised and is used for the source program. An assembly program (SCATRAN) is in turn translated into a sequence of instruction blocks. These instruction blocks then produce an eight-level program tape which is used by the programmer-controller or the computer. The station utilizes a plugboard switching-scheme tied in with the interface connectors into which the modules to be tested are inserted. When a test is to be changed, the plugboard interconnections can be changed easily to meet the new connection requirements. The plugboards are indexed with a wired-in code number corresponding to the card with which each is to be used. General Dynamics, Electronics Division, Rochester, N. Y.

Circle No. 228 on Inquiry Card

SCAN CONVERTERS

Three new double-ended scan converter storage tubes are electrical input-electrical output tubes designed for service in which stored information written in one particular scanning mode is read out with either a different scanning mode or the same mode scanned at a different rate. A feature of the tubes is the shielding between the writing and reading sections, which eliminates write-read crosstalk at the signal output electrode. Type H-1161, a 2⅝-inch diameter tube, features two flooding guns, connected externally for parallel operation, by means of which immediate erasure can be performed, or the decay rate of stored information can be controlled. Resolution is 800 TV lines at 50 per cent modulation by orthogonal reading. Type H-1203, with 4-inch diameter, and Type H-1213, with a 3-inch diameter, are designed as versatile tubes which permit erasure of selected portions, or of the entire storage target area performed as a time-shared operation with either the writing or reading gun. It is also possible to control the information decay rate by applying suitable pulses simultaneously to the read-gun cathode, control grid, and prefocus electrode during sweep retrace intervals. Resolutions are 2000 lines for the H-1203 and 1600 lines for the H-1213, both at 50 per cent modulation by orthogonal reading. Hughes Vacuum Tube Products, Oceanside, Cal.

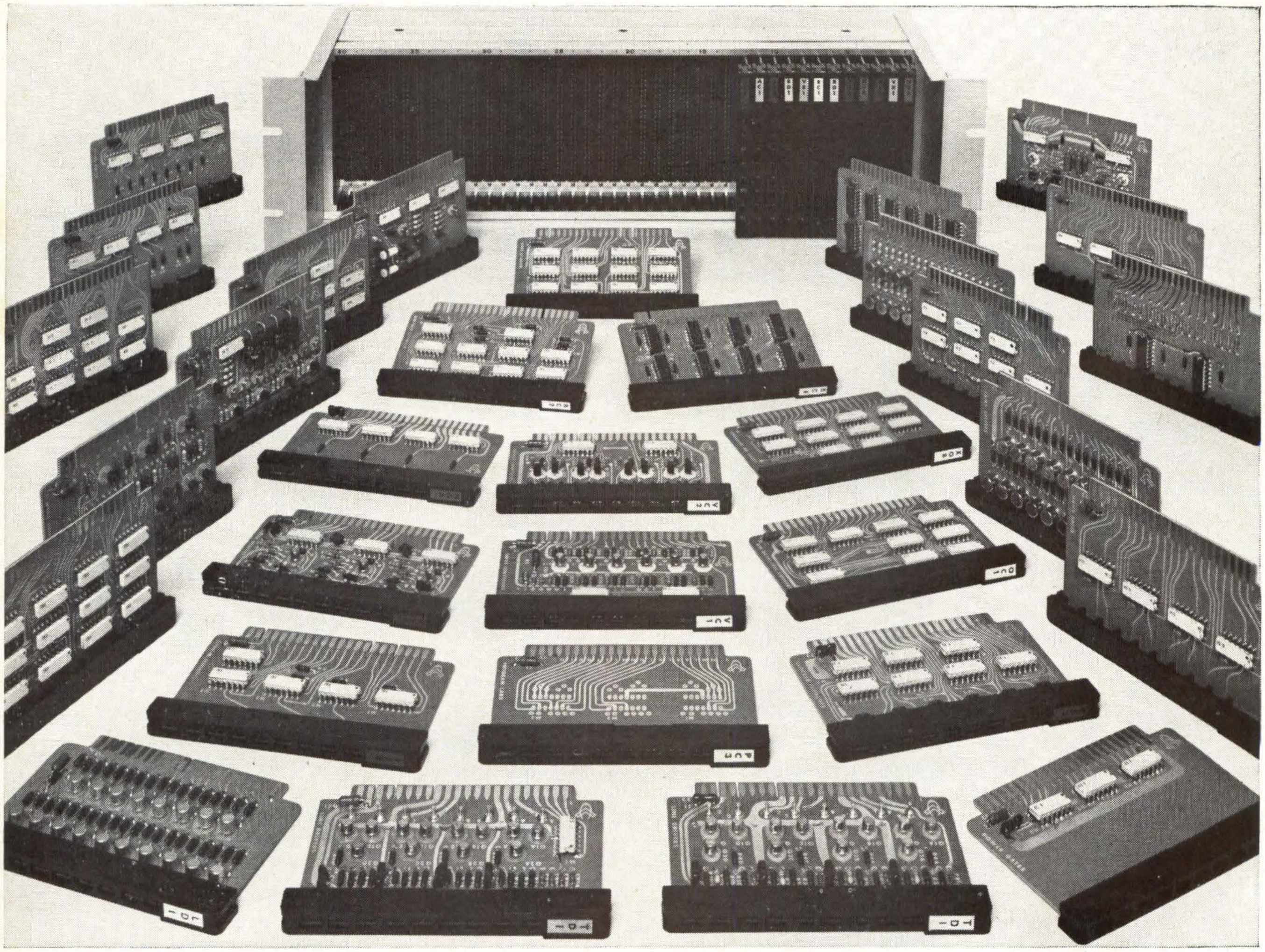
Circle No. 251 on Inquiry Card

BCD ENCODER

Shaft encoder with its associated logic card provides non-ambiguous BCD 8421 output. The encoder counts from +000.0° to +179.9° then, −179.9° to −000.0°. The electronic card consists of dual-in-line integrated circuit logic modules. Output voltage levels are 5 volts and operating power is 5 volts at 150 mamps. Units are available with 100, 200, or 400 count resolution — internal select electronics — full count range 0-359.99, 0-99999, and 0 ± 179.99. Vernitron Corp., Encoder Div., Farmingdale, L.I., N.Y.

Circle No. 235 on Inquiry Card

THE COMPLETE FAMILY OF MICRO LOGIC PRODUCTS.



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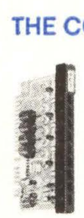

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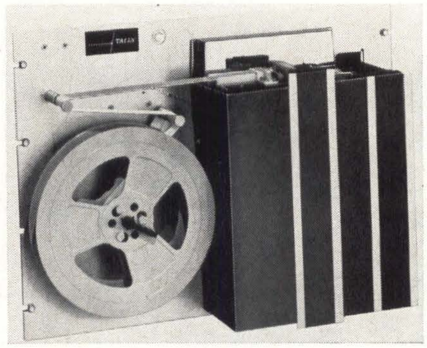
CIRCLE NO. 47 ON INQUIRY CARD

NEW PRODUCTS



TAPE PERFORATOR

A new high speed paper tape perforator features integral tape handling on a space-saving rack mounted panel. The new model, designated the P-150A, operates asynchronously up to 150 characters per second. Error control options allow the motion of each punch pin to be mechanically sensed as the character is being punched. Odd or even parity can be checked. If an error has occurred, the tape advance pulse can be inhibited and the erroneous character overpunched with a delete code. Standard units have unidirectional tape advance with remote tape backup at a modest extra cost. Tally Corp., Seattle, Wash.

Circle No. 262 on Inquiry Card

DIGITAL DECODER ASSEMBLIES

New digital assemblies include binary-to-octal, BCD-to-decimal, 2421-to-decimal, 5421-to-decimal, excess 3-to-decimal, and binary-to-hexadecimal decoders. The binary-to-octal decoder card provides conversion from a 3-bit to an 8-bit octal equivalent and is available with options for either a single decoder, a dual decoder, or a decoder with drivers. The binary-to-hexadecimal decoder assembly provides conversion from a 4-bit binary code to a 16-bit alphanumeric equivalent. The other assemblies all provide conversions from a 4-bit binary code to a 10-bit decimal equivalent and can be ordered with options for either a single or dual decoder. Cambridge Thermionic Corp., Cambridge, Mass.

Circle No. 268 on Inquiry Card

RECORDING STORAGE TUBE

A miniature recording storage tube is capable of simultaneously reading and writing. The CY1519 is a dual-gun storage tube which may be regarded as an electronic input-electronic output storage device which combines high output signal with high resolution. The tube has a nominal length of 16½ inches and a maximum bulb diameter of 1.5 inches. Resolution is typically 850 TV lines per diameter. The chief application is scan conversion to television-type presentation of the outputs of such airborne sensors as sonar, infrared, and radar. This system yields a bright display with high resolution and adjustable gradual erasing. Stored signals can be held for a long period, read several thousand times, or erased in a fraction of a second. The storage capabilities permit additional coherence of target information despite high noise levels. The tube achieves a wide range of gray shades, fast writing speeds, and selective erasure of stored information. Erasing operations can be carried out by either the reading or the writing gun. Raytheon Co., Industrial Components Operation, Quincy, Mass.

Circle No. 226 on Inquiry Card

INCREMENTAL PLOTTERS

First of a new family of incremental plotters operating at the rate of 800 steps per second is said to feature high speed and accuracy, with a resolution up to 0.0025 inches. According to the manufacturer, this increase in incremental performance will extend the use of digital plotting for applications previously requiring high-precision drafting systems. All models in the new incremental family make use of an exclusive engineering concept that allows the generation of multiple plotting commands from a minimum of digital input. Over an average run of plotting applications, the logic design is said to save from 50% to 90% of computer write-time. By shrinking plotter command lists, the same principle also serves to reduce the amount of input media used. The plotter is designed to operate on-line with computer, multiplexed to a time-sharing system, or off-line with magnetic tape input. Benson-Lehner Corp., Van Nuys, Cal.

Circle No. 224 on Inquiry Card

FLEXIBLE CIRCUITS

Principal characteristics of a new flexible flat cable and printed wiring circuit is a flat conductor of 0.003" average thickness. Conductors will be etched from a foil (forming a planar pattern) or rolled and laminated using either polyimide, Teflon, polyester, or polyvinyl chloride insulation. Finished cables are thin, flexible, and may be furnished, shielded or in harness assemblies. They are said to offer increased reliability, consistent electrical characteristics, and extreme ease of handling Cerro Corp., Old Saybrook, Conn.

Circle No. 201 on Inquiry Card

NEW PRODUCTS

CRT DISPLAY CONVERTER

Two new CRT display converters enable a recorder to provide a large, precisely scaled plot of a CRT display. It is an interface device which fits between any oscilloscope and X-Y or strip chart recorder. The first new device, called the PM 1001-02, enables the instrument to operate properly with curve tracers. New circuitry senses the absence of a sampling pulse which causes the pen-lift relay to energize and the retrace circuit to cycle. This becomes necessary with the curves of certain transistors because the CRT trace terminates before it has progressed to the right edge of the graticule. It senses the end of the CRT trace, lifts the recorder pen, and initiates retrace. An additional control on the new converter allows an operator to set the recorder vertical start point even though the CRT trace starts after the first vertical graticule line. The second unit, for recording waveforms at very low repetition rates, is the PM 1005. It is able to record oscilloscope waveforms at repetition rates as low as one every 10 seconds. Pacific Measurements, Palo Alto, Cal.

Circle No. 222 on Inquiry Card

DATA ACQUISITION

New line of stored-program data acquisition systems samples a large number of analog and digital inputs, performs A/D conversion, formats the system data for computer compatibility, and records data on magnetic tape. The system is available in three models, each offering varying degrees of data manipulating facility. Model 100 includes the essential commands which provide control over sampling sequence and tape block length. Model 200 includes an expanded command list which allows a more sophisticated approach to data acquisition. Model 300 is provided with a general-purpose computer interface which allows on-line processing of the data collected. Key to the flexibility of the data acquisition system is a high speed core memory providing storage as a data buffer as well as for program steps, one hundred of which can be stored. Program steps, consisting of input channel identifiers and control functions, are entered into the memory via a ten-key keyboard as decimal digits. A standard system includes a sixteen channel multiplexer, expandable to one hundred channels, an A/D converter, a 4000 word 8-bit core memory and a digital tape transport. Each of these units are selectable to be compatible with user requirements. Conversion rates as high as 100,000 conversions per second are obtainable. Information Control Corp., El Segundo, Cal.

Circle No. 231 on Inquiry Card

NEW PRODUCTS

GLASS FIBER OPTICS

Said to be the industry's first continuous length flexible fiber optics made of glass, non-coherent fiber optic bundles, jacketed in polyvinylchloride (PVC), are available in single lengths up to 10,000 feet. The glass fibers can be twisted and flexed without degradation of light transmission. Initial selling price is 10 cents per foot in quantities of 50,000 feet. As volume increases, the company expects the price to fall to five cents or less per foot, depending on quantity and specifications. The jacketed fibers can easily be cut, terminated, end finished, and installed to light source and output devices. They are particularly useful in applications where multiple light sources can be replaced by a single source or where direct light might be impractical. Uses include transmission of remote light or optical data, medical instrumentation, electronic data processors, inspection systems, and high-speed printing systems. A 10-foot length of flexible glass fibers with polished ends will transmit 40 per cent of input light. Corning Glass Works, Corning, N. Y.

Circle No. 243 on Inquiry Card

SYSTEMS POWER SUPPLY

A systems power supply produces five voltages from +20 to −20 VDC at currents from 1 to 7 amperes. Typical of systems supplies designed for data processing equipment, the Model 11578 incorporates features which can be adapted to specific system requirements. The supply accepts inputs of 100 to 250 VAC at 47 to 63 Hz, and incorporates four series regulators and one shunt regulator. Additional features include 1% envelope regulation, margin-checking, turn-on and turn-off sequencing, and remote sensing. Also provided are automatic current limiting, interlocks, and high pulse load capabilities. Advanced Development Corp., Gardena, Cal.

Circle No. 249 on Inquiry Card

AXIAL FAN

Miniature axial fan is of all-metal construction and is said to incorporate an exclusive and proved broached dual-sleeve bearing system which assures longer and more reliable operation. It offers lubrication-free life expectancy in excess of 20,000 operational hours, continuous duty at 55°C. Designed specifically for industrial and commercial applications, the Model 4500 exhibits a low noise figure of less than 37.5db SIL (Speech Interference Level) which is of primary concern in computer and office machine applications. Pamotor, Inc., San Francisco, Cal.

Circle No. 200 on Inquiry Card

RESISTOR NETWORKS

Precision matched thick-film resistor networks are offered in values from 100 ohms to 100K. The networks are glassivated and "fired" on a common alumina substrate to assure stability and temperature tracking. Temperature tracking of a ratio of 25ppm/°C from −55°C to +125°C is standard. The networks show less than 0.05% change in absolute resistor value after 1000 hours load life. Price of the thick-film resistor networks depends upon number of bits and package configuration. Microtek-Electronics, Inc., Cambridge, Mass.

Circle No. 265 on Inquiry Card

DELAY-LINE MEMORIES

New delay line memories are capable of storing up to 20,000 bits in a single magnetostrictive delay line. Input and output characteristics are designed to be completely compatible with system requirements. Newly-designed modules employ integrated circuitry in and out, with a special low voltage series using a single power supply of $+4\frac{1}{2}$ or $+5$ volts. Model MM offers up to 5000 bits (bipolar, 1 MHz bit rate) or 10,000 bits (NRz, 2 MHz bit rate) and will perform over a wide temperature range. Delay Devices Corp., Watertown, Mass.

Circle No. 291 on Inquiry Card

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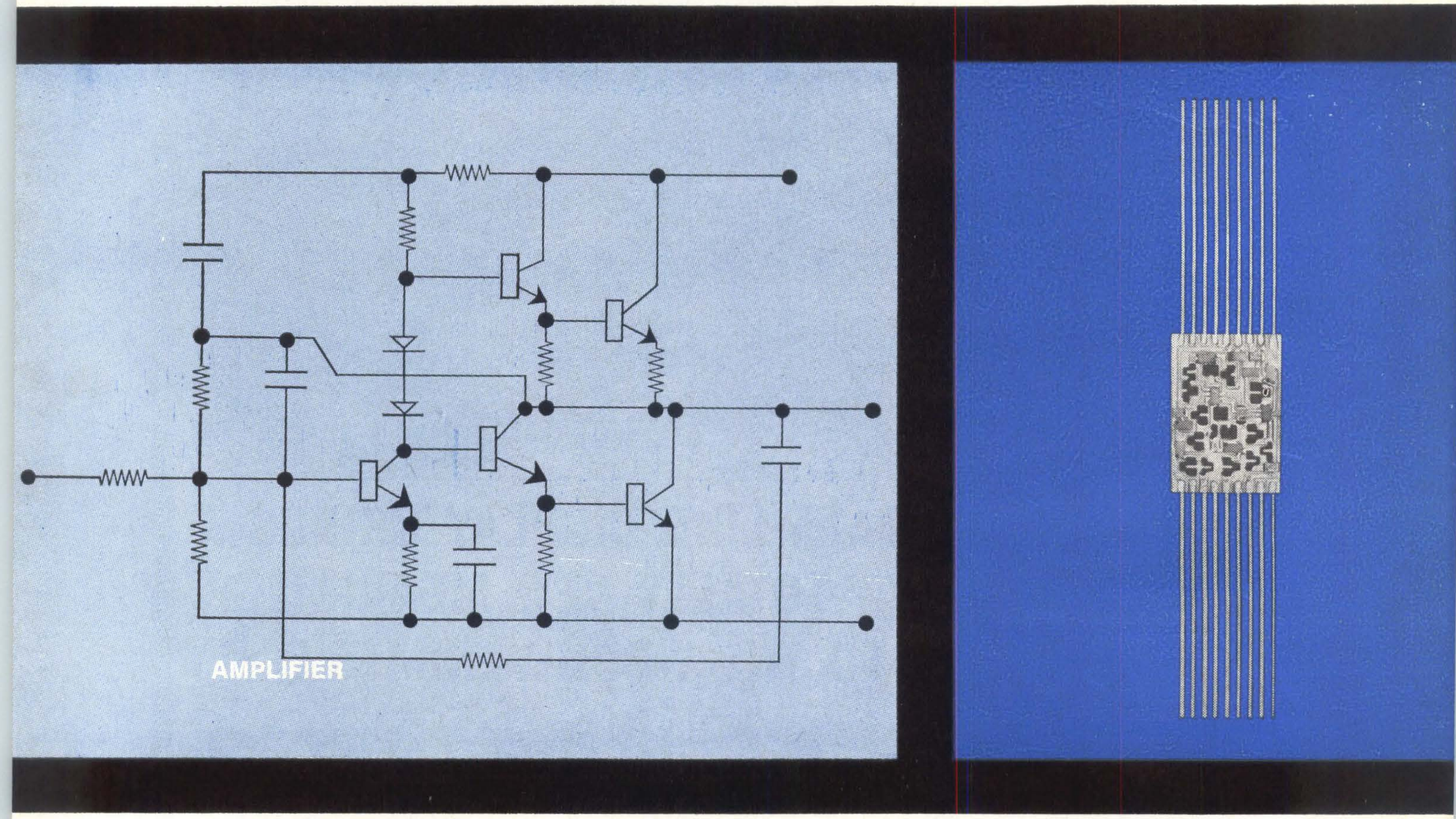

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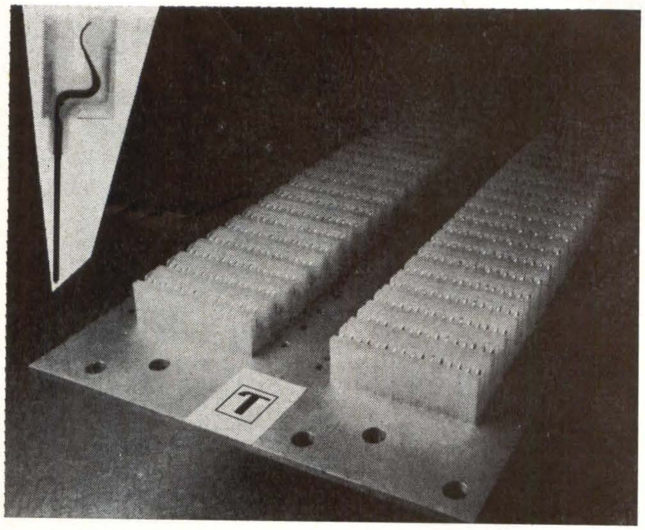
CIRCLE NO. 55 ON INQUIRY CARD

NEW PRODUCTS



CONNECTOR PLATE ARRAYS

Large scale aluminum plate connector arrays are capable of accepting all current manual and automatic machine wiring methods. Back panel wiring terminals are precisely indexed, available in square or rectangular geometries, and identified by alphanumeric stamping or silk screening. Circuit card contacts range from leaf, fork, and male posts through special spring cage types. Contact insulators are molded in various colors and materials with modular single, double and cluster configurations. Transitron Electronic Corp., Wakefield, Mass.

Circle No. 240 on Inquiry Card

BINARY CODE SWITCH

Compact switching matrix for memory, programming, data, voice, and broadband switching applications offers 2,040 switching contacts in 670 cubic inches. Switch includes ten modules, each with 17 multiple positions having 12 make contacts per position. Maximum power voltage is 56V, minimum 44V. The Ericsson Corp., New York, N. Y.

Circle No. 284 on Inquiry Card

SELF-DECODED ENCODER

A size 11, 13-bit, self-decoded encoder with natural binary output requires no external decoding or drive electronics. The new encoder offers a true, natural binary, unambiguous output. A second unit, supplies as an output both the natural binary number and its complement, available to those who need an encoder with self-checking ability. Encoder Div., Litton Industries, Chatsworth, Cal.

Circle No. 212 on Inquiry Card

NEW PRODUCTS

SHAFT ENCODER

Based on a simple patent-applied-for mechanical-optical principle, a high code-count shaft encoder is priced at under $400, complete with self-contained solid-state electronics. Specially sealed against hostile environments, the 3½-pound package measures less than 3½" x 5" x 6". Count capacity is 32,768 (2^{15}) in reflected binary (gray) code, delivered after internal amplification to a sealed terminal connector. Other codes, requiring external solid-state translation, are available. Input shaft motion results in 2048 counts per revolution, monitoring accurately up to 10,000 counts per second. Rotation adds or subtracts, depending on direction, repeating the code sequence after 16 full turns. The unit features two uniquely interacting code discs each geared to the input shaft. Ambiguity is said to be permanently eliminated, without electronics. The single, instantly-replaceable incandescent lamp is rated 5,000/10,000 hours and is monitored for output by a clear track on the fast code disc. Consolidated Controls Corp., Bethel, Conn.

Circle No. 227 on Inquiry Card

MULTIPLE VOLTAGE POWER

Specifically designed for systems use, new rack-mounted power supplied allow users to select up to four independent dc output voltages in the same chassis. Offered in the 3½-inch and 5¼-inch rack panels, these supplies feature output voltages to 60 vdc, output current up to 25 amps, voltage regulation better than ± 0.1 percent, ripple less than 5 mv, ± 5 percent voltage adjustment, independent floating outputs for positive or negative polarity, and input and output protection. Eastern Dynamics, Inc., Bloomfield, Conn.

Circle No. 244 on Inquiry Card

DATA RECORDING SYSTEM

Third generation data collection, transmission, and computer input device replaces punched cards and punched paper tape. Direct recording from IBM Selectric I/O on ¼" magnetic tape in continuous loop cartridges provides the media for computer input, data transmission, and automatic typing. Variable length cartridge and variable densities provide for virtually unlimited cartridge capacity. Standard cartridge capacity is 190K. Transmission speeds are put to 300 CPS using standard Dataphone sets. Marksmen, Inc., Kansas City, Mo.

Circle No. 234 on Inquiry Card

IC SOCKETS

New sockets were developed for aging, production, breadboarding, and life or sampling test of dual-in-line IC packages. The new sockets accommodate all packages in common use with 14 or 16 leads on 0.100″ centers. Round, rectangular, and octagonal leads, trimmed as short as 0.100″, are accepted. Large chamfered entrances permit fast, easy insertion of devices. Quick-removal slot facilitates rapid withdrawal, and ejection slot is available for semi-automatic device removal. Designed for chassis mounting or dip soldering to PC boards, units are available with or without mounting flanges and with tubular or tab type terminals. Overall socket dimensions include ¼″ above board and ½″ wide by ¾″ long. Barnes Development Co., Lansdowne, Pa.

Circle No. 205 on Inquiry Card

COUNTERMODULES

Versatile single-wheel counter modules feature electric reset, readout, and transfer. New models in this series consist of a BCD counter and a unit equipped with an acknowledgment switching function. The BCD model offers four-line — 1,2,4,8 — readout. The "acknowledgment" decade utilizes a switching function to verify the account registration at a remote location. This model is also available as a subtractive version. A completely new pushbutton switch is also offered with either decimal or BCD output. This 10-position switch can be used as a separate component or in combination with a decade to provide a predetermining function. They are said to be ideal for a variety of predetermining controls in automatic systems such as data processing equipment, peripheral computer equipment, and machine tool numerical controls. The counters are easily stacked to form a compact, multi-digit control package in a variety of configurations. Improved Delrin materials are used for the figure wheel, drive gear, drive pawl and arm, no-back pawl, and preset button. Veeder-Root, Hartford, Conn.

Circle No. 208 on Inquiry Card

LITERATURE

Information Retrieval

The BOLD (bibliographic On-Line Display) system for automated document storage and retrieval is described in a new brochure. The BOLD user, located at a station equipped with teletypewriter and CRT display, communicates with the computer, using a language approximating everyday English, to receive data from a stored document collection. The brochure lists the features of BOLD which include a browse capability patterned after features found in conventional libraries, a search capability using coordinate index terms that the machine helps the user to specify, and instant display of document numbers, titles, authors, and abstracts. System Development Corp., Santa Monica, Cal.

Circle No. 307 on Inquiry Card

Circuit Design Program

CIRC, an SDS-developed computer program to assist in circuit design engineering, is described in a 5-page bulletin. CIRC is said to reduce circuit breadboarding and testing time by permitting engineers to simulate, evaluate, and modify their designs on an SDS 900 Series computer. It permits computer analysis of circuits containing 50 or more nodes and provides nonlinear models that accurately simulate semiconductor components. Circuit equations are written automatically. In addition to providing a general description of the program, the bulletin takes the reader through a detailed, step-by-step solution to a typical problem in circuit analysis. Scientific Data Systems, Santa Monica, Cal.

Circle No. 301 on Inquiry Card

Transistors and IC's

An 18-page catalog describes more than 500 types of silicon transistors and integrated circuits. Among the more than 400 silicon transistors listed are new epoxy-molded 25 cents types, JAN-approved types, NPN and PNP small signal units, differential amplifiers, PNP avalanche transistors, radiation-resistant devices, medium power switches, and integrated choppers. The new catalog also lists flip-flops, registers, gates, buffers, adders, counter adders, and inverters in a line of RTL integrated circuits. Milliwatt RTL integrated circuits, including flip-flops, expanders, adders, buffers, and gates are also described. National Semiconductor Corp., Danbury, Conn.

Circle No. 321 on Inquiry Card

Fluid Logic

A new publication of interest to persons working in the technology of fluidics is published quarterly in newsletter form. Called "Fluidic Forum" it serves as a medium of exchange for ideas, opinions, and experiences between users of fluidic systems. The bulletin will feature reader's reports and schematic drawings on significant fluidic applications. Featured in the first issue is a definition of what a fluid power system is and how such a system can duplicate, and in many instances, improve upon electronic, electromechanical and mechanical operations. A review of basic fluidic terminology is also included. Corning Glass Works, Corning, N. Y.

Circle No. 311 on Inquiry Card

Multilayer Printed Circuits

An 8-page technical bulletin on multilayer printed circuits details the entire manufacturing process, and also offers long life and environmental test results to demonstrate the high reliability of the boards. Multilayer boards with plated-through holes are described as having evolved into the ideal interconnecting system for integrated circuits. Photocircuits Corp., Glen Cove, N.Y.

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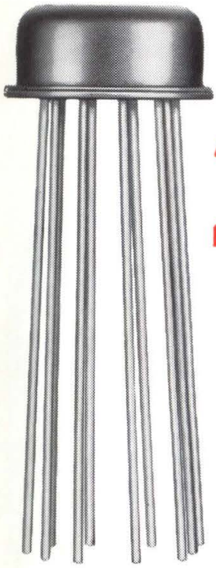

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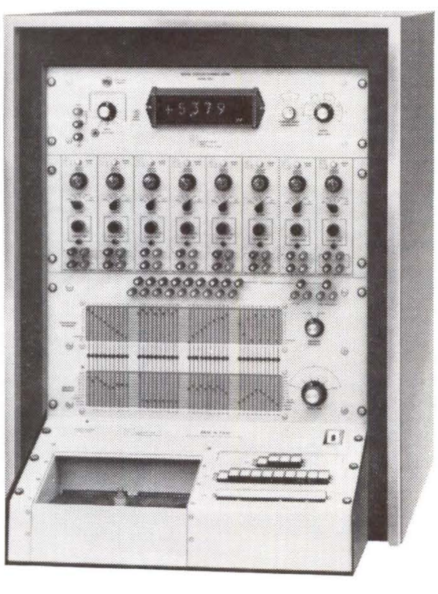

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