COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

JANUARY 1968

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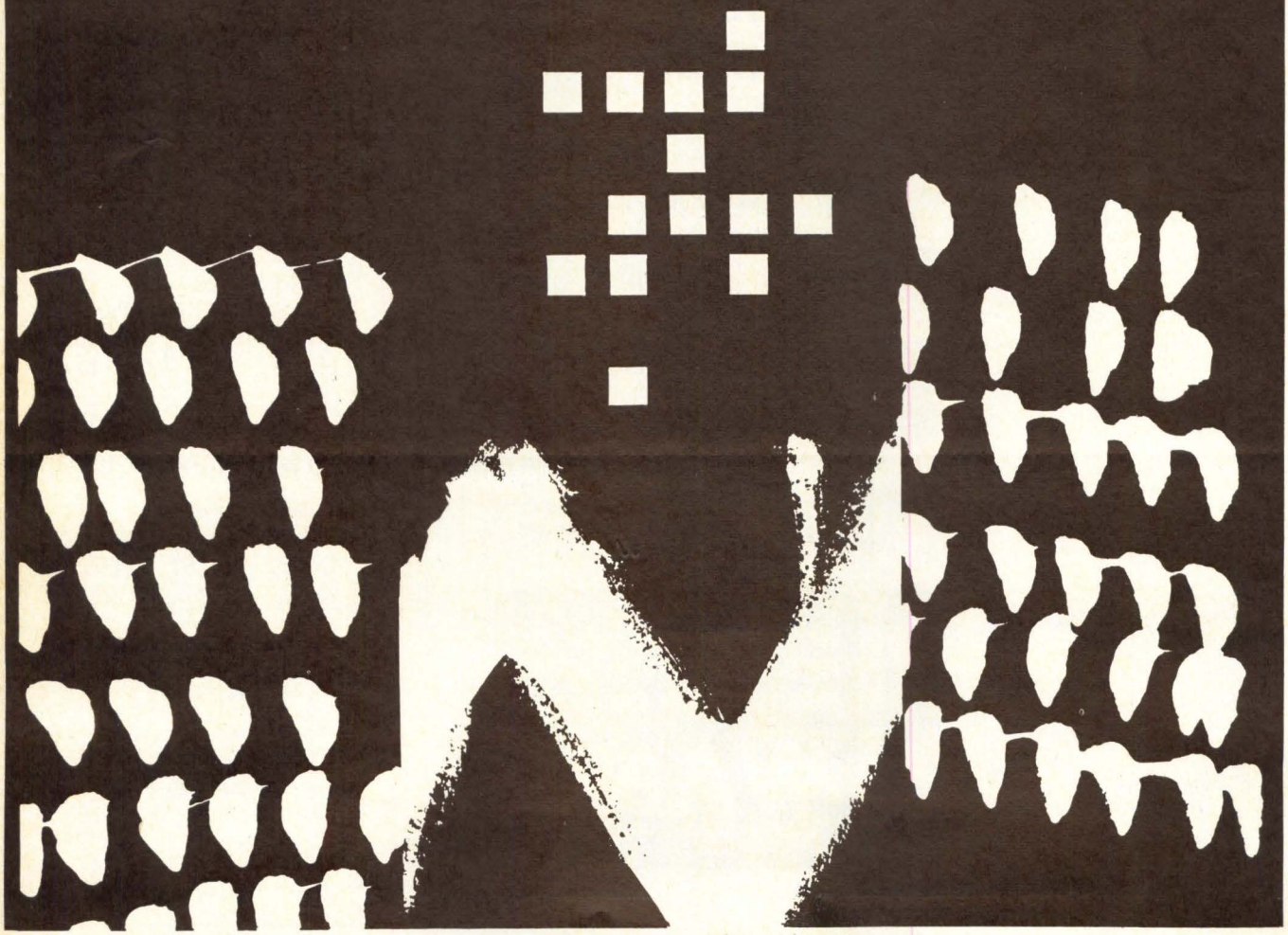

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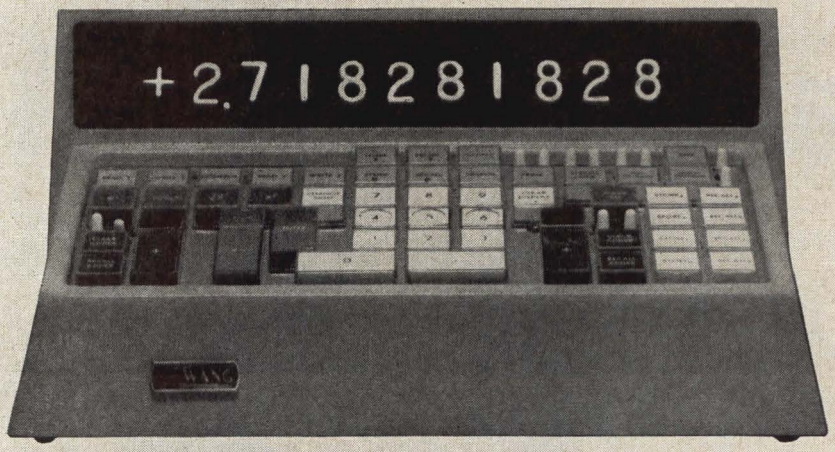

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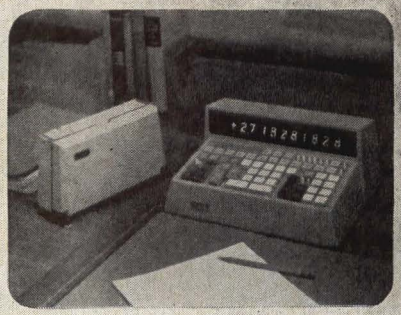

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Make your move now toward time-saving, work-saving computer set up. You can do it with a call to your local HP field engineer. Or get all the information by writing Hewlett-Packard, Palo Alto, California 94304; Europe: 54 Route des Acacias, Geneva.

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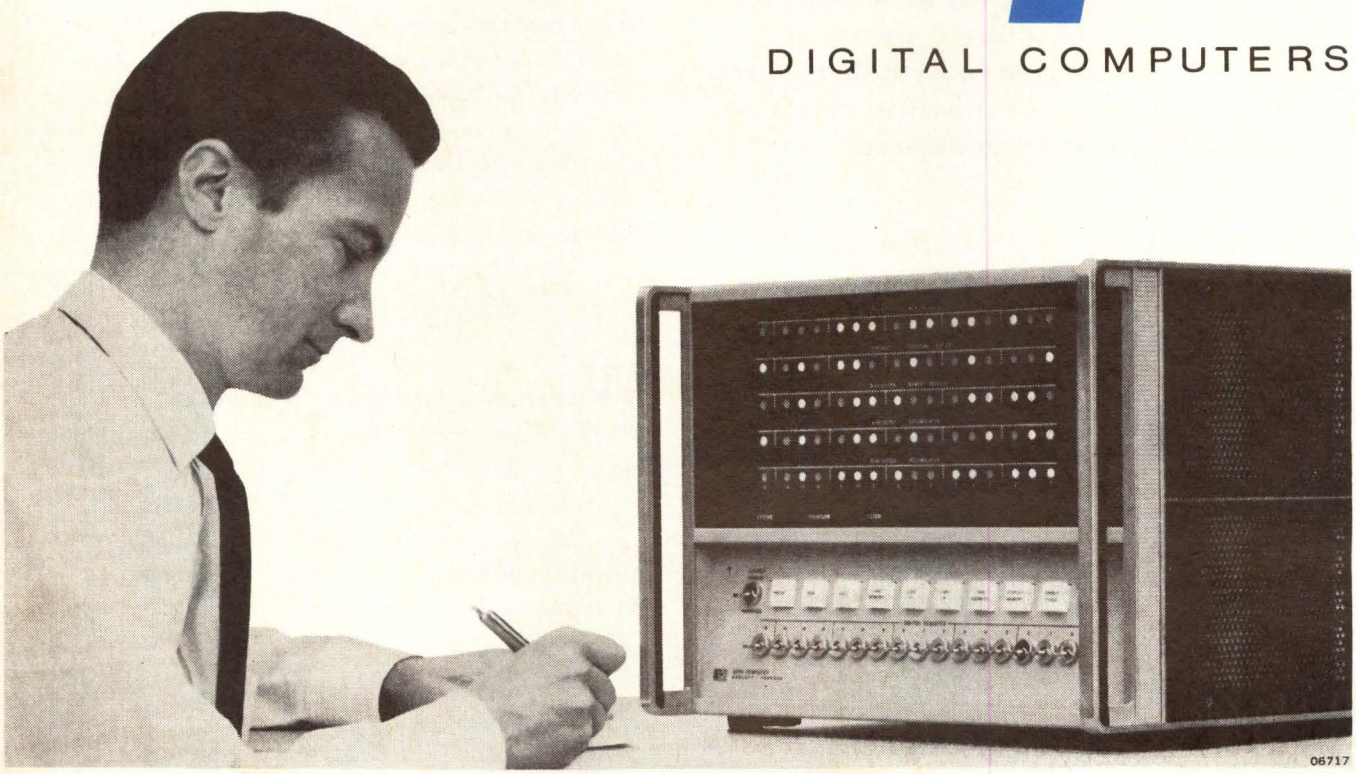


CIRCLE NO. 5 ON INQUIRY CARD

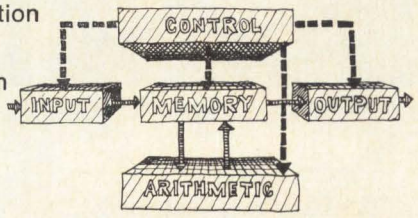
← CIRCLE NO. 40 ON INQUIRY CARD

The great LSI race.

While the rest of the semiconductor industry tried to squeeze enough ICs on a chip to get into the MSI/LSI business, Fairchild turned systems inside out. We were looking for an intelligent alternative to component mentality. Our investigation led to a whole new set of design criteria for medium and large scale integration devices.

A computer isn't a computer.

It's a digital logic system. It has the same functional needs as any other digital system: control, memory, input/output and arithmetic. There's no logical reason to custom design a complex circuit for each system. That's why Fairchild MSIs and LSIs are designed to function as fundamental building blocks in *any* digital logic system. Even if it's a computer.



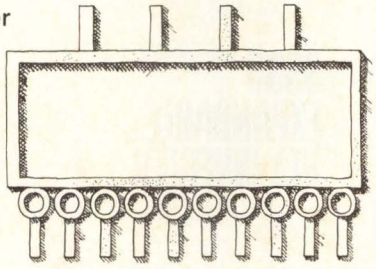
A little complexity goes a long way.

Anybody can package a potpourri of circuitry and call it MSI or LSI. But, that's not the problem. Why multiply components, when you should divide the system? Like we did. We found that sub-systems have a common tendency toward functional overlap. There are too many devices performing similar functions. More stumbling blocks than building blocks. Our remedy is a family of MSIs and LSIs with multiple applications. The Fairchild 9300 universal register, for example, can also function as a modulo counter, shift register, binary to BCD shift converter, up/down counter, serial to parallel (and parallel to serial) converter, and a half-dozen other devices.

Watch out for that first step.

There are all kinds of complex circuits. Some of them have a lot of headache potential. Especially if you want to interface them with next year's MSIs and LSIs. We decided to eliminate the problem before it got into your system. All Fairchild building blocks share the same compatible design characteristics.

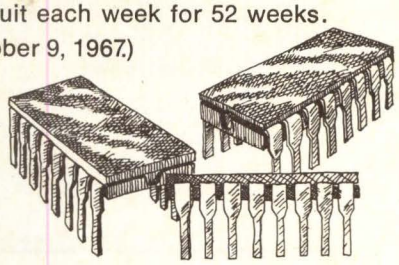
We're also making the interface devices that tie them together. For example, our 9301 one-of-ten decoder can be used as an input/output between our universal register, dual full adder and memory cell. (It could also get a job as an expandable digital demultiplexer, minterm generator or BCD decoder.)



Hurry. Before the price goes down.

Gate for gate, today's complex circuits are about the same price as discrete ICs. But, by the time you're ready to order production quantities, the price should be a lot lower. At least ours will. The reason is simple: Fairchild devices are extremely versatile. There are fewer of them. But, they do more jobs. That means we'll be producing large quantities of each device. That also means low unit cost to you. And you'll have fewer devices to inventory. And fewer to assemble.

If you agree with our approach to medium and large scale integration, we'd like to tell you more about it. There are two ways you can get additional information. One is by mail. Simply write us on your company letterhead. You can also get more data by watching the trade press. Fairchild is introducing a new integrated circuit each week for 52 weeks. (We started on October 9, 1967.) Many of them will be MSI and LSI. If you'd like to see the last few we've introduced, turn the page.



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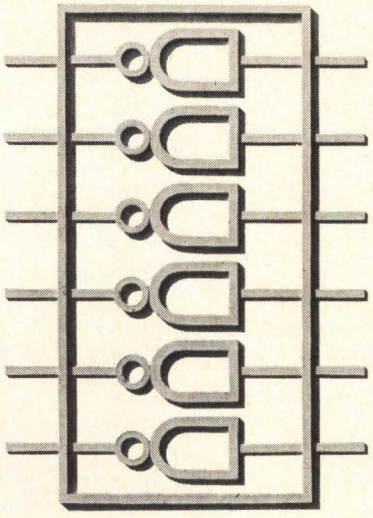
RECAP:

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **6.**

9112 HIGH LEVEL HEX CONVERTER

The 9112 is part of our new family of high noise immunity integrated circuits. It is designed to convert CCSL logic levels to high logic levels. It is ideal for driving MOS devices. The 9112 consists of six high-level DTL gates. Each gate performs a single inversion operation. Worst case noise immunity is 0.5 volts. This high voltage device (usable over the entire range of 12 to 26V) operates from 0°C to +70°C. It comes in an hermetic dual in-line package and is available in volume quantities. Fairchild distributors have it in stock now. Write for complete specs and applications information. Ask about our other new products, too.



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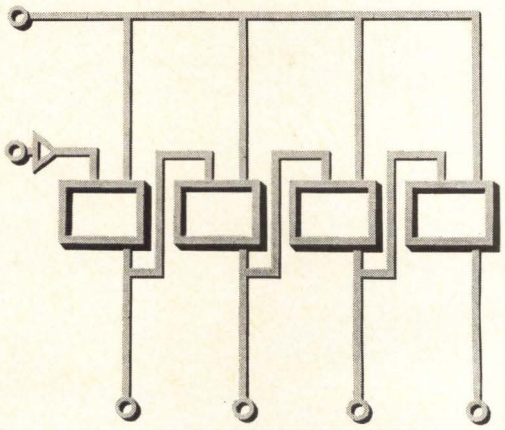
CIRCLE READER SERVICE NUMBER 106

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **7.**

9989 FOUR-BIT BINARY COUNTER

The 9989 is a low-cost, high rate, modulo 16 counter in a single package with preset capability. It is compatible with the entire $C_{2}L$ family and can operate directly into RTL, DTL or TTL circuitry. Typical power dissipation is only 132mW. Its operating frequency is 15MHz. It's designed to operate in the 0°C to +70°C temperature range with nominal power supply voltage of 3.6 to 5.5 volts. The 9989 comes in a 14-pin hermetic DIP. Primary applications include counters, event meters and logic conversion functions. The four-bit binary counter is available in volume quantities. Fairchild distributors have it stock now. Write for complete specs and applications information. Ask about our other new products, too.



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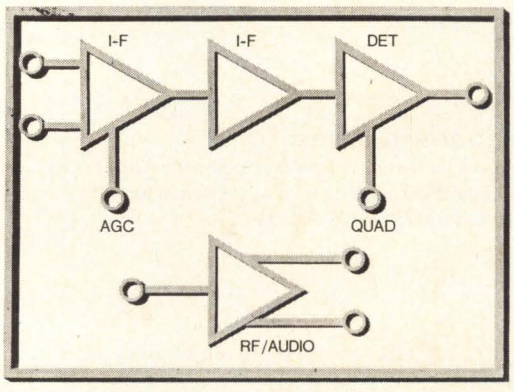
CIRCLE READER SERVICE NUMBER 107

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **8.**

μA719 HIGH FREQUENCY COMMUNICATIONS SYSTEM

The μA719 is a new linear integrated circuit for military and industrial communications systems. It can function as an FM detector, an AM or FM IF amplifier, a modulator or an audio amplifier. It contains two independent amplifiers designed for IF systems to 50MHz. It provides excellent stability (75dB stable gain), AGC capability and extreme flexibility. And, it has three capacitors directly on the chip. The μA719 comes in a hermetic TO-99 package. It's available in quantity in both military and industrial temperature ranges (–55°C to +125°C and 0°C to +70°C). Your Fairchild distributor has it in stock now. Write for complete specs and applications information. Ask about our other new products, too.



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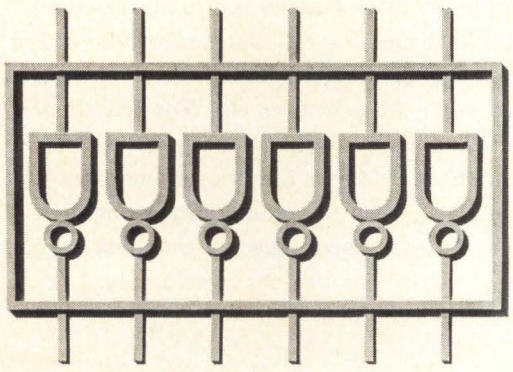
CIRCLE READER SERVICE NUMBER 108

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **9.**

9935 EXPANDABLE HEX INVERTER

The Fairchild 9935 is a fundamental element in the CCSL family. It can serve as the genesis of virtually any digital logic circuit. It consists of six DTL gates without input diodes. Each gate performs a single inversion operation. The device can be expanded to an unlimited number of inputs and, therefore, can be used in a great variety of functions. For example, it can serve as a latching circuit, a one-shot multivibrator, or as a flip-flop in adders, registers, counters, decoders, etc. It can be "wired or" connected to reduce overall system count. The 9935 comes in both a 14-pin hermetic DIP and Fairchild's Cerpak™ It's available in both military and industrial temperature ranges (–55°C to +125°C and 0°C to +70°C). Propagation delay is typically 35 nanoseconds. Typical power dissipation is 8 milliwatts per gate. The 9935 is available in volume quantities. Fairchild distributors have it in stock now. Write for complete specs and applications information. Ask about our other new products, too.



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CIRCLE READER SERVICE NUMBER 109

Fairchild is introducing a new integrated circuit every week. The last two months look like this.

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SEMICONDUCTOR

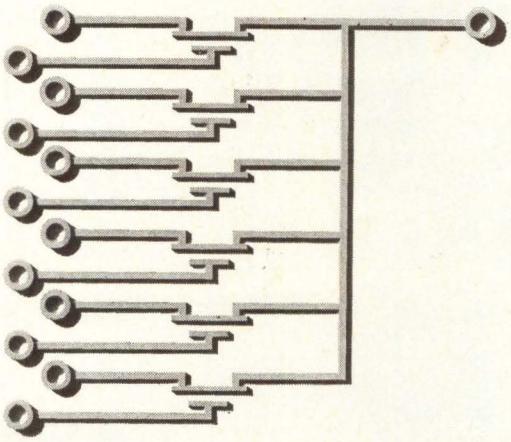
Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **10.**

3701 SIX-CHANNEL MULTIPLEX SWITCH

The Fairchild 3701 is a P-channel enhancement mode MOS six-channel single output switch. It can be used in virtually any switching application. It's ideal for analog and digital data transmission; logic control in industrial systems; and sense line switching in core memory systems. The 3701 approximates a perfect switch. It has very low "on" resistance (300 Ohms), extremely high "off" resistance (2 x 10^10 Ohms), and zero offset voltage. Output leakage currents is typically as low as 0.1 nanoamps. Input gate protection minimizes handling problems. It can accept input signals up to ±5 volts. Stability and reliability are assured by Planar II* technology. The 3701 comes in a 14-pin flatpack. It will operate over a temperature range of —55°C to +85°C.

Volume quantities of this device are now available. Your Fairchild distributor has it in stock. Write for complete specs and applications information. Ask about our other new products, too.

*Planar is a patented Fairchild process.



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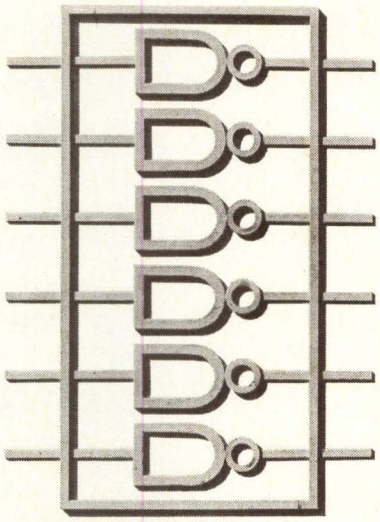
CIRCLE READER SERVICE NUMBER 110

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **11.**

9016 TTL HEX INVERTER

The 9016 completes our 9000 series TTL family. It is a CCSL device designed primarily for high speed inverter applications. It consists of six inverting gates with input clamping diodes to prevent ringing. Active pull-up is provided in the output for high capacitive drive. It can also be used as a line driver. Propagation delay is 11 nanoseconds maximum (standard for the entire TTL family). Power dissipation per gate is typically 14mW. The 9016 comes in a 14-lead hermetic DIP and in flatpack. It's available in both military and industrial temperature ranges (—55°C to +125°C and 0°C to +70°C). You can now order volume quantities of the 9016. Fairchild distributors have it in stock. Write for complete specs and applications information. Ask about our other new products, too.



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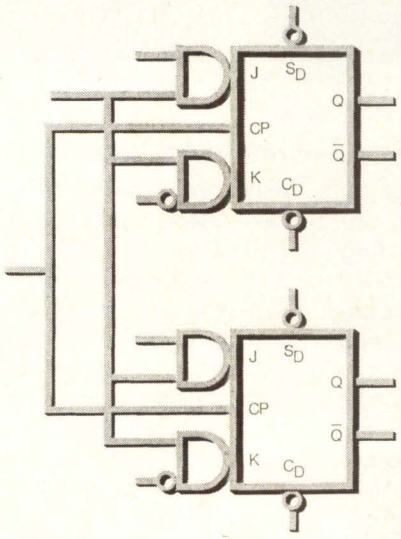
CIRCLE READER SERVICE NUMBER 111

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **12.**

9022 DUAL JK FLIP-FLOP

The 9022 is a CCSL device in a 16-pin hermetic DIP. This TTL circuit consists of two JK flip-flops with a common clock input, common JK input, and separate J and K inputs. The K allows the 9022 to perform as a dual type D flip-flop by tying the J and K inputs together. The common JK input eliminates the need for gating clock waveforms and can result in simplified logic designs and minimized clock skew problems. The 9022 is fast (30MHz) and flexible. It is a true DC-sensitive master-slave dual flip-flop. As a companion to our 9020 dual JKR flip-flop, it provides additional logical flexibility because it has separate set-direct inputs in addition to clear-direct's. Both types of inputs are truly asynchronous and overriding. A single clock buffer reduces clock fan-in and noise. The 9022 comes in both military and industrial temperature ranges (—55°C to +125°C and 0°C to +70°C). It is available in volume quantities. Your Fairchild distributor has it in stock. Write for complete specs and applications information. Ask about our other new products, too.



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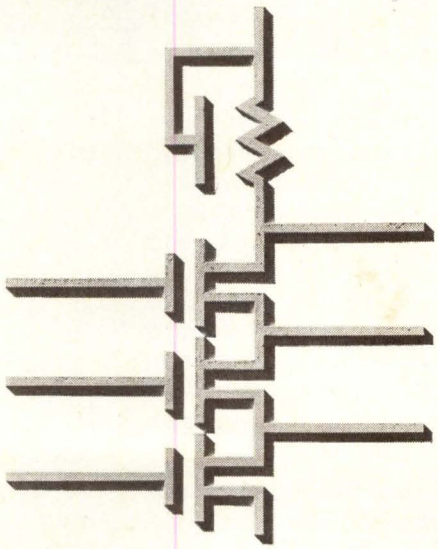
CIRCLE READER SERVICE NUMBER 112

Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **13.**

3102 MOS THREE-INPUT GATE

The 3102 is an extremely versatile three-input breadboard gate which can serve as the fundamental element in any MOS digital logic system. It can also function as an evaluation tool for determining the performance of Fairchild's line of MOS devices; or simply as a vehicle for gaining familiarity with MOS integrated circuitry. The 3102 comes in both TO-5 cans (one 3102 per can) and in 16-pin DIPs (two devices per package). The availability of all source and drain leads for each transistor provides excellent logic versatility. Input protection reduces handling problems. Power consumption is typically as low as 6mW. Operating temperature ranges from —55°C to +85°C. Volume quantities of the 3102 are now available. Your Fairchild distributor has it on his shelf. Write us for complete specs and applications information. While you're at it, ask about our other new products, too.



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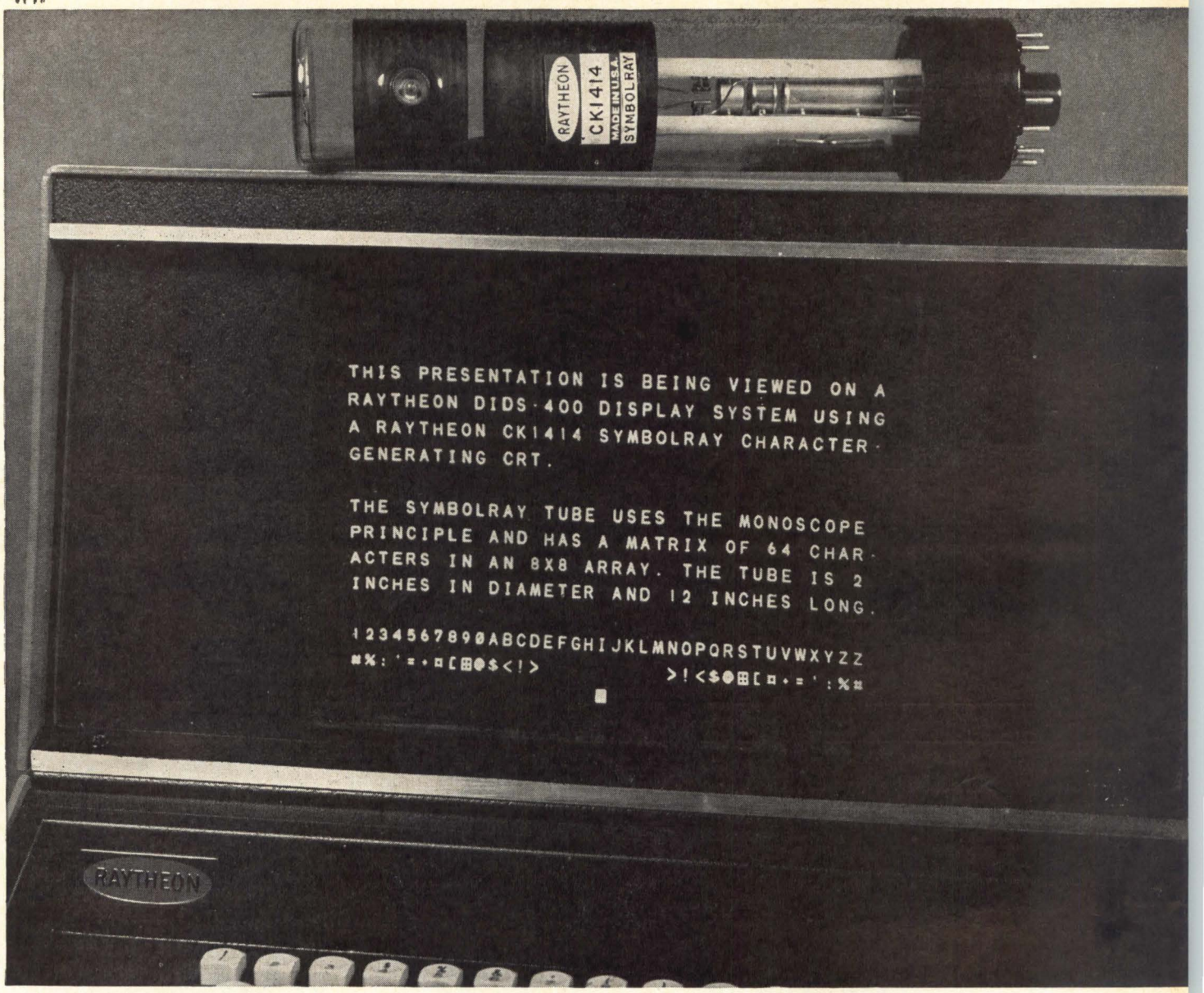
CIRCLE READER SERVICE NUMBER 113

Data Display Devices from Raytheon



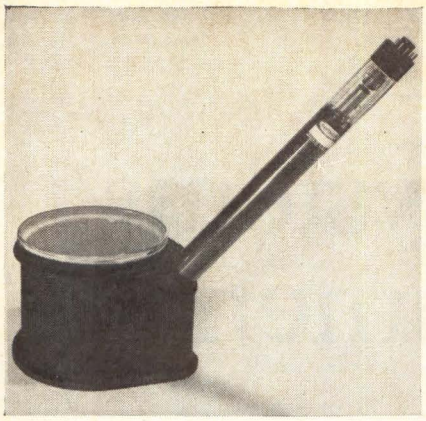
The presentation you see above was generated by a Symbolray* Cathode Ray Tube identical to the one lying on the console. A new type of monoscope, the Symbolray can generate alphanumerics from electrical signals for cathode-ray display or for hard copy print-out. The presentation here is shown on a Raytheon tube (CK1415) used in a Raytheon DIDS-400 display system.

An economical method of generating characters. Priced at less than $100 in quantities of 1,000, the Symbolray provides a more economical method of generating electronic displays than using large numbers of circuit cards.

The output of the Symbolray operating as a monoscope is obtained by electrically deflecting the electron beam to desired characters on the target and scanning them sequentially with small raster. The display cathode ray tube on which this output is viewed is scanned in synchronism. When the Symbolray method is used in conjunction with buffer-memory techniques, full messages can be displayed—as shown above. The Symbolray tube uses electrostatic deflection and focus, and is available in designs with 64 and 96 character matrices.

Raytheon's wide range of Dataray* CRTs cover the screen sizes from 7 to 24". Electrostatic, magnetic and combination deflection types are available for writing alphanumeric characters while raster scanning. Raytheon also offers combination deflection or "diddle plate" types and all standard phosphors. Or, Raytheon can meet your special CRT design requirements.

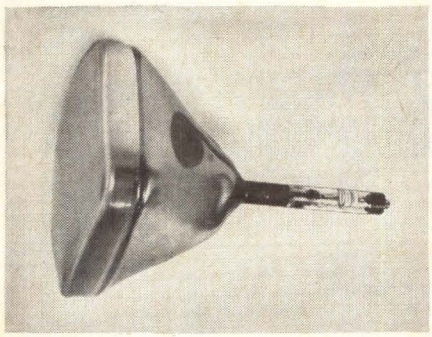
For more information—or a demonstration—call or write your Raytheon regional sales office.



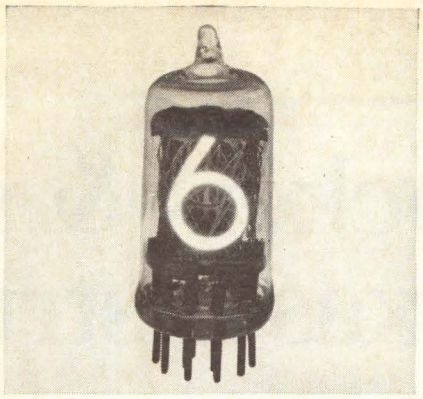
Cathode-Ray Projection Tube. A new family of Projectoray* CRTs provide high quality projection of television or other displays. As compared with more conventional projection tubes, the Projectoray provides substantial improvement in life and brightness without sacrifice in picture quality.

These devices are available in designs which utilize refractive optics or Schmidt optics, with one special design using a Schmidt spherically-curved mirror built within the cathode-ray tube.

The high light output and long life—more than 500 operation hours—are due to novel design. The phosphor screens are deposited on thermally conductive materials capable of being cooled readily by air flow or liquid cooling techniques to inhibit screen burning. The final display will provide 15 foot-lamberts on a 3-foot by 4-foot lenticular screen, permitting operation of the projection system in a lighted room.

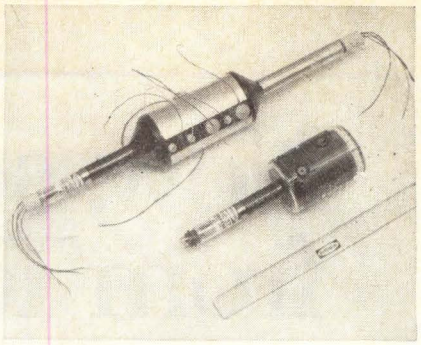


Dataray* Cathode Ray Tubes. Raytheon makes a wide range of industrial CRTs—including special types—in screen sizes from 7″ to 24″. Electrostatic, magnetic, and combination deflection types are available for writing alphanumeric characters while raster scanning. All standard phosphors are available and specific design requirements can be met. Combination deflection or "diddle plate" types include CK1395P (24″ rectangular tube), CK1400P (21″ rectangular), and CK1406P (17″ rectangular).



Datavue* Side-view Tubes. Type 8754 with numerals close to the front, permits wide-angle viewing. These side-view, in-line visual readout tubes display single numerals 0 through 9, preselected symbols, + and — signs, and decimal points. Their 5/8″ high characters are easily read from a distance of 30 feet. Less than $5 each in 500 lots, they can be supplied with lacquer coating to eliminate the need for expensive filters. Datavue types are interchangeable with NL840, 841, 842, 843, and 848 tubes.

Datavue* End-View Tubes. Raytheon makes round (CK8421) and rectangular (CK8422) Datavue indicator tubes on automated equipment capable of high production rates and top quality. The CK8422 rectangular tube is also available with decimal point, ± symbols, and in other special versions. Both round and rectangular types fit existing sockets and conform to EIA ratings. These ultra-long-life tubes are designed for 200,000 hours or more of dynamic operation.



Recording Storage Tubes. The two new designs shown utilize miniaturized guns and necks to provide high deflection and focus sensitivity, resulting in savings in coil and power supply weight and size. They provide Kiloline resolution, long storage and fast erase capability. The single-gun version is Type CK1537 and the dual-gun version is Type CK1535.

Raytheon's complete line of electrical-output storage tubes feature high resolution and non-destructive reading. Information can be written and stored by sequential techniques or by random-access writing. Complete, gradual or selective erasure is possible.

Raytheon storage tubes are readily available for applications in radar scan conversion, slow-down video, signal processing, signal enhancement, time delay, and stop motion.

Send Reader Service Card for literature on the:

Symbolray CRT	50
Projectoray CRTs	51
Datavue Indicator Tubes	52
Recording Storage Tubes	53
Dataray CRTs	54

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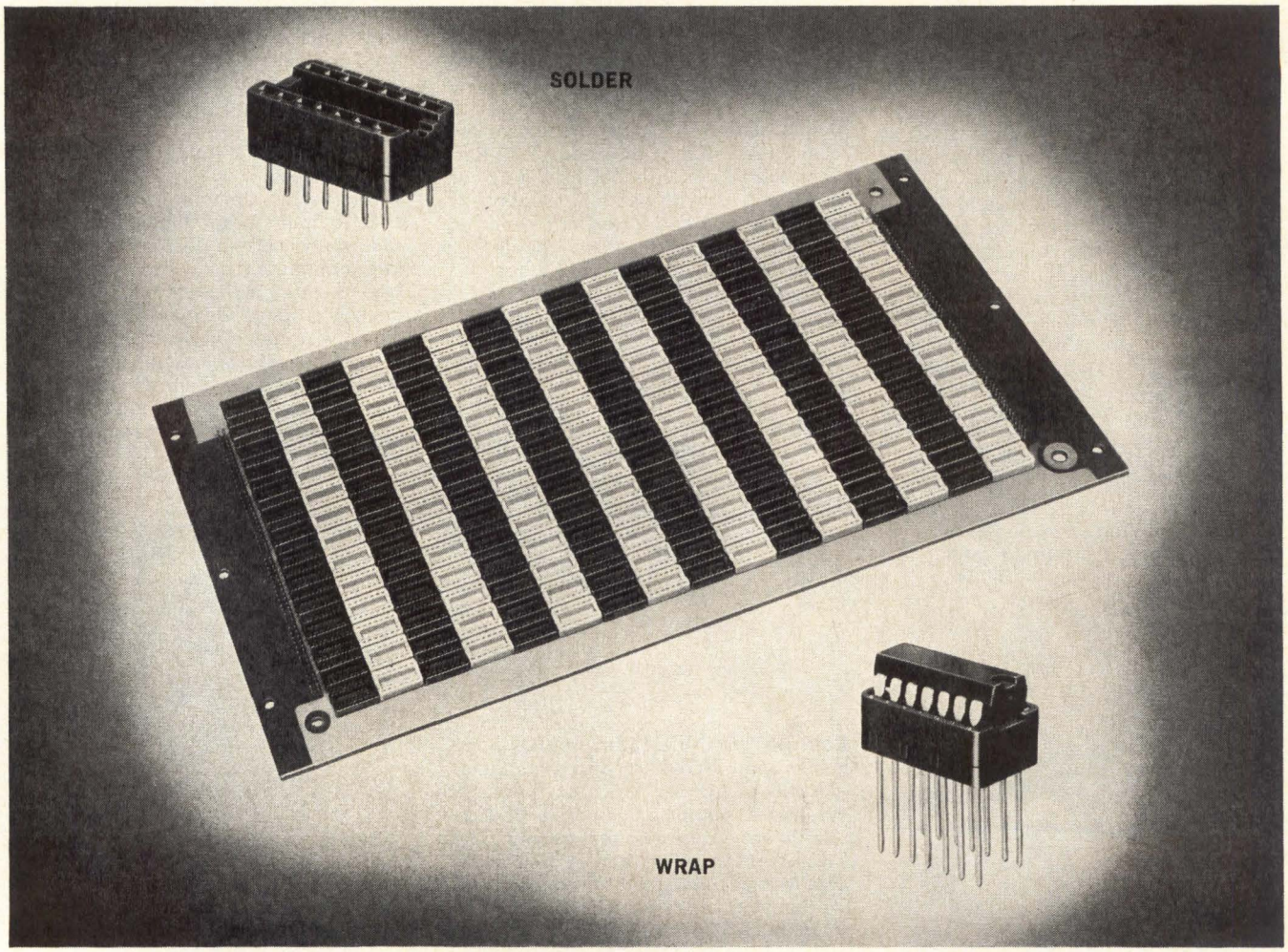

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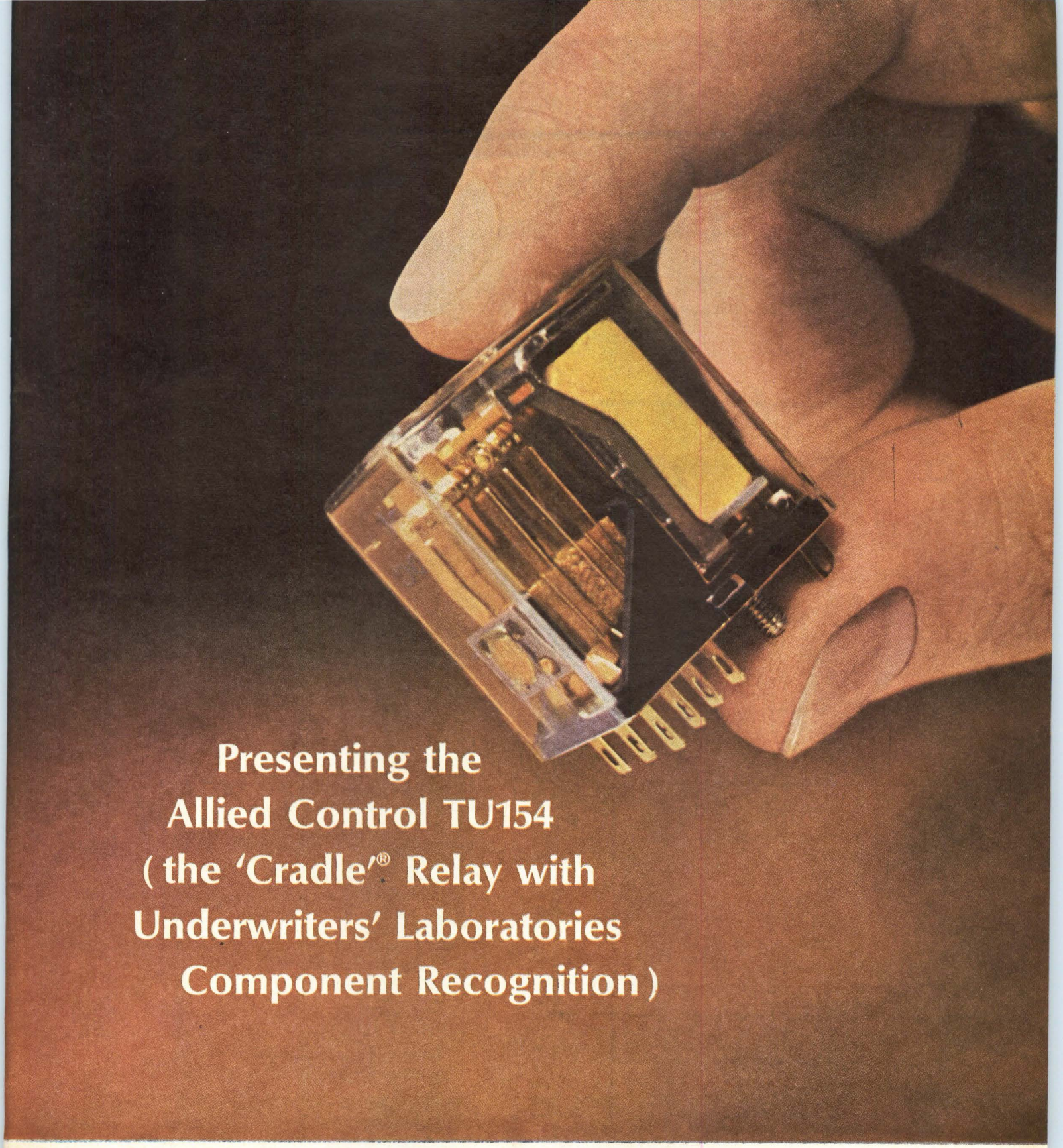

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what do you think?

This department is devoted to a continuous interchange of ideas, comments, and opinions on significant problems facing the industry. What do you think about the impact of a computer-automated world and the engineer/scientist's role in it? What do you think about engineering unions — professional societies — industry conferences? Or any significant facet of your professional life. COMPUTER DESIGN will print your views here. Write to: CD Readers' Forum, Computer Design, Baker Ave., West Concord, Mass. 01781.

CD READERS' FORUM

COMPATIBLE LOGIC SYSTEM

by
R. E. Connally

Editor's Note: The following letter and accompanying article have proven to us that an industry-wide standard for logic symbols is still a vital issue.

Gentlemen:

I have been on your subscription list since February of this year and have been following your "Readers' Forum" sequence on Logic Symbol Standard with great interest. I was disappointed when I read your October issue in which you mention your long campaign for an industry-wide standard is no longer considered a vital issue.

With new textbooks being written every day and the great proliferation of integrated circuit logic modules into commercial and consumer products, a single, easily understood logic symbol standard is vitally needed, now! To this end I would like to submit the following letter to your "CD Readers' Forum" section.

Very truly yours,
R. E. Connally
Research Associate
Radiochemical Analysis
Battelle Northwest
Battelle Memorial Inst.
Richland, Wash.

The long-standing debate over a logic symbols standard need not be resolved by the acceptance of one standard and the rejection of the other. The two logic symbols standards now in use can be compatible with each other if we follow a few simple rules:

1. The distinctive shape symbols of the Military Standard 806B will be used.
2. The rules of USA Standard Y32.14 will be followed, with certain restrictions.
   a. The 1-state will be high (H) (POSITIVE LOGIC).
   b. The logic negation symbol will also indicate that a low (L) level is required to implement an input or that an output is low (L) when implemented.
3. When signal lines are labeled with English titles we must recognize that the English title is negated whenever we pass through the logic negation symbol, in entering or leaving a logic symbol. For example in Case I of Figure 1 we negate the literal after we have applied the AND connective. In Case II we take the negation of the literals A and B before we combine them with the OR connective.

With these restrictions on the Y32.14 Standard the resulting logic diagram can't be distinguished from a logic diagram based on the 806B Standard. Those who prefer 806B can continue to use their familiar symbols. Those

who prefer Y32.14 will recognize we have utilized the wide flexibility incorporated into this standard to implement the compatible logic system. Those who have no strong attachment to either standard should welcome a settlement to the logic standards dispute if a compatible logic system were to find industry-wide acceptance.

The suggested restrictions for Y32.14 are taken from the following USAS Y32.14 paragraphs:

Either the distinctive shape or the uniform shape symbols are allowed in paragraph 1.2.1. Paragraph 6.9.1 specifies a triangular symbol for an amplifier where the gain can be of any value and of either sign. A gain of -1 is included in this set, therefore our inverting amplifier symbol can be identical to the 806B triangle. Paragraph 4.4.4 allows us to omit the small, filled (high level indicating), right triangle if it is understood we are using "Positive Logic". From Appendix D we find the low level indicator may be replaced by its opposite kind and adjacent small circle (logic negation symbol). This results in the small circles indicating a low activating level and lines without small circles indicating a high activating level as in Standard 806B.

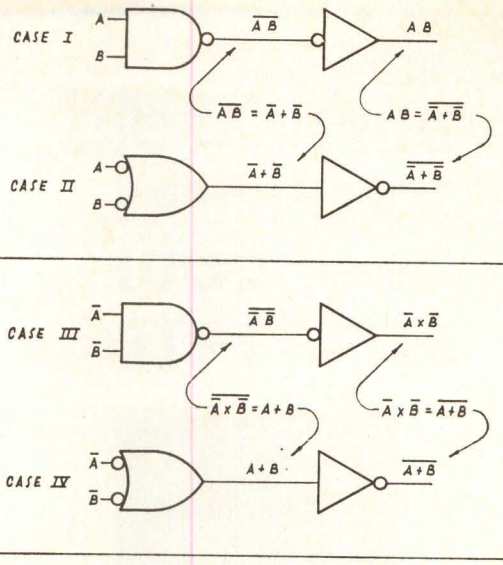
In order to obtain universal interpretation of Boolean statements taken from separate logic diagrams, it is preferred that we assign English titles as follows:

1. The assignment for gate outputs which are low when implemented should show the entire output expression as negated. And, conversely, we should not negate the entire expression for outputs which are high when implemented.
2. When the English title is a single letter the Boolean assignment is straight forward. The output of a gate, flip flop or single shot which is high upon implementation is assigned the English letter. The output which is low upon implementation is assigned the negated English letter.

As an example of preferred English titles, in Figure 1 we have shown a logic gate followed by an inverter. Let us examine this condition in more detail by use of Case I, Case II and their truth table. For Case I the ouput is low when implemented and for Case II the output is high when implemented. However, we see from the truth table that only one gate is implemented for any particular input combination, the other gate is not implemented. The output of the implemented gate will take on the level indicated by its output line (low for a small circle, high otherwise). The nonimplemented gate will have an output level opposite to that indicated by its output line. Thus, the two gates not only have opposite indicated output levels, but when one is implemented, the other is not implemented. The net result is identical electrical outputs with equal Boolean expressions. However the form of the English titled output is a function of the logician's original choice of logic symbol.

When drawing a logic diagram from a circuit diagram the logician must recognize that each gate can be represented by two equivalent logic symbols which follows from DeMorgan's Theorem as shown in Figure 2. We have found this transition to involve three steps in sequence as follows:

A FAIRCHILD "946 GATE, FOLLOWED BY AN ELECTRIC INVERTER



	A INPUT	B INPUT	GATE OUTPUT	INVERTER OUTPUT
CASE II IMPLEMENTED	L	L	H	L
	L	H	H	L
	H	L	H	L
CASE I IMPLEMENTED	H	H	L	H

TRUTH TABLE OF A "946 LOGIC GATE, CASE I & CASE II

Fig. 1. Examples of Boolean assignments.

EXAMPLES OF CONVERTING HARDWARE TO LOGIC SYMBOLS

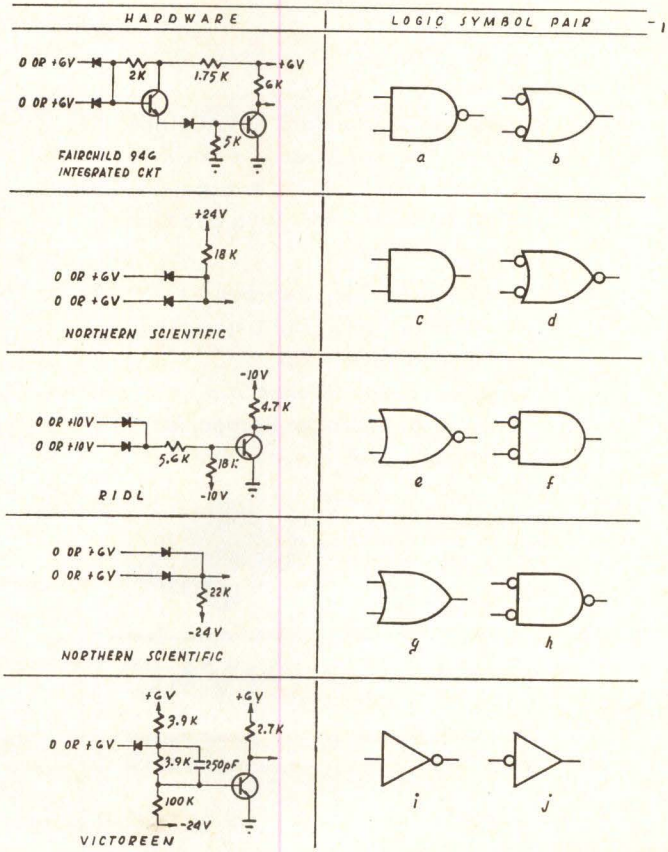


Fig. 2. Examples of converting hardware to logic symbols.

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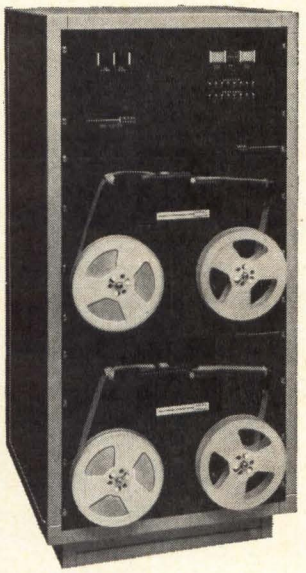

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CIRCLE NO. 9 ON INQUIRY CARD

1. The logician must first decide whether he wants to consider the logic gate as performing and AND or an OR function. Once selected, the proper symbol is drawn.
2. The inputs are analyzed one at a time to determine the electric level which implements the logic function selected. If a low (L) input implements the function, the logic negation symbol is used to show that a low (L) electric level is required for implementation. If a high (H) input implements the function, no special symbol is required on the input line.
3. The output of the logic circuit is analyzed to determine the output electric level which results when the gate is implemented. The logic negation symbol is used to indicate a low (L) output when implemented. If the implemented output is high (H) no special symbol is required on the output line.

DEFINITIONS

DeMorgan's Theorem DeMorgan's Theorem changes the form and not the value of a Boolean expression and is implemented as follows:

1. Add parentheses around all product terms.
2. Negate the entire function.
3. Change all connectives (exchange all x for + and all + for x).
4. Negate each literal.
   For example: $AB + CD = (AD) + (CD) = \overline{(\overline{A} + \overline{B}) \quad (\overline{C} + \overline{D})}$

Implement To implement is to satisfy the input conditions which are indicated by a particular distinctive shape logic symbol. A logic gate will have the indicated output level when implemented and the opposite level when not implemented.

Literal An alphabetic letter or combination of letters (sometimes an acronym or a mnemonic sequence) used to indicate a Boolean variable.

Logic Negation Symbol A small circle drawn at the point where a single line joins a logic symbol indicates a logic negation.

NAND Gate A logic gate with a low output only when all inputs are high. Symbol (a) of Figure 2.

NAND/NOR Gate Any AND or OR logic gate with a negated output. Symbols (a), (b), (e) and (f) of Figure 2.

Negation The negation of a binary variable x is the opposite of x, written either x′ (x-prime) or $\overline{x}$ (x-bar). $\overline{x}$ is also called not x.

NOR Gate A logic gate with a low output when at least one input is high. Symbol (e) of Figure 2.

Positive Logic If all signal line terminals in a logic diagram have the same pair of physical states, and if both are electric potentials or currents, and if the more positive is consistently selected as the 1-state, the diagram is said to have positive logic.

Truth Table A tabulation of all possible input level combinations and their resulting output level.

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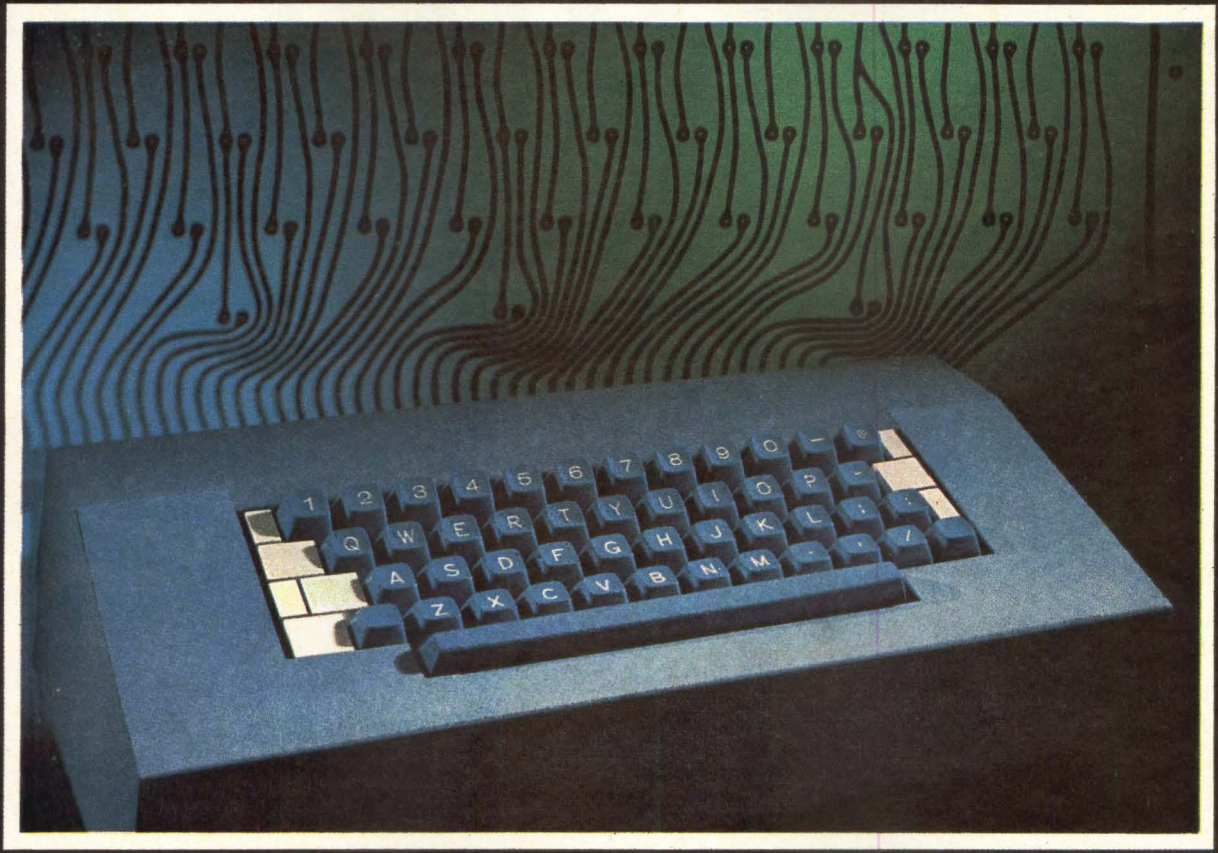

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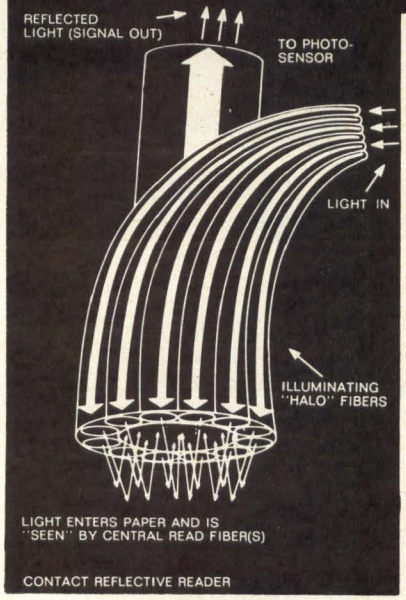

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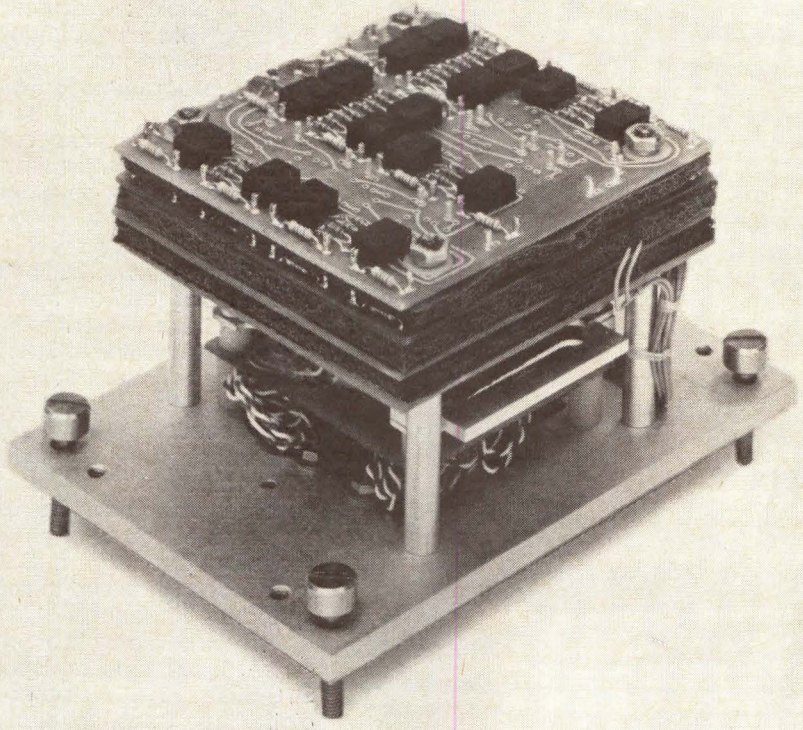

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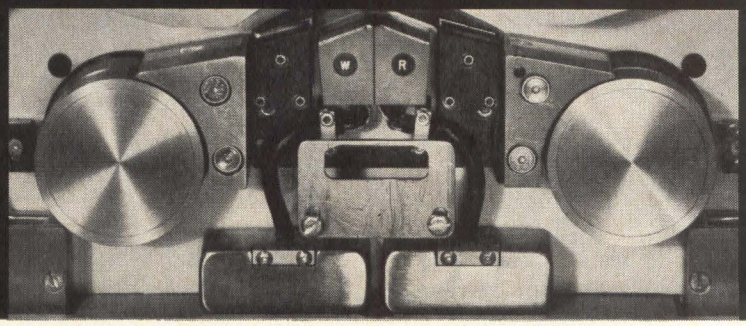
IBM STARTED SOMETHING WITH ITS DUAL-CAPSTAN TAPE DRIVE. (MIDWESTERN FINISHED THE JOB.)



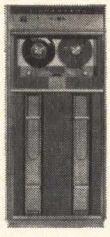
In the field of high performance digital tape transports for use with computer systems, there are really only four names to consider: IBM, Midwestern Instruments, Ampex and Potter. If it's an IBM system you're working with, there are only two logical choices: IBM and Midwestern. If data reliability to the order of 10^9 data bits is any criteria, there's only *one* choice: Midwestern's 4000 series transport.

Both IBM and Midwestern tape transport designs utilize a rapid-response, dual-capstan drive. This eliminates the necessity for programmed delays which are required by single-capstan drive systems. But not even IBM's original equipment can equal the trouble-free performance, the extended tape life and the data reliability of the patented, positive-pressure dual-capstan drive developed by Midwestern.

Midwestern's 4000 series transports cover the complete range of operating speeds required by various computer systems, from a low of 25 ips to a high of 150 ips, at bit densities of 200, 556 or 800 bpi (1600 bpi on special order). These units can be provided in either 7 track or 9 track configurations, and all are available to interface with either discrete component or integrated circuitry.

These Midwestern 4000 series transports and IBM original equipment units are the *only* field-proven IBM-compatible digital tape transports—the only units actually working on line with IBM computers at various customer installations. What's more, no other unit (*including* IBM) can guarantee data reliability in the order of one transient error per 10^9 data bits. If the 4000 series can out-perform IBM units on their own computing systems, doesn't it stand to reason they're the best choice for *your* system application?

If you'd like to hear more about our 'small wonder' 4000 series digital tape transports, just give us a call (collect) at 918-627-1111. We're programmed for fast analysis of any digital tape transport application, no matter how unique.



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CIRCLE NO. 13 ON INQUIRY CARD

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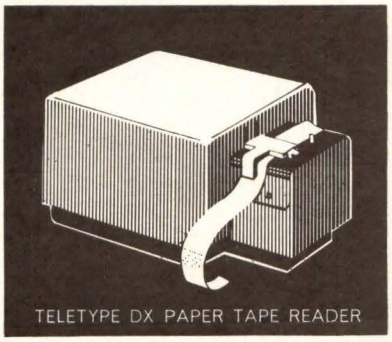


TELETYPE DX PAPER TAPE READER

OPERATING SPEEDS

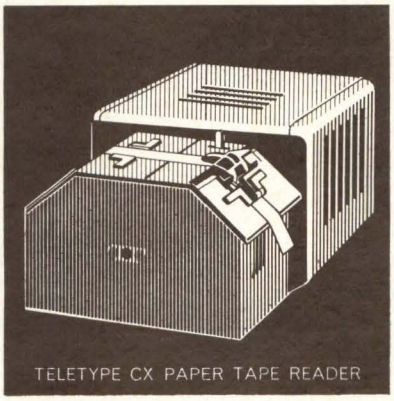
The Teletype DX reader generates parallel-wire signals. Equipped with step-by-step feeding, the DX reader operates at any speed up to 240 characters per second (2400 words per minute) without modifications.

Operating speed of the CX reader is 105 char/sec (1050 wpm). It generates parallel-wire signals that may be converted externally to sequential signals by Teletype electronic storage and conversion equipment.

Both readers are capable of sending 5, 6, 7, or 8-level coded data including the official United States of America Standard Code for Information Interchange (ASCII). They also may be equipped to control computers, buffer storage units, and other electronic register elements.

ASSURES LONGER LIFE

These Teletype readers utilize precision machined parts and rubber motor mounts to permit quieter operation and longer life. A TAUT TAPE mechanism can stop the readers until the tape is slackened. A TAPE OUT switch automatically can stop the readers at the end of tape.



TELETYPE CX PAPER TAPE READER

The CX reader has a pulse generator that provides synchronization to accurately control timing of code intelligence to associated equipment.

Both readers are available as self-contained units or can be mounted in upright cabinets with driving electronics for use as sending terminals in tape-to-tape systems as well as for many other applications.

COMBINES WITH HIGH-SPEED PUNCHES

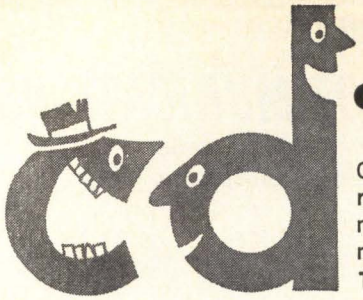
For high-speed data transmission and reception over vast distances, the CX and DX readers can be combined with a Teletype BRPE and DRPE paper tape punch. The BRPE punch operates at 105 char/sec (1050 wpm) and the DRPE up to 240 char/sec (2400 wpm).

For more about these *two talented tape terminals,* contact: Teletype Corporation, Dept. 71A, 5555 Touhy Avenue, Skokie, Illinois 60076.

machines that make data move

TELETYPE

CIRCLE NO. 17 ON INQUIRY CARD



commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

THE IMPACT OF L. S. I. ON COMPUTER MEMORIES

by
T. PAUL BOTHWELL
Vice President, Engineering
Computer Controls Division
Honeywell, Incorporated

Computational capability has developed at an astonishing rate during the brief life of the electronic digital computer. Figure 1 shows than since 1959, computing power per dollar of first cost for small scientific computers has not only been increasing, but accelerating. It constitutes a straight-line trend on a logarithmic scale — a 200-to-1 improvement during the past eight years. Computing power is the word length multiplied by the average number of instructions (weighted) executed per second in a machine having a 4,000-word mainframe with minimum paper tape I/O.

Can the performance per computer dollar go on increasing at this pace? Not indefinitely. History tells us that all products eventually level off. Has that time come for computers?

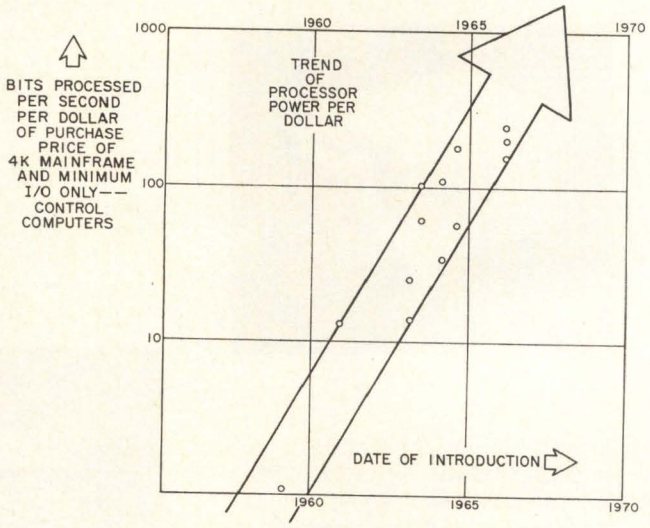


Fig. 1

Two Important Power Factors

Much of the gain in computing power per dollar has come about through the evolution of the magnetic core memory. During the dozen years that core memory has dominated main memory design, both cost per bit and cycle time have been reduced by a factor of ten, which represents a gain in memory value of 100 during these years. Another factor in gain of computer power, of course, is the lowering cost and rising speed of semiconductors. This achievement, together with the ingenuity of the logic designers, has greatly increased value in the non-memory part of computers, and has contributed to the growth in memory value.

Memory costs will continue to reduce. Core memory will probably give way to the plated wire memory. But even when we consider the substantial cost and performance improvements this will offer, it is hard to foresee another hundred-to-one reduction.

L.S.I. As A Factor

It seems, then, that the trend of the last few years may not continue beyond this decade unless something new enters the picture. And that "something" may be future developments in integrated-circuit technology — conveniently lumped into the term "L.S.I." As used here, the term applies to a chip containing more than 100 logic gates.

As I/C technology advances, circuits are growing more and more complex. We measure this complexity by the number of logic gates per chip (Fig. 2). A chip with up

DATA COMMUNICATIONS

equipment for on-line, real-time processing

keeping track of the ins and outs

Teletype data communications equipment serves as the terminals in a variety of computer systems. Many systems designers specify Teletype terminal equipment because they have found the sets to be the most reliable, versatile, and economical available.

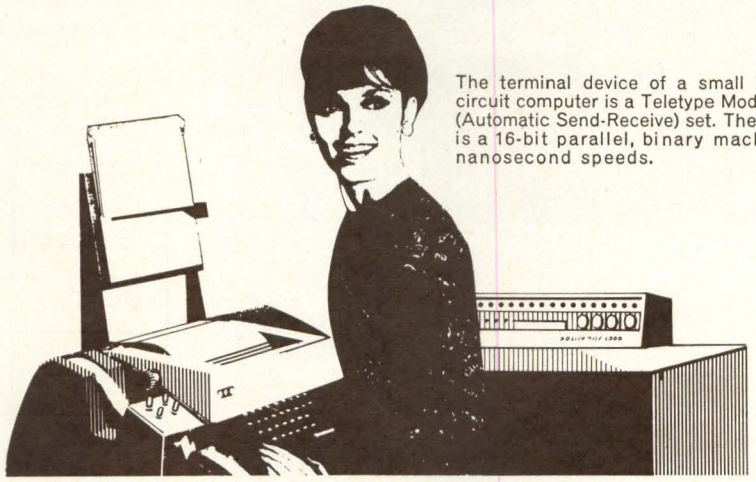
The examples below point up the many capabilities of Teletype equipment as used in a number of different computer systems.

AIDS SCIENTIFIC COMPUTATIONS

Primarily designed for control applications and scientific computations, a computer that uses monolithic integrated circuits can be operated alone, as a multiprocessor system, or as a satellite to a larger computer system. A Teletype Model 35 KSR (keyboard send-receive) set is the system's terminal. It uses an 8-level code compatible with the United States of America Standard Code for Information Interchange (ASCII).

AIDS BILLING AND INVOICING

An electronic billing and invoicing machine uses a Teletype Model 33 ASR (automatic send-receive) set to provide on-line communications involving a variety of accounting data. Continuous pin-feed invoice forms with multiple copies are used in the system. In addition, a punched by-product tape is prepared for further analysis by management.



The terminal device of a small integrated circuit computer is a Teletype Model 33 ASR (Automatic Send-Receive) set. The computer is a 16-bit parallel, binary machine with nanosecond speeds.

Users of a time shared computer system can contact the computer for service and inputs of all instructions, data, and plot programs through standard Teletype equipment. The computer processes the data and transmits via a Model 33 ASR set a complete plot program, including identification codes for that particular plotter and output signals for remote on-line plotting.

A compact 16-bit real-time computer provides high-speed data acquisition and control. The system multiplies and divides faster, has a faster throughput and costs less than many larger systems. It uses a Teletype Model 33 ASR set as its terminal.

AIDS TO YOUR SYSTEMS

These are only a few of the many Teletype equipment applications in both large and small computer systems. To learn how Teletype equipment can aid the systems you're designing, send for our brochure, "ALL ABOUT TELETYPE EQUIPMENT." Contact: Teletype Corporation, Dept. 71A, 5555 Touhy Avenue, Skokie, Illinois 60076.

machines that make data move

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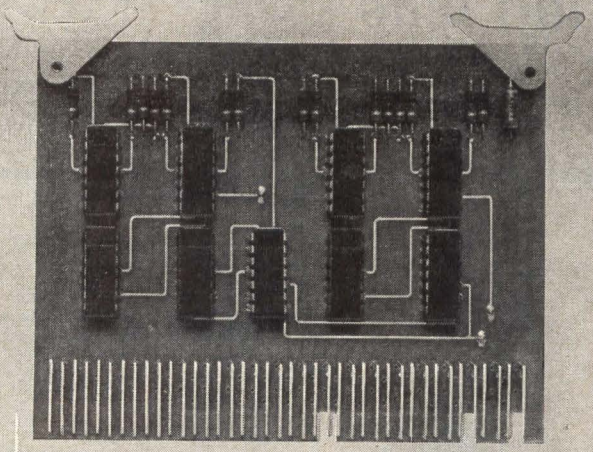

The complete MicroVersaLOGIC line gives you all the ready-made building blocks you need for anything from a register to an entire digital system—with a 7:1 size reduction because of MicroVersaLOGIC's high density IC packaging.

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to 10 gates is simply an integrated circuit; 20 or 30, functional array; close to 100, M.S.I. L.S.I. is still a few years away, but is certainly coming, and it is interesting to speculate its impact on memories.

By its nature, L.S.I. is applicable where large numbers of similar circuits are required, where interconnection between the circuits can be made all on the same wafer of silicon and where it offers the lowest unit circuit cost. Industry sources project costs as low as a penny per gate in five or ten years.

Now, remembering that two gates can make a flip-flop, and that a flip-flop is still one of the fastest and simplest memory elements ever devised, it is clear that L.S.I. will be used for the construction of memories.

Many different types of memories are used in computers today, however, and many more have been suggested for the computers of tomorrow. Which of these are likely to make effective use of L.S.I.?

Although many L.S.I. enthusiasts would disagree, I believe it will be a long time before L.S.I. can achieve the performance and economic advantages of magnetic main memories and mass memories. The development of batch fabricated magnetic devices, represented by flat film and plated wire, the extreme desirability of the non-volatile storage properties, and the high level of technological momentum in magnetics combine to provide

DEFINITIONS

	INTEGRATED CIRCUIT	FUNCTIONAL ARRAYS	MSI	LSI
NO. OF GATES	1–10	8–30	30–100	100
NO. OF COMPONENTS	5–50	50–300	150–1000	500
NO. OF PINS	14–30	14–50	14–50	30–100
INTERNALLY CONNECTED	NO	YES	YES	YES

Fig. 2

formidable obstacles to the integrated circuit as the primary memory device.

In contrast, however, application of L.S.I. to peripheral buffers and the more specialized memories is not only technically feasible today, but will offer increasing advantages during the next decade. Since cost per bit of a core memory rises steeply as the size is reduced, core memory will soon lose its cost advantage for small memories. Moreover, many of the more specialized memories, such as read-only and scratch-pad units, can make good use of the very high speed available from L.S.I. technology.

The advent of L.S.I. is going to stimulate the introduction of more specialized memories into computer systems. Specialized memories, such as scratch-pads, read-only memories and content addressable memories, have long been attractive to the computer designer, but

DATA COMMUNICATIONS

equipment for on-line, real-time processing

...at the press of a button

Time. In today's data communications and processing systems it is measured in microseconds. And Teletype R&D engineers know it. For instance, look at the Push Button Data Generator they have developed to cope with the situation.

The PBDG is an automatic data preparation unit that simplifies and speeds the flow of fixed data. By preprograming fixed data into the PBDG, you can automatically print up to 24 alphanumerics and other characters *by pressing a single button.*

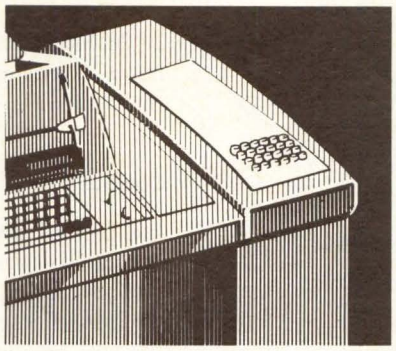
AIDS COMPUTER OPERATION

The PBDG can be used wherever there is a need for automatic handling of repetitive data. For instance, in a time sharing system, the intricate instructions needed to activate the computer for a particular user can be programed into the PBDG, and transmitted automatically to the computer merely by *pressing the appropriate button.*

In addition, the PBDG offers many important advantages to data communications and processing operations. Information is stored and reproduced in the same form every time at the press of a button. Data is easily programed or reprogramed for automatic transmission of fixed data. This saves time, saves key strokes, and eliminates errors.

GENERATES 288 CHARACTERS

Operating on either a 5 or 8-level code, the basic Teletype PBDG unit consists of 12 pushbuttons capable of generating a total of 288 characters. The PBDG can be used as a self-contained unit or combined with other Teletype equipment to punch paper tape, print page copy, or transmit to a remote unit.



Cabinet at right of this Teletype Model 35 ASR set houses control panel and circuitry of Push Button Data Generator

Programing is made and/or changed simply by movement of push-on type terminals. No technical skill is needed to make or change a program. The unit also may be programed to stop on any predetermined character position. This permits insertion of variable information from a keyboard. After the variable data has been entered, automatic entry of fixed data is continued *at the press of a button.*

AVAILABLE IN SPECIAL CABINET

Where space permits, the PBDG control panel and its associated electronics can be housed in a Teletype printer console. When more than 24 pushbuttons are needed, special cabinets can be provided that contain as many as 96 buttons in units of 12.

For more information about transmitting your data *at the press of a button,* simply request our PBDG data sheet by contacting: Teletype Corporation, Dept. 71A, 5555 Touhy Avenue, Skokie, Illinois 60076.

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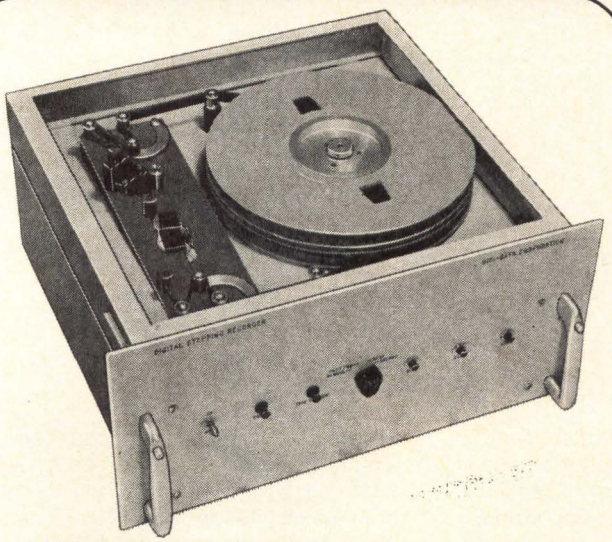

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MEMORY REQUIREMENTS

Memory Type	Price Range Cents/Bit
Mass Memories	0.5 to 0.01
Main Memories	5 to 10
Peripheral Buffers	10 to 25
Specialized Memories	10 to 100
Read Only Memories	
Control Memories	
Scratch Pads	
Content Addressable Memories	

Fig. 3

because of their excessive cost (Fig. 3) have been bypassed in favor of more main memory and software devices. Such memories can have dramatic effects on overall computer power and will have a significant effect in maintaining the power-per-dollar trend.

L.S.I., by virtue of the great reduction in the length of interconnections and the even smaller geometry of the transistor junctions, will permit faster logic switching in the computer, thus increasing the demand for more memory speed. The need, therefore, to relieve the main memory of as much mundane work as possible will be intensified. This, in turn, will increase the need for more specialized memories to take over suitable functions.

Conclusion

L.S.I. will have primary impact in changing our approach to memory and computer system organization, resulting in many more economic, specialized memory devices. These devices, in turn, will modify our views on the role and mode of use of the memory, software logic and system architecture.

Computer architecture has really changed very little in a decade — in fact, almost two decades. The early concept of a single main memory into and out of which all information is pumped as it is stored and processed has not changed appreciably. Ten years or more of design has been devoted primarily to optimizing that principle and re-optimizing it in the light of new components and new application knowledge.

L.S.I. will change many of the rules which have been axioms for system architects for ten years. The availability of economic, fast, specialized memories will gradually modify the basic single memory concept which has held sway so long; and this will lead us into a new era of computer power in the 1970's. We are a long way from the end of the road in computer power per dollar.

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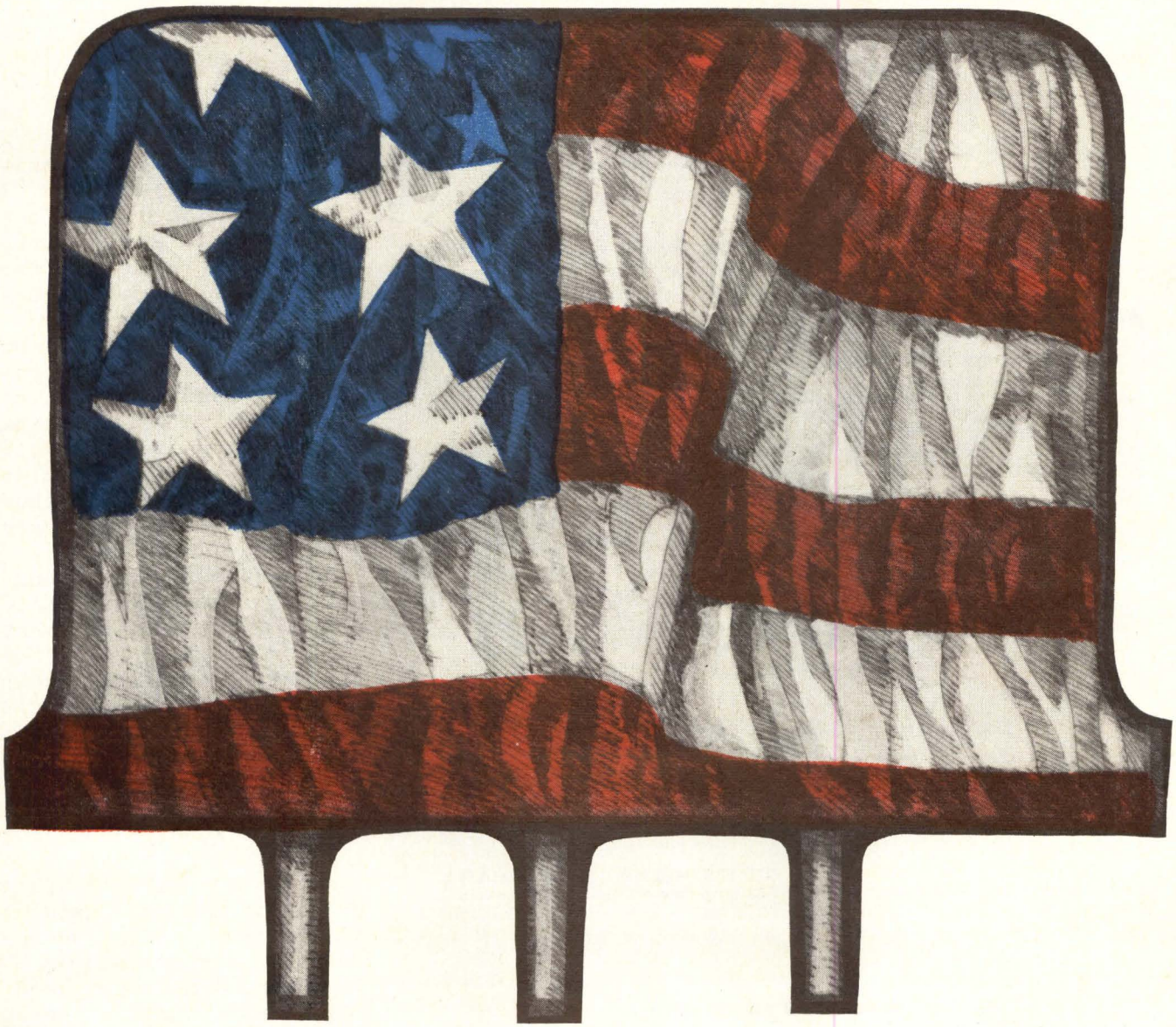
What this country needs is a good 50¢ phototransistor.



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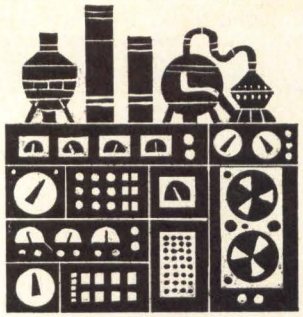

INDUSTRY NEWS

PHOTO-DIGITAL STORAGE SYSTEM—The Atomic Energy Commission recently completed installation of what is claimed to be the world's largest computer storage system at the University of California Lawrence Radiation Laboratory. More than one trillion bits of information—enough data to provide the average person with nearly 200 years of uninterrupted reading—can be stored by this photo-digital storage system which was built for the AEC by International Business Machines Corporation under a $1 million contract. Any item in the system's file is directly accessible upon request and can be retrieved in seconds without scanning other items in the memory. Information is handled entirely automatically within the system.

When fully activated, the IBM Photo-Digital Storage System will store and retrieve information for a network of interconnecting computer systems at the Livermore Laboratory. This network—said to be one of the most powerful time-sharing data processing facilities in operation—stores and analyzes data obtained from large-scale computations.

The photo-digital system stores information at very high densities by using a beam of electrons to record the data on 1.3- by 2.7-inch "chips"—pieces of high-resolution, photographic film. Nearly five million bits of information can be packed on a single film chip.

The chips are positioned in a vacuum chamber for recording, and the information is "written" during repeated sweeps of the beam across the chip surface. The beam, in effect, paints data as combinations of dark and clear spots corresponding to the zeros and ones of the binary language of the computer. Sensitive control devices in the recorder continually align and adjust the beam.

The photo-digital system houses its own film-processing "laboratory" which develops the film chips under automatic control. Chips are treated individually with chemicals, then washed and dried to prepare them for filing.

Recorded chips are transported and stored in protective plastic cells somewhat smaller than a cigarette package. A single cell holds 32 chips and could store enough information to process a complete payroll for a 30,000-man company.

Cells are blown through transport tubes connecting the processing stations to the storage area. This pneumatic transport network is designed for two-way travel at speeds reaching 25 feet per second.

In the storage area, cells

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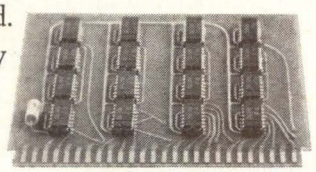

These will cost you less.

And save yourself the time and cost of making your own: designing, assembling, testing, new procedures, new equipment, new personnel, additional training, to say nothing of the added paper work.

If you're building systems, you must have better things to do than go into the module assembly business. Such as reading our J Series catalog.

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SDS

Scientific Data Systems, Santa Monica, California

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FACT'S flexible. Adaptation to new projects requires only new tapes or test decks, plus the appropriate adapter cables.

It's completely modular — designed for easy expansion and adaptable to a wide variety of test conditions.

FACT is now reporting wiring discrepancies for many commercial military and space programs. And producing significant cost/schedule savings.

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CIRCLE NO. 22 ON INQUIRY CARD

are placed in individual compartments of movable trays resembling a stack of egg crates. A computer keeps track of all records stored in the trays and initiates requests for the retrieval of information.

Individual cells are withdrawn from any location in the file and pneumatically delivered to a reader where the selected chip is read by a high-speed flying spot scanner. Data is automatically checked and corrected before it is transmitted to the computer.

The photo-digital system operates under the control of a stored-program processor similar to the control computers which regulate an automatic assembly line or traffic network. This control processor is part of the system and sets in motion the many discrete mechanical, electrical, and chemical processing steps that make up such activities as positioning the storage trays or developing the film chip.

Requests are translated into action by the processor in response to a program that speeds the flow of events by allowing many independent actions to occur at one time in a variety of combinations. The control program also acts as a tool for continuous, automatic diagnosis of the system's performance.

A second photo-digital system is scheduled for the Lawrence Radiation Laboratory facility located on the Berkeley campus of the University of California. Somewhat smaller in capacity, this system will store masses of data used to track and identify atomic particles.

Both systems were developed by IBM's development laboratories in San Jose, Calif.

* * *

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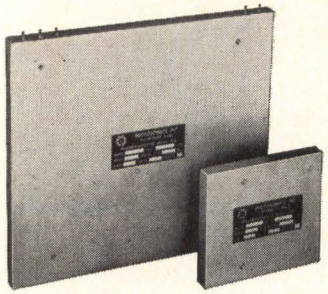
We need Senior Development Engineers and Programmers. Write to Mr. Bruce Ferris.

CIRCLE NO. 23 ON INQUIRY CARD

DELAY LINES



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Systems provide for the delay or storage of both analog and digital signals and are available to handle all modes of modulation (RZ, NRZ and Bipolar). Output signals are available in either clocked or unclocked signal.

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REPORT ON MEETING OF IFIP GENERAL ASSEMBLY IN MEXICO CITY. At the meeting of the General Assembly of the International Federation for Information Processing (IFIP) held recently in Mexico City two further countries were admitted to membership — Yugoslavia and Cuba. This brings the number of countries represented on IFIP to 28. Professor R. Tomovic is the delegate for Yugoslavia and Mr. Rual Alvarez Marcer for Cuba.

President-elect

Professor A. A. Dorodnicyn of the U.S.S.R. has been elected to succeed Dr. A. P. Speiser as President of IFIP following IFIP Congress 68. A second Vice-President—Mr. D. Chevion of Israel was elected and given responsibility for co-ordinating and supervising the activities of the IFIP special interest groups and IFIP Technical Committee 3 (TC3—Education). Professor L. Lukaszewicz of Poland will continue as Vice-President and be responsible for the activities of the other IFIP Technical Committees.

IFIP Congress 71

Yugoslavia will be the host country for IFIP Congress 71 which will be held in Ljubljana.

Administrative Data Processing Group

The bylaws of the Administrative Data Processing Group were approved by the General Assembly and the Group will become operative when at least five member countries have ratified the bylaws and appointed delegates to serve with the Group.

New IFIP technical committee formed

A new IFIP technical committee—TC 4—has been formed. Its area of interest will be medical data processing and Professor F. Gremy of France has been elected its first chairman.

Joint Conference

In association with other professional organizations, IFIP are to sponsor a number of joint conferences over the next two years. The first will be held in June 1968 at Novosibirsk in the U.S.S.R. and the subject will be "Optimal programming in process control and economics". In June 1968, an IFAC/IFIP conference on the state of the art in the application of control computers will be held in Toronto; and plans are being considered for an IFAC/IFIP conference in 1969 on programming languages for numerically-controlled machine tools. In September 1969 a conference on hybrid computing will be held in Munich, Germany in association with the A.I.C.A.

SEEING IS BELIEVING—Work pioneered by IBM and continued by IBM, United Aircraft, and General Motors has resulted in the production of holograms of objects that do not exist. Computers, after being programmed with information about what an object should look like, calculate the interference pattern that the object would produce. This pattern is recorded and transferred to a transparency. When the transparency is viewed in monochromatic light, a three-dimensional image of the "object" appears. So far the images have been of relatively simple objects like letters or geometrical figures, but the technique should have wide application. For example, designs of objects could be displayed and studied in three dimensions before being built. Computers also can be used to translate holograms of very large or very small objects into useful display sizes. Several possible uses of this technique have already become apparent to researchers. An acoustical hologram of a

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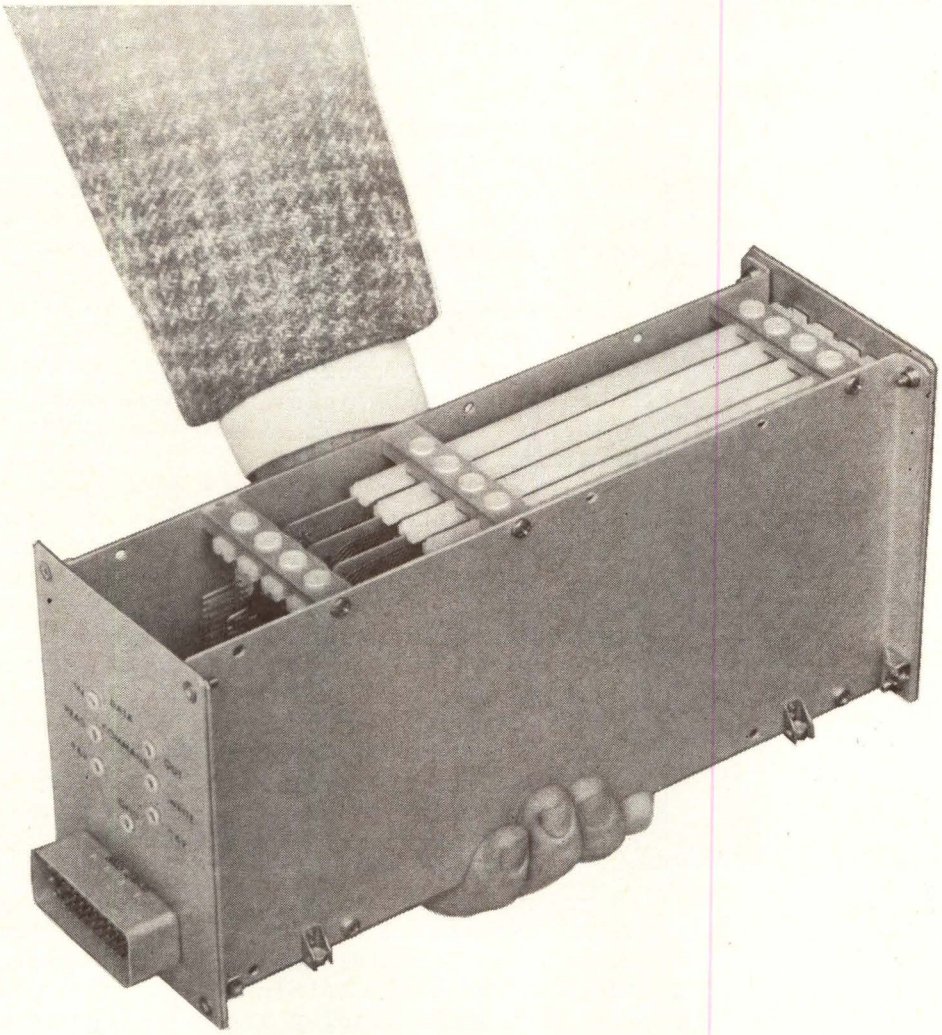

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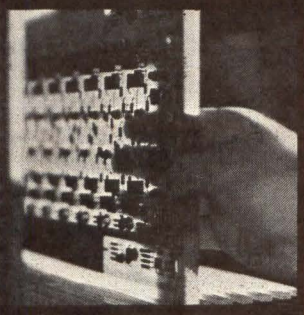
large object, like a submarine or part of the ocean floor, can be made with long wavelength sound energy. A computer calculates the interference pattern that would have been formed with short wavelength light energy and produces the transparency of this pattern. In the developed hologram, the object would be small enough to study in an ordinary room. It is also possible to reverse the process and to enlarge a hologram made of a microscopic object. In this case, the original hologram would be made with radiation having a very short wavelength. The computer would calculate the interference pattern for longer wavelength radiation, and the result would be an enlarged three dimensional image of the object.

AUTOMATIC TICKET AGENCIES—Computicket Corporation, a subsidiary of Computer Sciences Corp., has awarded a $3.3 million contract for production of electronic terminals that will serve as neighborhood box offices in the company's computer-based instant ticketing system. The terminals will be manufactured by Wyle Laboratories, El Segundo, Calif., to specifications developed by Computicket engineers. The terminals will be installed in neighborhood markets, banks, and other retail and commercial outlets, and will be linked by private communication lines to a central computer complex. The units will be used to request seats to sports, theater, and other entertainment events, and to print the actual admission tickets for these events. Television-like screens at each terminal will instantly display the computer's response to requests. The development of the Computicket terminals is said to have a significance extending beyond the ticketing business. The units are flexible enough in their design to satisfy the inquiry, response and high speed printing requirements of a number of other important applications; for example, travel and hotel reservations, inventory control and credit checking. The first terminals produced will be installed in the Southern California Computicket network, which will begin operation next spring. Similar networks will be established in New York and other metropolitan areas throughout the United States in 1968 and 1969. The ultimate plan is to form a nationwide Computicket network.

RCA TO BUILD $11.7 MILLION COMPUTER PLANT—RCA has announced plans to build a 220,000 square-foot facility in Marlboro, Mass. for the engineering and production of computer peripheral equipment. Construction of the new plant, to be located on a 128-acre site on Interstate Highway 495, will begin in 1968, with the target date for initial occupancy scheduled for early 1969. A temporary 50,000-square-foot facility has been leased near Framingham, Mass., to recruit and train the personnel who will form the nucleus of the permanent operation four miles away. Engineering efforts will begin at the Framingham plant around January 1968. Initially, a limited number of different types of electronic data processing devices for RCA's Spectra 70 systems will be assembled at the Marlboro plant. At full operation, a broad range of computer peripheral devices will be designed and manufactured. According to James R. Bradburn, Vice President and General Manager of RCA Electronic Data Processing, the new plant will be built with an eye toward additional expansion in the early 1970's.

CIRCLE NO. 27 ON INQUIRY CARD



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We know of more than 300 systems that couldn't afford not to have the DATA 620/i, because that's how many we sold in the first six months. We'd be happy to show you what it can do for your system, or at least send you our illustrated brochure full of functional and operational information. Just call or write.

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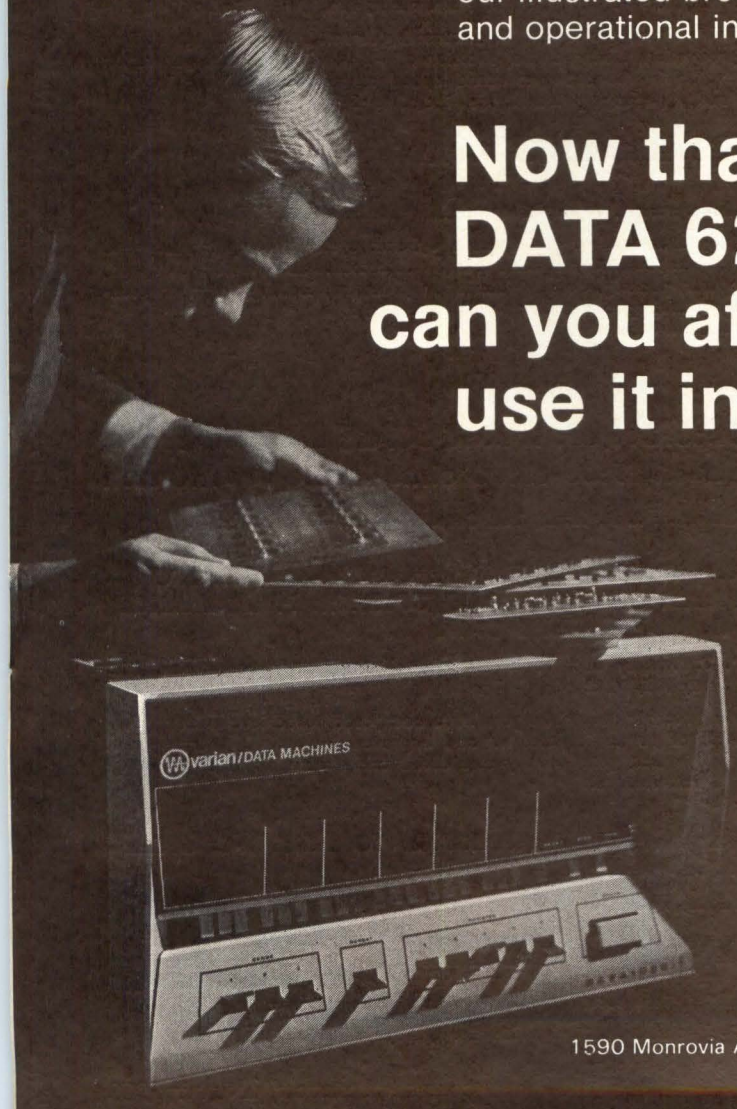

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1968 SOLID-STATE CIRCUITS CONFERENCE

University of Pennsylvania and Sheraton Hotel

Philadelphia, Pa., Feb. 14, 15, 16, 1968

TECHNICAL PROGRAM SUMMARY

Reflecting the extraordinary growth of solid-state technology, this year's International Solid-State Circuits Conference has scheduled more papers than ever before — 15 formal sessions comprising 78 invited and contributed papers authored by over 140 scientists, engineers and educators from here and abroad will be presented at the University of Pennsylvania.

In the evenings, informal discussions will again be held at the Sheraton Hotel. Twelve sessions, with over 80 participants, are on the agenda.

Those daytime sessions and evening informal discussions of prime interest to Computer Design *readers are listed in the following schedule.*

FORMAL OPENING — Wed., 1:45-2:45 p.m., Irvine Auditorium

KEYNOTE ADDRESS: MAKING INTEGRATED ELECTRONICS TECHNOLOGY WORK

R. N. Noyce, Fairchild Semi-Conductor, Mountain View, Calif.

Applications of large-scale integration require solutions to technical, organizational, economic and logistic problems significantly more complex than those in applications of today's integrated circuits. The solution will require greater flexibility and communication between vendor and user.

SESSION III — INVITED: THE FUTURE OF INTEGRATED ELECTRONICS IN SYSTEMS — Wed., 2:50-5:30 p.m., Irvine Auditorium

Moderator: R. L. Petritz, Texas Instruments, Inc., Dallas, Texas

Progress in integrated electronics has had a widespread impact on the electronics industry prompting a critical appraisal of its productive application to real systems. In the keynote address, technology problems and their interface with customers were underscored. The following invited papers will report on allied problems. The first three will discuss the application of the technology to three major systems: computers, telecommunications and consumers. The concluding presentation will consider a new approach to integrated electronics through recent discoveries of bulk phenomena in semiconductors.

3.1: THE IMPACT OF LSI IN LARGE COMPUTER SYSTEMS

M. O. Paley, IBM Corp., Menlo Park, Calif.

LSI technology offers significant performance gain in large computers through higher-speed switching and higher circuit density. The challenge to the system designer is to balance this increased logic with high performance memory, input-output considerations and architectural innovations.

3.2: INTEGRATED ELECTRONICS IN TELECOMMUNICATIONS

G. C. Dacey, Bell Telephone Laboratories, Inc., Holmdel, N. J.

Integrated electronics offers a new approach to the design of telecommunications systems. This factor and related problems will be discussed in this paper. The touch-tone dial system will be assessed as a system application.

3.4: SOLID-STATE BULK PHENOMENA AND THEIR APPLICATION TO INTEGRATED ELECTRONICS

R. S. Engelbrecht, Bell Telephone Laboratories, Murray Hill, N. J.

Bulk phenomena in semiconductors can be used to achieve oscillation, amplification, modulation, detection, logic decisions, pulsed-train generation and other functions. Methods for combining these phenomena in single structures for achieving integrated electronic functions will be discussed.

INFORMAL DISCUSSIONS Wed., 8:00 p.m., Sheraton Hotel

1: HIGH SPEED DIGITAL INTEGRATED CIRCUITS

(West Ballroom)

Moderator: D. Chung, Texas Instruments, Inc., Dallas, Texas

Two general topics will be discussed: current problems in the design, production, testing and application of 1-2 ns ICs, and next generation circuits in the sub-nanosecond speed range with emphasis in high density packaging techniques, including LSI.

4: WHERE MOS IS TODAY

(Pennsylvania East)

Moderator: H. C. Lin, Westinghouse Electric Corp., Elkridge, Md.

The advantages of static versus dynamic systems, complimentary and non-complimentary circuits will be discussed. Such factors as speed, power, packing, density fabrication problems, loading, interface problems, and specific-end use will be assessed.
Panel Members:

SESSION IV: LARGE-SCALE INTEGRATION, Thurs., 9:00-12:00 a.m., Irvine Auditorium

Chairman: R. A. Henle, IBM Corp., Hopewell Junction, N. Y.

4.1: TRANSISTOR-TRANSISTOR LOGIC WITH HIGH PACKING DENSITY AND OPTIMUM PERFORMANCE AT HIGH INVERSE GAIN

B. T. Murphy and V. J. Glinski, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

Very narrow epitaxial layers have been used to achieve packing densities of 10^5 logic gates/in^2 and improved logic circuit performance. High inverse gain, usually considered undesirable, provides improved TTL performance.

4.2: A FLEXIBLE APPROACH TO EMITTER-COUPLED LOGIC ARRAYS

M. D'Agostino, RCA, Somerville, N. J.; A. Feller, RCA, Camden, N. J.

A CML array fabrication approach which originated in a systems-circuit study will be described. The design attempts to merge high-speed computer system requirements and solid-state fabrication capabilities, incorporating design automation techniques.

Chairman: R. A. Henle, IBM Corp., Hopewell Junction, N. Y.

4.3: LSI SUBSYSTEMS ASSEMBLED BY THE SILICON WAFER-CHIP TECHNIQUE

C. G. Thornton, Philco-Ford Corp., Blue Bell, Pa.

This paper will cover techniques for face-down bonding of individual LSI chips onto a high-density silicon interconnection substrate, projected to permit the design of several large multi-chip subsystems.

4.4: TOTAL DESIGN OF HIGH-SPEED COUNTERS: PROCESS TO SUB-SYSTEM

R. C. Foss and J. S. Brothers, The Plessey Co., Ltd., Northants, England

High-speed counting sub-systems in which process technology, circuit and logic design are optimized separately and together will be described. A current steering counter element achieves 10 MHz/mW at a 350-MHz counting rate.

4.5: AN APPROACH TO SMALL MACHINE DESIGN IN LARGE-SCALE INTEGRATION

C. S. Gurski, IBM Corp., Endicott, N. Y.; W. R. English and G. G. Langdon, Syracuse University, Syracuse, N. Y.

This paper will consider the large-scale integration part-number problem by consolidating the development of several small machines A portion of the physical embodiment of this concept was constructed in large-scale integration.

INFORMAL DISCUSSIONS
Thurs., 8:00 p.m., Sheraton Hotel

7: LSI IMPLICATION IN COMPUTER ORGANIZATION
(West Ballroom)

Moderator: L. M. Spandorfer, UNIVAC/Sperry Rand Corp., Blue Bell, Pa.

The problems in making hardware/software tradeoffs and introducing new system organizations for the purpose of accommodating LSI will be discussed.

10: WHICH MEMORY TECHNOLOGY FOR FUTURE SYSTEMS
(Pennsylvania East)

Moderator: J. H. Wuorinen, Bell Telephone Labs., Inc. Murray Hill, N. J.

The range of memory applications expected in future data-processing systems will be explored and the relative merits of ferrites, thin films, semiconductors and optics for this range of applications evaluated.

12: IMAGING MOSAIC SENSORS AND DISPLAYS
(Hall of Flags)

Moderator: T. E. Bray, General Electric Co., Syracuse, N. Y.

A variety of mosaic sensor and display techniques will be discussed and compared. Probable applications, image surface-device characteristics, and problems encountered with interfacing circuitry will also be appraised.

SESSION X: MEMORY TECHNIQUES
Thurs., 9:00-12:00 a.m., Irvine Auditorium

Chairman: A. W. Lo, Princeton, N. J.

10.1: COINCIDENT-SELECT MDS STORAGE ARRAY

J. H. Friedrich, Fairchild Semiconductor, Palo Alto, Calif.

This paper will discuss the development of a coincident-select 64-bit p-channel MOS monolithic storage array to achieve low cost and high performance in future random access memory.

10.2: A MONOLITHIC DECODE-DRIVE CIRCUIT FOR MAGNETIC MEMORIES

W. F. Jordan, Jr., Computer Control Div./Honeywell, Framingham, Mass.

Integrated circuits are now being used for low-cost, high-speed, high-current switching in magnetic memories. Details of a new monolithic function and its application in a new address selection scheme will be described.

10.3: A 100-MHz, 1024-BIT, RECIRCULATING ULTRASONIC DELAY LINE STORE

G. L. Heiter, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

By combining a short high-speed delay line with integrated recirculation circuitry, it is possible to obtain a small size, relatively fast-access digital store which holds the promise of great economy. A suitable configuration will be discussed.

10.4: HIGH-SPEED, INTERLACED DRO AND NDRO OPERATION OF A PLATED-WIRE MEMORY SYSTEM

T. R. Finch and S. Waaben, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

Interlaced DRO and NDRO 150-ns read-write operation of an 80,000-bit plated-wire memory system will be described. Functional integration of read-write, select circuits, using beam-lead, sealed-junction technology will be reported.

10.5: AN 80-NS PLATED-WIRE STORE FOR A TIME COMPRESSION MULTIPLEX TRANSMISSION SYSTEM

J. D. Heightley and A. J. Perneski, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

Sequential read and sequential write of a 720-word 9-bit per word plated-wire memory system at a 12-MHz rate will be described. Time compression multiplex system requirements and store performance will be discussed.

SESSION XV: HIGH-SPEED CIRCUIT TECHNIQUES
Fri., 1:30-4:30 p.m., Annenberg Auditorium

Chairman: R. B. Seeds, Fairchild Semiconductor, Palo Alto, Calif.

15.1: LOW TEMPERATURE OPERATION OF Ge PICOSECOND LOGIC CIRCUITS

E. S. Schlig, IBM Corp., Yorktown Heights, N. Y.

Low-temperature operation of emitter-coupled logic circuits offers potential advantages in power dissipation, noise immunity, and reliability. Experimental ps germanium integrated circuits exhibit significant improvements in delay with moderate cooling, in contrast to observed degradation in the performance of comparable silicon circuits.

15.2: A NEW TECHNIQUE TO CONTROL STORAGE TIMES IN INTEGRATED-CIRCUIT TRANSISTORS

F. Capocaccia, SGS-Fairchild, Agrate Brianza, Italy

This paper will cover a Limited Saturation Device technique found to improve the absolute value, spread and temperature dependence of storage times in integrated transistors, and compatible to existing integrated-circuit processing.

15.3: CONTROLLED SATURATION AS AN APPROACH TO HIGH-SPEED LOGIC

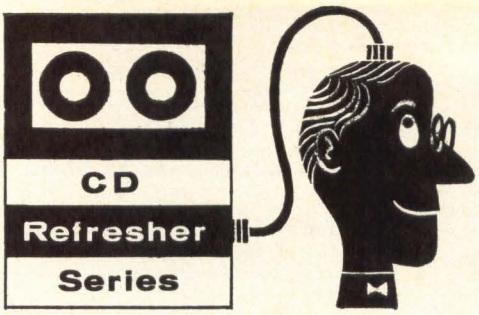
H. Mukai, Nippon Telegraph and Telephone Public Corp., Tokyo, Japan

A controlled saturation logic gate developed in a monolithic integrated circuit form has been found to offer exceptional performance and speed capability through saturation control coupled with operation of a push-pull output network.

15.4: TRANSISTOR-SCHOTTKY BARRIER-DIODE INTEGRATED-LOGIC CIRCUIT

Y. Tarui, Y. Hayashi, H. Teshima and T. Sekigawa, Government Electrotechnical Laboratory, Tokyo, Japan

A new high-speed, low-power logic circuit using Schottky barrier diodes to avoid saturation of bipolar transistors will be described. Both devices are compatibly realized in the form of monolithic integrated circuits.



A Review of Digital Differential Analyzers

NORTON MARKIN
Senior Engineer
The Bendix Corporation
North Hollywood, California

Mr. Markin discusses the applications, advantages and disadvantages of the DDA, describes how it is designed, programmed and used, and indicates recent improvements that make the DDA faster and more accurate.

The DDA was developed about 20 years ago,[2] to provide a greater precision than could be obtained using analog computers. It is composed of a set of integrator units that perform an integration by summing incremental areas under the curve of the function to be integrated. The basic block diagram for such a unit is shown in Fig. 1: For the arbitrary function $Y = f(x)$ shown in Fig. 2, a rectangular area, Δz, is added to the integrator unit each time an iteration is performed; when all the Δz areas under the curve have been summed, an approximation to the integral Ydx is obtained. The value of this approximation approaches the value of the integral as Δx approaches zero; therefore, the accuracy of the integration process can be increased at the expense of increased computation time by decreasing the Δx increments.

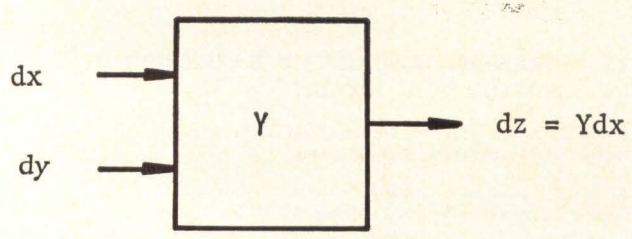


Fig. 1: Block diagram of integrator unit.

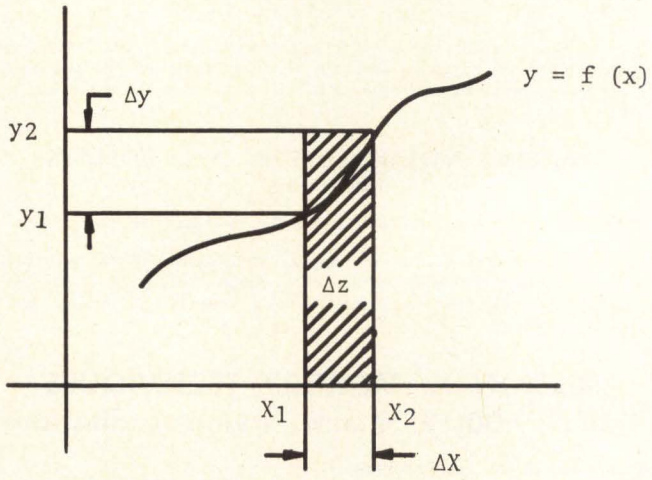


Fig. 2: Approximation of integral by rectangular summation.

The DDA can be used for solving any ordinary differential equation of any order or degree, linear or nonlinear, or a simultaneous set of such equations.[1] It can also be used to solve integral equations, transcendental algebraic equations, and simultaneous sets of such equations. Complexity of the equations that can be solved by a DDA is limited only by the number of available integrator units.

In general, DDA's are much slower than electronic analog computers. For example, a serial DDA with an operating speed of 100 kc takes ten times as long to produce an answer with an accuracy equivalent to that of an electronic analog computer.[2] However, with today's inexpensive integrated circuitry and technological advances, parallel DDA's can be built that operate at speeds more closely approaching the speed of the analog computer. For example, MOS integrated DDA chips are commercially available from which a parallel 500 kc DDA can be built, and each integrator unit in this DDA is composed of only 2 MOS chips.[3,4]

Advantages of the DDA over the analog computer include its greater precision (i.e., given enough time, the DDA can produce an accurate answer to more significant places than an analog computer), its ability to make logical decisions, its compactness, and its flexibility. Moreover, since the DDA handles information in digital form it is more readily adaptable for use as a part of a large computer system.

Since the DDA is specifically designed to solve differential equations, it is faster, simpler, and requires fewer programming steps than a general purpose digital computer, and is less expensive because it has no need for the elaborate control system or stored program required by the digital computer. Also, since the DDA output is of a differential form (i.e., the output indicates a change in a previous value rather than the new value itself), it is more adaptable for process control work (e.g., oil refining, power generation, machining, etc.) than the digital computer. Thus even with today's faster and cheaper general purpose computers there are still applications where the special purpose DDA cannot be easily replaced.

Programming

The method for setting up a differential equation on a DDA is similar to that used for an analog computer. The basic properties of the integrator unit shown in Fig. 1 are (1) the dy input is integrated in the unit to obtain a Y value; and (2) this value is multiplied by the dx input to give a resulting output of Ydx, which is called dz. The general procedure involved in setting up a problem for integrator units having such properties is as follows[1,5]:

1. Isolate the highest derivative of each independent variable on the left side of the differential equation.
2. Multiply both sides of the equation by the differential of the independent variable.
3. Assume the highest derivative in the equation formed in Step 1 is known and stored in the first integrator unit. Then use the output from this unit as an input into other units to generate the lesser order derivatives. Finally, sum the appropriate lesser order terms given by the equation derived in Step 2 to form the required input to the first unit.

The equation $d^2y/dt^2 + a(dy/dt) + by = 0$ will be used to illustrate the above procedure. First the highest derivative of the equation is isolated:

$$d^2y/dt^2 = -a(dy/dt) - by \qquad \text{(Eq. 1)}$$

Next, the multiplication in Step 2 is carried out:

$$(d^2y/dt^2)(dt) = -a(dy/dt)(dt) - by(dt)$$

or,

$$d(dy/dt) = -a(dy/dt)(dt) - by(dt) \qquad \text{(Eq. 2)}$$

Finally, Step 3 results in the interconnections among

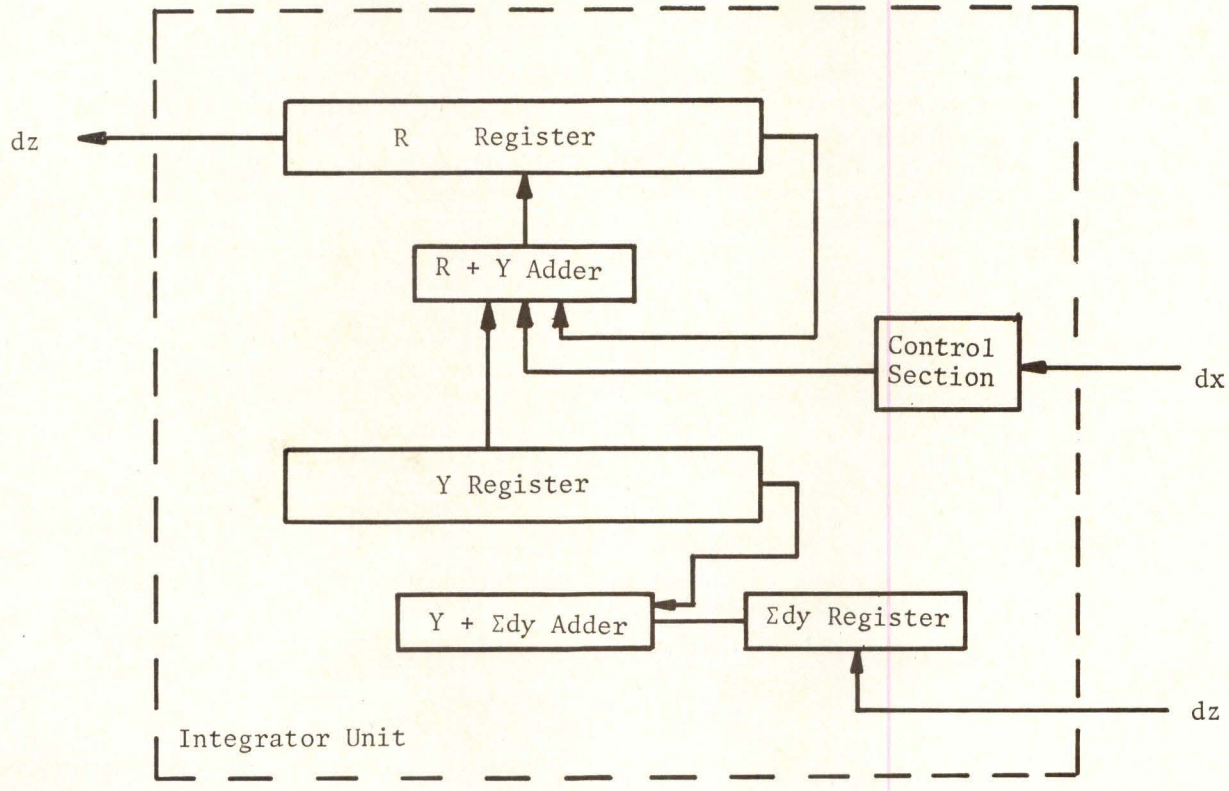


Fig. 3: Detailed diagram of integrator unit.

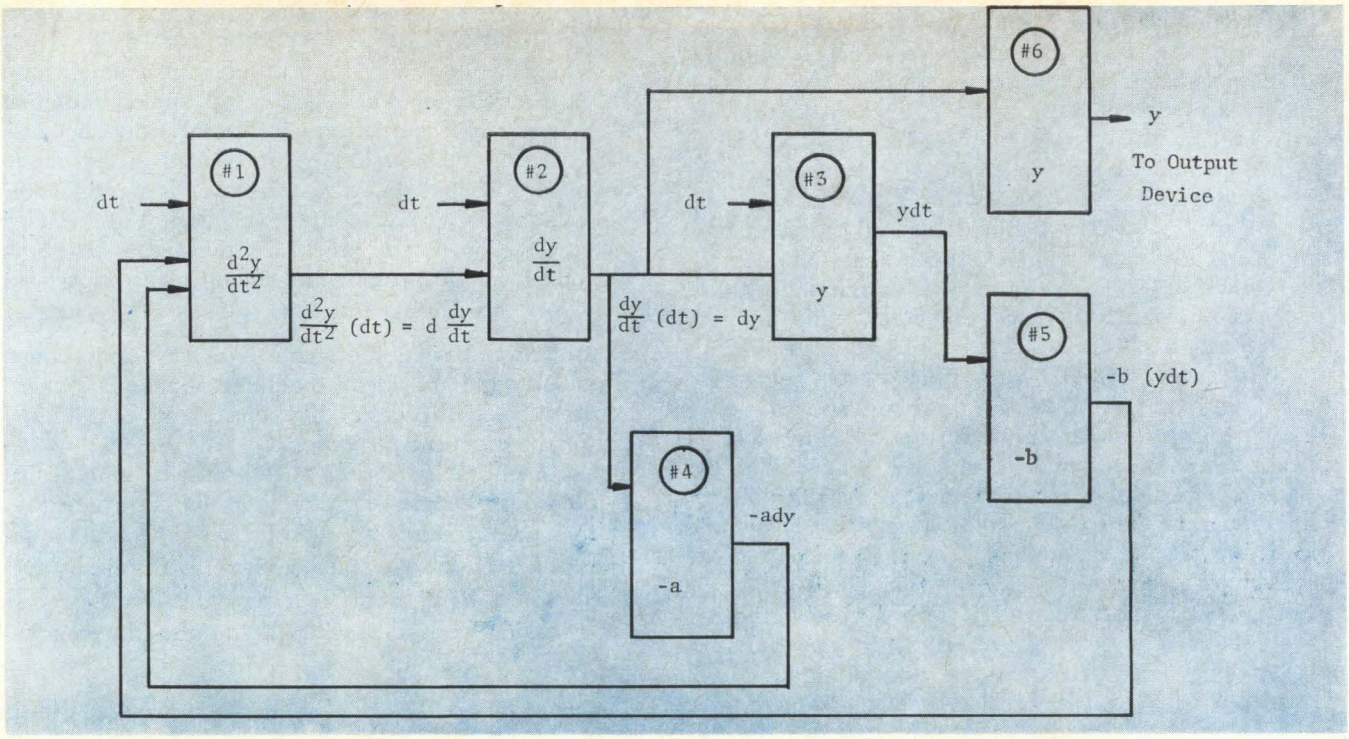


Fig. 4: Schematic representation for $(d^2y/dt^2) + a\,(dy/dt) + by = 0$

integrator units as shown in Fig. 4. To generate this diagram, it is first assumed that the derivative d^2y/dt^2 on the left side of equation 1 is available in integrator unit 1. Then integrator unit 1 integrates this value to form dy/dt, and integrator unit 2 integrates dy/dt to form dy. The dy output from unit 2 is put into the "dx" position (the multiplier position) of unit 4, which is used to multiply dy by a constant value, $-a$. This resulting product is used as one of the necessary inputs to unit 1 to satisfy Equation 2. There is no "dy" incremental input into unit 4 because unit 4 contains a constant value in the Y register. The ydt output of unit 3 is put into unit 5 to produce $-bydt$, and this output becomes the other required input to unit 1. With these two inputs going into unit 1, Equation 2 is satisfied and the iteration loop is completed. The dy output from unit 2 can be put into unit 6 where it is integrated to form the value for Y, the output.

After the interconnections shown in Fig. 4 are determined, initial values determined from the initial conditions given in the original problem are inserted into the integrator unit registers before the integration process begins. The quantities in the problem are scaled so that the capacity of the integrator unit registers will not be exceeded. Scaling consists of estimating the maximum value each variable is likely to attain during the course of the problem and then designating the number of significant digits for each integrator unit. If the estimate is too low, the register will overflow and the problem will have to be rescaled; if the estimate is too high, it will take longer than necessary to obtain a solution.[1]

Basic Design

Figure 3 is a detailed block diagram of an integrator unit.[5] For each iteration the dy inputs to the unit are added together and the sum updates the contents of the Y register. At this same time, the Y value is multiplied by the incremental dx input and the resulting "rectangular area" is added to the areas already stored in the R register. Thus, for the curve in Fig. 2, the previous contents (y_1) of the Y register are modified by Δy, and during the next iteration time the updated value in the Y register (y_2) is multiplied by Δx to obtain the cross-hatched Δz area. Since the value of the dx increment is taken as unity, the multiplication process consists of simply adding the contents of Y to the contents of R.

If it were necessary to store the entire sum of all Ydx products in the R register, the R register would have to be larger than the Y register. This requirement is eliminated by having the capacity of the registers equal and summing the R register overflow (i.e., the dz output) in another integrator unit when it is necessary to actually obtain the value of the integral. For most cases it is not necessary to sum the value in an integrator unit because the dz outputs are mainly used to satisfy the input requirements to other integrator units.

When designing a particular DDA, the methods for mechanizing the basic components shown in Fig. 3 are based upon a consideration of cost, computation speed, accuracy, precision, and reliability. One of the more conventional methods of mechanization, which represents a compromise between cost and iteration speed, is shown in Fig. 5. In this method each integrator unit is represented by a segment on a magnetic drum. One recirculating track represents the Y registers for all integrator units; another track represents all R registers; a third track, called the L track, contains instruction information for all integrator units; a fourth track contains the dz information; and a fifth track (not shown) is the clock track. If the integrator unit information is recorded and processed serially, all units can share a common set of adder circuits, coincidence circuits, etc.

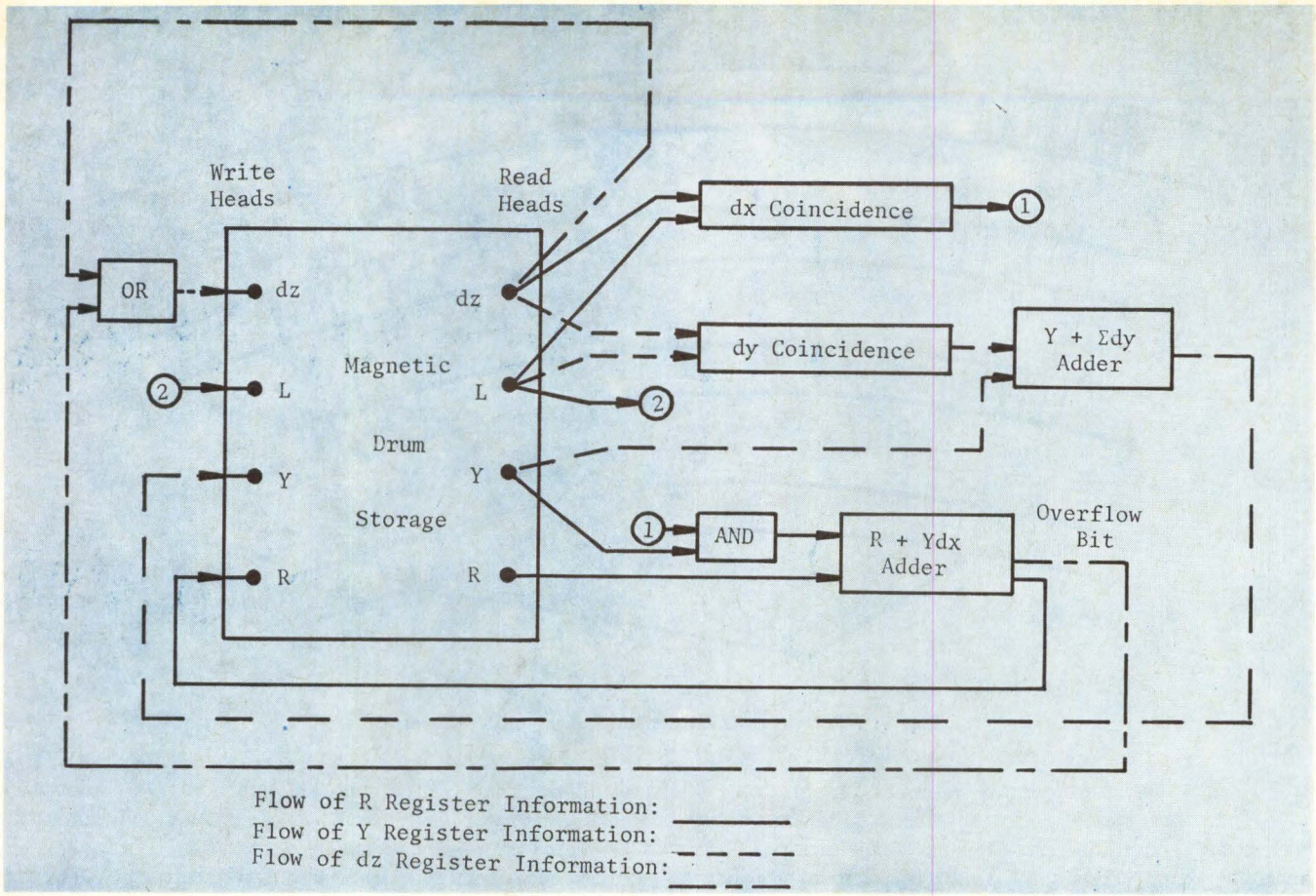


Fig. 5: Mechanization of serial DDA.

The interrelation between track segments is shown in Fig. 6. The dz output from each particular integrator unit is written into a specific position on the dz segment. Thus the overflow bit from the R register of unit 1 is always recorded in position 1 on the dz segment, the overflow from unit 2 is always recorded in position 2, etc.; and this dz segment is then repeated for all integrator units around the drum.

During one iteration period all dy inputs to the integrator unit being read are summed and added to the present contents of the Y register; and this result replaces the Y information that was just read. The dy inputs come from the outputs of other integrator units and can be found on the dz line during the iteration time. The L track information indicates which of these other integrator outputs are to be used as dy inputs. For example, if bits 3, 8, and 13 of the L track are true, then the dz outputs from integrator units 3, 8, and 13 will be summed together with the present Y register information to form the new Y register information.

At the same time that the Y register is being updated, the present Y register information is added to the contents of the R register, if the dx input is present, and this result replaces the contents of the R register. Once again the L track is used to indicate which integrator unit output is used as the dx input. Finally the overflow bit from the updated R register is recorded in the proper position of the dz segment, replacing the previously recorded bit.

The iteration process just described is shown in the diagram of Fig. 5. This process, which occurs each time a track segment representing an integrator unit passes under the read head of the drum, can be summarized as follows: (1) the value of Y is updated, (2) a new Ydx area is added to the R register, and (3) the overflow bit from the updated R register is recorded on the dz segment.

Improvements On Basic Design

In the basic binary design described, there is no true representation for an output of "zero." An output of $+1$ indicates addition and a -1 indicates subtraction. Thus a "zero" dy input to an integrator unit is represented by alternate values of $+1$ and -1; and at any given time the round-off error (ε) is $\varepsilon \leq |\,dz\,|$, where dz is the dy input that comes from another integrator unit.[1,6] If this dz output error is fed back to its own integrator unit directly or through a short loop, the error term becomes additive and the computation process soon becomes worthless. This type of error can be eliminated by using a ternary number representation, with the outputs $+1$, 0, and -1, so that a "zero" value is actually represented. This increases hardware costs but reduces the error to $\varepsilon \leq \frac{1}{2}\,|\,dz\,|$. If the same precision is maintained, the computation speed will be doubled when a ternary representation is used.

Another improvement of the basic DDA design involves approximating the integral by trapezoidal summation instead of by rectangular summation. In rectangular summation (shown in Fig. 2) each area is approximated by $y\Delta x$, while in trapezoidal summation (shown

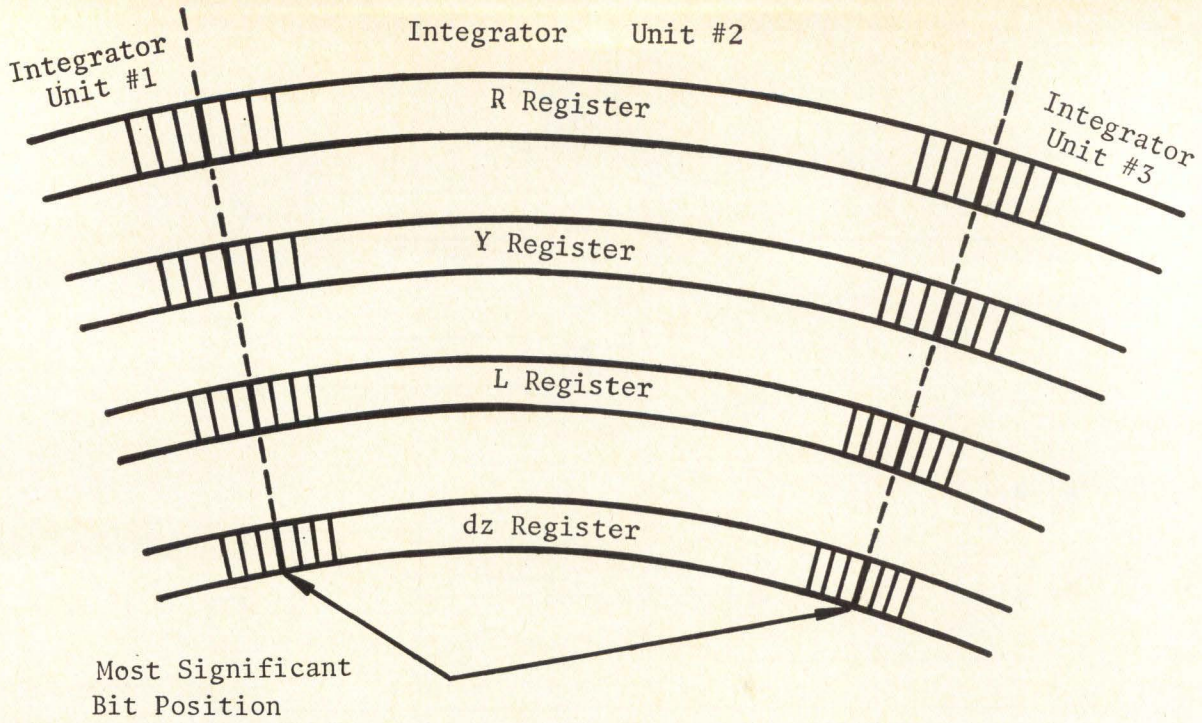


Fig. 6: Relationship between integrator unit registers.

in Fig. 7) the fundamental area of integration is $(y + \frac{1}{2}\Delta y)\,\Delta x$. The ratio of the trapezoidal error term to the rectangular error term is of the order of dx^6; therefore, when Δx is some small fraction, a considerable amount of error reduction can be attained by adding the extra hardware for trapezoidal integration.

For real-time problems where time is of the essence, computation time can be reduced by processing all integrator units in parallel — i.e., the arithmetic process is still done serially, but the integrator units are all processed at the same time. Thus, if 20 integrator units are processed in parallel instead of serially, the iteration speed is increased by a factor of 20. However, the cost is also increased considerably because this method requires 20 separate adders, 20 separate coincidence circuits, etc.

One such parallel DDA uses trapezoidal integration, a ternary number representation, and delay lines instead of a magnetic drum to store the integrator unit register information.[7,8] Three separate delay lines are used for each integrator unit: Two perform the same functions as were previously described; and the third register stores the initial value of Y entered into the DDA at the beginning of a problem; enabling repetition of the computation process without having to re-enter the initial conditions. Wired plugboard programming is used to connect the dz output from an integrator unit directly to specific dy and dx inputs. As a result, an L instruction line and a dz information line are no longer necessary.

In the design of this parallel DDA, separate adders are used for summing the dy inputs together. This means that all dy inputs must first be added separately. The result is then fed into the integrator unit where it is added to the contents of the Y register. Since most integrator units normally have only one dy input, the total amount of hardware can be reduced by using a group of adders that are common to all integrator units — i.e., fewer adders are necessary if they are shared among integrator units than if separate adders are used for each unit. Similarly the DDA also uses a group of multipliers common to all integrator units in order to reduce hardware.

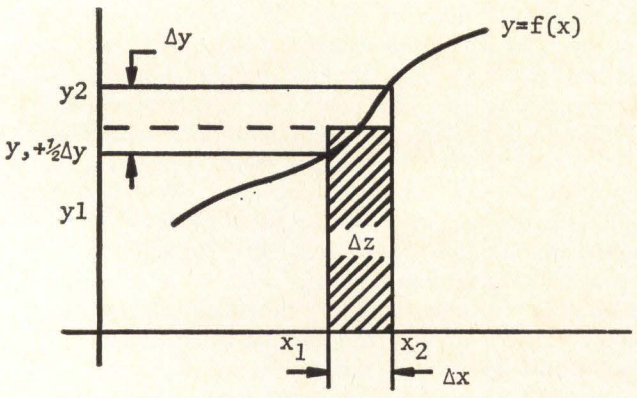


Fig. 7: Approximation of integral by trapezoidal summation.

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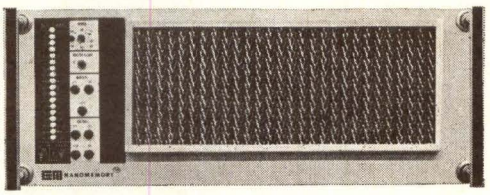

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CIRCLE NO. 28 ON INQUIRY CARD

The Development of a Large Integrated Complementary MOS Memory Array

by
S. KATZ and C. HANCHETT
Radio Corporation of America
Electronic Components and Devices
Somerville, N.J.

Complementary-symmetry MOS circuits are ideal for high-density memory arrays because of their economic use of silicon area, extremely low power dissipation and high-speed circuit operation which is tolerant of large variations in device parameters. The authors describe progress made in design and fabrication of a word-organized 288-bit complementary memory array on a high silicon chip.

Batch fabrication of both logic and memory systems is important in increasing the operating speed of computers while reducing their size and cost. There are indications that future high-speed scratch-pad and possibly main memories will be built entirely with large monolithic semiconductor arrays. The random-access storage matrix, and the address decoders used to select a particular memory cell location, can be processed simultaneously on a common substrate. Most active memory cells currently in use employ flip-flops to store binary information; some logic gating is incorporated in the cells to ensure that information is written into, or read out of, only the selected memory location. To decrease cycle time, the state of the cell is usually sensed in a nondestructive read-out mode (NDRO).

An active memory cell designed for large integrated arrays should meet the following requirements:[1]

- It should consume a small amount of silicon area so that the cost per bit is minimized.
- Power dissipation should be low so that the cost of packaging and cooling is kept low.
- The memory cell should be capable of high-speed operation so that it can be used in a variety of applications.
- Memory-cell circuit operation should be tolerant of large variations in device parameters, so that circuit yield is high.
- Stored information should be capable of being sensed with a minimum of circuitry.

Extremely low quiescent-power dissipation is desirable in any volatile memory system, and especially in aerospace and portable battery-

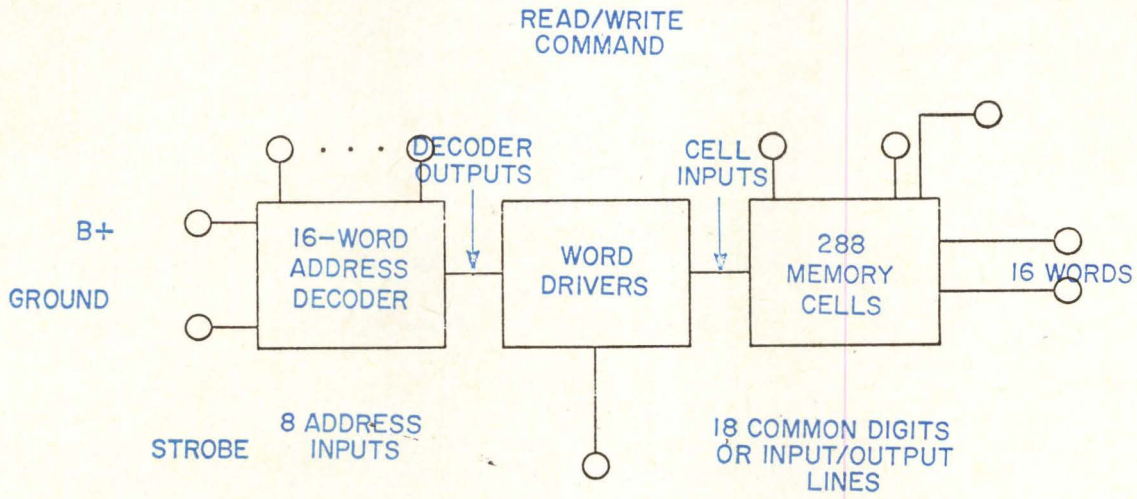


Fig. 1 — Block diagram of proposed 288-bit complementary MOS memory array.

operated equipment.

Thus far, only small monolithic bipolar memory arrays have been built; the size of the isolation regions required for bipolar devices, and the relatively high power dissipation characteristics of these devices appear to restrict the potential for large-capacity memories. Some work has been done in the fabrication of memory arrays composed almost entirely of p-channel MOS transistors.[2,3] Although amenable to high-packing densities, the single-channel MOS cells operate at lower speeds and dissipate higher standby power than cells consisting of both p-channel and n-channel MOS devices.

Complementary-symmetry MOS digital circuits[4] are ideal for high-packing-density memory arrays because of their economical use of silicon area, extremely low power dissipation, high-speed circuit operation, and tolerance to large variations in device parameters. A process has been established that permits fabrication of high-gain stable p-channel and n-channel MOS enhancement transistors on a common substrate.[4] Circuits of this type require little silicon area because they are composed entirely of MOS devices that exhibit natural isolation between units and bilateral properties. In addition, complementary MOS digital circuits feature excellent noise immunity and large fanout capability and require only one supply voltage. MOS cells requiring a minimum of circuitry to nondestructively detect their stored binary information have been designed.

This paper describes the work accomplished to date toward the fabrication of a 16-word by 18-digit complementary MOS memory array (module), including decoder and word drivers, on a single silicon chip. An experimental design of the memory cell and basic selection circuitry has been completed. Although the final array remains to be built, several integrated complementary MOS circuits which incorporate the functions of the final module have been successfully fabricated.

AN EXPERIMENTAL 288-BIT INTEGRATED MOS MEMORY ARRAY

A block diagram of the proposed 288-bit complementary MOS memory array, (16 words by 18 digits) is shown in Fig. 1. The memory is strobe activated, word organized, and nondestructively sensed. Word organization simplifies the memory cell, but at the same time makes decoding and word-drive circuitry more complex. However, because of the much greater number of cells, overall pellet size is minimized. The integrated array consists of a 16-output address decoder, 16 word drivers (which also select either the read or write mode of operation), and 288 memory cells. Eight address inputs are required for a high-speed 16-word MOS address decoder when a quaternary tree configuration is used. A read/write command signal is necessary for activation of the word-drive circuitry. To minimize the external connections to the chip, data is written into, and read out of, common digit (input-output) lines. The memory operates with a single

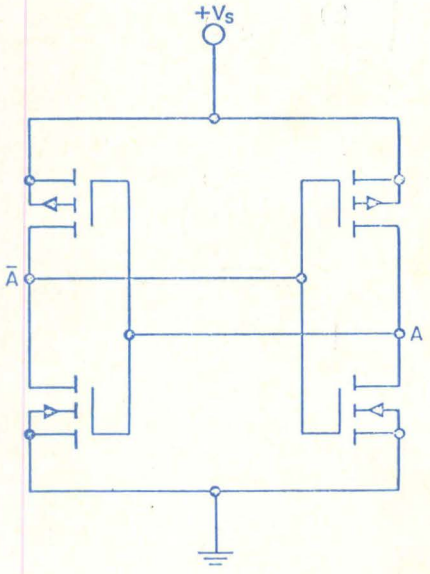


Fig. 2 — Complementary MOS flip-flop.

voltage supply. The 288-bit array, consisting of approximately 1800 devices, can be fabricated on a silicon chip 150-mils square for mounting in a 30-terminal package. Large memory systems can be constructed through the use of many of these arrays.

COMPLEMENTARY MOS MEMORY CELLS

Fig. 2 shows a flip-flop configuration common to all complementary MOS memory cells. The flip-flop, consisting of two cross-coupled inverter stages, dissipates negligible power when holding stored binary information. The circuit also exhibits excellent noise immunity because of the level of threshold voltage of the enhancement devices. Low power dissipation and excellent immunity are characteristic of complementary MOS logic.

A useful circuit configuration that simplifies and improves memory-cell performance is shown in Fig. 3(a).[4] The circuit is called a single transmission gate. Current can flow in either direction in the gate because of the bilateral property of the MOS device, i.e., the functions of source and drain can be interchanged. If, with the p-channel device biased off, terminal A of Fig. 3(a) is considered to be at a fixed potential and B is considered to be at a relatively high impedance, the voltage at B is independent of that at A. When the transistor is conducting, the voltage at B approaches that of A. Depending on the current direction, the transistor operates as either a drain-loaded or source-follower stage. The source-follower mode is characterized by slow-speed operation. Under this mode the circuit may cease conducting when the source-to-gate potential equals the threshold voltage. Both slow-speed and non-conducting tendencies can be greatly reduced or eliminated if the voltage swing at C is made larger than that at B and A or if the complementary transmission-gate of Fig. 3(b) is used. Although this gate requires an extra transistor and a gating signal, it operates on just two basic logic levels, ground and supply voltage, thus simplifiying the memory system. One MOS transistor in the complementary transmission-gate always operates in the drain-loaded state.

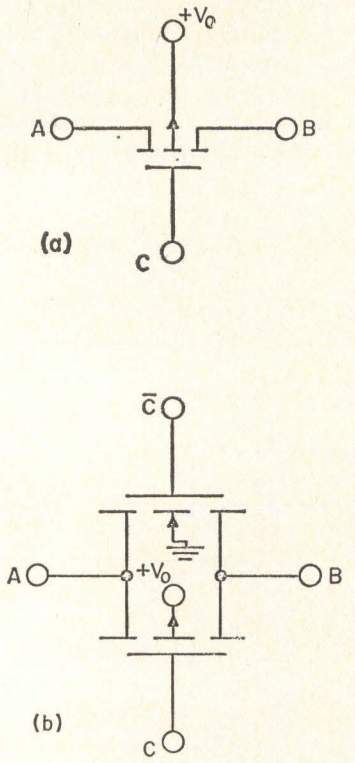


Fig. 3 — MOS transmission gates:
(a) Single gate
(b) Complementary gate

Several circuit configurations have been investigated in the search for a reliable high-speed memory cell well suited to high-packing-density complementary MOS arrays. These circuit configurations are first described, and then compared below. The optimum cell should contain a minimum number of transistors and signal lines in a simple mask layout so that silicon area is conserved.

Description and Operation of Memory Cells

The circuit of Fig. 4 represents a feedback memory cell. The cell consists of 12 transistors; a word-write line, W; a word-read line, R; and a digit line, D.[5] In the quiescent state, transistors Q_7 and Q_8 conduct, while Q_5 and Q_6 are biased off. Therefore, points C and A are shorted together while an open circuit exists between C and D. Transistors Q_1, Q_2, Q_3 and Q_4 form the flip-flop; transistors Q_5 and Q_6, and Q_7 and Q_8 form two complementary transmission gates. The inversion for the word-write complement, $\overline{W}$, is obtained with transistors Q_9 and Q_{10}. The digit line cannot change the state of an unselected cell because transistors Q_5 and Q_6 remain nonconducting, i.e., $W = +V_S$ and $W = 0$. Data is written into a selected cell by opening the feedback loop from C to A and connecting C to the digit line; then, $W = 0$ and $\overline{W} = +V_S$. The write signal returns to the supply voltage, $+V_S$, as soon as the digit information is securely transferred to C and A. This constitutes an extremely reliable write operation. Transistors Q_{11} and Q_{12} are included in the cell to allow nondestructive sensing of the state of the flip-flop by setting $D = R = 0$. Under these conditions the voltage at A determines whether a current is present in the low-impedance digit line. If $A = +V_S$ there is no current, if $A = 0$ there is a current. When $A = 0$ there is a surge of sense current at the start of the read command that is greater than the final steady-state sense current because the initial source-to-drain voltage of transistor Q_{12} equals the full supply. All twelve enhancement transistors are usually the same size.

The push-pull memory cell shown in Fig. 5 consists of twelve transistors; a word-write line, W; a word-read line, R; and two digit lines, D and $\overline{D}$. During the quiescent state, A and $\overline{A}$ are disengaged from D and $\overline{D}$ respectively; $W = +V_S$ and $\overline{W} = 0$. Transistors Q_1, Q_2, Q_3, and Q_4 form the flip-flop, and transistors Q_5 and Q_6, and Q_7 and Q_8 form two complementary transmission gates. The inverted-write signal is obtained through transistors Q_9 and Q_{10}. The D line and its complement $\overline{D}$ (obtained internal to the chip) cannot alter an unselected cell state because neither transmission-gate is conducting. Both gates are activated during the write-in operation for a selected cell when $W = 0$ and $\overline{W} = +V_S$. As one side of the flip-flop is charging to $+V_S$, the opposite side is discharging to ground potential, i.e., the voltage at A is forced to that of D, and correspondingly, the voltage at $\overline{A}$ is forced to that of $\overline{D}$. This push-pull drive scheme results in very high-speed operation, but at the expense of an additional digit line. The width of each of the four flip-flop transistors is less (the source-to-drain impedance is greater) than that of each of the transmission-gate drive transistors to ensure a change in cell state during the write-in operation. The difference in flip-flop and transmission-gate transistor

widths also increases the speed of the cell while lowering the quiescent power dissipation. The ratio of flip-flop to transmission-gate transistor size is 3:1. The sense arrangement for this circuit is the same as that of the memory cell shown in Fig. 4.

A simplified eight-transistor version of the basic complementary push-pull cell is depicted in Fig. 6. The circuit requires one word-write line, W; a word-read line, R; and two digit lines D and $\overline{D}$. The complementary transmission-gates and associated inverter used in Fig. 4 are replaced by single gates. The write signal need not be overdriven for high-speed operation because of the action of the push-pull digit drive.

By using the transmission-gates to sense the state of the flip-flop, transistors Q_7 and Q_8 and the associated read line can be eliminated with little sacrifice in reliability. The resulting cell, shown in Fig. 7, is composed of only six transistors; one word line, W; and two digit lines, D_1 and D_2. The input-output lines complement each other during the write operation, but are equal during read-out. The write operation is the same as that for the circuits of Figs. 5 and 6, i.e., $W = 0$ and $D_2 = \overline{D_1}$. Nondestructive sensing of the cell state requires that both transistors Q_5 and Q_6 be biased in the source-follower mode, i.e., $W = D_1 = D_2 = 0$. Current in only one digit line need be detected. If the voltage at A is $+V_S$ there will be a current in digit line D_1; if the voltage at A is zero there will be no current. Transistors Q_5 and Q_6 must not change the state of the flip-flop when they are in the source-follower mode and nondestructive-readout operation is desired. Therefore, transistors Q_1, Q_2, Q_3 and Q_4 are smaller in periphery than either Q_5 or Q_6 for reliable write-in operation, but not small enough to cause a destructive read-out. D_2 digit-line signals are obtained with some simple gating circuitry internal to the package.

Another six-transistor circuit that uses a transmission-gate to reliably write and read information into and out of a memory element appears in Fig. 8. The memory cell has two word lines, W_1 and W_2, and one digit line, D. Transistors Q_1, Q_2, Q_3, and Q_4 make up the binary-storing flip-flop, and transistors Q_5

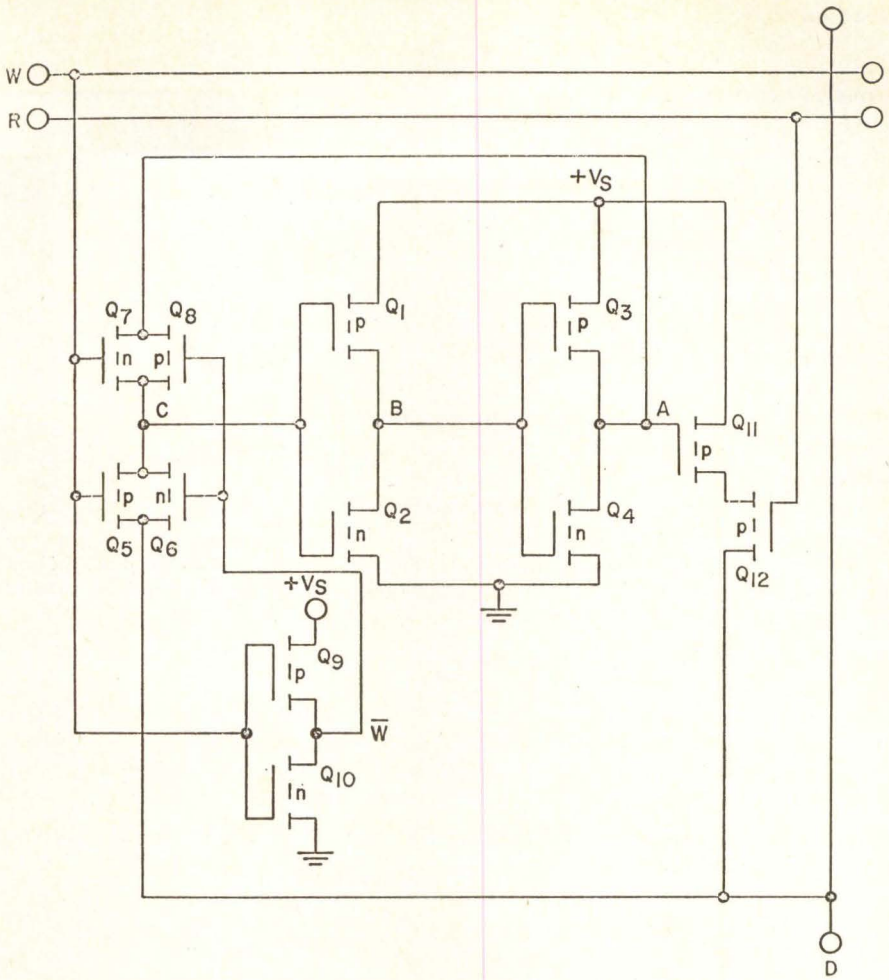


Fig. 4 — Feedback memory cell. All n-channel substrates connected to ground; all p-channel substrates connected to $+V_S$.

and Q_6 form a complementary transmission-gate. Information is written into a memory cell by activating the transmission-gate, i.e., by making $W_1 = 0$ and $W_2 = +V_S$. This brings the voltage at A to that of the digit line. Transistors Q_3 and Q_4 are smaller in width than devices Q_5 and Q_6 so that a change in cell state will be ensured. Transistors Q_1 and Q_2 are made larger in width than either Q_3 or Q_4; this increases the speed of the write-in operation. The state of the flip-flop is sensed with signals $W_1 = W_2 = D = 0$. Under these conditions Q_5 is biased on and Q_6 is biased off. If there is zero potential at A, there is no sense current in the digit line. However, if $A = +V_S$ a current will be sensed because transistor Q_5 is operating as a source-follower. To avoid a change in cell state when nondestructive-readout operation is desired and Q_5 is in the source-follower mode, and to ensure reliable write-in operation, transistors Q_3 and Q_4 are made smaller in width than Q_5 but not small enough to cause a destructive read-out. Because transistor Q_6 is nonconducting during the sense operation, there is no limitation on how large its size may be relative to Q_3 and Q_4. When $A = +V_S$ in the cells of Figs. 7 and 8, there is a surge of sense current at the start of the read command. This occurs because the initial source-to-drain voltage of Q_5 equals the full supply voltage. The steady-state voltage at A during the read command is a function of the relative impedances of transistors Q_3 and Q_5.

Comparison of Memory Cells

To select the complementary-MOS memory cell best suited for use in reliable high-speed high-packing-density arrays, a comparison was made of the five cells described above. To aid in the comparison each circuit was bread-boarded using semi-integrated transistors (separate p-channel and n-channel transistors, four to a package).

Readout Time

The basic bipolar-transistor digit-drive circuitry shown in Fig. 9 was used to measure the readout time of each memory cell, i.e., the delay from the leading edge of the read command to the sense-out voltage.[6] The circuit of Fig. 9 operates as follows: To write a "1" into the cell, the data input signal is pulsed to the supply voltage; this places a forward bias on the n-p-n transistor. To write a "0" into, or sense the state of, the memory cell, the data line is set to ground potential. Even with a heavy capacitive load (C_L) on the digit line to simulate the effect of unselected cells, the low input impedance of the forward-biased p-n-p transistor results in a fast readout or sense time.

All five memory cells exhibit essentially the same readout time of 5 to 10 nanoseconds under a capacitive load of 100 picofarads with a 10-volt supply. The basic sense arrangement common to the circuits of Figs. 4 through 6 offers little or no increase in speed over the transmission-gate sense scheme incorporated in the six-transistor cells of Figs. 7 and 8. The somewhat lower steady-state sense current of the six-transistor cells resulting from the smaller width of transistor Q_3 is offset by the light capacitive load on the digit line. The initial sense-current surge is equal for both six-transistor circuit configurations.

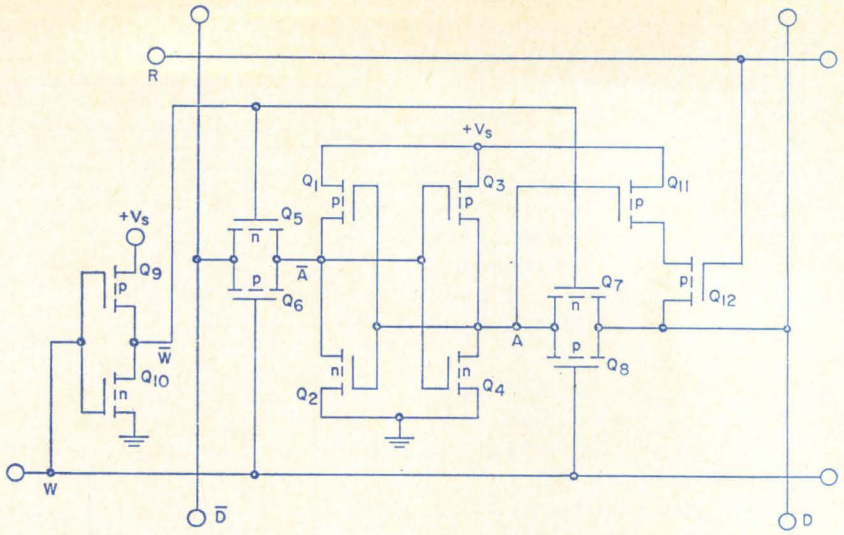


Fig. 5 — Twelve-transistor push-pull memory cell. All n-channel substrates connected to ground; all p-channel substrates connected to + V_S.

Write Time

The cell write times were obtained by measuring that minimum word-write pulse width, at 50 percent of signal swing, required for the cells to change state. It is not necessary that the storage flip-flop be completely switched when the write signal is removed; however, the flip-flop output voltage, A in Figs. 4 through 8, should be at 80 percent of its final value at the time a read command is initiated at the same location. It may be necessary to sense the stored binary state 50 to 70 nanoseconds after the removal of the write signal. Actual measurements were made by alternately writing a "1" (A = $+V_S$) and a "0" (A = 0) into each cell using a 10-volt supply, and by monitoring the flip-flop output voltage with an extremely low-capacitance probe. Table I compares the number of devices, external signal lines, reliability, and average write times for each memory cell.

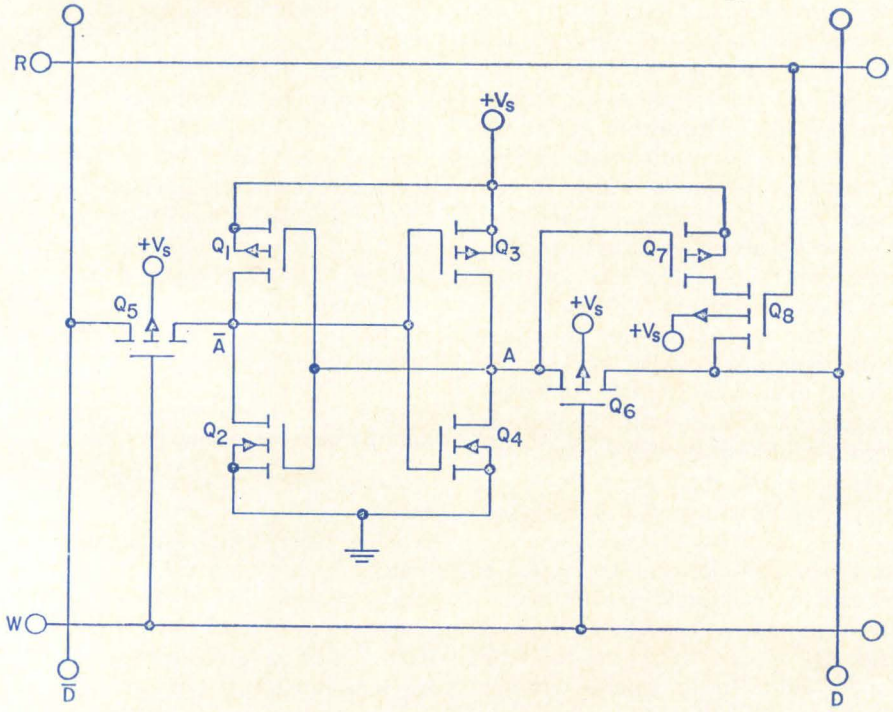


Fig. 6 — Eight-transistor push-pull memory cell.

General Comparisons

Although the complementary push-pull cell of Fig. 5 demonstrates fast write-in operation, it incorporates a large number of MOS transistors and signal leads and offers only slight improvement in overall memory-array cycle time at a high cost in silicon area. The twelve-transistor feedback cell of Fig. 4 requires an area of approximately 170 square mils in integrated form. Both six-transistor memory cells exhibit sufficiently good reliability and essentially the same high-speed performance as the more complex circuits while requiring fewer transistors, fewer signal lines, and correspondingly less area.

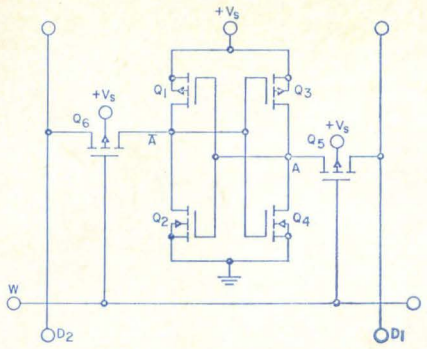


Fig. 7 — Six-transistor push-pull memory cell.

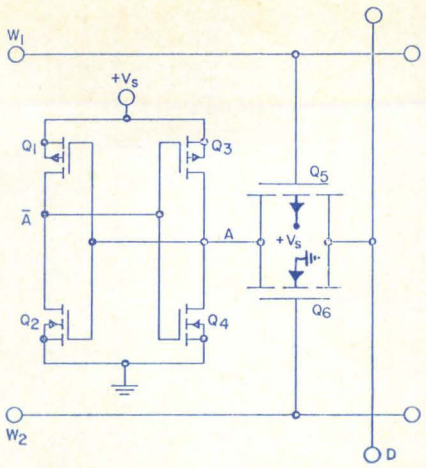


Fig. 8 — Six-transistor single-digit drive.

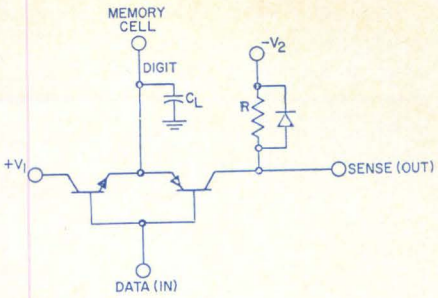


Fig. 9 — Bipolar-transistor digit-drive circuit for measuring memory-cell read-out time.

Results of Comparison

The six-transistor single-digit-drive cell of Fig. 8, which requires 60 square mils of silicon, has tentatively been designated best for high-packing density memory arrays. Because of its single-digit drive, the cell permits a simpler mask layout than that required for the circuit of Fig. 7. In addition, the write-in speed of the single-digit circuit can be increased without adverse effect on nondestructive readout operation by lowering the impedance of drive transistor Q_6; the push-pull cell of Fig. 7 does not offer this feature. Under the present state-of-the-art, the fabrication of 288-bit MOS memory cells on a single pellet is feasible provided that the cell design follows that of Fig. 8.

COMPLEMENTARY MOS DECODER-WORD DRIVERS

The 16-output quaternary-tree decoder shown in Fig. 10 may be used in the 288-bit array. The strobe-activated decoder includes 21 n-channel and 16 p-channel MOS enhancement devices and requires 8 input lines for 16 outputs. A given address signal is conducted by only one path consisting of two transistors. Because the strobe signal is at ground potential during the quiescent state, the p-channel devices are biased on, and all outputs are brought to the positive supply voltage $+V_S$. Upon command, the common n-channel strobe-controlled transistor activates the selected address path and switches the output to ground. The other fifteen unselected outputs remain at $+V_S$. When the strobe signal (which can be the decoded output of a large memory system) returns to ground, the selected output voltage reverts to the supply voltage. The maximum strobe-pulse width is limited by the time required for unselected lines to charge toward ground potential due to device leakage current.

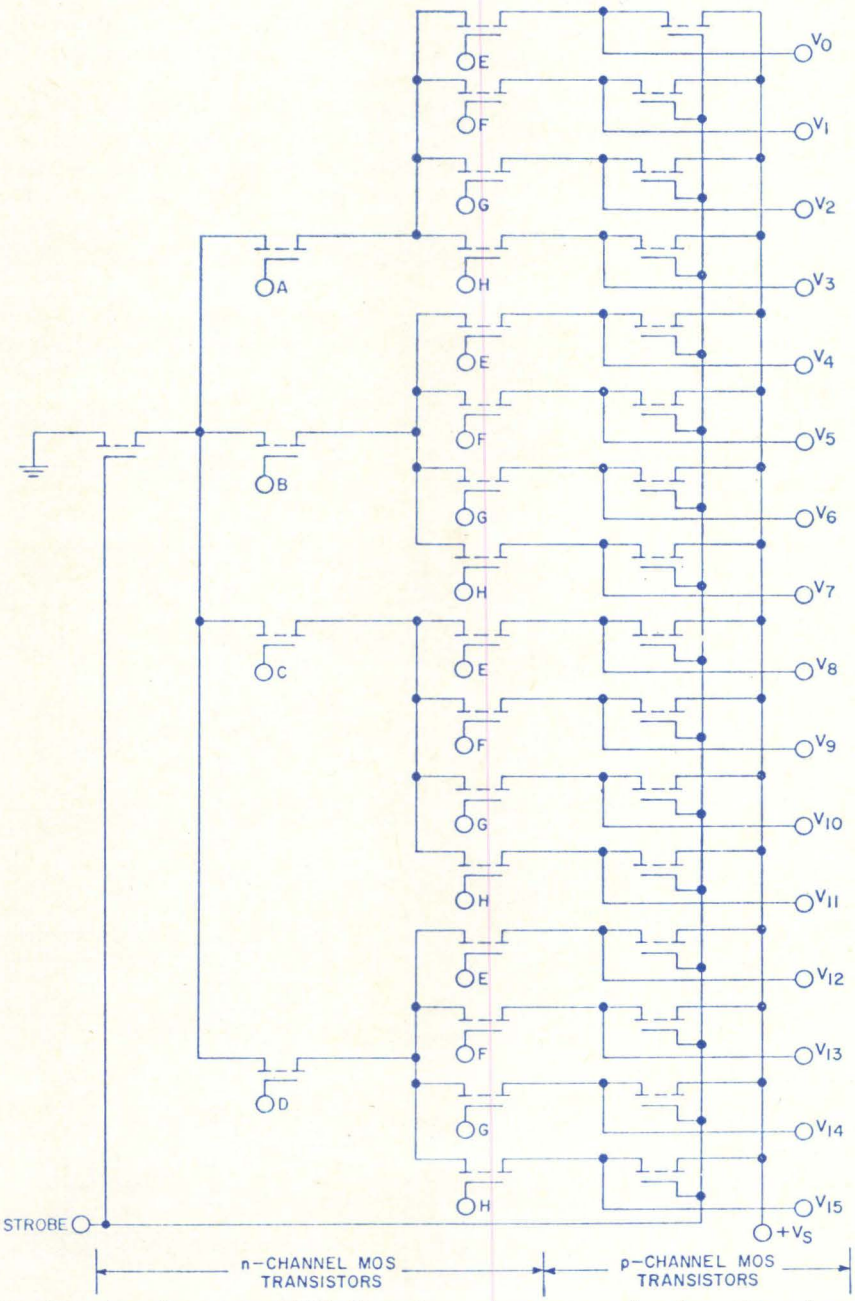


Fig. 10 — Complementary MOS 16-word quaternary-tree decoder. All n-channel substrates connected to ground; all p-channel substrates connected to $+V_s$.

The word-drive circuitry, which determines whether the cell is in the read or write mode of operation, is driven by the selected decoder output as shown in Fig. 11. Only one inverter per word line and one read/write command signal for each individual module is required for the memory cell of Fig. 8. Stored information is read out of a selected location with the read/write command at ground level, i.e., with $W_1 = W_2 = 0$. Data is written into the memory with the command signal at the supply voltage level, i.e., with $W_1 = 0$ and $W_2 = +V_S$. The time required by the decoder to perform its function constitutes a major portion of the module cycle time. Decoder time is defined as the time required to discharge the W_1 line capacitance through a three-level tree. The capacitance of the decoder is about equal to that of 18 MOS gates in parallel, i.e., one MOS gate per digit line.

As an alternate approach to the use of the quaternary decision tree just described, consideration is being given to the use of a tree similar to that of Fig. 10 except that the n-channel and p-channel devices are interchanged along with supply and ground lines, and an inverter is added to each output. Higher-speed operation may result because the total line capacitance is discharged through an inverter.

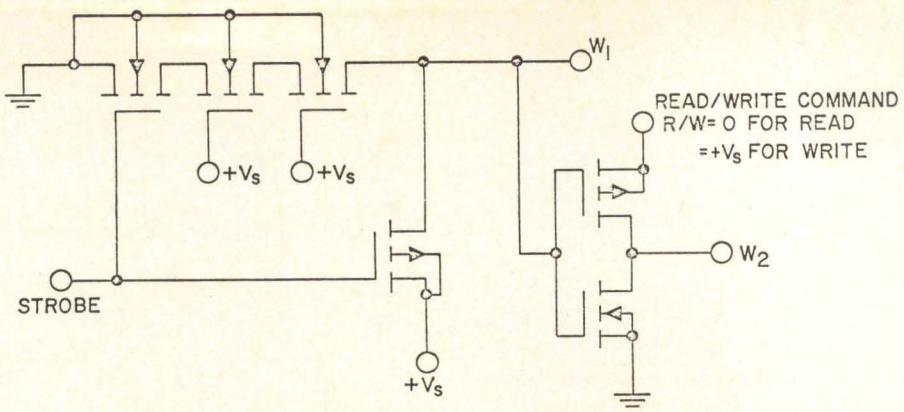


Fig. 11 — Decoder-word-driver-for selected line output.

FABRICATION OF INTEGRATED COMPLEMENTARY MOS TRANSISTORS

The processing steps involved in the fabrication of integrated complementary-symmetry MOS transistors on a single chip are illustrated in Fig. 12.[4] Steps 1 and 2 prepare the substrate for the p-channel devices. As shown, a p-type region is diffused into the n-type silicon substrate. The p-type region then becomes the substrate for the p-channel transistors.

Steps 3 through 6 provide the heavily doped p+ and n+ source and drain regions for the transistors. After these diffusions are completed, the diffusion-masking oxide is removed from the active region of the chip, the region occupied by the transistors. A new oxide is then grown in this area. This new oxide, the channel oxide, determines the characteristics of the transistors of which it is a part.

The final processing step consists of making contact openings over the source and drain diffusions, metalizing the wafer, and defining the metal pattern which consists of the gate electrode, the source and drain contacts, and interconnections. The wafer is then ready for electrical testing and dicing into individual circuit pellets.

The fabrication process used to construct integrated complementary-symmetry MOS transistors has yielded high-gain stable enhancement type MOS devices with good source-to-drain breakdown voltages: about 40 volts for the p-channel transistors and about 25 volts for the n-channel transistors. All breakdown voltages are measured at zero gate-to-source bias. Typical threshold voltages are −2.5 volts for the p-channel transistors and +1.5 volts for the n-channel transistors. The stability of MOS devices fabricated

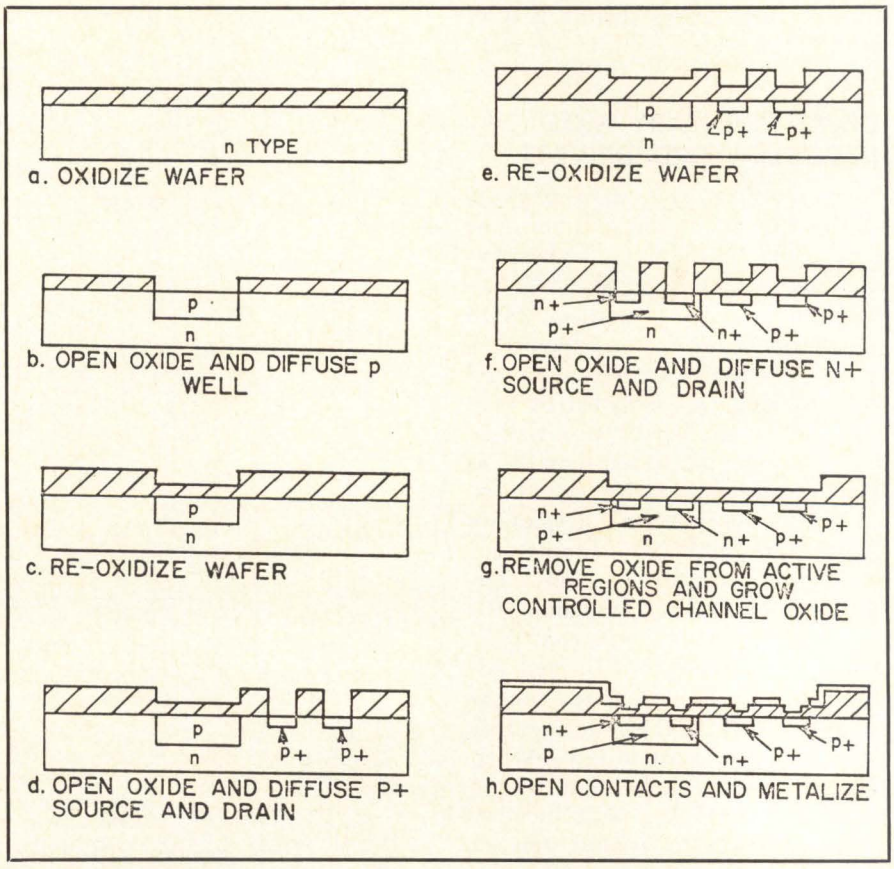


Fig. 12 — Complementary-symmetry MOS transistor processing stops.

by the complementary-symmetry process was evaluated under voltage-stress conditions at elevated temperatures. Typical transfer-characteristic shifts of less than 200 millivolts were exhibited after 1000 hours of operation under a gate bias of 10 volts and a temperature of 125°C.

RESULTS OF INTEGRATED MEMORY CIRCUIT FABRICATION

The layout design of the final 288-bit memory-array mask has been programmed for a future date. However, several integrated complementary-MOS circuits that functionally represent the ultimate module have been successfully designed and fabricated.

Single Memory Cells

The basic memory cells of Figs. 4 and 5, less the $\overline{W}$ line inverter, have been processed on the same wafer for a direct comparison in integrated form. Both cells, consisting of 10 MOS transistors each, are fabricated on a 35- by 25-mil silicon chip and mounted one per 12-lead package. Except for transistors Q_1, Q_2, Q_3, and Q_4 of Fig. 5 which have channel widths of 1.67 mils, all transistors fabricated have channels 5 mils wide; the channel length in all transistors is 0.2 mil. Some crossovers are performed external to the package. Photomicrographs of the single memory cells appear in Fig. 13.

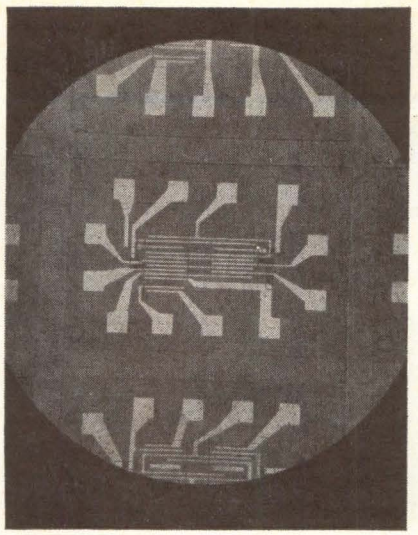
The integrated push-pull cell of Fig. 13(a) has a typical write-in time of 10 nanoseconds, as compared to 20 nanoseconds for the feedback cell of Fig. 13(b). A switching waveform for the push-pull circuit appears in Fig. 14. The cell write time can be reduced by eliminating the external crossover wiring. The sense time for both cells is approximately 10 nanoseconds for a 100-picofarad digit-line load. The quiescent power dissipation in both circuits is typically 30 microwatts. Recent process improvements would contribute an even lower value of standby-power dissipation. All measurements were taken with a supply of 10 volts.

Binary Tree Decoder

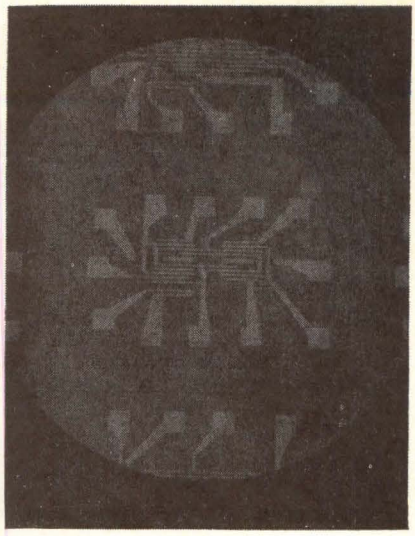
An experimental 16-output complementary-MOS address decoder, equivalent to 16 five-input NAND gates, has been processed on a 120- by 70-mil silicon chip.[7] The fabrication of the decoder demonstrates the feasibility of making large complementary MOS circuit arrays.

The circuit, which is shown in Fig. 15, is a strobe-activated binary decision tree that comprises 31 p-channel and 16 n-channel MOS enhancement devices, a four-bit binary input with corresponding address complements, and 16 outputs. The circuit is mounted in a 28-lead flat-pack. Because the decoder tree fans out toward the output, transistor channel widths can be changed without affecting the linear dimensions of the chip. Therefore, the channel width of the five series p-channel transistors varies from 20 mils to 7 mils. All n-channel units are 6-mils wide. The increase in device size improves the speed of operation of the decoder because the "on" path resistance is reduced without increasing the overall silicon area. The total active gate width is quite large, exceeding 500 mils. Both p-channel and n-channel transistors have a 0.3-mil channel length. A photomicrograph of the pellet is shown in Fig. 16.

Measurements on samples of the integrated decoder show an output rise-time of 125 nanoseconds with a 10-volt supply and a 7-picofarad load. The rise time is reduced to 70 nanoseconds when the magnitude of the source-to-gate voltage is increased from 10 to 15 volts. Because there is only one n-channel transistor at each output, as compared to the series of five p-channel MOS units, the typical fall time is about 40 percent of the rise time. Standby power dissipation, measured on operational units, is about 10 microwatts with a supply voltage of



(a) Feedback cell of Fig. 4.



(b) Push-pull cell of Fig. 5.

Fig. 13 — Photomicrographs of memory cells:

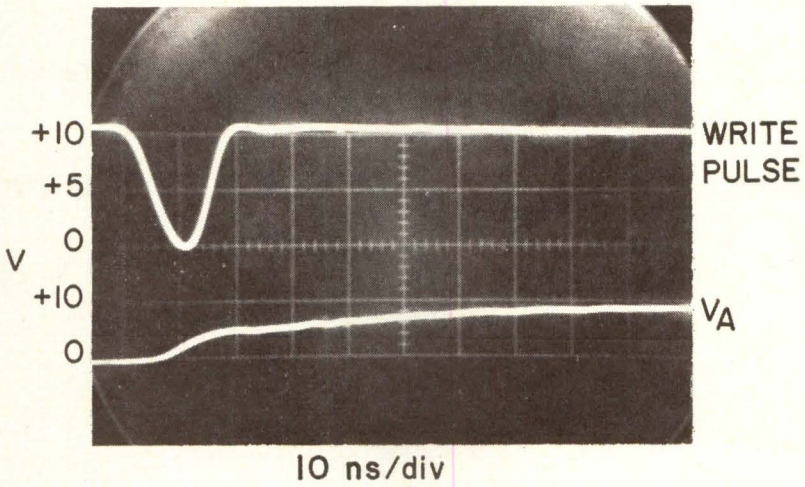
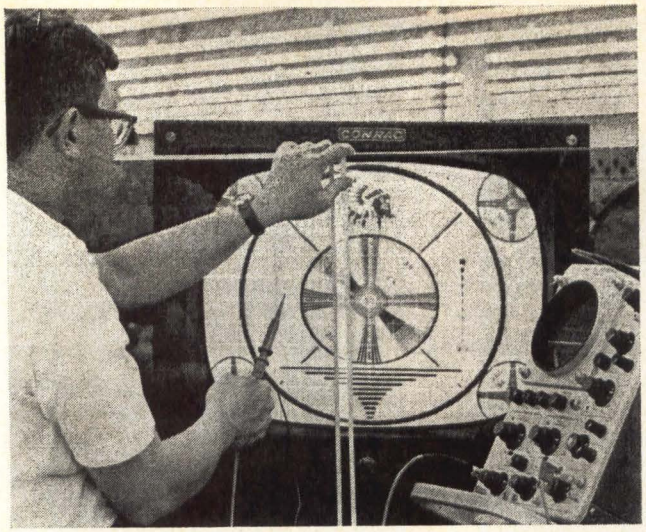
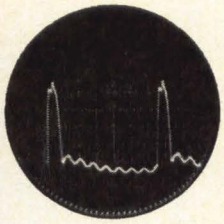


Fig. 14 — Switching waveform for the push-pull cell of Fig. 5.





Scope in photo (left) shows effectiveness of Sierracote transparent RF shielding. Scope above shows RF penetrating uncoated glass.

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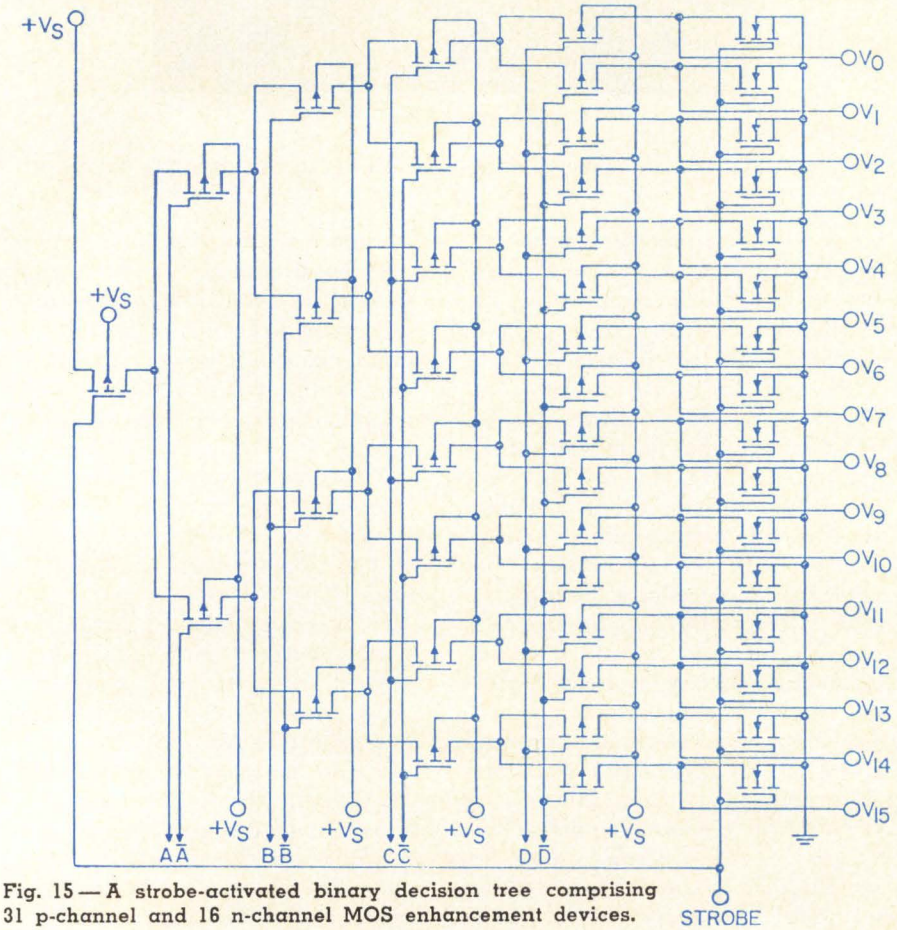

Fig. 15 — A strobe-activated binary decision tree comprising 31 p-channel and 16 n-channel MOS enhancement devices.

10 volts. Recent process improvements would contribute a lower quiescent-power dissipation. Because of the presence of the five series transistors, the binary-tree decoder is slower than the quaternary-tree decoder.

Memory Cell Arrays

An experimental 4-word by 9-digit memory array made up entirely of circuits of the type shown in Fig. 4 has been designed and fabricated on a 135- by 75-mil silicon pellet. Both p-channel and n-channel devices included are 1 mil in width and 0.3 mil in length. Individual cells require approximately 170 square mils of silicon area. The complete memory-cell array consists of 432 MOS transistors and is mounted in a 28-lead flat-pack. A photomicrograph of the pellet, which contains no decoding or word-drive circuitry, appears in Fig. 17. Several 36-bit memory arrays with all bits operational have been fabricated. Typical write-in and read-out times of 30 nanoseconds have been measured. The quiescent power dissipation of the pellets fabricated is approximately one milliwatt with a supply of 10 volts.

An experimental 8-word by 9-digit memory array composed entirely of 6-transistor cells such as those shown in Fig. 8 is presently being designed on a 103- by 81-mil silicon chip. Optimum device geometries have been determined by means of a computer-aided worst-case analysis. The mask design requires no metalized crossovers. Each cell requires 60 square mils, sharply increasing the packing density over that of the 36-bit array.

The 288-bit memory module will be designed after full evaluation of the 36- and 72-bit memory cells.

CONCLUSIONS

Complementary-symmetry MOS circuits are ideal for high-packing-density memory arrays because of their economical use of silicon area, extremely low power dissipation, and high-speed circuit operation which is tolerant of large variations in device parameters. A process has been established whereby high-gain stable p-channel and n-channel MOS enhancement transistors are fabricated on a common substrate.

Progress has been made, in the design and fabrication of a word-organized 288-bit complementary MOS memory array on a single silicon chip. The array is composed of an experimental 16-output quaternary-tree decoder, 16 word drivers, and 288 memory cells. The tentative cell design consists of six MOS transistors and requires an area of 60 square mils, making it ideal for high packing density arrays. The memory module, incorporating approximately 1800 devices, can be fabricated on a 150- by 150-mil silicon chip.

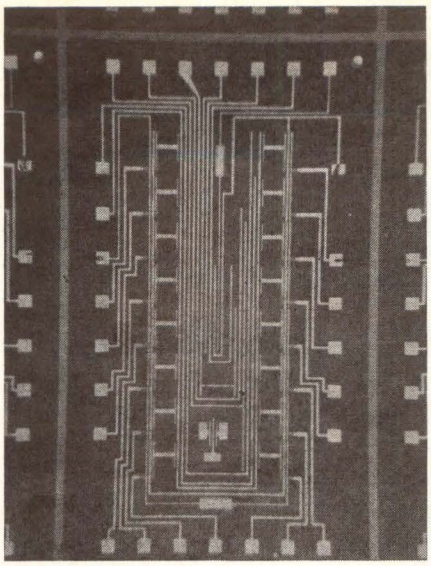

Fig. 16 — Photomicrograph of the pellet containing the circuit of Fig. 15.

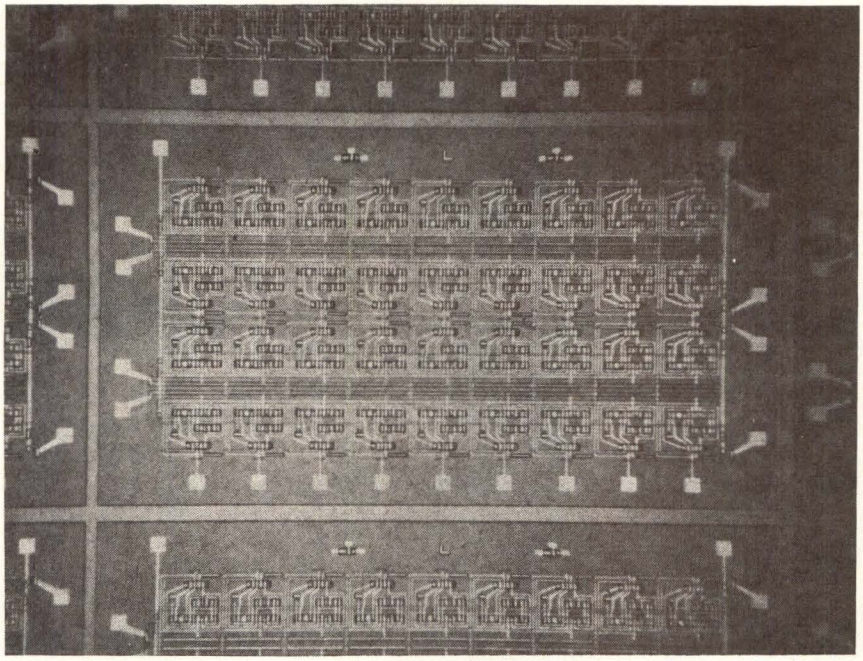

Fig. 17 — Photomicrograph of a 36-bit memory-cell array.

Although the mask layout of the final array is programmed for the future, several integrated circuits that functionally represent the final module have been successfully fabricated. Two of these are individual memory cells which demonstrate the advantages of complementary-symmetry MOS circuitry. The feasibility of making large complementary MOS arrays has been proven with the successful processing of a 16-output address decoder on a 120- by 70-mil silicon chip. Several operational 36-bit memory-cell arrays of 12 transistors per cell have also been fabricated.

ACKNOWLEDGMENTS

The authors express their appreciation to the technical personnel at RCA whose ideas and efforts have contributed to the integrated complementary MOS program. Special thanks are extended to R. Feryszka and A. K. Yung for their contributions concerning the monolithic decoder, A. Pittius and D. Puntillo for fabrication of the memory cells, and J. A. Ford for his work in obtaining the experimental results.

The work described in this article is supported by Air Force contract AF33(615)-3491.

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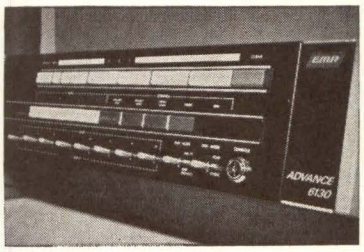

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TABLE I

COMPARISONS OF MOS MEMORY CELLS

Memory Cell	No. of Devices	No. of Signal Lines*	Reliability	Write Time (nsec)
Feedback Cell (Fig. 4)	12	3	Excellent	18
12-transistor push-pull cell (Fig. 5)	12	4	Very Good	12
8-transistor push-pull cell (Fig. 6)	8	4	Very Good	20
6-transistor push-pull cell (Fig. 7)	6	3	Good	20
6-transistor single-digit drive cell (Fig. 8)	6	3	Good	20

*Two additional lines are needed for supply voltage and ground.

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(5) J. R. Burns, J. J. Gibson, K. C. Hu, and R. A. Powlus, *"Integrated Memory Using Complementary Field-Effect Transistors"*, ISSCC, Feb. 1966.

(6) Circuit developed by J. R. Burns of RCA Laboratories.

(7) R. Feryszka, S. Katz, and A. K. Yung, *"Monolithic Complementary-Symmetry MOS Decoder"*, Digest of IEC, Toronto, Canada, Sept. 1967.

Chapter III. *The Word from GENISCO.*

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A GRAPHIC TABLET DISPLAY CONSOLE FOR USE UNDER TIME-SHARING.

Discusses the problems of using highly interactive graphic consoles with a time-shared processor. Some solutions to these problems are given and are illustrated in the graphic tablet display (GTD) console used with the SDC Time-Sharing System (TSS). Report also describes the components of the GTD, its interface with the TSS, and its operation.

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AN ANALYTICAL COST COMPARISON OF COMPUTER OPERATING SYSTEMS.

Evaluates computer system performance on general system characteristics that include the computer and its operating system and users and their jobs.

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THE MAKING OF TEST, THESAURUS OF ENGINEERING AND SCIENTIFIC TERMS.

Final report of Project LEX describes the background and building of the Thesaurus of Engineering and Scientific Terms. Appendices include authorizing papers, agreements, reference material, participants, and joint EJC-DoD conventions for thesaurus building. Results show collection and development of a large data bank, and description of final product as well as computer support and interface to automatic typesetting equipment.

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PRESENT AND FUTURE STATE OF THE ART IN GUIDANCE COMPUTER MEMORIES.

Discusses non-destructive read-out vs. destructive read-out type memory techniques and technologies with particular reference to six types of advanced solid-state memory devices: magnetic cores, plated wire, planar-magnetic thin

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TOWARD ECONOMICAL REMOTE COMPUTER ACCESS.

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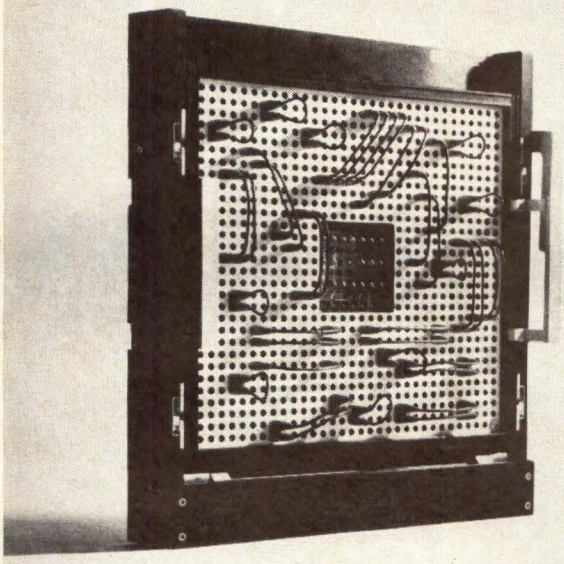

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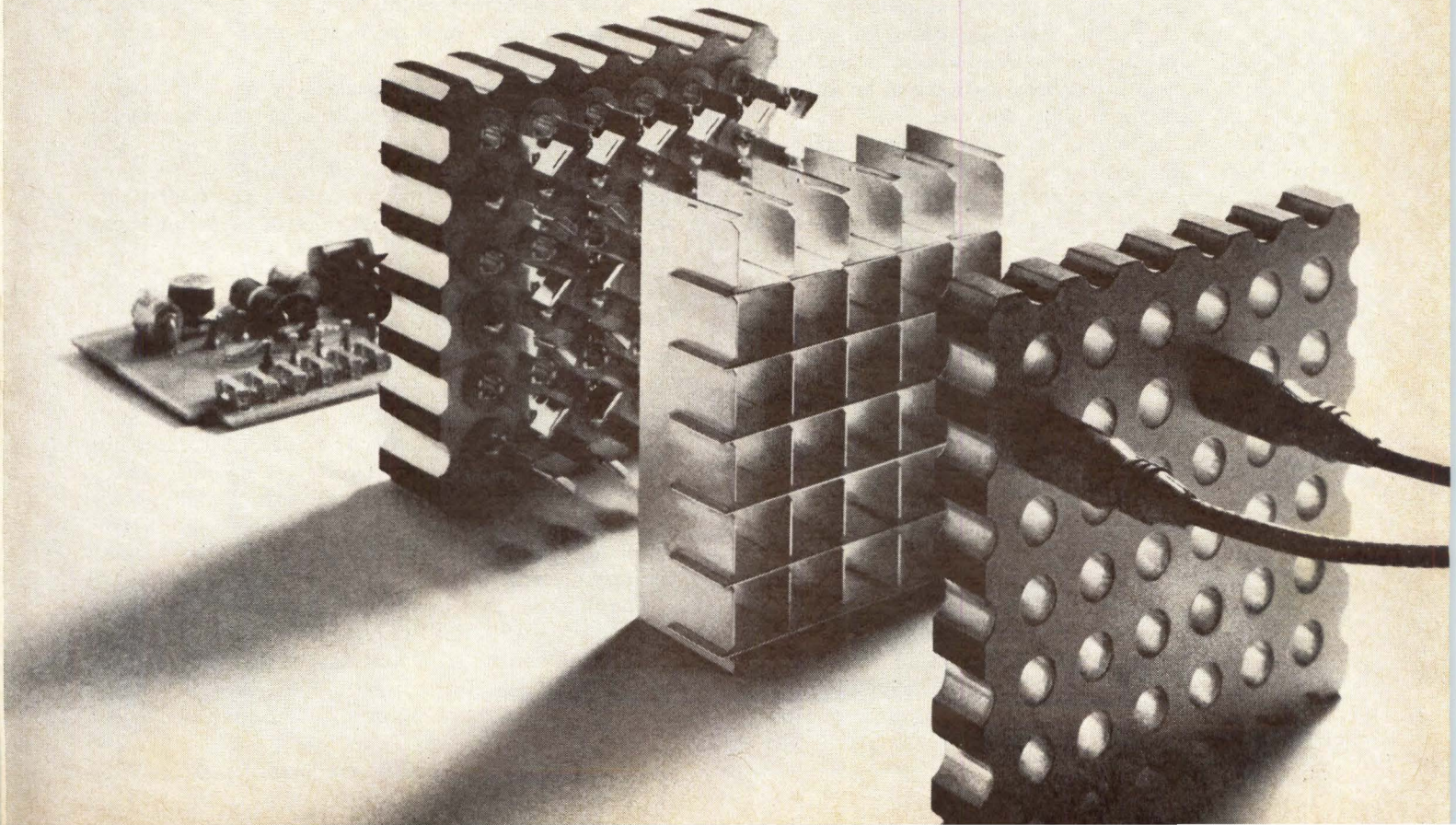


A design problem of a small logic system is used as an example to demonstrate the application of a simulation program. After the system requirements are established, a flow diagram for the timing and sequence control is developed. The simulation program can be considered the next step in the design phase. Written in the most basic Fortran, the program requires only a short time to write, debug and run.

SIMULATION OF A SMALL LOGIC SYSTEM

DONALD R. STANG
Southwest Center for Advanced Studies
Dallas, Texas

A logic designer faced with a small logic system or subsystem can easily write a simulation program himself. Much actual breadboard time may be saved with computer simulation, and flexibility in testing is gained without investment in elaborate test circuitry. Many types of input situations, both usual and unusual, may be applied to the system in order to test, evaluate, and analyze the system behavior. Discovery of errors at this stage in the design is a tremendous aid.

A brief description of a sample design problem is given below. The system requirements are outlined and a block diagram is drawn. A flow diagram is worked out which defines the modes of operation for the control. Next, the flow diagram is converted into a Fortran program, the terminology used in the program is defined and the input data is described. Finally, a sample printout is shown to demonstrate the operation of the system in accordance with the system requirements.

Design Problem

A logarithmic electrometer amplifier provides the output signal for an ion mass spectrometer satellite experiment. The electrometer amplifier signal is characterized by base line or zero voltage and voltage peaks. The mass spectrometer is swept by an exponentially decreasing voltage having a one second period. Peak position within the 1 second sweep range determines the ion mass in amu (atomic mass units). The peak amplitudes range from 0 volts to +5 volts and are the logarithmic function of the ion density.

The problem is to design a circuit that will find the peak values in digital form. First, the analog signal is sampled and digitized at 1 KHz rate, by an analog-to-digital converter whose output is a 9 bit number that represents the analog signal. The circuitry operates on these digital numbers to determine the average peak value, and then supplies this value to the spacecraft telemetry (TM) for readout. There may be up to 10 peaks within the 1 second sweep, each made up of approximately 20 points. The TM readout is fast enough so that no peaks will be lost.

The criteria for peak detection are as follows:

1. Points that are increasing indicate that a peak may be coming up.
2. After 3 increasing points in a row, check to see if the last sample is 4 or more increments above the base line.
3. Start "looking" for the peak. The peak is found if adjacent points are within a limit of ± 3 increments from each other.
4. Accumulate 4 points that fall within the limit.
5. The peak has occurred when three points in a row are decreasing. Store the average of the 4 accumulated points for readout.

Block Diagram of Logic System

A block diagram of the peaks logic circuitry is shown in Fig. 1. The logic beyond the A-to-D converter consists of registers (A, B, S, S′, O), a 3 bit shift-register (SR), a 2 bit counter (Accum. Ctr.), an adder, control bits (Look and Line), compare circuit (A:B), limit check ($\leq \pm 3$), and control. The registers A, B, and O are 9 bits; registers S and S′ are 11 bits. The control provides the timing or program sequence for the "peaks" circuitry operation.

The flow diagram of Fig. 2 incorporates the criteria for peaks and provides the basis for the control design. The overall control sequence may be divided into four phases or modes of operation. These are (1) Search Mode; (2) Peak Look Mode; (3) Accumulate Mode;

WITH A FORTRAN PROGRAM

(4) Output Mode. The mode descriptions given below refer to Figs. 1 and 2.

• **Search Mode:** The point in register A is transferred into register B, and the new point from the A-to-D converter is transferred into register A. These two points are then compared. If the number in register A is larger than the number in register B (A>B), a "1" is shifted into the shift register; if the number in register A is smaller or equal to the number in register B (A≤B), a "0" is shifted into the shift register. The adder in the circuit is used for subtraction by 1's complementing the lesser of A or B and then adding A and B. The end around carry is not performed so that the result in the sum register S will be A-B-1 or B-A-1.

After three successive 1's are detected in the shift register, a check is made to see if the last point is 4 or more increments above the base line. Each "1" in the SR means that A was greater than B by at least 1. Three 1's mean that the last point must be at least 3 increments above the base line. Therefore, if any of the 3 subtractions A-B-1 ≥ 1, the "line" bit will be set.

The control remains in the search mode till the three 1's and the base line 4 conditions are met. These conditions set the peak look bit which puts the control into the peak look mode.

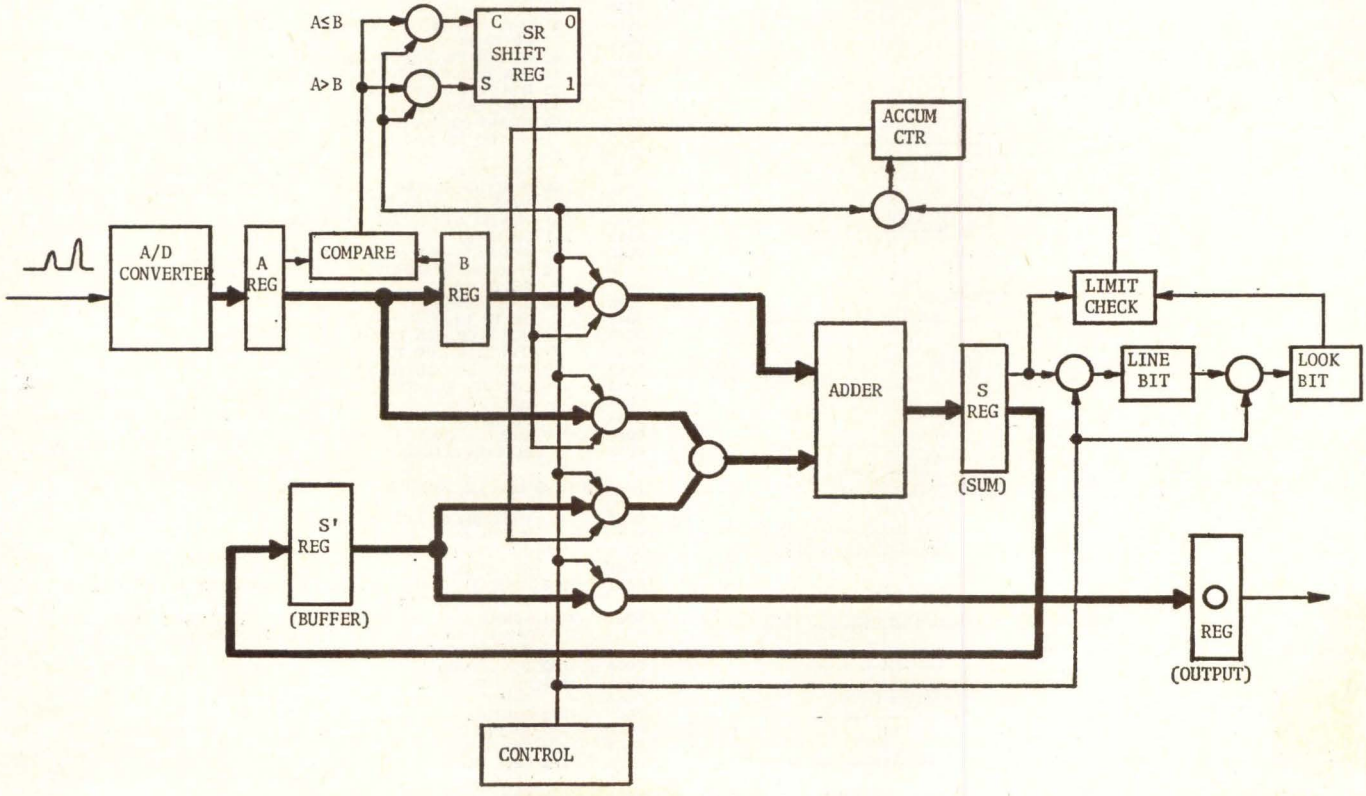


Fig. 1 — Block diagram of "peaks" circuitry.

• **Peak Look Mode:** When in the peak look mode, the control is looking for the condition where adjacent points are within a limit of ±3 increments. If A < B, A is 1's complemented and added to B as described above. This result is $\overline{A} + B$ = B-A-1. If the B < A, B is 1's complemented and added to A to form A-B-1. If either of these results falls within the limit, B is accumulated. B is automatically accumulated for the case A = B.

• **Accumulation Mode:** The first point that meets the limit criteria is accumulated. Four points are accumulated in the accumulation mode. If the peak of the curve is smooth, the 4 points will all meet the limit criteria successively; however, if a noise spike occurs after the first accumulation, the circuitry sees that the limit criteria is not met, the noise point is ignored, and the last point is **again** accumulated.

• **Output Mode:** After 4 points have been accumulated, the control circuitry looks for three consecutive 0's in the shift register. Three 0's mean that the peak has occurred and the input signal is decreasing toward the base line. The control returns to the search mode. The accumulated result divided by 4 (average peak value) is transferred to the output register for readout by the TM.

Simulation of Peaks Control by Computer

Operation of the control circuitry under different peak sizes and shapes tests that the peaks criteria is met. The program by operating on such a variety of inputs (peaks with different amplitudes, with noise etc.) is a great aid in uncovering errors that may exist in the design.

In general, the flow diagram for the control serves equally well for a Fortran simulation program. However, much more detail is required to obtain a program that will run on the computer. This detailed flow diagram (Fig. 3) and the program as written (Table I) are shown below. The Fortran statement numbers appear in parentheses in the boxes of the flow diagram.

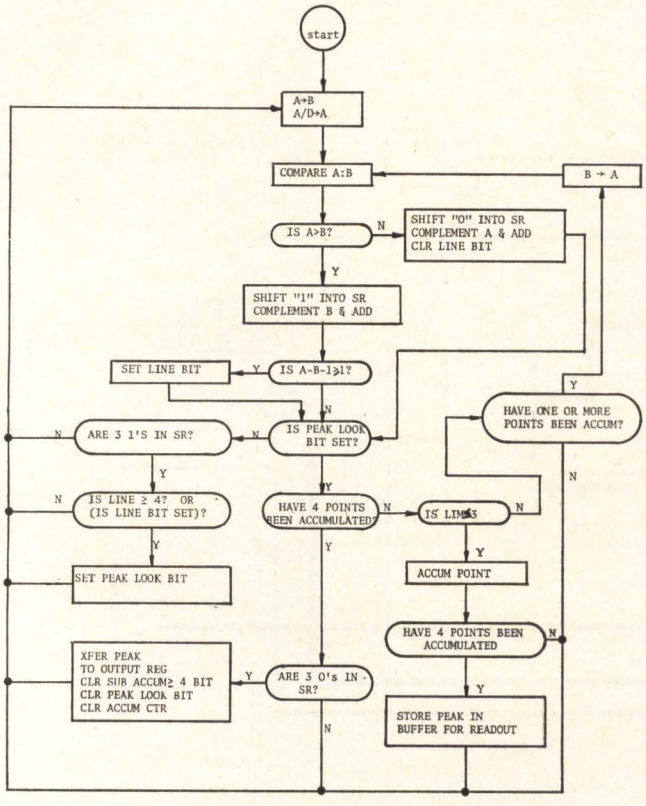


Fig. 2 — Flow diagram of "peaks" circuitry.

Definitions of the terminology used in the program are:

Input (I) = point I in the A/D converter output register

A (I) = point I in the A register

B (I) = point I in the B register

N(1), N(2), N(3) = 3 stages of the shift register

Accum = accumulation counter which keeps track of number accumulations that have been completed

TABLE I

FORTRAN SIMULATION PROGRAM

```
Fortran IV G Level 0, MOD 0        Main

0001          IMPLICIT INTEGER(A-Z)
0002          DIMENSION A(100),B(100),INPUT(100),SUM(100),N(3)
0003          J=1
0004        5 READ(1,1000)(INPUT(K),K=1,20)
0005     1000 FORMAT(20(1X,13))
0006          N(1)=0
0007          N(2)=0
0008          N(3)=0
0009          LOOK=0
0010          LINE=0
0011          OUTPUT=0
0012          BUFFER=0
0013          ACCUM=0
0014          WRITE(3,2001)
0015          I=1
0016          SUM(I-1)=0
0017          A(I)=INPUT(I)
0018          GO TO 11
0019       10 WRITE(3,2000)I,INPUT(I+1),A(I+1),B(I),N(1),N(2),N(3),LINE,LOOK,
              1ACCUM,SUM(I),BUFFER,OUTPUT
0020          IF(I.EQ.20)GO TO 100
0021          I=I+1
0022       11 B(I)=A(I)
0023          A(I+1)=INPUT(I+1)
0024          N(3)=N(2)
0025          N(2)=N(1)
0026       12 IF(A(I+1).GT.B(I)GO TO 30
0027       20 N(1)=0
0028          LINE=0
0029          GO TO 40
0030       30 N(1)=1
0031       31 IF(A(I+1)-B(I)-1.GE.1)LINE=1
0032          GO TO 40
0033       40 IF(LOOK.EQ.1)GO TO 60
0034       41 IF(N(3).EQ.0)GO TO 10
0035       42 IF(N(2).EQ.0)GO TO 10
0036       43 IF(N(1).EQ.0)GO TO 10
0037       50 IF(LINE.EQ.1)GO TO 51
0038             GO TO 10
0039       51 LOOK=1
0040          GO TO 10
0041       60 IF(ACCUM.EQ.4)GO TO 70
0042      161 IF(A(I+1)-B(I).GT.0)GO TO 61
0043      261 IF(B(I)-A(I+1).LE.3)GO TO 80
0044      361 GO TO 62
0045       61 IF(A(I+1)-B(I).LE.3)GO TO 80
0046       62 IF(ACCUM.GT.0)GO TO 63
0047          GO TO 10
0048       63 A(I+1)=B(I)
0049          GO TO 12
0050       70 IF(N(3).EQ.1)GO TO 10
0051       71 IF(N(2).EQ.1)GO TO 10
0052       72 IF(N(1).EQ.1)GO TO 10
0053          OUTPUT=BUFFER
0054          LOOK=0
0055          GO TO 10
0056       80 SUM(I)=SUM(I-1)+B(I)
0057          ACCUM=ACCUM+1

Fortran IV G Level 0, MOD 0        Main

0058          IF(ACCUM.EQ.4)GO TO 90
0059          GO TO 10
0060       90 BUFFER=SUM(I)/4
0061          GO TO 10
0062     2000 FORMAT('  ',4X,13,4X,I5,2(5X,I5),4X,I1,2(3X,I1),6X,I1,7X,I1,
              8X,I1,81X,I5,2(5X,I5))
0063     2001 FORMAT('  ',6X,'I',4X,'INPUT(I+1)',2X,'A(I+1)',2X,'B(I)',3X,
              'N(1)N(12)N(3)',3X,'LINE',4X,'LOOK',5X,'ACCUM',5X,'SUM(I)',4X,
              'BUFFER',4X,1'OUTPUT')
0064       100 IF(J.EQ.4)GO TO 110
0065       101 DO 102 I=1,20
0066           SUM(I)=0
0067       102 CONTINUE
0068           J=J+1
0069           GO TO 5
0070       110 CALL EXIT
0071           STOP
0072           END
```

TABLE II

PRINTOUT OF PEAKS SIMULATION

PEAK NUMBER 1

I	INPUT(I+1)	A(I+1)	B(I)	N(1)	N(2)	N(3)	LINE	LOOK	ACCUM	SUM(I)	BUFFER	OUTPUT
1	0	0	0	0	0	0	0	0	0	0	0	0
2	1	1	0	1	0	0	0	0	0	0	0	0
3	2	2	1	1	1	0	0	0	0	0	0	0
4	4	4	2	1	1	1	1	1	0	0	0	0
5	10	10	4	1	1	1	1	1	0	0	0	0
6	20	20	10	1	1	1	1	1	0	0	0	0
7	50	50	20	1	1	1	1	1	0	0	0	0
8	90	90	50	1	1	1	1	1	0	0	0	0
9	100	100	90	1	1	1	1	1	0	0	0	0
10	100	100	100	0	1	1	0	1	1	100	0	0
11	100	100	100	0	0	1	0	1	2	200	0	0
12	100	100	100	0	0	0	0	1	3	300	0	0
13	90	100	100	0	0	0	0	1	4	400	100	0
14	50	50	100	0	0	0	0	0	4	0	100	100
15	20	20	50	0	0	0	0	0	4	0	100	100
16	0	0	20	0	0	0	0	0	4	0	100	100
17	0	0	0	0	0	0	0	0	4	0	100	100
18	0	0	0	0	0	0	0	0	4	0	100	100
19	0	0	0	0	0	0	0	0	4	0	100	100
20	0	0	0	0	0	0	0	0	4	0	100	100

PEAK NUMBER 2

I	INPUT(I+1)	A(I+1)	B(I)	N(1)	N(2)	N(3)	LINE	LOOK	ACCUM	SUM(I)	BUFFER	OUTPUT
1	0	0	1	0	0	0	0	0	0	0	0	0
2	2	2	0	1	0	0	1	0	0	0	0	0
3	5	5	2	1	1	0	1	0	0	0	0	0
4	10	10	5	1	1	1	1	1	0	0	0	0
5	20	20	10	1	1	1	1	1	0	0	0	0
6	40	40	20	1	1	1	1	1	0	0	0	0
7	50	50	40	1	1	1	1	1	0	0	0	0
8	53	53	50	1	1	1	1	1	1	50	0	0
9	50	50	53	0	1	1	0	1	2	103	0	0
10	53	53	50	1	0	1	1	1	3	153	0	0
11	50	50	53	0	1	0	0	1	4	206	51	0
12	53	53	50	1	0	1	1	1	4	0	51	0
13	49	49	53	0	1	0	0	1	4	0	51	0
14	40	40	49	0	0	1	0	1	4	0	51	0
15	30	30	40	0	0	0	0	0	4	0	51	51
16	10	10	30	0	0	0	0	0	4	0	51	51
17	5	5	10	0	0	0	0	0	4	0	51	51
18	0	0	5	0	0	0	0	0	4	0	51	51
19	0	0	0	0	0	0	0	0	4	0	51	51
20	0	0	0	0	0	0	0	0	4	0	51	51

PEAK NUMBER 3

I	INPUT(I+1)	A(I+1)	B(I)	N(1)	N(2)	N(3)	LINE	LOOK	ACCUM	SUM(I)	BUFFER	OUTPUT
1	5	5	0	1	0	0	1	0	0	0	0	0
2	10	10	5	1	1	0	1	0	0	0	0	0
3	5	5	10	0	1	1	0	0	0	0	0	0
4	1	1	5	0	0	1	0	0	0	0	0	0
5	3	3	1	1	0	0	1	0	0	0	0	0
6	5	5	3	1	1	0	1	0	0	0	0	0
7	10	10	5	1	1	1	1	1	0	0	0	0
8	20	20	10	1	1	1	1	1	0	0	0	0
9	30	30	20	1	1	1	1	1	0	0	0	0
10	25	25	30	0	1	1	0	1	0	0	0	0
11	30	30	25	1	0	1	1	1	0	0	0	0
12	40	40	30	1	1	0	1	1	0	0	0	0
13	45	45	40	1	1	1	1	1	0	0	0	0
14	47	47	45	1	1	1	1	1	1	45	0	0
15	50	50	47	1	1	1	1	1	2	92	0	0
16	49	49	50	0	1	1	0	1	3	142	0	0
17	46	46	49	0	0	1	0	1	4	191	47	0
18	30	30	46	0	0	0	0	0	4	0	47	47
19	10	10	30	0	0	0	0	0	4	0	47	47
20	0	0	10	0	0	0	0	0	4	0	47	47

PEAK NUMBER 4

I	INPUT(I+1)	A(I+1)	B(I)	N(1)	N(2)	N(3)	LINE	LOOK	ACCUM	SUM(I)	BUFFER	OUTPUT
1	1	1	0	1	0	0	0	0	0	0	0	0
2	2	2	1	1	1	0	0	0	0	0	0	0
3	3	3	2	1	1	1	0	0	0	0	0	0
4	4	4	3	1	1	1	0	0	0	0	0	0
5	10	10	4	1	1	1	1	1	0	0	0	0
6	15	15	10	1	1	1	1	1	0	0	0	0
7	25	25	15	1	1	1	1	1	0	0	0	0
8	40	40	25	1	1	1	1	1	0	0	0	0
9	41	41	40	1	1	1	1	1	1	40	0	0
10	42	42	41	1	1	1	1	1	2	81	0	0
11	50	42	42	0	1	1	0	1	3	123	0	0
12	40	40	42	0	0	1	0	1	4	165	41	0
13	30	30	40	0	0	0	0	0	4	0	41	41
14	20	20	30	0	0	0	0	0	4	0	41	41
15	30	30	20	1	0	0	1	0	4	0	41	41
16	35	35	30	1	1	0	1	0	4	0	41	41
17	20	20	35	0	1	1	0	0	4	0	41	41
18	10	10	20	0	0	1	0	0	4	0	41	41
19	0	0	10	0	0	0	0	0	4	0	41	41
20	0	0	0	0	0	0	0	0	4	0	41	41

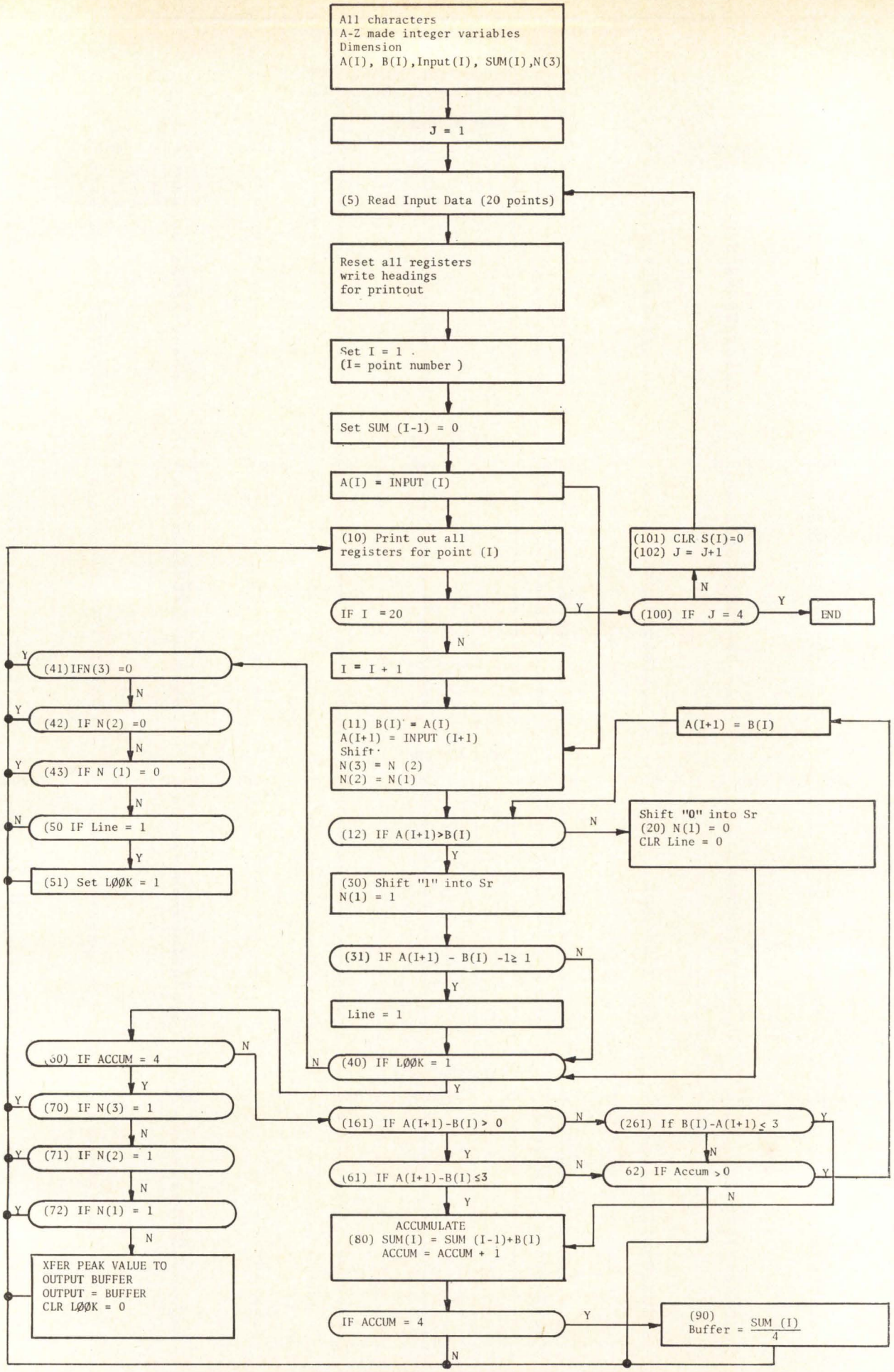
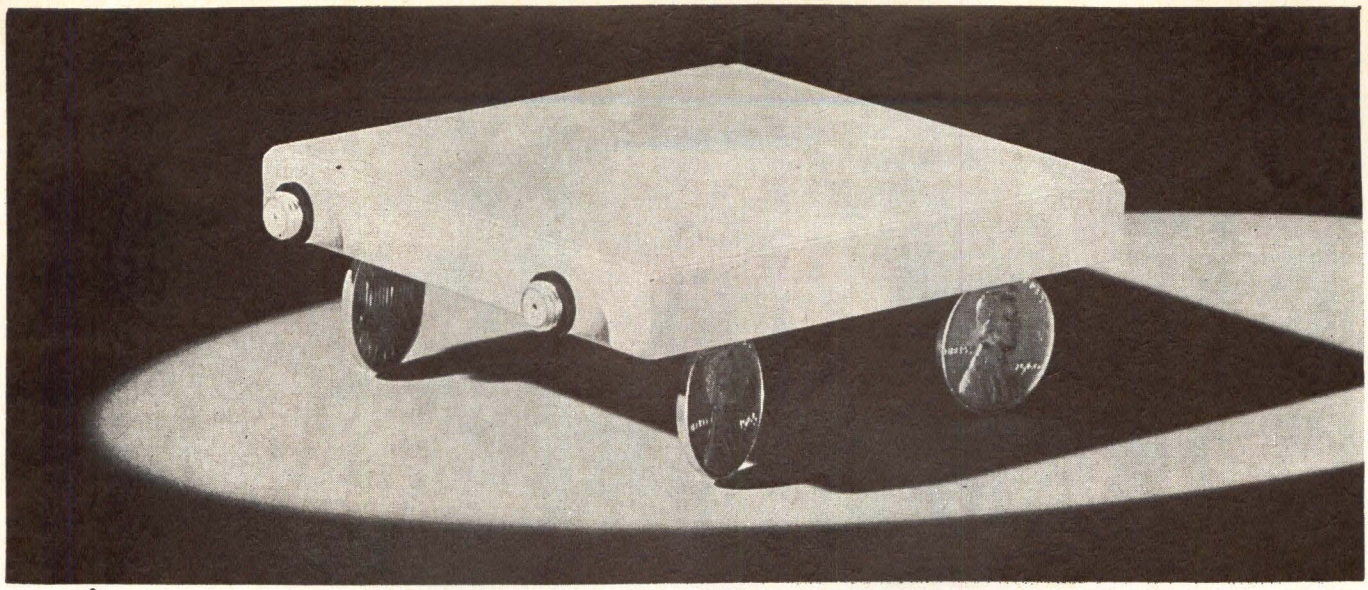


Fig. 3 — Flow diagram of "peaks" circuitry simulation.



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Line = control flip-flop is set when the point is 4 or more increments above the base line
Look = control flip-flop is set in the peak look mode
Sum (I) = is the accumulated sum up to and including point I
Buffer = register where the average value to peak is stored
Output = output register for TM readout

Data input to the program consists of 20 points (called I, where I = 1 to 20) that make up the peak. The program first reads in 20 points as input data. All four modes of operation are executed as the program processes all of these 20 points. A printout is done after each point of all registers, and control bits. The modes of operation become apparent when the total printout is observed.

The program exits after 4 peaks are processed. This number of peaks can be changed to any number by substituting another instruction for Fortran statement 100.

Computer Printout

A sample printout is shown in Table II. The contents of each register appear for each of the 20 points (I = 1 to 20) across the row. The contents of the registers Input (I + 1), A(I + 1), and B(I) are decimal numbers for simulation purposes.

Four different shapes of peaks have been used as examples for this particular run. These types are likely to occur so must be handled successfully by the logic system. A summary of the program printout of these peaks follows.

Peak number 1 has a smooth top at value 100 which is reached at point I = 10. The 4 values of 100 are accumulated, divided by 4 and transferred to the buffer. When three 0's are detected, the buffer value is set into the output register.

Peak number 2 oscillates between values 50 and 53 at the top. The first 4 points that fell within the limit ±3 were accumulated, averaged, and stored for readout. The average of 51 appears in the output register.

Peak number 3 has some base line noise which is rejected because the 3 criteria is not met. Also, a negative spike occurs after the program is in the peak look mode. This point is also rejected. At point I = 14 the limit is found and the next 4 points are accumulated. The average value is 47.

Peak number 4 has a noise spike (I = 11) after the program is in the accumulation mode. This noise spike is rejected, and the value 42 is accumulated twice. The average peak value in this case is 41.

Conclusion

A simulation program such as described above is a very worthwhile step in the design phase of a small logic system in terms of time and money. Also, this phase can be very enjoyable because the designer can observe his system in operation long before it is built.

negative radix arithmetic

M. P. deRegt

Part 8. COMPLEMENTARY ARITHMETIC

The negadecimal arithmetic presented thus far is characterized by being closely parallel to decimal, in that the same tables for addition, subtraction, and multiplication are used. In fact, the basic rule for the arithmetic is "same as decimal, except change sign of carry." In this article, new arithmetic operations will be introduced in which negative carry-outs do not occur, and the tables contain only positive digits. These operations in positive radix arithmetic are trivial because they involve only sign manipulation; in negative radix arithmetic, the tables are new, and the old addition, subtraction and multiplication tables do not apply. If we extend the possibilities by permitting use of negative digits, the operations comprise, with the negative radix notation, a rather distinctive, elegant and remarkable system of computation. The practical result is an incredible wealth of algorithms by which the normal arithmetic operations can be accomplished.

1. Complementation

The first of these operations is complementation, or changing the polarity of a number. This is a trivial operation in posiradix notation, in which it consists simply of changing the sign. In negaradix, however, it is not trivial; it is done by subtraction from zero. Note that this is somewhat related to complementation of a number in a system using the complement on R for negative numbers, except that in these cases, the subtraction is not from zero, but from R^n, where n is the number of digits including the sign position. Naturally, subtraction from zero is much cleaner; no separate convention such as a specified and known number of positions is required.

Since we have already discussed subtraction, in Part 3, it is necessary here only to focus on the case where the minuend is zero. The table is simple; it is the first

or zero minuend column of the nagadecimal digit-difference table, Table 4, of Part 3. However, since a negative carry-out cannot occur, the "N" carry column may be deleted. Several examples follow.

Example 1:

00000	000000
−(21797)	−(180423)
180423	021797

2. Co-addition

The name of this operation derives from the term "complementary addition," or the operation which combines two numbers to produce the additive inverse of their sum. The symbol "@" will be used to represent the operation, and the result will be called the "co-sum." Thus, the cosum R of A and B is defined as:

$$R = A \mathbin{@} B = -(A + B) = (-A) + (-B)$$

It should be noted that this operation does not replace addition, but is defined in terms of addition. In fact, the operation of addition will continue to be used as the basic operation for carrying, so that negative digits can still appear within the carry arithmetic. For the properties of the operation, the inverse and commutative laws apply; the associative law does not, and there is no identity element. These properties are all readily demonstrated by examples.

An interesting property of this operation is that the positions of the operation and equal symbols may be interchanged, and the positions of the operands may be interchanged without altering the truth of the equation. For example, in decimal:

$$3 \mathbin{@} 5 = -8$$
$$3 = 5 \mathbin{@} (-8)$$
$$5 = 3 \mathbin{@} (-8)$$
$$(-8) = 3 \mathbin{@} 5$$

The digit cosum table for decimal is trivial; for nagadecimal, however, it is a completely new table, as shown in Table 1. Note that all carries are positive, and that

TABLE I

NEGADECIMAL DIGIT COSUM TABLE

Carry Digit			Co-Augend Digit									
2	1	0	0	1	2	3	4	5	6	7	8	9
0	−	−	02	01	00	19	18	17	16	15	14	13
1	0	−	01	00	19	18	17	16	15	14	13	12
2	1	0	00	19	18	17	16	15	14	13	12	11
3	2	1	19	18	17	16	15	14	13	12	11	10
4	3	2	18	17	16	15	14	13	12	11	10	29
5	4	3	17	16	15	14	13	12	11	10	29	28
6	5	4	16	15	14	13	12	11	10	29	28	27
7	6	5	15	14	13	12	11	10	29	28	27	26
8	7	6	14	13	12	11	10	29	28	27	26	25
9	8	7	13	12	11	10	29	28	27	26	25	24
−	9	8	12	11	10	29	28	27	26	25	24	23
−	−	9	11	10	29	28	27	26	25	24	23	22

Co-Addend Digit

there are still three carry possibilities: 0, +1, and +2. In negabinary, there are only two carry possibilities, 0 and +1, so that the negative carry is eliminated, and only one carry signal line is required. Thus, a full negabinary co-adder circuit has a structure like that of a full binary adder, and can be used as a module for combining operands in completely novel ways. For example, if an "@" sign represents such a module, the structure implied by the left hand side of each of the following equations will perform the arithmetic on the right.

$(A \mathbin{@} B) \mathbin{@} 0 = A + B$ (2 modules)
$(A \mathbin{@} 0) \mathbin{@} B = A - B$ (2 modules)
$(A \mathbin{@} B) \mathbin{@} C = A + B - C$ (2 modules)
$(A \mathbin{@} B) \mathbin{@} (C \mathbin{@} D) = A + B + C + D$ (3 modules)

There is no limit to the number or arrangement of modules. Thus, circuits providing for combination of more than two operands can be provided. Since the operands may have either polarity, such structures are possible only using negaradix co-adder modules. Similar structures comprising positive radix co-adders for sign and magnitude notation are imposible; for complementary notation, they would require hopelessly complex overflow discrimination circuits, because each negative operand would have an R^n bias.

An example of co-addition follows:

Example 2.

86074	+73934
7642	−6438
148504	−67496

3. Co-multiplication

Co-multiplication is defined as the operation which combines two numbers to produce the additive inverse of their product. The symbol "#" will be used to represent the operation, and the result will be called the co-product. Thus, the co-product, R, of A and B is

$R = A \# B = -(A \times B) = (-A)(B) = (A)(-B)$

Co-multiplication may also be defined in terms of co-addition. Co-addition was defined for a pair of numbers, but the operation can be extended to apply to three or more numbers. Thus, $R = A_1 \mathbin{@} A_2 \ldots \mathbin{@} A_n = -(A_1 + A_2 \ldots + A_n)$.

If all the A_1 are equal, then we have

$R = A \mathbin{@} A \mathbin{@} \ldots$ to N terms
$= -(A + A + \ldots$ to N terms$)$
$= -(AN)$
$= A \# N$

For co-multiplication, the associative and commutative laws hold, as does the distributive law over addition. The identity element is −1, so that $A \# (-1) = A$, and the inverse law (for $A \neq 0$) is $A \# (1/A) = -1$. The various laws can easily be demonstrated using decimal numbers.

The table of digit co-products for decimal is trivial, but for negadecimal it is a completely new table, having only two positive digits. It is presented in Table 2.

Examples of co-multiplication follow, as usual with negadecimal on the left, and decimal on the right.

Example 3 (+ , −):

541	+461
67	−53
4833	+1383
3373	+2305
36573	+24433

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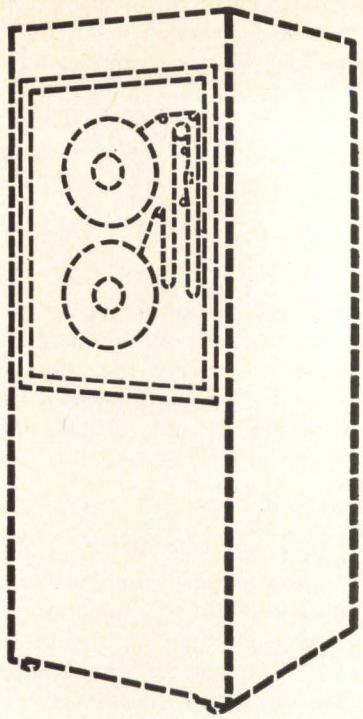

Example 4 (+ , +):

267	+147
316	+296
1298	−882
1953	−1323
1659	−294
164528	−43512

An interesting application of the co-multiplication operation is that the two square roots of opposite polarity may be co-multiplied to produce the square.

Example 5:

194	−14
26	+14
0096	+196
0032	
00216	

4. Multiplication Using Co-addition

In examples 3 and 4, it is quite obvious that if the additive inverse of the sum of the digit products had been taken, the result would have been the product of the operands instead of the co-product. In other words, we can also multiply two numbers by co-adding the digit co-products. This is a trivial distinction in normal decimal, but it is a different algorithm in negadecimal, as illustrated in the following example.

Example 6: Multiply by co-adding the digit co-products.

7219	−6801
461	+341
14801	+6801
40806	+27204
33204	+20403
18480959	−2319141

TABLE 2

NEGADECIMAL DIGIT CO-PRODUCT TABLE

#	1	2	3	4	5	6	7	8	9
1	19	18	17	16	15	14	13	12	11
2	18	16	14	12	10	28	26	24	22
3	17	14	11	28	25	22	39	36	33
4	16	12	28	24	20	36	32	48	44
5	15	10	25	20	35	30	45	40	55
6	14	28	22	36	30	44	58	52	66
7	13	26	39	32	45	58	51	64	77
8	12	24	36	48	40	52	64	76	88
9	11	22	33	44	55	66	77	88	99

Although it is not possible in this short summary to go into details, it is clear that a host of possible algorithms can be defined for multiplication, co-multiplication, division, and co-division* by combining use of digit product or digit co-product tables with addition, subtraction, co-addition or co-subtraction*. This wealth of method provides an extremely large choice of design options for special purpose equipment.

*We have not defined co-division and co-subtraction, but the reader should have no difficulty in doing this for himself.

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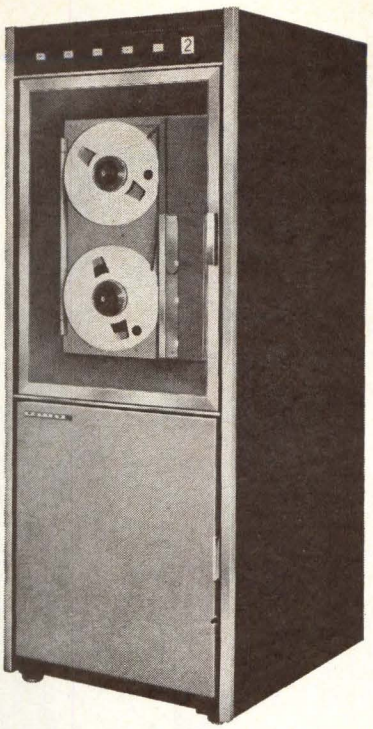

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5. Complementary Representation

The notion of a number system having digits of negative value was discussed in Parts 1 and 2; in Part 2, the cobinary system was defined as one whose base is -2 and whose numerals are 0 and -1. It was further explained in that article that overflow in multiplication was possible in negabinary, but not in cobinary. This fact is generally true for other radices, and the implications can be more readily understood for cobinary by considering "co-decimal" — the system whose base is -10 and whose numerals are 0 and -1 through -9. Some idea as to the implications of the use of negative digits (represented by italics) in multiplication and division can be obtained by multiplying numbers of minimum and maximum magnitude for the quantity of digits, as we did in Part 4, p. 43 of the August 1967 issue. Note that the digits product table for codecimal *looks* like the digit co-product table for negadecimal except that it is all in italics, e.g., $\overline{8} \times \overline{7} = \overline{64}$.

$$\begin{aligned} \overline{1}\overline{9}\overline{0}\overline{9} \times \overline{1}\overline{9}\overline{0}\overline{9} &= \overline{9}\overline{8}\overline{9}\overline{9} \\ \overline{9}\overline{0}\overline{9} \times \overline{1}\overline{9}\overline{0}\overline{9} &= \overline{9}\overline{8}\overline{8}\overline{9}\overline{9} \\ \overline{9}\overline{0}\overline{9} \times \overline{9}\overline{0}\overline{9} &= \overline{9}\overline{8}\overline{7}\overline{8}\overline{9}\overline{9} \end{aligned}$$

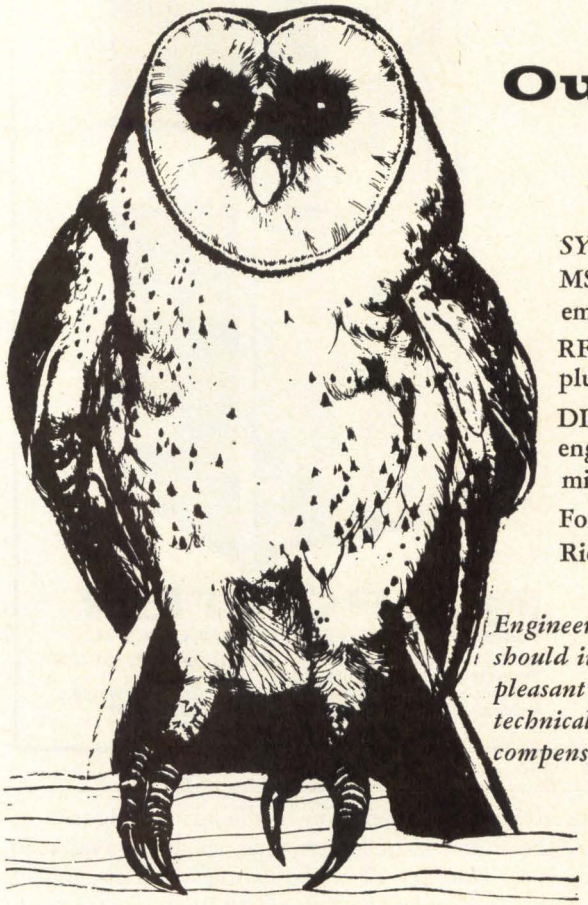
Without going into the details of the arithmetic, it is evident that, unlike degadecimal, the quantity of digits in the product is equal to the sum of the quantities of digits in the two factors, or it is two or four less. In other words, no overflow is possible, and for mechanical division, this may mean that a restore operation could be indicated by an overflow, just as in normal division. To explore in detail the operation of the various algorithms would take much more space than we have available. In fact, if we consider all of the various combinations of using digit product or co-product; addition, subtraction, coaddition, or cosubtraction; and positive or negative digits, we have a total of 2 x 4 x 2 or sixteen different ways to multiply and sixteen different ways to divide. These sixteen ways to divide do not include the methods using alternating diminishing operations and "special" systems which we discussed in Parts 6 and 7.

It is clear that if we had investigated these different possibilities using binary number systems as examples, we should by this time be hopelessly confused in zeros and ones. As it is, we are in some position to draw a tentative conclusion as to which of these many possible systems might be most appropriate for a system of computation using a negative radix. It will be discussed next.

6. Through The Looking Glass

Although much more consideration is required, the arithmetic which appears to be simplest for mechanical operation from all points of view, including division, is one using:

- a negative radix,
- negative digits,
- co-adder modules for addition and subtraction,
- repeated subtraction of digit co-products for multiplication,



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- repeated addition of digit co-products for division,
- a non-restoring division algorithm using both polarity and overflow tests.

Because virtually everything in this list is the inverse of the normal, the title of the Rev. Mr. Dodgson's famous book has been borrowed for this section. And yet, compared with the negative radix arithmetic we have discussed, the arithmetic looks so much like normal arithmetic, that (given stage-level adder-subtractor circuitry) the arithmetic control logic of a conventional computer could almost be used for such relatively complex operations as multiplication and division — even perhaps for the so-called high-speed operations, such as carry-save multiplication. On the other hand, the control logic for addition and subtraction is just as simple as for any negative radix system.

One item of critical importance which should be mentioned, but which is more appropriately discussed under the topic of logic design, is the matter of polarity determination. The logic for this is extremely simple and fast, and is amenable to modular design and incorporation with add/subtract modules. A signal for the polarity of a newly-computed number can be provided at the same instant as the signal for its most significant digit.

This series of articles is complete, but before leaving it, the reader should review that portion of Part 1 entitled "Arithmetic, Computers, and Integrated Circuits." It starts on page 60 of the May 1967 issue. As a final note to emphasize the significance of what is suggested there, we should say that the potential of digital computation using negative radix arithmetic does *not* lie in a small saving of circuit cost or operation time in a computer designed to look and act just like one of the current or future generations of computers. The potential of negative radix arithmetic lies in using it to do things which are impracticable or perhaps even impossible using conventional arithmetic. The challenge, then, is to explore such possibilities, to evolve their designs, and to develop their applications.

A New Design Transmission-Line Adder

Use of directional couplers adds another dimension to logical adder design in that the carry propagations are now free of circuit delays, thereby permitting fast add times without use of additional logical decisions for look-ahead capabilities.

M. H. Bolt, H. H. Nick
IBM Systems Development Division
Poughkeepsie, New York

In the logical design of an adder, we begin by considering the addition of two n-position registers. The following definitions and sum expressions are arrived at by Booleanizing the adder operation of two- and three-position sums, and will allow us to write a general expression for an n-position sum.

Let

P_k = k^{th} bit of the P register
Q_k = k^{th} bit of the Q register
C_k = carry bit from the k-1^{st} position during a sequential add operation between the P and Q registers
S_k = result in the k^{th} position of adding the P and Q registers

Then

$$S_1 = C_1 M_1 + \overline{C}_1 \overline{M}_1$$
$$S_k = C_k M_k + \overline{C}_k \overline{M}_k$$
$$S_n = C_n M_n + \overline{C}_n \overline{M}_n \qquad \text{(Eq. 1)}$$

where C_1 = input carry into the adder

$$C_{k-1} \cdot (P_{k-1} + Q_{k-1}) + P_{k-1} \cdot Q_{k-1}$$
$$\overline{C}_k = \overline{C}_{k-1} \cdot (P_{k-1} + \overline{Q}_{k-1}) + \overline{P}_{k-1} \cdot \overline{Q}_{k-1}$$
$$M_k = P_k \cdot Q_k + \overline{P}_k \cdot \overline{Q}_k$$
$$\overline{M}_k = P_k \cdot \overline{Q}_k + \overline{P}_k \cdot Q_k \qquad \text{(Eq. 2)}$$

n = number of positions in the register, i.e., $1 \leq k \leq n$

Also, $C_{out} = P_n Q_n + C_n \overline{M}_n$ = output carry from the adder.

Before the k^{th} position can produce a correct sum, it must know the condition of the k-1^{st} position or the k-2^{nd} position, etc.; that is, if the bits in the k-1^{st} position are:

$$\left[\begin{array}{l} P_{k-1} = 0 \\ Q_{k-1} = 0 \end{array}\right] \quad \text{or} \quad \left[\begin{array}{l} P_{k-1} = 1 \\ Q_{k-1} = 1 \end{array}\right]$$

then S_k may be computed.

If the bits in the k-1^{st} position are:

$$\left[\begin{array}{l} P_{k-1} = 1 \\ Q_{k-1} = 0 \end{array}\right] \quad \text{or} \quad \left[\begin{array}{l} P_{k-1} = 0 \\ Q_{k-1} = 1 \end{array}\right]$$

then we must look into the k-2^{nd} position.

The following definitions will help generalize the above property:

Let

$\text{Gen}_k^T = P_k \cdot Q_k$ for $1 \leq k \leq n$
No $\text{Gen}_k^T = \overline{P}_k \cdot \overline{Q}_k$ for $1 \leq k \leq n$

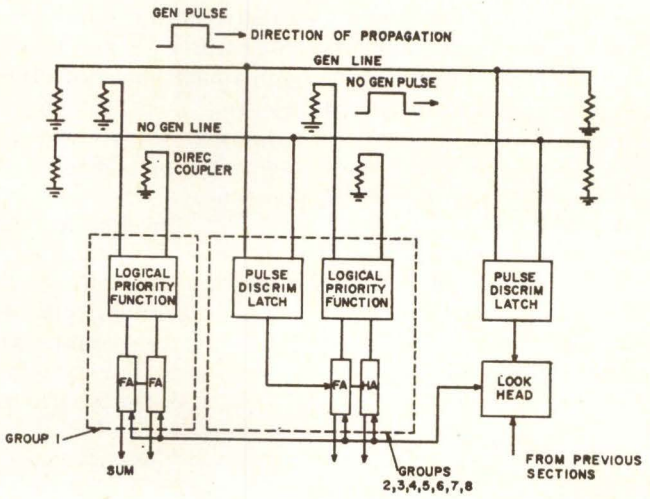

Fig. 1 — Main logic flow

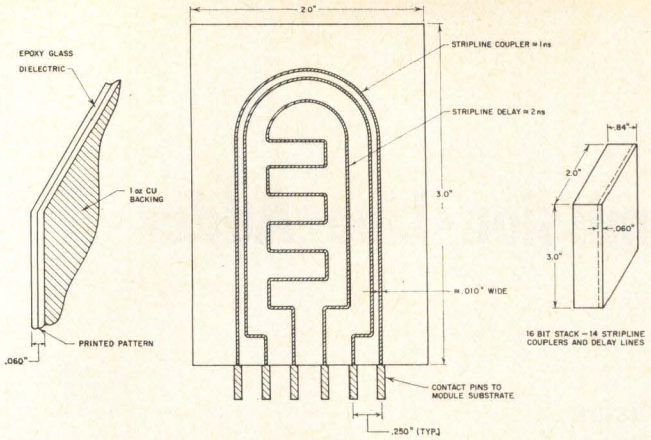

Fig. 2 — Directional coupler assembly

$\text{Gen}_k^R = \text{Gen}_l^T$ for $l < k$ such that if there exists a No Gen_p^T for $p < k$, then $p < l$.

$\text{No Gen}_k^R = \text{No Gen}_l^T$ for $l < k$ such that if there exists a Gen_p^T for $p < k$, then $p < l$.

In order to compute S_k, it is only necessary to establish whether a Gen_k^R or a No Gen_k^R exists. This implies that the lowest-order position of the adder is position 1. The succeeding higher-order positions proceed in a conventional manner, i.e., 2 through n. The establishment of a Gen_k^R or a No Gen_k^R can be accomplished without logical interference if we provide capabilities for each position in the adder to transmit its information (being a Gen^T or No Gen^T) down one of two transmission lines toward the higher-order positions, and each position to sense the transmission lines in order to determine whether a Gen^T or No Gen^T was transmitted. With each position spaced along the transmission lines, and by reserving one line for Gen^T transmission, and the other for a No Gen^T transmission, a Gen_k^R is easily distinguished from a No Gen_k^R because the true signal will first arrive at position k.

General Adder Philosophy and Design

The adder is divided into four main sections; each section consists of 16 add positions and is further divided into eight groups of two positions each. Every two-position group may contain one full adder and one half adder, or two full adders. Two drivers and two transmission line couplers are associated with each group (see Fig. 1), except the eighth group, which does not drive its information onto the transmission lines since there are no further higher-order groups in the section. If the directional couplers are one-nanosecond long when driven by a step of voltage, they will emit a two-nanosecond pulse onto the transmission line traveling toward the higher-order groups in the section.

A logical priority function in each group allows priority to be established by the higher-order position. Should, for example, the higher-order position be required to emit a Gen^T and the lower-order member be required to emit a Gen^T or a No Gen^T, the lowest-order group will be inhibited from any transmission. In Fig. 1, a number of blocks labeled logical priority function, pulse discriminating latch, FA, HA, look-ahead, and their various input/output connections are shown, and the

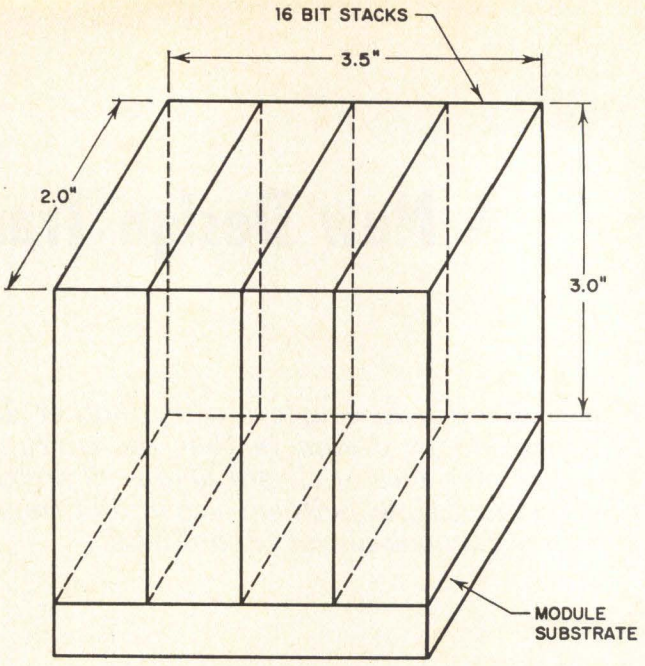

Fig. 3 — Complete adder

diagram also depicts a general section containing, as previously discussed, eight groups and 16 adder positions. The look-ahead circuits are of the standard type and are present at the output of each section of the adder.

A model of the adder was constructed with Gen and No Gen Transmission lines and with the couplers mounted on a series of small cards (2 x 3 x 0.06 inches). When packaged, the cards form one assembly consisting of 14 directional couplers (see Fig. 2). A length of strip line, used as a two-nanosecond delay line, and not part of the coupling mechanism, is packaged on the card for convenience. It is used in the latch circuits as a means of widening the Gen and No Gen pulses. Transmission line continuity is maintained via strip line connections between the small cards that are affixed to a larger card. Connections of circuit modules are made via the large card where the modules are also packaged. There are actually two 3 ft. 9 in. transmission lines packaged in sections on the 14 coupler cards whose assembled dimensions are 2 x 3 x 0.840 inches. The complete adder (Fig. 3) consists of a base card with modules affixed to one surface. Mounted on the other surface are the small pluggable cards containing the directional couplers and the delay lines. The dimensions of the 64-bit adder are 3 x 2 x 3.5 inches.

Summary

Unique features of the new design transmission-line adder are summarized as follows:

- Carry look-ahead within a section is accomplished by transmitting carries via directional couplers along a transmission line.
- Coupling length per group is a function of the pulse width required by the pulse discriminating latch.
- Group priority logic allows the couplers to be spread in a continuous string along the transmission line.
- Allowances for circuit skew may be made by adjusting the spacing between any two directional couplers.

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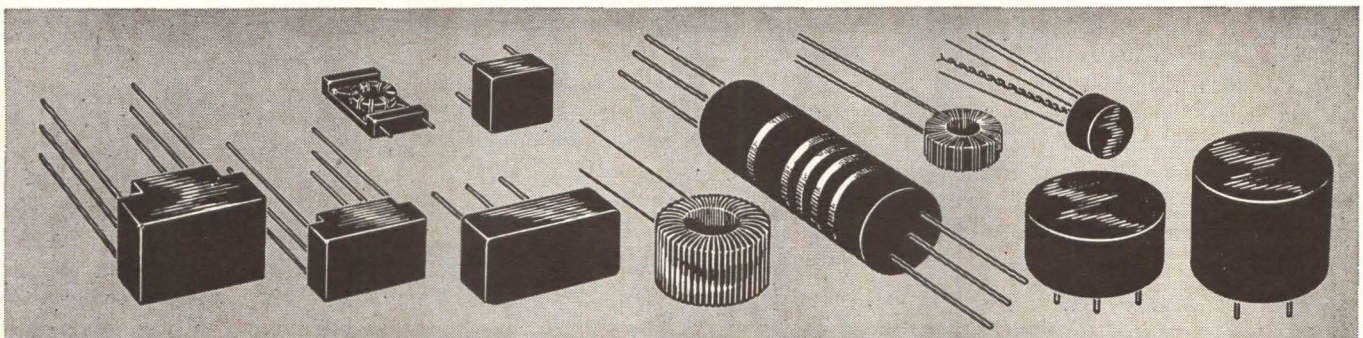

Here are commonly used packages for which tooling is available. Other configurations are always possible.

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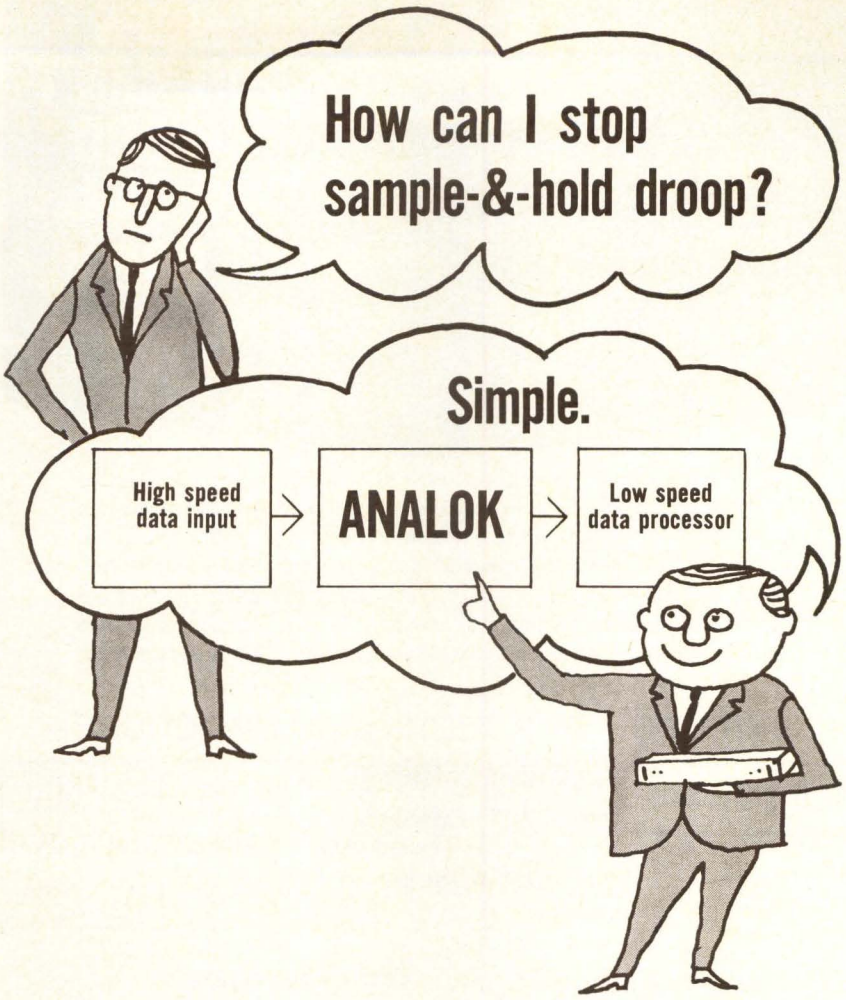

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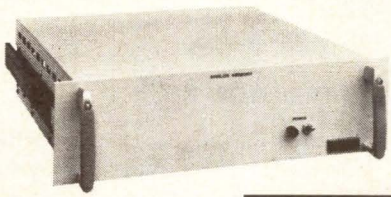

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Circle No. 208 on Inquiry Card

PRECISION X-Y CRT DISPLAY

Model PD900 Precision X-Y CRT Display is a high resolution 5-inch cathode ray tube display specifically designed to offer maximum performance in terms of resolution and speed at the lowest possible cost. It utilizes all solid-state circuitry and is intended for application in film and hard copy recording and film reading. It resolves more than 1700 elements/diameter and is capable of random access X-Y deflection from DC to a slewing speed of 7 microseconds for the full diameter. Small-signal bandwidth is greater than 1 megahertz. Other features include high stability, repeatability and linearity. Mating of the basic option package, OP900, to the Model PD900 display enables the inclusion of optional circuits such as video amplifiers, sawtooth generators and phosphor protection circuits. The

display utilizes a narrow deflection angle cathode ray tube to minimize deflection defocusing and pin cushion distortion. It is a 5-inch flat face magnetically deflected and electrostatically focused tube. Through the use of highly regulated power supplies, temperature stable components and temperature stabilized circuits, exceptional stability and reliability is achieved. The display includes deflection and blanking circuits, CRT and power supplies. Availability: 60-90 days; price: $6,200.00. Beta Instrument Corp., Newton Upper Falls, Mass.

Circle No. 205 on Inquiry Card

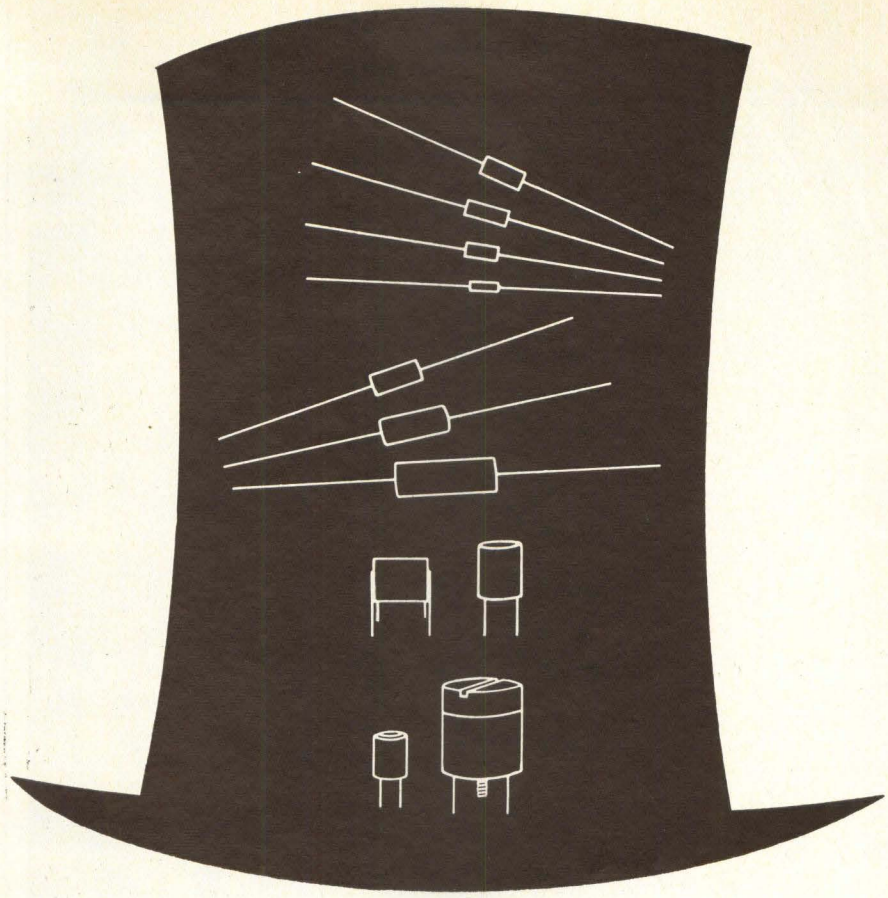
20-MHz IC COUNTER-TIMER

General Radio has announced its first integrated-circuit instrument, a 20-MHz counter featuring eight digits, storage, and programmability of all major functions. The new Type 1191 counter measures frequency, frequency ratio, period, and time-interval. Time base is either a 10-MHz crystal oscillator operating at room temperature or, for extreme stability, a crystal oscillator in a proportional-control oven. Another optional extra is provision for BCD data output. Readout is eight digits of high-intensity neon tubes, with automatically positioned decimal point and units. The basic counter is priced at $1340 in the U.S. With high-precision time base and data output, the price is $1540. General Radio Co., W. Concord, Mass.

Circle No. 212 on Inquiry Card

MOLDED MEMORY PLANE

A new memory plane for coincident current applications in commercial, military and industrial computers is available from Indiana General Corporation. Named Cor-Gard, the plane includes supporting plates to prevent core mat sag, encapsulating compound over solder connections and a foam pad (optional) over the cores, resulting in high resistance to shock and vibration. For ease in stacking, the plane offers these advantages: All X, Y, sense, and inhibit wire terminations are inside the frame, eliminating the chance of damage during handling and soldering; planes fit flush, one against the other, providing structural rigidity; pins of an upper plane can contact pins of a lower plane allowing dip



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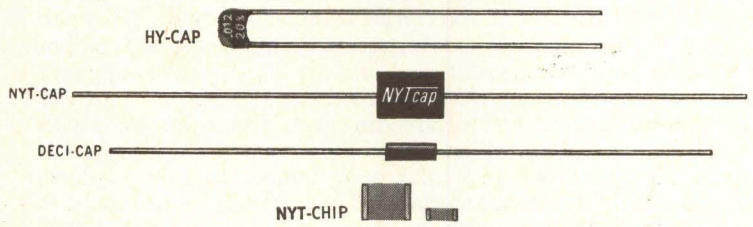

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NYT-CAP: Molded epoxy package 0.1" diameter by 0.250" long.... 4.7 to 220 pf; and 0.350" by 0.250" by 0.1"..... 270 to 4700 pf; T/C does not exceed ±40 ppm/°C (−55°C to +125°C); and 200 WVDC.

DECI-CAP: Epoxy molded envelope 0.100" diameter by 0.250" long.... 4.7 to 27,000 pf; and ±10% tolerance.

NYT-CHIP: 0.170" by 0.065" by 0.070" ...4.7 to 220 pf; and 0.280" by 0.195" by 0.070"....270 to 4700 pf; T/C does not exceed ±40 ppm/°C (−55°C to +125°C); and 200 WVDC.

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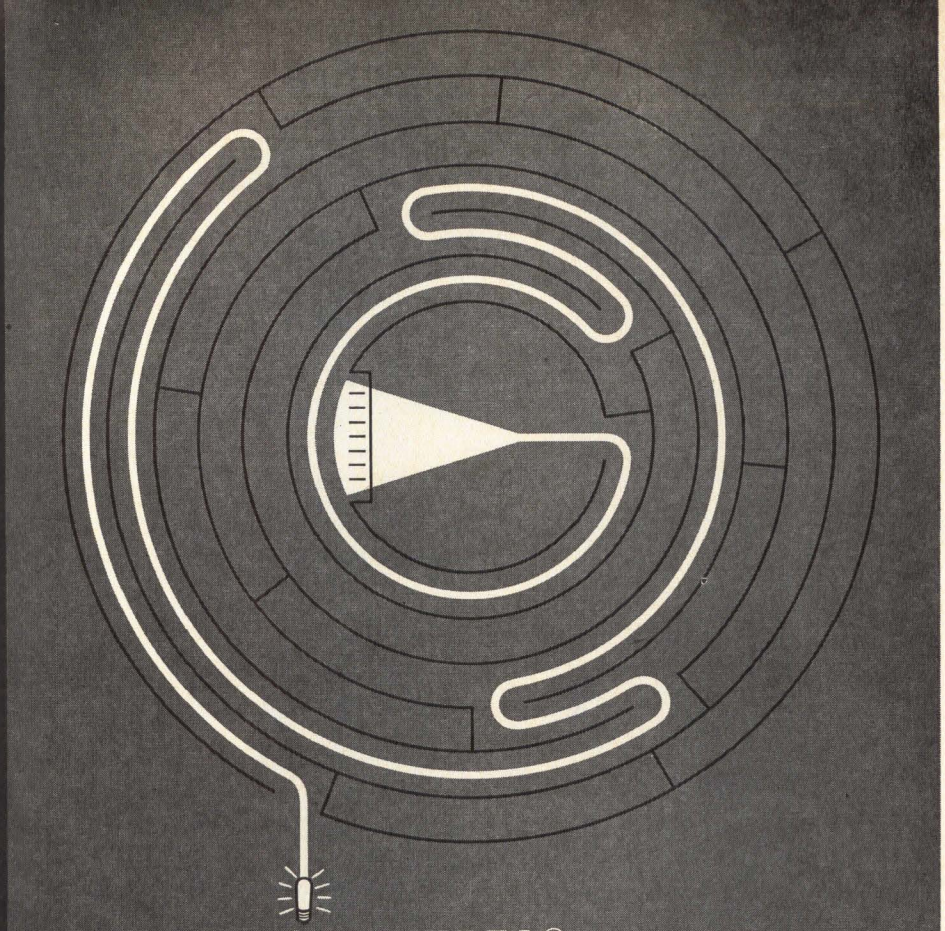

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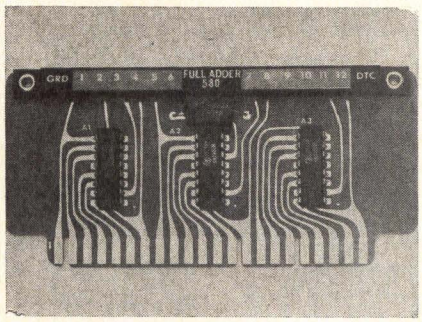
ADVANCING ELECTRONIC/OPTICAL INSTRUMENTATION

soldering; a frame is replaceable (without disturbing any mat wires) by heating the pins and sliding a thin blade between them. Flexibility in design is made possible by accommodating a variety of winding configurations with up to 32 sense and inhibit terminals. The plane is available, off-the-shelf, with 30-mil Ferramic[R] cores in the following matrices: 1 bit — 128 x 128; 2 bits — 64 x 128; 4 bits — 32 x 128; 8 bits — 16 x 128; 4 bits — 64 x 64; 8 bits — 32 x 64; and 16 bits — 32 x 32. The plane can also be strung with 20-mil cores. Although Cor-Gard is designed for coincident current applications, it can be modified for linear select memories on special request. The plane meets temperature requirements of MIL-E-5400 and MIL-E-16400. Electronics Div., Memory Products, Indiana General Corp., Keasbey, N. J.

Circle No. 213 on Inquiry Card



12-BIT ADDER

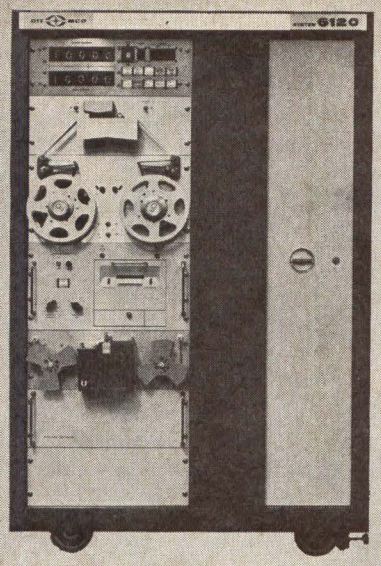
Twelve-bit adder, consisting of three four-bit circuits, performs a four-bit addition in 60 nsec, and a carry in 48 nsec. Test points are provided on all circuit outputs, and a unique color-coded test point strip clearly identifies each test point, without card removal. With power requirements of +5 volts, 78 mA, the unit features a decoupling capacitor for minimizing noise interference, and is compatible with the Blue Chip modules and all DTL and TTL logic circuits. Module size is 5.4″ x 2.16″ with gold-plated 44-pin connector. Data Technology Corp., Mountain View, Calif.

Circle No. 219 on Inquiry Card

TEST PANEL

A telegraph-data test panel for fixed installations has recently been announced, which combines units providing both generating and testing

CIRCLE NO. 40 ON INQUIRY CARD



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CIRCLE NO. 39 ON INQUIRY CARD

facilities. The TMG-3 is a solid state portable test generator that simulates the language of any computer and that programs two characters continuously or one character at a time in 5, 6, 7, or 8-level codes. The new test panel, providing this broad test capability in a fixed installation, will enable communications and other test centers to find trouble quickly, easily, and economically. According to the manufacturer, it has been the habit of small or extremely busy installations to rely on portable test packages for routine testing. This new product, which will measure and test all data signals, also has jacks for testing MIL-188B interface, EIA interface, and conventional teletype loops, so will permit such installations to have an always-available, economical unit to do the same jobs. H. I. Clarkson Associates, Washington, D. C.

Circle No. 217 on Inquiry Card

PRINTED CIRCUIT CORREEDS

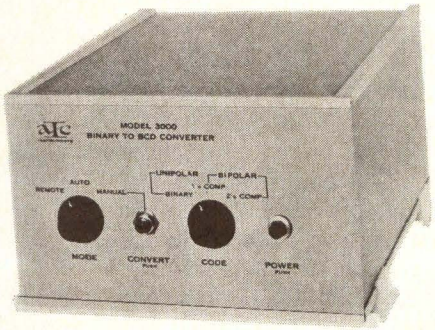
Miniature printed circuit (MPC) correed, compatible with the high-density packaging demanded by the computer industry, has a low silhouette (0.350" above the mounting surface), and is said to simplify equipment and system design. Terminals are located on multiples of 0.050" centers to match circuit board grids. Magnetically shielded coils permit close spacing of modules and improve the sensitivity. Each reed switch in an MPC Correed consists of two overlapping ferro-magnetic blades sealed in a glass capsule, and separated at the overlap by a small air gap. They are plated with rhodium over gold at the contact area. Automatic Electric Company, Northlake, Illinois.

Circle No. 210 on Inquiry Card

MAGNETIC TAPE

"Minireels" of magnetic computer tape, 200 feet on a 6-inch reel, are designed to fill a gap in tape packaging resulting from the growing use of remote auxiliary data processing units. In addition to facilitating mailings from such units, the small tapes also offer cost-savings where the relatively limited data do not require standard 2400-foot reels. "Minireels" also make possible greater efficiencies where magnetic tape input equipment is used to replace punch card operations. Both Audev K-61 and Audev K-68 are offered in "Minireel" form. Audev K-68 is a newly-introduced magnetic computer tape that features specially balanced characteristics for extended reliability in modern digital computer systems. Audio Devices, Inc., New York, N. Y.

Circle No. 207 on Inquiry Card



BINARY TO BCD CONVERTER

A new Binary to BCD converter, which translates binary inputs into a 1-2-4-8 BCD output at a rate of one

micro-second per decimal digit, accepts unipolar binary inputs, or bipolar inputs in one's complement or two's complement code. Binary inputs of up to 20 bits with corresponding BCD outputs of up to 6 decades are available. Conversion capacity of units with less than 20 bits input can be expanded at any time by addition of plug-in cards. The all solid-state Model 3000 converter uses silicon transistors throughout and integrated circuits in the logic circuitry. It is packaged in a 5¼" high, 8½" wide, 12" deep box. Price $375.00 up. AIC Instruments, Div. of AIC Corp., Houston, Texas.

Circle No. 218 on Inquiry Card

IC VOLTAGE REGULATOR

Designed to power integrated circuits in computers, control, automation, GSE, and other systems using digital logic, a new device is said to advance the state-of-the-art of voltage regulators to that of integrated circuits. Markedly improved performance is claimed because this I. C. voltage regulator 1) dissipates only 20% of the power consumed by conventional regulators; 2) distributes power to digital systems in the form of higher voltage and lower current; 3) delivers high current only at the point of installation; and 4) reduces system noise by reducing buss bar currents. Circuitry and operating characteristics conform with integrated circuit requirements. Size: 1-9/16 x 1¼ x ½ in. high. With an output power of 2.5 W., unit provides an output voltage of 4.5, 5.0, or 5.5 VDC from a nominal input voltage of 20V. Efficiency at full load: greater than 65%. Designed to operate in the 0° to 65°C. temperature range. Gar Enterprises, Pasadena, Calif.

Circle No. 216 on Inquiry Card

MAGNETIC CORE MEMORY

Model DC-31 Magnetic Core Memory is a compact 2D high-speed device featuring random access operation with full cycle time of less than 900 nanoseconds. Memory access time is less than 450 nanoseconds. Maximum capacity of the unit is 1024 x 12 in one bit per word increments. Prices for the new unit start at $1210 and delivery can be made in 30 days. Datacraft Corp., Fort Lauderdale, Florida.

Circle No. 235 on Inquiry Card

LOGIC TRAINER

A digital logic trainer designed especially for the teaching of digital computer logic is said to use 60 separate basic computer circuits, identical to those employed in computers in industrial and commercial use today, to enable the student to construct computer logic circuits. Each of the 60 circuits is screened on the front panel and corresponds to the logic diagram in the student manual which accompanies the trainer. This versatile device may be used in the teaching of computer maintenance and logic systems breadboarding. A telephone dial and numerical display panel combine to serve as an input-output device which simulates entering and retrieving data from a computer. Designed for continual use, the unit uses solid-state components mounted on individual printed circuit boards. It also contains built-in short-circuit protection. A removable rear panel provides access to all components for instruction in computer maintenance and servicing. Digital Electronics, Inc., Plainview, L.I., N.Y.

Circle No. 243 on Inquiry Card.

HYPERBOLIC CONTACT

A hyperbolic contact for use in all electrical connectors and interconnection devices utilizes a design concept that is basically linear generatrices of a hyperbola achieved by stringing very fine wires inside a tube at some angle to the tube axis and securing these wires to the tube ends. The tube then receives an outer sleeve with the appropriate terminal (solder cup, pin, turret, wire wrap, etc.) and the socket is complete. The inserted pin is "hugged" in a grip of taut wires. Extremely low contact resistance, low insertion/extraction forces, over 100,000 mate/unmate life cycling, and no noise (discontinuity) at high shock or vibration levels are achieved by the hyperbolic wire design. High density, multiple pin connectors are capable of being mated and unmated by hand, thus permitting lighter and less expensive jacking or locking devices. This contact design is applicable to all common and many non-standard connector configurations including cylindricals, rack and panel, edgeboards, etc. Contacts will be initially available in size #'s 26, 20 and 16, and later in all other commonly used sizes. The insertion/extraction forces and contact resistance parameters may be varied by changing the angle of inclination of the wires and/or the number of wires in the socket. Increase of angle within the range 6°-10° increases insertion/extraction forces and decreases contact resistance. Increasing the number of wires employed produces the same effect. Wire materials are normally phosphor bronze or beryllium copper. With variations depending on connector materials, accessories, finish, specifications, etc., price per mated contact pair will begin at 6¢ to 9¢. Industrial Electronic Hardware, New York, N.Y.

Circle No. 244 on Inquiry Card.

PROGRAM BOARD

A new program board engineered for machine-tool programming applications features 12 x 33 hole format and 12 x 3 spares for pin storage. It will permit pre-selection of spindle speeds and tool selection, and is supplied drilled for lights to indicate program step and active functions per step. The board is supplied with engraving for easy program set-up of machine tool functions and is supplied with a drilled cover panel for indicator lamp mounting. Sealectro Corporation, Mamaroneck, N.Y.

Circle No. 246 on Inquiry Card.

SNAP-IN INDICATOR

Snap-in neon glow indicators feature long operating life, low cost and are self-securing for dependable electrical connections. Simple, square lenses permit the indicators to be mounted exactly side-by-side for compact installations, and lend themselves to a wide variety of applications as panel indicator lights. Two models are available in different neon lamp intensities: a bright bulb intensity for a 5,000 hour operating life, and a medium intensity for a 25,000 hour life. Each is available in red, clear, amber, and opal for color coding various circuits, switches, parameters, etc. All assemblies are complete with lamp; incandescent models available 4 to 28 volts. Chicago Switch, Chicago, Ill.

Circle No. 247 on Inquiry Card.

COMPOSITING SYSTEM

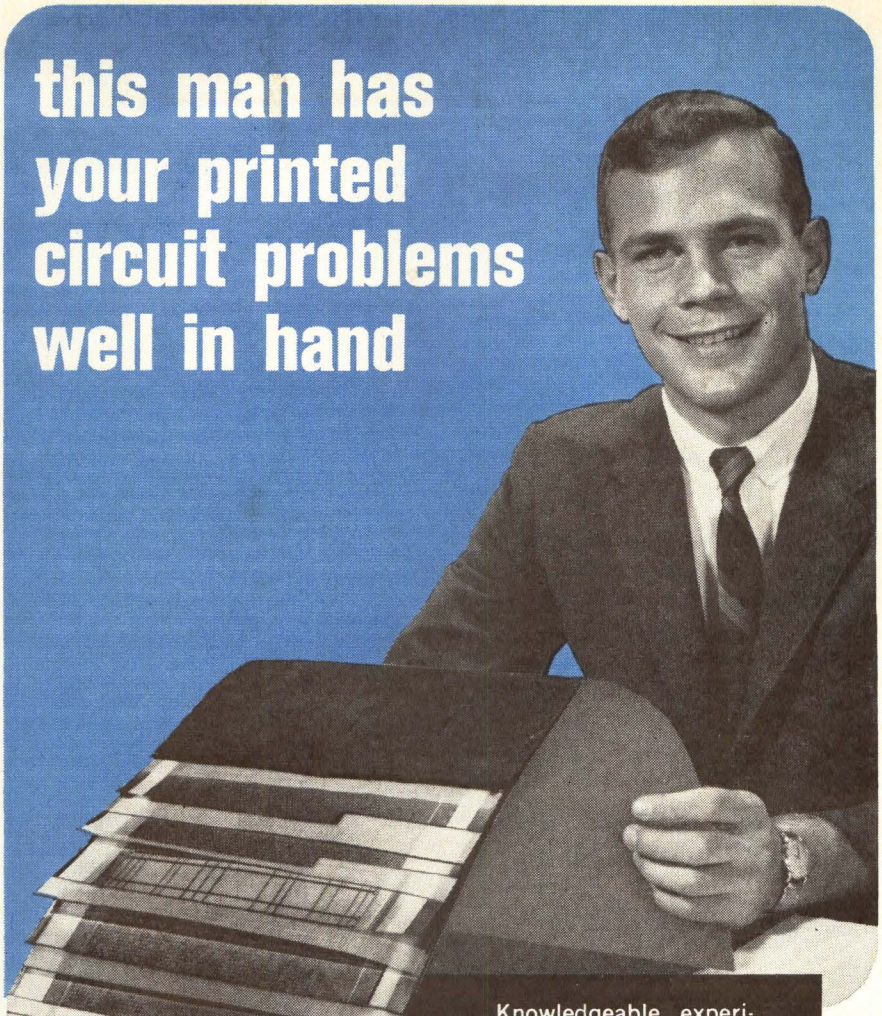
A portable integrated digital compositing system employing disk pack and a core memory provides rapid access to limited amounts of data. Coupled with this is the random access disk pack capable of holding in excess of six million bits of data. The system concept replaces the tape loop as a mass storage medium. From an operator's viewpoint, the entire memory system can be thought of as a nearly instantaneous access, 6-million bit, all-electronic memory. The primary features of the compositing system are: continuing normalization during compositing operation; compliance with either SEG format A or B (it has an exponent resolution of 6db); stacked conventional recordings, fixed gain recording, and binary gain recordings (since it incorporates floating point addition it will accept the information with or without gain coding information); instant start capabilities because of its random access feature (no tape or other mechanical changes are necessary when changing sampling rate and length of recordings); reliability far exceeds tape loop systems because disk files are practically error free. Dresser Ind., Houston, Texas.

Circle No. 249 on Inquiry Card.

STEPPING MOTOR SYSTEM

A computer-controlled system incorporating both software and hardware is now available for use in stepping motor applications. The computer automatically selects the motor to be driven and programs its operation according to a prescribed stepping sequence. If the application requires that the computer control a number of stepping motors, they can be accommodated on a real-time basis, including positive regulation of their acceleration and deceleration characteristics. Feedback from transducers governing how far these motors are to be moved on the basis of readings from an analog-to-digital converter is also assimilated by the new system. Typical applications include numerical control machine problems, computer-controlled gain systems, circuit synthesizing networks, and stage lighting control systems. IRA Systems, Lexington, Mass.

Circle No. 250 on Inquiry Card.



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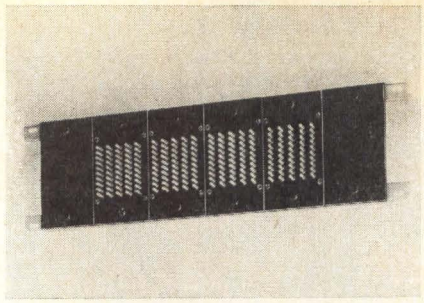

PROGRAM BOARD

A 10 x 20 captive pin programmer, featuring modular construction and bussed upper-individual lower contacts, mounts in a standard 19″ cabinet rack. A maximum of six 10 x 5 individual modules can be grouped in the board to provide up to 10 x 30 of program selection. Features include spare "blank" panels and pins that "make" in the up position. Pins and contacts are available with either gold or silver plating for minimum contact resistance. The design employed permits rapid programming and program cancellation. Sealectro Corporation, Mamaroneck, New York.

Circle No. 211 on Inquiry Card

IC SENSE AMPLIFIERS

A new generation of integrated circuit sense amplifiers, called series 7520N, are designed for high-speed coincident-current computer memory systems. The ICs detect bipolar, differential-input signals from the memory, and provide a faster, more stable interface between memory and logic sections than previously available sense amplifiers, either in discrete or integrated form. Low-level pulses originating in the magnetic-core memory are detected and translated into logic levels compatible with standard TTL or DTL circuitry. The computer designer may choose from three basic circuit designs — two versions of dual preamplifiers driving common-output circuits, or two complete sense amplifiers in a single package. Two threshold levels for each of the three basic circuits provide additional design versatility. Series 7520N sense amplifiers offer substantial cost savings because of four factors. First, dual amplifiers in a single chip inherently cost less than two separate packages. Second, a selection from six different combinations of circuit complexity and threshold sensitivity enables the designer to use and pay for only that level of performance actually needed. Third, a high degree of integration reduces the amount of peripheral circuitry required. And fourth, encapsulation in a 16-pin dual in-line plastic package reduces assembly cost. The SN7520N and SN7521N sense amplifiers include dual preamplifiers driving a common-output circuit consisting of two cascaded TTL NAND gates, each with external gate inputs. Complementary-output logic levels compatible with standard TTL, and two strobe inputs permit application flexibility. Differential input threshold voltage for the SN7520N ($V_{ref}=15$ mV) ranges from 11 to 19 mV, while the SN7521 ranges from 8 to 22 mV. Threshold-voltage levels of the SN7522N and SN7524N are the same as the SN7520N, and the SN7523N and SN7525N correspond with the SN7521N. These input threshold levels are virtually drift-free over a wide range of power-supply voltage levels (15 to 40 V) and temperature ranges (0° to 70°C). This stability is the result of a "matched amplifier" design, based on matched resistor ratios rather than absolute values. The SN7524N and SN7525N units include two completely independent but simple sense channels in a single chip. A common reference voltage establishes the threshold level on both channels simultaneously. The outputs are TTL gates with high fan-out. Typical characteristics of the entire series are low propagation delay (25 nsec input-to-output and 15 nsec strobe-to-output), fast overload recovery time to both differential and common-mode signals (20 nsec with 2-volt input), and high d-c logic noise margin (1 V). Independent strobing of dual sense-input channels permits signal detection to take place when signal-to-noise ratio is at a maximum. Logical "1" output is 3.9 V and logical "0" is 0.25 V. Supply voltage is ±5 V. The new sense amplifiers are available in production quantities. Prices at the 100-999 quantity level are $13.20 for SN7520N, $10.10 for SN7521N, $12.65 for SN7522N, $9.50 for SN7523N, $11.90 for SN7524N, and $8.90 for SN7525N. Texas Instruments, Dallas, Texas.

Circle No. 232 on Inquiry Card

D/A CONVERTER SYSTEM

An integrated circuit digital to analog converter system, designed for use as an output device for general purpose digital computers, Data Loggers, PCM Decommutators or systems outputting address and data in a parallel binary multiplex, accepts 8, 10, or 12 bit binary data at rates up to 100-kc. The system includes front panel mounted thumbwheel switches which allow decommutation of any 16 selected words from the multiplex source. Analog output signals from the converter are plus or minus 10-volts with output currents to 100 milliamps. The device includes such options as bi-level channels, bi-polar operation, and sub-frame decommutation, thus providing many possible operational configurations for custom system applications. Discon Corp., Fort Lauderdale, Fla.

Circle No. 233 on Inquiry Card

TAPE READER

The Model 1282 paper tape reader is a low cost, asynchronous device adaptable to a wide variety of paper and mylar tape processing applications. The standard unit reads 8-level 1 inch tape; other models are available for 5, 6, and 7-level narrow tapes. Extremely compact and reliable, the reader offers positive interrogation of even those tapes that are well worn or that exceed EIA hole-to-hole tolerances. Paper or mylar tape is advanced and sensed at up to 30 characters per second, asynchronously. A push-button permits manual advance of tape. The extremely small size of the tape reader (4″L x 3¾″H x 1½″W) permits it to be mounted on the same plane as the tape spools; no separate mounting plate or rear mounted driving motors are necessary. Shock mounting is available as an option. The pin sensing method ensures long tape life because the pins do not rub against the tape but are withdrawn when the tape is in motion. Even when sensing, each pin exerts only 20 to 30 grams of pressure against the tape. In current life tests, the reader has sensed and advanced standard parchment tape over 10,000 times without tape damage. No external drive mechanism is required. A single external advance

pulse (45V, 6.5 amp peak) is used to feed and interrogate tape. Driver units are available as separate assemblies. Internally timed, the tape reader is controlled solely by the inertia of its few moving parts, a characteristic which never varies. It requires a minimum of lubrication and field adjustment. Price is $295 and is available from stock. Navigation Computer Corp., Norristown, Pa.

Circle No. 234 on Inquiry Card

LOW POWER DTL IC's

Low power DTL integrated circuits are available in a new ceramic-and-metal "dual in-line" package with "plug-in" capability. Called the "CD2200D Series," the low power DTL circuits are electrically identical with the RCA CD2200 Series, but utilize the ceramic-and-metal 14-lead "dual in-line" package employing the popular 100-mil lead spacing and 300-mil spacing between rows. This package provides "plug-in" capability and embodies several unique design features which contribute to its reliability, hermeticity, and ruggedness. The hermetically sealed ceramic units are designed for application in aerospace and airborne computers, portable military equipment, instrumentation and industrial control equipment and other applications where circuits with low device dissipation and high noise immunity are primary design requirements. Features of these low power DTL integrated circuits are: low device dissipation of 2.3 mW per gate or 7 mW per flip-flop; full military operating temperature range of −55°C to +125°C; low impedance T^2L type output; excellent noise immunity of 1200 mV typical at 25°C; and typical flip-flop clock frequencies of 3 MHz for a fanout of 5. RCA Electronic Components and Devices, Harrison, N.J.

Circle No. 236 on Inquiry Card

DELAY MODULE

A 5 MS delay module employs a magneto-strictive delay line in the RZ mode and interfaces directly with DTL 930 micrologic and TTL. Designated model 213A/RZ-9, the new module is designed specifically for logic and information processing engineers who desire a digital delay module for direct interface with their integrated circuitry. Only input pulse data and a suitable power supply are required for operation. In addition, the module easily converts into a serially-recirculating memory through the addition of an external feed-back loop with appropriate gating and clocking. The device features a maximum delay of 5 MS with a 1 MHz prf. Power supply requirements are +10 volts DC, ±10%, 56 ma; −10 volts DC, ±10%, 20 ma and +5 volts DC, ±10% at 35 ma. Sealectro Corporation, Mamaroneck, New York.

Circle No. 237 on Inquiry Card

ON-LINE INPUT DEVICE

A versatile, low-cost, on-line computer input device that rapidly and accurately transmits alphanumeric and graphic information as a function of its X-Y page position is said to require less communication time and bandwidth than keyboard type computer terminal devices, reduce operator errors, and permit fast, economical information handling in applications such as hospital and management information systems, reservation systems, planning, production and inventory control, and computer-aided teaching. Called Datacoder, it consists of a traveler and manually operated cursor linked to wipers on a pair of X-Y 8-bit Grey encoder boards. The introductory model of the unit is fully enclosed in an 18″ x 20″ x 3″ cabinet, and has a 12½″ x 10½″ active working area. The Datacoder is used in conjunction with a teletypewriter in a remote, time-shared computer terminal. In operation, possible input data are typed out in list form (up to 63 lines of standard teletypewriter printing per sheet) by the computer, which maintains an image of the location of individual items on the list. After placing the list on the Datacoder, the operator selects an individual item with the cursor and presses the "Transmit" button. The X-Y coordinates of the selected item are sent to the computer, and the item is identified by comparison with its retained image on the list. In graphic-to-digital applications — such as transmitting

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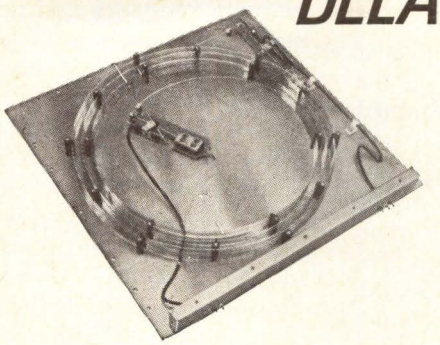

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data from charts, graphs, etc. — the operator selects the graphic data to be digitized with the cursor. The encoder boards are strobed from an external source when the "Transmit" button is pressed. This provides a direct digital output of the X and Y coordinates of the cursor. Data can be transmitted from hard copy or from film and slide images projected through the Datacoder's translucent working surface. Accuracy is better than ±0.5%; resolution is 1 part in 256. Small quantity price is $995.00. Bolt, Beranek and Newman, Santa Ana, Calif.

Circle No. 221 on Inquiry Card

WIDEBAND DC AMPLIFIER

Gains up to 12,500 at very low noise levels are possible with a new wideband dc data amplifier. Called Model 2820, it is a direct-coupled, active guard differential amplifier designed for research instrumentation and data acquisition. In addition to low noise the unit features outstanding rejection of RF interference, wide bandwidth, and a high level of common mode rejection. Full scale output is ±10 volts and ±100 mA. It provides differential isolation between the input signal source and output common. No common mode return path is required to achieve a common-mode rejection of 120 dB, dc to 60 Hz. If desired, the amplifier may also be used as a single-ended unit, inverting or non-inverting, in applications in which either the signal source or the load is isolated from ground. System noise contributed by the amplifier circuitry is exceptionally low. The noise referred to the input at a gain of 1,000 is less than 4 microvolts rms at full bandwidth and less than 1 microvolt, peak to peak, at a 10 Hz bandwidth. Gain controls include specific gain settings, plus a vernier that covers a range equal to 2½ times the nominal gain setting. The result is a continuously variable gain from the lowest setting to 2½ times the highest setting. Up to eight amplifiers fit in a standard 7-inch by 19-inch rack supplied by the manufacturer. Dana Laboratories, Inc., Irvine, Calif.

Circle No. 222 on Inquiry Card

MEDIUM CURRENT SILICON RECTIFIERS

A new series of medium-current silicon rectifiers is said to meet the moisture resistance specifications required by glass-to-metal seal types. Designated Series M, these rectifiers offer stable uniform electrical characteristics by using a passivated double-diffused junction technique. Using compact tubular construction, Series M rectifiers incorporate pure silver axial leads to facilitate point-to-point circuit soldering and to provide excellent thermal conductivity. Many stud-mounted types can be replaced by this design and reduced assembly costs are claimed. Standard and bulk avalanche types are available in voltage ratings from 50 to 1000 volts PIV and currents range from 1.5 to 3.0 amps. Edal Industries, Inc. East Haven, Conn.

Circle No. 227 on Inquiry Card

COMPUTER GRAPHICS SYSTEM

A high precision CRT display system, which has been signed for real-time and analytical off-line applications, includes a 16-inch cathode ray tube masked to a 10.24 by 10.24 inch image area, vector generator, intensity compensation logic, electromagnetic deflection network, maintenance controls and a digital control unit. Standard system options include a high-speed character generator, line texture control unit, light pen, function switches and a computer graphics processor. Systems Engineering Labs, Ft. Lauderdale, Fla.

Circle No. 226 on Inquiry Card

CHIP CAPACITOR

Introduction of a broad line of miniature chip capacitors, to be used in thick or thin film hybrid circuits for filtering, buffering, bypass, coupling, timing and tuning applications, has been recently announced. The K1200 bodies are available in a capacitance range of 120pf to 3.3 Mfd with voltage ratings of 50, 100 and 200 VDCW. Standard tolerance is ±10%, with ±5% and ±20% available. Sixteen body configurations are scaled from .075" x .035" x .040" to .865" x .595" x .080". The monolithic chips have silver electrodes as standard, with gold or palladium gold also available. The precious metal electrodes provide excellent bonding characteristics for mounting by soldering or welding. The chips are manufactured through an exclusive process which insures the stability of the electrical characteristics while optimizing high capacitance packing into small physical size units. Moisture resistant and contamination free, the chips meet all applicable paragraphs of MIL-C-11015 and MIL-C-39014. Prices range from $.13 to $1.86 in production quantities. Availability is 10 days. U. S. Capacitor Corp., Burbank, Calif.

Circle No. 225 on Inquiry Card

SIX FORM "A" REED RELAYS

Designed for low-level switching, multiplexing and many other switching applications, a new reed relay card provides six Form "A" normally open single-pole single-throw contact relays each controlled with a 3-input driver. The reed contact is closed when all three inputs to each driver are true and open when any one of the three inputs is false. Only one +5v power supply is required. Each IC driver is protected from reverse surge by diodes mounted on the card. The IRR-2293 sells for $84.00. Delivery is stock to 4 weeks. Form "C" (make before break) single-pole double-throw contact relays are available as IRR-2294. Price is $100.00. Electronic Engineering Co., Santa Ana, Calif.

Circle No. 224 on Inquiry Card

FIVE-INCH-ROUND CRT

A compact high-brightness CRT that features 70 degrees magnetic deflection and a 0.004-inch (4 mil) line width has been developed for use in precision airborne radar and other monitor display applications. The CRT's 5-inch-diameter, aluminized faceplate allows 90 percent light transmission. The electrostatically focused tube weighs only one pound, is less than 8 inches long, and has a 0.87-inch-diameter neck. It can be mounted in any position and is inherently rugged. Other important features of the unit include flying leads and low deflection power. Although normally supplied with phos-

phor P31, it is available with most standard JEDEC phosphors to suit various applications. Westinghouse Electronic Tube Division, Elmira, N. Y.

Circle No. 223 on Inquiry Card

DDC CONTROL OF BATCH PROCESSES

BATCH, a software system designed to simplify programming for direct digital control of batch sequence processes, is designed to run in a minimum of core memory. The new system can be easily learned and applied by process people who do not have a background in computer technology. Process engineers may write batch process control programs using 12 basic control statements such as CONT (Contact Output) and SETV (Set Value). BATCH can reduce the cost of a batch process computer system by reducing programming time by the vendor or user. The system has been used successfully to program batch processes in textile mills and chemical plants and has shown promise for use in the start-up and shutdown of continuous processes. BATCH consists of a language, a compiler and an operating system. The compiler converts the language into an operational sequence control program. The operating system executes the compiled statements and implements the actual sequence control. Foxboro Co., Foxboro, Mass.

Circle No. 242 on Inquiry Card.

VOLTAGE REGULATOR

A hybrid, cermet thick-film, adjustable d-c voltage regulator, Model 806 can be externally adjusted to provide any output from +3 to +9 volts with ±0.1% regulation for both line and load variations. It is short-circuit proof and has a current handling capability of 0.5 amps. Operating temperature range is from −55°C to +125°C, and power dissipation is 5 watts at +25°C with heat sink. All units are fully sealed and environmentally tested to meet the most stringent aerospace and military specifications. The new solid-state regulator measures only 1″ x 0.5″ and is 0.170″ high. Beckman Instruments, Fullerton, Calif.

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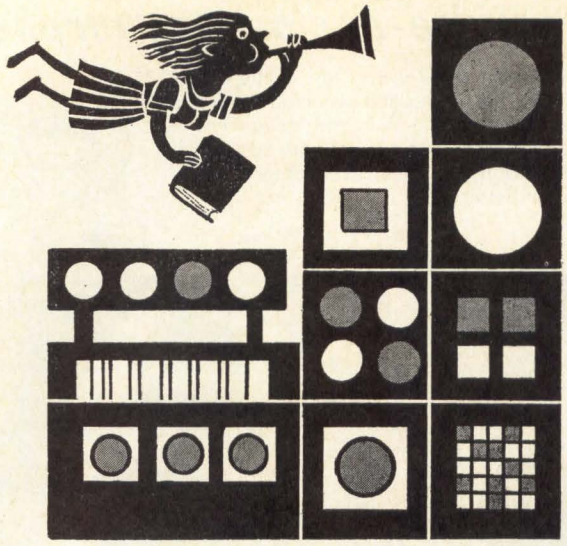

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DESK-TOP READER

Developed by Motorola Instrumentation and Control, a desk-top reader, called "MDR-1000", provides a simple means of entering into a data processing system, in computer language, data marked or punched on cards or marked on standard 8½" x 11" documents. Cards can be fed into the device singly or automatically in batches of up to 500 with an optional automatic hopper.

The reader offers systems designers a new, low-cost method of getting raw data, right from the source, without need for skilled data processing equipment operators. In addition, the unit is small enough (16¾" wide by 16¼" deep by 9¾" high) to fit almost anywhere.

The MDR-1000 produces a standard USASCII output that is compatible with standard telephone transmission interfaces for long-distance transmission or directly with standard data processing equipment, such as teletypewriters, tape recorders, or computers. Cards fed to the optical-read head can be either tab-punched or pencil-marked (mark-sense) or carry a combination of both types of data. Thus cards can be prepunched with certain basic or identifying data for later variable data marking by field personnel.

Also, the device will accept mark-sense data from the edge of page-size documents, in a 12-row band equivalent to a standard tab card. Input format for the reader is standard Hollerith coding arranged in either 80- or 40-column spacing. Data can be handled in either bit serial or bit parallel form. Bit serial data rates can be either 10 characters per sec (110 bits per sec) or 105 characters per sec (1050 bits per sec). Bit parallel data rate is 75 characters per sec (750 bits per sec). Parity can be either odd or even.

Besides USASCII, other codes, such as BCDIC, PTT6, and Binary are available on request. Document rates at 10 characters per sec are 5 sec per card for 40-column spacing and 10 sec per card for 80-column. At 105 characters per sec, document rates are 0.5 sec per card at 40-column spacing and 1 sec per card at 80-column spacing.

Communications facilities can be either a 150-Baud channel or voice-grade circuit. The telephone transmission is by Data-Phone Model 202C, 103A, or their equivalents. The electronic interface is dry contact, EIA standard RS-232B. Manual feed is standard, but automatic card feed with a hopper capacity of 500 cards is optionally available. Power requirement is 115 volts AC, 60 Hz. Motorola Instrumentation and Control, Inc., Phoenix, Ariz.

Circle No. 220 on Inquiry Card

ELECTRONICS ENGINEERING POSITIONS IN SOUTHERN CALIFORNIA

Lockheed Electronics Company is the fastest growing commercial computer memory systems company in the country today. Its engineers are involved in all phases of memory systems technology, from the smallest ferrite cores to the largest sophisticated systems. The company is staffed with an engineering team with many years of digital circuit logic and systems design experience.

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FILM RESISTOR NETWORKS

Eight new standard tin-oxide film resistor networks that exhibit high volumetric efficiency and low noise characteristics are now available for applications where tight packaging of components is required. Number of resistors on a single network range from two to nine. Each network contains one more pin, or lead, than the number of resistors. Resistance values range from a minimum of 20 ohms to a maximum of 250K, depending on purchase tolerance. The eight resistor network types have purchase tolerances of 1, 2, or 5 percent. Also available on special order are networks with 0.5 and 10 and 20 percent tolerances. Tracking between resistors on a single network substrate is typically less than 50 PPM. Resistance values on a single substrate can be matched to 0.5 percent of nominal resistance. The 200 PPM TC of the networks is guaranteed over a range of −55°C to +165°C. A TC of 150 PPM is typical over this temperature range. Load life change is guaranteed to be less than 1.0 percent under tests specified in Mil-R-10509F, characteristic D. Resistance change under low temperature operation at −65C is typically 0.1 percent and is guaranteed not to exceed ±0.25 percent. Resistance change due to moisture is guaranteed not to exceed 1.5 percent when the units are subjected to 90-98 percent relative humidity at 25C to 65C for 240 hours. Corning Glass Works, Electronic Products Division, Raleigh, N. C.

Circle No. 229 on Inquiry Card

DIGITAL PLOTTER

A built-in photoelectric punched-tape reader (with self-contained tape handler), integrated circuit electronics, and a versatile manual control panel are central highlights of the Model 501-1 Digital Plotter. The series, the manufacturer reports, retains all the features of previous first-of-kind lines of equipment which function to produce permanent 3-D removable hard-copy graphs/charts/records from a compact, self-contained desk-height cabinet. Typical uses and fields of application for this unit are cited to include stress and strain measurements, economic growth, urban renewal, traffic engineering, highway design, earth moving, statistical data, historical trends, antenna patterns, servo analysis, circuit analysis, seismic waves, magnetic and gravitational fields, natural resources, ocean currents, demonstration models. Also, design aids, wind patterns, barometric pressures, temperature, ocean floor, salinity, undersea tracking, nuclear measurements, heat flow, electro-magnetic fields, population maps, income distribution. And, teaching aids, race distribution, missile trajectories, aircraft tracking, submarine movements, relief maps, mathematical analyses, earth's strata, industrial design models, others.

The primary feature of the new built-in tape reader incorporated in Model 501-1 is a self-contained tape handler — handling up to 175 feet of paper tape or 500 feet of mylar tape, on easily removable 4-inch diameter tape reels. From this capacity, average size 3-D plots may be prepared with but a single tape loading. Quick rewinding is also a feature of the tape handler. The electronic control section uses DTL integrated circuit logic and all silicon semiconductors. Result is a high degree of noise immunity, plus 0° to 70°C operating temperature range for high reliability. Circuits are mounted on color-coded plug-in cards, with color-coded test points for ease of servicing and maintenance. The manual control panel features a convenient control layout. Here, a single control is provided for simultaneously resetting the X, Y, and Z axes of the plotter before starting a plot. Make-up of a plot is a series of vertical wires firmly fixed into lightweight, removable plotting board, 12" x 18" x ½-inch. Visible from any angle, plot displays mathematical functions or empirical data involving any three variables. The new system operates to receive data in incremental form from eight level punched paper-tape. Data points may be placed anywhere on board within the resolution of positioning mechanism. Stepping motors, internal wire-spool supply, wire cutter mechanism all are within the console. Also included with Model 501-1 is a special Fortran program, PINPLOT, to prepare incremental punched-paper tape for operation of the plotter. This program features scaling, optimizing point density, ordering data. Special requirements may also be met, upon request. Spatial Data Systems, Goleta, Calif.

Circle No. 251 on Inquiry Card.

DATA PHONE INTERFACE

A Data Phone Interface has been designed to complete the connection between any digital data generating, recording, or handling device and the Bell System Data Phone Series, and other similar modems. The DPI-1 can be supplied as a rack mounted unit or in a convenient case which sits beneath the 202-C and supports it, the entire assembly being approximately 1½ inches higher than the Data Phone alone without occupying any additional surface area. The device accepts parallel characters up to 10-bits in length and transmits them serially over the Data Phone link. It also receives serial characters from 5 to 10 bits in length, and presents them in parallel to the user. The unit can be supplied to match any common user signal levels, while its interface with the Data Phone conforms to the EIA RS-232 A specification. The DPI-1 generates its own bit rate clock for transmit and receive, while the user controls the character rate. The interface automatically detects, and resets, false starts due to line impulse noise in the receive mode. Infotech, Westbury, N.Y.

Circle No. 254 on Inquiry Card.

Woven Ribbon Cable

New flat ribbon cable's unique feature is that the bundling is a weaving process, using yarn of nylon, kapton, nomex, teflon, or others as required. Special features of Fab-Ri-Cable, as it is called, are its light-weight, durability, flexibility, and ribbon thin-ness. It offers wide design and functional possibilities, in that any number of conductors from 4 to 100 may be used, of any tape manufactured today. Single or multiple fold and cut lines are possible. The number of "picks" (cross-weavings) may be varied for tighter bundling or better abrasion resistance. It is possible to route conductors from a single connector to a number of different locations throughout the electronic package. The cable may be tacked, accordion-folded, spiraled, or folded. Zippertubing Company, Los Angeles, Calif.

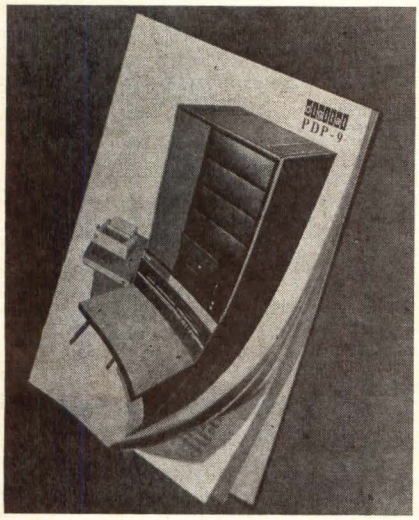
Circle No. 303 on Inquiry Card.

Hardware/Software Evaluator

An evaluation program that enables any 360 user to determine his hardware and software requirements for a communications system before installation encompasses DOS or OS communication's systems run with programs written in BTAM or QTAM macros. According to the manufacturer, the evaluator represents a major breakthrough in eliminating costly design errors in communications systems. The evaluator can pre-determine: 1. The minimum system configuration necessary to handle message loads. 2. The time it takes for messages to pass through the system. 3. The time available for non-communication programs in other partitions. 4. The optimum design for message processing programs. The evaluator can also be used as a design tool for further modification of existing communications systems. It can determine the effect of changes to an existing system before the changes are implemented, and can help 360 users who are planning to install a communications system as well as 360 users who already have a communications system operating but wish to effect certain changes. Perhaps the greatest potential for the program is with second generation users who are planning to go to the 360 and plan to incorporate a communications system. Descriptive literature is available. Worldwide Computer Services, Port Chester, N.Y.

Circle No. 322 on Inquiry Card.

LITERATURE



Computer Brochure

50-page illustrated brochure explains the PDP-9 computer system for complex problems in data acquisition, process or instrument control, computation or man/machine communication. The publication's first three pages cover questions and answers in applying the computer, which is priced at $35,000 for the basic system. Processor and memory specifications, I/O facilities, instructions, software, options and detailed application information also are covered. More than a score of charts, graphs and pictures are included. Digital Equipment Corporation, Maynard, Massachusetts.

Circle No. 316 on Inquiry Card

I/C Capability

Described as being a first-of-its-kind Perpetual Integrated Circuits Condensed Catalog a new 50-page guide has been designed so that pages — or complete sections — can be replaced or added to accommodate updating material as new I/C devices are announced. Included in the catalog are eight different families of digital circuits, and five family groups of linear circuits (operational amplifiers, high-frequency amplifiers, power amplifiers, differential amplifiers, and sense amplifiers). The families are color-coded on multi-colored pastel stock for quick, easy location. Device functions and characteristics, plus logic diagrams are included for each family. The sections are assembled in "loose-leaf" fashion and bound with a metal slide fastener for updating ease. A "Comparison Chart" is included that allows the designer to quickly compare some of the major features of the different I/C logic families, weigh the advantages and limitations of each logic line, and select the most suitable circuit for his particular set of system requirements. An "Application Selector Guide" lists all circuit functions available, indicating which functions are provided by each logic family. In all, specifications are provided for 25 linear types and 376 digital types, each available in one or more package styles: flat pack (2 versions), metal can (6 versions), and the 14-pin dual in-line plastic package — for a total of more than 675 different devices to meet exact design specifications. Motorola Semiconductor Products Inc., Phoenix, Arizona.

Circle No. 317 on Inquiry Card

High-Speed Printer

A printer that operates at speeds of up to 120 characters per second (1,200 words per minute) is described in a new product flyer now available. Detailed is how the machine prints by electrostatic deflection of highly charged ink particles fired at ordinary teletypewriter paper from jets. The jets trace characters in much the same way that a beam of electrons traces patterns on an oscilloscope tube. Up to 64 alphanumerics can be printed at a maximum of 80 a line. Potential data communications applications for the Inktronic include use as a monitor in high-speed tape-to-tape systems, computer interrogation when equipped with a keyboard and for computer print-out. Teletype Corporation, Skokie, Illinois.

Circle No. 315 on Inquiry Card

Power Modules

Catalog sheet 147A, which describes the recently introduced LC series of low-cost wide-range power modules. This new series of compact power supplies provides DC outputs over the range 4-32 vdc with current ratings from 750 milliamperes to 10 amperes. The bulletin offers electrical and physical data, descriptive information, application data and prices. Electronic Research Associates, Inc., Cedar Grove, New Jersey.

Circle No. 314 on Inquiry Card

Mercury-Wetted Contact Relays

Two new engineering manuals on mercury-wetted contact relays for wired assemblies and printed circuit board applications describe relays that incorporate low, constant-contact resistant characteristics, no contact bounce, maximum reliability over 22 x 10^9 operations and switching speeds as fast as 1 ms. New 32-page Manual 801 describes in detail electrical, environmental and physical characteristics of Mercury-wetted contact relays for wired assemblies. Basically, these are the various types of HGS (high-speed relays) and HG high load-carrying capacity relays. These models are available in round cans, with plug-in or solder terminals or AN connectors. The characteristics of Types HGSR, HGM, HGSM and HGPM relays for printed circuit board applications are included in 24-page Manual 802. Completely compatible with other pcb components, these relay modules provide a wide range of electrical characteristics. Circuit board assemblies, combining HG relays with other components on pcb boards, are also included in Manual 802. C. P. Clare & Co., Chicago, Ill.

Circle No. 311 on Inquiry Card

Ceramic Capacitors

General characteristics and complete ordering data by series for a com-

plete line of ceramic capacitors — type 1200 or NPO — are highlighted in a new 16-page brochure. Details provided in the illustrated brochure cover the following series of ceramic capacitors: G5, 50 volts, dipped or molded; B1, 100 volt, dipped or molded; RH, 200 volt, dipped or molded; WM, 100 volt, dipped or molded; CK, 200 volt and 100 VDC, both per MIL-C-11015; and CKR, in 100 VDC and 200 VDC configurations, per MIL-C-39014. Also featured is the SC series, type 1200 or NPO, of ceramic capacitor chips. Information given in the brochure extends comprehensively from sizes and configurations in each series to temperature ranges and coefficients, capacitances, tolerances, types of leads, and electrical parameters. Completing the brochure is a series of charts comparing typical temperature, voltage and frequency characteristics of the type 1200 and NPO ceramic capacitors. San Fernando Electric Manufacturing Co., San Fernando, Calif.

Circle No. 312 on Inquiry Card

High Speed Data Sets

Two 4-page technical bulletins on Modem 4400 data sets are available describing models that transmit digital data at rates of 2400 bps and 4800 bps and are capable of transmitting this high speed data over unconditioned voice frequency channels. The bulletins highlight the advantages of the narrow band approach to transmission, and also include a general technical description of each 4400 data set. Milgo Electronic Corp., Miami, Fla.

Circle No. 310 on Inquiry Card

Capacitors

Sixteen page brochure presents manufacturer's complete line of film and metallized capacitors. Of particular interest is the section devoted to Polycarbonate units. Also featured are high voltage, low current, solid state power supplies, hermetically sealed, for both military and industrial applications. Wesco Electrical Co., Inc., Greenfield, Mass.

Circle No. 309 on Inquiry Card

Miniature Switches

52-page catalog includes the latest prices for momentary contact push button switches, up to 12 position multi-deck rotary switches, test clips, binding posts, plastic cases and header boards, stand-off insulators, and printed circuit test jacks. Detail drawings, product photographs, electrical ratings, and materials give design engineers necessary specifying data. Grayhill, Inc., La Grange, Ill.

Circle No. 305 on Inquiry Card

Memory Systems

A full line catalog and standard price sheet listing over 500 different memory systems for off-the-shelf delivery has just been published. The 22-page 8 x 11 inch book is the first catalog ever published listing off-the-shelf memory systems and prices. It contains specifications on 513 standard systems with word and bit capacities from 128 x 8 to 4096 x 32 and a summary of the complete line of standard coincident-current magnetic-core memory systems, said to be the largest and most diversified line of standard memory systems in the industry. Operational theory, applications and packaging are discussed in detail and illustrated through the use of charts, graphs and block diagrams. Ferroxcube Corp., Englewood, Colo.

Circle No. 306 on Inquiry Card

Data Acquisition System

Major feature of an advanced, fully computer programmable data acquisition system for automatic checkout of missile components, subsystems and systems are described in a new applications bulletin. The illustrated bulletin highlights the computer-compatibility of the system which permits range, throughout rate, channel addressing mode and other functions to be totally controlled under computer program. Applications cited in the brochure include current use of the system at several remote test stations, with a digital computer, as part of a large checkout complex for a major missile manufacturer. Among major system capabilities listed in the bulletin are: up to 256 fully differential analog input channels, open-circuit detection on all channels, and auto ranging of two different ranges ($\pm$5V full scale and $\pm$40V full scale). Redcor Corp., Canoga Park, Calif.

Circle No. 307 on Inquiry Card

Printed Circuit Test Point Connectors

Designated Series 672 and TJ, 8-page catalog covers a variety of configurations and sizes from single contact to 63 contacts, all designed to accept an .080 test probe. Recessed and protected floating pin terminals are mounted at right angle to the test socket and dip solder to a printed circuit board. Various molding materials are available. Complete technical specifications, outline drawings and illustrations are also available. Continental Connector Corp., Woodside, N. Y.

Circle No. 308 on Inquiry Card

I/C Logic Modules

General-purpose digital logic modules that use dual-in-line diode-transistor-logic (DTL) circuits are described in a four-page brochure. Designated J Series, these modules operate at clock rates up to 5 MHz and supplement the high-performance T Series modules, which are the basic building blocks of Sigma computers. The J Series family is a complete set of components needed to build a digital system. The brochure describes J Series features, including use of DTL ICs and low price. The DTL ICs are easy to obtain, easy to replace, and are housed in hermetically sealed, ceramic 14-lead dual-in-line packages. Typical prices are $2.50 per NAND gate and $7.50 per clocked flop-flop. Available modules by model numbers, together with price and number of circuits per module, are listed. J Series accessories, services, and major specifications are also briefly described. Scientific Data Systems, Santa Monica, California.

Circle No. 302 on Inquiry Card

Drum Memory System

Drum memory and drum memory systems are described in a new 3-part modular brochure which contains a 12-page booklet on standard drum memories and an 8-page booklet on standard drum memory systems.

The new product booklets are completely revised versions of earlier editions. DB6711 (12-pg. booklet) covers drum reliability; mechanical, magnetic and electronic design factors; and standard logic modules used. It also provides dimensioned illustrations, specifications and operating parameters of five standard drum models with capacities from 2,624,000 to 64,307,200 bits. SB6711 (8-pg.) discusses standard VRC drum memory systems for use with small computers, such as the PDP-8 and 8/S. The booklet describes three different system configurations and provides basic I/O instructions and programming data. Vermont Research Corporation, North Springfield, Vermont.

Circle No. 319 on Inquiry Card

Zeners, Reference Diodes, Silicon Rectifiers

48-page catalog C-67/68 contains descriptions, ratings and specifications for Zener voltage regulator diodes, voltage reference diode and low-power silicon rectifiers and lists 66 different series of Zener regulator diodes ranging from 150 miliwatts to 50 watts in nine package designs. In addition, there are 11 different series of voltage reference diodes listed with nominal temperature coefficient ratings to five parts per million, as well as 34 different series of low power silicon rectifiers in current ranges from 0.4 amperes to 16 amperes and voltage ratings (maximum peak reverse) ranging from 50 volts to 100 volts. The catalog is completely indexed with numerical cross-reference lists and includes an "easy-to-locate" table of contents to facilitate device location. International Rectifier, El Segundo, California.

Circle No. 320 on Inquiry Card

Switch/Relay Catalog

A 24-page catalog describes high density switches and relays capable of switching from 4 to 144 circuits simultaneously in computers, automatic testers, and process controls. Relays, toggle switches and pushbutton switches are described. A new low profile 4-pole flat pack relay is also illustrated. Typical applications and unique advantages of each type are listed. Environmentally and hermetically sealed versions and latching types are also described and fully specified. Electronic Controls, Inc., Wilton, Connecticut.

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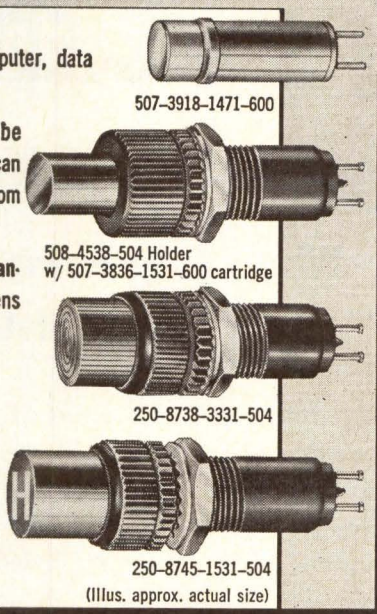

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Micro Switch

Over a dozen switch applications to help solve industrial problems are described in the latest edition of "Uses Unlimited," an 8-page booklet now available featuring uses of CMC (Coordinated Manual Control) in controlling the action of blast furnaces in the steel industry. Another article points out how small precision switches help set bindery records by preventing paper jams... and insuring perfect page alignment. The direct programming of machine settings is shown to be easy with a KB matrix which eliminates numerical control tapes and punch cards. Other features describe various switching mechanisms used to control hydraulic pumps, launch missiles, economize on special communication systems, and gauge, sheer, and stack sheet metal with proximity sensors. Micro Switch, Freeport, Illinois.

Circle No. 300 on Inquiry Card

Desk-Top Computer

An informative 18-page full color brochure provides complete and detailed information on the features and operations of the EAI 580, a desk-top computer providing advanced analog computing capabilities and all the essentials necessary for expansion into a hybrid system. The information is presented both in brief outline form and in detailed descriptions. Pictures of the overall system and its sub-systems are used liberally to provide a comprehensive understanding of the computer. The brochure covers the system's advanced analog and hybrid features, design and operation of the master control panel and analog readout panels, programming, the digital logic system, the individual computing components, system expansion and options, applications and company support. Electronic Associates, Inc., W. Long Branch, N. J.

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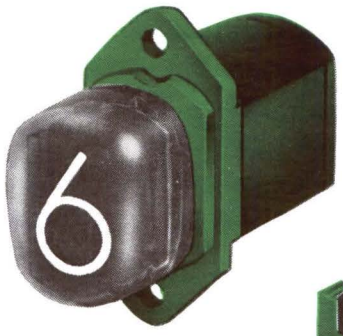

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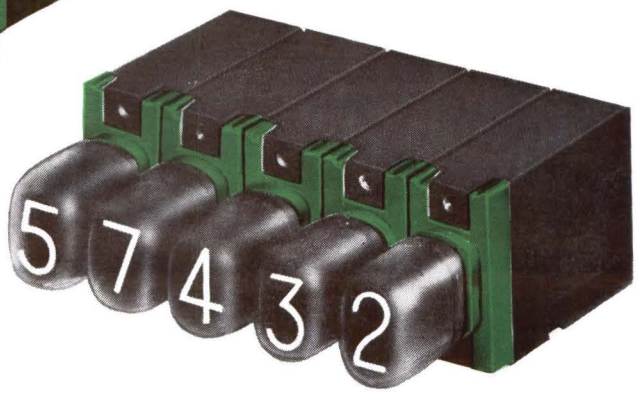

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