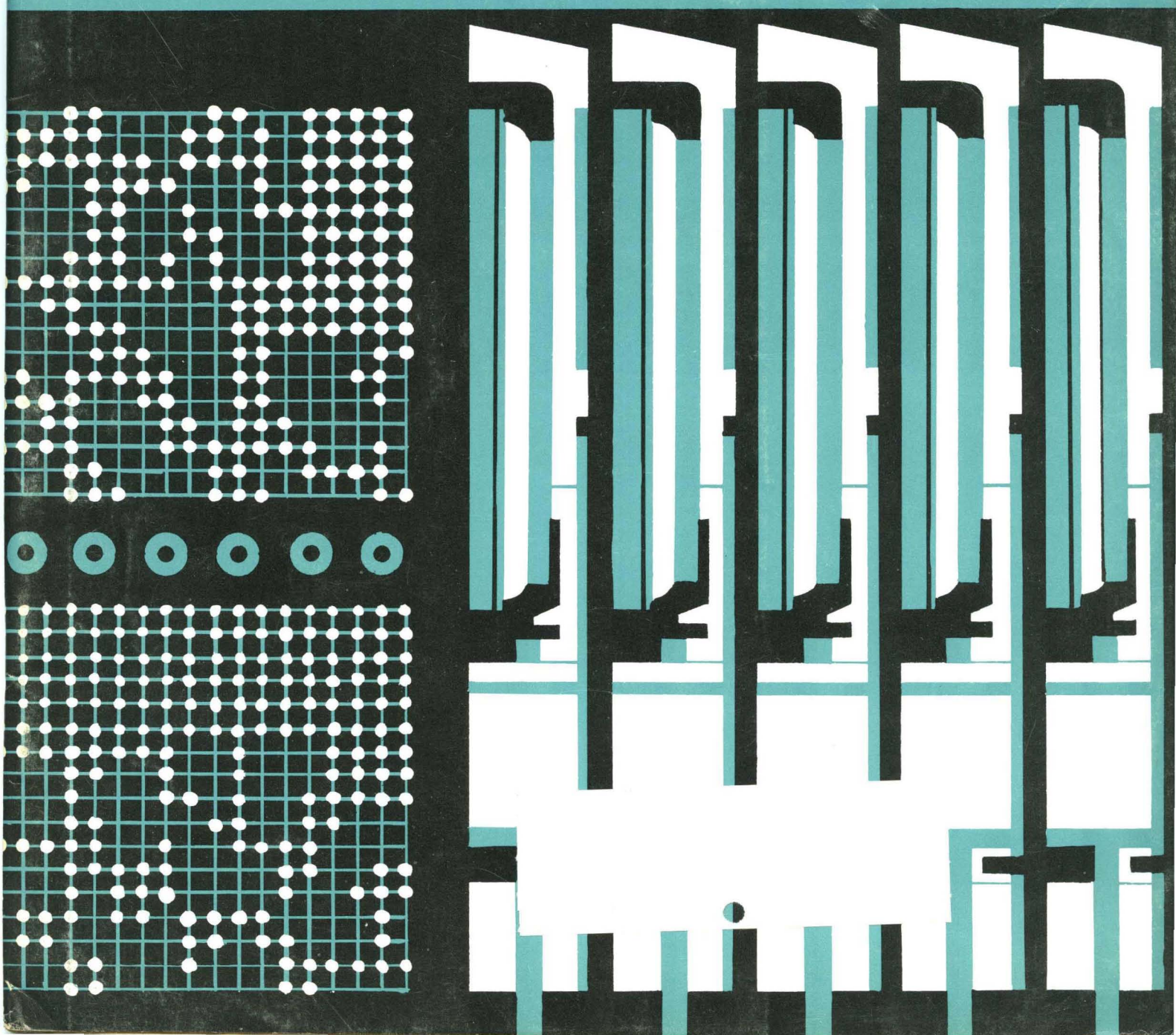
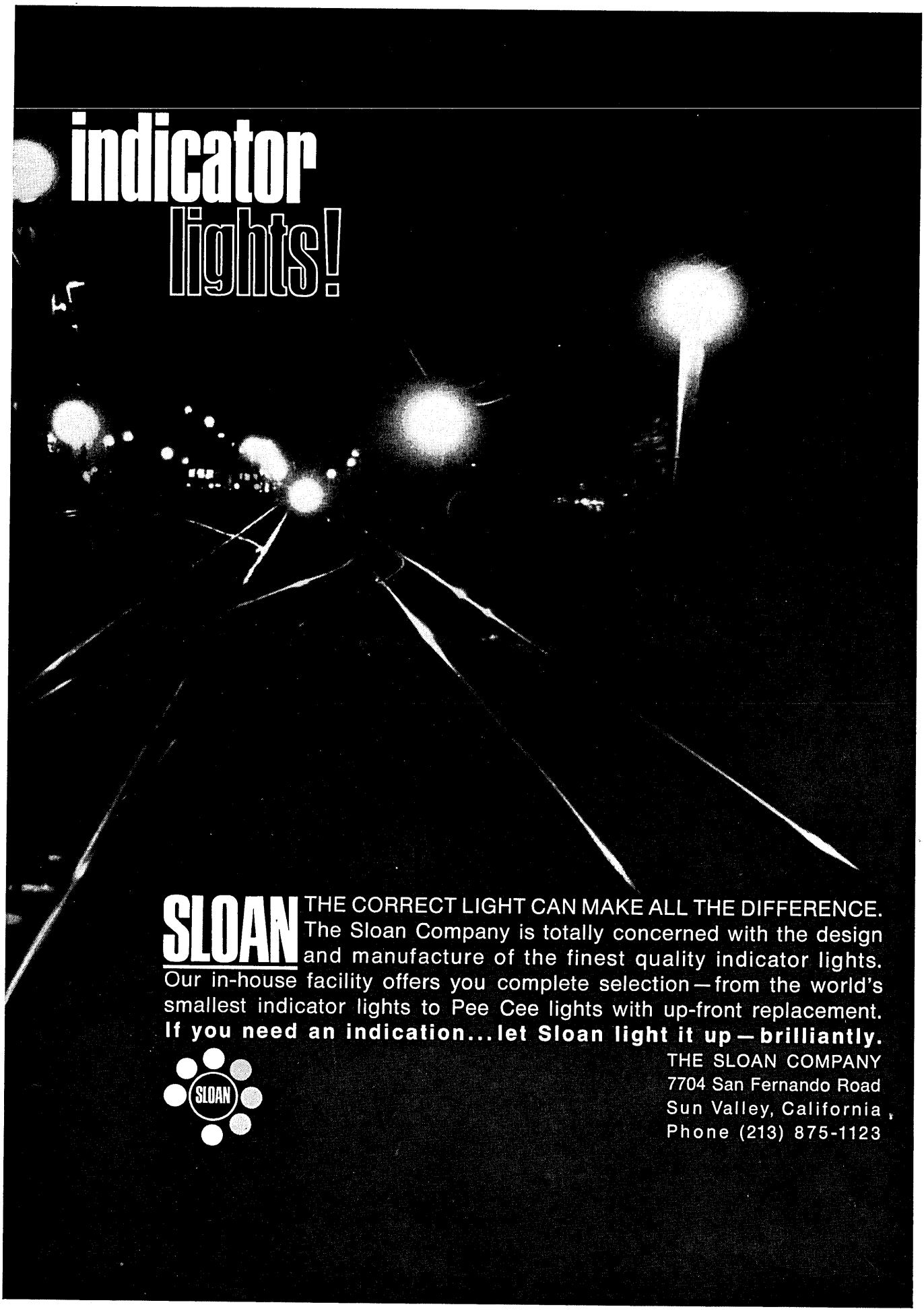
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JULY 1968

HIGH SPEED COMPUTER MECHANIZATION





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CIRCLE NO. 1 ON INQUIRY CARD

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Medium-Power DTL CD2300 Line

at economy prices

45 types / 3 package styles / 2 Temperature Ranges
Gates / Expanders / High Fanout Gates
Clocked Flip-Flops / Hex Inverters
2KΩ and 6KΩ Output Pull-Up Options

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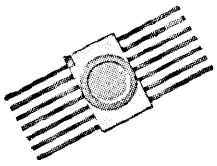
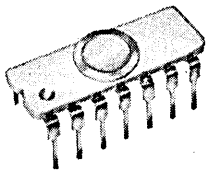
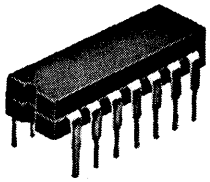
  CD2300 Series—15 circuits in RCA's Unique Ceramic Flat Package.
  CD2300D Series—15 circuits in RCA's Unique Ceramic Dual In-Line Package.
- For Industrial and Commercial Applications:
  CD2300E Series—15 circuits in RCA's Dual In-Line Silicone Package.
- Compatible with RCA CD2200 and 2200D Low-Power DTL Series.

exact replacements for 830 and 930 series DTL







	–55°C to +125°C Operation				0°C to +75°C Operation	
Circuit and Pull-up Option	**14-Lead Ceramic Flat Pack**	**Price (1000 Units)**	**14-Lead Ceramic Dual In-Line Package**	**Price (1000 Units)**	**14-Lead Dual In-Line Silicone Package**	**Price (1000 Units)**
NAND Gates						
Dual-4 Expandable (6KΩ)	CD2300/930	$2.50	CD2300D/930	$2.50	CD2300E/830	$1.05
Dual-4 Expandable (2KΩ)	CD2301/961	$2.50	CD2301D/961	$2.50	CD2301E/861	$1.05
Dual-4 High Fanout, Expandable (transistor output pull-up)	CD2306/932	$2.75	CD2306D/932	$2.75	CD2306E/832	$1.15
Dual-4 High Fanout Expandable (no output pull-up)	CD2307/944	$2.75	CD2307D/944	$2.75	CD2307E/844	$1.15
Triple-3 Input (6KΩ)	CD2308/962	$2.75	CD2308D/962	$2.75	CD2308E/862	$1.15
Triple-3 Input (2KΩ)	CD2309/963	$2.75	CD2309D/963	$2.75	CD2309E/863	$1.15
Quadruple-2 Input (6KΩ)	CD2302/946	$2.75	CD2302D/946	$2.75	CD2302E/846	$1.15
Quadruple-2 Input (2KΩ)	CD2303/949	$2.75	CD2303D/949	$2.75	CD2303E/849	$1.15
Hex Inverters						
Diode Input (6KΩ)	CD2310/936	$2.90	CD2310D/936	$2.90	CD2310E/836	$1.45
Diode Input (2KΩ)	CD2311/937	$2.90	CD2311D/937	$2.90	CD2311E/837	$1.45
Expandable Input (6KΩ)	CD2312	$2.90	CD2312D	$2.90	CD2312E	$1.45
Expandable Input (2KΩ)	CD2313	$2.90	CD2313D	$2.90	CD2313E	$1.45
Flip-Flops						
Clocked RS with JK Capability (6KΩ)	CD2304/945	$3.00	CD2304D/945	$3.00	CD2304E/845	$1.90
Clocked RS with JK Capability (2KΩ)	CD2305/948	$3.00	CD2305D/948	$3.00	CD2305E/848	$1.90
Input Expander						
Dual 4-Diode	CD2314/933	$2.25	CD2314D/933	$2.25	CD2314E/833	$ .90

Ask your RCA Representative for details. See your RCA Distributor for his price and delivery. For technical information, write Commercial Engineering, Section ICZB-7, RCA Electronic Components, Harrison, N.J. 07029.

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The Varian Data 620/i is designed strictly for systems work, fully IC'd for reliability and small size. It is fast (1.8 μsec cycle time, with hardware registers and our unique Micro-Exec addressing), capable (16- and 18-bit words, 4K to 32K word memory, 100-plus basic commands), versatile (Party Line I/O, proven software, complete peripherals and options), and low price ($13,900, in standard configuration, with teletypewriter).

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←CIRCLE NO. 2 ON INQUIRY CARD

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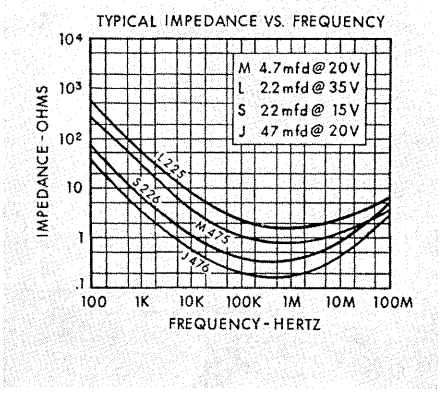
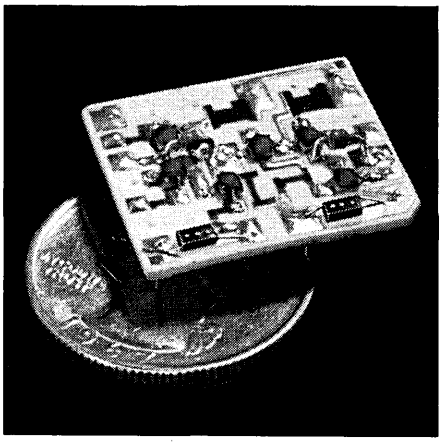
Bypass your problems

or...how Components, Inc. can help clean up digital pulses in a small way

The problem of unpremeditated switching noise is apt to crop up in even the best of IC and hybrid logic arrays, once they are plugged into the system. When it does, the designer has the option of redesigning the circuitry or simply filtering out the spurious noise at appropriate stages. The second approach, although less heroic, is often more practicable if filter components can be found which are sufficiently economical of both space and cost.





C.I.'s Minitan® Series, world's smallest electrolytic capacitors, are a natural solution here, just as they are wherever size and performance are critical.

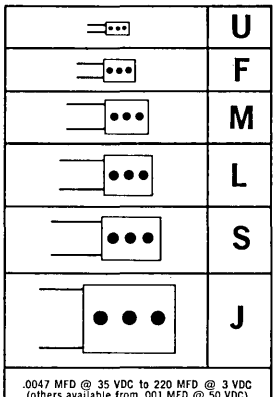
These micro-miniature, solid-tantalum electrolytics provide ideal physical and electrical properties for computer bypass and filtering applications. They are compatible with thick-film and integrated circuitry in both size and reliability, and present extremely low impedance and excellent temperature stability. Rated for use from —55°C to 125°C, they are available in values from .001 to 220 mfd., with axial or radial leads.

Need a Two-Way Street? . . .

C.I.'s Non-Polar Minitan capacitors are available for use where ac or occasional voltage reversals are present. Unlike other non-polar solid-tantalums, these little capacitors were designed as non-polars from the ground up. Result: 1) they are available in standard, rather than off-beat capacitance ratings; 2) they are ½ to ¼ the size of other units; 3) they are extremely reliable, even with frequent voltage reversals.

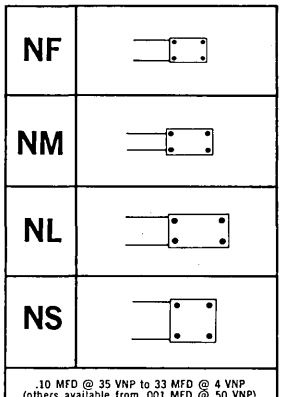
When the squeeze is on . . . call Components, Inc. If you have a space problem, C.I. has the capacity to solve it. We offer more subminiature case styles and ratings than anyone else in the business. We welcome requests for samples, performance and reliability data, and application assistance. Standard prototypes normally shipped within 24 hours. Write or call today for data or samples.

MINITAN MODULAR
(Also available with axial leads)



.0047 MFD @ 35 VDC to 220 MFD @ 3 VDC
(others available from .001 MFD @ 50 VDC)

MINITAN NON-POLAR
(Also available with axial leads)



.10 MFD @ 35 VNP to 33 MFD @ 4 VNP
(others available from .001 MFD @ 50 VNP)

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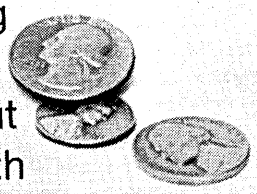
CIRCLE NO. 3 ON INQUIRY CARD

Is it possible to get a really good computer for less than $10K? How about $9,950 and some odd change?

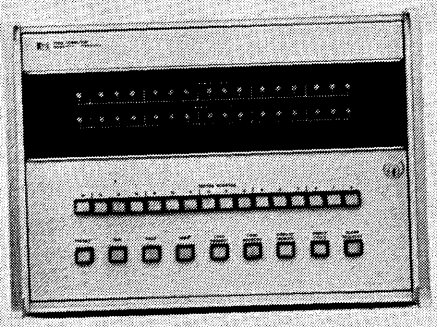
That's what the new Hewlett-Packard 2114A will be pegged at. But it'll heave to just like its big brothers. Throwing around big 16-bit words. Storing 4000 (or 8000) of them at a time in memory. Fetching them out of memory in two microseconds. It'll tie in I/O devices with standard plug-ins and use the same set of programming languages—FORTRAN, ALGOL and Conversational BASIC. It may be the littlest computer in the HP family... but even at that it more than holds its own against its big brothers.



That's right. The HP 2114A offers the most desirable price/performance ratio of any computer on the market. And it won't take up much room, either, not even on your desk. One compact package 12¼" tall houses both processor and power supply.

Yet the economy model is fully compatible with all the 2115/2116 software and I/O interfaces. The main frame accepts either 4K or 8K memory, has eight I/O plug-in slots and operates within a wide temperature range. Low-cost options include parity error check and power-fail protection.

If you think this powerful little computer is right for you, get more information from your local HP field engineer. Or write Hewlett-Packard, Palo Alto, Calif. 94304; Europe: 54 Route des Acacias, Geneva.



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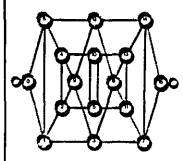
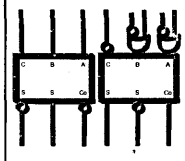
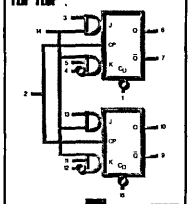
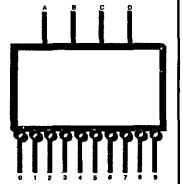
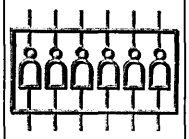
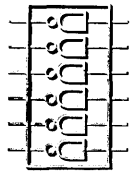
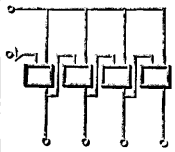
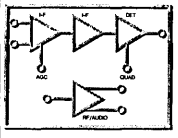
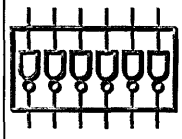
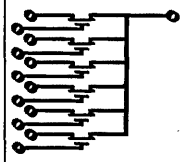
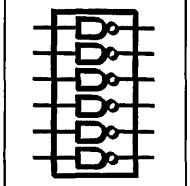
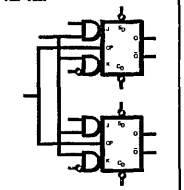
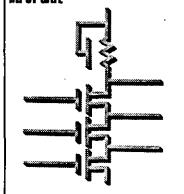
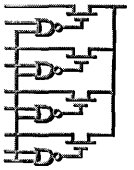
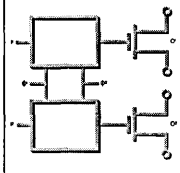
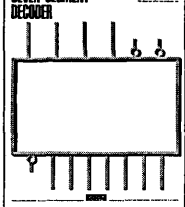
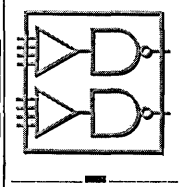
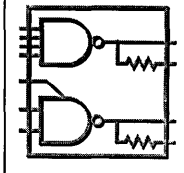
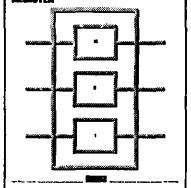
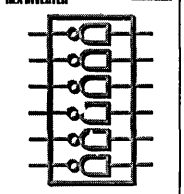
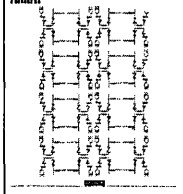
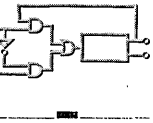
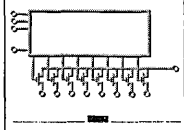
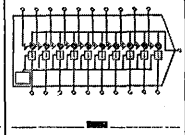
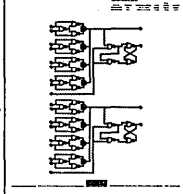
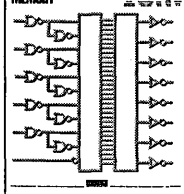
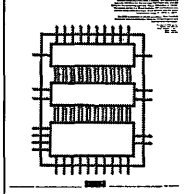
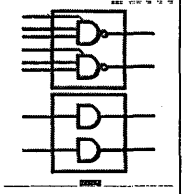
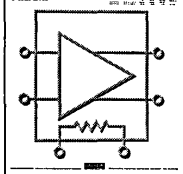
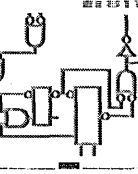
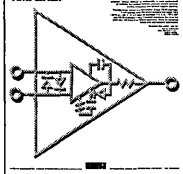
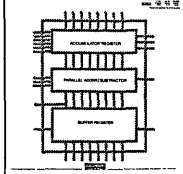
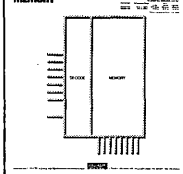
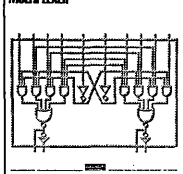
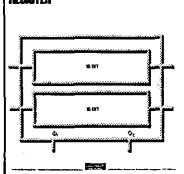
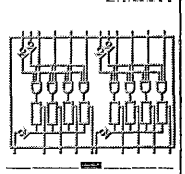
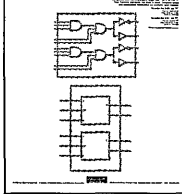
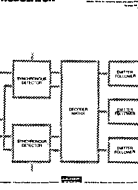
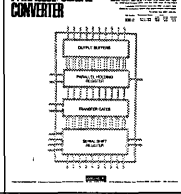
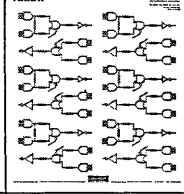
DIGITAL COMPUTERS

06810

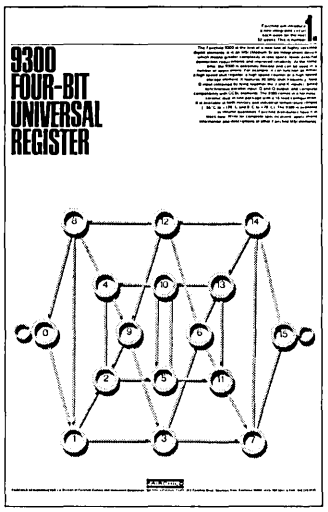
CIRCLE NO. 4 ON INQUIRY CARD

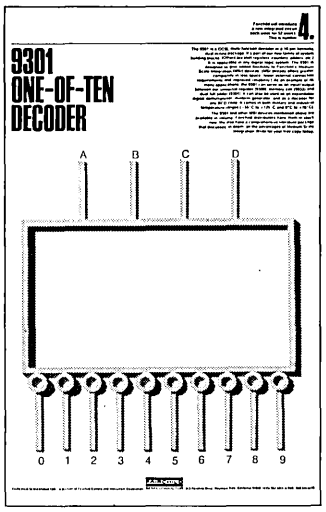
Fairchild has introduced 40 new products in the last 40 weeks.

Our goal is fifty-two new integrated circuits in fifty-two weeks. To obtain the Reader Service number for any product announcement ad, simply add 100 to the new product number. For example, New Product No. 3 is Reader Service No. 103.

1. 9300 FOUR-BIT UNIVERSAL REGISTER 	2. 9304 DUAL FULL ADDER 	3. 9029 DUAL J-K FLIP-FLOP 	4. 9301 ONE-OF-TEN DECODER 				
5. 9109 HIGH LEVEL HEX CONVERTER 	6. 9112 HIGH LEVEL HEX CONVERTER 	7. 9099 FOUR-BIT BINARY COUNTER 	8. μA719 VHF FREQUENCY COMMUNICATIONS SYSTEM 	9. 9935 EXPANDABLE HEX INVERTER 	10. 3701 SIX-CHANNEL MULTIPLEX SWITCH 	11. 9016 TTL HEX INVERTER 	12. 9022 DUAL J-K FLIP-FLOP 
13. 3102 MOS THREE-INPUT GATE 	14. 3700 FOUR-CHANNEL MULTIPLEX SWITCH 	15. 3303 DUAL 25-BIT DYNAMIC SHIFT REGISTER 	16. 9307 BCD TO SEVEN-SEGMENT DECODER 	17. 9620 DUAL DIFFERENTIAL LINE RECEIVER 	18. 9621 DUAL LINE DRIVER 	19. 3300 25-BIT MOS STATIC SHIFT REGISTER 	20. 9310 HIGH LEVEL LOGIC HEX INVERTER 
21. 4500 BIPOLAR MICROMATRIX™ ARRAY 	22. 3320 MOS 64-BIT, 4-PHASE SHIFT REGISTER 	23. 3705 8-CHANNEL MOS MULTIPLEX SWITCH 	24. μA722 PROGRAMMABLE D/A—A/D CONVERTER CURRENT SOURCE 	25. 4510 DUAL FOUR-BIT COMPARATOR 	26. 9034 256-BIT READ-ONLY MEMORY 	27. 3758 10-BIT MOS-LSI D/A CONVERTER 	28. 9624/9625 INTERFACE CIRCUITS 
29. μA727 TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMP 	30. 9601 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR 	31. μA741 FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER 	32. 3800 EIGHT-BIT MOS/LSI PARALLEL ACCUMULATOR 	33. 3501 1024-BIT MOS/LSI STATIC READ-ONLY MEMORY 	34. 9309 DUAL FOUR-INPUT DIGITAL MULTIPLEXER 	35. 3304 MOS/LSI DUAL 16-BIT STATIC SHIFT REGISTER 	36. 9308 DUAL FOUR-BIT LATCH 
37. 3100/3101 MOS FUNDAMENTAL ELEMENTS 	38. μA737 COLOR TV CHROMA DEMODULATOR 	39. 3301 MOS 10-BIT SERIAL/PARALLEL PARALLEL/SERIAL CONVERTER 	40. 4600 TTμL MICROMATRIX™ ARRAY 	July 15, 1968	July 22, 1968	July 29, 1968	August 5, 1968
August 12, 1968	August 19, 1968	August 26, 1968	September 2, 1968	September 9, 1968	September 16, 1968	September 23, 1968	September 30, 1968

More about:

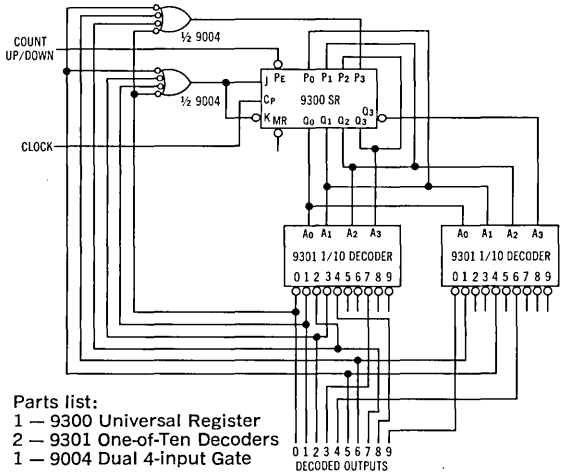




Up/down decoded decade counter.

Combine New Products #1 and 4, and you have the basis of an up/down counter with decoded outputs for process control. If only the decoded outputs are used, you don't need a weighted up/down counter. A shift counter will do the job.

The 9300 universal register can be used to form a decade shift counter counting through a sequence of 10 stable states. A logic "1" or "0" is injected into the first stage of the register at each clock pulse and the previous contents shift one place. After 10 clock pulses, the shift counter has passed through all 10 stable states in a loop. On the next clock pulse, it arrives back at the starting state. A shift register can be made to count in this sequence by decoding the states through which it passes and by using the decoder outputs as a minterm generator to effectively force a logic "1" at the input of the shift register when the state sequence demands. The following block diagram shows a circuit of this type which requires only four devices.



Parts list:
1 — 9300 Universal Register
2 — 9301 One-of-Ten Decoders
1 — 9004 Dual 4-input Gate

Consider the up count sequence below with the desired input for the next state included:

In states 0000, 1000, 1100 and 0011 a logic "1" must be forced into the first stage of the shift register on the next clock pulse. This may be accomplished by using two 9301 one-of-ten decoders to decode all the sixteen possible minterms from four variables, then sum the appropriate minterms by a 4-input active low input OR gate and let the OR gate drive the JK inputs connected together on the 9300 shift register. Each 9301 decoder acts as a 1/8 decoder with the most significant A_3 input acting as an enable input. The first three outputs of the shift register go to the first three inputs of the decoders and the first decoder has Q_3 from the shift register as the A_3 input and the other decoder the Q_3 thereby producing a one-of-sixteen decoder. The outputs of the two decoders are so arranged as to give the decoded outputs in sequence which can then be used to select or drive external circuitry.

COUNT SEQUENCE									
UP					DOWN				
Q_0	Q_1	Q_2	Q_3	INPUT	Q_0	Q_1	Q_2	Q_3	INPUT
0	0	0	0	1	0	0	0	1	0
1	0	0	0	1	0	0	1	0	0
1	1	0	0	1	0	1	0	0	1
1	1	1	0	0	1	0	0	1	1
0	1	1	1	0	0	0	1	1	1
0	0	1	1	1	0	1	1	1	0
1	0	0	1	0	1	1	1	0	0
0	1	0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0	0	0
0	0	0	1	0	0	0	0	0	1

The synchronous parallel enable facility can be employed to make the shift register effectively shift to the left rather than the right by connecting the three most significant shift register outputs to the corresponding lower stage parallel inputs and operating the 9300 in the parallel enable mode. The same shift count sequence can now be used. Appropriate minterms are summed by an additional active low input OR gate which drives the shift left counter, making it pass through the same 10 stable states as before, but in the opposite direction. By this means, the shift counter performs as an up/down decoded decade counter with the parallel enable/shift input as a count up/count down control. Since only the desired minterms are summed and logic "0s" are inserted into the first stage of the register rather than at specific states, no lock-up sequence can occur.

To obtain specifications and other applications information, simply circle Reader Service numbers 101 and 104. If you have an immediate requirement, call your local Fairchild distributor now.

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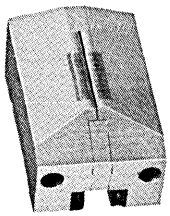
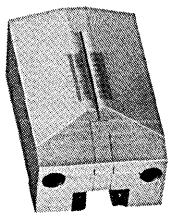
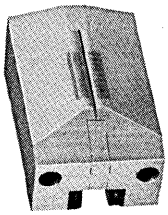


CEC digital recording heads don't exactly live up to their guarantee.



It's a matter of recorded history that they live far beyond it. Case on record: the *first* magnetic tape head replaced in a certain military data-processing installation in Germany logged more than 10,000 hours—or *five times the guaranteed life.*

An atypical performance perhaps? Yes. It was *subpar.* Unit records show an *average* utilization in excess of 12,000 tape passing hours. And a peak head life of 16,000 hours. The system operates around the clock at 120 ips.



CEC has conquered the tape head aging process through use of advanced materials developed by Bell & Howell's Research Center. The upshot has been outstanding magnetic properties, an extremely low wear rate...and Methuselahian life-span.

You're assured that, whatever make or model recorder you're using, we've got the head for it. Regardless of interface parameters. And, although we're alone in guaranteeing our heads for 2000 hours, you're assured we try never to live down to it.

That's why we're known as the old heads in the business. For all the facts on the complete line, call your nearest CEC Field Office. Or write Consolidated Electrodynamics, Pasadena, California 91109. A subsidiary of Bell & Howell. Bulletin Kit 1711-X2.

CEC/DATA INSTRUMENTS DIVISION

BELL & HOWELL

CIRCLE NO. 5 ON INQUIRY CARD

Now—save vital space with 30-gauge hook-up wire

General Electric saved space and weight in wiring the back panels of its GE-PAC® Process Computers by using 30-gauge hook-up wire insulated with Kynar.

. . . Made with tough, durable Kynar®

Thirty gauge wire is nothing new . . . but what is new is wire insulated with Kynar, the fluoroplastic that's tough. It has twice the cut-through resistance of other fluoroplastics, cuts and strips smoothly, takes 180° bends without splitting, stands up to the punishment of automatic wiring machines or semi-automatic hand tools.

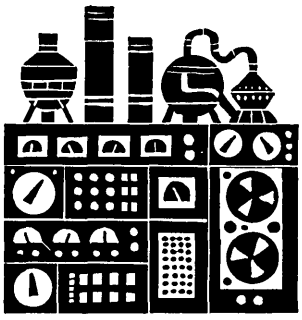
What's more, Kynar resists cleaning solvents, won't degrade with age, and operates at temperatures from −80° to 300°F.

For samples of 30-gauge wire insulated with Kynar plus information on how you can save space, reduce weight, write Plastics Department, Pennsalt Chemicals Corporation, 3 Penn Center, Philadelphia, Pa. 19102.

Kynar...the fluoroplastic that's tough!

PENNSALT®

CIRCLE NO. 6 ON INQUIRY CARD



INDUSTRY NEWS

NEW COMPUTER CONTROL CONCEPT—How can several computers linked together adapt automatically to an unexpected situation — such as a sudden fault — and continue to operate despite the fault?

A patent (No. 3,386,082) for a way to answer that question was awarded today to IBM engineers T. S. Stafford, D. C. Burnstine, J. R. Rogaski, and G. T. Paul of the company's Systems Development Laboratory, for their invention entitled Configuration Control in Multiprocessors.

The ordinary computer control consists of many separate units that are interconnected to form a system, in much the same way that a house consists of separate units, or rooms, each room having its own wiring circuit, with all circuits linked together at a central fuse box. If a fault occurs, the central box suspends normal operation until the faulty unit is located and repaired.

With the new computer control there is no "central fuse box." Instead, each unit of the system contains a set of switches that connect that unit with every other unit in the system. Special instructions or "commands" built into the computer keep watch over all the switches. This means that if a fault occurs in any unit, the computer releases its stored commands which take the faulty unit out of action and replace it with a standby unit. The change-over takes place automatically.

The invention is said to have dramatic significance in situations where system reliability is of paramount importance, as in computer monitoring of hospital patients, or surveillance of aircraft in flight.

IFIP COUNCIL MEETING — The council of IFIP held their spring meeting in Tbilissi, the state capital of Georgia, U.S.S.R. This, their first visit to the Soviet Union, was made at the invitation of Professor A. A. Dorodnicyn, the president-elect of IFIP.

A prominent item on the agenda was the report on preparations for IFIP Congress 68. F. Genuys, chairman of the programme committee, reported on the final selection of some 220 papers out of the 600 submitted.

A progress report prepared by B. B. Swann, chairman of the Congress Committee, on the administrative arrangements for the congress and exhibition was also given.

Dr. H. Zemanek, chairman of technical committee TC-2, programming languages, reported that the draft of ALGOL 68 had been published, and it was hoped to have the final version ready by late July. Professor A. van Wijngaarden would present a paper on ALGOL 68 at the Congress.

The council reviewed the program of activities of the Administrative Data Processing Group (IAG), and approved the proposals to publish a quarterly journal and the documentation of the six-month seminar held in London last year.

Council also approved plans to investigate the possibility of establishing an international abstracts service, and expressed their thanks to the representatives of the Netherlands, Soviet Union and United States for their offers of services, staff and finance.

The next meeting of the council will take place in Edinburgh, Scotland, on 31st July and 1st August prior to the opening of IFIP Congress 68.

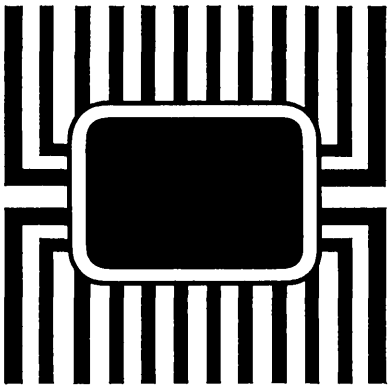
THICK-FILM RESEARCH — A broad-scope research program directed toward improved fabrication and performance of thick-film microcircuits has been recommended by Battelle Memorial Institute's Columbus Laboratories to manufacturers and users of thick-film electronic components.

The proposed program, which would require the joint support of a number of companies, was described recently at a meeting at Battelle-Columbus. In attendance were 75 representatives of supplier, manufacturer, and user companies.

Through research, Battelle proposes to establish the inherent capabilities of selected thick-film components, investigate degradation and failure mechanisms, and study new materials and processing procedures. This laboratory research would be coupled with the preparation of a definitive bibliography of literature in this area. The research program is designed to produce practical results in the design and use of thick-film circuits through a better understanding of the limits of their capabilities, and in the formulation of pastes and the fabrication of circuits.

In briefing company representatives on the purpose of the proposed research, Battelle specialists pointed out the evolutionary state of thick-film technology and the need for exploring the capabilities and limitations of passive components comprising the latest material formulations.

"Compared with knowledge of other devices, little is known about operating limits and reliability of printed components and the factors that influence them," according to H. Clay Gorton, associate chief of electronic materials and devices at Battelle-Columbus. "Factors that should be investigated include processing variables, materials interactions, and operating conditions. Substrates and their influence on the quality, stability, and operating life of the components have received little attention. In addition, the interface between components and conducting interconnections is a subject requiring investigation. The proposed research program will consider these and related problems."



1024-bit Read-Only Memory. Costs less than 5¢ per bit!

Join system designers investigating the new Philco 1024-bit fixed-storage MOS memory arrays for next-generation computers.

At new economical prices, you can make use of pre-wired subroutines such as lookup tables, log or sine-cosine generators.

A couple of big advantages. You can easily change the function without changing the program, and you can add functions to an existing system. Integral output buffers drive T^2L devices directly. You can expand to any desired memory size.

Delivery? Three weeks if your bit pattern is typical. We use computerized software to transfer your bit pattern to the pM1024 with complete accuracy. Immediately available from our distributors is the pM1024 sine lookup table from 0° to 90°. For complete details and specs, contact Philco-Ford Corporation, Microelectronics Division, Santa Clara, California 95051. 408-245-2966.

Model	Temp. Rating	Read Time	Price (100-999)
pM1024C	0 to 70°C	2 microsec.	$45
pM1024AC	0 to 70°C	1 microsec.	$60
pM1024	−55° to +125°C	2 microsec.	$70
pM1024A	−55° to +125°C	1 microsec.	$90

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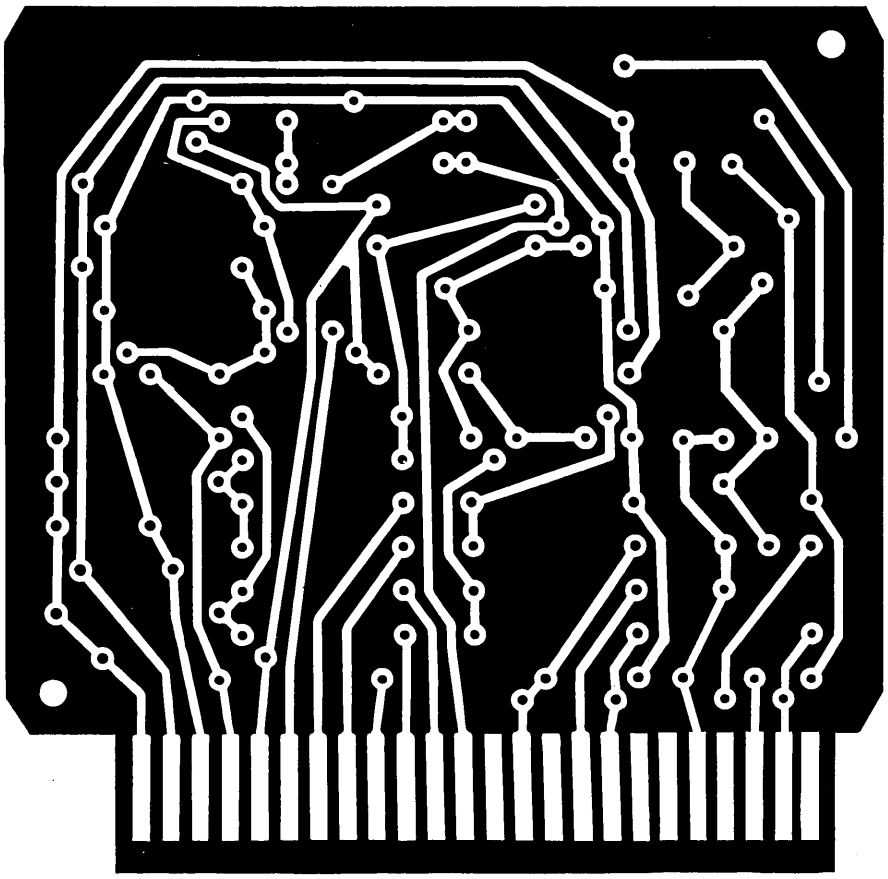
CIRCLE NO. 7 ON INQUIRY CARD

The Clearest Logic:



Logic modules are built on printed circuit cards. Hole location and front-to-back registration must be very accurate for machine assembly. **Hand assembly is costly.** Plated thru-holes must provide positive continuity. **Rejects are costly.** Circuit boards for logic modules must be easily solderable. **Poor solderability is costly.** Printed circuit cards must be delivered in volume quantity for large-scale logic module production. **Time delays are costly.**

These are the reasons that Cinch-Graphik boards are built with such exacting precision. **Anything less is too costly.**

CINCH-GRAPHIK

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AIR DEFENSE CONTROL TRAINER — A digital training device which simulates air attacks to train air defense control personnel has been delivered to the U. S. Marine Corps by Sylvania Electric Products Inc.

The unit will prepare Marine air defense controllers and operators to track enemy airborne targets, direct interceptor aircraft, and designate hostile targets for surface-to-air missiles (SAMs). The trainer, which includes an instructor's console, 12 auxiliary consoles, a missile battery console, and associated electronics, was designed, produced, and installed under a $1.3 million contract from the Naval Training Device Center, Orlando, Fla.

At the instructor's command, the trainer simulates air attacks, duplicating the movements of targets in actual battle conditions. Students at the TAOC consoles answer the "attacks" by controlling the launching of either interceptor aircraft or SAMs.

A training exercise, once started, can be modified by the instructor or interrupted to provide corrective instruction to the students. The performance of the trainees can be monitored on the instructor's console.

PATENT FOR SOFTWARE SYSTEM — A patent for a sorting system has been granted by the United States Patent Office to Applied Data Research, Inc. The significance of this event is that it is the first patent the Patent Office has granted for a computer system embodied in a computer program or software.

For many years patents have been granted for hardware forms of computer systems. However, legislation, which had been introduced in Congress to prevent the patenting of computer programs, had led to doubts that patent protection would be available for the software forms of such computer systems. Recently this legislation was withdrawn.

The patented system, initially developed in 1964, was described by Martin A. Geotz, of ADR, in a paper delivered to the Spring Joint Computer Conference that year. The sorting system uses a read-forward oscillating merge principle for the sorting of information on a computer and could be used with various computers.

DATA BLOCK BUSTER

Got a data block?

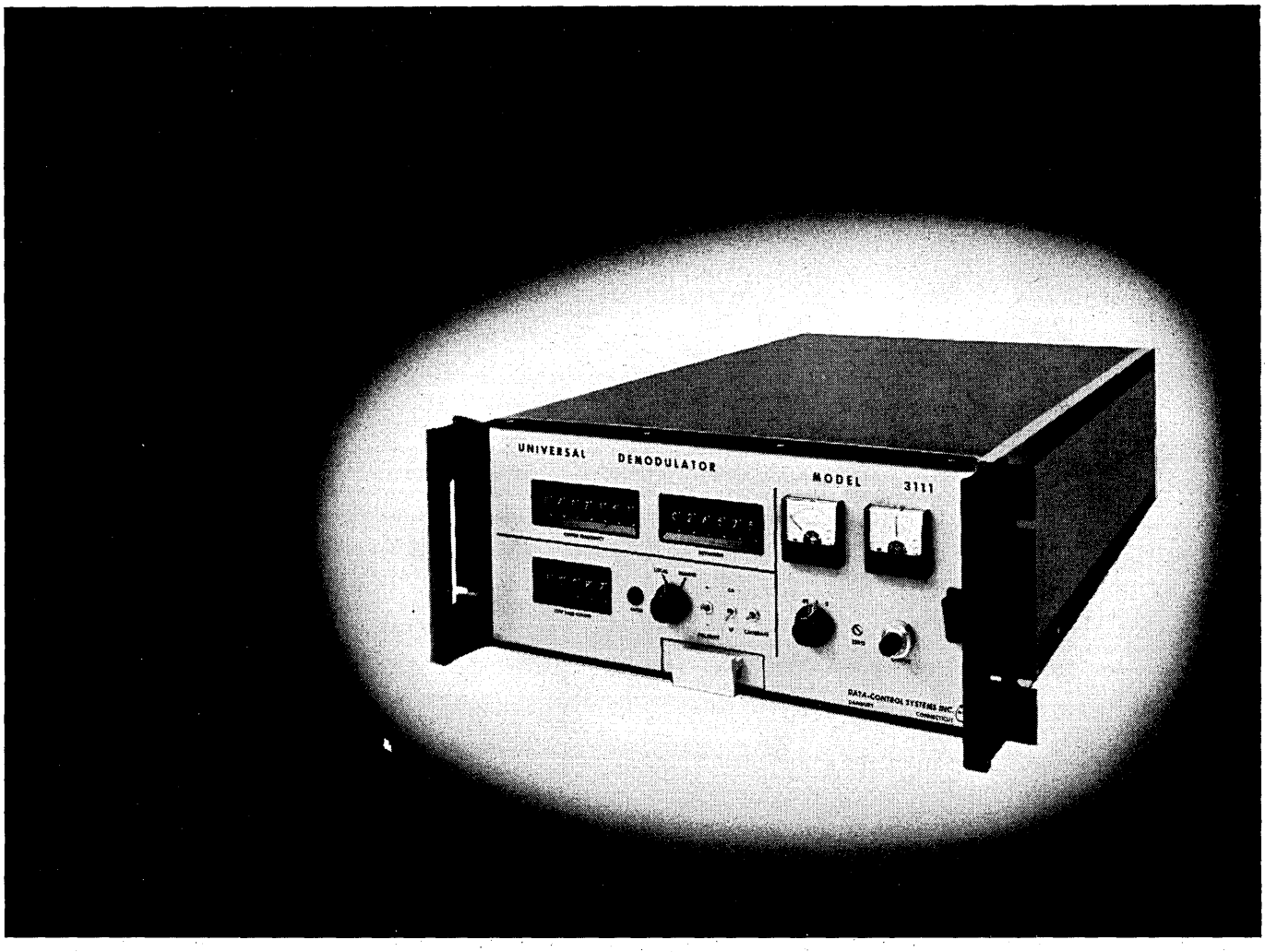
Maybe your computer doesn't handle incoming data efficiently. Maybe you're tired of buying and storing demodulator plug-ins — or using tunable demodulators that can't handle the range of bandwidths you need.

Here's the way to really bust your data block: the new DCS Series 3000 Universal Demodulator, a single unit that can process any subcarrier multiplex between 400 Hz and 1.5 MHz at any tape speed. Accuracy equivalent to the finest fixed-tuned demodulator. Reaction time in milliseconds. Manual or computer programmable. No need to recalibrate when changing set-up.

Sound fantastic? Just drop us a line and let us know about your data problem. We've got a man in your area who'll be glad to come around and bust your block for you.

Any time you say.

DCS **DATA-CONTROL SYSTEMS INC.**
Instrumentation for Research
East Liberty Street, Danbury, Conn. 06810



CIRCLE NO. 8 ON INQUIRY CARD

Beta • graphics™

HARD-COPY CRT PRINTER

MODEL HC610

PRODUCES 8½ X 11″ PRINTS OF COMPUTER-GENERATED GRAPHICS AND ALPHANUMERICS IN SECONDS . . . COMPLETELY DRY (NO LIQUIDS USED).

Model HC610 is designed to be interfaced to a computer, coupled to a display controller or slaved to any graphical computer display.

The Betagraphics Printer is a random-access X-Y device, featuring high-speed magnetic deflection, geometry correction and dynamic focus. Full format settling time is less than 12 microseconds, point-plotting rate is 500,000 points per second, line-writing rate is 2 microseconds per inch and character-writing bandwidth is greater than 1 megahertz.

Operation is simple, with only three controls in addition to the power switch — an exposure TIMER, an EXPOSE-DEVELOP switch for single exposure, development and delivery, and an EXPOSE switch for the multiple overlay or slow-buildup mode. All command and status interface signals are available for remote operation.

The Betagraphics line of peripheral display devices is here, now, to give you high quality computer graphics at reasonable prices. We'll be happy to send you complete specifications.

Beta Instrument Corp.

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TIME-SHARING SOFTWARE FOR SYSTEM 360/MODEL 50 — A time-sharing system that combines an easy-to-use computer language and telephone access to a System/360 Model 50 has been announced by IBM.

The new system, Call/360 Basic, allows subscribers to communicate with the computer using a version of the "Basic" language. Originally developed at Dartmouth College, Basic consists of ordinary English and simple algebraic expressions.

"With about two hours of training almost anyone can take advantage of the wide-ranging capabilities of the system," said L. E. Donegan, Jr., director of IBM's Information Marketing Department.

"Fast response time, security controls, a large storage capacity and a ready-made library of IBM application programs are some of the system's features," Mr. Donegan said.

The version of the Basic language used with Call/360 includes new computer commands that are said to make it easier to store and handle data, format printed output and extend the precision of mathematical computations.

Since April, organizations in New York, San Francisco and Chicago have been using Call/360 Basic in an operational test, communicating with a remotely-located computer in San Francisco. Additional computer centers are scheduled to be opened in New York and Chicago this summer, with service extended to 34 major cities by year-end. Subscribers need only dial a local IBM telephone number to gain access to the computer from their terminals.

Subscribers have the option of using IBM 2741 communications terminals — with a keyboard designed especially for remote computing — or Teletype terminals Models 33 and 35.

A minimum monthly usage charge of $100 for Call/360 Basic covers various combinations of system use time, storage utilization and establishment of the user's own program library, as well as access to the IBM applications program library. Terminal and local telephone line costs are additional. Monthly rental for an IBM 2741 is $103.50.

DUAL-ACCESS ROLE BY COMPUTER SUCCESSFUL — Hughes Aircraft Company has announced that its H-3118M general purpose computer has successfully operated for the first time in a fully-extended 131,000-word-memory configuration in a multi-processing mode.

Two arithmetic and control processors operate with a "floating executive" accessing the memory simultaneously.

The machine is said to be capable of 450,000 instructions a second, performing in the dual-processing mode with eight high-speed input-output channels.

The computer is contained in five cabinets, which include the two processing units, each in its own cabinet with more than 16,000 words of memory; and three additional cabinets, each of which contains about 32,00 words of memory.

Variations of the computer are available in single or dual processor capabilities. Either can contain up to 131,000 words of central memory.

Hughes is currently under contract to provide variations of the computer for a number of major systems, the largest of which is the $300-million NATO Air Defense Ground Environment (NADGE) program for Europe.

← CIRCLE NO. 11 ON INQUIRY CARD

IC BREADBOARD — Canadian Westinghouse of Hamilton, Ontario, Canada, has recently announced the Insta-Board, a macroscopic breadboard for use in the design, development and study of integrated circuits.

The device can be used repeatedly in circuit design applications and is actually an enlarged version of the Westinghouse Insta-Circuit — a microscopic, monolithic integrated circuit breadboard.

Insta-Board features a printed circuit layout, approximately 7" by 10", containing a component ohmic contact pattern in a one-to-one correspondence with the component contact pattern on the actual monolithic breadboard. Another printed circuit layout behind the patterned board contains an array of 12 Insta-Circuits in 12-pin packages.

Internal connections between the two layouts bring out selected component terminals in the packaged devices to "jack-type" connection points on the patterned board which thus becomes an enlarged version of the monolithic Insta-Circuit.

Miniature patchcords, two to four inches in length, are provided for use in interconnecting the Insta-Board components into a desired circuit configuration. This interconnect procedure can be performed quickly so that the user can go from a circuit idea to a "monolithic" circuit in a matter of minutes.

Besides its applications in prototype circuit design, the Insta-Board is also an ideal tool for teaching integrated circuit concepts.

TIME SHARING SOFTWARE FOR SIGMA 5 COMPUTER — Scientific Data Systems has developed a time sharing software system for its Sigma 5 computer, thus adding simultaneous time sharing to the Sigma 5's batch processing capability, and increasing the number of time sharing computers in the SDS product line to four.

The new Sigma 5 time sharing system is a lower priced version of the time sharing system available with the Sigma 7.

The new software permits interactive time sharing for up to eight simultaneous users; at the same time the system runs batch problems written in Fortran, Cobol, or assembly language. Batch throughput is maintained at a high level by dedicating primary system resources and significant percentages of time to batch jobs and assigning on-line users to specified time slices as their demands require.

Sigma 5 time sharing configurations, including eight teletype terminals, 48,000 words of core memory, 6-million bytes of Rapid Access mass storage, and the usual complement of peripherals, lease for less than $13,500 per month. The minimum Sigma 7 time sharing configuration, which is slightly faster and offers greater growth capabilities, leases for under $17,000 per month.

MANAGEMENT CONTROL SYSTEM — PROMPT (Program Monitoring and Planning Techniques), a new computer-based management control package developed by ARIES Corporation, is now available for purchase, according to an announcement by William T. Miller, Jr., vice president of the firm's Proprietary Products Division.

Describing PROMPT as a "fine-tuned" PERT, Miller explained that it provides detailed computerized reports, oriented to multiple levels of management, so

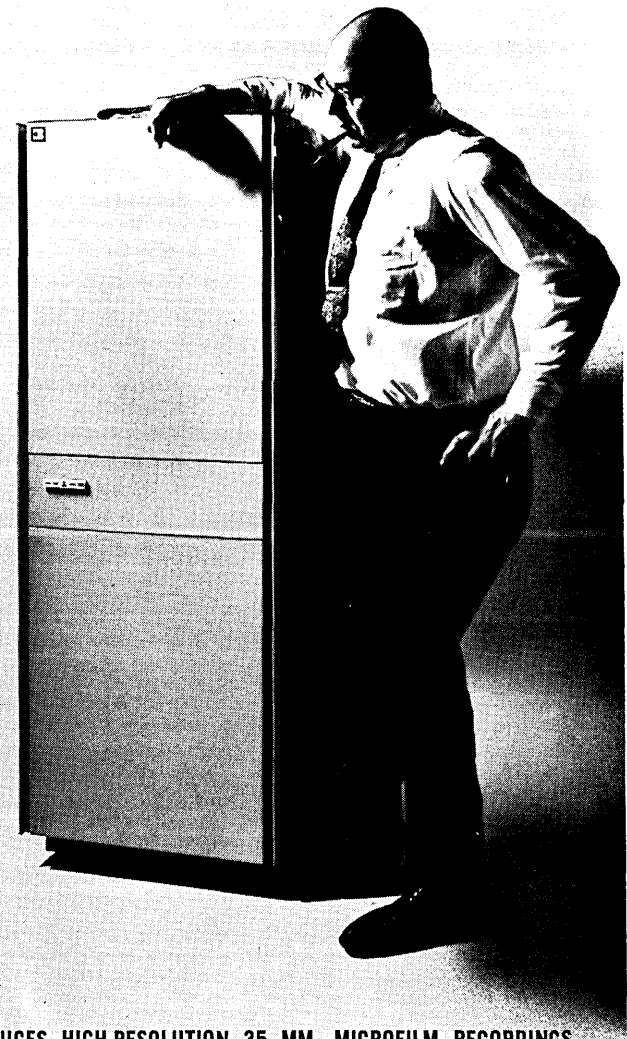
Continued on page 16

CIRCLE NO. 12 ON INQUIRY CARD →

Beta • graphics™

MICROFILM CRT RECORDER

MODEL MR606



PRODUCES HIGH-RESOLUTION 35 MM. MICROFILM RECORDINGS OF COMPUTER-GENERATED GRAPHICS AND ALPHANUMERICS.

Model MR606 is designed to be interfaced to a computer, coupled to a display controller or slaved to any graphical computer display.

The Betagraphics Recorder is a random-access X-Y device, featuring high-speed magnetic deflection, geometry correction of the image and dynamic focus of the electron beam. 1500 x 1500 resolvable elements are produced on film in a double-frame format. Positive fixed-pin registration provides ±.0005" frame to frame registration accuracy.

Operation is simple, with only two controls in addition to the power switch — an EXPOSE-ADVANCE switch for single exposure and frame advance and an EXPOSE switch for the multiple overlay or slow-buildup mode. All command and status interface signals are available for remote operation.

The Betagraphics line of peripheral display devices is here, now, to give you high quality computer graphics at reasonable prices. We'll be happy to send you complete specifications.

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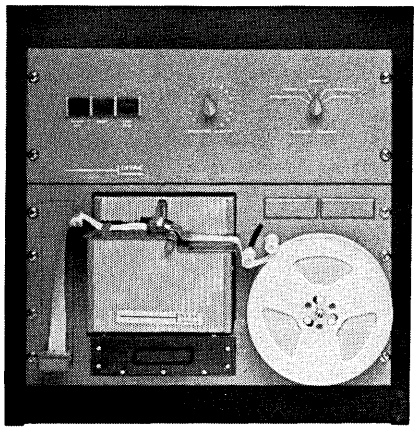
INVAC
DATA LOGGERS
PUNCH DATA AUTOMATICALLY



INVAC Data Loggers convert data signals directly into perforated tape in machine or computer format. Gone are costly, time-consuming, error-prone manual conversions. Compatible with the outputs from digital voltmeters, event or frequency counters, analog-to-digital converters, shaft or position encoders and other digital instrumentation.

. . . Single or multichannel inputs; simplex or multiplex
. . . Use any code or data format
. . . Punch speeds up to 60 cps
. . . Up to 60 digits per reading
. . . Up to 8 bits per character
. . . A-to-D converters available
. . . Optional Editing Keyboard or Typewriter

I/O TYPEWRITER is ideal for editing and data printout.

Write for Data

INVAC CORPORATION

A Division of DIGITRONICS CORPORATION

26 Fox Road, Waltham, Massachusetts 02154
Tel. (617) 899-2380

Systems Incorporating
TAPE PUNCHES READERS AND HANDLERS
PHOTOELECTRIC KEYBOARDS
I/O TYPEWRITERS AND PRINTERS

CIRCLE NO. 9 ON INQUIRY CARD

Continued from page 15

that they know exactly what's happening at any phase of their program cycle down to the most basic task performed by each man, every hour of the day. The system is said to have been proven in over three years of implementation at Aries.

"This new, upgraded commercially-available package," Miller said, "will permit management personnel to pinpoint work slippages, make cost-effective analyses of labor, optimize deployment of available resources and evaluate individual performance — while providing historical data which can be used as a reliable basis for planning new jobs."

The basic package is written in COBOL and includes a specifically-tailored program deck, three instruction manuals, an educational and usage indoctrination course, and technical assistance in setting up and running the program on the user's computer. Miller stated that the system is adaptable to any computer operation.

CANON INTRODUCES IC CALCULATORS — A Tokyo camera manufacturer has reversed current trends in the business machine and semiconductor industries by building electronic office calculators in Japan with integrated circuits made in the United States.

Canon Camera Company Inc. has introduced one-memory and two-memory desk-top calculators using 120 and 170 Texas Instruments monolithic ICs, respectively. Only 22 Japanese-made ICs are used in the units. Increased use of ICs in the new calculators is said to result in wider arithmetic capability at lower cost and higher reliability than possible with semi-integrated units.

Model 161S, Canon's one-memory calculator, will cost $1195. The two-memory Model 163 will cost $1395. The two-memory model, 163, performs three functions automatically: 1) regular storage, 2) item count, and 3) sum of the multiplicand. The latter two functions have not been available on previous electronic calculators. Both units will be sold by dealers of Canon USA, the company's marketing organization here.

By applying ICs to all circuits except certain power areas — numeral-tube amplifiers and a few switching functions — TI engineers helped Canon designers reduce the number of transistors in both calculators to only 60. This compares with 250 to 317 transistors in existing imported IC calculators. The change also reduced the number of diodes to 100 instead of the 1,200 to 1,775 in the existing calculators.

TI will deliver 270,000 of its DTL (diode-transistor-logic) integrated circuits to Canon each month — believed more than Japan's entire monthly production of DTL circuits. The ICs will be made at TI's semiconductor manufacturing facilities in Dallas.

PROTOTYPE TAPE TRANSPORTS FOR POSEIDON MISSILE — Potter Instrument Company, Inc., has delivered the first six prototypes of an advanced-design, dual magnetic tape transport system to the U. S. Navy's Fleet Ballistic Missile program. Developed under subcontract to the Sperry Systems Management Division of Sperry Rand for use in the Poseidon Navigation System, the prototypes are undergoing extensive environmental and other testing by the Navy and other facilities to the rigid specifications required for operation in electronic data processing systems aboard the Navy's missile firing submarines.

The transports contain more than one-thousand (1,000) micro-integrated circuits per system with each system being completely redundant for added reliability. The transports also possess diagnostic routine capability.

BACHELORS OF COMPUTER SCIENCE—The Purdue University Department of Computer Sciences will introduce an undergraduate degree program in computer science next fall.

Prof. S. D. Conte, head of the department, observed that needs are rapidly increasing in Indiana and throughout the country for computer scientists with bachelor's degree backgrounds.

"By permitting students to begin college thinking about computers as a focal point rather than a sidelight in their studies," Conte said, "we believe more will become interested in careers in the field."

As a further step in this direction, he said, Purdue will eventually implement similar bachelor's degree programs at its regional campuses in Indianapolis, Fort Wayne, Hammond and Westville. The four now have two-year associate degree programs in computer technology.

WHY COMPROMISE?

NEED RELIABILITY IN YOUR SYSTEM?

The PDC-808 Programmed Digital Controller was designed for those applications requiring long term reliability. We run the memory at eight micro-seconds to obtain low power consumption, broad operating margins, and complete interchangeability of parts.

CONCERNED ABOUT PROGRAMMING COST?

The PDC-808 is easy to learn and easy to program. There are no gimmicks. The instruction set is straightforward and powerful. Liberal use of Macro instructions keeps programs short. The logic is in the machine, not in software.

WATCHING YOUR SYSTEMS COST?

If your system needs a controller, buy a controller; one that is designed for control applications. Avoid the inefficient, microprogrammable "core burner." An additional 4K memory module may wipe out any potential hardware savings.

Memory utilization in the PDC-808 is the highest in the field. A 12-word bootstrap for instance. The debug package requires only 512 words. Register change, control, skip and shift instructions use only 8 bits of memory, and use only 1 memory cycle. Memory Reference and I/O use 16 bit instructions for power and flexibility.

The PDC-808 interface is the most economical and powerful in the industry. Why spend money in logic outside the machine when the problems have been solved inside the PDC-808. This means bucks saved in parts cost and engineering time. Your bucks.

Your savings start with the purchase price. $6600 for PDC-808 with 4K memory, console and power. No give-aways. Just the best buy going.

COMPUTER AUTOMATION, INC. / 895 W. 16TH ST., NEWPORT BEACH, CALIF. 92660

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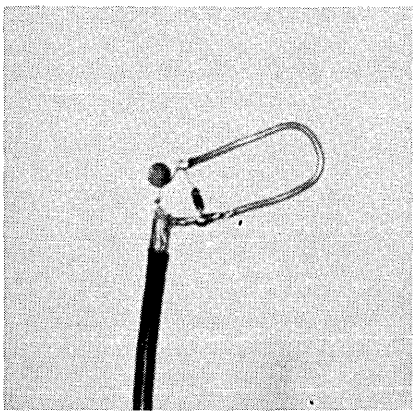
CIRCLE NO. 10 ON INQUIRY CARD

DEVELOPMENTS

Oscillator Invention Capable of Increasing Computer Speeds

Two Australian scientists Dr. F. Hirst, head of the Computation Department of the University of Melbourne, and Dr. P. Thorne, a research fellow of the department, have invented a device which they say is capable of increasing computer speeds by 500 times.



Dr. Hirst will deliver a paper about the discovery at the International Federation of Information Processing conference to be held in Edinburgh, Scotland, from August 5 to 10.

In 1961, Mr. T. Pearcey, of the division of computing research of the Australian Commonwealth Scientific and Industrial Research Organization, and Dr. Hirst began computer investigations of the nature of the solutions of a certain mathematical equation. In 1962, Dr. Hirst suggested that a certain feature of the solution of the equation could be used to design a computer memory cell. In 1963, Dr. Thorne began research into electrical networks that would be in practice the equivalent of the mathematical equation arrived at by Dr. Hirst and Mr. Pearcey.

These efforts led to the development of an oscillator which can operate in two modes of vibration. Since the computer counts in a scale of two's rather than decimals, the basic cells of a computer's memory must be able to operate in two states. In conventional computers this requirement is accomplished by using electromagnetic cores which can be magnetized in either of two directions. With available components the new device should achieve a speed of about one nano second.

New Type of Electronic Display Utilizes Liquid Crystals

Scientists at RCA Laboratories, Princeton, N. J., have developed flat, low-power, low-cost displays using a newly discovered electro-optical effect in liquid crystals. The displays can reproduce any graphic data electronically and can be addressed and driven by solid-state, integrated circuits. They are said to be simple to operate, to have no moving parts, and to be compact and rugged.

Liquid crystals are organic compounds having the mechanical properties of a liquid and the regular molecular arrangements characteristic of a polycrystalline solid.

Early research disclosed that certain transparent, liquid crystals at high temperatures became milky white when exposed to electric fields, but returned to their transparent condition when the electric field was removed. Since then, new materials that exhibit this behavior at room temperature and over a range from 0° to 212°F have been developed.

When an electric field is set up on certain liquid crystals, its presence creates ions that travel through the material. These traveling ions then produce an effective turbulence that causes a dynamic scattering of light and give the liquid crystal a milky white appearance.

To construct a display, a thin film of liquid crystal only one one-thousandth of an inch thick is placed between two sheets of thin glass. The inner face of each sheet is coated with an electrode. At least one of the electrodes must be transparent so the display can be seen. This electrode is usually a conductive species of tin oxide. The other electrode may also be transparent, or it can be reflective, in which case it is ordinarily an evaporated film of metal such as nickel or aluminum. In effect, the display is a parallel plate capacitor with the liquid crystal acting as the dielectric.

Thus far, RCA has made liquid crystal displays up to 3 x 4 inches. However, there appears to be no reason why they cannot be made substantially bigger. Obviously, if there were no other way, very large displays could be formed from mosaics of smaller ones.

Liquid crystal displays have a grey scale that varies with the intensity of the applied voltage, which ranges from 6 to 60 volts. The power required for a reflective display is one milliwatt per square inch and can be either DC or pulsed. Pulsed power is used when the effect of motion is desired, the pulses being addressed to minute areas in proper sequence through integrated circuits. Operating tests of experimental liquid crystal displays thus far have shown that they last in excess of 3,000 hours.

Electron Gun Development Improves CRT Performance

A cathode-ray tube electron gun developed by Rank Electronic Tubes, Sidcup, Kent, England is reported to be the first to have its electron beam almost completely collimated by an electrostatic focusing system before the final aperture of the gun. Advantages include longer life, uniform brightness of spot and line, uniform spot size across the screen and increased current density.

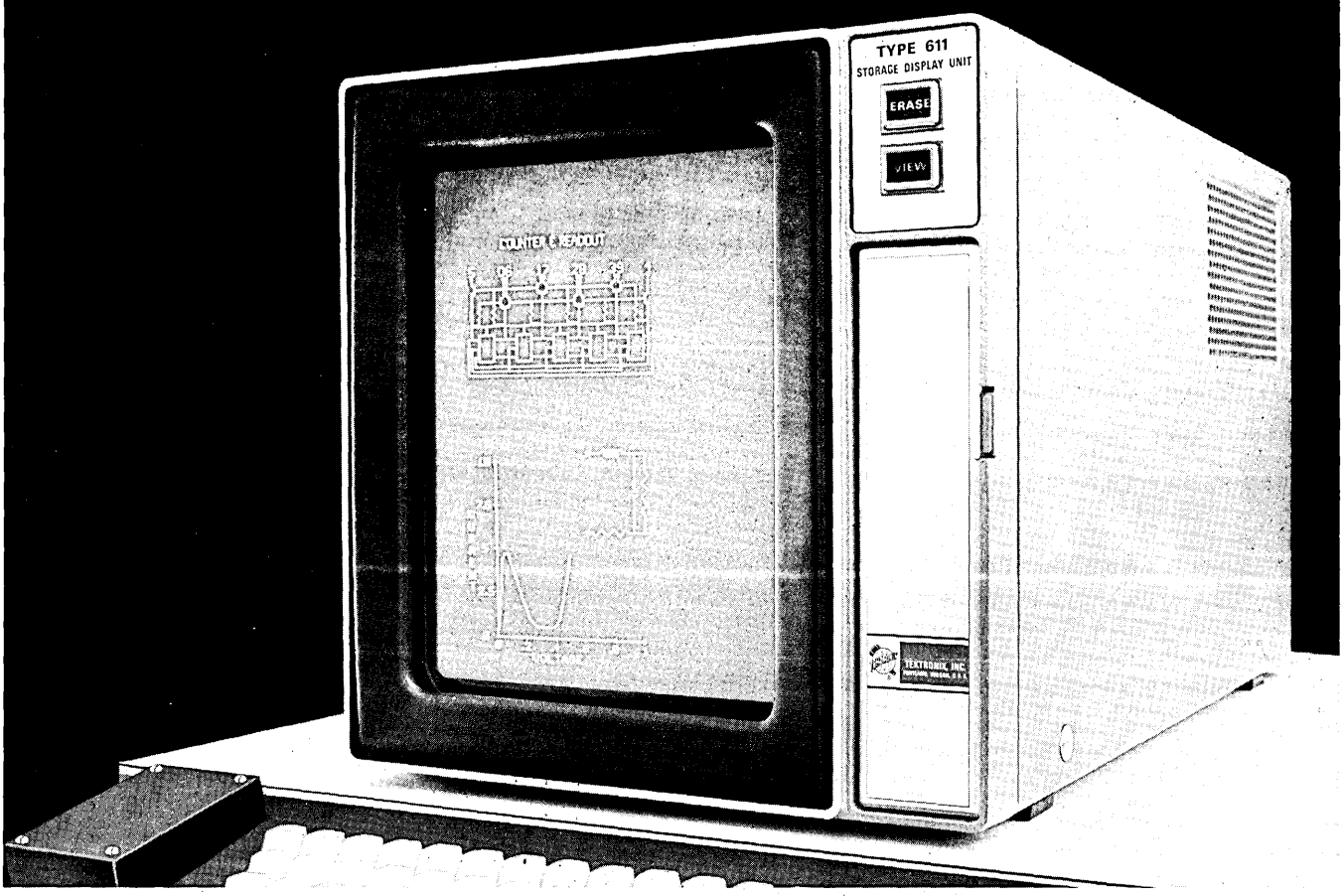
The design allows tubes to be operated over a wide range of screen potentials while the gun potentials remain far below the level at which internal sparking and cold emission occur.

Widely different final anode potentials can be applied, according to application. For any potential, brightness is greater than that of a conventional tube, and peak cathode loading is said to be lower than that of other guns, thereby increasing life expectancy. Energy distribution (and therefore brightness) is substantially uniform across the spot and across a scanned line. The beam diameter at the point of deflection is small, so that deflection distortions are minimized. The spot size is substantially constant over the whole tube face.

Electron acceleration is provided by a helix on the inside of the tube which is integral with the electron optics. Deflection coils can be placed over the helix to introduce a post-deflection acceleration for increased sensitivity.

continued on page 20

Flicker-Free CRT Storage



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DEVELOPMENTS

continued from page 18

The spot shape on the screen is an exact image of an aperture of the gun, and spots of any shape can be produced. Size remains constant despite increase of drive voltage, and astigmatism and coma—distortions of the spot shape — are minimized. Spot size can be varied up to ½" in diameter by adjustment of the gun potentials without loss of focus or alteration in brightness. The variable spot size is said to make the gun suitable for use in data display applications where differing line widths are often required.

Magneto-Optic Memory Elements Successfully Demonstrated

Scientists at the Lockheed Research Laboratory Palo Alto, Calif. report they have successfully demonstrated the use of gadolinium iron garnet (GdIG) memory elements with stable bit densities of 10^6 per square inch.

The GdIG magneto-optic memory element was proposed by Chang, Dillon and Gianola in 1965. The basic property of GdIG utilized for memory purposes is the coercivity of the magnetization as a function of temperature shown in Fig. 1.

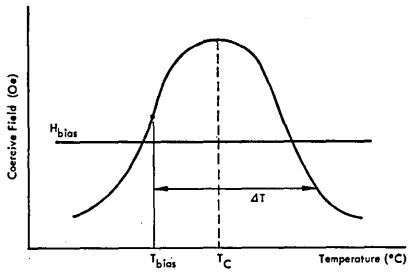

Fig. 1. Coercive field vs. temperature for GdIG.

Procedure for operating GdIG as a memory element is as follows: A film or wafer of GdIG is magnetized to saturation normal to its surface. The field is then reversed and increased to a value below the coercive field at the bias temperature T_{bias}. A writing beam which can be a laser or electron beam is used to heat a small spot of the wafer to $T_{bias} + \triangle T$. Fig. 1 shows that, in this spot at this temperature, the magnetic bias field exceeds the coercivity. Therefore, at the heated spot the film will magnetically switch; that is, a bit is written.

To read the information thus written on the memory, the film is illuminated by polarized light. Direction of the magnetization is sensed by the sign of the Faraday rotation. In the written bit the rotation is opposite to the unwritten part of the film. By analyzing the polarization of the light, the bit can be interrogated electronically.

Thin wafers of GdIG, made by sectioning and polishing single- and polycrystals, were studied magneto-optically to determine the parameters useful in conjunction with the use of the crystals as memory elements. It was found that coercivity determined by Faraday rotation in these wafers was tenfold higher than that in bulk material determined by conventional means.

Thermal and coercivity considerations showed that for a given thermal input, a steep and wide peak in the coercivity versus temperature curve is desirable for small bit size and high writing speed. This was confirmed experimentally and a bit density of 10^6/sq. inch was obtained on poly-crystalline wafers. Bits were stable with time and with temperature up to 50°C. They could be erased selectively by the same writing beam with reversed magnetic bias. In addition, a memory cycling test, consisting of writing, erasing and rewriting of a point on the wafer, showed no degradation of performance after three million cycles.

For writing, a He-Ne laser beam (8mW at 6328Å) was focussed to about 10 microns in diameter. In a typical case, bits were spaced 1.5 mils between centers and were well resolved. With 1 mil between centers (10^6 bits per square inch), packing density approached the resolution limit of the wafer. Such a resolution limit is closely related to the grain size of the investigated sample. In the polycrystalline samples, grain sizes are in the order of 10 microns. Thus, on the average, the bits which are packed 1 mil between centers cover only three to four grains per bit. Smaller grains would give even higher density.

Because of the lack of an efficient optical deflector for large numbers of deflections, the arrangement of Fig. 2 is considered for implementation. A finely focussed electron beam is an efficient tool for heating a small spot and fast deflection of 1000 spots is achievable. For convenience in reading, bits in the film are organized into an array of submatrices. Instead of point-to-point deflection of a focussed optical beam to illuminate a bit, deflection of a large beam, e.g., from a discharge lamp, to illuminate the submatrix is used to lessen the requirement imposed on the deflector and light source. As an example, for a one square inch memory plane containing 10^6 bits, the number of deflections need only be 7 x 7; such a deflection at megahertz rates can be readily obtained by using electro-optic crystals.

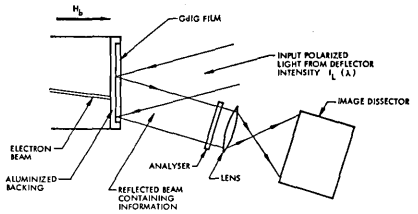

Fig. 2. Advanced writing and reading arrangement using GdIG memory element.

The random access feature is preserved by interrogation of the large beam with either an image dissector or a photodiode array. Combination of the controls of the deflector and the sensor will then give precise access to the bit.

Since the GdIG film is a good insulator, a thin film of aluminum is evaporated over the GdIG to avoid any charging during electron beam writing. With such an arrangement, the most convenient way of reading is to interrogate the reflected light which has essentially double rotation due to the double pass of the light through the film, as shown in Fig. 2. The lamp and the dissector required in this scheme are commercially available. The magneto-optic memory element is under evaluation for use in airborne high density data storage applications.

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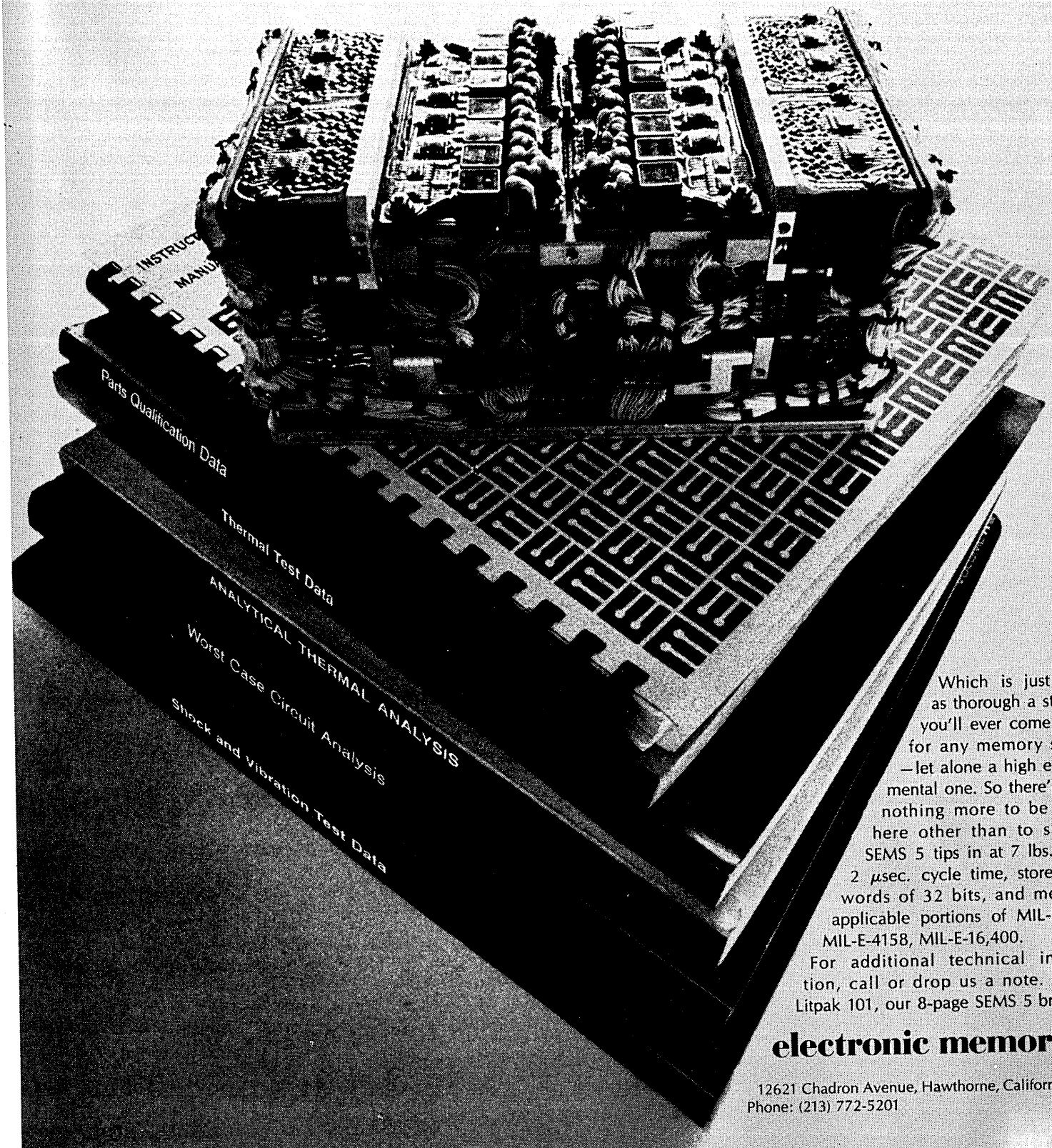

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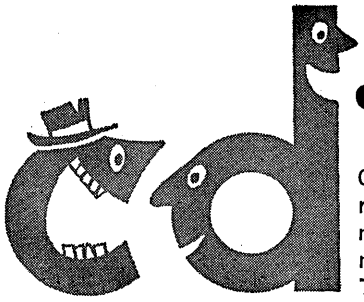

commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

FERRITE CORE MEMORIES
Present & Future Status

R. W. Reichard

Just as the internal-combustion engine has survived the challenge of numerous contenders for its role in the automobile industry, the ferrite core memory continues to survive the onslaught of many contenders for its role in the digital computer industry. It would be generally conceded that the latter work-horse has undergone considerably greater evolution, however, as indicated in Table I.

The latter three columns indicate an order of magnitude increase in capability, which is a most impressive feat. Obviously, not all of this is attributable to ferrite core characteristics, but there certainly have been synergistic attainments in the areas of active devices, packaging, market demand, and other relevant factors.

Although Table I does not involve the parameter of time, it has been noted previously in this column and elsewhere that the cost and cycle time of core memories have simultaneously halved about every 2½ years during the past decade. It is highly conjecturable that this can continue and there exists some tangible reasons for expecting the fall-off rate to decrease:

1. It appears, as noted in the table, that capacities are leveling off. At the moment, one is inclined to project that main memory will comprise several identical modules, each of a few hundred kilobits capacity. Since some contribution to falling costs in the past were due to amortization of fixed costs — registers, timing, control, hardware — over increasing number of bits, a leveling off of capacity curtails this possibility.
2. Considering fully switched cores of present materials, cycle time can decrease only via smaller cores. Cores cannot continually progress to smaller diameters unless smaller wire is used. There just may be practical limits on usable wire size. Number 44 wire has a fusion current rating of about 0.8 amperes, which is not too comforting, relative to 0.4-to-0.5 ampere drive currents for state-of-the-art small cores, especially in direct-coupled drive circuitry and arrays with limited heat-transfer ability.
3. The ferrite core plane industry has long been highly competitive and still suffers from a high ratio of labor cost to material cost in its product.

TABLE I

Cores of This Diameter	With Switching Time Of	Enabled System Cycle Time Of	And System Capacity up to	To Be Sold at a Per-Bit Cost Of
80 mils	1.5 μsec.	12 μsec.	20 kilobits	$1
50 mils	0.9 μsec.	5 μsec.	80 kilobits	$ .30
30 mils	0.4 μsec.	1 μsec.	200 kilobits	$ .12
23 mils	0.25 μsec.	0.6 μsec.	300 kilobits	$ .08

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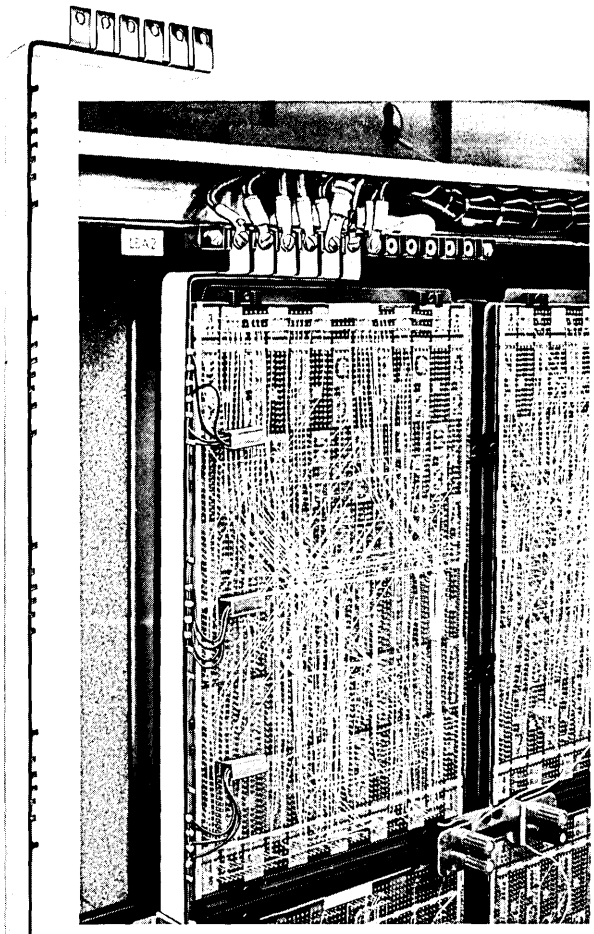

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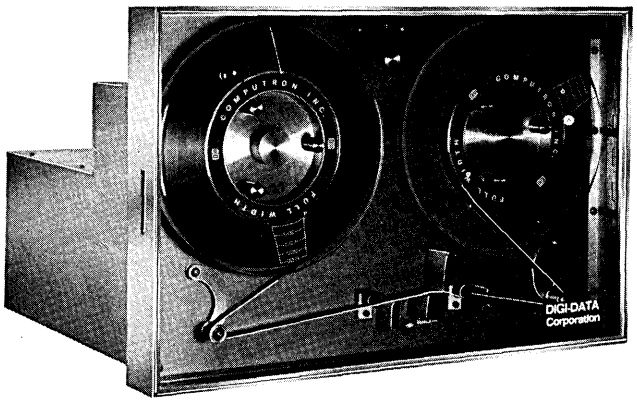

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CIRCLE NO. 15 ON INQUIRY CARD

The desire to lower labor costs by automating the process of threading cores may provide further restraint against continuing reduction in size of cores.

All of the factors above tend to indicate that the ferrite core memory business may be reaching a static state, which almost inevitably indicates demise in such a dynamic industry as digital computers. It is tempting to indulge in idle speculation on avoiding such a fate, and as electrical engineers are prone to do, we cast the blame for our ills upon the metallurgists or materials technologist.

In this case, we point out that the availability of a core material of several times the flux density and a fraction of the coercive force of present cores, with similar squareness ratio and switching constant, would enable us to score another giant step in the performance race. This latter step, incidentally, would probably seal the fate of flat-film memories, resulting in a copout for Uncle Sam who has invested several tens of millions of dollars in sponsoring flat-film memory developments over the past decade. However, there are some newly emergent factors that may be considered which offer new possibilities.

1. The continual downward trend in monolithic integrated circuit costs, which has already enabled the decade-old $2\frac{1}{2}D$ selection scheme to become an economic practicality, may enable other long-since pigeonholed ideas to be resurrected and economically applied. One plausible example is that the necessary complex circuitry for a common sense-digit scheme may be economically realized since the number of semiconductor devices is not a design restraint. The result of this might be, for example, practical two-wire arrays in high-performance systems.
2. A reduction in monolithic circuit costs, as in the previous section, must prompt reconsideration of linear selection schemes, which offer the possibility of faster cycle times with given core sizes.
3. Limited dissipation capability of IC's suggests partial switching of cores; the latter enables higher speed with given core size and limits self-heating effects as well. The penalty for partial switching historically has been the expense of providing stringent control on pulse current amplitudes and durations, particularly if an operating ambient temperature range of more than a few degrees was necessary. The improved uniformity of present-day cores mitigates these problems and in fact the technique of using two cores per bit would further alleviate it.

It is, therefore, to be expected that once more, advancing technology and techniques will further extend the applicability of core memories.

Mr. Robert W. Reichard, the author of this month's CD Commentary, is Manager of the Memory Products Engineering Department at Honeywell's Computer Control Division. He is responsible for the design, release and sustaining engineering for the division's high speed computer and product memories.

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The major considerations for high speed computer designs are propagation delay, clock pulse skew, noise, crosstalk, and integrated circuit performance. All of these considerations can be significantly enhanced by the implementation of the Micro-Electronic Modular Assembly (MEMA) *packaging technique.*

HIGH SPEED

The electrical characteristics of packaging and the interconnections in high speed digital computers can introduce limiting restrictions on computer operation. Therefore, it is necessary for the electronic designer to consider seriously the implications of the packaging and interconnections and for the package designer to consider the electrical characteristics of the physical design. The packaging techniques, described in this article, illustrate the approach developed from the collaboration of the logical, electronic, and mechanical designers at Teledyne. In addition, the Advanced Systems Division has maintained full cognizance over the detailed hardware design and system design to ensure compatibility on all levels of development.

The approach to the micro-miniaturization of electronic equipment that has been adopted and developed, is one in which multiple components, including monolithic integrated circuits chips, are mounted and interconnected within a single flat pack. Designated as the Micro-Electronic Modular Assembly (MEMA), these multichip circuit modules have already found applicaion in digital and analog equipment for major avionic systems. The advantages made possible by the use of this packaging technique are dramatic reductions in system size and weight, greatly simplified manufacturing and maintenance procedures, increased reliability and performance and considerable savings in recurring manufacturing costs.

This technique takes maximum advantage of the characteristics of integrated circuits. These are:

1. Preserving the small size characteristic of the integrated circuit chip by placing many chips in a single package.
2. Preserving the high speed characteristics of the integrated circuits by placing them in very close proximity with extremely short interconnections.
3. Preserving the inherent reliability of the integrated circuit by eliminating multiple packaging levels.

The MEMA is implemented by interconnecting up to thirty integrated circuit "bare chips" on a single ceramic substrate (Fig. 1). The substrate and associated electronics are then hermetically sealed to form the completed MEMA, which has the physical characteristics of a single flat pack, but contains the functional complexity of several large printed circuit cards with discretely packaged integrated circuits.

Several levels of functional modularity are mechanized to form a high speed digital computer (Fig. 2). The integrated circuit "bare chips" are mounted and interconnected within the MEMAS, which are mounted and interconnected on submodules. The submodules are clipped together to form modules, and the modules are plugged into the motherboard to form the computer.

High speed digital computers require special considerations involving propagation delay, clock pulse

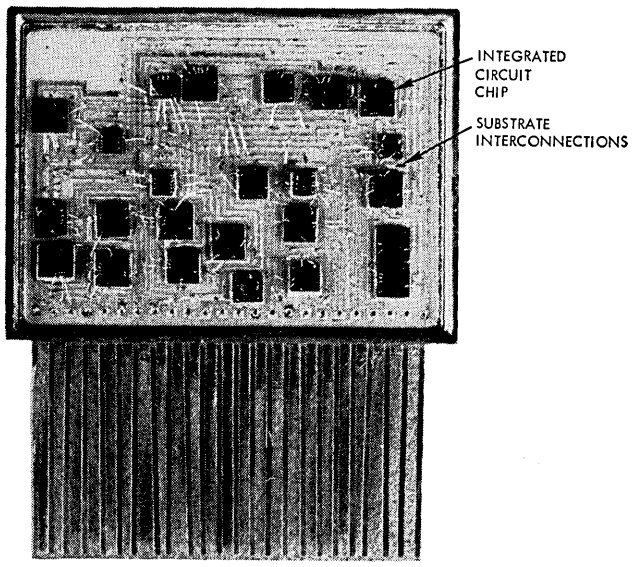

Fig. 1 Micro-Electronic Modular Assembly (MEMA).

COMPUTER MECHANIZATION

G. P. HYATT

Consulting Editor
Computer Design

skew, noise, crosstalk, and integrated circuit performance. Each of these considerations can be significantly enhanced merely by reducing the physical size of the computer. Special design techniques will improve these considerations, but to a lesser degree than the physical size consideration. Miniaturized computers implemented with MEMA type techniques inherently minimize these considerations to the degree that they are not the predominating limitations associated with high speed computers. In addition, many of the special high speed computer implementation techniques may be eliminated merely by using the MEMA type packaging to miniaturize the computers.

PROPAGATION DELAY CONSIDERATIONS

Propagation delay of digital pulses is generally caused by two mechanisms, which are:

(1) The switching delay through logic functions, determined by the switching speed of the logic.

(2) The transmission delay through interconnections, determined by the velocity of propagation through the medium and settling of the signal due to impedance mismatches.

Interconnections in electronic systems are often treated as simple conductors. This approach is valid

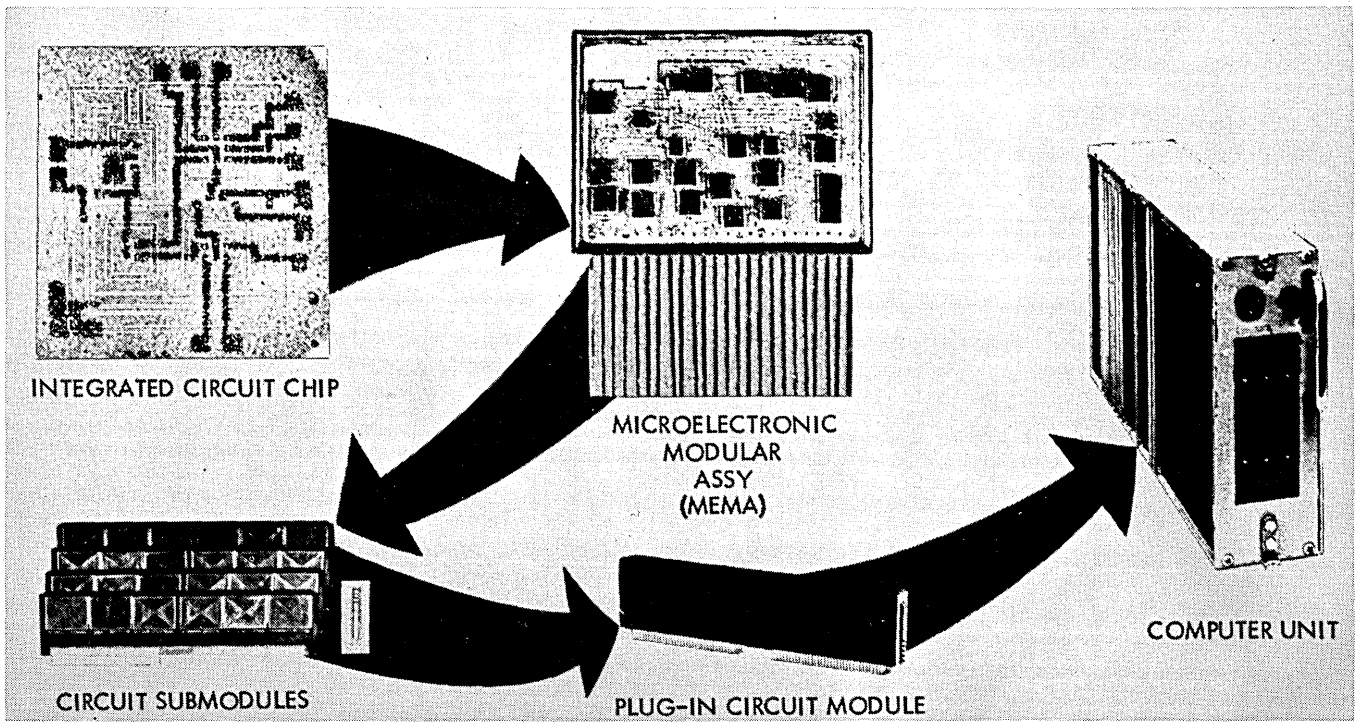

Fig. 2 Levels of modular packaging.

only in relatively slow speed, small dimensional systems. In applications with clock periods that approach the transmission propagation delays, the interconnections must be considered as transmission lines. The high speed switching of the digital logic can introduce Fourier frequency components in the hundred megacycle frequency range, which is in the low radar band. Much of the theory associated with electromagnetic fields and waves as applied to radar systems is directly applicable to these systems.[1]

The criterion for the treatment of interconnections as either conductors or transmission lines is based upon a comparison of the clock periods and transmission propagation delays. If the propagation delay along a line is in the order of magnitude of the clock period, the interconnections should be treated as transmission lines. An electrical signal will propagate at approximately one foot per nanosecond for a nominal permitivity (ϵ) and permeability (μ) of the surrounding median. A transmitted signal will propagate along a line to an impedance mismatch interface, where a portion of the energy will be reflected. This reflection will propagate along the line in the reverse direction to another impedance mismatch interface, being reflected back and forth until the signal in the line stabilizes at the excitation level. The number of reflections that will occur prior to the signal stabilizing at an acceptable level is a function of the impedance mismatch. For larger mismatches, a larger number of reflections will occur prior to stabilization. For relatively longer transmission lines or lower propagation velocities, the delay for each reflection will be relatively longer. Therefore, the propagation delay through a wire is a function of the impedance mismatch in addition to the line length and propagation velocity.

For short lines and relatively slow clock rates, successive reflections will stabilize in a relatively short time compared to the clock period. For long interconnections or fast clock rates, the line stabilization periods may approach the clock periods and become a significant consideration. Relatively long interconnections can be better tolerated if impedance matching is implemented. The integrated circuits typically contain a low output impedance and a relatively high input impedance to enhance noise immunity and fan-out. Typical transmission lines provide a good impedance match with integrated circuit output impedances, but introduce a moderate impedance mismatch with integrated circuit input impedances. The fan-out to multiple input loads can reduce the mismatch considerations because the input loads are, effectively, in parallel. Impedance matching can generally be accomplished by adding terminating resistors to the high impedance end of long interconnections to minimize reflections and the resulting signal stabilization delays. Pulse transformer techniques could also be used to satisfy the impedance matching considerations, but result in a higher hardware complexity than with resistive termination.

The switching propagation delay, characterized by the state transition delay in switching the electronic elements, is typically in the range of tens of nanoseconds for present higher speed integrated circuits. It is generally important that the propagation delay due to the logic elements be large compared to the difference in propagation delays between the various paths, in order to minimize the clock pulse skew considerations.

The interconnections between integrated circuits within a MEMA contain line lengths of less than an inch, with typical propagation delays in the magnitude of tenths of a nanosecond. The electrical signals in these lines will stabilize in sub-nanosecond periods, even for the more severe impedance mismatch. The interconnections between the MEMAS are less than six inches within each submodule. Therefore, line propagation delays assemblies in the same submodule will be a fraction of a nanosecond for impedance matched lines and a worst case of under two nanoseconds for mismatched lines of the magnitude obtained with integrated circuit terminations. The longest transmission line within the typical computer is approximately one foot. In addition, approximately four inches of interconnections are contained in small links interconnecting localized logic in the same chain. Therefore, the maximum transmission line length will introduce a propagation delay typically of several nanoseconds and in the very worst case, under six nanoseconds. This worst case line propagation delay is in the magnitude of a single high speed integrated circuit gate propagation delay. Therefore, the small computer dimensions associated with the MEMA type packaging techniques reduces the worst case interconnection propagation delays to a very small value, even with severe impedance mismatches.

Impedance matching techniques within the high speed digital computer implemented with MEMA techniques can be neglected due to the extremely small dimensions. Computers with larger dimensions must implement impedance matching to the degree dictated by the transmission delays and impedance mismatches.

CLOCK PULSE SKEW CONSIDERATIONS

The clock pulse generation for a high speed computer requires special considerations to insure proper operation. The clock pulse skew condition is a serious potential problem that can cause "critical race" conditions. The design should fully consider the clock pulse skew condition and minimize this effect to the level where it will not jeopardize computer operation.

Effectively, the clock pulse skew condition reduces to that of unequal propagation delays for the synchronizing clock pulse to various logic elements. This condition may cause the data changes to propagate more rapidly than the clock pulse, resulting in critical race conditions that can cause erroneous or ambiguous data to be set into the flip-flops. Clock pulse skew is caused primarily by:

1. Unequal propagation delays through the clock pulse transmission lines, primarily due to unequal line lengths between the clock pulse generator and the synchronous elements.
2. Unequal propagation delays through logic chains, primarily in the clock pulse fan-out network, caused by an unequal number of stages or a spread in switching delays of the integrated circuits.

The reduction of the longest clock pulse transmission delays will significantly aid in the minimization of the clock pulse skew effect. Inherent in the different transmission delays between the local and the more remote synchronous elements, the longer the distance that a clock pulse line must be routed, the more skew that will be introduced. The longest clock pulse transmission lines can be reduced in length by physically locating the clock pulse generator and fan-out circuiting in the center of the computer. In addition, certain types of logic functions that are not sensitive to the skew effect should be located at the more remote parts of the computer. This technique will permit the more critical forms of logic to be located in closer proximity to the clock pulse generator. Logic that requires communication in only one direction, such as computer input/output logic, and logic that can operate asynchronously are types that are not sensitive to the clock pulse skew effect.

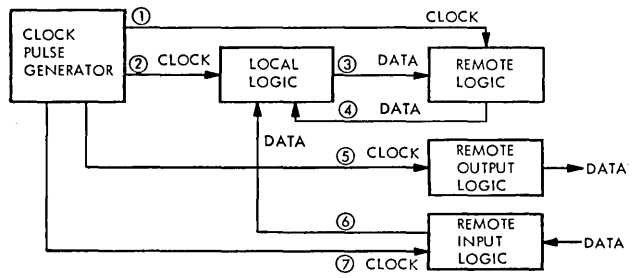

Fig. 3 Systems communication.

A typical implementation of communication within a synchronous digital system is illustrated in Fig. 3. The clock pulse generator will clock local and remote synchronous logic elements. This clock will cause data changes to propagate through the system. If the data change from the local logic propagates to the remote logic before the clock pulse, a hazard condition will exist. Therefore, the sum of the delays along paths 2 and 3 must exceed the delay along path 1 (Fig. 3), to eliminate hazards due to the clock pulse skew effect. It should be noted that paths 4, 5 and 6 are not sensitive to the clock pulse skew effect.

The clock pulse propagation delays between local and remote synchronous elements can be equalized by:

1. Increased propagation delays in the clock lines that are routed to local synchronous elements, defined by path 2 (Fig. 3).
2. Increased propagation delays in the data lines that are routed from local to remote parts of the computer, defined by path 3 (Fig. 3).
3. Decreased propagation delays in the clock lines that are routed to remote parts of the computer, defined by path 1 (Fig. 3).

The techniques described in items (1) and (2) are the most convenient to implement; accomplished merely by adding propagation delays. The techniques described in item (3) can only be implemented with considerable design effort, because propagation delays in high speed computers are typically low and therefore not easily reduced further. It should be noted that item (3) can be implemented with the use of MEMA packaging techniques, where propagation delays can be reduced by approximately an order of magnitude. Therefore, the computer will require a minimum of special considerations for clock pulse skew effect.

The propagation delays in clock lines to local synchronous elements can be increased with the use of both transmission delays and switching delays. The transmission delays can be implemented by increased line length through indirect routing, coiling, or lumped parameter delays; impedance mismatching; and the use of transmission lines with lower propagation velocities. The latter technique is the most feasible, where the delay can be precisely defined and accomplished in a manner physically identical to an unequalized system. The switching delays can be implemented by longer clock fan-out chains, capacitive loading of clock fan-out logic, and the application of slower speed logic elements in the clock fan-out chain associated with the local synchronous elements. The latter technique is the most feasible due to the availability of compatible integrated circuits with different characteristic switching speeds, permitting implementation in a manner physically identical to an unequalized system.

The propagation delays in data lines from local to remote synchronous elements can be increased by the techniques discussed for the clock line delays, with the additional technique of implementing the local synchronous elements with slower speed logic elements.

The propagation delays in clock lines to remote synchronous elements can be decreased by using techniques converse to those discussed for items (1) and (2). The use of high speed clock fan-out logic, directly routed high velocity transmission lines, and accurate impedance matching techniques will reduce propagation delays; but the most effective technique will be to reduce the computer physical size with MEMA type packaging.

The clock pulse fan-out should be performed in a radical tree type of array where a different clock line is routed directly to each module, as contrasted to a "daisy chain" distribution where a single clock line is strung out from module to module. Clock pulse fan-out in a localized area, such as a MEMA, may be accomplished in a "daisy chain" manner with inconsequential skew problems. Proper termination of all of the radial clock pulse lines should be implemented, where necessary, to insure mimimal, but well defined, clock pulse propagation delays.

The clock pulse fan-out logic should be implemented to minimize the number of levels of logic required. This precaution is taken because of the spread in the propagation delay parameters for the fan-out gates. The characteristic of relative consistency of the propagation delay through the gates on a particular chip should be considered. In addition, clock pulse fan-out and control logic chains should contain equal numbers of logic elements to equalize delays to corresponding parts of the computer.

The dimensions of the typical computer, implemented with MEMA techniques, reduce transmission delays to a level so small that the only delays that need be considered are unequal clock pulse fan-out switching delays. Effectively, the small dimensions automatically relegates the physical considerations to an insignificant level when compared to the electrical considerations.

NOISE AND CROSSTALK

Noise generated by the switching operation of the logic devices can be divided into two predominating mechanisms, defined as power supply transients and digital crosstalk. The actual mechanisms are too complex to define rigorously but can be treated as generalized lumped parameter effects.

The power supply transients are generated by the state switching of the logic devices. A state transition will result in transients reflected through the power supply lines caused by the current surge drawn during the state transition and by the step change in steady state current drawn between the two logic states of the logic gates. The state transition will cause a power surge to occur because the circuit output is neither in cutoff nor saturation during the switching transition. This surge will correspond in time and duration with the rise and fall times of the logic elements. The surge current will cause voltage drops in the power supply lines due to the line resistance and inductance. The inductive drop will predominate due to the high rate of change of the surge, causing a large di/dt voltage drop, as compared to the low current amplitude, causing a small iR voltage drop. The step change in steady state current will be caused by the different power requirements of the logic gates in the two binary states; this condition will contribute only to the resistive voltage drop and is, therefore, of small consequence.

The voltage drop will be distributed along the power supply line, contributed to by all logic elements common to that power supply line. The power supply transients will couple through the circuits and transmission lines, resulting in noise on the logic signals and, possibly, false triggering of the synchronous elements.

The digital crosstalk can be described as the reactive coupling of digital pulses between lines that are routed in close proximity. This crosstalk can result in forward and backward travelling waves.[2] It can couple into clock lines and cause false triggering of the synchronous elements.

The noise and crosstalk mechanisms described will be primarily a function of the line lengths, where the inductance of the power supply lines is a function of the line length and the reactive coupling for power supply and data logic line transients is a function of line length.

These sources of digital noise can be reduced by the selection of low inductance power supply lines, decrease in the distance through which lines are routed together, and decrease in line length. The latter technique is the most effective because short lines inherently decrease line inductance, and decrease the distance that lines are routed together. The decrease in line length is inherently implemented by the MEMA type packaging which reduces the noise and crosstalk considerations to a minimum.

INTEGRATED CIRCUIT PERFORMANCE

High performance integrated circuits are required for high speed computers, where many of the characteristic circuit parameters can be significantly enhanced by the reduction in the length of interconnections and the resultant line capacitance. The circuit characteristics that are most affected by the interconnections are the: switching speed, noise immunity, fan-out and power consumption. These parameters are primarily a function of the intrinsic characteristics of the circuits, but can be significantly affected by the packaging and interconnections for high speed applications.

The switching speed of an integrated circuit is a function of the capacitive load that must be driven. The load will define an RC time constant associated with the circuit source impedance and the line capacitance. A large line capacitance, caused by relatively long interconnections, will require the circuit to discharge a relatively large amount of charge through the output impedance. The switching speed will be degraded by the associated time constant.

The noise immunity of a computer can be enhanced by reducing the characteristic noise generated by normal computer operation. The computer will tolerate an externally imposed noise level that depends upon the inherent noise immunity of the circuits degraded by the internally generated noise "bias" of the computer. The reduction of this noise "bias" will increase the effective system noise immunity. The internally generated noise has been previously discussed, classified as power supply noise and crosstalk. This noise can be significantly reduced by decreasing the interconnection line lengths, thereby reducing the computer noise "bias" and effectively increasing the system noise immunity.

The fan-out of an integrated circuit is a function of the steady state load and the switching load imposed on the circuit. The steady state load is defined by the number of circuits loading the signal. The switching load will be composed of the capacitive load of both the line and the circuits that are loading the signal. For high speed operation, the switching load can present the predominating limitation on circuit fan-out. Therefore, the fan-out characteristic will be degraded by the capacitive load caused by the interconnections.

The power consumption associated with a logic element can be divided into two parts, defined as the steady state and switching transition power. The steady state power consumption remains relatively constant over the spectrum of operating conditions. The switching transition power will only be dissipated during the transition between the two logic states of the device. It is characterized by a power surge during each state transition, with a surge period that is a function of the switching time. This transition power will be dissipated because the circuit output is neither in the saturated nor cutoff states. This transitionary period will be set by the switching speed of the device, which is a function of line capacitance and, therefore, interconnection line lengths. The switching transition power dissipation will be a function of the duty cycle of the surge determined by the computer clock rate and circuit switching speed. The clock rate is an inherent characteristic of the computer, but the switching speed is partially a function of the interconnection capacitance. Therefore, power dissipation for a particular circuit will be increased as a function of clock rate and line capacitance.

The considerations discussed are not necessarily mutually exclusive, but inherently related. For example, a decrease in interconnection line capacitance will enhance circuit speed and fan-out, but increasing either of these parameters will reduce the advantage for the other parameter.

HARDWARE IMPLEMENTATION

The basic MEMA package is a flat pack measuring 1.0 in. x 0.75 in. x 0.06 in., with 24 or more leads. Within the flat pack, a number of monolithic integrated circuit and/or discrete component chips are bonded to an alumina substrate and interconnected by etched interconnections on the substrate. This circuit package contains an average of 20 monolithic integrated circuits or 15 discrete component circuits. The two most common flat packs have 24 or 36 leads, but a different number of leads are provided in many special purpose MEMAS.

The usual commercial packaging technique is to encase each integrated circuit chip in a separate flat pack which is mounted on a printed circuit board. The MEMA package introduces a level of simplification, where the bare integrated circuit chips are mounted directly onto ceramic substrates such that the substrate becomes the circuit board. The substrate is then sealed, forming an element with a functional complexity greater than standard printed circuit cards.

Although this package exhibits a higher level of functional capability, it still meets the throwaway requirements. This is due to the more compact packaging achievable by this technique and its economical advantages. Mounted on a submodule card, it offers the same functional capability normally attained by the assembly of a grouping of discrete component printed circuit cards.

A typical MEMA of the integrated circuit variety is shown in Fig. 1. A fabricated assembly with discrete components is pictured in Fig. 4.

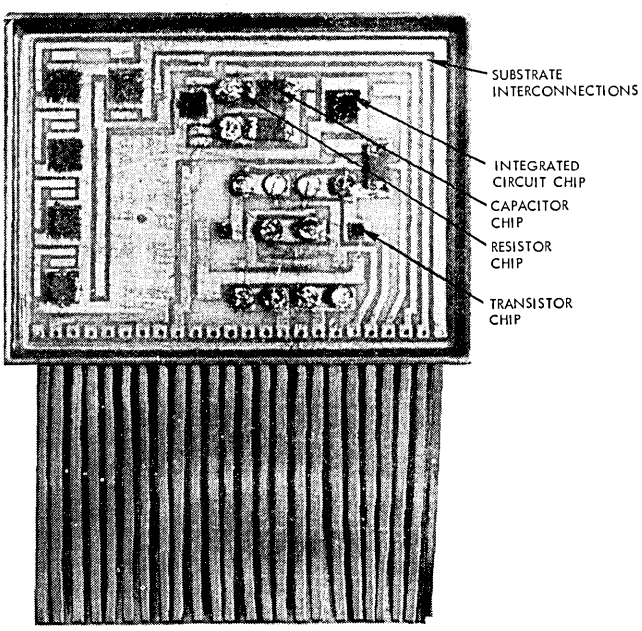

Fig. 4 Discrete component (MEMA).

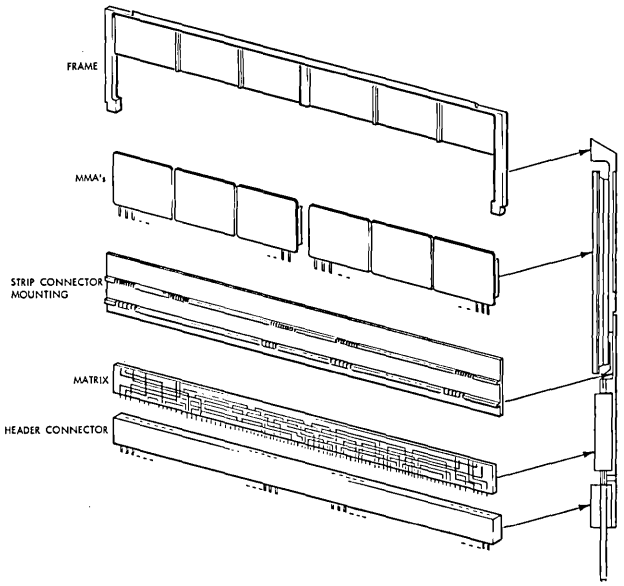

Fig. 5 Digital submodule construction.

The modular level of packaging is the primary level of field maintainability of the equipment. The equipment can be disassembled with simple mechanical operations down to the submodular level before bonding and soldering operations are required to assemble and disassemble the electronic equipment.

The submodule is composed of up to six MEMAS, a multilayer interconnection matrix, and a connector (Fig. 5). The frame provides structural support and heat conduction for cooling. The matrix provides for connections between the various MEMAS and to the connector. The multilayer interconnection matrix can contain in excess of 30 conduction layers, but with an average of approximately twenty layers. This matrix provides compact, reliable, and inexpensive interconnection. The interconnection matrix achieves these desirable characteristics by the simplicity of the concept, where each conduction layer is isolated from all other layers; thereby eliminating feedthroughs, plated through holes, and other relatively expensive and unreliable interconnection techniques. The matrix is implemented with each layer making all nodal connections for one or more circuit nodal points. Each node point is planar in nature, inherently isolated from all other matrix planes; thereby eliminating the need for electrical interconnections between layers. Electrical access to each layer is obtained by connection to the ribbon conductors that protrude from the nodal plane (Fig. 6). All interconnections to a nodal point are made on one side of the matrix while the connector is attached to corresponding node points on the opposite side of the matrix. The conductors that protrude from the matrix are designed to automatically line up with the corresponding MEMA and connector leads for semi-automatic assembly.

The various nodal conduction layers are isolated with layers of insulating film. Alternate layers of conduction plane and insulating film are built up, then bonded into a single unit, formed by the adhesion of

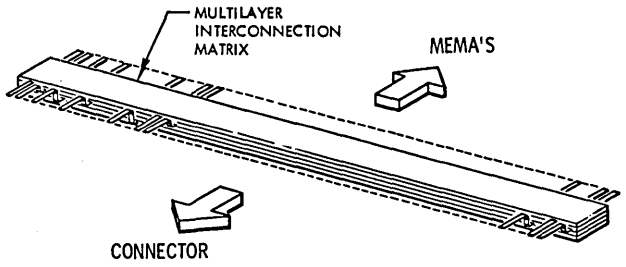

Fig. 6. Submodule interconnection matrix.

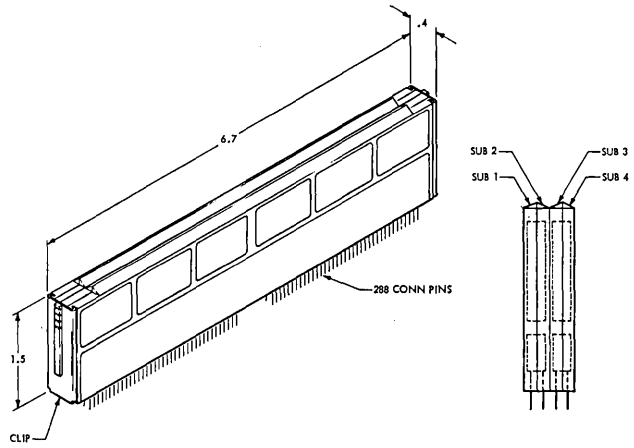

Fig. 7 Digital module.

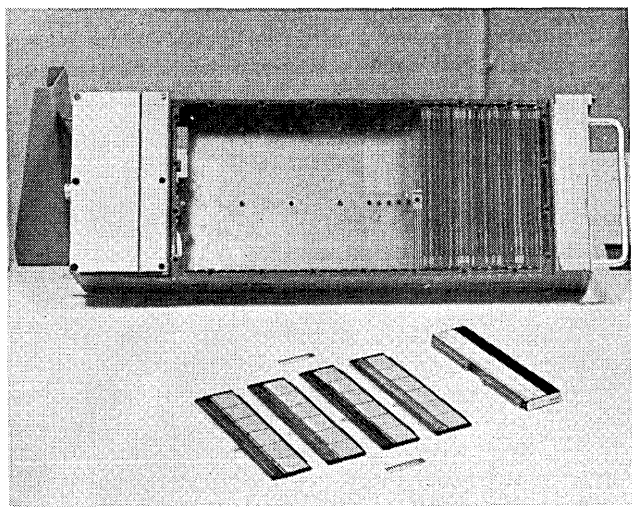

Fig. 8 Computer package.

the insulating film layers. The matrix also provides layers for the ground plane, voltage plane, and clock pulse plane, which are used to supply all MEMAS on a submodule.

The digital modules are implemented by physically clipping together four submodules (Fig. 7). The typical module will contain approximately 500 integrated circuits completely interconnected to form an extremely high level of functional complexity within a small volume. The volume of a module is approximately four cubic inches, resulting in a packaging density of approximately 200,000 integrated circuits per cubic foot. The interconnection between modules and computer package requirements will degrade this density to approximately 100,000 integrated circuits per cubic foot. A typical computer package is illustrated in Fig. 8, showing the modularity inherent in the dense packaging techniques.

CONCLUSION

High speed digital computers require special considerations for proper operation. The most important considerations are propagation delay, clock pulse skew, noise, crosstalk, and circuit performance. Each of these considerations can be significantly enhanced merely by reducing the physical size of the computer, with the resultant reduction in interconnection lengths.

Additional techniques can be implemented to enhance these considerations, but they have a significantly smaller impact than the physical size reduction technique. This physical size reduction technique is the predominating consideration because, as the physical size approaches an extremely small parameter, the other techniques become inconsequential.

The implementation of a high speed digital computer should start with packaging tradeoffs to determine the degree of miniaturization that is feasible based upon technical, economical, and risk considerations. The special techniques should then be implemented to the degree necessary to enhance operation to the required degree. If the packaging technique is "equal to the job," a significant amount of economy can be achieved with the minimization or elimination of the special techniques.

The MEMA packaging technique is technically and economically advantageous. It is in an advanced state of high production, resulting in a low risk packaging consideration. The implementation of computers with this technique will reduce the degree to which special techniques will be necessary to achieve the required degree of performance.

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Computer system requirements drawn from a broad spectrum of guidance and control applications are presented in this article. Based upon these requirements, design objectives such as adaptability and flexibility, and constraints of size, weight, power consumption, and reliability, a baseline aerospace computer system is derived.

SYSTEM DESIGN OF A GENERAL PURPOSE AEROSPACE COMPUTER

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The purpose of this article is to describe the rationale leading to the logical design of a computer that can be adapted to a wide range of aerospace applications. The computer represents an attempt to satisfy the diverse requirements of missile boost guidance, midcourse guidance, re-entry guidance, vehicle attitude control, and navigation, in one baseline design.

MISSION REQUIREMENTS

Most guidance and control computers in the past have been tailored for a specific mission even though they are called general purpose in the sense that a stored program is incorporated into the design. However, power and weight limitations have made the luxury of a truly general purpose computer organization too costly.

A primary objective is to design a computer system that can be adapted to a variety of aerospace missions, without changing the basic central processor organization, with a minimum of increased hardware. The requirements for typical aerospace computations have dictated the following systems requirements. The manner in which the requirements are satisfied is presented in this article.

1) The computations required for guidance, navigation, and experiment data processing have led to the assumption that the solution of algebraic problems should be performed as efficiently as possible. Algebraic is defined as those computations requiring sums of products, such as vector and matrix manipulations and integration. This does not mean that the standard data manipulation computations are neglected. It just means that special innovations should be incorporated into the design to facilitate the algebraic computation.

2) One of the more important results of the mission analyses was to realize that the input-output portion of the computer must change from mission to mission dependent upon the external hardware. However, the central processor structure need not change if a generalized scheme for communication between the central processor and the I/O is developed.

3) Certain input-output constraints are often present in aerospace applications. Some of these constraints include: gyros, accelerometers, and a real time clock. These dictate the necessity for servicing incremental inputs at a high peak rate.

4) Major functions of any aerospace computer are systems checkout and self-check. The computer systems should be designed so as to facilitate these checkout functions.

5) Low power consumption weight and volume are prime requisites. A main objective is to provide the smallest possible system consistent with the assumed mission.

6) The real-time nature of aerospace type computations dictates the necessity for a multi-level priority interrupt scheme. The number of levels is peculiar to the mission or mission phase.

7) As the complexity and volume of the computational load increases faster and faster, computers will be necessary to meet the requirements. It was decided to design the fastest possible machine, without pushing the state-of-the-art in integrated circuit technology or in memory development.

8) Since different missions might dictate different combinations of DRO and NDRO memories, the computer was structured to accept any of the present or future types of memory which include core, plated wire, thin film, or wired memory.

9) The desire for the smallest possible program

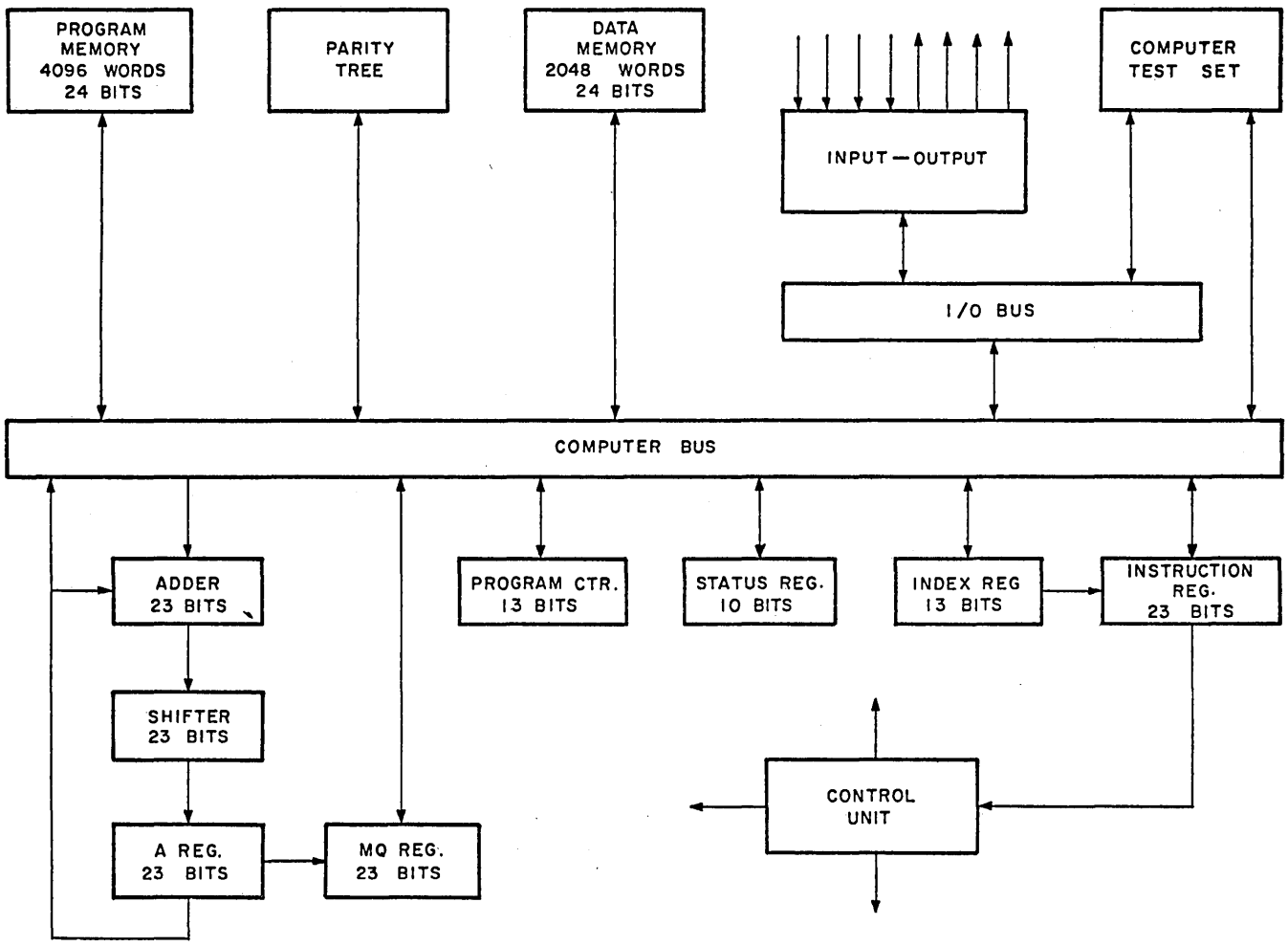


Fig. 1 Functional block diagram of computer.

necessary to perform a particular function led to the incorporation of a number of multi-function instructions such as, in one instruction, multiply, add, and store.

10) If more than one memory is used, the flexibility to execute instructions and read data from either memory is provided.

11) Since the computer has been designed before the specifics of its application were solidified, the structure considered expandability from the outset. The system can adapt to a wide variety of I/O interfaces and memory configurations. The memory size is readily expandable as mission requirements dictate. The structure is readily adaptable to multiprocessing and redundancy, where speed or increased reliability are required.

LOGICAL ORGANIZATION

Any design is, of necessity, a compromise between the various design features. In an aerospace computer, power, weight, and volume are traded off against computational power and flexibility. In any design process, one must first decide on the necessity of a feature and then the amount or degree of the feature which is necessary to meet the requirement.

The first task (qualitative in nature) is usually straightforward. The second task (quantitative in nature) presents a much more difficult problem with many points of argument. A fundamental aspect of the design philosophy was based upon the contention that a little bit of a feature is very worthwhile and quite often the differential gain achieved by increasing the amount of the feature is of much less importance. For example, one index register is almost a necessity for efficient address modification. However, the addition of two or even three more index registers does not improve the machine computational ability as much as the first index register.

In conjunction with the above philosophy, it was decided that a limitation in programming flexibility without limiting systems functional ability was a desirable way to save hardware. It is not necessary to provide three or four different ways to program a particular task. One method that is efficient will suffice.

During the mission investigations, it was decided that certain operations that are frequent in nature should be made automatic if the hardware cost was minimal. Such features include the double precision mode (used in conjunction with the normal instruction complement to increase speed in double precision software), unconditional indirect branch instruction

for returning from subroutines, and the concept of cycle stealing used to process incremental inputs.

Since the simpler the machine organization the smaller the hardware count, a minimum number of registers were used in the design. However, multifunctional registers do, of necessity, increase the control unit complexity.

The above design philosophy has been employed as far as practicable in the generation of the machine organization depicted in Fig. 1.

Most of the functional blocks communicate through the computer bus. The concept of a bus was employed for three main reasons. First, hardware is saved since all the inputs to each of the registers need not be OR'ed together at the input to the register. This is accomplished by the bus hardware. Second, even if direct connections between registers were provided, the advantages of simultaneous transfers between registers would not save substantial execution time. This is true because the sequences of most instructions is more sequential than parallel in nature. Third, the bus enables all registers to communicate and, thus, provides flexibility in instruction execution and computer expandability. It enables one parity tree to be used by two memories and facilitates the execution of instructions and acquisition of data from either memory.

The organization shown in Fig. 1 shows both a data memory and program memory. A number of reasons made this configuration desirable. The possibility of a requirement for a wired memory for program storage necessitates a two-memory system. The data memory would have to be electrically alterable. The present design provides for the possibility of one or two memories — either core, braid, plated wire, or thin film — without major redesign of the central processor and control unit. A two-memory system can be used to decrease instruction execution time by overlapping of the next instruction fetch with the present instruction. Also, the two-memory system provides a measure of redundancy in case one memory fails. In this sense, graceful degradation has been built into the system. A two-memory system also facilitates self-check. If the self-check program is stored redundantly, it can be executed even if one memory fails.

In order to efficiently fetch instructions and data from either memory or from the I/O, both memories and the addressable I/O registers have been made continuously addressable. The fact that the I/O can be addressed just like any memory register, in effect, makes every instruction requiring memory access an I/O instruction. The addressing scheme also allows instructions to be executed from I/O which greatly aids preflight checkout and enables the central processor to be debugged even if the memories are not operable.

The instruction format contains a 13-bit address to directly access all of memory and the I/O as well as a 3-bit second address to provide many of the important features of a two-address machine without the significant cost of a full two-address structure. The 3-bit address refers to an 8-word portion of memory and is referred to as the scratch pad. To eliminate data transfers between main memory and the scratch pad section, the scratch pad section is addressable by the 13-bit address as well as by the 3-bit address.

Mission requirements dictate that an efficient scheme for address modification should be incorporated into the design. In many computers, the index register serves functions other than address modification and, therefore, more than one index register is necessary. In this machine, the functions of program loop counting and the storage of subroutine return addresses are handled by scratch pad locations. The application of the scratch pad for these functions will be presented in the section entitled "Instruction Set."

The clock rate for the system was determined so as to allow an inter-register transfer in one clock time and a full 23-bit add in two clock times. If an add time was completed in one clock time, then either the clock rate would have to be low and instruction execution inefficient or an exorbitant amount of carry look-ahead logic would have to be employed. Experience indicates that at least six logic delays should be provided between clocked flip-flops. These gates include three delays in the control unit before a control pulse is generated and three delays for data to propagate. With a gate delay of 25 nsec, six gates give 150 nsec. Add to this a 25 nsec clock width and a 25 nsec safety factor and one obtains 200 nsec or a 5 MHz clock rate.

Parity has been incorporated into the design for error detection purposes. In order to fully exploit the properties of the parity check, it is desirable to have an odd parity on an odd number of bits. This will detect not only all single errors, but also failures where all the bits in a word including the parity bit become all "0" or all "1." An odd number of information bits plus one parity bit requires an even number of bits for a memory word. Parity is generated whenever a word is written into memory and is checked whenever a word is read out of memory.

A number of factors enter into the determination of the word length. The data word length is dictated by the accuracy requirements of the mission under consideration. To maximize program speed, it was determined that the majority of the arithmetic operations should be single precision. Double precision arithmetic should be the exception rather than the rule. No more than a few of the arithmetic operations should be double precision. Investigations of typical aerospace computations showed a 24-bit memory word, 22 bits + sign + parity, is sufficient.

The program memory word length is determined by the amount of information needed to specify an instruction as well as the extent of direct addressing desired. Since the number of bits in an instruction word was within 2 bits of the data word, it was also decided to make the program memory word 24 bits, 23 + parity.

A number of advantages are apparent when the data and instruction word lengths are the same. First, data and instructions can be executed out of either memory without introducing problems because of different word lengths. Second, with a 23-bit instruction, direct addressing in the baseline computer can be provided for both memories and the I/O without reverting to a banking scheme. Memory expansion is possible through a unique banking scheme that is discussed in the memory section.

The program counter shown in Fig. 1 is on the computer bus. This simplifies the problem of executing instructions out of either memory or the I/O. If the program counter were made part of the program memory address register, accessing of data from the program memory would require storage of the program counter in a special register. As will be explained later, the program counter being on the bus also simplifies the priority interrupt sequence.

The instruction register is used to hold the instruction during execution and frees the memory buffer register so that memory overlap can be employed. In the normal operating mode with data out of data memory and the instructions out of program memory, the fetch of the next instruction is overlapped with the execution of the previous instruction, thus saving 2 μsec on most instructions.

Incorporated into any computer structure are a number of flip-flops which must be either set or reset by the programmer as well as by certain automatic conditions. Such flip-flops include: the parity flip-flop, overflow flip-flop, double precision flip-flop, inhibit interrupts, inhibit cycle stealing, and others. All these flip-flops comprise the "status registers." The usefulness of one addressable register instead of individually addressable flip-flops will become clear in the discussion of the instruction repertoire and the interrupt scheme.

INSTRUCTIONS

Addressing Structure

In choosing the computer addressing structure, studies were conducted that demonstrated the computational advantages of a double address structure over a single address structure. In typical problems, a double address format is likely to save up to 30% in program space and 10% in execution time over a comparable single address format. A triple address structure was rejected as providing only marginal improvement in program size and execution speed over double address at considerable hardware cost. A list processing structure was rejected for similar reasons.

A double address machine, however, is more costly to implement than a single address machine. Investigation into the functions that are likely to be performed by an aerospace computer reveals those features of a double address structure that actually contribute most of the savings in program space and execution time.

There are several forms that double address instructions can take, and numerous repertoires can be chosen using groups of instructions of each form. It was hypothesized that a repertoire that achieves nearly the 30%/10% savings could be implemented with only slightly more hardware than would be required by a single address machine. A repertoire having the following two features (along with tailored instructions) satisfies these requirements.

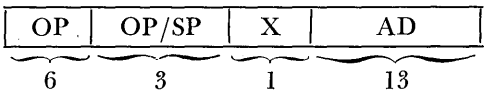
1. The existence of an "and store" option on each arithmetic and logic instruction which involves memory and the A register. This effectively eliminates the store instruction, that is so consistently required for saving temporary values. Execution time is saved not only by the elimination of an instruction, but also by the overlapping of part of the data memory cycle (for storing) with the actual operation that simultaneously takes place in the arithmetic subsystem.

2. The utilization of a "small" second address that refers to a section of memory (designated as scratch pad). Due to the way in which the scratch pad is used, only a relatively few (less than 8) locations are simultaneously employed in a typical computation; hence, only 3 bits in the instruction word are needed for addressing. In order to properly take advantage of scratch pad, it is important that the main address in the instruction can access the scratch pad section as well as the main section of memory. Hence, if a parameter is stored in scratch pad, it need not be moved to be available for use by successive instructions.

An inspection of the complete instruction set reveals that most two-address instructions have one-address analogs. This relationship helps to keep control hardware to a minimum.

Instruction Set

The complete instruction set for a typical guidance and control computer is given in Table 1. The basic format for all instructions is shown below:



The AD field specifies a location in data memory, program memory, or I/O where data is taken, to where data is stored, to where the program will branch. The X field indicates the presence or absence of indexing. The OP (Operation) field specifies all two-address instructions *or* aids in specifying one-address instructions. If a two-address instruction is decoded by the OP field, the OP/SP field indicates the required scratch pad location. If a one-address instruction is sensed by the OP field, the OP/SP field provides the final decoding to completely specify the instruction.

One index register is designed into the prototype computer. Looping is accomplished by operating on a scratch pad location in the accumulator (DTB instruction); returns from subroutines and interrupts are achieved by using the Unconditional Branch Indirect (UCBI) instruction. Hence, the index register is used strictly for address modification. N index registers require many more than N times the hardware of one index register (additional bits in the instruction word, switching logic). It was decided that the additional hardware was not justified for the increased programming flexibility.

Even though only one index register is used, others may be simulated by storing the index register in memory and loading a new data into the index register. More than one index register adds hardware because selection logic and switching logic must be provided in addition to the registers themselves.

TABLE 1

INSTRUCTION SET

No.	Instruction	Mnemonic	Execution Time (μS)
1	Add	ADD	2.6
2	Add and Store	ADDS	4.6
3	Subtract	SUB	2.6
4	Subtract and Store	SUBS	4.6
5	Logical And	AND	2.6
6	Logical And and Store	ANDS	4.6
7	Logical Exclusive Or	XOR	2.6
8	Logical Exclusive Or And Store	XORS	4.6
→ 9	Update Add	UADD	3.4
10	Update Subtract	USUB	3.4
11	Update Logical And	UAND	3.4
12	Update Logical Exclusive Or	UXOR	3.4
13	Load Accumulator	LD	2.6
14	Load Absolute Value	LDABS	2.6
15	Load Index Register	LX	2.6
16	Load M-Q Register	LMQ	2.6
17	Store Accumulator	STO	2.6
18	Store Index Register	STX	2.6
19	Store M-Q Register	STMQ	2.6
20	Multiply	MPY	11.4
21	Multiply And Round	MPYR	11.4
22	Multiply And Store	MPYS	13.0
23	Multiply, Round, And Store	MPYSR	13.0
→24	Multiply And Accumulate	MAC	13.8
25	Multiply, Round, And Accumulate	MACR	13.8
26	Square	SQR	11.4
27	Square And Round	SQRR	11.4
28	Square And Store	SQRS	13.0
29	Square, Round And Store	SQRSR	13.0
→30	Square And Accumulate	SAC	13.8
31	Square, Round And Accumulate	SACR	13.8
32	Divide	DIV	11.4
33	Divide And Store	DIVS	13.0
34	Branch On Negative Accumulator	BM	2.8
35	Branch On Zero Accumulator	BZ	2.8
36	Branch On Non-Zero Accumulator	BNZ	2.8
37	Branch On Positive Accumulator	BP	2.8
38	Branch On No Overflow	BNOV	2.8
39	Branch On Accumulator ODD	BODD	2.8
40	Branch On Accumulator EVEN	BEV	2.8
41	Branch On I/O Conditions 1-8	BIO1	2.8
42	Branch On I/O Conditions 9-16	BIO2	2.8
43	Unconditional Branch	UCB	2.8
44	Store Program Counter And Branch	SCB	4.6
45	Unconditional Branch (Indirect)	UCBI	4.6
46	Unconditional Branch (Indirect) For Interrupt Return	UCBII	4.6
47	Decrement, Test, And Branch	DTB	5.4
48	Decrement, Test, Branch, And Increment Index Register	DTBX	5.4
49	Shift Left Arithmetic	SLA	2.6 + .2N*
50	Shift Left Arithmetic And Round	SLAR	2.6 + .2N
51	Shift Left Arithmetic And Store	SLAS	4.6 + .2N
52	Shift Left Arithmetic, Round And Store	SLASR	4.6 + .2N
53	Shift Right Arithmetic	SRA	2.6 + .2N
54	Shift Right Arithmetic And Round	SRAR	2.6 + .2N
55	Shift Right Arithmetic And Store	SRAS	4.6 + .2N
56	Shift Right Arithmetic, Round And Store	SRASR	4.6 + .2N
57	Shift Left Logical	SLL	2.6 + .2N
58	Shift Right Logical	SRL	2.6 + .2N
59	Round	RND	2.6
60	Round And Store	RNDS	4.6
61	Set Status Register	SET	2.8
62	Reset Status Register	RESET	2.8
63	Increment Index Register	INC	2.8

*N = Number of Shifts

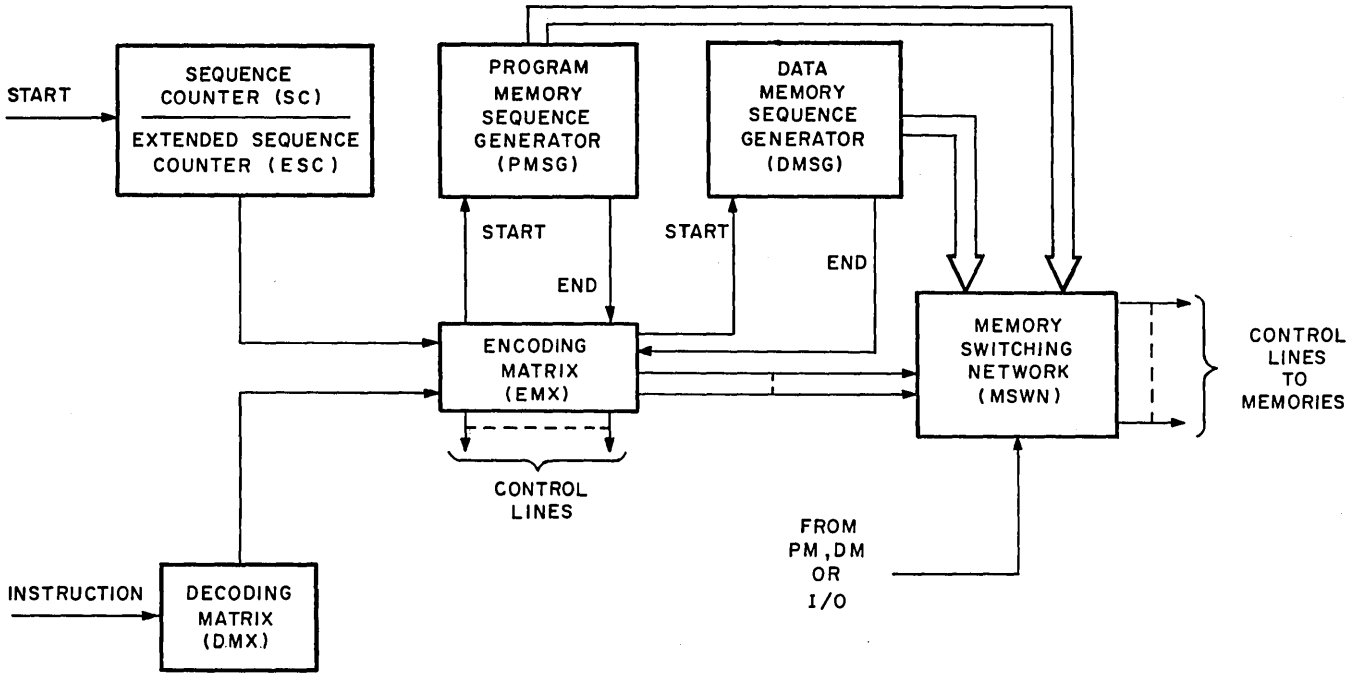


Fig. 2 Control unit block diagram.

Every instruction in the repertoire may have the address field modified by indexing. Indeed, it costs hardware to divide instructions into indexable and non-indexable groups. The index register is a 13-bit register which can be loaded, unloaded, or incremented. When indicated, the 13-bit index register will be logically OR'ed with the 13-bit address field of the instruction. Conventional index registers usually add the index register to the instruction address field. The OR'ing does not seem to pose a disadvantage over adding. There is, however, a significant savings in hardware as well as execution time.

SUBSYSTEM DESIGNS

Structure of Control Unit

The control unit provides timing and gating pulses to registers, the arithmetic unit, memories, and I/O for the execution of all instruction sequences, cycle stealing, and interrupt sequences. A block diagram of the control unit is shown in Fig. 2.

The Sequence Counter (SC) and Extended Sequence Counter (ESC) provide basic timing pulses for instruction. The Decoding Matrix (DMX) decodes the OP field to yield individual instructions and groups of instructions. The Memory Switching Network (MSWN) is discussed in the section entitled "Structure of Memory Subsystem." The Encoding Matrix (EMX) combines basic timing pulses from the SC and ESC with instruction groups from the DMX providing outputs which are in the form of control line Σ(INGP) · (TP) · (COND),

where INGP = instruction or group of instructions
TP = timing pulse
COND = condition (which may be = 1)

The section on memory subsystems describes the advantages of employing separate memory sequence generators with regard to adaptability and flexibility. In addition, considerable hardware savings are realized by generating timing and gating associated with memories in a logic block apart from the main sequence counter.

Consider a Clear/Write memory cycle. This may require (for example) six specific control pulses each having a fixed time duration and in a fixed prescribed order (for example, initiate memory pulse, a memory mode line, a data-to-memory strobe, end pulse, etc.). A Clear/Write cycle is required at different times during different instructions and during different cycle steals. Suppose there are four different starting points for the Clear/Write cycle; this would require 4 x 6 = 24 Boolean terms associated with memory during a Clear/Write cycle. However, if memory timing is developed separately upon the application of a start pulse, this start pulse requires only four Boolean terms.

There is a trade-off between the number of Boolean terms saved and the cost of a separate sequence generator, but for this computer, separate generators required the least hardware.

The DMSG is a feedback shift register capable of providing timing for Read/Restore, Clear/Write and Read/Modify/Write cycles upon being properly initiated.

Structure of Memory Subsystem

Application

A key tenet in the design of the computer was to allow for the application over a wide range of guidance and navigation type problems employing different memory structures. To demonstrate this capability, two memories appear in the Central Processor for the prototype computer. The memories are configured symmetrically (Fig. 3).

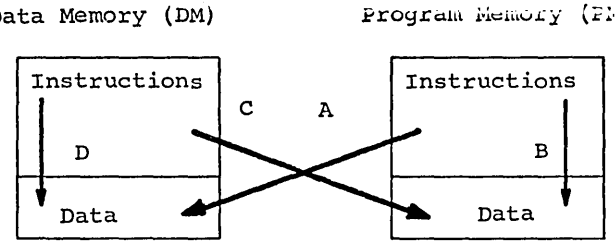


Fig. 3 Symmetrical configuration of memories.

The two-memory structure:

(1) Achieves speed (by means of memory overlap)

(2) Achieves redundancy (by double data store or degraded operation with one memory)

(3) Is required for applications that have wired mission programs

(4) Is adaptable to single memory applications

The I/O Subsystem is assumed to be structured like one of the memories in the CPU. This accomplishes a three-way symmetry that allows instructions and/or data to be placed in I/O, PM, and/or DM. The resultant flexibility of operating modes is shown in Table 2.

TABLE 2

MEMORY OPERATING MODES

Instr Data	PM	DM	I/O
PM	DM failure; for one memory application	Normal mode	Checkout; telemetered instructions; multiprocessing systems
DM	Normal mode	PM failure; for one memory application	Checkout; telemetered instructions. Multiprocessing system
I/O	Checkout; telemetry; navigation inputs I/O instructions	Checkout, telemetry, navigation inputs I/O instruction	Checkout; telemetered program; PM and DM Failure; Multiprocessing System

Memory Switching Network

In order to exploit the symmetrical memory arrangement, a memory switching network is employed. In this manner, if an instruction is to be fetched from PM, the control lines for instruction fetch are switched to PM; if data for an instruction is located in I/O, the control lines for data are switched to I/O.

Memory Scratch Pad

The actual location of the scratch pad memory is dictated by the following rules. In two-address arithmetic type instructions (e.g., ADDS, MAC), the bit pattern of the AD field chooses the memory for SP (as well as for AD). In two-address instructions where the AD field does not refer to data (e.g., SHFTS, SCB, DTB) two flip-flops in the status register choose the memory for SP. This rule allows SP to be located in PM, DM, or I/O. The most flexible rule would allow two status register bits to specify the location of SP for every instruction. This rule, however, would greatly complicate the end sequences, and memory switching network. The rule that was chosen affords good flexibility at little hardware costs.

When interrupt programs are required for a mission, each interrupt program is assigned a separate group of scratch pad locations. This is accomplished by a scratch pad bank register which is controlled by the I/O and is used in formatting the scratch pad address when required in a control sequence.

The use of an integrated circuit (IC) scratch pad was ruled out for three reasons: (1) The two microsecond memories used in the prototype computer were considered fast enough to obviate the need for the IC's (main advantage being access speed). (2) Often, time is wasted simply transferring data between IC scratch pad and memory (as during interrupts). (3) Hardware and power considerations resulting from a third memory which requires added timing and control.

Banking

The uniqueness of the banking scheme lies in the fact that independent bank bits are provided for banking of data and instructions. The instruction bank bits are considered part of the PC. They are left adjusted and wired in the carry logic so that programs which are contiguous over adjacent banks are executed automatically. The data bank bits are considered part of the IR. They are left adjusted, can be indexed, and are transferred to the bus with the address field of the IR during an instruction register transfer subcommand.

The data and instruction bank bits are changed under program control by means of the Set and Reset instructions. In this sense the bank bits are considered part of the status register.

During interrupts, the bank bits and the critical status bits are automatically stored away during the store counter and branch (SCB) instruction. Since the I/O, DM, and PM are continuously addressable, any additional memory can be distributed arbitrarily between the I/O, DM, and PM as long as the memory addressing logic is changed.

Memory Sequence Generator

Two separate Memory Sequence Generators are incorporated in the computer. They generate the timing and gating that are required by the specific memories and provide pulses to the Control Unit signifying the completion of a memory cycle.

It follows that memory timing cannot be completely independent of the main control sequences, but the utilization of separate memory sequence generators has provided a modular situation in which a variety of memories may be integrated within the CPU necessitating only minor (if any) design changes. The section concerning the structure of the control unit highlights efficiencies that are realized by employing separate memory sequence generators.

Structure of the Arithmetic Subsystem

The arithmetic subsystem consists of the adder, shifter, A register (accumulator), and MQ register. It consists of 22 bits plus sign and performs 2's complement arithmetic. By appropriate control of the various sections of the arithmetic subsystems, the operations of add, subtract, multiply, divide, logical AND, and exclusive OR can be performed.

The series configuration of the adder and shifter enables the add/shift cycle present in the multiply and divide algorithms to be executed in 400 nsec, thus, achieving a fast multiply and divide instruction. Simple algorithms were employed to save hardware. The multiply algorithm does not shift over 0's since the worst case multiply time would not be affected. The non-restoring divide algorithm does not utilize quotient or remainder corrections and thus, saves substantial hardware. The standard quotient correction only redistributes the error but does not change the maximum value. If the exact remainder is desired, it can be achieved by software means.

The logic for the carry look-ahead circuits is contained on two separate modules so that if an expansion in word length is desired without changing speed, only the carry modules need to be redesigned.

As previously mentioned, no double precision instructions are incorporated into the design, since most arithmetic operations are assumed to be single precision. However, a small amount of special hardware has been incorporated into the computer to make double precision software as simple as possible. This hardware includes a double precision flip-flop (DP), in the status register, used to put the computer in the double precision mode. This flip-flop can be set by the "SET" instruction. It is reset automatically after each add or subtract operation.

Another flip-flop used to facilitate double precision operations is the carry flip-flop (CFF), which is set whenever a carry out of bit 22 occurs. If no carry occurs, it is reset.

If DP = 1 and CFF = 1, then during the next add or subtract operation an extra one will be added into the adder in the case of an add instruction or subtracted in the case of a subtract instruction. That is, the carry from either addition or subtraction of the least significant parts of the double precision numbers is automatically saved in CFF and taken care of during the addition or subtraction of the most significant parts of the double precision numbers.

Cycle Stealing and Interrupts

Real time considerations and the nature of typical accelerometer inputs indicate the desirability of employing the cycle stealing mode. At the end of each instruction, the cycle stealing flip-flop will be tested. If this flip-flop is set, one of a number of automatic hardware sequences will be executed. The sequence will either load a particular location in memory, unload a location in memory, or cause a memory location to be incremented or decremented. The memory location will be specified by the I/O. The cycle stealing sequences involving the loading or unloading of memory require 2.2 μsec. Those involving the incrementation or decrementation of a memory location require 3.0 μsec.

Block loads and unloads of the computer memory may be achieved by cycle stealing. This is accomplished by performing any cycle steals in succession and not executing the next instruction until all the cycle stealing is finished.

Cycle stealing can also be used to put the computer in a temporary pause mode. This is accomplished by a "Do Nothing" cycle steal in which the memories are not exercised. This will save substantial power.

Since the cycle stealing process may employ the Arithmetic Subsystem, the A register is temporarily stored in the IR and restored at the end of the cycle.

Interrupts initiated by the I/O unit cause the present program to be suspended and a new program to be executed. At the end of each instruction, if the cycle stealing flip-flop is not set, the interrupt flip-flop will be tested. If it is in the logical "1" state, the address of the interrupt program, which is generated by the I/O unit, will be gated into the memory address register via the bus. The instruction in the specified memory address will then be read and executed. This instruction must be a store counter and branch (SCB) instruction. The program counter (which contains the return address to be used by the interrupt program) is stored away in an SP location, and the program counter is loaded by the Address field of the SCB instruction. This address field is the starting location of the interrupt. The unconditional branch indirect (UCBI) instruction provides means for returning to the main program.

This type of program interrupt facility allows for multiple level interrupts. Any priority problems are resolved by logic in the I/O unit. The prototype design allows for 8 levels of interrupts.

Input-Output

The Input-Output section is effectively an additional processor attached to the computer bus. It normally contains an address register, data register, serial-to-parallel converters, parallel-to-serial converters, and self-contained counters and control logic. Depending upon the application, it may also contain A/D and D/A buffers and converters, multiplexers, and possibly arithmetic and data conversion capability. For other applications, it may also contain a memory subsystem which is time-shared with one or more additional central processors.

These input-output capabilities are controlled from the central processor by instructions which address the I/O sections as if they were part of the data or program memories. This allows the full complement of instructions to be used as I/O instructions. The ability to execute instructions out of I/O greatly facilitates computer checkout, especially when either data memory or program memory is not functioning.

Elaborate self-test and diagnosis programs for both the computer and the system, it is to be used in, can be executed without consuming the memory capacity of the central processor. For example, with appropriate buffering circuitry, it would be possible to do all prelaunch checkout of a guidance system via a memory system external to the vehicle itself, thus, simplifying and minimizing the flyable hardware.

In order to keep the central processor design essentially independent of the system application, the selection and priority control for cycle stealing and program interrupts was placed within the I/O section. The control sequences are, of course, part of the central processor; however, the addresses to specify data locations (for either data storage or fetches) or transfers addresses are supplied by the I/O section. This technique has been found to provide a great degree of design flexibility from application to application without requiring redesign of the central processor.

CONCLUSIONS

The detailed logic design for the computer system described in this article has been completed, and an engineering model fabricated and tested. The adaptability of this design has been proven by a number of proposed modifications for various customer applications. In addition to performance modifications such as increased word length, multiple index registers, special instructions, and input-output features, it has been possible to update the logic with available MSI devices in order to reduce size and mechanical complexity of the computer.

The airborne computer has demonstrated its system performance capability in a strapdown guidance system application. Complete system sofeware has been developed and verified first on a General Purpose Computer Simulator and more recently in actual operation in the strapdown guidance system.

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CIRCLE NO. 25 ON INQUIRY CARD

An automatic testing philosophy which has resulted in the development of a Controller/Programmer/Evaluator (CPE) to serve as the nucleus of an automatic test station is described. The CPE contains all of the circuitry necessary for program control, test point selection and measurement of the electrical response of the unit under test.

AN ECONOMICAL AND VERSATILE SOLUTION TO AUTOMATIC TESTING REQUIREMENTS

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The need for a portable low cost automatic test set for testing large complicated electronic systems, has resulted in the design and development of a unit, which we have called the Controller/Programmer/Evaluator (CPE). This general purpose unit occupies less than 3.5 cubic feet of space and fulfills the bulk of automatic test equipment requirements.

It contains up to 1,000 test points, 1,000 stimuli control points, 100 reference points, and 10 ground points. Measurements can be made at the rate of 3 to 4 per second with accuracies better than 0.1 percent.

Compact size and versatility allows the CPE to be readily adaptable to the role of shop and flight-line support equipment. Due to its small size the unit, including appropriate adapters, can be easily moved about within the maintenance shops or taken to the aircraft to troubleshoot individual subsystems.

The CPE contains the necessary logic circuitry to program specific tests automatically from punched tape, manual keyboard, or a digital computer. It also contains test point selection and measurement circuitry. Present models utilize miniature relays for test points; however, solid-state switches are available where weight savings or signal characteristics warrant their use. (As an example, it might be used as an onboard test system.) The criteria for the measurement capability implemented in the test set was based on general live testing requirements of most avionic subsystems. It was not intended to incorporate measurement circuitry to meet every conceivable need; only those measurements which were needed repeatedly to evaluate the majority of electronic subsystems were included.

In order to circumvent restrictions on testing most aerospace electronic systems, provisions were made to include specialized measurement devices and stimuli (which are also more often specialized) as ancillary equipment or within a special adapter. The importance of this approach can be recognized by the time and cost that can be saved in not having to design and develop the programmer/controller, test point selection and measurement circuitry for every new application or test requirement.

To construct an automatic test system, the standard, CPE is coupled with an adapter which will mate with the Unit Under Test (UUT). The adapter is required in the design of nearly all automatic test systems. The function and use of adapters are discussed in detail, later.

The CPE utilizes digital techniques for control, evaluation, and comparison. Extensive use of integrated circuits (modular packaged by a proprietary method) increases reliability and reduces cost, size, and weight. The evaluation circuitry employs a noise insensitive analog-to-digital converter.

The programming format is convenient and English language oriented. The program code is suitable for tape preparation and printing by a standard Flexowriter. The test set uses a bidirectional line tape reader, which reads 8-level paper or mylar tape at the rate of 100 lines per second, but is not limited to this input device.

Additional features are provided to enhance the test operator's role and improve the maintenance task. These include provisions for recording test results on a printer and control of microfilm information re-

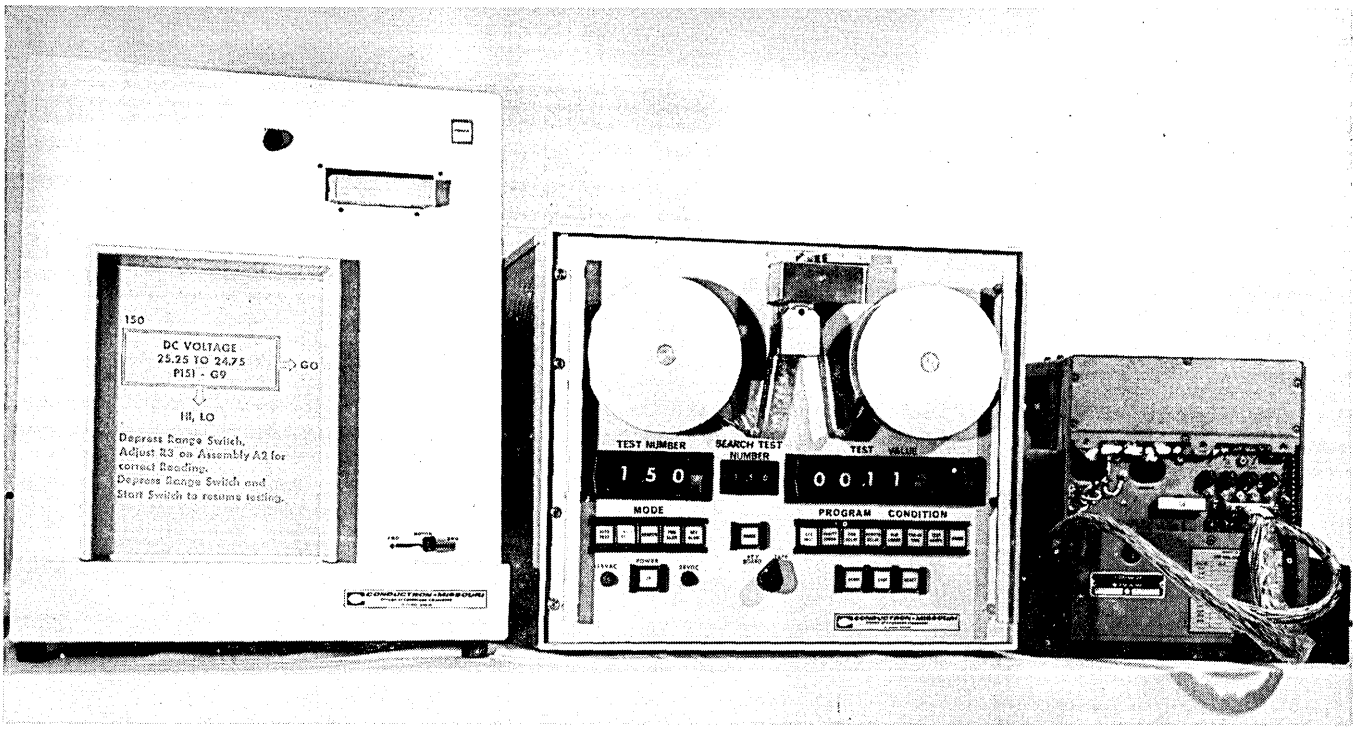

Fig. 1 Automatic test station.

trieval systems to circumvent the use of numerous technical orders, technical manuals and handbooks frequently confronted in the maintenance task.

CPE APPLICATIONS

The initial considerations in the design of any automatic test system must include the operator and his role in the testing activity. Some proponents of automatic testing would lead one to believe that typical automatic test equipment requires little or no operator participation except for turn ON and turn OFF, and connecting and disconnecting the unit under test (UUT). Such equipment may be a reality someday, but until software preparation technology is refined and the UUT's are designed for 100 percent automatic testing (i.e., sufficient and proper test points, elimination of the requirement for analyzing complex waveforms, etc.), the operator is a necessary and important element required to "close the loop". He must be able to make intelligent judgments in those situations that may occur beyond the scope of the programmer's anticipation or when sufficient test points are not available. He must also visually and mentally evaluate the integrity of the unusual wave shapes on a scope, etc.

A notable and significant feature is the use of an automatic microfilm information display system which readily provides maintenance information. Such a microfilm information display system, when used with the CPE, projects, for the viewer, written instructions and/or photographs, schematics, etc. In operation, the CPE sends out a code representative of the test number. If the test program stops as the result of a programmed stop for operator participation, or as a result of a NO-GO reading, a signal is sent to the display unit. This signal causes the film-image, identical to the test number code on which testing stopped, to be displayed.

The following information can be rapidly displayed to the test operator: cabling instructions, manual settings associated with the UUT (dial and switch settings), readout information (photos of CRT and indicator displays for the test operator to compare with actual equipment), probing instructions (where test points must be probed manually), adjustment and alignment instructions, photos of hardware and component locations, repair instructions, assembly and disassembly insructions and subroutine test instructions.

A paper copy of repair instructions can be obtained with a copier attachment to provide a maintenance record, requisition parts, or supplement repair work orders.

Such a Display System is an important new adjunct to the test system because it frees the operator's hands and saves him time locating the specific data he might require. Fig. 1 shows one such automatic display unit connected to the controller/programmer/evaluator. This particular display does not show the dry copier attached.

A printer is also deemed a valuable asset to the maintenance task. Therefore, output provisions were incorporated in the CPE for using a printer when a record of the test results is required.

A summary of a trade-off analysis of a manual test bench versus the CPE automatic test set approach is provided in Table 1. This analysis shows the value and time that can be realized by automatic testing. It is obvious from this table that utilization of an automatic test system offers very definite advantages over the manual test bench.

TABLE I

Trade-Off Analysis

Amplifier-Control Assy. (AN/ASA-32 Autopilot)

	MANUAL TEST BENCH	CPE WITH ADAPTER
TEST TIME	≃2 Hours	≃5 Minutes
NUMBER OF TESTS	≃200	≃300
ADVANTAGES AND DISADVANTAGES	1. Not a complete test (would take 6 hours longer). 2. Static test only. 3. Phase relationships and measurements) require a scope plus 1 additional hour of test time. 4. Requires high skill level technicians. 5. Accuracy and repeatability of tests are coupled with human error.	1. A complete test. 2. Static and dynamic tests. 3. Phase relationships and measurements are made automatically. 4. Can be operated by minimum skill level technician. 5. Tests are repeatable with same accuracy. 6. Accessory printer can record test results and values automatically. 7. Accessory Automatic Data Retrieval and Display can eliminate Handbook or T.O. 8. Use of the CPE means not using some conventional test benches already in inventory.

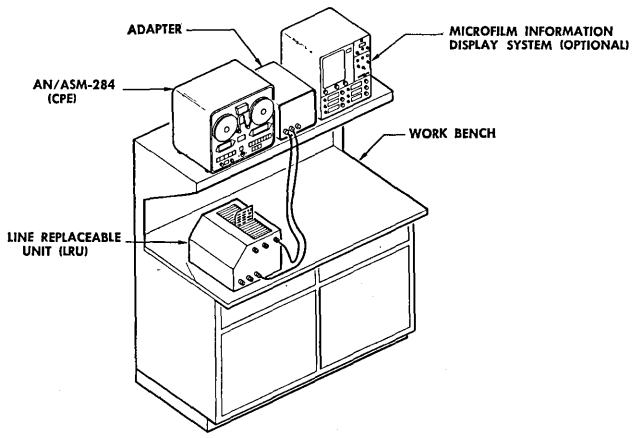

Fig. 2 Typical field/depot test set up.

A typical application of the CPE is shown in Fig. 2.

ADAPTER CONSIDERATIONS

The subject of an "Adapter" warrants attention because, in general, it represents an "unknown" for those not familiar with the controller/programmer/evaluator (CPE) or the unit under test (UUT). The following discussion will enable the reader to evaluate the value and purpose of the adapter as it applies to any specific testing task.

The first item of concern is that the CPE supplies no stimuli or simulated loads to the UUT. It supplies controlling commands to the special purpose adapter to "call-up" the desired loads and stimuli as required for the tests being performed.

The decision not to include general purpose stimuli or loads in the CPE design was based upon realistically simplifying the complex and costly number of stimuli and loads required for a large number of yet undefined UUT's. Certainly, stimuli and loads could be categorized into a few general types that would encompass a majority of the requirements. However, to cover the spectrum of only DC voltages is a costly undertaking considering variations such as accuracy, range, resolution, and grounding problems. If two DC stimuli are required simultaneously, the hardware is doubled. A test system can soon grow to unreliable and enormous proportions when considering all possible commonly used stimuli such as frequencies, AC voltages, current limited AC and DC voltages, pulses of various amplitudes and widths, modulated frequencies, servo error signals, etc. This situation is further complicated by adding both resistive and complex loads. No matter how well the designer of the general purpose adapter second guesses future require-

ments, he will not include all that will ultimately be desired or even required. Experience has shown that even on large test complexes with a variety of load simulators and stimuli building blocks, the UUT, in most cases, cannot be plugged-in directly. It still requires a special purpose adapter to mate with the general purpose adapter or test system. The question then arises, "Why have a general purpose adapter at all?" For this basic reason, it is recommended that no general purpose stimuli or loads be provided, but rather that such functions be provided on an "as required" basis in the special purpose adapters.

The adapters which mate the CPE to the UUT usually contain some or all of the following functional capabilities.

1. Necessary cabling interface between UUT and the CPE.
2. Simulated loads.
3. Stimuli to exercise the UUT and switching, which is controlled by the CPE, to select the stimuli level and route it to the UUT.
4. Mounting provision for the UUT.
5. Test jacks for standard test equipment (oscilloscope, waveform analyzer, etc.) to evaluate unusual wave shapes.*

Experience has shown that the adapter design is a straightforward step-by-step process. Small segments of the circuitry are all independent of each other; therefore, "race" conditions or sequencing problems are minimized. Most wiring is pin to pin or straight through from the UUT connector directly to the CPE. The electrical components are common off-the-shelf items readily available. As an example, the adapter for a rather complex UUT (the autopilot control amplifier for the Phantom F-4 which contains six connectors and 400 terminations) contains the following components:

ITEM	QUANTITY
1) Resistors	36
2) Potentiometers	3
3) Relays	48
4) Transformers	6
5) Connectors	13
6) Diodes (arc suppression)	47

Utilizing a different adapter for each UUT provides the designer with additional latitude and the user with improved performance and reliability from that possible with a general purpose testing system. Some of these benefits are as follows:

1. The test capability is not limited to specific stimuli or loads available in general purpose adapters. In some cases, the programmer would be forced to compromise the test. This results in a sacrifice of test performance or test validity. The special purpose adapter allows the designer to select the exact stimuli and loads required to optimize the test, and in some cases, ease the test program design tasks.
2. Interface and compatibility problems are minimized. The stimuli and loads are controlled by simple ground commands from the CPE. The signals for evaluation are merely routed straight through to the CPE.
3. The adapter is physically close to the UUT. This eliminates excessive cable runs and the resultant signal deterioration and noise pick-up.
4. The user may elect to design and build the adapters "in-house" or go out for competitive bids with a minimum of technical coordination required.
5. If design changes in the UUT occur which necessitate adapter changes, these changes can be accomplished without affecting any other adapter or the CPE.
6. The holding fixture and cabling interface can be incorporated as part of the adapter, thereby reducing costs. The resulting adapter will require approximately the same storage space as the holding fixture and interconnection cables.
7. The adapters may be fabricated or purchased as the requirement arises. Therefore, capital expenditure need not occur until the actual requirement arises.
8. The designer still maintains the option of designing an adapter that could service two or more UUT's that are functionally similar. He can, at his discretion, consolidate stimuli and loads to reduce hardware costs. An example might be the use of a single adapter to accommodate two different variations or dash numbers of the same basic UUT.
9. For systems on which manual testing procedures already exist, the adapter can be designed to duplicate the manual test. Therefore, time proven procedures and established tolerances can be directly converted to an automatic sequence. A general purpose adapter would not have this flexibility and the result would be a costlier software program, a delay in becoming operational, and less confidence in the test results.

The programmable adapter provides the interface necessary to allow the CPE to "talk to" the associated UUT. The programmable adapter is a special purpose device designed for the specific test requirements of the UUT. This allows the optimum in testing, with a minimum of programming and design time.

TECHNICAL DISCUSSION

The controller/programmer/evaluator, as the nucleus of an automatic test station, contains all of the circuitry necessary for program control, test point selec-

** As an example, programmable waveform analyzers used in large scale general purpose test systems are still subsidized by the more trustworthy oscilloscope.*

tion, and measurement of the electrical response of the unit under test. Control is accomplished by intelligence contained on perforated tape. The CPE automatically performs analog measurements on a GO/NO-GO basis and has the capability to enter subroutines for detailed diagnostic testing. The evaluation circuitry is a noise-insensitive analog-to-digital converter.

The CPE utilizes digital techniques for control, evaluation, and comparison. Extensive use of integrated circuits, modular packaged by a proprietary method, increases reliability and reduces cost, size, and weight. This packaging and assembly technique offers cost and labor savings through an automatic stitch wiring process. The installation of 3 cards per inch in the card rack provides a density of 12 integrated circuits per cubic inch.

No sacrifice in maintainability is made in using such high density packaging methods. Troubleshooting techniques are provided which are direct and simple for identification of defective flat packs or integrated circuits. Removal and replacement of a flat pack is made easy using standard tools, since each lead can be independently unsoldered and lifted from its pad. This technique avoids many problems associated with removing a component lead from a printed circuit board without affecting the quality of the underside interconnecting pad wire since it is a welded joint.

The programming format is convenient and English language oriented. The program code is suitable for tape preparation and printing by a standard Flexowriter. The tape reader employed in the current models is a bidirectional line reader which reads 8-level paper or mylar tape at the rate of 100 lines per second.

The CPE contains all necessary digital logic and memory to perform the following operations per tape programmed instructions which essentially constitute one test:

1. Display the test number.
2. Select and hold the desired commands to the adapter to route proper stimuli and loads to the UUT.
3. Select the desired test points and test point returns.
4. Select the measurement type and range.
5. Load the tolerance register with high and low limits for comparison of the tested parameter.
6. Select the conditional procedures; that is, depending on the test results (GO or NO-GO), continue the test routine, stop, print, or search to a subroutine for detailed fault isolation.
7. Stop the tape reader and illuminate the "SEE INST" light if operator participation is required.
8. Load the delay time generator if a time delay is required to allow the UUT to respond to a programmed stimulus.
9. Store the search test number if the conditional procedure (6, above) requires it.

After all of the above parameters (which comprise the test set-up) are read-in, an "X" (execute) is programmed. The CPE then performs the measurements to the specified tolerances and advances to the next test per the conditional procedure (6, above).

The following three modes of operation can be selected by the operator:

1. *Automatic* — The test advances in sequence performing all instructions contained on the tape.
2. *Single Test* — All instructions for one test are accomplished. The test then stops, regardless of the test result, and the actual measured value of the tested parameter is displayed.
3. *Search* — The tape reader slews until a test number decoded from the program tape coincides with the manually selected "SEARCH TEST NUMBER".

The controller/programmer/evaluator can evaluate the following types of electrical parameters: DC voltage, AC voltage (rms), AC voltage (phase sensitive), time intervals, voltage ratio, events per unit time (EPUT), events (absolute), voltage versus time (i.e., ramp signals), resistance (optional) and current (optional).

All measurements are made with a floating differential input to the ground reference supplied by the UUT.

Control

As the binary data is read (a line at a time from the program tape), it is tested for odd parity before being accepted. The data is then decoded to determine if it is an alphabetical character or decimal data. Alphabetical characters are used for signal routing and constitute the "major" address. The major addresses are decoded and then enable the subsequent decimal data to be routed to the desired register and memory. For example, the character "S" enables the next three characters (decimal characters) to be routed to the test search memory. A "minor" address is also generated. Its purpose is to route the individual decimal characters to the proper memory within a specific major address. For example, S456 would cause a "4" to be loaded in the hundreds memory, "5" in the tens, and a "6" in the units memory. By this method, the various memories are loaded with the desired parameters for test (Fig. 3).

Test Point, Ground Point, and Reference Point selectors consist of relays which are activated by a coordinate matrix technique. The desired test point is selected by a 3-decimal digit. The last digit (least significant) selects the "X" coordinate and the center digit the "Y". This energizes one (and only one) relay. The most significant digit then selects one test point of the particular relay energized. The logic automatically de-energizes all relays before selecting a test point.

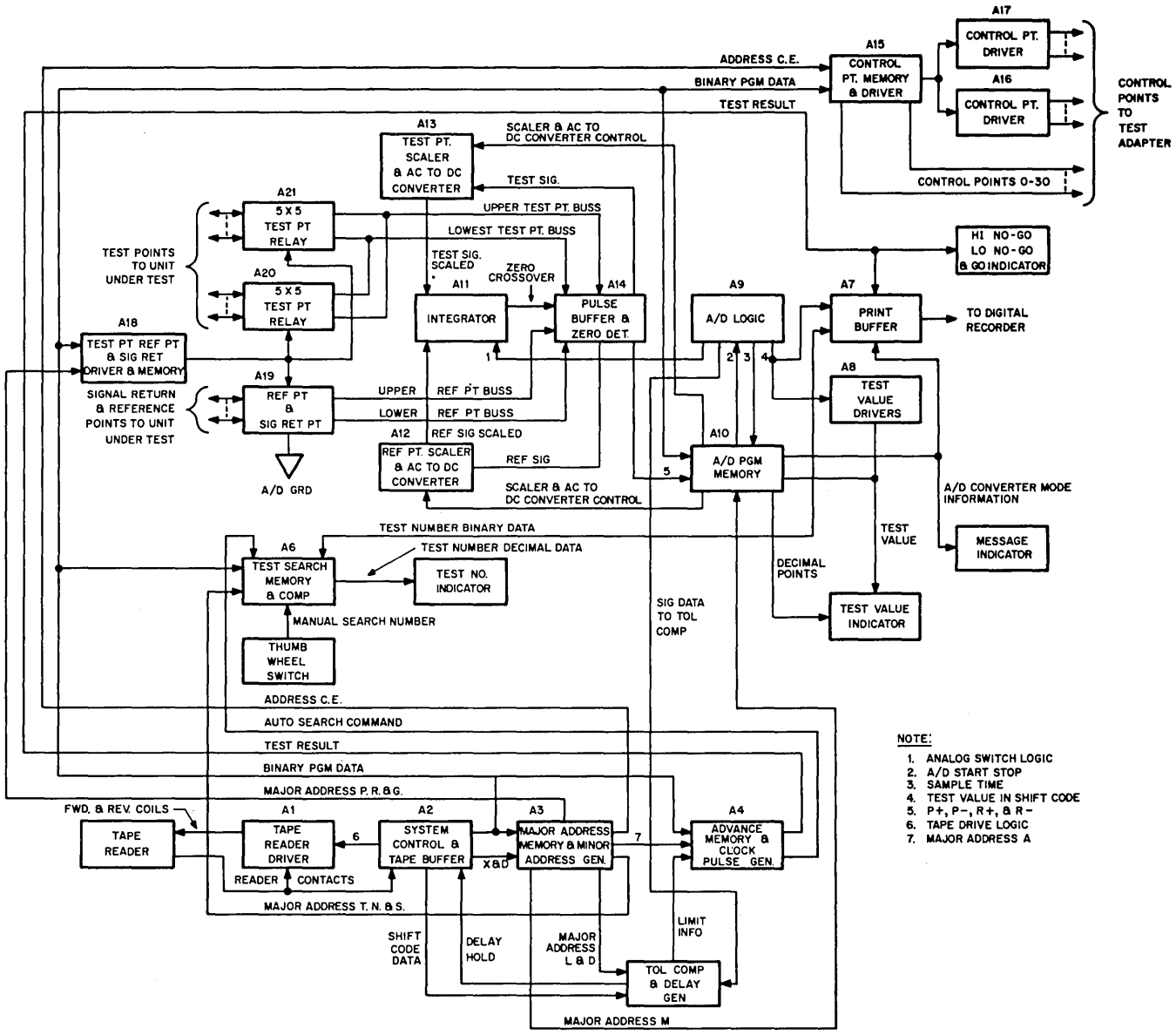

Fig. 3 CPE detailed block diagram.

The control point drivers, which provide grounds to control the adapter, are also selected by a coordinate matrix technique. The circuitry employed is entirely solid-state. The control points are called up one at a time per tape programmed instructions. Each control point remains in one state until specifically programmed to change states. The control points can each sink up to 200 milliamps.

The delay generator consists of decade counters which store the desired delay time. However, the delay actually will not occur until "X" (execute) or until the specific command "H" (hold) is read-in by the tape reader. At this time, the delay generator receives accurate pulses from the crystal oscillator time base. The counter is run down to 0000, allowing the test to proceed.

The test numbers are stored in flip-flop memories. This binary data is decoded to decimal. Integrated circuit drivers are used to provide the power for the test number indicator display. Included is the test search comparator. This circuitry, when in the automatic search mode, examines the test number and the test search number for coincidence. It provides the commands to drive the tape reader in the proper direction until the search test number and the test number are the same.

The A-D Converter

The analog-to-digital converter used for signal evaluation is based on a double integration technique. An unknown voltage "E" is integrated for a fixed time interval ("X" counts). Then the input to the integrator is changed to a precision reference voltage of opposite polarity. The time for the integrated output to return to zero is measured. This time is directly

proportional to the unknown "E" voltage. A counter is used to count the number of pulses which occur while the integrator is integrating down. The pulses, which enter into a decade counter, are decoded and displayed as the actual value of the measured unknown voltage "E". For simplicity, Fig. 3 shows relays for switching. All switching is actually accomplished by solid-state components.

The analog-to-digital converter is in reality a DC voltage to pulse count converter. Signal conditioning is accomplished prior to A-D conversion to normalize the signal to DC voltage within range of the integrator. The A-D used in the CPE has a 0.1 percent accuracy over the temperature range of —40°C to +55°C. Under a laboratory environment, the circuit is better than 0.01 percent accurate.

The comparator circuitry consists of a HI tolerance counter and a LO tolerance counter. These counters are set at the desired value prior to A-D conversion. These tolerance counters are countdown counters and receive the same pulses as those that record the actual value of the measured parameter. Therefore, for a "GO" condition, the HI counter must not have reached zero, and the LO counter must have reached zero. Otherwise, the output indication would be a HI and LO respectively.

Tape Preparation

Tape preparation (programming) for the controller/programmer/evaluator, to test any specific unit under test, actually begins with the design of the adapter. For optimum testing, the design of the adapter and programming considerations should occur simultaneously. The adapter designer should become familiar with the UUT by reviewing its specification and performance requirements so that he can provide the optimum stimuli and loads in the adapter. If possible, the adapter designer should provide suggestions to the UUT designer to insure that sufficient and proper test points are made available external to the UUT so that the desired degree of fault isolation can be accomplished. Most times, however, this ideal design is not possible, and he will have to work with the test points available.

The stimuli and loads provided in the adapter are generally controlled by relays in the adapter. The coils of these relays are wired to the CPE control points. By using a one-to-one correspondence between relay identification and control point identification, programming is made easier, i.e., relay 001 is energized by control point 001, relay 002 by control point 002, etc.

The programmer then proceeds in much the same manner as if he were preparing a handbook for a manual tester. He simply selects relays to be energized that will apply the correct loads and stimuli. He then selects the test points necessary to evaluate the circuitry. The UUT specifications assist him to establish acceptable tolerances for the responses to the applied stimuli. These tests are each assigned a test number and are organized in a step-by-step sequence. During this process, the programmer must develop a cross-reference table to indicate specifically what failed in the UUT (should the particular test fail) or show a HI or LO Limit exceeded. The controller/programmer/evaluator has the capability to enter a subroutine, if programmed, to perform detailed testing for fault isolation. Some tests will require subroutine fault isolation, others will not. The aforementioned cross-reference table can be supplied as a repair instruction handbook or be photographed and projected in the Microfilm Information Retrieval System if desired.

The mechanics of tape preparation require a Flexowriter and operator. The operator can be a trained typist. The Flexowriter punches a tape and prepares a typed printout simultaneously. The printout is checked for accuracy against the programmer's handwritten forms. To facilitate tape punching, general purpose tape preparation equipment that may be used instead of the Flexowriter, has been developed. This equipment is not necessary for CPE tape preparation, however it provides a convenient time saving device to edit, duplicate, and verify program tapes.

After the tapes are prepared, the UUT, adapter, and tapes are "played" together to determine compatibility. The CPE is operated in the single test mode so that the actual test value can be observed and compared to a predicted value. By using a printer in conjunction with the CPE, the test value is automatically printed and the check accomplished "off line". Any errors in the program tape are noted and corrected and the process repeated. Once a good tape is obtained, a duplicate is prepared with a printout and stored in a master file. A keyboard is available so that test programs can be generated "on-line" to assist the "debugging" process. Preparation of the tape can best be understood by noting the simplified software preparation chart.

SOFTWARE PREPARATION

Test Number . . . . . T---N,
Control Points, Set . . . . . C---,
Eliminate (Reset) Control Point . E---,
Test Point Select . . . . . P---,
Ground Point Select . . . . . G–,
Mode, Evaluation and Range . . M---,
Advance Instructions
(GO-NO GO Reaction) . . . A–,
Limits (Hi and Lo Tolerances) . L----------,
Reference Point . . . . . R--,
Delay Time . . . . . D----,
Execute Test . . . . . X,
Operator Participate . . . . . O,
Search Test Number . . . . . S---,
Clear . . . . . K,
Hold Reader for Delay . . . . H,
Finish (Test Complete) . . . . F,

Example Test:
T246N, C43, P145, G8, M4Ø4, A4, S247, RØ6, LØ11ØØØØ9ØØ, DØØØ, X, O,

This article describes the design features and operational capabilities of a series of three wire memory systems. These systems are random-access, three-wire coincident-current memories having capacities of 4096 through 32,768 words with bit lengths from 4 through 72 per word.

A THREE-WIRE MEMORY SYSTEMS DESIGN

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This three-wire memory system is an improvement on the conventional four-wire coincident-current memory. In the three-wire system, one wire is eliminated and a single wire performs both the sense and inhibit functions. This wire (the "sense/inhibit" wire) carries the inhibit current during the "write" portion of the cycle and the sense voltage during the "read" portion. The function of the X and Y wires is the same as in the conventional four-wire system.

GENERAL SYSTEM DESCRIPTION

As shown in the block diagram of Fig. 1, each system has two registers, one for addressing and one for information. The Memory Address Register (MAR) holds the location designation of each information word and varies in capacity from 12 bits (4096 words) to 15 bits (32,768 words). The Memory Information Register (MIR) accepts the incoming information word during the Clear/Write mode of operation and delivers the outgoing information word during the Read/Restore mode of operation. It ranges in capacity from 4 to 72 bits, depending on the numbr of bits per word. Program control signals from external equipment initiate each memory cycle. Clock inputs permit the system Timing Generator to produce the internal timing command and control pulses required for each cycle.

Each magnetic-memory stack consists of parallel planes, each containing 16,384 ferrite cores arranged in four quadrants with one sense/inhibit winding in each quadrant. The planes are assembled into a stack on four stacking rods, and the terminals on one plane are connected to the terminals of the next to provide continuity for the drive lines through the stack. Sense/inhibit lines are wired to connectors, and the drive lines are connected to a decoding matrix attached to the stack. The input to the decoding matrix is accomplishd by means of connectors. Thus, the complete stack is a plug-in module.

WIRING ARRANGEMENT

Operation of the three-wire magnetic memory is best explained by examination of one quadrant of a plane.

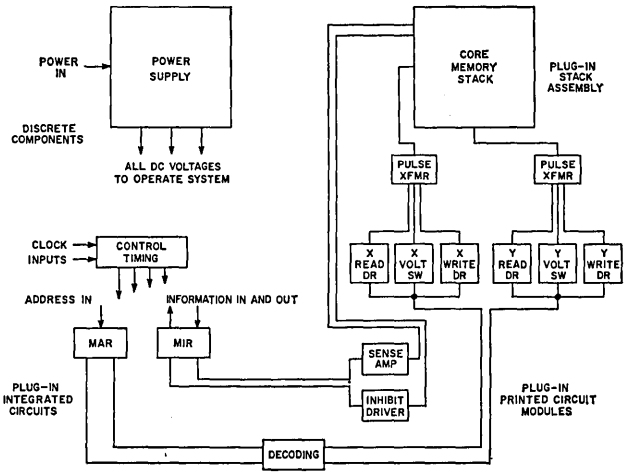


Fig. 1 System block diagram.

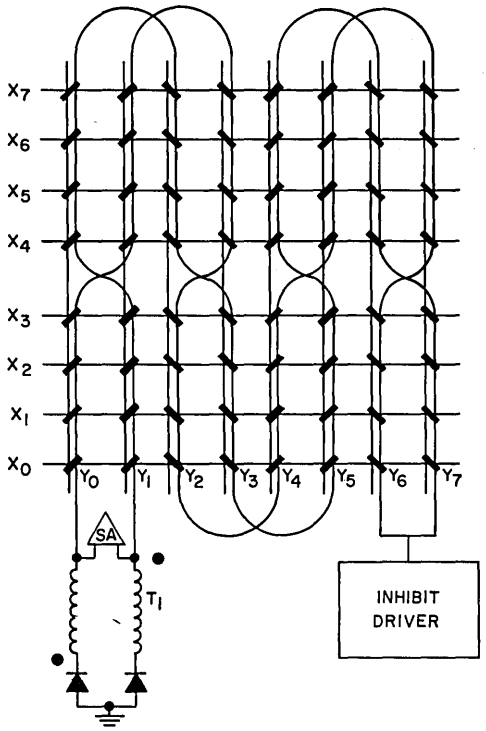


Fig. 2 Eight by eight core array.

Fig. 2 shows a typical eight-by-eight core array. The X-axis drive wire carries a half-select "read" or "wire" current pulse equivalent to one-half the current required to switch a core. The Y-axis drive wire also carries a half-select "read" or "write" current pulse. Either half-select pulse is insufficient to switch a core. The sense/inhibit wire carries a half-select current pulse during the "write" operation, and also carries the sense voltage during the "read" operation.

During the "write" operation, when a ONE is to be written, half-select current pulses are driven along the X and Y wires and add at the selected address to change the flux state of the core. When a core is to be left in the ZERO state, X and Y lines again receive half-select current pulses, but at the same time a half-select current pulse is driven along the sense/inhibit wire. The direction of this pulse opposes and therefore cancels the X pulse. The net result is one half-select pulse which is insufficient to switch the core; as a result, the core remains in a ZERO state.

During the "read" operation, X and Y half-select current pulses are again applied, but in the opposite direction. These current pulses add at the core location to switch the core. The sense/inhibit wire functions during this portion of the cycle to carry the sense voltage to the differential sense amplifier.

The technique of using one wire for both the sense and inhibit functions involves splitting the sense/inhibit winding into two wires or legs (Fig. 2), and driving the inhibit current into each leg. Only one inhibit-driver circuit is required for the two legs. The bisecting of the wire results in a shorter period of time required for transient decay. In addition, the use of a differential sense amplifier for detection of the signal provides a means of eliminating noise transients. This amplifier has a high common-mode rejection that combines and rejects the major part of the common mode noise.

The purpose of the balun transformer T_1 is to force an impedance balance between leg 1 and leg 2 of the sense/inhibit wire so that the inhibit current is the same in each leg regardless of the resistance unbalance in the two legs.

DRIVE SYSTEM

The coordinate drive lines in the core stack are divided into 64 X and 64 Y lines for a system of 4096 words, and into 128 X and 128 Y lines for a system of 16,384 words. A given X or Y drive line is connected to the secondary winding of a pulse transformer. The direction of current flow in the drive line is determined by a split primary winding of the same pulse transformer; one-half of the winding provides "read" current when it is activated, and the other half provides "write" current.

The drive transformers for the X lines are connected in an eight-by-eight matrix for a system of 4096 words. A typical matrix is shown in Fig. 3. Eight primary-winding center taps are connected together and are selected by means of a voltage switch that provides a current path to ground. (Eight "read" primary windings are connected together, and eight "write" windings are similarly connected.) Groups of eight primary windings are selected by means of the appropriate current switch. Current switches, when activated, provide a current path from "read" or "write" current sources through a primary of the drive transformer that has been selected by a given voltage switch. The inputs to the voltage switches are supplied by decoder circuits that are, in turn, driven by the Memory Address Register circuits.

The inputs to the current switches are connected in a matrix that permits selection of one "read" or "write" current switch from a group of eight "read" and eight "write" switches. The transformers used for inputs to the current switches are driven by Decoder Drivers and Decoder Switches. The decoders select a particular current switch by decoding the outputs of the Memory Address Register.

The drive system for the Y lines is identical to that described for the X lines. The drive matrix for 16,384-word systems is the same as that used for the 4096-word memory, except that 16 primary-winding center taps are connected together by the voltage switch. The increased capacity also requires the use of an eight-by-sixteen selection matrix which enables the system to decode 128 lines for both X and Y drive lines. Decoding of 8192-word systems is accomplished by the use of an eight-by-eight matrix on the Y axis and an eight-by-sixteen matrix on the X axis.

TIMING GENERATOR

The timing generator supplies command pulses and levels by use of series combinations of delay lines. These pulses and levels are used within the system to perform timing operations in their proper sequences during a cycle. The timing generator requires a "start-read" pulse or a "start-write" pulse to initiate each

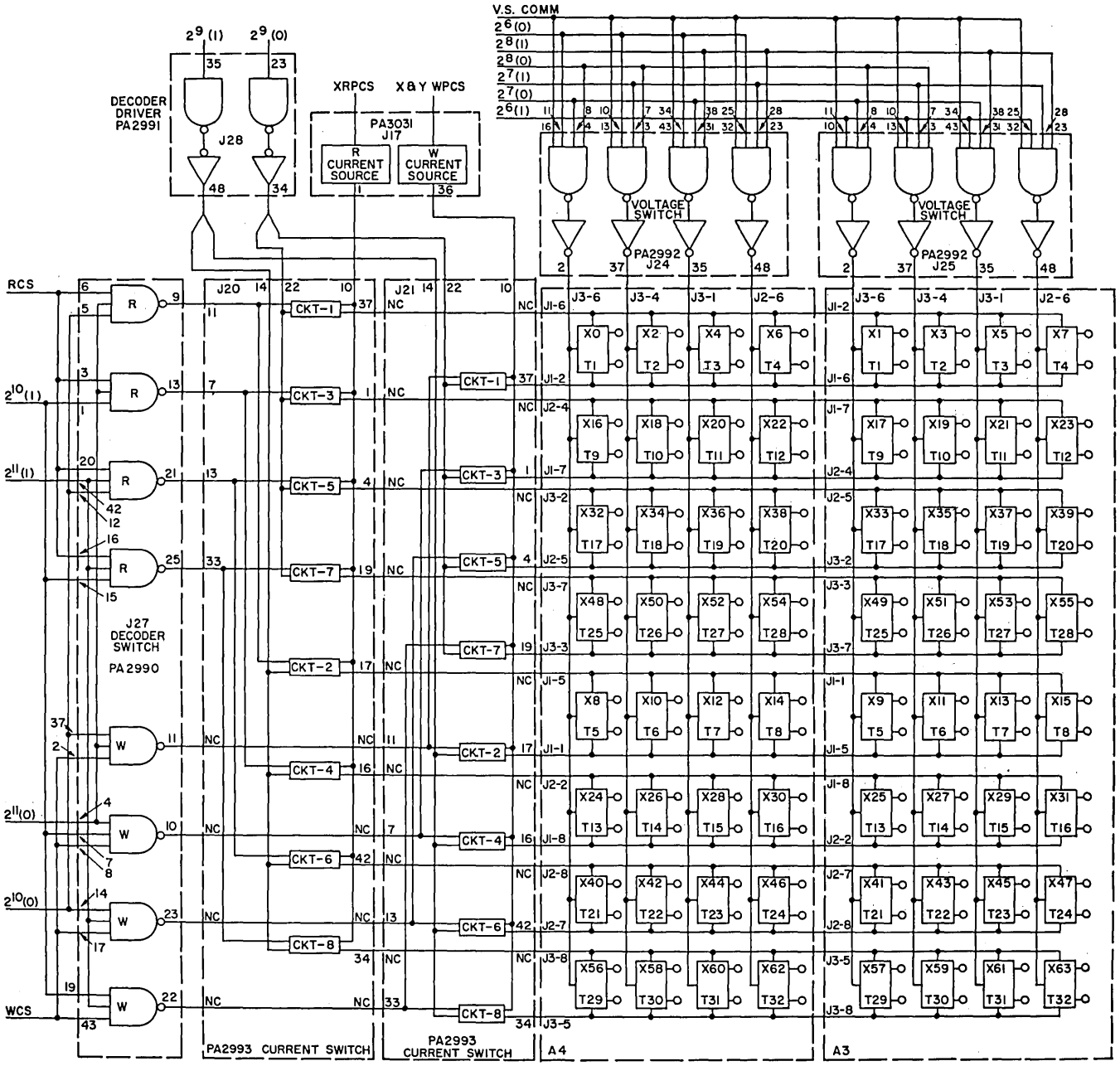


Fig. 3 Typical 4096-word matrix.

cycle. (An optional input-clock feature can also be used to initiate the memory cycle. In this case, the start pulse is combined with a mode input signal to indicate the type of cycle: Read/Regenerate or Clear/Write.) The leading edge of the "start-read" or "start-write" pulse is the determining factor in starting the timing sequence. In certain cases, such as in the use of the sense strobe, a narrow pulse width is desired; consequently, a pulse shaper is used and a multi-tapped delay line determines the pulse width. (The function of the sense strobe pulse is to transfer information from the sense amplifiers to the flip-flop circuits of the Memory Information Register.)

The reset line in the timing generator provides a means for clearing information from the information registers. A flip-flop output inhibits the generation of a sense-strobe pulse during the Clear/Write mode of operation. Figs. 4 and 5 show typical timing diagrams for the Read/Regenerate and the Clear/Write modes of operation.

SYSTEM REGISTERS

The Memory Address Register holds the location designation of each selected information word. It receives an address from an external data-processing control unit, and stores this address in a group of flip-flop circuits. The number of flip-flops required is determined by the number of words in the memory stack: 12 flip-flops for a 4096-word system, 15 for a 32,768-word system. Address input signals are strobed into the input of each flip flop. Therefore, the external equipment is not required to maintain selection levels during the entire cycle.

At the start of the memory cycle, the signals on the MAR output lines are routed to decoder drivers and

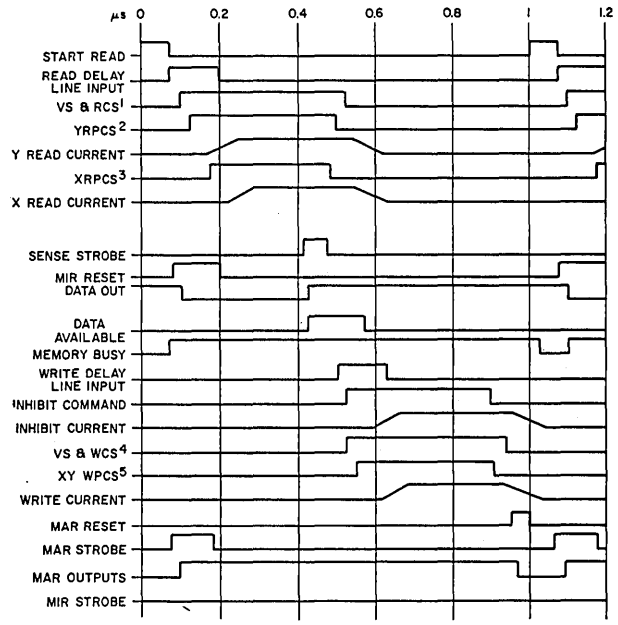


Fig. 4 Timing diagram for read/regenerate mode.

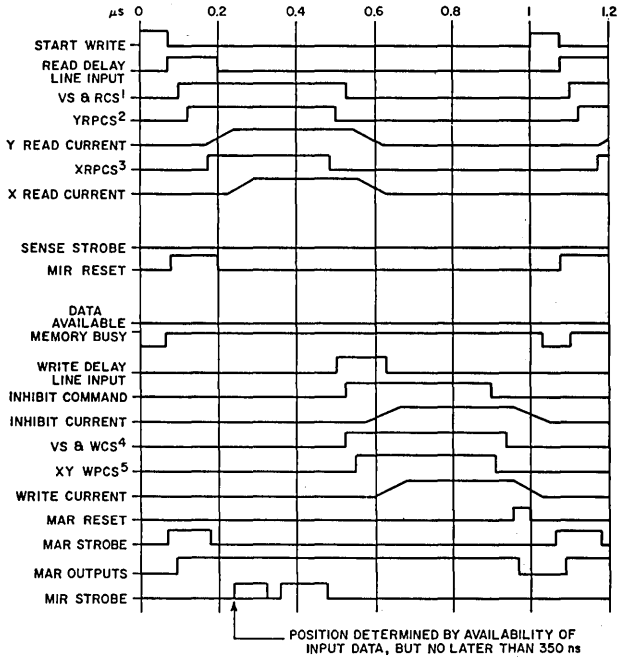


Fig. 5 Timing diagram for clear/write mode.

1 — Voltage Switch and Read Current Switch
2 — Y Read Pulsed Current Source
3 — X Read Pulsed Current Source
4 — Voltage Switch and Write Current Switch
5 — X and Y Write Pulsed Current Source

decoder switches. The signals are translated into activating levels for the selection of the appropriate access drivers and switches corresponding to the required word locations in the core stack. The maximum-capacity memory stack that can be addressed without duplication of read/write drivers is 16,384 words of 20 bits each, due to driving limitations.

Address registers are separated into X and Y flip-flops. For a system of 4096 words, flip-flops 2^0 through 2^5 contain the X address information and flip-flops 2^6 through 2^{11} contain the Y address information. In a 32,768-word system, flip-flops 2^0 through 2^7 contain the X address information and flip-flops 2^8 through 2^{14} the Y address information. The mode of address selection is random-access. Address inputs may be single rail (one line per bit) or double rail (two lines per bit) and are compatible with T^2L logic levels.

The Memory Information Register accepts the incoming information word (single or double rail) during the Clear/Write mode of operation and delivers the outgoing information word during the Read/Regenerate mode of operation. The MIR ranges in capacity from 4 to 72 bits, depending on the number of bits per word. Inputs of the MIR may be single or double rail and are compatible with T^2L logic levels. The outputs are single rail and are also compatible with T^2L logic levels.

MODES OF OPERATION

The Clear/Write mode of operation consists of clearing all the information bits which make up the word at the selected memory address during "read" (clear) time. The new data word is then inserted into the same address during "write" time.

Information is loaded into the MIR during the "read" (clear) portion of the cycle, and the sense strobe is inhibited to preserve the MIR information. All cores of the selected word location are switched to the ZERO state by the "read" drive current. During the "write" portion of the cycle, the information is inserted into the cores at the same location. If a given MIR bit is in the ONE state, its associated inhibit driver is disabled; therefore, no inhibit current flows, and the "write" current switches the core to the ONE state. If a given MIR bit is in the ZERO state, its associated inhibit driver is enabled; therefore, inhibit current flows in a direction opposing the "write" drive current, and the core remains in the ZERO state. (The information detected by the sense amplifies at "read" time is not strobed into the MIR because the strobe command is inhibited.)

The Read/Regenerate mode of operation consists of reading out all information bits that make up the word at the selected memory address during "read" time. This information is stored in the MIR and is made available at the interface for external use. The information is then returned to the same address location during "write" (regenerate) time.

After the MIR has been reset to the ZERO state, information is strobed into it during "read" time by the sense strobe. It stores this information until it is again reset. The outputs of the MIR are connected to inhibit-driver inputs. If a given MIR bit is in the ONE state, its associated inhibit driver is disabled so that no inhibit current flows; the "write" drive current then switches the core to the ONE state. If a given MIR bit is in the ZERO state, its associated inhibit driver is enabled; therefore, inhibit current flows in a direction opposing the "write" drive current, and the core remains in the ZERO state.

OPTIONAL FEATURES

Provision for a Read/Modify/Write (R/M/W) mode of operation permits a full read-write memory cycle to be interrupted between the "read" and "write" portions of the cycle to allow time for revision or modification of the stored data. In this mode of operation, the information at a specified memory location is read into the MIR and then modified by external means. The revised data is written into the same memory location during the subsequent "write" half-cycle. The full cycle in this type of memory operation is increased by the time required to modify the data. The minimum "modify" time is 100 nanoseconds.

Single-error-detection circuits may be incorporated in the design of these memory systems by the inclusion of an extra or redundant bit in each binary word. The extra bit is called the "parity" bit. Circuits can be provided to generate this parity bit during a Clear/Write cycle and to check the parity bit during a Read/Regenerate cycle. The systems can be provided with parity-generate circuits or parity-check circuits, or both, depending on requirements. In addition, the type of parity, odd or even, can be specified.

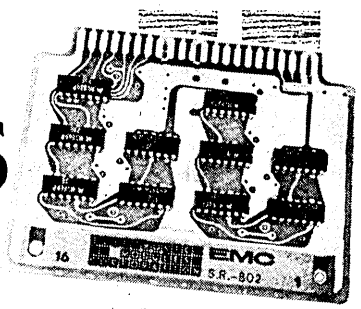
All outputs of the memory information register are connected to inputs of the parity circuits. Any two successive information bits have their ONE or ZERO outputs connected to the inputs of an exclusive-OR gate. The logic to be implemented by the gate is given by $AB + \overline{A}\,\overline{B}$, where A and B are the two successive information bits. All bits of the MIR are divided into groups of two in this manner. The resulting outputs are again divided into groups of two, and connected to another exclusive-OR gate. Successive division of outputs is continued until a final single output is derived. This final output is then used to determine whether a ONE or a ZERO will be written into the parity bit together with the information word. This operation takes place during a Clear/Write cycle.

During a Read/Regenerate cycle, the selected information word is strobed into the MIR during the "read" portion of the cycle. The parity of the information word is again determined, and an appropriate error signal is provided if there is an error. During system "turn-on" or "turn-off," or during a power failure, loss of information stored in the cores can be prevented by inhibiting the clock inputs and turning the supply voltages on or off in a prescribed manner.

CONCLUSION

This series of systems were developed to satisfy the growing need for reliable low-cost memories cycling at 750 to 2000 nanoseconds in the broad capacity range covering 4096 to 32,768 words. The three-wire stack design permits significant savings in the manufacture of the magnetic portion of the system, as well as faster cycle times through use of smaller cores. The coincident-current arrangement improves reliability by permitting a reduction in the number of components required for operation with excellent margins.

SPECIFY EMC INTEGRATED LOGIC CARDS



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CIRCLE NO. 30 ON INQUIRY CARD

APPLICATION NOTE

A Word Interlace Technique for Mating Disc Memories to Computers

R. RONALD TROXELL

Manager Systems Engineering
Data Disc, Inc.
Palo Alto, California

This application note describes a method of mating disc memories having high input rates to computers with considerably lower data transfer rates. Using the formulas and block diagrams provided, the transfer rate of a disc memory can be reduced by any factor of 2^n. The technique was developed for use with Data Disc's F-Series disc memories; however, the method is applicable to any head-per-track disc memory.

The interlacing technique for reducing the word-transfer rate can be explained by the following example, that shows the technique requires only 3 bit times between sectors, instead of the 6 bit times recommended in our earlier application note 004.
Each sector contains one computer word.

Word length = 16 bits + parity
= 17 bits/word

Sector length = word length + 3
= 17 + 3
= 20 bits/sector

Number of sectors possible per track $= \frac{10^5 \text{ bits/track}}{20 \text{ bits/sector}}$
$= 5 \times 10^3$ sectors/trk

Choose 4096 sectors/trk for this example
$= 2^{12}$ words/track

Desired transfer rate = 10,000 words/second

Data Disc maximum word (sector) rate
$= \frac{3 \times 10^6 \text{ bits/sec.}}{20 \text{ bits/word (sector)}}$
$= 15 \times 10^4$ words/sec.

Therefore, reading every 16th word will give a word-transfer rate of $15/16 \times 10^4$, or 9375 words/sec., which is near the desired 10,000 words/sec. rate.

Assume that there is a requirement to set up block transfers of 128 words in length = 2^7 words/block. With 2^7 words/block and 2^{12} words/track, each track will have:

$$\frac{2^{12}}{2^7} = 2^5 \text{ blocks/track}$$

The interlaced blocks on the disc would be organized as shown in Fig. 1. The first word of Block 0 is in Cycle 0 after Track Origin. The second word of Block 0 is in Cycle 1 after Track Origin, and is also labeled 0, continuing thus to the 128th word of Block 0, which is in Cycle 127. Therefore, we can see in Fig. 2 that because there are 32 blocks per track, 16 are distributed in the 128 cycles on the first half of the disc, and 16 are distributed in the 128 cycles on the second half of the disc.

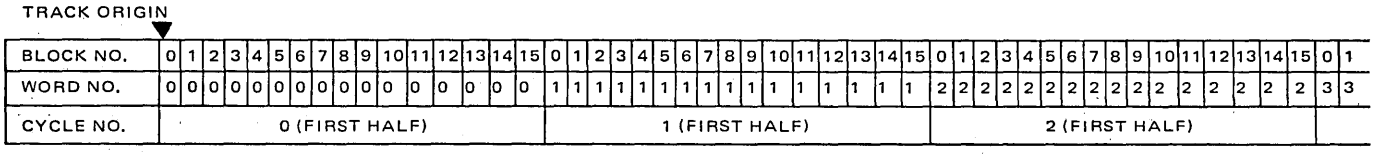

Fig. 1 Organization of interlace blocks.

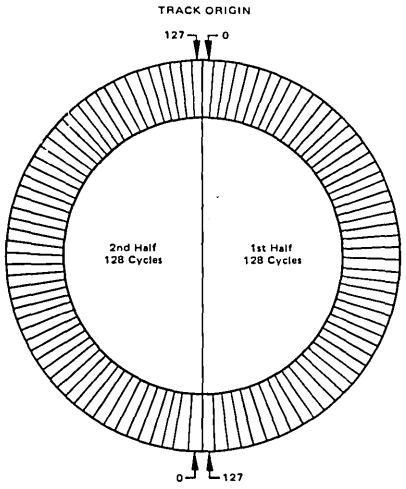

Fig. 2 Cycle distribution for one track.

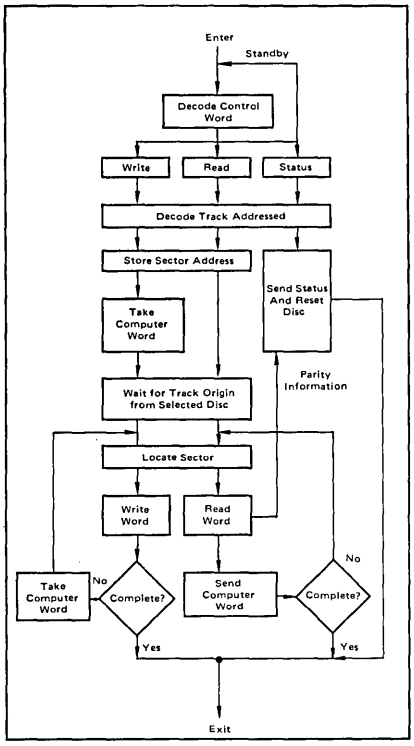

Fig. 3 Flow diagram of controller operation.

A block transfer of 128 words requires taking one word from each cycle on one half of the disc. This results in a block transfer that requires one half of the disc-revolution time: 16.7 msec.

Fig. 3 is a flow diagram of the controller operation for the different modes of operation.

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CIRCLE NO. 17 ON INQUIRY CARD

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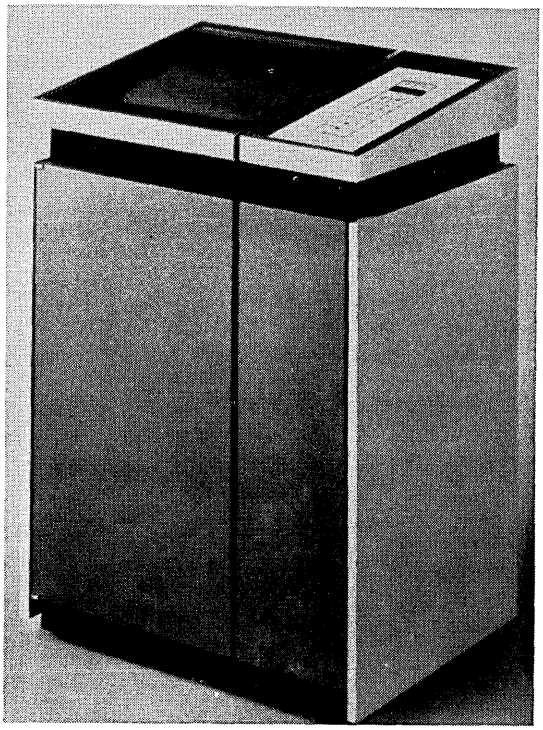


TALLY CORPORATION
Seattle, Washington

A multicopy serial printer that prints out computer or communication data a single character at a time, up to 60 characters per second, has been introduced by Tally Corporation. The unit's speed of 600 words per minute far exceeds other data processing serial printers and is four times faster than an automatic typewriter and six times faster than a teletype machine.

The low-cost printer, which sells in the $4,000 to $6,000 price range, depending on the model desired, fills the void that exists between conventional typewriter printout equipment and the much more expensive line printers. The printer makes it economically feasible to couple printers to remote data terminals in data communications networks, or to bring the advantages of high-speed printout to small computer systems.

OPERATING CHARACTERISTICS

The printer prints asynchronously at 60 characters per second with each character in a word recorded serially (one at a time). Each character is printed as it is received; there is no buffer storage utilized. The printing impression is achieved by a 64 character font cylindrical print element that revolves and moves up and down as it is positioned, character-by-character across the page. A printed line is the standard 120-character width. The carriage may be set to return at any place in the printed line to provide unrestricted format control. The printer utilizes standard computer fanfold, pin feed paper in various sizes up to 15″ wide. In operation, the unit features a minimum noise level and accepts up to six part pin-feed forms.

DESIGN & SPECIFICATIONS

Basic Mechanism

The page printer consists of the print head, paper drive, character select and print head advance mechanisms, ribbon drive, impact print hammer, framework, and appearance covers together with the power supplies, pertinent interval logic and amplifiers necessary to operate the mechanisms. The printing mechanisms can be provided without electronics or enclosure for OEM applications.

Operating Speed

The printer prints asynchronously at 600 words per minute (60 characters per second). Carriage return may be requested at any place in the printed line and is 30-150 milliseconds depending on line length. Backspace and tab functions are optional. Paper advance time is less than 30 milliseconds for single space.

Paper Forms

The standard printer handles fanfold, pin feed paper in various widths up to 15 inches. One to six part copies may be printed. An optional friction feed mechanism handles roll type paper. The paper is loaded from the bottom front and exits from the back of the cabinet top cover.

Character Coding

The print element contains 64 characters consisting of upper case alphabet, numeric and special symbols. The select mechanism is constructed so that data may be transmitted from punch tape to the selection acuators without decoding when six bit ASCII code is used. (2^6 binary bits input). The print element is not replaceable by the operator.

Printing Format

Vertical linespacing is six or three per inch as selected by the operator. Horizontal character spacing is ten per inch. Maximum line length is 120 characters. Character size is .055 inch wide and .080 inch high measured at the center line of the character. Vertical character position accuracy is ± .003 inch character to character and ± .012 inch from nominal position. Horizontal character position accuracy is ± .006 character to character and ± .030 inch from nominal position. The third character line above the line being printed may be read by the operator. The printer uses a multi-pass inked fabric ribbon, replaceable at intervals of six to 24 hours of machine operation.

Operator Controls
Operator controls include: AC power on-off, print start, print stop, carriage return, paper feed slew, paper feed single or double step selection, and function error reset. (Print start, print stop, and function error reset do not directly control page printer logic.) Indicator lights are used to indicate end of paper form and to illuminate control switches as required.

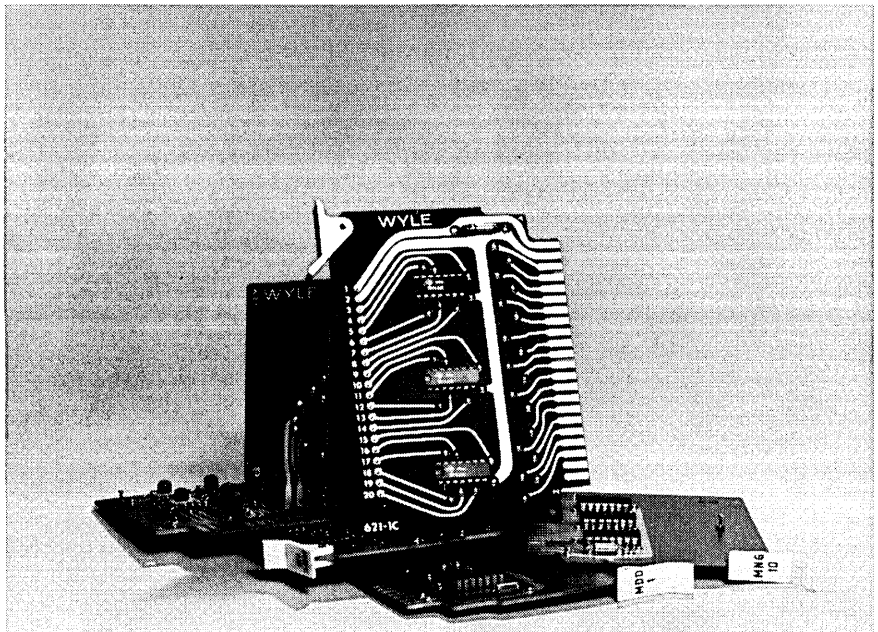
Environmental Conditions
The ambient operating temperature limits are 40 degrees F to 115 degrees F. The storage temperature limits are 30 degrees F to 150 degrees F. Operating and storage relative humidity limits are 30% to 90% (non-precipitating). The machine attitude must be vertical and free air ventilation must be allowed on all sides of the machine.

Electrical Requirements
AC power input requires a separate, fused 20 amp service with a three wire grounded termination. Surge currents up to 40 amps peak for 10 cycles (167 milliseconds) can be expected at turn on time. The system draws approximately 15 amps at 115 volts nominal 60 cps. Operation is between 105 and 125 volts and 60 ± .25 cps. Input signals are to RS 232A E/A or optionally to other logic levels. The output inhibit line must be used to condition signals during carriage return and paper feed functions. During operation driven by an externally clocked source, panel controls must be interlocked with the inhibit line and the source.

Mechanical Configuration
The cabinet size is approximately 34″ wide by 46″ high by 23″ deep. The top cover pivots open to provide the operator with front access to the ribbon mechanism and paper path. Drive mechanisms are shielded to prevent operator hazard. The paper forms box is enclosed in the printer base. Front panels in a choice of colors and a paper receiving frame are optionally available. The mechanism weighs 85 lbs., the electronics 145 lbs. and the covers 200 lbs.

The printer will be available in limited quantities later this year, with full scale production scheduled by the end of 1968.

For additional information circle No. 199 on the Inquiry Card.



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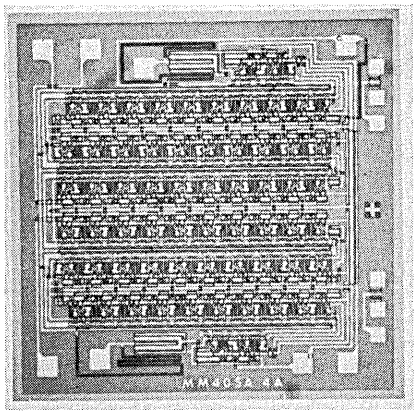
CIRCLE NO. 18 ON INQUIRY CARD

NEW PRODUCTS

MOS STATIC SHIFT REGISTER

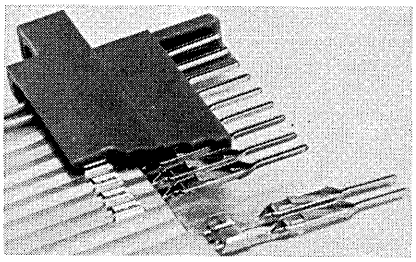
The MM405 dual 32 bit MOS static shift register operates from DC to 1MHz, and is designed with low threshold transistors permitting operation with a V_{DD} supply voltage of −10 V; a clock amplitude and V_{GG} supply of less than 16 V. Other features are low power consumption of 1.7 mW per bit and a low output impedance of 500 ohms. Each register cell is designed to avoid race conditions during latching, thereby insuring proper operation under all specified electrical characteristics. This design also permits considerable flexibility in clock pulse waveshape and amplitude. The MM405 is designed for digital memory or delay line applications in synchronous or asynchronous digital systems. National Semiconductor Corp., Santa Clara, Calif.



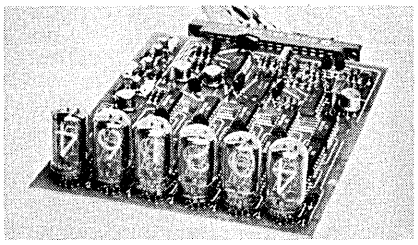
Circle No. 200 on Inquiry Card.

FLEXIBLE FLAT CABLE CONNECTOR

AMP-UNYT™ flexible flat cable connectors utilize an insulation piercing crimp to make physical and electrical contact with the cable. Designed primarily for use with cables meeting NAS 729 (0.063″ wide conductors on 0.100″ centers), they are available in cable-to-cable, cable-to-wire, and cable-to-board configurations. The crimp-on, snap-in contacts avoid the uncertainties caused by heat of soldering or welding, and reinforce the end of the relatively fragile cable rather than weakening it by removal of the structurally necessary insulation. The mating end of the phosphor bronze contacts is an 0.025″ square post (on 0.100″ centers) compatible with the AMPMODU™ interconnection techniques. The connectors meet the high potential, insulation resistance, corrosion, thermal shock, high temperature life, contact resistance, and low potential requirements of the Institute of Printed Circuit Standard IPC-FC-218. Current carrying capacity is rated at 3 A. Amp, Inc., Harrisburg, Pa.



Circle No. 210 on Inquiry Card.



ELECTRONIC COUNTER

The Model KO1-5221A counter board counts electrical events at rates up to 10 MHz and displays the results on long-life Nixie® tubes as a total or, when the count is gated for precise intervals, as a frequency. It can also be used to measure time intervals. The board includes all circuits but the power supply, input signal conditioner, and front-panel control functions. Required inputs, brought into the board through a single printed circuit board connector, are: 5.1 Vdc at 750 mA for circuit operation; 170 Vdc at 1.5 mA per Nixie for display operations; 9 V rms ac at 60 Hz for the time base.

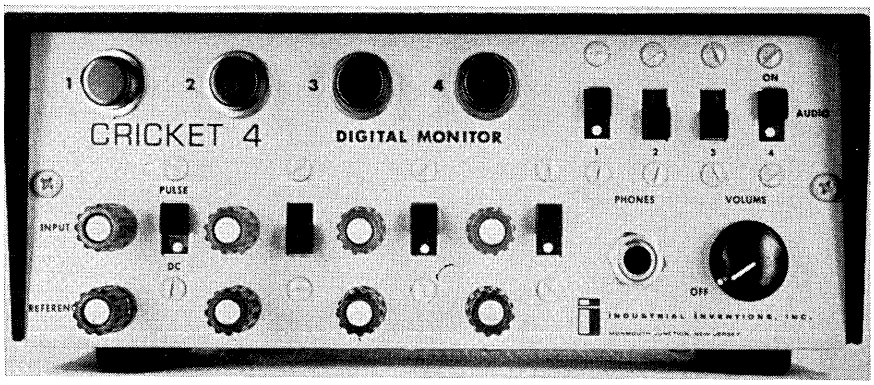
Counter reset and gate time, either variable or fixed at 0.1 or 1 second (derived by the counter from the 60 Hz power line), are controlled by contact closures to ground on other pins of the connector. The input signal should be in the form of pulses more than 40 ns wide, between +3 and +5 V in amplitude, and with risetime less than 10 ns. An optional input amplifier board permits positive or negative pulses and sine waves at frequencies from 5 Hz to 10 MHz, and at amplitudes between 100 mV and 3.5 V, to be counted. Hewlett Packard, Palo Alto, Calif.

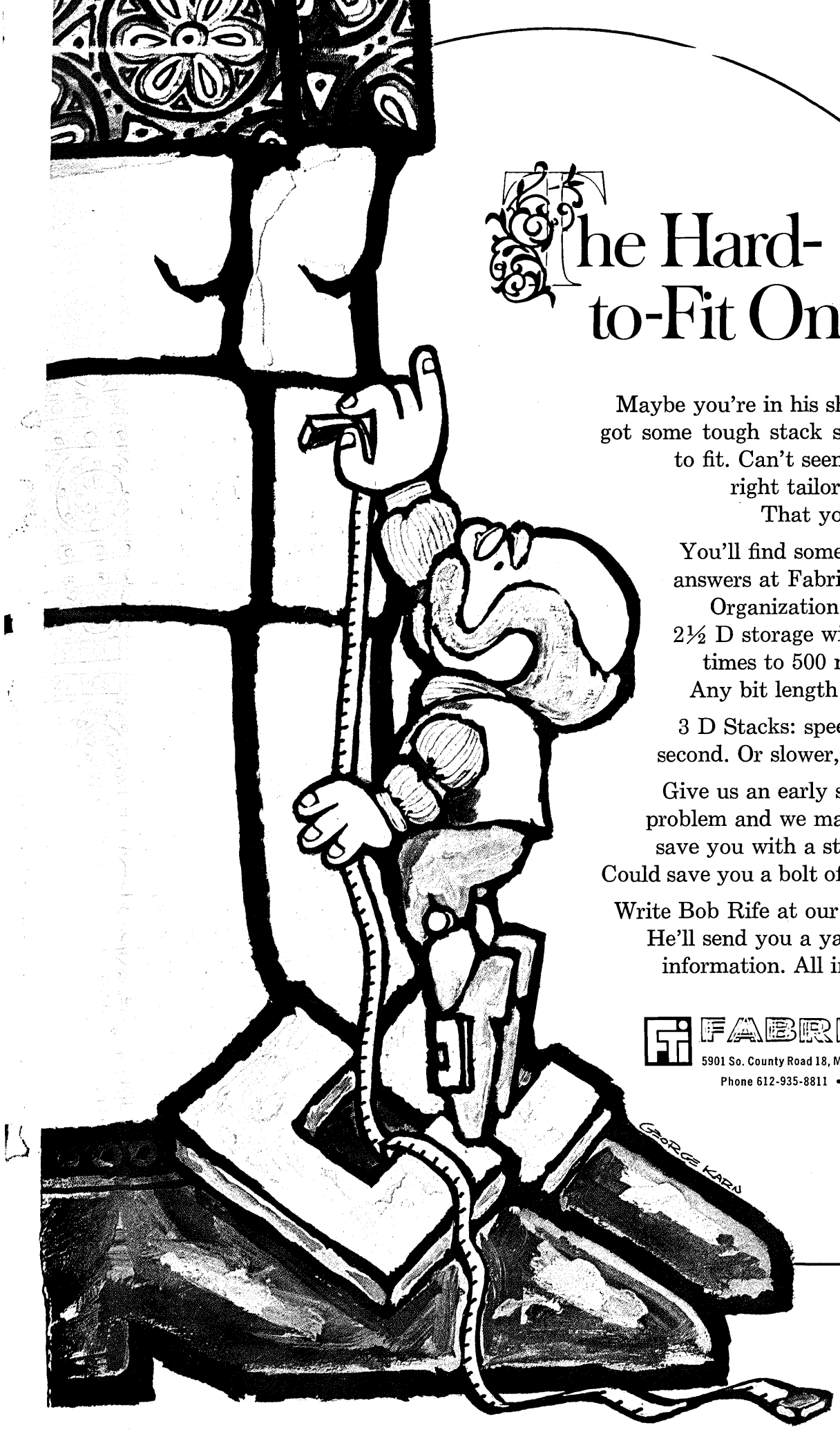
Circle No. 225 on Inquiry Card.

SYSTEM/CIRCUIT TESTER

The Cricket 4 digital monitor provides a new concept in system and circuit testing. It has four channels and each produces a different audible tone and lamp indication when triggered by negative-going pulses. Thus, the engineer can audibly monitor circuit points while making changes or adjustments at the bench or at remote locations. The instrument does not require synchronization and can replace an oscilloscope in numerous applications. It may be left permanently in the circuitry while breadboarding or trouble shooting a system. It is extremely useful for tracking down and investigating electrical noise. With four points being monitored, complex circuitry can produce a characteristic tone pattern which is useful in determing correct operation. The unit also has a DC mode which can be used to indicate binary "1" or "0" logic levels with any common logic or voltage system and with any type of integrated or discrete circuitry, Industrial Inventions, Inc., Monmouth Junction, N.J.

Circle No. 245 on Inquiry Card.





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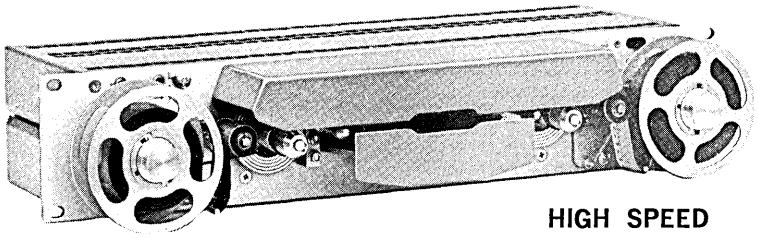

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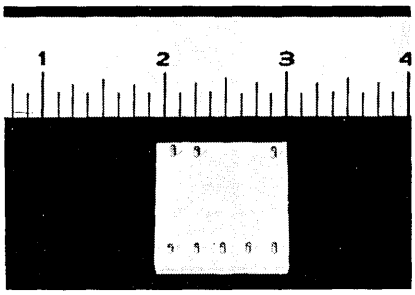
CIRCLE NO. 19 ON INQUIRY CARD

NEW PRODUCTS



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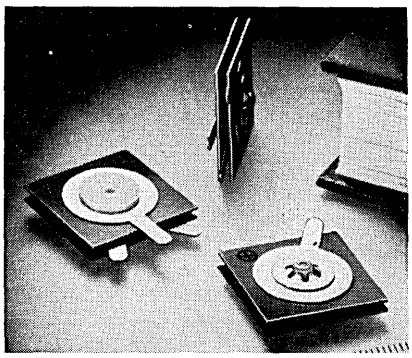
Circle No. 206 on Inquiry Card.



HIGH CURRENT RECTIFIERS

A line of 70 A transient voltage protected silicon rectifiers, designated as the ST-11 series, have PIV ratings from 100 to 1000. The units are hermetically sealed in stud mounted cases measuring only 15/16" in height, exclusive of the mounting stud. These high current rectifiers are designed primarily for application in computers, speed controls, power supplies, battery chargers, switch gear, variable drives, motors and generators. Sarkes Tarzian, Inc. Semiconductor Division, Bloomington, Ind.

Circle No. 202 on Inquiry Card.

MULTIPLE NOR MOSFET ARRAYS

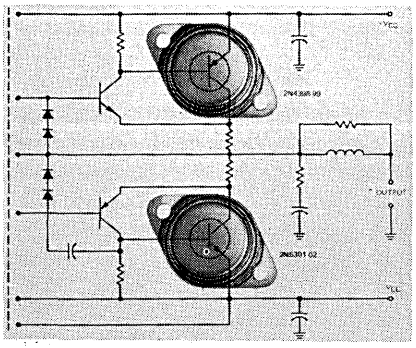
The type HRM2304 monolithic MOSFET array, consists of three triple-input and two dual-input NOR gates.

The monolithic chip is .050" x .053" in size, and is normally packaged in a 22-lead sound flatpack. Input threshhold voltages are nominally −2 V so that the chip may be used to interface DTL, TTL and RTL logic systems with higher level MOS logic arrays.

Each NOR gate output is capable of swinging 24 V when properly biased and operating speeds are typically 1 megacycle. All input gates are diode protected and the NOR gate outputs may be connected together to expand the number of inputs at each gate.

Hughes MOSFETS, Newport Beach, Calif.

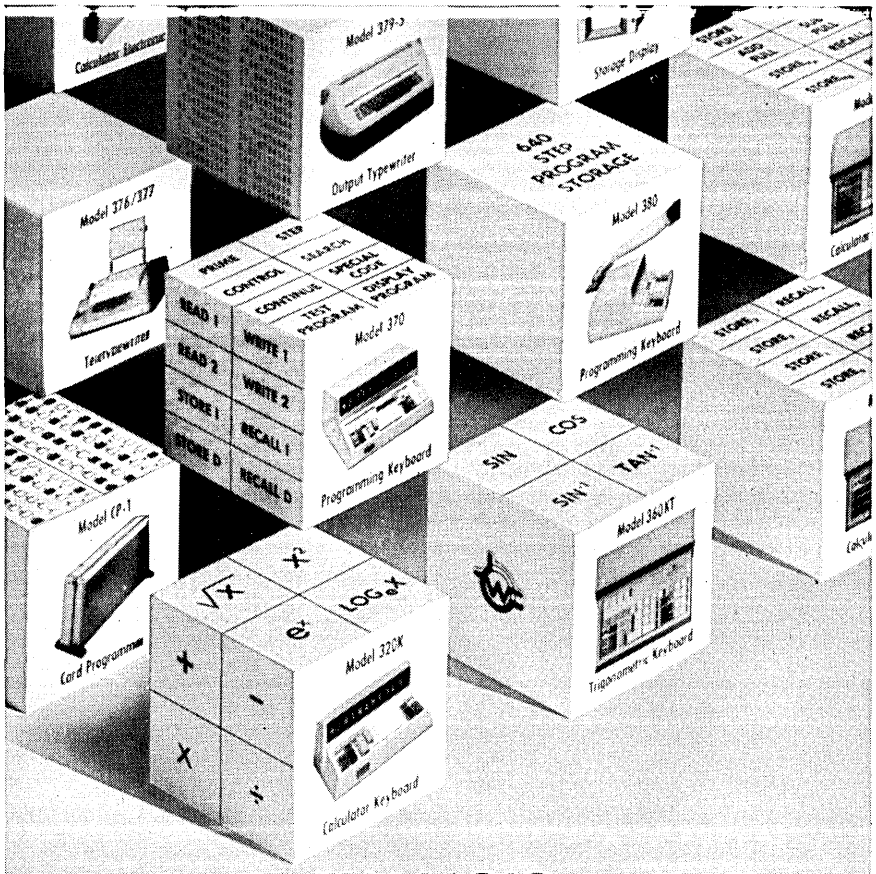
Circle No. 204 on Inquiry Card.



HIGH POWER TRANSISTORS

Series 2N5301 and 2N5302 NPN transistors in 40V and 60V versions can be paired with Series 2N4398 and 2N4399 30 A transistors to furnish the highest silicon power transistor complementary symmetry capability possible. The units can handle 200 W of power to 30 V V_{CE} enabling direct, plug-in replacement of germanium types in "extra tough" amplifier, voltage regulator and modulator designs. Lighter, simpler and less-costly head sinking also results through low thermal resistance — θ_{JC} of 0.875°C/W. Elimination of power/speed trade-offs in switching applications is achieved through 400 ns delay and rise time (@ 10 A I_C, 30 V V_{CE}) which affords minimum losses. Highly efficient, low-power-loss performance and the capability to swing down in voltage without loss of current gain (to 1 V @ 10 A) in low-distortion audio amplifiers is ensured due to low saturation voltage (1.0 V @ 15 A) of the transistors. Other advantages include a gain linearity over a 5 to 20 A range, 50 A peak current and low-silhouette, TO-3 packaging. Motorola Semiconductor Products, Inc., Phoenix, Ariz.

Circle No. 203 on Inquiry Card.



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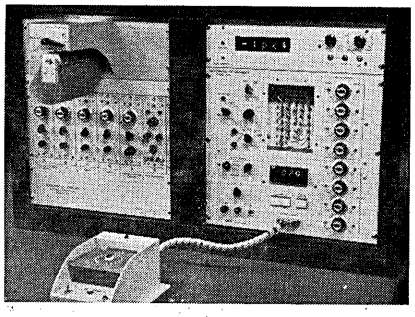
CIRCLE NO. 21 ON INQUIRY CARD

MINIATURE THUMBWHEEL SWITCHES

Series 200 and 700 Miniswitch® sealed thumbwheel switches are designed for equipment or systems that operate in severe environments. The switches are interchangeable and have the same mounting dimensions. In the Series 200, wire leads serve as output terminals so that no part of the printed circuit board is exposed to possible contaminants. In the Series 700, the printed circuit board extends from the rear of the case. The PC extensions provide for direct soldering and the mounting of components directly on the printed circuit board in some models. The switch is only 1.15" high and 0.5" wide requiring a panel cut out of only .920" high. With modular construction any number of switches can form a single, unitized assembly. No separate escutcheon plates, special mounting brackets or other hardware are required for assembly mounting. They are available with two, eight or ten dial positions for binary, octal or decimal outputs. The Digitran Company, Pasadena, Calif.

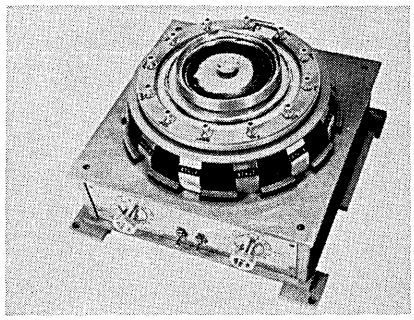
Circle No. 221 on Inquiry Card.



IC AUTOMATIC TESTER

The Model 2400 automatic test system for incoming inspection of integrated circuits performs all of the parameter tests for devices with up to 16 leads. Programming is achieved by an 82 channel punched rope/mylar tape loop affording an unlimited number of tests at a rate of 15 tests per second. The readout is GO/NO-GO with visual display of the measured parameter and test number; data logging outputs are available. Programming is simple and be easily altered. RFS Engineering Co., Phila. Pa.

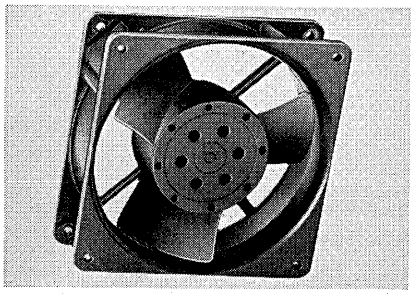
Circle No. 251 on Inquiry Card.



CORE SIZER

This Vibro-core-selector, Mark IV, will precisely grade ferrite memory cores at rates between 50,000 and 400,000 pieces per hour. Flat, round, square or cube-shaped cores as large as 50 mils and as small as 7 mils can be handled. The sizer is designed for total compatibility with the high standards of quality control required for computer memory systems. Selection accuracy is 0.00005 in. Dimensions are 13 x 13 x 9 in.; weight is 40 lb. Shurtronics Corp., Santa Ana, Calif.

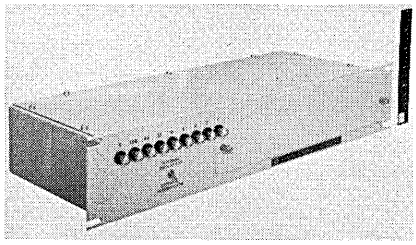
Circle No. 229 on Inquiry Card.



MINIATURE FAN

The Model 4800 all-metal miniature axial fan keeps acoustical disturbance to an absolute minimum with a 17.9 db SIL (Speech Interference Level) rating and silently moves 70 cfm of air. The impedance-protected, two-pole, shaded-pole motor of the fan offers a life expectancy of 100,000 hours, continuous duty, at room temperature (25°C) and 20,000 hours continuous duty at an ambient temperature of 55°C. A hand-fitted, broached dual-sleeve bearing system with a large oil reservoir ensures longer, more reliable operation. The compact fan is 4½" square x 1½" deep. Pamotor, Inc., San Francisco, Calif.

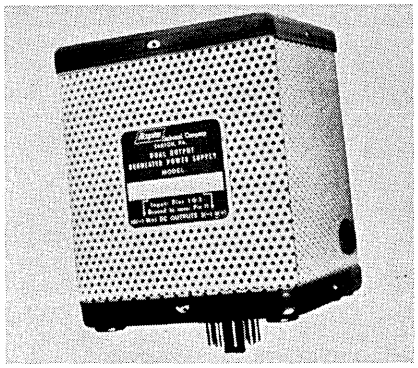
Circle No. 231 on Inquiry Card.



ANALOG TO DIGITAL CONVERTER

This analog-to-digital converter converts to 9-bit digital words at a rate of 10^6 words per second. It was designed for such high-speed applications as radar moving target indicators, data collecting and logging and computing systems. The converter combines a pair of densely packed printed circuit cards and a compact cabinet, suitable for 19-inch-wide rack mounting, to form a complete high-speed unit. The cards, which are accessible from the front panel, contain the A/D converter as well as the sample, hold and timing circuitry. Other features include small size (19" x 8½" x 3½"), lightweight and temperature range of −33°C to +62°C for the circuit cards. Westinghouse Defense and Space Center, Surface Div., Baltimore, Md.

Circle No. 228 on Inquiry Card.

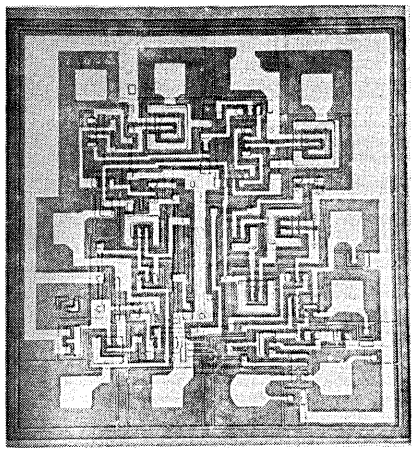


AC TO DC PLUG-IN POWER SUPPLY

A dual 15-volt, 60 mA AC to DC plug-in power supply for operational amplifier applications has short circuit protection, may be used in series, and is operative without additional heat sinking. Specifications include: continuous duty at full load over a temperature range of −20 to +71°C, impedance of 0.07 ohm at 1 KHz and 0.12 ohm at 10 KHz. Outputs are floating. Each individual section may be connected as a separate power supply. Either the negative or positive side of one section may be grounded irrespective of the other section. Acopian Corp., Easton, Pa.

Circle No. 226 on Inquiry Card.

CIRCLE NO. 36 ON INQUIRY CARD →



RETRIGGERABLE MULTIVIBRATOR

An advanced high speed TTL "one-shot" circuit, or monostable multivibrator, TTμL 9601, features a retriggerable design, which eliminates false triggering, low fan-out, low duty cycles, limited pulse width stability, and inaccurate pulse sensitivity. The unit provides a stable and accurate output pulse adjustable from 50 ns to any width within the range of practical capacitor values. The pulse width timing circuit is immune to noise spikes on the supply voltage, ground, and trigger input lines. The input circuitry has no recovery time limitation and is distinguished by a maximum repetition rate greater than 10 MHz. The output pulse has a duration and accuracy that are the sole function of external timing components. Output waveform is independent of pulse width. The 9601 comes in a flat 14-pin Cerpak™ packaged and in a face-down bonded Fairpak™, with optimized pin locations for printed circuit layouts. Fairchild Semiconductor, Mountain View, Calif.

Circle No. 205 on Inquiry Card.

IC VOLTAGE REGULATORS

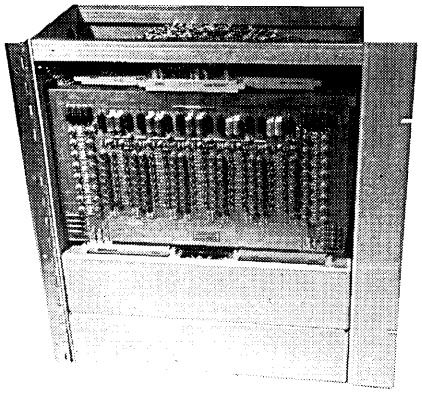
LA-100, LA-200 and LA-300 integrated circuit voltage regulators offer an output voltage adjustable from 2 to 30 V, input voltage range 35 to 40 V, line regulation as low as .05% and load regulation as low as .1%. Output currents in excess of 5 A are possible with external components. Units adapt to both plus and minus output voltages. Operating temperatures are: LA-100 (−55° to +150°C); LA-200 (0° to 70°C) (−50° to +125°C typical); and LA-300 (0° to 70°C) (−50 to +110°C typical). The regulators are packaged in an 8 lead TO-5 package with a monolithic chip. Nucleonic Products Co., Inc., Los Angeles, Calif.

Circle No. 201 on Inquiry Card.

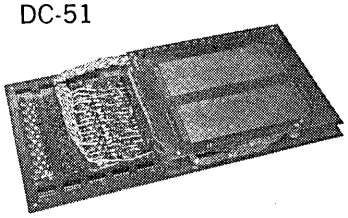
. . . . How's Your Memory?

If you're not getting what you paid for, give us a call next time you have to order one. Chances are, you won't pay as much and you won't have to make any adjustments to get it to turn on.

DC-20



DC-51



DATACRAFT MEMORY PRODUCTS

MODEL	SPEED (FULL CYCLE)	MAX. CAPACITY
DC-20	600 NANOSECONDS	8K X 25
DC-30	1 MICROSECOND	1K X 32, 2K X 24, 4K X 18
DC-31	900 NANOSECONDS	512 X 16, 1K X 8
DC-32	1.5 MICROSECONDS	8K X 26
DC-33	1 MICROSECOND	1K X 8
DC-51	4 MICROSECONDS	256 X 18, 512 X 9
DC-53	2 MICROSECONDS	1K X 10

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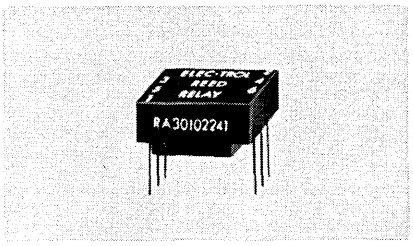
CIRCLE NO. 20 ON INQUIRY CARD

NEW PRODUCTS

RELAY SOCKET ASSEMBLIES

Designated the RS15, these compact printed circuit track-mounted socket assemblies snap in (or out) vertically into a pre-punched vinyl track up to 45" long, which holds up to 20 sockets. A standard-sized, 15-pin receptacle accepts all miniature size 4 P. D. T. relays with two coil leads and ground. Barrier-type terminal blocks, with #2-56 screws and surface clamps, accept up to #16 AWG wire securely, without lugging or looping of wires. Each terminal screw is clearly numbered from 1 to 14, plus ground G, and marking strips are available for relay identification. Installation time is slashed, as only 2 or 3 mounting screw holes must be laid out, drilled, and tapped to securely fasten the track for up to 20 sockets. Current rating of the assemblies is 5 A at 125 V. Curtis Development & Mfg. Co., Milwaukee, Wis.

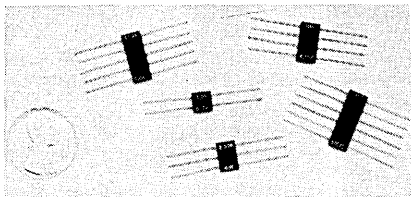
Circle No. 215 on Inquiry Card.



FLAT PACK REED RELAYS

A line of flat pack reed relays are designed for closer board spacing. The relays are compatible with existing flat-pack assembly and welding techniques, and with IC and transistor circuitry. Features include: Pole configurations: 1, 2, 3, 4 and 6, size: height .250", length .50", width .250" to .800" — coil voltages: 6, 12, 24 Vdc (nominal) — pick up time: 150 us — drop-out time: 100 us (nominal) — life: 1 million operations at rated load; 10 million at signal levels — initial contact resistance: 200 milliohms (max.) — max. contact rating: 300 mW — insulation resistance: 10^{11} ohms minimum — vibration 20 G's 10-2000 Hz — shock 150 G's — temperature rating: —50°C to +85°C. Elec-Trol, Inc., Saugus, Calif.

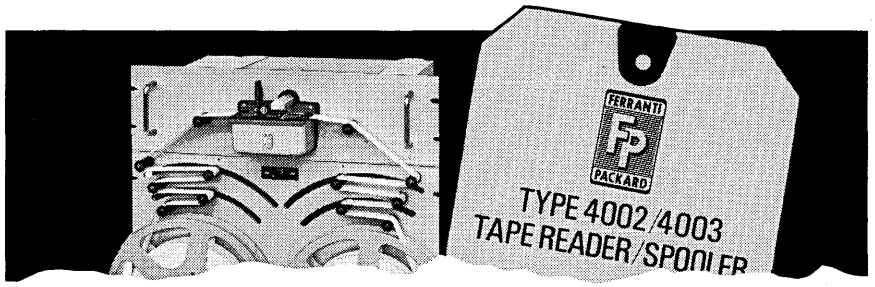
Circle No. 220 on Inquiry Card.



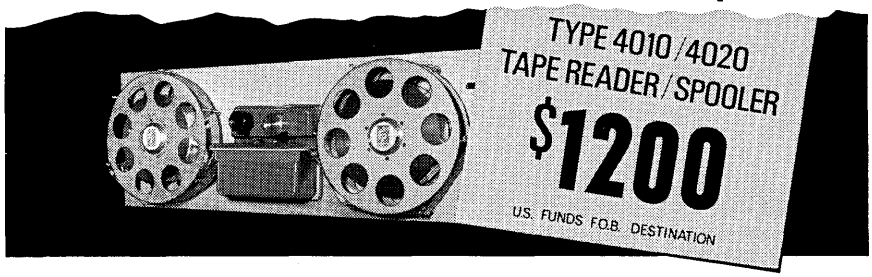
MULTICOMPONENT ASSEMBLIES

Microminiature circuits, consisting of resistors and/or capacitors offer up to six precision components in a single package. Designated "Flat Packs," resistors conform to MIL-R-10509F and capacitors to MIL-C-11015 and may be specified by the customer for characteristics and circuit location. Resistor tolerances as low as ±0.1% are standard with temperature coefficients of 0 ±25 ppm/°C. Lead wires may be tinned copper, goldflashed dumet, or bare nickel "A." Available in five models, they are 0.190" wide and 0.075" thick with length ranging from 0.200" to 0.600", depending on the number of components, which can range from two to six. American Components, Inc., Conshohocken, Pa.

Circle No. 217 on Inquiry Card.



We've taken our 1000 C.P.S. Paper Tape Reader/Spooler, slowed it down to 300 C.P.S., halved the price...



...and come up with a dependable unit that can't be matched in terms of quality, economy and delivery.

Medium speed range — up to 300 characters/second — photoelectric sensing — stops on character at 300 characters/second — bidirectional — silicon logic — tried and tested design concept and components — off the shelf delivery from mid 1968 — low unit price of $1,200.00. For complete details, write, wire or phone.

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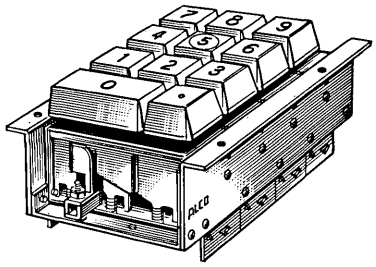
CIRCLE NO. 22 ON INQUIRY CARD



REED SWITCH KEYBOARD ASSEMBLY

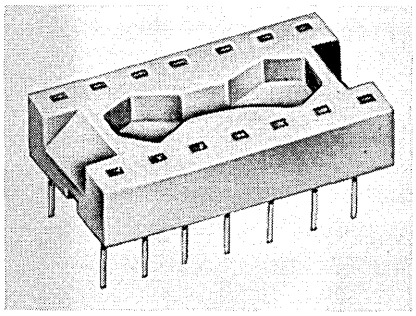
A reliable keyboard using long-life, open circuit reed switches, Model SB-033 provides smooth operation of the switch plunger for data processing and test equipment, communications gear, and other applications. All details of this switch line are designed for light pressure (5 ounces), operator's convenience, and positive input of data with long life for heavy office type of usage. Highly efficient "single-pole open circuit" reed switches assure reliability and extremely long-life expectancy. Square, light grey buttons (19/32") have an industry standard 0-9 marking and placement along with a period. All switch positions contain a "positive lockout" between sections and rows. This feature prevents more than one position from operating at the same time. An extra "decimal" button is also provided to enhance design use. Alco Electronic Products, Inc., Lawrence, Mass.

Circle No. 211 on Inquiry Card.

ULTRA-MINIATURE FLEXIBLE COAX

An ultra-miniature, air-spaced coaxial cable has been designed for use where cable flex-life is extremely important such as data processing applications and wherever small cables are frequently flexed because of doors, drawers, etc. The 95 ohm cable has a nominal outside diameter of 0.105" and is covered by a nylon jacket to minimize outside dimensions. The inner conductor consists of seven strands of no. 38 gauge, copperclad, tin-coated steel. The cable is also available jacketed in a flame-retardant copolymer. Times Wire and Cable, Wallingford, Conn.

Circle No. 219 on Inquiry Card.



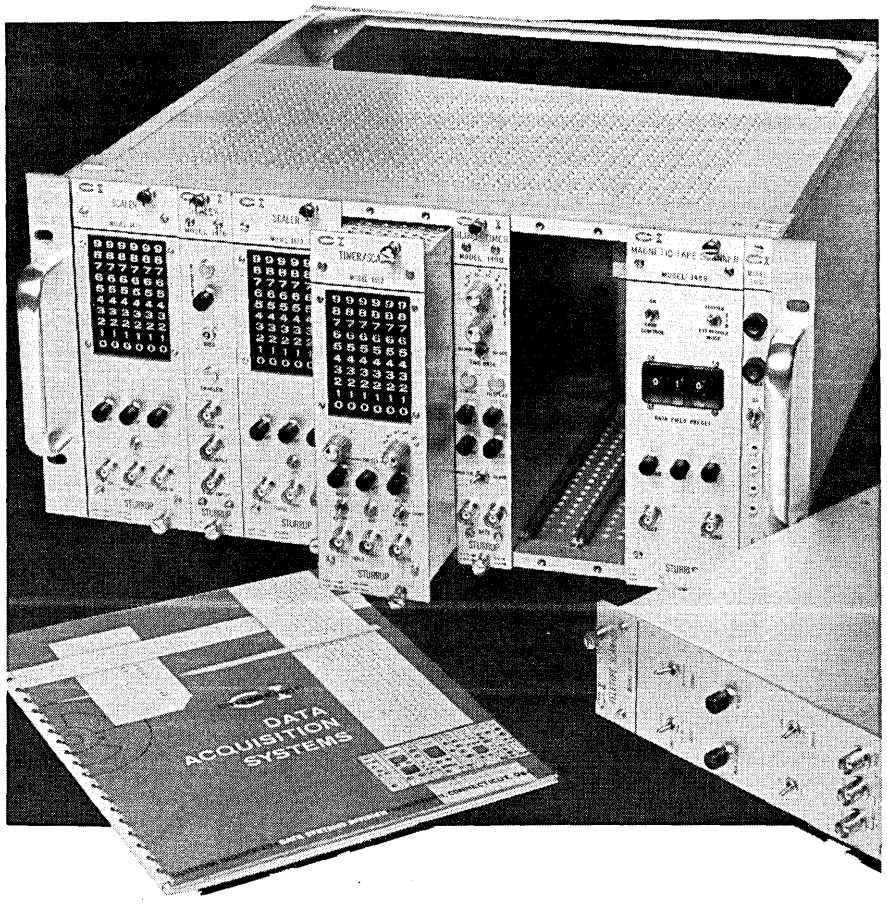
MINIATURE MOUNTING SOCKETS

Series 041-001 production mounting sockets for dual-in-line packages are molded in either nylon or polysulfone, and accept all standard 14 and 16 lead dual-in-line packages with rolled or flat leads and minimum lead lengths of 0.085". Spacing is 0.300" bewteen rows, 0.100" between lead centers. Operating temperature range of nylon sockets is —55° to 125°C; polysulfone operating temperatures range from —65° to 150° C.

A low body profile of only 0.160" above the P. C. board, including a standoff height of 0.020", permits greatest packing density between boards. Sockets can be mounted on a grid of 0.100" centers between them in both X and Y axes, affording maximum packing density and simplfying programming and operation of automatic wire wrapping machines. Barnes Corp., Lansdowne, Pa.

Circle No. 222 on Inquiry Card.

MODULAR DATA SYSTEMS...



TIME . . . COUNT . . . MEASURE . . . RECORD!

SUIT YOUR SYSTEM TO YOUR NEEDS!

The sensible module system that offers the industries' best price-performance package is value engineered with integrated circuit reliability. And system designed: Need teletype readout? Paper tape? Magnetic tape? Just add a readout module and you're on the air . . . no matter how many counters, timers, DVM's etc. are being read out. The readout module for complete interface to a standard teletype costs only **$850.**

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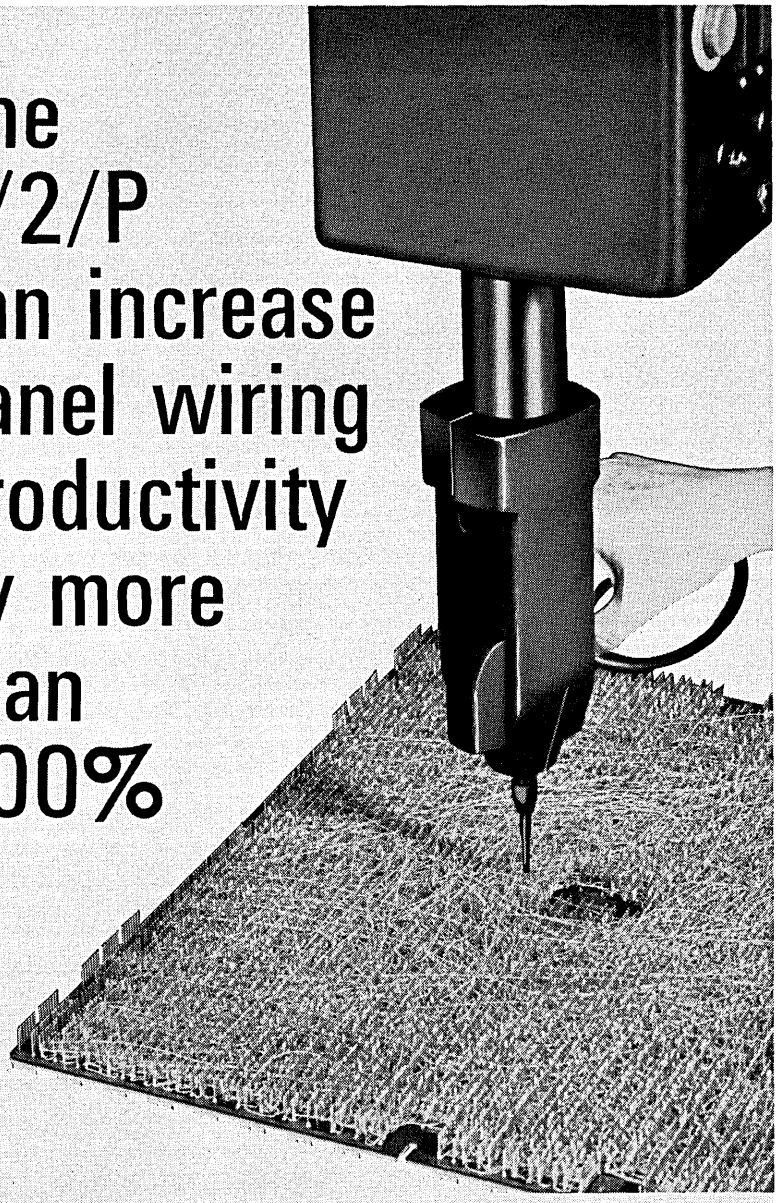
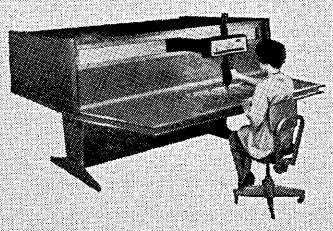
CANBERRA

The P/2/P can increase panel wiring productivity by more than 500%



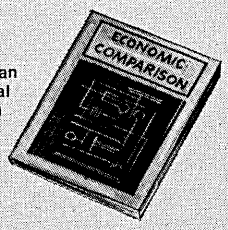
The P/2/P Wiring System combines numerical control, automatic indexing, and a human operator to form a highly efficient production facility for wire wrap or clip on termination wiring.

It provides the advantages of total automation (automatic travel and positioning of the tool) while eliminating the problems of hand wiring (slow production rates and human errors). The result—flawless panel assembly at less than ⅓ the hand wrap cost, and at ⅛ the initial investment required for a fully automatic system.



Write, wire, or call to arrange for a demonstration of the P/2/P Wiring System, and see these benefits for yourself.

"Economic Comparison", an objective survey of several wiring methods now in use, is yours on request.



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CIRCLE NO. 23 ON INQUIRY CARD

NEW PRODUCTS

LOGIC MODULE MOUNTING HARDWARE

This complete line of compatible mounting hardware virtually eliminates the mechanical and electrical interconnection problems that frequently occur in assembling a digital system. Products include a completely integrated set of system cabinets, swing frames for module mounting cases, and power supplies. The line offers packaged solutions to the problems of airflow control, sound-proofing, and DC power wiring. Three kinds of signal cabling are offered: coaxial cables, ribbon cables, and conventional logic wiring. This hardware is suitable for both large and small systems, but it is designed with particular emphasis on meeting the stringent requirements of large digital systems. Scientific Data Systems, Los Angeles, Calif.

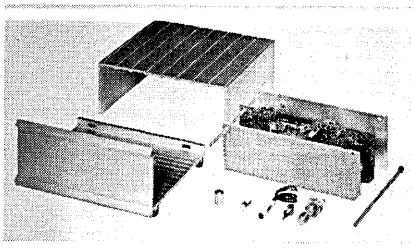
Circle No. 230 on Inquiry Card.

ANALOG MULTIPLIER/DIVIDER

The M201 is an encapsulated solid state FET type analog multiplier featuring true four quadrant multiplication, small size, and a dc to one MHz frequency response in both X and Y channels. The solid state module multiplies/divides/squares/square roots/ with no external adjustments or feedback networks required.

Pertinent specifications are: ±10 V—X and Y inputs (ac or dc), ±10 V output; 0.5% linearity; 1% total accuracy; X and Y input impedance of 10K ohms, output impedance of less than 1 ohm, and X and Y bandwidth of dc to 1 MHz. Power supply requirements are ±15 V at 100 mA, and module size is 3" x 2" x 0.625". Intronics Inc., Newton, Mass.

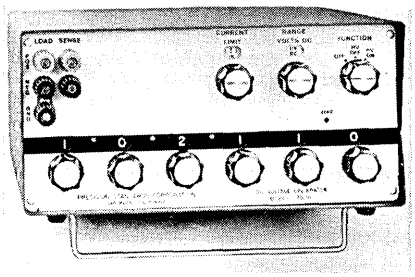
Circle No. 213 on Inquiry Card.



CIRCUIT PACKAGING KITS

Powering and packaging circuitry may no longer post a problem to the design enegineer with the Model E-1000 Designer's Kit, consisting of blank circuit boards, power supply and an enclosure. The enclosure is an aluminum cabinet that is formed to accept up to 5 circuit cards without any additional mounting hardware. Two interlocking extrusions are used in a novel fashion for which patent is pending. A selection of single or dual 110/220 V power supply cards are available. Outputs are well regulated DC at 3.3 or 5.2 V (IC logic) and/or any combination of voltages totaling 30 or less, such as ±15. Aritech Corp., Boston, Mass.

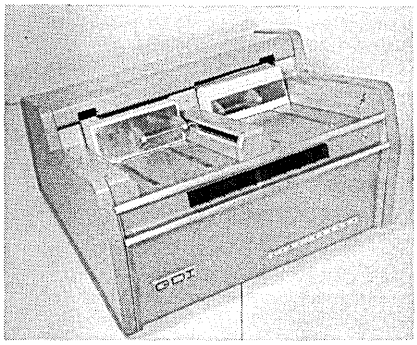
Circle No. 235 on Inquiry Card.



DC VOLTAGE CALIBRATOR

Model 460A, with a voltage range of 0 to 1111.10 Vdc provides output stability of 20PPM +10 μV per hour and 30PPM +20 μV per 200 hours. Having 5 decade switches and one single turn potentiometer, it features output resistance of 0.001 ohm or 0.0002E at dc. Output Current is 0 to 30mA, resolution is 1 μV and accuracy of ±01%. Completely solid state (with the exception of a high voltage pass tube) the Voltage Calibrator is chopper stabilized and features an ultra stable Zener reference and a current limit control. Ripple and noise are 100 μV RMS. Precision Standards Corp., Pasadena, Calif.

Circle No. 249 on Inquiry Card.



DATA CARD READER

Model 500 card reader is designed to provide a high-performance, low cost data card reader that will also accurately process damaged data cards. A unique vacuum pick finger is used to separate a single card from the input deck. It gently separates only one data card at each pick command, permits elimination of the sharp, restrictive throat edges which tend to further mutilate cards which are only slightly damaged and would otherwise be readable. The card track is nominally set at 4 to 6 card thickness and may actually be set at twice that. Specifications are: Speed: 600 CPM (nominal), Capacity: 1000 cards, Size: 26" wide x 20" deep x 12" high, Weight: 75 pounds including power supply. General Design, Inc., Melbourne, Fla.

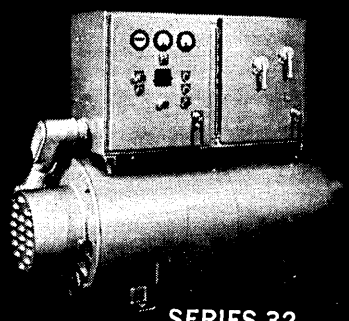
Circle No. 240 on Inquiry Card.

DRUM MEMORY

Medium scale integrated circuit logic has been utilized in the design of the Model 8403 drum memory system. The unit has been specifically designed to meet the data storage requirements for small computer systems. The basic memory configuration is equally adaptable to I/O or direct memory access applications. The drum memory provides a 1.1 million bit data base with 64 tracks and an average access time of 8.5 or 17 ms. Additional features include a nickel cobalt recording medium, individual flying heads, and a modular set of completely self-clocked, peak detecting, device-oriented electronics. Magnafile, Inc., Phoenix, Ariz.

Circle No. 238 on Inquiry Card.

400 CYCLE MG SETS



SERIES 32

This new series 32 brushless, synchronous 400 cycle MG set combines motor and alternator into a compact, two-bearing unit that provides a reliable and economical source of prime power for a variety of applications in the 5.0-250 KVA range.

FEATURES

- Low maintenance, long life
- No brushes or slip rings
- Class F winding insulation
- Bearings shielded and pre-greased for life
- 5 frame sizes
- Control options available

For new six page catalog describing in detail the series 32 write: Precision Power Group, American Electronics, Inc., 1600 E. Valencia Dr., Fullerton, California, (714) 871-3020, TWX 910-592-1256

Precision Power Group AEI AMERICAN ELECTRONICS INC.

Please rush literature on 400 Cycle Power.

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TITLE

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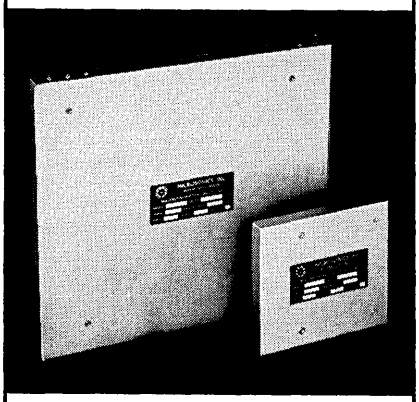
CIRCLE NO. 24 ON INQUIRY CARD

Computer Delay Line Storage Systems



Microsonics has proven capabilities and facilities to design and manufacture reliable computer delay line storage systems at high information rates (up to 100mc) which gives long term service in difficult environments of shock, vibration, and temperature. These systems have capability of handling digital signals for computer storage or analog information as in radar signal processing.

Ultrasonics computer storage lines, using fused quartz or zero T.C. glass, represent an ideal medium for high-speed computer storage up to 20mc rates.

Be it Computer Storage Systems; Digital Delay Lines; Magnetostrictive Delay Lines; or Variable and Tapped Delay Lines — Microsonics has the experience and capability to deliver both off-the-shelf and custom-designed systems for any specific operation.

Send for Microsonics' Brochure Nos. M735 and 5350.

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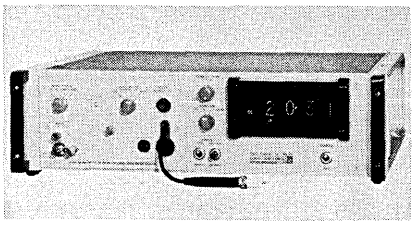
CIRCLE NO. 26 ON INQUIRY CARD

NEW PRODUCTS

BINARY/BCD/BINARY CONVERTERS

The Model BDC-1 accepts up to 24 bits of binary data from a computer or other source and converts it to 7 decimal decades in 1-2-4-8 BCD code. The conversion is initiated by an externally supplied trigger signal. The speed of the unit is such that a complete conversion is achieved in 12 μs (0.5 μs per binary bit). Applications include use with binary computers for driving BCD output devices such as printers or special purpose transducers such as frequency synthesizers or other decimal signal generation devices. The Model BDC-2 operates in the reverse to convert BCD data to binary form. Up to 7 BCD decades of data are accepted at the BCD-2 input and converted to a 24 bit binary output. Conversion speed is 14μs (2 μs per decade). Applications include using BCD input devices for computers such as digital voltmeters and counters. Curry, McLaughlin & Len, Inc., Syracuse, N. Y.

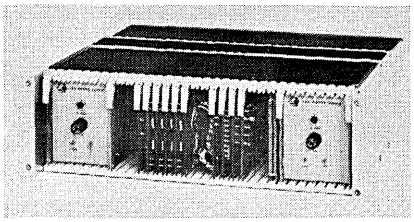
Circle No. 250 on Inquiry Card.



AC/DC DIGITAL VOLTMETER

Two plug-ins and one adaptor make the 1820 DVM a versatile general-purpose laboratory voltmeter. Voltage can be presented either in dB (re 100 μV) or volts; range is selected automatically. The decimal point is positioned and the proper measurement units are selected and displayed automatically. As a dc multimeter/uhf voltmeter, it measures ac (peak reading, calibrated in rms) and dc voltage and current, and resistance to $\pm 0.1\%$ accuracy in most cases. As an ac/dc millivoltmeter, it measures both ac (average) and dc with microvolt sensitivity. Direct current can be measured with picoampere resolution and, with a standard scope probe, alternating current can be measured with nanoampere resolution. With an adaptor added to either plug-in, conversion to a fully-balanced differential voltmeter with better than 100-dB common-mode rejection is possible. General Radio Co., West Concord, Mass.

Circle No. 248 on Inquiry Card.

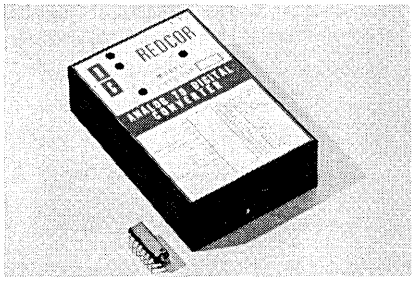


MEMORY SYSTEMS

The FI-3 series of coincident-current ferrite core memories offers storage capacities from 1K x 6 bits to 4K x 18 bits and features a 3-usec full cycle time (2-usec half-cycle time). Access time is one micro second maximum. The systems utilize integrated DTL circuits and silicon semiconductors mounted on PC cards. They are available with address register, sequential counter and memory retention. One timing and control card provides all necessary internal timing pulses.

Construction of the FI-3 is 3D organization, 4-wire, using 30-mil low temperature coefficient cores. Packaged to fit a 19-inch rack, the systems contain all electronics including (optional) +6 and −12 V power modules. Ferroxcube Corp., Systems Div., Englewood, Colo.

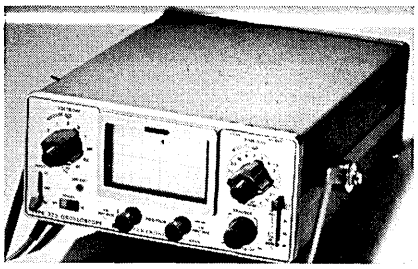
Circle No. 232 on Inquiry Card.



A-TO-D CONVERTER MODULE

This 12-bit analog-to-digital converter module offers a conversion rate of 20,000/second and up to 12-bit accuracy. Designated 770-750, the module is designed to be mounted on printed circuit boards. It is a high performance low-cost module for applications requiring 12-bits or less, with control inputs and digital outputs designed for DTL, TTL compatibility. Coding is available in offset binary, one's complement or two's complement. Signal inputs can be ± 10 V or 0 to 20 V. Other features include a low temperature coefficient of 0.002% per degree centigrade and a conversion time of 4 μ sec/bit. Package size is 2.3 x 3.5 x 1.10 inches. Redcor Corp., Canoga Park, Calif.

Circle No. 214 on Inquiry Card.



PORTABLE OSCILLOSCOPE

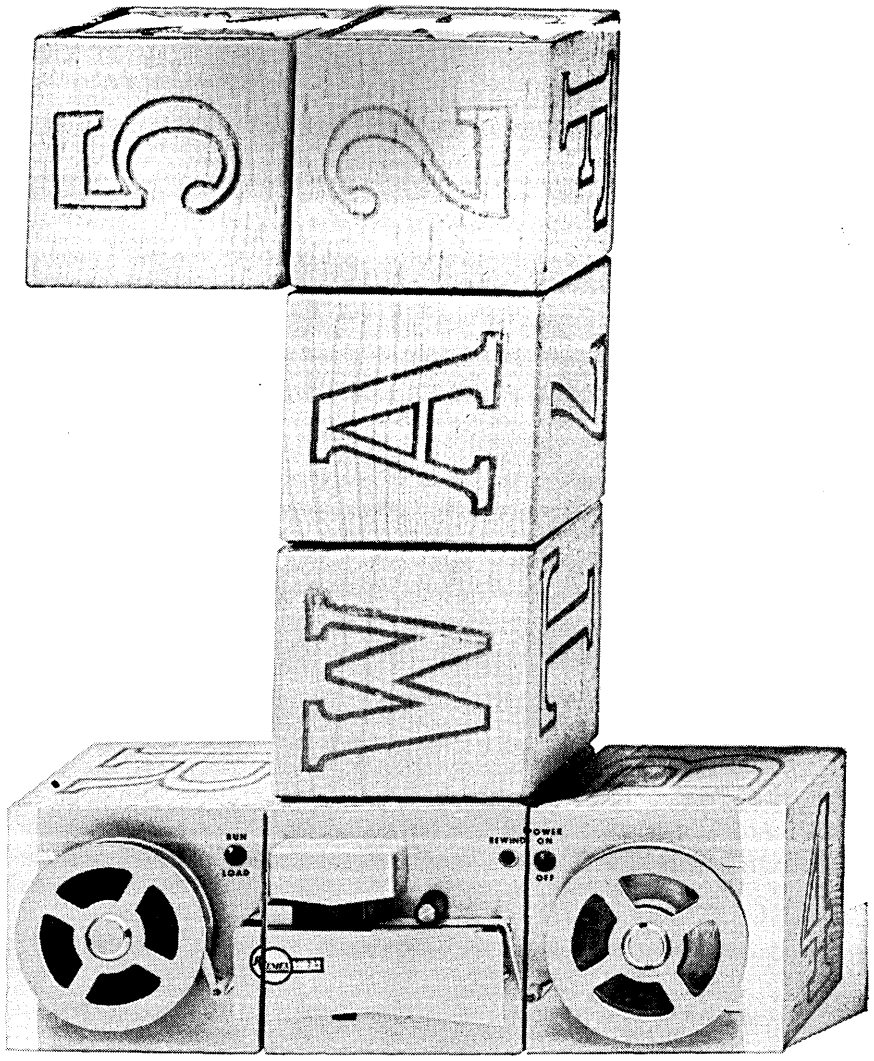
The Type 323 Sony-Tektronix all solid-state, 4 MHz portable oscilloscope permits the operator to choose ac, dc or internal batteries for instrument power. Internal rechargeable batteries provide up to 8 hours continuous operation. Power consumption from an external dc source (6 V to 16 V) is up to 4.5 W (typically 1.6W) and 14 W when powered from the ac line (115 Vac.) 4 MHz bandwidth is provided at 10 mV/div deflection factor. For low signal level applications 1mV/div deflection factor is provided with 2.75 MHz bandwidth. Sweep rates are 5 μs/div to 1 s/div. An X10 sweep magnifier extends the fastest sweep rate to 0.5 μs/div. The CRT uses a low power direct heated cathode, providing a useful display 2 seconds after turn-on. A 6 x 10 div (1/4 inch div internal non-illuminated graticule permits parallax free measurements. Dimensions are: depth 10 5/8", width 8 1/2", height 4 1/4" and weight approximately 7 pounds (including batteries). Tektronix, Inc., Beaverton, Oreg.

Circle No. 246 on Inquiry Card.

RACK MODULE POWER SUPPLY

H Series E case rack module power supplies offer a selection of voltages from 0.5 Vdc to 50 Vdc. Higher voltages up to 252 Vdc can be furnished upon request. Typical amperage level for the low voltage ratings go as high as 46 A at 50°C with no forced air required. Optional features are high stability to $\pm$0.001%/8 hrs or $\pm$120 μV/8 hrs, whichever is greater and to $\pm$0.005%/mo or $\pm$600 μV/mo, whichever is greater, temperature coefficient to $\pm$0.001%/°C or $\pm$120 μV, whichever is greater and built-in overvoltage protection that has a maximum voltage overshoot about the set level of 0.5V for a maximum time of 10μs. Remote programming at 200 ohms/ volt and remote sensing are standard on every unit. The unit size is 3 15/32" high, 17" long, and 19" wide for rack mounting. Dynage, Inc., Bloomfield, Conn.

Circle No. 227 on Inquiry Card.



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CIRCLE NO. 27 ON INQUIRY CARD

LITERATURE

Automatic Circuit Test Set

A 4-page brochure describes the Model AP-502 Automatic Circuit Test Set. The AP-502 is a portable tester that weighs less than 40 lbs. and can check cables, connectors and harnesses for continuity and insulation resistance at speeds of up to 1200 tests per minute. The brochure shows a photograph of the tester and gives complete physical and electrical specifications. Teleproducts, Inc., Moorestown, N. J.

Circle No. 312 on Inquiry Card.

Thick Film Power Driver Module

A 4-page engineering data sheet is available on a new line of power driver modules. The new data sheet provides maximum ratings and electrical specifications for all types. Case temperatures as functions of current and voltage are graphically displayed. Six schematics representative of potential application for the modules are included. Bendix Semiconductor Division, Holmdel, N. J.

Circle No. 305 on Inquiry Card.

Circuit-Board Laminate

The properties of the new 65M27 glass-epoxy circuit-board laminate are described in this 4-page illustrated folder. Properties specified include: volume resistivity, surface resistance, water absorption, dielectric breakdown parallel, dielectric constant, dissipation factor, flectural strength, arc resistance, solder blister, and peel strength. Westinghouse Industrial Micarta Division, Hampton, S. C.

Circle No. 303 on Inquiry Card.

Data Acquisition Systems

This brochure describes, in detail, new systems for digital data acquisition. Components can now be interconnected to make up either highly sophisticated systems with advanced solid state components and controls, or more economical versions using less complex servo null-balance equipment. These systems provide monitoring, automatic scanning, recording and limit detection for a wide range of industrial applications. Howell Instruments, Inc., Fort Worth, Texas.

Circle No. 315 on Inquiry Card.

Hybrid Integrated Circuits

This brochure entitled "A Designer's Guide To Crystalonics Hybrid Microcircuits" includes information on hybrid and monolithic integrated circuit comparisons, techniques used to translate a customer's circuit requirement into a breadboard, production processes and controls, quality assurance and reliability stress processing procedures, and helpful hints on designing and ordering hybrid ICs. Crystalonics, a Teledyne Co., Cambridge, Mass.

Circle No. 320 on Inquiry Card.

Panel Meters

Ranges, prices, resistances, photographs, diagrams and mounting specifications for DC and AC meters within the 1½-inch, 2½-inch, 3½-inch and 5-inch sizes in both taut-band and pivot-and-jewel construction are presented in a 16-page two color booklet. Catalog 35F also lists models, sizes, voltages and prices for elapsed-time indicators, VU meters and null indicators. Honeywell Precision Meter Division, Manchester, N. H.

Circle No. 307 on Inquiry Card.

Plug-In Power Supplies

Over 62,000 different types of AC to DC plug-in power supplies are listed in a new 16-page catalog. Included are regulated and unregulated supplies, singles and duals, and models for operation in various temperature ranges. The literature also describes panel assemblies for rack mounting power supplies, in addition to a laboratory power supply with built-in indicating meter, and other power supply accessories. Acopian Corp., Easton, Pa.

Circle No. 301 on Inquiry Card.

Isolation Transformers

This bulletin features 7 new Laboratory series power line/noise isolation transformers from 100 to 2500 watts. It illustrates the double shielded Electro-Guard series transformers having less than .001 pf leakage capacitance between primary and secondary coils. The Lab-line transformer insures 170 dB of common mode isolation and attenuation of troublesome ground loop currents. James Electronics Inc., Chicago, Ill.

Circle No. 308 on Inquiry Card.

High Speed Integrated Circuits

A 100+-page loose-leaf bound brochure includes current data sheets for 56 new high-speed logic MECL II integrated circuits (29 different functions). Each data sheet contains application "ideas" for that circuit function. Data pertinent to all the MECL families of integrated circuits is quickly categorized for instant reference in this easy-to-use, stiff-covered all-in-one data storage file. Motorola Semiconductor Products Inc., Phoenix, Ariz.

Circle No. 310 on Inquiry Card.

Bar Indicator Switches

This 2-page catalog sheet illustrates and technically describes three thumb-wheel and pushbutton switches which are directly connected to a 7-bar indicator. Included are 6 dimensional drawings, electrical ratings, electrical and mechanical characteristics, environmental characteristics and quality control standards. Chicago Dynamic Industries, Inc., Precision Products Division, Chicago, Ill.

Circle No. 300 on Inquiry Card.

CRT Displays

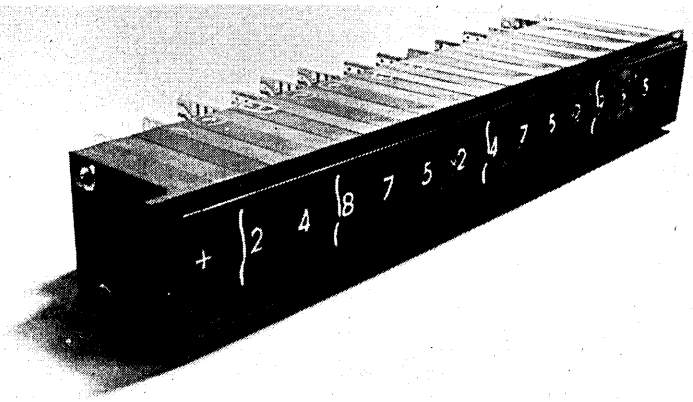
Cathode ray tube displays is the subject of 4 important articles presenter in this 12-page booklet. The articles give a comprehensive picture of present status of displays, opinions of leading manufacturers on raster-scan techniques, technical considerations which are influencing CRT display design, description of a CRT console for remote computing, and the use of magnetic disc with TV monitors for low-cost graphic displays. Each article contains illustrations, some with complete schematics of the systems described. Data Disc, Inc., Palo Alto, Calif.

Circle No. 304 on Inquiry Card.

Tape Readers/Reelers

A complete reader line including "through-the-tape" and reflected light readers and associated tape handling equipment are illustrated in an 8-page brochure (GEA-8492). Products are designed for use in digital data handling, communications, numerical control, phototypesetting, ground support and other tape-programmed systems. Specification and application information such as capability, size, and special features appear on the same page as the product illustration. General Electric Company, Philadelphia, Pa.

Circle No. 311 on Inquiry Card.



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With a Digitran thumbwheel switch, you can dial in any number between zero and the national debt. Fast, easy, and error-free. Digitran's modular design lets you program any number of digits.

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CIRCLE NO. 28 ON INQUIRY CARD

ELECTRONICS ENGINEERS

You can make tomorrow's memories today. How? Come to Lockheed Electronics Company in Los Angeles...where the world's fastest 2½D memory system is already in production. Lockheed engineers conduct research in all phases of memory systems technology. Not only do they develop advanced memories, but also what memories are made of—the finest printed circuits, stacks and ferrite cores. With such a large number of successful projects underway, Lockheed Electronics has become the country's fastest-growing company in the memory system field. ☐ To continue growing, Lockheed needs talented engineers in logic design, circuit design and magnetic memory design. There are also openings for engineers with managerial experience. ☐ Tomorrow's memories can't wait. Send your resume today to Professional Employment Group, Lockheed Electronics Company, 6201 East Randolph Street, Los Angeles, California 90022. Lockheed is an equal opportunity employer.

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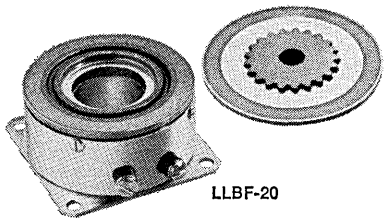
CIRCLE NO. 901 ON INQUIRY CARD

APILON®- FACED COMMERCIAL CLUTCHES/BRAKES



LLBF-20

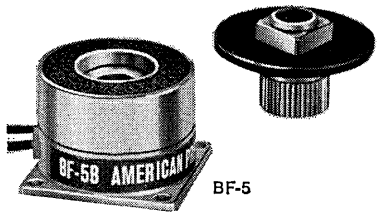
(½ actual size)

American Precision Industries' Apilon®-faced electro-magnetic clutches and brakes, at rated loadings, have life expectancies of 100 million cycles. The unique Apilon® friction facing outlasts conventional types 10 to 1, virtually eliminating the need to replace facings. An added benefit — no unsightly or contaminated wear products.

Apilon® ceramic friction-faced clutches and brakes are ideally suited for applications where unusually severe loads are placed upon the product for long durations, such as in high-speed printers or in tape tensioning devices where continuous slippage occurs.

Units are available in ratings of 2 lb. in. to 70 lb. in. of torque, in sizes of 1" to 2⅝" body diameter.

HIGH-TORQUE COMMERCIAL CLUTCHES/BRAKES



BF-5

(actual size)

A low-cost line of commercial clutches and brakes is also available for less demanding applications.

These units can transmit torque without burnishing and are available in the same size and torque ratings as the Apilon® line. Standard coil voltage, 24 VDC. Other voltages available at no additional charge.

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CIRCLE NO. 31 ON INQUIRY CARD

Test Equipment

A 1968 forty-seven page, multi-colored catalog documents systems and individual products. It is broken down into 6 basic equipment sections and one general section. The catalog contains detailed specifications and prices on each product and a list of E-H publications and general Corporate information. E-H Research Laboratories, Inc., Oakland, Calif.

Circle No. 306 on Inquiry Card.

Plastic Encased Transistors

Twenty-seven new types of plastic-encased transistors, making 92 in all are summarized in an Econoline Short Form Catalog (CN-200B1). Also included in the new catalog are 4 differential amplifiers, 2 complementary pair transistors, and 5 dual transistors, all in a unique 6-lead plastic package. Sprague Electric Co., North Adams, Mass.

Circle No. 319 on Inquiry Card.

Semiconductor Heat Sinks

Catalog #68-B-2 covers a line of heat sinks for TO-5 transistors. This new product is known as the 2225 Series, and is a series of finned, 1 piece press-on units for circuit board applications. Catalog #68-B-2 contains the following: Outline drawings, performance curves, prices, materials and finishes, and application information. Thermalloy Company, Dallas, Texas.

Circle No. 309 on Inquiry Card.

IC Core Memories

Key operating specifications for a line of integrated circuit core memories, are summarized in a new brochure. The ICM-500, ICM-47, ICM-40 and ICM-42 core memories are described. Full cycle times for the systems vary from 600 nanoseconds to 1.5 microseconds. Word capacities range from 1K to 32K words per memory module. Honeywell, Computer Control Division, Framingham, Mass.

Circle No. 317 on Inquiry Card.

Paper Tape Readers

Paper tape readers are the subject of a 4-page brochure which illustrates and describes 11 reader models, and points out general applications. The brochure also explains and illustrates in isometric view the basic tape feed system, shows the method of tape sensing, and lists mechanical and electrical specifications. Ohr-Tronics, Inc., Montvale, N. J.

Circle No. 316 on Inquiry Card.

DTL Integrated Circuits

Five new data sheets describe a line of 10 DTL integrated circuits. The 4-page, 2-color data sheets contain more than 80 technical illustrations, charts, and graphs and provide comprehensive information on device specifications, test conditions and limits, and typical dynamic characteristics. Pertinent application information is also presented. Stewart-Warner Microcircuits, Inc. Sunnyvale, Calif.

Circle No. 318 on Inquiry Card.

Data Communication Equipment

A new folder 3C8 illustrates a line of data communication products, and provides a condensed description of the MODEM 4400 data sets and companion equipment. The folder includes a brief technical summary of three models of data sets, specialized voice adapters for voice/data transmission and transmission test equipment. Milgo Electronics Corp., Miami, Fla.

Circle No. 314 on Inquiry Card.

DCL Integrated Circuits

The specifications, usage rules and applications for the Designer's Choice Logic (DCL) Series 8000 line of IC's are covered in a 120-page handbook. The handbook is heavily illustrated with schematic drawings, package configurations, performance curves in addition to a number of charts and tables involved with testing and design considerations. Signetics Corp., Sunnyvale, Calif.

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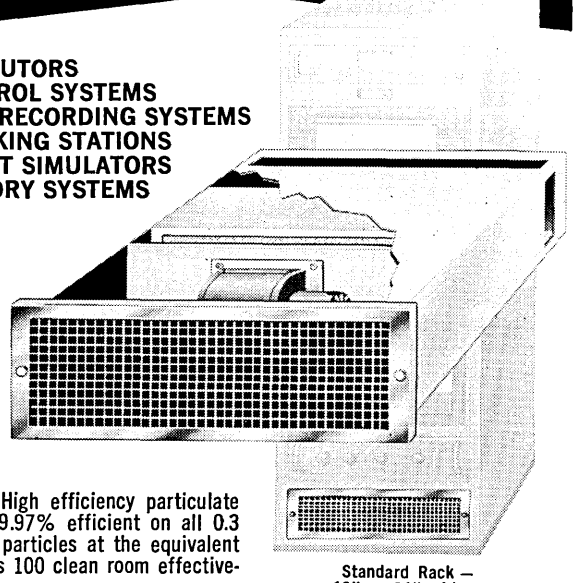

(HEPA) High efficiency particulate filter 99.97% efficient on all 0.3 micron particles at the equivalent of Class 100 clean room effectiveness.

Standard Rack — 19″ or 24″ wide x 20″ deep x 7″ to 12½″ high.

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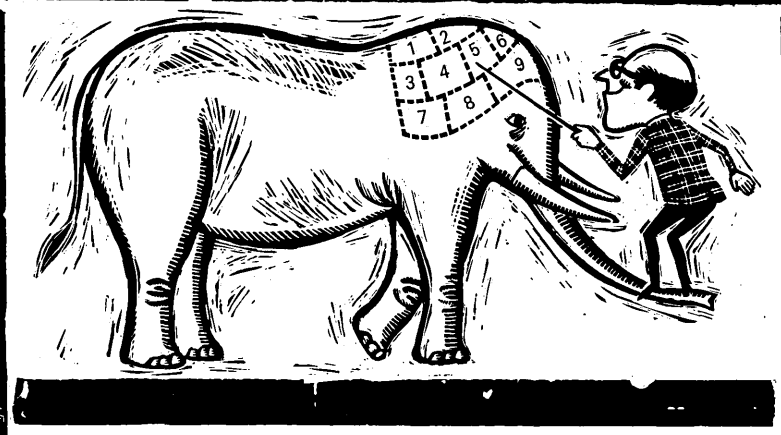

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We're looking for a number of EE's experienced in system and circuit design associated with a wide spectrum of advanced military memory systems. Your background should include a minimum of four years in one or more of these areas: military memory system design; core or film memory circuit design; semiconductor memory system and circuit design; 2½ D circuit design. Think about it. Then write Jim Anderson.

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NEW

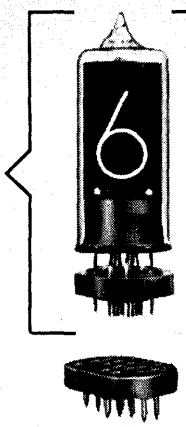
high-brightness NIXIE® tubes. designed for tomorrow, delivered today.

TYPE B-5750

LOW COST:
$3.95 each in 1000 quantities.

HIGH BRIGHTNESS:
time sharing up to 12 digits, or for DC operation.

TUBE SIZE:
0.53″ diameter; 1.5″ height.

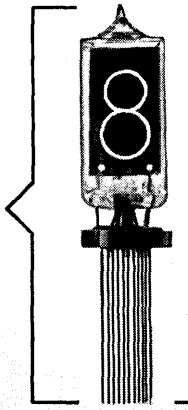


TYPE B-5855

LOW COST:
$4.35 each in 1000 quantities.

ULTRA-HIGH BRIGHTNESS:
time sharing more than 12 digits, or for DC operation.

MINI TUBE SIZE:
0.51″ diameter; 1.35″ height.



TUBES SHOWN ACTUAL SIZE

TIME-SHARING OPERATION:
like numerals can be driven in parallel, reducing driver costs, and without sacrifice of brightness.

IC-COMPATIBLE PIN CONFIGURATION:
dual-inline layout designed for IC decoder/drivers.

OPTIONAL PIN CONFIGURATION:
conventional plug-in type for socket mounting, or flying leads for direct soldering.

COMBO PIN SPACER/LEAD STRAIGHTENER:
simplifies PC-board and/or socket insertion.

DECIMAL POINTS:
positioned left and right, independently operable.

CHARACTER HEIGHT: 0.5″

MINI-SIZE, LOW-COST SOCKETS:
for DC or time-sharing operation.

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like all ultra-long-life NIXIE tubes.

LONGEST STATIC LIFE:
for demanding applications.

SPECIAL-CHARACTER TUBES:
+/− tubes available from stock. Alpha/special-character tubes made to order.

MOST COMPLETE HARDWARE BACK-UP:
low-cost IC decoder/drivers available off-shelf. Custom assemblies at production costs through modular design.

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Burroughs

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By engineering many moving parts out of the Tally photo reader, maintenance has been minimized and performance maximized.

The parts we took out—gears, belts, pulleys, and pinch rollers—put reliability into Tally photo readers.

Tally faced the moving parts dilemma by replacing most of them with three low-inertia servomotors to create a fast, smooth, quiet and more reliable photoelectric tape reader. The motors attach directly to the capstan wheel and the reeling, eliminating all troublesome gears, belts, pulleys and pinch rollers. No adjustments are necessary. Maintenance is greatly reduced and accurate read out over long periods of time can be expected.

Tape movement through the read head is in exact accordance with the rotation of the motor armature. The high speed response of the motor allows a great variety of reading operations by merely controlling the current applied to the motor terminal.

It's fast. Searches at 1,000 characters per second. Reads synchronously at any rate up to 500 char/sec and stops before the next character. Reads asynchronously under control of external signals at any rate up to 200 char/sec. Runs in either direction in all modes.

It's easy on the tape. The smooth, quiet action of the servo-controlled reels eliminates tape breakage, reduces tape wear and prevents reading errors.

It's offered with many options. Many optional configurations are available, including recessed mount, flush mount, integral reeling, external reeling, and fully militarized construction.

For complete information contact Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. Phone (206) MA 4-0760. In the U.K. and Europe address Tally Ltd., 6a George Street, Croydon, Surrey, England. Phone: 01-686-6836.

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