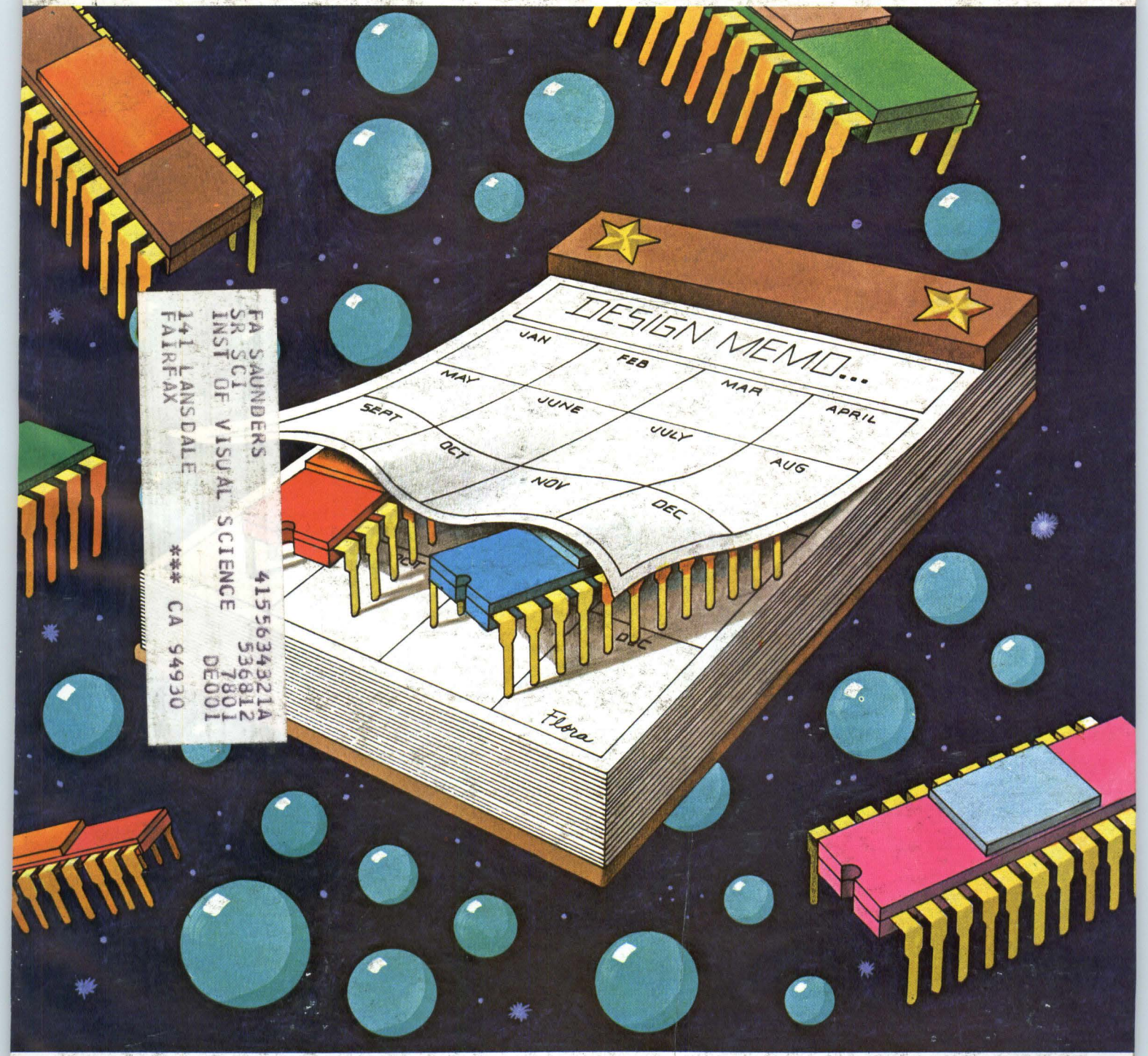
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

DECEMBER 1979



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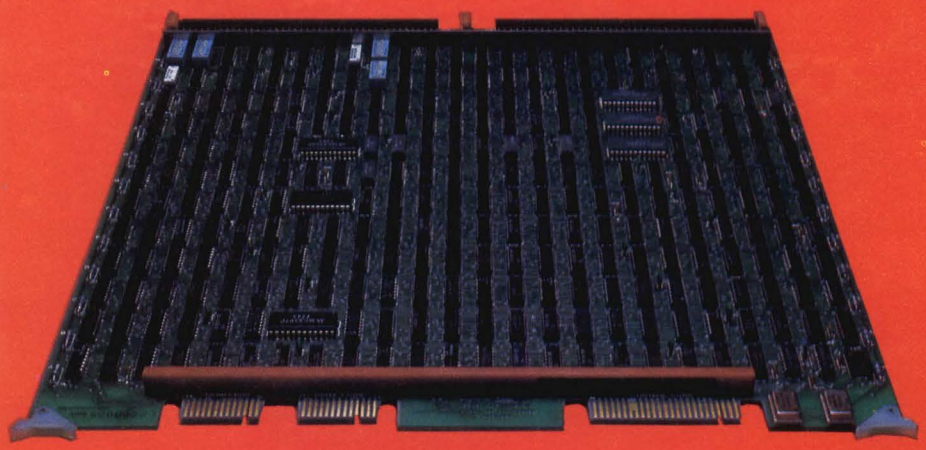

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CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

DECEMBER 1979

VOLUME 18, NUMBER 12

DEPARTMENTS

FEATURES

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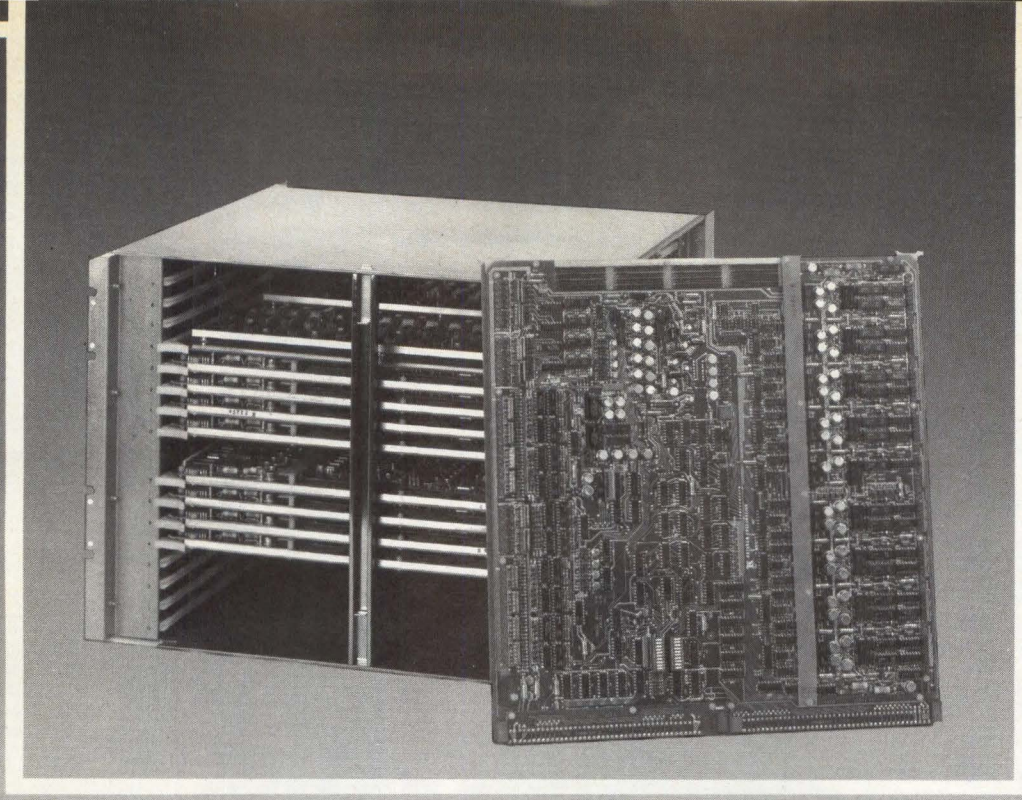

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CALENDAR

CONFERENCES

JAN 7-10—ATE Seminar/Exhibit and Test Instruments Conf, Pasadena Convention Ctr, Pasadena, Calif. INFORMATION: Karen Knope, ATE Seminar/Exhibit or Test Instruments Conf, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

JAN 9-11—AFCEA Western Conf and Exposition, Disneyland Hotel, Anaheim, Calif. INFORMATION: Judith H. Shreve, Armed Forces Communications and Electronics Association, One Skyline Plaza, 5205 Leesburg Pike, Suite 300, Falls Church, VA 22041. Tel: 703/820-5028

JAN 15 AND FEB 6—Invitational Computer Conf, Orange County, Calif and Ft Lauderdale, Fla. INFORMATION: B. J. Johnson & Assoc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

JAN 28-30—Communications Network '80, Sheraton Washington Hotel, Washington, DC. INFORMATION: William Leitch, The Conference Co, 60 Austin St, Newton, MA 02160. Tel: 617/964-4550

JAN 29-31—Aerospace and Electronic Systems Winter Convention (WINCON), Sheraton Universal Hotel, North Hollywood, Calif. INFORMATION: Phillip G. Halamandaris, Gould Inc, Navcom Systems Div, 4323 Arden Dr, El Monte, CA 91731. Tel: 213/442-0123, X602

JAN 30-FEB 1—MIMI'80 Asilomar (Internat'l Sym on Mini and Microcomputers), Asilomar Conf Grounds, Pacific Grove, Calif. INFORMATION: The Secretary, MIMI'80 Asilomar, PO Box 2481, Anaheim, CA 92804. Tel: 714/774-6144

FEB 12-14—Data 80 Data Communications Conf and Exhibition, Harbour Castle Hilton Hotel and Convention Ctr, Toronto, Ontario, Canada. INFORMATION: Whitsed Publishing Ltd, 2 Bloor St W, Suite 2504, Toronto, Ontario M4W 3E2, Canada

FEB 13-15—Internat'l Solid State Circuits Conf (ISSCC), Hilton Hotel, San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 19-22—Southwestern Computer Conf, Myriad Convention Ctr, Oklahoma City, Okla. INFORMATION: Oklahoma State U Technical Institute, 900 N Portland, Oklahoma City, OK 73107. Tel: 405/947-4421

FEB 19-21, FEB 26-29, AND MAR 5-7—TechEx America, Europa, and Asia, Atlanta, Ga; Copenhagen, Denmark; and Singapore, Republic of Singapore. INFORMATION: Dr Dvorkovitz & Assoc, PO Box 1748, Ormond Beach, FL 32074. Tel: 904/677-7033

FEB 25-28—COMPCON Spring, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

MAR 4-6—Internat'l Zurich Sem on Digital Communications, Zurich, Switzerland. INFORMATION: Prof P. E. Leuthold, Eidgenossiche Technische Hochschule Zurich, Institut fur Hochfrequenztechnik, Sternwartstrasse 7, Zurich, Switzerland

MAR 14-16—West Coast Computer Faire, Civic Auditorium and Brooks Hall, San Francisco, Calif. INFORMATION: Computer Faire, 333 Swett Rd, Woodside, CA 94062. Tel: 415/851-7075

MAR 17-19—Industrial Control & Instrumentation Applications of Mini & Microcomputers (IECI), Sheraton Hotel, Philadelphia, Pa. INFORMATION: Dr Paul Russo, RCA Labs, Princeton, NJ 08540. Tel: 609/452-2700, X3234

MAR 17-20—Interface '80, Miami Beach Convention Ctr, Miami Beach, Fla. INFORMATION: Peter Young, Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

MAR 19-21—Design Technology for Computers & Datacomm Systems '80, Disneyland Hotel Convention Ctr, Anaheim, Calif. INFORMATION: Industrial & Scientific Conf Management, Inc, 222 W Adams St, Chicago, IL 60606. Tel: 312/263-4866

MAR 24-28—Eurocon'80 (European Conf on Electrotechnics), Stuttgart, Germany. INFORMATION: Prof Dr W. E. Proebster, IBM Deutschland GmbH, Postfach 80 08 80, D-7000 Stuttgart 80, Germany

MAR 31-APR 2—Internat'l Computer Aided Design Conf and Exhibition, Metropole, Brighton, England. INFORMATION: The Organisers, CAD 80, IPC Science and Technology Press Ltd, PO Box 63, Westbury House, Bury St, Guildford, Surrey GU2 5BH, England

APR 16-17—Peripherals 80, Bloomsbury Ctr, London, England. INFORMATION: Iliffe Promotions Ltd, Dorset House, Stamford St, London SE1 9LU, England

MAY 6-8—Internat'l Sym on Computer Architecture, La Baule, France. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

JUNE 3-5—Networks 80, Bloomsbury Centre Hotel, London, England. INFORMATION: Online, Cleveland Rd, Uxbridge UB8 2DD, England

SHORT COURSES

JAN 8-10—Automatic Test Equipment: How to Select It—Apply It—Manage It; Introduction to Digital Testing; AND MAR 6-7—Advanced ATE Technology and Management, Pasadena, Calif; and Atlanta, Ga. INFORMATION: Kate Fitzgerald, ATE Courses, Benwill Publishing Corp, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

JAN 16-18—Computer Communication Systems and Networks, JAN 21-25—Digital Signal Processing, JAN 28-FEB 1—Structured Programming and Software Engineering, FEB 6-8—Modular Software Design, AND MAR 10-12—Recent Advances and Current Trends in Data Networks, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel: 202/646-6106

JAN 17-19; FEB 7-9; AND MAR 3-5—Hands-On Microprocessor Peripherals Workshop, Arlington, Va; Jacksonville, Fla; and Atlanta, Ga. INFORMATION: Paul A. Willis, Polytechnica Institute, PO Box 29, Arlington, VA 22210. Tel: 703/533-2826

FEB 4-5, MAR 5-6, AND APR 9-10—Microprocessors: Hardware, Software, and Application, Worcester Polytechnic Institute, Worcester, Mass; Holiday Inn, Boston, Mass; and Worcester Polytechnic Institute, Worcester, Mass. INFORMATION: Ginny Bazarian, Office of Continuing Education, WPI, Worcester, MA 01609. Tel: 617/753-1411

FEB 11—Fundamentals of High Resolution Lithography, AND FEB 12—Integrated Circuit Technologies for the 1980s, Palo Alto, Calif. INFORMATION: Continuing Education in Engineering, University of California Extension, 2223 Fulton St, Berkeley, CA 94720. Tel: 415/642-4151

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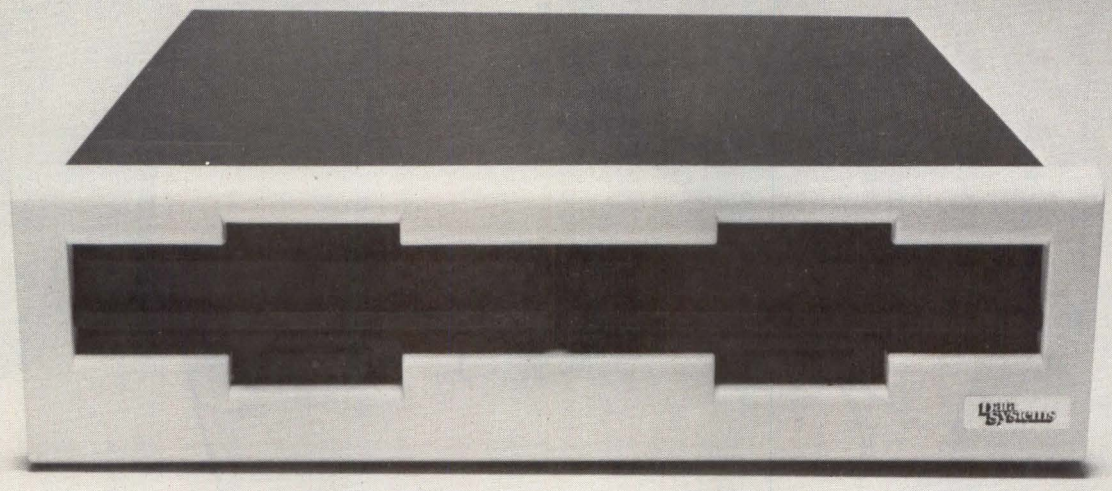
THE DSD 440. TOTAL DEC® RX02 COMPATIBILITY,



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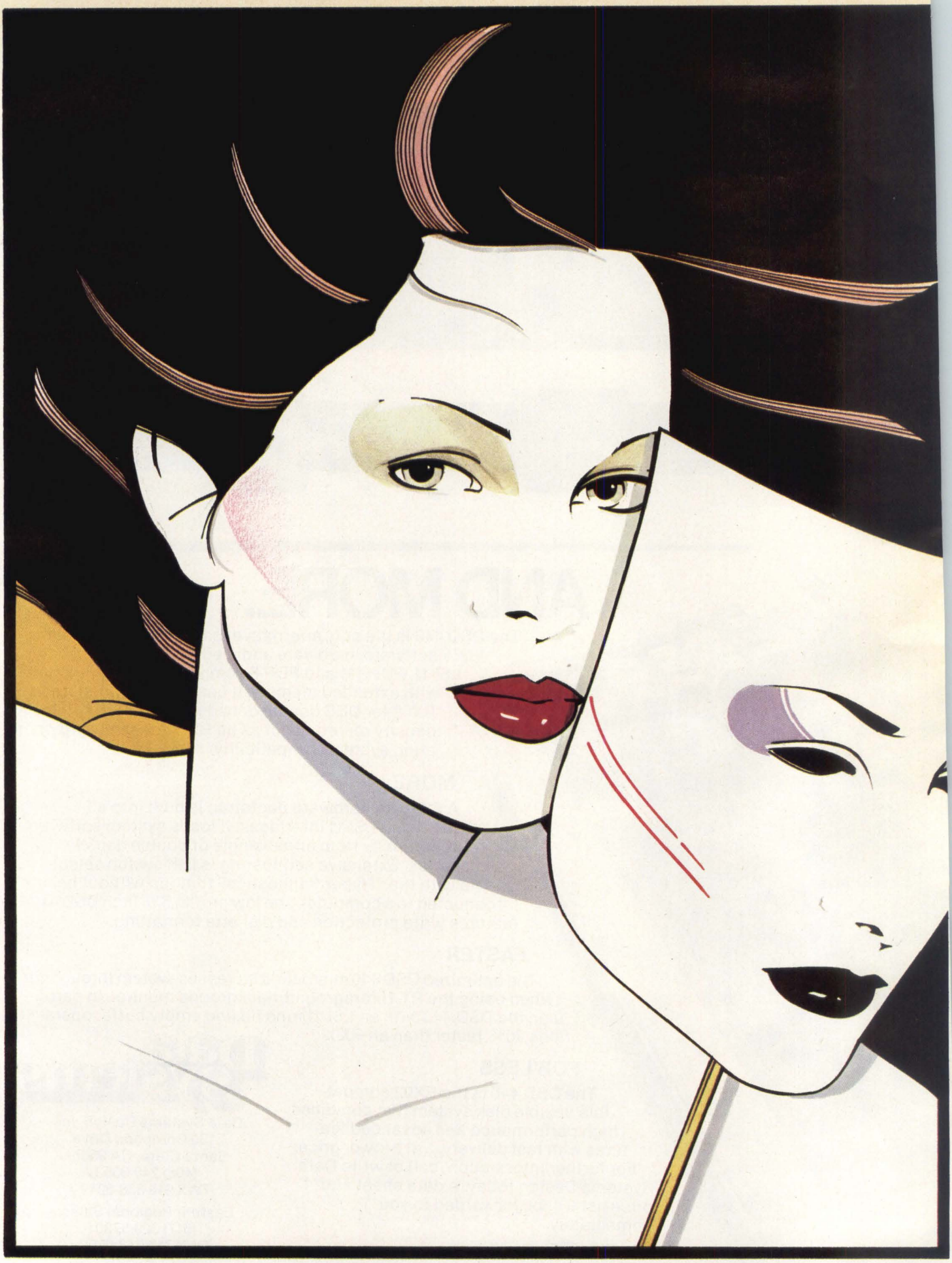

8088: Twin Reality

Intel unveils the ultimate 8-bit CPU. Powerful. Practical. Beneath the surface, the heart of an 8086.

True beauty is never skin deep. Such is the case with our new 8088 microprocessor. On first impression, you'll see a powerful third generation CPU with the convenience and practicality of an 8-bit bus. Look closer and you'll discover the remarkable 16-bit internal architecture, megabyte addressability and advanced instruction set of our 8086.

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When we introduced the 8086 family more than 18 months ago we called it a new beginning, a microcomputer system architecture so advanced it would deliver a dramatic increase in system sophistication, performance and expandability. Now the 8088 delivers the same performance increase for 8-bit designs.

8088: Designed with reality in mind.

We built the 8088 to perform in the type of systems you're designing today and well into the future, too.

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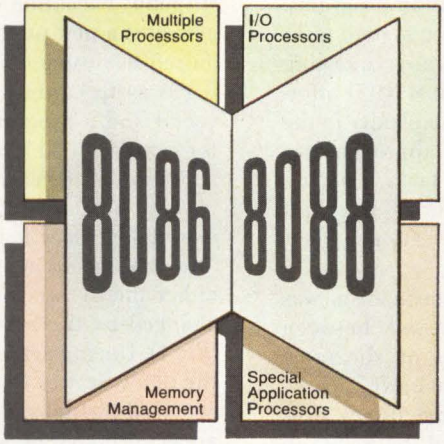
Its byte-wide orientation and extensive string-handling instructions give it unprecedented capabilities—block moves, string comparisons, data scans and translations—that make the 8088 the ideal CPU for your business-oriented applications as well.

The 8088 addresses up to a megabyte of memory, in 64K byte segments. Segmentation and efficient register utilization enabled us to build in the capability for such minicomputer-like features as instruction pre-fetch, re-entrant code, position independent code and dynamic relocation. And 64K I/O space and indirect I/O simplify programming even further.

Make your own reality.

Any way you look at it, the 8088 is a tantalizing prospect. If you are upgrading your 8080, 8085 or Z80 design, the basic 5MHz 8088 delivers two to five times



the performance, yet preserves your entire hardware investment. And with the CONV-86 code converter and PL-M/86 compiler, your software can be easily upgraded, too.

The 8088's 100% software compatibility with its 16-bit twin ensures the smoothest possible transition to any future 16-bit processor needs.

Its 16-bit internal architecture and elegant instruction set are super efficient for implementing high-level, block-structured languages such as Pascal or PL-M/86.

Etched into its HMOS* circuitry, the 8088 allows compatible interface to multiprocessing configurations with the 8086 and Intel's new generation of I/O processors, math processors, memory managers and distributed intelligence configurations.

For more space—and cost-sensitive applications, though, four other readily available Intel® bus multiplexed peripherals combine with the 8088 for a complete 8-bit system of unprecedented performance.

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Because the 8088 shares the instruction set and object code of her more powerful sister, the same Intellec® development system and software package you use for 8086 program development fully support the 8088, too.

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*HMOS is a patented Intel process.

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CIRCLE 8 ON INQUIRY CARD

COMMUNICATION CHANNEL

HARDWARE INTERRUPT STRUCTURE FOR A DISTRIBUTED PROCESSING SYSTEM

R. J. Gallagher International Business Machines Corporation, Kingston, New York

Efficient management of a system operating in a multiprogramming system environment requires that work be performed on a priority basis: high priority system error handling, medium priority I/O device and communication services, and medium to low priority application programs. In addition, priorities of many other operating system tasks vary with the priority of the application program requesting service. One objective in the design of the IBM 8100 information system[1,2] was to avoid unnecessary complexity in the operating system. Therefore, a hardware approach was undertaken to control priority management tasks. This approach led to the development of a priority interrupt mechanism allowing for program, I/O, and system error interrupts.

In order to conserve interrupt levels, a mechanism was also required to allow control to be passed between operating system and application programs on the same priority interrupt level. This objective was achieved by using a dual program status vector facility. Eventually, this mechanism was also used to pass control between an operating system dispatcher and other operating system tasks.

PSV Swap Procedure

Hardware for either of the two available processors in the information system, the 1500-ns 8130 or the 800-ns 8140, provides eight priority interrupt levels. Dual program status vectors are associated with each level. Each program status vector (PSV) and an associated address control vector (ACV) define a set of program facilities. With this arrangement, the operating system can assign two programs to each level. Typically, one of these programs acts as a dispatcher.

At any given time, only one PSV and its associated ACV are being used to control the execution of instructions. The remaining PSVs and ACVs are held in reserved areas waiting to be activated by PSV swap hardware that, activated by either the priority interrupt mechanism or the dual PSV facility, causes a PSV swap to take place. To do this, the processor suspends execution of the currently activated program and activates a new program. Hardware saves all parameters required to resume execution of the suspended program.

PSV swap hardware contains a current priority level (CPL) vector and a program activation vector (PAV). The CPL vector contains a 3-bit number that indicates the priority interrupt level of the currently active program. Which of the two PSVs on a priority interrupt level is to be activated when a swap takes place is indicated by the 8-bit PAV.

Following suspension of the currently active program, either the CPL vector or the PAV bit for the current level is changed by the hardware before an activation takes place (Fig 1). During activation, the hardware uses the contents of the CPL vector to find the appropriate PAV bit. Both vectors are used to find the PSV/ACV registers in either of two save areas, primary or secondary. Hardware then fetches the PSV/ACV vectors and places them in the active PSV/ACV registers. This procedure defines all the parameters required for the program's execution, such as register set, condition indicators, address space, and instruction address.

This design places save and activate functions completely in hardware. It not only has the advantages of speed and programming simplicity, but also provides a mechanism that prohibits an application program from tampering with saved PSVs and ACVs.

Dual PSV Facility

Dual PSVs on each interrupt level are called "primary PSV" and "secondary PSV." Each contains a field that is used to

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Centronics' new Model 730 miniprinters shatter the rules of the game. On price, performance, features, and support, Model 730 is a clear winner—no other miniprinter can compete! Here's why it's the newest sensation of the circuit...

ADVANTAGE: FLEXIBILITY Model 730's exclusive three-in-one paper handling system gives you built-in flexibility. Payroll checks on pre-printed continuous forms. Inventory listings on fan-fold. Direct mail on company letterhead. General information on roll paper. The 730 does it all.

ADVANTAGE: QUALITY Model 730 sets new quality standards for miniprinters. Centronics' innovative technology fits high-end features into a compact (10 lbs.), quiet unit. Its 7 x 7 dot matrix produces clear, clean characters at 100 cps. Simple operational design ensures unsurpassed reliability.

ADVANTAGE: LOW COST OF OWNERSHIP Model 730's low total cost of ownership only starts with its attractive purchase price. It also provides more applications opportunities with minimum investment. Our simple design employs fewer parts for higher reliability. That means maximum uptime, plus easier training and service requirements.

ADVANTAGE: INTERNATIONAL CAPABILITY International models of the 730 can print in any of six languages, and are available in all standard international power requirements, so it's ready for any tour.

ADVANTAGE: CENTRONICS Model 730 is leading the way to a whole new era in miniprinters. Naturally, it's from the leader: Centronics. We pioneered dot matrix printing and have been ranked #1 ever since. No other company can match our strong serve in performance, selection, and value. And our high-volume production capability means we won't fault on your delivery.

Get the advantage. For more information on products or employment opportunities, write or call today: Centronics Data Computer Corporation, Hudson, New Hampshire 03051, (603) 883-0111.

CENTRONICS® PRINTERS
...the advantage

CIRCLE 9 ON INQUIRY CARD

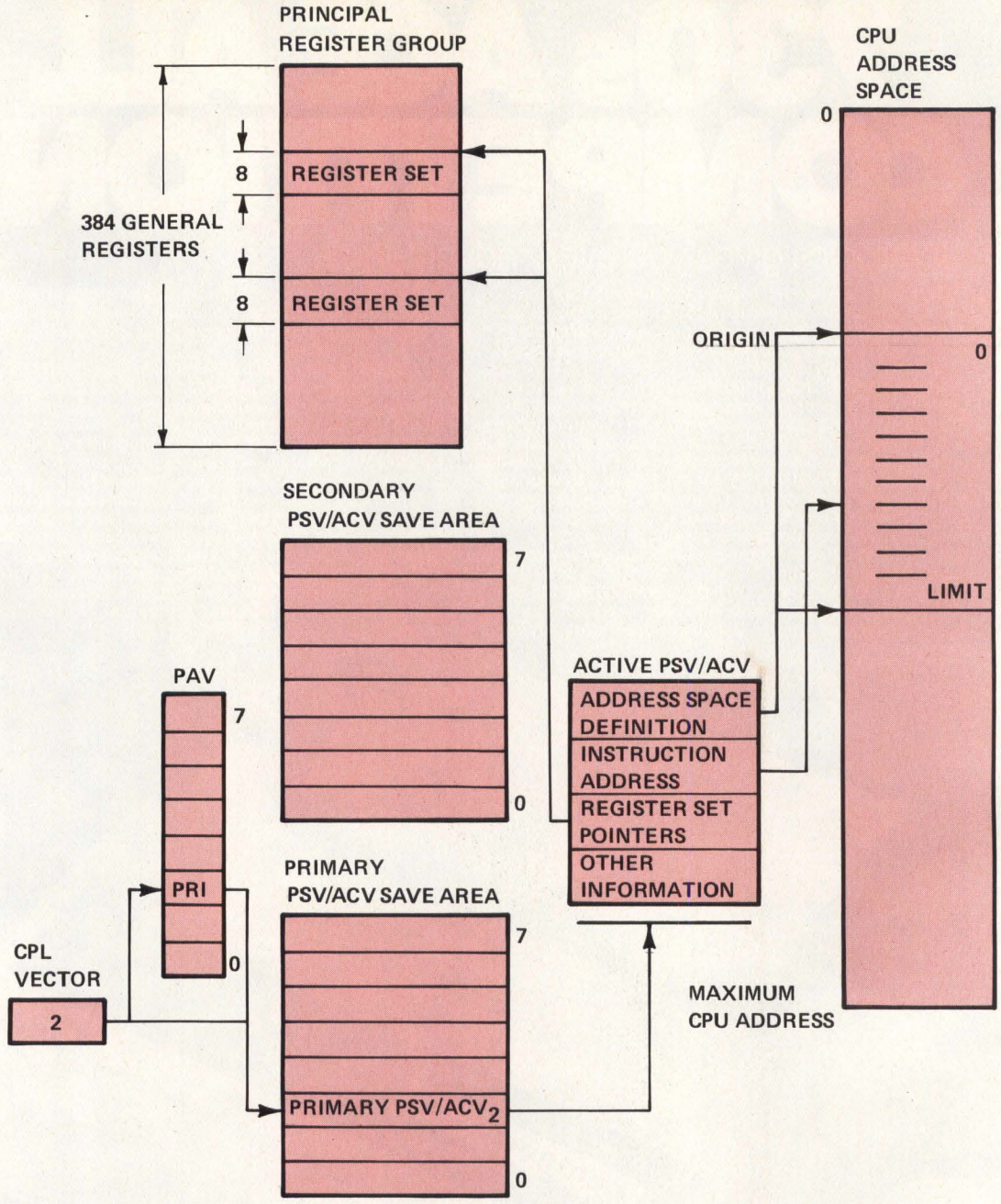


Fig 1 PSV activation hardware. Two PSVs for each of eight hardware priority interrupt levels are saved and activated by hardware. Active PSV defines all program facilities required for execution to begin

specify privilege modes that, in turn, allow programs to be designated as supervisor or application. A typical operating system might use secondary PSVs for application programs and split control functions between primary and secondary PSVs.

A supervisor program can change the protection mechanism. It can also manipulate the contents of the interrupt structure to dispatch new programs on any interrupt level. However, the hardware prohibits an application program from performing these actions. The instruction set that the application program can execute excludes those instructions that could be used to change the protection mechanism and the interrupt structure in general. However, the application program can force a PSV swap on its own level and thereby activate its supervisor.

This procedure can be accomplished in two ways. One is to issue a CALL PSV instruction. That action causes suspension of the currently active program, changes the PAV bit, and acti-

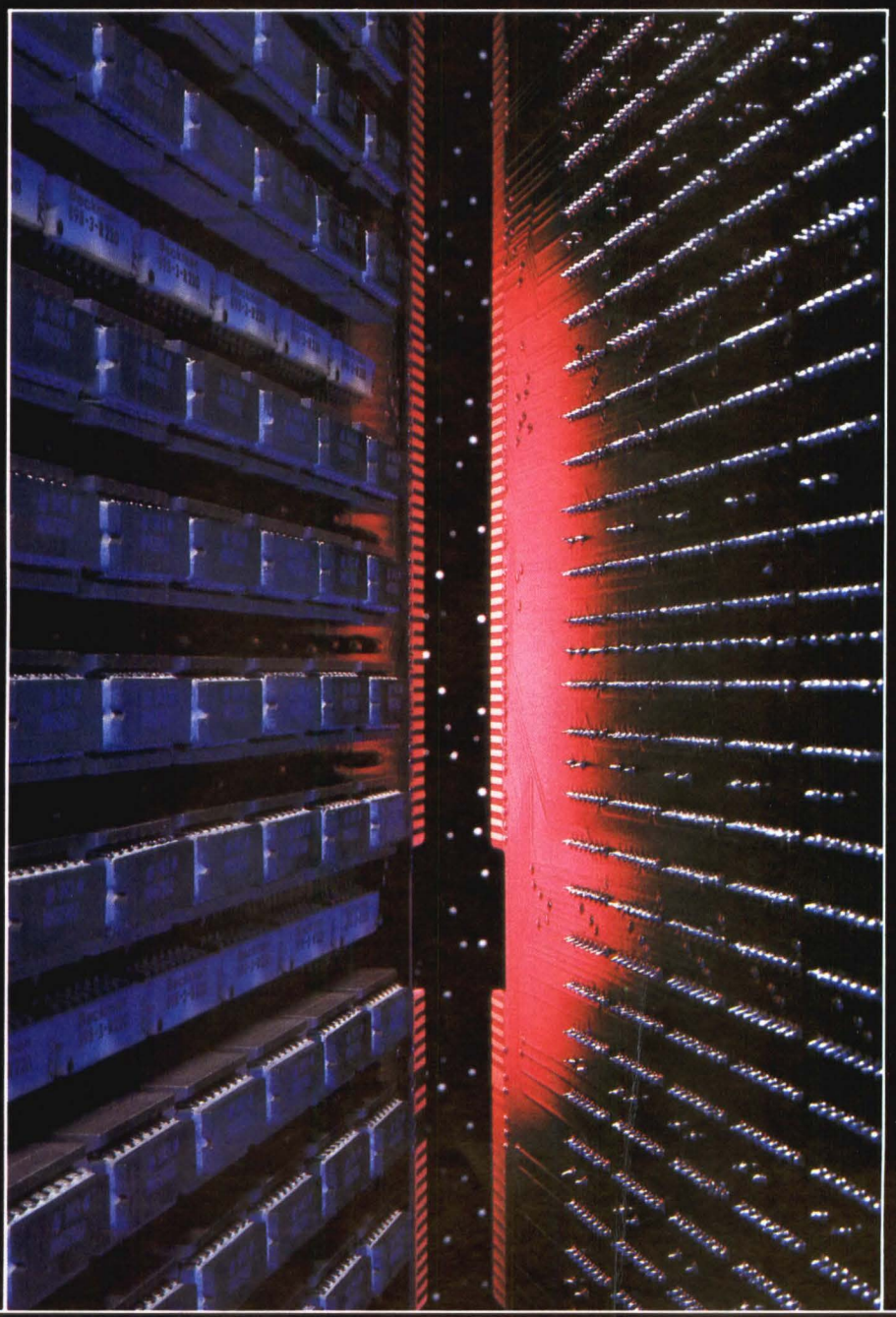
NO. 3

NATIONAL ANTHEM

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY.

MST™-Industry's only batch tester of memory components.

MEMORIES TESTED 4 TIMES, WITH 4 SET-UPS, AND 3 TESTERS.



Low-cost, high-speed BIFETs in National service

MICRO-DAC D/A converters get you off the bus easy

Analog I/O board simplifies system design

Wizardry made practical

Data Acquisition Digital Discrete Hybrid Linear Memory Components
Microcomputers Microprocessors MOS/LSI Optoelectronics Transducers

New mil-temp BIFET™ Op Amps inducted into National service.

Introducing low cost, high-speed, JFET input operational amplifiers with internally trimmed input offset voltage.

National Semiconductor invented BIFET technology back in 1975. And because of their low bias current and high-speed performance, these devices soon made themselves indispensable to the industry. Predictably, the competition copied National's BIFETs, and continue to imitate what National developed.

National, however, moves on. From invention to an 80-plus list of op amps, multiplexers, sample and holds, comparators, switches, and A/Ds. Their latest offering consists of three new low-cost, high-performance military temperature range op amps, designated the LF151A, LF151, and LF153.

The LF151A and LF151 singles. The LF151A and LF151 were designed to close the price/performance gap between National's LF156H mainstay and their top-of-the-line model LF156AH. Both of the new models come complete with a solid, dependable list of guarantees over the −55° to 125°C temperature range.

By way of illustration, the LF151A features a maximum input offset voltage of 2mV coupled with a maximum input offset voltage drift of less than 20μV/°C. In addition, the minimum slew rate is 10V/μsec, and the bandwidth is 3MHz minimum.

All these parameters are fully tested (including temperature drift), and are unconditionally guaranteed. That means there are no exceptions, qualifications, asterisks, or footnotes along with your product.

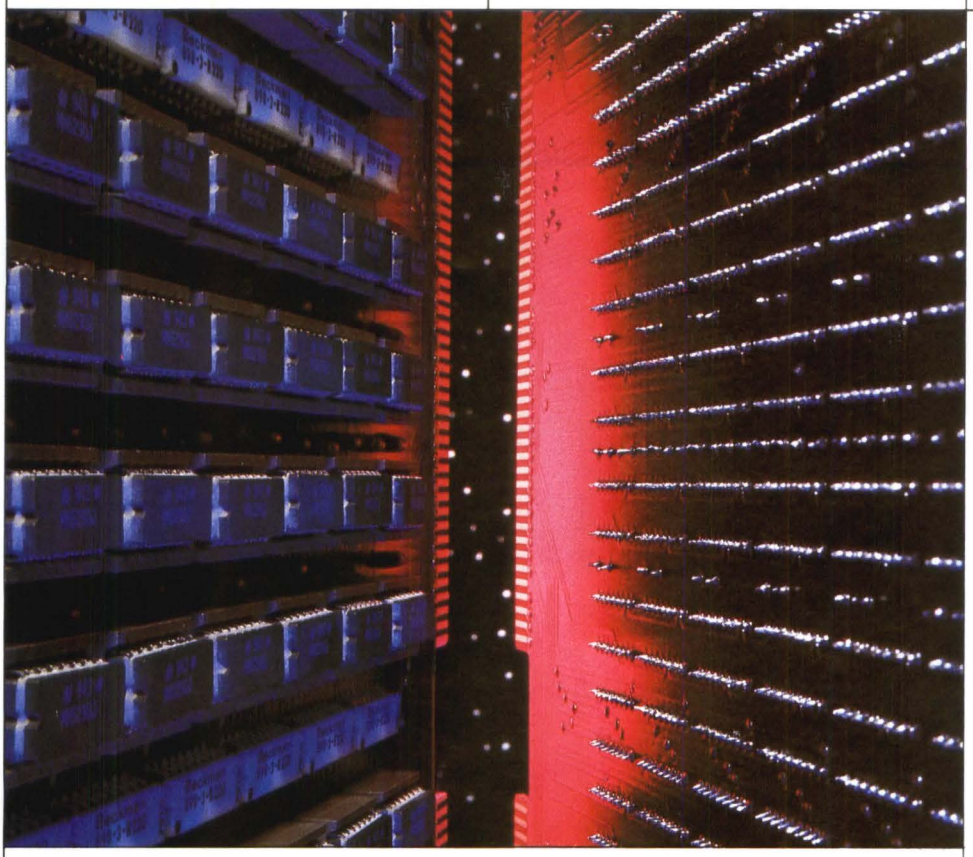
Two LF151's for the dual minded. If a dual op amp is what you're looking for, there's National's LF153, nothing more than two LF151's on the same die.

National guarantees that its input offset voltage will not exceed 7mV over the full military temperature range. You also get low bias current, high-speed, and a very capable and efficient pair of op amps in a practical-sized, single 8-pin package.

It is another sensible, timely solution from the people that invented the BIFET.

On top of everything, they're available now. In addition to the attractive features of these three new op amps, there are two more appealing aspects: all three are available now, for as low as $3.25 for the single, and $6.00 for the dual (100 unit price). For more information, simply call or write your local National distributor or sales engineer. They'll be more than happy to answer any questions you may have about BIFETs.

Or about anything else in the semiconductor-related industry, for that matter.



National tests memory components at the system level, so the customer doesn't have to.

In addition to the usual component level processing, MST™ ensures more reliable memory components through testing in a system environment.

Thanks to National's Memory System Test (MST) program, customers specifying MST can eliminate or greatly reduce their own board level testing.

That's because the MST manufacturing flow includes a lot of benefits. Such as correlated accelerated stress testing equivalent to 168 hours at 125°C; inherent stress integrity in the MST equipment, not found in conventional burn-in systems currently in use; and board-level environmental testing over the ambient temperature range of +25° to +70°C, as well as over all power supply limit combinations. These tests are performed in addition to National's usual final testing and QA component level processing.

This combination of board level and component level testing, with its multiple insertions, results in parts that are significantly better in quality and reliability.

Separating the good from the bad. The MST program has been developed by National over a four-year span, and investigated extensively in their engineering and production facilities. The system correlates fully with standard component test equipment, with some important improvements.

With standard equipment, certain devices could be intermittent failures, a certain card in a system environment may fail, or their failure simply may not be detected.

The MST system also detects units that experience one or more "soft errors" at any time during the many hours they are in the system test environment. This type of failure is usually detected during a board level system test.

Multiple test patterns, power supply margin tests, real time error logging, and hours of continuous testing over the operating temperature range in a card-level system help separate the good units from the bad.

Providing a real memory system environment. When National's customer specifies MST processing, he receives parts that have been tested in a true card-level system environment. MST is a **memory system** with built-in testing and diagnostic capabilities. And it makes use of memory storage cards operating in a temperature chamber.

The memory storage card is a multilayer printed circuit board holding 72 units. Each MST module holds 64 cards operating as a memory system in a temperature chamber. Which represents 4608 units operating under test simultaneously.

The bottom line is that National's MST processing is unique to the entire industry. And specifying MST may cost a little more, but it's worth a lot more.

New MICRO-DAC™ Series is the easiest way to get from D to A.

National's DAC 1000 is the first of a series of four quadrant multiplying D/A converters which easily interface to a μP.

The DAC1000 is the only microprocessor-compatible 10-bit DAC that is truly μP-compatible without the need for any support chips. In fact, it looks like a memory location or I/O port with all control functions right on the chip. So you get easy interface with any 8 or 16-bit data bus.

The "Best Straight Line" Myth. The competitions' linearity spec is based upon a "best straight line," which doesn't correspond to real world applications, and can mean several adjustments to find the "best straight line." The competitors benefit by shipping these lower accuracy devices. You lose.

With National's "end point" linearity spec only two adjustments are needed – Zero and Full Scale; set these, and the linearity specification is met. Thus, National's linearity specifications ease calibration of the system. In addition, where low reference voltage, or reference voltage changes are required, linearity is maintained even with a 10 to 1 reduction.

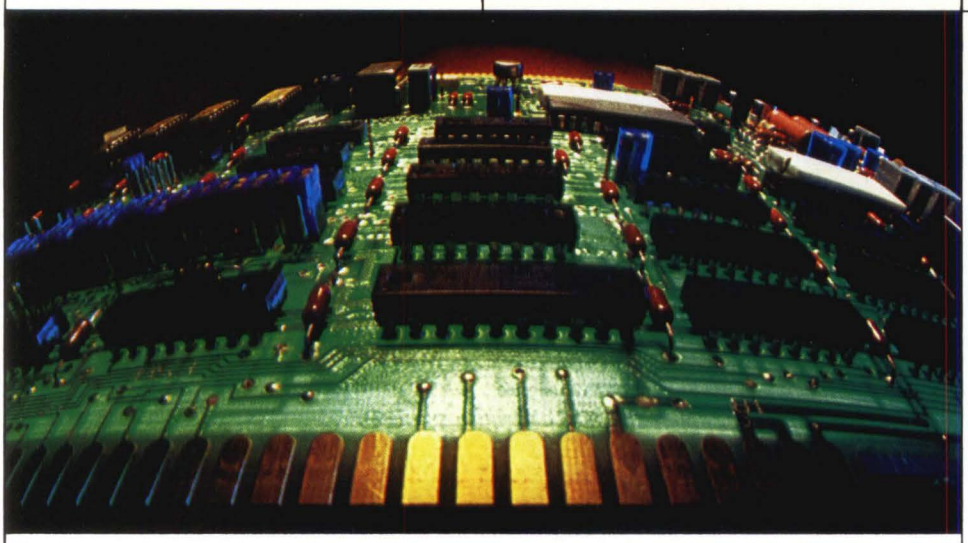
It fits into a lot of places and takes up a lot less space. The MICRO-DAC1000 Series is used primarily for building D/A conversion systems. But these DACs can also be used as building blocks for digitally controlled amplifiers, alternators, active filters, and even oscillators. They're also more flexible than any DACs around – 4 quadrant multiplying, double buffered, single supply operation from +5V to +15V, right or left justified data format, micro power operation (2mA max.), and output current mode setting time of 500ns.

In the 20 pin package they're only .3" wide compared to .6", so they're easily inserted and use a lot less space.

If you don't need μP interfacing, National's still got you covered. The DAC1020 and DAC1220 are 10 and 12-bit DACs without all the μP interfacing. And they still offer application flexibility along with improved linearity.

If you're already using AD7520, AD7521, AD7530, AD7531, or AD7533, National's DACs are direct replacements. They're also priced at least 30% lower and in some cases as much as 300% lower. These inexpensive DACs start at $4.00 at 100 pieces and because of National's volume capacity, no one can sell for less.

The MICRO-DAC Series opens up a whole new world for design engineers. Because National's D to A's are better from A to Z.



BLC-8737 simplifies MULTIBUS design.

The new BLC-8737 analog I/O board is the newest addition to National's already broad line of more than 75 MULTIBUS-compatible products. It provides easy interface to the real world of analog, thanks to its built-in intelligence that handles analog functions automatically.

The BLC-8737 eliminates the time formerly spent writing conversion routines, because it takes care of the complete analog conversion and scanning control. So you save substantial development costs, and get to the market quicker, too.

The board also comes with a warranty of a full 12 months – four times longer than the competition's. That's just one more reason why National's boards aren't just simpler, they're simply better.

Who and what are practical wizards?

Practical wizards are people with vision, vast knowledge, and a desire to help people through their work. They're not afraid to offer solutions that are new and different from anything that's been tried before.

They're people like Thomas Edison, the wizard of Menlo Park, also called the father of modern electronics. Edison was concerned with improving the human condition, and he attempted to do so with his insights into the workings of electronics. He was a visionary, true, but practicality was the hallmark of everything he did. And ultimately, it was that human practicality that made his accomplishments even more profound and far-reaching.

Just as Edison changed the world with his ideas, the practical wizards at National contribute their part through semiconductor technology. With their expertise, and level-headed, sensible approach to solving problems, they are the embodiment of "wizardry made practical."

National Semiconductor
The Practical Wizards
of Silicon Valley.

What's new from the National archives?

001 ☐ BLC 8737 Data Sheet
002 ☐ COPS 402 Data Sheet
006 ☐ Special Functions Data Book ($6.00)
007 ☐ Interface Data Book ($6.00)
008 ☐ Pressure Transducer Data Book ($3.00)
009 ☐ ROM MM 52116 Data Sheet
010 ☐ ROM MM 52132 Data Sheet
011 ☐ ROM MM 52164 Data Sheet
012 ☐ DAC 1000 Data Sheet
013 ☐ LF 151, 151A, 153 Data Sheet
014 ☐ New Data Acquisition Products Brochure
015 ☐ MST Program Brochure

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vates the other PSV on the same interrupt level. The application program normally uses this method to call the supervisor program for system service, such as I/O, real storage allocation, or program termination. The CALL PSV instruction is also generally used by the supervisor program to dispatch new application programs or to redispatch an application program that has been awaiting system service.

In the second method, the primary PSV is activated by a program exception in the program executing under the secondary PSV. A program exception occurs when there is an attempt to perform illegal operations, such as an attempt to access storage outside the program's protected region, an attempt to execute an undefined instruction code, or an application program's attempt to execute an excluded instruction.

If a program is executing under a secondary PSV and a program exception takes place, the program's execution is suspended, the PAV bit for that level is changed to "primary," and a program activation of the primary PSV takes place. The program exception can then be handled on the level at which it occurs. If, however, the program exception occurs in the primary PSV, a high priority interrupt is activated. A field in the secondary PSV/ACV save area, which can be read by the supervisor program executing under the primary PSV, indicates whether its activation is from a CALL PSV instruction or a program exception. In the case of a program exception, the hardware provides additional information to help identify the type of error that occurred.

An example of the normal passing of control between a supervisor program and an application program is shown in Fig 2 (a). The supervisor program determines that an application program is to be run, sets up the PSV/ACV save area of the application program, and issues a CALL PSV instruction. This instruction activates the secondary PSV, which is the action that dispatches the application program. Then, that program runs until it requires a system service, in this case, I/O. The application program issues a CALL PSV instruction, activating the supervisor program at the instruction address immediately following the supervisor's CALL PSV instruction that originally dispatched the application program. The supervisor program determines the nature of the request and, when ready, redispatches the application program with another CALL PSV instruction. In this case, the application program runs until completion, and then requests termination.

When the supervisor program receives control, it determines whether more application programs are ready to be run on the same level. If true, a new application program is dispatched. If there is no additional work, the interrupt request for the level is turned off, and control is relinquished to another priority level.

In Fig 2 (b), the application program that has been dispatched contains an illegal instruction, and a program exception takes place when the hardware attempts to execute this instruction. This exception automatically activates the supervisor program which determines that its activation is caused by a program exception and takes appropriate action. Depending on the operating system, the application program can be terminated, or control can be passed back to the application progam at an error handling entry point.

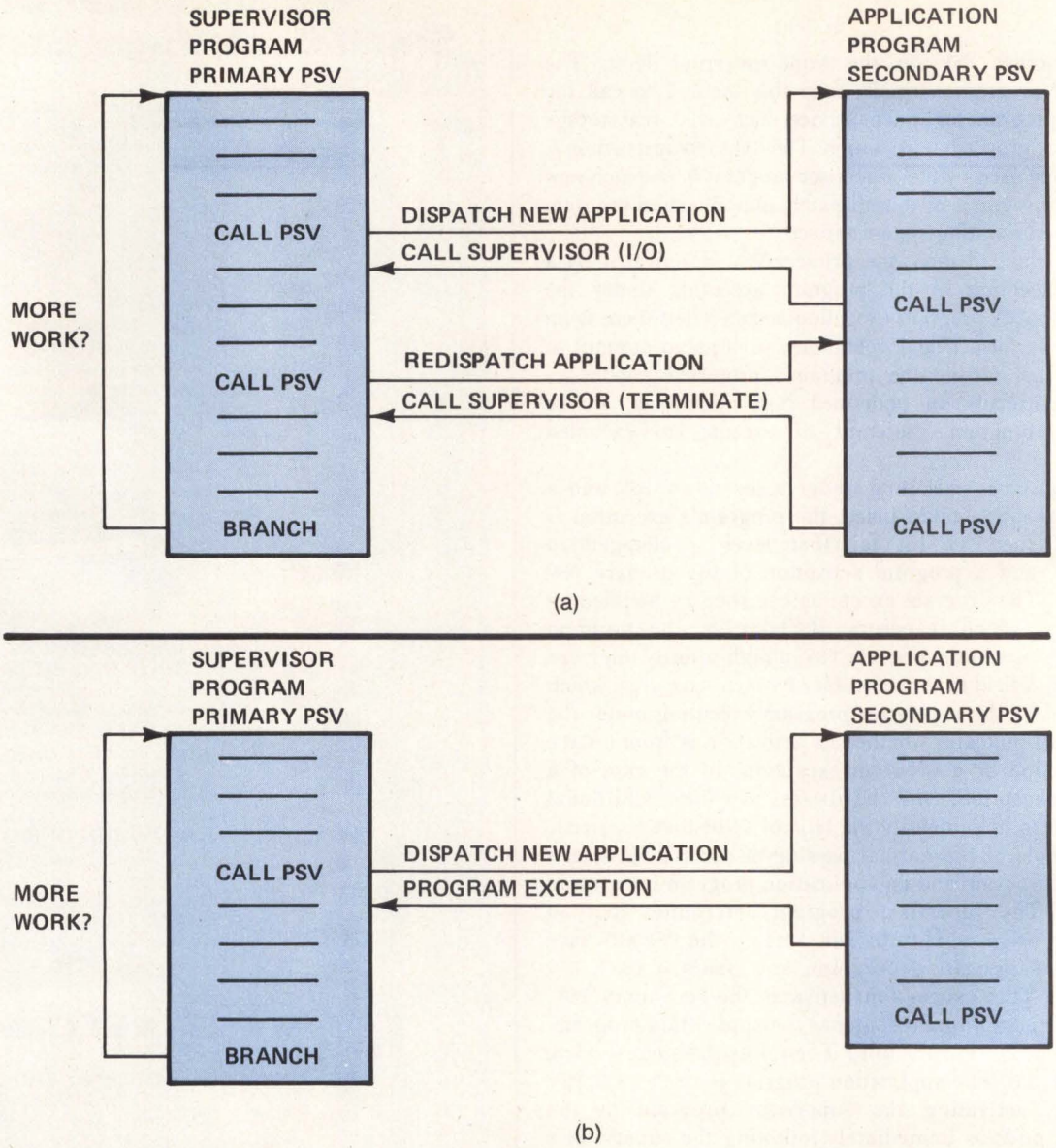

Fig 2 Supervisor/application programs. Examples of passing control between supervisor and application program are shown. In normal operation (a), supervisor program acts as dispatcher. Dual PSV facility allows both programs to coexist on one interrupt level. In (b), control is passed due to program exception. PSV field provides information to help identify cause of exception

Priority Interrupt Mechanism

Three sources of interrupt exist within the interrupt structure: I/O interrupt request vector (IOIRV), program interrupt request vector (PIRV), and error interrupt request vector (EIRV). Both IOIRV and PIRV are eight bits long, with each bit corresponding to a priority interrupt level. EIRV is seven bits long, but creates an interrupt only on a single level.

IOIRV provides a mechanism through which I/O devices can create interrupts across the I/O bus and is used by devices to signal their requirements for service. PIRV allows programs to create interrupts. It is generally used by supervisor programs to maintain activation of their own level following an I/O interrupt, or may be used to activate other interrupt levels for higher or lower priority work.

EIRV creates interrupts only on level 0, the highest priority level available. This interrupt is created whenever a hardware system check, a channel exception, or a program exception in a primary PSV occurs. Different bit settings of the EIRV indicate the nature of the error.

In addition to the interrupt sources, the interrupt mechanism contains two masks, common and master. In a multilevel machine, certain code sequences cannot allow interruption by programs on other levels. An example is a routine that updates a queue used to communicate between levels. During this update, the program cannot allow interruption by another level that might also attempt to use the same queue. To handle such situations, the program masks other levels. The common mask is eight bits long, each bit corresponding to a priority interrupt level. It can be used to mask or disable designated interrupt levels.

In the information system, a program's execution will not continue unless its level is enabled with an interrupt pending or the master mask bit is reset. During execution of instructions, the hardware examines the interrupt sources and the common mask to select the highest priority interrupt level that is enabled and has an interrupt pending. If that level is different from the currently active level, a PSV swap will occur unless prevented by the master mask. If there is no longer any enabled level with an interrupt pending, the processor enters a wait state unless prevented by the master mask. While in the wait state, instruction execution stops while the processor continuously examines the interrupt sources for a new interrupt on an enabled level.

The master mask contains one bit and can be used to prevent entry into the wait state or program suspension by all other levels except 0. When the master mask is reset, the currently active program will continue to execute until the master mask is set or a level 0 interrupt takes place. Interrupts to level 0 cannot be prevented by the master mask since this is the level on which the EIRV interrupts. If these interrupts were masked, system errors could not be immediately detected and system integrity might be jeopardized. For the rare cases when masking of level 0 is justified, the common mask can be used.

If a PSV swap to a new level is to take place, the program executing on the current level is suspended. The new level is loaded into the current priority level vector and a PSV activation takes place.

Summary

The hardware-oriented interrupt system for the IBM 8100 processors provides efficient handling of the tasks associated with distributed processing and facilitates the architecture of a multiprogramming operating system.

References

1. "Interactive Communication System Improves Plant Productivity," *Computer Design*, Dec 1978, p 26
2. E. J. Steubesand, "Distributed System Hardware Design Offers Interchangeable Communications," *Computer Design*, Sept 1979, pp 14-27

"THE 8086 HAS UNSURPASSED SUPPORT!"

By now, you've probably heard a whole lot about the 8086 and its development system. Intel's seen to that.

But there's one or two tiny, little facts that could get lost in all the noise:

The 8086 isn't the best 16-bit CPU. It doesn't even have the best development system.

The AmZ8000 does.

Our new System 8/8 was designed especially to support the AmZ8000. It beats Intel's system hands down.

System 8/8 can be used as an 8-bit or a 16-bit system via the Multimaster Bus. Intel's system can't. System 8/8 can translate both 8080/8085 and Z80 programs. Intel's system can't. System 8/8 has an optional arithmetic processor, a PASCAL compiler, and 8080, 8085, Z80 and AmZ8000 macroassemblers. Intel's system doesn't. System 8/8 comes unbundled; you buy just the pieces you want or need. Intel makes you buy the entire package whether you need it all or not.

But the best thing about System 8/8 is the CPU it supports: The AmZ8000.

The AmZ8000 has a more powerful, more advanced, much more flexible architecture than the 8086. It also has more addressing modes, more general-purpose registers, larger addressing spaces, better I/O capability and more

"The AmZ8000's is better."

powerful instructions. It can even accommodate more data types. And the AmZ8000 has a lot higher throughput using standard NMOS than the 8086 using HMOS.

To demonstrate the capability of the AmZ8000, we developed a fully assembled and tested Evaluation Board with a memory, an I/O and a monitor. Ask for it by name: AMC 96/4016. You can also get a full ASCII keyboard/display and an assembler.

One last thing: we know it hurts to drop Intel for somebody else. We went through it ourselves. But it's going to hurt a lot more next year. By then, your competitors could be so far ahead of you, you might never catch up.

Call Advanced Micro Devices. We'll send you all the latest information on the AmZ8000, System 8/8 and the AMC 96/4016. Or, we'll line you up for our next 4-day seminar.

When you've looked at all the facts, one fact is going to come through loud and clear:

The AmZ8000 is better.

Advanced Micro Devices

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CIRCLE 12 ON INQUIRY CARD

Statistical Multiplexer Prevents Data Loss

A version of the Supermux 480 statistical multiplexer, available for use in networks with printers and other terminals having a "transmit off" (XOFF) command capability, is switch-programmable to recognize that and other stop data commands. The multiplexer at the terminal end stops data flow to the terminal when it sees the XOFF command, which many terminals use to signal the host CPU to stop sending data. However, the multiplexer will permit the CPU to continue transmission and will itself generate the XOFF message if its own individual channel buffer reaches 80% of capacity before the terminal is ready to resume reception of data. This results in a reduction of CPU load and elimination of lost data, according to Infotron Systems Corp, Cherry Hill Industrial Center, Cherry Hill, NJ 08003.

Both this and the earlier version of the multiplexer have a common 16k-byte RAM buffer for all input lines. Outages as long as 10 s on a fully loaded 9600-bit/s line can be handled.

Up to eight asynchronous input lines are concentrated over a single high speed output. Aggregate input data rate may be up to 38,400 bits/s. Switch-selectable input speeds for each channel range from 50 to 9600 bits/s. Input codes may be 5-, 6-, 7-, or 8-bit, Baudot, ASCII, or IBM.

The output line can operate at any synchronous speed to 9600 bits/s, and can also be operated at switch-selectable isochronous speeds of 300, 1200, or 1800 bits/s via 103 or 202 modems.

Transmission protocol is compatible with SDLC and CCITT X.25 level 2 framing: flag, zero insertion, and 16-bit CRC, with variable block length of 128 characters maximum. Error correction is via automatic request for repetition (ARQ). Built-in diagnostics display system status on seven front panel LED indicators. The multiplexer comes in either 4- or 8-channel models, with the 4-channel version field-expandable.

Circle 400 on Inquiry Card

Satellite Data Link to Aid Pilot Training

A high speed satellite data link between the Air Force Command and Evaluation Center at Hill Air Force Base, Utah, and Nellis Air Force Base, Nev, will enable observation, analysis, and critique of new F-16 fighter pilots flying simulated combat missions. The 76.8k-bit/s simplex satellite data circuit will have a 5-m transmit earth station at Nellis, and a similar receive station at Hill. Earth stations will be placed in operation by American Satellite Corp, 20301 Century Blvd, Germantown, MD 20767, under terms of a contract with Cubic Corp's Defense Systems Div, prime contractor on the F-16 combat readiness test program. The satellite data network is scheduled to be operational by early January 1980.

Part of the program calls for pilots and crews to fly combat missions out of the Nellis base. The test environment is designed to simulate actual combat conditions, including air-to-ground attacks, ground radar detection defenses, and mock air combat engagements. Data pertaining to these missions will be collected on a real-time basis from various sensors and range instruments.

Circle 401 on Inquiry Card

Independent Telephone Company Invests in Digital Communications Firm

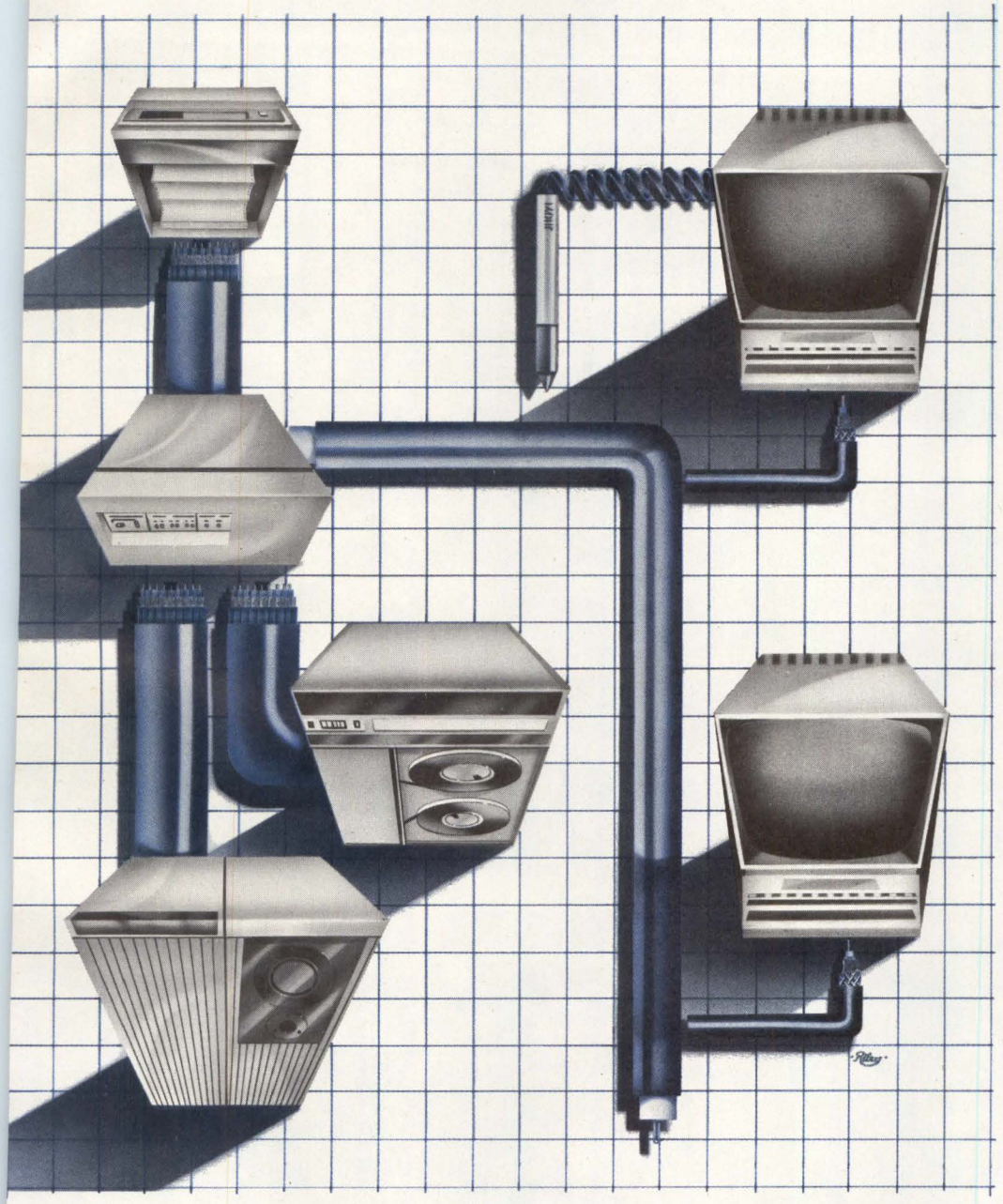
Continental Telephone Corp, third largest U.S. independent telephone holding company, with operating subsidiaries in 38 states and in several foreign countries, has acquired an approximate 20% equity in Tran Telecommunications Corp, 2500 Walnut Ave, Marina del Rey, CA 90291. Total value of the transaction was about $4.7 million.

Tran, a pioneer in the field of digital telecommunications, has been involved in many large scale digital networks, including Canada's Dataroute, two South African national networks, Pacific Telephone's Data Service for the State of California, and a large number of private networks. Tran Chairman Ray Sanders stated that the association with Continental and its concomitant financing would allow a broader application of his company's technology in public and private networks in order to meet future business market demands for packet, facsimile, video, and digitally-encoded voice transmission.

Charles Wohlstetter, Continental Telephone's board chairman, said that application of Tran's digital technology would directly benefit the operating companies, and give Continental an advantageous position in the growing field of digital communications.

Circle 402 on Inquiry Card

TODAY'S EDP SYSTEMS ARE RUNNING ON TIMES.



Today as cable becomes increasingly critical to the design of EDP systems, leading companies are doing exactly what people in the military and CATV industry are doing. They're hooking up with Times.

After all, we've got the most standard designs and the most experience in custom designs in the world. Times covers a dozen categories from which we can offer design variations that number in the tens of thousands. And we're also busy at work making fiber optics a practical reality for EDP systems too.

No matter what size, electrical characteristics or packaging requirements your system calls for, Times gives you a bigger choice. For linking your Mainframe with your Tape Drive, we've got Multi-conductor Coax. To connect your Modem with your Terminals, there's our Data Bus and Coaxial Computer Cables. All of which can be delivered quickly. Because Times has manufacturing facilities located across the nation.

You'll find it all explained in our new catalog. Send for it. It's the only way to keep abreast of the newest developments in cable. Because it's the only catalog that keeps you up with Times.

Times Wire & Cable, 358 Hall Ave., Wallingford, Ct., 06492 203-265-2361.

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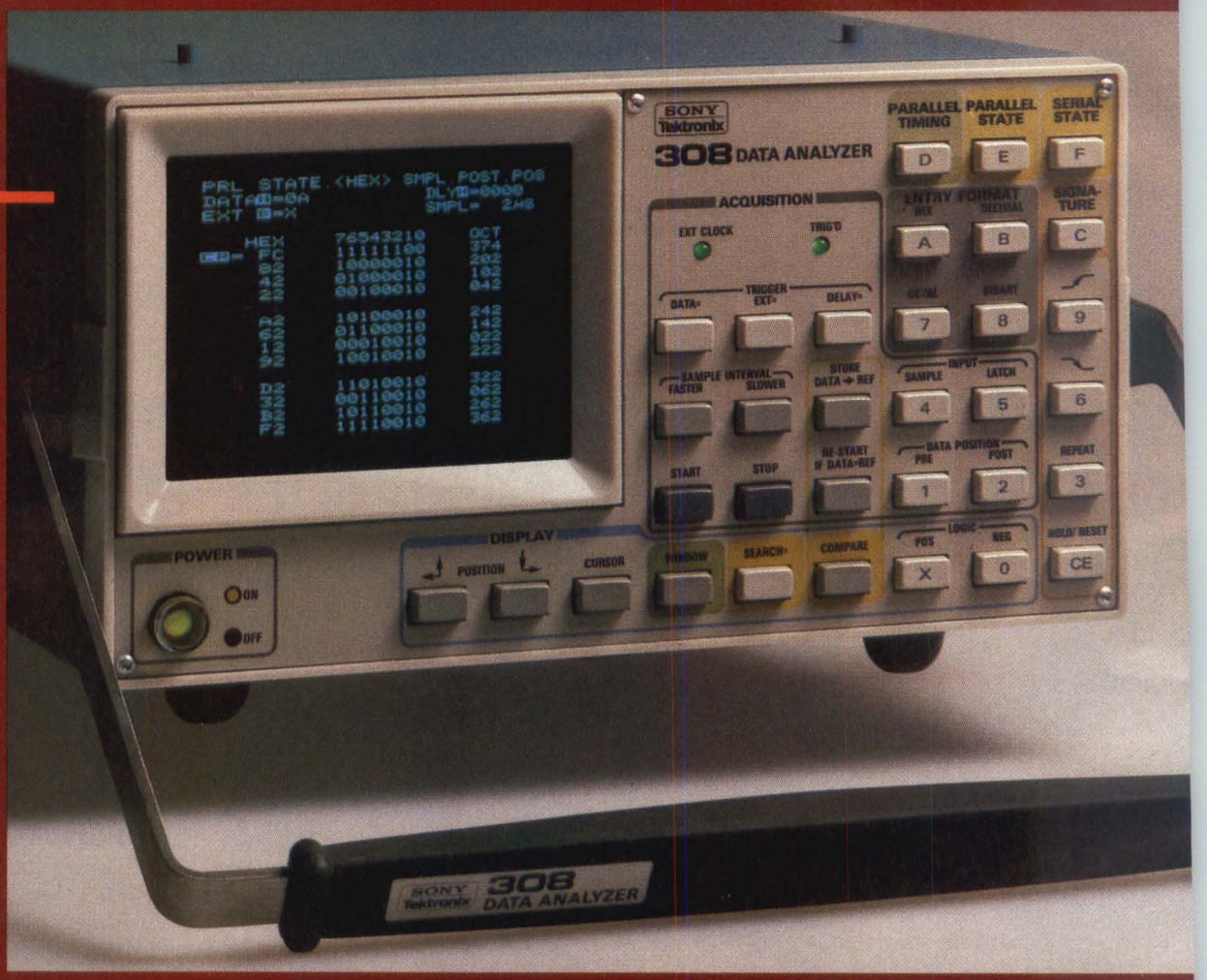
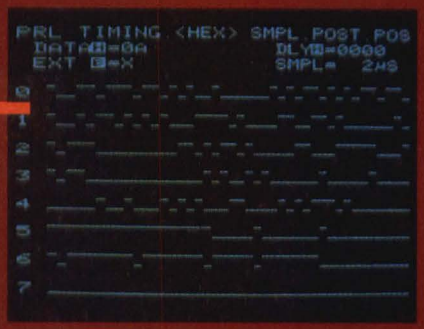
CIRCLE 13 ON INQUIRY CARD

308 DATA ANALYZER



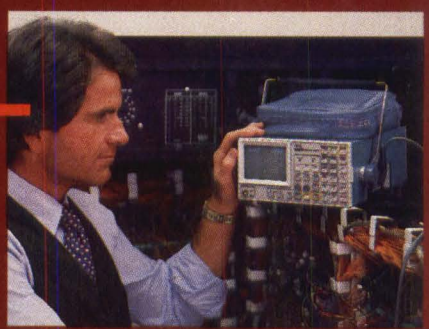
308 display of parallel state data.



Parallel timing diagram can also be displayed as a state table in hex, binary and octal.

Signature display will hold and display up to 8 signatures at once.

Serial display includes ASCII readout in addition to hex and binary.



The 308 is lightweight (3.6 kg/8 lb) and portable.

All logic analyzers handle parallel data. Only one also does serial and signature.

Introducing the 308 Data Analyzer.

Until now, logic analyzers have been confined to parallel state and timing data. Unfortunately, digital problems haven't. They might originate at a serial data port. Or appear as a faulty signature output.

So we've designed a logic analyzer that handles all four data formats: Parallel state. Parallel timing. Serial state. Signature analysis. Each with an impressive array of display and sampling features. All contained in a single lightweight (3.6 kg/8 lb) portable package. The 308 Data Analyzer, from Tektronix. A unique instrument. The first of its kind.

The 308 includes a reference memory for data comparison and word searches. Latch mode. Word recognition up to 25 bits. Pre- and post-trigger control. Synchronous and asynchronous sampling. Digital delay. Timing and state displays in hex, binary and octal. Plus ASCII and parity error in the serial mode. Plus optional accessories for easy probe connection.

And much more. All in a compact and convenient package. One that's cost-effective. And backed by the unmatched experience of Tektronix in the field of digital test instrumentation and service. Interested? Contact your local Tektronix Field Office, or write us.

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TECHNOLOGY AND ECONOMICS: MANUFACTURING COST FOR A MICROPROGRAMMED SYSTEM

Montgomery Phister, Jr
Systems Consulting
Santa Monica, California

Many of today's computer systems, large and small, are microprogrammed. Designers of microprogrammed processors have certain degrees of freedom, depending on the components used and the architecture to be realized. Specifically, they may be able to look at two or more designs having arithmetic logical units (ALUs) of different complexity and may find that there is a degree of complexity that minimizes system manufacturing cost.

Microprogram Efficiency

To see how this may happen, consider the cost model presented in the panel. It assumes we start with a nonmicroprogrammed system having e logic elements, and that the ith alternative microprogrammed design contains an ALU with $(1 - f_i)e$ logic elements and a control memory containing bf_ie bits. The factor b is the "microprogram efficiency"—that is, the number of bits required to replace one logic element. System cost is then simply a function of e, f_i, and b; of the manufacturing cost of a logic element in the ALU; and of a bit in the control memory. For simplicity, replace the discrete values f_i with the continuous variable f.

The cost model shows that, if b is constant, system cost will be a minimum either with no microprogramming or with the maximum possible microprogramming (ie, the minimum ALU), depending on the value of b relative to the ratio of bit and logic element costs. However, Husson* suggests that the power of a microinstruction is a function of the complexity of the ALU: with a bare-bones ALU it will take many control memory bits to replace a logic element; with a complex ALU it will take fewer. Under these circumstances, there may be a value of f

*S. S. Husson, *Microprogramming Principles and Practices*, Prentice-Hall, 1970, pp 69-72

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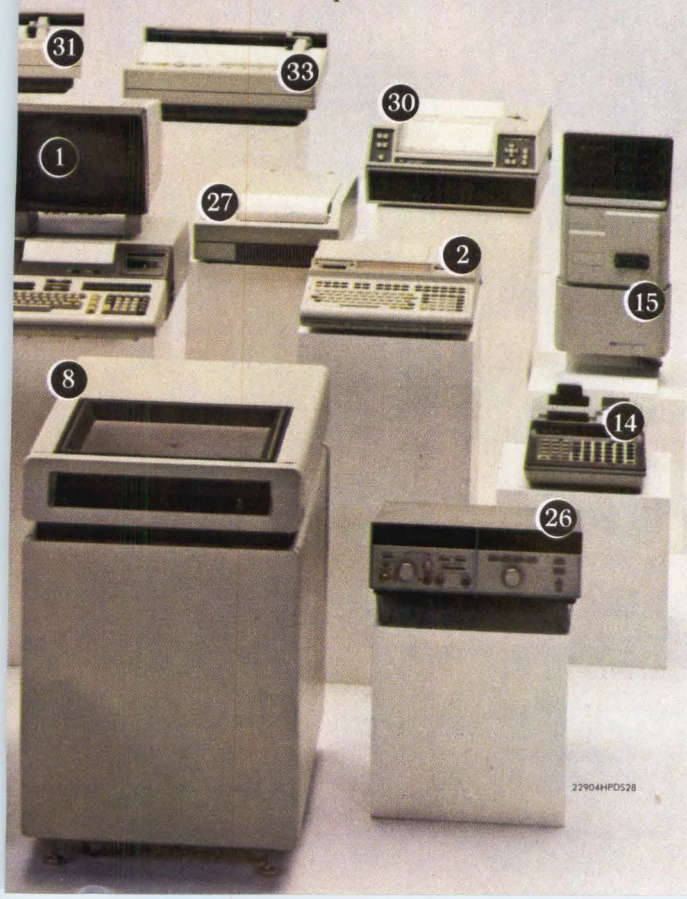

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System Cost Model

Suppose:

- C = System manufacturing cost
- e = Number of logic elements in a nonmicroprogrammed processor
- f = Fraction of logic elements replaced by microprogram control store
- b = Number of control memory bits required to replace one logic element
- c = System manufacturing cost per logic element
- c_m = System manufacturing cost per control memory bit

Then

$$C = c(1-f)e + c_m b f e$$

Two cases are:

(1) b is constant, independent of system size

Then

$$C = c(1-f)e + c_m b f e$$

$$\frac{C}{e} = c - f(c - c_m b)$$

If $c_m b < c$, C/e will be minimum with $f = 1$ (no logic to be controlled by the microprogram)

If $c_m b > c$, C/e will be minimum with $f = 0$ (no microprogramming)

(2) b is a function of amount of logic to be controlled, eg

$$b = b_0 + b_1 \text{Exp}(-ke(1-f))$$

Then

$$C = c(1-f)e + c_m f e [b_0 + b_1 \text{Exp}(-ke(1-f))]$$

$$\frac{C/c}{e} = 1 - f\left(1 - \frac{c_m}{c} b_0\right) + \frac{c_m}{c} b_1 \text{Exp}(-ke(1-f))$$

This cost function is minimized for a value of f which satisfies the transcendental equation

$$(1 + fke)\,\text{Exp}(-ke(1-f)) = \frac{c}{b_1 c_m} - \frac{b_0}{b_1}$$

The equation will generally have a solution, if

$$e > \frac{1}{k}\left(\frac{c}{b_1 c_m} - \frac{b_0}{b_1} - 1\right)$$

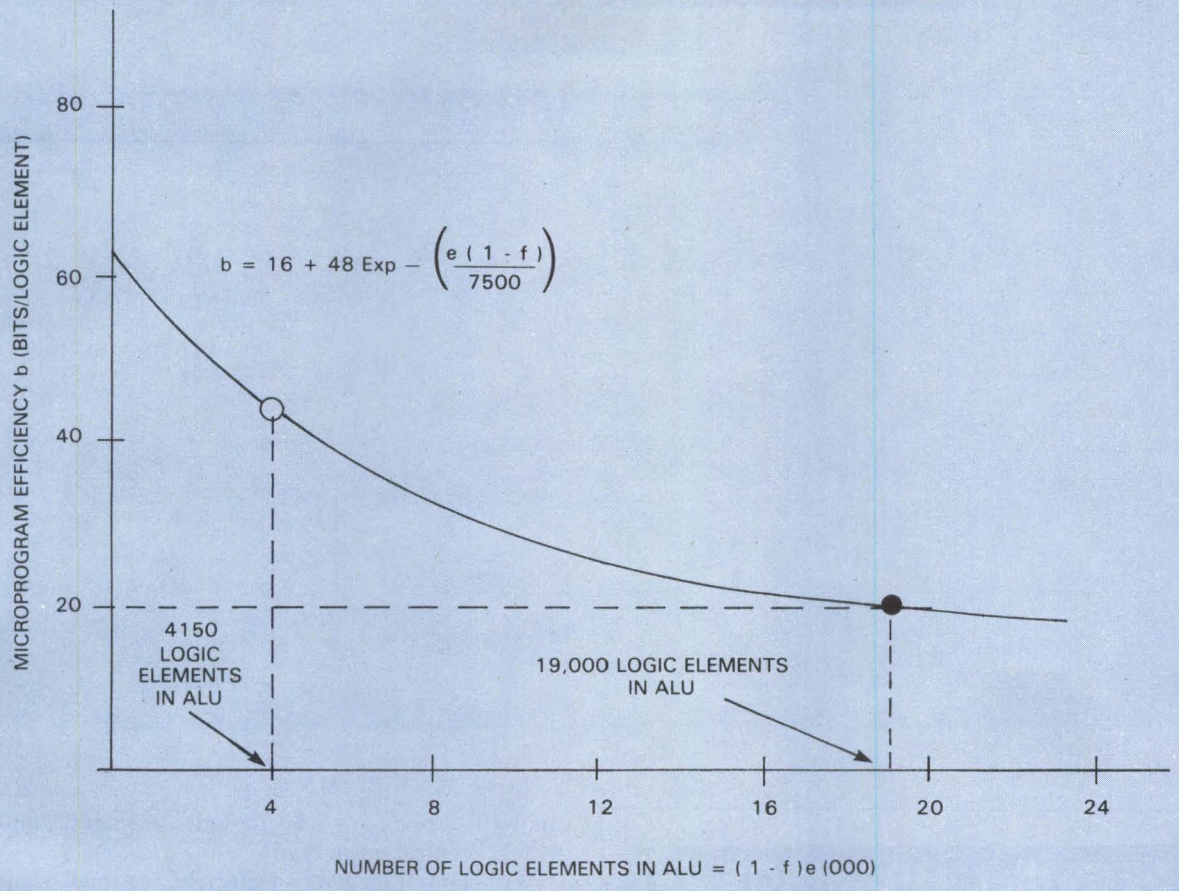


Fig 1 Microprogram efficiency vs ALU size. As arithmetic logic unit (ALU) of microprogrammed system increases in complexity, accompanying microprogram gets simpler, and fewer and fewer control memory bits are needed to implement new functions or features. If ALU contains subtractor only, for example, several microinstructions would be necessary to implement addition; if ALU has both adder and subtractor, microprogram for addition would require fewer control memory bits. This graph proposes an exponential form for the relationship between efficiency and ALU size. System described in a recent *Computer Design* article contained ALU with about 19,000 logic elements and presumed efficiency of 20 bits/logic element, as shown by solid dot. Optimum system shown in Fig 2 has 4100-logic-element ALU and requires about 44 bits/logic element in control store

which minimizes cost, because if f is too large (ALU is too simple) the inefficient control memory is too big and expensive, while with f too small, the ALU itself will be too complex and expensive. Fig 1 provides a seemingly reasonable expression relating b and f.

Estimated Manufacturing Costs

To make use of the model, we must estimate values for c and c_m, the manufacturing cost of a logic element and of a control memory bit. The manufacturing cost model which appeared in a recent issue of *Computer Design* (Sept 1978, p 97) contains data from which these parameters may be computed. The costs given there can be divided into two parts: one covering the ALU, the other the control memory. Control memory components consist of the P/ROMs plus 14 MSI and 27 SSI ICs for each 64 memory ICs. Power costs are distributed in proportion to power consumption of the two parts, and other noncomponent costs are distributed in proportion to number of components. The results of the

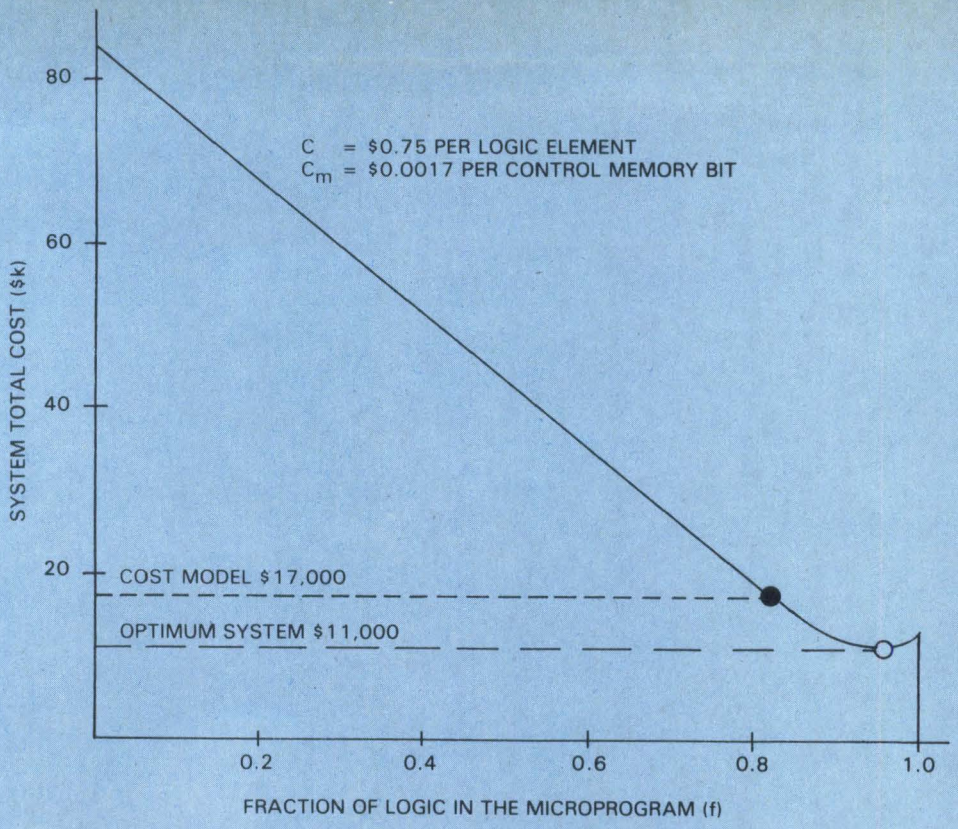


Fig 2 System cost vs microprogram size. Given relationships shown in cost model and Fig 1, and cost parameters given here, system cost decreases as ALU gets simpler—ie, as more and more logic is put in microprogram. In practice, designer does not have unlimited flexibility in choice of ALU size. But with ROM bits cheaper every year, he is more and more motivated to use simple ALUs, if major goal of design is low cost

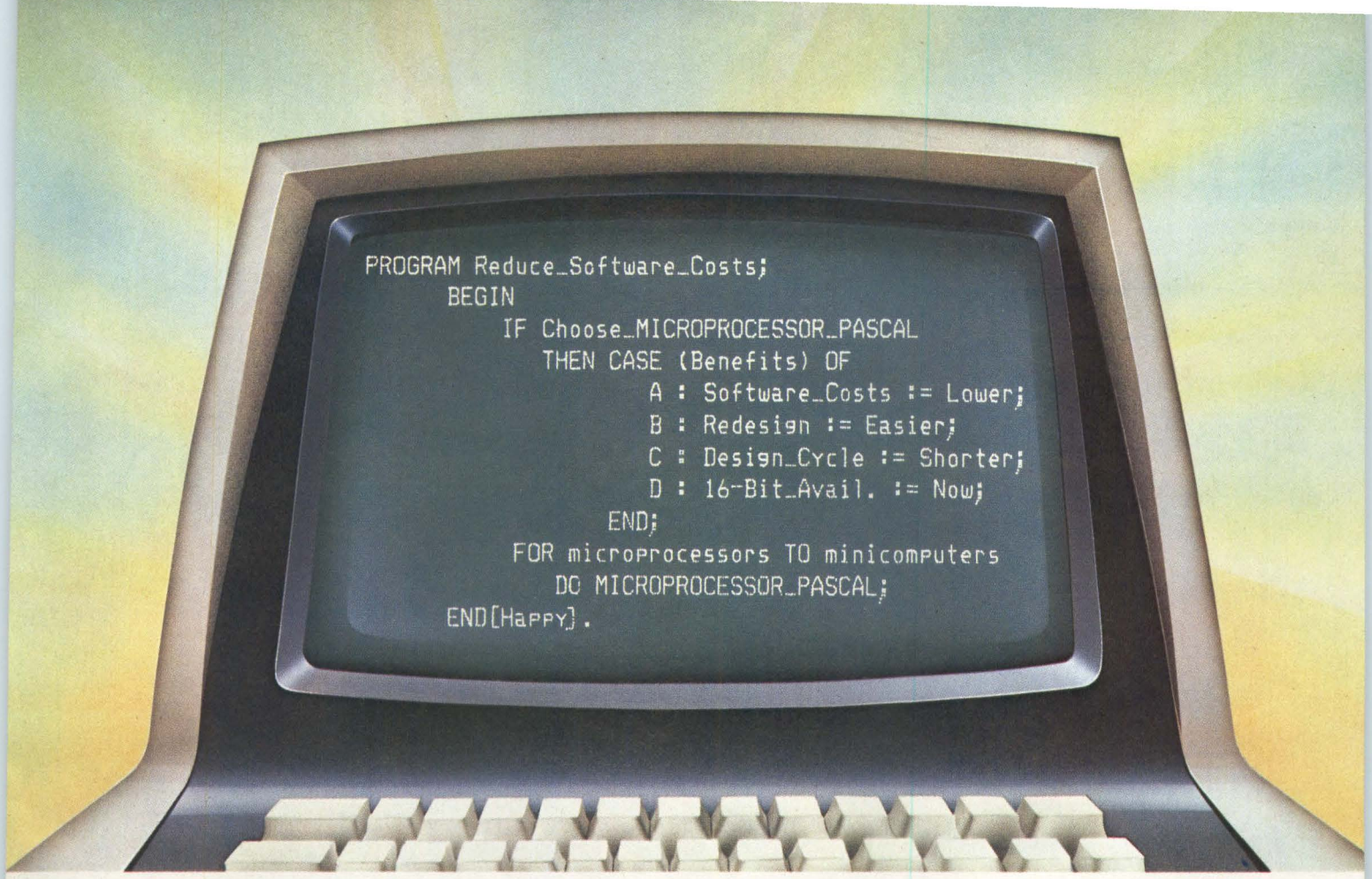
analysis are c = \$0.75/logic element, and c_m = \$0.0017/control memory bit.

With control memory so cheap (c_m so small compared to c), the equations given in the cost model indicate that, assuming b is constant and in the range 20 to 60, the lowest cost system will have the smallest ALU. If b varies as shown in Fig 1 there will be an optimum value of f for minimum manufacturing cost. Fig 2 shows this minimum for the cost parameters presented in the September article. It indicates that manufacturing cost could be reduced to \$11,000 from the \$17,000 shown there, by simplifying the ALU and using a bigger control memory.

Conclusions

In practice the designer may not have much freedom in varying ALU size. Architectural, performance, and component constraints limit his ability to simplify the ALU design. However, as control memories get cheaper and cheaper relative to ALU type logic, the designer must remember that simple ALUs lead to low cost systems—especially important when low manufacturing cost is a major design goal.

The author solicits comments on the material presented here, data supporting or contradicting his approach, and suggestions for topics to be covered in future articles.
— Ed.



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Large Scale Computer Offering Includes Evolutional Operating System

Large scale DPS 8 computers recognize the trend toward distributing data outward from a central computer location into end user departments, and provide total operating system compatibility from large to small configurations. Included in the announcement by Honeywell United States Information Systems Group, 200 Smith St, Waltham, MA 02154, are four large scale computers and evolutionary GCOS 8 operating system designed specifically for the distributed systems market. With powerful transaction processing and communications capabilities, the systems provide a systems approach to balancing workloads, and offer protection for application software investment.

At the top of the line, the single processor DPS 8/70 offers twice the power of the model 66/80. Available in multiple processor configurations, increased power and failsafe backup are provided by systems with up to four processors.

The 8/52, based on 8/70 technology and field upgradeable to it, offers 60% of the power of the 8/70 and 2.5 times the power of an 8/20. A midrange system, the 8/44 offers 50% more power than the 8/20. The 8/20, designed for use as free standing or remote host system, offers 33% more power than a similar 66/10.

All systems make extensive use of microprocessors, LSI circuit elements, and enhanced logic packaging techniques at board level. From this they derive cost and performance advantages over previous large scale systems. Microprocessor technology is used in the system's maintenance/diagnostic section, and is supported by LSI circuitry. In addition, the two smaller systems use bit-slice processors in certain execution units.

LSI circuits are also used within the processor's execution and control areas as well as in cache, directory, and control store. A high density universal (HDU) board allows high chip density on each board and, in conjunction with LSI circuits, reduces total number of boards in the system. These technologies offer reduced energy consumption, heat output, and floor space requirements.

The communications oriented GCOS 8 operating system provides the systems with multidimensional, multiprogramming, and multiprocessing capabilities. It offers expanded memory utilization, sophisticated memory management capabilities, high throughput, extensive modularity and flexibility, advanced transaction processing, and privacy and security capabilities. Multidimensional modes of system or program operation include batch processing, remote and interactive remote job entry, timesharing, transaction processing, direct program access, online document handling, and online test and diagnostics. All modes operate concurrently.

Architecturally the system allows full access of all user and system procedures to all configured resources of the hardware system with procedures isolated from one another through enhanced security capabilities. It also operates interconnected with Level 6 computers acting as remote terminal controllers and/or satellite processors; and permits interconnection of multiple host systems via network links between hosts and/or satellite processors and offers file transfer facilities for data exchanges.

Basis of the system's memory management is segmentation; the working space concept is also basic to the operating system. Memory management is controlled by a combination of hardware and operating system software and is transparent to applications, programmers, and users. Maximum physical memory is 64M bytes. Theoretical maximum managable logically addressable memory is 8T bytes.

Up to 511 concurrent processes are supported; 488 of these can be user processes. Tightly coupled multiprocessor configurations may operate under control of one copy of the operating system and associated system software. This functionality makes all coupled processors effectively interchangeable and enables them to share the load being processed. Online processor reconfiguration allows any processor to be deconfigured and later reconfigured without system interruption or manipulation of hardware switches.

Timesharing capabilities are provided through hardware extension features and the operating system architecture. The entire real storage minus OS residence can be used for timesharing. 400 concurrent users can be supported. User programs can use all processors simultaneously and transparently. Through a multicopy option, four separate timesharing worlds can operate concurrently and simultaneously in multiple processor configurations.

All systems operate under compatible versions of GCOS 8 and the existing GCOS III operating systems. Initial shipments will have GCOS III; GCOS 8 will become available in third quarter 1980. DPS 8/20 will be offered with GCOS 8 only.

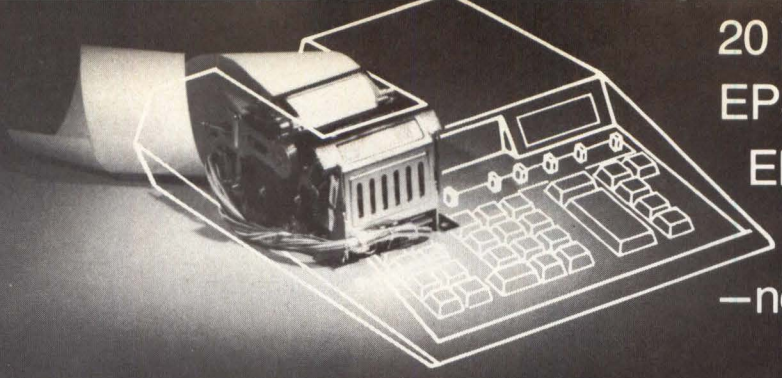
A DPS 8/20 consists of central system packaged in one cabinet and containing CPU, system control unit (SCU), 1M-byte main memory, and I/O multiplexer (IOM) with 19 channel function slots. Memory expands to the 2M- or 4M-byte level, and the system is field upgradable to the DPS 8/44 and can be configured with two frontend network processors. DPS 8/44 is similar in design, packaging, and memory options, but offers 50% more performance.

Offering 2.5 times the performance of an 8/20 the 8/52 is a midrange system. It consists of free standing central system composed of CPU, SCU, 1M-byte main memory, and IOM with 35 channel function slots, expandable to 54 slots. Memory expands to 8M bytes. The 8/52 is capable of supporting two frontend processors and two system consoles. The system is field upgradable to an 8/70.

A freestanding DPS 8/70 central system consists of CPU, SCU, 1M-byte main memory, and 35-slot IOM. Memory can be expanded to a 16M-byte maximum; I/O expands to 54 channel function slots; and three additional CPUS, IOMS, and SCUS can be configured. Eight frontend processors and four system consoles can be supported.

Purchase prices for systems in basic configurations are 8/20—$149,048; 8/44—$225.500; 8/52—$556,791; and 8/70—$1,156,399. GCOS 8 is scheduled for general release in third quarter 1980; DPS 8 systems will be available for delivery in second quarter of 1980.

Circle 176 on Inquiry Card



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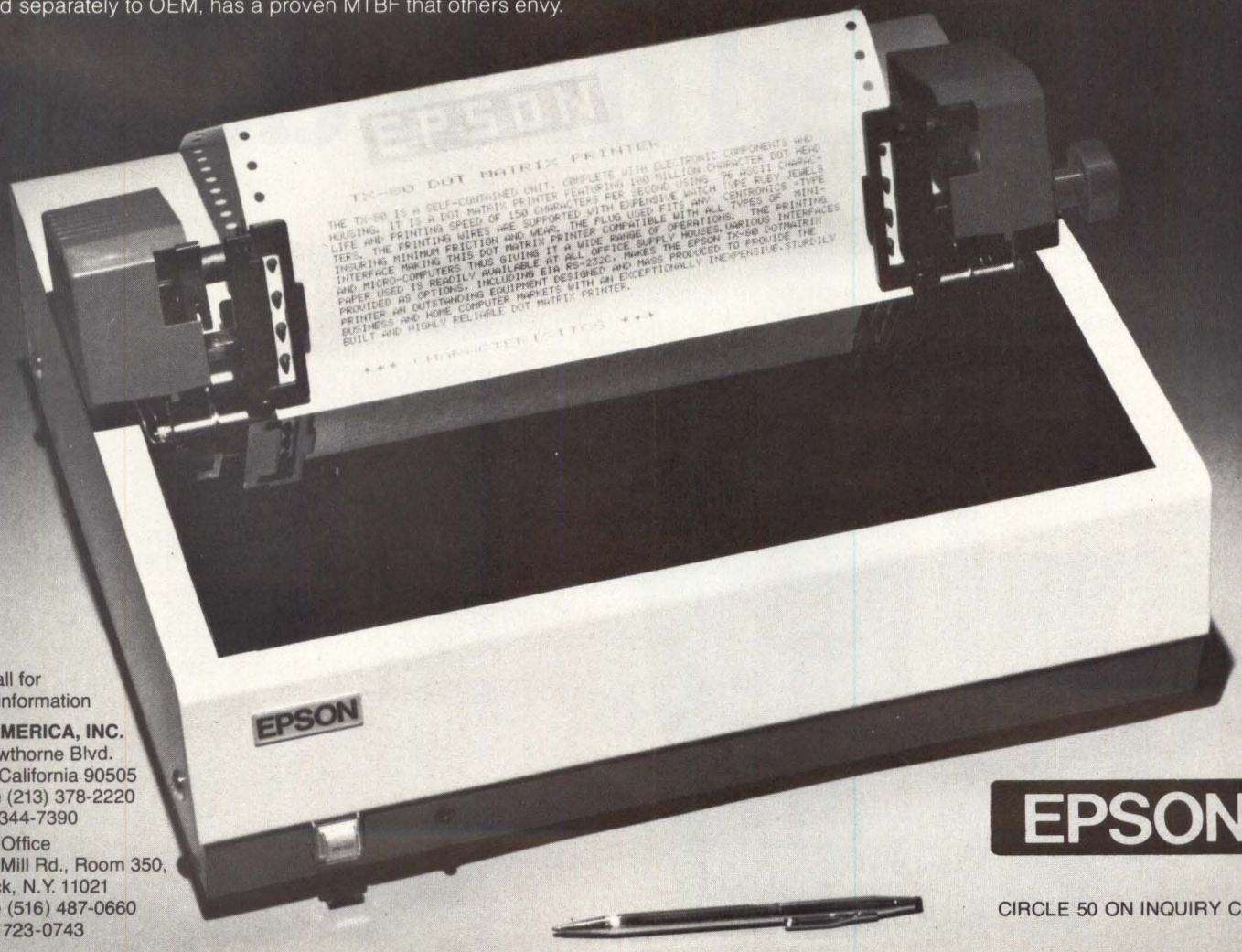

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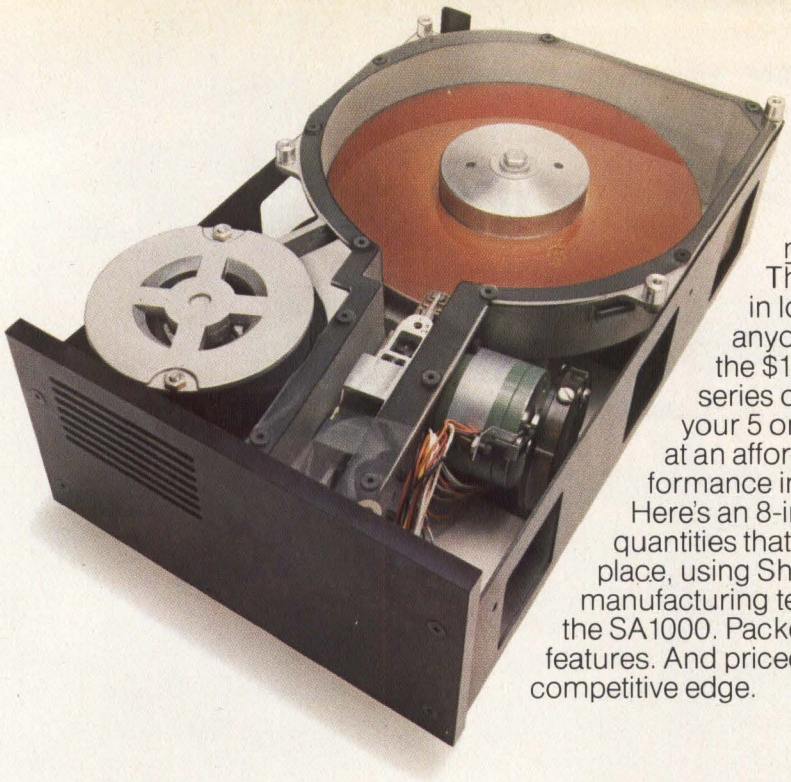

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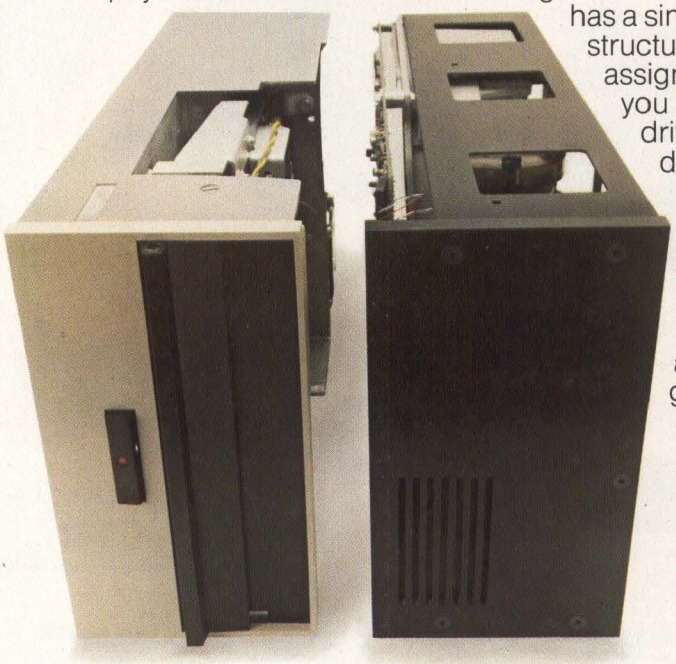

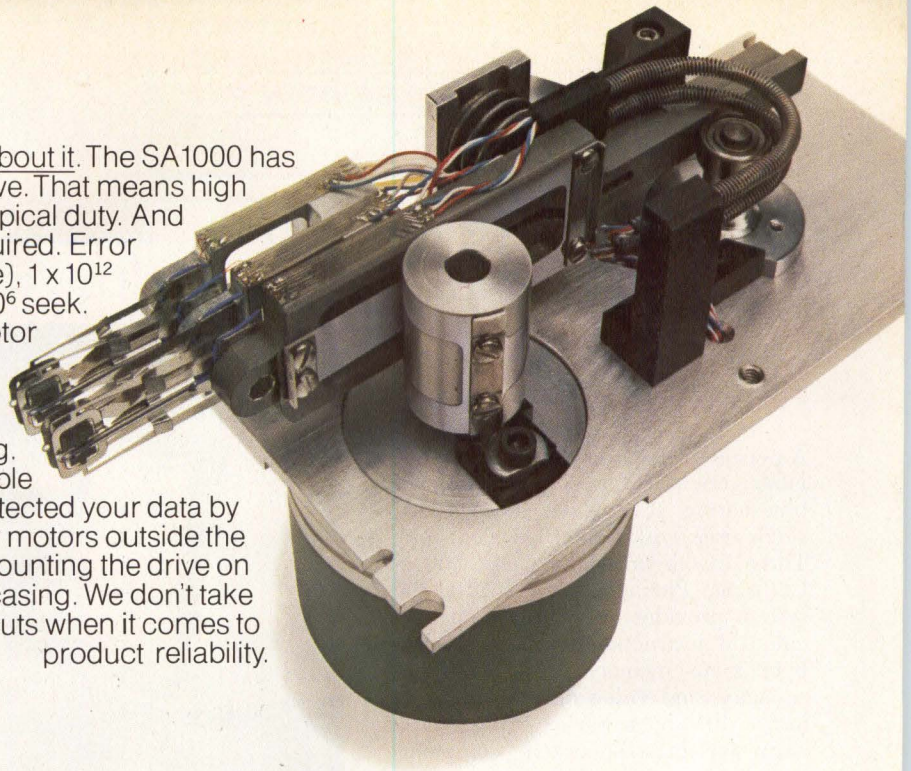

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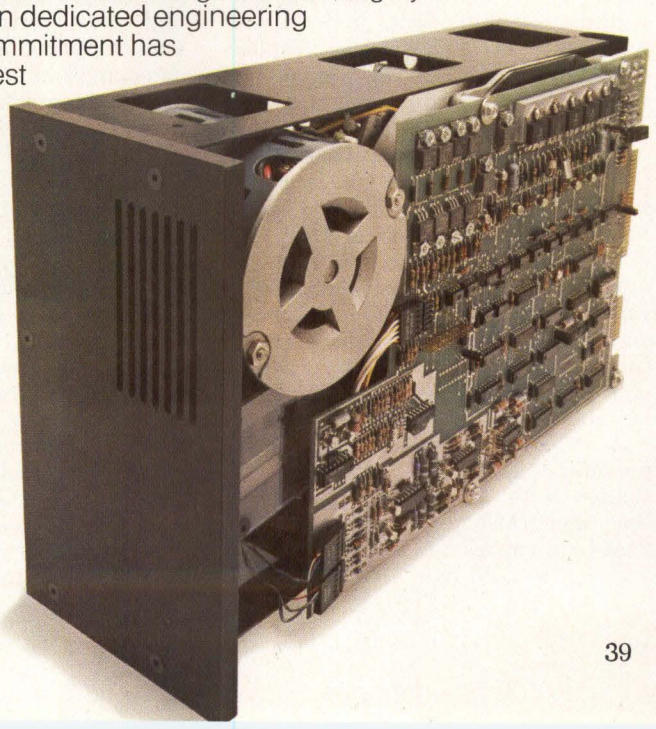
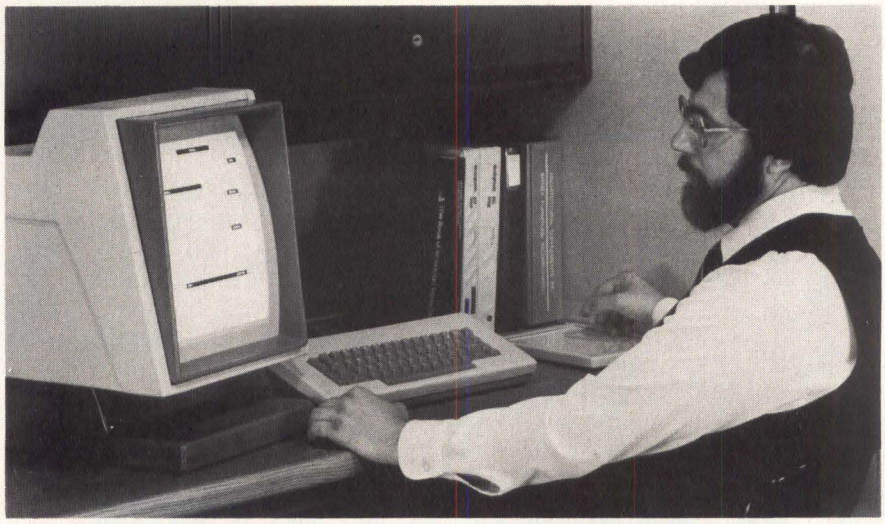


Shugart®

The Headstrong Company

CIRCLE 20 ON INQUIRY CARD

Single User Workstation Offers Assets of Timeshared Mainframe



Three Rivers' single-user PERQ computer offers 32-bit segmented virtual addressing mechanism, 256k-byte main memory, and 12M-byte online disc storage. System ties into packet stream network for communication with other similar systems

A personal computer for professionals, PERQ provides the sophistication of timesharing systems on a low cost, single-user workstation. Developed by Three Rivers Computer Corp, 160 N Craig St, Pittsburgh, PA 15213, the system provides a CPU that can execute 1M instructions/s; has a 0.25M-byte main memory, 12M-byte disc capacity, and video display; and ties into a 10M-bit/s Packet Stream Network for between-system communications.

System processor is a bipolar microprogrammed CPU that executes the highlevel P-code instructions used by many Pascal compilers at a rate of 1M/s. The processor has a 32-bit segmented virtual addressing mechanism that permits efficient execution of large programs, and includes instructions for operating on 8-, 16-, and 32-bit data. 256k bytes of RAM with 680-ns average cycle time is standard; a 1M-byte RAM option is available. A parity option is offered for the RAM. A 4k writable microstore is available; microcycle time is 170 ns.

Vertically oriented, the 8.5 x 11″ (21.6 x 27.9-cm) video display screen has 768 x 1024 resolution with 60-Hz noninterlaced black on white refresh. It displays multiple font, proportionally spaced text as well as complex flicker free graphics. The display bit map occupies a part of main memory, and hardware and microcode in the CPU facilitate rapid manipulation of the screen, allowing dragging, smooth scrolling, and online justification functions on the raster scanned image.

The onscreen cursor is positioned using a touch tablet. This finger activated pointing device is used to select and manipulate items on the display. Cursor movements track the position of the finger on the small rectangular tablet.

A 14″ Winchester technology disc provides 12M bytes of formatted storage with 97-ms average access time and 7M-bit/s transfer rate. A 24M-byte capacity is available as an option; a 1M-byte double-sided, double-density floppy disc drive is also offered.

The detachable 60-key solid state keyboard offers N-key rollover and auto repeat. A continuously variable slope Delta modulator used at a 16k-baud data rate supplies arbitrary stored speech output. Prerecorded data are stored on the disc to provide voice response, audible signaling, and other speech applications.

With full-duplex, multiple protocol high speed serial data port, the system supports asynchronous, bisynchronous, and SDLC/HDLC/ADCCP protocols at speeds to 56k bits/s. All line and protocol parameters are programmable and modem control is standard. A full IEEE 488-1975 standard implementation of the GPIB offers a simple way of compatibly interfacing a range of medium speed peripherals, laboratory facilities, or test equipment and instrumentation.

A proprietary wide band network interconnects PERQ systems on a single coaxial cable using cable TV technology. Up to 64 workstations can be connected on up to 2000′ (610 m) of cable. Broadcasting packets of data at 10M bits/s, the network allows one system to access files on another system. The network is also used to provide access to shared resources such as printers and tape drives, to allow all users to share resources.

Software facilities for the system are provided through an operating system designed to support a single user. Multiple process capability allows the user to have more than one context established at one time, providing rapid switching from editor to compiler to debugger. Background I/O spooling or network access does not interrupt the user. The distributed file system features multiple tree structured directories, linked and contiguous files, and access to files on other systems. A display window manager manipulates screen information, partitioning the screen into separate areas that may be moved, enlarged, or contracted in two dimensions, scrolled, and clipped under user control.

A full Pascal compiler included with the system has optimization algorithms to minimize code size and execution time. An interactive debugger, editor, and network support package are also supplied.

Cost of the system is $19,500 for a single unit; the network option is priced at $2000, and control store option at $3000.

Circle 175 on Inquiry Card

Disk Microcontrol at 4 million operations/second.

Signetics' 8X300 μP speeds bit-stream management without bit-slice bother.

Our 8X300 brings bit-slice speed to intelligent I/O control. Without bit-slice burden. Because the 8X300's control-oriented architecture streamlines software development.

At 4 million operations/second, it's the world's fastest bipolar μP. Much faster than any MOS device. And easy to implement for disk microcontrol.

As an IOP, the 8X300's got more than three years of rugged field experience in a wide range of control applications. When you design it in, look for lower parts count. Its high speed demands less external logic to move serial bit streams.

Check your price/performance goals for disk microcontrol. Whether for 5540 cartridge-type drives, or the latest breed of Winchesters, our 8X300 is tough to beat.

Fact is, we think you'll find that bit slice, brute-force TTL, and MOS aren't really options anymore. The 8X300 is the breakthrough device in a growing LSI family which we're developing for the disk controller OEM. Soon new Signetics parts will join it. And that's going to mean even greater design ease for microcontrol users.

Let us help you start moving from design to prototype to product, faster. Our brochure *Microcontrol Mastery* tells how one 8X300 user put a disk microcontroller on a single standard format board. Send us the coupon today.

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Computer Systems Serve Distributed Processing Needs

Small and medium scale computer systems, subject of two separate announcements made by Burroughs Corp, Detroit, MI 48232, extend the 900 family of computers to meet recognized demands for small systems in distributed and standalone processing applications. The B 1905, 1955, and 1985 additions to the 1900 series, do 30% more work in a given time than current machines and occupy 50 to 65% less floor space. B 91 and 92 models, initial units in the 90 series, operate at speeds two to five times faster than earlier small systems.

B 1900 machines incorporate advances in technology and design that include dense, fast logic and memory circuits, more efficient programming and control software, larger capacity main memory, and larger, faster cache memories. The systems use the company's variable micrologic architecture. In this design special sets of microinstructions act as interpreters, dynamically reconfiguring processor logic to optimize performance from one program to another.

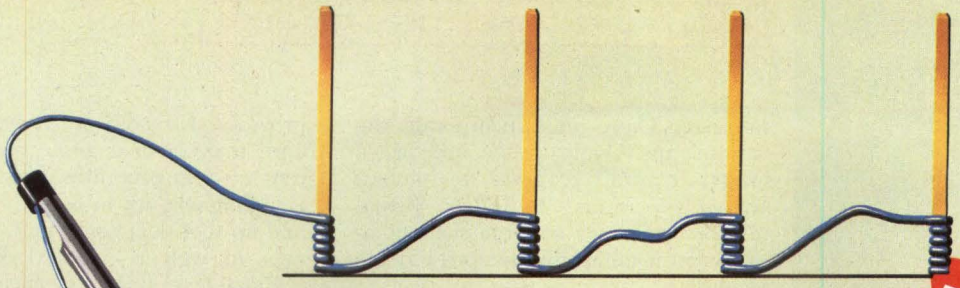
The CPU uses TTL bipolar microcircuitry and main memory formed of 16k MOS chips. The processor provides memory addressing to the bit level, eliminating the need for predefined structures such as words or bytes, and permitting full use of each memory position. Cache memory with 8k-byte capacity and a 55-ns access time is used to store interpreters for instantaneous retrieval. Processor logic includes simultaneous fetch/execute to effectively eliminate read access time from cache.

Entry level B 1905 systems operate in normal office environments. The 4-MHz central processor has a basic memory of 131k-bytes that is expandable to 512k bytes. A dual-disc drive provides 65M-bytes capacity, expandable to 530M-bytes. Standard on the system is a 320-line/min printer, single-line data communications control, and operator display terminal. Options include 650-line/min printer and second communications control.

The B 1955 configuration is based on a 6-MHz central processor with 512k-byte memory, expandable to 2.04M bytes. This system uses a 65M-byte disc drive (expandable to 1G bytes), 650-line/min printer, 8-line data communications control, and operator display terminal.

With dual 6-MHz CPUs, the B 1985 expands from 512k to 2.04M bytes of main memory. Its disc drive has a 130M-byte capacity that can be expanded to more than 1G bytes. A 650-line/min printer, 8-line communications control, and operator display terminal complete the system.

With prices beginning below $18,000, B 90 series units combine high capacity, high speed disc storage with fast internal speeds and advanced



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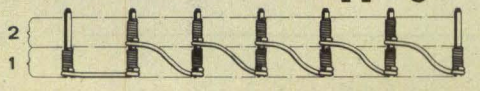
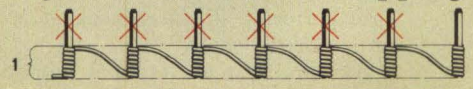
traditional Wire-Wrapping



JUST WRAP Wire-Wrapping



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CIRCLE 22 ON INQUIRY CARD

software. These units incorporate the variable micrologic design and use a master control program to govern system operation to offer virtual memory efficiency of large scale computers in a minicomputer price range machine.

Operating with the Super Mini-Disk II, a 6M-byte capacity, 157-ms access time disc drive that stores 3M-bytes of data on each of two flexible 8" discs, the B 90 can function both as a standalone data processing system or as a remote processor in computer networks. The systems can control their own network of terminals and simultaneously perform multiple data processing tasks. Terminals can be used as multiple data input and programming stations as well as for entering questions and displaying answers.

Central processors in series 90 units are formed using LSI circuitry and offer a 2-MHz cycle time. Basic memory is 128k bytes, expandable to 512k bytes. A 4k-byte memory is provided for cold start, warm start, and maintenance test routine. The CPU also incorporates from 6 to 11 I/O channels, up to 3 disc controllers, and up to 4 data communication channels, as well as onboard diagnostics.

Entry level B 91 systems incorporate processor, up to 512k-bytes main memory, display screen, electronic keyboard, 90-char/s bidirectional matrix printer, flexible disc storage, and related controls in a single cabinet. Peripherals include a wide line printer with speeds up to 650 lines/min; a choice of flexible, removable, or fixed media disc drives providing up to 46.8M-bytes online storage; and up to 11 I/O channels and 4 data communication channels.

A B 92 processor has the same basic memory capability but provides up to 11 I/O channels, up to 3 disc controllers, and up to 4 channels for data communication. Two line printers may be added to this system, as well as a magnetic tape cassette unit.

Circle 177 on Inquiry Card

Transaction Processing Software Reduces Programming Requirements

Pathway, a transaction processing system developed for use on Non-Stop™ computer systems, significantly reduces programming requirements and simplifies development of online transaction processing applications. Combining a set of terminal control processes, screen formatting language, user controlled application monitor, and interactive screen definition facility, the software system takes full advantage of the multiprocessing capabilities of the fault tolerant computer systems from Tandem Computers Inc, 19333 Vallco Pkwy, Cupertino, CA 95014.

Other capabilities provided by the software are ability to access multiple applications from the same terminal, and to perform online addition, modification, or deletion of transaction types, screen definitions, applications, and terminals. Programmers are released from consideration of terminal characteristics, thereby increasing productivity.

Further simplification of application design and programming is provided by the system's division of terminal control and file manipulation into separate programs. The software performs all data checking and format validation.

With the system, terminal oriented functions are isolated within terminal control processes (TCP); although each TCP can control multiple terminals, each terminal remains logically independent of the others and maintains distinct data areas and control information. An application monitor supervises and controls all working processes. This multiterminal control program that allows load sharing is the first to be executed and is responsible for initiating the rest of the system. An interactive screen definition facility supports online design and modification of screen formats directly at the terminal.

User application programs can be written in COBOL, FORTRAN, MUMPS, or T/TAL (Tandem/Transaction Application Language). The software supports terminals of several different types.

Licenses for the software are priced at $8500, plus a $2000/processor microcode charge. Deliveries are scheduled for February.

Circle 178 on Inquiry Card

Multitasking Computer Handles Network and Standalone Processing

SYFA® JR-200 series business systems bring power and versatility of larger, more expensive network processing systems to a level affordable in smaller applications. These members of the SYFA family from the Commercial Systems Div of Computer Automation, Inc, 2181 Dupont Dr, Irvine, CA 92713, incorporate performance features of their larger predecessors at approximately one-third the cost.

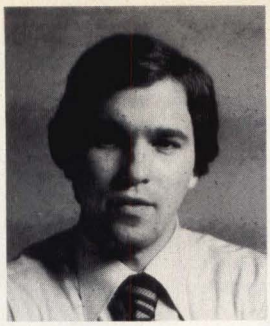
Basically 2- to 4-terminal systems, the units are compatible with the SYFA operating system, data communications software, and application program development aids. This provides capability to upgrade to large systems and to be assimilated into the Virtual Network™ concept. The -200 can grow into a full-scale network processor supporting 32 online terminals, all major communications protocols, and 2400M bytes of disc storage.

Designed both for use as a discrete dedicated computer system and to provide communications with a central mainframe computer, the systems use the same programming language and system software as the larger SYFA systems. This, in addition to the scaled down hardware configuration, adapts the systems to standalone applications or for use as network nodes in remote locations having moderate workloads.

Four Information Station CRT terminals, local or remote, 32M bytes of online disc storage, a spooled 150-char/s bidirectional character printer, and RJE capabilities are supported by Model A which provides 64k of MOS memory. The B version supports this configuration but replaces the character printer with a 600-line/min printer.

Software for the systems encompasses the SYFA Concurrent Logic Operating System that incorporates virtual storage techniques, a demand paging scheme, three file access methods, and dynamic allocation of all system resources. Each system can concurrently perform up to seven individual tasks, one synchronous communications task, and/or one batch utility program. Applications programs are written in the SYFA Business Oriented Language. Utility programs, programming aids for application development, and an IBM 3780 communications emulator are also included.

Circle 179 on Inquiry Card



"Take solder baths. Now that's what we should get rid of in our multilayer boards. But I want something just as reliable. Something that costs less."

Some good news. AMP

Expensive solder baths are gone... along with broaching, rupturing, distortion, tearing and damage to plated-through holes. All because you don't need solder with an AMP ACTION PIN Contact. Most important, these inherently more troublefree contacts are now available in a range of standard I/O connectors. Just insert the contacts and snap on the housings. It's a truly simple way to fewer rejects and easier repairs in a smaller amount of space.

The contact's AMP-engineered compliant design has proven reliable in thousands of feed-through post and mother/daughter card applications.

Choose from subminiature D Type connectors for RS 232 and 449 applications, a popular telecommunications style, or shrouds which quickly convert feed-through posts to headers for use with .050" centerline ribbon cable. In each case, you get a completely solderless back panel. And repair of damaged contacts is easily accomplished without degrading mechanical and electrical performance.

So take the trouble out of your panel making. With AMP ACTION PIN Contacts, I/O Connectors and Tooling. For more details, call the AMP ACTION PIN Information Desk at (717) 564-0100, Ext. 8400. Or write AMP Incorporated, Harrisburg, PA 17105.

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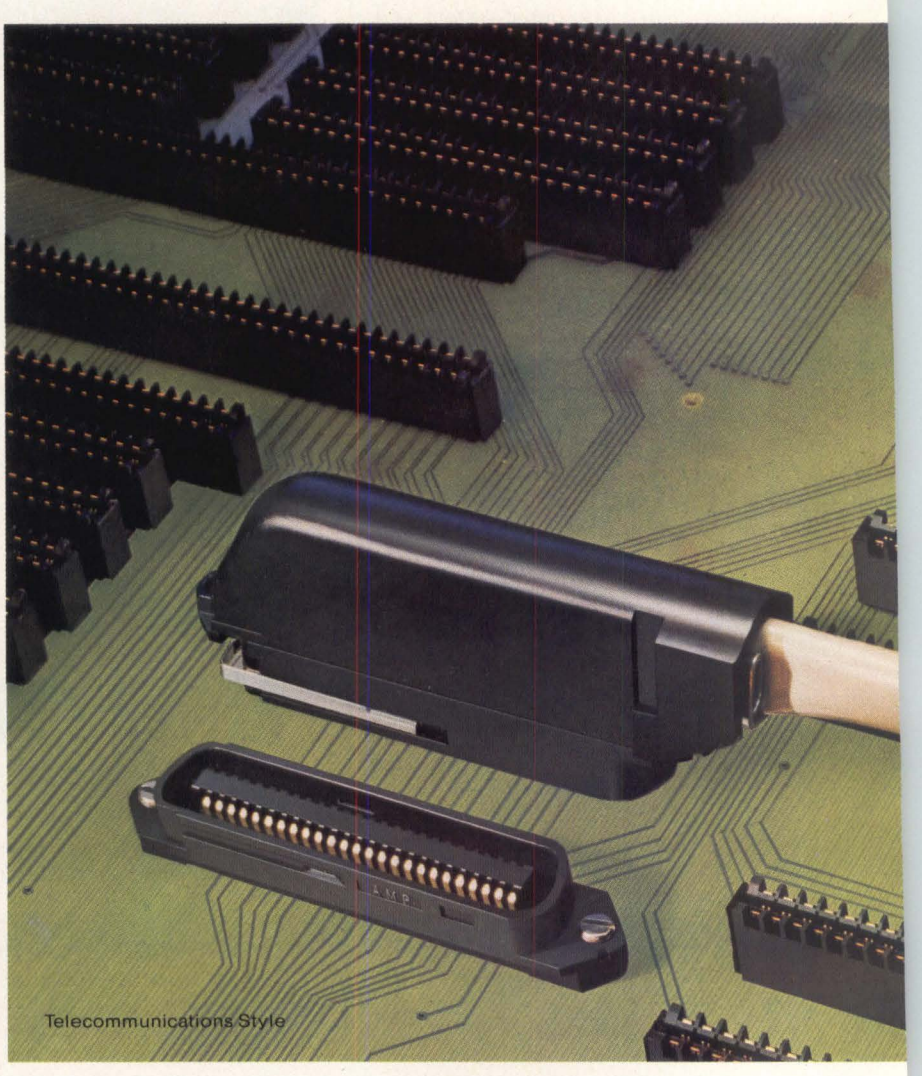
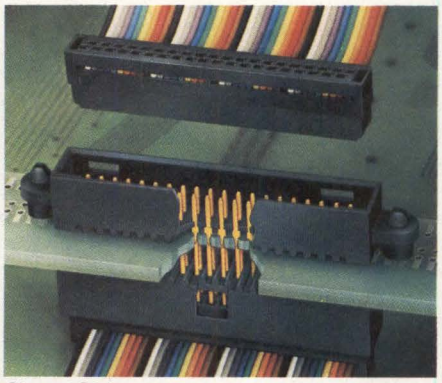


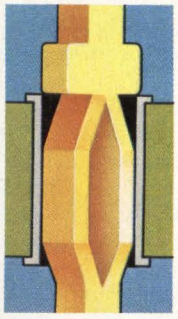
Telecommunications Style

ACTION PIN Contacts.

Subminiature D Style



Shroud Style



Contacts feature unique compliant pin design.

Some facts worth knowing about AMP ACTION PIN Contacts

Tooling: Complete range available from prototype to production rates in excess of 10,000 an hour.

Assemblies: Boards preassembled to your specifications with AMP components are available from panel suppliers. Contact AMP Incorporated for more details.

Environmental Tests:

Test	Type		Results in Milliohms				
			Change in Resistance, △R				△R Values
			Min.	Max.	Mean	Std. Dev.	(95% CL)*
Thermal Shock and Vibration: −65° to +125°C for 5 cycles; 10-200 Hz three planes, 12 hours	Gold	3A	0.058	0.281	0.121	0.038	0.301
	Tin press fit	3A	−0.002	0.176	0.094	0.046	0.313
High Humidity: 96 hours at 40° ±2°C, 90-95% RH	Gold	3A	−0.043	0.017	0.010	0.017	0.070
	Tin press fit	3A	−0.066	−0.016	−0.028	0.011	0.026
Salt Spray: 48 hours at 5% concentration NaCL	Gold	150mA	−0.076	0.034	−0.008	0.022	0.098
		3A	−0.052	0.051	0.013	0.021	0.113
	Tin press fit	150mA	−0.062	0.062	−0.012	0.028	0.121
		3A	−0.056	0.049	0.007	0.026	0.129

*Exceeded by fewer than 1/10,000 samples.

Where to telephone: Call the ACTION PIN Information Desk at (717) 564-0100, Ext. 8400.

Where to write: AMP Incorporated, Harrisburg, PA 17105.

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AMP

CIRCLE 26 ON INQUIRY CARD

Touch Panel Switches Are Based On Membrane Switch Concept

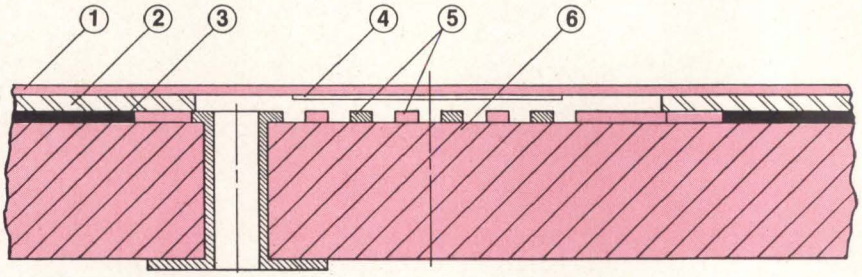
Four groups in the TIP® (touch in panel) switch line meet performance specifications and cost goals of industrial, medical, and appliance users. By providing both switch and electronics in an integrated subsystem, the manufacturer, Oak Technology, Inc, Switch Div, 100 S Main St, Crystal Lake, IL 60014, has resolved the problems encountered when discrete components are acquired from different vendors.

A combination of simple concepts and complex engineering, the switches are light, flat, thin, sealed front panels with graphics, nomenclature, colors, and pictograms. Although they operate with a light touch, they can withstand a heavy hand, are mounted and interconnected, and have a 10M-cycle life expectancy. The switch line includes devices having integral electronics package, rotary or other switches, or potentiometers.

The switches consist of (1) substrate with stationary conductors formed on it that are spaced from each other, electrically isolated from each other, and form the two contact points to be switched; (2) membrane with flexible movable conductor applied to its underside; and (3) spacer, an insulator that is placed such that the membrane is held several thousandths of an inch above the substrate. These three parts are assembled so that the flexible conductor on the membrane is spaced from and immediately above the conductors on the substrate.

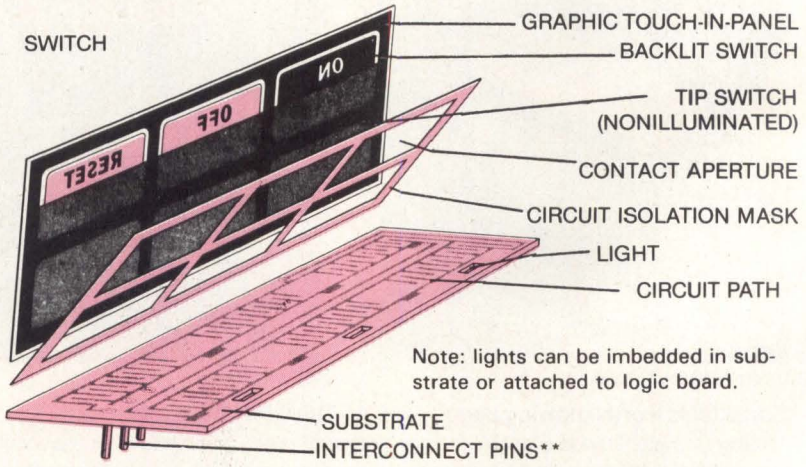
When a finger or other actuator applies pressure, the flexible membrane is forced through an opening in the spacer, so that the movable conductor makes contact with the fixed conductors on the substrate, shorting them together and thus closing the switch. When the actuating member is removed, resiliency of the flexible membrane causes it to return to the normal position.

Formed with conductors on both sides of the substrate with interconnection between front and rear conductors, Product A provides high switch and interconnect density and long life. Switches can be placed anywhere on the panel as close as

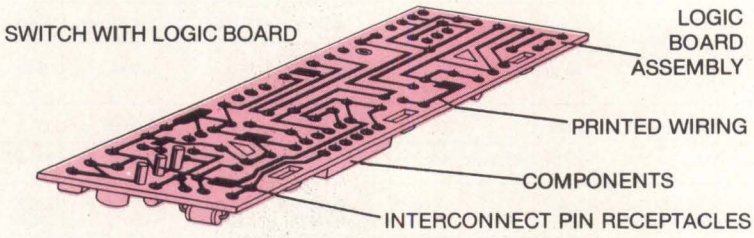


1. MEMBRANE
2. SPACER
3. GROUND PLANE
4. FLEXIBLE CONDUCTOR
5. FIXED CONDUCTORS
6. PC BOARD

Touch In Panel switches from Oak Technology are based on a membrane switch concept. Switches consist of substrate with stationary conductors, membrane with movable conductors, and spacer



**Note: Interconnect pins are commonly used when a logic board system is required.
Interconnect pins, edge connectors or flexible connectors are commonly used when logic board system is not required.



Providing both switch and electronics in integrated subsystem, TIP switches fill needs for high switch and interconnection density with longevity in severe environments. Concept allows simple components to be mounted, forming complete assembly

TODAY MAY BE THE BEST TIME TO MAKE YOUR CAREER MOVE

But first make sure your new employer measures up.

With all of those prospective employers trying to attract your engineering skills, now is the best time to look beyond "just a job" and consider your career. Your real objective is to find the perfect combination—challenge, satisfaction, security, and reward. To assist you, we've prepared a checklist of points to consider when you're evaluating a new employment possibility. It's a good way to compare the companies seeking your expertise.

Career Opportunity Checklist for Engineers

INDUSTRY GROWTH AND STABILITY

No one wants to be "phased out," so check for security:	YES	?	NO
Is the company part of an industry that's vital, growing, dynamic?	☐	☐	☐
Will the growth continue throughout the 1980s and beyond?	☐	☐	☐

COMPANY HISTORY AND REPUTATION

You can tell a lot about a firm by its track record:			
Is the company recognized and respected in the industry?	☐	☐	☐
Have sales and profits increased at a steady rate?	☐	☐	☐
Is it known for its technological innovations?	☐	☐	☐
Are its employees motivated and well rewarded?	☐	☐	☐
Does the company seek technological employees on a permanent, ongoing basis?	☐	☐	☐

WORKING CONDITIONS AND ENVIRONMENT

Look for good people, team spirit, and top-notch facilities:			
Is the atmosphere one of loyalty, pride, and achievement?	☐	☐	☐
Do employees welcome the challenge of difficult assignments?	☐	☐	☐
Are creativity and independent thinking encouraged?	☐	☐	☐
Are the company's engineering goals clear-cut and attainable?	☐	☐	☐

THE COMPANY LOCATION

Relocation is a big professional and personal commitment.			
Is the company located in an existing or emerging electronics center?	☐	☐	☐
Are there major universities and other technological resources nearby?	☐	☐	☐
Will the company assist me in relocating?	☐	☐	☐
Can I provide my family a comfortable lifestyle in this area?	☐	☐	☐
Are there cultural and entertainment opportunities?	☐	☐	☐
Is there a variety of recreational and leisuretime activities?	☐	☐	☐
Are the climate and surroundings pleasant?	☐	☐	☐

PERSONAL AND PROFESSIONAL GROWTH

Job satisfaction means more than just a paycheck:			
Does the company give full recognition to the engineering role?	☐	☐	☐
Will I be working and interacting with other talented professionals in my field?	☐	☐	☐
Will my accomplishments be acknowledged, appreciated, rewarded?	☐	☐	☐
Will I be encouraged to seek more challenge and responsibility?	☐	☐	☐
Will the company pay for advanced training in technology and management?	☐	☐	☐
Can I pursue my own career goals within the company framework?	☐	☐	☐

THE LONG RANGE PICTURE

Where will you be professionally in 5 years?...in 10 years?			
Are there plenty of opportunities for rapid advancement within the company?	☐	☐	☐
Does the company encourage engineers to assume positions of authority?	☐	☐	☐
Will I be allowed to move into those engineering areas that interest me most?	☐	☐	☐
Can I choose my own career path—into technological leadership or executive management?	☐	☐	☐

One Company to Evaluate

At Racal-Milgo, we're looking for capable communications hardware and software people to join our engineering team. Our success has created needs at every level, from entry to top management. We have a lot to offer you.

The mainstream of our business is data communications—where today's action is. We're a pioneer, and a recognized leader in the field. Our state-of-the-art product lines include modems, multiplexers, data encryption, and systems for sophisticated network control and performance assessment.

We're proud of our growth—$64 million in sales two years ago, $80 million last year, and over $100 million this year—and we're still growing. Applied research and technology keep us on the leading edge in data communications; our engineers face some of the industry's most challenging (and rewarding) responsibilities.

Racal-Milgo is a great place to work. We encourage our technical people to think creatively, to turn their innovative ideas into successful products—in an atmosphere of friendly, professional teamwork. We provide them with one of the nation's most advanced engineering facilities. Our salaries and benefit programs are among the best in the business.

We're located in suburban South Florida, one of the growing new electronics centers in the sunbelt. It's an international area, gateway to Latin America, blessed with a pleasant climate year-round. There are excellent cultural and entertainment opportunities, plus swimming, diving, boating, sport fishing, golf, tennis, and all the other benefits of a cosmopolitan resort. There's a wide choice of employee clubs to introduce you and your family to new activities. And if you're interested in furthering your professional or business related education, we'll pay for your coursework at any of the major universities nearby.

At Racal-Milgo, we're experiencing dynamic growth, and we need good people at all levels. The working conditions are excellent...advancement and rewards come fast...and our new two-track career program lets you decide whether to rise to the top on the technical side or to move into management. (Our president and board chairman are both EE's.)

We're looking for the best. If you are too, let's get together. I hope to personally welcome you aboard. Send me your resume today; no letter required. You'll receive a prompt reply.

Ed Hilpert

Ed Hilpert
Vice-President, Engineering

Racal-Milgo™

Racal-Milgo, Inc.
8600 N.W. 41st Street Miami, Fl. 33166

CIRCLE 19 ON INQUIRY CARD

0.5" (1.27 cm) on center. This configuration also permits simple components to be mounted. When implemented using a double-sided plated through hole PC board, it is designated APC.

Fixed conductors are formed by PC traces. The membrane is a polyester sheet 0.005 to 0.007" (0.127 to 0.178 mm) thick with nomenclature, graphics, and flexible conductor back printed by silkscreen techniques. The spacer is made by punching holes in a polyester sheet. Substrate, spacer, and membrane are bonded together to form a complete assembly.

Product B offers a medium or nondense switch configuration, nondense interconnect pattern, and no component mounting. This switch has conductors on one side of the substrate. A BPC unit is formed with print and etch PC technology; screening a conductive paint onto a rigid substrate results in product BSS.

Having the same characteristics of Product B, Product C uses a nonrigid polymer film substrate that may be attached with an adhesive to a rigid substrate. The flexible substrate can have an integral interconnect "tail" when a suitable connection scheme is provided to attach it to the customer's circuit at the other end. Constructed using a plated copper conductor PCB, these units are suitable for severe environments. When a flexible silk screened silver conductor substrate is used, they adapt to low cost consumer goods.

Microprocessor systems or other associated circuitry for logic and timing functions can be incorporated as part of the switch substrate or added as interconnected PC boards. The switch panel will interface with all control logic. The panel can be provided with feed through pins, or terminals. Flat cable, flexible cable, or edge connection can be included. The switching system can be completely front sealed against liquids, dust, or other contaminants.

Circle 180 on Inquiry Card

Upgraded Connector Series Meets MIL-C-38999 Performance Requirements

Super Series I™ meets stringent performance criteria of MIL-C-38999 Revision G without requiring total replacement of existing connectors, by maintaining intermateability with Series I connectors. The connector, introduced by Bunker-Ramo Corp's Amphenol North America Div, 2122 York Rd, Oak Brook, IL 60521, offers an alternative in high shock, vibration, and emi/emp environments.

The "scoop-proof" high density circular environmental connectors feature a bayonet coupling mechanism, self-sealing rear grommet, closed entry hard front socket inserts, and rear release crimp removable contacts. Designed and successfully tested to performance requirements of MIL-C-38999 Revision G, the unit retains the polymer contact retention construction of earlier Series I connectors, thereby offering up to 115% greater dielectric separation than metal clip contact retention systems used in competitive devices.

Among the major modifications that distinguish this device from earlier designs is the coupling design (patent pending), the use of emi grounding fingers, and elimination of bayonet holes. Design of the coupling eliminates the conventional detent or locking area on the bayonet track, and the wear resulting from the high pressure produced in this area during vibration or mating/unmating operations.

In the upgraded series, the bayonet track has no detent or locking area; locking is achieved by use of a stainless steel detent ring that is located at the rear of the coupling ring (see diagram) and separate from the coupling track. This detent ring is keyed to and rotates with the coupling ring to engage three stainless steel pins or rollers located in the plug shell. The resulting stainess steel/stainless steel detent achieves 500 mating cycles rather than the 250 cycles achieved with the stainless steel/aluminum detent of Series I connectors.

Elimination of bayonet holes excludes possible intrusion of sand, dust, and moisture into the coupling area. Emi grounding fingers are incorporated in the design to increase

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you need MAXIBOX.™

MAXIBOX is a full-scale minicomputer designed to outperform any 16-bit and most 32-bit computers.

Any of the 15 slots in its flexible backplane can be used for I/O controllers, CPU options, peripherals interfaces, and up to 1 MByte of fast, economical MOS memory. Its standard 256 KByte configuration leaves you with 9 "nondedicated" slots for total design flexibility.

No other mini of any size can offer 26.7 MByte bandwidth on a computer that requires only a 115Vac utility outlet. With 600 ns ECC MOS memory for maximum computation speed and a virtually universal backplane, MAXIBOX is a must for "peripheral intensive" designs or products where speed, space and power are prime considerations.

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Writable Control Store allows you to tailor the MAXIBOX to your product environment. Regional Processing Units let you develop sophisticated intelligent I/O controllers and give you parallel processing never before available; it's like having an independent processor attached to the MAXIBOX for discreet I/O functions.

We feel that for the product OEM concerned with simplified design and maximum return on investment, MAXIBOX is the best minicomputer available. To find out more about the MAXIBOX, return the coupon for additional literature, specifications and pricing information. Or, call SYSTEMS toll-free.

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CIRCLE 28 ON INQUIRY CARD


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Memory Module
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Multiple Choice Memory

Intel's new modular Series 90 system with BXP™ bus lets OEMs build to suit.

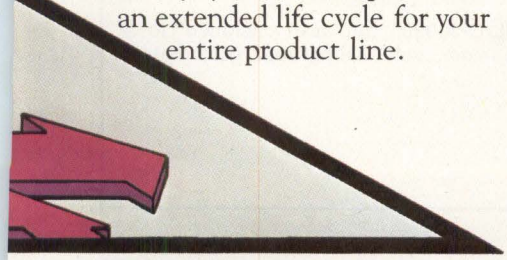
Choose your capacity. Choose your memory technology. Choose your speed. Now you can choose from a wide range of performance features that precisely match your product requirements—all with a single memory system.

Intel's Series 90 gives designers a ready-made family of memory modules and intelligent controllers that dramatically simplify and speed-up OEM memory design. Better yet, Series 90 eliminates the cost of designing new memory interface and control circuits for each new system and each new performance or density upgrade.

New bus standard for memory systems

The key to Series 90's design flexibility is our BXP bus. It's the first bus standard made exclusively for memory systems, and it's designed to make interfacing easy. Connect your system directly to the BXP bus or use our standard control interface.

Intel's BXP architecture lets you build to today's customer needs with flexibility for the future. The BXP bus will accommodate vastly increased capacity, including tomorrow's higher density memory technologies as they arrive. And you won't have to redesign even then. Intel's BXP bus adds up to more efficient memory system development and an extended life cycle for your entire product line.



Performance to spare

Series 90 memory modules incorporate Intel's highest performance semiconductor memory components to give your systems the competitive edge. Our static memory modules use revolutionary HMOS* technology to provide capacity from 32-64K bytes each with 100 ns cycle times. Or build with Series 90 dynamic memory modules for 128-256K bytes and cycle speeds of 350 ns.

Even better, our BXP bus allows you to interleave modules or combine both static and dynamic memory in the same system. However you configure, Series 90 lets you achieve the highest speeds with no performance penalty.

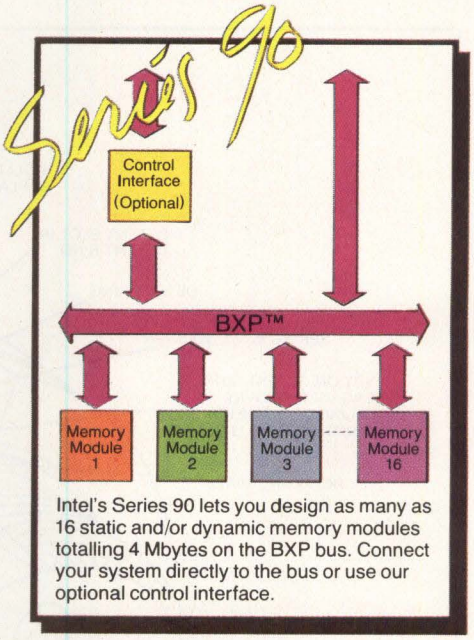
Address up to 2 billion bytes

Series 90 gives you plenty of memory for today's applications—plus wide open capacity for growth. Our BXP bus can accommodate word sizes from 16 to 80 bits plus Error Checking and Correction. It can easily address up to sixteen Series 90 memory modules for a maximum capacity of 4 megabytes. Entire Series 90 systems can be daisy-chained for even greater capacity.

Whether you're adding more of today's memory technology or upgrading to higher density components of the future, our BXP bus stays with you. It has addressing space already allotted for up to 2 billion bytes.

ECC for unimpeachable data integrity

A primary function of Series 90's optional control interface is our ECC feature. With single-bit error correction and double-bit error detection, it gives your system the highest data integrity available. The controller also supports an optional error logger and display.



Intel's Series 90 lets you design as many as 16 static and/or dynamic memory modules totalling 4 Mbytes on the BXP bus. Connect your system directly to the bus or use our optional control interface.

Non-stop to market

Series 90 memory modules and controllers are available now, so you can start designing today. For complete information, plus our convenient Configuration Guide, contact your local Intel sales representative. Or write Intel Corporation, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051.

*HMOS is an Intel patented process.

CIRCLE 29 ON INQUIRY CARD

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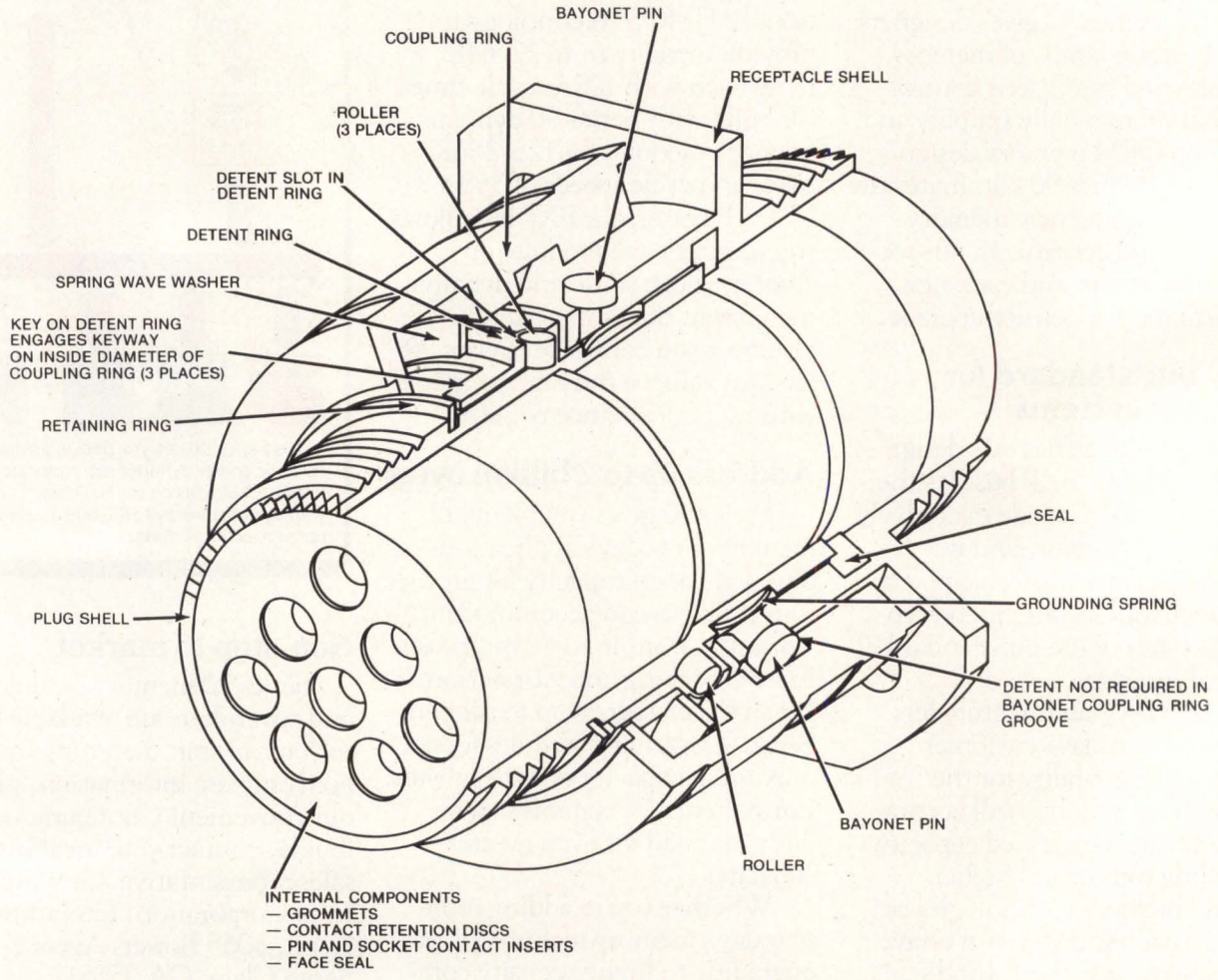
emi/emp attentuation to 90 dB at 100 MHz and 65 dB at 10 GHz.

There are 29 insert configurations in the upgraded connector line and a choice of 6 shell styles in sizes 9 through 25, including straight plug, wall mounting, jam nut, and box mounting receptacle. Connectors may be ordered in electroless nickel or olive drab cadmium over nickel finish. Pertinent technical performance data include capability of withstanding vibration in excess of 80 G rms, and shock of 65G with 11-ms duration.

By retaining intermateability with standard Series I military connectors, the units can be substituted for them by replacement of the readily accessible plug. Receptacles mounted on black box electronic equipment need not be changed to attain higher performance standards. The replacement process is further eased by the interchangeability of existing backshell hardware cable clamps, inplace crimped contacts rfi adapters, and contact insertion withdrawal tools between series. □

Circle 181 on Inquiry Card



ISOMETRIC DRAWING — AMPHENOL® SUPER SERIES I PLUG CONNECTOR

Amphenol's Super Series I plug connectors meet performance requirements of MIL-C-38999, but are designed to intermate with existing connectors. Design features include bayonet coupling mechanism, self-sealing rear grommet, closed entry hard front socket inserts, and rear release crimp removable contacts

This Dual Floppy/LSI-11 does everything the 11V03-L will do in half the space...

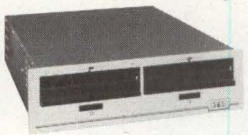
and gives you RX02 software/media compatibility, too!

The MF-211 Dual Floppy/LSI-11/2 system, featuring the low-cost CRDS Double Density Controller, is functionally identical to the DEC 11V03-L, but uses only 10½″ of rack space!

PLUS:

- KD11HA, DEC LSI-11/2 central processor
- Dual Shugart Drives
- Double and single density operation
- Complete LSI-11/2 software compatibility
- Over one megabyte of storage per system
- 4 Quad slot or 8 quad slot backplane
- Upgradable to LSI-11/23
- Unique CRDS controller with all interface, bootstrap loader and formatter electronics on one dual-height PC card, with complete RX02 software media/compatibility

. . . And for RX02 plug-replacement:
The FD-211 is a compact, low-cost, highly reliable plug-replacement for RX02 applications in 5¼″ low-profile chassis.



PLUS:

- Complete PDP-11, LSI-11 compatibility
- Switch and photocell write-protect
- Bootstrap loader
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CIRCLE 30 ON INQUIRY CARD

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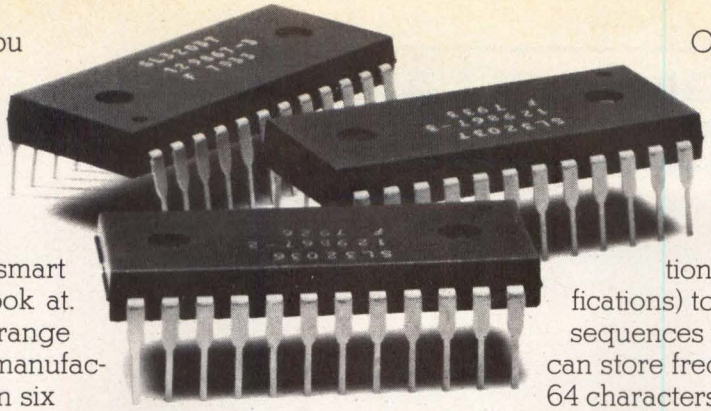


PERSONALITY PROMS AND FACTORY ASSISTANCE MAKE USER-REPROGRAMMING A SNAP.

At Lear Siegler, you don't have to decide among dozens of smart terminals, each offering something slightly different, each not quite right for you.

We have just two smart terminals for you to look at. But they can handle a range of tasks it takes other manufacturers four, five, or even six models to accomplish.

Of course, we realize that some terminal manufacturers might say that two models aren't enough to qualify as a complete line. But we like it that way.

After all, we want to make your life simpler, not more complicated.

THE ADM-31 & ADM-42 WILL LET YOU CHANGE THEIR MINDS.

When we designed the ADM-31 and ADM-42, we realized we couldn't second-guess our customers. Because no matter what capabilities we gave them, somebody out there might want something different. So we did the next best thing.

We gave each a truly flexible personality by putting the instruction sets inside their PROMS. So, unlike the hardware, the firmware is capable of easy OEM reprogramming, thanks to the fully-documented programming instruction manual we provide. And you end up with a terminal that performs to your exact specifications.

We even have a special Application Engineering Staff to answer any questions you may have about reprogramming. Consult with you on interfacing problems. Help you set the terminals' personality. Explain the features and functions. Talk about special applications. Or even suggest something you maybe never thought of.

Feeling your life getting simpler yet?

THE ADM-31 & ADM-42. ALL THE TERMINALS YOU'LL EVER NEED.

Even if you decided not to reprogram their PROMS, our two terminals come with all the standard features you need in a smart terminal. And then some.

Features like full editing capabilities. Formatting. Reduced intensity for identification of protected fields. Blinking, blanking, and reverse video. High resolution monitors. Even limited line drawing capabilities.

What's more, both the ADM-31 and ADM-42 come equipped with a microprocessor, making them even more reliable and easy to use. Because their design architecture has a microprocessor with multiple microprocessor-based controllers that tie into the master.

Nor did we forget those indispensable function keys. Naturally, both the ADM-31 and ADM-42 have them.

On the ADM-42 for example, you get 16 function keys, shiftable to 32 functions, and optionally programmable to store up to 64 characters. This lets you store escape code functions (such as personality modifications) to reduce several escape sequences to one key stroke. And you can store frequently-used phrases up to 64 characters, which provides you with impressive time savings.

When you get right down to it, the ADM-31 and ADM-42 are really functions of your imagination.

THE CHOICE IS SIMPLE. THE CHOICE IS YOURS.

So the ball's in your court.

Choosing your new smart terminal can go one of two ways. You could start sifting through dozens of data sheets, talking to dozens of salesmen, and looking at dozens of expensive, slightly different terminals.

Or you can look at two smart terminals from Lear Siegler — the ADM-31 and ADM-42. Complete with user-reprogrammable personality, function keys, and an eager and willing Applications Engineering Staff to help you with any problems you may run into during the reprogramming.

The choice seems pretty easy to us. But if you want more information, call or write to us at Lear Siegler, Inc./Data Products Division, 714 North Brookhurst Street, Anaheim, California 92803, (800) 854-3805. We'll be happy to tell you all about the ADM-31 and ADM-42.

And show you how you can make your terminals behave.

LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

Lear Siegler, Inc./Data Products Division, 714 N. Brookhurst Street, Anaheim, CA 92803. (800) 854-3805. In California (714) 774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices San Francisco (408) 263-0506. Los Angeles (213) 454-9941. Chicago (312) 279-5250. Houston (713) 780-2585. Philadelphia (215) 968-0112. New York (212) 594-6762. Boston (617) 423-1510. Washington, D.C. (301) 459-1826. England (4867) 80666.

CIRCLE 31 ON INQUIRY CARD

Five Minicomputers Control Entire Wood Processing Plant

All production processes in the A/S Union wood processing plant at Skien, Norway are fully supervised and controlled by a distributed computer system developed by Noratom Industrial Process Control, Holmenveien 20, Oslo 3, Norway. Five minicomputers made by Norsk Data A/S, Lindebergveien nord 20, Oslo 10, monitor and control the entire plant, which is said to be the only one of its kind in Scandinavia.

Set up in a parallel configuration of computer pairs, the computers are programmed such that under emergency conditions two can take on all duties necessary to maintain operation with no adverse effects on production. As an indication of complete confidence in reliability, there is no conventional form of emergency or standby control. The entire wood processing plant—6-unit digester, washing and screening, sulphite liquor evaporation, combustion, and chemical recovery—is supervised by a configuration based on Noratom's CONSUP system for control of industrial processes.

Through individual keyboards and trackballs, each of four operators in a central control room can request diagrammatic representations of any portions of the process to appear on a color CRT for study. Modification in the process or instructions for specific operations can be ordered in a similar manner from the operator panel for immediate action and a confirmation report.

Only those portions of the process that require aid or change need be analyzed. The other parts are automatically controlled without interference from modification instructions.

System Description

Developed and designed in cooperation with the OECD Halden Reactor Project, a Norwegian nuclear research center, the CONSUP system is based on use of a group of dedicated but program compatible minicomputers with a common memory, plus a "background" computer for program development and data collection. Although the dedicated computers in the A/S Union plant originally were Norsk Data NORD-10M OEM versions and the background computer was a NORD-12, all are now NORD-100 single-board minicomputers.

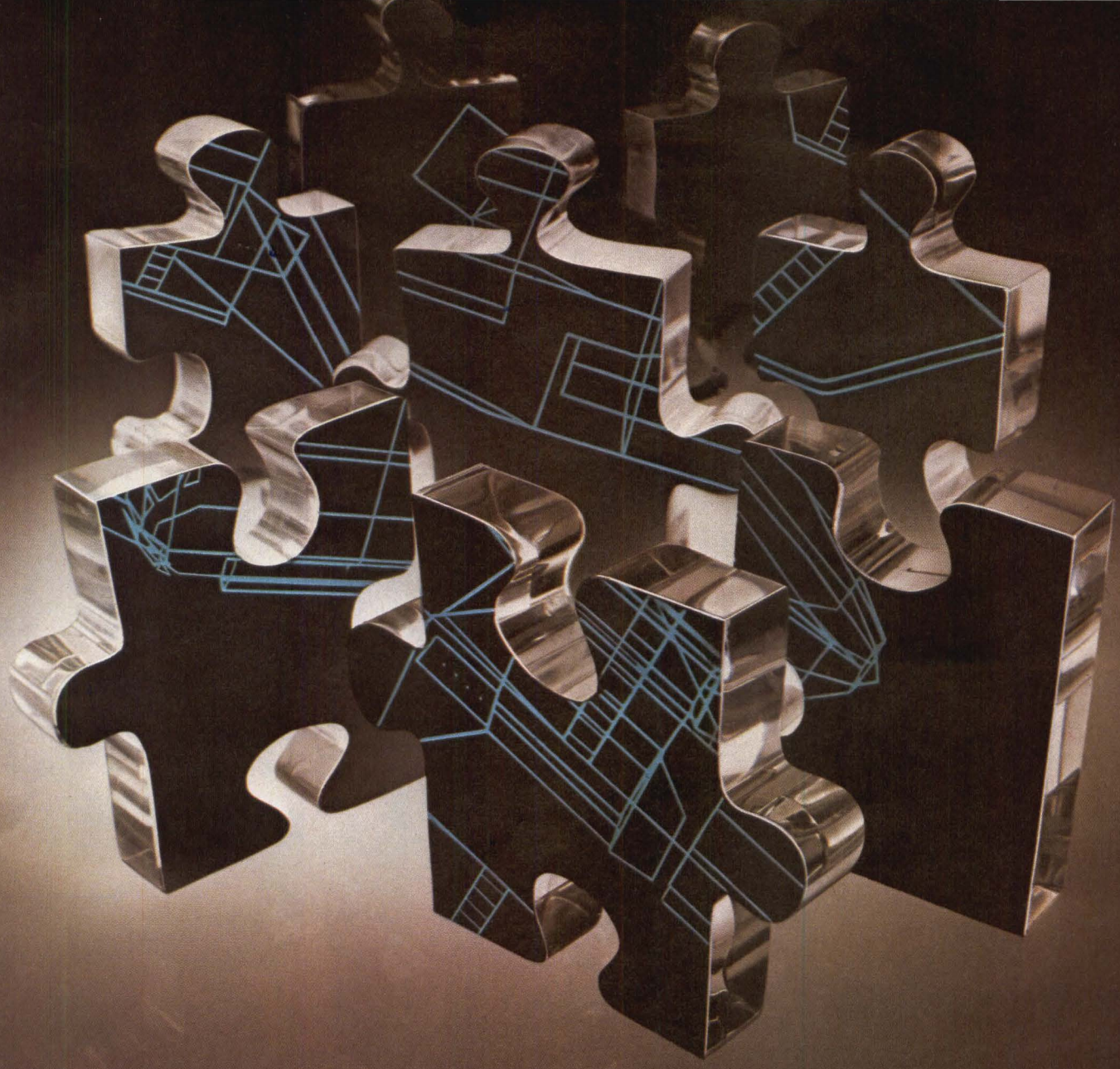
The CONSUP distributed computer system is divided into four functional blocks (Fig 1): process control, process data base, operator communications, and background processor. All parts of the system communicate through the process data base (PDB), a common memory for the system that is continuously updated by the process control units to maintain realtime status of the process.

Communications units retrieve and process information from the PDB for operator review and transfer operator commands back to the PDB for execution by the process control units. Intelligent interface controllers in the PDB control data traffic and reduce the probability of interference from malfunctioning parts of the system. Data transfer is through serial interfaces.

Process control units are made up of control processors (minicomputers) plus input/output (I/O) circuits for interface to the process. Each control unit monitors and supervises a portion or all of the process, updates the PDB on process status, and executes programmed control functions and operator commands.

I/O signals are made up of both analog current or voltage I/Os and digital on/off signals. The process contains 960 standard 4- to 20-mA analog sensors that measure valve position, temperature, pressure, level, flow, weight, and motor current. Digital signals consist of 150 control loop inputs and 1000 start/stop and increase/decrease outputs.

Each NORD-100 single-board minicomputer consists of a 16-bit parallel microprogrammed central processing unit with bit, byte, single-, double-, and triple-word, and register file instructions; eight memory addressing modes; fixed and floating point arithmetic with 48-bit single precision; 128k bytes of virtual address space and 32M bytes of main memory; and 16-level priority interrupt system with each level having a set of eight central registers. Other features include bootstrap loading in firmware from discs, writable control store, in-



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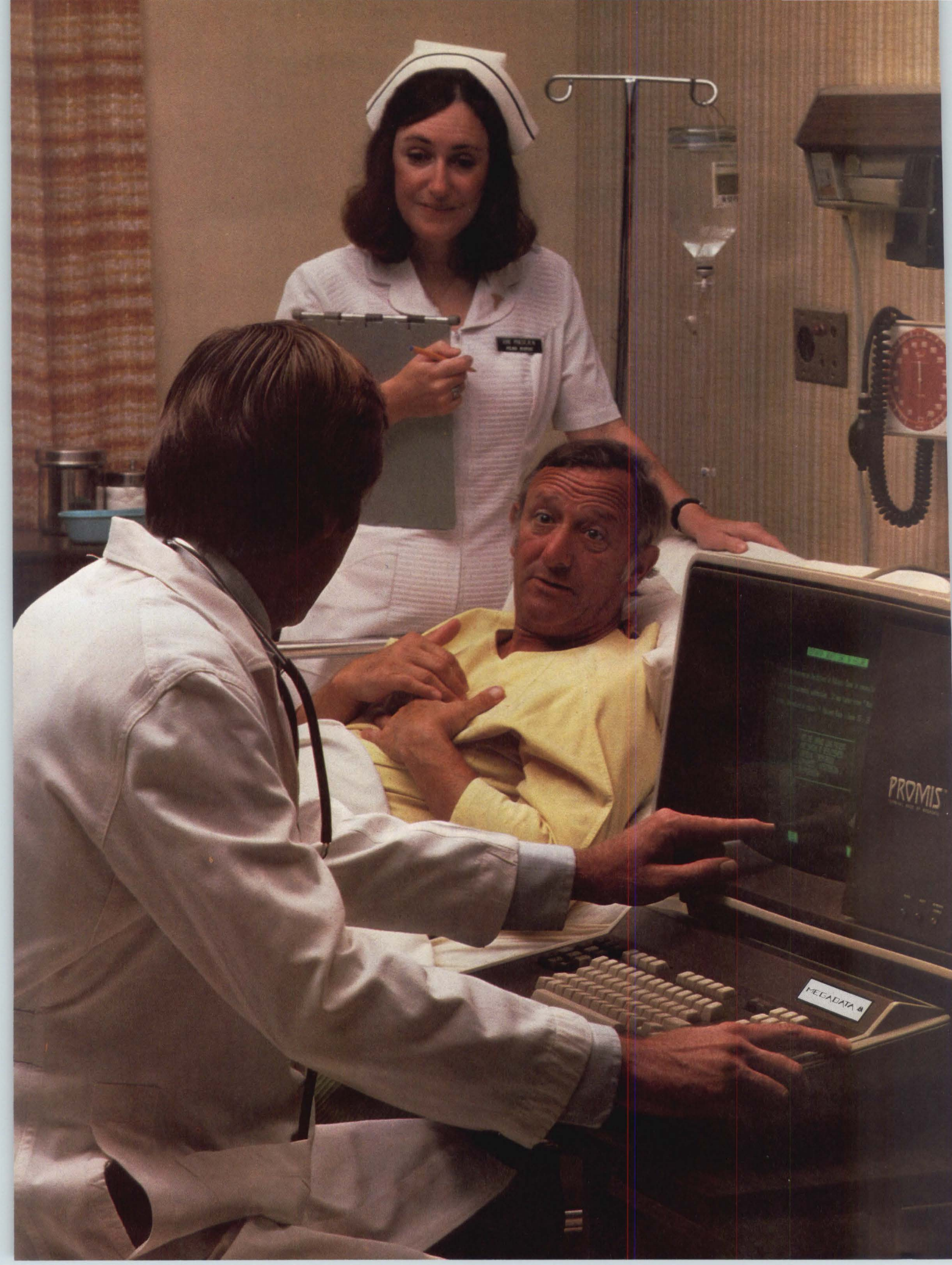
CIRCLE 32 ON INQUIRY CARD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CIRCLE 33 ON INQUIRY CARD

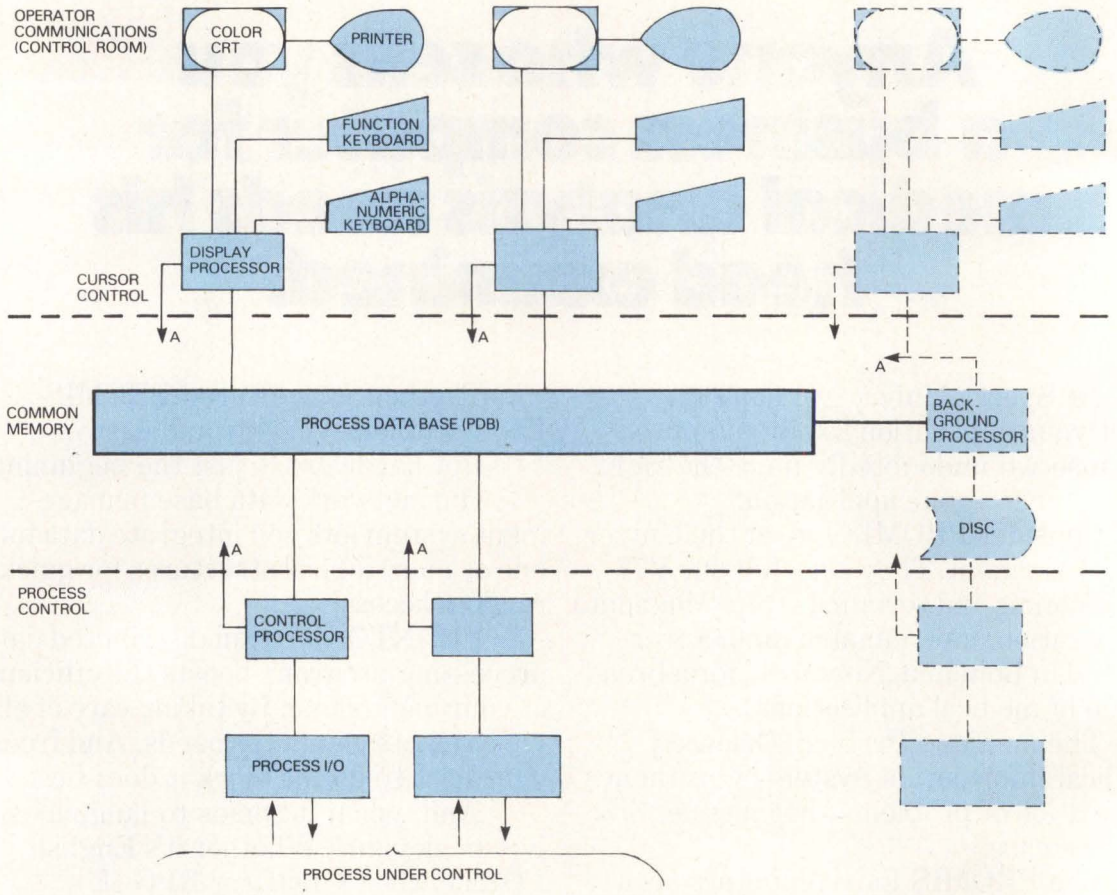

Fig 1 CONSUP distributed computer system for control of wood processing plant. Process database (PDB) serves as common memory for other system units: operator communications, process control, and background processor. Each of five processors (NORD-100 minicomputers) continuously updates PDB which stores all inputs from process equipment and all commands from the operators

struction prefetch, firmware monitor, optional 2k-byte cache memory, and optional fast cycle.

Among the peripheral units for a typical minicomputer system, as shown in Fig 2, are a display terminal with color CRT and keyboard, rackmounted or freestanding floppy disc drives for up to 308k bytes of memory, as many as eight hard disc drives for a total of 2304M-byte capacity, a variety of magnetic tape drives, 160-char/s matrix printers, 300/600/1000-line/min printers, and electrostatic printer/plotters. Communications equipment includes synchronous and asynchronous modem controllers and direct memory access interface.

A microprocessor, operating independent of program execution, drives the operator's panel, containing a digital clock with battery backup and a digital display for debugging from the system console. When power returns after a power failure, the system automatically restarts and the realtime clock is updated by the digital clock.

Because the PDB is the only single unit in the system that might cause total system failure if it malfunctioned, it is protected from possible disturbances caused by malfunctioning of other parts of the system. Power supplies are duplicated and an error correction scheme automatically corrects all 1-bit errors.

Interface controllers detect transmission errors and protect the memory from them. In order to access data in the PCB, interfacing units must match a password assigned to each data element or block.

Operator communications units (Fig 3) are made up of a console containing a 625-scan line color CRT mon-

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You'll love letting Data I/O's System 19 do your programming while you do the important things.

Once you've developed a PROM program on your development system, simply download it into a Data I/O System 19. This frees your development system for the next person who needs it.

Later, if you discover that a statement has been left out, or you need to edit the program, you can use the System 19 to make all the necessary changes without once interrupting work being done with the development system. And your System 19 can program every kind of bipolar and MOS PROM—not just the few MOS PROMs that most development systems program.

The System 19 saves you time by eliminating the need for you to build software packages so your development system can transmit data to the programmer. System 19 offers all these development system object code formats in a single package:

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Best of all, Data I/O System 19 is priced within just about everyone's budget.

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Programming systems for tomorrow...today.

CIRCLE 34 ON INQUIRY CARD

itor, display processor (minicomputer), terminal controller, function and alphanumeric keyboards, cursor control trackball, and audible alarm. All components in the console connect to the display processor. The software definable function keyboard is configured to meet the specific requirements of the process being controlled; the alphanumeric keyboard allows plain language communication.

The background processor, a minicomputer with disc storage and printer for hardcopy records, is used for program development and simulation. In addition, it serves as a storage medium to enable quick restart of the control and display processors. This processor also collects and evaluates long-term maintenance data, automates measurements, generates reports, and performs general processing of data.

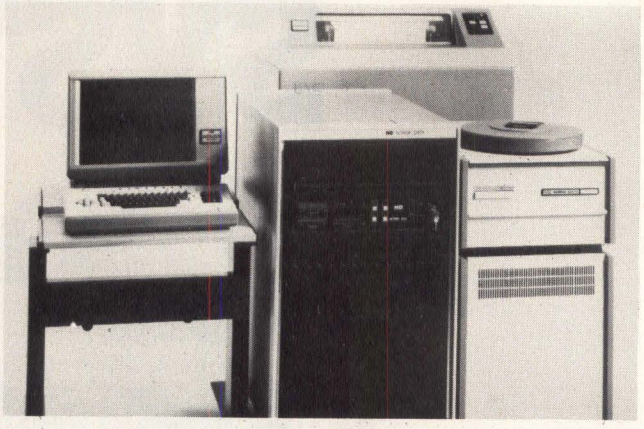

Fig 2 Components of typical NORD-100 minicomputer system. Single-board 16-bit computer interfaces with color CRT terminal, floppy and hard disc drives, printers, and magnetic tape drives

Functional Description

Analog and digital inputs from all process equipment being monitored, operator instructions, and control parameters (setpoints, alarm limits, configuration commands) are stored in the PDB. Data from local memory are transferred to the PDB at intervals specified for the type of variable and need for data. However, process control units routinely maintain control, perform redundancy switchovers, and carry out process procedures independent of the PDB.

Display processors tie the operator to the PDB by presenting needed data in the form of mimic or block diagrams; alphanumeric alarms, status tables, or measurements; bar graphs; or trend curves with variable time scales. Images requested by the operator are generated, picture elements are connected to variables or groups of variables, and images are updated by frequent access to the PDB. These processors also keep track of variables not related to the current display in order to alert the operator when important changes in equipment status occur.

Frequently used diagrams and displays are generated and stored by the display processor, while others are stored in the background processor and transferred to the display processor on request. When process change signals are detected by the process control unit, a control processor outputs a signal to change a value in the PDB. The display processors scan the PDB to detect such changes and then convert the changes to the correct display and position. Irregularities trigger a light or sound alarm according to priority and specify to the operator which diagram is involved. On occasion, the operator may use this capability for noncrisis alarms by introducing thresholds within normal operating

Fig 3 Operator communications units at control room. Each of four consoles contains color CRT display, display processor, terminal controller, function and alphanumeric keyboards, and trackball. Operator calls for diagrammatic display through commands on function keyboard and chooses area for study by moving trackball. Alphanumeric keyboard enables plain language communication

ranges in order to be notified when those limits are passed.

Most operator commands are entered through the function keyboard. An operator presses one or more buttons to select a required display, uses other buttons to specify a choice of fixed functions, and manipulates a third group to choose variable functions. To enter a command, the operator moves the display cursor to the appropriate symbol on the screen and presses the associated button on the keyboard. However, before that command is passed to the PDB it is checked for validity by the display processor.

Software

Operating system SINTRAN III is a general purpose system based on a virtual storage concept with additional features such as output spooling. Each interactive terminal is allotted an equal share of system resources, but time-slicing provides each operator with the feeling of total command of the computer.

Operations such as multilingual programming, data entry and retrieval, and file manipulation are performed without time lags. Several realtime programs can be run simultaneously by assigning task priorities. Batch operations include both multiple local batch streams and remote batch emulator software. Batch processing does not interfere with realtime tasks.

DC&AS BRIEFS

Microprocessor Based Data Entry/Display Terminal Provides Simplified Interface

Communication in serial ASCII with 20-mA current loop and RS-232-C/V.24 conditioning at up to 1 mi (1.6 km) from the CPU is enabled by the TM25 Microterminal at a fraction of the cost of a full-scale CRT and printing terminal. This 8.5 x 4.5 x 0.6" (21.6 x 11.4 x 1.5-cm) device from Burr-Brown, PO Box 11400, Tucson, AZ 85734, contains an 8-digit LED display, seven function indicators, hexadecimal or numeric keyboard, and seven function keys on its waterproof front panel.

Buffered data entry permits message verification before transmission to the CPU and allows the terminal to transmit complete messages at maximum speed. Depressing a function key generates preprogrammed action by the user's CPU. These key functions are defined in CPU software and identified on the terminal's panel. Function indicators show CPU acceptance of keyboard entries and can be programmed to initiate operator action. Both power and signal I/O are provided through a single RS-232 connector. □

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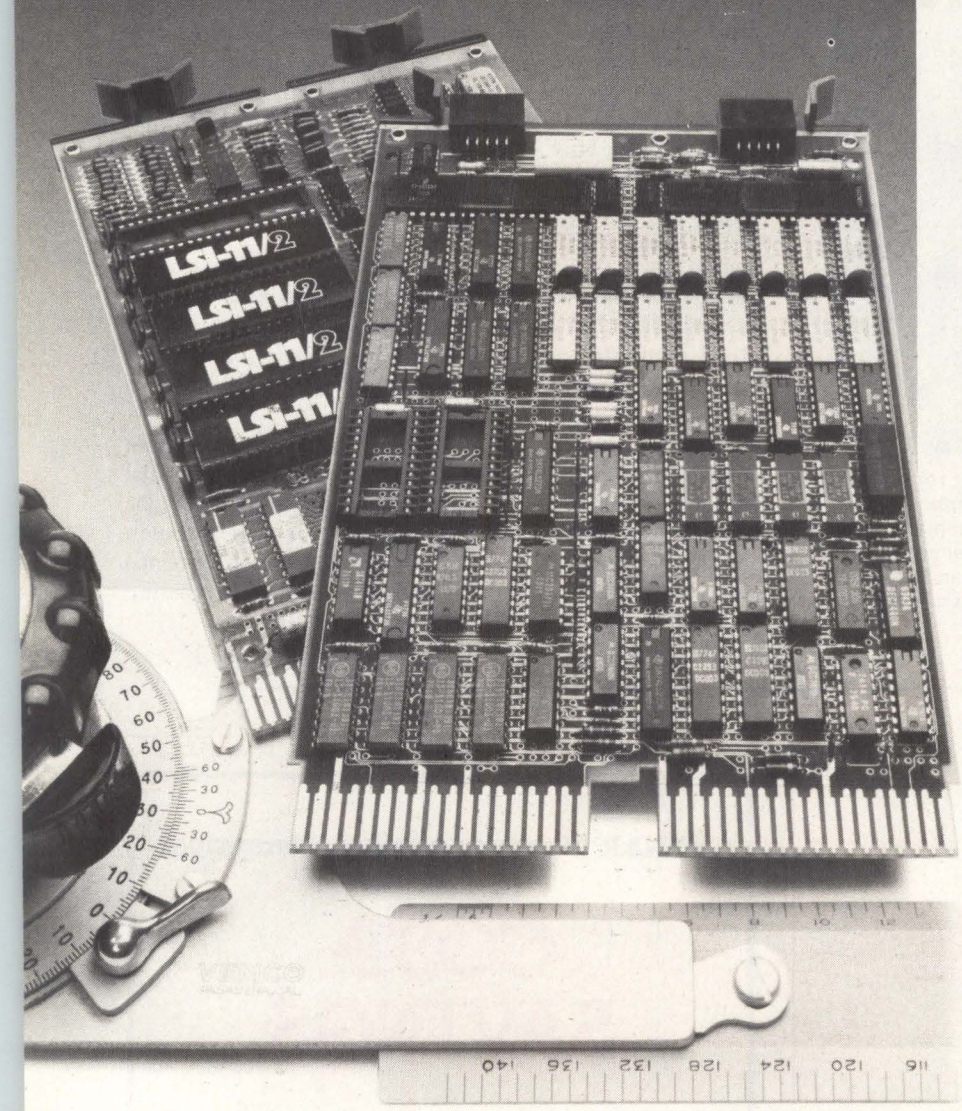

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SEMICONDUCTOR MEMORY UPDATE—PART 1: ROMS

A comprehensive perspective clarifies the availability of semiconductor memory types and technologies, beginning with read only memories, to assist designers in developing reliable, efficient, and cost-effective computer storage implementations

Eugene R. Hnatek Monolithic Memories, Incorporated, Sunnyvale, California

Availability of semiconductor memories—random access, read only, charge-coupled, and magnetic bubble—offer many memory component combinations that can meet specific design criteria. This 3-part overview of the various technology options, along with type of memory and fabrication process, has been arranged to help the designer to make the necessary tradeoffs, thus assuring reliable and cost-effective memory use. Part 1 analyzes ROMs; parts 2 and 3, to be published in consecutive months, will present similar in-depth summaries, respectively, of RAMs and higher density technologies (principally CCDs and magnetic bubbles).

Improvements in computer system work potential have been achieved through the realization that processor technology could be distributed, software could be produced to control the resulting network, and memories could be organized to allow access to local and global data bases. Vast, low cost memories, hierarchically organized according to speed and thus cost, make the data to be processed available to a system with minimal or no human intervention. In addition to effecting a possible decrease in systems software overhead, the provision of direct access to greater volumes of data improves application speed, freeing more time for increased processing.

Large, cost-effective memories can also augment system usage by providing more space for software. This factor, in turn, has a significant and positive impact on the cost of software production and maintenance. Developments in very large scale integration (VLSI) will make megabit storage chips a practical reality in the early 1980s (eg, the Intel 7110 1M-bit bubble memory).

A single semiconductor chip in 1985 will contain a relative performance equal to that of an IBM 370/158 high end mainframe. The 8080 microprocessor has a performance equivalent to about 1/100 that of the /158. VLSI technology continues to drive down the cost of computing, while increasing performance will create a fundamental reversal from centralized data processing to dispersal of processing power. However, this reversal complicates the management of data processing functions. In addition, VLSI combined with low cost hardware will allow the implementation of inexpensive software.

Advent of the 4k dynamic n-channel metal oxide semiconductor (NMOS) random access memory (RAM) resulted in the adoption and proliferation of semiconductor memories in lieu of ferrite core for bulk storage applications in the 1973-1974 time frame. This choice was based on device reliability, performance, cost, and

TABLE 1

Semiconductor Memory Types and Applications

Application	Memory Technology
High Density Bulk Storage	64k NMOS dynamic RAM, magnetic bubble, MOS ROM
Microprogram Writable Control Stores	Magnetic bubble, static NMOS, ECL, and TTL RAM
Disc Replacement (Fixed and Floppy)	16k/64k dynamic RAM, magnetic bubble
High Speed	Bipolar (TTL/ECL), static NMOS RAM
Byte Organization (Microprocessor Support)	Static NMOS/CMOS RAM, bipolar P/ROM, CMOS/NMOS EPROM, programmable array logic
EPROM Compatible	Static NMOS RAM, MOS ROM
Low Power	CMOS P/ROM-RAM, static and power shutdown NMOS RAM
Nonvolatility	Bipolar P/ROM, magnetic bubble, bipolar/MOS ROM, EAROM
Intelligent Terminals	Magnetic bubble, static NMOS RAM
Peripherals	Magnetic bubble, bipolar P/ROM-ROM, MOS EPROM, EAROM, static RAM

the potential for further dramatic price reduction. The increased density available with 16k and 64k RAMs, coupled with increased and unprecedented performance (high speed, low power, etc) due to circuit design innovations, reduced memory storage cell sizes and processing, and masking innovations, has firmly entrenched the use of semiconductor memory for computer applications. In addition, the microprocessor and its widespread use in computer applications has further increased the use of semiconductor memory in mainframe computers.

Technology Background

Different categories of semiconductor memories and specific data storage applications where they find primary use provide system designers with a wide range of options (Table 1). In general, MOS electrically programmable read only memories (EPROMs) and dynamic RAMs are used extensively in microcomputer and minicomputer applications, while slow electrically alterable read only memories (EAROMs) are more suited to peripherals, at present. In addition, large volumes of dense dynamic MOS RAMs are used in small and large mainframe computers for bulk storage. Bipolar programmable read only memories (P/ROMs) provide high speed microprogram capability to microcomputers, minicomputers, peripherals, and small and large mainframe computers. Bipolar RAMs serve as scratchpad and file memories in minicomputers and small and large mainframe computers. The most recent category of memory that is receiving considerable attention is the MOS static RAM, which is challenging the bipolar RAM from performance and cost viewpoints, both in buffer and cache applications and in microcomputer and peripheral applications. Magnetic bubble memory, charge-coupled device (CCD) memory, and high density (32k and 64k) MOS read only memories (ROMs) find extensive applications as tape, disc, and drum memory replacements and as bulk storage.

Discussion of the relative merits of semiconductor memories centers on packaging density (maximizing the number of bits or cells per chip), speed of the memory system in terms of access time (the faster the speed, the shorter the access time), and cost per bit of storage—a widely used figure of merit to compare various memory technologies. Figs 1 and 2 compare cost per bit versus access time and price per bit versus storage capacity, respectively, for several categories of semiconductor memories. As shown in Fig 1, bipolar technology has the shortest access time but at the highest cost per bit, whereas CCDs and magnetic bubbles exhibit both a lower cost per bit and longer access time. Fig 2 shows that MOS RAMs, CCDs, and magnetic bubbles have similar storage capacities but at differing prices. Thus, the particular memories that are ultimately selected depend on several tradeoff constraints.

A prime distinction between memories is the manner in which information is stored (written) and accessed (read). RAMs involve column and row matrices, which allow information to be stored in any cell and accessed in approximately the same time. By contrast, serial access means that information is stored in column order, and access time depends on where the desired bit is with respect to the sensing station. Shift registers

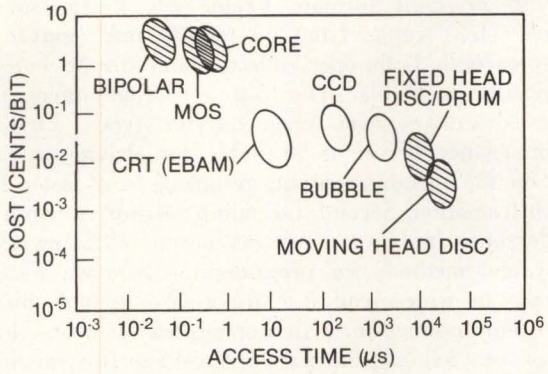


Fig 1 Memory type and cost per bit vs access time. Bipolar RAMs have lowest access times (highest speeds) but also greatest costs. Magnetic bubbles and disc/drum memories are slow speed devices but at lowest cost

are examples of serial access memories. On a larger scale, CCD and magnetic bubble memories are types of shift registers that are gaining use in low speed applications. They are not, however, based on transistor-cell configurations.

Permanence of information entered is indicated by the designations of read/write (R/W) memory and ROM. A R/W memory permits data to be entered or read out at any time. In contrast, a ROM may have data entered either permanently or semipermanently, mainly for readout purposes. Thus, in ROMs, a permanent program is fixed or unchangeable, while a semipermanent program is reversible and changeable.

As for process technology, memories employ the same manufacturing processes and variations as digital logic systems. These include the bipolar technologies—transistor to transistor logic (TTL), emitter-coupled logic (ECL), and such variations as Schottky TTL and integrated injection logic (IIL), plus the MOS technologies—p-channel MOS (PMOS), n-channel MOS (NMOS), complementary MOS (CMOS), and vertical MOS (VMOS). Performance qualities that distinguish products built in each of these technologies carry over to their applications in memory devices. Technologies that permit fast logic also permit fast memories, those that permit high density logic permit high density memories, and those that permit low power consuming logic permit low power consuming memories. Accordingly, there is a direct carryover of principal characteristics from medium scale and large scale integrated logic to memory products. Memories and logic fabricated by the same process are also easier to interface because of the similarity of electrical characteristics.

Speed-power product (SPP) tradeoffs exist for memories just as they do for logic families. The fastest

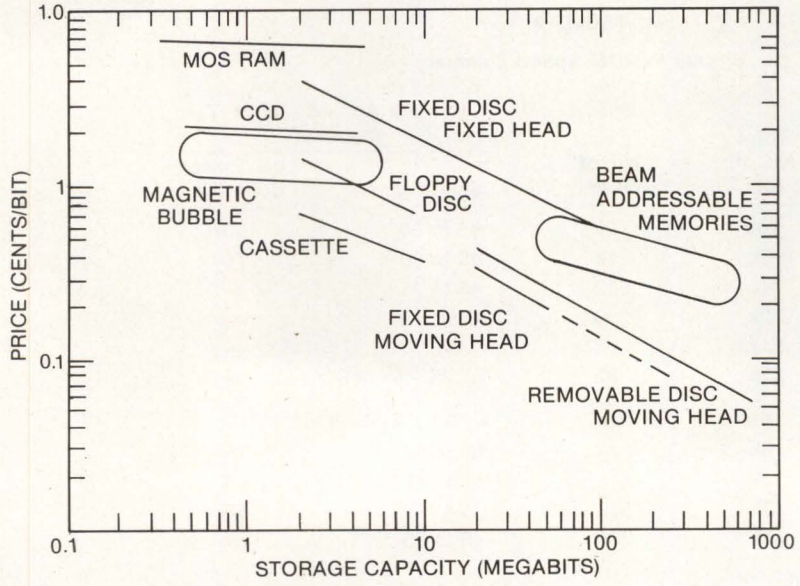


Fig 2 Memory storage capacity vs cost. MOS RAMs and magnetic bubbles have same basic storage capacity, but bubbles are almost a factor of 10 cheaper. Floppy, fixed, and removable disc memories have greater storage capacities at a lower cost per bit by several orders of magnitude

memories are bipolar ECL and Schottky TTL devices. Such devices have access times of about 5 to 100 ns; however, power consumption tends to be higher. MOS memories have access times that overlap those of bipolar devices (from about 35 ns to 5 μs), but power drain is generally lower and supply regulation is less critical. Presently, most semiconductor memories have shifted from PMOS to NMOS because of increased speed and packing density. CMOS devices have lower power consumption, but are more expensive.

Obviously, static and dynamic memory cells differ. Static memories are internally regenerative; they are designed to protect against false or ambiguous operation and come in two varieties: high speed and low power. Conversely, dynamic memories require refreshing at periodic intervals and are subject to high current transients, but they cost less, are simpler, and need less silicon area.

Important, but confusing, distinctions exist in the ROM class. These memories are set to yield the same output at all times unless they are altered to change the data placed within them. The term ROM generally refers to a memory programmed during a final mask step as part of the factory fabrication process. Factory programmed ROMs are likely to function as decoders, translators, or even as libraries of universal or standard data. Factory programming is most economical for medium to large quantities of memories with set patterns and a fixed circuit design. Programs subject to change or engineering alteration, however, may use some form of P/ROM. In these devices, permanent changes in the cell interconnects are produced either by electrically destroying or "burning out" fusible metal links or by deforming a transistor junction with an overvoltage.

Bipolar P/ROMs

The majority of bipolar or fusible link P/ROMs use Schottky TTL technology to achieve address access times (T_{AA}) of 30 to 90 ns (max), depending on memory size and organization, typically 32 to 2048 words in either 4- or 8-bit formats (Table 2). Power supply currents (I_{CC}) range from 65 to 180 mA (max).

P/ROMs with both open-collector and 3-state outputs are readily available. The 3-state output offers two major advantages over open-collector types. First, a low impedance driver is available for driving capacitance on the memory output, resulting in a faster low to high transition. Second, no pullup resistor is required.

Differences in bipolar P/ROMs occur in fusing technology and methods for programming P/ROMs. Fusible materials in widespread use are nichrome, polysilicon, and titanium-tungsten. Nichrome-fused P/ROMs have been proven reliable, but use high voltage programming techniques; polysilicon-fused P/ROMs utilize low voltage programming techniques. While titanium-tungsten fuses provide high speed P/ROMs with low programming voltages (high reliability), they do not have high usage history. The type of fuse that the system designer selects depends upon the method of programming and documented reliability. Bipolar P/ROMs from several manufacturers may be completely pin compatible, although totally different from a programming viewpoint.

TABLE 2

Bipolar P/ROM Speed Summary

Bipolar P/ROMS	Total No of Bits	No of Words	Address Access Times T_{AA} (ns max)	
			Schottky	Low Power Schottky
8 bits wide	16k	2k	65 to 90	120
	8k	1k	45 to 90	175
	4k	512	45 to 75	—
	2k	256	45 to 70	—
	512	64	40	—
	256	32	25	35
4 bits wide	16k	4k	70	—
	8k	2k	60 to 90	75
	4k	1k	50 to 80	65
	2k	512	45 to 70	55
	1k	256	45 to 65	55

Once programmed, bipolar P/ROMs cannot be changed. Thus, they provide nonvolatile, nonalterable storage and are useful for prototype systems. Many bipolar P/ROMs are completely interchangeable (electrically and pin compatible) with an equivalent ROM. In addition, there is upward compatibility of devices, ie, the ability to replace a 512 x 8-bit, 24-pin P/ROM with a 1k x 8-bit, 24-pin P/ROM using the same socket, without redesigning the printed circuit board. This upward compatibility exists for other devices as well.

High speed bipolar P/ROMs are incorporated in systems using high performance microprocessors, such as the Z80, where it is not feasible to use slow speed MOS memories that require the CPU to wait for memory. Some bipolar P/ROMs are designed to replace an MOS equivalent product; the Signetics 82S2708 is a direct, high speed, bipolar equivalent to the popular Intel 2708 MOS EPROM. Other bipolar P/ROMs are pin compatible with static MOS RAMs, such as the Monolithic Memories 6353, Intel 2114, and Texas Instruments TMS4045, for use as writable control stores in microprocessor based equipment. However, differences occur in speed of operation, as well as in power dissipation—especially since the 2114 and 4045 can be operated in a power-down (low power dissipation) mode, but the 6353 cannot. Interchangeability among these three memories provides the designer with flexibility to change from an essentially fixed program device (P/ROM) to a R/W memory device (static RAM).

State of the art in density for bipolar P/ROMs is 16,384 bits, organized as 2048 x 8-bit words. In the near future, 16,384-bit P/ROMs should become available in 4096 x 4-bit organizations; in the long term, 32k P/ROMs in 4096 x 8 and 8192 x 4 configurations and 64k P/ROMs in 8192 x 8 configurations (as developed by Toshiba), will be forthcoming. Two performance areas are being stressed: high speed (low address access time) and low power dissipation. Since these two characteristics cannot be obtained concurrently, several versions of the same organizations will exist—a speed enhanced version and a low power consumption version—all with open-collector and 3-state outputs. In addition, power switched and synchronous/asynchronous registered P/ROMs will soon be available in both Schottky and low power Schottky TTL technologies.

Development by Fujitsu of a new bipolar P/ROM fuse and isolation technology, in conjunction with Schottky TTL, will cut access times to half of those available with present devices. The faster access time results from several isolation techniques and a diffused eutectic aluminum process (DEAP) that replaces conventional fuse links and reduces cell size to half that of conventional P/ROMs. Two passive isolation techniques—shallow V-groove (SVG), which appears to be a bipolar version of VMOS, and isolation by oxide and polysilicon (IOP)—give closer cell spacing. These techniques allow the fabrication of a 1k x 4-bit P/ROM with a T_{AA} of 25 ns, P_{DISS} of 450 mW, and one-half of the required programming energy of present P/ROMs; permit an increase of P/ROM density to 32k bits; and cut die sizes in half for 4k and higher density P/ROMs. These new speeds should increase P/ROM usage in high speed applications. Fujitsu will begin sampling the MB7122 25-ns 1k x 4 P/ROM, the MB7128 2k x 4 P/ROM, and the MB7132 1k x 8 P/ROM using DEAP technology in the first quarter of 1980.

Although bipolar P/ROMs traditionally have been used for programming writable control stores, this situation will change in the near future. MOS ROMs and P/ROMs will become available and will impact this market. One such device, the Mostek 120-ns, 150-mW, 64k MOS ROM, planned to have a T_{AA} of 80 ns, should be available in 1980.

TABLE 3

Commercially Available Bipolar ROMs*

Organization	Manufacturer	Part Number	Outputs	T_{AA} (ns, max)	I_{CC} (mA, max)
1024 x 8	Monolithic Memories	6280/6281-1	OC/TS	100	180
	Monolithic Memories	6280/6281-2	OC/TS	55	180
	Monolithic Memories	6282/6283-1	OC/TS	100	180
	Advanced Micro Devices	AM27S80/S81	OC/TS	70 to 135	140/170
	National Semiconductor	DM85S29/S28	OC/TS	90	160
2048 x 8	Monolithic Memories	6275/6276-1	OC/TS	110	190
1024 x 9	Monolithic Memories	6260/6261-1	OC/TS	100	165
1024 x 10	Monolithic Memories	6255/6256-1	OC/TS	100	165

Notes:

*Notably absent are ROMs with a density of less than 8192 bits, as well as Fairchild 934XX and Signetics S25XX devices.
OC = Open Collector
TS = 3-State

Bipolar ROMs

Bipolar ROMs duplicate MOS ROMs in memory cell array, X-address decode or row select circuits, and Y-address or column select circuits. Output drivers provide the degree of output drive necessary for offchip load circuits. Since bipolar devices have much lower impedance than MOS, more drive capability is required throughout bipolar ROM circuits.

Bipolar ROMs are fabricated using Schottky TTL technology to obtain low access times and low power requirements. By eliminating programming circuits, smaller die size and higher reliability monolithic devices are obtained. These ROMs offer a low cost solution to program memory for high volume usage. A major deterrent to their use, however, is their inflexibility to change. This precludes their use in prototype or very low quantity production systems. As mentioned, bipolar ROMs that are interchangeable with bipolar P/ROMs are available.

Prior to 1978, bipolar ROMs were available with speeds of 25 to 100 ns and with densities of 256 to 16,384 bits. However, due to the customized nature of these devices, the general shortage of semiconductor memories (and of fabrication capacity), and the increased profit margins of other memory device types subsequent to this time frame, the only available bipolar ROMs are for densities of 8192 bits and greater from two suppliers (Table 3).

The near future for bipolar ROMs appears dim. After both Fairchild and Signetics announced similar type devices, they decided not to proceed with production. For the long-term future, bipolar ROMs, except for unique devices, should disappear from the marketplace. The void will be filled by MOS EPROMs and MOS ROMs, due to their high density and low cost. When speed

TABLE 4

Commercially Available MOS EPROMs (UV Type)

Mfr—Model No	Inter-changeable ROM	Size	Access Time (ns max)	Power Supply (V)	Maximum Current (mA)	
					Active	Standby
Intel 1702A	1302	2k	1000	5, −9	65 (885 mW)	65
Intel 2704	—	4k	450	12, ±5	65 (800 mW)	65
TI TMS2508	—	8k	250, 300, 350	5	446 mW	131 mW
Intel 2708	2308	8k	350, 450	12, ±5	65 (800 mW)	65
TI TMS27L08	—	8k	450	12, ±5	580 mW	—
Intel 2708L	2308	8k	450	12, ±5	425 mW	—
Intel 2758	—	8k	450	5	525/132 mW	—
Intel 2716	2316E	16k	350 to 450	5	100 (550 mW)	25 (138 mW)
TI TMS2716	—	16k	450	12, ±5	45 (720 mW)	—
Mostek MK2716T	MK31000	16k	350, 390	5	N/A	N/A
TI TMS2516	—	16k	350, 450	5	285 (525 mW)	50 < 131 mW
Hitachi	—	16k	250	5	330 mW	—
Intel 2732	2332/2364	32k	450	5	150 (788 mW)	30 (158 mW)
TI TMS2532*	TMS4732	32k	450	5	168 (840 mW)	10 (131 mW)
TI TMS25L32	TMS4732	32k	450	5	95 (500 mW)	131 mW
Motorola MCM2532/25A32	MCM68A332	32k	350, 450	5	N/A	—
Motorola MCM68764/68A764	MCM68A364	64k	350, 450	5	500 mW	100 mW
TI TMS2564	TMS4764	64k	450	5	840 mW	131 mW

Notes:
*Not compatible with 2716 or 2732
N/A = Not available
All UV EPROMs are encased in industry standard 24-pin DIPs except TMS2564, which fits in a 28-pin DIP.
TMS2532 is not pin compatible with Intel 2732.
MCM68764 will be encased in a 24-pin DIP, departing from industry accepted 28-pin DIP, TMS2564 64k EPROM.

is mandatory, bipolar P/ROMs should fulfill application requirements.

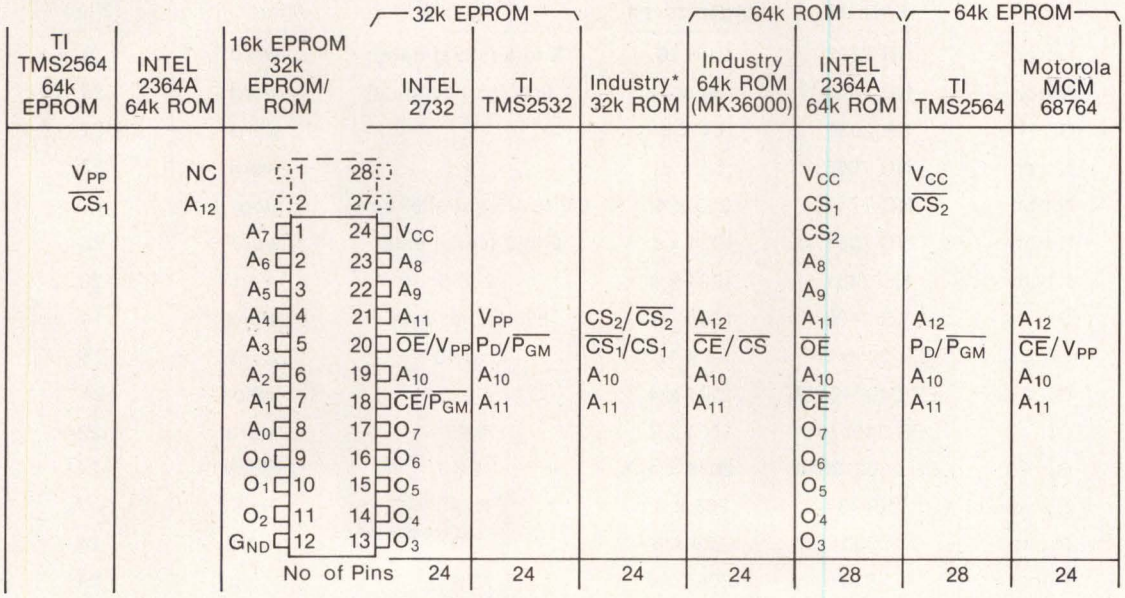
MOS Ultraviolet EPROMs

The MOS ultraviolet EPROM is both field programmable and reprogrammable. Commercially available EPROMs (Table 4) use floating gate avalanche injection MOS (FAMOS). Floating refers to the fact that the gate of each transistor is left unconnected, or electrically floating in an insulating layer of silicon dioxide. MOS EPROMs are typically five to ten times slower than bipolar types, they need multiple power supplies for operation (however, newer versions such as the Intel 2716 all use single 5-V supplies), and they are volatile to the extent that sunlight or fluorescent lighting can cause charge loss and thus erasure. These disadvantages are offset in many applications by their flexibility (field programming) and low cost. They can be programmed for a certain content, used, and then reprogrammed with a different content. Thus, they are ideal for prototype product development and applications that have constantly changing data requirements.

Reprogramming capability is gained by use of a trapped electronic charge technique for programming, instead of the destruction of a fusing element as in bipolar memories. Application of a high voltage across the transistor causes a "tunneling" of high energy carriers that open a conducting channel. However, several minutes' exposure of the chip to an intense, low frequency, ultraviolet light source causes a photo-current to flow that reverses the process by sweeping the charge from the floating gate and returns the gate to its floating state. The device may be reprogrammed and erased indefinitely. Erasure must be performed properly to ensure programmability and to avoid dropping bits with age and temperature. There are no reprogrammable bipolar EPROMs because the trapped charge technique cannot be implemented easily in bipolar technology.

The industry standard 2708 8k EPROM has been replaced by the 16k 2716, available from major semiconductor manufacturers. Recently introduced TI TMS2532 and Intel 2732 32k EPROMs are organized as 4k x 8 bits and operate from a single 5-V supply. However, a pinout problem exists with current 32k EPROMs. This problem, if not solved immediately, will be compounded with the advent of the 64k EPROM and cause confusion for designers. Basically, the manufacturers of 32k EPROMs have aligned themselves into two methodologies (similar to what happened in 1974 for 4k NMOS dynamic RAMs). This situation has been prompted by attempts at predicting future pinouts of 64k EPROMs and at adjusting pin compatibility with available 16k EPROMs, 32k and 64k MOS ROMs, and static RAMs.

Two distinct pinouts for the 32k EPROM involve the functions appearing on pins 18, 19, 20, and 21, as represented by the Intel 2732 and TI TMS2532 devices. The Intel 2732 is functionally and pin compatible with the 2716 16k EPROM and its own 32k ROM—a natural progression of parts. The Fujitsu MB8532 is also pin compatible with the 2732. The pinout of the TMS2532,



*Industry standard 32k ROM is supplied by TI, Electronic Arrays, Motorola, National Semiconductor, NEC, Signetics, and Synertek.

Fig 3 ROM and EPROM pinout variations. Differences occur on pins 18, 19, 20, and 21 among device categories. Ultimate resolution of industry standards will be accomplished by system designers

while not compatible with the 2716, has been chosen with a view toward the future—easy upgrading of 32k EPROM systems to 64k systems. The main functional difference between the Intel and TI devices is the output enable feature of the Intel device, which controls the output buffer to eliminate bus contention probblems in multiplexed microcomputer systems. The TMS2532 is compatible with ROMs manufactured by a variety of suppliers. Motorola's 64k EPROM (MCM68764) is also fully pin compatible with the TMS2532.

Two package types for 64k ROMs are 24 and 28 pins. The 28-pin package allows ROMs to better cope with the newer higher speed microprocessors and yields easy upgrading compatibility with the Intel 2732 EPROM. The 24-pin device is pin compatible with the industry standard 32k ROM and the TMS2532 32k EPROM, also allowing easy upgrading.

At the next level of integration, 64k EPROMs require a 28-pin package to handle the extra control pin. The exception is the Motorola MCM68764, which will be encased in a 24-pin DIP for easy upgrading from, and pin compatibility with, present generation products: the TMS2532 32k EPROM and the Mostek 36000 industry standard 64k ROM. The 28-pin approach, as exemplified by the TI TMS2564, allows simple upgrading from the TMS2532 EPROM and compatibility with future products, but it must be adapted for current products. Thus, the problem facing designers is whether to use a 64k EPROM that is immediately compatible with current products, or to use a device that will be upward compatible with future generations but requires separate board design for EPROM and current ROMs. In the meantime, some manufacturers, including Mostek, Intel, National Semiconductor, and Synertek, are developing their own 64k EPROM strategies, some with different pinouts.

Although EPROMs present a confusing and frustrating implementation for systems designers, they will ultimately decide the pinout to be accepted as the industry standard. This will hopefully lead to a single standard rather than a dual (32k EPROM), or even quadruple (64k EPROM) standard. Fig 3 depicts the packages for the two different 32k-bit EPROMs, in comparison with the industry standard 32k ROM pinout, the Intel 2464A and Mostek 36000 64k ROM pinouts, and the TI TMS2564 and Motorola MCM68764 64k EPROM pinouts.

Versatility, ease of use, and low power consumption should promote new and improved EPROMs. A 64k unit should appear within the next 12 to 18 months, as should

TABLE 5

Typical Available EAROMs (MNOS)

Mfr	EAROM	Organization	Max Access Time (μs)	Alterability	Pkg DIP (Pins)
Nitron	NC 7033	21 x 16	2 to 5 (serial data)	word	8
Nitron	NC 7040	64 x 4	2 to 5 (parallel data)	word	24
GI	ER 2055	64 x 8	2	word	22
Nitron	NC 7055	64 x 8	4	word	22
Nitron	NC 7714	256 x 4	0.9 to 1.5 (parallel data)	word	22
Nitron	NC 7051	1024 x 1	2 to 5 (serial data)	word	28
Nitron	NC 7451	1024 x 4	2 to 5	word	22
GI	ER 1400	100 x 14	833 (serial data)	word	14
GI	ER 2050/51	32 x 16	6 to 10	word	28
GI	ER 2401/2402	1024 x 4	2	chip	24
GI	ER 3400/01	1024 x 4	0.95	word	22
GI	ER 2805/2810	2048 x 4	2.6	block	24
Rockwell	10443	256 x 8	N/A	N/A	N/A
Nitron	7053	128 x 8	1.0	word	24
Nitron	7810	2048 x 4	1.4	chip	24

Notes:
GI = General Instruments
N/A = Not available

higher speed and lower power versions of 32k and 64k. Initial 64k EPROM samples should appear in early 1980. In addition, 128k- and 256k-bit versions are expected by 1985. Also, there is a lot of activity in CMOS P/ROMs (both fusible link and ultraviolet types) from Intersil and Harris because of the need for low power dissipation in battery applications and ease of use. Intersil offers a low power CMOS EPROM in two versions: 1k x 4 bits (6603) and 512 x 8 bits (6604). Harris has 512 x 8, 1024 x 8, and 2048 x 8 versions available.

MNOS EAROMs

Metal nitride oxide semiconductor (MNOS) EAROMs (Table 5) are useful in reduced power applications where data loss is intolerable, ie, for severe noise environments or recurring power interruptions. Such EAROMs permit complete or selective writing of bits into either state. This means that the memory can be programmed electrically while it is still in the circuit and that alterations may be made without wiping out remaining stored information.

Nitride EAROMs are slow (with read times of 0.95 to 5 μs) for most realtime program storage applications, are costly, and are not widely sourced. However, since they provide almost infinite store times, they are being used increasingly as auxiliary memory in applications where remote systems are inaccessible for routine field changes and in aerospace (satellite) systems. There is less design work occurring with EAROMs than with EPROMs and P/ROMs. A major reason for this situation is the limited usage for slow devices coupled with the difficulty of developing a viable, producible silicon nitride process. However, an increased wave of interest has centered on the EAROM because of its nonvolatility advantage.

Floating Gate EEROMs

Floating gate electrically erasable programmable ROMs (EEROMs) are similar to ultraviolet EPROMs, where charge is stored on a floating gate. There is no quartz lid to allow erasing; however, an electrical gate controls erasing and writing. Devices of this type presently use special voltages and complex voltage sequencing, making them impractical for in-circuit programming.

Floating gate EEROMs have access times and data retention similar to ultraviolet EPROMs; they are usually removed from the circuit for erasing and reprogramming. Erase time, however, is much shorter than for ultra-

TABLE 6

EEROM Availability Summary

Manufacturer	Part No	Organization	Voltage (V)	T_{AA} (max, ns)	Pkg DIP (Pins)
SGS-ATES	M120	256 x 4	5	450	18
Hitachi	48016*	2048 x 8	5	250	24
RCA	1842	256 x 8	5	250	N/A
RCA	1843	1024 x 8	5	N/A	N/A
NEC	upD454**	256 x 8	12, 5	800	24
Xicor	X2201/2202†	1024 x 1	5	250	18
NEC	upD458	1024 x 8	12, 5	450	28

Notes:
*2716 UV Replacement
**Pin compatible with 1702A EPROM
†Nonvolatile RAM contains both 1024 x 1 static RAM and 1024 x 1 EEROM that shadows RAM bit by bit.
N/A = Not available

TABLE 7

Summary of Selected CMOS ROMs

Memory Size / Mfr	RCA	Motorola	Harris	Intersil	Hughes	Solid State Scientific	Super Tex
256 x 4		MCM14524	HM6611 (P/ROM) HM6661 (P/ROM)				
256 x 8	CDP1842(P/ROM)						
512 x 8	CD40032 CDP1831 CDP1832		HM6641 (P/ROM)	IM6654(EP)	HCMP 1831 HCMP 1832	SCP 1831 SCP 1832	
1024 x 4				IM6653(EP)			
1024 x 8	CDP1833/34 CDP1843*(P/ROM)		HM6708 (EP)		HCMP 1833/34	SCP 1833 SCP 1834	
1024 x 12			HM6312/A	IM6312/A		SCM 5316	
2048 x 8			HM6716 (EP)	IM6316	HCMP 1835/1836		
8192 x 8			HM6388 HM6389	1M6364			
4096 x 8							CM3200

*Pin compatible with Intel 2758

TABLE 8

Summary of Selected CMOS EPROMs (ROMs)

Part Number	Mfr	Organization	EPROM	ROM	T_{AA} (ns max)	I_{CC} (μA max)	Power Supply (V max)	DIP Pkg (Pins)
HM6611	Harris	256 x 4	X (F/L)		250	15/200	12.0	18
HM6661	Harris	256 x 4	X (F/L)		250	15/200	12.0	18
HM6641	Harris	512 x 8	X (F/L)		300	100	5.0	24
IM6654	Intersil	512 x 8	X		300, 450, 600	100	5.0	24
IM6653	Intersil	1024 x 4	X		300, 450, 600	100	5.0	24
HM6708[A]	Harris	1024 x 8	X			350	5.0	24
HM6312/A	Harris	1024 x 12		X	220 (10 V) 350 (5 V)	10mA/800	12.0	18
IM6312	Intersil	1024 x 12		X	400	100	5.0	18
IM6312A	Intersil	1024 x 12		X	200	500	12.0	18
HM6716[B]	Harris	2048 x 8	X		350	100	5.0	24
IM6316	Intersil	2048 x 8	X		350 (typ)	100	5.0	24
SCM5316	SSS	2048 x 8		X	450	7mA/100/10	5.0	24
CM3200	Super Tex	4096 x 8		X	450	20 mA/20	5.0	24
HM6388	Harris	8192 x 8		X	550	100	5.0	24
HM6389	Harris	8192 x 8		X	550	100	5.0	28

Notes:
Listed limits are guaranteed at 25 °C.
F/L = Fusible Link
All have TTL compatible I/O and 3-state outputs.
[A]Pin compatible with 2708 NMOS EPROM
[B]Pin compatible with 2716 NMOS EPROM

violet EPROMs, typically one minute or less. Floating gate EEROMs are just becoming commercially available and do not cover a wide range of devices.

A recent method of achieving nonvolatile storage is Xicor's 1k static RAM. Using standard NMOS processing techniques, the X2201/X2202 contains a 1024 x 1 static RAM with an identical triple silicon floating gate EEROM array that shadows the RAM on a bit by bit basis. The floating gate is part of an n-channel transistor where ability to turn on and off is the basis for the operation of this memory; when the memory is being programmed, the floating gate is charged with electrons turning the transistor off, and during erase, electrons are removed from the gate turning the transistor on. The floating element always stores nonvolatile data, regardless of static RAM contents, which are valid with or without power. Nonvolatile memory data remain separate from the contents of the RAM and depend only on the condition of the programmed floating gate electrode.

Each array location actually consists of a normal static RAM bit and an overlaid electrically erasable nonvolatile bit for a total of 2048 bits. This memory consists of a normal static RAM bit and an overlaid electrically erasable nonvolatile bit for a total of 2048 bits, plus a complete duplicate backup RAM.

Data move between the RAM and EEROM by means of two TTL control signals: store and recall. With a store signal applied, a 1024-bit snapshot of the RAM is copied into the EEROM for later recall or modification. Anytime that the recall signal is applied, EEROM data are copied back into the RAM.

Automatic array recall occurs when power is applied. This memory powers up with a copy of the nonvolatile EEROM data and is ready for immediate use. The Xicor part is encased in an 18-pin DIP. The X2201 has total memory array recall, while the X2202 has single-bit recall. Data contained in this device can be electrically altered (by writing, reading, or erasing) without removing them from the circuit. Table 6 summarizes the few commercially available EEROMs.

Increased emphasis on floating gate EEROMs, as well as EAROMs, should occur. The beginning of 1980 should see the sampling of the 16k HM48016 EEROM from Hitachi. This product represents the first of many EEROMs from most major MOS EPROM manufacturers.

MOS ROMs

High density MOS ROMs of 32k and 64k bits have emerged as critical members of the microprocessor chip set, expanding the instruction capacity of microprocessor based systems and holding immediate promise for fixed programs in larger hierarchies. These memories have proven popular and are widely sourced. In addition, high density ROMs are generally viewed as the most cost-effective of all semiconductor memories and may well impact tape and disc storage.

Microprocessors—perhaps the high performance 8-bit and also 16-bit versions—will use ROM extensively for software storage. By 1980, 80-ns 64k ROMs as well as 128k and 256k MOS ROMs are expected. Also becoming more readily available are low power CMOS ROMs and EPROMs for battery powered and energy critical applications (Tables 7 and 8).

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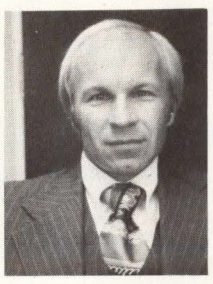

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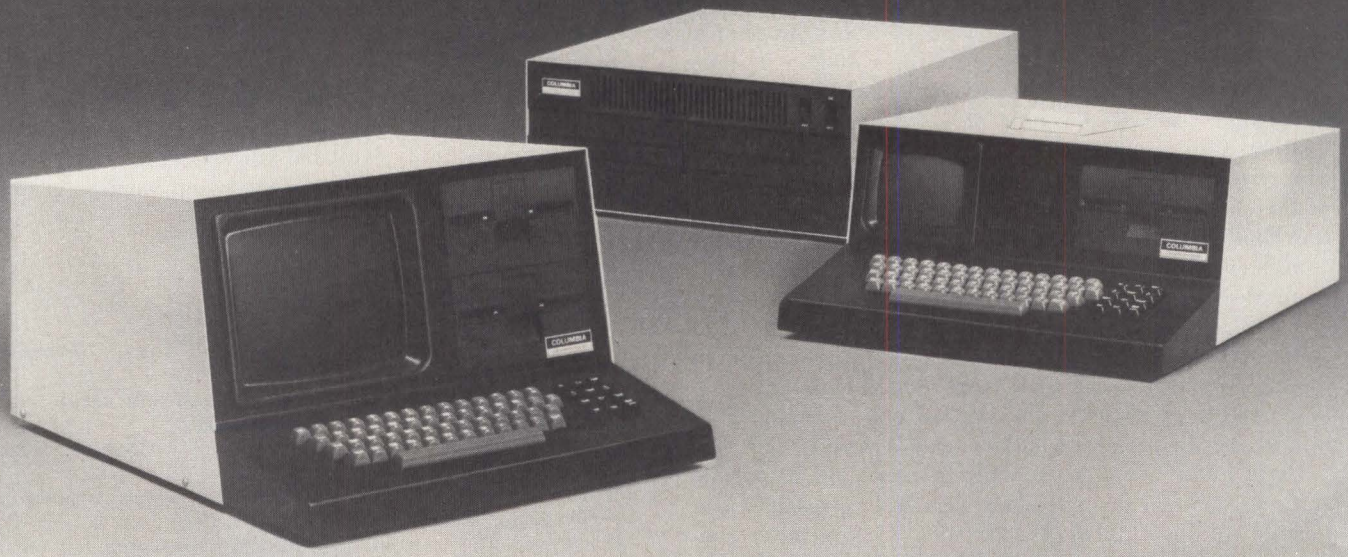

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ASSEMBLER STREAMLINES MICROPROGRAMMING

Microprogram assemblers are structured to manipulate programmer-generated symbology directly into binary format, independent of hardware configuration, technology, or applications

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With the advent of bit-slice logic devices, such as the transistor-transistor logic 2900 and emitter-coupled logic M10800 families, cost-effective high speed microprogrammable processors are becoming easier to construct. These devices condense system hardware into bipolar large scale integrated building blocks, making it feasible to achieve the highly flexible architecture, variable data widths, emulation of existing instruction sets, and random logic reduction that microprogramming provides.

However, the software design effort required to microprogram the processor remains a time consuming and therefore costly task. Consequently, microprogram assemblers, such as the Motorola MACE-Assembler or the Advanced Micro Devices AMDASM/29 assembler, have evolved to streamline microprogram writing, checking, and debugging.

Microprogrammed processor development requires interrelated parallel hardware and software design efforts (Fig 1). Overall system specifications are first resolved into a hardware design that defines processor word size, input/output (I/O), bus structure, microprogram word size, and a microfunction set. Further defining the microprogram word, this microfunction set is a central reference point used by the microprogrammer to write microcode and by the design engineer to develop hardware. Parallel development paths merge when the system prototype executes microprogram routines during system checkout. In the figure, note the feedback paths for both hardware and software design efforts. System checkout normally requires several passes, each with microprogram changes or corrections and/or hardware modifications.

Microprogram assemblers operate in two successive phases. After completion of the microfunction set, the assembler definition phase sets up microprogram word structure and mnemonic assignments within the assembler. The following assembly phase takes microprogram source statements expressed in terms established by the definition program and translates them into processor compatible bit patterns, similar to a microprocessor or minicomputer assembler. Many different microprograms can be developed for a given system after the definition stage is finished. Similarly, changes to a processor

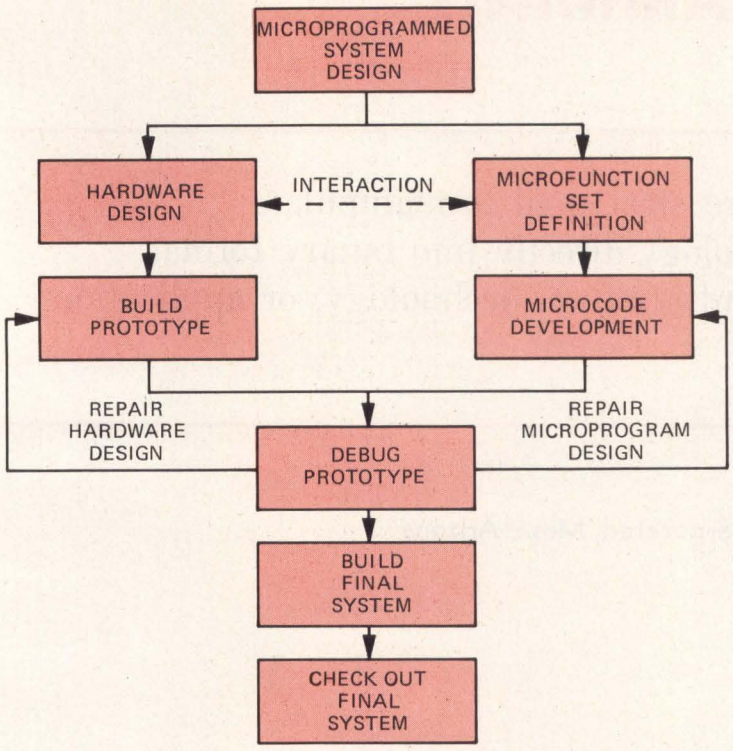

Fig 1 Parallel hardware and software design. Successful microprogrammed system design requires combination of hardware and software development. Error in either parallel path compromises final system design. Bipolar bit-slice circuits reduce hardware design effort by incorporating major processor sections into standard LSI components. Available microprogram assemblers simplify microprogram development with address labels and easily interpreted mnemonic codes. Coordination of microprogram assembler and development hardware facilitates system debug and checkout

microfunction set or different processor designs use the same microprogram assembler by modifying or replacing the definition program.

Efficient design results when a microprogram development system and associated microprogram assembler are used early in the processor development cycle, for example, at the Debug Prototype block in Fig 1. Both definition and assembly phase programs are entered through a keyboard terminal and are stored on floppy disc (Fig 2). Assembled microprograms are also stored on the disc. High speed random access memories (RAMs) substitute for the prototype system microprogram memory, with a complete interface for microprogram address, data, and control. Microprograms stored on disc are placed in RAM, and then are used to verify both microprogram and prototype hardware operation. Processors designed using programmable read only memories (P/ROMs) for microprogram storage benefit from use of the microprogram development system because microprogram changes, corrections, or additions are easily performed through the keyboard with software editing and assembly rather than programming P/ROMs with new binary bit patterns.

Microprogram Development System

A microprogram development system has three primary functions.

(1) Provide writable control storage (WCS) for microprogram memory.

(2) Provide software for microcode development.

(3) Provide system diagnostic help.

For example, the M6800 based EXORcisor system provides the host or executive processor, metal oxide semiconductor (MOS) memory, floppy disc, printer, and terminal, along with interface hardware and operating software. Originally developed for MOS microprocessor design support, the EXORcisor concept is extended to bipolar bit-slice microprogrammable processors through the MACE 29/800 Microprogram Development System (Fig 2). The MACE chassis houses high speed bipolar RAM, address and data interfaces, clock source, and diagnostic hardware necessary for bit-slice processor development.

The MACE-Assembler is a general purpose 2-phase assembler specifically designed for microprogrammable

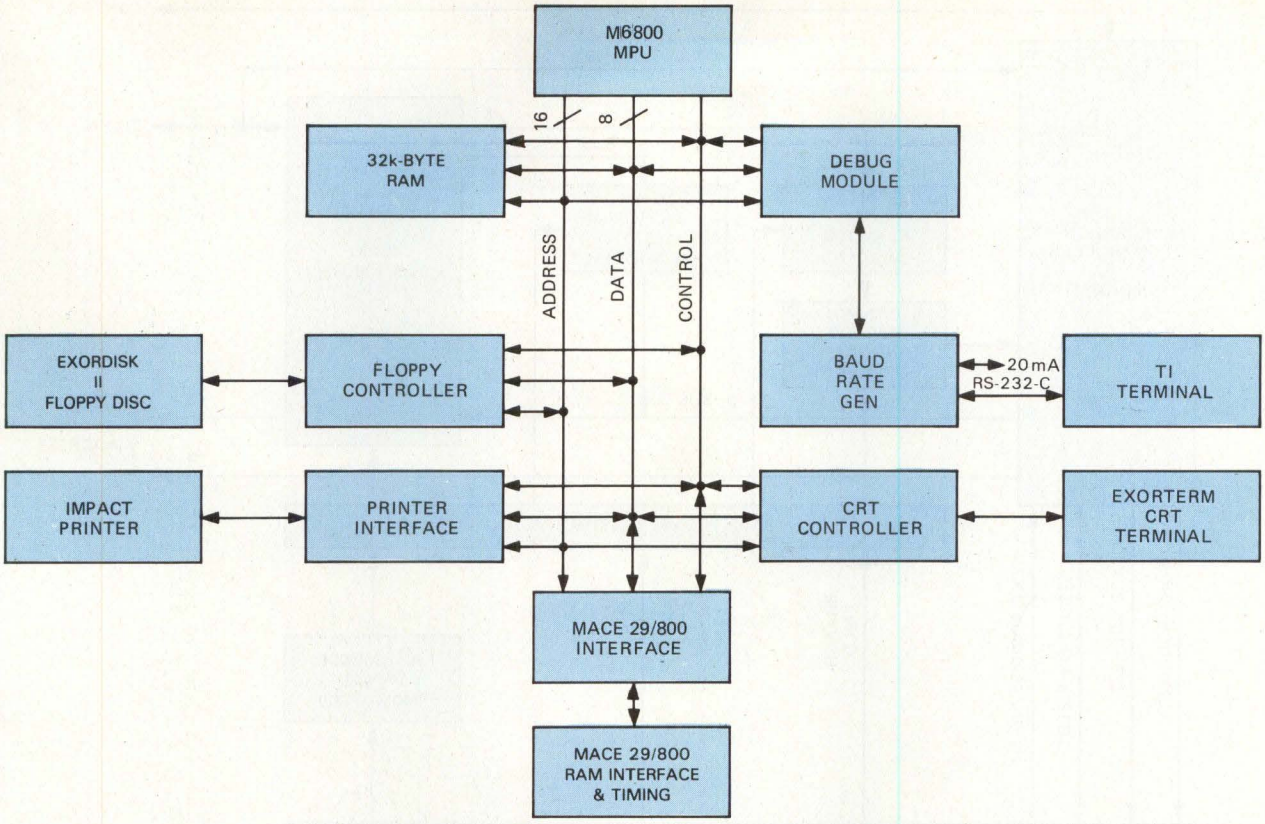

FIGURE 2 – EXORciser BUS NETWORK

Fig 2 Microprogram development system. CRT terminal houses 6800 host processor, 32k bytes of MOS RAM, plus interfaces to floppy disc, printer, and MACE hardware. Microprogrammer inputs are entered through terminal, which uses M6800 microprocessor to run microprogram assembler. Hardcopy of microprogram source statement inputs and assembled program outputs are furnished through line printer. Both microprograms and operating system software are stored on dual floppy disc. Development system supports both bipolar bit-slice and M6800 MOS microprocessor families

processor development. Definition statements permit microword size and format to be established and thus applied to a particular hardware configuration. During the definition phase, the designer in effect creates a unique microassembler for a system. Microprogram word length, field sizes, operator values, mnemonic assignments, and data entry formats are all defined by the definition source file. The definition phase reads a definition source file on disc and creates a definition table, also on disc. Next, the assembly phase uses the definition table to convert microprogram source statement files to binary microwords for the writable microprogram memory. Definition and assembly source files are built on the floppy disc with a standard MDOS editor. Format definition files, source listings, and object files are also created by the MACE-Assembler.

Interface to the prototype system is through address and data probe circuits which handle both emitter-coupled logic (ECL) 10,000 and transistor-transistor logic (TTL) compatible signals. Interface to the floppy disc and keyboard is through the EXORcisor network. MACE hardware operates in two basic modes as controlled by system commands. Management mode places the MACE system under control of the EXORcisor M6800 host processor. This mode is used for operator control of microprogram memory read and write, plus diagnostic clock functions. Prototype mode turns memory control over to the processor under development. In this mode, the development system becomes transparent and does not alter microprogrammable processor structure or basic operation.

Typical Microprogrammable System

Microprogram assembler source statement programs are written around a given processor design and microfunction set. Fig 3 shows a small, general purpose 8-bit microprogrammed processor built with ECL large scale integrated (LSI) circuits. Main capabilities include

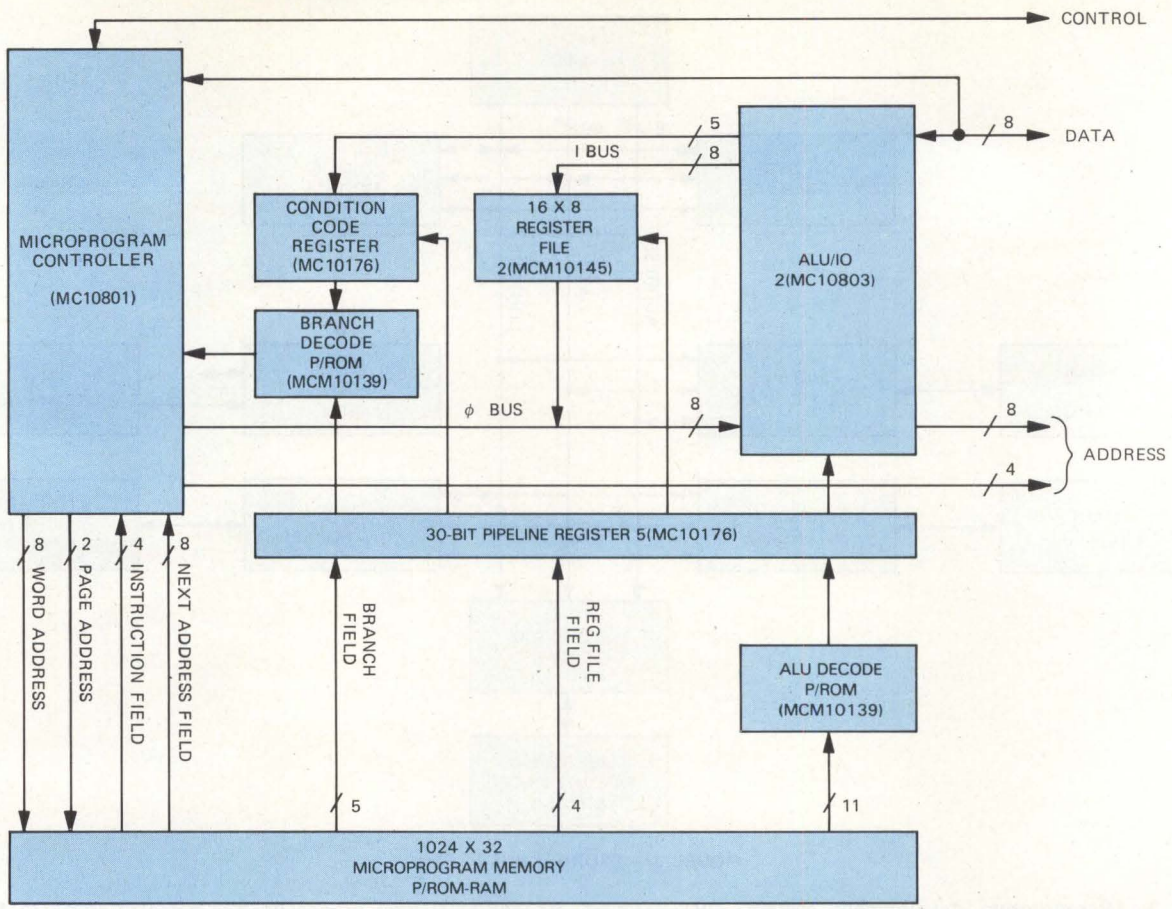

Fig 3 Microprogrammable processor. Three main sections of processor are microprogram controller, microprogram memory, and ALU-I/O. ALU performs all arithmetic and logic operations on data. I/O transfers data to and from processor, while register file holds data. All three sections are controlled by bit patterns in microprogram memory. ALU-I/O instruction sequence is determined by microprogram controller, which supplies address to microprogram memory, and uses feedback from microprogram to generate address combinations required to execute program. Condition code register and branch logic supply ALU status results to help make microprogram flow decisions. Pipeline register improves processor performance by allowing faster basic clock rates, and ALU and branch decode logic lower system cost by reducing microword data bit width

a 100-ns microinstruction cycle time and a flexible microprogram function set. Limitations are the 8-bit arithmetic logic unit (ALU) word size and a general purpose I/O interface not optimized for a specific application.

Two ALU-I/O circuits control all data and address I/O interfacing, and work with a 16-location register file to perform arithmetic and logic operations on data within the processor. Each ALU-I/O is four bits wide, and several of these parallel circuits can be cascaded to meet increased system I/O word sizes. Microprogram controller circuits address microprogram memory and control the instruction sequence that executes a microprogram routine. Also 4-bit wide parts, parallel controller circuits can also be cascaded to meet increased microprogram memory address size requirements. Once addressed, microprogram memory outputs go to the various processor sections during a single microinstruction. The pipeline register minimizes microinstruction cycle times by temporarily holding microprogram memory outputs, allowing microinstruction execution and fetch cycles to be overlapped. Small 32-word x 8-bit P/ROMs located in branch and ALU-decode blocks reduce the microprogram word width by expanding small microprogram fields into a larger number of ALU and branch-decode logic select lines.

I FIELD (4 BITS)	NEXT ADDRESS FIELD (8 BITS)	BRANCH FIELD (5 BITS)	RF FIELD (4 BITS)	ACC FIELD (2 BITS)	ALU FIELD (5 BITS)	DESTINATION FIELD (4 BITS)

INSTRUCTION FIELD		
HEX	MNEM	DESCRIPTION
0	JSR	JUMP TO SUBROUTINE
1	JL2	JUMP AND LOAD CR2
2	JMP	JUMP TO NA
3	JLA	JUMP & LOAD ADDRESS
4	BSR	BRANCH TO SUBROUTINE
5	BRC	BRANCH ON CONDITION
6	BRM	BRANCH AND MODIFY
7	ROC	RETURN ON CONDITION
8	JIB	JUMP TO I BUS
9	JIN	JUMP TO I BUS & LOAD CR2
A	JPI	JUMP TO CR2
B	RPI	REPEAT INSTRUCTION
C	INC	INCREMENT
D	RSR	REPEAT SUBROUTINE
E	JEP	JUMP TO ϕBUS
F	RTN	RETURN FROM SUBROUTINE

BRANCH FIELD					
HEX	MNEM	DESCRIPTION	HEX	MNEM	DESCRIPTION
00	BR1	BRANCH = 1	10	LDR2	LOAD DIN → CR32
01	TLSB	TEST LSB	11	LDR3	LOAD DIN → CR33
02	TSMS	TEST SIGN MSB	12	STR2	SET CR32
03	TZD	TEST ZERO DETECT	13	STR3	SET CR33
04	TOVF	TEST OVERFLOW	14	CLR2	CLEAR CR32
05	TCL	TEST CARRY LINK	15	CLR3	CLEAR CR33
06	TSZD	TEST SIGN & ZERO DETECT	16	TR2	TEST CR32
07	TLLI	TEST LSB AND LINK	17	TR3	TEST CR33
08	STP0	SET MPO	18	CLUP	CLEAR UPR
09	STP1	SET MP1	19	STUP1	SET UPR = 01
0A	STP2	SET MP2	1A	STUP2	SET UPR = 10
0B	STP3	SET MP3	1B	STUP3	SET UPR = 11
0C	CLMP	CLEAR MP	1C	ENCR1	ENABLE CR1 →ØB
0D	LNMP	LOAD NA → MP	1D	ENCR2	ENABLE CR2 →ØB
0E	LDMP	LOAD DB → MP	1E		
0F	CAR1	CARRY = 1	1F		

RF FIELD	
HEX	REGISTER
0	RF0
1	RF1
2	RF2
3	RF3
4	RF4
5	RF5
6	RF6
7	RF7
8	RF8
9	RF9
A	RFA
B	RFB
C	RFC
D	RFD
E	RFE
F	RFF

ACC FIELD	
HEX	ACCUMULATOR
0	ACC0
1	ACC1
2	ACC2
3	ACC3

ALU FIELD					
HEX	MNEM	DESCRIPTION	HEX	MNEM	DESCRIPTION
00	ADAR	ADD ACC + RF	10	IVRF	INV RF
01	ADAD	ADD ACC + DR	11	TRF	TRA RF
02	ADARC	ADD ACC + RF + C	12	TDR	TRA DR
03	ADADC	ADD ACC + DR + C	13	TAR	TRA AR
04	SUAR	SUB ACC – RF	14	INAR	INC AR + 1
05	SUAD	SUB ACC – DR	15	ADRD	ADD RF + DR
06	SUARC	SUB ACC – RF + C	16	ASRR	ASR RF
07	SUADC	SUB ACC – DR + C	17	ASRA	ASR ACC
08	ANAR	AND ACC 0 RF	18	LSRR	LSR RF
09	ANAD	AND ACC 0 DR	19	LSRA	LSR ACC
0A	ORAR	OR ACC U RF	1A	RORR	RSR RF
0B	ORAD	OR ACC U DR	1B	RORA	RSR ACC
0C	EXAR	EXOR ACC θ RF	1C	LSLR	LSL RF
0D	EXAD	EXOR ACC θ DR	1D	LSLA	LSL ACC
0E	INRF	INC RF + 1	1E	RSLR	RSL RF
0F	DERF	DEC RF – 1	1F	RSLA	RSL ACC

DESTINATION FIELD				
		DESCRIPTION		
HEX	MNEM	INTERNAL	EXTERNAL	CC
0	AACC	ALU → ACC	–	1
1	AAC	ALU → ACC	–	0
2	ARFC	ALU → RF	–	1
3	ARF	ALU → RF	–	0
4	ADRC	ALU → DR	–	1
5	AACDC	ALU → ACC	DB → DR	1
6	DBAR	–	DB → AR	0
7	DBAC	–	DB → ACC	0
8	AAR	ALU → AR	–	0
9	AARRF	ALU → AR,RF	–	0
A	AARDC	ALU → AR	DB → DR	1
B	AARD	ALU → AR	DB → DR	0
C	AARDR	ALU → AR	DB → RF	0
D	AARAD	ALU → AR	ACC → DB	0
E	AARRD	ALU → AR	RF → DB	0
F	AARDD	ALU → AR	DR → DB	0

Fig 4 Microprogram memory fields. Typical 32-bit microprogram word is divided into seven fields, each controlling different processor section. Microprogrammer assigns microfunction set mnemonic codes to various microprogram field positions. For example, microinstruction BRC 05 TZD RF,5 ACC,1 ADAR ARF makes microprogram branch decision, either jumping to address 05 or incrementing, depending on zero detect status. At same time, register file word 5 is added to accumulator word 1, with results placed back in register file. Microprogram assembler would take combination of mnemonics, compare with microfunction set definition table, and generate hexadecimal bit pattern 5051AA03, which could then be put in microprogram memory. Microprogrammer can select combination of field commands that performs required microprogram instruction or combination of microinstructions to perform system level instruction

```
0010  TITLE SYSTEM 800 MICROPROGRAM FIELD DEFINITION
0020  SIZE 32
0030  OPT L=#CN
0040 ;
0050 ; MICROPROGRAM INSTRUCTION FIELD
0060 ;
0070 JSR     FORM  4H0,28X          ; JUMP TO SUBROUTINE
0080 JL2     FORM  4H1,28X          ; JUMP AND LOAD CR2
0090 JMP     FORM  4H2,28X          ; JUMP TO NEXT ADDRESS
0100 JLA     FORM  4H3,28X          ; JUMP AND LOAD ADDRESS
0110 BSR     FORM  4H4,28X          ; BRANCH TO SUBROUTINE
0120 BRC     FORM  4H5,28X          ; BRANCH ON CONDITION
0130 BRM     FORM  4H6,28X          ; BRANCH AND MODIFY
0140 RDC     FORM  4H7,28X          ; RETURN ON CONDITION
0150 JIB     FORM  4H8,28X          ; JUMP TO I BUS
0160 JIN     FORM  4H9,28X          ; JUMP TO I BUS AND LOAD CR2
0170 JPI     FORM  4HA,28X          ; JUMP TO CR2
0180 RPI     FORM  4HB,28X          ; REPEAT INSTRUCTION
0190 INC     FORM  4HC,28X          ; INCREMENT
0200 RSR     FORM  4HD,28X          ; REPEAT SUBROUTINE
0210 JEP     FORM  4HE,28X          ; JUMP TO D BUS
0220 RTN     FORM  4HF,28X          ; RETURN FROM SUBROUTINE
0230 ;
0240 ; NEXT ADDRESS FIELD
0250 ;
0260 NA      FORM  4X,8VHTFF,20X    ; ADDRESS VECTOR
0270 NC      FORM  4X,8VH,20X       ; NUMERICAL CONSTANT
0280 CC      FORM  4X,8VHNT,20X     ; CYCLE COUNT
0290 ;
0300 ; BRANCH FIELD
0310 ;
0320 BR1     FORM  12X,5H00,15X     ; BRANCH = 1
0330 TLSB    FORM  12X,5H01,15X     ; TEST LSB
0340 TSMS    FORM  12X,5H02,15X     ; TEST SIGN/MSB
0350 TZD     FORM  12X,5H03,15X     ; TEST ZERO DETECT
0360 TOVF    FORM  12X,5H04,15X     ; TEST OVERFLOW
0370 TCL     FORM  12X,5H05,15X     ; TEST CARRY LINK
0380 TSZD    FORM  12X,5H06,15X     ; TEST SIGN & ZERO DETECT
0390 TLL     FORM  12X,5H07,15X     ; TEST LSB & LINK
                                    .
                                    .
                                    .
0600 ENCR1   FORM  12X,5H1C,15X     ; ENABLE CR1 ONTO D BUS
0610 ENCR2   FORM  12X,5H1D,15X     ; ENABLE CR2 ONTO D BUS
0620 ;
0630 ; REGISTER FILE ADDRESS FIELD
0640 ;
0650 RF      FORM  17X,4VH0,11X     ; REGISTER FILE ADDRESS
0660 ;
0670 ; ACCUMULATOR ADDRESS FIELD
0680 ;
0690 ACC     FORM  21X,2V00,9X      ; ACCUMULATOR ADDRESS
0700 ;
0710 ; ALU FUNCTION FIELD
0720 ;
0730 ADAR    FORM  23X,5H00,4X      ; ADD ACC + RF
0740 ADAD    FORM  23X,5H01,4X      ; ADD ACC + DR
0750 ADARC   FORM  23X,5H02,4X      ; ADD ACC + RF + C
0760 ADADC   FORM  23X,5H03,4X      ; ADD ACC + DR + C
0770 SUAR    FORM  23X,5H04,4X      ; SUB ACC - RF
0780 SUAD    FORM  23X,5H05,4X      ; SUB ACC - DR
                                    .
                                    .
                                    .
1030 ROLR    FORM  23X,5H1E,4X      ; ROTATE LEFT RF
1040 ROLA    FORM  23X,5H1F,4X      ; ROTATE LEFT ACC
1050 ;
1060 ; DESTINATION FIELD
1070 ;
1080 AACC    FORM  28X,4H0          ; ALU TO ACC, LOAD CC
1090 AAC     FORM  28X,4H1          ; ALU TO ACC, NO CC
1100 ARFC    FORM  28X,4H2          ; ALU TO RF, LOAD CC
1110 ARF     FORM  28X,4H3          ; ALU TO RF, NO CC
1120 ADRC    FORM  28X,4H4          ; ALU TO DR, LOAD CC
1130 AACDC   FORM  28X,4H5          ; ALU TO ACC, DB TO DR, LOAD CC
1140 DBAR    FORM  28X,4H6          ; DB TO AR, NO CC
1150 DBAC    FORM  28X,4H7          ; DB TO ACC, NO CC
1160 AAR     FORM  28X,4H8          ; ALU TO AR, NO CC
1170 AARRF   FORM  28X,4H9          ; ALU TO AR & RF, NO CC
1180 AARDC   FORM  28X,4HA          ; ALU TO AR, DB TO DR, LOAD CC
1190 AARD    FORM  28X,4HB          ; ALU TO AR, DB TO DR, NO CC
1200 AARDR   FORM  28X,4HC          ; ALU TO AR, DB TO RF, NO CC
1210 AARAD   FORM  28X,4HD          ; ALU TO AR, ACC TO DB, NO CC
1220 AARRD   FORM  28X,4HE          ; ALU TO AR, RF TO DB, NO CC
1230 AARDD   FORM  28X,4HF          ; ALU TO AR, DR TO DB, NO CC
1240 ;
1250 ; OTHER COMMANDS
1260 ;
1270 NOP     FORM  12X,4H0,16H0138; NO OPERATION
1280  END
```

Fig 5 Microprogram example. Microprogram assembler starts with field definition file and creates lookup table which defines microprogram source statement terms to assembler. This, in effect, configures assembler tailored to microprogrammed processor under development. Each mnemonic term is sequentially listed and defined. Definition consists of selecting associated binary bit pattern codes and placing coded bits within total microprogram word. Flexibility to completely define mnemonics and field position allows for variable field microprogram word structures, where one field establishes field structure for remainder of word. Only restriction is that each mnemonic term must be unique and appear only once in definition file. It is also possible to have mnemonic terms cover any or all microprogram bits independent of normal field structure. For example, NOP mnemonic (line 1270) identifies bit pattern for 12 "don't care" bits (these are I field and NA field), followed by a 20-bit instruction that performs "no operation" processor function

Microprogram word structure and field assignments (Fig 4) provide insight into processor operation. The relatively small 32-bit word length possible with ALU and branch-decode logic is wide enough to control major system sections in parallel, yet minimize memory size and cost. Seven independent fields within the 32-bit word of microprogram memory form the processor microfunction set that becomes the basis for all microprogramming.

The 4-bit instruction (I) field goes directly to the microprogram controller and is used for microprogram address flow. Instruction commands and mnemonics are an integral part of the microprogram controller, which decodes and executes each program flow instruction. An 8-bit next address (NA) field assists program flow by providing jump and subroutine destinations. Equally important, NA field can be routed to the ALU-I/O logic for ALU constants, bit-pattern masking, and address vectors. NA is a variable field, which means that the bit pattern is assigned when writing a microprogram, rather than being part of a fixed microfunction table.

The 5-bit branch (BR) field covers several independent system functions. The first eight branch instructions (00 to 07) control microprogram flow by routing different test parameters to the microprogram controller. Instructions 08 to 0E control a 4-bit output page address, giving the 8-bit processor a total of 12 address lines (Fig 3). Branch instruction 0F sets carry to 1 for subtraction and multiprecision arithmetic. Branch instructions 10 to 17 handle I/O interrupts and processor status lines. Instructions 18 to 1B control microprogram page address bits which expand microprogram memory size from 256 to 1024 words. The last two BR instructions route NA information to the ALU and I/O logic. In this processor design, instruction field commands are fixed as defined by the microprogram controller, while the branch field is adaptable to system application needs and is easily modified by changing the branch decode P/ROM.

A 4-bit register file (RF) field addresses 1 of 16 register file words. The register file is augmented by a 2-bit accumulator (ACC) field which addresses one of four accumulators located within the ALU-I/O logic. Selected register file and accumulator words are normally used as ALU operands.

Thirty-two different ALU functions selected by the 5-bit ALU field perform all logic, arithmetic, and shift operations on data in the processor. The general-purpose ALU function set can be easily changed to fit specific system needs by reprogramming ALU decode logic. A 4-bit destination field completes the 32-bit microprogram word. This field is responsible for routing ALU results to register file, accumulator, and to a data buffer register or an address register located in the ALU-I/O logic. The destination field also controls all I/O operations through processor data and address ports.

The 32-bit microprogram word is unique to this particular processor design and application. The MACE microprogram assembler works with this microfunction set, as well as with the wide range of other microprogram word lengths and field combinations characteristic of bit-slice processors.

Assembler Definition Phase

To use the MACE-Assembler to assemble a microprogram for a particular processor, a definition source file, which defines total microword size, individual field sizes, mnemonics, and operator values, must first be created using the host system editor. Fig 5 lists the definition source file for the microprogram system example given in Fig 3. In Fig 5, the first three program lines are a title line, which identifies the file as a microprogram field definition for a particular processor design, a word size line to define the processor's 32-bit microprogram word, and a third line which specifies an optional output device—a terminal printer in this case. The remaining program steps define each mnemonic term using the format

LINE # MNEMONIC FORM VALUE & POSITION

Comments following a semicolon are for programmer convenience and are ignored by the assembler.

In Fig 5, program lines 0070 through 0220 define the microprogram instruction (I) field. The first mnemonic defined, JSR (jump to subroutine), has a word position, size, and value of 4H0, 28X. This means that 4 bits are expressed as hexadecimal code "0" (4H0), followed by 28 "don't care" bits (28X), completing the 32-bit microprogram word. The second mnemonic (JL2) has the same format, except that the first four bits are expressed as hexadecimal "1". This sequence continues a total of 16 times through line 0220, RTN, which is expressed by hexadecimal code "F". This particular set of instructions and bit values are defined by the microprogram controller. Although other microprogram controllers would use different terms and bit patterns, assembler definitions would be programmed in a similar manner.

Definition program lines 0260 through 0280 define the NA field. Since this field is variable, ie, bit values are established by the microprogram assembly phase, a full set of mnemonics is not required. Instead, the three program mnemonic codes assist microcode writing by identifying the NA field function. The NA mnemonic designates a next address vector to be used for microprogram jump destinations. Its format statement 4X, 8VHTFF, 20X means four don't care bits (4X), which are already covered by the instruction field; followed by eight variable bits expressed in hexadecimal notation (8VH); the letter "T" truncates input information to the eight least significant bits; and FF is a default pattern if NA bits are not found in the microprogram. The eight NA bits are followed by 20 don't care bits (20X), completing the 32-bit microprogram word. The next two mnemonics define next address as an ALU operand designated by NC (numerical constant), and as a microprogram cycle counter, CC, for program loops. The letter "N" in the field definition (8VHNT) automatically generates the 2's complement (negation) of the cycle count as required by the microprogram controller.

Thirty branch instructions are programmed in a 5-bit BR field expressed as hexadecimal 5H00 through 5H1D. This field is physically located after the 12 previously

defined don't care bits (12x), and is followed by 15 don't care bits (15x). Hexadecimal numbers 5H08 through 5H1B are not shown in Fig 5 since the pattern repeats for the full list of BR field mnemonics.

Register file address (program line 0650) is a 4-bit variable field with a default to address 0 (4VH0). Don't care bits before (17x) and after (11x) position the four register file bits within the microprogram word. Accumulator address (program line 0690) is a 2-bit variable, default to 0 field (2VQ0), and is structured like the RF field. The letter "Q" illustrates the assembler's ability to work with octal data formats in addition to hexadecimal; binary format is also possible but is not illustrated in this example.

ALU function field and destination field follow the same patterns as described for the instruction and branch fields. Each field mnemonic is assigned a hexadecimal bit pattern and a location in the microprogram word. Various fields can be combined into other more complex instructions, as illustrated by the NOP (no operation) instruction, program line 1270. NOP has a format of 12 don't care bits (12x) followed by a 4-bit hexadecimal 0 (4H0), and a 16-bit fixed hexadecimal pattern 0138 (16H0138). Other higher level commands are possible and can be used to assist in writing microprograms.

Microprogramming Approach

The definition source file given in Fig 5 establishes the mnemonics to be used for writing microprograms. Assembly phase source files contain the microprogram routines that are assembled into system microcode. Fig 6 uses the previously defined mnemonic terms in a program example.

Performing a largest number task, the microprogram examines three binary numbers located in register files RF0, RF1, and RF2, and then moves the largest numerical value to RF3. Basically, the routine compares RF0 and RF1, and places the larger value in ACC3. Then, it compares ACC3 with RF2 and again places the larger value in ACC3. The last step transfers ACC3 to RF3. thereby accomplishing the program objective.

Writing this microprogram starts with a program title statement, followed by an option (OPT) line. The OPT line selects the definition table to be used, in this case, SYS800, which is the name of the file in Fig 5.

```
0010  TITLE LARGEST NUMBER
0020  OPT T=SYS800, L=#CN, N=80
0030  DCARE 1
0040 ;
0050 ; TEST RF0,RF1,RF2 LARGEST TO RF3
0060 ;
0070  ORG 000H
0080  FORM 32X
0090  ORG 100H
0100 ;                                          COMMENTS
0110 ; ENTER PROGRAM
0120 ;
0130  INC NA BR1 RF,1 ACC,3 TRF AAC           ;RF1>ACC3
0140  INC NA BR1 RF,0 ACC,3 SUAR ADRC         ;SUB ACC3-RF0>DR
0150  INC NA TCL RF ACC TRF ARF               ;TEST CARRY OUT
0160  BRC NA,SUBT NOP                         ;GO TO SUBT IF=1,INC IF=0
0170  INC NA BR1 RF,0 ACC,3 TRF AAC           ;RF0>ACC3
0180 SUBT INC NA BR1 RF,2 ACC,3 SUAR ADRC     ;SUB ACC3-RF2>DR
0190  INC NA TCL RF ACC TRF ARF               ;TEST CARRY OUT
0200  BRC NA,MOVE NOP                         ;GO TO MOVE IF=1,INC IF=0
0210  INC NA BR1 RF,2 ACC,3 TRF AAC           ;RF2>ACC3
0220 MOVE INC NA ENCR1 RF,3 ACC,3 ANAR ARF    ;ACC3>RF3
0230 ;
0240 ; EXIT PROGRAM
0250 ;
0260  INC NA CLUP RF ACC TRF ARF
0270  JMP NA,0BB NOP
0280  END
```

Fig 6 Largest number routine. Microprogram is entered through terminal keyboard using microprogram disc operating system (MDOS) editor. With editor, microprogrammer creates new disc file and enters all program information. When complete, file contents are stored on floppy disc. Microinstructions are written in terms established by field definition file in Fig 5. Additional program information is required to support next address, register file, and accumulator variable fields. In line 0130, RF,1 and ACC, 3 set bit patterns for respective fields. NA, not required in microinstruction, is allowed to default to FF. Program line 0160 establishes field value for NA through use of label (SUBT). When assembled, microprogram word address used for program line 0180 becomes line 0160 NA value. END statement concludes program

The output terminal is L=#CN, and the maximum printed line length is N=80. An optional don't care statement (DCARE 1) places logic 1 bits in any microprogram location not defined by the program.

Originating at word address 000 (ORG 000H), the microprogram is immediately followed by a form statement (FORM 32X) to put 32 don't care (logic 1) bits in all defined word locations between 000 and 100. A new originate statement at hexadecimal 100 (ORG 100H) redefines the program starting address and loads don't care 1s into words 000 through 0FF. This process is necessary because the processor used for this program example has preprogrammed (fixed) microprogram memory (P/ROMs) in the first 256 microprogram words. This fixed program includes I/O overhead, plus a keyboard interface to enter data, and a 7-segment LED display to output results. By loading 1s into a microprocessor development system (MDS) writable microprogram memory, the processor is able to do a logic AND between P/ROM and RAM at the same microprogram addresses, and thus have fixed P/ROM for the first 256 addresses and microprogram development RAM for the remaining memory words. Alternate approaches might merge the operating system into each microprogram routine, or hardware disable development RAM when addressing the first 256 program locations; however, the don't care statement is more convenient because these outputs are wire-ANDed to the resident P/ROMs.

The largest number routine starts at microprogram word hexadecimal 100, and each microinstruction is entered in field mnemonic terms. Microinstructions start with an instruction field command (INC or BRC), followed by next address (NA), branch (BF1), etc. Most program lines start with the instruction field command located two spaces after the line number. Lines 0180 and 0220 are exceptions in that the program line starts with a label identifier (SUBT or MOVE) one space away from the line number, followed by a normal microinstruction. As with any assembler, the use of labels eliminates the need to keep track of program addresses, and facilitates editing or merging programs. A 2-word exit program starting at line 0260 jumps the program back into the P/ROM operating system after the largest number routine is completed.

Taking the programmer understandable program in Fig 6 the microprogram assembler converts it to processor compatible microprogram bit patterns, as shown

```
0010                              TITLE LARGEST NUMBER
0020                              OPT T=SYS800, L=#CN, N=80
0030                              DCARE 1
0040                    ;
0050                    ;         TEST RF0,RF1,RF2 LARGEST TO RF3
0060                    ;
0070                              ORG 000H
0080 0000 FFFFFFFF                FORM 32X
0090                              ORG 100H
0100                    ;
0110                    ;         ENTER PROGRAM
0120                    ;
0130 0100 CFF00F11                INC NA BR1 RF,1 ACC,3 TRF AAC
0140 0101 CFF00644                INC NA BR1 RF,0 ACC,3 SUAR ADRC
0150 0102 CFF28113                INC NA TCL RF ACC TRF ARF
0160 0103 50500138                BRC NA,SUBT NOP
0170 0104 CFF00711                INC NA BR1 RF,0 ACC,3 TRF AAC
0180 0105 CFF01644 SUBT           INC NA BR1 RF,2 ACC,3 SUAR ADRC
0190 0106 CFF28113                INC NA TCL RF ACC TRF ARF
0200 0107 50900138                BRC NA,MOVE NOP
0210 0108 CFF01711                INC NA BR1 RF,2 ACC,3 TRF AAC
0220 0109 CFFE1E83 MOVE           INC NA ENCR1 RF,3 ACC,3 ANAR ARF
0230                    ;
0240                    ;         EXIT PROGRAM
0250                    ;
0260 010A CFFC0113                INC NA CLUP RF ACC TRF ARF
0270 010B 2BB00138                JMP NA,0BB NOP
0280                              END

TOTAL ERRORS      0
```

Fig 7 Typical assembler output listing. By showing program line number, microprogram word address, memory contents, labels, and field mnemonics, microprogram assembler output listing makes satisfactory work sheet for microprogram corrections. During system debug, simple changes can be made directly on microprogram development hardware using hexadecimal bit patterns; more extensive changes can be made by correcting microinstruction mnemonics and reassembling program. In any case, assembler output makes permanent record of microprogram contents. Bottom assembler output line shows that there are no program errors, which would prevent assembler from assigning microprogram bit patterns. Most common error results from typing mistakes, causing mnemonic terms that do not exist in definition lookup table. Other errors include improper label assignments and source statement combinations that do not equal proper microprogram word length. MASM microprogram assembler checks for and identifies up to 56 error types to help correct program errors

```
0010                        TITLE 2'S COMPLEMENT MULTIPLY
0020                        OPT T=SYS800, L=#CN, N=80
0030                ;
0040                ;       MULTIPLY RF0 TIMES RF1 TO RF2 RF1
0050                ;
0060                        HEADER 6/INST/,9/NXT ADD/,8/BRANCH/,6/RF/,
0070               /7/ACC/,66/ALU/,6/DEST/

     ADD  HEX OBJ  LABEL    INST  NXT ADD  BRANCH  RF     ACC     ALU    DEST

0080                        ORG 10CH
0090                ;
0100                ;       ENTER PROGRAM
0110                ;
0120 010C D00E0111          RSR   NC,00    ENCR1   RF     ACC,0   TRF    AAC
0130 010D DF800802          RSR   CC,08    BR1     RF,1   ACC,0   ADAR   ARFC
0140 010E 01238113          JSR   NA,SUB   TLL     RF     ACC     TRF    ARF
0150                ;
0160                ;       EXIT PROGRAM
0170                ;
0180 010F CFFC0113          INC   NA       CLUP    RF     ACC     TRF    ARF
0190 0110 2BBE1083          JMP   NA,0BB   ENCR1   RF,2   ACC,0   ANAR   ARF
0200                ;
0210                ;       SUBROUTINE
0220                        ORG 112H
0230                ;
0240 0112 61700138 SUB      BRM   NA,17    NOP
0250 0113 FFF009A2 SHR      RTN   NA       BR1     RF,1   ACC     RORR   ARFC
0260 0114 21300170          JMP   NA,SHR   BR1     RF     ACC,0   ASRA   AACC
0270 0115 21700041          JMP   NA,SHA   BR1     RF,0   ACC,0   SUAR   AAC
0280 0116 21700001          JMP   NA,SHA   BR1     RF,0   ACC,0   ADAR   AAC
0290 0117 21300170 SHA      JMP   NA,SHR   BR1     RF     ACC,0   ASRA   AACC
0300                        END

TOTAL ERRORS      0
```

```
010C  1101000000001110 0000000100010001
010D  1101111110000000 0000100000000010
010E  0000000100100011 1000000100010011
010F  1100111111111100 0000000100010011
0110  0010101110111110 0001000010000011
0111  XXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXX
0112  0110000101110000 0000000100111000
0113  1111111111110000 0000100110100010
0114  0010000100110000 0000000101110000
0115  0010000101110000 0000000001000001
0116  0010000101110000 0000000000000001
0117  0010000100110000 0000000101110000
```

Fig 8 2's complement multiply routine. Each microprogram field shows what is happening in a particular section of microprogrammed processor. For example, first instruction, line 0120, translates as: RSR (microprogram control reads contents of NA field), NC,00 (numerical constant value=00), ENCR1 (transfer NA constant to ALU register file input), RF (not used), and ACC,0 TRF AAC (transfer register file/next address value through ALU to accumulator word 0). Program line 0250 illustrates programming power of single microinstruction. RTN returns from subroutine, but also examines cycle count initialized in line 0130. Depending on count value, it either returns to microprogram address 010E and stays in loop or returns to address 010F, which ends program. Simultaneously, remainder of microinstruction rotates contents of register file word one bit to right. Each program line is executed in one machine microinstruction cycle time (100 ns for Fig 3 processor), independent of mnemonic selection

in the assembler output listing (Fig 7). In addition to source statements (Fig 6), the assembler adds microprogram word addresses followed by the 32-bit (8 hexadecimal digit) program data. Program line 0080 shows eight Fs or all binary 1 bits, for don't care locations 0000 through 00FF. Unless otherwise directed, the program follows consecutive word addresses, in this example 0100 through 010B. The microprogram assembler also stores the assembled program output on floppy disc, which can be easily loaded into the development system RAM for program debug.

A second example, the assembler output of a 2's complement multiply microprogram routine (Fig 8), shows a method of writing and locating subroutines, and the use of a header statement to format the assembler output into field-oriented columns. Program lines 0060 and 0070 provide column heading and column spacing information. A program starting address (ORG 10CH) allows the program to immediately follow the assembler output listing (see Fig 7), which ends at address 010B.

This 8-bit 2's complement integer multiplication routine begins with the multiplicand in RF0 and the multiplier in RF1. Based on Booth's algorithm, the following program flow calculates a double-precision product located in RF2 and RF1.

	Program Step			Program Line (Fig 8)	
(1)	Zero ACC0 and link bit			0120	
(2)	Set cycle counter to 8			0130	
(3)	Test RF1 LSB and link bit (4-way branch)			0240	
	LSB	Link			
	0	0	GO TO 4		
	0	1	GO TO 5		
	1	0	GO TO 6		
	1	1	GO TO 7		
(4)	Arithmetic shift right ACC0, GO TO 8			0260	
(5)	Subtract ACC0 − RF0→ACC0, GO TO 7			0270	
(6)	Add ACC0 + RF0→ACC0			0280	
(7)	Arithmetic shift right ACC0			0290	
(8)	Rotate shift right RF1			0250	Combined
(9)	Decrement cycle count; if ≠0, GO TO 3			0250	Combined
(10)	Transfer ACC0 to RF2			0190	
(11)	Exit			0180, 0190	

The program flow in Fig 8 closely follows the program steps, although some microinstructions are not intuitively clear and would require a detailed understanding of processor operation. For example, the first microinstruction, program line 0120, zeros ACC0 using instruction RSR, numerical constant (NC) 00, and branch ENCR1 to generate the constant, put it on the register file ALU input, then transfer it through the ALU to the accumulator (ACC). BRM in program line 0240 looks at the LSB and link bit, tests the results (TLL in line 0140), and does a 4-way branch to microprogram addresses 0114, 0115, 0116, or 0117, as established by NA, 17 following the BRM instruction. The multiply program also uses an originate statement (ORG 112H) internal to the program to establish the subroutine starting address. In this manner, a subroutine can be placed anywhere in microprogram memory for smoother program continuity.

The bottom section of Fig 8 shows the microprogram assembler's binary output listing. Binary data are especially useful at system checkout since they eliminate the hexadecimal to binary conversions otherwise required to look at digital signals. Notice that all Xs are placed in microprogram word 0111 since the word is not defined in Fig 8.

Summary

The microprogram examples (Figs 7 and 8) illustrate the bookkeeping power of microprogram assemblers. Taking programmer oriented source statements, the assembler assigns microprogram addresses and digital bit patterns. When used with microprogram development hardware, the assembler allows system checkout without requiring microcode to be entered in error-prone binary format. The microprogram examples are written around a particular processor design and microprogram word structure. However, the microprogram assembler, through the definition phase program, adapts to a wide range of system sizes and architectures. Being technology independent, the assembler works with LSI or MSI ECL, TTL, or CMOS microprogrammed processor designs. Also application independent, the assembler can be used for peripheral controllers, signal processors, test equipment, process control, minicomputers, or any application taking advantage of microprogrammable processor performance and flexibility.

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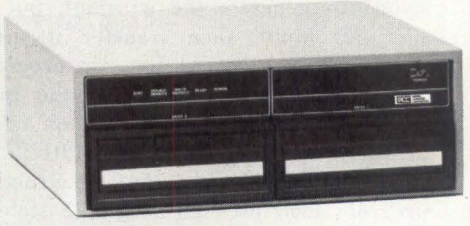

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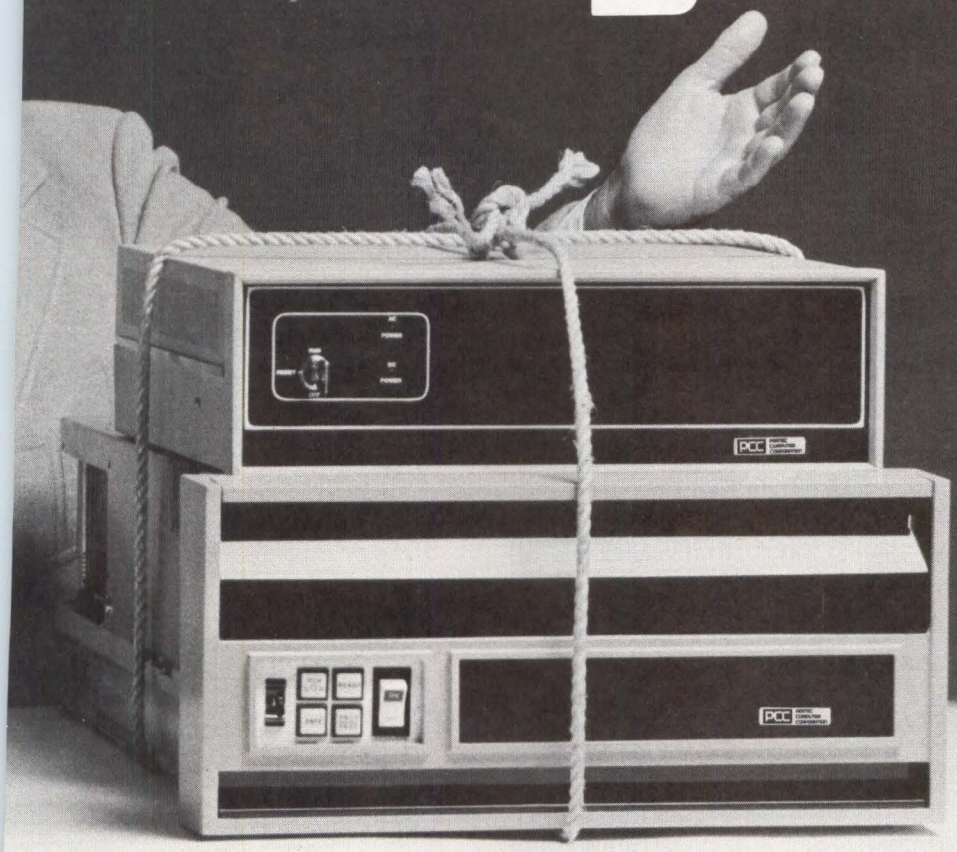

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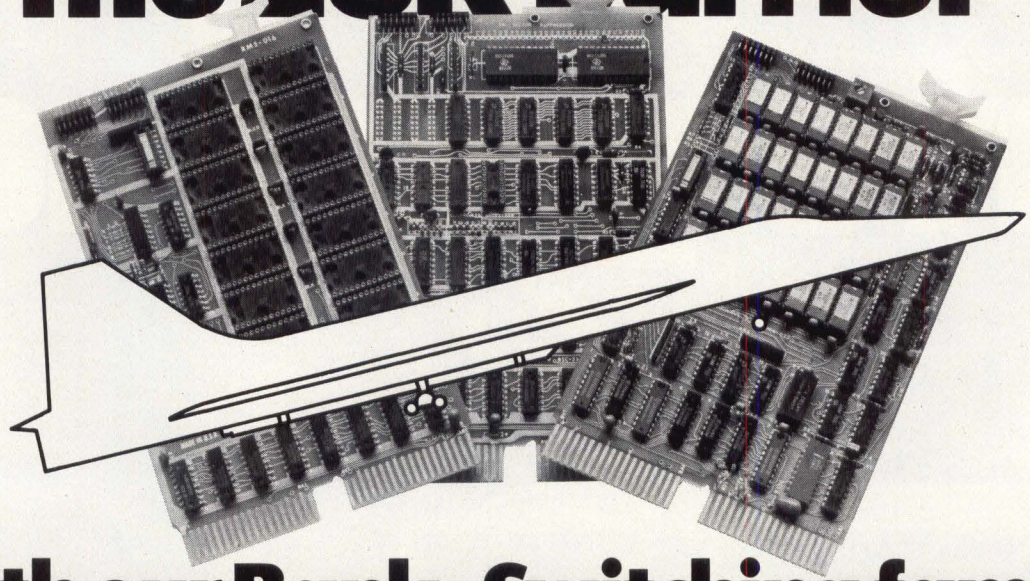

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MILITARY MULTIPLEX STANDARD DEFINES VERSATILE SERIAL BUS

A bus interface and communication protocol for avionic digital signal multiplexing, MIL-STD-1553B defines high speed serial address, command, and signal information for up to 31 terminals interconnected by a single shielded twisted pair

David R. Brickner Sperry Flight Systems, Phoenix, Arizona

A decade ago, military and NASA aircraft electronic designers visualized an airborne central computer complex for aircraft systems management. However, the wiring to remote sensors, actuators, and electronics, all converging on one centralized location, was a significant design obstacle. Consequently, as the space shuttle system and new military aircraft design requirements were being conceived in the late sixties, several industrial committees were formed to review future data communication needs and to develop a standard technique for handling digital signal multiplexing. The military standard that evolved, MIL-STD-1553B[1], is now in its third generation. This standard defines a high speed, low error rate characteristic using a shielded twisted conductor pair as the transmission medium. Up to 31 terminals can be tied to the single signal conductor or bus. The standard differs from most other connection protocols in that all address data, command data, and signal information are carried in serial format on the same single bus. Redundant buses may be used as required by the particular aircraft mission. The standard also provides capabilities that allow distributed data processing within the network of terminals.

Background Information

Fig 1 shows an outline of a typical aircraft data terminal multiplex system installation. Two multiplex buses interconnect data terminals in the forward instrument panel area, in the overhead control panel, in the midship electronics area, and in the aft area. As an example, each terminal might connect between 30 and 300 signals to either of the dual data buses. In this installation, one can appreciate the dramatic reduction in wiring that is made possible. A maze of wires, cable clamps, and bulkhead connectors is replaced by a pair of bus conductors. The only real need for two buses is to provide redundancy, a reliability level that may not have even existed for most signals in a conventional aircraft system.

Terminals connected to the bus may be functionally dedicated to such tasks as air data computing and gyroscopic sensing, or they may be general purpose units designed to connect several independent sensors, actuators, or subsystems to the data bus. Terminals are presently being designed into radios, navigation systems, flight control systems, and monitoring instruments. Cathode ray tube displays are being developed for direct interface to the

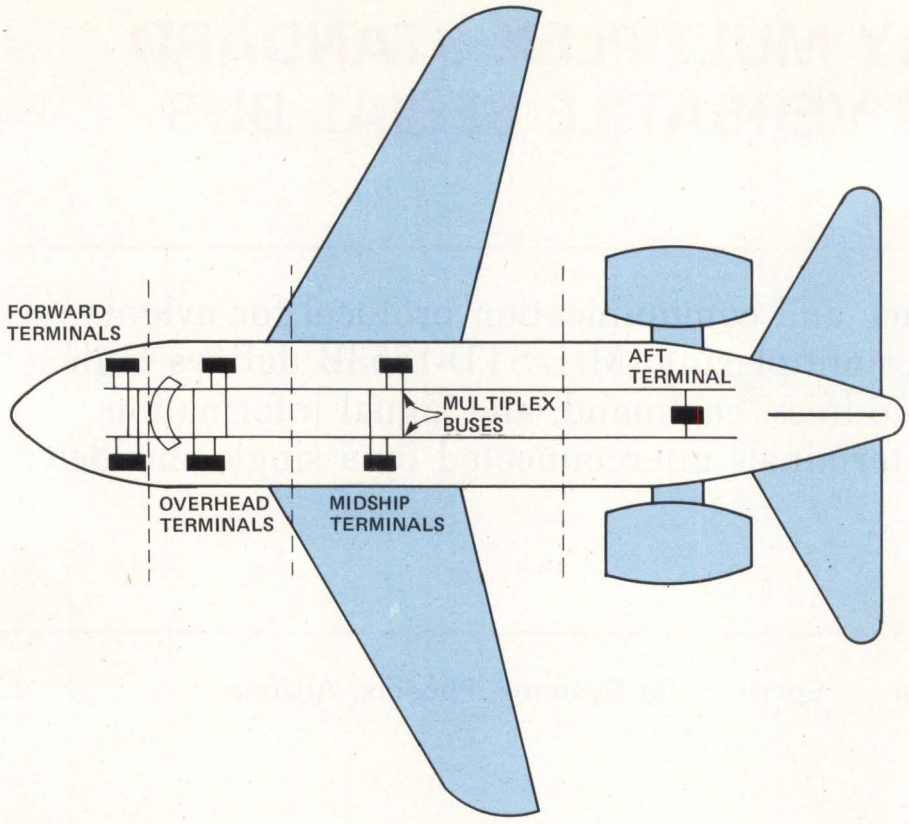

Fig 1 Typical aircraft communication system. Multiple terminals are used to connect electrical and control signals over two redundant data buses. Any two terminals act as bus controllers to direct data flow

multiplex bus and will eventually replace conventional instruments and gauges in the cockpit. Other terminals contain signal conditioning equipment to adapt signals from conventional equipment for use in new multiplex systems. In either case, any terminal connected to the bus has access to every signal on the bus.

A designated bus controller terminal directs data traffic on the bus. The military standard allows this controller function to be independent, or colocated with other terminals on the bus. The latest version of the standard provides for dynamic reassignment of the bus control function. This allows the concept of a distributed processor system to be developed within the specifications of the standard for both avionic and non-avionic applications.

Less wiring, lighter weight, and reduced complexity are several major benefits of multiplex. Since a broadly accepted standard exists for the multiplex characteristics, equipment can be added or changed in the aircraft system without affecting other major wiring, an outstanding advantage for increased flexibility and virtually unlimited growth. Another significant advantage is the ability for total system integration. For instance, aircraft handling characteristics may be modified as a function of weapon delivery or change in mission. This type of integrated approach is possible because all terminals in the network have access to all data in the network.

Multiplexing Methods

Two common multiplex techniques are frequency division multiplex (FDM), where each signal is assigned a different modulation frequency, and time division multiplex (TDM), where each signal is assigned a different time slot. The latter technique, widely applied to data and address bus structures in microprocessor based systems, has been selected for aircraft systems integrated to meet the design goals of minimal wiring, light weight, and change and growth flexibility. Multiplexed signal paths to send and receive terminals involve one or more of the following processes:

Simplex—a terminal sends signals on one conductor and receives signals on another.

Half duplex—a terminal sends data on the same conductor over which data are received, but never simultaneously.

Full duplex—a terminal sends and receives signals simultaneously over the same conductor.

The half-duplex mode has been incorporated into MIL-STD-1553B. If full duplex had been chosen, some form of FDM would be required to separate the sending and receiving signals on the bus. On the other hand, selection of a simplex scheme would require attachment of multiple conductors to terminals which had to both send and receive data. Half duplex offers the compromise of a slightly lower data exchange rate without additional signal conductor hardware.

Signals on the bus are in Manchester format with a 1-MHz basic bit rate. The self-clocking Manchester waveform is prevalent in data encoding schemes for tape or disc storage.[2] The key characteristic concerns easy clock synchronization to a received Manchester signal. Once synchronized, data can be selected by examining the transition of the signal within each clock period. In Fig 2 (a), data consist of a typical random pattern of 1 s or 0 s. In Figs 2 (b) and 2 (c), the synchronization characters are included. One of the two characters is used at the start of each word transmitted on the bus. Data synchronization distinguishes data words from command and status words.

Messages on the data bus are in groups of 16-bit words, where each word is preceded by an appropriate 3-bit time synchronization, and appended with a parity bit, for a total of 20 bits. Maximum data transfer rate over the bus is approximately 48k data words/s, or 768k baud. In most applications, actual bus utilization is considerably less, with typical "bus loading" of from 20 to 60%.

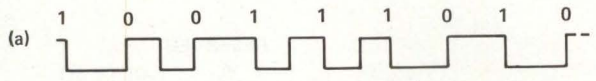

Fig 2 (a) Typical Manchester data. Data are contained in "mid-bit" transition, where falling signal indicates logic one, while rising signal signifies logic zero

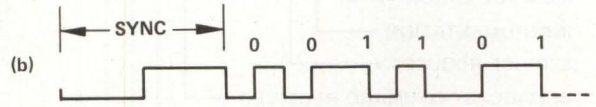

Fig 2 (b) Data word with sync. Waveform which lasts for 1.5 bit times without change is illegal Manchester signal. Two such illegal signals form synchronizing character for data words

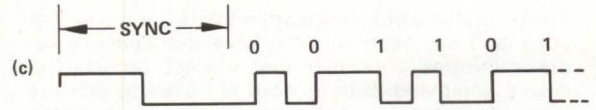

Fig 2 (c) Command or status word with sync. Synchronization for command word is opposite in polarity to synchronization preceding data words

Bus Controller

The standard assumes the existence of a single bus controller at any given time. However, bus control authority may be granted from one terminal to another. Each terminal is assigned an address via hardwiring at the terminal. This terminal address, which designates the message transmitter or listener, also designates a new controller when a control transfer is issued.

The bus controller directs signal traffic on the bus by issuing command words containing the address of the terminal commanded to listen to data on the bus, or to transmit data on the bus. Four message exchange types are:

Controller to Terminal—called a "receive command"; the terminal may receive up to 32 words and must respond with a status word.

Terminal to Controller—called a "transmit command"; the terminal must transmit a status word and up to 32 data words.

Terminal to Terminal—called a "terminal to terminal transfer command"; the controller first designates the receiver, and issues a second command word to designate the transmitter. The transmitter responds with a status word and up to 32 data words. The receiver answers with its own status word.

Broadcast—the controller issues a receive command to specific address "31", followed by up to 32 data words. All terminals equipped for broadcast command recognize this reserved address and receive the data. No status commands are issued.

Protocol Organization

The command word is made up of a command synchronization, followed by 17 bits of information; the last bit is reserved for parity. As shown in Fig 3, the address designates the terminal to which the command word is directed. While all terminals must monitor the bus, they can disregard any command that does not contain their address. The assumption is that each terminal has some form of

Optional Mode Codes

Mode Code	Function
00000	Dynamic bus control
00001	Synchronize
00010	Transmit status word
00011	Initiate self test
00100	Shut down transmitter
00101	Override transmitter shutdown
00110	Inhibit terminal flag bit
00111	Override inhibit terminal flag bit
01000	Reset remote terminal
10000	Transmit vector word
10001	Synchronize
10010	Transmit last command word
10011	Transmit bit word
10100	Shut down selected transmitter
10101	Override selected transmitter shutdown

hardwired address to compare with the command word address. In most installations, this address is wired into a connector that mates with a terminal at a given location.

The subaddress/mode code field provides for 32 major operations in a terminal. Use of the subaddress field is left entirely to the designer of the terminal function. In some terminals, only a single subaddress is required for data transfer. In others, it may be necessary to use one subaddress to designate an index code where the message data words provide subaddress expansion. In such cases, there is no limit to the addressing possibilities.

The all-zeros content of the subassembly field is reserved to designate the word count field as a mode code. Normally, this field is used for the obvious task of designating the number of words in the message. In the special case of code operations, the specific mode code designates the operation, and whether or not a message word is to be exchanged. Mode codes are intended to be reserved for controlling the terminal itself and have nothing to do with the data exchanged through the terminal. Any words accompanying mode codes are referred to as message words. In any application, not more than one of these message words is allowed.

Mode codes are a problem in the standard because they tend to complicate the machinery needed to operate on the bus. Designers of the standard had the foresight to make the use of mode codes optional, as required by the function of the terminal. Fifteen different mode codes are allowed (see Table).

One mode code adds a special dynamic enhancement to the standard. This mode is coded with an all-zeros mode control field and designates a handoff of bus control. One bit of the status word is designated as an accept bit for this transfer. Thus, if a system is designed with more than one bus controller, at the option of the terminal in control the control is passed to any other terminal on the bus using this command. When the designated terminal responds with the status word containing the acknowledgment, the transfer is complete. Multiple controllers of this type are used in multiplex systems to allow division of the data processing load among several terminals to form a distributed system, and to allow a system to have redundant controllers for purposes of increasing system reliability. Both uses are allowed by the standard.

Data words have a simple structure (Fig 4), and there are no restrictions on the data transmitted. The standard does require that the most significant data bit be transmitted first and that any unused bits be transmitted as zeros. Status words are issued by remote terminals as transmission/acknowledgment signals. The format shown in Fig 5 is used to signal the controller that the command has been properly received and can be executed properly. Status bits also inform the controller of other terminal information, as shown by the specific bits defined in the figure. The designers attempted to allow broad applications of the standard by defining specific meanings of bits in the status word, but making the application optional. Only two bits, message error and parity, must be used.

Message Formats

Three types of messages are shown in Fig 6. In the first message [Fig 6 (a)], the controller needs to send data to a remote terminal. The command word selects the terminal and specifies how many words it is to receive. It is then fol-

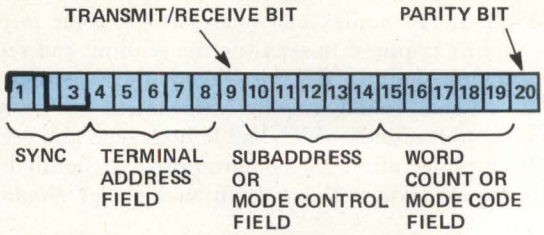

Fig 3 Command word. This word is used by bus controller to direct activity on bus. Terminal address selects terminal that is to react to command. Subaddress and word count field specify action to be performed by terminal

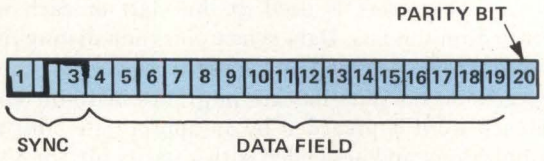

Fig 4 Data word. No restrictions are placed on data contents. Data may originate at any terminal in system under command of bus controller. Data are always transmitted most significant bit first and immediately after sync field

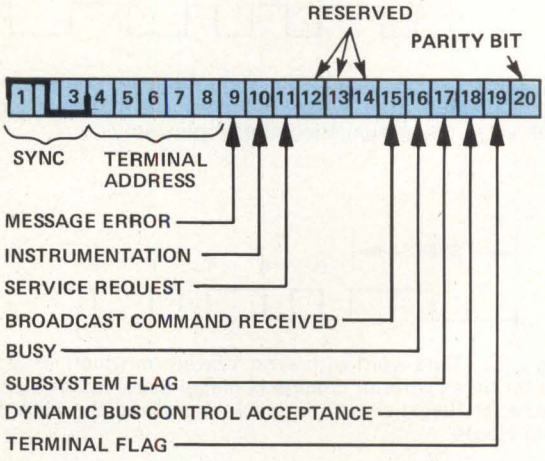

Fig 5 Status word. This word informs controller that command has been correctly received. Terminal address informs controller that correct terminal received command. Bits in word are used to indicate terminal status to controller. Three bits in status word are reserved for future extensions of standard and cannot be used at this time

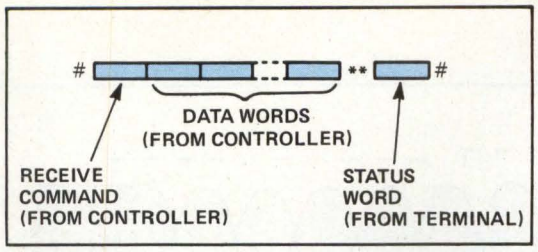

Fig 6 (a) Controller to remote terminal (RT) transfer. Controller sends command word and up to 16 data words. Terminal receives data and responds with status word

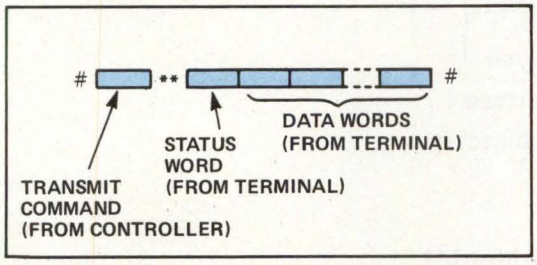

Fig 6 (b) Remote terminal to controller transfer. Controller initiates transfer with command word. Addressed terminal then responds with status word and appropriate number of data words (up to 16)

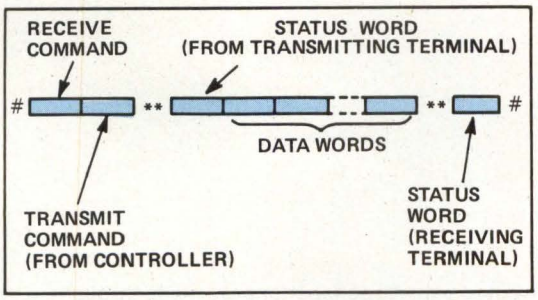

Fig 6 (c) RT to RT transfer. Data transfer between terminals is directed by bus controller. Transfer is initiated by two commands which select sending and receiving terminals. Message also contains status word for each commanded terminal

Fig 6 Message formats. Three message formats are allowed on multiplex bus. ** depicts allowed response time of from 2 to 10 μs; also, # indicates between message gap which must be at least 2 μs

lowed by the number of words specified. The controller waits until the receiving terminal replies with a status word confirming that the message was correctly received. In the status word format, the address of the receiving terminal is contained within the status word, confirming that the desired terminal is responding.

The second message [Fig 6 (b)] is similar except that the controller asks the remote terminal to transmit data; the remote terminal begins with the status word.

The last message [Fig 6 (c)] is terminal-to-terminal transfer; the controller must send two consecutive commnd words to get the attention of the two terminals. This message also contains two status words, indicating correct response by both terminals. Other message formats deal with broadcast data and mode codes. These formats are detailed in the standard and provide subtle operations and capabilities beyond the scope of this article. Presently, the most common systems use only the first two formats of Fig 6.

Electrical Definitions

The basic intention of the standard is to use a shielded twisted pair as the signal conductor. Information is impressed on the signal pair differentially. Cables are terminated in their characteristic impedance, and all terminals are intended to be transformer coupled on and off the bus. The general structure is to use a trunk and stub arrangement; direct connections are also allowed. Common parameters are voltages and waveforms on the main trunk; both connections are shown in Fig 7. Total cable length in the system should not exceed 300 ft (91 m), according to the standard.

Voltage on the main trunk is expressed as 6 to 9 V peak to peak in normal operation and is measured between the twisted lines. This amplitude is usually sufficient; should one terminal in the network become shorted, communication to other terminals is still possible on the bus system. Thus, there is adequate design margin in the system. In some non-aircraft applications it may be possible to design systems with greatly reduced signal levels. Input impedance is 1.5 kΩ or greater when the terminal is listening, and drops to near zero when transmitting. Designers must be especially cautious about dc offset in the transmitter circuit, because dc terms in the transmittal signal tend to "charge" the transformer coupled lines. This effect dramatically increases susceptibility to noise and may preclude any communication.

The airborne environment for which the standard is primarily intended is filled with noise sources, from spurious transmissions and ground loops to intentional jamming attempts. Understandably concerned with transmission security under such conditions, the standard requires a maximum word error rate of one part in 10^7 when 200 mV rms of white noise in the 1-kHz to 4-MHz band is added to a valid signal level of 3 V peak to peak. This requirement places stringent filtering and decoding requirements on the receiver. However, for non-aircraft applications, the system can be designed for less noise rejection.

Applications

Several applications of multiplex were reported at two Air Force sponsored conferences on multiplex[3,4]. The Air Force

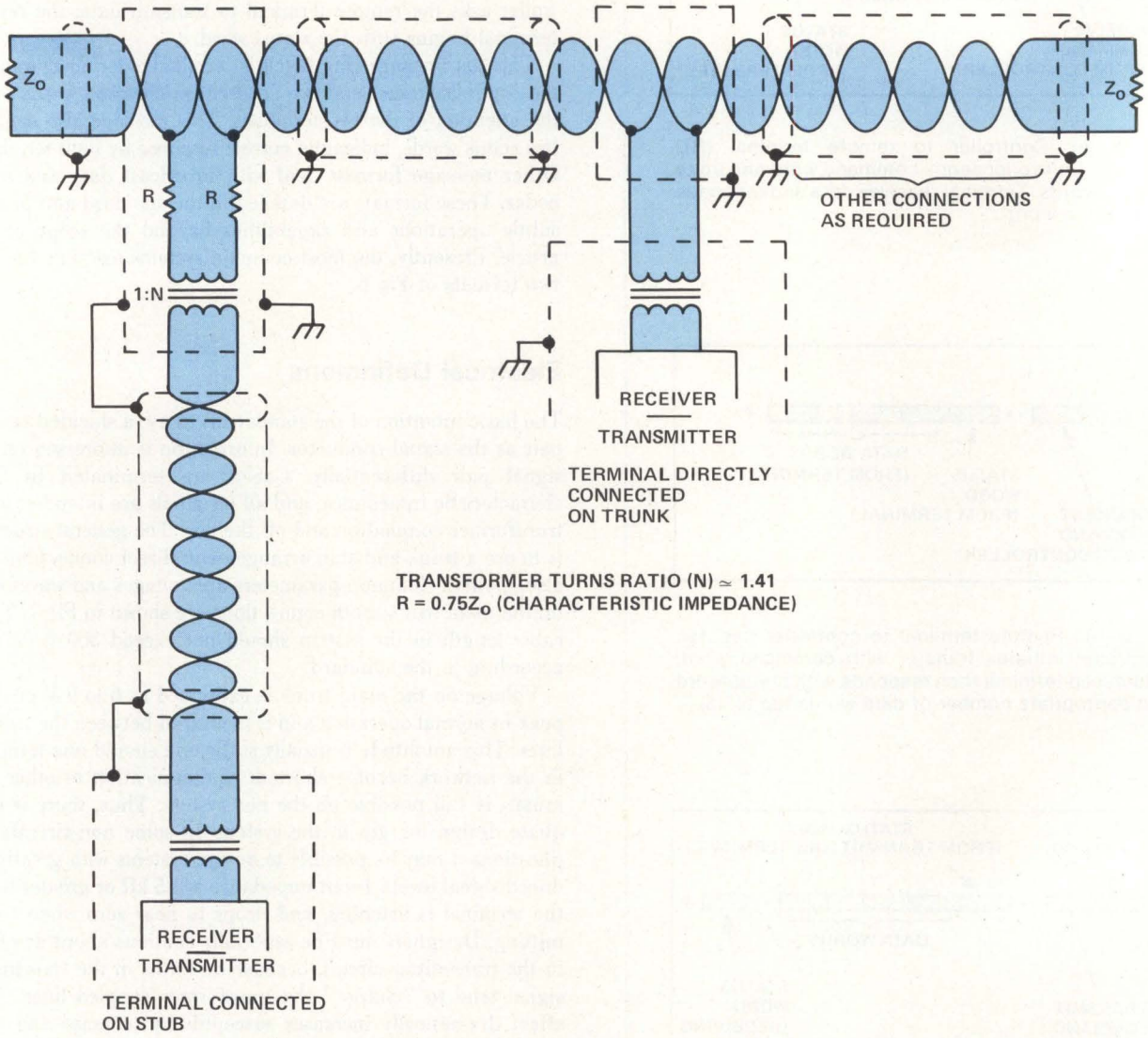

Fig 7 Terminal connections to serial data bus. Cable is shielded twisted pair. All connections are made through signal transformers. Long connections must be made with bus coupler, which reduces reflected stub length and matches stub impedance to trunk. Transmitter amplitudes must be adjusted so that signals impressed on main trunk are from 6 to 9 V peak to peak, line to line

uses a system concept called DAIS (digital avionic integration system) to study future applications of the concept to fighter aircraft; the Army has a program called ADAS (army digital avionic system) with a similar goal for tactical helicopter applications. F-16 and F-18 fighter aircraft and the advanced attack helicopter designs have successfully used multiplex to reduce wiring and to increase flexibility.

The advanced attack helicopter system uses nine remote terminals and redundant data buses to integrate the fire control system. This system features dynamic bus control as part of the redundant bus control concept. The space shuttle system has a network of 28 data buses and over 20 ter-

minals to interconnect all systems on the orbiter and solid rocket booster. Fig 8 shows a typical terminal for use in space shuttle payloads. This terminal provides conditioning of subsystem data signals on the data bus as well as a subsystem control via a microprocessor.

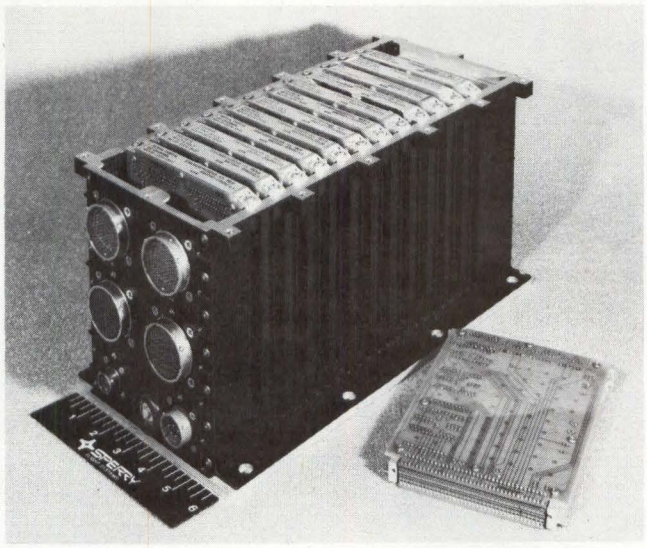

Fig 8 Space shuttle payload terminal. This terminal couples payloads carried by space shuttle to orbiter data multiplex system. Terminal also provides signal conditioning and control for payload or experiment signals. Modular terminal may be reconfigured in field

Several semiconductor companies have recently introduced large scale integrated (LSI) circuits for the bus interface function of the standard. These circuits provide the address decoding and logic to determine message functions. Terminals use these LSI functions along with other LSI and hybrid integrated circuits to achieve both small size and high reliability. Availability of off-the-shelf terminals and LSI functions is expanding the implementation of multiplex. Presently, several aerospace companies are trying various schemes to replace the trunk and stub array with fiber optics for increased reliability and reduction of susceptibility to electric and magnetic interference.

The ability to connect up to 31 terminals on a single shielded twisted pair has applications in many areas other than aircraft. For non-aircraft applications, the designer may consider other multiplex variations. For instance, for short (a few feet) runs, it might be practical to use TTL or nonreturn-to-zero (NRZ) coding, instead of transformers and Manchester coding. In other applications, modulation of a carrier and communication over existing power cables might be considered. Broad application of this standard will benefit both civilian and military designers by making a wider range of terminals and LSI functions available at lower cost.

Summary

The United States military has developed a serial data multiplex standard for use in aircraft. The standard provides for low error-rate data transmission in electrically noisy environments. The data bus can be used to interconnect up to 31 independent terminals with data transfer message organized in a demand-response format. All message traffic is controlled by the bus controller, whose role is transferable among the terminals on the data bus network. Electrical format of the standard is based on transmission of data using Manchester waveforms over a differential twisted shielded pair. All terminals are transformer coupled to the bus in a manner that allows communication to continue on the data bus even in the event of a faulty terminal in the network. Redundant data bus networks are allowed in critical applications.

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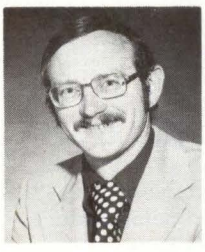
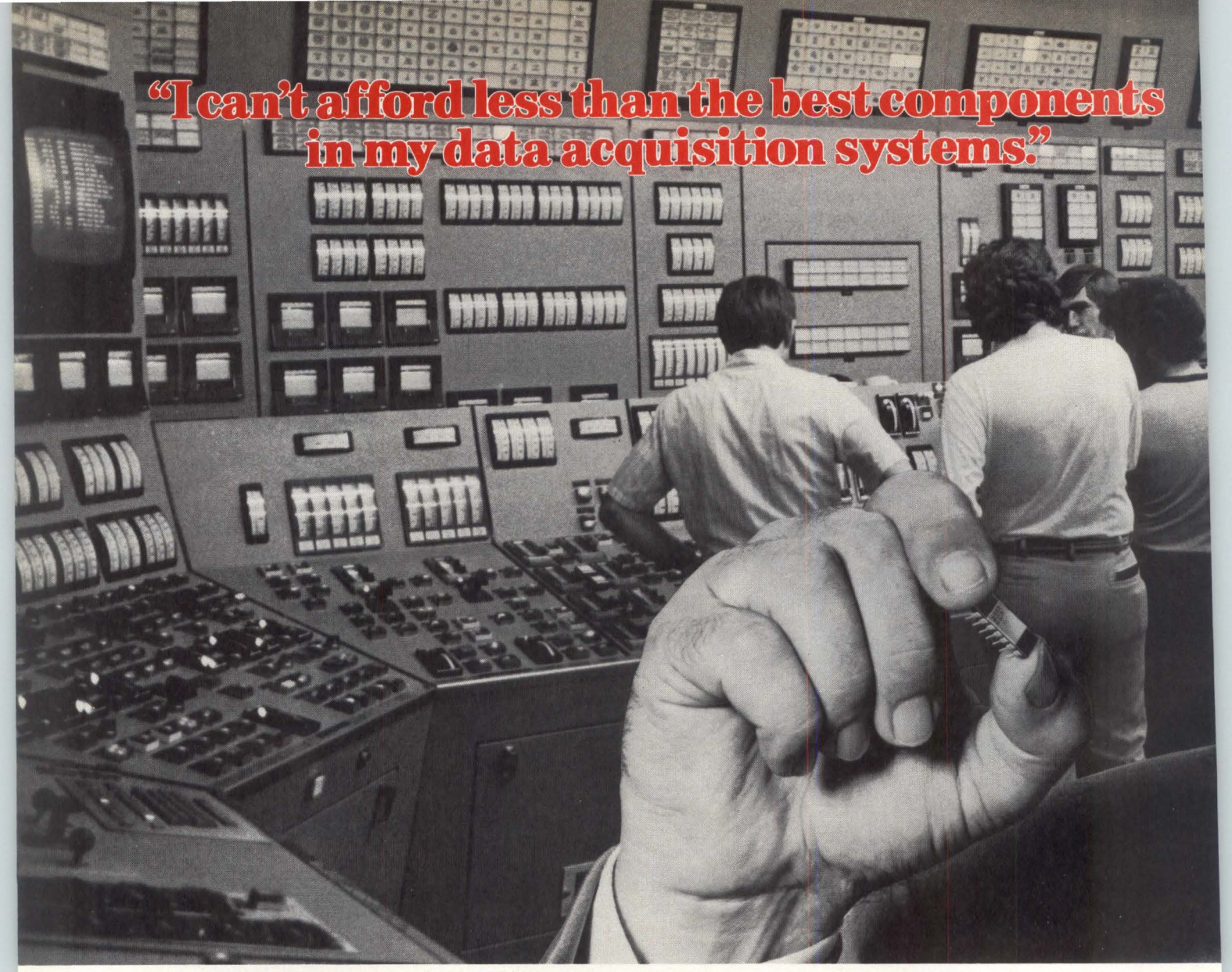


David R. Brickner is an engineering section head at Sperry Flight Systems. He is currently the company's representative on the A2K Multiplexing Committee of the Society of Automotive Engineers. Mr Brickner holds a BEE degree from General Motors Institute and an MSE from Arizona State University.



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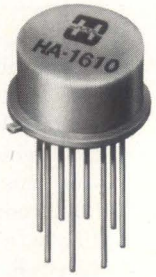

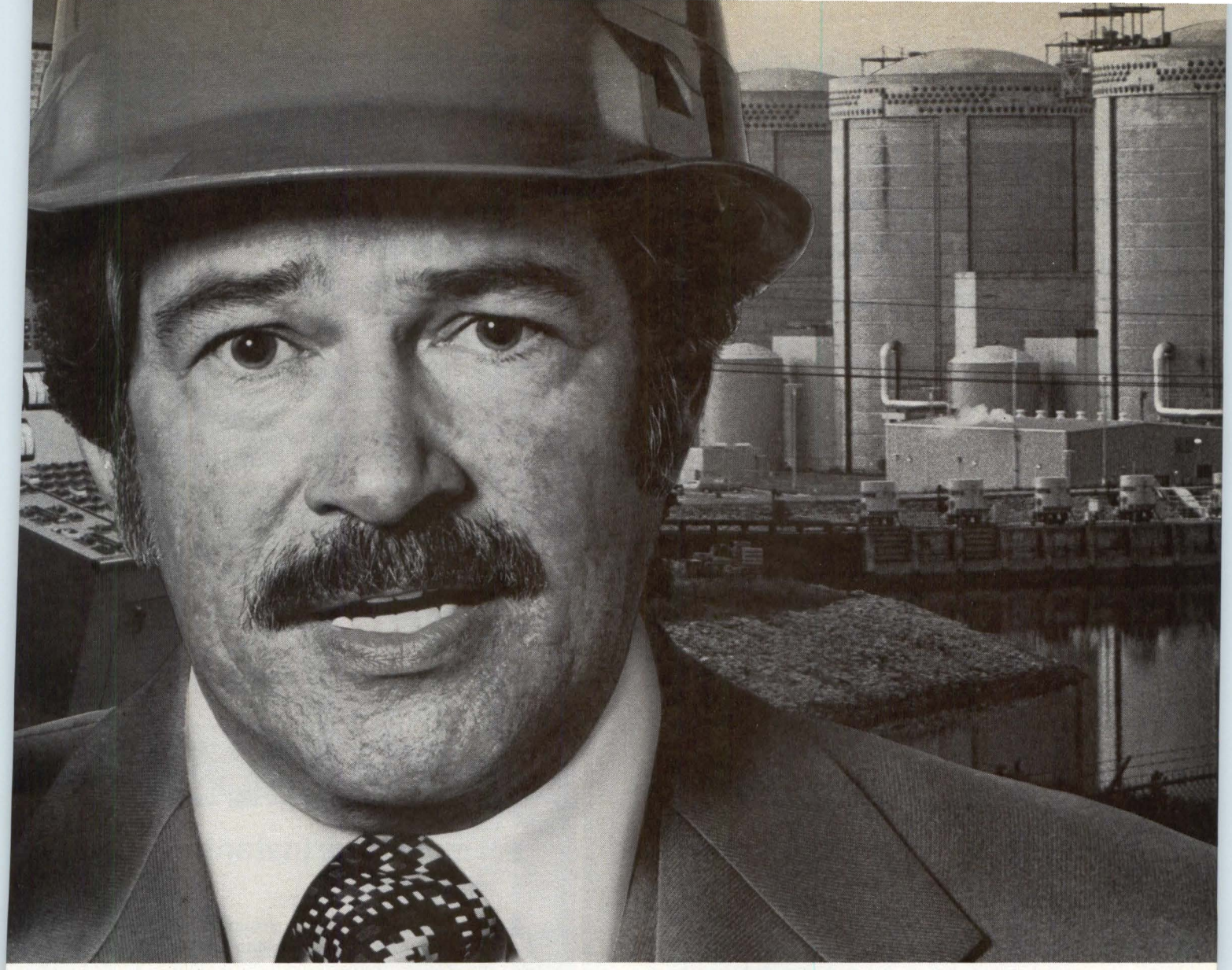

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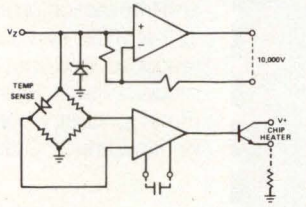

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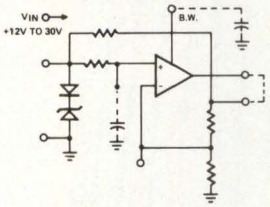
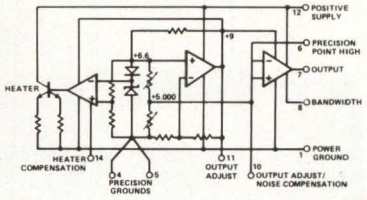
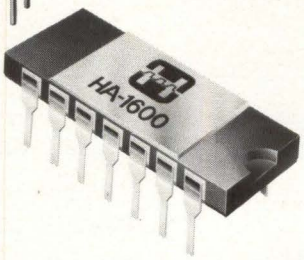


HA-1620 Precision 5 Volt Reference
With Adjustable Output





Harris Precision Voltage References Performance Parameters

Harris Part No.	Output Voltage	Temperature Range	Package	Tempco, Max. (ppm/°C)	Line Reg., Max. (%/V)	Load Reg., Max. (%/mA)	Resolution for 1 LSB Accuracy
HA1-1600-2	+10	−55 to +125°C	14-Pin Hermetic Dip	1.35	0.002	0.002	12 Bits
HA1-1602-2	+10	−55 to +125°C	14-Pin Hermetic Dip	2.70	0.002	0.002	11 Bits
HA1-1605-5	+10	0 to +75°C	14-Pin Hermetic Dip	3.25	0.002	0.004	12 Bits
HA2-1610-2	+10	−55 to +125°C	TO-99 Metal Can	3.0	0.004	0.004	10 Bits
HA2-1610-5	+10	0 to +75°C	TO-99 Metal Can	3.0	0.004	0.004	12 Bits
HA2-1615-2	+10	−55 to +125°C	TO-99 Metal Can	5.0	0.004	0.004	9 Bits
HA2-1615-5	+10	0 to +75°C	TO-99 Metal Can	5.0	0.004	0.004	11 Bits
HA2-1620-2	+5	−55 to +125°C	TO-100 Metal Can	1.0	0.002	0.002	12 Bits
HA2-1620-5	+5	0 to +75°C	TO-100 Metal Can	1.0	0.002	0.002	13 Bits

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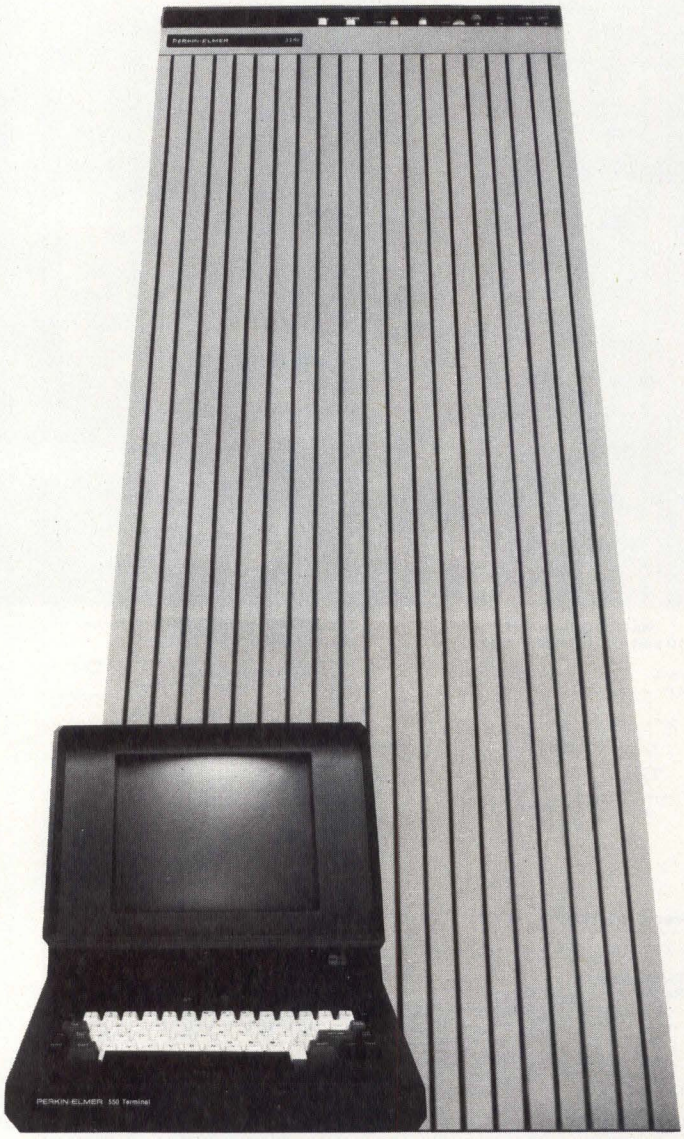

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DESIGN NOTE

Timing Circuit Generates Selectable Clock Frequencies

Four switch selectable clock frequencies with flexibility in width, phase relationship, and cycle time to service a variety of timing applications are generated from a single time base

F. Chitayat Canadian Marconi Company, Montreal, Canada

In the design of a microprocessor based system, it is sometimes inconvenient to use a fixed frequency clock generator, such as that provided by the microprocessor manufacturer, due to the dedicated inflexibility of such a device. Where flexibility is desired, for instance, to accommodate a range of memory speeds while maintaining microprocessor cycle time at an optimum rate, the timing circuit shown in Fig 1 generates several cycle times and corresponding clock signals for the Motorola 68B00 2-MHz microprocessor. This circuit can be readily adapted for use with other microprocessors.

Cycle times are switch selectable among 800, 700, 600, and 500 ns, which correspond to clock frequencies of 1.25, 1.43, 1.67, and 2 MHz, respectively. For each cycle time, the two necessary nonoverlapping clock signals $\phi 1$ and $\phi 2$ are generated for microprocessor input. Each repeating pattern of $\phi 1$ and $\phi 2$ can be lengthened or shortened independently to suit the application. Also, a number of special clock signals—data bus enable (DBE), for example—can be similarly generated.

Principles of Operation

Logic devices U1 and U2—a pair of 74LS175 4-bit registers—connect the output of each internal flipflop to feed the input of the succeeding flipflop, thereby forming a single synchronously clocked 8-bit serial register with complementary outputs. The clock input frequency is 10 MHz. Each successive flipflop output presents a delay of one clock period, or 100 ns, with respect to the preceding output.

To generate the required cycle times, certain flipflop outputs are NANDed by gate U6. When all these outputs are 1s, the output of U6 goes low, thus resetting latch U7 and presenting a 0 input to serial register U1/U2. Then, this register proceeds to successively drop all its outputs to 0s, and the output of NAND gate U5, which is connected to the corresponding complementary outputs of U1/U2, goes low, setting latch U7.

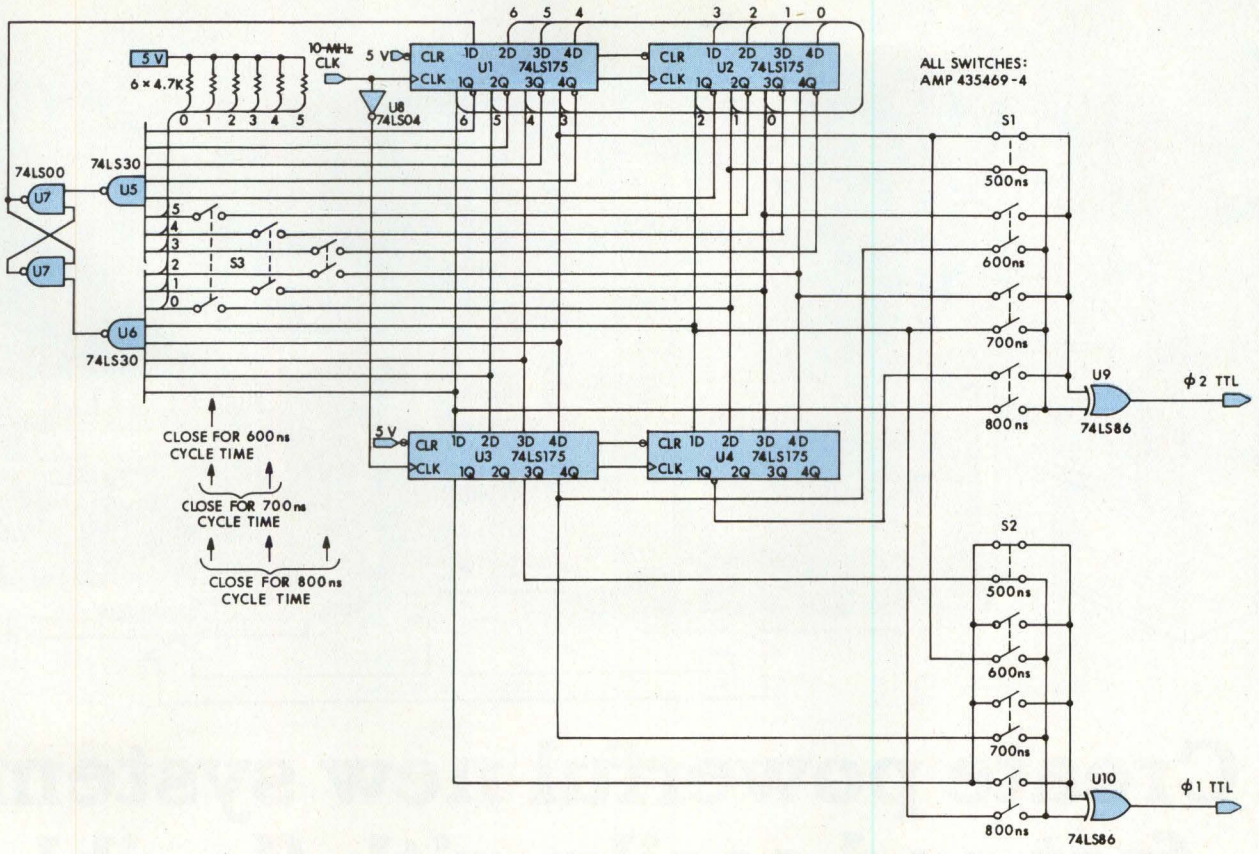

Fig 1 Clock circuit schematic diagram. From single 10-MHz timebase, circuit provides four switch selectable combinations of $\phi 1$ and $\phi 2$ clocks for 6800 microprocessor timing. Four cycle times—500, 600, 700, and 800 ns, are available

Next, this latch presents a 1 input to serial register U1/U2, and the entire operation is similarly repeated.

Only the first five flipflop outputs of U1 and U2 are fed to U5 and U6 to generate a 500-ns cycle time, as each output contributes a 100-ns delay. For an 800-ns cycle time, all eight outputs of U1 and U2 are fed to U5 and U6. Selection of cycle times is made by a multiple-section double-pole single-throw switch (S3 in Fig 1). Poles that are ganged together are shown connected by a dotted line. Pullup resistors—connected to the switched inputs of U5 and U6—provide noise immunity when these gates are opened.

Logic devices U3 and U4 form another pair of 74LS175s whose inputs are connected to the corresponding outputs of U1 and U2, but which are clocked by the negative-going edge of the master clock via inverter U8. Thus, an intermediate 50-ns step delay is provided, and the resolution for signal generation is correspondingly increased to 50 ns.

To generate the desired clock signal, any two outputs and/or complementary outputs of U1, U2, U3, and U4 are selected and exclusively ORed through U9 and/or U10, respectively. As each cycle time requires a different $\phi 1$ and $\phi 2$ clock width, the pair of outputs needed to generate the clock frequency for each cycle time are fed to a double-pole section of switches S1 and S2. Thus, S1 provides the $\phi 2$ clocks necessary for all four cycle times, and switch S2 similarly provides the $\phi 1$ clocks.

A representative timing diagram (Fig 2) for the 500-ns cycle time shows the timing relationships of the various signals. Signal (1) shows the 10-MHz master clock. Signals (2) through (6) show the first five outputs of U1 and U2. Transitions of these signals are coincident with the rising edge of the master clock and are delayed by exactly one clock period, or 100 ns, with respect to each other. Signal (7)—the output of U5 or the $\overline{\text{SET}}$ signal for U7—goes low when signals (2) through (6) are low. Signal (8)—the output of U6 or the $\overline{\text{RESET}}$ signal for U7—goes low when signals (2) through (6) are high.

Signals (9) through (13) represent the first five outputs of U3 and U4. Transitions of these signals occur at the falling edge of the master clock and are delayed by one clock period, or 100 ns, with respect to each other,

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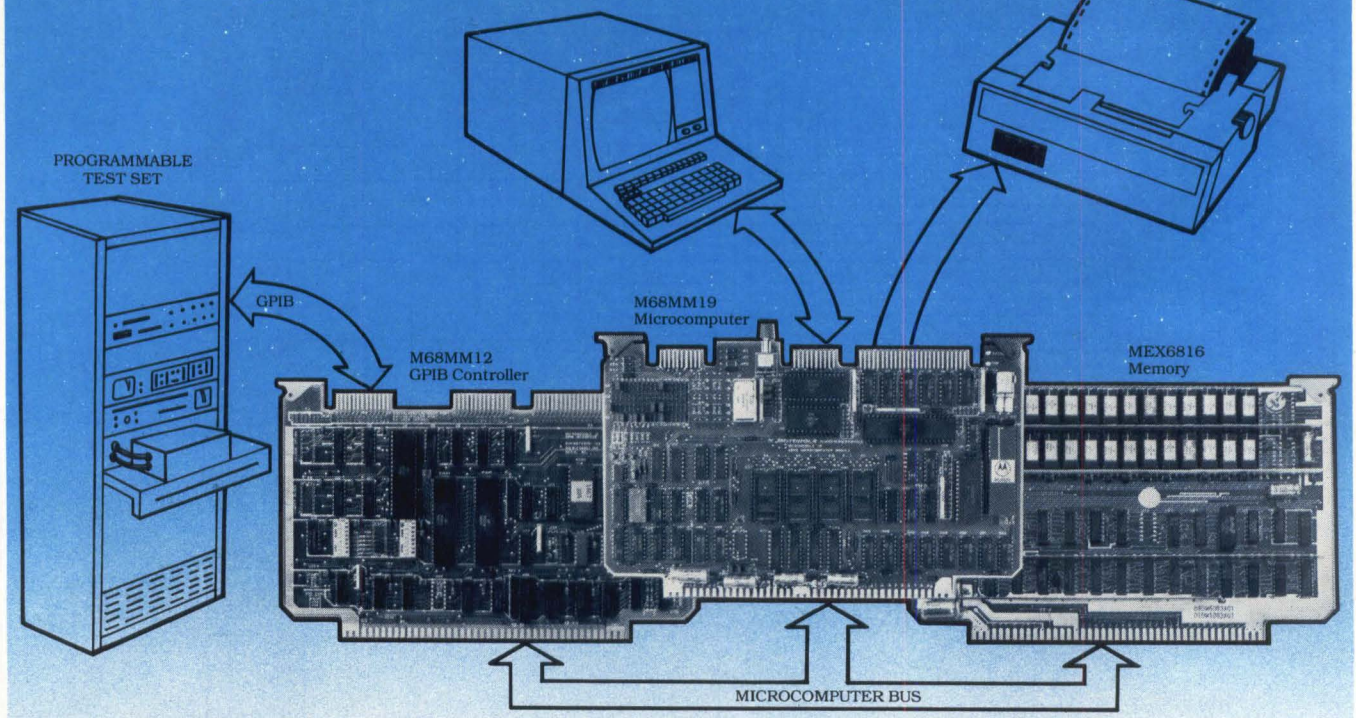

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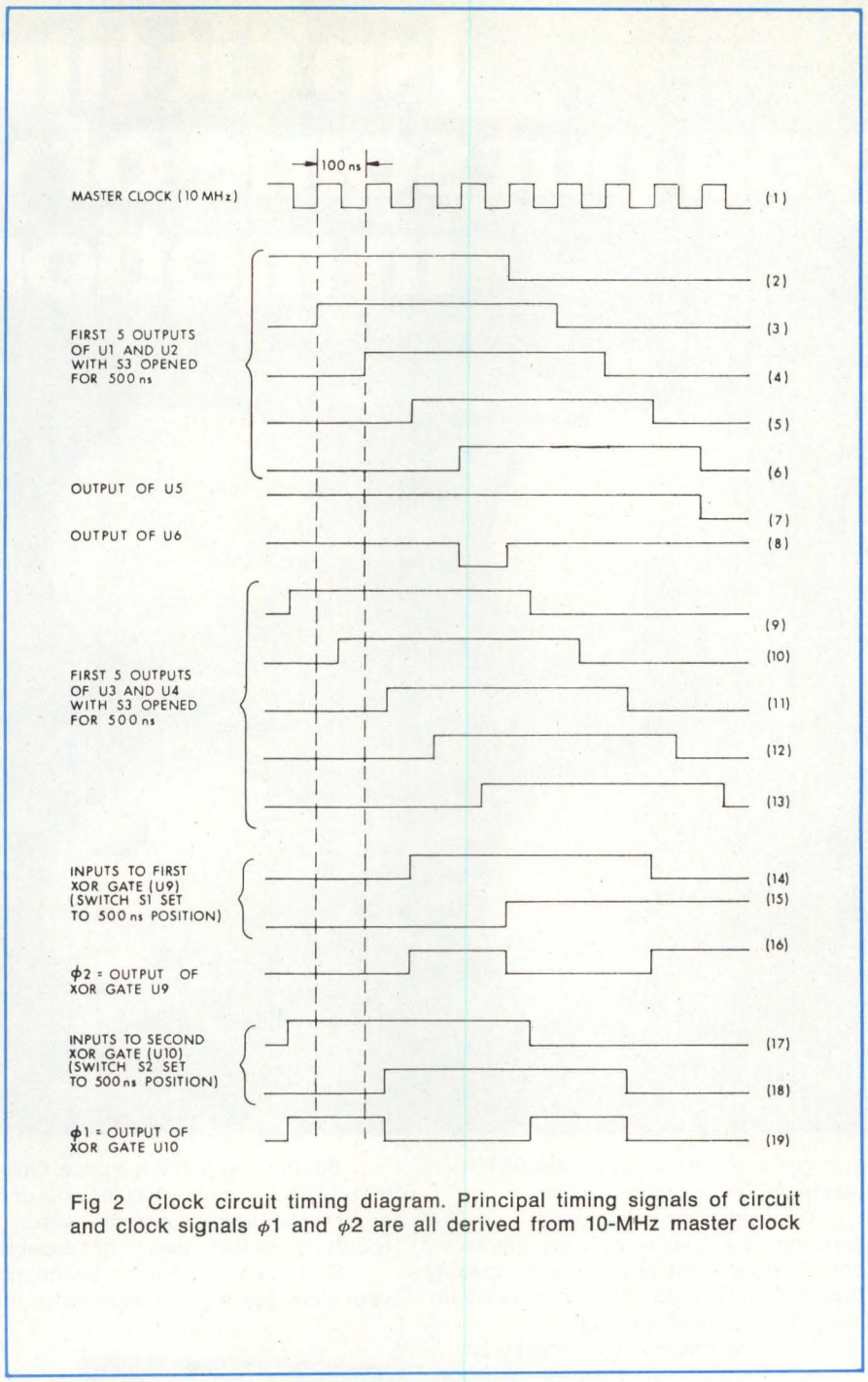

Fig 2 Clock circuit timing diagram. Principal timing signals of circuit and clock signals $\phi 1$ and $\phi 2$ are all derived from 10-MHz master clock

and one-half of a clock period, or 50 ns, with respect to signals (2) through (6), respectively. Signals (14) and (15) are two outputs, which have been selected from among signals (2) through (6) and (9) through (13), to feed the inputs of XOR gate U9, the output of which generates clock $\phi 2$, signal (16). Clock $\phi 2$ is thus 200 ns wide and has a 500-ns period. Signals (17) and (18) similarly feed the inputs to XOR gate U10 to generate clock $\phi 1$, signal (19). Clock $\phi 1$ is thus also 200 ns wide with a 500-ns period, and has a 50-ns nonoverlap zone with $\phi 2$.

Bibliography

C. Bolon, "Decoders Drive Flip-Flops for Clean Multiphase Clock," *Electronics*, Apr 14, 1977, pp 107-109

Motorola, Inc, *M6800 Microcomputer System Design Data Book*, Phoenix, Ariz, 1976

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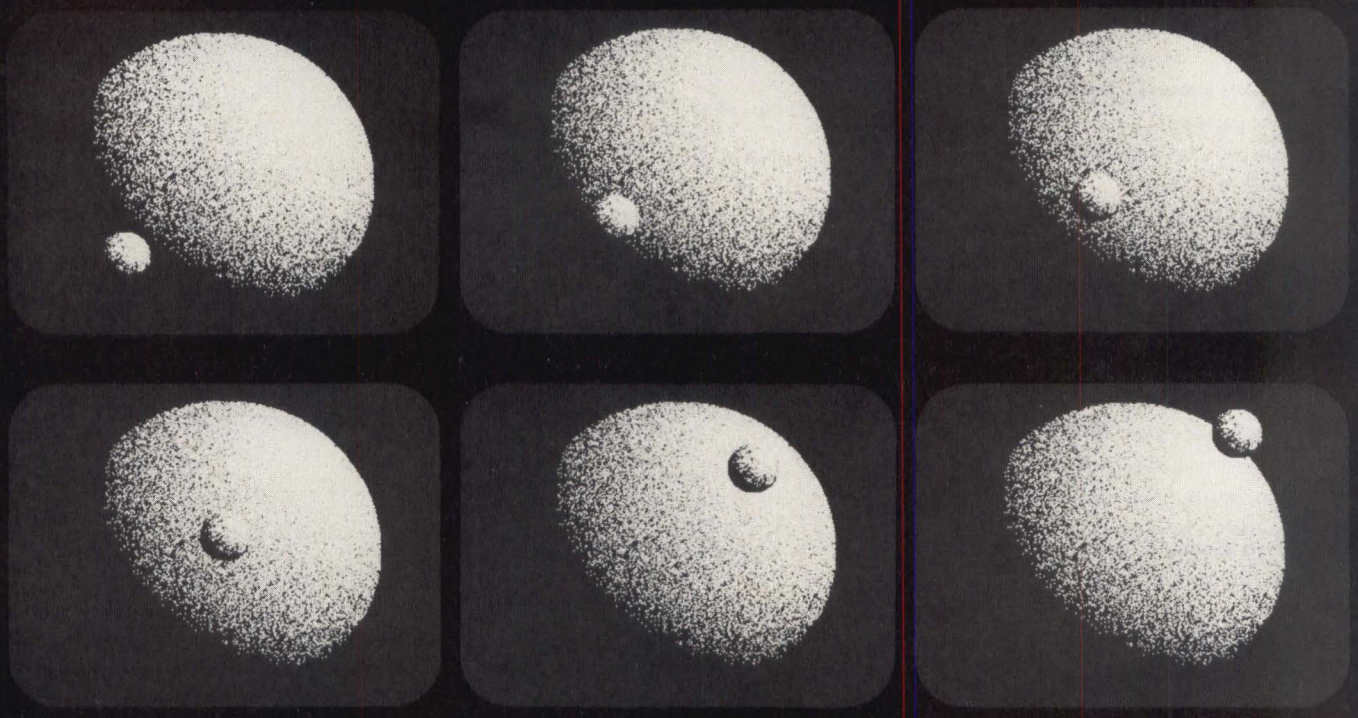

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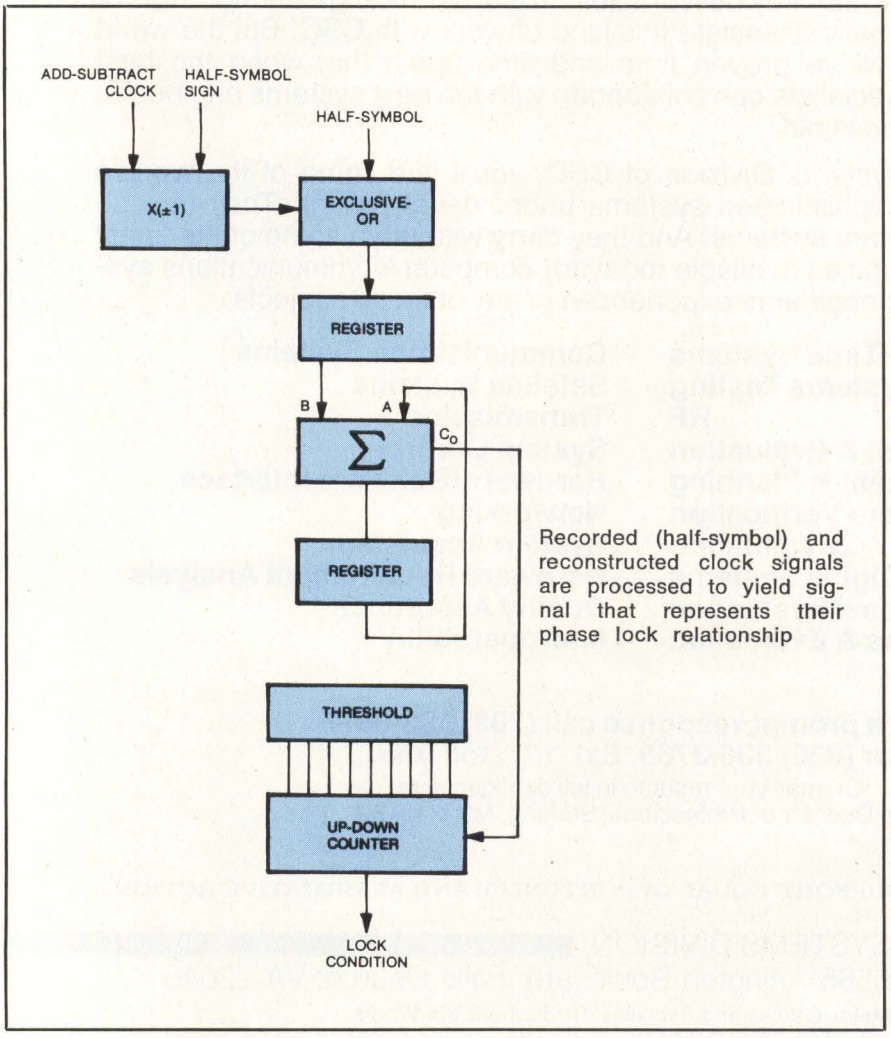
TECH BRIEF

Bit-Synchronizer Lock Detector

Simplified circuit indicates phase error between recorded and reconstructed clock signals



Recorded (half-symbol) and reconstructed clock signals are processed to yield signal that represents their phase lock relationship

A circuit that measures the phase error in a phase locked loop between the clock signal recorded in data on magnetic tape and the reconstructed clock signal presents the error as a digital word that can be compared with a predetermined threshold to indicate lock status.

The lock detector utilizes an early/late algorithm used in a NASA bit-rate synchronizer, but implements it by treating a half bit time as the smallest unit of time of interest (rather than a full bit time). This renders part of the algorithm redundant and unnecessary and reduces the amount of hardware required. In the aerospace application for which it was designed, the detector requires seven fewer integrated circuits and two fewer discrete components.

The circuit operates (see Figure) by taking the absolute value of two in-phase half-symbol integrations, subtracting the sum of the absolute values of two quadrature half-symbol integrations, and then summing over 2^n symbol times (n being the number of symbols). The output is a maximum for either 0° or 180° phase offset between the recorded and reconstructed clocks. It is zero for ±45° offset and a negative maximum for ±90°. The equality of the output for phase locked and 180° out-of-phase clocks is a characteristic of any lock detector operating on a Manchester encoded signal, which uses only half-symbol instead of full-symbol information.

Note

This work was done by Douglas C. Huey and Benedict A. Itri of TRW, Inc, for Johnson Space Center. For further information, write to: John T. Wheeler, Johnson Space Center, Code AT3, Houston, TX 77058.

Patent Status

Inquiries concerning rights for the commercial use of this invention should be addressed to the Patent Counsel, Marvin F. Matthews, Lyndon B. Johnson Space Center, Mail Code: AM, Houston, TX 77058. Refer to MSC-16744.

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Next step in the discussion of the evolution of the Motorola 6800 family, summarized in Fig 1, is the 6801 microcomputer on a chip. This microcomputer is important because of its flexibility. It features software and bus compatibility with the 6800, and expands with 6800 peripherals and memory. For small and dedicated applications, it can function as a single-chip microcomputer with internal, but limited, read/write memory, read only memory, and programmable input/output. Alternatively, it can be expanded to 65k address bytes for large system applications. This adaptability has caused the Swiss government to place an order for 150k 6801 chips to computerize their telephone system, which amounts to approximately one 6801 for every 43 people. In the United States, a special version of the microcomputer is being prepared for General Motors and Ford to use in future automobiles.

Three basic operating modes—single chip, expanded nonmultiplexed, and expanded multiplexed—are user selectable (see Fig 2). Single-chip mode permits the device to function as a standalone microcomputer. The user must supply the power and an external crystal to provide the clock frequency. This mode uses 128 bytes of internal read/write (R/W) memory, 2k bytes of internal read only memory (ROM), three independent programmable 8-bit input/output (I/O) ports, and access to the internal timer and serial communications interface via a 5-bit port. Clearly, this mode of operation suits small dedicated applications found in appliances, toys, games, and simple process control.

Expanded nonmultiplexed mode provides access to the internal data bus and lower eight address lines, thus permitting expansion via the addition of 256 bytes of memory. In this mode, two 8-bit I/O ports are sacrificed; however, one 8-bit I/O port, the internal timer, and the serial communications interface are still available.

Finally, the expanded multiplexed mode provides access to the 8-bit data bus and the 16-bit address bus. This permits memory expansion to as much as 65k bytes. Since the data and address buses are multiplexed, the user still has access to a single 8-bit I/O port, the internal timer, and the serial communications interface. All of these capabilities are achieved from a single 40-pin chip since selection of a particular operating mode configures the individual pins to specific capabilities.

Functions that the microcomputer combines on a single chip—R/W memory, ROM, clock timer, several I/O ports, and serial communications interface—previously required multichip and board-level systems. For example, a compar-

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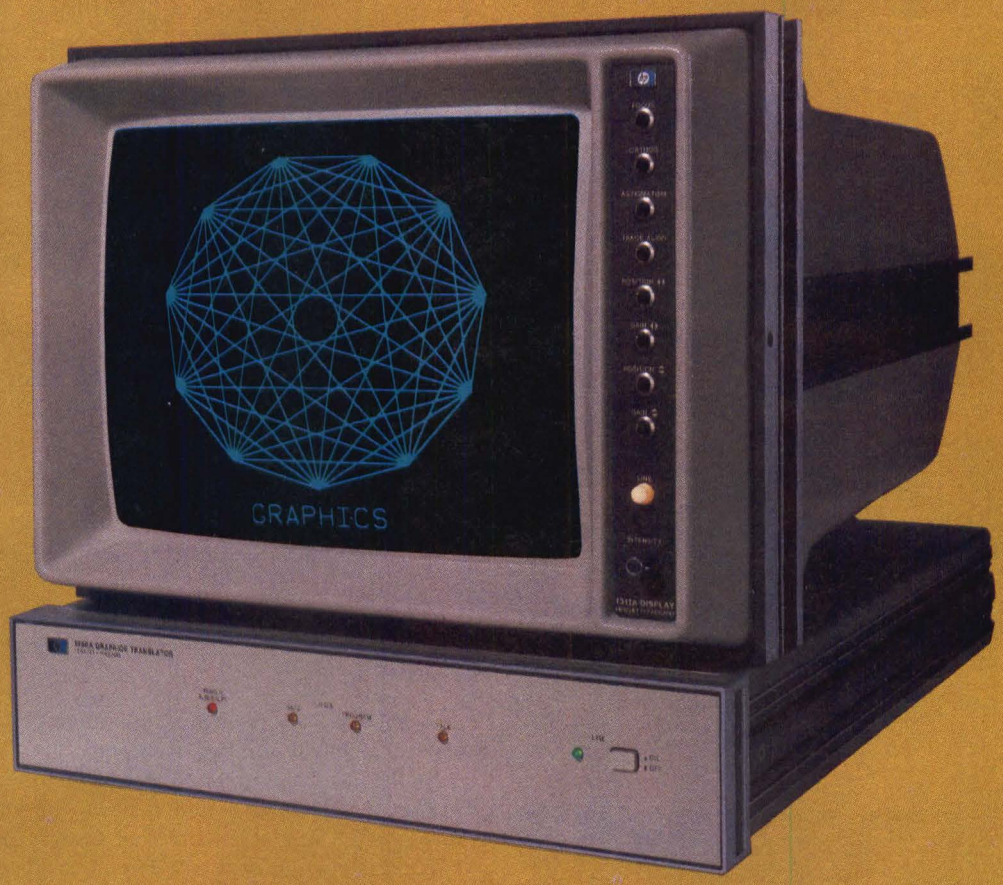

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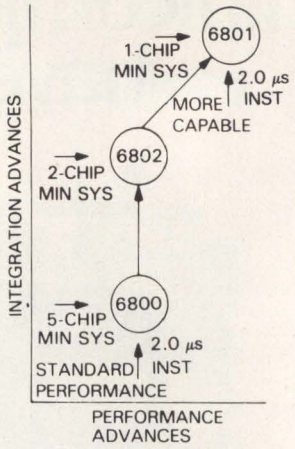
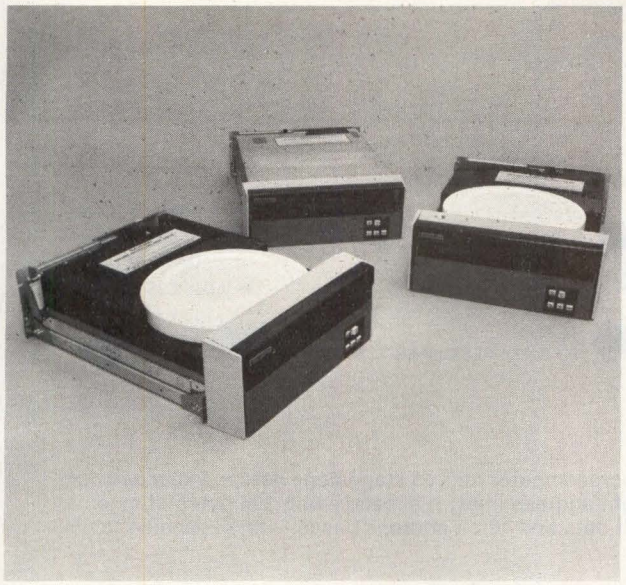


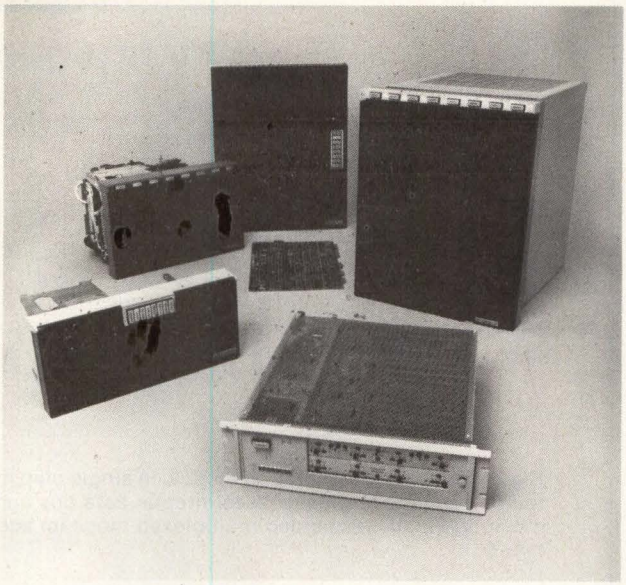
Fig 1 Evolution of 6800 microprocessor/microcomputer family. Advanced microcomputer (6801) progressed from 6802 and 6800 microprocessors; these three require one, two, and five chips, respectively, to configure minimum system

able 6800 based system requires nine chips to provide the same system capabilities as a single 6801 chip.

Specifically, the first 64 bytes of the internal R/W memory can be retained in a power-down, or standby, situation through the use of an external battery, which supplies a maximum current of 8 mA. The internal serial communications interface, or universal asynchronous receiver/transmitter (UART), is capable of full- and/or half-duplex operation in standard mark/space format for typical terminal or modem interfaces, or in bi-phase (fm) format for use between processors. The UART also contains a programmable bit-rate generator to provide four software selectable rates covering a range of from 150 to 76.8k baud, depending upon the crystal used. The internal timer is, in effect, a 16-bit freerunning counter. Programming for one of three timing functions allows the microcomputer to be used in applications that require very accurate time measurement. The oscillator/driver associated with the internal clock requires an external crystal. The clock contains an internal divide by 4 circuit, so that a 4-MHz crystal is used instead of a 1-MHz crystal. Use of an inexpensive 3.58-MHz color-burst crystal can provide an oscillator frequency of 0.895 MHz without seriously sacrificing chip performance. Finally, the 6801 is completely bus compatible with the 6800 family of microprocessors, memories, and programmable peripheral devices.

Architecture of the 6801 is designated in Fig 3; the only difference between its and the 6800's architectures is the addition of 16-bit accumulator D (ACCD) that combines the contents of the two 8-bit accumulators ACCA and ACCB. Eleven instructions have been added to the basic 6800 instruction set to facilitate the use of this new accumulator





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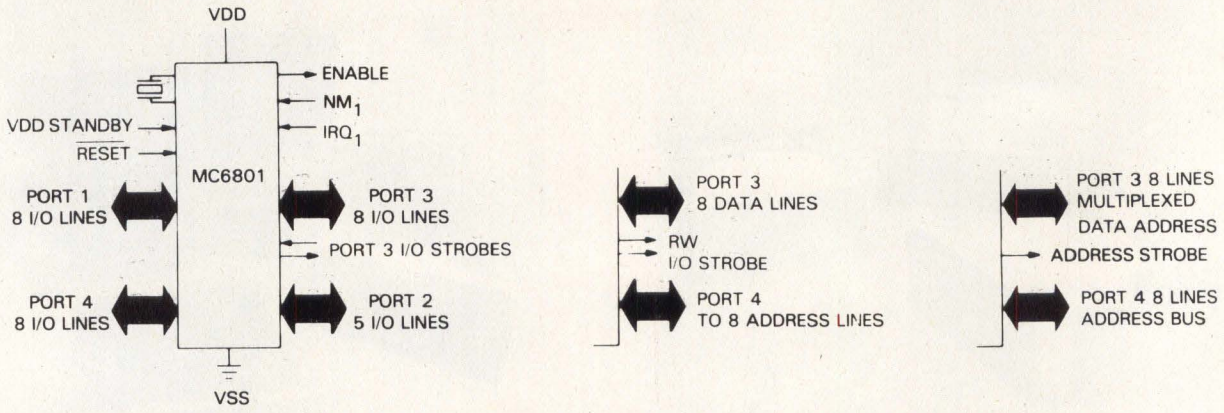

Fig 2 Summary of operating modes. In single-chip mode (a), microcomputer runs as standalone device. Expanded nonmultiplexed mode (b) accesses internal data bus and lower eight address lines; it expands with 256 bytes of external memory. Finally, expanded multiplexed mode (c) accesses 8-bit data and 16-bit address buses, with expansion to 65k bytes

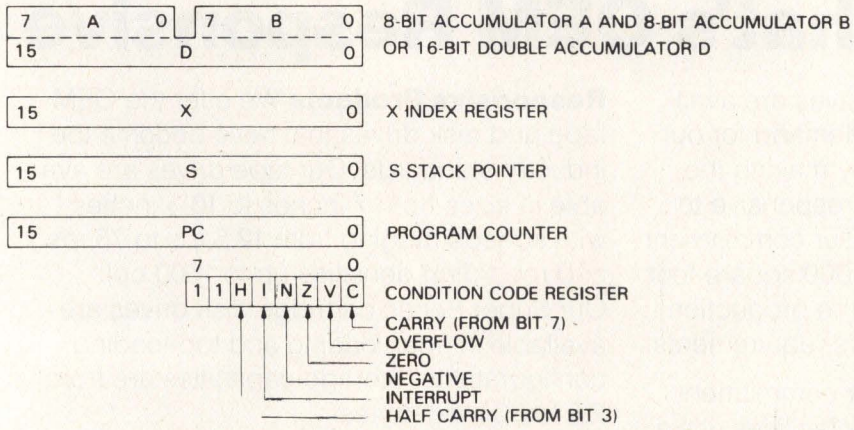

Fig 3 Architecture of 6801 microcomputer. Accumulator D (16 bits) combines contents of 8-bit accumulators A and B. Further, 11 added instructions handle accumulator and optimize use of index register

and to provide greater use of the index register. The instructions are ABX add to index register; ADDD add to accumulator D; ASLD arithmetic shift left, accumulator D; BNO branch never; LDD load accumulator D; LSRD logic shift right, accumulator D; MUL multiply; PSHX push index register; PULX pull index register; STD store accumulator D; and SUBD subtract from accumulator D (the 6800 instruction mnemonics have previously been summarized*). With the exception of BNO, all of these instructions involve 16-bit operations, thus providing for more efficient program execution. In addition, the instruction cycle times of the most often used 6800 instructions have been reduced to provide faster execution of a 6801 program.

As a final point, the 6801 is available in two other forms: the 6803, which is simply a nonROM version, and the 68701, which is an erasable programmable ROM (EPROM) version. The 2048-byte EPROM of the 68701 can actually be programmed with the aid of the internal R/W memory on the chip.

*A. C. Staugaard, *et al*, "Interfacing Fundamentals: The 6800 Instruction Set," *Computer Design*, Sept 79, pp 142, 144, and 146

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

Assembled Development Board Utilizes 1M-Bit Magnetic Bubble Memory

A 7110 bubble memory module, an 8085A based controller, and standard components comprise the 128k-byte development board. The single 6.75 x 12" (17 x 30-cm) SBC board interfaces with MULTIBUS™ systems; it plugs into Intellec® Series II microcomputer development systems and can be used with the ISIS-II operating system. All address, data, and control signals are TTL and MULTIBUS compatible.

IMB-100 uses transparent redundancy inherent in the 7110 bubble memory (see *Computer Design*, July 79, pp 159, 161). Nominal data rate is 68k bits/s. The device is mounted in a socket to facilitate system checkout before applying power. Operation is from 0 to 50 °C over ±12- and 5-Vdc power supplies.

CPU communication with an 8085A is through a set of registers on the board via I/O commands. The microprocessor interprets these registers and controls timing and analog circuits to perform bubble memory accesses. I/O commands also pass data via an onboard FIFO.

Software programs for exercising the development board are contained on a double-density diskette (single-density is optional). Intel Magnetics, 3000 Oakmead Village Dr, Santa Clara, CA 95051, has included six programs to transfer data between an internal RAM buffer and either a standard ISIS-II device and file, or the bubble memory.

Circle 410 on Inquiry Card

Adaptable System Monitor Operates Standalone Computer/CPU

Dual-purpose SBC/9™ is a 6809 CPU for use as an upgrade card in ss-50 bus microcomputers or as a standalone control computer. Also included on the board are 1k of RAM, 110- to 19.2k-baud clock generator, and full-duplex RS-232-C serial interface. An operating system has also been developed by Percom Data Company, Inc, 211 N Kirby, Garland, TX 75042, in five 1k ROM (2708) versions. The board's circuitry accommodates either two 2708 ROMs or one 2716 ROM.

The card provides for multi-address, 8-bit bidirectional data lines to interface directly to offcard I/O devices such as a keyboard. The data bus features multilevel data bus decoding that allows multiprocessing and bus multiplexing of other bus masters under control of a single executive program.

Extended address line capability accommodates up to 16M bytes of memory. All address, control, and data lines are fully buffered.

PSYMON™, the system monitor, includes 15 callable utilities and 8 single-letter, monitor-type commands. It adapts to any hardware environment because interfacing is accomplished with simple, specific device driver routines.

These routines reference a table of parameters called a device control block (DCB), which is independent of the operating system. Receiving control, usually from the 6809 power-on vector, the system initializes its RAM area, configures its console, and "looks ahead" for a second ROM. If present, the ROM may contain user written routines that alter the pointers and enhance or modify the commands.

Circle 411 on Inquiry Card

System Structure Houses All Necessary Elements On One Board

Design philosophy behind the Z80 based VP computer systems maximizes use of LSI circuitry and simple, direct bus structures to eliminate the need for external components such as card cages, multiple boards, and power supplies. All normal system elements are on a single board. This covers 64k of RAM and 1k to 8k of EPROM or ROM; two serial channels using SDLC, HDLC, RS-232, or any protocol, with dual programmable baud rate generators; four programmable counters/timers; and 40 bidirectional I/O latched and buffered parallel lines.

In addition, Data World, Inc, 7541 Ravensridge Dr, St Louis, MO 63119, has supplied a 2-phase clock with 5- and 12-V drivers, clock and calendar with battery backup, five programmable timers, and a 4-channel DMA controller. A programmable video generator has separate or composite video and programmable characters and fields. A subminiature disc control system handles up to eight floppy discs or Winchester drives. An unregulated transformer-rectifier or battery supplies power. Expansion area accommodates any added equipment.

Choice of a multidisc, CP/M compatible operating system includes CP/M, OASIS, SOS, TEMPOS, and CDOS. A variety of BASIC interpreters, as well as APL are available, along with DISK BASIC, COBOL, FORTRAN, Pascal, OPUS, Basic-E, and C BASIC compilers. Assemblers and macro assemblers are suited to the 8080 and Z80. Utilities consist of copy files, linker loader, Z80 and 8080 disassemblers, file editor, memory test, program relocator, and dynamic debug.

Circle 412 on Inquiry Card

Controller Emulates Hardware and Software Of Eight Disc Systems

Flexible diskette controller ZX-4DD interfaces one to four full-sized or miniature disc drives to the Intel MULTIBUS™. Software costs are reduced because the interface is functionally identical to the standard disc systems used in the MDS. The controller is a bus master with full master capability for override and DMA data transfer.

Firmware on the controller allows emulation of SBC-201, -202, -211, and -212, as well as MDS-2DS, -DDS, -710, and -720. Program jumpers select full or mini size, single-density IBM 3740 fm or double-density IBM System 34 mfm format.

The 201 mode of operation sets the controller for direct, media compatible running of single-density disc

With Raytheon new Beam-Penetration Color CRT's. Designed specifically for computer color-graphic system applications, Raytheon Beam-Penetration Color CRT's offer better color resolution and better overall system performance than conventional color tubes and other beam penetration CRT's.

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CIRCLE 49 ON INQUIRY CARD

operating systems; the 202 mode allows execution of double-density disc operating systems after conversion of media data to mfm recording. Intel ISIS-II (DD) systems which are recorded in m²fm can be converted using instructions provided by Zendex Corp, 6398 Dougherty Rd #32, Dublin, CA 94566.

An 8085A CPU performs intelligent disc control and data manipulation; an NEC UPD 765 controller provides for up to four double-sided, double-density drives. The 201/202 emulation program contained in the socketed 8355/8755A type ROM/EPROM may be replaced by a custom program.

Using one card slot, the intelligent controller requires 5 V only, and can be operated from the system's logic supply. A hardware user's manual accompanies the unit. Software driver routines for the 8080/8085 host CPU are provided as hardcopy listings, so that previously written or currently available software for the Intel development systems can be run.
Circle 413 on Inquiry Card

Microcomputer Systems Operate In Industrial Environments

Three RacPac industrial computers consist of two host/development computer systems and a target/remote computer, all usable with equipment that is to be mounted in standard 19" (48-cm) racks or sealed in NEMA 12 cabinets with integral 19" (48-cm) racks. OEMs and systems integrators can employ the systems for process monitoring and control, industrial equipment control, and testing procedures in rugged environments.

The 3900A is a Flexibus II based, 12-slot, rackmounted, host/development microcomputer with modular expansion. It consists of a dual-floppy disc assembly and CPU, in addition to 4k bytes of bootstrap EPROM, 60k bytes of RAM, and interfaces to an optional CRT, printer, and EPROM burner.

The other host/development system that Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176, has introduced is a SuperBoard based microcomputer with a CPU and integral 12" (30-cm) CRT, full function keyboard, and rackmounted dual-diskette assembly. The 3905A RacPac features 98k of RAM, 4k of bootstrap EPROM, interfaces for an optional printer, EPROM programmer, and a 20-mA upload/download serial channel. Three serial channels can be added.

Similar software for the two systems are single-user diskette BASIC, PascalPac operating system, and SPDS. The latter provides editors, assemblers, linkers, FORTRAN compiler, and runtime libraries for all three systems; for target/remote program development, the SPDS offers full up/download capability. As a freestanding application system, the 3900A may be equipped with integral BASIC, FORTRAN, and Pascal capabilities.

The third RacPac unit is also a SuperBoard based microcomputer packaged with a CPU, integral 12" (30-cm) CRT, power supply, 16k dynamic RAM, sockets for up to 8k of EPROM, one serial I/O channel, a CRT controller, and keyboard. The 3945A system is configured at the time of purchase with a few field installable options; it may be ordered with added memory, serial channels, floppy disc controller, and parallel interfaces. EPROM based SpurCom software package features virtual console functions via the CRT and keyboard, and built-in debug capability. It also provides I/O drivers for the FORTRAN runtime library.
Circle 414 on Inquiry Card

High Powered μComputer Systems Package Disc Storage With Processor

Performance and functionality of midrange minicomputers have been transferred to the microcomputer level in the form of two PDP-11/23 based systems. Execution speeds of both are two and one-half times that of the entry level PDP-11/03 systems. Thus, the systems from Digital Equipment Corp, Maynard, MA 01754, are suited to OEM and end user applications in engineering, scientific, and commercial environments.

PDP-11V23 is housed in a 30" (76-cm) high cabinet. A standard configuration includes two RX02 floppy disc drives, a PDP-11/23 with 128k bytes of memory (expandable to 256k bytes), and either hardcopy or video terminal. A workstation desktop attachment is optional. The RT-11 operating system, programming language compilers such as ANSI standard FORTRAN IV and BASIC, editors, and utilities comprise the software.

A 40" (102-cm) high enclosure houses the PDP-11T23, consisting of the processor and two RL01 hard discs, as well as the choice of hardcopy or video terminals. In addition to the software of the -11V23, this system runs under the RSX-11M multiuser, multitasking operating system, allowing more powerful compilers such as BASIC-PLUS-2, FORTRAN IV-PLUS, and PDP-11 COBOL. The result is increased analytical power and performance.
Circle 415 on Inquiry Card

Hardware Modules Implement Interfaces To IEEE STD 488 Bus

Micromodules™ 12 and 12A are monoboard systems that create an interface between a microprocessor and one or more test instruments according to the IEEE STD 488-1978 bus specification. The units are bus compatible with the full Micromodule family and M6800 EXORciser™ development systems (when run at 1 MHz), all of which are available from Motorola Microsystems, PO Box 20912, Phoenix, AZ 85036.

M68MM12A allows the user's system to send/receive data bytes, request service, and respond to parallel and serial polls. This provides the listener/talker function only. With all of these same capabilities, M68MM12 further adds the controller function—the ability to send commands and conduct parallel/serial polls. It has onboard EPROM contain-

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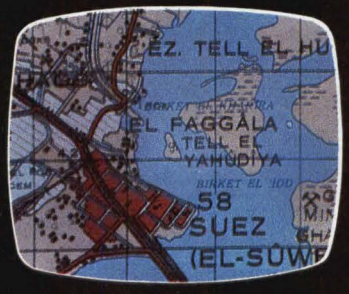

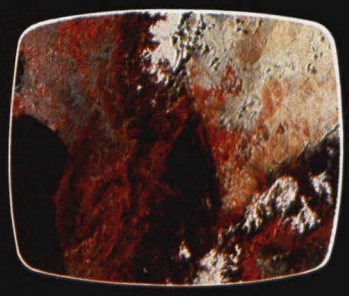

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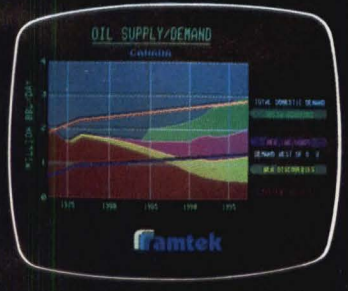

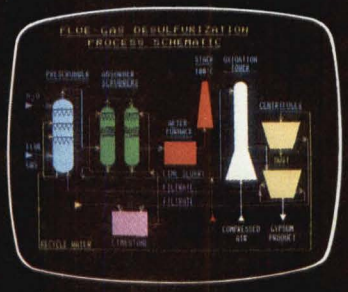

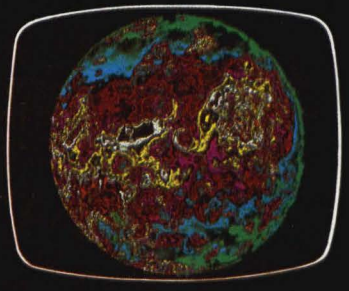

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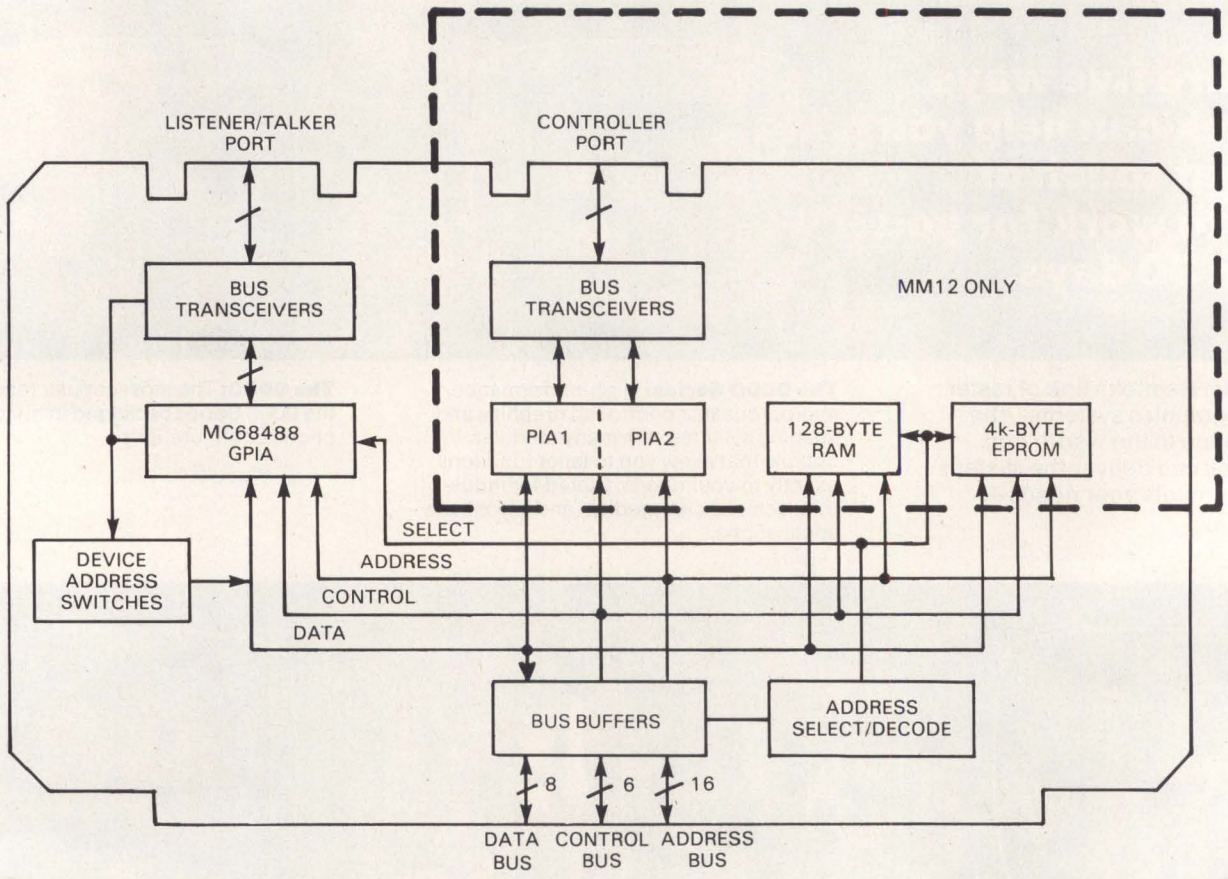
CIRCLE 57 ON INQUIRY CARD



GPIB Micromodules. Identical sections of Motorola's 12 and 12A units are shown, with added parts of MM12 enclosed in dotted lines. Hardware, supported by optional M6800 software routines, implements interface to IEEE STD 488 for use with Micromodule based systems

ing all interface firmware, and RAM for use as a message table and scratchpad area.

Mutual hardware features are 1-MHz operation, capability for generating interrupts to speed up GPIB operation, and onboard switches for selection of device address. The onboard hardware meets all IEEE STD 488-1978 signal level requirements and timing requirements without the need for microprocessor interrupts. Address and control bus is TTL voltage compatible and the data bus is 3-state TTL voltage compatible.

Power requirements are 5 V at 1.4 A max. The 9.75 x 6.15 x 0.50" (24.77 x 15.62 x 1.27-cm) module operates from 0 to 70 °C. GPIB data rate is 50k bytes/s max guaranteed, with rates up to 1M bytes/s possible.

Supporting software to implement the bus protocol is provided on the MDOS diskette: M68MM12SWM for Micromodule 12 and M68MM12ASWM for Micromodule 12A. The former provides the source code for the firmware EPROM, which is used to implement the GPIB protocol and may be modified using the software. The latter software implements the protocol for the GPIB listener/talker interface; it contains source code for a demonstration program and for the communication protocol using a local message table. Both packages include a training program on how to use the communication protocol.

"Device driver" software allows the user to send messages to and receive them from the interface without getting involved in bus protocol. The user is free to configure the system since interrupts are not required.

Circle 416 on Inquiry Card

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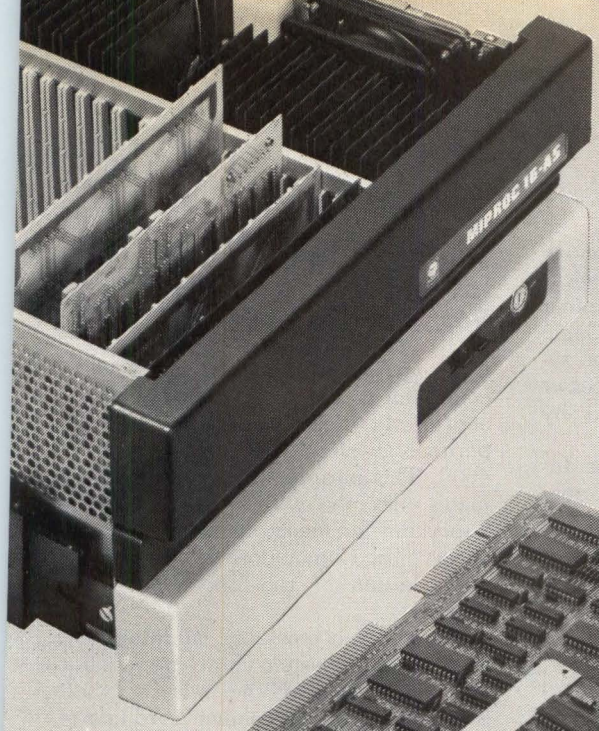

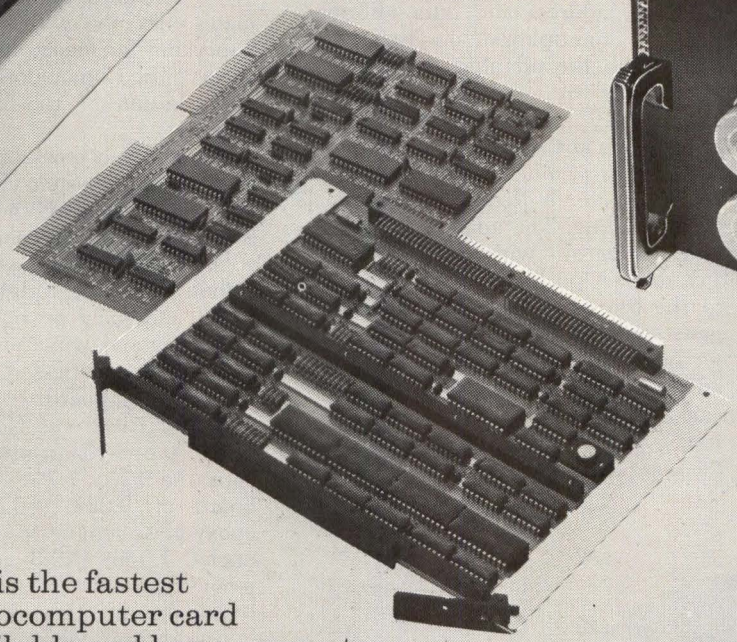

Miproc-16 is the fastest 16-bit microcomputer card family available and has a compute-rate of 4 million instructions per second.

INSTRUCTION POWER Up to 170 instructions including multiply/divide and bit manipulation give Miproc-16 formidable processing capability.

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SOFTWARE POWER Easy to use cross-assemblers for mainframe or mini-computer make programming faster, *and* PL-MIPROC, a super-efficient high level assembly language. And soon a disk-operating system with PASCAL.

HARDWARE POWER Comprehensive range of processor, memory and interface cards backed up by sophisticated hardware development aids.

RUGGEDIZED POWER Miproc can be configured to meet any known military specification.

Miproc-16 can be brought into action in your application, in either a standard commercial format or a full military conduction-cooled board system.

The commercial application system *(above left)* has room for three Miproc CPUs, is smartly styled and equipped with add-in 13- or 20-slot card bay modules, fans and power supply.

The military system, contained in a 1-ATR size chassis *(above right)* provides up to 3.6 million instructions per second with conduction-cooling, compliance with MIL-E specifications and an unmatched cost-to-performance ratio.

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CIRCLE 58 ON INQUIRY CARD

Adapter/Logic Analyzer Team Handles Most 8-Bit μProcessor Applications

An 8-bit microprocessor analysis system for such processors as the Intel 8080 and 8085, Zilog Z80, Motorola 6800, MOS Technology 6502, and RCA 1802 is formed through the combination of the model 2710 logic analyzer and the 2710 MPU adapter, introduced by Gould Inc, Biomation Div, 4600 Old Ironsides Dr, Santa Clara, CA 95050. This allows the analyzer (see *Computer Design*, Jan 79, p 48) to be applied to many microprocessors without losing its performance characteristics.

The system's universality is enhanced by the adapter's AND/OR clocking and common address/data bus demultiplexing features. The former provides easy clocking, recording, and simultaneous display of address and data information that are read or written at different times.

The adapter pod provides four clock signals for switch selectable OR clocking of data recordings; any combination of these signals can form a single master clock signal. Complete or selective recordings of microprocessor program execution are obtained by changing switches.

In microcomputers such as the Intel 8085, address and data information are multiplexed on the same pins. With the adapter, therefore, it is possible to demultiplex, record, and display both data and address information at the same time.

All signals going through the adapter pod are buffered for minimal signal loading. The adapter loads systems under test with one low power TTL gate. A pushbutton switch added to the top panel and several unused gates and buffers built into the pod's PC board allow customization of the adapter by the user. Open board space can be used to add gates or other circuitry.

Circle 417 on Inquiry Card

Universal microprocessor adapter (left) connects to Biomation's 2710 Data Domain Analyzer (right) to analyze 8-bit microprocessors, using added features of AND/OR clocking and common address/data bus demultiplexing

Low Cost Boards Ease Interface Construction For Microcomputers

Users may construct special control, communications, peripheral, or memory interface circuits, as well as experimental circuits, with the model 4609. This peripheral interface board mates directly with Apple II and Superkim microcomputers, and connects to the Commodore PET unit with the addition of the Expandamem™ adapter.

Three connectors, in addition to the standard system bus, are available for I/O. On the rear of the board is a 20/40-contact card-edge connector that mates with a 3M type ribbon connector; a right-angle solder-tail header may be positioned in the same location. Miniature SIP type connectors may be placed on the periphery or in mid-board.

Vector Electronic Co, 12460 Gladstone Ave, Sylmar, CA 91342, fabricates the 2.75 x 7.7" (6.99 x 19.6-cm) board of 0.062" (0.157-cm) thick epoxy-glass-composite material. An unclad 1.9-in² (12.3-cm²) area holds mounting relays, switches, indicators, terminals, or other discrete devices.

DIPS or DIP sockets of 14 to 40 pins mount in 0.042" (0.107-cm) diameter holes located on 0.1" (0.3-cm) centers. At each DIP pin position are 2-hole pads; the first allows tack soldering for component mounting, while the second accommodates wrapped wire pins or three 26-gauge wires for interconnections. Wrapped wire or soldered power connections are made with the heavy duty buses on the wiring side; a third unconnected bus is located on the component side for the designer's use.

Circle 418 on Inquiry Card

Dedicated Microprocessors Speed Operation of Compact Microcomputer

Advanced design of the compact WH89 microcomputer requires minimum space to produce all the functions necessary for small business or professional tasks. Heath Data Systems, PO Box 167, St Joseph, MI

49085, developed the 8-bit system around the WH19 video terminal. Two Z80 microprocessors, a 72-key keyboard with 12-key numeric pad, and 16k of RAM were added to this component. The final addition was a floppy disc system built into the right front area of the terminal for high speed access and mass storage capacity of 100k bytes/disc for programs and data.

Separate microprocessors for the video terminal and microcomputer itself assure that the two units never share processor power. Broadening system capabilities, this configuration also increases operation speeds and eases operator control.

The 12" (30-cm) diagonal CRT features a wide bandwidth monitor that produces sharp 0.2" (0.5-cm) high characters in a 5 x 7 (upper case) or 5 x 9 (lower case with descenders) dot matrix on the P4 phosphor screen. Display format is 25 lines of 80 characters. Graphics characters use an 8 x 10 dot matrix. Display size is 6.5" (16.5-cm) high by 8.5" (21.6-cm) wide.

Users can control terminal functions from the keyboard or with software. Eight user definable keys allow programming of special functions. Characters and lines are inserted to and deleted from anywhere on the screen through direct cursor addressing. Line graphics capability from the keyboard or computer is also featured. Keyboard selectable baud rates range up to 9600.

The single-drive floppy disc system stores 100k bytes on the 5.25" (13.34-cm) diskette. Specs include a 30-cm max track-step time and typical random sector access time of less than 250 ms.

Weighing 50 lb (23 kg), the single-unit system measures 13 x 17 x 20" (33 x 43 x 51 cm). Suggested list price is $2295. It requires 120/240 V at 50/60 Hz, 90 W maximum.

Accessory 2-port serial I/O interfaces communicate with printers or timeshare systems via a modem. All communication is EIA RS-232 standard. Two additional chip sets expand RAM to full capacity of 48k.

The operating systems software package consists of extended Benton Harbor BASIC, a 2-pass absolute assembler, text editor to prepare source code for BASIC and other languages, console debugger, and a set of disc utility programs for file manipulation. Dynamic file allocation efficiently uses available space; a special feature permits copying and transferring between discs in a single-drive system. Programs written in Microsoft™ BASIC and assembler may be run.

Circle 419 on Inquiry Card

Integrated 8-bit microcomputer. Heath WH89 (with cover removed) contains keyboard, numeric keypad, floppy disc system (right front area), WH19 video terminal, 16k of RAM, and two Z80 microprocessors, all of which combine to handle high speed data processing tasks

Graphics Entry Tablet Capitalizes On μComputer's High Resolution Color

The Graphic Tablet attaches to any Apple II computer, Apple Disk II, and TV set or monitor to supply graphics input capabilities. Connection of the computer to a printer provides a hard copy of the graphics. Among the graphics operations are freehand drawing, creating original art, digitizing and modifying drawings, tracing an existing design, and producing color separations by creating a multicolored illustration and stripping out the individual colors. Six colors used are black, white, magenta, green, orange, and blue. The tablet processes 100 points/s, with virtually no time lag between a pen motion on the tablet and a result on the screen.

Elements of the tablet are an 11 x 11" (28 x 28-cm) drawing surface, coated mylar overlay with menu of tablet functions, stylus, disc based software, and PC interface card. The plug-in interface card contains 2k bytes of ROM firmware to handle hardware and software utility functions, thereby saving programming time.

Functions that Apple Computer, Inc, 10260 Bandley Dr, Cupertino, CA 95051, has incorporated include Pen Color, Draw, Frame, Box, Line, Dot, Window, Distance, Area, and Clear. In addition, Calibrate maps a portion of the tablet to the full size of the monitor screen for enlarging. A section of an image can be chosen with the Viewport function; this area can be modified while protecting the rest of the image. Then, the Reduce function is implemented to use the entire surface to work on the sectioned area.

To select a function, the user touches the stylus to the appropriate label on the overlay. To change the function, the user touches the stylus to the next selected function. Applesoft BASIC software routines give the option of modifying the functions to user needs. These may alter, eliminate, or add such functions as standard shapes, symbols, or colors.

Circle 420 on Inquiry Card

ROM Simulator Causes Microcomputer To Act As Graphics Terminal

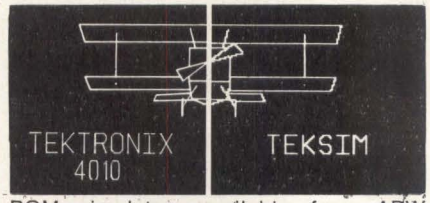
An advanced programming technique of distributed processing, together with the plotting resolution of the Apple II computer enables TEKSIM to offer an affordable graphics display alternative. The Apple II/Tektronix 4010 simulator ROM permits the Apple computer to operate as a graphics terminal when connected to a host computer. No modifications to the host resident program are necessary to display or input graphical data.

Simulation is of the Tektronix 4010 series terminals. All characteristics of the 4006 and 4010 are precisely simu-

lated; for the 4012 and 4014, all features except lower case/variable size characters and enhanced graphics are emulated. Graphical resolution of the Apple is 280 x 192 as compared to 1024 x 1024 for the Tektronix terminal, so that TEKSIM can never produce as good an image as that of the Tektronix unit (see Figure). However, the quality is sufficient for many applications where cost factors are involved.

Basic features allow the user to display graphical output from a program residing on a host computer, to send graphical input to a host using game paddles or a joystick, and to issue local commands for erasing the screen, returning to the Apple monitor, and sending a break signal. Minor changes to the host-resident program produce 6-color graphics displays. The standard video output lets any TV set function as a monitor.

The ROM chip and special Apple adapter unit, marketed by ABW Corp, PO Box M 1047, Ann Arbor, MI 48106, plug into the D8 socket inside the computer. The simulator also requires an Apple communications interface card for communicating with a host computer. ROM supports operation with Apply's Disk II, so that screen images can be saved while online, and recalled later in an offline environment. Disc based application packages under development will support various graphics tablets and plotters which operate with Apple's I/O capabilities.



ROM simulator, available from ABW Corp, causes Apple's microcomputer to act as graphics display, simulating Tektronix 4010 series terminals. Comparison demonstrates differences in quality due to resolutions; TEKSIM image (on right) is acceptable in many applications that have cost restrictions

Circle 421 on Inquiry Card

Battery Power Backs Up Microcomputer MOS Memory And Refresh Logic

UPS-2708A, an uninterruptible dc power system rated between 5 and 50 W, can power Digital Equipment Corp's LSI-11 MOS memory (MSV11) and refresh logic, independent of the computer's main power supply. Normal mode is ac line/dc regulated 5 and 12 Vdc that automatically transfers without interruption to the hold mode, which offers dc-dc regulated 5- and 12-Vdc battery backup power in the event of an ac line power outage.

The 8.75" (22.23-cm) high rack panel package consists of four primary subassembly modules: an ac/dc linear conversion subassembly, 40-W battery charger, 5- and 12-V output converter module assembly, and battery protection cutout relay assembly. The 12-Vdc sealed lead-acid battery is neither orientation sensitive nor prone to leakage. Minimal outgassing rapidly dissipates into a free air environment. Battery float life is greater than 8 years. A cut out relay protects the battery from damaging discharges by disconnecting it from the system at a preset level until ac line power is restored.

The system, offered by Stevens-Arnold, Inc, 7 Elkins St, S Boston, MA 02127, provides three outputs: 5 Vdc ±0.5% at 3 A, 12 Vdc ±0.5% at 1 A, and 14.1 Vdc at 3 A (for the battery charger). Output noise and ripple are 20 mV pk-pk. Overvoltage and short circuit protection are included. Other specs are tempco of ±0.01% max/°C, voltage stability of ±0.1% max/24 h, and ambient operating temperature of 0 to 60 °C.

Circle 422 on Inquiry Card

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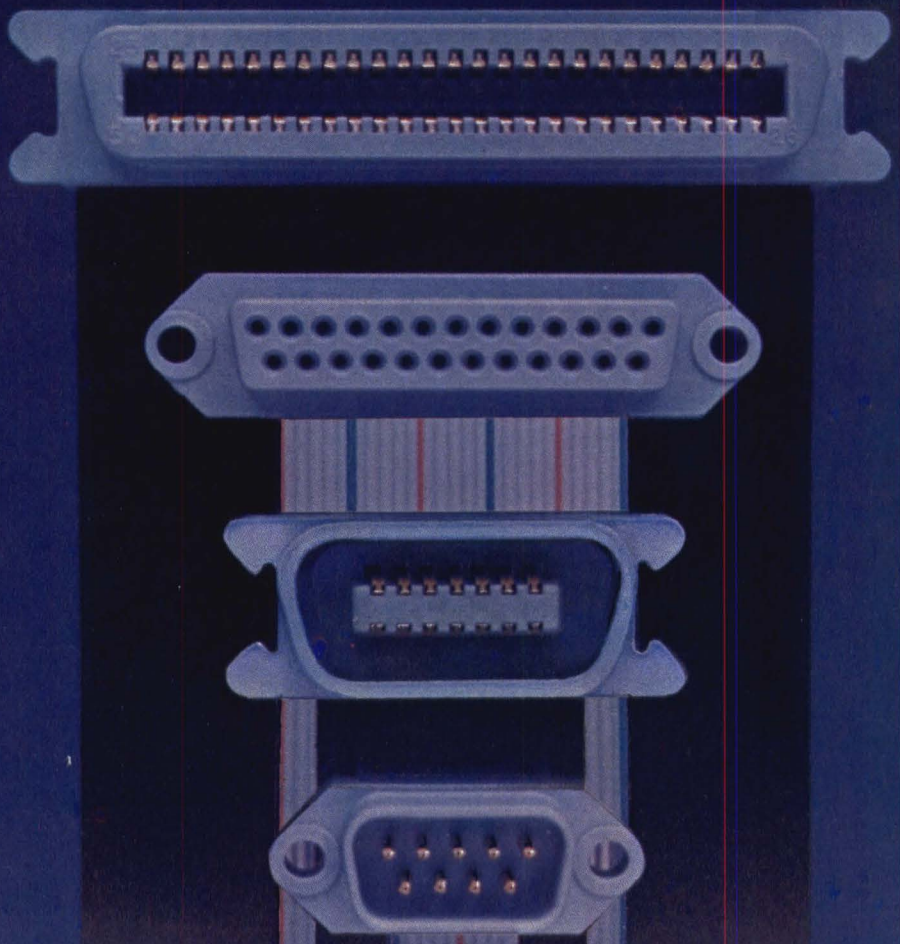

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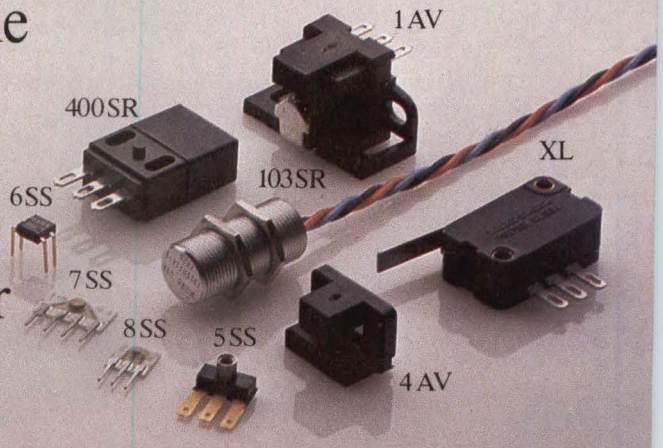

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MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

SOFTWARE

C Compiler Produces Faster Code Than Pascal, With Extensive Facilities

A full C compiler, operating on 8080, 8085, and Z80 computers under CP/M, has 75 functions for performing formatted or direct I/O, string manipulations, and storage allocation in a machine independent manner. The code is faster than that of Pascal. Compiler output is in A-Natural source, translatable to Microsoft MACRO-80 assembler source. The CP/M package complements the PDP-11 based C Compiler and 8080 cross compilers already released by Whitesmiths, Ltd, 127 E 59th St, New York, NY 10022, for use under RT-11, RSX-11M, RSTS/E, IAS, and UNIX.

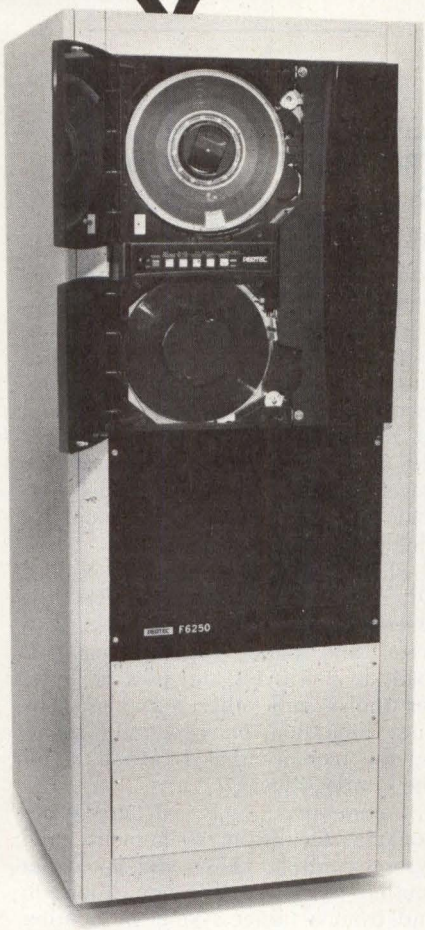
The A-Natural narrative assembler includes a linking loader, librarian, extensive 8080 subroutine library in A-Natural relocatable format, and translators. It facilitates writing the small amount of low level support code needed by most C applications. It can be assembled to relocatable form for use with the company's loader, or translated to assembler code that is compatible with either Microsoft or ISIS-II assemblers.

Output from the loader is in CP/M or ISIS-II executable format. Separate RAM and ROM load addresses may be specified. An ISIS-II interface is available; library support exists for 16- and 32-bit integer arithmetic, as well as 32- and 64-bit floating point.

Each of three sequential passes of the compiler produces a file of similar size to the original C source. Operating on an 8080 with full memory, the compiler can replicate itself and all associated utilities and libraries. Other available utilities are a translator from ISIS-II executable file format to standard Intel hexadecimal for communicating between systems, and a CP/M diskette maintenance program for use on PDP-11 computers.

Circle 424 on Inquiry Card

"Golly, I found a pain in my parity."



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CIRCLE 67 ON INQUIRY CARD

Software Transforms Microcomputer Into Development System

ROM based monitor/debugger, diskette based editor/macro assembler, diskette based relocating loader, diskette utilities package, and a freestanding EPROM programmer with choice of personality modules for the 2708, 2716, TMS2716, 2732, and TMS2532 comprise the 6502 microprocessor development package. It runs on an Apple II computer with 48k bytes of RAM, Apple Disk II, and Autostart ROM to produce a software development system.

The screen oriented monitor accesses all operating modes via the Reset key. As the basis of the operating system, the monitor allows object code or files to be moved, relocated, verified, modified, displayed, loaded, dumped, disassembled, and loaded from or burned into EPROM.

Using the debugger, code can be traced stepwise, transparently, or sent to the output printer port. The debugger supports four software breakpoints, maintains a 128-step trace history, and has four possible external registers. In addition to line, character, or string oriented editing, the editor supports user selectable auto line numbering and renumbering, string searches and replacement, block moves or deletions, and appended files.

Fully relocatable diskette based object code files are generated by the macro assembler. It supports macros, global macros, conditional assembly, output paging, and printout titling. Like the relocator feature of the monitor and complementing similar assembler capabilities, the relocating loader supports separate user defined destination and target addresses in the process of linking and relocating object code files.

The Diskette Utilities Package consists of a comprehensive diskette dump/modify/catalog/copy utility, an object code print utility, symbolic disassembler for use with the editor/macro assembler, and a subroutine relocator which traces and relocates undocumented object code. Optionally available from Micro Power Designs, Inc, 13955 Murphy Rd #112, Alief, TX 77411, is EE Pac I, engineering software consisting of active filter design, 2-dimensional curve fit, 2- to 4-dimensional surface fit, quadratic solution and simultaneous equations, Thevenin equivalences, FFT (up to 4096 data points), and Decision, a weighted comparative analysis program.

Circle 425 on Inquiry Card

Software Assembles Z80/8080 Source Code On Development Systems

Written in EXORciser™ compatible FORTRAN IV, the EXOR 80/XASM assembles Z80 and 8080 source programs into machine code. The assembler runs on Motorola's EXORciser and EXORterm™ 100, 200 Development Systems under MDOS I, II, and III operating systems. This expands the usage and flexibility for software development. Object and source remain on the development system for changes and efficient handling.

Phoenix Digital Corp, 3027 N 33rd Dr, Phoenix, AZ 85017, offers the assembler in MDOS floppy disc, cassette, and paper tape versions. It loads in 28k bytes and uses 8k bytes for tables and other variables. The only limitation on program size is by the memory that is available for the symbol table.

Communication is via COMMAND FORMAT, file/listing assignments, and system controls. Down and up loader routines provide communication to and from a target system or another development system; the only requirement is available ACIA ports. Editing and P/ROM programming can be handled with standard EXORciser software. Other features include assembly control, pseudo-operations via normal Zilog syntax, and an optional Z80/8080 disassembler.

Circle 426 on Inquiry Card

Interactive Program Offers Hardcopy Graphics Capability

Problems of retention and resolution associated with graphics on microcomputer CRTs are solved by a hardcopy graphics program for Commodore PET, Radio Shack TRS-80 (Level II), and Apple II microcomputers (minimum memory requirements of 16k bytes of RAM). For hardcopy output the computers connect through an RS-232 interface to a Houston Instruments' HIPLOT plotter, which features eight directions of pen movement under software control.

Written in BASIC on tape cassette, CURVE can produce finished graphs of tabular data and mathematic equations. Plot capabilities are Cartesian equations $Y = f(X)$, parametric equations $X = h(T)$ and $Y = g(T)$, polar equations $R = f(S)$, data points entered from the keyboard, and bar graphs. Although straight-line interpolation is used between data points, the plotter traces out Cartesian equations accurately to within one plotter step using an algorithm. Internal checks prevent overrunning plot region boundaries; the pen lifts whenever the trace attempts to move beyond defined boundaries.

Combinations of these functions produce professional graphs and charts using either of two versions of the program. The first version, CURVE PROGRAM, is a keyboard interactive code which fully guides the user through its operation. It contains built-in error messages and requires no programming experience. The CURVE SUBROUTINE version allows the user to add customized hardcopy graphics to existing BASIC programs.

West Coast Consultants, 1775 Lincoln Blvd, Tracy, CA 95376, has included an alphanumeric character set (upper case) with software control of both character size and style. A bold character font is also provided. Choice of four colors is available. A flashing message on the CRT and an audible tone signal when it is time to change the pen.

Circle 427 on Inquiry Card □

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MBI-49-LPC For IBM Series/1
MDB-4034 For Data General**, programmed I/O
MDB-42XX For Data General, data channel (DMA)
MDB-46-206 For Perkin-Elmer (Interdata)
MDB-49044 For Hewlett-Packard, 2100, 21MX & 1000

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MDB also supplies other peripheral device controllers, general purpose logic modules, systems modules and communication/terminal modules for DEC PDP-11 and LSI-11, Data General, Perkin-Elmer and IBM Series/1 computers. MDB has also announced new interface modules for use with Intel Multibus Single Board Computers.Δ Product literature kits are complete with data sheets, pricing and discount schedules.

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Circle 68 for LSI; 69 for PDP; 70 for DG; 71 for P-E; 72 for IBM; 142 for H-P.

8-Bit Slice ECL Computer Component Family

Paul Chu

Fairchild Camera & Instrument

Mountain View, California

Recent advances in large scale integration of ECL components have provided an opportunity for designers of ultrafast systems to utilize LSI techniques previously available only in slower systems using NMOS or TTL components. The use of LSI ECL components, coupled with high speed bipolar memories, makes system design much easier, and at the same time provides enhanced performance and more economical systems. Microprogram control is becoming increasingly popular in very high performance systems, offering needed flexibility in the instruction set as well as allowing variations in control word and data path width as required for modular system architectures. Implementation of these capabilities in ECL is now leading to the development of new bit-slice architectures.

8-Bit Slice Family

The F100220 8-bit slice family of subnanosecond ECL parts developed by Fairchild provides flexible logic building blocks based on the best attainable compromise between semiconductor processing economics and packaging constraints. Table 1 indicates the basic elements of the family and their functions. An example of a generalized system configuration utilizing these elements is shown in Fig 1.

Designed on a bit-slice basis to provide easy modularity and to minimize interconnection problems, while enhancing high speed performance, the family utilizes bidirectional capabilities of an ECL-driven bus to allow very modular and flexible system architecture. Word widths may be increased by adding more functional elements in parallel. Modularity is enhanced through the capability of connecting many functions on a bus and communicating among them in either direction. System reliability is enhanced by generation, storage, and detection of byte parity at the device level.

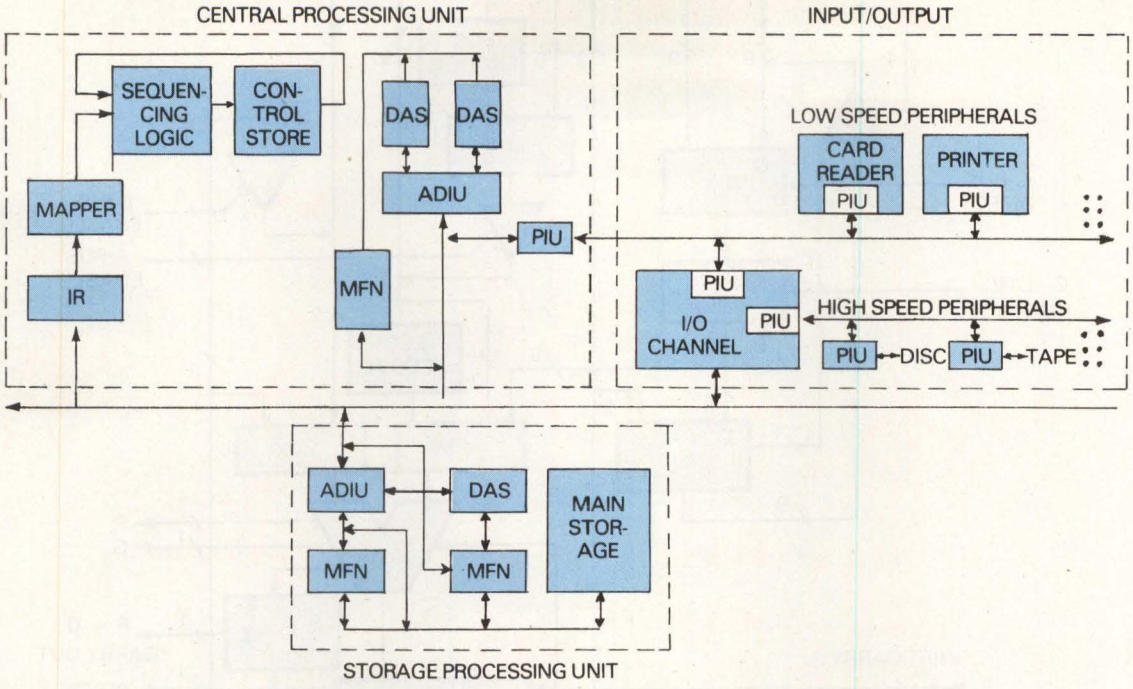

Fig 1 Generalized computer implementation. Four members of Fairchild's F100220 8-bit slice family used here are address and data interface unit (ADIU), dual access stack (DAS), multiple function network (MFN), and programmable interface unit (PIU)

TABLE 1

System Functions in F100220 Family

System Functions	Devices
Random Access Memory Interface Arithmetic Logic Unit	Address and Data Interface Unit (ADIU)—F100220
Register Stacks for CPU Register Stacks for I/O Applications Registers for Data Buffering	Dual Access Stack (DAS)—F100221
Multiplexers, Demultiplexers, and Shifters Exclusive-OR Logic Array (For ECC) Multiport File	Multiple Function Network (MFN)—F100222
I/O Interface Logic High Current Drivers/ Receivers for I/O	Programmable Interface Unit (PIU)—F100223
Next Address Controller For Microprogram Memory	Microprogram Sequencer Unit (MSU)—F100224*

*In development

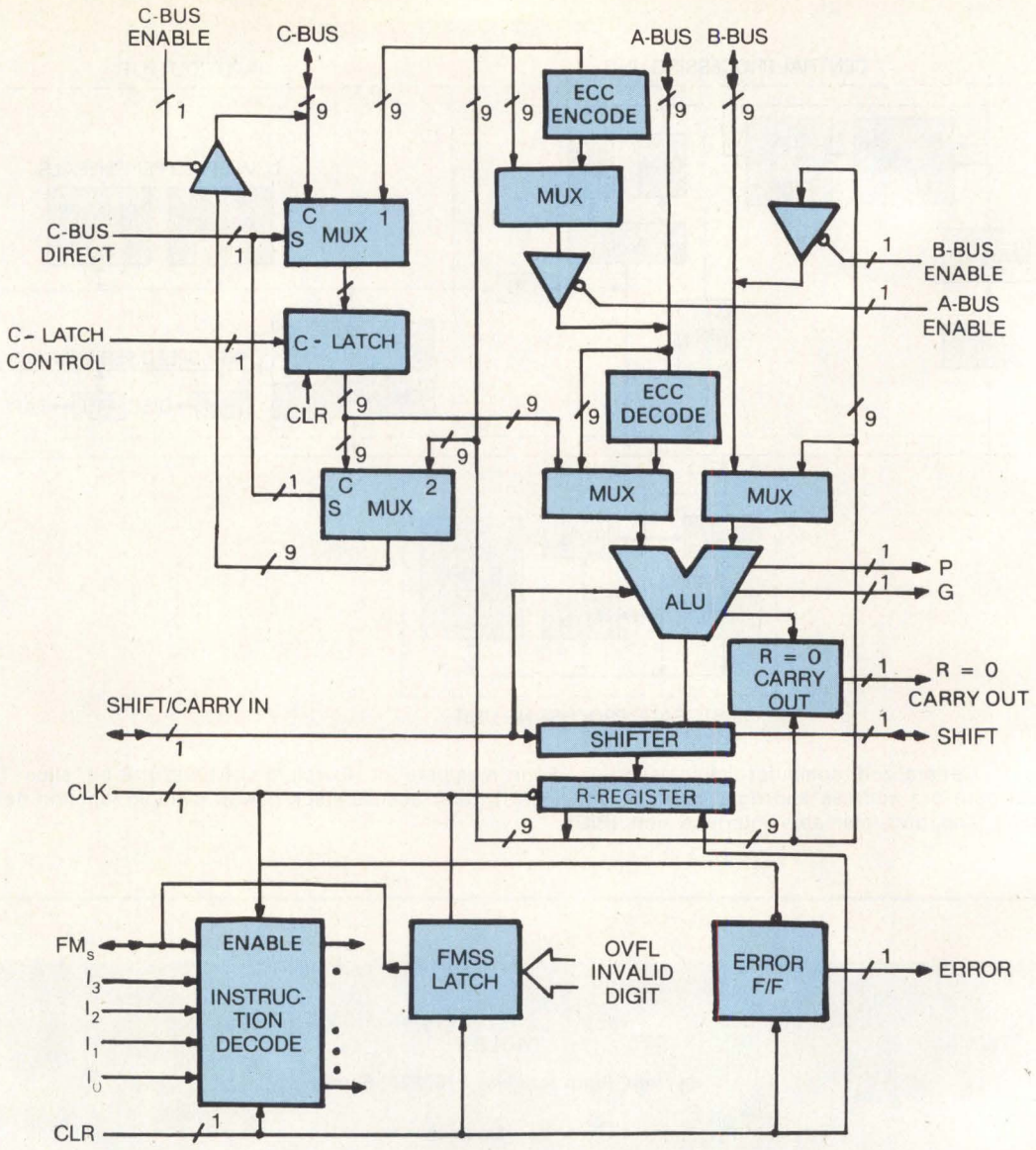

Fig 2 ADIU block diagram. Diverse functions include internal ALUs, multiplexers, register, bi-directional buses, and error correction logic

Address and Data Interface Unit (ADIU)

A prime element in this family, the ADIU is designed to serve multiple functions; for example to operate as an arithmetic and logic unit (ALU) or as a random access memory interface. A block diagram of this device is presented in Fig 2. Three 9-bit buses (8 bits plus parity) are included. These buses are bidirectional, with built-in drivers and receivers, and serve as sources for the ALU operands and also as destinations for the ALU result. Associated with the C-bus is a latch (C-latch) that functions as temporary data storage for either ALU source operand or result.

Operation of the ADIU is controlled by a single clock (CP). The state of four instruction lines (I_3 to I_6) along with a function modifier and special status line (FMS) are decoded at the rising edge of CP to select 1 of 27 possible instructions. This instruction set (see Table 2) includes binary and decimal add and subtract (handling BCD arithmetic in both packed and unpacked formats), single-bit left and right shifts, AND, OR, exclusive-OR, and bus to bus transfers.

Source operands are also encoded by the instruction and can originate from any one of the buses, result register (R), or the C-latch. The result of an operation is always strobed into the R-register during the falling edge of CP. Thus, the active high part of CP is responsible for the decode and execution of an instruction. The ALU result stored in the R register is made available

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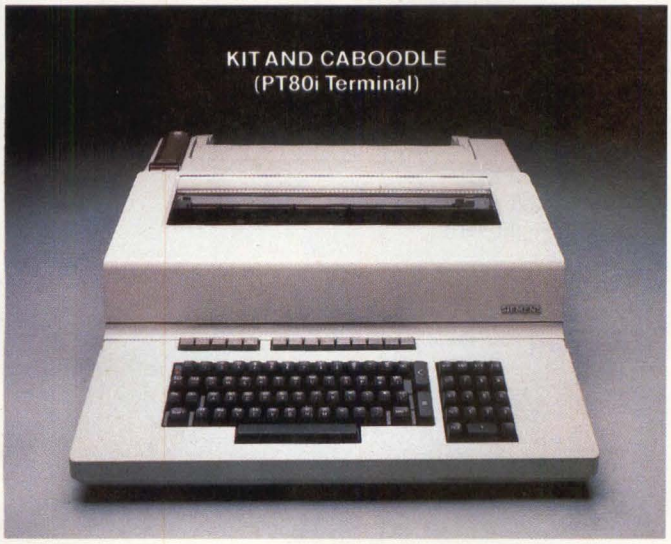

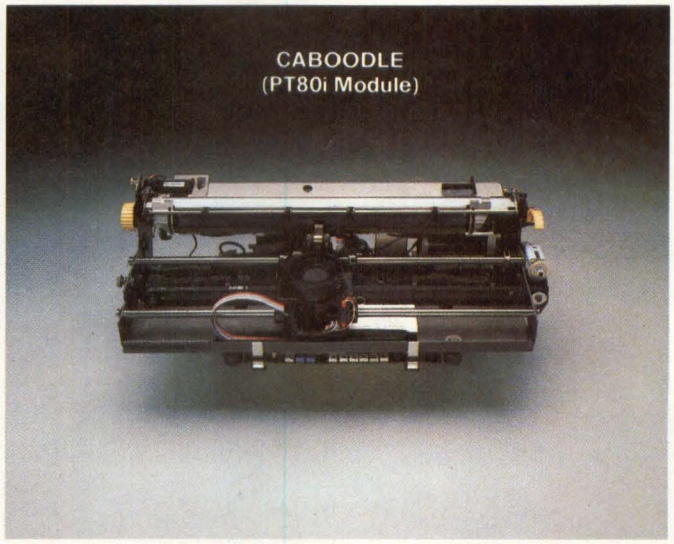

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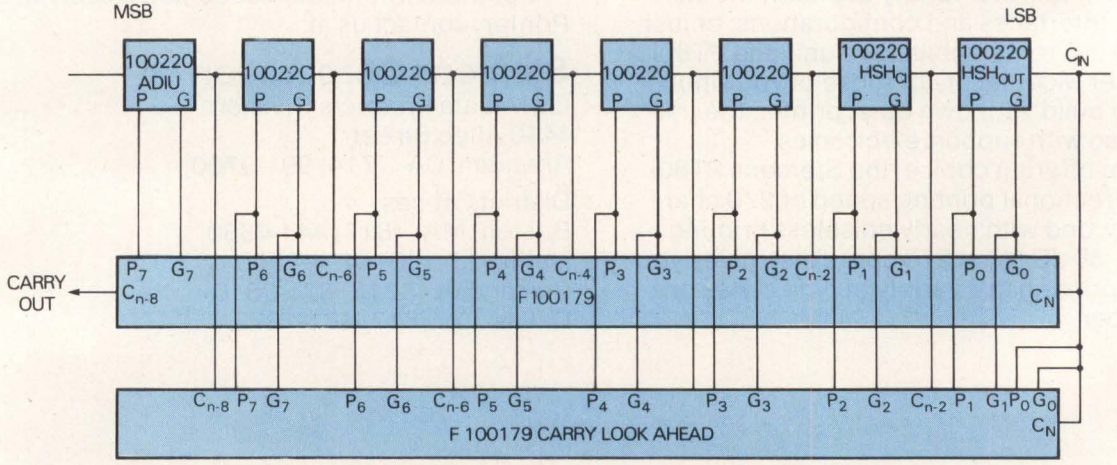
TABLE 2

ADIU Functions

I_3	I_2	I_1	I_0	FMS	Hex Code	ADIU Functions
L	L	L	L	L/H	0	No Operation
L	L	L	H	L/H	1	C→R, ECC Encode of R→A
L	L	H	L	L/H	2	A Minus B→R (Decimal Unpacked) A Minus B→R (Decimal Packed)
L	L	H	H	L/H	3	A Plus B→R (Decimal Unpacked) A Plus B→R (Decimal Packed)
L	H	L	L	L/H	4	B Minus A→R (Binary)
L	H	L	H	L/H	5	R⊻Zero→R R⊻ECC Decode of A→R
L	H	H	L	L/H	6	A Minus B→R (Binary)
L	H	H	H	L/H	7	A Plus B→R (Binary) C Plus B→R (Binary)
H	L	L	L	L/H	8	A Shift Left→R A Shift Right→R
H	L	L	H	L/H	9	B Shift Left→R B Shift Right→R
H	L	H	L	L/H	A	$\overline{A}$→R $\overline{\overline{A}}$→R
H	L	H	H	L/H	B	$\overline{A \wedge B}$→R $\overline{A \vee B}$→R
H	H	L	L	L/H	C	$\overline{B}$→R $\overline{\overline{B}}$→R
H	H	L	H	L/H	D	$\overline{A \vee B}$→R $\overline{A \wedge B}$→R
H	H	H	L	L/H	E	$\overline{C}$→R $\overline{\overline{C}}$→R
H	H	H	H	L/H	F	A⊻B→R



TIMING CALCULATIONS	TYPICAL	MAXIMUM
1) CLK TO P, G	14	23
2) P, G TO C_{n-2}, C_{n-4}, C_{n-6}, ETC.	2.1	3.3
3) C_{IN} TO CLOCK (FALLING EDGE)	6	8.5
	22.1 ns	34.8 ns

Fig 3 High speed 64-bit addition/subtraction using carry lookahead. Eight address and data instruction units operate in parallel to achieve system speed of 22.1 ns

to all three buses by activating their respective bus enable inputs (EO_A, EO_B, EO_C). Routing the result register to its destination and setting up the instruction for the next operation occurs during the inactive low part of CP.

Used as a memory interface, this component supports single-bit error correction and double-bit error detection, with the aid of the multiple function network (MFN). ADIUS generate the partial parities for the Hamming matrix on a byte-wide basis and the MFNS perform further XOR to obtain the check and syndrome bits. Upon detecting a single-bit error, the byte-in-error and bit-in-error information is passed back to the ADIUS, which correct the error bit.

The philosophy in maintaining the data integrity can be illustrated by the three error checking methods of the ADIU. Parity is checked for each of the two source operands selected as ALU inputs for every ADIU operation. Moreover, the ADIU often serves as a center in the data path for bus to bus address or data transfer. Instead of the information being routed around the data path, it can be routed through the ADIU in the data path. The ADIU in this case will generate parity on the otherwise unaltered bus information and will compare the generated parity with the received parity to perform a check. During single-bit error correction operations, the ADIU will check the incoming encoded bit-in-error information for a fixed pattern to prevent the accidental inversion of the wrong data due to multiple or check bit errors.

If an error is found in any of these cases, an error flip-flop is set at the falling edge of CP. In addition, several condition codes, such as binary overflow, invalid decimal digit, zero result, and carry out, are available for use as status indication during conditional branching instructions by the microprogram sequencer.

Fig 3 illustrates the use of eight ADIU components in parallel for a high speed 64-bit addition/subtraction system using carry lookahead. Typical speed for this system is 22.1 ns.

Summary

The ADIU is a byte-wide slice, which can be used to interface a memory or to build a processor data path. As a memory interface device, it can handle address and data transfers between a memory and a processor. It is capable of modifying address on the way to memory, and the validity of memory data transfers can be checked because it has built-in error correction code logic. The component has a full spectrum of arithmetic and logical capabilities and the ability to shift data in either direction. Properly timed, it can take an argument from a given bus, operate upon that argument, and return the result of that operation to the same bus as well as to the other two buses during the same microcycle.

Arithmetic capabilities of this element may also be used in conjunction with the MFN and DAS units of the family to control main memory and addressing (Fig 1). In later columns, the capabilities of those and other members of this modular family will be treated in further detail. As is seen in the case of the ADIU, the family as a whole is characterized by the multiplicity and diversity of functions available within each component.

Analog Building Block Acts as ADC Front End

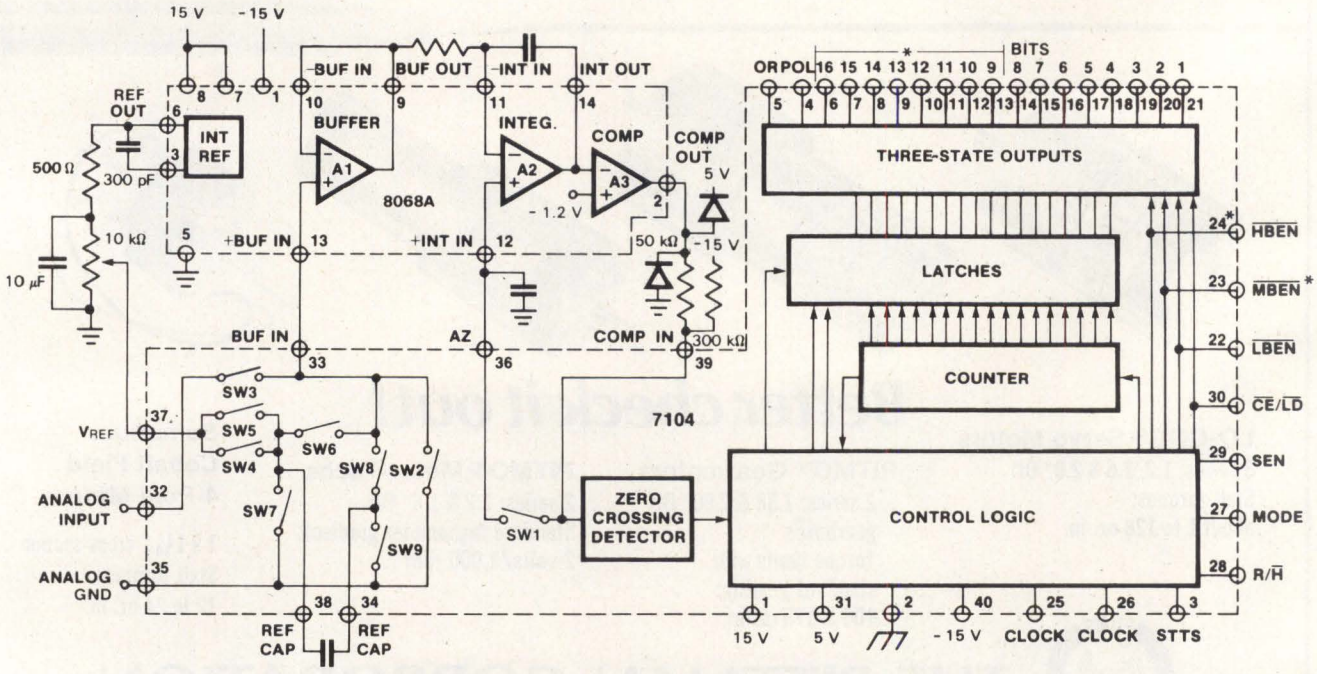
All essential analog elements of a very accurate dual-slope integrating A-D converter are provided by a building block chip, the ICL8068, produced by Intersil, Inc, 10710 N Tantau Ave, Cupertino, CA 95014. Ion implantation combines bipolar op amps with JFET input stages to form high impedance unity gain buffer stage, integrator, and comparator elements. The device can be used with any of the digital controller ICs from the same manufacturer to provide a 2-chip ADC with precise autozero, autopolarity with ±0 null indication, true input integration over a constant period for maximum emi rejection, ratiometric operation, over-range indication, and a built-in reference. These 2-chip pairs allow a manufacturer to generate an entire family of instruments using only one basic PC board with two or three jumper points.

This chip is particularly appropriate for situations in which noise figures (typically below 2 to 3 μV) are an important consideration or where the input is a low level signal. An alternative analog building block, the ICL8052, offers significantly lower input leakage currents and may be found preferable in systems with high input impedances. However, the device presented here will give better performance in noise-critical systems.

A 2-chip set including this building block and the ICL7101 digital controller acts as a 3½-digit A-D pair with parallel BCD outputs, and is well suited for data processing applications or liquid crystal display interface. The combination provides 4½-digit accuracy in a 3½-digit format. Typical system performance is 100-pA input leakage, autozero operation to 10 μV with less than 1-μV offset drift/°C, and linearity to 0.002%.

Combination of the analog chip with the ICL7104 CMOS controller results in a 16-bit binary output ADC specifically intended for microprocessors. The interface capability of the pair allows it to be used with virtually all microprocessor systems with buses up to 18 bits wide. Providing high performance and low noise, the A-D chip set will operate in either close-in parallel or handshake mode. It features not only 16-bit accuracy, but also full 3-state output to permit interface with most current 8-, 12-, or 16-bit microprocessors, along with UART handshake compatibility. The CMOS controller section performs the analog phase switching and all digital functions of a 16-, 14-, or 12-bit binary ADC, with the companion analog section adding the linear circuits.

Using the byte organized parallel mode, the pair can interface directly with the data buses of such microprocessors as the Intersil 6100, the Intel 8080 and 8048, and the Motorola MC6800. In the ICL7104-16, there are 18 data output lines providing 16 bits of magnitude, plus polarity and out of range. These output lines can be grouped in three 8-bit bytes for 8-bit microprocessors, with each byte activated with its own byte enable line. The output lines can also be grouped in a 10- and



Analog building block ICL8068 from Intersil is shown in combination with ICL7104 CMOS controller from same manufacturer. 2-chip set functions as 16-bit ADC and is particularly useful in systems where noise level is critical. Alternate analog chip, ICL8052, whose performance is not as good with regard to noise, offers lower input leakage current

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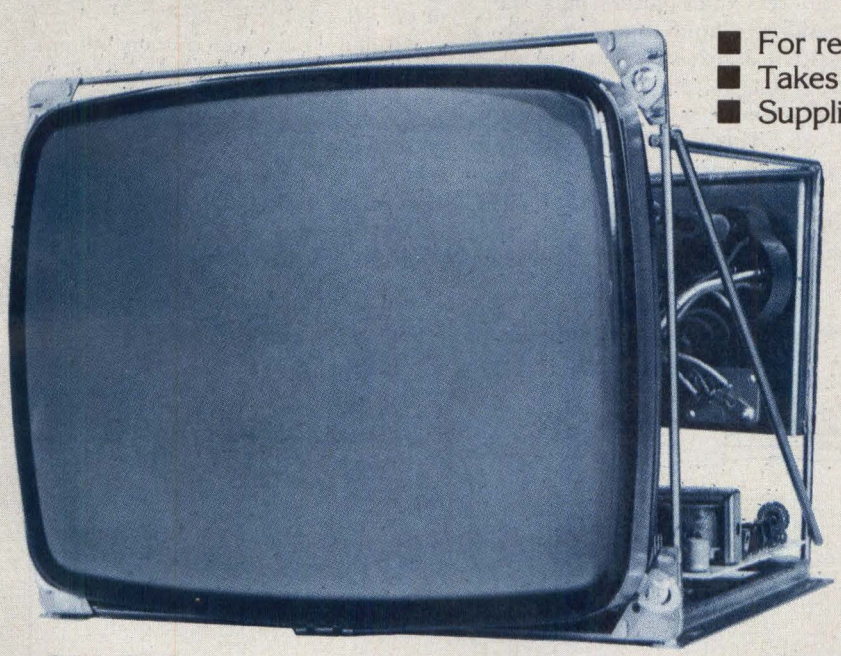

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CIRCLE 75 ON INQUIRY CARD

8-bit byte for 12-bit microprocessors, or grouped in a 16- and 2-bit byte for 16-bit microprocessors.

In the handshake mode, the controller has two inputs that allow the device to sequence through three bytes (for the 16-bit version) or two bytes (for the 14- and 12-bit versions) either synchronously or on demand without the addition of external components. The chip set can thus interface directly with such devices as UARTs for remote data transmission.

Circle 350 on Inquiry Card

Memory Address MUX And Refresh Counter Combine To Support Dynamic RAMs

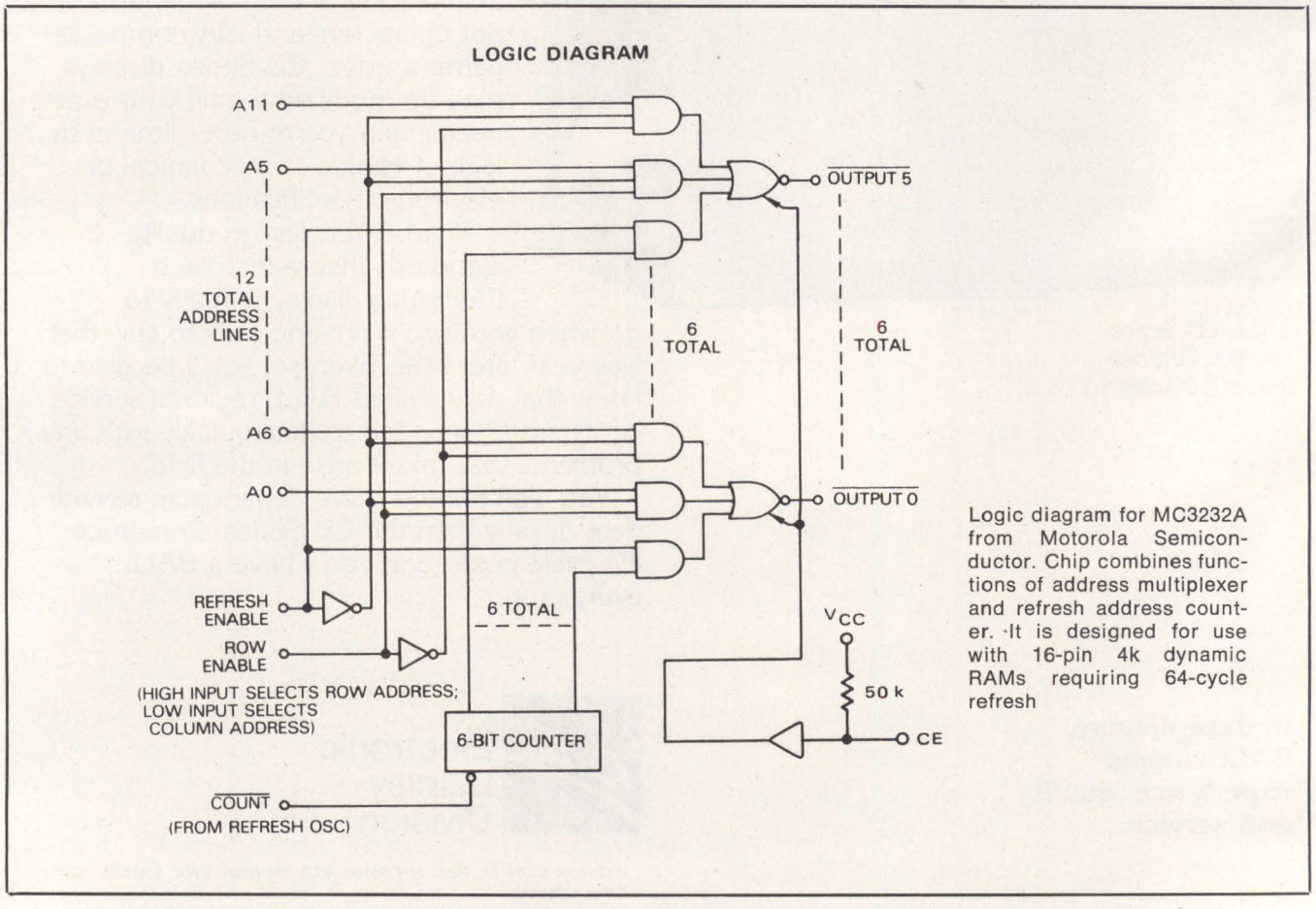
Designed specifically for use with 16-pin, 4k dynamic random access memories, the MC3232A combines the functions of a memory address multiplexer and a refresh counter. This memory interface IC from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, is for use with RAMs that require a 64-cycle refresh. It multiplexes 12 system address bits to the six input address pins of the memory device. The 6-bit refresh counter on this chip is clocked externally to generate the 64 sequential addresses required for refresh. In conjunction with the previously introduced MC3480 memory controller, this IC accomplishes the entire memory control function in a 2-chip set with an external refresh oscillator.

The address multiplexer splits the 12-bit address input signal (representing 4096 addresses) into two sequential 6-bit outputs representing row and column address segments, respectively. This satisfies the 16-pin memory requirement calling for the use of the same six input pins for all address bits in order to reduce the size and complexity of the memory package. In addition, the 6-bit counter uses the same multiplexer output pins to select all 64 memory rows sequentially during the refresh portion of the memory cycle. Thus, in response to timing signals from the controller, this chip provides the complete memory address function.

Other characteristics include a high input impedance for minimum loading of the bus (I_F = 0.25 mA max) and Schottky TTL for high performance address input-to-output delay (25 ns for C_L = 250 pF, 9.0 ns for C_L = 15 pF). The device is a second source to Intel's 3232, with detect zero function not included and additional power fail feature added at pin 13.

Absolute maximum ratings require that all voltages (V_{CC}, V_I, V_O) lie between −0.5 and 7.0 V. Output current is not to exceed 100 mA. The allowable temperature range is 0 to 75 °C in operation and −65 to 150 °C in storage. Both plastic and ceramic packages are available.

Circle 351 on Inquiry Card



Logic diagram for MC3232A from Motorola Semiconductor. Chip combines functions of address multiplexer and refresh address counter. It is designed for use with 16-pin 4k dynamic RAMs requiring 64-cycle refresh

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8k Memory Claimed as Industry's Fastest EPROM

Featuring a maximum access time of 250 ns, an 8k-bit electrically programmable read only memory offers automatic chip-select/power-down, low power dissipation, and fully static operation. TMS2508 is an addition to an existing family of EPROMs produced by Texas Instruments Inc, PO Box 1443, Houston, TX 77001. It is pin compatible with the other memories in the family and, like them, needs only a single 5-V power supply.

Organized as 1k x 8, with fully TTL compatible I/O, the device is believed to be the fastest EPROM available, standing in contrast to typical EPROM speeds in the 350- to 450-ns range. This speed capability is seen as particularly significant as increased capabilities of microprocessors have placed performance demands on memory access times.

The memory is fabricated using n-channel silicon gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs, including program data inputs, can be driven by Series 74 TTL circuits without the use of external pullup resistors, and each output can drive one Series 74 TTL circuit without external resistors. Data outputs are 3-state for OR tying multiple devices on a common bus.

A 25-V supply is needed for programming, but all programming signals are TTL level, requiring a single 50-ms pulse. For programming outside the system, existing 5-V EPROM programmers can be used. Total programming time for all bits is 50 s.

Additional features include JEDEC standard pinouts and guaranteed dc noise immunity with standard TTL loads. Typical power dissipation is 250 mW (active) and 50 mW (standby).

In addition to the 250-ns version (suffix -25), the device is offered in a 300-ns version (suffix -30). These devices can be programmed singly or in blocks, and data can be erased by ultraviolet light. Both versions are available in 24-pin ceramic dual-inline (JL suffix) or sidebraised (JDL suffix) packages, and both are rated for operation from 0 to 70 °C.

Absolute maximum ratings require that supply voltages V_{CC} and V_{PP} lie, respectively, between −0.3 and 6 V and −0.3 and 28 V. All input and output voltages with respect to V_{SS} must remain between −0.3 and 6 V.

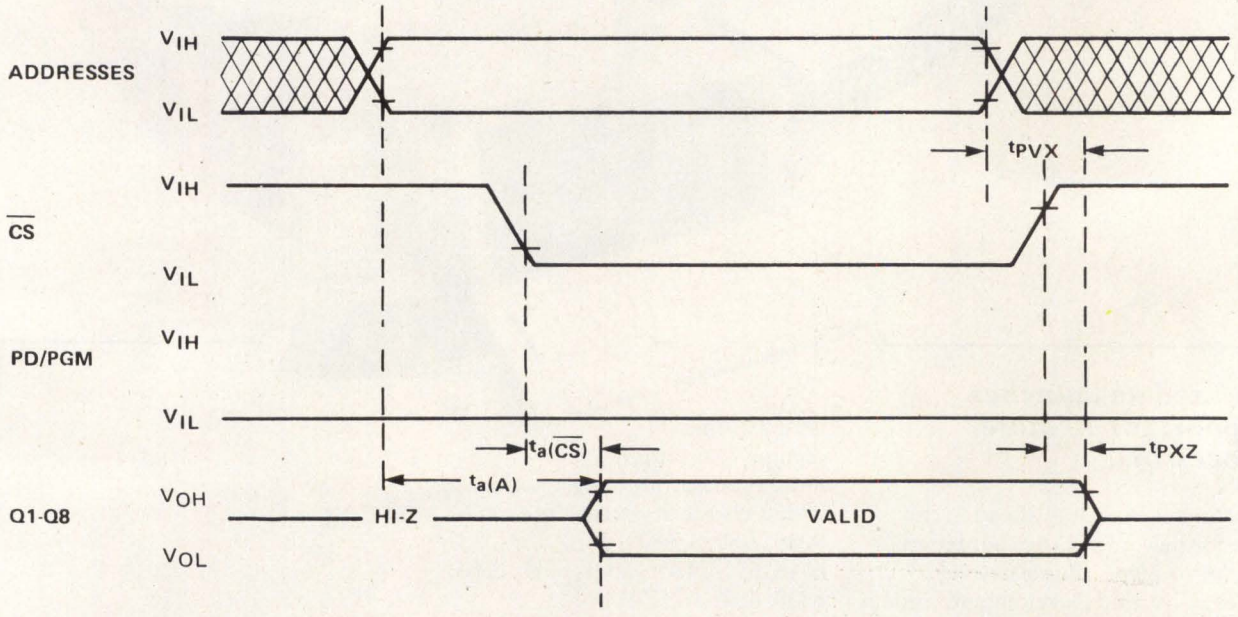

Diagram indicates read cycle timing for fast 1024 x 8 TMS2508-25 EPROM from Texas Instruments. Access time from address, $t_a(A)$, is 180 ns (typ), 250 ns (max). Max access time from chip select, $t_a(CS)$, is 125 ns. Output not valid from address change, t_{PVX}, and output disable time from chip deselect, t_{PXZ}, must both be non-negative, with latter parameter not to exceed 100 ns

Circle 352 on Inquiry Card

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A digitizer is a graphic peripheral input device for transmitting points, lines and curves from the surface of a flat matrix tablet to a computer which accepts the data for immediate processing or future use and modification.

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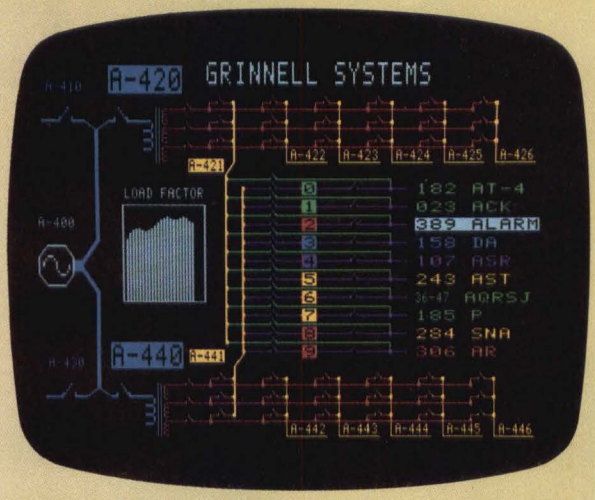

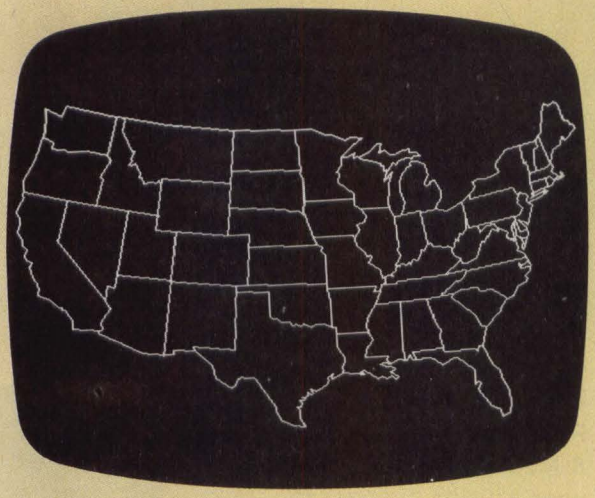

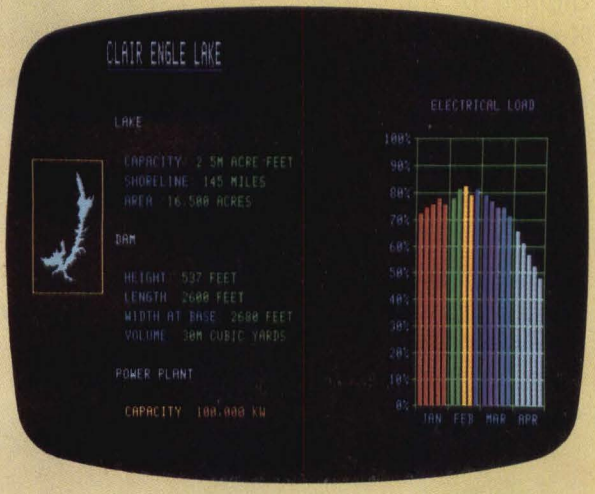

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And, every GMR-37 display is a complete operating system: display generator, MOS refresh memory, vector and rectilinear graphics, alphanumerics in 4 sizes, bi-directional RS-232 computer interface and RS-170 video interface. Systems, including power supplies, are housed in a 7″, rack-mountable chassis and drive standard closed circuit monitors.

Four basic GMR-37 models can be tailored to fit into almost any computer-based system. Here are just a few examples. (Prices are F.O.B. San Jose, and quantity discounts are available. TV monitors are extra.):

GMR 37-20: $3700
256 x 512 resolution, one channel RGB color plus blink. (Two channels: $4500)

GMR 37-30: $4500
512 x 512 resolution, one channel RGB color plus blink.

GMR 37-60: $4700
1024 x 1024 resolution, one channel B/W.

In addition, you can also have several economical options: independent cursors, joysticks, keyboards, special character sets and 16 bit, plug-compatible parallel minicomputer interfaces.

Further, if you ever want to move up, Grinnell has a complete line of larger systems—all software compatible with the GMR-37—to do things like animation, image processing and real-time frame grabbing.

So, if quality graphic displays are important to your product, look at the GMR-37 line. For a quotation on the system that meets your specific requirements, call or write.

GRINNELL SYSTEMS

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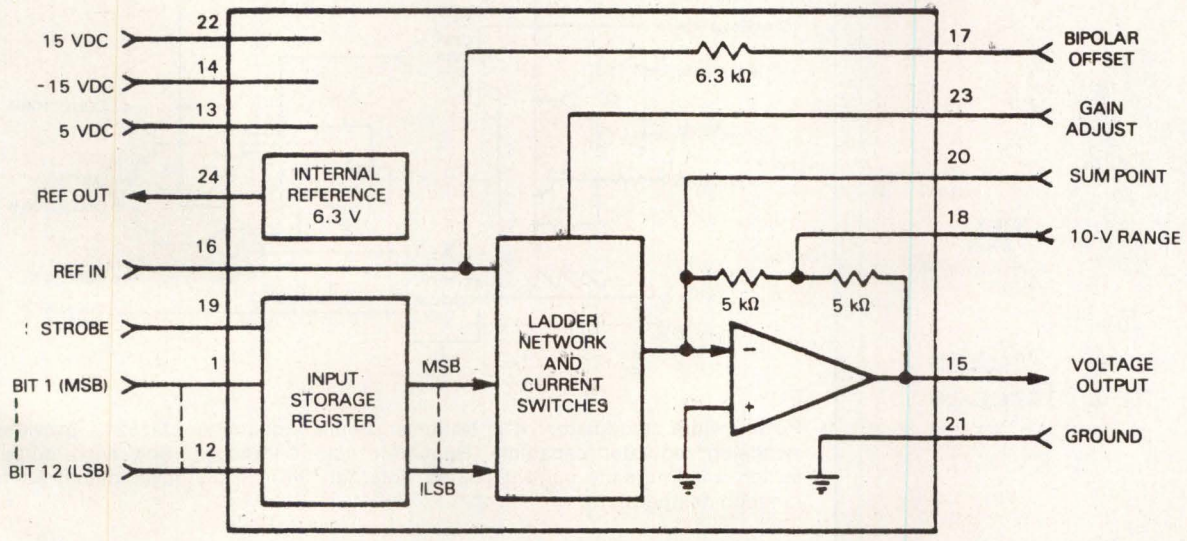
CIRCLE 78 ON INQUIRY CARD

Fast, Low Power 12-Bit DAC Contains Strobed Input Register



DAC-SL from ILC Data Device Corp features 12-bit strobed input register. Internal reference provides 6.3 ±0.3 V, and device can also accept external reference

Having a power consumption of 450 mW (typ) and a settling time to 0.01% FSR of 5 μs (typ) and 10 μs (max) for the ±10-V output range, a D-A converter of 12-bit resolution features a strobed internal input register, able to store the digital input. The leading edge of the 20-ns strobe pulse can be simultaneous with the leading edge of the data pulse, or it can be delayed, and the data bits must remain valid until the strobe pulse is complete.

Designed for use in medical instrumentation, CRT displays, and avionics systems, the DAC-SL from ILC Data Device Corp, Airport International Plaza, Bohemia, NY 11715, is complete with an internal reference and feedback resistors. An external reference can be used so that the output can track a system reference. Maximum linearity error is ±0.0125% of full scale over the temperature range, and the gain and offset errors can be trimmed out. Coding is complementary binary or complementary offset binary.

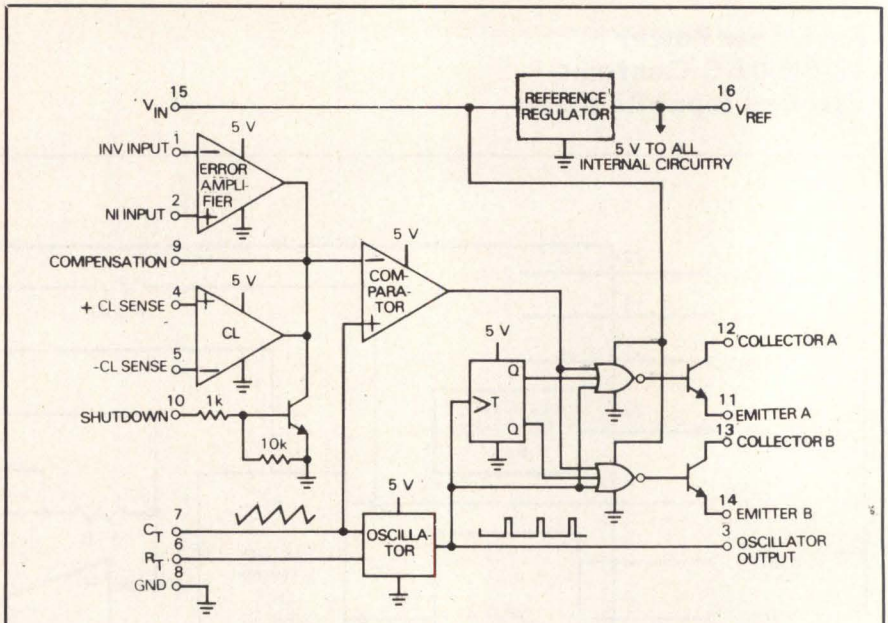
The DAC requires ±15- and 5-V power supplies. Input is TTL compatible and pin programmable output ranges are ±10, ±5, and 0 to 5 V. For the latter two ranges, the values for settling time to 0.01% FSR are reduced to 3 μs (typ) and 6 μs (max). Size is 0.8 x 1.4 x 0.2" (2 x 3.6 x 0.5 cm) and weight is 0.4 oz (11.3 g) typ. Two operating temperature ranges are available, −55 to 125 °C and 0 to 70 °C.

Housed in a hermetically sealed 24-pin dual-inline package, the hybrid converter is processed to MIL-STD-883, and screening is based on methods 5004/5008. With optional burn-in, the MTBF is 2.2 x 10^6 h for ground fixed conditions and 25 °C case temperature.

Circle 353 on Inquiry Card

Low Cost Pulse Width Modulator Chip Features Thermal Shutdown

A regulating pulse width modulator chip contains a 5-V voltage regulator capable of supplying up to 50 mA to external circuitry, a control amplifier, an oscillator, a pulse width modulator, a phase splitting flipflop, dual alternating output switch transistors for both push/pull or single-ended applications, and current limiting and shutdown circuitry. The LM3524 from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, is a second-sourced version of the corresponding part (SG3524) from Silicon General, and is claimed to be the first version of this regulator to employ an internal



Pulse width modulator IC, National Semiconductor's LM3524, provides switching regulator capability. Regulator output transistor and each output switch are internally current limited. Internal thermal shutdown circuit limits junction temperature

thermal shutdown circuit to limit junction temperatures.

Applications include step-up and step-down switching regulators, transformer coupled dc to dc converters, transformerless polarity converters, voltage doublers, motor speed controllers, and other power control devices. The chip contains the control circuitry to build a switching regulator capable of handling inputs from 5 to 40 V.

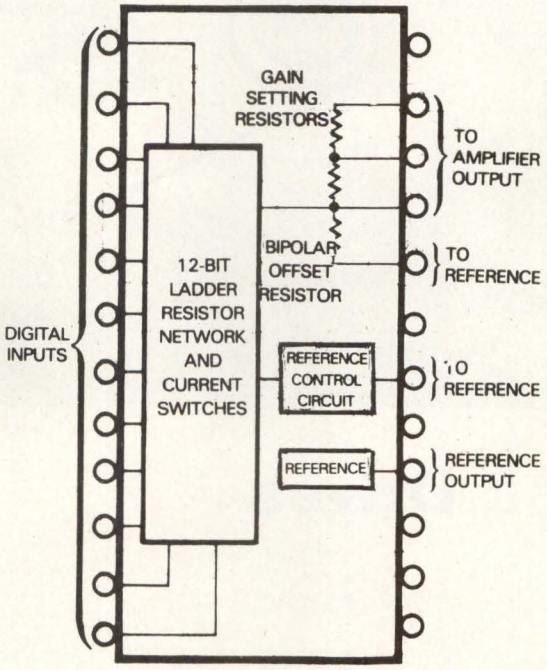
A 2% variation limit on frequency over the operating temperature range is a key specification, with frequency adjustable to more than 100 kHz. Total quiescent current is rated at less than 10 mA. The outputs are npn transistors, capable of a max current of 100 mA. These transistors are driven 180° out of phase and have noncommitted open collectors and emitters.

Frequency of the stable onchip oscillator is set by an external resistor, R_T, and capacitor, C_T. The oscillator's output provides signals for triggering an internal flipflop, which directs the pulse width modulator information to the outputs, and a blanking pulse to turn off both outputs during transitions to ensure that cross conduction does not occur. Width of the blanking pulse, or dead time, is controlled by the value of C_T. Recommended values are 1.8 to 100 kΩ for R_T and 0.001 to 0.1 μF for C_T.

A differential-input transconductance amplifier acts as the error amplifier. Its gain, nominally 80 dB, is set by either feedback or output loading with either purely resistive or a combination of resistive and reactive components.

LM3524 is rated for operation over the commercial range of 0 to 70 °C and is available in a 16-pin dual-inline package at $4 in 100-up quantities. A higher performance version, LM1524, is specified over the −55 to 125 °C range. LM2524 is an intermediate version, specified over the commercial temperature range, while sharing the tighter electrical specifications of the higher performance model.

Absolute maximum ratings limit input voltage to 40 V, reference voltage (forced) to 6 V, and reference output current to 50 mA. Output current at each output must not exceed 100 mA, nor may oscillator charging current exceed 5 mA. Internal power dissipation of the device is limited to 1 W.



Burr-Brown's DAC863 12-bit current output DAC is implemented in 3-chip set. It differs from DAC862 by same manufacturer in providing internal reference chip

12-Bit DAC Contains Internal Reference

A 12-bit current output digital to analog converter with nonlinearity as low as ±¼ LSB, gain drift of ±5 ppm/°C (max), and bipolar offset drift of ±4 ppm/°C (max), is implemented on three chips. These are a stable weighted current switch chip, a thin film laser-trimmed resistor chip, and an internal reference chip. The DAC863 from Burr-Brown, PO Box 11400, Tucson, AZ 85734, differs from the existing DAC862 by the same manufacturer only in having the internal reference, which utilizes a xener diode, and is stabilized for consistent accuracy over temperature.

Analog output is accurate to within ±0.01% and 12-bit monotonicity is guaranteed over the entire operating temperature range. The digital input code is positive true logic and is compatible with TTL or CMOS logic without buffering. Offset binary code is created by offsetting the output amplifier with the DAC reference. Two's complement code is obtained from offset binary by inverting bit 1 (MSB) externally.

Settling time is guaranteed to be <3.5 μs for FSR change to within 0.01% of final value. For a 1 LSB change at the major carry point (the point at which the MSB changes states), settling time is 1.8 μs typ.

The DAC is pin compatible with the AD563 from Analog Devices, and is provided in two temperature ranges. A KG suffix denotes an operating range of 0 to 70 °C, and a BG suffix denotes −25 to 85 °C. Screening to the requirements of MIL-STD-883 is available for the devices, which are provided in hermetically sealed 24-pin dual-inline packages. □

Circle 354 on Inquiry Card

PRODUCT FEATURE

Tape Transport Provides Backup For Winchester Disc Drives

Data Streamer™, a low cost 0.5″ (1.3-cm) reel-to-reel tape transport announced by Kennedy Co, provides backup and archival storage for multiplatter 8″ (20-cm) and 14″ (36-cm) Winchester disc drives. In streaming mode, the model 6809 stores or restores 12M bytes of data in little more than 1 min. Total capacity is 46M bytes on a 10″ (25-cm) reel.

Control Features

Microprocessor control eliminates mechanical or vacuum column tape tensioning elements and capstan as well as numerous analog circuit elements normally associated with servomechanisms. An encoder on an idler roller monitors tape movement and provides source signals for tape position. Tension feedback signals are supplied by a separate sensor. The microprocessor, using sophisticated algorithms stored in onchip P/ROM, calculates the radii of the tape on both reels and supplies proper servomotor signals to maintain constant tape tension at the 100 in (254-cm)/s ±5% streaming mode speed.

Routines also control tape movement when errors are detected. The tape is ramped to a stop, reversed at 12.5 in (31.8 cm)/s to a position where it can be ramped up to 100 in (254 cm)/s prior to the erroneous data block. In addition, microprocessor control provides diagnostic routines to aid service in the field.

An integral formatter has all logic necessary for reading, writing, and control of 1600 char/in (630/cm) phase-encoded ANSI and IBM compatible 9-track tape. It generates preamble, postamble, file marks, and identification bursts. All timing is referenced to a quartz crystal controlled oscillator.

Specifications

In streaming mode (100 in [254 cm]/s), access time is 295 ms for both read and write; in start/stop mode (12.5 in [31.8 cm]/s), read access time is 44 ms and write access is 40 ms. Rewind is accomplished at 200 in (508 cm)/s. Nominal recovery time is 1165 ms when a new command is given while the transport is in the streaming mode. When stopped, recovery time is 870 ms.

Mean time before failure is more than 5000 h; mean time to repair is only 0.5 h because of the modular construction. Recoverable read/write errors are less than 1 bit in 10^9.

The transport can be mounted horizontally in a lowboy console or vertically in standard EIA racks. Dimensions are 8.75 x 19 x 24″ (22.2 x 48.3 x 61 cm); weight is 50 lb (22.7 kg).

Required voltage is 115 V at 60 Hz. Available options are 100-V, 50- or 60-Hz; 220-V, 50-Hz; 230-V, 60-Hz; and 240-V, 50-Hz. Maximum power consumption is 250 W.

Price and Delivery

The model 6809 Data Streamer transport, with integral formatter, is priced at $2500 each in OEM quantities. Delivery is 60 to 90 days ARO. Kennedy Co, 1600 S Shamrock Ave, Monrovia, CA 91016. Tel: 213/357-8831.

For additional information circle 199 on inquiry card.

NOW 1,344,000 BYTES

672,000 BYTE TAPE DRIVE FOR 3M DC100A DATA CARTRIDGE

Qantex

MODEL 200 MINIDRIVE™...

The most compact tape drive ever...
Large, up to 1,344,000 bytes capacity...
Recording on one, two or four tracks...
Read-after-write capability...
3M DC100A or ITC TC-150 Data Cartridge...
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Low power requirements, +5 and +12 Volts DC only...
High electrical and mechanical reliability...
Flexible configurations range from basic OEM building blocks to complete tape memory systems...
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From $250 in single unit quantities...
Contact us today for complete details...

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North Atlantic Industries
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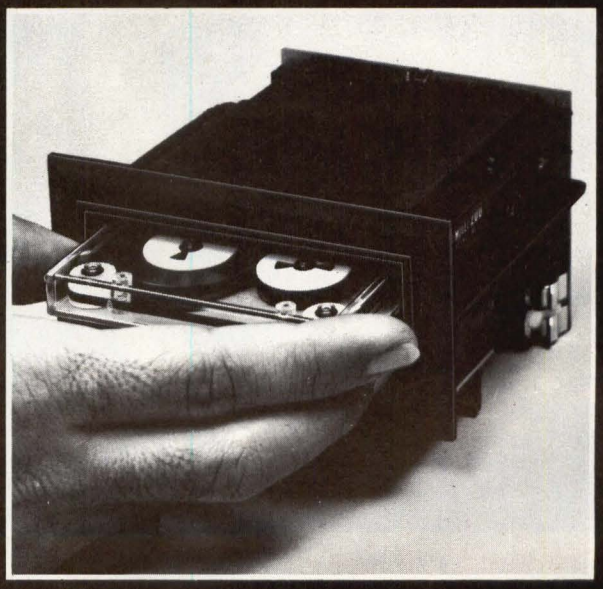
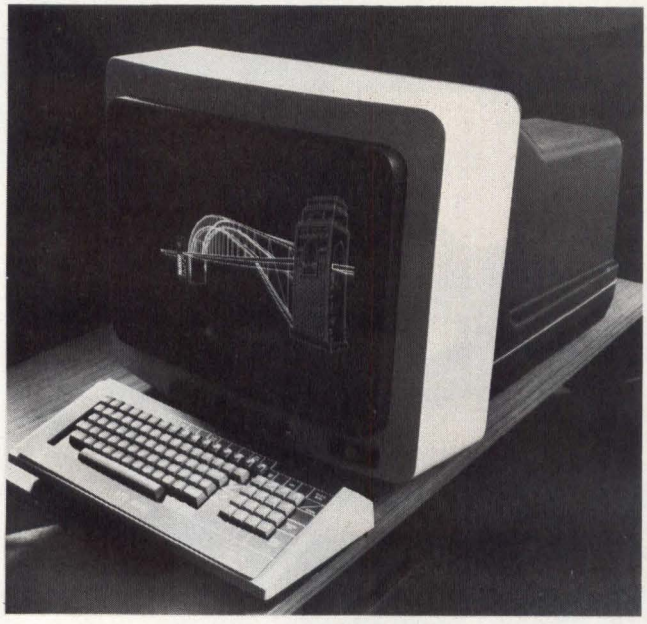


PRODUCTS

Graphic Indicators Display Four Colors Simultaneously With Greater Stability

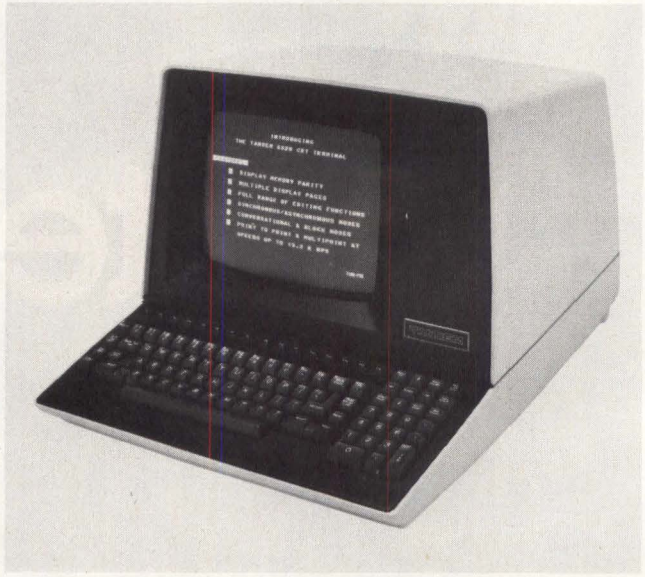
Application of a layered phosphor, beam penetration technique on 740 and 760 series Color Indicators enables simultaneous display of red, orange, yellow, and green. By utilizing full deflection rates of a high speed display system for all 4 colors, a typical character can be traced in 2.1 s in any color, including red. A dual-anode technique reduces system stress and increases reliability of the indicator because it requires less power than single-anode color units. It also provides greater color stability and fewer maintenance adjustments. A built-in test feature displays a test pattern that visually identifies any failed modules. 740 series have a 21″ (53-cm) rectangular face; 760 series have a 23″ (58-cm) round configuration. Both are available in either desktop or rackmounted versions and the 740 can be either vertical or horizontal.

Input specs include 10M-bit asynchronous color selection; 0- to 2-V low-true signal, serial multiplexed on Z graphics input; X and Y graphics 5 Vdc (full scale) into 75 Ω; and Z graphics 0 to 1.5 V into 75 Ω. Each color on the P49 phosphor screen has an individual control for a 4:1 min contrast ratio; positioning accuracy and repeatability are ±0.1% of FS. Random position time is 25 μs max for full-screen deflection of the viewing area, character write time is 150 ns/stroke, vector write time is 3 μs/in (1.2/cm), and color switching requires 175 μs. Electrical input can be within a range of from 100 to 240 Vac ±15%, 47 to 63 Hz. Power consumption is 500 W avg, 1000 W worst case. Each unit uses self-contained forced air cooling for operation over the 15 to 45 °C range at relative humidity of 10 to 90% noncondensing. **Sanders Associates, Inc, Information Products Div,** Daniel Webster Hwy S, Nashua, NH 06031.



Circle 200 on Inquiry Card

Video Display Terminal Provides Memory Parity Checking



Believed to be the only available terminal that provides data integrity from display memory, rather than offering I/O parity checking on the communications line, the model 6520 monitors characters written from display memory to the host processor as well as from the processor back to the terminal. If an entry keyed into display memory is not the one transmitted to the host computer, an error message is presented to the operator and any I/O activity in progress is terminated to prevent contamination of the data base. In addition, the terminal offers multiple display paging for high data throughput and reduced line use, and provides a full complement of video and data attributes, plus editing and program function keys. Numeric keypad and 16 function keys with 32 user programmable functions are included.

Features include conversational and block modes, plus point to point and multipoint operation at 9 speeds between 110 and 19.2k bits/s. Synchronous and asynchronous protocols together with RS-232 and current loop communication links ease interfacing and simplify communications. Display memory is divided into 5 pages, each made up of 1920 characters when the terminal is in block mode. Conversational display memory consists of 120 lines, with 24 displayable at any time. Mode and status information can be shown on the 25th line. The multiple display page feature allows the host processor to read from, or write to, the terminal on any page including the one from which the operator is working, and results in markedly higher data throughput. In conversational mode, the terminal works as a point to point TTY. As keystrokes are made, characters are transmitted. Modes can be changed by a control sequence from the attached host processor. Model 6524 has essentially the same features plus a printer port option. **Tandem Computers, Inc,** 19333 Vallco Pkwy, Cupertino, CA 95014.

Circle 201 on Inquiry Card

The Paper Tiger.™
At $995*, why settle for less.

The Paper Tiger has it all. Eight software-selectable character sizes. 80 and 132 column formats. 96 upper/lower case characters. Continuous duty cycle operation. Stepper-motor tractor feed. Forms control. Multi-part forms. Re-inking ribbon system. Microprocessor electronics. Parallel/serial interface. Self diagnostics. Paper-out sensor. Uni-directional print speeds to 198 char/sec. DotPlot™ graphics option, with 2K buffer. And more.

For a free brochure or print sample, write or call. Integral Data Systems, 14 Tech Circle, Natick, Massachusetts 01760. (617) 237-7610.

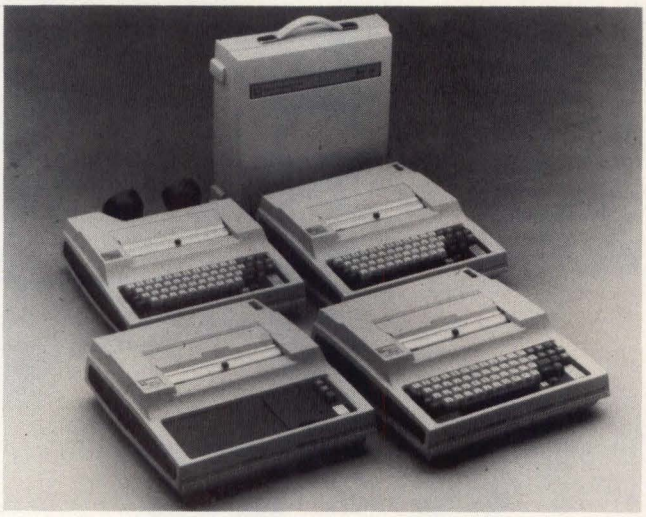
Integral Data Systems, Inc.

*Single unit price. Generous quantity discounts available.

CIRCLE 82 ON INQUIRY CARD

PRODUCTS

Portable Data Analyzer Allows for Parallel Timing And State, Serial State, and Signature Analysis



Data acquisition capabilities for state and timing logic analysis, serial data analysis, and signature analysis are combined in the model 308 data analyzer. Parallel timing and state analyzers each provide 8 channels at 20 MHz with a 252-bit/channel memory size. An 8-channel parallel word recognizer offers internal triggering at recognition of a preset digital-system state. With an optional word recognizer probe, this can be expanded to 24 channels. A memory window provides magnification for viewing timing displays. The serial state analyzer acquires 5-, 6-, 7-, or 8-bit/char data synchronously or asynchronously. 2-char word recognition provides internal triggering upon recognition of preset digital-system state.

Digital delay counts up to 65,535 plus, and data can be stored at sample intervals of 50 ns to 200 ms for the parallel timing and state analyzers and at rates of 50 to 9600 baud for the serial state analyzer. Stored data can be displayed on a self-contained 4" (10-cm) TV type CRT screen in timing format for the timing analyzer and in binary, hex, and ASCII formats for the state analyzers. The signature analyzer provides data input, start/stop gating inputs, and a 20-MHz clock input. A sequence of data between start and stop gates is connected to a 4-digit alphanumeric code and displayed as a 4-digit signature. Built-in self-test on power-up plus 7 levels of diagnostic routines enable the operator to verify the operation of all data analyzer functions. For further information, write on letterhead to **Tektronix, Inc,** PO Box 500, MS 76-260, Beaverton, OR 97077.

120-Char/s Thermal Printing Data Terminals Feature Dual-Matrix Printhead

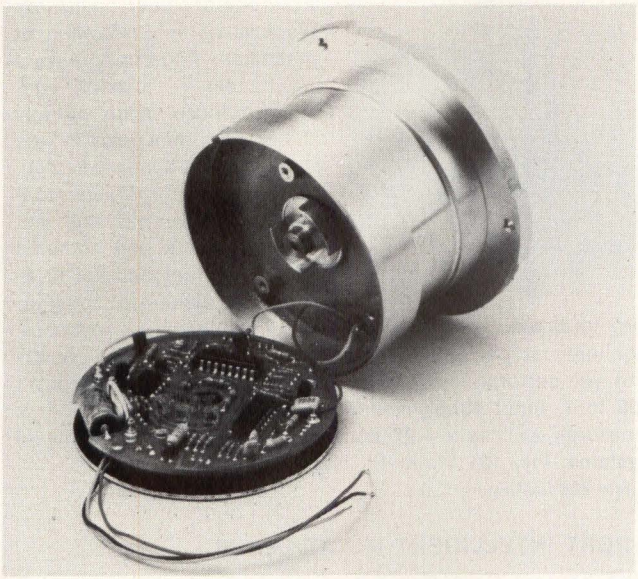
Silent 700™ 780 series includes model 781 receive-only (RO) printer, model 783 keyboard send-receive (KSR) data terminal, model 785 portable data terminal, and model 787 portable communications data terminal. All use a dual-matrix printhead that offers expanded printing capabilities, while providing virtually silent thermal printing. Two 5 x 7 dot matrix characters are printed with each movement of the printhead across the page. Std features include 120-char/s optimized bidirectional printing, full-duplex operation, receive buffer for data overflow protection, and answerback memory capable of storing up to 21 characters in nonvolatile memory for terminal identification to the host computer. A full 128-char ASCII set and a preprogrammed self-test diagnostics capability to automatically verify power-up, parity checks, and maintenance diagnostics are also std. The operator has last-character-printed visibility while inputting data.

RO and KSR desktop models communicate at from 110 to 9600 bits/s, and offer 1000-char receive buffer and EIA/dc-current loop interface as std features. The RO printer has an integral operator control keypad for reference and control of parity selection, interface assignments, communications speeds, and self-test diagnostics capability, and offers an optional 2000-char receive buffer. Each of the portable terminals weighs 17 lb (7.7 kg). The 785 includes an internal 1200-bit/s acoustic coupler while the 787 has a direct-connect internal originate/automatic answer modem with automatic speed selection. The latter also features a "hang-up" command to disconnect telephone communications with the host computer or network communication. Both portable terminals offer an optional RS-232 interface for communication at rates from 110 to 9600 bits/s. **Texas Instruments Inc,** PO Box 1444, M/S 7784, Houston, TX 77001.

Circle 203 on Inquiry Card

PRODUCTS

Brushless DC Motors Drive Discs Directly

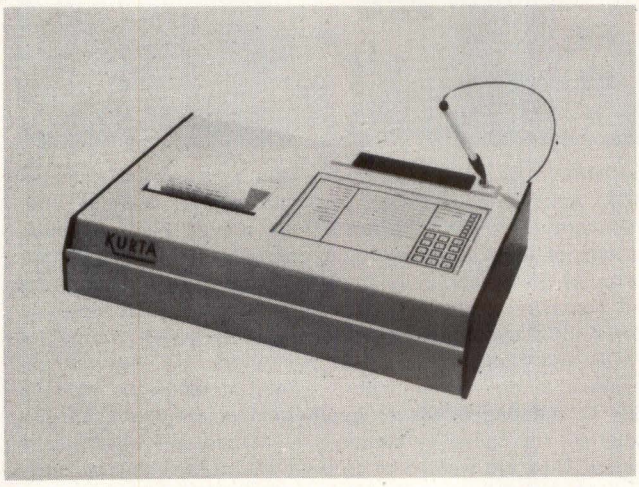


Advantages claimed for 3ϕ Sextant brushless dc motors over comparable ac induction motors include elimination of intermediate belt drives to each disc spindle; more exact speed control (regulated by integral solid state circuitry) to achieve higher bit density; very low power consumption and, therefore, low heat generation (about half that of comparable ac motors); improved reliability resulting from simplified construction; and compact size. The motors are electronically commutated with PM rotors and, because they are driven by dc, may be used anywhere in the world, regardless of international power variations or local ac characteristics. Preset closed loop servo speed controls protect the drives against local voltage fluctuations. In addition, dc construction simplifies acceptance by safety agencies such as UL, CSA, VDE, and BSI. The motors are small enough to be enclosed in the center hole of a standard 8" (20-cm) disc. They achieve head flying speeds quickly (1500 r/min in 3 s), and have torque ratings of 2 to 50 oz-in (0.014 to 0.35 N•m) typ at 3600 r/min and 150 oz-in (1.05 N•m) peak. First production units are 3.5" (8.9 cm) in dia and 2.5" (6.4 cm) long. **Rotron Inc,** Woodstock, NY 12498.

Circle 204 on Inquiry Card

Intelligent Electronic Writing Tablet Data Terminal Accepts Ordinary Handwriting

Instead of a conventional keyboard for entering data into a computer, the Quil™ terminal incorporates an intelligent electronic writing tablet. In write mode, with a sheet of paper placed on the tablet surface, the terminal outputs data to a computer directly or over std telephone lines, and simultaneously produces hard copy for the user on a thermal printer built into the system console. In mark-sense or menu mode, the system's emulation capability is used to input data as the operator checks off items on a preprinted form placed on the tablet surface, employing the pen that is part of the system. The system accepts such check mark inputs as if they were detailed keyboard entries. Inputs can be stored or used to create a CRT display or a hardcopy printout at a local or remote location. Sketches, drawings, diagrams, and signatures can be generated. **Kurta Corp,** 2202 S Priest, Bldg 102, Temple, AZ 85282.



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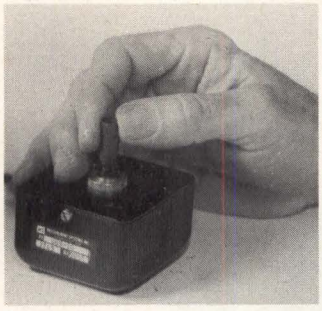
For General Information Circle 83
For Detailed Specifications Circle 84

PRODUCTS

FORCE OPERATED 2-AXIS JOYSTICK CONTROL



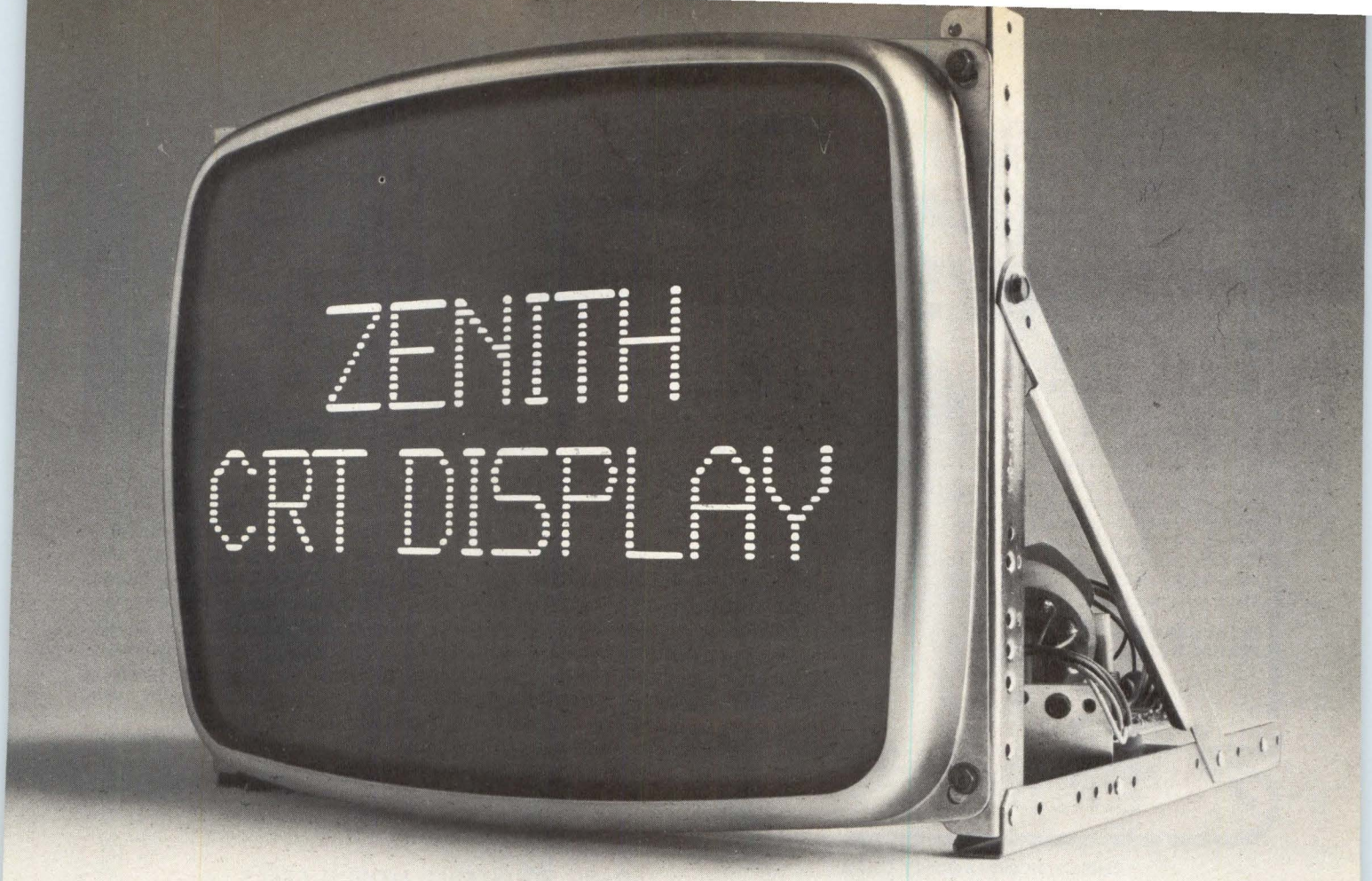
For cursor positioning on displays or in positioning of machines, fingertip pressure on handle of joystick control produces pulse outputs that vary continuously in rate in proportion to applied force. Model 869 incorporates model 469 miniature 2-axis isometric joystick and compact redesign of model 31C10 2-axis pulse generator; together they form readily mountable device for console or keyboard. Nonlinear output pulse rate permits operator to slew rapidly and yet perform fine positioning. Dynamic control range is 500 to 1. Input supply voltage is 5 Vdc at 160 mA. Module measures 2.5" sq x 1.2" deep (6.4 x 3.0 cm). **Measurement Systems, Inc,** 121 Water St, Norwalk, CT 06854.
Circle 206 on Inquiry Card

4-PORT INTELLIGENT MULTIPLEXER

Data Express DE-4 is a 4-port microprocessor based intelligent multiplexer that features total data transparency, ARQ error correction, and fast propagation of data. Unit concentrates up to 4 synchronous devices onto a single line, making use of otherwise wasted terminal idle time. Terminal speeds, parity, and word lengths are selectable by terminal port. Each terminal can run at speeds up to 9600 bits/s for an aggregate of 38,400 bits/s. Composite speed can be synchronous up to 19,200 bits/s. Buffering allows terminal data to temporarily exceed the composite network, allowing the unit to handle a data rate that exceeds modem speed. **Compre Comm, Inc,** 51 E Chester, Champaign, IL 61820.
Circle 210 on Inquiry Card

HIGH ENERGY LITHIUM PRIMARY BATTERIES

Available in AA, C, D, and button versions, bromine complex (BCX), solid cathode (SCS), and high temperature (HiT) batteries are designed to provide high power levels for long periods of time under extreme operating conditions. Lightweight, high power cells in BCX system serve electronics and communications industries, providing long life portable power. SCX system serves as keep alive power source for CMOS and NMOS memory in computers. HiT devices are designed to deliver continuous power at temps as high as 150 °C, meeting needs of geothermal environment. Lithium batteries are cased in stainless steel and are hermetically sealed. They are welded in an inert gas at atmospheric pressure. **Electrochem Industries, Inc,** 9990 Wehrle Dr, Clarence, NY 14031. Circle 208 on Inquiry Card



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Quality is what has made Zenith famous for over sixty years and number one in the television industry. It's that quality, that commitment to excellence—that insures the reliability of every product we make.

Our manufacturing facilities, laboratories, equipment, procedures, experience and know-how give you the quality and reliability that you look for in a CRT Display. A CRT Display that will hold up under really tough operating conditions.

And to all this, our people add the personal service and special attention you want from your CRT Display source.

Exhaustive testing

Our testing insures that every component operates to exacting Zenith standards. Exhaustive computer analysis, electron microscope and thermograph scan tests are only a sample of what we do.

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Every CRT Display we design has our customers in mind. Before our engineers even begin new circuit layouts, we'll meet with you and find out what your exact needs and specifications are.

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Components in the CRT Display are designed with reserve capacity for low maintenance and continued reliability.

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Important Zenith Features

The Zenith CRT Display is precision engineered. No linearity controls are required and the CRT Display's vertical and horizontal synchronization is automatic.

The Zenith CRT Display frame can be adjusted to virtually any angle you want. This will satisfy many customer requirements without having a frame custom designed.

But we do welcome the opportunity to meet all your special requirements.

Zenith tradition

At Zenith we'll make sure you get the same service, quality and reliability in your CRT Display that we've been giving our customers for over sixty years.

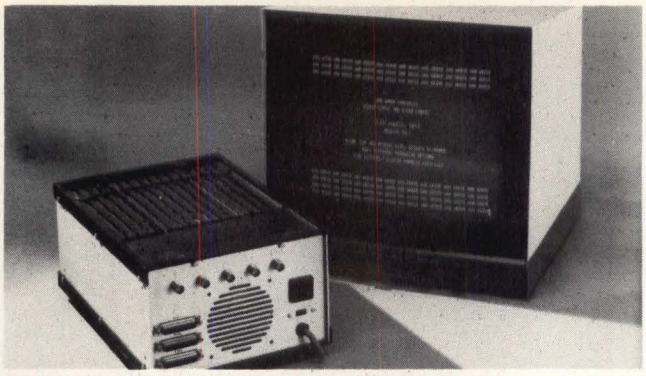
For further information and specifications, write CRT Display Engineering Division, Zenith Radio Corporation, 1000 Milwaukee Avenue, Glenview, Illinois 60025, or call 312-773-0074.

ZENITH®

The quality goes in before the name goes on.

CIRCLE 87 ON INQUIRY CARD

RECEIVE-ONLY TERMINALS AND CONTROLLERS



With 7-bit interface, units are software compatible with the company's product line but add several features. R1680-Compat and R2480-Compat have std display formats of 16 lines of 80 char and 24 lines of 80 char, respectively. 8 lines of 32 char, 16 lines of 32, and 24 lines of 40 char formats are available for longer viewing distances. Blink, dim, and reverse video accents are std for highlighting purposes. Test mode permits display of the full 128-char ASCII set to facilitate system debugging. Absolute cursor addressing is std; other commands include erase screen; cursor home, return, up, down, right, and left; and set roll or page display mode. Cursor is a blinking field. **Ann Arbor Terminals, Inc,** 6107 Jackson Rd, Ann Arbor, MI 48103.

Circle 209 on Inquiry Card

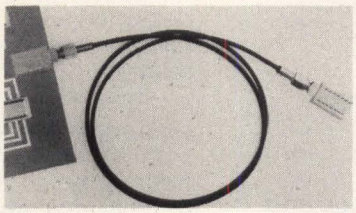
BOARD MOUNTABLE LITHIUM CELLS

Eternacell[R] lithium cells are available in 4 std sizes from 0.5 to 1.9 Ah for PCB mounting. Providing continuous power of 5 to 20 μA for up to 10 yr, cells are suited for CMOS memory standby applications. Simple diode isolation to other voltage sources allows the steady 2.9 V/cell to maintain memory circuits from short-term brownout to years of standby service. Rugged hermetic seal construction, coupled with high energy density, allows for storage and operation from −40 to 160 °F (−40 to 71 °C). Cells can be wave soldered with conventional manufacturing techniques. **Power Conversion Inc,** 70 MacQuesten Pkwy S, Mount Vernon, NY 10550.

Circle 207 on Inquiry Card

LOW PROFILE FIBER OPTIC LINKS

Fiber optic transmit/receive modules in Skini-DIP, 0.295″ (0.75-cm) high DIPs can be used on 0.5″ (1.27-cm) centers. Links built using these 14-pin modules and appropriate fibers are good for transmissions of more than 2 km. Digital links specified from dc to 30M bits/s, with a bit-error rate of better than 10^{-11}, can be produced using the MDL4777-SKP pair. Transmitter can inject more than 200 μW into low loss single-fiber cable at data rates to 30M-bits/s. Receiver is a PIN-diode photodetector followed by two cascaded transimpedance amps. Receiver can drive 6 TTL loads with output rise fall time of 5 ns. Min threshold power at the specified bit-error rate is 2 μW. **Meret, Inc,** 1815-24th St, Santa Monica, CA 90404.



Circle 211 on Inquiry Card

Can you imagine if everyone tried to communicate at once?

We can.

We're Telcon Industries. We've been solving the problems of format and protocol conversions worldwide for ten years.

We can solve your communications problem with a complete turnkey system of format and protocol conversion hardware and software on a lease or purchase basis. No matter what data communications task you have, rely on Telcon for the most efficient, economical system deliverable today and ready for tomorrow.

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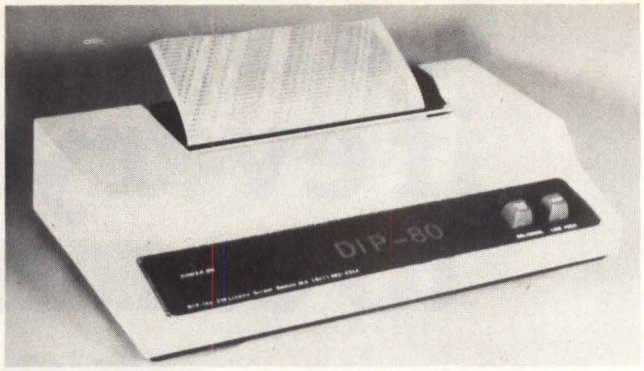
London: 76 Shoe Lane • Suite 307 • London, England • EC4A3JB • 01-353-6621

CIRCLE 90 ON INQUIRY CARD

DOT MATRIX IMPACT PRINTER



DIP-80 features 7 x 7 or 14 x 7 matrix printing, u/lc char set, 100-char/s bidirectional printout, roll or fanfold paper, cartridge ribbon loading, and 3.5″ (8.9-cm) profile. Complete with microprocessor electronics, unit interfaces directly with mini and microcomputers. With full 96-char ASCII set, it is capable of both u/lc printing at either 80 or 96 char/line on 8.5″ (21.6-cm) wide paper. Std unit incorporates a 2-line char buffer. Paper feed, at 1 line/s, is accomplished with friction roller. Operator controls include power, select/deselect, and line feed. Interface options include Centronics compatible parallel, RS-232-C serial, or 20-mA current loop. **DIP, Inc,** 210 Lincoln St, Boston, MA 02111.
Circle 212 on Inquiry Card

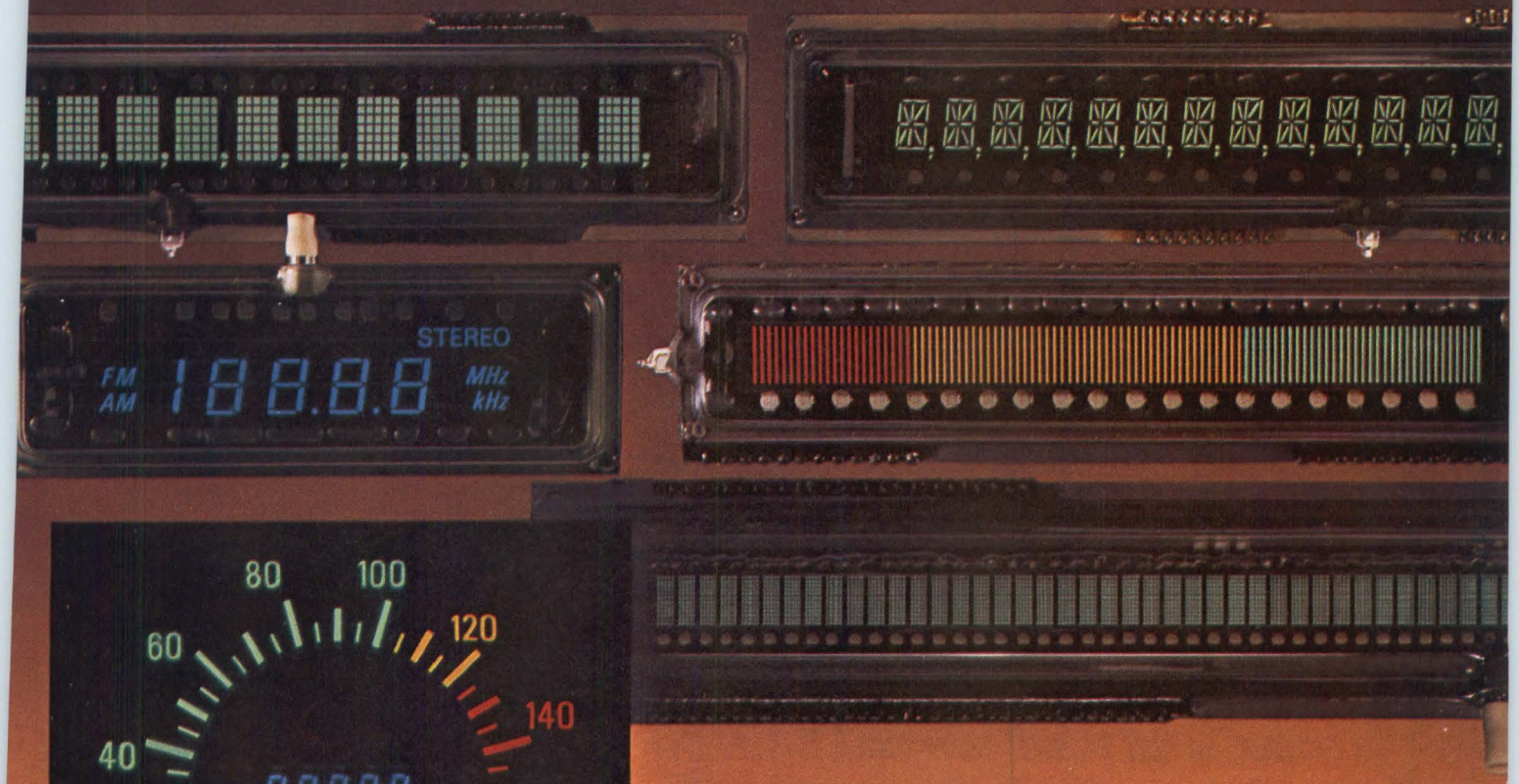
TAPE SYSTEM FOR IEEE 488 INTERFACE BUS

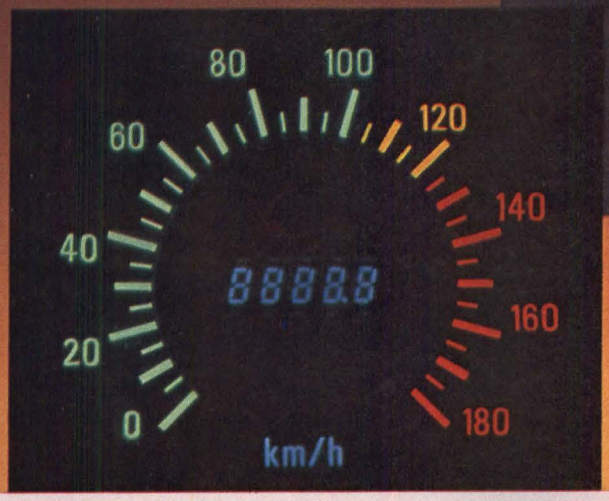
Model GPIB-1050 operates with or without a general purpose interface bus system controller, permitting data recording with IEEE 488 intelligent devices. Rugged and operationally simple, the complete subsystem is embedded within the tape transport. It provides dual-density 9-track, 45-in/s (114-cm/s) operation, in either NRZI or PE mode, storing 30M bytes of data on a 2400′ (731-m) reel. Transparent to HP or Tektronix desktop computer, system generates and reads IBM/ANSI and ECMA compatible 0.5″ (1.27-cm) magnetic tape in binary, ASCII, and/or EBCDIC code. Additional features include dual 2048-byte buffers, 20k-byte/s data transfer rate, and 7- or 9-track read-after-write. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117. Circle 213 on Inquiry Card

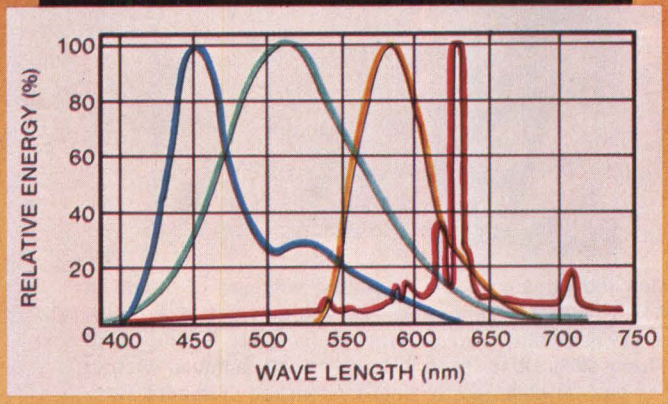
NONIMPACT PRINTER FOR FORMS, TEXT, AND GRAPHICS

Designed for use with 2640 graphic and alphanumeric terminals, 9825 and 9835 desktop computers, and other computer systems, the 7310A prints up to 500 lines/min. Built-in paper cutter and stacker automatically trims paper to 8.5 x 11″ (21.6 x 27.9 cm) or to European A4 std; it can be programmed to cut page lengths of any size from 2 to 20″ (5 to 50 cm). Text forms and graphics are printed as they appear on the display. Included is a full 128-char fixed space ASCII set, proportional spaced ASCII set, and an HP Roman extension set. Graphics resolution is 100 dots/in (40/cm). Raster encoded data are printed at up to 12,500 dots/s. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304. Circle 214 on Inquiry Card

Make your readouts outstanding with the latest Itron innovations.







Multi-color configurations. Red, blue, yellow and blue-green arrays. 5 x 12 dot matrices for upper/lower case alphanumerics and 5 x 7 dot matrix displays. High density dot and bar graphic panels. 14-segment alphanumeric units. These latest, and all the other Noritake Itron advancements, are sure to open up new readout innovation opportunities for you.

And you'll realize all the advantages offered by Itron Fluorescent units over ordinary digital displays. Their cost-effective pricing and simple, fast installation will save you time and trouble, as well as a great deal of money. Interfacing with peripheral circuits is easy too; further reducing costs. They operate at low voltage and consume little power. Their bright fluorescent output and flat-glass packages make for easy readability, at a distance and at wide viewing angles, even under high ambient light conditions.

What's more, Itron displays have a proven long-life track record for reliable performance under stringent conditions. And we can quickly and economically fabricate custom configurations. Since there's much more you should know to make an optimum display selection, contact us for all the particulars.

itron®

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INTERNATIONAL REPRESENTATIVES

WEST GERMANY: Neumuller GmbH, Eschonstr 2, 8021, Taufkirchen, Munich Phone. 089/6118-245 Telex. 522106

FRANCE: Europavia, France, 5 Avenue Leon Harmel 92167 Antony Cedex Phone. 666-21-10 Telex. 42204381

UNITED KINGDOM: ITT Meridian, West Road, Harlow, Essex CM20 2BP Phone. 0279-35351 Telex. 817202

SWEDEN: AB Nordqvist & Berg, Box 9145 S-10272, Stockholm Phone. 08-690400 Telex. 10407

HONG KONG: Phone. 5-232420 TAIPEI: Phone. 351-0293

Circle 93 for Sales Contact

NORITAKE ELECTRONICS, INC.

L.A. OFFICE: 22410 Hawthorne Boulevard, Torrance, CA 90505, (213) 373-6704, Telex: 67-4910

N.Y. OFFICE: 41 Madison Avenue, New York, NY 10010, (212) 481-3440, Telex: 12-5469

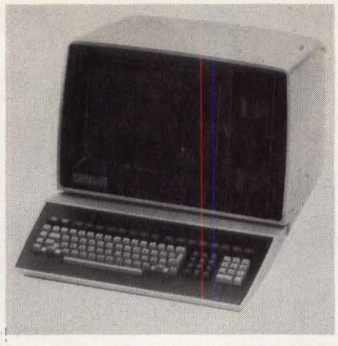
NORITAKE COMPANY, LIMITED

JAPAN: 1 - 1 Noritake Shinmachi, Nishiku, Nagoya-Shi, (052) 561-7111, Telex: J59738

EUROPE: Burotel Belgium SA, Rue de la Presse 3-5, 1000 Bruxelles, (02) 217-83-60, Telex: 4626962

Circle 94 for Literature Only

INTELLIGENT USER PROGRAMMABLE CRT TERMINAL

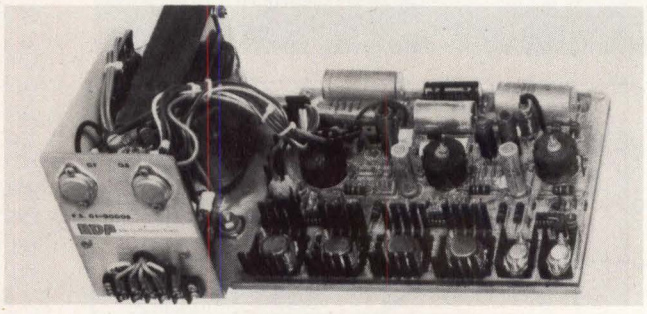


Upgraded ZMS-70 offers dual-density diskettes and Business BASIC. Minidiskettes increase online storage capacity to 268k bytes with transfer rate of 250k bits/s. Built-in disc controller operates in autonomous DMA mode and may read or write data in either single- or double-density mode concurrently with the normal functioning of the microprocessor. Controller allows for addition of 2 5 or 8" (12.7 or 20.3 cm) diskette drives. Users may write programs in extended version of BASIC and run them through the ZOS/70 operating system which incorporates system resources in a set of interactive, preprogrammed software routines. Language extensions allow interactive use of CRT and keyboard. **Zentec Corp,** 2400 Walsh Ave, Santa Clara, CA 95050. Circle 215 on Inquiry Card

INTELLIGENT PERIPHERAL PROCESSORS

Disc processor and magnetic tape processor operate independently and in parallel with CPU, allowing I/O and other CPU processing to occur concurrently. Both are designed for use with 32 series computers and the MPX-32 operating system, and provide fast, efficient I/O processing for up to 4 disc or tape units. Disc processor features include 16M-byte addressing capability, independent disc I/O processing, queueing of disc I/O operations, command and data chaining, error correction code, overlapped seeks and angular position targeting, and dual-port operation with full software support. Tape processor features 16M-byte addressing, command and data chaining, and error detection and correction. **Systems Engineering Laboratories, Inc,** 6901 W Sunrise Blvd, Fort Lauderdale, FL 33313. Circle 216 on Inquiry Card

5-OUTPUT REGULATED SWITCHING POWER SUPPLY



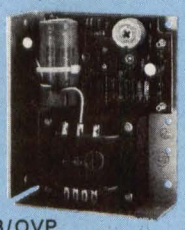
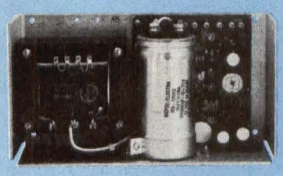
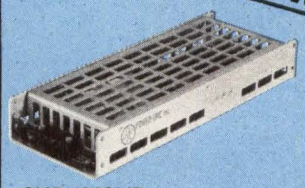
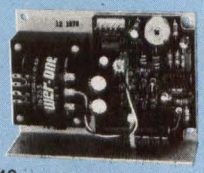
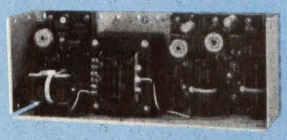
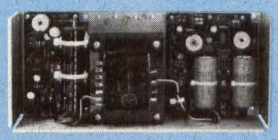
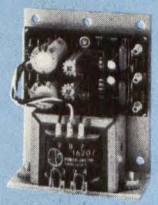
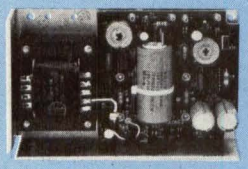
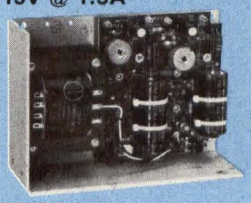
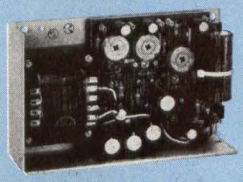
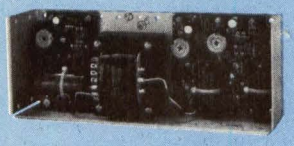
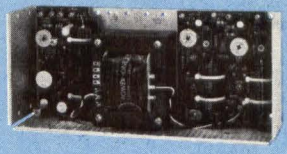
Providing individually regulated output voltages of 5 Vdc at 8 A, ±12 Vdc at 2 A each, and ±24 Vdc at 1.5 A (4 A pk for 30 ms at 30% duty cycle), module features regulation of ±1% from 25% load to full load on all outputs. Output voltages can be changed to meet custom requirements. Considerably smaller and lighter than conventional power supplies, the units require less power and generate less heat. The supply provides for either ac (115/230-Vac) or dc (36-V battery) uninterruptible service with automatic switchover in event of power failure or dip. Measuring 13 x 5 x 8" (33 x 13 x 20 cm), units can be configured to meet virtually any space requirement. **Electro Dynamics Power,** Rising Sun Rd, Bordentown, NJ 08505. Circle 217 on Inquiry Card

POWER-ONE D.C. POWER SUPPLIES

Now available for small systems applications

Power-One, the leader in quality open-frame power supplies, now offers a complete line of single, dual, and triple output models for small computer systems. Also available are special purpose models for Floppy Disk and Microcomputer applications.

Below are just a few popular examples of the over 90 "off the shelf" models now available from stock.

SINGLE OUTPUT & LOGIC POWER SUPPLIES • 56 "off the shelf" models • 2V to 250V, 0.1A to 40A • ± .05% regulation • 115/230 VAC input	**5V @ 3A, w/OVP**  HB5-3/OVP $24.95 single qty.	**5V @ 12A, w/OVP**  HD5-12/OVP $79.95 single qty.	**5V @ 40A, w/OVP** NEW  SK5-40/OVP Switching Model $250.00 single qty.
FLOPPY-DISK SERIES • 8 "off the shelf" models • Powers most popular drives • Single/dual drive applications • 2-year warranty	**5V @ 0.7A, w/OVP** **12V @ 1.1A/1.7A PK** NEW  CP340 For one 5.25" Media Drive $44.95 single qty.	**5V @ 1A, w/OVP** **−5V @ 0.5A, w/OVP** **24V @ 1.5A/1.7A PK**  CP205 For one 8.0" Media Drive $69.95 single qty.	**5V @ 2.5A, w/OVP** **−5V @ 0.5A, w/OVP** **24V @ 3A/3.4A PK**  CP206 For two 8.0" Media Drives $91.95 single qty.
DUAL OUTPUT MODELS • 15 "off the shelf" models • ±5V to ±24V, 0.25A to 6A • I.C. regulated • Full rated to +50°C	**12V/15V @ 0.25A** NEW  HAD12-.25/HAD15-.25 $32.95 single qty.	**5V @ 2A, w/OVP** **9 − 15V @ 0.5A**  HAA512 $44.95 single qty.	**±12V @ 1.7A or** **±15V @ 1.5A**  HBB15-1.5 $49.95 single qty.
TRIPLE OUTPUT MODELS • 10 "off the shelf" models • 5V plus ± 9V to ± 15V outputs • Models from 16W to 150W • Industry standard size	**5V @ 2A, w/OVP** **± 9V to ± 15V @ 0.4A**  HTAA-16W $49.95 single qty.	**5V @ 3A, w/OVP** **±12V @ 1A or** **±15V @ 0.8A**  HBAA-40W $69.95 single qty.	**5V @ 6A, w/OVP** **±12V @ 1.7A or** **±15V @ 1.5A**  HCBB-75W $91.95 single qty.

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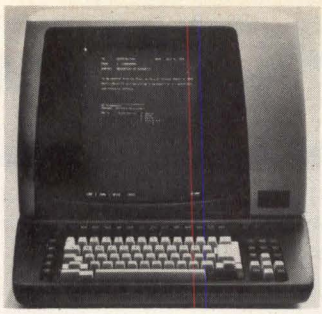
CIRCLE 97 ON INQUIRY CARD

WORD PROCESSING SYSTEM CRT DISPLAY



In addition to a nonglare, full page screen, the W105 display for use on Wordstream™ word processing systems offers a status line which shows typing position, typamatic (automatic repeat) keys, operator selectable automatic word wraparound, and an improved Selectric style keyboard for easier operator training and use. Status line at the bottom of the display continuously shows diskette drive number, line number, and character position. Typamatic keys speed cursor positioning, character and word deletions, and movement of lines and columns on the screen. Automatic word wraparound is totally controlled by the operator. Control keys are located above the keyboard in a single line. **Wordstream Systems Group, Basic Four Corp,** 300 E 44th St, New York, NY 10017.

Circle 218 on Inquiry Card

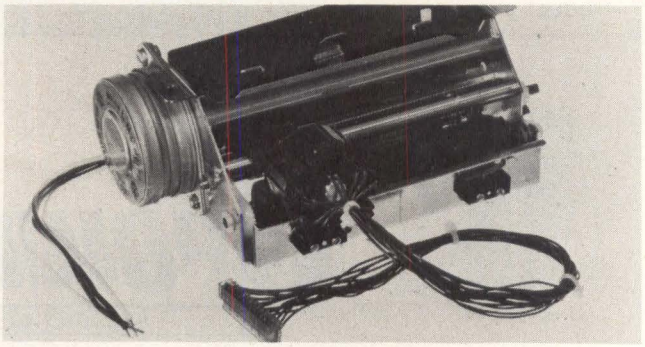
MICROPROCESSOR BASED LOGIC ANALYZER

LA5000, a cost-effective alternative to the 100-MHz, 16-channel K-100D, is a microprocessor based instrument with keyboard control, automatic self-test, integral CRT display, active probes, sophisticated recording capabilities, and powerful data analysis modes. Designed to operate at a max data rate of 50 MHz, using 4 channels of input and storage capability of 1024 words of memory, the analyzer can be expanded to 8 channels at 25 MHz and 512 words of memory, or to 16 channels at 12.5 MHz and 256 words of memory. Operating modes include sample and latch; timing diagram displays; data domain displays in binary, hexadecimal, or octal; data comparison mode; and graph mode. **Gould Inc, Biomation Div,** 4600 Old Ironsides Dr, Santa Clara, CA 95050.

Circle 219 on Inquiry Card

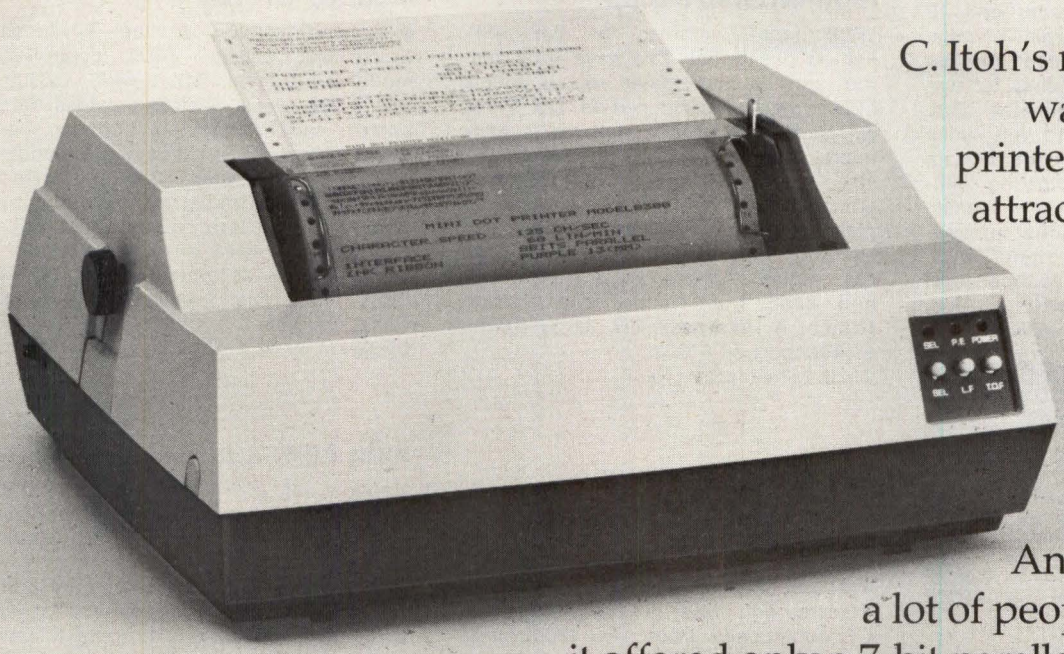
40-COL DOT MATRIX IMPACT PRINTER MECHANISM

Using same design techniques as 80-col version, 40-col impact printer mechanism features long life ribbon cartridge, small size, and high reliability. Measuring 2.5 x 7 x 5″ (6.4 x 17.8 x 12.7 cm), the unit operates at 2 lines/s and its continuous duty head has a min life of 100M char. Options include stepper motor paper control, adjustable tractor feed for continuous forms, and right to left printing. A split paper version provides independent paper advance for audit journal. Applications include POS terminals, electronic cash registers, personal and small business computer systems, as well as instrumentation and industrial uses. **Two-Day Corp,** 1915 W Glenoaks Blvd, Glendale, CA 91201.



Circle 220 on Inquiry Card

Only one printer is equal to our Model 8300P.



C. Itoh's model 8300 was one, fine printer. It was an attractive, quiet, low-cost unit with a straightforward, reliable design. And although a lot of people liked it, it offered only a 7-bit parallel interface.

Our 8300R.

So when we created our new 8300 Series Printers, we not only made them better, we gave you a choice: the 8300R has an RS-232C designed to interface at rates up to 9600 Baud with a 20/40/60 mA current loop; and the 8300P designed with a 7-bit parallel interface. Both feature a continuous-duty 7-wire head with a life expectancy of 100 million characters, and both print bi-directionally in 80 columns of crisp, 9x7 dot matrix at 125 CPS. An 132 column format with condensed print capability is also available. Both accept multi-ply pin-feed paper in any width from 4.5" to 10"; paper can be loaded from the bottom or rear; and the print position line is easily adjustable. Both our 8300P and our 8300R are still attractive, quiet, low-cost units with straightforward, reliable designs. Because both are still from C. Itoh. Of course.

C. Itoh Electronics, Inc.

Write or call for detailed specifications.

5301 Beethoven Street, Los Angeles, CA 90066
Call: (213) 390-7778 • Telex: WU 65-2451

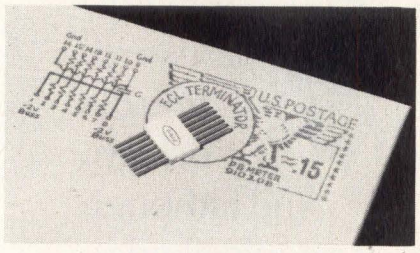
East Coast
666 Third Avenue, New York, NY 10017
Call: (212) 682-0420 • Telex: WU 12-5059

C. Itoh is part of the 119-year-old C. Itoh and Co., Ltd., worldwide trading organization.

CIRCLE 100 ON INQUIRY CARD

ECL TERMINATOR

A 0.1-μF decoupling capacitor and 12 thick film resistors in 16-pin flatpack network eliminate the need for an extra component by providing for capacitance within the terminator. ECL signals may have rise and fall times of 1 ns or less, and under certain conditions all signals terminating within the network may switch in phase. Filtering the bus close to the terminator prevents crosstalk in signal lines, thus maintaining proper voltage level during transients. **Dale Electronics, Inc,** PO Box 74, Norfolk, NE 68701.



Circle 253 on Inquiry Card

SINGLE-BOARD CLOCK MODULE

A plug-in half-board module for Perkin-Elmer/Interdata computers incorporates a precision interval clock and a line frequency clock together with power fail/auto restart hardware. Universal Clock Module, a direct replacement for the Perkin-Elmer M48-000, generates program selected time intervals of 1 μs, 10 μs, 100 μs, and 1 ms. A program-controlled count of 0 to 4095 can be stored to yield interrupt intervals from 1 ns to 4.095 s. **Macrolink,** 1740-E S Anaheim Blvd, Anaheim, CA 92805.

Circle 221 on Inquiry Card

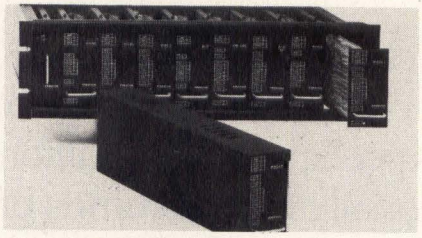
PUSHBUTTONS WITH HIGH INTENSITY LEDS

"Full face" versions of the AML lighted pushbutton line have total button surface illuminated by a single LED. Lamps are housed in std T-1¾ wedge base adapters. Half life is 100k hours. Addition of LED to pushbutton also eliminates shock and vibration damage, ends the need for lamp replacement, and reduces power consumption. Red, amber, and green lamps are available in projected, transmitted, and dead front color styles. **Micro Switch, A Honeywell Div,** 11 W Spring St, Freeport, IL 61032.

Circle 222 on Inquiry Card

PRIVATE LINE MODEM

Bell compatible P-202T, online compatible with Western Electric 202T data set series, operates at 1200 bits/s over unconditioned 3002 private lines. Transmission rate is 1400 bits/s on C1 conditioned lines and 1800 bits/s on C2 conditioned lines. Simplex and half-duplex operating modes are available on 2-wire circuits, with a full-duplex capability on 4-wire circuits. The modem features std RS-232-C interface and nom telephone line termination of 600 Ω. **Prentice Corp,** 795 San Antonio Rd, Palo Alto, CA 94303.



Circle 223 on Inquiry Card

MILITARIZED STORAGE MODULE SYSTEM

Militarized version of the Advanced Electronics Design 8000 controller, model 3353, meets MIL-E-5400, -16400, and -4158 specs. System provides data control and intermediate buffering between processor and its storage module disc drives. Model 3354 militarized storage module drive, manufactured by Control Data Corp, operates in MIL-E-16400 and -4158 environments, storing 67M bytes of formatted data. **ROLM Corp,** 4900 Old Ironsides Dr, Santa Clara, CA 95050.

Circle 224 on Inquiry Card

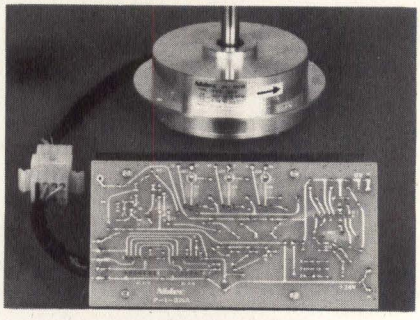
HIGH POWER DC SUPPLIES

Capable of 300-, 600-, and 1200-W outputs, Brute series supplies provide high current, continuously adjustable dc in 2- to 25- and/or 5- to 50-Vdc ranges. The units operate from 105 to 130 and/or 210 to 260 Vac at 47 to 63 Hz, and provide outputs filtered to 1% or 500 mV rms max and regulated to ±0.1%. Op temp range is 0 to 55 °C with convection cooling; units operate to 65 °C with 25% derating. **Adtech Power, Inc,** 1621 S Sinclair St, Anaheim, CA 92806.

Circle 225 on Inquiry Card

BRUSHLESS DC MOTORS

Ceramic rotor in OEM motors eliminates the need for rare earth metals; pancake construction uses conventional PM rotor and stator windings with either wye or delta connections. Units are available in 2-, 4-, 6-, or 8-pole designs. Specs for F-2401 and F-4001 are preferred voltage of 24 and 40 V, rated current of 2.3 and 4.9 A, rated torque of 8 and 28 oz-in (0.056 and 0.196 N•m), and starting torque of 27 and 110 oz-in (0.189 and 0.77 N•m), respectively. **Nidec America Corp,** 1821 University Ave, St Paul, MN 55104.



Circle 226 on Inquiry Card

Inventory reports

Point-of-sale

Data entry

Environmental control

Financial reports

Computer graphics

Sylvania breaks the color barrier.

Introducing America's first 19-inch color data display tube.

Not just a tube with color.

A tube with gorgeous, glorious, sharp Sylvania color.

Color that provides clearer images and better contrast than anything available anywhere.

Color that makes small characters a breeze to read, with less fatigue.

Crystal clear color created by a high density tri-dot mask.

Color sharpened by a multiple-beam electron gun and enhanced by a Chromatrix dark surround negative guard band, and a rare earth phosphor system.

Sylvania color.

It's completely changed the picture in data display tubes.

Write Product Marketing Manager for our latest catalog:

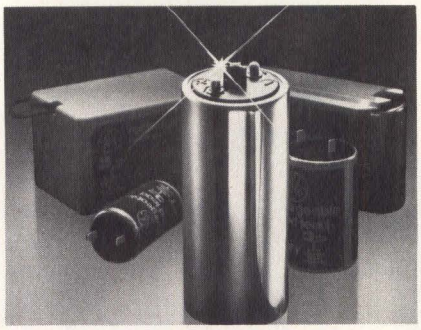
GTE Sylvania
Data Display Tube Division
700 North Pratt Street
Ottawa, Ohio 45875

SYLVANIA | GTE

CIRCLE 102 ON INQUIRY CARD

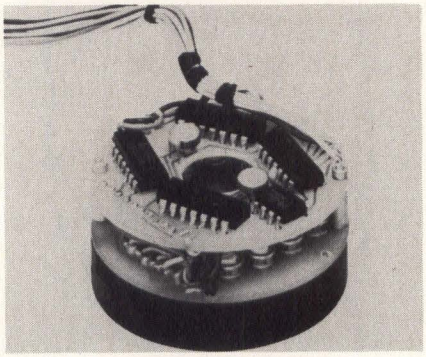
10-Ah SEALED LEAD CELL

Cylindrical sealed lead battery serves as a power source for many standby, portable, and cyclic demanding applications. Termination is improved with threaded heavy duty stud terminals along with high current carrying interconnecting links. Special barrier on cell cover between the stud terminals minimizes accidental short circuits. Extended discharge capability with low internal resistance is featured. **General Electric,** Suite 301, 2100 Gardiner Ln, Louisville, KY 40205.



Circle 227 on Inquiry Card

MODULAR ABSOLUTE OPTICAL ENCODERS



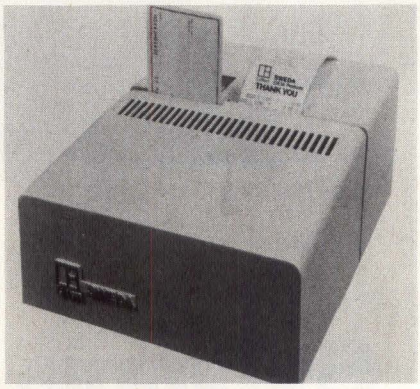
With resolution as high as 12-bits Gray code or 0-999 XS-3 BCD, encoder outputs are normally TTL compatible or can be supplied in CMOS or DTL format. Terminations are available as pigtails, cables with or without connectors, or terminals. Factory prealignment eliminates the need for phasing adjustments while the encoder is being installed. **Trans-World Instruments, Inc, Optical Encoder Div,** 700 E Mason St, Santa Barbara, CA 93103.
Circle 228 on Inquiry Card

PC BOARD LED ASSEMBLY

Eliminating the hard wiring in front panel displays, LED mount combines P-C-Lite with Cliplite in an assembly that allows either vertical or horizontal mount of std T1-¾ LEDs on PC board. When this assembly is used breakdown does not occur until an electrostatic discharge of 15k to 16k V is applied. Lens portion of assembly is available in 5 transparent colors: red, green, amber, yellow, or clear. **Visual Communication Co,** PO Box 986, El Segundo, CA 90245.
Circle 229 on Inquiry Card

2-STATION ALPHANUMERIC DOT MATRIX PRINTER

Basic mechanism of model MR-1824 has a printhead with bi- or unidirectional capability. Independently operated lefthand station prints up to 18 char at 12 char/in (5/cm) at a speed of 1.4 lines/s. Line spacing is 5.4 lines/in (2.1/cm). Out of paper sensor, top or left slip or form insertion, and automatic paper take-up spool are std. Righthand station prints up to 24 char at 12 char/in (5/cm) at a speed of 1.4 lines/s. **Sweda International, Inc, OEM Products,** 34 Maple Ave, Pine Brook, NJ 07058.



Circle 230 on Inquiry Card

HIGH SPEED SYNCHRO TO DIGITAL CONVERTERS

Patterned after the 168F series, the 168L series accepts frequencies to 10 kHz. 10-, 12-, and 14-bit configurations have resolutions to 0.352, 0.088, and 0.022°, respectively, and offer max tracking rates from 10,800 to 129,600°/s at a reference frequency of 2600 Hz. Converters are capable of acceleration rates from 22,000 to 3,-159,000°/s². Accuracies vary from ±4 min ±0.9 LSB to ±30 min depending on resolution. **Control Sciences, Inc,** 8399 Topanga Canyon Blvd, Suite 303, Canoga Park, CA 91304.
Circle 231 on Inquiry Card

ROLM'S 1602B: An Army Standard Computer Designed for Full Integrated Logistics Support

IT'S A COMPLETE PROCESSOR IN A SINGLE 20" CHASSIS.

The 1602B (AN/UYK-19) has space for 7 I/O modules, control panel interface, CPU and 64K of directly addressable memory. An additional 15 I/O slots can be made available with ROLM's 2150 Expansion Chassis.

IT HAS SINGLE SIDED ACCESS.

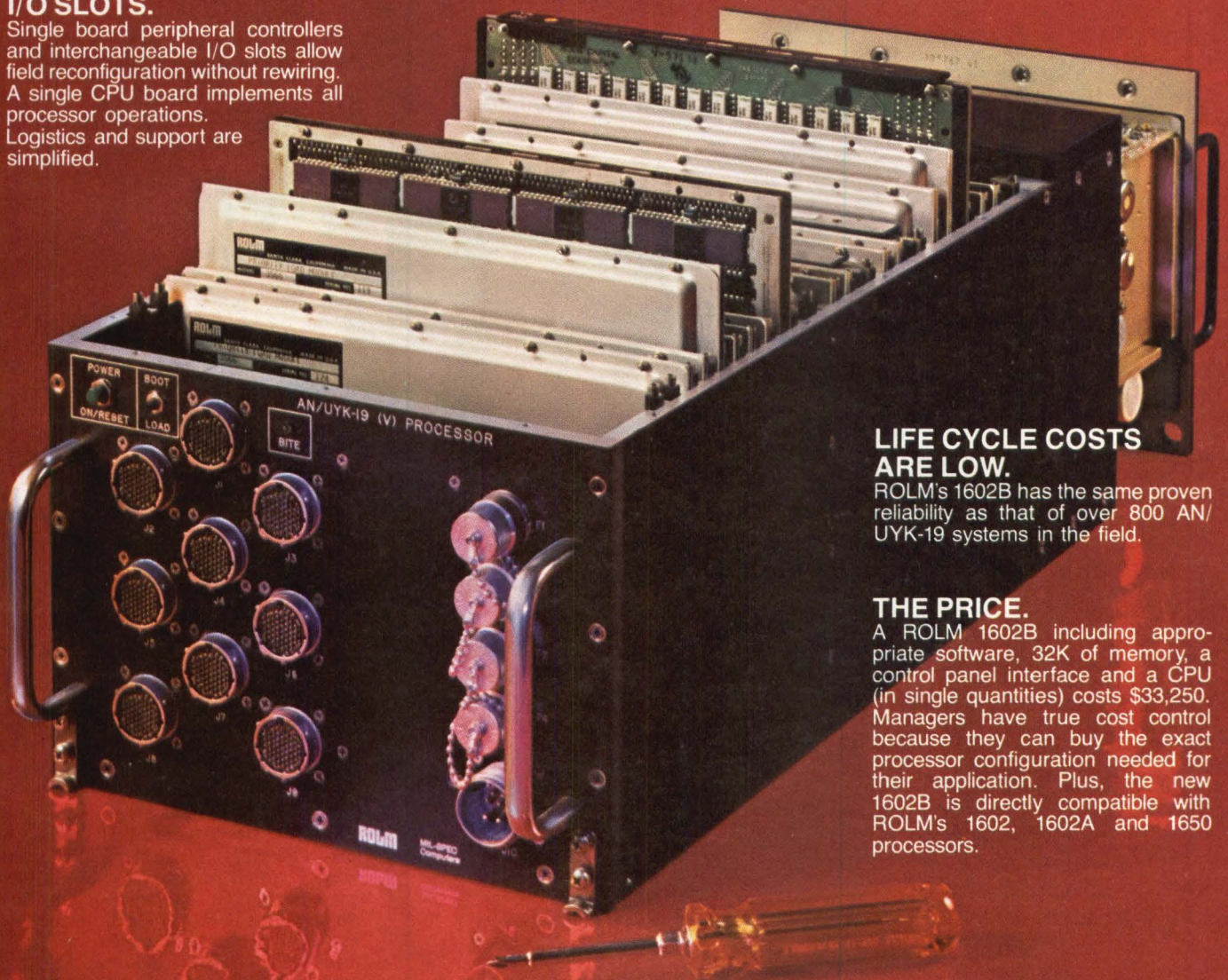
Maintenance is simplified by quick, easy access to the interior of the conductively cooled chassis. The 1602B also has a new plug-in AC or optional DC power supply.

EXCELLENT DELIVERY WITH FULL SUPPORT.

Since AN/UYK-19 processors are in continuous production, delivery is no problem. They are fully mil-qualified and backed up by complete training and documentation. And ROLM's extensive software has really impressed program managers. They find that our total support program can't be matched.

INDEPENDENT CARDS & INTERCHANGEABLE I/O SLOTS.

Single board peripheral controllers and interchangeable I/O slots allow field reconfiguration without rewiring. A single CPU board implements all processor operations. Logistics and support are simplified.



LIFE CYCLE COSTS ARE LOW.

ROLM's 1602B has the same proven reliability as that of over 800 AN/UYK-19 systems in the field.

THE PRICE.

A ROLM 1602B including appropriate software, 32K of memory, a control panel interface and a CPU (in single quantities) costs $33,250. Managers have true cost control because they can buy the exact processor configuration needed for their application. Plus, the new 1602B is directly compatible with ROLM's 1602, 1602A and 1650 processors.

That's Why We're #1 in Mil-Spec Computer Systems

ROLM MIL-SPEC Computers

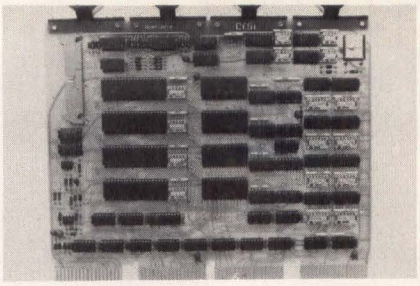
4900 Old Ironsides Drive, Santa Clara, CA 95050. (408) 988-2900. TWX 910-338-7350.

In Europe: Muehlstrasse 19 D-6450, Hanau, Germany, 06181 15011, TWX 4-184-170.

See us at AFCEA Western Conference, Anaheim, Jan. 9-11.

CIRCLE 104 ON INQUIRY CARD

MULTIPLE SERIAL LINE CONTROLLER FOR PDP-8

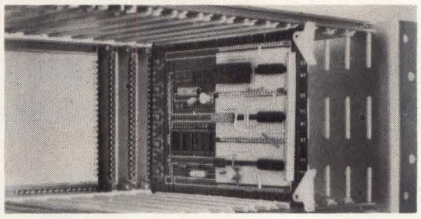


Equivalent to 4 independent KL8J asynchronous line controllers on a single quad PC board, the Quadart interfaces a PDP-8 and 4 asynchronous devices. Each channel has independent device code selection for the transmitter and receiver, 13 baud rate selections, and UART control DIP switches. Other switch selectable functions are number of data bits; odd, even, or no parity; number of stop bits; and RS-232 or 20-mA format. **Computer Extension Systems, Inc,** 17511 El Camino Real, Houston, TX 77058.
Circle 232 on Inquiry Card

ADD-IN MEMORY FOR VAX-11/780

PINCOMM 780S, a semiconductor RAM module, is pin compatible with the VAX-11/780 and requires no modification to existing DEC hardware or system cabling. Memory card capacity is 256k bytes (32k x 64 + 8 ECC); error correction bits provide single-bit error correction and double- or multiple-bit error detection. RUN LED indicates memory is being accessed; an online/offline switch allows memory to be switched offline to aid in troubleshooting. Socketed RAMs with 2 onboard spares ease field repair. **Trendata/Standard Memories,** 3400 W Segerstrom Ave, Santa Ana, CA 92704.
Circle 233 on Inquiry Card

PROTOTYPING CIRCUIT CARD



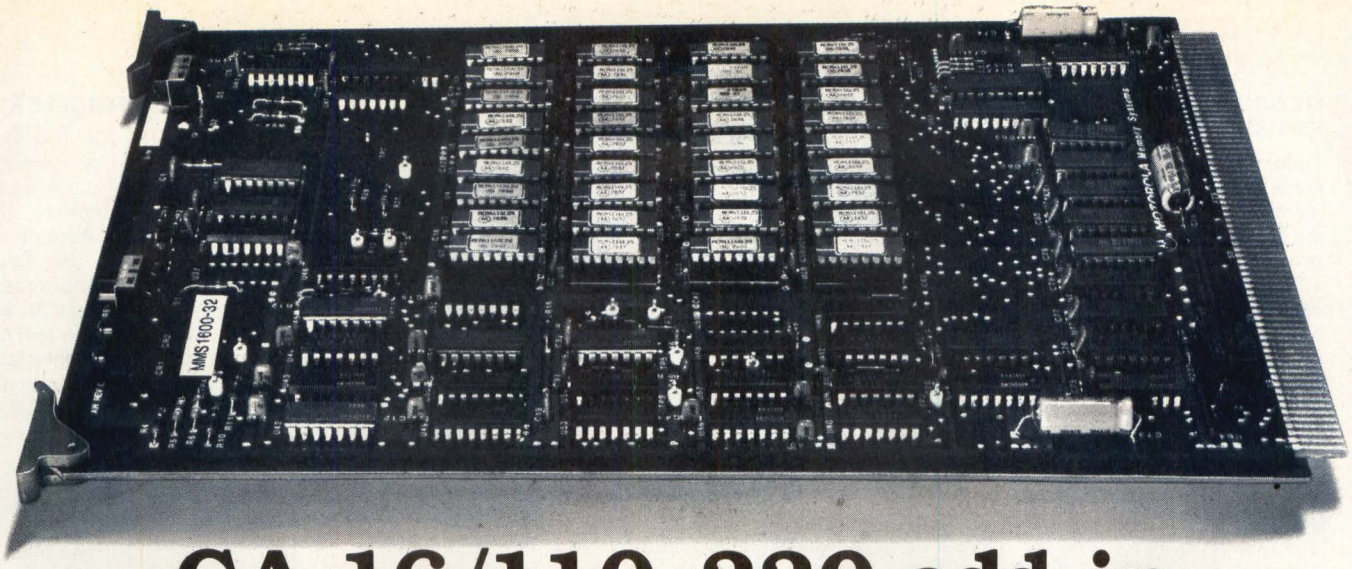
With areas for soldered and wrapped wiring, as well as patchboard terminal blocks, 3677-2B, an FR4 epoxy glass composite board, has 0.042" dia holes on 0.1" grid. Up to six 16-pin, three 40-pin, or combination of DIPs and discrete devices may be mounted on permanent wiring section. Six nylon blocks with 144 quads, each with 4 common patch points, are also installed on the 4.5 x 6.5" board. **Vector Electronic Co,** 12460 Gladstone Ave, Sylmar, CA 91342.
Circle 234 on Inquiry Card

MICROPROCESSOR BASED GPIB CONTROLLER

Compatible with instruments using the IEEE 488 bus and std data communications equipment, the microprocessor based model 609 is a small computer functioning as an industrial grade GPIB controller. Users write BASIC programs into a 4k RAM; Blast instruction transfers programs to an internal P/ROM, eliminating tape loading routines. Control features include serial or parallel poll and reception of BCD or ASCII messages. **Physical Data, Inc,** 8220 SW Nimbus Ave, Beaverton, OR 97005.

Circle 235 on Inquiry Card

Technological leadership.



GA 16/110, 220 add-in. Another fully-compatible memory from Motorola. Now.

The MMS1600. It's Motorola's hardware- and software-compatible add-in for users of General Automation's 16/110 and 220.

So good it's warranteed for a full year. You get that rare combination of high performance and low cost with the assurance of quality. It's the add-in GA system users have been wanting but probably couldn't get.

The MMS1600 has the speed you look for, with a fast 400 ns maximum read access time and a minimum cycle time of just 450 ns. The low typical power consumption of 0.9 A and a worst-case drain of only 1.6 A @ +5 V make it a great system power saver. And, there's nothing like the extra 5° in the wide 0°C to 55°C operating temperature range for providing a cushion of reliability.

Four board configurations provide excellent design flexibility. Choose between the basic 32K-word × 16 and 16K-word × 16 sizes, or use either of the 32K-word × 18 and 16K-word × 18 parity option versions.

Small (1–9) quantity prices are low at $1350 for the 16K-word × 16 and just $1800 for the 32K-word × 16 memory. Yes, OEM discounts are available. Get the MMS1600 off-the-factory-shelf, now.

Add-ins for a broad range of popular systems.

Motorola add-ins are available for every PDP*-11 model, and for LSI-11 systems. We also provide board-level memory for SBC80/10, 80/20 and MDS† systems as well as for a variety of M6800-based systems.

Our expert design/production team generates custom systems, large or small, to meet any need.

All Motorola add-in memories are backed by comprehensive warranty and factory service plans, full testing, 100% burn-in and engineering support in the field. Highly competitive prices and fast delivery complement the broad line and system advantages.

For MMS1600 information, write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

To learn more about the complete add-in line, contact your Motorola sales office or authorized distributor.

In memory systems as in semiconductor components, Motorola leads the way with

Innovative systems through silicon.

MOTOROLA INC.

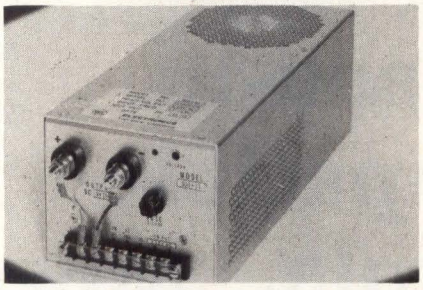
*Trademark of Digital Equipment Corporation.
†Trademark of Intel Corp.

CIRCLE 106 ON INQUIRY CARD

PRODUCTS

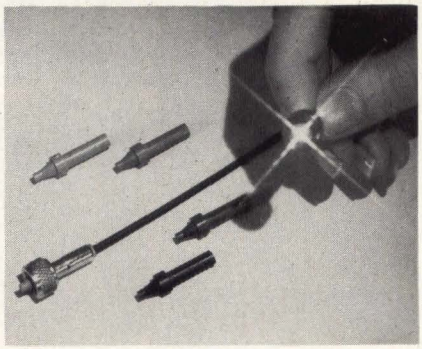
MEDIUM POWER SWITCHING SUPPLIES

Tight line regulation (0.1% max) and close load regulation (0.15% max) are features of 375 W SD series supplies. Inputs required are 115 and 230 Vac; brownout protection ranges are 97 to 127 Vac and 194 to 254 Vac—15 to 10% of center voltages. Overvoltage and overload protection, ac power fail signal, and internal thermal cutoff are std. Units provide 5 Vdc at 75 A, 12 Vdc at 32 A, and 24 Vdc at 16 A with efficiencies of 80 to 85%. **KEC Electronics, Inc,** 21535 Hawthorne Blvd, Torrance, CA 90503.



Circle 236 on Inquiry Card

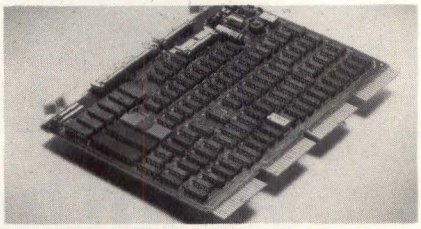
FIBER OPTIC CONNECTOR FOR 125-μm CABLES



Connector accepts plastic-clad silica, all-glass step index, and all-glass graded index optical fibers as small as 125-μm dia. Termination mates with a splice bushing, a bushing that can house TO packaged sources and detectors, and a metal housing for Motorola electro-optic semiconductors. Connector related insertion loss is <2 dB. Metal connector body provides emi/rfi shielding for critical receiver circuitry. **AMP Inc,** Harrisburg, PA 17105.
Circle 237 on Inquiry Card

QUAD SIZE DISC CONTROLLER

Soft sector format of DQ-200 provides up to 20% more capacity through variable sector size and number of sectors/track. Controller interfaces any 2 removable media or Winchester drives with SMD interface in one Qbus card slot. Included are a microprocessor and all electronics for operation, automatic self-test firmware diagnostics, and interface through SMD interface cable to both LSI-11 and any industry std disc. **Distributed Logic Corp,** 12800-G Garden Grove Blvd, Garden Grove, CA 92643.



Circle 238 on Inquiry Card

LARGE CAPACITY HARD DISC SYSTEM

Incorporating SA4000 disc drives, model 604 controls up to 4 Winchester technology drives, providing 116M bytes of storage. The system stores 14.5M or 29M bytes per unit (unformatted), transfers 7.1M bits/s, has a MTBF of 5k power-on hours (typ), and mounts in a 19" (48-cm) RETMA rack. Interfaces are available for Hewlett-Packard 2100, 21MX, and 1000 series and for DEC LSI-11 and PDP-11 series. **Dicom Industries, Inc,** 715 N Pastoria Ave, Sunnyvale, CA 94086.
Circle 239 on Inquiry Card

MICROPROCESSOR BASED MODEM

Bell compatible MX 48A/B operates at 4800 bits/s and provides leased line and dial operation capabilities into one unit, which is line compatible with either 208A or 208B or equivalent modems. Leased line multipoint, point to point, and dial applications are supported. Fault isolation and error detection capabilities quickly locate and correct system malfunctions to minimize network downtime. **Codex Corp,** 20 Cabot Blvd, Mansfield, MA 02048.

Circle 240 on Inquiry Card

There's a bright new face in 12" data monitors.

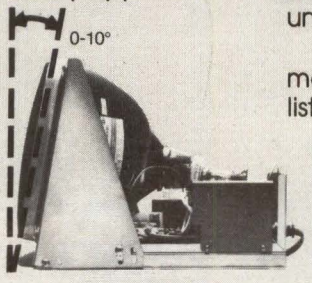
If you've got a need for a 12" CRT monitor, Sanyo has a model that will fill it.

For cost-sensitive applications, choose the 5000 series. You get your choice of AC or DC power, P4 or P31 phosphors, and separate or composite video and sync inputs. 15 MHz bandwidth and standard 15.75 kHz scan rate provide excellent resolution and easy application.

For extra-demanding jobs, pick the 6000 series. You get 1,000 line resolution and 22 MHz bandwidth for ultra-sharp graphics and crisp, high definition 80-character lines. TTL-compatible sync inputs make interfacing a snap.

With either series, you get a compact, rugged steel chassis with adjustable CRT tiltback to fit virtually any enclosure design. You also get adjustable scan size, plus remote brightness control capability. Single-PCB construction and one-connector hookup save time in assembly, testing, and maintenance. And Sanyo's many years of manufacturing field-proven CCTV monitors, and our unparalleled QC assure long, trouble-free service.

For all the facts on these exciting new open-chassis monitors, contact your local Sanyo sales representative listed below.



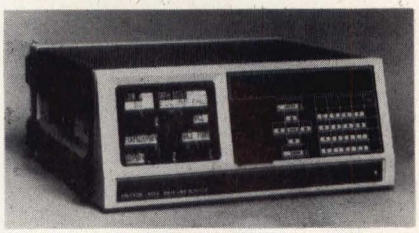
SANYO

Communications Products Division
1200 W. Artesia Blvd., Compton, CA 90220 (213) 537-5830

CIRCLE 108 ON INQUIRY CARD

Contact your nearest Sanyo rep:
AKRON: Avcom, Inc. (216) 777-2060 **ATLANTA:** Len Elliott Company (404) 875-9701 **ATLANTIC CITY:** Austin Associates (609) 871-9290 **BALTIMORE:** David H. Brothers, Inc. (301) 764-7189 **BOSTON:** Piper Associates (617) 449-1144 **CHICAGO:** George Petit Company, Inc. (312) 261-0342 **DALLAS:** The Crockett Sales Co. (214) 748-8209 **DENVER:** Mile-High Marketing (303) 457-2058 **DETROIT:** Burcaw Co. & Associates (313) 533-7700 **INDIANAPOLIS:** Midwest Rep. & Assoc., Inc. (317) 844-4555 **KANSAS CITY:** Pacer Sales Corporation (816) 358-6638 **LOS ANGELES:** Marketing Specialists (213) 341-1471 **MIAMI:** L. Haas Company (305) 945-6544 **PORTLAND:** Earl & Brown Co., Inc. (503) 245-2283 **SAN FRANCISCO:** Tech-Rep Associates (415) 785-4531 **SEATTLE:** Earl & Brown Co., Inc. (206) 284-1121 **ST. PAUL:** Skor, Inc. (612) 645-6461 **WHITE PLAINS:** Irving Langbaum Assoc., Inc. (914) 634-1141

DATA MONITOR



Plug-in-and-use 802A accommodates data rates from 50 to 19.2k bits/s, with optional capability to 56k bits/s. Its 7″ (18-cm) CRT displays up to 1024 char. Capabilities include statistical error analysis, storage capacity to 64k bytes, display of continuous key configuration parameters, and automatic turnaround time measurement. Basic transmitting capability permits polling of terminals or sending a block of just-received data to terminal or printer. **Halcyon, Inc,** 2121 Zanker Rd, San Jose, CA 95131.
Circle 241 on Inquiry Card

DOUBLE-DENSITY FLOPPY DISC INTERFACE

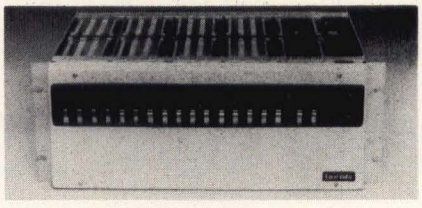
Basic input/output system (BIOS) software for CP/M operating systems, provided on a single-density diskette, permits intermixing of single- and double-density diskettes. The system automatically determines whether single- or double-density is in use. As many as 4 drives can be selected. The 8″ (20-cm) Shugart compatible disc interface contains phase-lock loop and write precompensation. **Tarbell Electronics,** 950 Dovlen Pl, Suite B, Carson, CA 90746.
Circle 242 on Inquiry Card

AC-DC POWER SOURCES

Three output voltages—±5, ±12, and ±15 V—with inputs of 115, 220, or 240V ac are offered in line of ac-dc power sources. Packaging options for these supplies are PCB or chassis mounting. Line regulation is ±0.02% for PC mounting units and 0.05% for chassis mounting supplies. Load regulation varies from ±0.02% to ±0.15% depending on output and mounting configurations. Ripple and noise range from 0.5 to 2.0 mV rms. **Reliability Inc,** PO Box 37409, Houston, TX 77036.
Circle 243 on Inquiry Card

2400-BIT/s DIRECT CONNECT MODEM

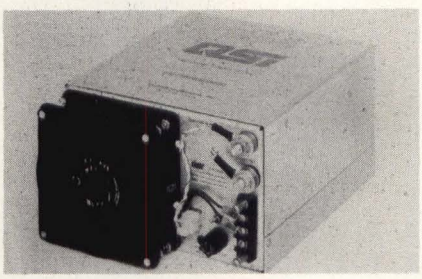
VA2440 is both Bell 201B/C and CCITT compatible. It connects to the switched network by plugging into a std RJ-11C voice jack, or through programmable data jacks (RJ-41S and RJ-445). Designed to operate with Multiline Automatic Calling System (MCAS) which allows up to 60 modems to be accessed from a single dialer, the modem features a switch selectable 75-bit/s and 150-bit/s reverse channel which can also operate as an auxiliary and forward channel. **Racal-Vadic,** 222 Caspian Dr, Sunnyvale, CA 94086.



Circle 244 on Inquiry Card

1-kW SWITCHING POWER SUPPLY

Fast recovery diodes replace Schottky diodes in 8000 series switching supplies. The 5-V, 200-A units supply additional power for large memory computer systems. Forced air cooled 5 x 8 x 11″ (13 x 20 x 28-cm) package yields 2.25 W/in³. Efficiency is greater than 70%, and MTBF is calculated at 43k h. Unit meets VDE 0875 level N for emi suppression. Features include overvoltage and overcurrent protection, remote sensing, and massive heatsinking. **Qualidyne Systems, Inc,** 2256 Main St, Chula Vista, CA 92011.



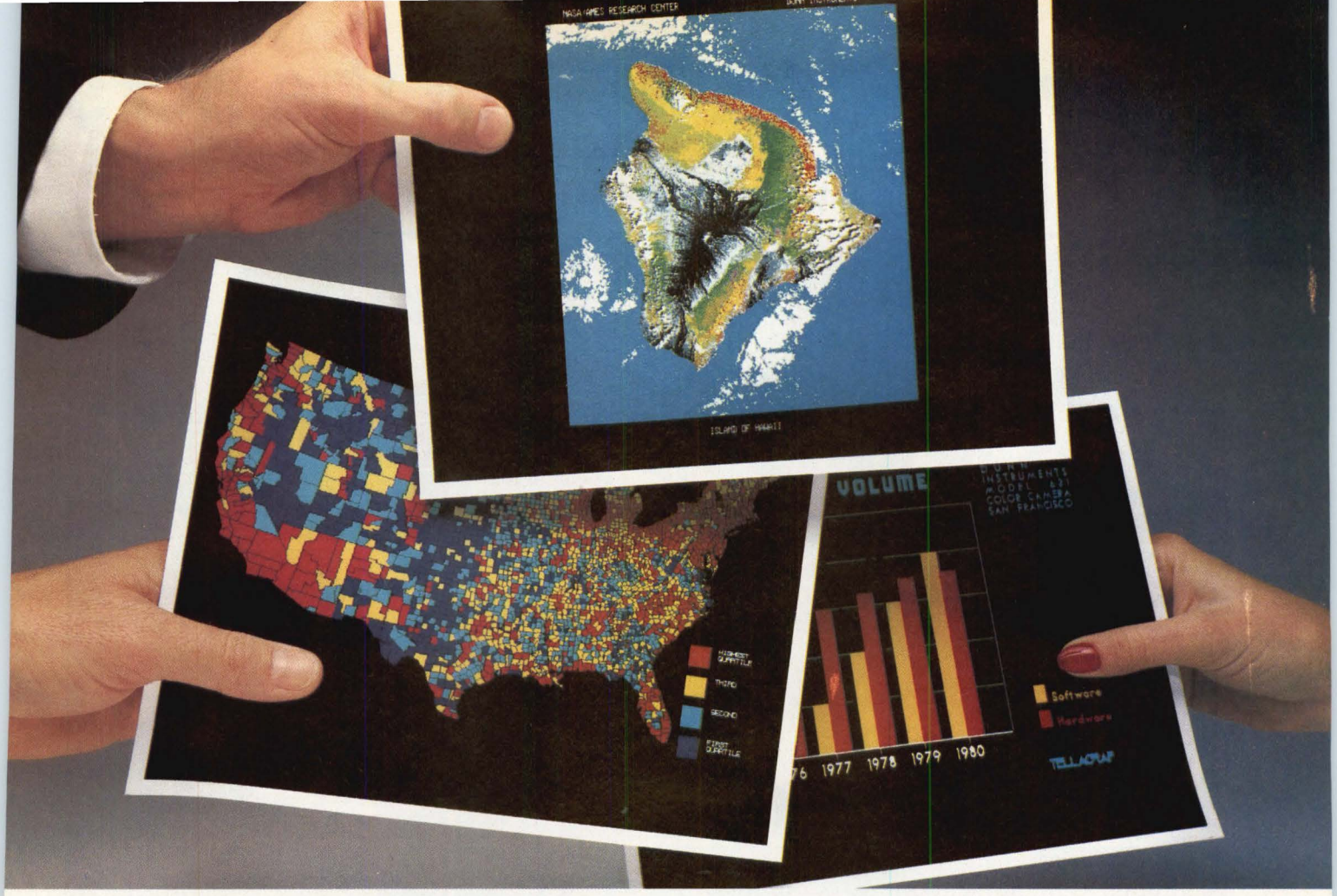
Circle 245 on Inquiry Card

POWER LINE MONITOR

Model 400, providing an indication of memory integrity, gives a visual warning and permanent record of primary ac power conditions caused by brownouts, line surges, and power failures. A flashing light or optional audible alarm indicates a power failure. An inkless chart records line voltages as a function of time for a min of 30 days. Voltage variations of as little as 1 V are recorded on the 90- to 140-V scale with a center scale accuracy of 1%. **Fleischman Electronics, Inc,** PO Box 1235, Montclair, NJ 07042.
Circle 246 on Inquiry Card

INTELLIGENT DISC CONTROLLER

Users of DEC Unibus and Q-Bus processors may store up to 5.4G bytes with models 650 and 550, both of which emulate the RM02/3, RP04/5/6, RK06/7, RP02/3, RS03, and RS04 offered by DEC. Features include transfer to 64k, 3-sector buffer storage, and error detection and correction. The 8.5 x 15″ (21.6 x 38-cm) single-board 650 plugs into any available Hex SPC I/O slot in the host computer backplane; 550 resides on two 8.5 x 10″ (21.6 x 25-cm) PC boards. **Xylogics, Inc,** 42 Third Ave, Burlington, MA 01803.
Circle 247 on Inquiry Card



Actual 631 images on Polaroid instant 8x10 film.

Color hard copy is finally at hand!

Color hard copy: the luminescent electronic image, captured in the permanence of photographic prints and transparencies. Dunn Instruments makes it brilliant, accurate and effortless to obtain from an affordable system. At last you can hold the new computer graphics and digital images in your hands.

The source is the 631 Color Camera System. It packs a high resolution, high linearity CRT, sophisticated optics and microprocessor exposure control into a compact, fast and friendly unit. For instant hard copy for immediate analysis, use it with Polaroid Type 808 film to make stunning 8x10 color prints. Add the optional motor-driven 35mm system for beautiful color slides. Or load 8x10 transparency film and produce images you can project overhead.

The 631 economically records the data from any raster scan CRT, for presentation, reproduction, access and display. Applications range from management information graphics to satellite remote sensing. Call or write for more information. We'll arrange for you to get your hands on actual results from the 631 Color Camera System.

Dunn Instruments, Inc.,
544 Second Street, P.O. Box 77172,
San Francisco, CA 94107.
415/957-1600.

The 631 COLOR CAMERA SYSTEM

"Polaroid" is a registered trademark of the Polaroid Corporation.

LANDSAT image courtesy NASA-Ames Research. Cartographic study courtesy Harvard Laboratory for Computer Graphics. Management information graphics courtesy ISSCO.

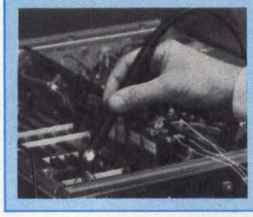
CIRCLE 110 ON INQUIRY CARD

DUNN INSTRUMENTS

Set your COURSE for the 80's

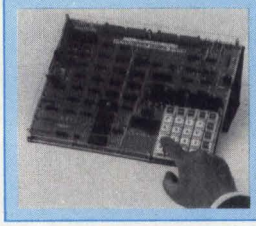
Through Advanced Technical Education from INTEGRATED COMPUTER SYSTEMS, INC.

Course 142—Five Days
Troubleshooting Microprocessor-Based Systems



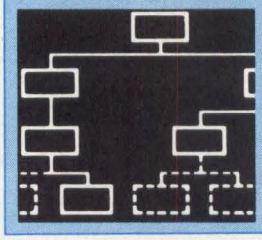
PHOENIX January 21-25
WASHINGTON, DC January 28-February 1
DALLAS February 4-8
DENVER February 11-15
SAN FRANCISCO February 25-29
SEATTLE March 3-7
LOS ANGELES March 10-14
BOSTON March 24-28
SAN DIEGO April 14-18

Course 160—Four Days
Microprocessors & Microcomputers



ATLANTA January 15-18
DENVER January 22-25
LOS ANGELES January 29-February 1
WASHINGTON, DC February 12-15
SAN DIEGO February 19-22
HOUSTON February 26-29
BOSTON March 4-7
SAN FRANCISCO March 25-28
DALLAS April 15-18

Course 320—Four Days
Structured Programming



ATLANTA January 15-18
SAN FRANCISCO January 22-25
WASHINGTON, DC February 5-8
SAN DIEGO February 12-15
HOUSTON March 4-7
SEATTLE March 25-28
LOS ANGELES April 15-18
BOSTON April 22-25
WASHINGTON, DC April 29-May 2

Course 330—Four Days
PASCAL: The Structured Language

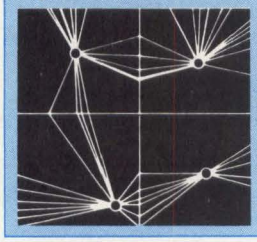
```
10: FUNCTION RFIB(N,LEVEL
11: VAR RF:INTEGER;
12: BEGIN
13:   DOTS(LEVEL);  WRITE
14:   IF N>1 THEN
15:     RF:=RFIB(N-1,LE
16:   ELSE
17:     IF N=1 THEN RF:
18:       ELSE RF:=0;
19:   RFIB:=RF;
20:   DOTS(LEVEL);
21:   WRITELN('LEAVE, N='
22: END(*RFACT*);
```

DALLAS January 22-25
SAN FRANCISCO February 12-15
WASHINGTON, DC March 4-7
LOS ANGELES March 11-14
ATLANTA March 18-21
HOUSTON April 15-18
BOSTON April 29-May 2
SAN DIEGO May 6-9

Course 340—Four Days
Engineering Project Mgmt.

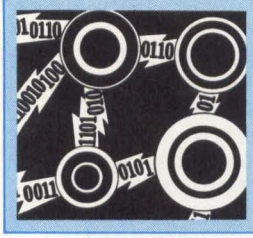
SAN FRANCISCO January 29-February 1
WASHINGTON, DC February 12-15
HOUSTON February 19-22 NEW
ATLANTA February 26-29
SAN DIEGO March 11-14
BOSTON April 15-18
WASHINGTON, DC April 22-25
LOS ANGELES April 29-May 2
SEATTLE May 6-9

Course 350—Four Days
Distributed Processing Systems



SAN DIEGO January 22-25
WASHINGTON, DC February 12-15
ATLANTA March 18-21
WASHINGTON, DC April 29-May 2

Course 355—Four Days
Computer Communication Networks NEW

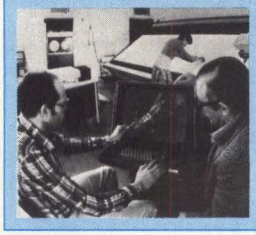


SAN FRANCISCO January 15-18
WASHINGTON, DC February 26-29
DENVER March 4-7
LOS ANGELES March 25-28
ATLANTA April 15-18
BOSTON April 22-25
MINNEAPOLIS May 6-9

Course 365—Four Days
Computer Graphics

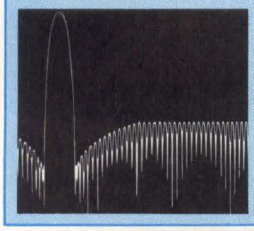
LOS ANGELES January 15-18
HOUSTON January 22-25
PHOENIX January 29-February 1
ATLANTA February 5-8
WASHINGTON, DC February 12-15
SAN DIEGO March 18-21
NEW YORK April 15-18
SAN FRANCISCO April 22-25
BOSTON April 29-May 2

Course 370—Four Days
CAD/CAM NEW



LOS ANGELES January 14-17
WASHINGTON, DC January 21-24
SEATTLE February 25-28
DALLAS March 3-6
SAN FRANCISCO March 17-20
NEW YORK March 24-27
BOSTON April 14-17
CINCINNATI April 21-24

Course 412—Five Days
Digital Signal Processing



HOUSTON January 21-25
WASHINGTON, DC January 28-February 1
PHOENIX February 4-8
SAN FRANCISCO February 11-15
ATLANTA February 25-29
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Course 525A Microcomputer Software/ Hardware

Course 536A Microcomputer Interfacing Techniques

Course 565 Developing Microcomputer Software

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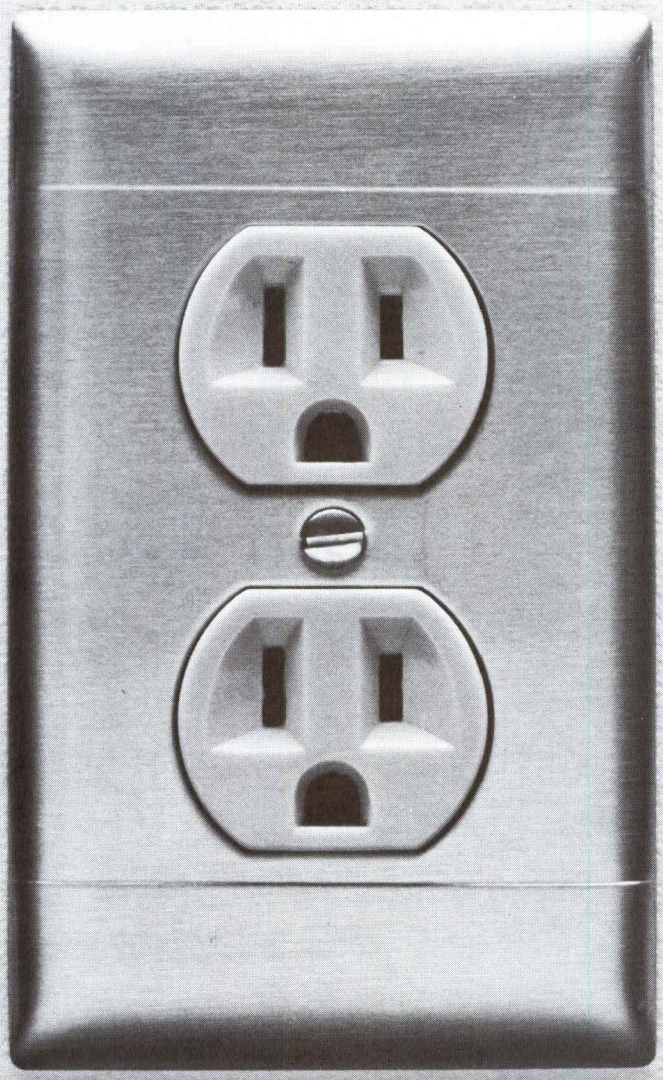
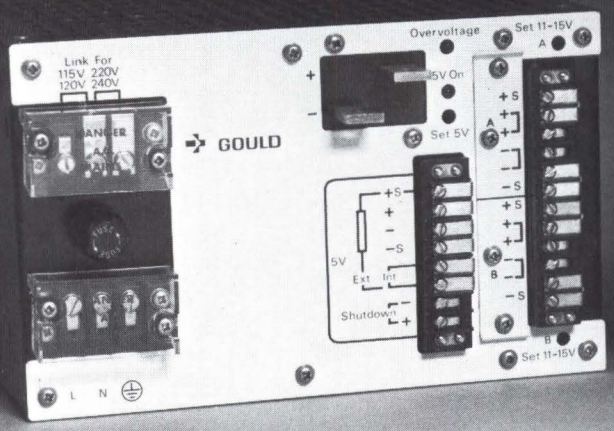


Can your mini handle it?

Gould has 39 ways to make sure.

AC power poses lots of problems for the systems designer: brownouts, dropouts, high-voltage spikes and the day-to-day fluctuations in amplitude and frequency.

That's why Gould makes scores of different switching power supplies for scores of different applications. But minicomputer designers tell us that our MG and SMG series are the ones that best meet their power requirements.



20 MG switchers that meet all international standards.

West Germany's VDE defines the toughest power supply standards in the world. And all MG switchers meet both VDE0804 and VDE0875 curve N, including our miniature MGs (MMG).

MG's top-of-the-line quality and reliability have made it the leading switcher in Europe for years. Now more and more U.S. engineers are designing it in as a solution to international marketing problems.

MG switchers are available in the following output/wattage combinations:

Output voltage	Watts							
	MMG				MG			
	25	50	100	150	200	300	400	500
5	X	X	X		X	X		X
12	X		X					X
15	X		X		X			X
24	X		X		X	X		X
5 & ± 15				X			X	

19 SMG switchers that deliver a low price per watt.

For some applications you may not need the tight specifications of a top-of-the-line power supply. But you need more than the lowest cost units have to offer.

That's exactly where the SMG series was designed to fit. And with a price per watt that's below most other switchers in this broad middle range.

With SMG you get the kind of reliability you would expect in a premium priced unit without paying a premium price.

SMG units are available at 5 volts in the following wattages: 8, 16, 40, 80, 120, 200, 250, 500, 750, 1,500, and 2,250. Twelve and 24-volt versions are available rated at 19, 38 and 96 watts.

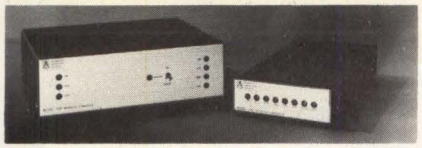
For complete specifications on Gould switchers and a free copy of our short form catalog, circle the reader service number below or contact Gould Inc., Electronic Power Supply Division, P.O. Box 6050, El Monte, CA 91731 (213) 575-4777.

GOULD

An Electrical/Electronics Company

CIRCLE 112 ON INQUIRY CARD.

COMMUNICATIONS INTERFACE CONVERTERS

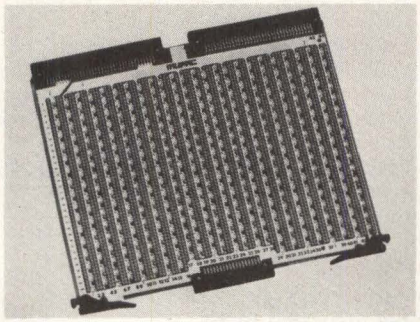


Terminal equipment is connected to communications equipment with incompatible interfaces through use of converters that provide electrical transformation of signal's impedances and voltages as required. Units are transparent to data formats. Operating speed is slaved to the modem clocks or to the terminal clock for externally timed modems. Cables provide mechanical compatibility between the interfaces—1 for terminal equipment and 1 for communications equipment. **Avanti Communications Corp,** Newport, RI 02840. Circle 254 on Inquiry Card

MINICOMPUTER ENCLOSURE

Enclosure offers 24.62″ (62.53-cm) vertical and 30″ (76-cm) horizontal mounting space. Complete unit contains 4 adjustable RETMA rails, screw-on vented rear panel with cable cut-out, vented spot welded sides, and 4 adjustable heavy duty glides. Stand-alone configurations are available, as are a variety of desktops to provide operator work area. Various colors, sheetmetal or Plexiglas doors, and casters are optional. **Computer Furniture & Accessories, Inc,** 1441 W 132nd St, Gardena, CA 90249.
Circle 255 on Inquiry Card

HIGH DENSITY UNIVERSAL PANEL



A 324 size panel maximizes universal rows of socket terminals. Rows of 65 socket terminals in 16 repetitive sections of 0.300″ (0.762 cm) with 0.100″ (0.254 cm) between sections permit packaging of DIL ICs with 0.300″ (0.762-cm) spacing as well as 0.400″ (1.016-cm) spacing. Rows of 62 socket terminals in 4 repetitive sections of 0.300″/0.300″ (0.762 cm) with 0.100″ (0.254 cm) between sections package devices with 0.600″ (1.524-cm) spacing. **Mupac Corp,** 646 Summer St, Brockton, MA 02402.
Circle 256 on Inquiry Card

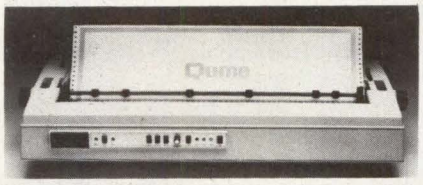
DOUBLE-CAPACITY MINIATURE TAPE TRANSPORT

Miniature tape drive records 4 tracks at 1600 bits/in (630/cm) providing 1.34M-byte unformatted capacity; earlier version of model 200 Minidrive recorded 2 tracks for 672k-byte storage. Drive uses 140′ (43-m), 0.25″ (6.35-mm) magnetic tape. Transport operates at 30 in (76 cm)/s for bidirectional read-write, giving a 6k-byte/s data transfer rate. Rewind and data search at 90 in (228 cm)/s give avg access to stored data in 20 s. 4-track recording heads feature read-after-write capability. **Qantex Div, North Atlantic Industries, Inc,** 60 Plant Ave, Hauppauge, NY 11787.
Circle 257 on Inquiry Card

CRT DISPLAY TERMINAL SOFTWARE

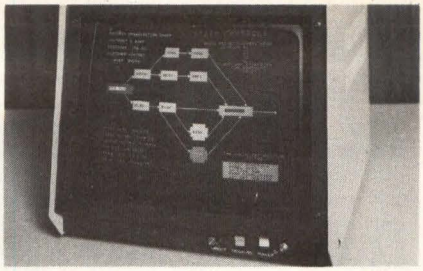
Version 1.7 adds editing features, such as erase to end of line and page, to the InterTube II. The terminal features a high powered text editing system with char and line insert/delete, full and/or block transmit mode, programmable end of line terminators, a self-test mode, and an RS-232-C serial printer port which operates from 50 to 9600 bits/s. Software enables the video display terminal to emulate other CRTs. **Intertec Data Systems Corp,** 2300 Broad River Rd, Columbia, SC 29210. Circle 258 on Inquiry Card

INTELLIGENT WIDE CARRIAGE PRINTER



RS-232-C interface and internal programming allow the Sprint 5 WideTrack™ printer to offer all of the capabilities of the Sprint 5 RO. The WideTrack combines a 264-col printing area and 40-char/s speed. Direct interface capability and an integral switching power supply allow interfacing to any CPU or microprocessor whether local or remote. Built-in microprocessor provides flexible character spacing, precise plotting resolution, and multi-directional carriage slewing. **Qume Corp,** 2350 Qume Dr, San Jose, CA 95150. Circle 259 on Inquiry Card

HIGH RESOLUTION, 13″ COLOR MONITOR



With fixed convergence feature, the 8039 monitor uses an inline gun, fine pitch, shadow mask to achieve resolution. It operates with composite video with RS-170 compatibility or with TTL digital inputs. Scanning frequency capabilities are 15 to 18 kHz horizontal, and 50 to 60 Hz vertical. Resolution is >600 TV lines. Video amplifier has a pulse rise and fall time of 40 ns. Unit is suited to alphanumeric or limited graphics applications. **Aydin Controls,** 414 Commerce Dr, Fort Washington, PA 19034.
Circle 260 on Inquiry Card

COMMUNICATIONS INTERFACE

The 8080A based A/S-1 protocol converter enables most asynchronous terminal devices to imitate the protocol presented by IBM 2770/2780/3780 or 3741 RJE terminals, as well as the 2741 protocol. Asynchronous ASCII is converted to bisynchronous EBCDIC, and vice versa. Asynchronous rates are 110 to 9600 bits/s; bisynchronous rate is determined by the synchronous modem or modem eliminator. BLACK BOX® provides blocking and error checking inherent in the IBM protocols. **Expandor, Inc,** 400 Sainte Claire Plaza, Upper St Clair, PA 15241.
Circle 261 on Inquiry Card

DATA NETWORK DISTRIBUTOR

Two asynchronous devices can operate at the same or different data rates on a single synchronous channel, provided that neither data rate exceeds one-half the main channel data rate, via a TP0212 data distributor. Unit provides individual channel status displays for transmit and receive data. Digital loopback switch permits easy fault isolation for each channel. **Tele-Processing Products, Inc,** 4565 E Industrial St, Bldg 7K, Simi Valley, CA 93063. Circle 262 on Inquiry Card

LINE CONCENTRATOR

Statistical multiplexing techniques allow the Micro300 to combine 4 or 8 multidrop lines, each supporting polled terminals at speeds to 1800 bits/s, down a single high speed line operating synchronously at up to 4800 bits/s. Using the same hardware as the Micro800, the unit is optimized for use with polled terminals. No retransmission on error is provided for end-to-end between devices. **Micom Systems, Inc,** 9551 Irondale Ave, Chatsworth, CA 91311.

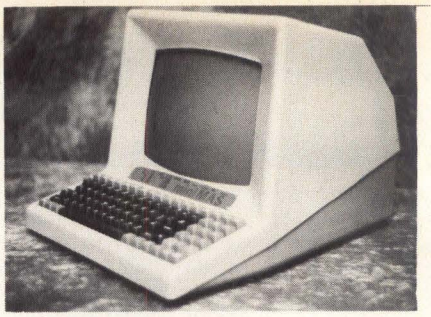
Circle 248 on Inquiry Card

CERAMIC PM DC MOTOR

Permanent magnet motor utilizes ceramic magnets for max torque and power with min losses. Torque constants of 3 to 75 oz-in (0.021 to 0.525 N•m)/A are offered, depending upon size, speed, and voltage. Other ratings include voltage of 12 to 130 Vdc and speed of 600 to 10k r/min. Available as enclosed or open construction, face or base mounted, the unit has a steel frame with aluminum end bells. **Electric Indicator Co,** 272 Main Ave, Norwalk, CT 06851.

Circle 249 on Inquiry Card

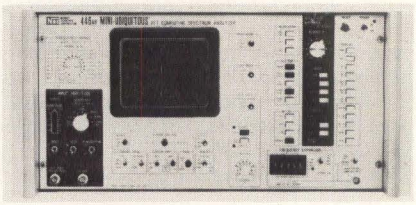
COMPACT CRT TERMINAL



For large volume applications, Z8 based miniMAS contains an external, wall mount power supply and a single 6 x 9″ (15 x 23-cm) logic/monitor board with 25 ICs. The 15-lb (7-kg), 14 x 12 x 18″ (36 x 30 x 46-cm) package includes a 12″ (30-cm) CRT, 7 x 9 ASCII dot matrix, 24 x 40 or 80 char, 25th line status display, 4k memory for 2-page display, inverse screen, and 16 baud rates. Software is supplied with the terminal. **Micro Application Systems, Inc,** 5575 N County Rd 18, Minneapolis, MN 55442.

Circle 250 on Inquiry Card

FFT ANALYZER FOR SYSTEM INTEGRATION



Upgraded realtime spectrum analyzer, 446AR, is configured for rackmounting in 8.75″ (22.23-cm) high space. A full IEEE 488 interface is built-in for remote control, sensing, and data transfers. Features are 400-line FFT analysis to 100 kHz, mathematical comparison of 2 stored averaged spectra, engineering unit calibration, and rms calculation of selected portions of the spectrum. **Nicolet Scientific Corp,** 245 Livingston St, Northvale, NJ 07647.

Circle 251 on Inquiry Card

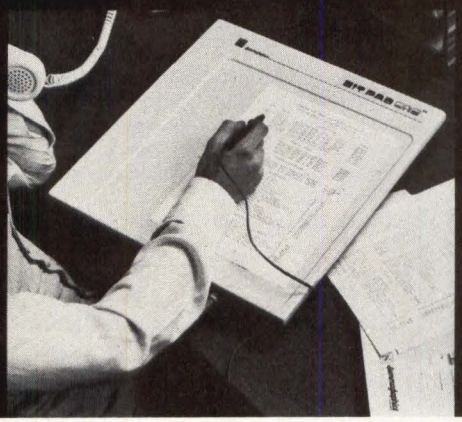
OPEN FRAME DC POWER SUPPLY

Designed to power micro- or minicomputer based systems, model OS150-06 has dc outputs of 5 V at 15 A, −5 V at 4 A, 12 V at 4 A, −12 V at 4 A, and 24 V at 4 A. Total max output power is 150 W. Specs are dual 115/230-Vac input (customer selectable), built-in overvoltage protection, foldback current limiting, 0.2% line and load regulation, 70% efficiency, and input surge protection. **Microcomputer Power, Inc,** 2272 Calle de Luna, Santa Clara, CA 95050.

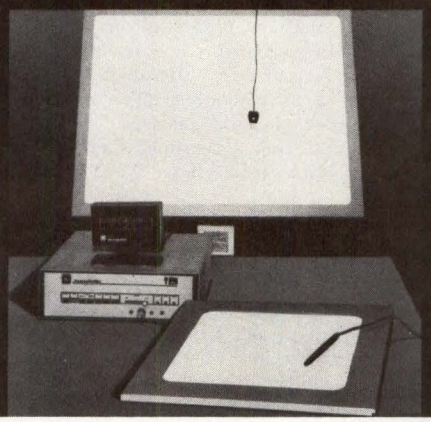
Circle 252 on Inquiry Card

from Apple to Zeta

When it comes to computer graphics, it all starts with Summagraphics.



Bit-Pad One



Intelligent Digitizer

Datagrid II, System 4

Beginning with the digitizer, of which it is the world's largest and most experienced manufacturer, Summagraphics has developed a complete range of graphic systems for both the OEM and end user.

From the simplest data input digitizer to complete stand-alone computer-aided drafting systems, each is designed to provide flexibility to meet your future needs, and each is very competitively priced.

Digitizers for data input. Summagraphics offers a complete family of digitizers for converting graphic information into digital form for processing and for speeding the entry of alphanumeric and programming information by eliminating keyboarding.

- Bit-Pad One provides an 11-inch by 11-inch tablet and resolution to .004 inch with a choice of RS-232, IEEE-488 or parallel-byte output.
- ID series data tablets provide similar resolution in tablets ranging in size up to 42 by 60 inches.
- Summagrid provides .001-inch resolution in back-lighted tablets as large as 42 by 60 inches.

CIRCLE 119 ON INQUIRY CARD

Intelligent digitizers incorporate microprocessors to automatically perform such functions as calculating areas, linear displacements and perimeters and for relocating origins, converting binary to BCD and formatting output data.

Preprocessing systems for remote job entry. Datagrid II, Systems 1 and 2, are designed for off-line digitizing and storage for subsequent entry into any graphic system or data base.

Preprocessing reduces communications and host processor loads.

Stand-alone computer-aided drafting systems. Datagrid II, Systems 3 and 4, are complete systems that provide computer processed solutions to a variety of drafting applications.

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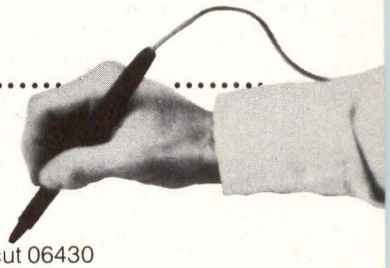

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☐ I would like information on the equipment checked below.
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My phone number is ( ) _____
☐ Digitizers ☐ Preprocessing for remote job entry ☐ Intelligent digitizers
☐ Stand-alone graphics systems

Name: _____
Department _____ Title _____
Company _____
Address _____
City _____ State _____ Zip _____

LITERATURE

Modems and Automatic Dialers

Featuring line of 1200-bit/s full-duplex modems, brochure also cites line of Bell compatible modems, CCITT compatible modems, automatic dialers, and a Multiline Automatic Calling System. **Racal-Vadic,** Sunnyvale, Calif.
Circle 300 on Inquiry Card

Industrial Microcomputers

Brief descriptions, options, and power requirements for industrial products ranging from microcomputers and power supplies to floppy disc subsystems and video terminals are given in catalog. **Process Computer Systems, Inc,** Saline, Mich.
Circle 301 on Inquiry Card

Personal Computers

Among the electronics kits and products described in catalog are personal computer system kits, and an educational program entitled "Computer Concepts for Small Business." **Heath Co,** Benton Harbor, Mich.
Circle 302 on Inquiry Card

Digital Electronic Training And Breadboarding

Photos, specs, and text in 44-p guide describe system of hands-on training and breadboarding products, textbooks, tutorials, seminars, and custom programs. **E&L Instruments, Inc,** Derby, Conn.
Circle 303 on Inquiry Card

Microcomputers

Presented in the 1980 catalog is the Model II business microcomputer; also described are the TRS-80 microcomputer system, Micronta test instruments, and tools, tubes, transistors, ICs, parts, plugs, and cables. **Radio Shack, a Div of Tandy Corp,** Fort Worth, Tex.
Circle 304 on Inquiry Card

Distributed Data Processing

Brochure outlines major differences between IBM's DPD and CSD products and Data General's Eclipse® and Commercial Systems that are designed for distributed processing applications. **Data General Corp,** Westboro, Mass.
Circle 305 on Inquiry Card

Communications Products

System diagrams in brochure illustrate flexibility of 6000 series communications frontend and intelligent network processors and statistical multiplexers. **Codex Corp,** Mansfield, Mass.
Circle 306 on Inquiry Card

MPU Board Test

Guide analyzes properties of MPU based systems and explains how testing problems can be solved using MicroSystem Analyzer for in-circuit emulation, signature analysis, and time domain analysis. **Millennium Systems, Inc,** Cupertino, Calif.
Circle 307 on Inquiry Card

Optoelectronics

In sections covering fiber optics, solid state LED displays and lamps, optocouplers, and emitter/detectors, 384-p source book provides photos, dimensions, operating characteristics, and performance graphs. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 308 on Inquiry Card

2-Wire Transmitters

Diagrams and text in technical paper explain basic operation of 2-wire transmitters for amplifying and transmitting low level process sensor signals. **Action Instruments Co, Inc,** San Diego, Calif.
Circle 309 on Inquiry Card

Static RAMs

Standard and low power versions of 1024 x 4-bit, TTL NMOS in/out, static RAMS are covered in data sheet containing parameters, characteristics, specs, timing diagrams, and pin configurations. **EMM SEMI, Inc,** Tempe, Ariz.
Circle 310 on Inquiry Card

Data Multiplexers and Concentrators

Equipment catalog encompasses Microplexer™ statistical, Timeplexer™ time division, and Lineplexer™ 19.2k-bit/s inverse multiplexers, as well as B101™ bit interleaved multiplexer for Telex networks. **Timeplex, Inc,** Rochelle Park, NJ.
Circle 311 on Inquiry Card

Speech Compression and Pitch Shifting Modules

Data sheet describes M8-A that lowers a pitch to as little as ⅓ of the original, and the M8-B that compresses speech to be intelligible at 2 to 3 times the original recording speed. **Variable Speech Control Co,** San Francisco, Calif.
Circle 312 on Inquiry Card

Scientific Instruments

Summary of electrometers, nanovoltmeters, current and voltage sources, picoammeters, and milliohmmeters provides performance features and key specs for more than 30 models. **Keithley Instruments, Inc,** Cleveland, Ohio.
Circle 313 on Inquiry Card

Electronic Packaging Hardware

IC sockets, dual in-line packaging, cards and panels, plus card file components and assemblies, are illustrated with dimensional drawings. **Scanbe, Div of Zero Corp,** El Monte, Calif.
Circle 314 on Inquiry Card

Computer Graphics Software Systems

Booklet explains advantages of graphics and the flexibility of the DISSPLA® and TELL-A-GRAF® systems that turn volumes of statistics into charts and graphics. **Integrated Software Systems Corp,** San Diego, Calif.
Circle 315 on Inquiry Card

Data Processing Training

Discussed in progress report are adaptations of data processing training programs presented at six companies; also described is the Resource 12 library of more than 2000 multimedia courses and programs. **Deltak, Inc,** Oak Brook, Ill.
Circle 316 on Inquiry Card

Custom Modems

Brochure describes company's capability to design and supply custom modems, automatic alternate voice-data modem sets, and network control systems. **Intertel, Inc,** Burlington, Mass.
Circle 317 on Inquiry Card

SELECTABLE STORAGE. AMPEX MAKES IT. AND MORE.

Selectable storage means getting as much disk as you need. But not having to buy more than you want.

Ampex disk storage modules are available in six models in two distinctive series. Choose from the DM-900 family; 5-high disk packs, with capacities of 40, 80 or 160 megabytes, for rack, console or table-top mounting.

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Selectable storage. It's just one of the surprising Ampex line of digital systems products. From plug-compatible memories for nearly any CPU you can name, through a wide range of tape peripherals. Even intelligent controllers, our own minicomputer, and completely-packaged, all-Ampex minicomputer systems.

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CIRCLE 115 ON INQUIRY CARD

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

Our Wildest Card Yet

A programmable 16-line multiplexer that beats everything in its class*

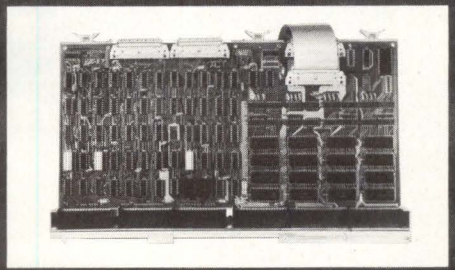
PDP-11 users, we have another winner for you. This time it's DMAX/16™, our new programmable multiplexer for connecting your PDP-11 to 16 asynchronous serial communications lines. DMAX/16 makes the most of the 11's DMA capabilities to establish computer overhead at a level far below that of competitive units like the DJ11 and DZ11. It also offers software compatibility with the DH11... in one-fourth the space!

Now, for the first time, you don't need an expansion box or special back planes. DMAX/16 consists of two hex boards which install easily into standard SPC slots and connect to the current loop or EIA/RS-232 panel by separate flat-ribbon cable. As many as 16 units can be placed on a single PDP-11 for a total of up to 256 lines. A DMUX/16™ option allows modem control for 16 channels.

DMAX/16 provides complete program control of the lines, each of which operates with several individually programmable parameters, such as character length and number of stop bits. Parity generation and detection are odd, even or none. The operating mode is half duplex or full duplex. Fifteen software programmable baud rates: 0 to 9600 baud – plus 19,200 baud – and an external baud rate. Breaks may be generated or detected on each line and the unit can echo received characters without software intervention.

Play the wild card now. You'll get top performance and a competitive price advantage of at least $1000 along with delivery from stock as usual. Write for details and find out why we consider ourselves the leader among manufacturers of DEC enhancements.

Able Computer Technology, Incorporated,
1751 Langley Avenue, Irvine, California 92714.
(714) 979-7030. TWX 910-595-1729



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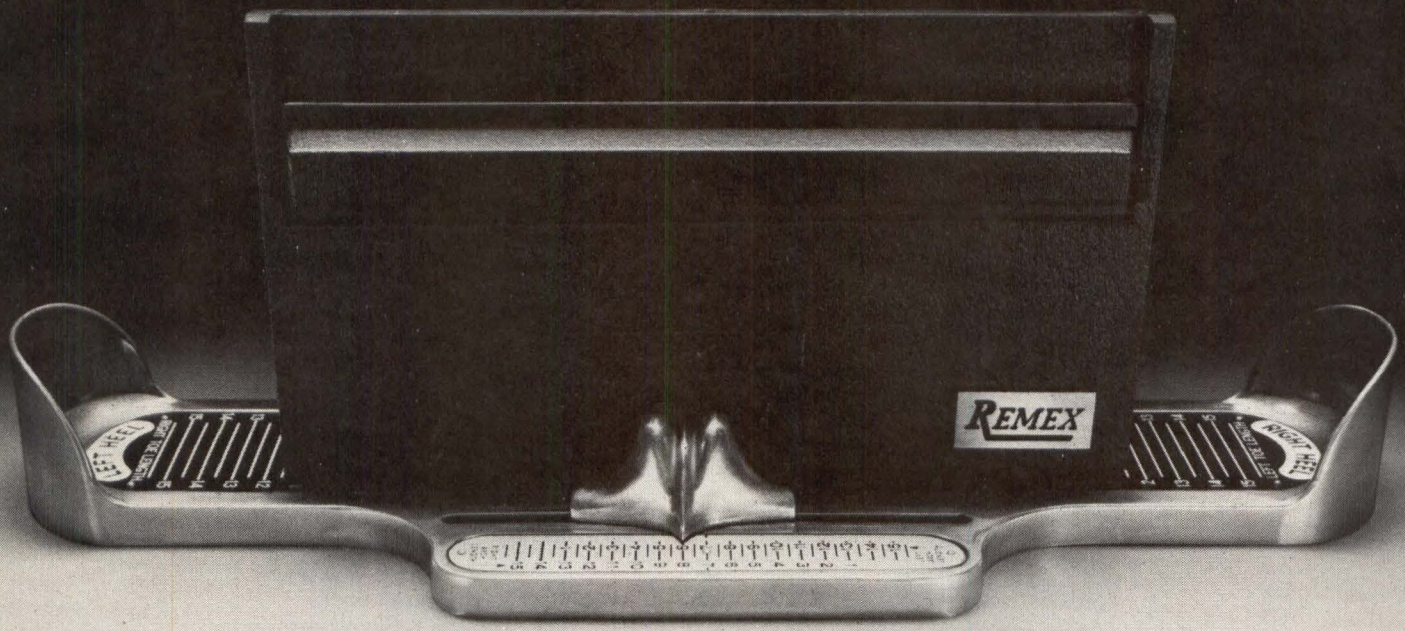
You will save half your bandwidth or run at twice the speed! Able does it again!

CIRCLE 117 ON INQUIRY CARD

If the Shugart fits...



If you've taken a shine to Shugart, you're in luck.

Specifying Shugart means you're also specifying Remex. We're your alternate source for fast, volume delivery.

Remex single and dual-headed drives, single or double density, are physically and electrically compatible to Shugart SA850R/851R units. So you can switch over to Remex without re-design.

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What's more, Remex has solved the dual-head media wear problem for good with a new, improved head and carriage assembly.

So remember this: If the Shugart fits, Remex fits, too.

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REMEX DIVISION

DATA WAREHOUSE

CIRCLE 114 ON INQUIRY CARD

GUIDE TO PRODUCT INFORMATION

NEVER HAS ONE CARD HELD SO MUCH ON SO LITTLE.

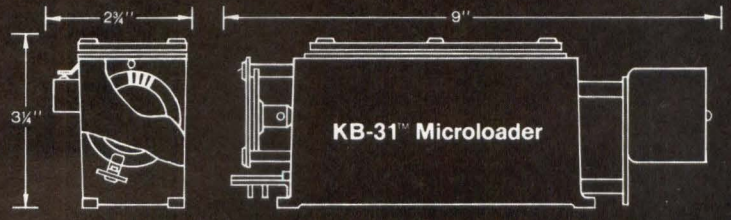
THE KILOBYTE CARD™ INCREASES THE SPEED AND LOWERS THE COST OF THOUSANDS OF DATA LOADING APPLICATIONS.

The challenge in more and more product designs is to increase the ease and efficiency of data loading while holding a tight line on costs.

Vertel's exciting new Kilobyte Card/KB-31™ Microloader Technology offers you the ultimate solution to today's challenge. This unique combination allows you to record 1088 8-bit bytes on the durable 4-stripe Kilobyte Card.

The KB-31 reader/writer features a shaft encoder, developed by Vertel to provide data accuracy during the write cycle regardless of head speed.

And the KB-31 holds the line on price—as little as $169 in OEM quantities.



Read/Write Cycle Time: 272 bytes per stripe, 5 seconds per stripe.
Reading System: Stationary Card, Moving Head.

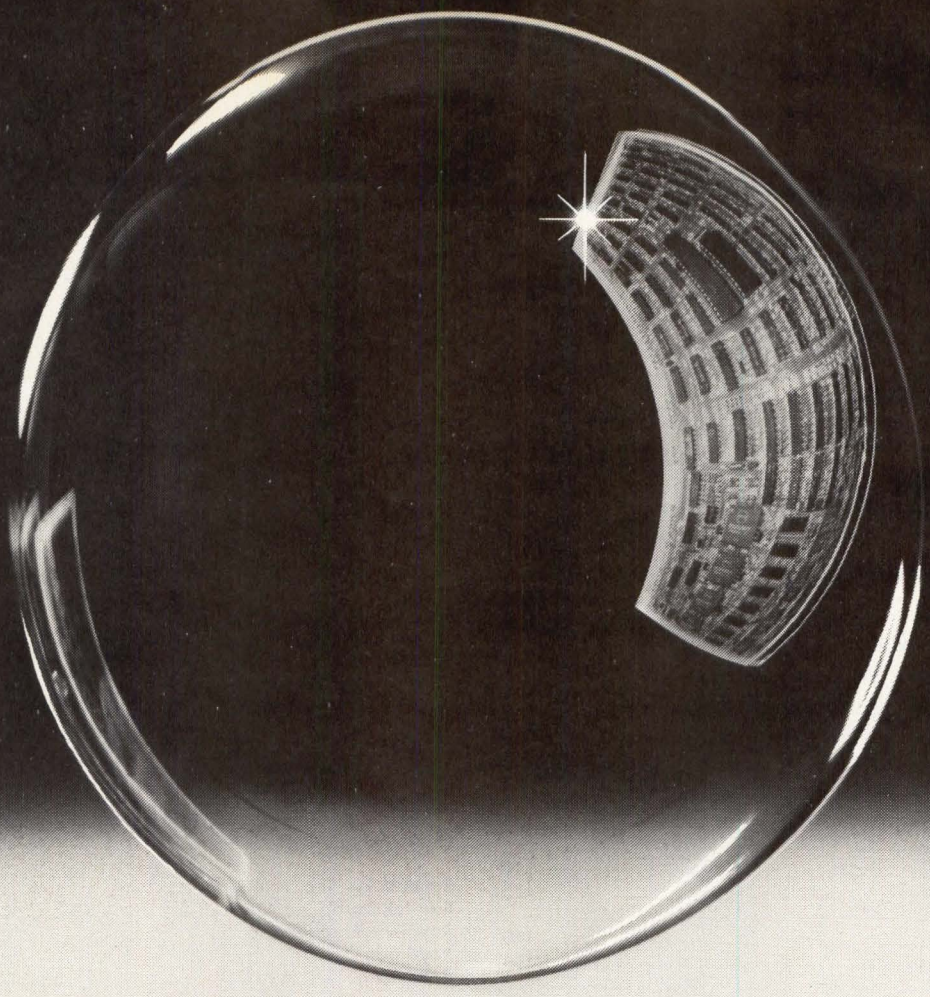
For complete specifications on the Kilobyte Card, the KB-31 Microloader and our RW-31 Credit Card reader/writer, send your request on your company letterhead to:

VERTEL

125 Ellsworth Street
Clifton, New Jersey 07012
(201) 472-1331

CIRCLE 121 ON INQUIRY CARD

GUIDE TO PRODUCT INFORMATION



Plessey bubble memories

standard add-ons and custom-built

Now you can confidently incorporate magnetic bubble memories in your next product development: Plessey is fully equipped to design and produce to your spec. Or you can buy add-in bubble memory cards for your Intel SBC systems. Plessey has a range of compatible systems actually in production. Shouldn't you be talking to us now?

Here are some Plessey bubble memory pluses:

- Rugged, maintenance-free, non-volatile storage at a lower cost than CMOS + battery.
- More compact, more reliable and faster than disc or cassette.
- 64 k or 256 k byte Multibus*compatible cards.
- Software compatible.
- Low power requirement.

Reliable products from a specialist manufacturer with many years' experience of standard and custom-built memories—Made from both magnetic and semiconductor devices.

Contact Plessey Microsystems sales office to discuss your needs for the future, or send for your copy of the Bubble Memory Systems literature folder.

PLESSEY
MICROSYSTEMS

Plessey Microsystems Inc., 19546 Clubhouse Road, Gaithersburg, Maryland 20760.
Telephone: (301) 948-2791. TWX: 710 828 9708
and at 1641 Kaiser Avenue, Irvine, California 92714.
TWX: 910 595 1930.

Plessey Microsystems Limited, Water Lane, Towcester, Northants NN12 7JN.
Telephone: Towcester (0327) 50312. Telex: 31628.

CIRCLE 122 ON INQUIRY CARD

*Intel trademark.

ADVERTISERS' INDEX

*Appearing in domestic issues only

Panasonic electrosensitive alphanumeric printers.

When you're this small, you don't have to make a lot of noise about your low price.

Print in silence and print at low cost with our electrosensitive alphanumeric-plus printer Model EUY-10E.

Naturally, you'll like the price. But that's not the major benefit.

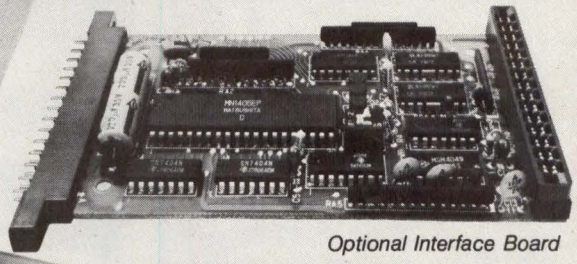
It isn't even the fact that the package is small (4.33″L x 3.5″W x 1.5″H). That makes it great in tight applications like POS cash registers, electronic calculators, data loggers, home computers and general peripherals—anywhere, in fact, where inexpensive hard copy is required.

The real achievement was to pack so much character-forming flexibility in that tiny space. We did it, with a 5 x 7-dot matrix that prints up to 128 different characters or symbols (including a full ASCII character set) on either 15, 21, 32 or 40 characters per line at just 530 msec per line with legibility that's sharp and clear.

There are two versions to choose from, each with reliability designed-in by eliminating all moving parts except the print head and the paper.

To make it easier for you to get rid of noise, bulk and big price tags, we've also made the EUY-10E easy to talk to. For quick microprocessor compatibility, we supply a 4-bit 1-chip microcomputer on a pre-programmed plug-in board that meets a variety of interfacing requirements, including that 128-strong variety of character formations.

For specifics on how beautiful small can be, write for information and prices to: Panasonic Electronic Components, One Panasonic Way, Secaucus, NJ 07094; or call (201) 348-7282/7289



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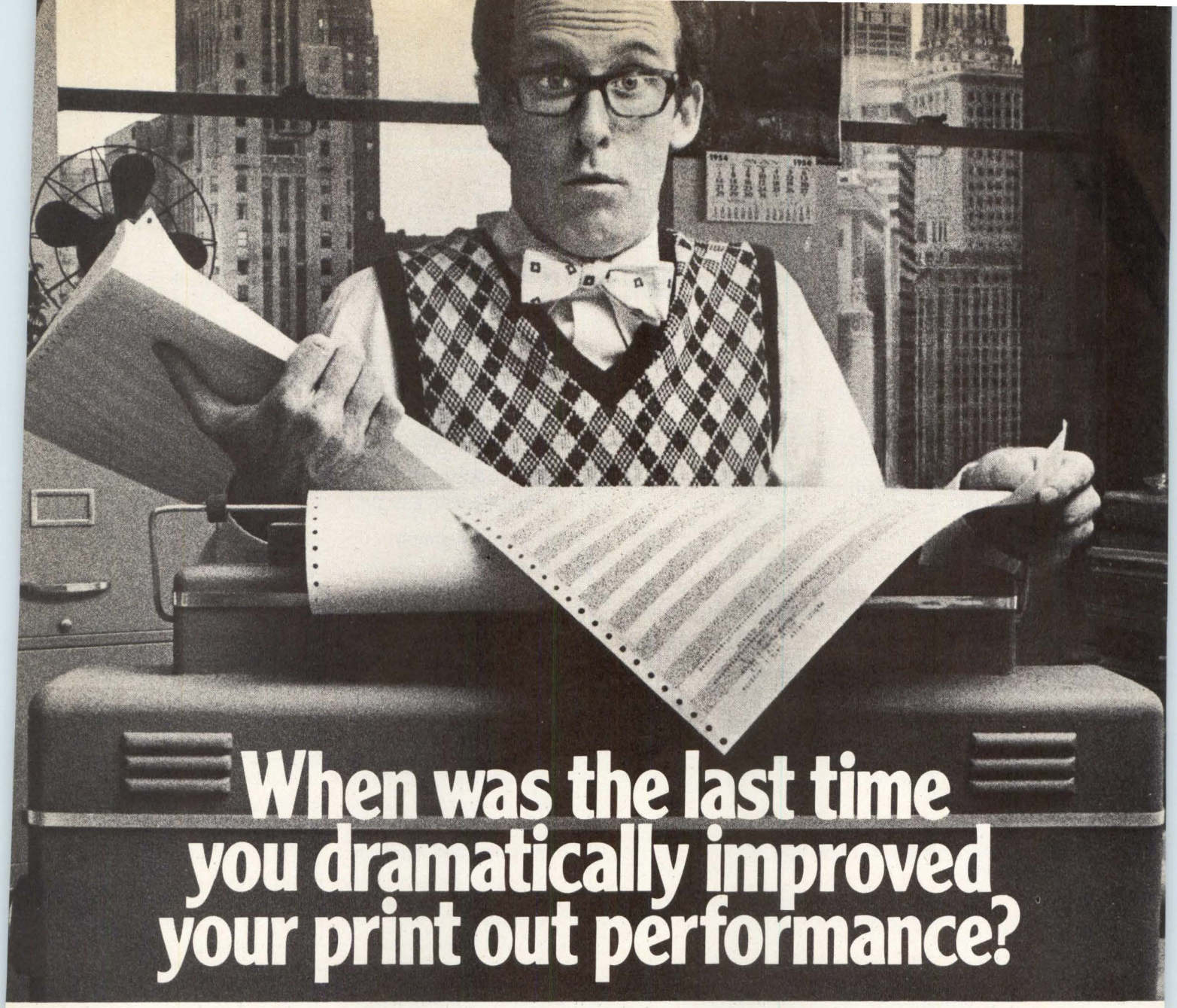
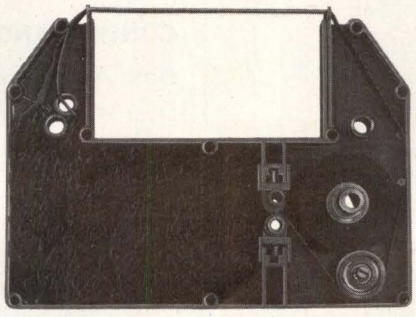


When was the last time you dramatically improved your print out performance?

Today's measure of a printer's performance goes beyond line speed and purchase price. A revolutionary Porelon reinking system now adds a new dimension to print out performance. It will dramatically increase the printing life of the ribbon in your impact printer and substantially reduce character cost.

Porelon's unique ribbon reinking system automatically begins to reink the impact printer's ribbon only after reinking becomes necessary. This is made possible through a patented delayed engagement device. The printing life of the ribbon is maximized and printouts continue to be crisp and clean for a longer period of time.



Find out how simple it is to add this performance feature to your impact printers. Your competition may already be considering it. Call (615) 432-4134. Or write Porelon, Inc., Cookeville, Tennessee, 38501, for further information.

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CIRCLE 126 ON INQUIRY CARD

1979 Computer Design Index

Annual listing of editorial feature articles and columns by subject and by author

SUBJECT INDEX

AED ANNOUNCES ITS NEW DEC TEAM.

Single card RM-02® emulation

The fullback for the PDP-11 team is AED's new STORM-02, a hex-card controller/formatter for storage module drives.

We tried out a lot of fullbacks for the team but STORM-02 was the only player that could offer everything! Single hex-card electronics; RH-11, RM-02 and RM-03 emulation; the ability to plug right into the SPC slot on your PDP-11; plus the ability to get along with the media. That's the kind of compatibility we like!

A standard single board STORM-02 handles 4 SMDs. With an optional second hex-card, the STORM-02 can accommodate four more drives for a total capacity of over 500 megabytes.

Our big surprise was the bottom line on the contract. The OEM price for the STORM-02 is just $2370 for the hex-card electronics — far less than any fullback in the league. The complete system with one 80-megabyte storage module drive, in quantities of one, is $13,500 . . . about half the price of a comparable DEC fullback.

For the complete statistics and quick delivery, call or write Bob Deisher, Rigid Disk Products Manager.

ADVANCED ELECTRONICS DESIGN, INC.

COMPUTER PERIPHERALS DIVISION
440 Potrero Ave., Sunnyvale, CA 94086
Phone 408-733-3555, Boston 617-275-6400

RL-01® compatible Winchester

The linebacker for our LSI-11 team, the WINC-01, is surprisingly small for a pro. He consists of just two PCBs — one a microprocessor-based formatter/controller mounted with a SA-4008 drive, and the second, a dual-width Q-BUS interface card that inserts directly into the CPU backplane.

However, when WINC-01 proved he could deliver Winchester technology to DEC LSI-11, -11/2, -11/23 users, we signed him up immediately. He amazed us by playing with up to three SA-4008 Winchester drives and tackling up to a total of 60 megabytes of data. Additionally, he has the capacity to include a plug-in floppy disk drive.

Best of all, he bunked with the DEC RL-01 driver software and we can report they are very compatible up to 20 megabytes.

In contract talks, the WINC-01 demanded considerably less than the DEC hardware: his two boards sell together for under $1150 in OEM quantities. The complete system, including the two PCBs, an AED power supply, one SA-4008 drive and a DEC look-alike cabinet sell for $6700 in quantities of one.

For WINC-01 technical information and quick delivery, contact Bob Deisher, Rigid Disk Products Manager.

Full color graphics system

The coach of PDP-11's team is our new AED512 graphics generating system that makes the blackboard obsolete. Now, when he plots the plays, the FIVE TWELVE's compact video terminal will display all the action in high-resolution detail using up to 256 simultaneous colors and 16.8 million different hue/intensity combinations on a 512 x 480 pixel screen. The AED512 is microprocessor controlled, and has the largest refresh memory of any system in the league.

Other features that make the new PDP-11 'coach' a cost/performance leader include:

- DMA interfaces (Q-BUS® or UNIBUS®) available.
- 2:1, 3:1 . . . 16:1 zooming. Panning via integral joystick.
- Vector and circle generation. Curve fill. Single-point addressability.
- Crosshair cursor with programmable color.
- SUPEROAM panning over 1024 x 2048 contiguous pixels.
- Programmable character fonts and 8 programmable special function keys.
- $6,875 with two colors only, excluding monitor and DMA.

For delivery information, write or talk to Jerry Kennedy, VP Marketing.

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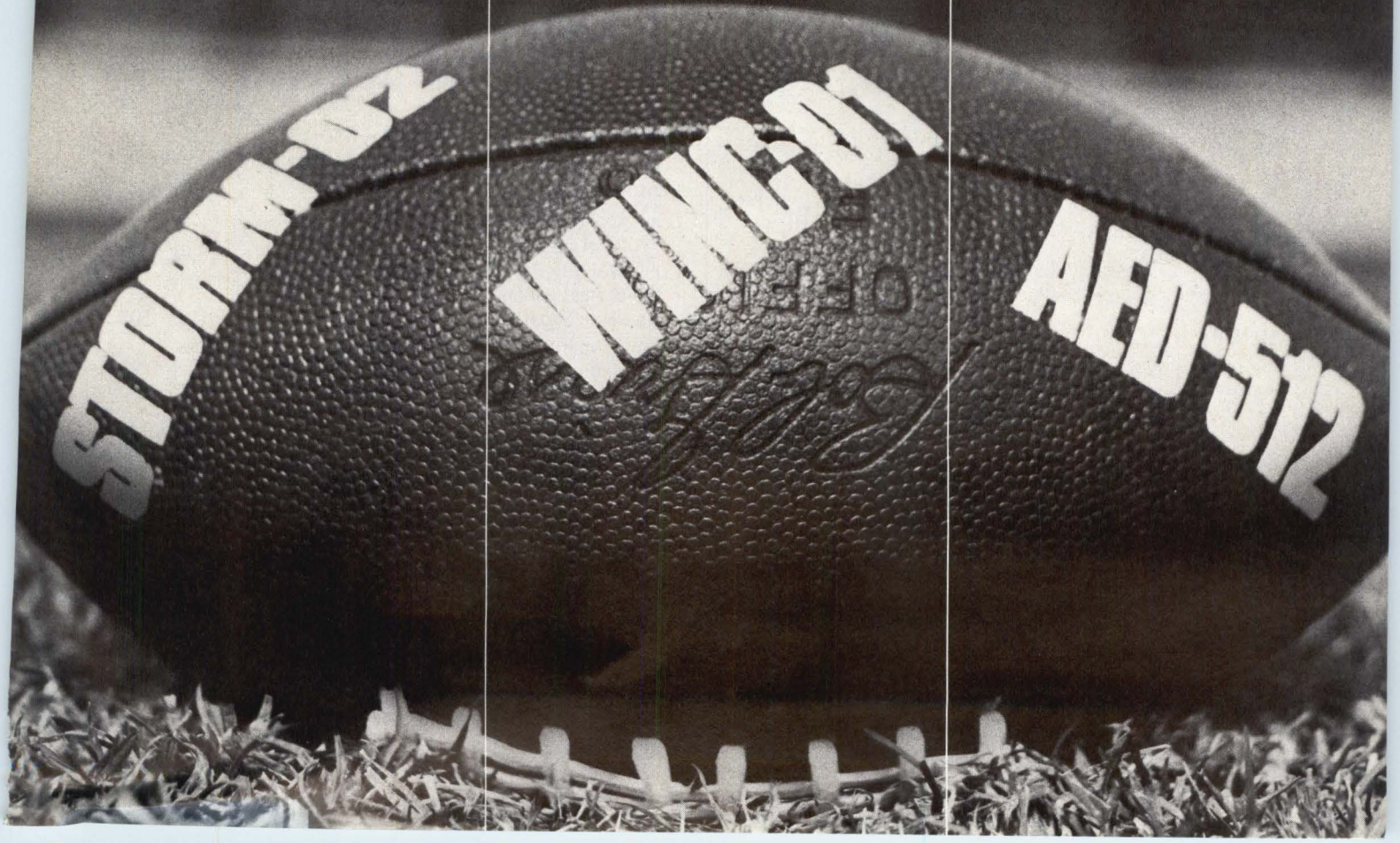
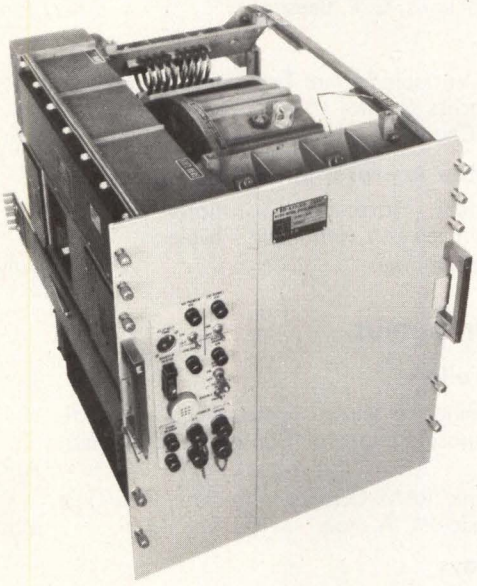
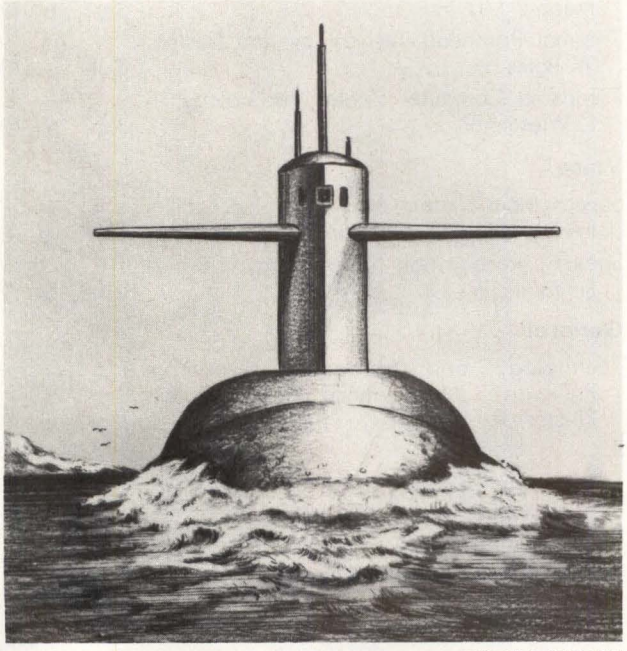
CIRCLE 127 ON INQUIRY CARD



Librascope's RD-433 Militarized Mass Memory Goes Anywhere The U.S. Navy Goes.



THE dependable Mass Memory subsystem the ultimate in data reliability for shipboard and submarine installations to interface the Navy's standard computers. This specially configured model for the Shipboard Tactical Intelligence (TACINTEL) program is listed in the Navy's inventory under the military designation RD-433 (XG-1)/SSH. TACINTEL is one of the latest operational systems in the Fleet Satellite Communications (FLTSATCOM).



Installed in any compartment on board a ship, the RD-433 fits in an open standard 19″ Retma rack, meets MIL-E-16400, Class 4, operational requirements in free air ambient 0°C to 50°C, and withstands MIL-S-901C drop hammer shock. The system is also humidity and drip proof, and EMI/RFI secure without additional enclosure just as shown in the photograph.

Modularly designed for easy on-call maintenance, no preventative maintenance is required. The controller is made up of low-cost SEMS (the Standard Electronic Modules developed by NAFI), with low power Schotky integrated circuits.

Other production Mass Memories such as the Model CL107MA, are used in the Integrated Radio Room (IR^2) of TRIDENT submarines and in a new torpedo fire control system for the Royal Australian Navy. Librascope's mass memories are on board in many other U.S. Navy programs such as, for example, the prominently successful BQR-24 program.

Call or write today for additional information on these rugged, reliable Militarized Mass Memory Systems.

The Singer Company, Librascope Division, Department N, 833 Sonora Avenue, Glendale, California 91201. Telephone (213) 244-6541, extension 1891.

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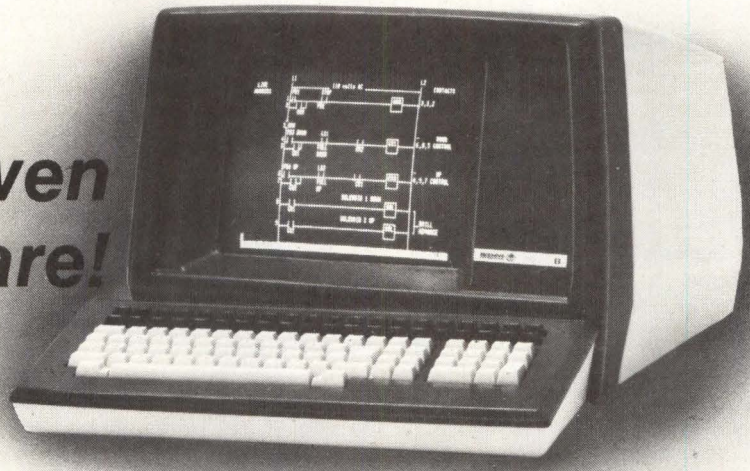

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The STORAGE DEMON is fully supported by SOFTWARE DYNAMICS' new SDOS interrupt-driven disk operating system. It features:

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- ☐ Automatic Disk Read-ahead
- ☐ Automatic Disk Sector Pooling
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- ☐ Complete Device Independence

SDOS supports EXORdisk™ I, II, and III, and permits you to use your existing floppy disk drives for additional memory storage and/or as back-up for the Winchester hard disk. The STORAGE DEMON utilizes the field-proven, dependable LOBO DRIVES INTERNATIONAL 10 Megabyte hard disk and controller and comes with the famous LOBO DRIVES 1 year, 100% warranty.

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Introducing

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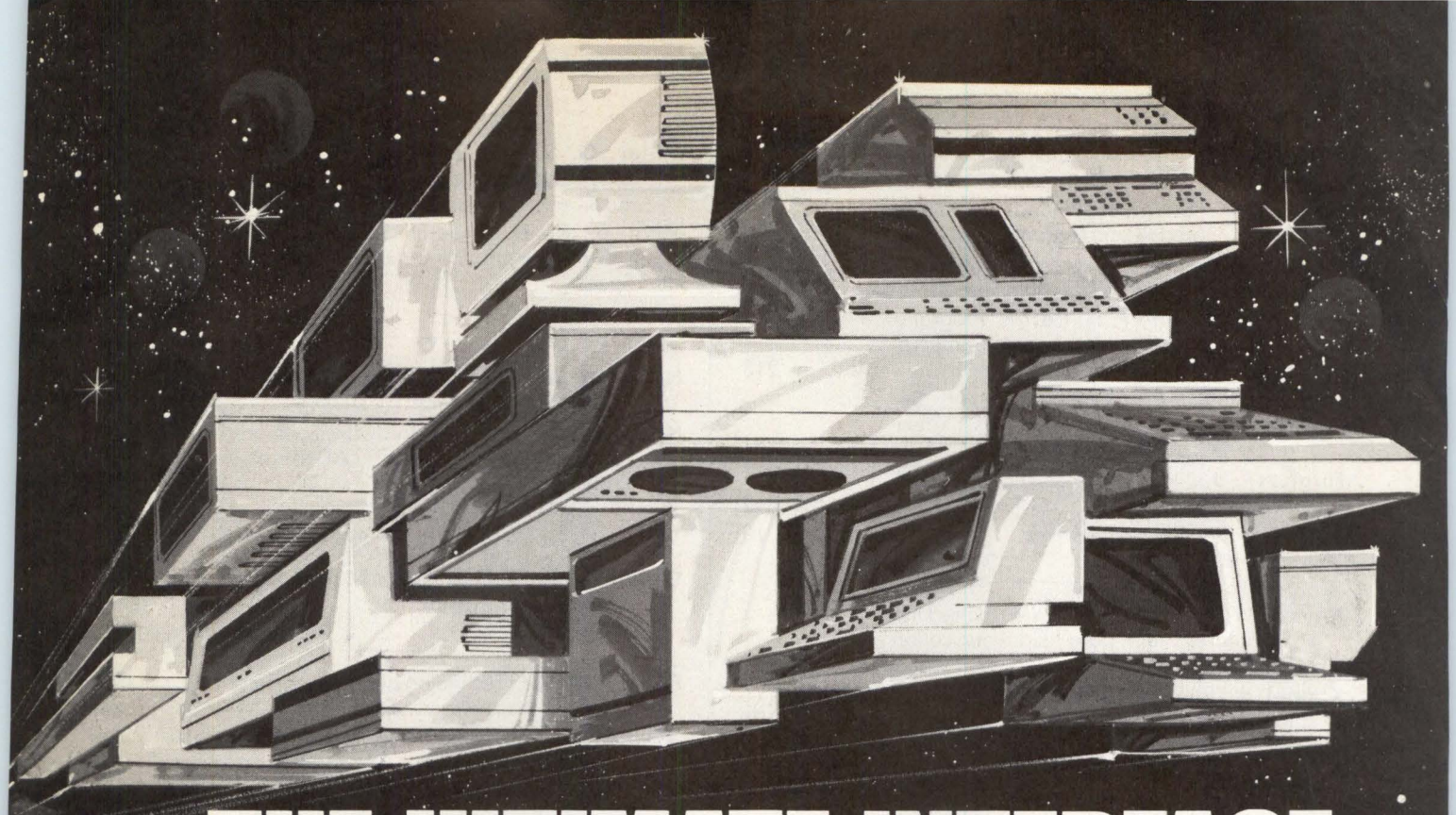
AUTHOR INDEX



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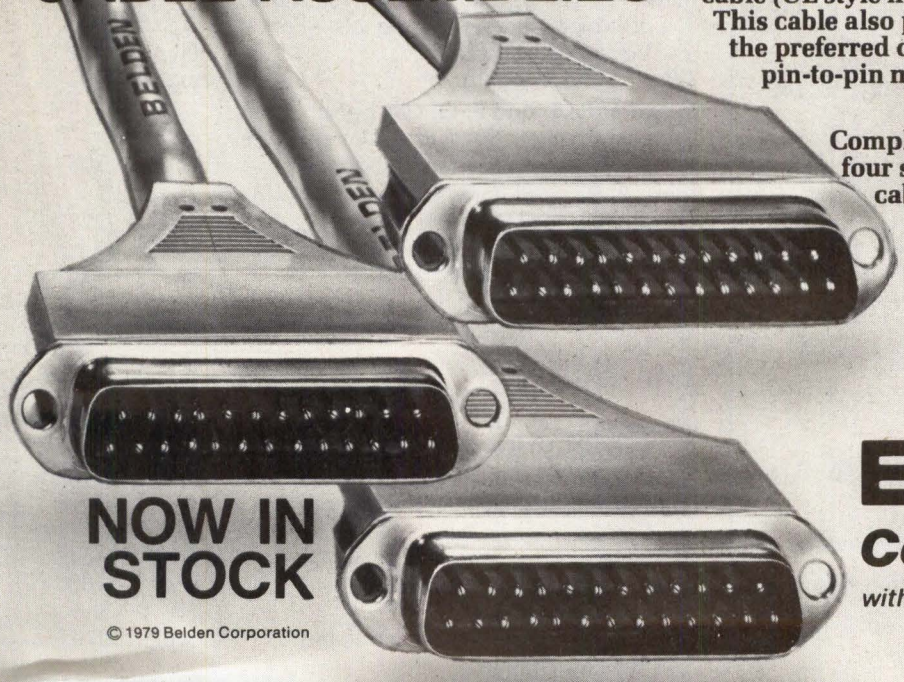
It's fast. Simple. Reliable. Accurate. In fact, it's the ultimate interface for your data terminal and communications equipment employing serial binary data exchange.

Belden's new 25 conductor molded cable assemblies are designed and built to meet EIA standard RS-232-C and types A through M standard interfaces.

These are cables you can count on. Belden's rugged 8459 cable (UL style number 2576) is used in these assemblies. This cable also passes the FR-1 vertical flame test and is the preferred cable for critical interfaces. And positive pin-to-pin mating using subminiature "D" type plug connectors means no mix-up.

Complete cable assemblies are now in stock in four standard lengths of up to 70′ (21m). Bulk cable is available in put-ups of up to 1000′. Custom designed assemblies are also available on special request. Belden Corporation, Electronic Division, P.O. Box 1327, Richmond, IN 47374; 319-966-6661. Out West contact our Regional Sales Office in Irvine, CA 714-833-7700.



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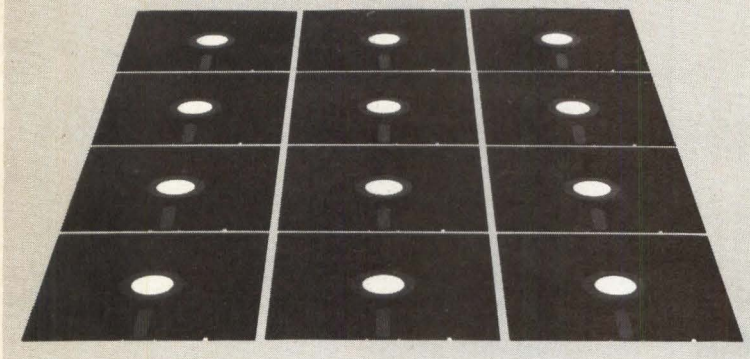

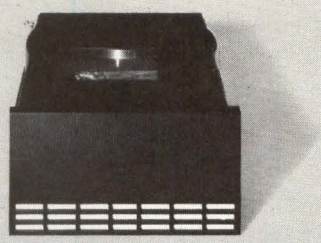

Meet the Mini Wini.™ The new 8" fixed disk drive that stores 20 megabytes.

It's the lowest-cost way of getting 20 megabytes in an 8" floppy slot. And with Winchester-type technology, to boot.

So you can expand the on-line capacity of your present desk-top system without having to redesign one bit of your present chassis.

Interfacing?
It's a snap. The Mini-Wini (alias the PCC D8000 fixed disk) has a microprocessor-controlled interface, featuring a bidirectional command/status bus and serial data transfer. It's easier and simpler to design the CPU interface.

And maybe best of all, it's made by Pertec Computer Corporation. At PCC, we don't just innovate. We have the production capacity to supply those innovative products when we say we will. Which is reassuring.

The PCC Mini-Wini. Small size. Big capacity. Call us for details.

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CIRCLE 133 ON INQUIRY CARD

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"WE OFFER YOU A SELECTION...

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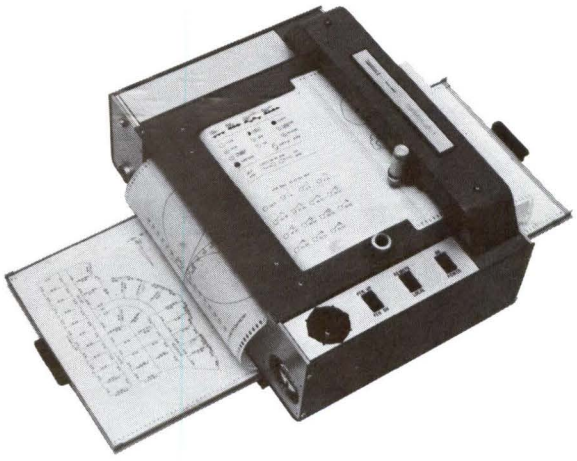
CØMPLØT electrostatic plotters and plotter/printers are available with models for printing (2,400 lines per minute on 8½" fan fold paper or 1000 lines per minute on 11" paper); plotting (2" per sec. on 8½" paper or 1.5" per sec. on 11" paper); or simultaneous plotting and printing.

CØMPLØT electrostatic CRT copiers provide fast, quality hardcopies from Hewlett Packard Series 2640 terminals or Tektronix® 4010 family terminals at only a few cents per copy. Prices for the Houston Instrument electrostatic products range from $3,450 to $5,975.*

The new Model 6000 TISPP Thermal/Intelligent/Strip/Plotter/Printer lets you get quality graphics output from either an analog or digital source and provides the continuity and clarity of a continuous trace with alphanumeric annotations under intelligent control. It's the ideal graphical output device for the new generation of microprocessor controlled instrumentation. Available in one or two pen versions. Prices start at $1,640.**

So... when you think of graphics, think of HI.

For complete information on any of Houston Instrument's digital plotters, printers, and plotter/printers, contact Houston Instrument, One Houston Square, Austin, Texas 78753. (512) 837-2820. For rush literature requests call toll free (outside Texas) 1-800-531-5205.



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